SoLID DAQ

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SoLID collaboration
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Outline

- R&D
- GEM
- Cerenkov
- TOF MRPC
- SPD
- Calorimeter
- possible ASIC SBIR
- Conclusion

R&D plan

- Mitigate issues
  - GEM max rate
  - DAQ deadtime for PVDIS
- Improve performance

- Test runs

GEM

- Simulation
- Rate limitation APV25
  - 100 KHz 1 sample for SIDIS, 200 KHz desired
  - 60 KHz 3 samples for PVDIS (is 3 samples enough ?)
  - Data reduction : being developped for SBS (1st version end of October)
- New chips : SAMPA, VMM3
- Deadtime for PVDIS asymmetry measurement

Cerenkov

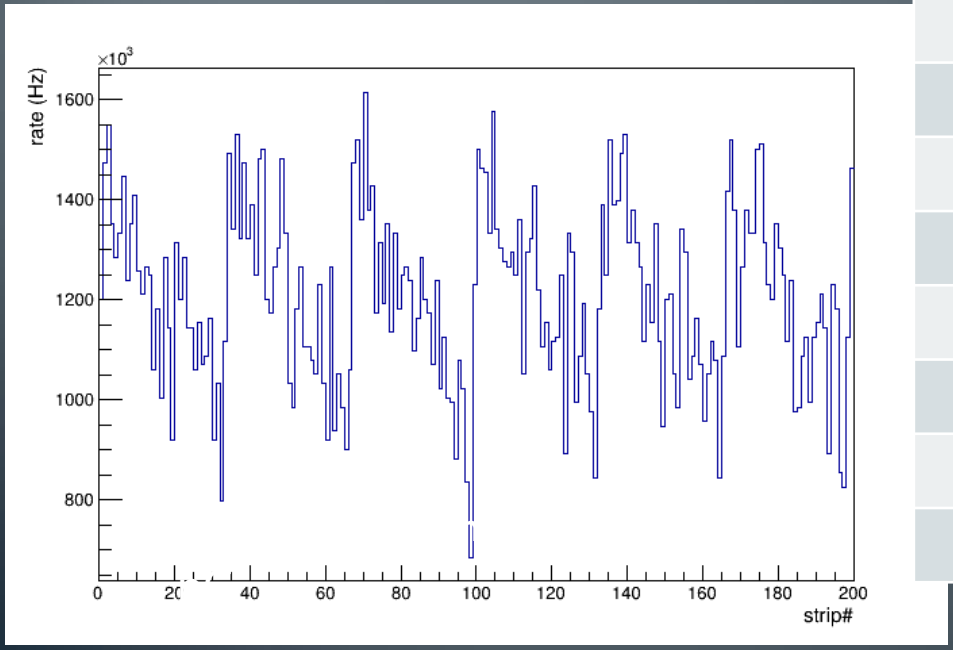
- Simulation
  - pixel readout needed ?
  - hit vs amplitude : FADC vs TDC only option
- Hardware
  - Sum of 64 pixels : passive possible, ASIC
  - MAROC option : test analog sum
  - MAROC option very likely : INFN redesigning board for CLAS12 RICH (new packaging) following up include sum
  - FADC ASIC
  - TDC ASIC

Time of flight

- Simulation
  - TDC vs sampling
- Hardware
  - need new chip to handle rate DRS5 or AARDVARC or other
  - Beam test : ensure time resolution reachable in realistic condition

Single rate

- Beam on target
- Average rate/channel:
  - total induced charge > 0.0 pC: 1.2 MHz
  - total induced charge > 0.5 pC: 893.2 kHz

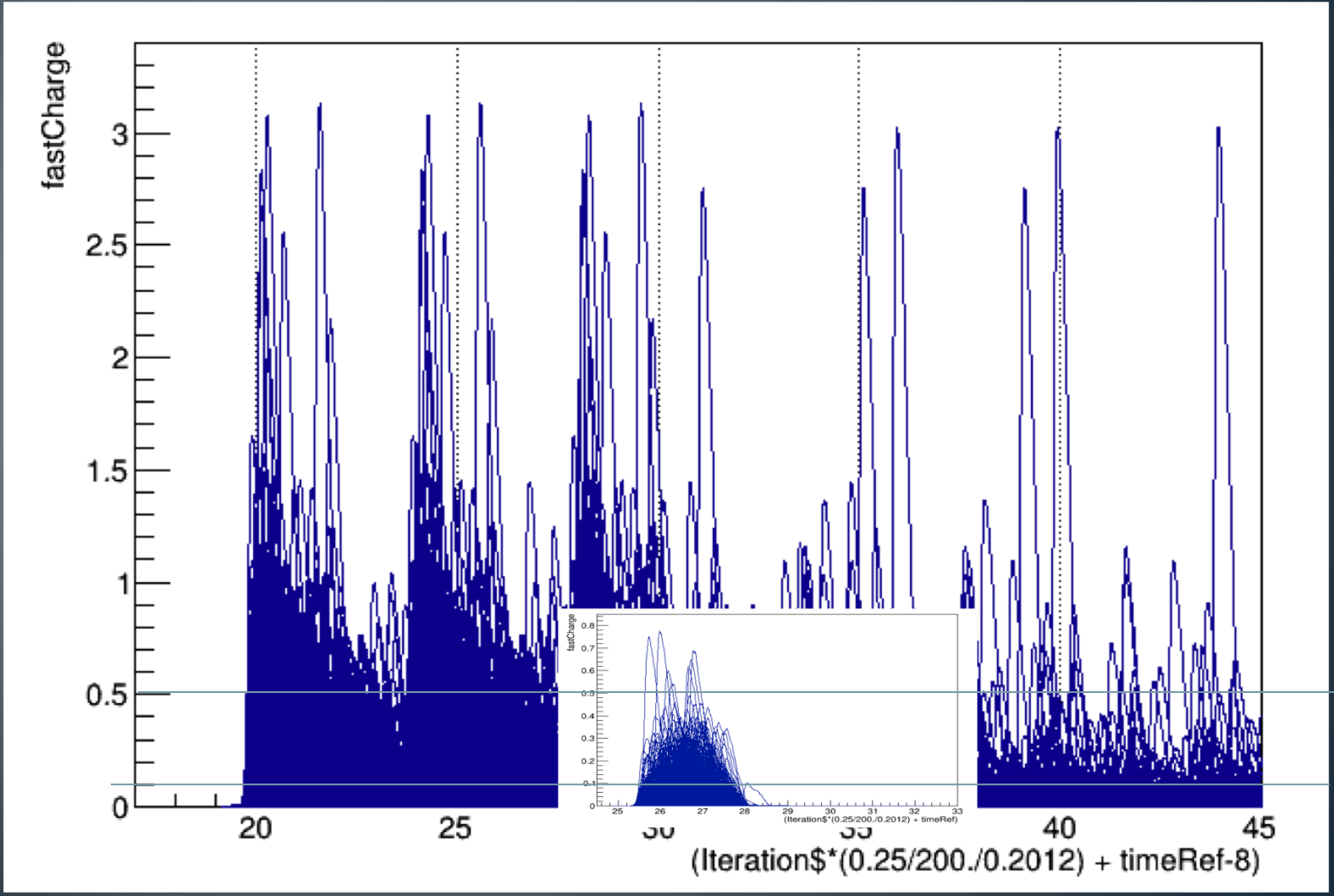


total induced charge cut (pC)	Average rate / channel (MHz)
0.0	1.20
0.1	1.11
0.2	1.06
0.3	1.00
0.5	0.95
0.6	0.84
0.7	0.80
0.8	0.76
0.9	0.72
1.0	0.69
1.1	0.65

Rate (kHz)/cm^2

Charge > cut	Rate (kHz)/cm^2	
	R = 96 cm	R = 105 cm
No cut	656	539
Charge > 0.00	38.7	36.3
Charge > 0.10	37.1	34.8
Charge > 0.20	35.6	33.0
Charge > 0.30	33.8	31.5
Charge > 0.40	32.3	30.1
Charge > 0.50	31.0	28.4
Charge > 0.60	29.6	27.5
Charge > 0.70	28.1	26.4
Charge > 0.80	27.0	25.6
Charge > 0.90	26.1	24.7
Charge > 1.00	25.2	23.6

Pulse background beam on target shifted -4ns -8ns



SPD

- Simulation
  - occupancy an issue ?
  - readout waveform : is that enough ?
- Hardware
  - gain
  - beam test
    - background
    - timing resolution

Calorimeter

- Simulation
  - digitization : PID sufficient ?
- Hardware
  - gain, amplifier
  - SiPM option

Electronics

- Full deadtime of DAQ chain
  - false asymmetry in PVDIS
  - FADC : DAQ group helping
  - GEM ?
- Simulation
- Test with fake signal
- Beam test

Computing ressources

- After CD0, can have concrete plan for ressources
- Network
- SILO
- Computer ressources

- Most likely able to handle SoLID requirements
- Data challenge : test experiment rate from Counting House to Silo

Discussion Summary SBIR with Alphacore

E. Mikkola and A. Camsonne discussed the following topics:

1) SoLID GEM tracker detector needs 160k channels to be read out. Ideal solution would be a 64-channel chip that has preamps, shapers and 40MSPS ADCs. Alphacore's current STTR Ph1 program provides 32-channel preamp+shaper chips with 100ns rise time and 32-channel 50MSPS ADC chips with 9.5 ENOB. Questions: Are these specs acceptable ? What is the expected input pulse rate ? What is the detector capacitance of these particular GEM detectors? Radiation hardness requirement?

2) SoLID Cerenkov readout needs are 700ch total. 200MSPS ADCs would be ideal. Alphacore's current STTR Ph1 program provides 16-channel 100MSPS ADC chips with 11.0 ENOB, and a time-interleaved mode that provides eight 200MSPS ADCs per chip. Questions: Are these specs acceptable ? Are preamps needed at all? Radiation hardness requirement?

3) SoLID ToF readout requires either 5 GSPS ADCs, or TDCs with <20ps resolution. We are trying to decide whether to write ADC or TDC proposal. The ADC could be >9 ENOB, 5GSPS, 10mW, 4 channels per chip. The TDC could be <5ps resolution, <1mW per channel, >100 channels per chip. We have been working on both ADC and TDC designs and I'd like to discuss this need in more detail. How many channels total ? Are these for PMTs ? Preamps needed ? Radiation hardness requirement?

The following slides discusses Alphacore's development status related to these needs.

Multi-Channel Readout IC for Nuclear Physics Experiments

ALPHACORE

Analog, Mixed Signal & RF Electronics

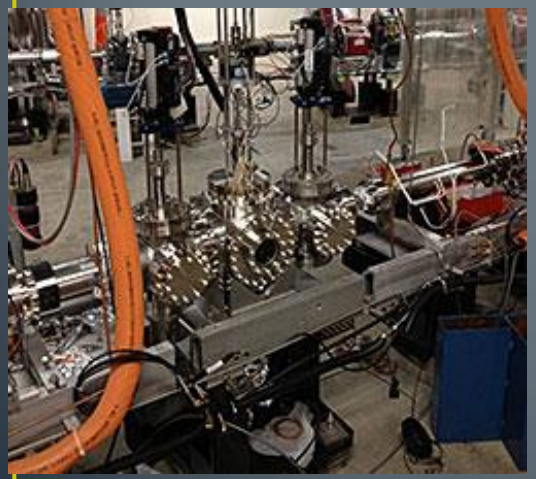
DOE STTR Phase I

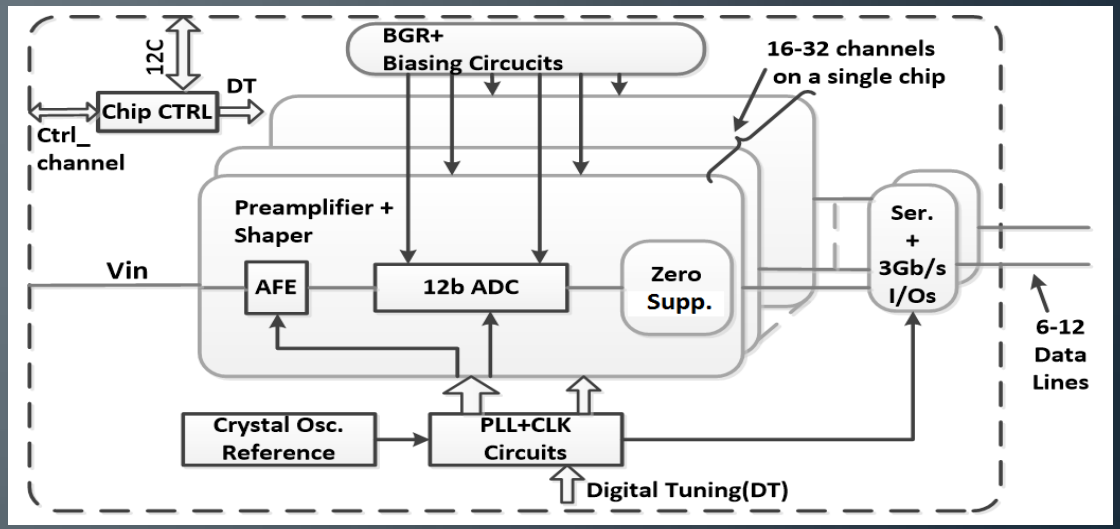
Key Features include:

- 16 channels, each with analog front end with low-noise preamp and shaping amplifier
- 16 parallel 12-bit, 100MSPS, 35mW pipelined ADCs with 11.0 ENOB
- Zero suppression logic block
- 3.25Gb/s per-pin serialized output (20 Gb/s total)
- Low-cost 180nm CMOS fabrication
- Rad-hard to > 500krads

DOE need:

High-performance, low-cost ROIC solution for several planned nuclear physics experiments





Alphacore's 16-Channel ROIC

Planned products

The following products will be developed in this STTR program:

Calorimeter

1) High-Performance Multi-Channel ADC Chip: 16-channels, 12b, 100MSPS, 65mW, LVDS output, rad-hard to 500krad(Si), SEL immune to 120MeV-cm^2/mg. We are also introducing a mode in which two adjacent channels can be time-interleaved to provide eight 200MSPS ADCs per chip. STATUS: Chip layout 90% ready. Tapeout in November.

2) Low-Power Multi-Channel ADC Chip: 32-channels, 10b, 50MSPS, 6mW, LVDS output, rad-hard to 500krad(Si), SEL immune to 120MeV-cm^2/mg. STATUS: Chip layout 30% ready. Tapeout in November.

GEM

3) High-Gain Multi-Channel Charge Sensitive Preamplifier Chip: 32-channels, Programmable 50ns – 1us shaping time, Detector capacitance range: 0 - 50pF, Noise < 1000ENC, power 10mW per channel, rad-hard to 500krad(Si), SEL immune to 120MeV-cm^2/mg. STATUS: Chip layout 60% ready. Tapeout in November.

4) Multi-Channel Current Mode Preamplifier Chip: 32-channels, Programmable 50ns – 1us shaping time, Detector capacitance range: 0 - 300pF Noise < 2,000ENC, power 10mW per channel, rad-hard to 500krad(Si), SEL immune to 120MeV-cm^2/mg. STATUS: Design completed, layout not started.

5) ROIC (shown on Slide 3): 16-channels, Programmable Preamplifiers, ADCs, Zero Suppression, LVDS, rad-hard to 500krad(Si), SEL immune to 120MeV-cm^2/mg. TDC can be added to the readout chain. STATUS: Designs for all components but Zero Suppression completed. Layout not started.

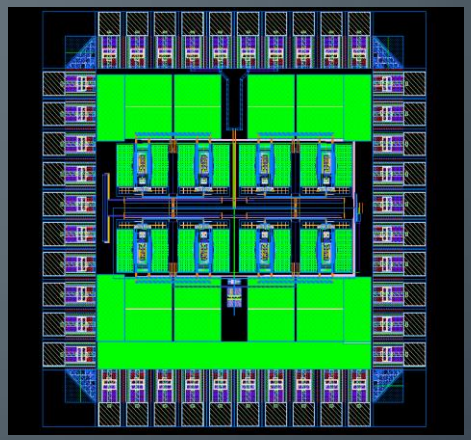
6) Full readout boards with above mentioned chips, FPGA, firmware and software will be available upon request

Action Item: We are currently seeking "last minute" input from potential customers on their ADC, preamplifier and ROIC system requirements. Our next wafer tapeout is in November 2017.

28nm CMOS Products: 10-bit/300MSPS ADC, 10-bit/3GSPS ADC, and 12-bit/2TSPS digitizer

Tapeout Status:

- 10-bit, 300MSPS, 1mW SAR ADC. Layout completed. Tapeout date Oct/2017. 28nm CMOS SOI process.
- 10-bit, 3GSPS, 11mW SAR ADC. Layout completed. Tapeout date Oct/2017. 28nm CMOS SOI process. Layout shown below.
- 12-bit, 2TS/s transient digitizer. Ultra-high burst-rate sampling rate can be achieved for digitizing picosecond transient pulses. Can be used in scientific experiments, TOF applications and LIDAR. Layout completed. Tapeout date Oct/2017. 28nm CMOS SOI process.



10b, 3GSPS SAR ADC layout

Conclusion

Mostly good for CD0

More ressources available for actual testing

Still need some work for CD1 or define R&D to completely mitigate potential issues

Most critical

- GEM chips
- MRPC
- Cerenkov
- Data amount : trigger rates / event size