

# SoLID DAQ update

## SoLID collaboration meeting

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June 7<sup>th</sup> 2018

# Outline

- Outstanding issues
- PVDIS / SIDIS data rates
- DAQ preR&D and R&D request
- FADC dead time simulation
- MRPC
- SAMPA test stand

# Outstanding issues

- PVDIS
  - trigger rate ok
  - GEM ok ( 3 samples readout do we need more ? )
  - calorimeter resolution and pion rejection ( pile-up, 3 samples readout sufficient )
  - finalize Cerenkov readout
  - data reduction ( improve trigger with Cerenkov pixel readout )
  - data transfer
- SIDIS
  - demonstrate 100 KHz rate capability with 1 sample
  - finalize Cerenkov readout
  - can we take all singles : 200 KHz several samples
  - SPD background ( pile up and photon rejection )
  - MRPC timing resolution with background
- J/Psi
  - ok in triple coincidences
  - trigger rates with 3 samples in double coincidence
  - reconstruction efficiency tracking

# PVDIS electron trigger

- Coincidence ECAL and Gas Cerenkov

	Old	Hall D
Singles ECAL	290 KHz	230 KHz
Singles rates Cerenkov	1.9 MHz	803 KHz
Accidental 30 ns	16.5 KHz	4.1 KHz
DIS electron	10 KHz max	7.7 KHz
<b>Total rate</b>	<b>27 KHz</b>	<b>12.1 KHz</b>

# Event size data rates PVDIS

				Event size		Data rate MBs	After noise cut	strips firing	event size bytes		MB/s
1	1156	21.17	244.73	3038.03	3038.03	60.76	9.97	115.25	1430.76	1430.76	28.62
2	1374	10.35	142.21	1765.39	1765.39	35.31	5.11	70.21	871.61	871.61	17.43
3	1374	8.81	121.05	1502.71	1502.71	30.05	4.42	60.73	753.92	753.92	15.08
4	2287	3.07	70.21	871.60	871.60	17.43	1.64	37.51	465.61	465.61	9.31
5	2350	2.79	65.57	813.93	813.93	16.28	1.50	35.25	437.60	437.60	8.75
					Total	159.83				Total	79.19
FADC											
	20000						10				
	Event size FADC	Nb channel	Header			Trailer	Sample				
	Calorimeter	14	4			4	12	280			
	Preshower	9	4			4	12	180	400		
	Cerenkov	9	4			4	12	180			
									11600000		
								740	11600000	11.6	
									Total rate	94	MB/s

About 2.9 GB/s for PVDIS at 20 KHz

# SIDIS event size

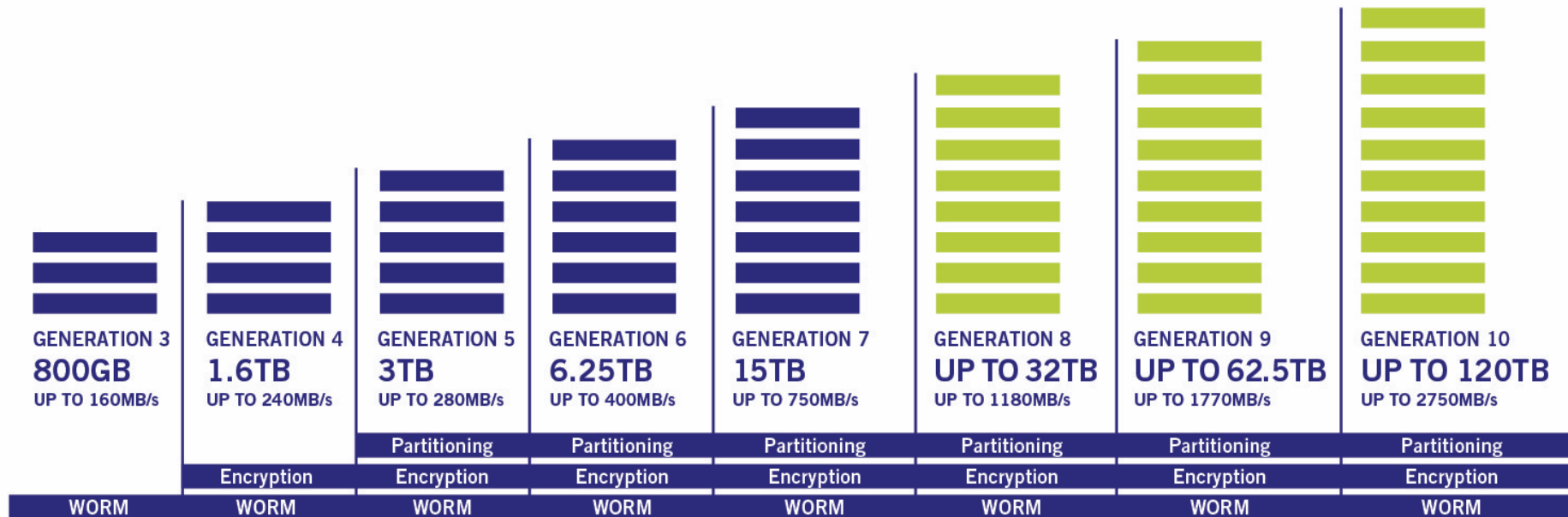
Occupancies with one sample readout by Weizhi , rates for 100 KHz

GEM	Occupancy	Number of strips	XY strips	Strips per chambers	MB/s
1	2.21	453	906	27180	245
2	8.78	510	1020	30600	1184
3	3.63	583	1166	34980	559.5
4	2.31	702	1404	42120	428.7
5	1.78	520	1040	31200	244.71
6	1.3	640	1280	38400	220
Total	20.01	3408	6816	204480	2901

GEM dominating ( 35 bigger than initial proposal ) 2.9 GB/s same requirement as PVDIS

# LTO timeline

## LTO ULTRIUM ROADMAP ADDRESSING YOUR STORAGE NEEDS



Note: Compressed capacities for generations 1-5 assume 2:1 compression. Compressed capacities for generations 6-10 assume 2.5:1 compression (achieved with larger compression history buffer).

Source: The LTO Program. The LTO Ultrium roadmap is subject to change without notice and represents goals and objectives only.

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Currently : 14 drives give 2.24 GB/s ( LTO4 to LTO6) up to 16 drives for now. With LTO8 could be up to 0.36 GB/s per drive max 5.78 GB/s for 16 arms  
Bottom-line : 3 GB/s is reasonable by 2020

# Silo current status

- 12,500 slots in 11 frames, with 16 frame maximum
- 24 tape drives
  - 8 LTO-5 drives, 140 MB/s 1.5 TB raw per LTO-5 cartridge, reads and writes LTO-4
  - 8 LTO-6 drives, 160 MB/s 2.5 TB raw per LTO-6 cartridge, reads and writes LTO-5, reads LTO-4
  - 4 LTO-7 drives, 300 MB/s 6 TB raw per LTO-7 cartridge; reads and writes LTO-6, reads LTO-5
  - 4 LTO-8 drives, 360 MB/s 12 TB raw per LTO-8 cartridge; reads and writes LTO-7 (*coming online Spring 2018*)
- potentially :
  - 8.64 GB/s with all 24 to LTO8
  - 11.52 GB/s with 32 LTO8

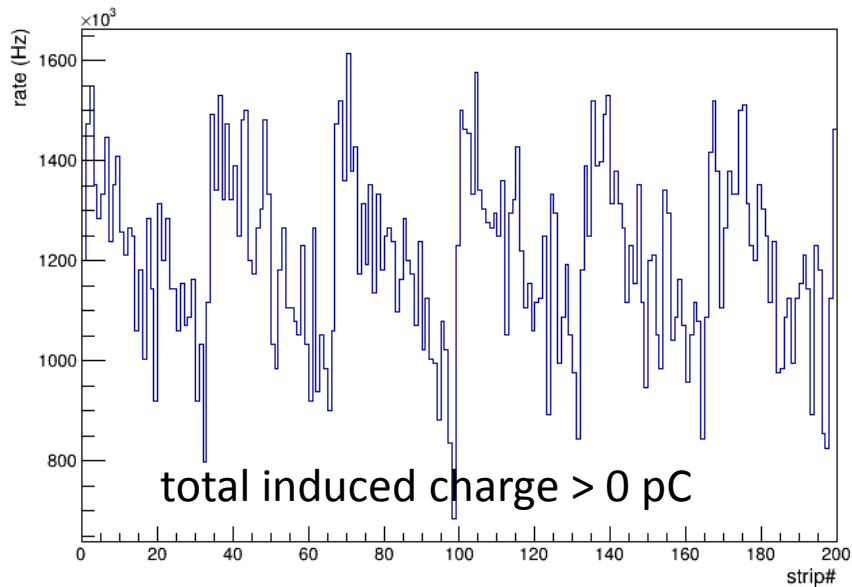
# Time of flight MRPC

- Simulation
  - TDC vs sampling
- Hardware
  - need new chip to handle rate DRS5 or AARDVARC or other
  - Beam test : ensure time resolution reachable in realistic condition

# Time of flight MRPC

## Single rate

- Beam on target
- Average rate/channel:
  - total induced charge > 0.0 pC: 1.2 MHz
  - total induced charge > 0.5 pC: 893.2 kHz



total induced charge cut (pC)	Average rate / channel (MHz)
0.0	1.20
0.1	1.11
0.2	1.06
0.3	1.00
0.5	0.95
0.6	0.84
0.7	0.80
0.8	0.76
0.9	0.72
1.0	0.69
1.1	0.65

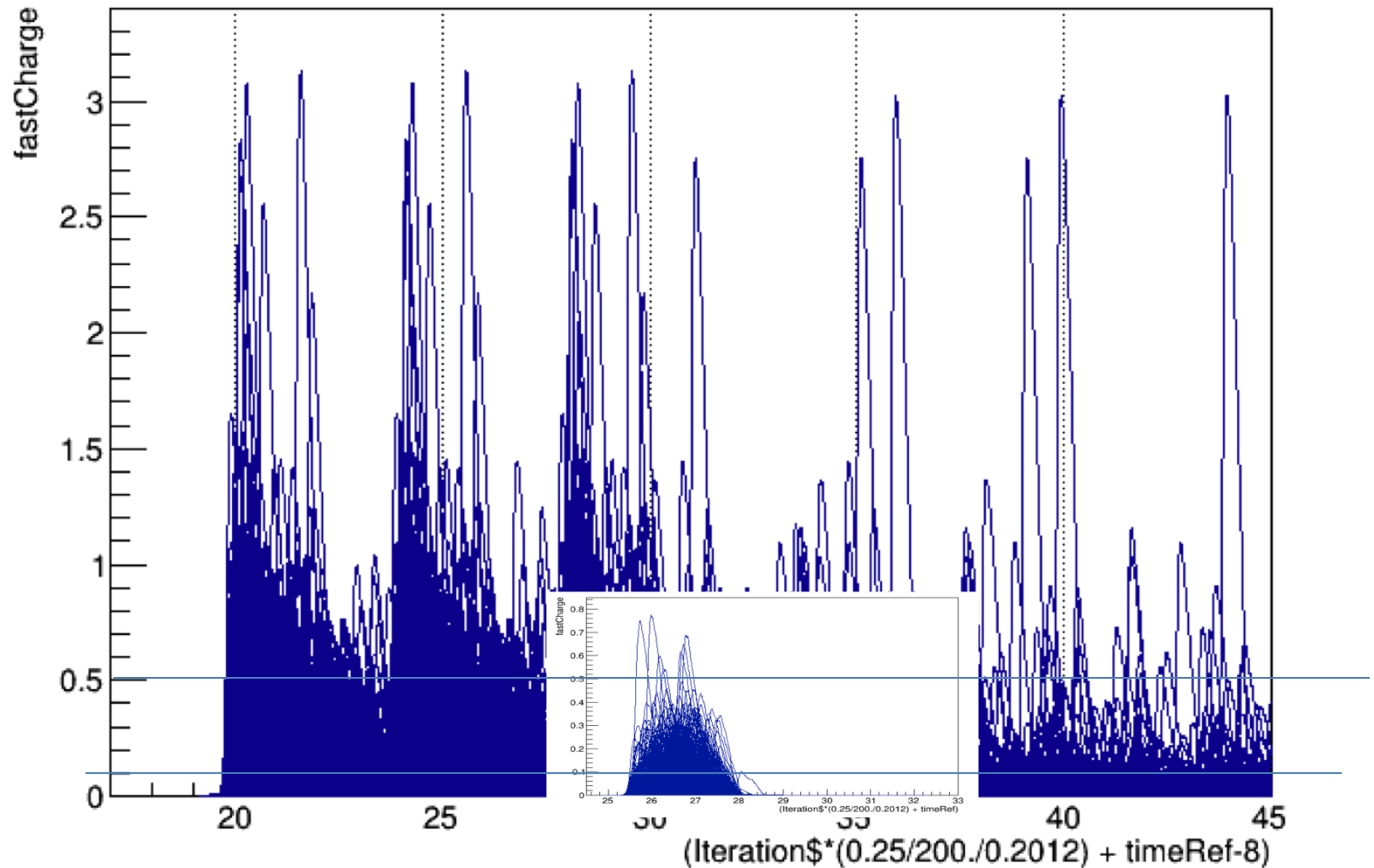
# Time of flight MRPC

## Rate (kHz)/cm<sup>2</sup>

Charge > cut	Rate (kHz)/cm <sup>2</sup>	
	R = 96 cm	R = 105 cm
No cut	656	539
Charge > 0.00	38.7	36.3
Charge > 0.10	37.1	34.8
Charge > 0.20	35.6	33.0
Charge > 0.30	33.8	31.5
Charge > 0.40	32.3	30.1
Charge > 0.50	31.0	28.4
Charge > 0.60	29.6	27.5
Charge > 0.70	28.1	26.4
Charge > 0.80	27.0	25.6
Charge > 0.90	26.1	24.7
Charge > 1.00	25.2	23.6

# Time of flight MRPC

Pulse background beam on target shifted -4ns -8ns



# Cerenkov PMT readout

- MAROC3 close to what we need

- 64 channels
- Variable gain
- Discriminated fast logic signal
- Missing : analog sum of 8, need sum of 64

8 sum of 8 available just need to sum them, will check with INFN for modified RICH board, requested 10 K\$ preRD money

- Radiation hardness is pretty good, need to be tested, possibility of new version to handle Single Event Upset
- MAROC default option
- MAROC test board available

- Will check design with electronics group for FADC analog output

- Possible readout schemes

- FADC only ( default )
- FADC + VETROC
- VETROC only : needs to be evaluated

- Preferred : Add TDC readout for each Cerenkov channel 232 VETROC additional 700 K\$, could improve Cerenkov trigger

- Need simulation to evaluate options
- Need to follow with electronics group to start testing ( anyone from Cerenkov group interested ? )

# TOF options

- Expected timing resolution 80 to 50 ps
- Default readout
  - NINO + TDC : 20 ps timing resolution
- R&D MRPC : 20 ps
  - Sampling TDC ASICs : PSEC4/5, SAMPIC, DRS4 give 5 to 1 ps resolution
  - Need new chip DRS5 or PSEC5 (AARDVARC NALU) to handle SoLID trigger rate ( analog pipeline ) first prototypes for 2018
- Depends on final detector choice
- sPhenix solution: DRS4 system , existing chip but not optimal
- Need to determine effect of photon background, might need sampling to deal with pile up

# GEM readout

- SRS deployed in Hall B Prad
- MPD implemented in CODA
  - BLT testing few KHz
  - Optical fiber readout to be implemented for high rate test ( 100 MB/s to 1.6 GB/s )
- Preliminary results from Weizhi : one sample no deconvolution not sufficient, new occupancy number
- Data reduction on SSP for SBS
- On chip deconvolution ( implemented in MPD ) still an option if needed
- preRD to get VMM3 chip
- SAMPA chip from ALICE

# preRD request

- GEM SAMPA test stand
- Calorimeter trigger and readout
- Coincidence trigger Cerenkov SPD MRPC
- Dead time measurements
- Cerenkov MAROC readout
- MRPC readout and test

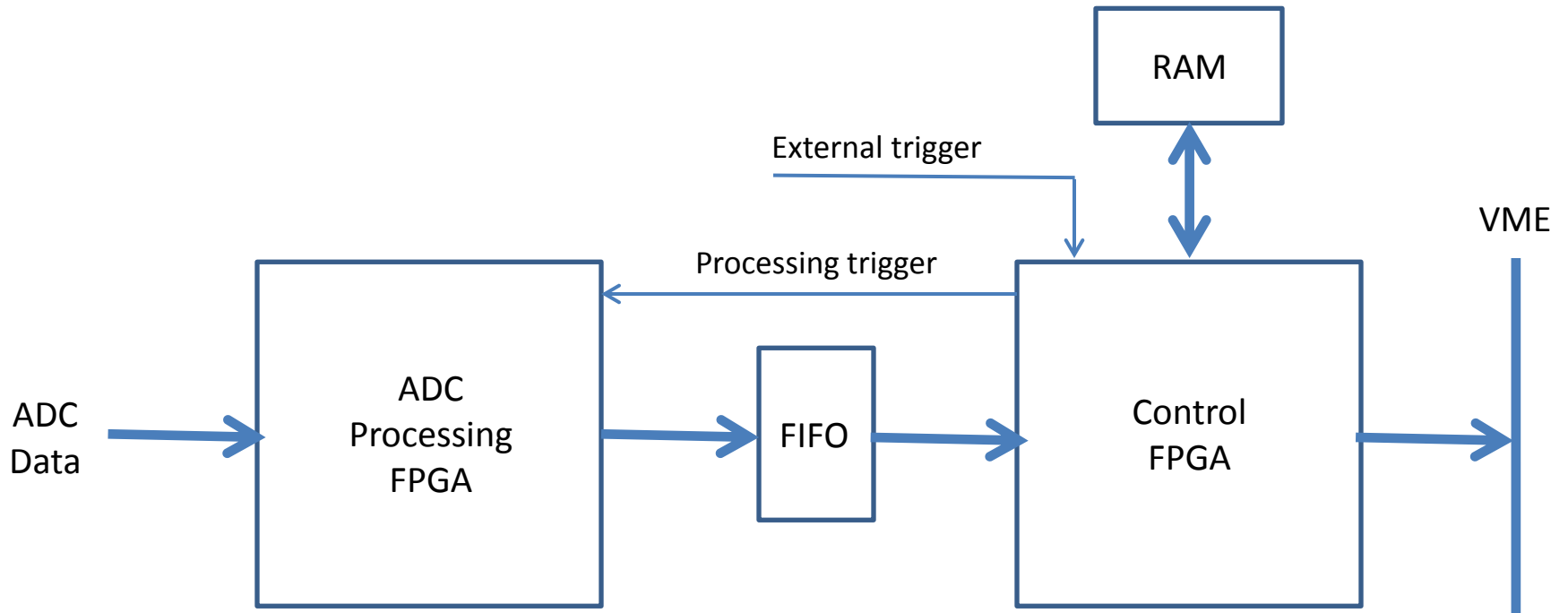
# preRD request

FADC 250	4500	4	18000	Cerenkov	4	18000
VETROC	4500	2	9000			
TD	3000	1	3000			
VTP	7000	1	7000			
SSP	5000	1	5000		1	5000
TID	3000	1	3000		1	3000
SD	2500	1	2500		1	2500
FADC trigger Dist	4000	1	4000		1	4000
VXS crate	15000	1	15000		1	15000
VME CPU	4500	1	4500		1	4500
Optical fiber	100	20	2000			
Computer	3000	1	3000			
APV readout	4500	1	4500			
Network router	10000	1	10000			
Total			72500			
GEM VMM3 eval	10000	1	10000			
MAROC eval	10000	1	10000			
		Total	92500		Total	52000

# preRD and RD request

Tasks	R&D	preR&D
Ecal trigger	3	3
GEM performance	3	3
PVDIS trigger prototype	3	3
SIDIS trigger prototype	3	3
FADC performance	3	
Data transfer test to SILO	1	1
Dead time for PVDIS	3	
Data reduction	6	
L3 farm need evaluation	3	
Cerenkov readout	3	3
Test stand - beam test	6	
Total months	37	16

# FADC Trigger Dead Time (Ed Jasztremski)



# FADC Trigger Dead Time (Ed Jasztremski)

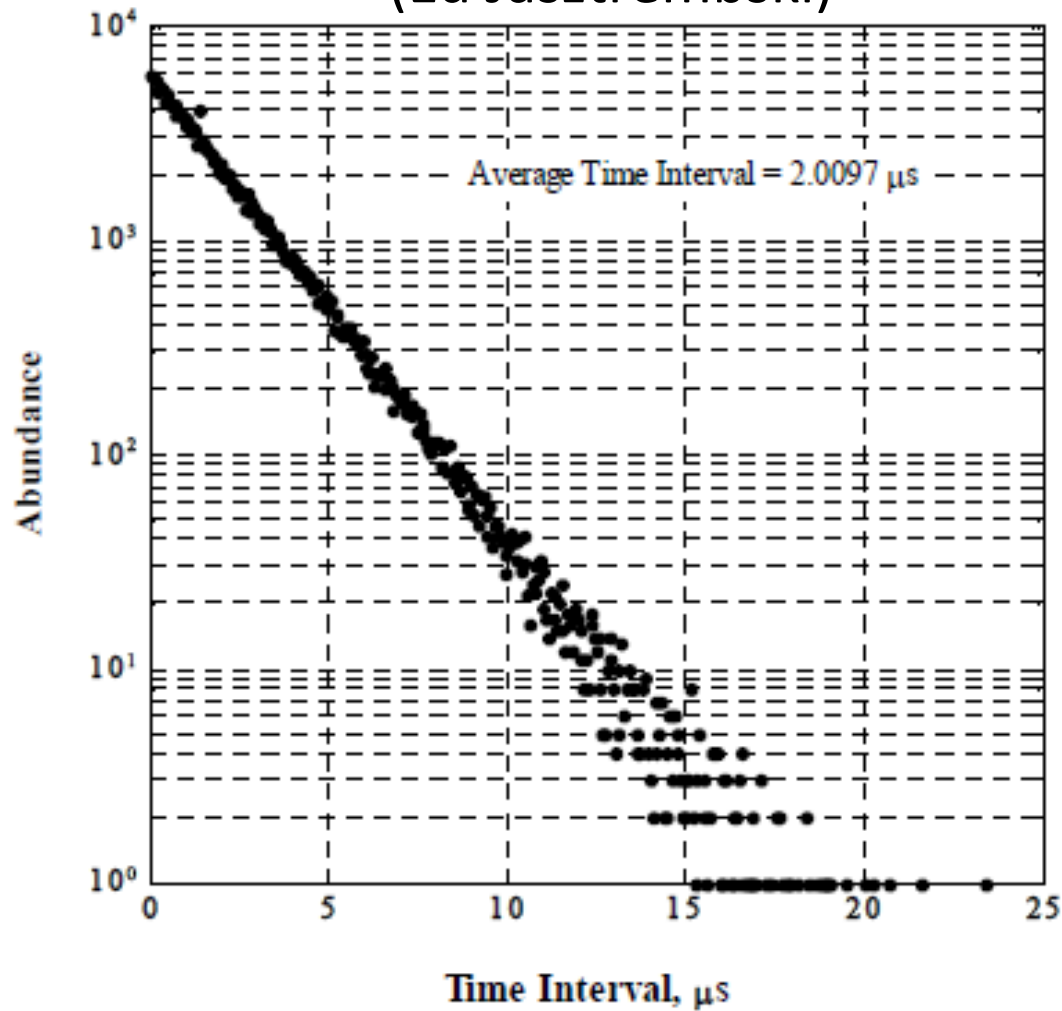


Figure 7. Histogram of the time intervals of the output pulses with Poisson PDF ( $GR_{\text{set}} = 500 \text{ kP/s}$ ,  $N.S. = 2 \times 10^5$ , 400 bins).

# FADC Trigger Dead Time

(Ed Jasztremski)

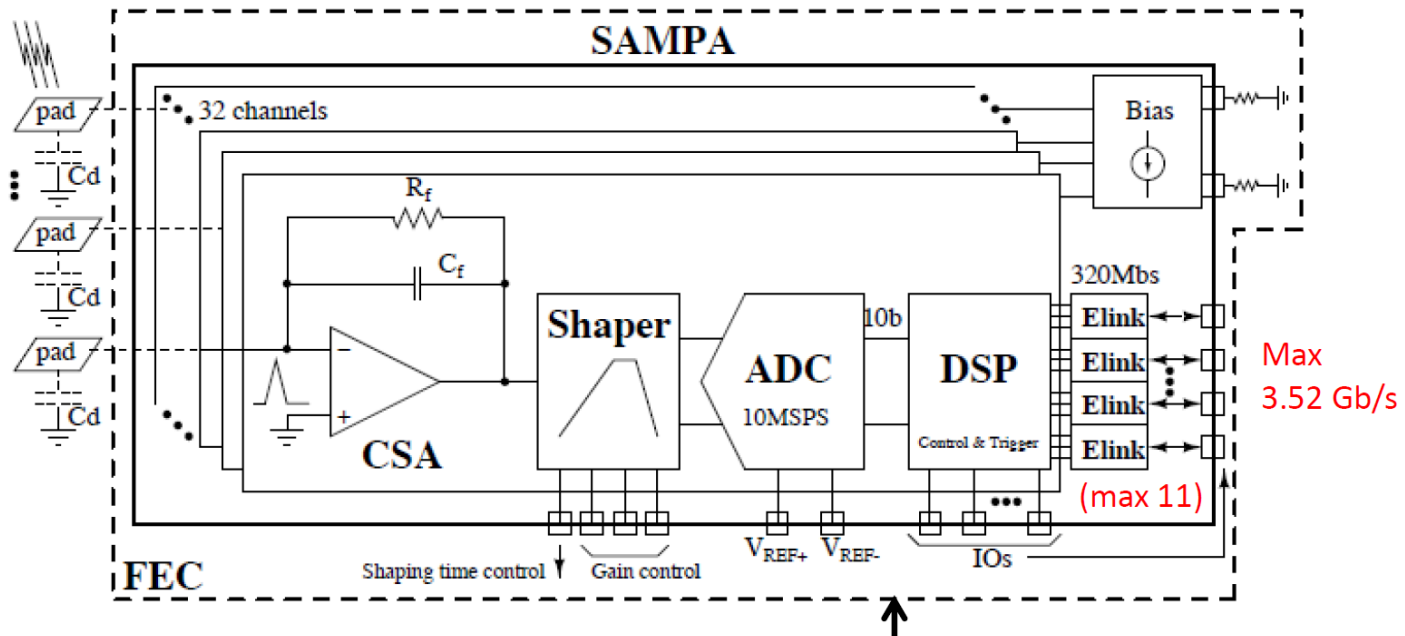
## Test of Simulation Code

100K triggers, Processing time per trigger = 6 us, Maximum stored triggers = 4

Trigger rate (KHz)	Trigger dead time (%)
50	0.2
75	0.6
100	2.0
125	4.6
150	9.2

# SAMPA

## SAMPA ASIC

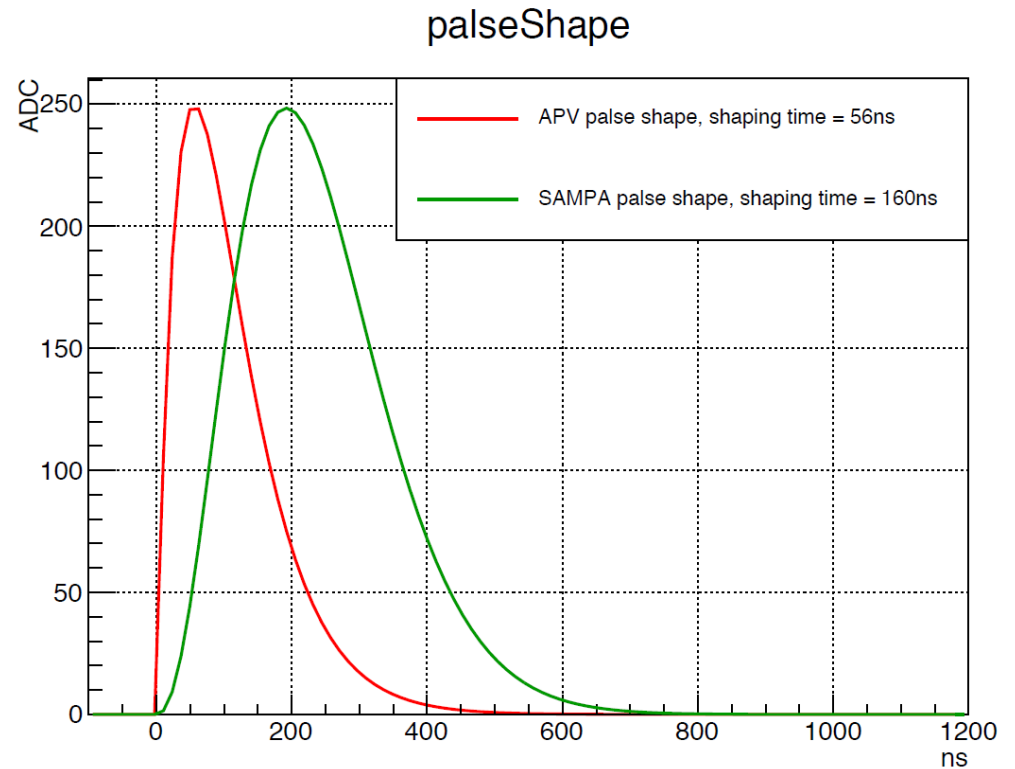


$$\begin{aligned} \text{Raw data rate (10MHz)} &= 32\text{ch} \times 10\text{b} \times 10\text{M/s} = 3.2\text{Gb/s} \\ \text{(20MHz)} &= 6.4\text{Gb/s} \end{aligned}$$

# SAMPA study by Weizhi

## Response function comparison: SAMPA vs APV25

- The SAMPA response curve is much longer than APV25
- The shortest sampling time for SAMPA is 50ns while APV25 uses 25ns
- These two reasons will likely increase the pile-up effects and occupancies
- It is unlikely we will have good results (>90%) for tracking if we only take 1 sample with SAMPA
- It will be better to have at least 3 samples using SAMPA
- For current study, I use 6 time samples



## Occupancy - 1 sample

- Raw occupancy means the # of strips above threshold cut / total # of strips
- Noise rejected occupancy means the # of strips above threshold cut and out-of-time noise rejection cut / total # of strips
- For 1 sample, raw occupancy would be the same as noise rejected occupancy

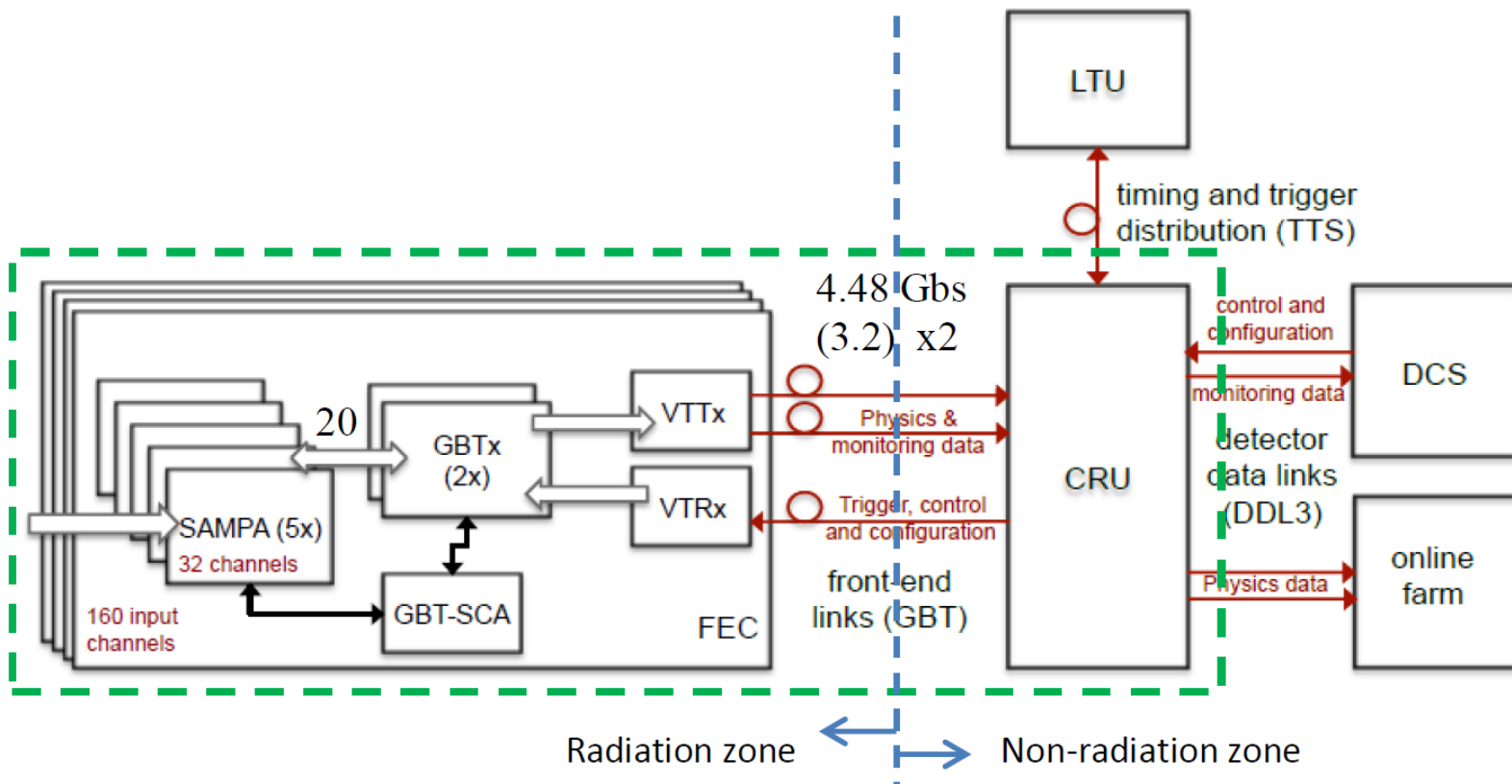
	Raw occupancy	Noise-rejected occupancy
SIDIS plane 1	4.00%	-
SIDIS plane 2	13.7%	-
SIDIS plane 3	5.79%	-
SIDIS plane 4	3.76%	-
SIDIS plane 5	3.36%	-
SIDIS plane 6	2.50%	-

## Occupancy - 6 sample

- Raw occupancy means the # of strips above threshold cut / total # of strips
- Noise rejected occupancy means the # of strips above threshold cut and out-of-time noise rejection cut / total # of strips

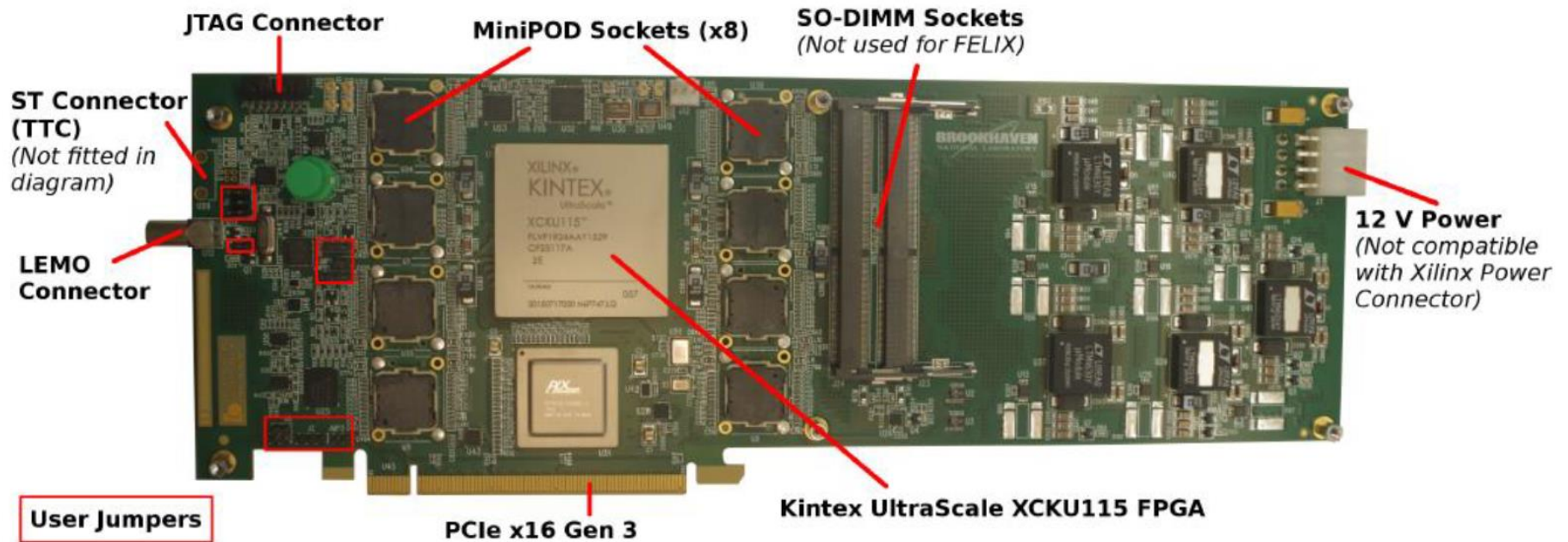
	Raw occupancy	Noise-rejected occupancy
SIDIS plane 1	10.0%	4.33%
SIDIS plane 2	26.3%	11.0%
SIDIS plane 3	14.2%	6.14%
SIDIS plane 4	9.20%	3.93%
SIDIS plane 5	8.67%	3.80%
SIDIS plane 6	6.50%	2.85%

# SAMPA readout (Ed Jasztremski)



# Readout board

BNL-711 V1.5



# SAMPA test stand

- Status as of 6/4/18:
  - (1) SAMPA chips - Acquiring tested chips has been difficult since ALICE is in the process of instrumenting a complete sector of their TPC. Marco Bregant (SAMPA designer) has just obtained 50 chips from the Lund test facility; he is shipping these to us.
  - (2) CERN custom ICs (GBTx, GBT-SCA, VTTx, VTRx) - ordered; should arrive within the next week.
  - (3) Front-End Cards (FEC) - We delayed construction until components (1) and (2) were available. Requisition will be placed in the next week. 4 week fabrication/assembly time has these ready by mid July.
  - (4) Common Readout Unit (CRU) - ATLAS BNL-711 PCIe card delayed until mid July.
  - (5) FEC power supplies - in place
  - (6) High performance PC - in place

# SAMPA budget

## Test Stand Cost

<b>PC</b> – Dell 7920 Dual Processor (Silver, 6x8GB)	<b>\$4,500</b>
<b>Ethernet Adapter</b> - Mellanox MCX4131A-BCAT ConnectX-4 Lx EN Network Interface Card 40GbE Single-Port QSFP28 PCIe3.0 x8	<b>\$400</b>
<b>Optical Transceiver</b> - Mellanox MC2210411-SR4L Optical Transceiver 40Gb/s QSFP MPO 850nm up to 30m	<b>\$155</b>
<b>Power Supply</b> – Keysight E3633A 200W (0 - 8V, 20A)    (\$1519 x 2)	<b>\$3,038</b>
<b>Common Readout Unit</b> – ATLAS BNL-711 (24 links)	<b>\$10,600</b>
<b>Fiber Optic Cable Assembly</b> – FEC → CRU (5m)	<b>\$200</b>
<b>Custom Integrated Circuits (6 FEC)</b>	
SAMPA        \$40 x 30        = \$1200	
GBTx         \$50 x 12        = \$600	
GBT-SCA     \$35 x 6         = \$210	
VTRx         \$200 x 6        = \$1200	
VTTx         \$150 x 6        = \$900	<b>\$4,110</b>
<b>Front End Card</b> – ( <b>\$3114</b> x 5)	<b>\$15,570</b>
<b>Total</b>	<b>\$38,573</b>

# JLab contribution to SoLID

- Ed Jasztremski : dedicated for Hall A
  - FADC dead time
  - SAMPA test stand
- William Gu
  - VETROC for MRPC readout
- Ben Raydo
  - FADC VXS readout
  - Calorimeter Cluster trigger
  - FPGA trigger in VTP for PVDIS and SIDIS trigger
  - MAROC readout

# Conclusion

- preRD hardware and manpower request
- PVDIS mostly ok : dead time / data rates
- SIDIS : GEM rate capability, TOF
- Finalize Cerenkov readout
- preR&D and R&D allows to book time with JLAB DAQ and electronics group
- SAMPA study by Weizhi
- SAMPA test stand ready by mid July