GEM Detectors for SoLID

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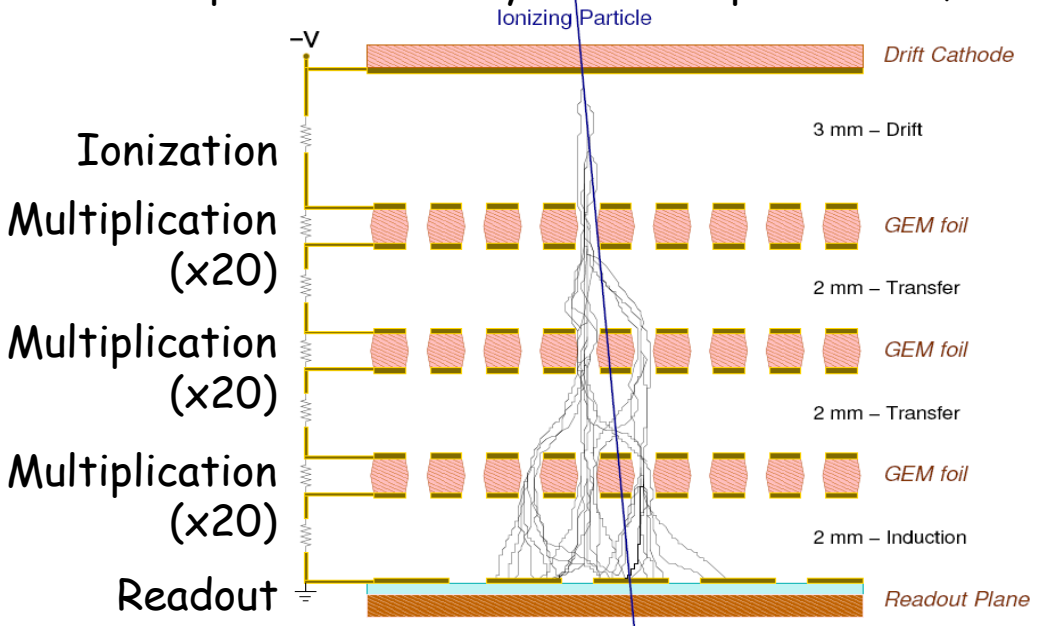
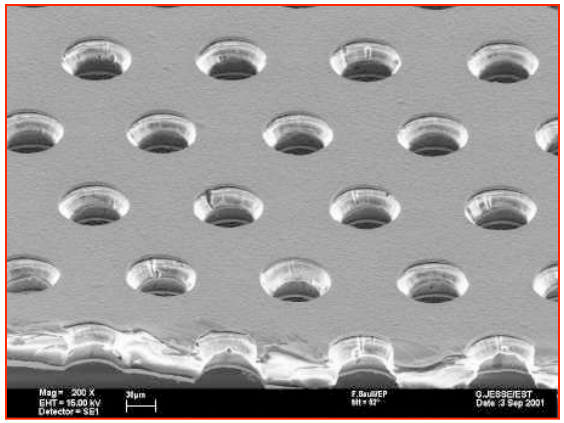
Why GEMs ?

- SoLID concept leads to high rate in trackers: and requires good resolution.
- Gas Electron Multiplier (GEM) detectors provide a cost effective solution for high resolution tracking under high rates over large areas.

- Rate capabilities higher than many MHz/cm^2
- High position resolution (< 75 μm)
- Ability to cover very large areas (10s – 100s of m^2) at modest cost.
- Low thickness (~ 0.5% radiation length)
- Already Used for many experiments around the world: COMPASS, Bonus, KLOE, TOTEM, STAR FGT, ALICE TPC, pRad etc.
- And planed for many future experiments:, CMS upgrade, SoLID, Moller, P2 @ Mainz

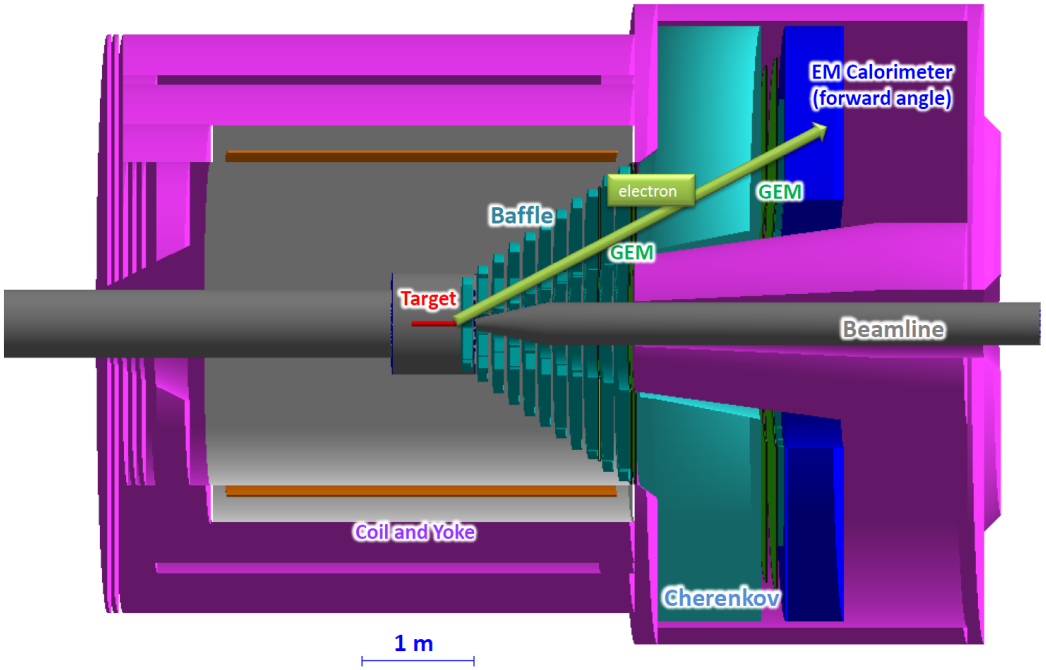


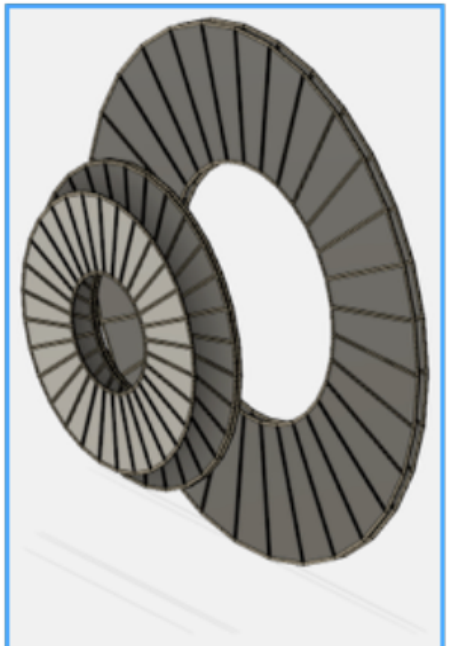
GEM foil: 50 μm Kapton + few μm copper on both sides with 70 μm holes, 140 μm pitch

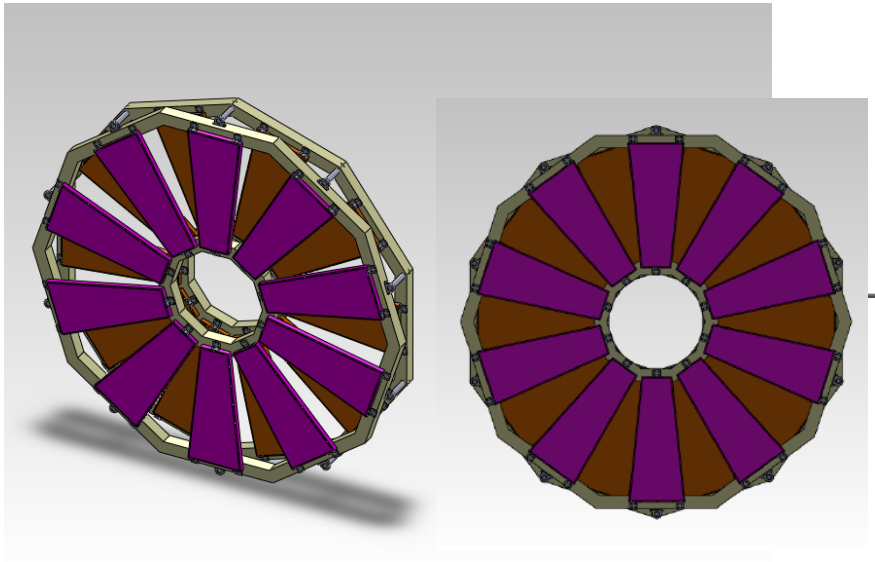


Novel technology: F. Sauli, Nucl. Instrum. Methods A386(1997)531

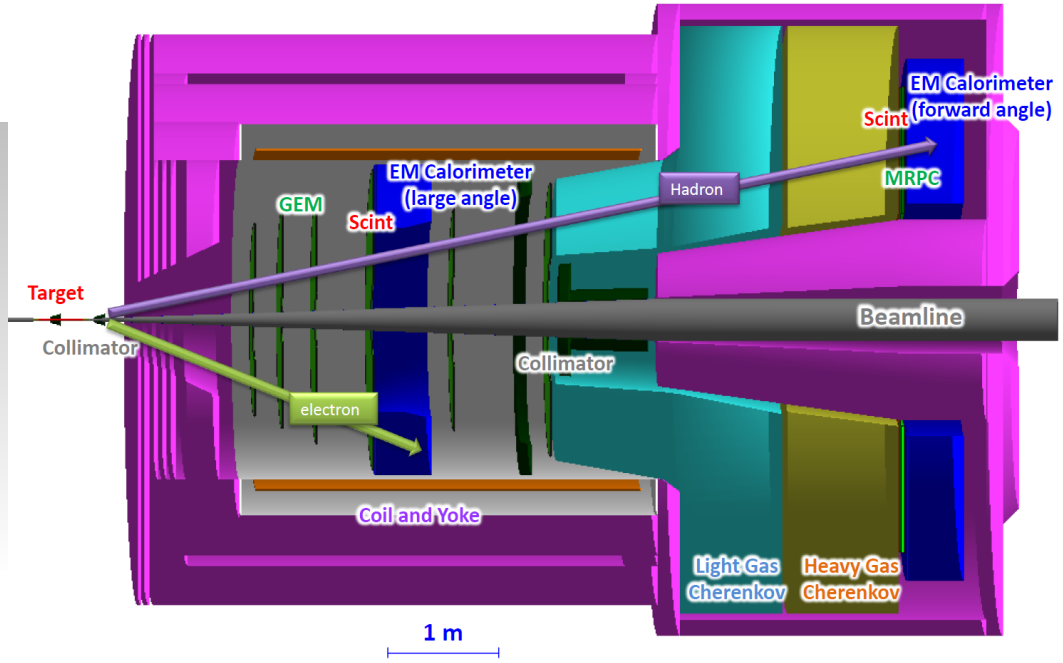
SoLID (PVDIS)







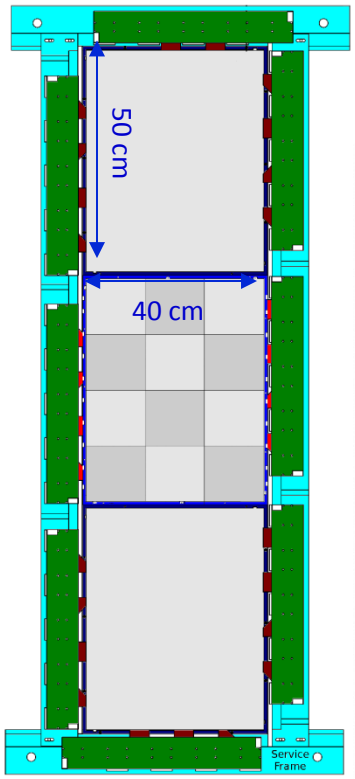
SoLID (SIDIS & J/ψ)

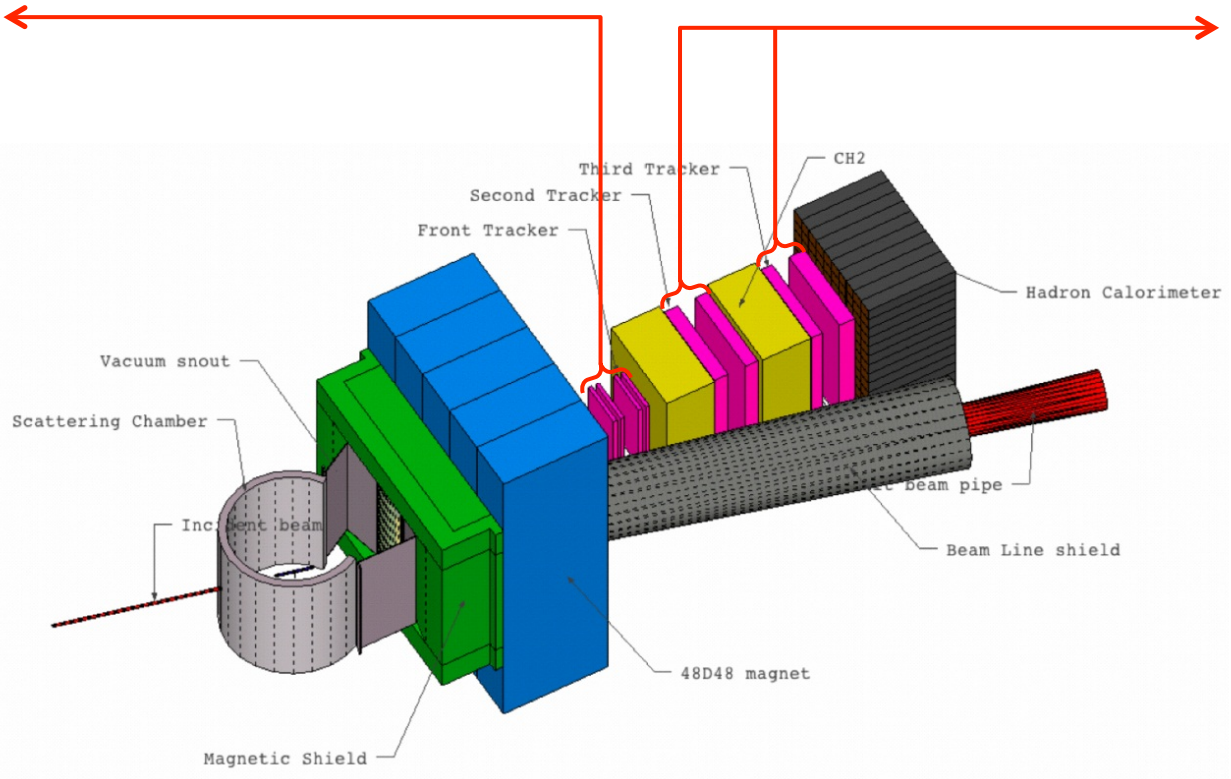


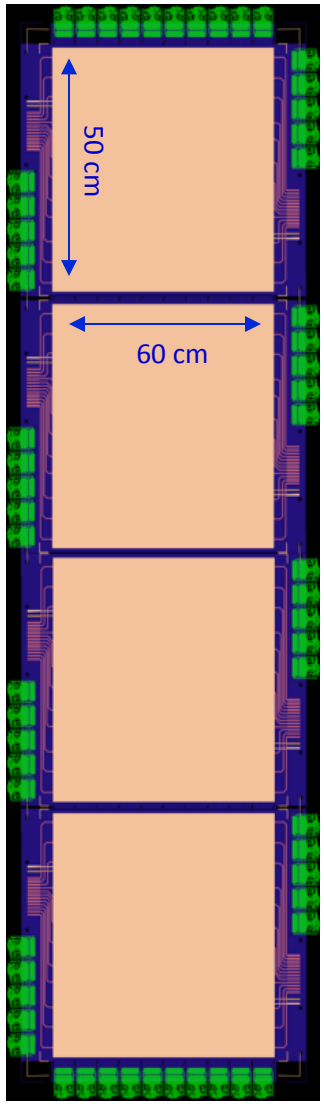
GEM Trackers for SBS

- Front Tracker:
- 6 GEM Layers (150 × 40 cm^2)
- Each layer = 3 GEM modules (50 × 40 cm^2)
- R&D and Production by INFN Roma, Catania

- Back Tracker
- 10 GEM Layers (200 × 60 cm^2)
- Each Layer = 4 GEM modules (50 × 60 cm^2)
- R&D and Production @ University of Virginia







Proton arm layout for GEp (5) experiment

Total Area ~ 16 m^2

SBS GEM Production complete

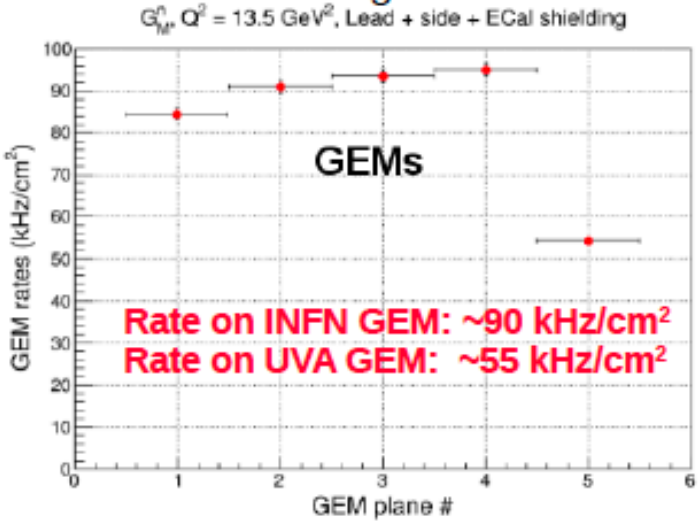
•Completed building 49 modules (plan was to build 48) and tested.
• 46 tested modules and all work per specs.
• Foils from CERN very high quality; over 90% yield; mostly on-time delivery.
• Foil QA at every step extremely important.

Ongoing work for SBS GEMs

• Installation of GEM modules into layers now
• Installation and testing of all electronics.
• Working with DAQ group to implement hardware level data reduction.
    • common mode correction
    • pedestal subtraction
    • zero suppression
    • filter out background not correlated with trigger time.
• Working on GEM background suppression and tracking for GMn experiment conditions (rates ~ 100 kHz/cm2)

GMN GEM background

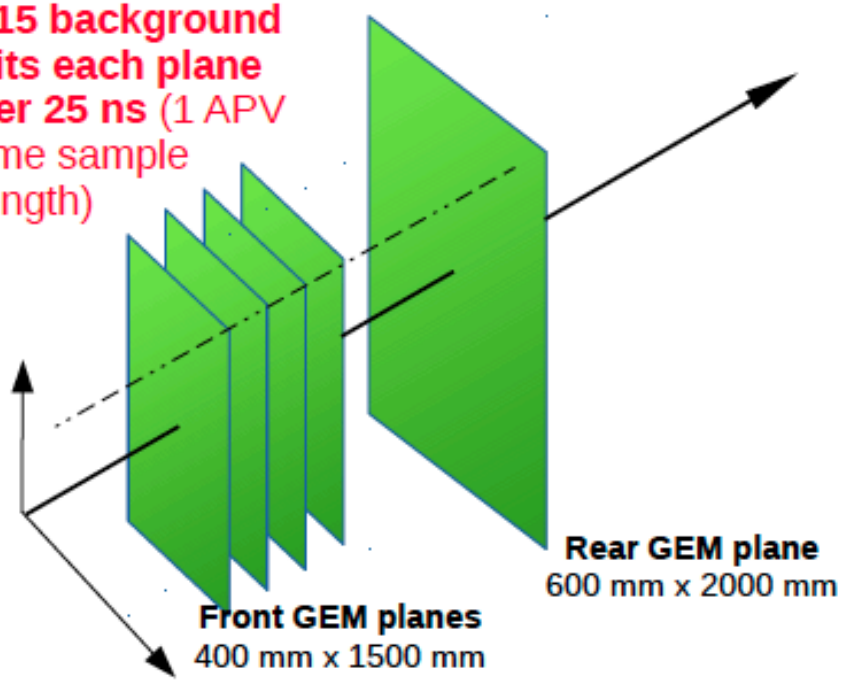
GEM background rate

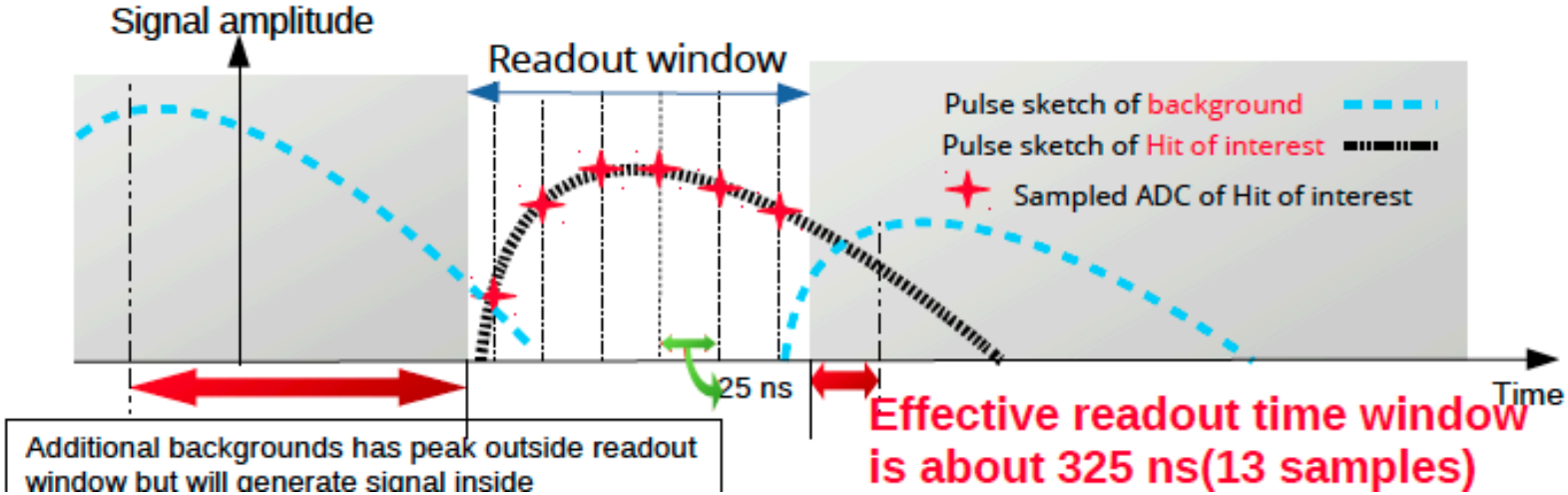


(From Eric, 2017 SBS summer collaboration meeting)

GEM planes in BigBite

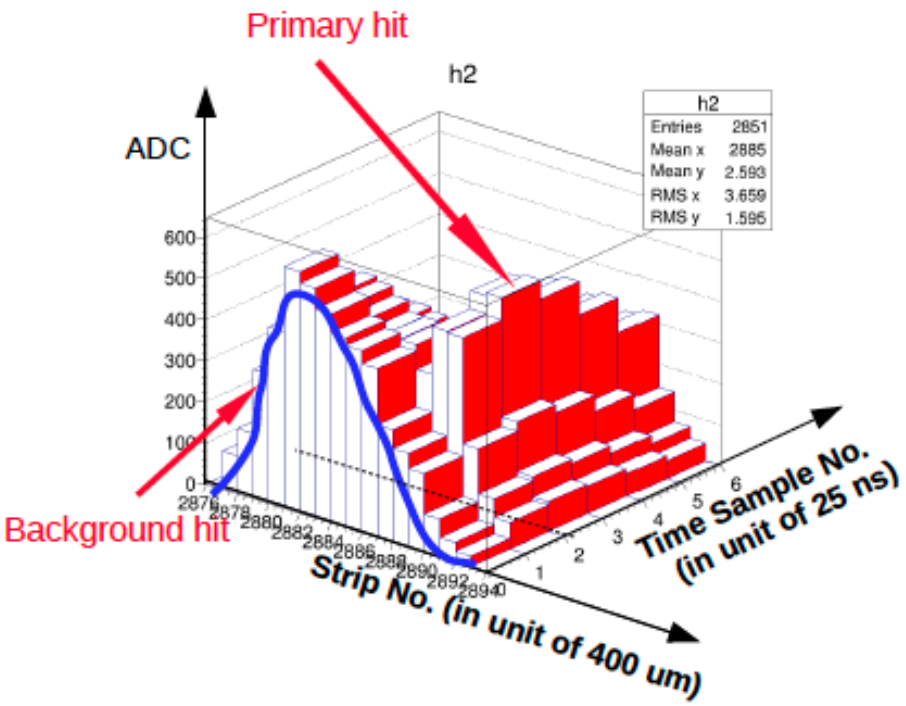
~15 background hits each plane per 25 ns (1 APV time sample length)

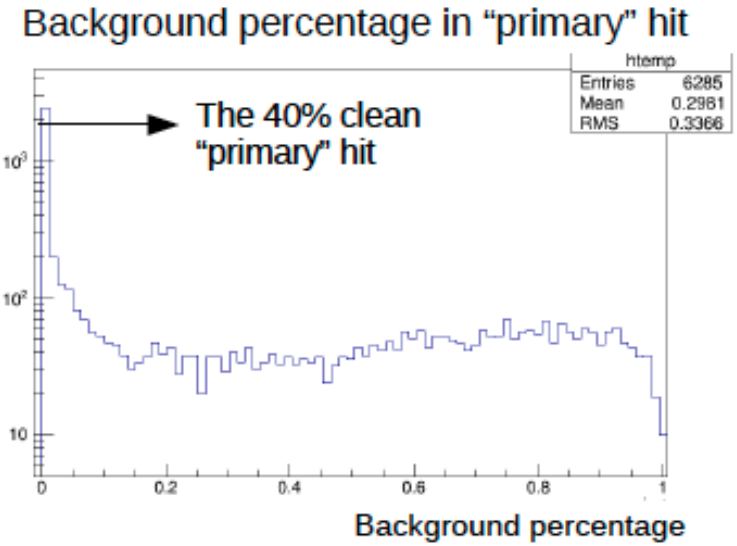




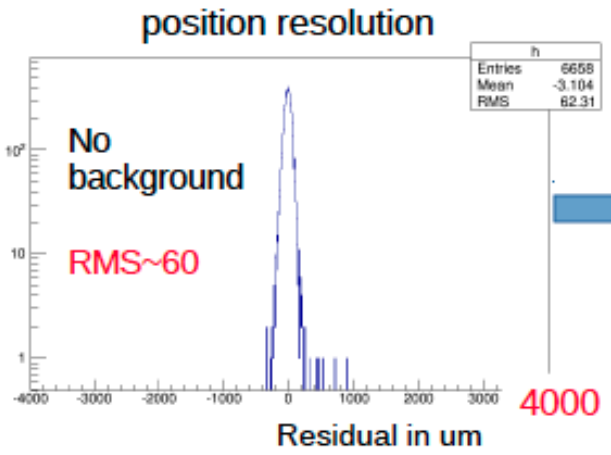
Effective readout time window is about 325 ns(13 samples)

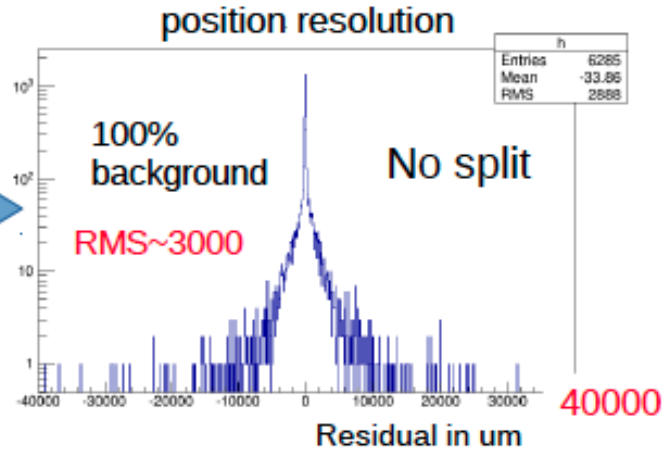
How primary hit overlaps with background





Affect time resolution
Affect position resolution
→ Efficiency drop





Ongoing work carried out by Kondo supported by EIC R&D.

- A new EIC prototype GEM with many new features successfully developed.
  - Moving all readout connections to the outer edge of the circle:
  - successfully demonstrated with small prototype, now implemented in full size module.

  - Composite frames: will reduce cost for SoLID

- Will be tested in beam test at Fermilab in two weeks.
- uRwell prototype
- Planning for a 1 k channel VMM based SRS test stand

Large & Low-mass Forward Tracker GEM for EIC R&D

Common GEM foil design:

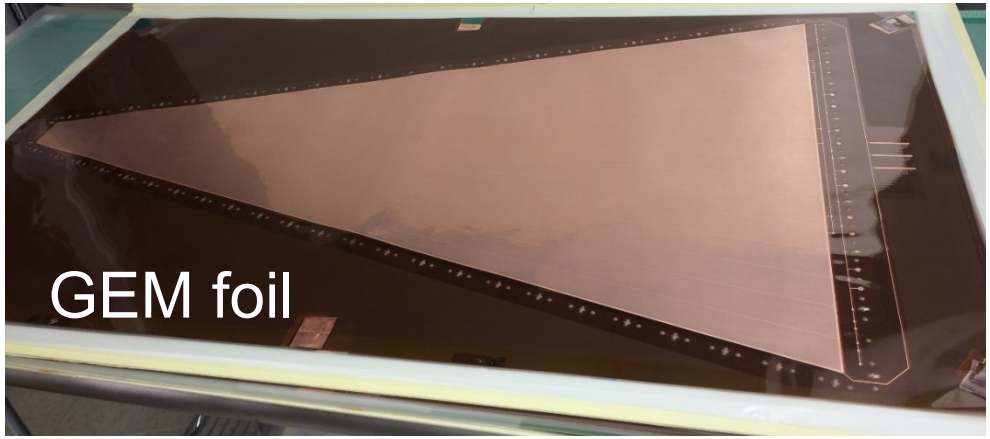
- (Univ. of Virginia, Florida Tech, and Temple U.)
- All connections (HV, gas flow structure and FE cards) are made on outer radius end.

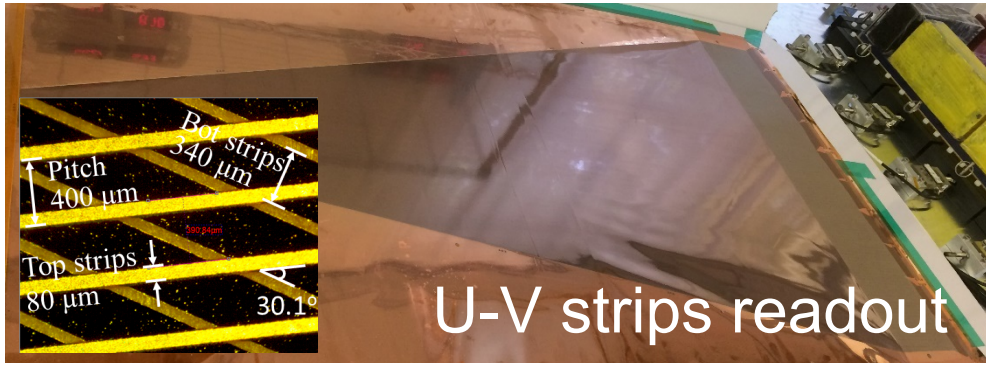
2D U-V strips readout (R/O)

- Spatial resolution improvement
- All readout electronics on outer radius end.
- No connectors or metallized vias on R/O

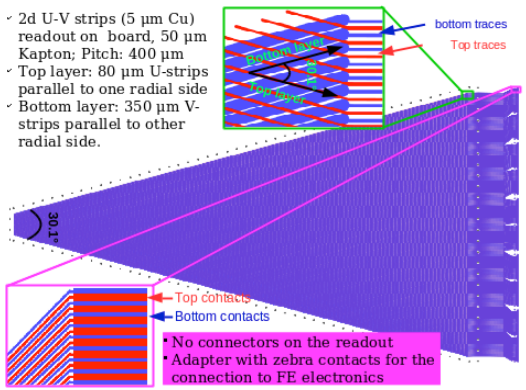
Double-sided zebra connection

- Large density of electronics channels read out on side of the detector (outer radius)
- No electronics on side or inner radius, no multiple scattering or radiation damage issues
- No connectors or metallized vias on R/O

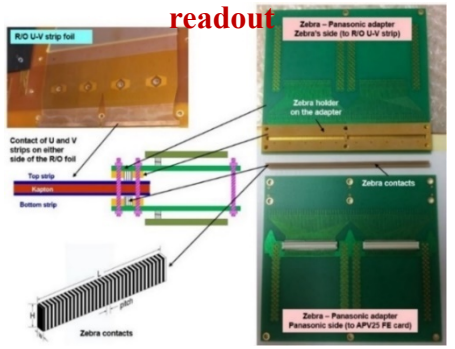




Design of EIC-Proto II 2D U-V strips readout board



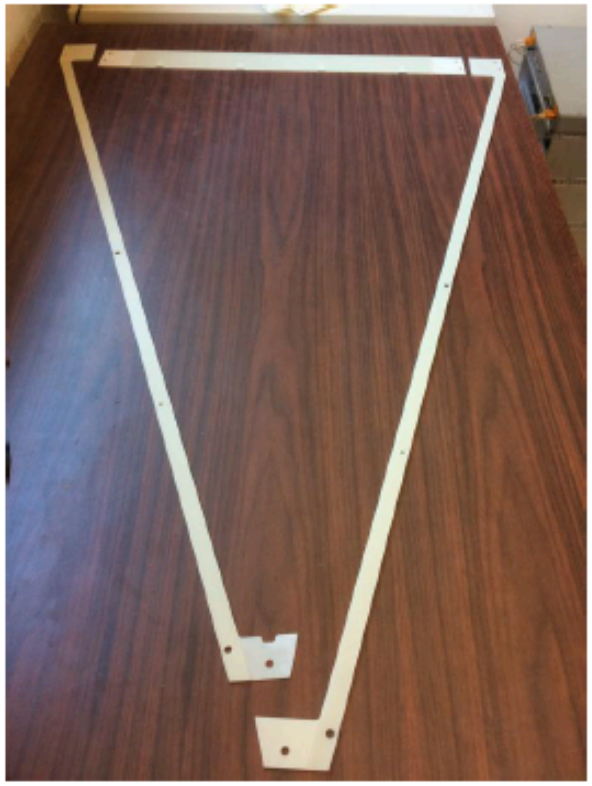
Principle of double-sided zebra connection on flexible PCB readout



EIC Low Cost Frames

Total set of pieces for all 4 frames

Set of 3 pieces for 1 frame



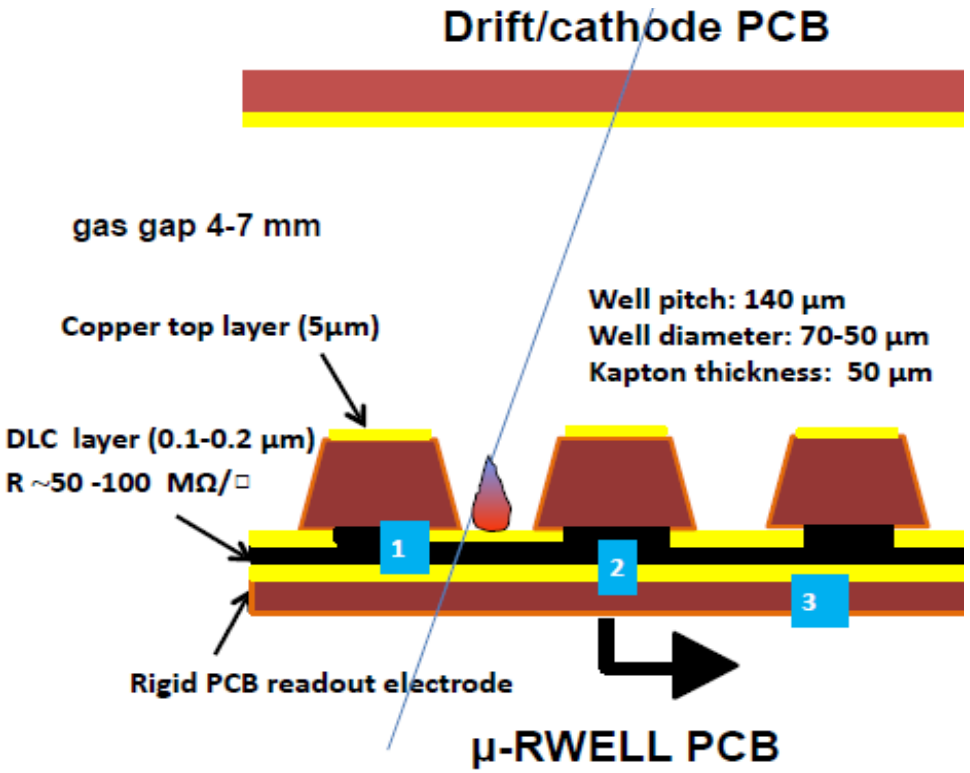
pieces fit together to form a frame

Large & Low-mass Forward Tracker GEM for EIC R&D

Going to the test beam at Fermilab FTBF in two weeks from now

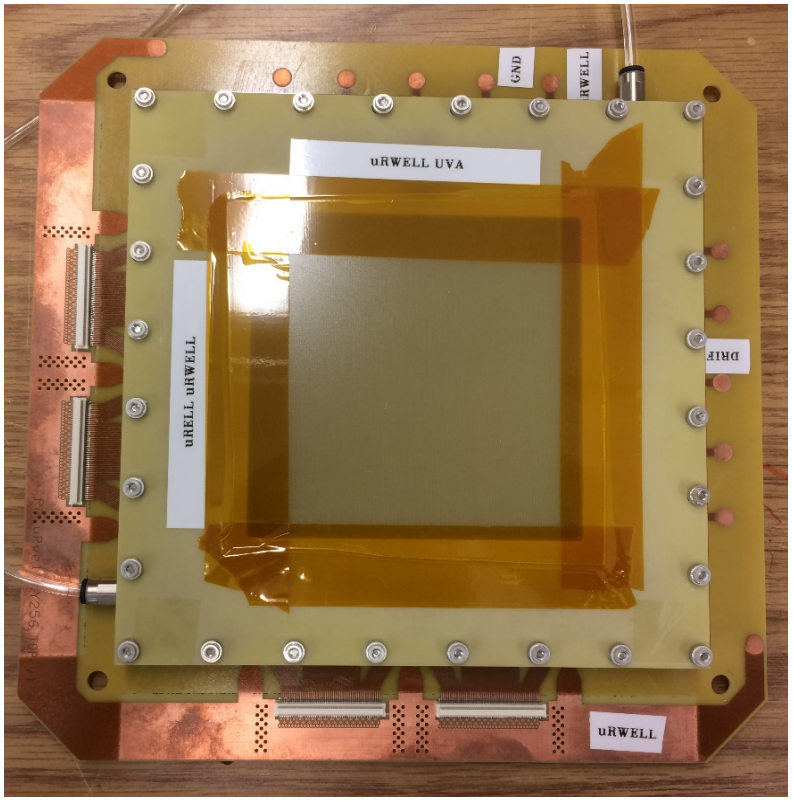
Ongoing work carried out by Kondo supported by EIC R&D.

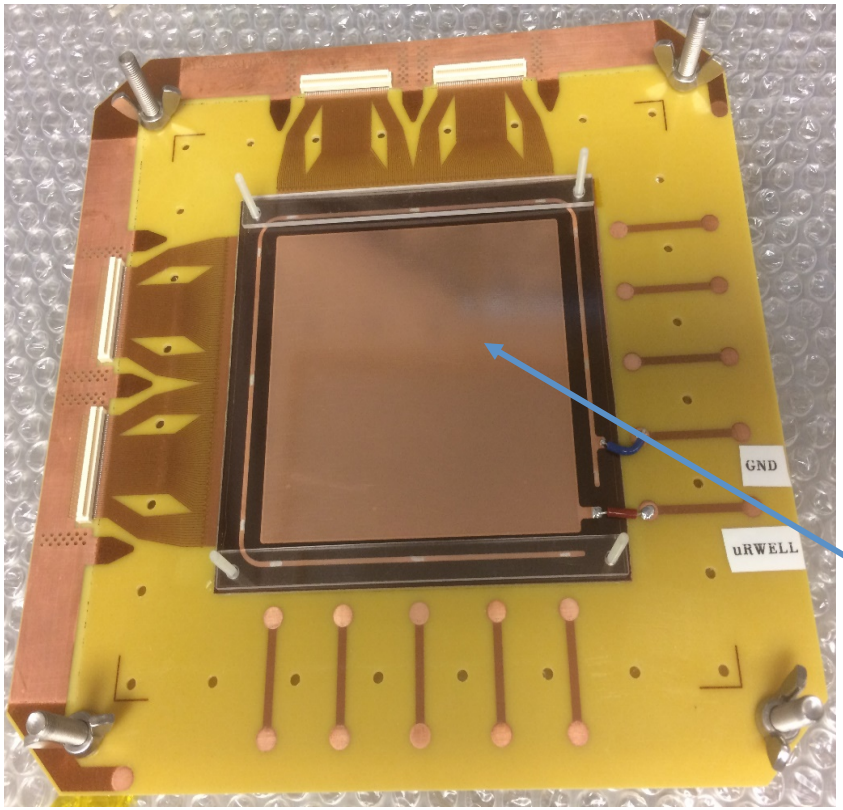
- Development of μ-RWELL detectors:
  - combines GEM and readout together
  - much lower cost
  - can work up to ~ 100 kHz/cm^2.

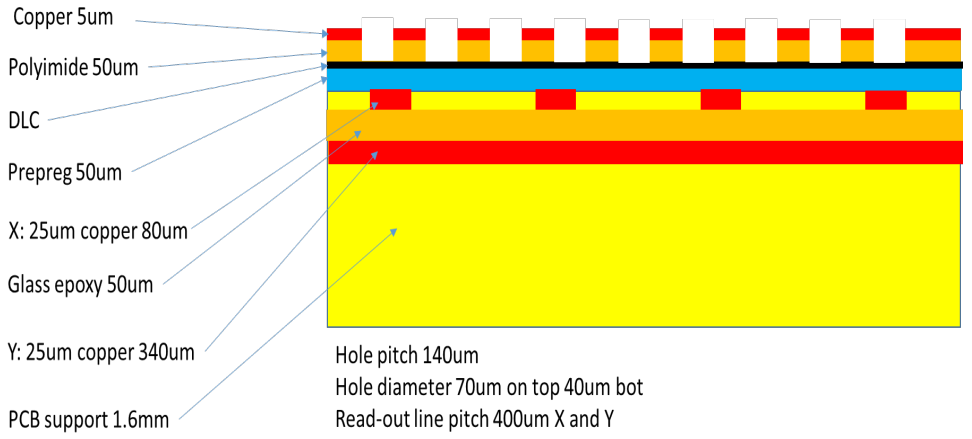


Small (10 cm × 10 cm) prototype of μRWELL detector

- ✓ μRWELL prototype produced by CERN with 2D "COMPASS" readout
- ✓ Going to put it together in clean room this week and test it on cosmic
- ✓ In principle, pretty simple to assemble just add the drift cathode
- ✓ Will also be tested in June FTBF test beam







Important Question: GEM readout Chip selection for SoLID

- Advantages of APV-25:
  - 25 ns time bin with multiple samples: allows pileup correction.
  - We now have a lot of experience with SBS: currently building a 160 k chan. readout for SBS, same size needed for SoLID.
  - Very cheap : ~ $ 3 - $4 per channel
- Disadvantages:
  - Rate is only marginally acceptable for SIDIS even with 1 sample readout.
  - **NO MORE APV CHIPS AVILABLE IN THE WORLD**

- Need to explore new options: Looking at two possibilities
  - SAMPA
  - VMM

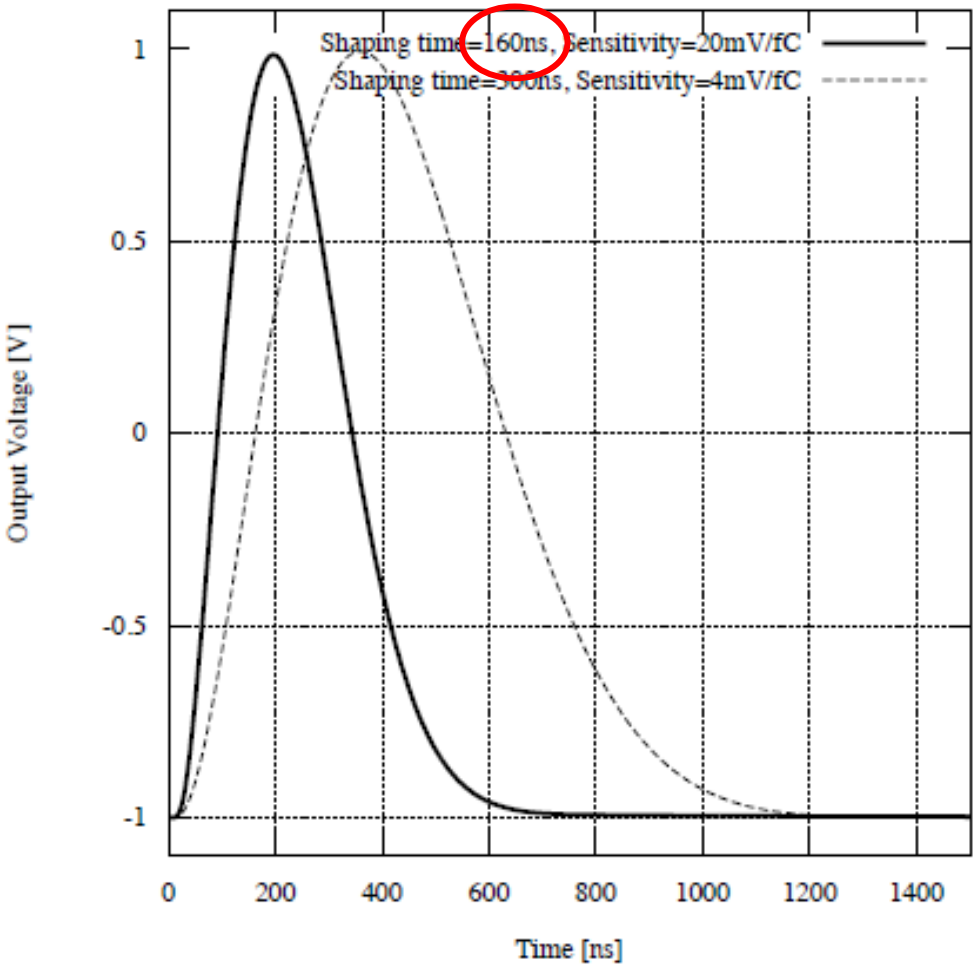
Alternate Chip Options: SAMPA

Weizhi performed a detailed analysis of SAMPA chip for SIDIS: it will work (next few slides)

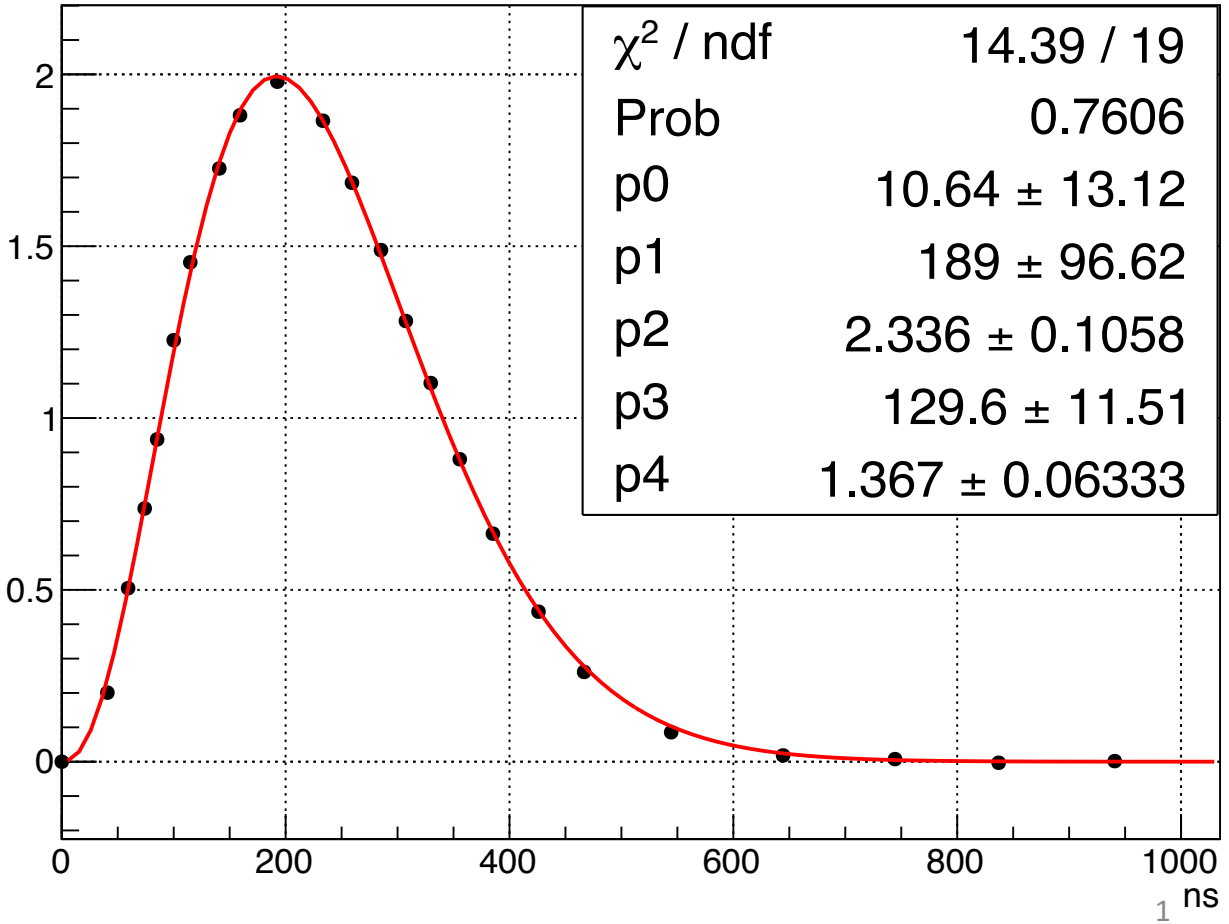
This study needs to be repeated for PVDIS rates; looks like may not work at these high rates

Extracting SAMPA response function

- Using plot digitizer to read off points from the plot and do a fit to get the SAMPA response function
- Shape reasonably well described by functional form: $p_0 \left(\frac{t}{p_1}\right)^{p_2} e^{-\left(\frac{t}{p_3}\right)^{p_4}}$

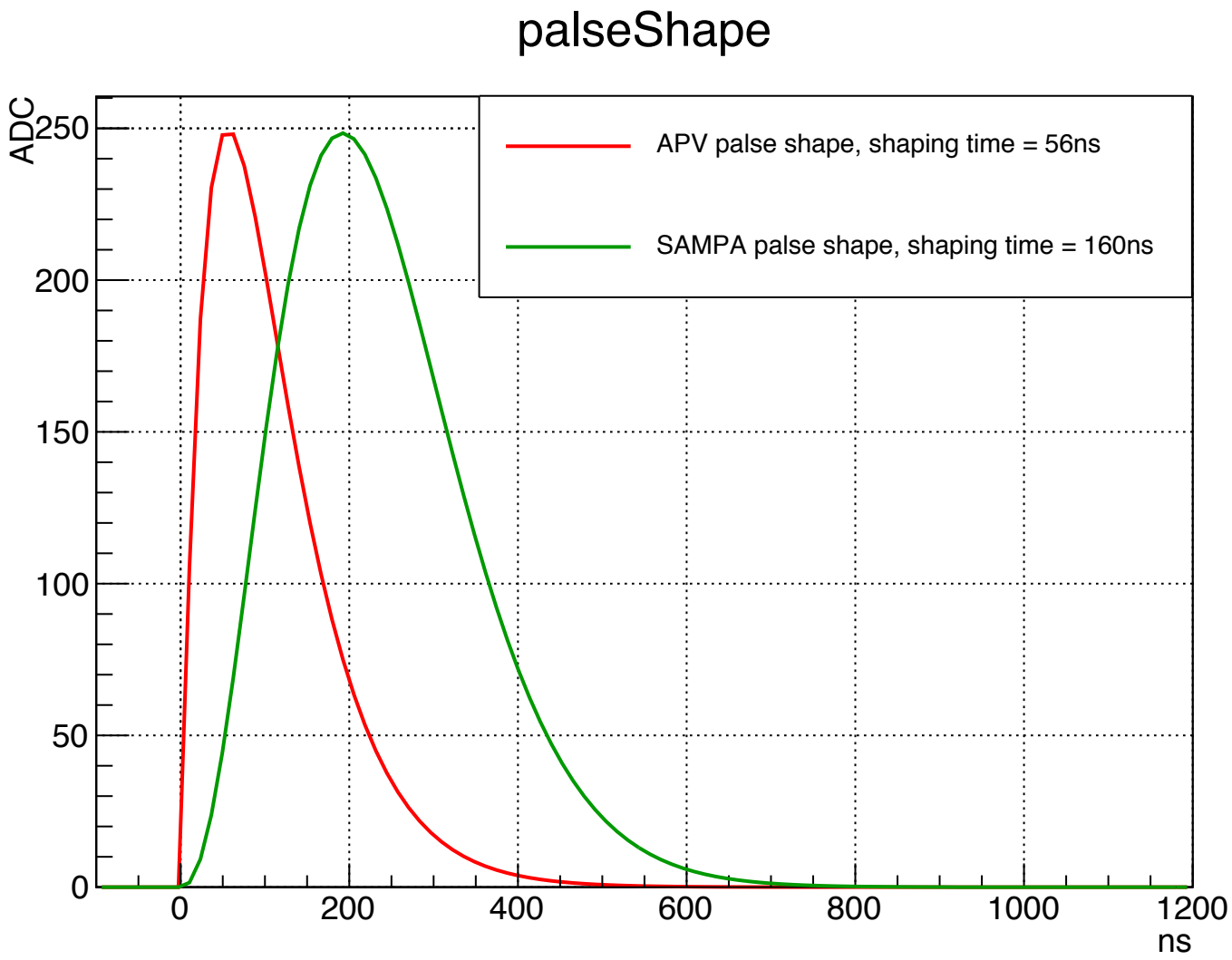


SAMPA palse shape



Response function comparison: SAMPA vs APV25

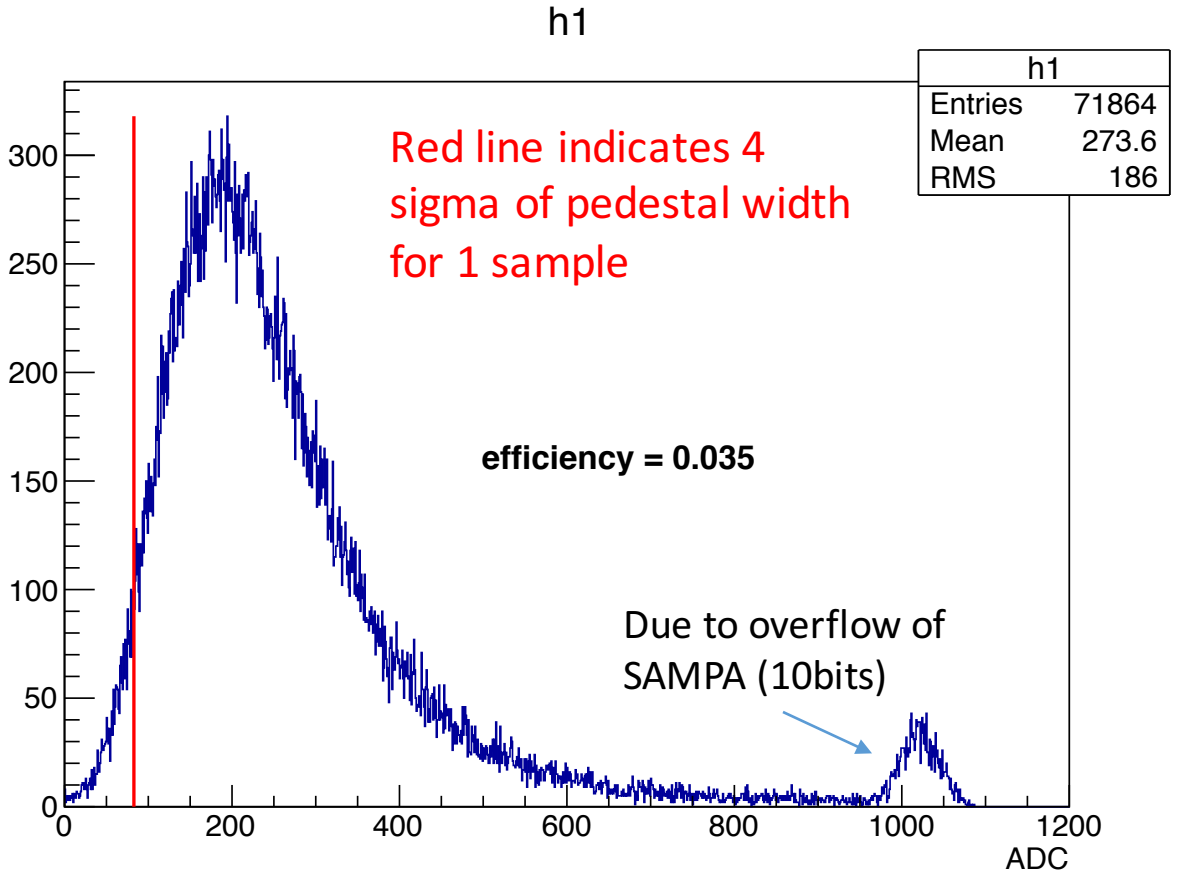
- The SAMPA response curve is much longer than APV25
- The shortest sampling time for SAMPA is 50ns while APV25 uses 25ns
- These two reasons will likely increase the pile-up effects and occupancies
- It is unlikely we will have good results (>90%) for tracking if we only take 1 sample with SAMPA
- It will be better to have at lest 3 samples using SAMPA
- For current study, I use 6 time samples



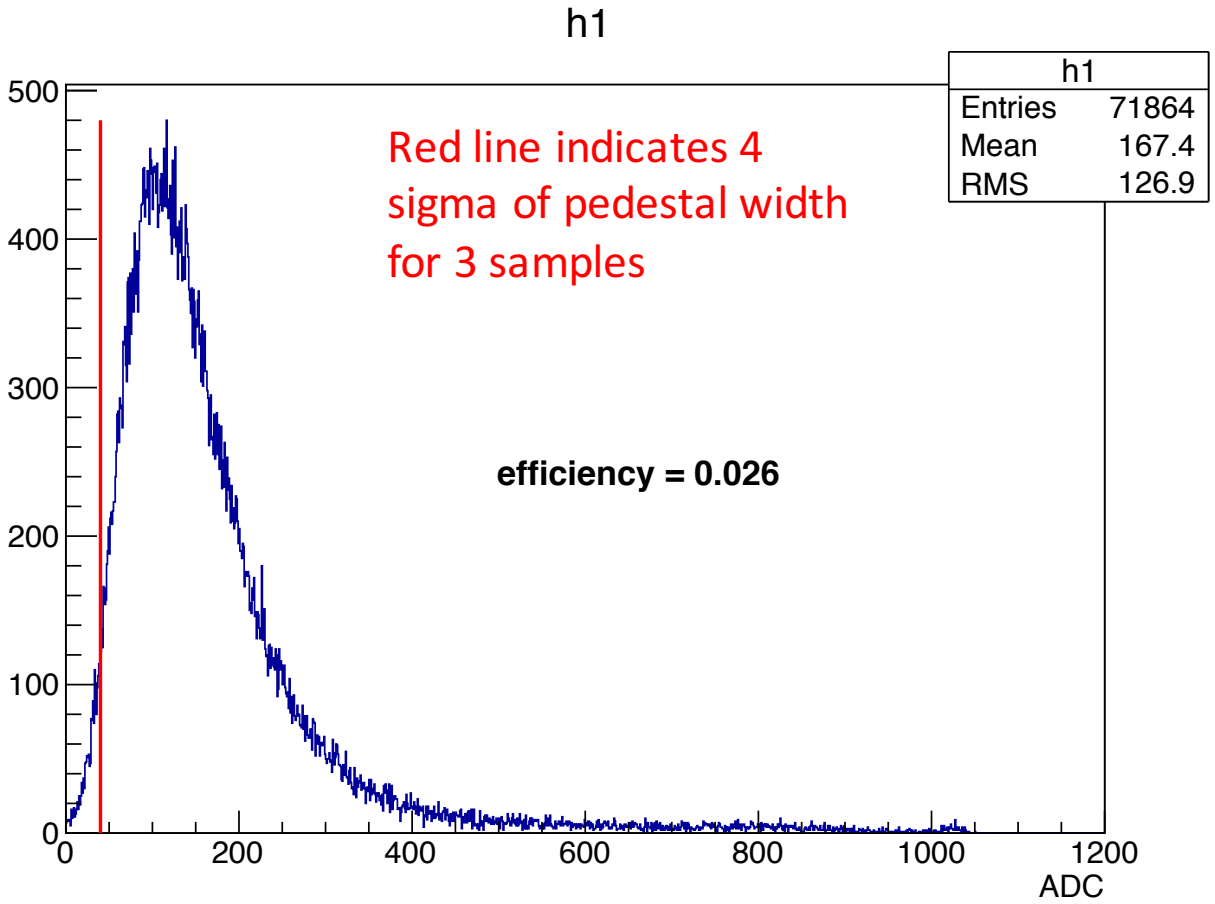
Signal to pedestal noise ratio – SAMPA (50ns sampling period)

Using ADCs on strip at cluster center

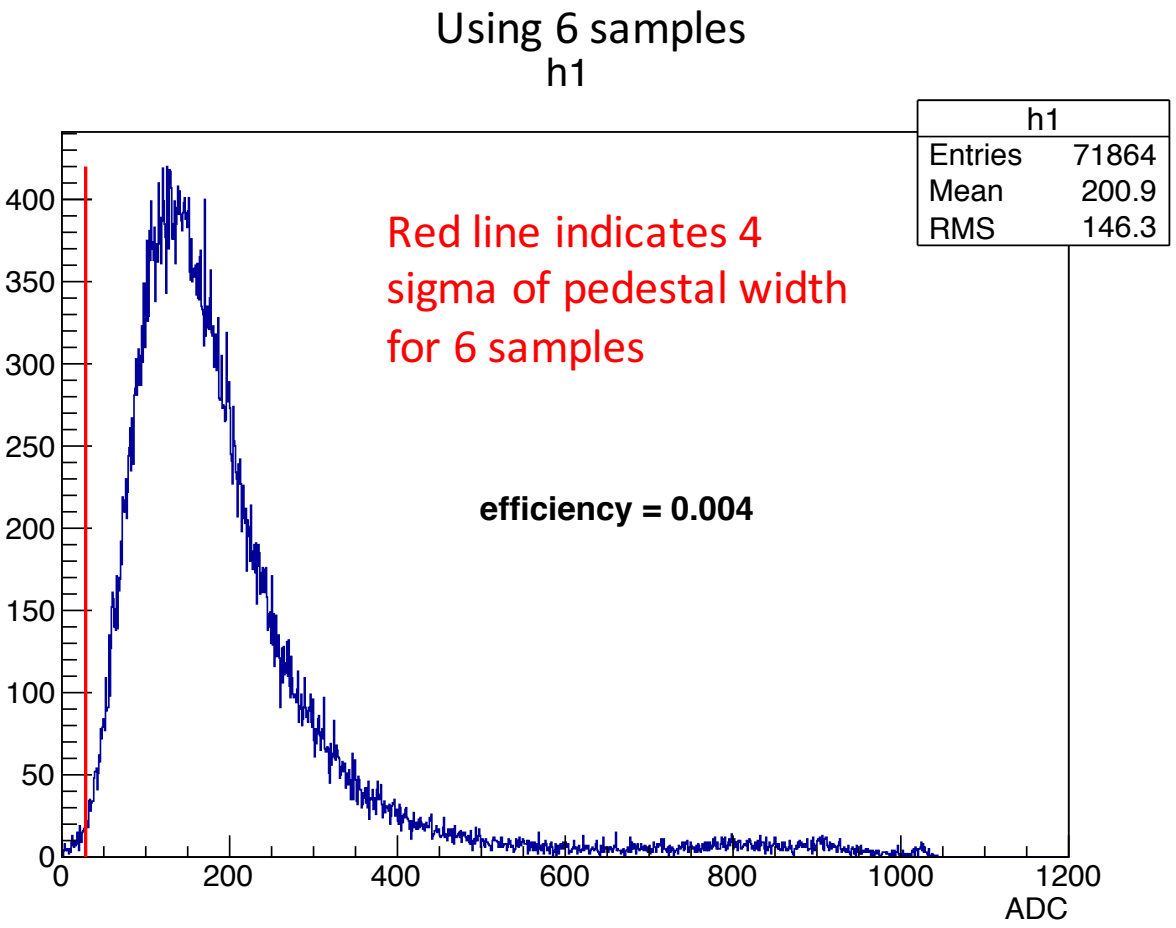
Using 1 sample (maximum one)

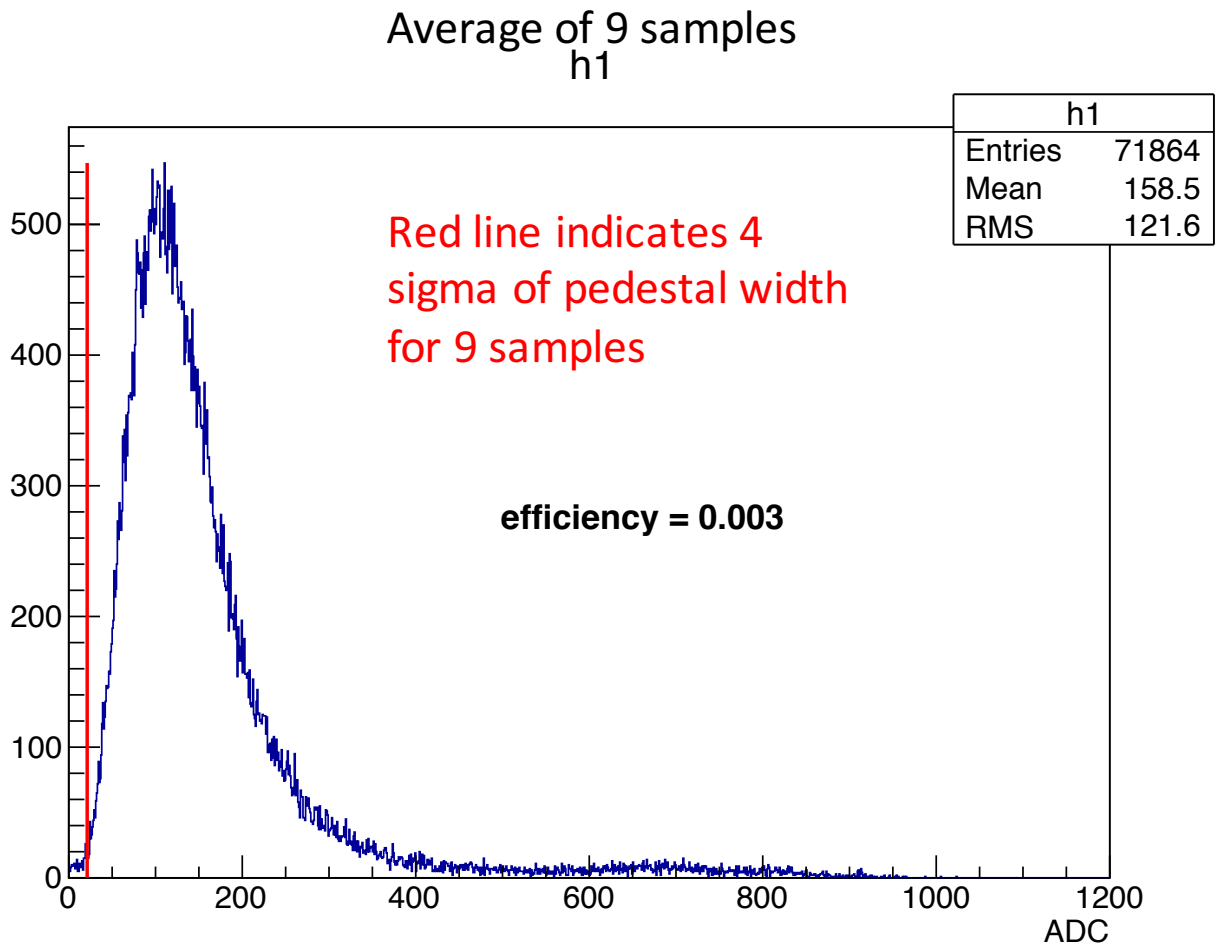


Average of 3 samples



Signal to pedestal noise ratio – SAMPA (50ns sampling period)





Background simulation in digitization and noise rejection

- When using APV25, we used a 275ns time window for the background simulation (200ns before trigger start time and 75ns after), because the pulse length is short and we consider at most taking 3 samples after the trigger start time

- When using APV25 with 3 samples, we compared the relative amplitudes between samples to reject out-of-time events (require leading edge)

- Currently for SAMPA, I use in total 1100ns time window for the background simulation (600ns before trigger start time and 500ns after), because the pulse length gets much longer and we will likely need up to 9 samples

- Still simply use the relative ratio between samples to reject out-of-time events, having in mind that there are more advanced algorithm for this purpose (like fitting to get more precise time info for instance)

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- Still simply use the relative ratio between samples to reject out-of-time events, having in mind that there are more advanced algorithm for this purpose (like fitting to get more precise time info for instance)
  - Require the maximum must be either the 2^{nd}, 3^{rd} or 4^{th} sample and the first sample must have less ADC than the maximum

Occupancy - 1 sample

- Raw occupancy means the # of strips above threshold cut / total # of strips
- Noise rejected occupancy means the # of strips above threshold cut and out-of-time noise rejection cut / total # of strips
- For 1 sample, raw occupancy would be the same as noise rejected occupancy

	Raw occupancy	**Noise-rejected occupancy**
SIDIS plane 1	4.00%	-
SIDIS plane 2	13.7%	-
SIDIS plane 3	5.79%	-
SIDIS plane 4	3.76%	-
SIDIS plane 5	3.36%	-
SIDIS plane 6	2.50%	-

Occupancy - 6 sample

- Raw occupancy means the # of strips above threshold cut / total # of strips
- Noise rejected occupancy means the # of strips above threshold cut and out-of-time noise rejection cut / total # of strips

	Raw occupancy	**Noise-rejected occupancy**
SIDIS plane 1	10.0%	4.33%
SIDIS plane 2	26.3%	11.0%
SIDIS plane 3	14.2%	6.14%
SIDIS plane 4	9.20%	3.93%
SIDIS plane 5	8.67%	3.80%
SIDIS plane 6	6.50%	2.85%

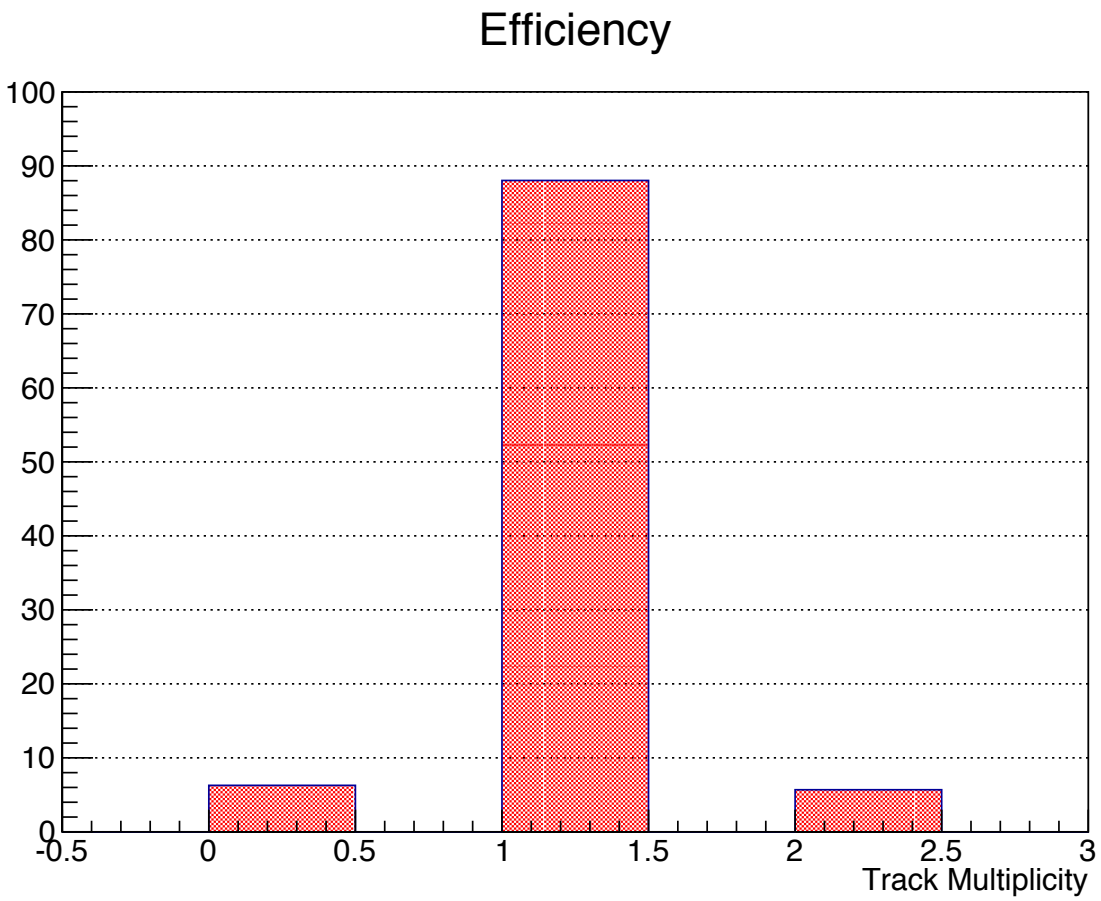
Occupancy - 9 sample

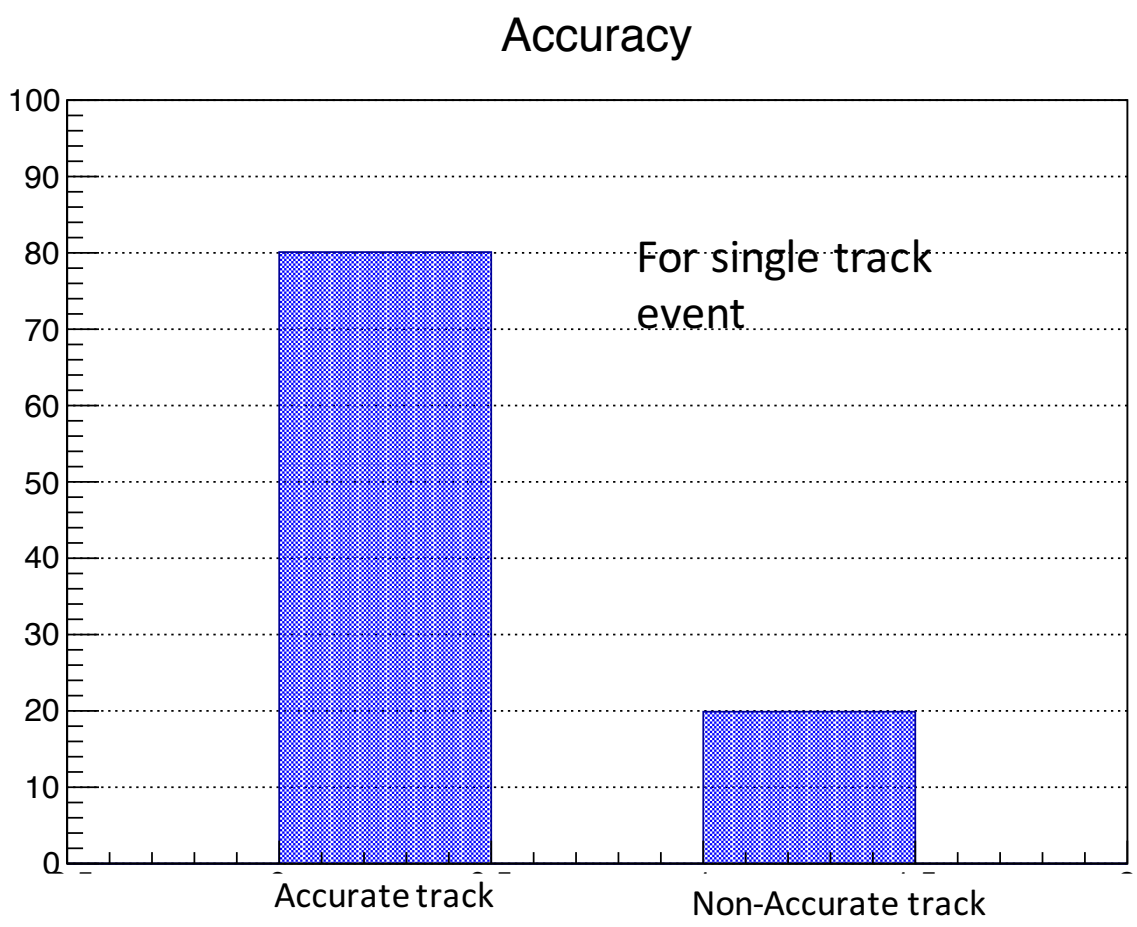
- Raw occupancy means the # of strips above threshold cut / total # of strips
- Noise rejected occupancy means the # of strips above threshold cut and out-of-time noise rejection cut / total # of strips

	Raw occupancy	**Noise-rejected occupancy**
SIDIS plane 1	8.50%	6.10%
SIDIS plane 2	30.3%	13.2%
SIDIS plane 3	17.9%	8.38%
SIDIS plane 4	11.9%	5.56%
SIDIS plane 5	11.3%	5.43%
SIDIS plane 6	8.53%	4.10%

Tracking results – SIDIS FA

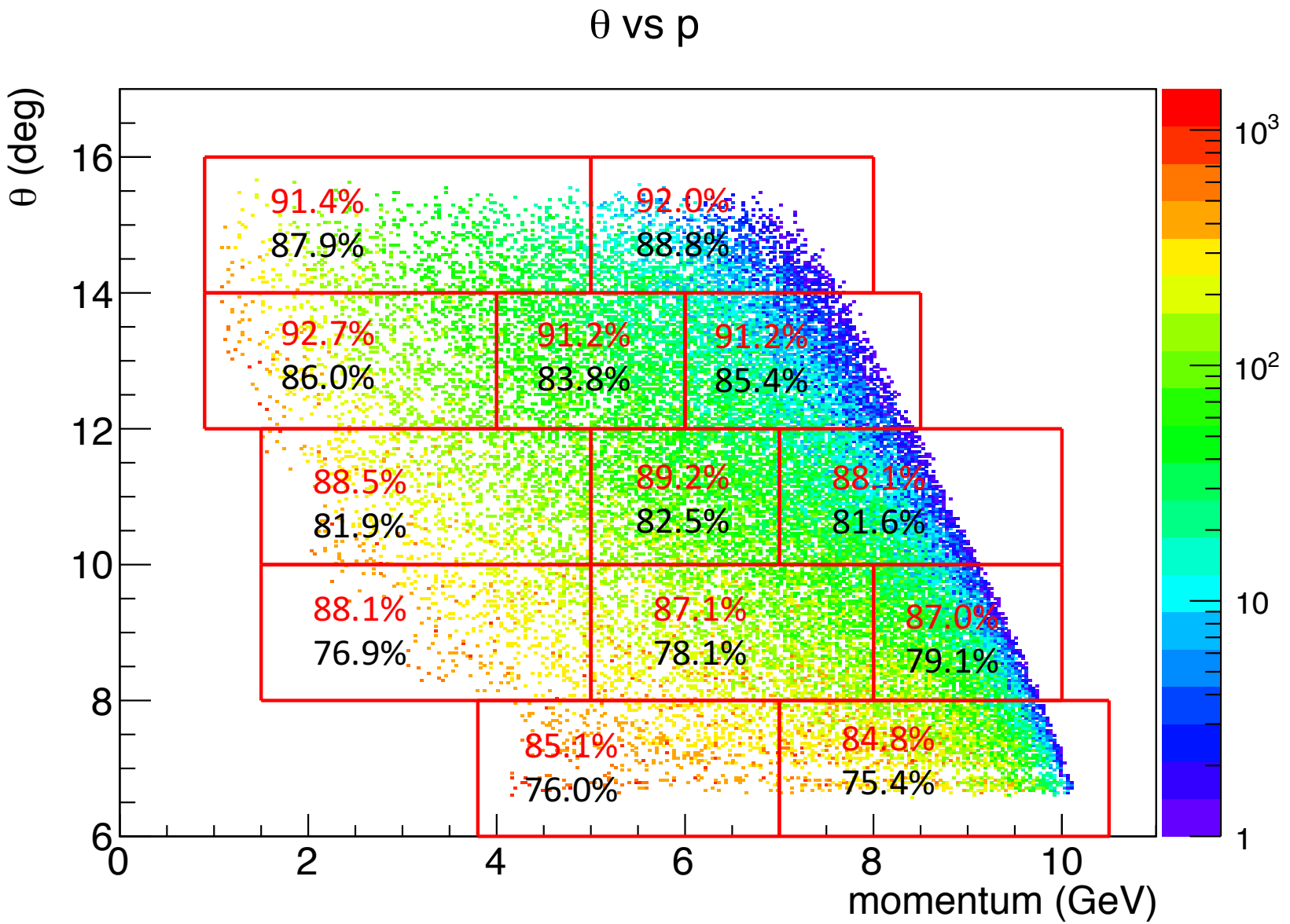
- Accurate track requires all hits of the track must be the ”best” reconstructed hit for the MC hit
- “best” reconstructed hit requires the hit must be the closest reconstructed hit for the MC hit, it must contains contribution from the MC, and the reconstructed hit cannot be over 3 strips away from the MC hit
- Number weighted by DIS cross section





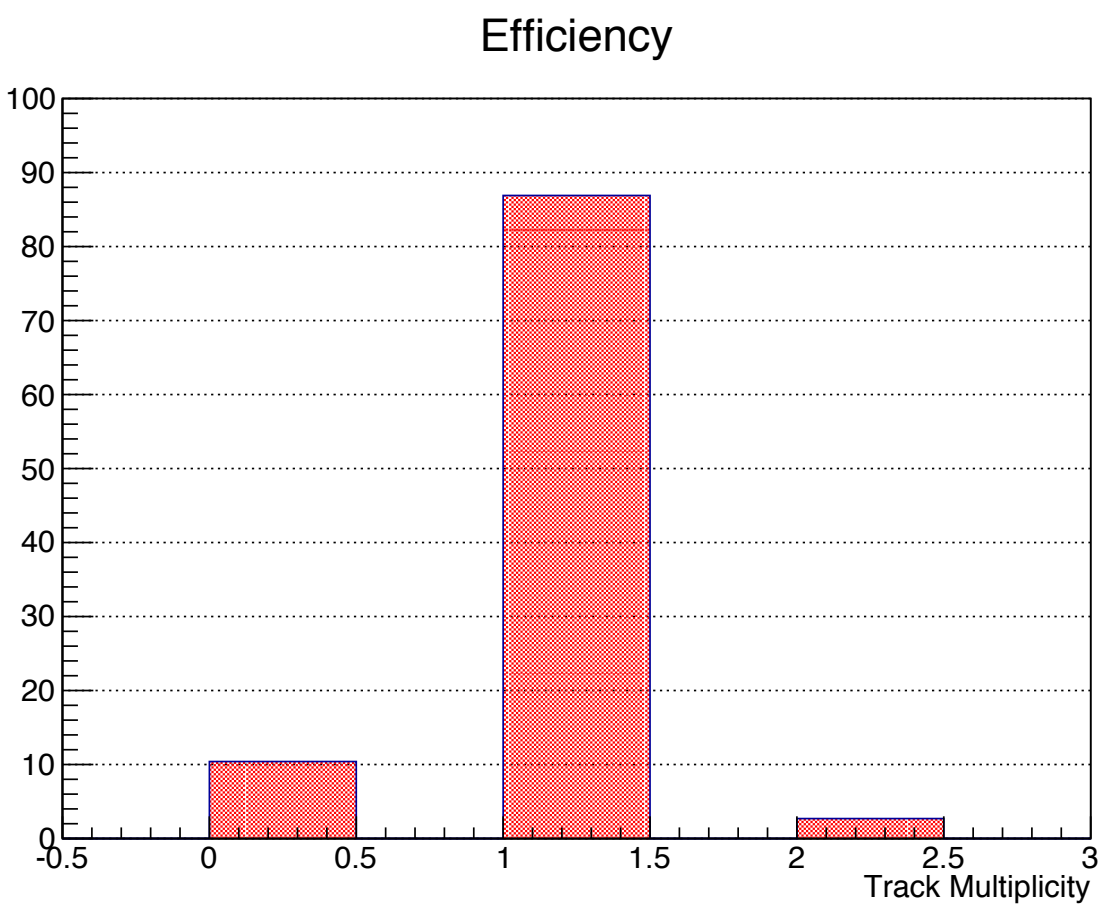
Tracking results – SIDIS FA

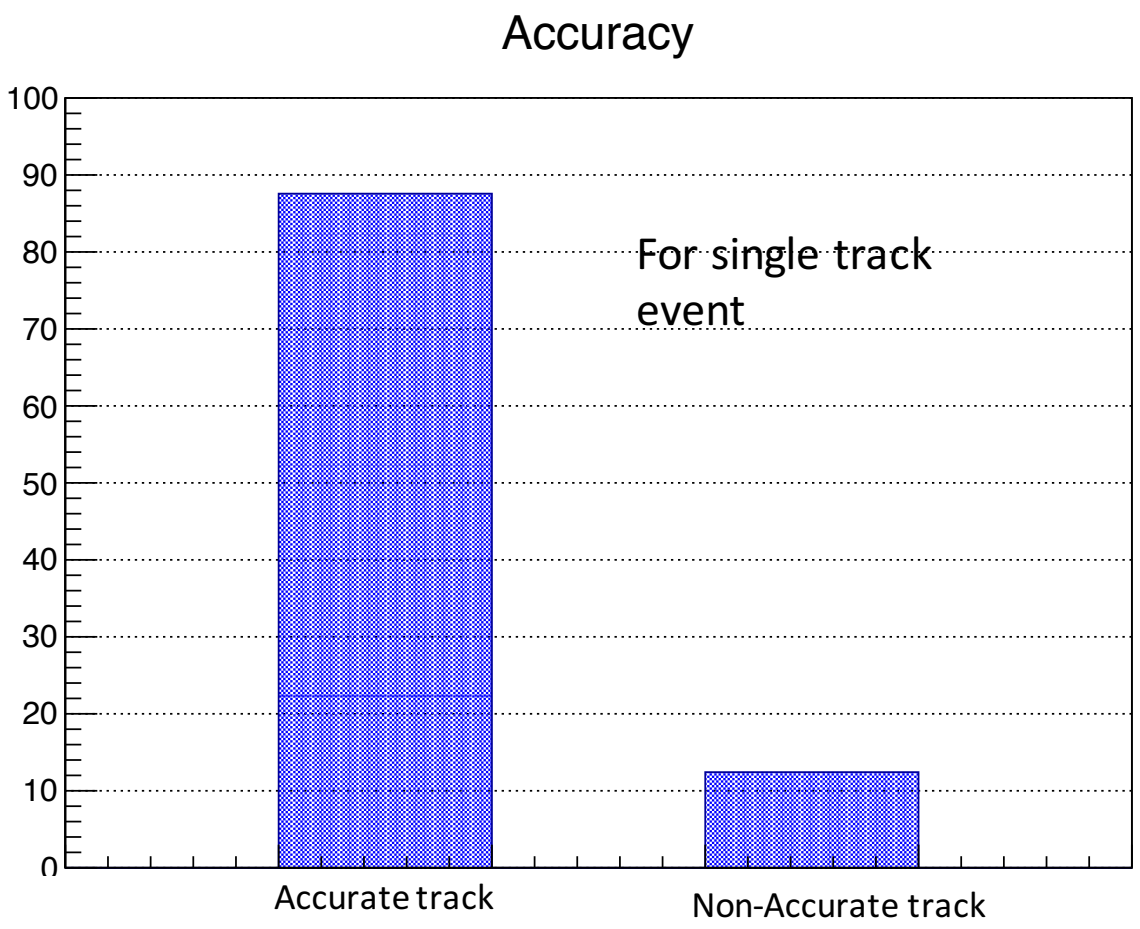
Efficiency in red
Accuracy in black



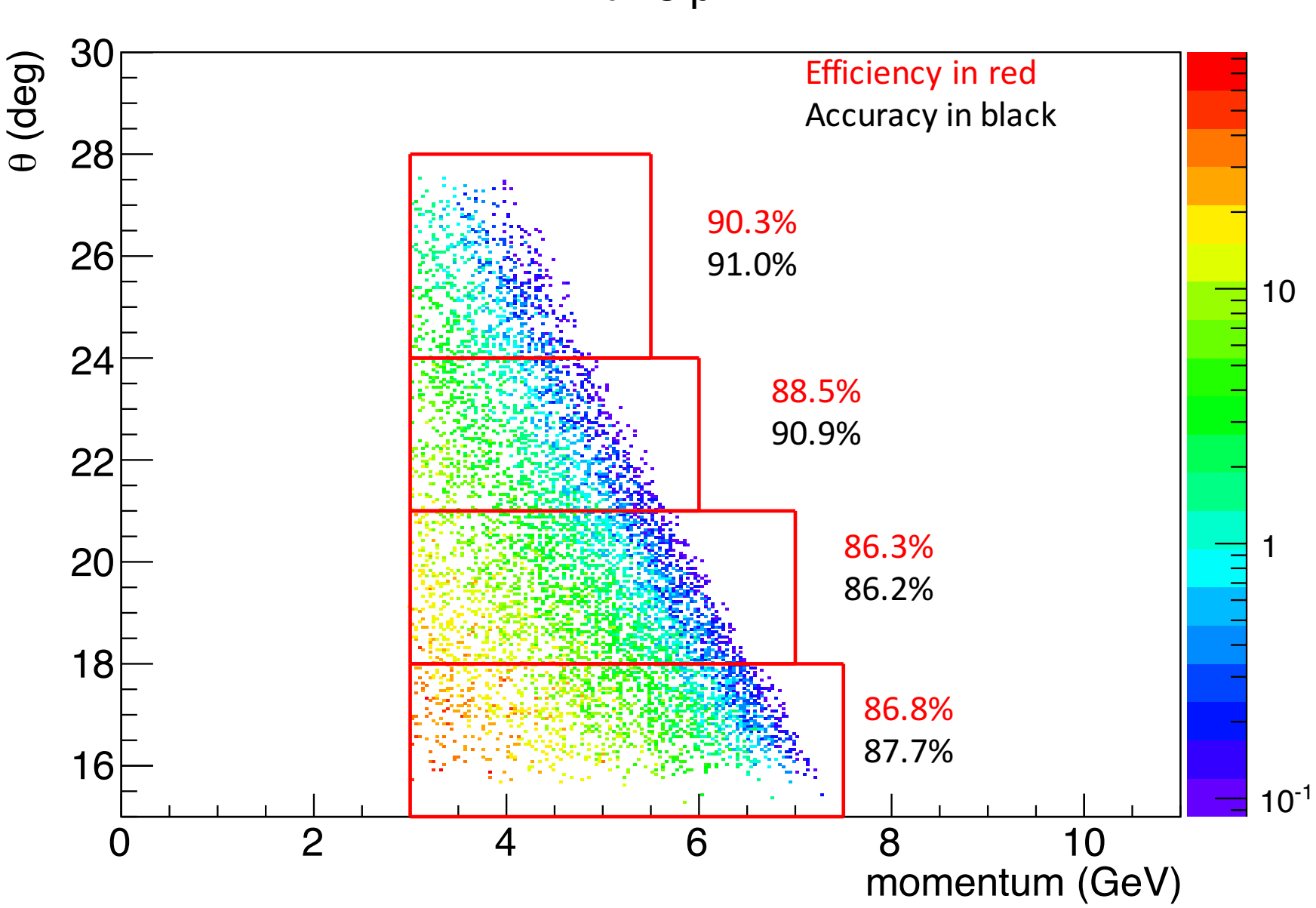
Tracking results – SIDIS LA

- Accurate track requires all hits of the track must be the ”best” reconstructed hit for the MC hit
- “best” reconstructed hit requires the hit must be the closest reconstructed hit for the MC hit, it must contains contribution from the MC, and the reconstructed hit cannot be over 3 strips away from the MC hit
- Numbers weighted by DIS cross section





Tracking results – SIDIS LA



Alternate Chip Options

- VMM3: Developed by BNL for ATLAS
  - Good
    - digital output with on board zero suppression
    - High rates
    - suitable for large detectors,
  - Bad
    - single sample; does not allow pileup correction or time based background rejection

Alternate Chip Options: VMM

APV (ANALOGUE)

APV (250 nm CMOS)

- Pipeline depth: max. 192 clocks
- Trigger latency: max. 3 us
- Noise: < 500 e- intrinsic >750..1400 e- on detector
- dynamic range: 25 fC
- Detector capacity: 18… < 60pf
- ADC ext. 4096/1000 [counts/baseline]
- Gain: fixed CSA gain 100uA/mip, 5 output signal gains (in step of 20%)
- Timing jitter : ½ (1/fc) [+- 12ns]
- Shaping times: 50 ns adjustable to 80 ns
- max readout rate: 7 kHz

VMM (DIGITAL)

SRS
Scalable Readout System

VMM (130nm CMOS)

- Pipeline depth: 64 digital frames (peak)
- Trigger latency: (self triggered) or L0 (12.8us)
- noise : < 400 e- on 10x10 detector reported
- dynamic range: expect >> 25 fC
- Detector capacity: 30pF …. < 1nF
- ADC: embedded, 10 bit
- Gains: 8 CSA gains [0.5..16mV/fC]
- Timing jitter: 20 bit t-stamp, 1ns resolution
- Shaping times: 4 [25… 200ns]
- max readout rates: estimated 4 MHz/ch

Alternate Chip Options: VMM: SRS version