Updates from the SoLID-GEM Chinese Collaboration

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for the SoLID-GEM Chinese Collaboration

University of Science and Technology of China

SoLID Collaboration Meeting
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JLab

SoLID-GEM Chinese Collaboration

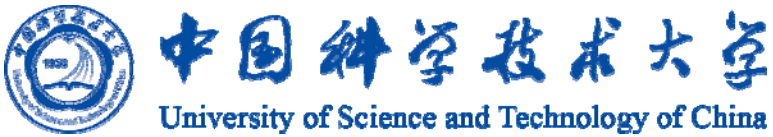
China Institute of Atomic Energy (CIAE)

Lanzhou University

Institute of Modern Physics, CAS (IMP)

Tsinghua University

University of Science and Technology of China (USTC)



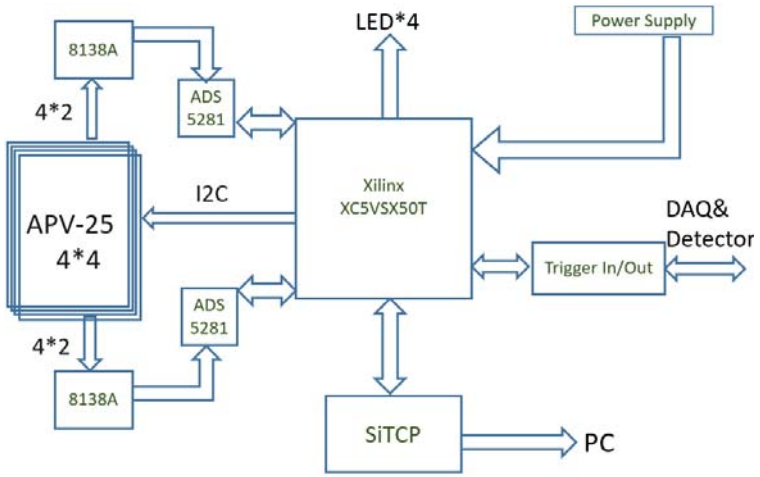
LZU

Lanzhou University

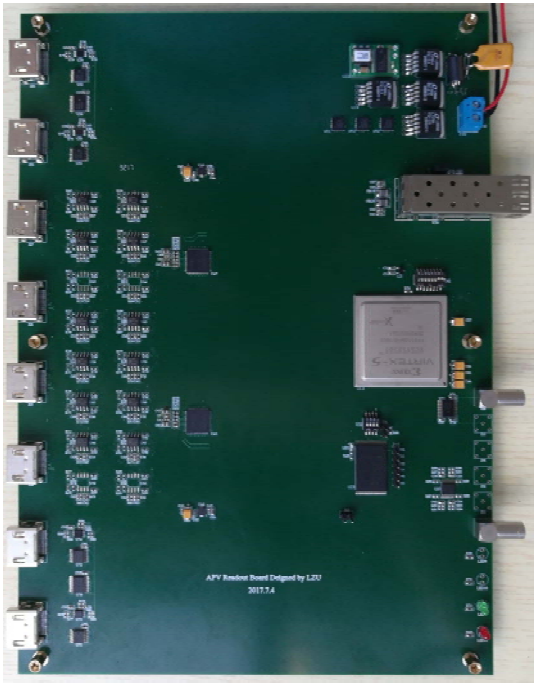
- Recent development on DAQ with APV25 readout

DAQ Design and development

Design Diagram



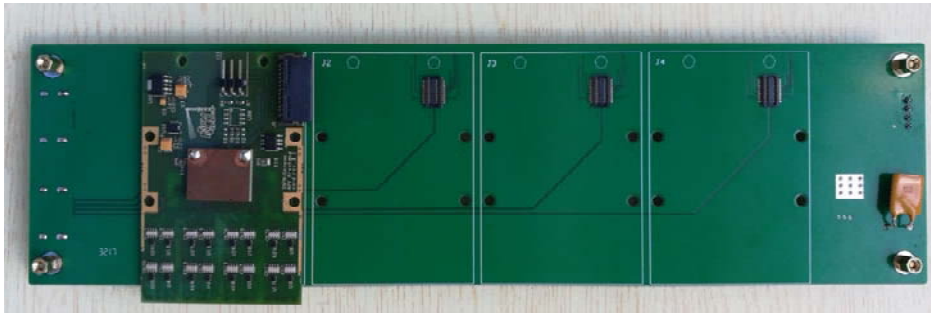
DAQ board



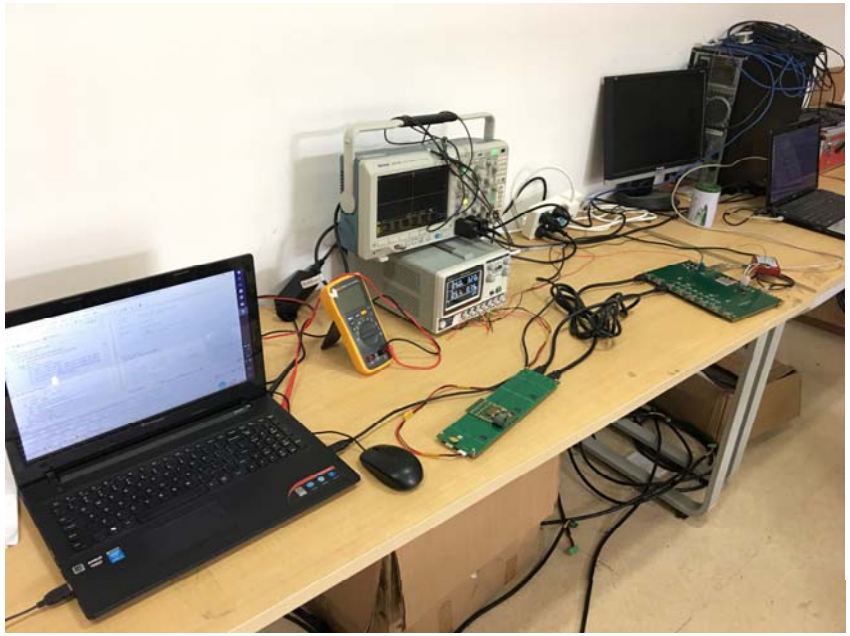
Comparison with MPD

	New DAQ	MPD
Chip	Xilinx XC5VSX50T: 4.752Mb-RAM	Altera EP1AGX50DF : 2.475Mb-RAM
Protocol	Ethernet 1000Mbps	VME 60Mbps
I/O	HDMI Type A Easy to buy	
Power	low-voltage power supply	

Backplane board copied from INFN



DAQ Test



0xFA	Detector ID	Board ID	Work Mode
Trigger Number			
Total Trigger Counts			
Time_data[63:32]			
Time_data[31:0]			
Reservel			
Channel No_1 Data		Channel No_2 Data	
Channel No_3 Data		Channel No_4 Data	
.....			
Channel No_125 Data		Channel No_126 Data	
Channel No_127 Data		Channel No_128 Data	
0xFB		Status	
Byte Count			

Data Format

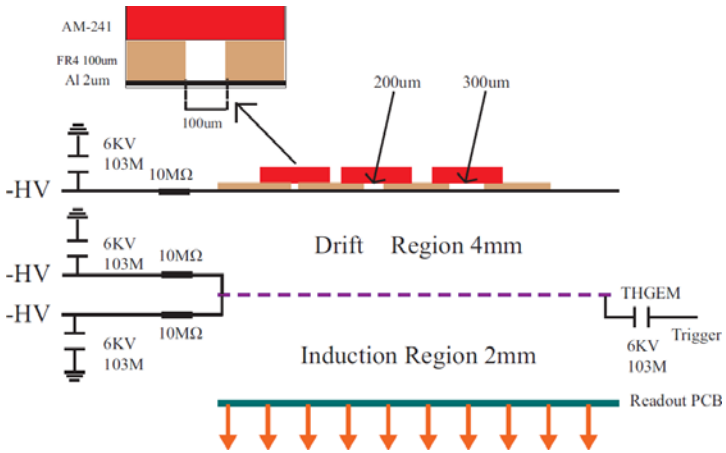
- One APV One sample per trigger : 288B
- One APV 30 samples per trigger : 8.408KB

4 chips * 30 samples * 320 rate *2 hours =800GB

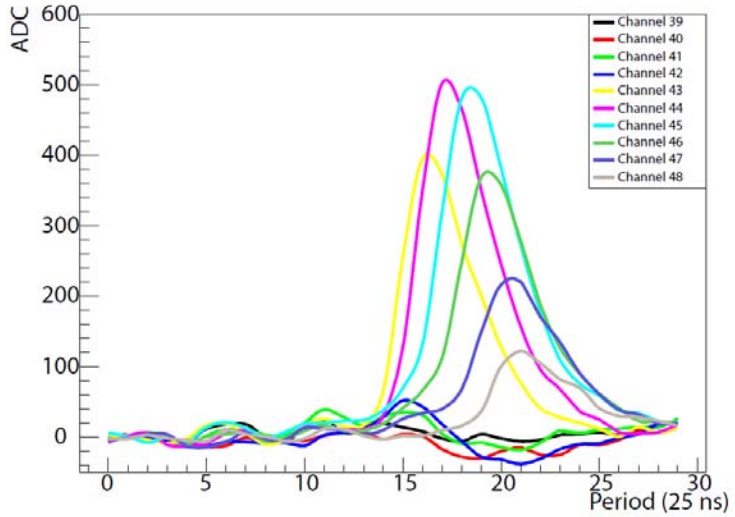
Working OK

Data transmission speed: 120MB/s when writing to memory
Reaching the limit of Gigabit Ethernet.

Test with a Detector

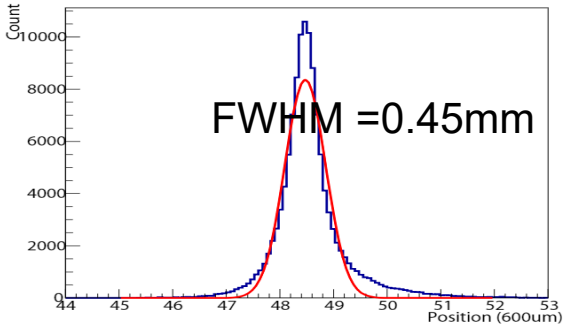


3 Alpha sources (Am-241), each illuminating the detector through a slit. Two-dimensional strip readout with 167 channels in each dimension.

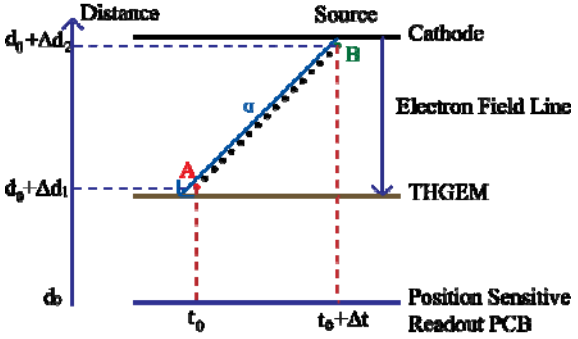


A typical Alpha signal with 30 samples

Position resolution



Position correction based on time information



USTC

中国科学技术大学

University of Science and Technology of China

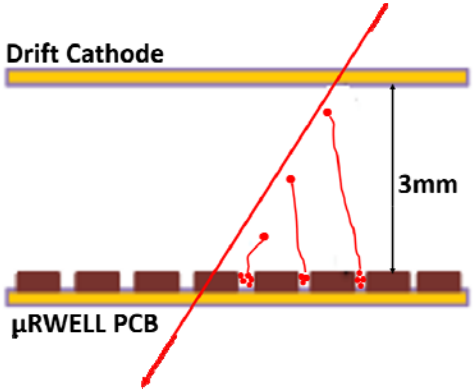
- uRWELL R&D
- VMM readout development

The uRWELL detector

- **Micro-Resistive WELL (µRWELL)** is a novel spark-protected Micro-Pattern Gaseous Detector (MPGD) with a single well-type amplification stage

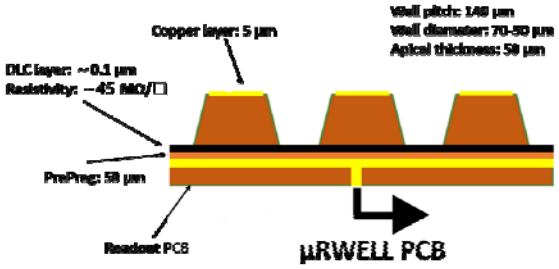
- Resistive Electrode
- One-stage WELL pattern

- Suppress discharge
- Better gain uniformity
- Compact and high granularity
- Fabrication fast



Typical structure of µRWELL detector

(Drift + µRWELL PCB = µRWELL)



Schematic of µRWELL PCB

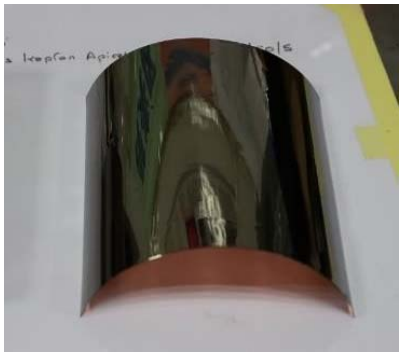
µRWELL PCB: A stack of "readout PCB / insulating pre-preg / DLC resistive layer / well-type amplification structure"

A critical component of µRWELL PCB is DLC resistive electrode which is used to suppress the discharge.

DLC resistive electrode

- We are collaborating with State Key Laboratory of Solid Lubrication, Lanzhou Institute of Chemical Physics, Chinese Academy of Sciences on DLC production.

Sigma/mean=12%



72 MΩ/□	62 MΩ/□	60 MΩ/□
64 MΩ/□	57 MΩ/□	63 MΩ/□
71 MΩ/□	59 MΩ/□	66 MΩ/□

a DLC sample of 15cm × 15cm,
resistivity uniformity: ± 12%

New sputtering system

A New sputtering system (Hauzer 850) is ready to make larger area DLC samples.

Chamber size: Φ800mm×900mm
Best Sample size (up to): 500mm×500mm (Rigid substrate),
500mm × 1900mm (Flexible substrate)

2-D μRWELL PCB with DLC

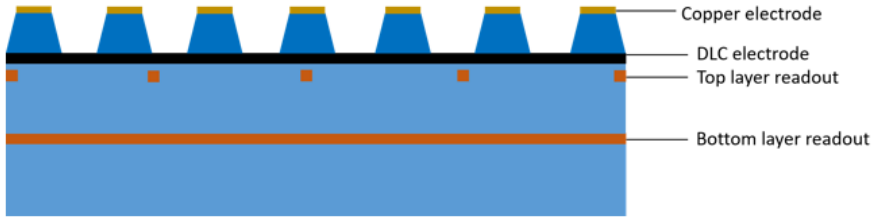
A 2-D μRWELL PCB with 15cm×15cm DLC was designed and fabricated. The DLC was made in China

μRWELL PCB

- Sensitive area: 10cm×10cm divided into 4 sectors
- Well pitch: 140 μm
- Pre_preg (50 μm) isolate the DLC electrode from readout strip

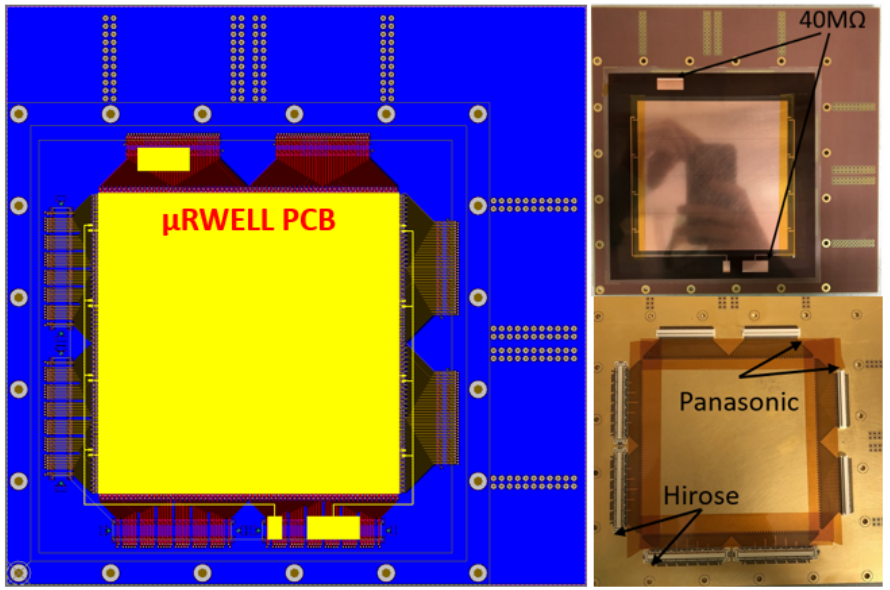
2-D readout strip

- Pitch: 400 μm
- Top layer: 80 μm
- Bottom layer: 350 μm
- Insulate thickness: 50 μm
- Readout strip channel: 1024



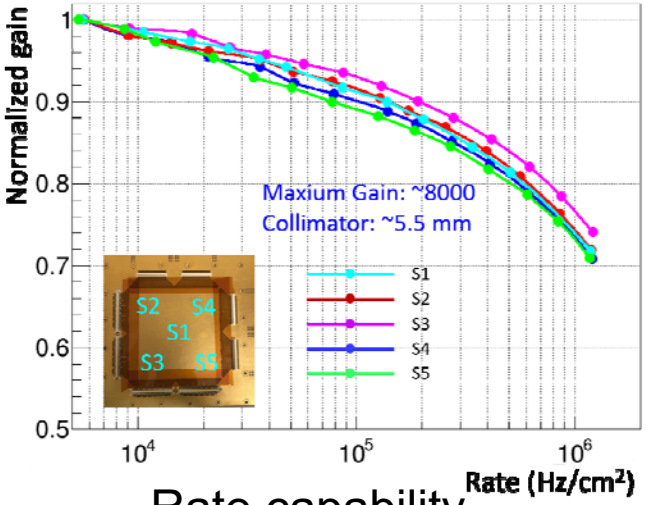
Schematic of μRWELL PCB

All the readout strips are connected to 4 HIROSE (for laboratory test) / PANASONIC (for beam test) connectors.



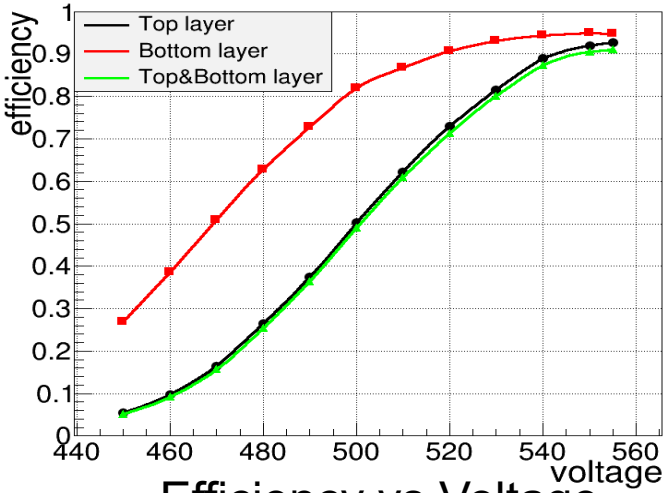
Performance

~ 100 kHz/cm2 for 8keV X-rays

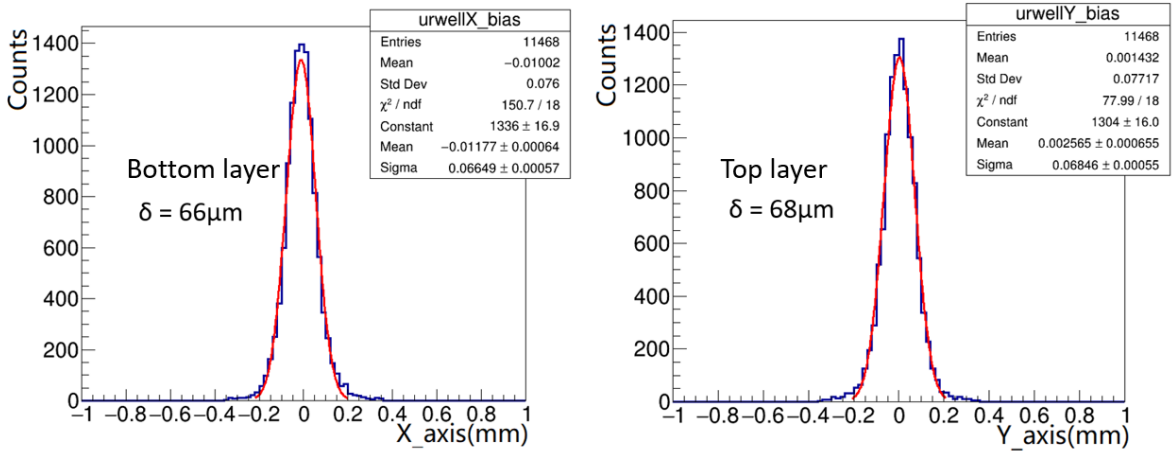


Rate capability

Efficiency > 90%



Efficiency vs Voltage



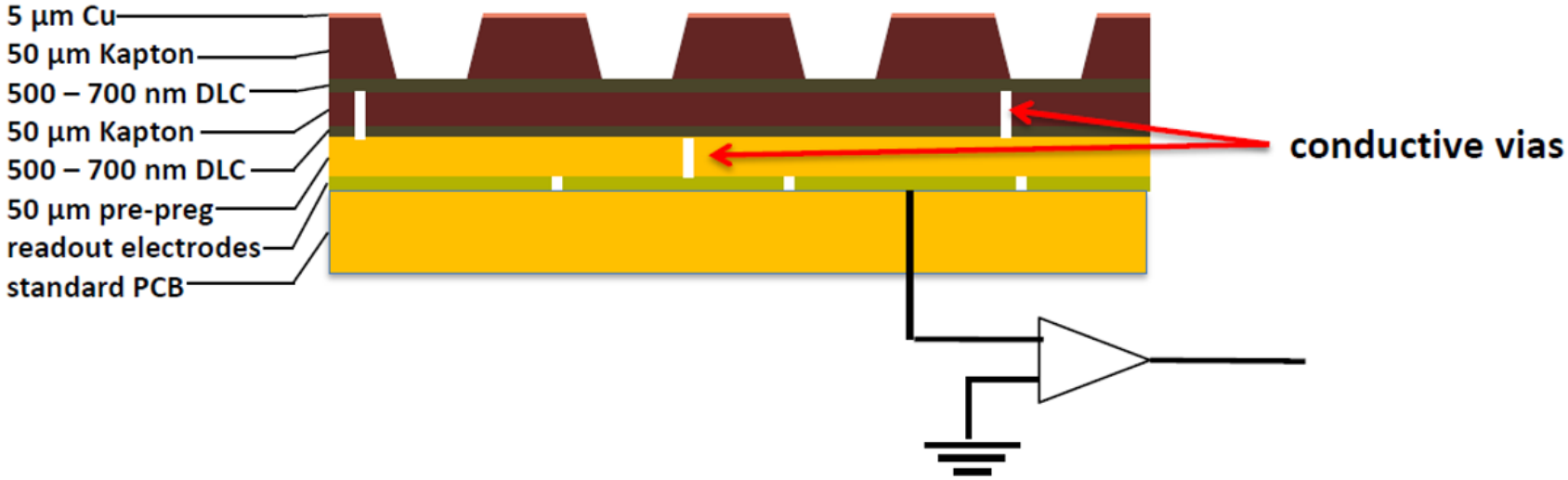
Position resolution

R&D on high-rate uRWELL

- High rate uRWELL aiming for > ~ 1 MHz/cm2
- Collaborating with G.Bencivenni from INFN
- Two Approaches
  - Double-resistive layer
  - Conductive-Dashed Grid

Double-resistive layer

Reduce the path of the current on the DLC surface by implementing a matrix of conductive vias connecting two stacked resistive layers. A second matrix vias connects the second resistive layer to ground through the readout electrodes.

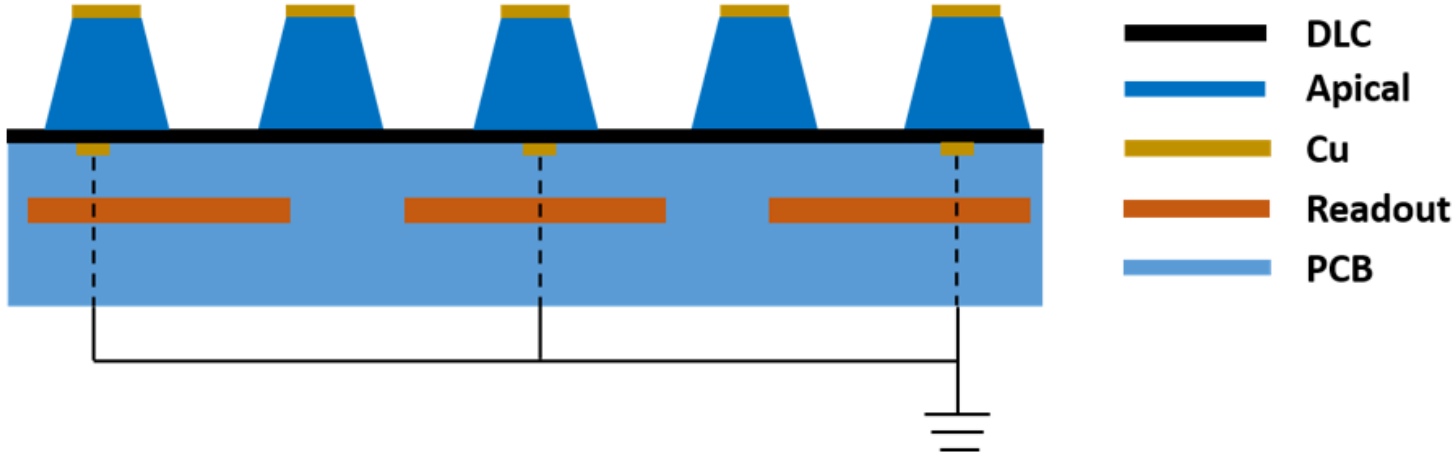


From G.Bencivenni, *The "MPGD Stability" workshop, 21-June-2018*

The engineering/industrialization of the double-resistive layer is difficult due to the manufacturing of the conductive vias on kapton foil. This solution was abandoned.

Conductive-Dashed Grid

The copper clad on the DLC is etched to dash strips and grounded at every a few mm.
The charge collected on the DLC can be quickly released via the grounded copper strips.
New combined structure (Cu/DLC/APICAL/Cu) is required to make high-rate µRWELL PCB.



Schematic of Conductive-Dashed Grid for high-rate µRWELL PCB

Technique for depositing copper on DLC needs to be developed.
This work is supported by a RD51 common project: DLC based electrodes for future resistive MPGDs.

RD51 Common Project

- DLC based electrodes for future resistive MPGDs

Title of project: *DLC based electrodes for future resistive MPGDs*

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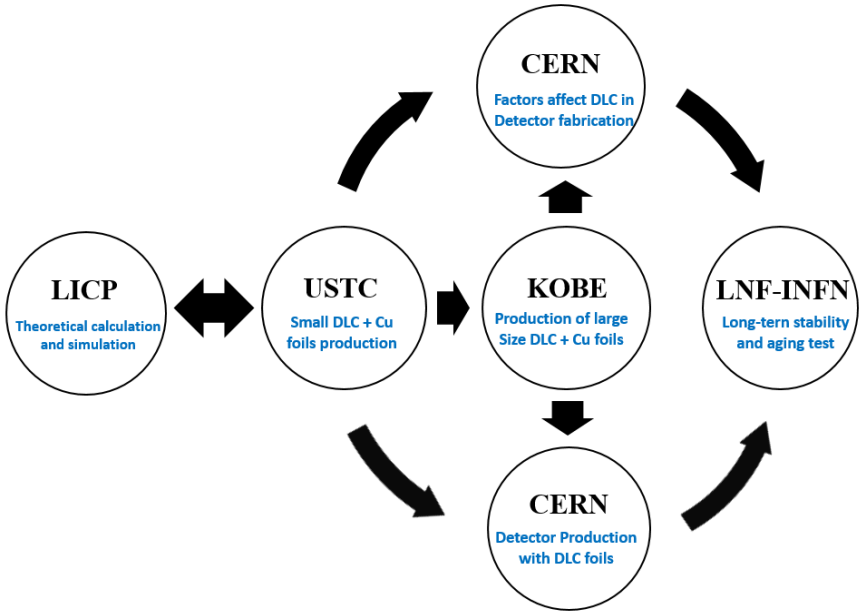


USTC is organizing this project.

Progress on copper coated DLC

Deposit copper on DLC by magnetron sputtering was developed.

1. Deposit DLC on APICAL/Cu substrate
2. Deposit copper on DLC/APICAL/Cu substrate

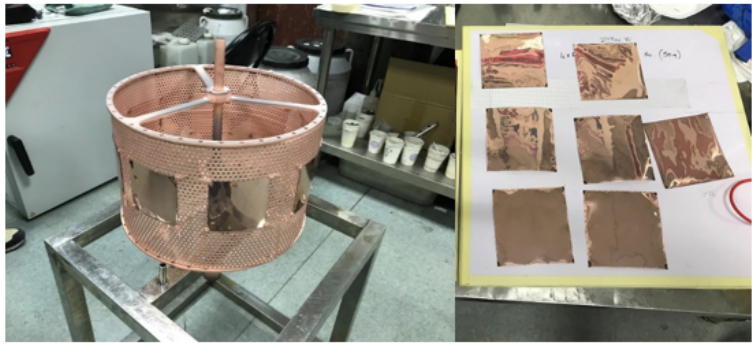
Good adhesion between DLC and copper.

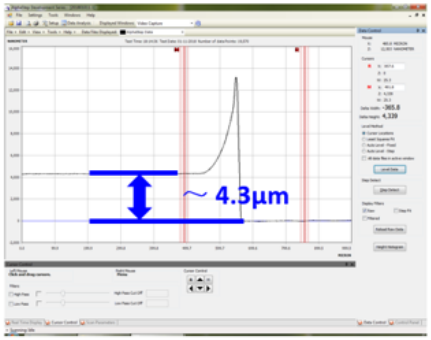
The thickness of copper can be adjusted from 1 µm to 5 µm.

Several substrates have been tried to make the Conductive-Dashed Grid µRWELL PCB.

Bending stress testing

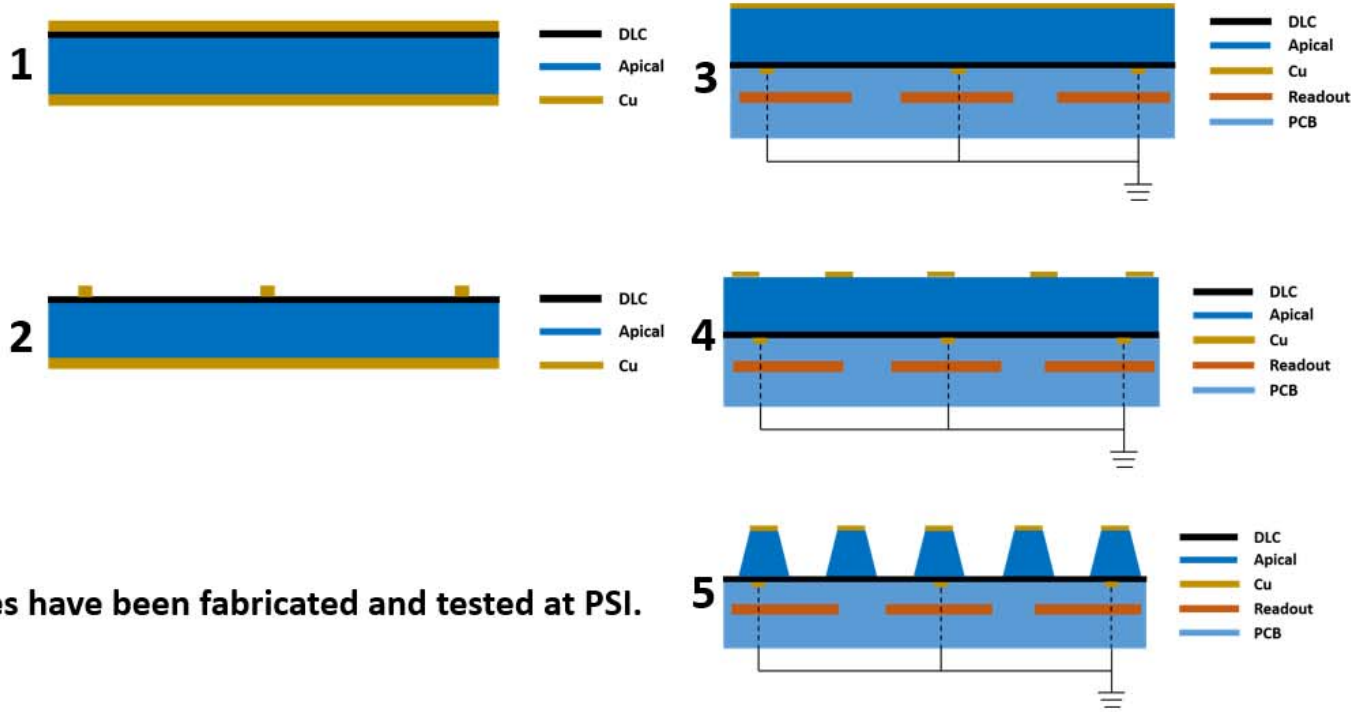
Cross-cutting testing





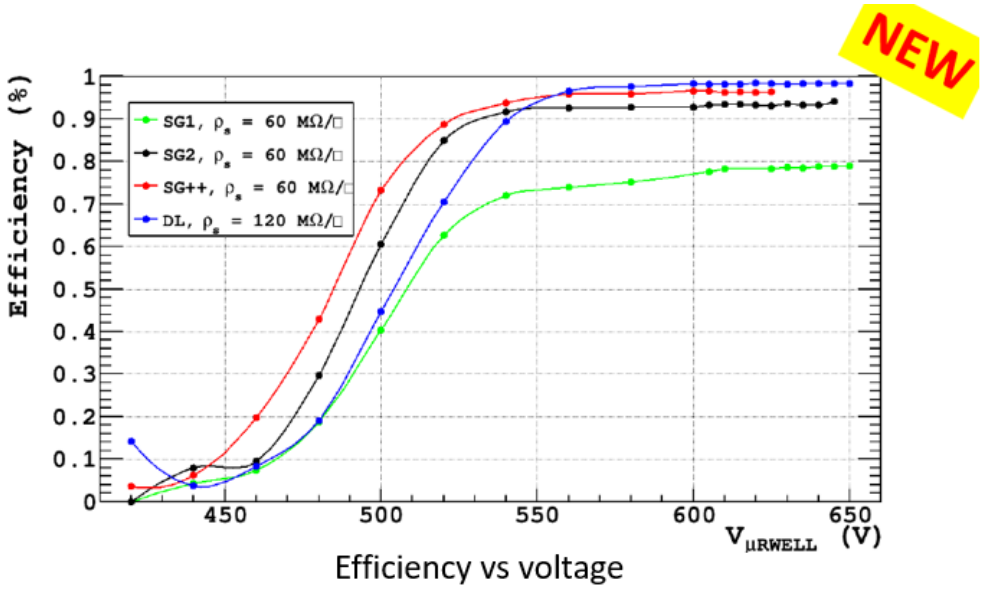
Conductive-Dashed μRWELL PCB

1. Cu/DLC/APICAL/Cu substrate
2. Etch the copper clad on DLC to dash strip
3. Glue the readout PCB and substrate
4. Etch the copper clad on the APICAL
5. Etch APICAL

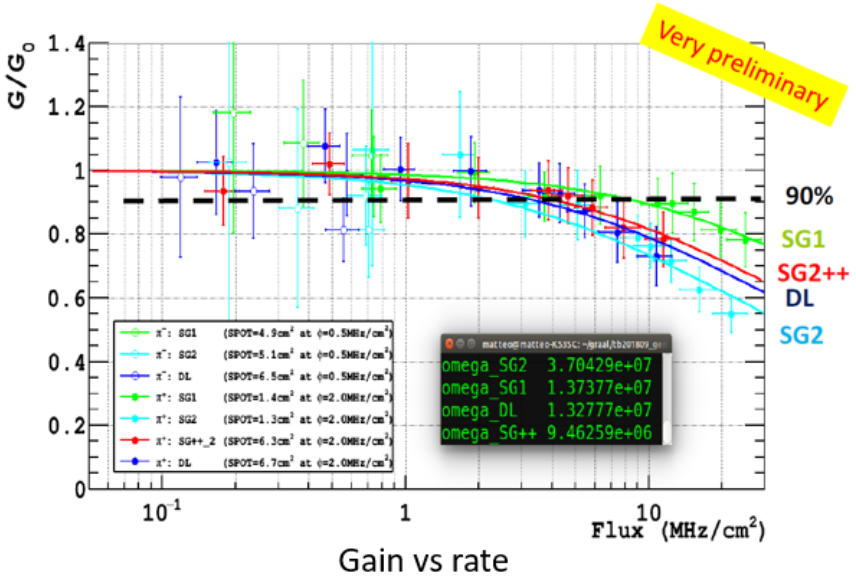


Several high-rate μRWELL prototypes have been fabricated and tested at PSI.

Performance



Efficiency vs voltage



Gain vs rate

Preliminary result from Giovanni

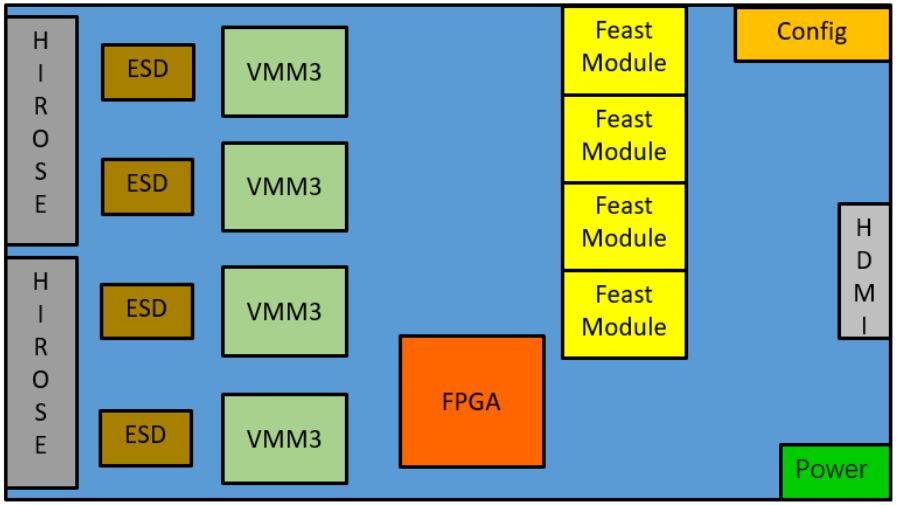
Conductive-Dashed Grid: SG2++

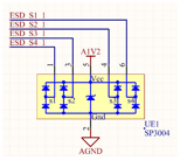
The resistive electrode of SG2++ was made by a new combined structure (Cu/DLC/APICAL/Cu) from USTC.

- Efficiency: 97% @SG2++
- Rate capability: Gain drop 20% @10 MHz/cm^2

Design of a VMM-based FEE card

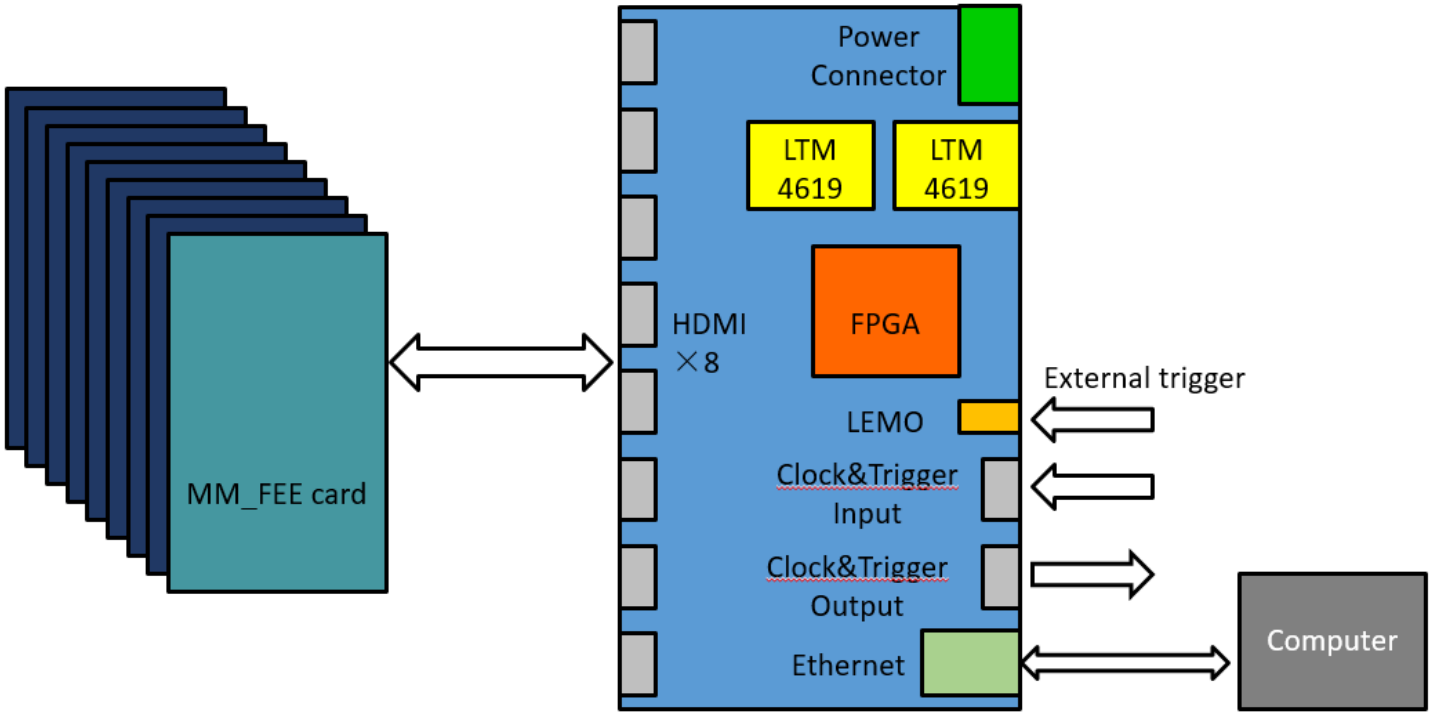
- Two 140-pin Hirose connector, four VMM chips ➔ 256 channels
- 64 4-channel ESDs (SP3004) for input protection
- HDMI with four high-speed Differential pairs (~340Mbps bandwidth) for output.





Design of a DAQ board

- 8 HDMIs (8 × 256 channels), scalable.
- Receive and fan out the clock and trigger signal
- Both auto-trigger and external trigger available.



Integration and test

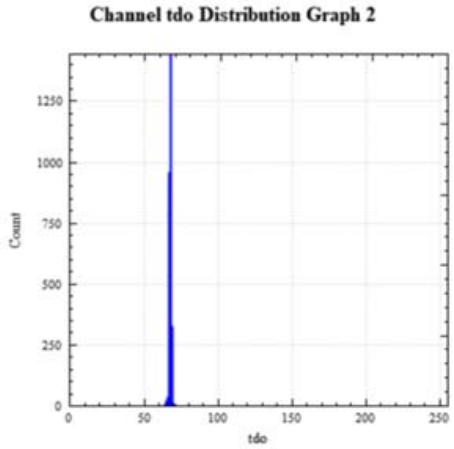
FEE noise:

Standalone: Vp-p<=4mV, Vrms<=800uV

With detector: Vp-p<=20mV, Vrms<=3mV

Timing resolution:

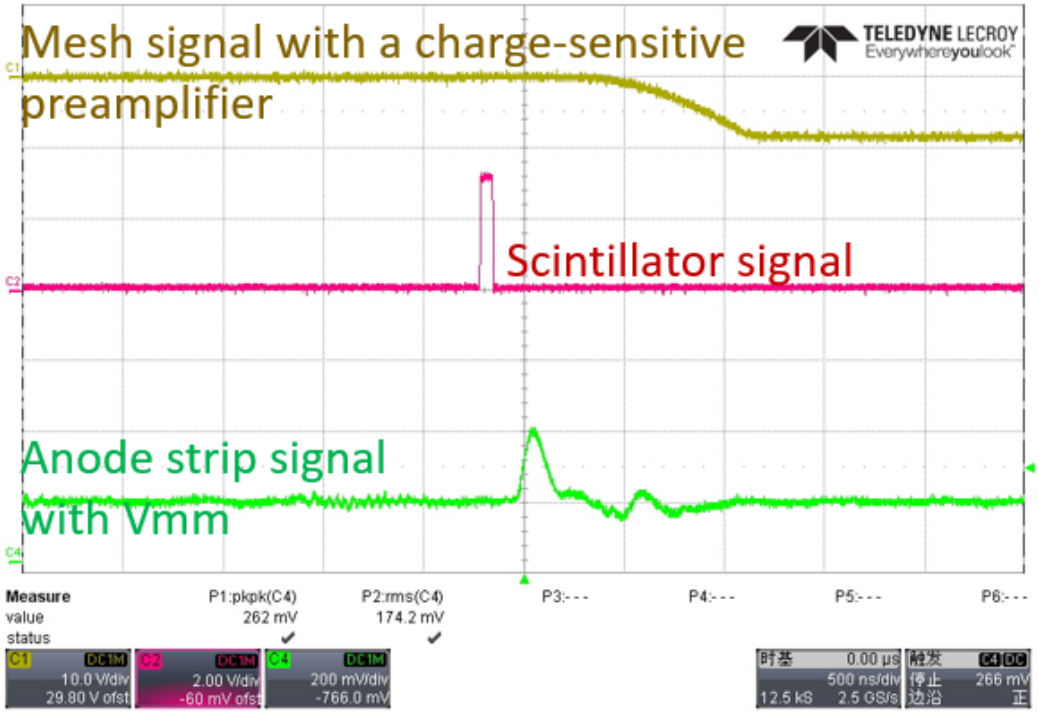
RMS = ~0.5ns



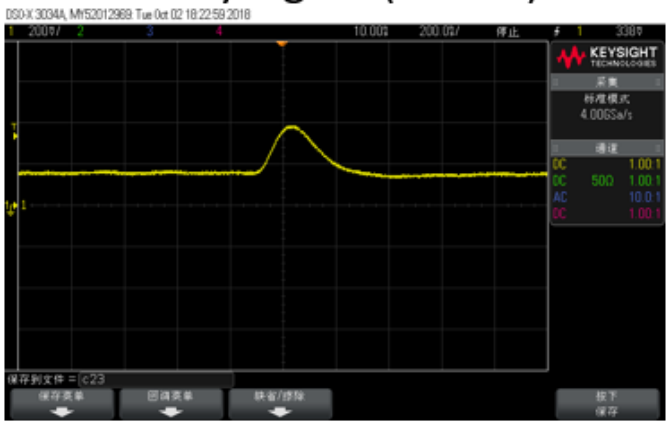
A Micromegas detector

Signal with cosmic rays and X-rays

Testing with cosmic rays and 5.9keV x-rays



cosmic ray signal (anode)



X-ray signal (anode)