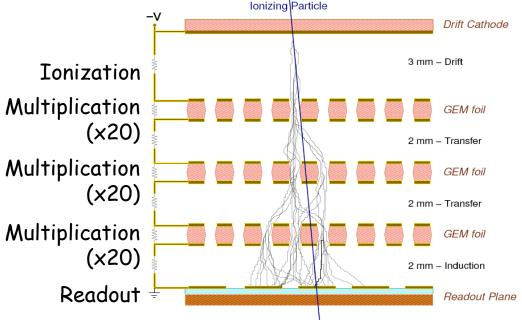
GEM Detectors for SoLID

Nilanga Liyanage and Knodo Gnanvo

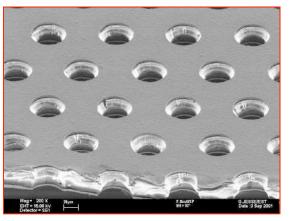
University of Virginia

Why GEMs?

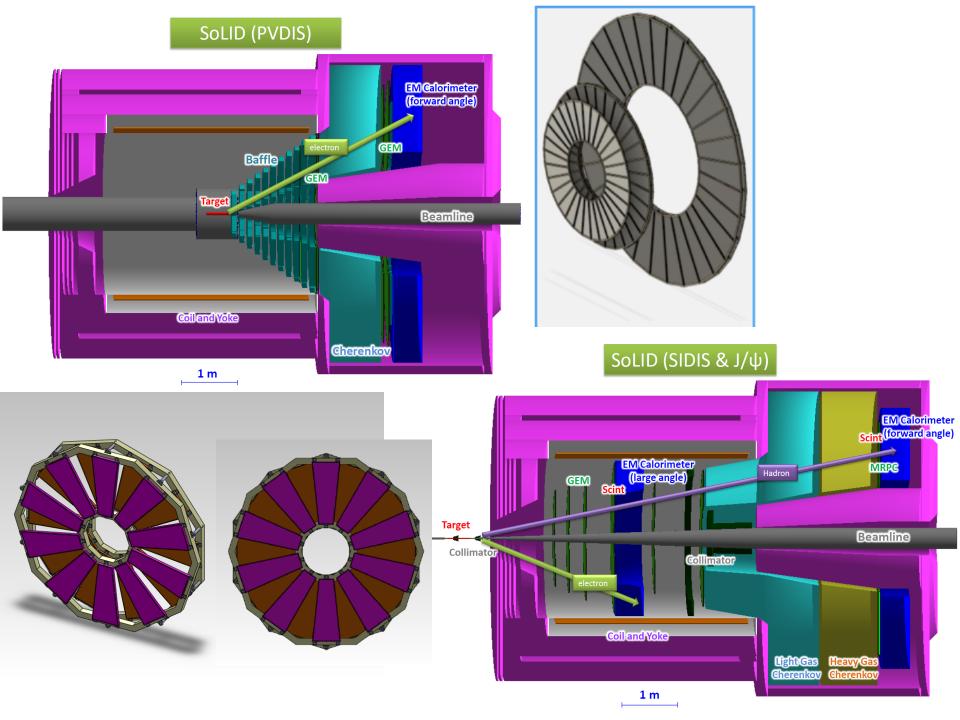
- SoLID concept leads to high rate in trackers: and requires good resolution.
 Gas Electron Multiplier (GEM) detectors provide a cost effective solution for high resolution tracking under high rates over large areas.
 - Rate capabilities higher than many MHz/cm²
 - High position resolution (< 75 μ m)
 - Ability to cover very large areas (10s 100s of m²) at modest cost.
 - Low thickness (~ 0.5% radiation length)
 - Already Used for many experiments around the world: COMPASS, Bonus, KLOE, TOTEM, STAR FGT, ALICE TPC, pRad etc.
 - And planed for many future experiments:, CMS upgrade, SoLID, Moller, P2 @ Mainz



GEM foil: 50 μ m Kapton + few μ m copper on both sides with 70 μ m holes, 140 μ m pitch



Novel technology: F. Sauli, Nucl. Instrum. Methods A386(1997)531



Major change in plans since last meeting

- Separated into baseline equipment and enhancements
 - Baseline:
 - Only GEM layers 1, 3, 4,5 for SIDIS: built by the UVa group
 - Reuse electronics from SBS and TDIS
 - Enhancements
 - GEM layers 2 (and 6 ?): Funded and Built by the Chinese collaboration
 - New electronics for these two layers and to replenish others

Plane	Z (cm)	R _I (cm)	R _O (cm)	Active area (m²)	# of channels
1	-175	36	87	2.0	24 k
2	150	21	98	2.9	30 k
3	-119	25	112	3.7	33 k
4	-68	32	135	5.4	28 k
5	5	42	100	2.6	20 k
-6	92	55	123	3.8	<u>26 k</u>
total:				~20.4	~ 161 k

105 k channels Needed for baseline

SIDIS GEM full configuration

• Six locations instrumented with GEM:

• PVDIS GEM modules can be re-arranged to make all chamber layers for SIDIS. - move the PVDIS modules closer to the axis so that they are overlapping with each other

100						
Plane	Z (cm)	R _I (cm)	R _o (cm)	Active area (m²)	# of channels	
1	-175	36	87	2.0	24 k	
2	-150	21	98	2.9	30 k	-100
3	-119	25	112	3.7	33 k	-150 -100 -50 0 50 100 150 v
4	-68	32	135	5.4	28 k	PVDIS
5	5	42	100	2.6	20 k	50
6	92	55	123	3.8	26 k	
total:				~20.4	~ 161 k	

- More than enough electronic channels from PVDIS setup.
- The two configurations will work well with no need for new GEM or electronics fabrication.

- Instrument five locations with GEMs:
- 30 GEM modules at each location: each module with a 12-degree angular width.

Location	Z (cm)	R_{min} (cm)	R_{max} (cm)	Surface (m ²)	# chan
1	157.5	51	118	3.6	24 k
2	185.5	62	136	4.6	30 k
3	190	65	140	4.8	36 k
4	306	111	221	11.5	35 k
5	315	115	228	12.2	38 k
Total				≈ 36.6	$\approx 164 \text{ k}$

Largest GEM module size required: 113 cm x (21-44) cm

With ~5% spares, we will need about 170 k readout channels.

• Large number of readout channels; but cost of electronics going down - cost per channel for the RD51 SRS APV-25 based readout is \sim \$ 3.00 + R&D expenses to optimize electronics for SoLID needs.

"PVDIS" GEM baseline configuration

• We can cover the 4 baseline SIDIS layers with layers 1, 3 and 4 of PVDIS.

Location	Z (cm)	R_{min} (cm)	R_{max} (cm)	Surface (m ²)	# chan
1	157.5	51	118	3.6	24 k
2	185.5	62	136	4.6	<u>- 30 k</u>
3	190	65	140	4.8	36 k
4	306	111	221	11.5	35 k
	215	115	228	12.2	281-
5	515	115	220	12.2	JOK
Total				≈ 36.6	$\approx 164 \text{ k}$

- Need 90 modules of 3 sizes ~ 70 cm, ~80 cm, ~110 cm.
- With 10% spares for each size => 99 modules total over 4 years.
- Well within the capabilities of the UVa group.
 - Built 48 large modules for SBS.
 - @ ~ 20 production modules per year.
 - could double to rate with the person-power requested for SoLID

Baseline Plan for electronics

- Need 105 k channels + 10% spares ~ 115 k chan.
- Reuse from SBS (APV-25) and TDIS (SAMPA)
- SBS will have a total of ~ 155 k of APV-25 (115 k chans. owned by Jlab (from UVa) ~ 40 k owned by INFN).
 - Assuming that we can get these all and ~ 66% survival rate after SBS run, we will have ~ 102 k of APV electronics for SoLID
- TDIS will have 27.5 chan. of SAMPA.
 - Assuming 66% survival: will have 18.k k chans. for SoLID.
 - Sufficient for base line.
 - Warning: SAMPA is not rad-hard
- No electronics funding in the baseline plane: only 0.5 FTE-year at Jlab for reconfiguring the old electronics for SoLID.
- Also assume reusing all upstream electronics modules (SSPs etc, transducers); but these will be obsolete by then and will require replacing.

Ongoing work carried out by Kondo supported by EIC R&D.

• A new EIC prototype GEM with many new features successfully developed.

Moving all readout connections to the outer edge of the circle:
successfully demonstrated with small prototype, now implemented in full size module.

• Composite frames: will reduce cost for SoLID

beam tested at Fermilab last summer

- uRwell prototype
- Planning for a 1 k channel VMM based SRS test stand

EIC Low Cost Frames

Total set of pieces for all 4 frames





pieces fit together to form a frame



Large & Low-mass Forward Tracker GEM for EIC R&D



Going to the test beam at Fermilab FTBF in two weeks from now

Large & Low-mass Forward Tracker GEM for EIC R&D

Common GEM foil design:

- (Univ. of Virginia, Florida Tech, and Temple U.)
- All connections (HV, gas flow structure and FE cards) are made on outer radius end.

2D U-V strips readout (R/O)

- Spatial resolution improvement
- All readout electronics on outer radius end.
- No connectors or metallized vias on R/O

Double-sided zebra connection

- Large density of electronics channels read out on side of the detector (outer radius)
- No electronics on side or inner radius, no multiple scattering or radiation damage issues
- No connectors or metallized vias on R/O

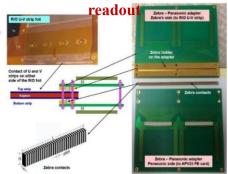




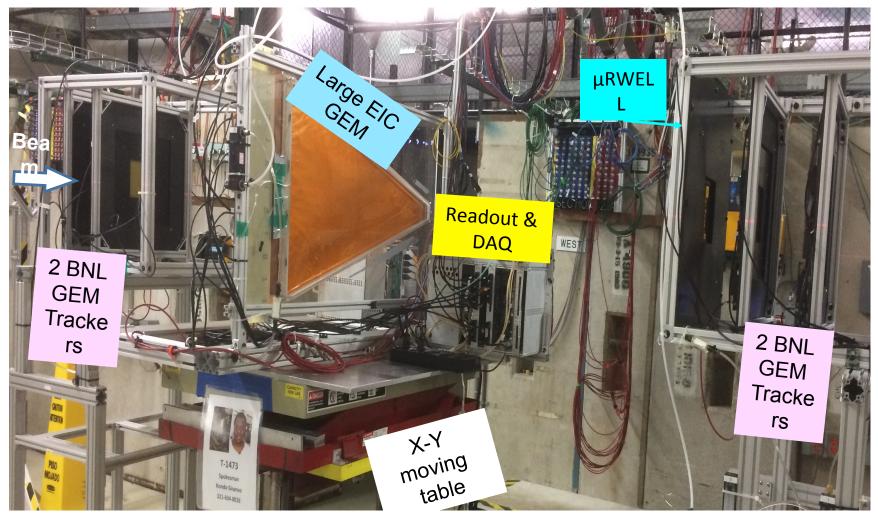
Design of EIC-Proto II 2D U-V strips readout board

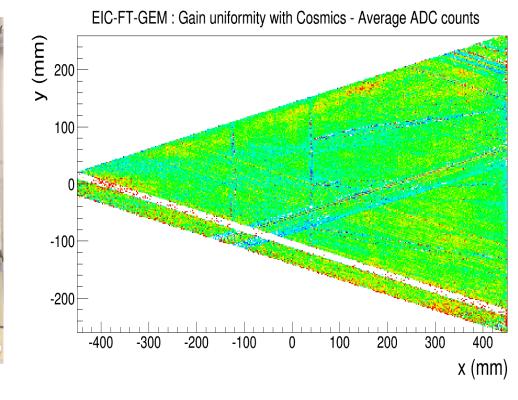
2d U-V strips (5 µm Cu) readout on board, 50 µm Kapton; Pitch: 400 µm
 Top layer: 80 µm U-strips parallel to one radial side
 Bottom layer: 350 µm V-strips parallel to other radial side.

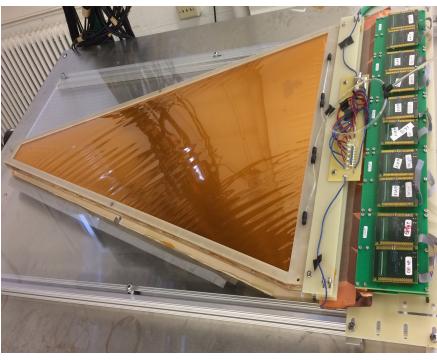
Principle of double-sided zebra connection on flexible PCB



Large GEM Setup in MT6.2b Area at the FTBF (June-July 2018)

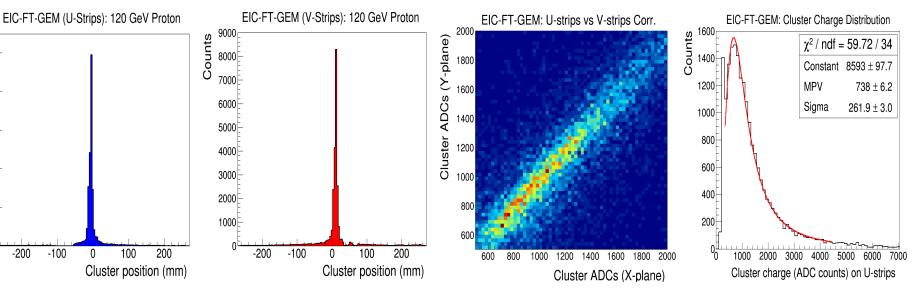




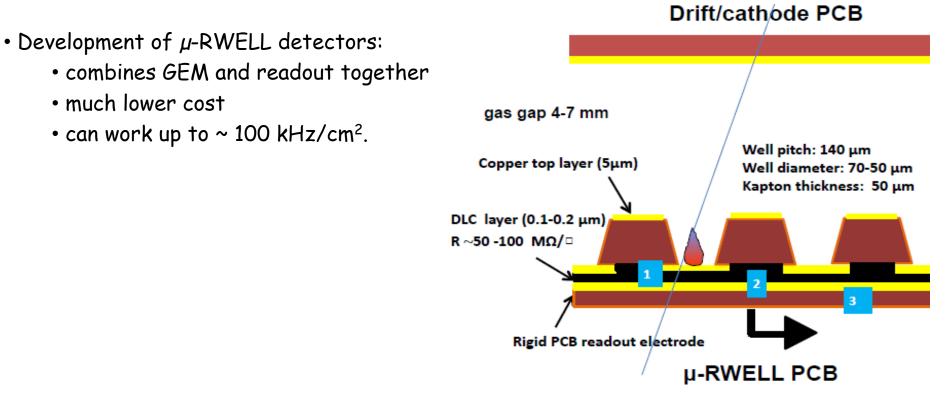


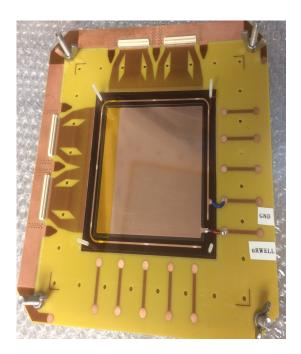
Counts

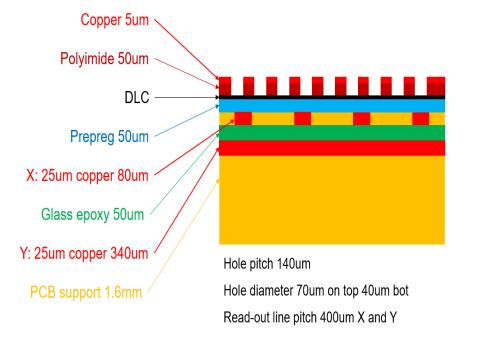
-200

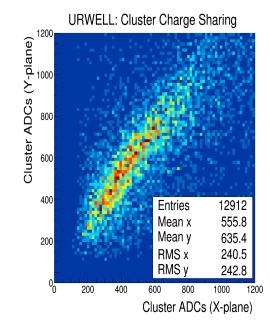


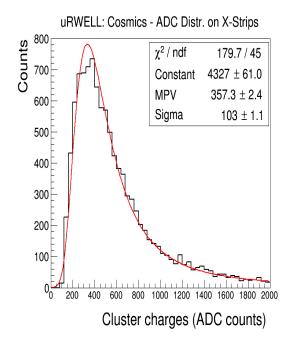
Ongoing work carried out by Kondo supported by EIC R&D.



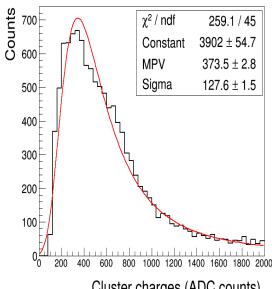




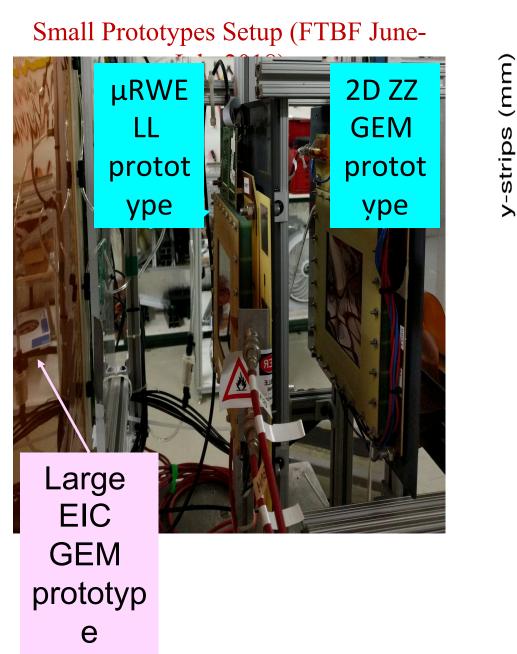




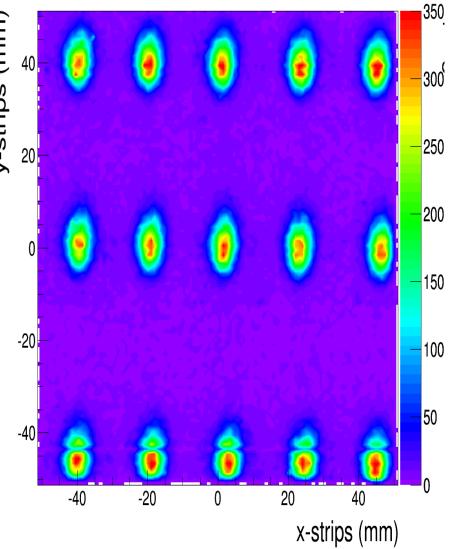
uRWELL: Cosmics - ADC Distr. on Y-strips

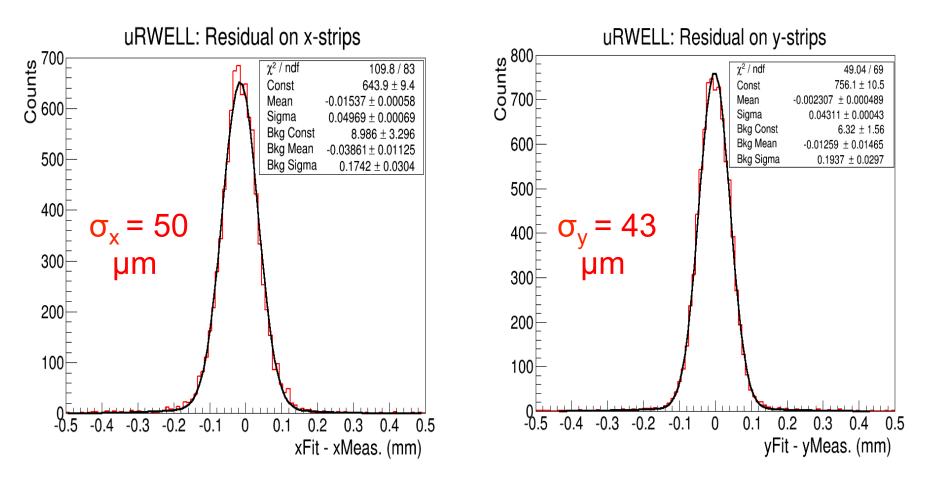


Cluster charges (ADC counts)

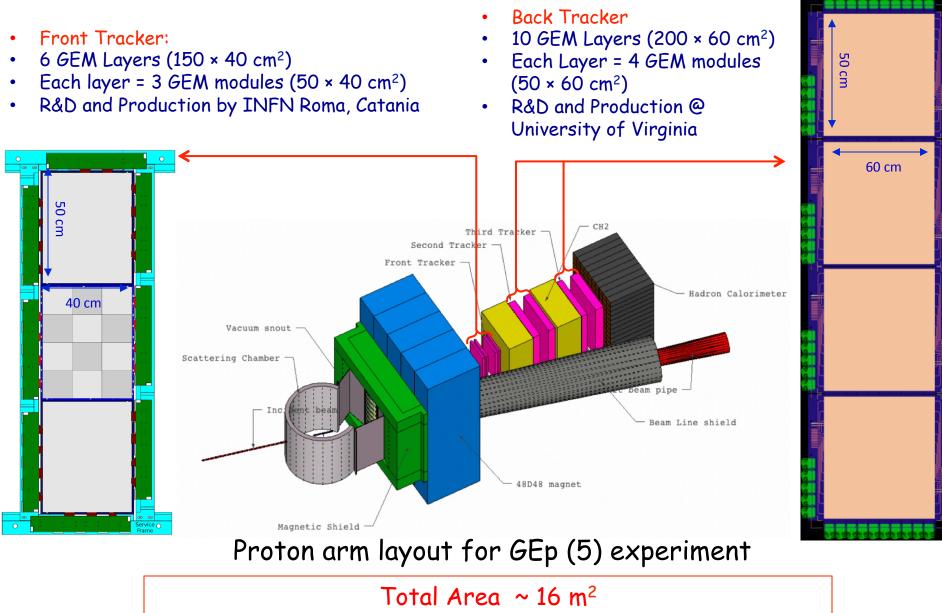


uRWELL: Hit Position Map





GEM Trackers for SBS



SBS GEM Production complete

- •Completed building 48 modules (plan was to build 40) and tested.
- 46 tested modules and all work per specs.
- Foils from CERN very high quality; over 90% yield; mostly on-time delivery.
- Foil QA at every step extremely important.

Ongoing work for SBS GEMs

- Installation of GEM modules into layers now
- Installation and testing of all electronics.
- Working with DAQ group to implement hardware level data reduction.
 - common mode correction
 - pedestal subtraction
 - zero suppression
 - filter out background not correlated with trigger time.

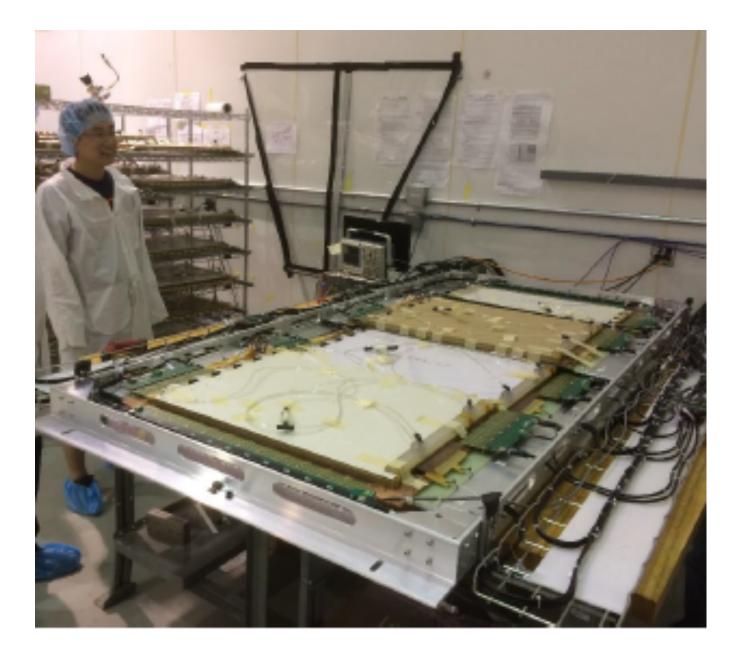
• Working on GEM background suppression and tracking for GMn experiment conditions (rates ~ 100 kHz/cm2)



Status of UVa GEMs for SBS (EEL Clean Room 124)



- 37 Modules for 9 SBS GEM layers already in store at JLab (EEL Clean Room 124)
- Additional 7 modules (+ spares) for 2 remaining layers to be shipped to JLab in the coming weeks (~November 2018)
- 2 INFN SBS GEM layers to be assembled / tested in Testlab CL after 4 INFN BB GEMs installed in BB in TED (Summer 2019)



Alternate Chip Options

- VMM3: Developed by BNL for ATLAS
 - Good
 - digital output with on board zero suppression
 - High rates
 - suitable for large detectors,
 - Bad

•single sample; does not allow pileup correction or time based background rejection

Alternate Chip Options: VMM

APV(ANALOGUE)

APV (250 nm CMOS)

- Pipeline depth: max. 192 clocks
- Trigger latency: max. 3 us
- Noise: < 500 e- intrinsic >750..1400 eon detector
- dynamic range: 25 fC
- Detector capacity: 18... < 60pf
- ADC ext. 4096/1000 [counts/baseline]
- Gain: fixed CSA gain 100uA/mip, 5 output signal gains (in step of 20%)
- Timing jitter : ¹/₂ (1/fc) [+- 12ns]
- Shaping times: 50 ns adjustable to 80 ns
- max readout rate: 7 kHz





VMM (130nm CMOS)

- Pipeline depth: 64 digital frames (peak)
- Trigger latency: (self triggered) or L0 (12.8us)
- noise : < 400 e- on 10x10 detector reported</p>
- dynamic range: expect >> 25 fC
- Detector capacity: 30pF < lnF
- ADC: embedded, 10 bit
- Gains: 8 CSA gains [0.5..16mV/fC]
- Timing jitter: 20 bit t-stamp, 1ns resolution
- Shaping times: 4 [25... 200ns]
- max readout rates: estimated 4 MHz/ch

Alternate Chip Options: VMM: SRS version

