

SoLID DAQ update

SoLID collaboration meeting

January 11 2019

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Outline

- Updated budget
- Trigger rates
 - PVDIS
 - SIDIS
- GEM readout
- Network infrastructure
- Tape Silo
- Streaming / EIC /SoLID / TDIS DAQ laboratory
- Conclusion

Updated budget

- 2016 : 1.9 M\$ (assumed 231 FADCs and 30 sectors)
- 2018
 - 1.8 M\$ (assumes 188 FADCs and 23 VXS crates) assume VXS readout from FADC done, allows readout FADC faster, more FADC per crates is OK
 - 0.9 M\$ Stage 1 : reduce EC channel by 3 no MRPC
 - Trigger rate for SIDIS increases by 15 % from 84 to 97 KHz (or same rate increasing threshold, reduces physics)

First stage baseline

Cost estimation	1 crates per sectors		
FADC 250	5800	145	841000
Cables	2510	100	251000
V1290	11000	0	0
VME64X	11000	0	0
VETROC	4000	0	0
TD	3000	16	48000
VTP	8000	11	88000
SSP	5000	4	20000
VTP	8000	1	8000
TS	4000	1	4000
TID	3000	13	39000
SD	2500	12	30000
VXS crate	15000	12	180000
VME CPU	3400	12	40800
		Total	
SRS computers	20000	1	20000
Shielding		1	50000
SD TD	2500	0	0
Total			
Summing module	1500	150	225000
			1844800
		Total detectors	1844800
	Substracted 145 FADC cost	Total	1003800

Full budget

Cost estimation	1 crates per sectors		
FADC 250	5800	295	1711000
Cables	2510	100	251000
V1290	11000	0	0
VME64X	11000	0	0
VETROC (MRPC)	4000	26	104000
TD	3000	16	48000
VTP	8000	21	168000
SSP	5000	4	20000
VTP	8000	1	8000
TS	4000	1	4000
TID	3000	24	72000
SD	2500	23	57500
VXS crate	15000	23	345000
VME CPU	3400	23	78200
		Total	
SRS computers	50000	1	50000
Shielding		1	50000
Total			
			2966700
		Total detectors	2966700
		Total minus 188 FADs	1876300

PVDIS electron trigger

- Coincidence ECAL and Gas Cerenkov

	Old	Hall D
Singles ECAL	290 KHz	230 KHz
Singles rates Cerenkov	1.9 MHz	803 KHz
Accidental 30 ns	16.5 KHz	4.1 KHz
DIS electron	10 KHz max	7.7 KHz
Total rate	27 KHz	12.1 KHz

Event size data rates PVDIS

				Event size		Data rate MBs	After noise cut	strips firing	event size bytes		MB/s
1	1156	21.17	244.73	3038.03	3038.03	60.76	9.97	115.25	1430.76	1430.76	28.62
2	1374	10.35	142.21	1765.39	1765.39	35.31	5.11	70.21	871.61	871.61	17.43
3	1374	8.81	121.05	1502.71	1502.71	30.05	4.42	60.73	753.92	753.92	15.08
4	2287	3.07	70.21	871.60	871.60	17.43	1.64	37.51	465.61	465.61	9.31
5	2350	2.79	65.57	813.93	813.93	16.28	1.50	35.25	437.60	437.60	8.75
					Total	159.83				Total	79.19
FADC											
	20000						10				
	Event size FADC	Nb channel	Header			Trailer	Sample				
	Calorimeter	14	4			4	12	280			
	Preshower	9	4			4	12	180	400		
	Cerenkov	9	4			4	12	180			
									11600000		
								740	11600000	11.6	
									Total rate	94	MB/s

About 2.9 GB/s for PVDIS at 20 KHz

SIDIS event size

Occupancies with one sample readout by Weizhi , rates for 100 KHz

GEM	Occupancy	Number of strips	XY strips	Strips per chambers	MB/s
1	2.21	453	906	27180	245
2	8.78	510	1020	30600	1184
3	3.63	583	1166	34980	559.5
4	2.31	702	1404	42120	428.7
5	1.78	520	1040	31200	244.71
6	1.3	640	1280	38400	220
Total	20.01	3408	6816	204480	2901

GEM dominating 2.9 GB/s same requirement as PVDIS

SAMPA occupancies SIDIS (160 ns shaping)

Chamber	1 sample %	6 samples %	6 samples Noise cut %	9 samples %	9 samples Noise cut %
1	4.0	10	4.33	8.5	6.1
2	13.7	26.4	11	30.3	13.2
3	5.79	14.2	6.14	17.9	8.38
4	3.76	9.2	3.93	11.8	5.56
5	3.36	8.67	3.80	11.3	5.43
6	2.50	6.5	2.85	8.53	4.10

SAMPA data rates SIDIS (160 ns shaping)

- Occupancies higher than with APV25
- Data rates assuming processing and recording one amplitude for 100 KHz
 - 1 samples : 4.4 GB/s
 - 6 samples : 4.2 GB/s
 - 9 samples : 5.7 GB/s
- Need to evaluate if tracking can be improved offline if record more samples in data file
- Data reduction on the fly desired with additional processing than noise cut

SAMPA tracking efficiency with full background

Efficiency comparison

	APV25	SAMPA 80ns	SAMPA 160ns
FA efficiency 0%	98.7%	97.8%	74.5%
FA efficiency 100%	97.3%	96.7% (95.3%)	74.6% (83.9%)
LA efficiency 0%	98.5%	97.9%	76.7%
LA efficiency 100%	93.4%	95.4%	70.2% (72.3%)

SAMPA: 80ns shaping time comparable with APV25
160ns significantly lower

GEM readout

- VMM3
 - 128 channels
 - no many sample readout but fast integration time 25 ns
 - read time and time other threshold, need to add to simulation to evaluate

SIDIS event size

Occupancies with one sample readout by Weizhi , rates for 100 KHz

GEM	Occupancy	Number of strips	XY strips	Strips per chambers	MB/s
1	2.21	453	906	27180	245
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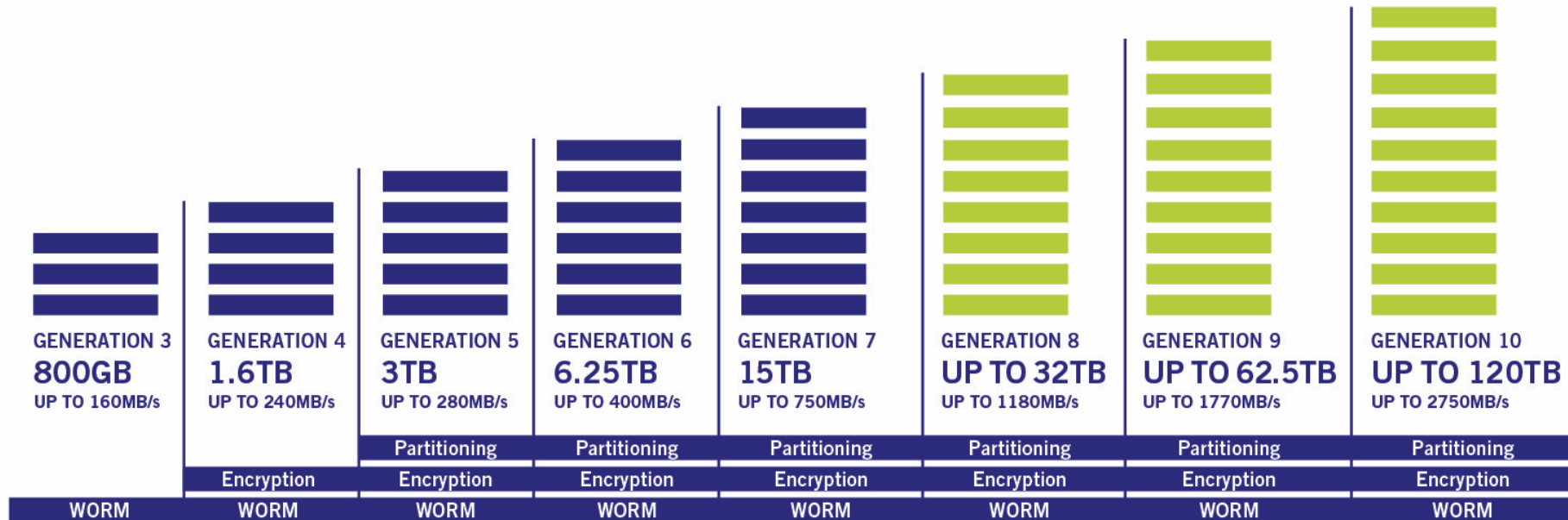
GEM dominating 2.9 GB/s same requirement as PVDIS

SILO capabilities

- Mix of LTO 5 to LTO 8 : 24 drives total
 - Current 5 GB/s
 - 8 drives LTO5
 - 8 drives LTO6
 - 4 LTO7 (300 MB/s)
 - 4 LTO8 (360 MB/s)
 - each LTO8 drive is 360 MB/s about 10 K\$ each
 - Max : $24 * 360 = 8.64$ GB/s
 - to handle 1 GB/s : 4 drives about 40 K\$
 - increase to 4 GB/s (1GB + dup + read) about 120 K\$
 - can upgrade all to LTO8 more : 200 K\$ -> 8.64 GB/s
 - need to write and read at same time
 - LTO8 available in 2017
 - Need to let IT know our real needs might need more drives
 - could do 8.64 GB/s for 200 K\$

LTO timeline

LTO ULTRIUM ROADMAP ADDRESSING YOUR STORAGE NEEDS



Note: Compressed capacities for generations 1-5 assume 2:1 compression. Compressed capacities for generations 6-10 assume 2.5:1 compression (achieved with larger compression history buffer).
Source: The LTO Program. The LTO Ultrium roadmap is subject to change without notice and represents goals and objectives only.
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Currently : 14 drives give 2.24 GB/s (LTO4 to LTO6) up to 16 drives for now. With LTO8 could be up to 0.36 GB/s per drive max 5.78 GB/s for 16 arms
Bottom-line : 3 GB/s is reasonable by 2020

Infrastructure status (from GMn SBS review) (500 MB/s)

Item	Status
LHRS DAQ	1 intel CPU 4 Vxworks CPU
Computer disks	2 raid arrays 2000 MB/s
Network	Gigabit ethernet in Hall (100 MB/s) 10 GigE router 10 Gig adapter on adaq1 and adaq2 (1000 MB/s) 1 fibers 10 Gig Ethernet to Silo (1000 MB/s)
Silo	8 drives LTO5 8 drives LTO6 4 LTO7 (300 MB/s) 4 LTO8 (360 MB/s) -> 5 GB/s

Current infrastructure should satisfy GMn and Gen close from limit for only high rate point

Infrastructure should (1GB/s) (from GMn SBS review)

Item	Status	Cost
LHRS	1 intel CPU 4 intel CPU	15 K\$
Computer disks	2 raid arrays 2GB/s 8 SSD (8x 2GB/s)	20 K\$
Network	1 Gigabit ethernet in Hall 40 GigE router 40 Gig adapter on adaq1 and adaq2 (1000 MB/s) 2 fibers 10 Gig Ethernet to Silo (2000 MB/s)	30 K\$ 5 K\$
Silo	8 drives LTO5 8 drives LTO6 4 LTO7 (300 MB/s) 4 LTO8 (360 MB/s) 4 LTO8 (360 MB/s) -> 6.2 GB/s	40 K\$ (IT)

Moderate upgrade 70 K\$: can easily handle GMn and GEn, can test CODA3,
should be ok for Gep unless bad background surprise

Easy upgrade to 40 gigE, can take full advantage of VTP readout

Infrastructure like (5 GB/s capability) (from GMn SBS review)

Item	Status	Cost
LHRS	1 intel CPU 4 intel CPU	15 K\$
Computer disks	2 raid arrays 2GB/s 8 SSD (8x 2GB/s) 1 PB disk array	20 K\$ 300 K\$
Network	10 Gigabit ethernet in Hall 40 GigE router 40 Gig adapter on adaq1 and adaq2 (5000 MB/s) 2 fibers 40 Gig Ethernet to Silo (8000 MB/s)	30 K\$ 30 K\$ 5 K\$ 20 K\$
Silo	8 drives LTO5 8 drives LTO6 4 LTO7 (300 MB/s) 4 LTO8 (360 MB/s) 14 LTO8 -> 11.2 GB/s	40 K\$ (IT) 140 K\$ (IT)

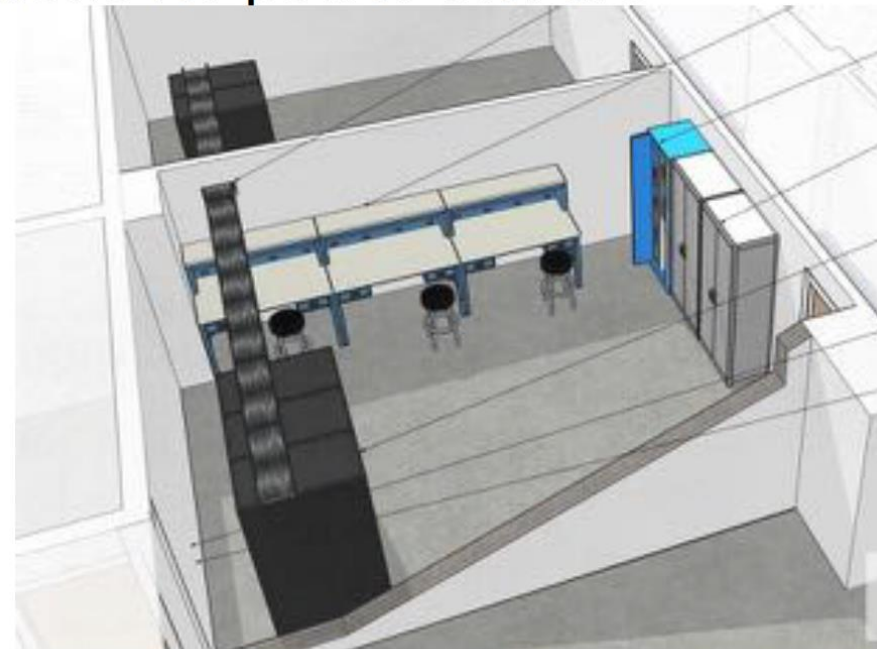
Safe for Gep, TDIS and future program, can use fast VTP readout
 120 K\$ upgrade + 300 K\$ disk + 140 K\$ silo
 (could delay silo and large disk for better cost and upgrade every year)

preRD request

- GEM SAMPA test stand (on going)
- Calorimeter trigger and readout
- Coincidence trigger Cerenkov SPD MRPC
- Deadtime measurements
- Cerenkov MAROC readout
- MRPC readout and test

Facility for Innovation in Nuclear Data Readout and Analysis (INDRA)

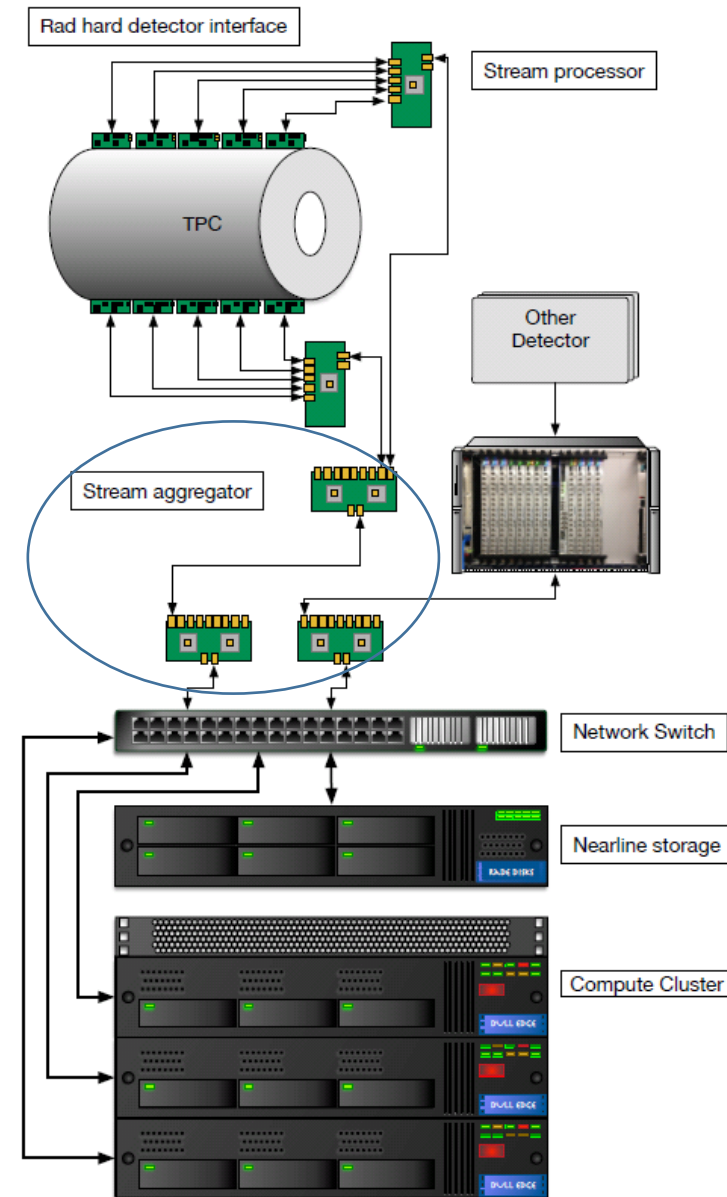
- Having a bunch of interesting projects is all well and good but progress would be speeded by having a dedicated facility for R&D.
 - Semi-permanent test stands without having to borrow hardware.
 - Proximity to existing data acquisition lab.
 - Proximity to JLab datacenter.
- Have acquired space and modifications for power etc. are underway.
- Procurement of hardware will start soon.



Streaming option for GEM

https://eic.jlab.org/wiki/images/6/6b/Graham_Heyes.pdf

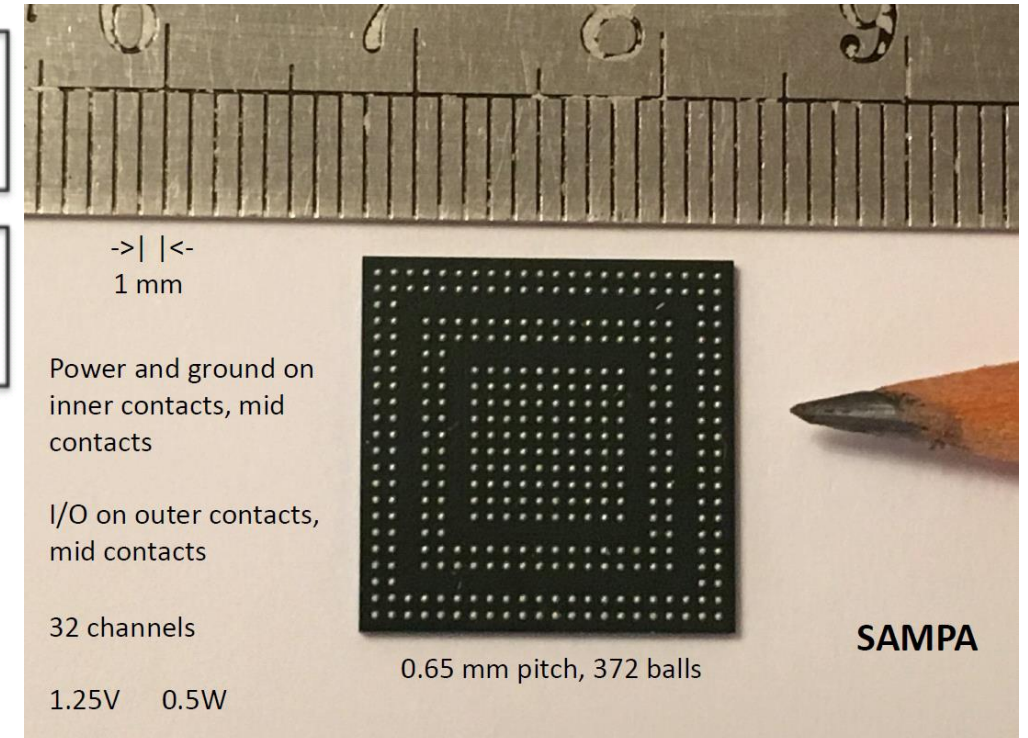
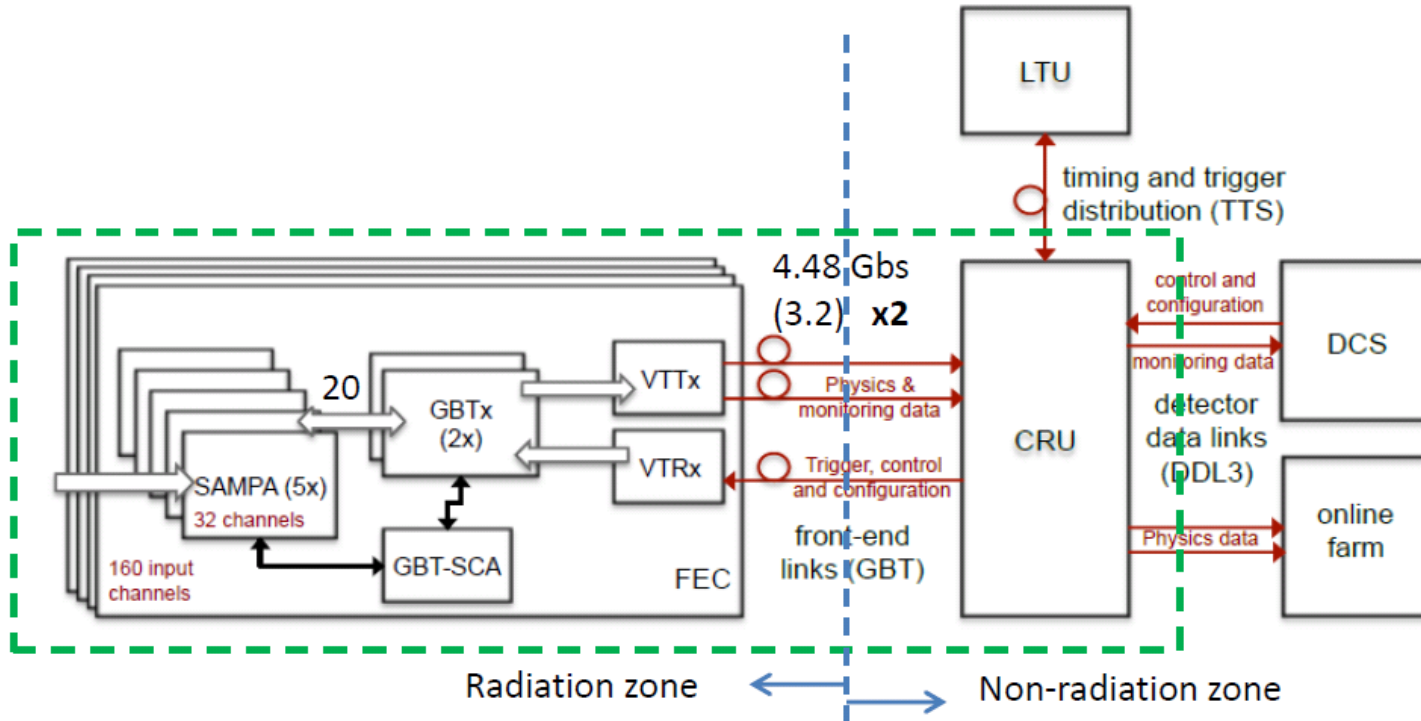
- Rad hard detector interfaces convert detector signals into serial stream.
- Stream processor – “smart” FPGA and maybe CPU equipped electronics processes the raw stream to reduce data rate.
 - See CRU in earlier slide
- Stream aggregator - since there may be many stream processors an optional SA aggregates streams to reduce the number of cables
 - Note : this is NOT event building, this is pushing more than one stream down a single fiber.
 - SA’s can be cascaded in a large system.
 - If the fiber protocol is a network standard like Ethernet we connect directly to a switch.
 - If not then we will provide a PCI card to put in the storage node(s).



GEM APV readout with SSP

- Implementation of noise rejection on SSP for SBS
- Need to evaluate rejection factor for SoLID background

Test stand at JLAB : SAMPA



FEC – Front End Card (160 ch / FEC)

CRU – Common Readout Unit (12 FECs / CRU = 1920 ch / CRU)

DCS – Detector Control System

LTU – Local Trigger Unit

Functional Blocks

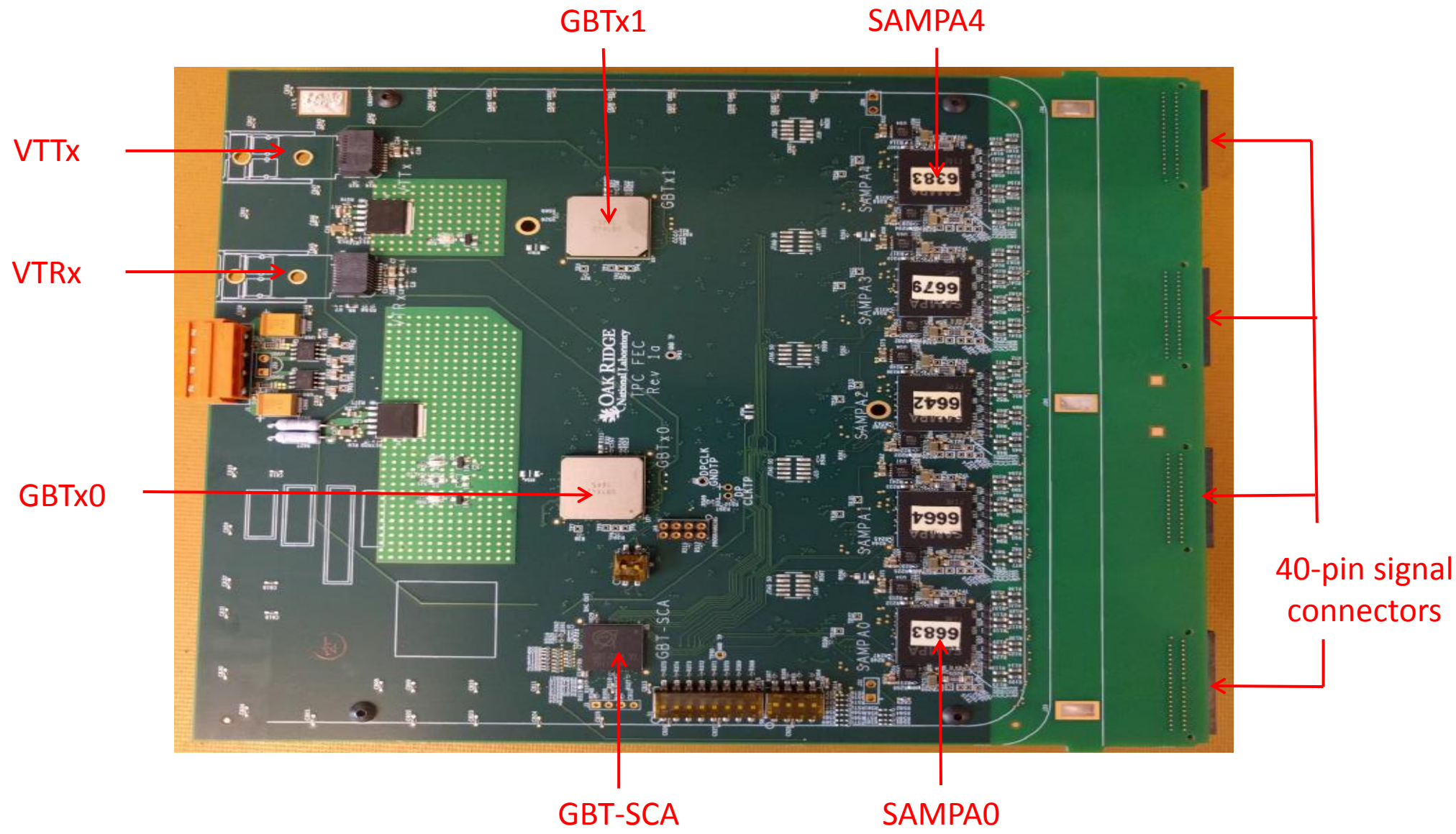
- Charge Sensitive Amplifier (CSA)

- Integrates and amplifies short current pulse
- Output is a Voltage signal with amplitude proportional to the total charge Q
- Tail of Voltage pulse is long ($T = R_f * C_f$)
- Vulnerable to pile-up unless followed by a shaping filter

- Shaper

- Creates a 4th order semi-Gaussian pulse shape
- Available shaping times (TS): 80, 160, 300 ns (SAMPA V3, V4)
- Permits sampling by ADC at reasonable rates (10, 20 MHz)
- 80 ns option eliminated in order to reduce noise in CSA
- SAMPA V5 is now in development with 80, 160 ns shaping times for sPhenix

FEC – JLab version



Plan of Action and Progress

- All components in place October 1
- Power board – measure all voltages O.K.
- Configure GBTx0 using external I2C master (Bus Pirate) O.K.
- Configure SAMPAs through GBT link and GBT-SCA IN PROGRESS
- Read out pedestal data in direct ADC mode (bypass DSP)
- Input pulses into SAMPAs with pulse generator card and read out data
- Configure SAMPAs to use DSP with zero suppression and read out data
- Configure system with multiple front end cards (5) and read out data
- Map front end card connectors to existing prototype GEM detector (800 channels) and read out data in continuous mode
- Slow start learning how to use FELIX card with ALICE front end card

Conclusion

- Budget
 - Baseline reduced calorimeter 1 M\$
 - 1.9 M\$
- SAMPA
 - tracking efficiency similar to APV for 80 ns shaping time
 - occupancies larger than for APV with 160 ns
- Network infrastructure for Hall A required for SBS and TDIS most likely satisfy SoLID
- Test stand in progress for General DAQ R&D
 - can validate SoLID requirements
 - 3 GB/s to tape
 - Data reduction online with hardware