

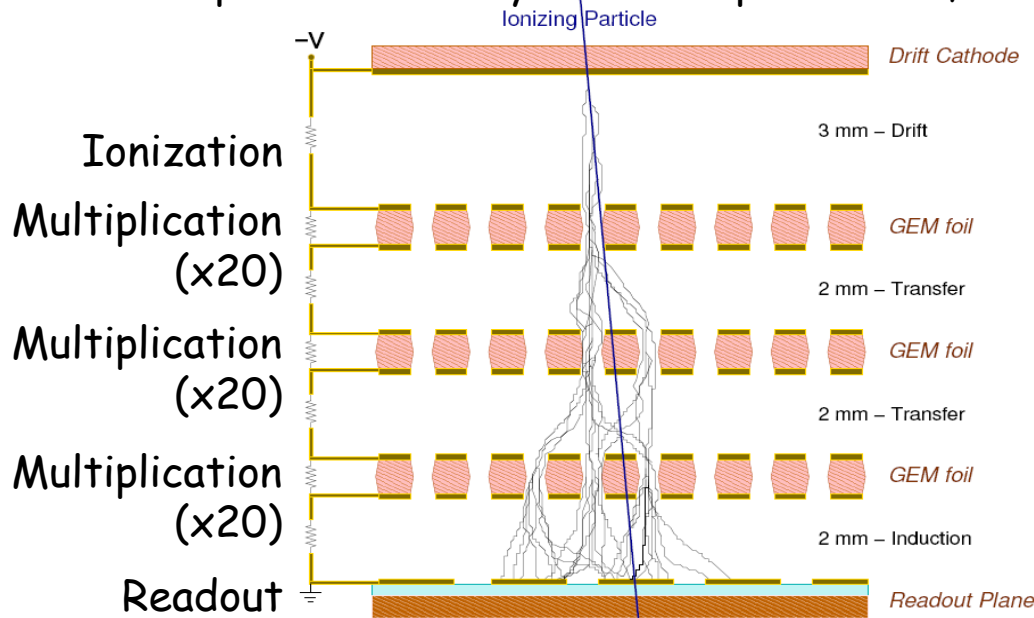
GEM Detectors for SoLID

Nilanga Liyanage and Knodo Gnanvo

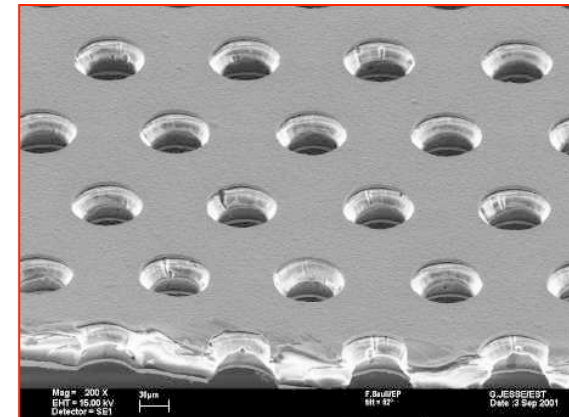
University of Virginia

Why GEMs ?

- SoLID concept leads to high rate in trackers: and requires good resolution.
- Gas Electron Multiplier (GEM) detectors provide a cost effective solution for high resolution tracking under high rates over large areas.
- Rate capabilities higher than many MHz/cm²
- High position resolution ($< 75 \mu\text{m}$)
- Ability to cover very large areas (10s - 100s of m²) at modest cost.
- Low thickness ($\sim 0.5\%$ radiation length)
- Already Used for many experiments around the world: COMPASS, Bonus, KLOE, TOTEM, STAR FGT, ALICE TPC, pRad etc.
- And planned for many future experiments: CMS upgrade, SoLID, Moller, P2 @ Mainz

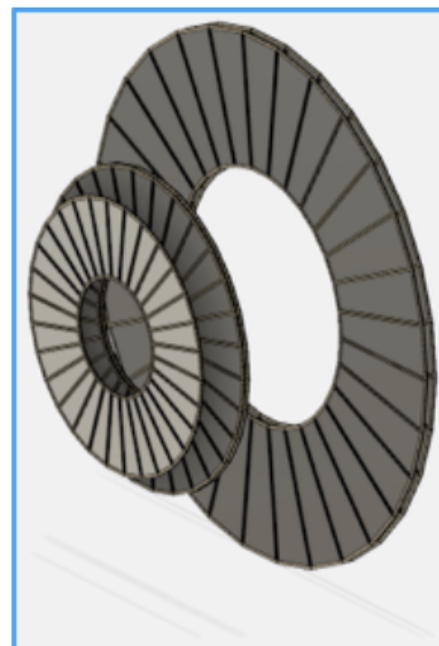
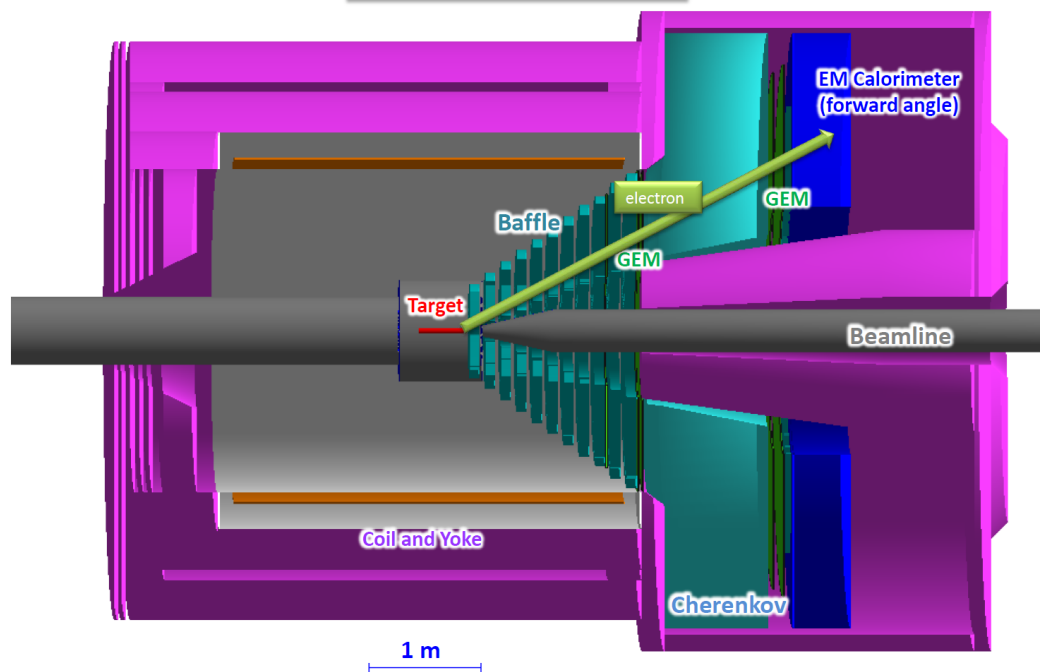


GEM foil: 50 μm Kapton + few μm copper on both sides with 70 μm holes, 140 μm pitch

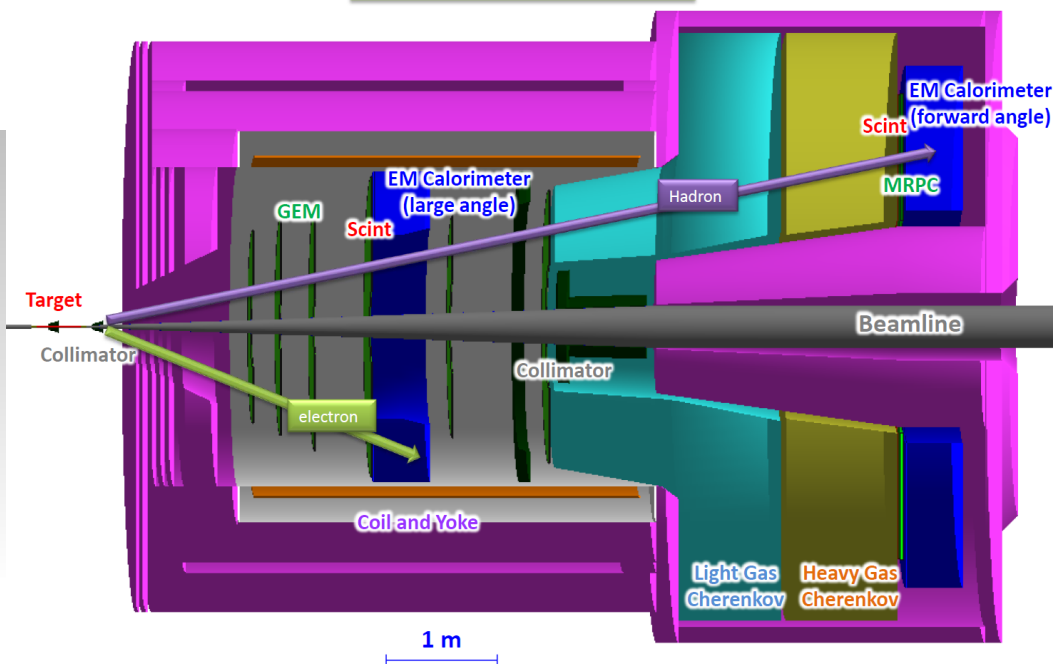
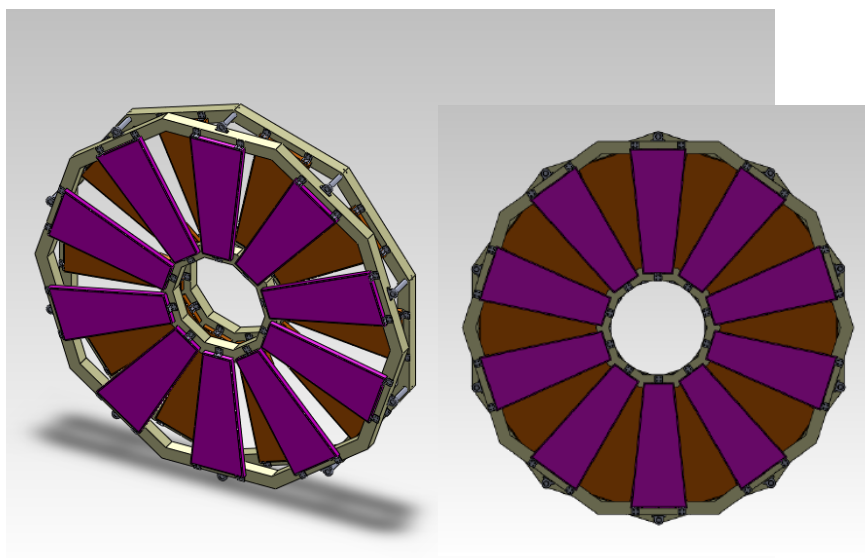


Novel technology: F. Sauli, Nucl. Instrum. Methods A386(1997)531

SoLID (PVDIS)



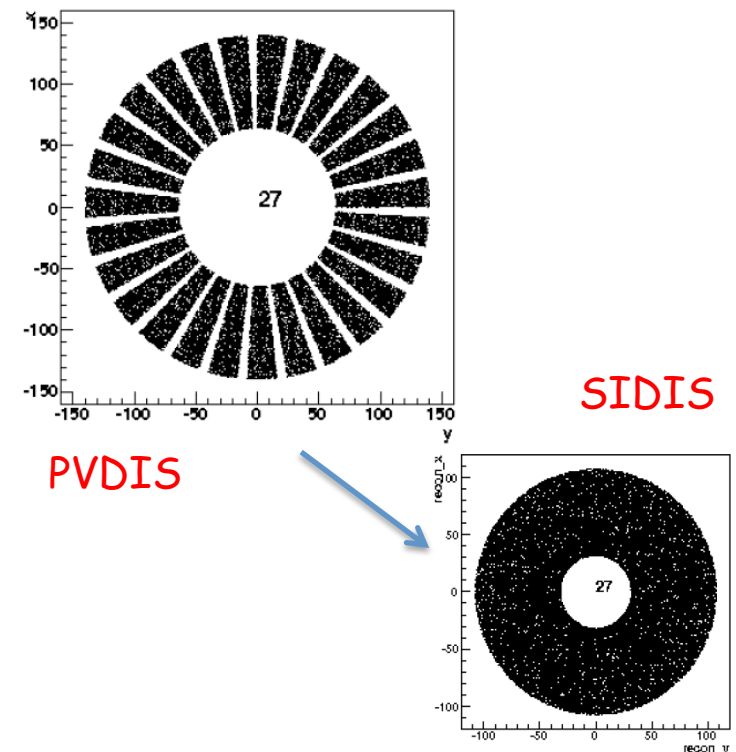
SoLID (SIDIS & J/ψ)



SIDIS GEM full configuration

- Six locations instrumented with GEM:
- PVDIS GEM modules can be re-arranged to make all chamber layers for SIDIS. - move the PVDIS modules closer to the axis so that they are overlapping with each other

Plane	Z (cm)	R_I (cm)	R_O (cm)	Active area (m ²)	# of channels
1	-175	36	87	2.0	24 k
2	-150	21	98	2.9	30 k
3	-119	25	112	3.7	33 k
4	-68	32	135	5.4	28 k
5	5	42	100	2.6	20 k
6	92	55	123	3.8	26 k
total:				~20.4	~ 161 k



- More than enough electronic channels from PVDIS setup.
- The two configurations will work well with no need for new GEM or electronics fabrication.

PVDIS GEM full configuration

- Instrument five locations with GEMs:
- 30 GEM modules at each location: each module with a 12-degree angular width.

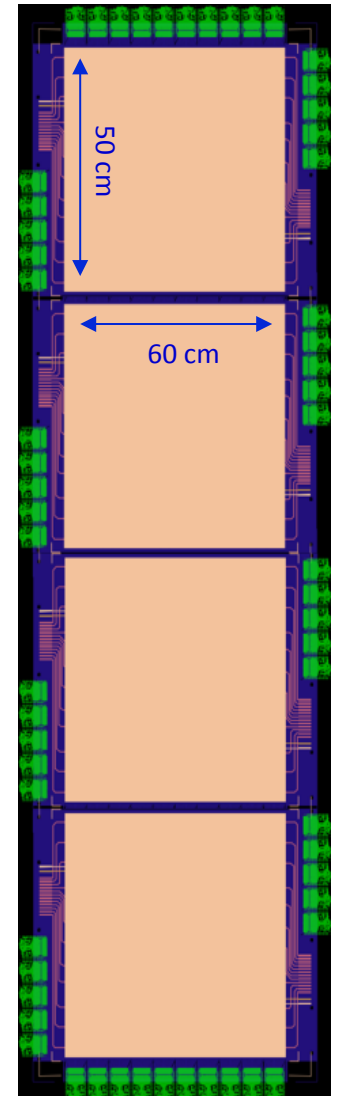
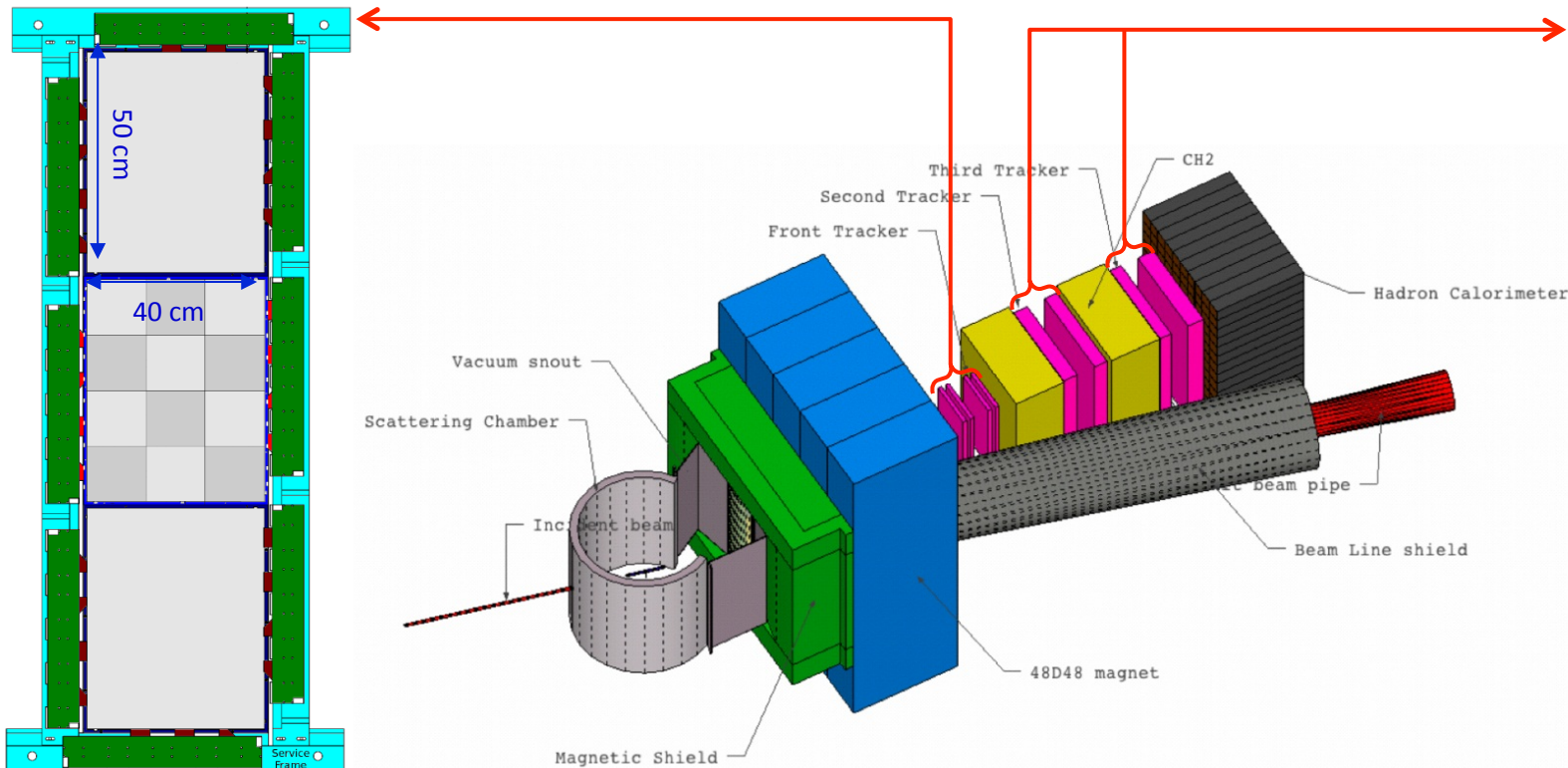
Location	Z (cm)	R_{min} (cm)	R_{max} (cm)	Surface (m ²)	# chan
1	157.5	51	118	3.6	24 k
2	185.5	62	136	4.6	30 k
3	190	65	140	4.8	36 k
4	306	111	221	11.5	35 k
5	315	115	228	12.2	38 k
Total				≈ 36.6	≈ 164 k

- The high occupancy at location 1 will require splitting each readout strip into two channels: this will add another 12 k channels
- Total number of channels needed: ~ 176 k
- With $\sim 15\%$ spares (to account for losses during production etc.) need to plan for 200 k channels

GEM plans for SoLID based on recent work for SBS

- **Front Tracker:**
- 6 GEM Layers ($150 \times 40 \text{ cm}^2$)
- Each layer = 3 GEM modules ($50 \times 40 \text{ cm}^2$)
- R&D and Production by INFN Roma, Catania

- **Back Tracker**
- 11 GEM Layers ($200 \times 60 \text{ cm}^2$)
- Each Layer = 4 GEM modules ($50 \times 60 \text{ cm}^2$)
- R&D and Production @ University of Virginia



Proton arm layout for GEp (5) experiment

Total Area $\sim 16 \text{ m}^2$

SBS GEM Production at UvA is complete:

- Completed building 49 modules (plan was to build 48) and tested.
- 46 tested modules and all work per specs.
- GEM foils and readouts from CERN: GEM frames from Resarm in Belgium
- All assembly done in clean-room at UvA.
- Foils from CERN very high quality; over 90% yield; mostly on-time delivery.
- Foil QA at every step extremely important.
- Production design and prototyping process takes at least about 1 year.
- The GEM foil ordering process has a long lead time, need at least ~ 1 year to get started.
- In production mode: ~ 2 modules per month.
- Could be increased to two parallel assembly lines, yielding ~ 4 modules/month.

Experience for SoLID geometry and size GEMs gained from two EIC GEM prototypes



All readout connections to the outer edge of the circle:

Large & Low-mass Forward Tracker GEM for EIC R&D

Common GEM foil design:

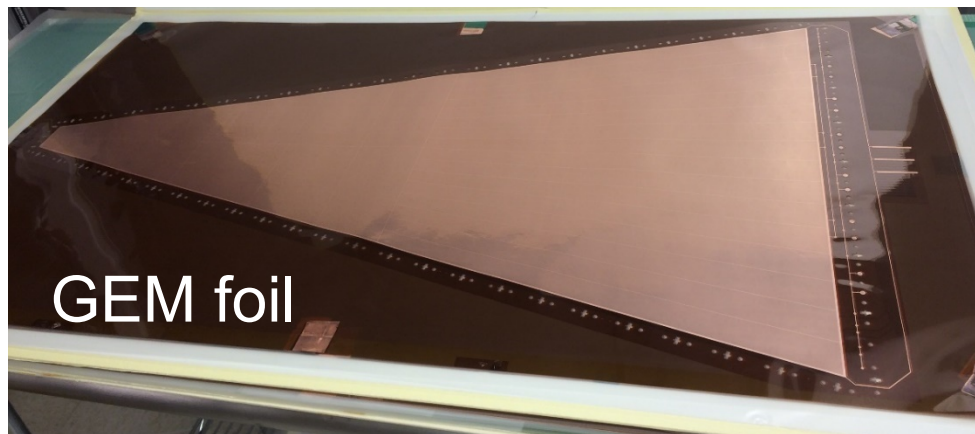
- (Univ. of Virginia, Florida Tech, and Temple U.)
- All connections (HV, gas flow structure and FE cards) are made on outer radius end.

2D U-V strips readout (R/O)

- Spatial resolution improvement
- All readout electronics on outer radius end.
- No connectors or metallized vias on R/O

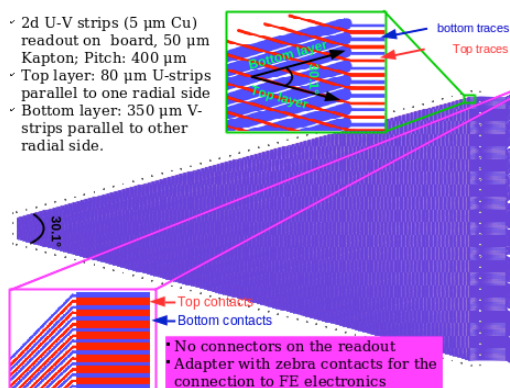
Double-sided zebra connection

- Large density of electronics channels read out on side of the detector (outer radius)
- No electronics on side or inner radius, no multiple scattering or radiation damage issues
- No connectors or metallized vias on R/O

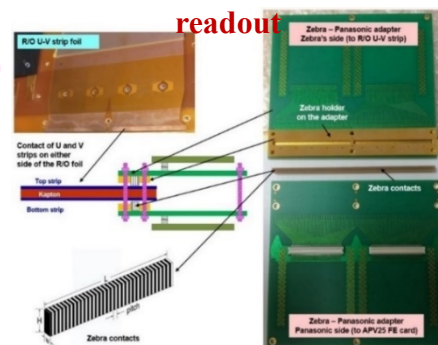


Design of EIC-Proto II 2D U-V strips readout board

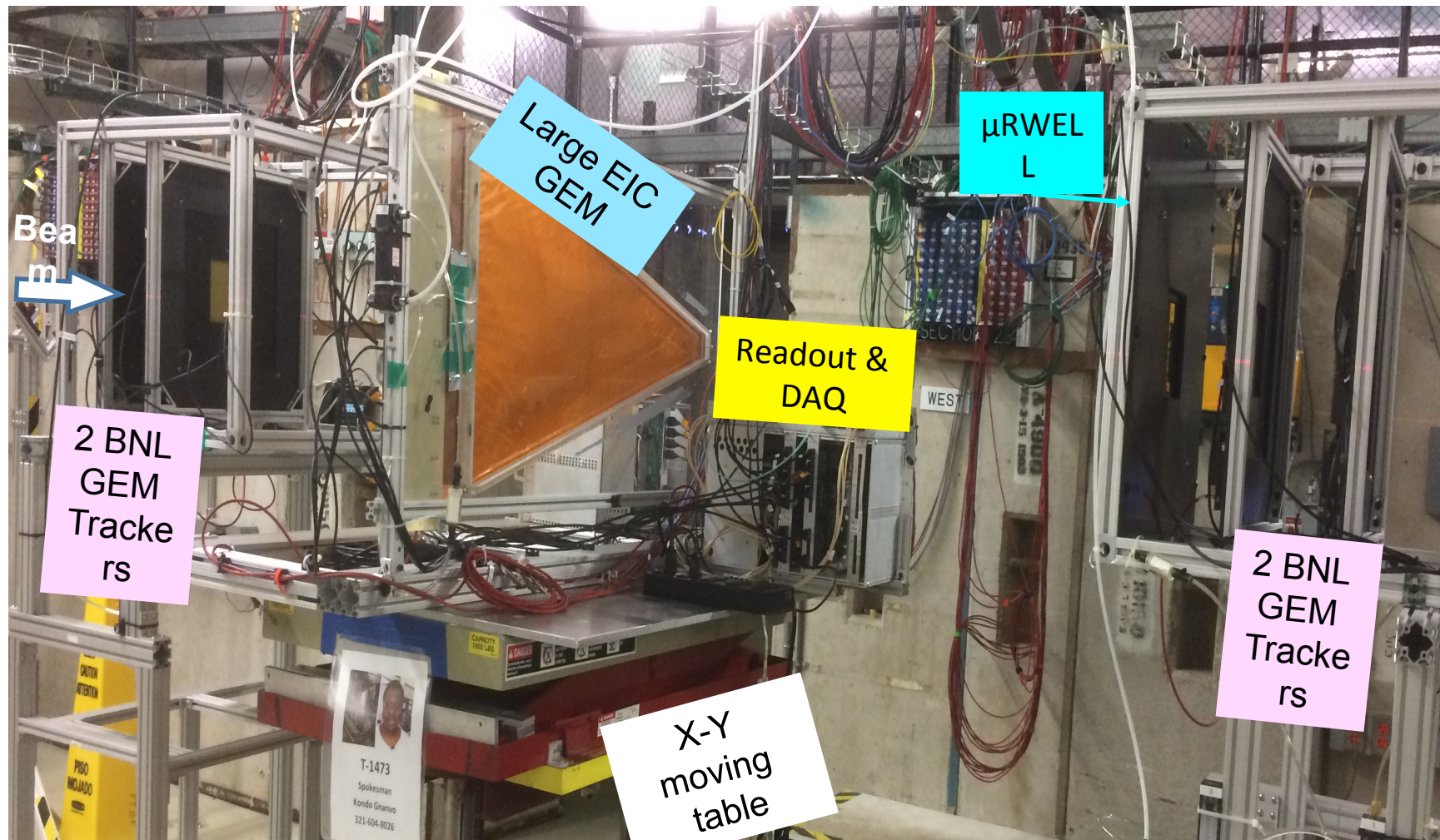
- ✓ 2d U-V strips (5 μm Cu) readout on board, 50 μm Kapton; Pitch: 400 μm
- ✓ Top layer: 80 μm U-strips parallel to one radial side
- ✓ Bottom layer: 350 μm V-strips parallel to other radial side.

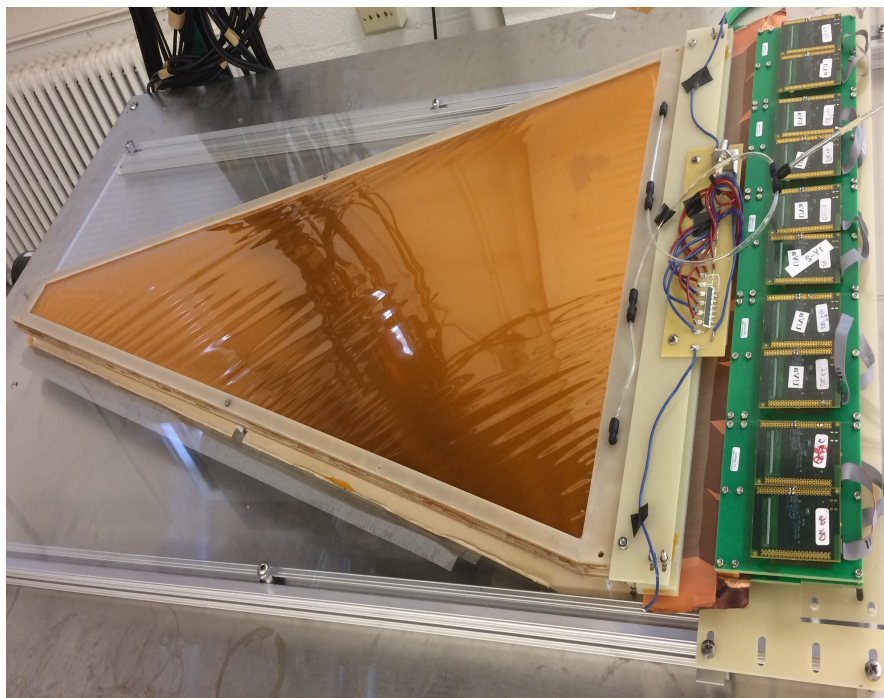


Principle of double-sided zebra connection on flexible PCB readout

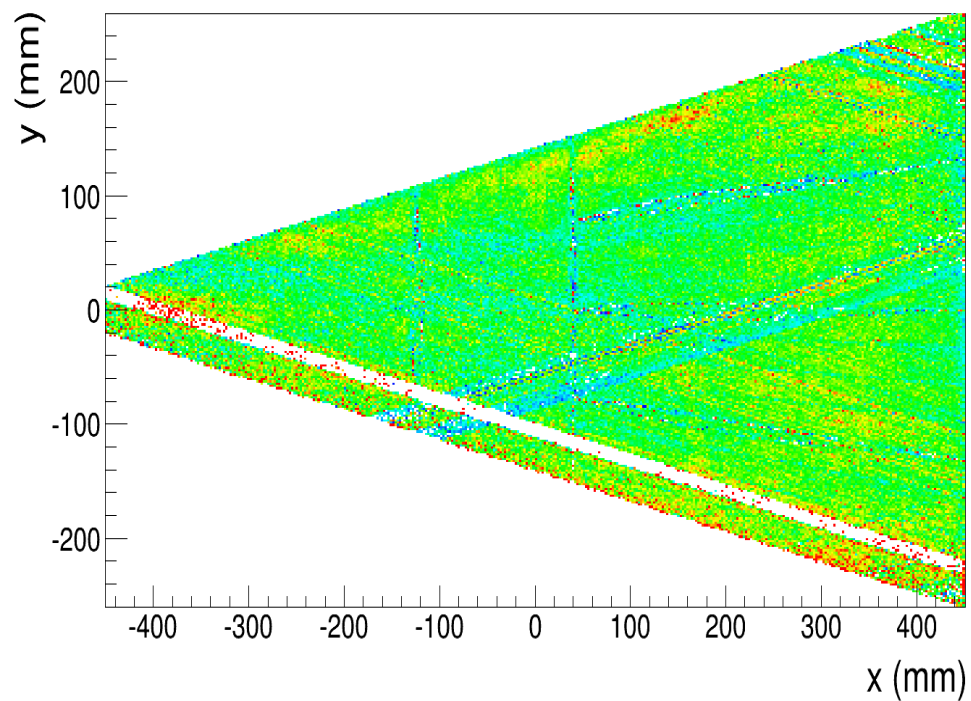


Large GEM Setup in MT6.2b Area at the FTBF (June-July 2018)

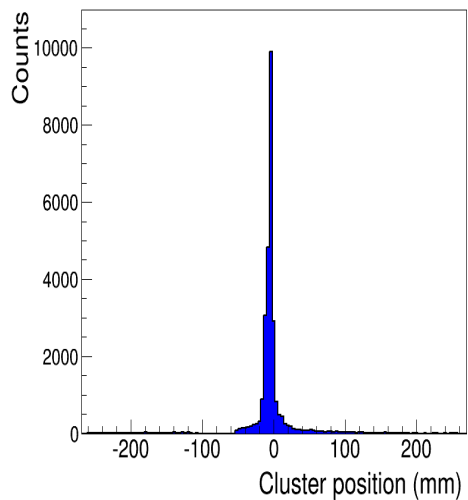




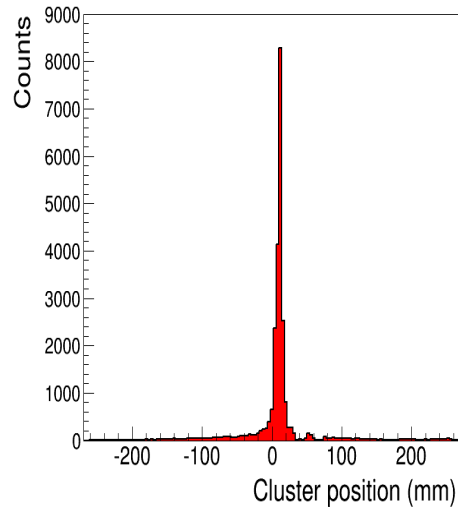
EIC-FT-GEM : Gain uniformity with Cosmics - Average ADC counts



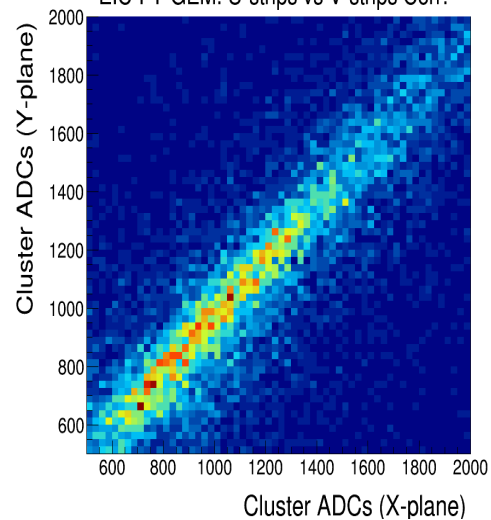
EIC-FT-GEM (U-Strips): 120 GeV Proton



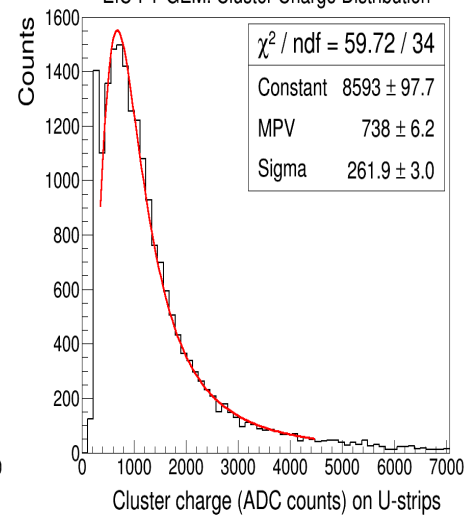
EIC-FT-GEM (V-Strips): 120 GeV Proton



EIC-FT-GEM: U-strips vs V-strips Corr.



EIC-FT-GEM: Cluster Charge Distribution



Plan for electronics

- Need 200 k chan.
- The plan has been to use APV-25 electronics.
 - Used for SBS
 - Already developed.
 - Lot of expertise at Jlab
 - Cheap
 - Unfortunately APV-25 chip is now extinct.
- Reuse APV-25 electronics from SBS :
 - SBS has a total of ~ 160 k of APV-25 (120 k chans. owned by Jlab (from UVA) ~ 40 k owned by INFN).
 - Assuming that at least ~ 66% survival rate after SBS run, we will have ~ 105 k of APV electronics for SoLID
- Need another ~ 100 k channels: need to find a suitable readout chip for these
- SAMPA chip is not rad-hard: will not work for SoLID
- VMM is a good choice: but need to develop direct mode readout.
 - Assume \$ 75 k for pre-R&D work
 - Assume \$ 200 engineering design and development of readout system
 - \$ 4/chan for fabrication costs.

Alternate Chip Options

- VMM3: Developed by BNL for ATLAS
 - Good
 - digital output with on board zero suppression
 - High rates
 - suitable for large detectors,
 - Bad
 - single sample; does not allow pileup correction or time based background rejection
- The direct readout mode (with fast ~ 200 ns reset time) may work well for SoLID.
- Only 6-bit ADC in this mode.
- Need to understand and evaluate the VMM chip for SoLID with pre-R&D work
- Important to get a collaborator to take over the project.

Alternate Chip Options: VMM

APV_(ANALOGUE)

APV (250 nm CMOS)

- Pipeline depth: max. 192 clocks
- Trigger latency: max. 3 μ s
- Noise: < 500 e⁻ intrinsic >750..1400 e⁻ on detector
- dynamic range: 25 fC
- Detector capacity: 18... < 60pf
- ADC ext. 4096/1000 [counts/baseline]
- Gain: fixed CSA gain 100uA/mip, 5 output signal gains (in step of 20%)
- Timing jitter : $\frac{1}{2}$ (1/fc) [+ - 12ns]
- Shaping times: 50 ns adjustable to 80 ns
- max readout rate: 7 kHz

VMM_(DIGITAL)

VMM (130nm CMOS)

- Pipeline depth: 64 digital frames (peak)
- Trigger latency: (self triggered) or L0 (12.8us)
- noise : < 400 e⁻ on 10x10 detector reported
- dynamic range: expect >> 25 fC
- Detector capacity: 30pF < 1nF
- ADC: embedded, 10 bit
- Gains: 8 CSA gains [0.5..16mV/fC]
- Timing jitter: 20 bit t-stamp, 1ns resolution
- Shaping times: 4 [25... 200ns]
- max readout rates: estimated 4 MHz/ch

Budget Estimates

Activity Name	Costed Labor (PW)	Contrib Labor (PW)	Total Labor (PW)	Labor Cost (\$K)	Procurement Cost (\$K)	Total Cost (\$K)
GEM	632.00	40.00	672.00	\$1,605.28	\$2,194.00	\$3,799.28
GEM Modules	484.00	0.00	484.00	\$1,229.36	\$1,464.00	\$2,693.36
GEM foils			0.00	\$0.00	\$620.00	\$620.00
GEM readout planes			0.00	\$0.00	\$464.00	\$464.00
GEM cathode foils			0.00	\$0.00	\$100.00	\$100.00
GEM module frames			0.00	\$0.00	\$230.00	\$230.00
GEM module supplies			0.00	\$0.00	\$40.00	\$40.00
GEM module tooling			0.00	\$0.00	\$10.00	\$10.00
GEM module assembly	484.00		484.00	\$1,229.36		\$1,229.36

- Main items: materials for 150 GEM modules.
 - 450 GEM foils from CERN shop.
 - 150 2-D readout boards from CERN shop
 - 150 GEM frame sets from Resarm
 - Technician manpower for GEM assembly: ~ 12 FTYE.
- All estimates based on recent lab experience from SBS GEM module production.

Budget Estimates

Activity Name	Costed Labor (PW)	Contrib Labor (PW)	Total Labor (PW)	Labor Cost (\$K)	Procurement Cost (\$K)	Total Cost (\$K)
GEM Readout	0.00	0.00	0.00	\$0.00	\$430.00	\$430.00
VMM electronics channels		✓	0.00 ✓	\$0.00	\$400.00	\$400.00
VMM electronics cables		✓	0.00 ✓	\$0.00	\$30.00	\$30.00
GEM high voltage	0.00	0.00	0.00	\$0.00	\$80.00	\$80.00
HV power supplies		✓	0.00 ✓	\$0.00	\$70.00	\$70.00
HV power cabling		✓	0.00 ✓	\$0.00	\$10.00	\$10.00
GEM gas system	0.00	0.00	0.00	\$0.00	\$30.00	\$30.00
GEM Gas plumbing		✓	0.00 ✓	\$0.00	\$30.00	\$30.00
GEM mechanical support	16.00	0.00	16.00	\$40.64	\$90.00	\$130.64
GEM mechanical support wheels	16.00	✓	16.00	\$40.64	\$90.00	\$130.64
Transport and travel		✓	0.00 ✓	\$0.00	\$100.00	\$100.00
Installation and Testing	132.00	✓	132.00	\$335.28	✓	\$335.28
Management		40.00 ✓	40.00 ✓	\$0.00	✓	\$0.00

- All estimates based on recent lab experience from SBS GEM module production.

Risks and Mitigation strategies

- On time availability of GEM foils.
 - Since this is a very large order of GEM foils, and since CERN has been the only supplier of GEM foils of this size, there is the risk of delays in GEM foil availability.
- Mitigation strategies:
 - Please the orders for the whole need well in advance (at least 1 year or more) to allow CERN shop to plan the delivery.
 - Now there are several companies around the world working with CERN on large GEM foils: need to engage them early and evaluate their foils.
- All Working with these companies, CERN shop is now completing a very large foil order for CMS upgrade project. This shows that advanced planning and early coordination with CERN, risks could be minimized.

Risks and Mitigation strategies

- The fabrication timeline may be too ambitious for one group to complete on time.
 - Based on SBS experience, it seems that the UVa group could build up to about 40-50 modules/year, but a more conservative and safe goal would be about 35-40 per year. This will require longer than anticipated in the plan.
- Mitigation strategies:
 - Work with partner institutions with GEM experience to distribute the production to more locations. Work with these institutions from prototyping stage to build readiness.
 - Work with groups at Temple U and Hampton U.

Risks and Mitigation strategies

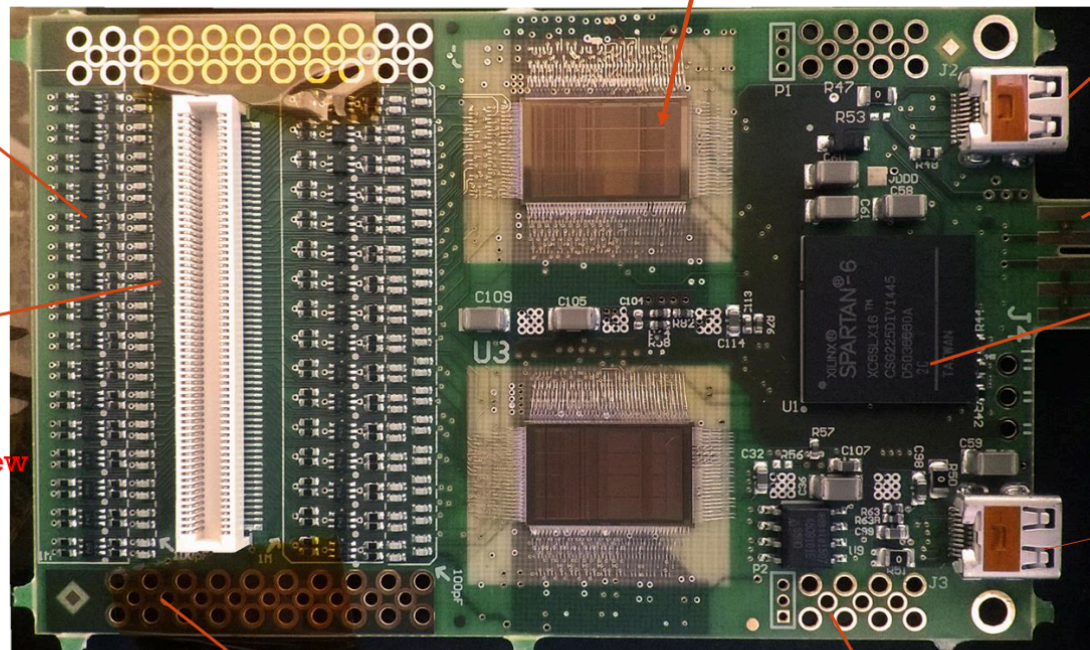
- Suitability of VMM electronics for high rate operation needed for SoLID ?
 - The standard operating mode of VMM looks too slow for SoLID conditions
- Mitigation strategies:
 - The direct readout mode of VMM appears to work as needed. Evaluate and characterize the chip in this mode as part of pre R&D. If SoLID rate needs are not met, look for alternate solutions.

Alternate Chip Options: VMM: SRS version

Photo: 2 x wire-bonded VMM2 chips -> new VMM3 board fully routed

AC coupling
&
spark protection

Panasonic 130 pin
connector for MPGDs
Will be replaced by new
140 pin HRS connector



HDMI link 1 DTCCP

JTAG

Companion FPGA

HDMI link 2 DTCCP

Detector GND MMCx

Neighbor-channel via MMCX