SoLID DAQ

SoLID collaboration meeting

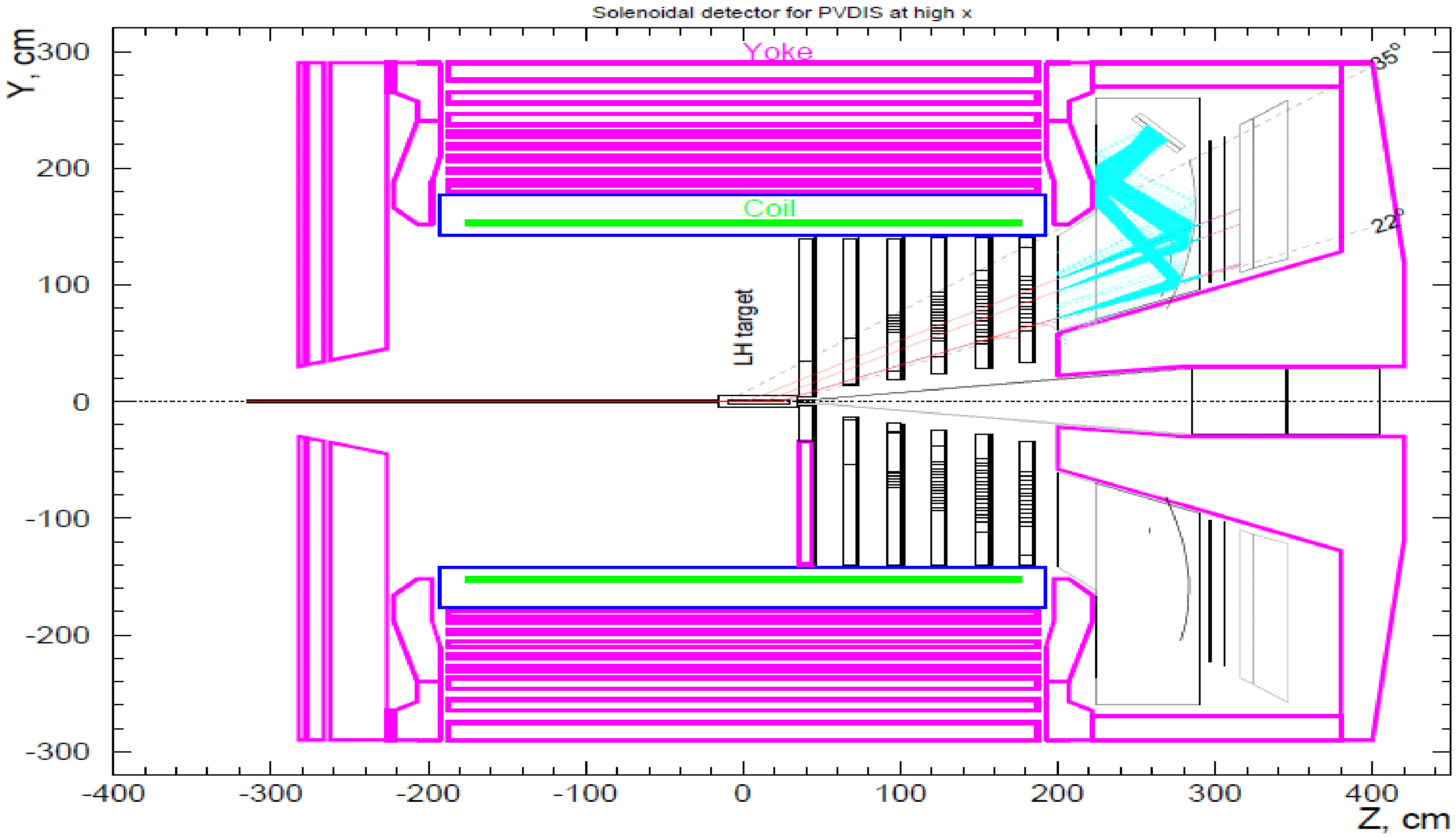
June 8th 2020

Alexandre Camsonne

Outline

- DAQ overview
- DAQ requirements
- Data rates
- R&D items
  - VMM
  - APV
  - FADC
  - Cerenkov
  - TOF
- Conclusion

Detector layout and trigger for PVDIS



Trigger

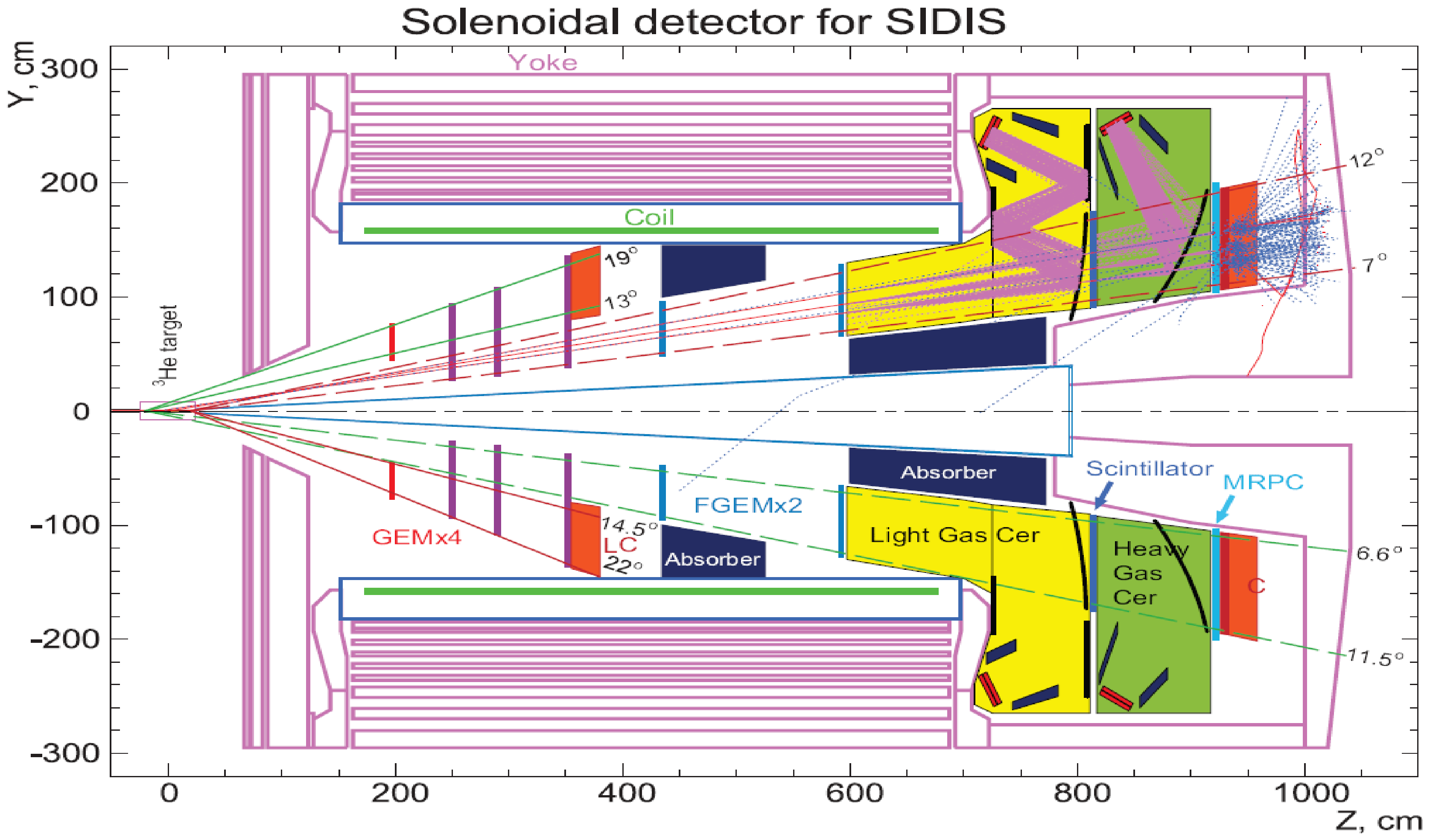
Calorimeter
+
Cerenkov

200 to 500 KHz of electrons

30 individual sectors

Max 17 KHz/sector

Detector layout and trigger for SIDIS



Trigger

Calorimeter
+
Cerenkov
+
MRPC

30 sectors
Combined
in
10 regions of interests
Max rate 200 KHz

Baseline 60 KHz
coincidence e- pion

SoLID requirements

Experiments	PVDIS	SIDIS-^{3}He	SIDIS-Proton	J/ψ
Reaction channel	$p(\vec{e},e')X$	$(e,e'\pi^{\pm})$	$(e,e'\pi^{\pm})$	$e+p\rightarrow e'+J/\Psi(e^-,e^+)+p$
Approved number of days	169	125	120	60
Target	LH_2/LD_2	^{3}He	NH_3	LH_2
Unpolarized luminosity ($cm^{-2}s^{-1}$)	$0.5\times10^{39}/1.3\times10^{39}$	$\sim 10^{37}$	$\sim 10^{36}$	$\sim 10^{37}$
Momentum coverage (GeV/c)	2.3-5.0	0.8-7.0	0.8-7.0	0.6-7.0
Momentum resolution	~2%	~2%	~2%	~2%
Polar angle coverage (degrees)	22-35	8-24	8-24	8-24
Polar angle resolution	1 mr	0.6 mr	0.6 mr	0.6 mr
Azimuthal angle resolution	-	5 mr	5 mr	5 mr
Trigger type	Single e^-	Coincidence $e^- + \pi^{\pm}$	Coincidence $e^- + \pi^{\pm}$	Triple coincidence $e^-e^-e^+$
Expected DAQ rates	<20 kHz $\times$ 30	<100 kHz	<100 kHz	<30 kHz
Backgrounds	Negative pions, photons	$(e,\pi^-\pi^{\pm})$ $(e,e'K^{\pm})$	$(e,\pi^-\pi^{\pm})$ $(e,e'K^{\pm})$	BH process Random coincidence
Major requirements	Radiation hardness 0.4% Polarimetry π^- contamination Q^2 calibration	Radiation hardness Detector resolution Kaon contamination DAQ	Shielding of *sheet-of-flame* Target spin flip Kaon contamination	Radiation hardness Detector resolution

Event size data rates PVDIS

				Event size		Data rate MBs	After noise cut	strips firing	event size bytes		MB/s
1	1156	21.17	244.73	3038.03	3038.03	60.76	9.97	115.25	1430.76	1430.76	28.62
2	1374	10.35	142.21	1765.39	1765.39	35.31	5.11	70.21	871.61	871.61	17.43
3	1374	8.81	121.05	1502.71	1502.71	30.05	4.42	60.73	753.92	753.92	15.08
4	2287	3.07	70.21	871.60	871.60	17.43	1.64	37.51	465.61	465.61	9.31
5	2350	2.79	65.57	813.93	813.93	16.28	1.50	35.25	437.60	437.60	8.75
					Total	159.83				Total	79.19
FADC											
	20000						10				
	Event size FADC	Nb channel	Header			Trailer	Sample				
	Calorimeter	14	4			4	12	280			
	Preshower	9	4			4	12	180	400		
	Cerenkov	9	4			4	12	180			
									11600000		
								740	11600000	11.6	
									Total rate	94	MB/s

About 2.9 GB/s for PVDIS at 20 KHz

SIDIS event size

Occupancies with one sample readout by Weizhi , rates for 100 KHz

GEM	Occupancy	Number of strips	XY strips	Strips per chambers	MB/s
1	2.21	453	906	27180	245
2	8.78	510	1020	30600	1184
3	3.63	583	1166	34980	559.5
4	2.31	702	1404	42120	428.7
5	1.78	520	1040	31200	244.71
6	1.3	640	1280	38400	220
Total	20.01	3408	6816	204480	2901

GEM dominating 2.9 GB/s same requirement as PVDIS

Address Recommendations from Director's Review

- Slow control responsible designated and costs included in budget
- Recommendation 1.1b.

Ability to handle the desired luminosities and backgrounds including impacts on both the apparatus and the beam line downstream of the target : The dead-time(s) in the DAQ chain should be modeled

FADC deadtime was studied current firmware implementation and deadtime of the system was measured to be 0.3% at 20 KHz which is within the requirement of PVDIS at 12 KHz.

- The plans for the High-Level Trigger and the needs for slow control need to be worked out in detail and the implications for resources need to be evaluated.
- The implications of the need for these resources in the context of availability of resources at the laboratory need to be understood.

Tape silo will be able to record 3 GB/s without high level trigger.
After discussion IT could consider farm processing if hardware cost cheaper than tape cost

Risks associated with DAQ

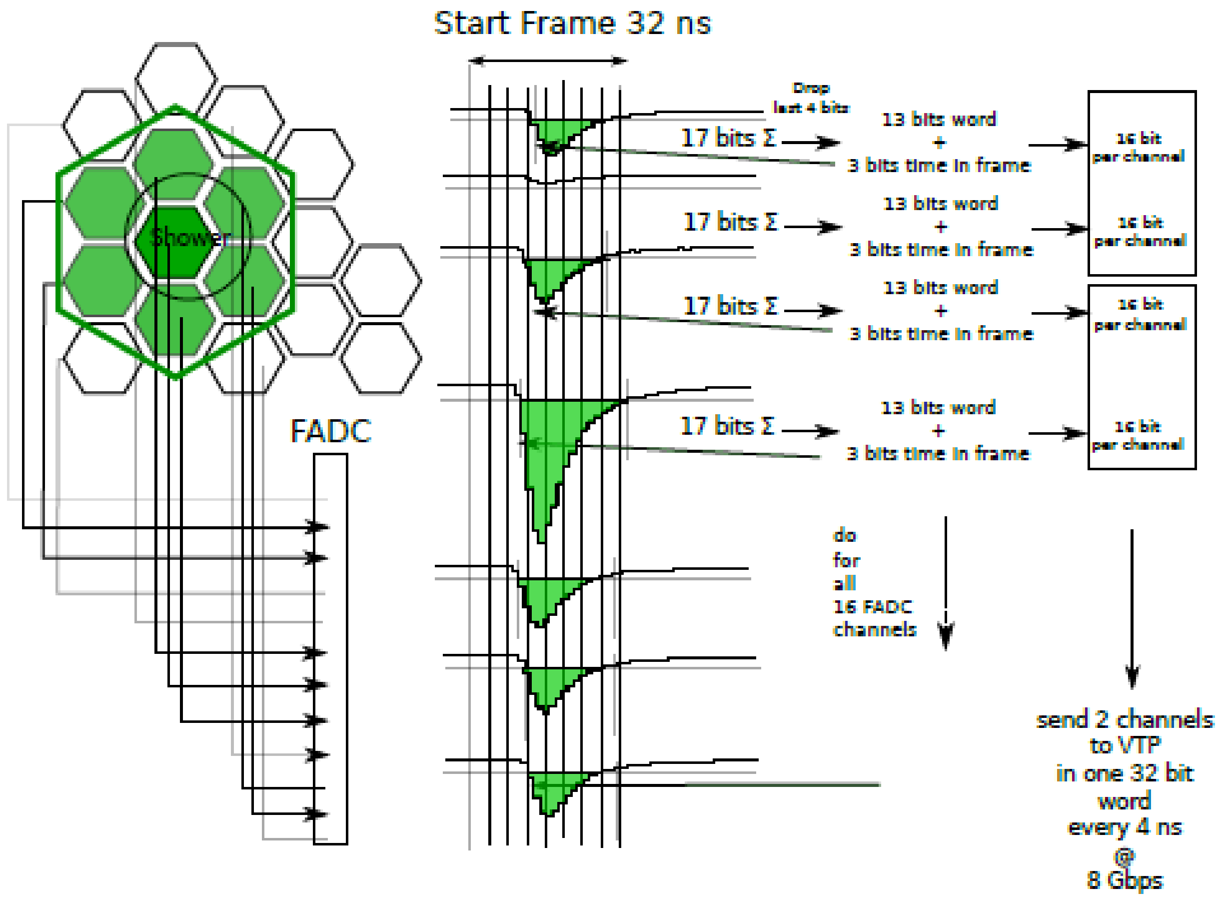
	Risk	Level	WBS	Mitigation
GEM readout	100 KHz capability Achieved resolution	High	1.2.4.2,1.1.5.3	Simulation, test
Data rates	Bandwidth sufficient, electronics can handle	Medium	1.1.5.1.4	Test (preRD and R&D)
Trigger rate	Can required trigger rate reached for SIDIS	Medium	1.1.5.1.7,1.1.5.1.8	Test (preRD and R&D)
Deadtime PVDIS	Can deadtime be an issue for PVDIS ?	High	1.2.4.2,1.1.5.3 1.1.5.1.7,1.1.5.1.8	Drives chip choice and electronics design
Data reduction	Can data be reduced to a reasonable size for silo ?	Medium		Simulation,test,beam test
Cost	Can performance required be reached within budget	Medium		Test
Particle ID	Background rejection sufficient	High		Simulation, beam test

SoLID DAQ overview

- DAQ based on 12 GeV FADC base pipelined electronics designed for 200 KHz trigger rates

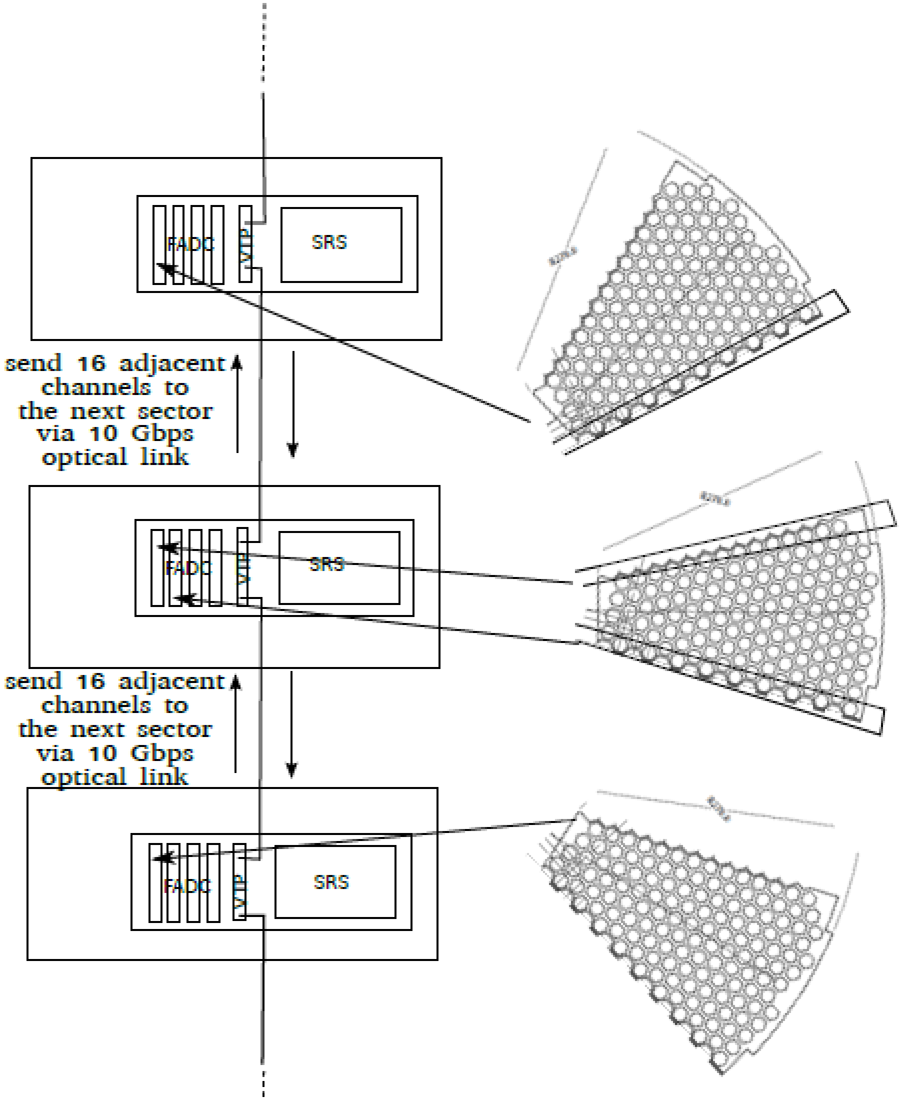
- Added GEM readout similar to SBS but with trigger rates up to 100 KHz

ECAL FADC trigger



- HPS scheme
- Will be used for SBS, NPS before SoLID

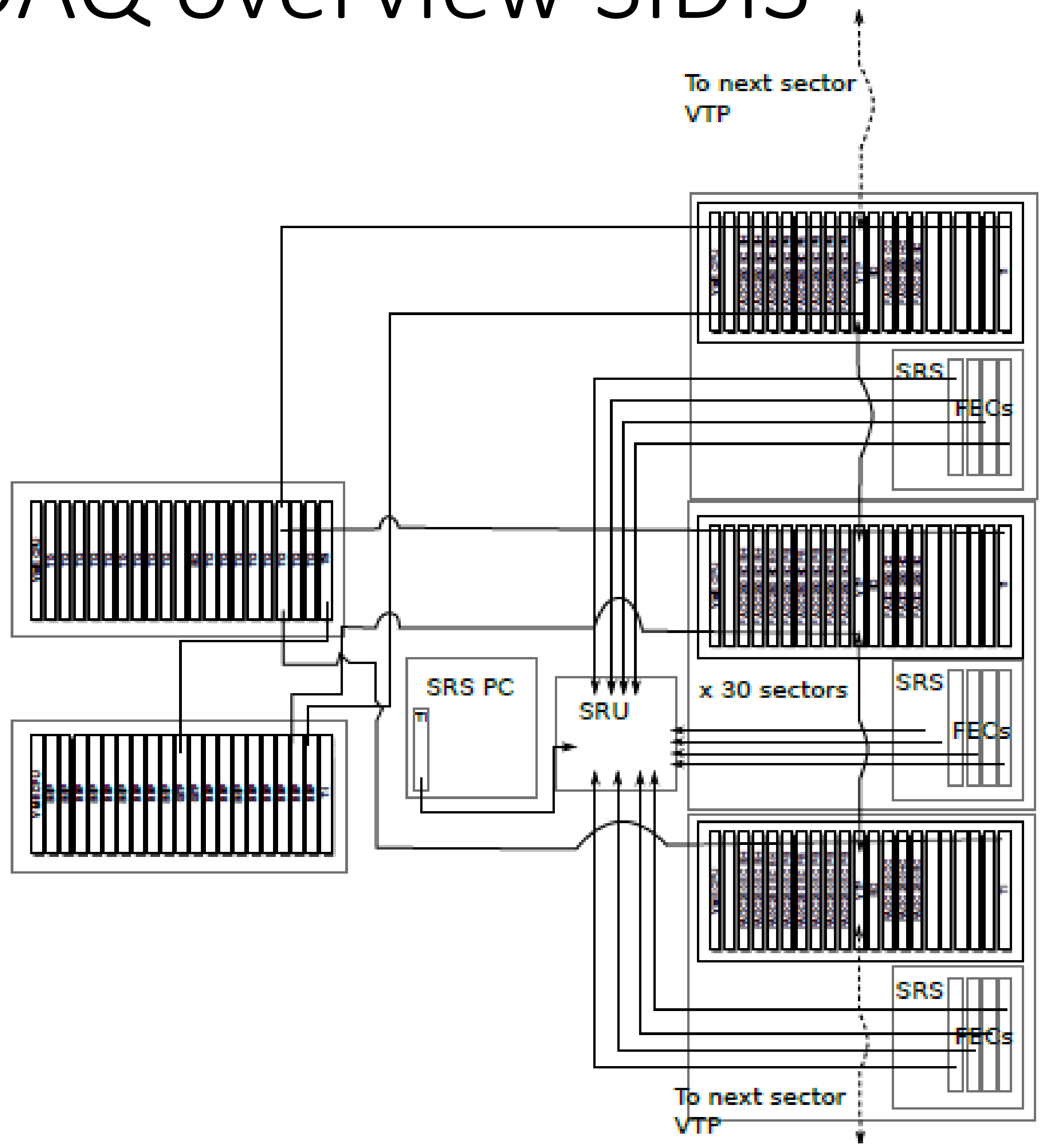
DAQ overview PVDIS



- 30 sectors
- Mostly independent
- Trigger : coincidence Ecal and Cerenkov
- Transfer data from adjacent blocks for clustering

- Scaling of SBS HCAL trigger from 2 to 30 crates

DAQ overview SIDIS



- Similar to Hall D
- Reconfiguration of PVDIS crates to gather data of each trigger to a main VTP to produce the electron pion coincidence
- 100 KHz trigger rate capability

PVDIS electron trigger

- Coincidence ECAL and Gas Cerenkov

	Old	Hall D
Singles ECAL	290 KHz	230 KHz
Singles rates Cerenkov	1.9 MHz	803 KHz
Accidental 30 ns	16.5 KHz	4.1 KHz
DIS electron	10 KHz max	7.7 KHz
Total rate	**27 KHz**	**12.1 KHz**

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GEM readout

- Baseline APV25
  - 164 K channels required
  - Assume reuse 100 K$ channels from SBS
  - Simulation shown
- Evaluation of VMM3 chip
  - Available
  - Radiation hardness should be sufficient
  - No default multisamples
  - Studying fast 6 bit ADC mode for high rate strips

SIDIS event size

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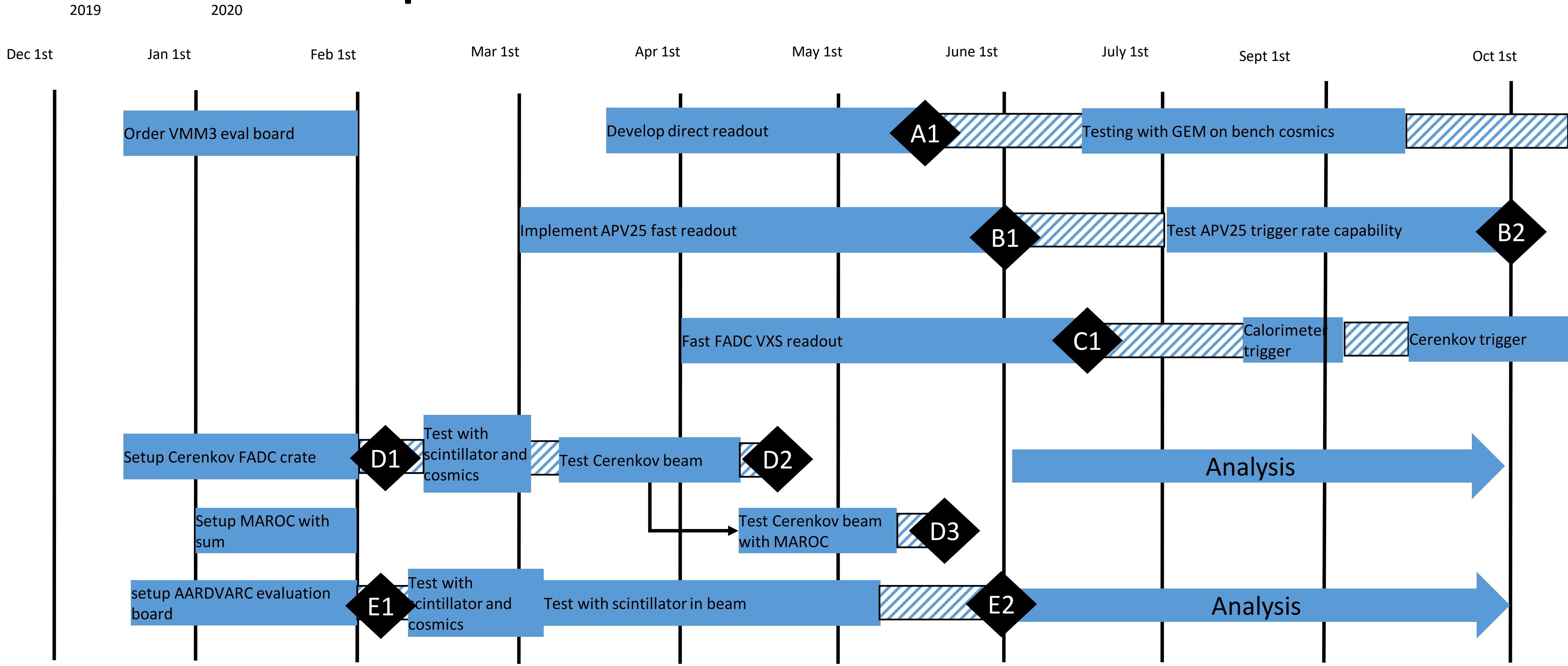
GEM dominating 2.9 GB/s same requirement as PVDIS

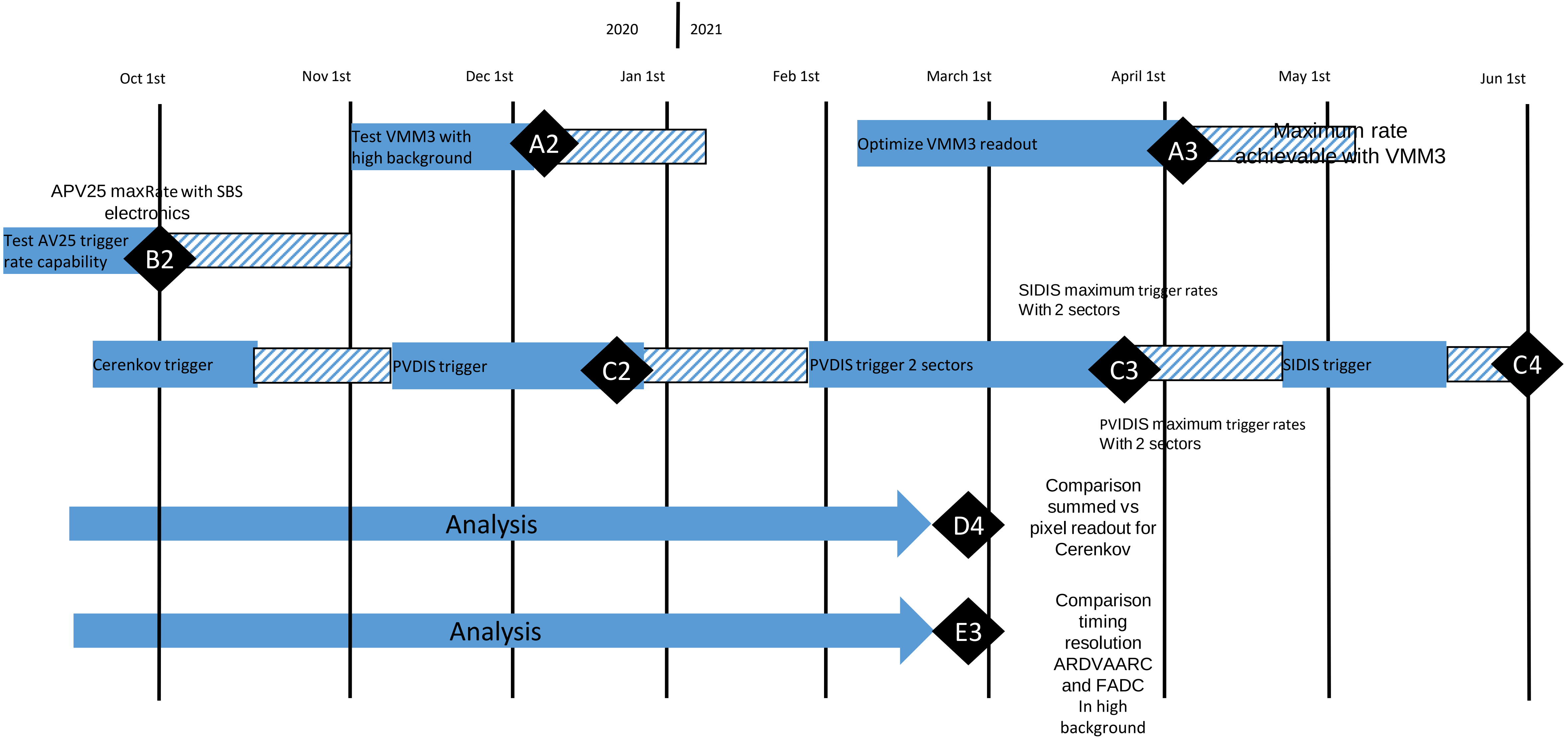
DAQ preRD milestones

- VMM
  - Milestone A1 April 1st 2020 : nish development of VMM3 direct readout
  - Milestone A2 November 1st 2020 : VMM3 will be tested with detector in high background using X-ray and radioactive sources to study behavior of the VMM3 and ensure signal can be well separated from background.
  - Milestone A3 March 1st 2021 : after optimization of the readout, we will determine what is maximum rate achievable for the VMM3 GEM readout
- APV25
  - Milestone B1 June 1st 2020 : while the intrinsic specs of thechip should allow 200 kHz trigger rate using one sample, some development is needed to determine if this is achievable with the existing electronics from SBS. It involves enabling the APV25 buffering and optimizing the data transfer of the readout
  - Milestone B2 October 1st 2020 : Determine rate limits of APV25 trigger rate and same testing in high
  - occupancy environment
- FADC DAQ
  - Milestone C1 April 1st 2020 : develop fast FADC readout (through VXS) to eliminate VME bus data bottle neck
  - Milestone C2 October 1st 2020 : after the full trigger for PVDIS is completed, maximum trigger rate of the setup will be studied for one single sector
  - Milestone C3 Feb 1st 2021 : communication between two sectors will be implemented maximum trigger rate of the setup will then be studied this will be close to final PVDIS setup
  - Milestone C4 March 15th 2021 : SIDIS will be implemented and maximum trigger rate will be determined
- Cherenkov readout
  - milestone D1 February 15th 2020 : Setup FADC crate for Cerenkov sum testing
  - milestone D2 April 15th 2020 : record beam data using total sum and FADC
  - milestone D3 : Test Cherenkov with MAROC in high background sample with beam.
  - milestone D4 February 15th 2020 : complete analysis conclude if pixel readout is required.
- Time of flight
  - Milestone E1 February 1st 2020 : acquire and setup AARDVARC evaluation board
  - Milestone E2 May 15th 2020 : acquire data of scintillator with beam
  - Milestone E3 February 15th 2021 : complete analysis and determine achieved timing resolution with AARDVARC and compare to FADC resolution

preRD schedule



preRD schedule



VMM test

- Ordered two test board 1500 $ x 2
- 1 month get VMM board to work (Ed, Ben)
- Test VMM with real GEM (check signal to noise) 3 months
- Cosmics test
- Develop prototype for data performance, test direct output and test
 with X-ray source

VMM3 prototype board development (Ed)

FPGA for VMM Direct Readout

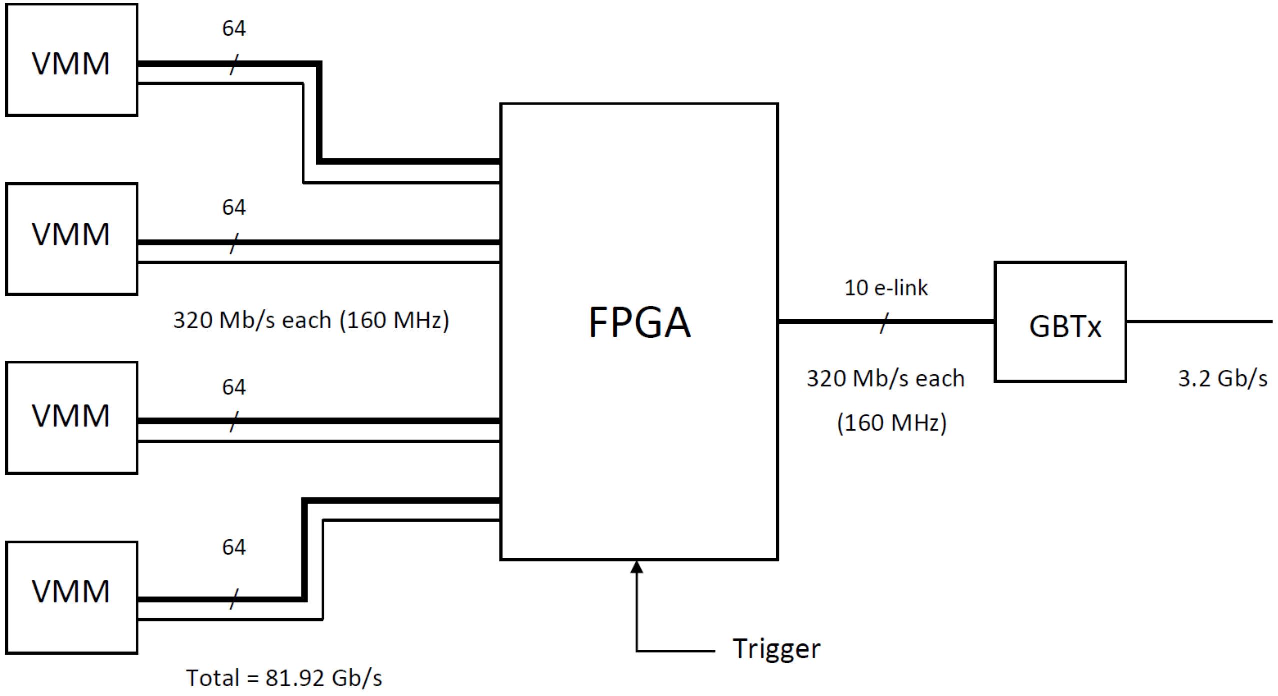
(E.J. 5/28/20)

Proposal

1 FPGA handles direct readout of 4 VMM chips

[64(channels/chip) + 1(clock/chip)] x 2(pins/signal) x 4(chips) = 520 pins (reasonable size, price FPGA)

1 GBTx data link for FPGA output data (10 e-links @ 320 Mb/s = 3.2 Gb/s)



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VMM3 prototype board development (Ed)

Trigger rate (max) = (3200 Mb/s) / (4656 + w*r*3072 b)

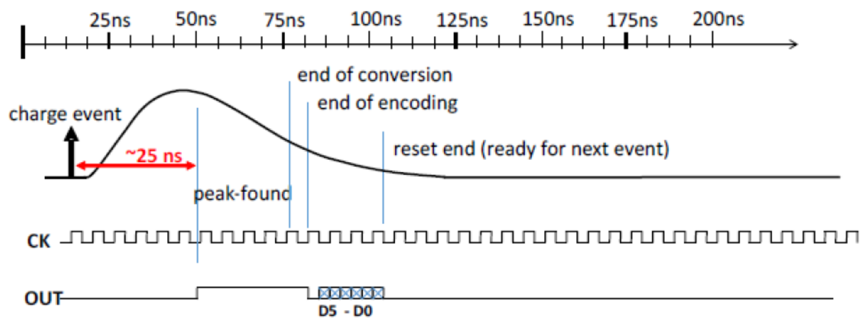
e.g. r = 10 MHz, w = 0.400 μs => Trigger rate (max) = 189 KHz

r = 15 MHz, w = 0.400 μs => Trigger rate (max) = 139 KHz

Or we can solve for the quantity w*r:

R = trigger rate (MHz)

$$w(\mu s) * r(MHz) = 1.04166 / R(MHz) - 1.51563$$



VMM 6-bit ADC Direct Output timing

VMM3 prototype board development (Ed)

- Direct readout with 15 MHz and 400 ns window gives 139 KHz trigger rate capability sufficient for PVDIS and SIDIS, most likely can reach 200 KHz if more segmentation and shorter window applicable

- Simulation of direct outputs by Jinlong ongoing

- Possible issues :
  - Low resolution ADC direct readout not good enough for high rate strips (PVDIS), instrument small angle with APV25 from SBS

VMM3 Risks

- GEM : evaluate VMM to replace APV – need to reach 200 KHz and be able to reconstruct in full backround
- Test ARDVAARC to achieve best timing resolution 150 ps from SPD
- Develop the 2 sectors trigger
- Cerenkov : test MAROC readout, effect of recording all pixels
- Optimize and study deadtime

APV25 tests

- Fiber and transceivers ordered for full scale test
- SSP new firmware up to 32 MPDs developed and being tested with 12 MPDs
- Will add more MPDs when access to lab
- High speed readout of MPDs with VTP will eliminate VME backplane bottleneck (200 MB / s vs 1.25 GB/s) in development (~ 2 months to complete)

AARDVARC / ASOC

- Received Eval board ASOC
- Software installed and running but need test with pulser / detectors
- Test with PMTs on bench cosmics
- Try opportunistic beam test during next run
- Test with Radioactive source

FADC test stand

- Duplicate setup at Umass / agreed to do FADC tests for SoLID
- Order crates and auxiliary board (delivered 3 months)
- Borrow FADCs (save 25 K$)

- Develop clustering and coincidence with Cerenkov (Ben 3 months)

- Beam test during A1n/d2n with calorimeter / Cerenkov / SPD

- Last 6 months order second crates and test with 2 sectors for interface

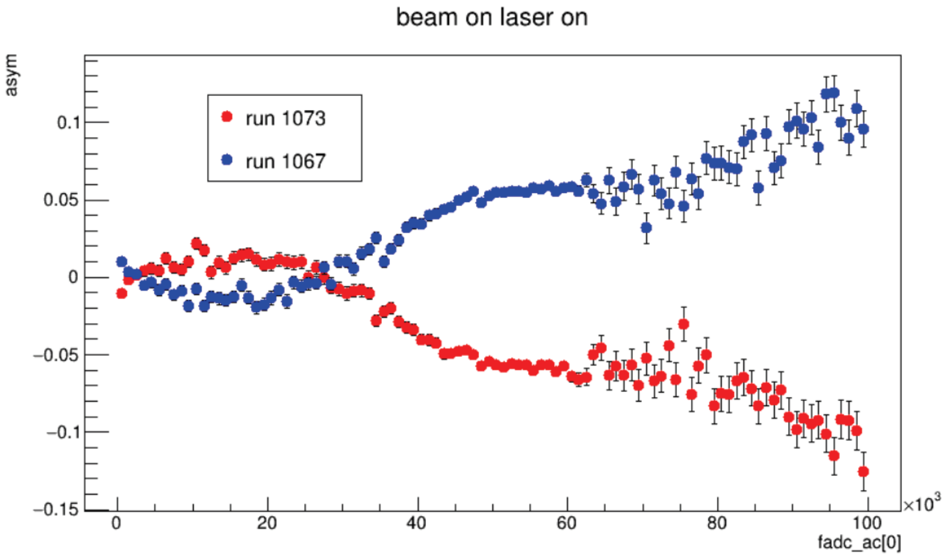
Preliminary results from Compton

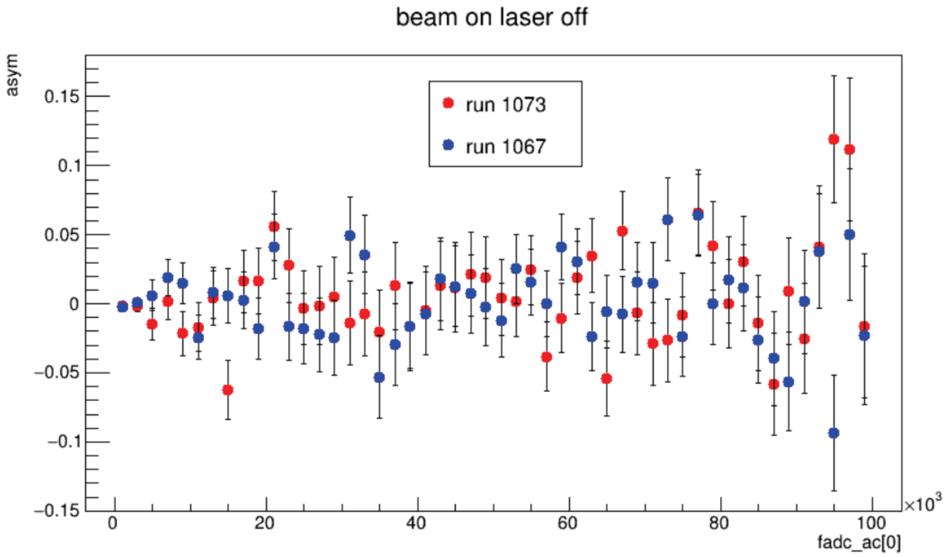
- FADC + VETROC + VTP (trigger module)
- Implemented delayed helicity readout
- Helicity scaler with VETROC and VTP for normalization (deadtime, power, position)
- Photon (and electron trigger)

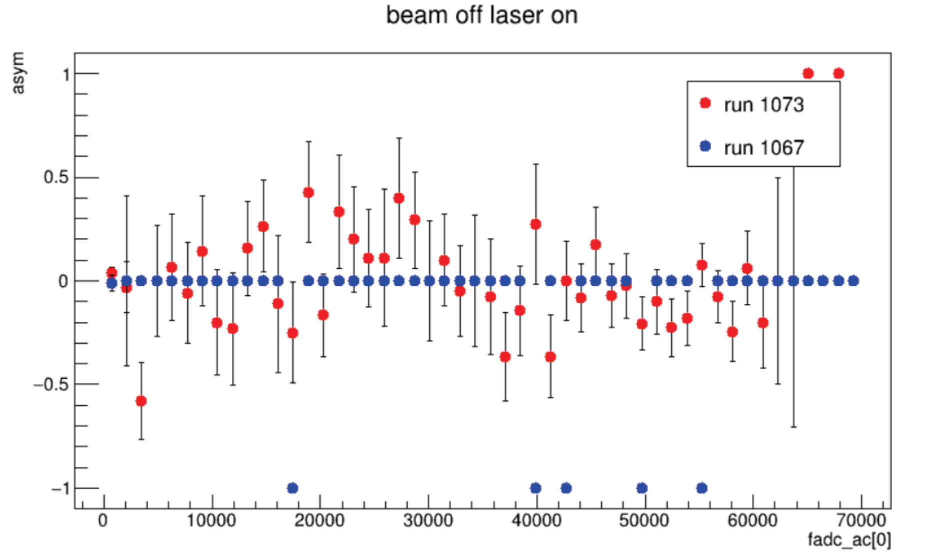
- Software

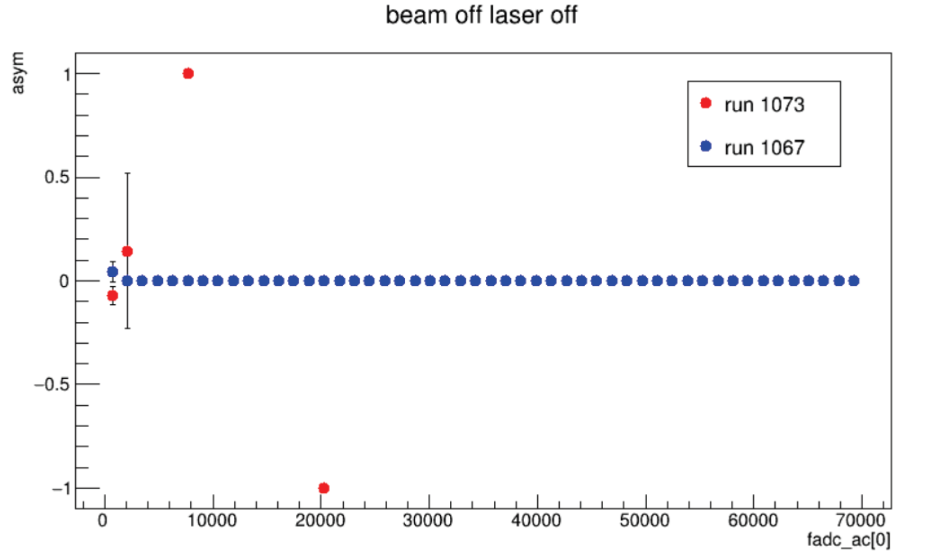
Preliminary results from Compton

- Rates up to 50 KHz with deadtime of about 10%
- Compton Asymmetry from Photon







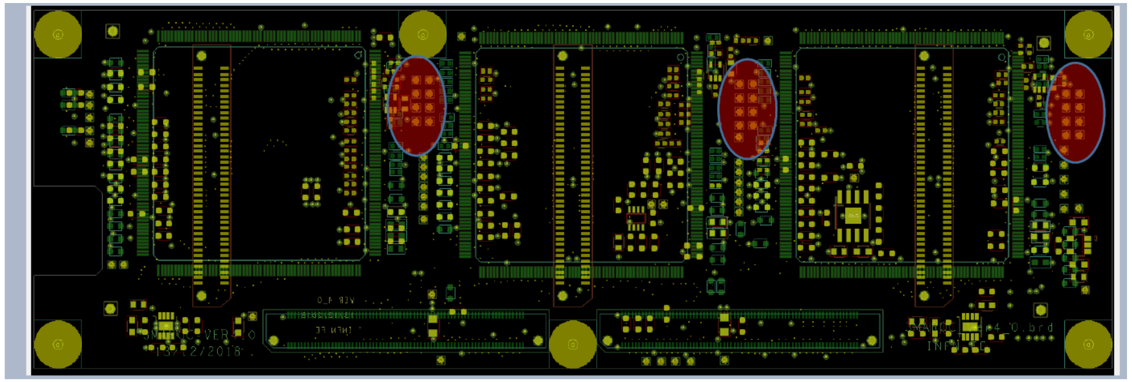


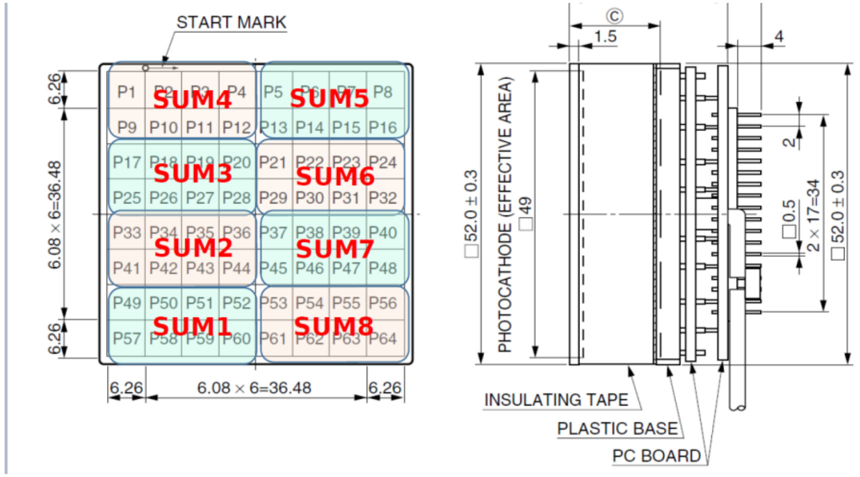
FADC test stand

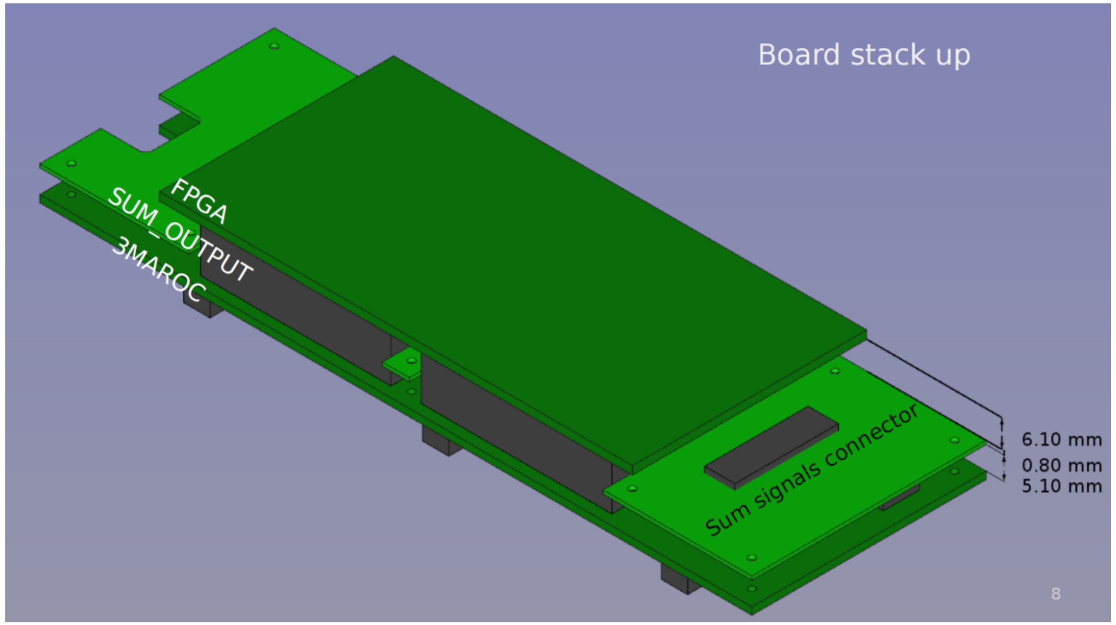
- Calorimeter and Cerenkov trigger ready to be test in Hall C
- On going VXS FADC readout for faster FADC readout
- Test calorimeter two crates trigger this summer

MAROC

- INFN Ferrara accepted to modify RICH board to have sum output (Big thank you !)
- Electronics produced and at JLab but stuck in shipping and receiving
- Need to test it and set up readout (1 week)
- Possible test run







Conclusion

- Requirements
  - 3 GB/s for PVDIS (20 KHz per sector) and SIDIS (100 KHz trigger rate) can be handled by SILO without L3 trigger
  - FADC deadtime ok for PVDIS, study of GEM readout deadtime ongoing (most likely ok for VMM3)
  - PreRD work on going
    - All tasks planned before end of preRD might be shifte
    - VMM preRD done close to the end, if direct readout

Backup

Tape

Cost							2018	2020	2023
		Days	Data rate	Seconds	Total data TB	Double	DLO8 in $	LTO 9	LTO10
E12-11-108	Pol proton	120	3900	10368000	40435	80870	473850	242611	126360
E12-12-006	J/Psi	60	4000	5184000	20736	41472	243000	124416	64800
E12-10-006	Transv. Pol. 3He	90	6000	7776000	46656	93312	546750	279936	145800
E12-11-007	Long. Pol. 3 He	35	6000	3024000	18144	36288	212625	108864	56700
E12-10-007	PVDIS	169	6000	14601600	87610	175219	1026675	525658	273780
	Total	474		40953600	213581	427162	2502900	1281485	667440
Actual days	Actual years		Time in s						
948	2.60	474	40953600						

Cost tape

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E12-10-006	Transv. Pol. 3He	90	6000	7776000	46656	93312	7290	3732	1944
E12-11-007	Long. Pol. 3 He	35	6000	3024000	18144	36288	2835	1452	756
E12-10-007	PVDIS	169	6000	14601600	87610	175219	13689	7009	3650
	Total	474		40953600	213581	427162	33372	17086	8899
Actual days	Actual years		Time in s						
948	2.60	474	40953600						

Number of tapes

GEM APV readout with SSP

- Implementation of noise rejection on SSP for SBS
- Need to evaluate rejection factor for SoLID background
- Check ultimate performance for trigger rates

PVDIS crate layout