VMM3 fast readout investigation

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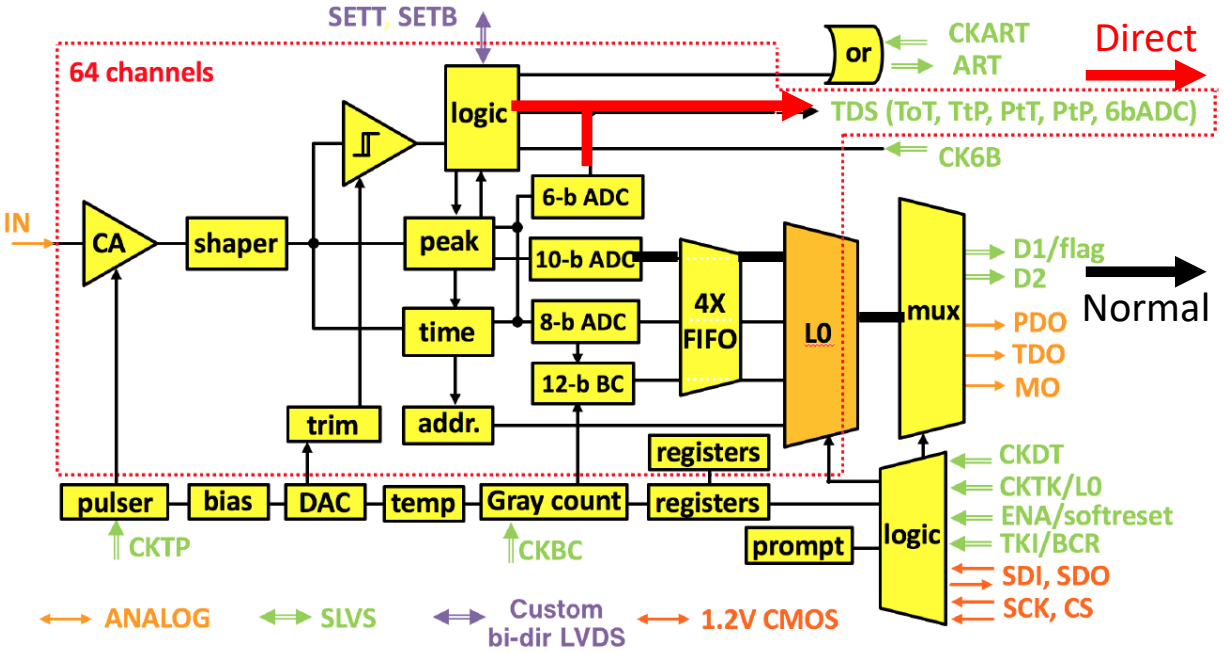
6/8/20

VMM3 chip

VMM3 block diagram



- ASIC for ATLAS New Small Wheel
- Radiation hard similar to APV25 : > 100 Mrad
- 64 channels
- Low noise over wide range of input capacitance (<1 pF to ~1 nF)
- Shaping times : 25 ns, 50 ns, 100 ns, 200 ns
- Pulse amplitude proportional to charge at input
- Gains : 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC
- **6 bit ADC (25 ns conversion)** and **10 bit ADC (250 ns conversion)**, 8 bits TDC (1 ns resolution), 12 bits Beam Crossing time stamp
- 4 MHz of rate per channel thanks to multilevel FIFO
- Continuous or triggered readout on normal data path
- Latency up to 16 μs in triggered mode
- **Fast direct outputs (64 channels) for ATLAS trigger (6b ADC, ToT)**
- Normal data link up to 320 Mb/s

- SoLID preRD
  - Check signal to noise with detector
  - Test fast direct output quality for high rate readout
  - Identify possible final readout solution of VMM3 for SoLID

VMM3 Evaluation Board

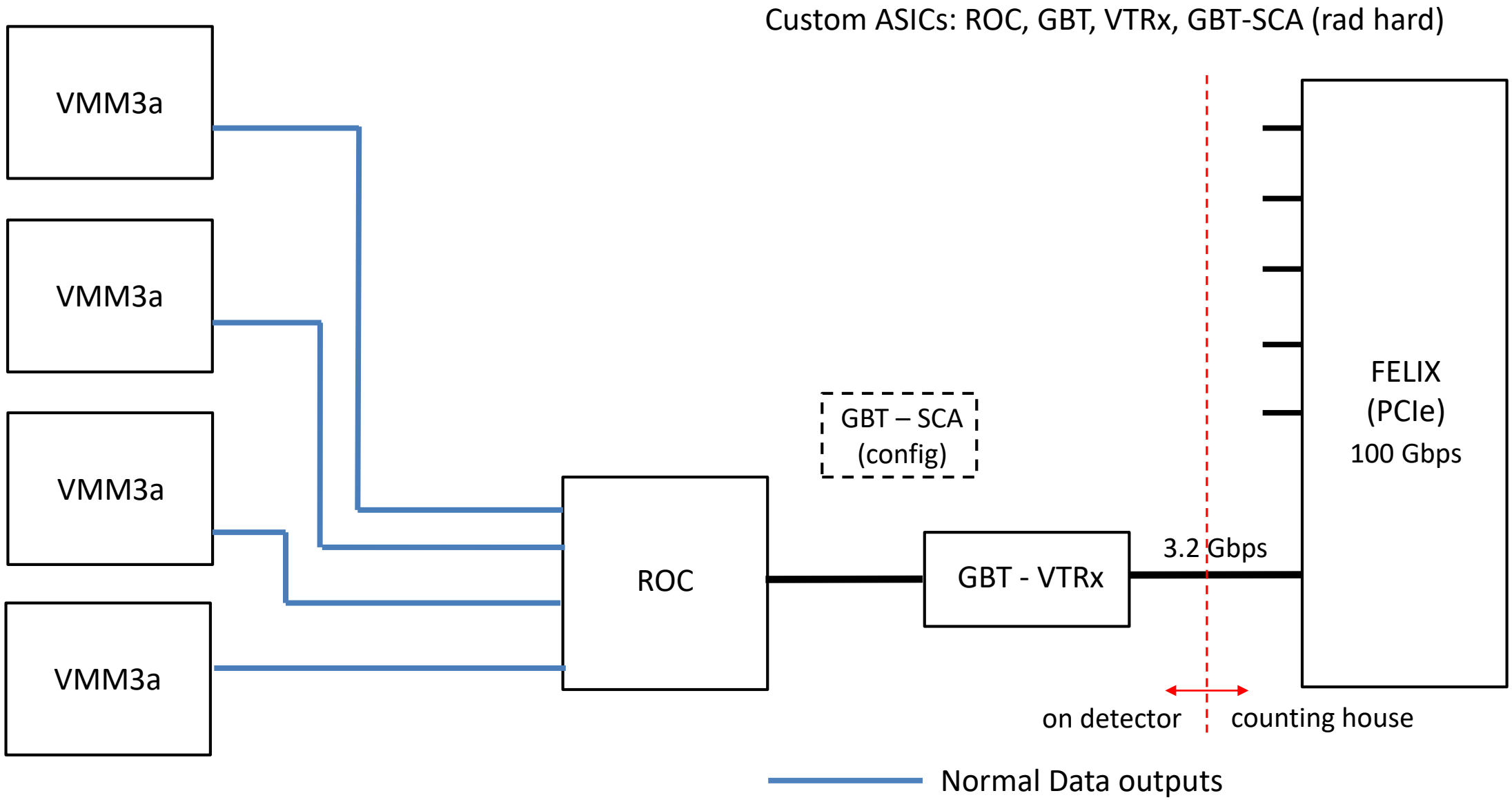
- Linux virtual machine (VirtualBox) on Windows 10 PC to run VMM configuration and acquisition software (VERSO)
- Able to configure VMM on evaluation board and acquire data using built in pulser of VMM chip (normal data path)
- Data has problems – no scope available to look at diagnostic outputs on board
- Discussions with ATLAS person about configuration parameters
- Now have later version of the software
- Work in progress …

- Evaluation board routes direct outputs of 12 VMM channels to connector
- Will cable this connector to an existing FPGA board to read out 6b ADC data
- Some firmware development required – will give us first look at direct outputs

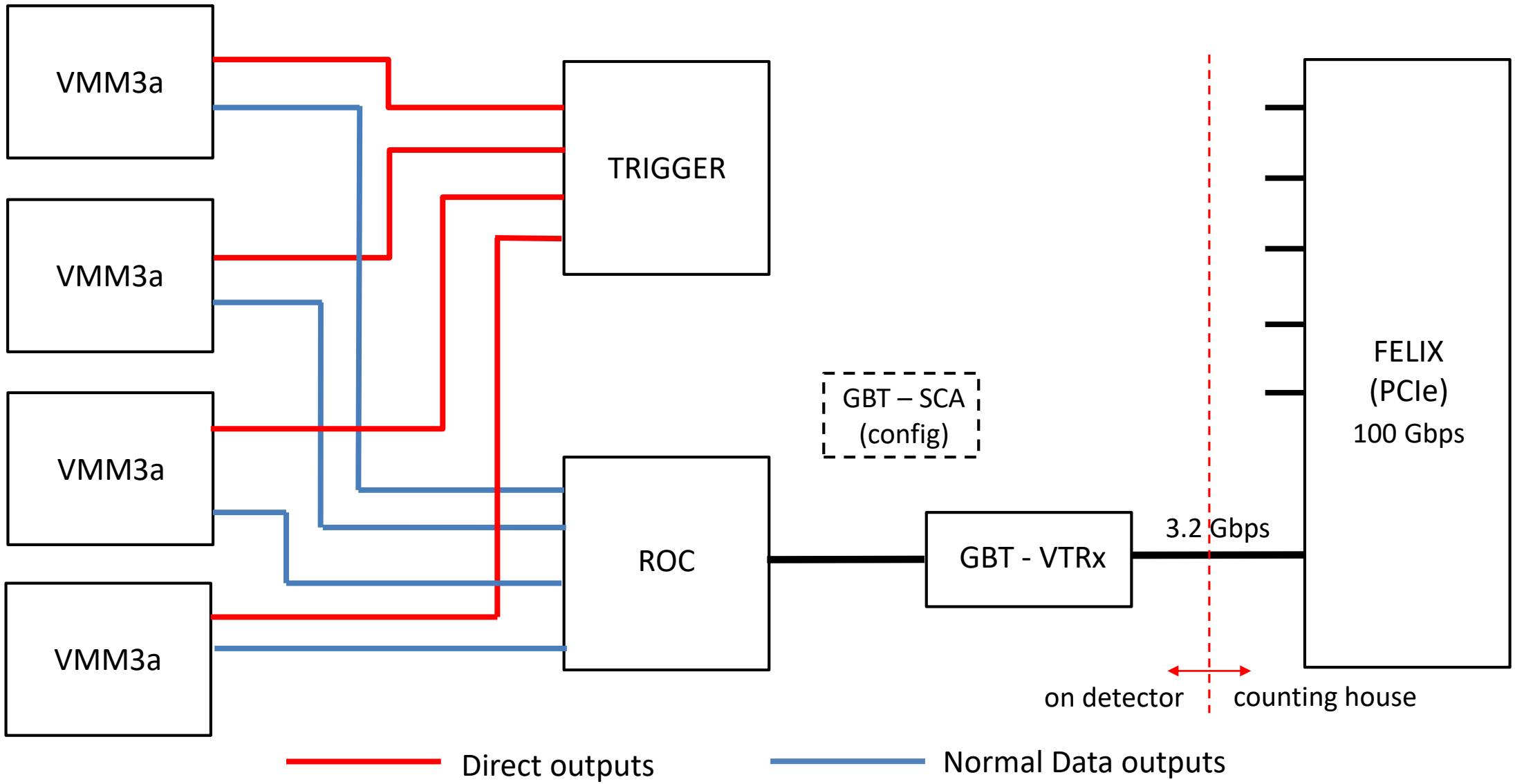
X-ray, beam test

- Require detector (~10 cm x 10 cm) readout with multiple VMM chips at high rate (8 VMM, 512 channels)
- Need to develop new circuit board
- Considering 2 options:
    (1) Add readout path for direct outputs while keeping normal ATLAS readout path intact
    (2) Combine direct and normal outputs into a new single readout path

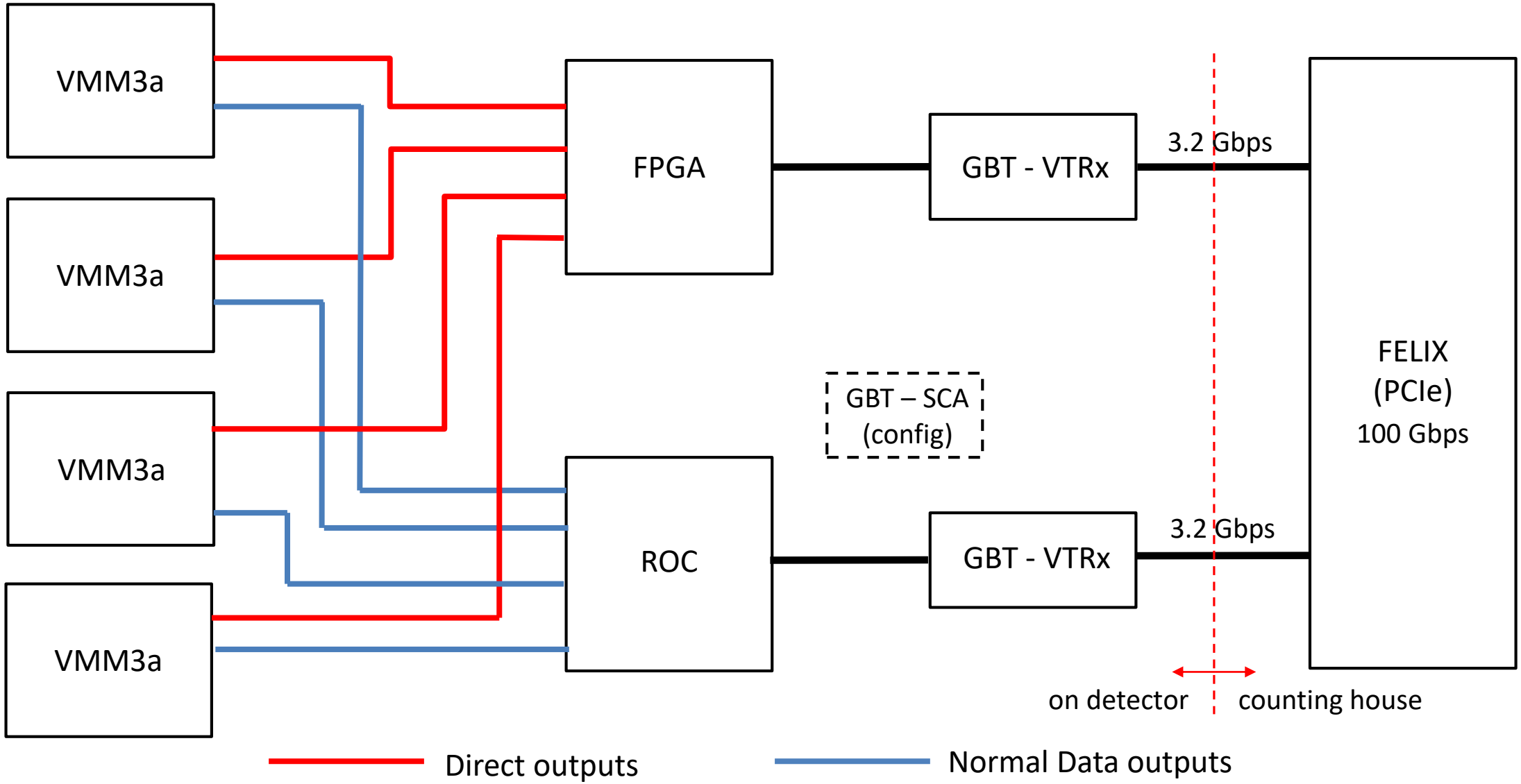
ATLAS New Small Wheel Readout



ATLAS New Small Wheel Trigger and Readout



Option 1: Add VMM Direct Output Data Path in Parallel to ATLAS Normal Data Path

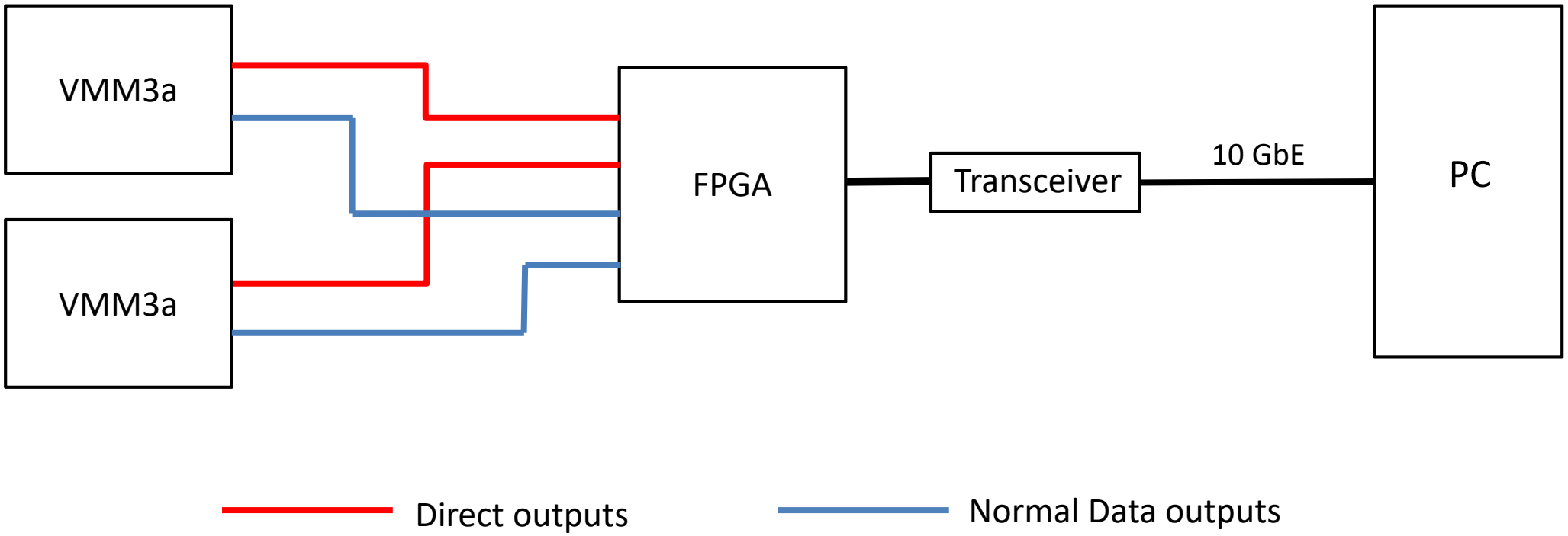


Option 1: Add VMM Direct Output Data Path in Parallel to ATLAS Normal Data Path

- Close to final solution for SoLID
  - All components on detector except FPGA are rad hard
  - 4 VMM group with 1 GBT in direct path meets (preliminary) high rate requirements
  - Supporting only 4 VMMs per board reduces size and complexity of FPGA (important when implementing design techniques to mitigate radiation issues, or in cost to replace FPGA with a custom ASIC)
  - Can choose either readout path for lower rate channels
  - Felix - GBT downlink has fixed latency for distribution of clock, trigger, sync; configuration path for all ASICs is defined (GBT-SCA)
  - Felix card in hand – high interest level at JLab to get Felix readout integrated into CODA

- Downside
  - Besides VMM, we need to acquire the custom ASICs from CERN and ATLAS collaborators soon (we have a few spare GBT, VTRx, GBT-SCA)
  - Only ONE Felix card on hand
  - PCB layout is complex (help from USTC, China – have their design, same CAD system)
  - Limited usefulness to others at JLab interested in evaluating VMM since Felix card is required ($12K, availability?)

Option 2: Combine VMM Direct and Normal Outputs into Single Data Path



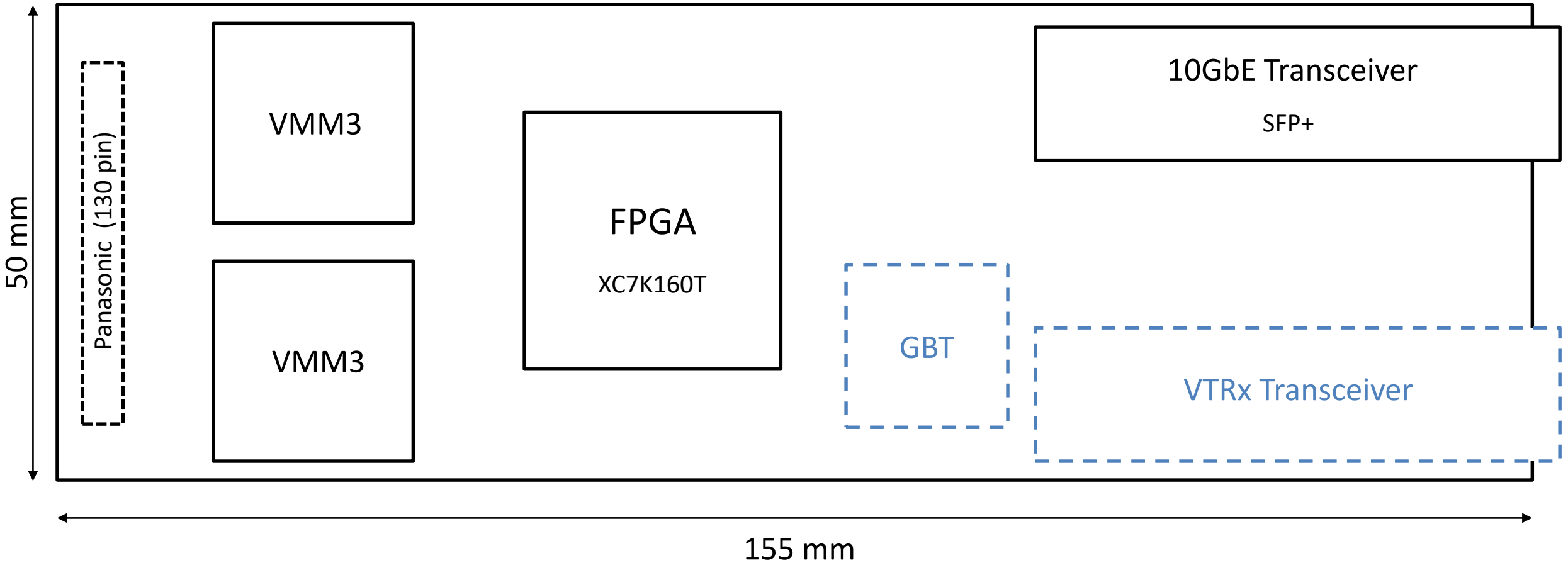
Option 2: Combine VMM Direct and Normal Outputs into Single Data Path

- A simpler solution for evaluating and comparing both readout modes
  - 2 VMM with single 10 GbE link exceeds all rate requirements
  - Except for VMMs, no custom ASICs
  - PCB is simpler with less components – complexity moved into FPGA (so deployed earlier)
  - 10 GbE interface for FPGA already exists (Ben Raydo)
  - Felix is not required – anybody can assemble a test stand with a PC and limited additional hardware

- Downside
  - Not a final solution for SoLID
  - Need to append clock, sync, and trigger distribution (no problem for small system)

- Probably the best approach to get a multichip VMM system running quickly

Single Data Path Implementation

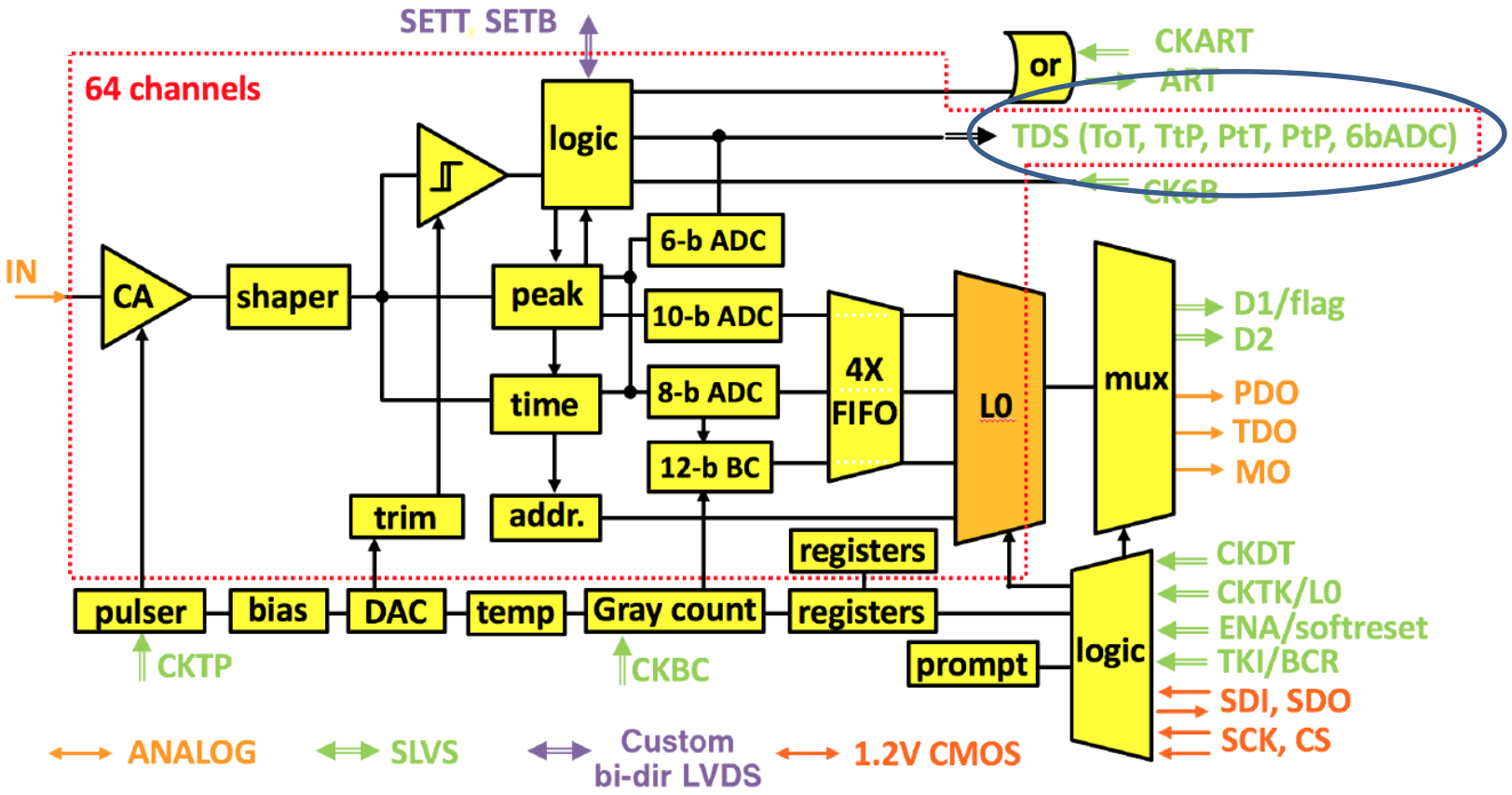


Other Activities

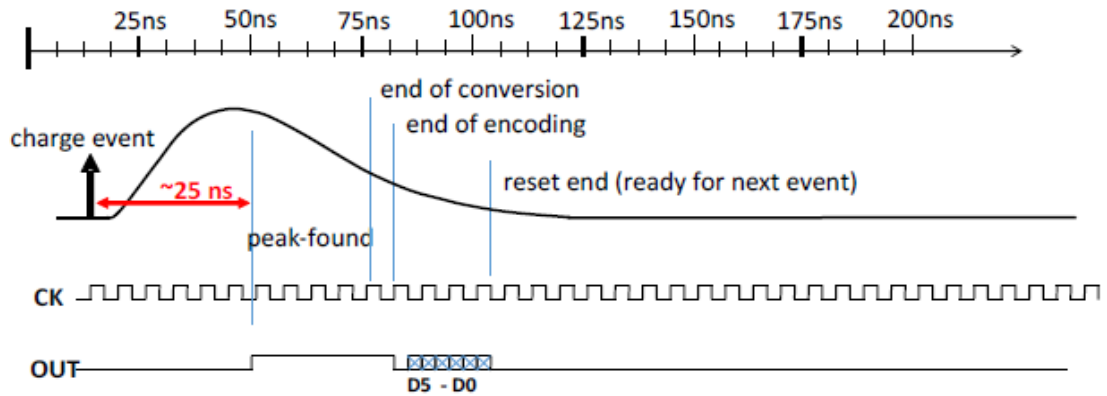
- Investigate FPGA design techniques to mitigate effects of radiation (TMR – Triple Modular Redundancy)
- Plan to test with cables connecting front-end boards (VMM3) to GEMs – lowers radiation exposure of FPGA
- Try to get a cost estimate for conversion of FPGA design to rad hard ASIC
  - ROC ASIC is of similar complexity as our FPGA in Option 1 (dual readout paths)
  - All digital, no high speed serialization
  - Will contact ROC designers about the process and cost

SPARE SLIDES

Direct readout path

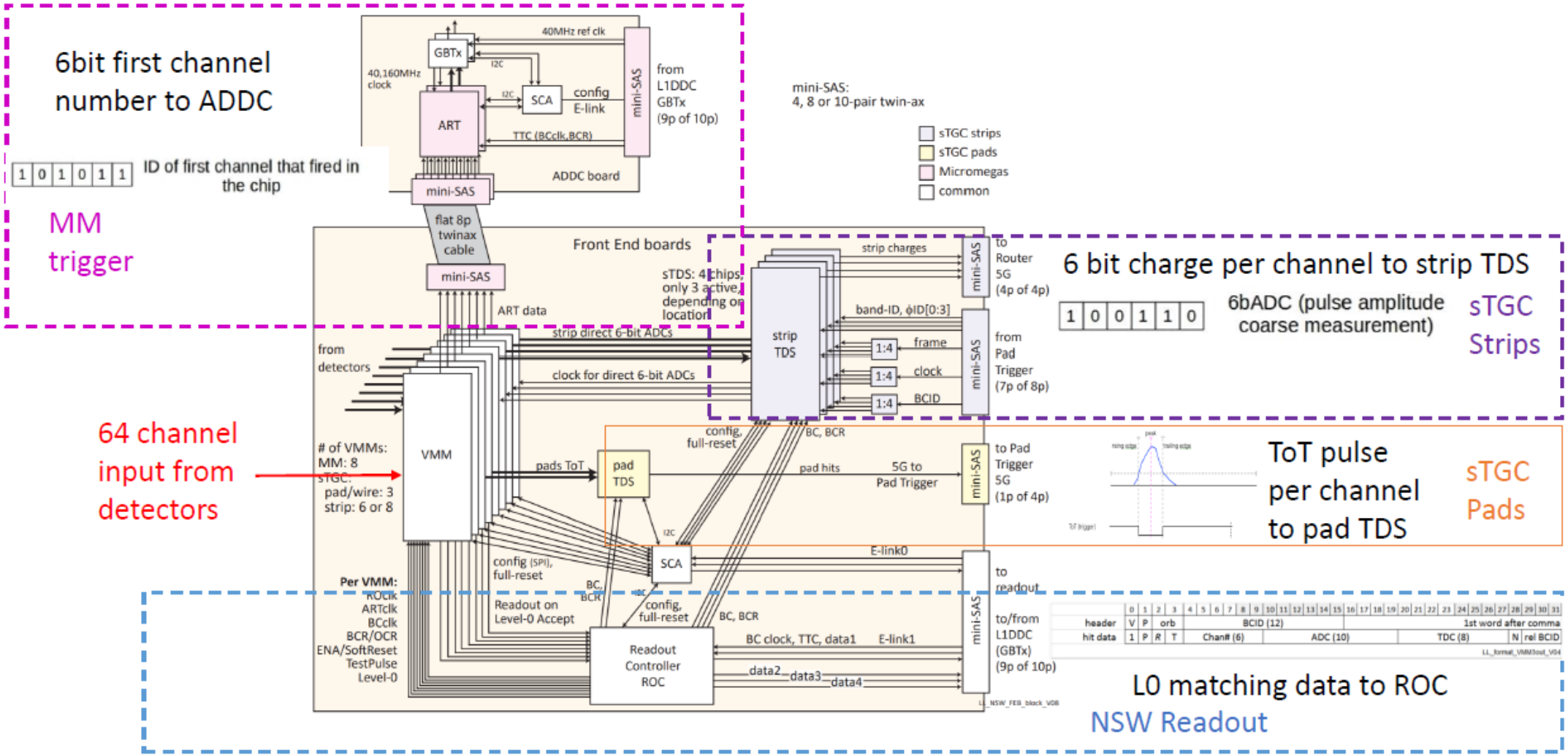


- sTGC path
  - 6 bit ADC
  - ToT
  - Threshold

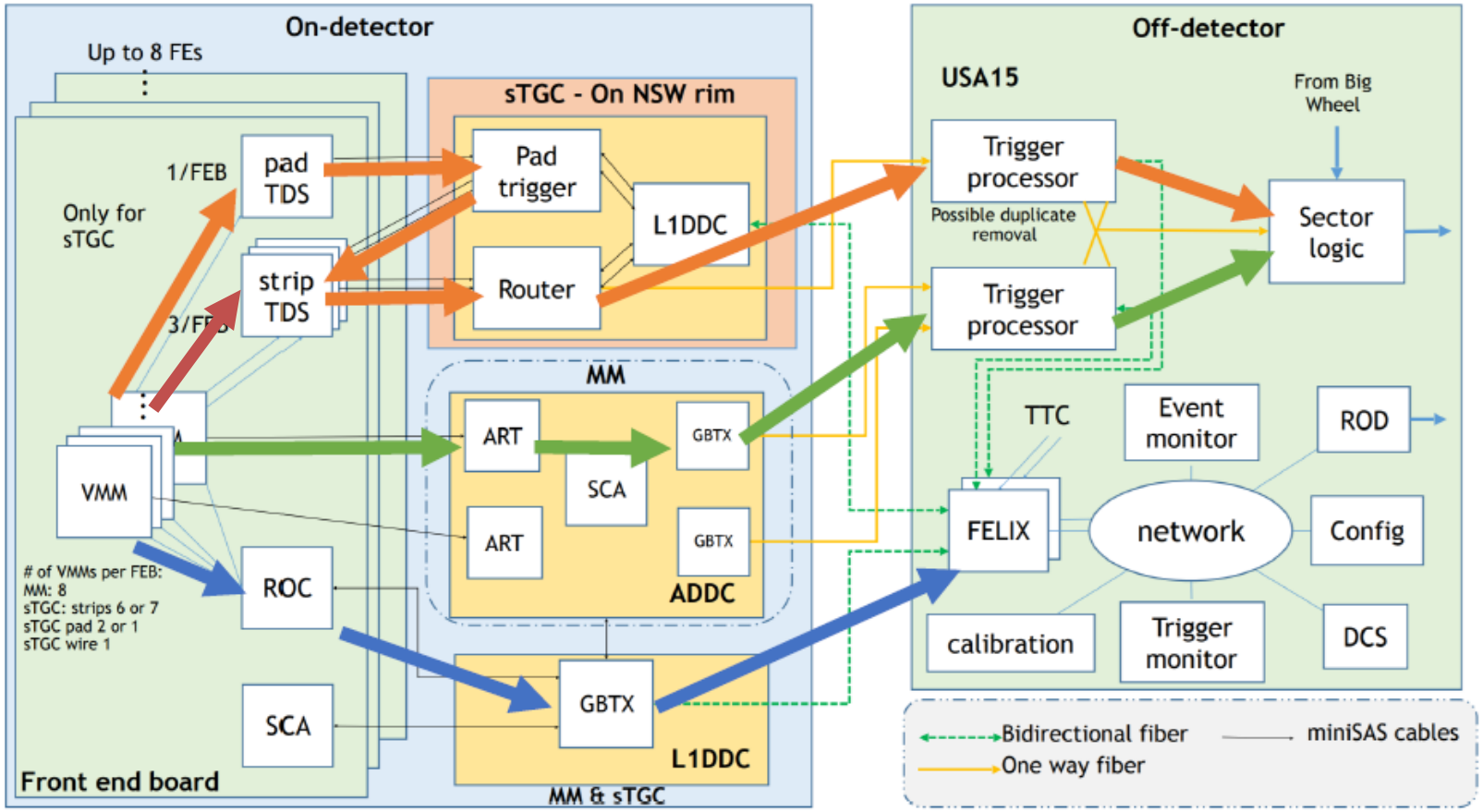


VMM 6-bit ADC Direct Output timing

VMM Interface



ATLAS New Small Wheel Electronics

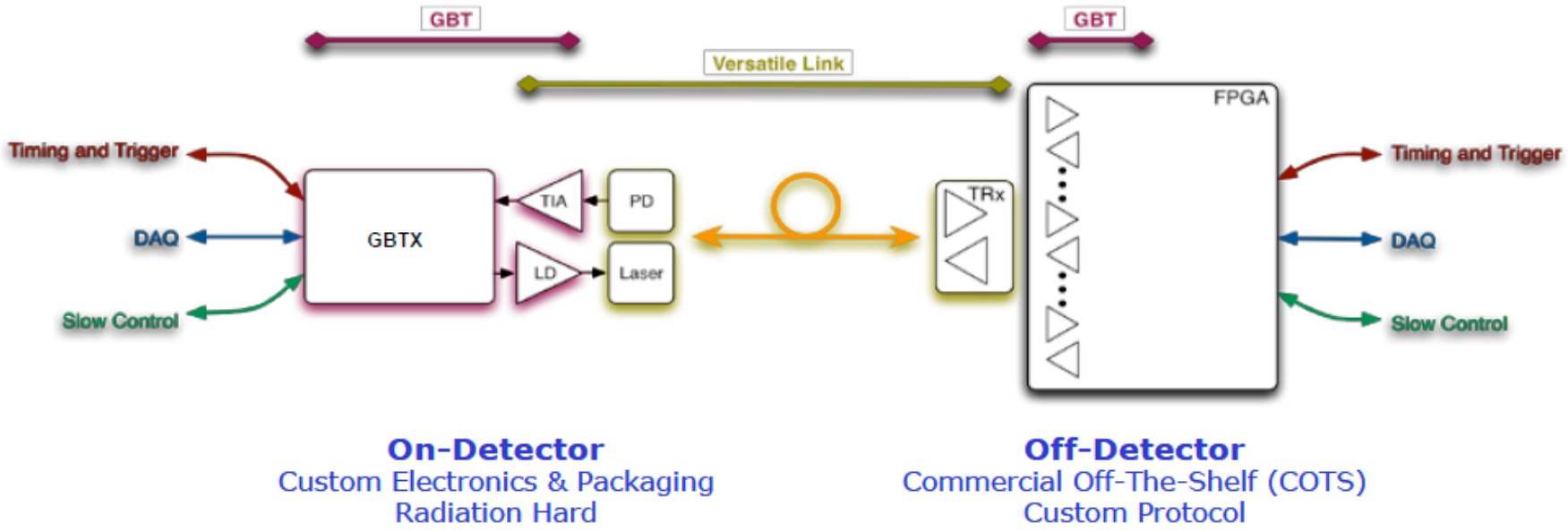


sTGC Trigger MM Trigger NSW Readout

Radiation tolerant ASICs:
- VMM (amplifier, shaper, discriminator)
- Read Out Controller (ROC)
- Trigger Data Serialiser (TDS)
- Address Real Time (ART)
- Slow Control Adapter (SCA)
- GigaBit Transceiver (GBTX)

PCBs:
pFEB/sFEB(sTGC pad/strip front-end board)
MMFE8(Micromegas front-end board)
L1DDC(Level-1 Data Drive Card)
Pad Trigger
Router
ADDC
FELIX(Front-End LInk eXchange)
Trigger Processor

GBT link



Single bidirectional optical link simultaneously provides data paths for:

- Timing and Trigger Control (TTC)
- Data Acquisition (DAQ)
- Slow Controls (SC) – configuration and monitoring

<u>Fixed Latency</u>

VMM3 Evaluation Board

- Received evaluation board from UVA just after lab shutdown began
- Wired up power supply at home