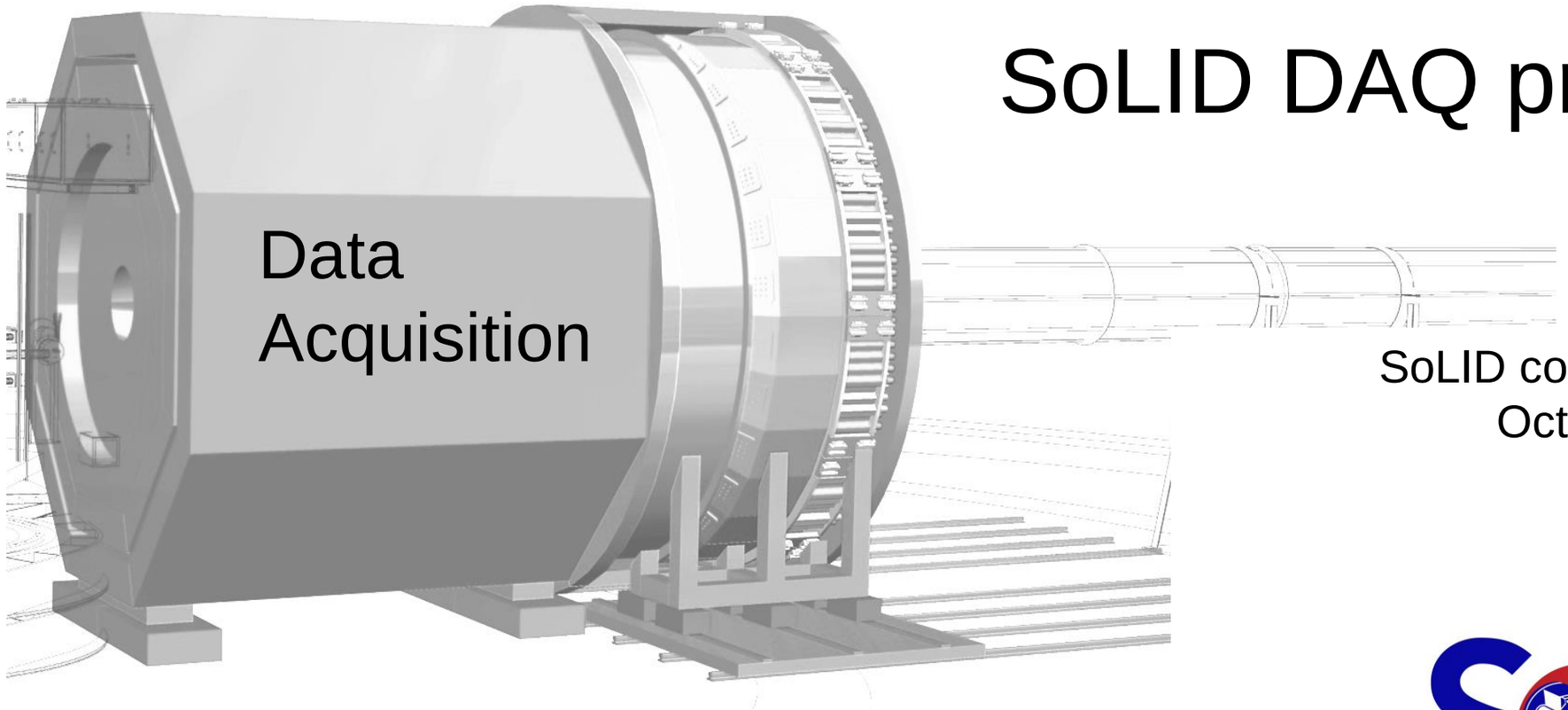


SoLID DAQ preRD

Data Acquisition

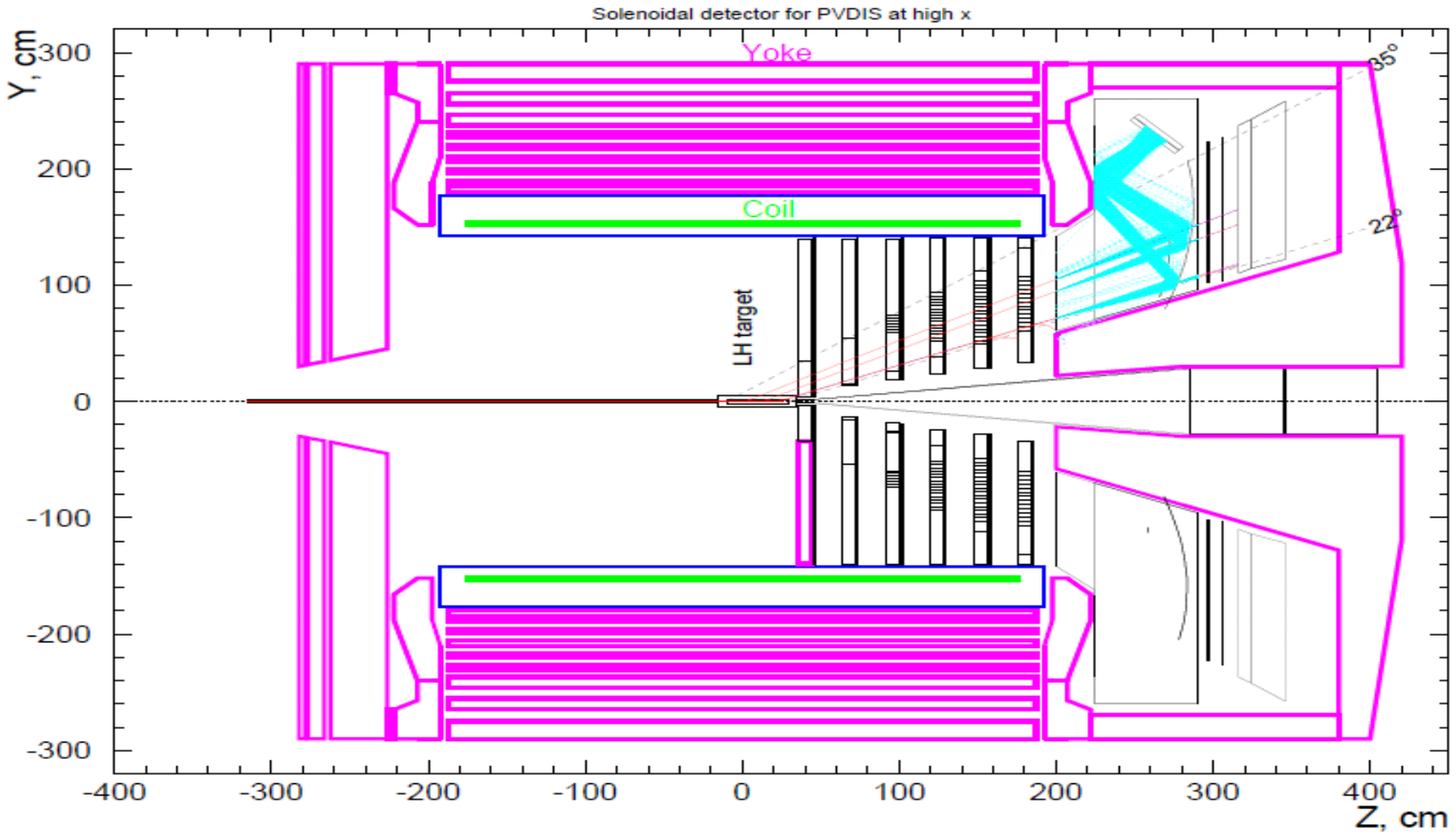
SoLID collaboration meeting
October 9th 2020

Alexandre Camsonne

Outline

- Requirements
- DAQ risks
- Data rates
- Timeline preRD
- PreRD items
  - VMM
  - APV25
  - FADC test stand
  - MAROC
- Tasks and milestone

Detector layout and trigger for PVDIS



Trigger

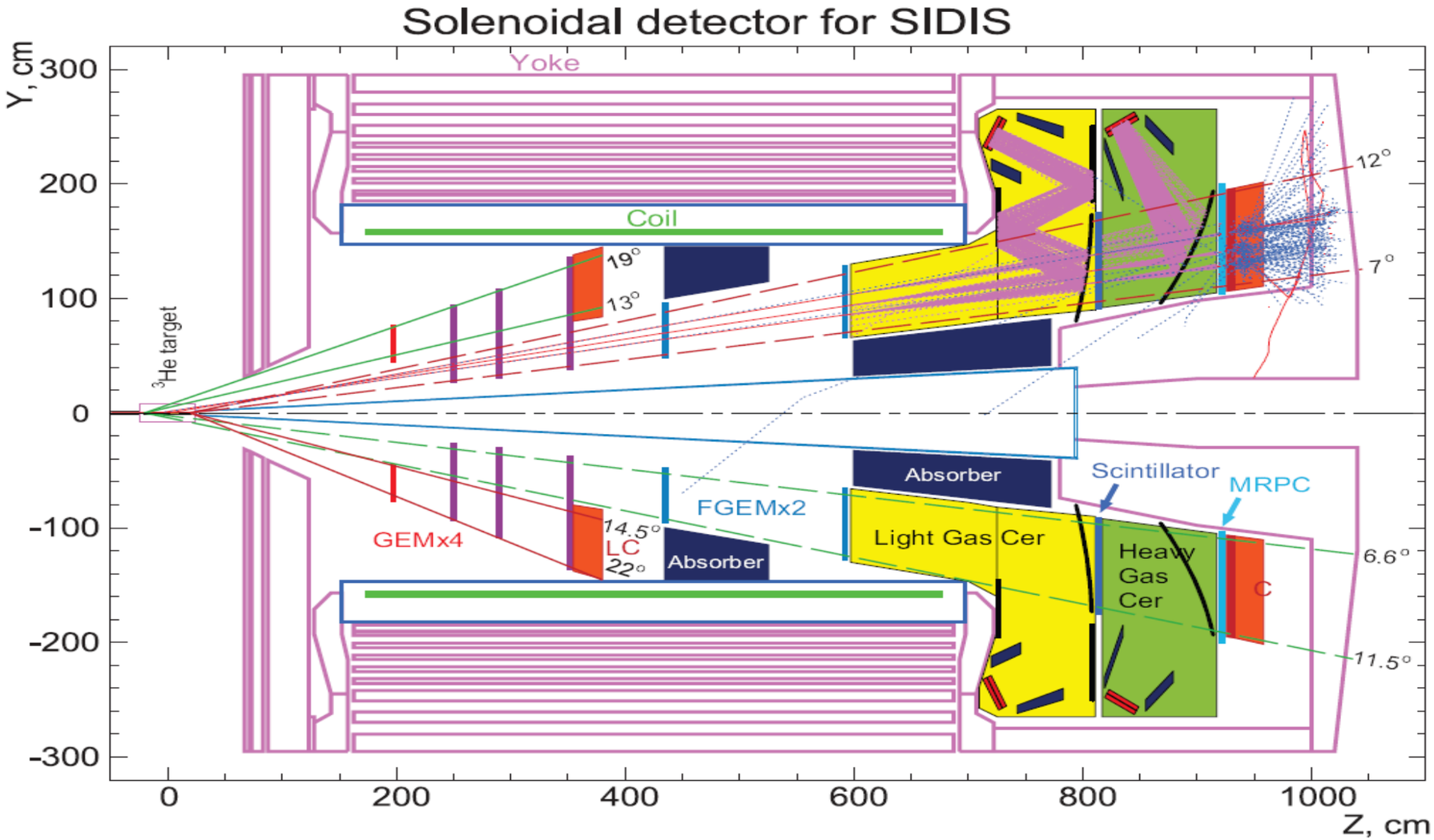
Calorimeter
+
Cerenkov

200 to 500 KHz of electrons

30 individual sectors

Max 17 KHz/sector

Detector layout and trigger for SIDIS



Trigger

Calorimeter
+
Cerenkov
+
SPD

30 sectors
Combined
in
10 regions of interests
Max rate 200 KHz

Baseline 60 KHz
coincidence e- pion

SoLID requirements

Experiments	PVDIS	SIDIS-^{3}He	SIDIS-Proton	J/ψ
Reaction channel	$p(\vec{e},e')X$	$(e,e'\pi^{\pm})$	$(e,e'\pi^{\pm})$	$e+p\rightarrow e'+J/\Psi(e^-,e^+)+p$
Approved number of days	169	125	120	60
Target	LH_2/LD_2	^{3}He	NH_3	LH_2
Unpolarized luminosity ($cm^{-2}s^{-1}$)	$0.5\times10^{39}/1.3\times10^{39}$	$\sim 10^{37}$	$\sim 10^{36}$	$\sim 10^{37}$
Momentum coverage (GeV/c)	2.3-5.0	0.8-7.0	0.8-7.0	0.6-7.0
Momentum resolution	~2%	~2%	~2%	~2%
Polar angle coverage (degrees)	22-35	8-24	8-24	8-24
Polar angle resolution	1 mr	0.6 mr	0.6 mr	0.6 mr
Azimuthal angle resolution	-	5 mr	5 mr	5 mr
Trigger type	Single e^-	Coincidence $e^-+\pi^{\pm}$	Coincidence $e^-+\pi^{\pm}$	Triple coincidence $e^-e^-e^+$
Expected DAQ rates	<20 kHz $\times$ 30	<100 kHz	<100 kHz	<30 kHz
Backgrounds	Negative pions, photons	$(e,\pi^-\pi^{\pm})$ $(e,e'K^{\pm})$	$(e,\pi^-\pi^{\pm})$ $(e,e'K^{\pm})$	BH process Random coincidence
Major requirements	Radiation hardness 0.4% Polarimetry π^- contamination Q^2 calibration	Radiation hardness Detector resolution Kaon contamination DAQ	Shielding of *sheet-of-flame* Target spin flip Kaon contamination	Radiation hardness Detector resolution

Risks associated with DAQ

	Risk	Level	WBS	Mitigation
GEM readout	100 KHz capability Achieved resolution	High	1.2.4.2,1.1.5.3	Simulation, test
Data rates	Bandwidth sufficient, electronics can handle	Medium	1.1.5.1.4	Test (preRD and R&D)
Trigger rate	Can required trigger rate reached for SIDIS	Medium	1.1.5.1.7,1.1.5.1.8	Test (preRD and R&D)
Deadtime PVDIS	Can deadtime be an issue for PVDIS ?	High	1.2.4.2,1.1.5.3 1.1.5.1.7,1.1.5.1.8	Drives chip choice and electronics design
Data reduction	Can data be reduced to a reasonable size for silo ?	Medium		Simulation,test,beam test
Cost	Can performance required be reached within budget	Medium		Test
Particle ID	Background rejection sufficient	High		Simulation, beam test

Event size data rates PVDIS APV25

				Event size		Data rate MBs	After noise cut	strips firing	event size bytes		MB/s
1	1156	21.17	244.73	3038.03	3038.03	60.76	9.97	115.25	1430.76	1430.76	28.62
2	1374	10.35	142.21	1765.39	1765.39	35.31	5.11	70.21	871.61	871.61	17.43
3	1374	8.81	121.05	1502.71	1502.71	30.05	4.42	60.73	753.92	753.92	15.08
4	2287	3.07	70.21	871.60	871.60	17.43	1.64	37.51	465.61	465.61	9.31
5	2350	2.79	65.57	813.93	813.93	16.28	1.50	35.25	437.60	437.60	8.75
					Total	159.83				Total	79.19
FADC											
	20000						10				
	Event size FADC	Nb channel	Header			Trailer	Sample				
	Calorimeter	14	4			4	12	280			
	Preshower	9	4			4	12	180	400		
	Cerenkov	9	4			4	12	180			
									11600000		
								740	11600000	11.6	
									Total rate	94	MB/s

About 2.9 GB/s for PVDIS at 20 KHz

Occupancy with VMM3 being studied

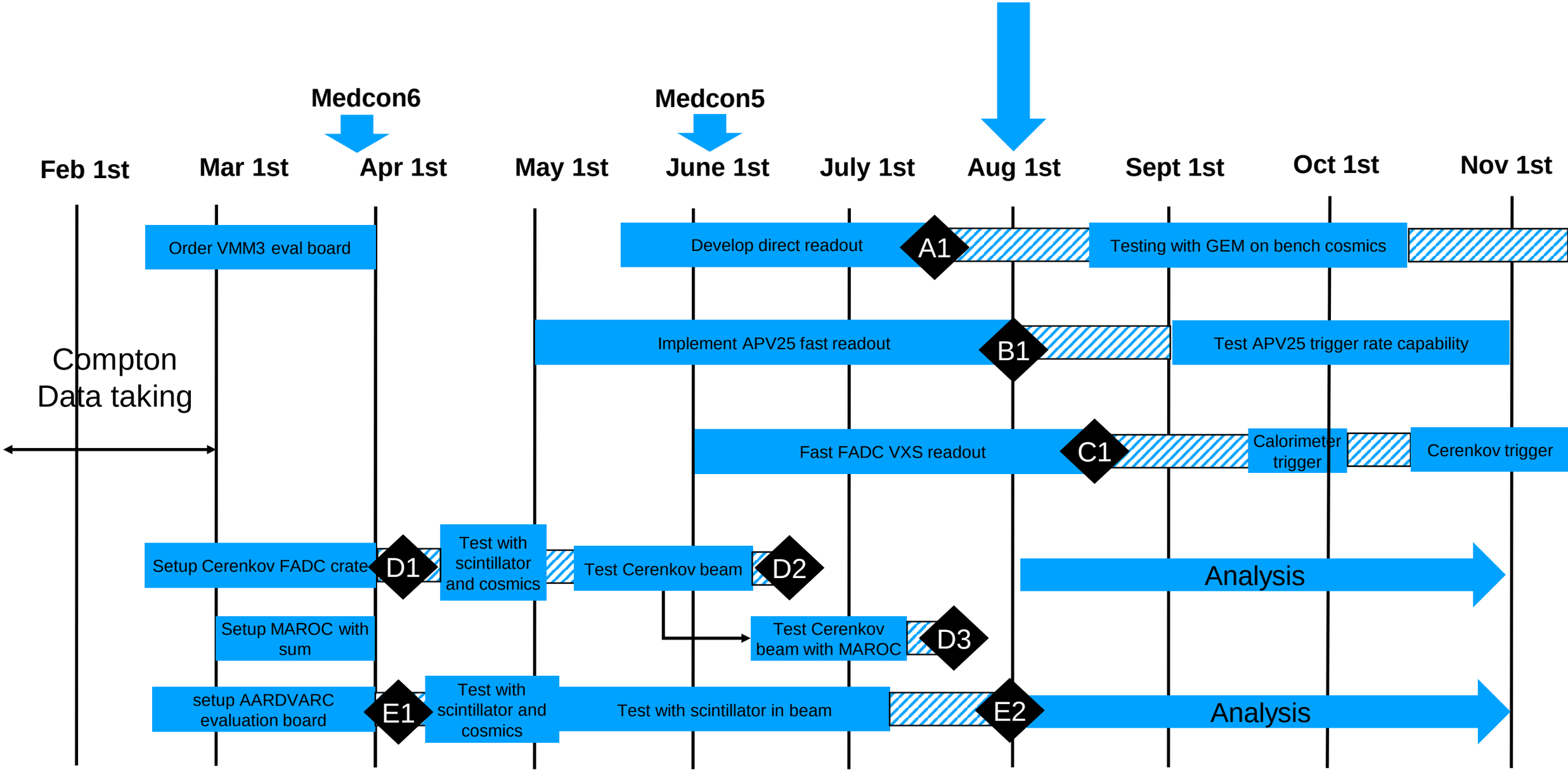
Expect factor 3 reduction due to faster integration time and no need for 3 samples

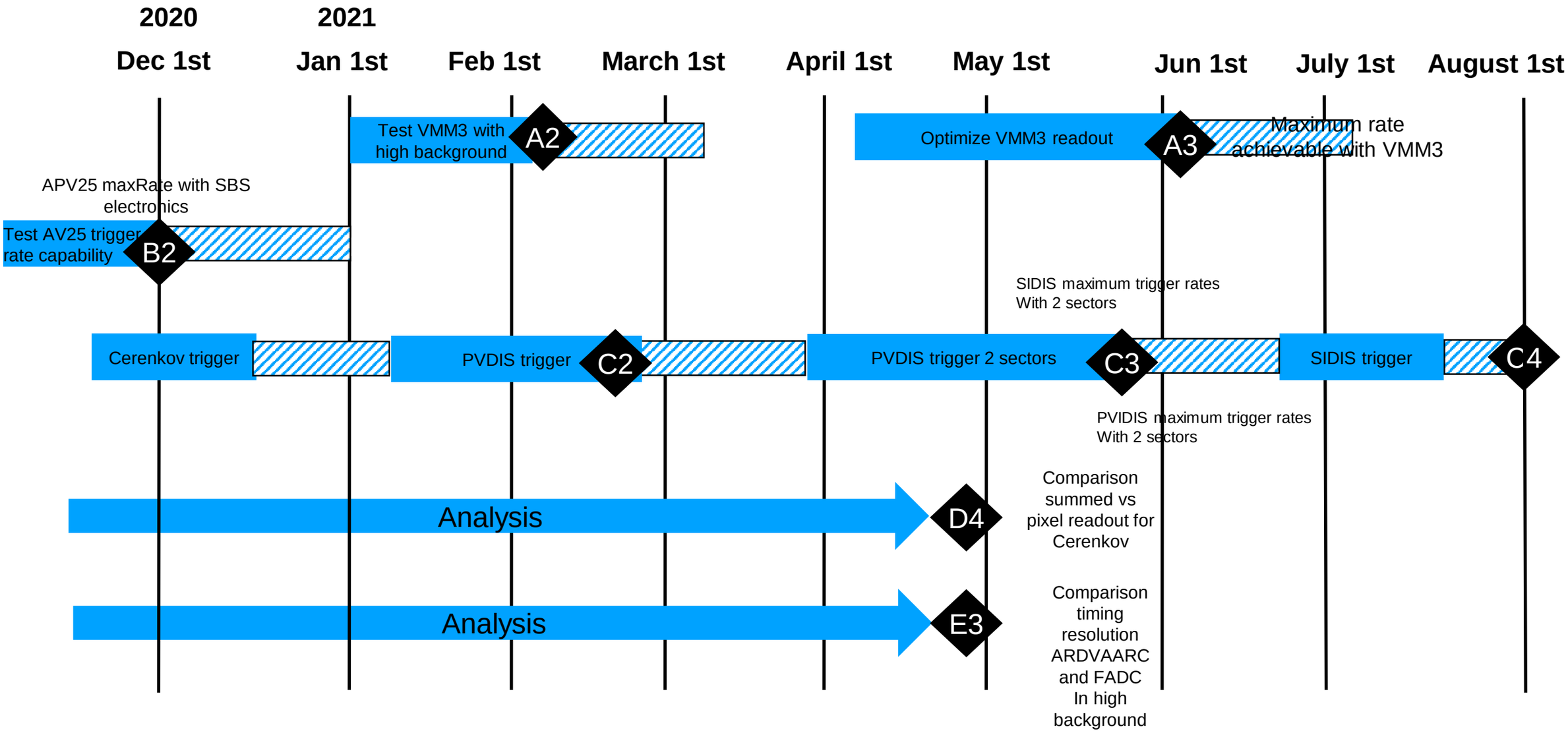
SIDIS event size APV25

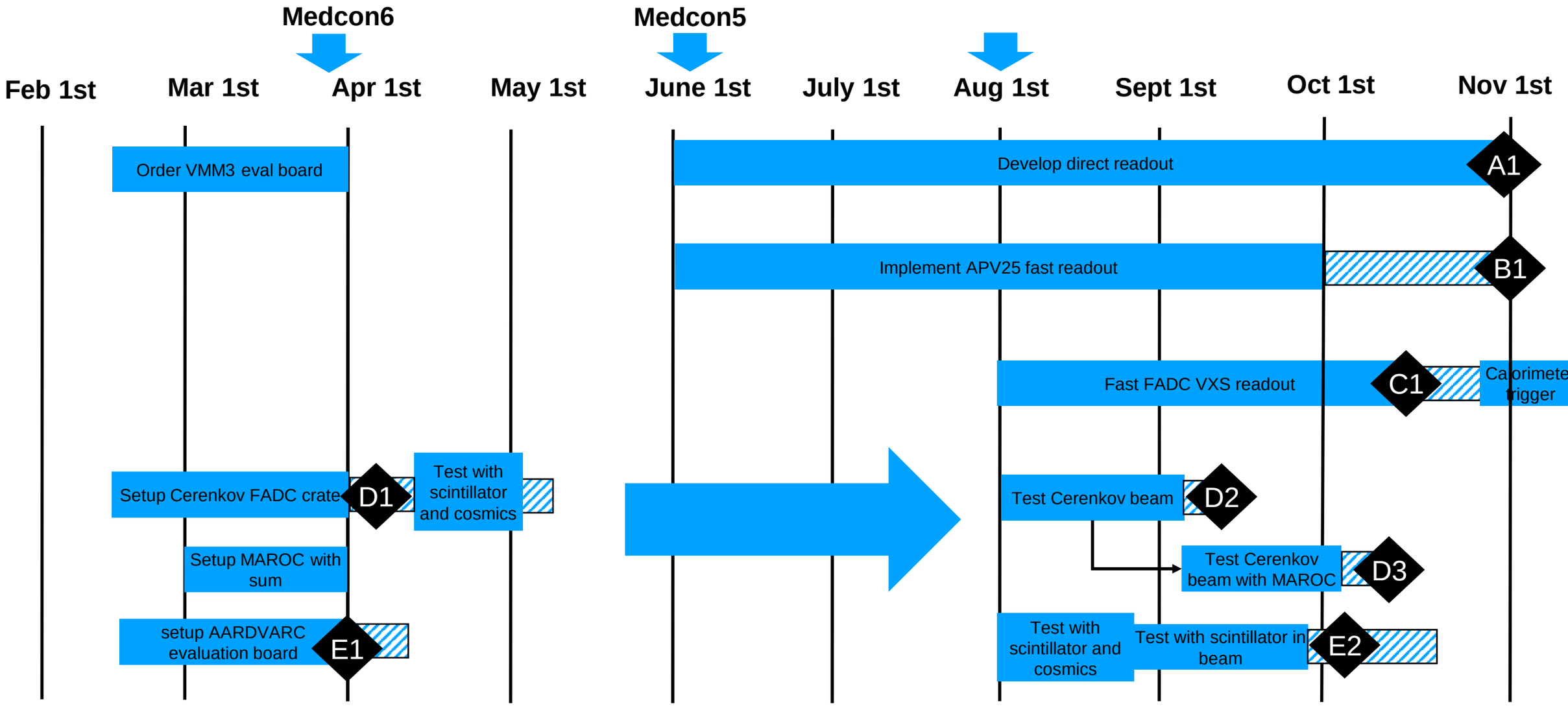
Occupancies with one sample readout by Weizhi , rates for 100 KHz

GEM	Occupancy	Number of strips	XY strips	Strips per chambers	MB/s
1	2.21	453	906	27180	245
2	8.78	510	1020	30600	1184
3	3.63	583	1166	34980	559.5
4	2.31	702	1404	42120	428.7
5	1.78	520	1040	31200	244.71
6	1.3	640	1280	38400	220
Total	20.01	3408	6816	204480	2901

GEM dominating 2.9 GB/s same requirement as PVDIS
Expect factor 2 reduction using VMM3


Medcon6
Medcon5
Feb 1st
Mar 1st
Apr 1st
May 1st
June 1st
July 1st
Aug 1st
Sept 1st
Oct 1st
Nov 1st
Order VMM3 eval board
Develop direct readout
A1
Testing with GEM on bench cosmics
Compton
Data taking
Implement APV25 fast readout
B1
Test APV25 trigger rate capability
Fast FADC VXS readout
C1
Calorimeter trigger
Cerenkov trigger
Setup Cerenkov FADC crate
D1
Test with scintillator and cosmics
Test Cerenkov beam
D2
Analysis
Setup MAROC with sum
Test Cerenkov beam with MAROC
D3
setup AARDVARC evaluation board
E1
Test with scintillator and cosmics
Test with scintillator in beam
E2
Analysis


2020
2021
Dec 1st
Jan 1st
Feb 1st
March 1st
April 1st
May 1st
Jun 1st
July 1st
August 1st
Test VMM3 with high background
A2
Optimize VMM3 readout
A3
Maximum rate achievable with VMM3
APV25 maxRate with SBS electronics
Test AV25 trigger rate capability
B2
SIDIS maximum trigger rates With 2 sectors
Cerenkov trigger
PVDIS trigger
C2
PVDIS trigger 2 sectors
C3
SIDIS trigger
C4
PVIDIS maximum trigger rates With 2 sectors
Analysis
D4
Comparison summed vs pixel readout for Cerenkov
Analysis
E3
Comparison timing resolution ARDVAARC and FADC In high background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Test Cerenkov beam
D2
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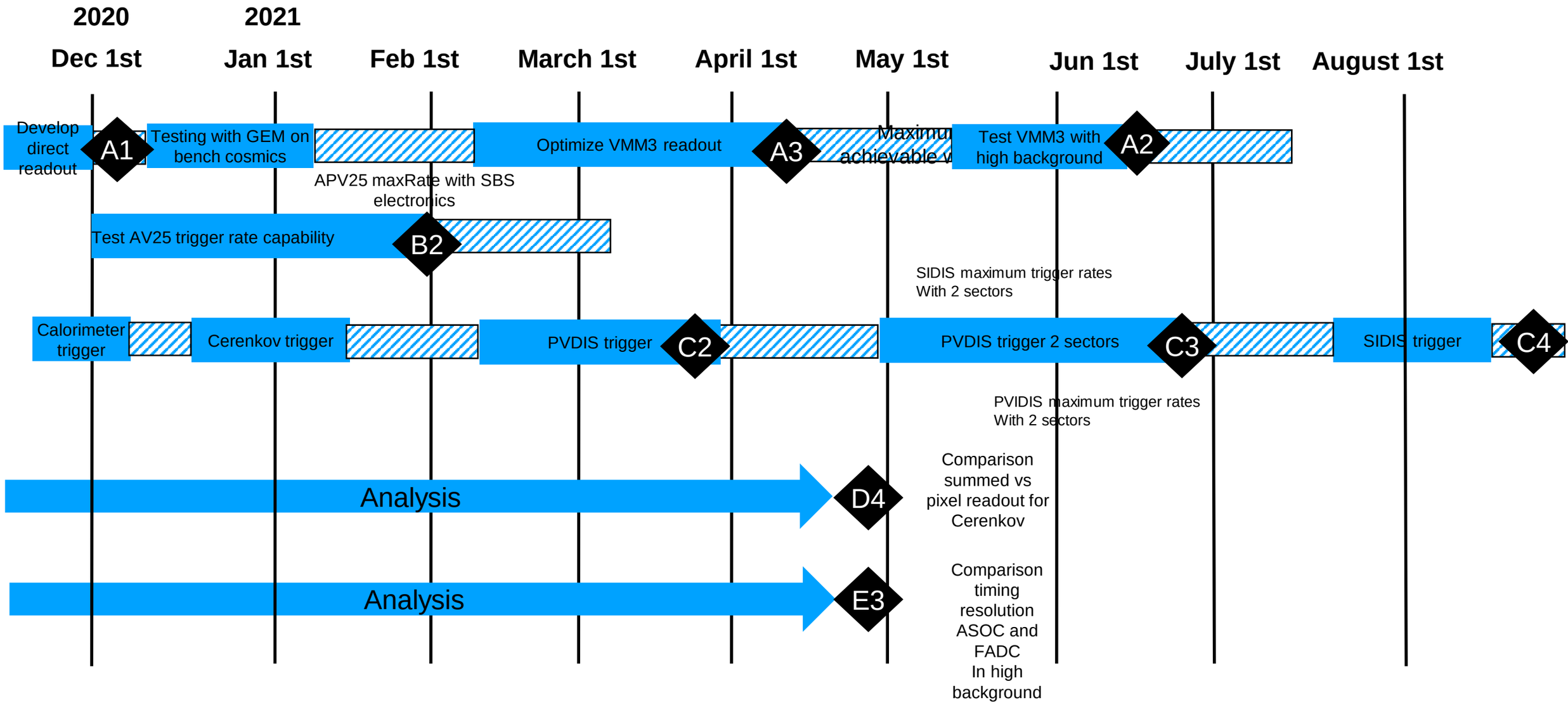
Test Cerenkov beam with MAROC
D3
setup AARDVARC evaluation board
E1
Test with scintillator and cosmics
Test with scintillator in beam
E2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SIDIS maximum trigger rates
With 2 sectors
Calorimeter trigger
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PVDIS trigger
C2
PVDIS trigger 2 sectors
C3
SIDIS trigger
C4
PVIDIS maximum trigger rates
With 2 sectors
Analysis
D4
Comparison summed vs pixel readout for Cerenkov
Analysis
E3
Comparison timing resolution ASOC and FADC In high background

Tasks and milestones

- A : VMM high rate test
  - A1 : procure evaluation board and test direct readout April 1st 2020 – delayed November 2020
  - A3 : develop prototype determine maximum trigger rate December 1st 2020 – ongoing
  - A2 : study behavior in high background February 15th 2021 – delayed June 15th 2021 on going
- B : APV rate capability
  - B1 : develop Fast Readout August 1st 2020 – delayed December 2020 (after FADC VXS readout)
  - B2 : demonstrate 100 KHz rate November 1st 2020 – delayed February 1st 2021
- C : FADC development (shift by 2 months)
  - C1 : Fast VXS readout August 15th 2020 – delayed October 15th 2020 – ongoing
  - C2 : Calorimeter trigger September 15th 2020 – delayed December 1st 2020
  - C3 : PVDIS trigger and test February 15th 2021 – delayed April 15th 2021
  - C4 : PVDIS trigger and test 2 sectors May 15th 2021 –delayed June 15th 2021
  - C5 : SIDIS trigger and test July 15th 2021 -

Tasks and milestones

- D : Gas Cerenkov Test support (shifted by 2 months due to COVID, beam resumed August 1st)
  - D1 : readout for Cerenkov test April 1st 2020
  - D2 : Cerenkov data with high background June 15th 2020 – delayed August 1st 2020 – on going
  - D3 : MAROC data with high background July 15th 2020 – delayed October 15th (
  - D4 : evaluation improvement with MAROC pixel readout April 15th 2021
- E : NALU ASOC Time of flight chip
  - E1 : install evaluation board April 1st 2020
  - E2 : sample high background data – delayed August 1st 2020 – October 15th 2020
  - E3 : timing resolution April 15th 2021

VMM test

- Ordered two test board 1500 $ x 2
- Evaluation board : can look at data with detector small subset of channels
  - Issue with external trigger but waiting for new firmware
  - Can check pedestal width
  - Signal to noise with detector with source and cosmics
  - Look at direct readout signals for 12 channels of detector
- Prototype development for data performance, test direct output with detector and X-ray source

VMM3 prototype board development (Ed)

FPGA for VMM Direct Readout

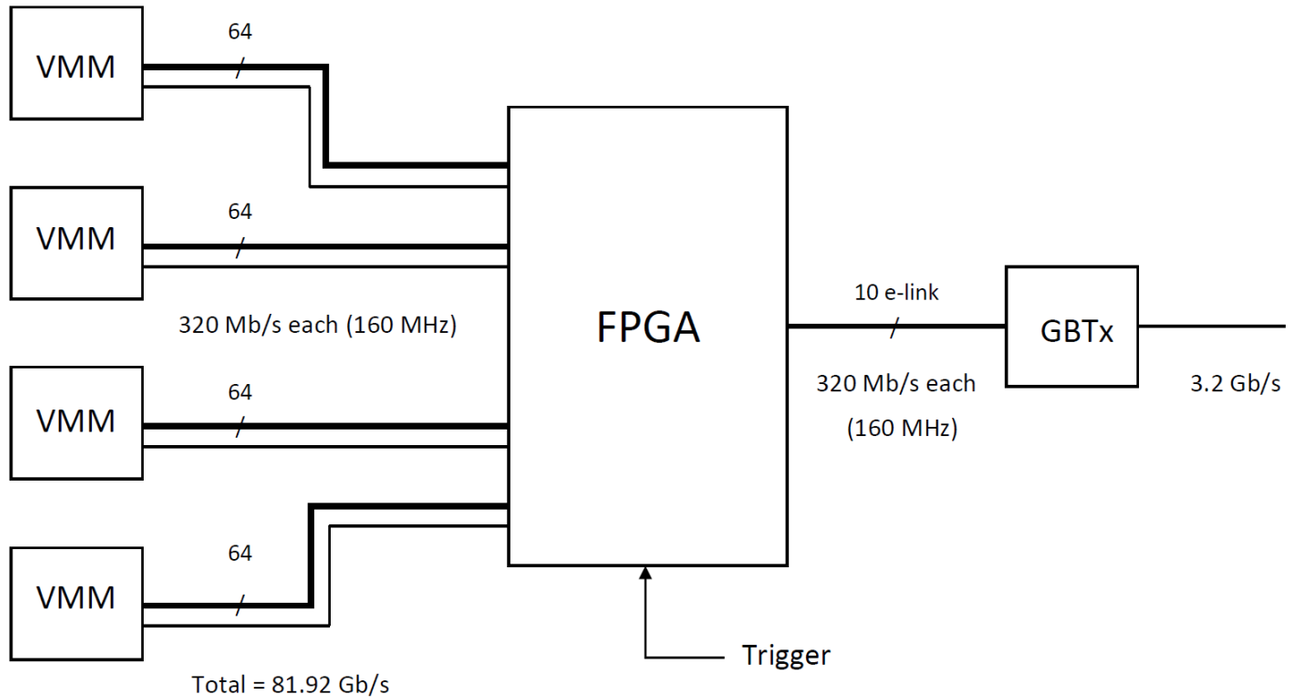
(E.J. 5/28/20)

Proposal

1 FPGA handles direct readout of 4 VMM chips

[64(channels/chip) + 1(clock/chip)] x 2(pins/signal) x 4(chips) = 520 pins (reasonable size, price FPGA)

1 GBTx data link for FPGA output data (10 e-links @ 320 Mb/s = 3.2 Gb/s)



VMM3 prototype board development (Ed)

Trigger rate (max) = (3200 Mb/s) / (4656 + w*r*3072 b)

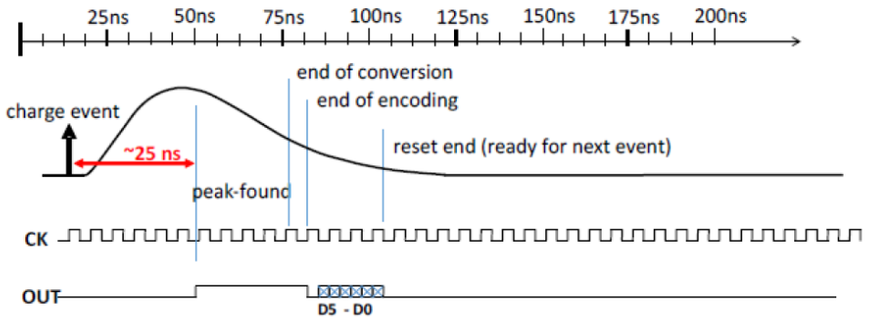
e.g. r = 10 MHz, w = 0.400 µs => Trigger rate (max) = 189 KHz

r = 15 MHz, w = 0.400 µs => Trigger rate (max) = 139 KHz

Or we can solve for the quantity w*r:

R = trigger rate (MHz)

w(µs)*r(MHz) = 1.04166 / R(MHz) - 1.51563



VMM 6-bit ADC Direct Output timing

VMM3 prototype board development (Ed)

- Direct readout with 15 MHz and 400 ns window gives 139 KHz trigger rate capability sufficient for PVDIS and SIDIS, most likely can reach 200 KHz if more segmentation and shorter window applicable

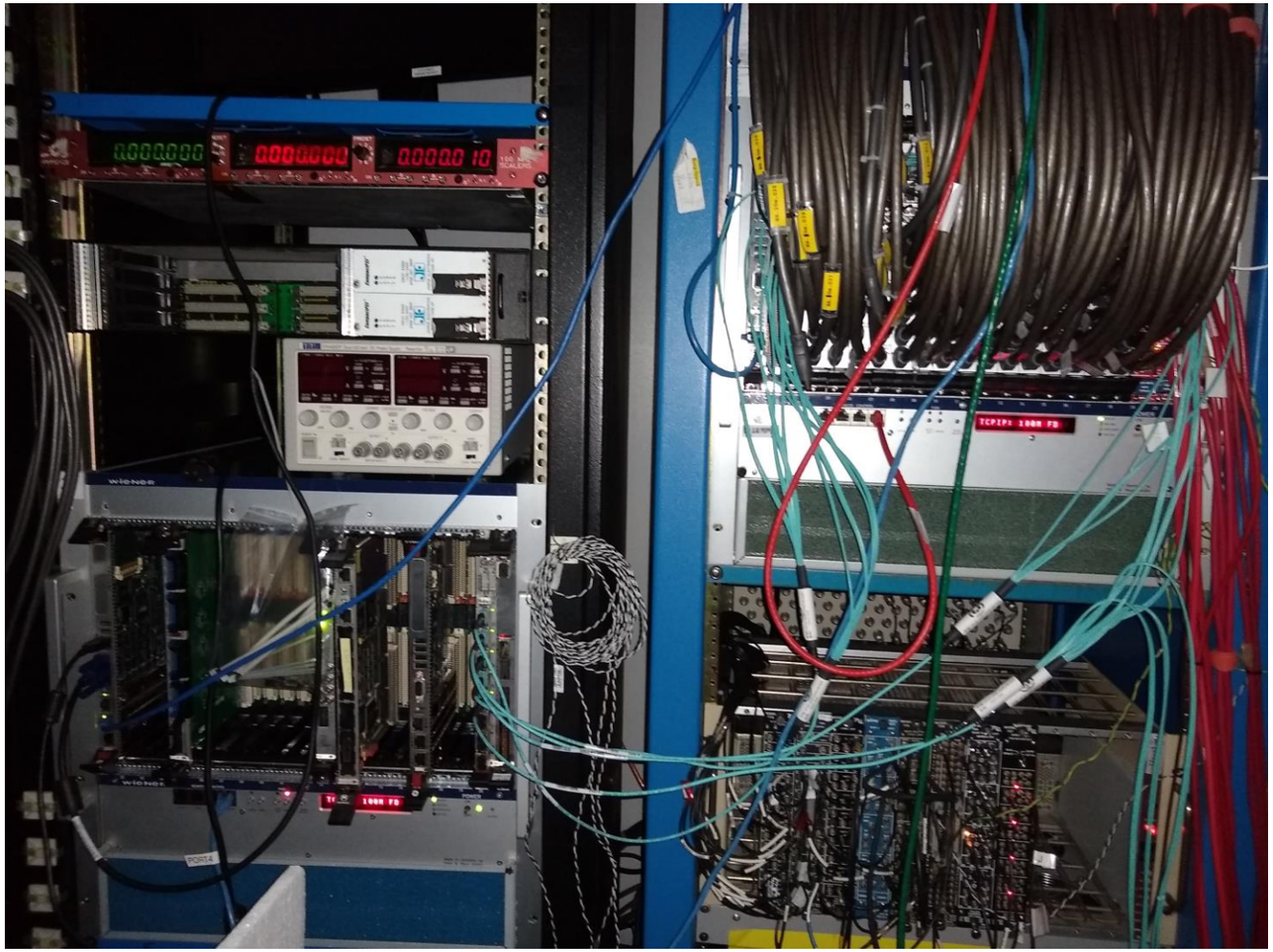
- Simulation of direct outputs by Jinlong ongoing

- Possible issues :
  - Low resolution ADC direct readout not good enough for high rate strips (PVDIS), instrument small angle with APV25 from SBS
  - Signal to noise worse when using 25 ns shaping time
  - Pile-up

APV25 tests

- Fiber and transceivers ordered for full scale test
- SSP new firmware up to 32 MPDs developed and being tested with 12 MPDs
- Will add more MPDs when access to lab
- High speed readout of MPDs with VTP will eliminate VME backplane bottleneck (200 MB / s vs 1.25 GB/s) in development
- Will test after MPD software updated and with more boards

APV25 tests



- Test setup using INFN clean room
- 1 VXS crate, 1 SSP , 18 MPDs, fully equipped chambers

- VTP readout development
- Optical to VXS adapter almost designed

- Delay in preRD due to noisy optical supply line, optical link speed had to be reduced from 2.5 Gbps to 1.25 Gbps

- Reduce data capability by a factor of 2

- Currently 10 kHz 5APV 6 samples 100% occupancy > 100 kHz with 8 APV ,1 sample at 30 % occupancy

FADC test stand

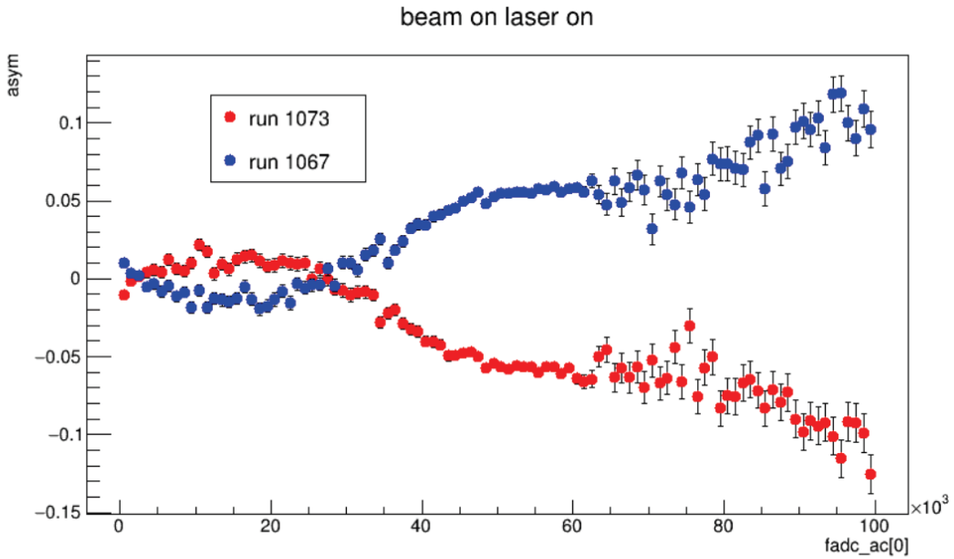
- Duplicate setup at Umass / agreed to do FADC tests for SoLID
- Working with Ben for calorimeter firmware developement

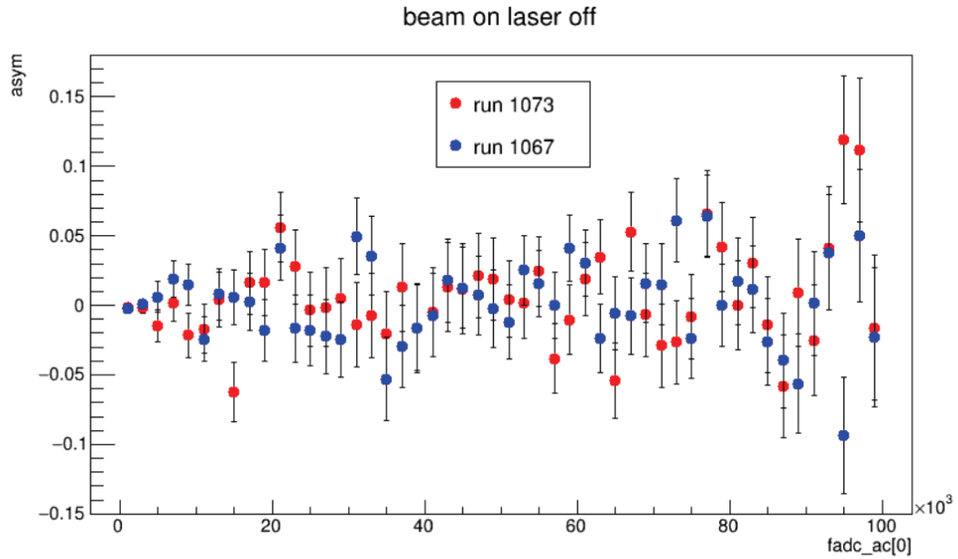
Preliminary results from Compton

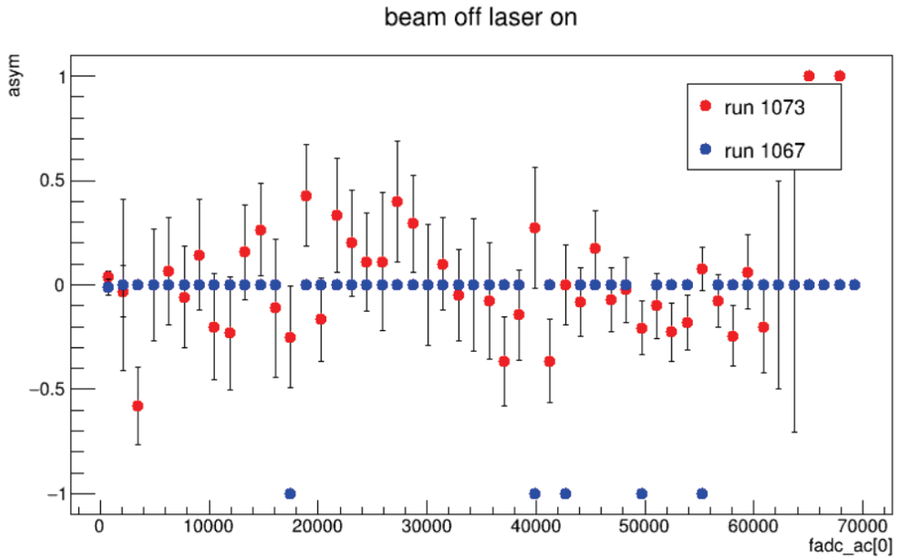
- FADC + VETROC + VTP (trigger module)
- Implemented delayed helicity readout
- Helicity scaler with VETROC and VTP for normalization (deadtime, power, position)
- Photon (and electron trigger)

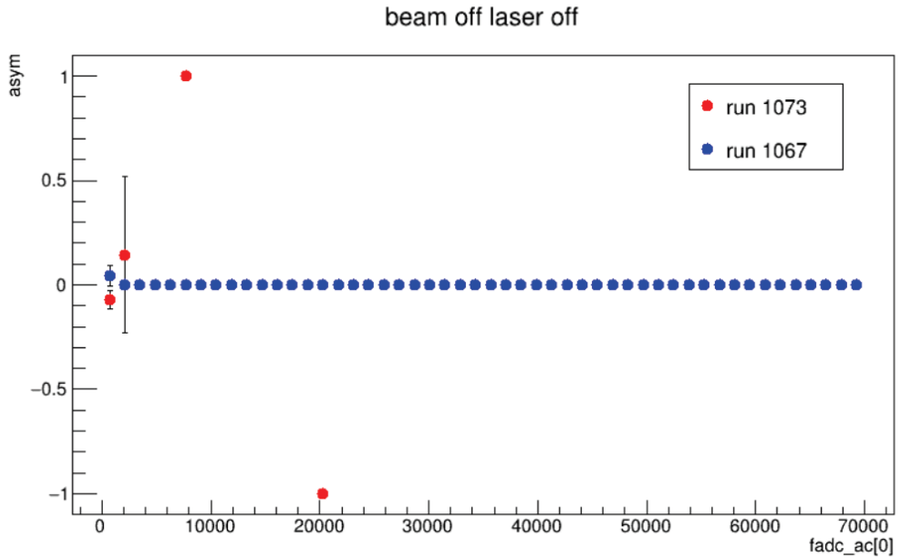
Preliminary results from Compton

- Rates up to 50 KHz with deadtime of about 10%
- Compton Asymmetry from Photon



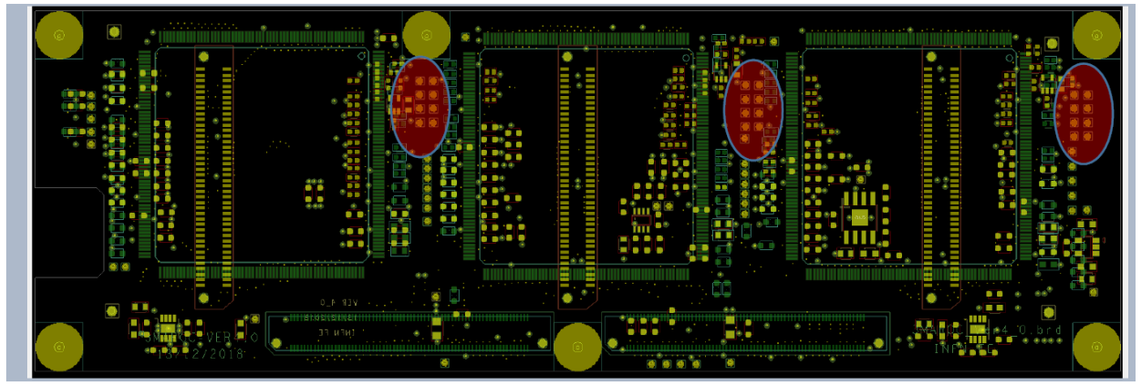


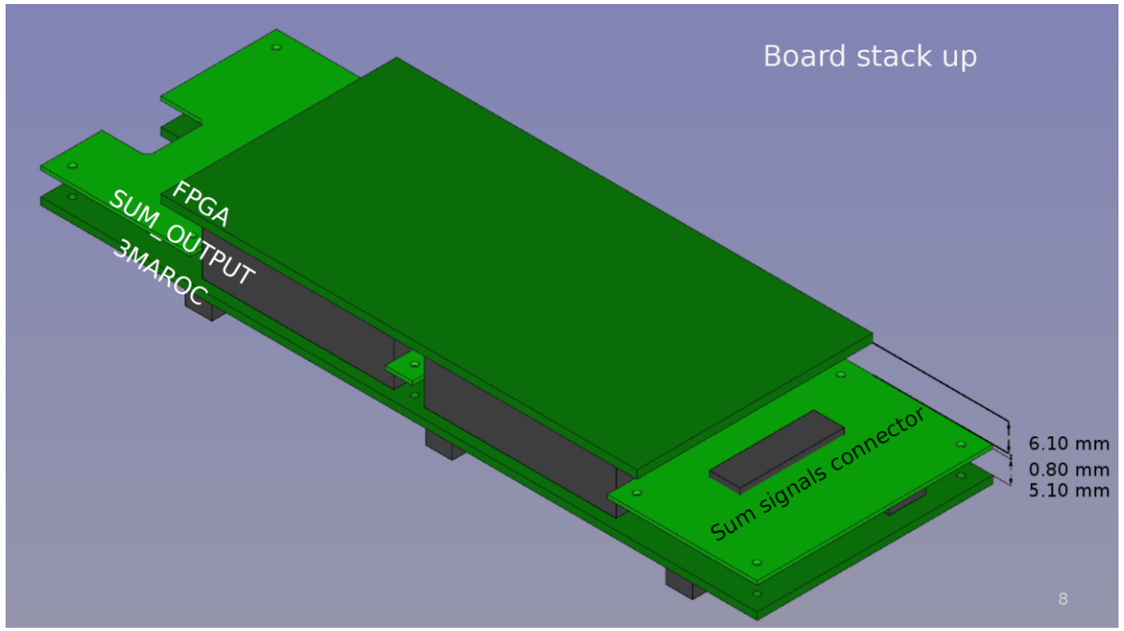


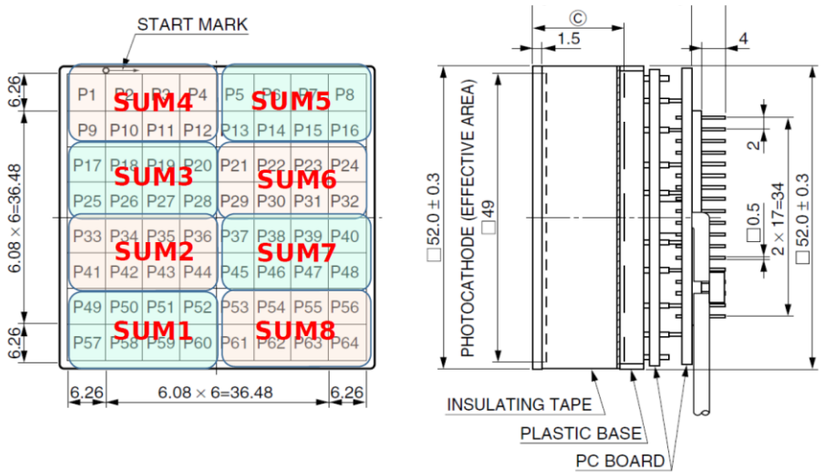


MAROC

- INFN Ferrara accepted to modify RICH board to have sum output
- Zhiwen and Bishnu are testing on bench





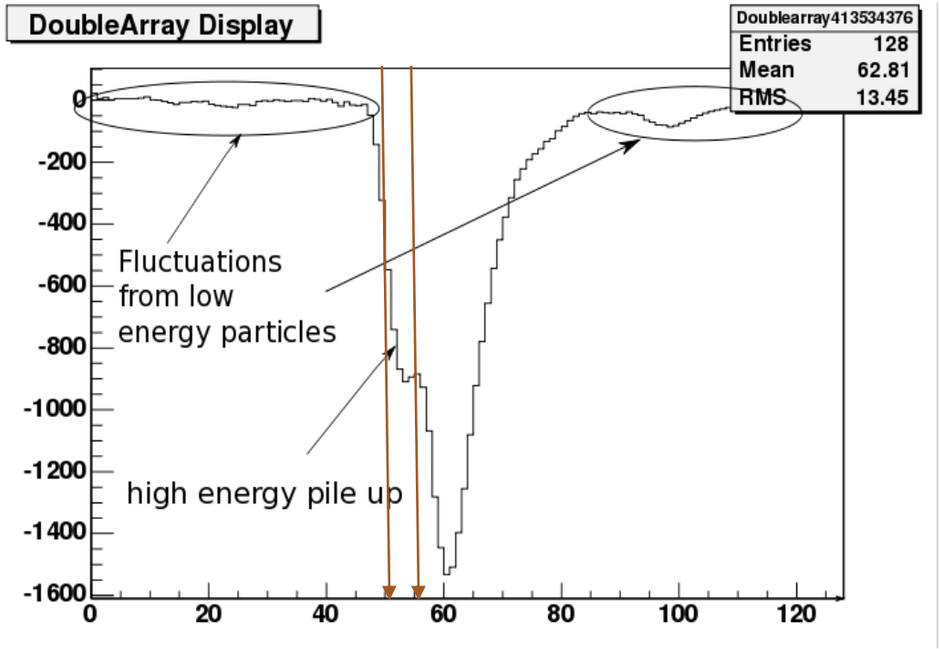


AARDVARC / ASOC

- Received Eval board ASOC
- Software installed and running but need test with pulser / detectors
- Test with PMTs on bench cosmics
- Test with Radioactive source

TOF ASOC chip

- Scintillator for TOF : want to evaluate effect of pile-up on timing resolution and compare FADC vs ASOC
- Testing ASOC instead of AARDVARC : more suitable for scintillator readout with PMTs
- Borrowed ASOC board from NALU
- Acquired Nexsys FPGA eval board
- Software installed and board running
- Tested with pulser but awaiting for spare
- Will test with radiactive source



SoLID preRD review

- In view of the uncertainties with the ongoing pandemic, including the possibility ofrenewed “shut-down”, prioritize test-areas so that they can be operated remotely andthat the data can be accessed remotely.
- Jefferson Lab is in the process of re-establishing beam for experiments in Hall-A andHall-C. The window to take data is upperbound by scheduling of activities for futureprojects and is likely to close by mid-September for a (very) extended period. The pre-R&D collaboration should prioritize taking data early on this window.
- The pre-R&D collaboration should clearly delineate DAQ tests that can be done onthe bench and those that (absolutely) need beam.
- Given that the VMM3 seems to be the preferred choice of readout chip, with theAPV25 being a backup and hybrids being undesirable, it is important to understand as early as possible within the pre-R&D effort the maximum rate capability of theVMM3 chip. The committee recommends, if possible, advancing the determination of the maximum rate capability of the VMM3 chip.

SoLID preRD review

- Most setup able to be accessed remotely with punctual access to lab
- Setup for bench test with pulser and radioactive source
- Setup of evaluation board will give preliminary results before science review for VMM3
- Hall network upgrade : will allow to test current data rate capability with APV readout during SBS

Conclusion

- Data rates
- PreRD timeline updated taking into account COVID delays
- PreRD ongoing with bench and source tests
  - VMM3 : prototype designed for 140 kHz trigger rate, will get preliminary results before science review and definitive results in summer
  - APV25 : should be able to handle SIDIS 100 KHz at 30 % occupancy
  - FADC : developments ongoing , 50 KHz 10% deadtime with slow readout, fast readout 10 faster
  - MAROC
  - ASOC
- PreRD review positive : comments taken into account

- Can test during SBS

- Should meet SoLID requirements with new developments