

Updates from the SoLID-GEM Chinese Collaboration

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for the SoLID-GEM Chinese Collaboration

University of Science and Technology of China

SoLID Collaboration Meeting

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JLab

SoLID-GEM Chinese Collaboration

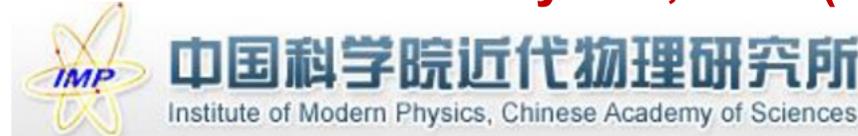
China Institute of Atomic Energy (CIAE)



Lanzhou University



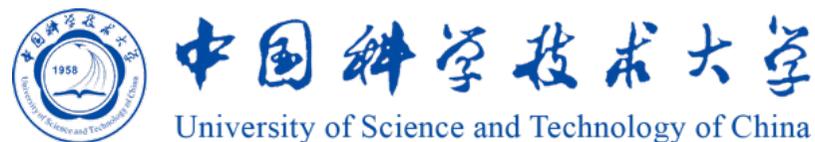
Institute of Modern Physics, CAS (IMP)



Tsinghua University



University of Science and Technology of China (USTC)

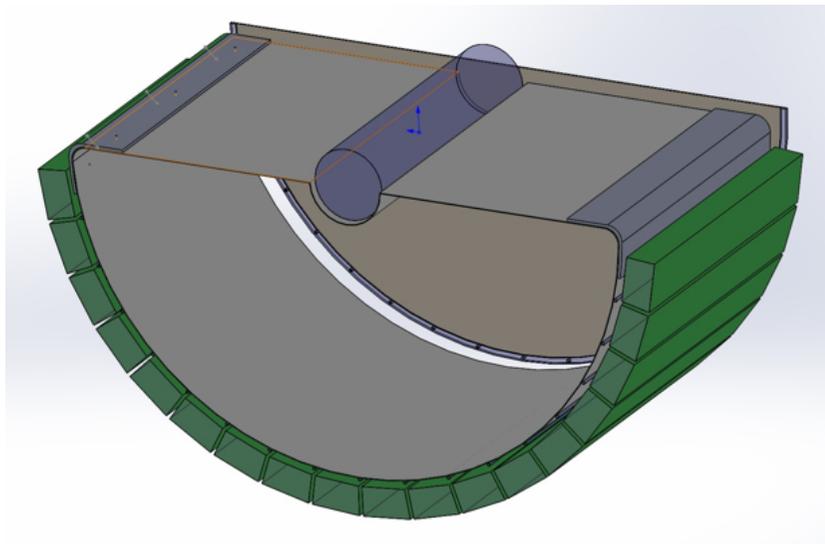


Lanzhou University



- Development of a TPC with GEM readout
 - The development of the GEM readout had been completed and was reported at the last collaboration meeting.
 - Development of the TPC is now ongoing

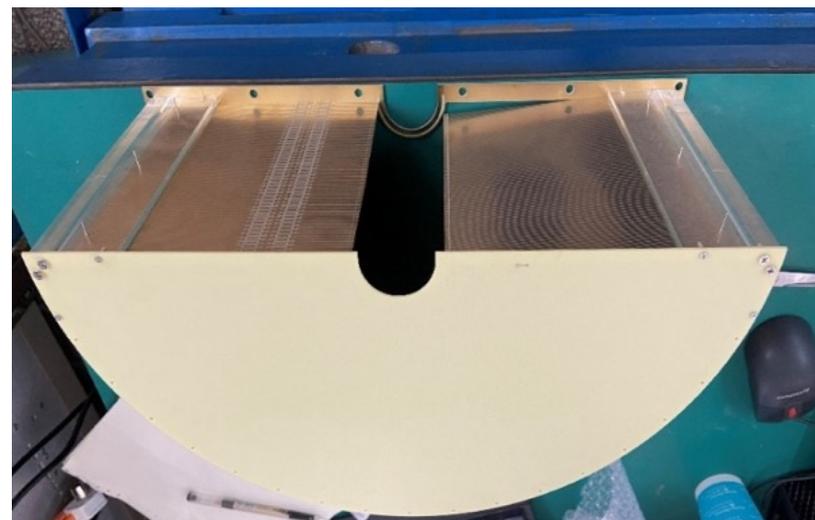
Design and Fabrication



Simulation of electric field uniformity

参考线	偏差最大值/%	偏差最小值/%
A	15.7	0.07
B	2.19	0.067
C	5.09	0.17

The TPC prototype in the making



APV25 Electronic and DAQ System Developed by CIAE

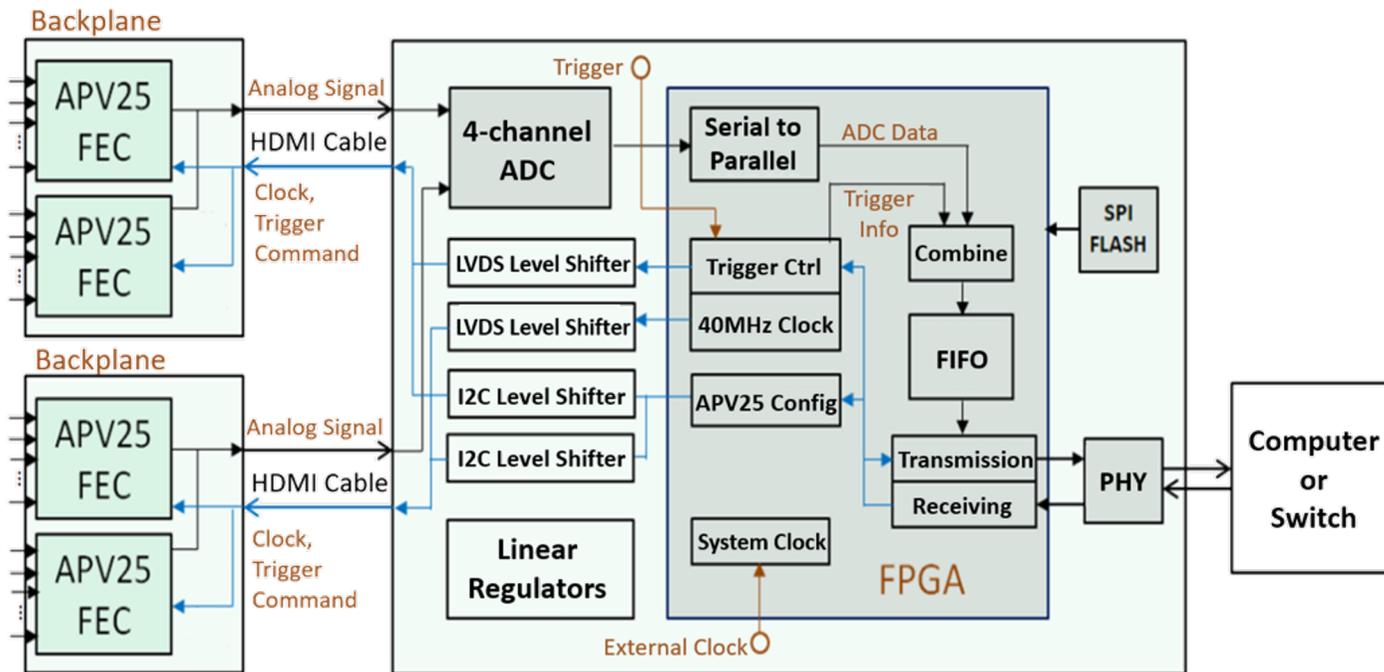
The APV25 Electronic and DAQ System uses *APV25* electronics front-end card, *APVDS* electronic digital system and newly developed data acquisition software *GeoAPV*. Both *APVDS* and *GeoAPV* are developed by CIAE.

Testing in the configuration of 1,024 channels, internal trigger mode while monitoring the sampling waveform, the transmission rate can stably maintain 715 Mbps



Development of APVDS Electronic Digital System

- **ADC (ADS5242) +FPGA (Spartan 6)**
- In 128-channel configuration, the system trigger rate can reach **285 kHz** - the upper limit of APV25

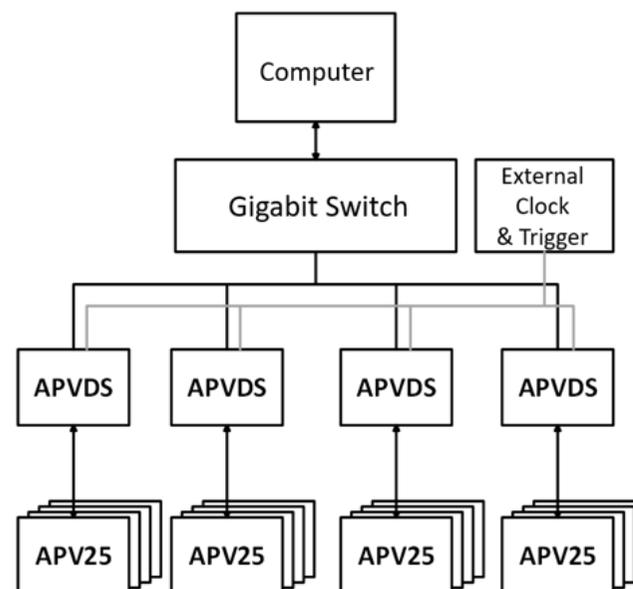


Hardware Integration

Each APVDS digitalization board is capable of processing 512 channels' input.

The whole system uses multiple APVDS board to expand the capacity of the system.

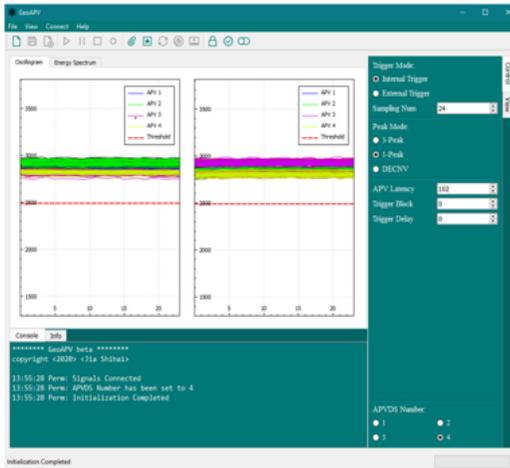
(4 APVDS boards designed; 2 APVDS boards tested)



Every APVDS has an independent IP address and shares a common external clock signal from APVTTTS board.

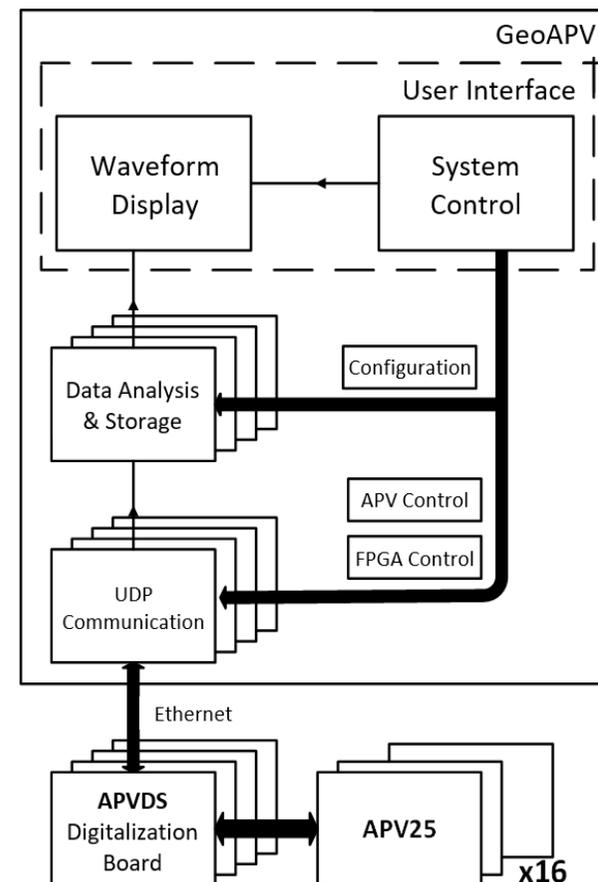
Data Acquisition Software

GeoAPV is developed for APV25 front-end card and APVDS board



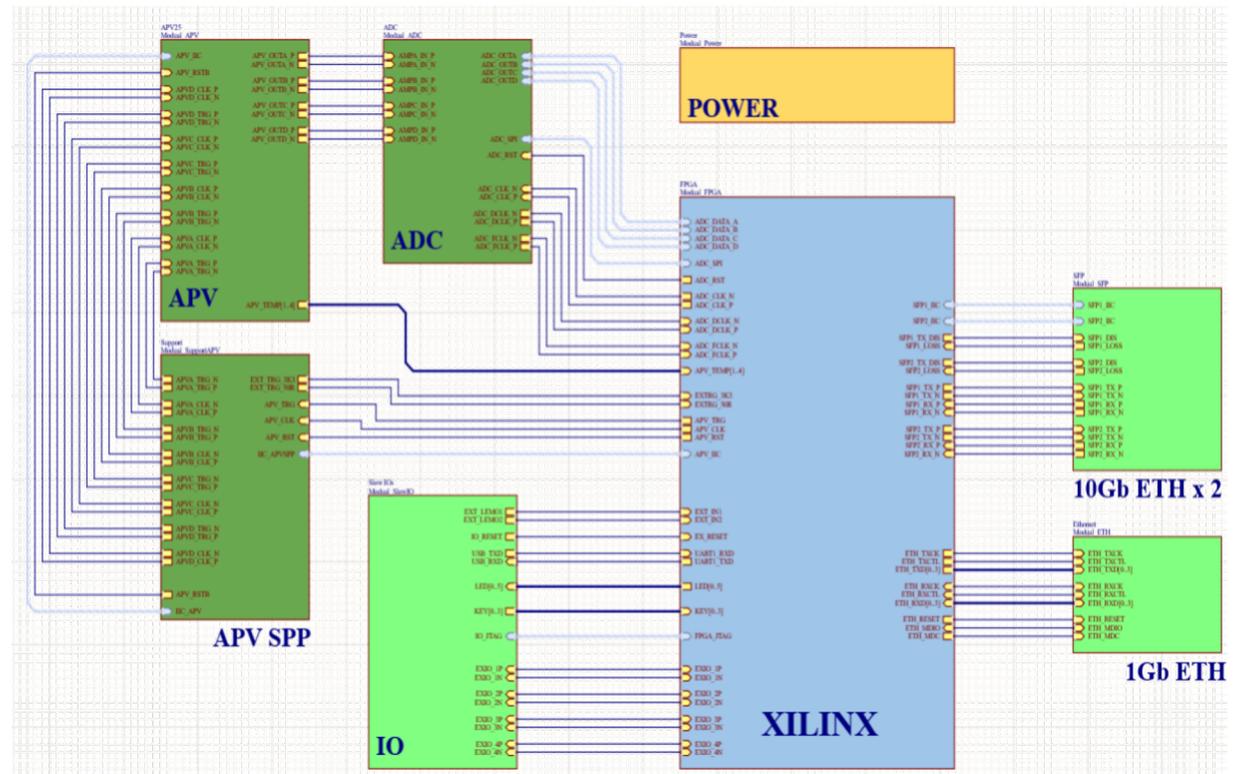
Mainly improved in usability, scalability, and modularity.

It performs intuitive operations, monitors input waveform in real time, and will integrate more functions in the future

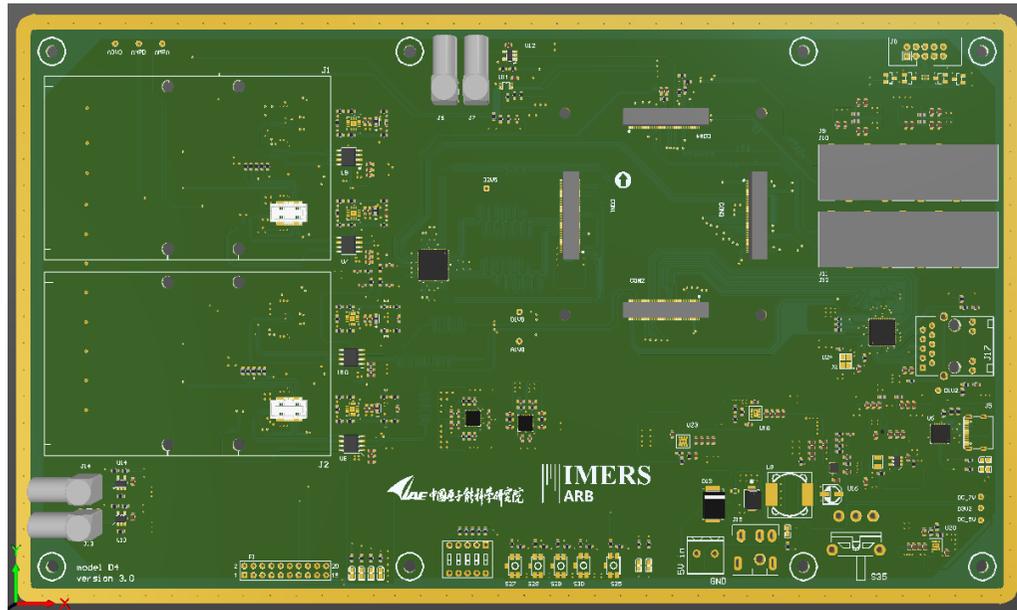


New Design of APVDS Board

- Single 1 Gbps Ethernet gets updated to Dual 10 Gbps Ethernet Ports
- Artix-7 FPGA Chip Provides 188% More Logic Cells
- ADC Analog Bandwidth Improved from 300 MHz to 540 MHz



APVDS v3.0



Version 3.0 focuses on improving the ethernet speed rate, system stability, and versatility. With the help of our new PCB design and choosing state-of-the-art components, we finished the design of the system which is capable of processing up to 4,096 channels of detector signal.

- 8-layered FR-4 PCB
- Quad Onboard APV25 Connectors
- UART, 1 Gbps Ethernet and 20-pin Extension Port

The whole new APVDS is being manufactured, and the first prototype will be tested by the end of 2020.



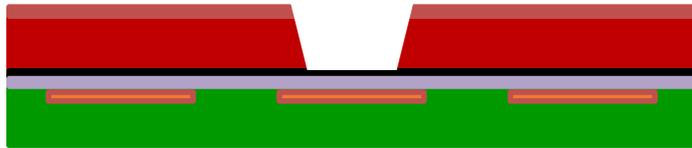
中国科学技术大学

University of Science and Technology of China

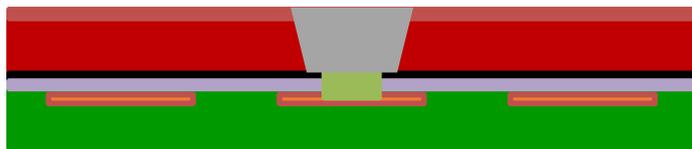
- Cosmic-ray test of high-rate uRWELL detectors

A novel idea to realize high-rate μ RWELL

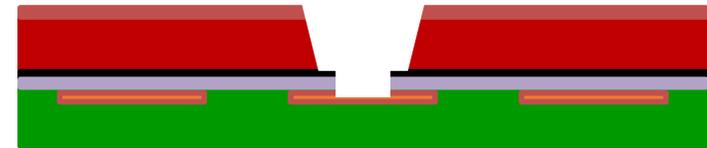
PEDF: Pattern , etch , drill & fill



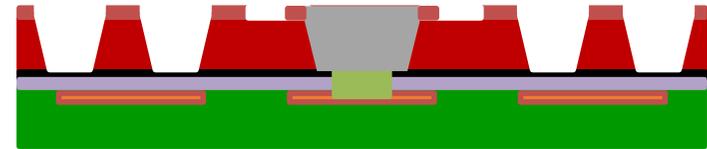
Step1: Copper & APICAL etching to make a big hole with DLC on bottom.



Step3: Connect the DLC to readout pad with silver glue.



Step2: Drill a small hole and expose the copper of the readout pad to the air.

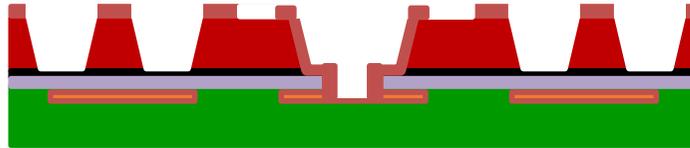


Step4: Make μ RWELL structure and remove the copper around silver glue.

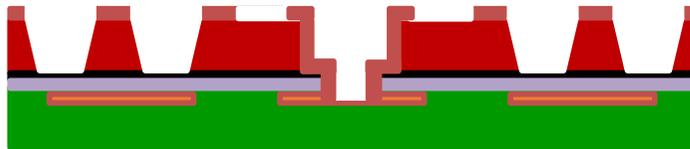
Advantages:

1. No copper-coated DLC needed, so better resistivity control
2. No alignment issue even for large area
3. Larger contact area between DLC and silver glue resulting in better contact between the two.

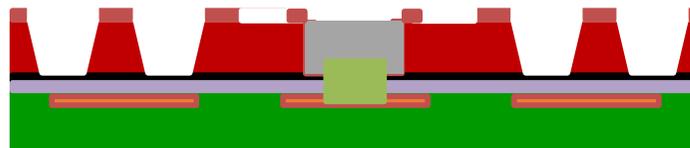
Derivatives: PEDP, DEF, DEP μ RWELL



PEDP: Pattern , etch , drill & plate



DEP: Drill , etch & plate



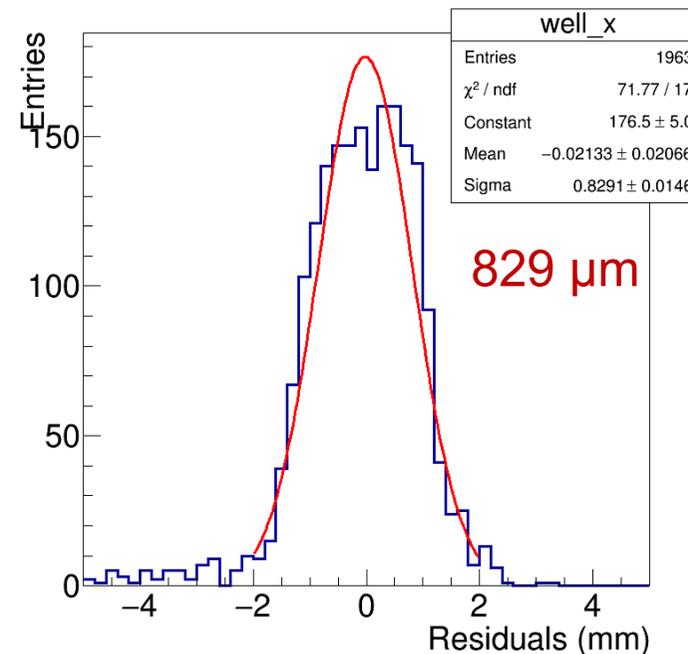
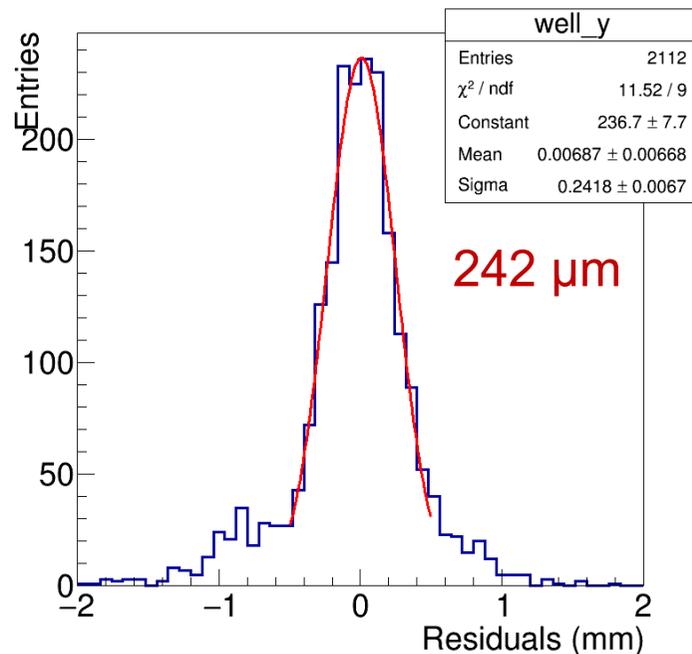
DEF: Drill , Etch & fill

Small-size μ RWELL PCB prototypes for the four high-rate options (PEDF , DEF , PDEP , DEP) have been produced at CERN and sent to USTC.

Thanks to Rui De Oliveira and CERN PCB workshop for technical support.

Position resolution

- A cosmic-ray telescope was set up using three GEM detectors with APV25 readout.
- The position resolution of the uRWELL prototype was measured with cosmic rays

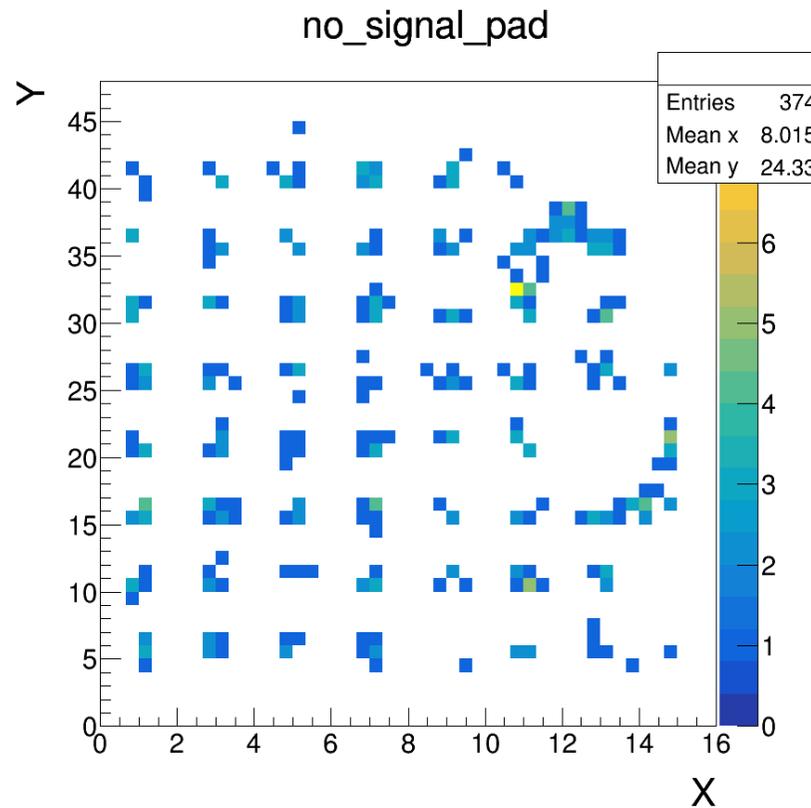


Incident angle < 5.7 degree

Position resolution: 240 μm (1mm pitch) and 830 μm (3mm pitch)

Detection efficiency

Detection efficiency: 95.2% (7858/8251)



Much of the inefficiency comes from the grounding holes (> 2%)