SoLID DAQ

SoLID collaboration meeting

January 6th 2021

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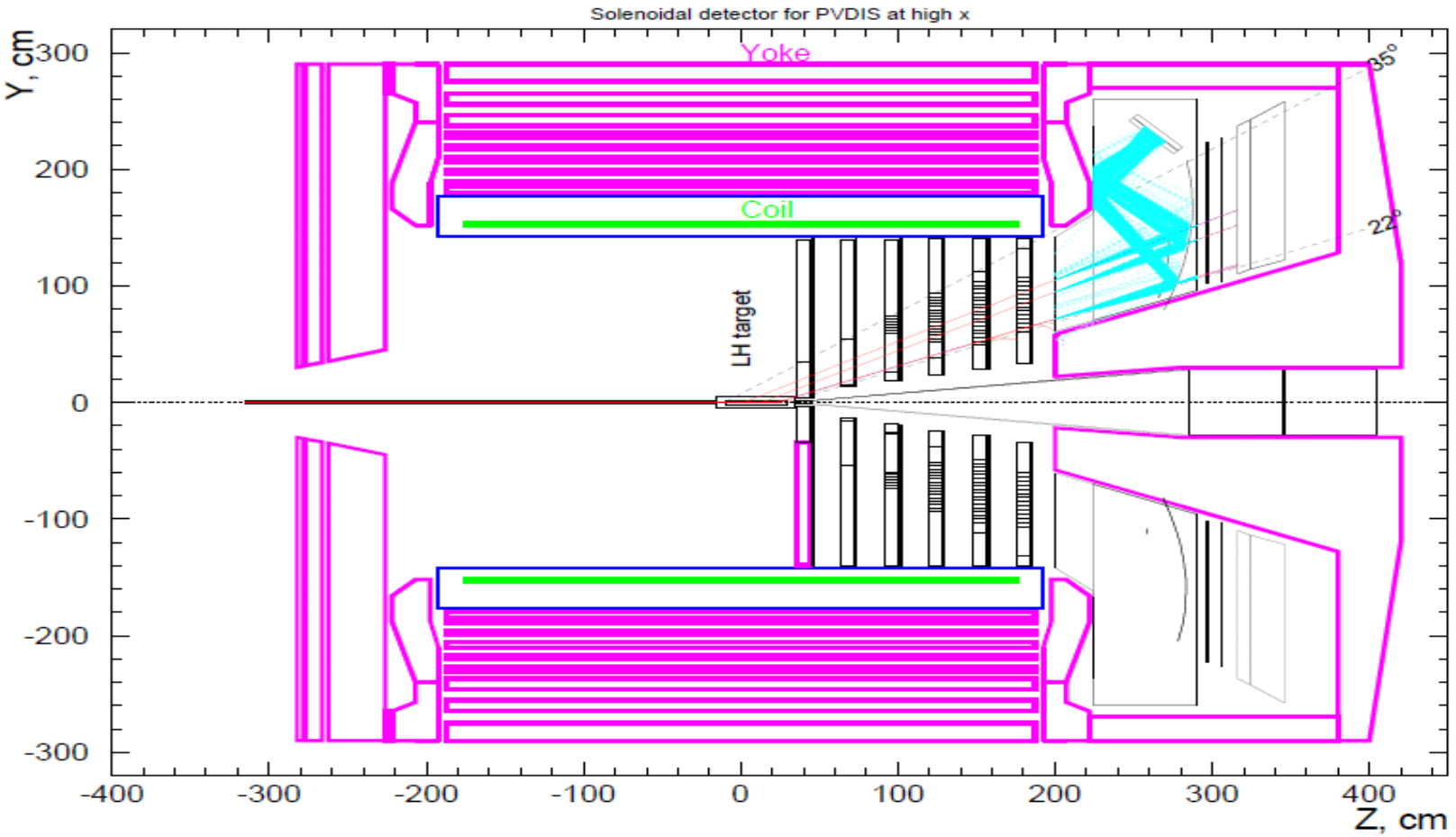
Outline

- DAQ overview
- DAQ requirements
- Data rates
- preR&D updates
  - VMM
  - APV
  - FADC
  - Cerenkov
  - TOF
- Conclusion

SoLID requirements

Experiments	PVDIS	SIDIS-^{3}He	SIDIS-Proton	J/ψ
Reaction channel	$p(\vec{e},e')X$	$(e,e'\pi^{\pm})$	$(e,e'\pi^{\pm})$	$e+p \rightarrow e'+J/\Psi(e^-,e^+)+p$
Approved number of days	169	125	120	60
Target	LH_2/LD_2	^{3}He	NH_3	LH_2
Unpolarized luminosity ($cm^{-2}s^{-1}$)	$0.5\times10^{39}/1.3\times10^{39}$	$\sim 10^{37}$	$\sim 10^{36}$	$\sim 10^{37}$
Momentum coverage (GeV/c)	2.3-5.0	0.8-7.0	0.8-7.0	0.6-7.0
Momentum resolution	~2%	~2%	~2%	~2%
Polar angle coverage (degrees)	22-35	8-24	8-24	8-24
Polar angle resolution	1 mr	0.6 mr	0.6 mr	0.6 mr
Azimuthal angle resolution	-	5 mr	5 mr	5 mr
Trigger type	Single e^-	Coincidence $e^-+\pi^{\pm}$	Coincidence $e^-+\pi^{\pm}$	Triple coincidence $e^-e^-e^+$
Expected DAQ rates	<20 kHz $\times$ 30	<100 kHz	<100 kHz	<30 kHz 100 kHz?
Backgrounds	Negative pions, photons	($e,\pi^-\pi^{\pm}$) ($e,e'K^{\pm}$)	($e,\pi^-\pi^{\pm}$) ($e,e'K^{\pm}$)	BH process Random coincidence
Major requirements	Radiation hardness 0.4% Polarimetry π^- contamination Q^2 calibration	Radiation hardness Detector resolution Kaon contamination DAQ	Shielding of *sheet-of-flame* Target spin flip Kaon contamination	Radiation hardness Detector resolution

Detector layout and trigger for PVDIS



Trigger

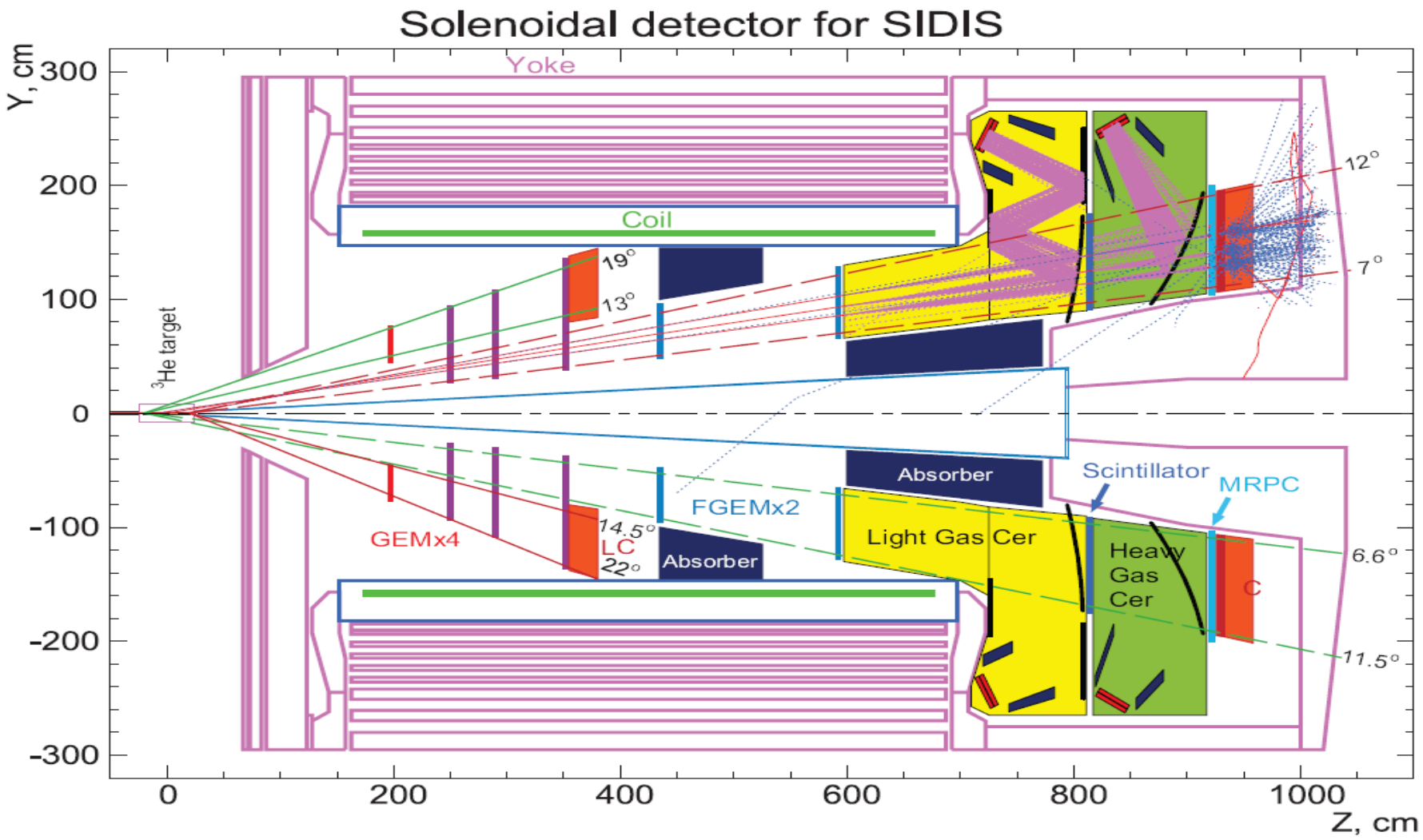
Calorimeter
+
Cerenkov

200 to 500 KHz of electrons

30 individual sectors

Max 17 KHz/sector

Detector layout and trigger for SIDIS



Trigger

Calorimeter
+
Cerenkov
+
SPD

30 sectors
Combined
in
10 regions of interests
Max rate 200 KHz

Baseline 60 KHz
coincidence e- pion

Updated data rates using VMM data format and occupancies

- 6 bit ADC and up to 400 ns time window (160 MHz clock = ~65 clock cycles)
- Add channel and chip ID
- Timestamp

VMM event format		Time stamp 250 MHz		VMM ID	VMM channel	Fine time	Amplitude
bit		48		14	4	7	7

- 8 bytes per channel

New Data rates PVDIS

PVDIS	30000 kHz						
		Total strips	Occupancy %	strips fired	event size bytes (time + amplitude)		data rate (MB/s)
1		34740	16.2	5627.88	22513.52		675.4056
2		41280	8.3	3426.24	13706.96		411.2088
3		41280	7.1	2930.88	11725.52		351.7656
4		68400	2.7	1846.8	7389.2		221.676
5		70560	2.7	1905.12	7622.48		228.6744
		256260	37	15736.92	62957.68	GEM rate	1888.7304
						FADC	176
						Total	2064.7304

New Data rates SIDIS

SIDIS He3	200000 KHz						
		Total strips	Occupancy %	strips fired	event size bytes (time + amplitude)		data rate (MB/s)
1		27120	1.8	488.16	1954.64		390.928
2		30540	5.5	1679.7	6720.8		1344.16
3		34920	2.5	873	3494		698.8
4		42060	1.6	672.96	2693.84		538.768
5		31140	1.6	498.24	1994.96		398.992
6		38340	1.2	460.08	1842.32		368.464
		204120	14.2	4212.06	16858.24		3371.648
						FADC	300
						Total	3671.648

1.8 GB/s at 100 KHz

New Data rates J/Psi

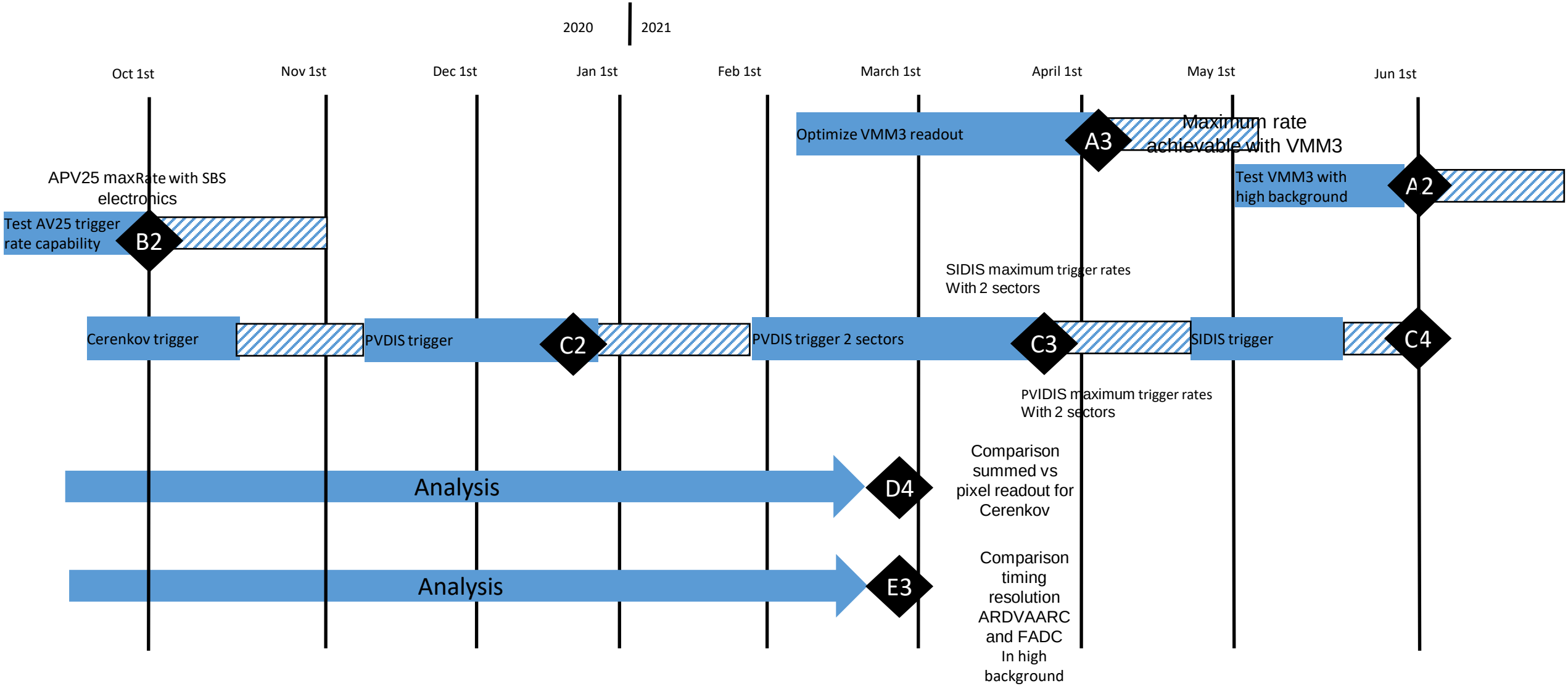
JPsi	100000						
		Total strips	Occupancy %	strips fired	event size bytes (time + amplitude)		data rate (MB/s)
1		27120	5.4	1464.48	5859.92		585.992
2		30540	9.7	2962.38	11851.52		1185.152
3		34920	6.1	2130.12	8522.48		852.248
4		42060	4.8	2018.88	8077.52		807.752
5		31140	4.3	1339.02	5358.08		535.808
6		38340	3.3	1265.22	5062.88		506.288
		204120	33.6	9914.88	39669.52		3966.952
						FADC	300
						Total	4266.952

Similar data rates as APV25 for Jpsi, slightly lower rate for PVDIS and SIDIS

DAQ preRD milestones

- VMM
  - Milestone A1 April 1st 2020 : nish development of VMM3 direct readout
  - Milestone A2 November 1st 2020 : VMM3 will be tested with detector in high background using X-ray and radioactive sources to study behavior of the VMM3 and ensure signal can be well separated from background.
  - Milestone A3 March 1st 2021 : after optimization of the readout, we will determine what is maximum rate achievable for the VMM3 GEM readout
- APV25
  - Milestone B1 June 1st 2020 : while the intrinsic specs of thechip should allow 200 kHz trigger rate using one sample, some development is needed to determine if this is achievable with the existing electronics from SBS. It involves enabling the APV25 buffering and optimizing the data transfer of the readout
  - Milestone B2 October 1st 2020 : Determine rate limits of APV25 trigger rate and same testing in high
  - occupancy environment
- FADC DAQ
  - Milestone C1 April 1st 2020 : develop fast FADC readout (through VXS) to eliminate VME bus data bottle neck
  - Milestone C2 October 1st 2020 : after the full trigger for PVDIS is completed, maximum trigger rate of the setup will be studied for one single sector
  - Milestone C3 Feb 1st 2021 : communication between two sectors will be implemented maximum trigger rate of the setup will then be studied this will be close to final PVDIS setup
  - Milestone C4 March 15th 2021 : SIDIS will be implemented and maximum trigger rate will be determined
- Cherenkov readout
  - milestone D1 February 15th 2020 : Setup FADC crate for Cerenkov sum testing
  - milestone D2 April 15th 2020 : record beam data using total sum and FADC
  - milestone D3 : Test Cherenkov with MAROC in high background sample with beam.
  - milestone D4 February 15th 2020 : complete analysis conclude if pixel readout is required.
- Time of flight
  - Milestone E1 February 1st 2020 : acquire and setup AARDVARC evaluation board
  - Milestone E2 May 15th 2020 : acquire data of scintillator with beam
  - Milestone E3 February 15th 2021 : complete analysis and determine achieved timing resolution with AARDVARC and compare to FADC resolution

preRD schedule



VMM test

- 2 test board :
  - 1 testing with detector to take cosmics : need work on grounding and shielding
  - 1 development of direct readout
- Prototype
  - Design close to complete
  - VMM chips ordered (estimate delivery end of February)
  - Firmware is scaling to 128 channels from 17 channels from eval board
- Test VMM with real GEM (check signal to noise) 3 months

VMM3 prototype board development (Ed)

FPGA for VMM Direct Readout

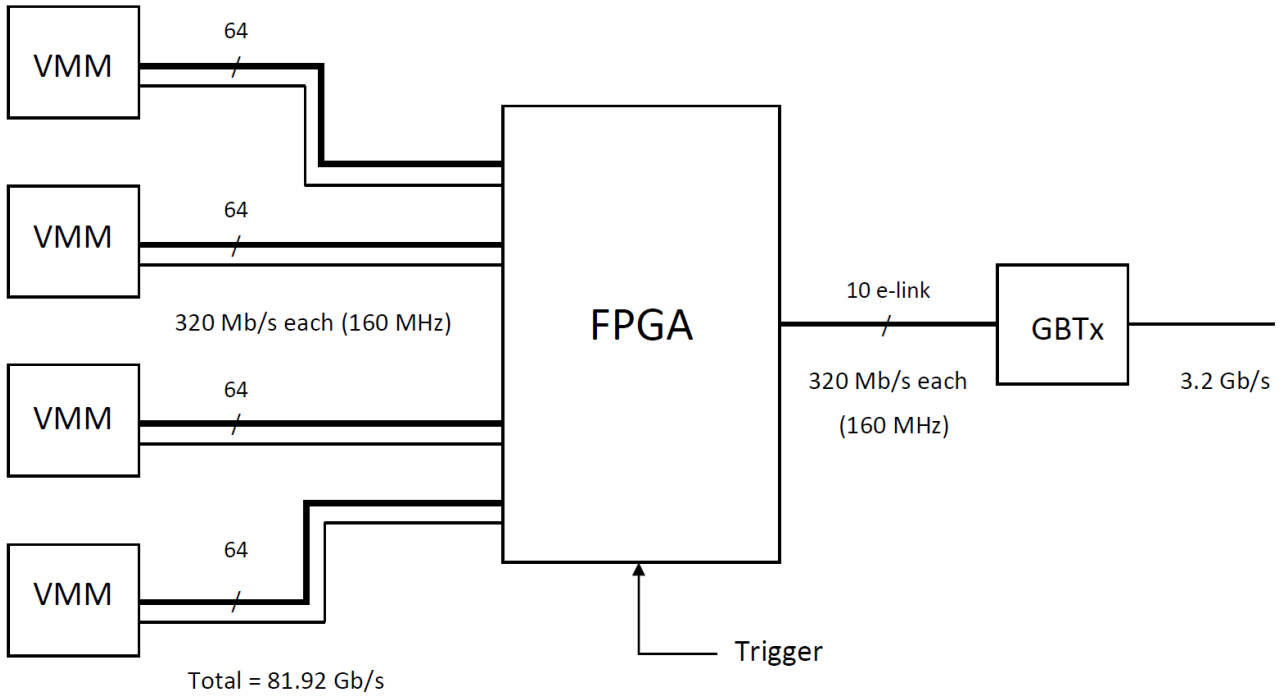
(E.J. 5/28/20)

Proposal

1 FPGA handles direct readout of 4 VMM chips

[64(channels/chip) + 1(clock/chip)] x 2(pins/signal) x 4(chips) = 520 pins (reasonable size, price FPGA)

1 GBTx data link for FPGA output data (10 e-links @ 320 Mb/s = 3.2 Gb/s)



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VMM3 prototype board development (Ed)

Trigger rate (max) = (3200 Mb/s) / (4656 + w*r*3072 b)

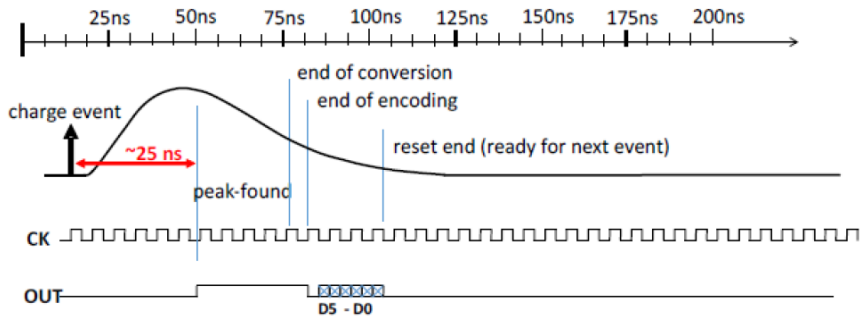
e.g. r = 10 MHz, w = 0.400 µs => Trigger rate (max) = 189 KHz

r = 15 MHz, w = 0.400 µs => Trigger rate (max) = 139 KHz

Or we can solve for the quantity w*r:

R = trigger rate (MHz)

w(µs)*r(MHz) = 1.04166 / R(MHz) - 1.51563



VMM 6-bit ADC Direct Output timing

VMM3 prototype board development (Ed)

- Direct readout with 15 MHz and 400 ns window gives 139 KHz trigger rate capability sufficient for PVDIS and SIDIS, most likely can reach 200 KHz if more segmentation and shorter window applicable

- Simulation of direct outputs by Jinlong ongoing

- Possible issues :
  - Low resolution ADC direct readout not good enough for high rate strips (PVDIS), instrument small angle with APV25 from SBS

APV25 tests

- Fiber and transceivers ordered for full scale test
- SSP new firmware up to 32 MPDs developed and being tested with 12 MPDs
- Will add more MPDs when access to lab
- High speed readout of MPDs with VTP will eliminate VME backplane bottleneck (200 MB / s vs 1.25 GB/s) in development (~ 2 months to complete)

APV25

- Tested ：Initial testing has with 6 samples per trigger has achieved ~10kHz trigger rate using 1 SSP with 1 MPD that had 5 APV chips connected. This is equivalent to 60kHz readout rate if we switched to 1 sample mode at 100% occupancy. Will test with full optimized setup
- Issue with MPD : noise on optical transceiver need to run at lower speed 1.25 GBps instead of 2.5 Gbps (seems ok for SIDIS but ideally would need to be replaced)

- VTP readout ongoing
  - Optical to VXS board complete end of January
  - VXS FADC readout first
  - MPD VTP readout adapted from FADC

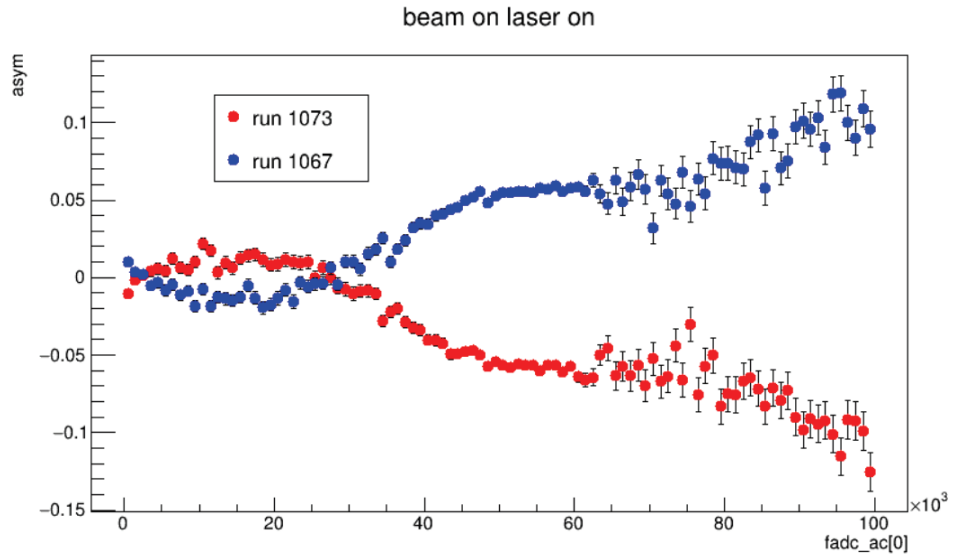
Preliminary results from Compton

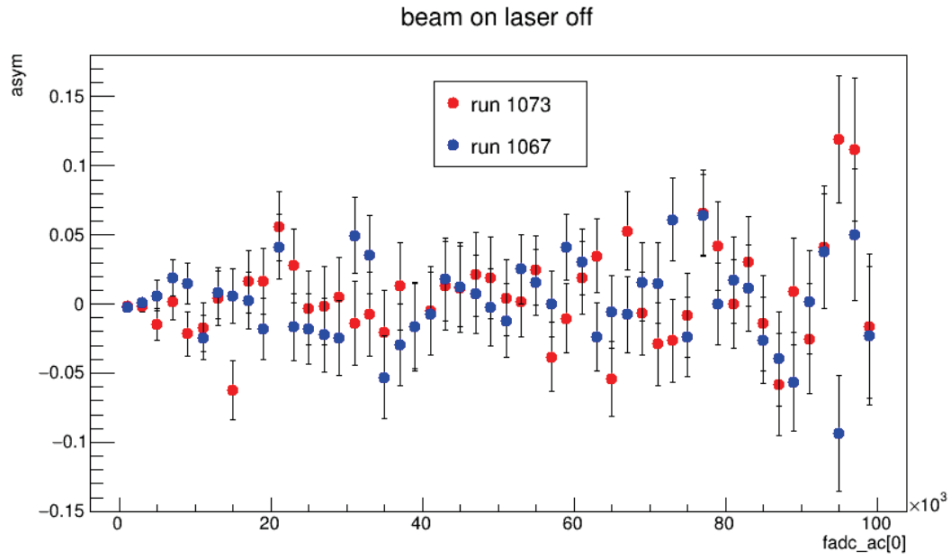
- FADC + VETROC + VTP (trigger module)
- Implemented delayed helicity readout
- Helicity scaler with VETROC and VTP for normalization (deadtime, power, position)
- Photon (and electron trigger)

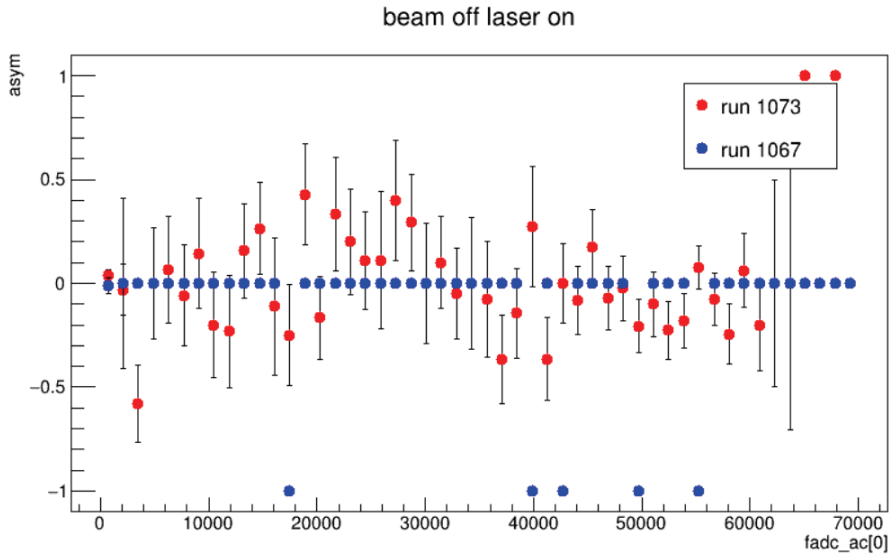
- Software

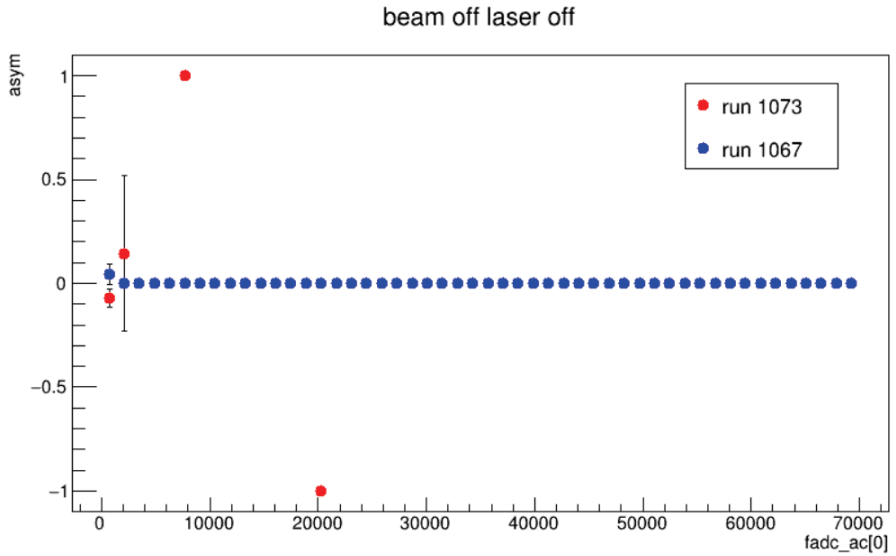
Preliminary results from Compton

- Rates up to 50 KHz with deadtime of about 10%
- Compton Asymmetry from Photon









Umass test stand setup

- Testing current FADC
- Helicity board set uo

- On going VXS FADC readout for faster FADC readout
- Upgrade network to 10 gigE

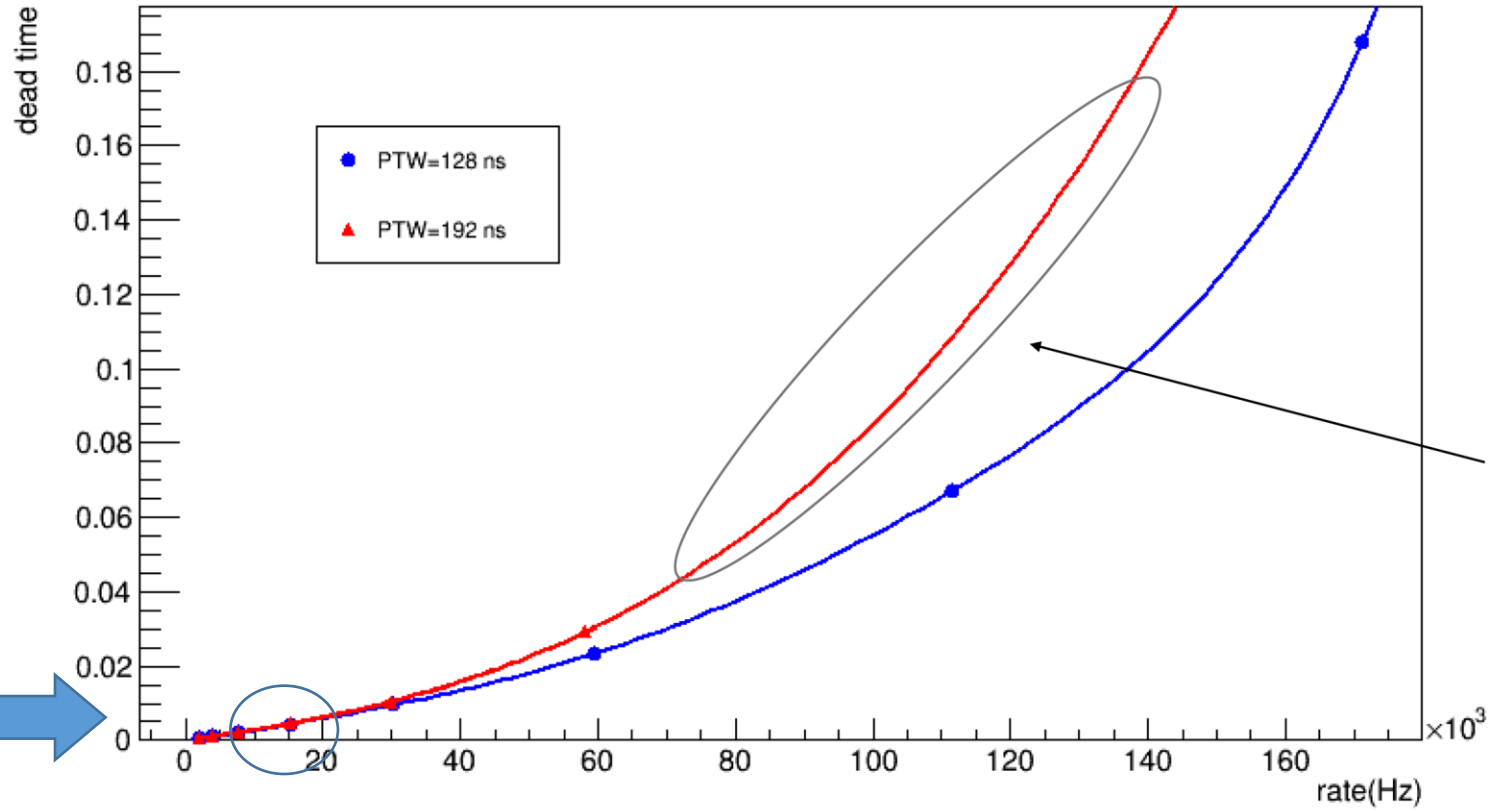
- Test calorimeter two crates trigger this summer

FADC

Dead time for raw mode (mode 1) (Narrow pulse)

Blocklevel=40 Bufferlevel=10

Compare the dead time when using different window width



Note: When PTW=192 ns, due to the data transfer limit (1Gb/s), the highest rate it can reach is 75 kHz;

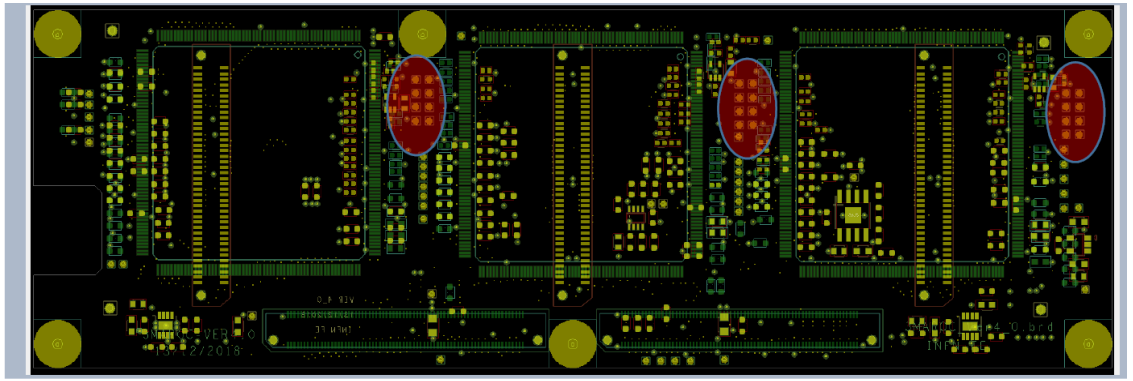
So the projection may not be right.

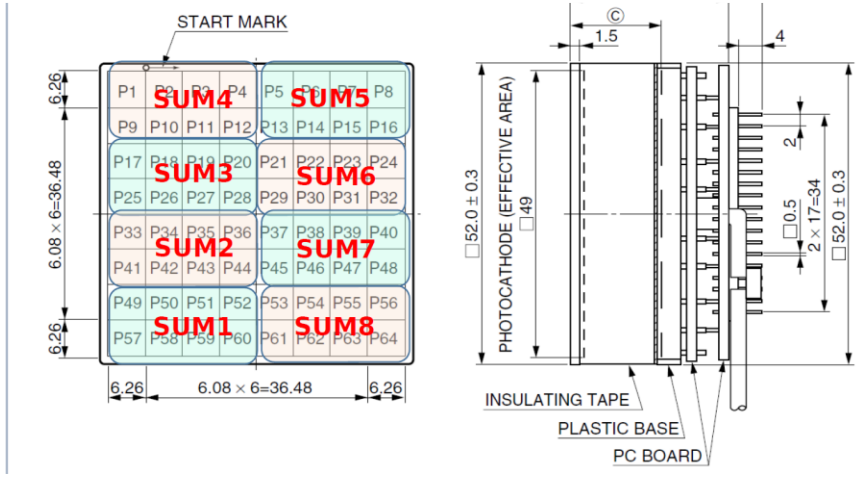
1%
At 20 KHz

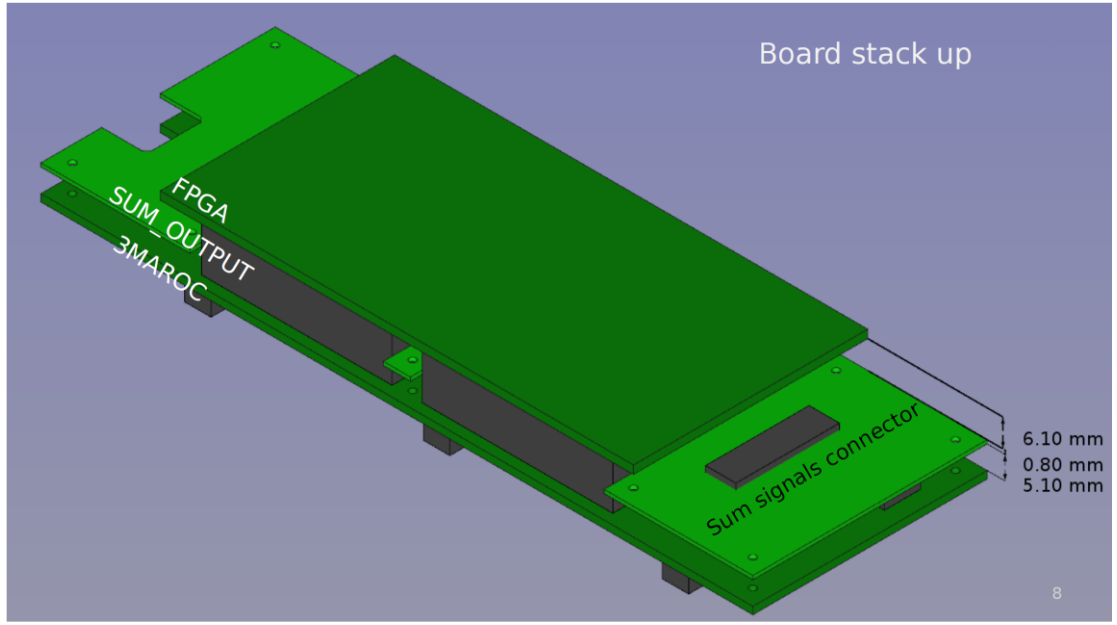
Improved with fast VXS readout and network upgrade to 10 gigE

MAROC

- INFN Ferrara accepted to modify RICH board to have sum output Electronics produced and at JLab
- Being tested in Test Lab and TEDF

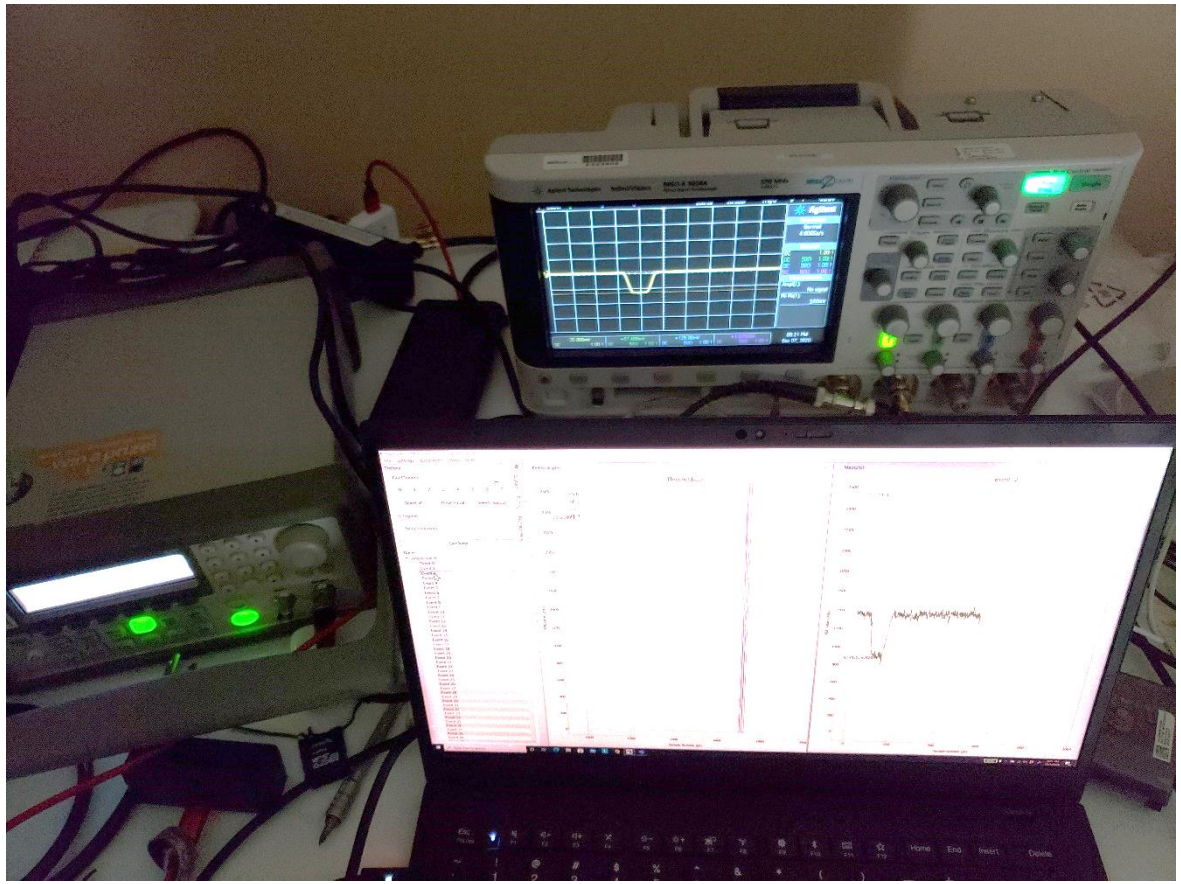






AARDVARC / ASOC

- Received spare board
- Working with pulser
- Setting up with detector in Test Lab



Conclusion

- Requirements
  - preRD ongoing
    - Still seems ok for SIDIS at 100 KHz with 1 sample with APV
    - Not an issue with VMM
    - VMM testing ongoing for signal to noise and behavior in high background when prototype build
    - FADC development ongoing : 1% deadtime at 20 kHz before fast readout implemented
    - MAROC testing : ongoing
    - ASOC testing
  - Updated data rates with VMM3
    - Can take more for J/Psi but need plan for silo
    - Most likely can take more for SIDIS but need to be tested