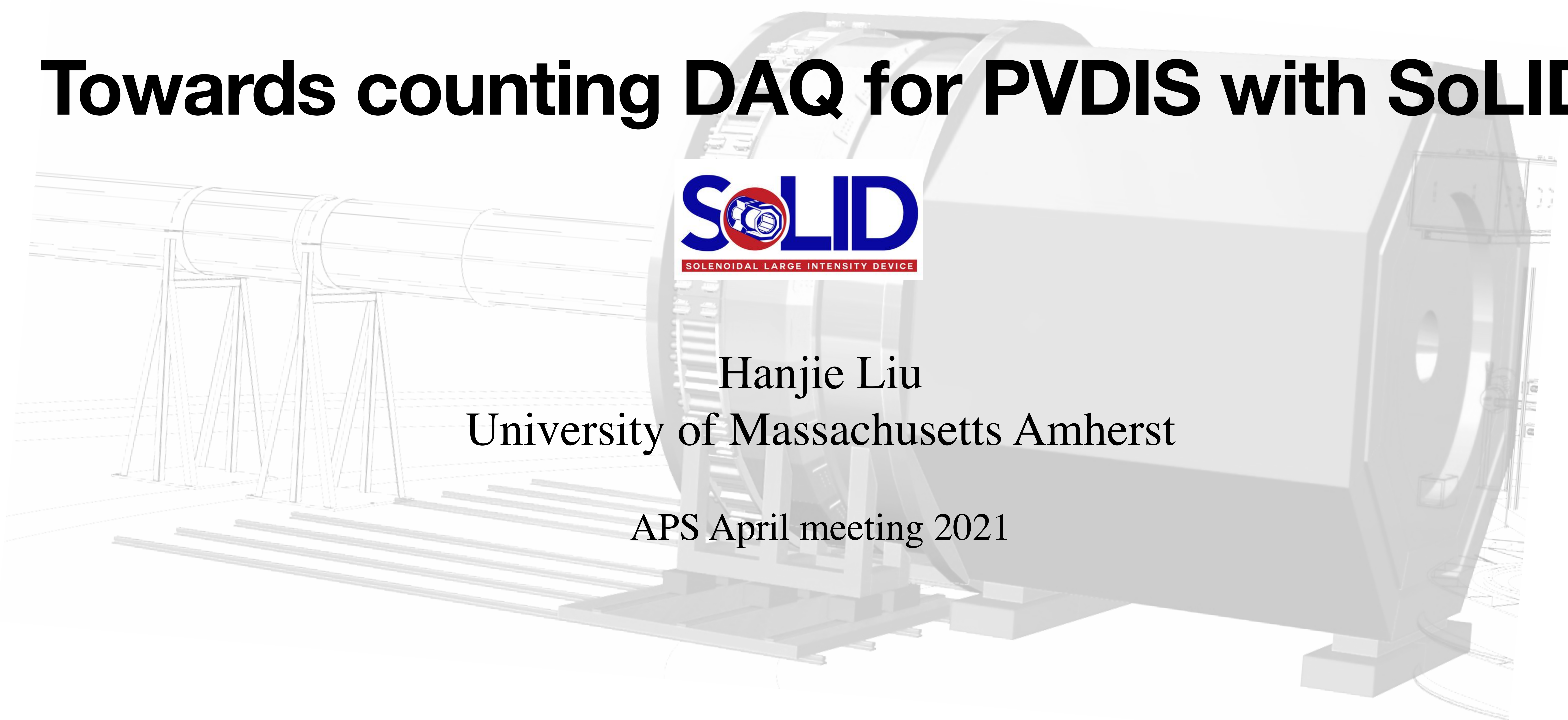
Towards counting DAQ for PVDIS with SoLID



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DAQ Requirements for PVDIS experiments

PVDIS observables: $$A_{PV} = \frac{\sigma_R - \sigma_L}{\sigma_R + \sigma_L}$$ ~ few hundreds of ppm

High precision measurements require high statistics → few hundred kHz

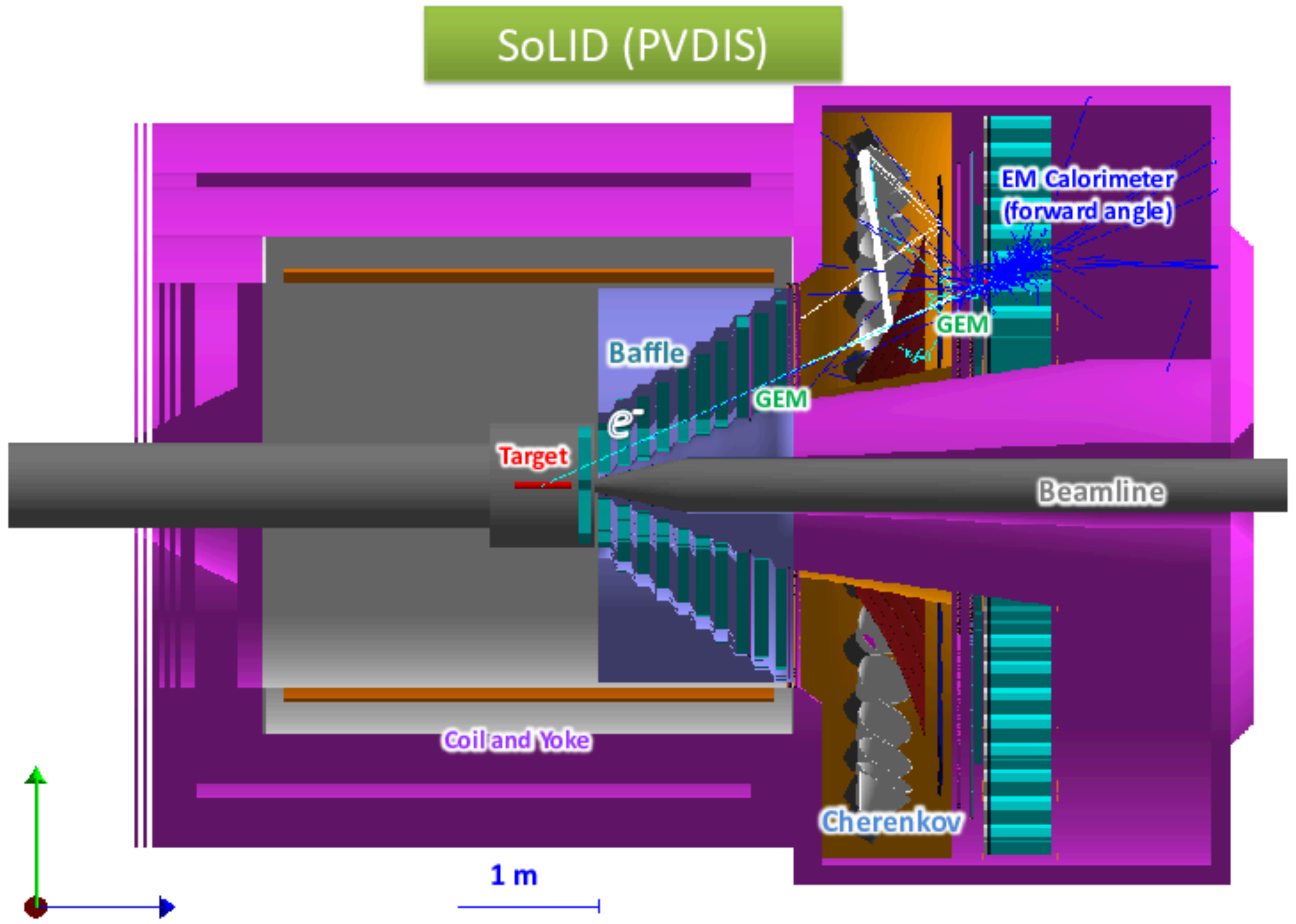
Deep inelastic scattering → high pion backgrounds

$$A_m = f_{\pi/e} A_\pi + (1 - f_{\pi/e}) A_e$$

↑

suppress by the (Cherenkov & Calorimeter) trigger

DAQ for 12 GeV PVIDS experiment



- Large acceptance
- High luminosity
- Higher precision requirement
- Larger and more complicated detectors

(over 160,000 GEM tracking channels and over 4,000 trigger/particle ID channels)

↓

VXS crates, FADC (Flash ADC Module), VTP (VXS Trigger Processor)…….

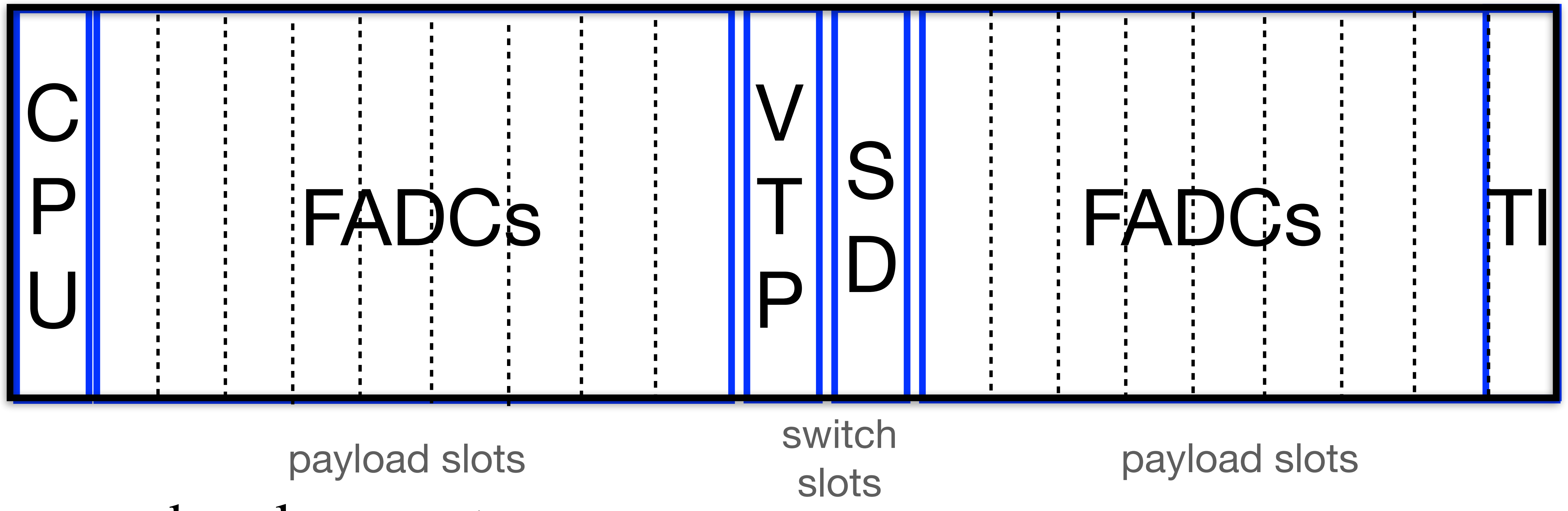
Have been successfully used in JLab CLAS 12 and GlueX experiments

Aim to run with almost no DAQ dead time for PVIDS

12 GeV DAQ development

VXS crates

- synchronize and pass signals between each of the payload slots to a central switch slot via the backplane



FADC

- 250 MHz pipelined flash ADC
- Can provide raw pulse samples, or integrated charge and time, and scaler counts
- Two distinct data paths:
  i. tigger data path: continuously stream trigger data to VTP,
  ii. readout data path: continuously stores digitized data for each channel in circular buffers

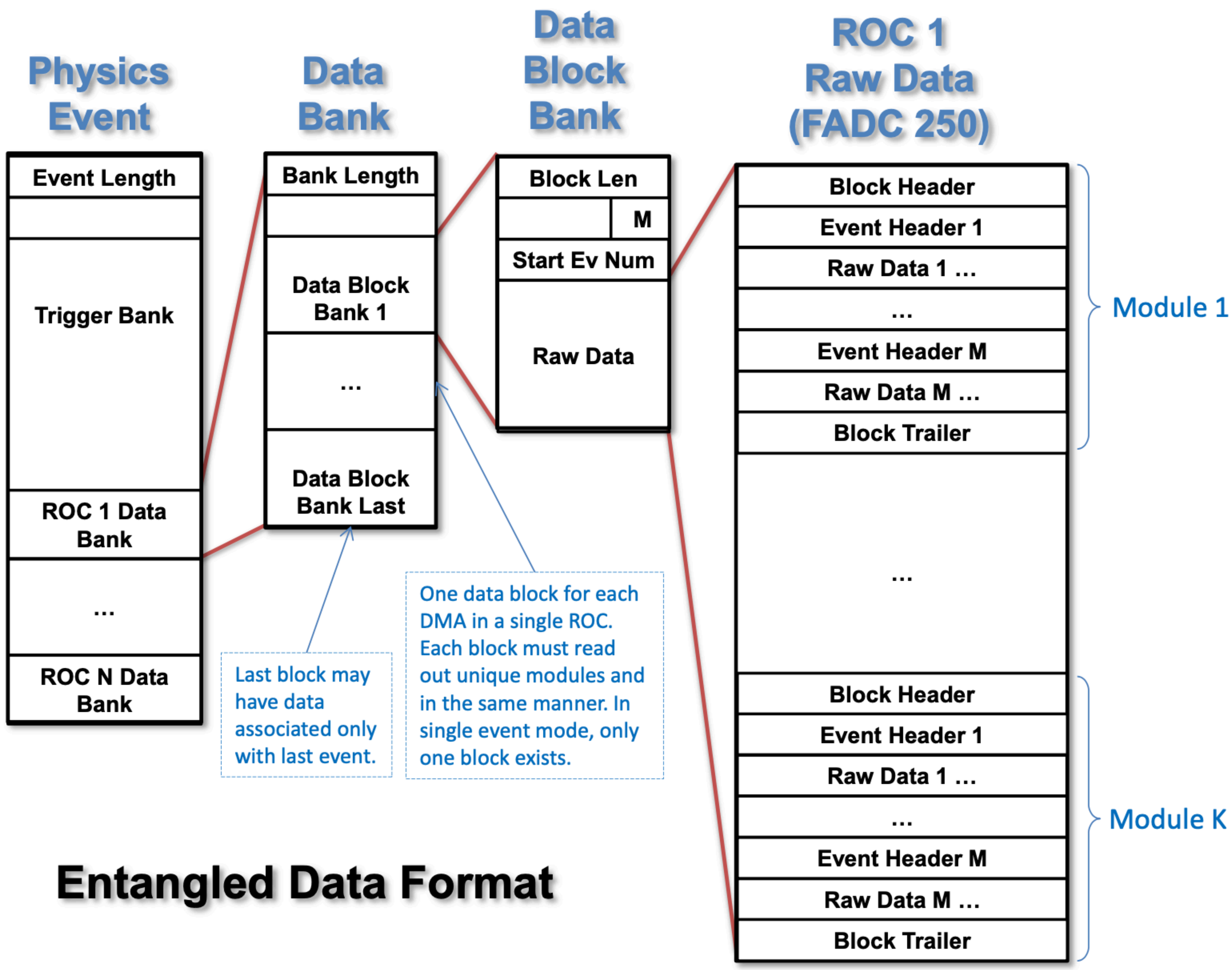
VTP (VXS Trigger Processor)

- Each FADC is connected to the VTP with 4 full duplex serial links that can operate up to 6.25Gbps each
- VTP receives integrated & calibrated pulse integrals & timestamps from up to 256 FADC channels in 1 crate
- Can exchange information with other VTPs using 1 or more of the full-duplex QSFP optical interfaces
- Forms triggers based on the modules data

12 GeV DAQ development

Event Blocking

- Data associated to N triggers is packed into a block for readout
- Typically readout in blocks of 20 or 40 events
- Trigger rates >100kHz can be achieved with low dead-time in this way – otherwise ~10kHz is the non-event blocking limit
- Event blocking has been used in the CREX Compton electron detector readout. Offline decoder is available



Entangled Data Format

12 GeV PVDIS DAQ pre R&D

PVDIS DAQ:

- Calorimeter, Cherenkov -> FADCs, GEM ->VMM3 or APV25;
- Trigger: Cherenkov & Calorimeter;
- Total trigger rate ~ 600 kHz (30 sectors); sector trigger rate < 20 kHz —— 30 DAQ systems;
- FADCs run in raw sample mode to correct the pile ups;
- Total data rate ~ 2.9 GB/s, sector data rate ~ 94 MB/s;

almost no dead time;
Pion contamination < 10^{-3}

DAQ Pre R&D key goals:

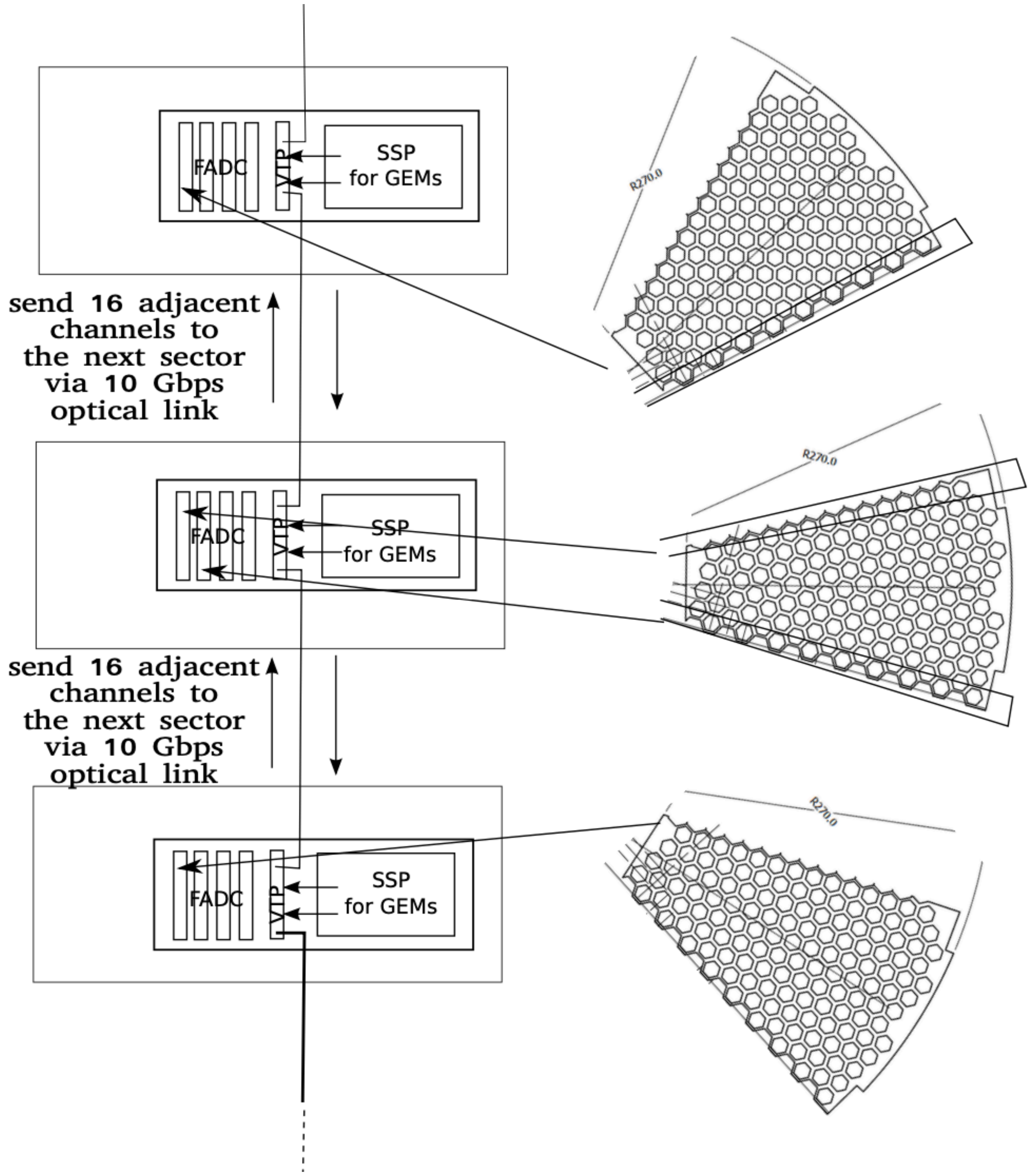
1. Develop FADC fast readout with VTP **(done)**;

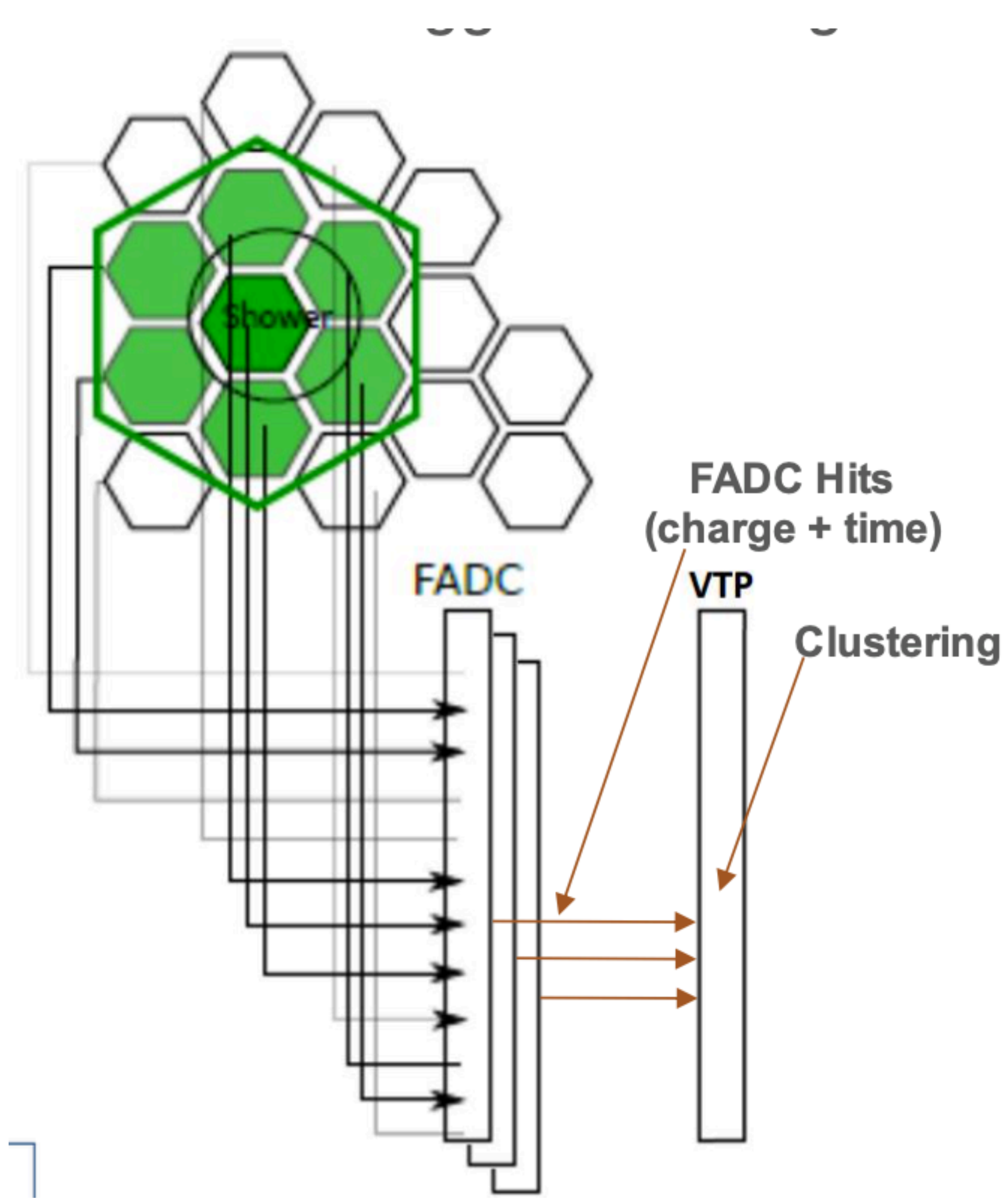
- VME readout is limited to 200 MB/s for 1 crate;
- FADC->VTP readout allows 200MB/s for each FADC;

12 GeV PVDIS DAQ pre R&D

2. Prototype Calorimeter trigger algorithm (mostly done)

- Finding a cluster to generate a trigger is possible through VTP



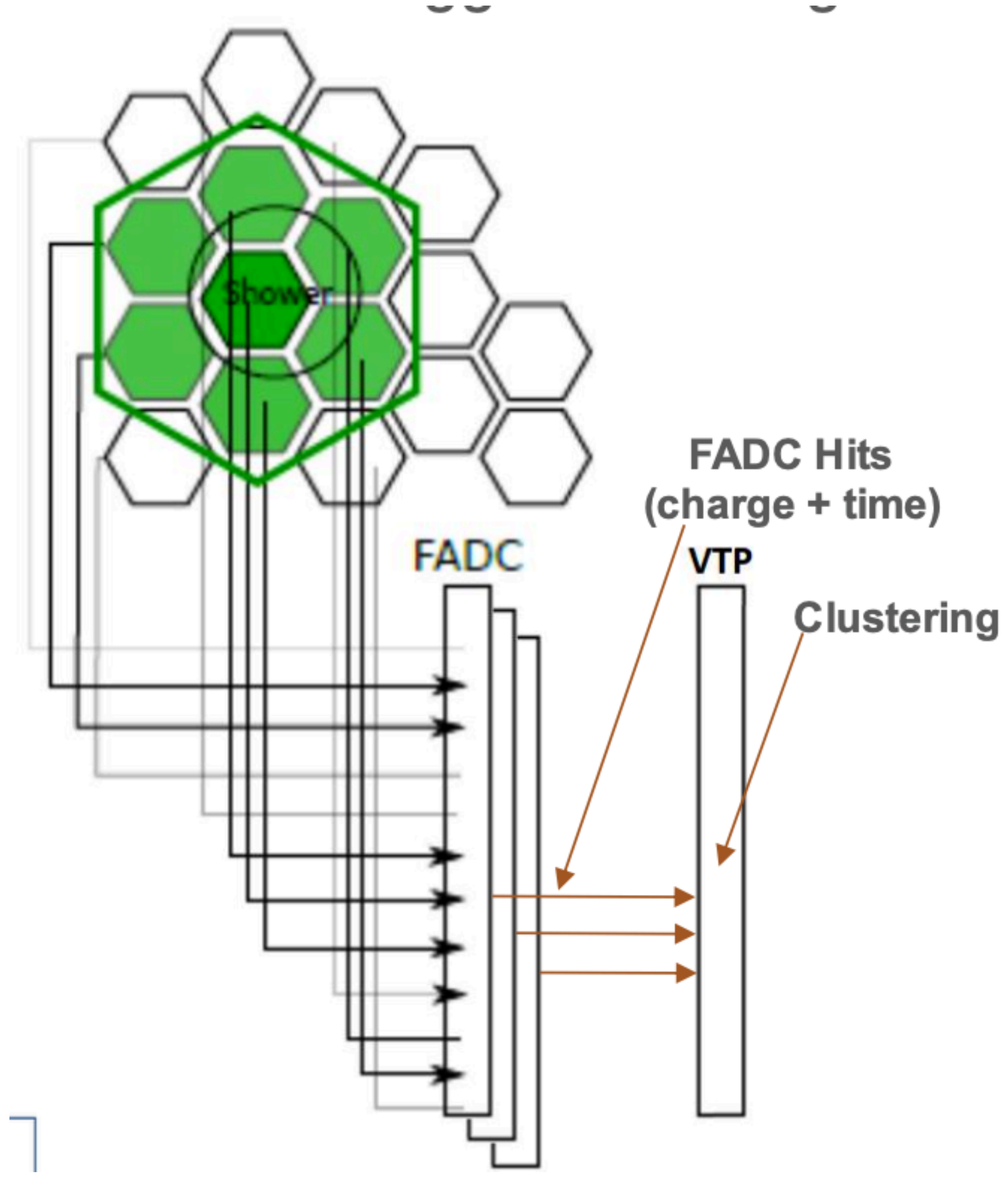


12 GeV PVDIS DAQ pre R&D

2. Prototype Calorimeter trigger algorithm (mostly done)

- Finding a cluster to generate a trigger is possible through VTP
- Trigger algorithm is designed using VIVADO HLS:

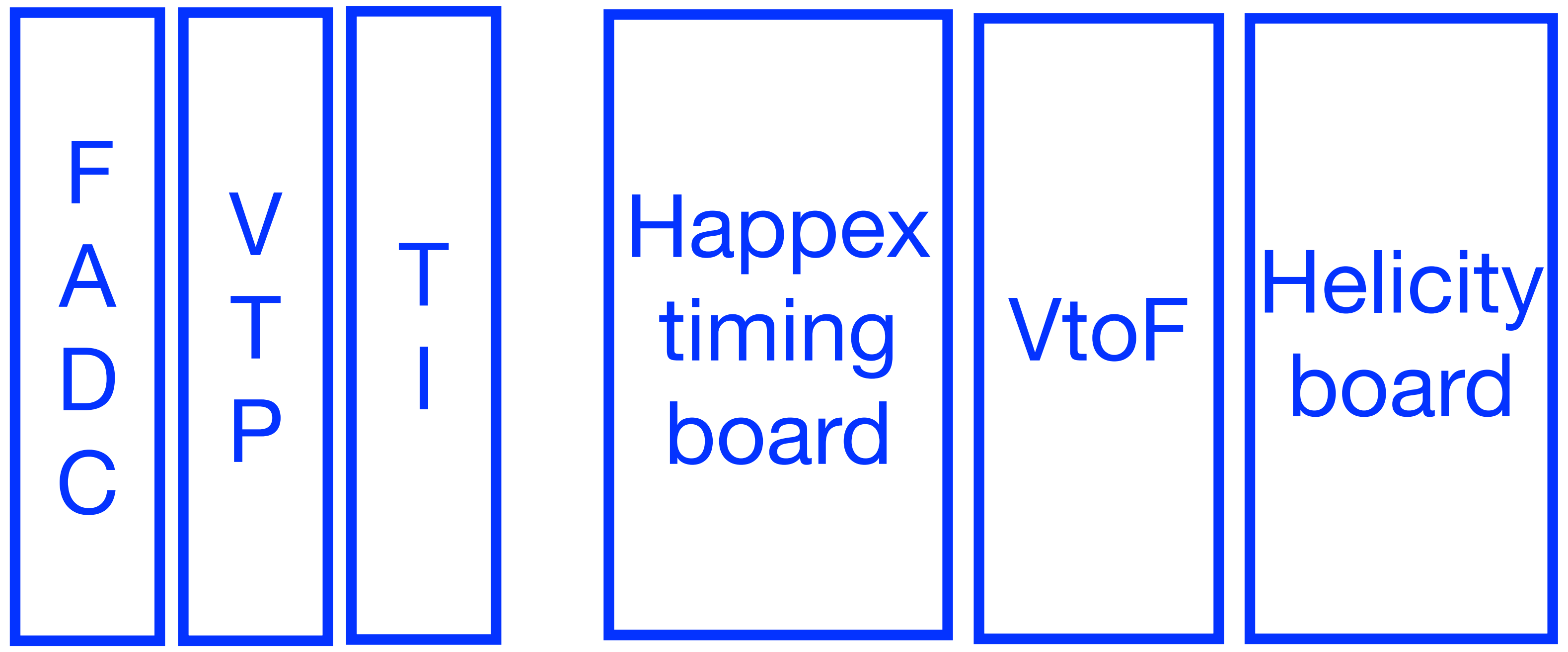
1. VIVADO HLS — convert C++ to Hardware Description Language (HDL);
   (scientists can involve in the trigger algorithm design;
   Use simulated data to test the trigger algorithm before applied to chips)
2. VIVADO synthesis — HDL to FPGA primitives;
3. VIVADO implementation — map FPGA primitives to chip and route connections.



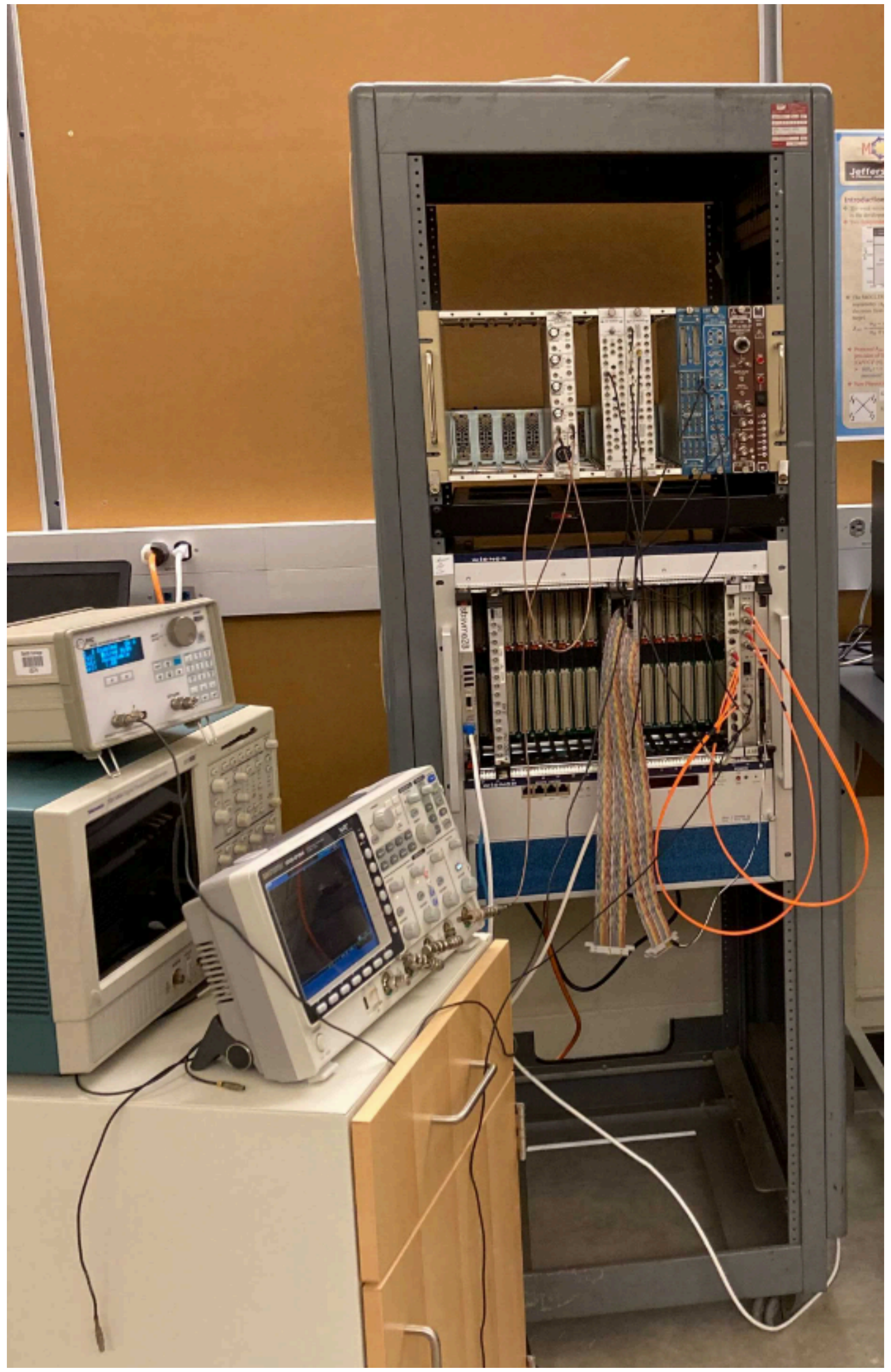
12 GeV PVDIS DAQ pre R&D

3. Rate capability test and trigger algorithm test (ongoing)

- A test stand has been built at UMass since last summer;



- Measure FADC dead-time with fast readout applied
- Test the ability to measure a ~ 600 ppm asymmetry at 20 kHz
- Test the Calorimeter triggers, and data sharing between two crates



DAQ pre R&D plan — — GEM

4. Develop GEM VMM3 based readout

- Complete the development and test of VMM3 direct readout: 6 bits ADC, 25 ns conversion
- An evaluation board with 12 channels is being tested with GEM (comics/radiative source) to study the high rate capability;
- A prototype front-end board that supports 128 channels is being built, and will be tested with GEM detector

5. GEM APV25 readout capability at high trigger rates

- Latest development: an MPD & SSP with 15APVs -> limit to 90 kHz with 1 sample at 30% occupancy
- Exploring new ways to improve: less APVs per MPD, or replace MPD with new boards
- Optimization using APV25 for GEM for SBS is ongoing

Summary

- The electronics development made for JLab 12 GeV upgrade makes it possible for PVDIS to record data event-by-event
- With careful system design, there will be almost no dead time for the DAQ system, and a high pion suppression factor
- The actively ongoing SOLID DAQ pre R&D helps develop and understand the trigger rate capability of the DAQ system

Backup

DAQ for 6 GeV PVIDS experiment

HRS DAQ —— calibrations

- Standard counting DAQ
- Detectors signals are recorded for each event

Kine#	HRS	E_b (GeV)	θ_0(deg)	E'_0 (GeV)	R_e(kHz)	R_{π^-}/R_e
DIS#1	Left	6.067	12.9	3.66	≈210	≈0.5
DIS#2	Left & Right	6.067	20.0	2.63	≈18	≈3.3
RES I	Left	4.867	12.9	4.0	≈300	$<$≈0.25
RES II	Left	4.867	12.9	3.55	≈600	$<$≈0.25
RES III	Right	4.867	12.9	3.1	≈400	$<$≈0.4
RES IV	Left	6.067	15	3.66	≈80	$<$≈0.6
RES V	Left	6.067	14	3.66	≈130	$<$≈0.7

Parity DAQ —— production running

- Scaler based, no detailed information on the detector signals
- NIM logic modules to generate the electron trigger and pion triggers

DAQ for 6 GeV PVIDS experiment

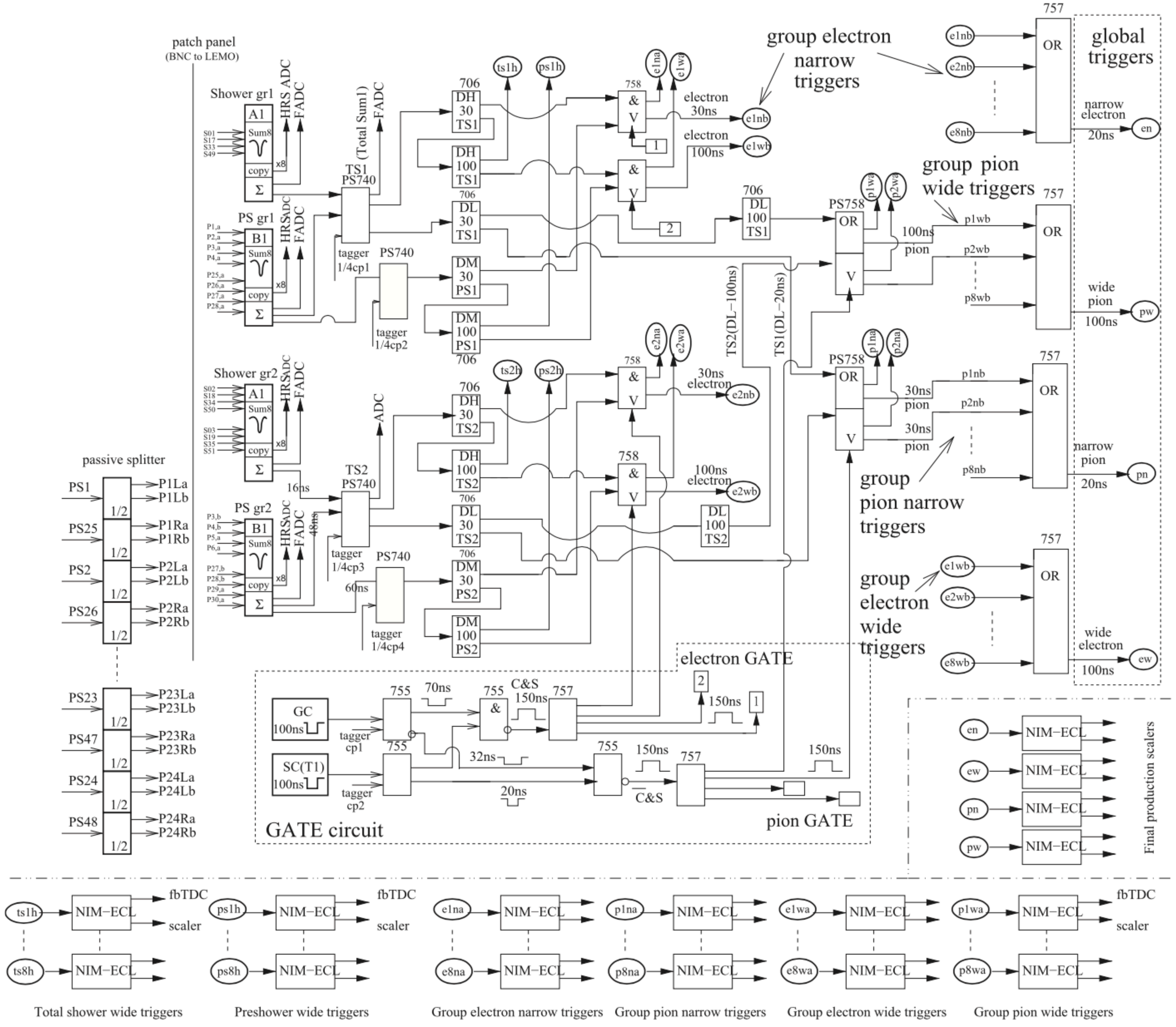
HRS DAQ —— calibrations

- Standard counting DAQ
- Detectors signals are recorded for each even

Parity DAQ —— production running

- Scaler based, no detailed information on the
- NIM logic modules to generate the electron t

Pion contamination $f_{\pi/e} < 2 \times 10^{-4}$
Parity DAQ dead time < 3% at 100 uA
Caused systematic uncertainty < 0.5%



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