SoLID DAQ

SoLID collaboration meeting

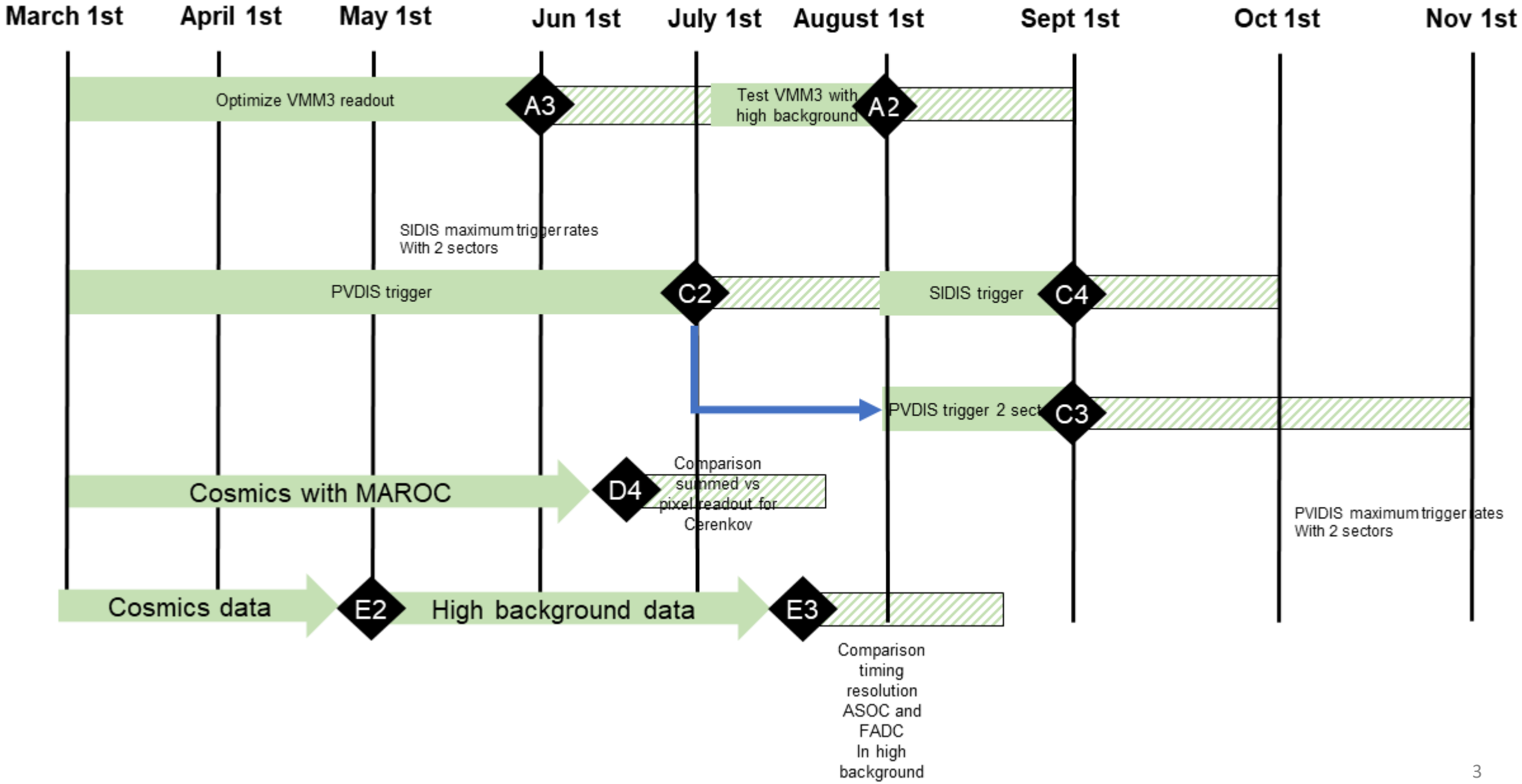
June 10th 2021

Alexandre Camsonne

Outline

- preR&D updates
  - VMM
  - APV
  - FADC
  - Cerenkov
  - TOF
- Additionnal tests beyond preRD
- Streaming readout option
- Conclusion

preRD schedule

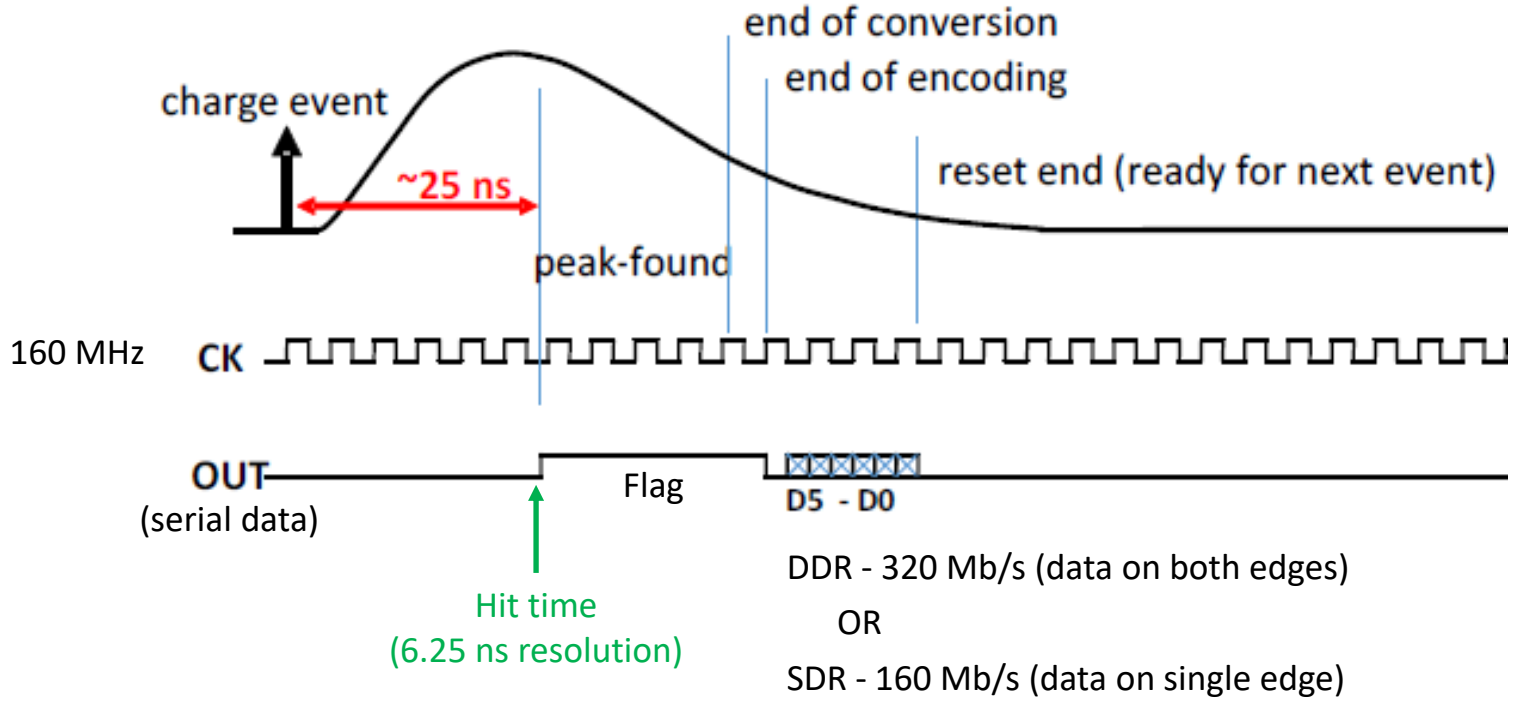


VMM test

- 2 test board :
  - 1 testing with detector to take cosmics : need work on grounding and shielding
  - 1 development of direct readout
- Prototype
  - Design close to complete
  - ~ 200 VMM chips received, testing testing setup
  - Firmware is scaling to 128 channels from 17 channels from eval board
- Test VMM with GEM cosmics and X-rays August 1st 2021

VMM 6-bit Direct Output data format

Peak amplitude converted to 6-bit value



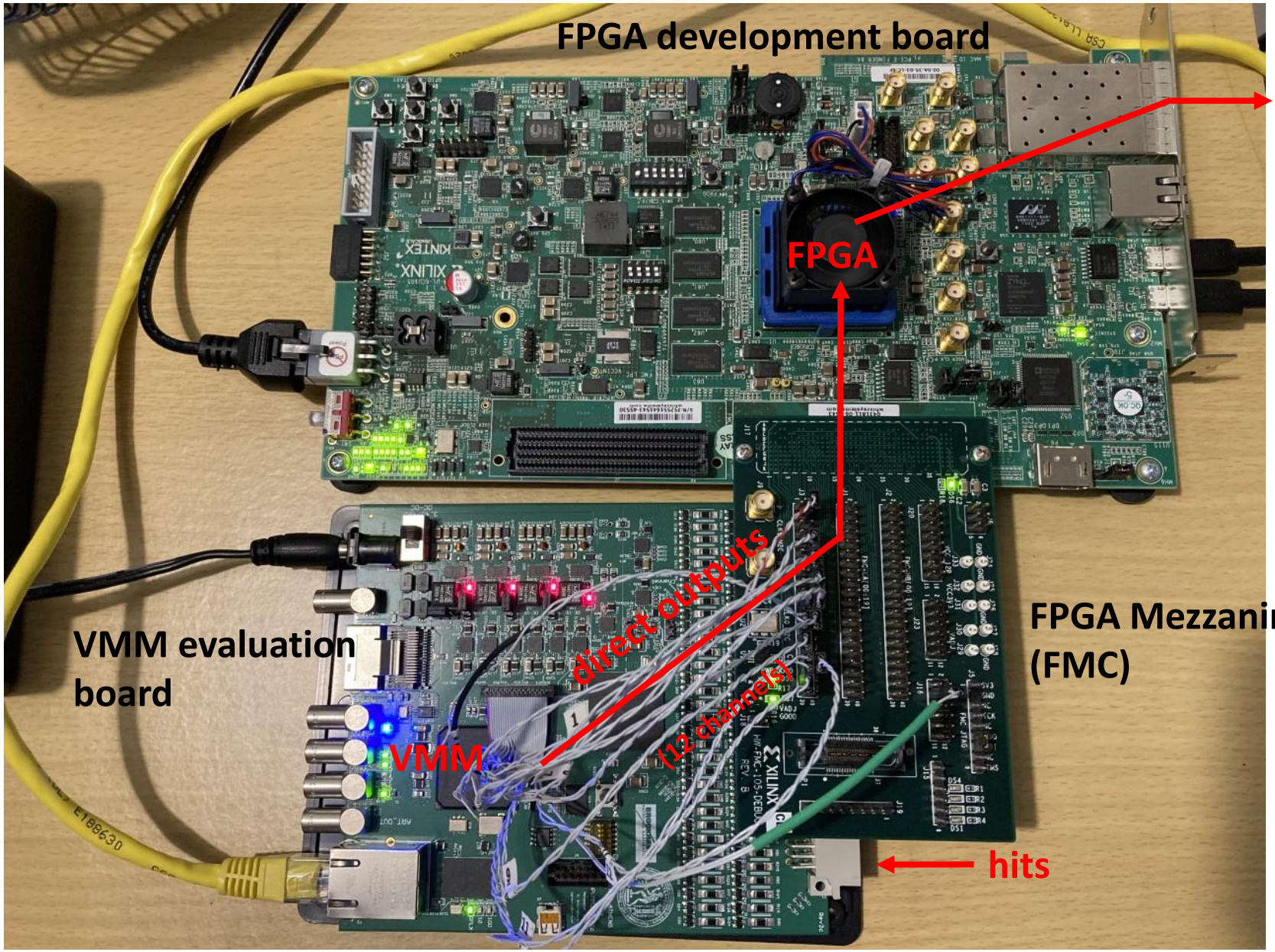
DDR - 320 Mb/s (data on both edges)

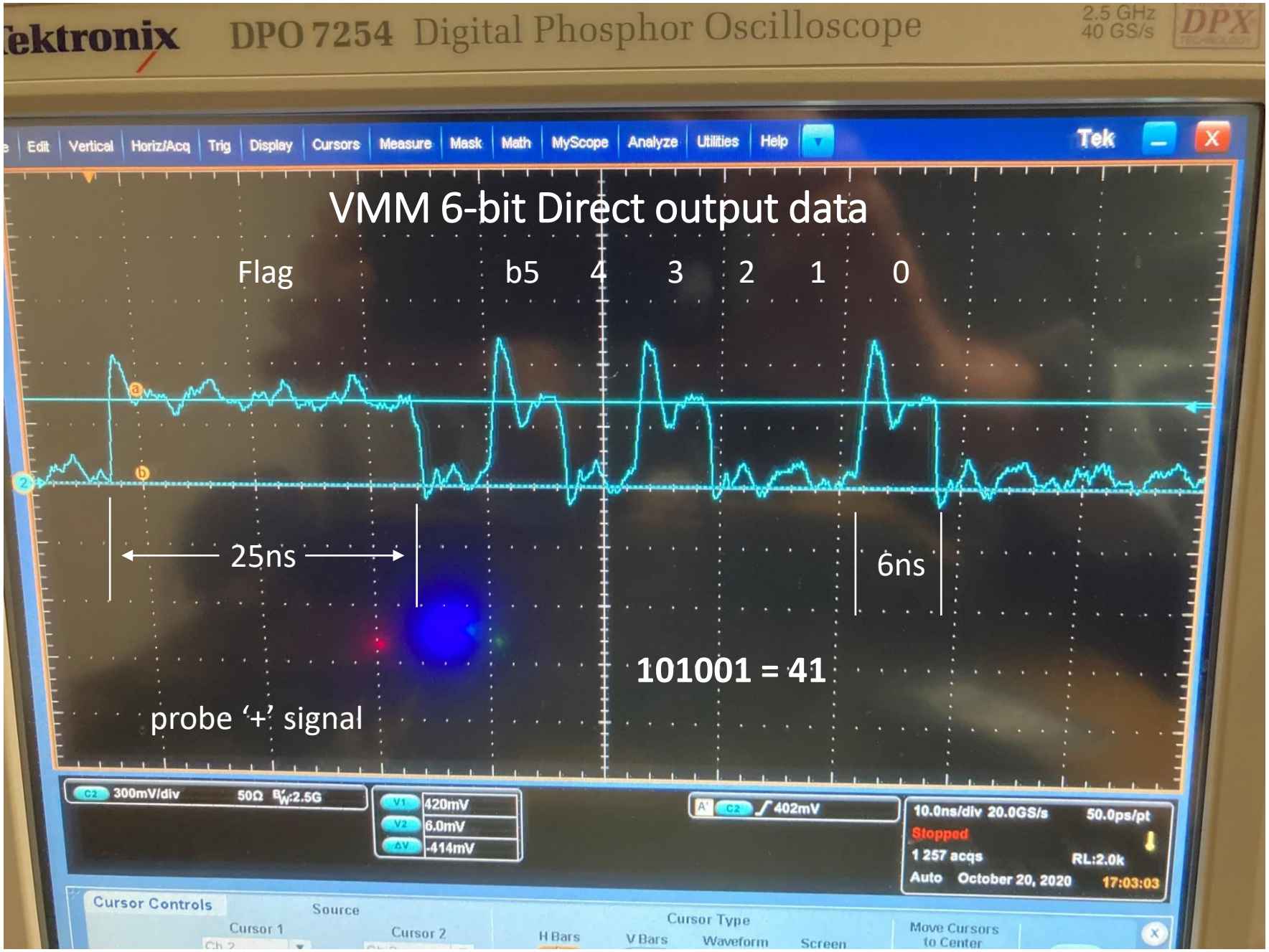
OR

SDR - 160 Mb/s (data on single edge)

Reading VMM Direct Outputs from Evaluation Module

Initial firmware development and testing done using KCU105 FPGA Development board

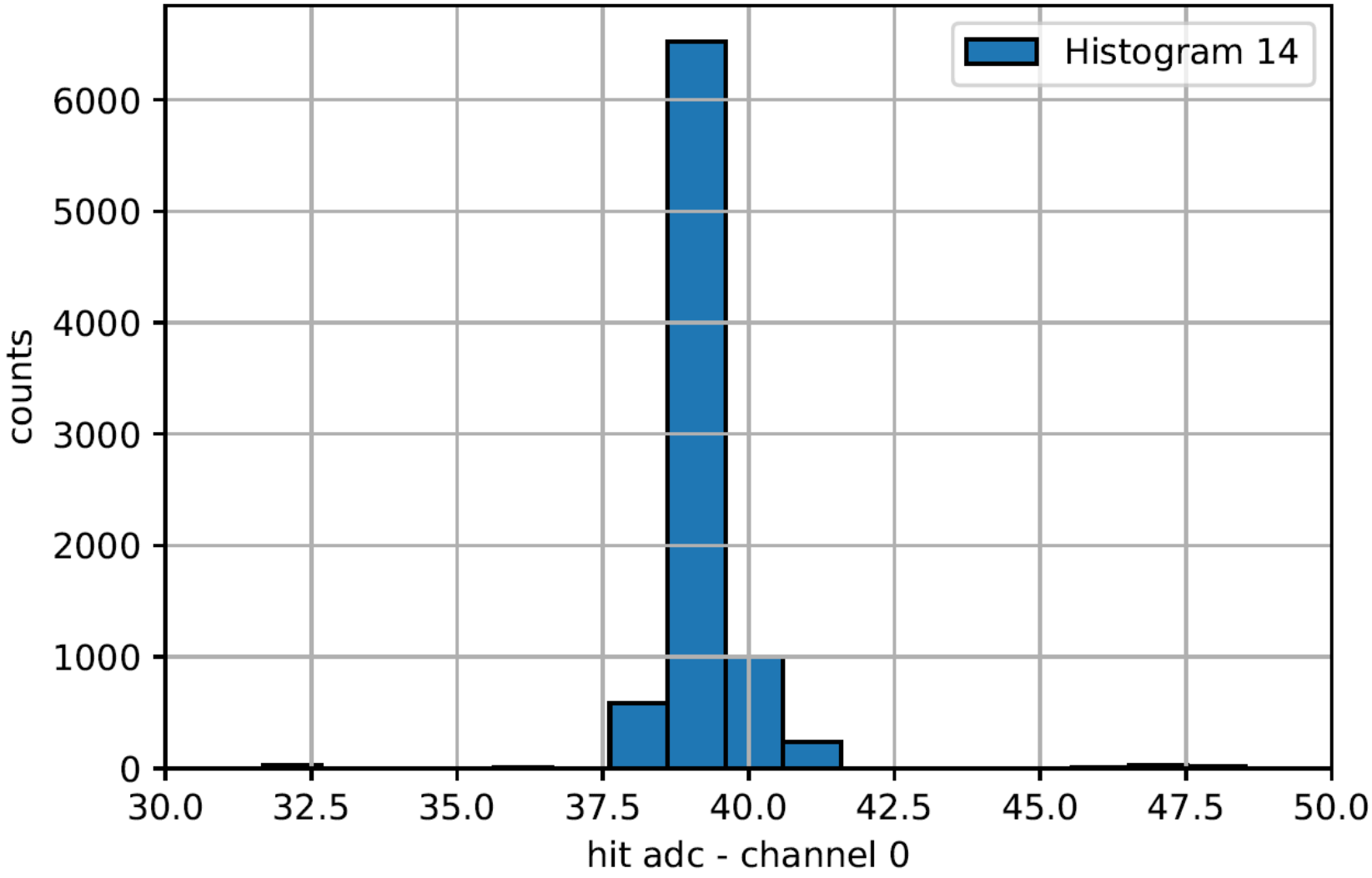




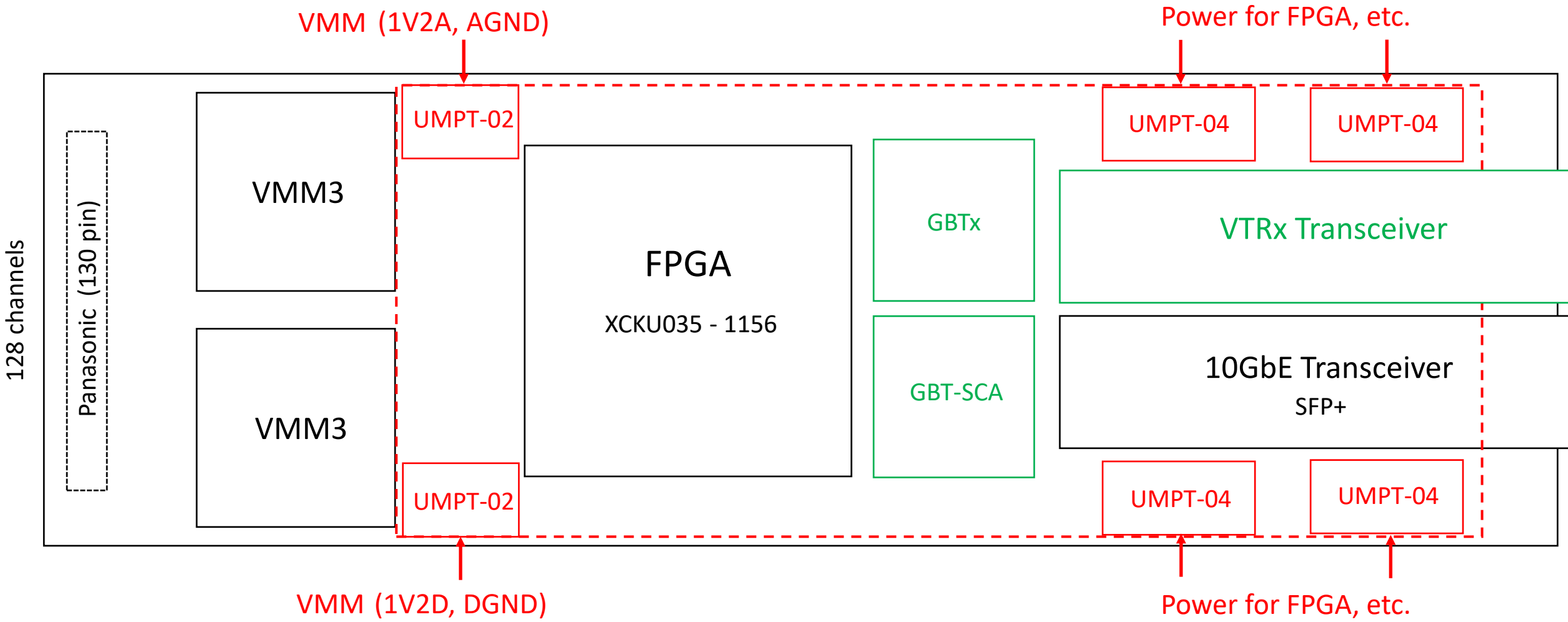
SDR - 160 Mb/s

41 x 16 = 656
consistent with
10 bit data avg

VMM 6-bit ADC direct data

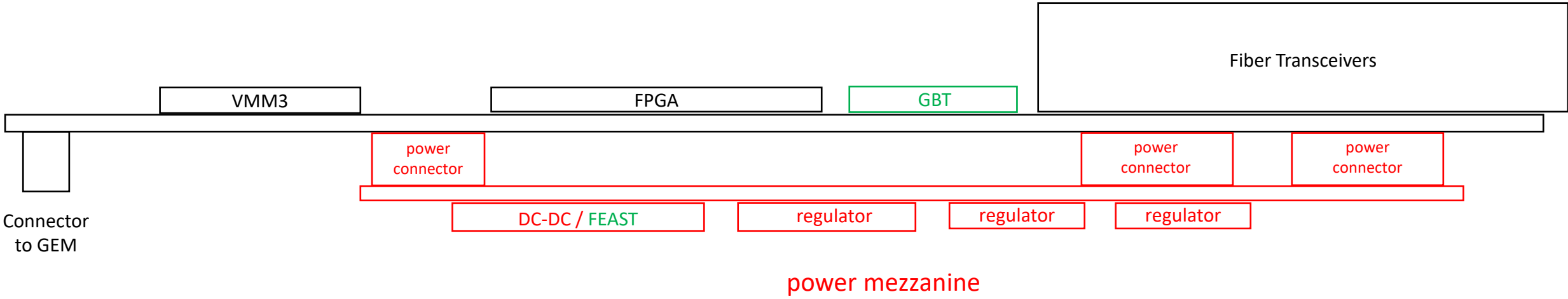


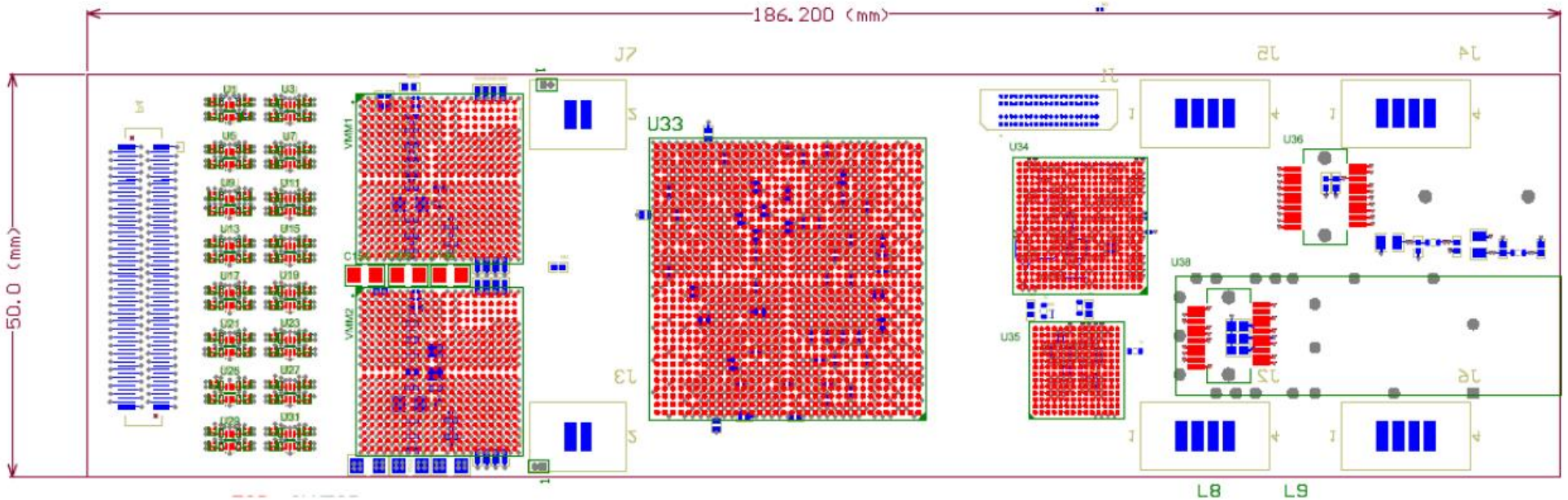
VMM Prototype Card



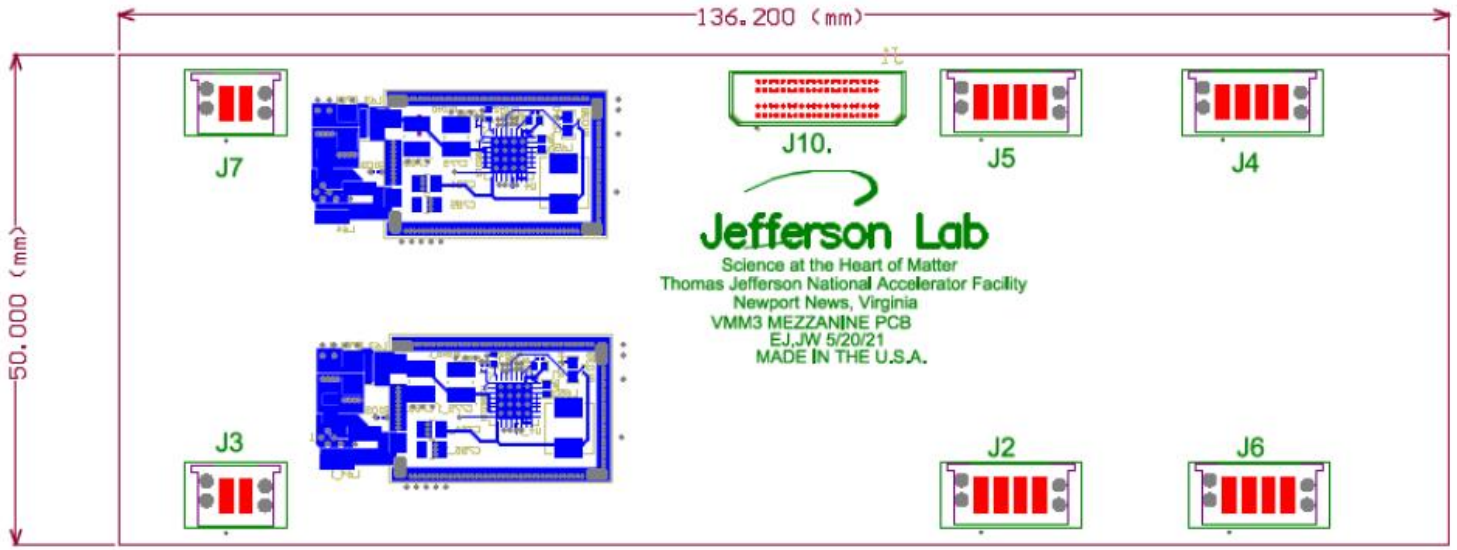
VMM Prototype Card

(side view)





VMM prototype board
(128 channels)



Power Mezzanine

APV25 tests

- Fiber and transceivers ordered for full scale test
- SSP new firmware up to 32 MPDs developed and being tested with 12 MPDs
- Will add more MPDs when access to lab
- High speed readout of MPDs with VTP will eliminate VME backplane bottleneck (200 MB / s vs 1.25 GB/s) in development (~ 2 months to complete)

APV25

- Tested : Initial testing has with 6 samples per trigger has achieved ~10kHz trigger rate using 1 SSP with 1 MPD that had 5 APV chips connected. This is equivalent to 60kHz readout rate if we switched to 1 sample mode at 100% occupancy. Should be fine for SIDIS with less than 30% occupancy = 180 kHz
- Issue with MPD : noise on optical transceiver need to run at lower speed 1.25 GBps instead of 2.5 Gbps (seems ok for SIDIS but ideally would need to be replaced). A new revision has been ordered to fix issue, should reach 120 kHz at 100% occupancy

- VTP readout ongoing
  - Optical to VXS board complete end of January
  - VXS FADC readout first
  - MPD VTP readout adapted from FADC

SBS – VTP MPDRO update

VTP – HW ROC

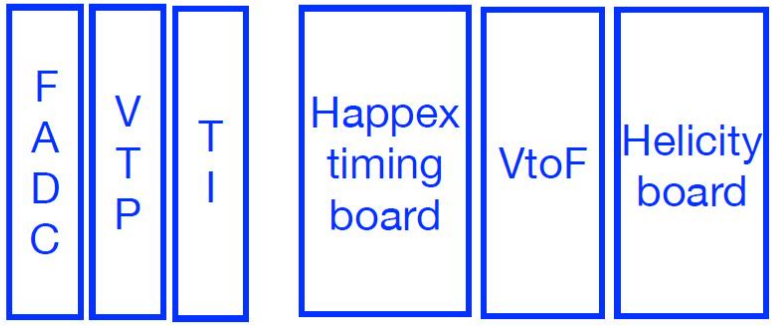
- Software ROC configures VTP (D. Abbott)
  - 10Gb links (MAC, IP, etc)
  - EventBuilder / EMU Connection
  - Handles CODA transitions
    - Download
    - Prestart / Go / End events
- Config files
  - VTP network connections
  - MPD / APV libconfig
    - Configure APV + MPD + VTP

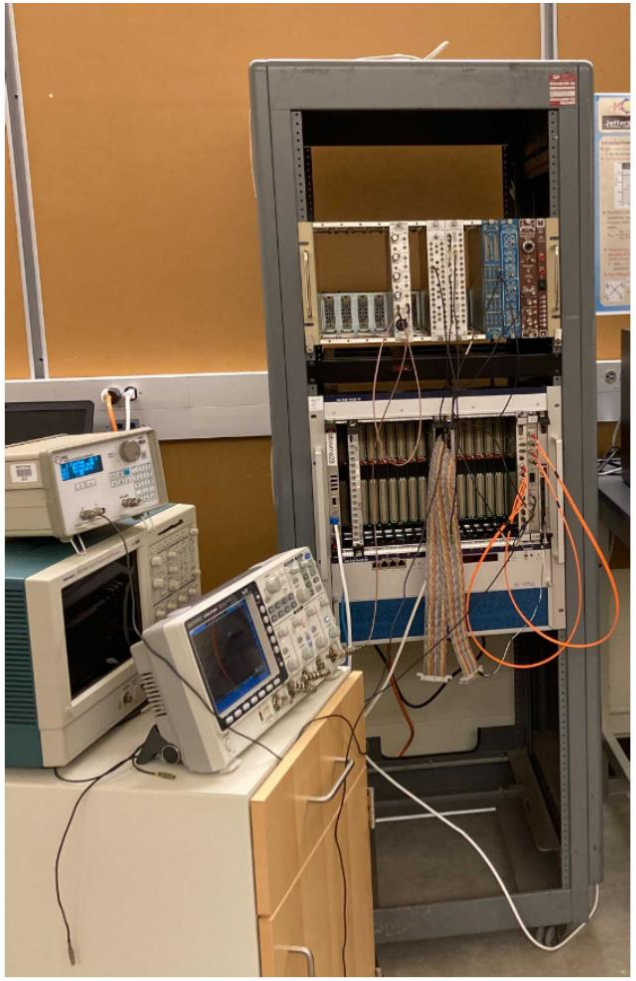
Test / Debugging programs

- QSFP-MPD link status
- MPD+APV link status
- MPD+APV init test
- mpdLibTest
  - Goalpost scan
  - Fish scan

Umass test stand setup

- A test stand has been built at UMass since last summer;



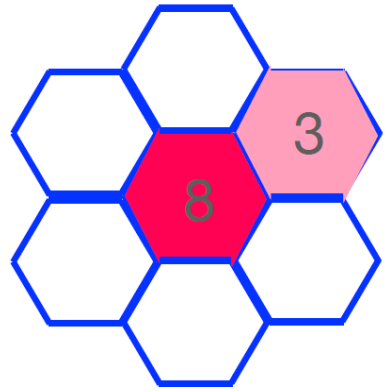


- Measure FADC dead-time with fast readout applied
- Test the ability to measure a ~ 600 ppm asymmetry at 20 kHz
- Test the Calorimeter triggers, and data sharing between two crates

FADC

- Finding a cluster to generate a trigger is possible through VTP
- Trigger algorithm is designed using VIVADO HLS (mostly done):

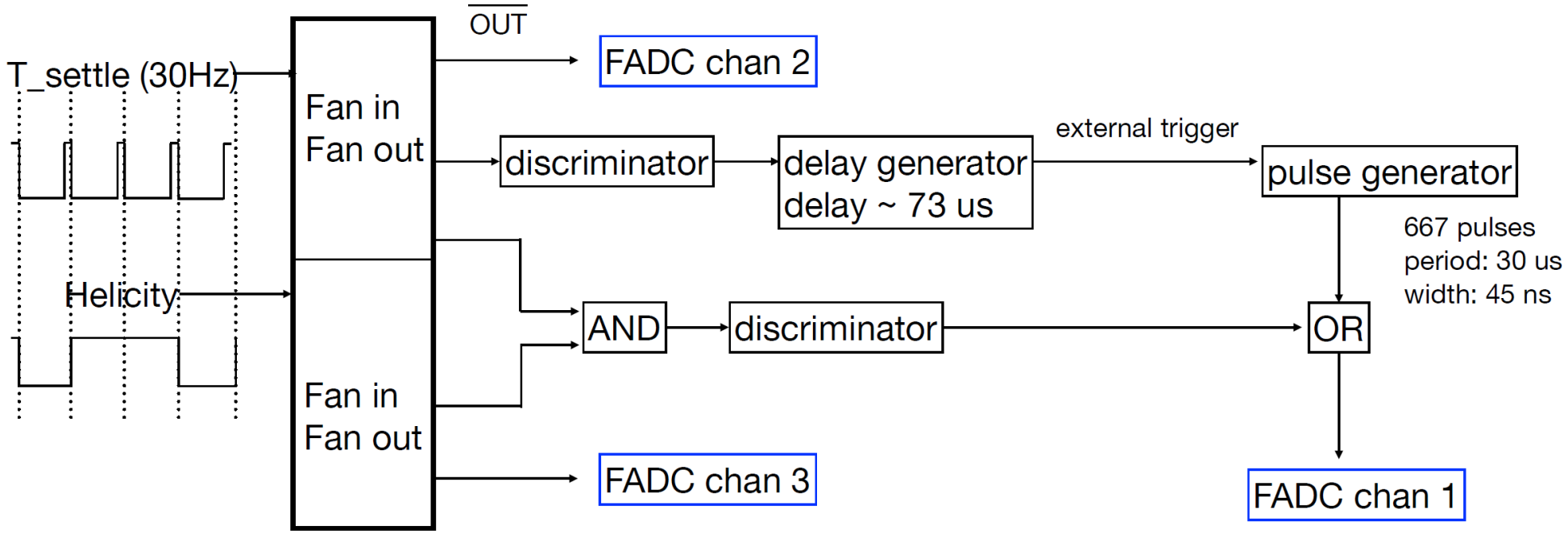
1. VIVADO HLS — convert C++ to Hardware Description Language (HDL);
   (scientists can involve in the trigger algorithm design;
   Use simulated data to test the trigger algorithm before applied to chips)
2. VIVADO synthesis — HDL to FPGA primitives;
3. VIVADO implementation — map FPGA primitives to chip and route connections.



- Trigger algorithm:
  - Seed hit > seed_threshold — —> center block
  - Center block should have the maximum energy deposit
  - The time difference between center block and the fired nearby block should be less than 8 ns
  - The cluster is reported with a total energy, (x, y) position, a time, and the number of hits

FADC asymmetry

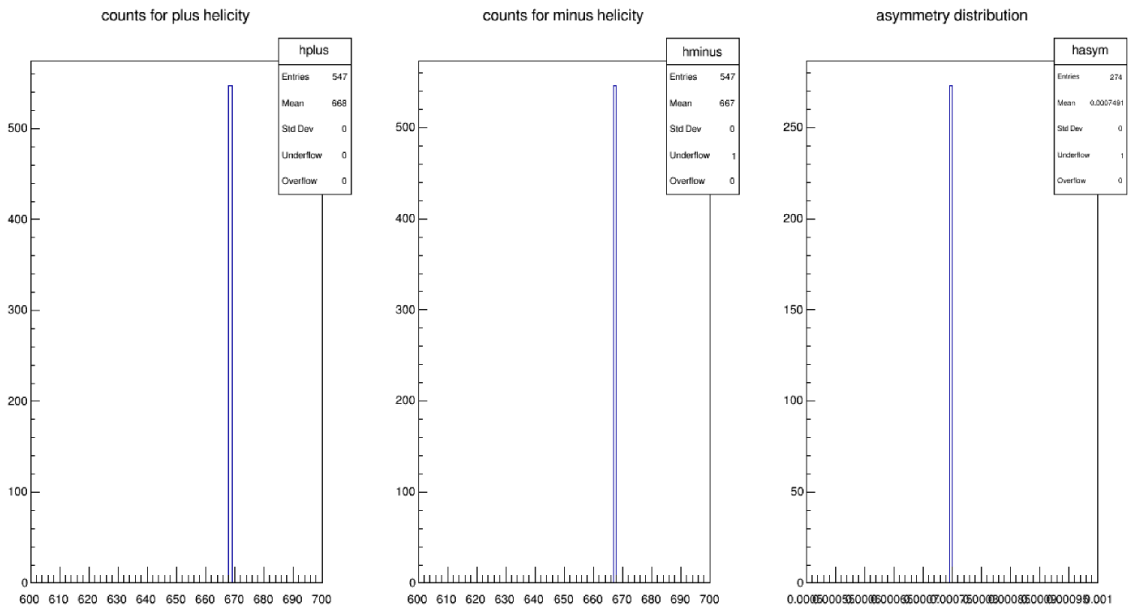
- Purpose: see if FADC is able to measure a 600 ppm-1000ppm asymmetry, and what issues might happen



- In "+" helicity, there are 668 pulses; in "-" helicity, there are 667 pulses.
- The expected asymmetry = (668-667)/(668+667) = 749 ppm

FADC asymmetry

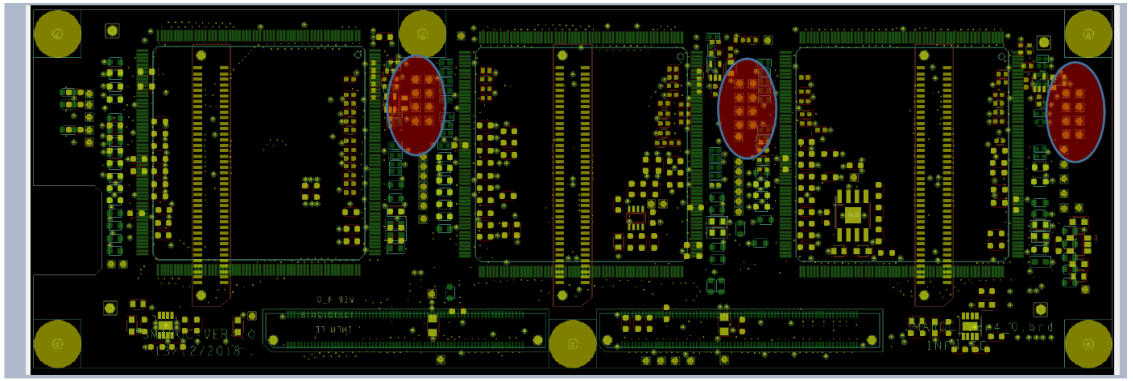
- Compton electron firmware; run in raw mode with Blocklevel=10, Bufferlevel=10;
- Helicity is 30 Hz Quad pattern (+—+ or -++-); helicity information is recorded both in VTP and FADC chan3. They agree with each other. The helicity pattern matches the prediction.
- The number of pulses in "+" ("-") is counted per helicity window;
- The asymmetry is calculated for each quad as: $(N_+ - N_-)/(N_+ + N_-)$, N_+ is the number of pulses observed in FADC chan1 when helicity is "+" in one quad

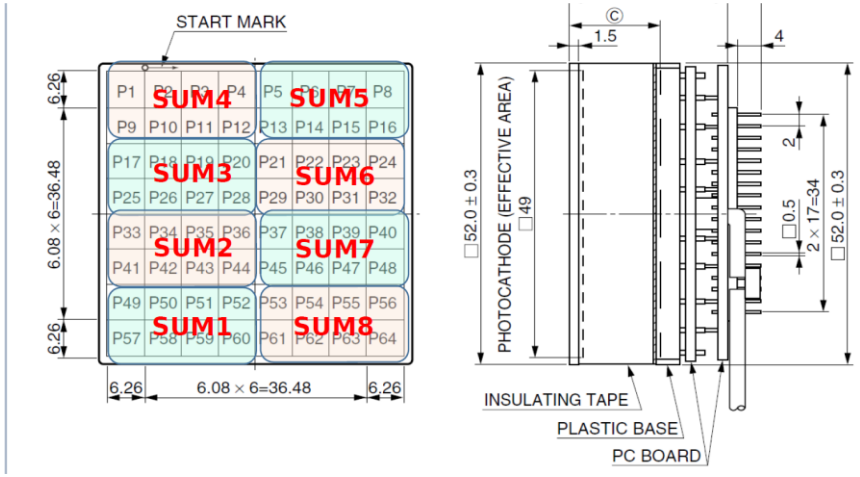


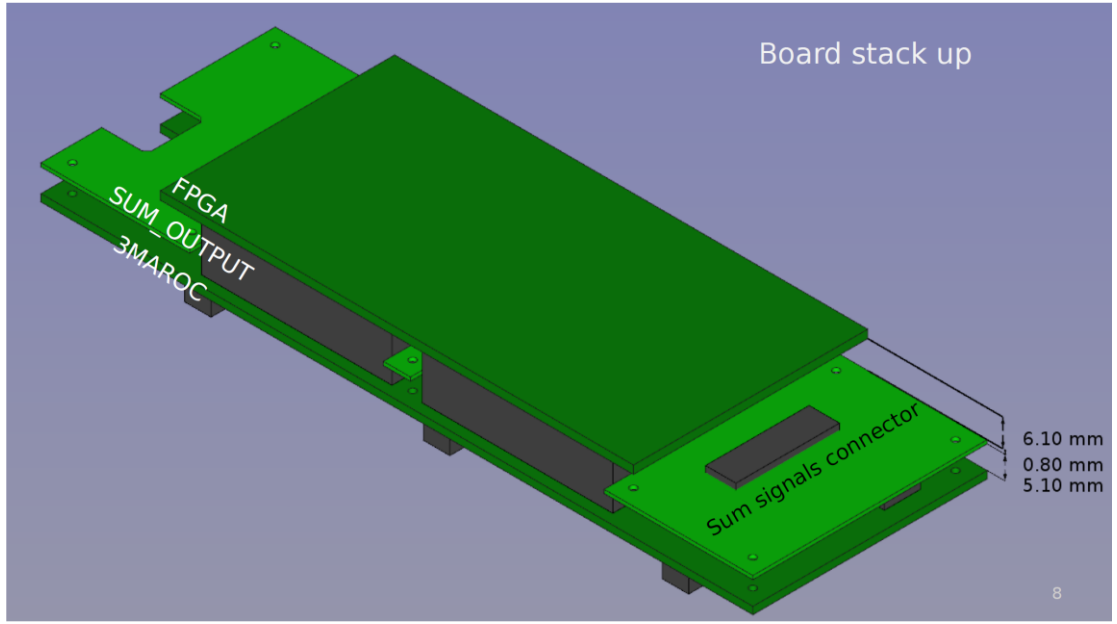
- No dead time effect in the fixed pulser generated asymmetry test

MAROC

- INFN Ferrara accepted to modify RICH board to have sum output Electronics produced and at JLab
- Being tested in Test Lab and TEDF

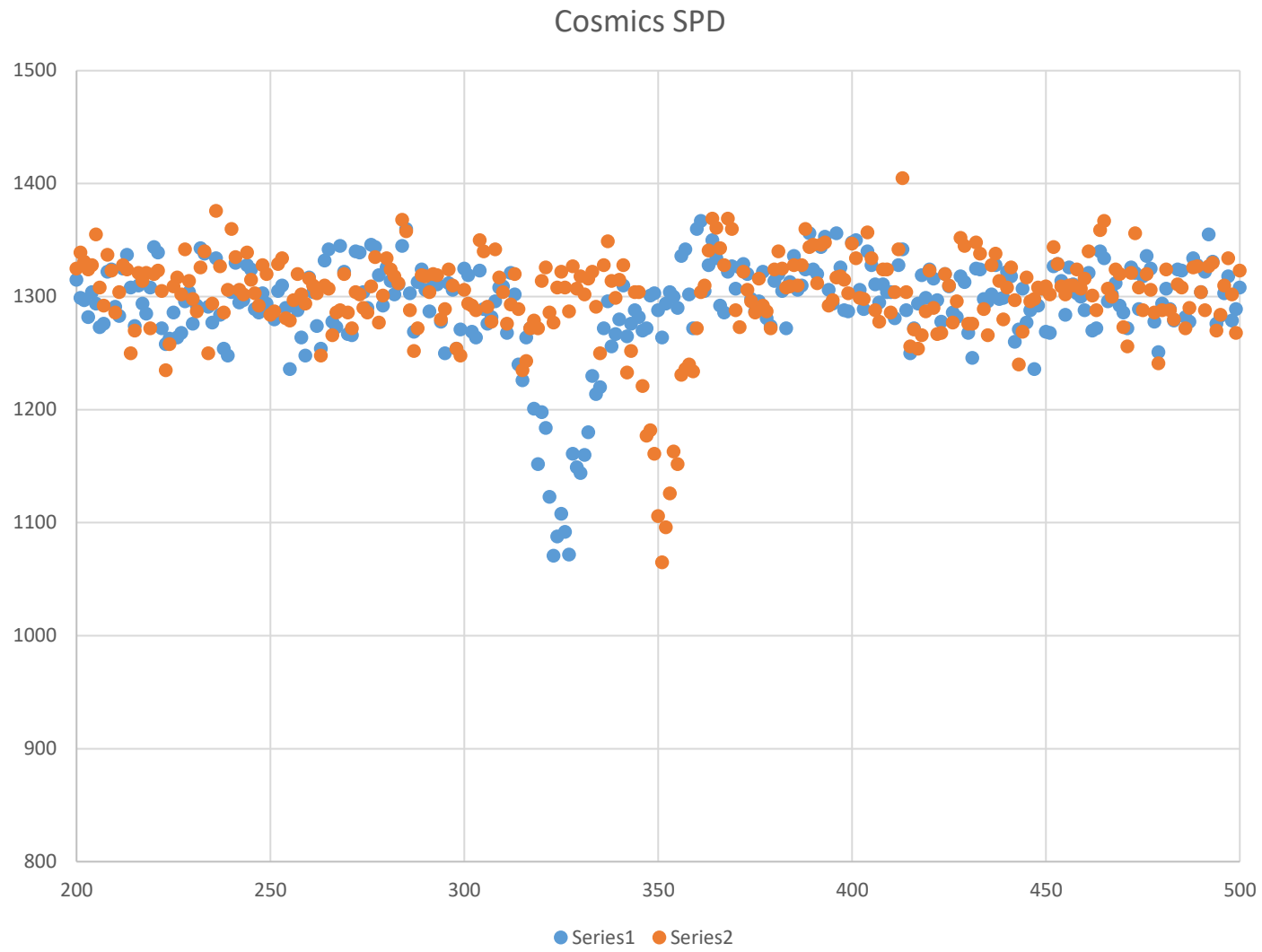






AARDVARC / ASOC

- Cosmics with ASOC in Test Lab
- SPD and 2 trigger scintillators
- Analysis cosmics data timing resolution
- Source high rate run
- AARDVARC received



Additionnal tests / developments

- Test small scale prototype during SBS or Hall C running
  - Similar to previous Cerenkov test but replace Calorimeter by SoLID Ecal and add GEM tracking
- Radiation hardness GEM VMM electronics
  - Dedicated test during SBS : replace APV25 with VMM electronics for test run
- HRS : PVDIS parasitic measurement (HRS only used for GMn calibration)
- ASIC developments
  - New VMM revision
    - Higher gain
    - Reduce dead time
    - Ability to take data with several modes at same time
    - Fix continuous mode FIFO
  - New SAMPA
    - Faster integration time (80 ns currently)
    - Radiation hardness
    - Redundancy logic for single event upset
    - Faster data transfer to be able to stream data out at 20 MHz
    - Higher sampling frequency
  - ASOC / AARDVARC : prototype board for evaluation of data transfer performances

Streaming readout option

Computer resources tracking triggered

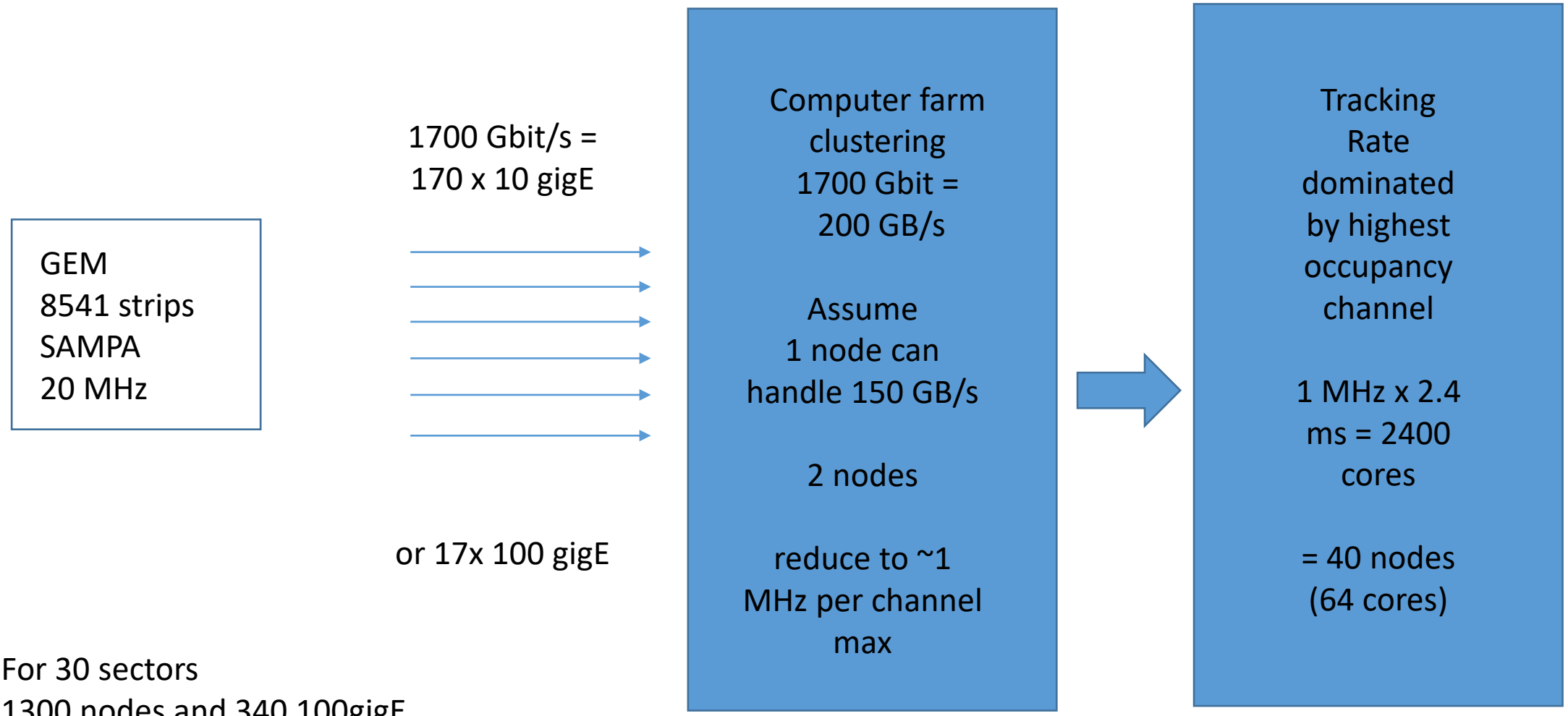
- PVDIS
  - Clustering : 0.4 ms
  - Tracking : 2 ms
  - 20 KHz x 2.4 ms= 48
  - 30 sectors = 1440 cores

- SIDIS
  - Clustering : 4.5 ms
  - Tracking : 1.7 ms
  - 100 kHz x 6.2 ms = 620 cores

SoLID GEM Streaming Readout

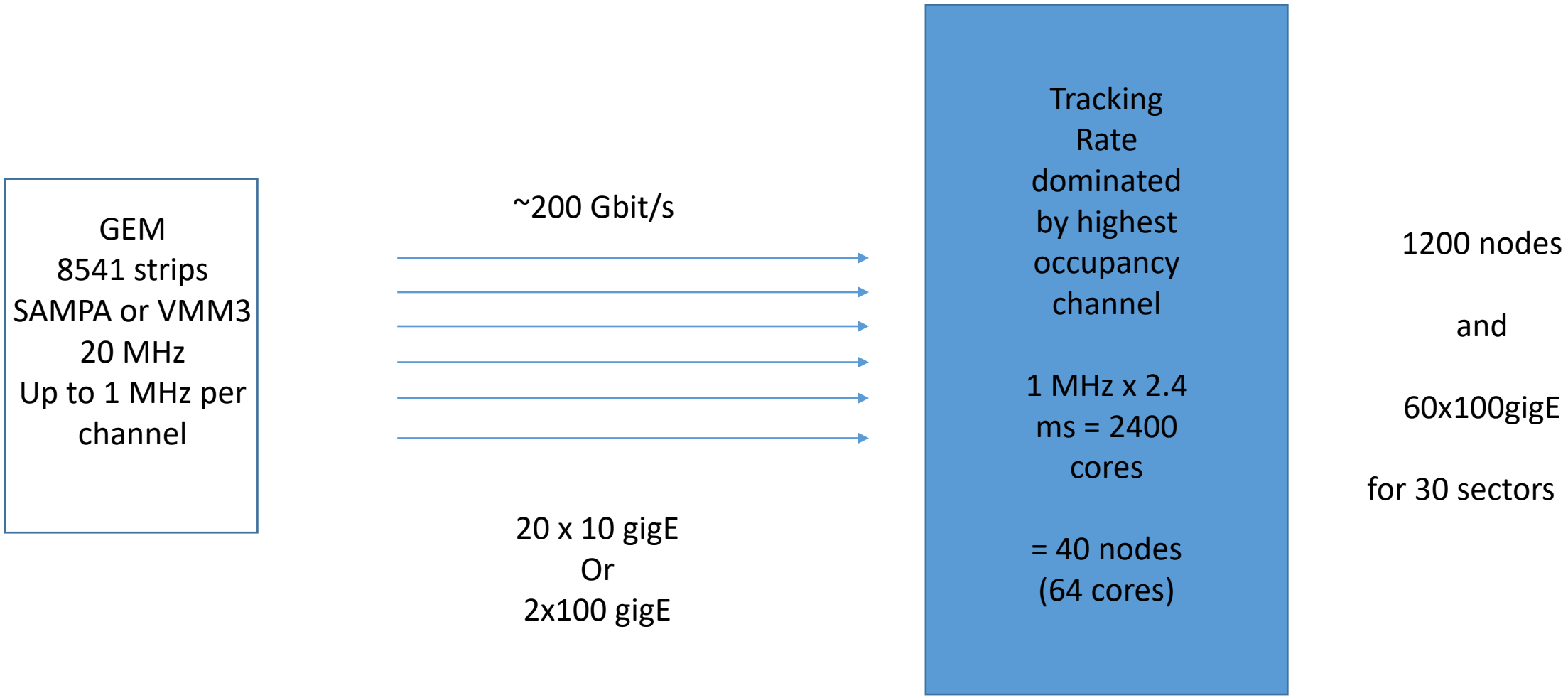
- L3 farm not included in project, seems tape silo can handle rate, triggered DAQ default solution
- Data dominated by GEM data
- Switch to VMM3 makes the system streaming capable
- PVDIS is a good candidate for streaming since sectors are independents and number of channels reduced
- SIDIS has larger event size but lower occupancy
- If computing resources available, would like to process more the data (tracking) to reduce the data size even in triggered or streaming mode

PVDIS full streaming per sector

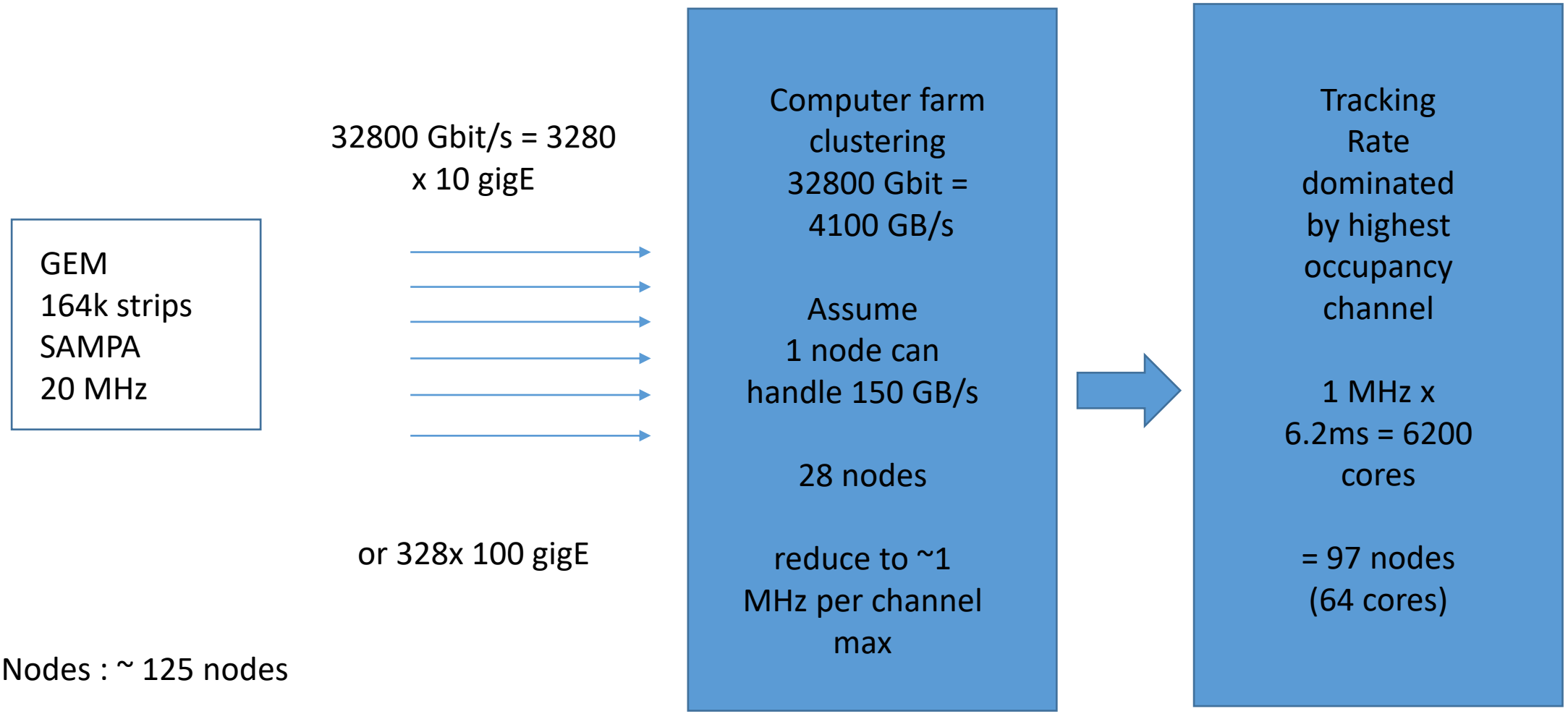


For 30 sectors
1300 nodes and 340 100gigE

PVDIS semi-streaming per sector (activate suppression on board)

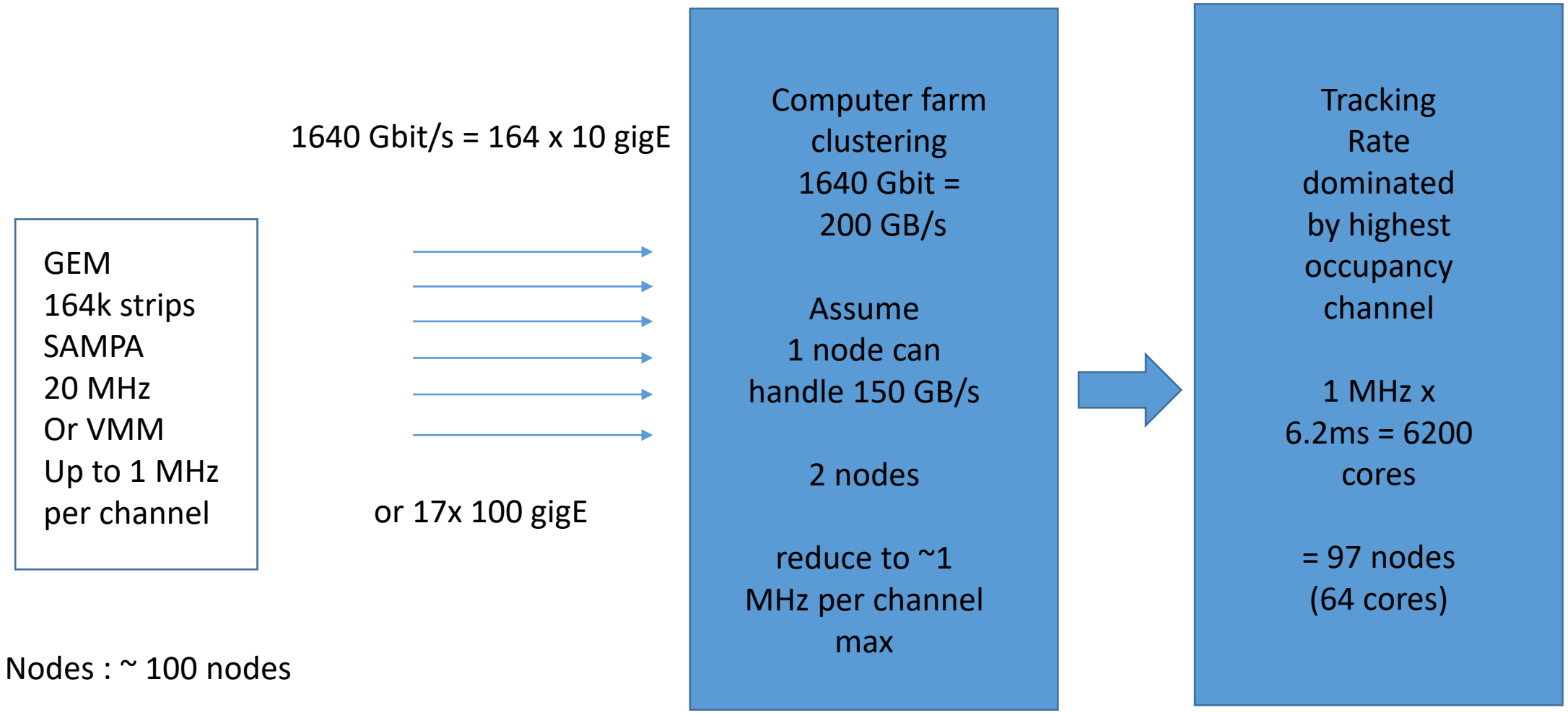


SIDIS full streaming per sector



Nodes : ~ 125 nodes

SIDIS semi-streaming per sector



Modification for streaming

- Assume 1 MHz rate max per channel (roughly 10x more rates than triggered)
- 6 bit adc, 20 bit channel, 38 bit timestamp = 64 bit / channel
- 64 bits x 64 channels at 1 MHz = 4 Gbit/s
- 1 or 2 VMM per board
- 4 x more data links

- About 4 times more electronics : 2 M$ to 8 M$

L3 and streaming option

- Online tracking L3 triggered (assume 64 core per node about 5K$)
  - PVDIS : 1440 cores ~ 200 nodes ~ 1M$
  - SIDIS : 620 cores ~ 10 nodes ~ 50 K$

- Streaming option using VMM seems doable
  - Need more data link from high occupancy
  - PVDIS ~ 72000 cores ~ 1200 ~ 7.2 M$
  - SIDIS ~6500 cores ~ 100 nodes ~ 500 K$
  - Need further study to evaluate required ressources but roughly 10 times more ressources than baseline triggered for PVDIS
  - Reasonable for SIDIS

Conclusion

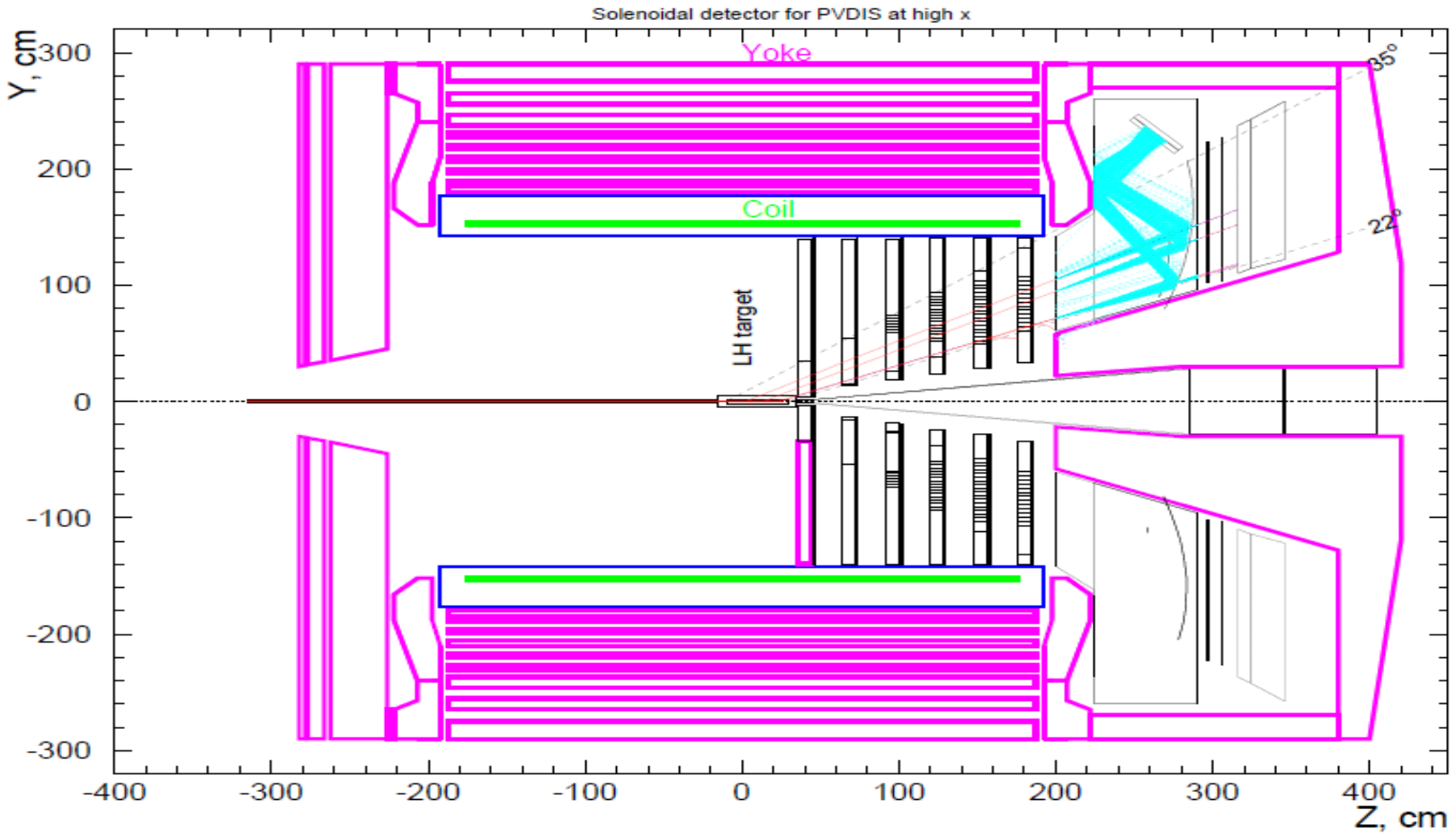
- PreRD ongoing
  - VMM prototype board almost complete
  - APV MPD VTP readout and FADC ~ summer 2021
  - Asymmetry setup at UMass
  - MAROC testing ongoing
  - SPD taking cosmics
- Additional testing
  - Beam test all subsystems
- development possible
  - GEM ASIC development
  - Radiation testing
- Online tracking triggered with L3
  - PVDIS : 1440 cores
  - SIDIS : 620 cores
- Streaming option using VMM seems doable
  - Need more data link from high occupancy
  - PVDIS : ~ 72000 cores ~ 1200 nodes
  - SIDIS ~6500 cores ~ 100 nodes
  - Cost increase 2M$ to 12 M$ with current costs
- Need simulation and software work to refine number

Backup

SoLID requirements

Experiments	PVDIS	SIDIS-^{3}He	SIDIS-Proton	J/ψ
Reaction channel	$p(\vec{e},e')X$	$(e,e'\pi^{\pm})$	$(e,e'\pi^{\pm})$	$e+p \rightarrow e'+J/\Psi(e^-,e^+)+p$
Approved number of days	169	125	120	60
Target	LH_2/LD_2	^{3}He	NH_3	LH_2
Unpolarized luminosity ($cm^{-2}s^{-1}$)	$0.5\times10^{39}/1.3\times10^{39}$	$\sim 10^{37}$	$\sim 10^{36}$	$\sim 10^{37}$
Momentum coverage (GeV/c)	2.3-5.0	0.8-7.0	0.8-7.0	0.6-7.0
Momentum resolution	~2%	~2%	~2%	~2%
Polar angle coverage (degrees)	22-35	8-24	8-24	8-24
Polar angle resolution	1 mr	0.6 mr	0.6 mr	0.6 mr
Azimuthal angle resolution	-	5 mr	5 mr	5 mr
Trigger type	Single e^-	Coincidence $e^-+\pi^{\pm}$	Coincidence $e^-+\pi^{\pm}$	Triple coincidence $e^-e^-e^+$
Expected DAQ rates	<20 kHz $\times$ 30	<100 kHz	<100 kHz	<30 kHz 100 kHz?
Backgrounds	Negative pions, photons	($e,\pi^-\pi^{\pm}$) ($e,e'K^{\pm}$)	($e,\pi^-\pi^{\pm}$) ($e,e'K^{\pm}$)	BH process Random coincidence
Major requirements	Radiation hardness 0.4% Polarimetry π^- contamination Q^2 calibration	Radiation hardness Detector resolution Kaon contamination DAQ	Shielding of *sheet-of-flame* Target spin flip Kaon contamination	Radiation hardness Detector resolution

Detector layout and trigger for PVDIS



Trigger

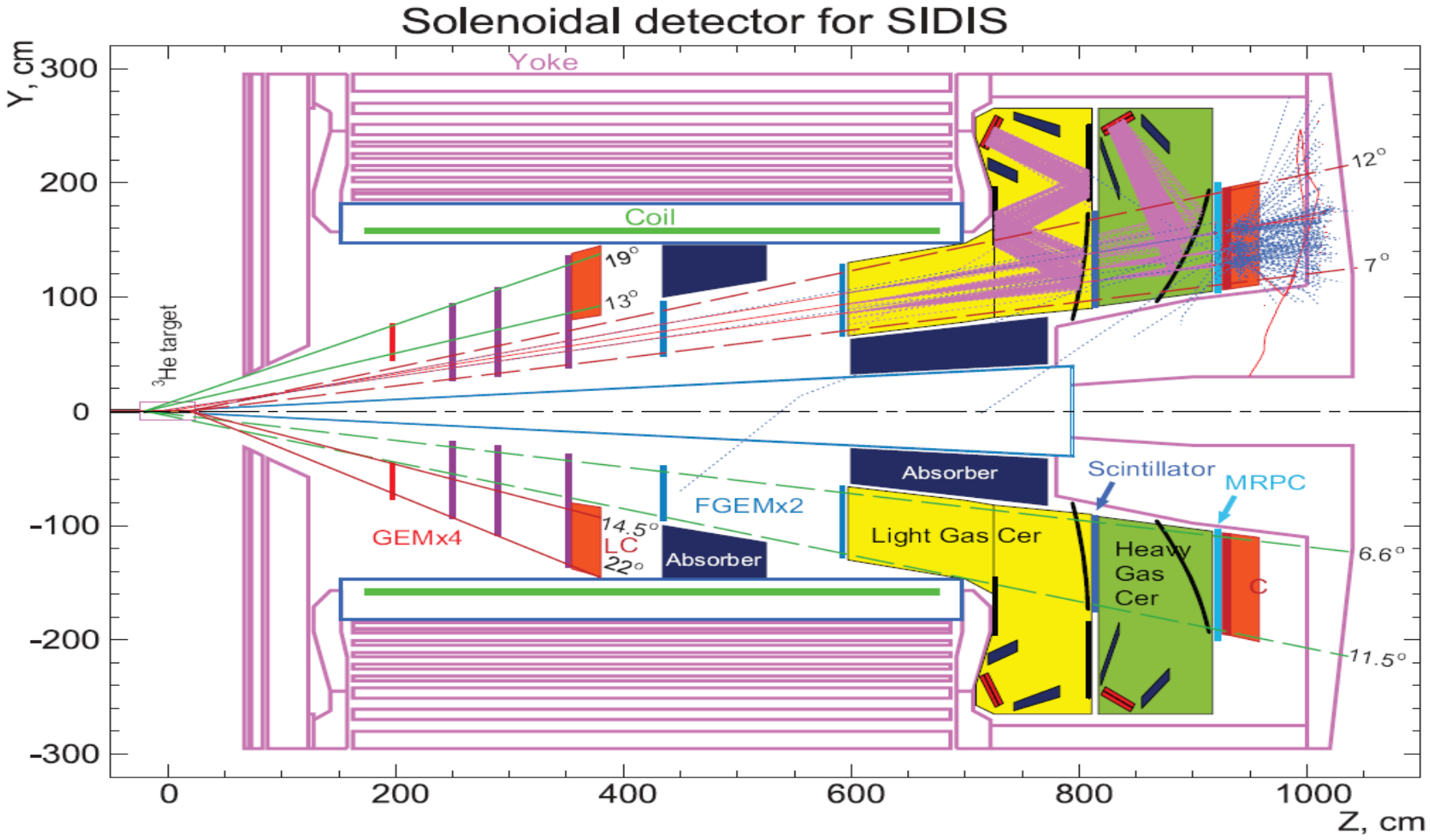
Calorimeter
+
Cerenkov

200 to 500 KHz of electrons

30 individual sectors

Max 17 KHz/sector

Detector layout and trigger for SIDIS



Trigger

Calorimeter
+
Cerenkov
+
SPD

30 sectors
Combined
in
10 regions of interests
Max rate 200 KHz

Baseline 60 KHz
coincidence e- pion

Updated data rates using VMM data format and occupancies

- 6 bit ADC and up to 400 ns time window (160 MHz clock = ~65 clock cycles)
- Add channel and chip ID
- Timestamp

VMM event format		Time stamp 250 MHz		VMM ID	VMM channel	Fine time	Amplitude
bit		48		14	4	7	7

- 8 bytes per channel

New Data rates PVDIS

PVDIS	30000 kHz						
		Total strips	Occupancy %	strips fired	event size bytes (time + amplitude)		data rate (MB/s)
1		34740	16.2	5627.88	22513.52		675.4056
2		41280	8.3	3426.24	13706.96		411.2088
3		41280	7.1	2930.88	11725.52		351.7656
4		68400	2.7	1846.8	7389.2		221.676
5		70560	2.7	1905.12	7622.48		228.6744
		256260	37	15736.92	62957.68	GEM rate	1888.7304
						FADC	176
						Total	2064.7304

New Data rates SIDIS

SIDIS He3	200000 KHz						
		Total strips	Occupancy %	strips fired	event size bytes (time + amplitude)		data rate (MB/s)
1		27120	1.8	488.16	1954.64		390.928
2		30540	5.5	1679.7	6720.8		1344.16
3		34920	2.5	873	3494		698.8
4		42060	1.6	672.96	2693.84		538.768
5		31140	1.6	498.24	1994.96		398.992
6		38340	1.2	460.08	1842.32		368.464
		204120	14.2	4212.06	16858.24		3371.648
						FADC	300
						Total	3671.648

1.8 GB/s at 100 KHz

New Data rates J/Psi

JPsi	100000						
		Total strips	Occupancy %	strips fired	event size bytes (time + amplitude)		data rate (MB/s)
1		27120	5.4	1464.48	5859.92		585.992
2		30540	9.7	2962.38	11851.52		1185.152
3		34920	6.1	2130.12	8522.48		852.248
4		42060	4.8	2018.88	8077.52		807.752
5		31140	4.3	1339.02	5358.08		535.808
6		38340	3.3	1265.22	5062.88		506.288
		204120	33.6	9914.88	39669.52		3966.952
						FADC	300
						Total	4266.952

Similar data rates as APV25 for Jpsi, slightly lower rate for PVDIS and SIDIS

VMM3 prototype board development (Ed)

FPGA for VMM Direct Readout

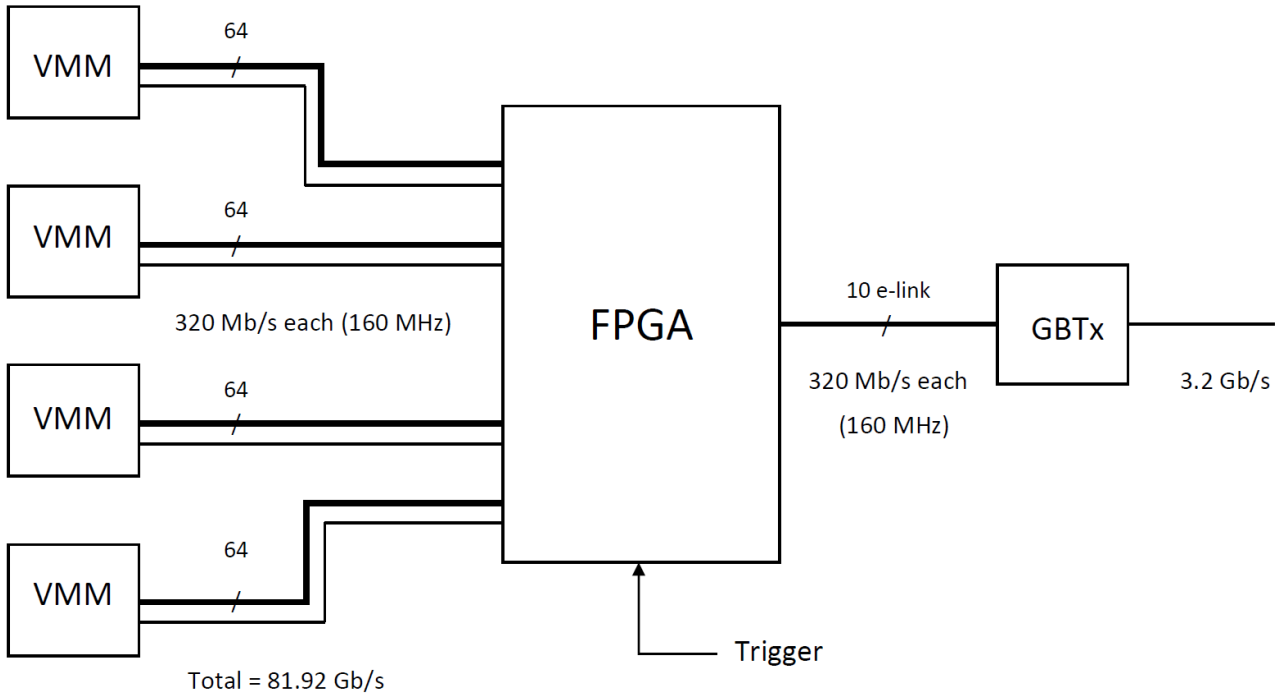
(E.J. 5/28/20)

Proposal

1 FPGA handles direct readout of 4 VMM chips

[64(channels/chip) + 1(clock/chip)] x 2(pins/signal) x 4(chips) = 520 pins (reasonable size, price FPGA)

1 GBTx data link for FPGA output data (10 e-links @ 320 Mb/s = 3.2 Gb/s)



1

VMM3 prototype board development (Ed)

Trigger rate (max) = (3200 Mb/s) / (4656 + w*r*3072 b)

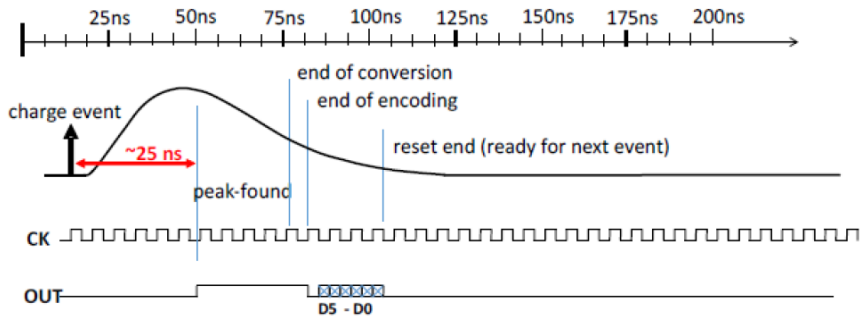
e.g. r = 10 MHz, w = 0.400 µs => Trigger rate (max) = 189 KHz

r = 15 MHz, w = 0.400 µs => Trigger rate (max) = 139 KHz

Or we can solve for the quantity w*r:

R = trigger rate (MHz)

w(µs)*r(MHz) = 1.04166 / R(MHz) - 1.51563



VMM 6-bit ADC Direct Output timing

VMM3 prototype board development (Ed)

- Direct readout with 15 MHz and 400 ns window gives 139 KHz trigger rate capability sufficient for PVDIS and SIDIS, most likely can reach 200 KHz if more segmentation and shorter window applicable

- Simulation of direct outputs by Jinlong ongoing

- Possible issues :
  - Low resolution ADC direct readout not good enough for high rate strips (PVDIS), instrument small angle with APV25 from SBS

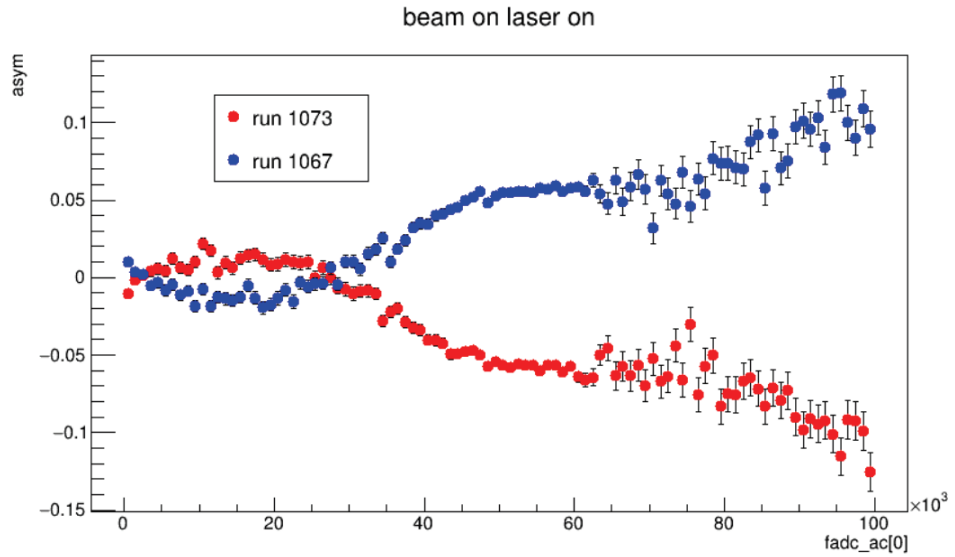
Preliminary results from Compton

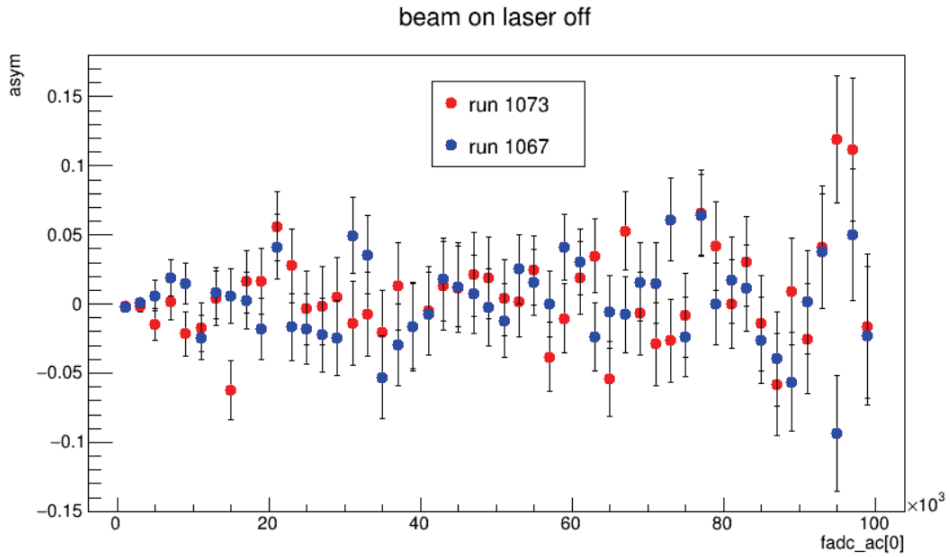
- FADC + VETROC + VTP (trigger module)
- Implemented delayed helicity readout
- Helicity scaler with VETROC and VTP for normalization (deadtime, power, position)
- Photon (and electron trigger)

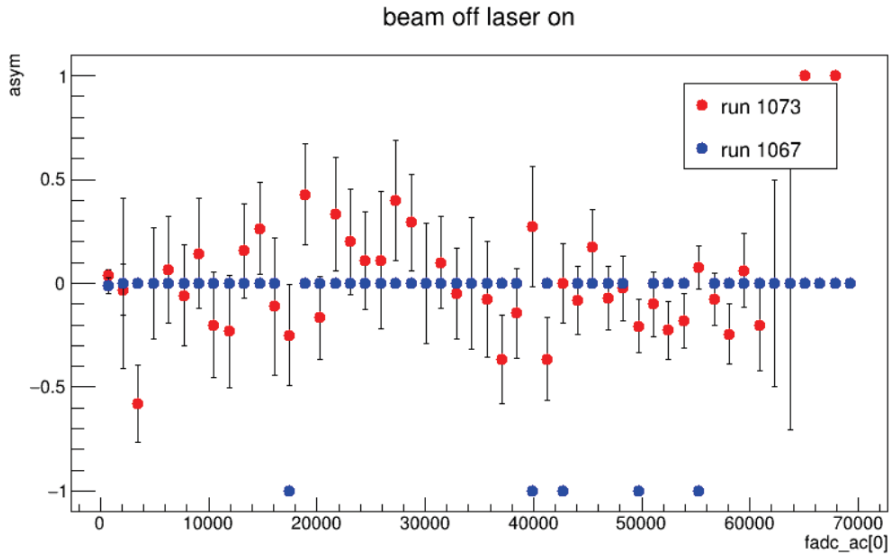
- Software

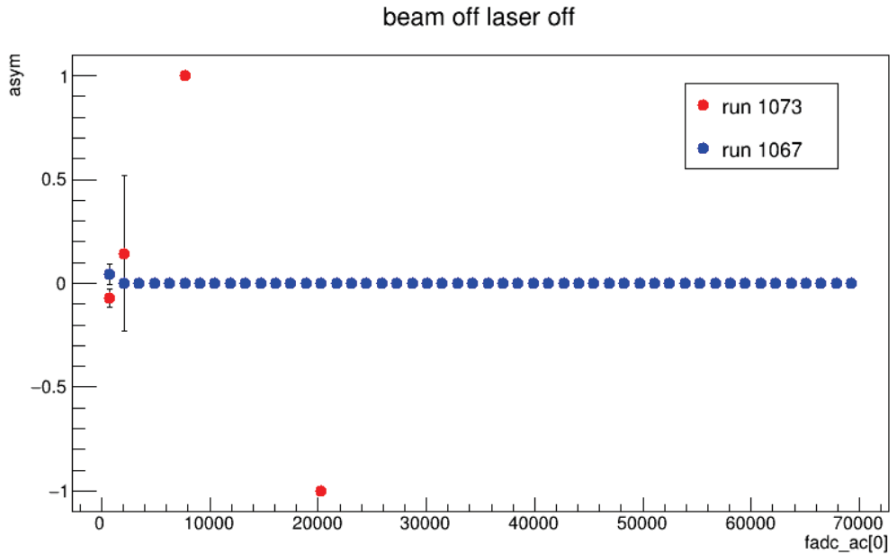
Preliminary results from Compton

- Rates up to 50 KHz with deadtime of about 10%
- Compton Asymmetry from Photon







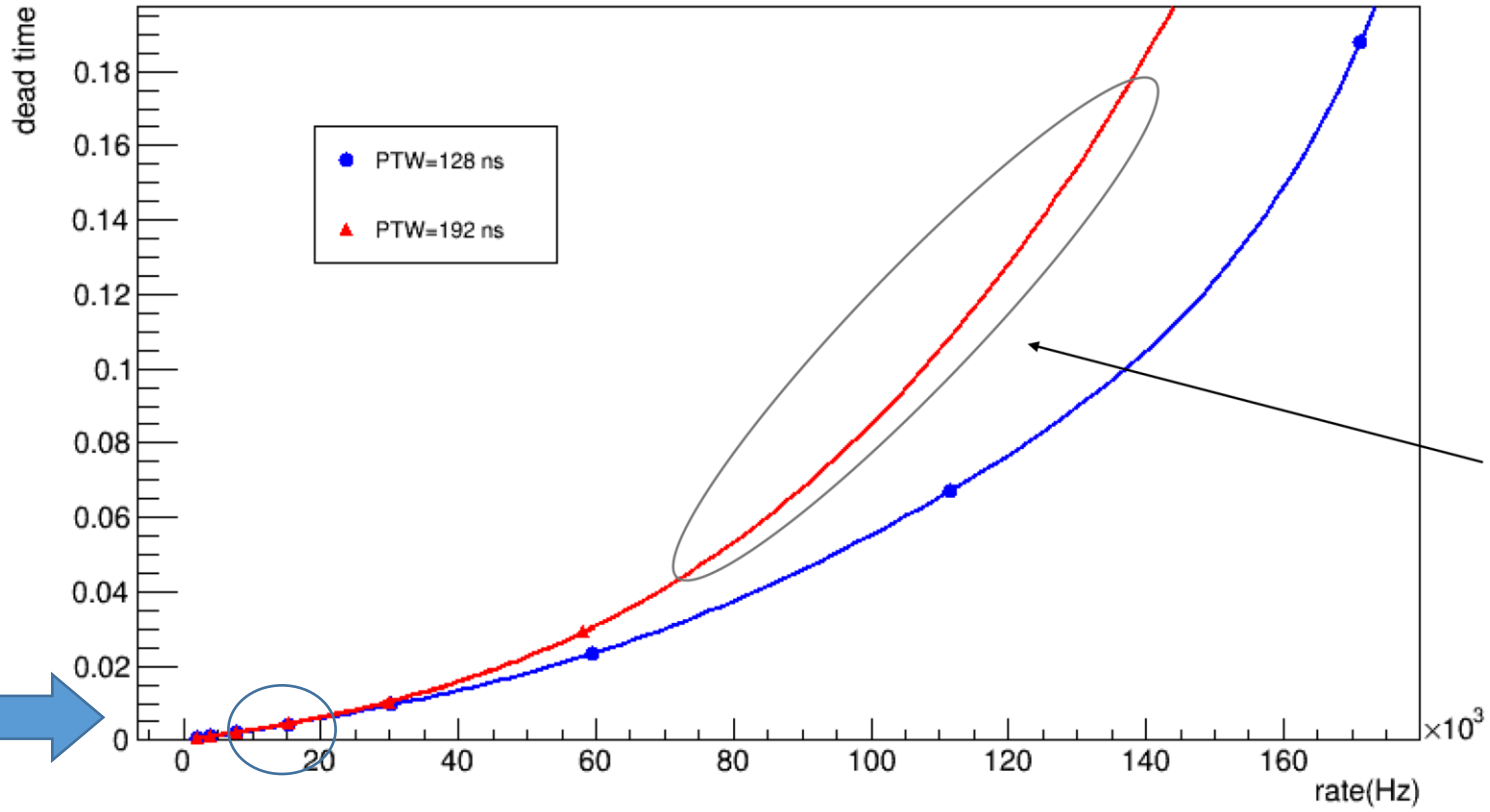


FADC

Dead time for raw mode (mode 1) (Narrow pulse)

Blocklevel=40 Bufferlevel=10

Compare the dead time when using different window width



Note: When PTW=192 ns, due to the data transfer limit (1Gb/s), the highest rate it can reach is 75 kHz;

So the projection may not be right.

1%
At 20 KHz

Improved with fast VXS readout and network upgrade to 10 gigE