SoLID preRD VMM update

01/31/202w

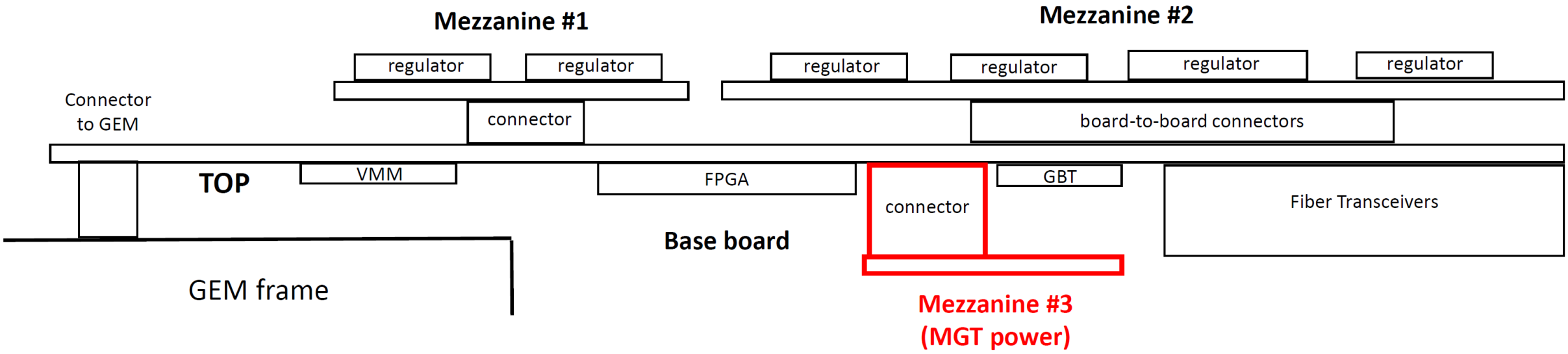
VMM prototype board status

VMM prototype update – 1/27/22

- VMM base board
  - Finalizing layout
  - Finished most difficult section – VMM power filtering (6 Inductors + 40 caps for **each** VMM) - (with minimal space; a work of art)
  - 16-layer PCB
  - JW doing final passes with autorouter – 128 differential pairs from VMMs to FPGA requires many routing layers (need stripline for controlled impedance, driving up plane layer count)
  - Change - moved 3 power regulators for MGT transceiver of FPGA (Ethernet) to *another* mezzanine card
    - Originally these regulators were planned to be on FPGA power mezzanine but ran out of space and connector pins; moved to base board
    - Move off base board frees up space and reduces base board complexity
    - These components are only used for Ethernet – would be damaged if base board was exposed to high radiation
    - Can simply unplug card when forced to use rad hard GBT data link
    - New mezzanine card designed and ordered already

- Plans for base board (among many possible)
  - **Plan 1** – 6 PCBs, assemble 4
    - If everything works we're done – 512 channels to play with
    - If design or circuit board has minor problems, we'll probably live with it for a while due to cost
    - If design or circuit board has major problems, components (VMM, FPGA, GBT, GBT-SCA) can be retrieved but must be re-balled (BGA)
    - Direct output functionality of VMM chips we use have NOT been tested. Might wind up no direct outputs or missing channels. Replacing a VMM chip on the board is difficult due to high density of power filtering components around it.
  - **Plan 2** – 6 PCBs, assemble 2. Board #1 with 2 VMMs, Board #2 with 1 VMM + BGA socket
    - If everything works we have 256 channels to play with – plenty to learn with. Assemble 2 more boards when satisfied with performance. Re-spin if not.
    - If design or circuit board has major problems, impact is less; components need not be recovered
    - Can test direct output functionality of all VMM chips before assembling onto all future boards built

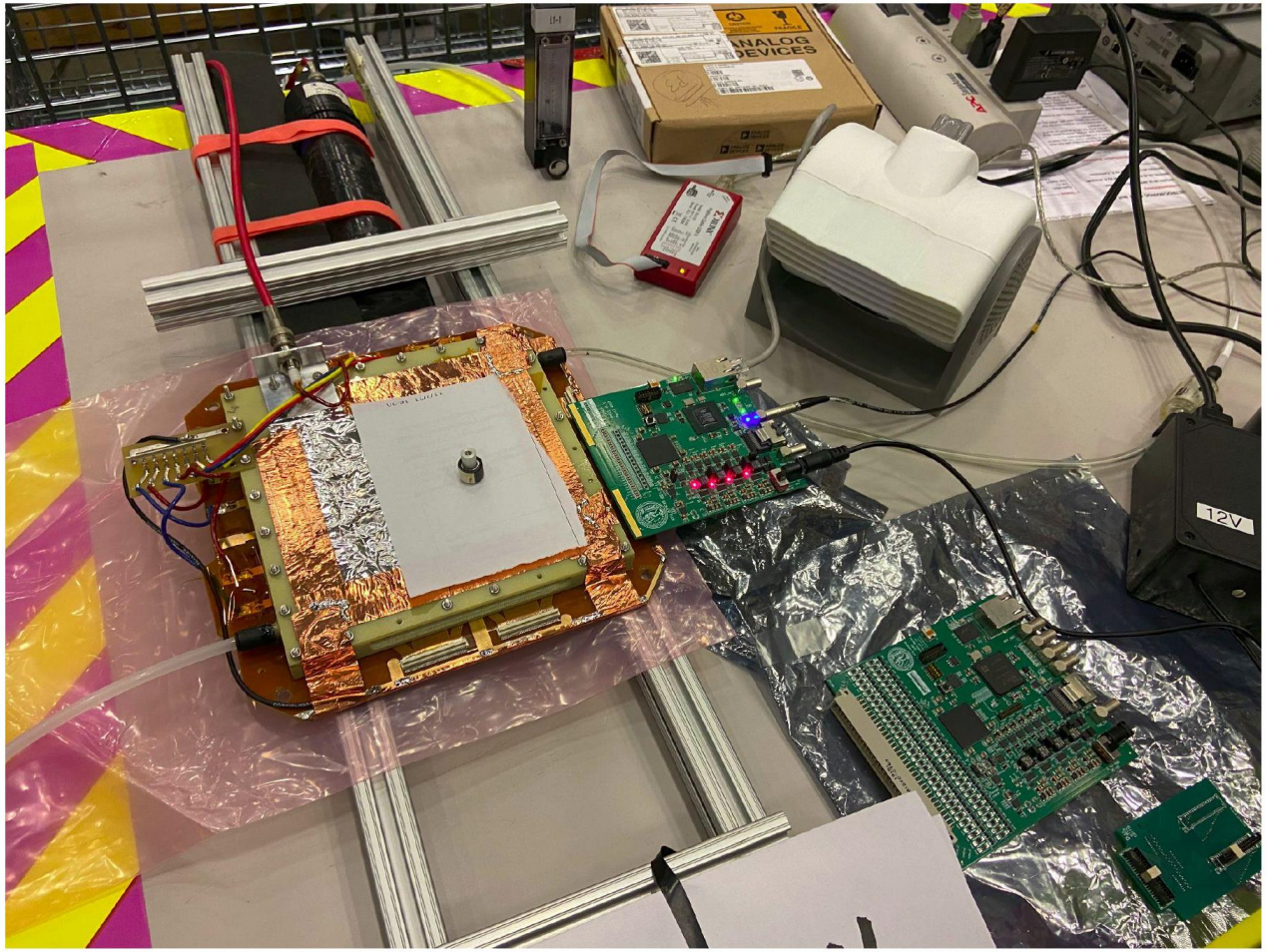
VMM layout


Mezzanine #1
Mezzanine #2
regulator
regulator
regulator
regulator
regulator
Connector
to GEM
connector
board-to-board connectors
TOP
VMM
FPGA
GBT
connector
Fiber Transceivers
Base board
GEM frame
Mezzanine #3
(MGT power)

VMM prototype testing

Test Setup

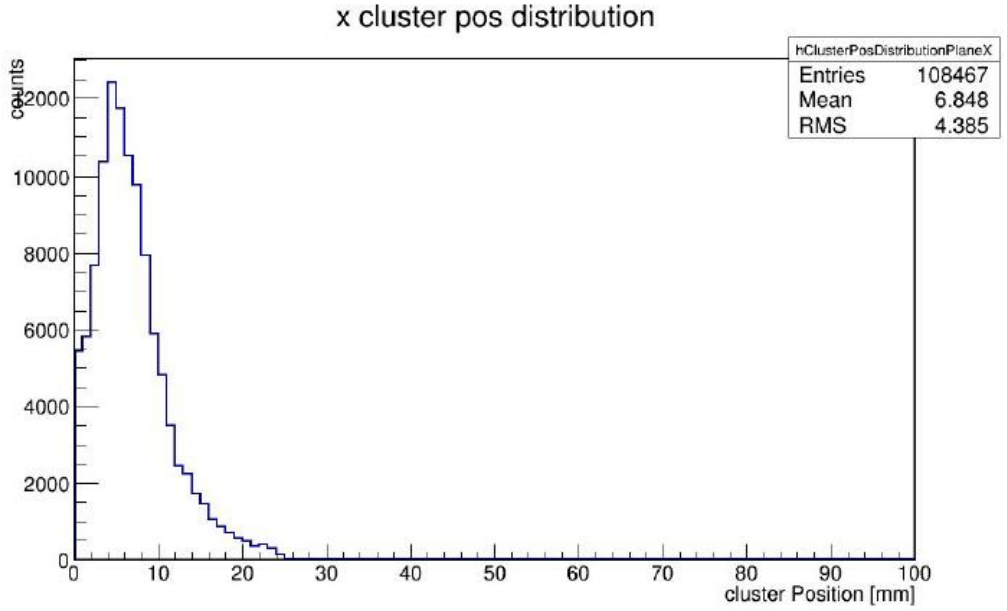
- Fe55 source on top of the GEM chamber
- One VMM test board connected to the chamber
- The 2nd VMM board needs a converter
- Continuous mode, self triggering
- 10-bit ADC
- VMM channel gain was set to 3.0 mV / fC

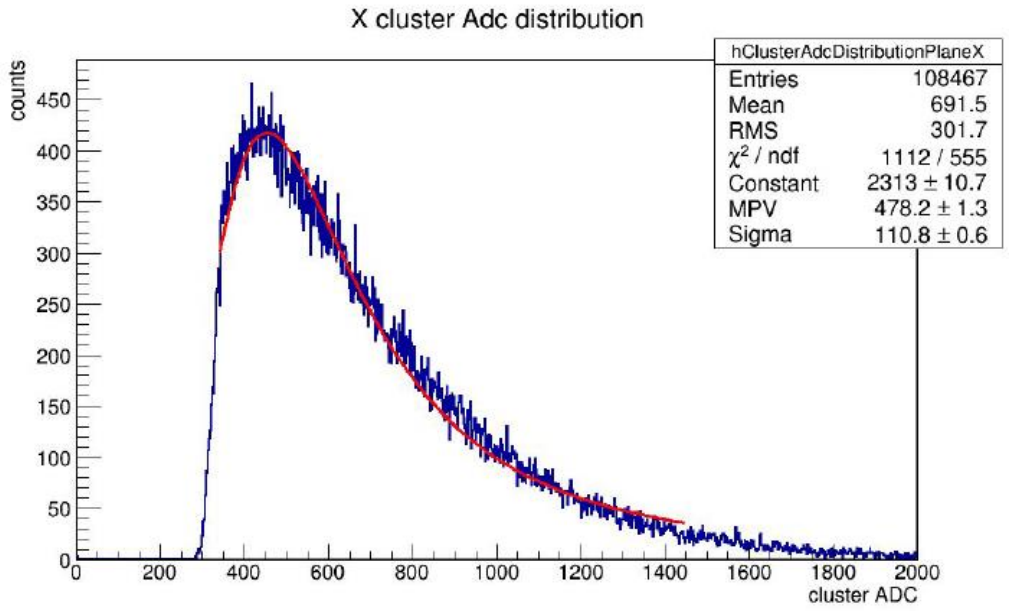


Fe55 signal

Test Results

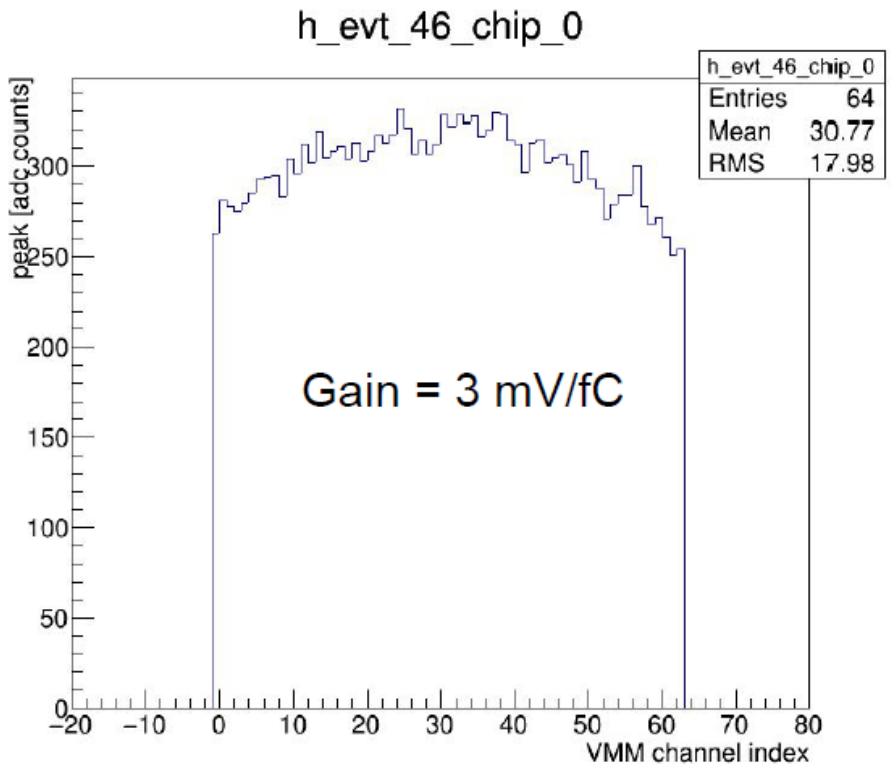
- One VMM board covers about 25.6 mm length (64 channels X 0.4 mm pitch)

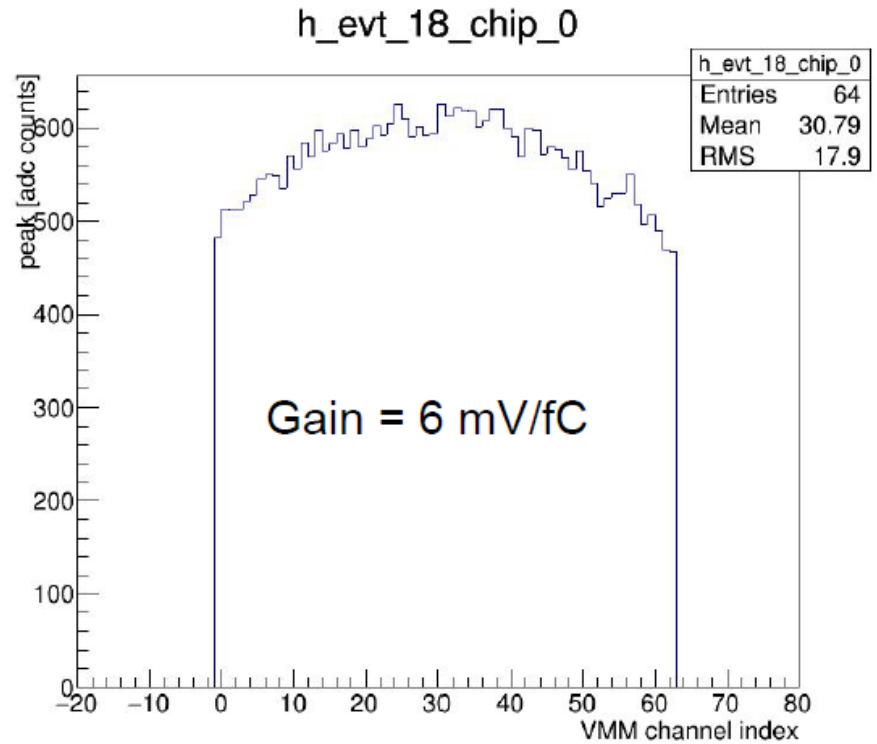




Pulser Test

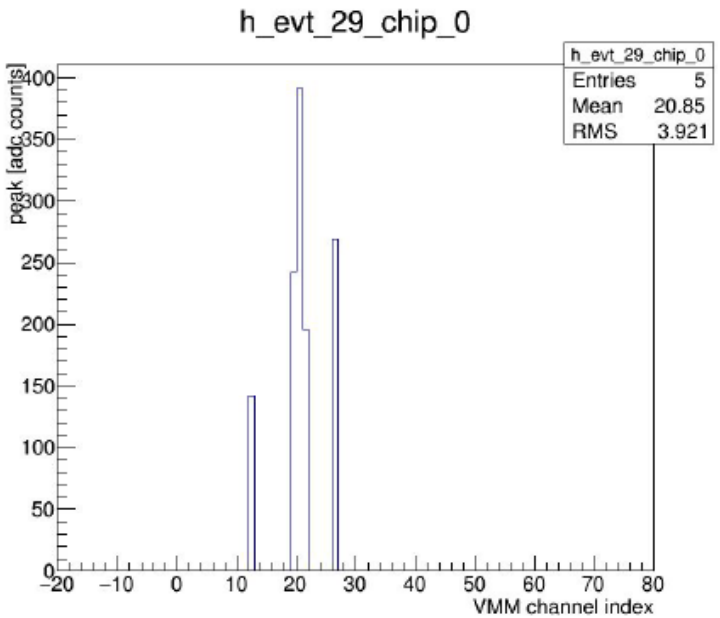
- Purely to test electronics, no GEM detector
- Use internal pulser (CKTP) to assert a pulse to each channel's input capacitor
- The pulse was set to 300 ADC using the VMM's DAC to convert to amplitude
- Try different gain
- Seems with gain = 3 mV/fC, no extra amplification

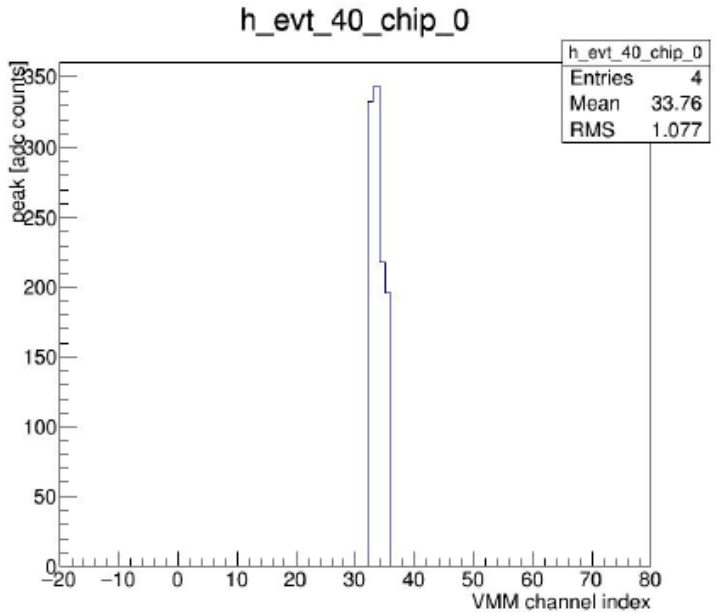


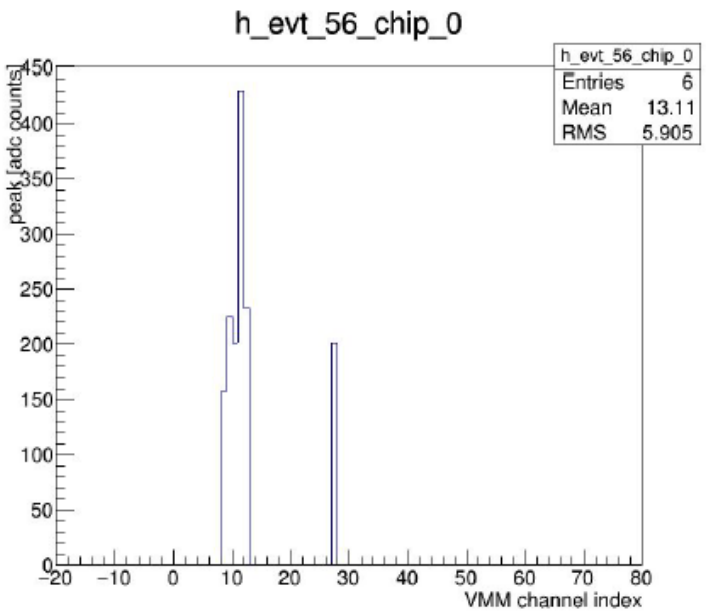


Signal

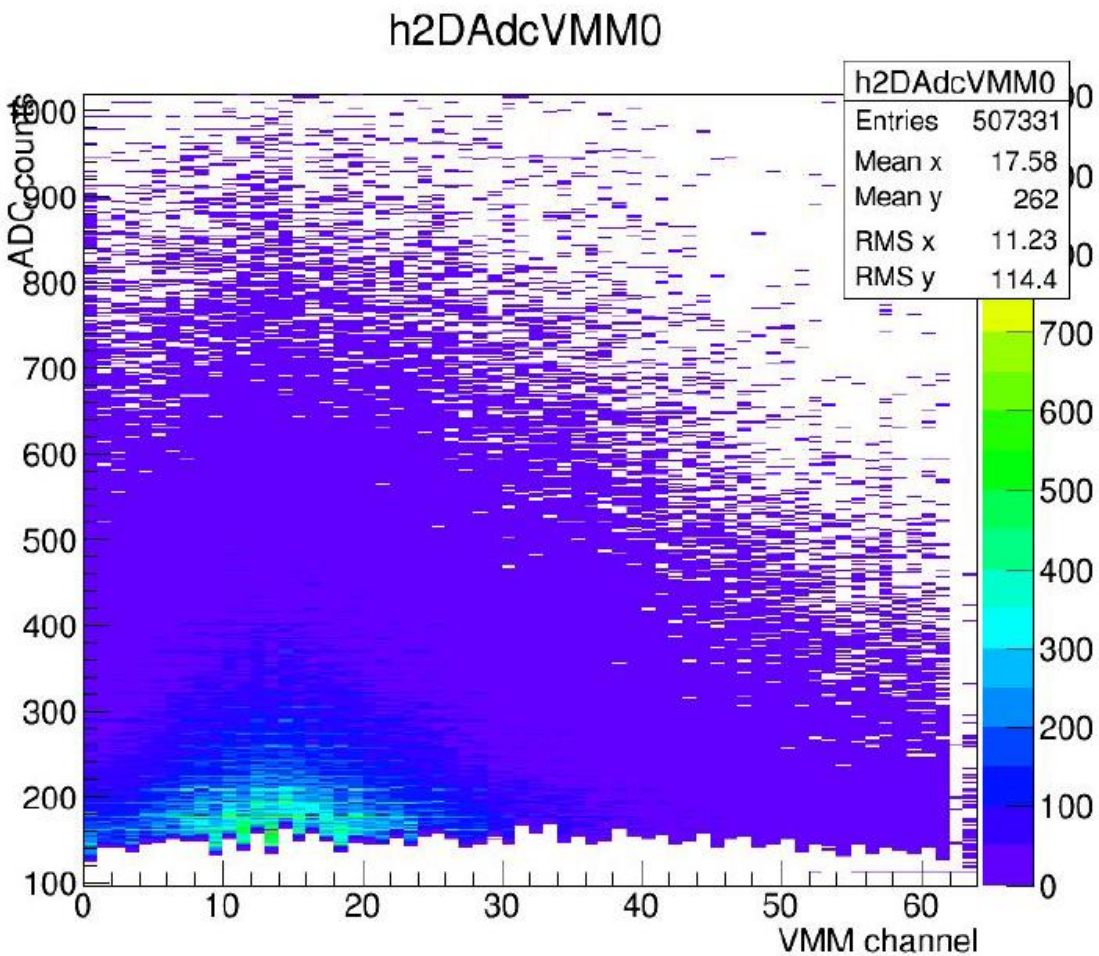
- Fe55 signals from GEM chambers
- Set a overall threshold, channels with ADC < threshold have no output
- A few signals

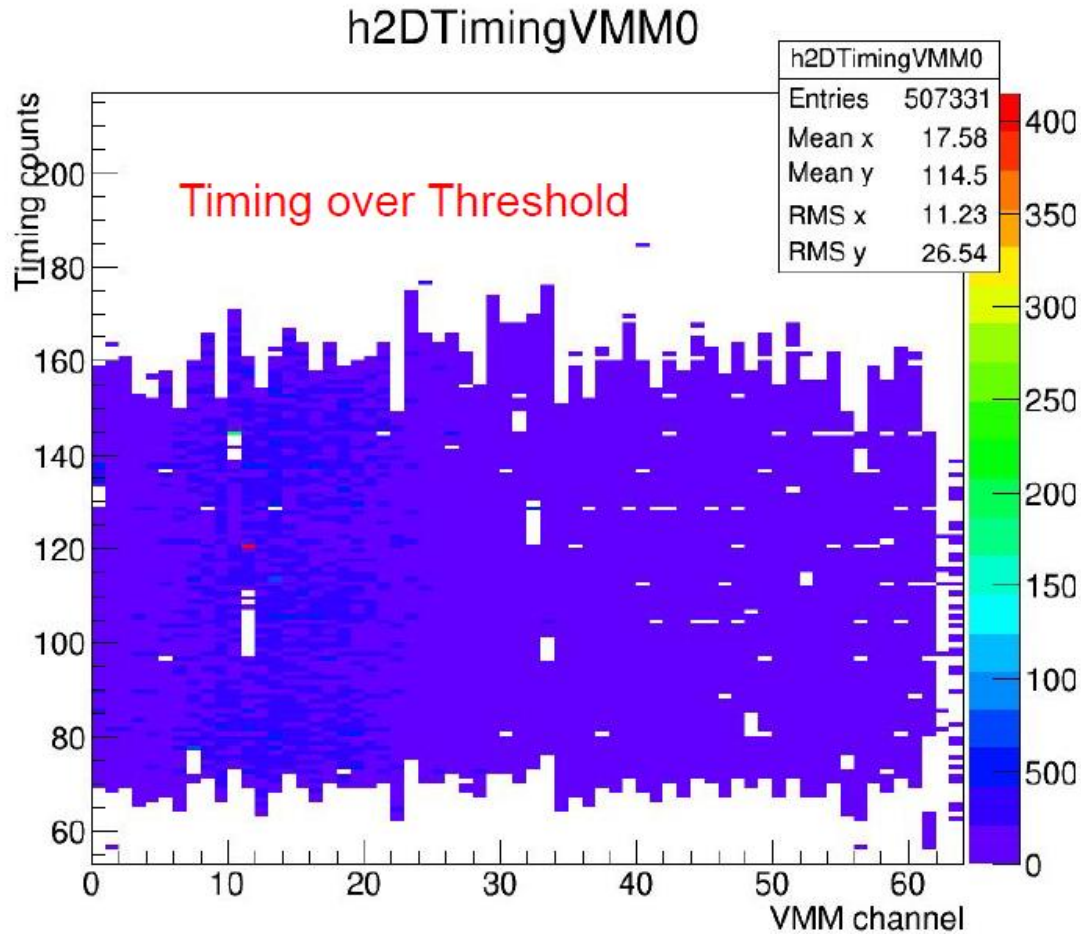




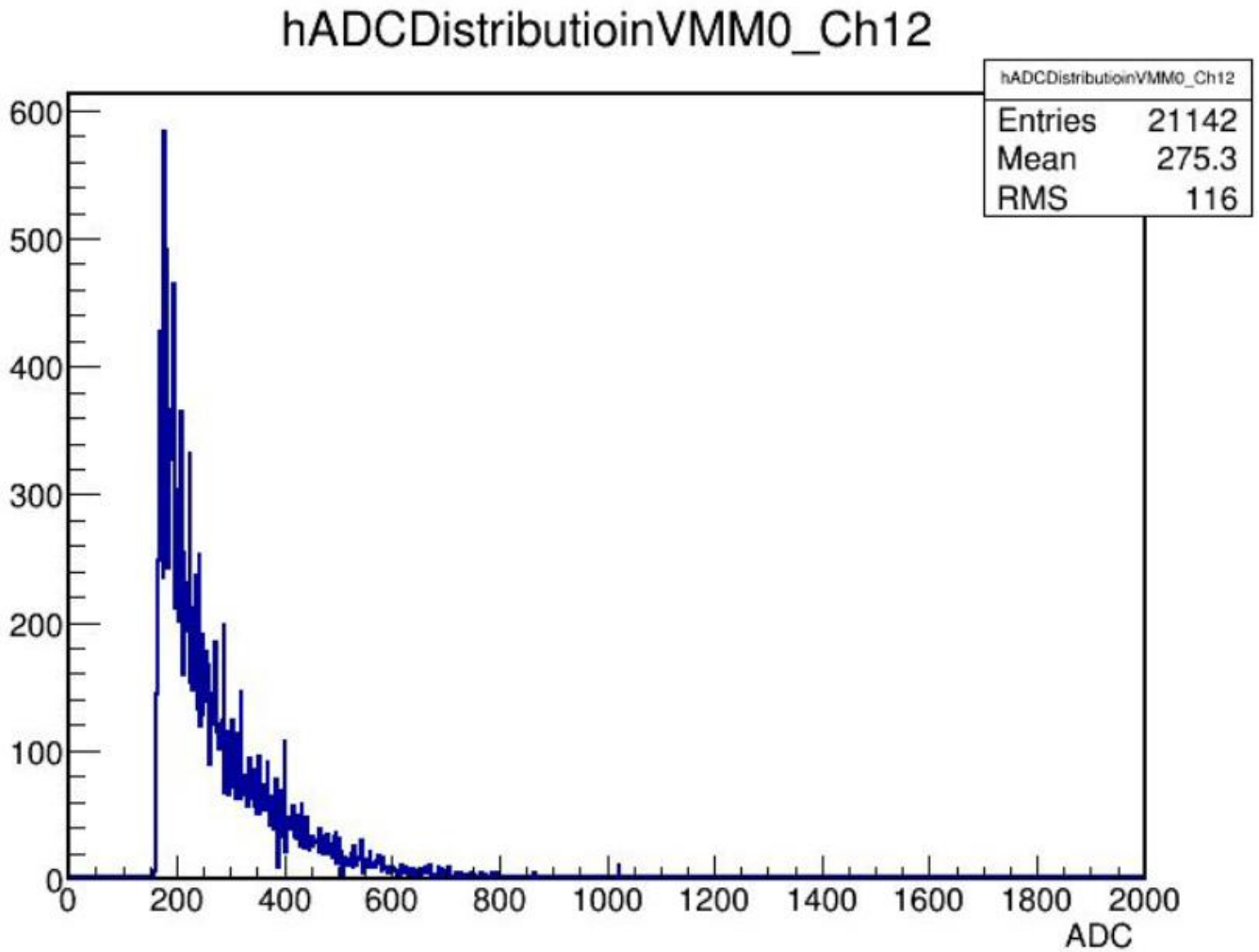


ADC, Timing Distribution Per Strip





ADC distribution for VMM channel 12



Fe55 expected spectrum

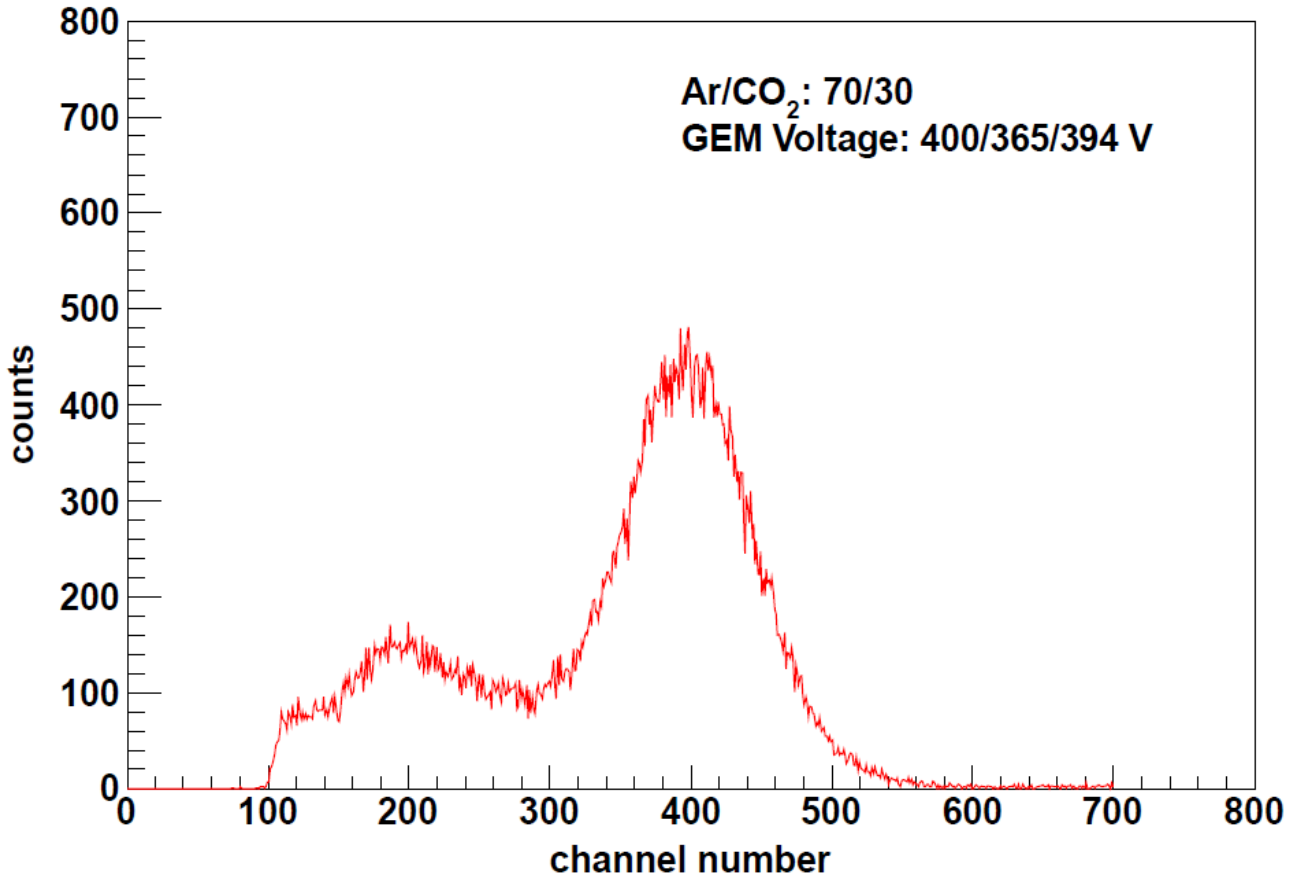


Figure 1: Fe^{55} X-ray spectrum obtained with triple GEM detector.

Plan

- Prototype board
  - Delivery mid February
  - Source testing : ~3 days
  - Cosmics UVA :~1 week
- Evaluation board
  - Test different gain / shaping time with Fe 55 and Sr90 : ~ 1 week to get SNR
  - Test 6 bit ADC direct output ~1 week