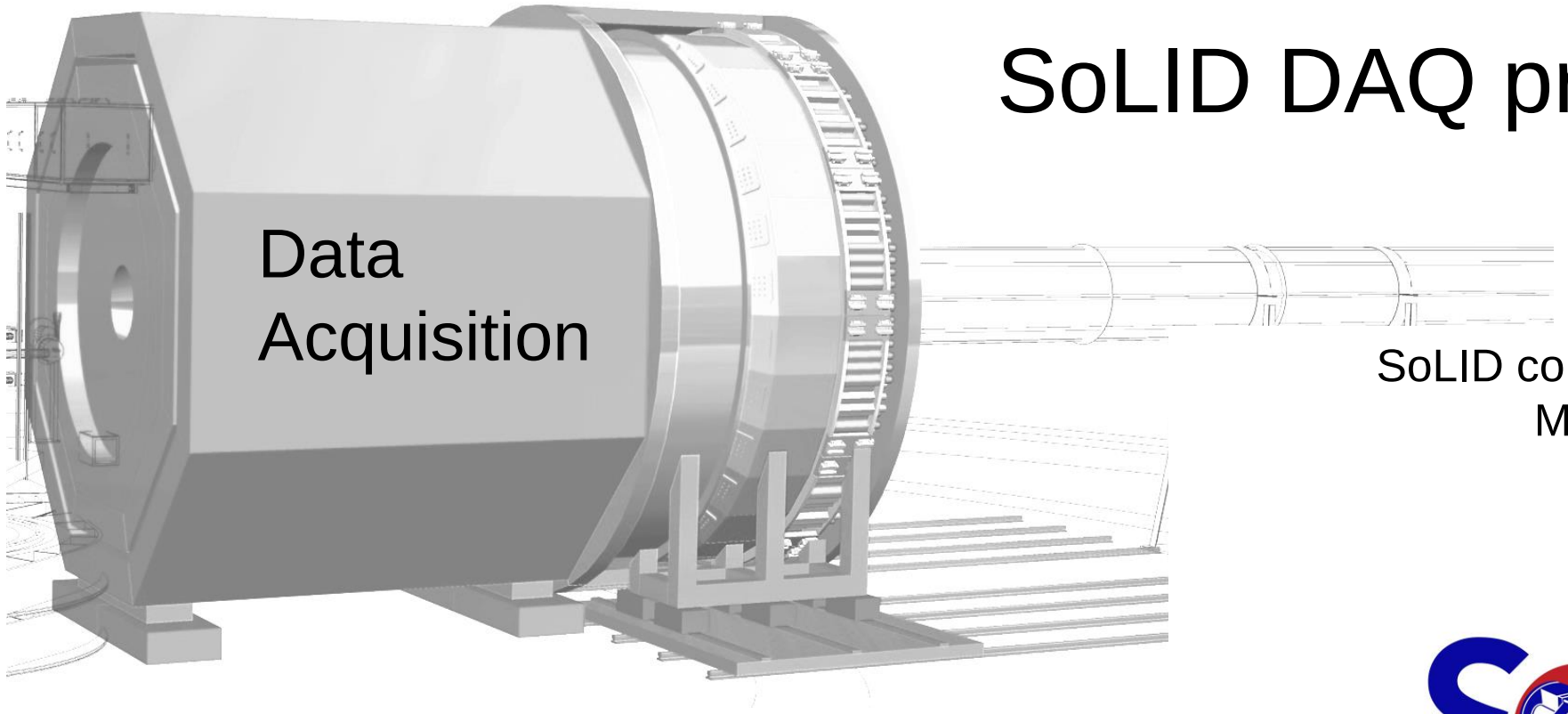


SoLID DAQ preRD

SoLID collaboration meeting
May 8th 2023

Alexandre Camsonne

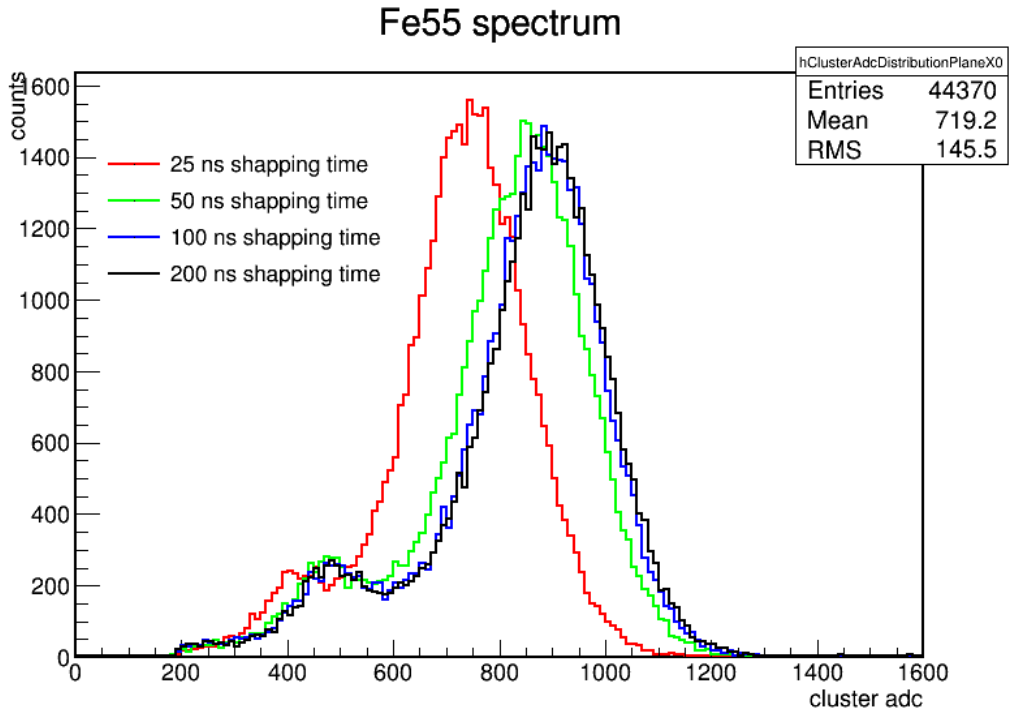
- Outline

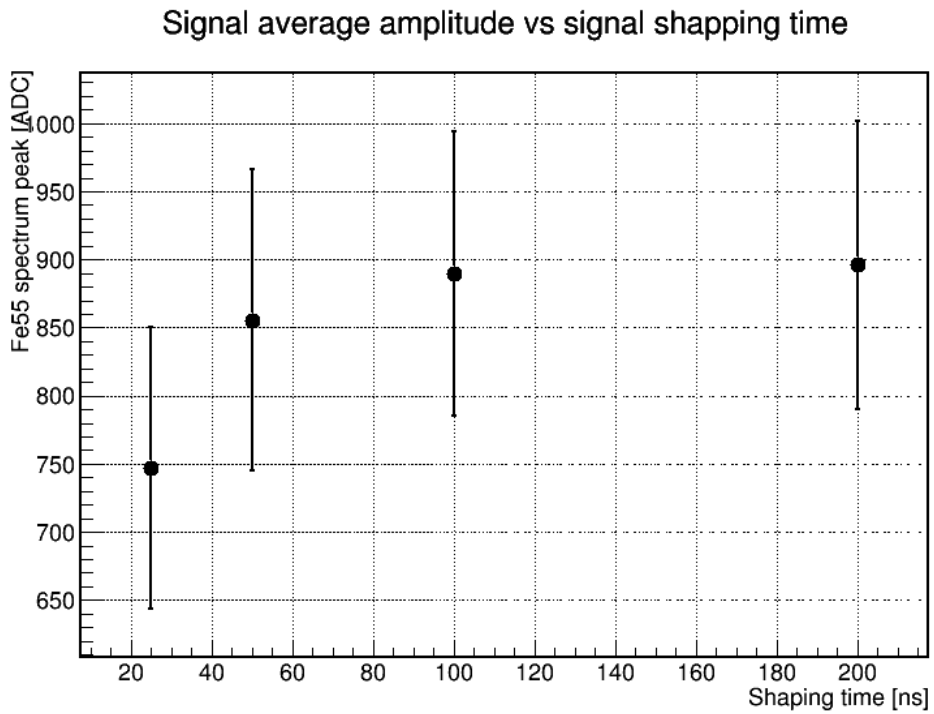
  - VMM
  - Beam Test VMM
  - Streaming
  - Conclusion

VMM test

- Ordered two test board 1500 $ x 2
- Build 6 SoLID prototype boards
- Evaluation board : can look at data with detector small subset of channels
  - Issue with external trigger but waiting for new firmware
  - Can check pedestal width
  - Signal to noise with detector with source and cosmics
  - Look at direct readout signals for 12 channels of detector
- Prototype development for data performance, test direct output with detector and X-ray source

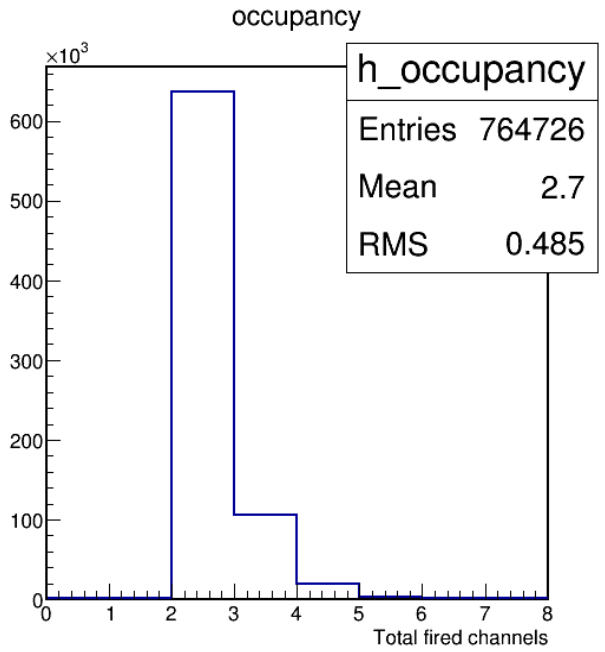
Signal gain vs shaping time, gain = 3 mV/fC

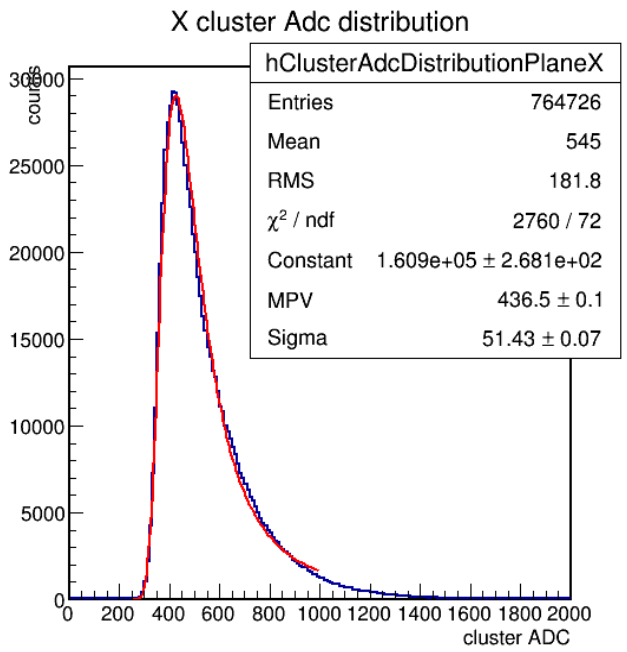


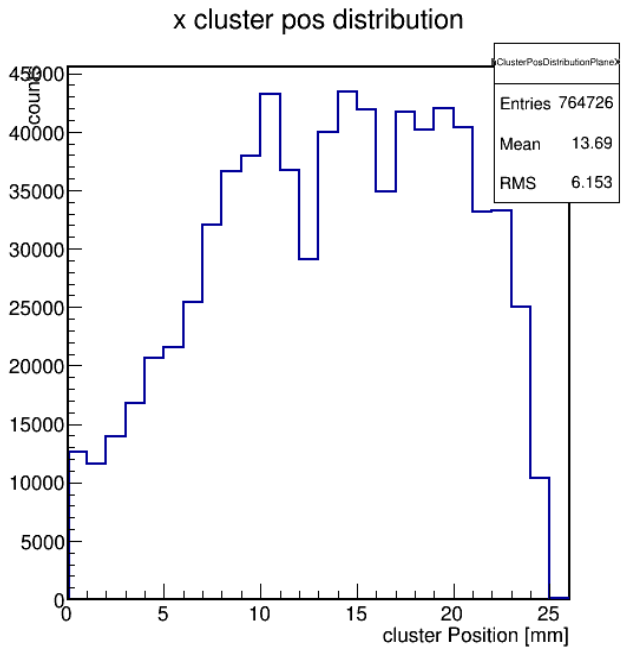


From source data, 25 ns shaping only about 15 % lower than 50 ns, so 25 ns shaping useable

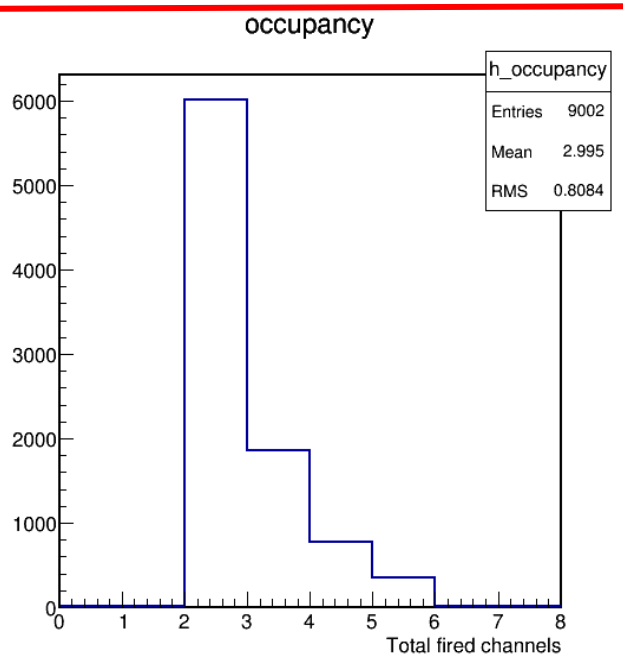
Sr90

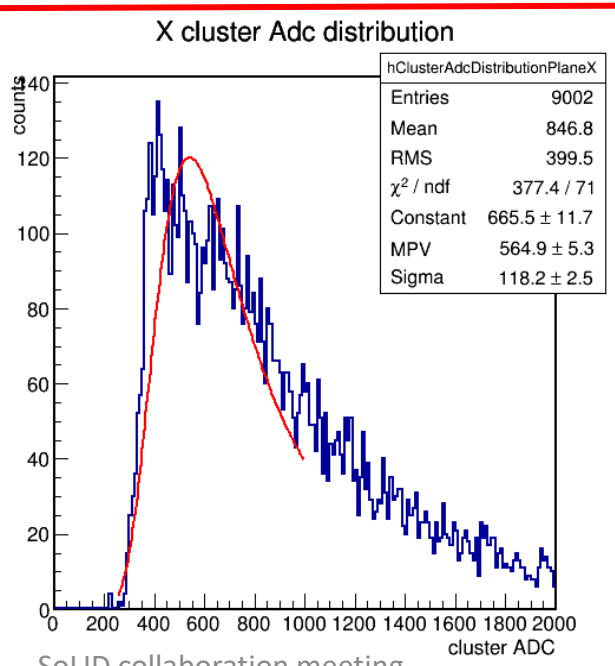

occupancy
h_occupancy
Entries 764726
Mean 2.7
RMS 0.485
Total fired channels

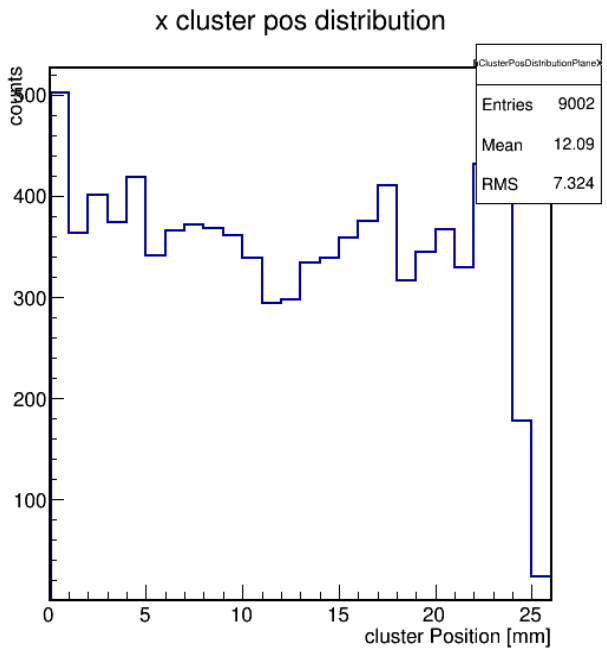

X cluster Adc distribution
hClusterAdcDistributionPlaneX
Entries 764726
Mean 545
RMS 181.8
χ² / ndf 2760 / 72
Constant 1.609e+05 ± 2.681e+02
MPV 436.5 ± 0.1
Sigma 51.43 ± 0.07
counts
cluster ADC


x cluster pos distribution
Entries 764726
Mean 13.69
RMS 6.153
counts
cluster Position [mm]

Cosmic


occupancy
h_occupancy
Entries 9002
Mean 2.995
RMS 0.8084
Total fired channels


X cluster Adc distribution
hClusterAdcDistributionPlaneX
Entries 9002
Mean 846.8
RMS 399.5
χ² / ndf 377.4 / 71
Constant 665.5 ± 11.7
MPV 564.9 ± 5.3
Sigma 118.2 ± 2.5
counts
cluster ADC


x cluster pos distribution
Entries 9002
Mean 12.09
RMS 7.324
counts
cluster Position [mm]

VMM3 prototype board development (Ed)

FPGA for VMM Direct Readout

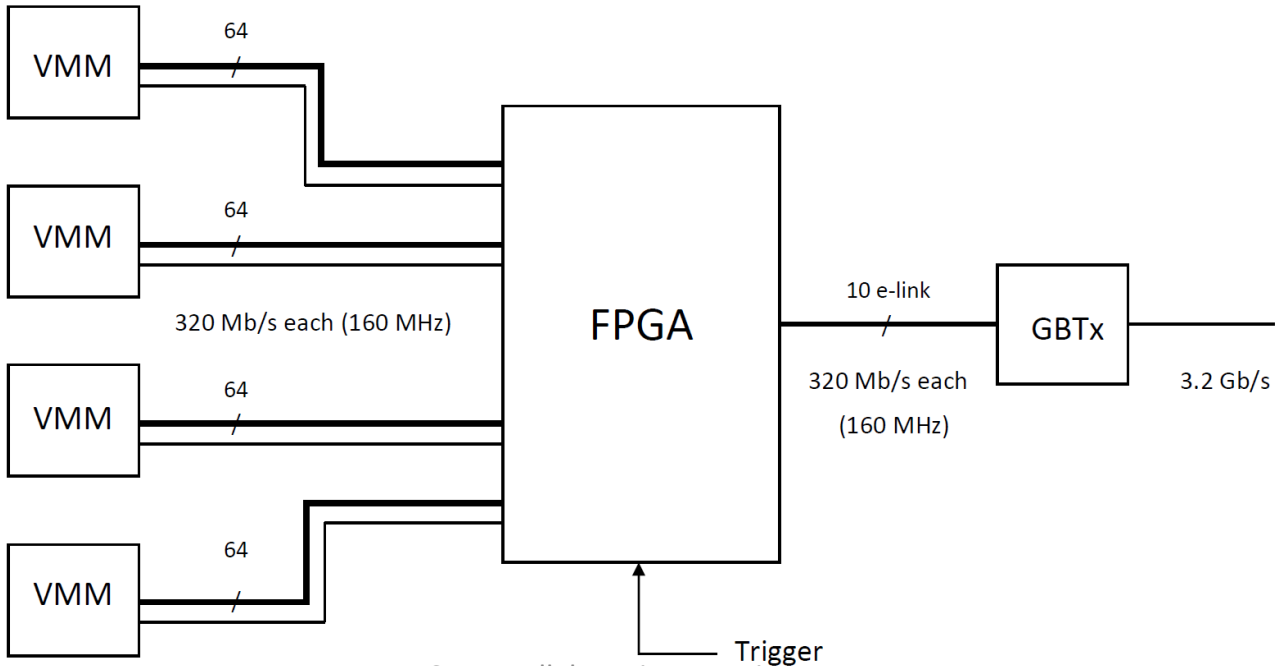
(E.J. 5/28/20)

Proposal

1 FPGA handles direct readout of 4 VMM chips

[64(channels/chip) + 1(clock/chip)] x 2(pins/signal) x 4(chips) = 520 pins (reasonable size, price FPGA)

1 GBTx data link for FPGA output data (10 e-links @ 320 Mb/s = 3.2 Gb/s)



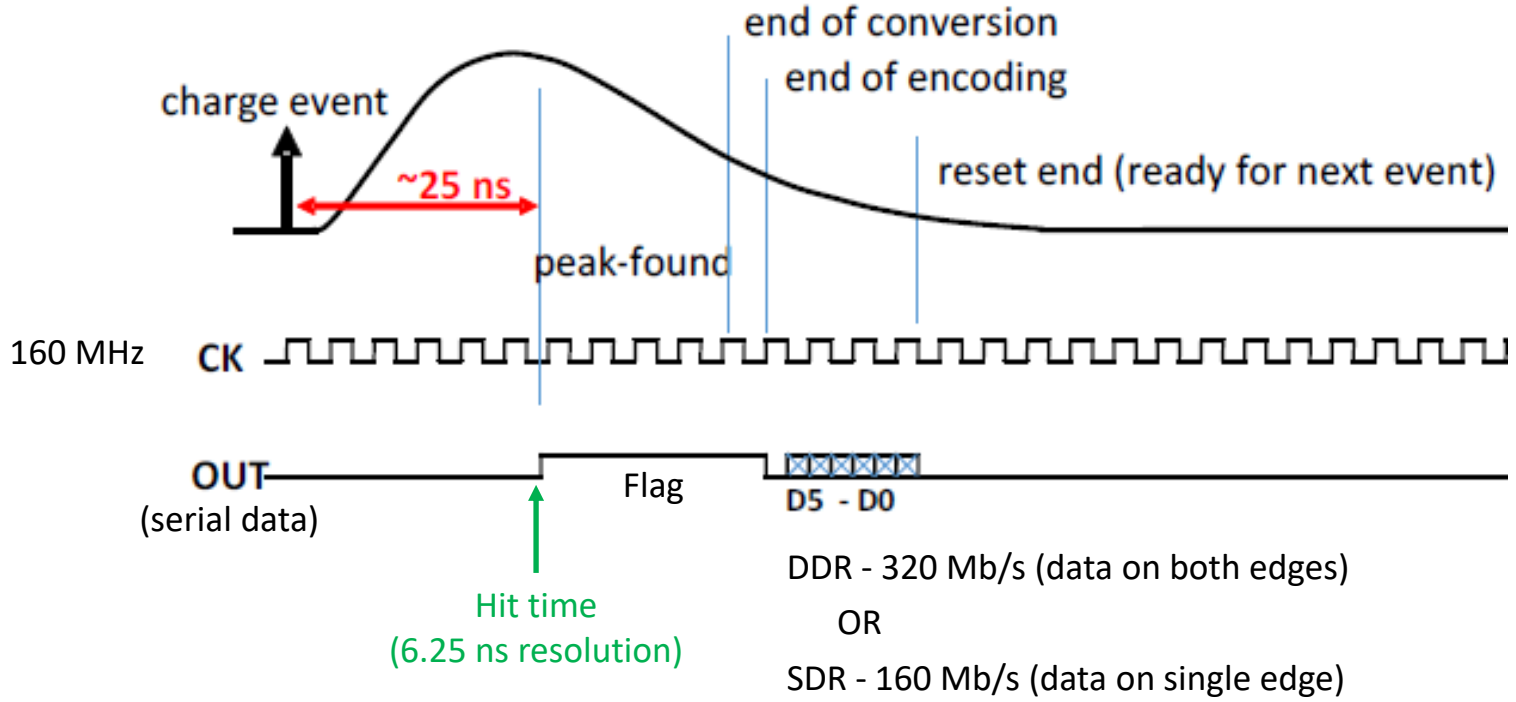
128 channel VMM prototype for SoLID

- Features
  - Fast 6-bit ADC data from each channel allows for high hit rates (~10MHz/ch)
  - Dual readout paths (fiber)
    - 10GbE for low radiation environments (FPGA → SFP+)
    - Readout using CERN rad hard components (FPGA → GBTx → VTRx)
  - Power and signal interface through mezzanine cards
    - Initially use commercial components on mezzanines
    - Later mezzanines with rad hard components – no modification of base board
  - Mitigation of effects of radiation on FPGA by triplicating logic and adding voting circuitry (TMR)

  - Status
    - Commercial component mezzanine boards fabricated
    - Base board fabrication in early May

VMM 6-bit Direct Output data format

Peak amplitude converted to 6-bit value



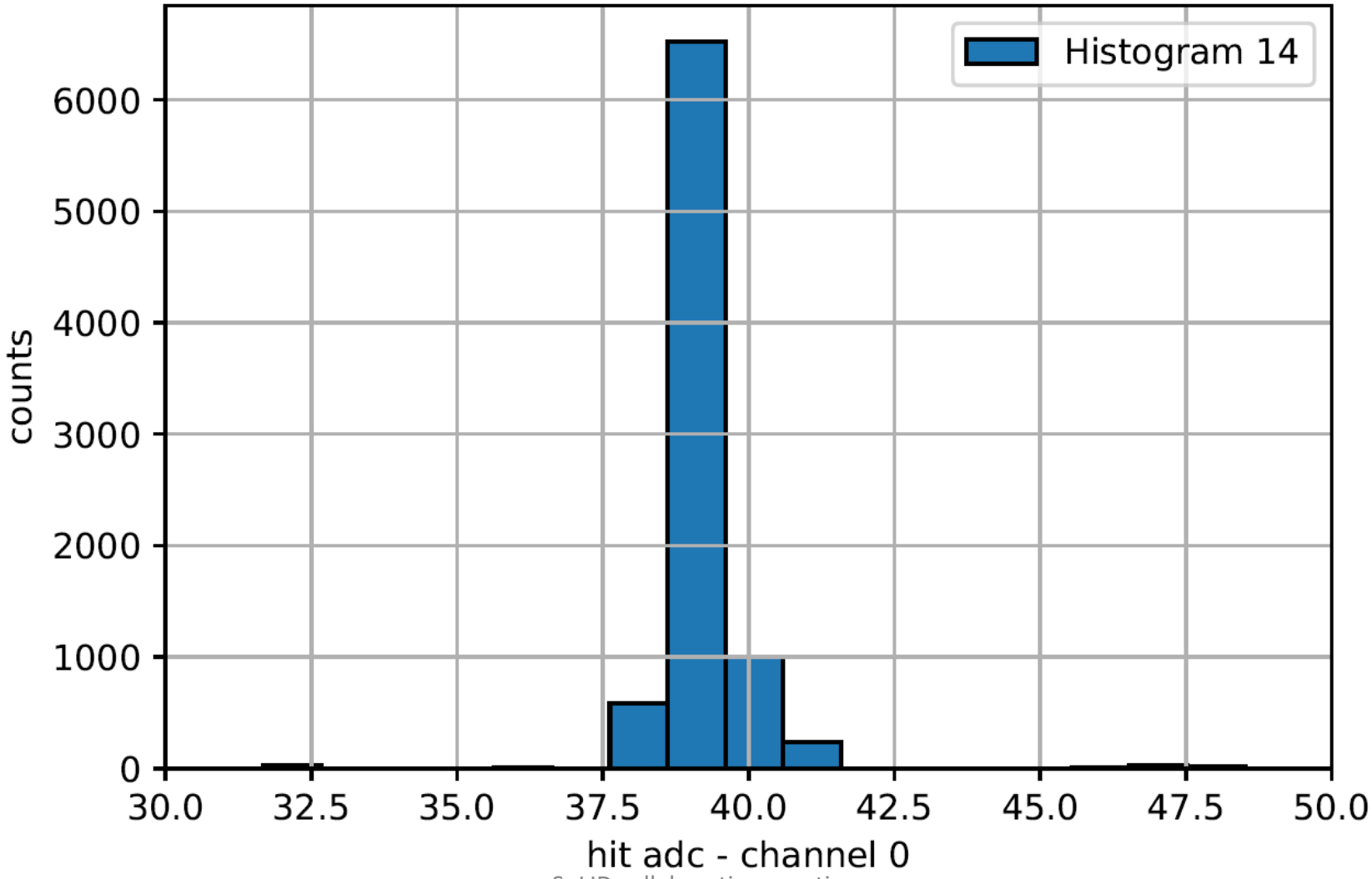
DDR - 320 Mb/s (data on both edges)

OR

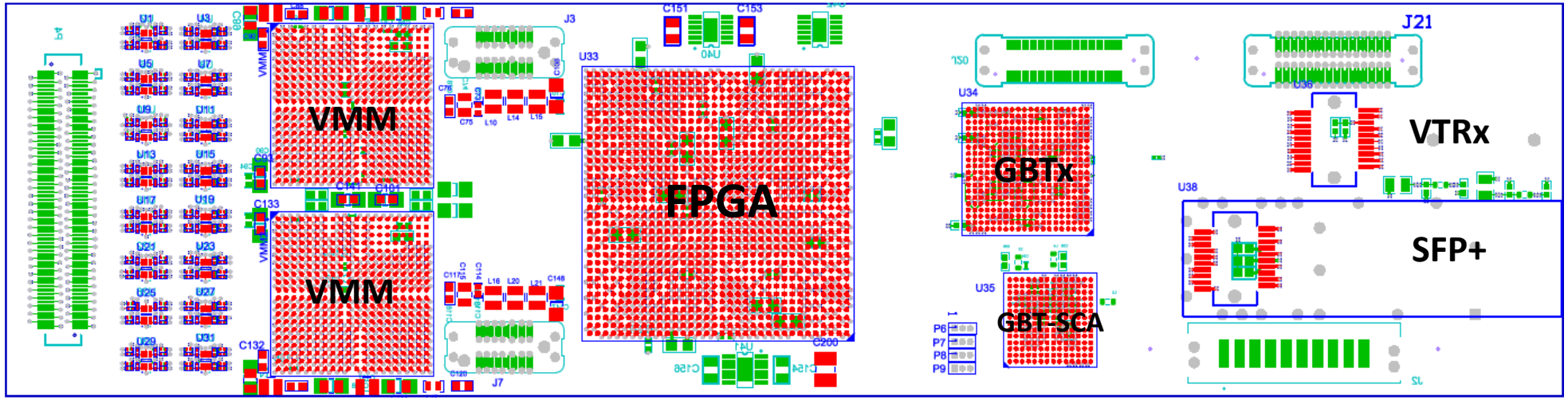
SDR - 160 Mb/s (data on single edge)

VMM 6-bit ADC direct data

(VMM evaluation board read out with Xilinx FPGA development card)



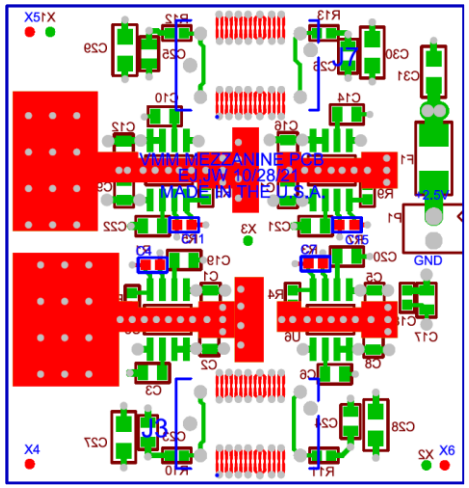
50mm

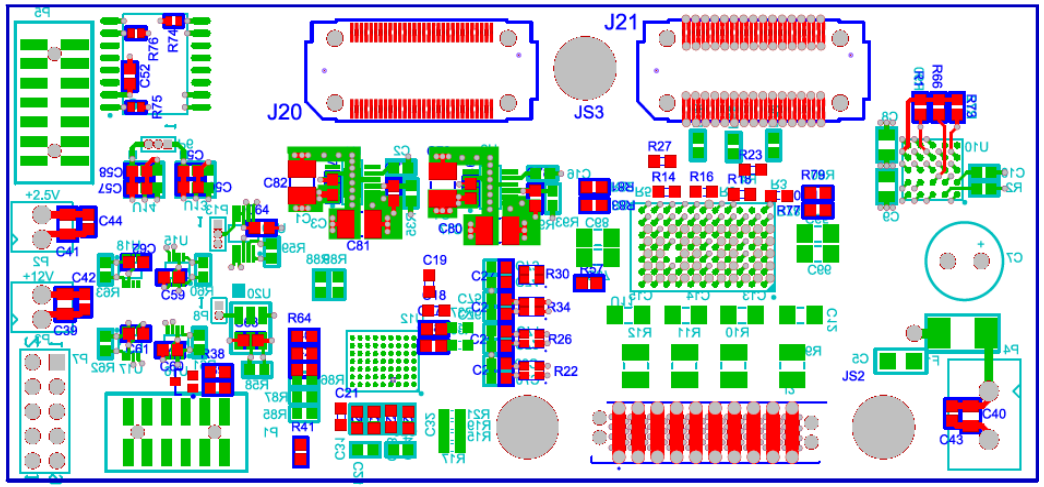


Base board

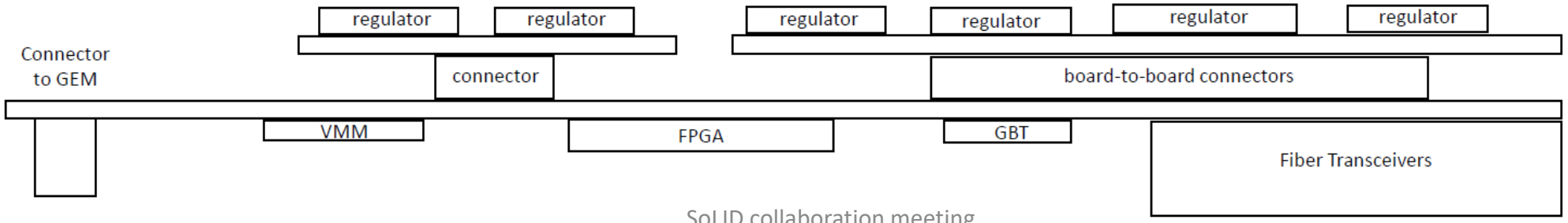
128 channel VMM prototype

VMM power mezzanine

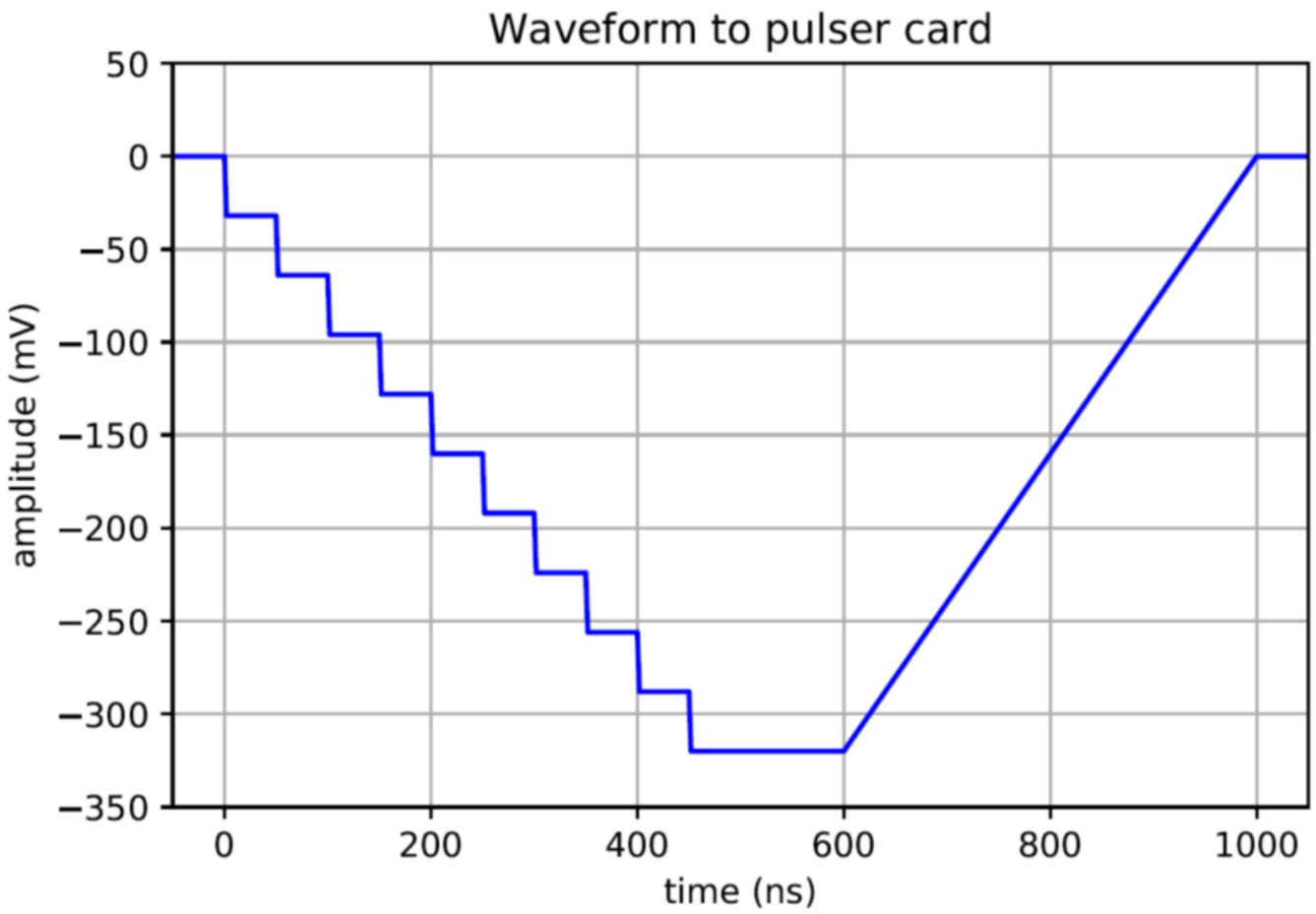


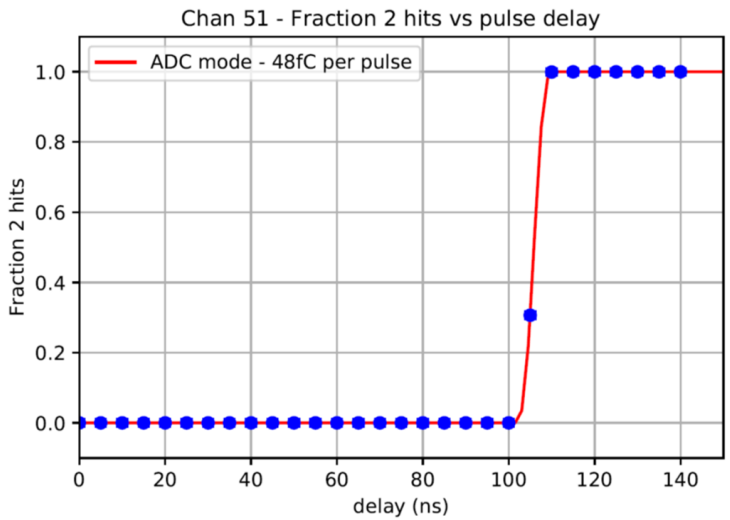


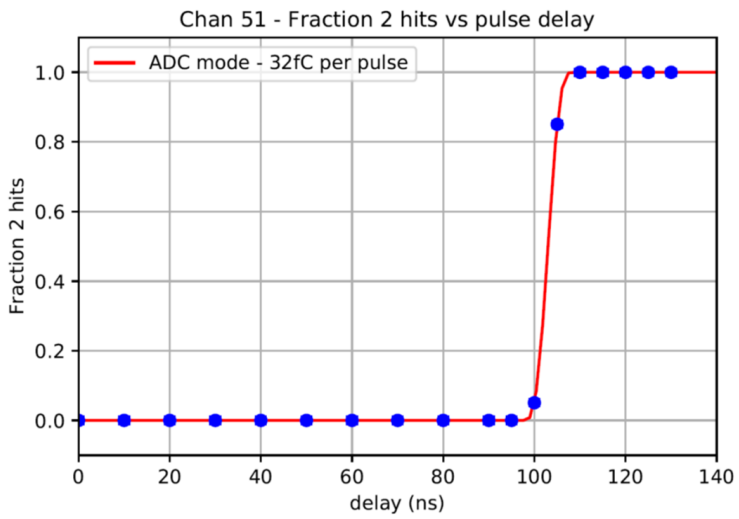
FPGA power mezzanine

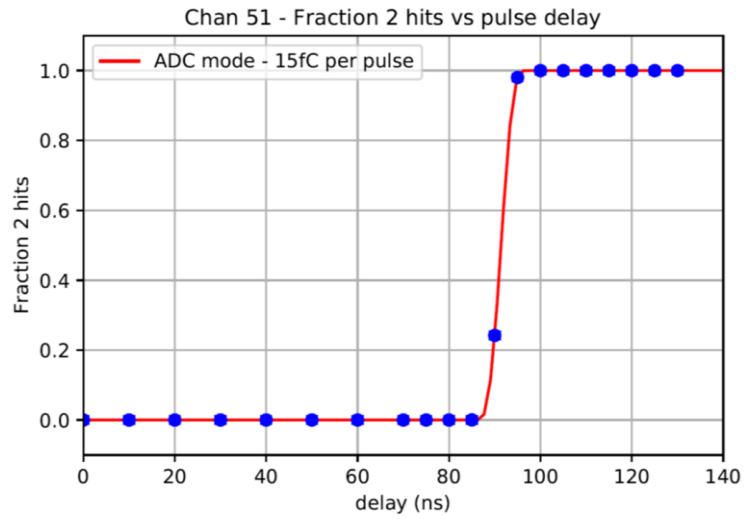


Assembly side view

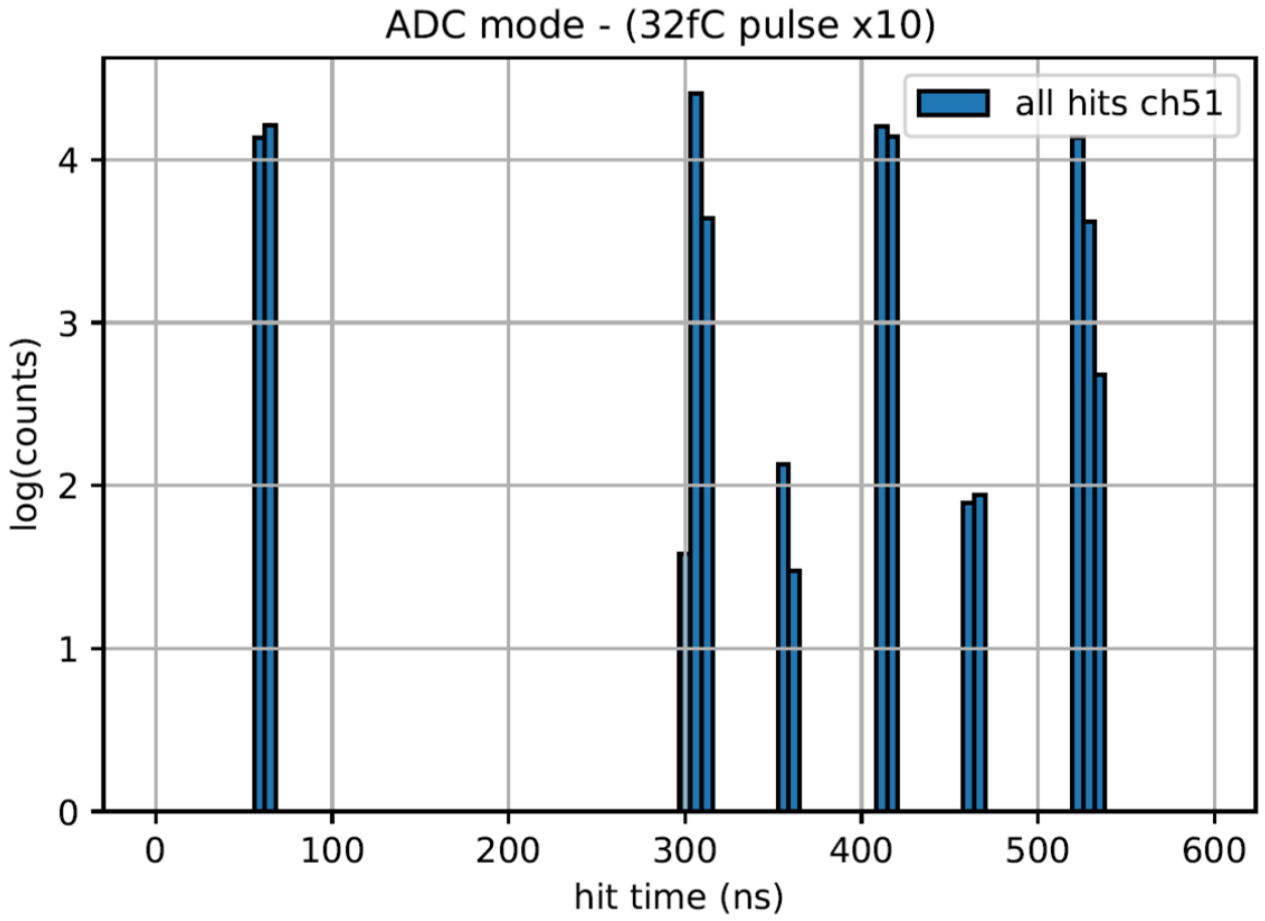

Waveform to pulser card
50
0
−50
−100
−150
−200
−250
−300
−350
amplitude (mV)
0
200
400
600
800
1000
time (ns)


Chan 51 - Fraction 2 hits vs pulse delay
ADC mode - 48fC per pulse
Fraction 2 hits
delay (ns)
0.0
0.2
0.4
0.6
0.8
1.0
0
20
40
60
80
100
120
140


Chan 51 - Fraction 2 hits vs pulse delay
ADC mode - 32fC per pulse
Fraction 2 hits
delay (ns)
0.0
0.2
0.4
0.6
0.8
1.0
0
20
40
60
80
100
120
140


Chan 51 - Fraction 2 hits vs pulse delay
ADC mode - 15fC per pulse
Fraction 2 hits
delay (ns)
0.0
0.2
0.4
0.6
0.8
1.0
0
20
40
60
80
100
120
140

VMM dead time pulser testing



VMM dead time pulser test 6 bit

- Dead time is :

25 ns (peaking time)
+
5 ns (peak finding)
+
25 ns data conversion
+
7 x 6.25 ns data transfer
=
~120 ns

Can go down to ~ 90 ns when using DDR (6.25 / 2)

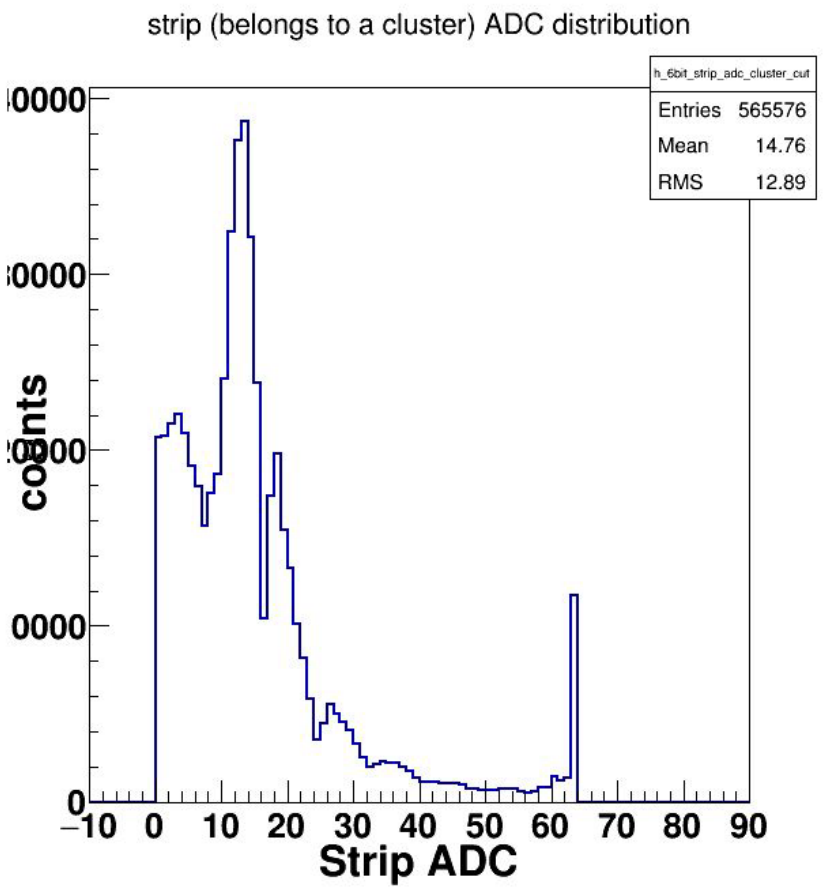
VMM dead time pulser test 10 bit

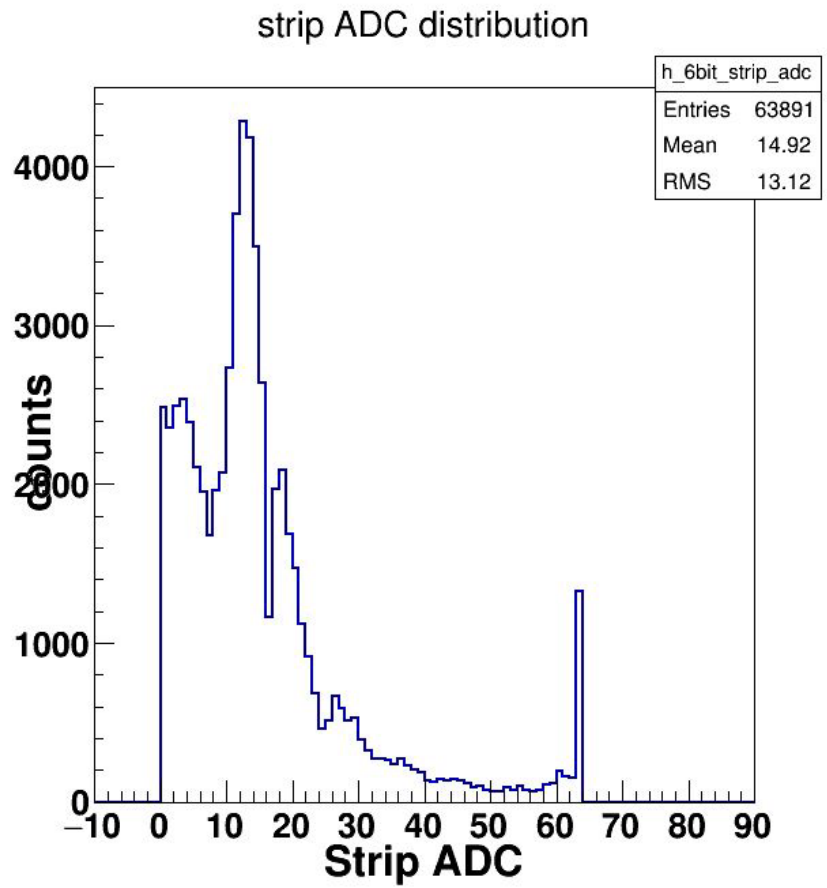
- Dead time is :

25 ns (peaking time)
+
5 ns (peak finding)
+
25 ns data conversion
+
7 x 6.25 ns data transfer
=
~120 ns

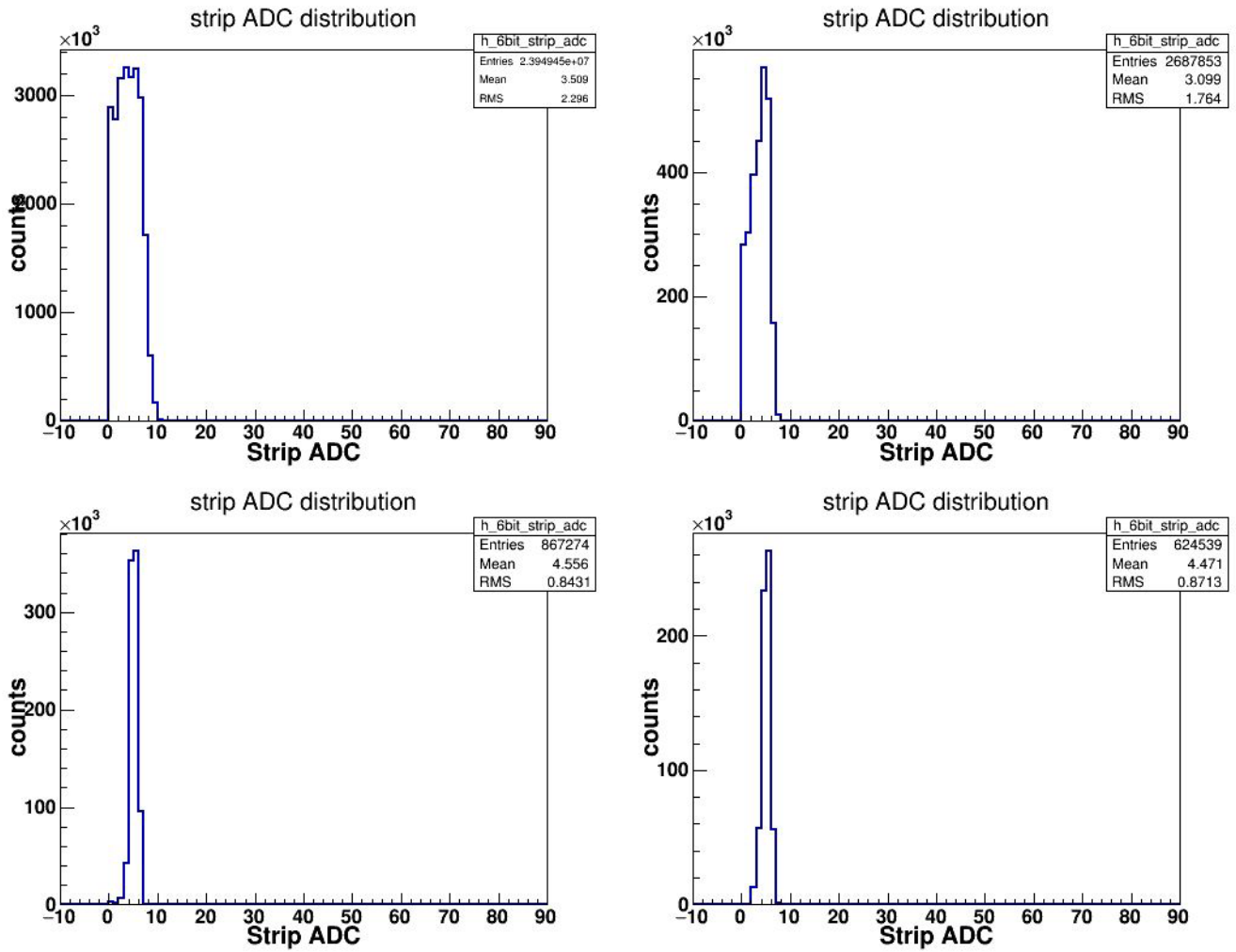
Can go down to ~ 90 ns when using DDR (6.25 / 2)

Sr90 VMM 6 bit 16mV/fC GEM at 4200 V

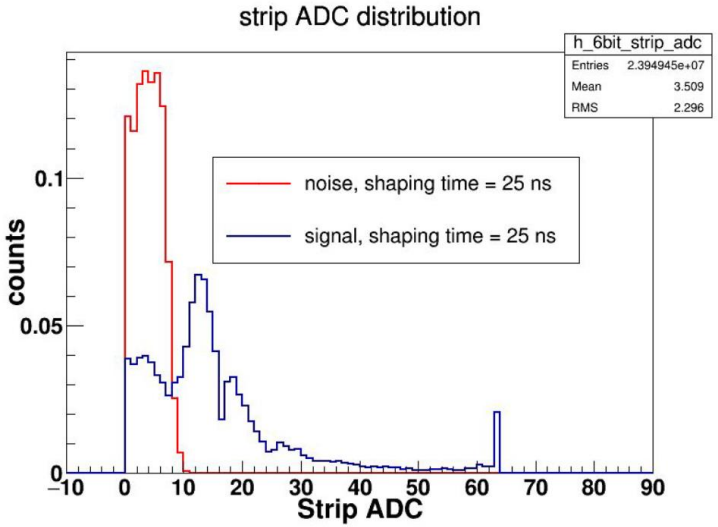


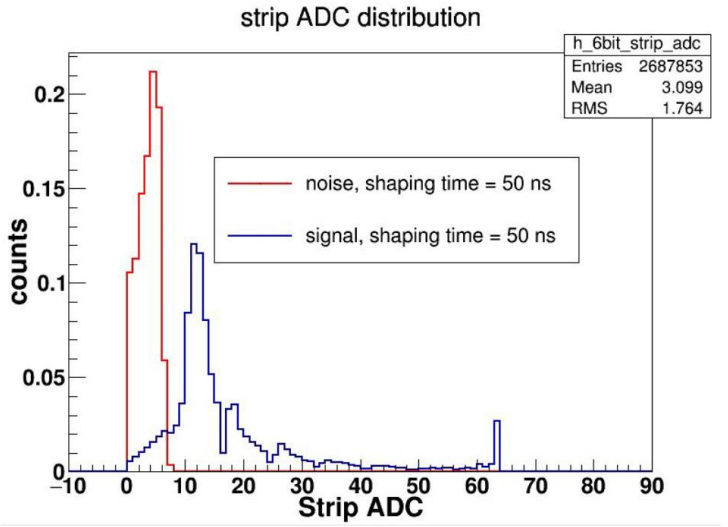


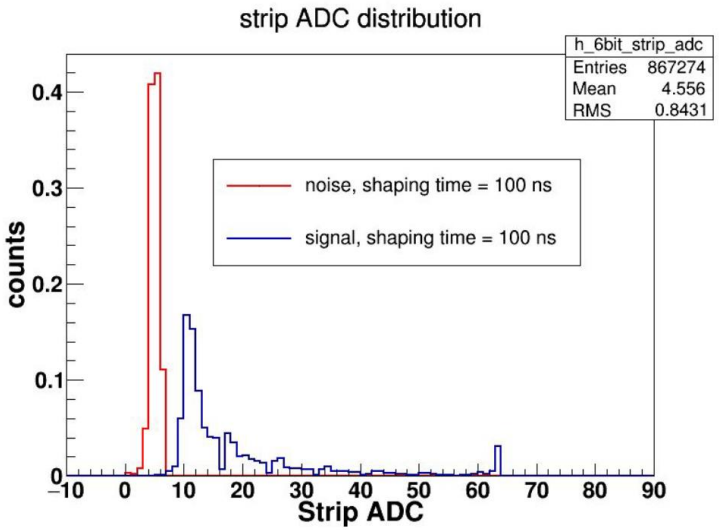
Noise 6 bit 16mV/fC

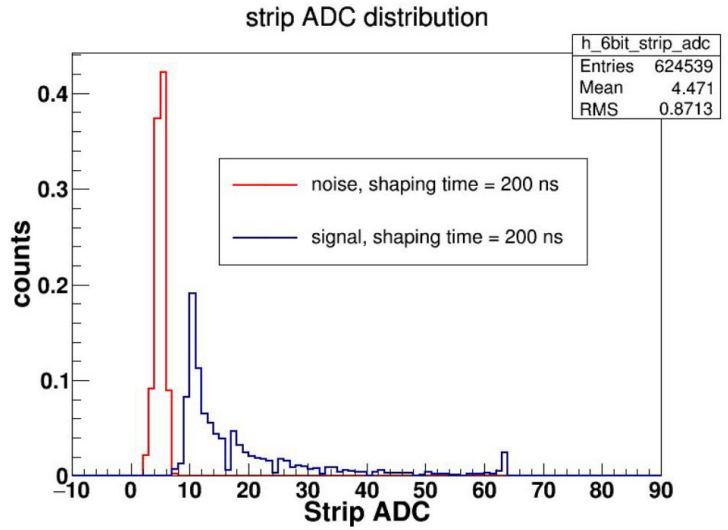


Noise 6 bit 16mV/fC Sr90









- Amplitude for MIP not change much
- Pedestal width dependent on peaking time

Conclusion VMM testing so far

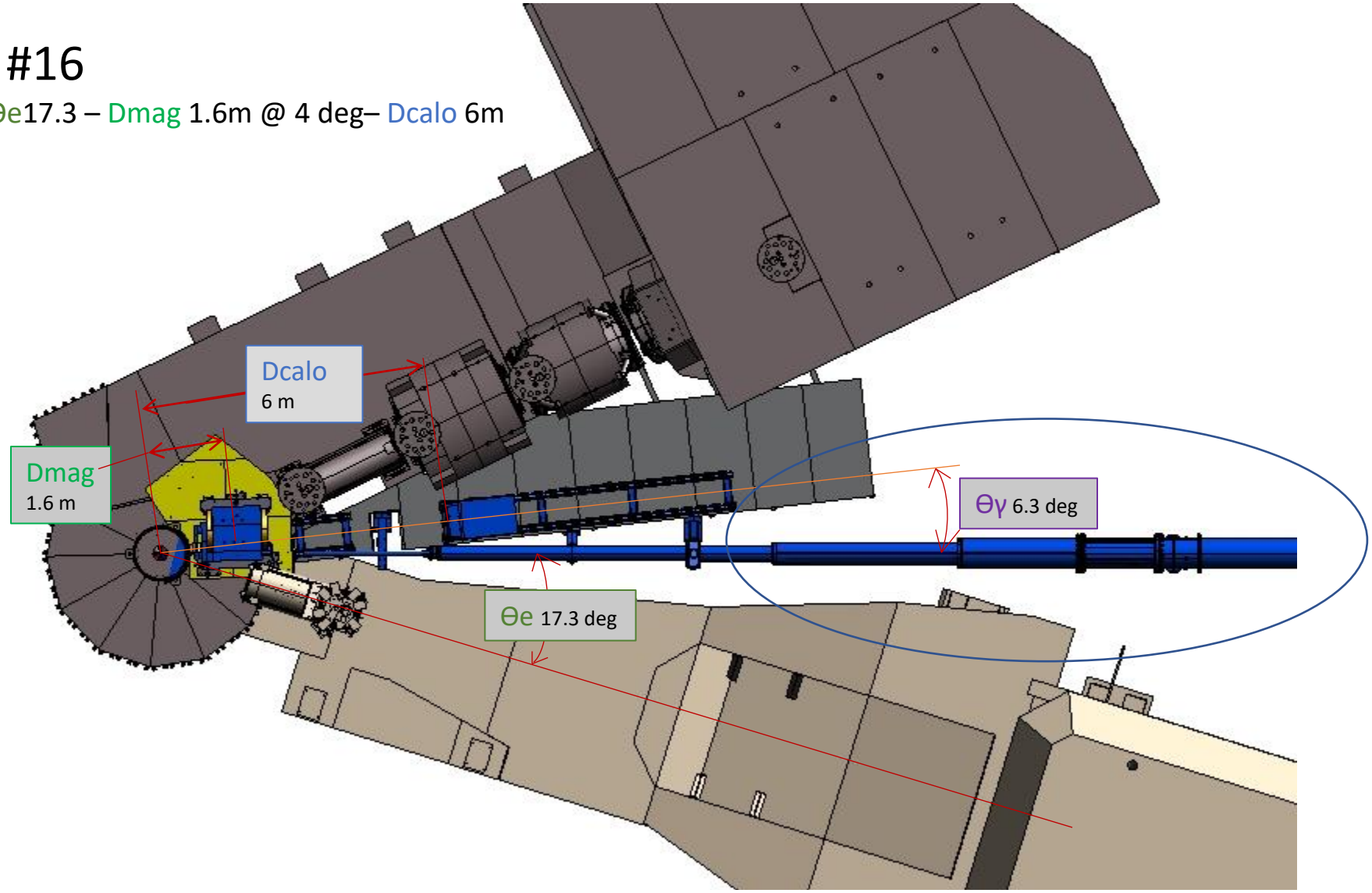
- 90 ns dead time in 6 bit mode
- Some noise seen in prototype
- Noise larger with decreasing integration time
- MIP a bit low in dynamic range of 6 bit prototype
- Implementing 10 bit to cross compare with evaluation board
- 250 ns for 10 bit mode

Test run

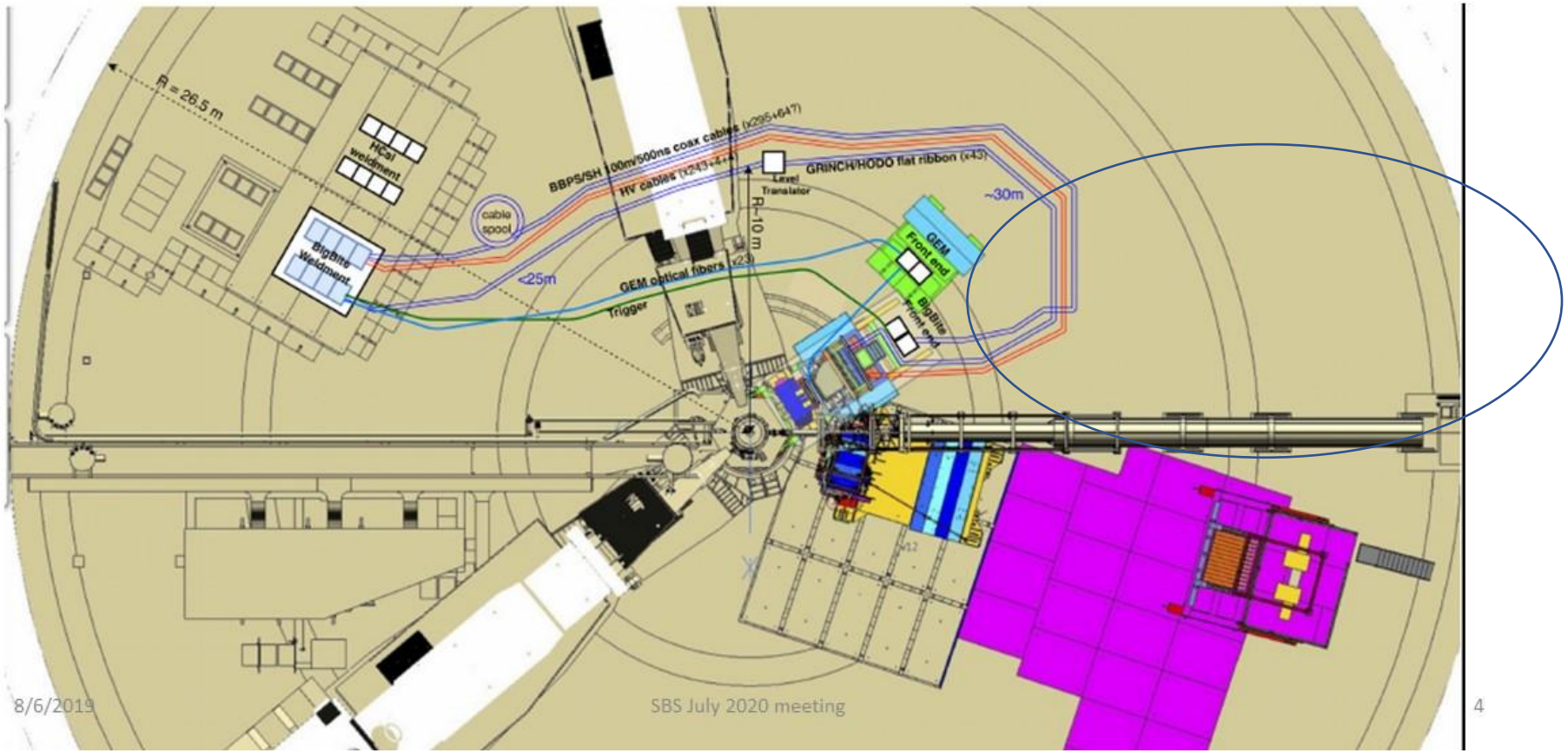
- Build small stand on wheels
  - Can move to any angle without tech support
- Roughly same detector stack as Ecal test run
  - 4 GEMs
  - ECAL
  - Small scintillators to define area for efficiencies and reduce photon background
  - Gas Cerenkov prototype for pion/e

NPS Layout configurations(cont)

- DVCS #16
- Θγ6.3 – Θe17.3 – Dmag 1.6m @ 4 deg– Dcalo 6m



Hall Layout


R = 26.5 m
HCal weldment
BigBite Weldment
cable spool
BBPS/SH 100mv/500ns coax cables (x295+64?)
HV cables (x243+24+6)
GRINCH/HODO flat ribbon (x43)
Level Translator
~30m
R~10 m
<25m
GEM optical fibers (x23)
Trigger
GEM Front end
BigBite Front end

Streaming readout option numbers

Detector	Area	SIDIS	Singles rate MHz	Event size	Data rate GB	PVDIS	Singles rate MHz	Event size	Data rate GB	JPSi	Singles rate MHz	Event size	Data rate GB
LGC	0.7	16	112	16	1.792	80	560	88	49.28	40	280	16	4.48
HGC	1.2	160	1920	16	30.72		0	88	0		0	16	0
SPD_FA	15.2	0.02	3.04	16	0.04864		0	88	0	0.06	9.12	16	0.14592
SPD_LA	3.7	0.12	4.44	16	0.07104		0	88	0	0.25	9.25	16	0.148
EC_preshower_FA	19	33	6270	16	100.32	90	17100	88	1504.8	77	14630	16	234.08
EC_shower_FA	19	10	1900	16	30.4	9	1710	88	150.48	14	2660	16	42.56
EC_preshower_LA	4.1	45	1845	16	29.52		0	88	0	80	3280	16	52.48
EC_preshower_LA	4.1	5	205	16	3.28		0	88	0	19	779	16	12.464
GEM	37	800	296000	16	4736	500	185000	16	2960	1600	592000	16	9472
	Rate in GB/s				4932				4664				9818

Around 10 to 5 TB/s, about 1000 more data than triggered

AI/ML hardware acceleration

Type	Hardware	Inference time	Max throughput (img/s)	Setup
CPU	Xeon 2.6 GHz,1 core	1.75 s	0.6	CMSSW, TF v1.06
CPU	i7 3.6 GHz,1 core	500 ms	2	python, TF v1.10
CPU	i7 3.6 GHz,8 core	200ms	5	python, TF v1.10
GPU (batch=1)	NVidia GTX 1080	100 ms	10	python, TF v1.10
GPU (batch=32)	NVidia GTX 1080	9 ms	111	python, TF v1.10
GPU (batch=1)	NVidia GTX 1080	7 ms	143	TF internal TF v1.10
GPU (batch=32)	NVidia GTX 1080	1.5 ms	667	TF internal TF v1.10
Brainwave	Altera Artix	10 ms	660	CMSSW, on-prem
Brainwave	Altera Artix	60 ms	660	CMSSW, remote

Could gain factor of ~ 100 processing with GPUs, might be able to do better

Conclusion

- VMM
  - VMM test with Eval board
  - Small amplitude variation with peaking time
  - Prototype board developed
    - Dead time measure 110 ns for 6 bit
    - Studying noise at high gain

- Test beam for VMM
  - Smaller stand
  - Hall A or C
  - Need to procure radiation hard low voltage components
  - Plan January 2024

- Streaming option
  - About 5 to 10 TB/s about 1000 more than triggered
  - Might be able to handle with AIML progress, network progress and CPU