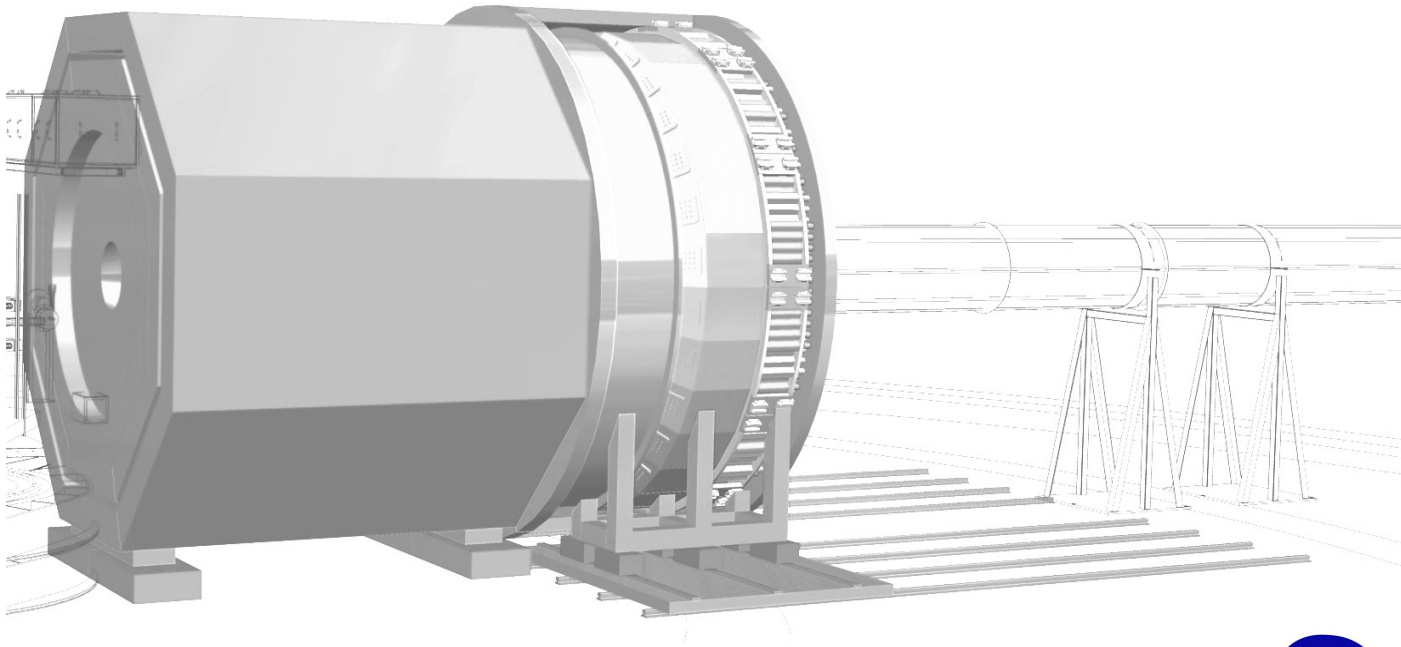


# Gas Electron Multiplier (GEM) Tracker



Nilanga Liyanage

SoLID GEM Group  
University of Virginia



U.S. DEPARTMENT OF  
**ENERGY**

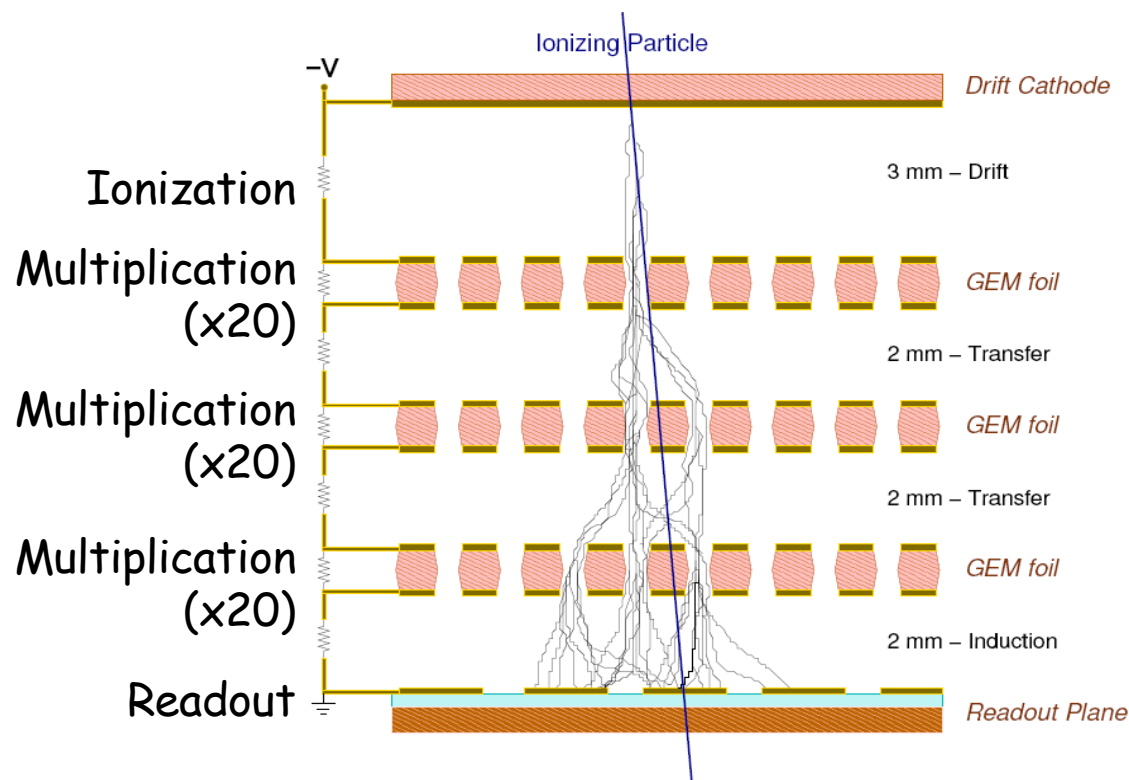
Office of  
Science



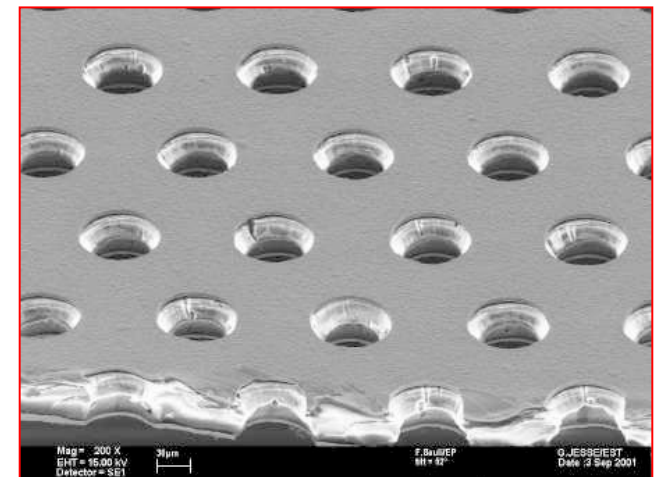
Jefferson Lab

# Why GEMs

- SoLID concept leads to need for high rate trackers with good position resolution.
- GEMs: cost effective for high resolution tracking under high rates over large areas.
  - Rate capabilities higher than many MHz/cm<sup>2</sup>
  - High position resolution ( < 75  $\mu$ m)
  - Ability to cover very large areas ( 10s – 100s of m<sup>2</sup>) at modest cost.
  - Low thickness ( $\sim$  0.5% radiation length)
- Used for many experiments around the world: COMPASS, CMS upgrade, ALICE TPC, pRad, SBS etc.

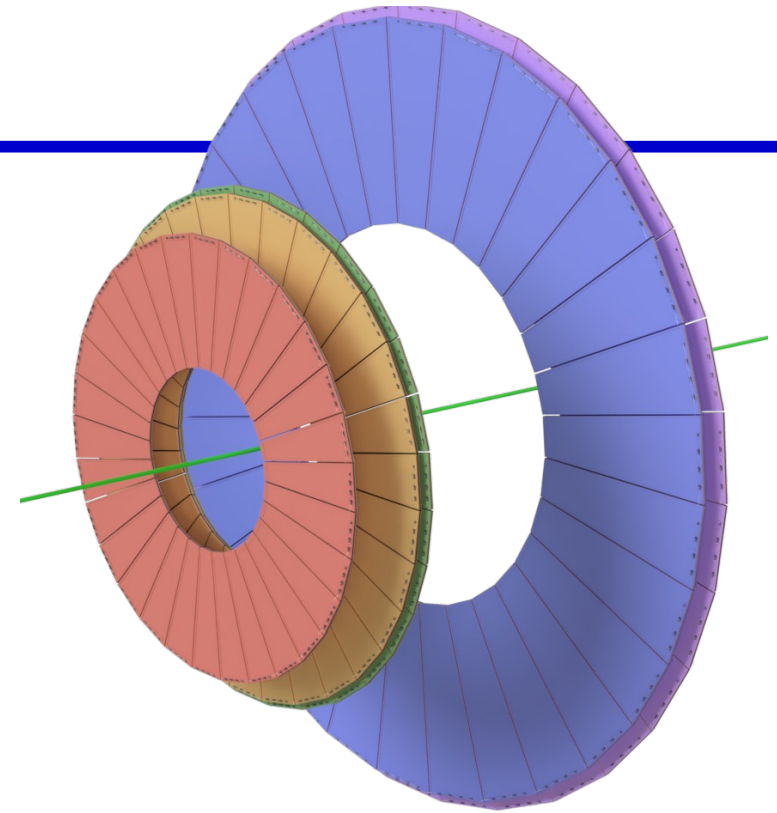
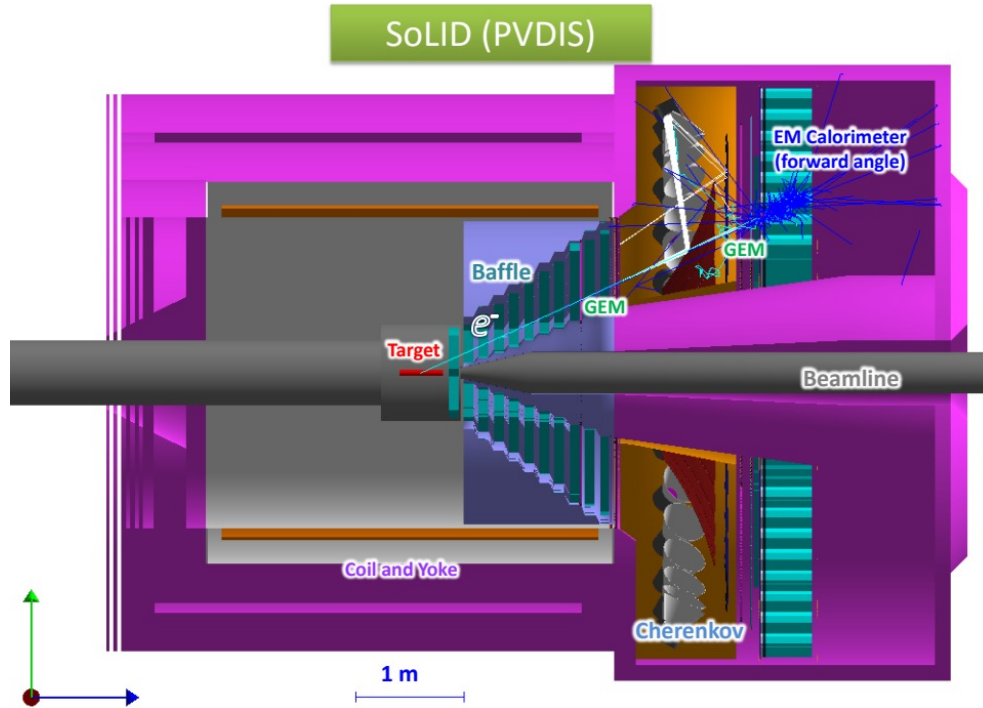


GEM foil: 50  $\mu$ m Kapton + few  $\mu$ m copper on both sides with 70  $\mu$ m holes, 140  $\mu$ m pitch

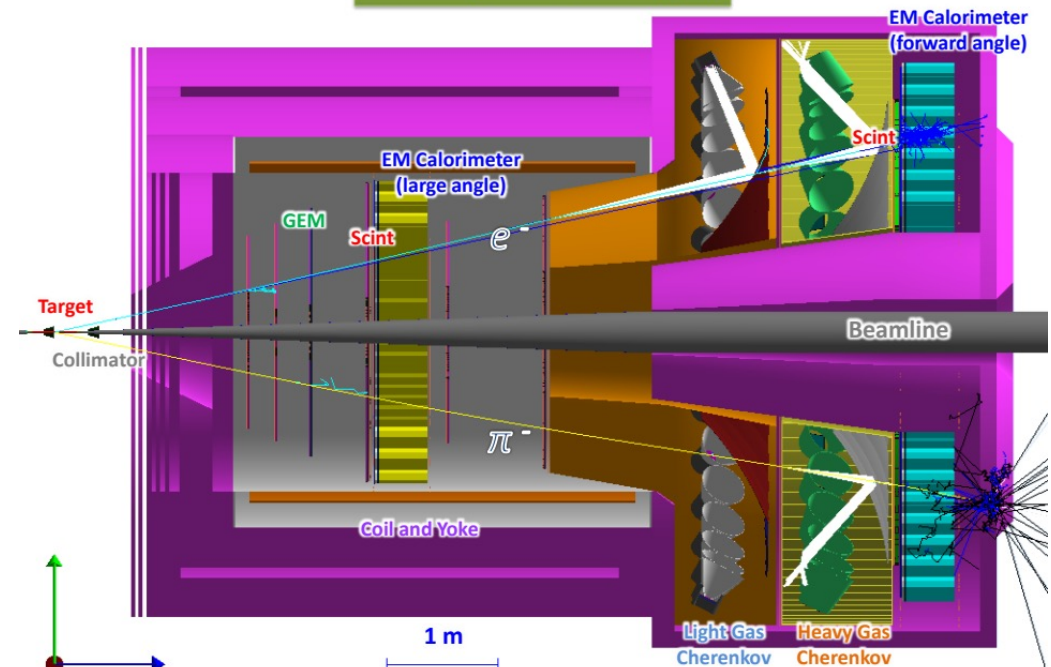
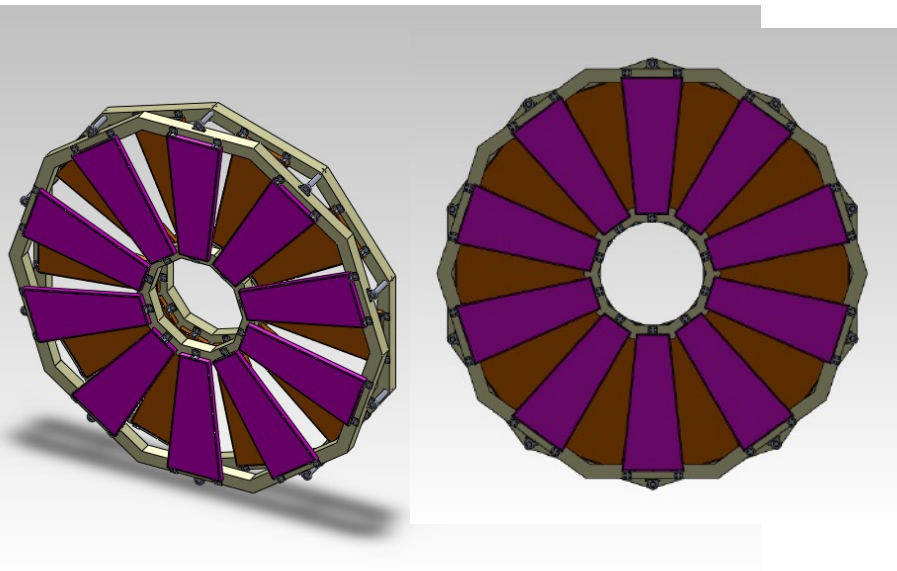


# GEM Overview

SoLID (PVDIS)



SoLID (SIDIS and J/ψ)

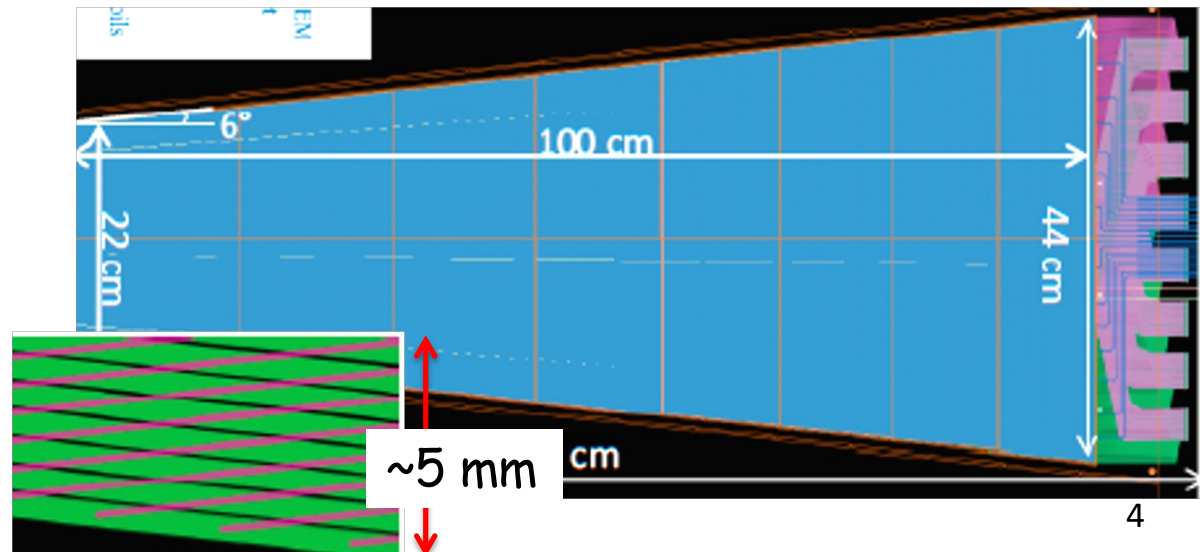
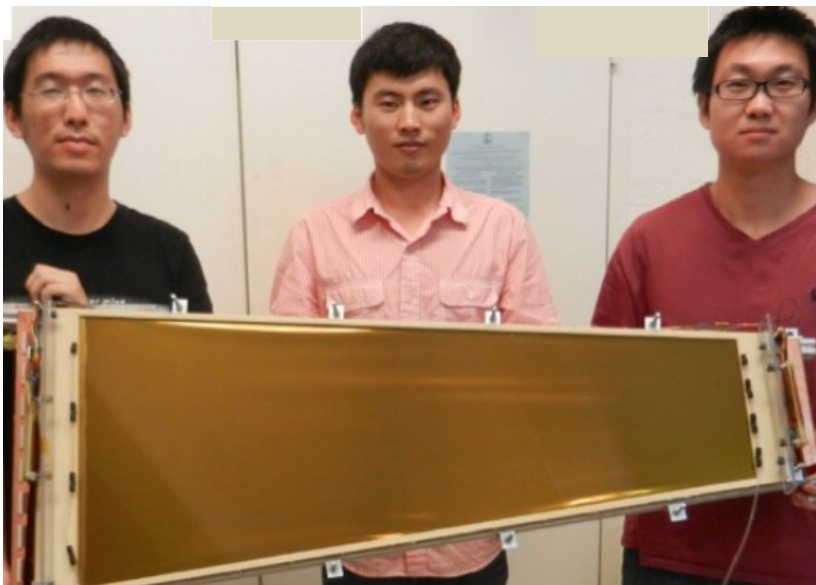




# GEM Requirements: for all experiments

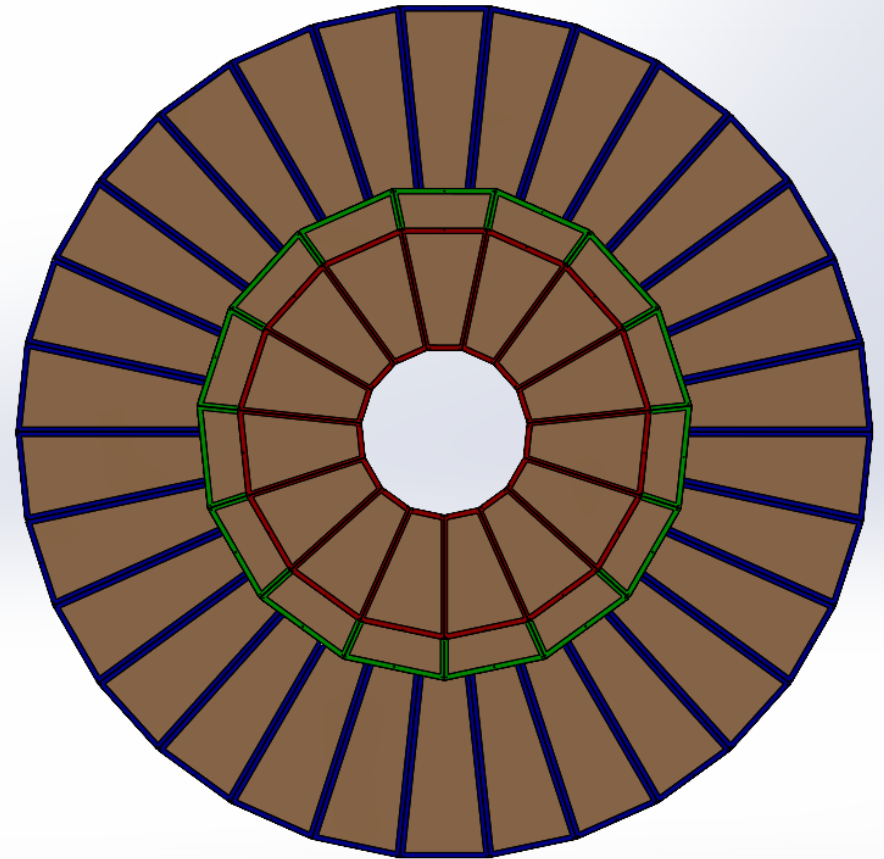
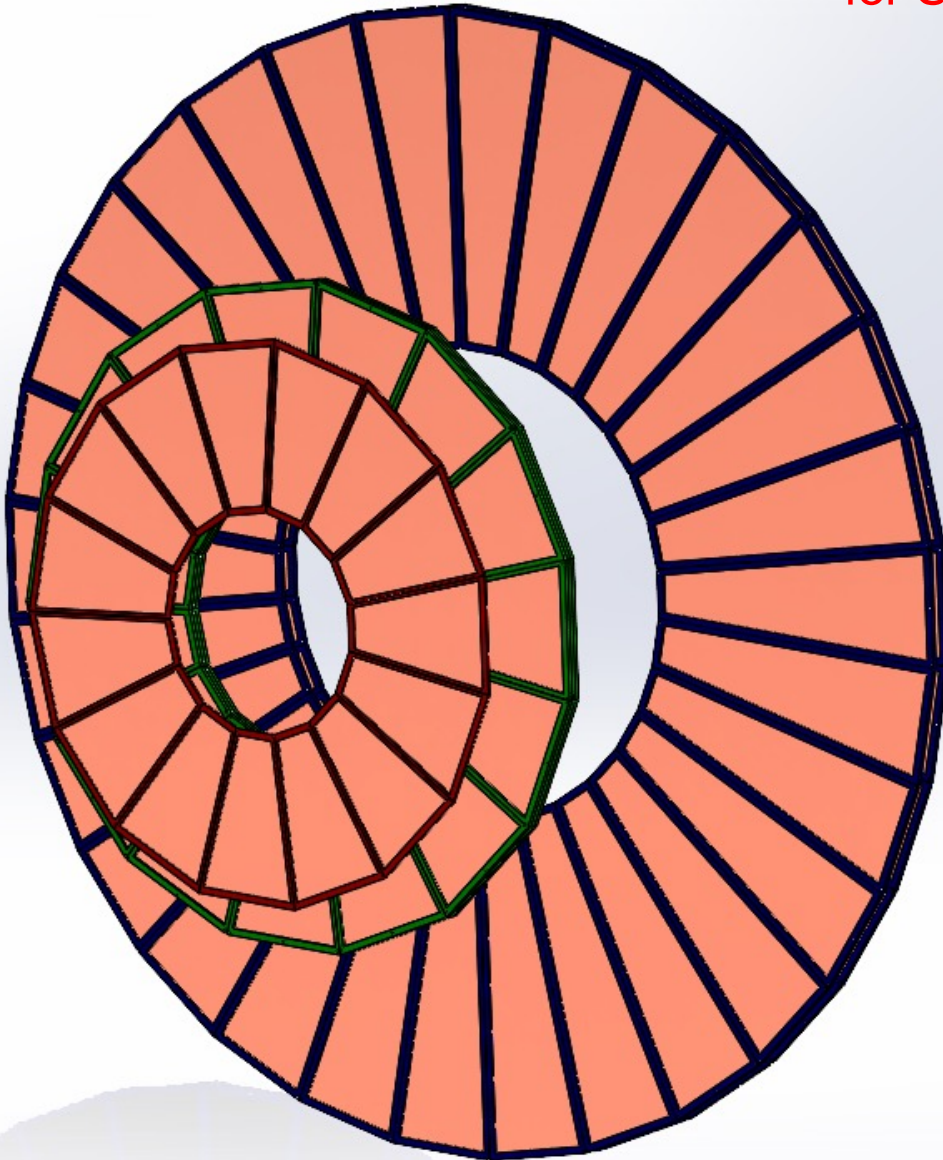
- ❑ Good position resolution
  - ❑ 100  $\mu\text{m}$  ( 1 mm) in azimuthal (radial) direction.
    - 2D U-V readout with 12-degree stereo angle between strips
    - 400  $\mu\text{m}$  (600  $\mu\text{m}$ ) strip pitch for layers 1-3 (5-6)
    - The high occupancy at layer #1: split each readout strip into two channels
    - Total number of channels  $\sim 215$  k (with 15% spares)
- ❑ 92 % overall GEM-module efficiency.
- ❑ modules with a trapezoidal geometry, with  $12^\circ$  angular width
- ❑ All readout electronics located at the outer edge: Given radiation exposure map.
- ❑ Side frames need to be very narrow: minimize material thickness in active area (especially for SIDIS, J/ $\Psi$ )

All requirements follow from tracking and neutron/radiation dose simulation to meet SoLID conditions.

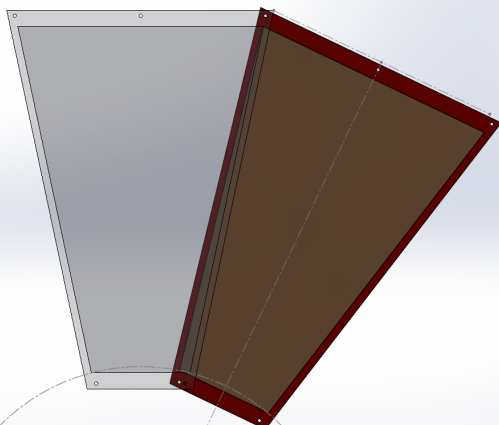
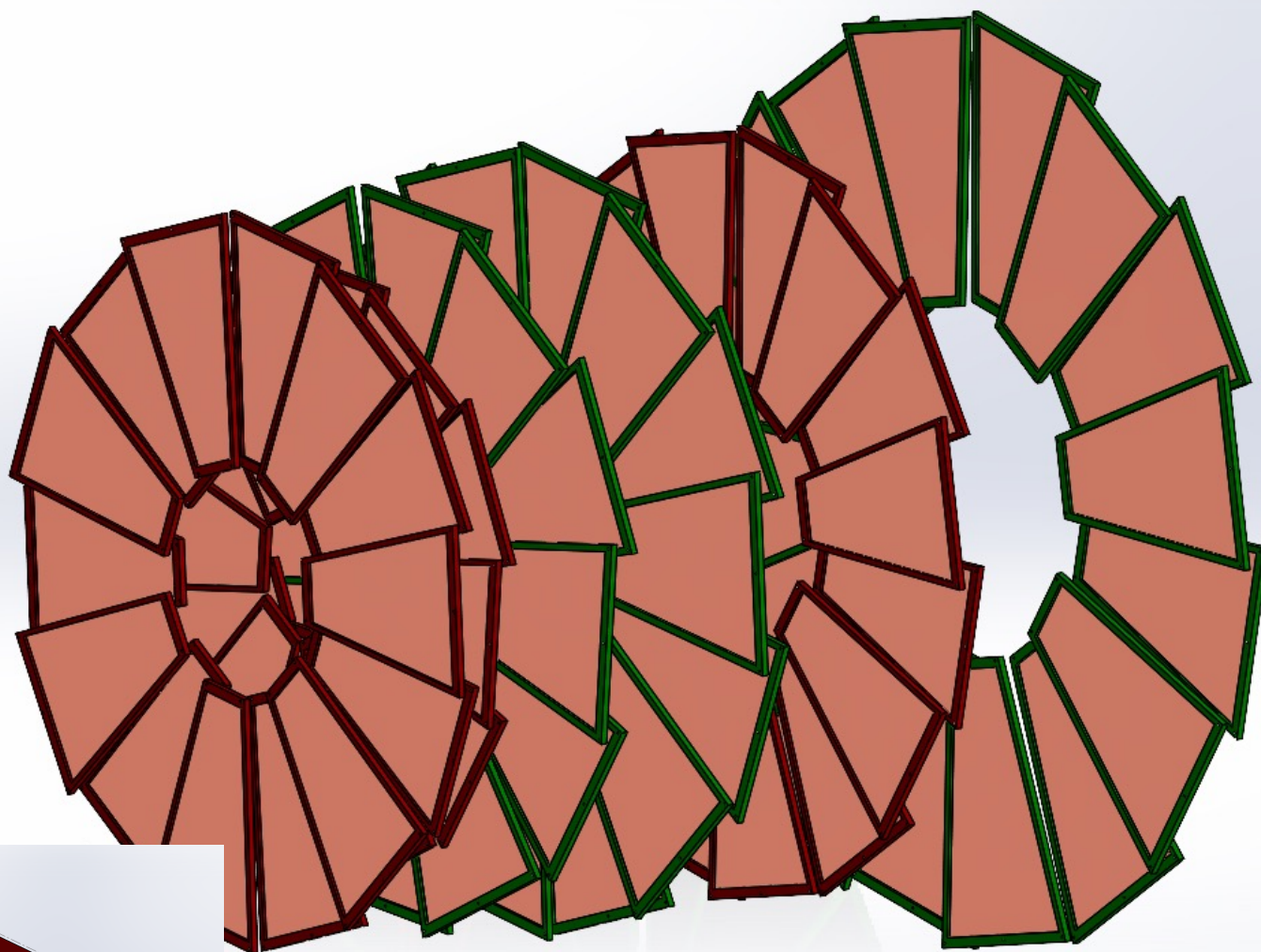


# Recently optimized GEM configuration - PVDIS

First 3 layers optimized to have only 15 modules:  
minimizes the number of frames in the active area  
for SIDIS



# Recently optimized GEM configuration - SIDIS



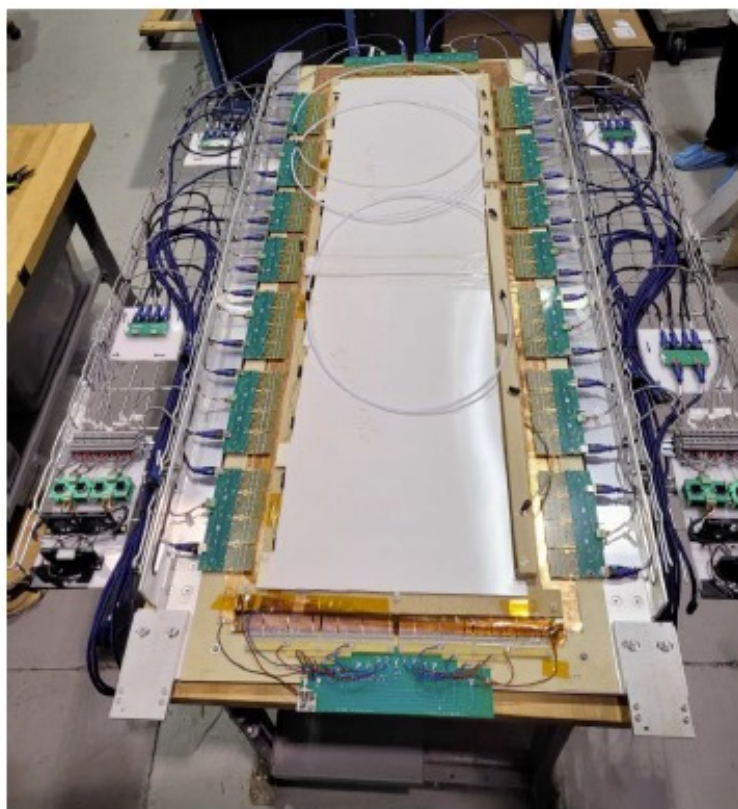
The components and fabrication methods to be used for SoLID GEMs were used by the UVa group for the successful fabrication of GEMs for PRad and SBS experiments.

These GEMs worked very well in beam with stable performance, high efficiency and good resolution; meeting or exceeding design parameters.



# The SBS GEMs produced at UVa

- 50 cm x 60 cm GEM modules for SBS rear tracker: 48 modules –All installed, 28 in beam
- 150 cm x 40 cm large GEM modules for SBS front tracker: 4 modules – all in in beam; two more under construction now



UV (shown)  
40 x 150 sq.cm  
Single module



XY (shown)  
60 x 200 sq.cm  
4 modules

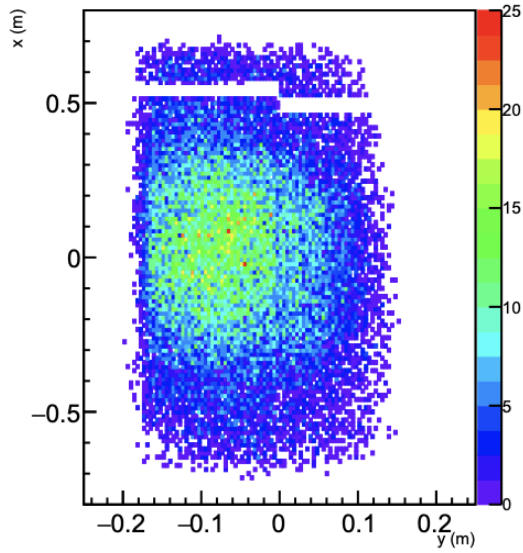


# GEM tracker status, issue and possible plans

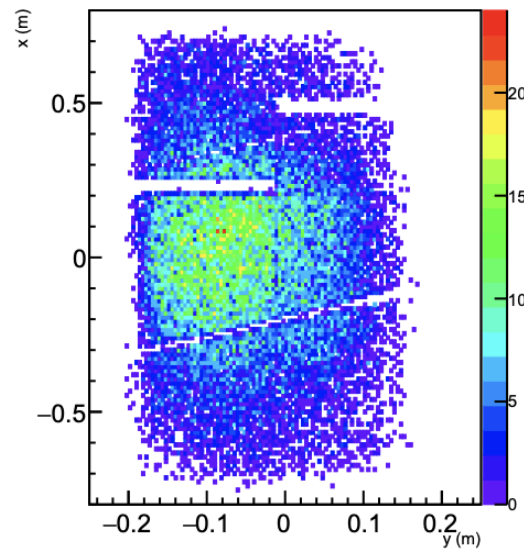
- For SBS we already ran the GEM tracker in unprecedented integrated rates (active area x local rate): luminosity upto to  $0.5 \times 10^{38}$
- UVa GEM tracker layers have been working very well:
  - Overall good efficiency
  - Very stable: very few HV trips
  - Noise levels sufficiently low
  - Good gain: signals well above noise
  - Very good resolution: close to what was achieved with comic's
  - Raw occupancy levels as high as 50%
  - Real time firmware zero suppression has been working very well.
  - Data volumes manageable
- The observed background hit rates within  $\sim 40\%$  of the expected; but total ionization in chambers  $\sim \times 2$  higher than predicted.

# 4 UV and 1 XY have been running successfully in BigBite since 2021

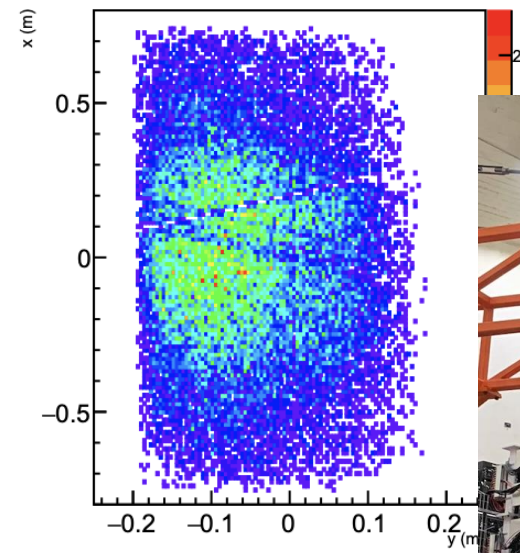
Layer 0



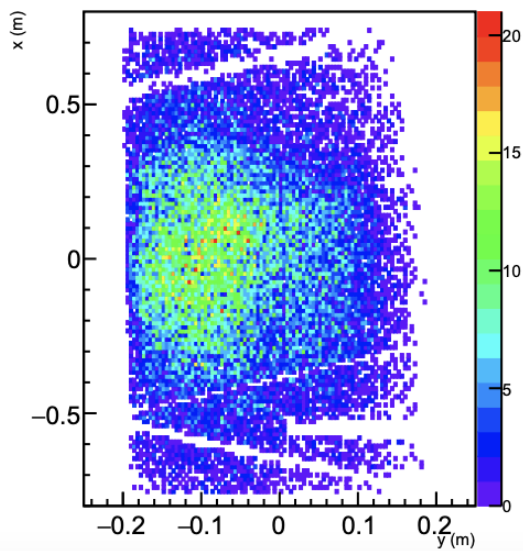
Layer 1



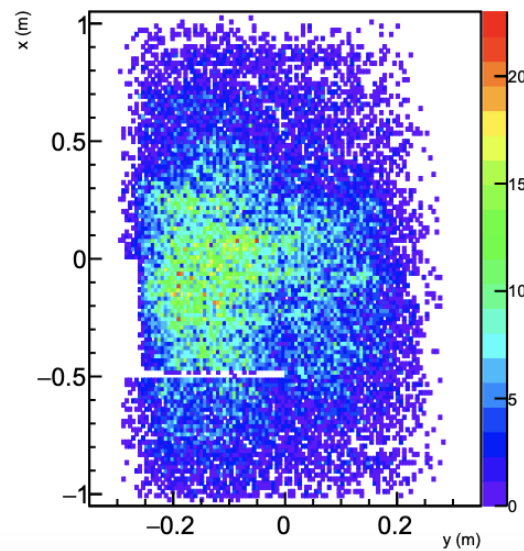
Layer 2



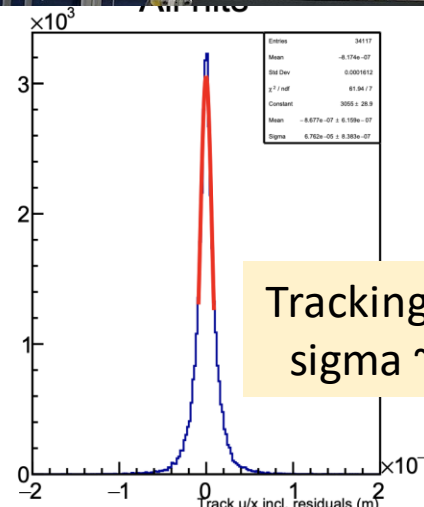
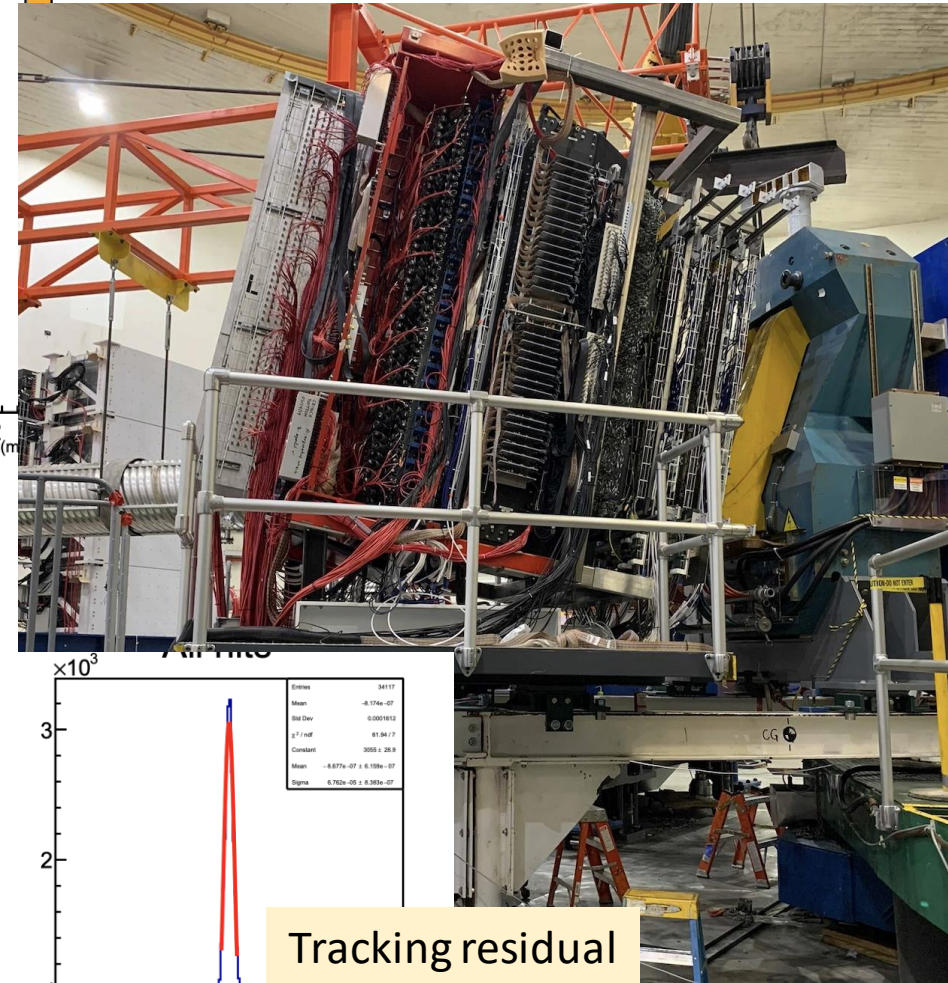
Layer 3



Layer 4



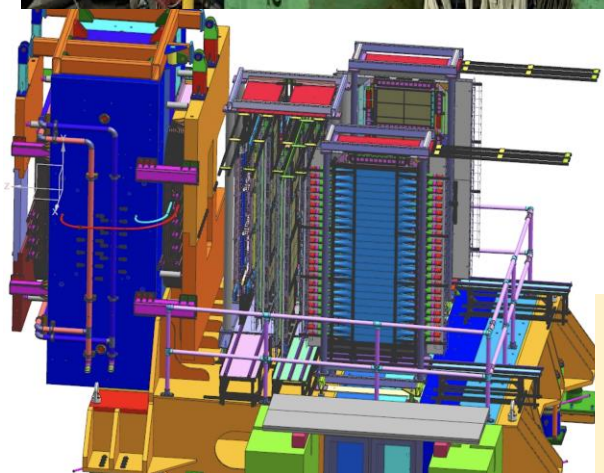
Hit maps with  
tracking constraints  
shown per layer



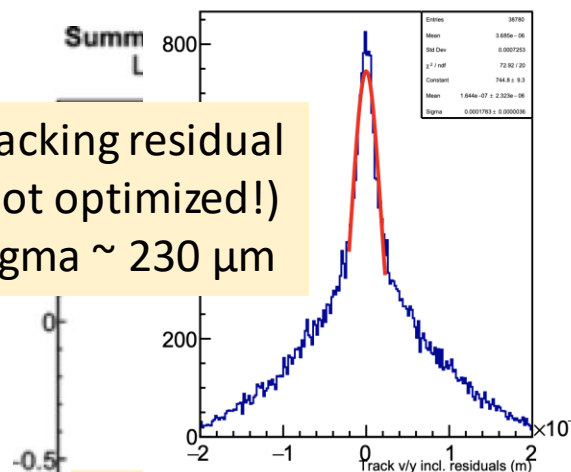
Tracking residual  
sigma  $\sim 70 \mu\text{m}$



# 6 XY have been running successfully in SBS since 2022



Tracking residual  
(not optimized!)  
 $\sigma \sim 230 \mu\text{m}$



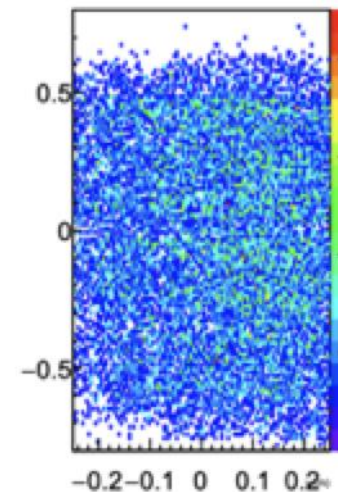
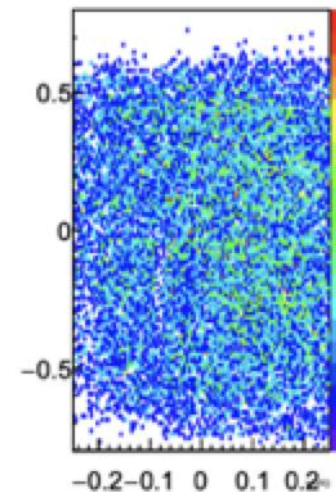
LV difficulties in LO&1 (INFN chambers).

All others working well in GEN!

maps on good tracks

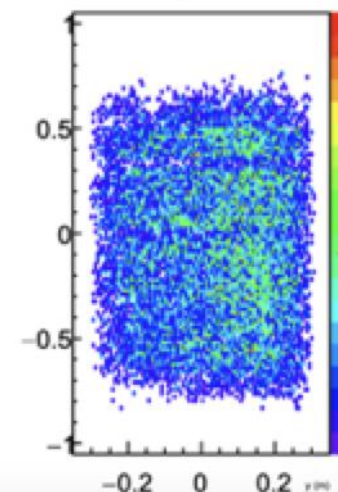
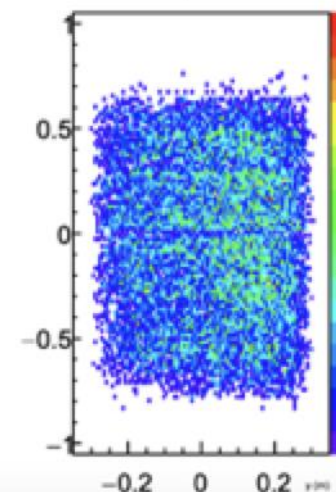
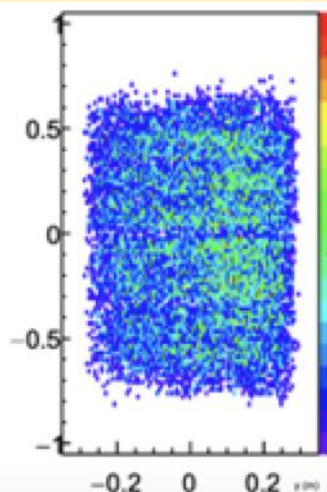
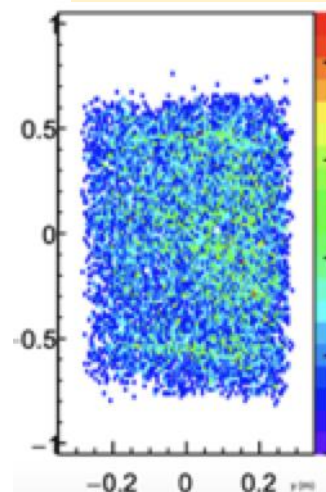
Layer 2

Layer 3



Layer 6

Layer 7

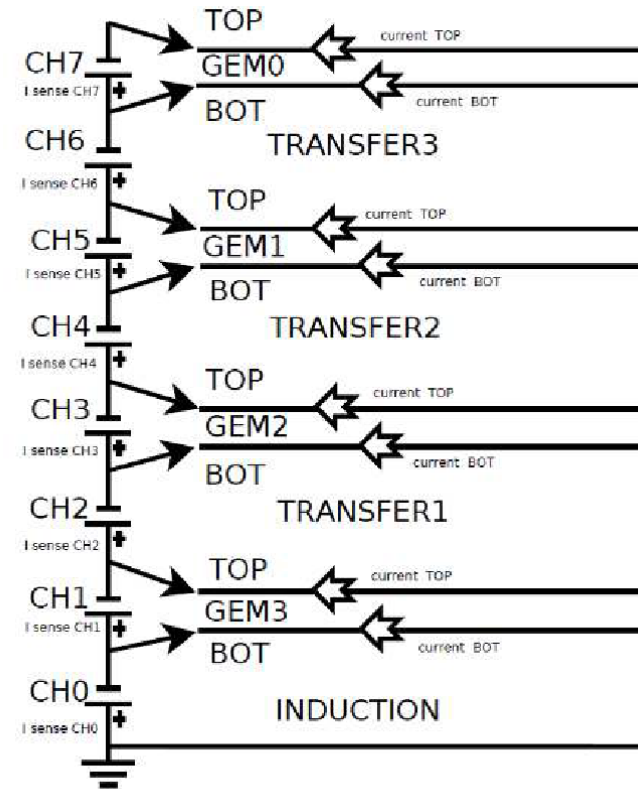
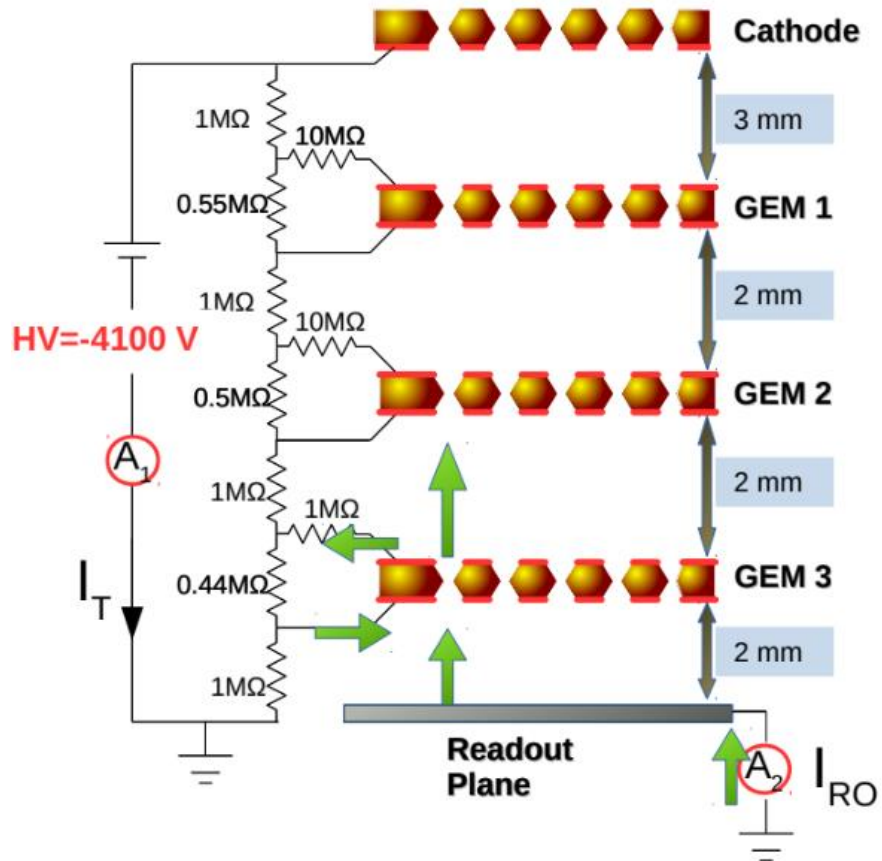


GEN-RP will run with  
all layers next spring  
(prior to GEP)

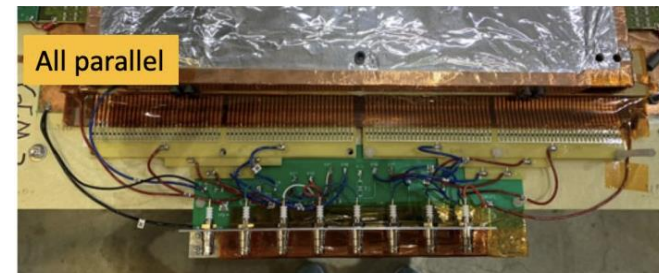
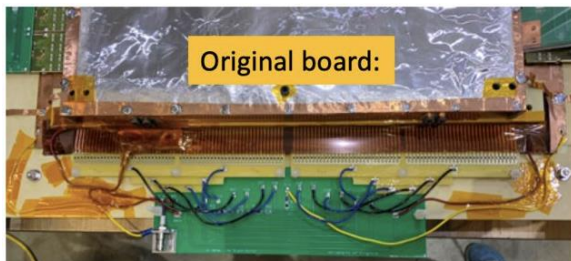


# High voltage individual power supply

Current equivalent to Hit rate x Gain x primary electrons x electron charge

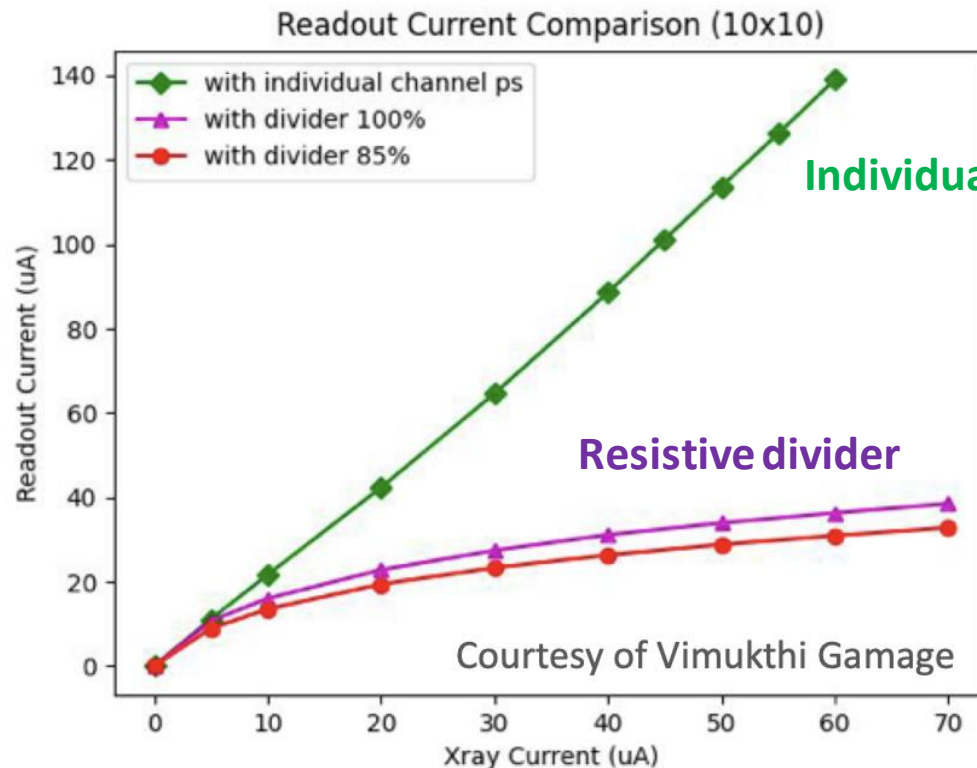


Note:  
protective  
resistors not  
shown  
here....see  
backup



# High voltage upgrades and lessons learned

- Observed a loss of tracking efficiency that was correlated with occupancy due to the HV divider configuration
- Observed a non-linear increase in the current draw with increased occupancy (replicated in the lab in the red curves below) as related to the divider



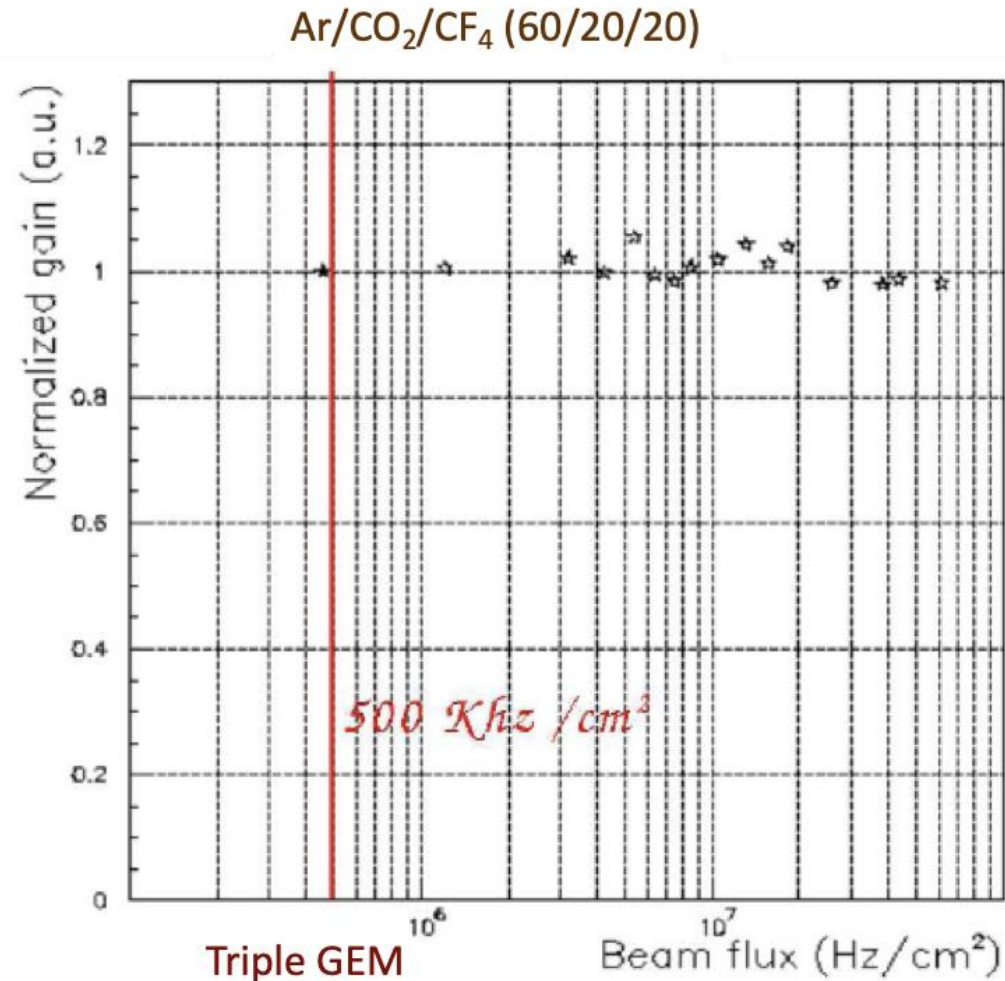
Individual power supply

**Slope** analogous to **gain!**

Recover gain with  
individual power supply

# GEMs have high gain in high rate environment

Current equivalent to Hit rate x Gain x primary electrons x electron charge

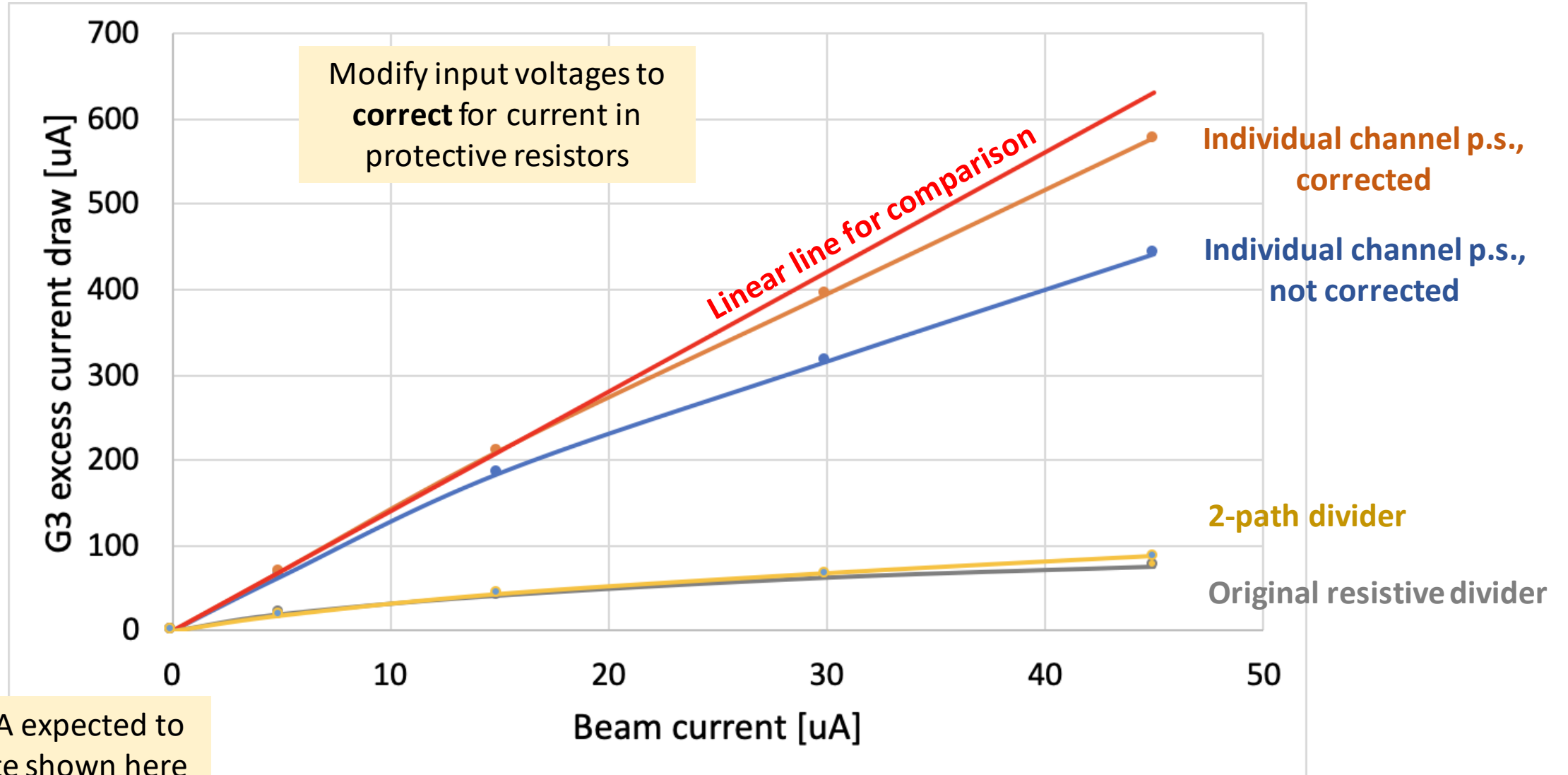


Gain is stable up to high rate (~100 MHz/sq cm)

Poli Lener, PhD Thesis - Rome 2005



# Luminosity scan with different HV divider configurations during GEn (on optics target)



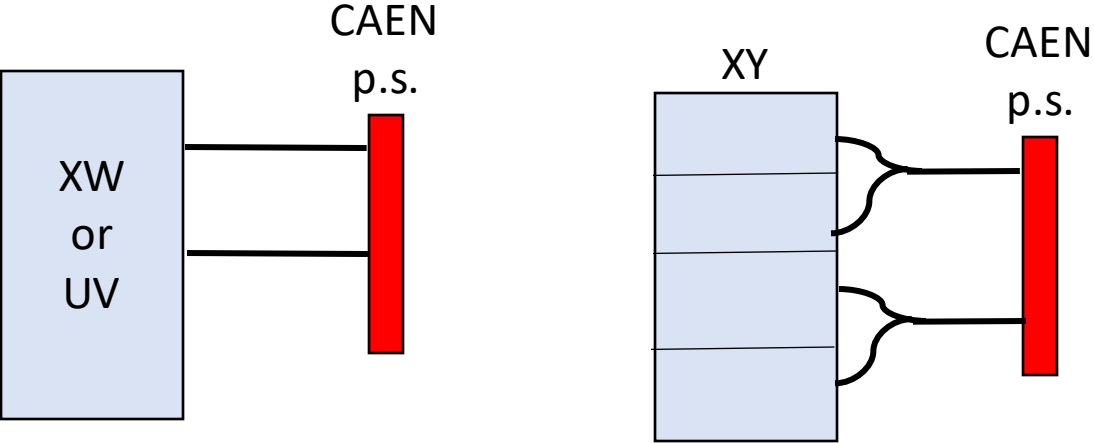
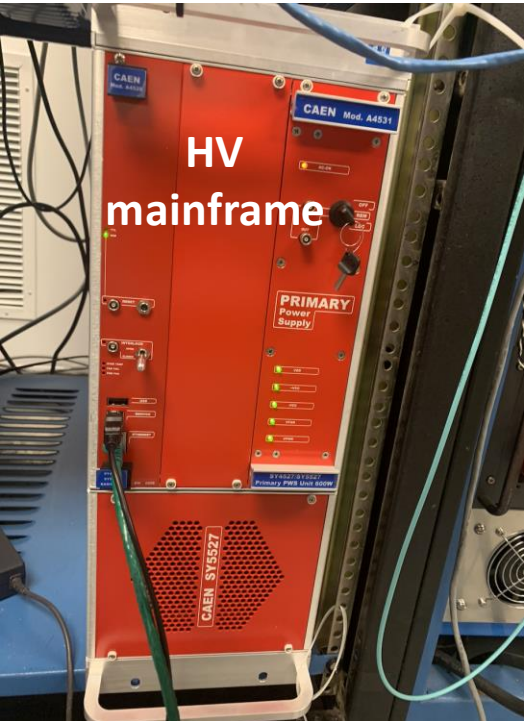
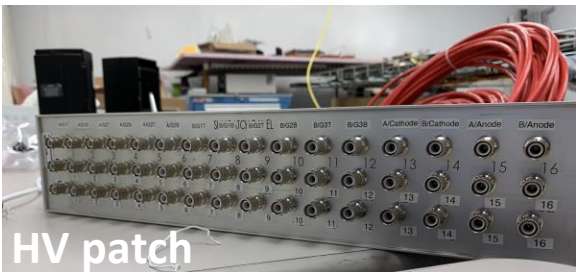
GEp at 50uA expected to increase rate shown here for 45uA by 2.7x

# High voltage

Install parallel-path HV supply on every layer

CAEN A1515BTG designed for triple GEMs:

- 2 channels with 7 outputs each
- 1 mA max per output
- Floating ground
- Can trip together



|                   | Need | On hand | To purchase (\$100k)         |
|-------------------|------|---------|------------------------------|
| CAEN A1515BTG     | 16   | 9       | 7<br>(2-INFN, 2-UVa, 3-JLab) |
| CAEN HV mainframe | 4    | 1       | 3                            |

Simulation shows back tracker receives 40% of the rate of the front tracker

## HV supply schemes to reduce gain drop

- **Use individual power channels for each electrode. Reduce the problem by a factor of 4-8 or more**

- Expensive: cost about \$ 700 per GEM ~ \$ 1 M for SoLID
- Tested extensively at Uva with X-ray illumination
- Then implement on one BB UV chamber for beam testing during Gen-II
- This method just adopted for all SBS GEMs: total cost was ~ \$ 250 k: SoLID can reuse some these supplies to bring down cost.

- **Build an active divider**

- We are working with a CERN GEM electronics group to build this
- ~ 1-2 year project.
- Cheaper, but need to make sure no extra noise.
- No other GEM group made this work yet
- Need support from Jlab electronics group

10



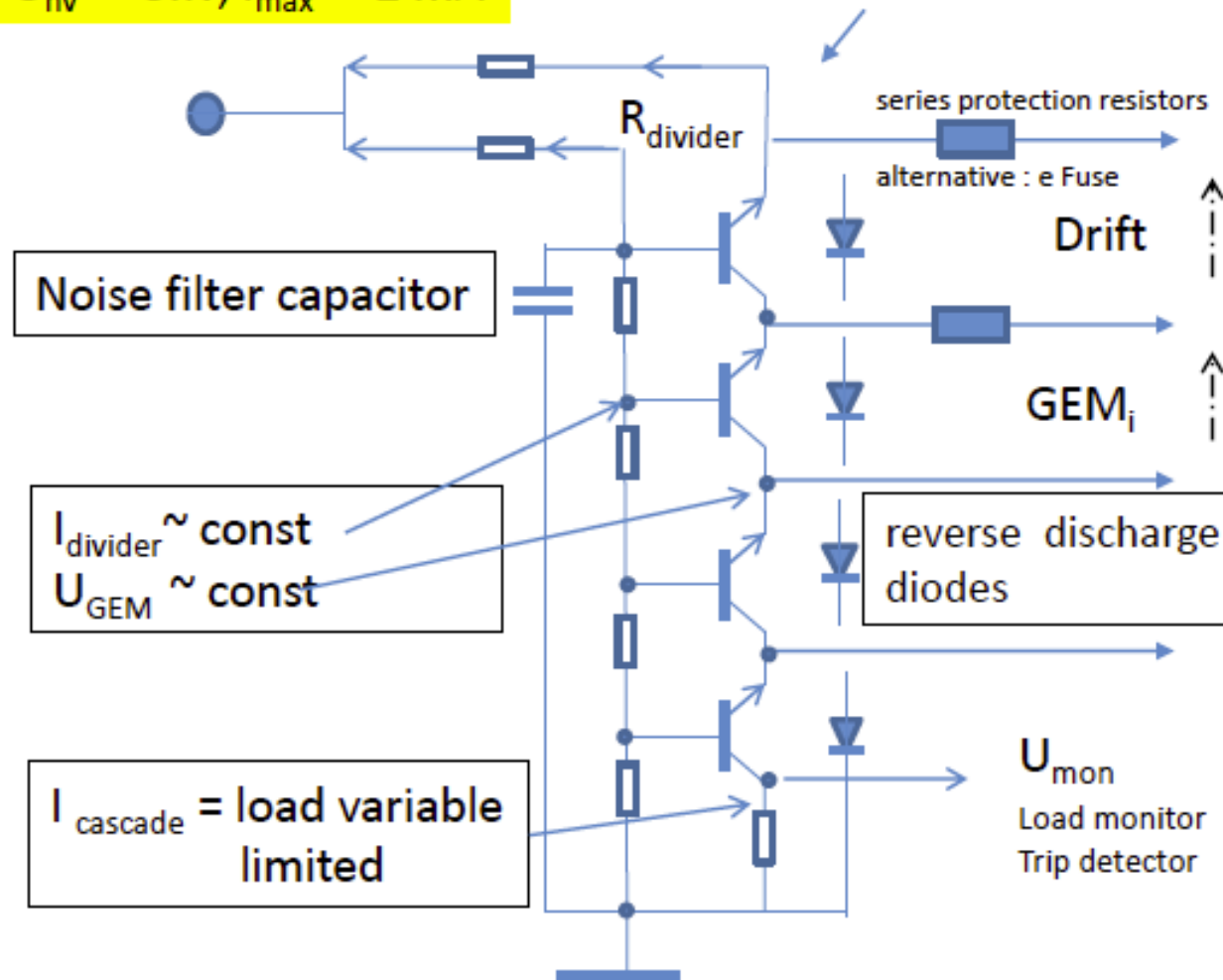
# AVD basic principle npn:

## max 600V between stages

$$U_{hv} = -5kV, I_{max} = 2 \text{ mA}$$

npn HV Transistor cascade

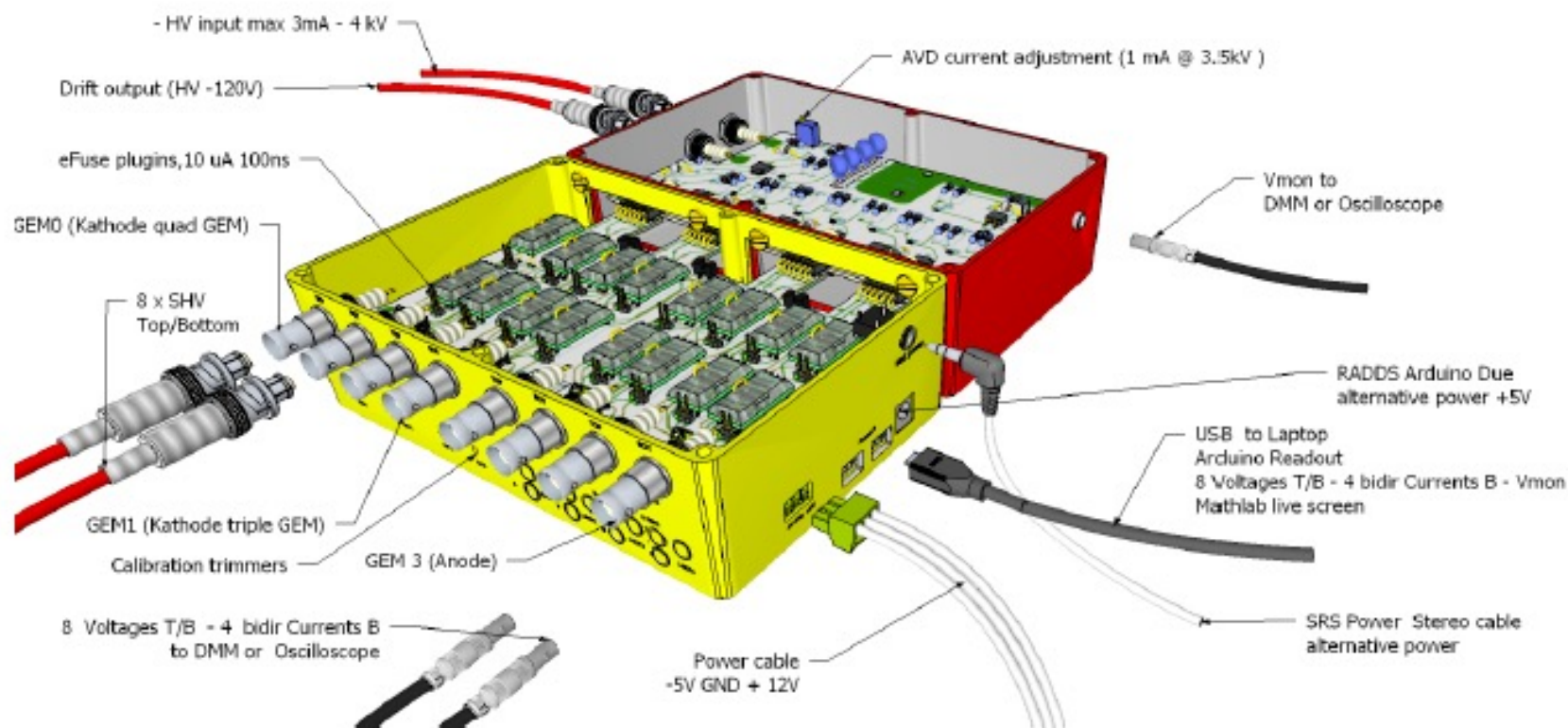
Principle:



- GEM Voltages follow Voltages of resistor divider by  $\sim 0.8 \text{ V}$  but at low output impedance ( $\Rightarrow$  constant voltage)
- load dependent currents flow Through transistor cascade, current load through  $R_{divider}$  divided by gain of the transistors ( $\sim 100$ )
- Regulation max 600 V for Drift and GEM<sub>i</sub>
- Primary filter capacitor decoupled From discharge into detector
- Dynamic currents available as  $U_{mon}$  for load monitoring and HV trip of all load-induced currents.
- $U_{mon}$  available as very fast trip signal for primary HV supply
- Reverse diodes discharge detector at ramp down

Advantage npn: voltages follow closely  $R_{divider}$   $U_{EB}$  variation  $\pm 0.2 \text{ V}$  @  $T = \text{const}$   
 Disadvantage npn:  $I_{EB}$  forward currents  $O(5 \mu A)$  reflect up 5% load into  $R_{divider}$

# AVD<sub>2015</sub> Prototype Implementation



2016: put all (including external HV module) into a single box

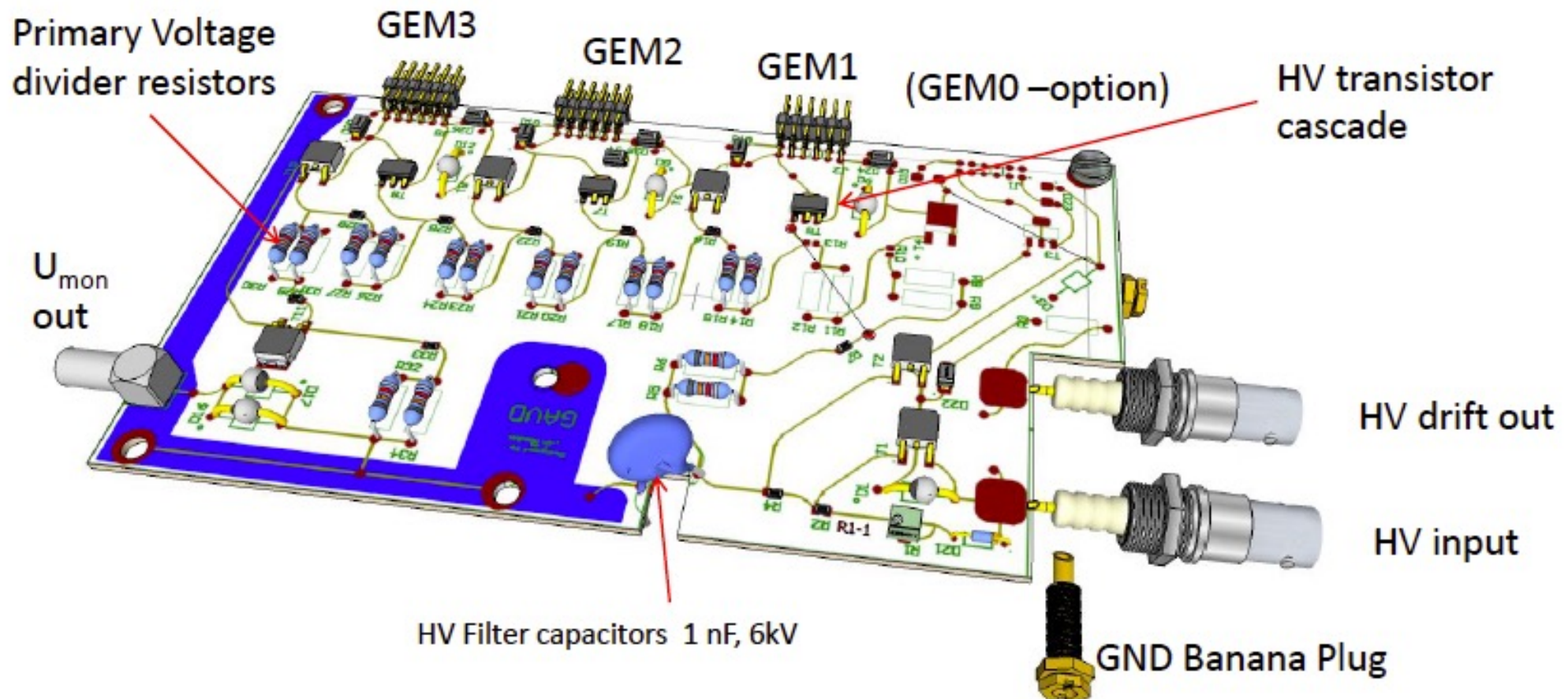
was successful but quite bulky

# AVD<sub>2015</sub> board

( single layer, ceramic )

⇒ make some component and connector updates

⇒ fit into NIM module PCB size





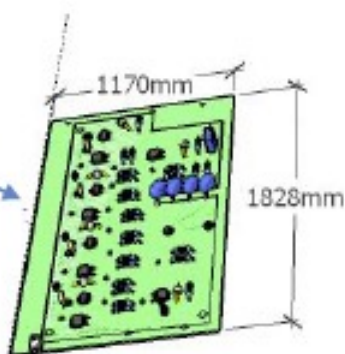
# 2022 re-boxing of AVD: fit in NIM module (shown status 2017)

External HV Power

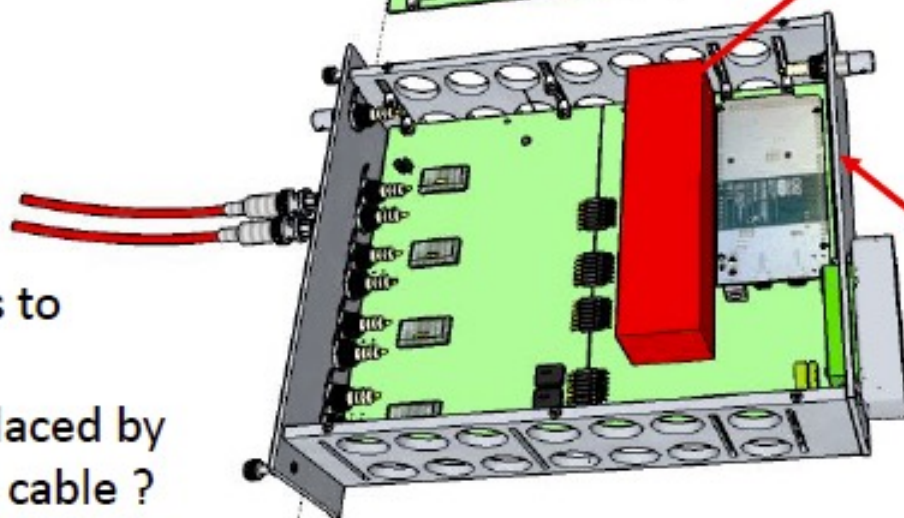
2016: embedded HV module

2022: external HV supply preferred

New PCB



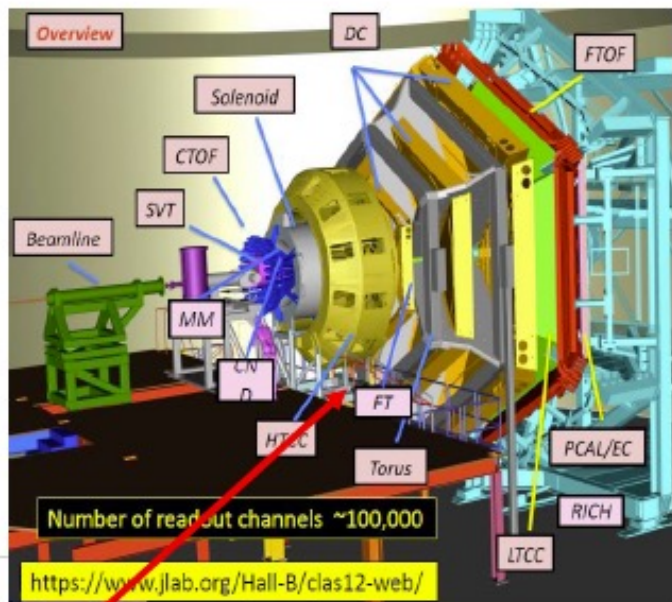
HV cables to  
Detector  
to be replaced by  
single HV cable ?



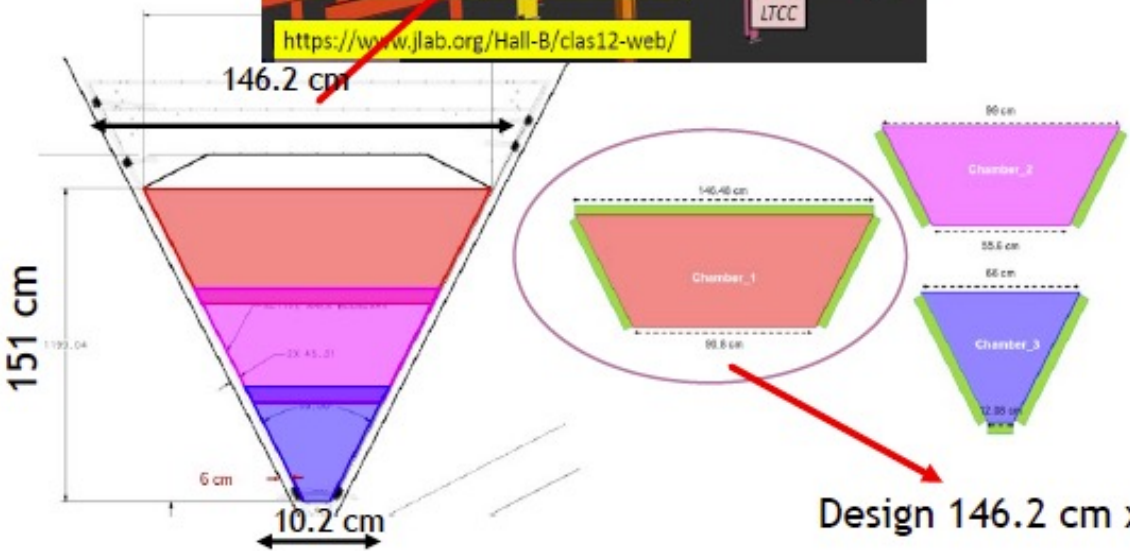
2016 Arduino card  
2022 replace by PYBD plugin  
much smaller, uPython,  
USB , wireless  
I2C , 10 bit ADCs

# Full size prototype of $\mu$ RWELL detector

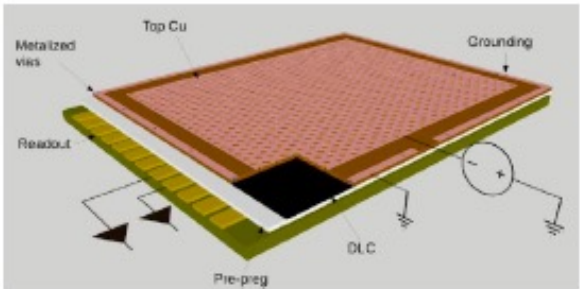
## Hall B of JLab: Upgrade of CLAS12 Forward Tracker with “ $\mu$ RWELL” detectors



- Goal for upgrade: achieve higher luminosity  $2 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$  than current running conditions  $0.7 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  per nucleon
- Limiting factor is forward tracker (FT)
- Introduce  $\mu$ RWELL technology in FT detectors
  - Low-material budget detector; “low mass”

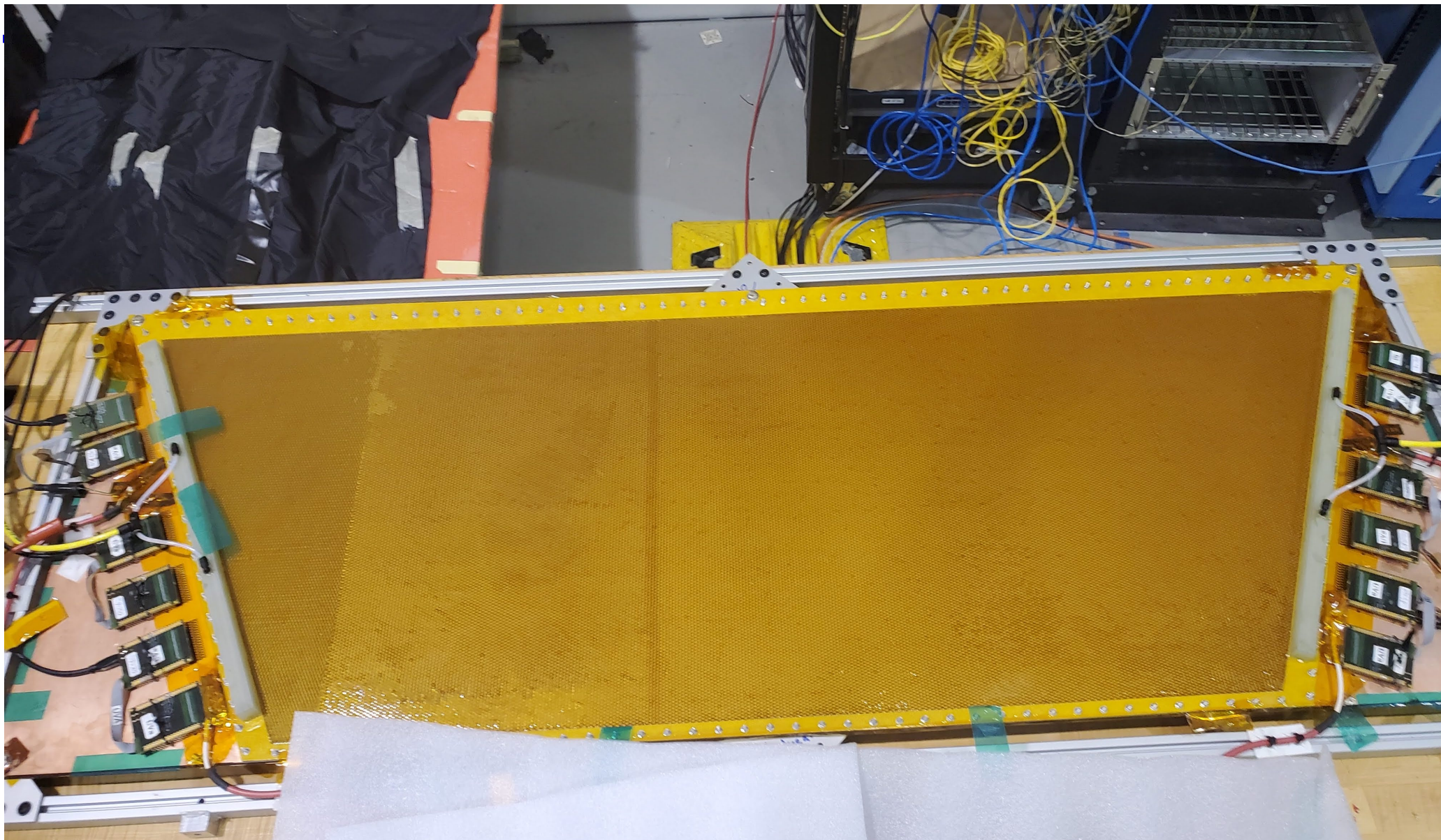


### $\mu$ RWELL technology



Design 146.2 cm x 101.2 cm Chamber 1 prototype at UVa/JLab





Large area uRwell prototype under testing at Jlab

# GEM R&D needed before production

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- Engineering designs for all sizes
- Several (3-4) prototypes of different sizes at Uva
- 1-2 large uRwell prototypes to establish the concept for the two large wheels.
- 2-3 prototypes at each of the partner institutions (MIT, SBU ?)
- One pre-production prototype for each size