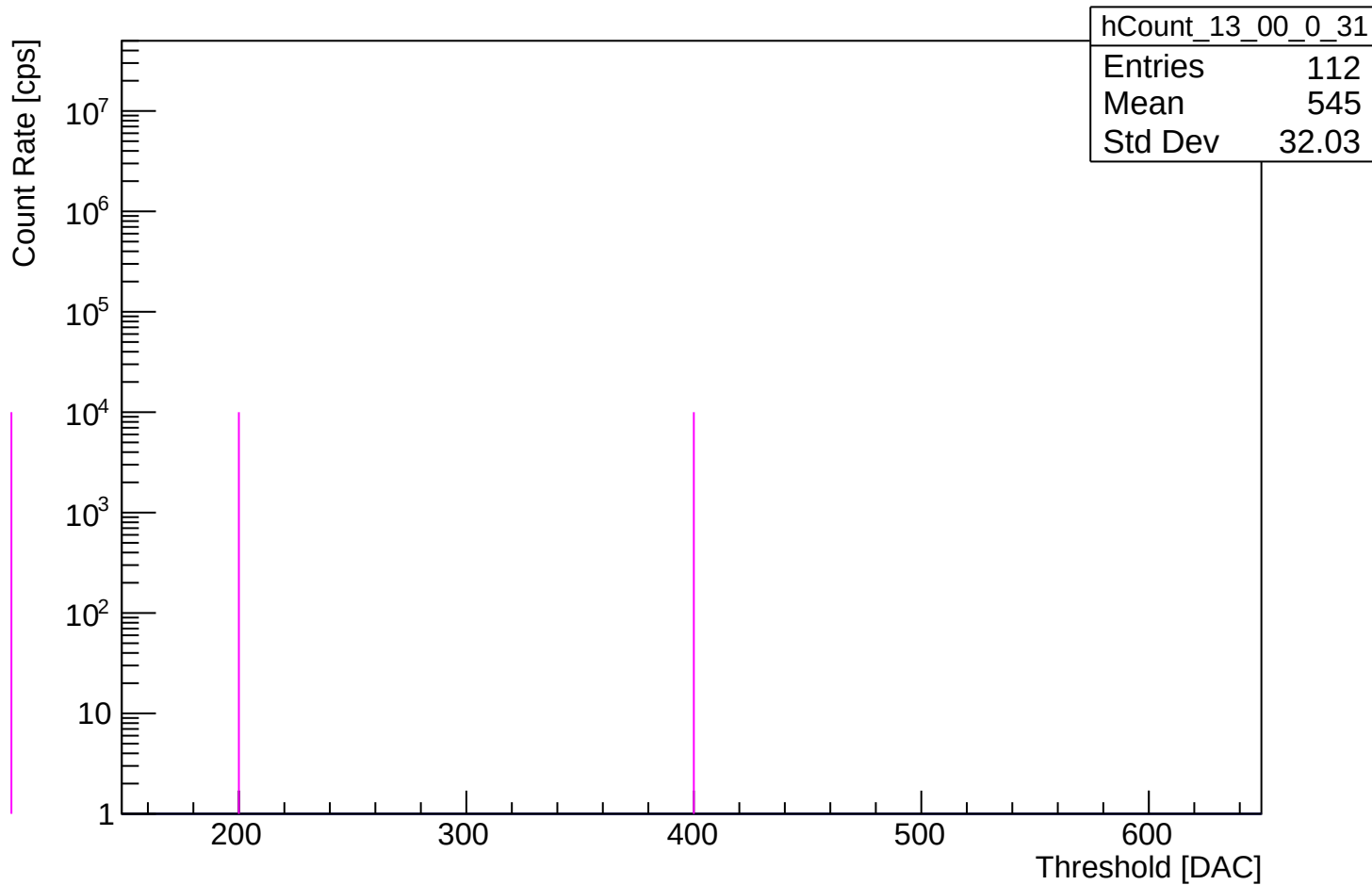
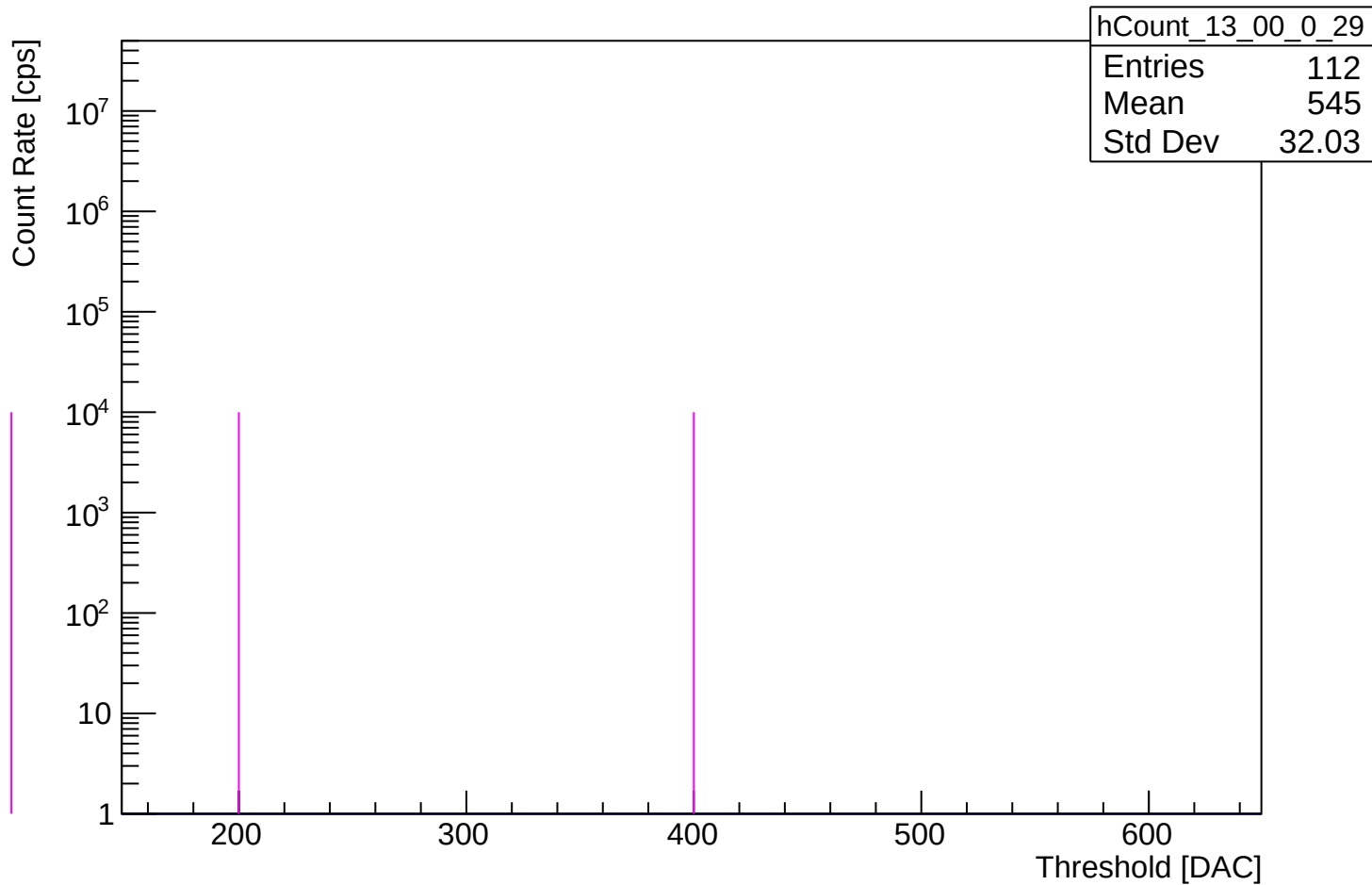


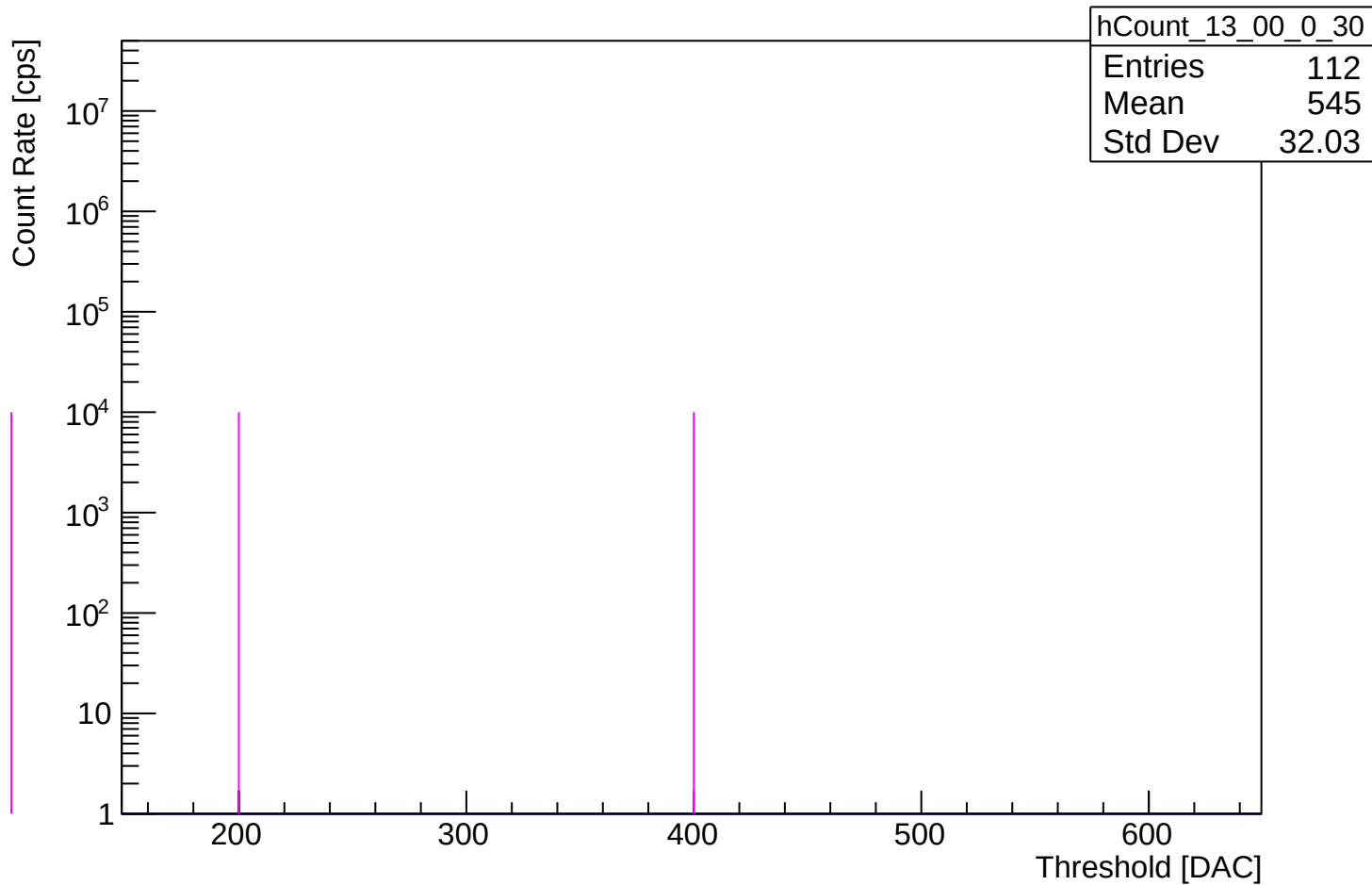
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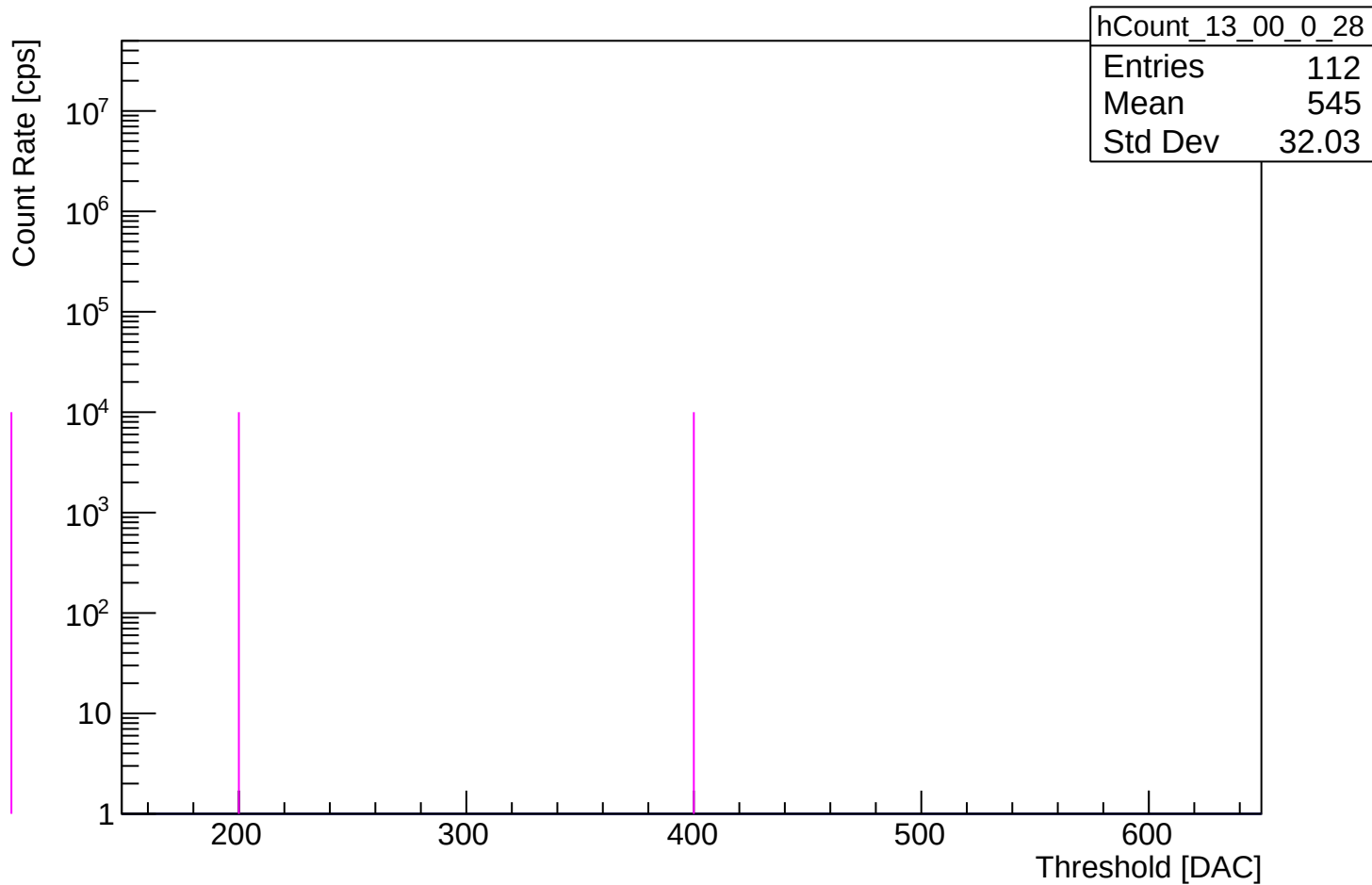
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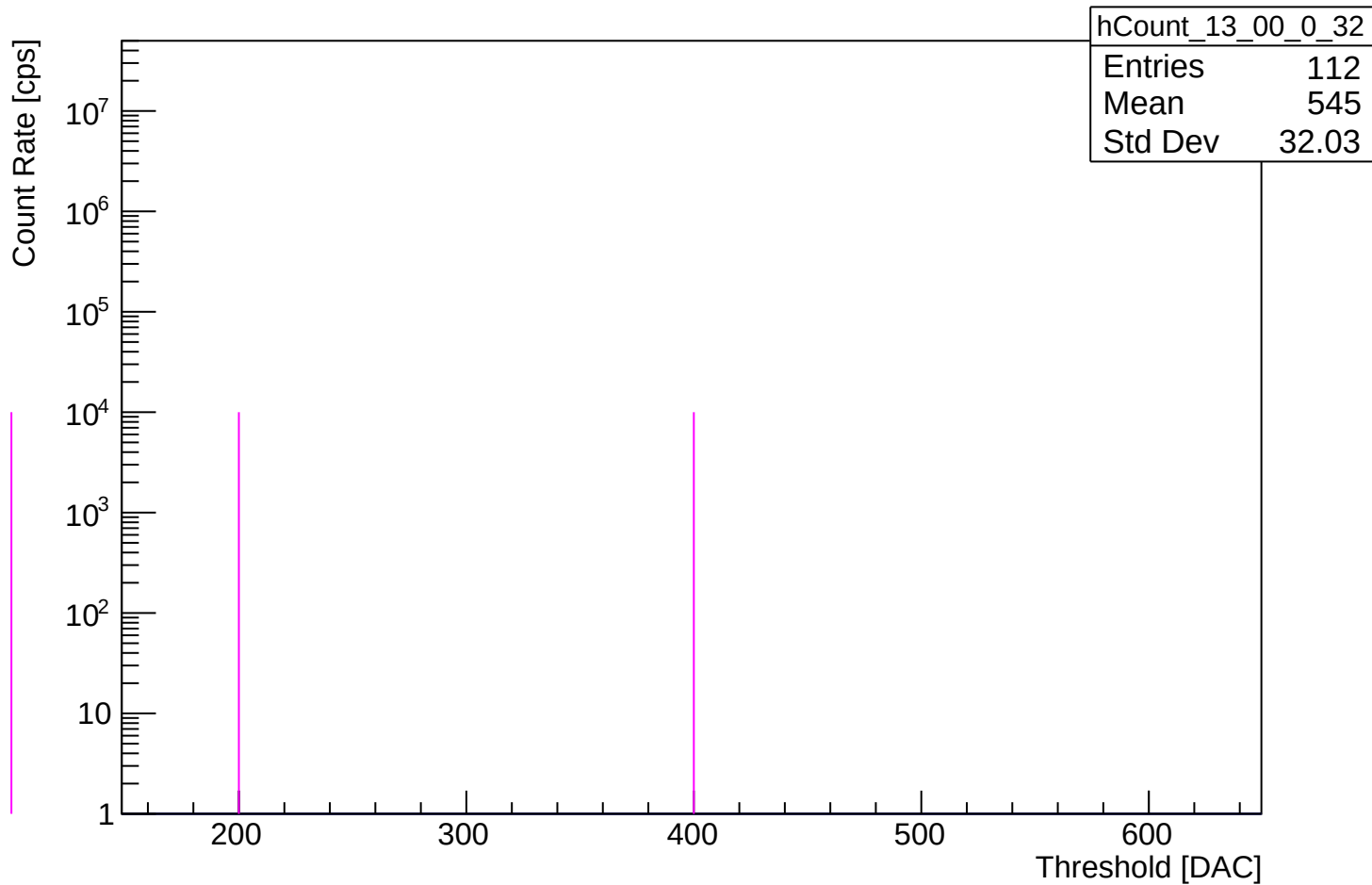
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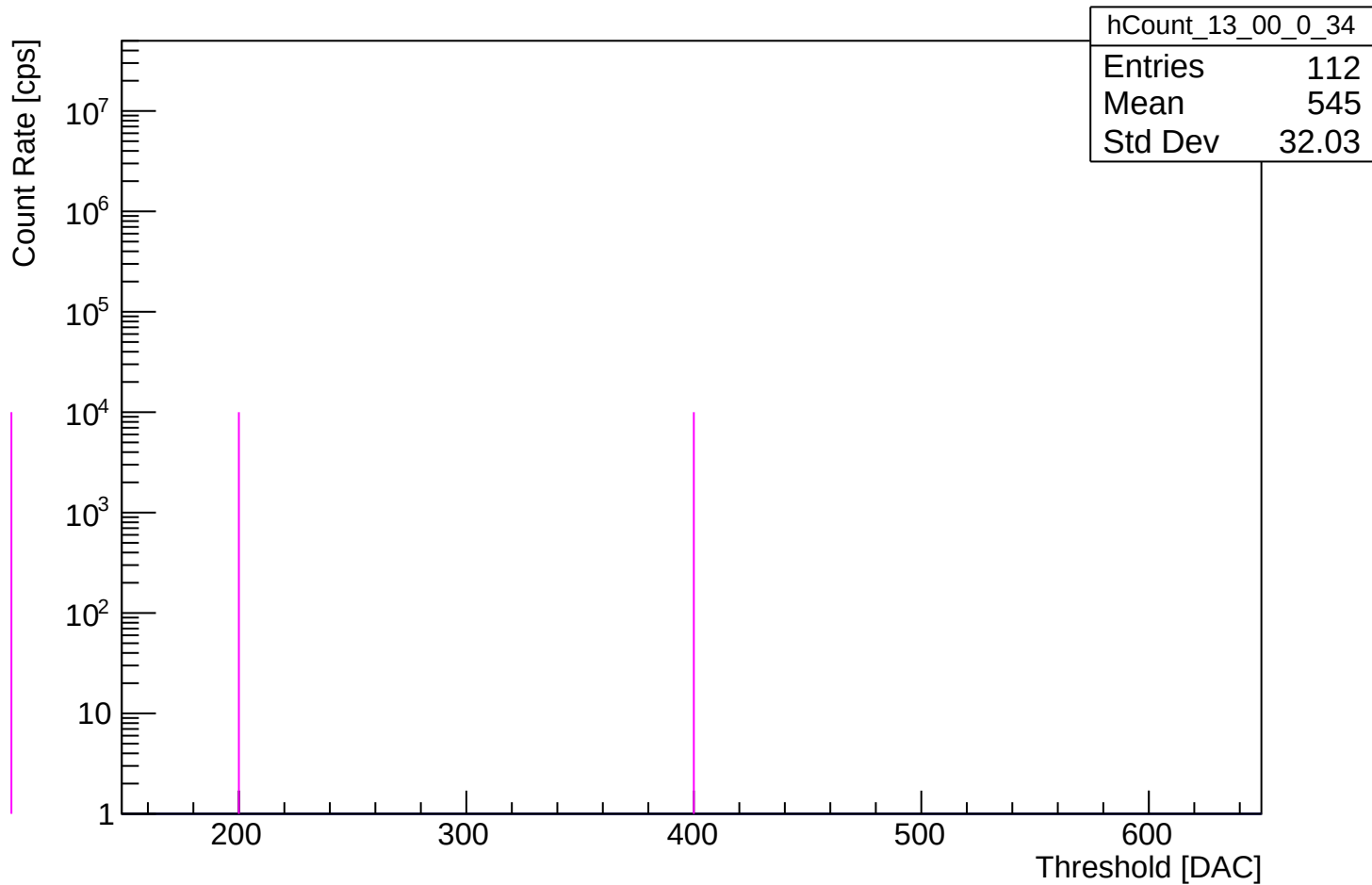
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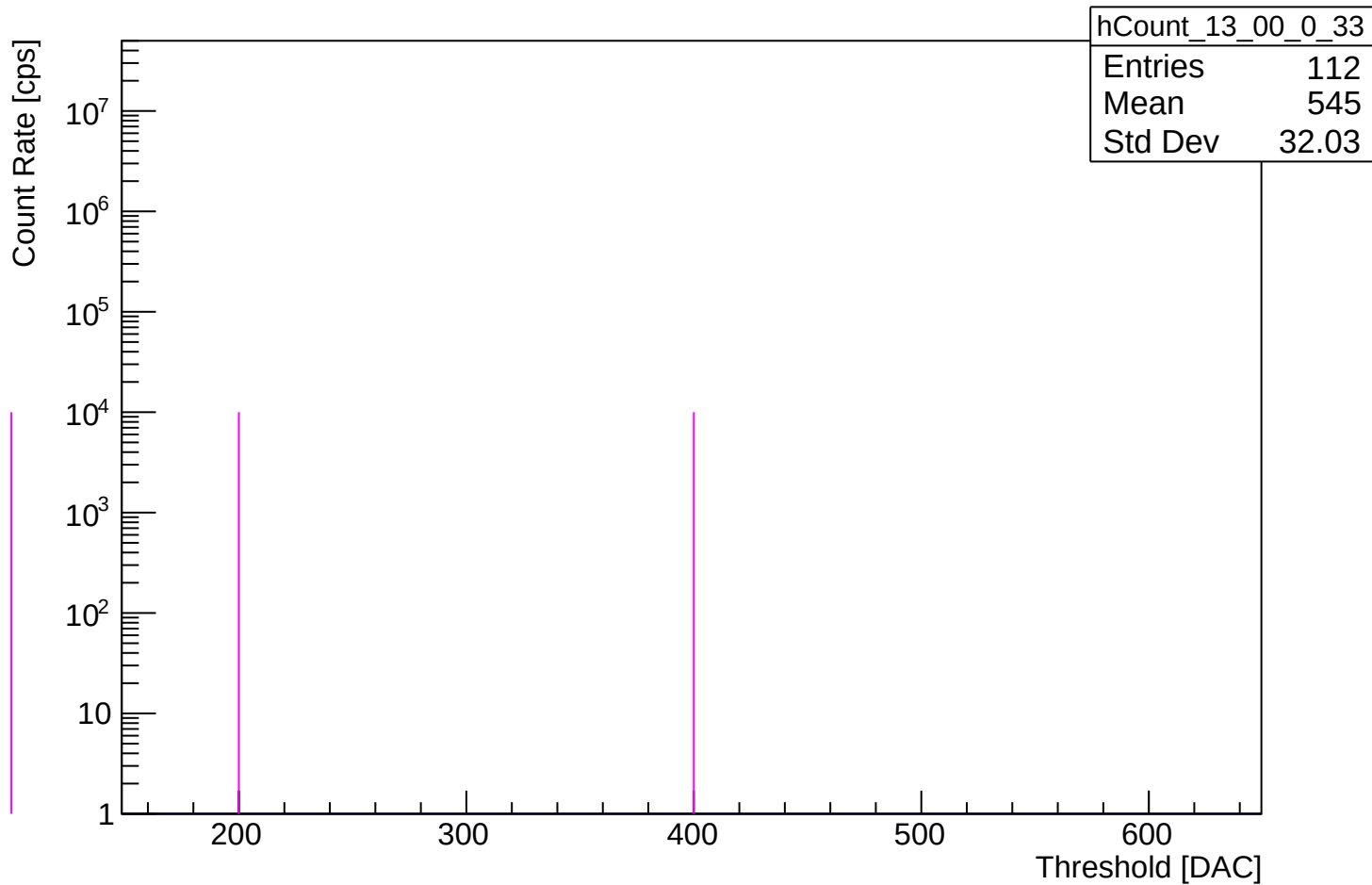
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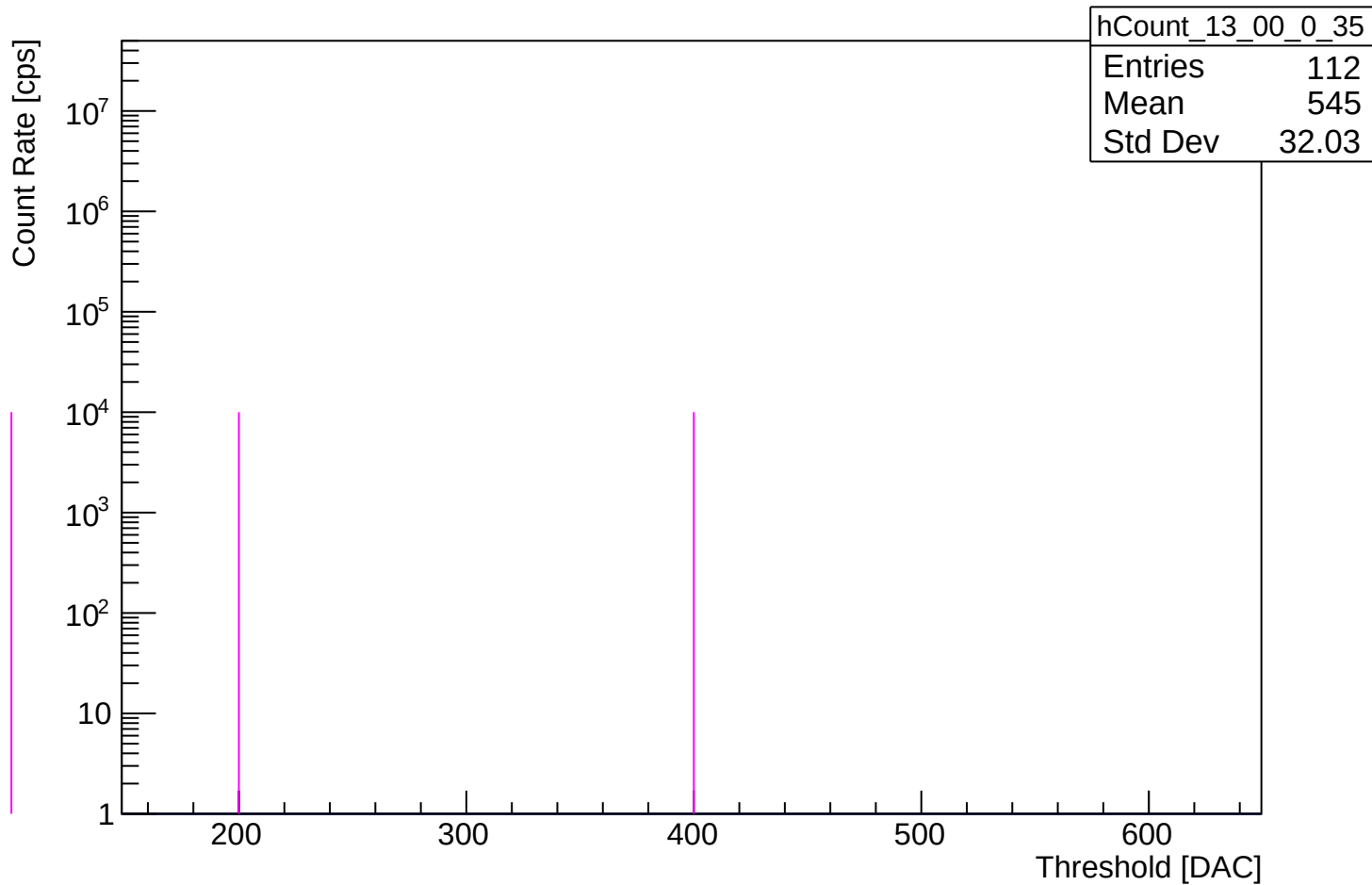
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Row 1 Tile 1 Pmt 1 Pixel 7 Slot 13 Fiber 0 Asic 0 Channel 33

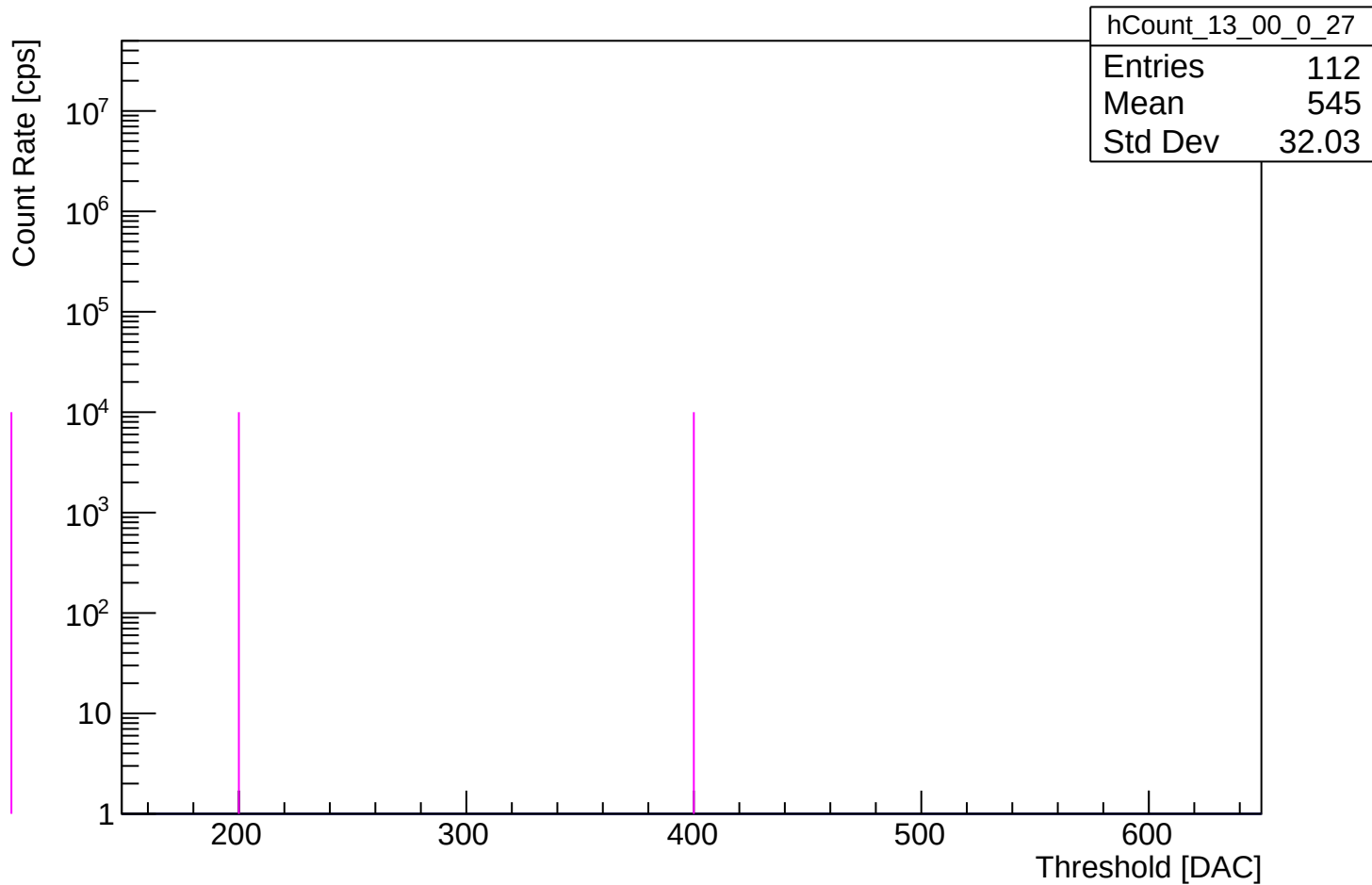


Row 1 Tile 1 Pmt 1 Pixel 8 Slot 13 Fiber 0 Asic 0 Channel 35

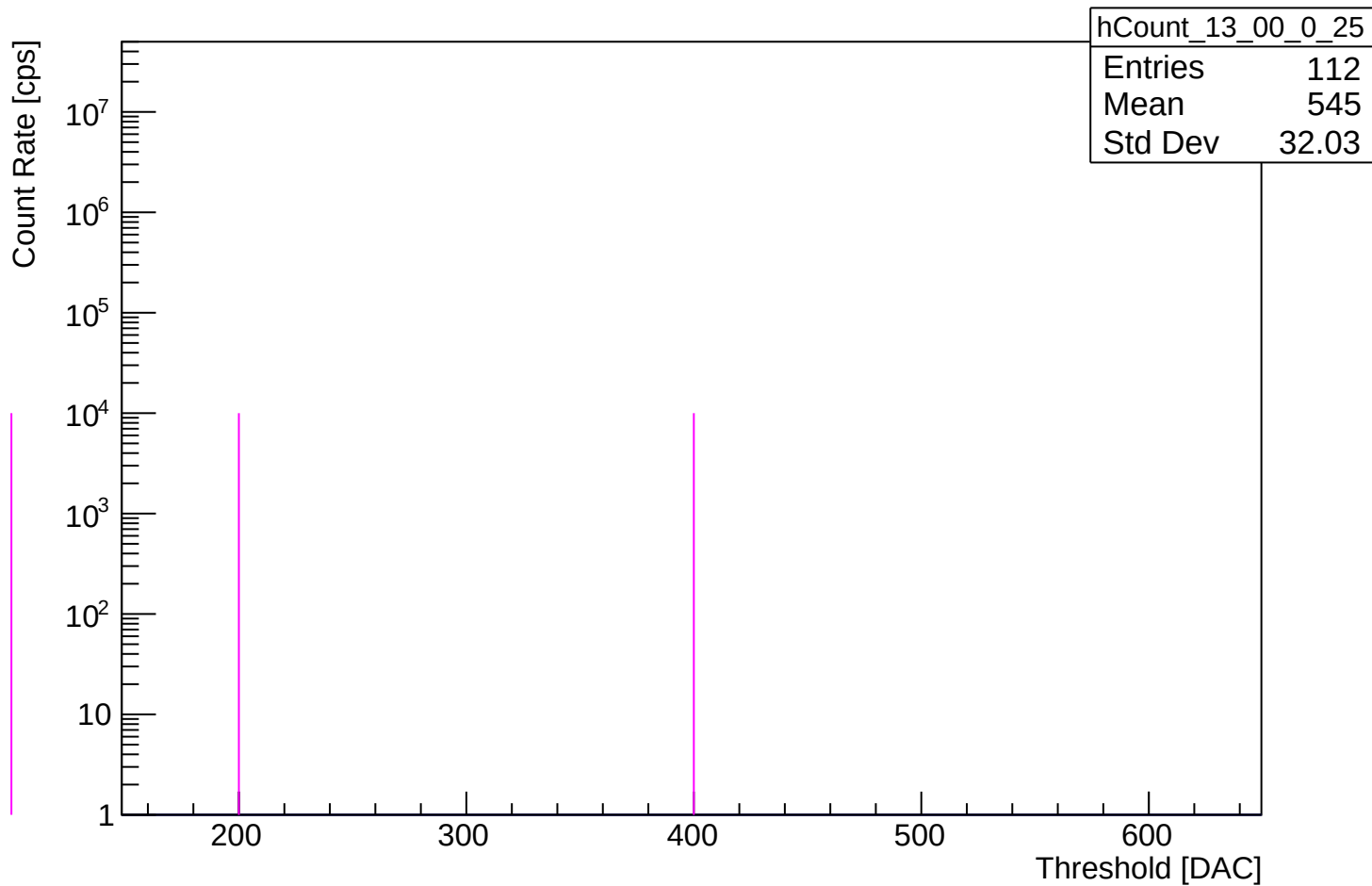




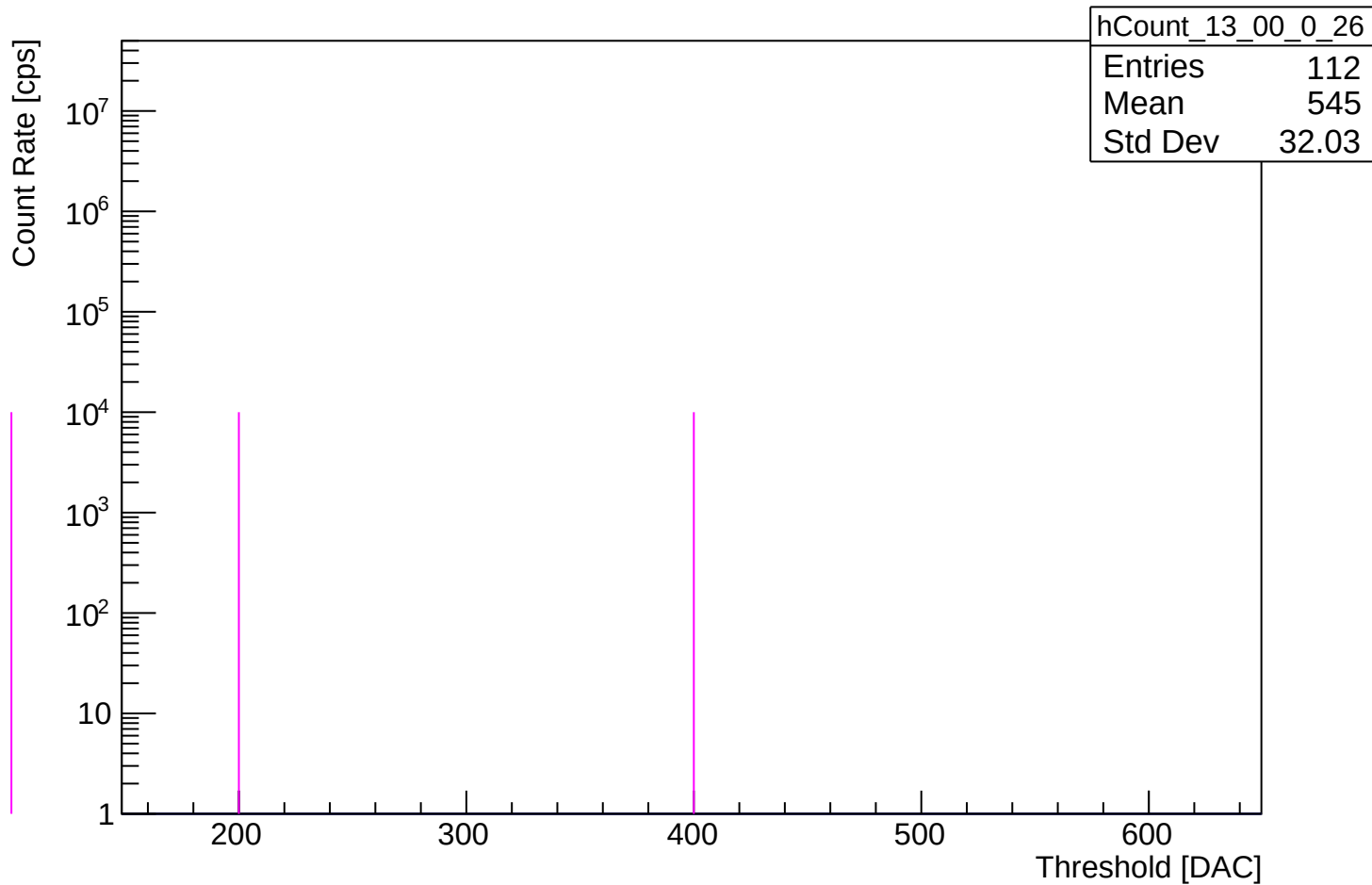
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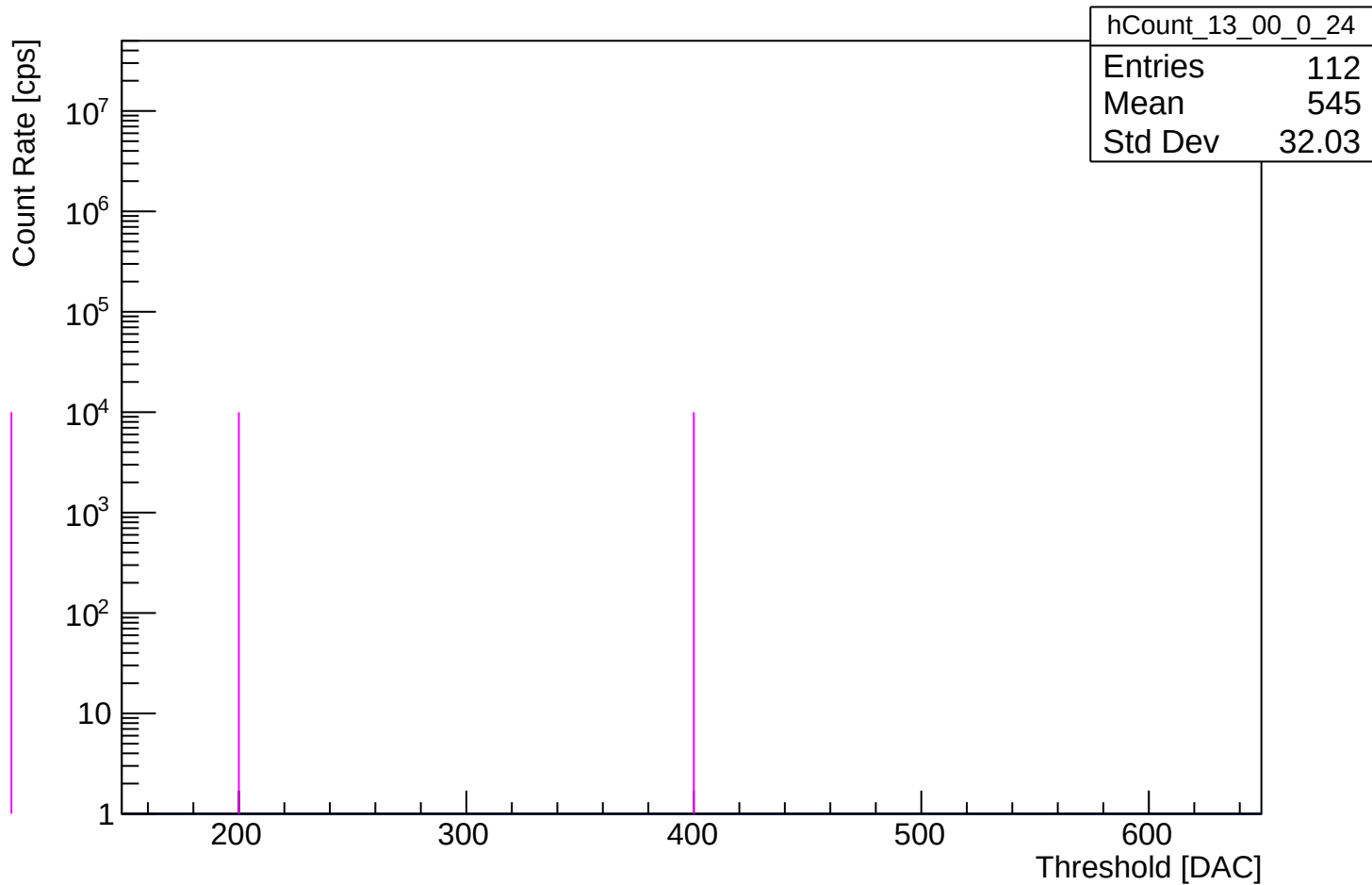
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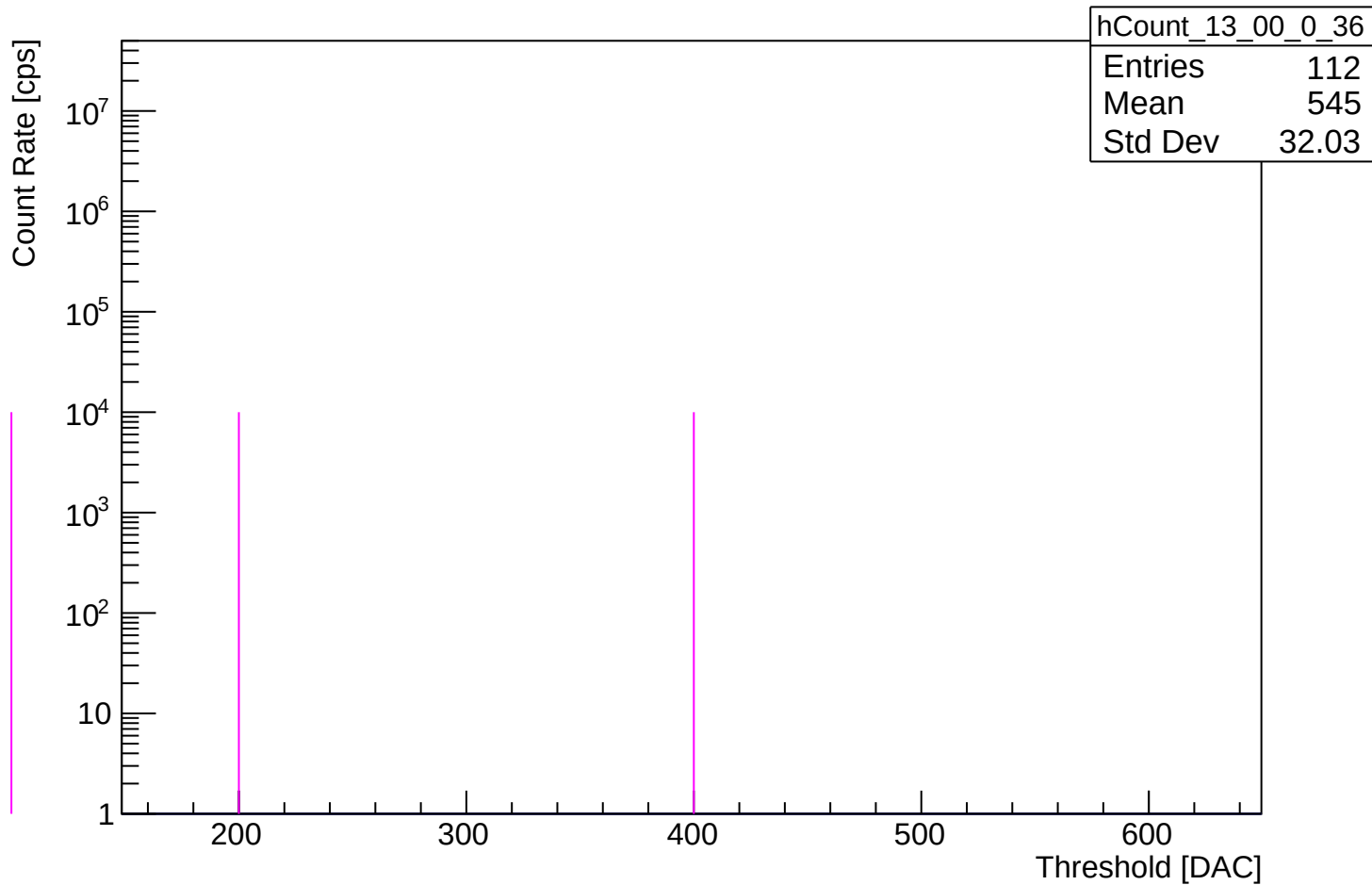
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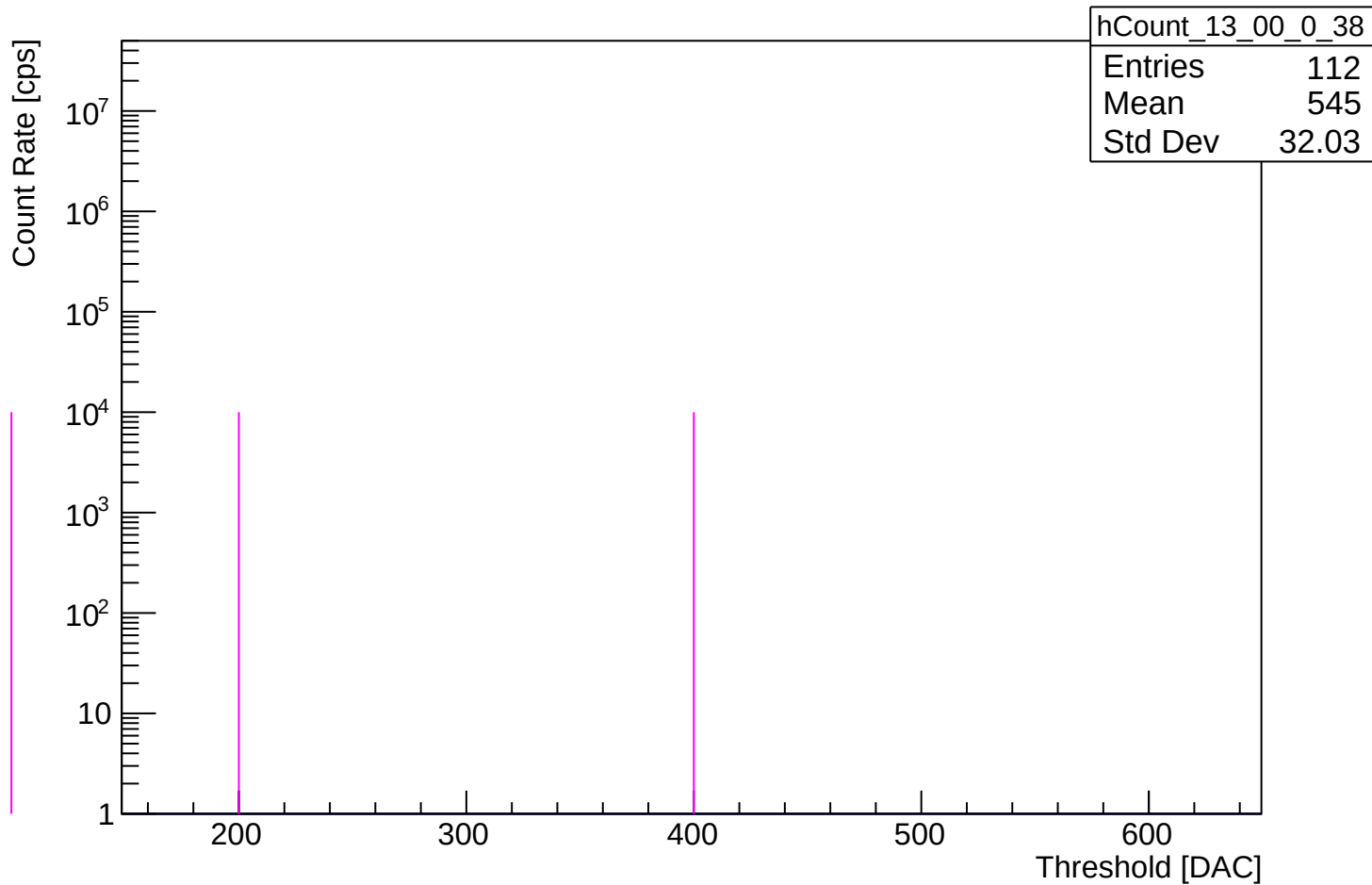
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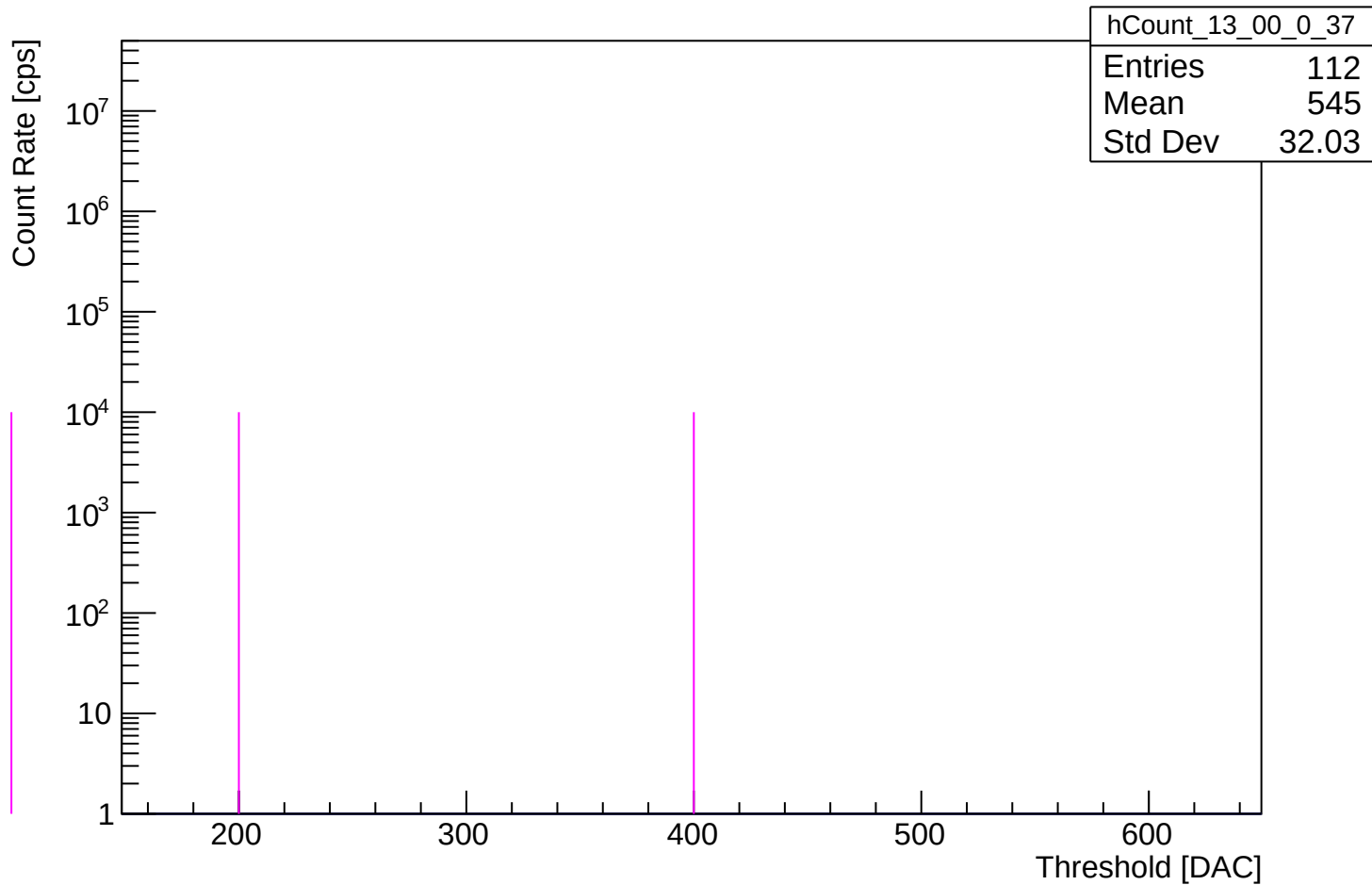
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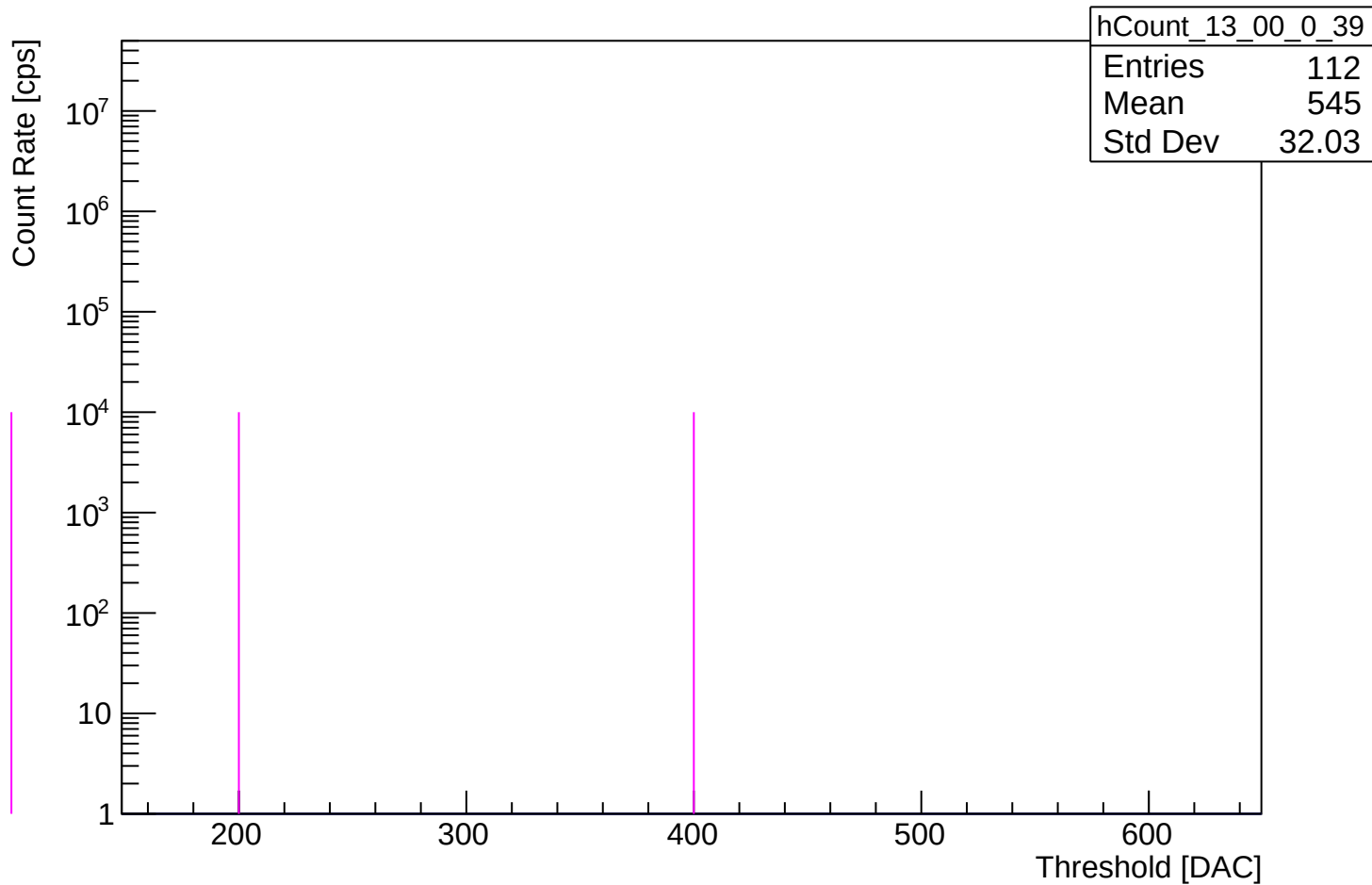
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Row 1 Tile 1 Pmt 1 Pixel 15 Slot 13 Fiber 0 Asic 0 Channel 37

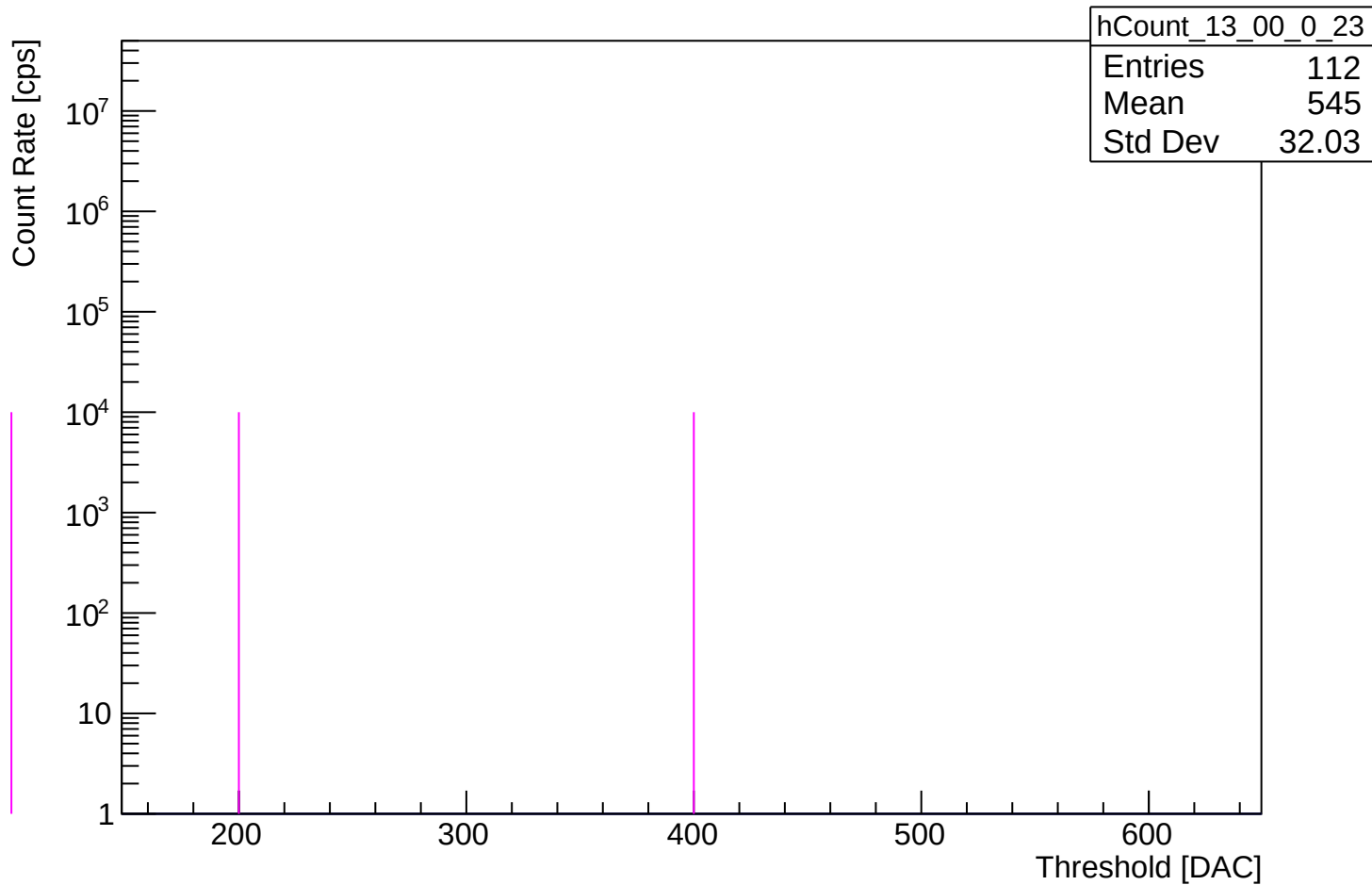


Row 1 Tile 1 Pmt 1 Pixel 16 Slot 13 Fiber 0 Asic 0 Channel 39

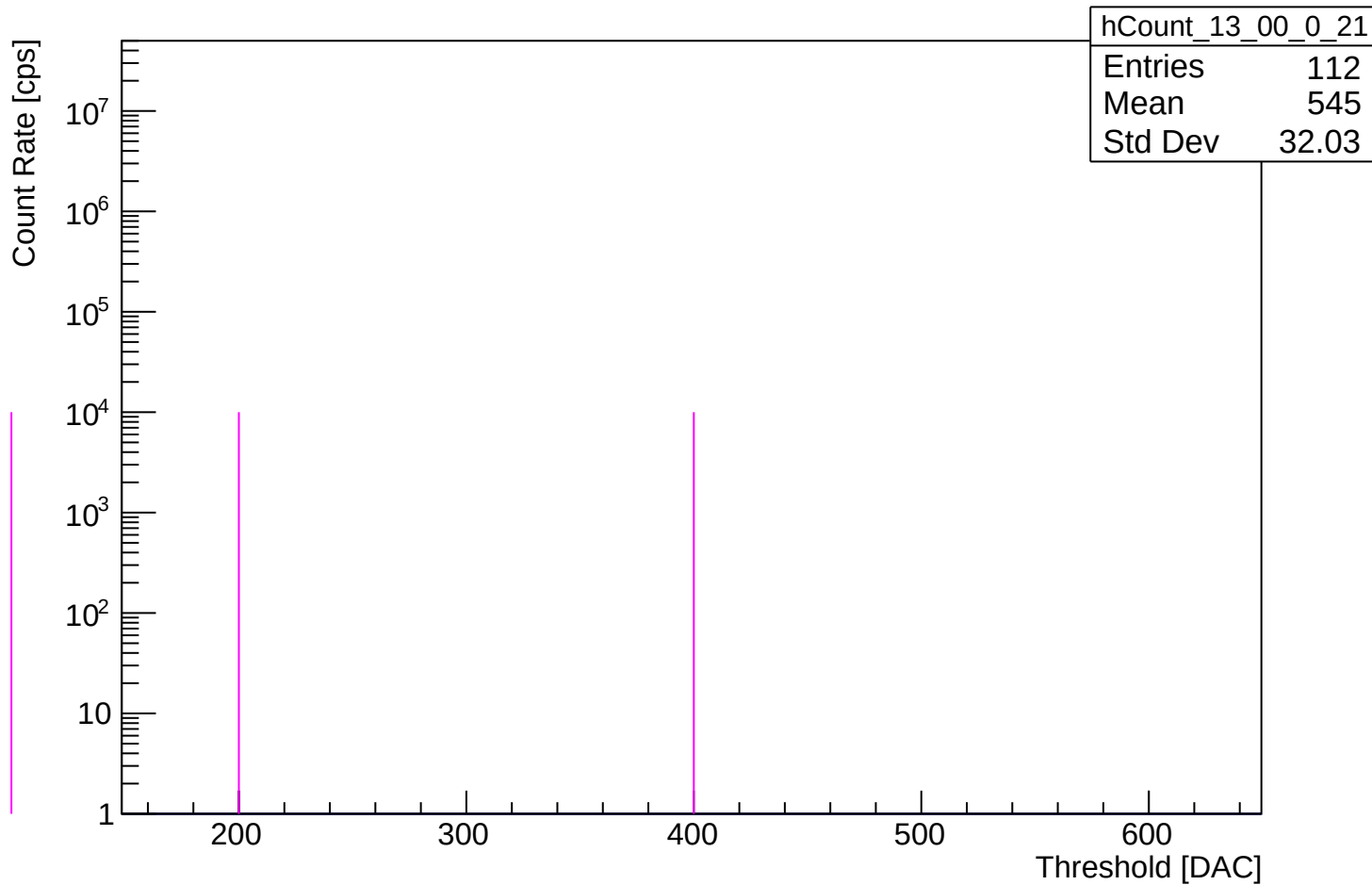




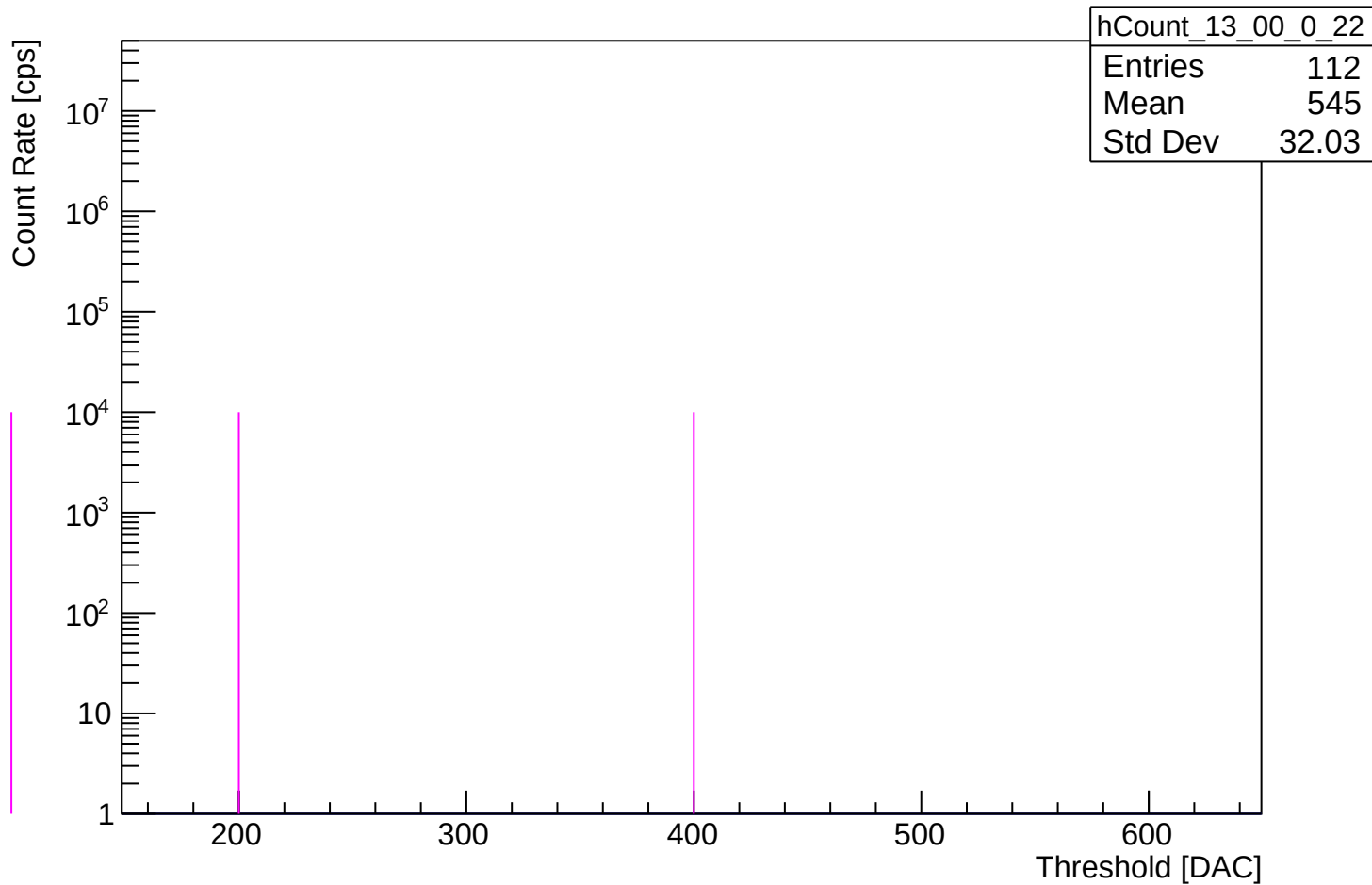
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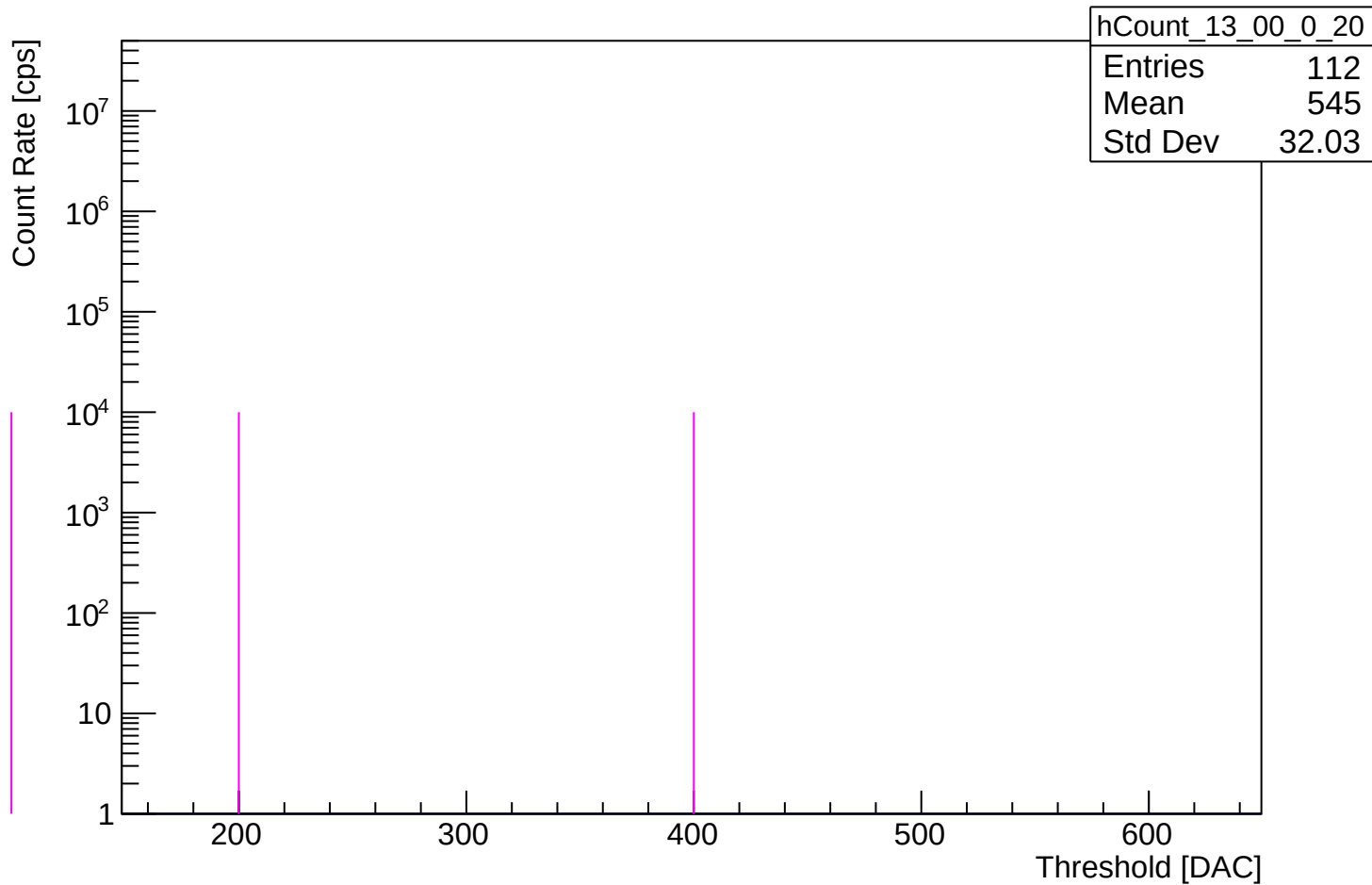
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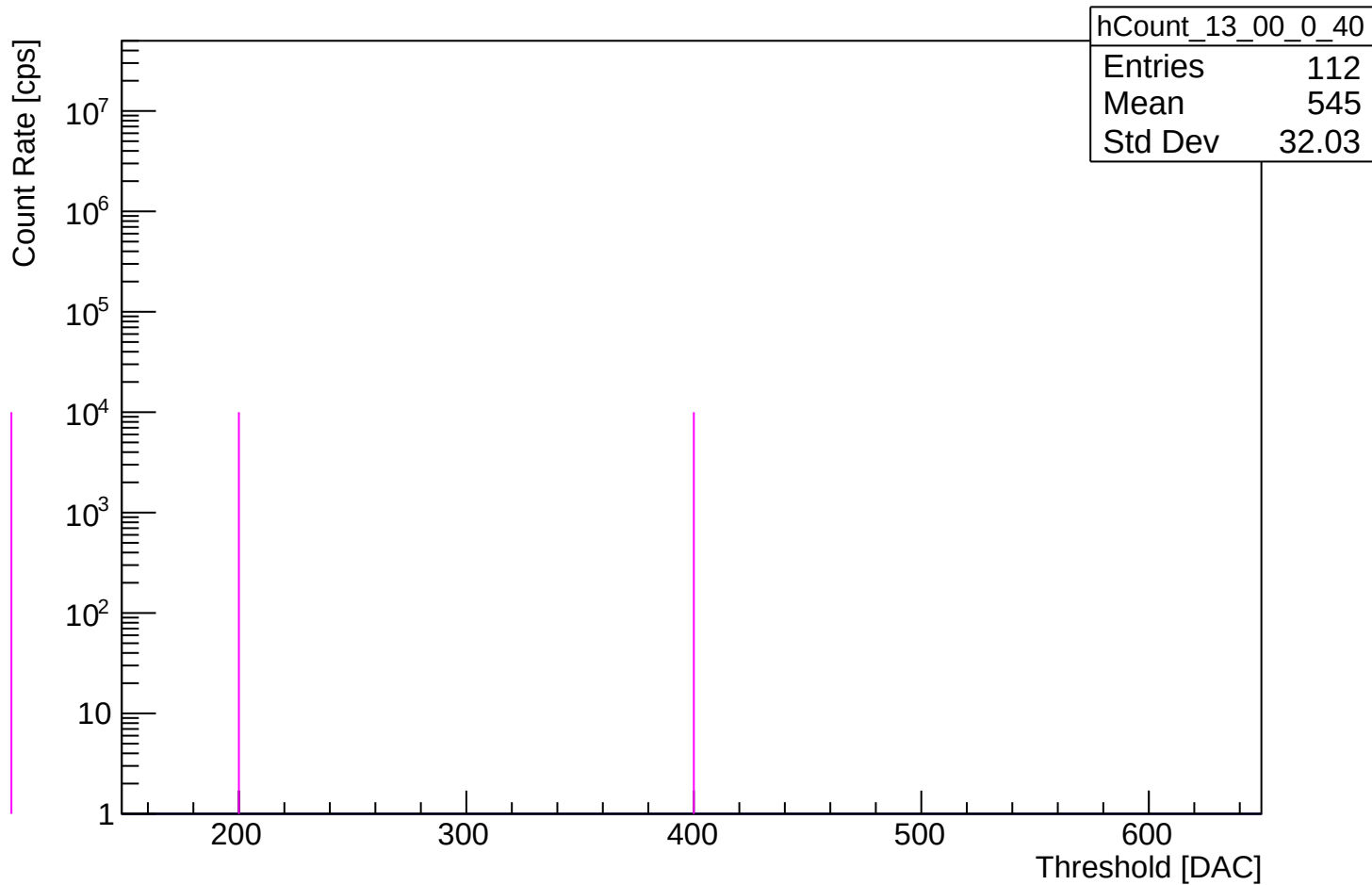
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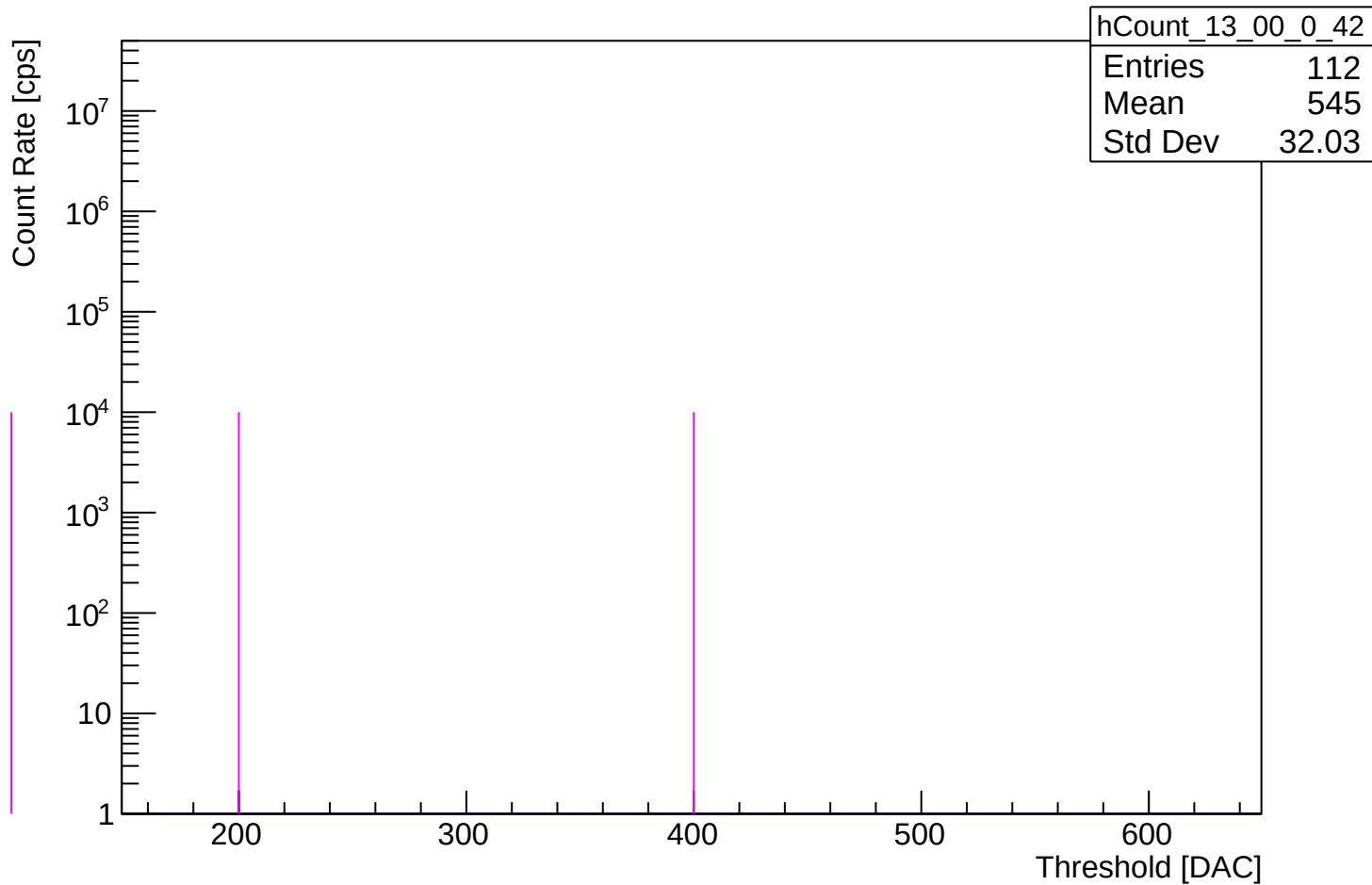
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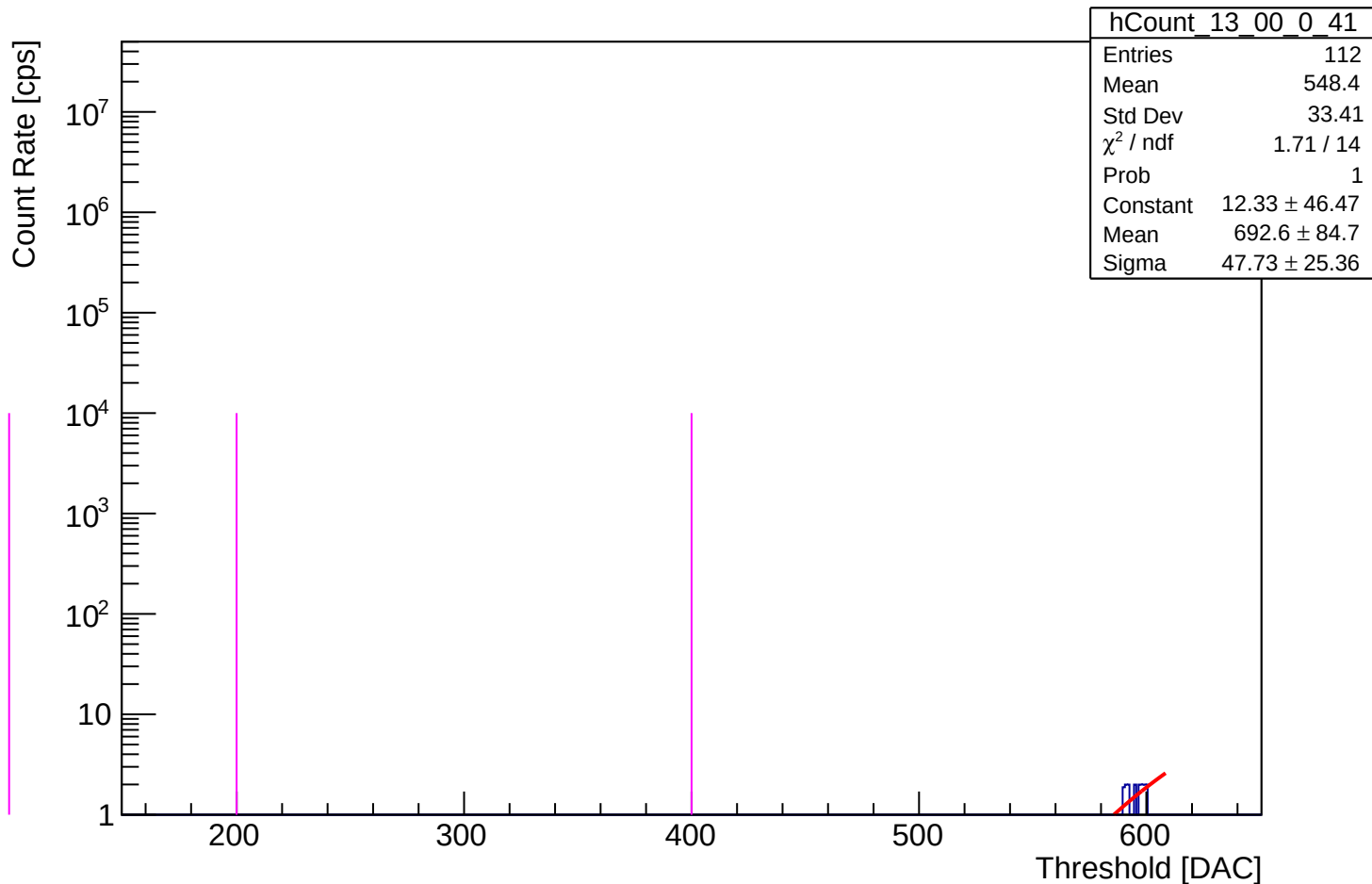
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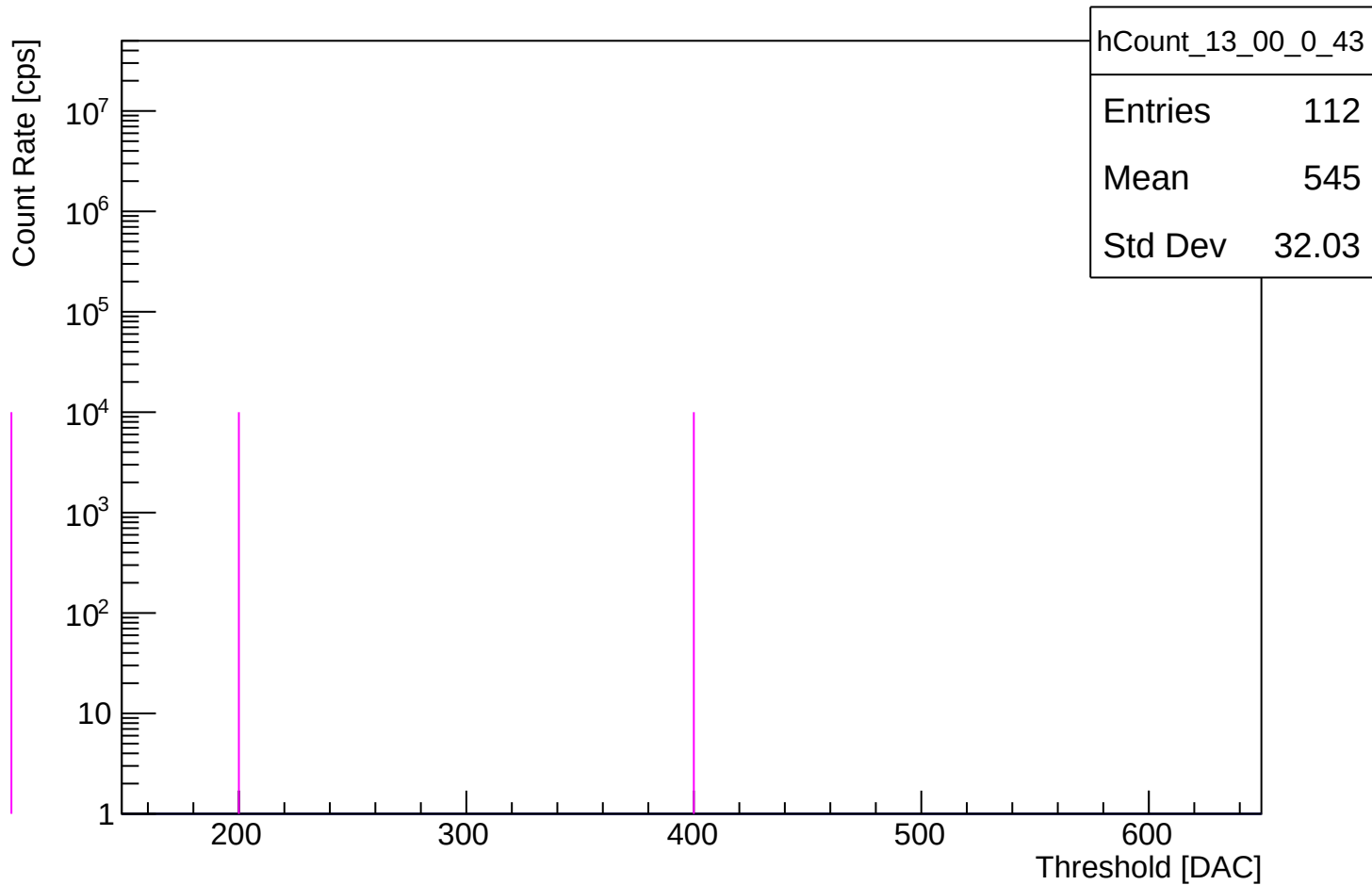
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Row 1 Tile 1 Pmt 1 Pixel 23 Slot 13 Fiber 0 Asic 0 Channel 41

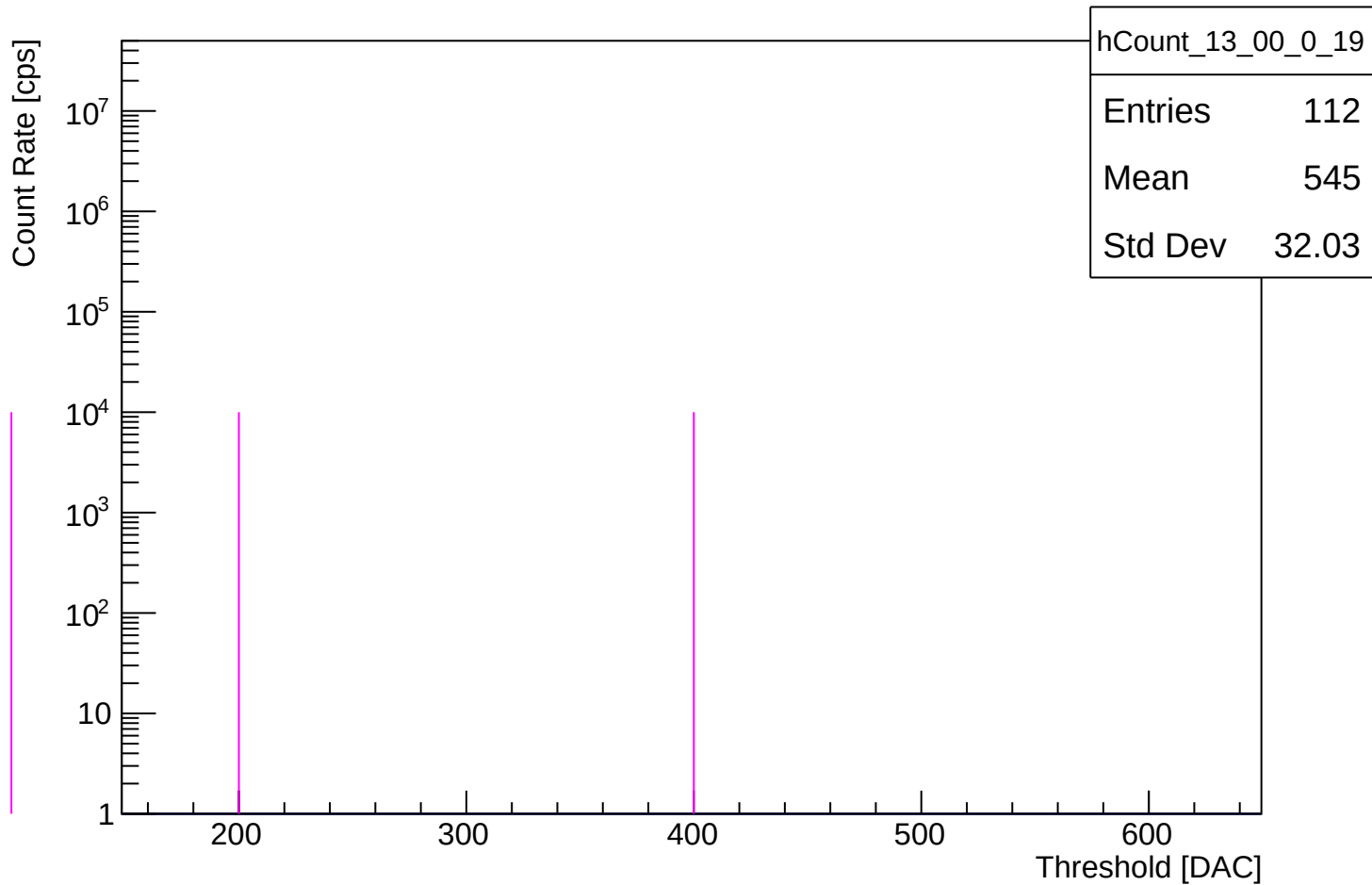


Row 1 Tile 1 Pmt 1 Pixel 24 Slot 13 Fiber 0 Asic 0 Channel 43

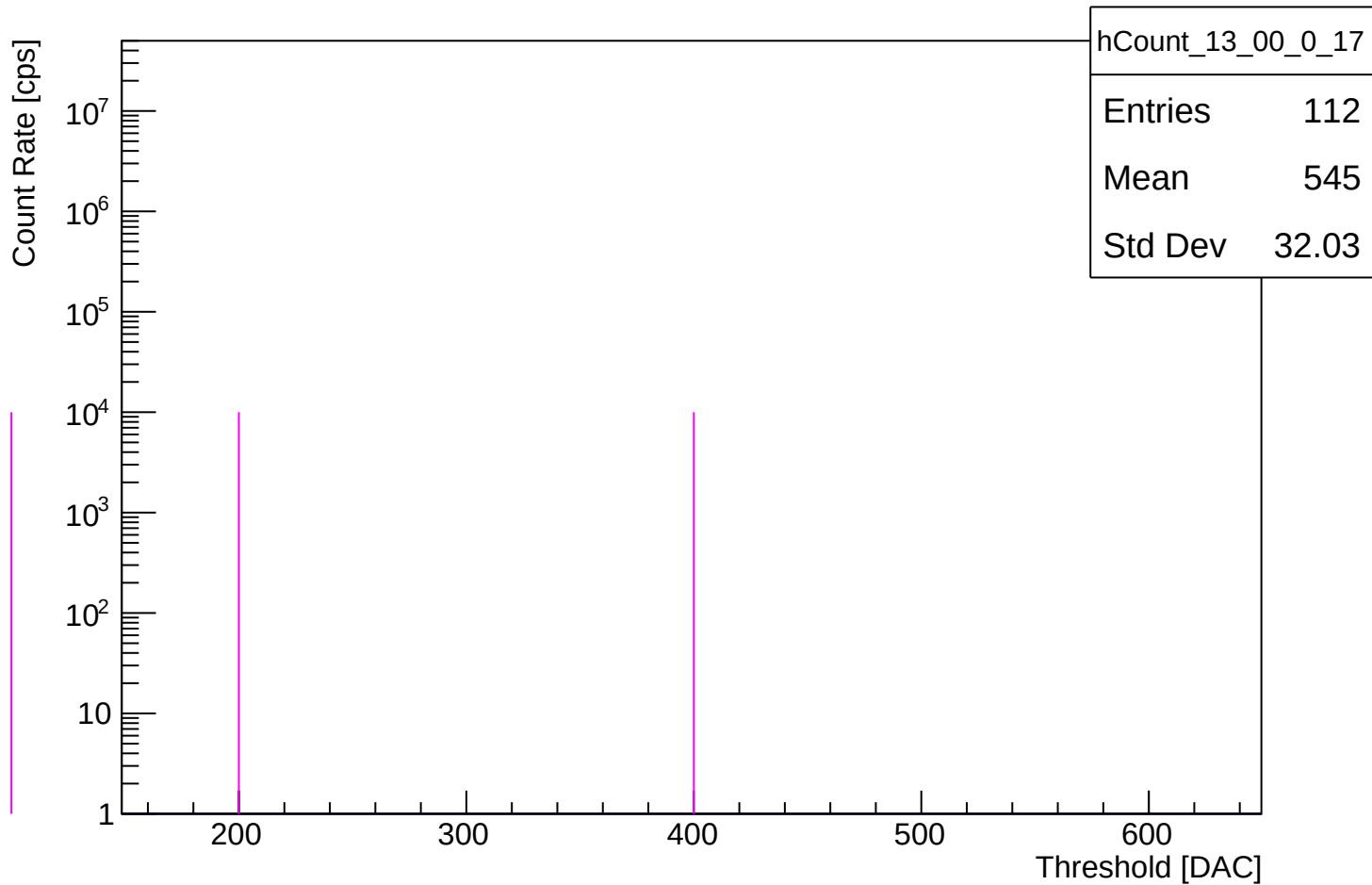




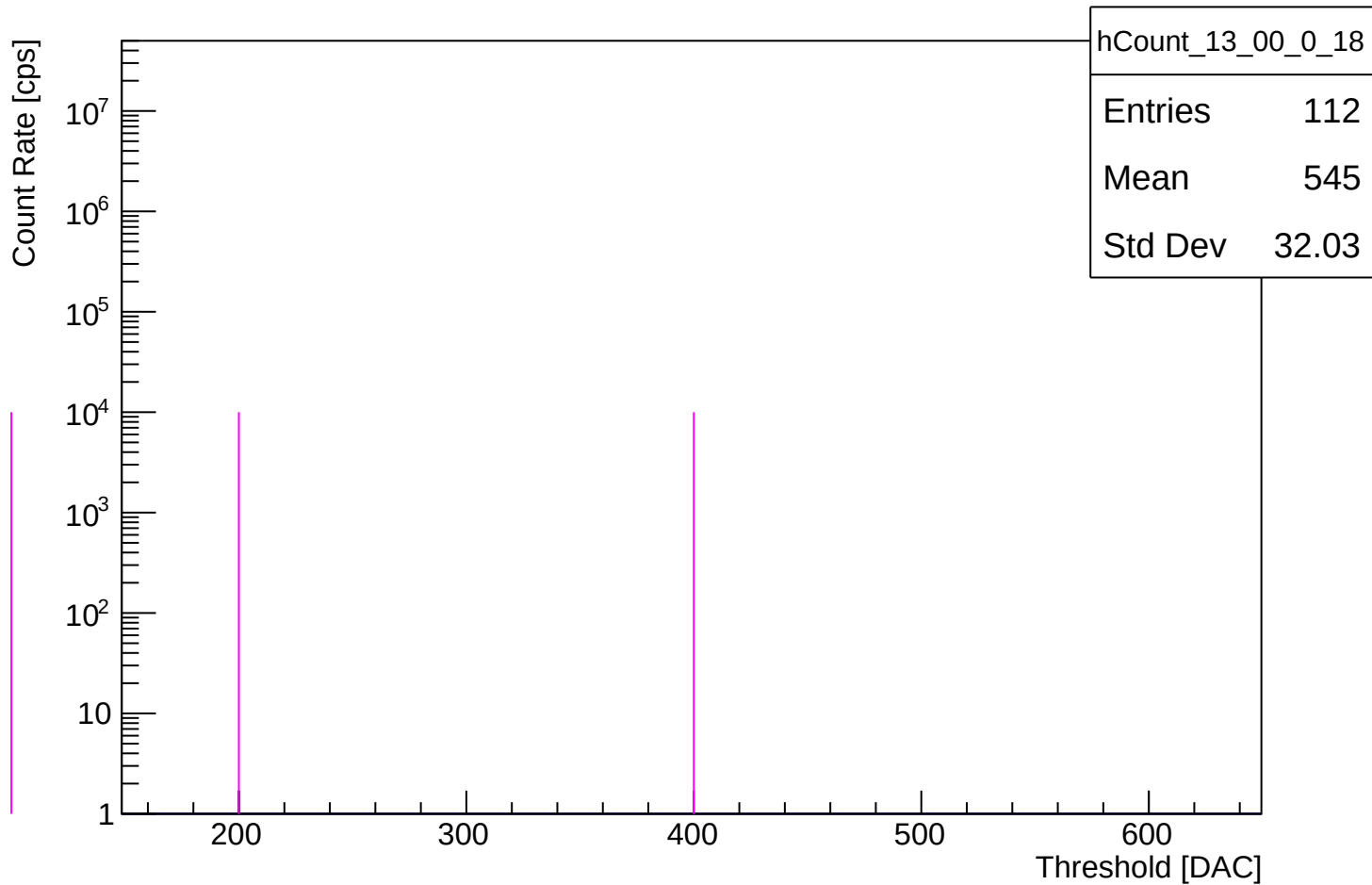
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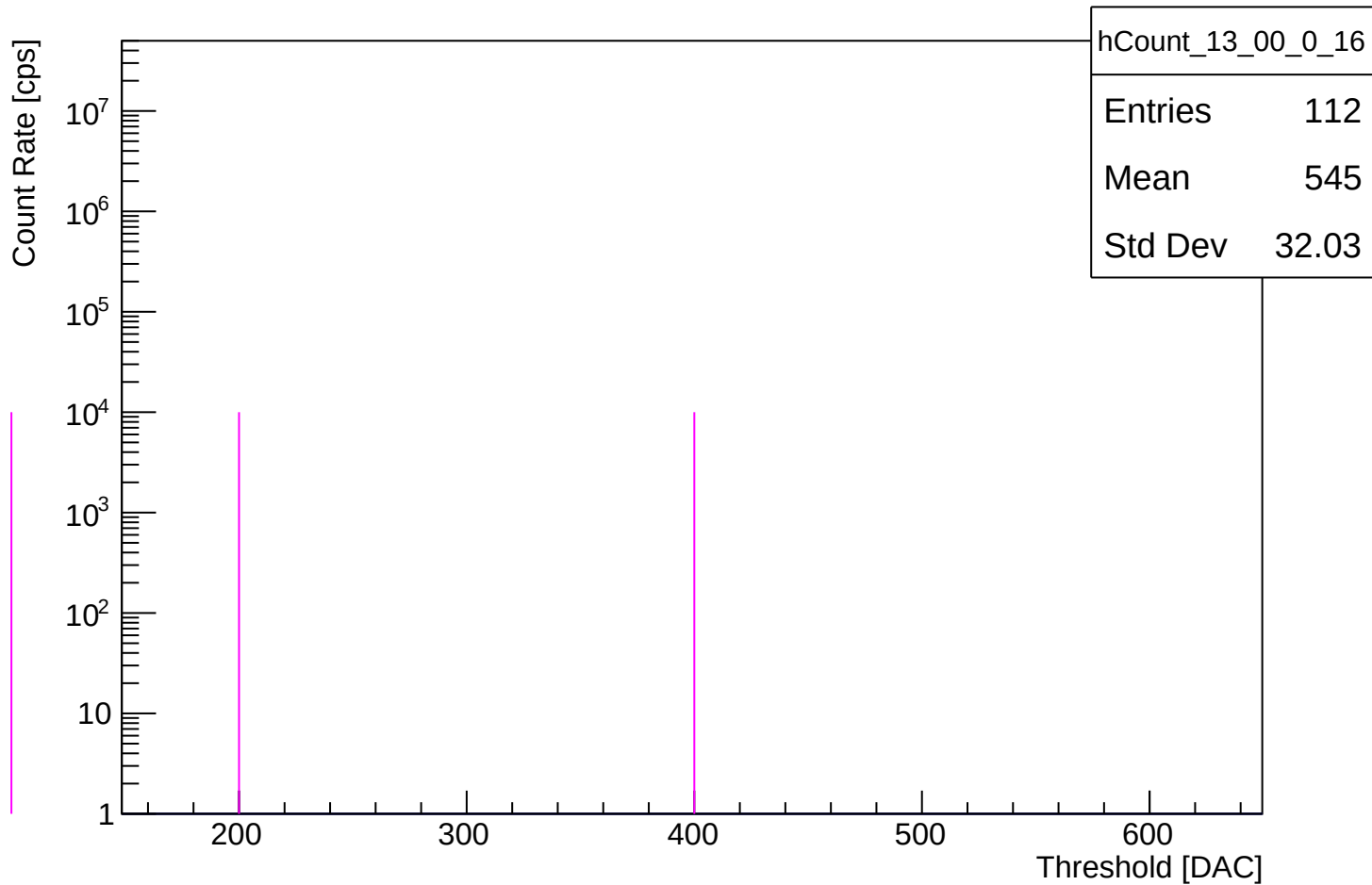
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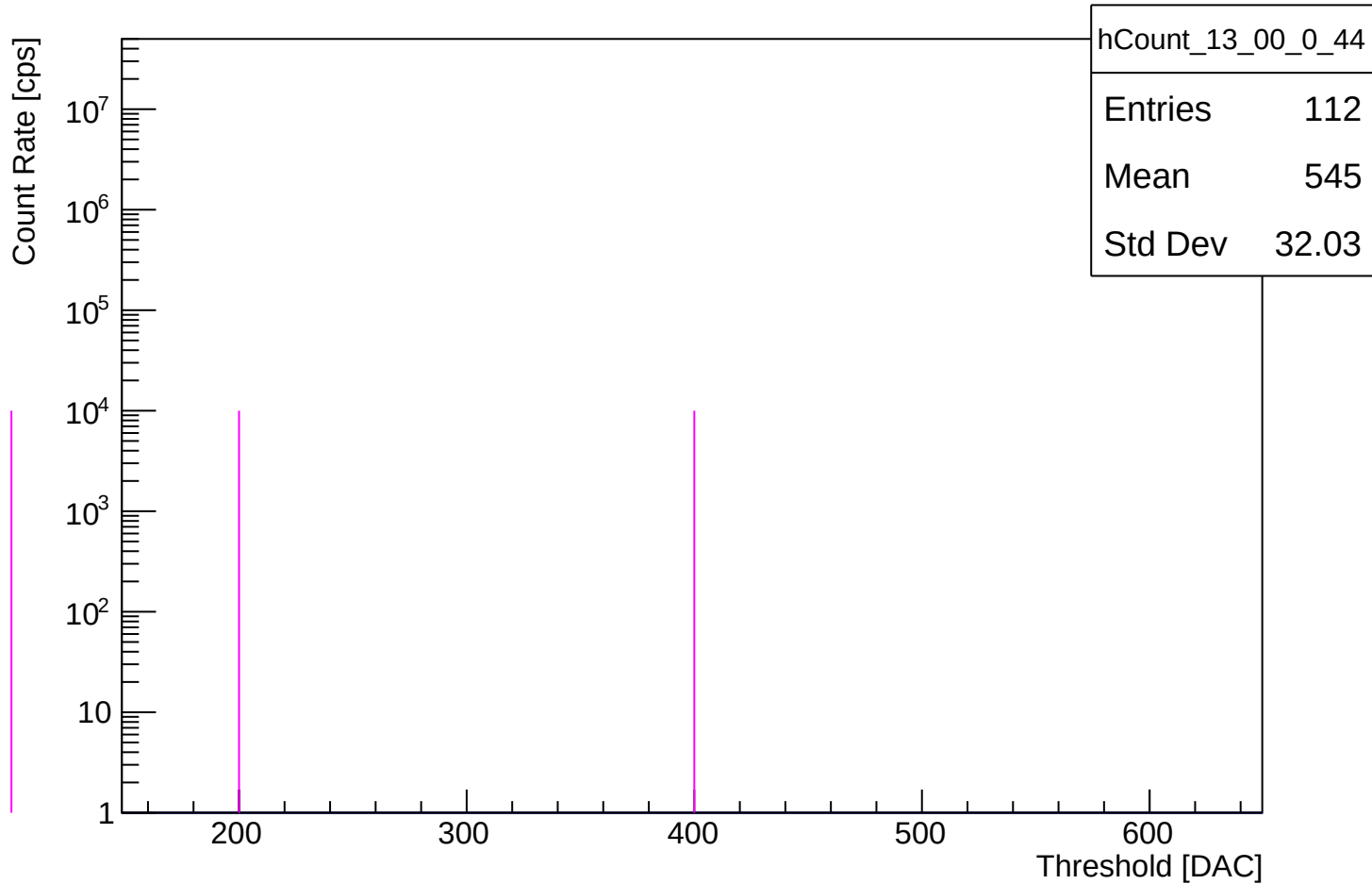
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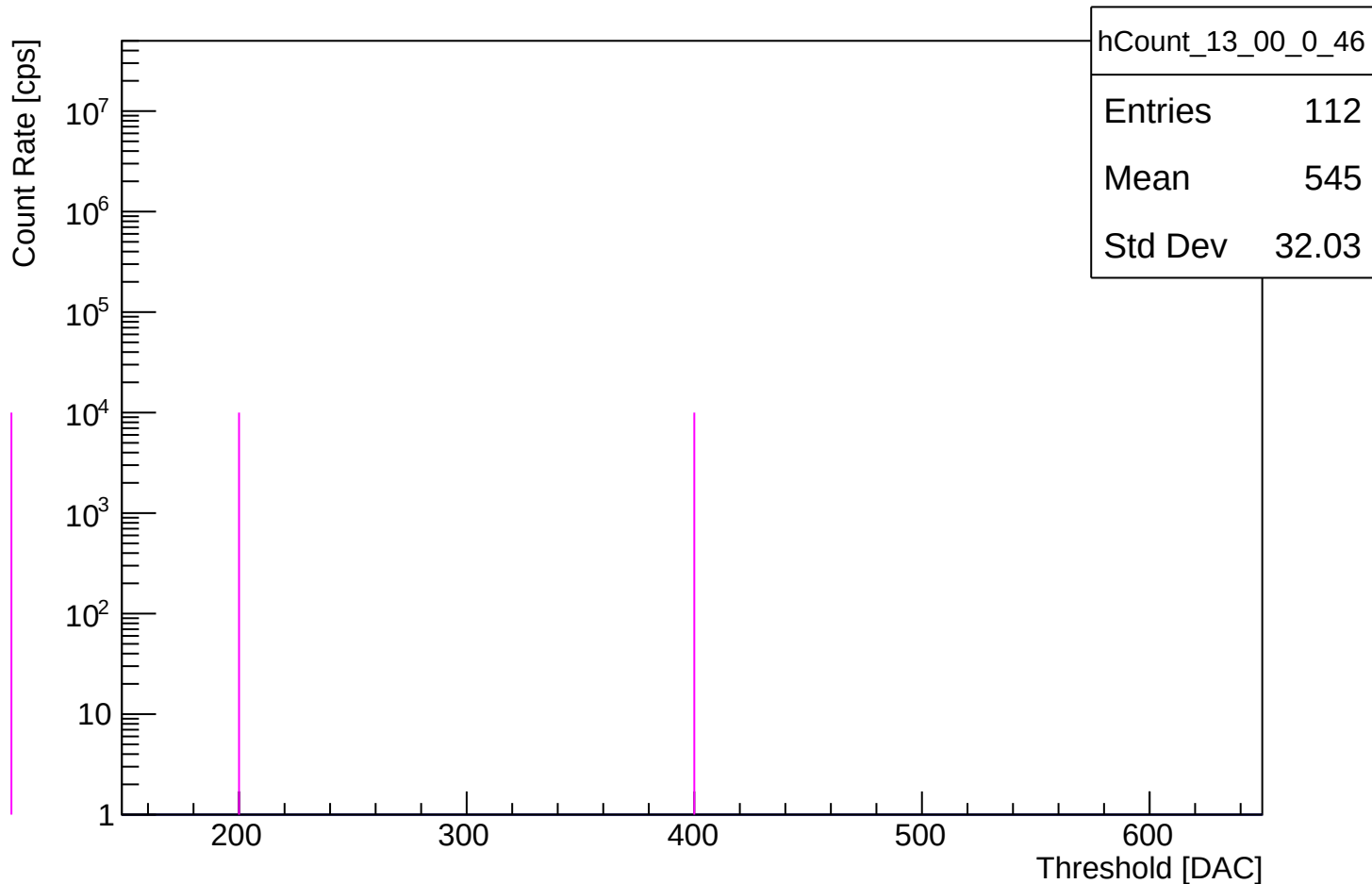
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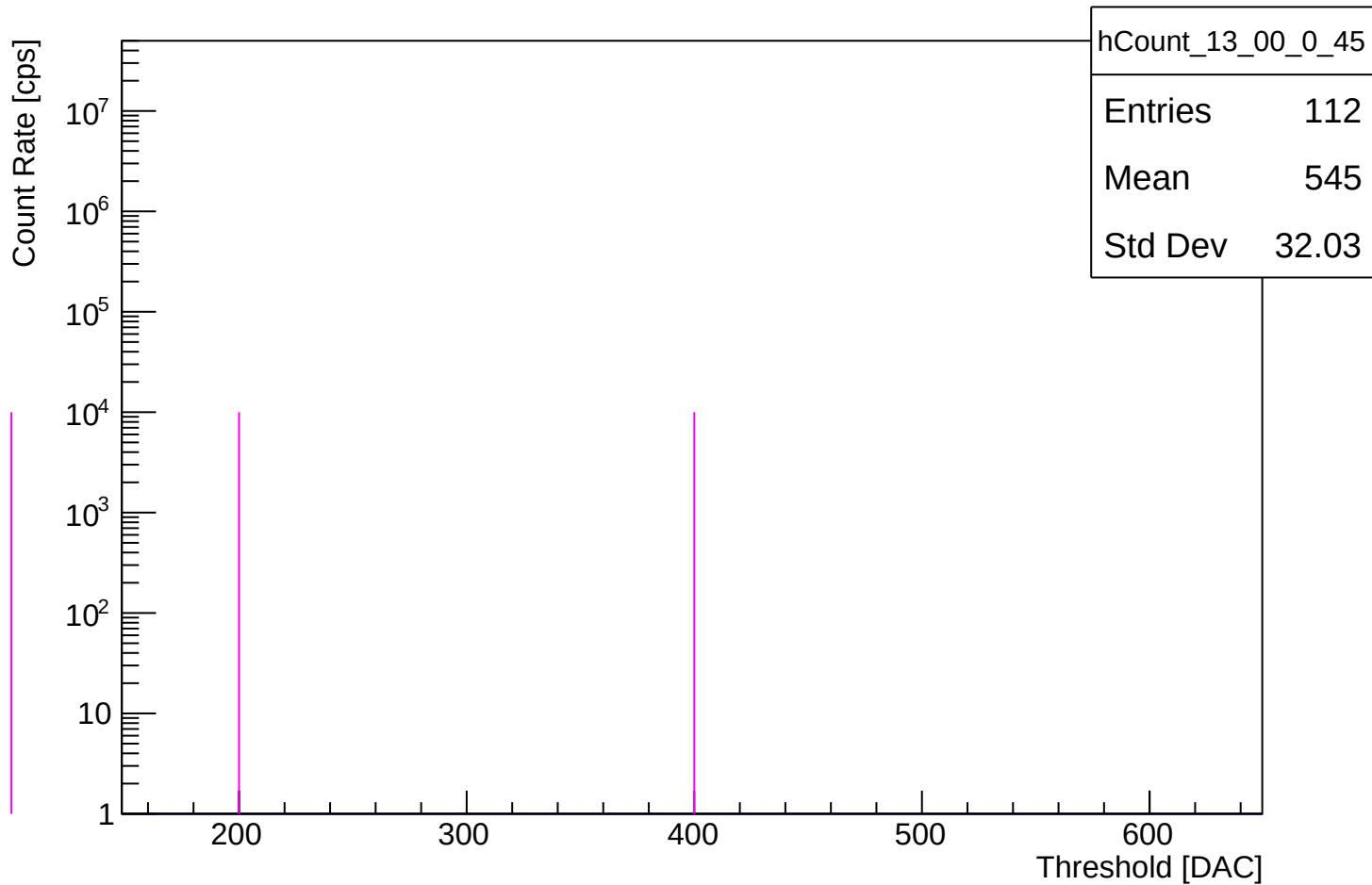
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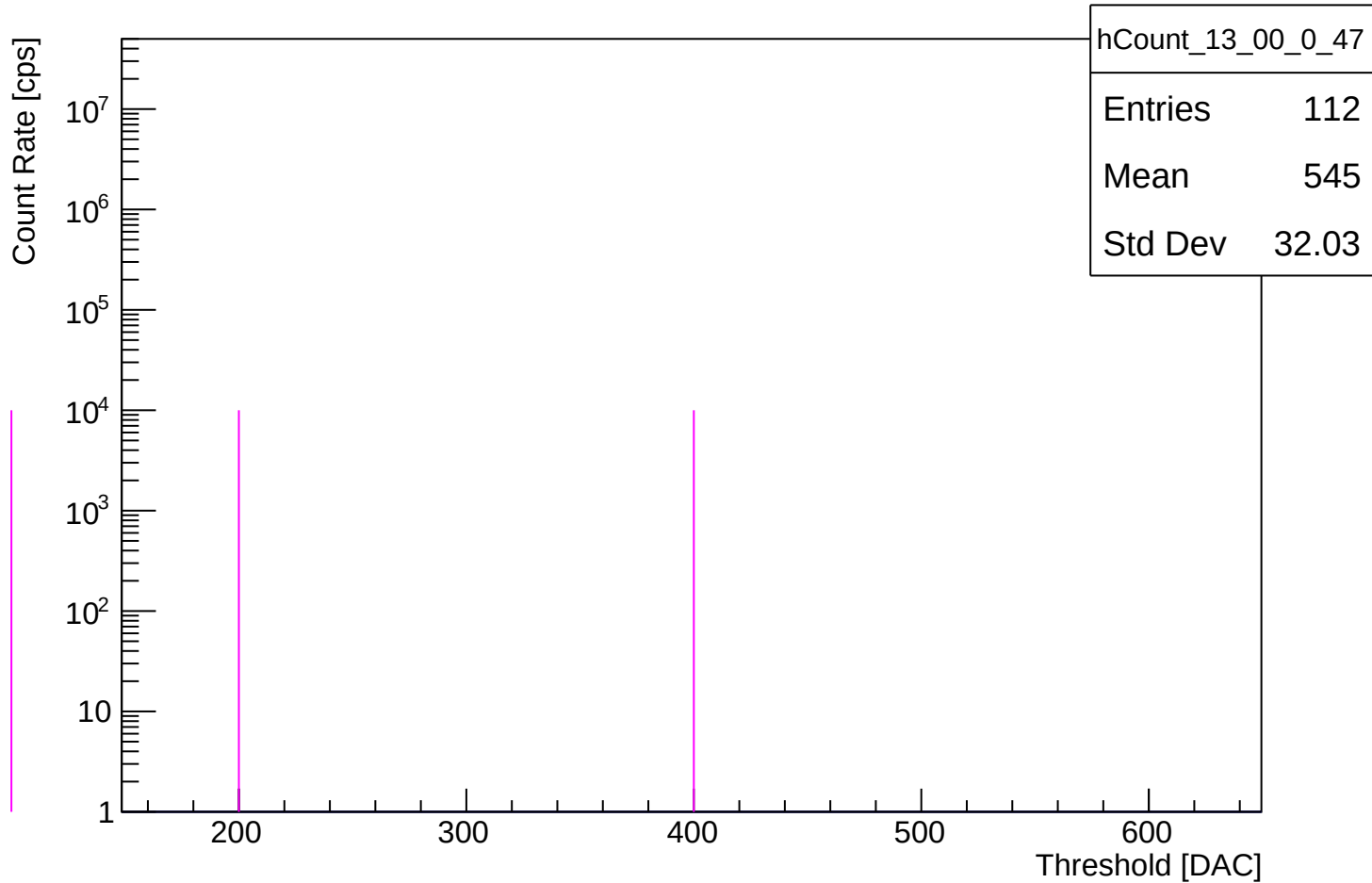
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Row 1 Tile 1 Pmt 1 Pixel 31 Slot 13 Fiber 0 Asic 0 Channel 45

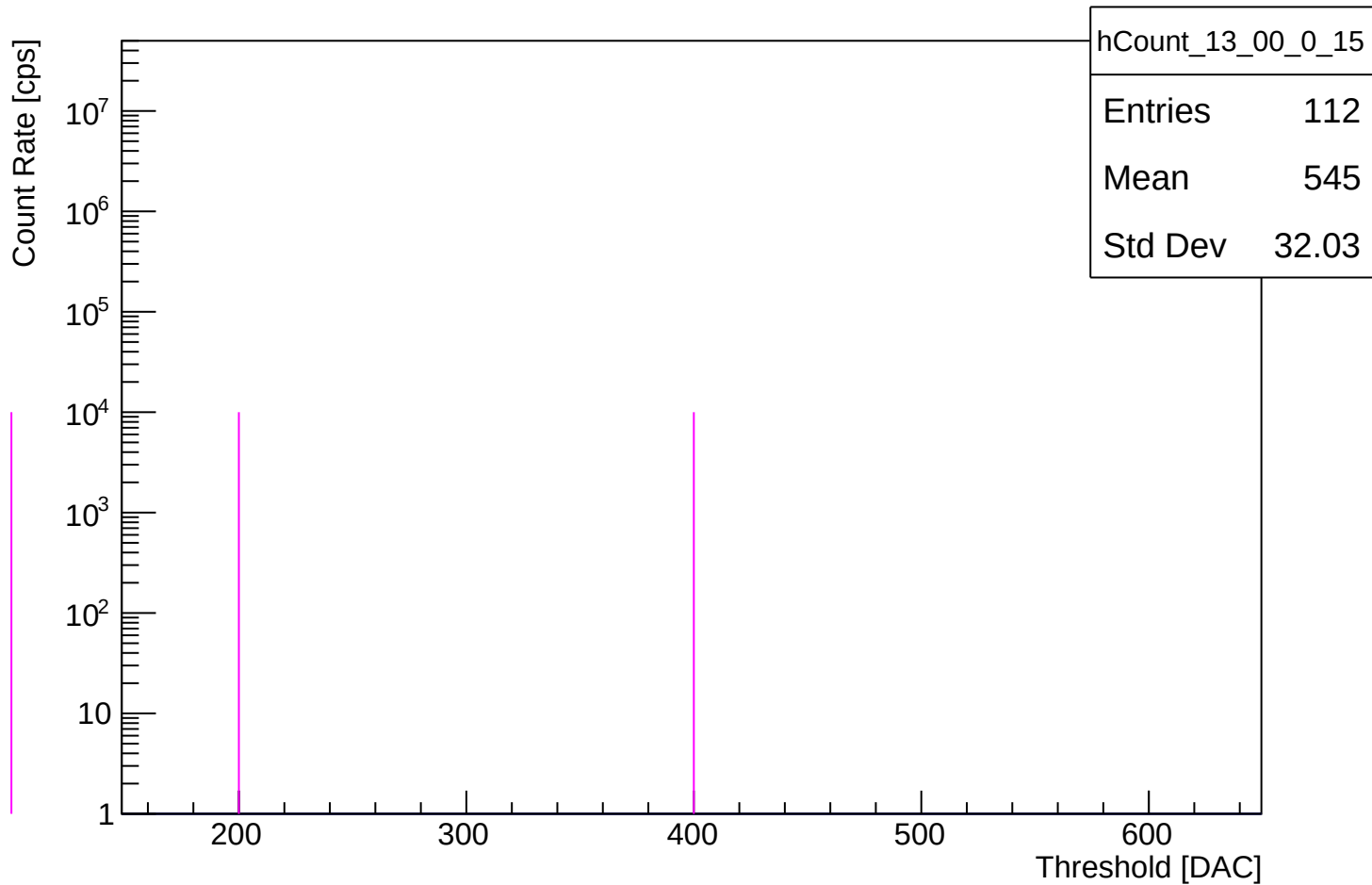


Row 1 Tile 1 Pmt 1 Pixel 32 Slot 13 Fiber 0 Asic 0 Channel 47

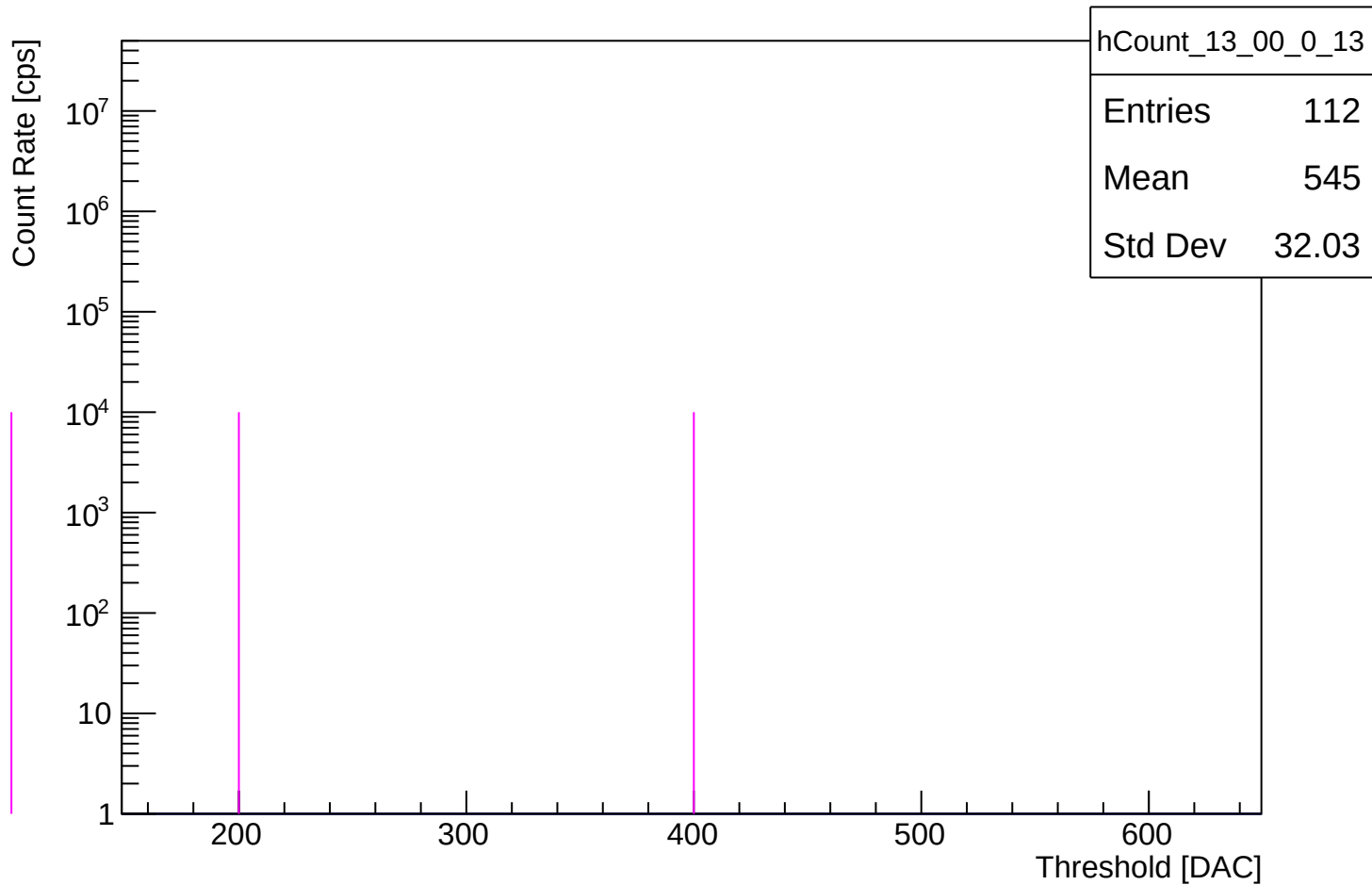




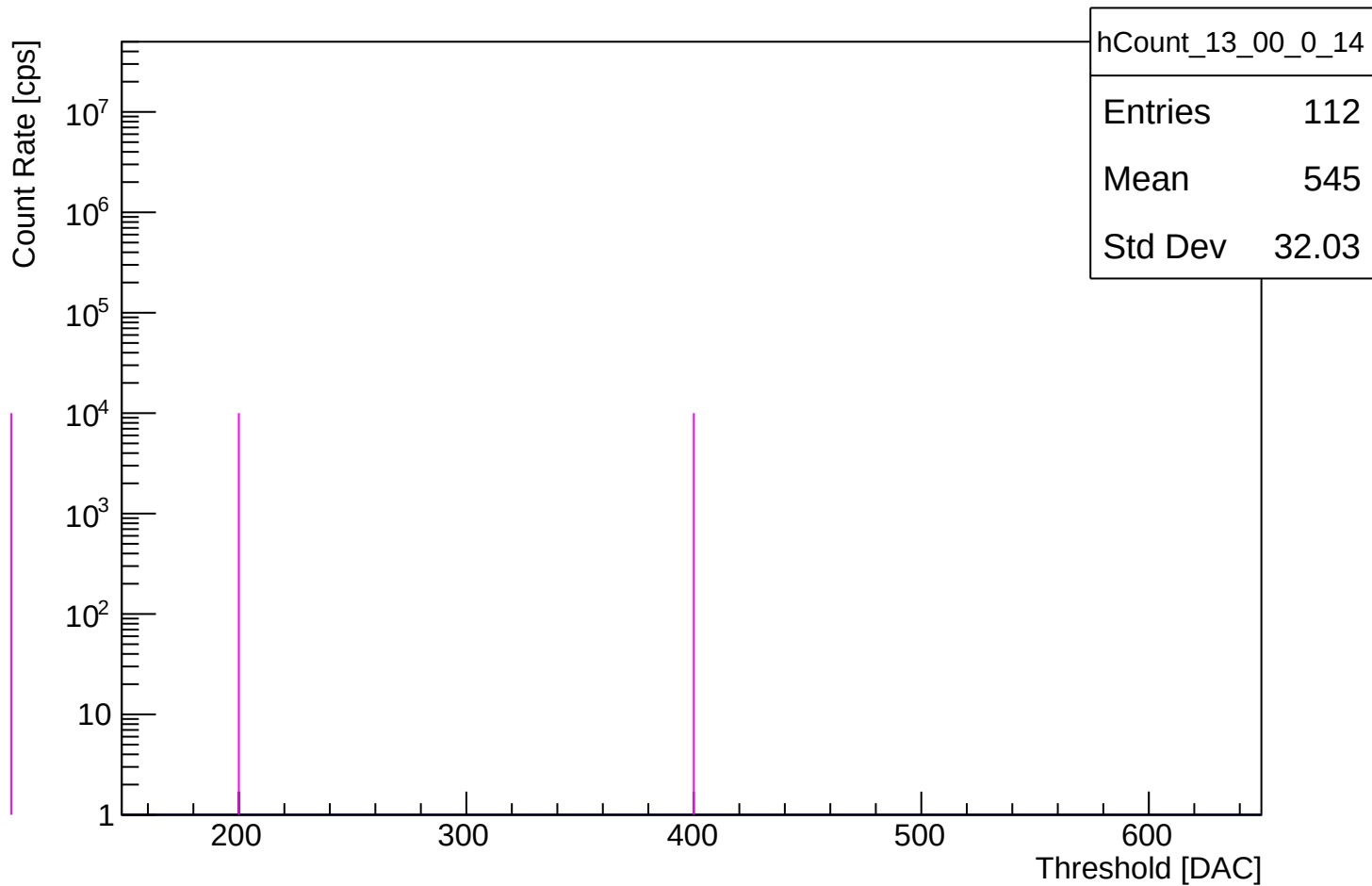
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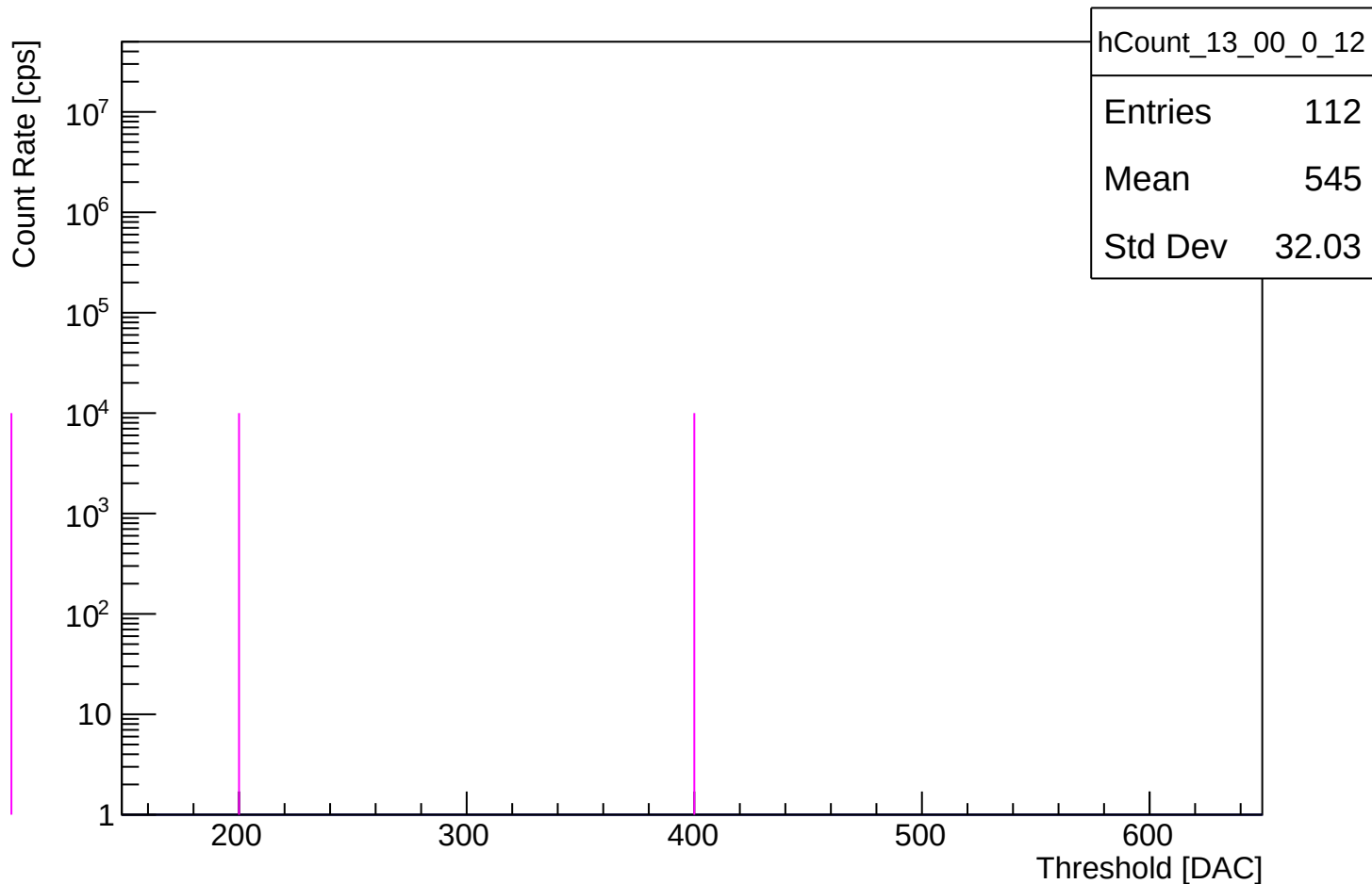
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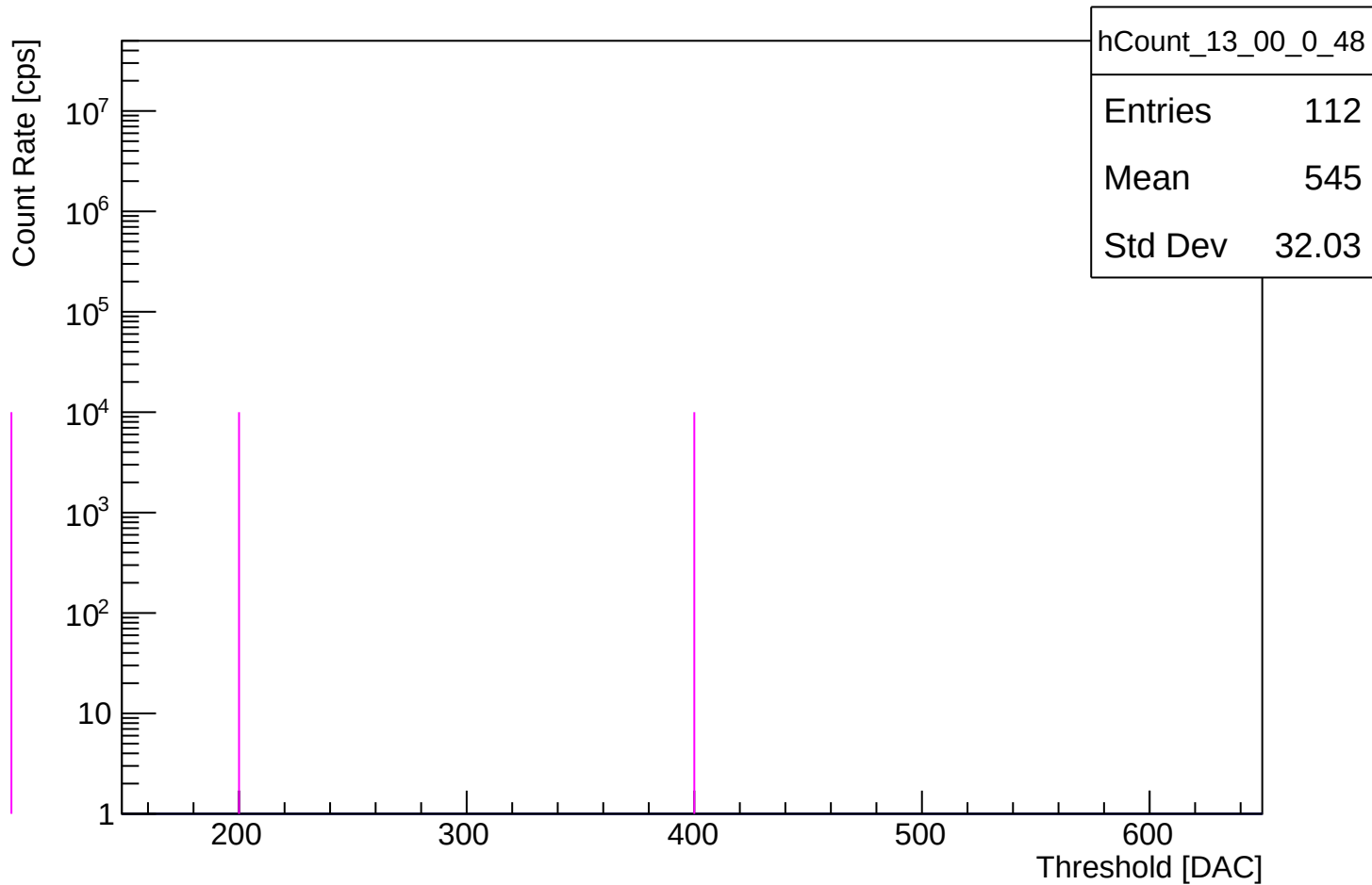
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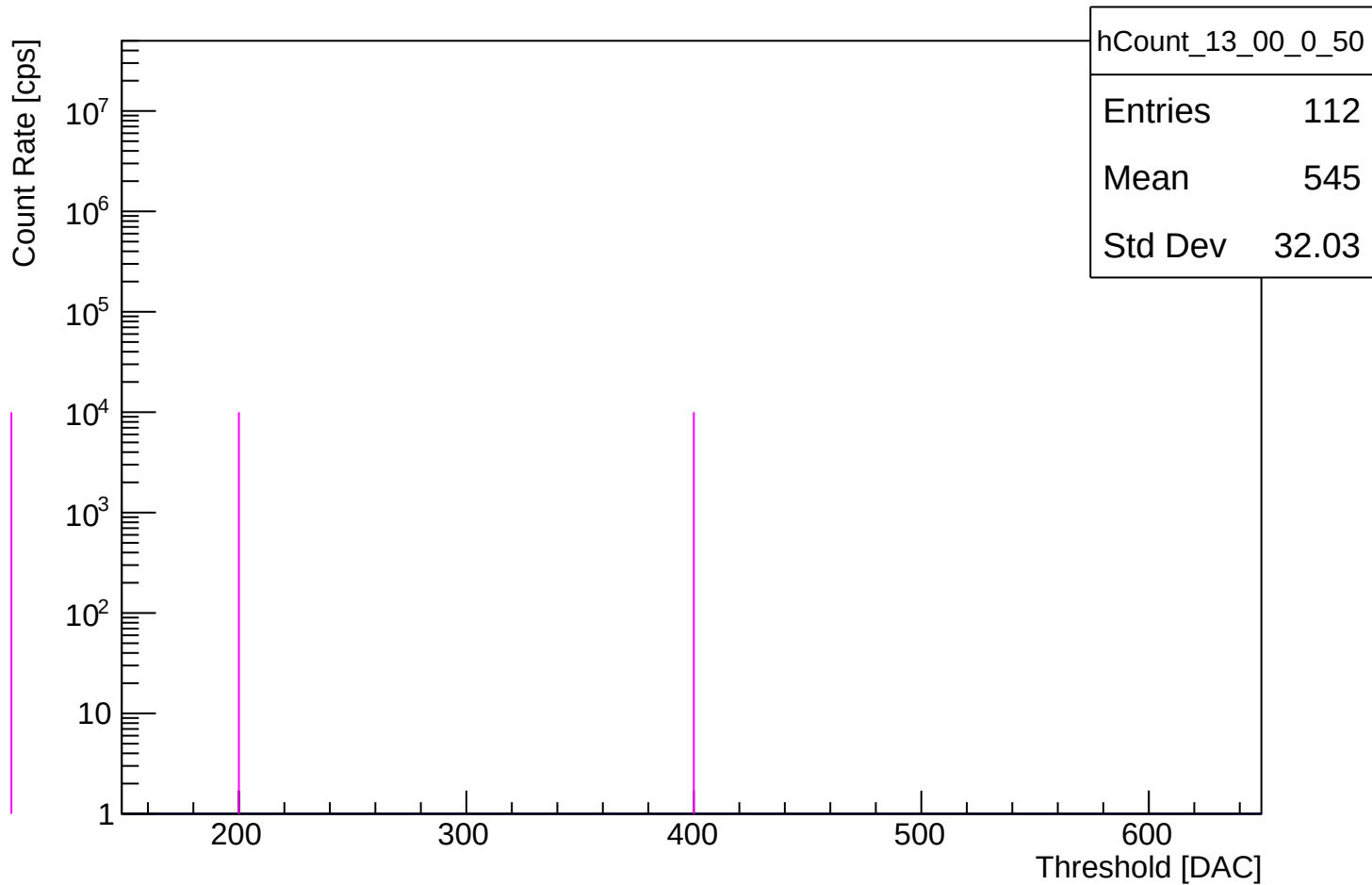
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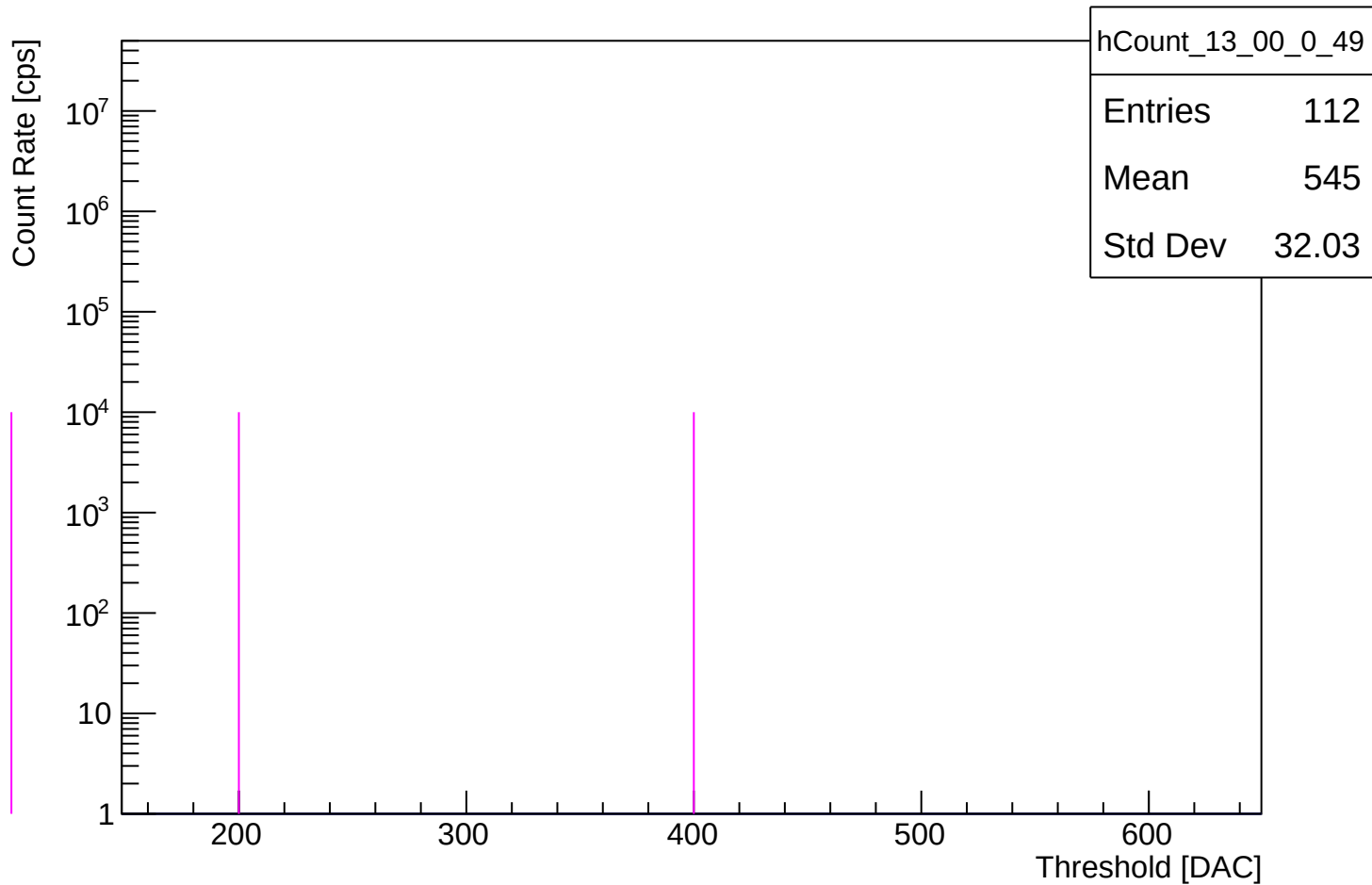
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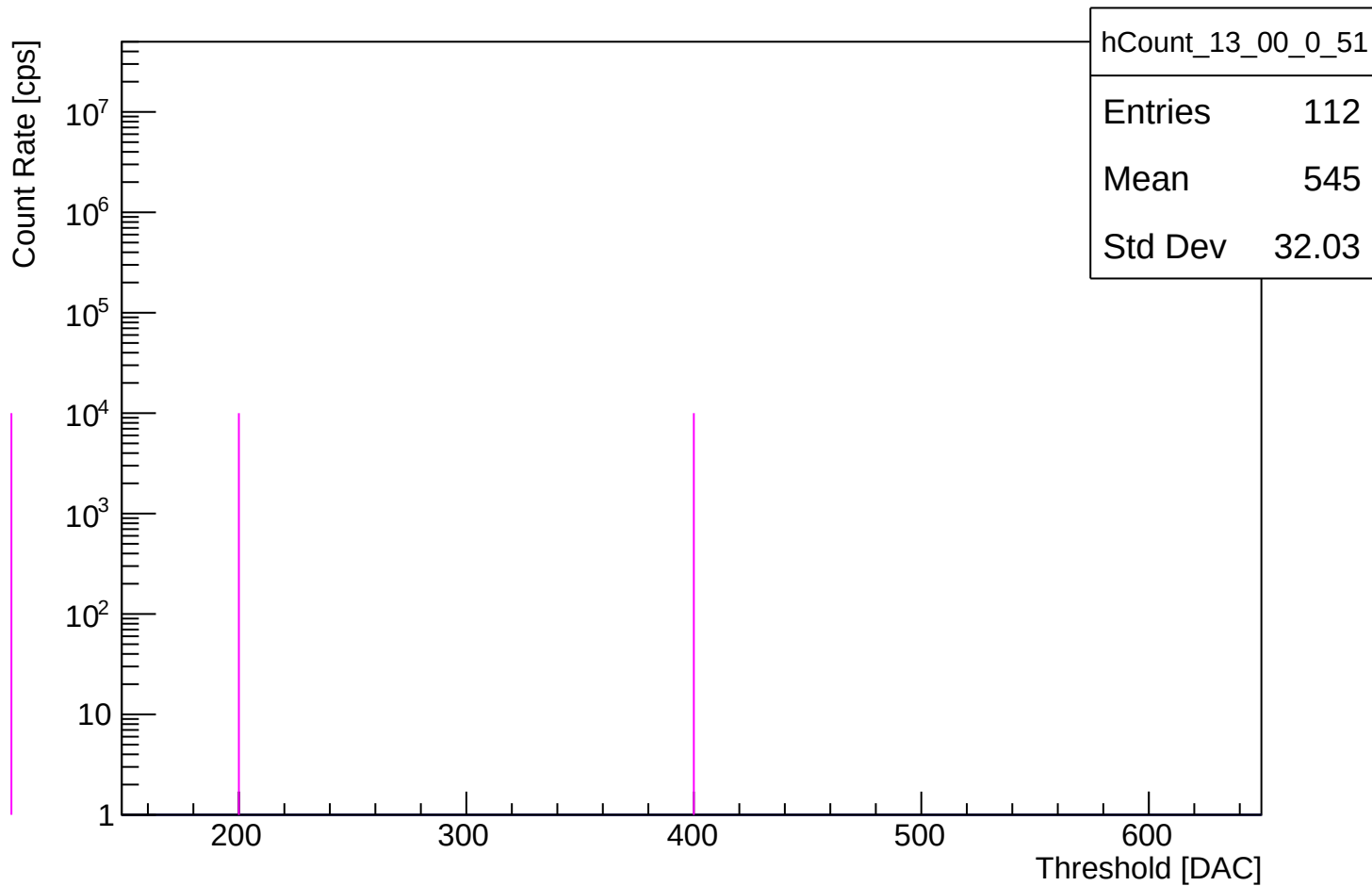
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Row 1 Tile 1 Pmt 1 Pixel 39 Slot 13 Fiber 0 Asic 0 Channel 49

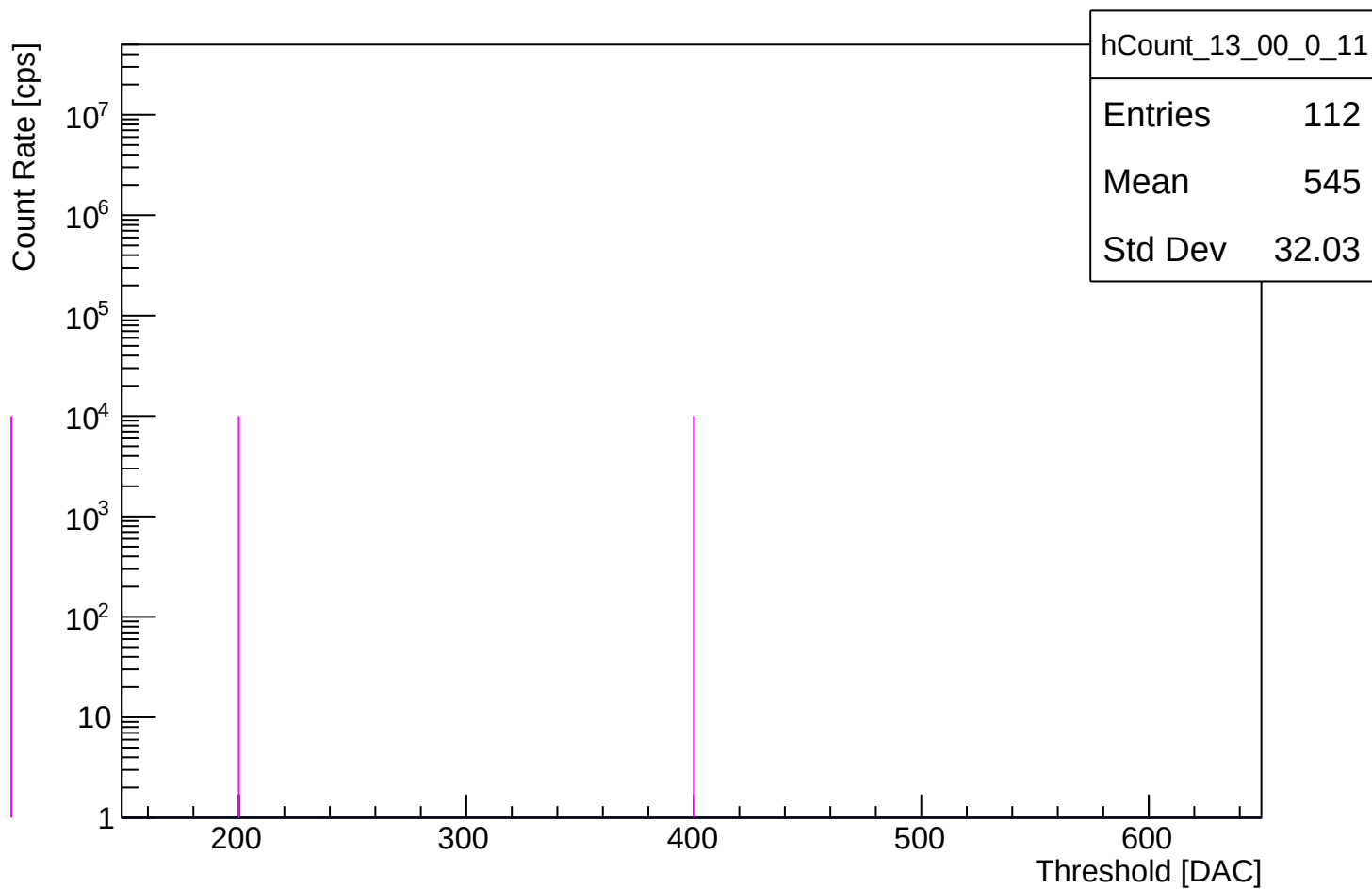


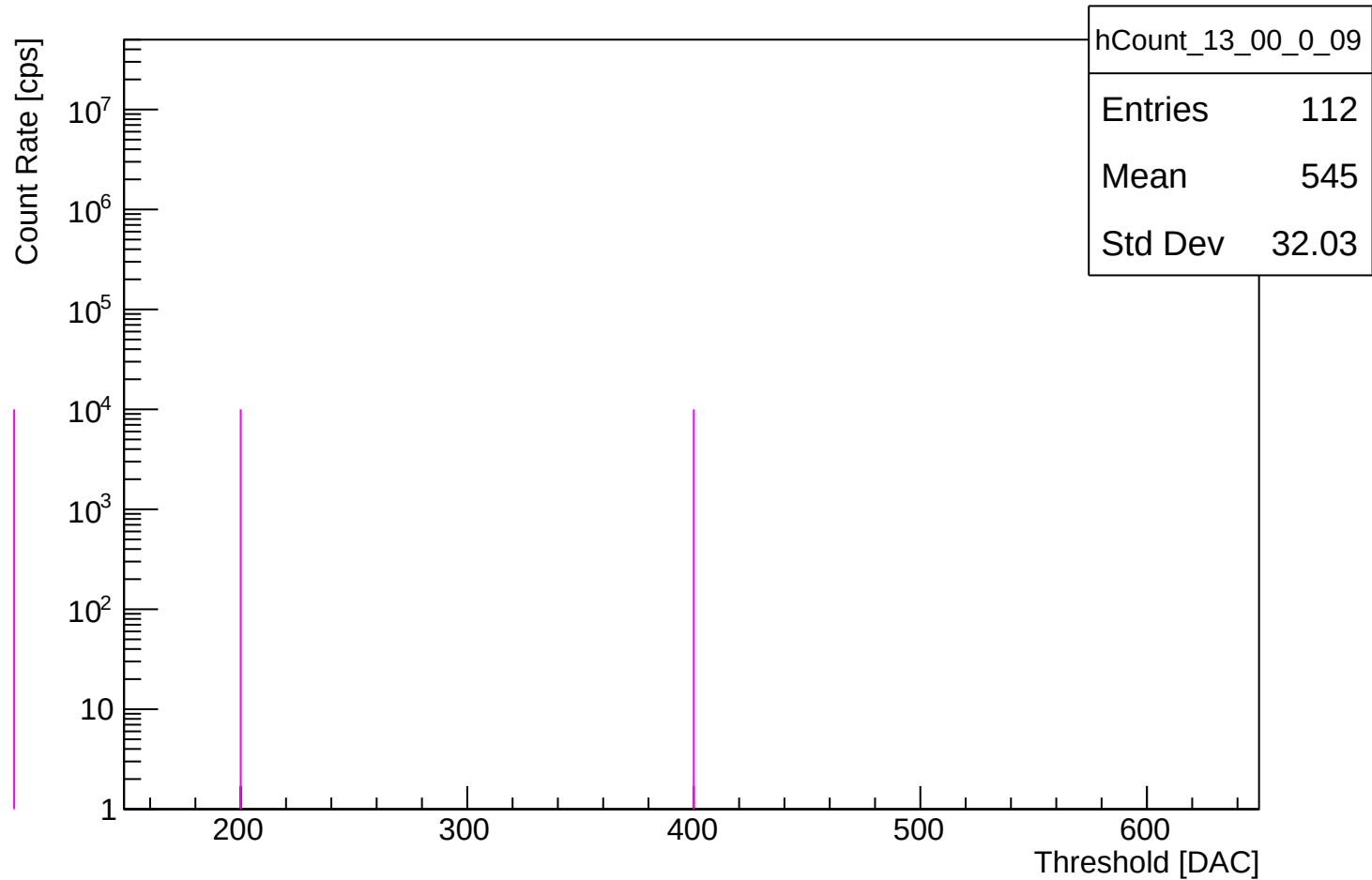
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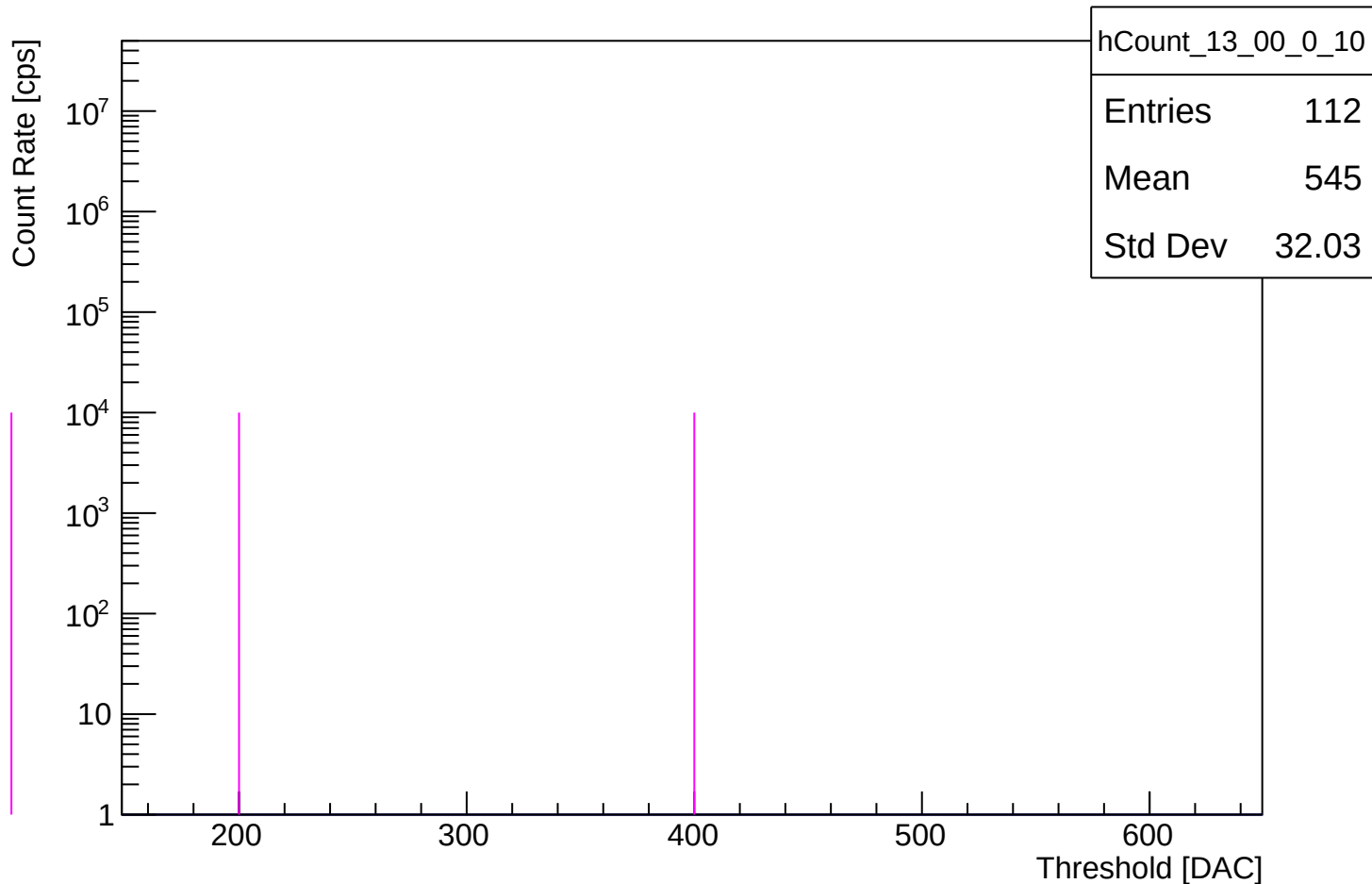


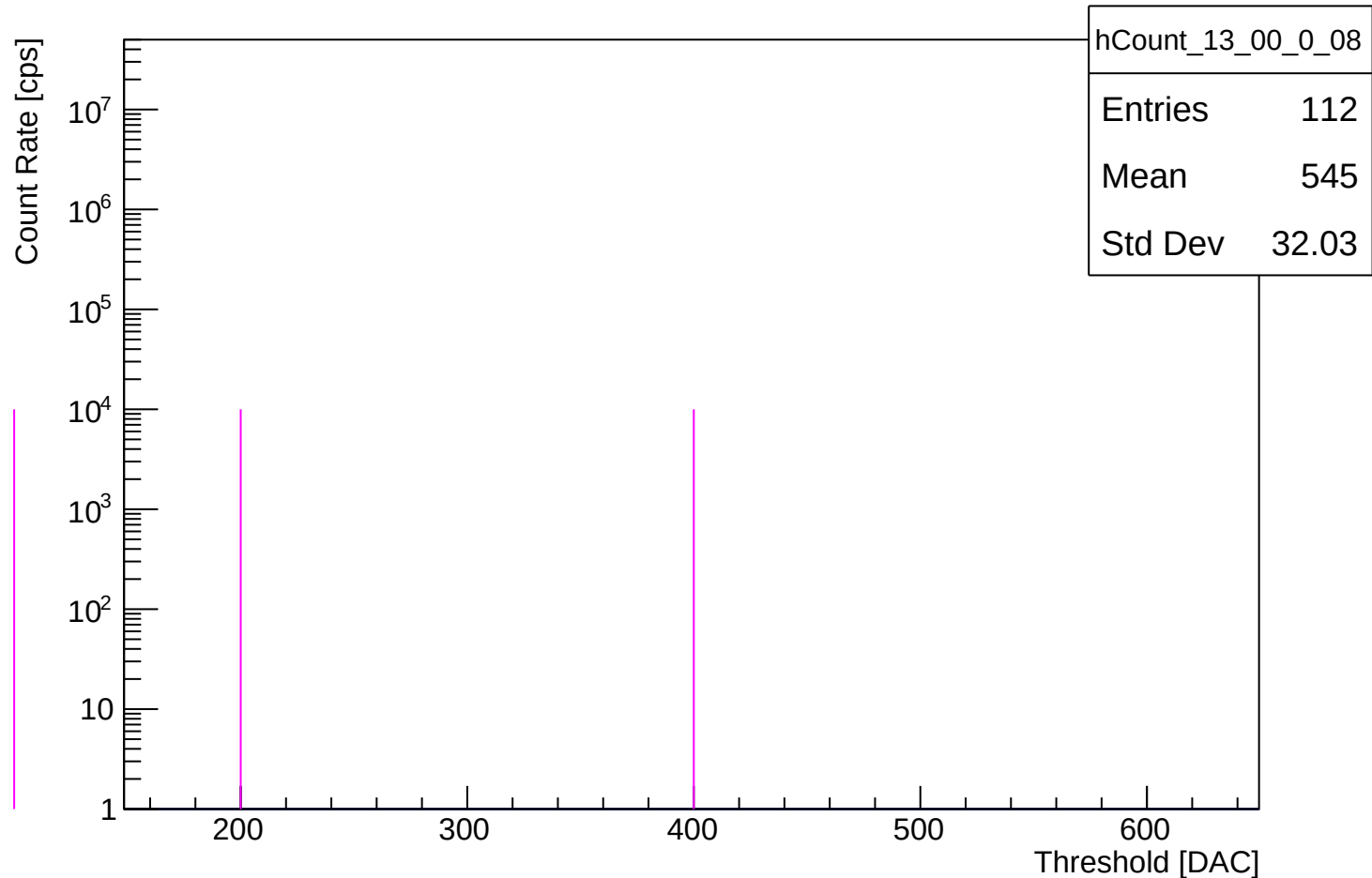
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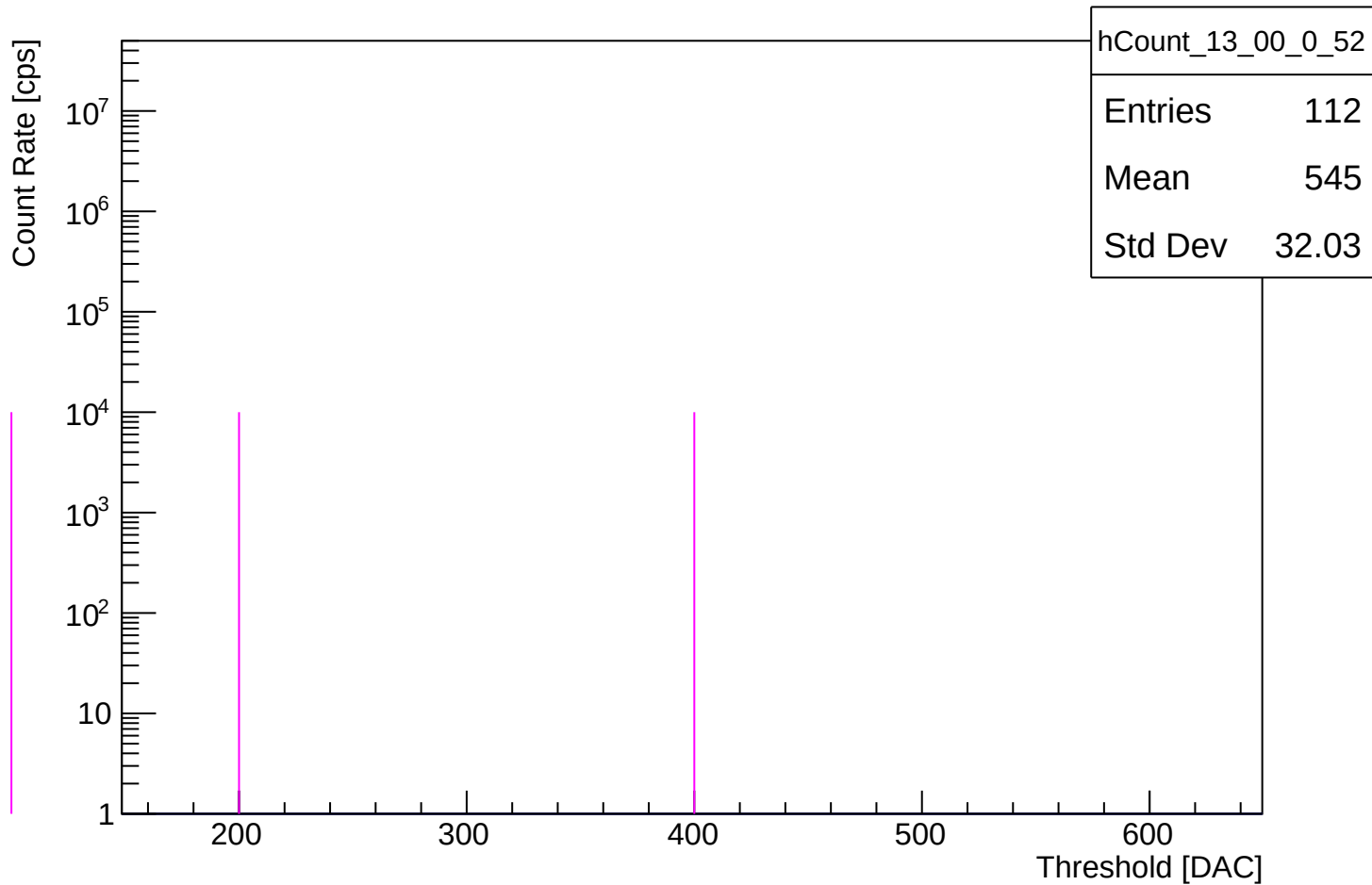


Row 1 Tile 1 Pmt 1 Pixel 43 Slot 13 Fiber 0 Asic 0 Channel 10

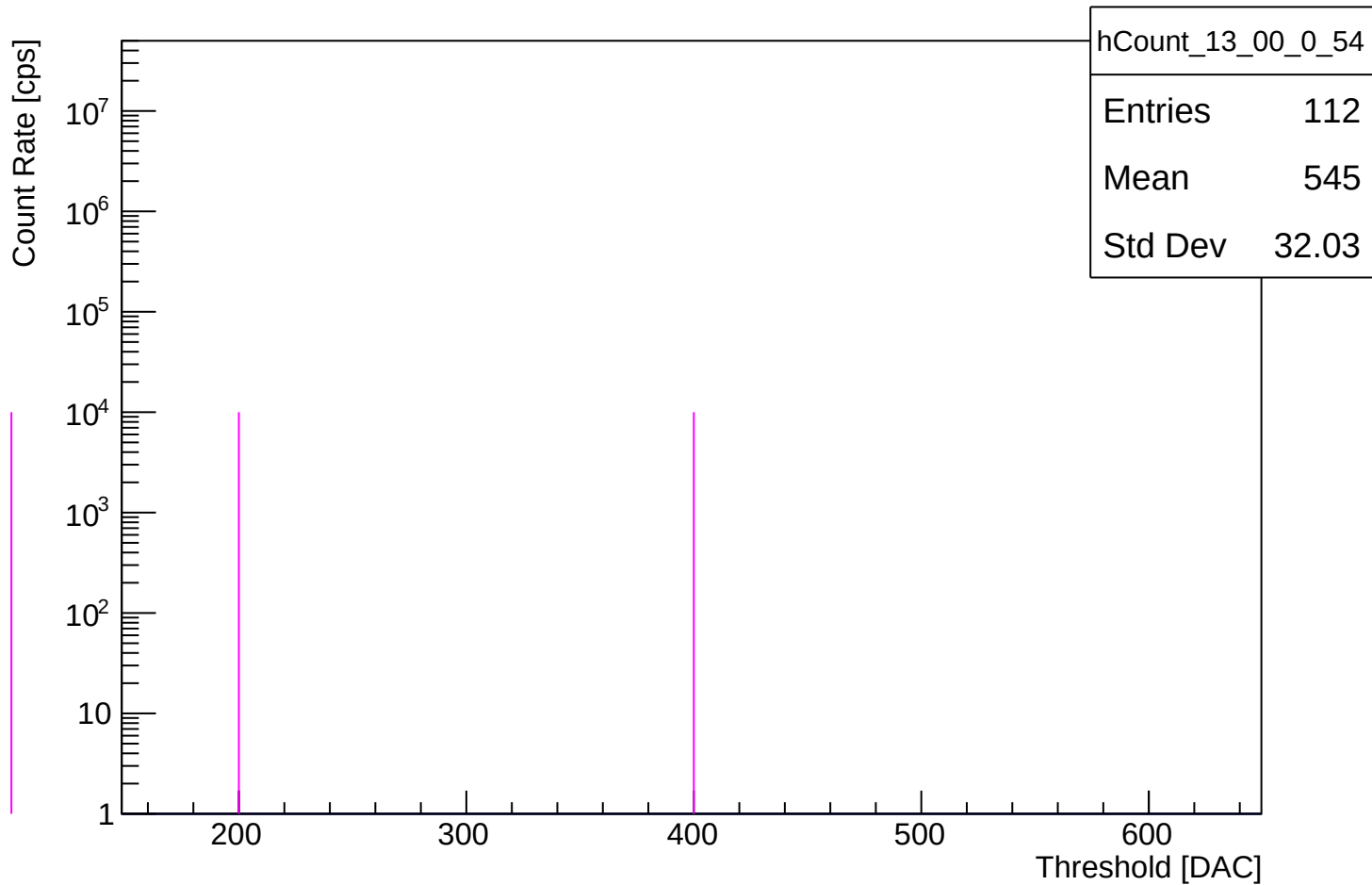




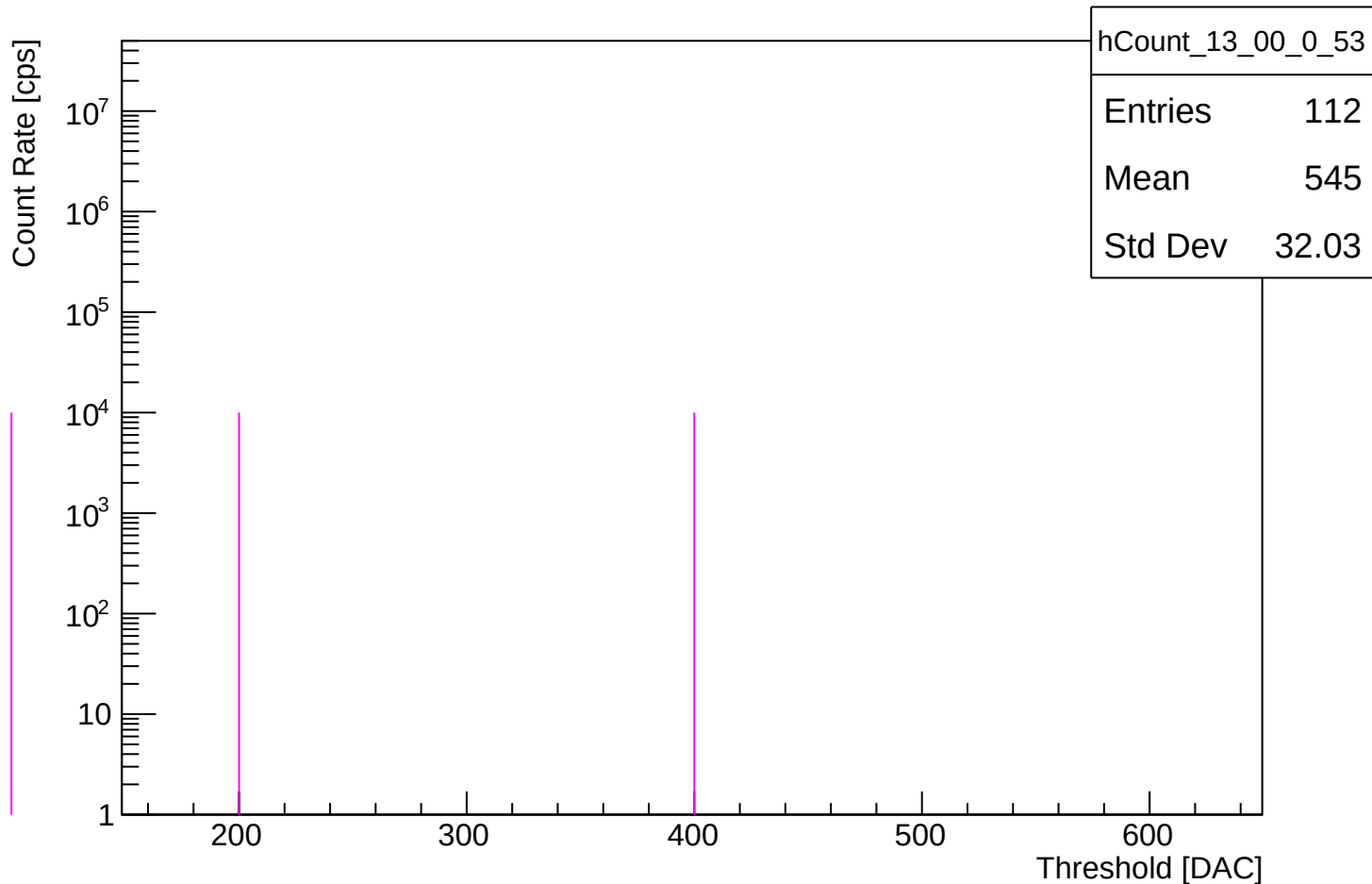
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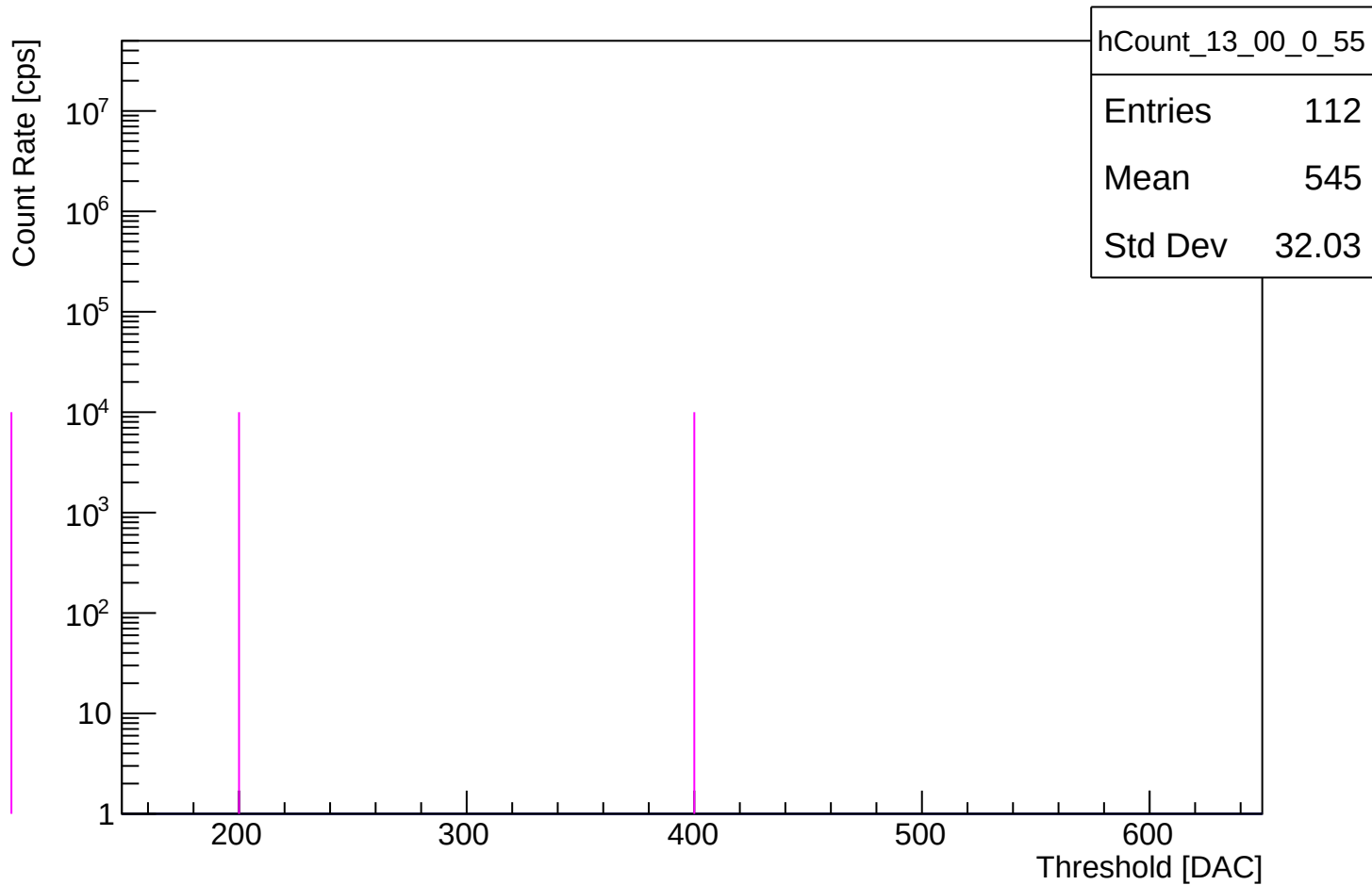
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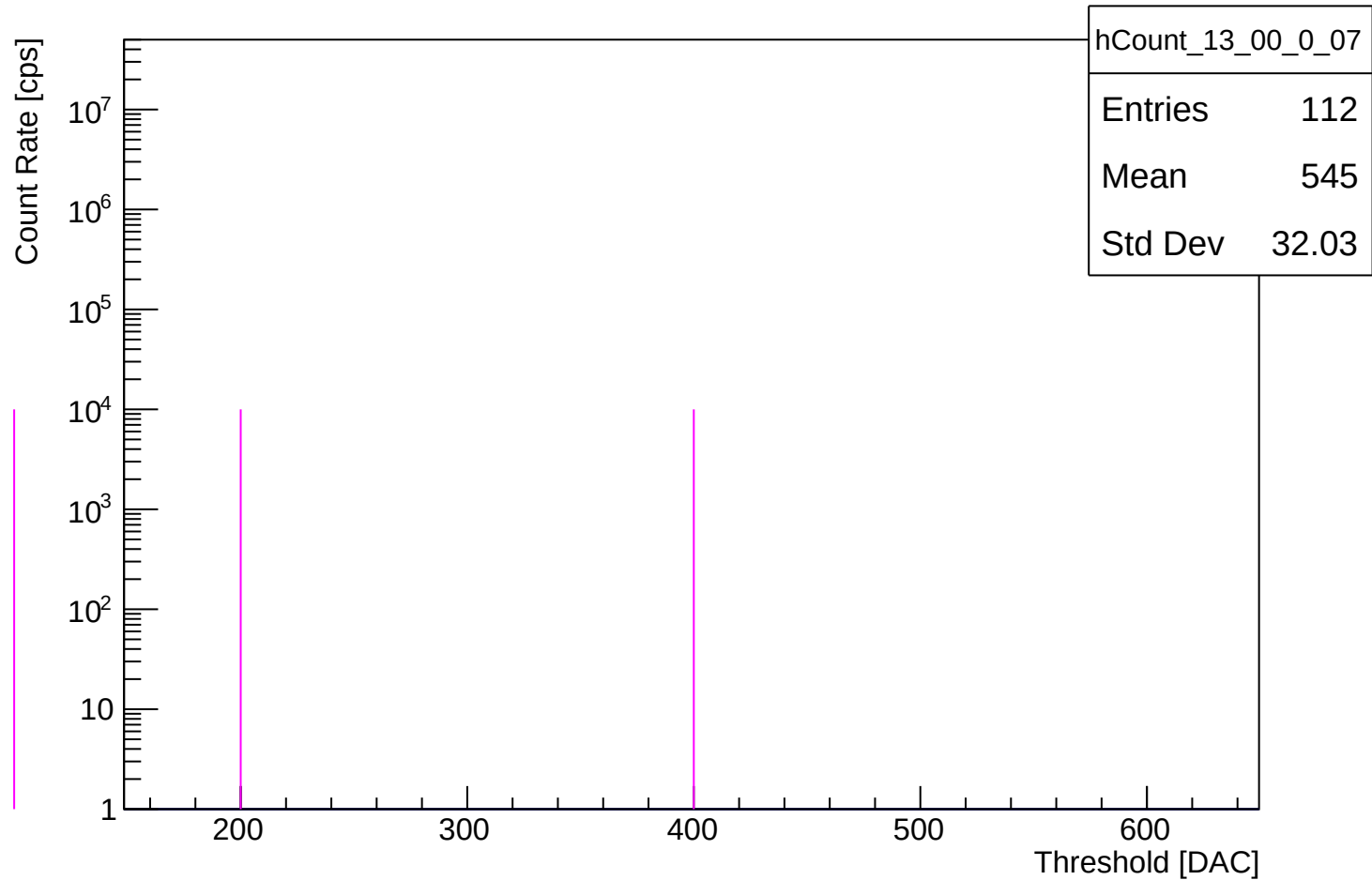
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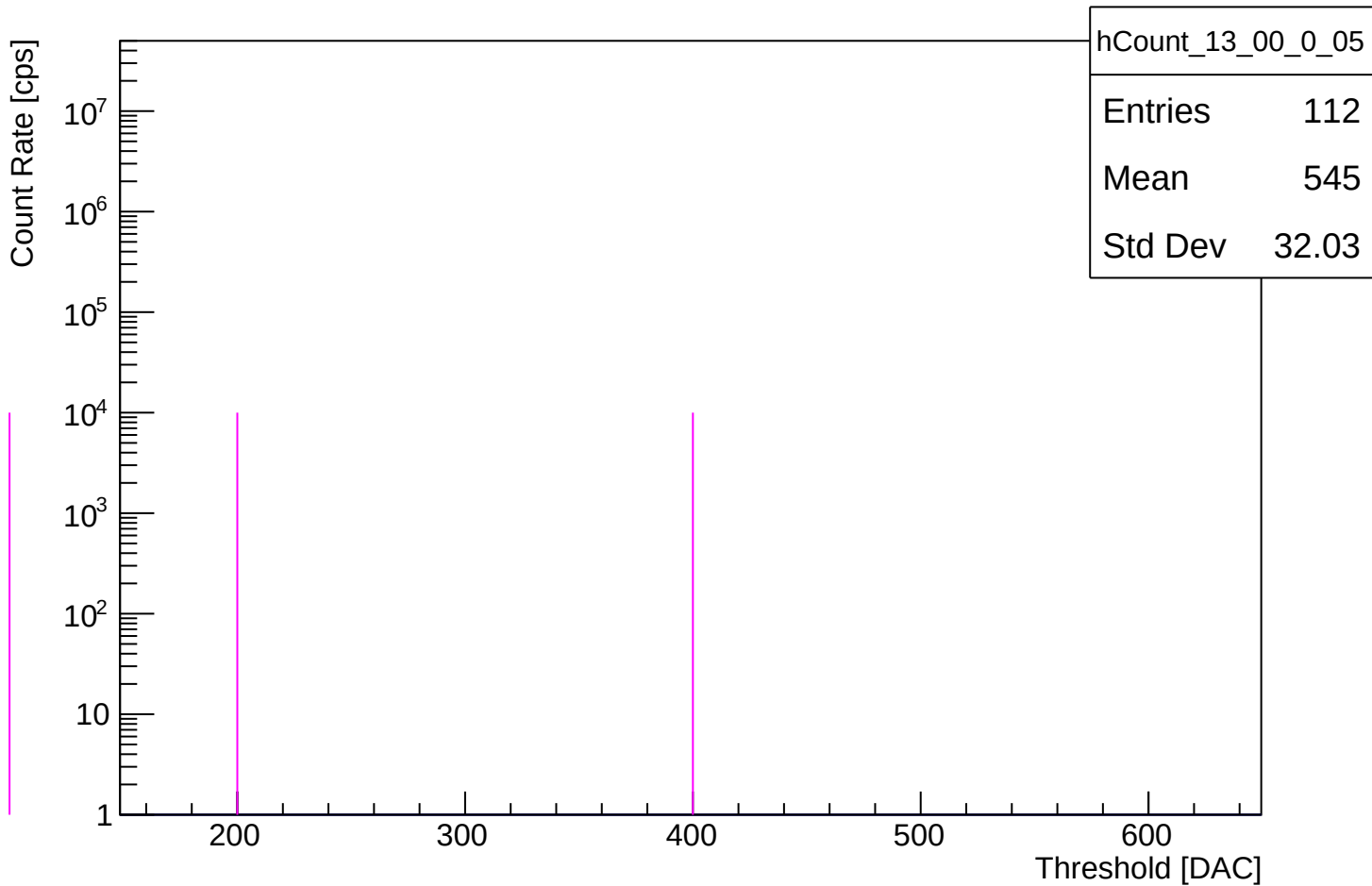
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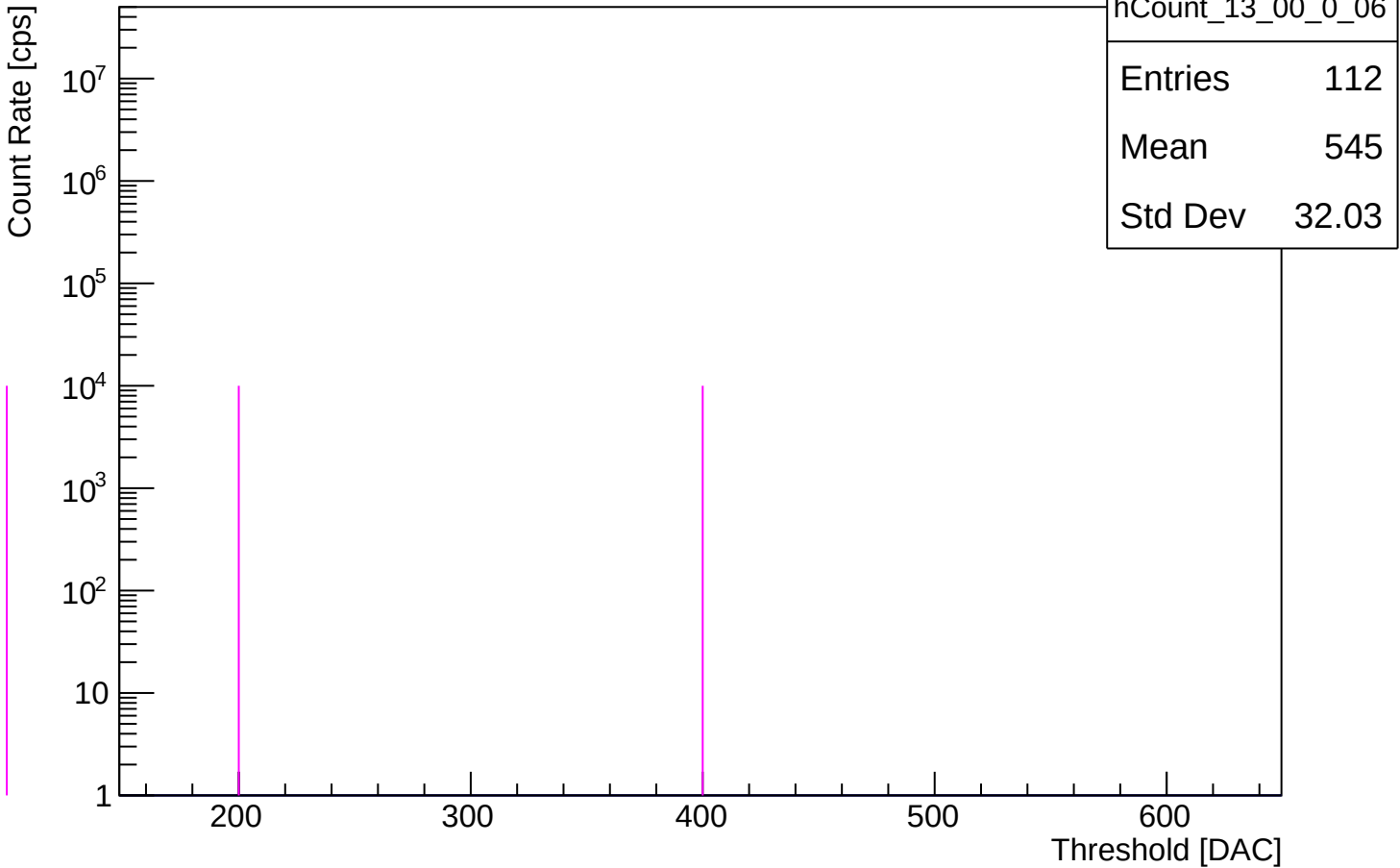


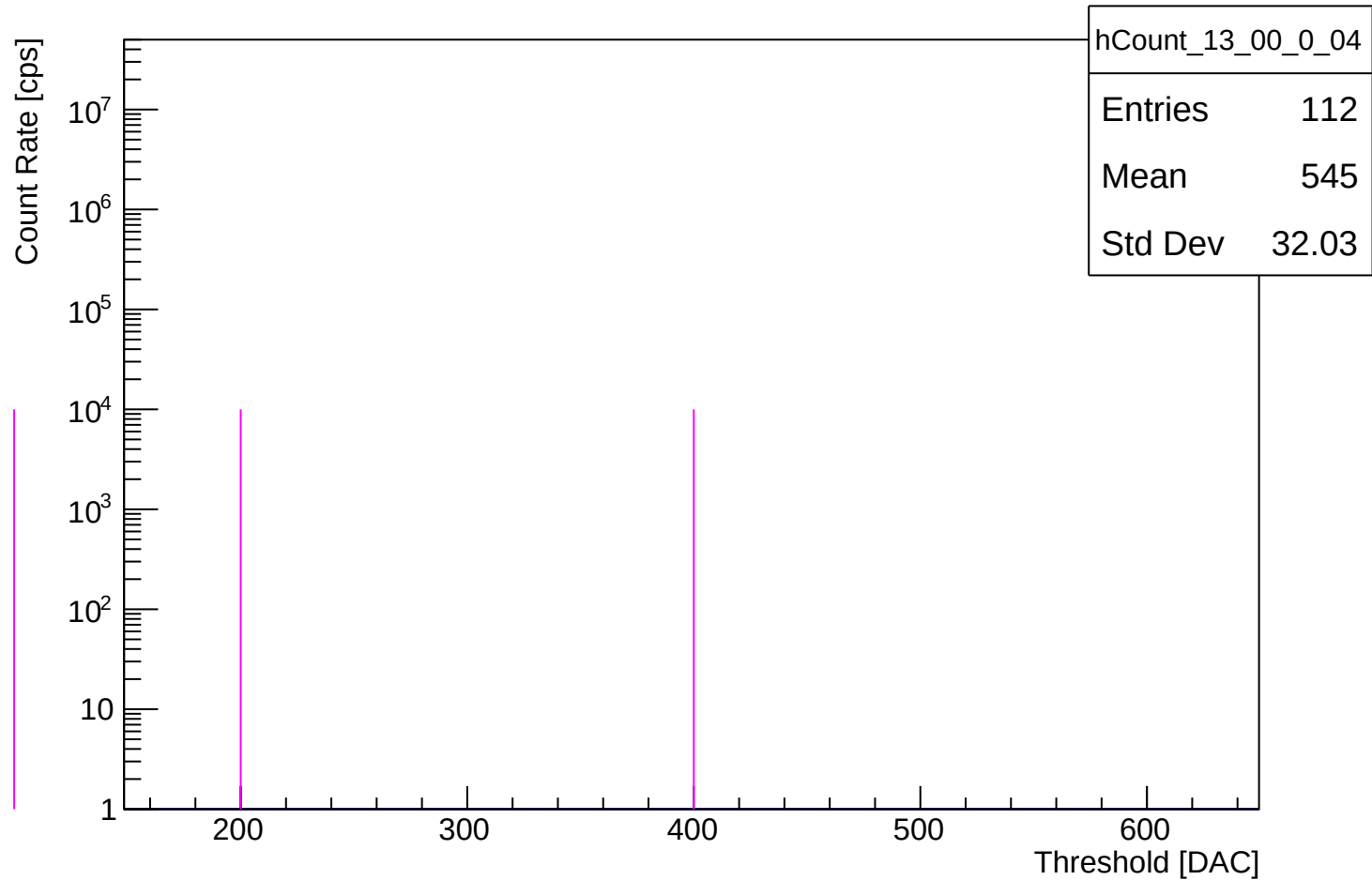




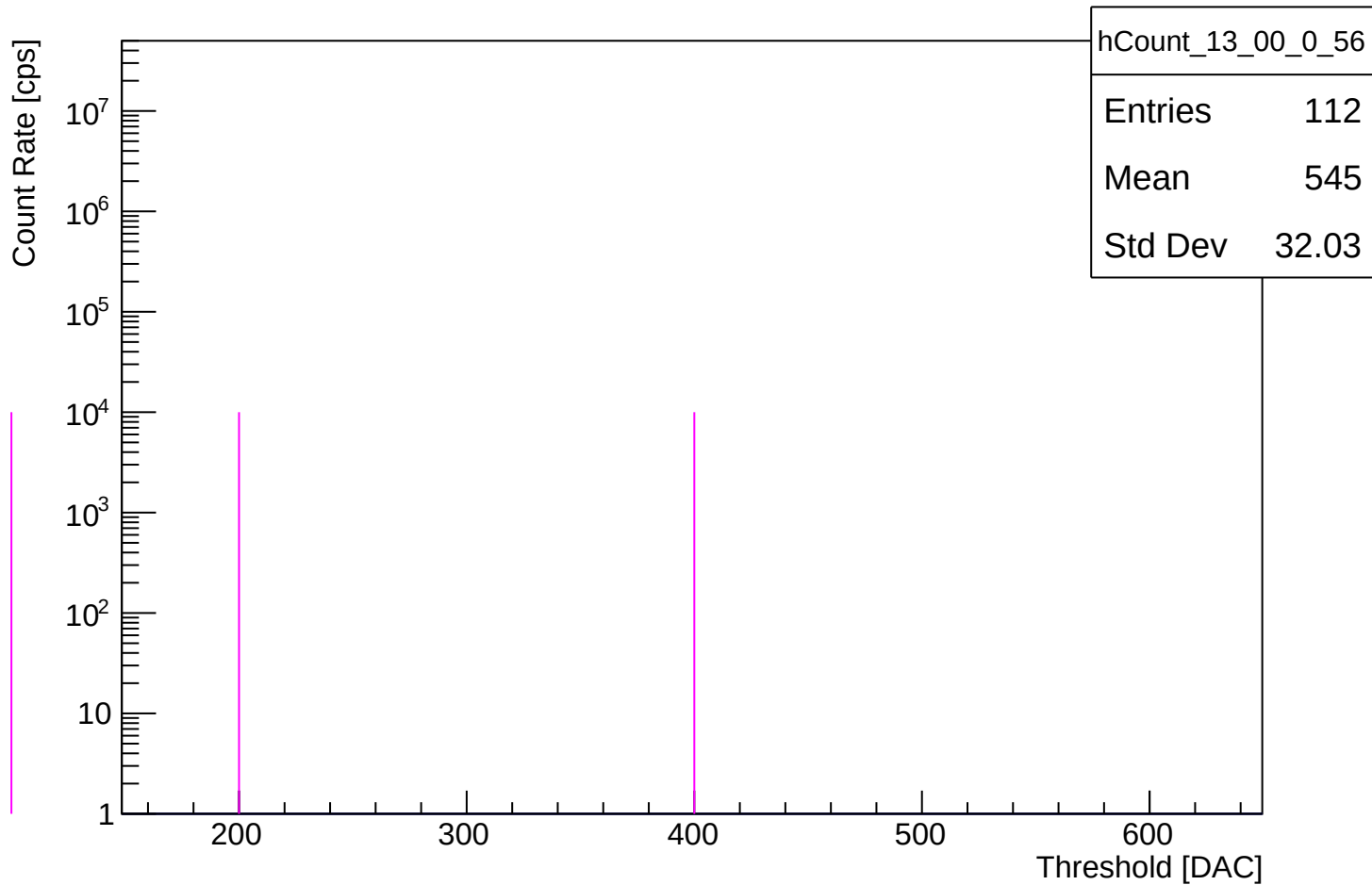
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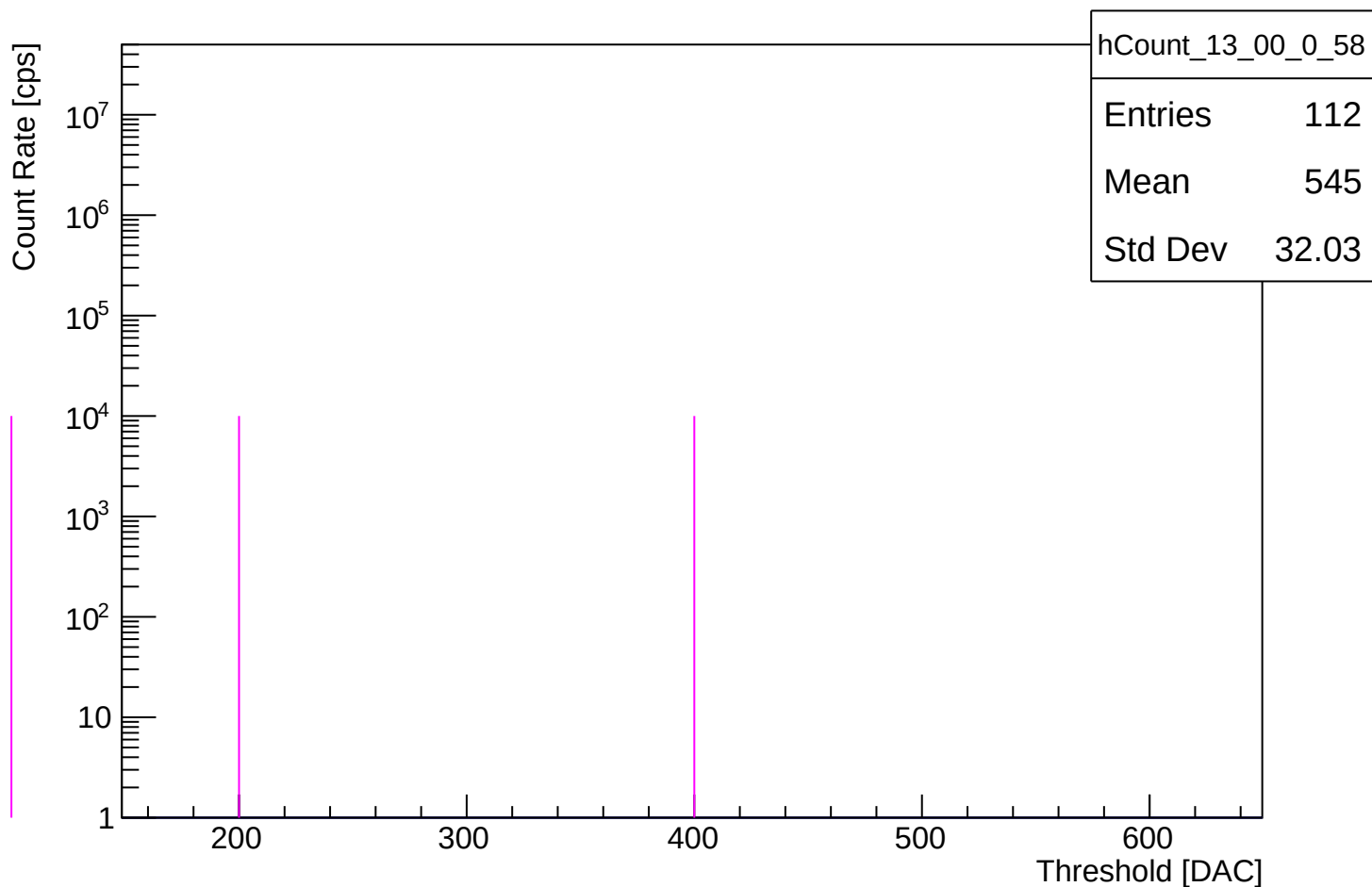




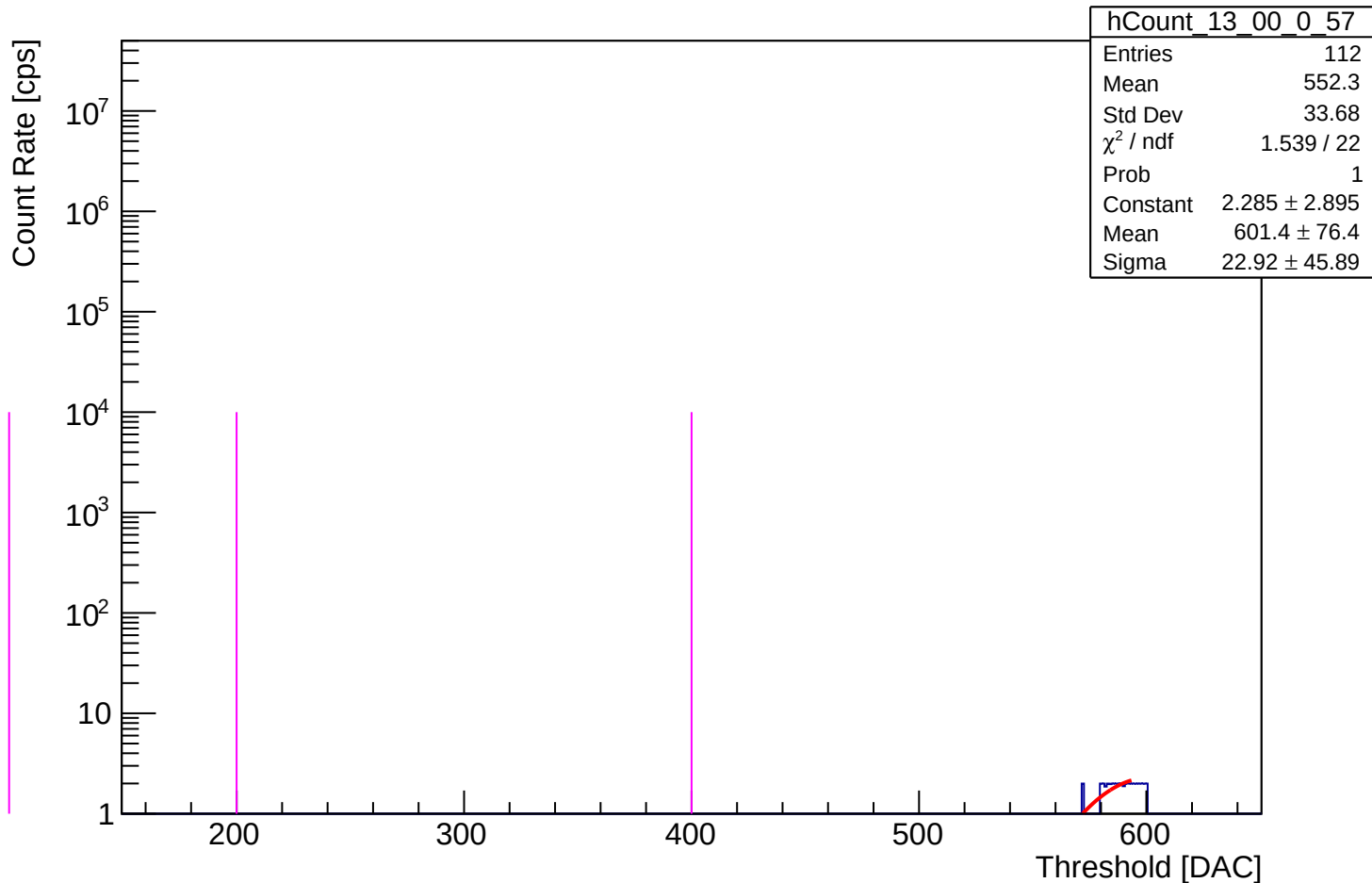
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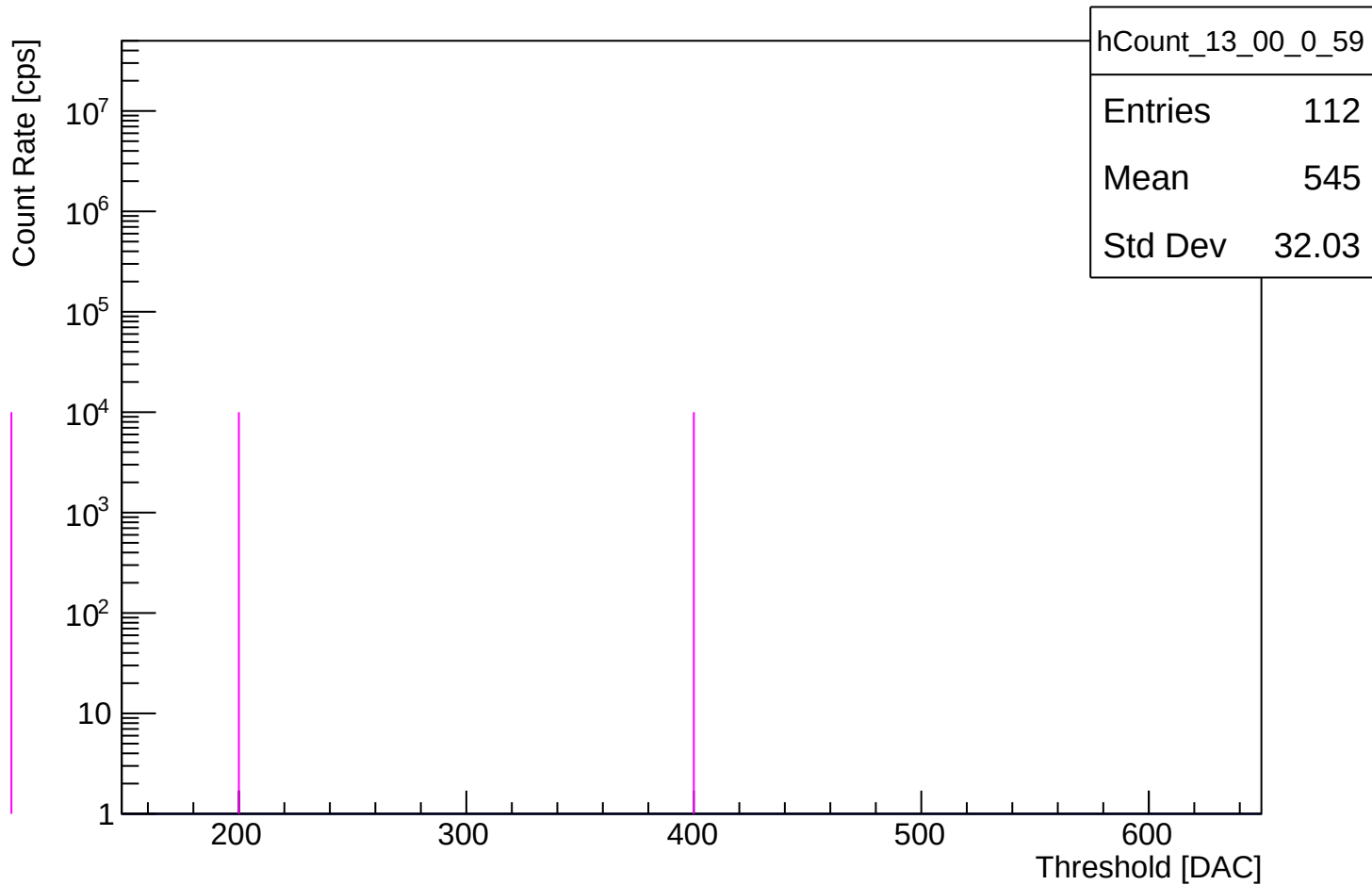
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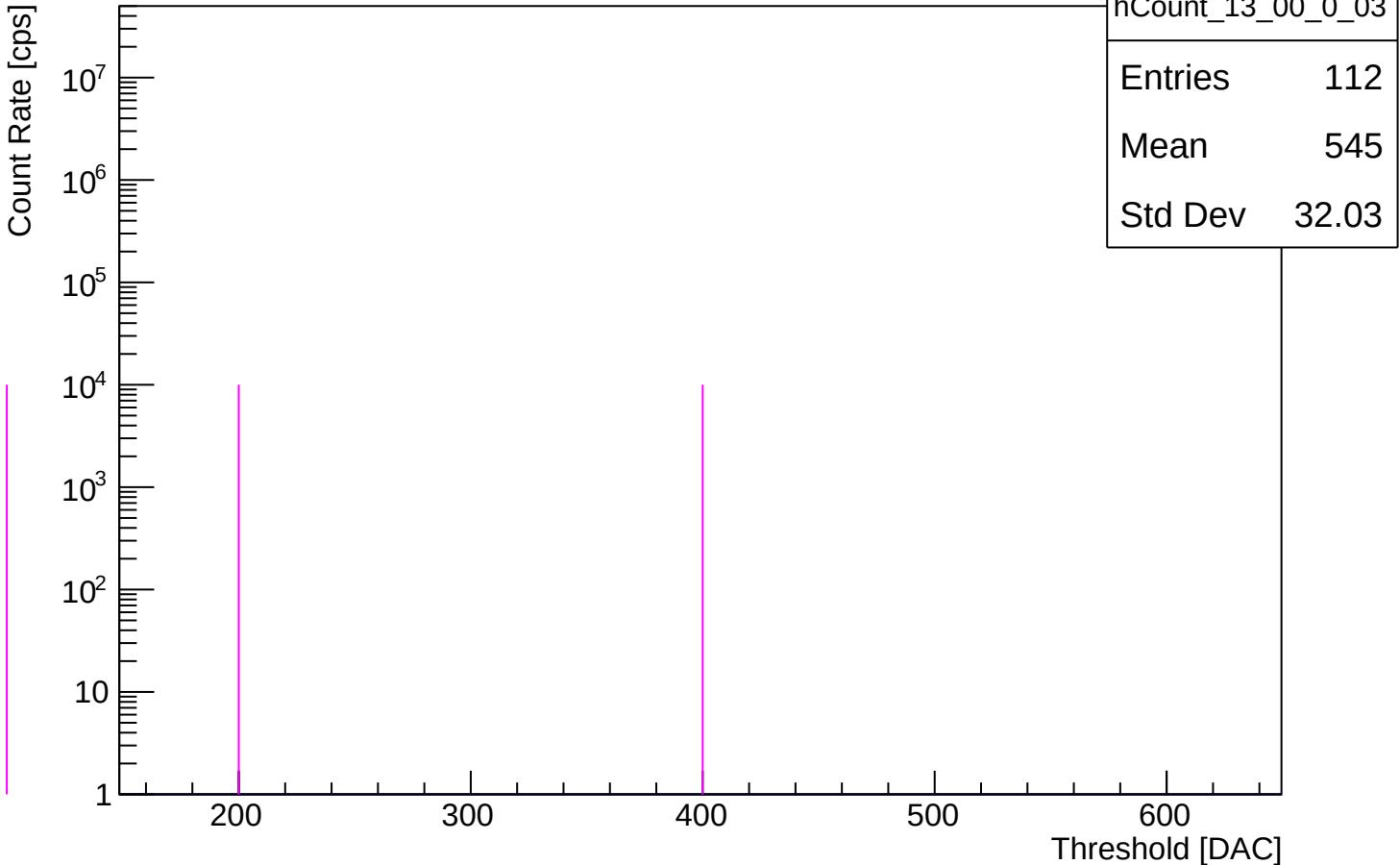
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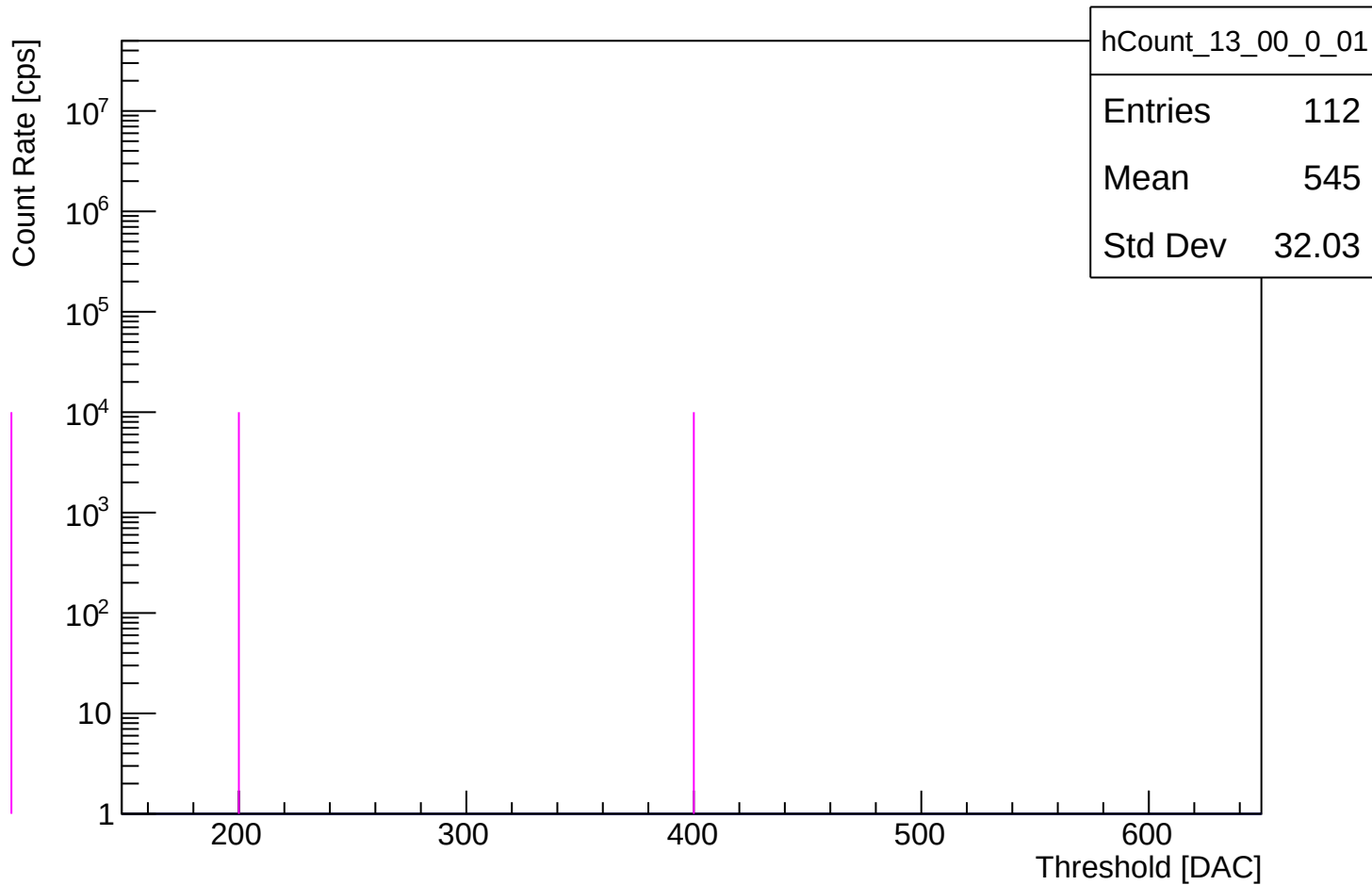
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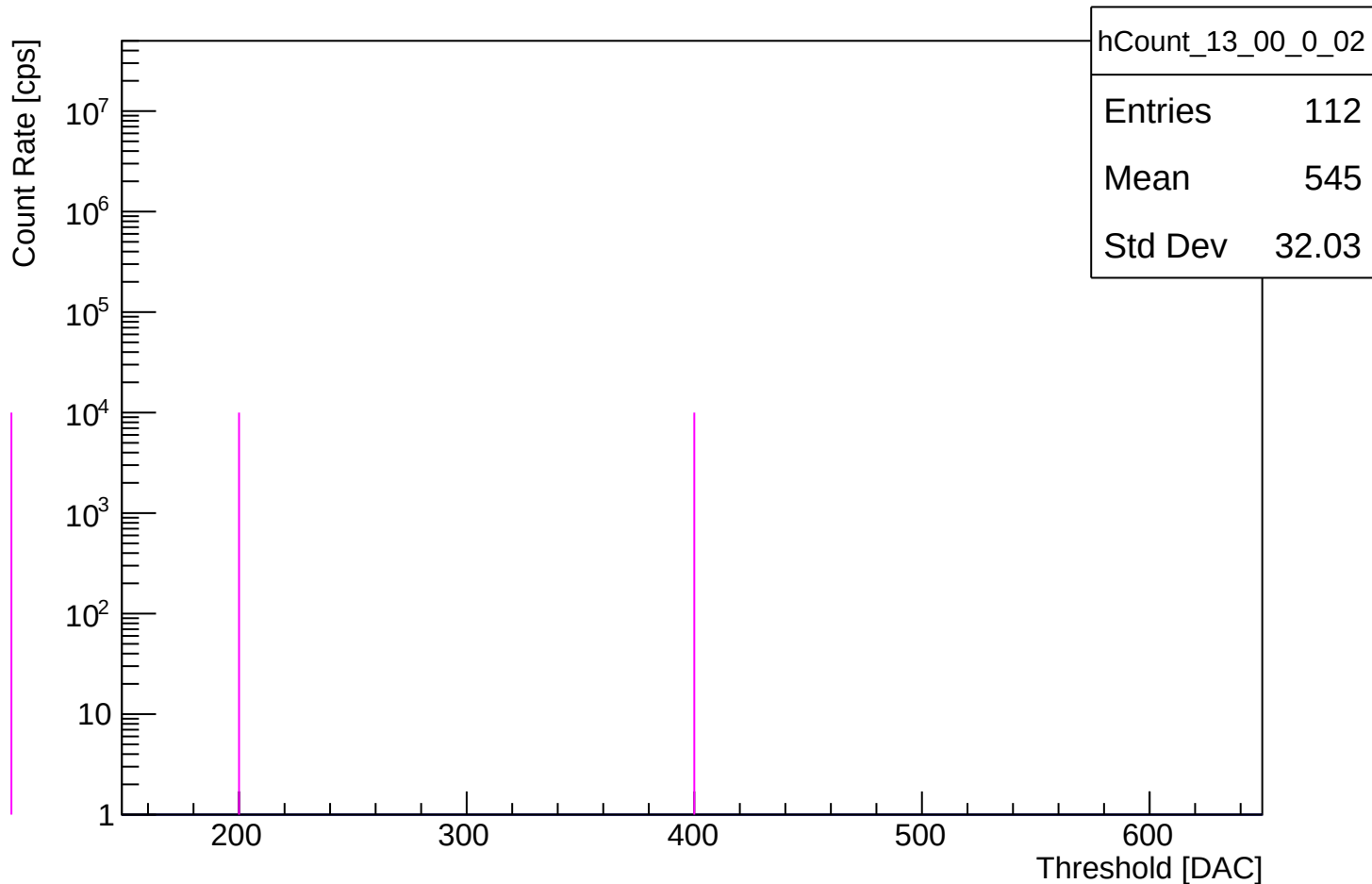


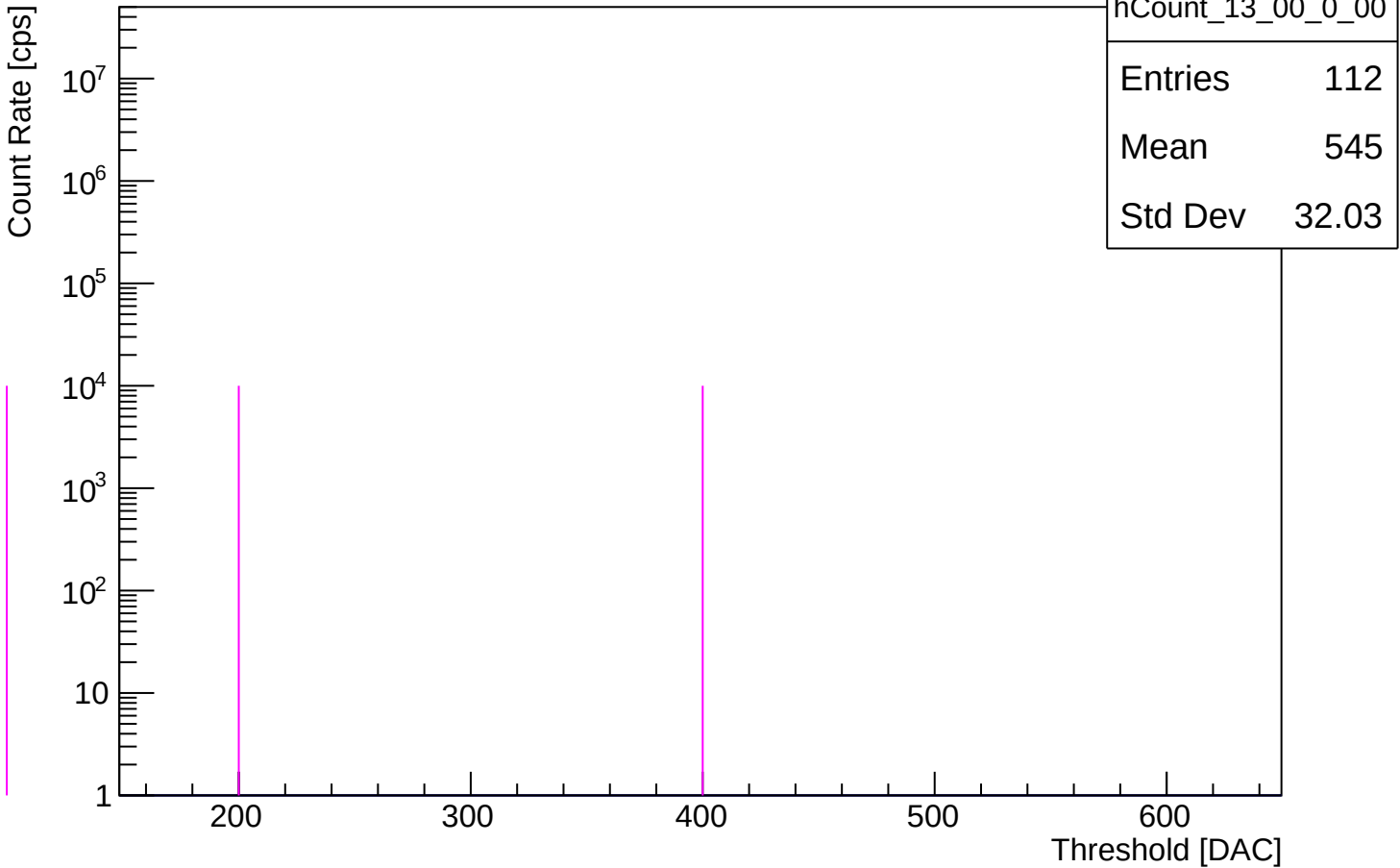


Row 1 Tile 1 Pmt 1 Pixel 58 Slot 13 Fiber 0 Asic 0 Channel 1

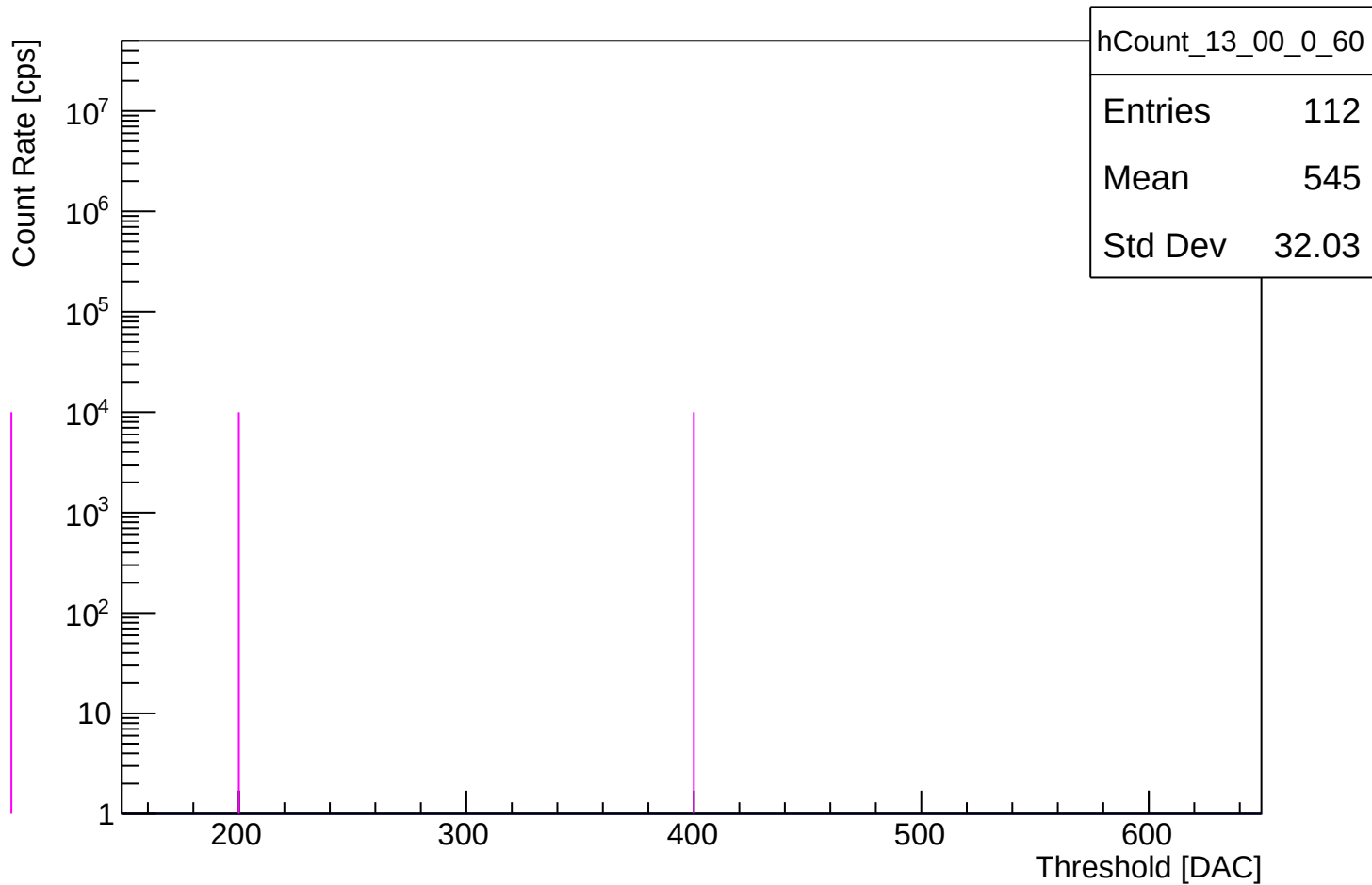


Row 1 Tile 1 Pmt 1 Pixel 59 Slot 13 Fiber 0 Asic 0 Channel 2

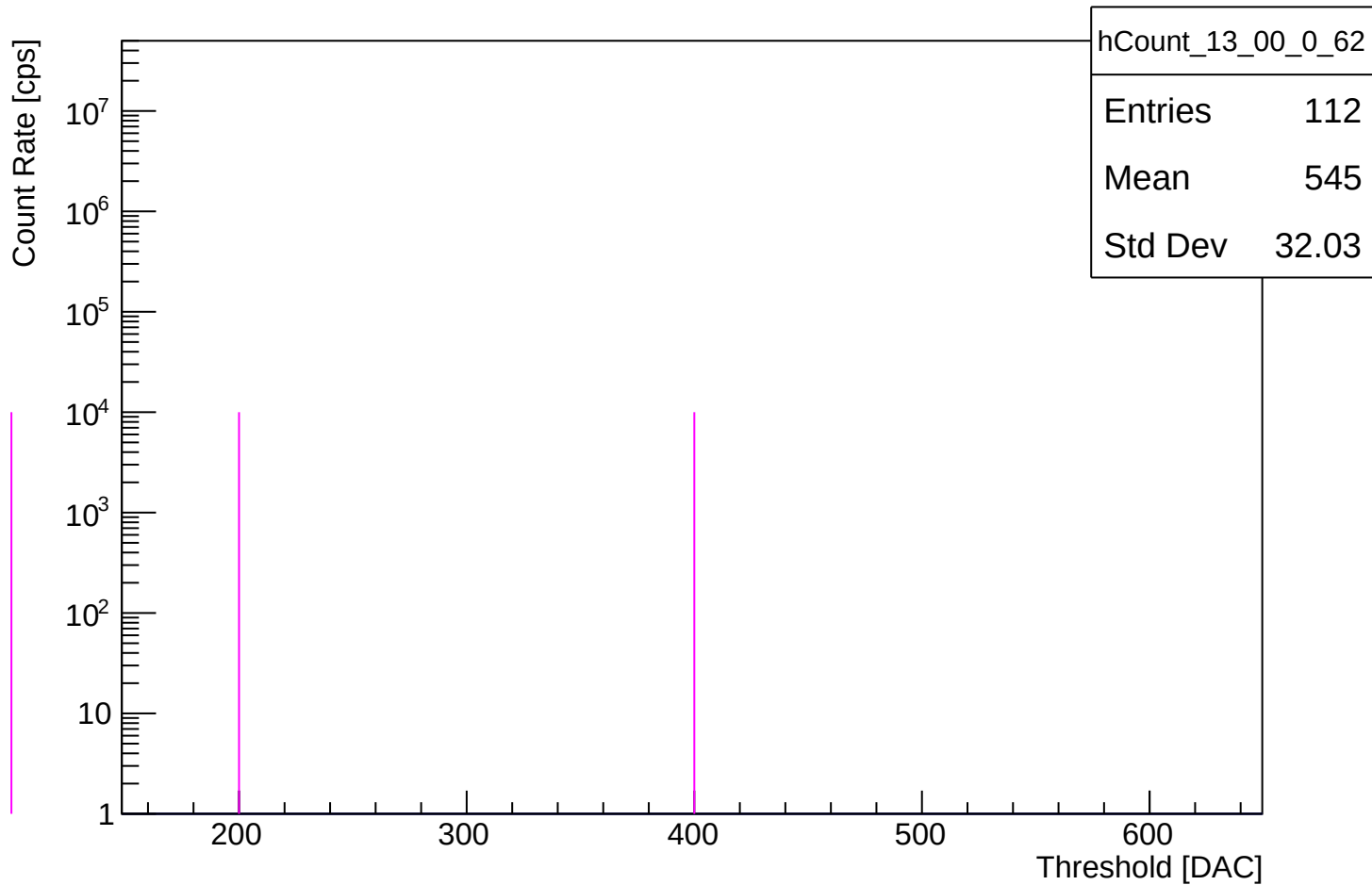




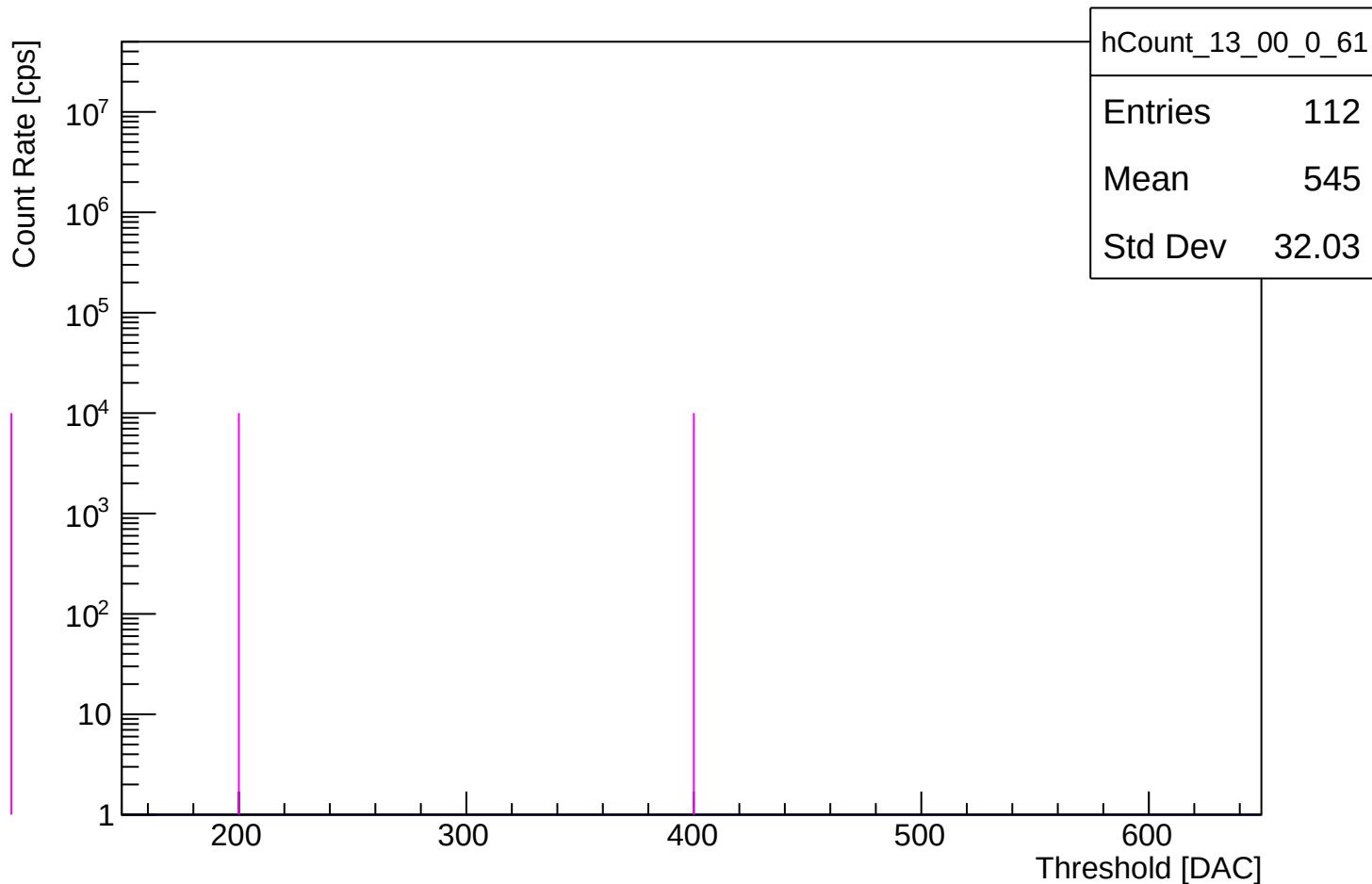
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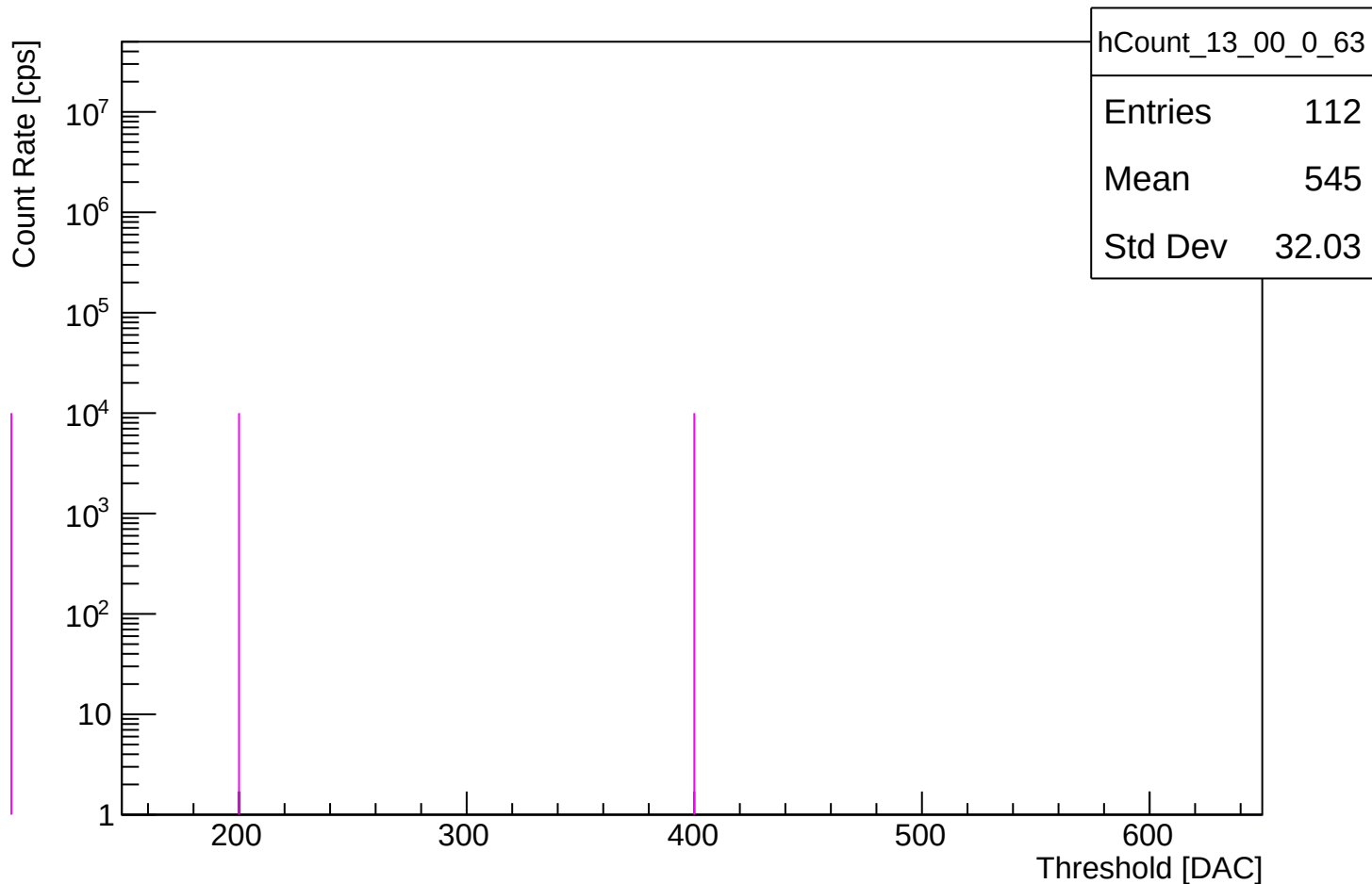
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Row 1 Tile 1 Pmt 1 Pixel 63 Slot 13 Fiber 0 Asic 0 Channel 61

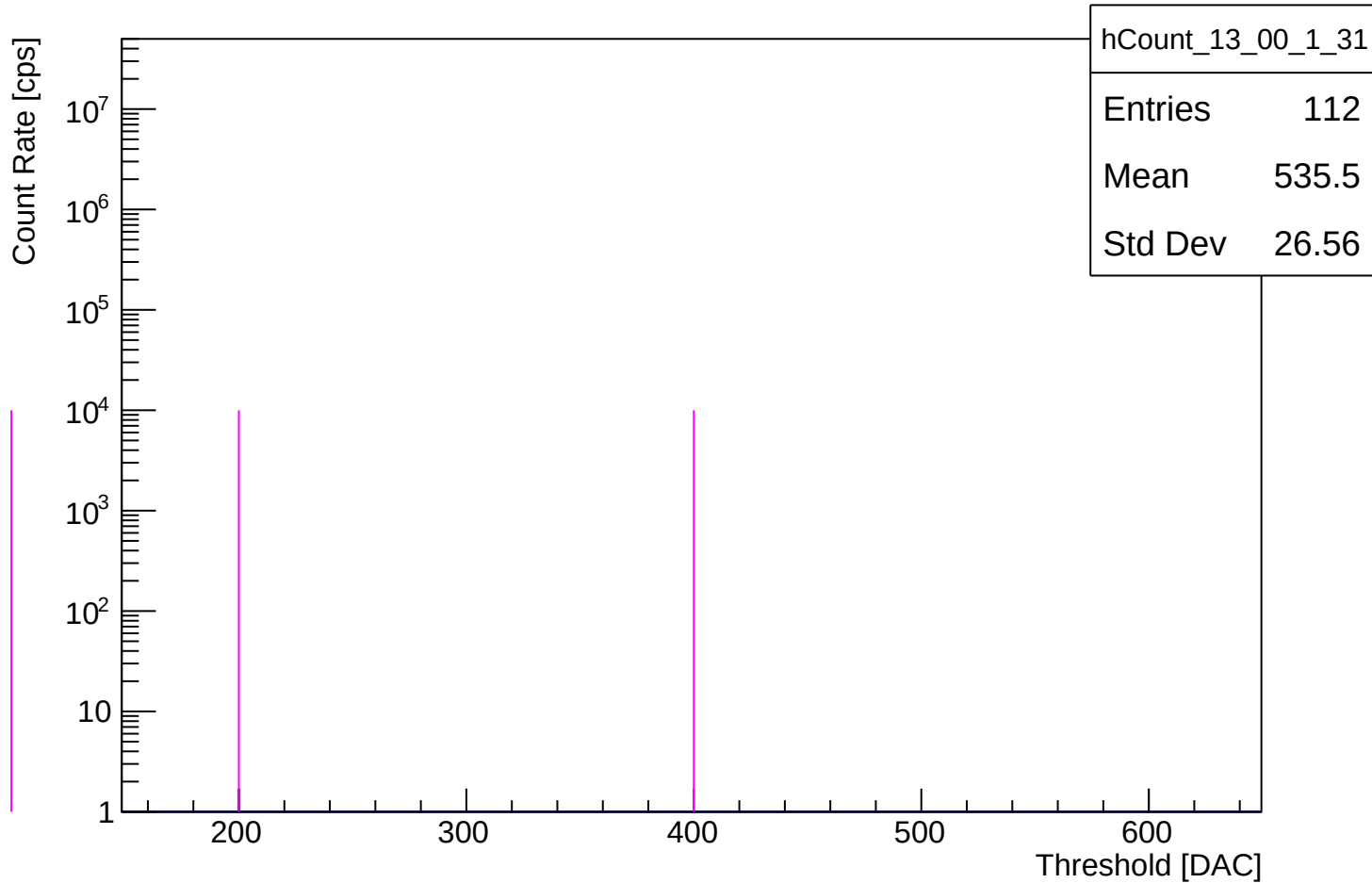


Row 1 Tile 1 Pmt 1 Pixel 64 Slot 13 Fiber 0 Asic 0 Channel 63

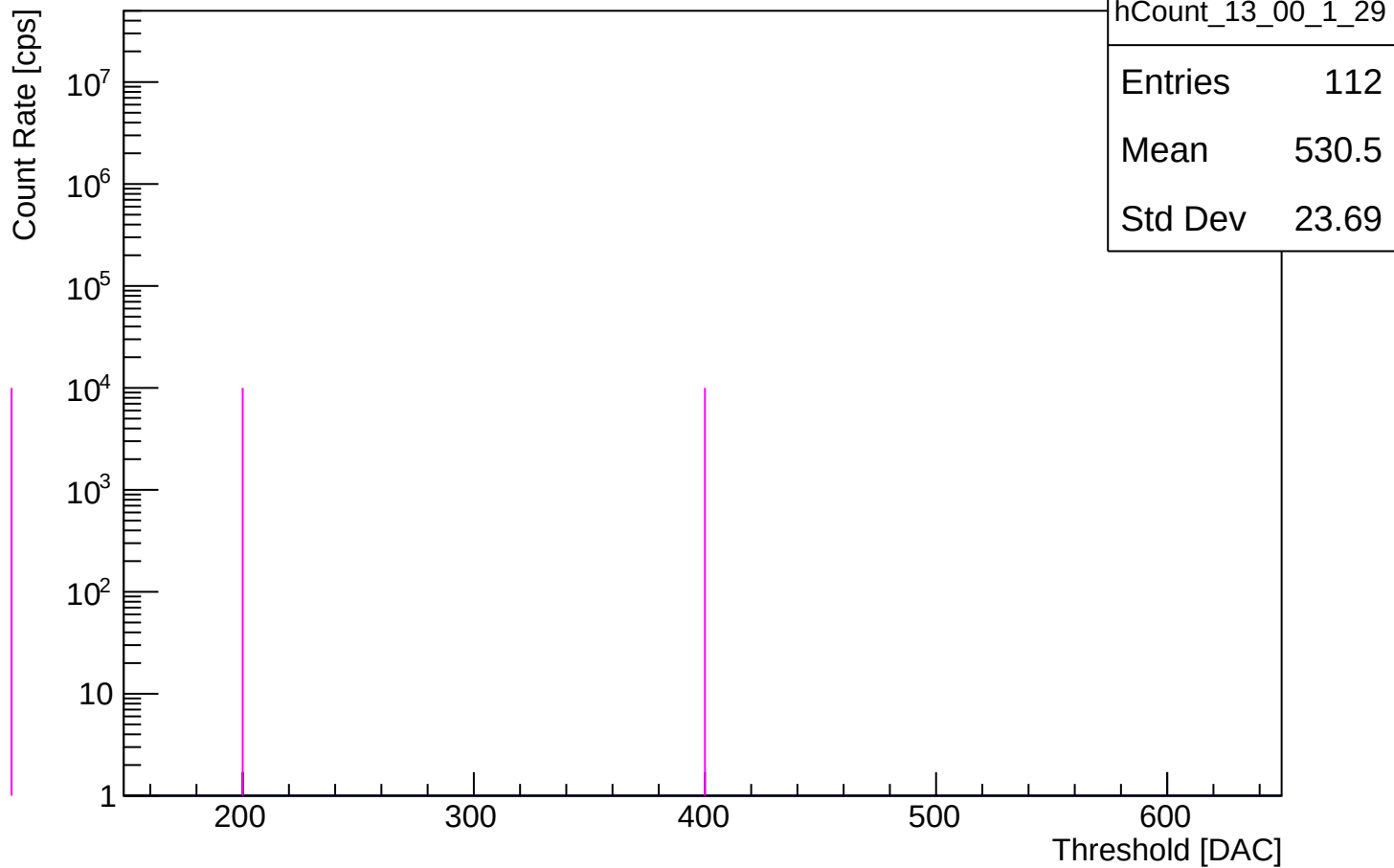




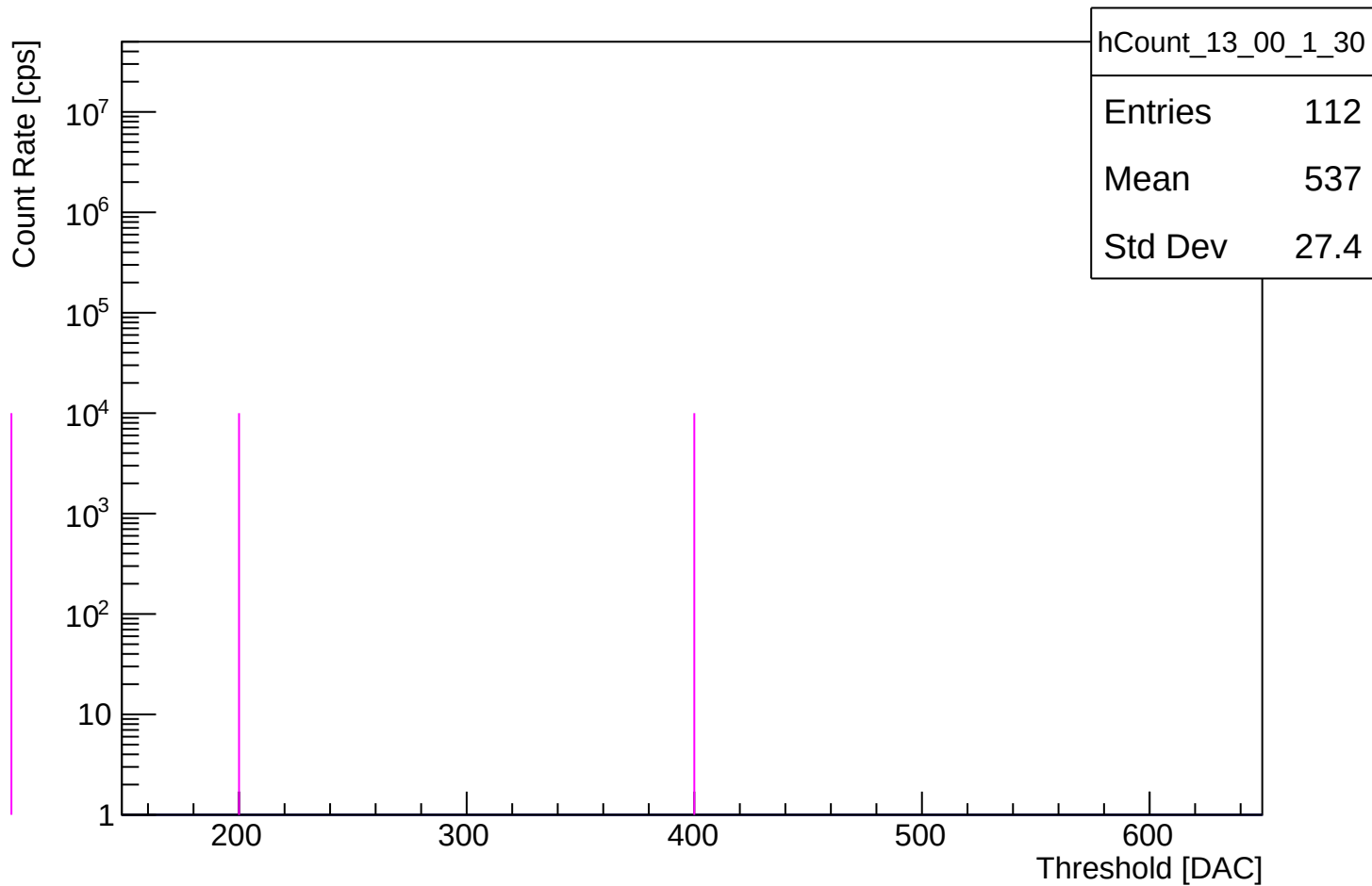
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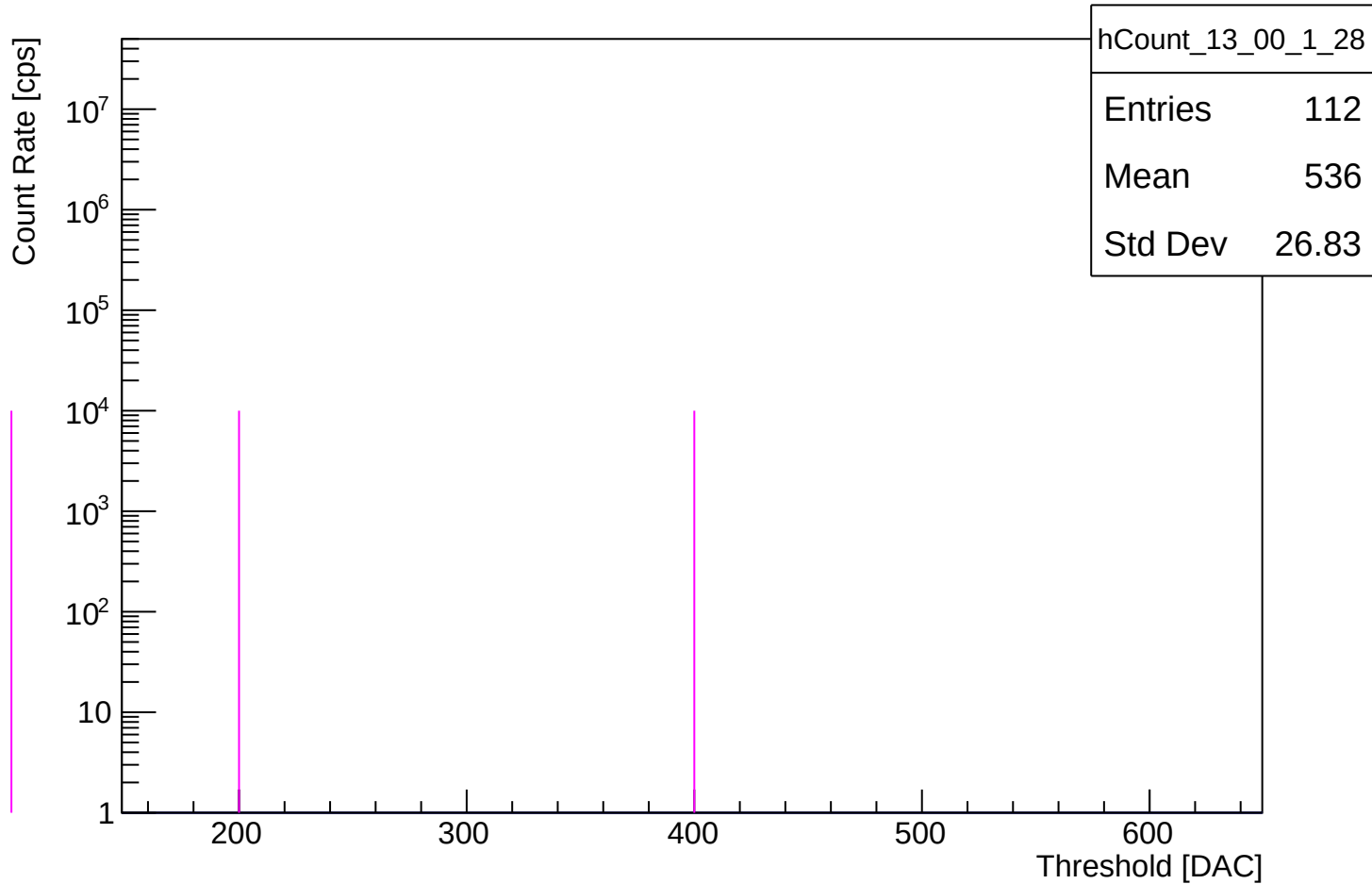
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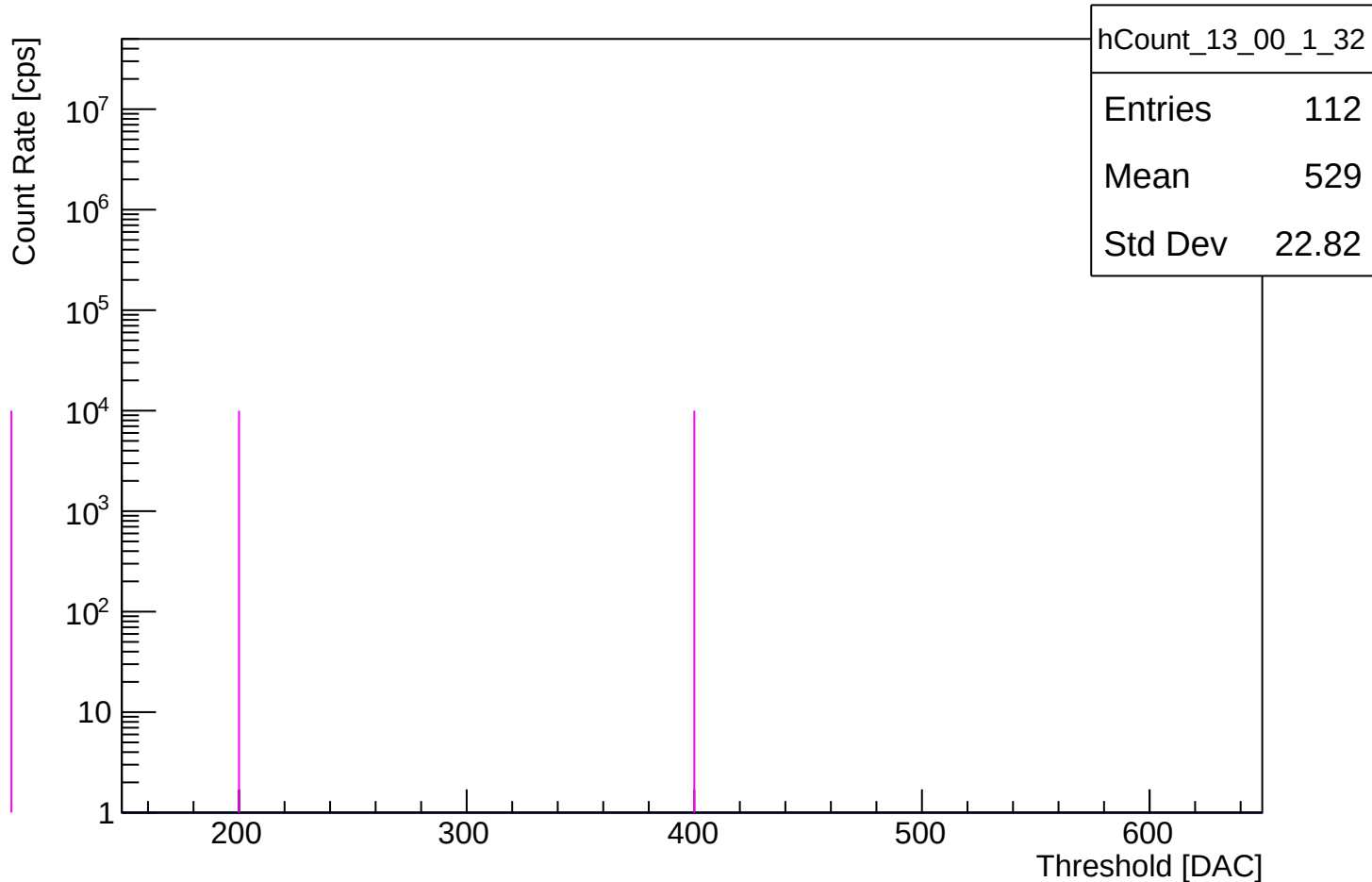
Row 1 Tile 1 Pmt 2 Pixel 3 Slot 13 Fiber 0 Asic 1 Channel 30



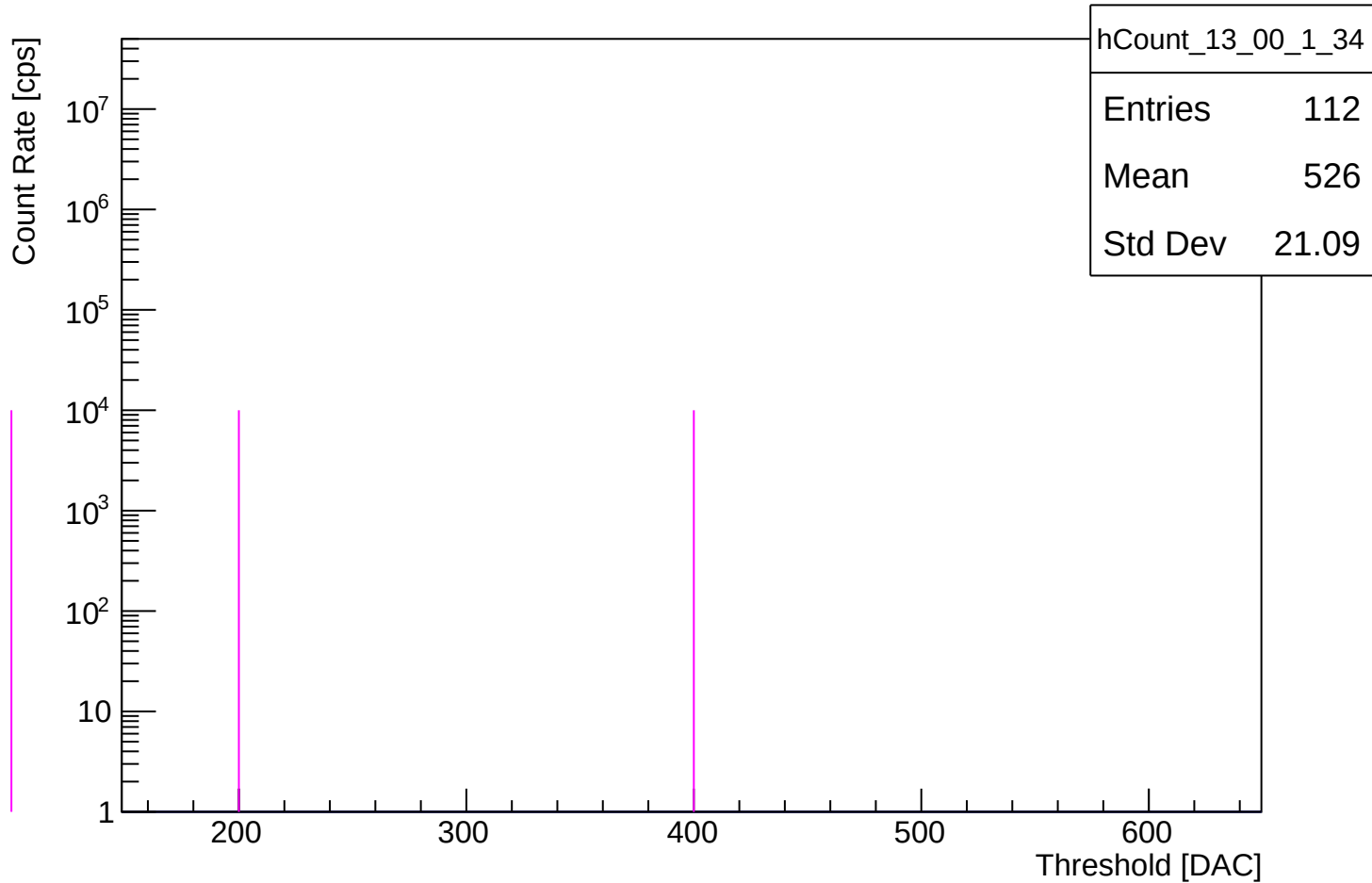
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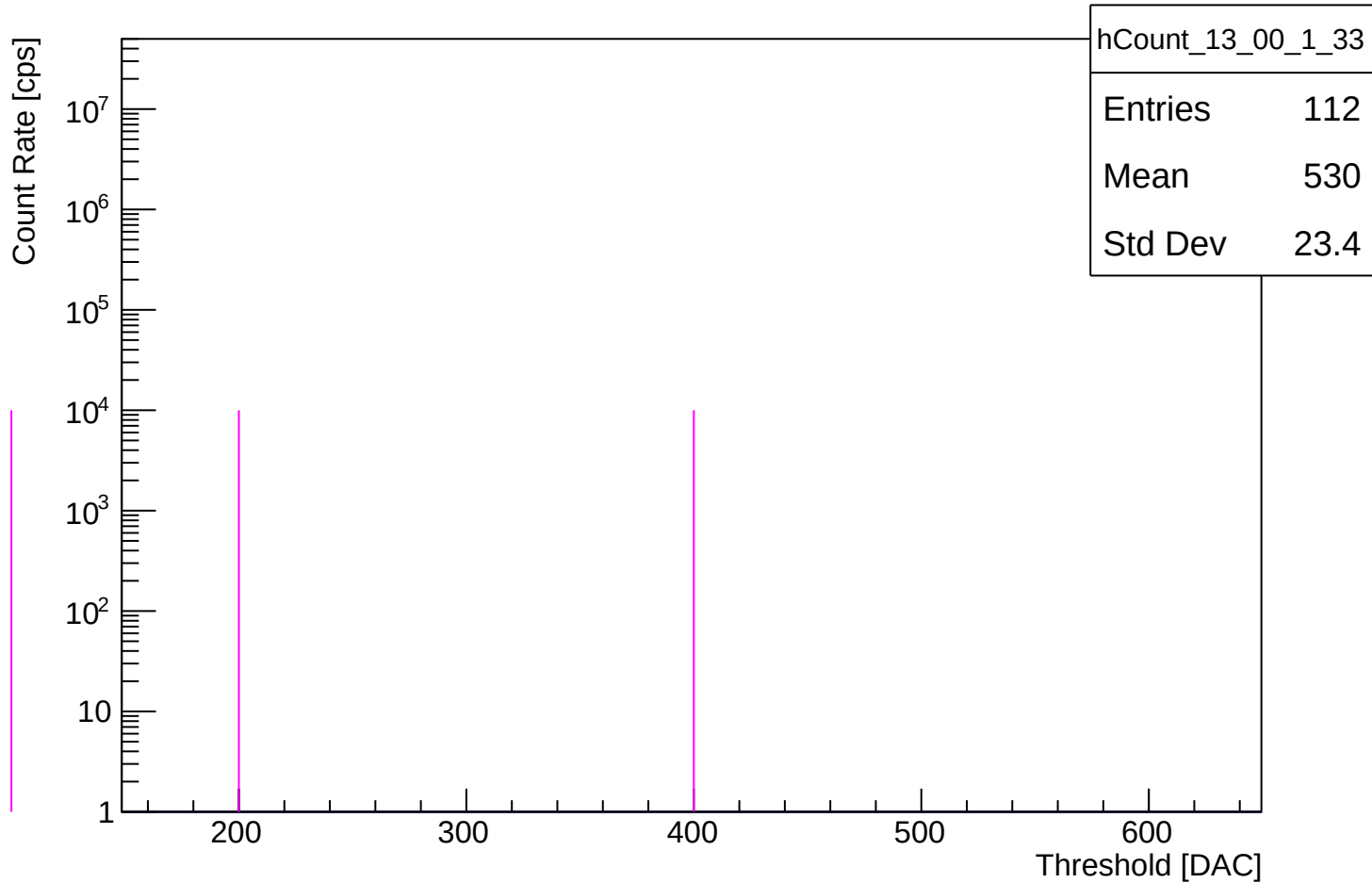
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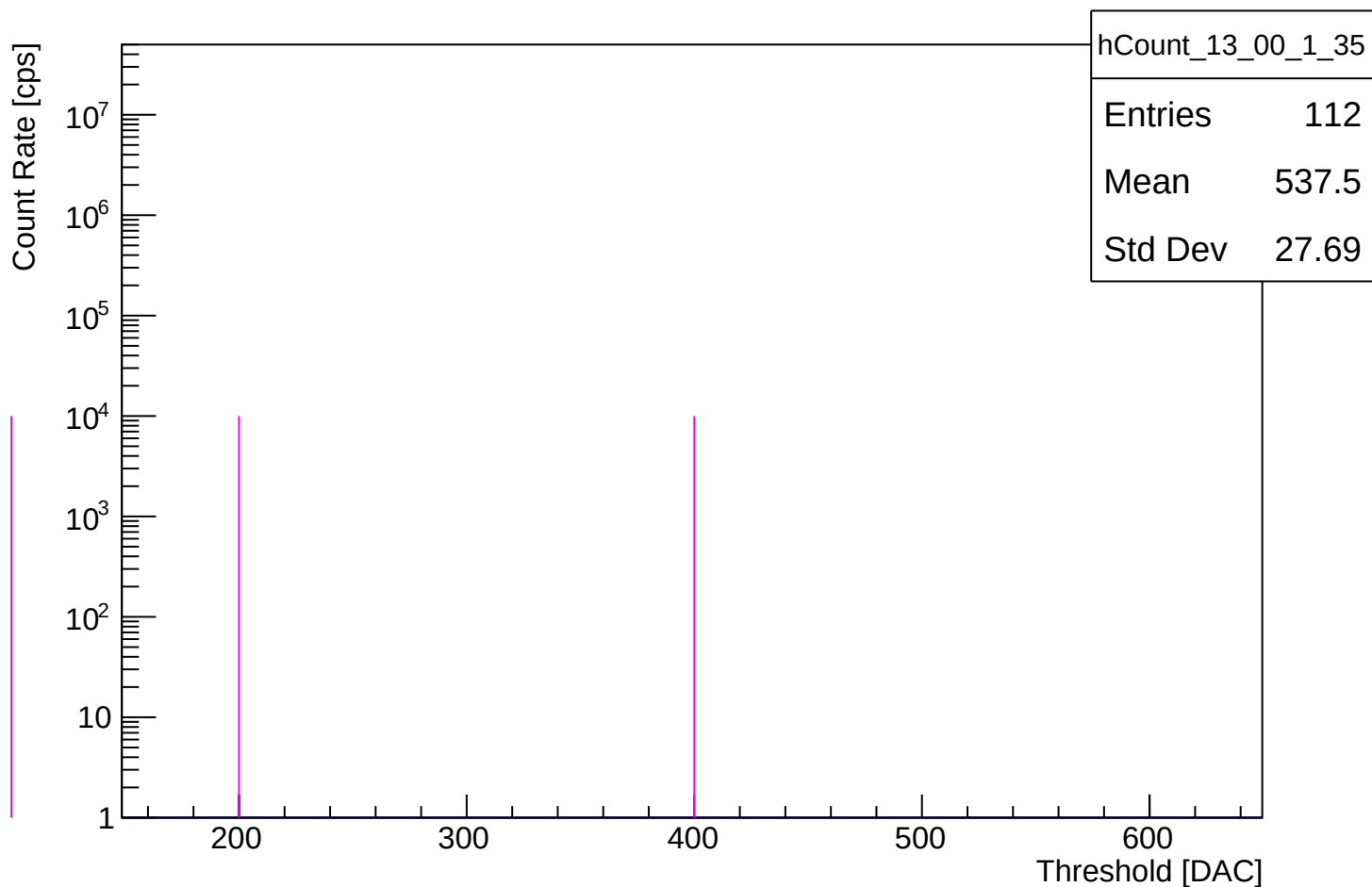
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Row 1 Tile 1 Pmt 2 Pixel 7 Slot 13 Fiber 0 Asic 1 Channel 33

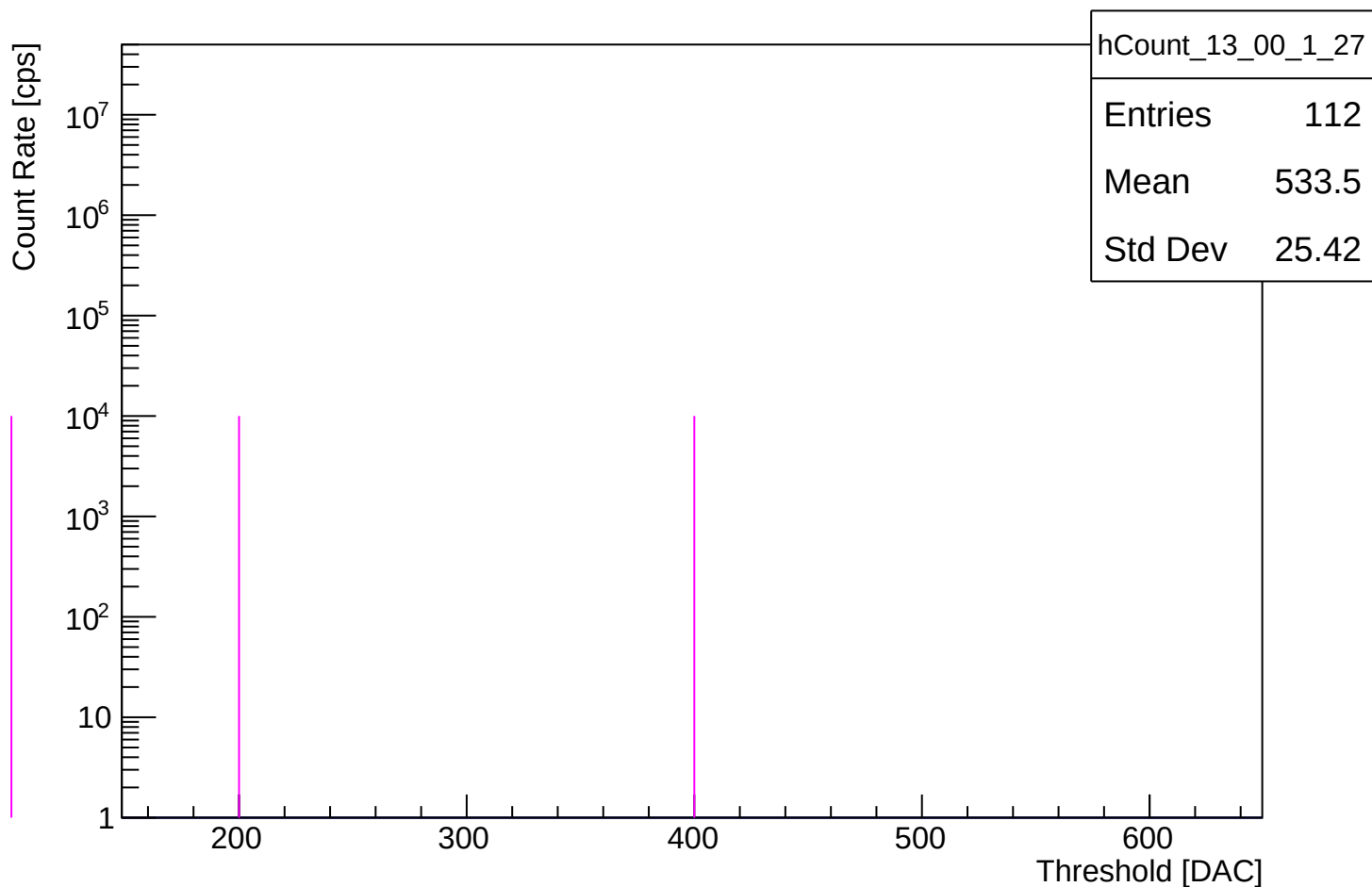


Row 1 Tile 1 Pmt 2 Pixel 8 Slot 13 Fiber 0 Asic 1 Channel 35

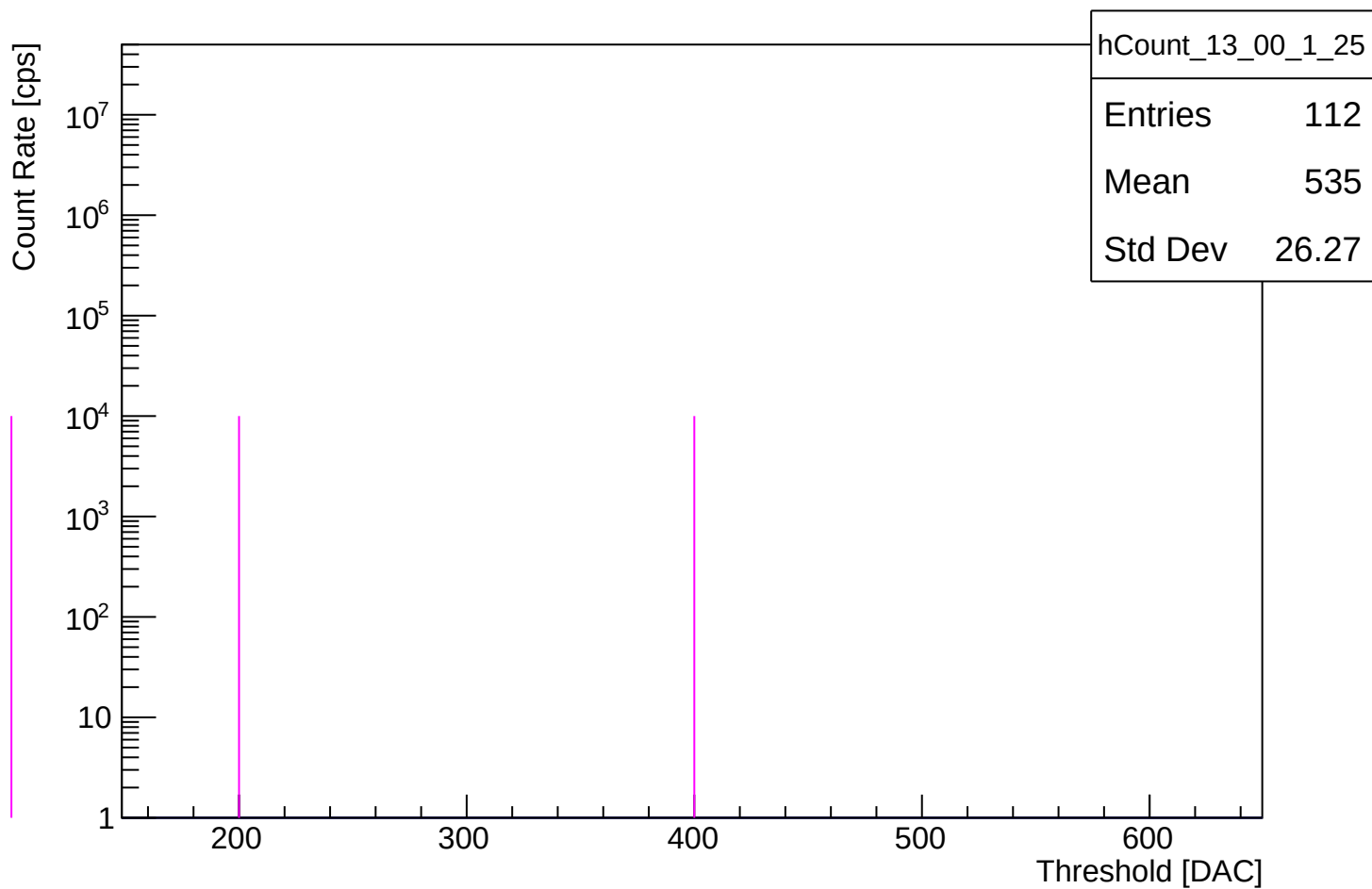




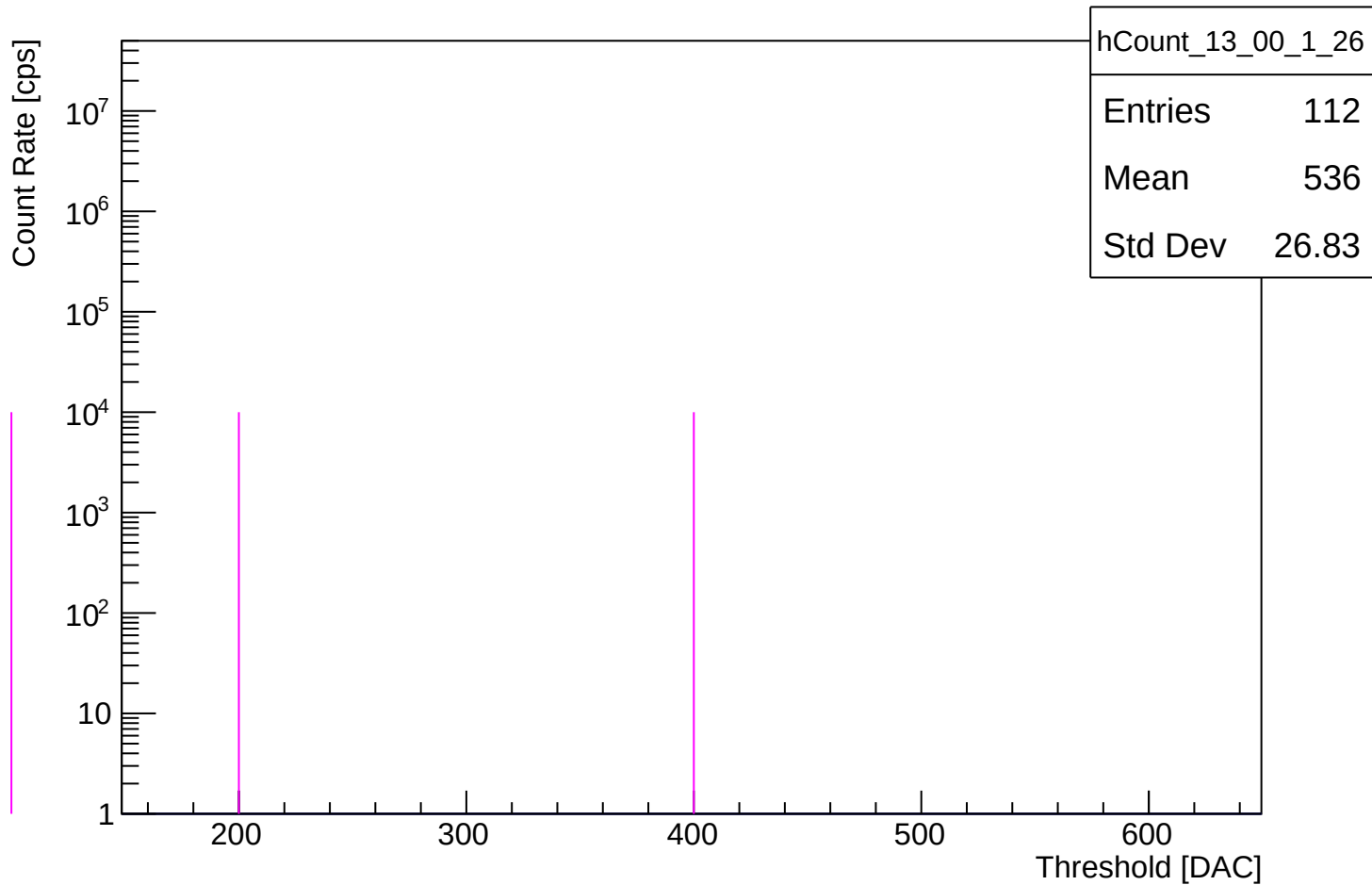
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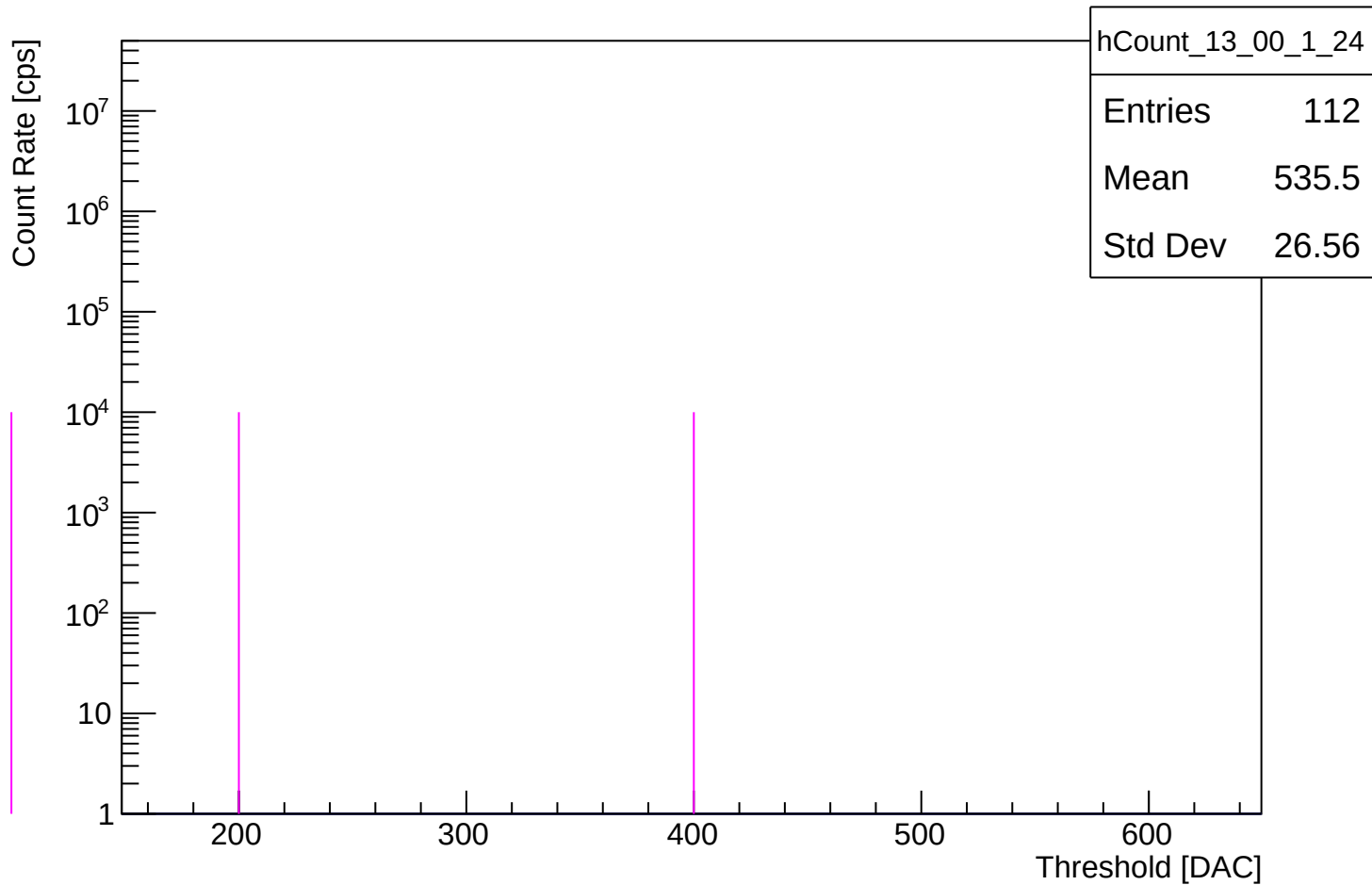
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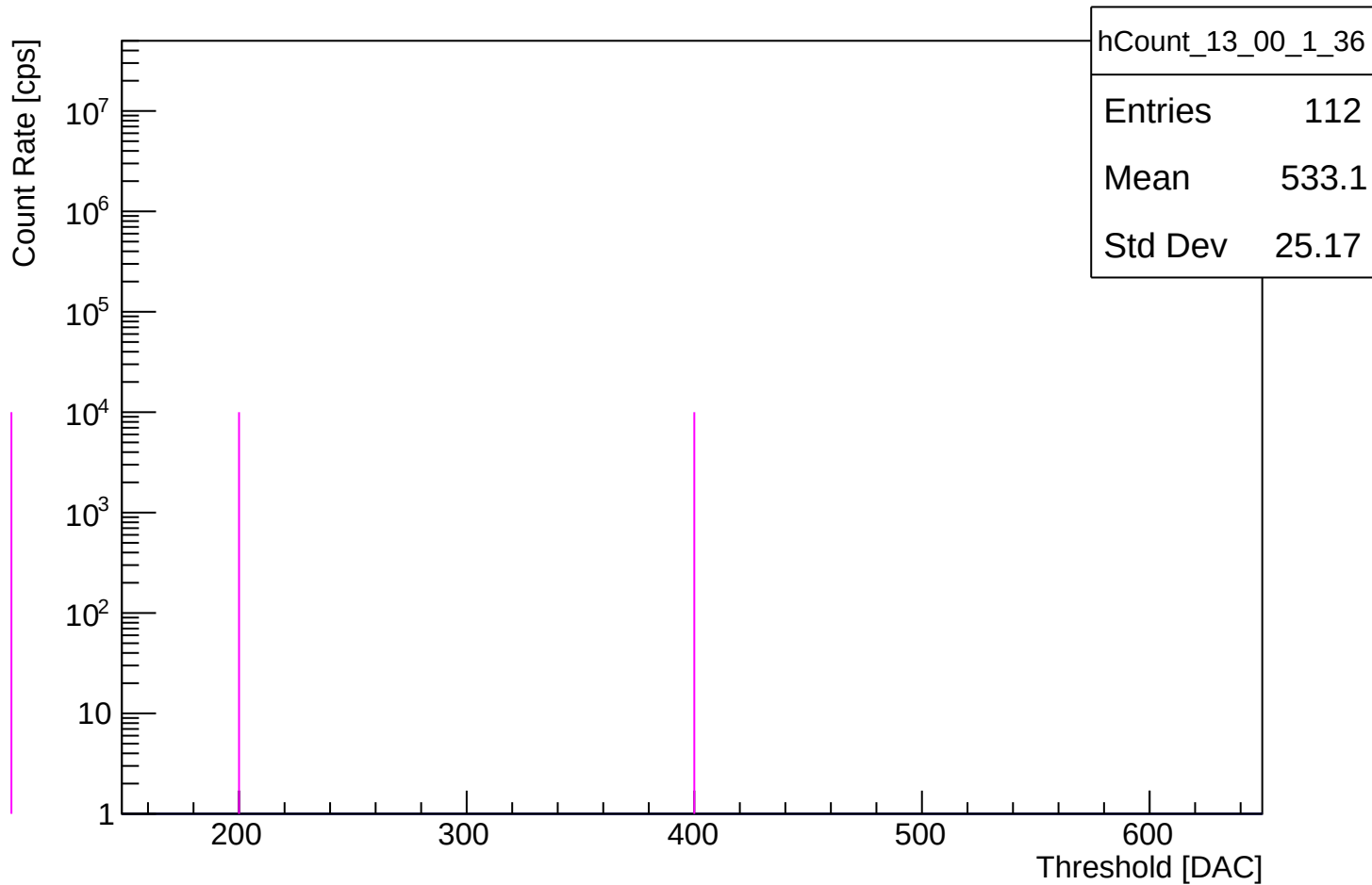
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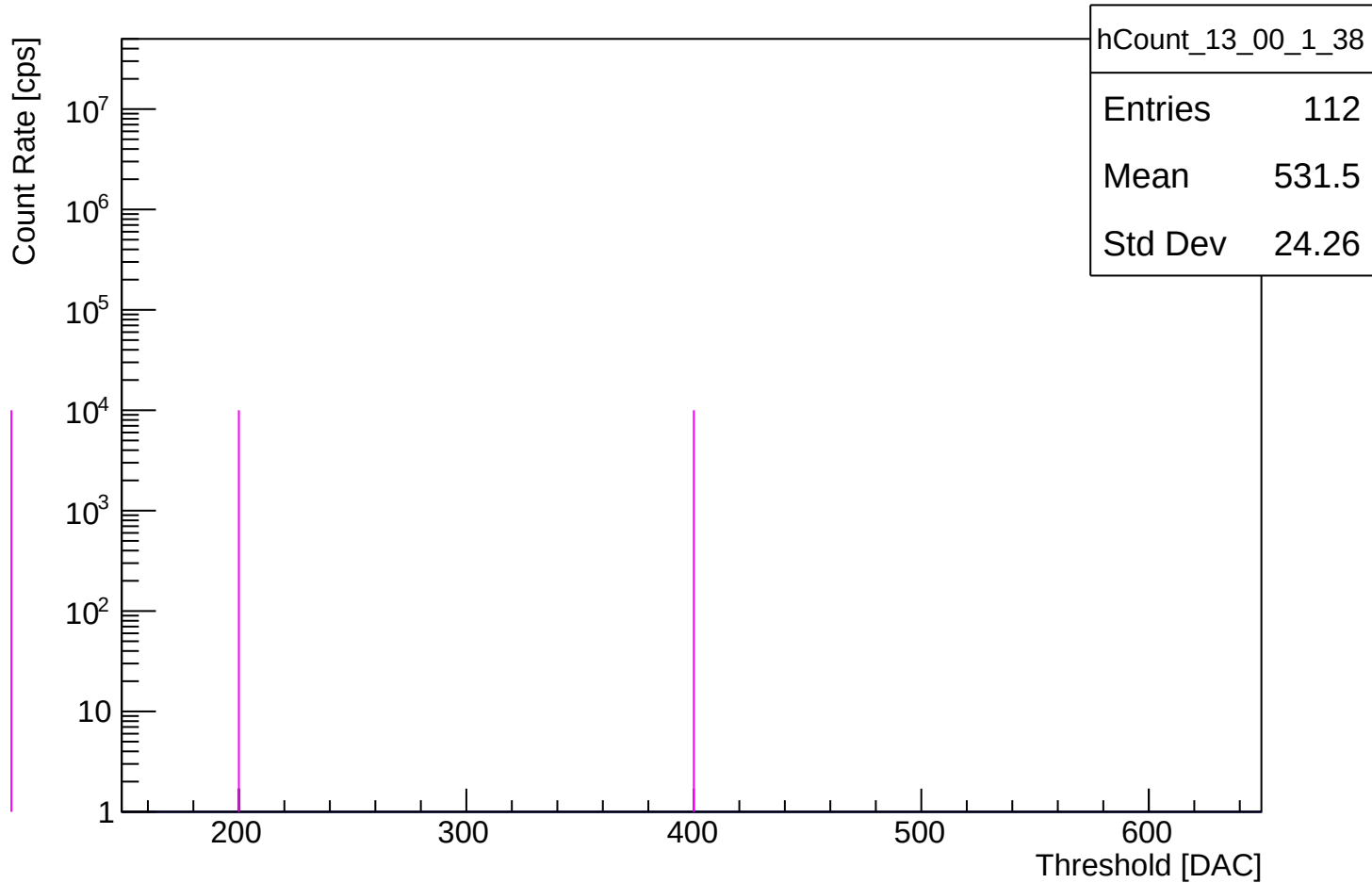
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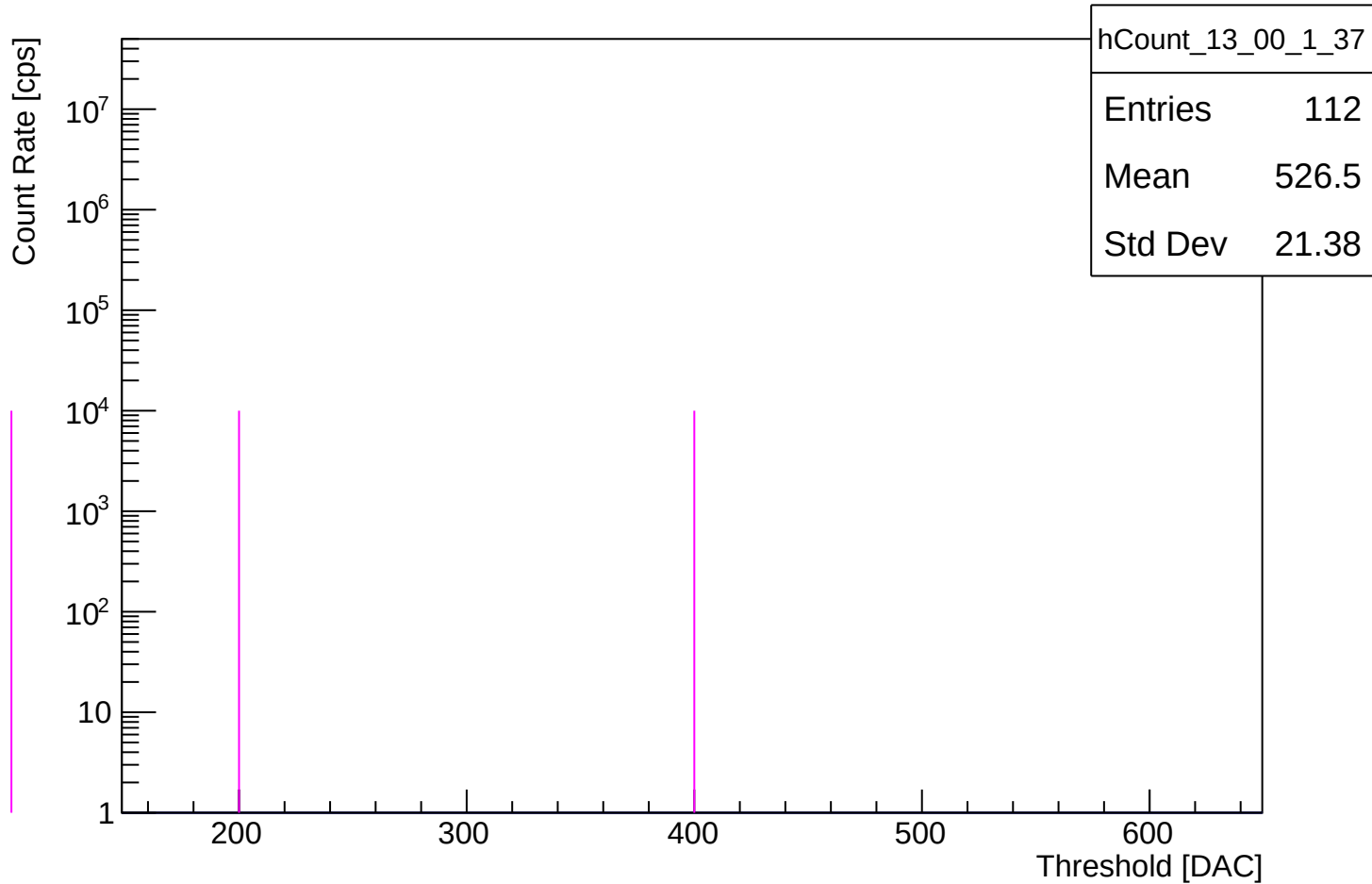
Row 1 Tile 1 Pmt 2 Pixel 13 Slot 13 Fiber 0 Asic 1 Channel 36



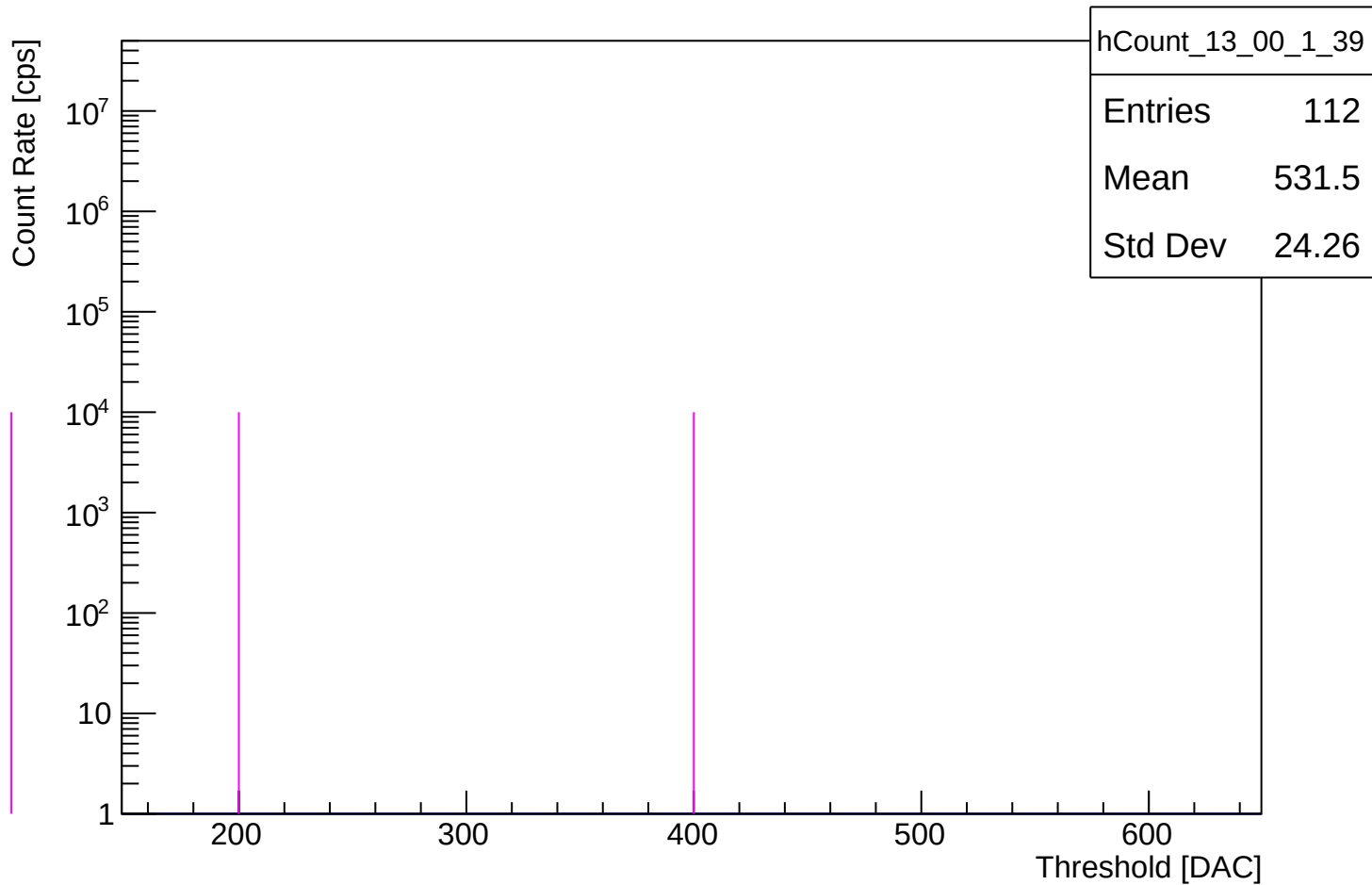
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Row 1 Tile 1 Pmt 2 Pixel 15 Slot 13 Fiber 0 Asic 1 Channel 37

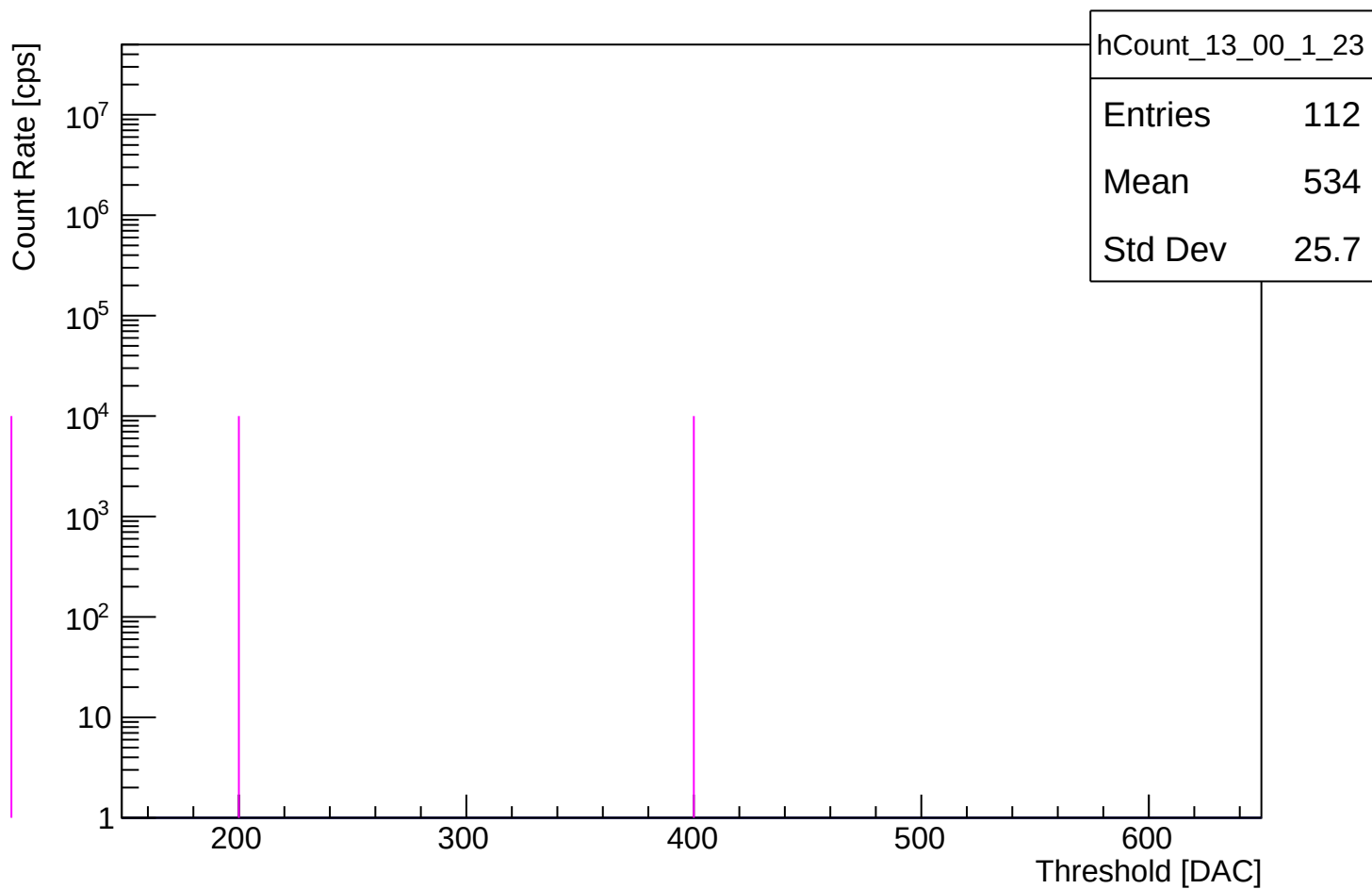


Row 1 Tile 1 Pmt 2 Pixel 16 Slot 13 Fiber 0 Asic 1 Channel 39

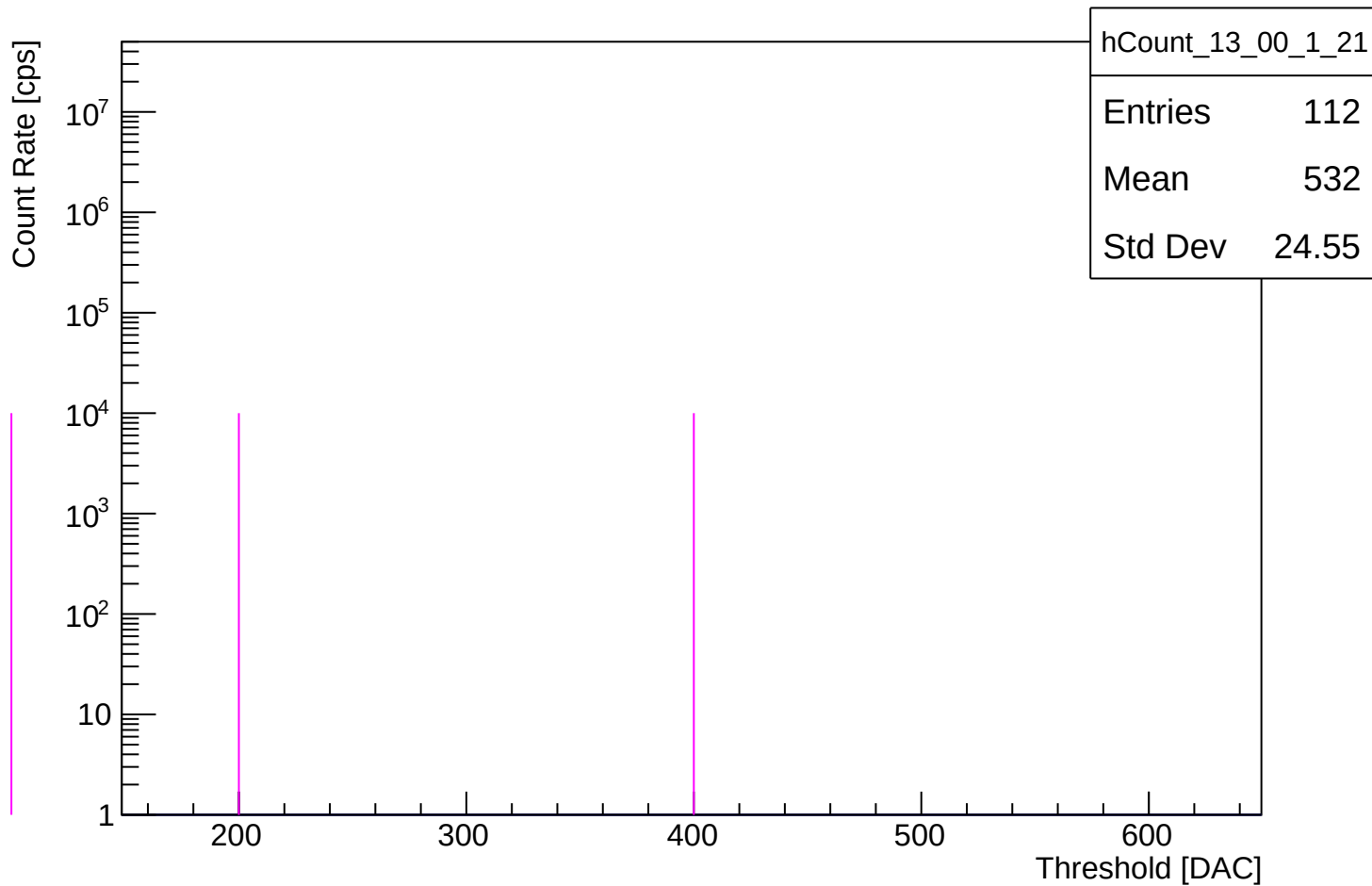




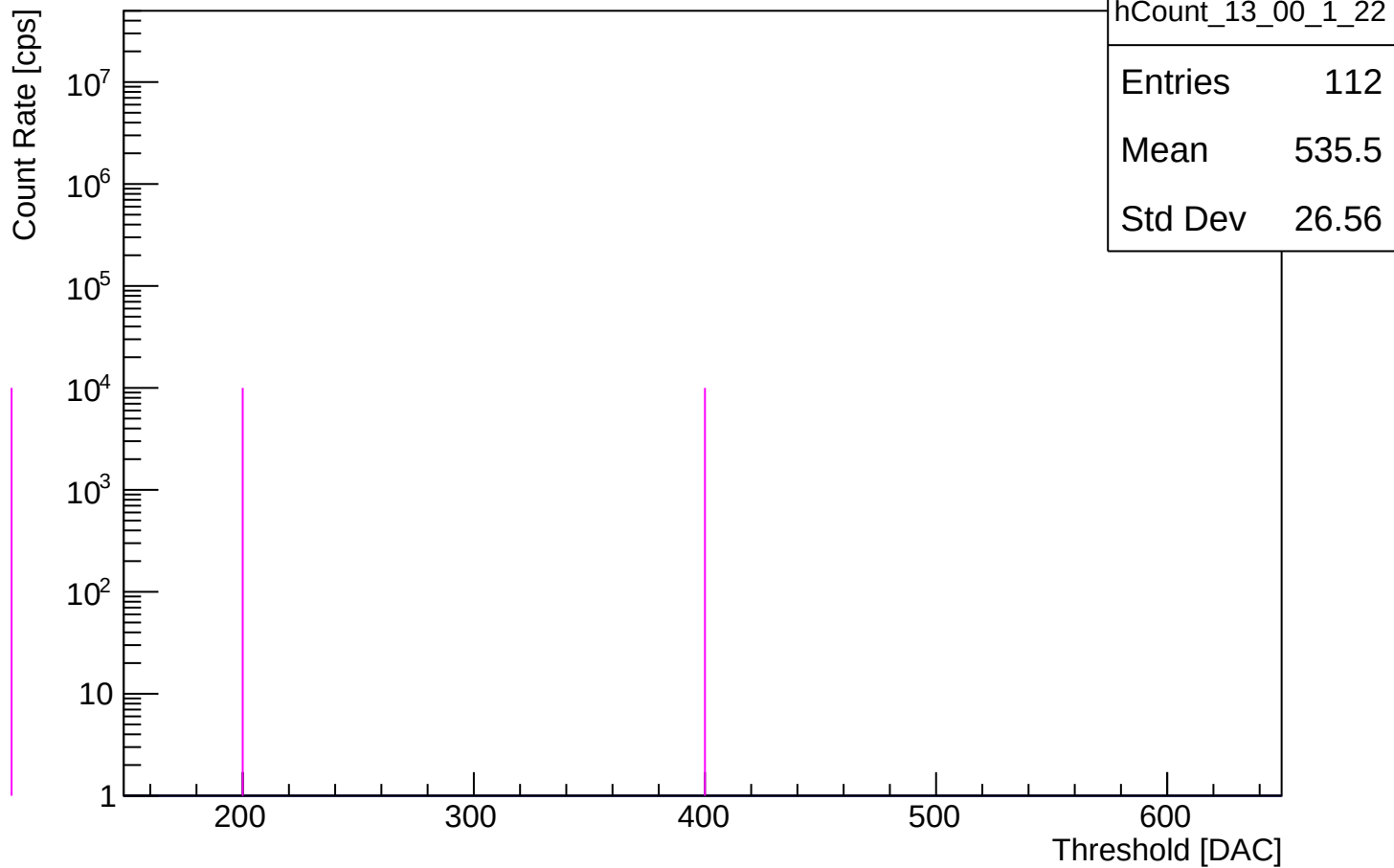
Row 1 Tile 1 Pmt 2 Pixel 17 Slot 13 Fiber 0 Asic 1 Channel 23



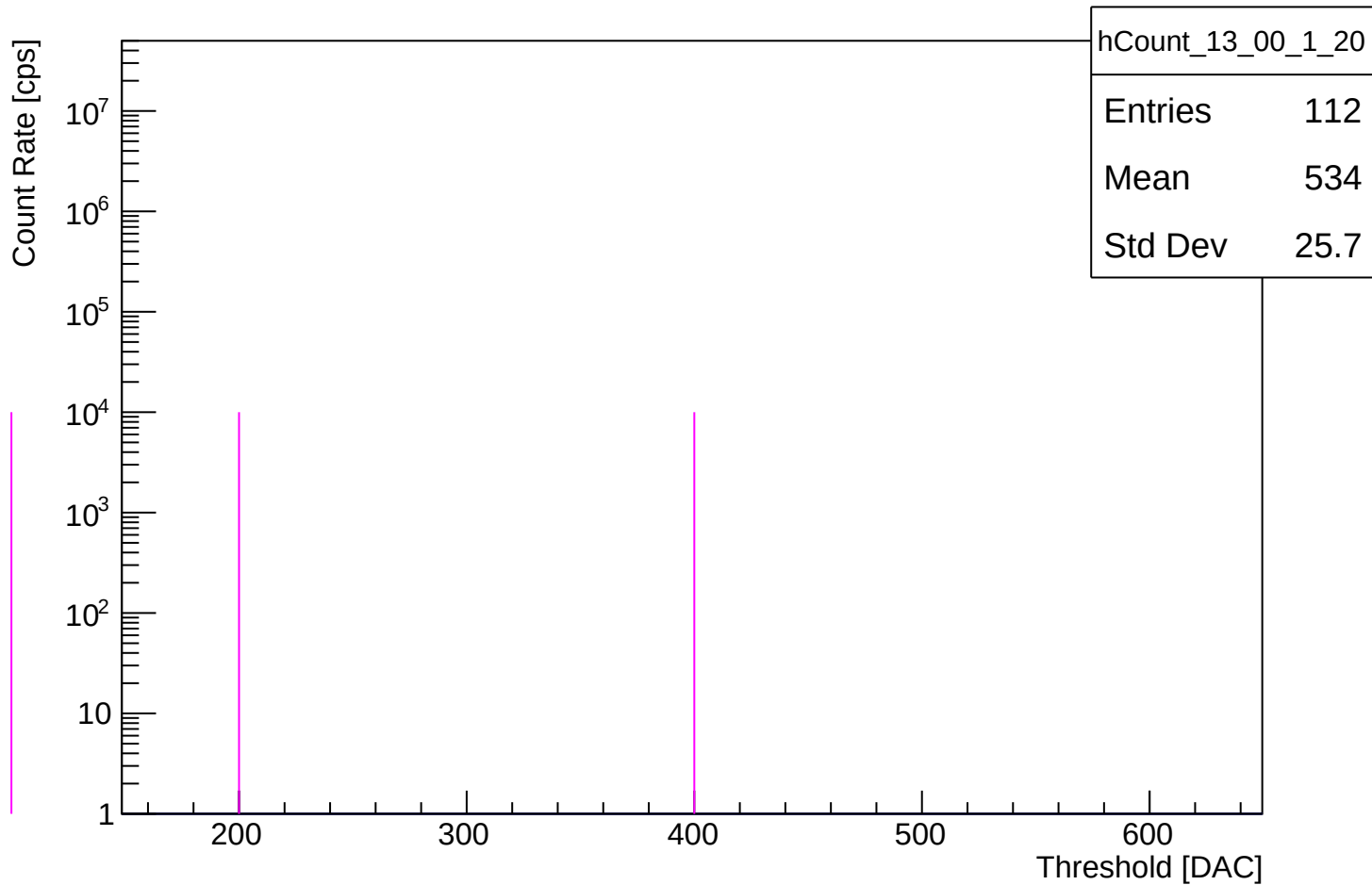
Row 1 Tile 1 Pmt 2 Pixel 18 Slot 13 Fiber 0 Asic 1 Channel 21



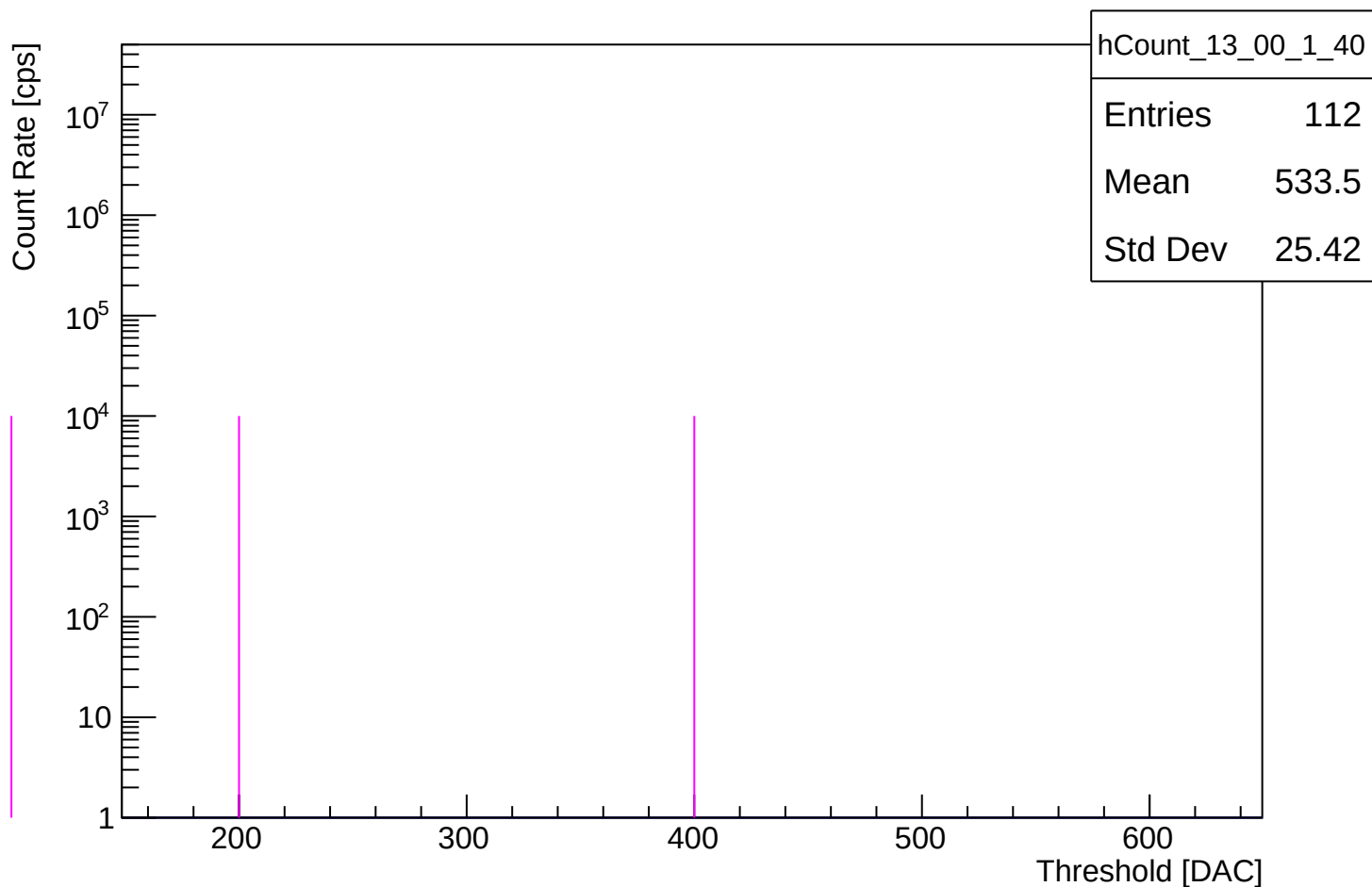
Row 1 Tile 1 Pmt 2 Pixel 19 Slot 13 Fiber 0 Asic 1 Channel 22



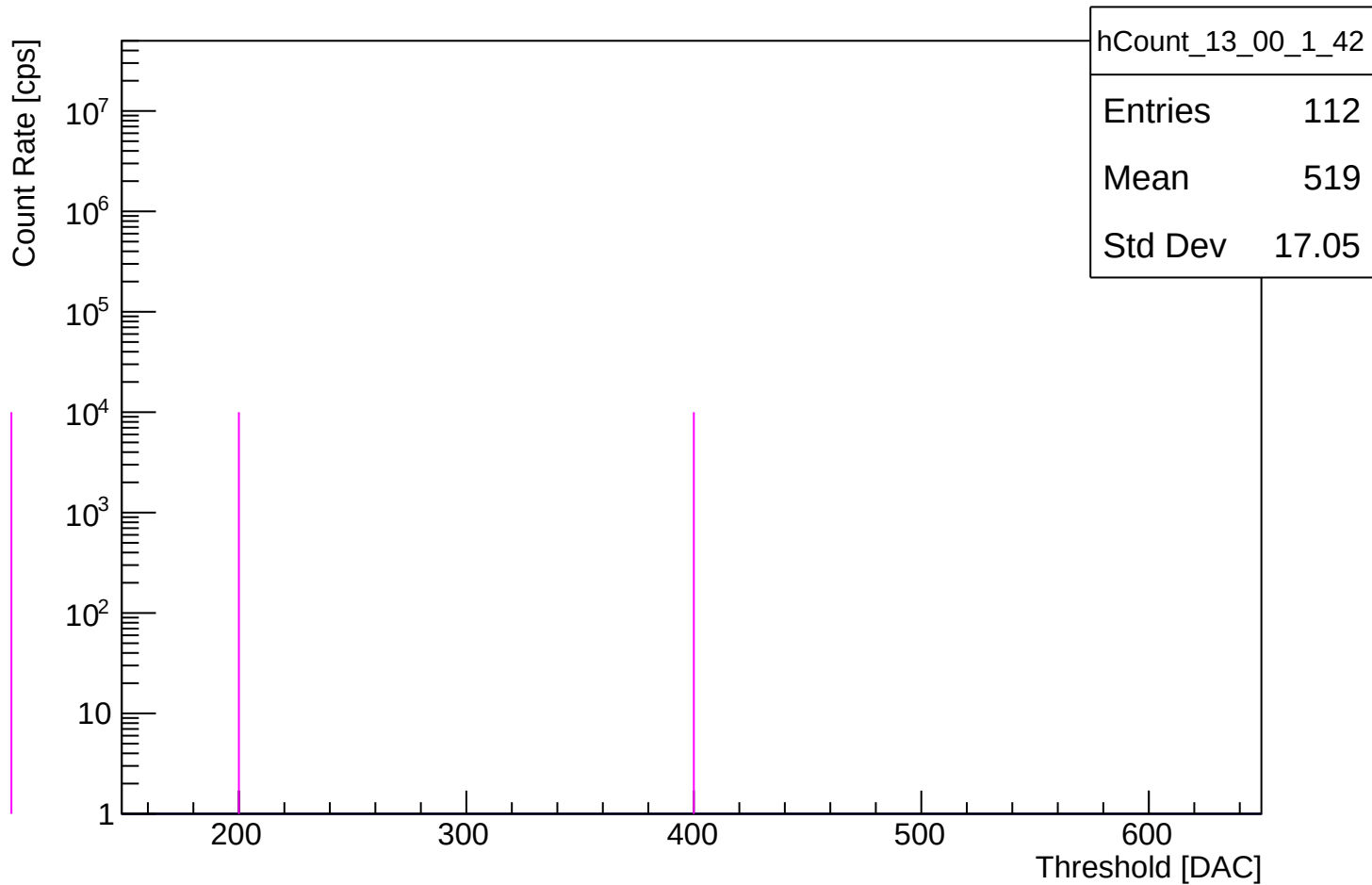
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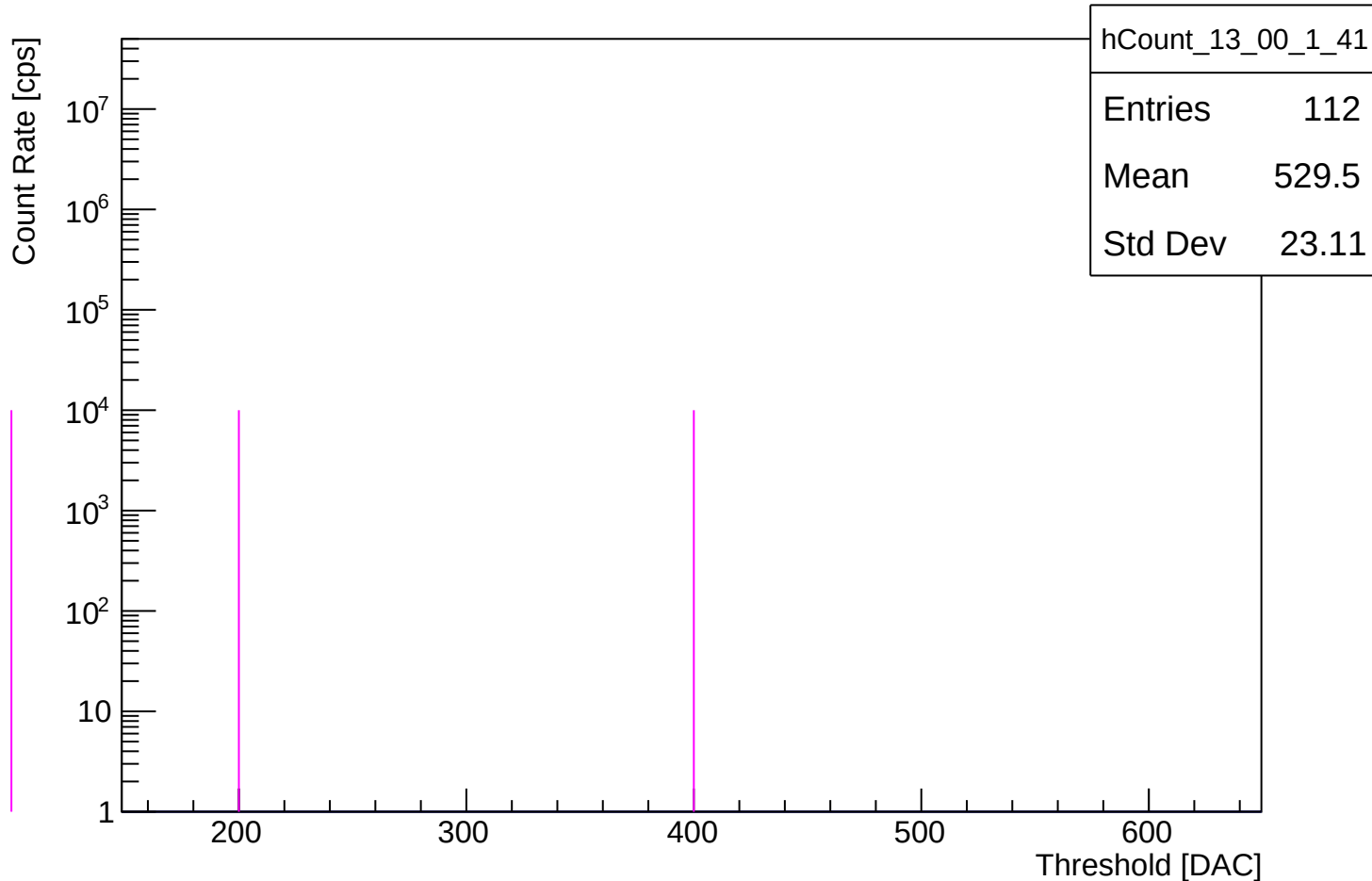
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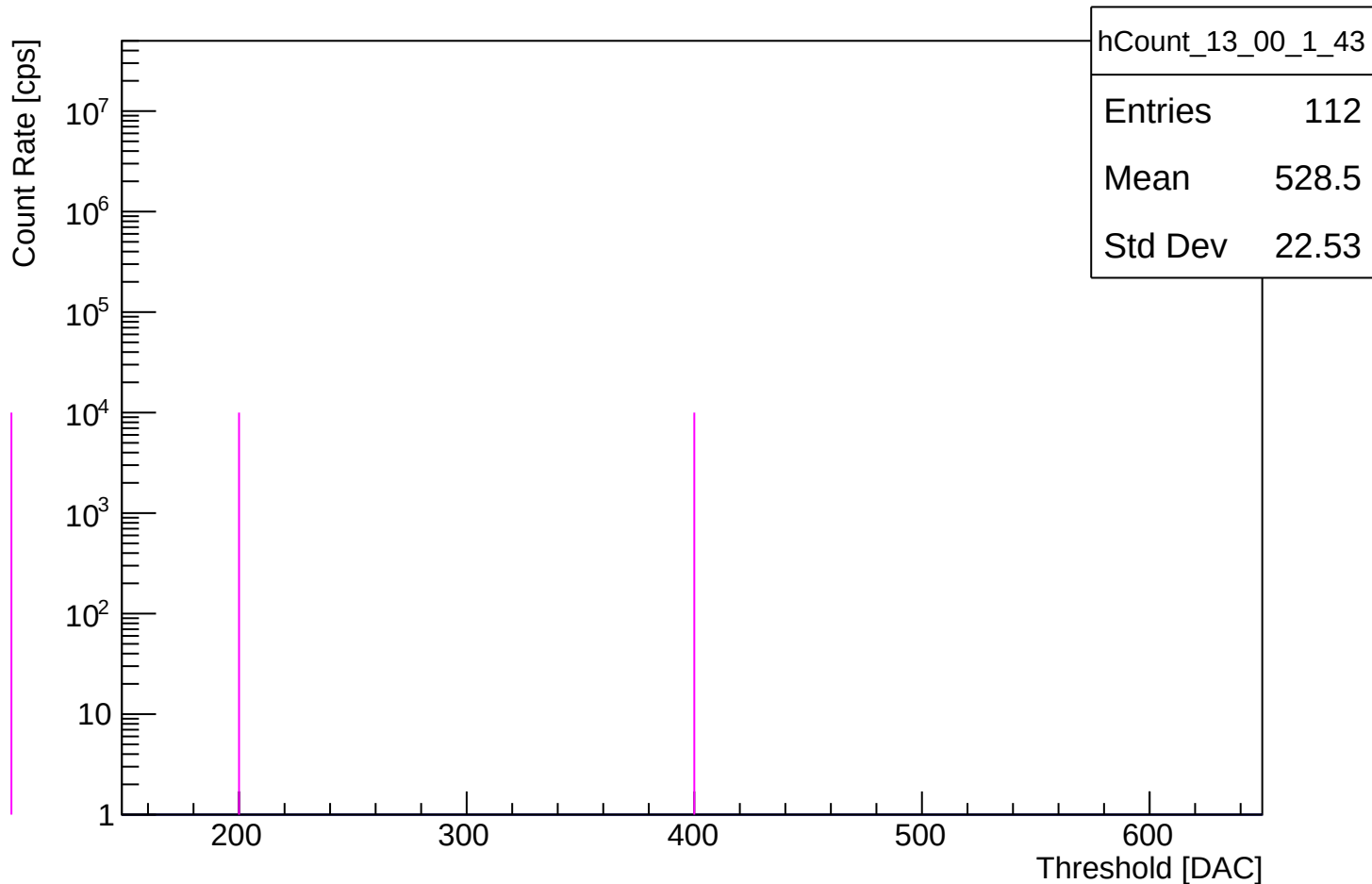
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Row 1 Tile 1 Pmt 2 Pixel 23 Slot 13 Fiber 0 Asic 1 Channel 41

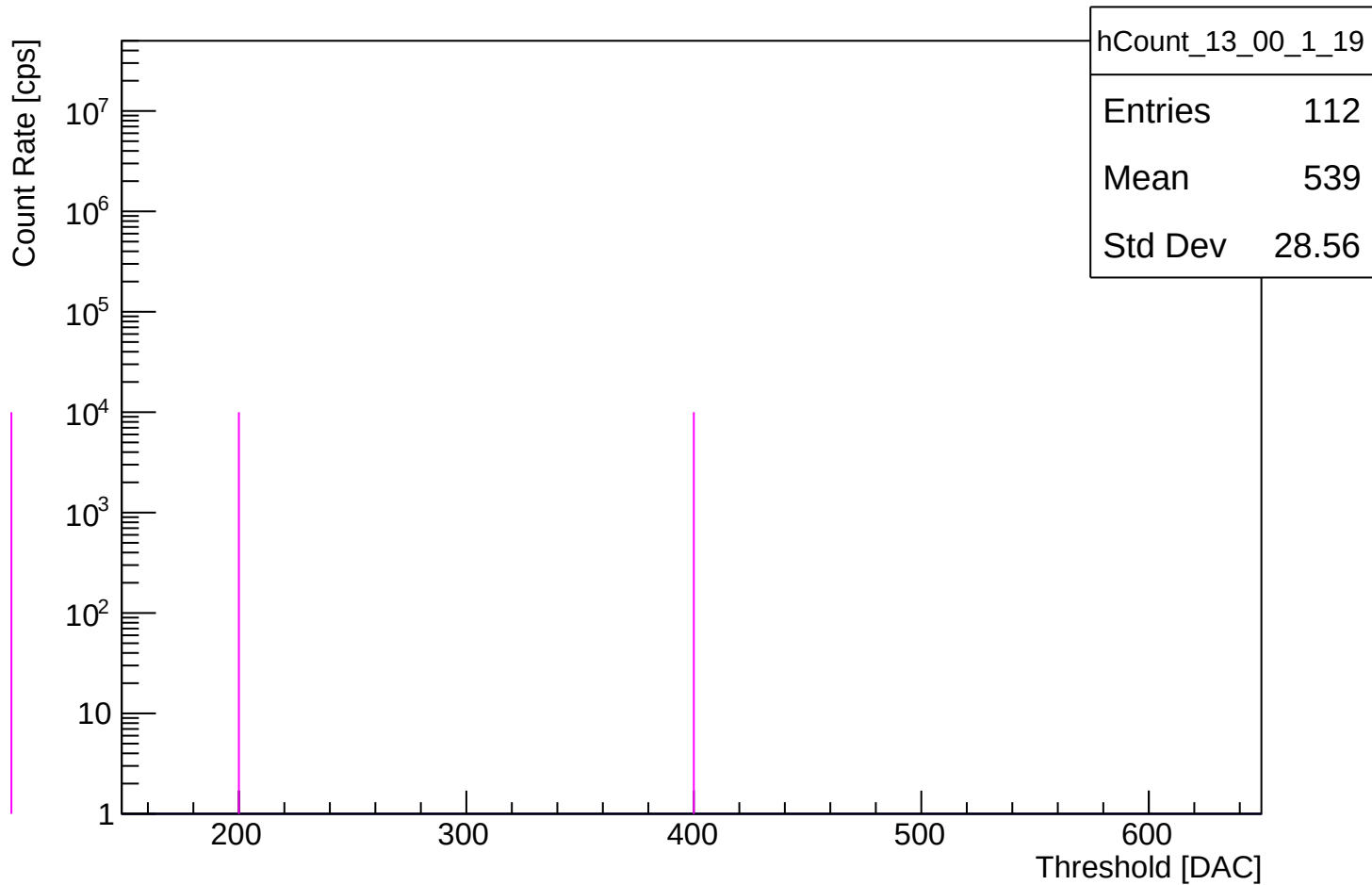


Row 1 Tile 1 Pmt 2 Pixel 24 Slot 13 Fiber 0 Asic 1 Channel 43

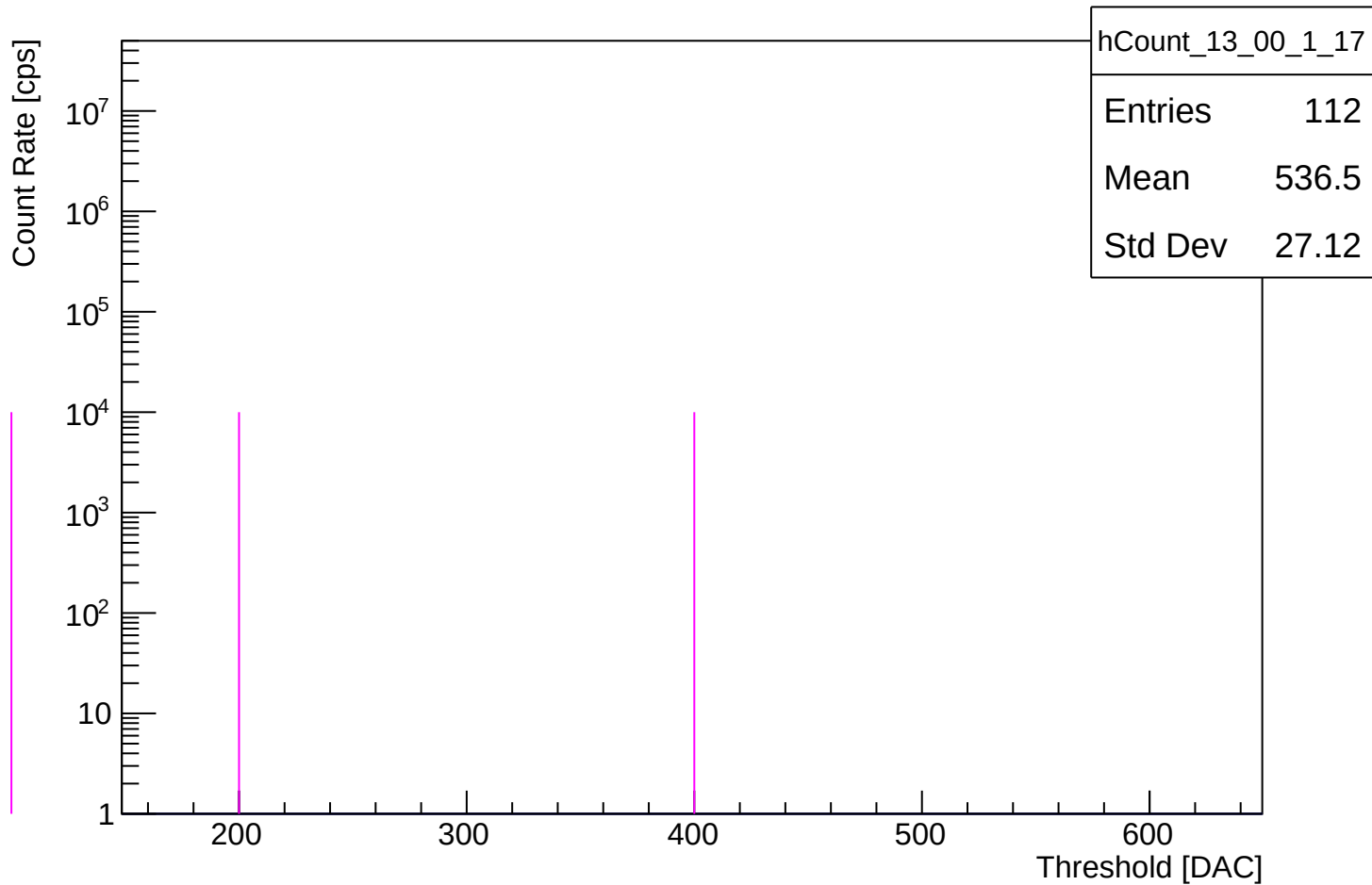




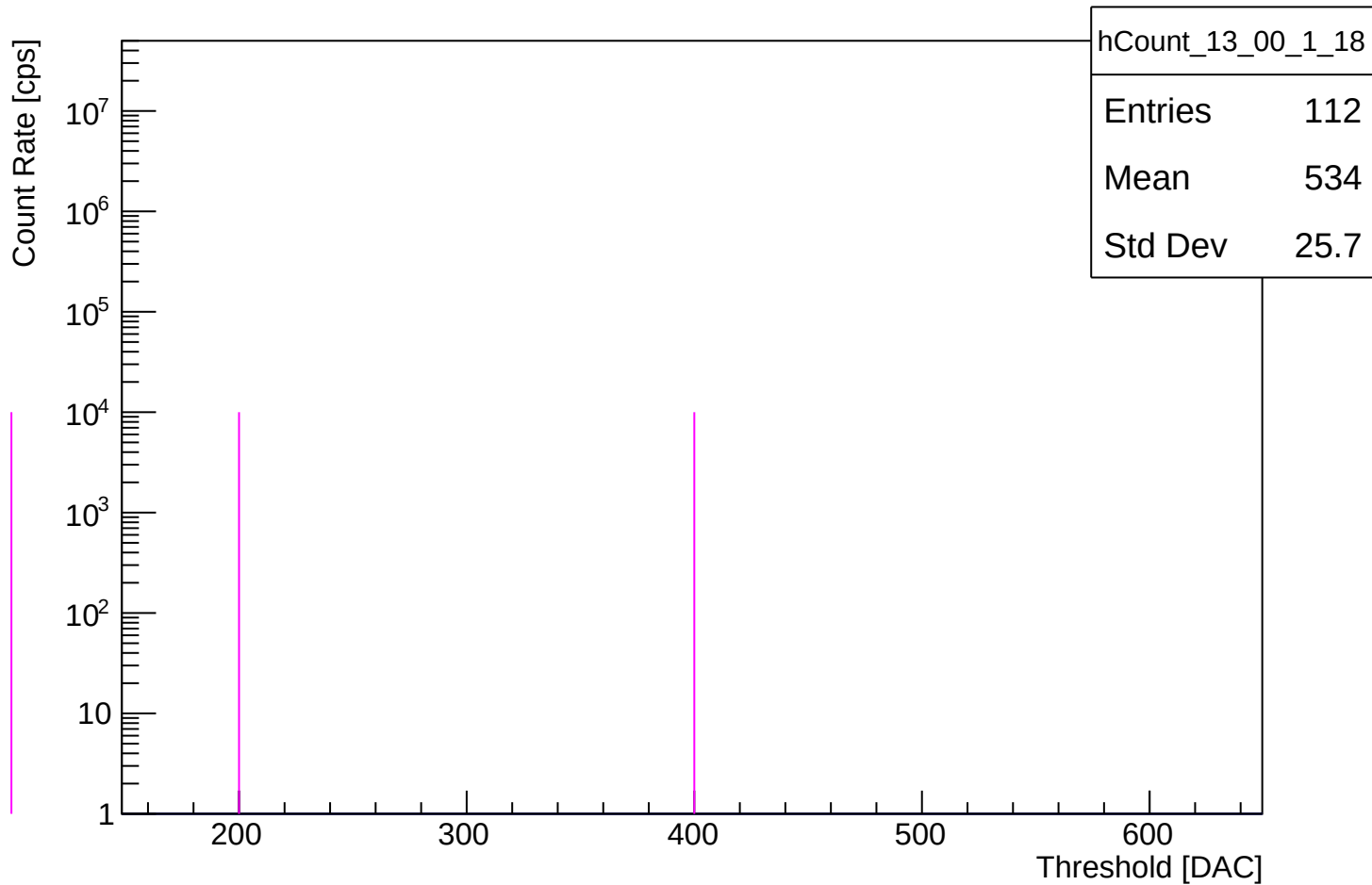
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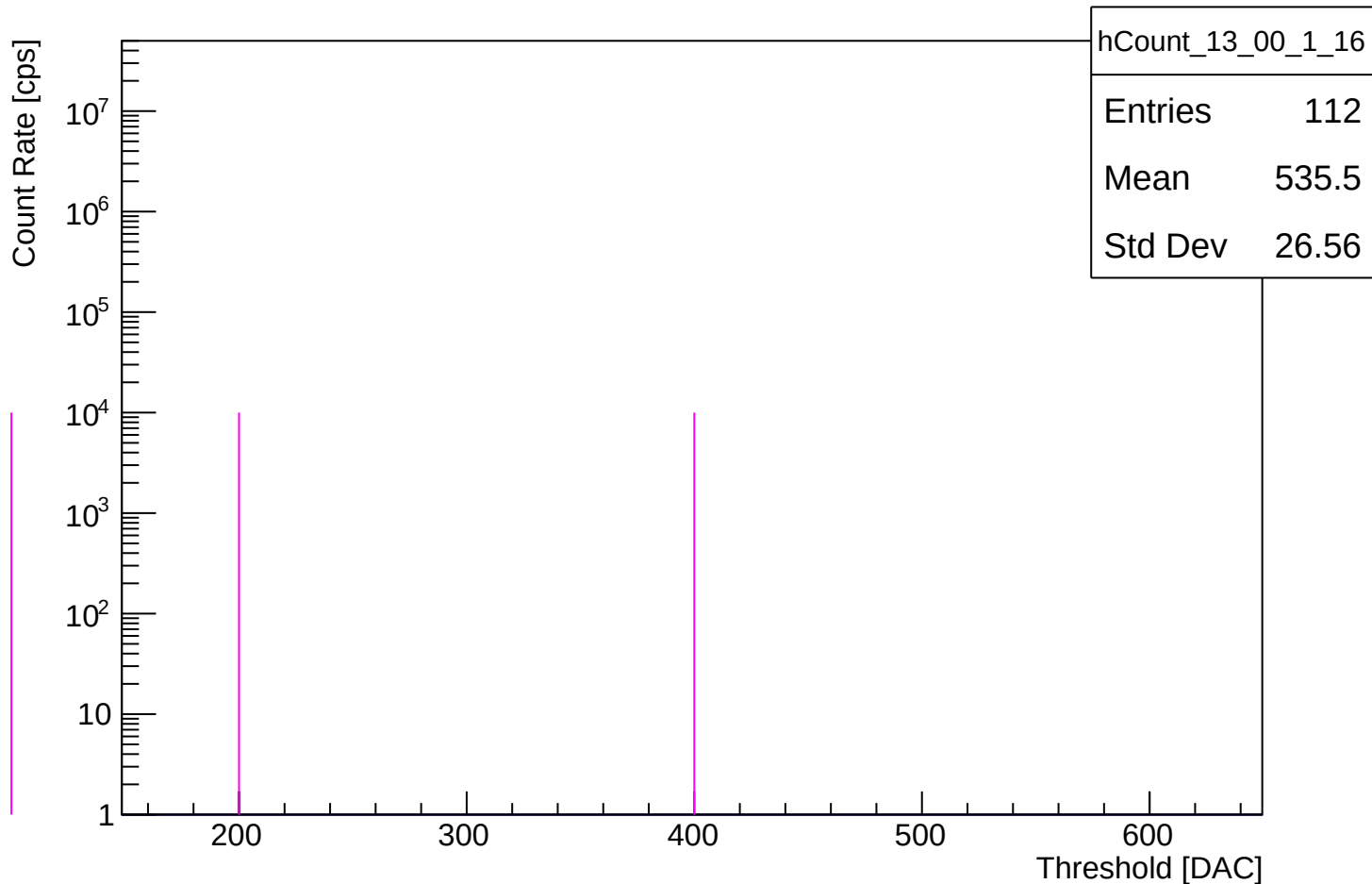
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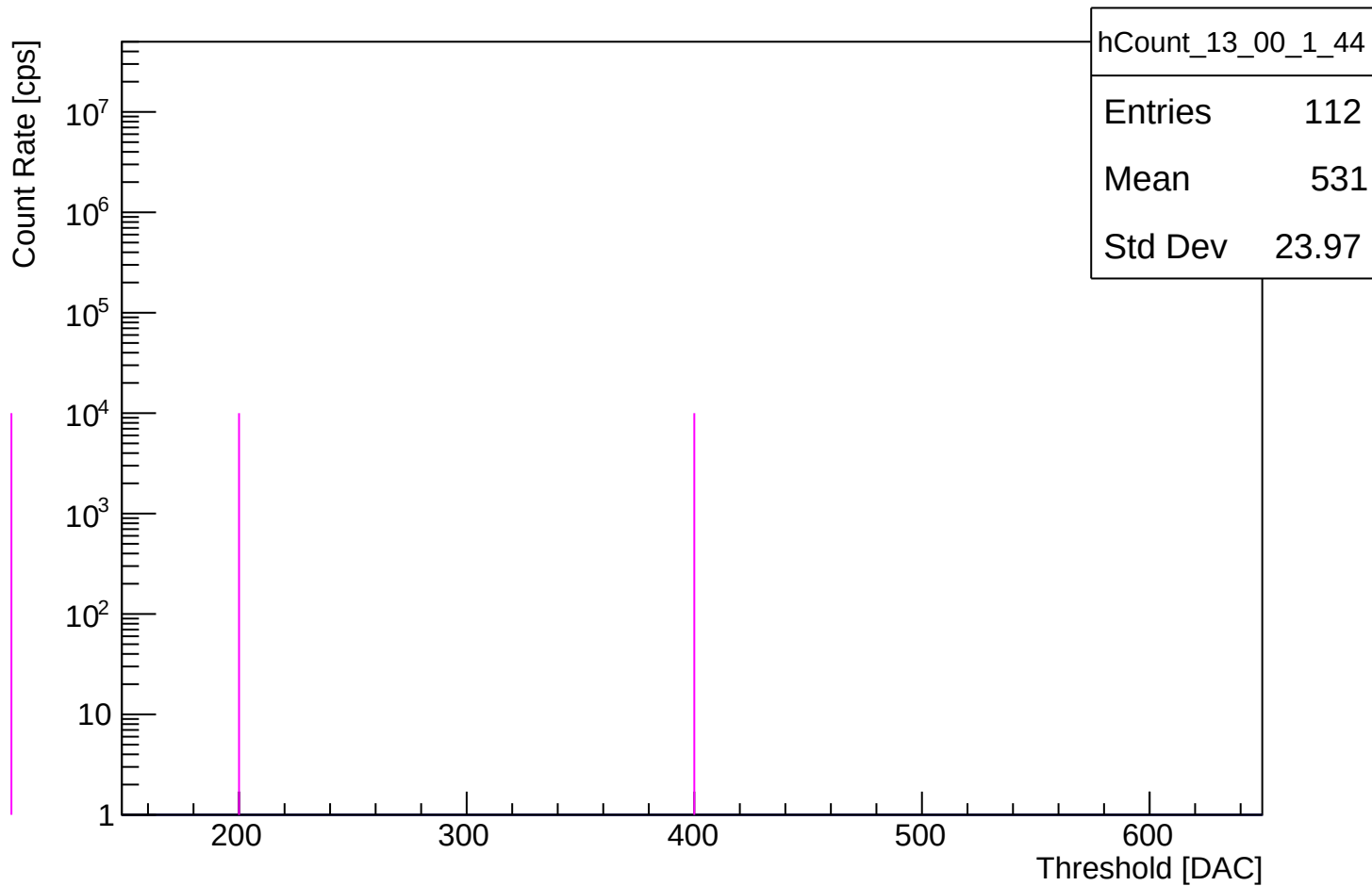
Row 1 Tile 1 Pmt 2 Pixel 27 Slot 13 Fiber 0 Asic 1 Channel 18



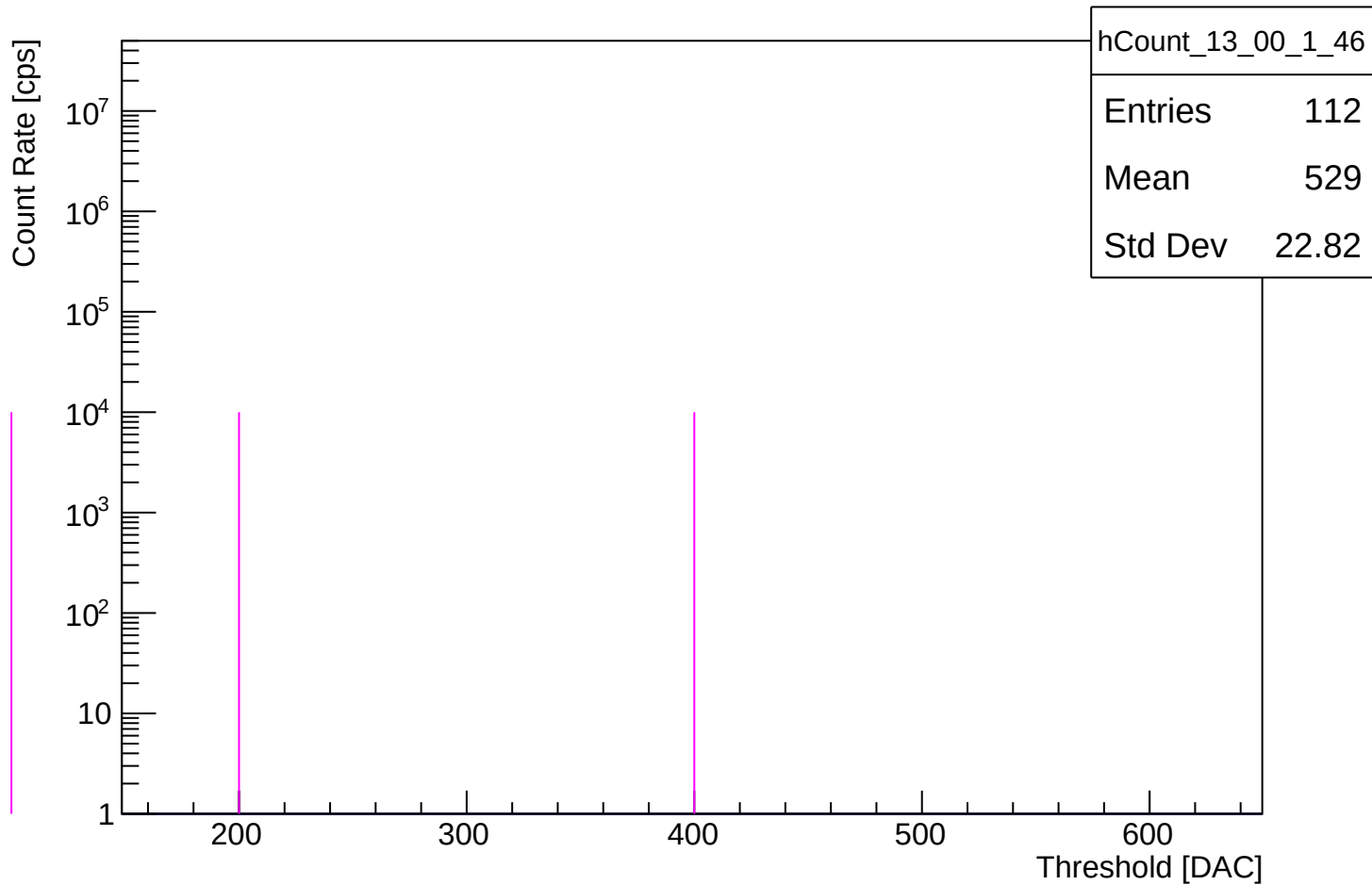
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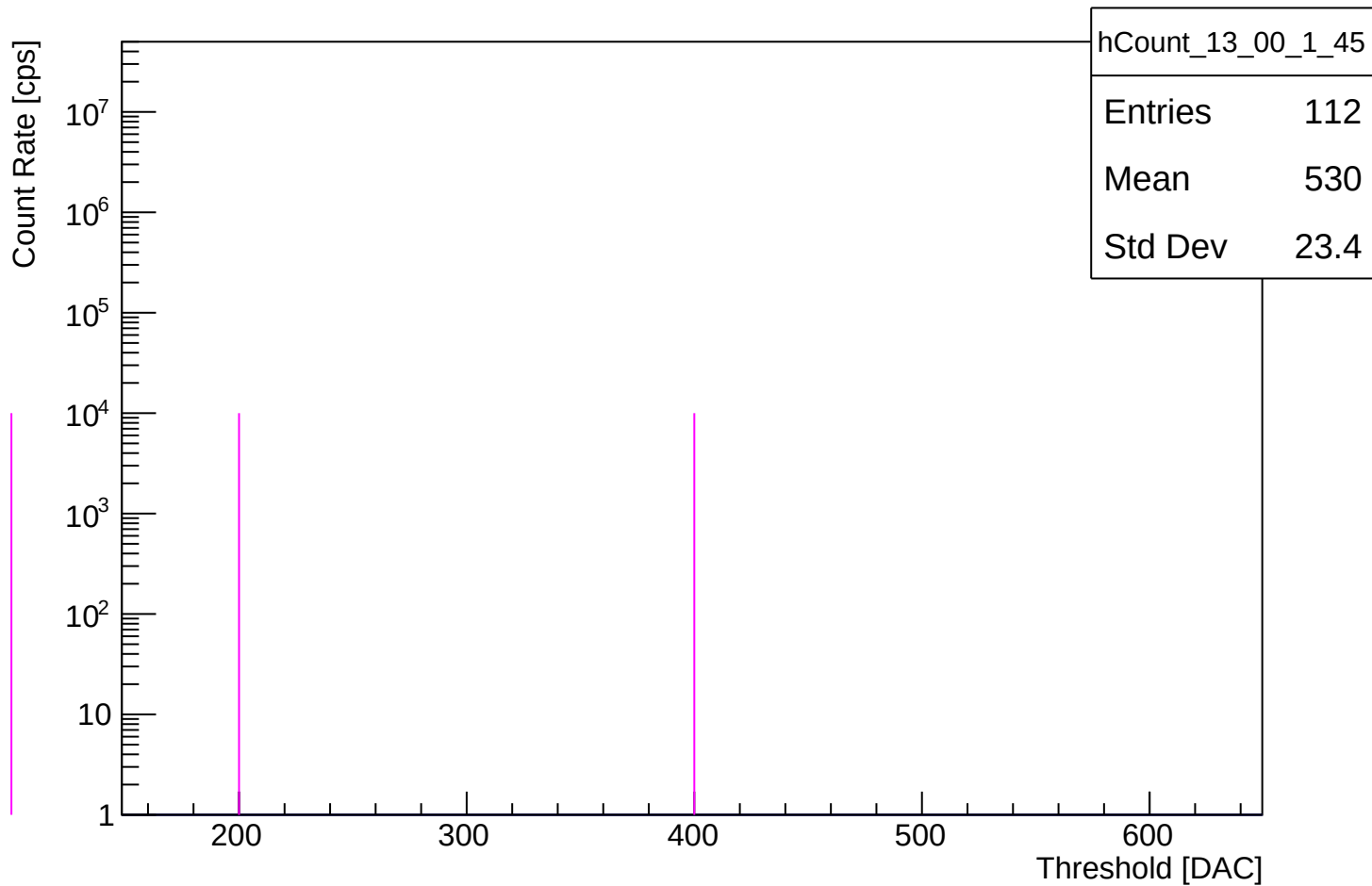
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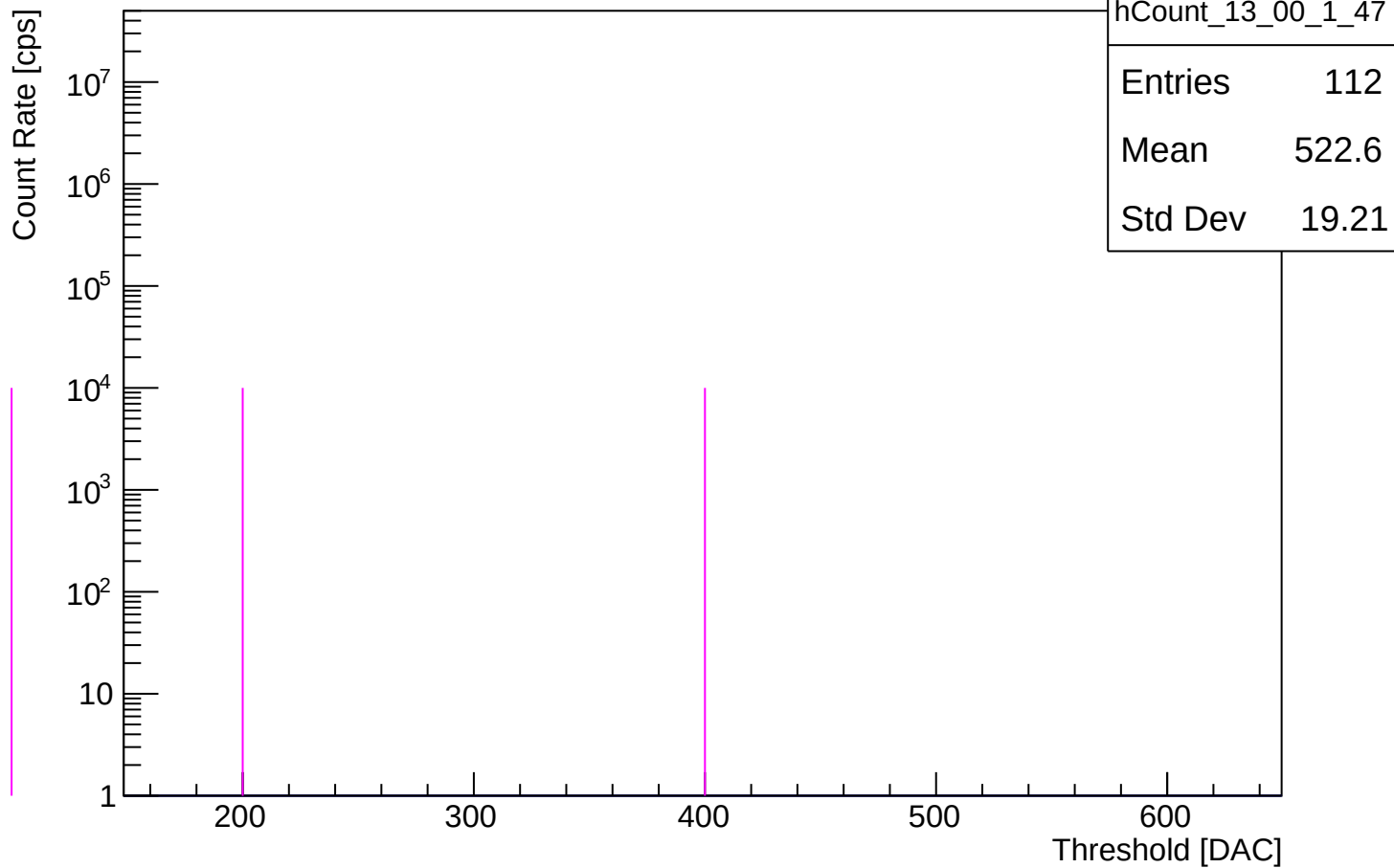
Row 1 Tile 1 Pmt 2 Pixel 30 Slot 13 Fiber 0 Asic 1 Channel 46



Row 1 Tile 1 Pmt 2 Pixel 31 Slot 13 Fiber 0 Asic 1 Channel 45

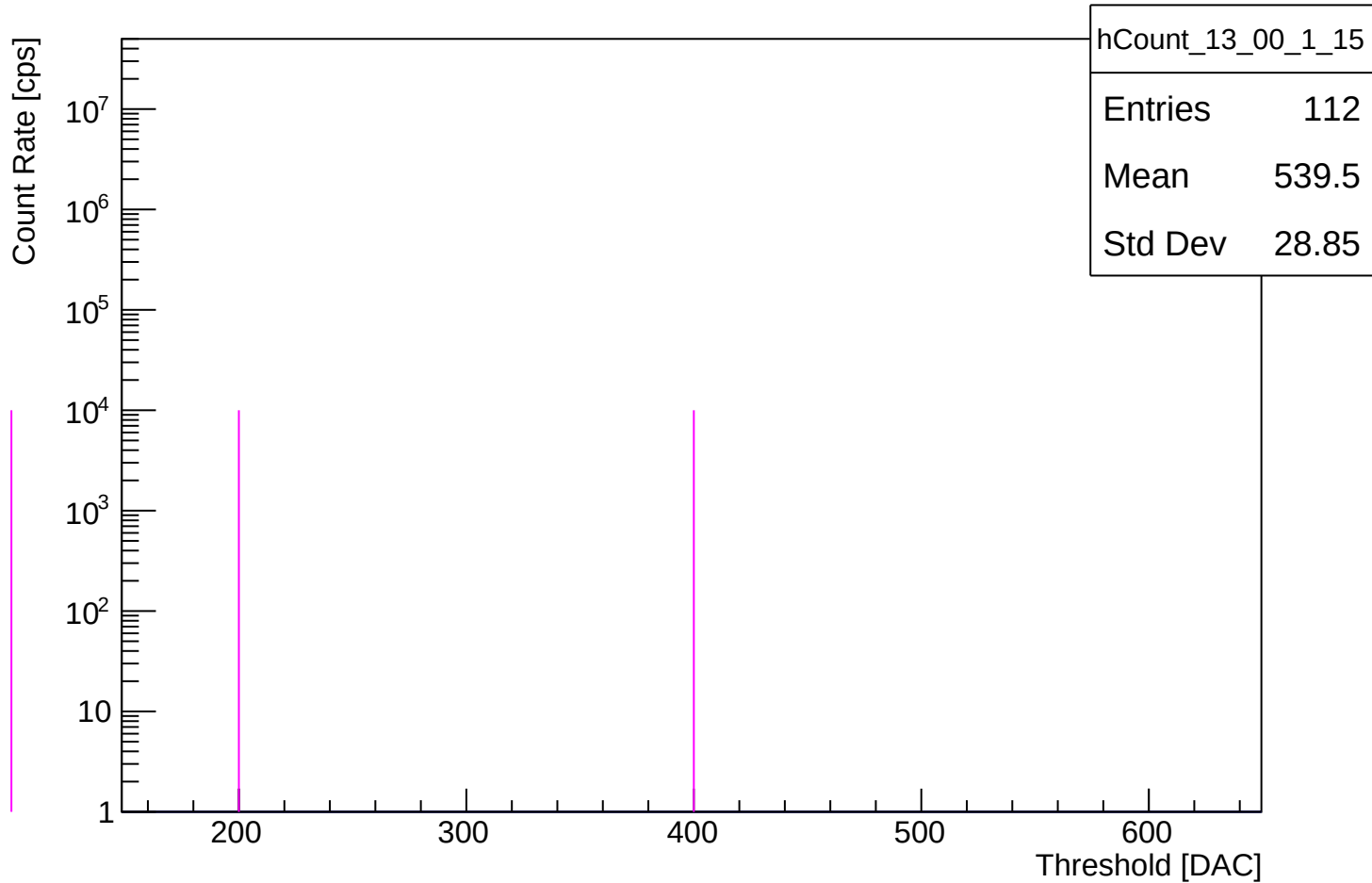


Row 1 Tile 1 Pmt 2 Pixel 32 Slot 13 Fiber 0 Asic 1 Channel 47

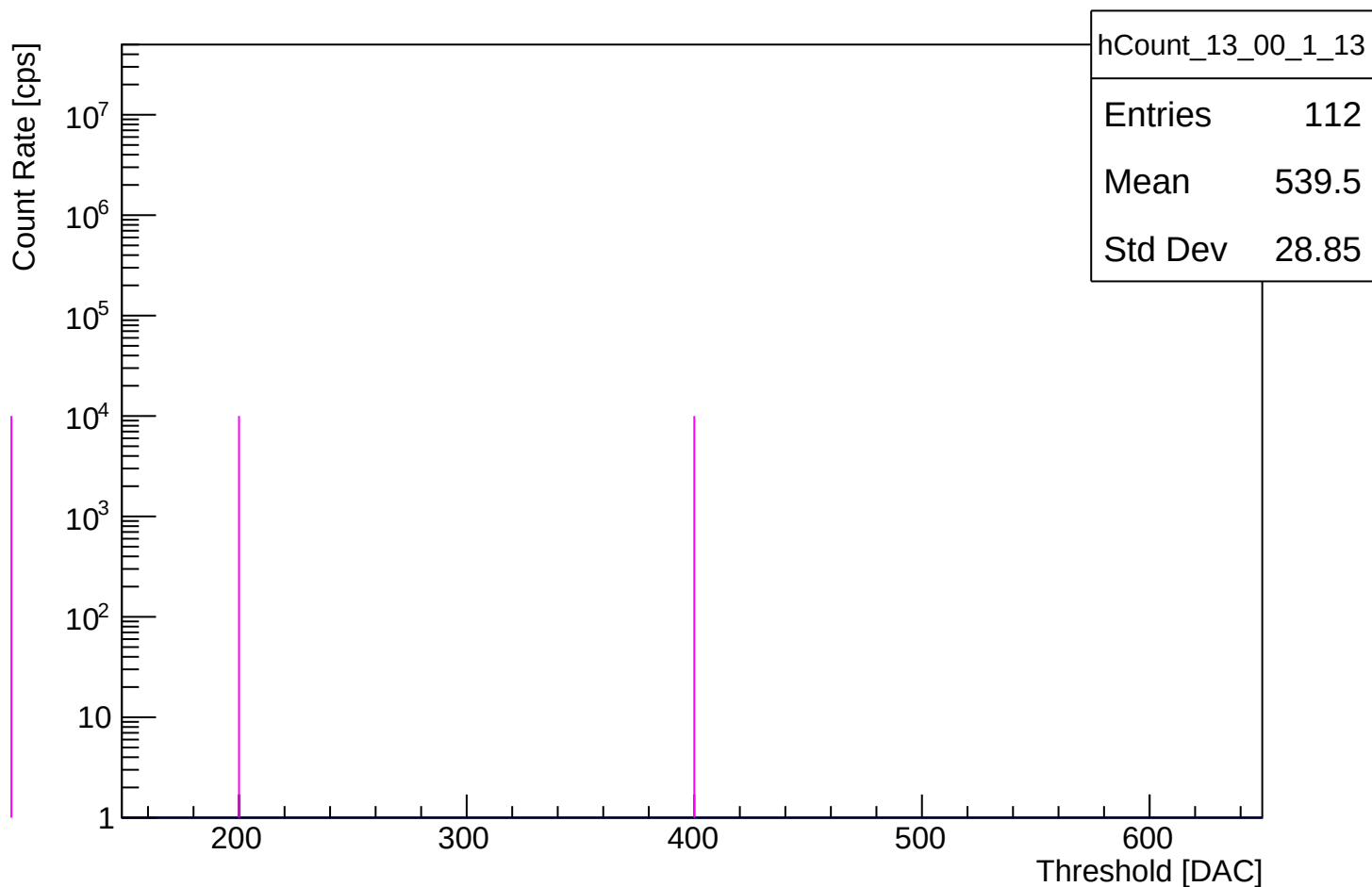




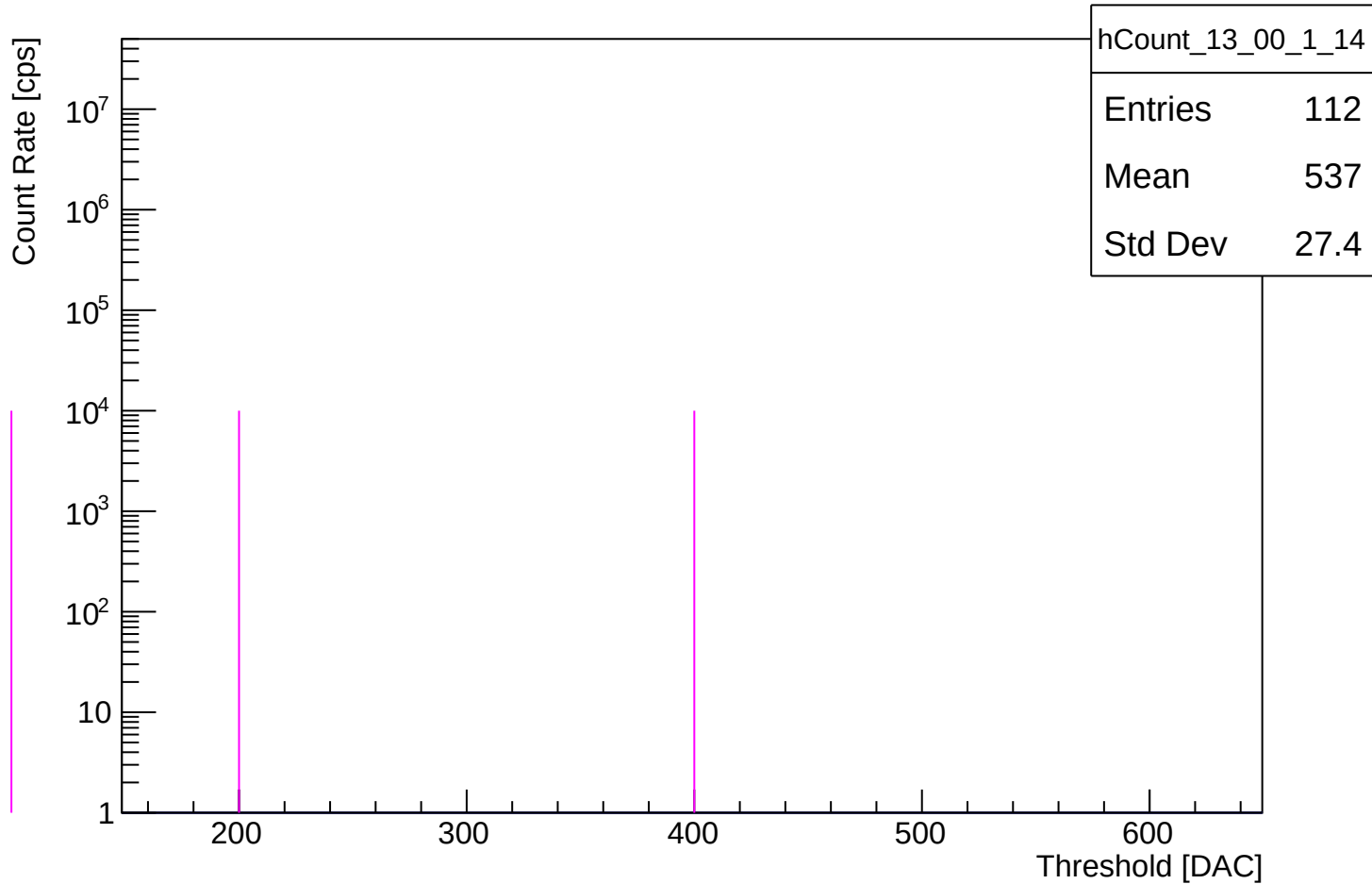
Row 1 Tile 1 Pmt 2 Pixel 33 Slot 13 Fiber 0 Asic 1 Channel 15



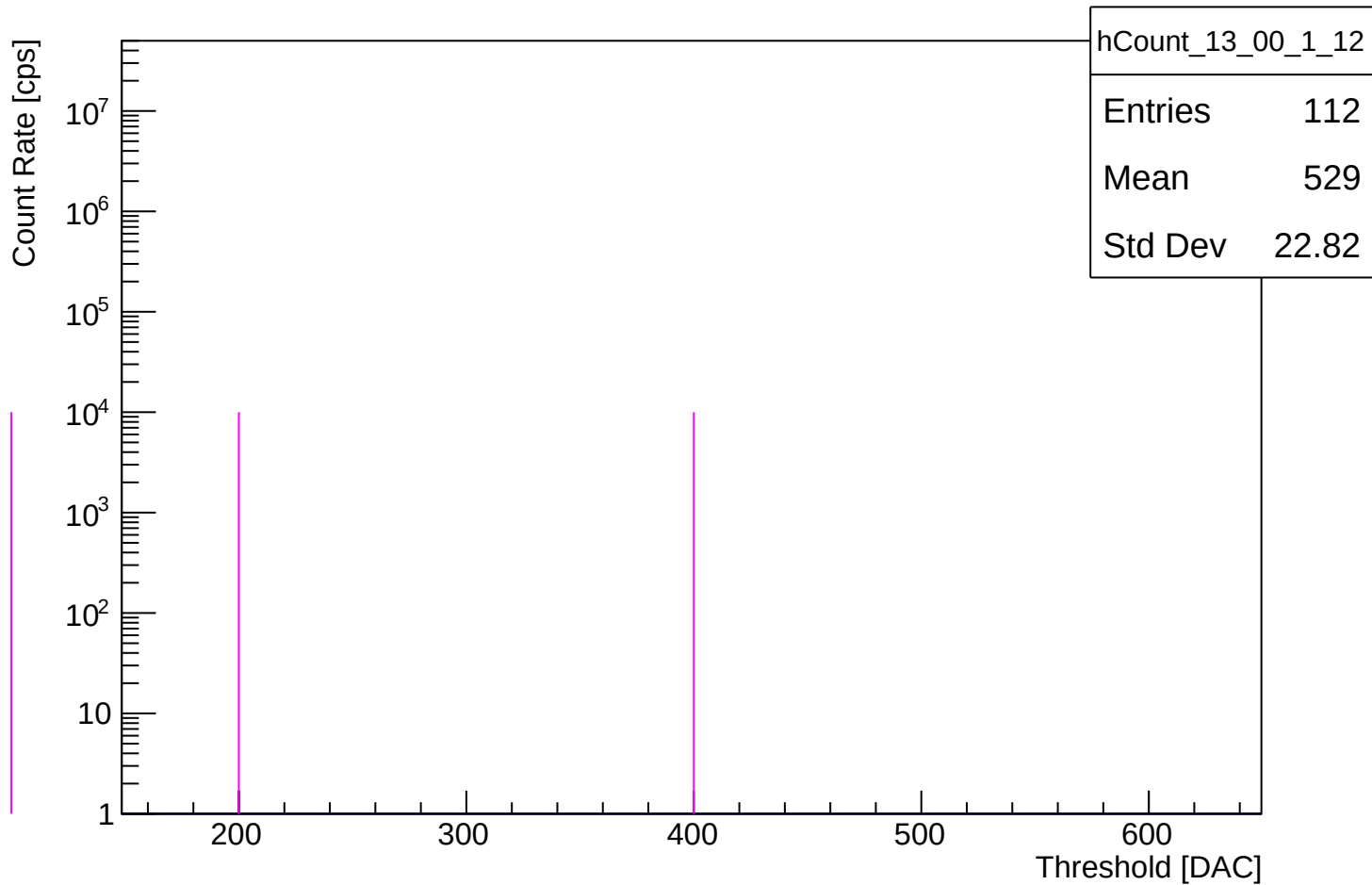
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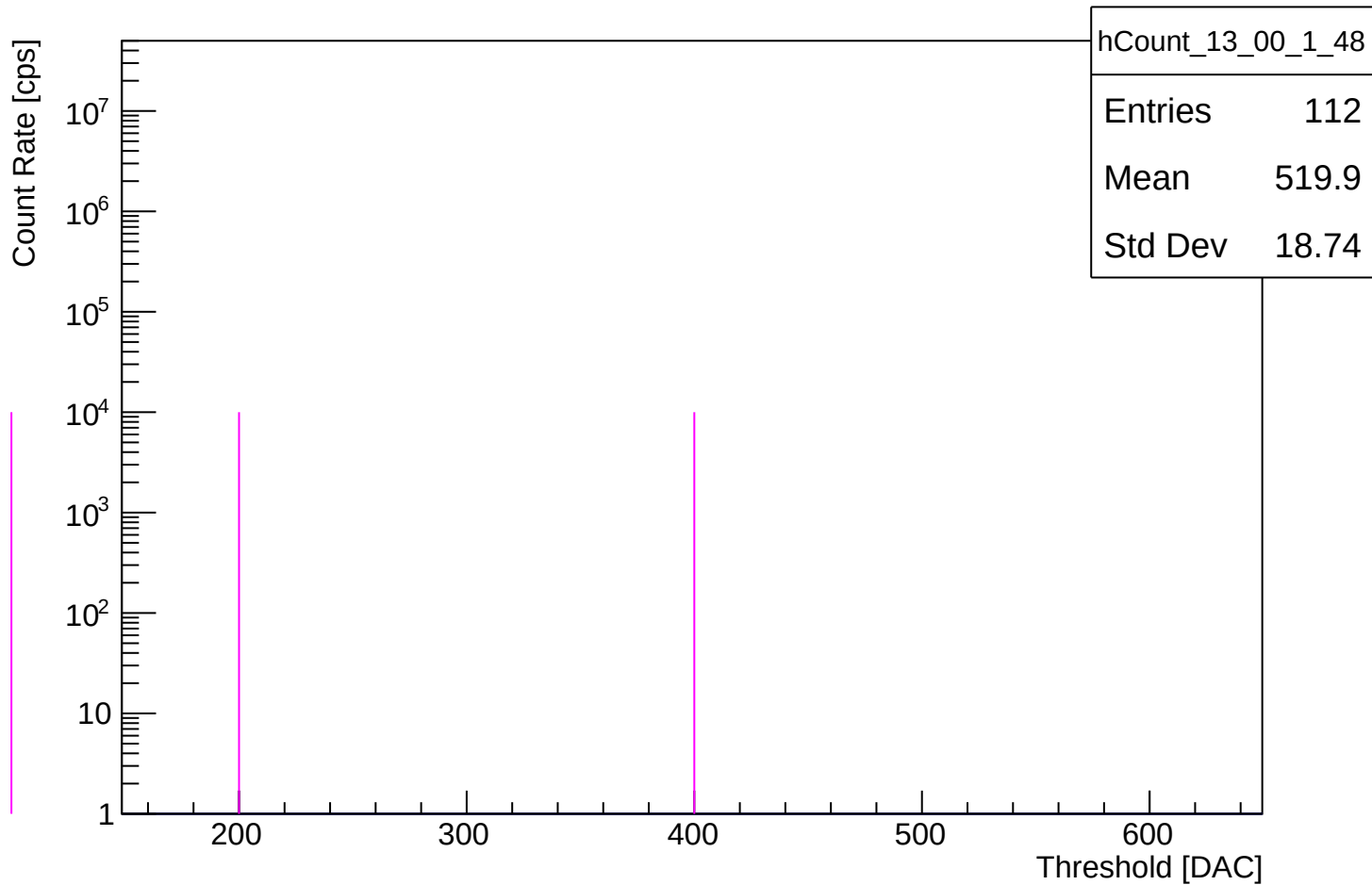
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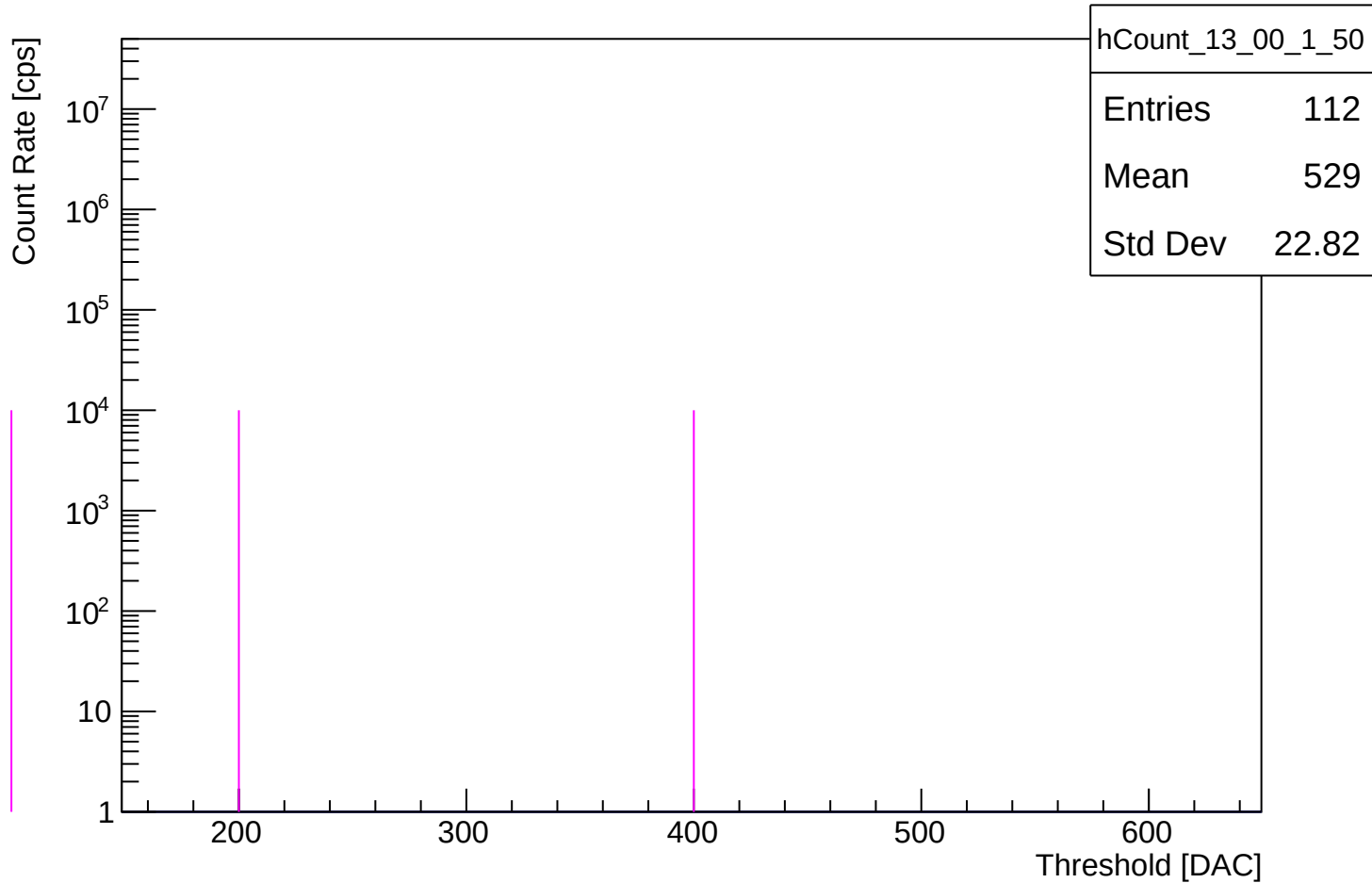
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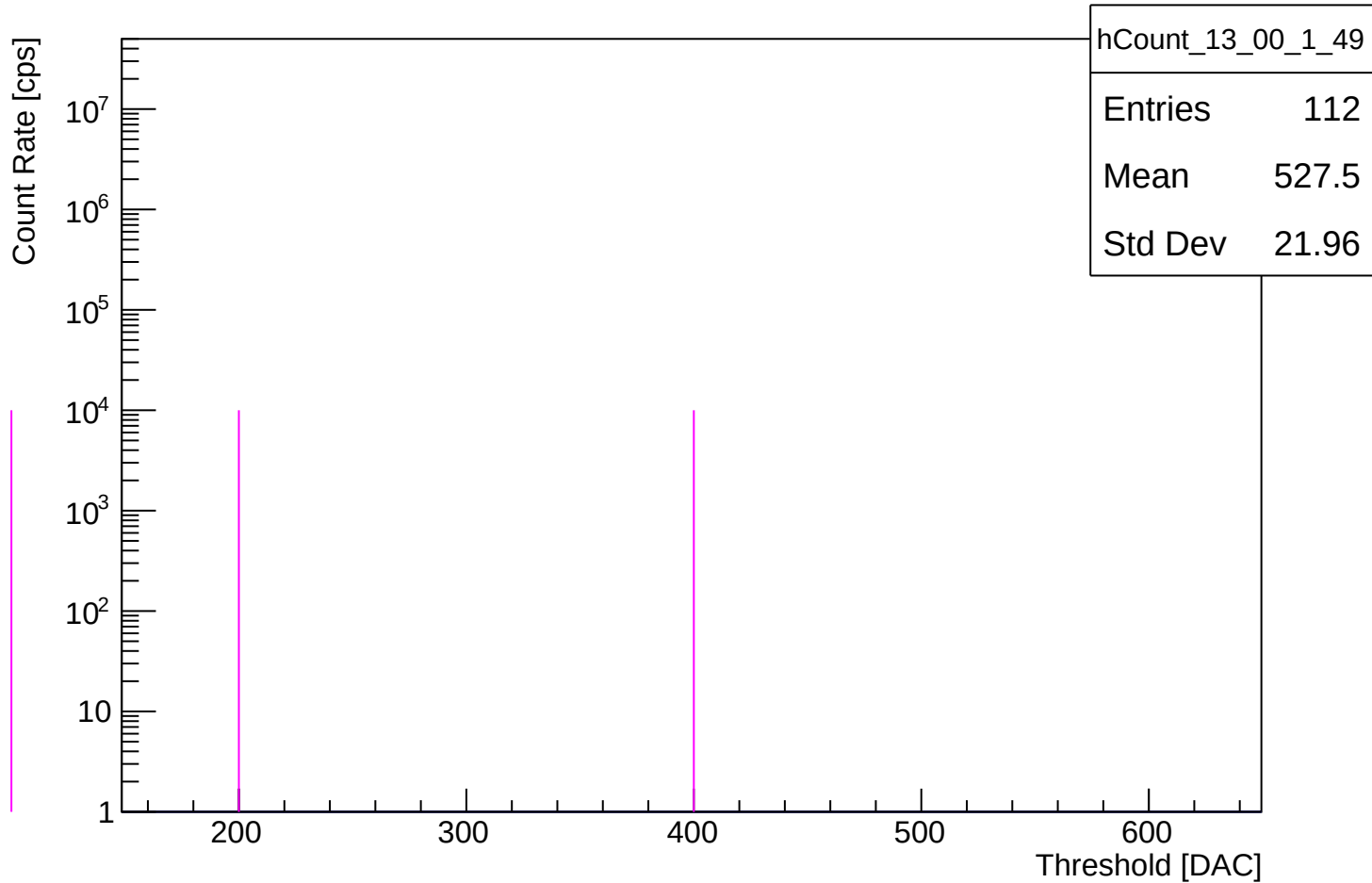
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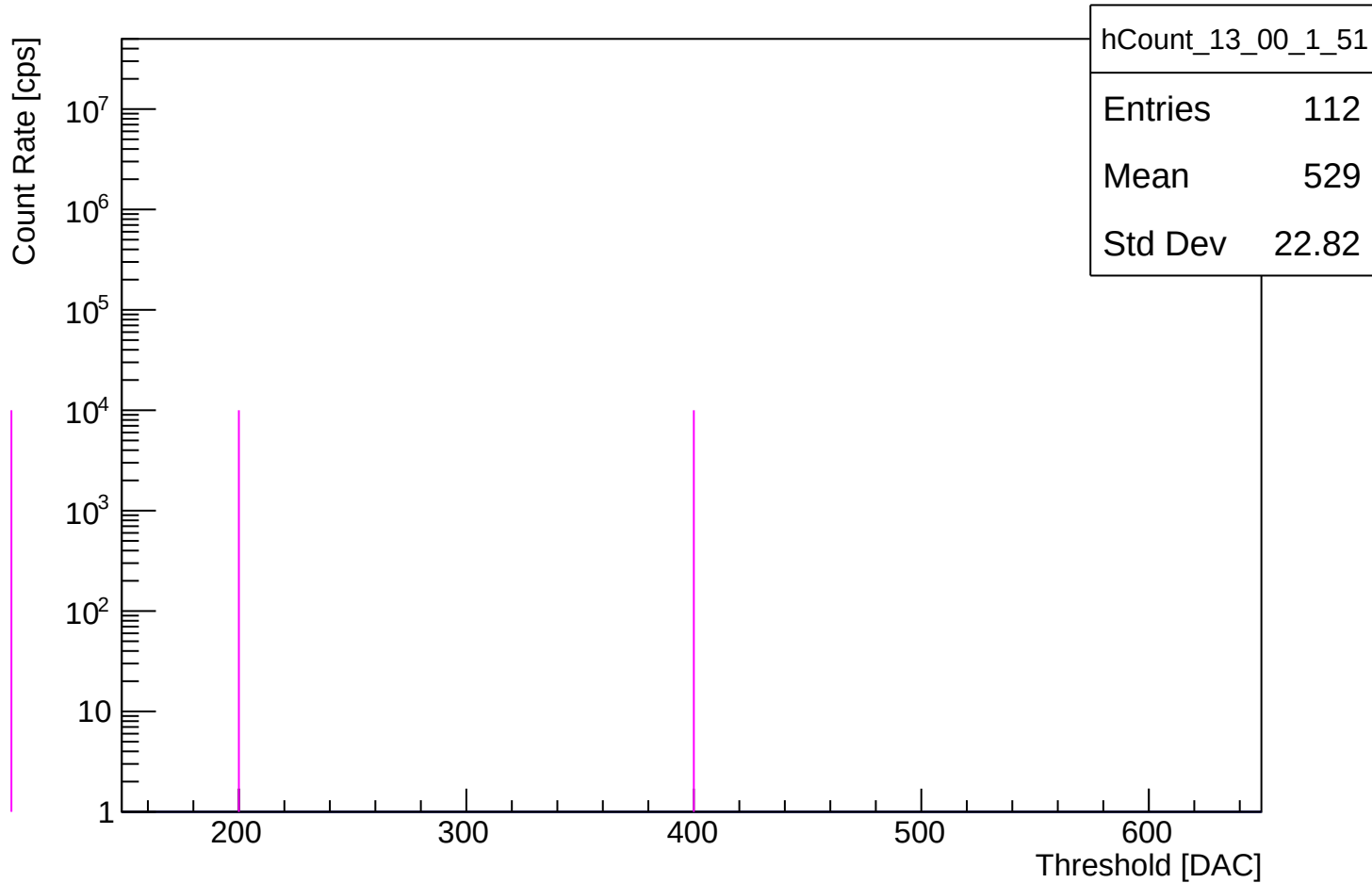
Row 1 Tile 1 Pmt 2 Pixel 38 Slot 13 Fiber 0 Asic 1 Channel 50



Row 1 Tile 1 Pmt 2 Pixel 39 Slot 13 Fiber 0 Asic 1 Channel 49

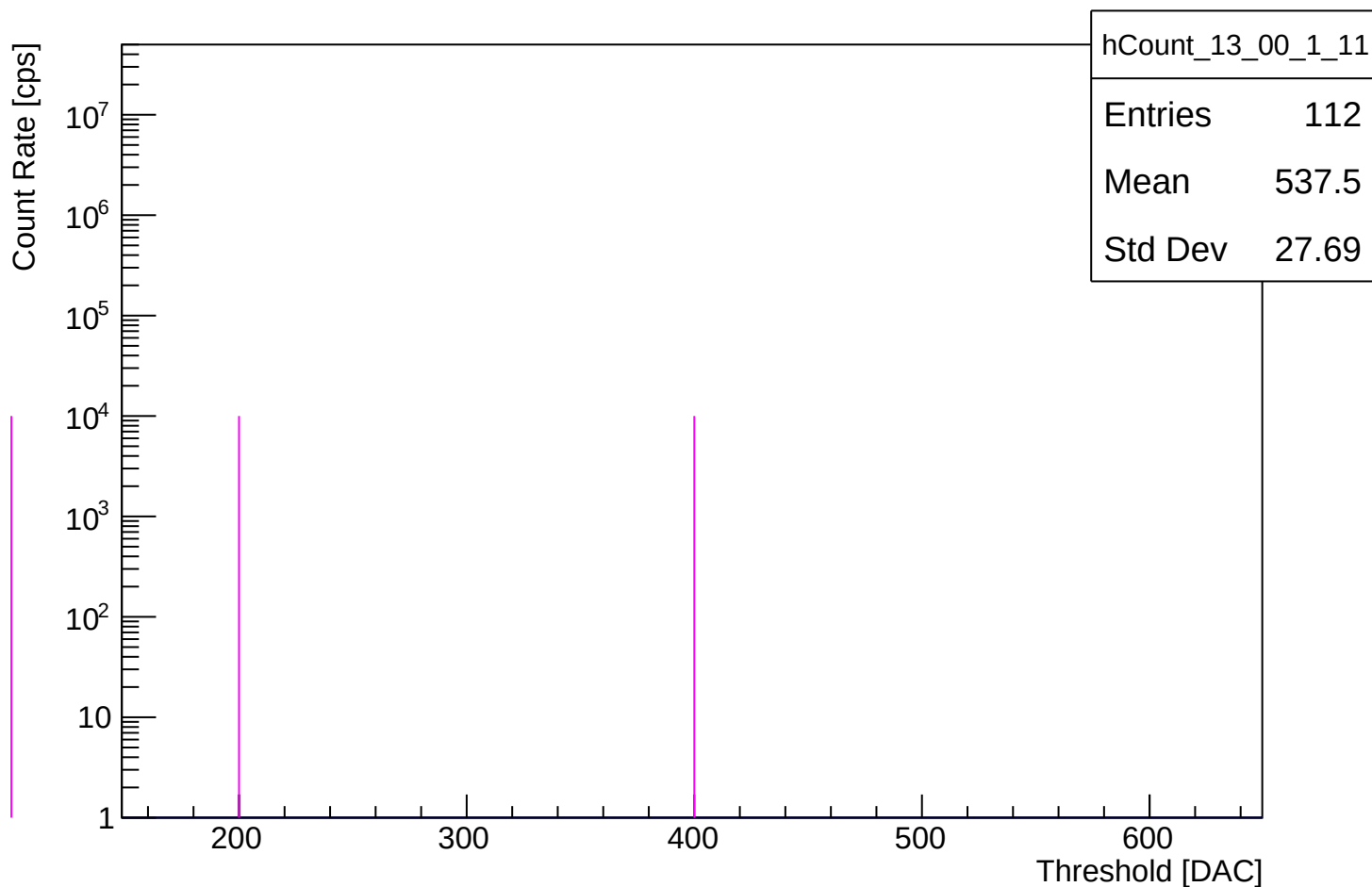


Row 1 Tile 1 Pmt 2 Pixel 40 Slot 13 Fiber 0 Asic 1 Channel 51

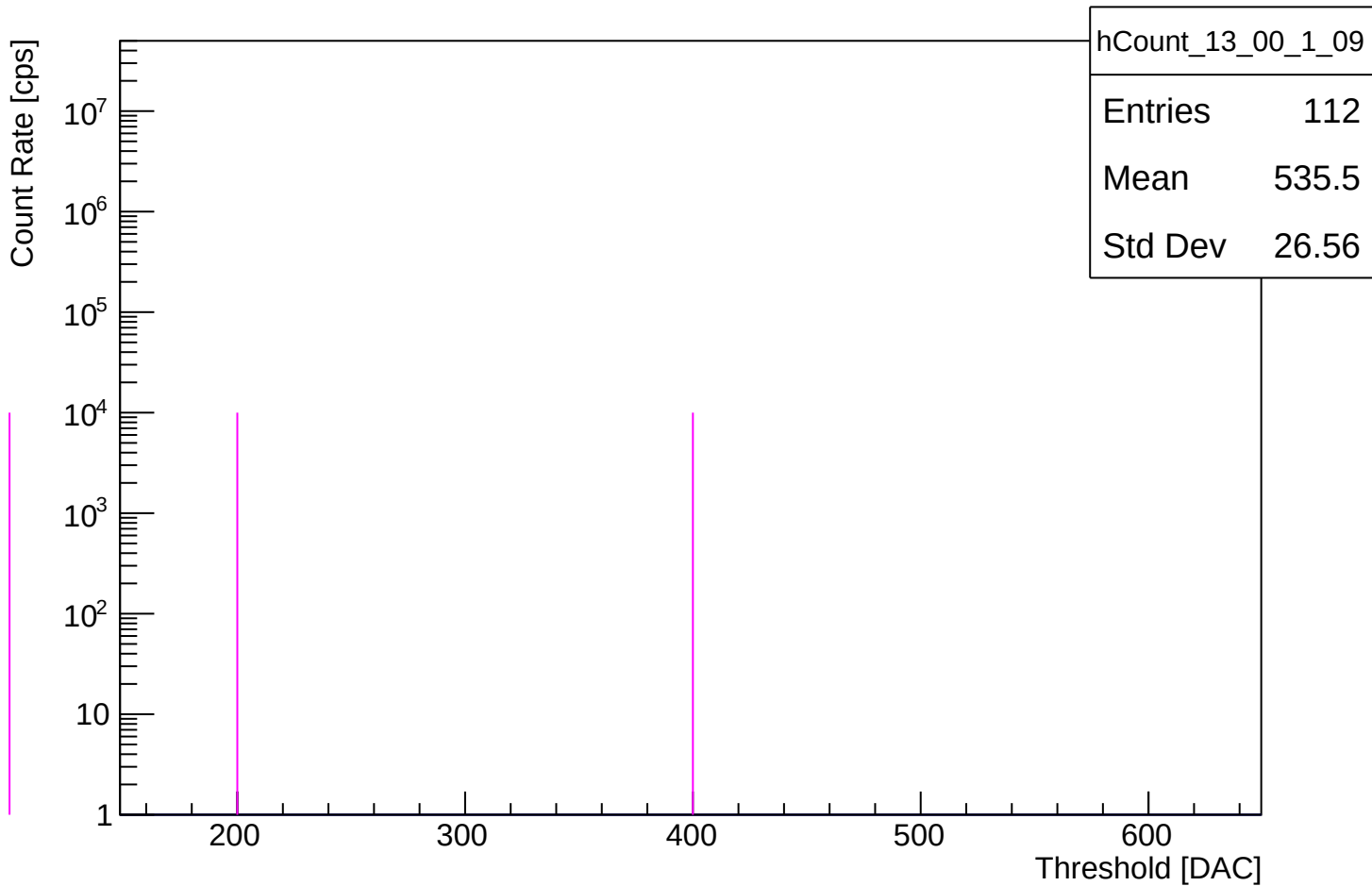




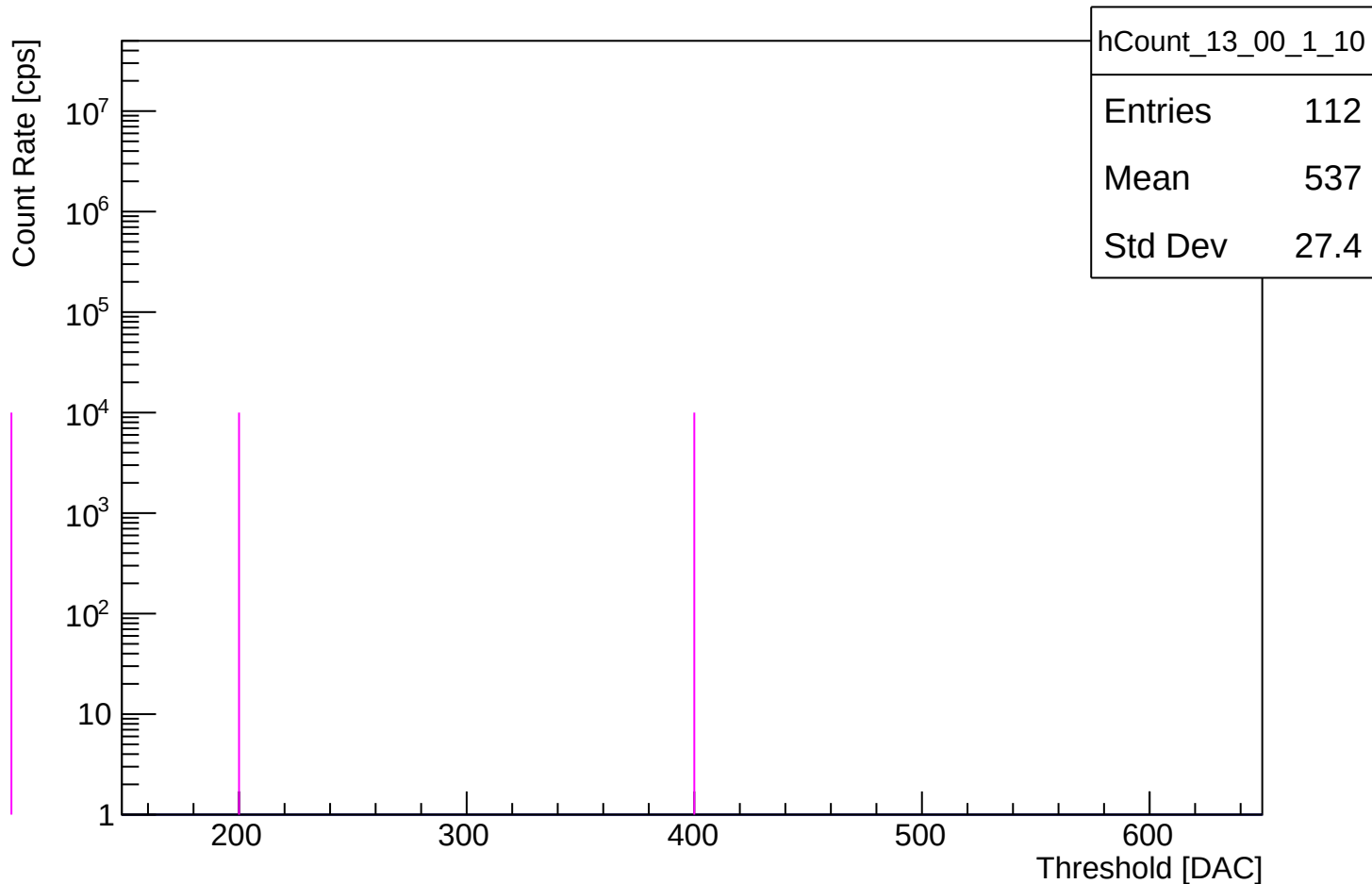
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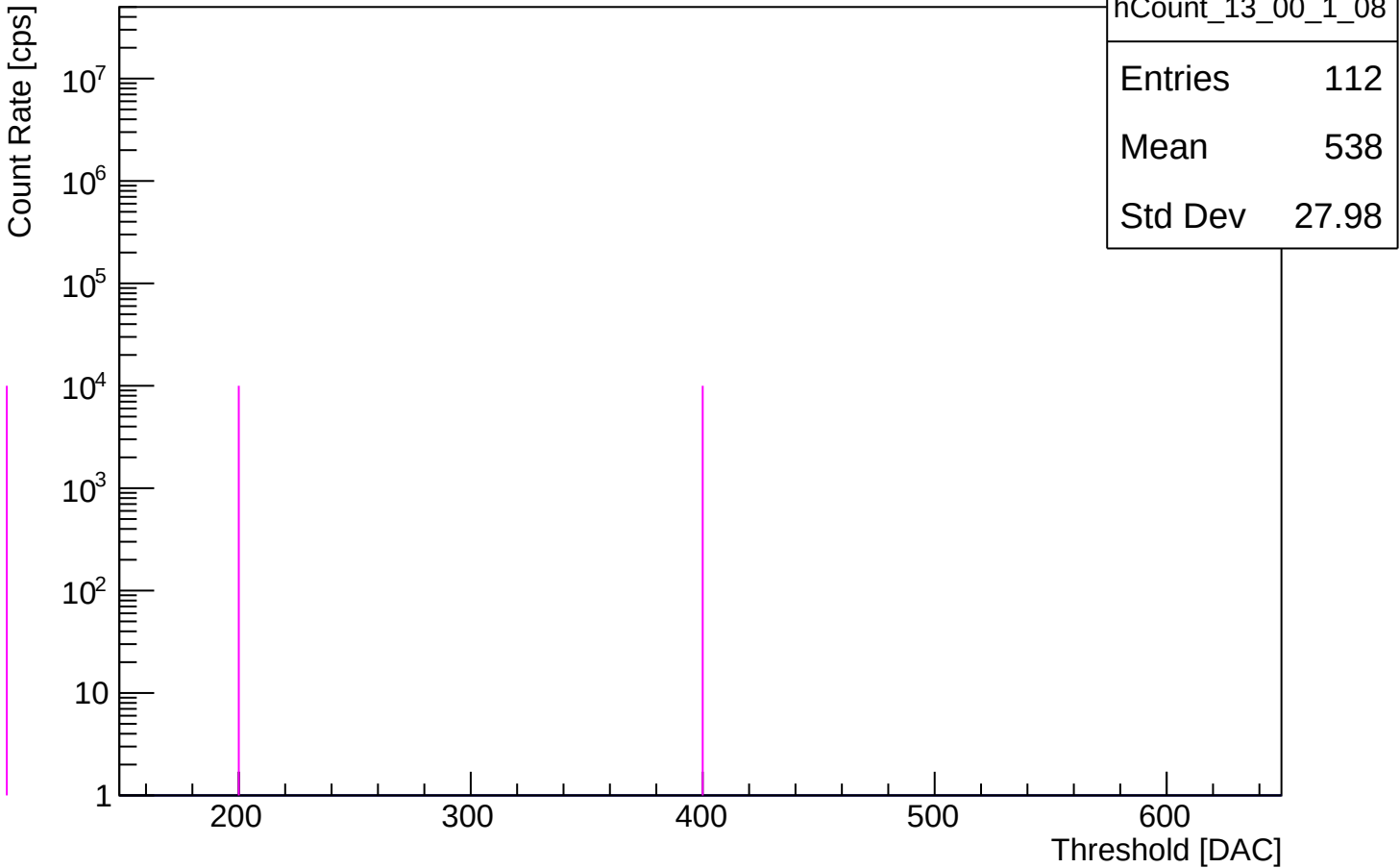


Row 1 Tile 1 Pmt 2 Pixel 42 Slot 13 Fiber 0 Asic 1 Channel 9

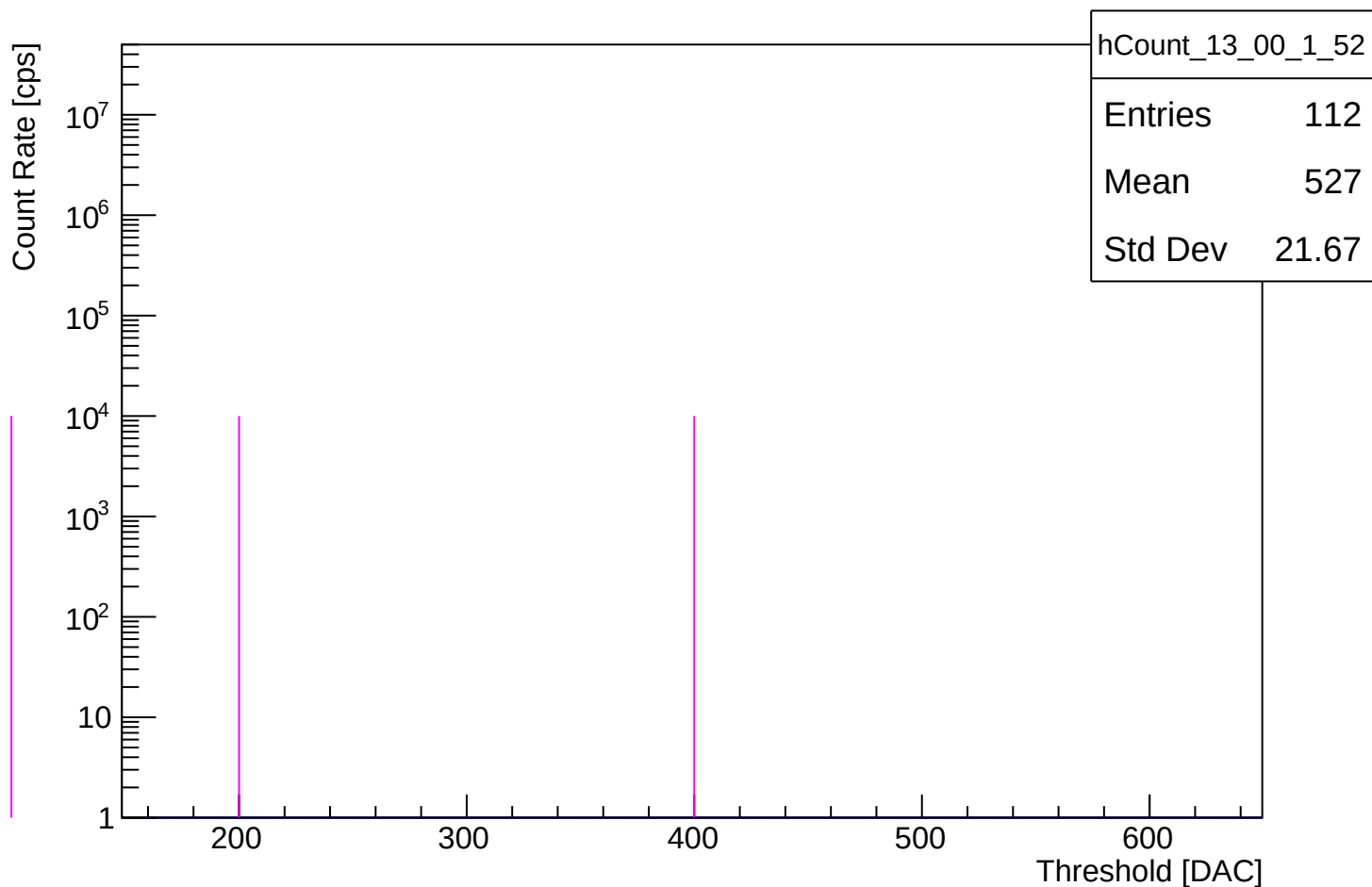


Row 1 Tile 1 Pmt 2 Pixel 43 Slot 13 Fiber 0 Asic 1 Channel 10

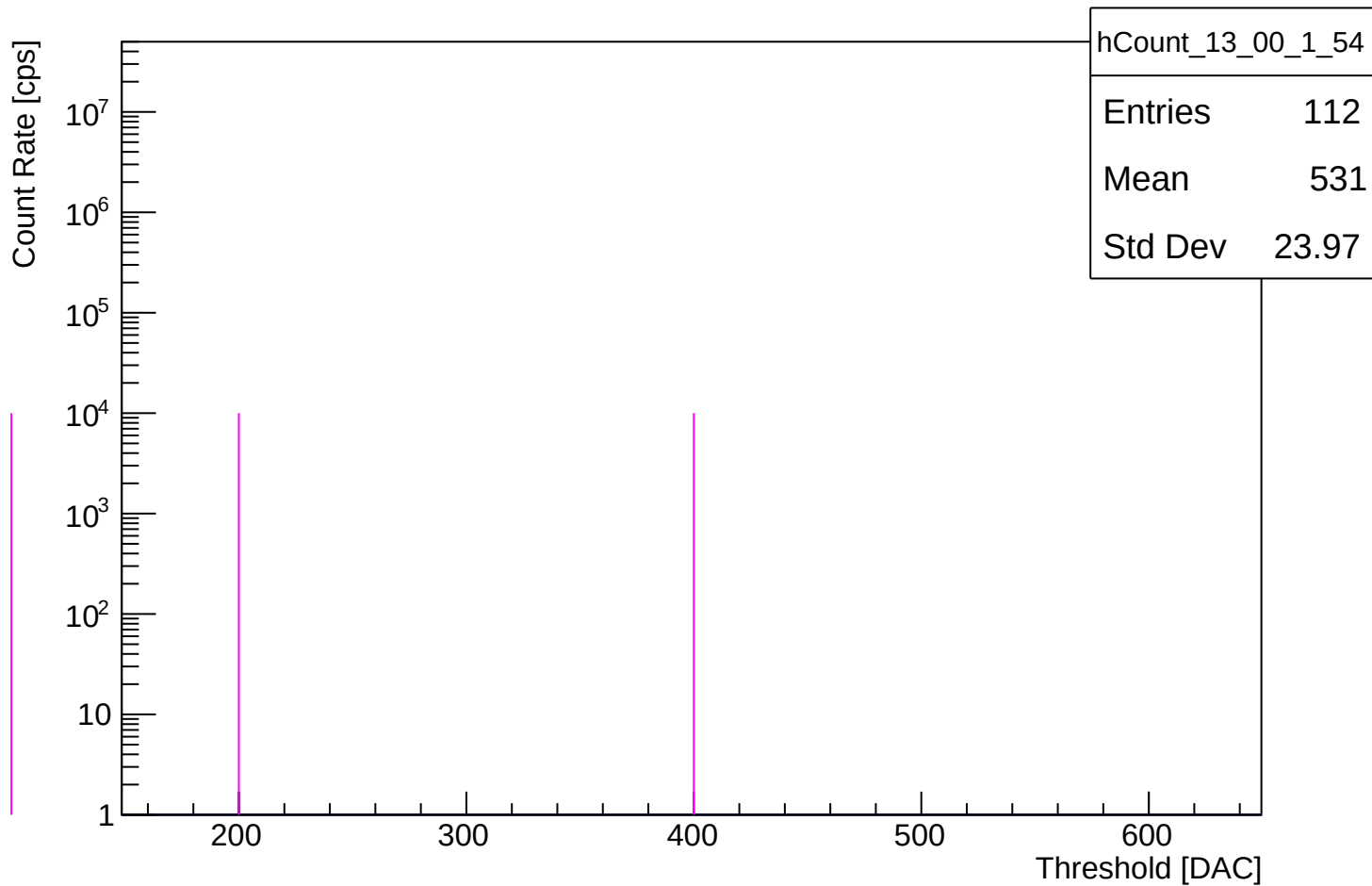




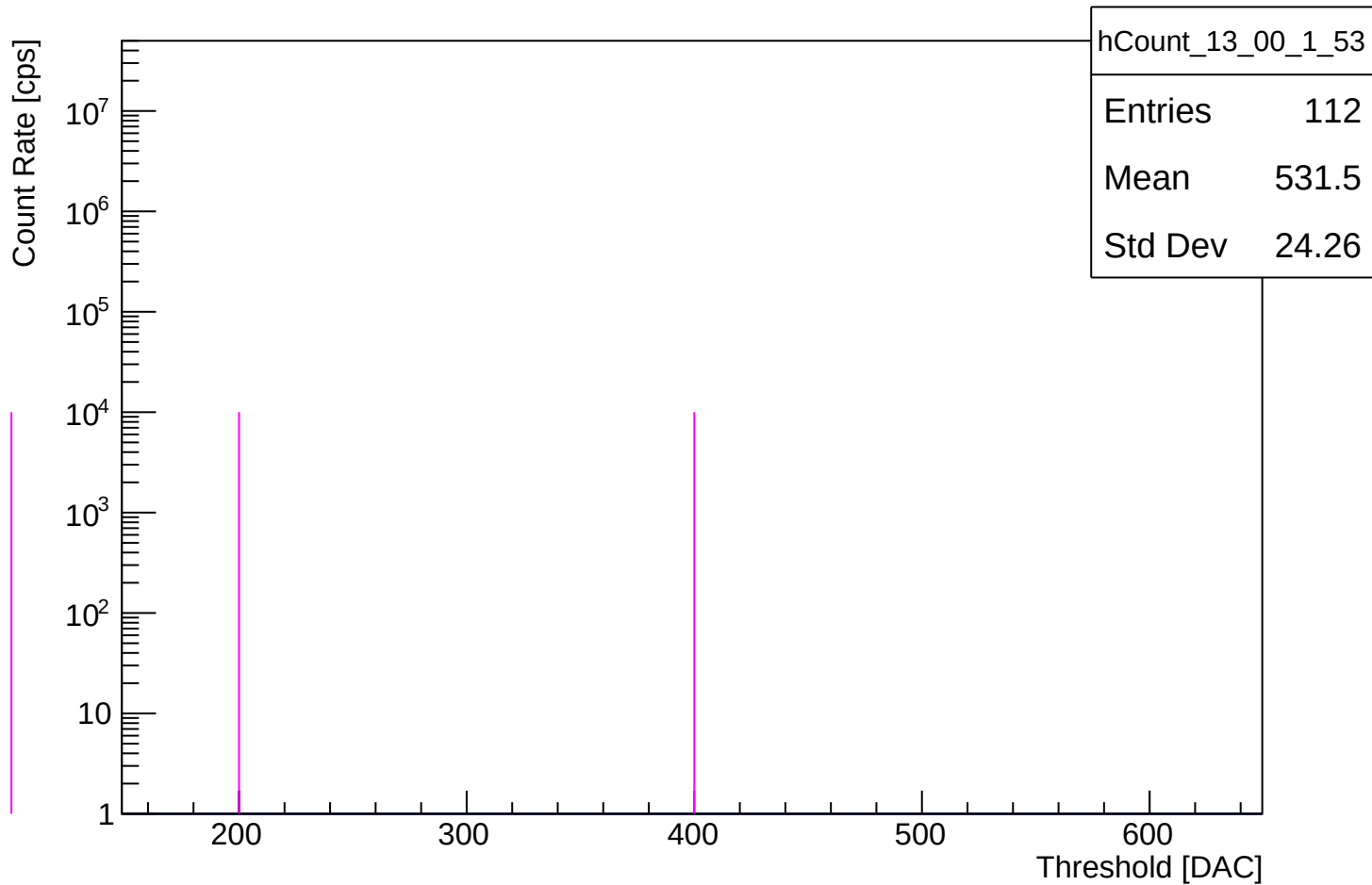
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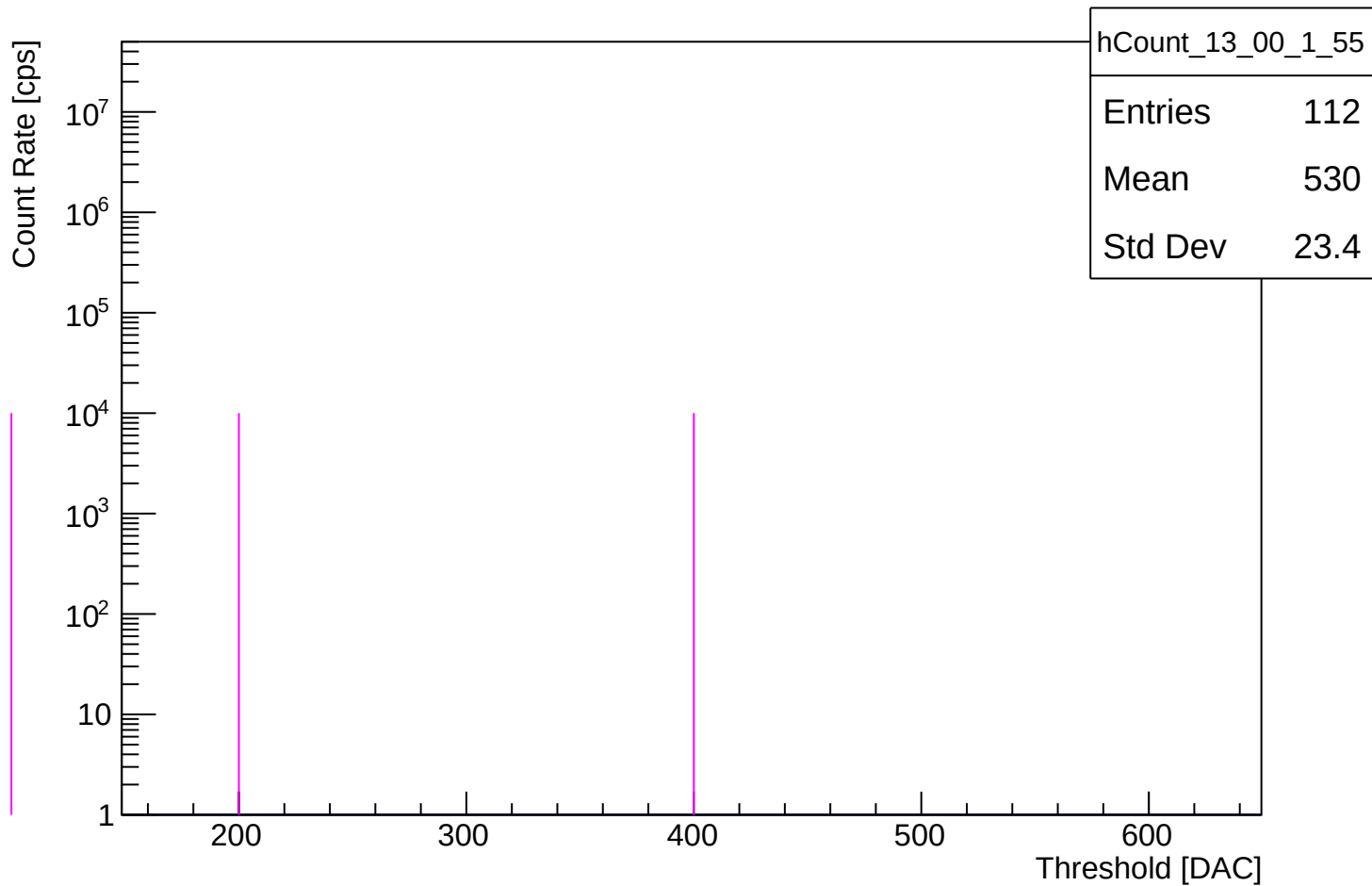
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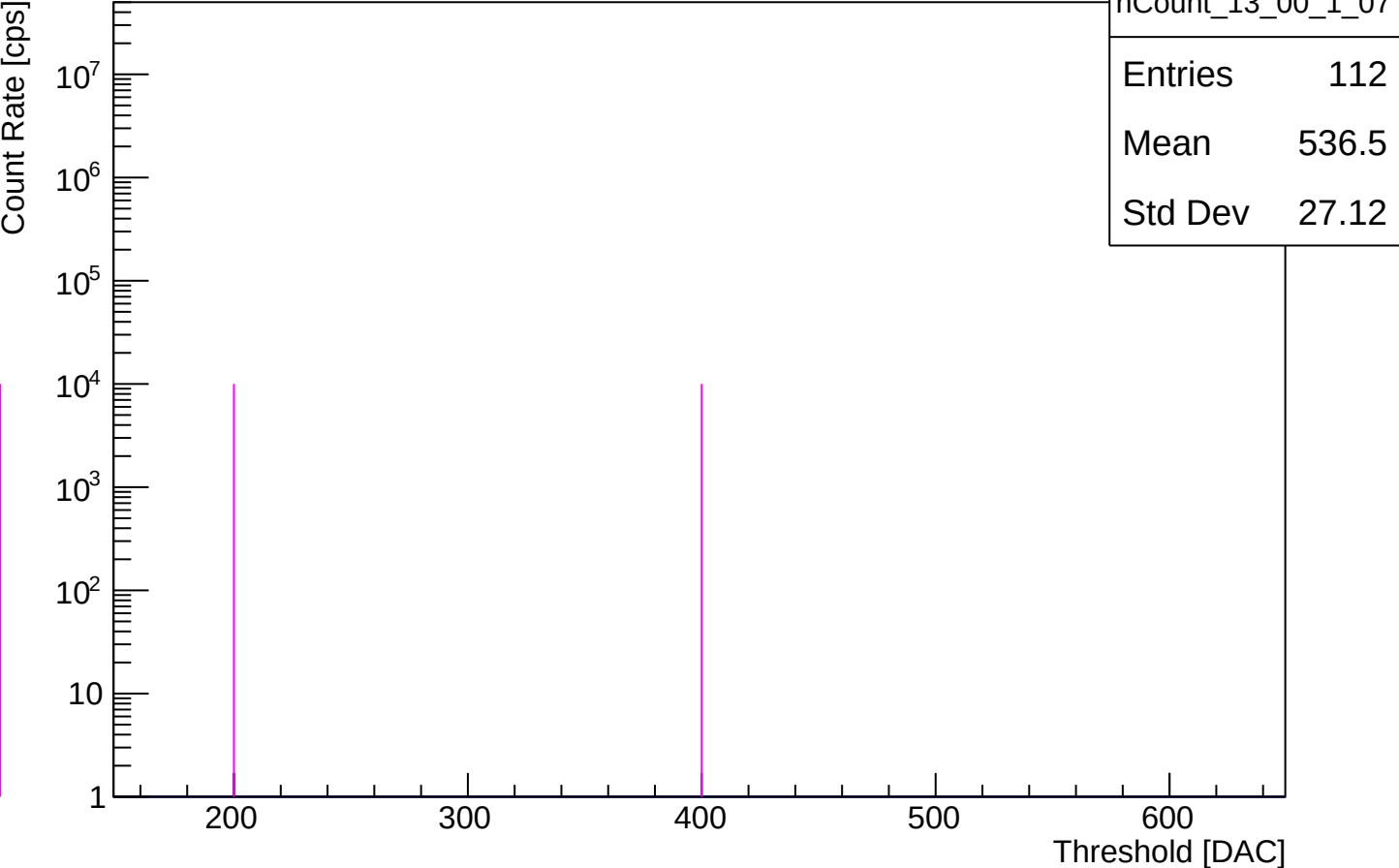
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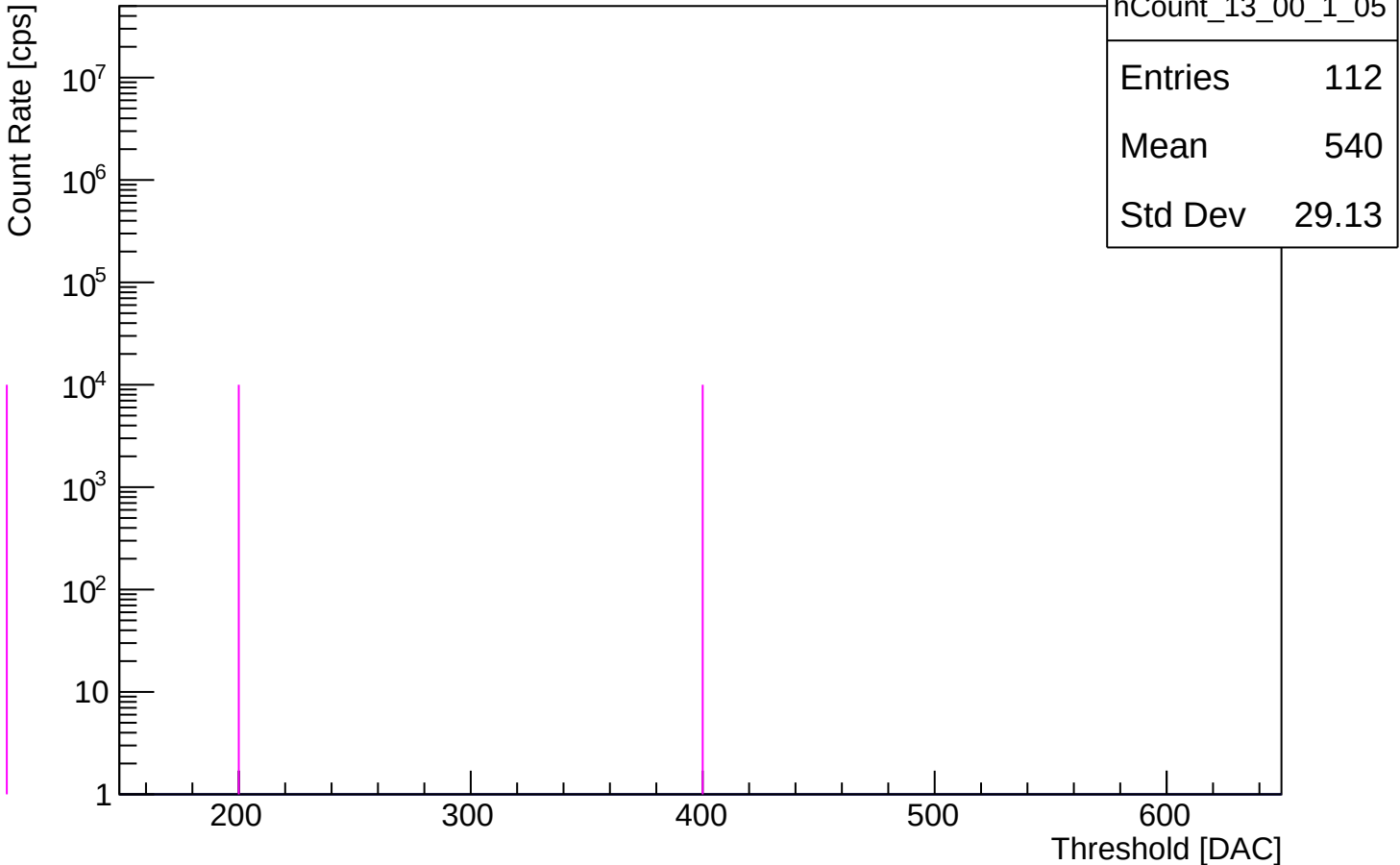
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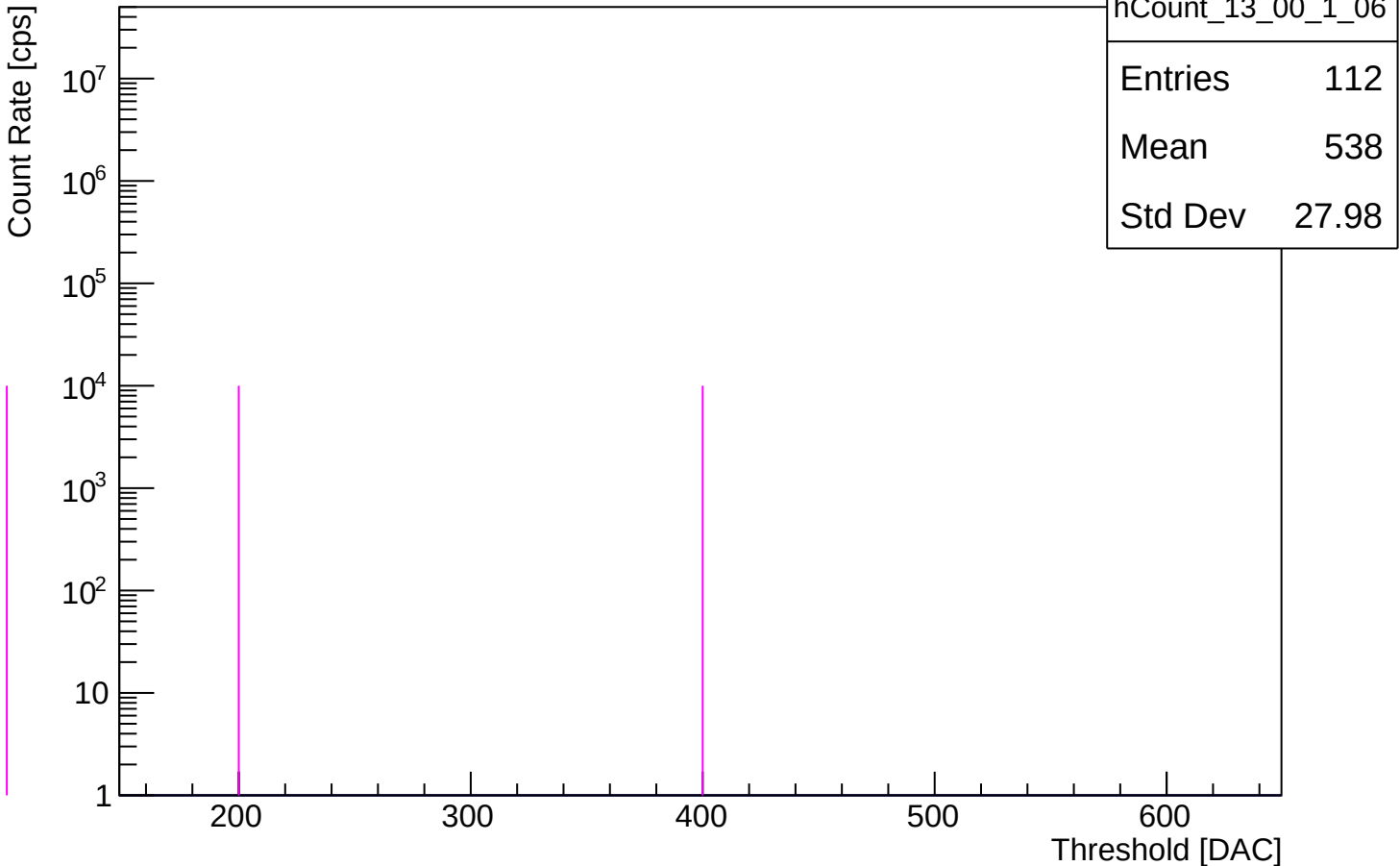


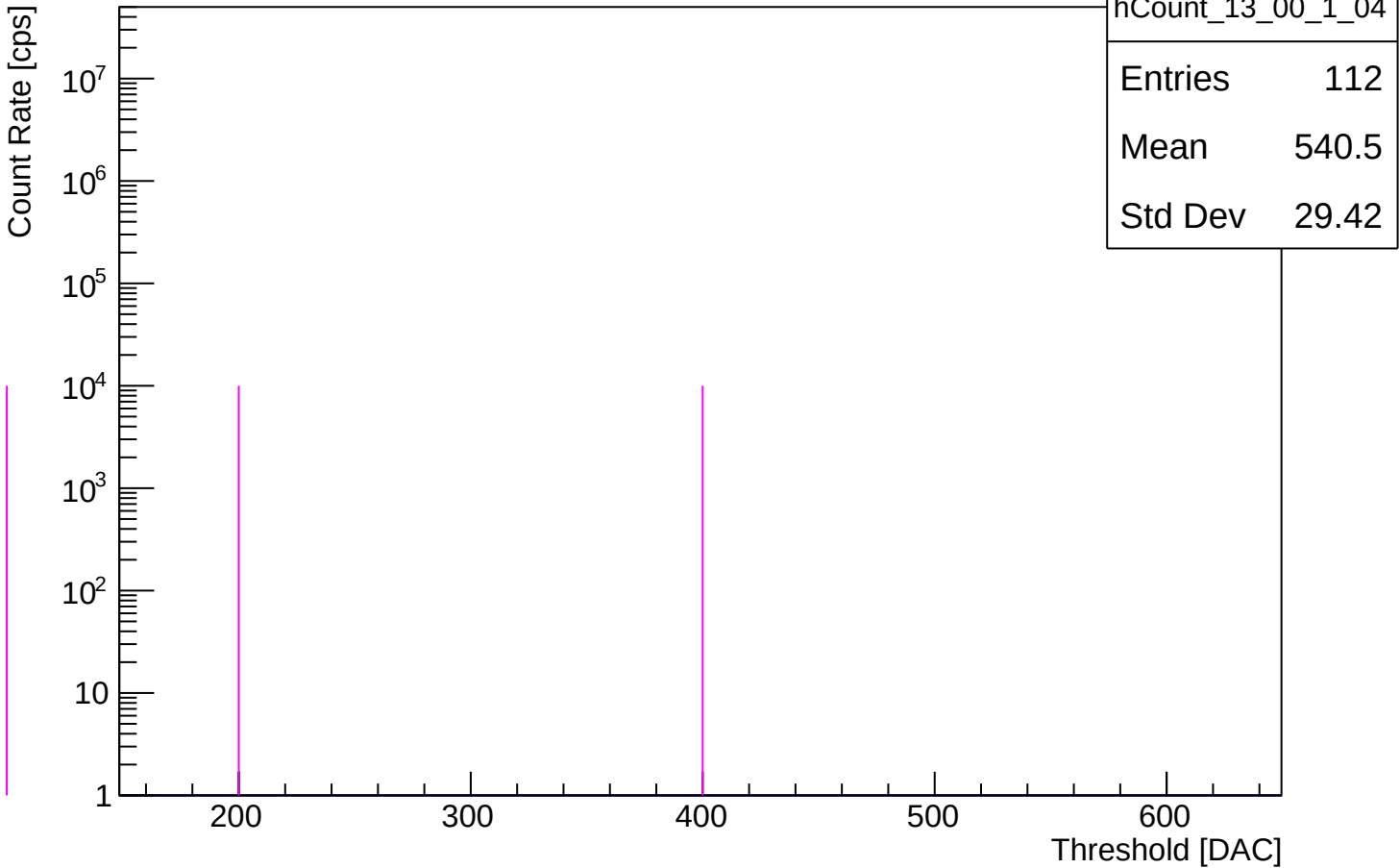




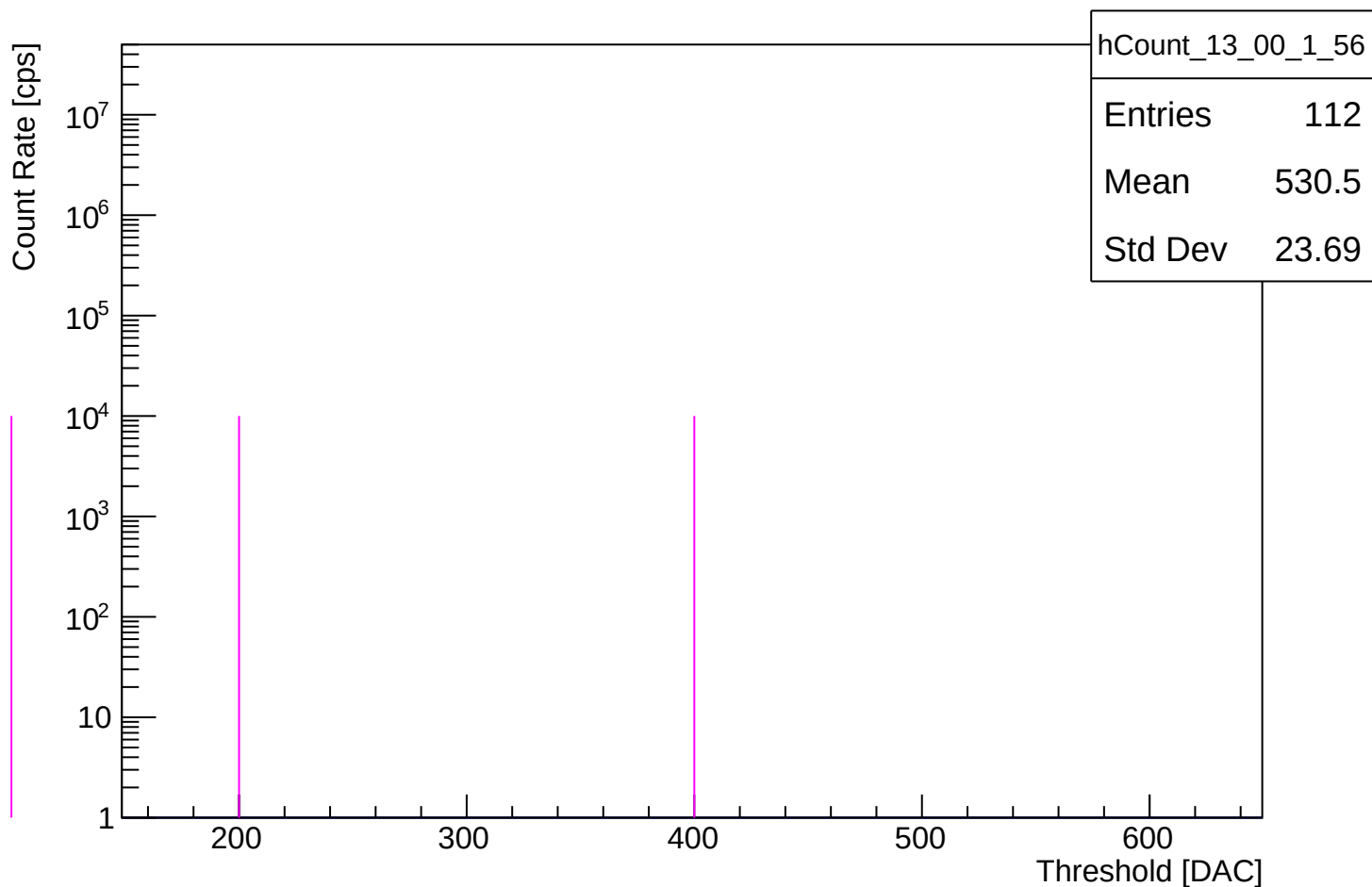
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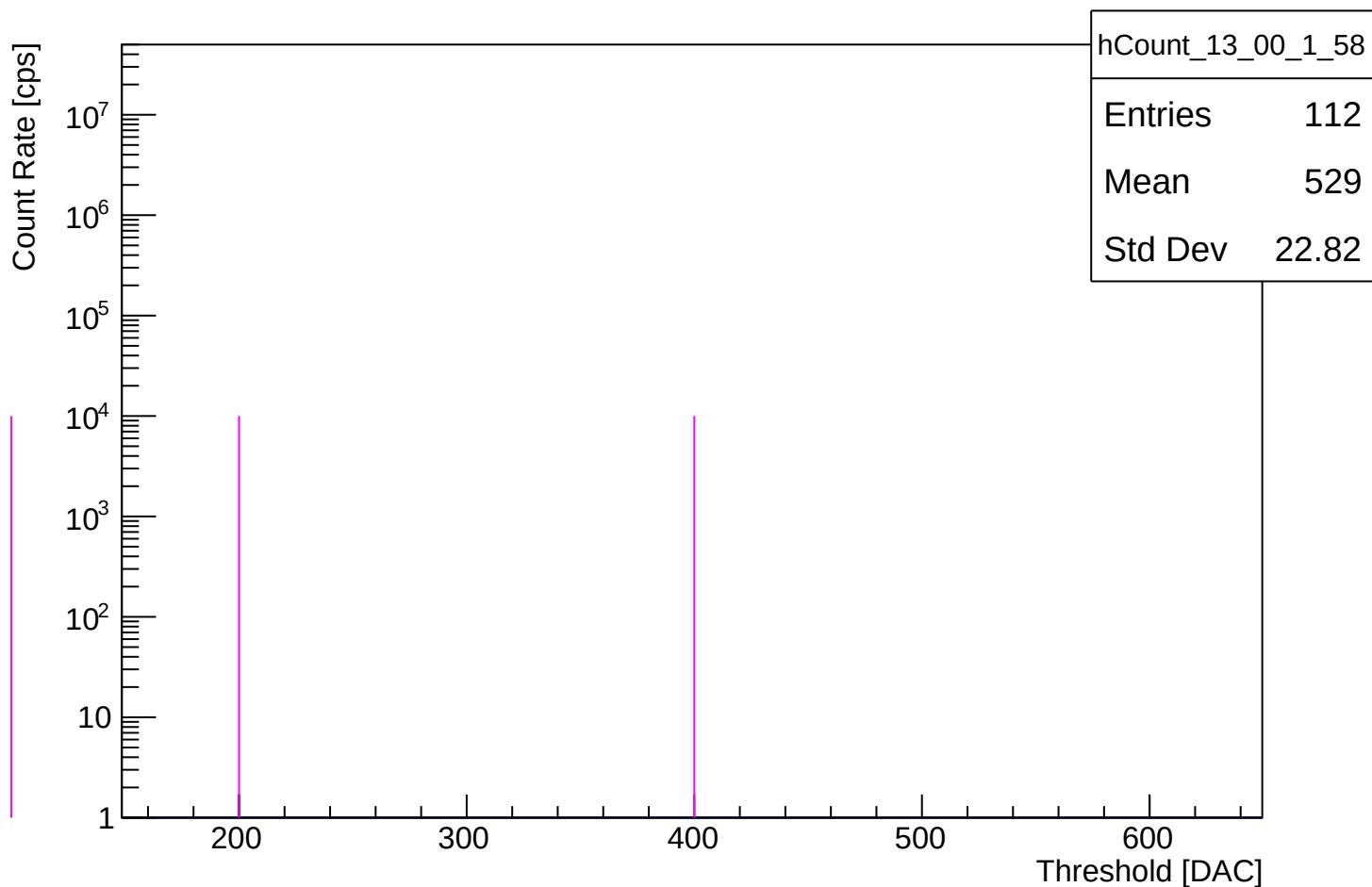




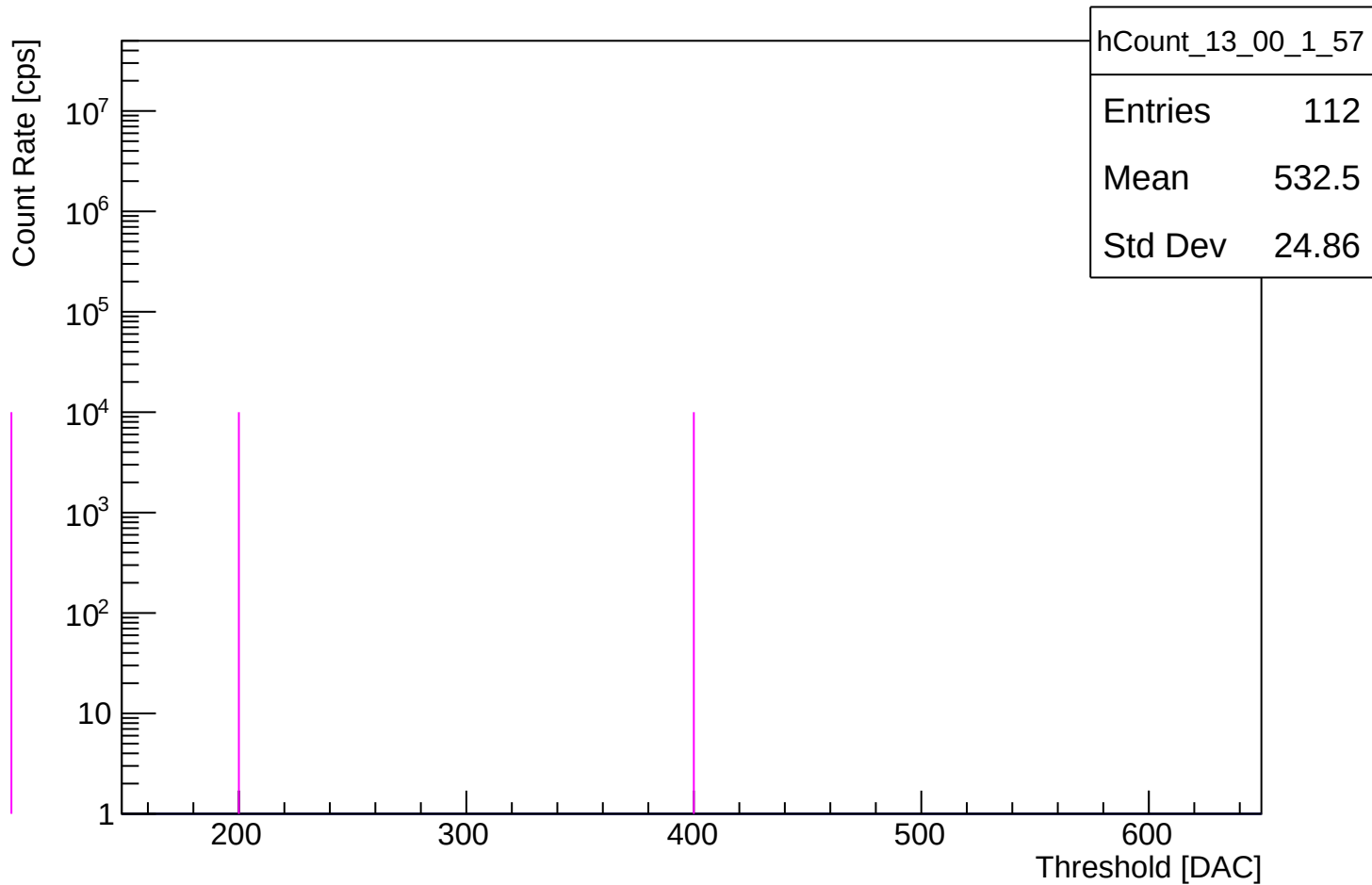
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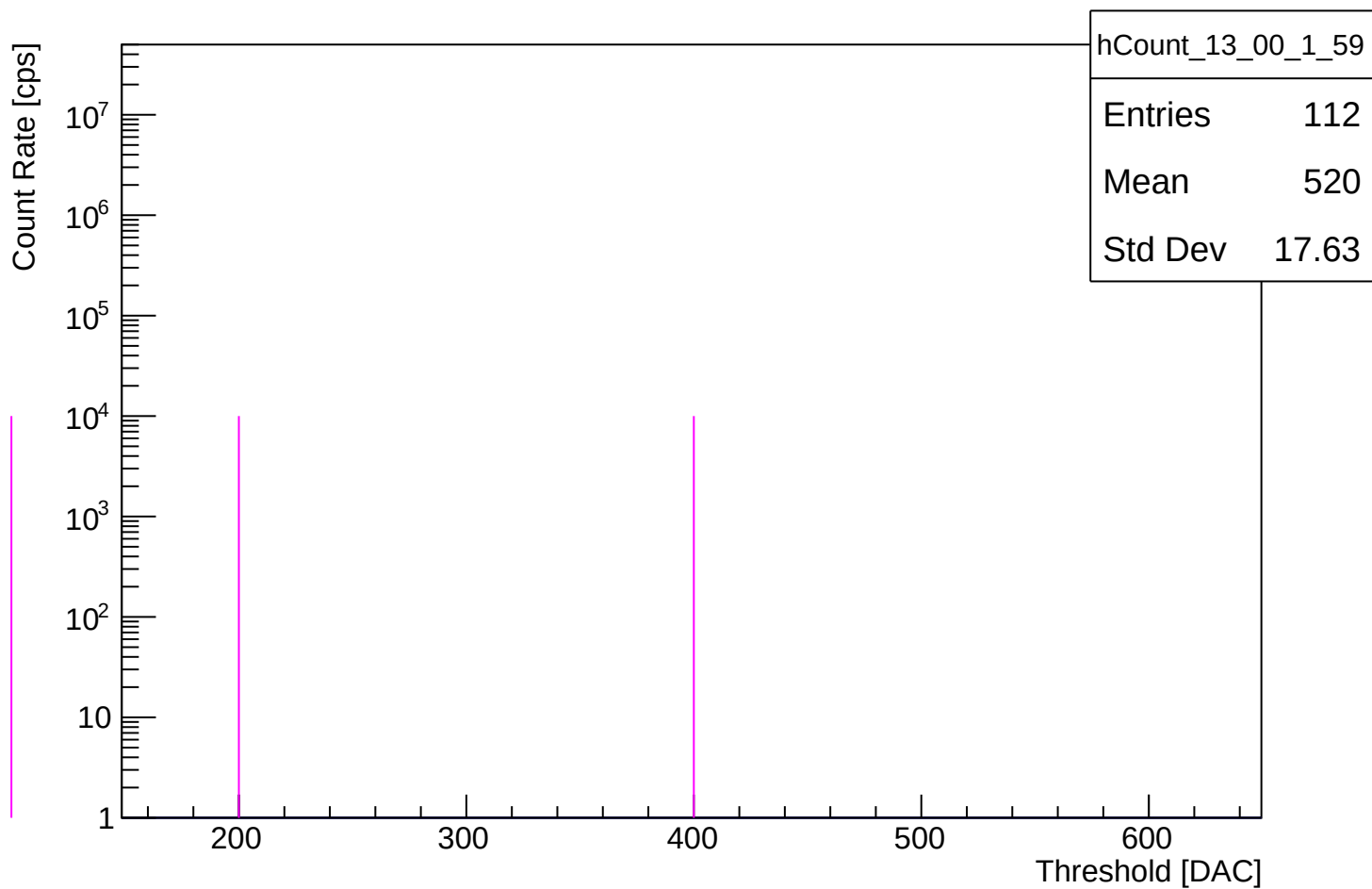
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Row 1 Tile 1 Pmt 2 Pixel 55 Slot 13 Fiber 0 Asic 1 Channel 57

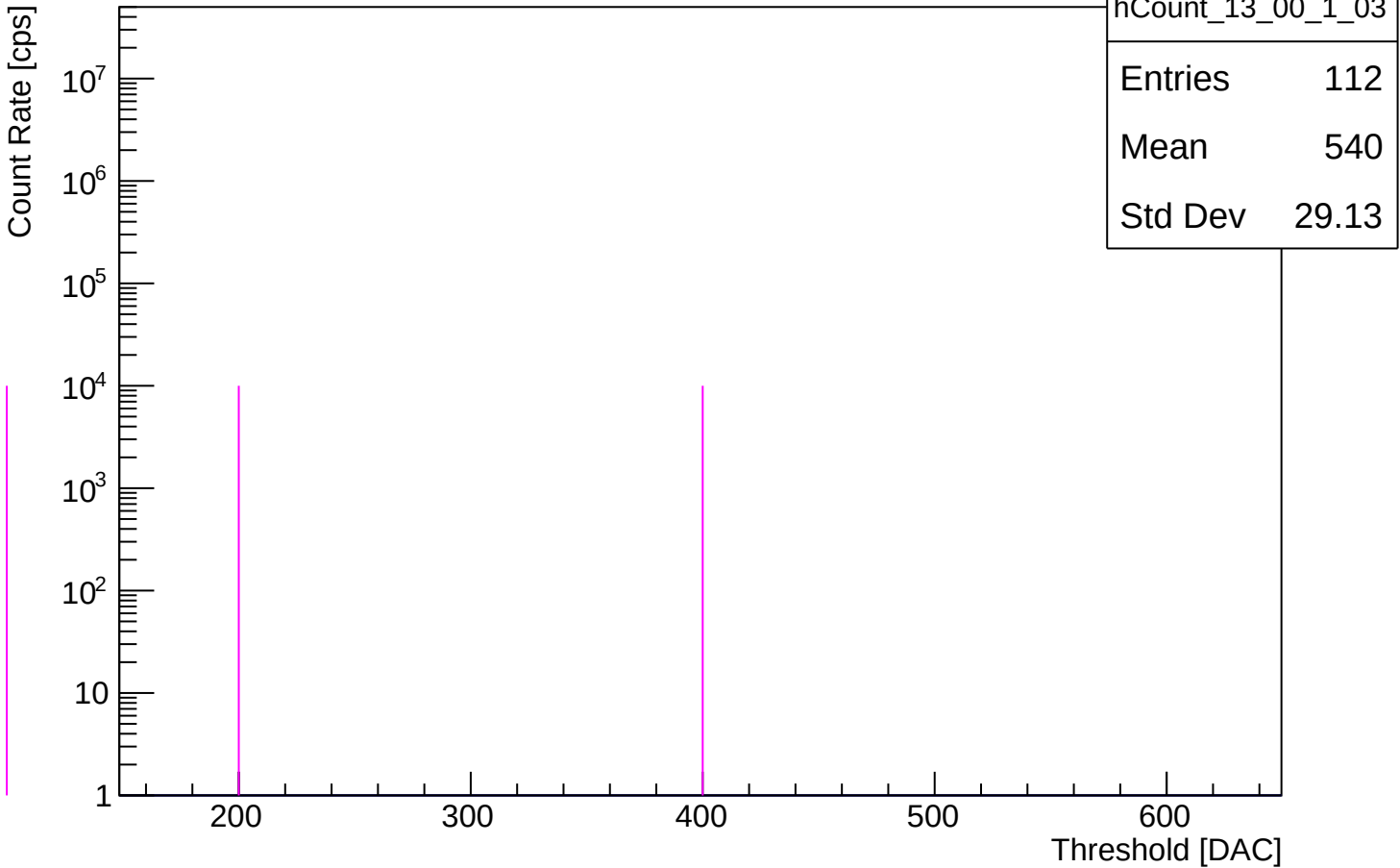


Row 1 Tile 1 Pmt 2 Pixel 56 Slot 13 Fiber 0 Asic 1 Channel 59

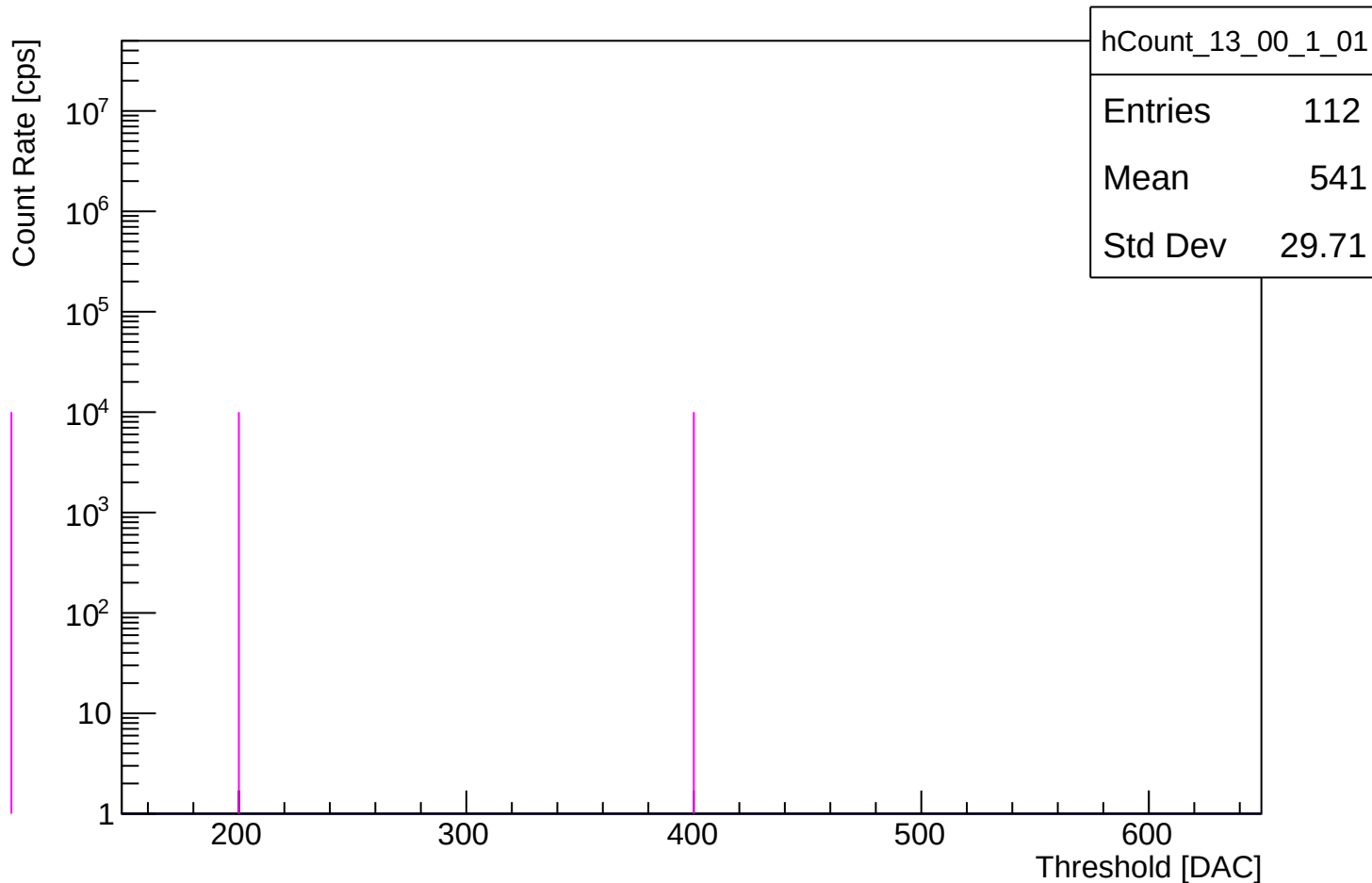


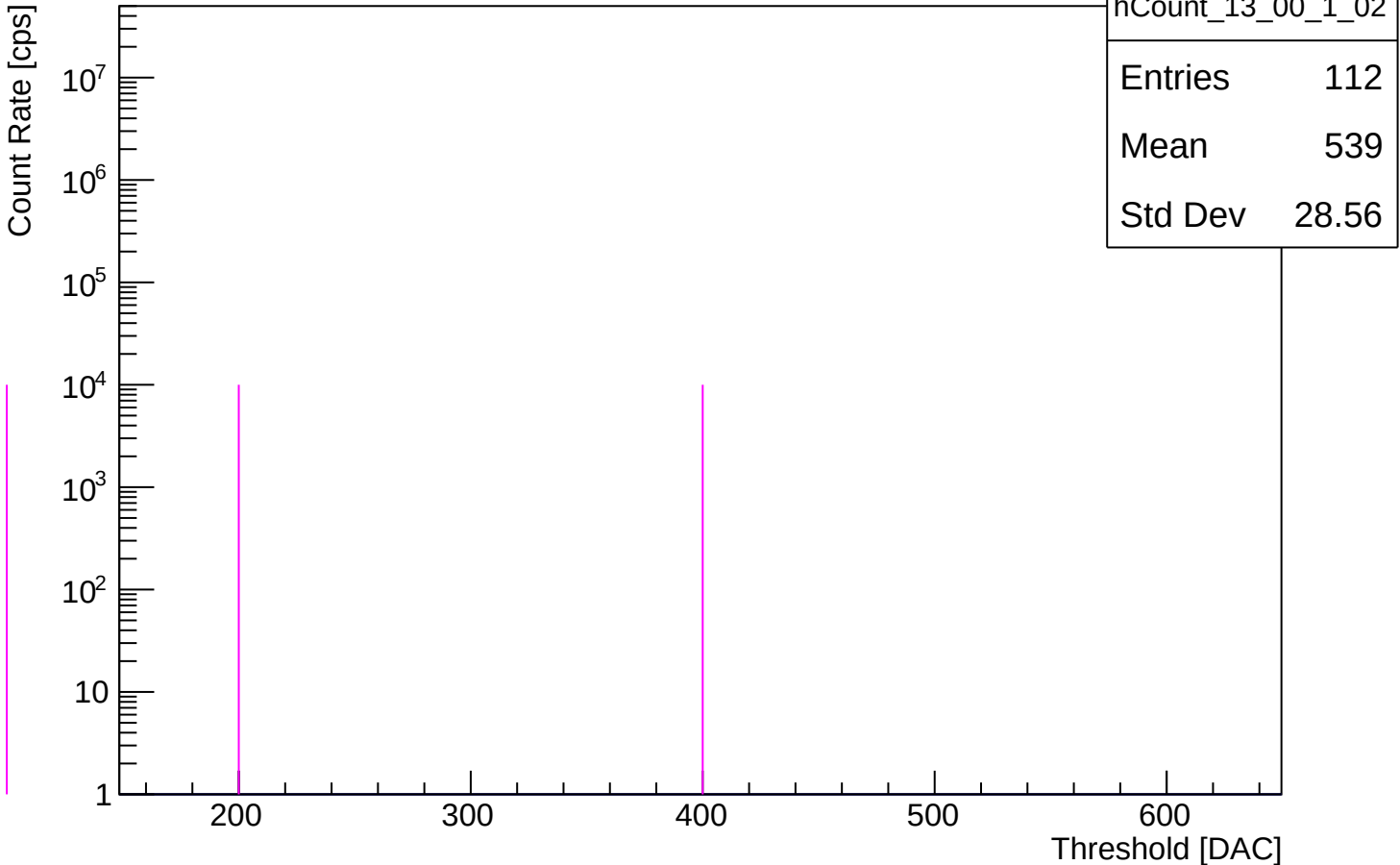


Row 1 Tile 1 Pmt 2 Pixel 57 Slot 13 Fiber 0 Asic 1 Channel 3

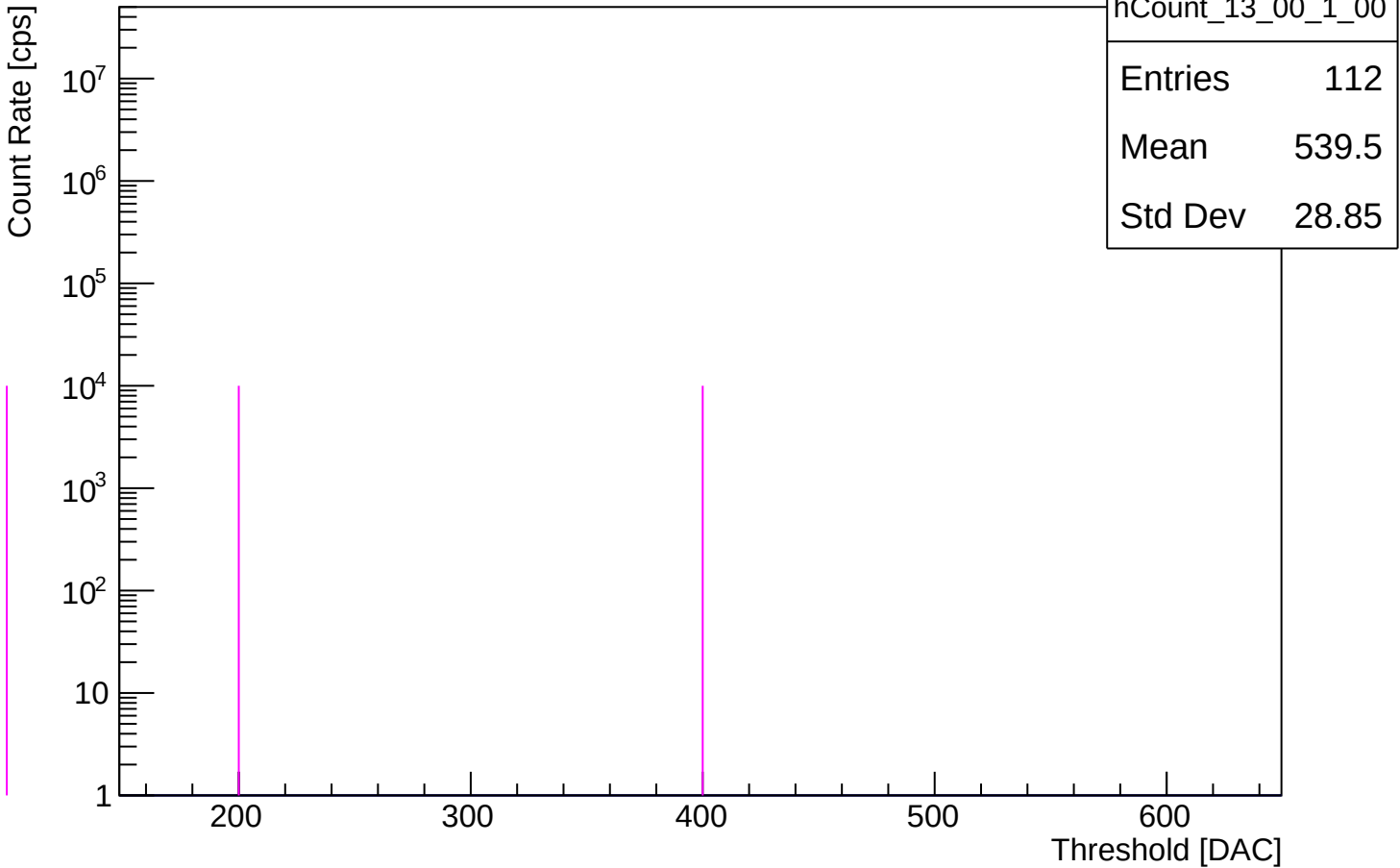


Row 1 Tile 1 Pmt 2 Pixel 58 Slot 13 Fiber 0 Asic 1 Channel 1

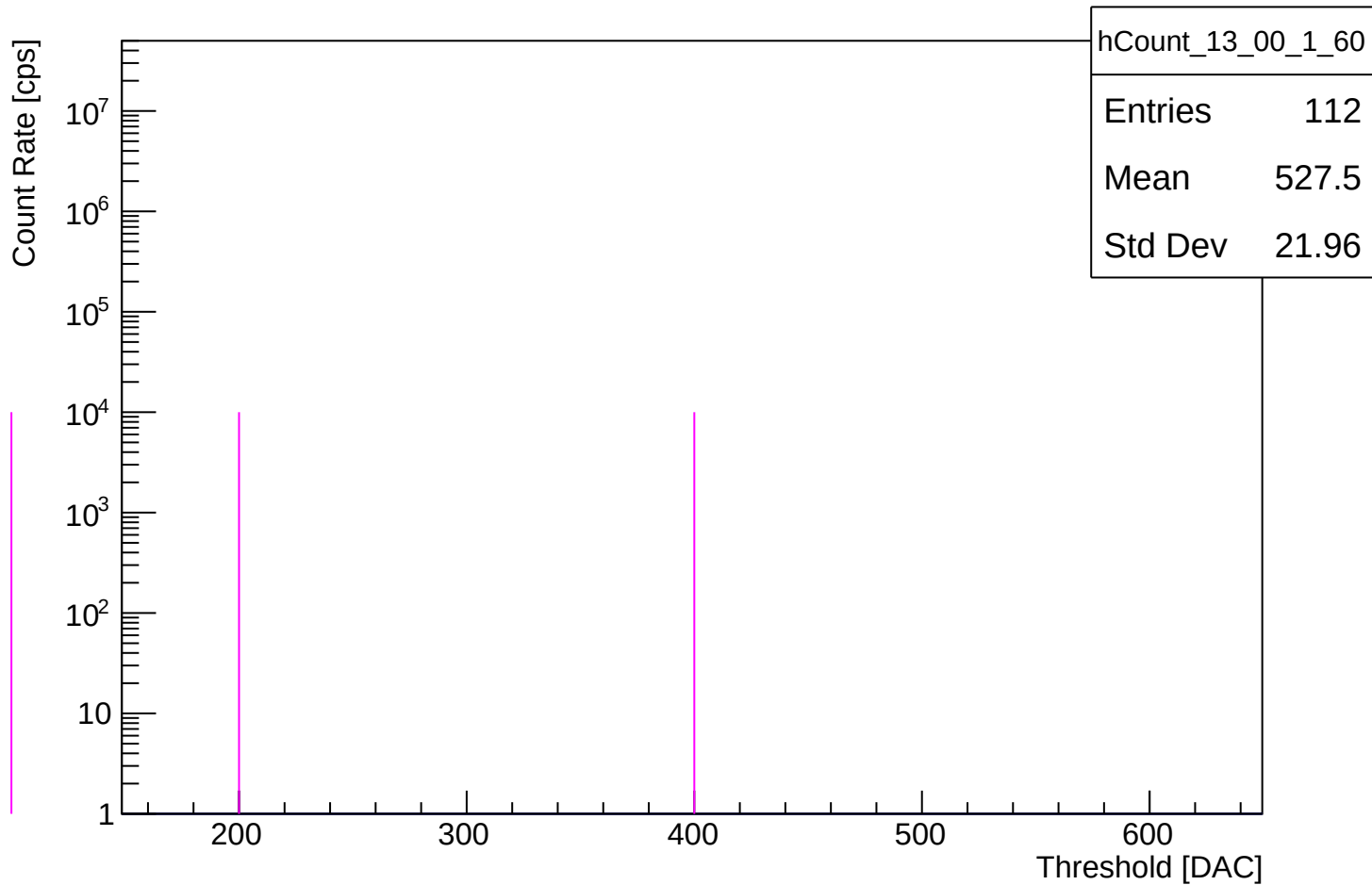




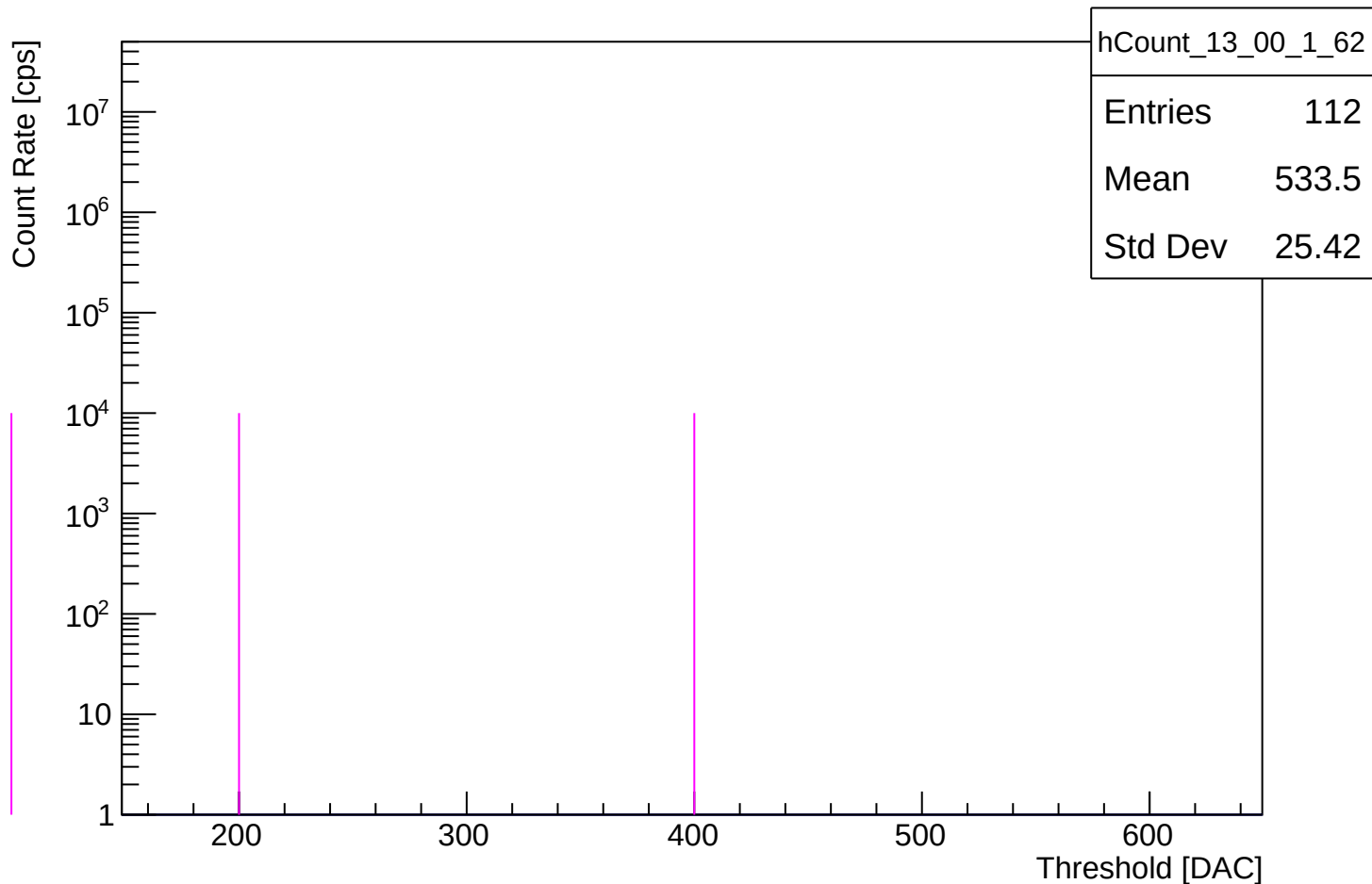
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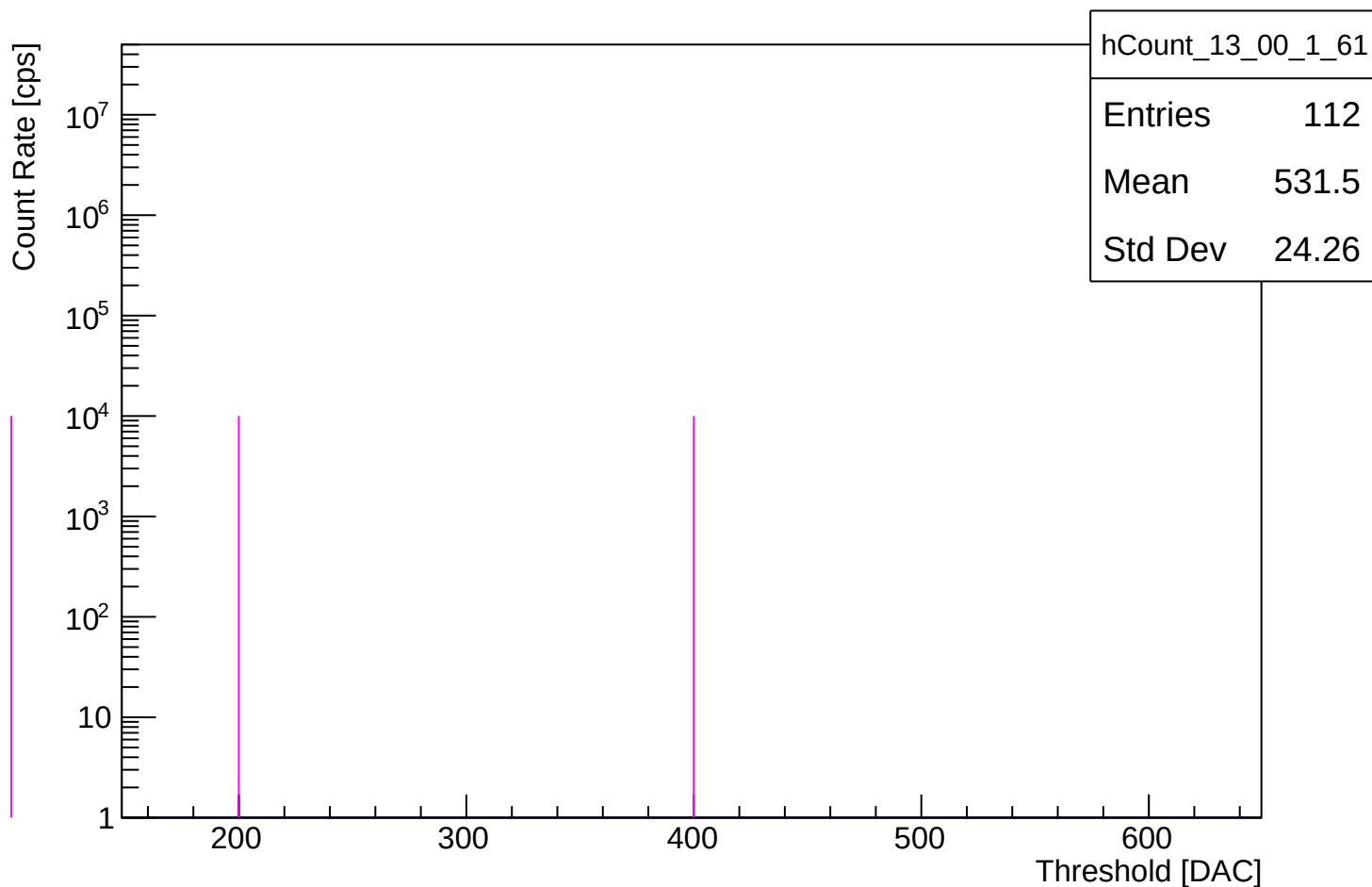
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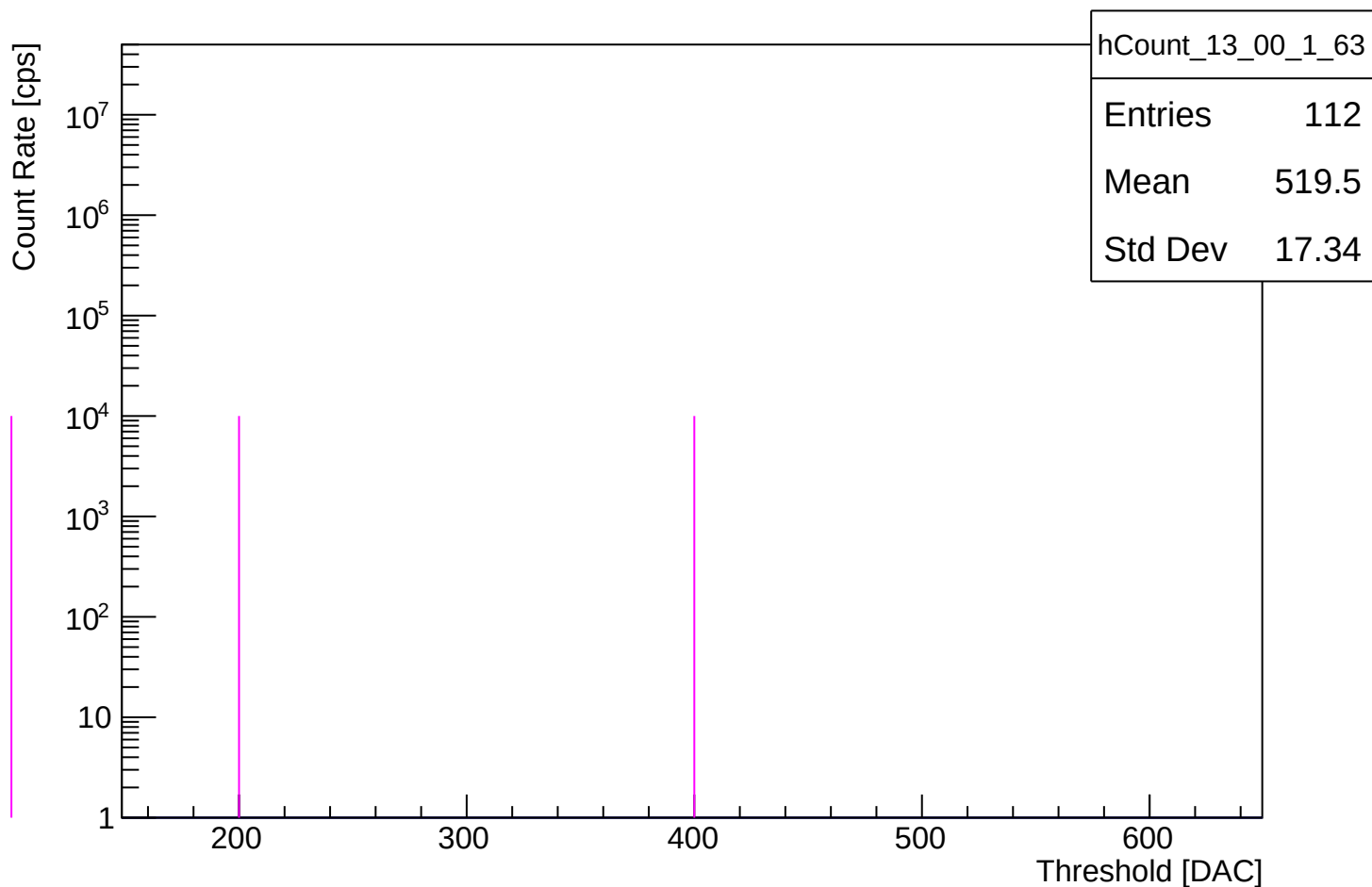
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Row 1 Tile 1 Pmt 2 Pixel 63 Slot 13 Fiber 0 Asic 1 Channel 61

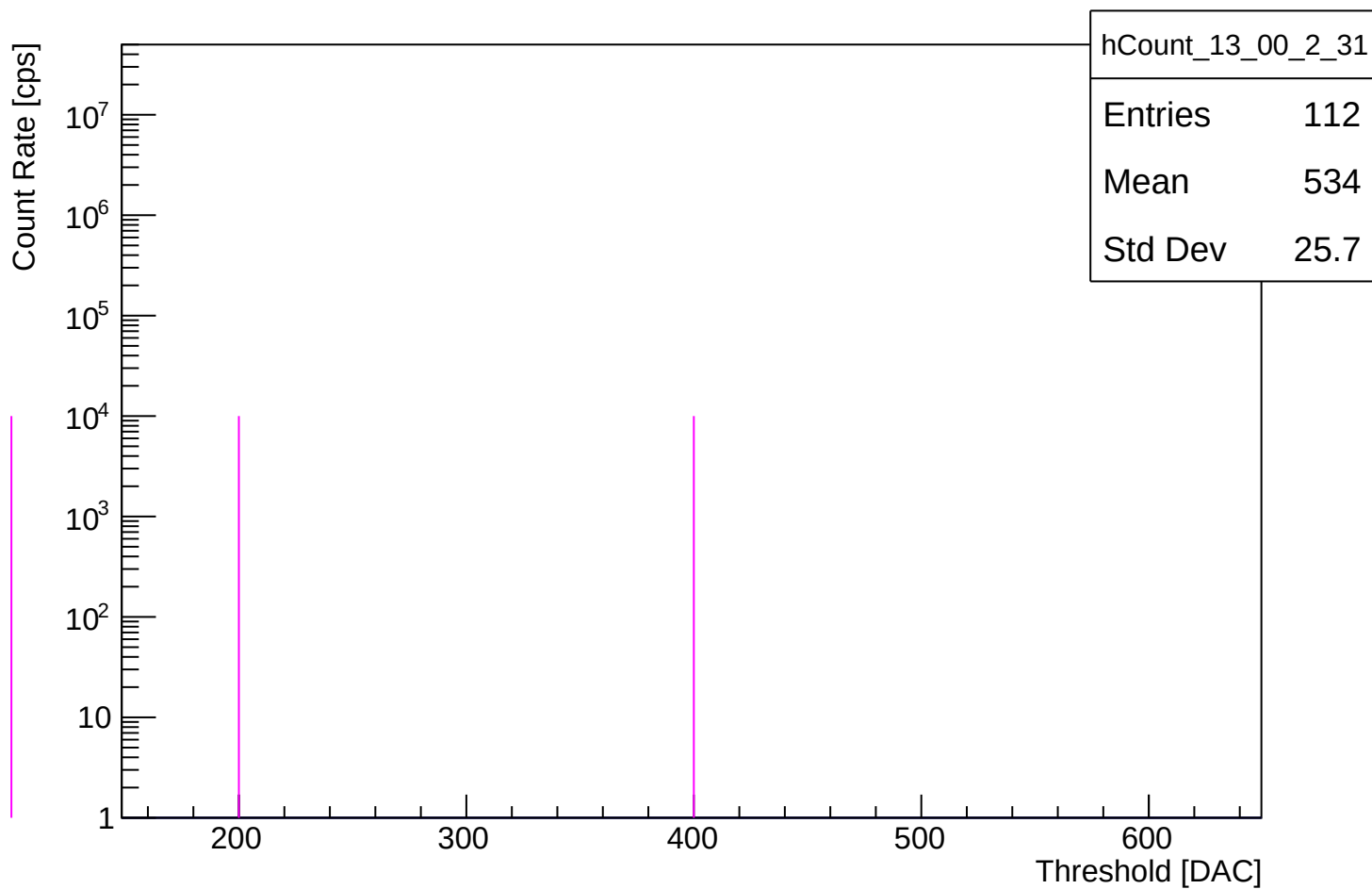


Row 1 Tile 1 Pmt 2 Pixel 64 Slot 13 Fiber 0 Asic 1 Channel 63

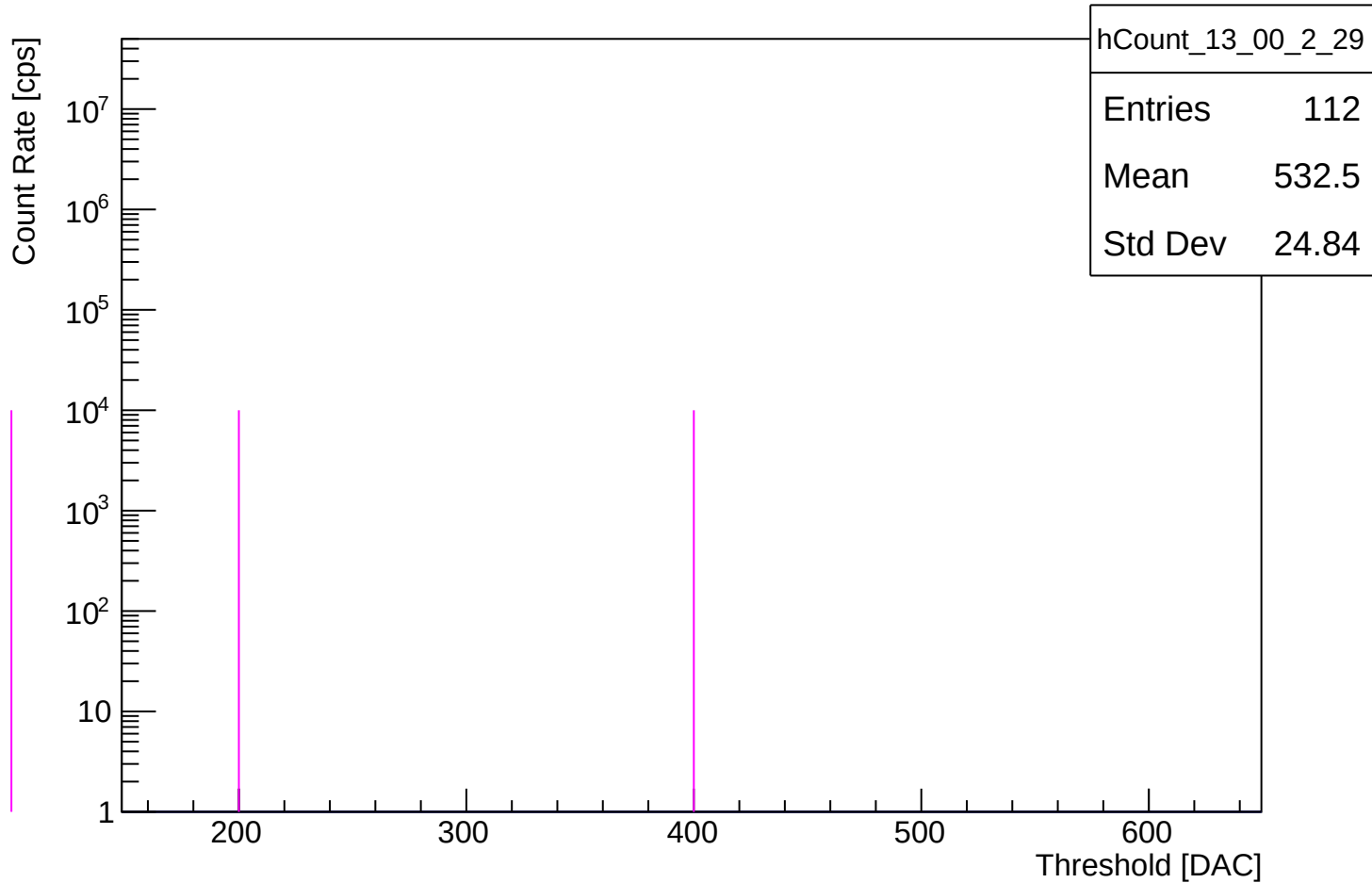




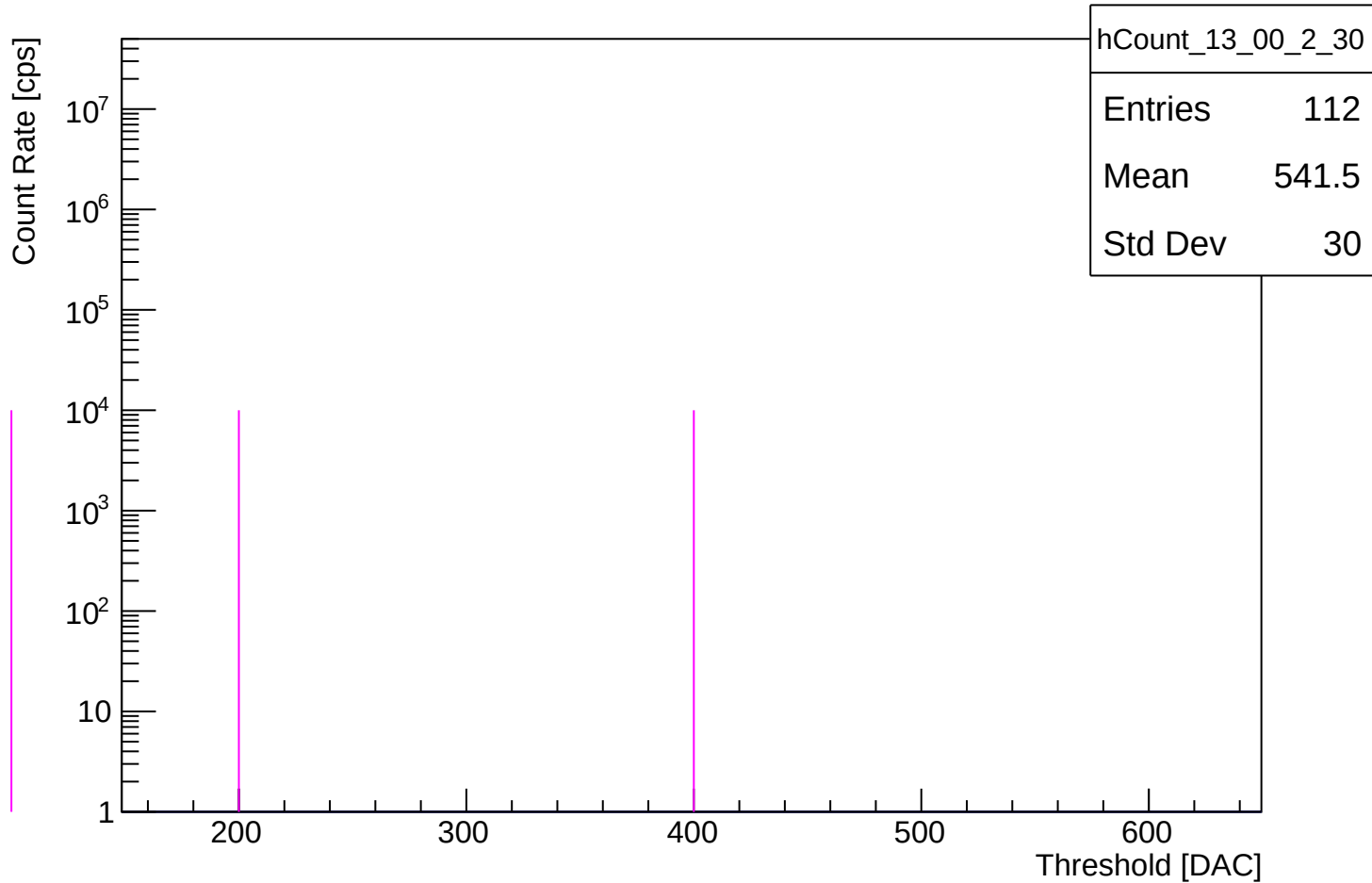
Row 1 Tile 1 Pmt 3 Pixel 1 Slot 13 Fiber 0 Asic 2 Channel 31



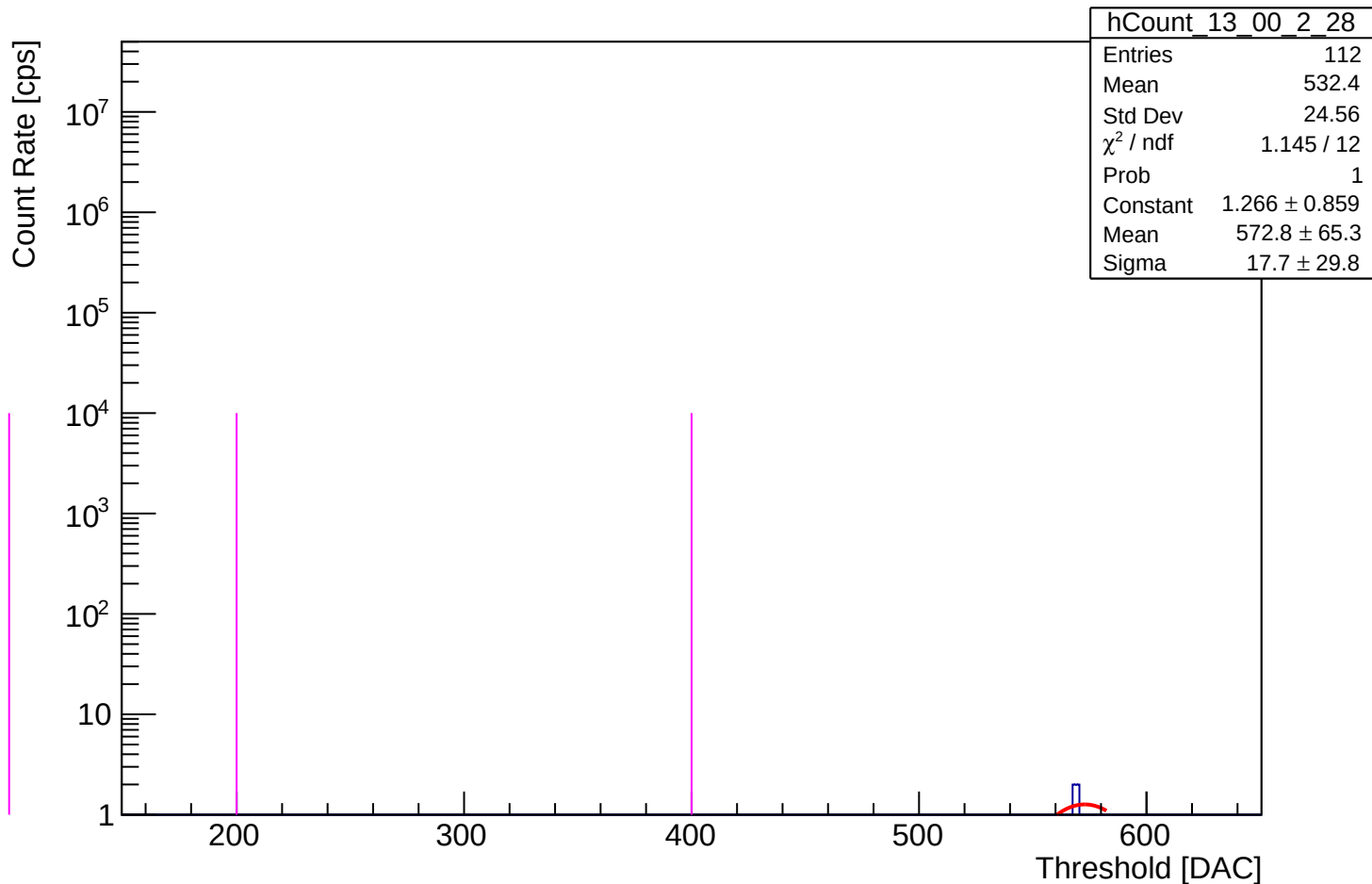
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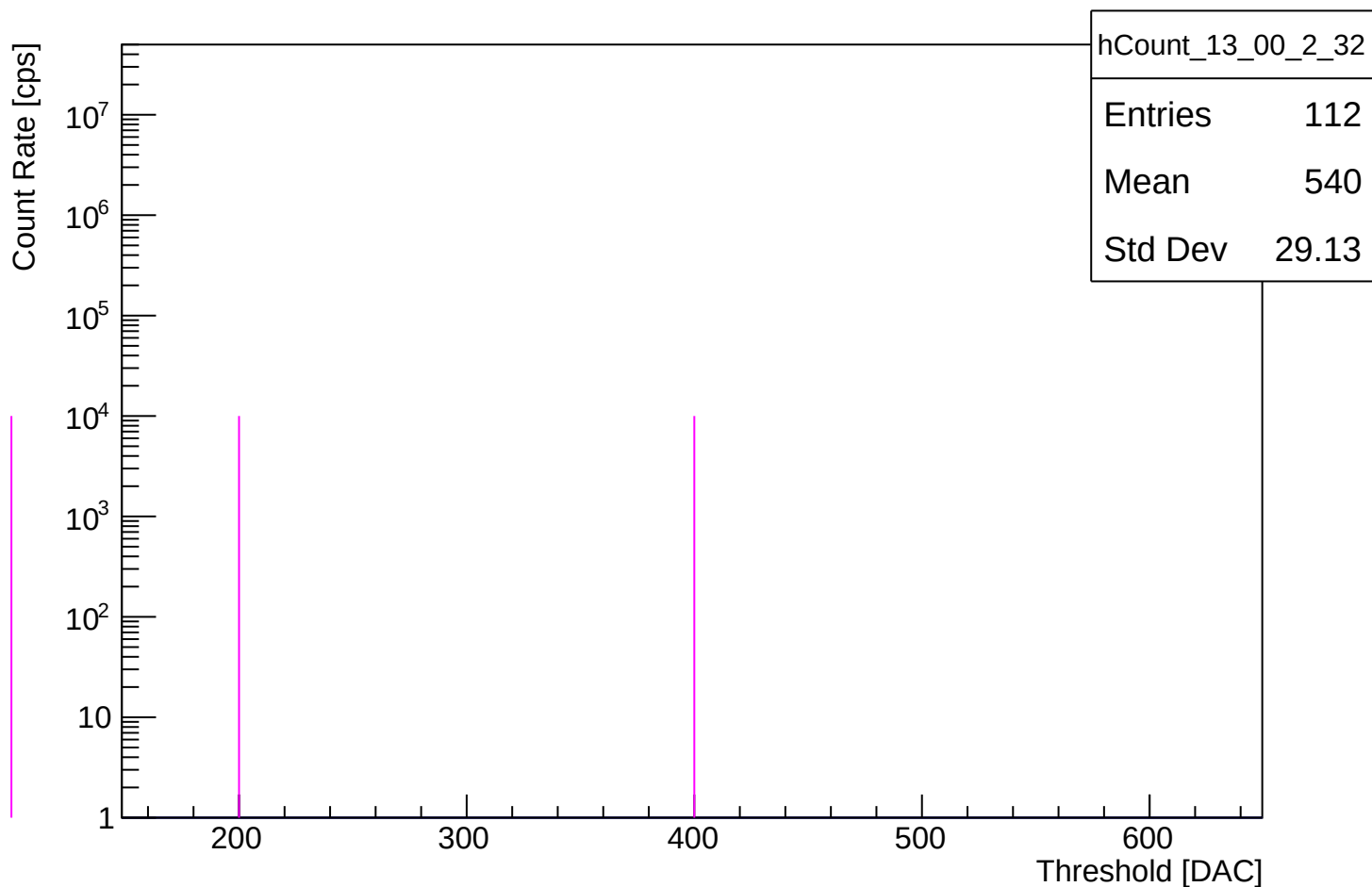
Row 1 Tile 1 Pmt 3 Pixel 3 Slot 13 Fiber 0 Asic 2 Channel 30



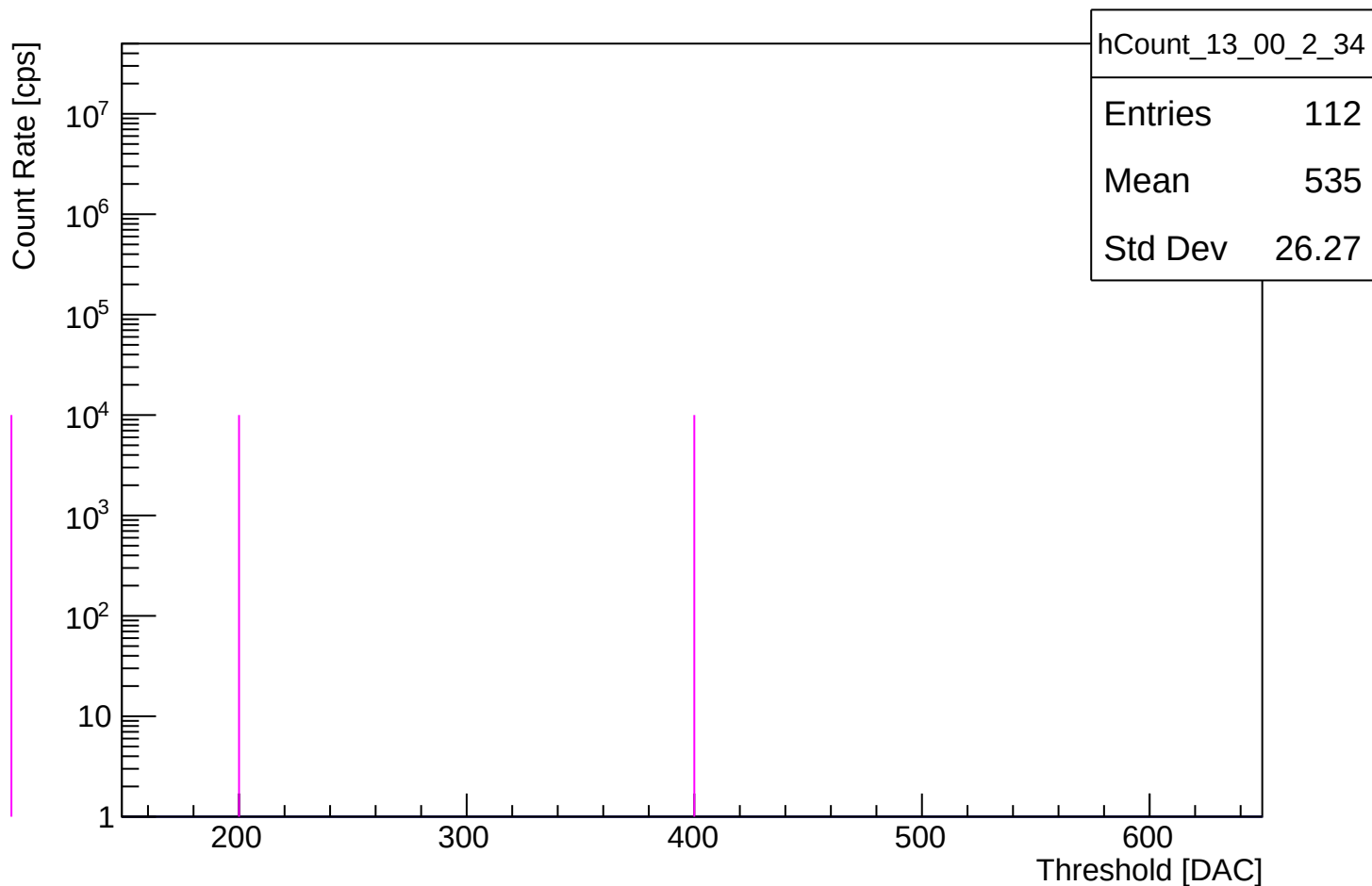
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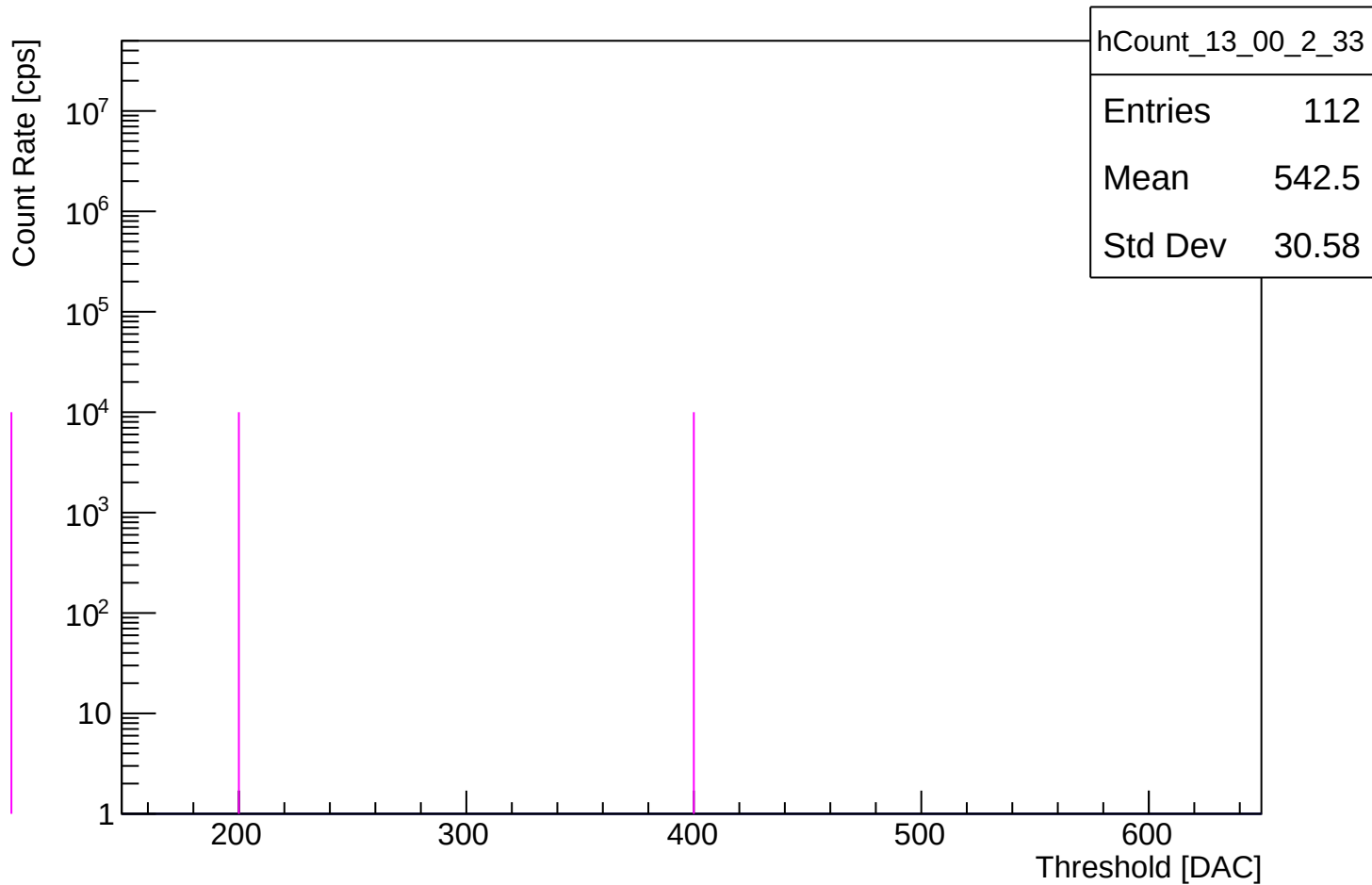
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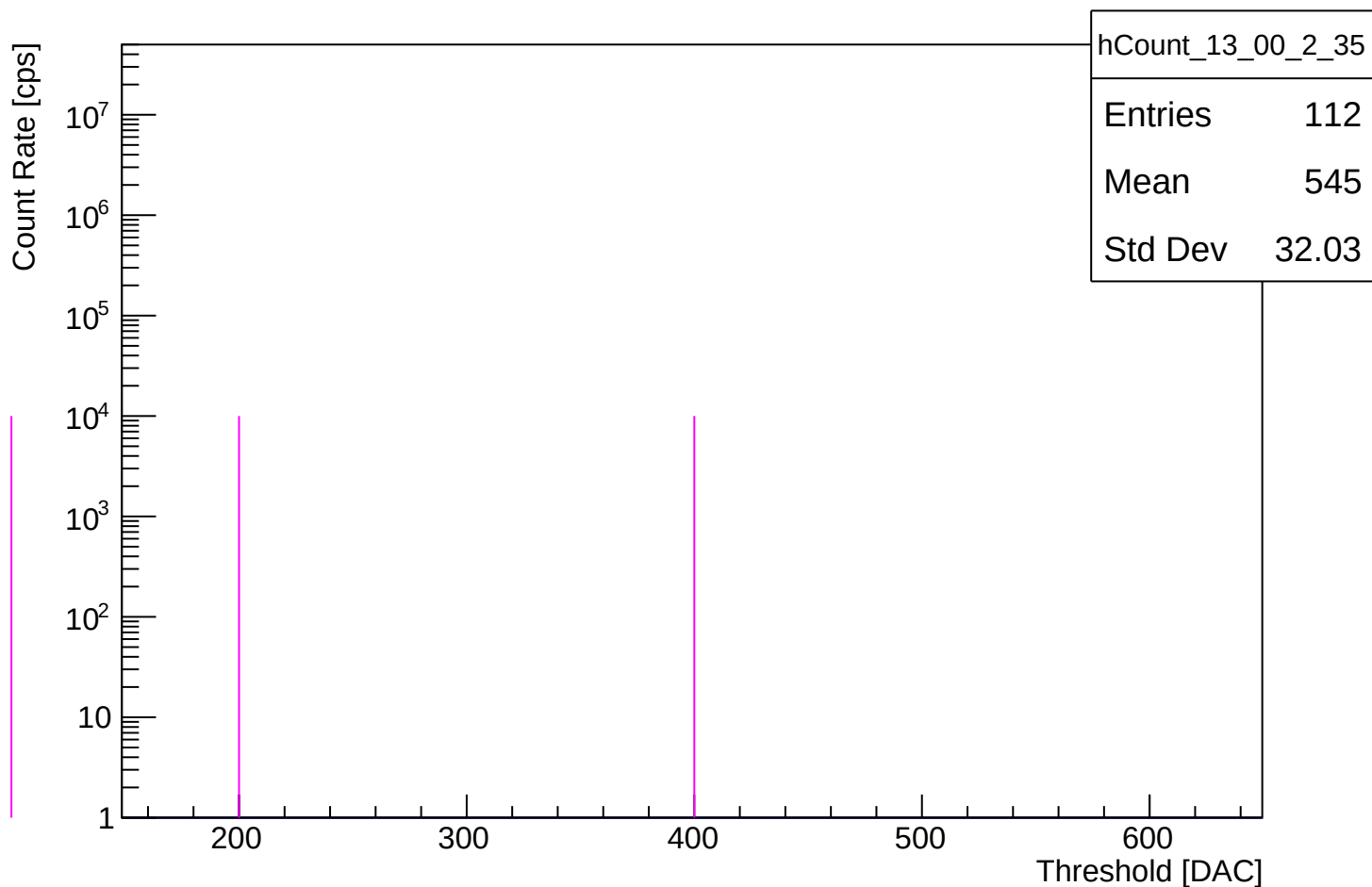
Row 1 Tile 1 Pmt 3 Pixel 6 Slot 13 Fiber 0 Asic 2 Channel 34



Row 1 Tile 1 Pmt 3 Pixel 7 Slot 13 Fiber 0 Asic 2 Channel 33

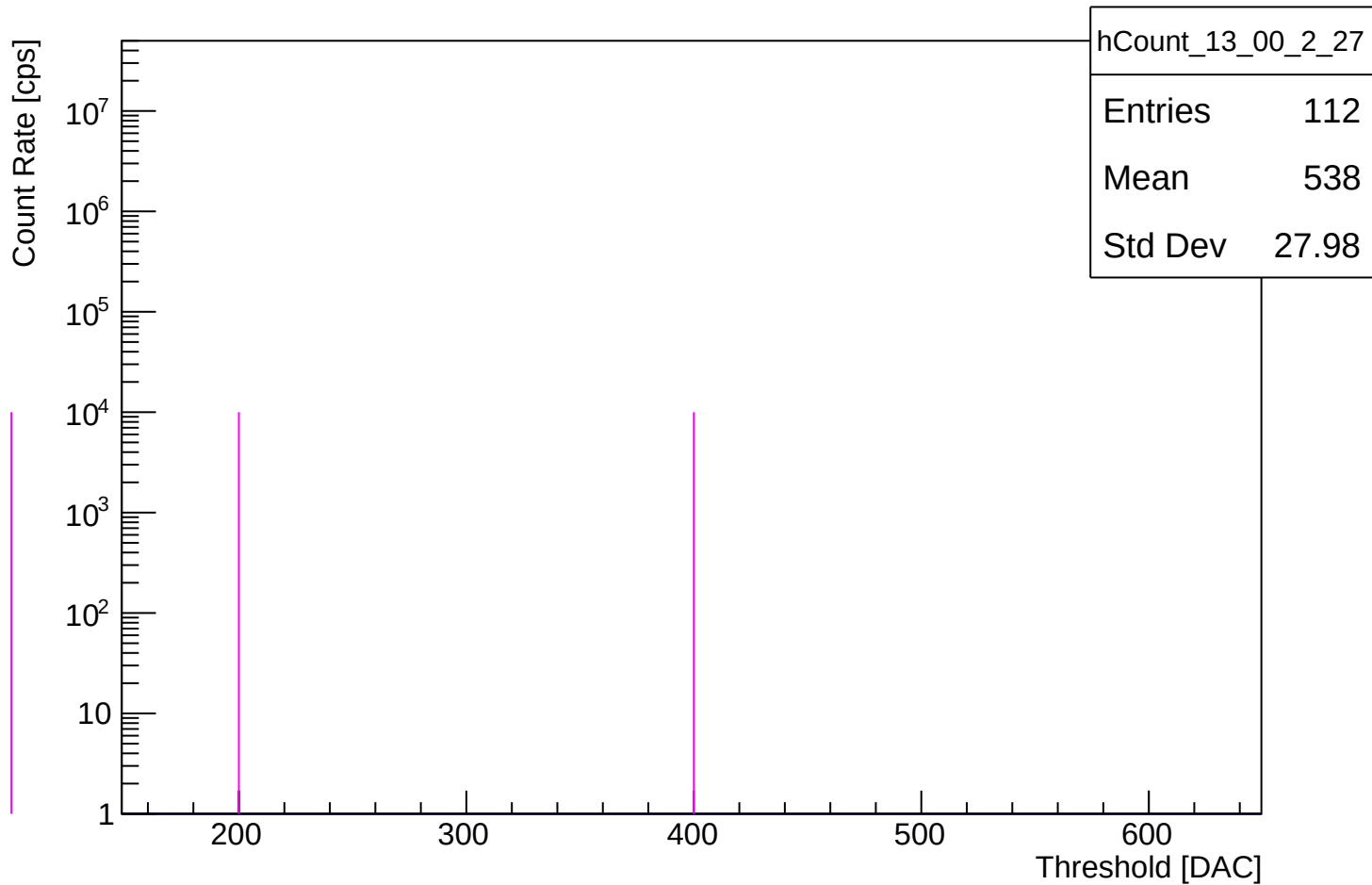


Row 1 Tile 1 Pmt 3 Pixel 8 Slot 13 Fiber 0 Asic 2 Channel 35

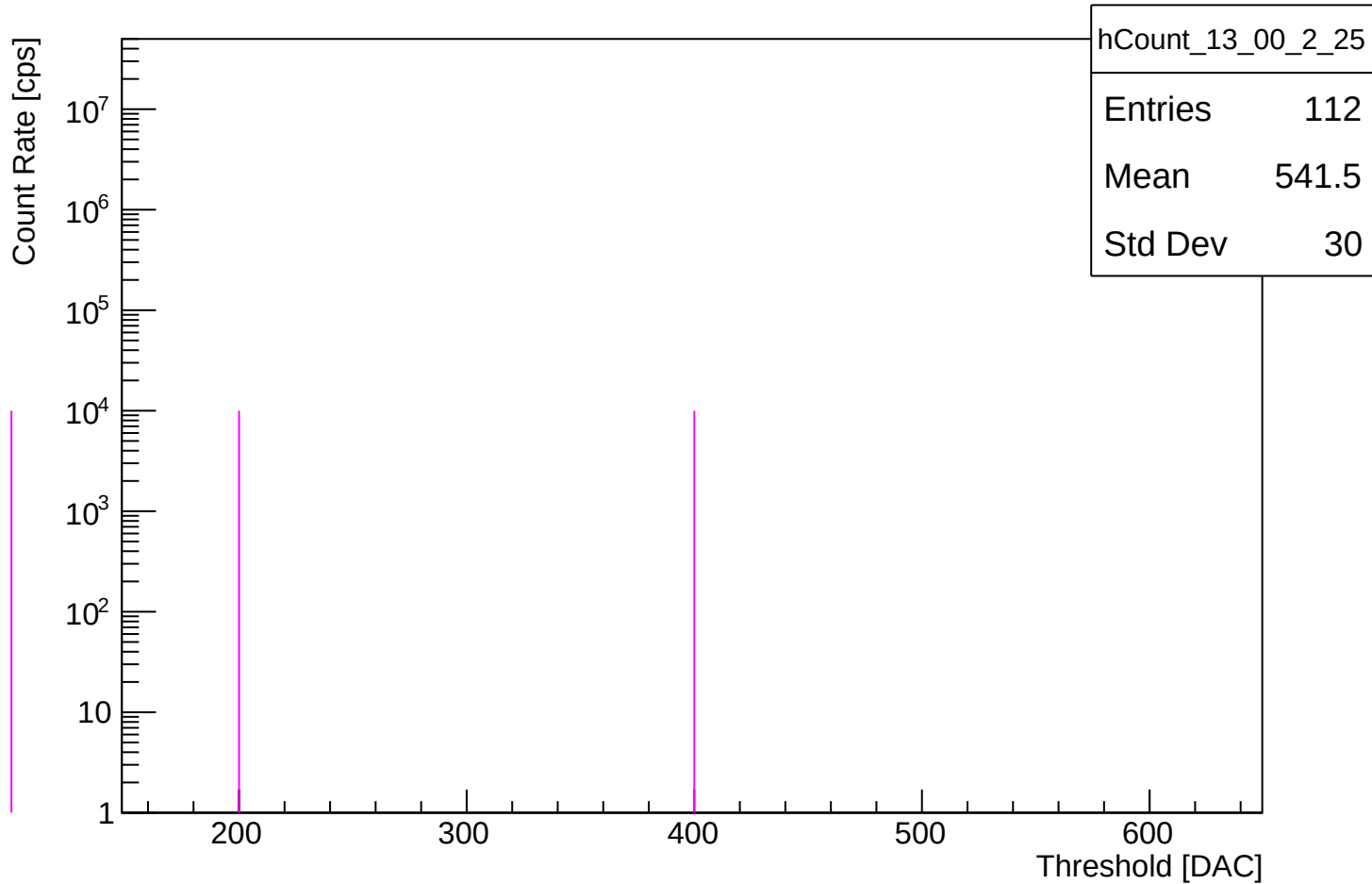




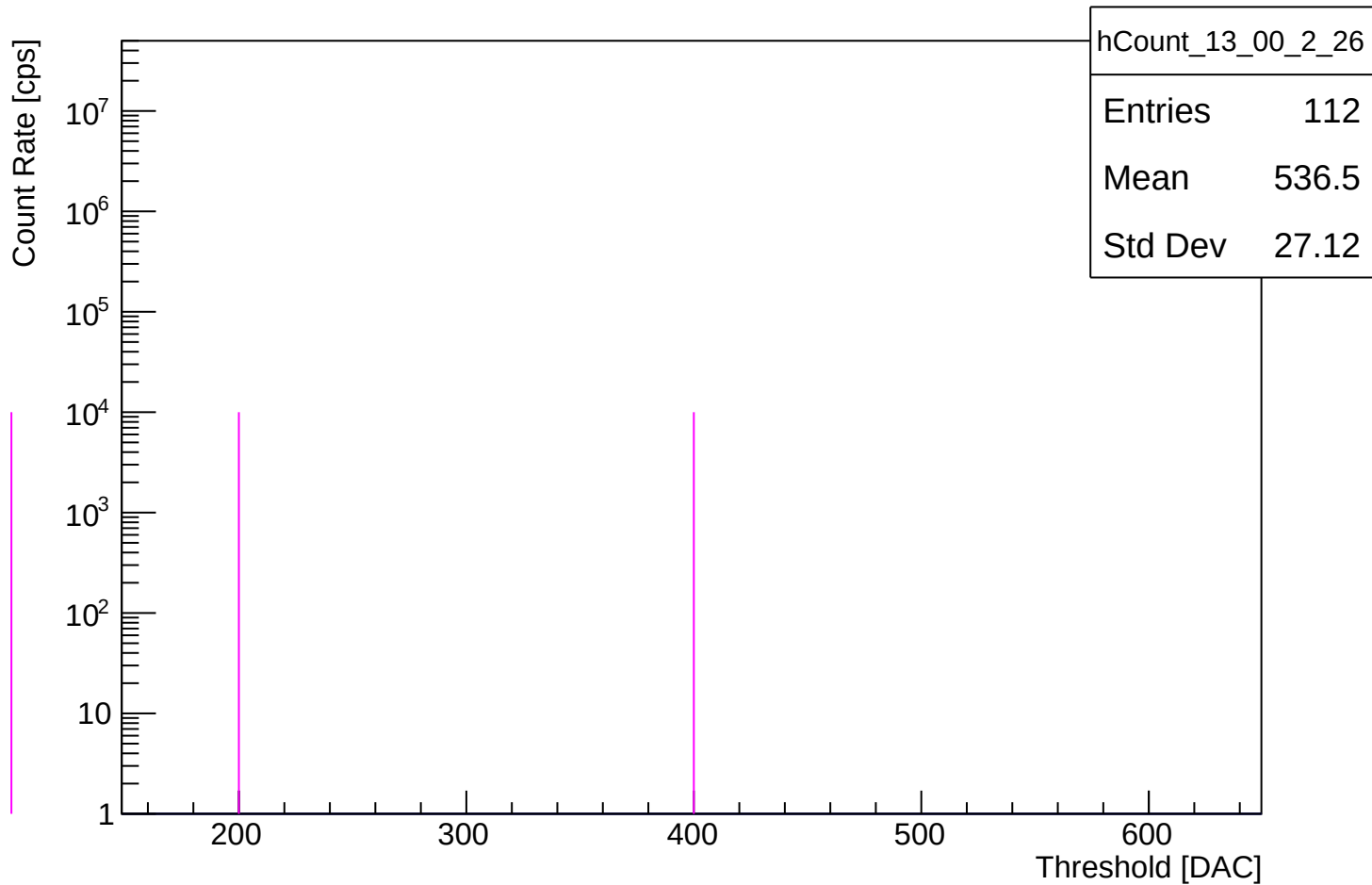
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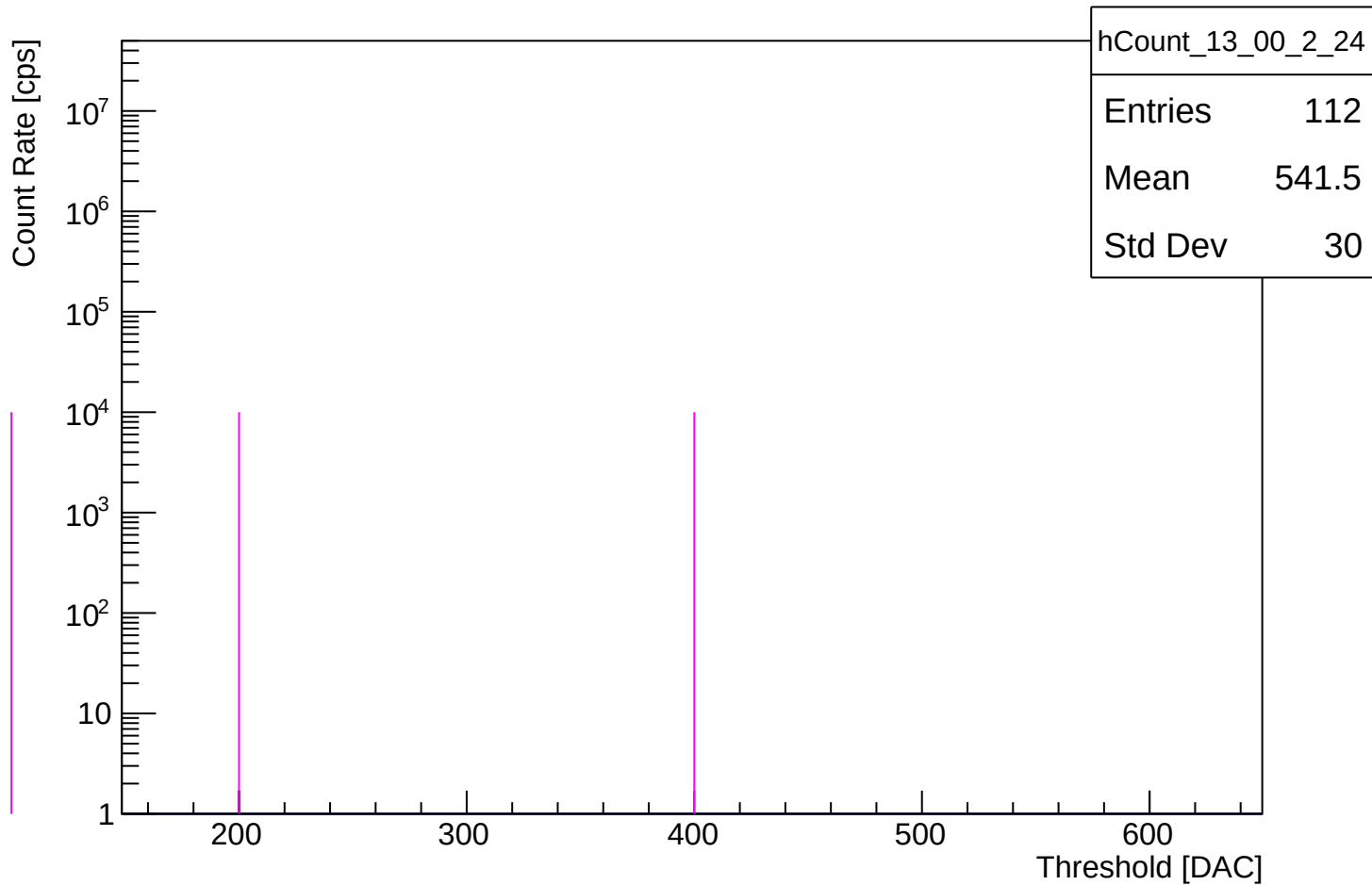
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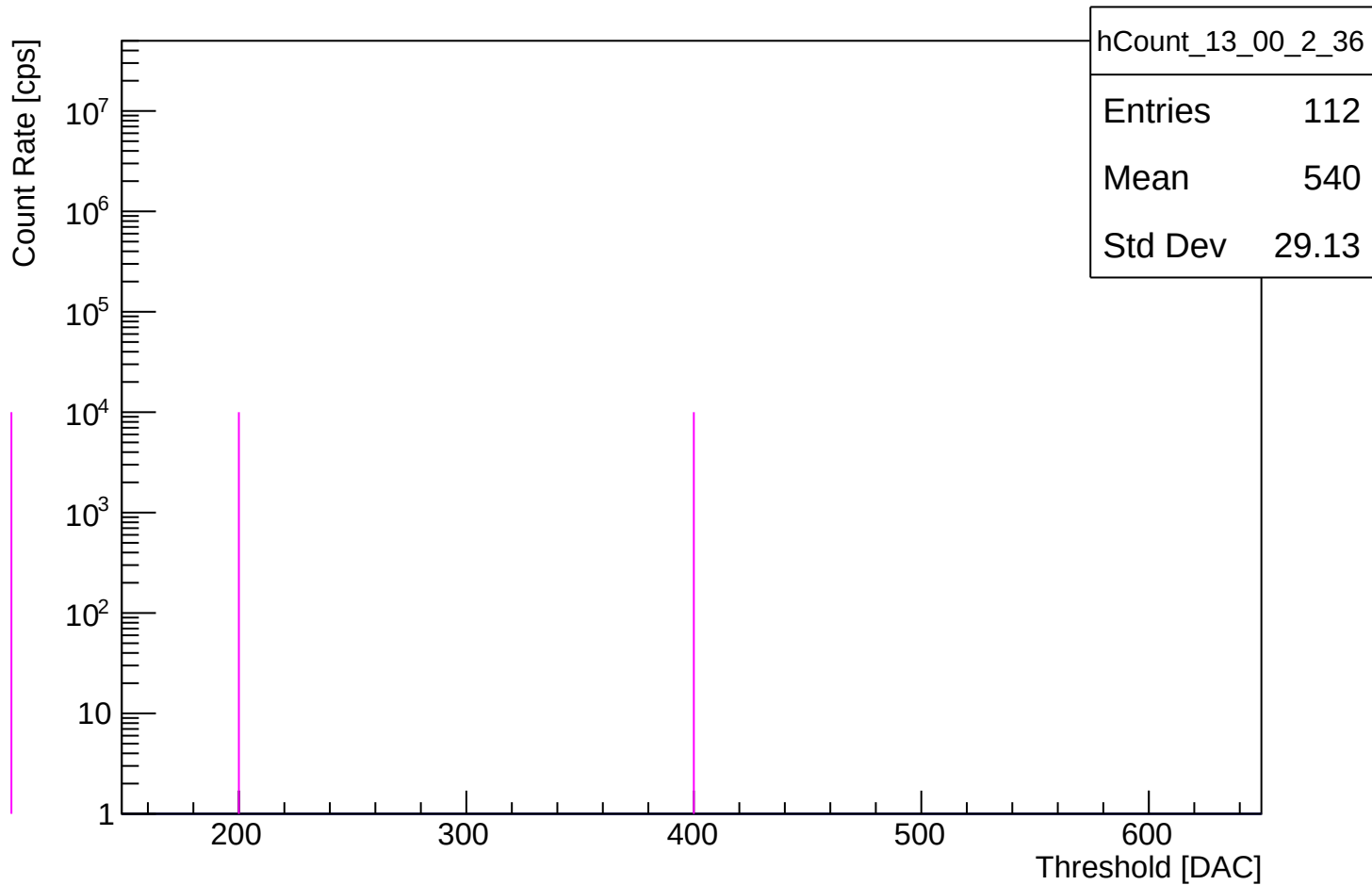
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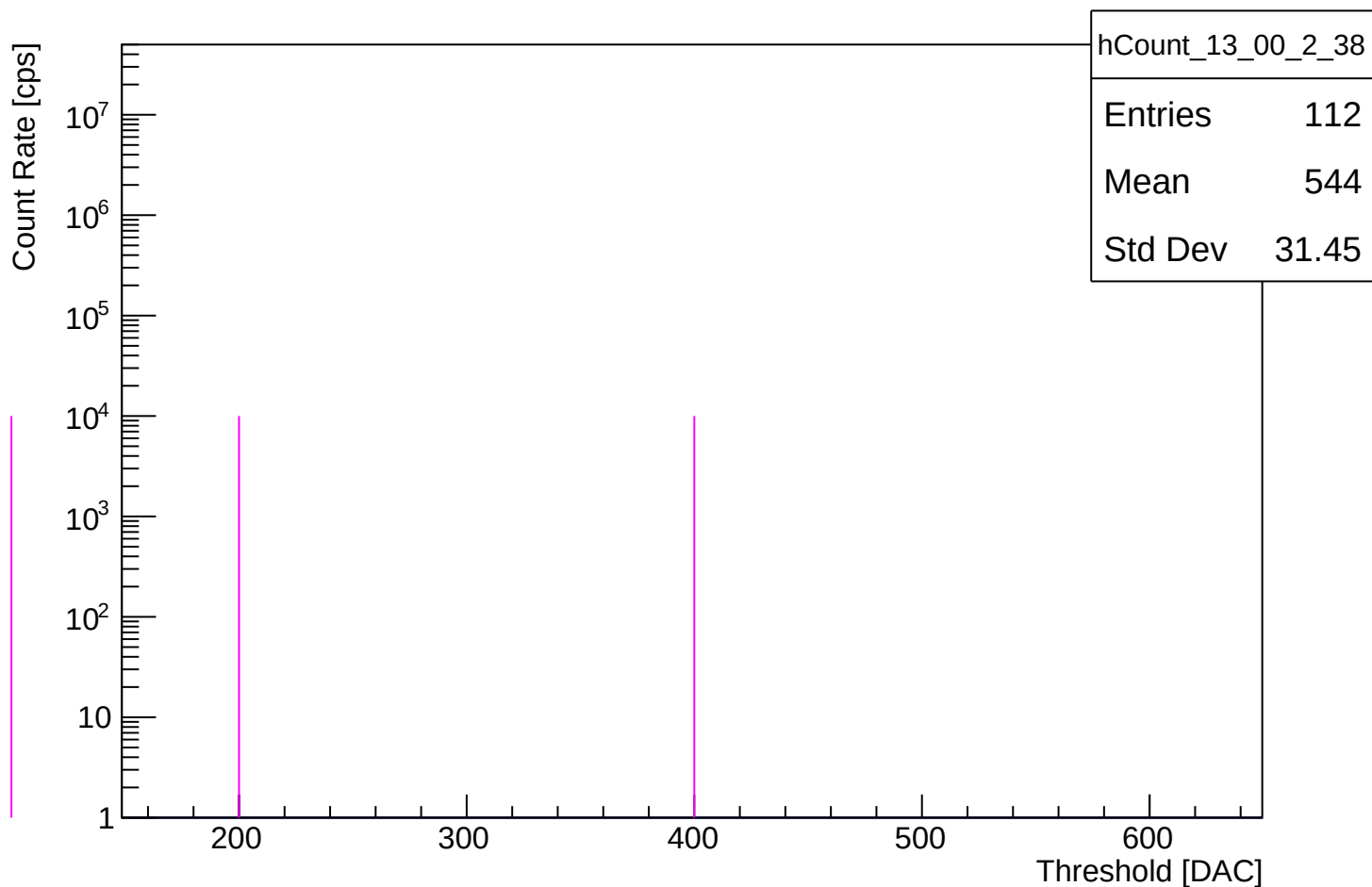
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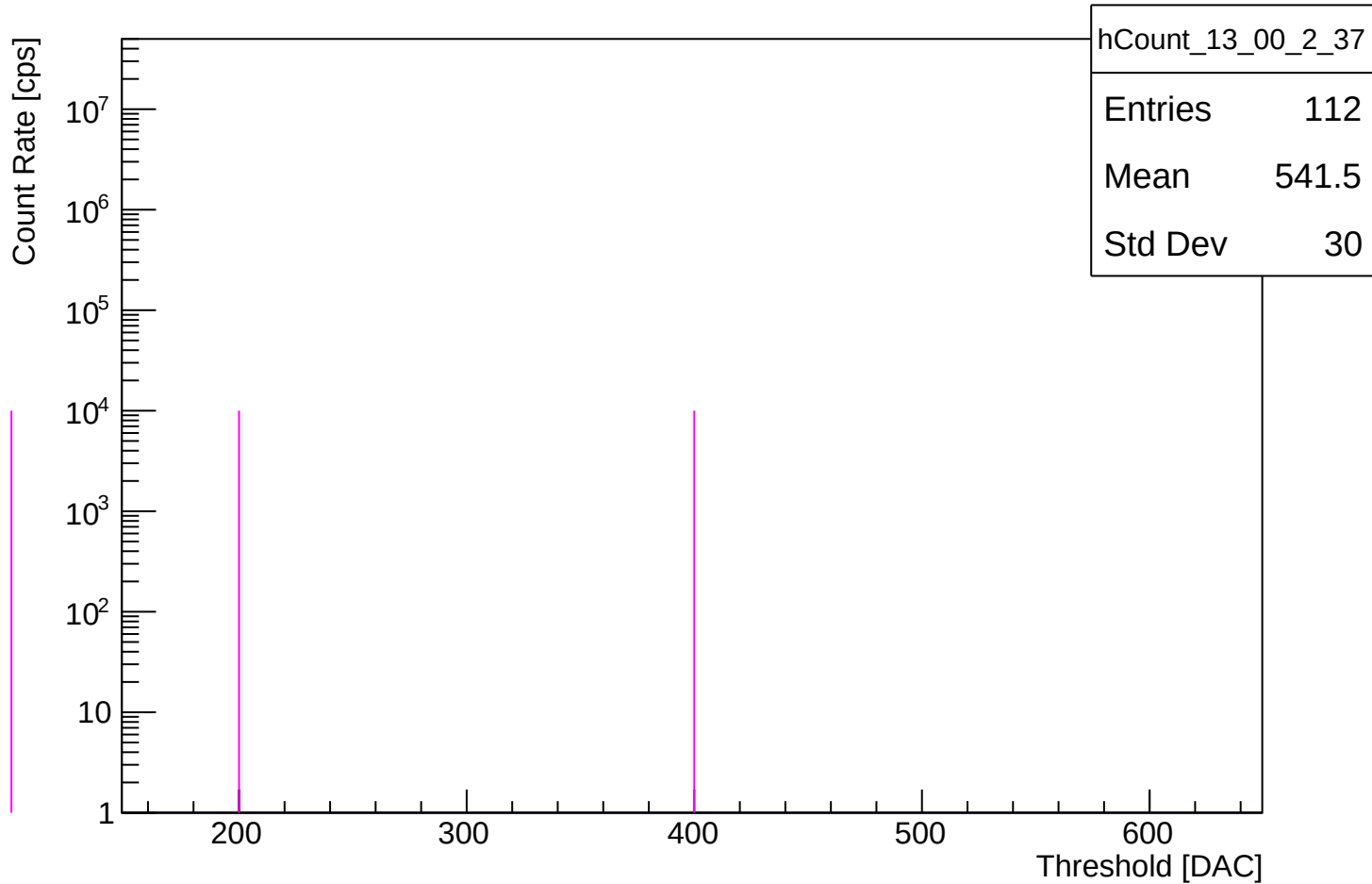
Row 1 Tile 1 Pmt 3 Pixel 13 Slot 13 Fiber 0 Asic 2 Channel 36



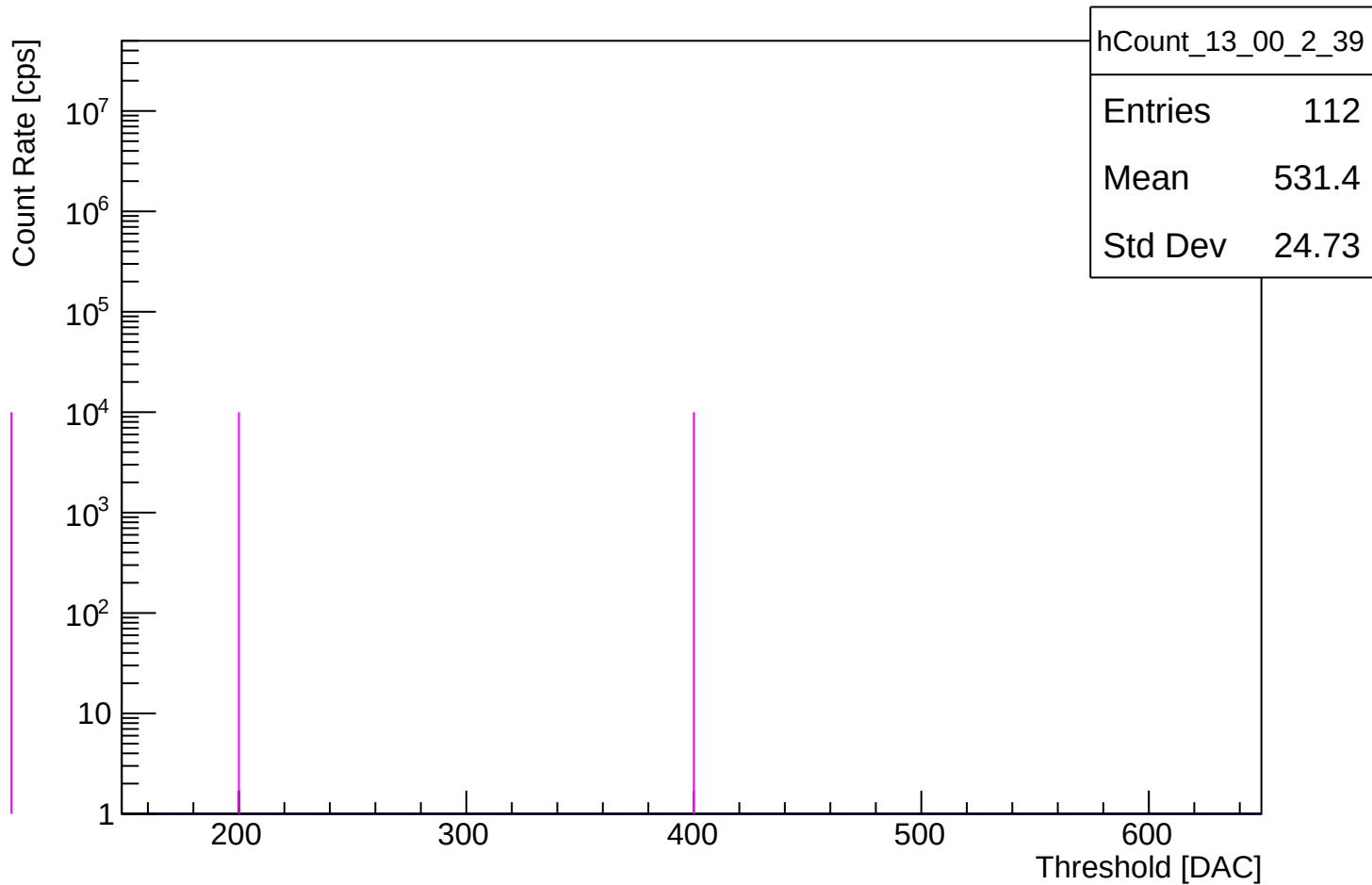
Row 1 Tile 1 Pmt 3 Pixel 14 Slot 13 Fiber 0 Asic 2 Channel 38



Row 1 Tile 1 Pmt 3 Pixel 15 Slot 13 Fiber 0 Asic 2 Channel 37

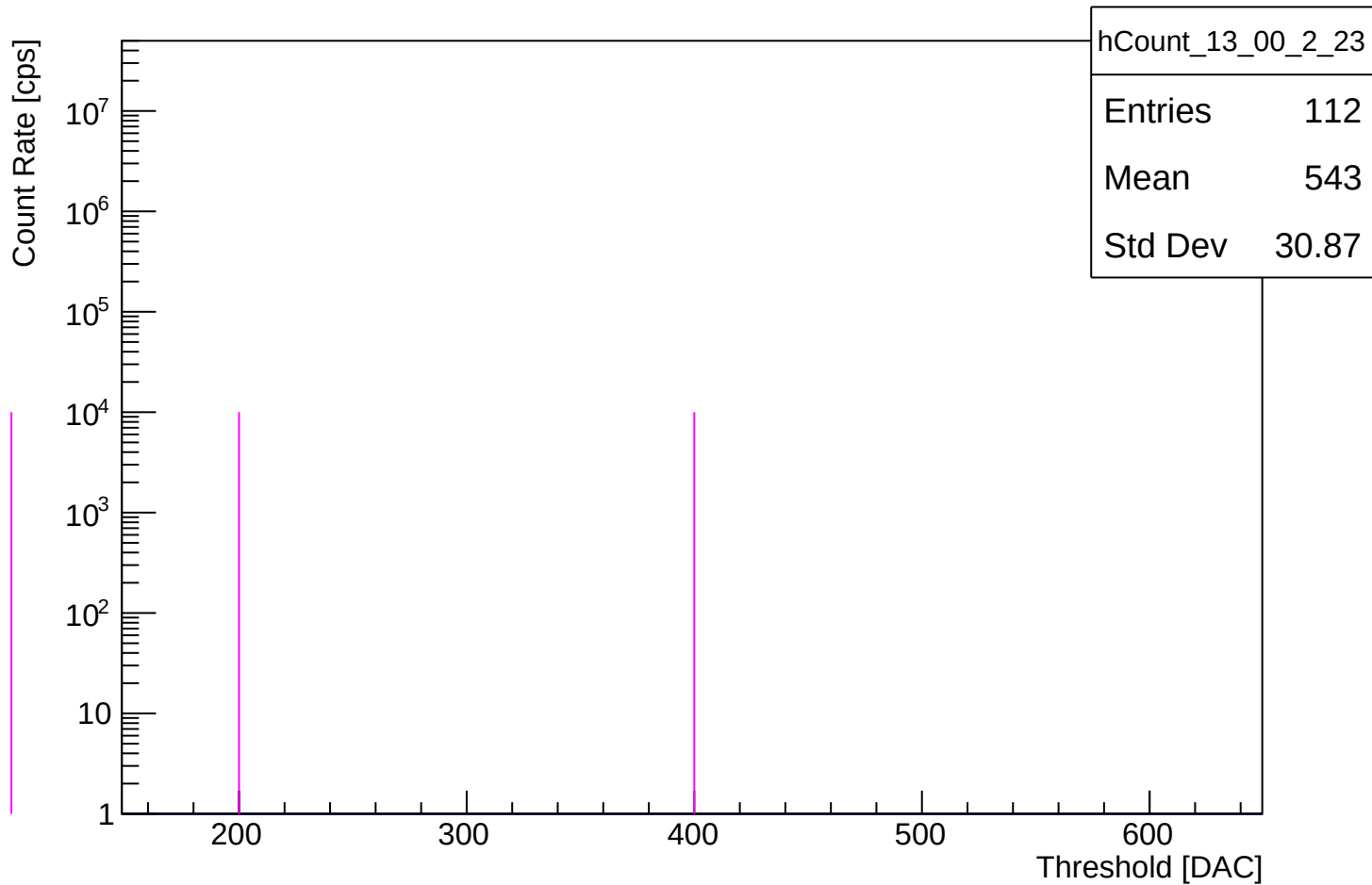


Row 1 Tile 1 Pmt 3 Pixel 16 Slot 13 Fiber 0 Asic 2 Channel 39

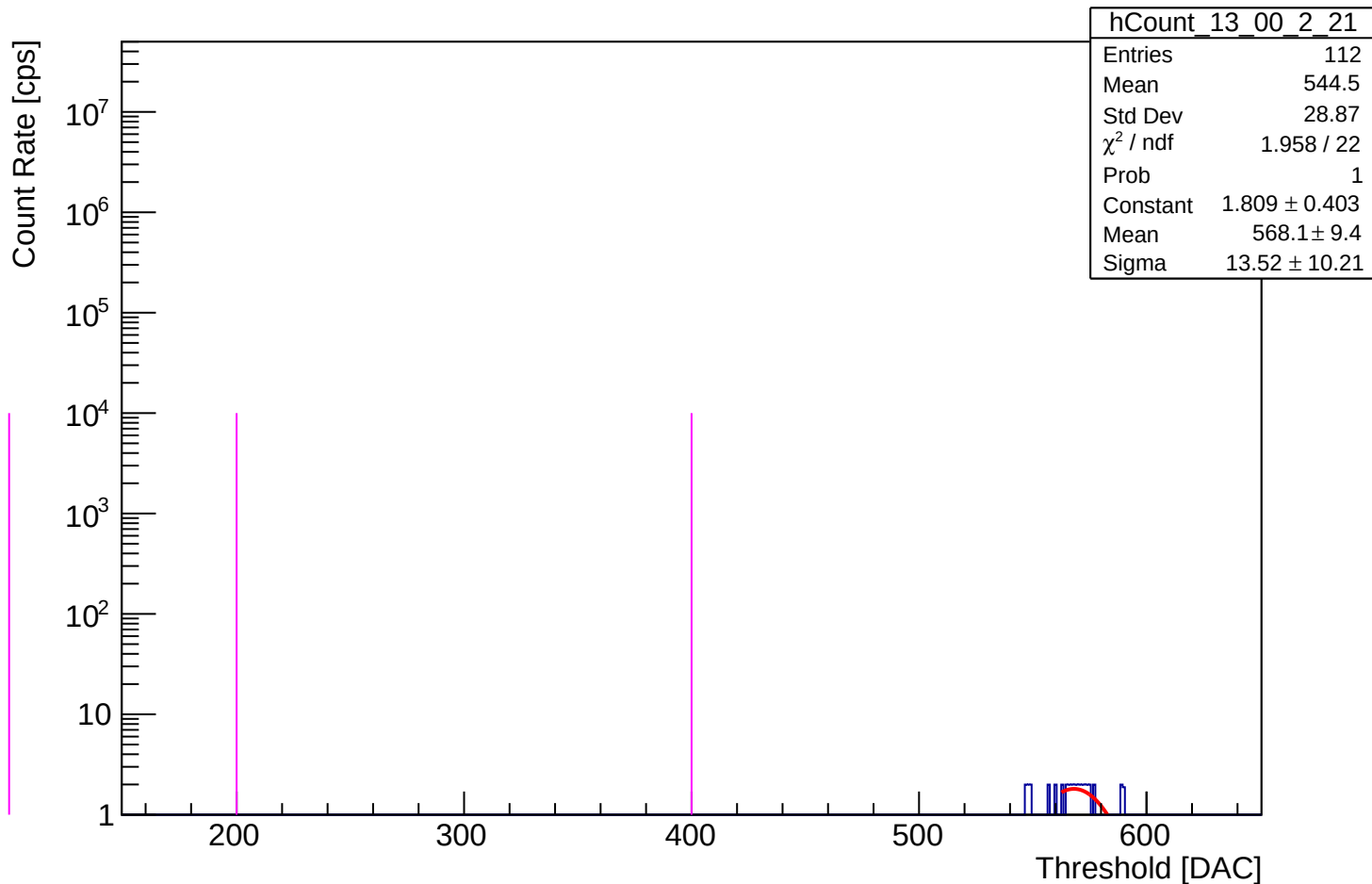




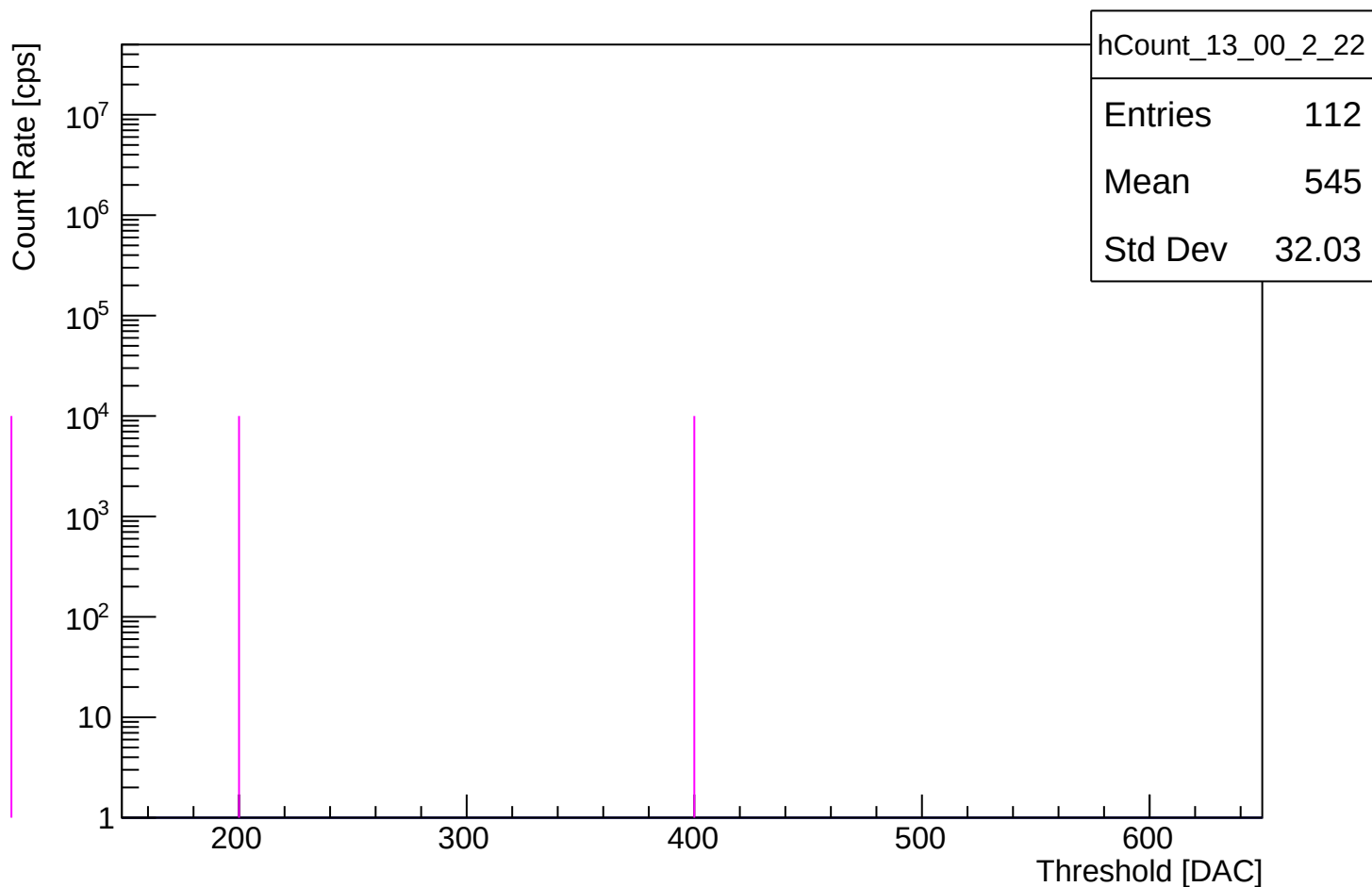
Row 1 Tile 1 Pmt 3 Pixel 17 Slot 13 Fiber 0 Asic 2 Channel 23



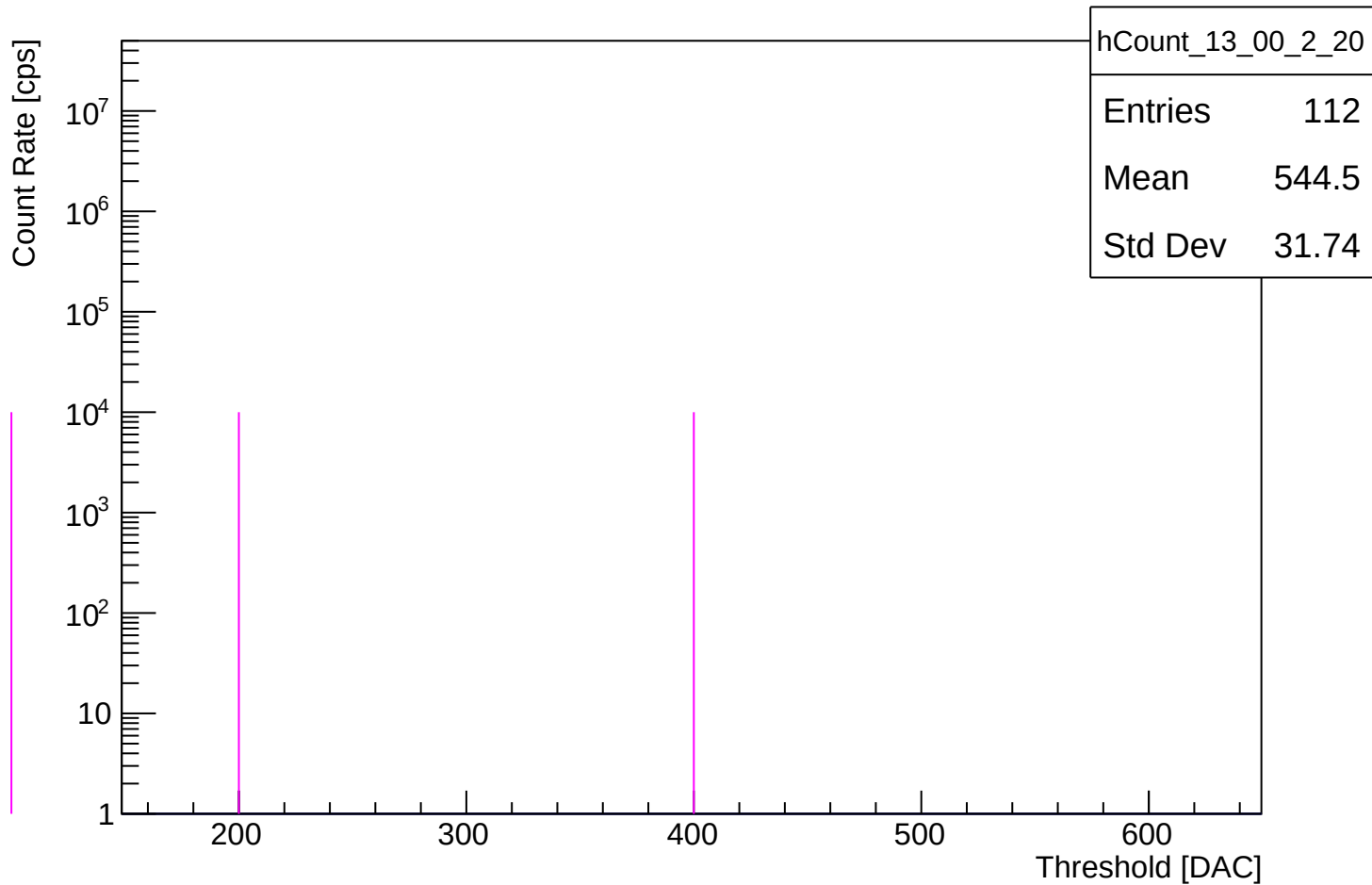
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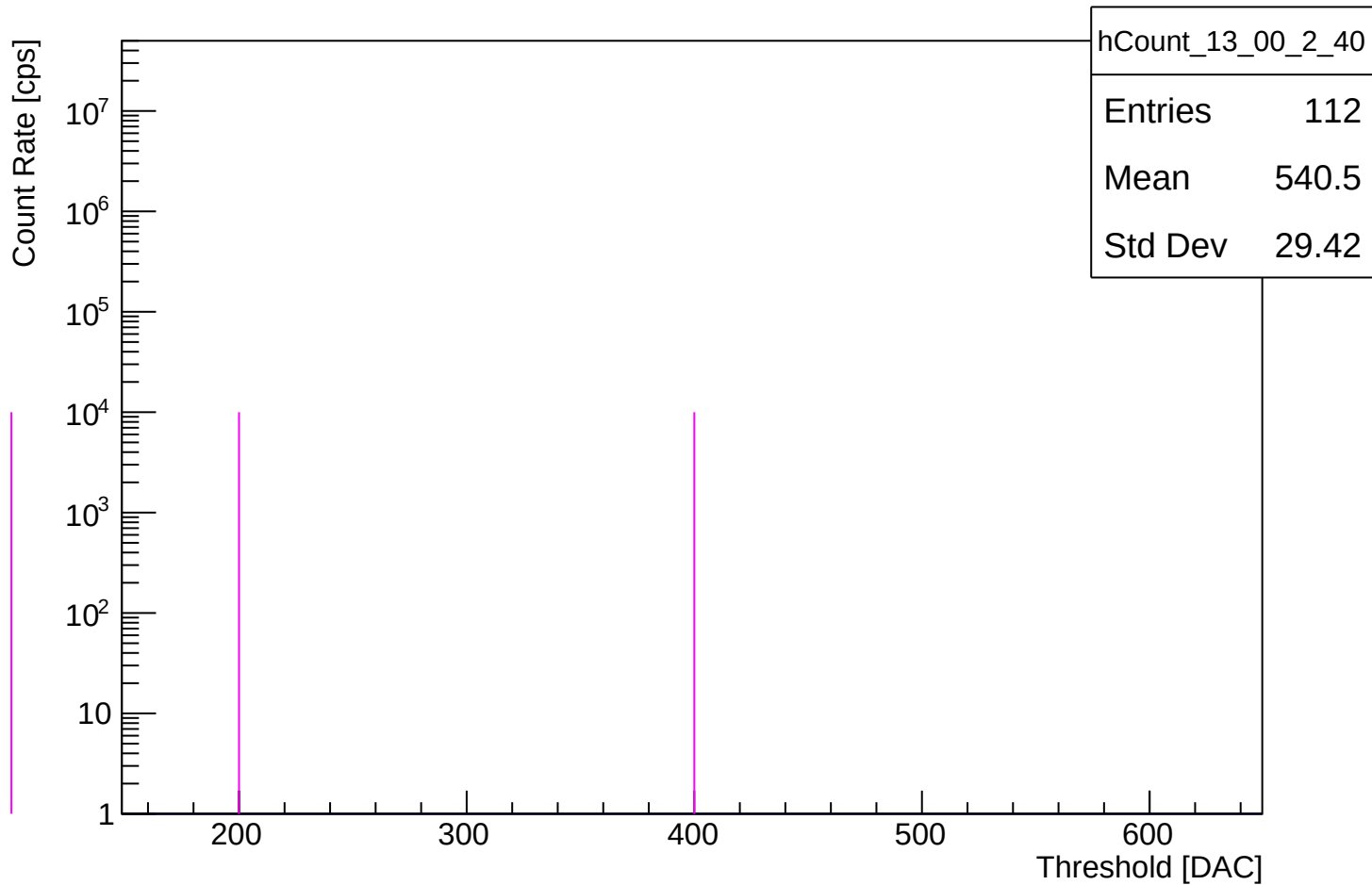
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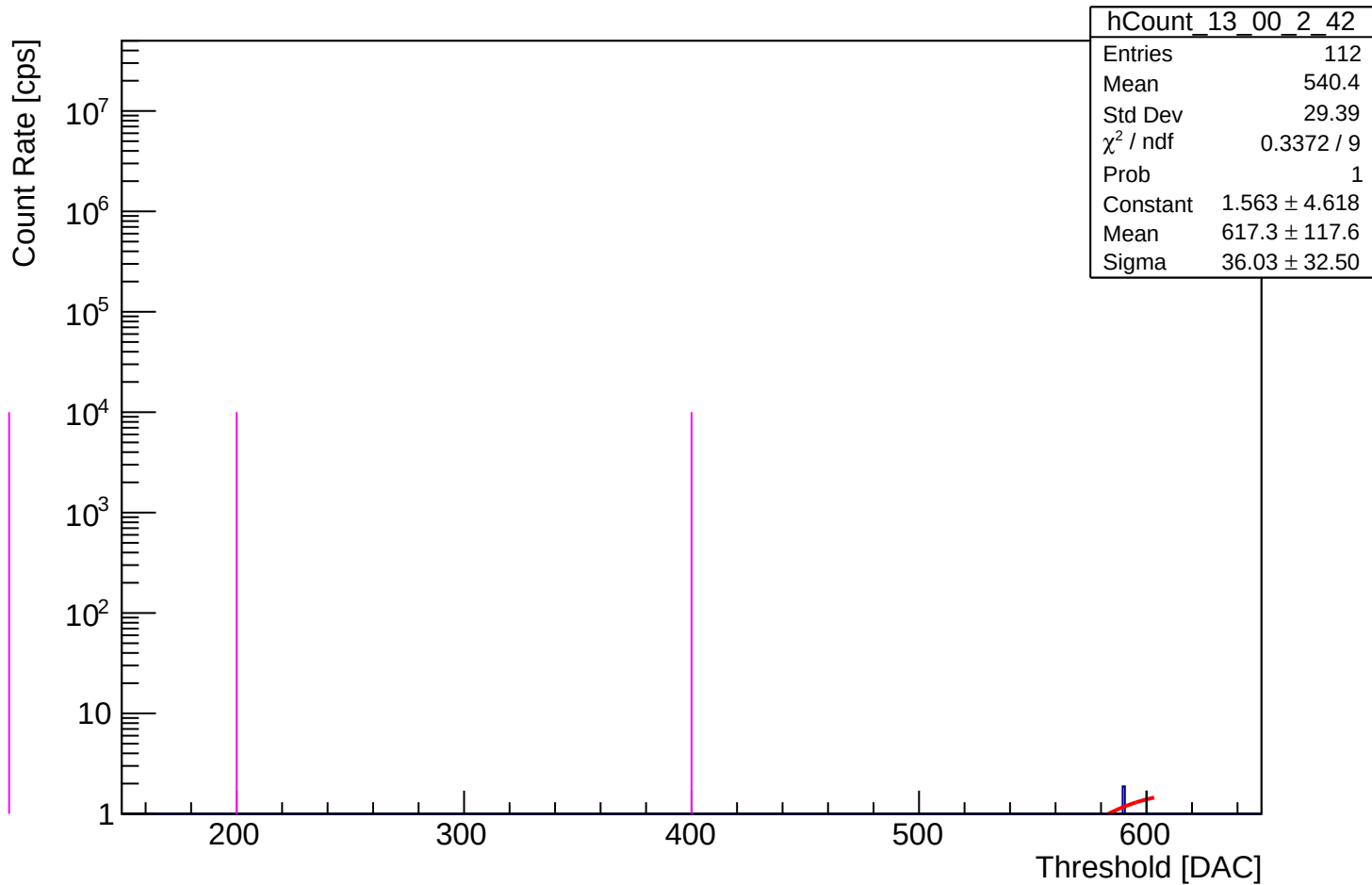
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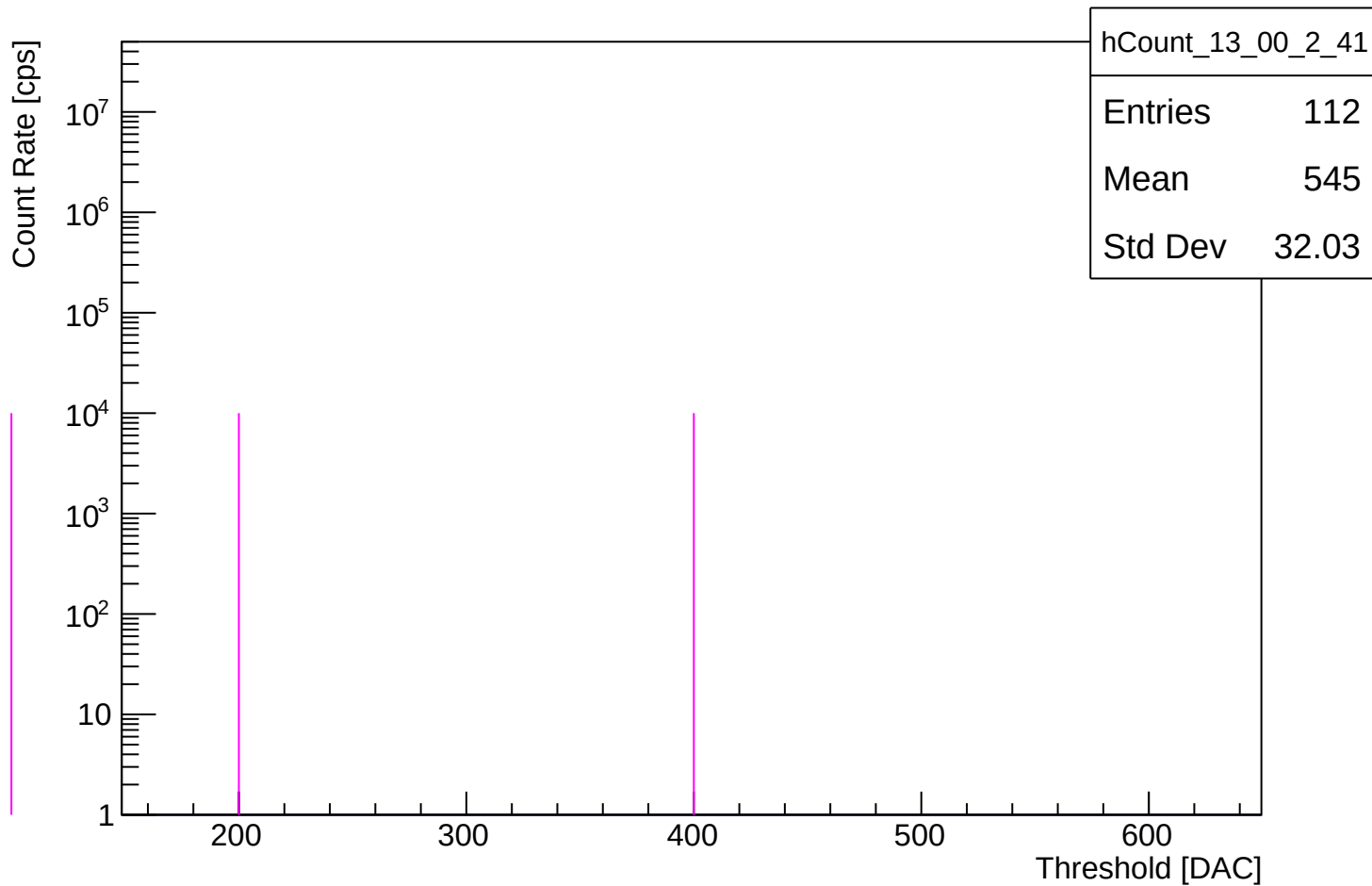
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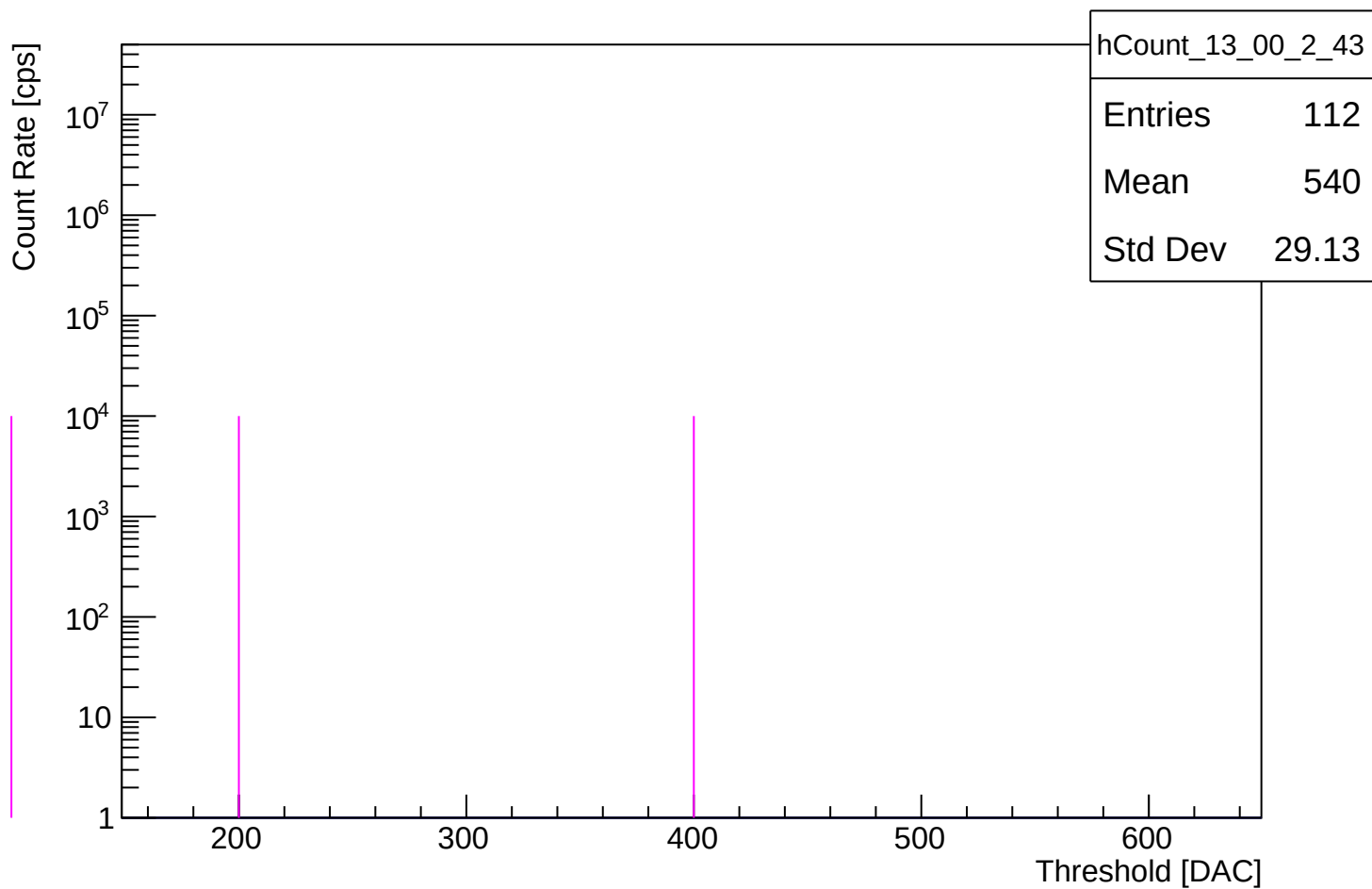
Row 1 Tile 1 Pmt 3 Pixel 22 Slot 13 Fiber 0 Asic 2 Channel 42



Row 1 Tile 1 Pmt 3 Pixel 23 Slot 13 Fiber 0 Asic 2 Channel 41

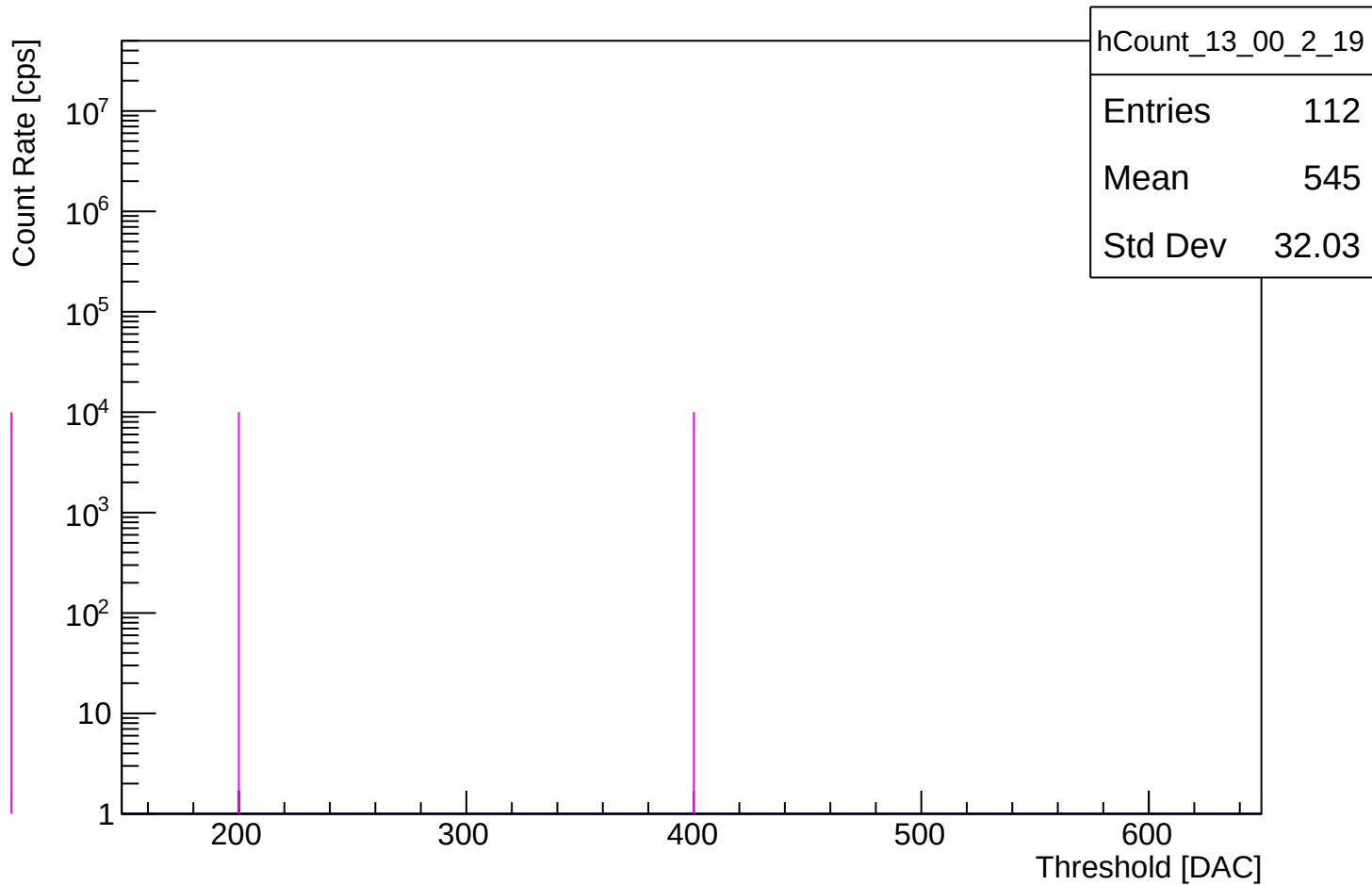


Row 1 Tile 1 Pmt 3 Pixel 24 Slot 13 Fiber 0 Asic 2 Channel 43

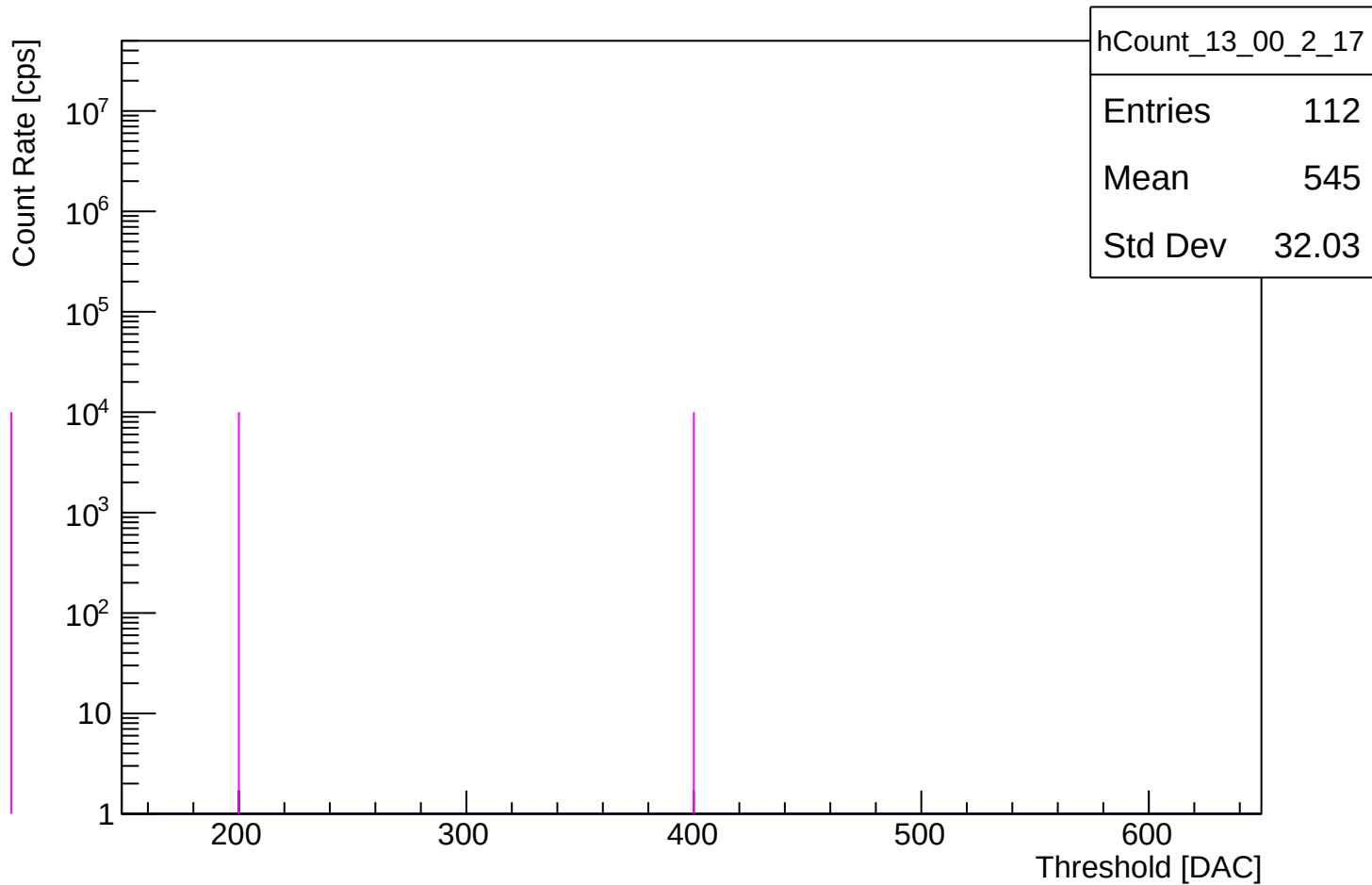




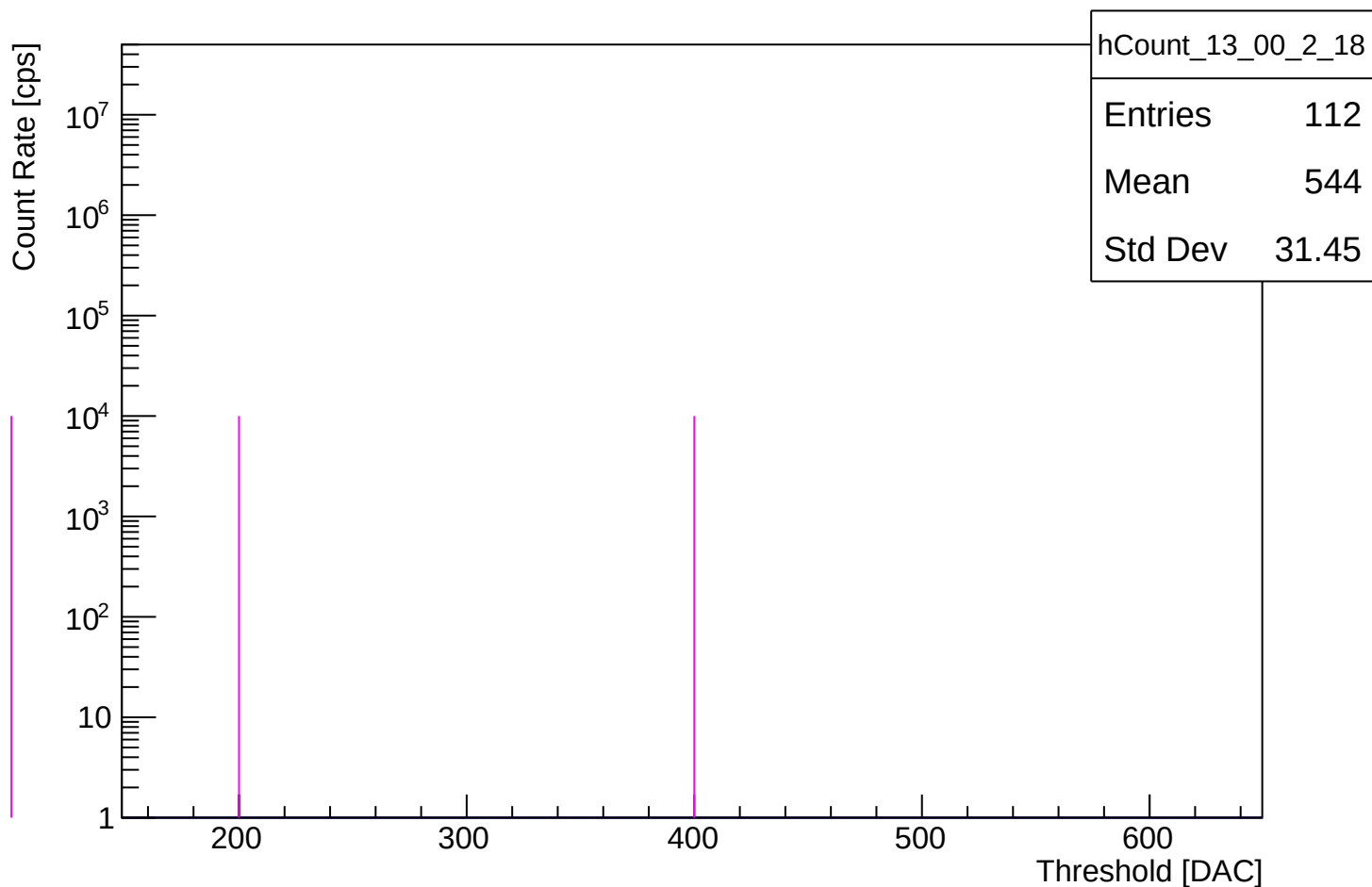
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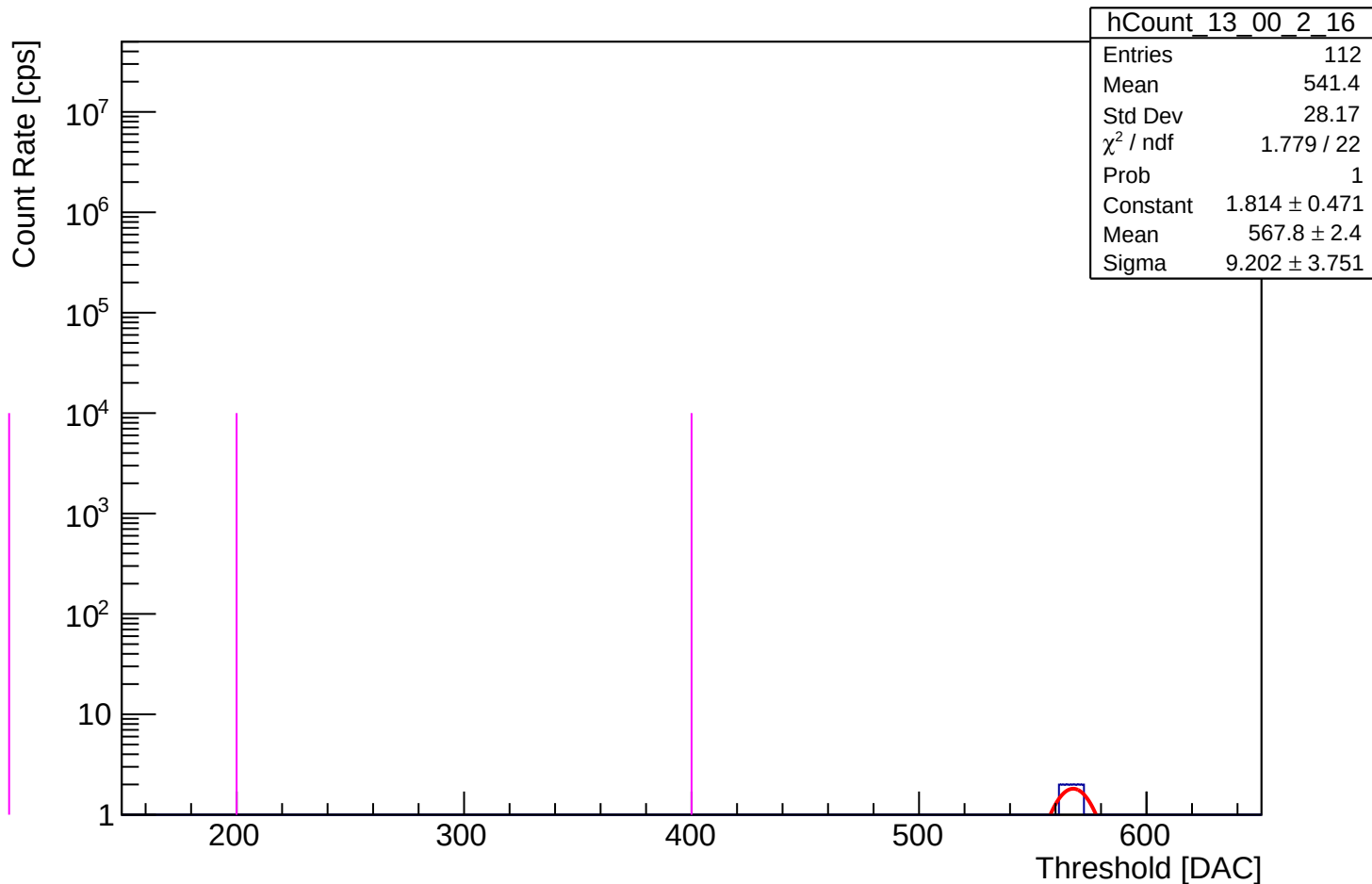
Row 1 Tile 1 Pmt 3 Pixel 26 Slot 13 Fiber 0 Asic 2 Channel 17



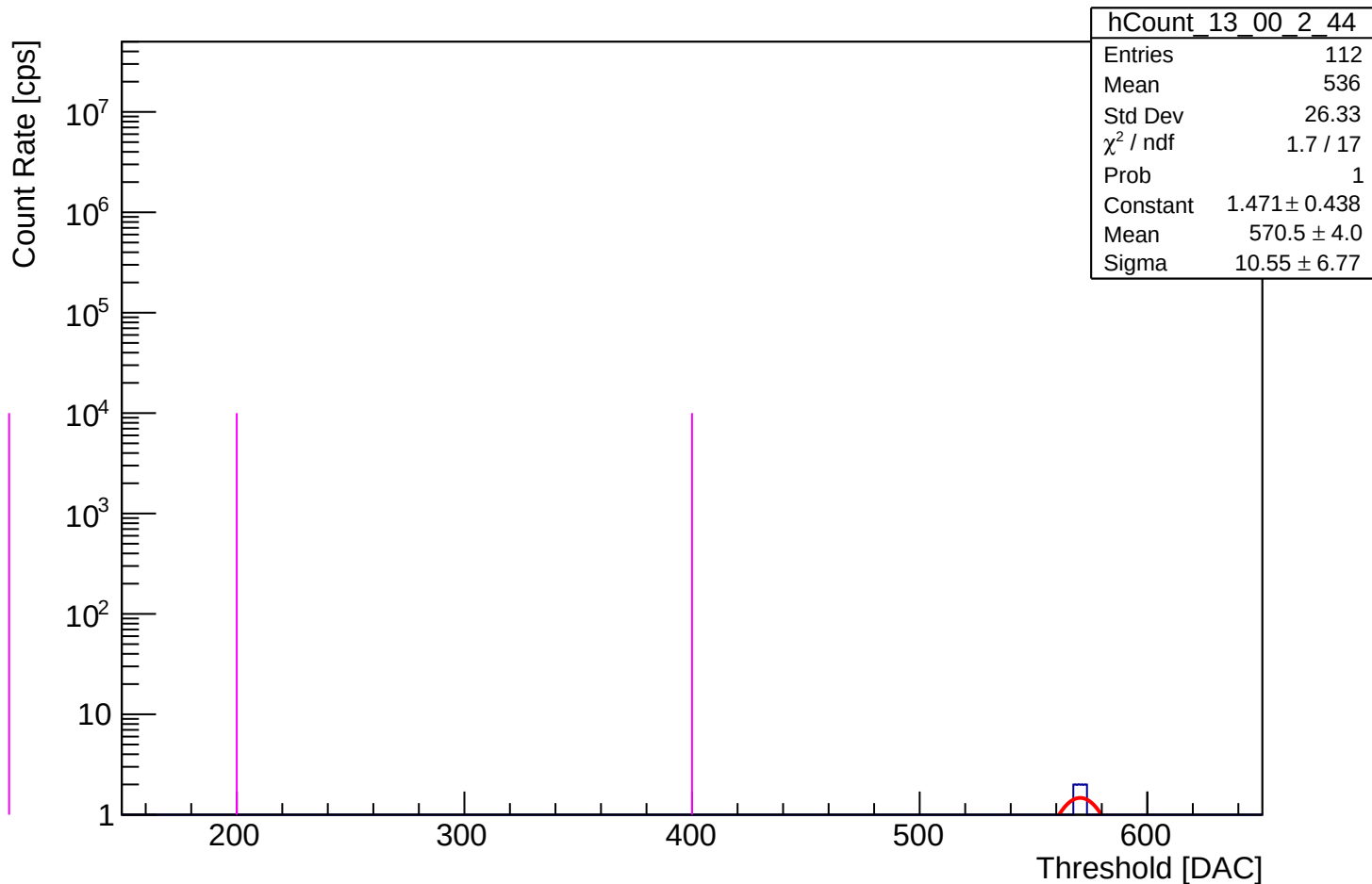
Row 1 Tile 1 Pmt 3 Pixel 27 Slot 13 Fiber 0 Asic 2 Channel 18



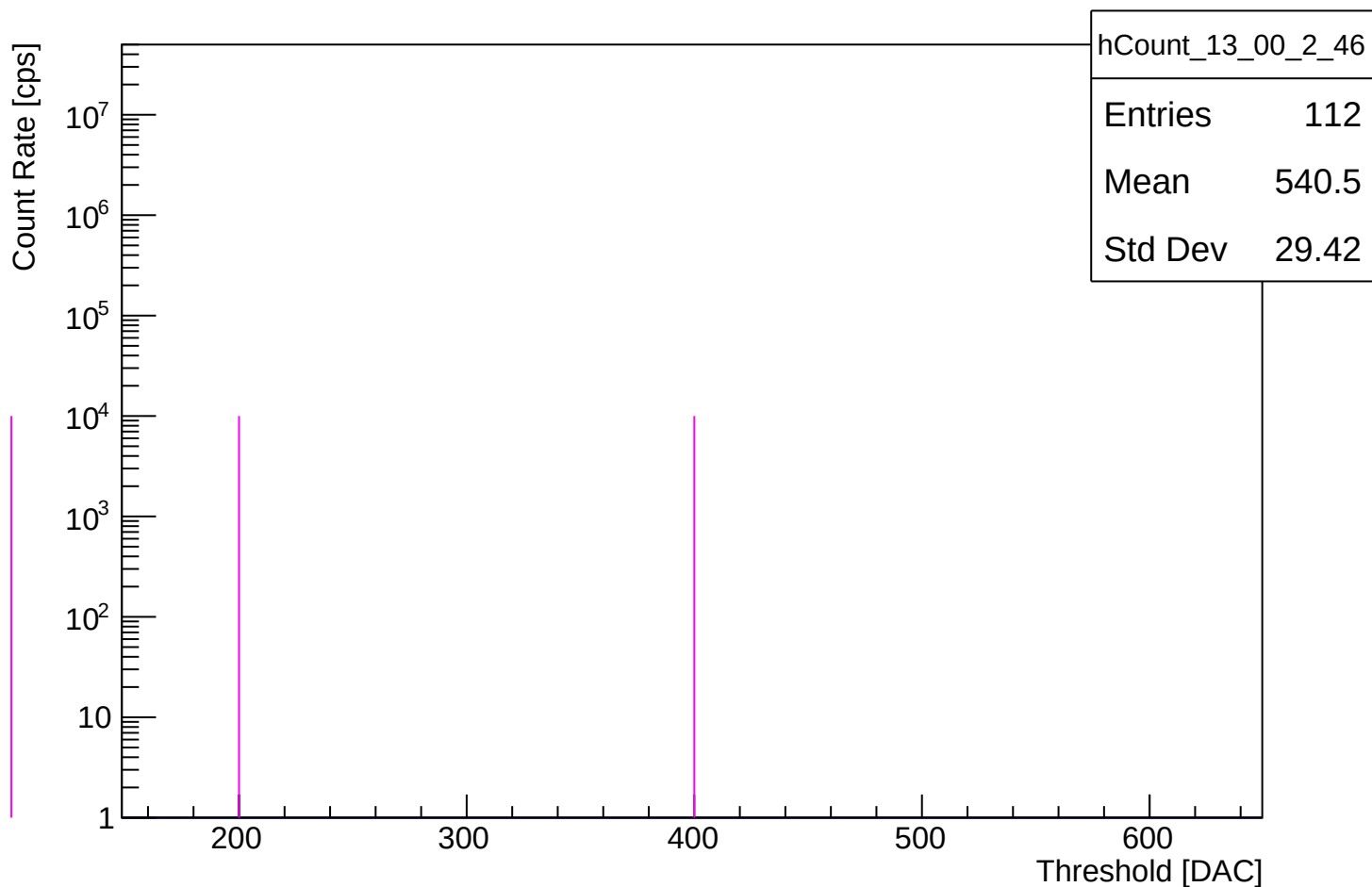
Row 1 Tile 1 Pmt 3 Pixel 28 Slot 13 Fiber 0 Asic 2 Channel 16



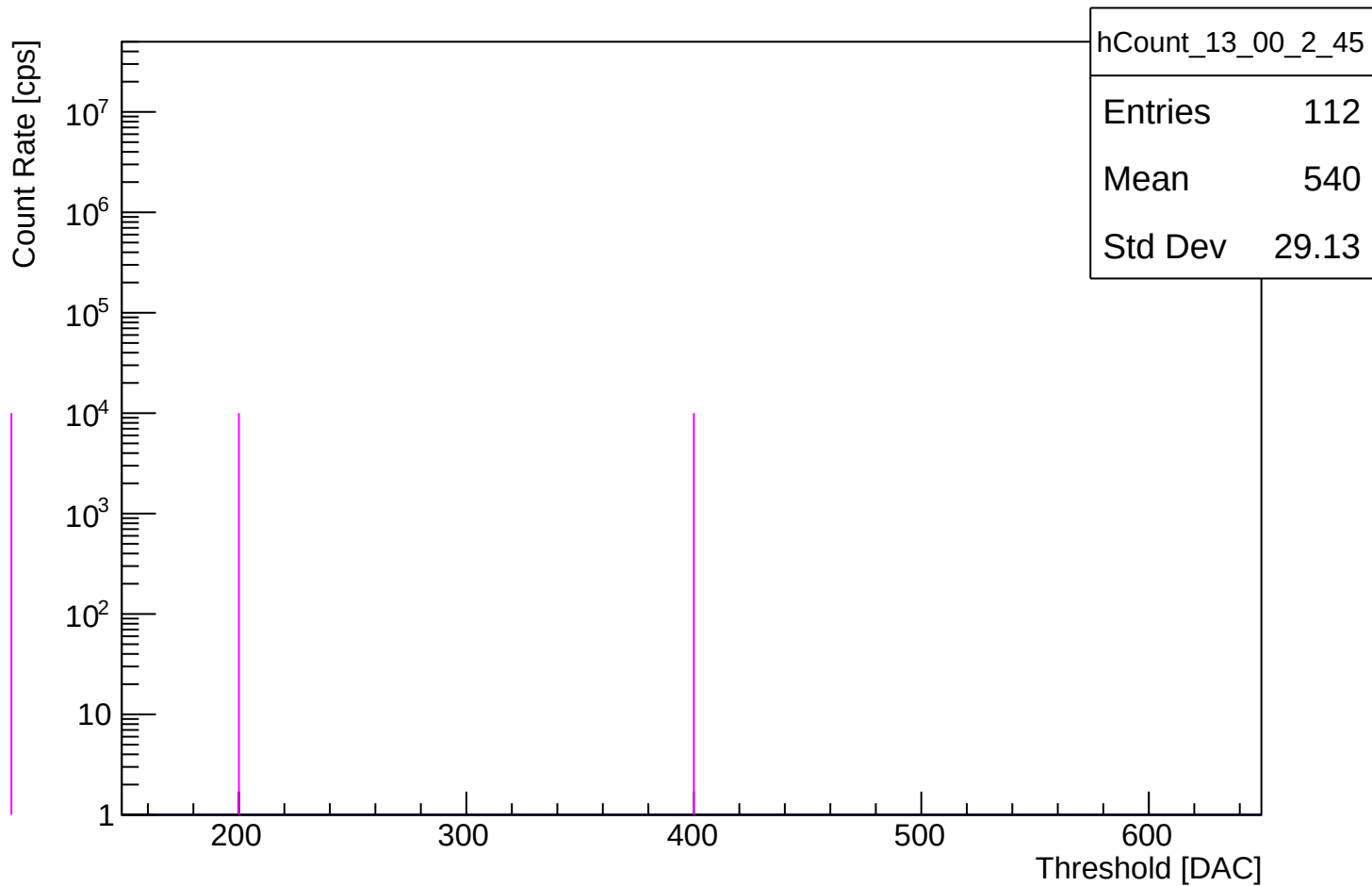
Row 1 Tile 1 Pmt 3 Pixel 29 Slot 13 Fiber 0 Asic 2 Channel 44



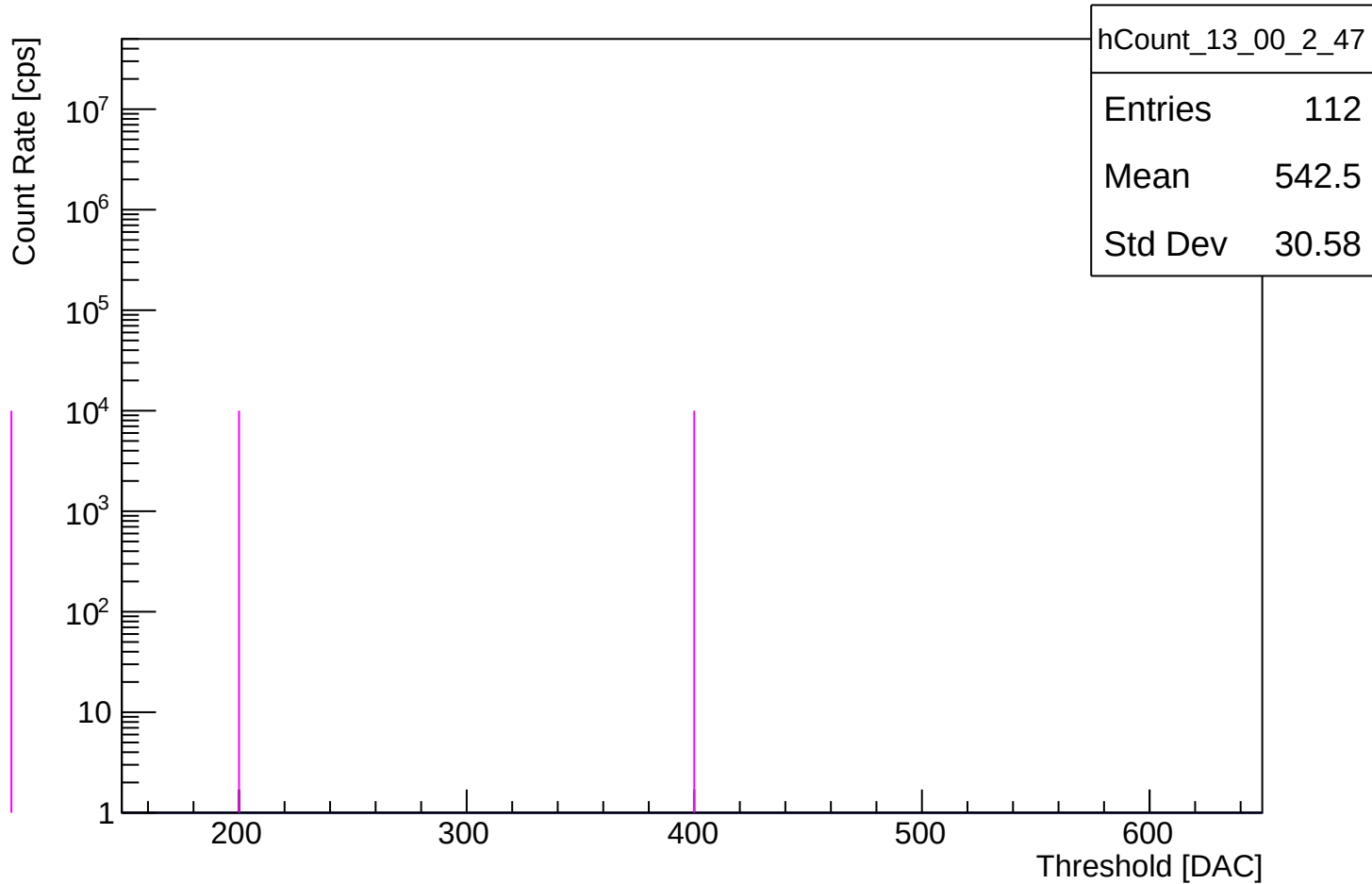
Row 1 Tile 1 Pmt 3 Pixel 30 Slot 13 Fiber 0 Asic 2 Channel 46



Row 1 Tile 1 Pmt 3 Pixel 31 Slot 13 Fiber 0 Asic 2 Channel 45

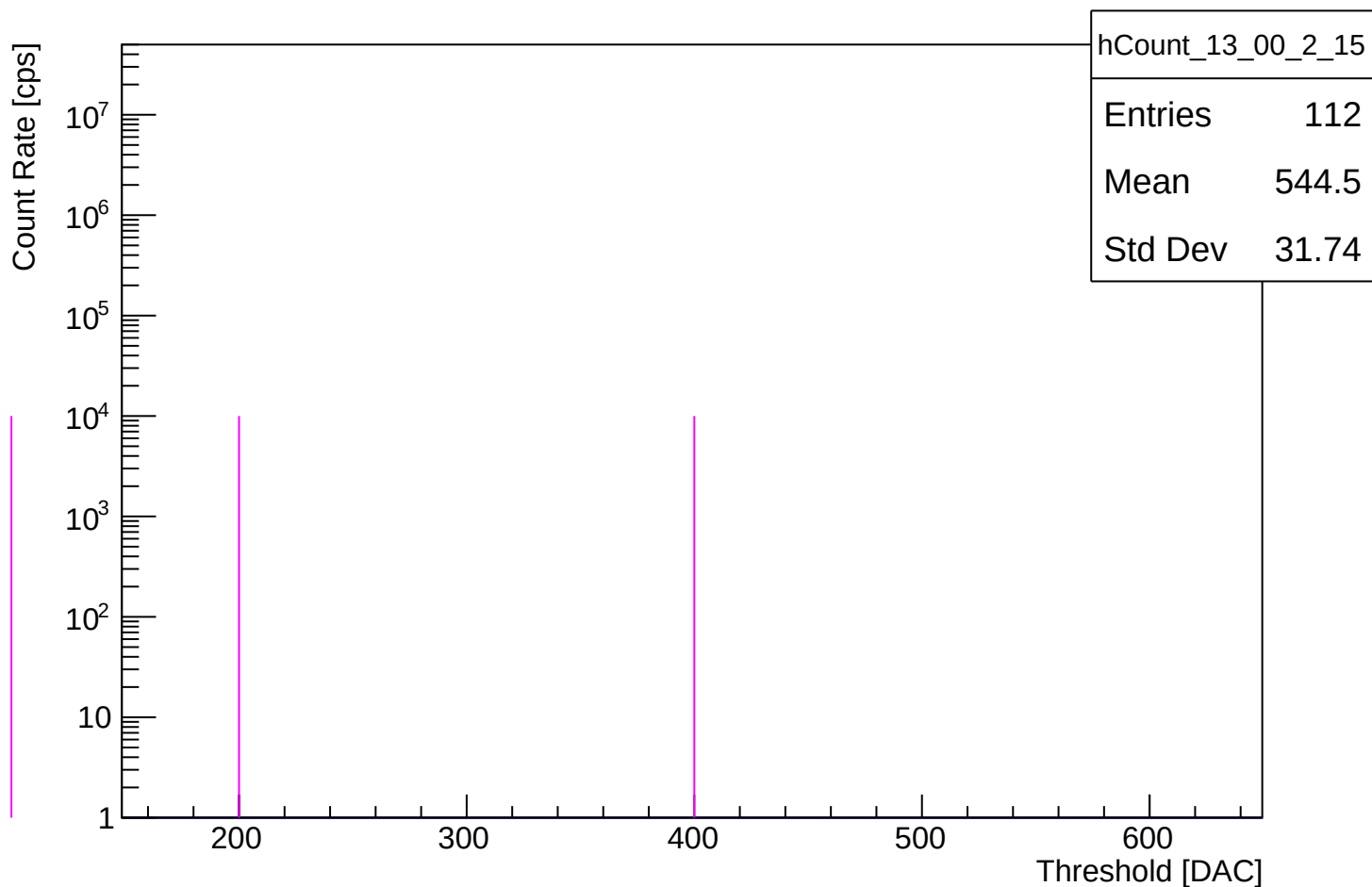


Row 1 Tile 1 Pmt 3 Pixel 32 Slot 13 Fiber 0 Asic 2 Channel 47

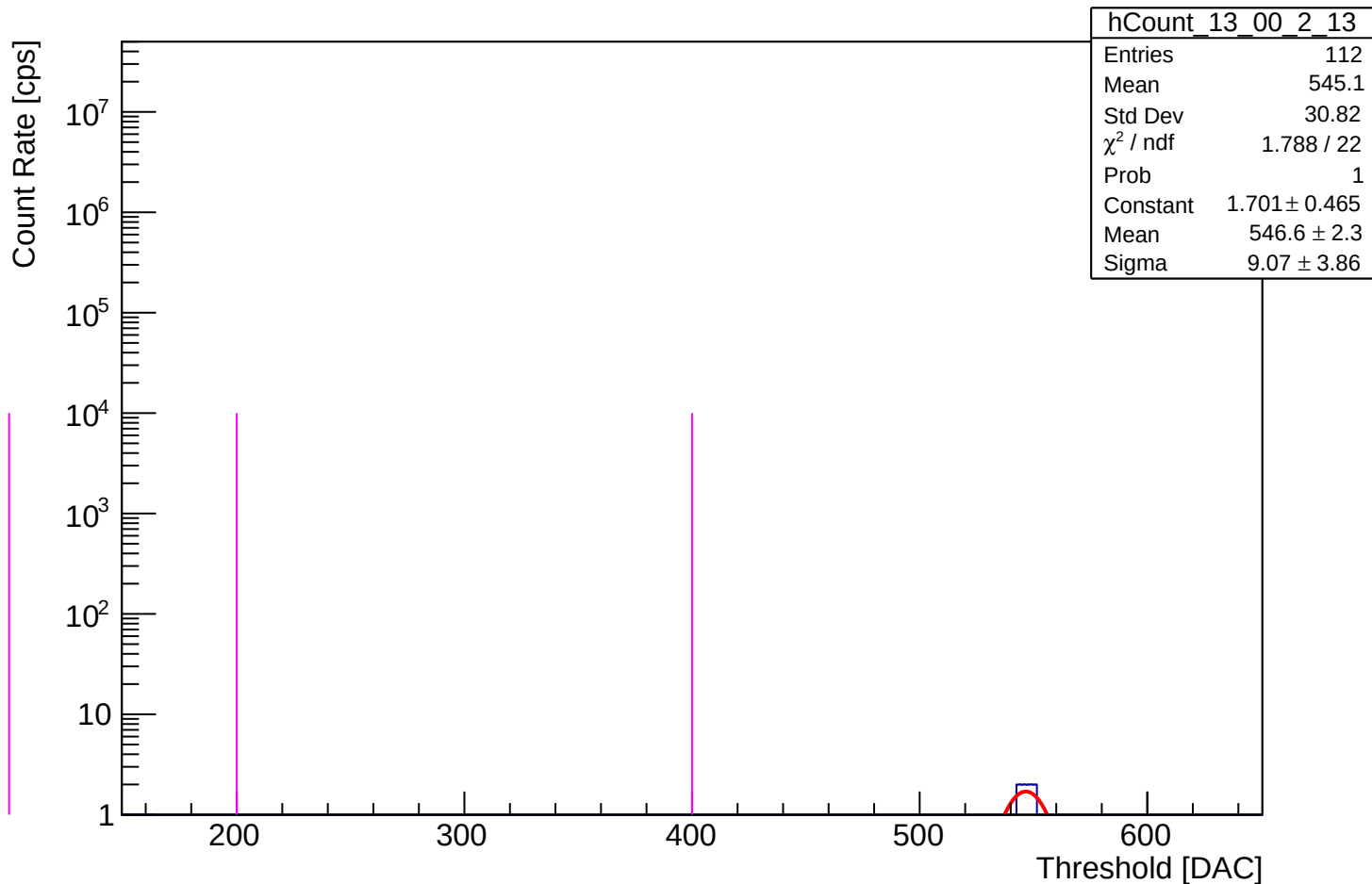




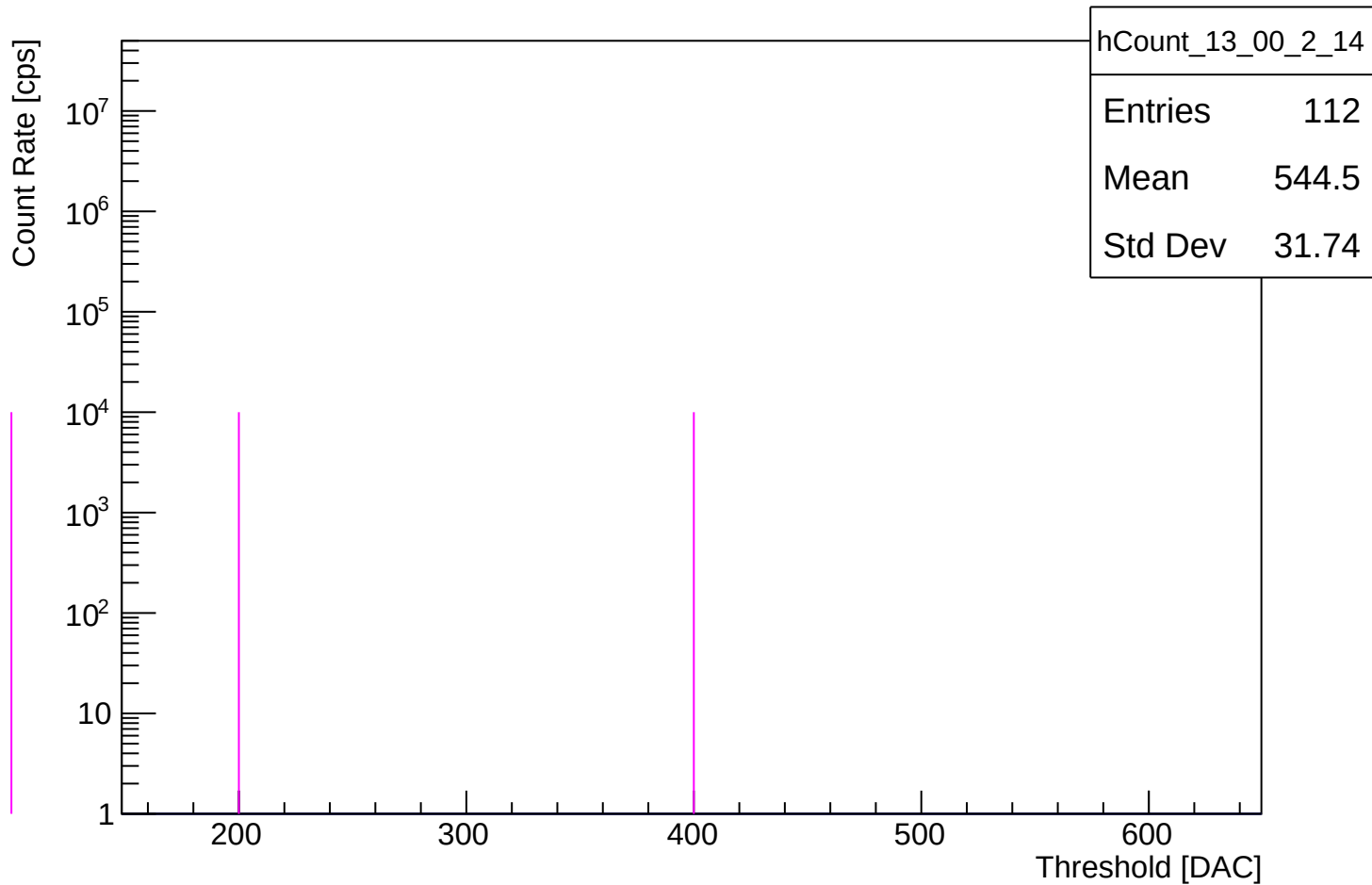
Row 1 Tile 1 Pmt 3 Pixel 33 Slot 13 Fiber 0 Asic 2 Channel 15



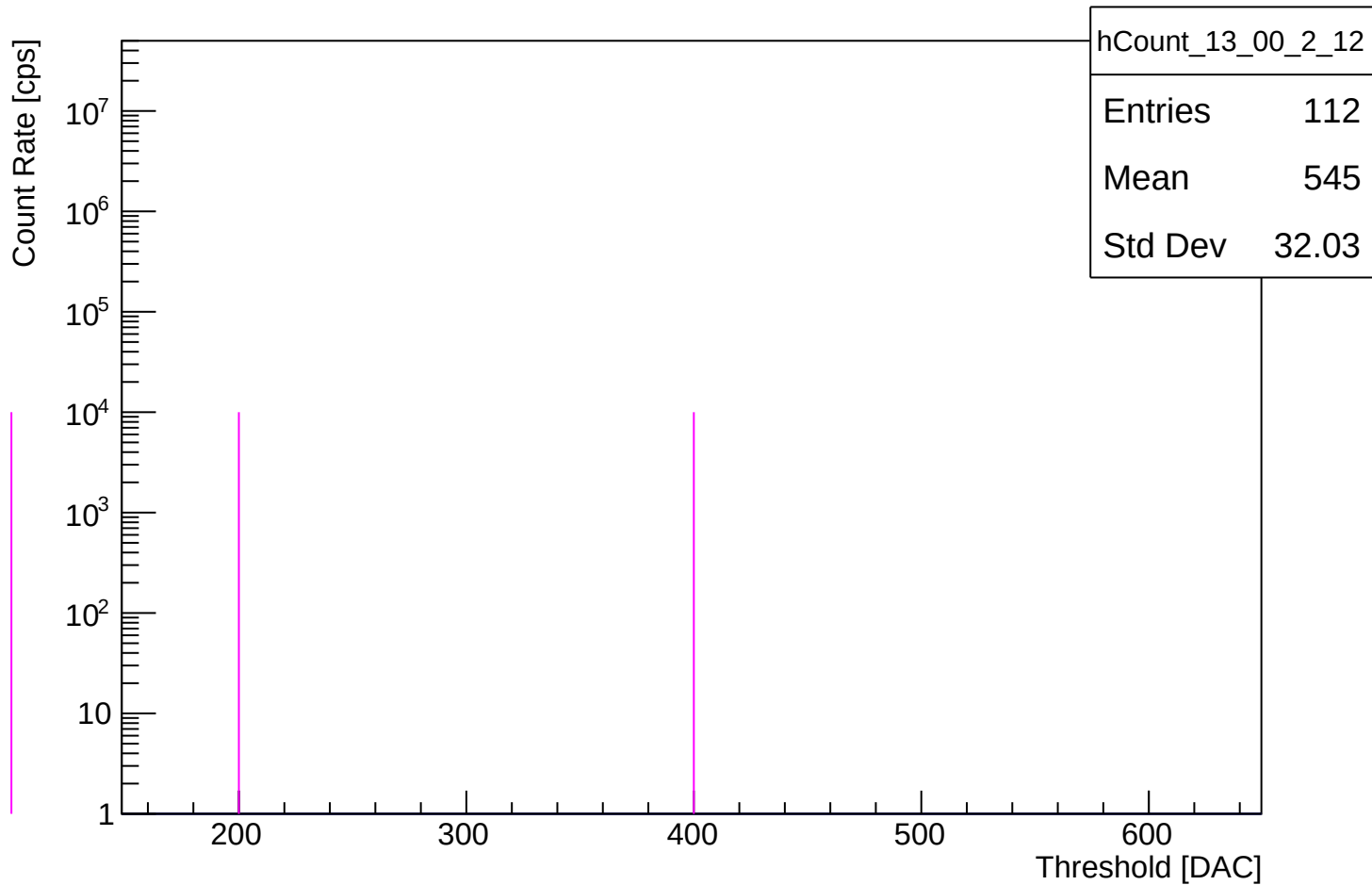
Row 1 Tile 1 Pmt 3 Pixel 34 Slot 13 Fiber 0 Asic 2 Channel 13



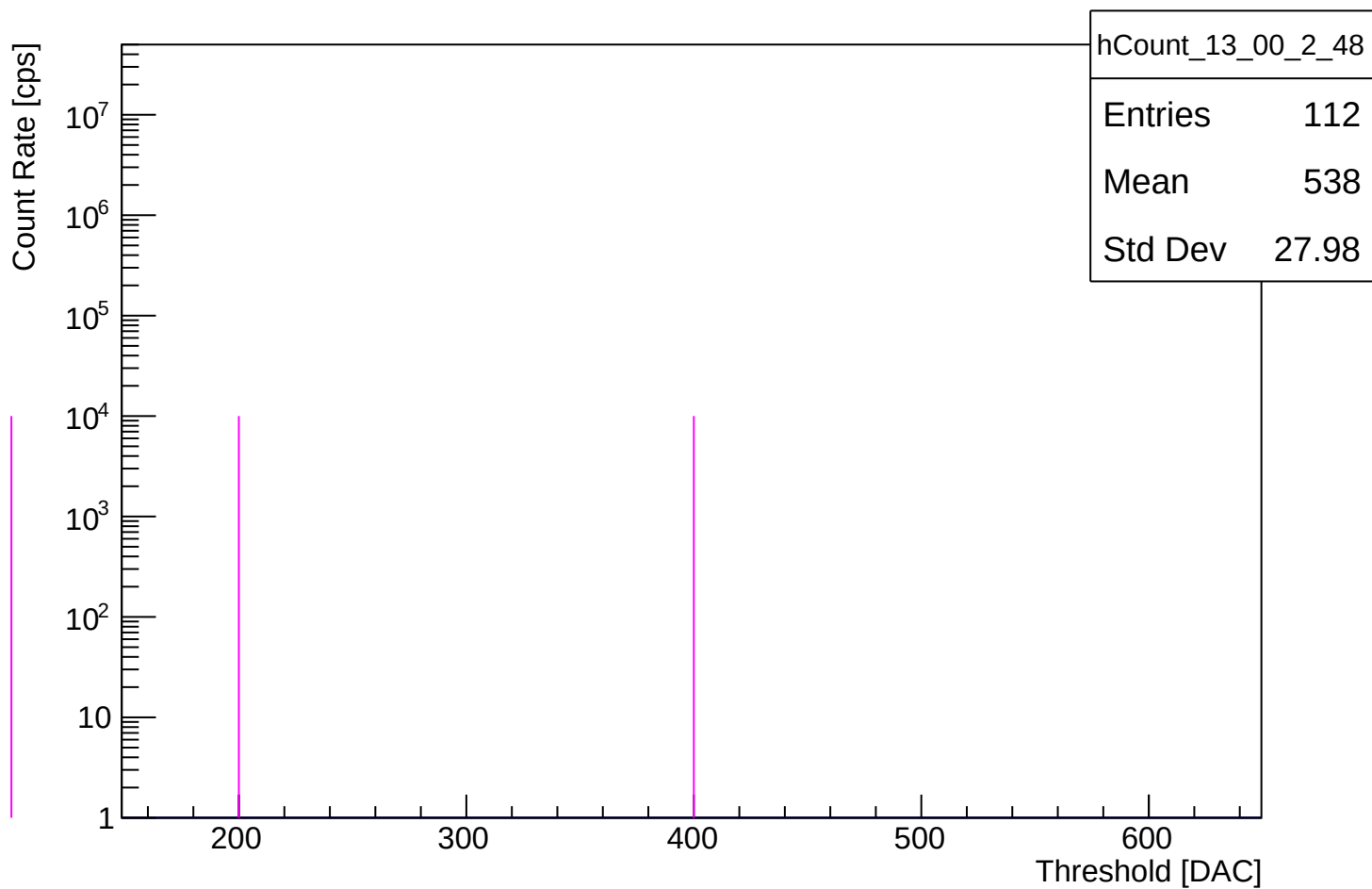
Row 1 Tile 1 Pmt 3 Pixel 35 Slot 13 Fiber 0 Asic 2 Channel 14



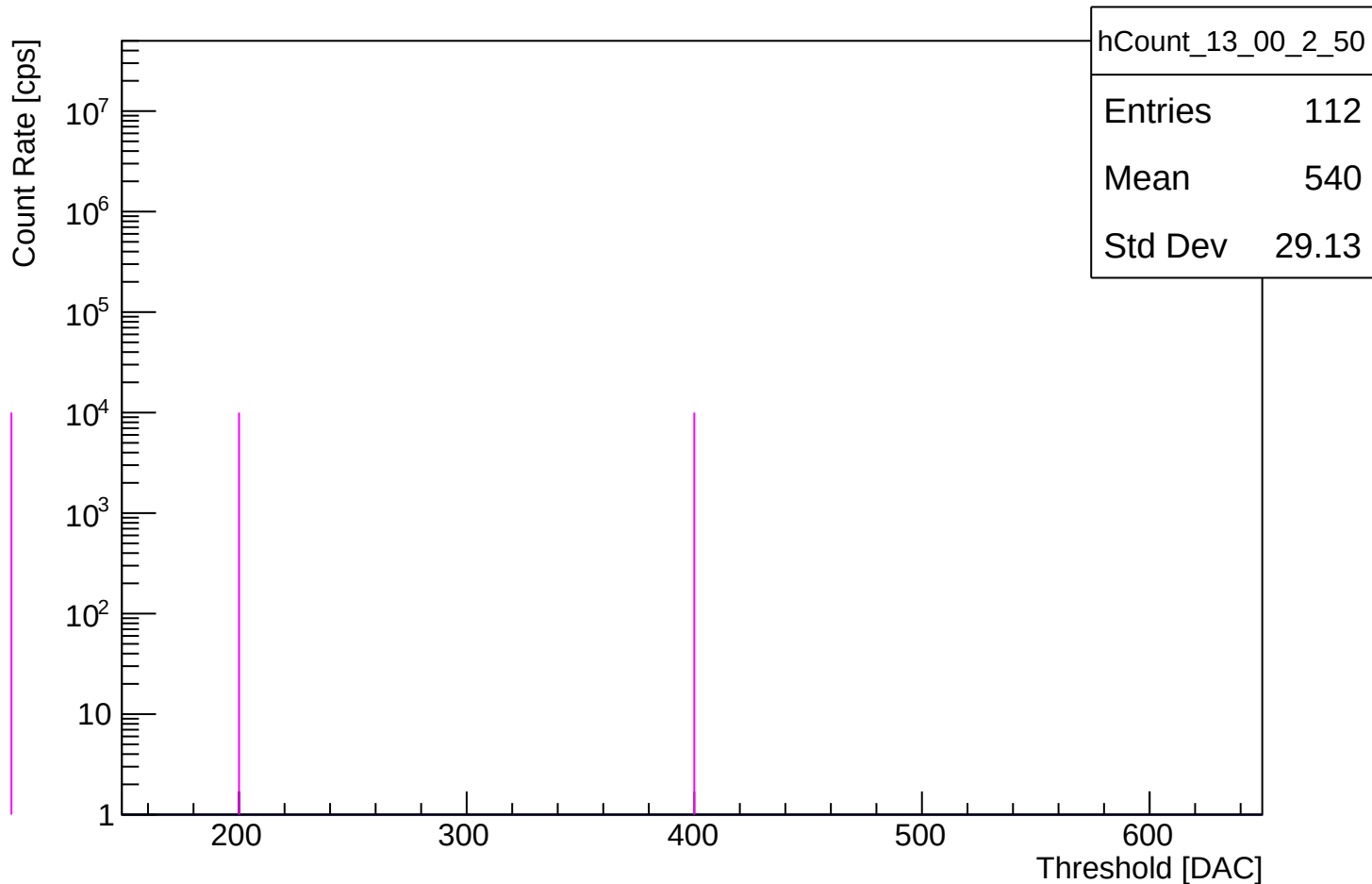
Row 1 Tile 1 Pmt 3 Pixel 36 Slot 13 Fiber 0 Asic 2 Channel 12



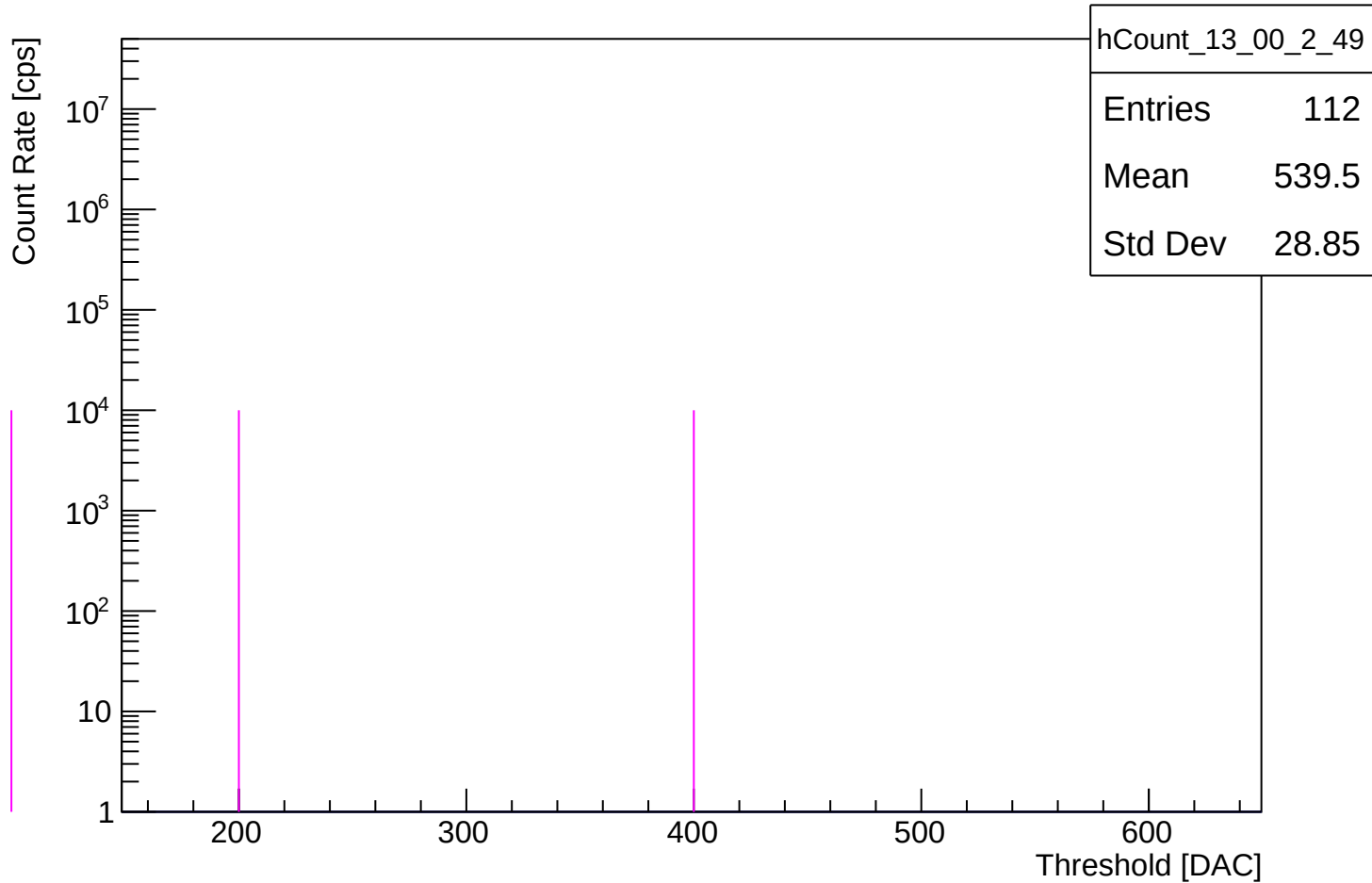
Row 1 Tile 1 Pmt 3 Pixel 37 Slot 13 Fiber 0 Asic 2 Channel 48



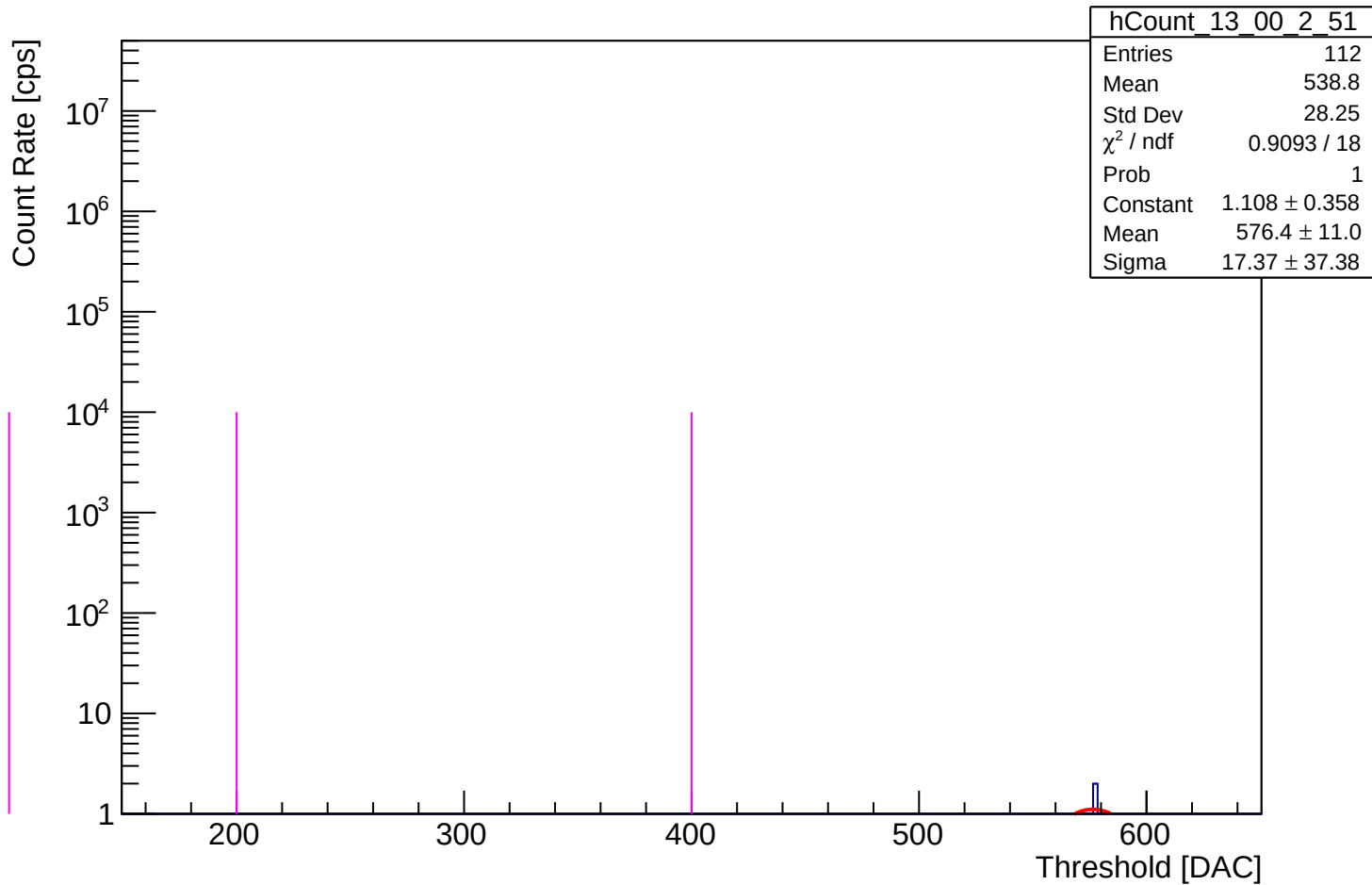
Row 1 Tile 1 Pmt 3 Pixel 38 Slot 13 Fiber 0 Asic 2 Channel 50



Row 1 Tile 1 Pmt 3 Pixel 39 Slot 13 Fiber 0 Asic 2 Channel 49

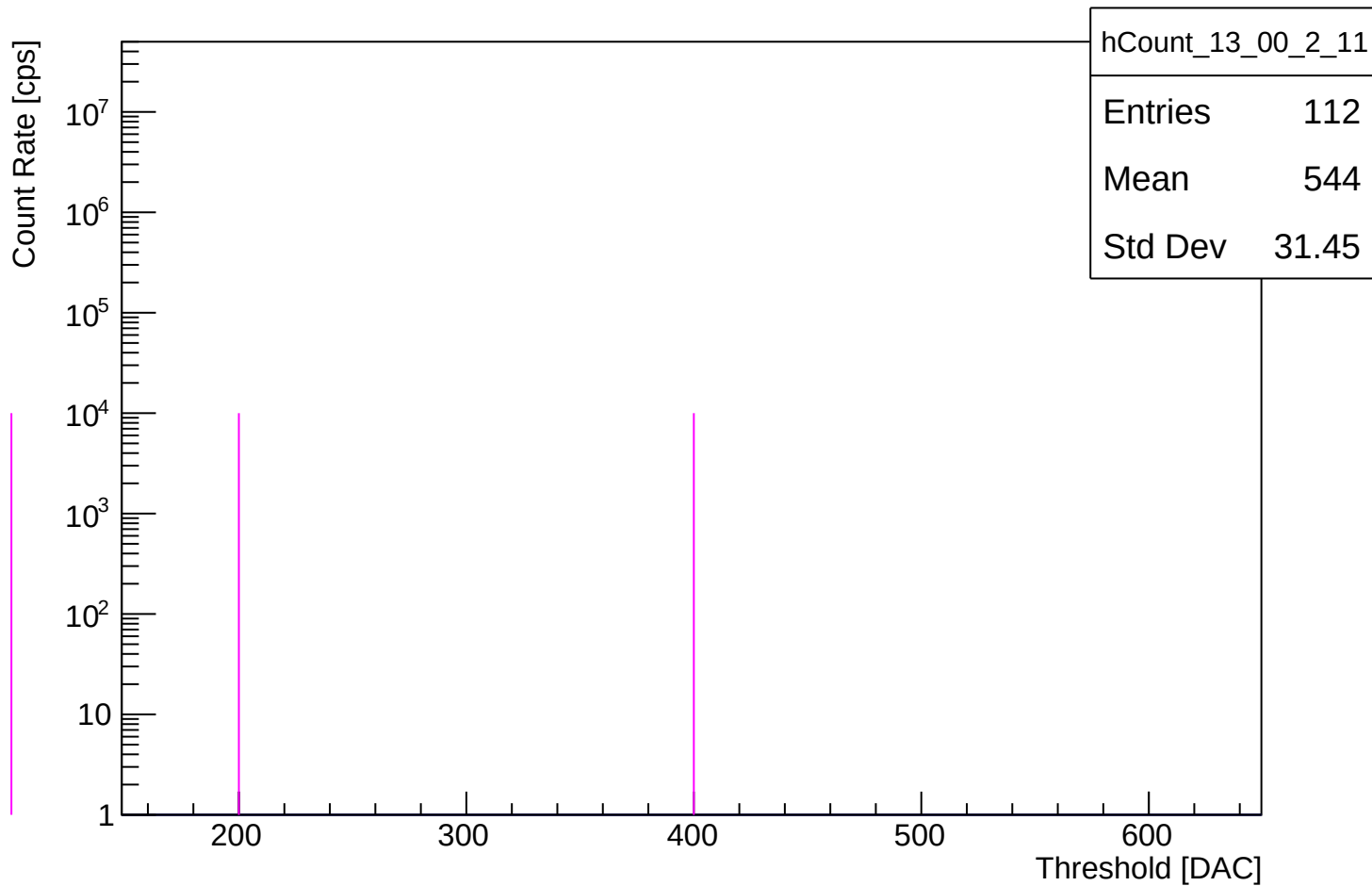


Row 1 Tile 1 Pmt 3 Pixel 40 Slot 13 Fiber 0 Asic 2 Channel 51

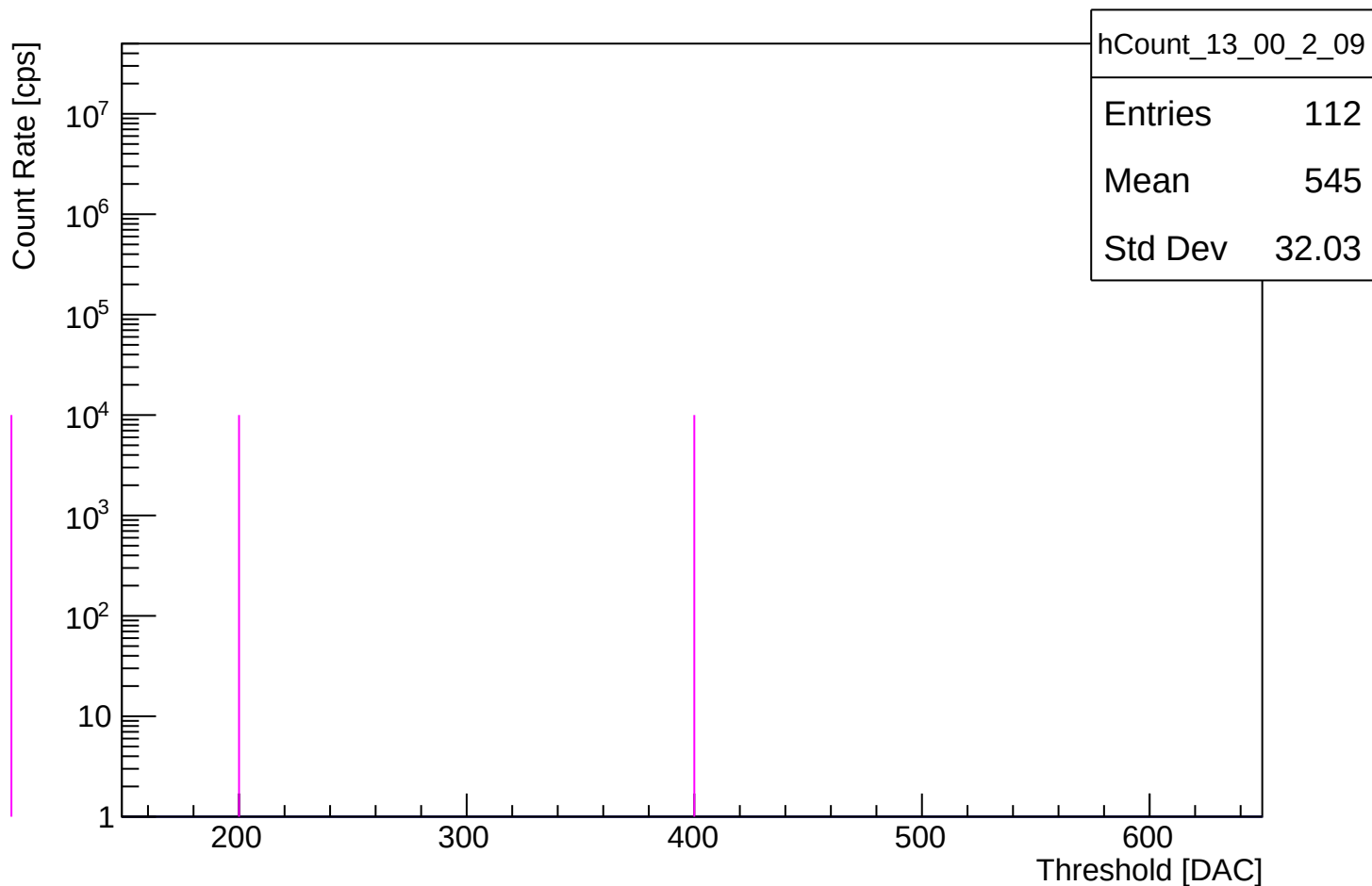




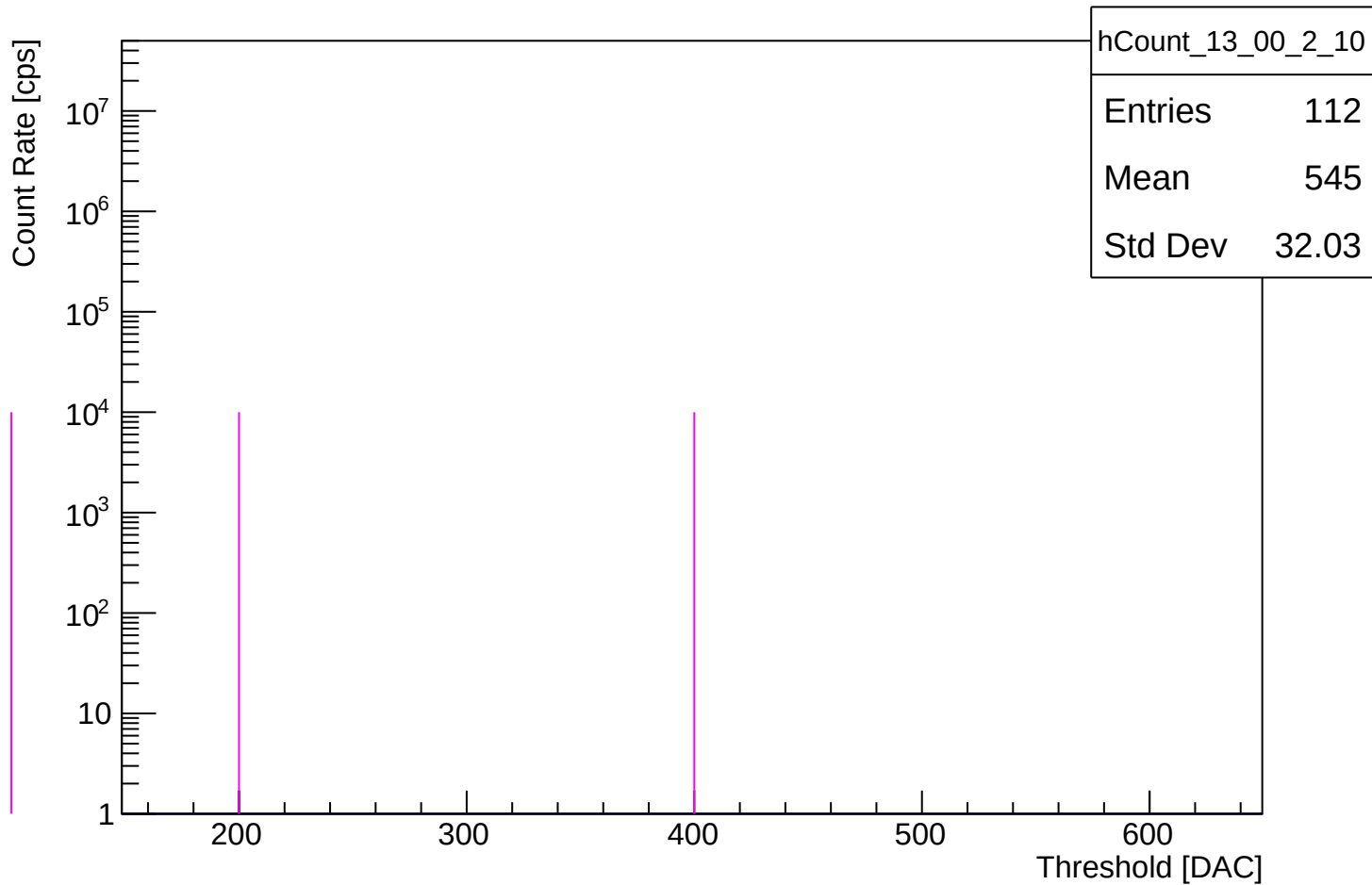
Row 1 Tile 1 Pmt 3 Pixel 41 Slot 13 Fiber 0 Asic 2 Channel 11

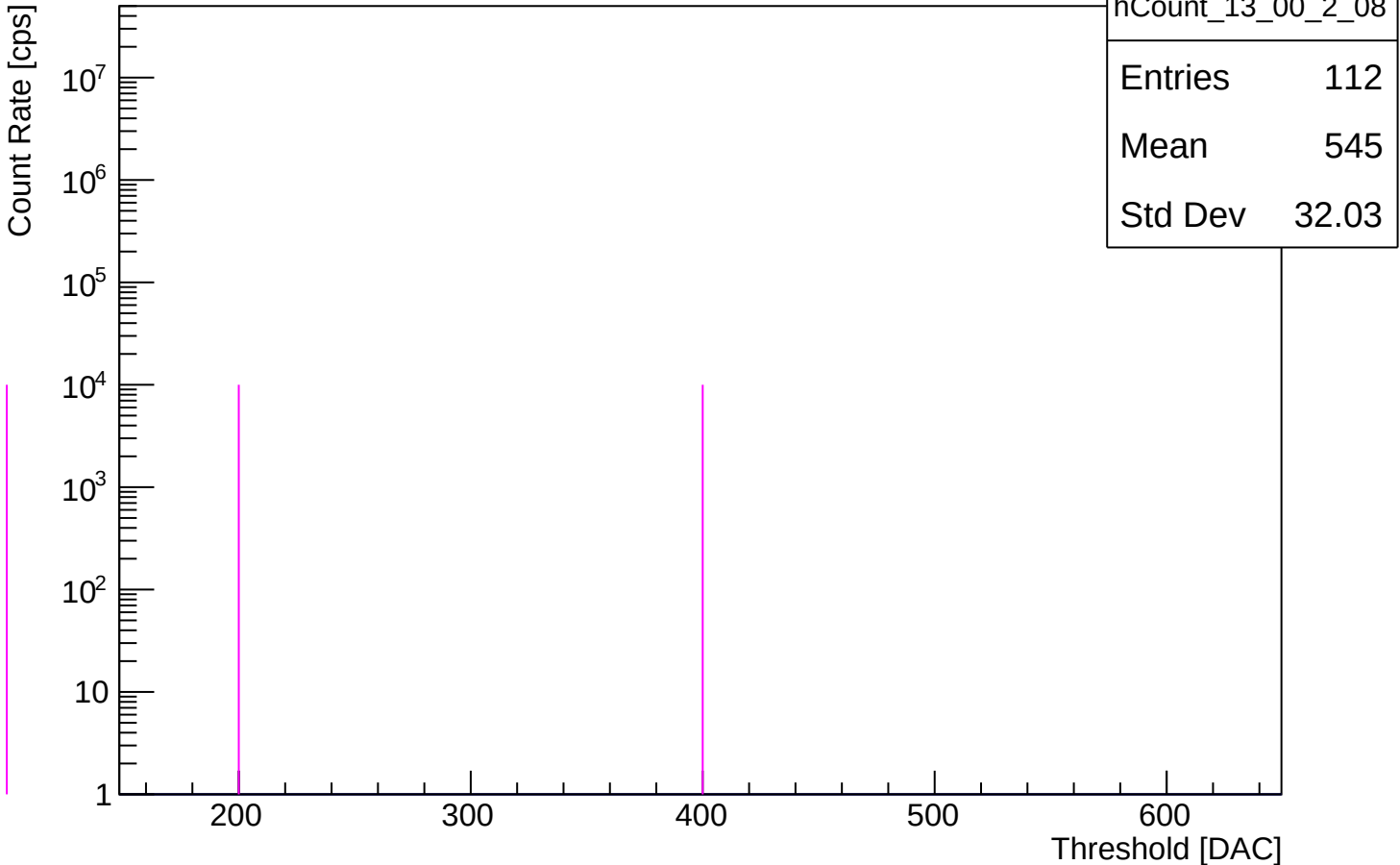


Row 1 Tile 1 Pmt 3 Pixel 42 Slot 13 Fiber 0 Asic 2 Channel 9

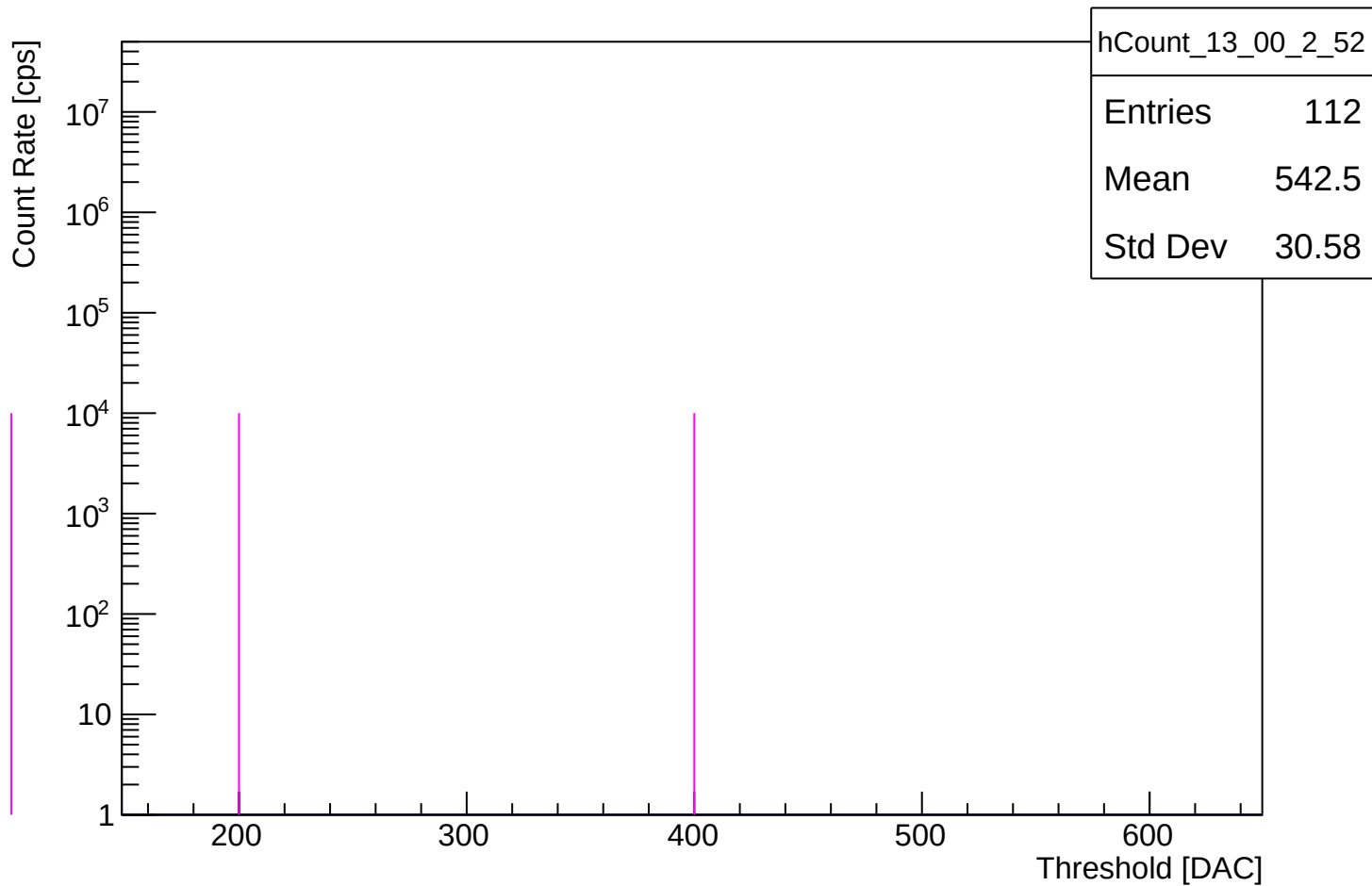


Row 1 Tile 1 Pmt 3 Pixel 43 Slot 13 Fiber 0 Asic 2 Channel 10

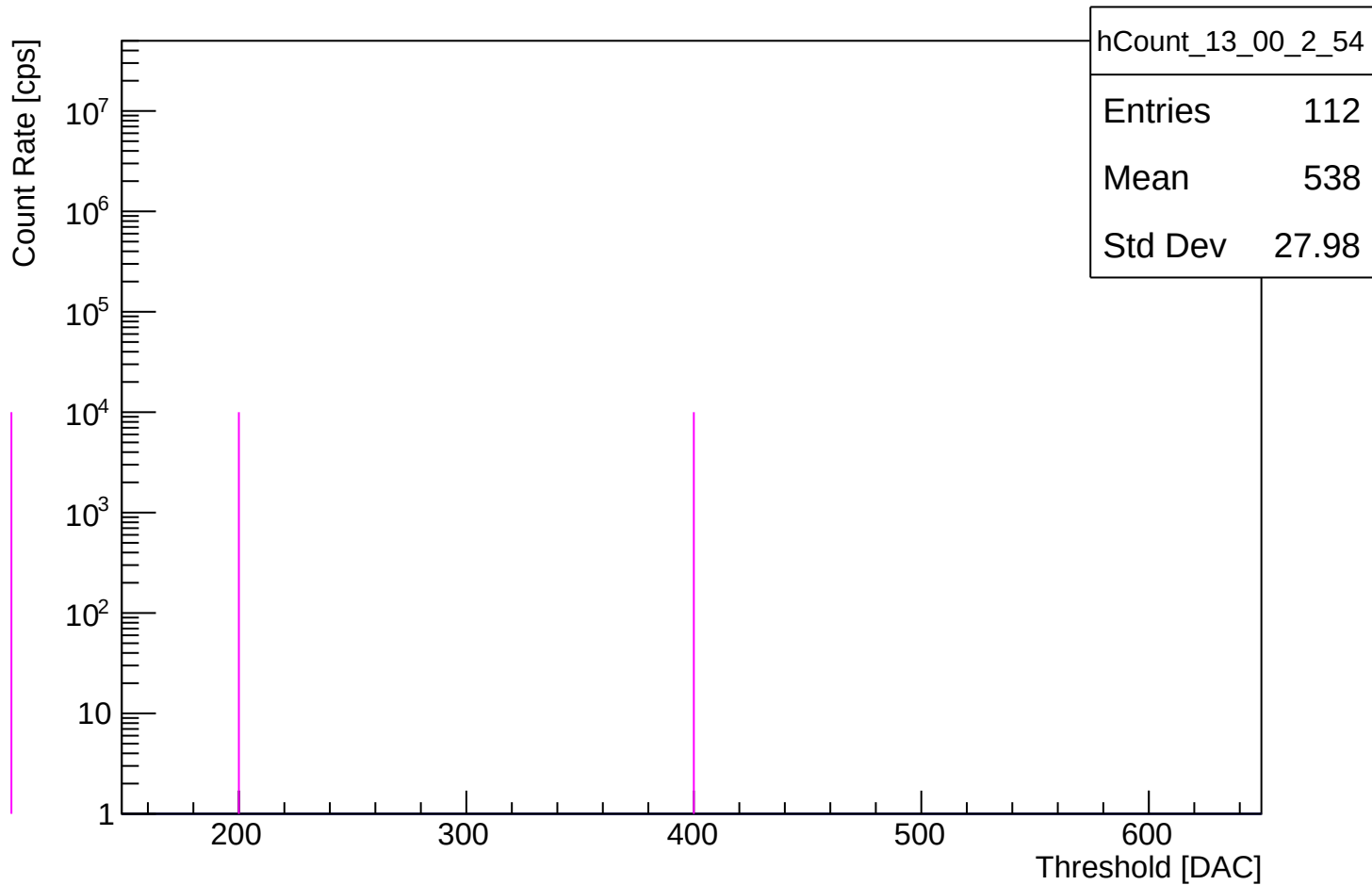




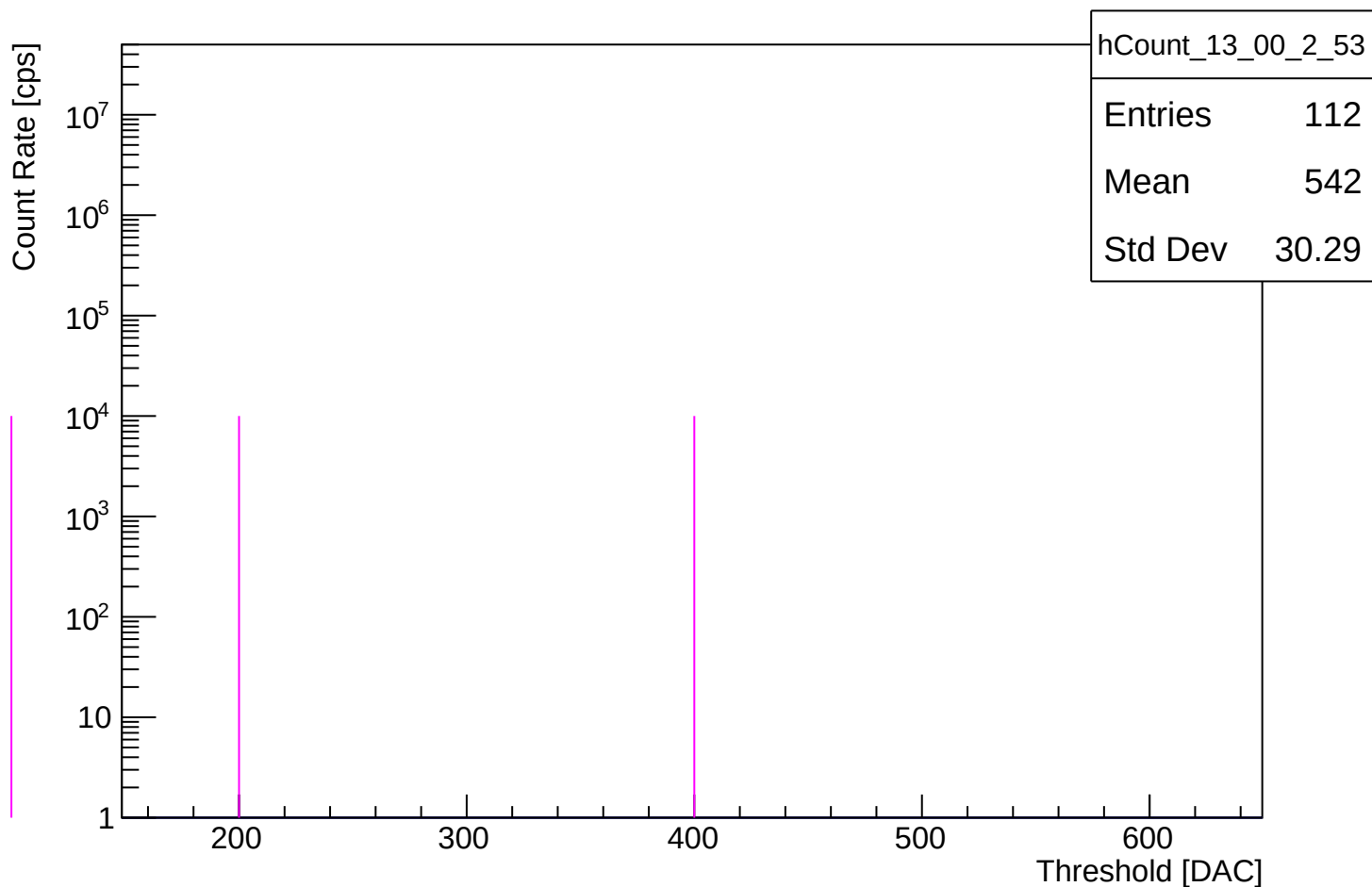
Row 1 Tile 1 Pmt 3 Pixel 45 Slot 13 Fiber 0 Asic 2 Channel 52



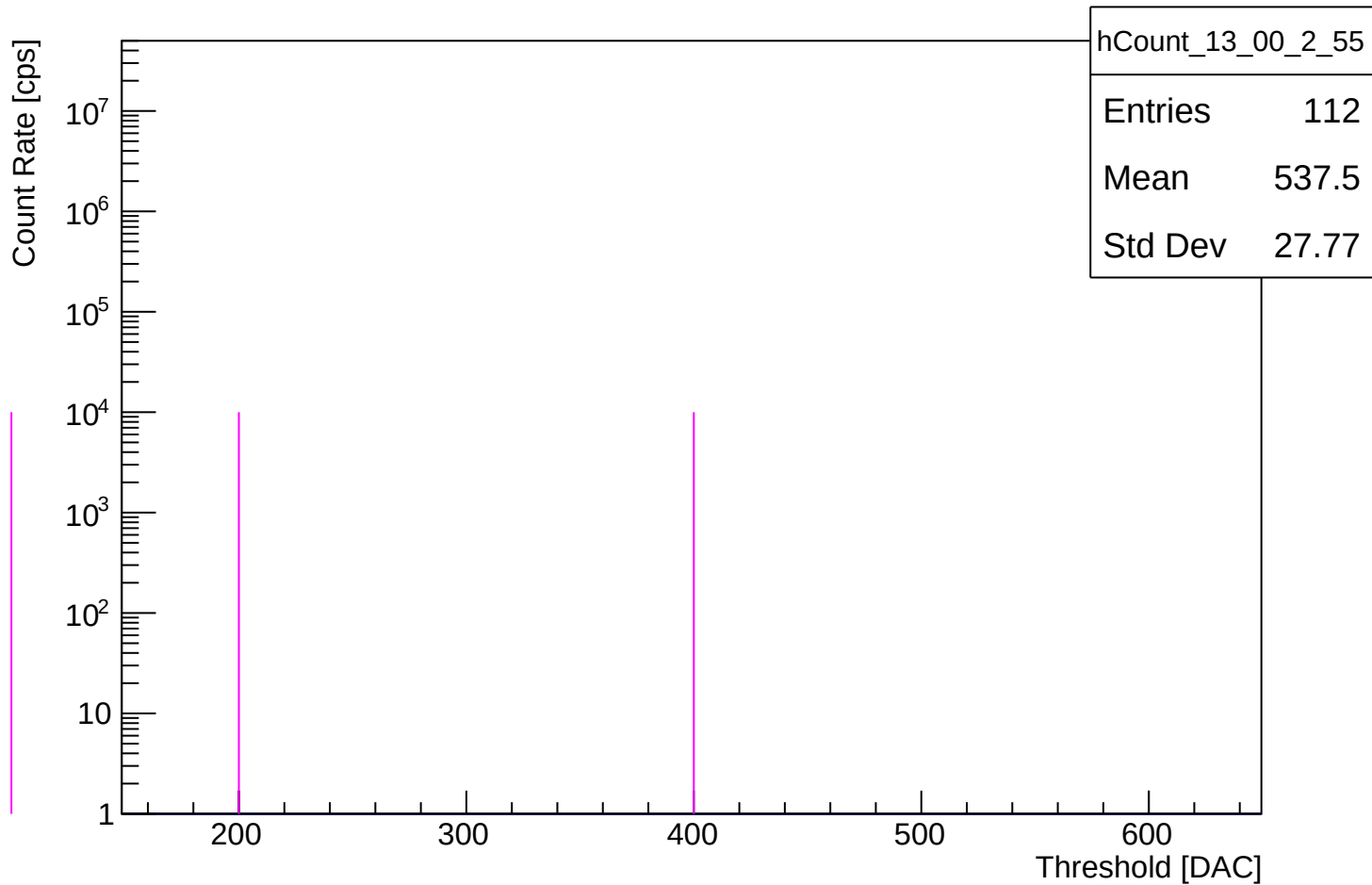
Row 1 Tile 1 Pmt 3 Pixel 46 Slot 13 Fiber 0 Asic 2 Channel 54



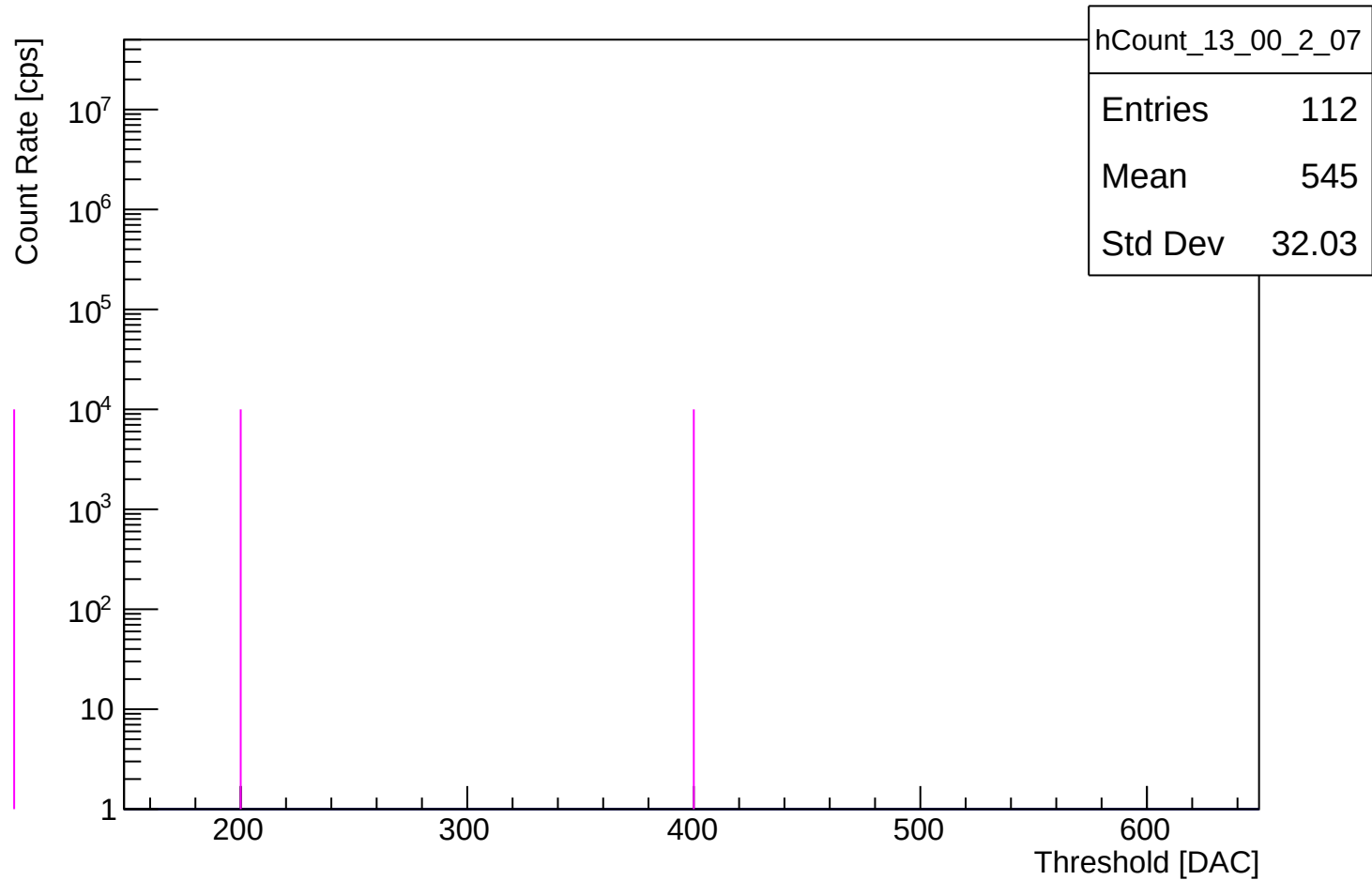
Row 1 Tile 1 Pmt 3 Pixel 47 Slot 13 Fiber 0 Asic 2 Channel 53

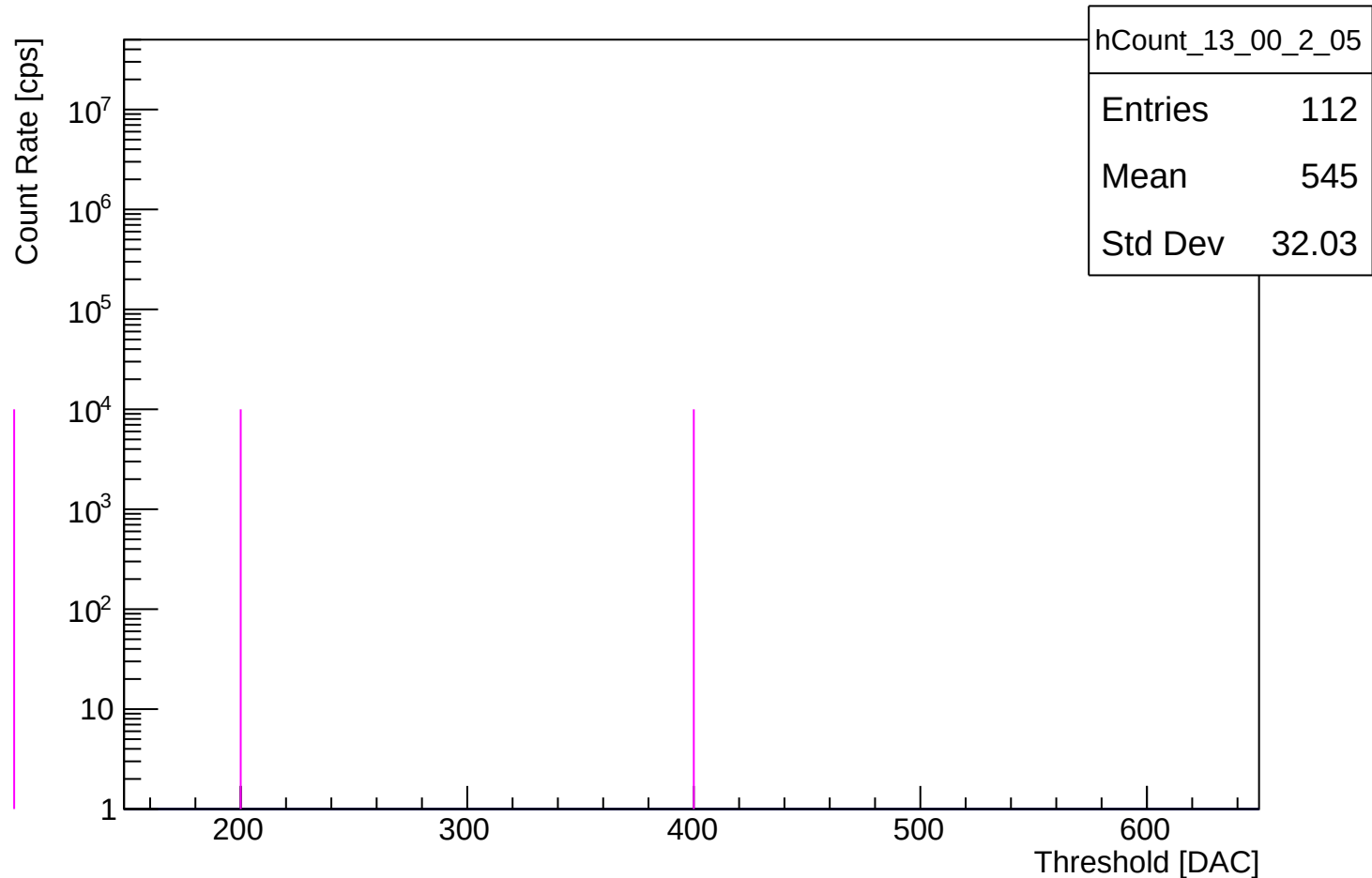


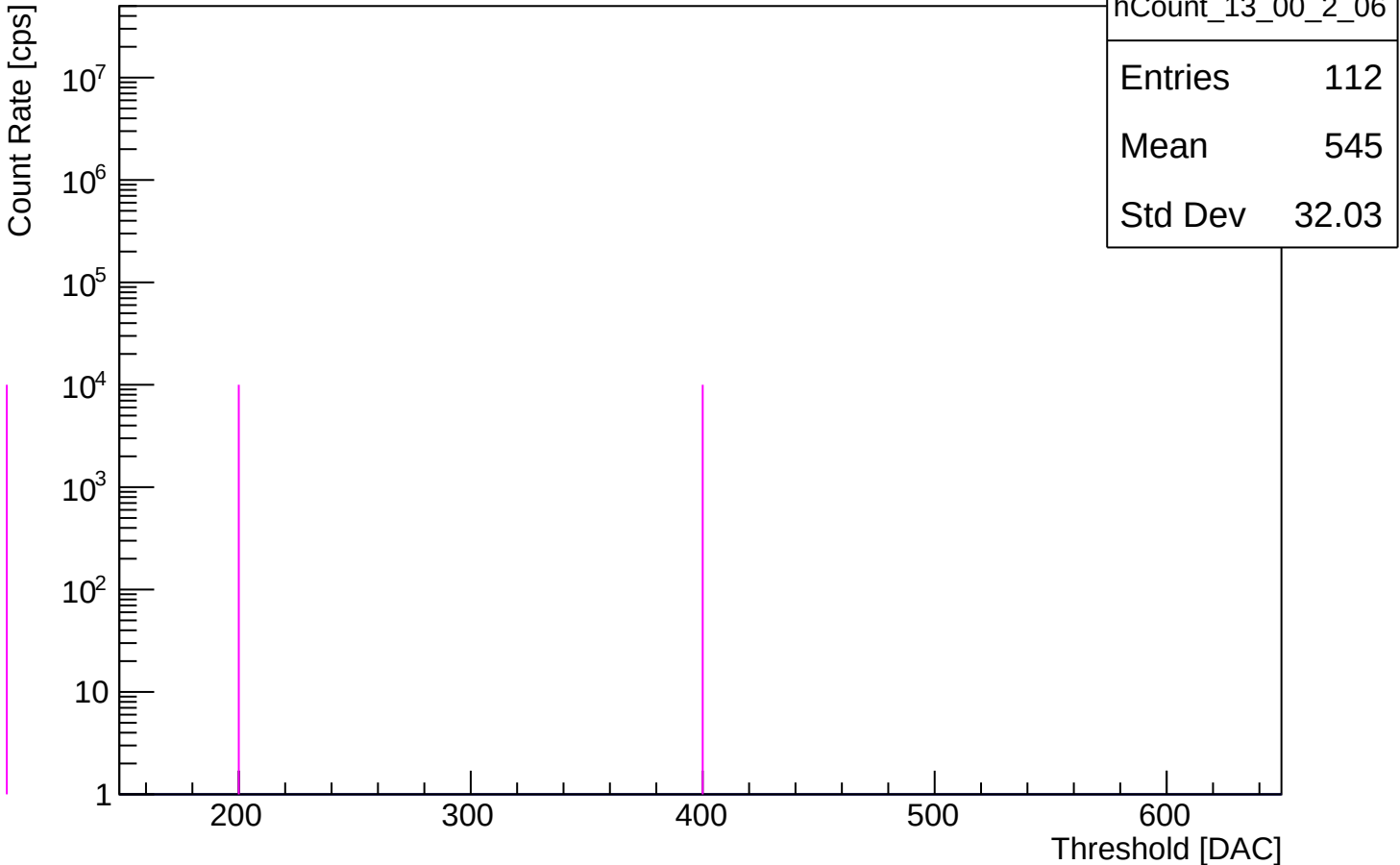
Row 1 Tile 1 Pmt 3 Pixel 48 Slot 13 Fiber 0 Asic 2 Channel 55



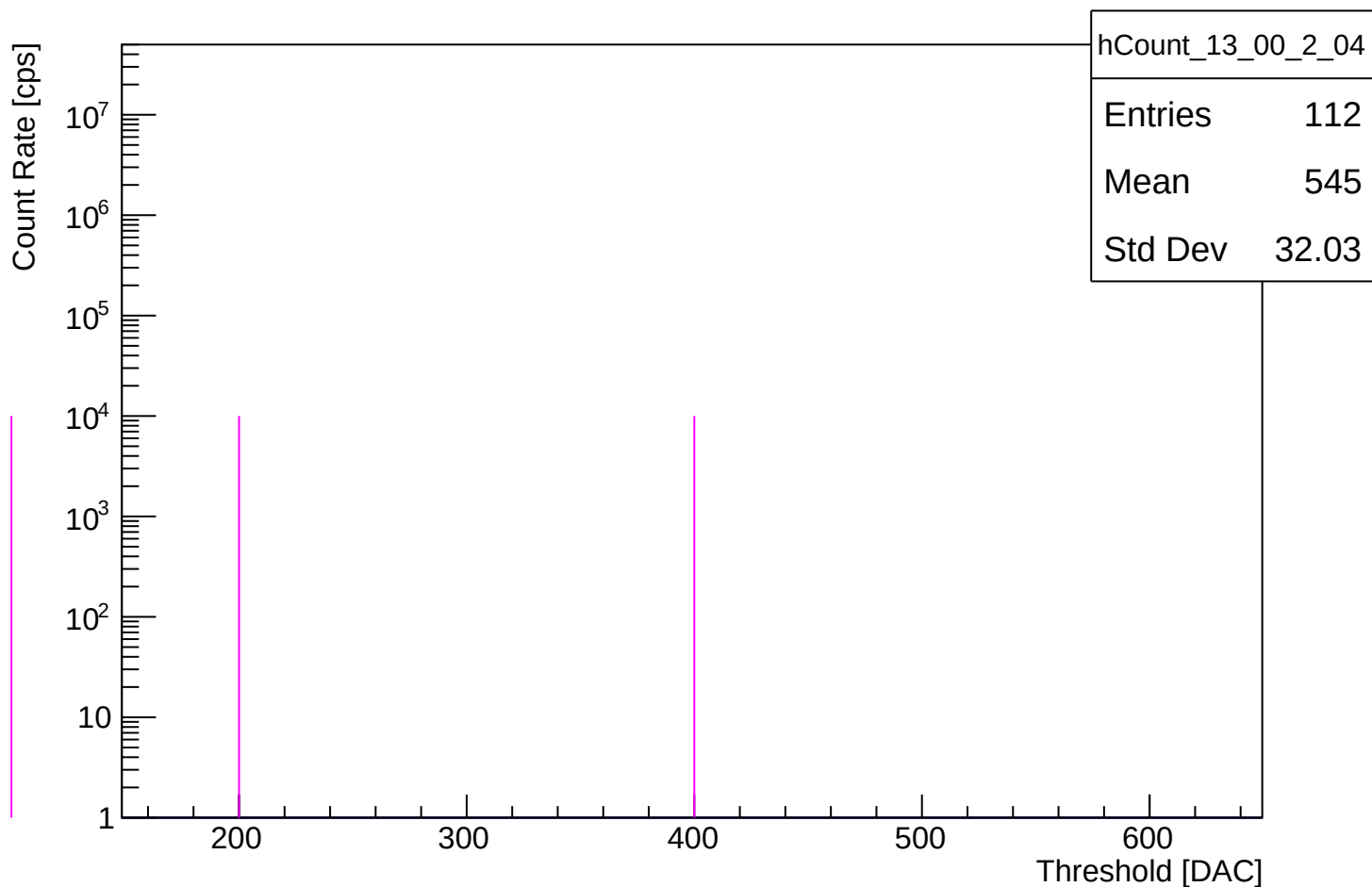




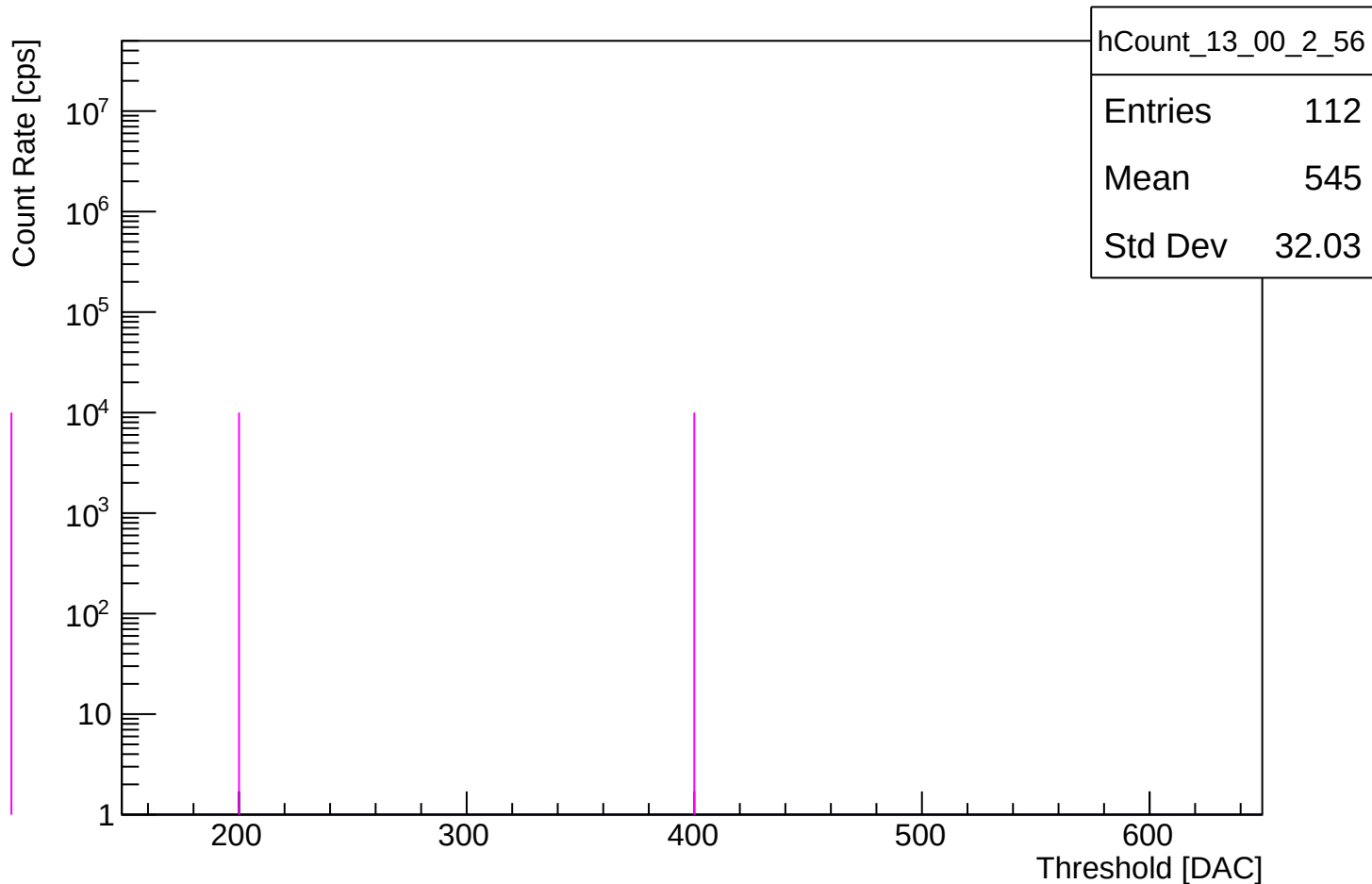




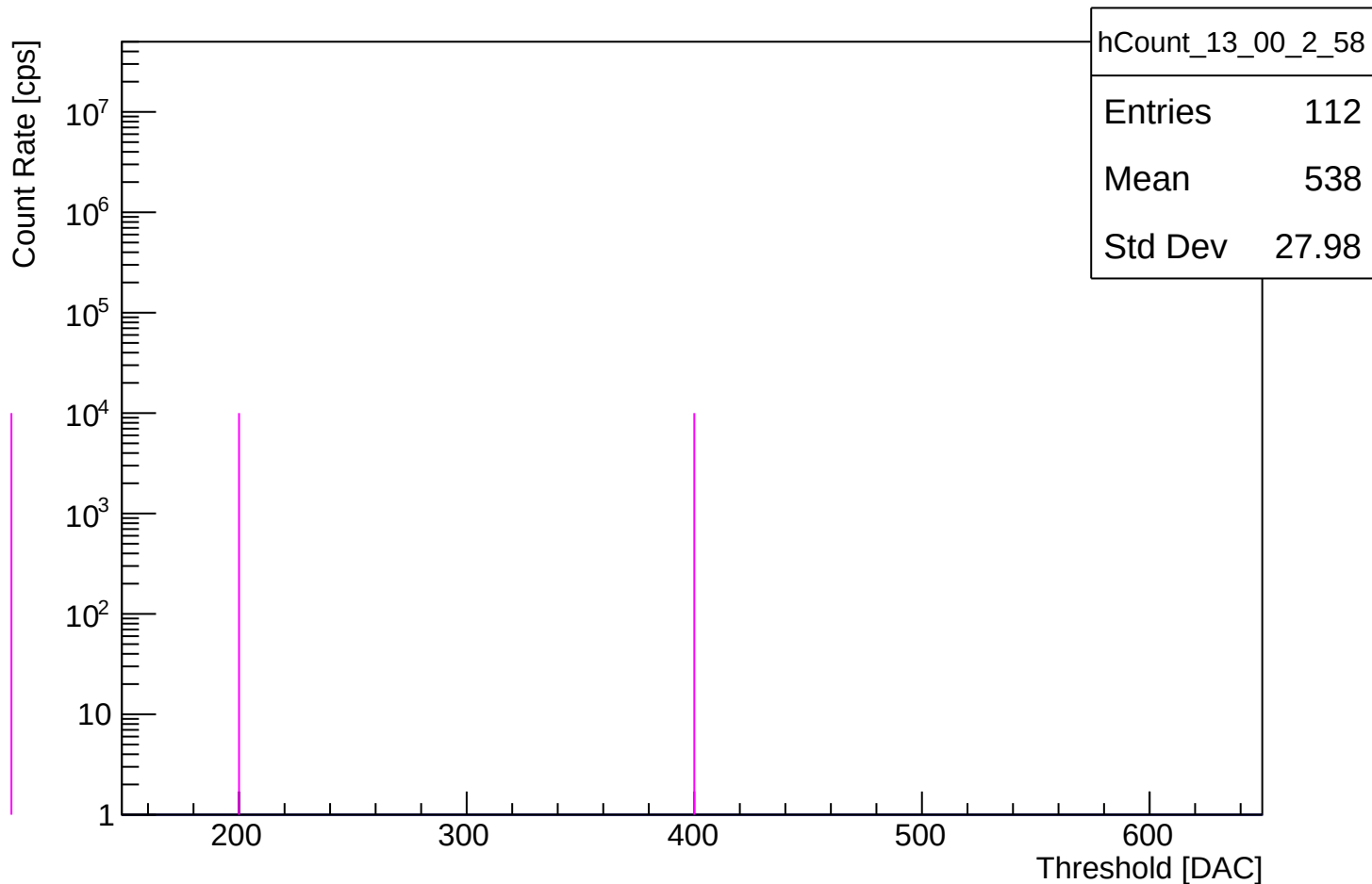
Row 1 Tile 1 Pmt 3 Pixel 52 Slot 13 Fiber 0 Asic 2 Channel 4



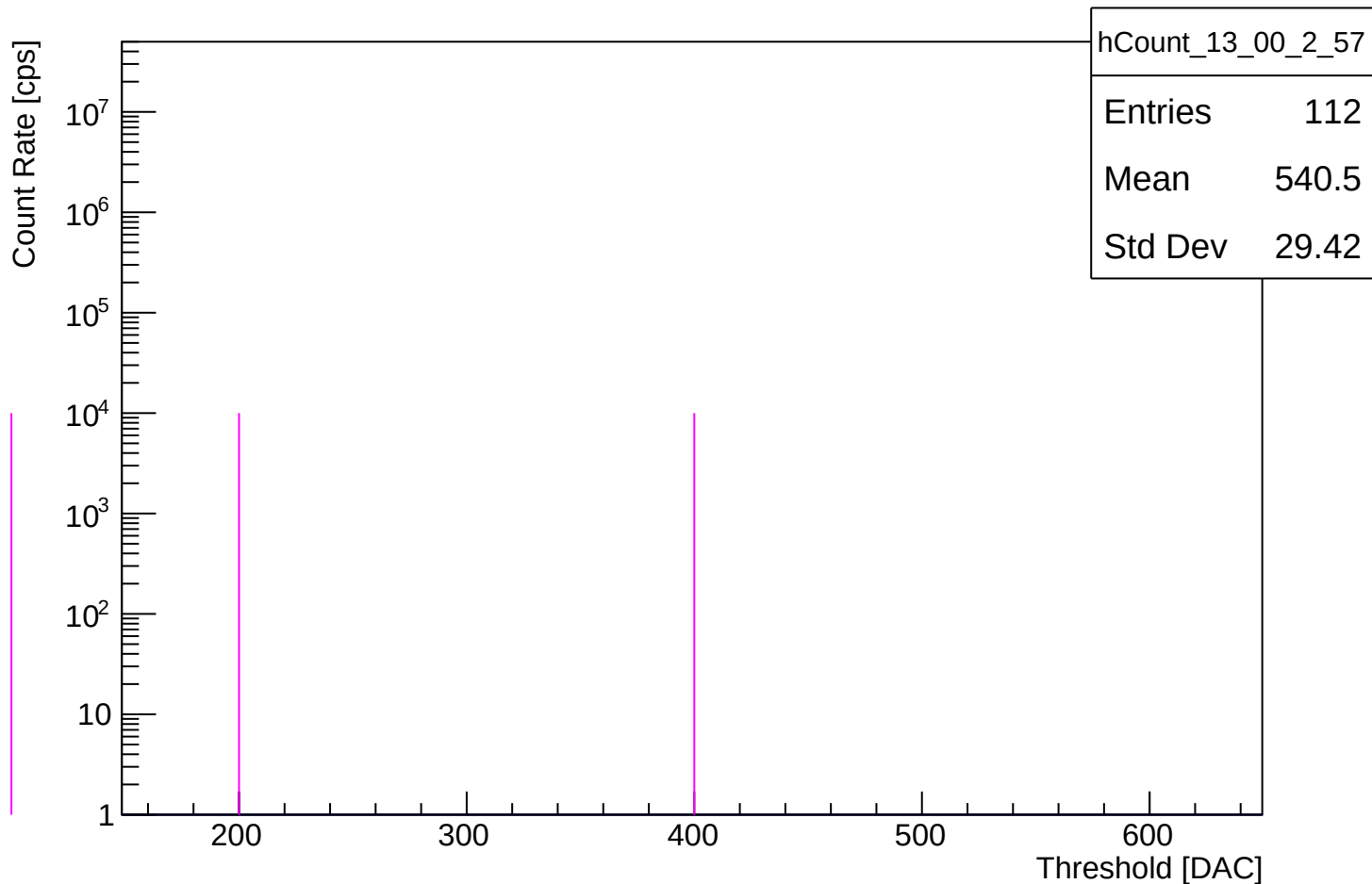
Row 1 Tile 1 Pmt 3 Pixel 53 Slot 13 Fiber 0 Asic 2 Channel 56



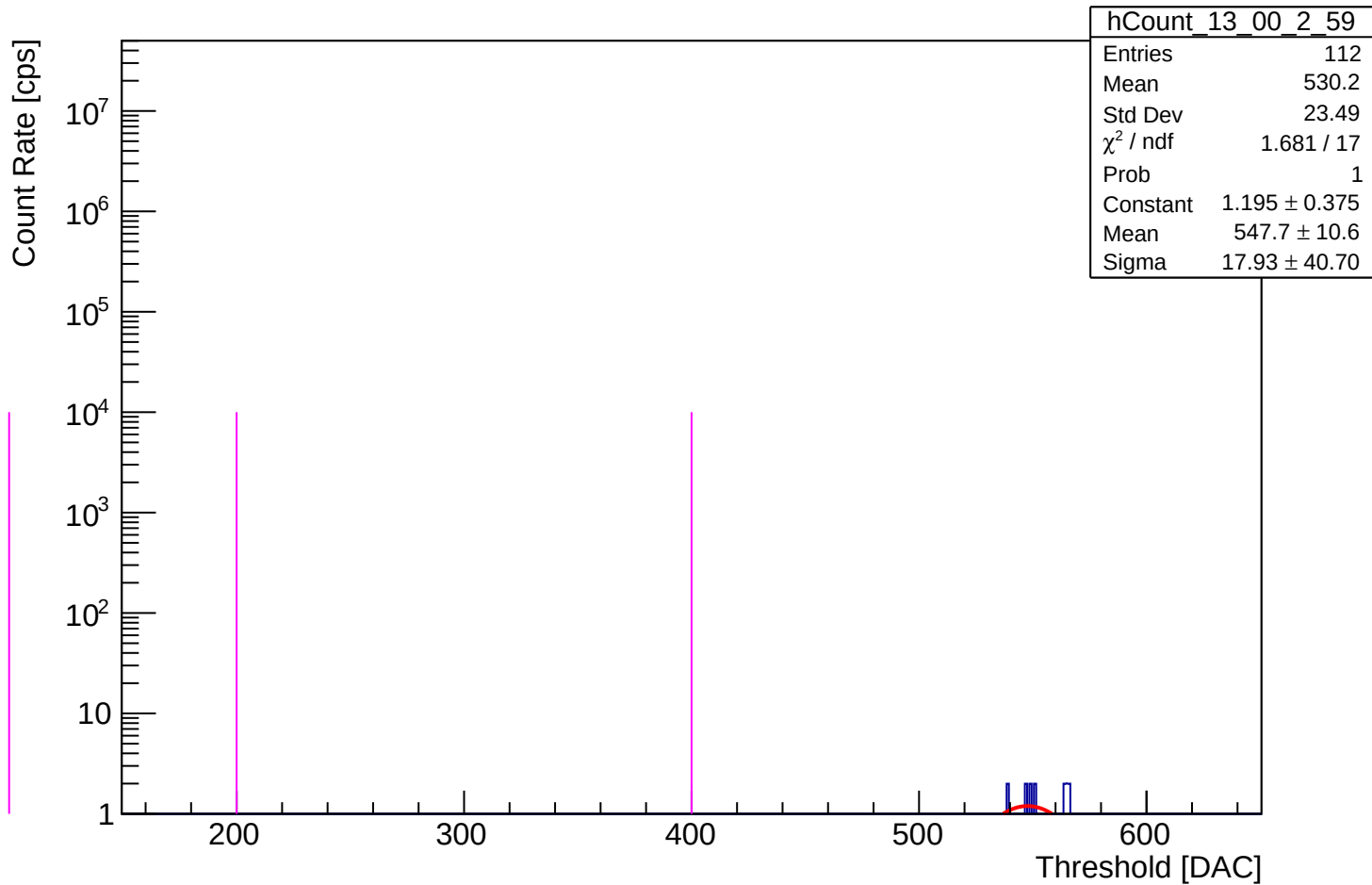
Row 1 Tile 1 Pmt 3 Pixel 54 Slot 13 Fiber 0 Asic 2 Channel 58



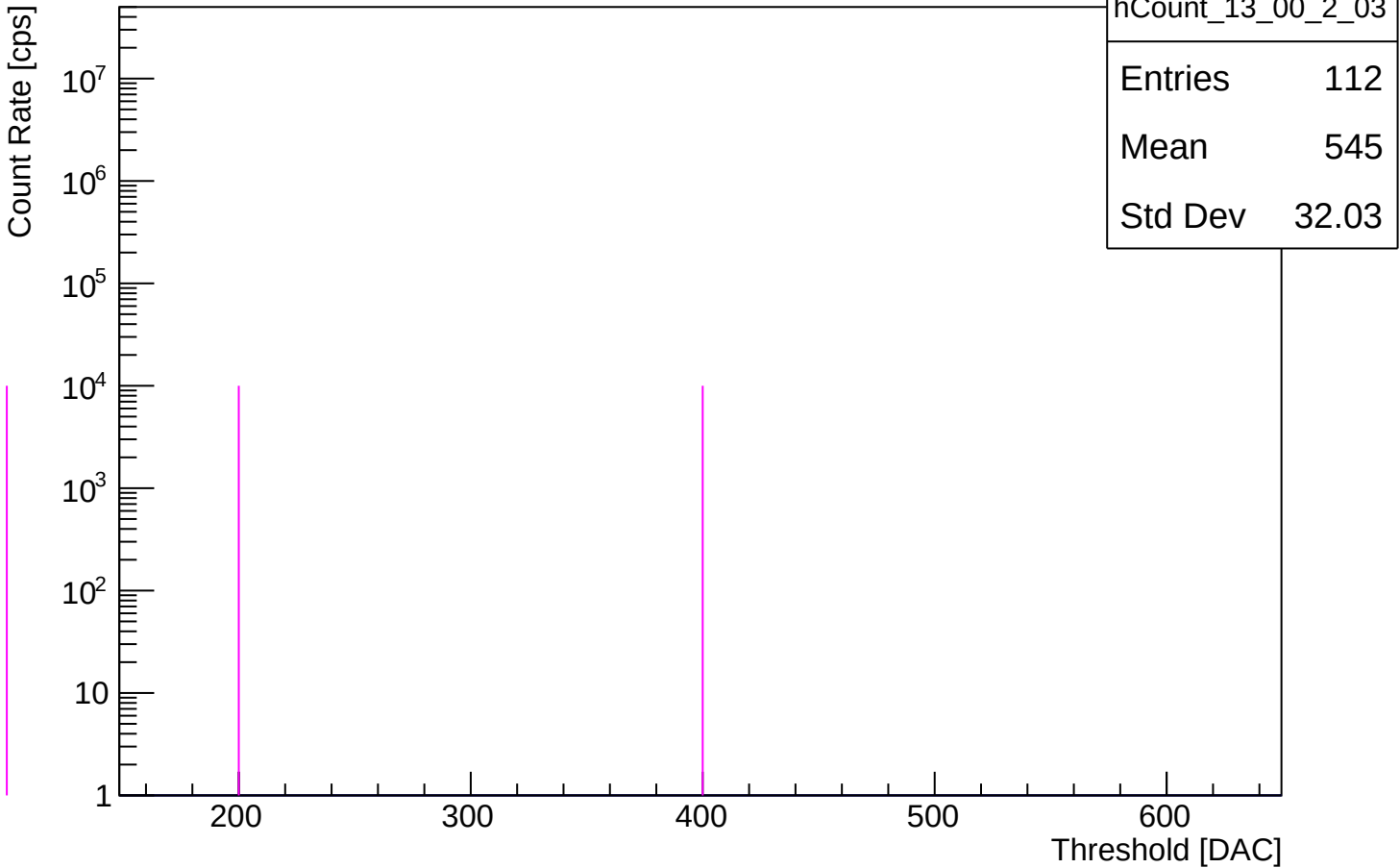
Row 1 Tile 1 Pmt 3 Pixel 55 Slot 13 Fiber 0 Asic 2 Channel 57



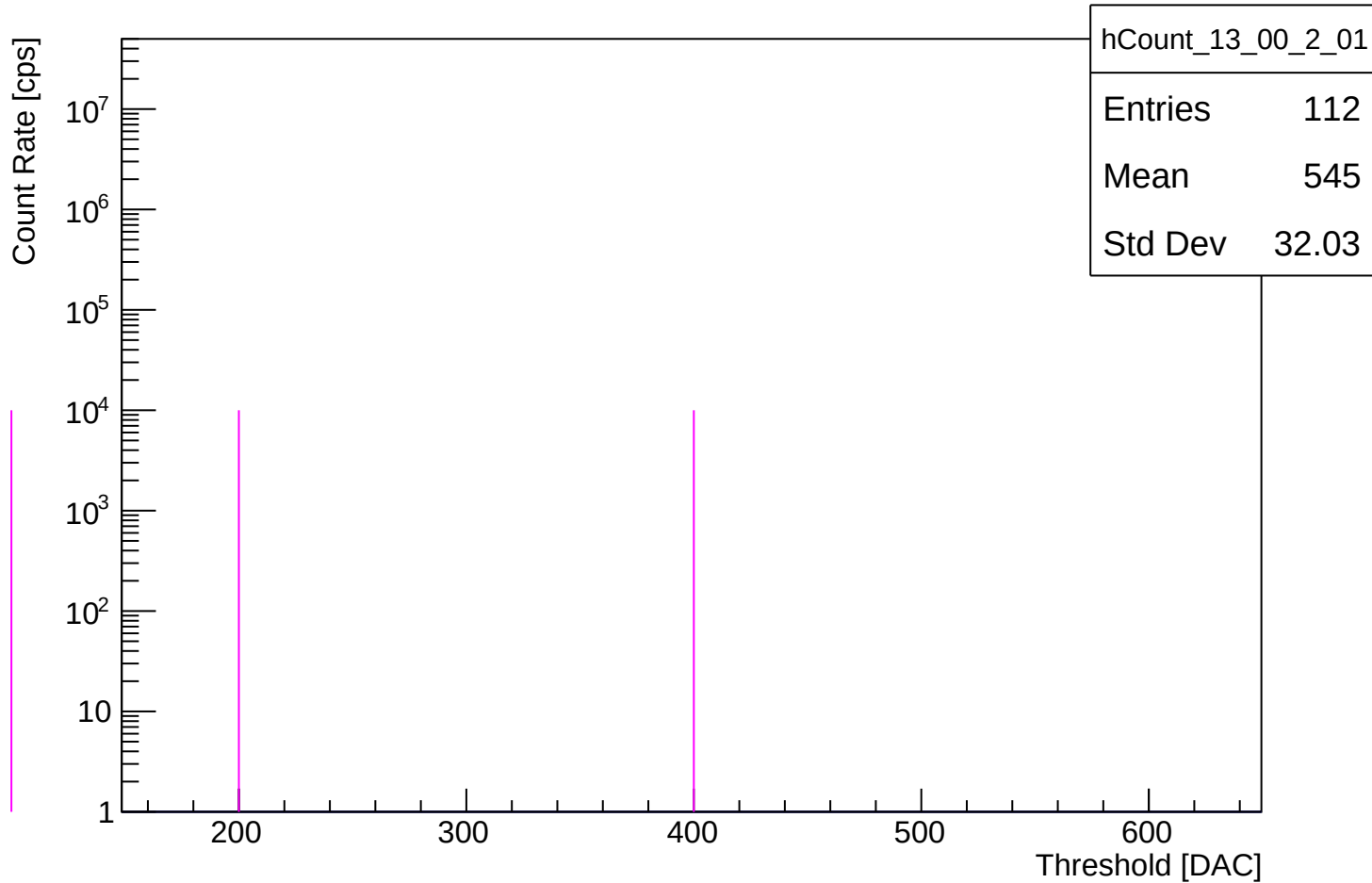
Row 1 Tile 1 Pmt 3 Pixel 56 Slot 13 Fiber 0 Asic 2 Channel 59



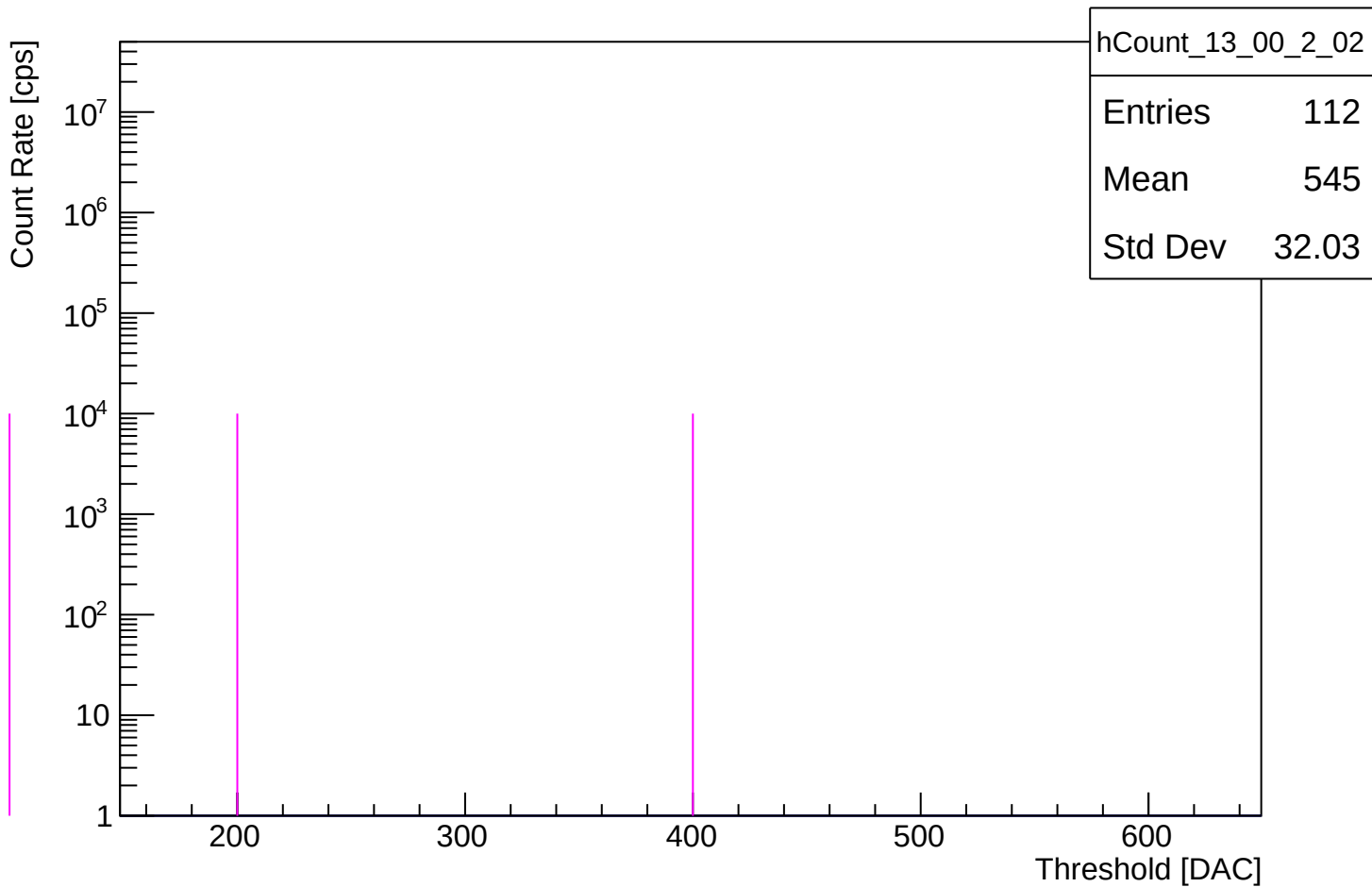




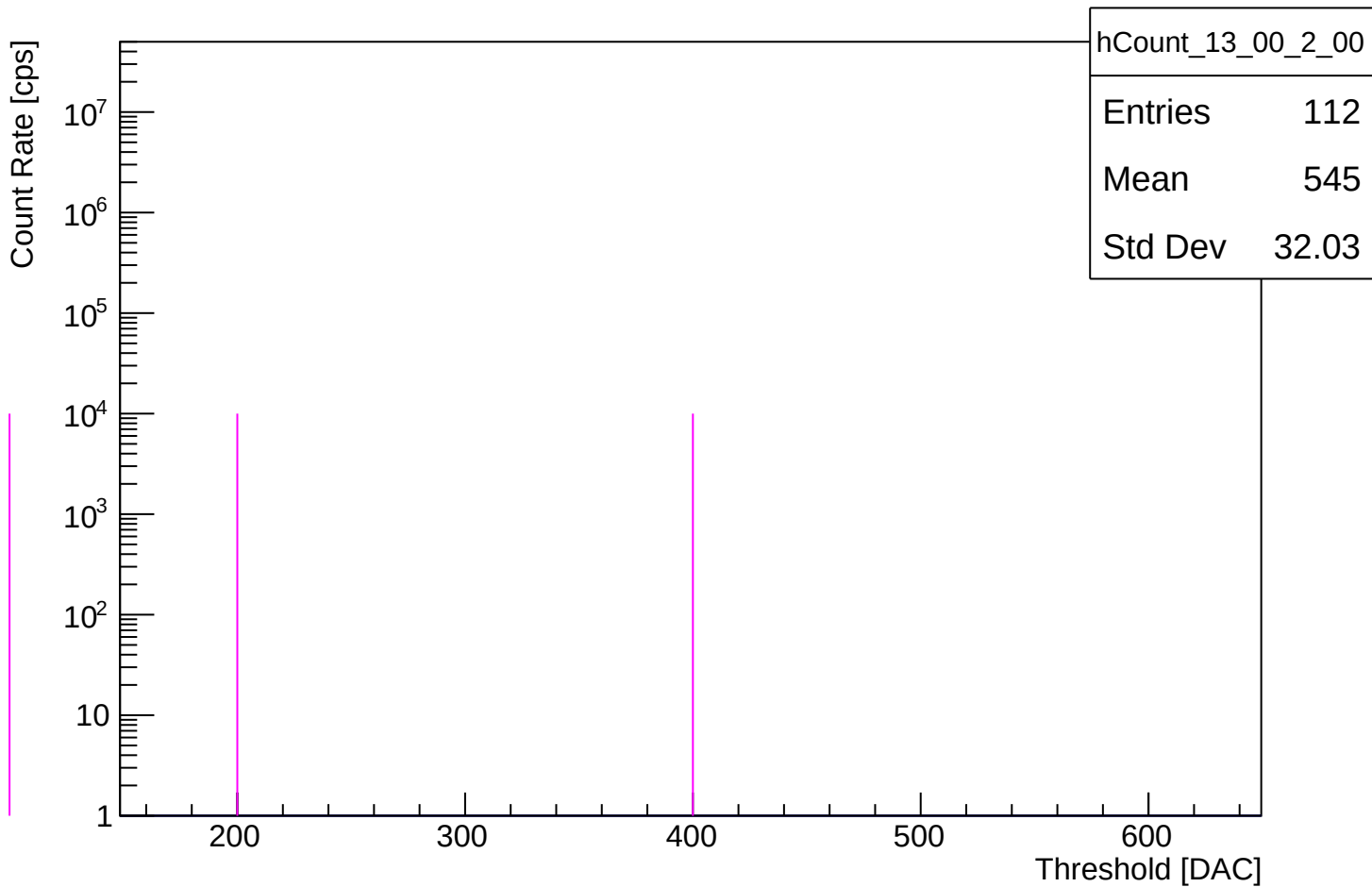
Row 1 Tile 1 Pmt 3 Pixel 58 Slot 13 Fiber 0 Asic 2 Channel 1



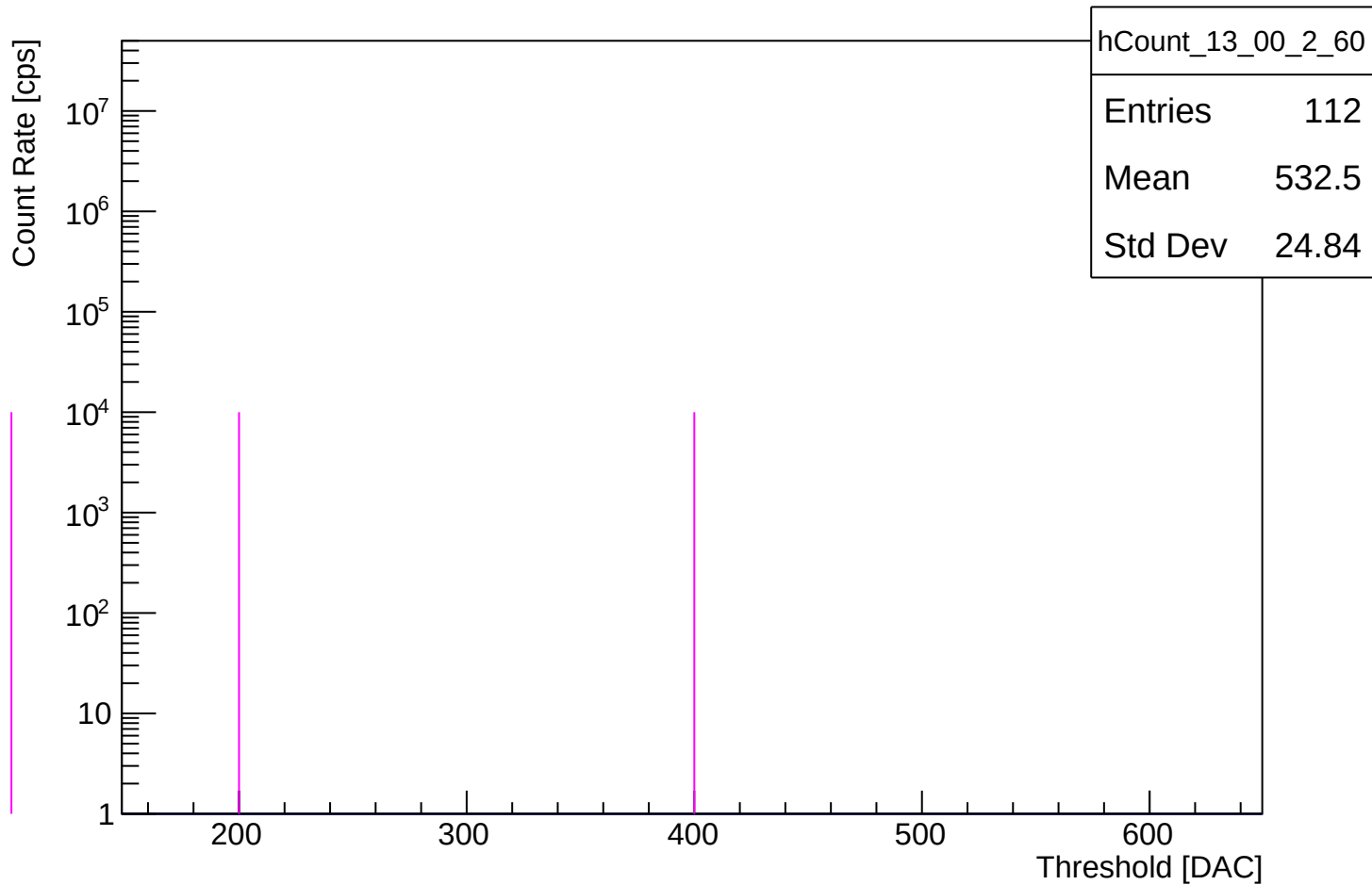
Row 1 Tile 1 Pmt 3 Pixel 59 Slot 13 Fiber 0 Asic 2 Channel 2



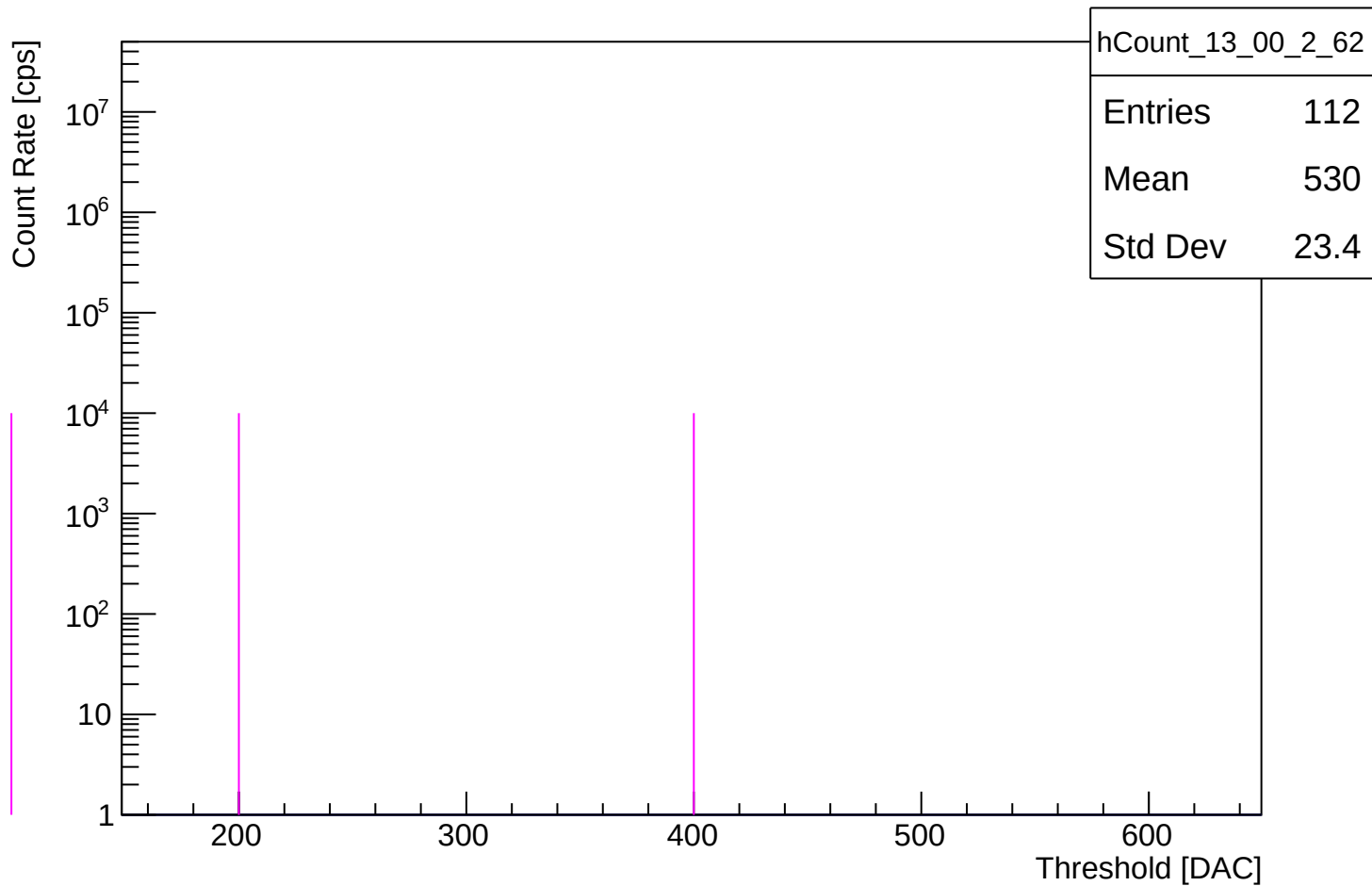
Row 1 Tile 1 Pmt 3 Pixel 60 Slot 13 Fiber 0 Asic 2 Channel 0



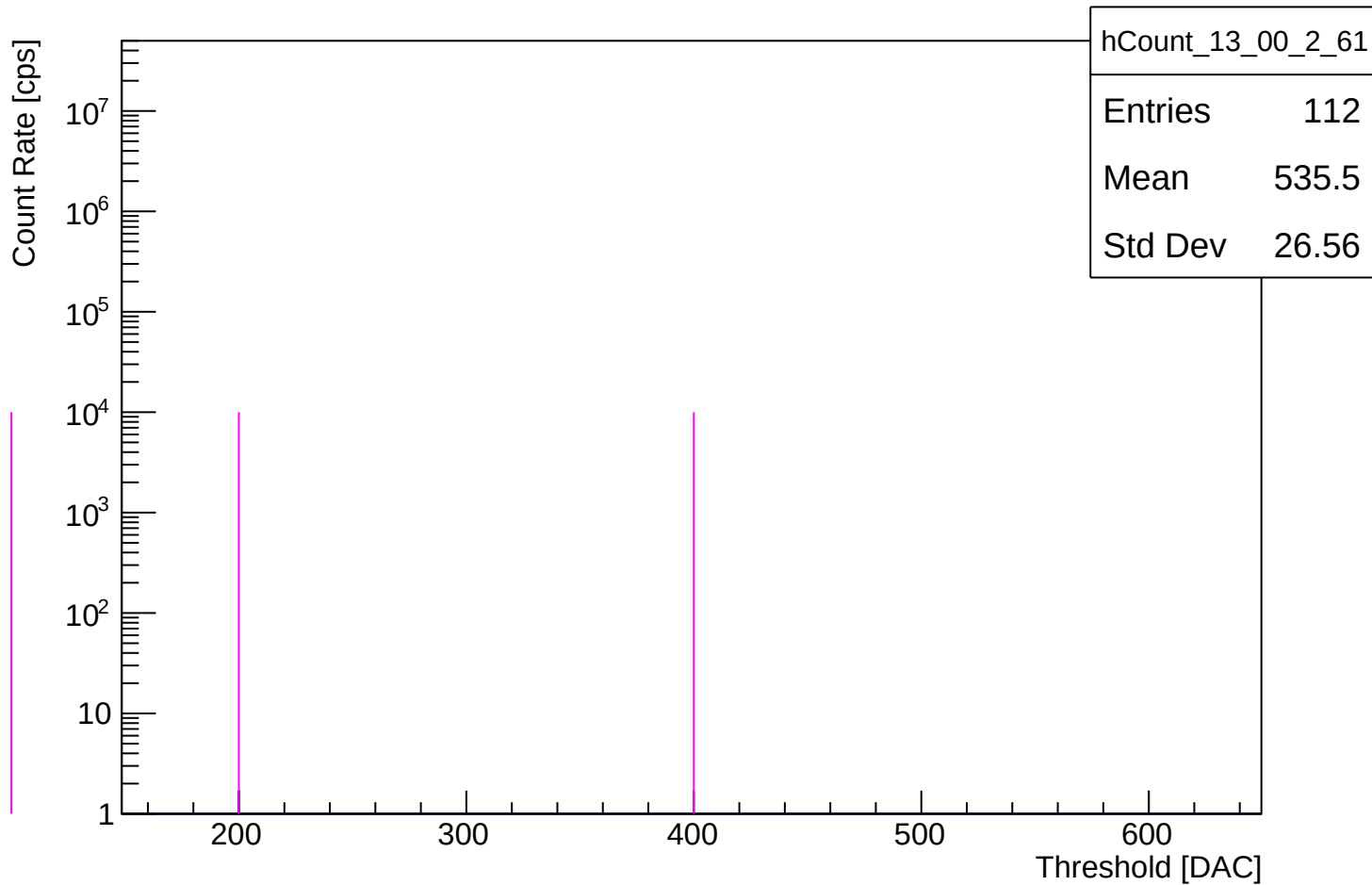
Row 1 Tile 1 Pmt 3 Pixel 61 Slot 13 Fiber 0 Asic 2 Channel 60



Row 1 Tile 1 Pmt 3 Pixel 62 Slot 13 Fiber 0 Asic 2 Channel 62



Row 1 Tile 1 Pmt 3 Pixel 63 Slot 13 Fiber 0 Asic 2 Channel 61



Row 1 Tile 1 Pmt 3 Pixel 64 Slot 13 Fiber 0 Asic 2 Channel 63

