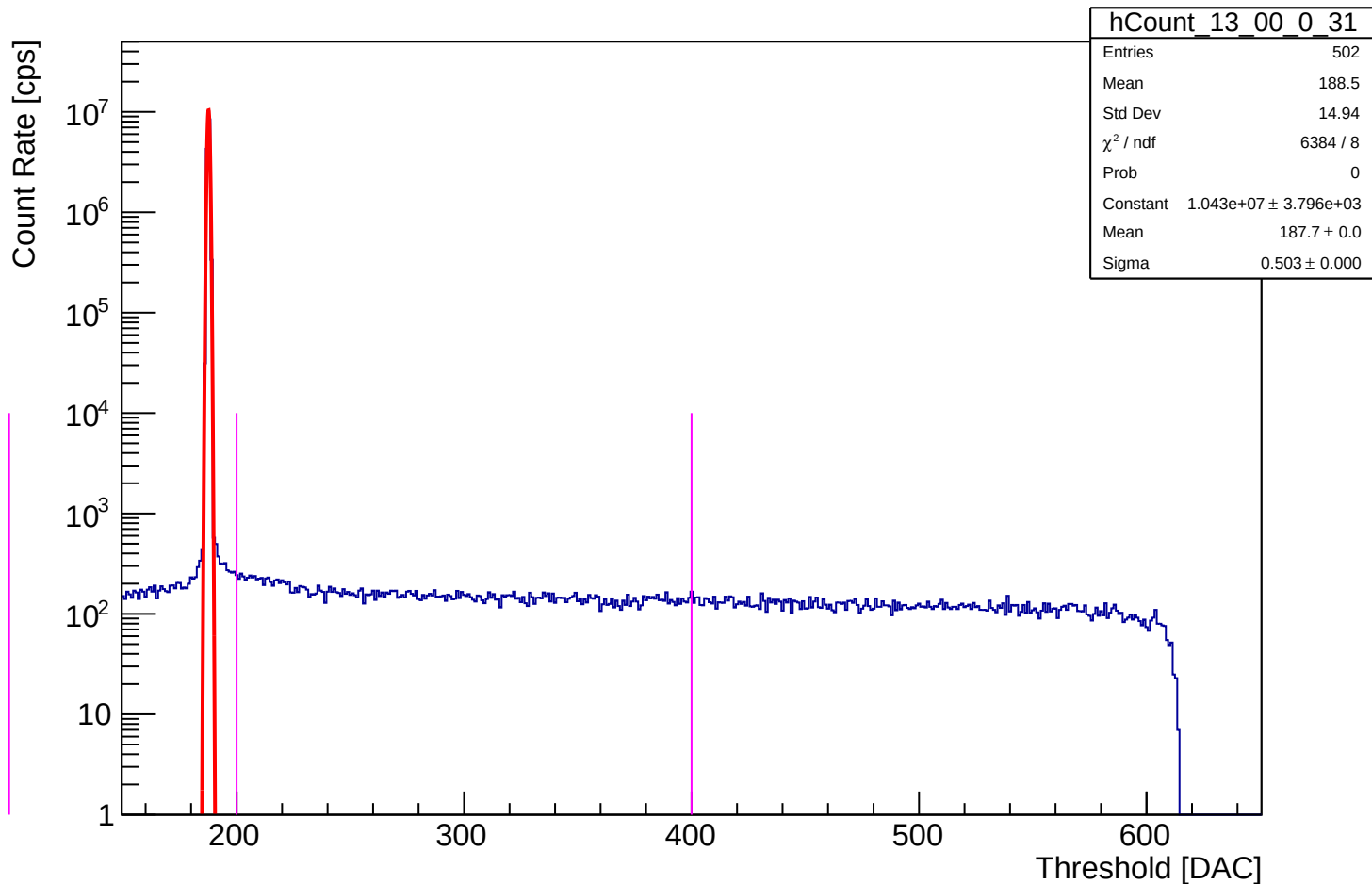
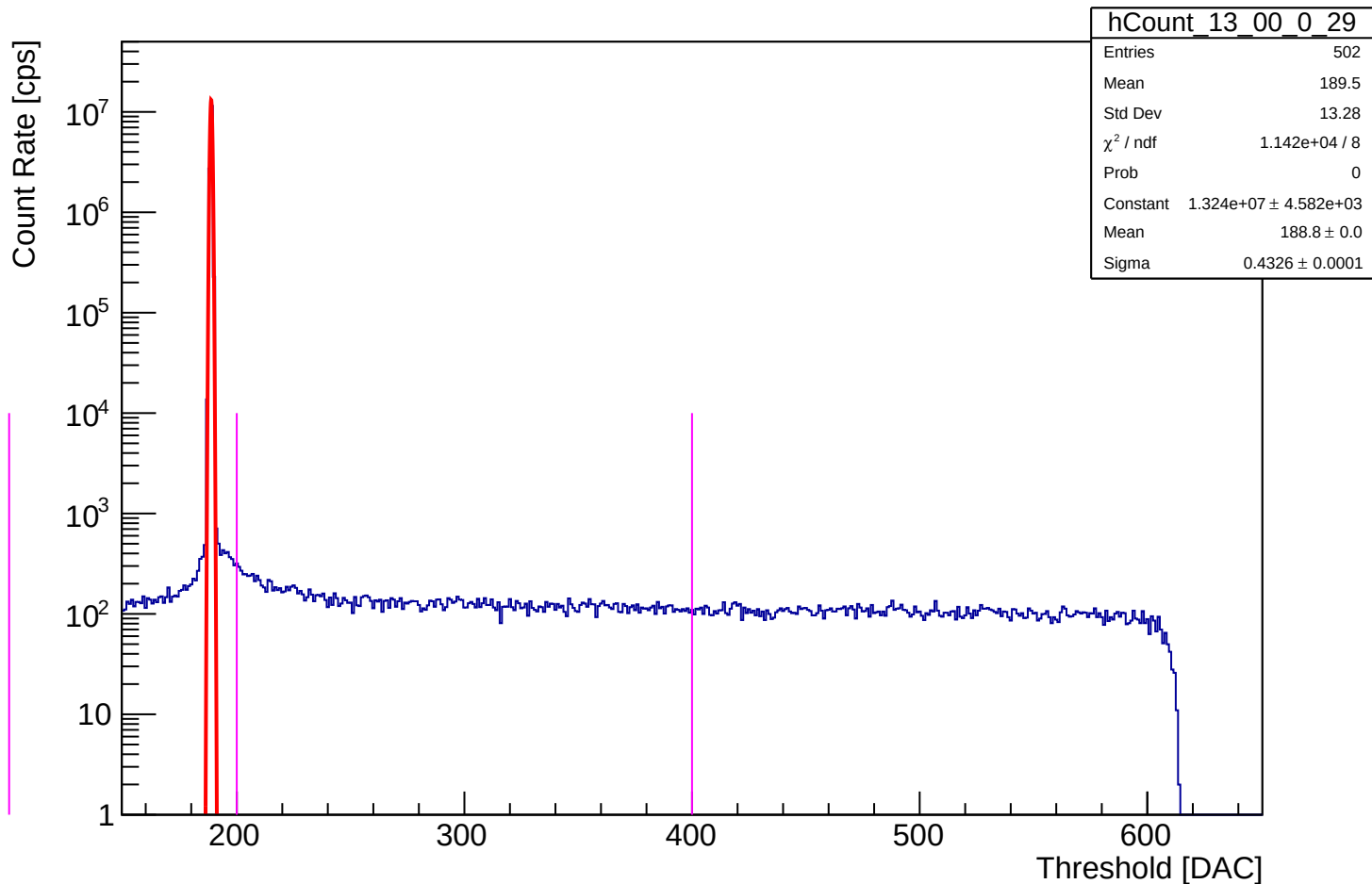


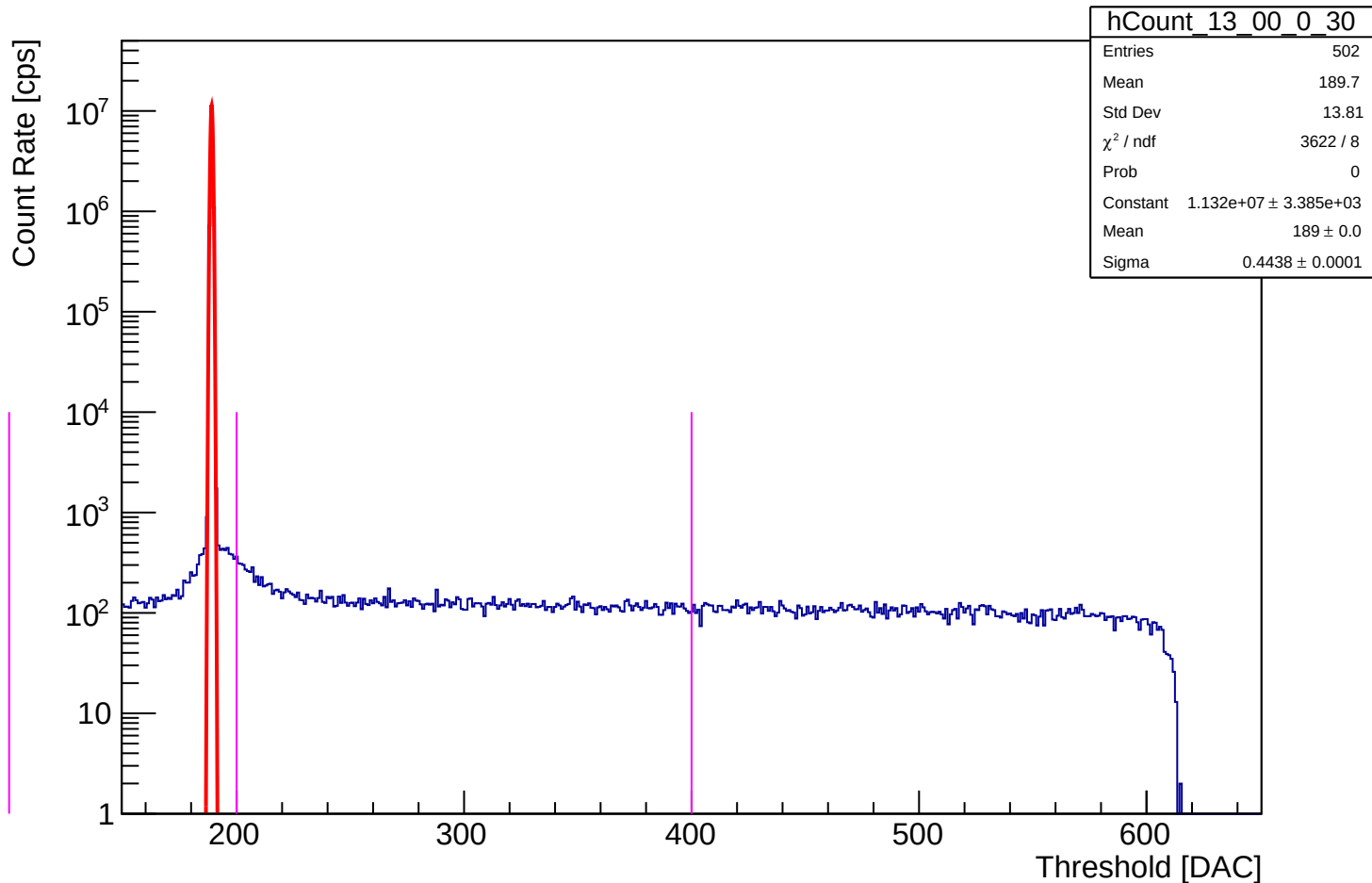
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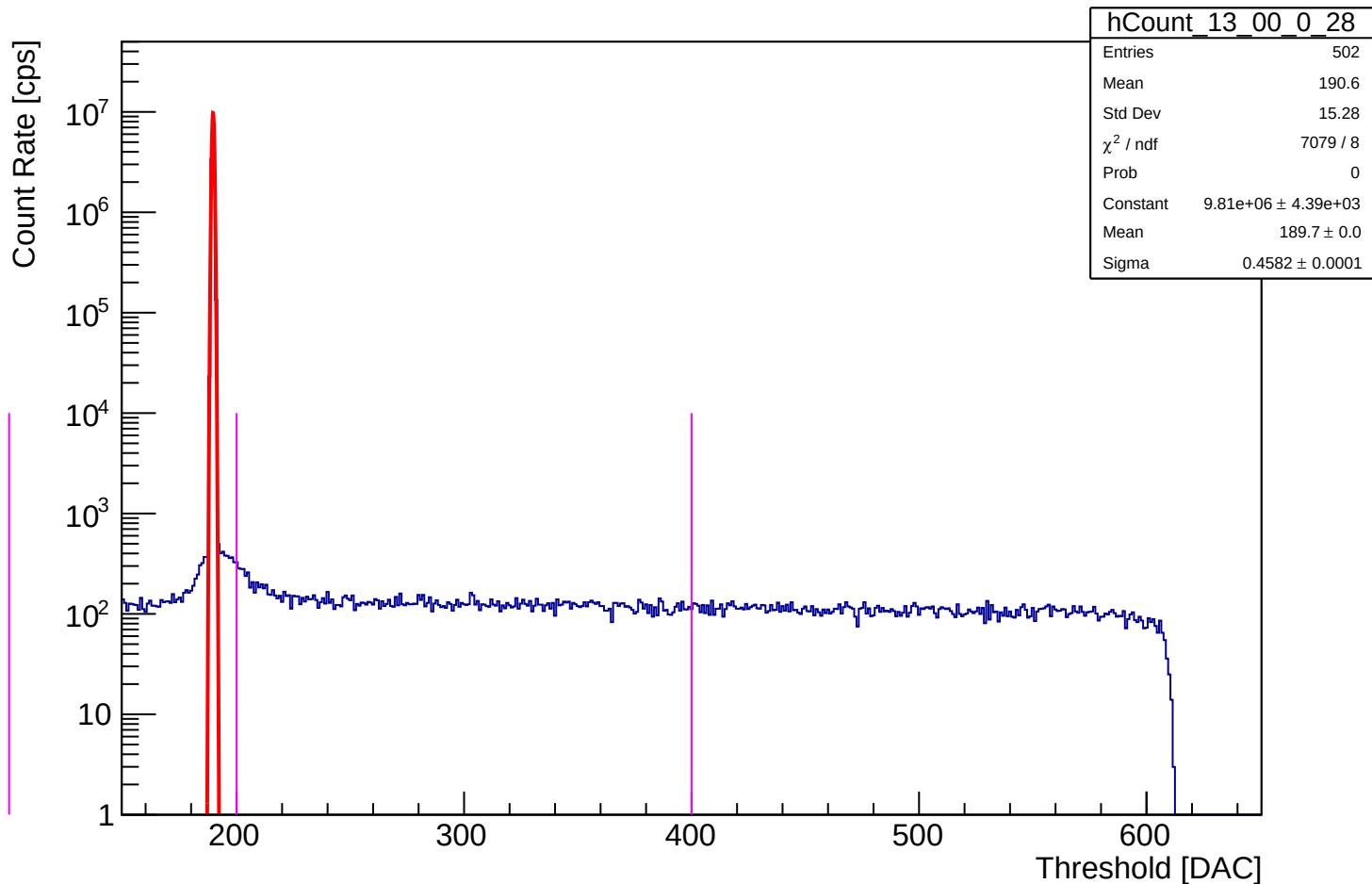
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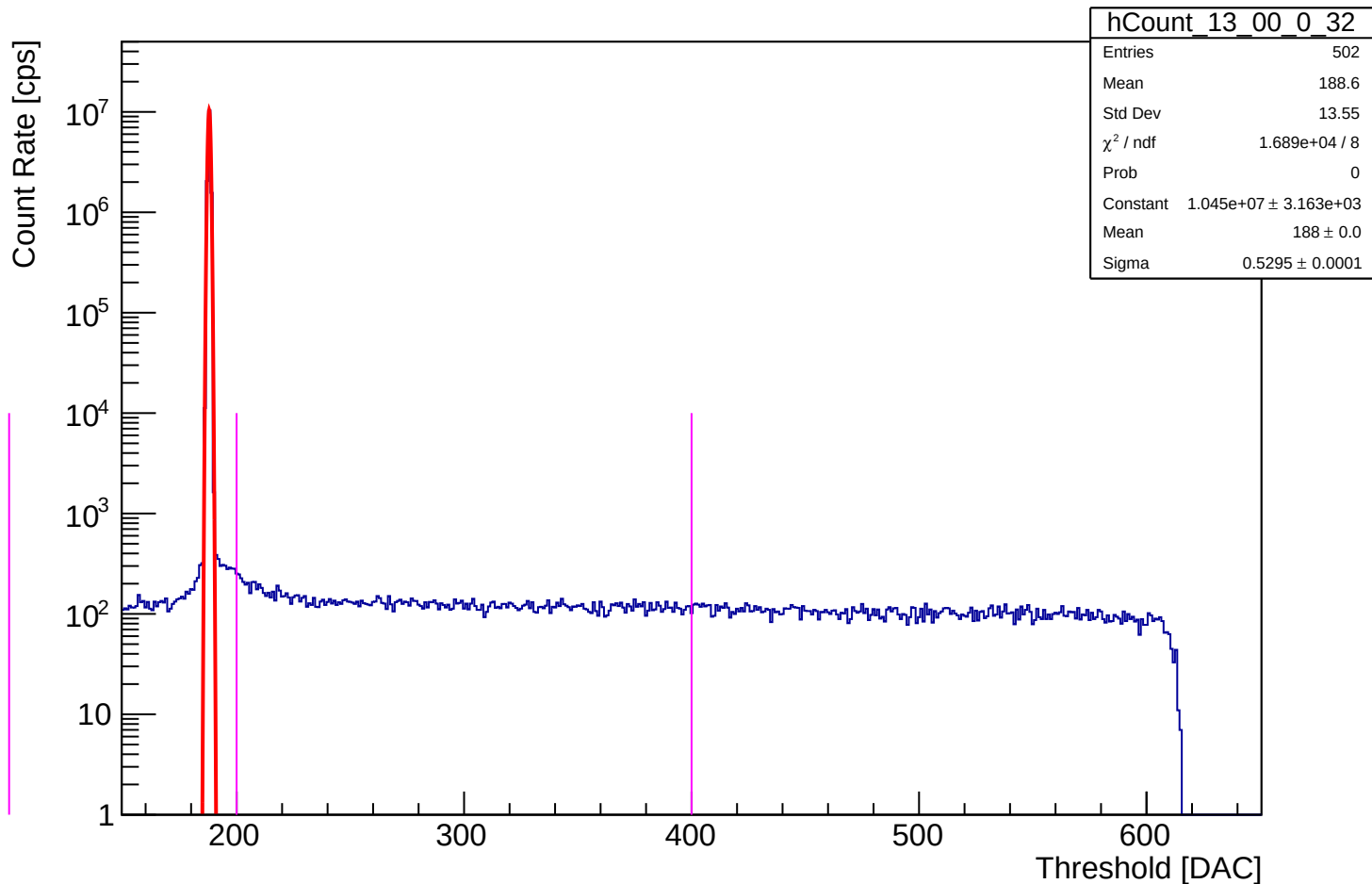
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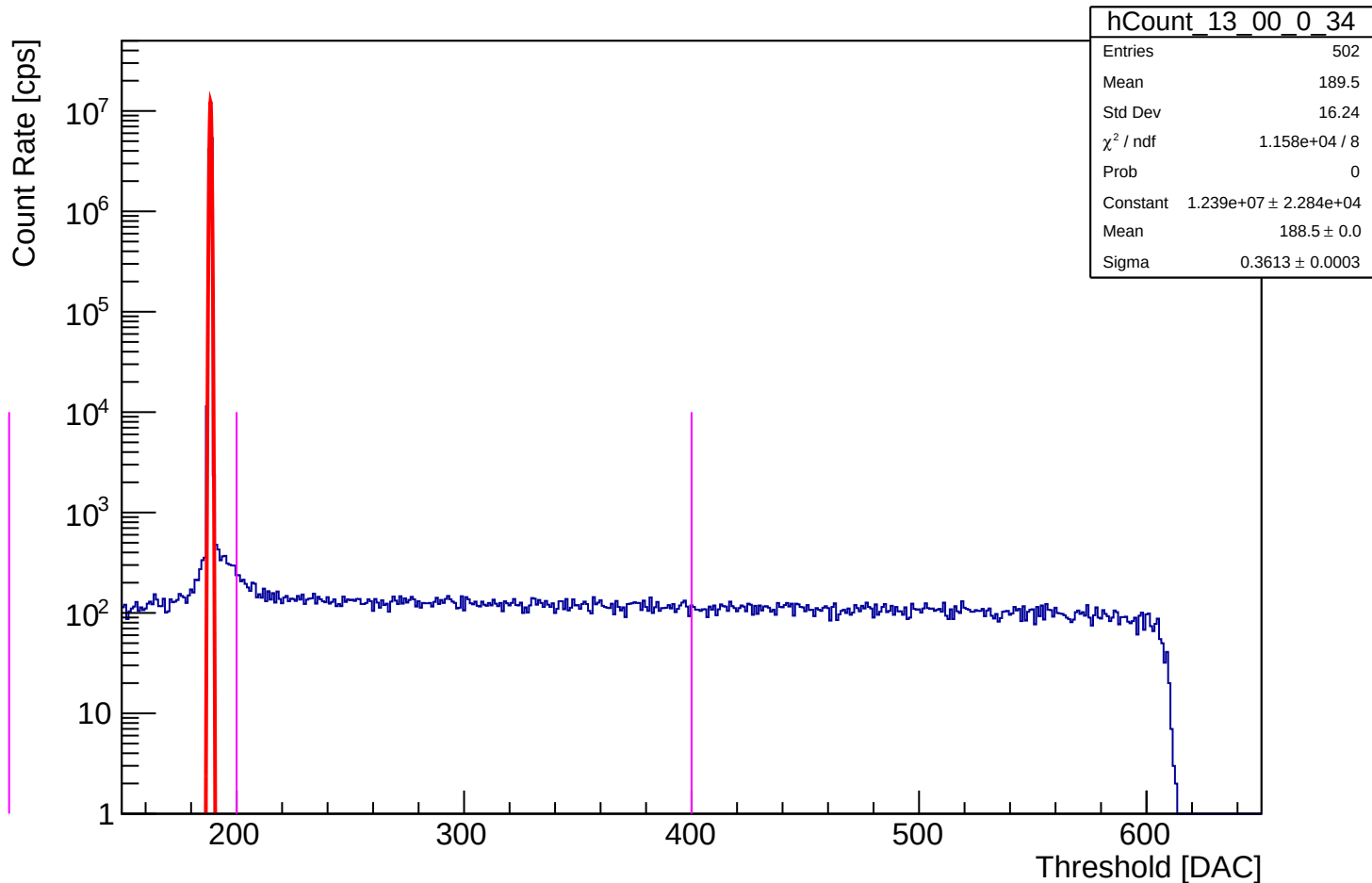
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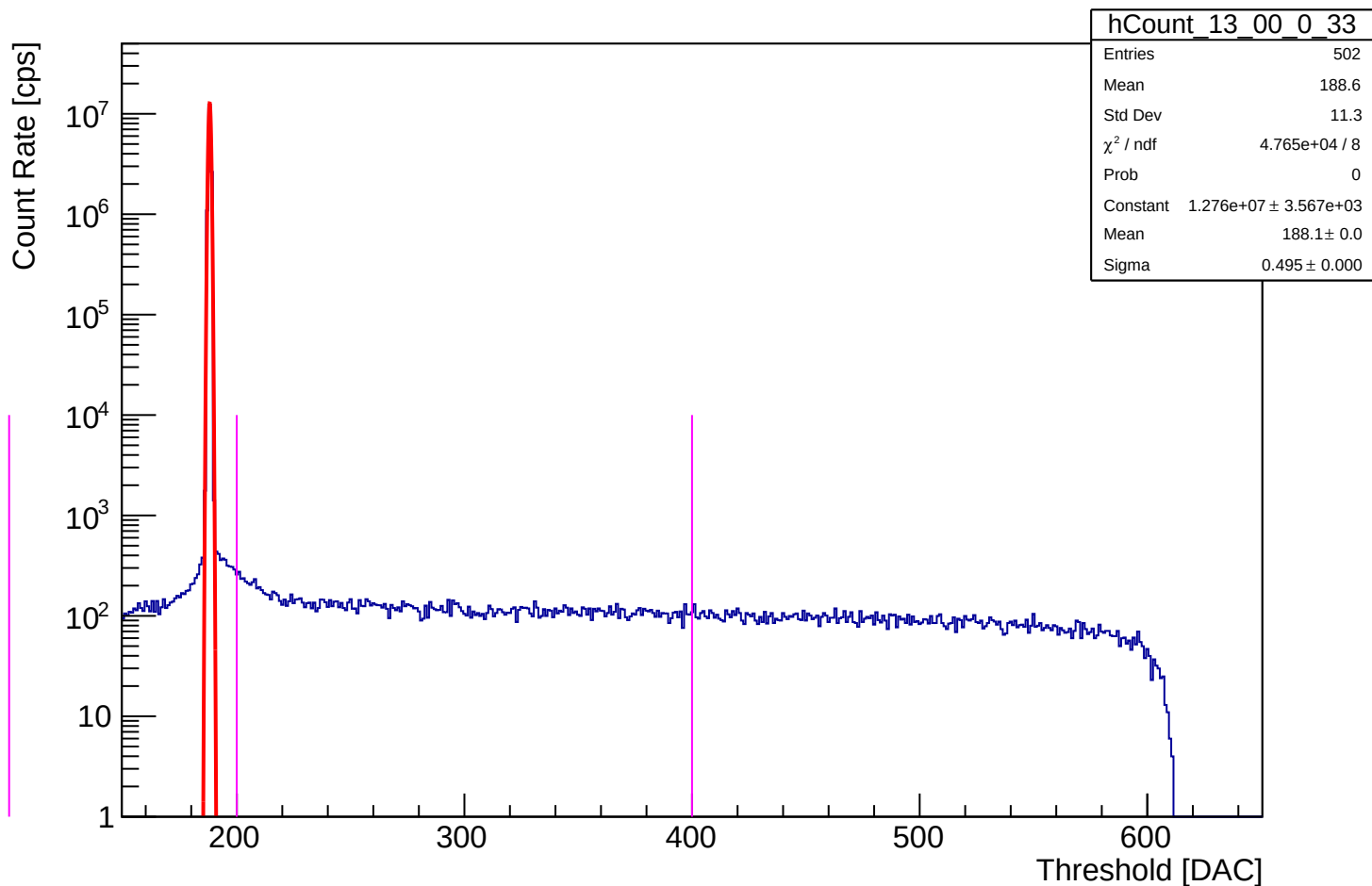
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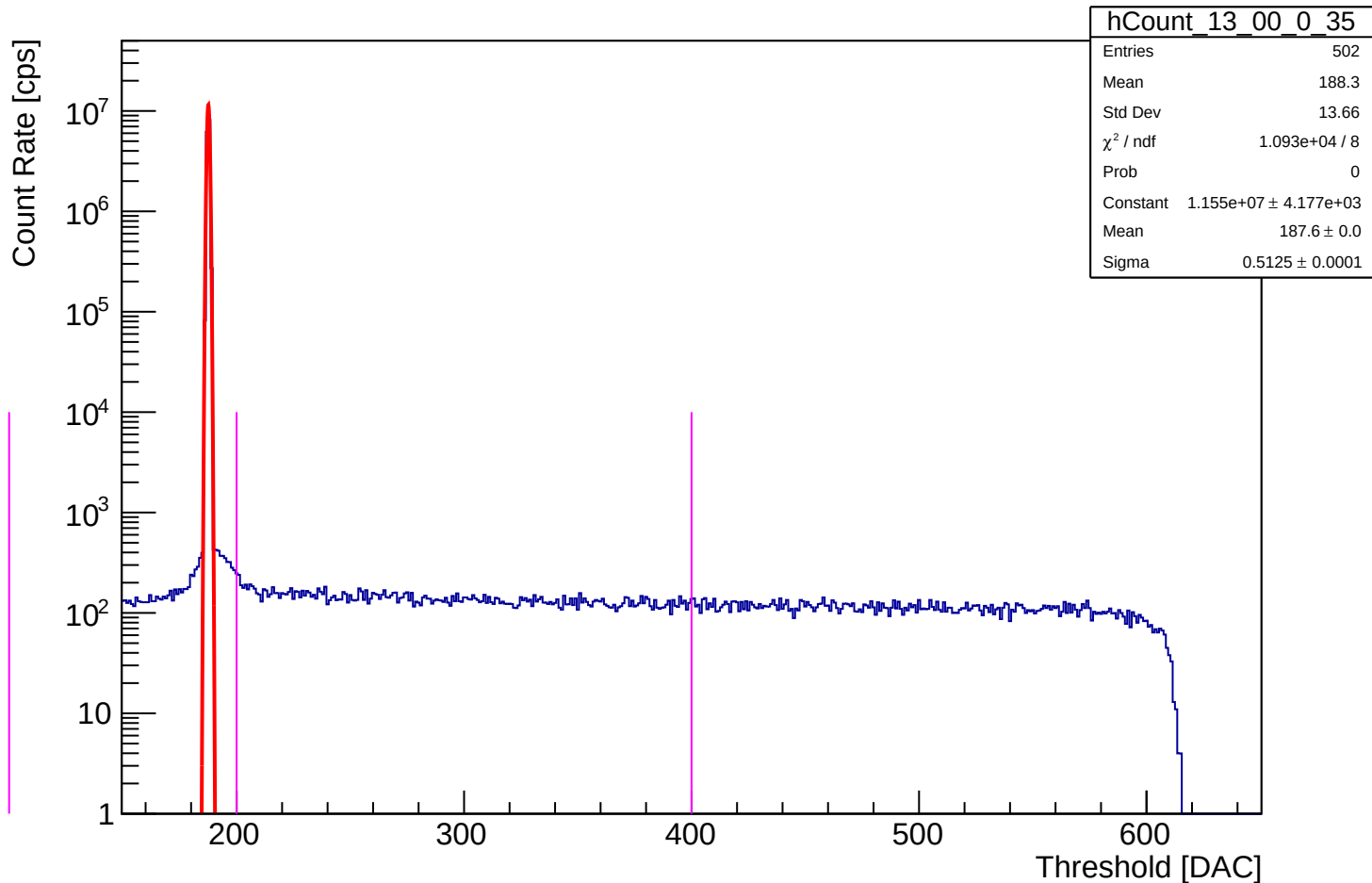
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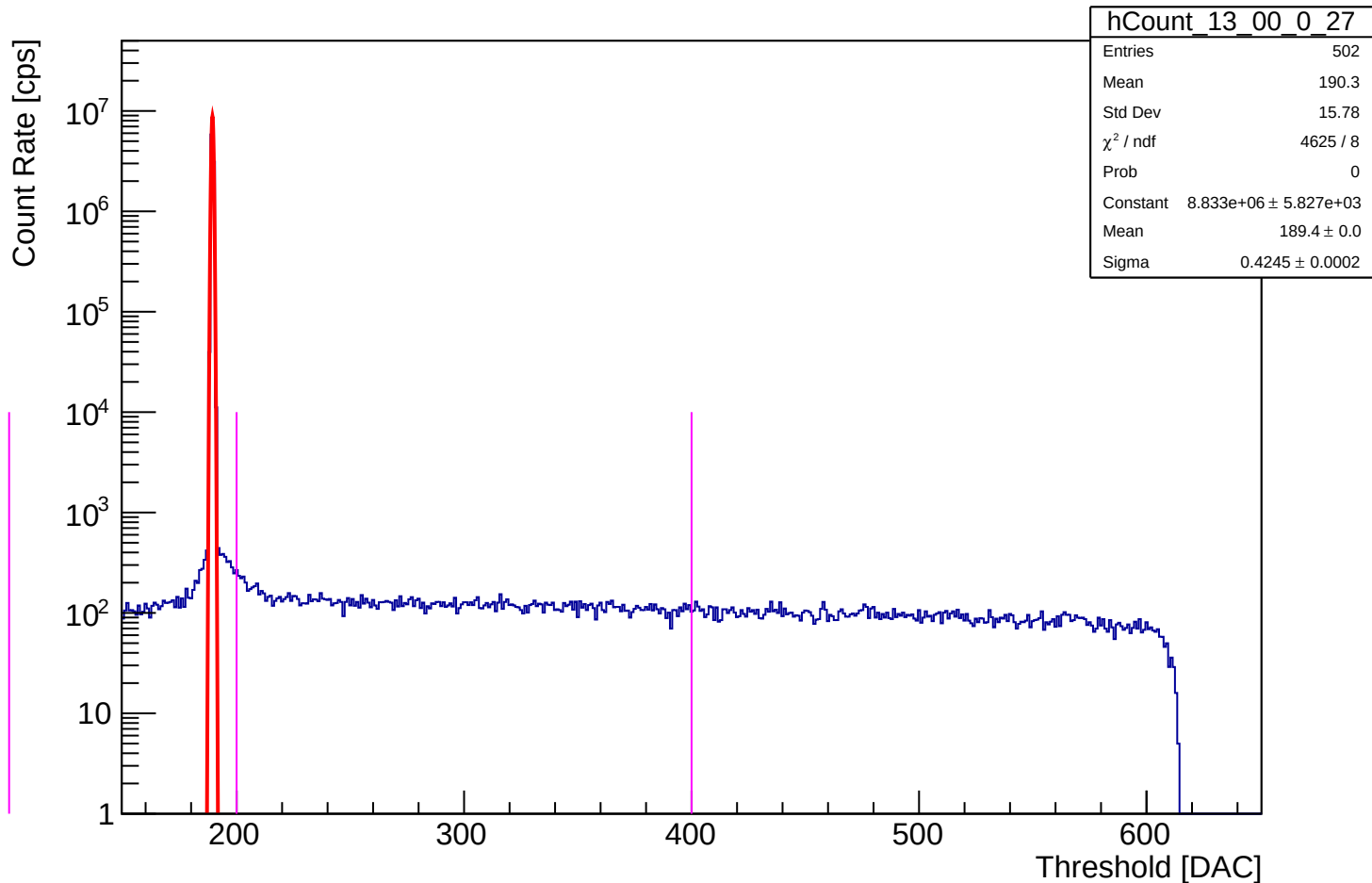
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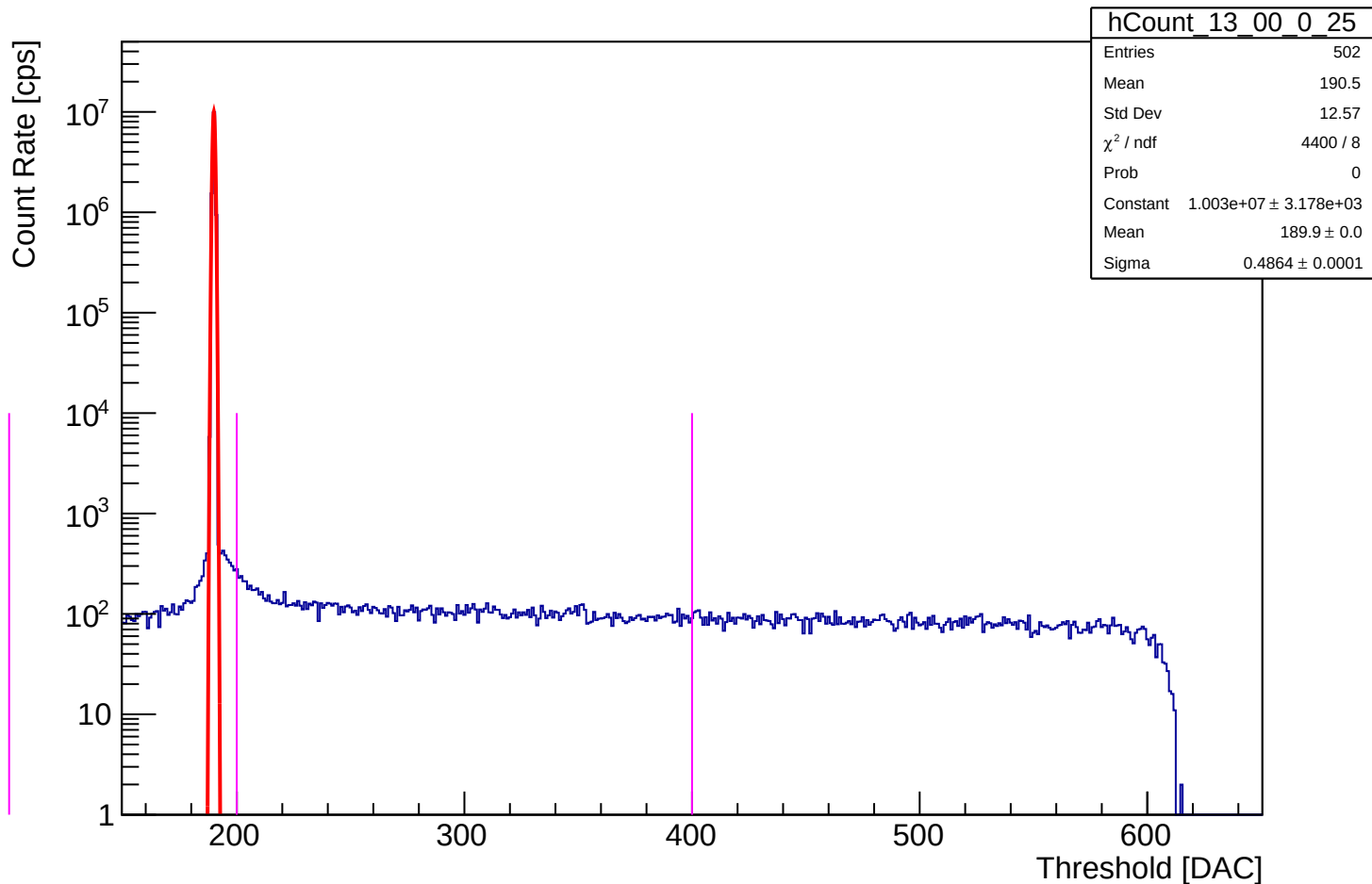
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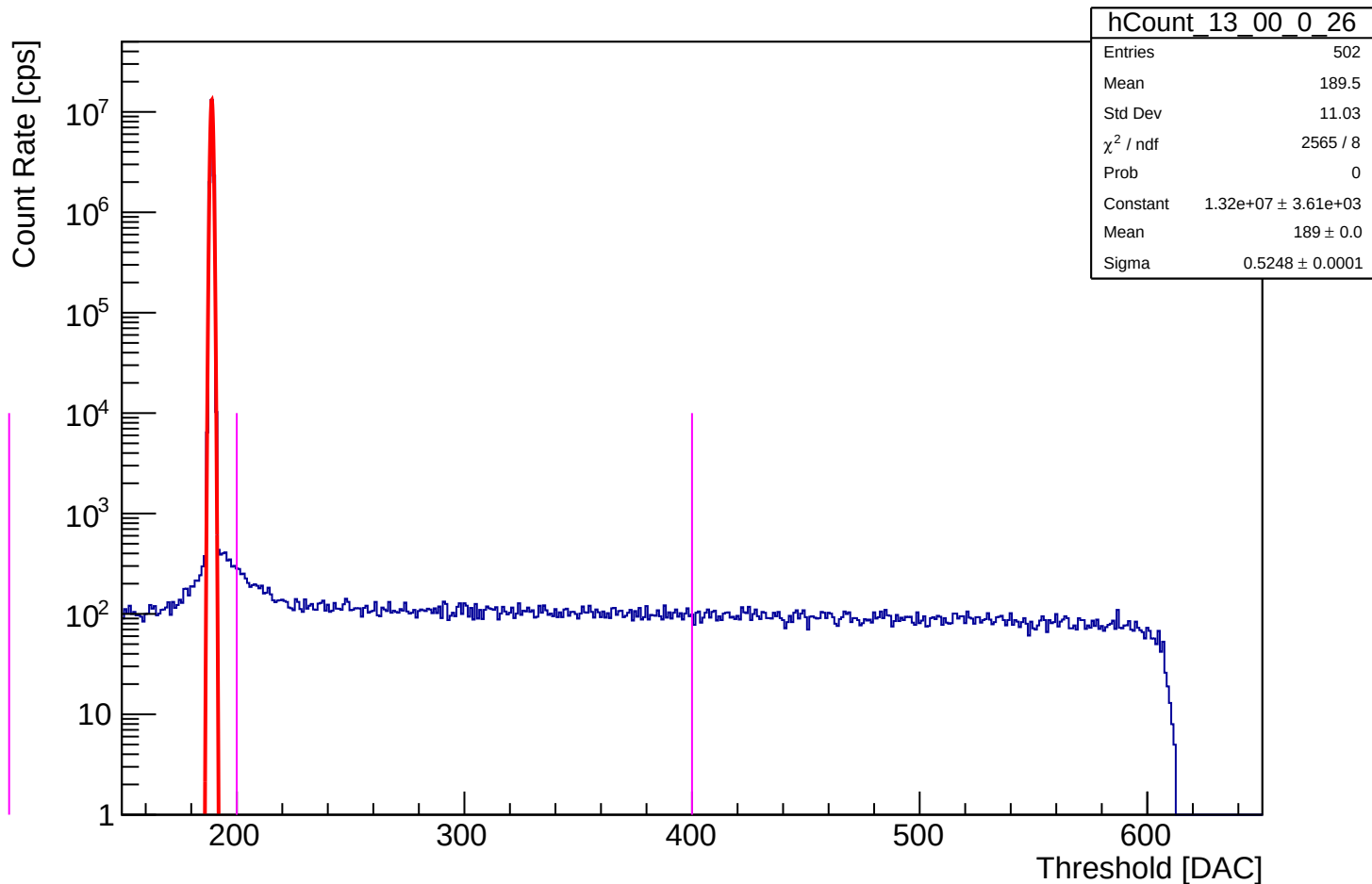
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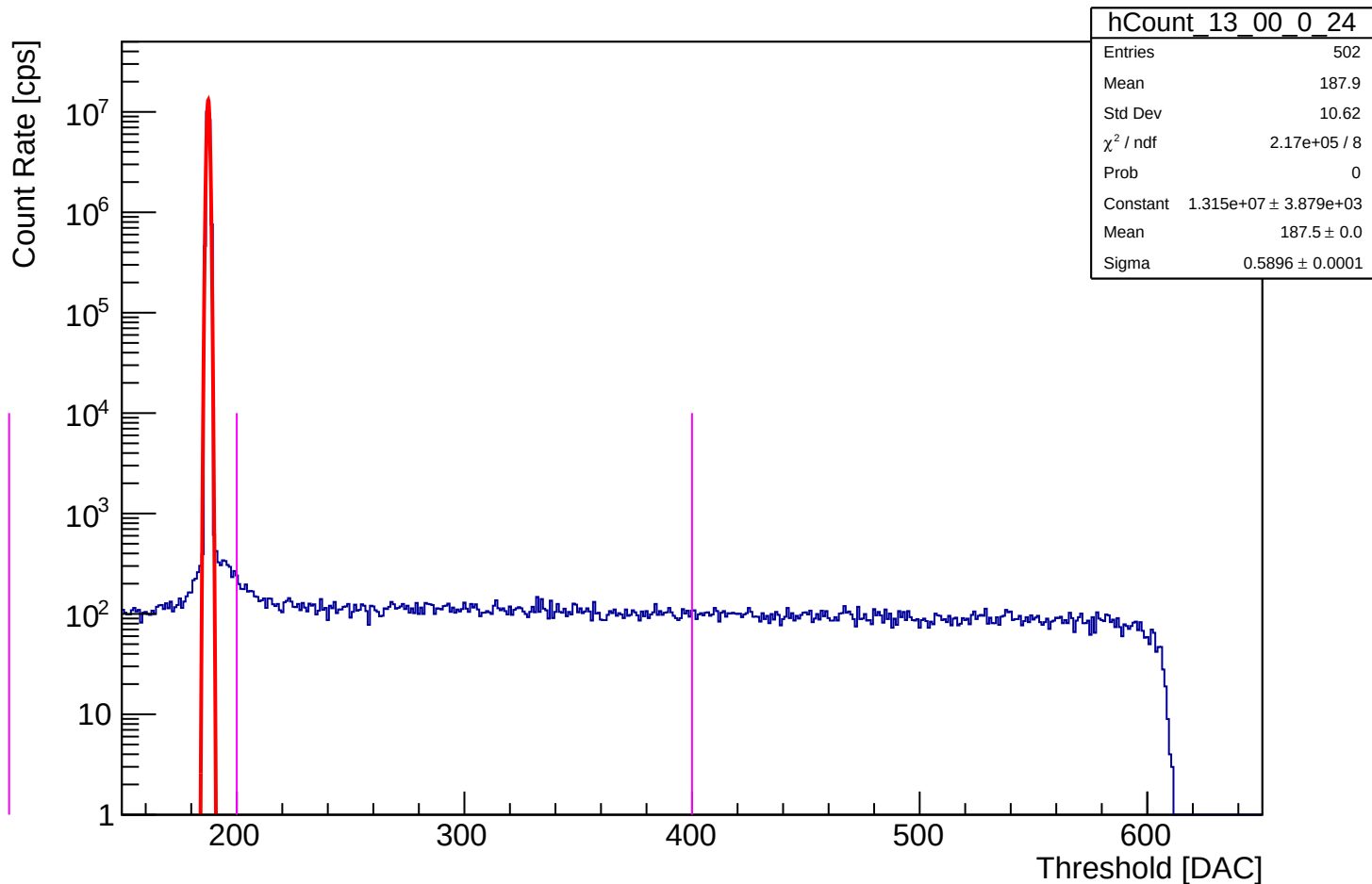
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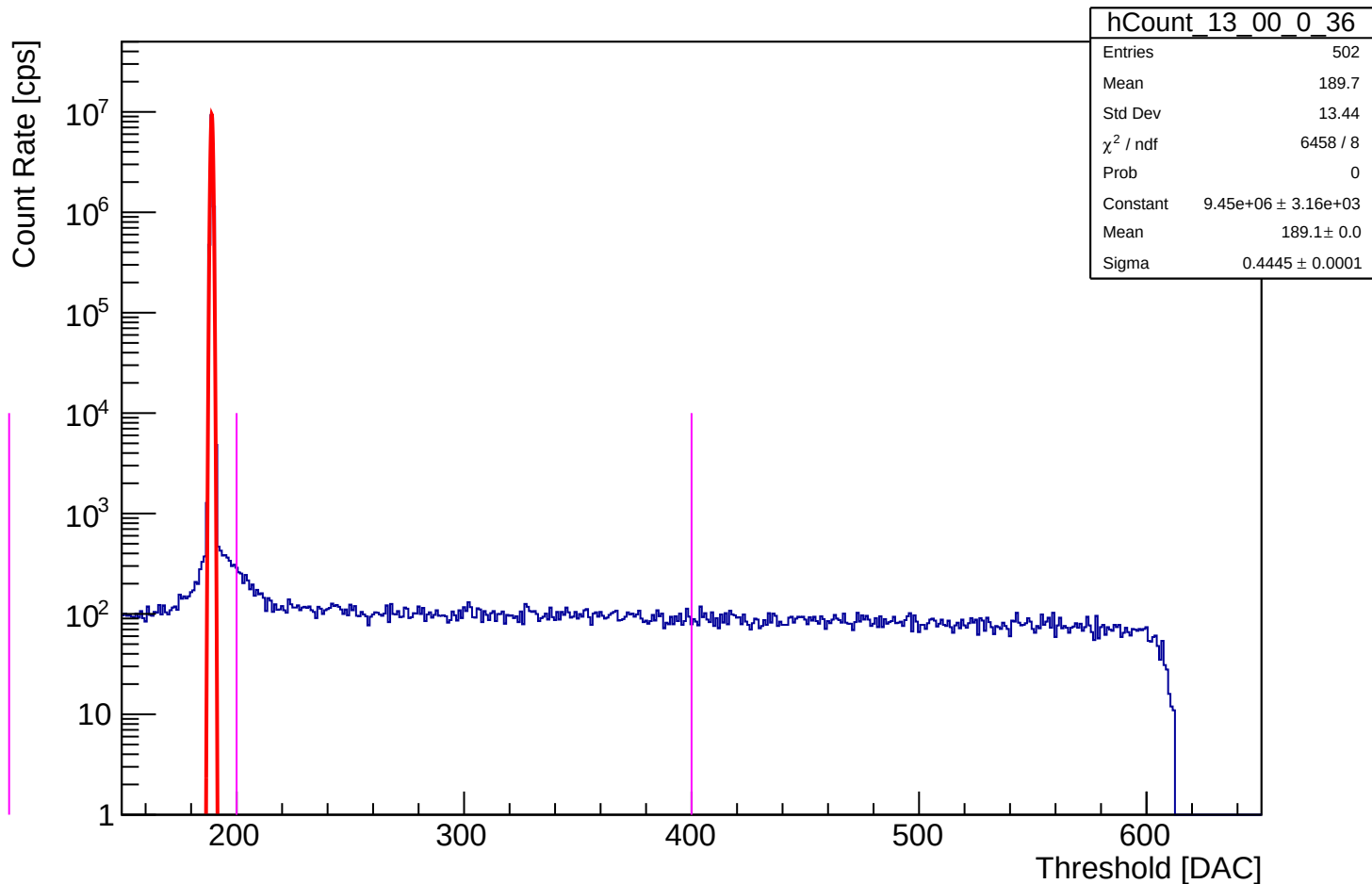
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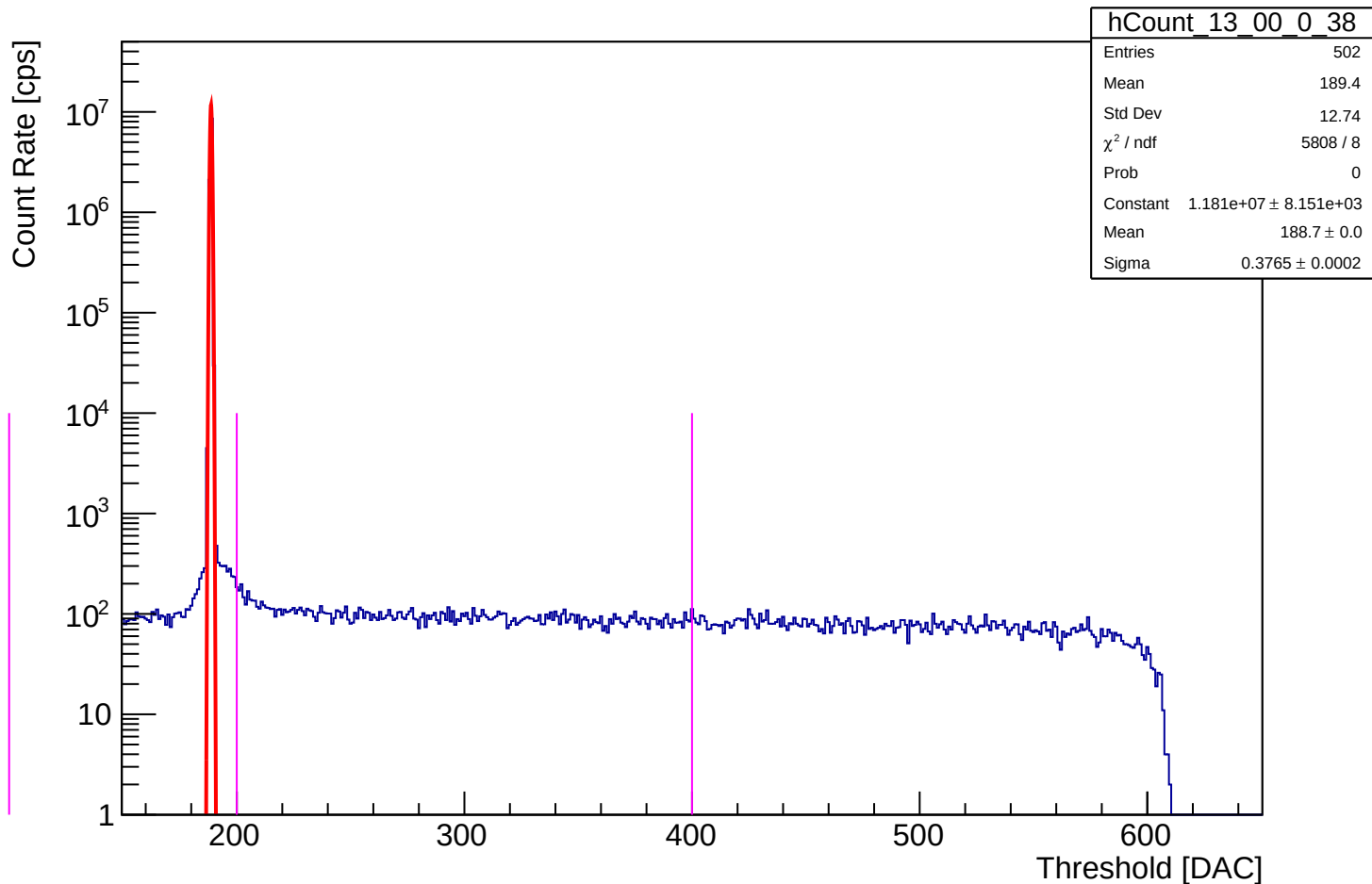
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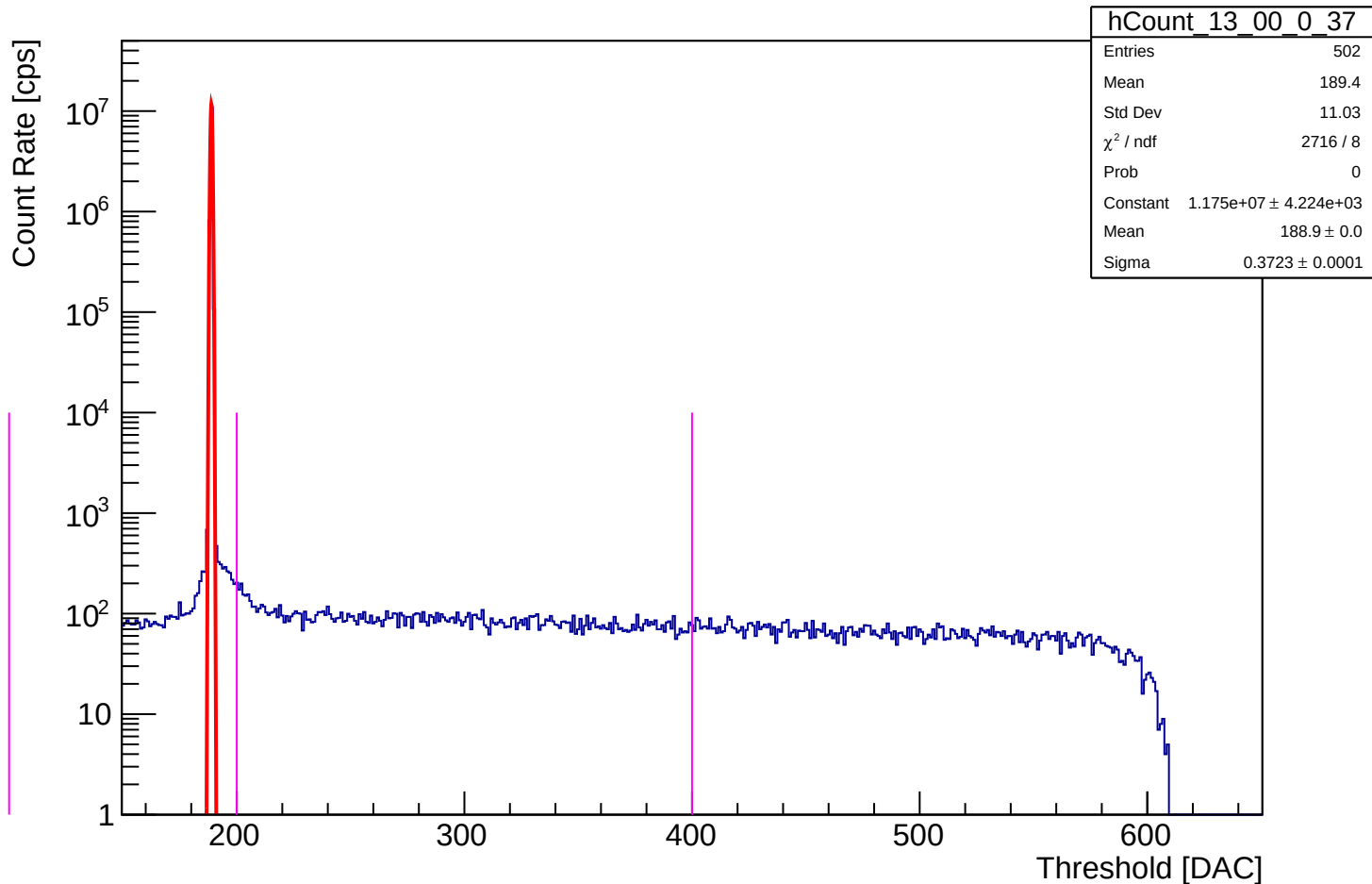
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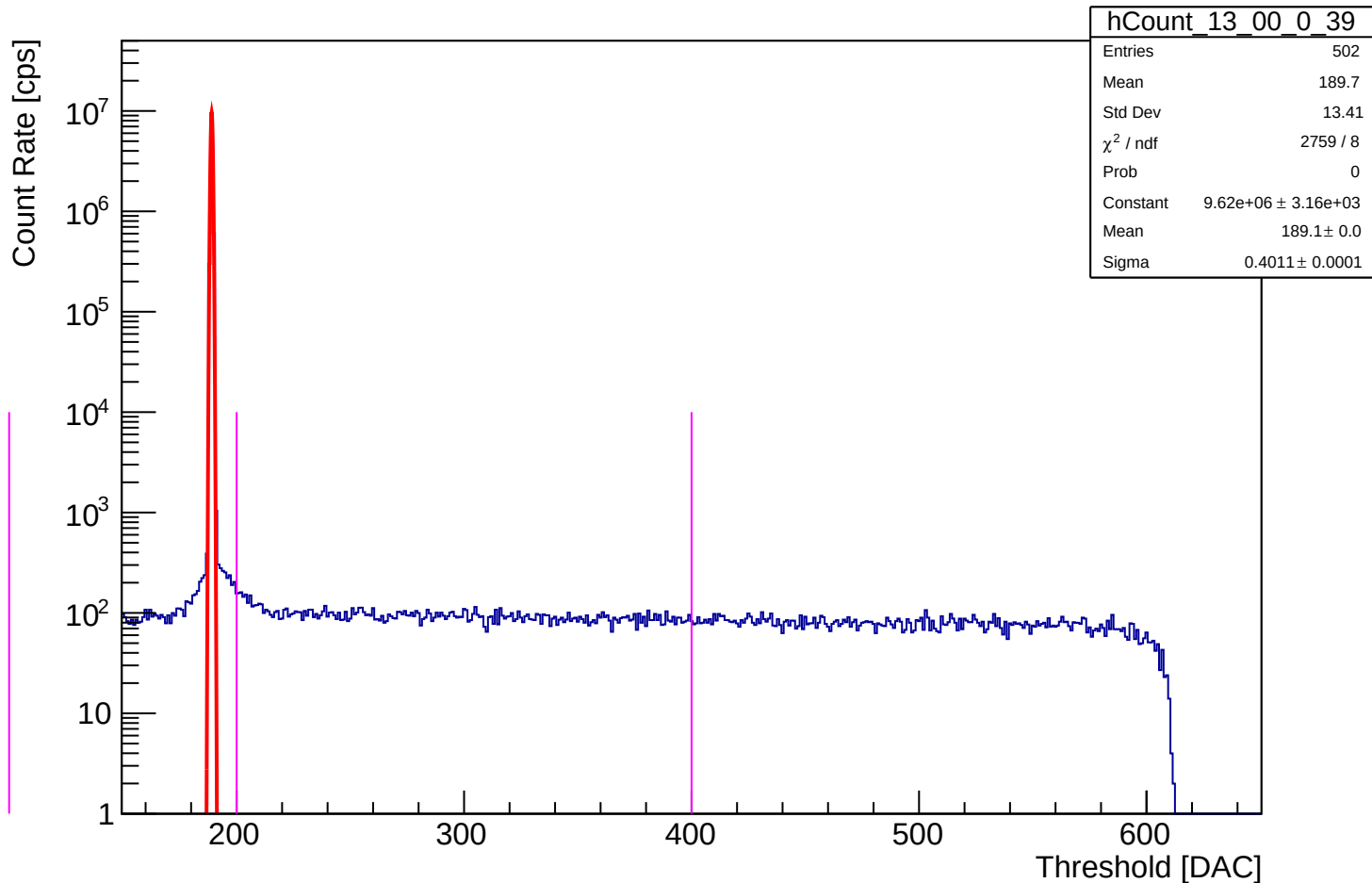
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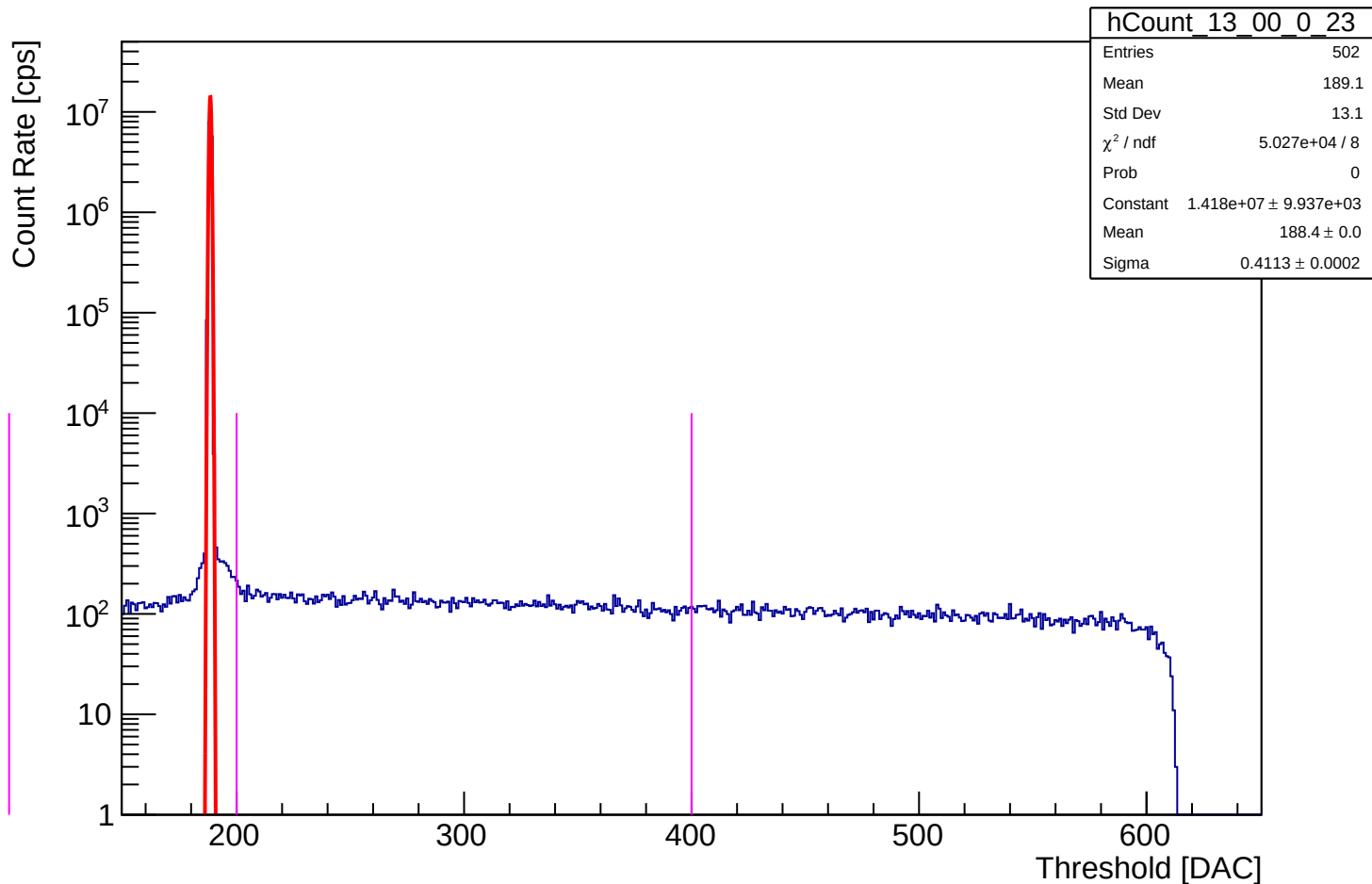
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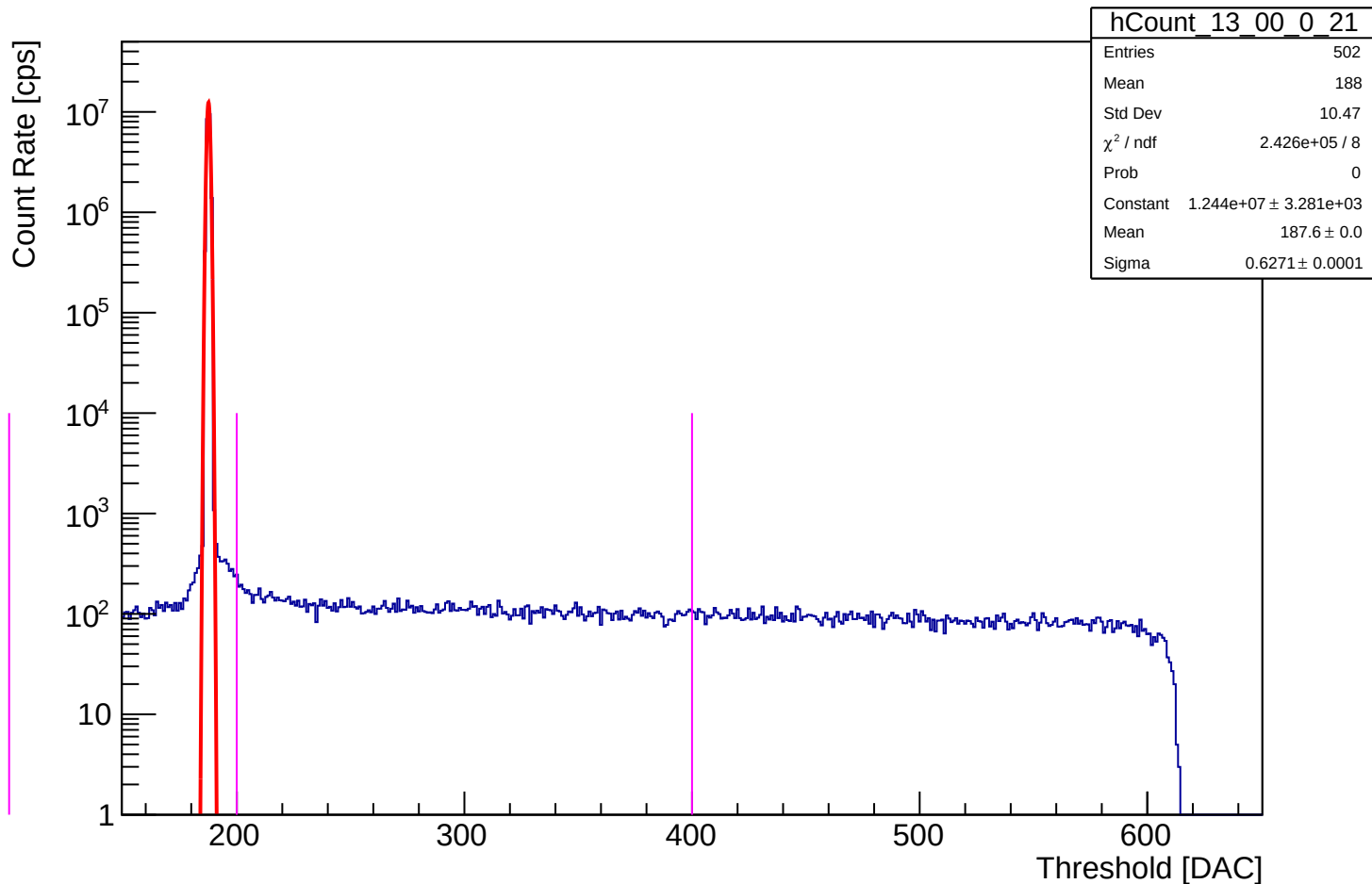
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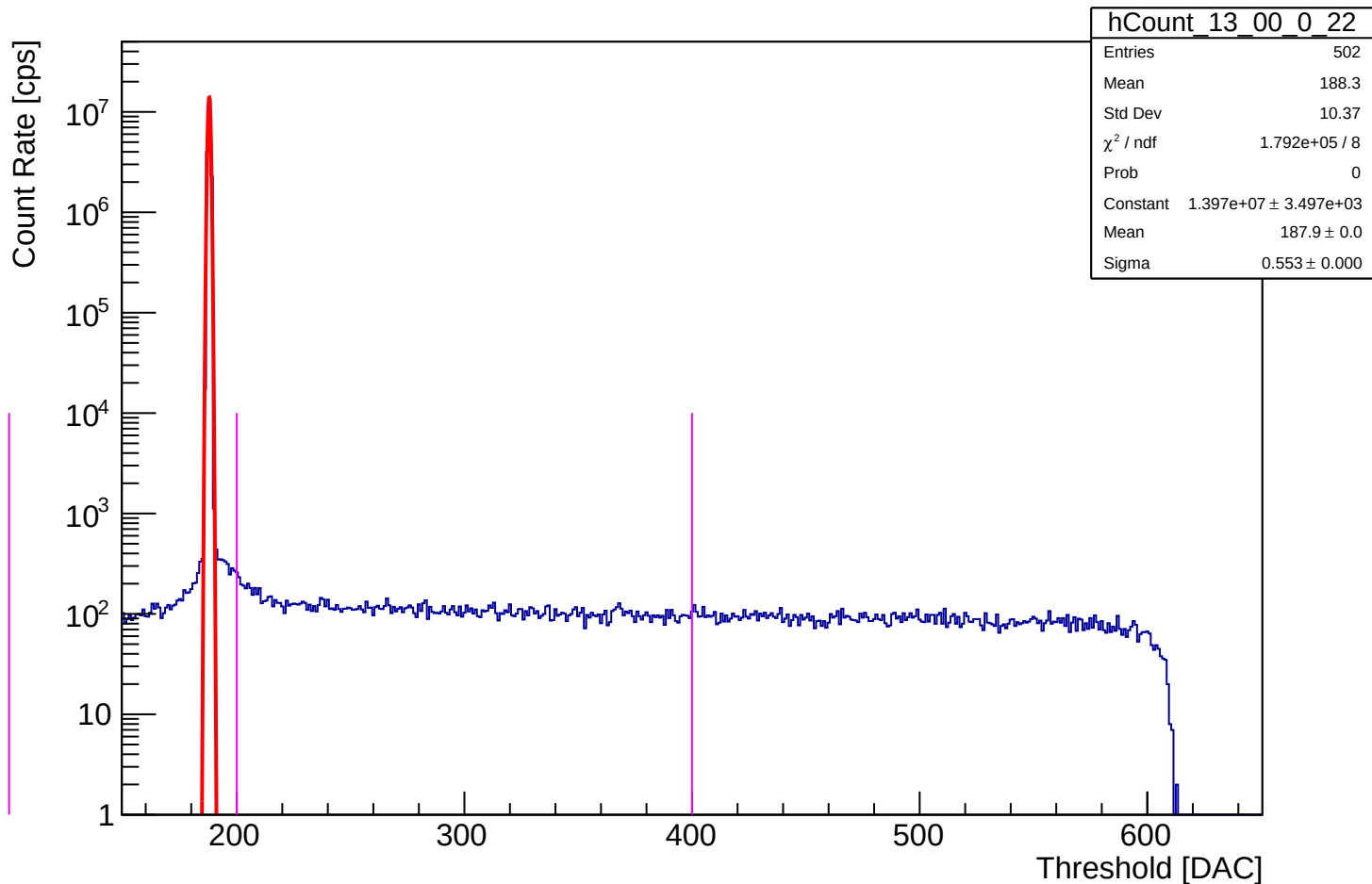
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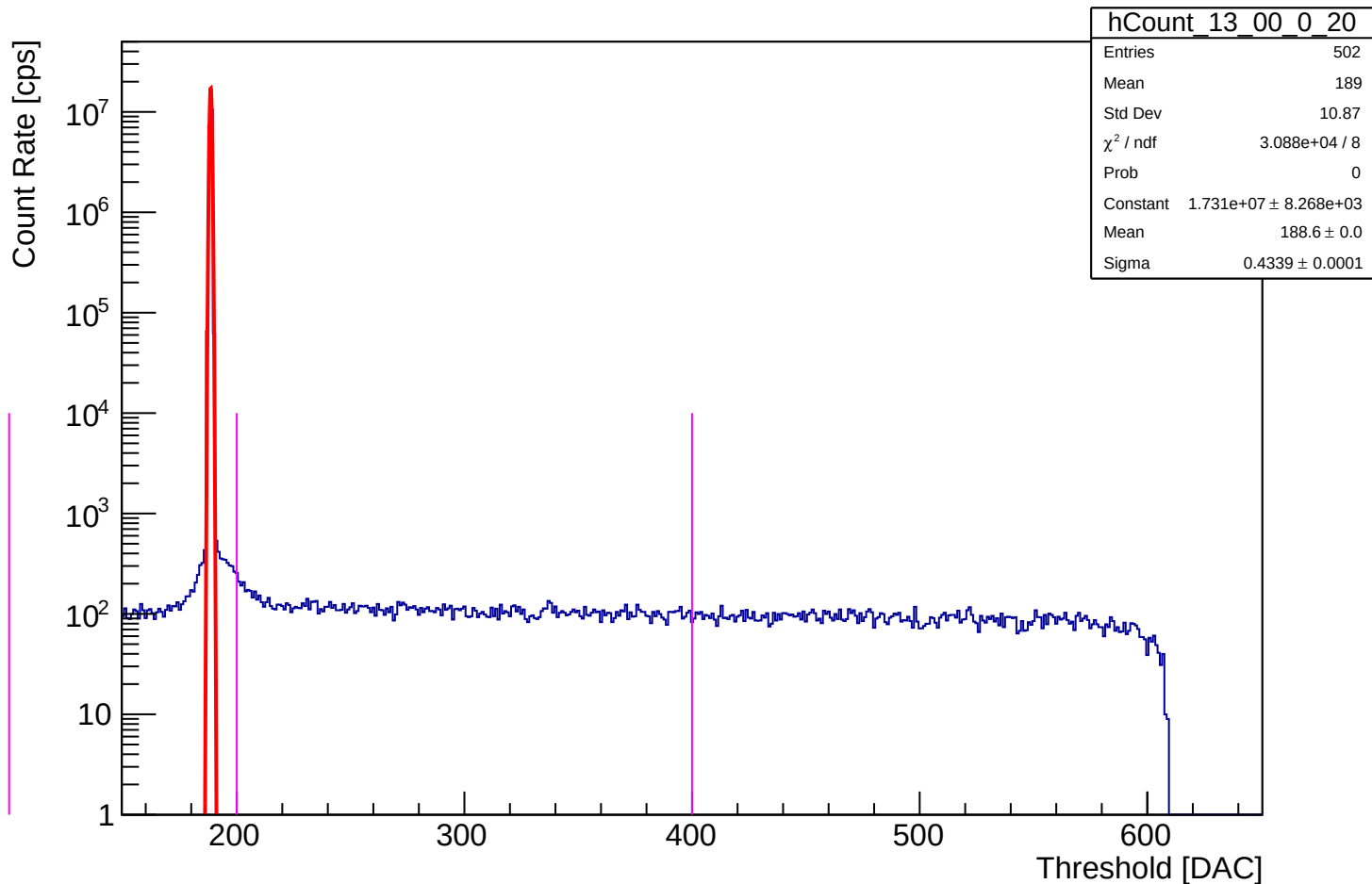
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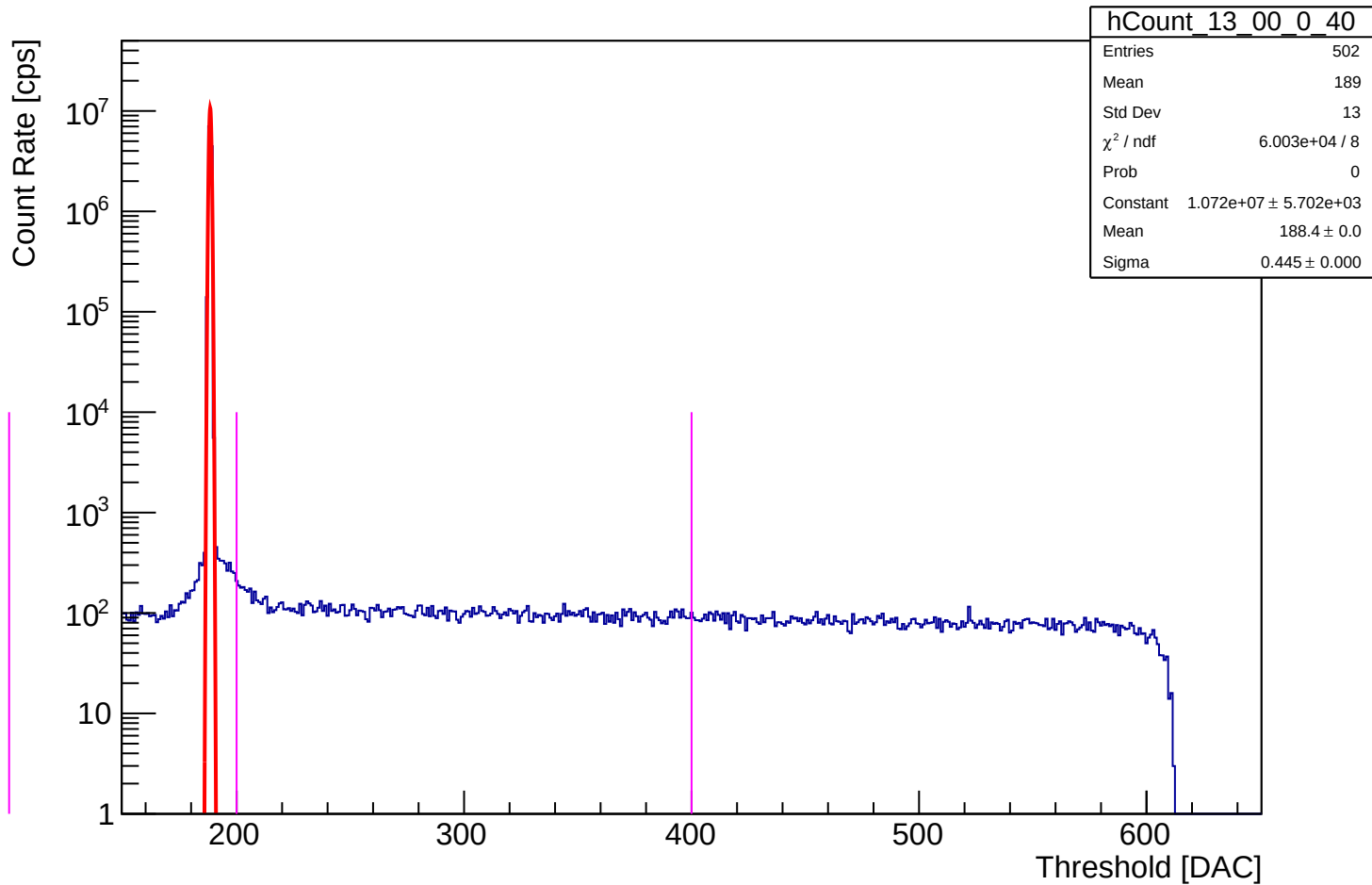
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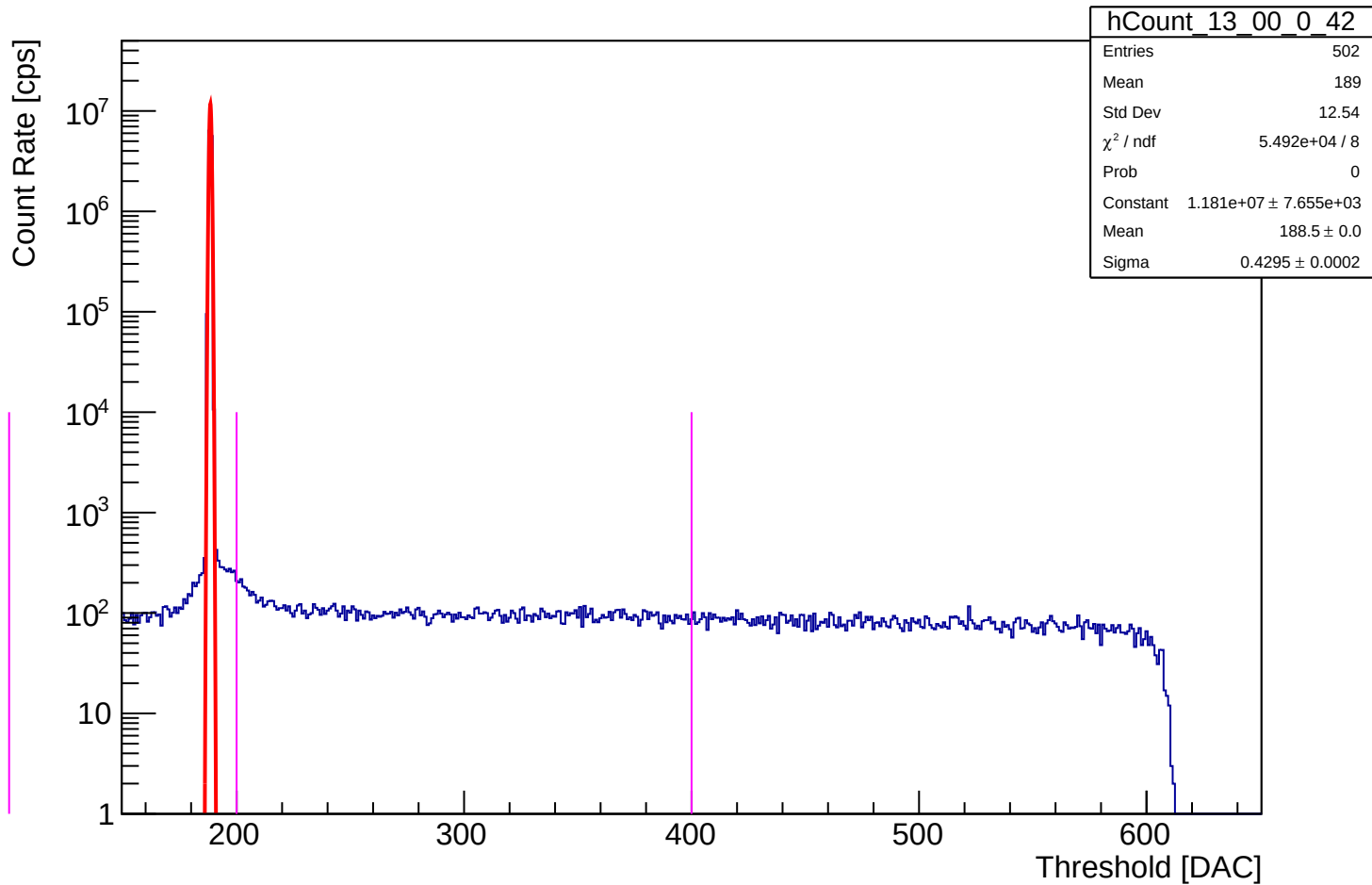
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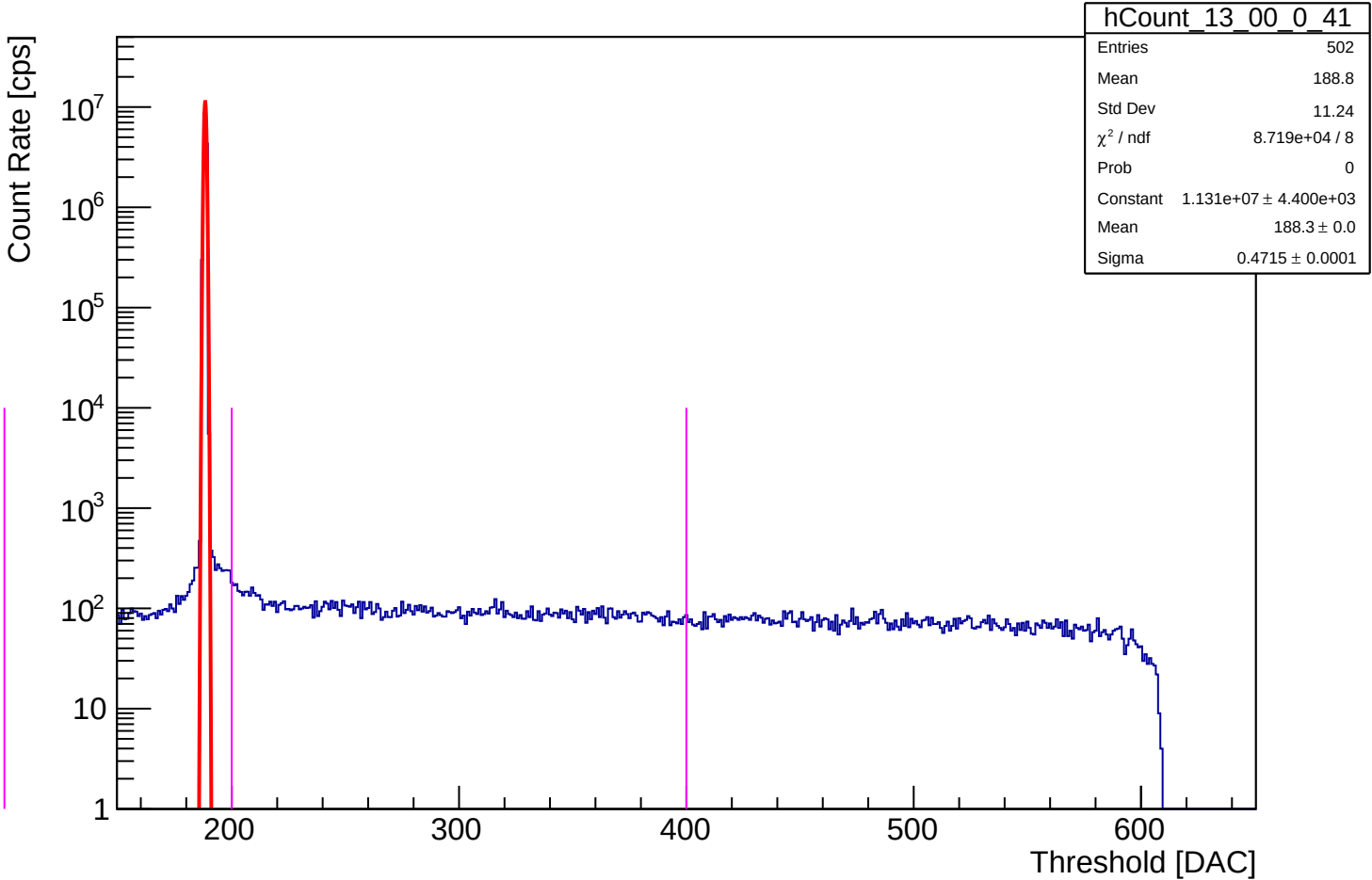


Row 1 Tile 1 Pmt 1 Pixel 21 Slot 13 Fiber 0 Asic 0 Channel 40

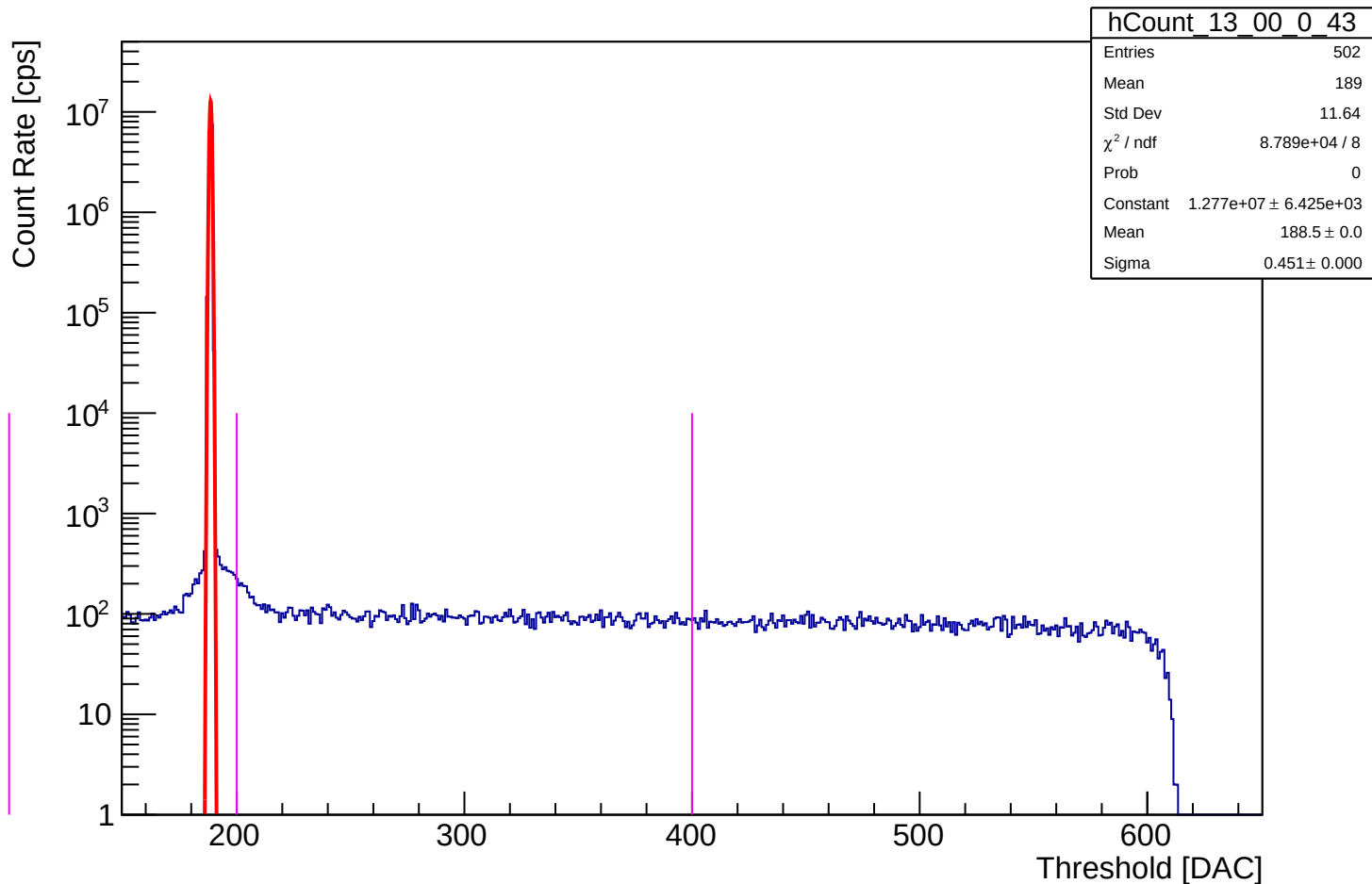


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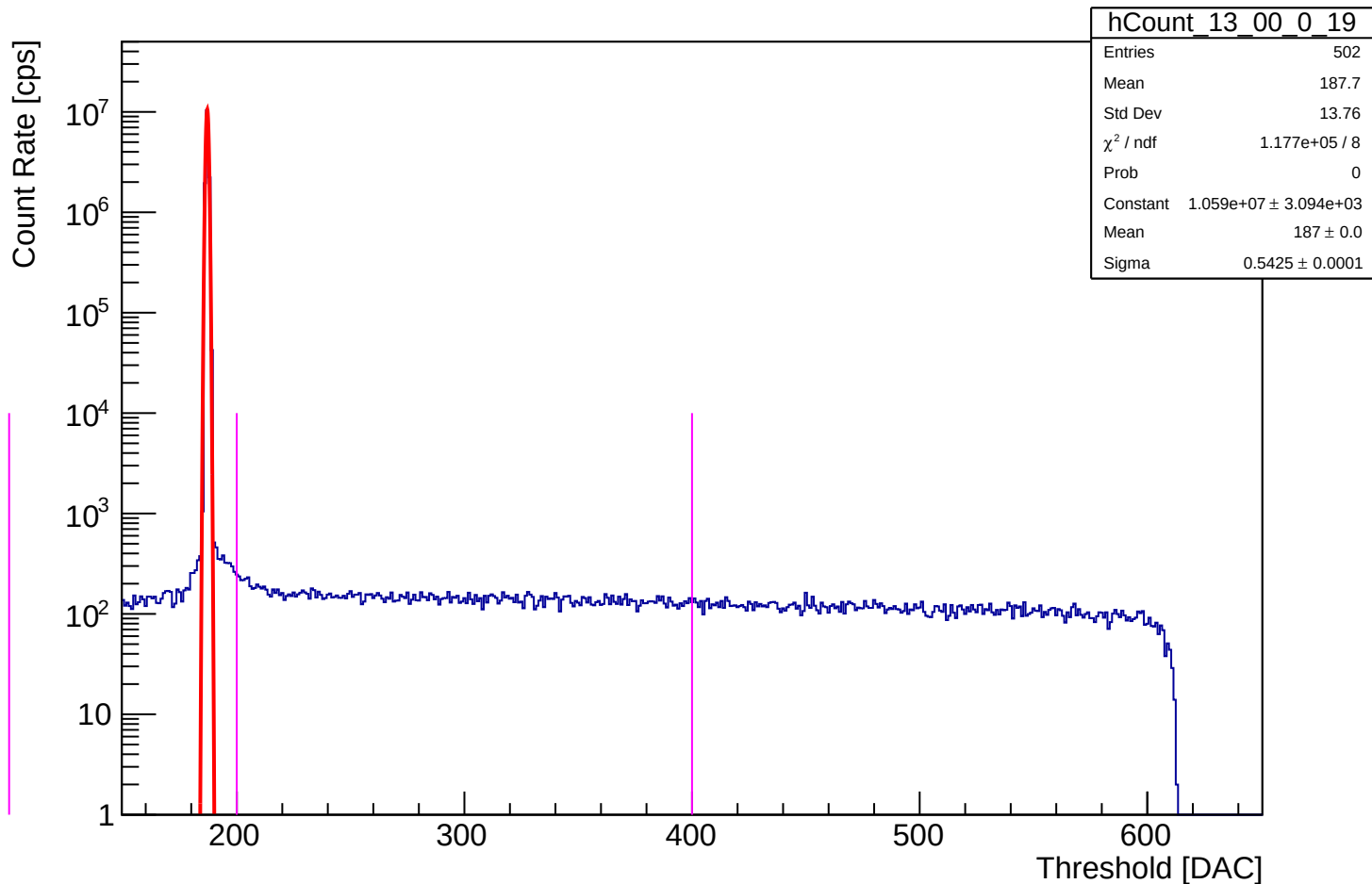




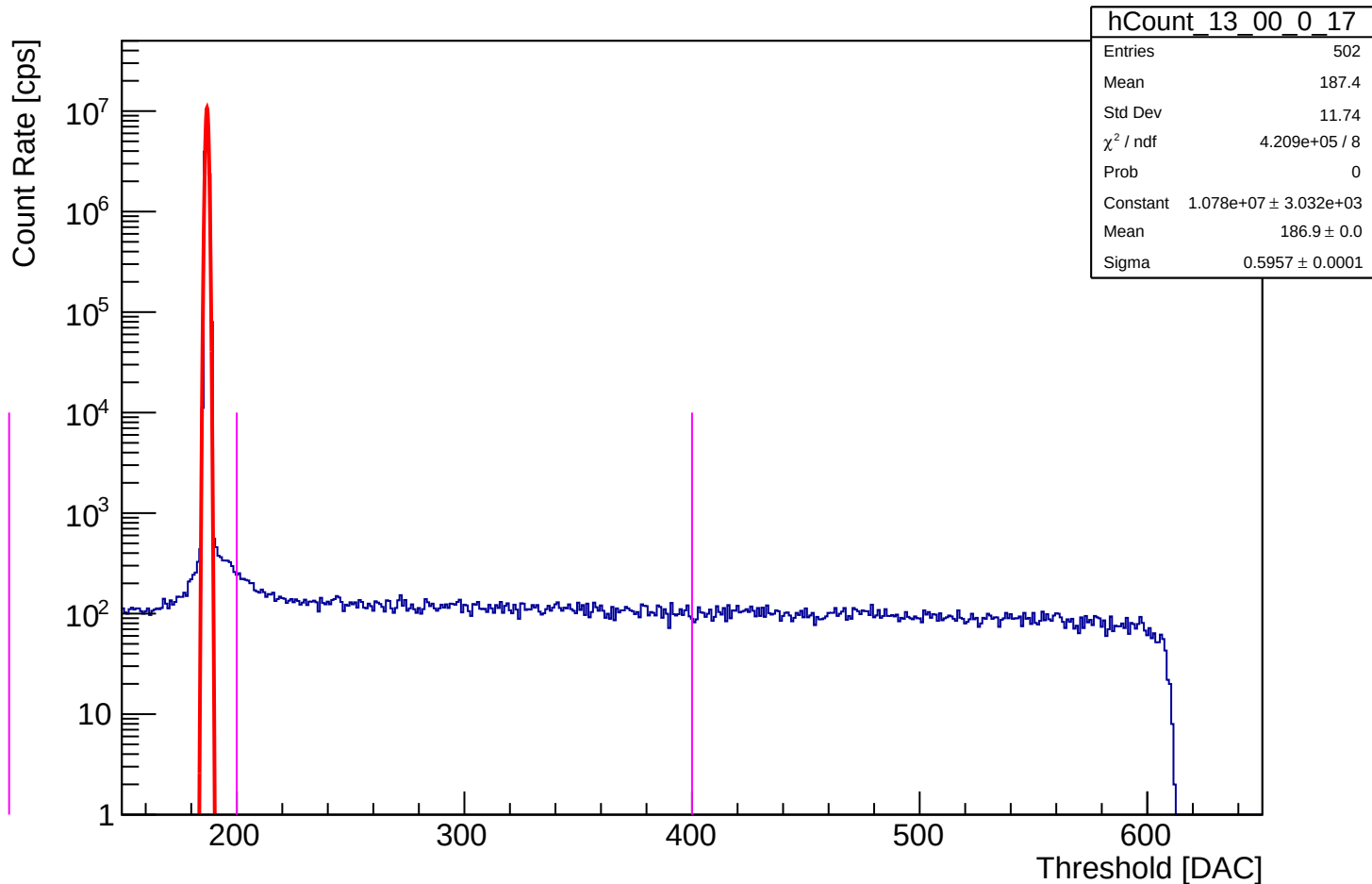
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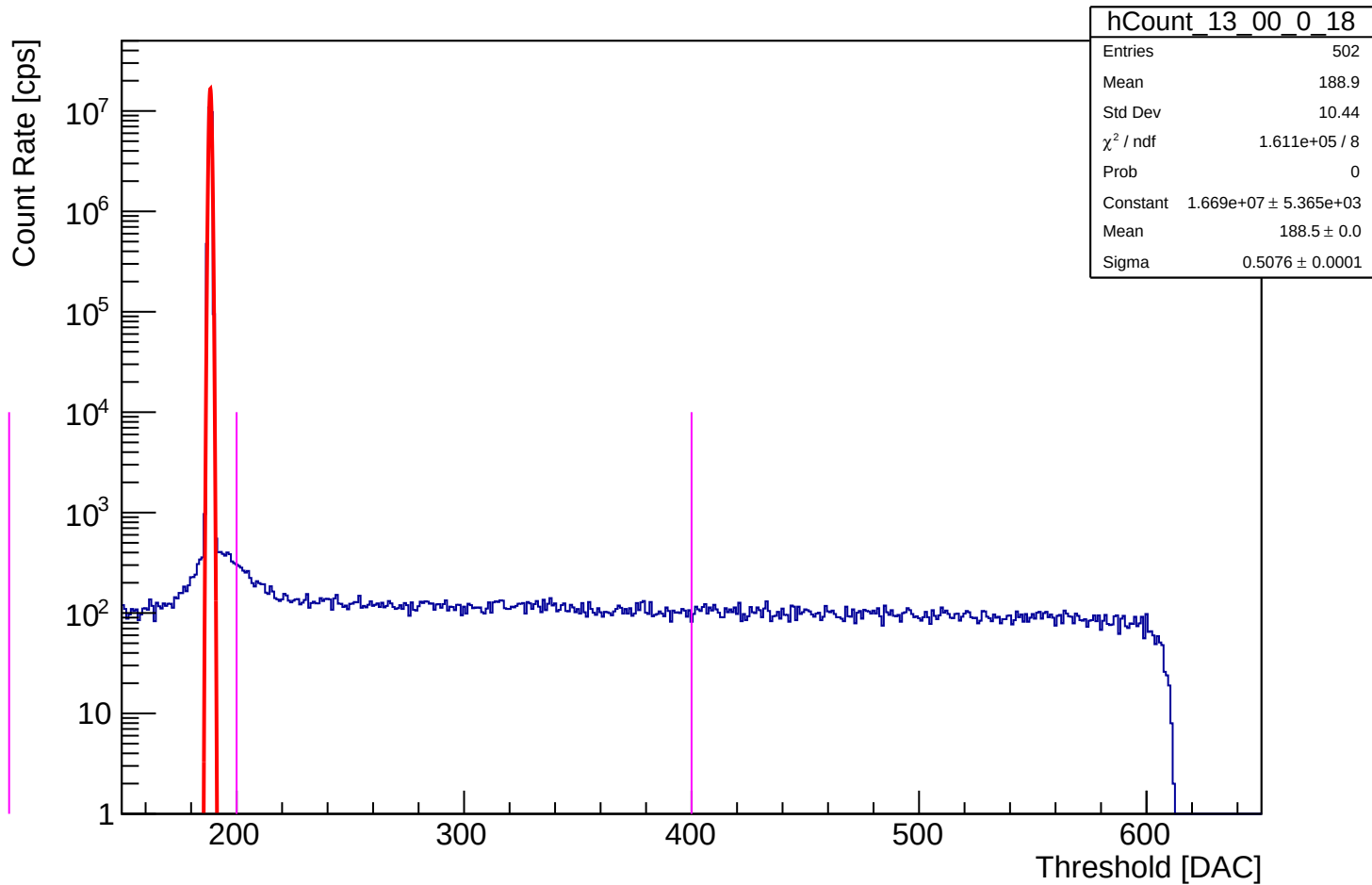
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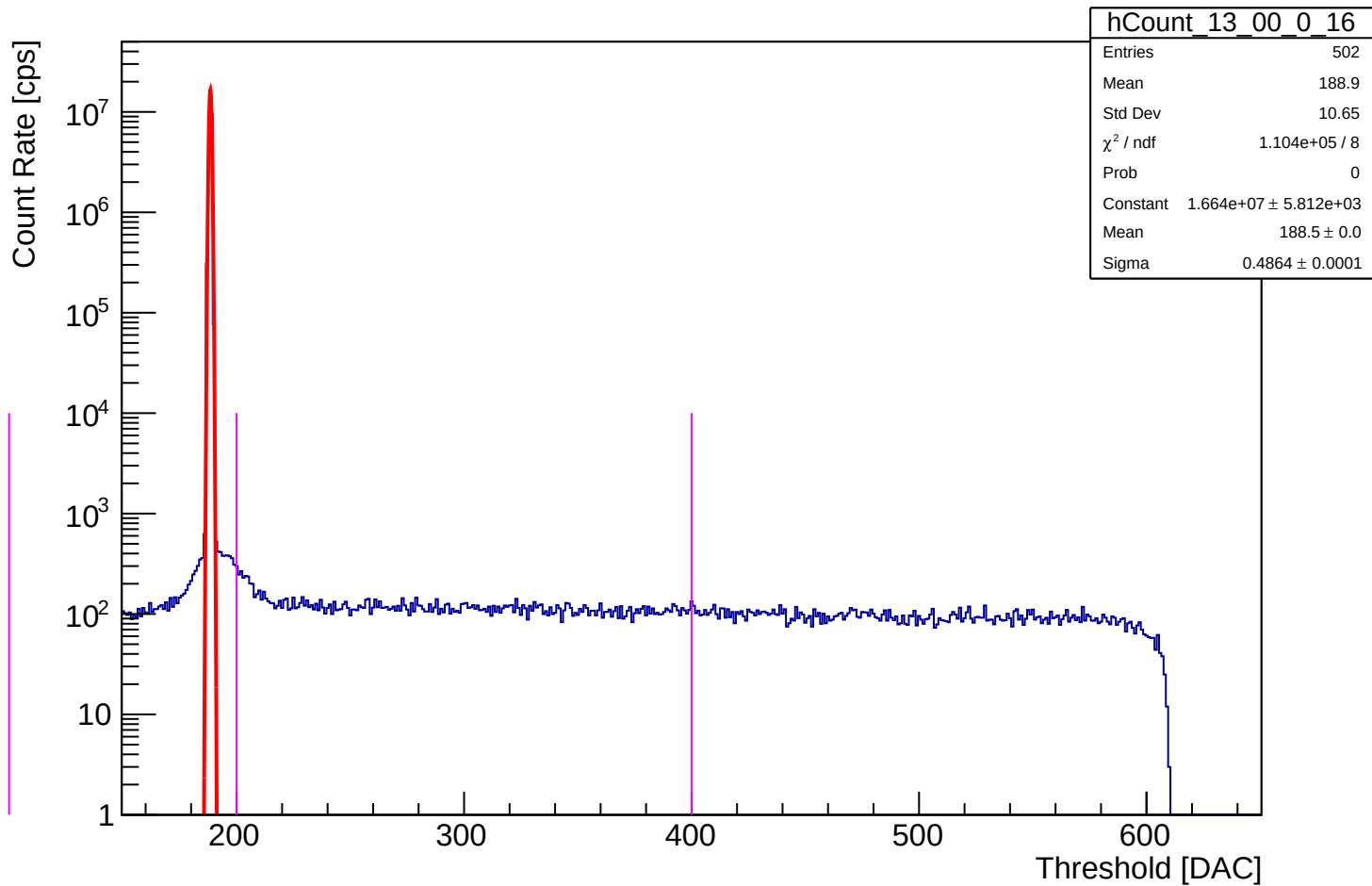
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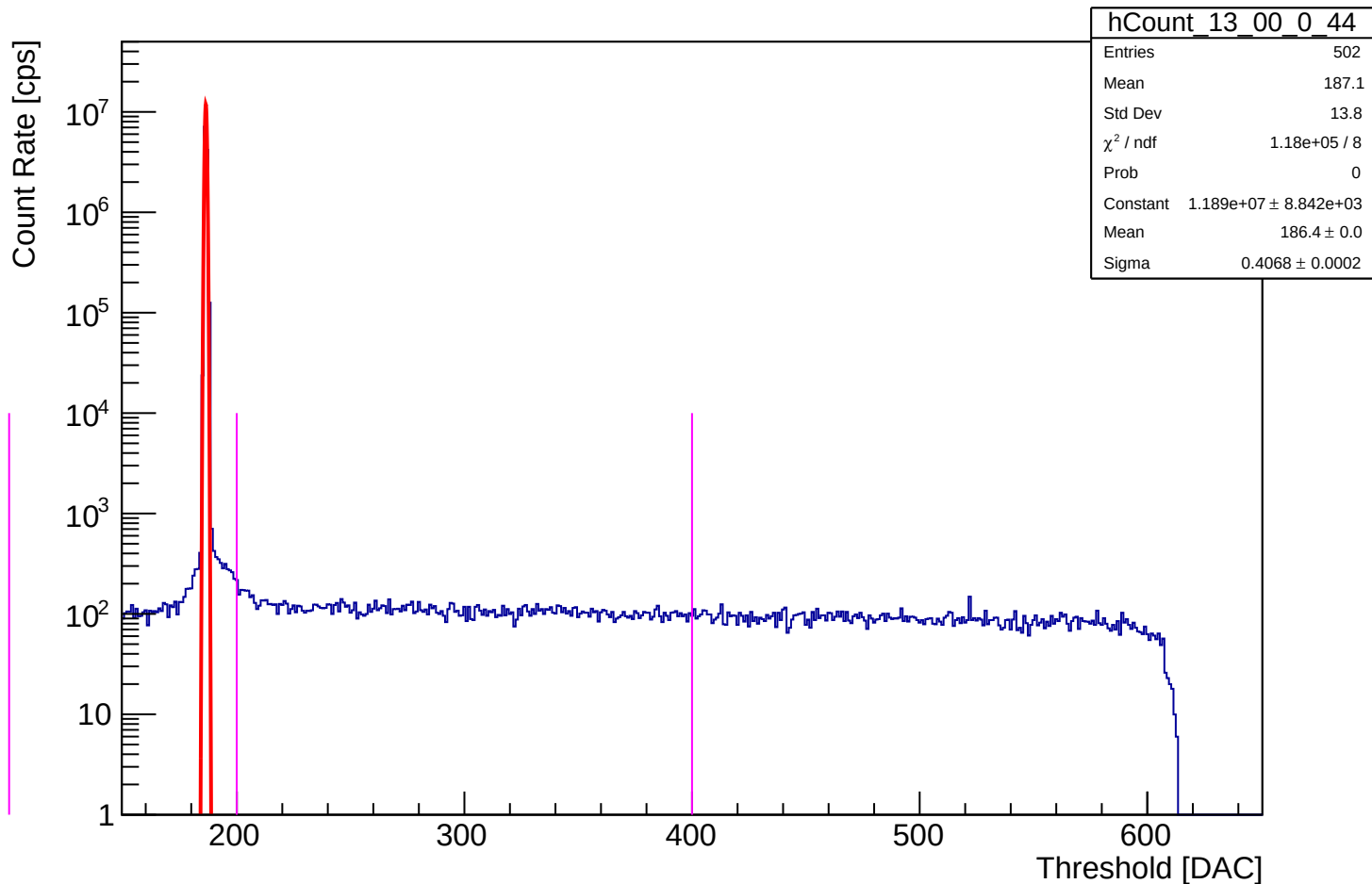
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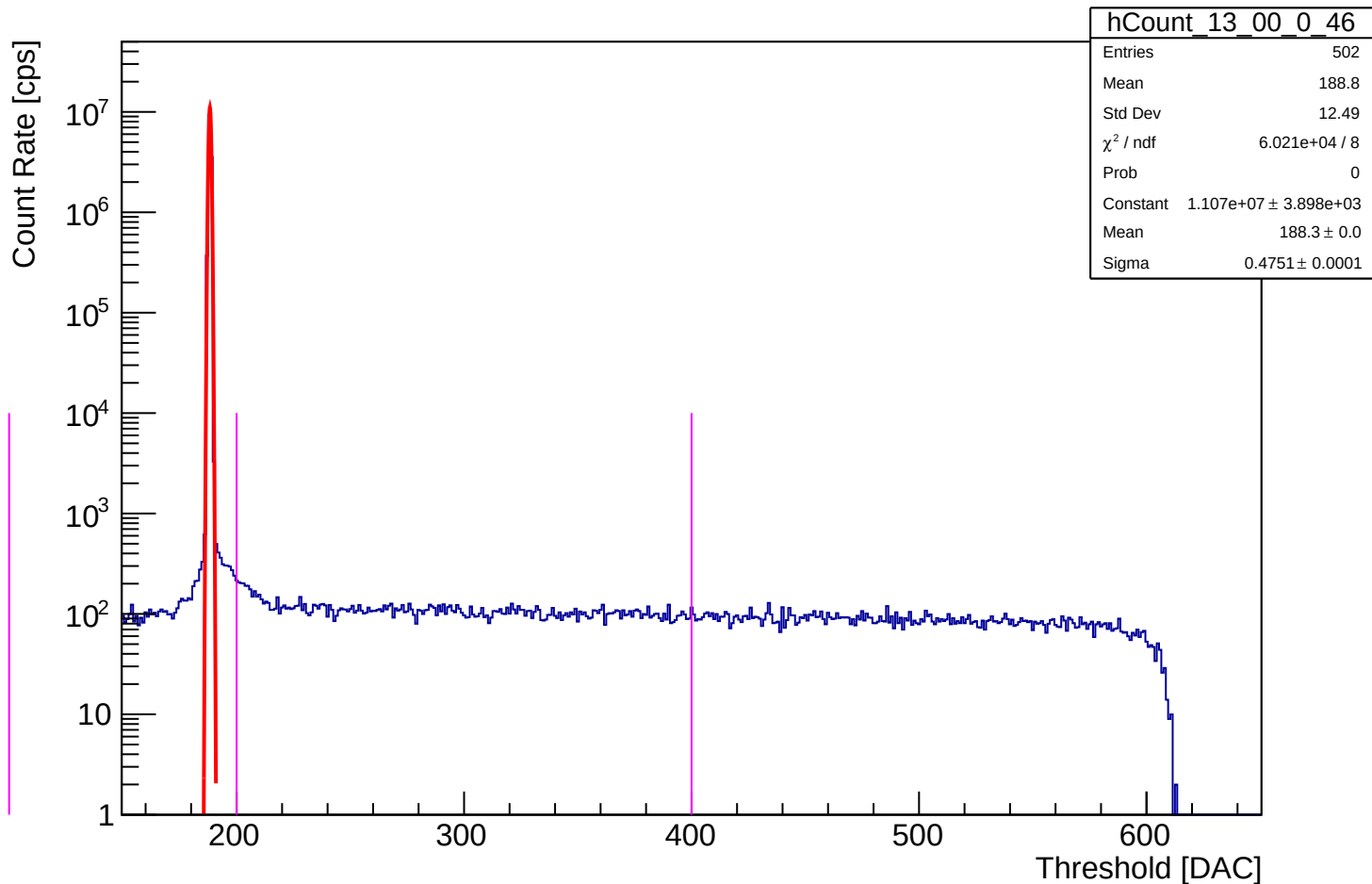
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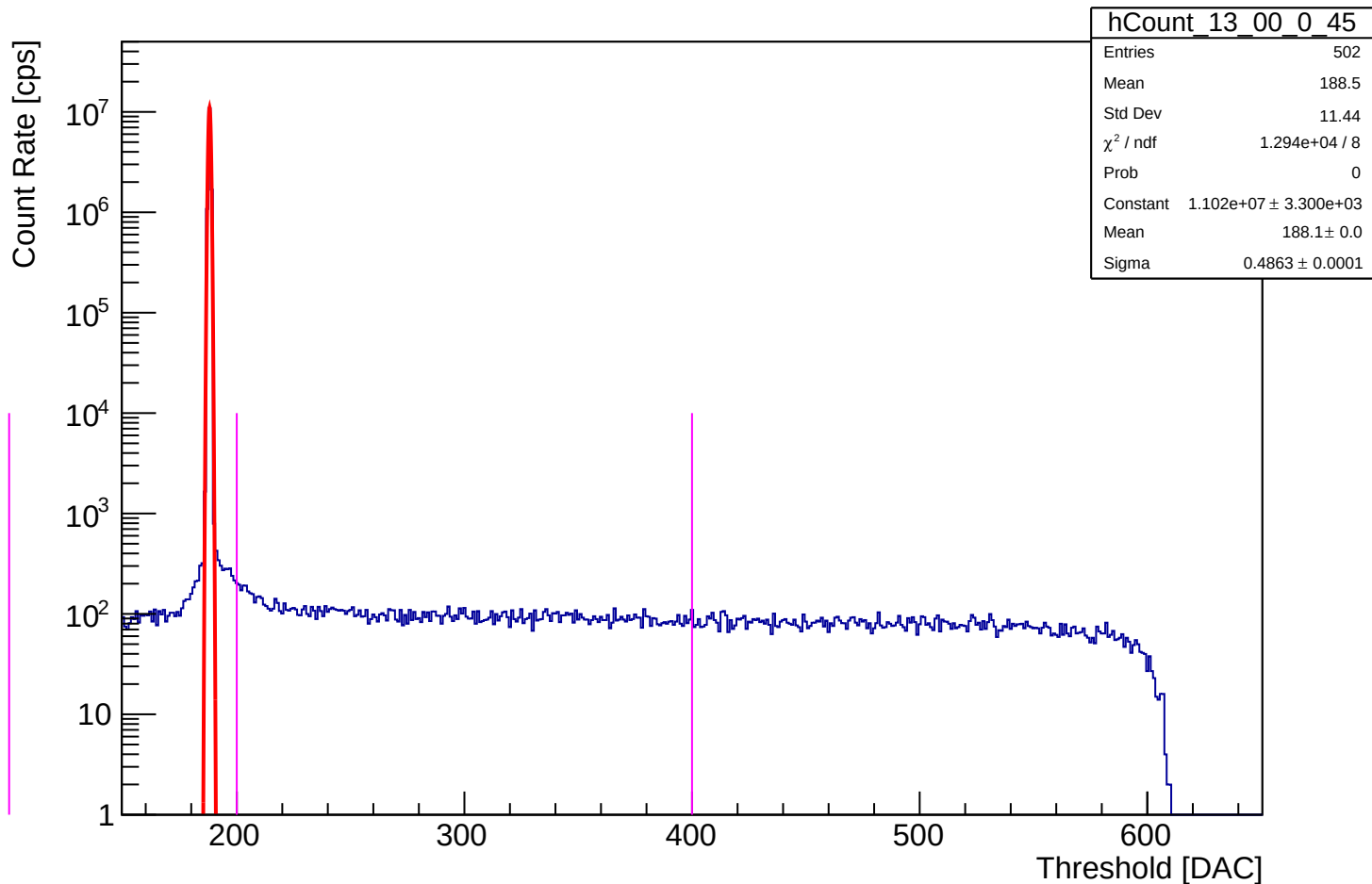
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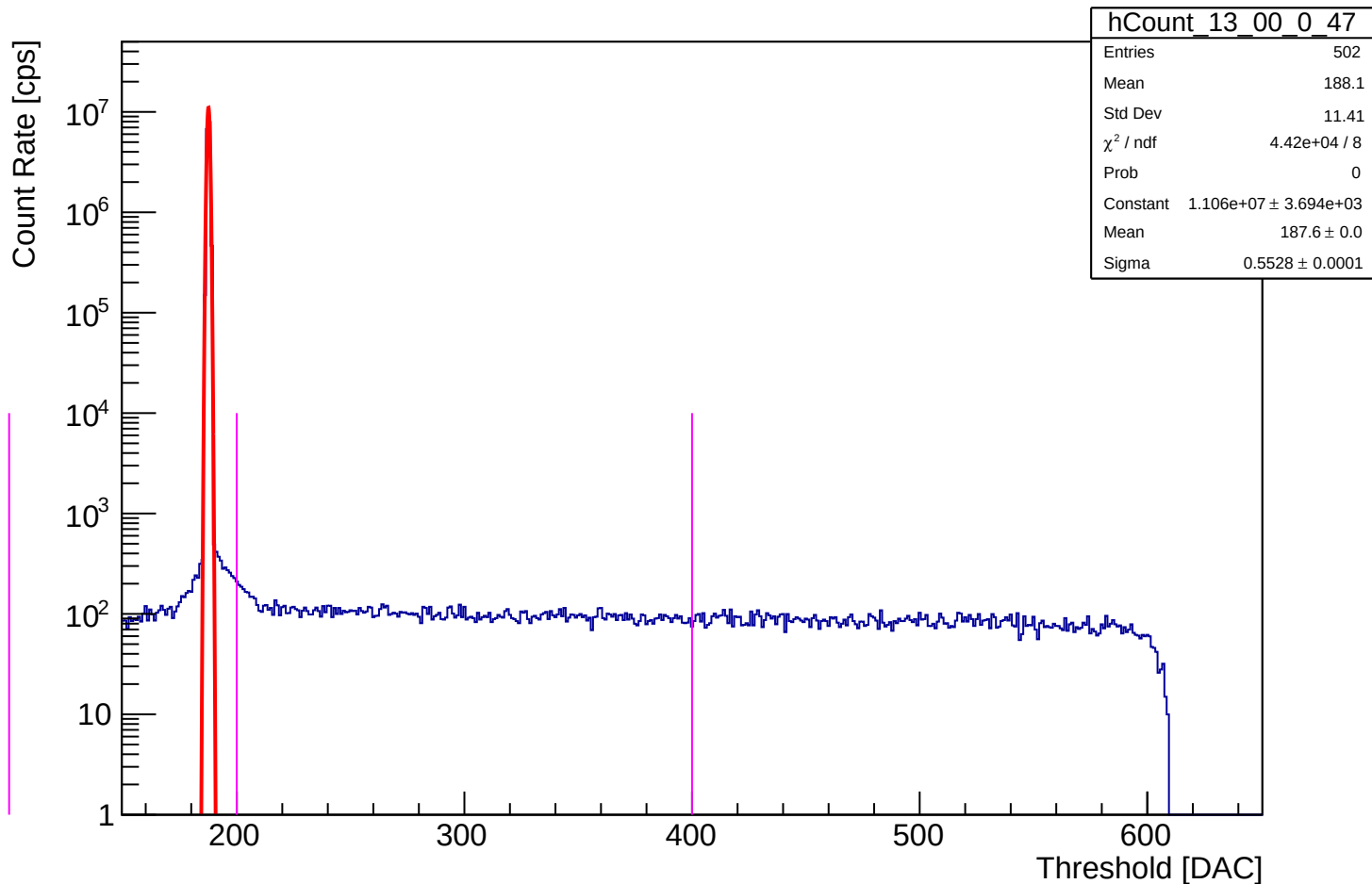
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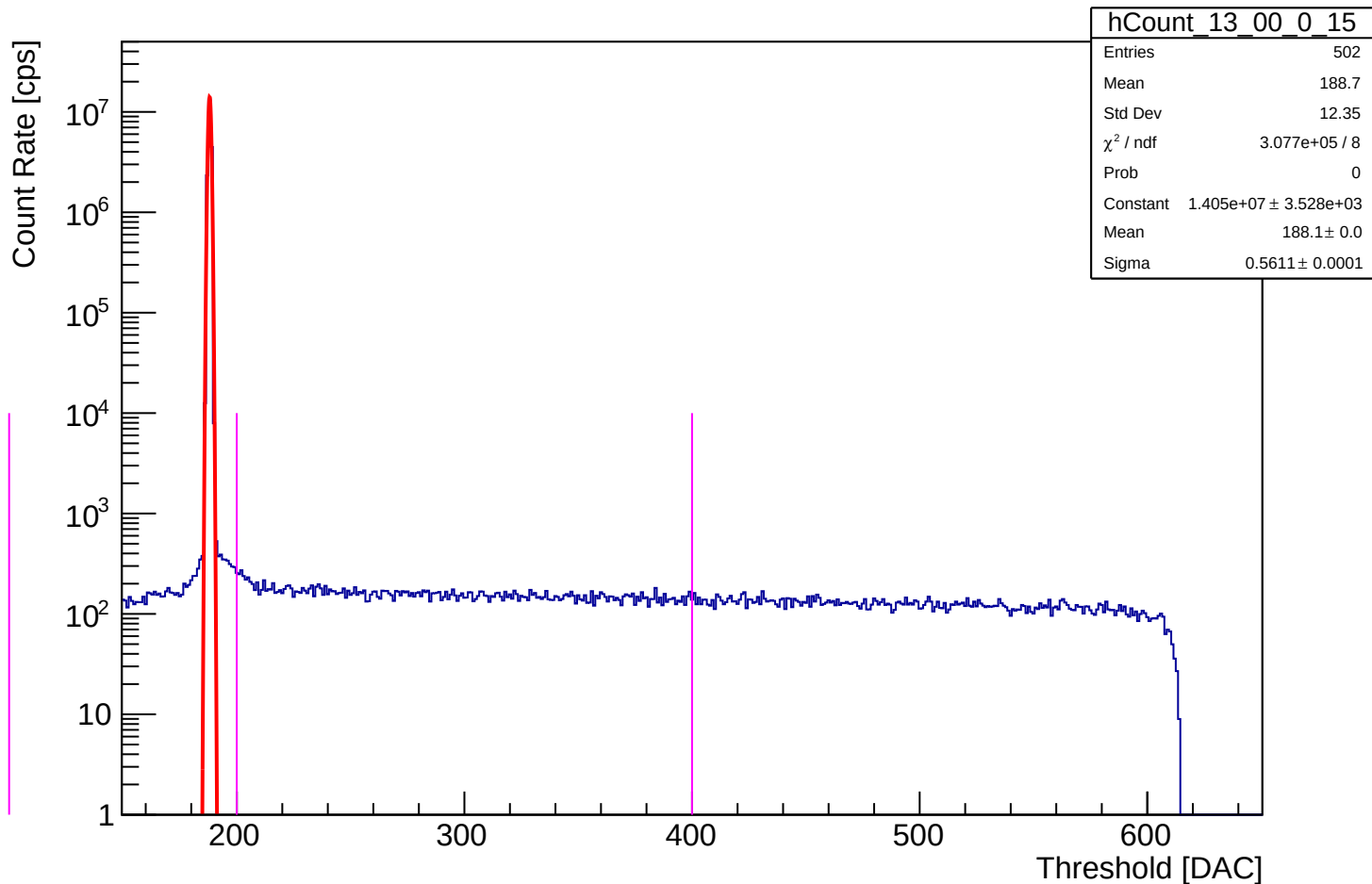
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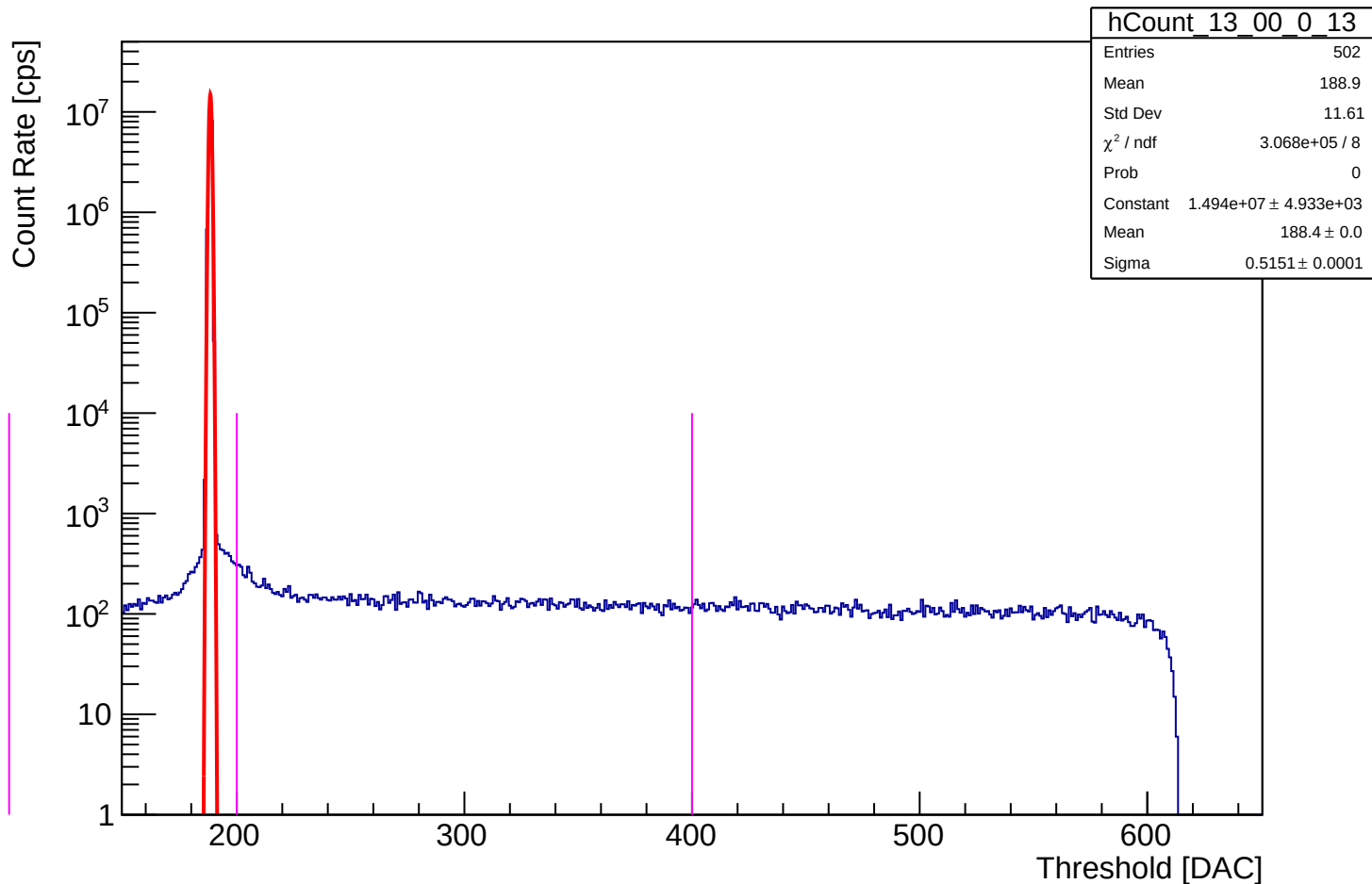
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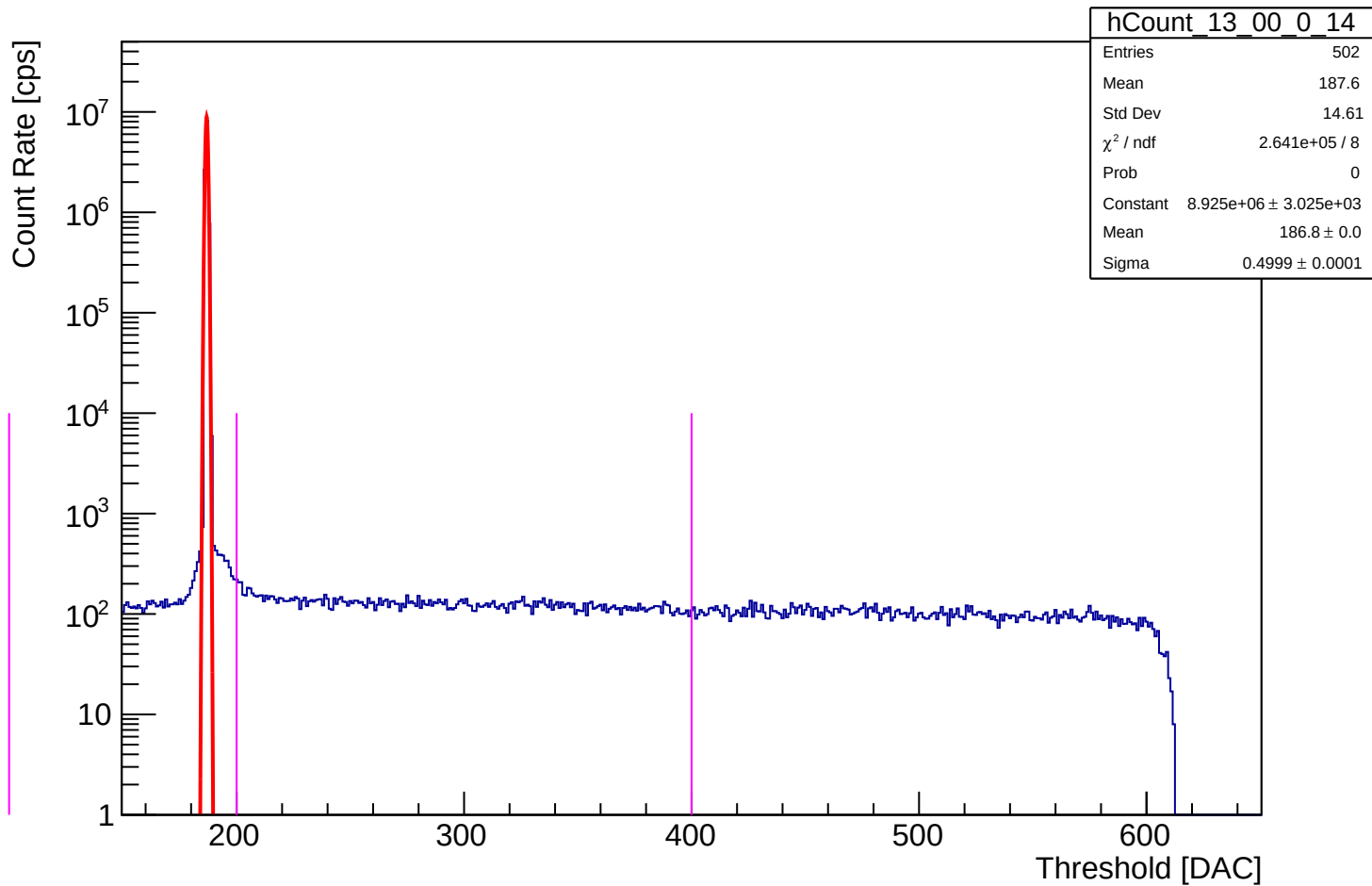
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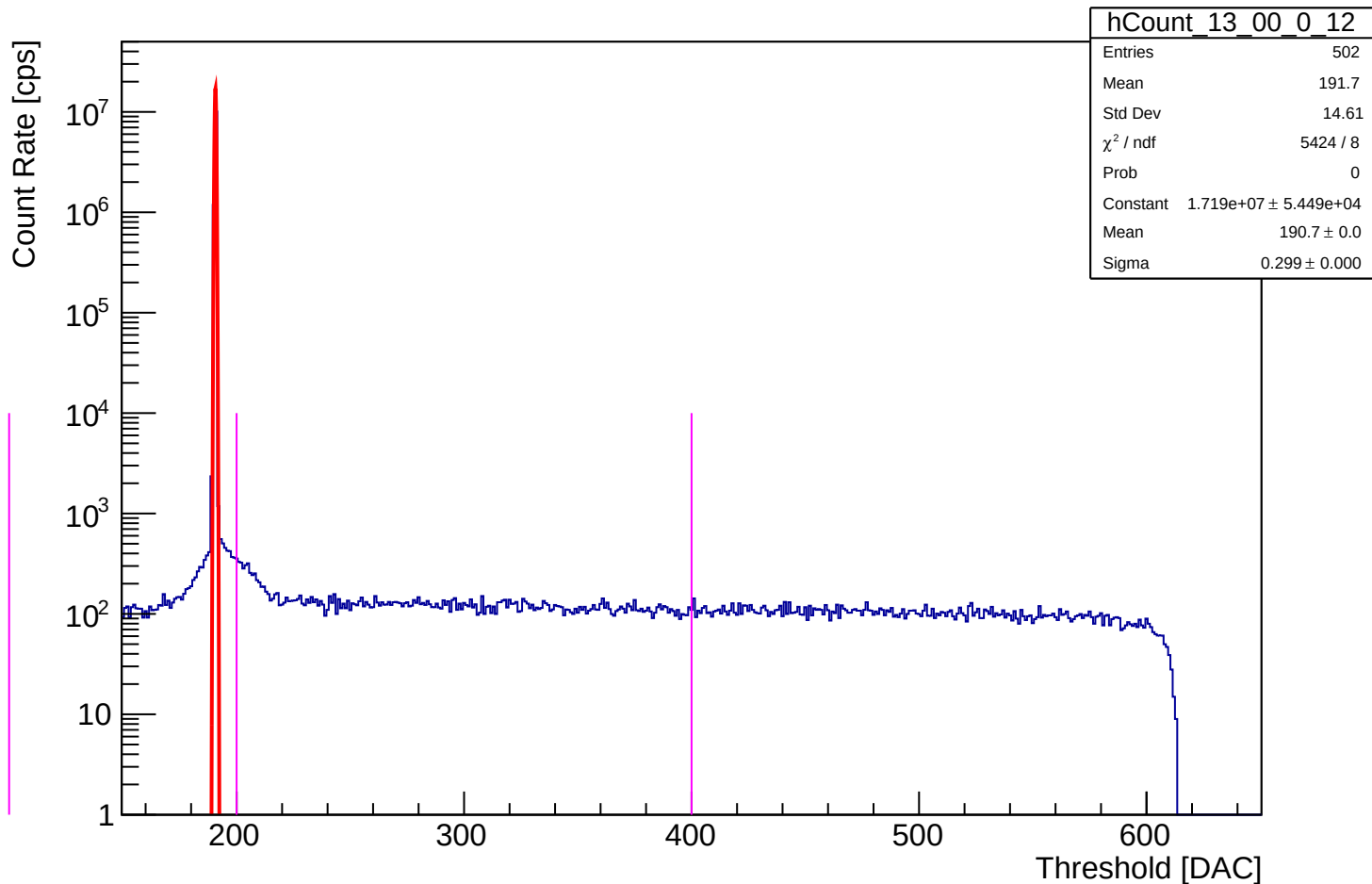
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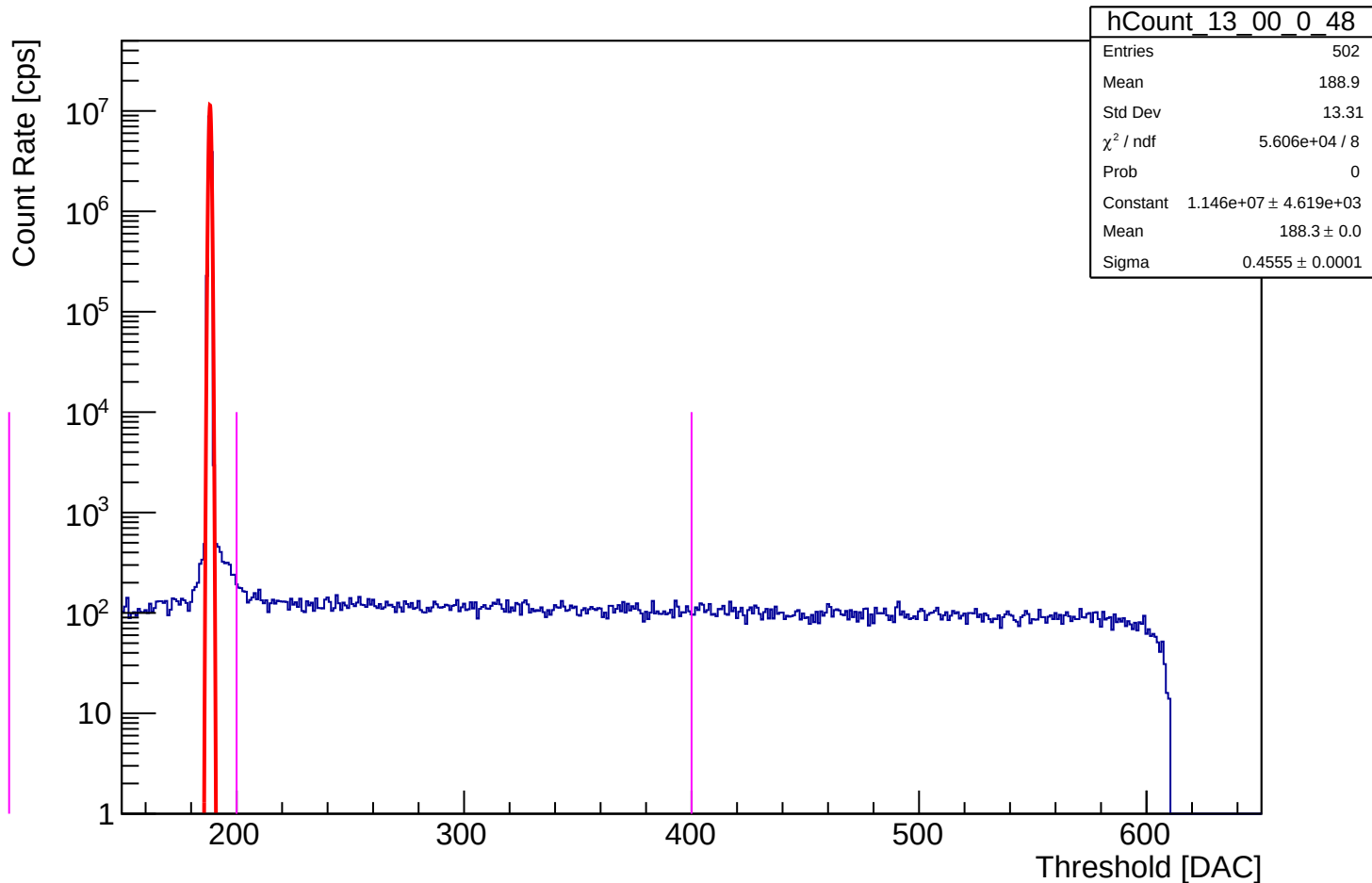
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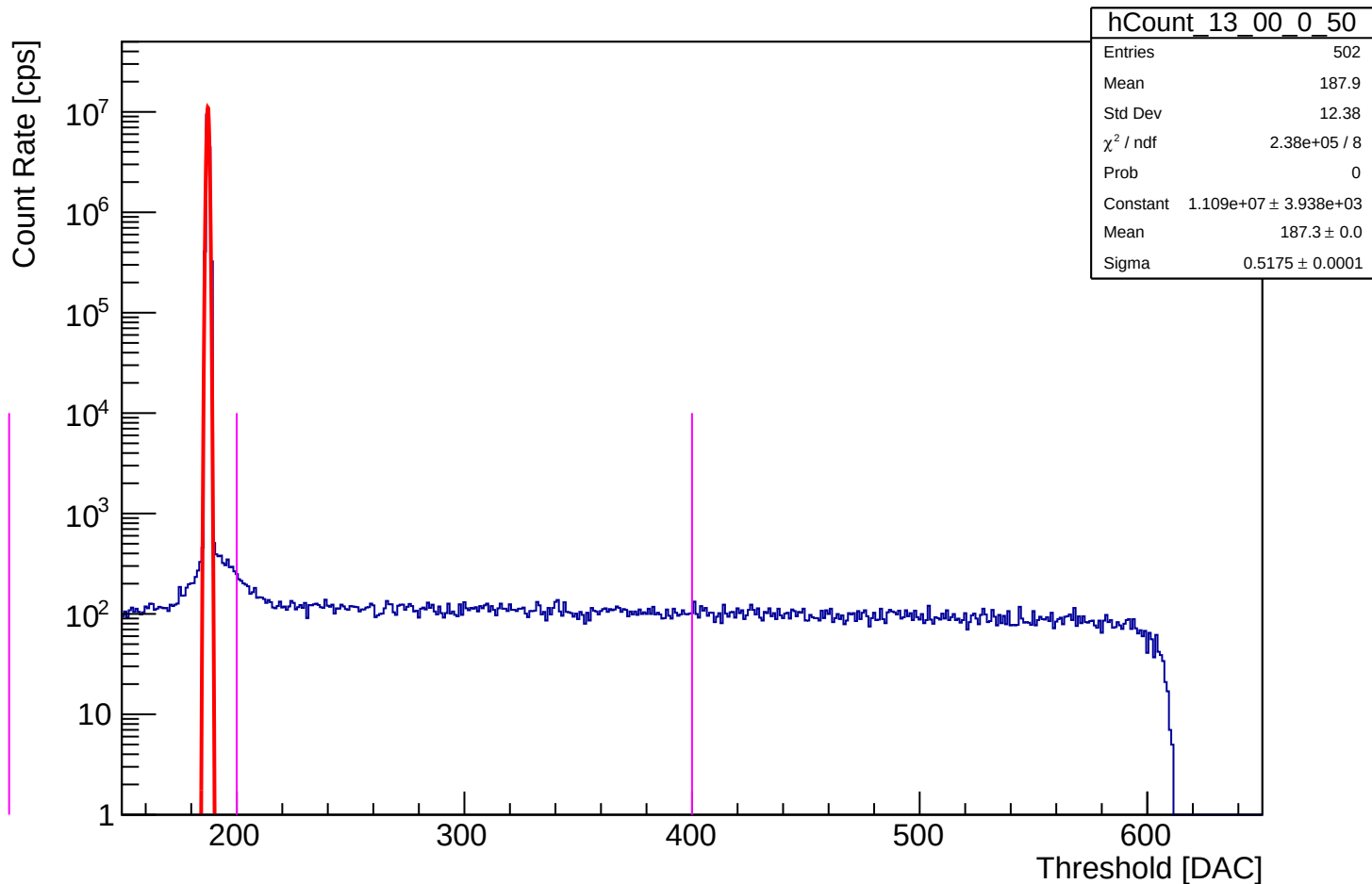
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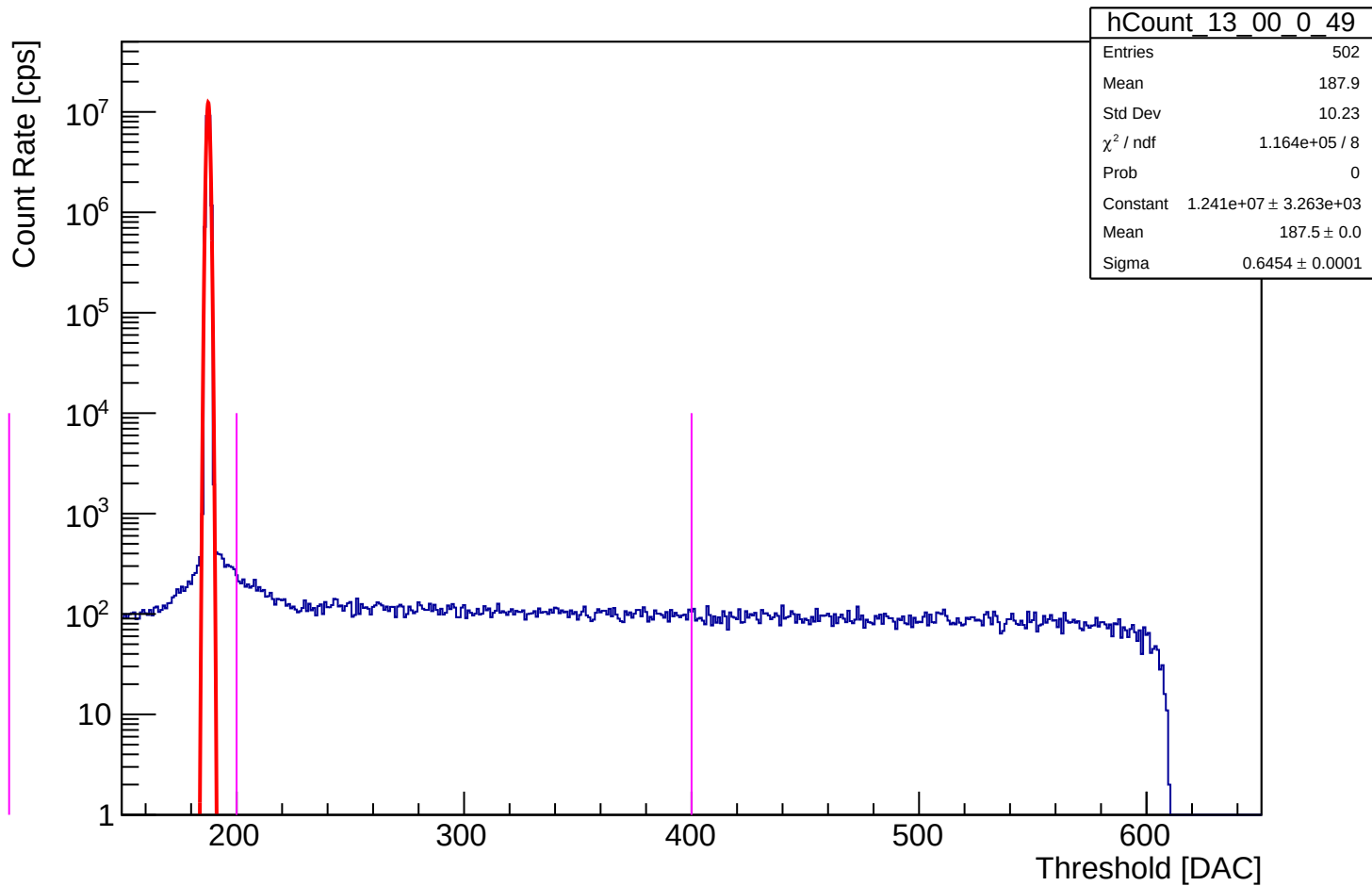
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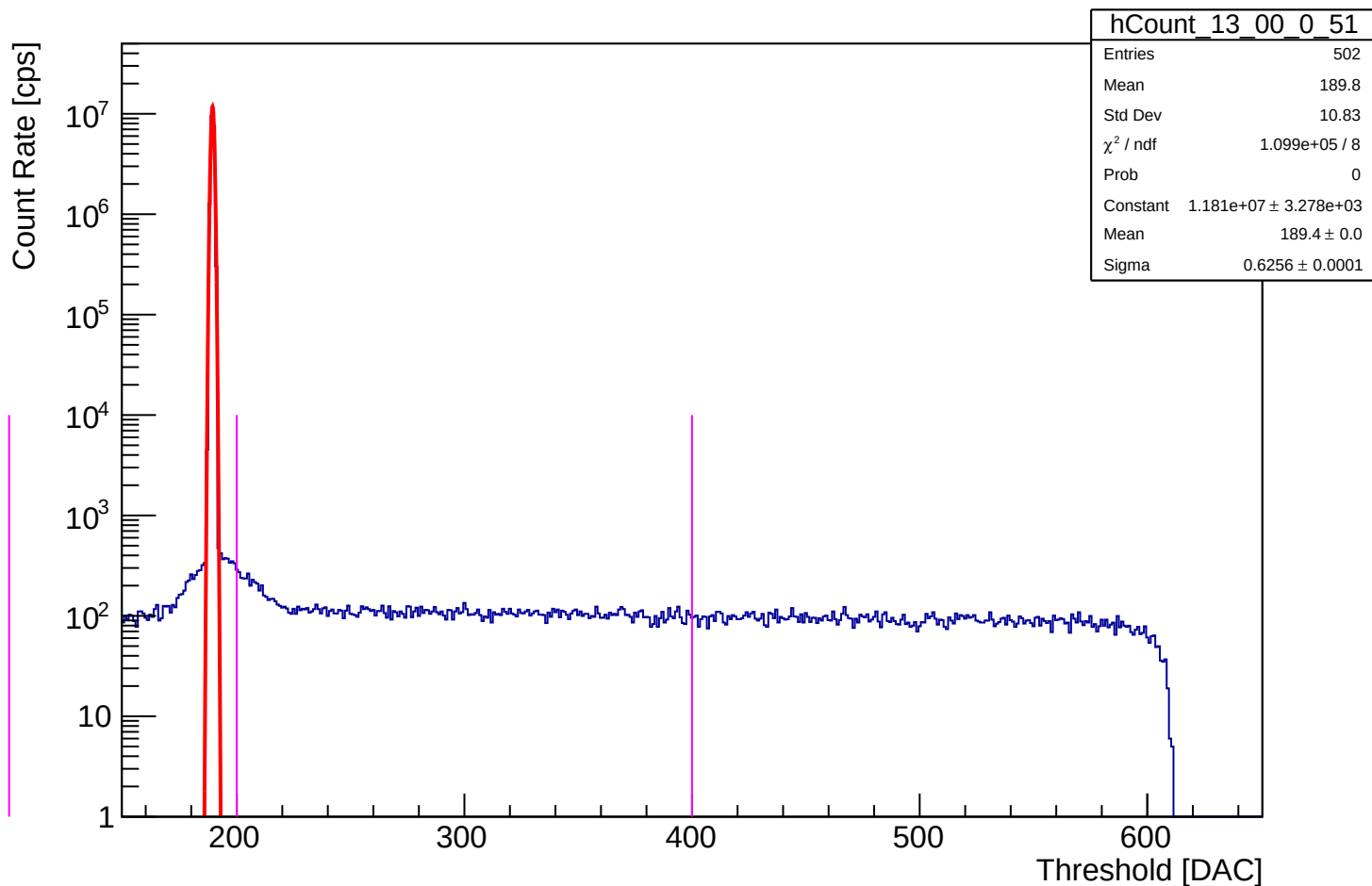
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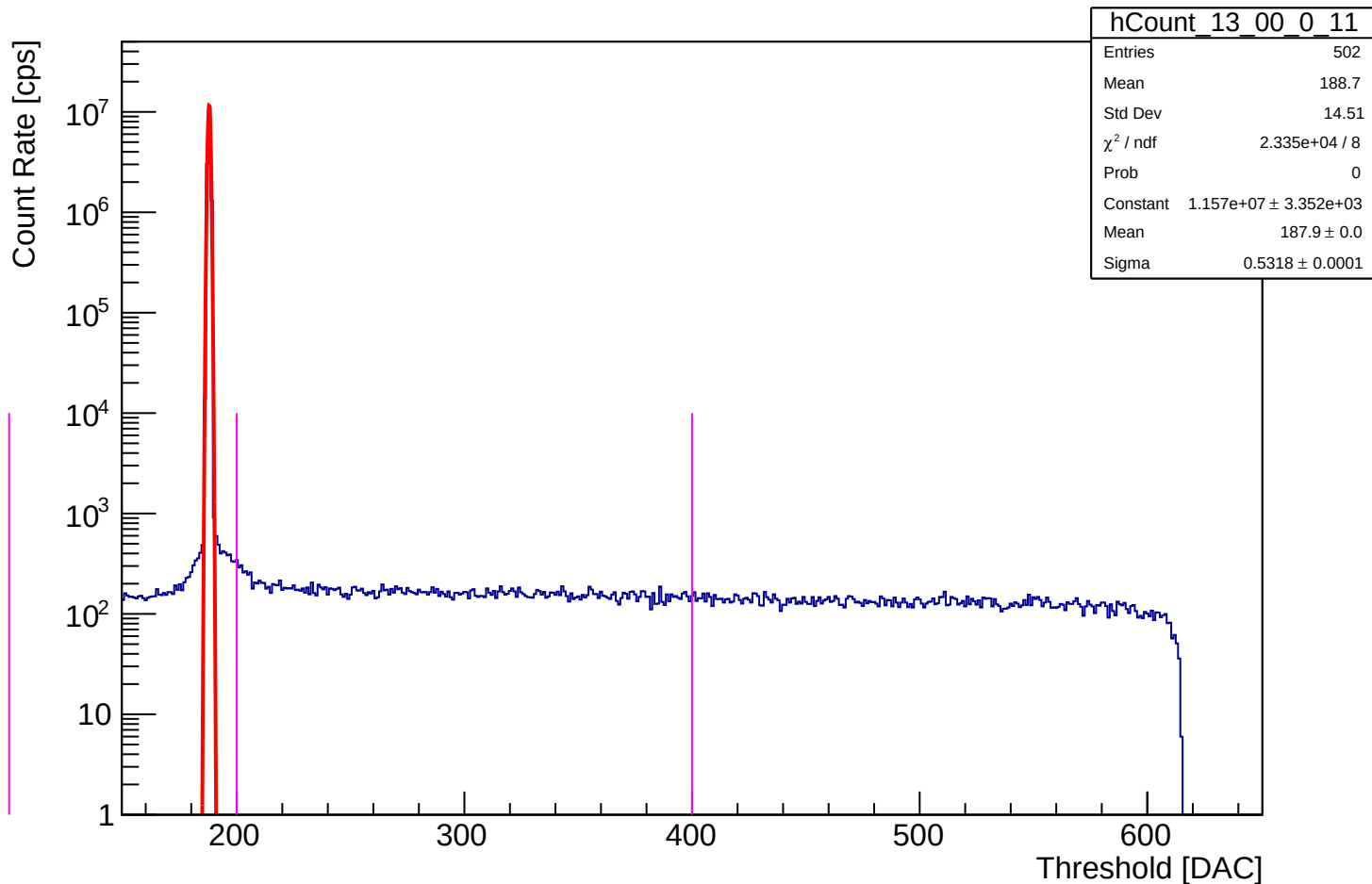
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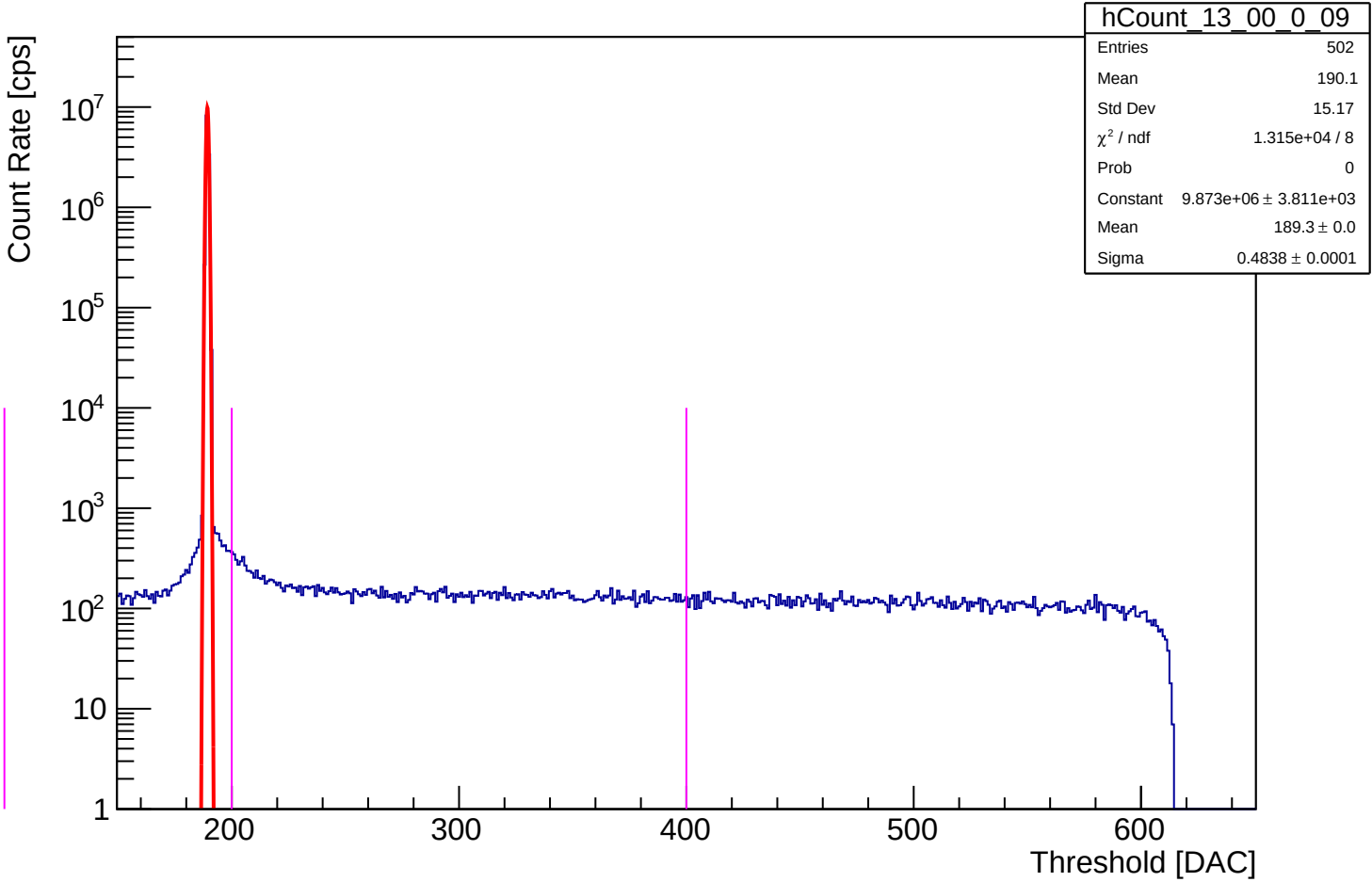


Row 1 Tile 1 Pmt 1 Pixel 40 Slot 13 Fiber 0 Asic 0 Channel 51

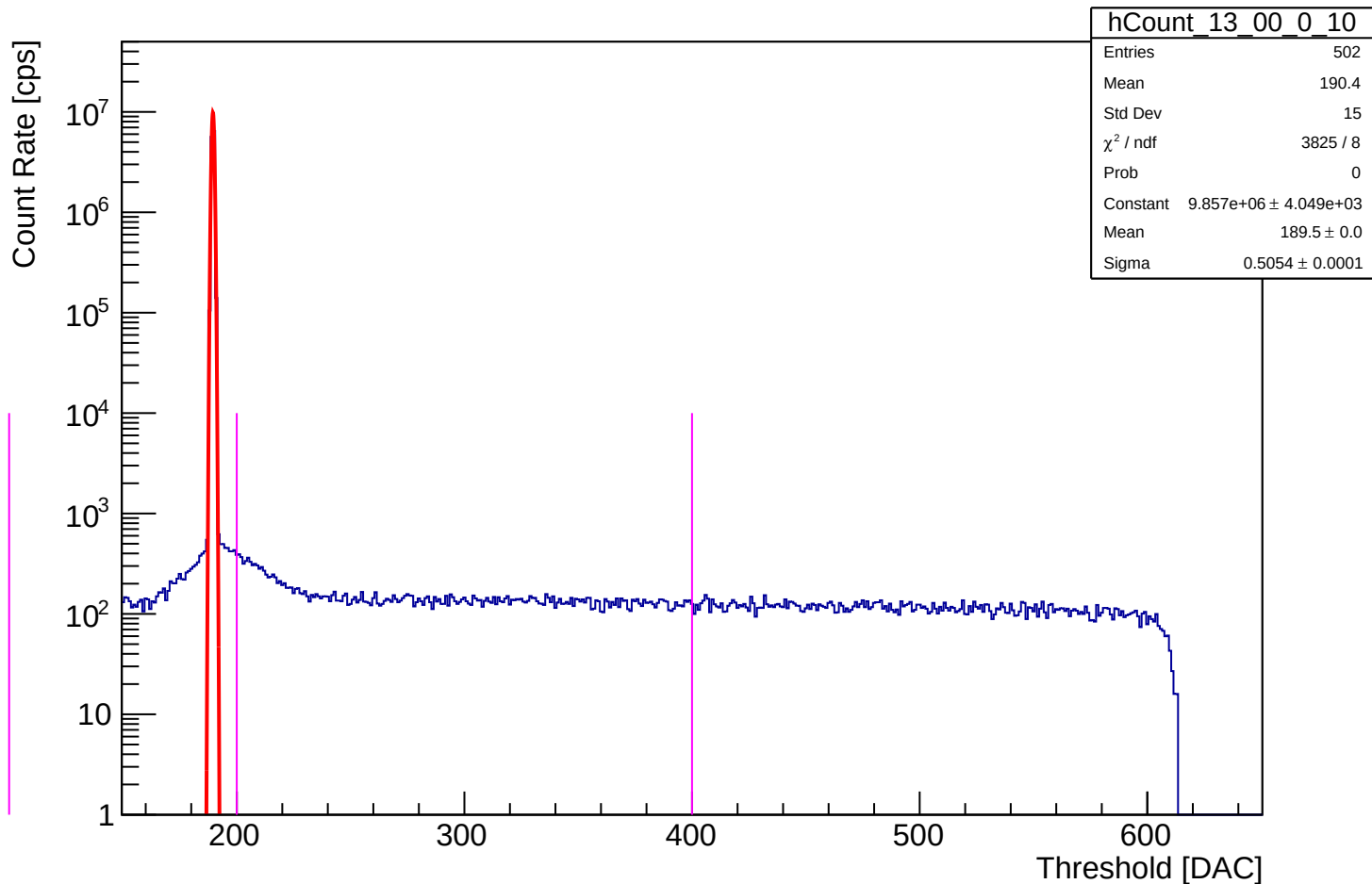


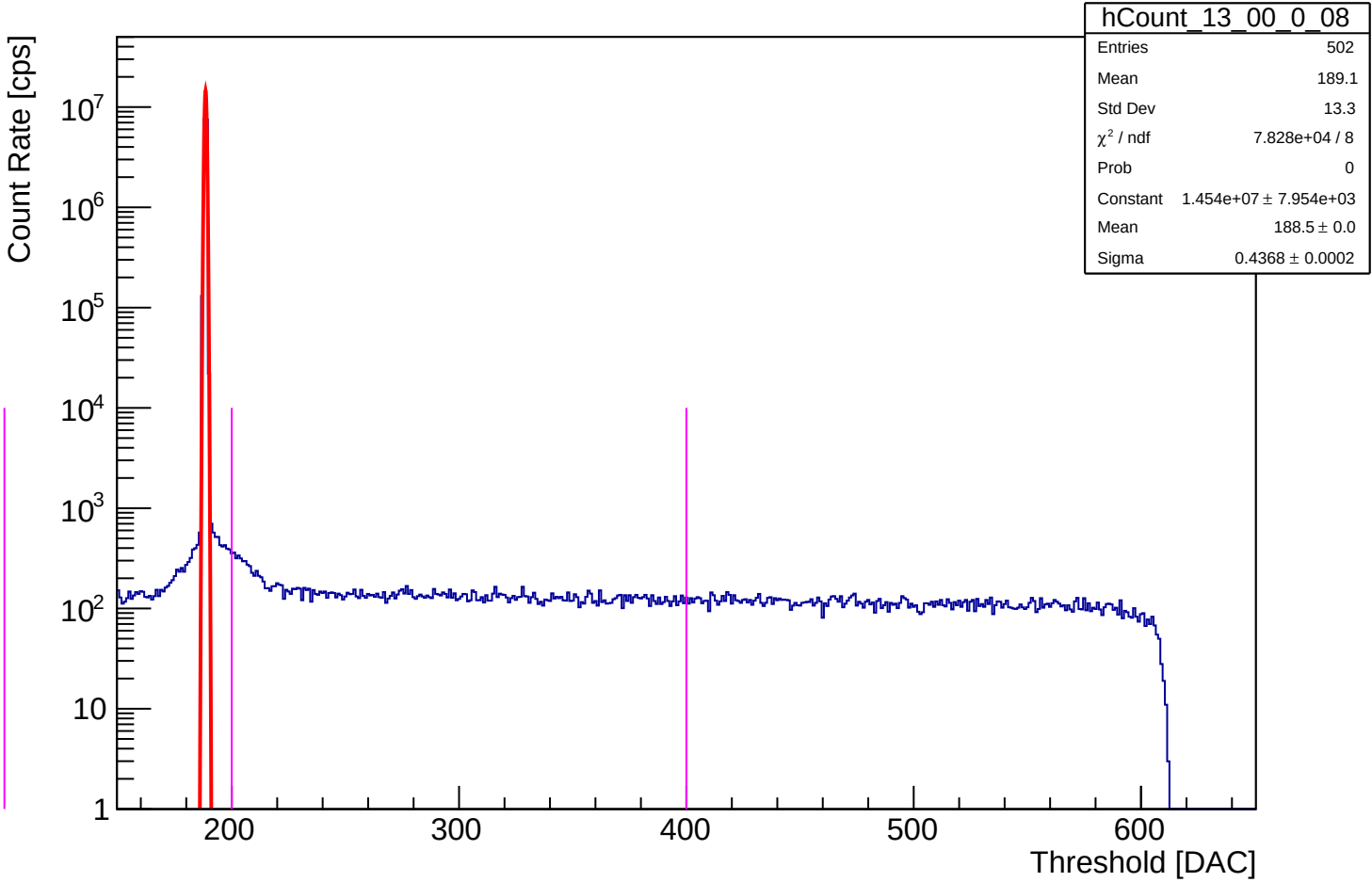
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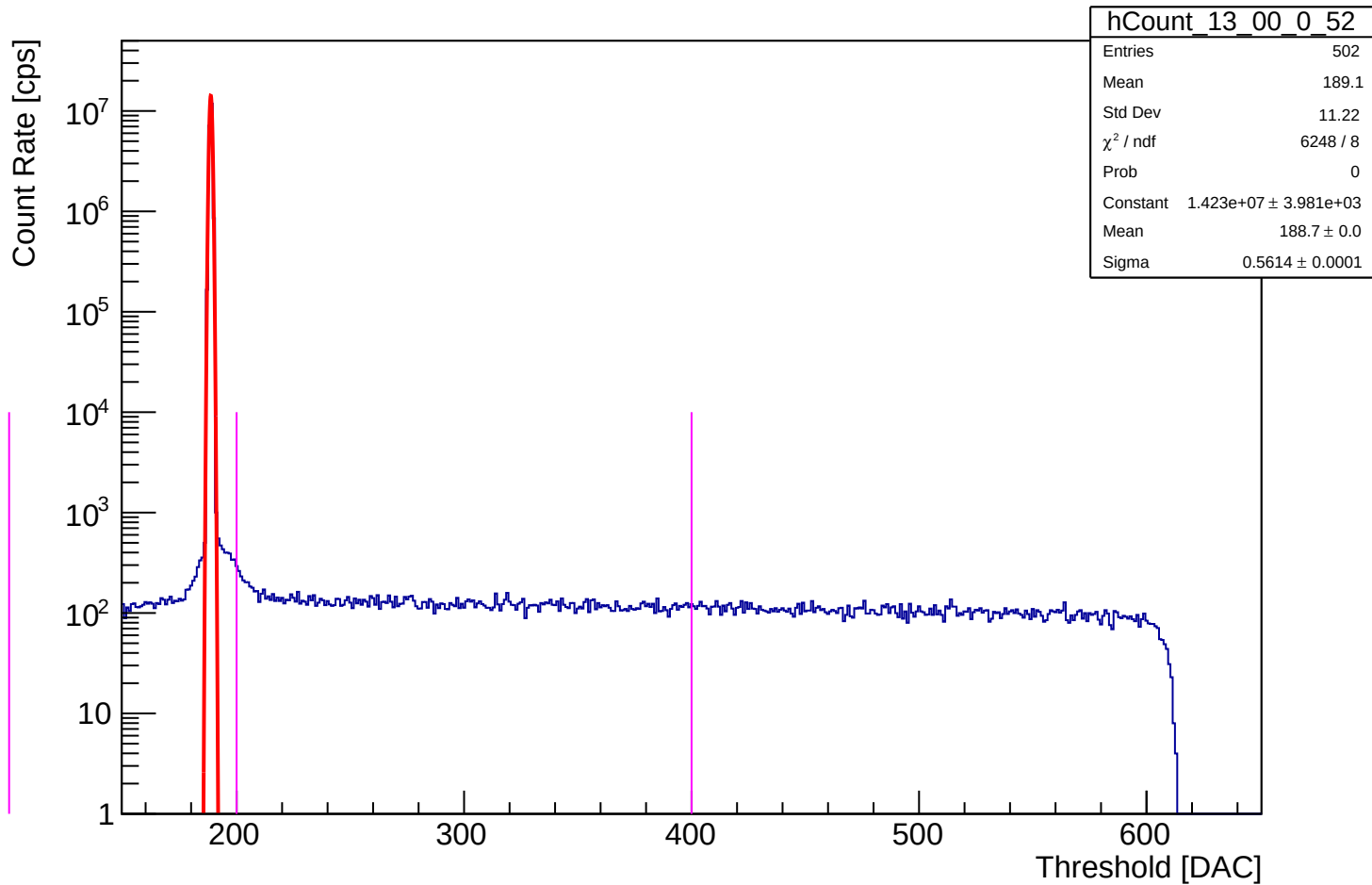


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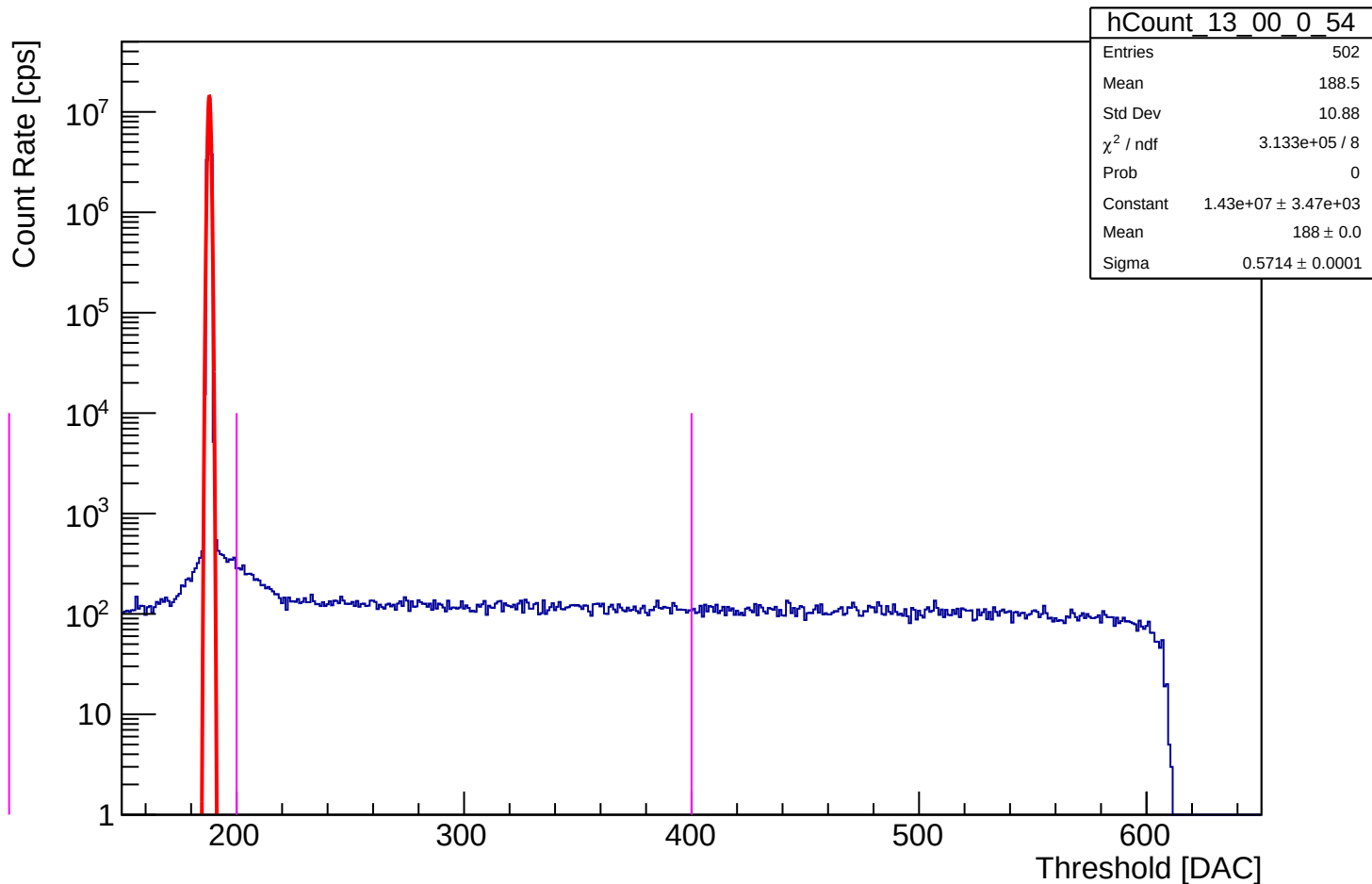




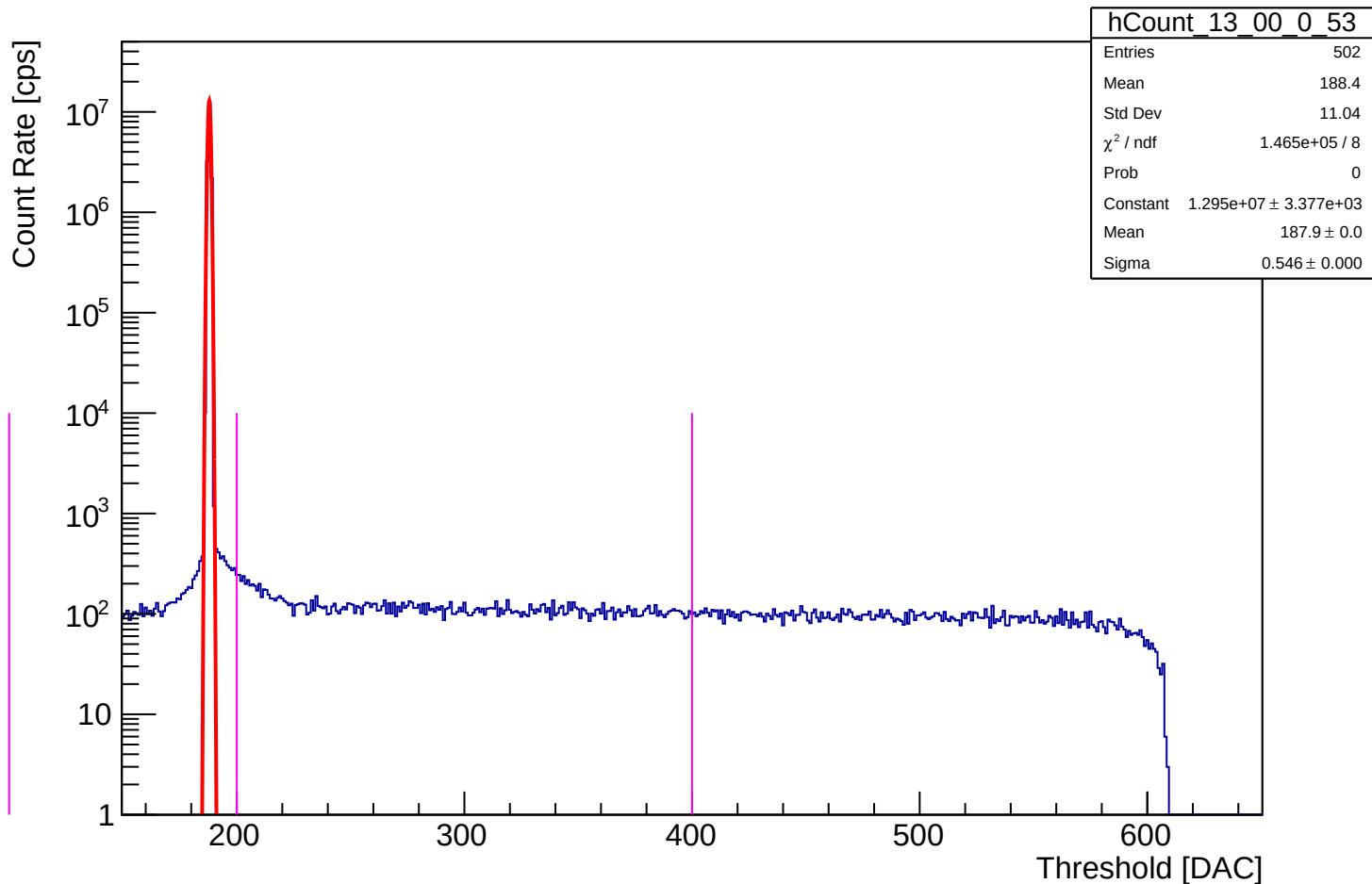
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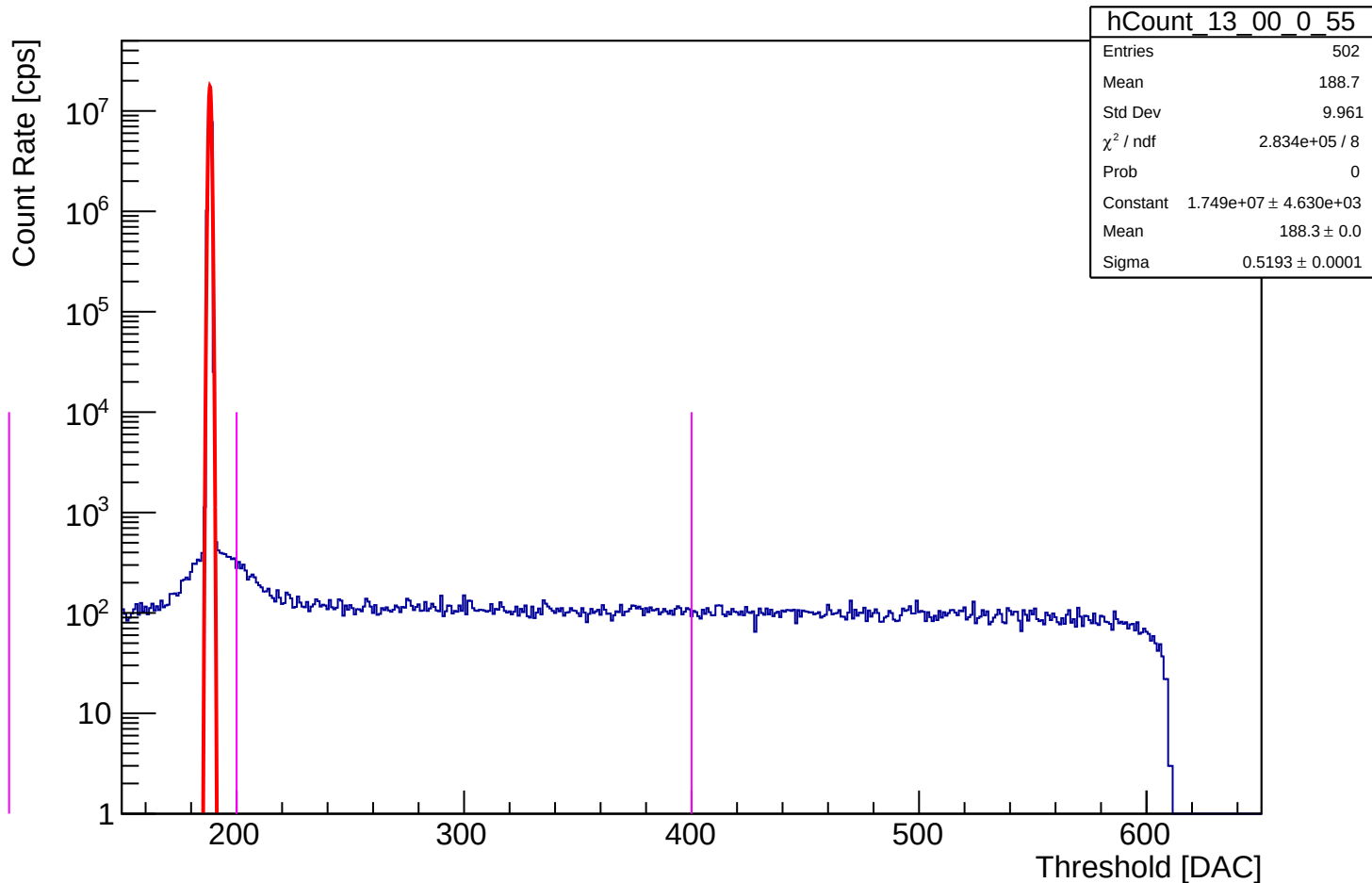
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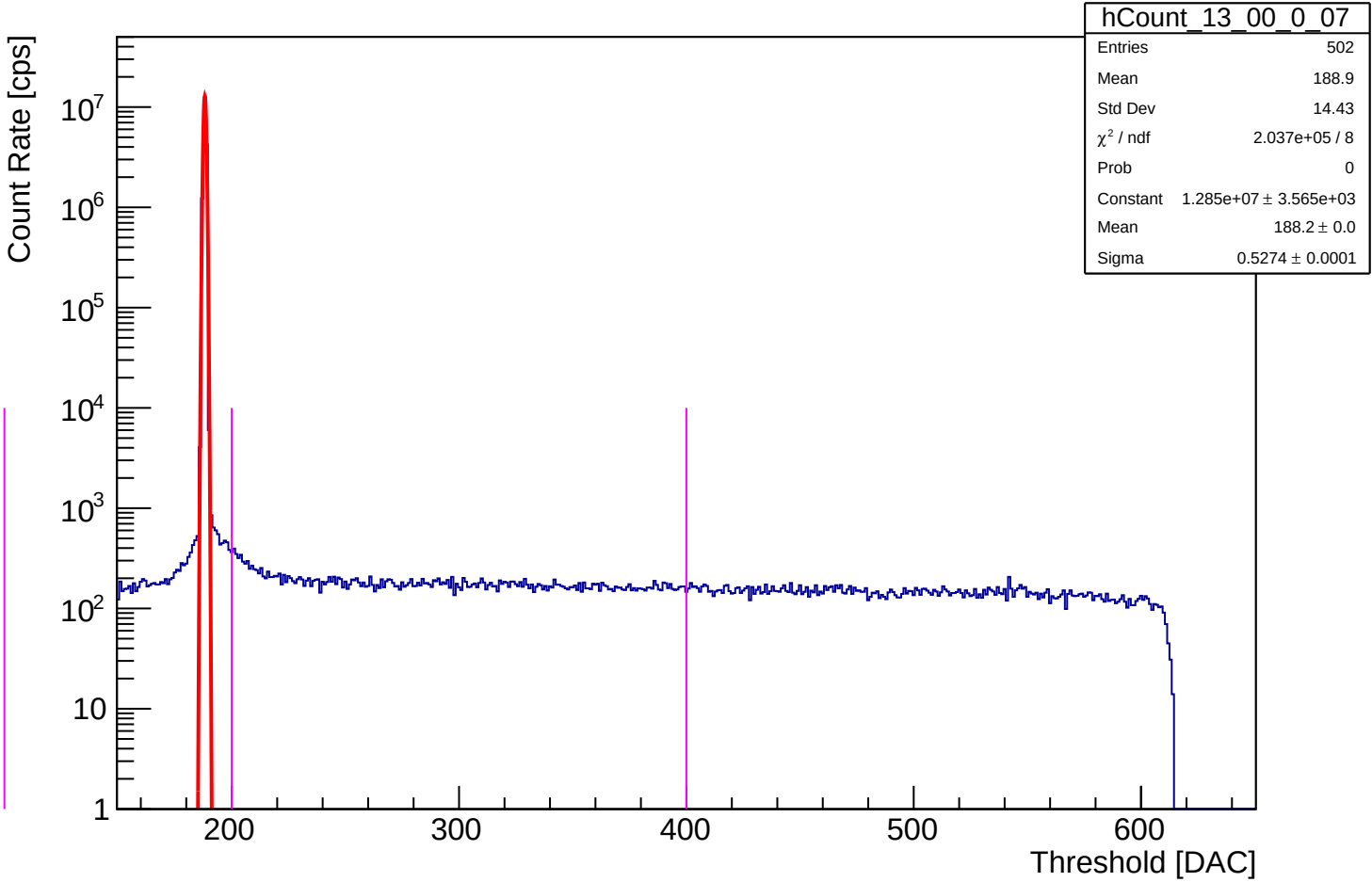


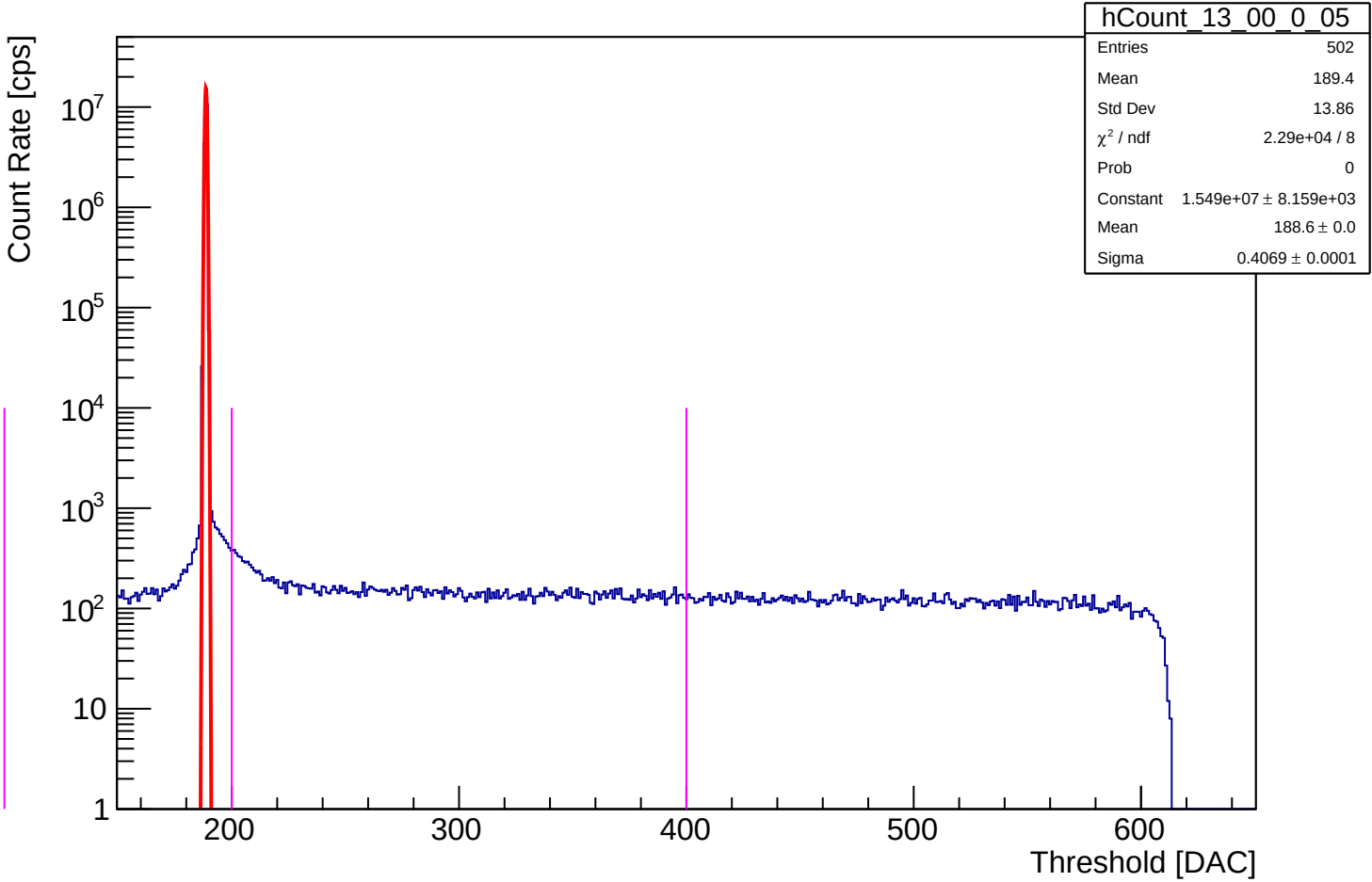
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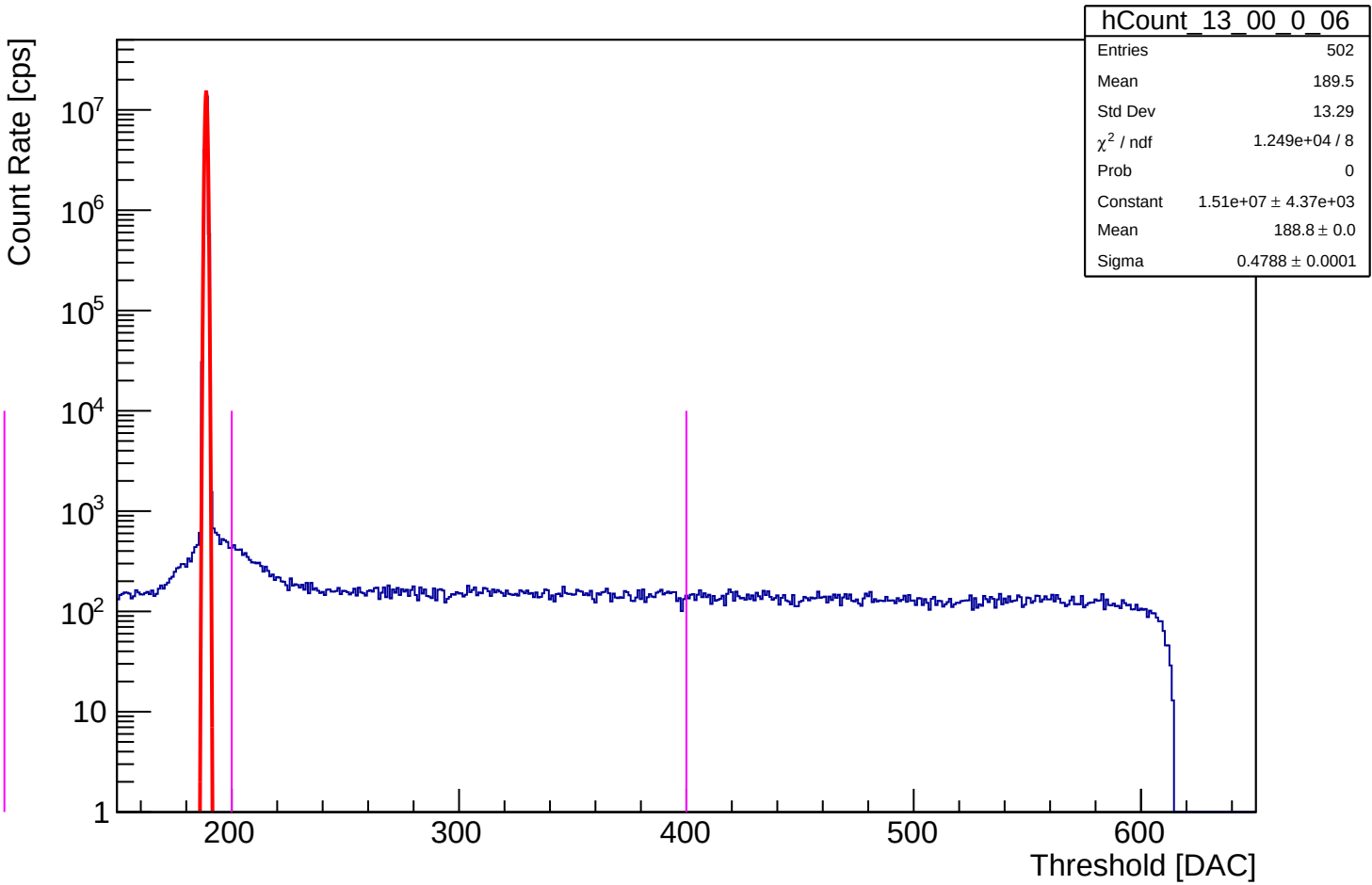


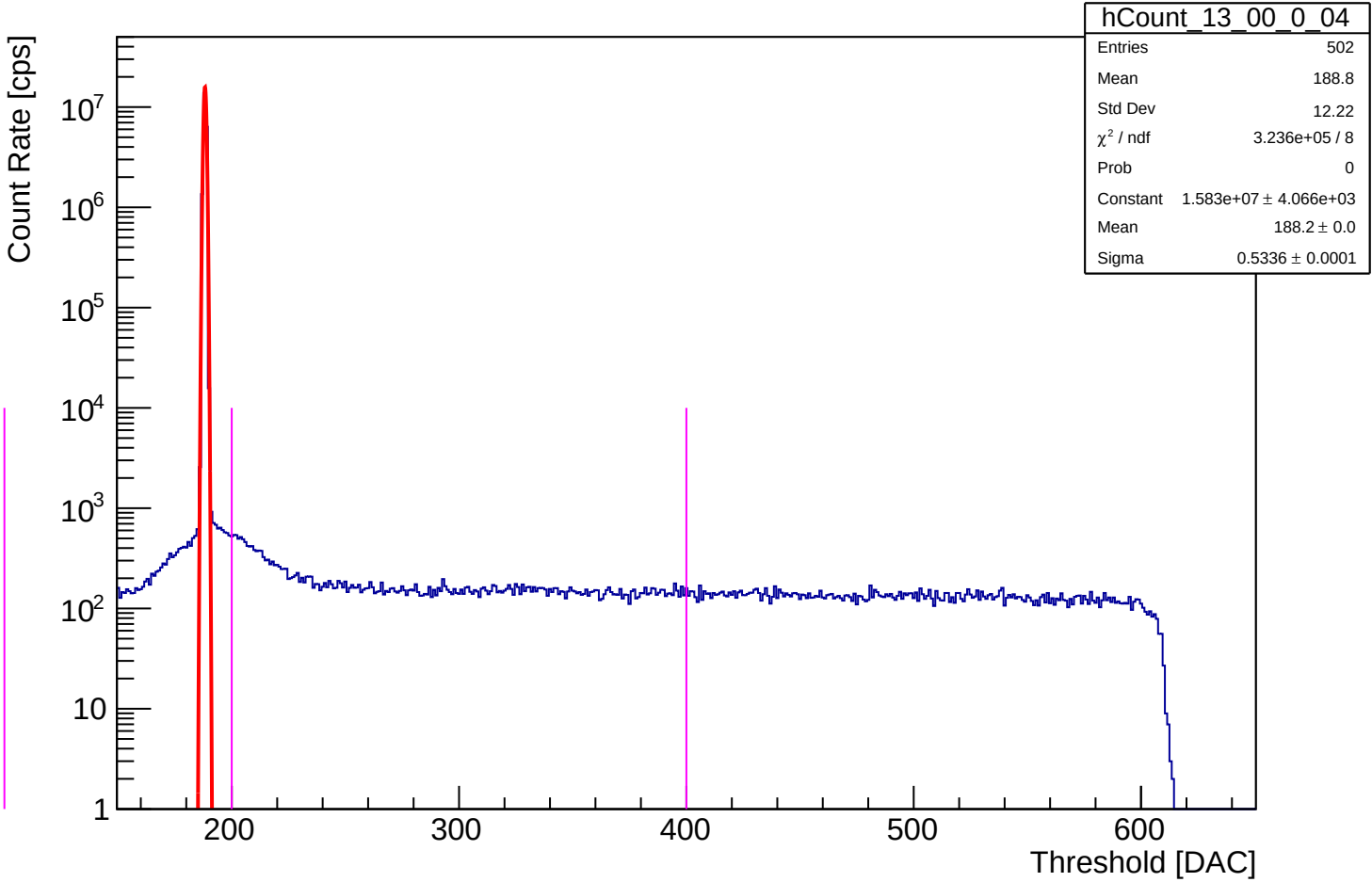
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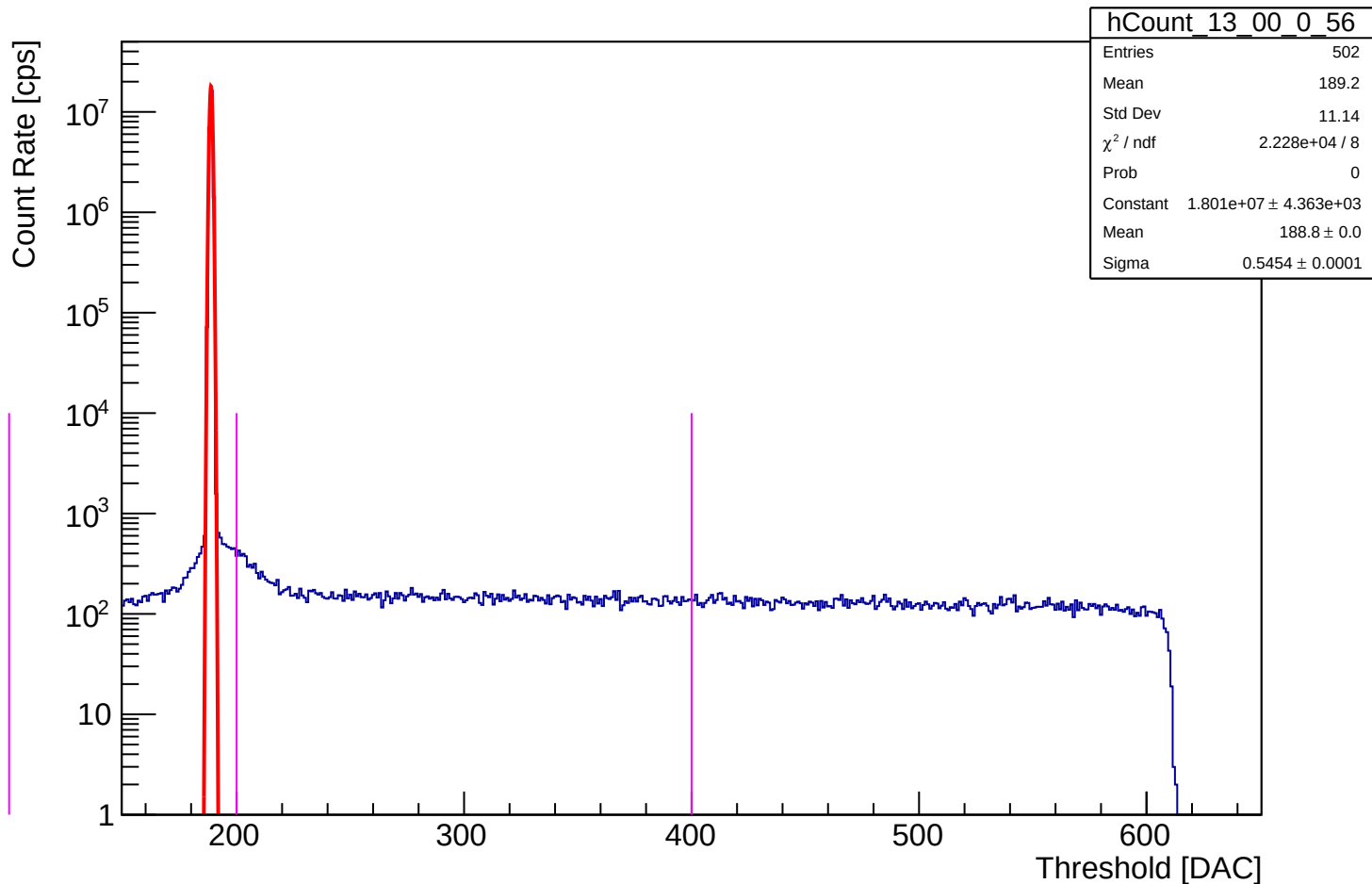




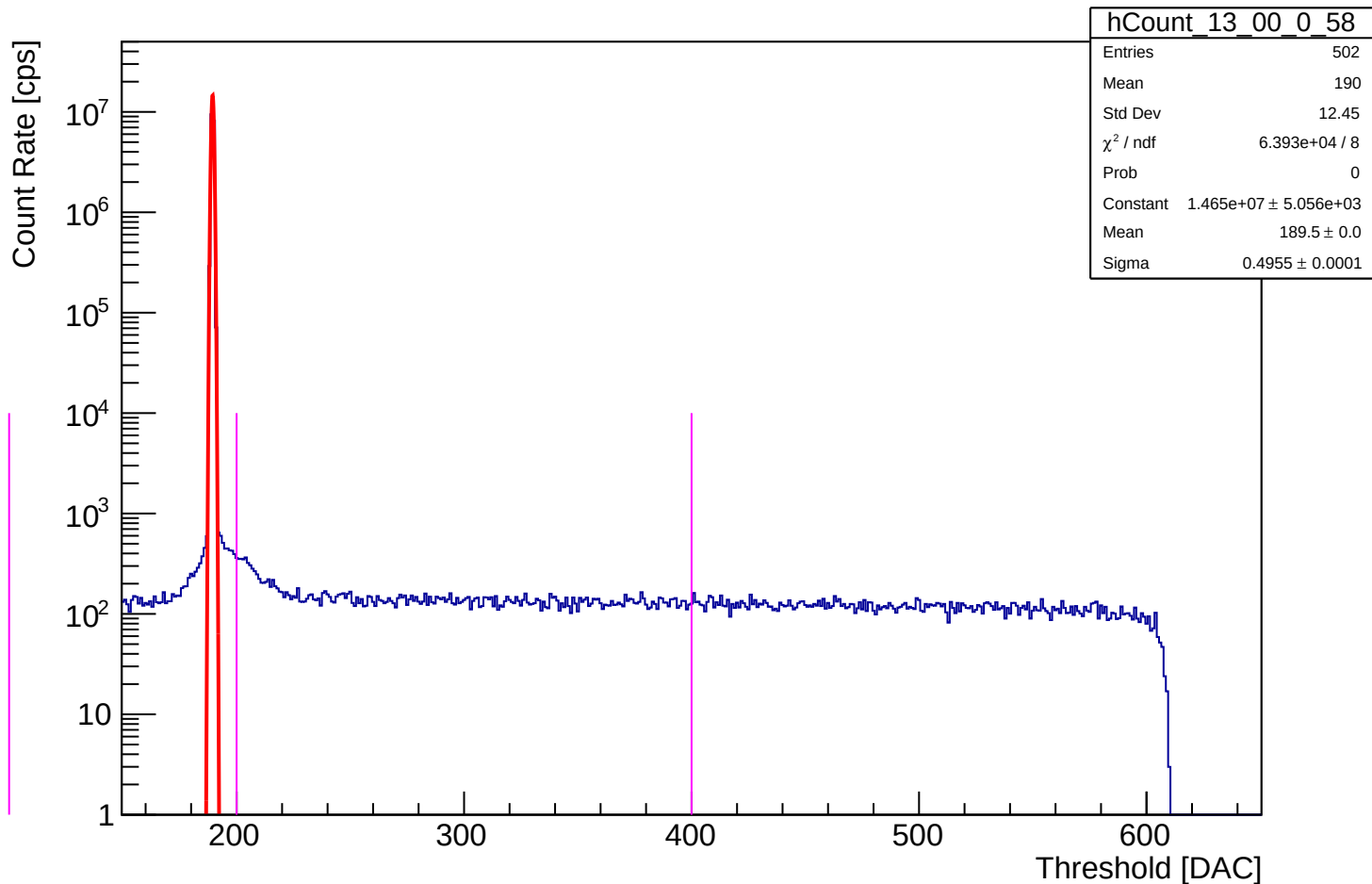




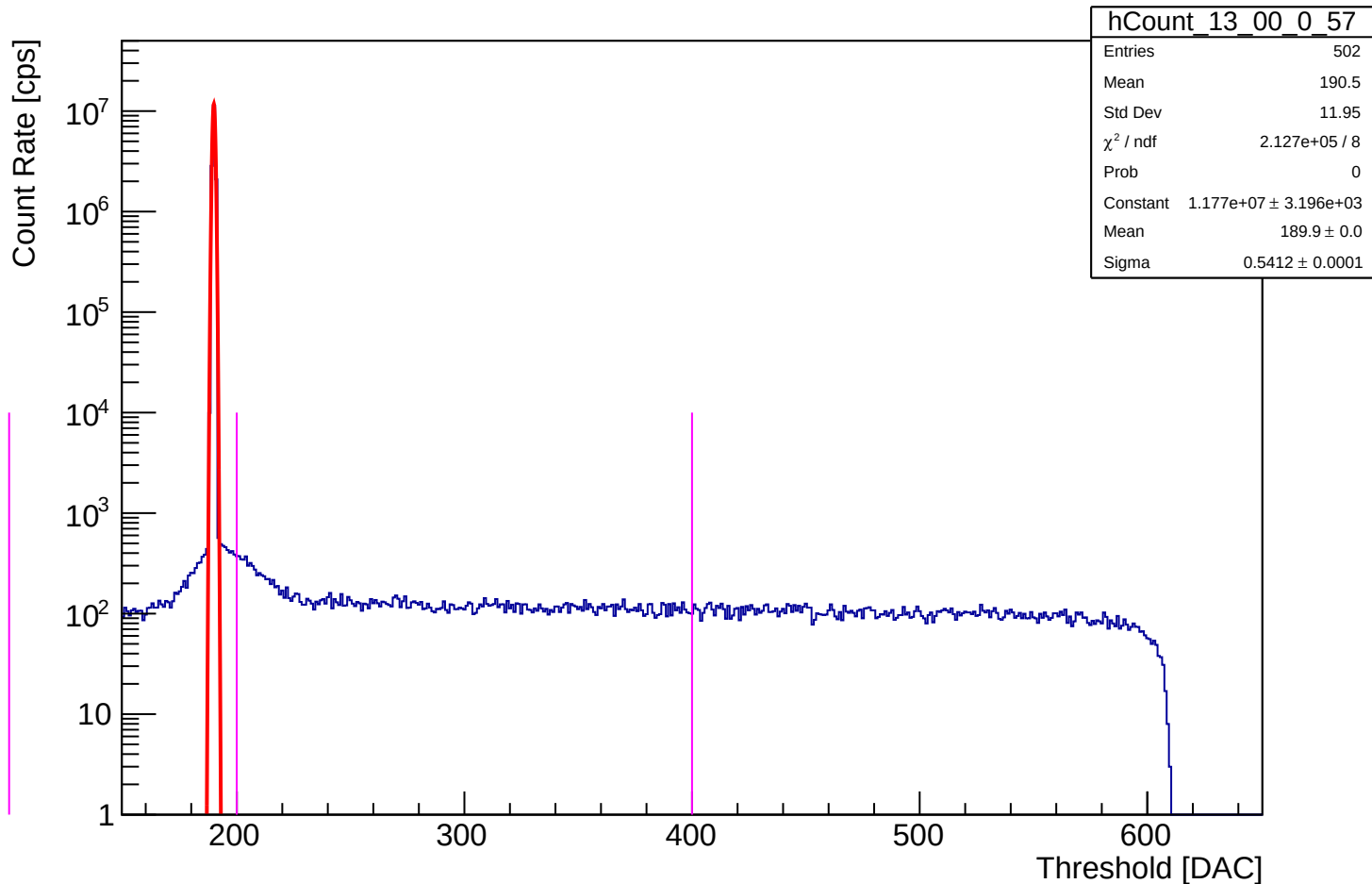
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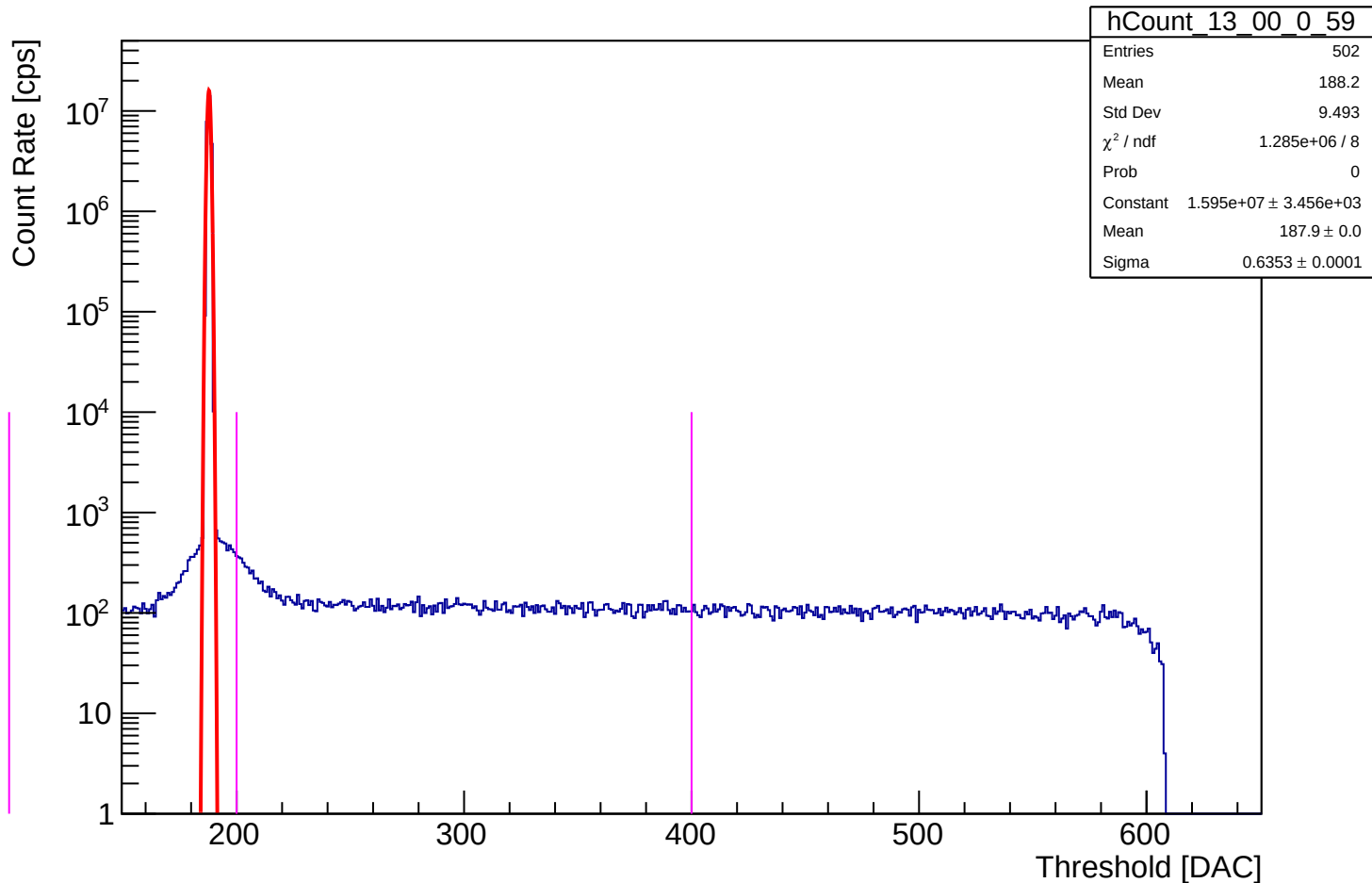
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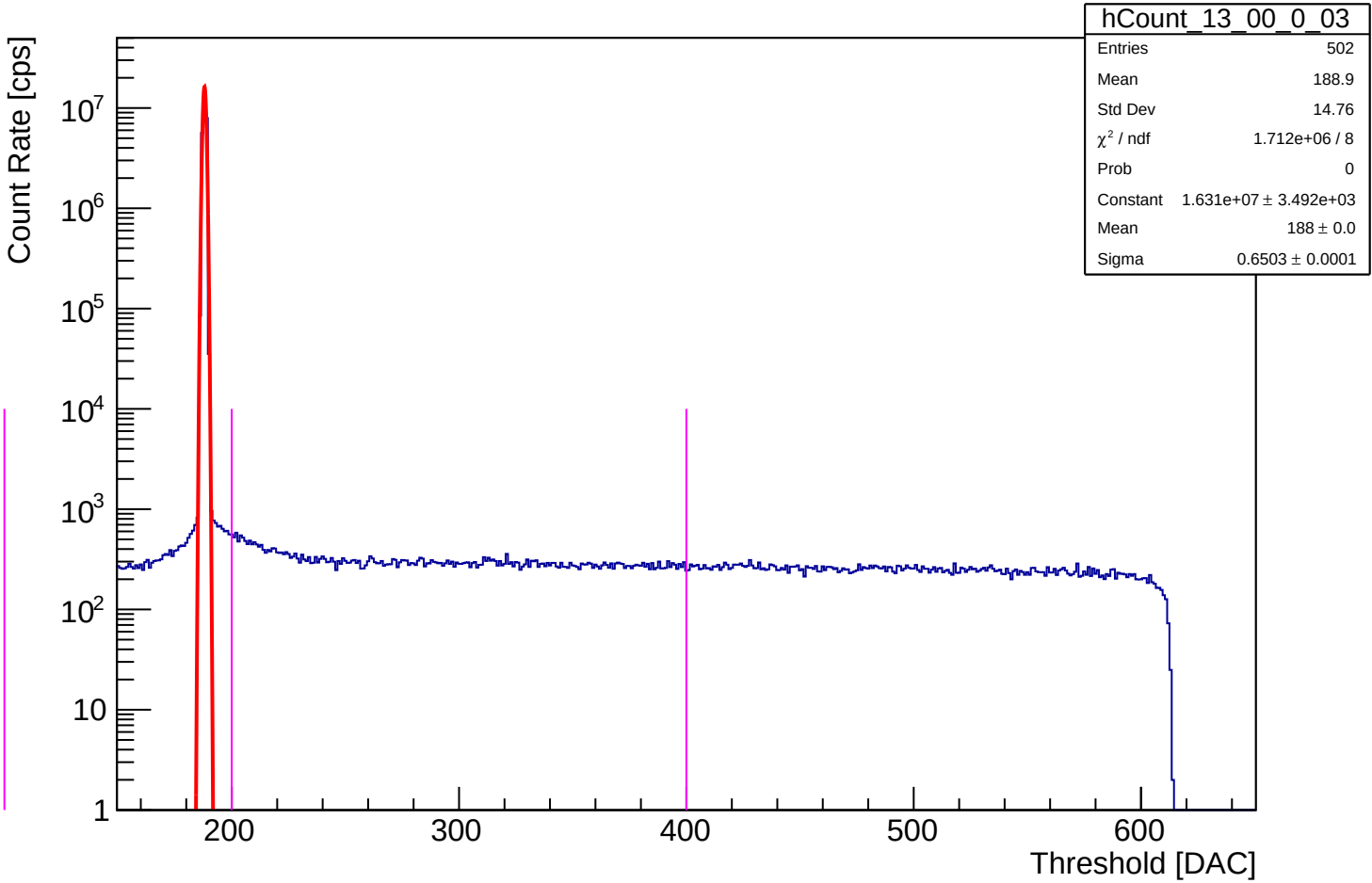


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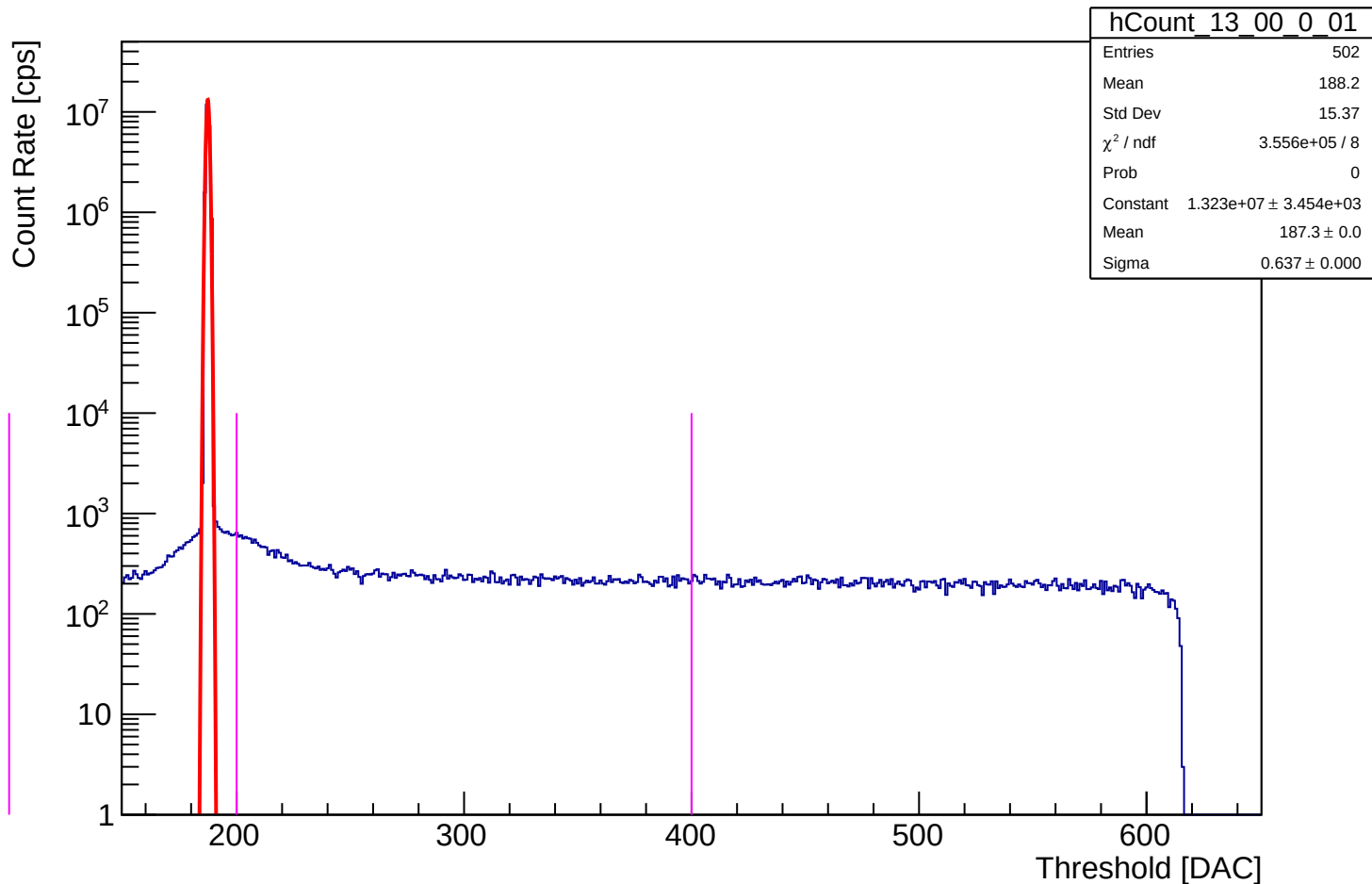


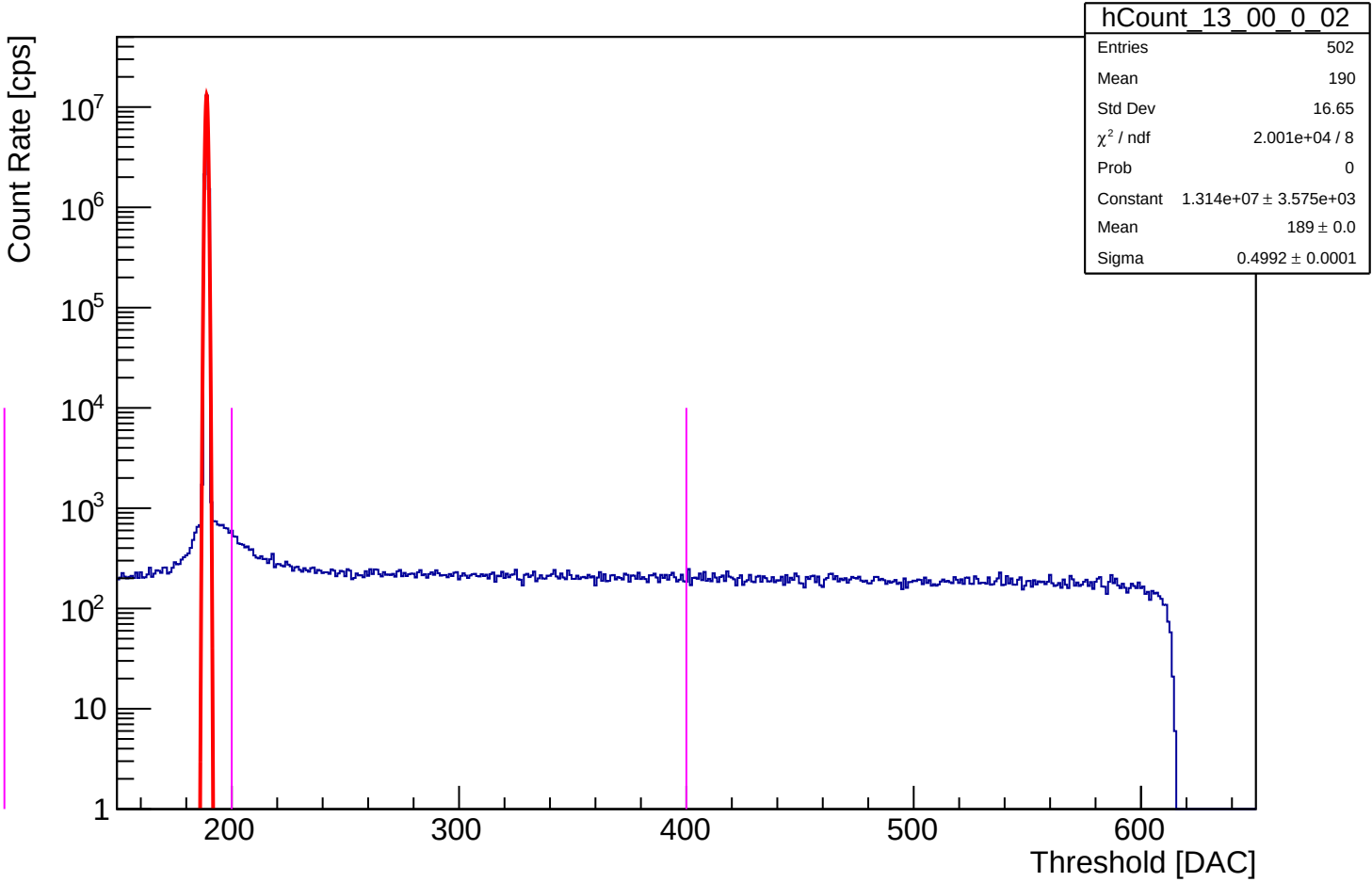
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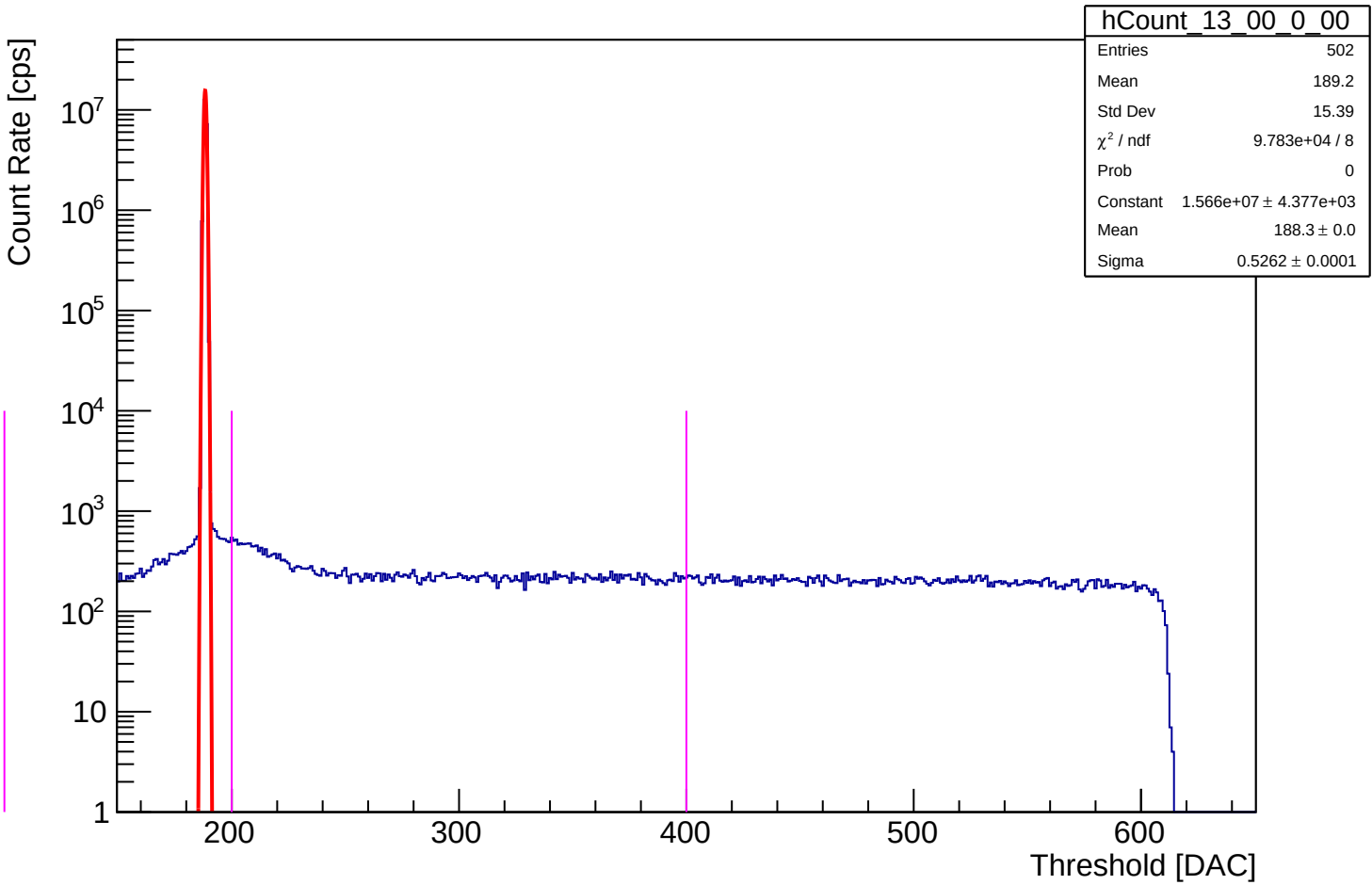




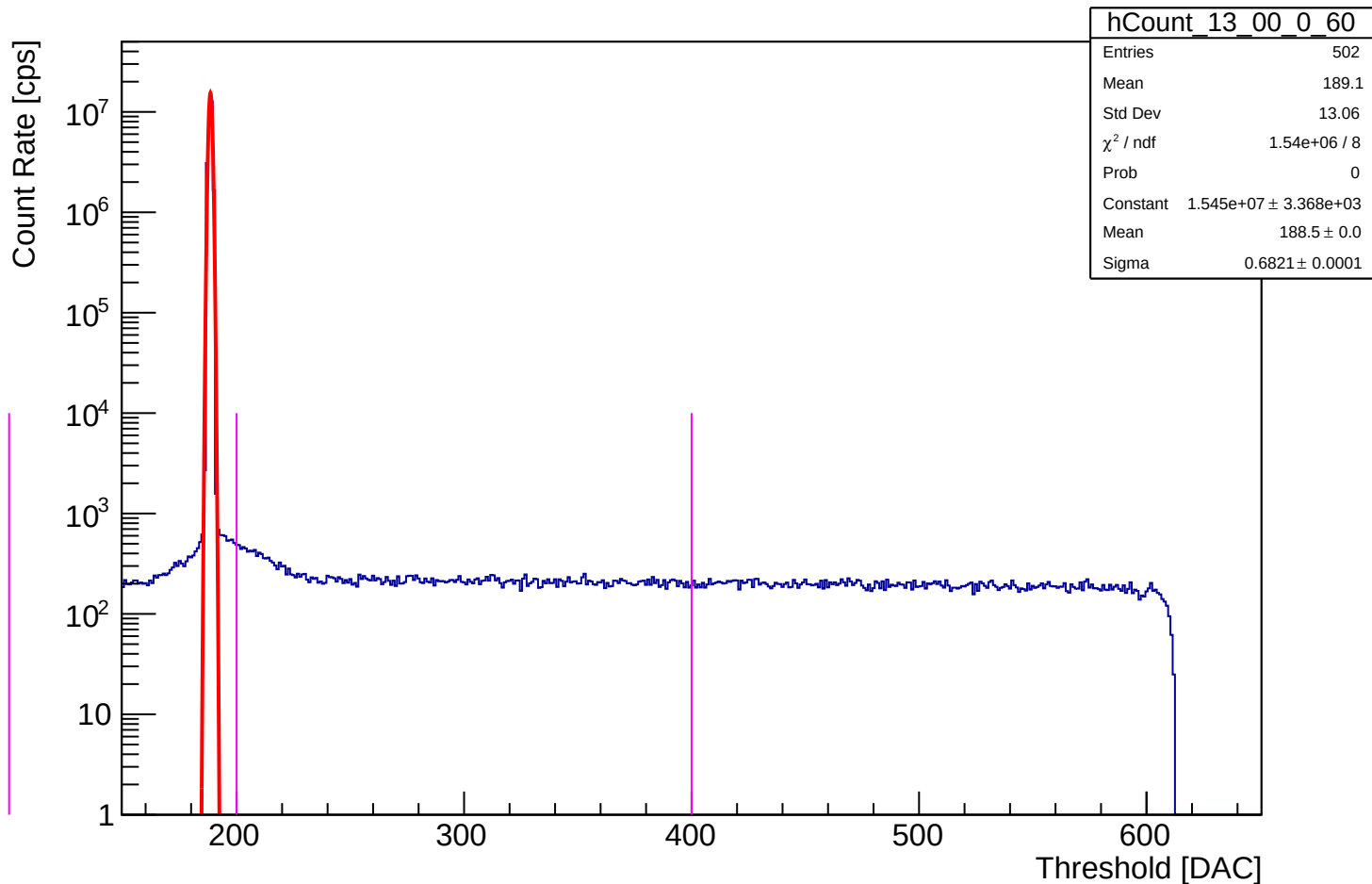
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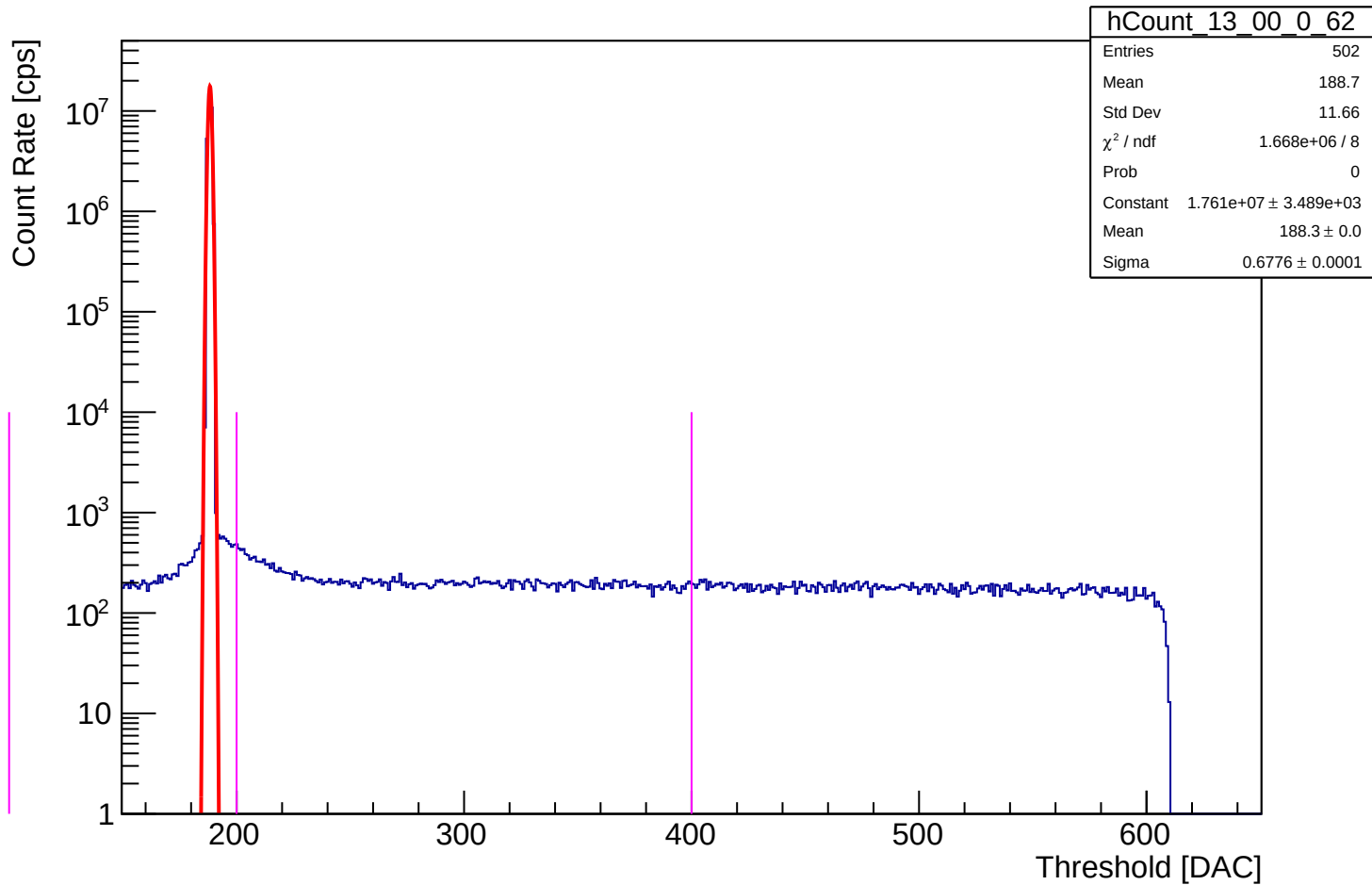


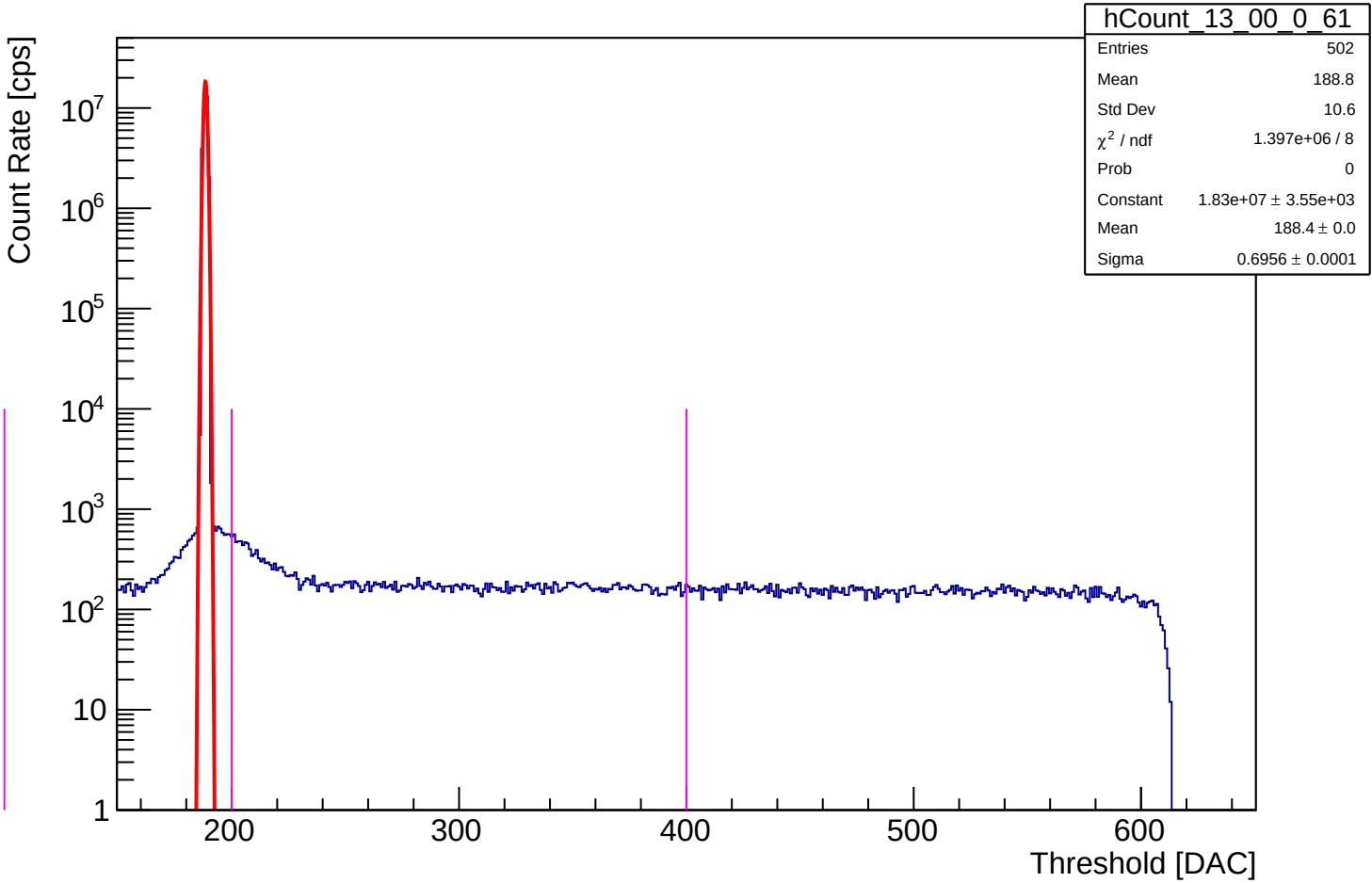


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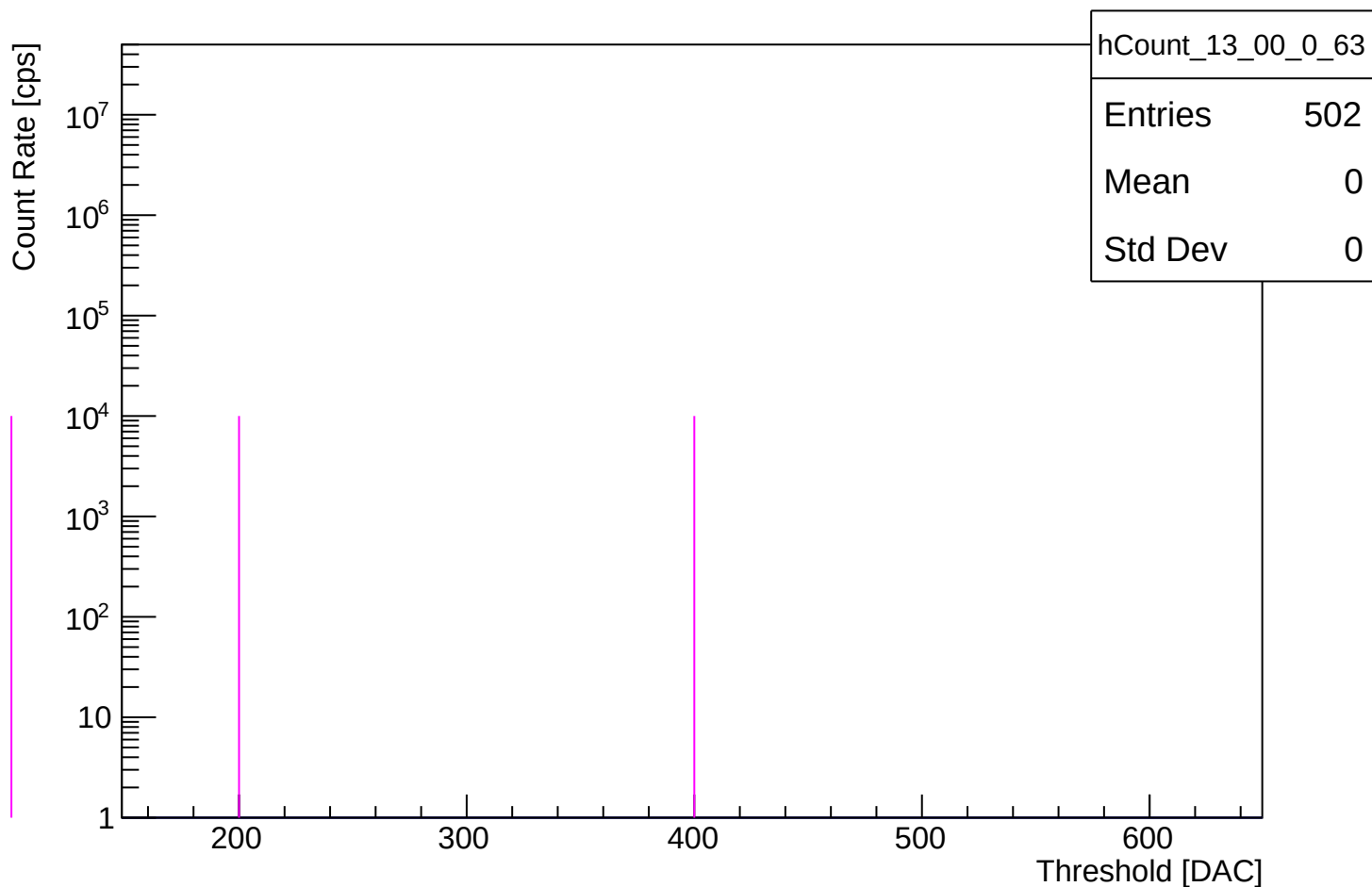


Row 1 Tile 1 Pmt 1 Pixel 62 Slot 13 Fiber 0 Asic 0 Channel 62

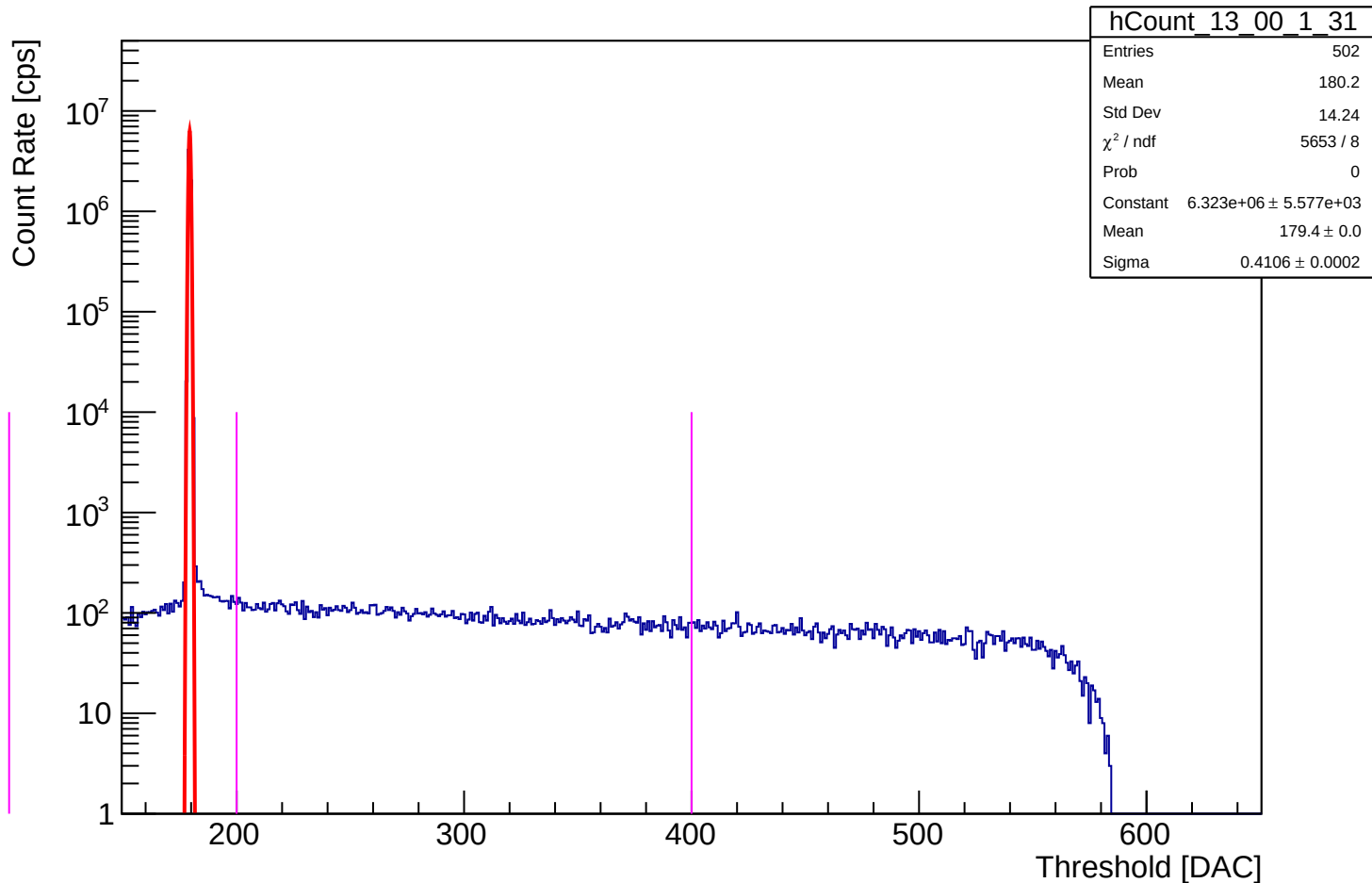




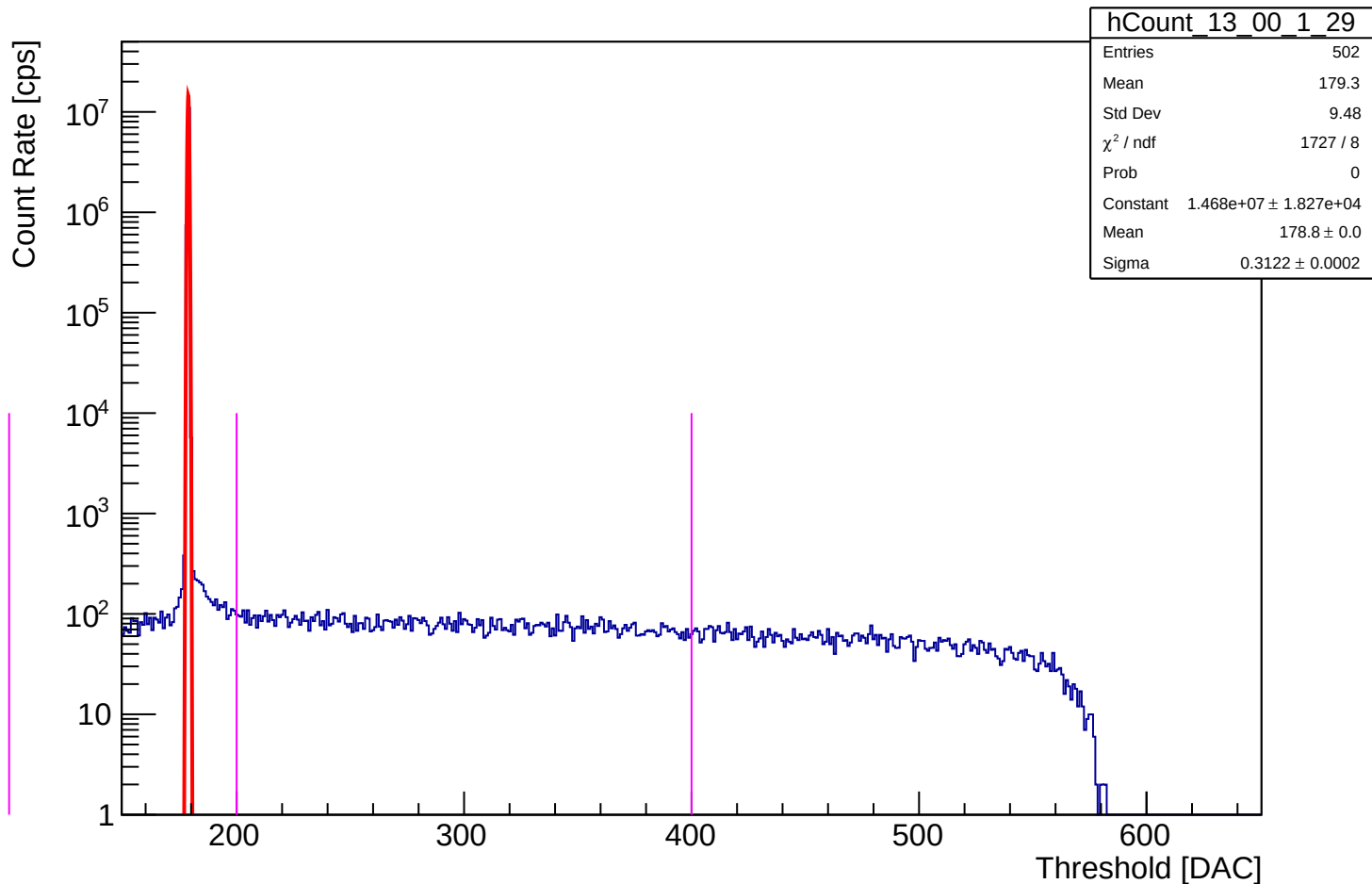
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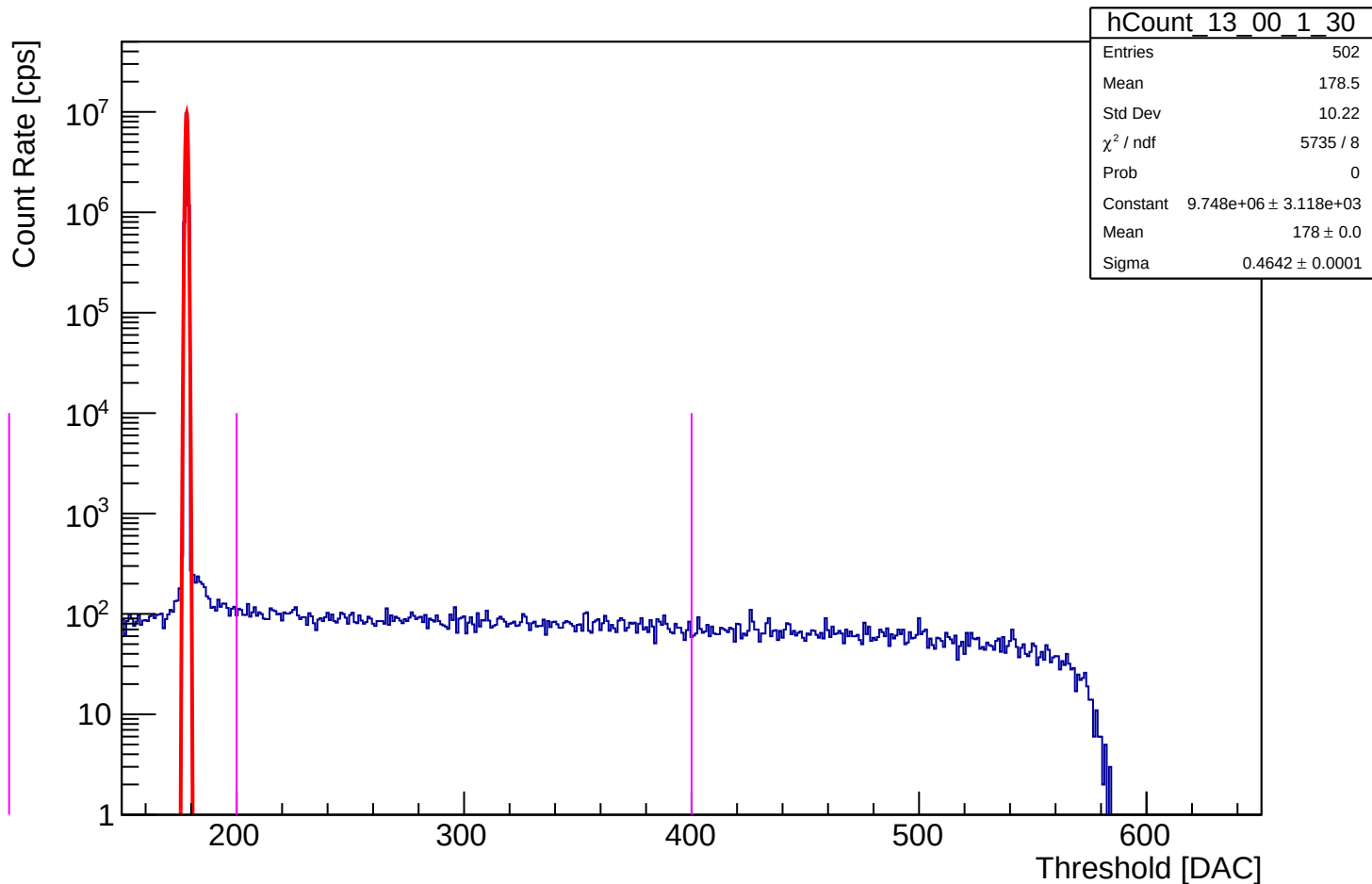
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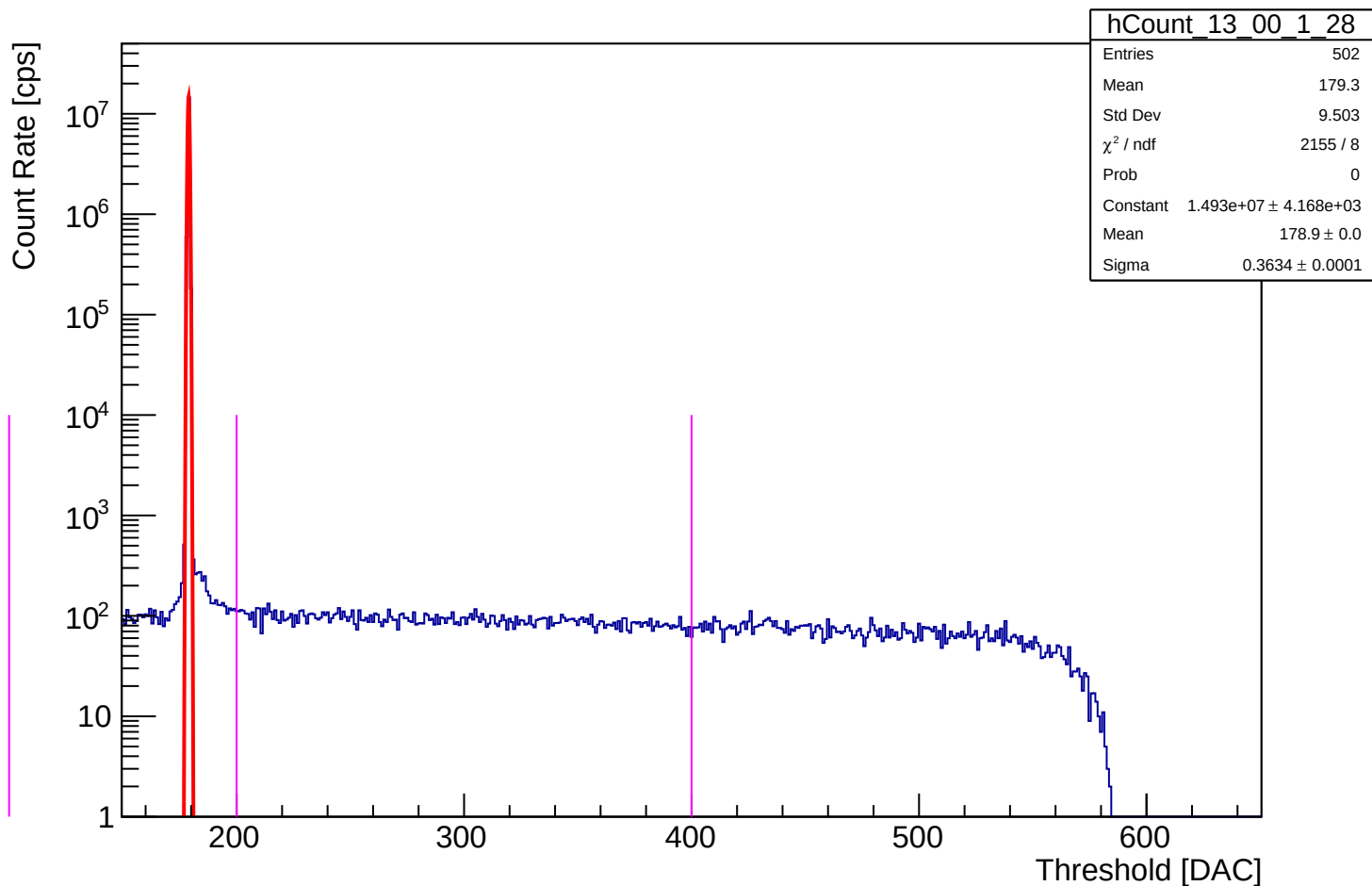
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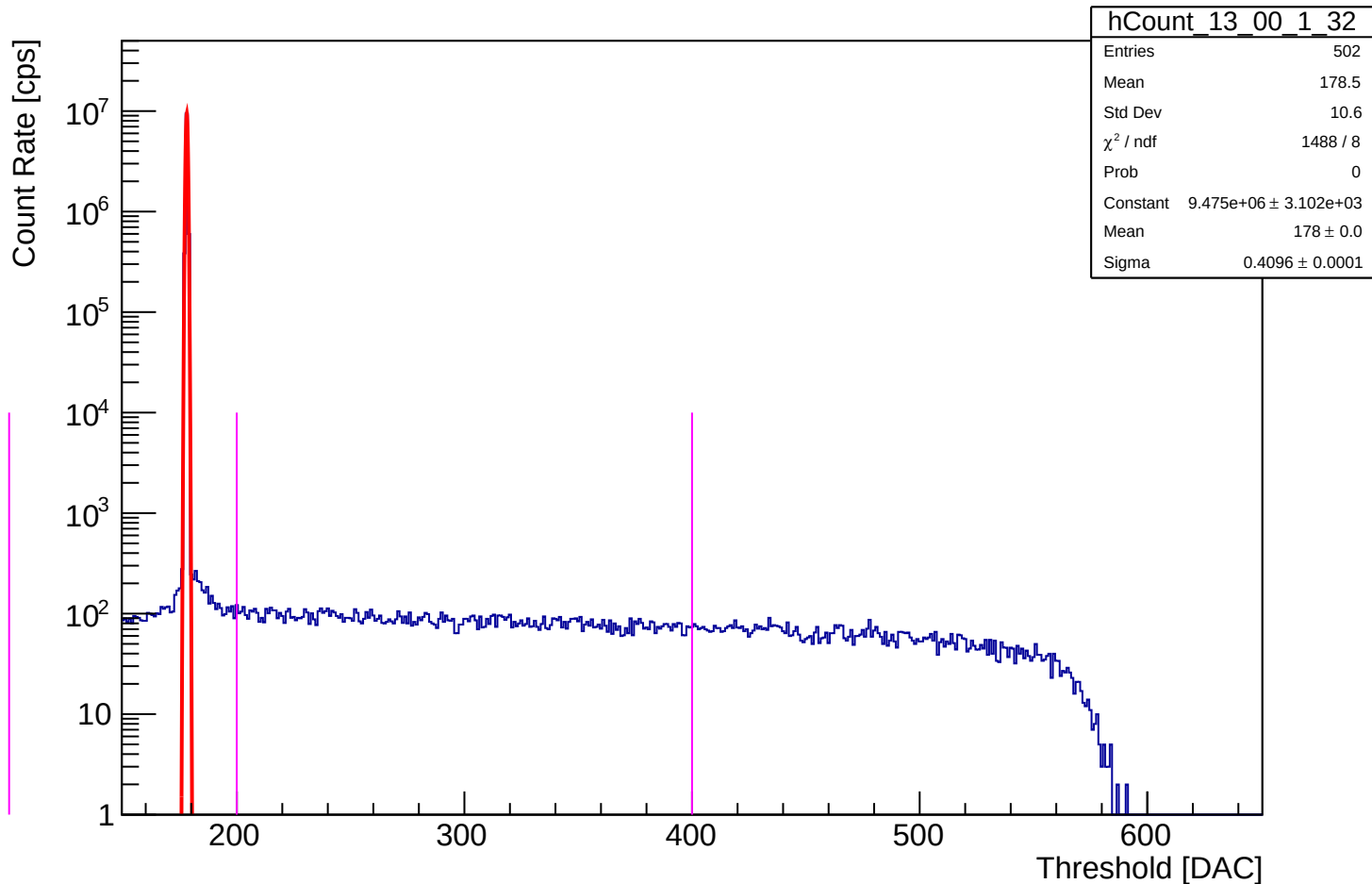
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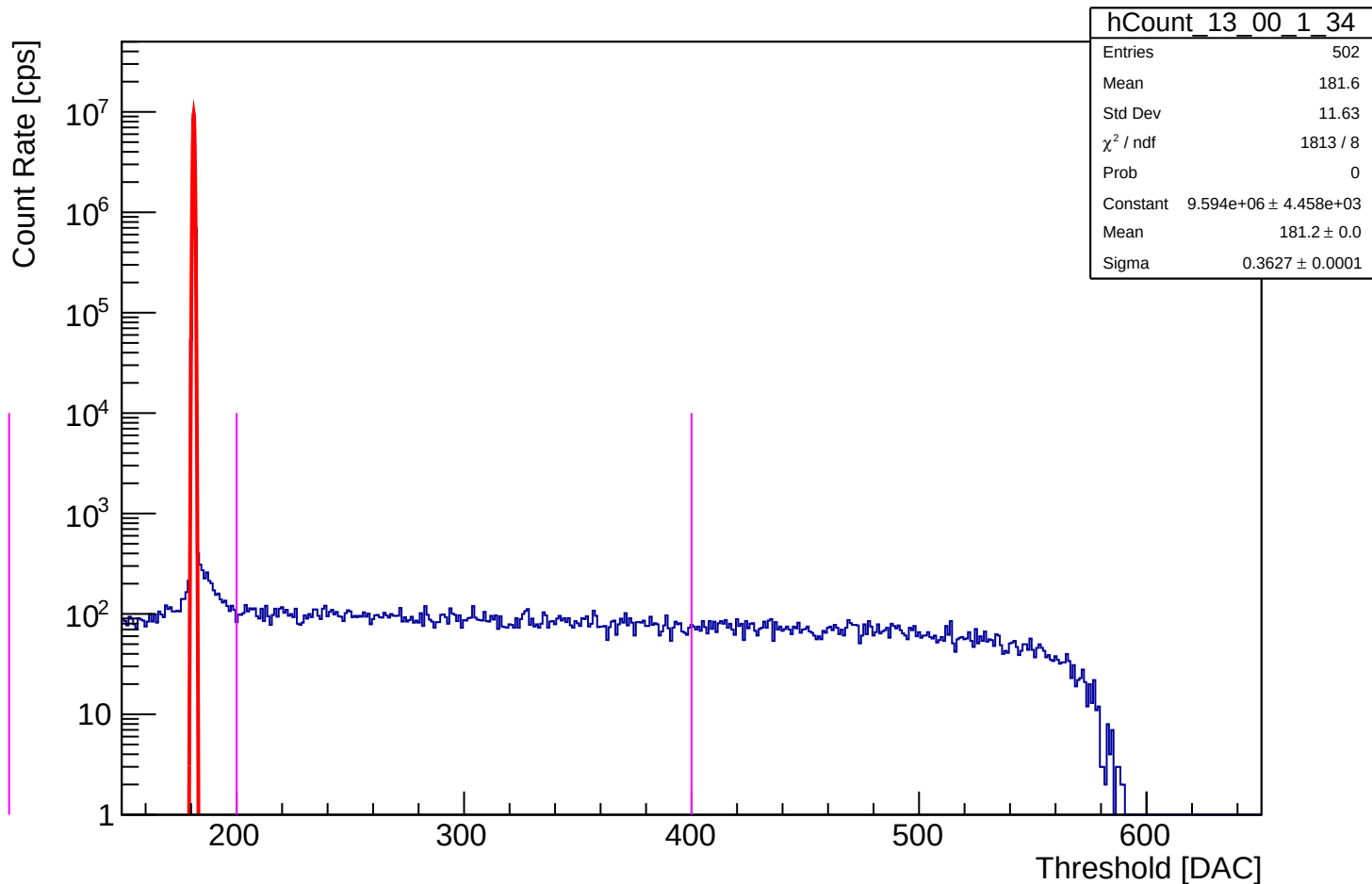
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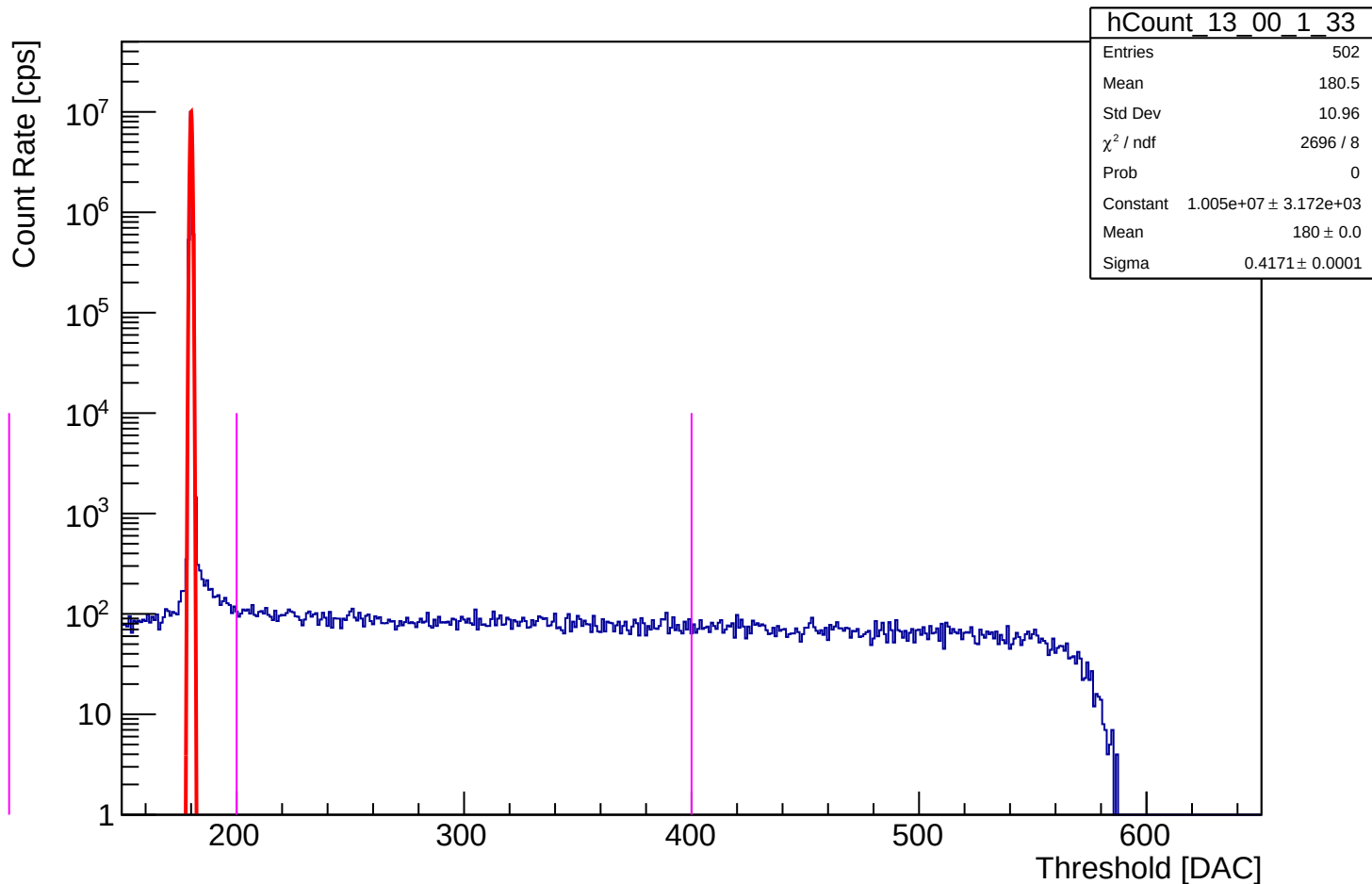
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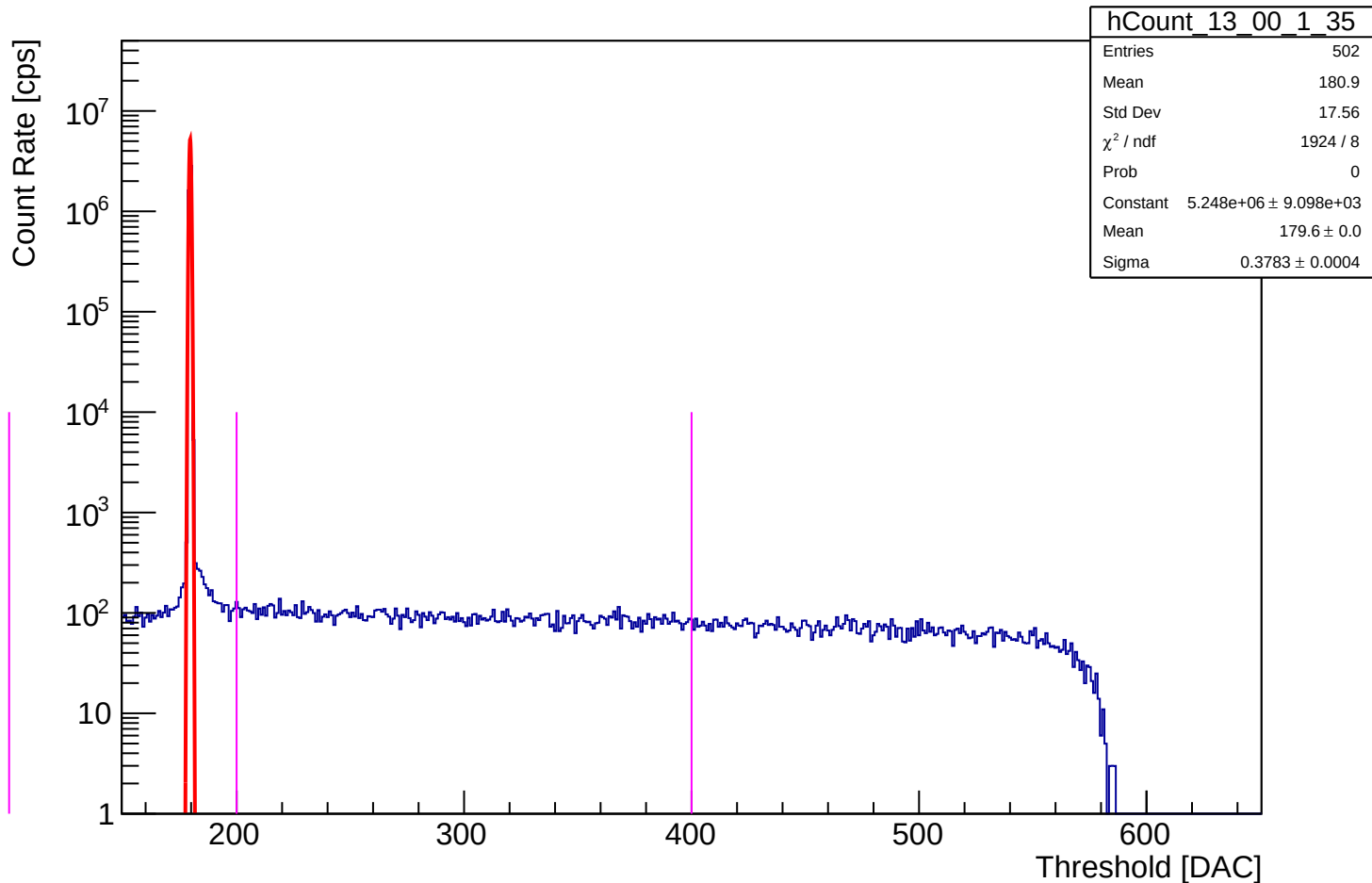
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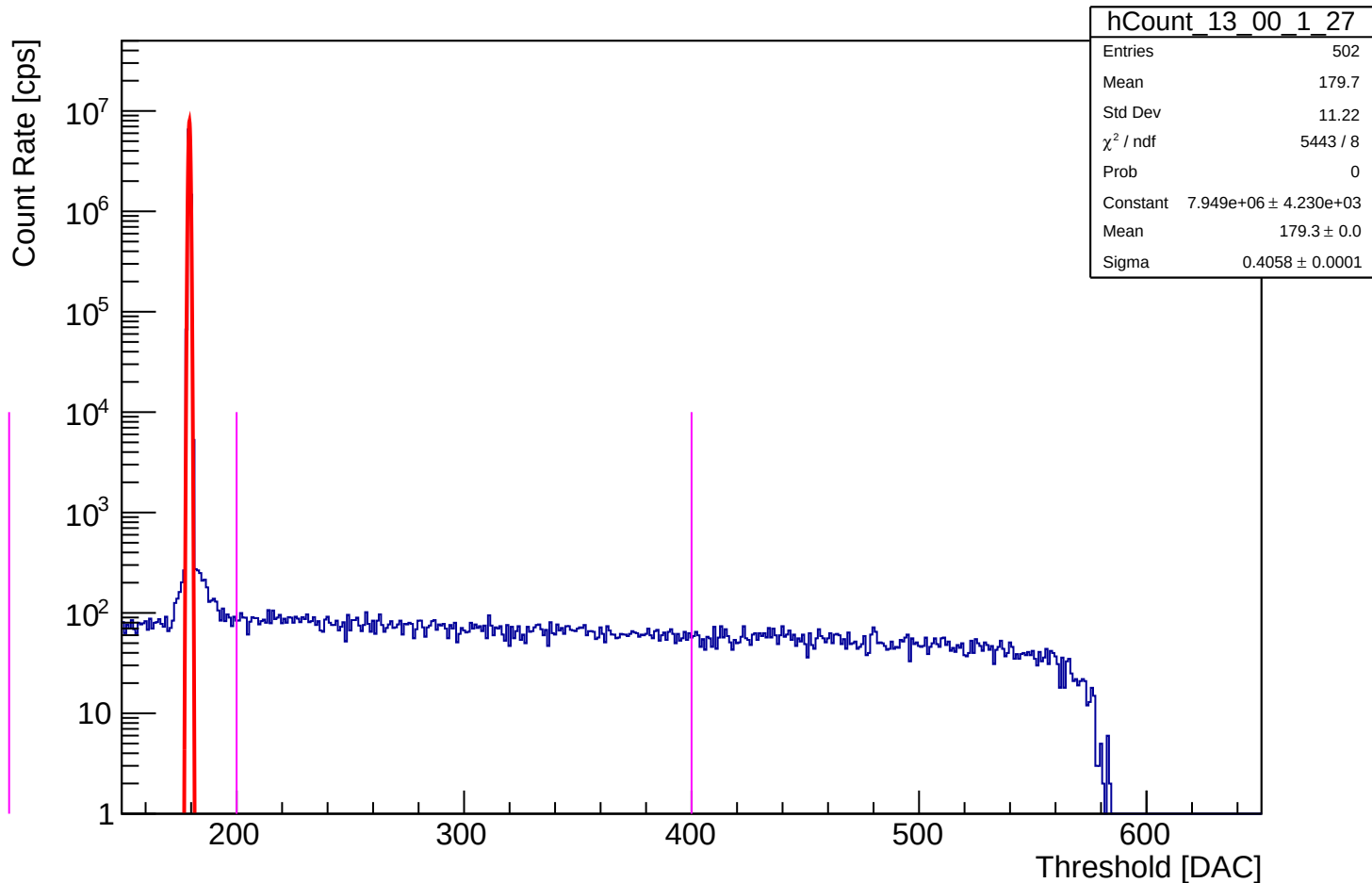
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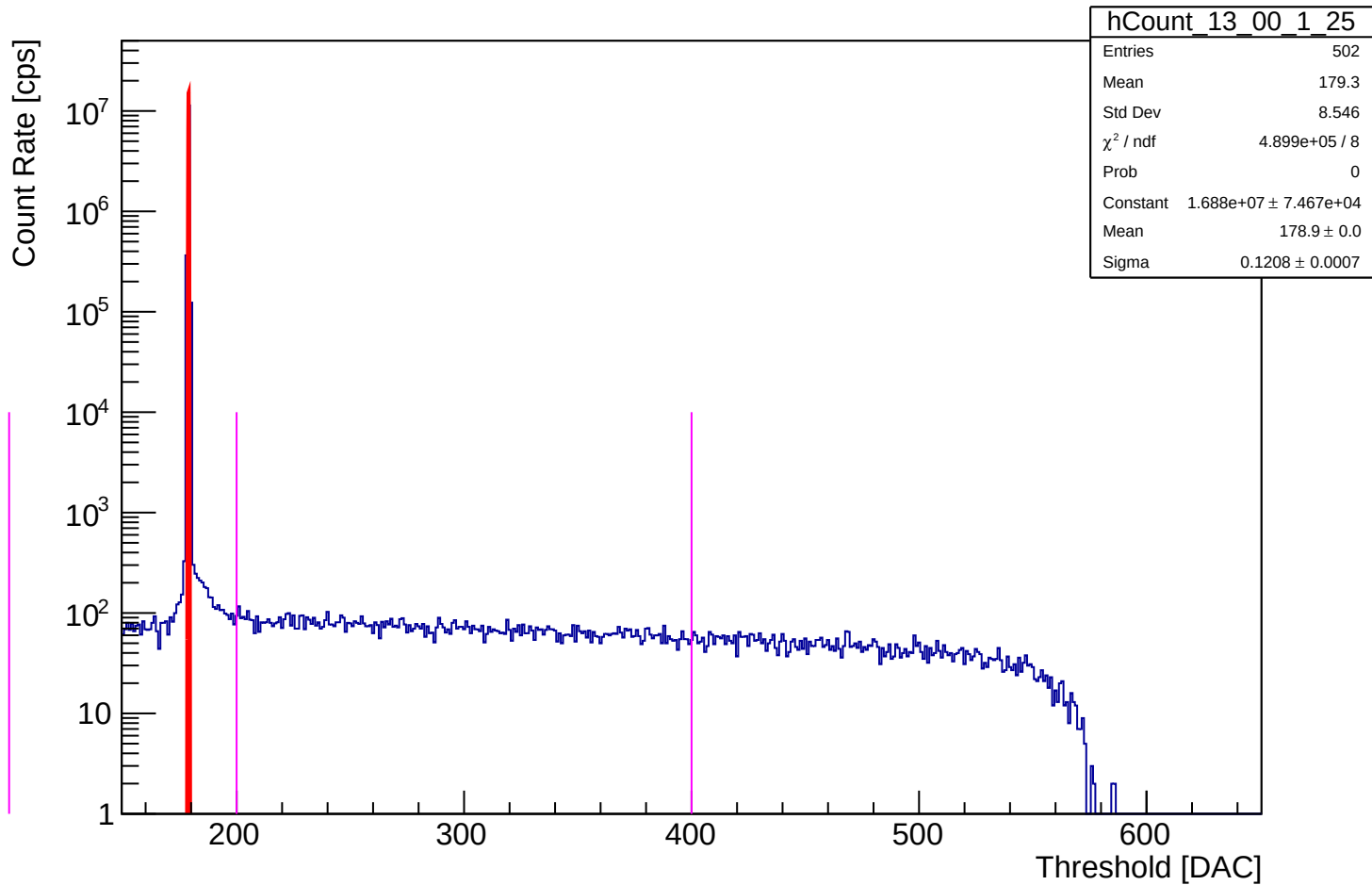
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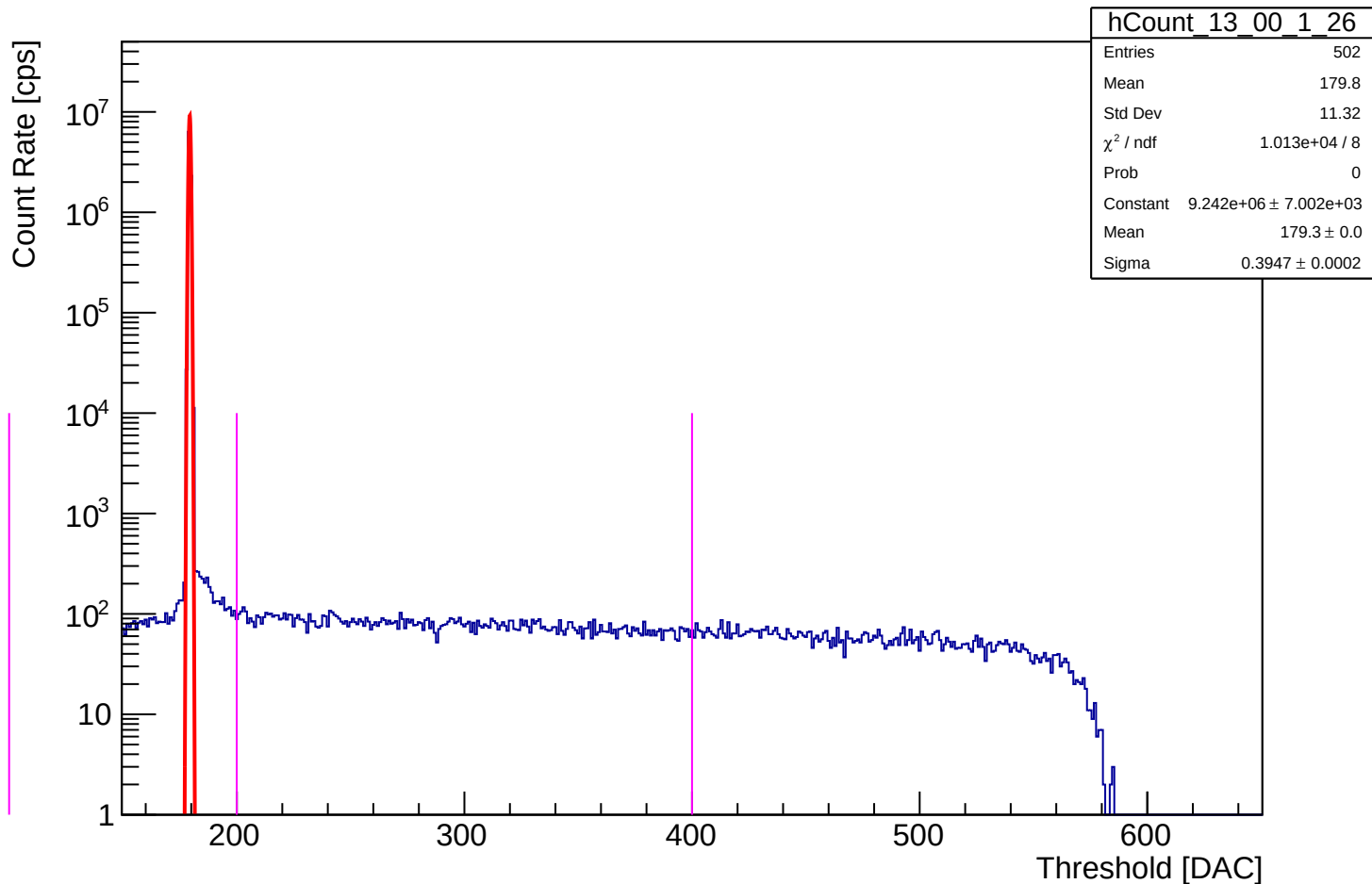
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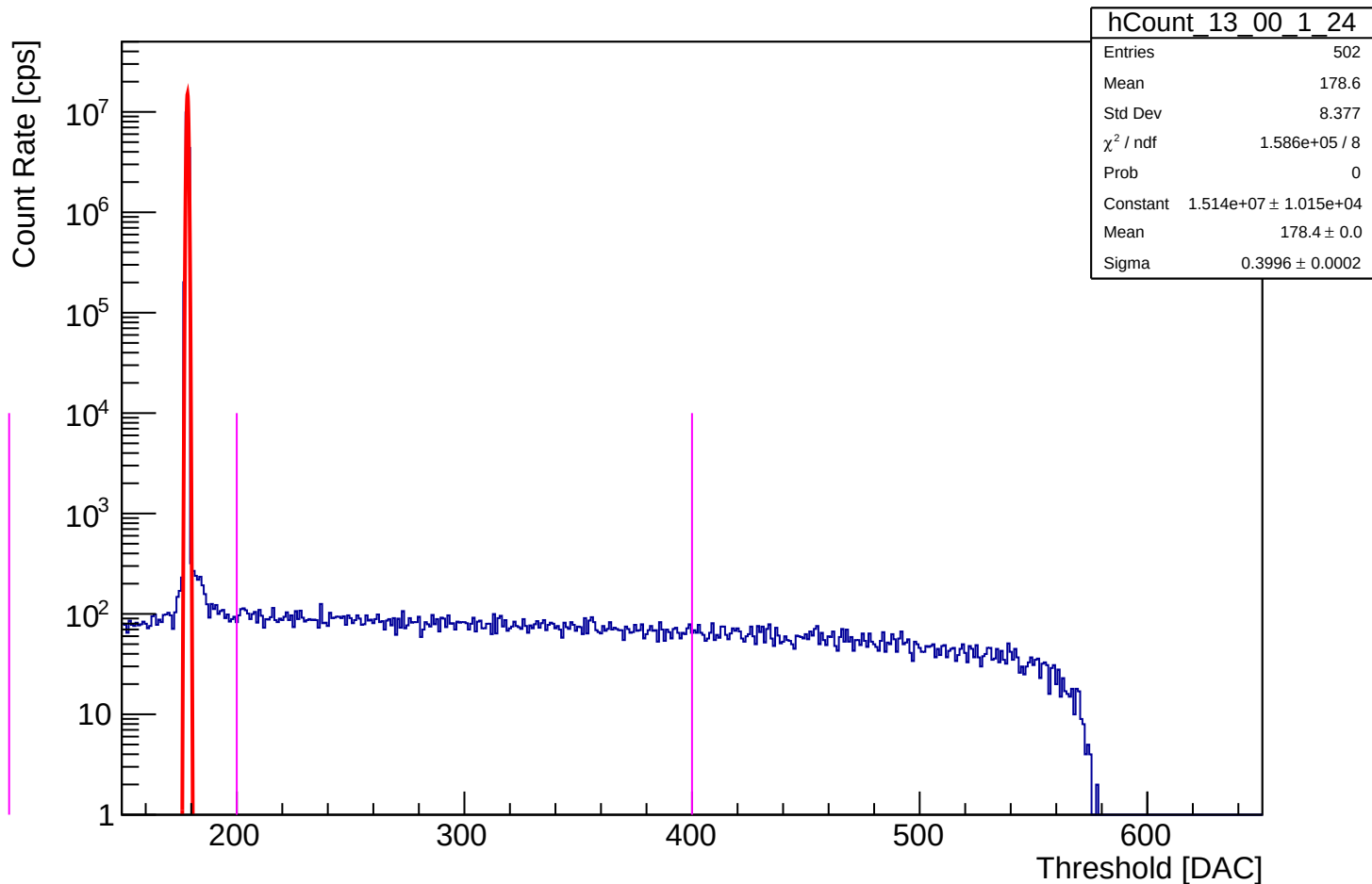
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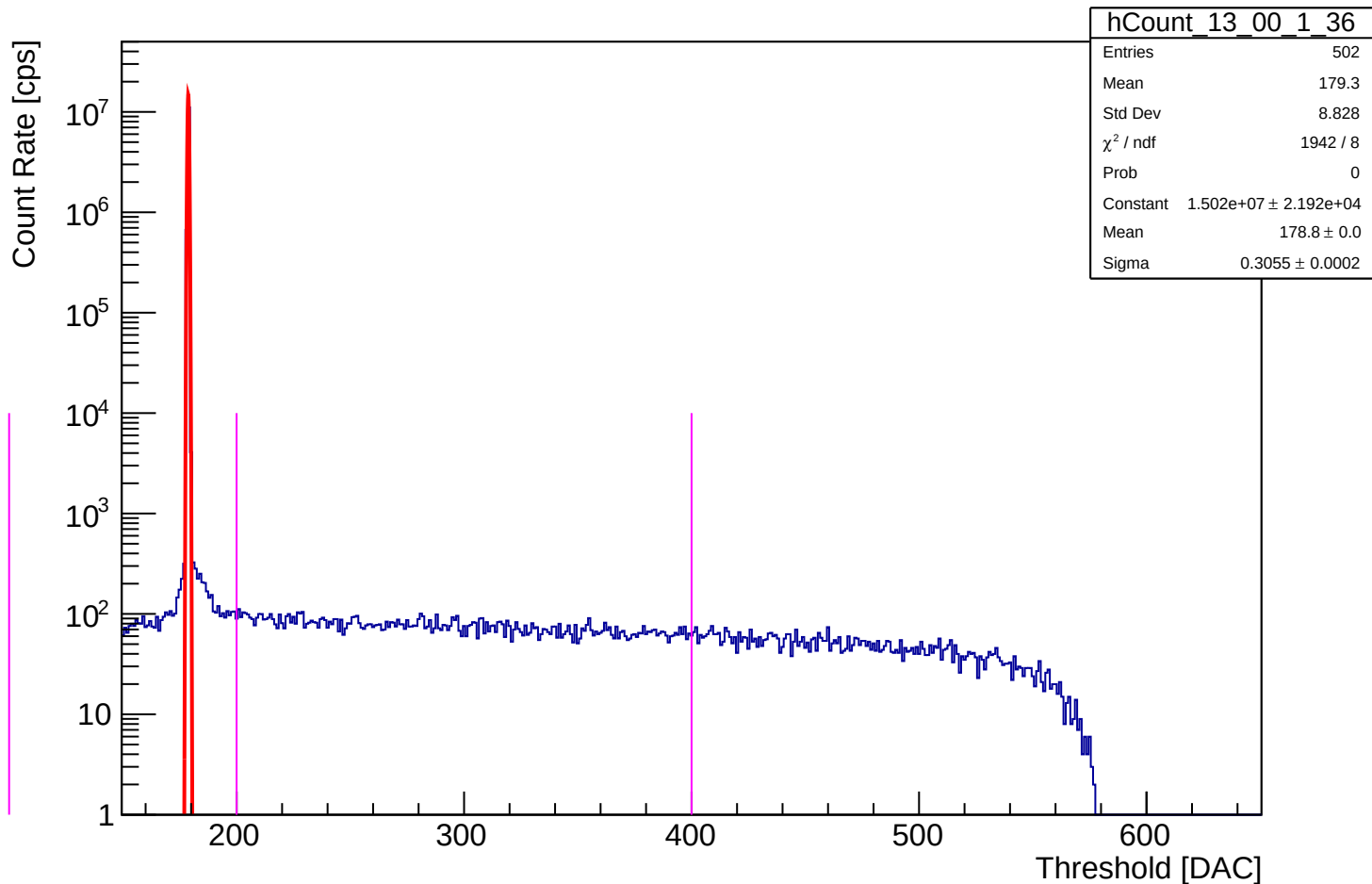
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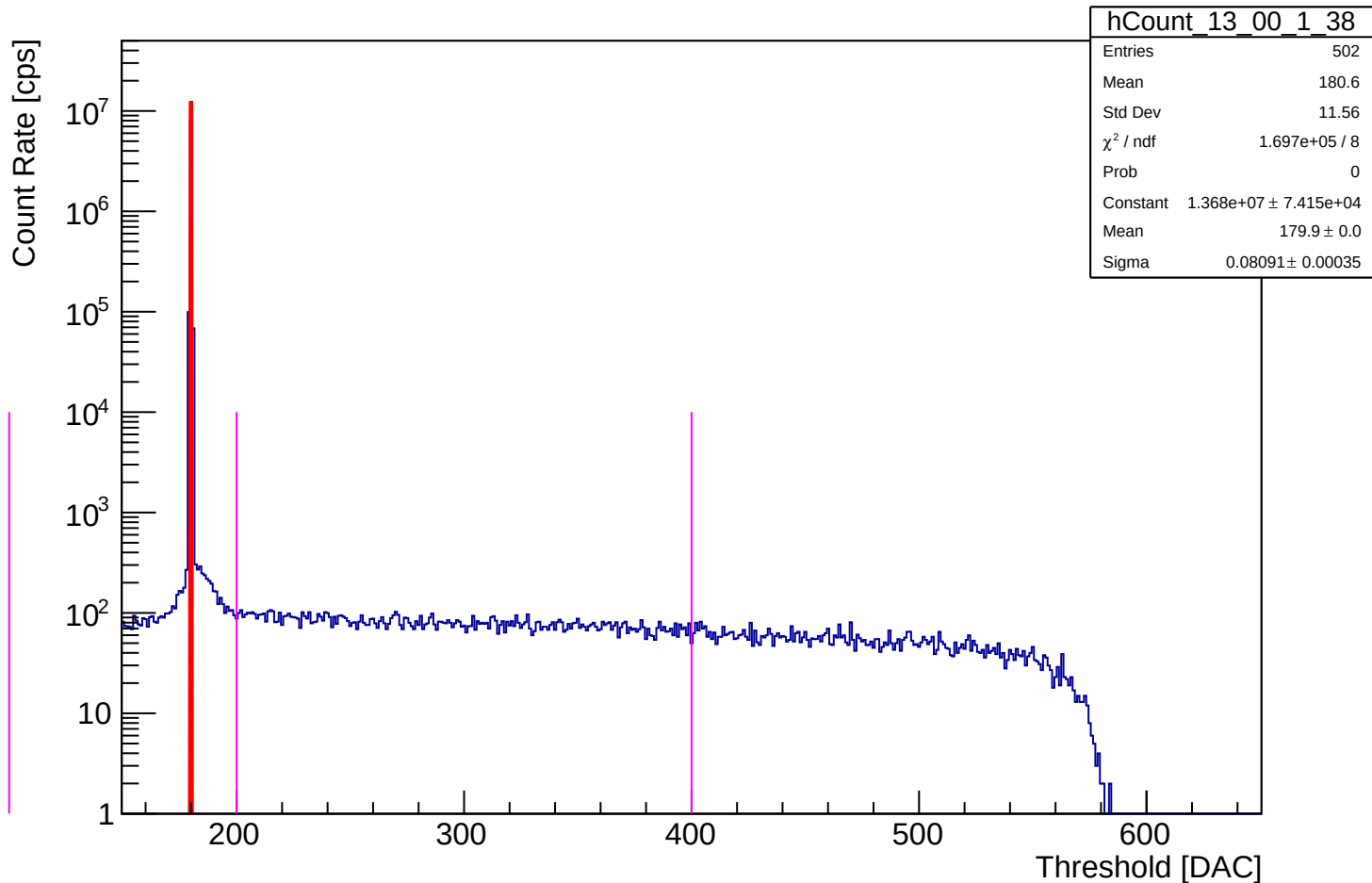
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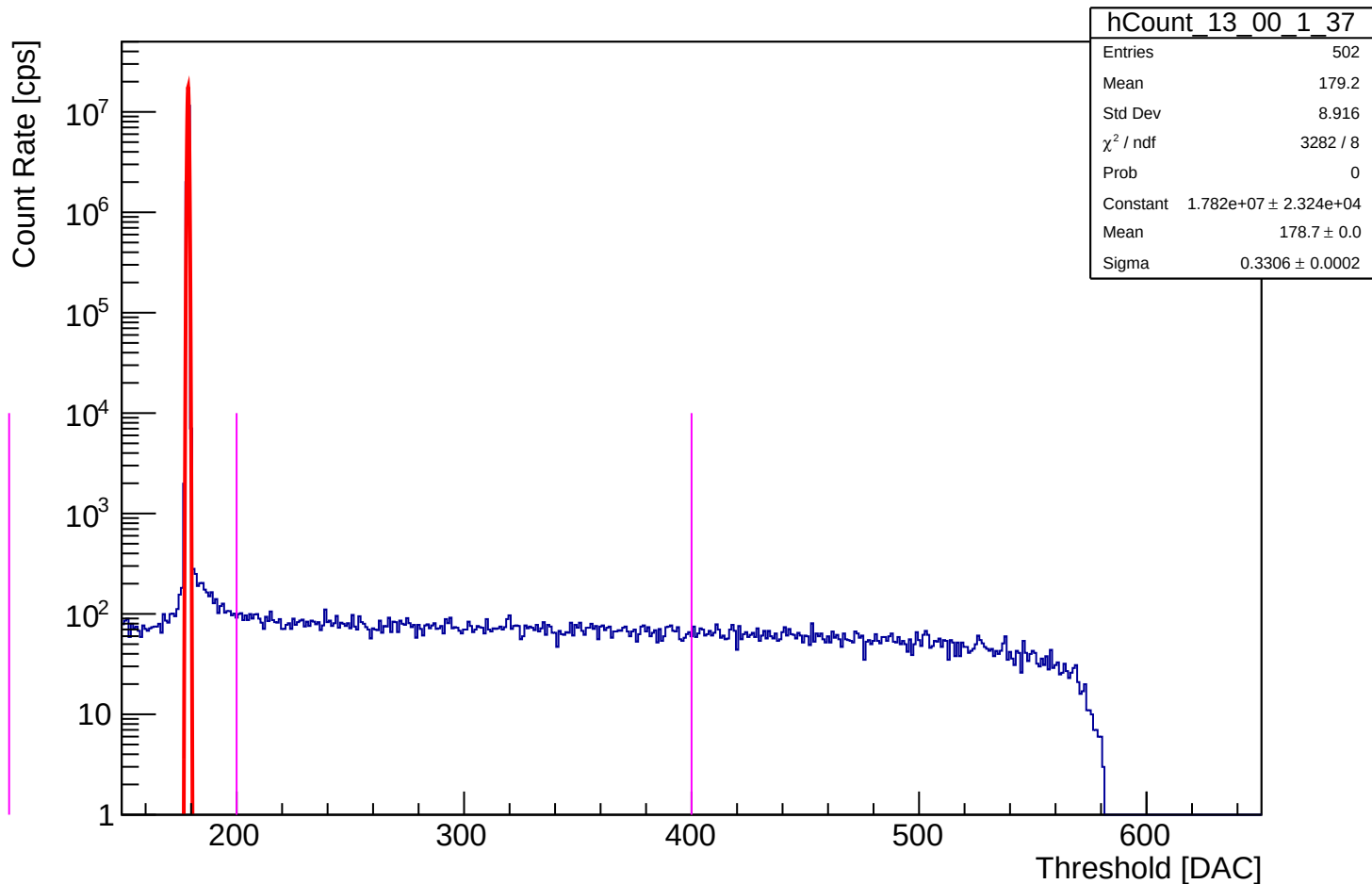
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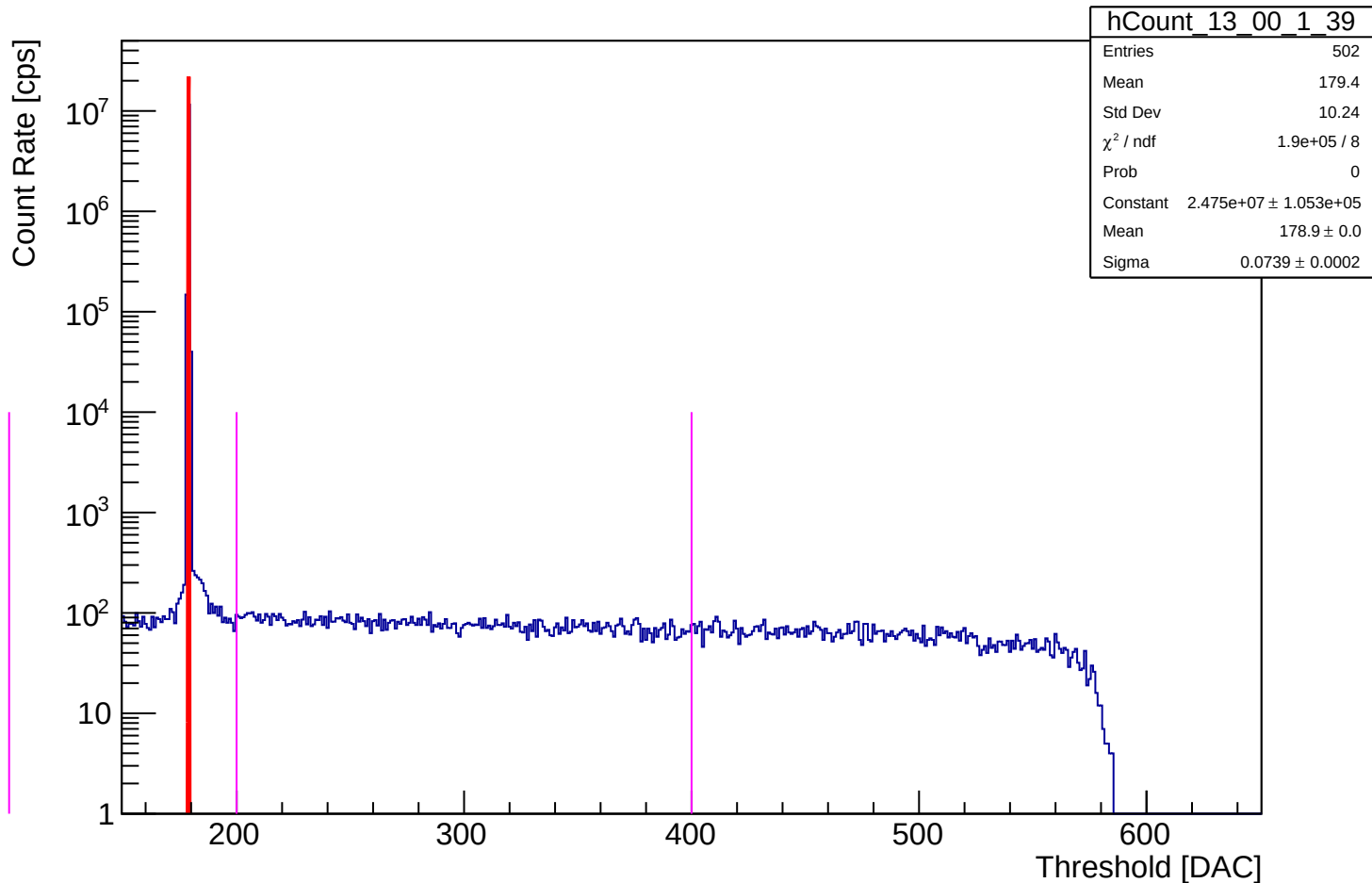
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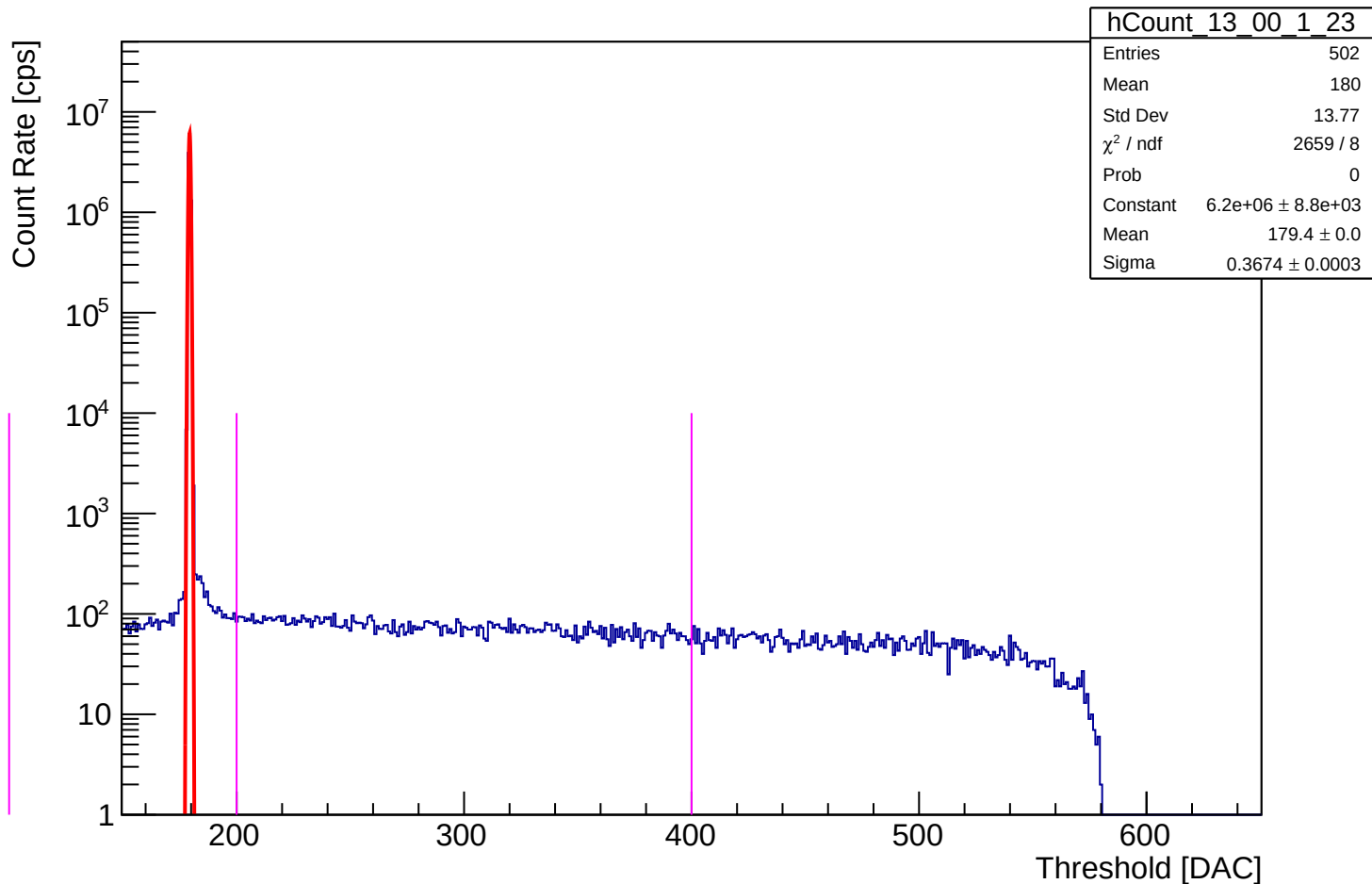
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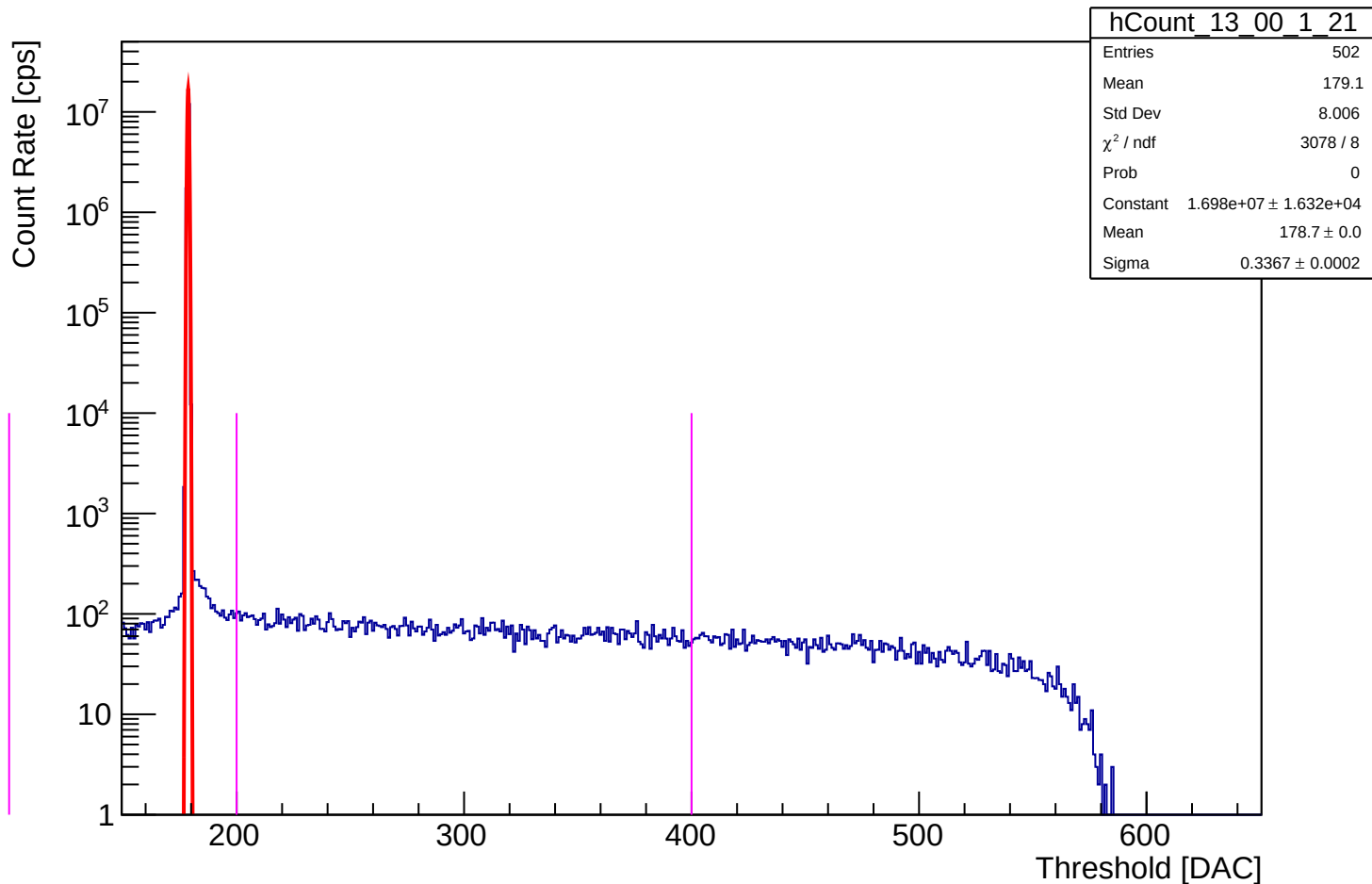
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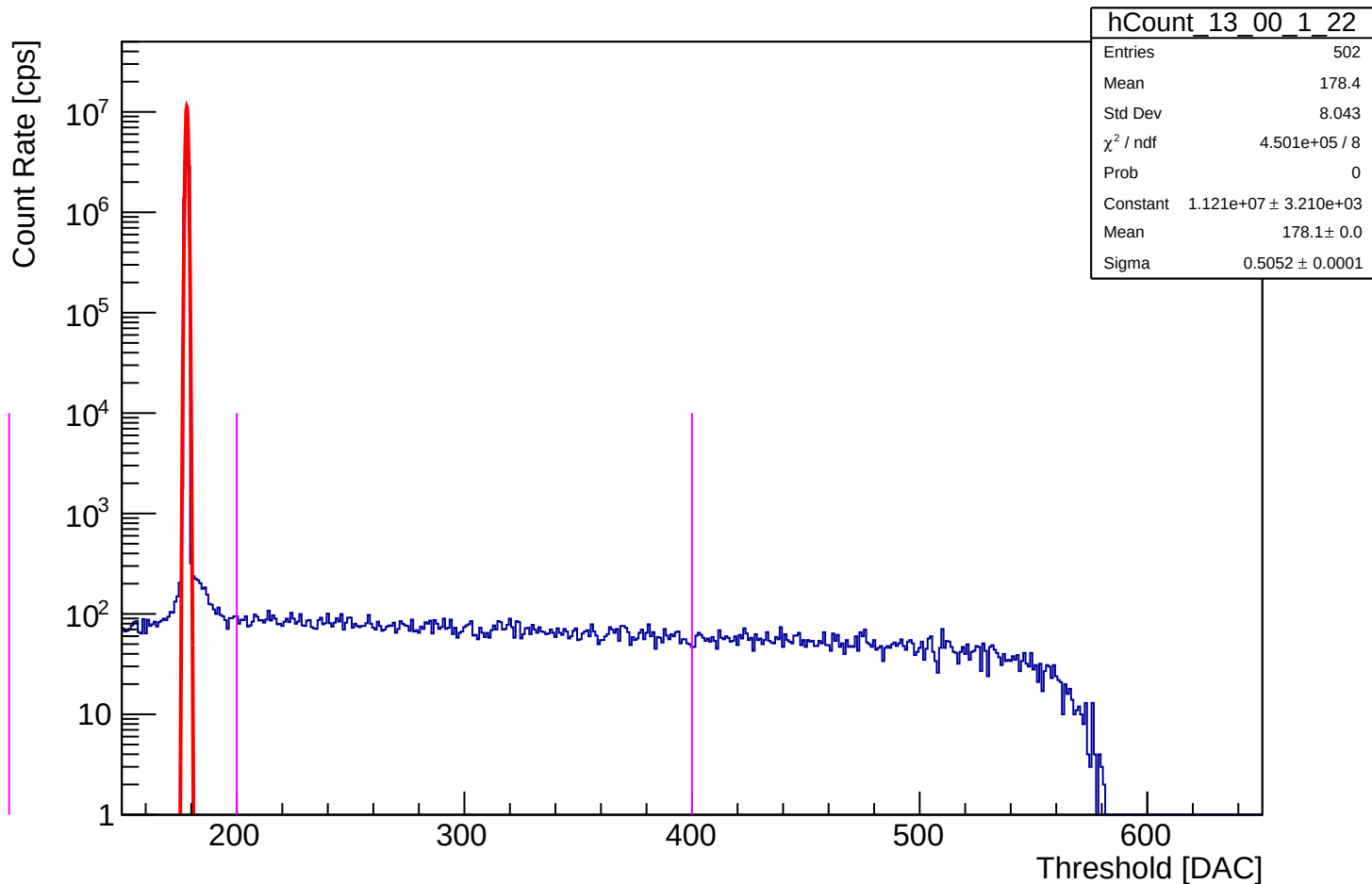
Row 1 Tile 1 Pmt 2 Pixel 17 Slot 13 Fiber 0 Asic 1 Channel 23



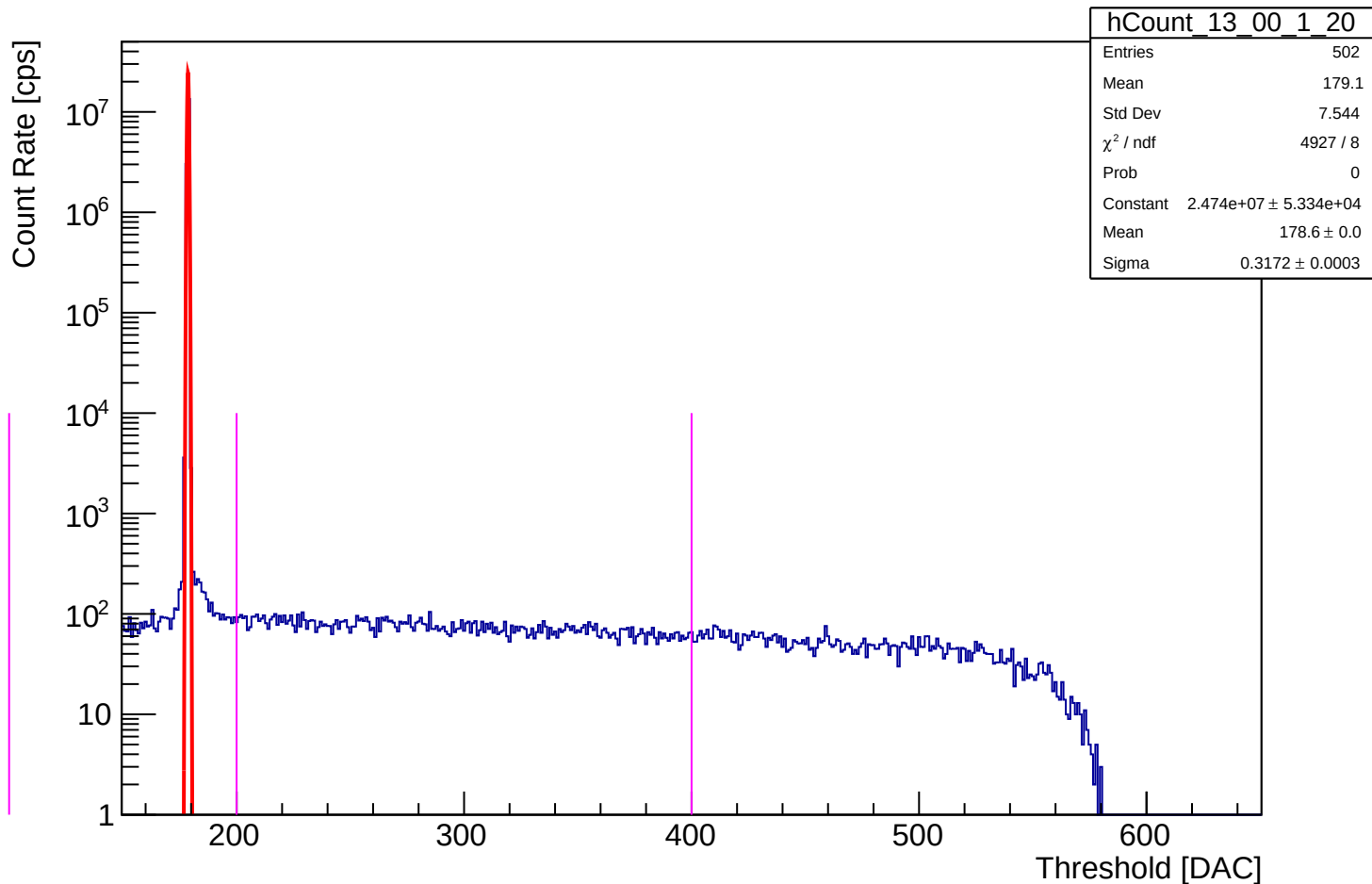
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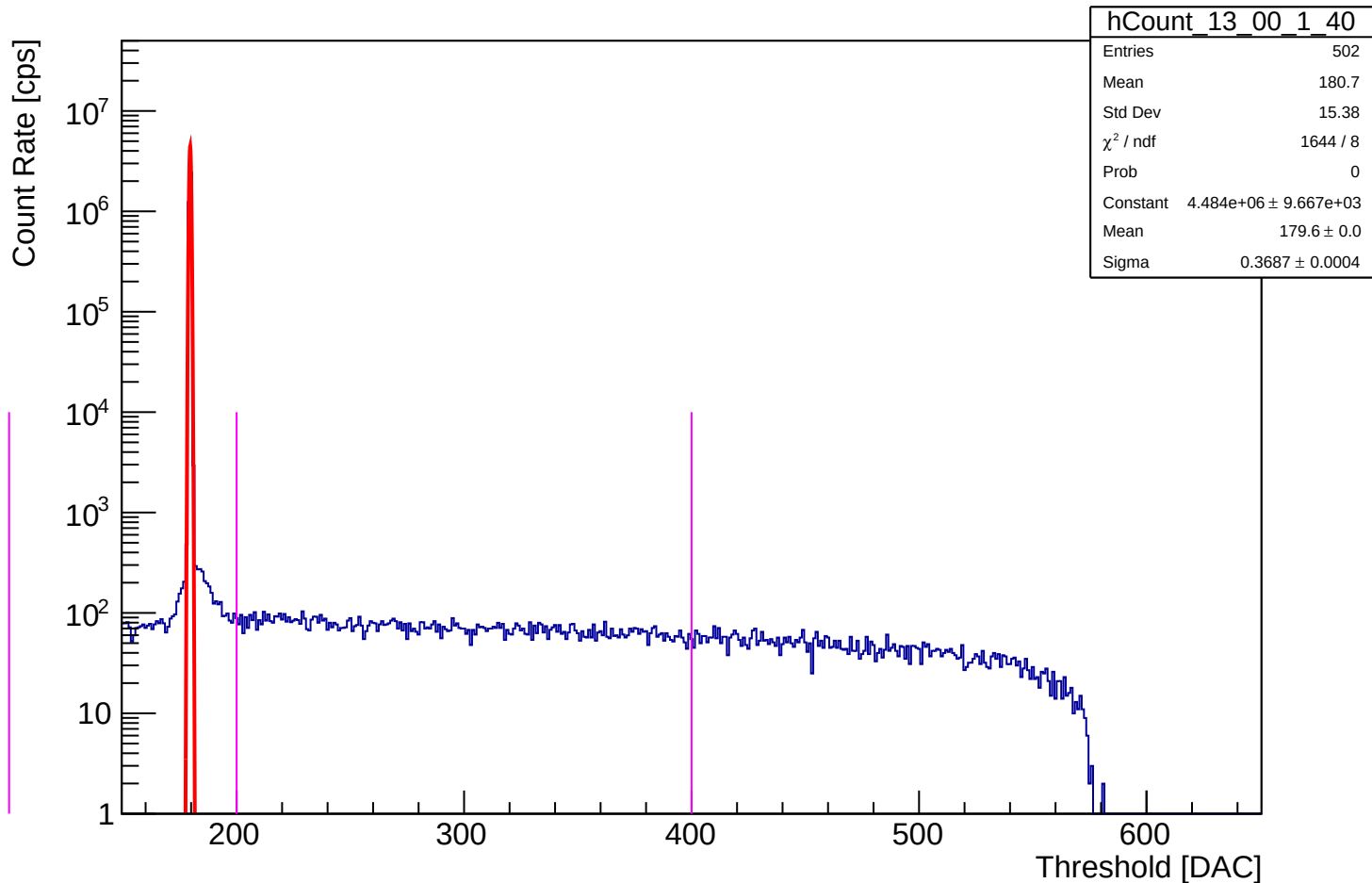
Row 1 Tile 1 Pmt 2 Pixel 19 Slot 13 Fiber 0 Asic 1 Channel 22



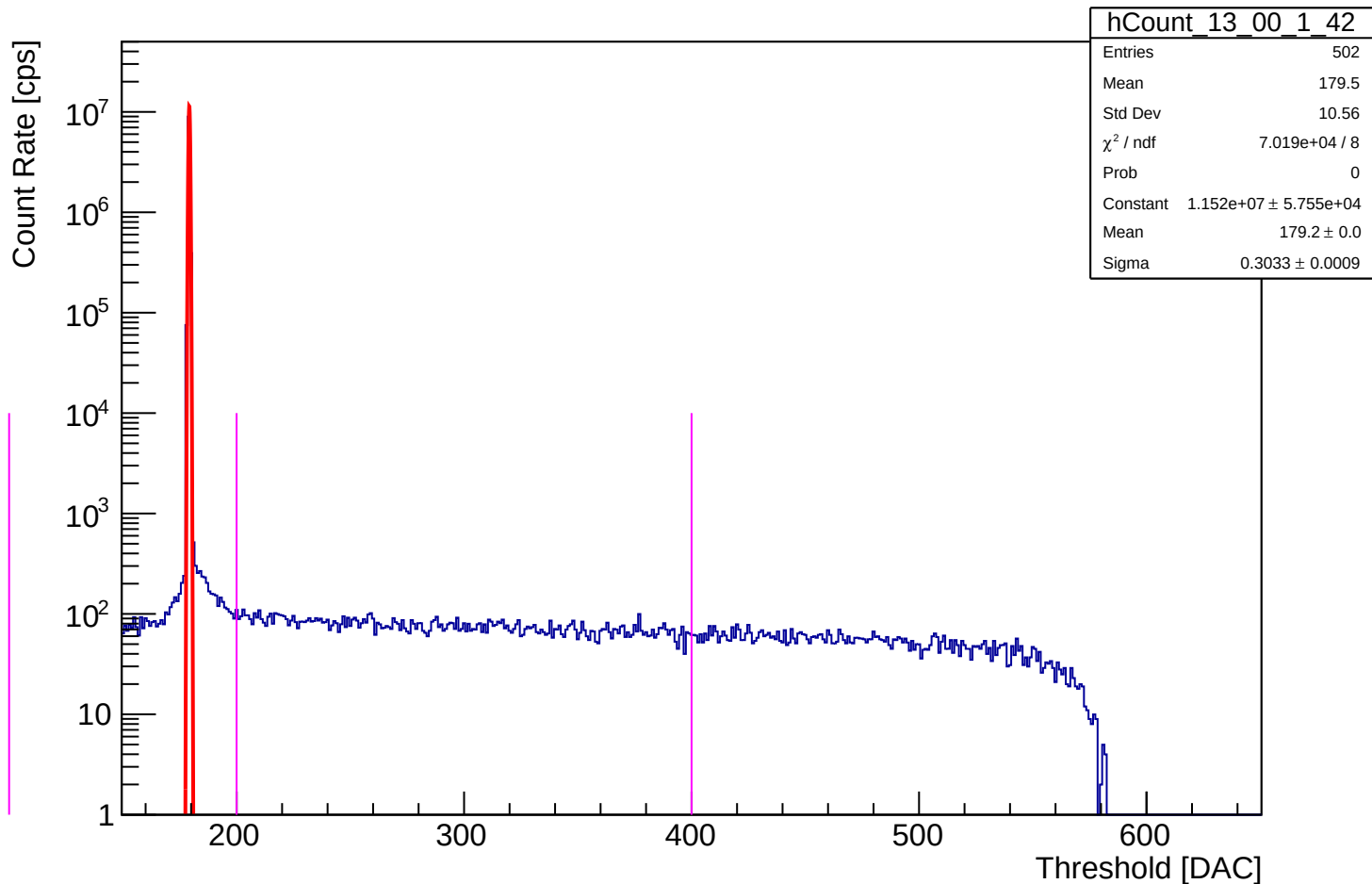
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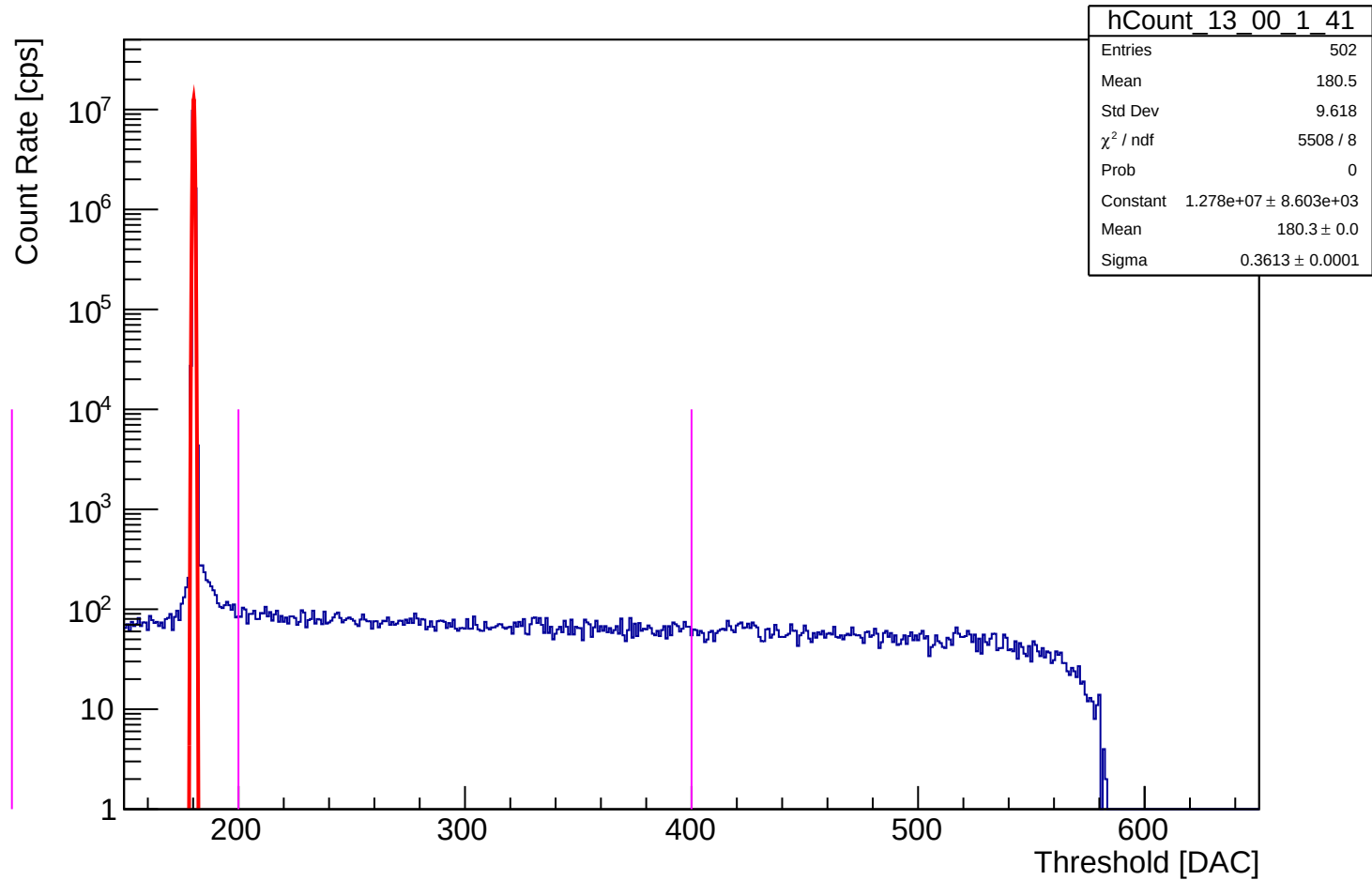


Row 1 Tile 1 Pmt 2 Pixel 21 Slot 13 Fiber 0 Asic 1 Channel 40

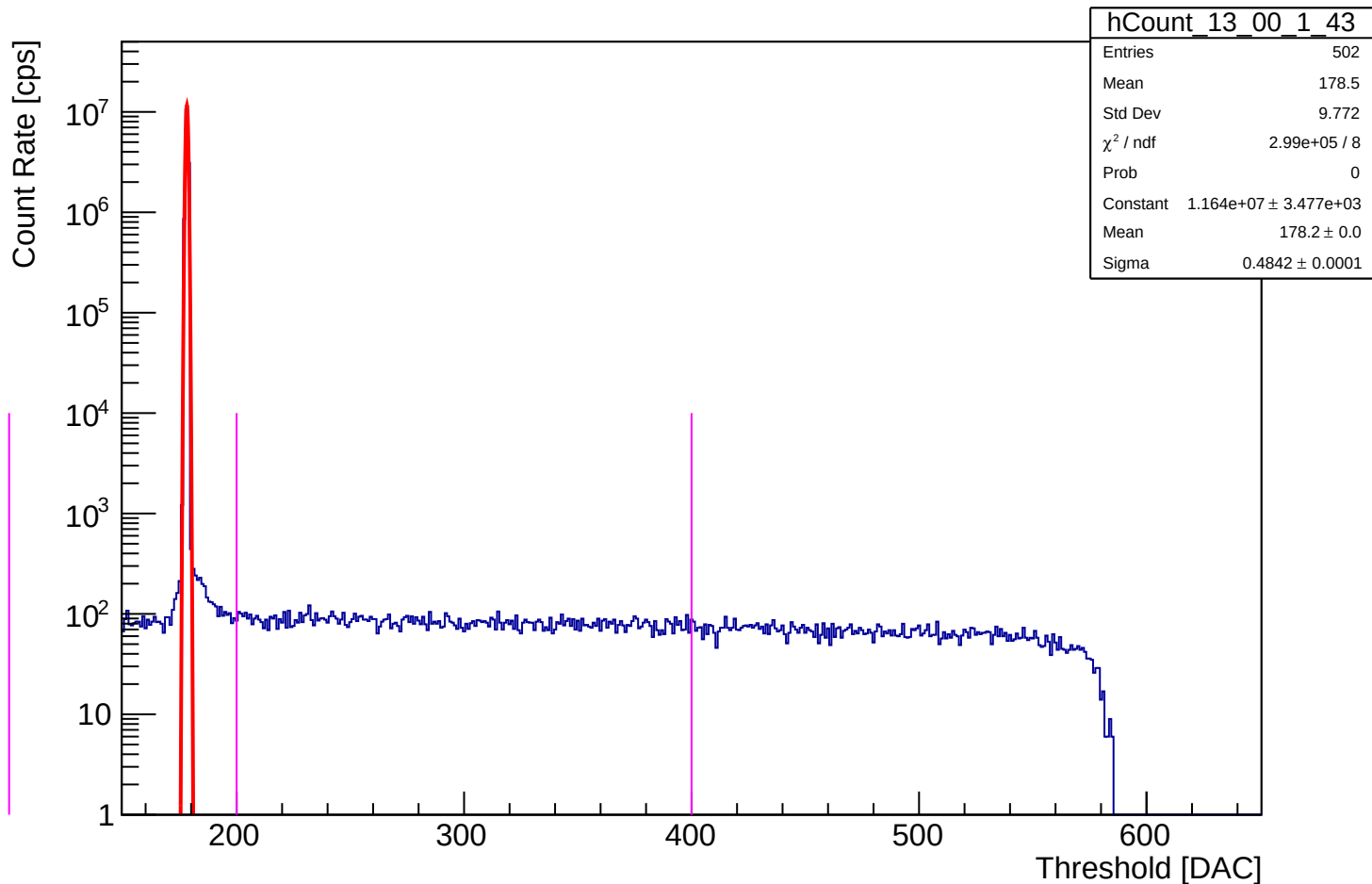


Row 1 Tile 1 Pmt 2 Pixel 22 Slot 13 Fiber 0 Asic 1 Channel 42

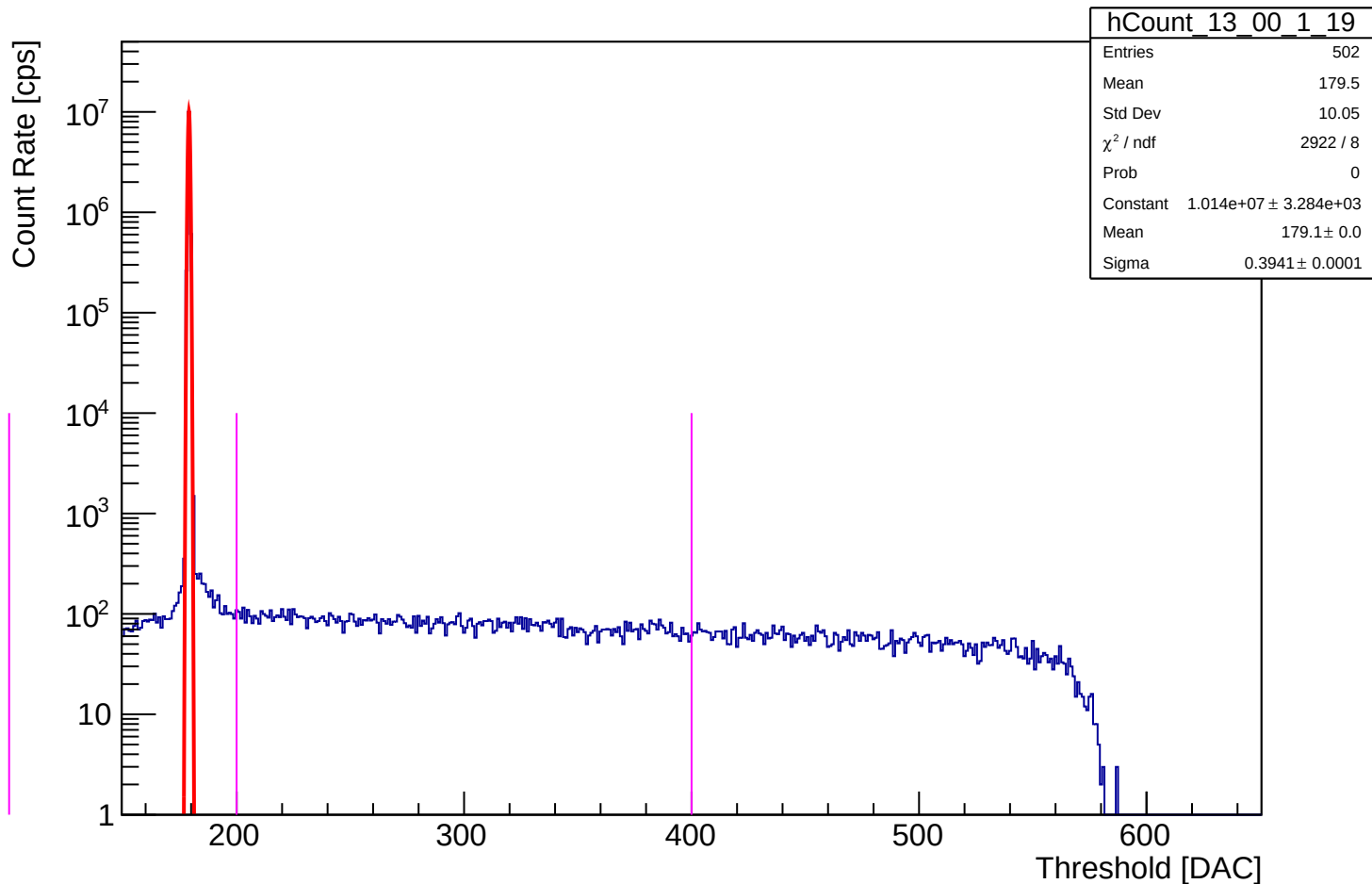




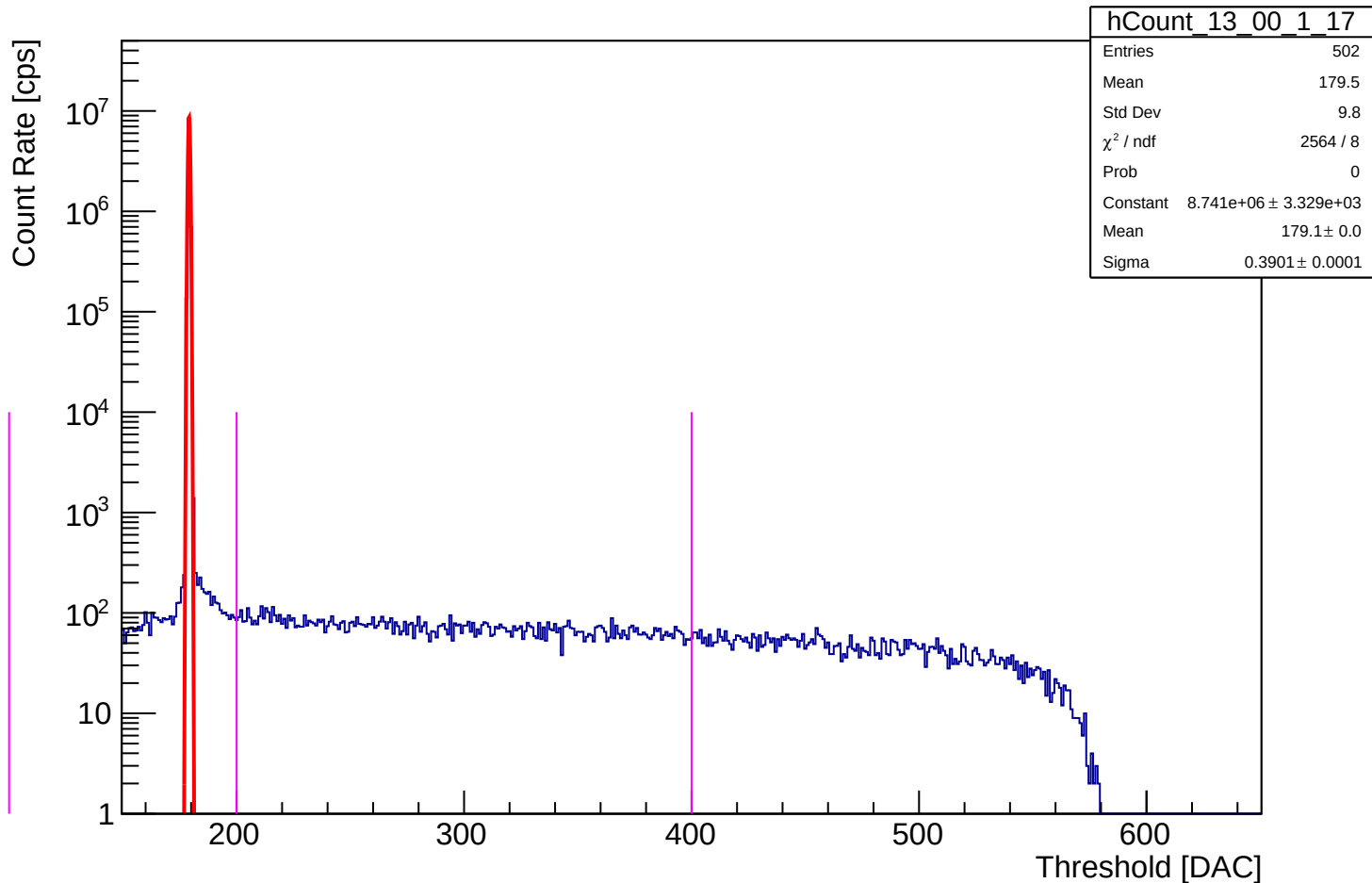
Row 1 Tile 1 Pmt 2 Pixel 24 Slot 13 Fiber 0 Asic 1 Channel 43



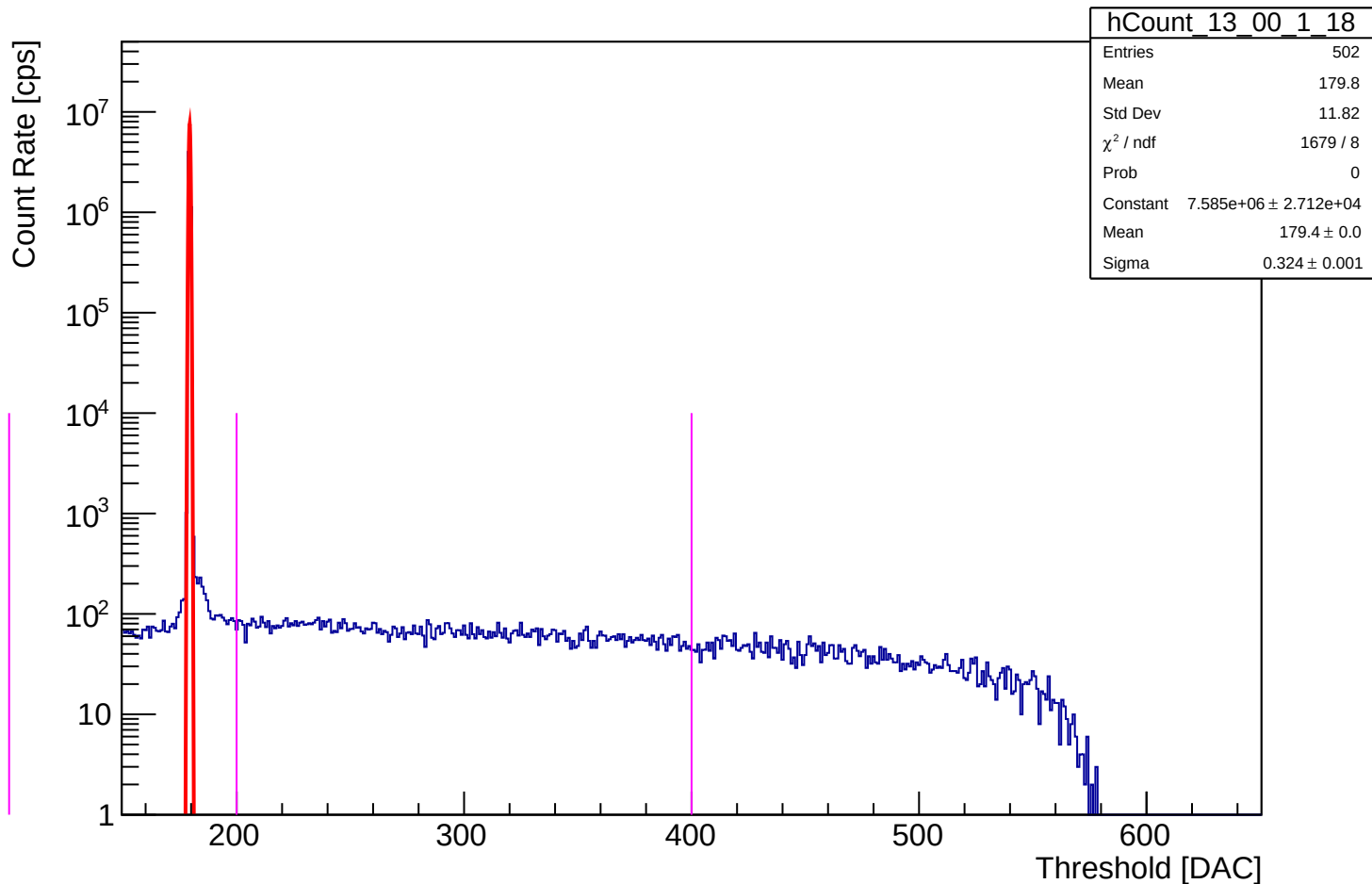
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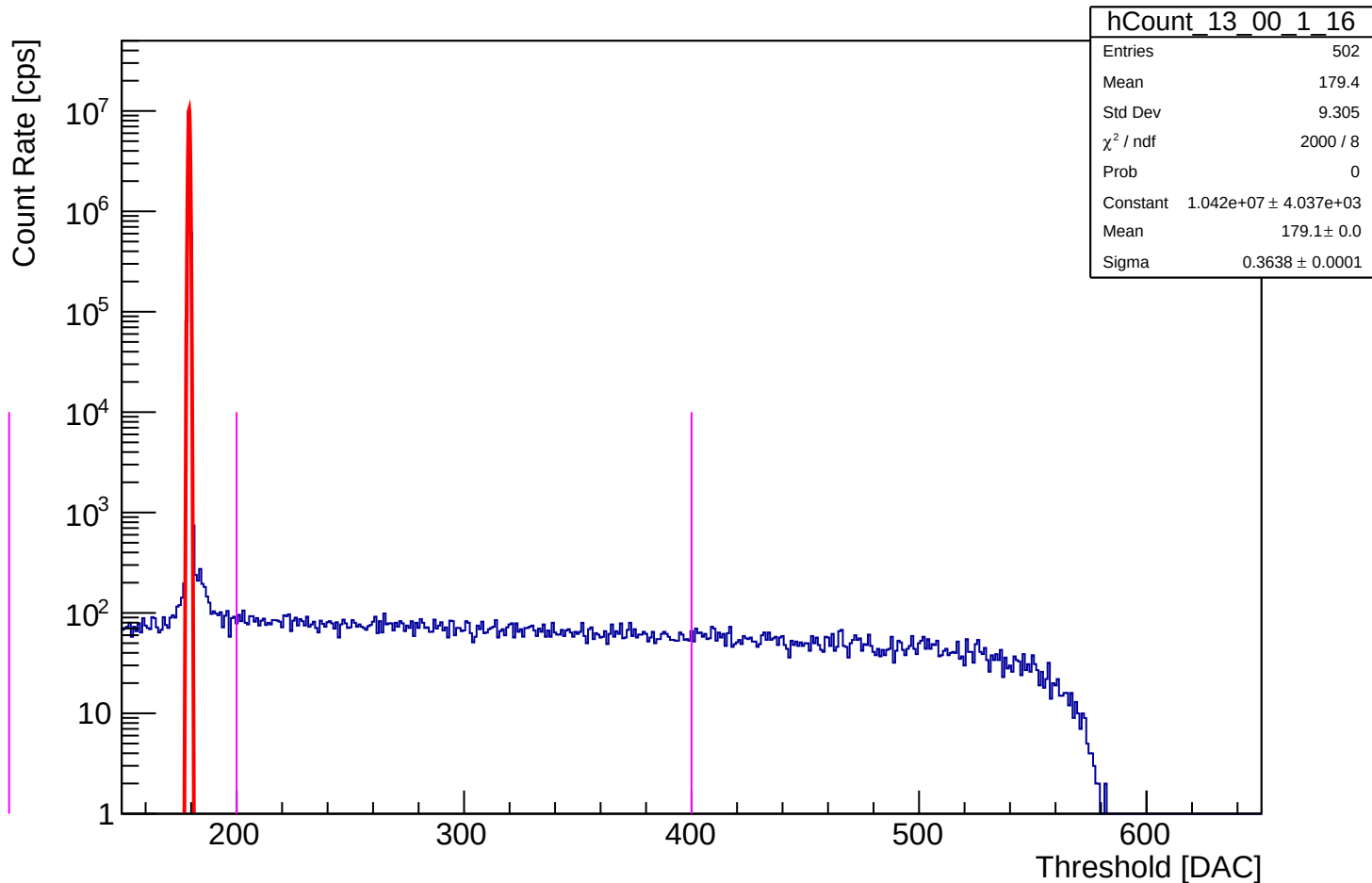
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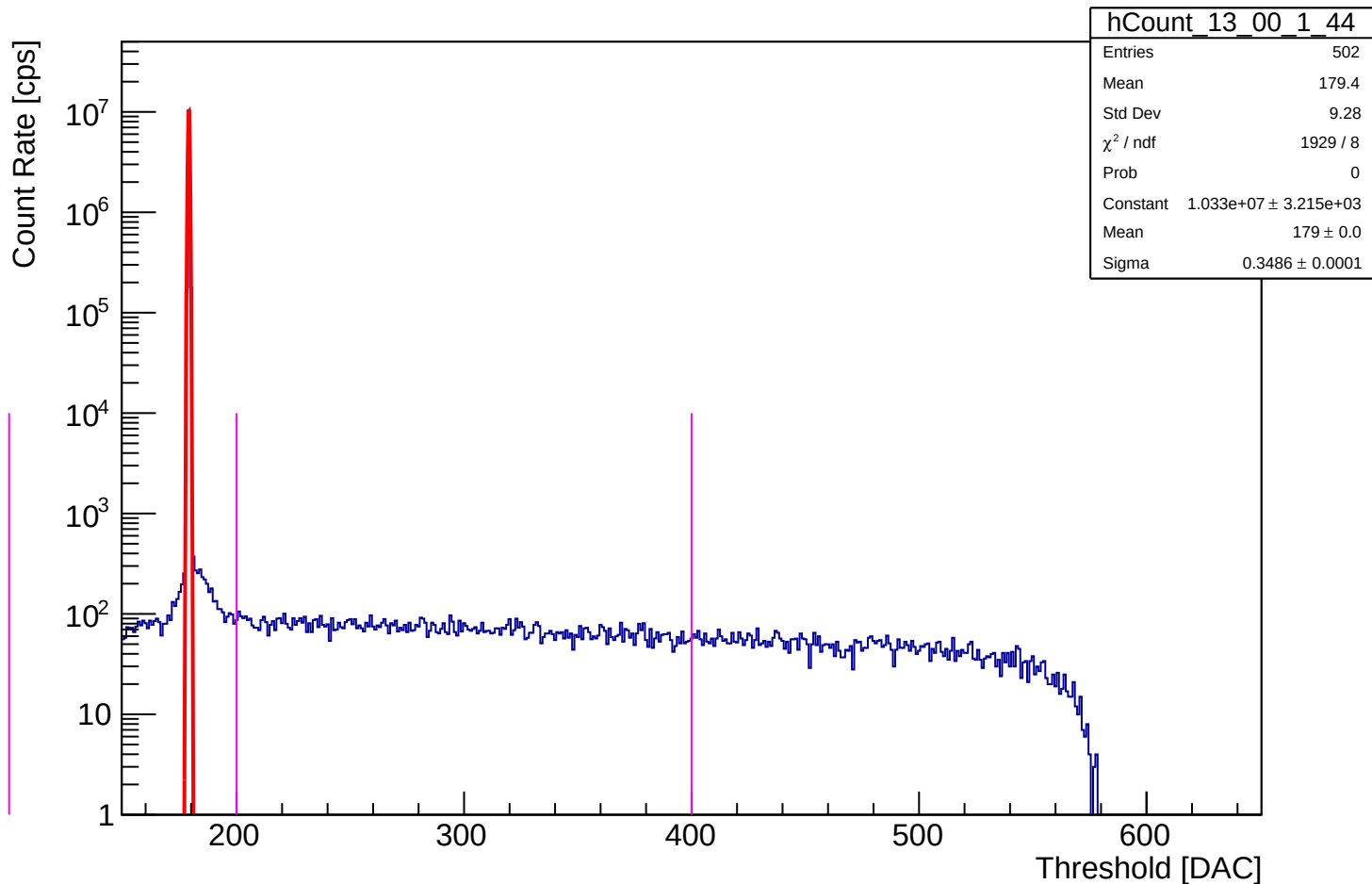
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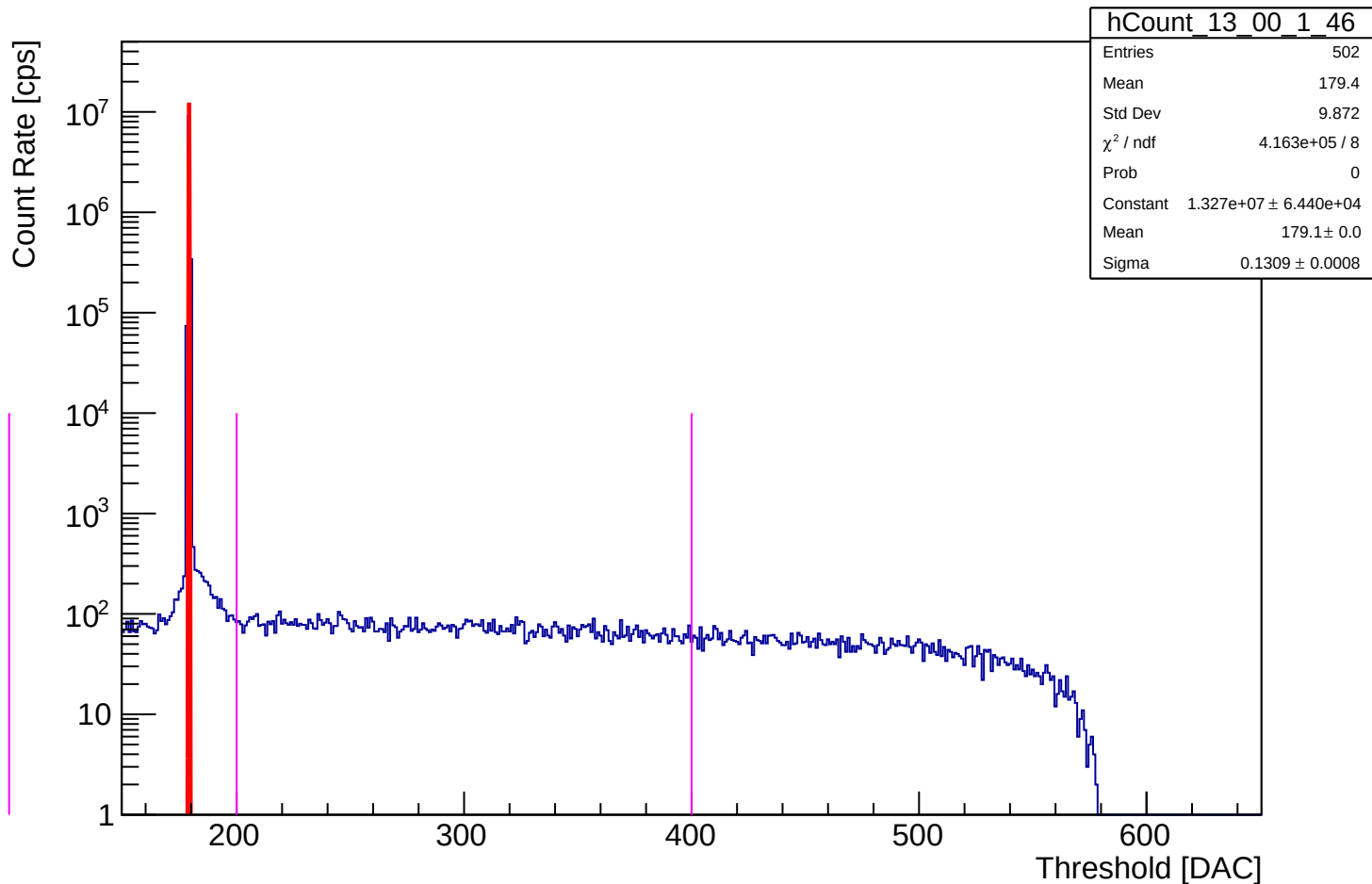
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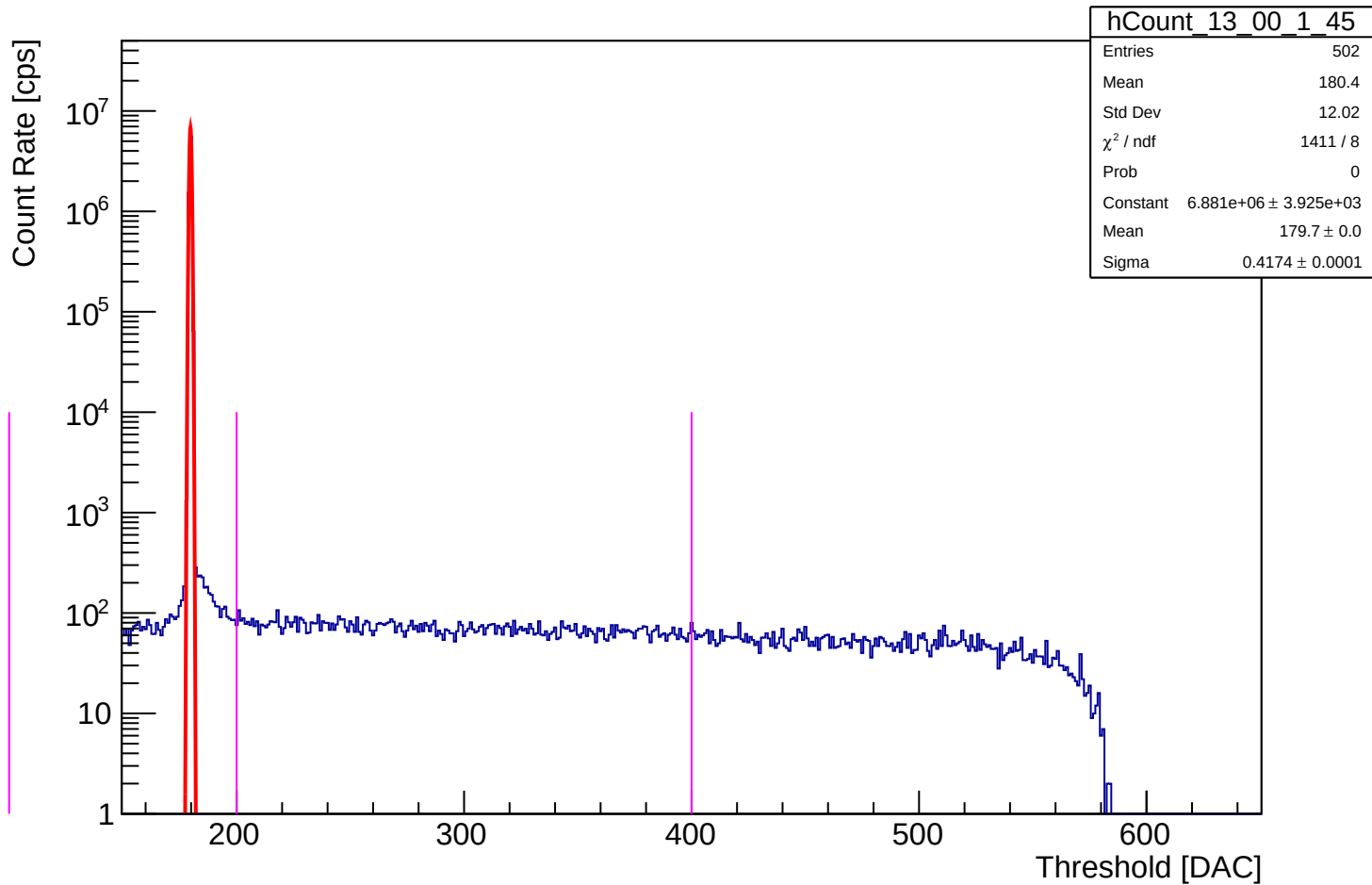
Row 1 Tile 1 Pmt 2 Pixel 29 Slot 13 Fiber 0 Asic 1 Channel 44



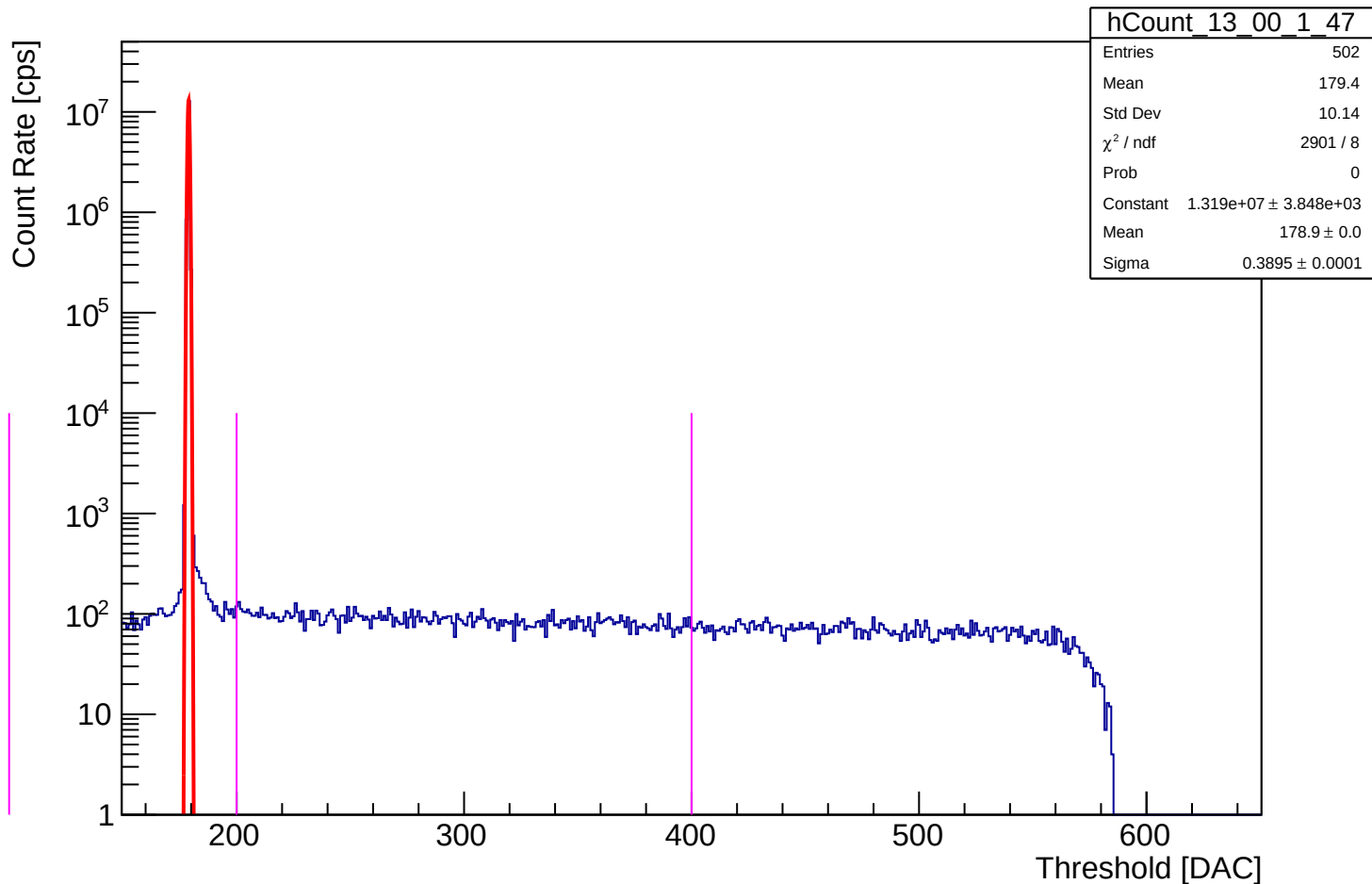
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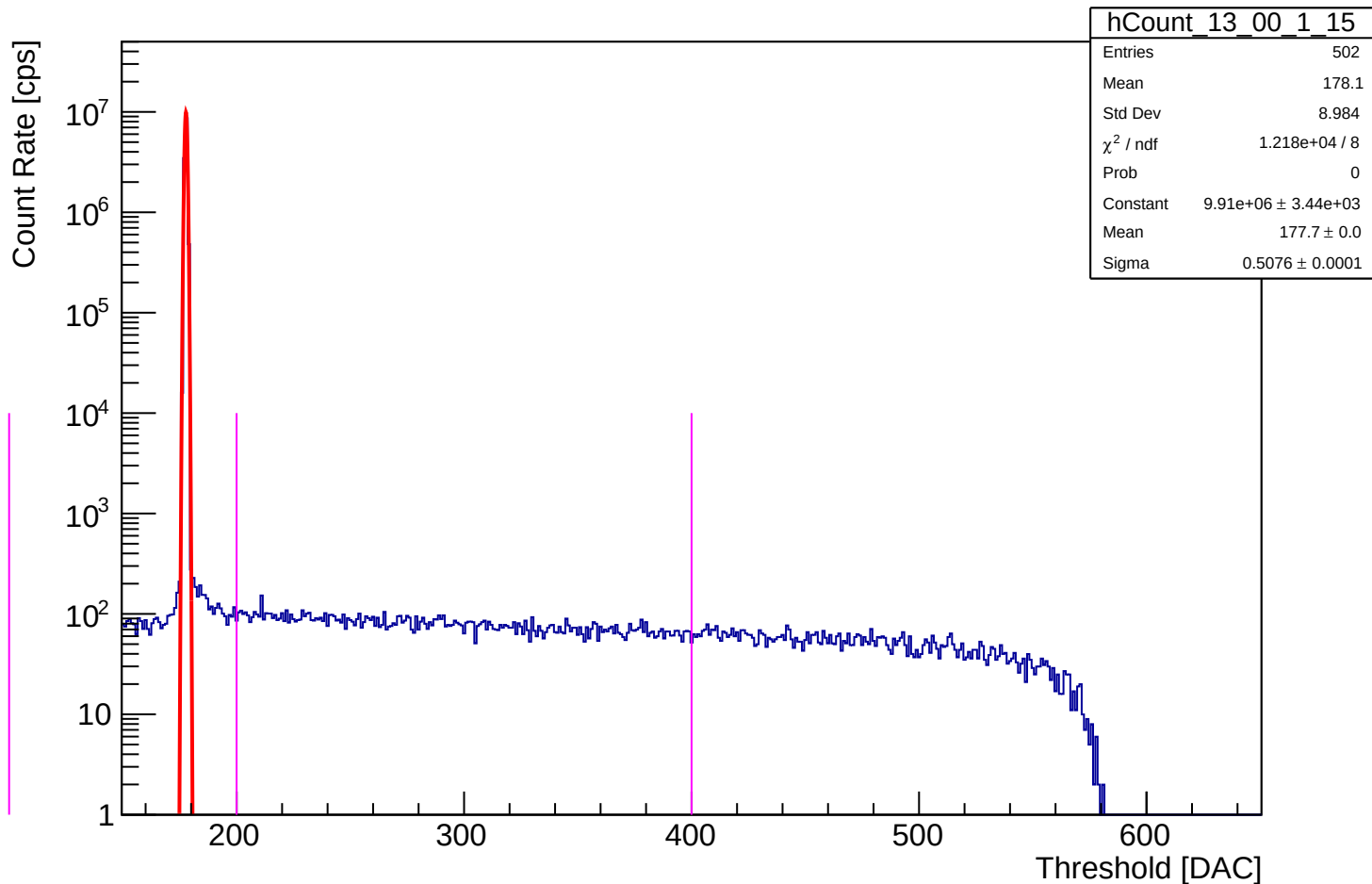
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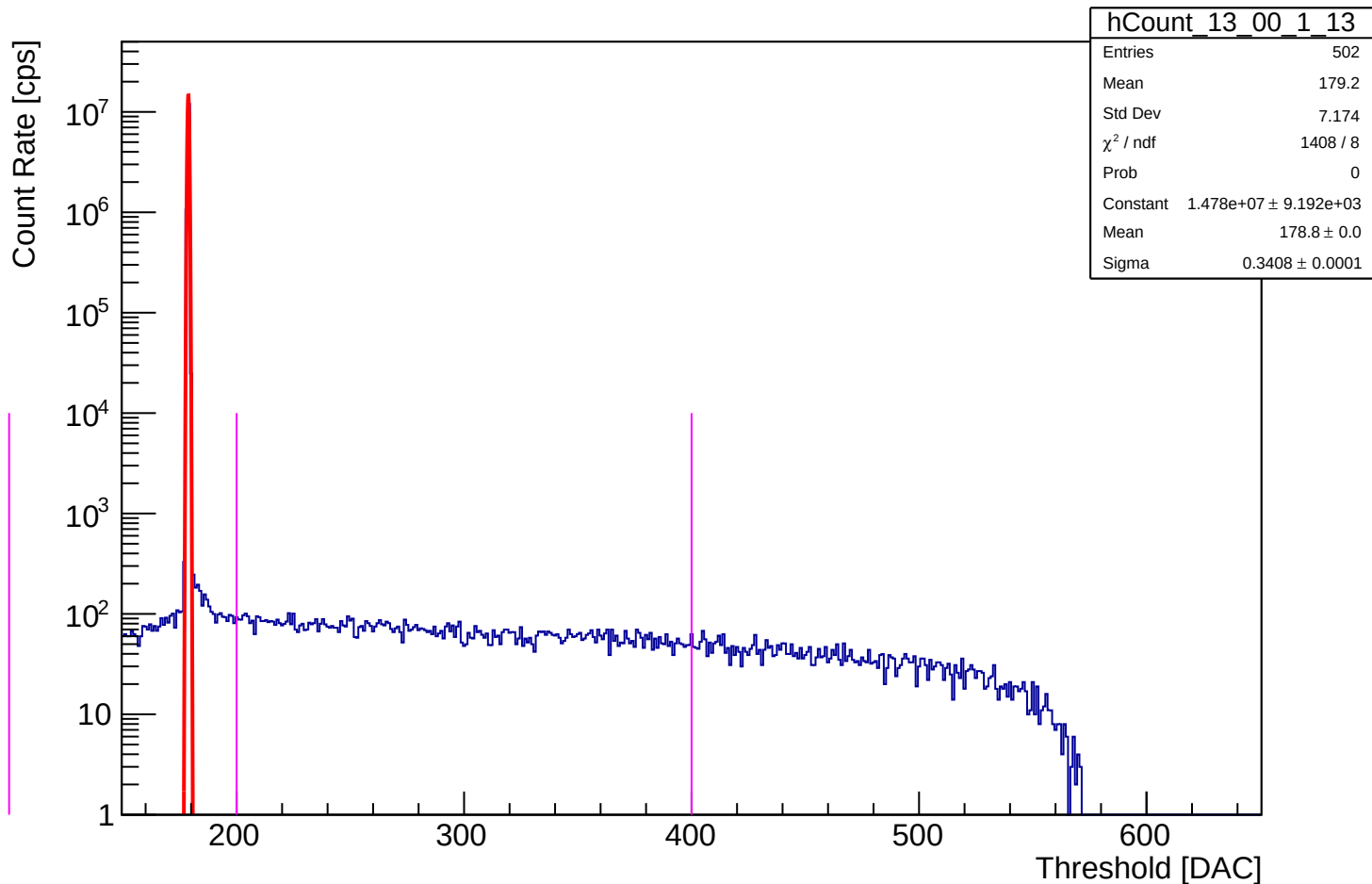
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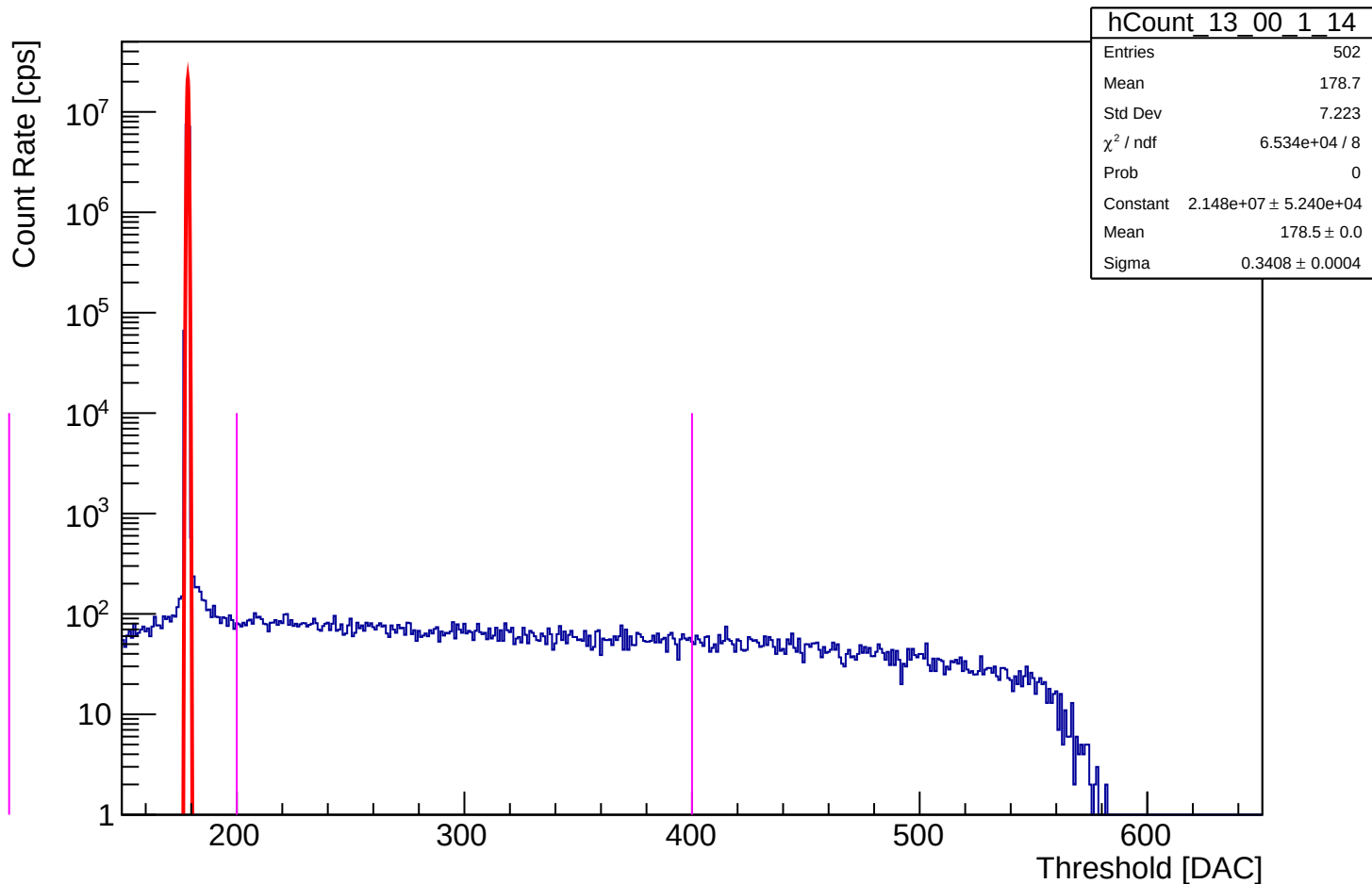
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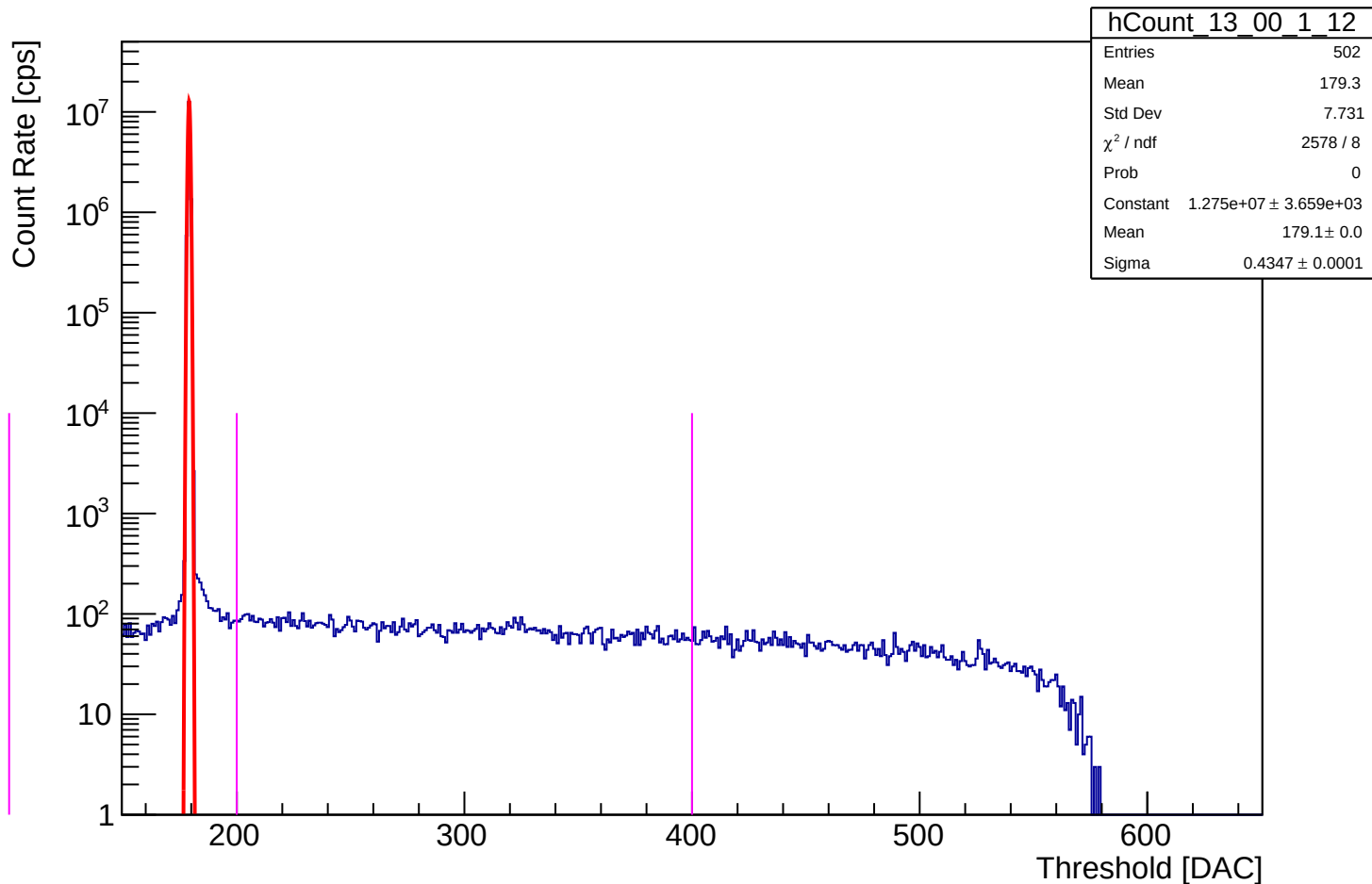
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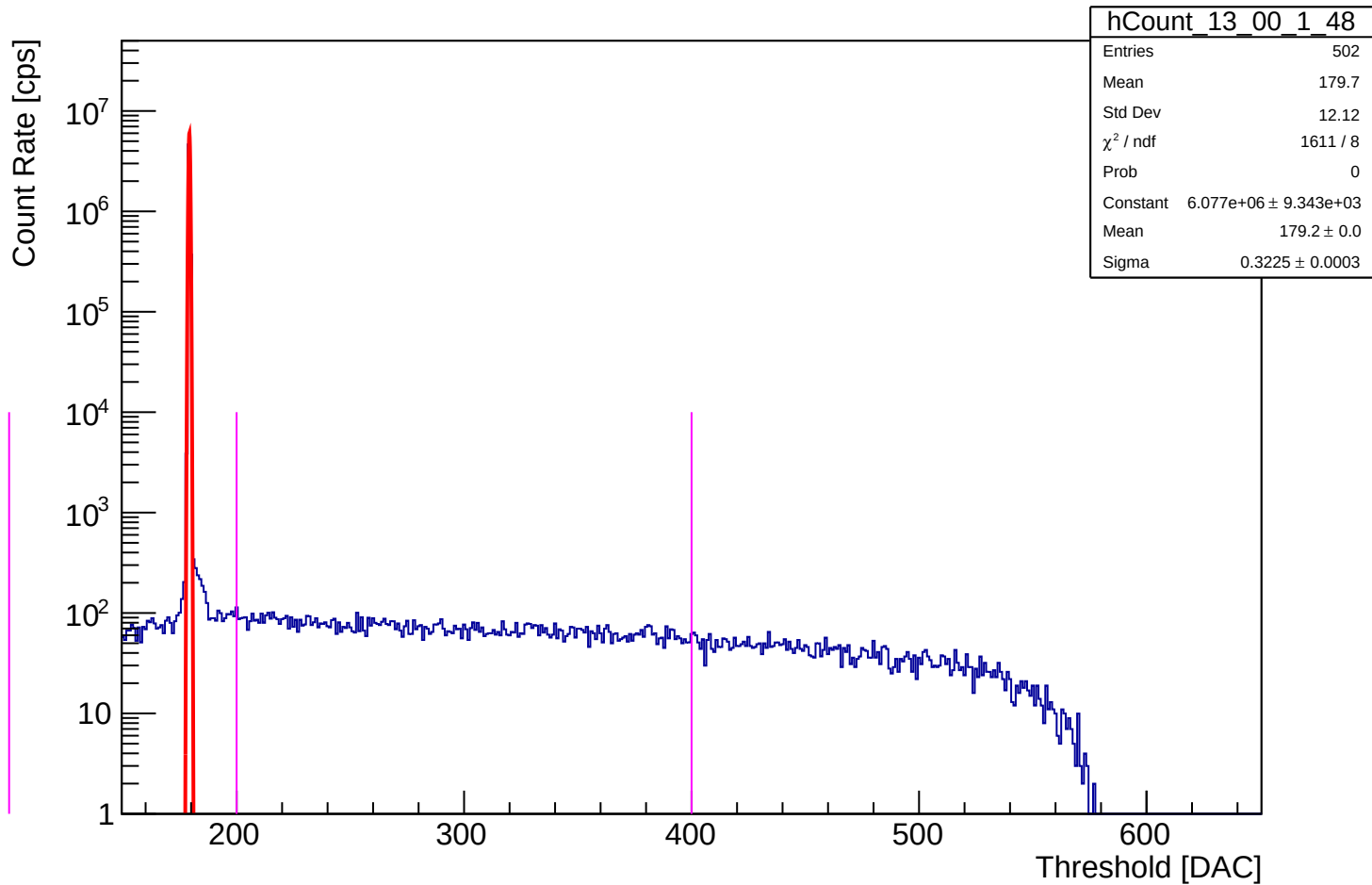
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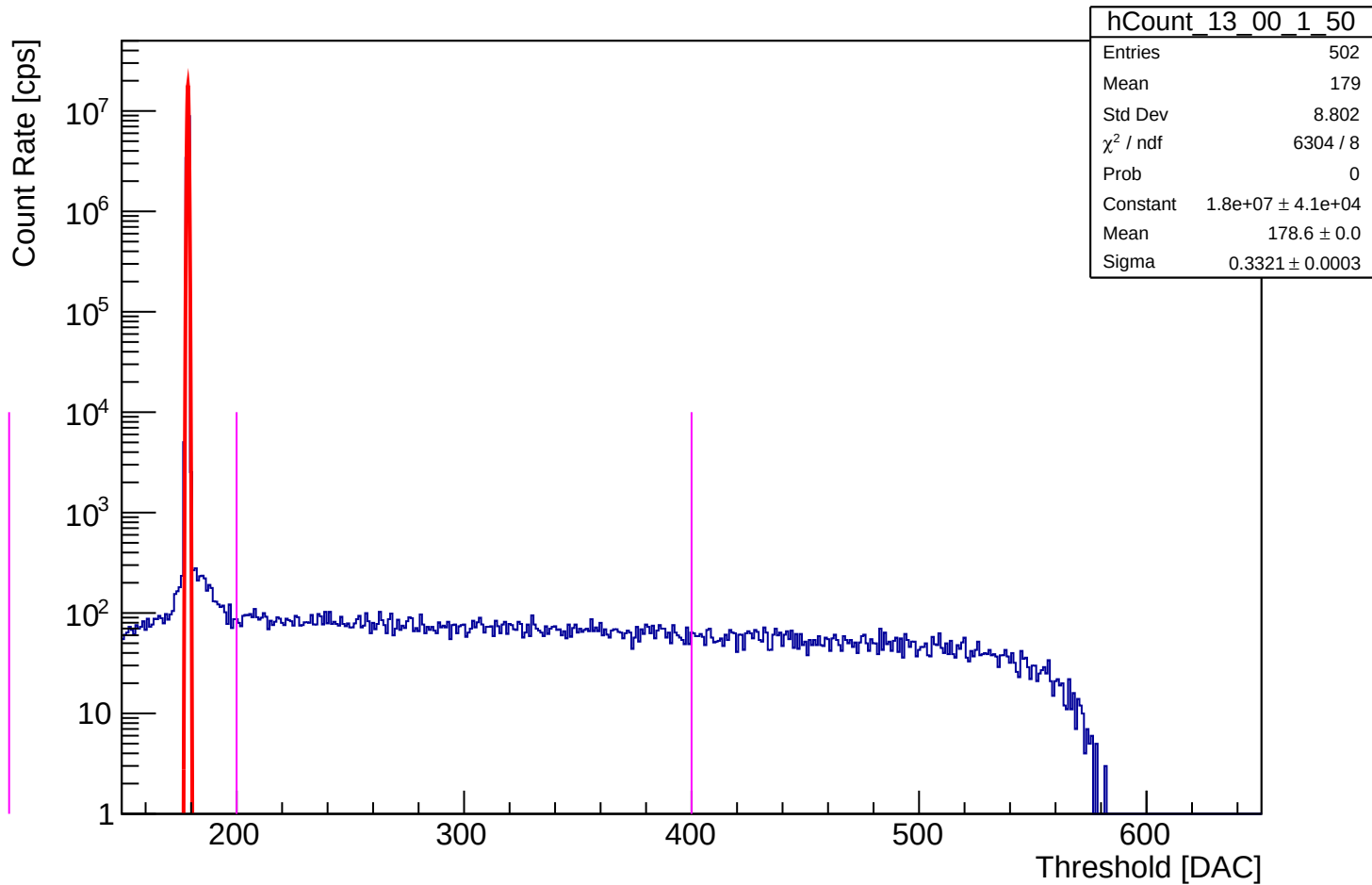
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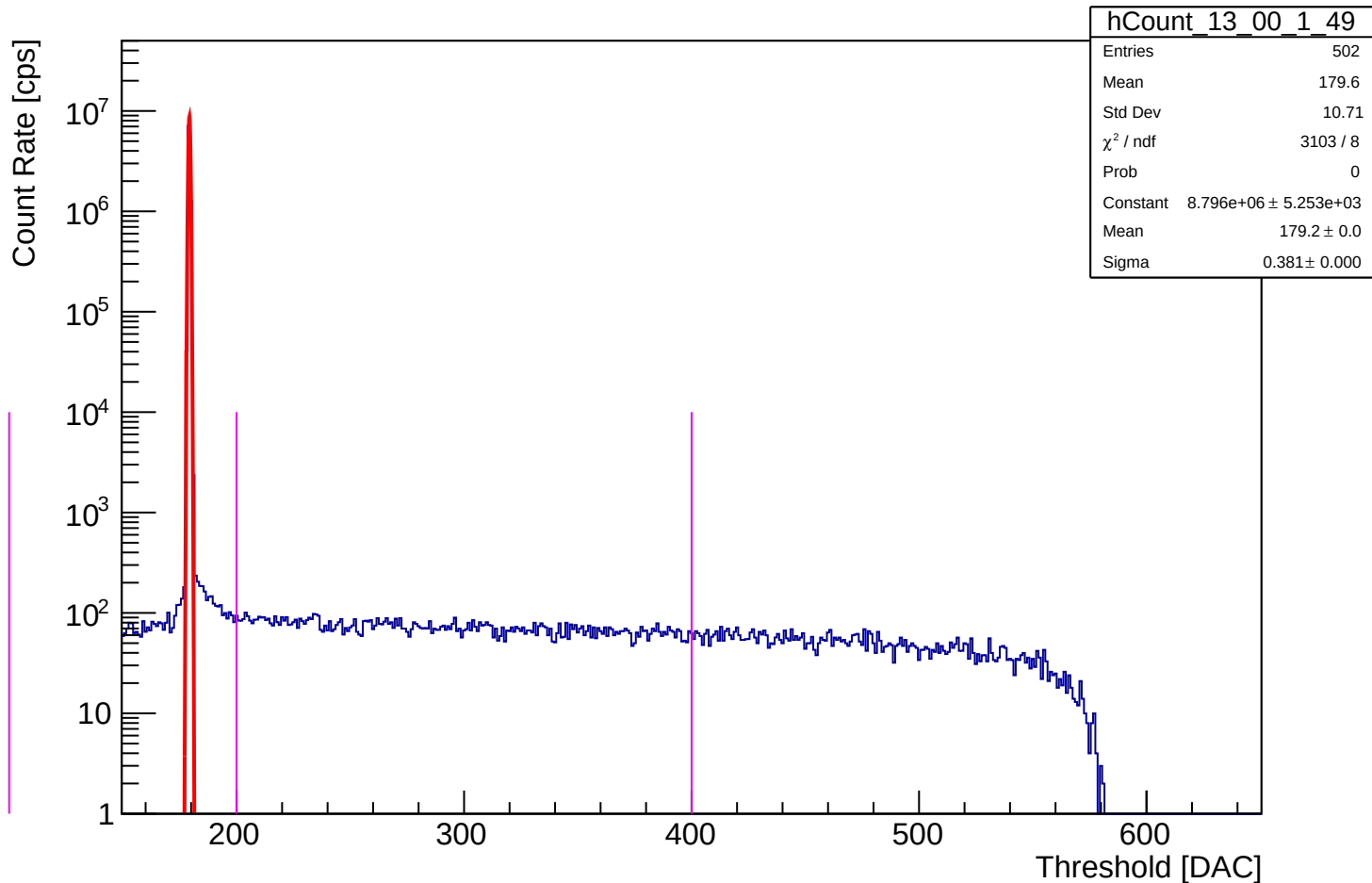
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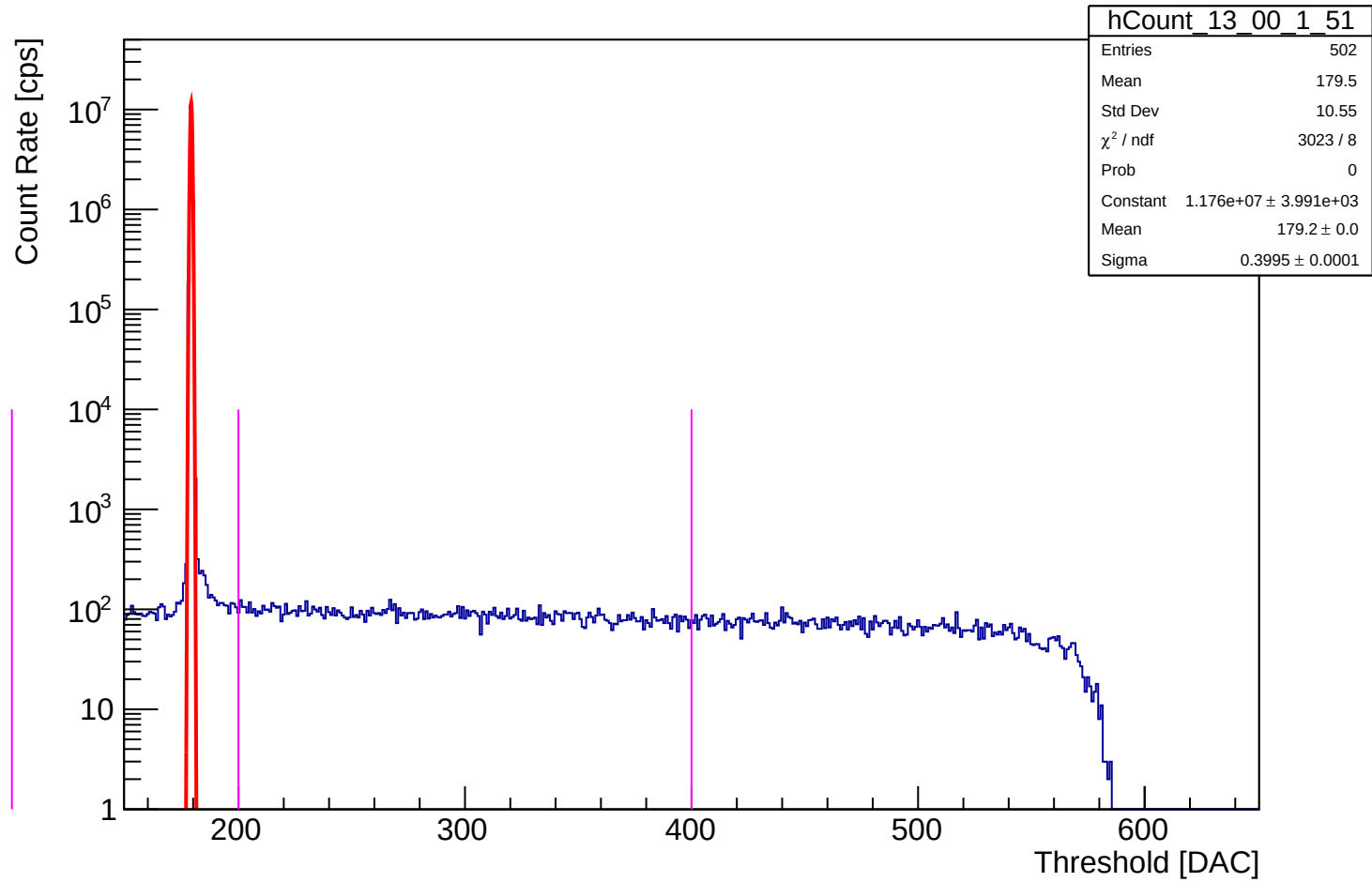


Row 1 Tile 1 Pmt 2 Pixel 38 Slot 13 Fiber 0 Asic 1 Channel 50

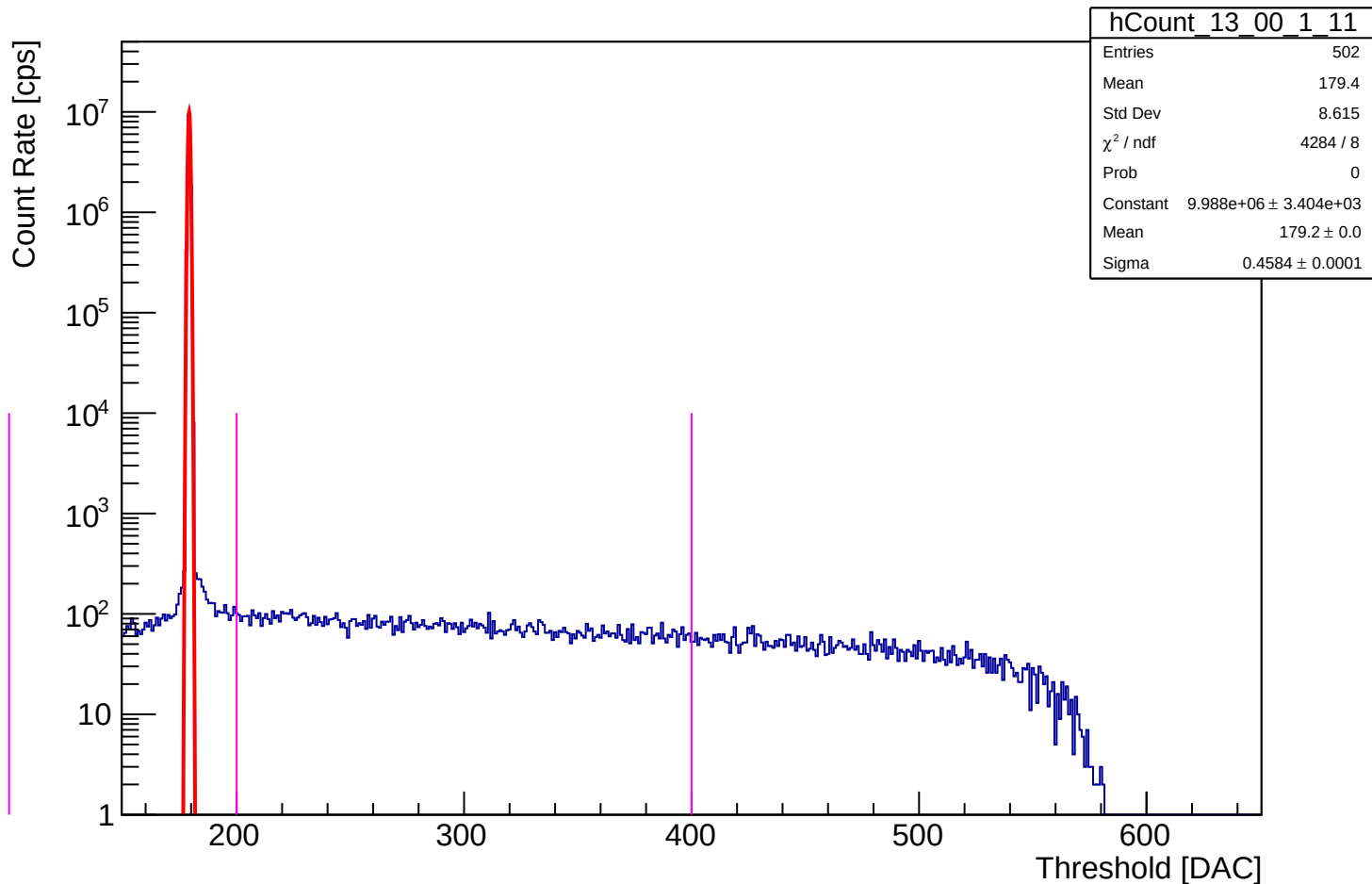


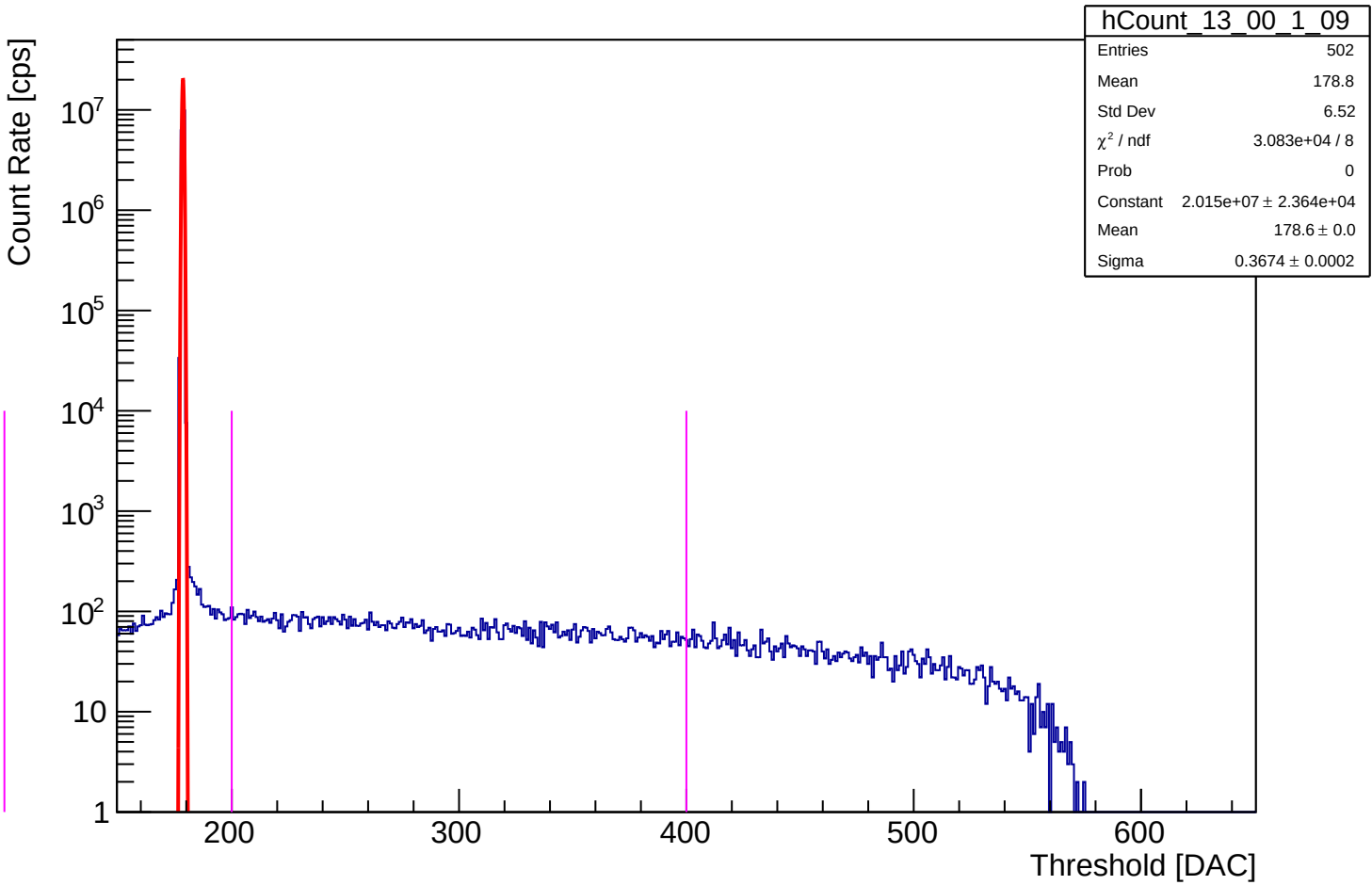
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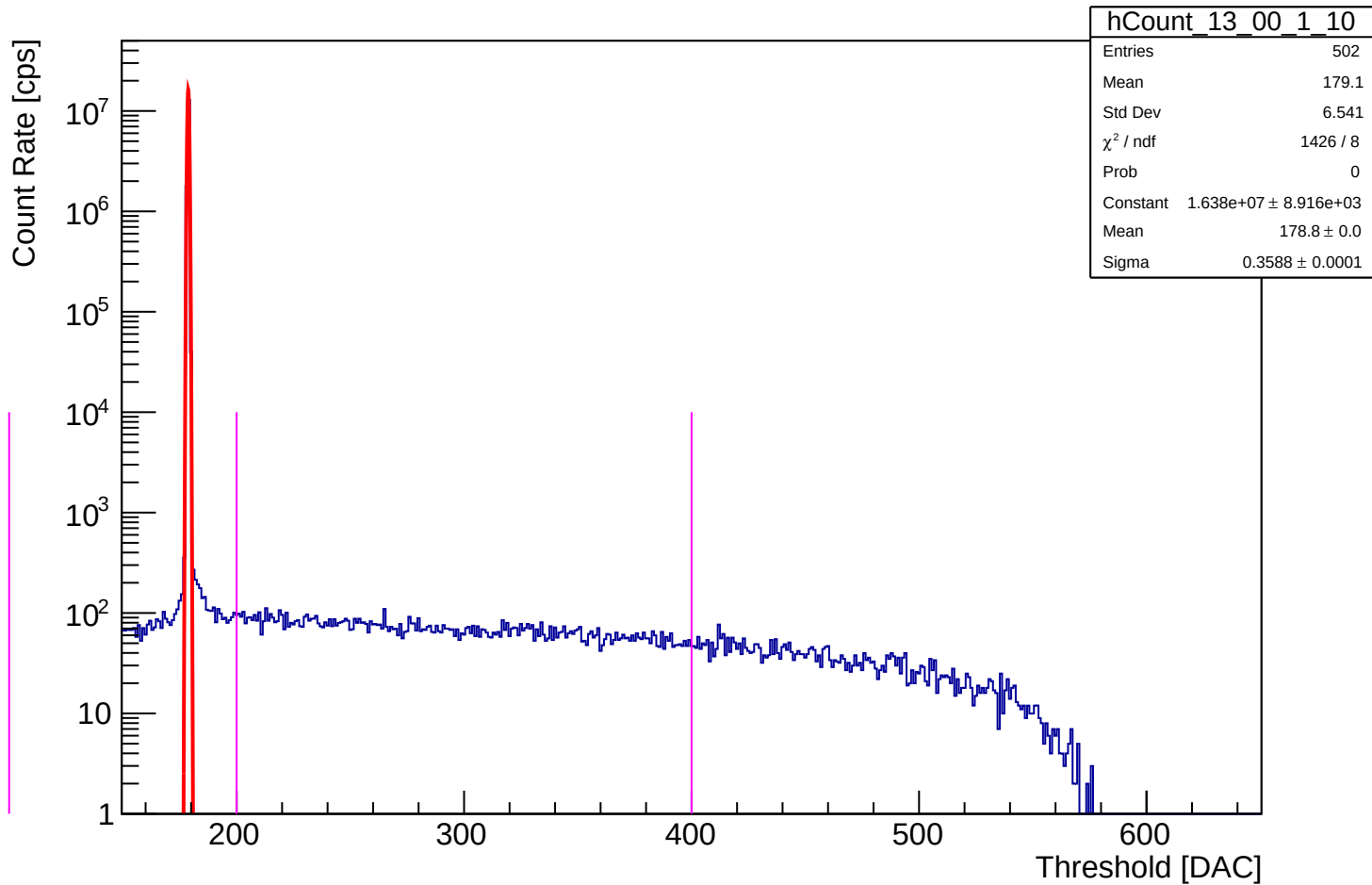


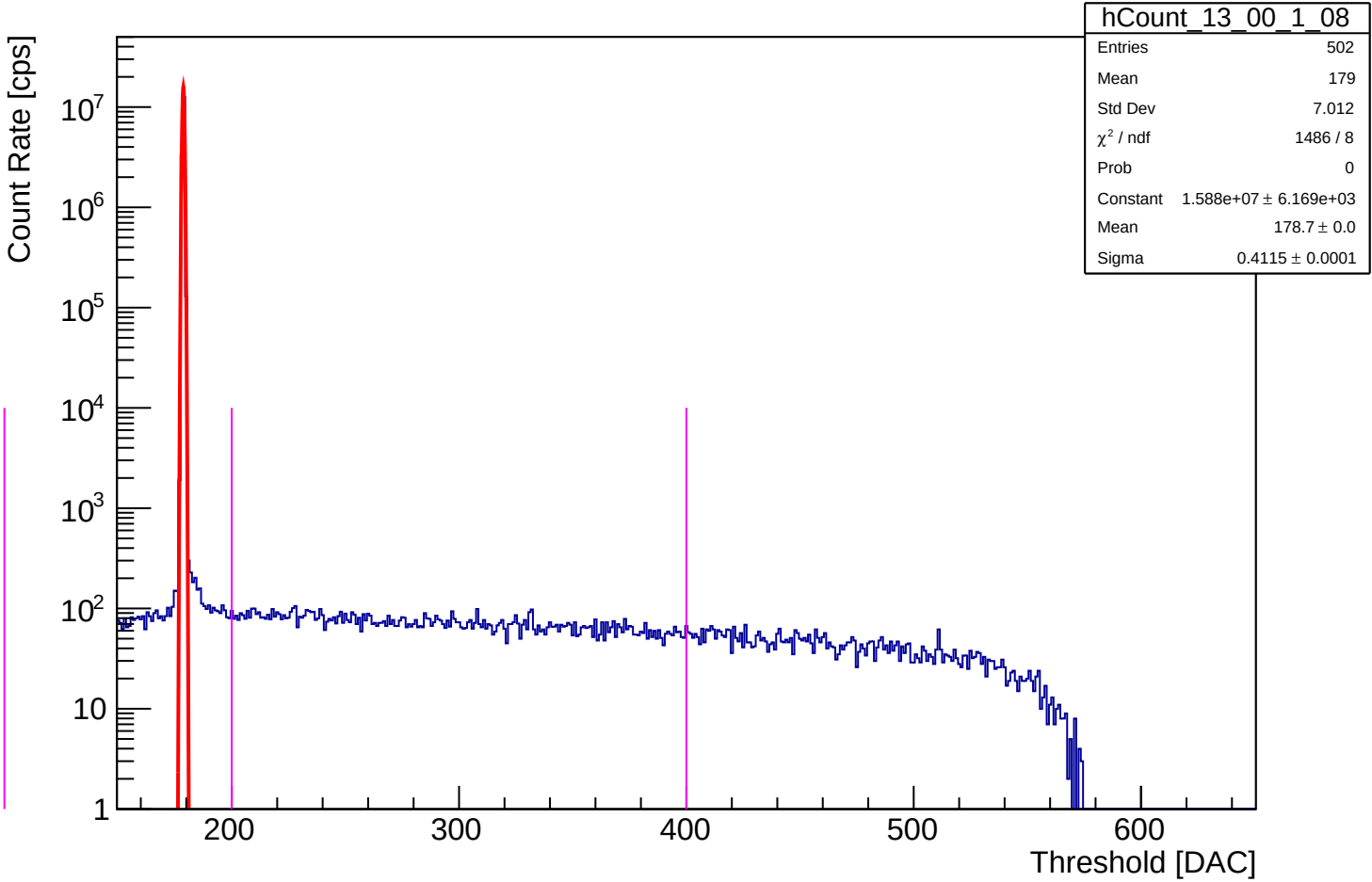
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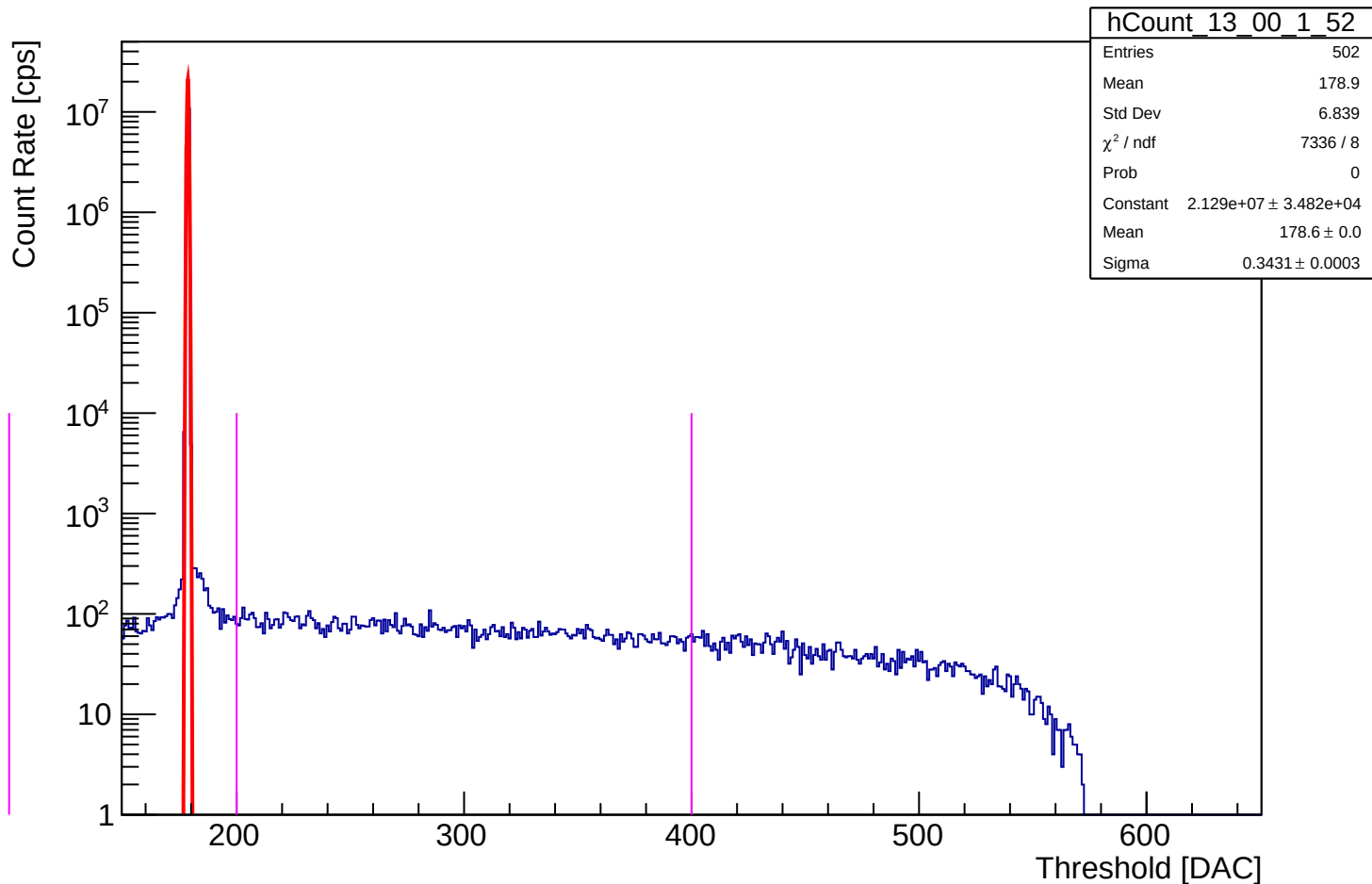


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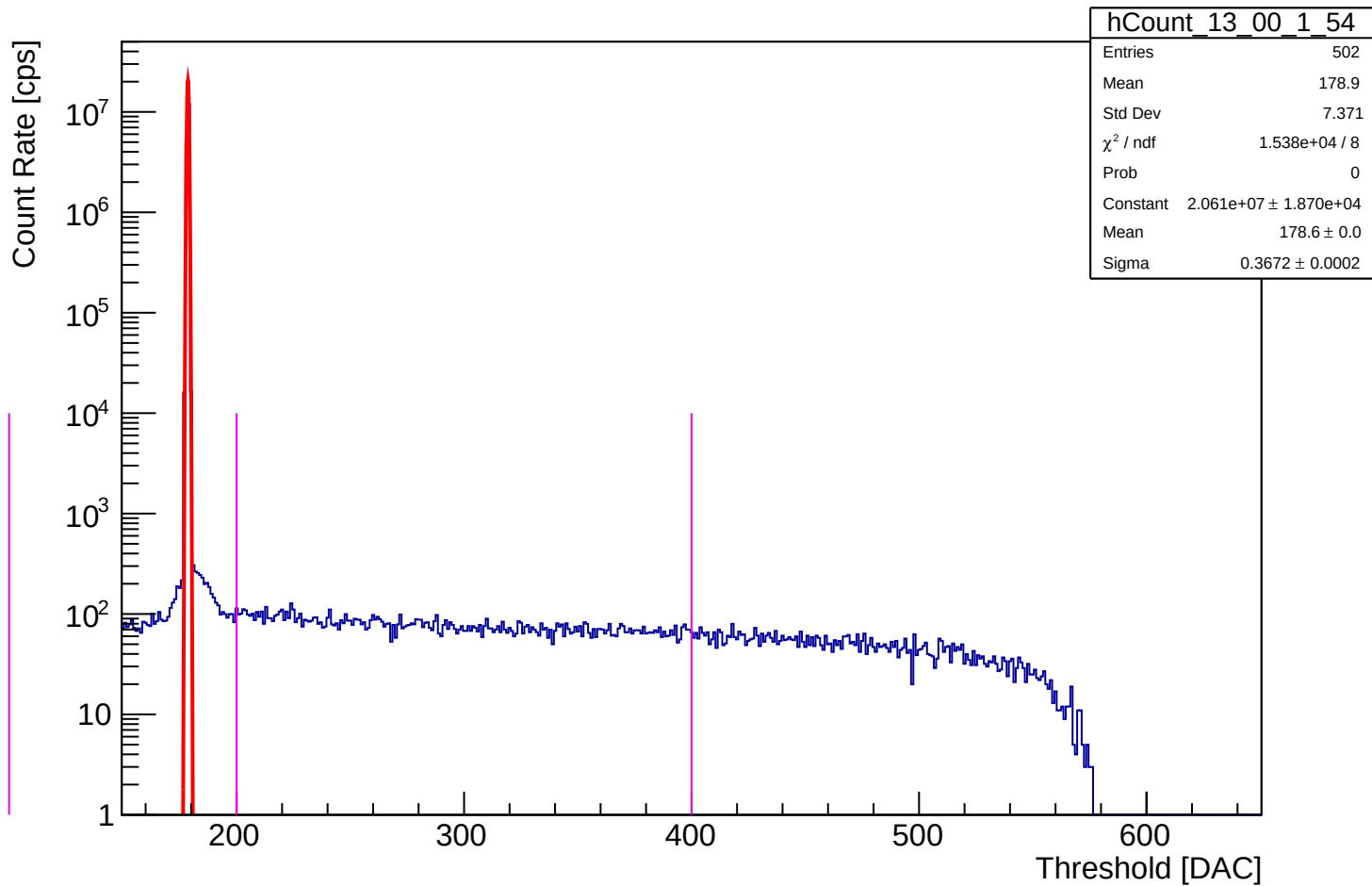




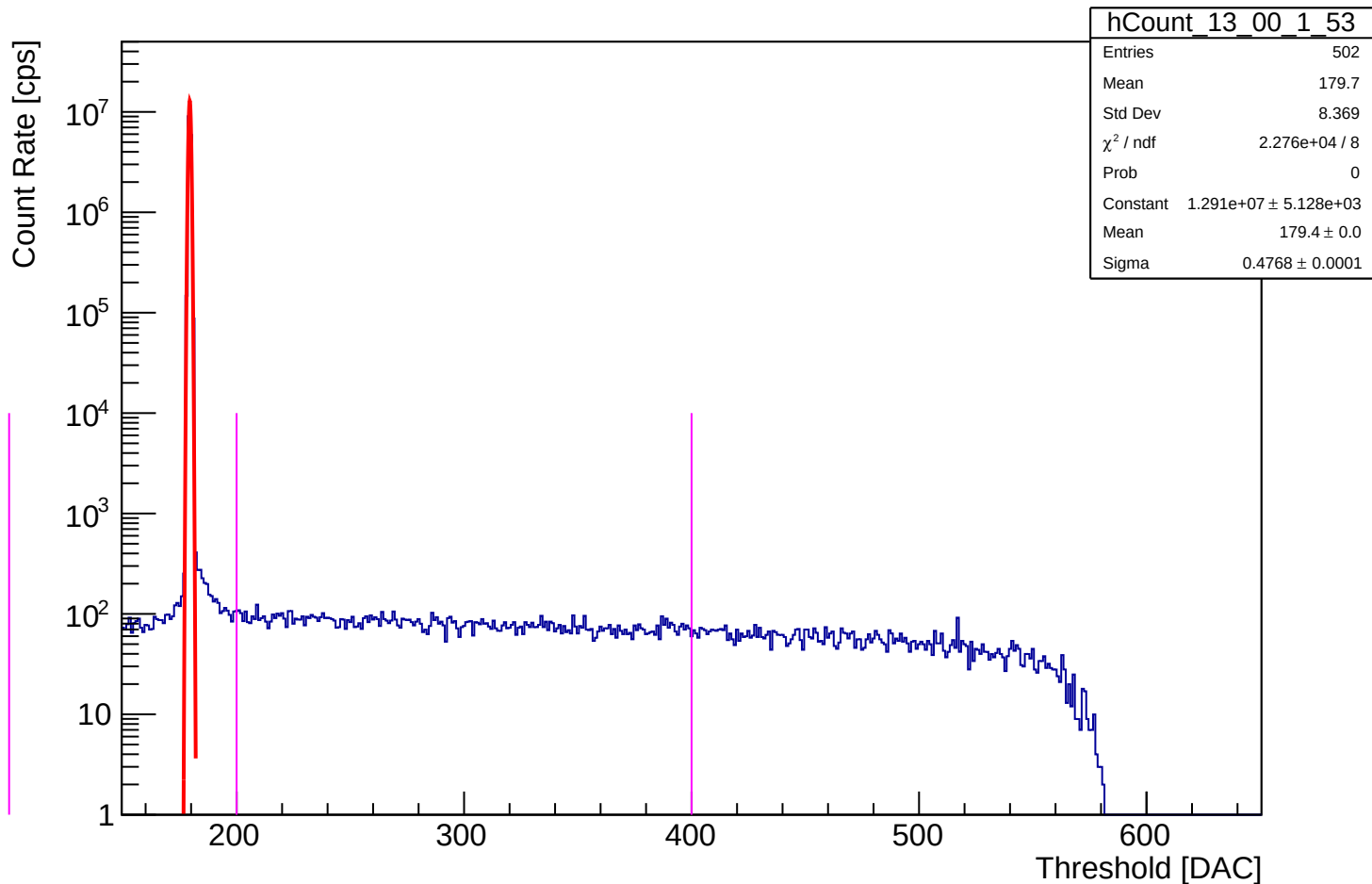
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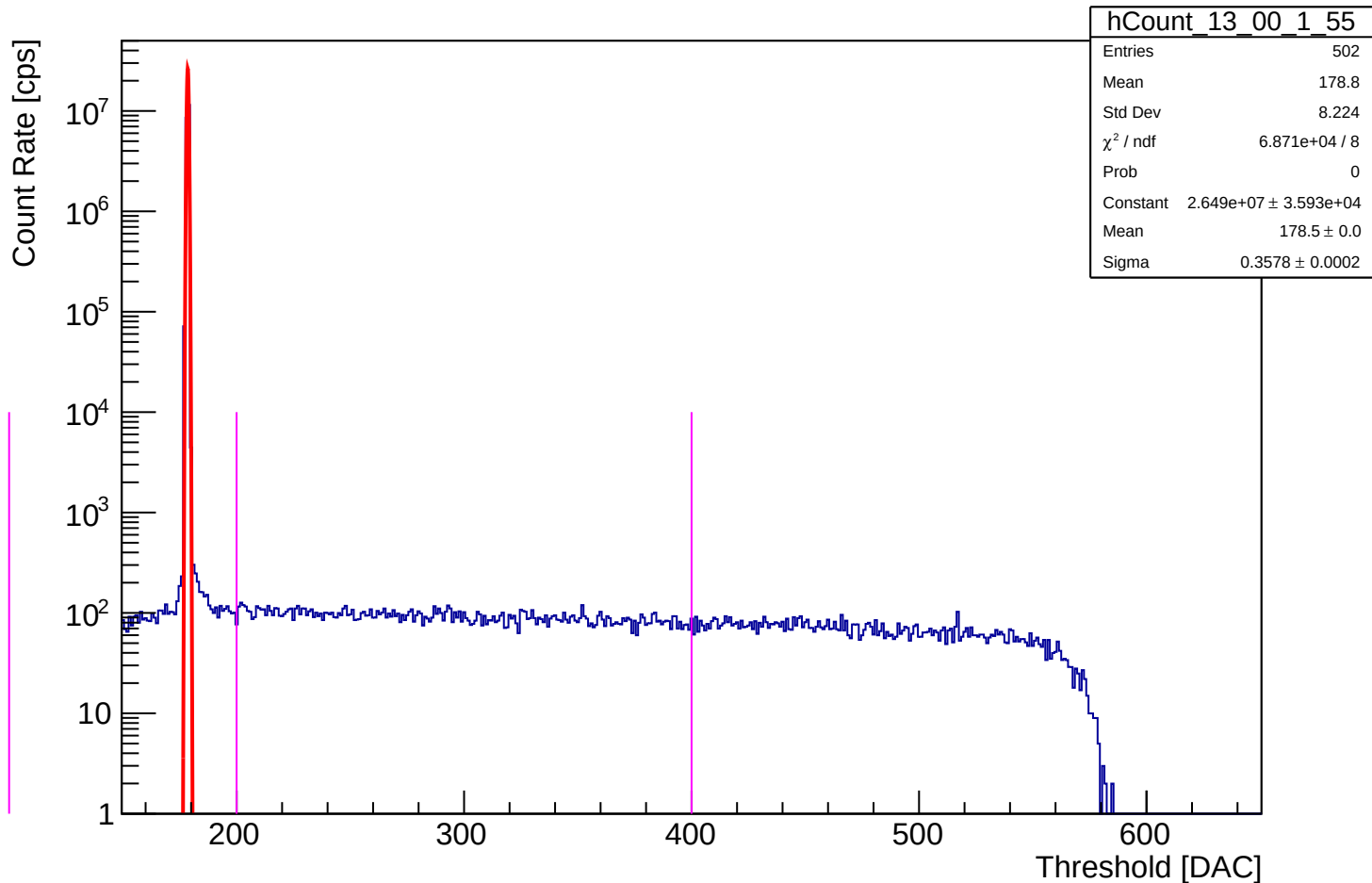
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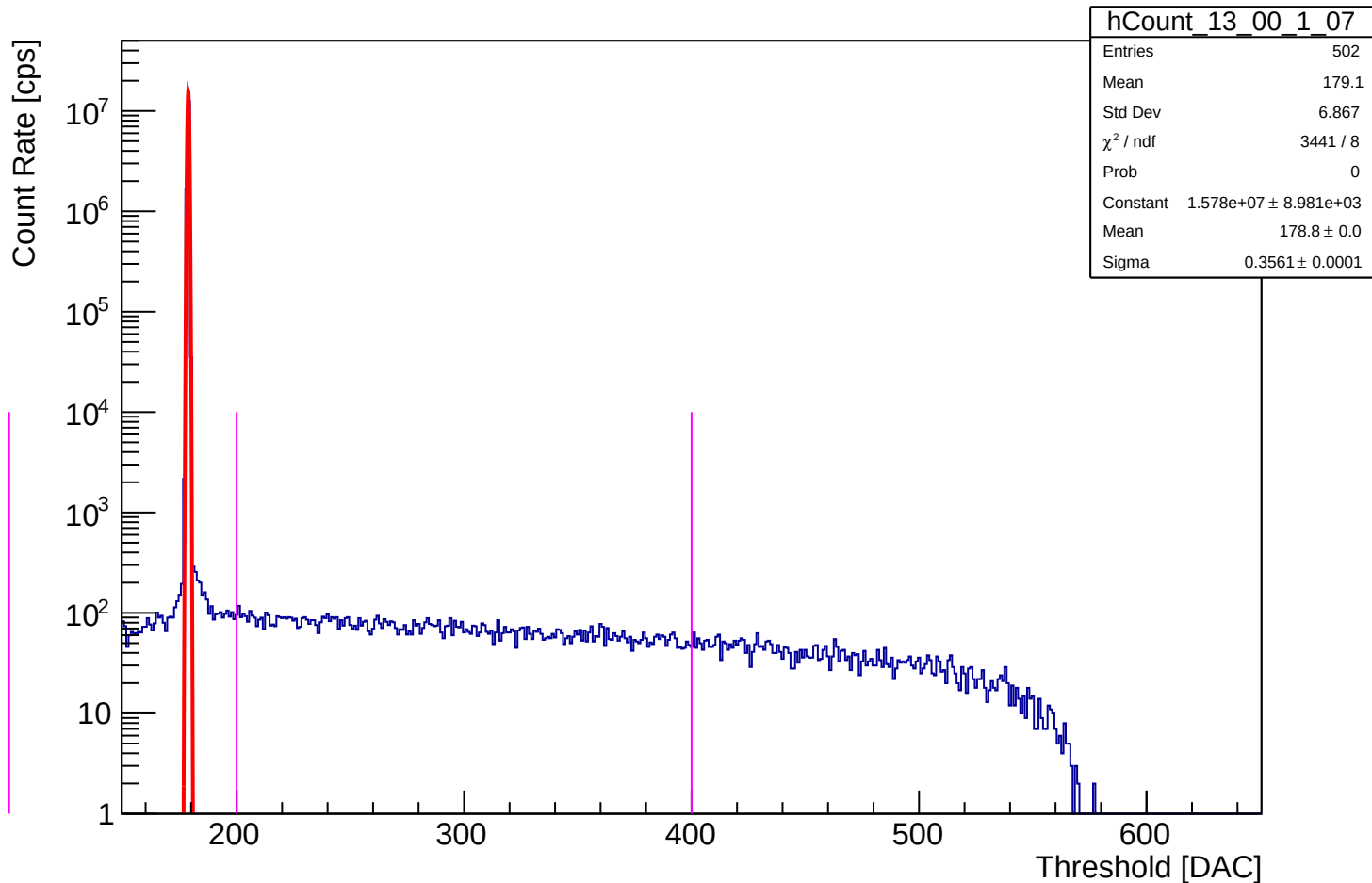
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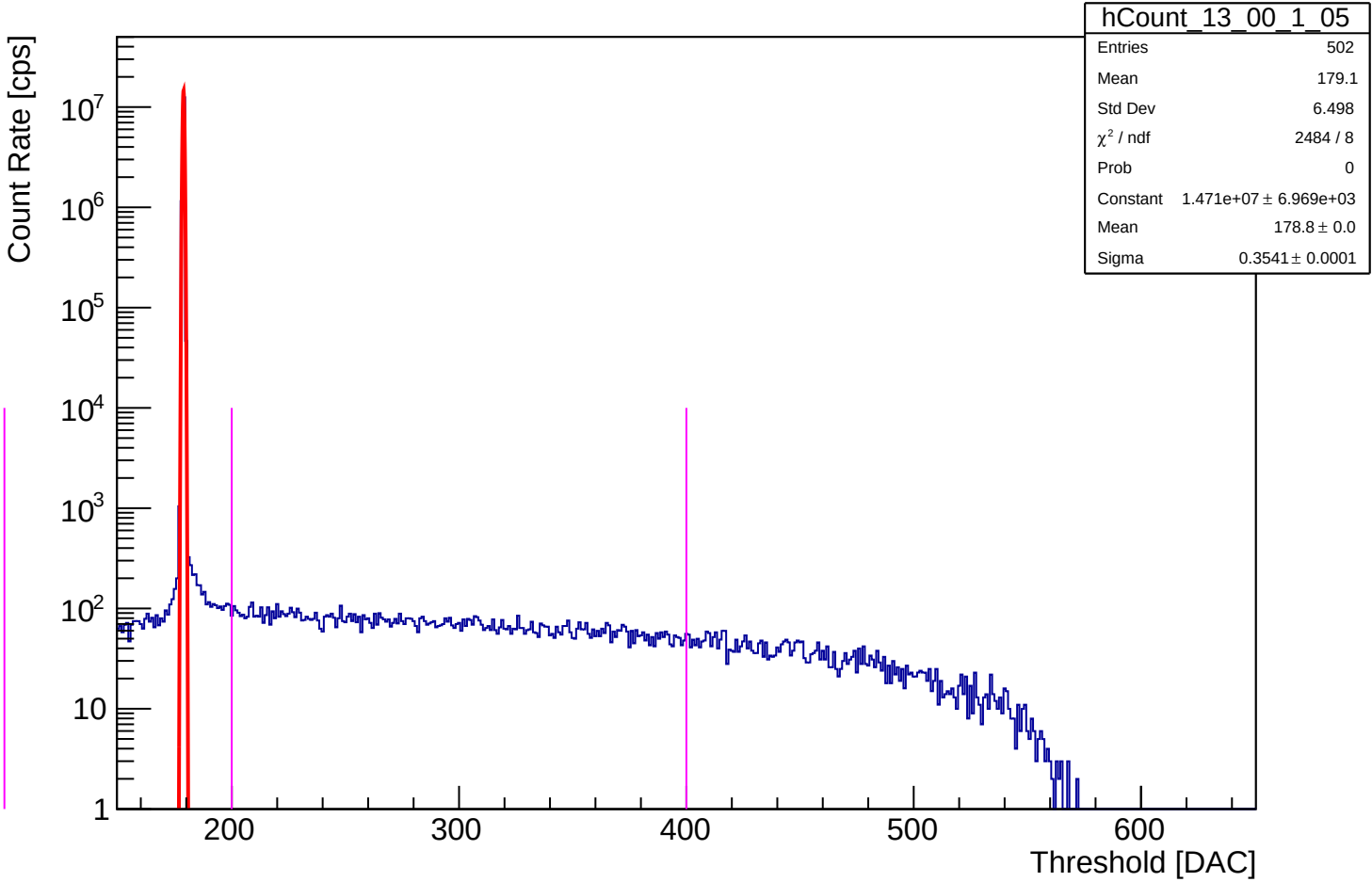


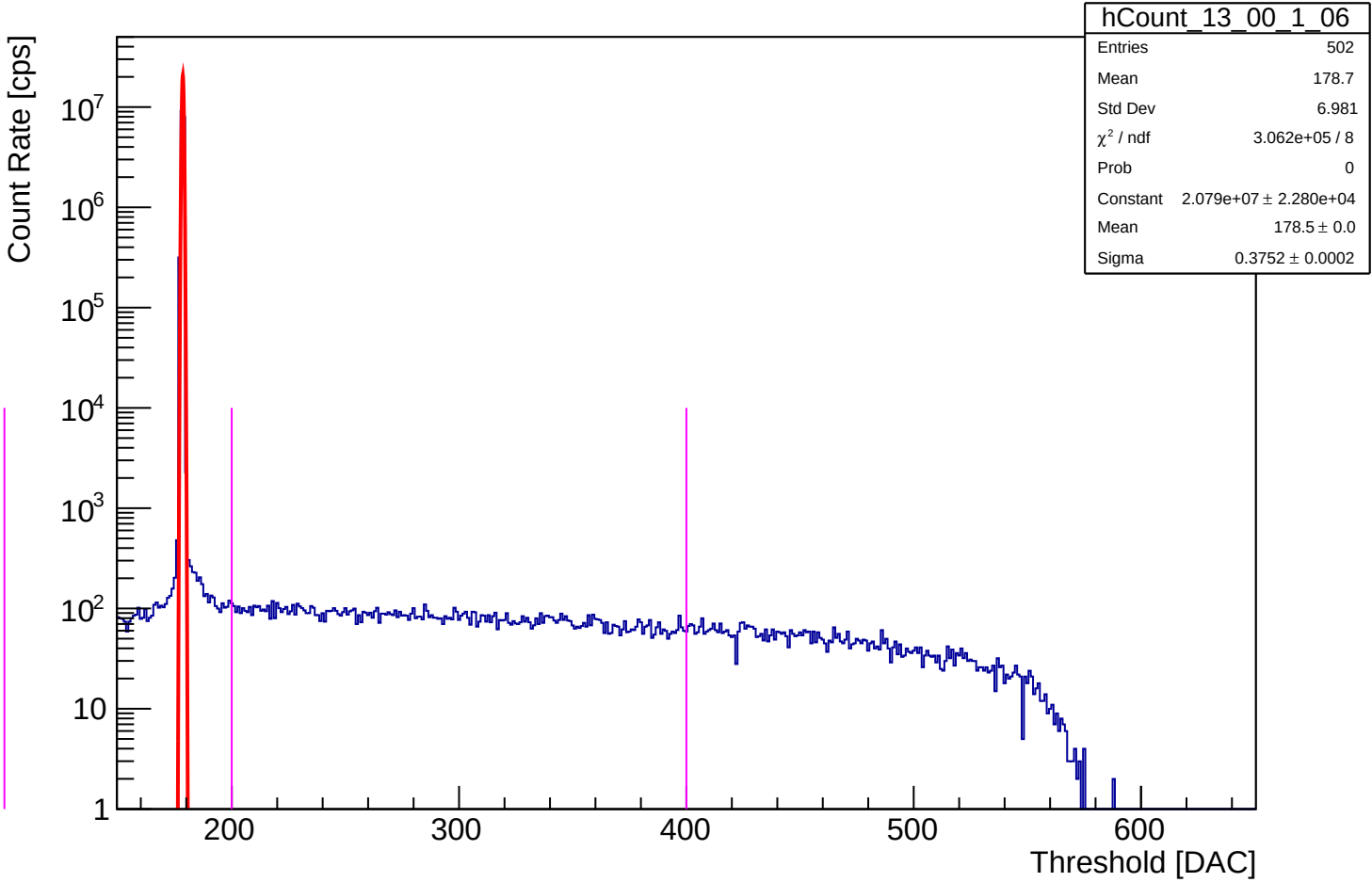
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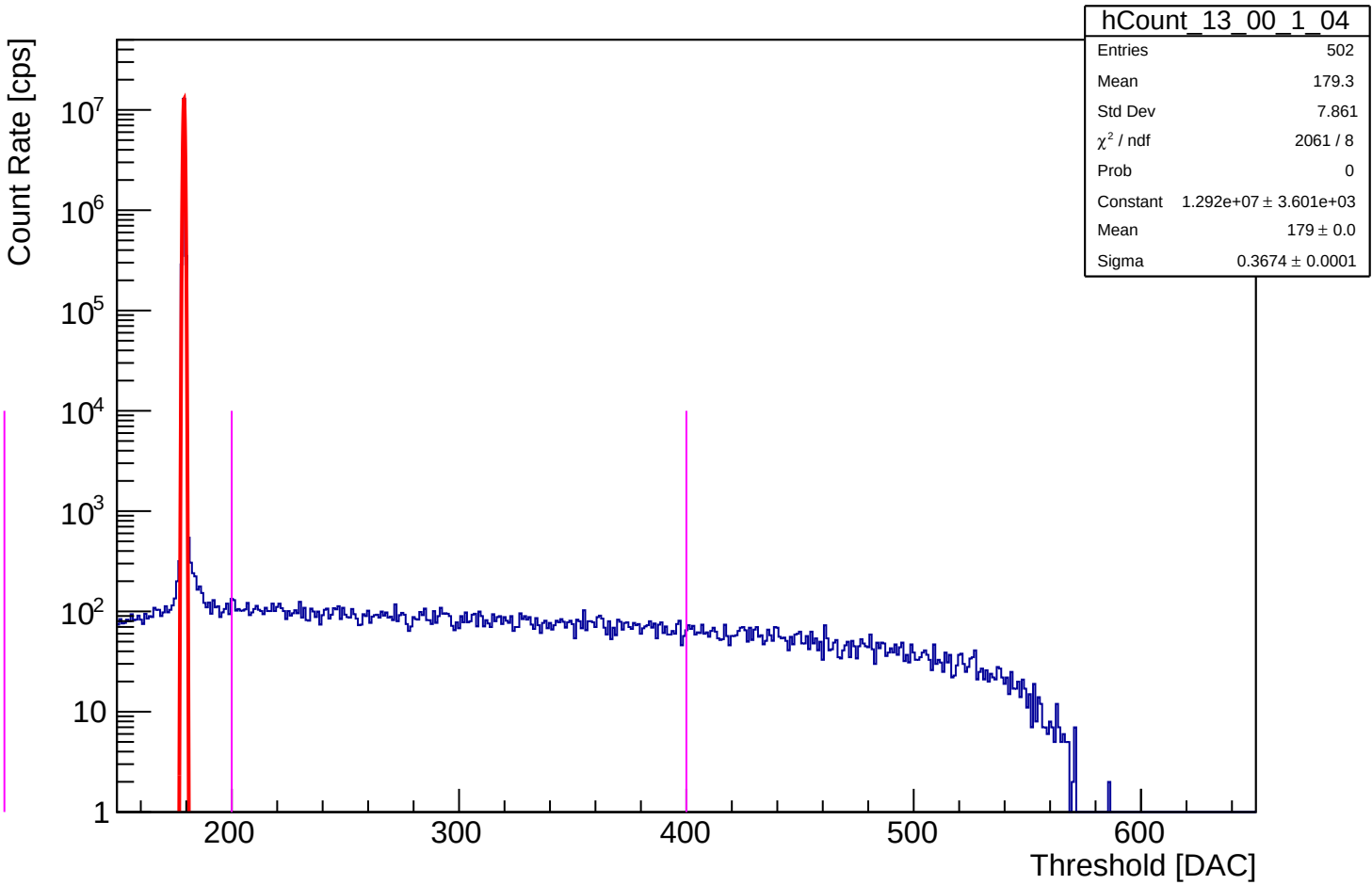


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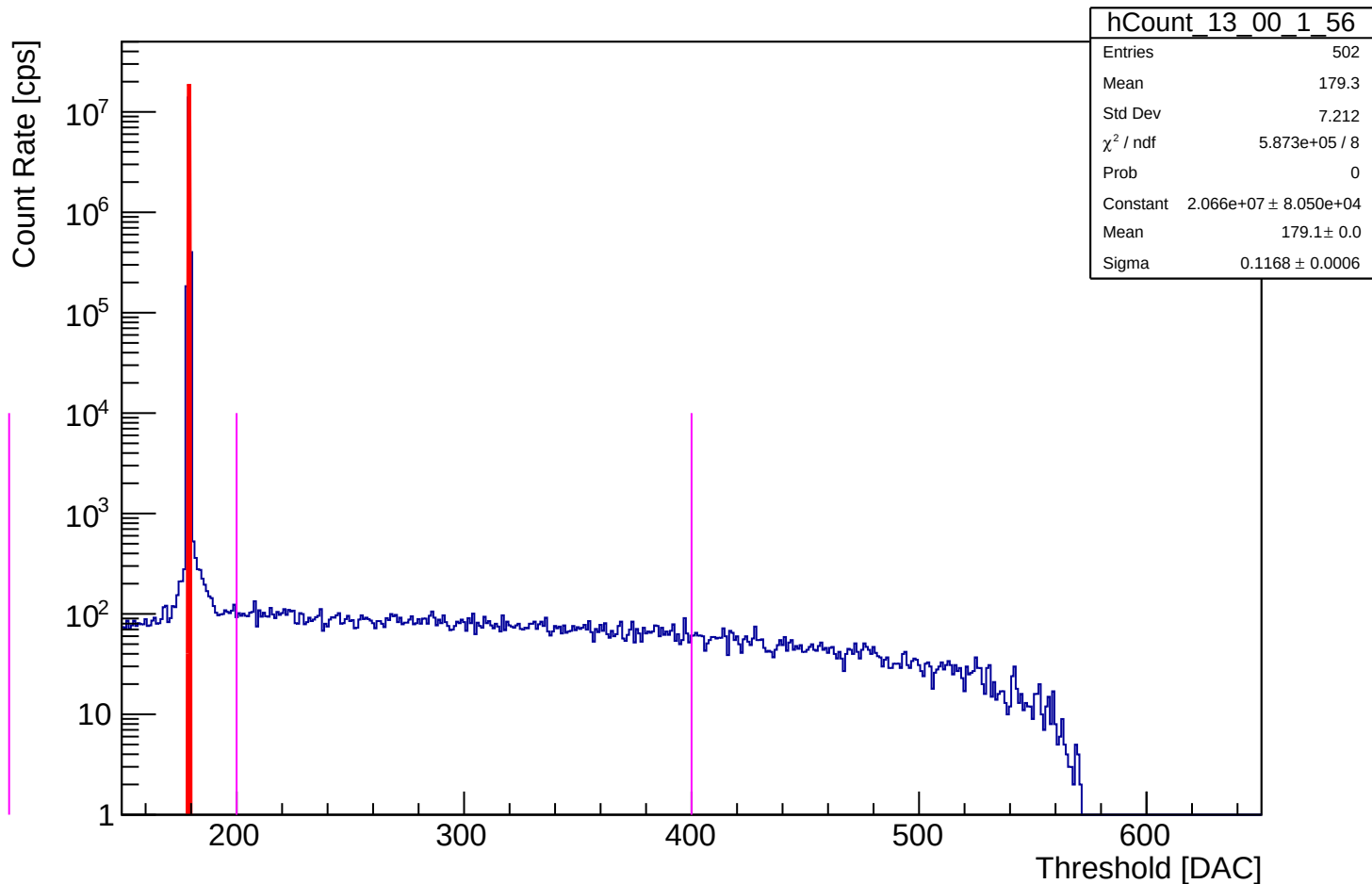




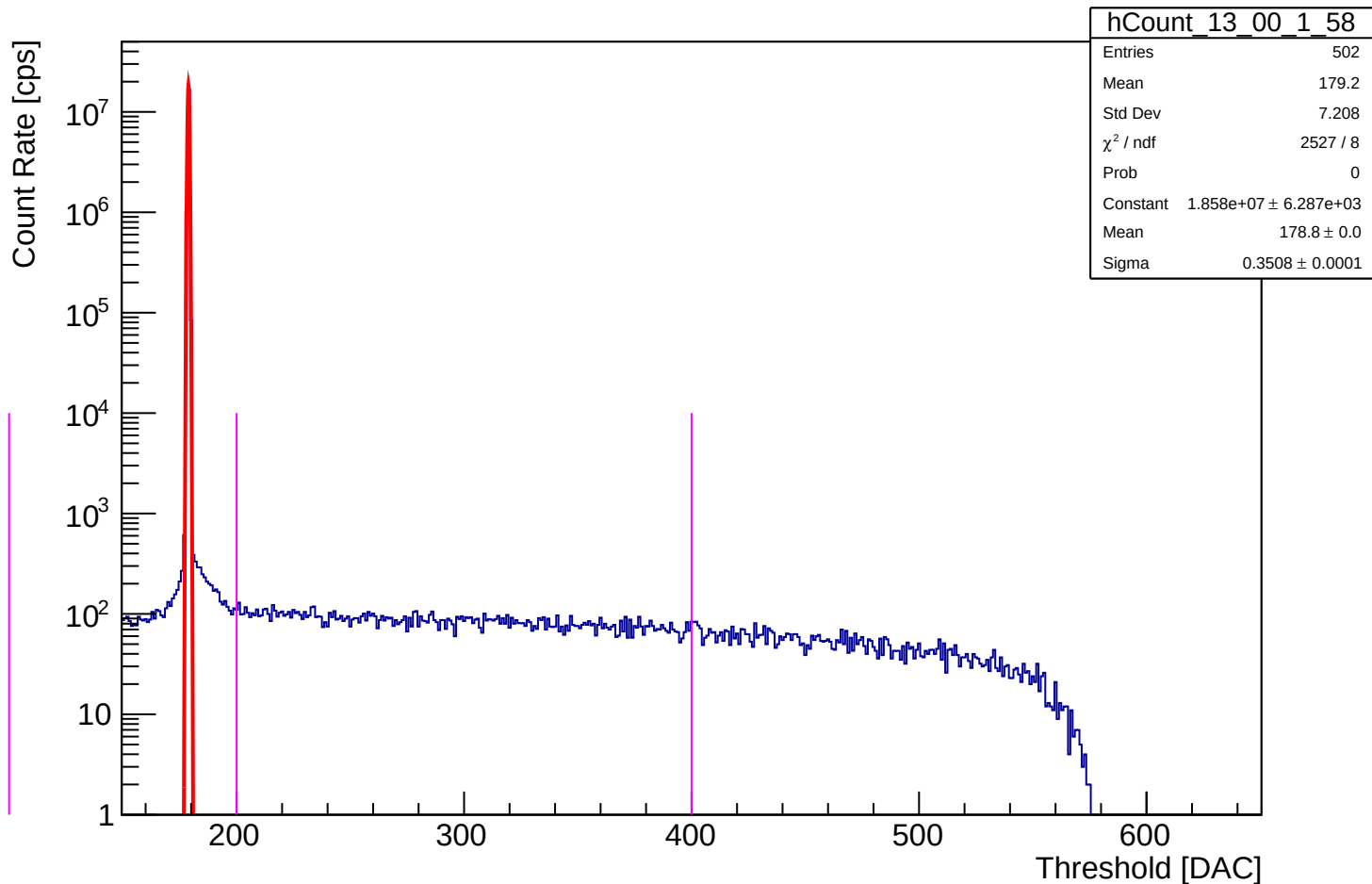




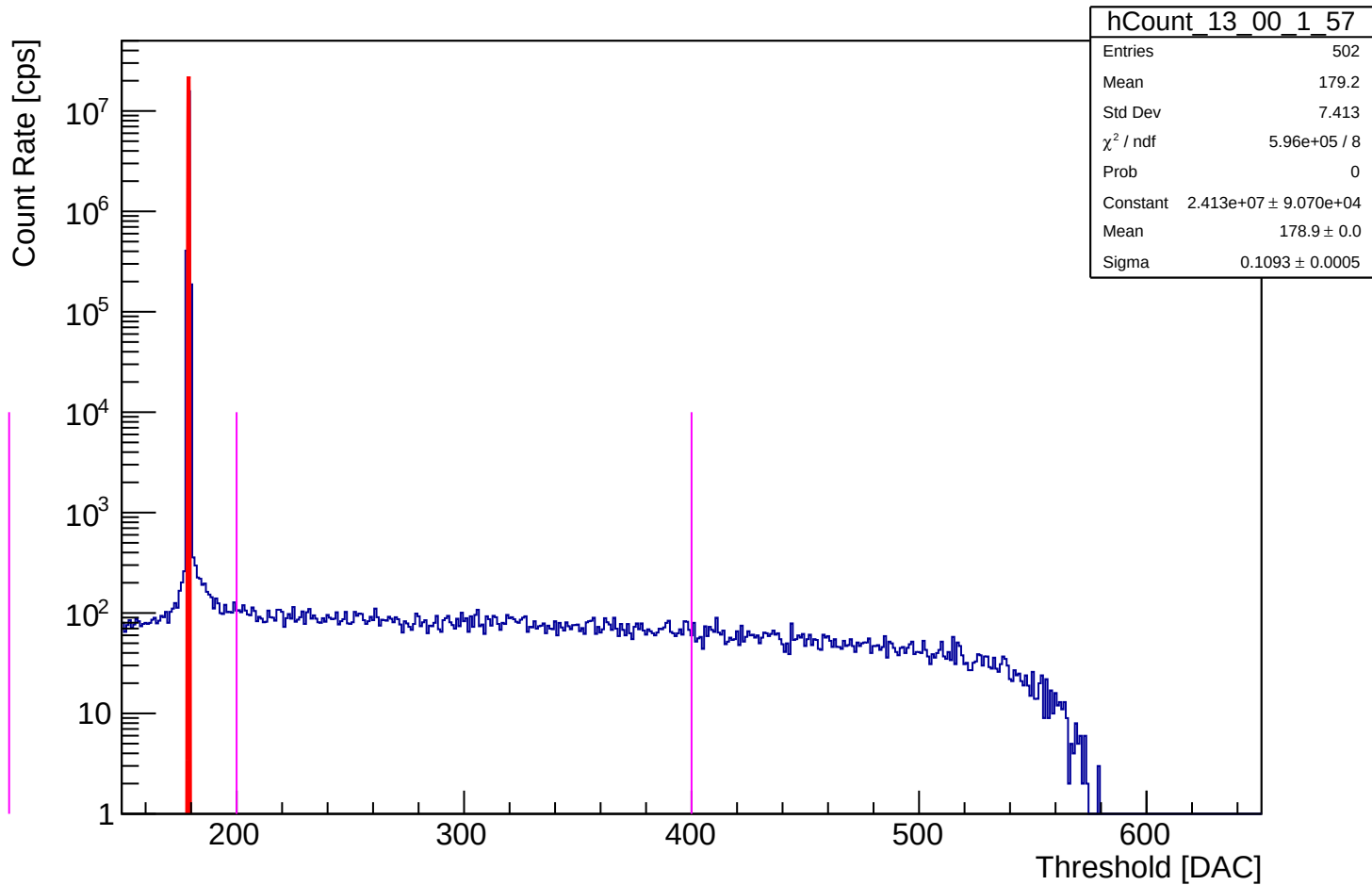
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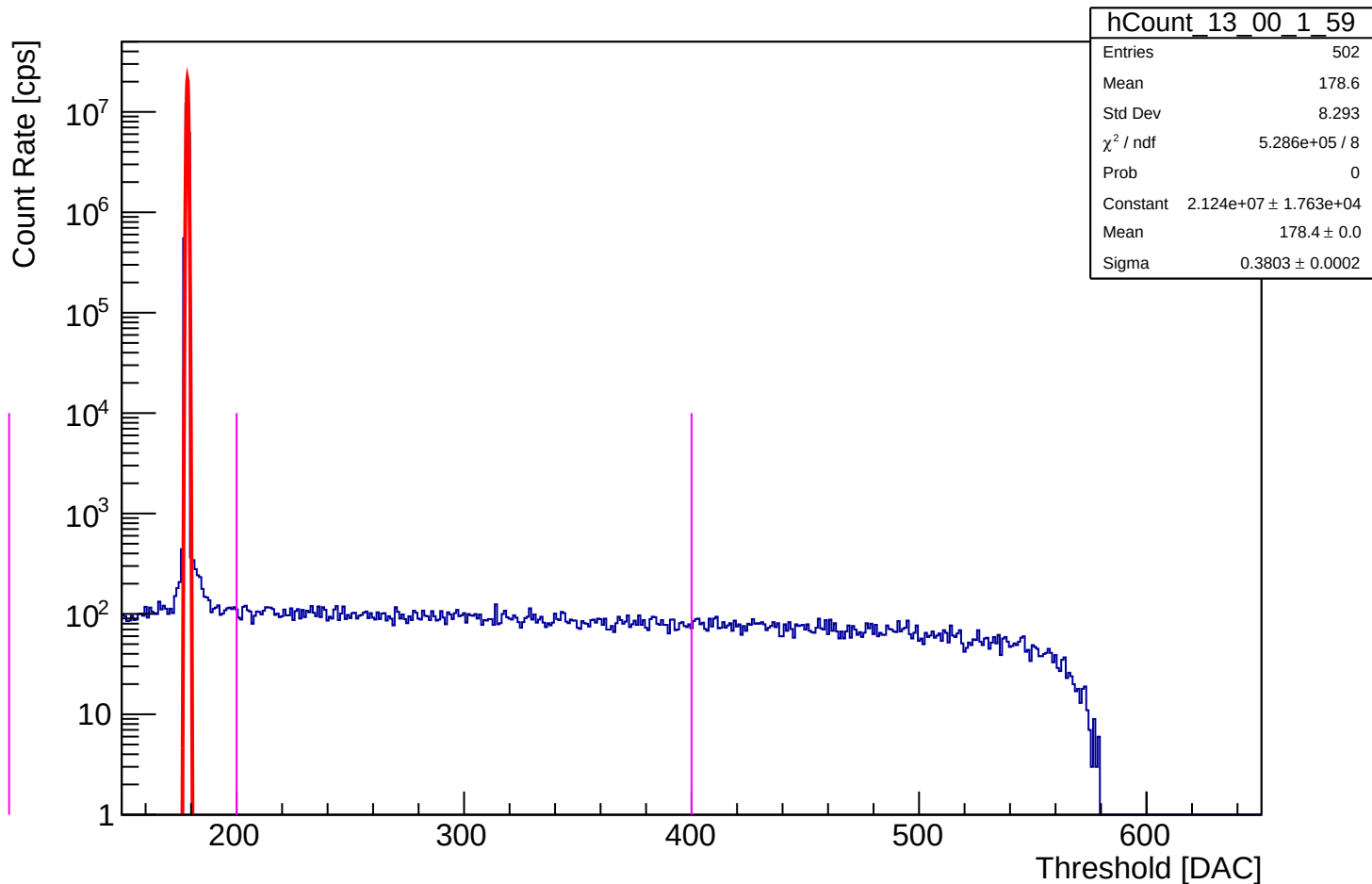
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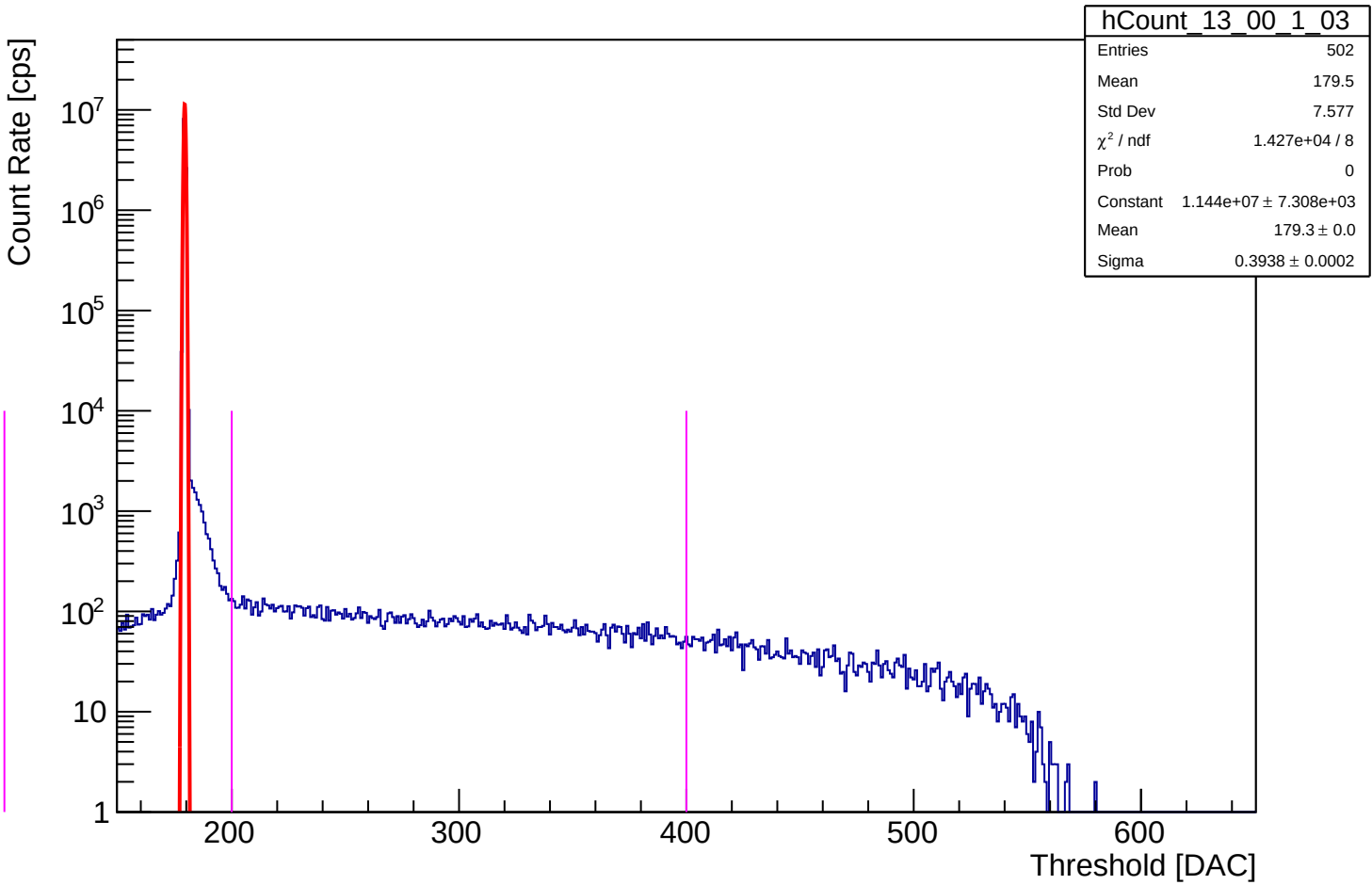


Row 1 Tile 1 Pmt 2 Pixel 55 Slot 13 Fiber 0 Asic 1 Channel 57

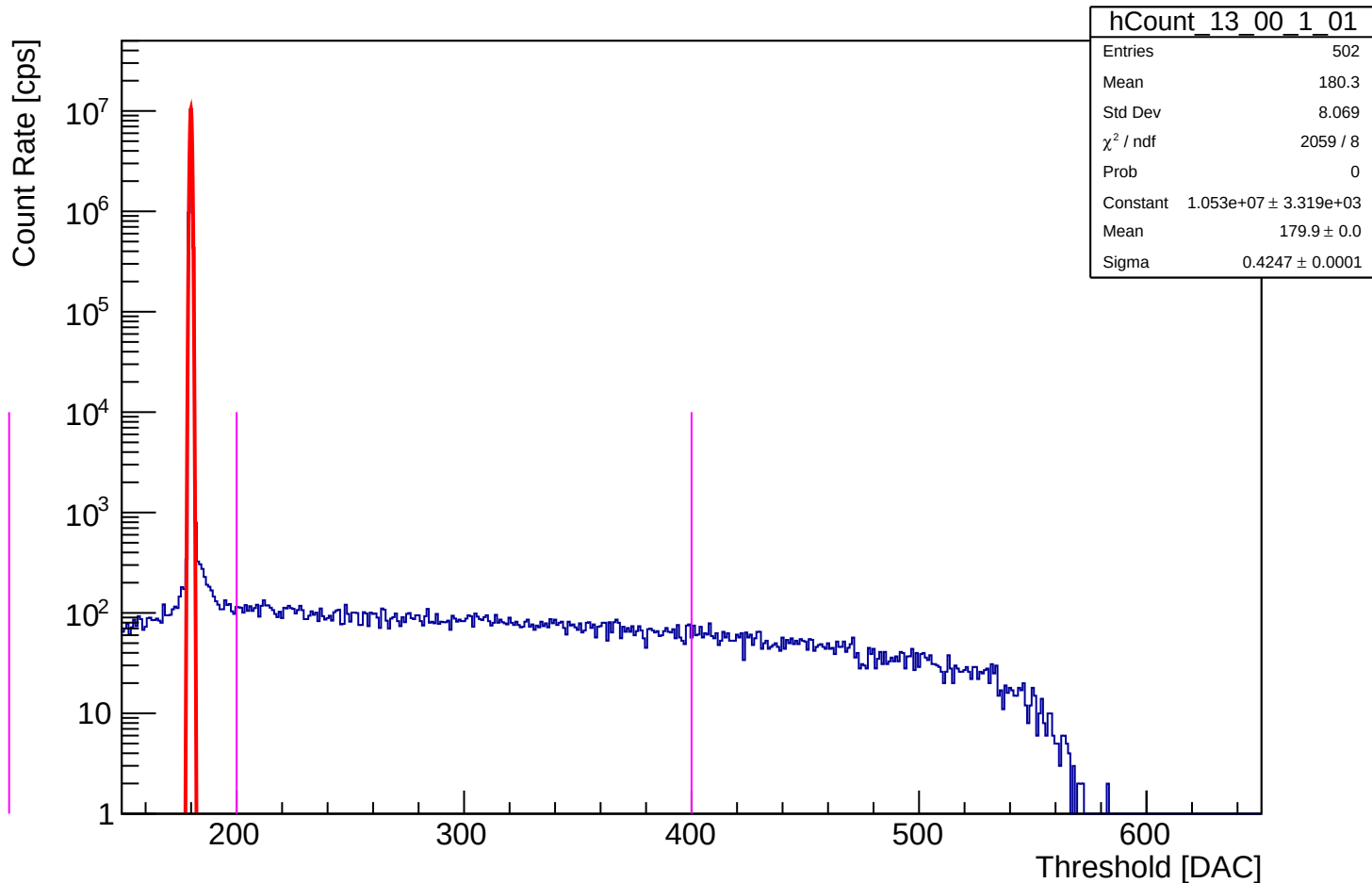


Row 1 Tile 1 Pmt 2 Pixel 56 Slot 13 Fiber 0 Asic 1 Channel 59





Row 1 Tile 1 Pmt 2 Pixel 58 Slot 13 Fiber 0 Asic 1 Channel 1



Count Rate [cps]

10⁷
10⁶
10⁵
10⁴
10³
10²
10
1

200

300

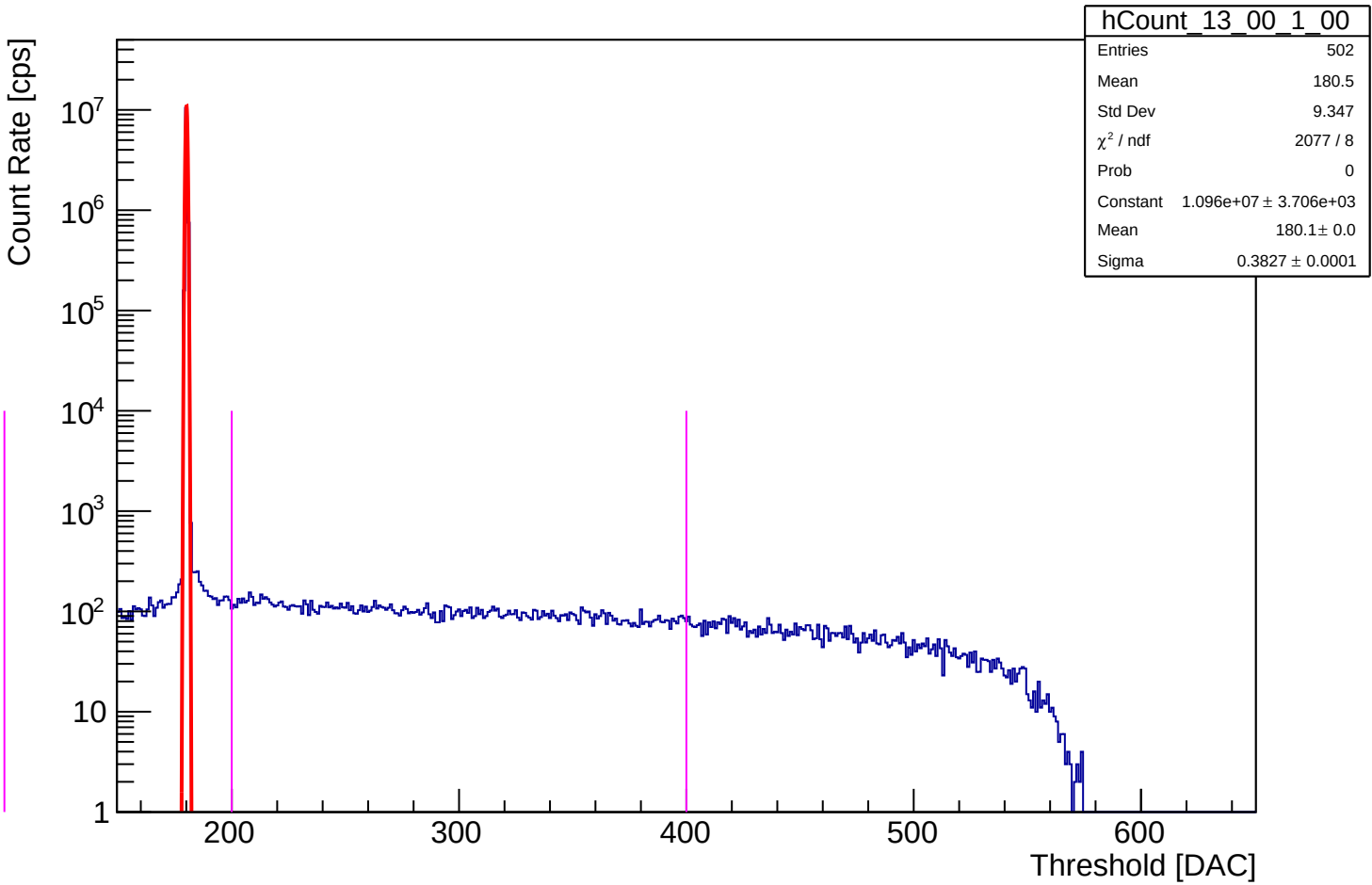
400

500

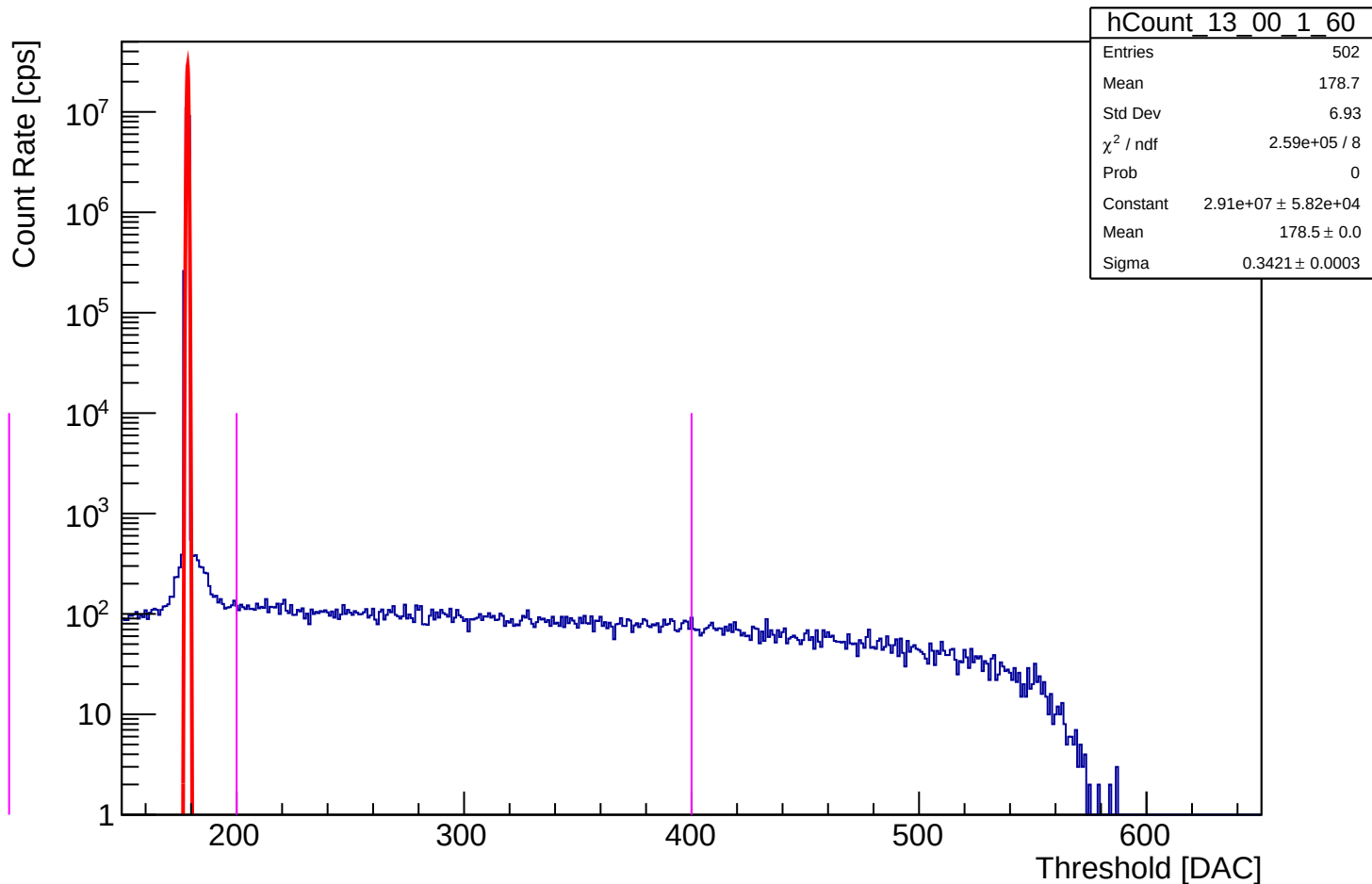
600

Threshold [DAC]

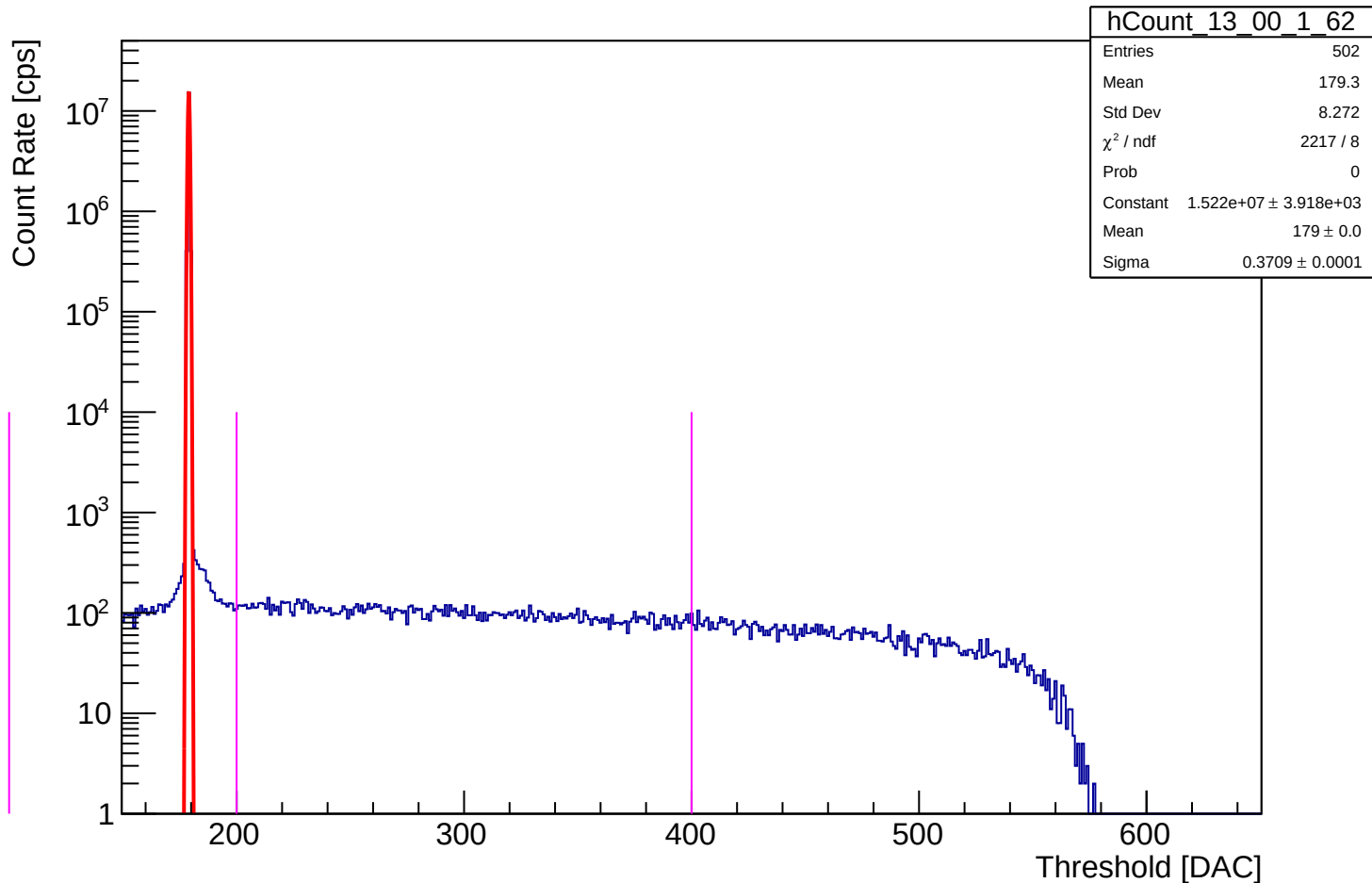
hCount_13_00_1_02	
Entries	502
Mean	179
Std Dev	6.171
χ^2 / ndf	6318 / 8
Prob	0
Constant	2.546e+07 $\pm$ 1.865e+04
Mean	178.7 $\pm$ 0.0
Sigma	0.3612 $\pm$ 0.0001



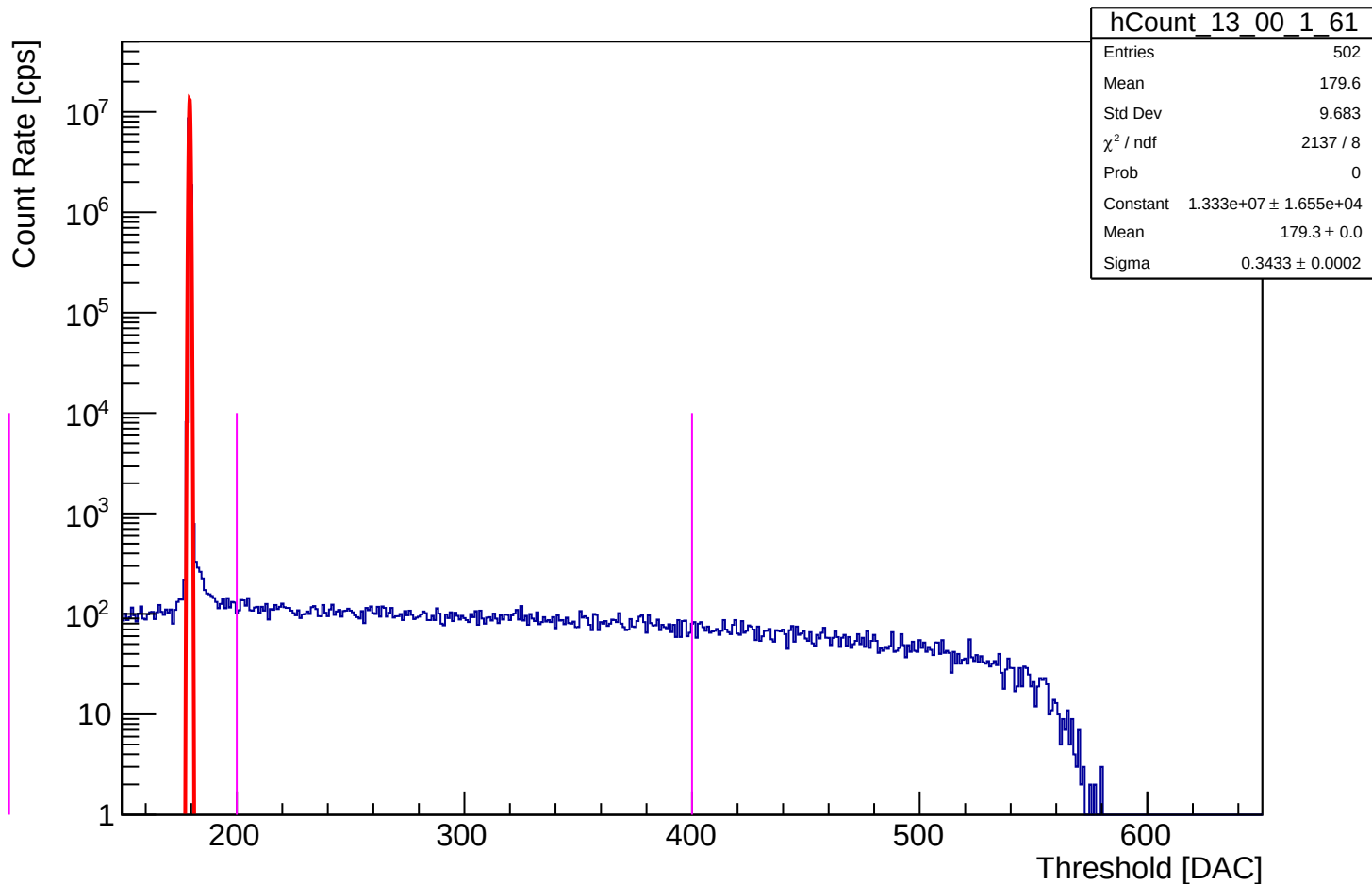
Row 1 Tile 1 Pmt 2 Pixel 61 Slot 13 Fiber 0 Asic 1 Channel 60



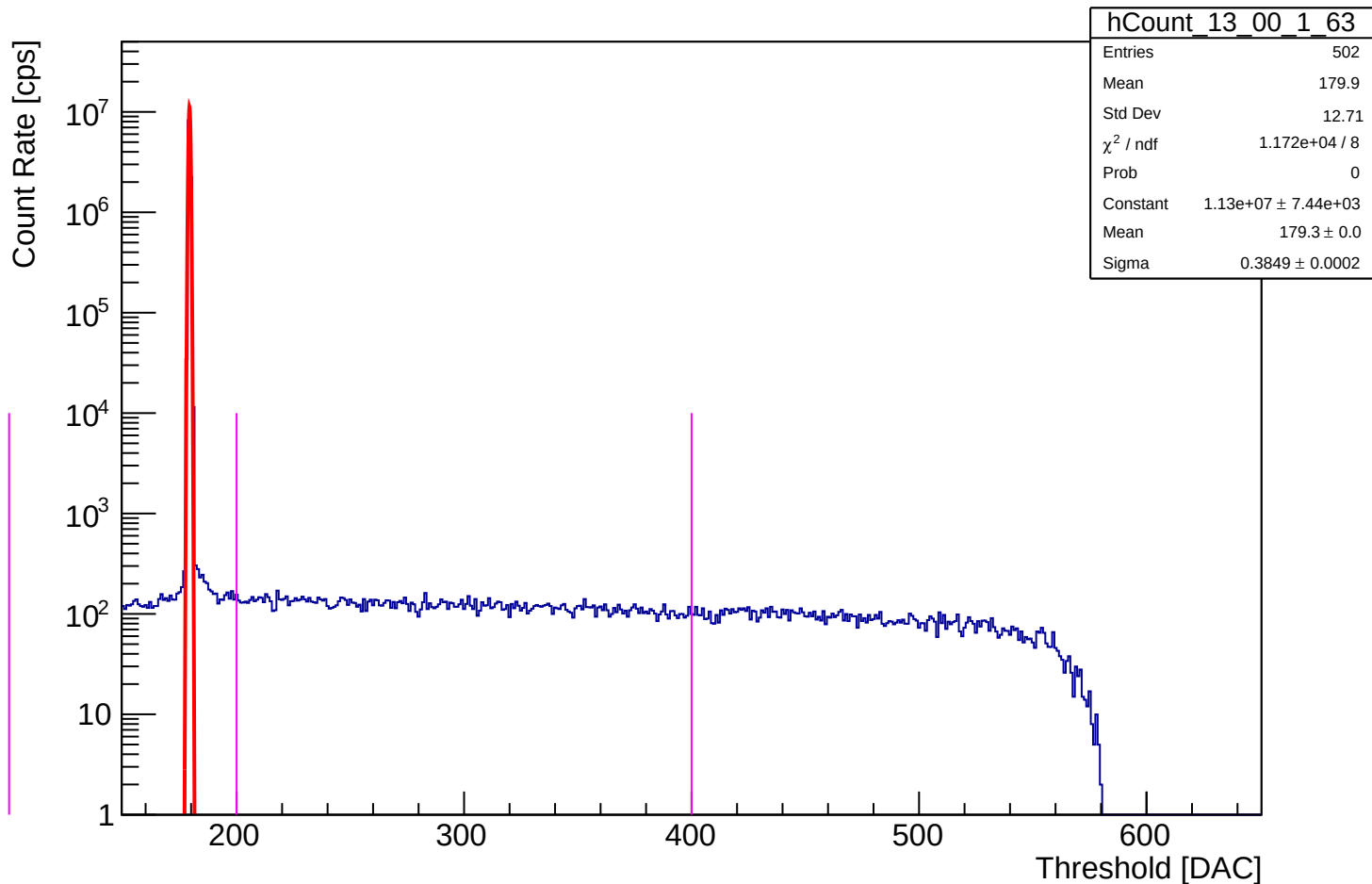
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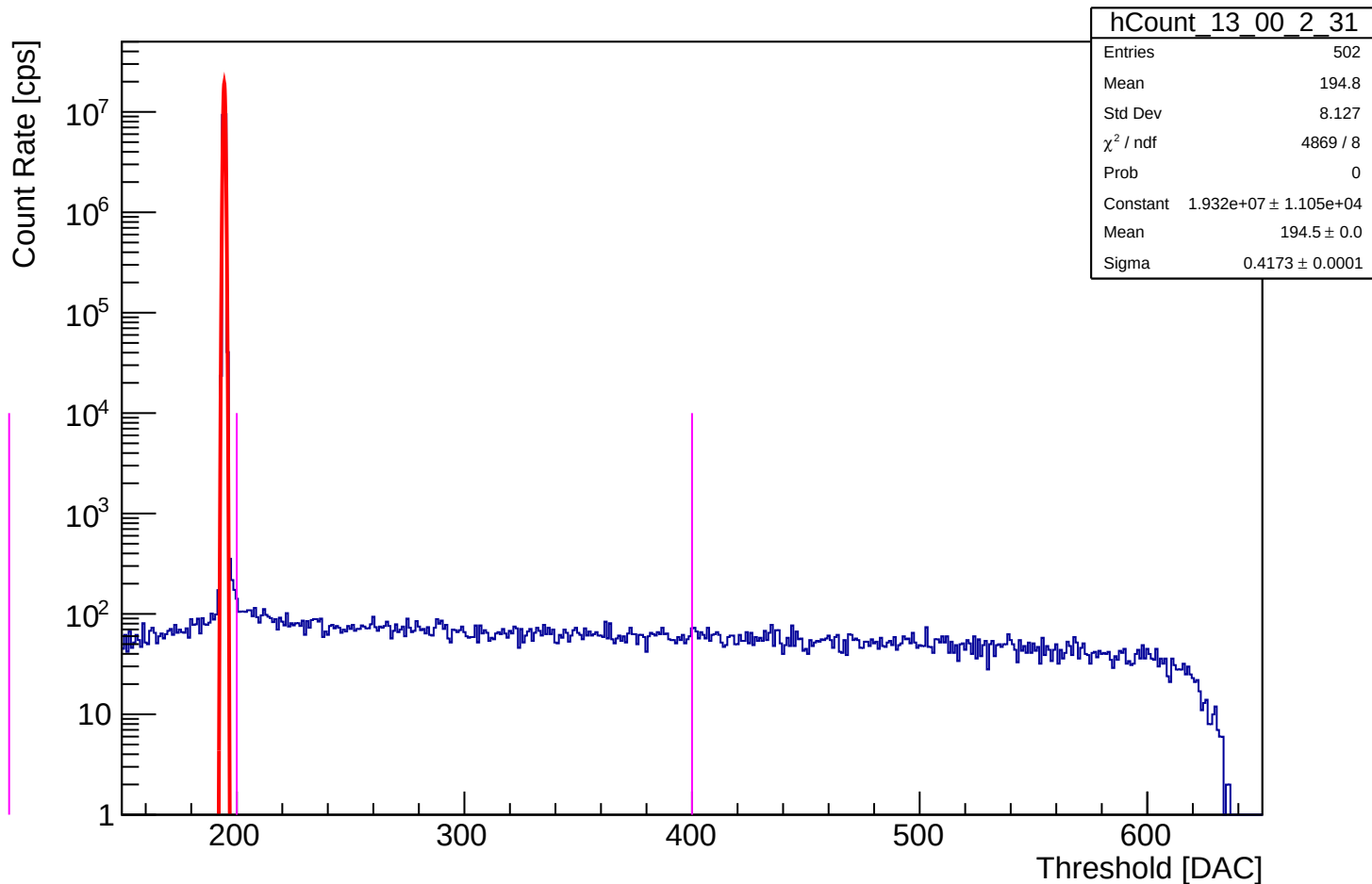
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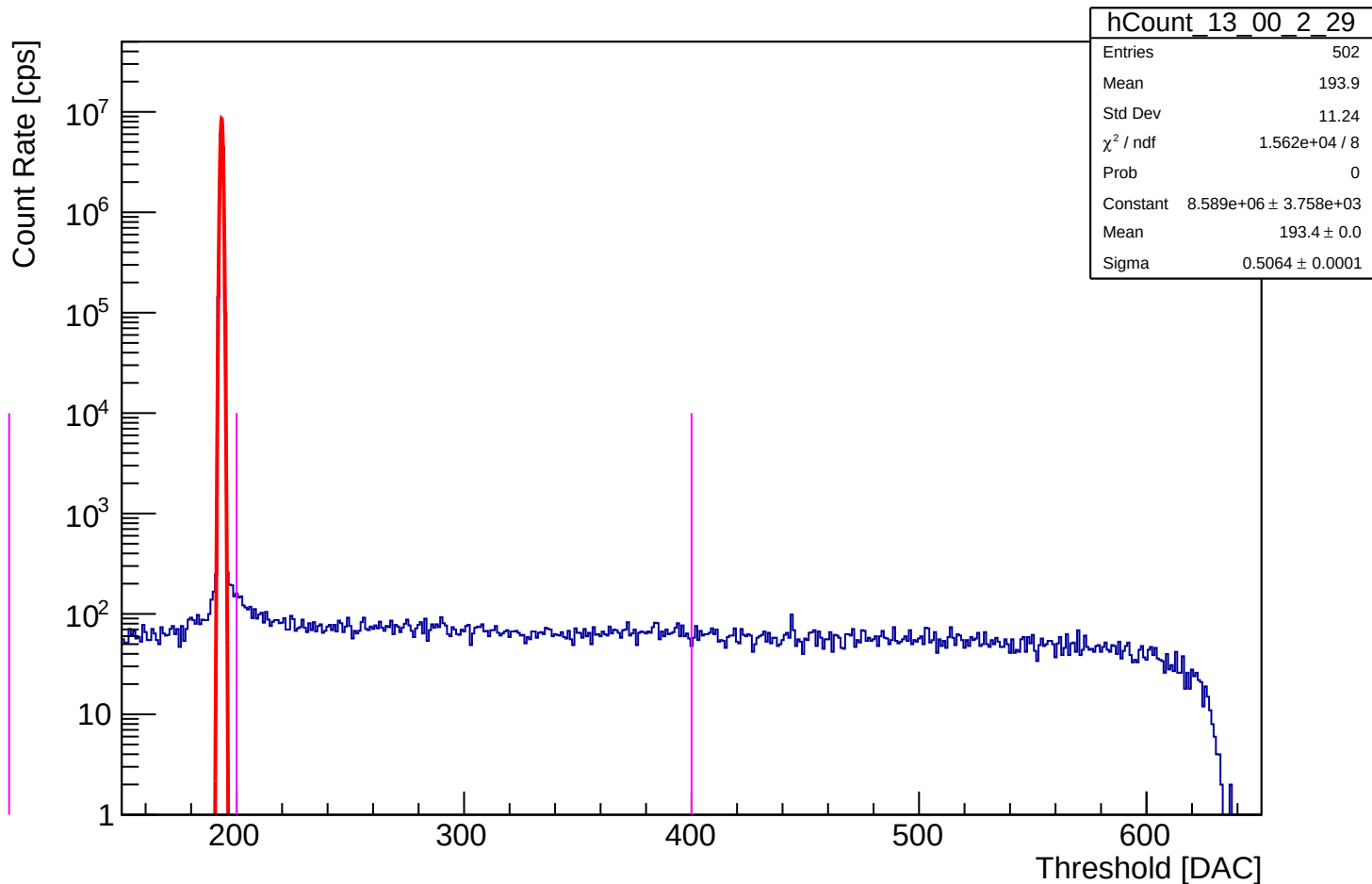
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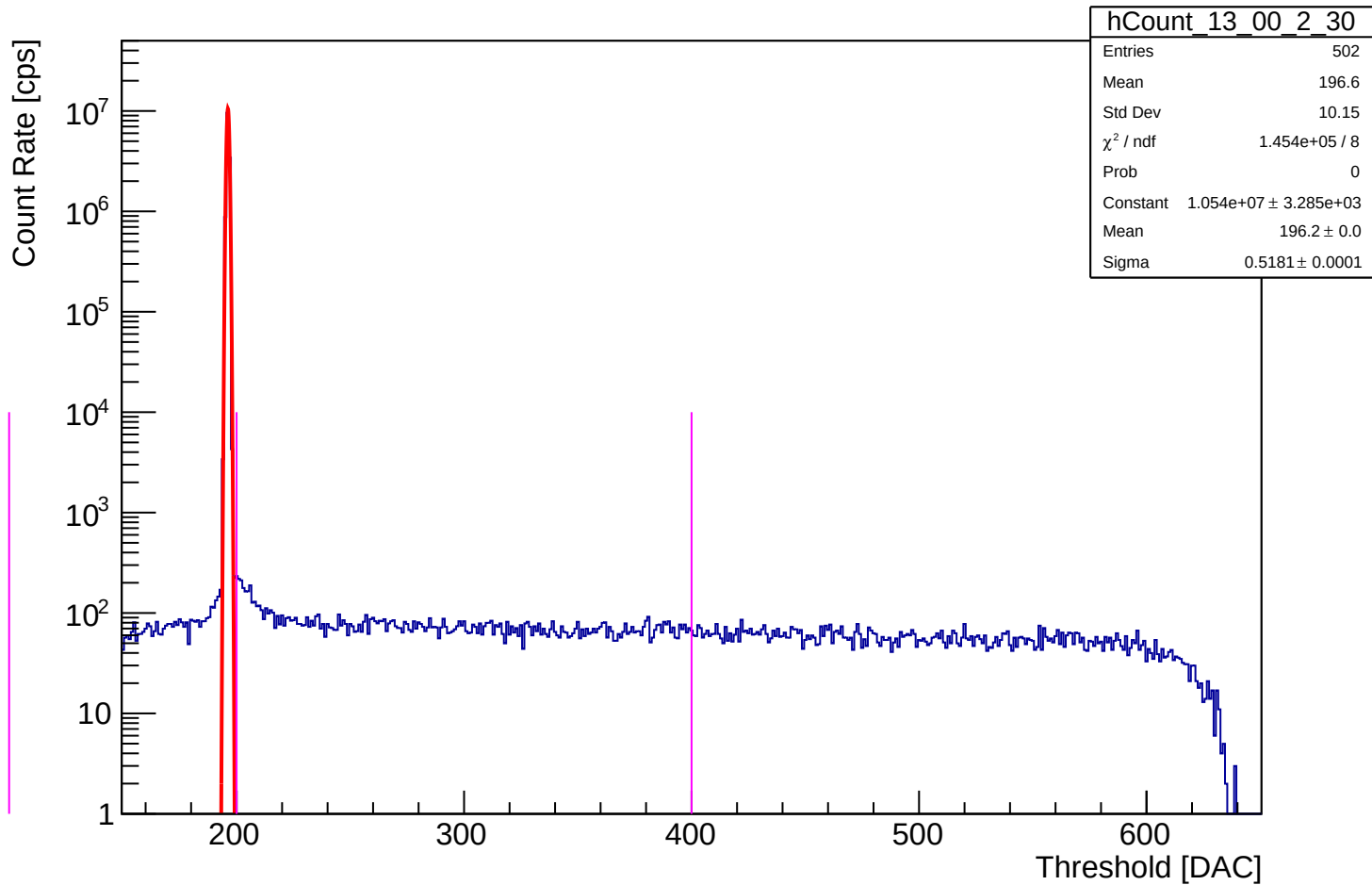
Row 1 Tile 1 Pmt 3 Pixel 1 Slot 13 Fiber 0 Asic 2 Channel 31



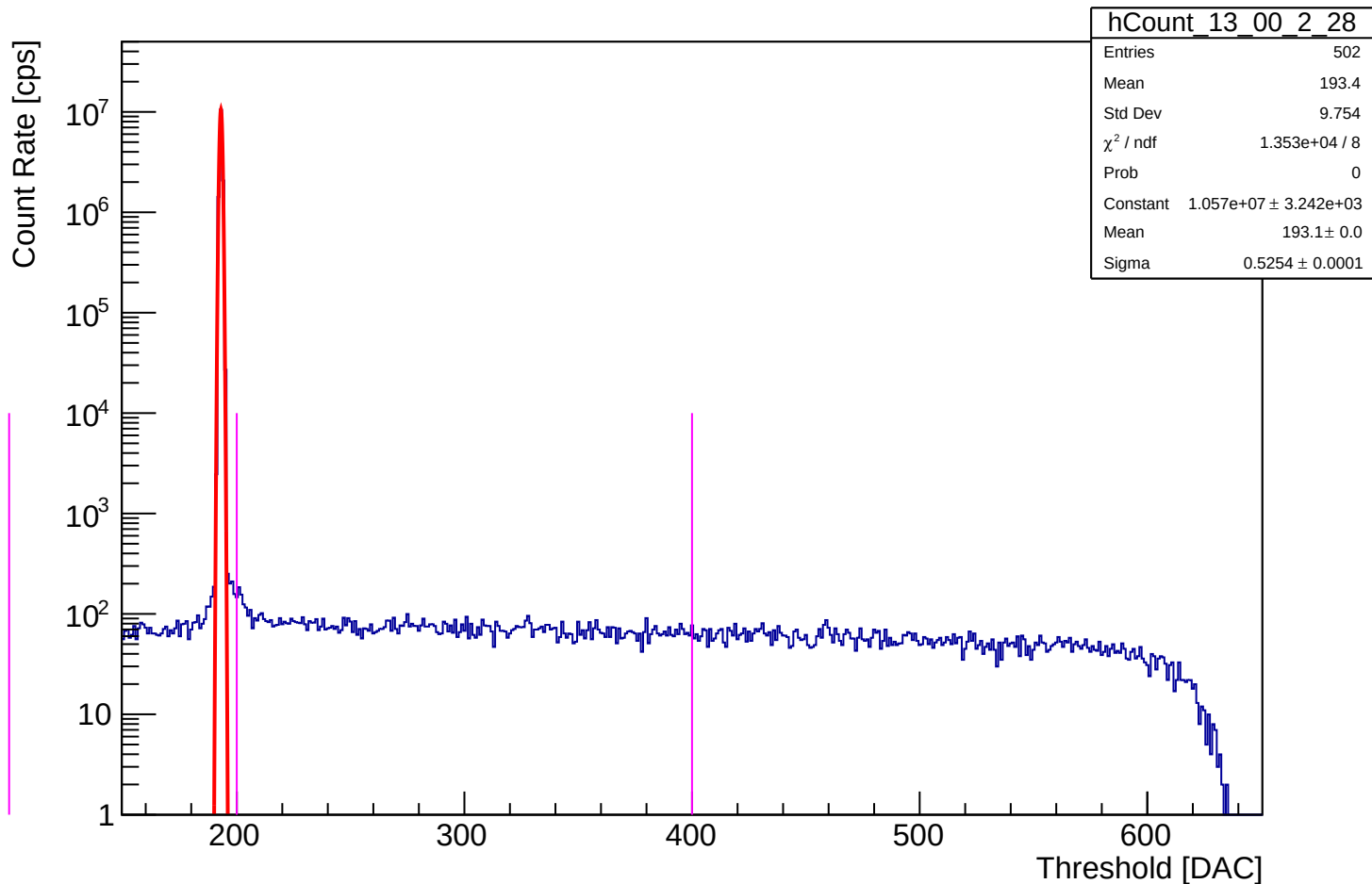
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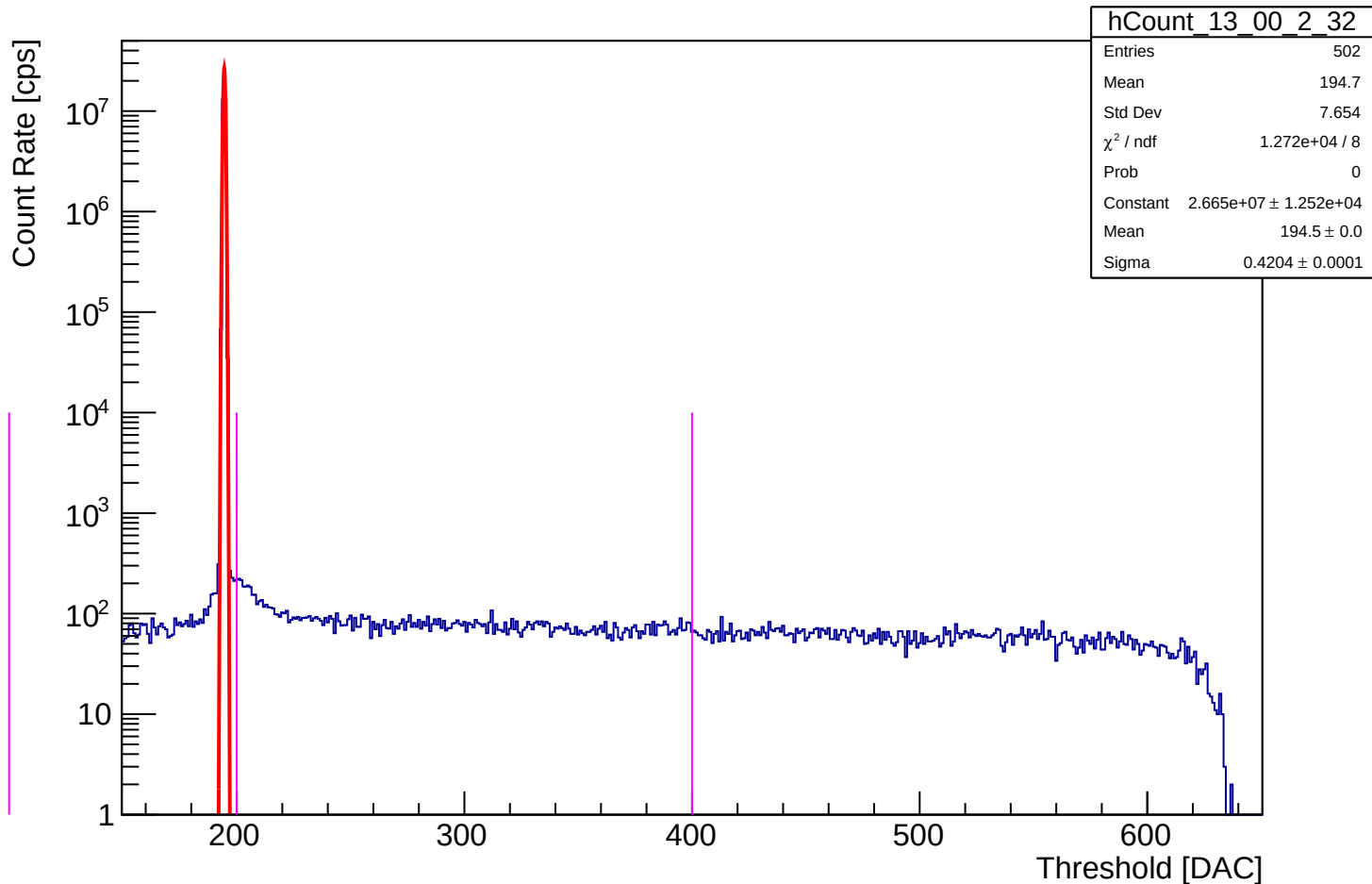
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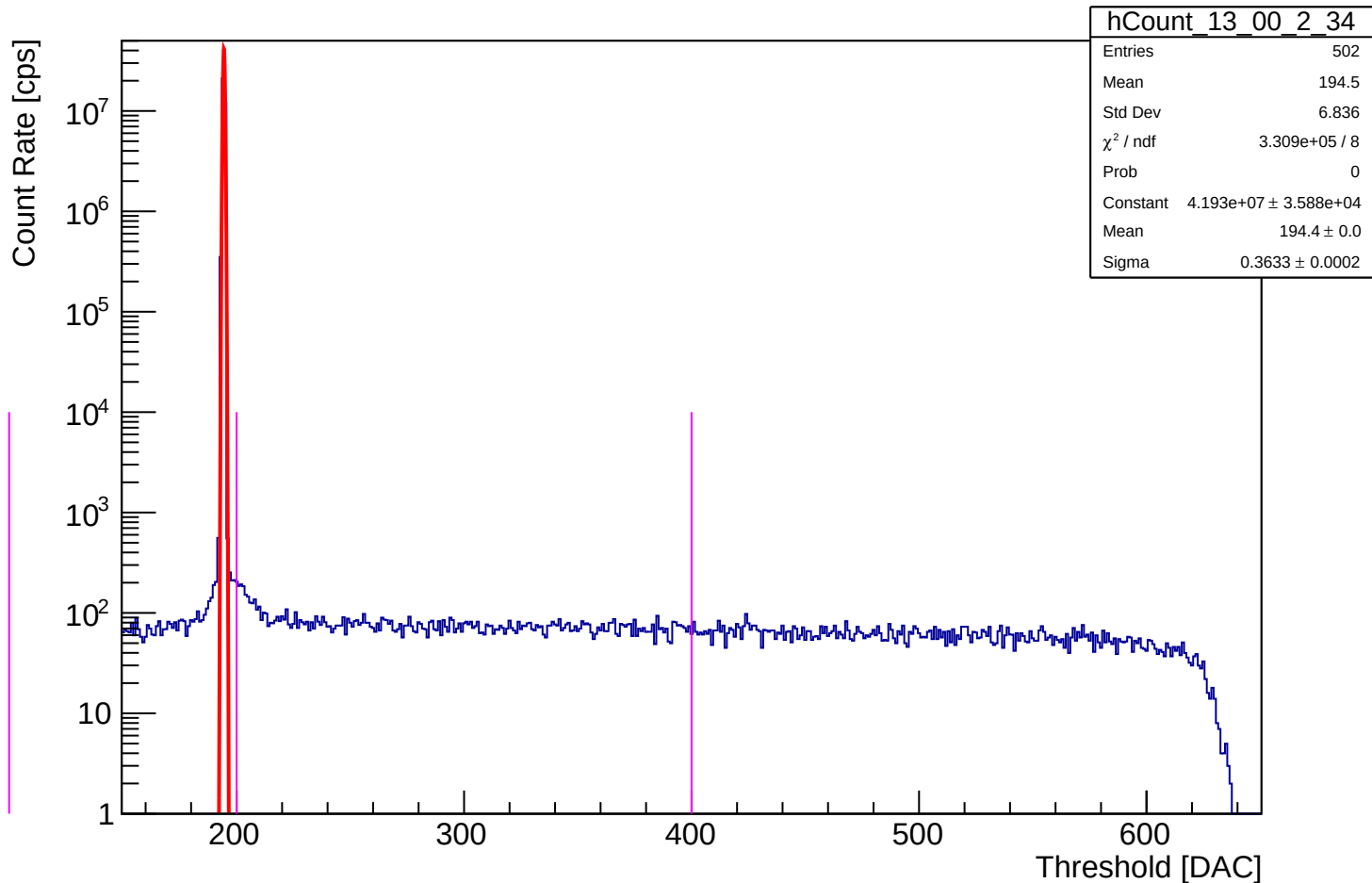
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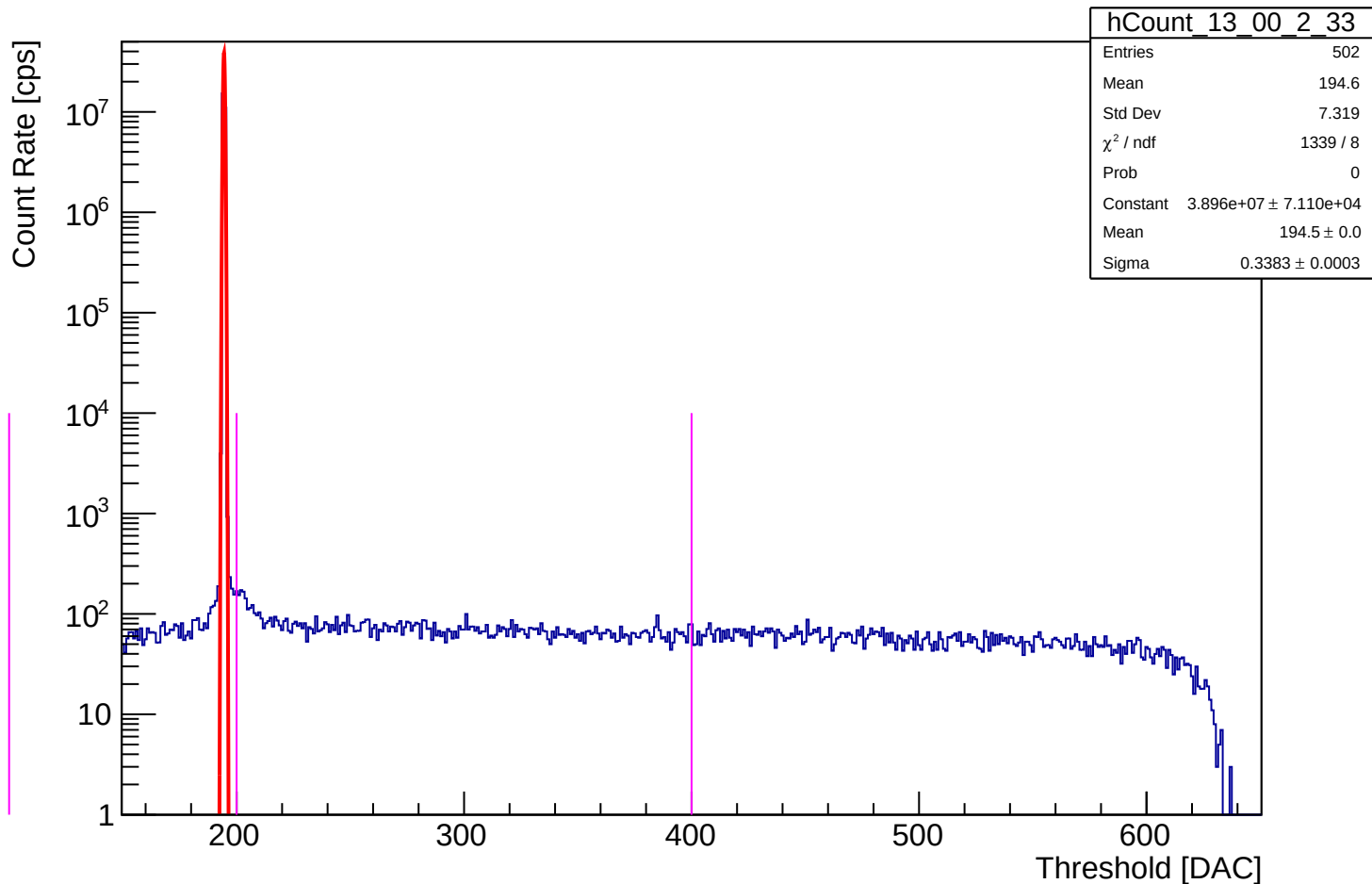
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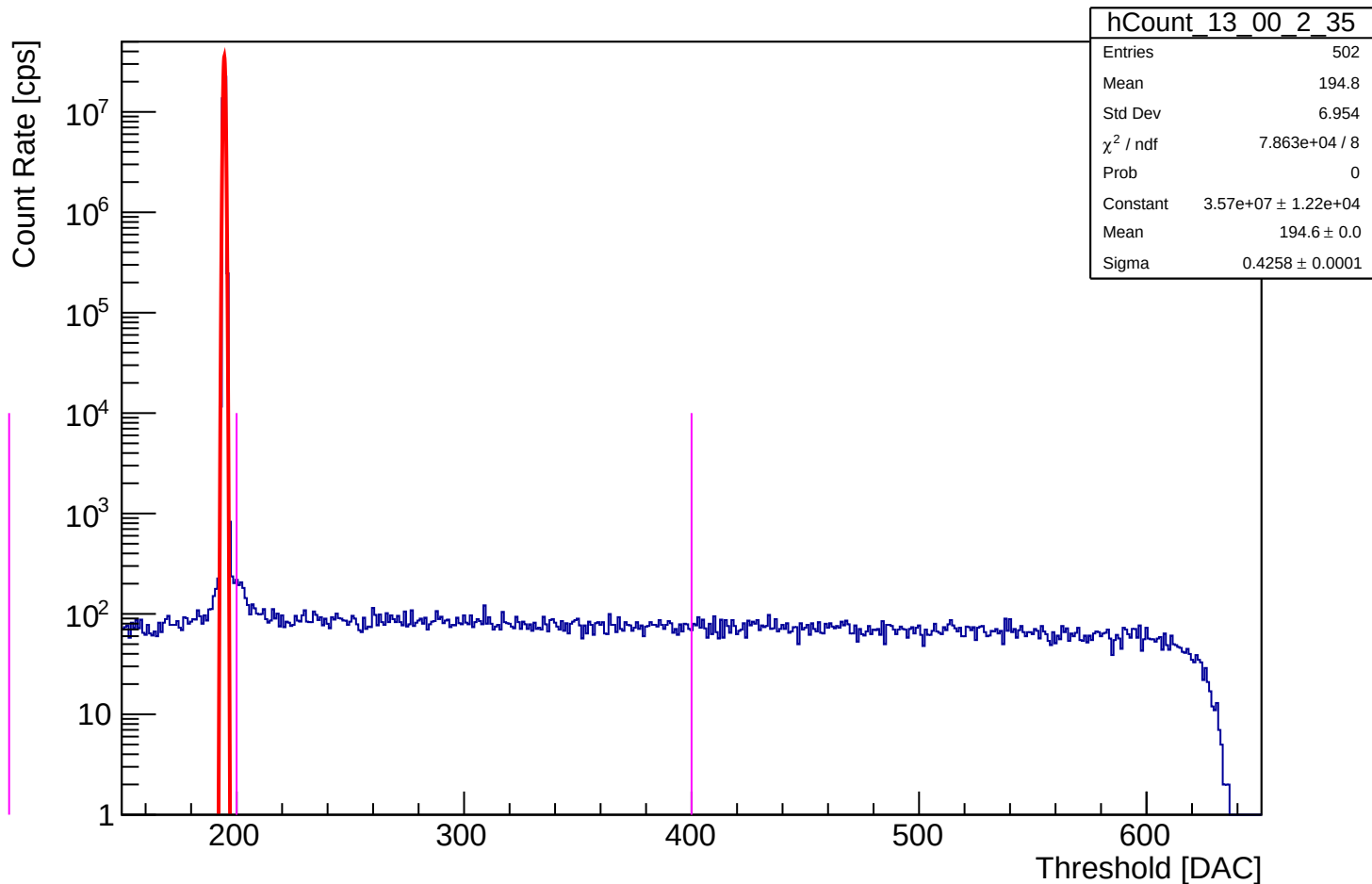
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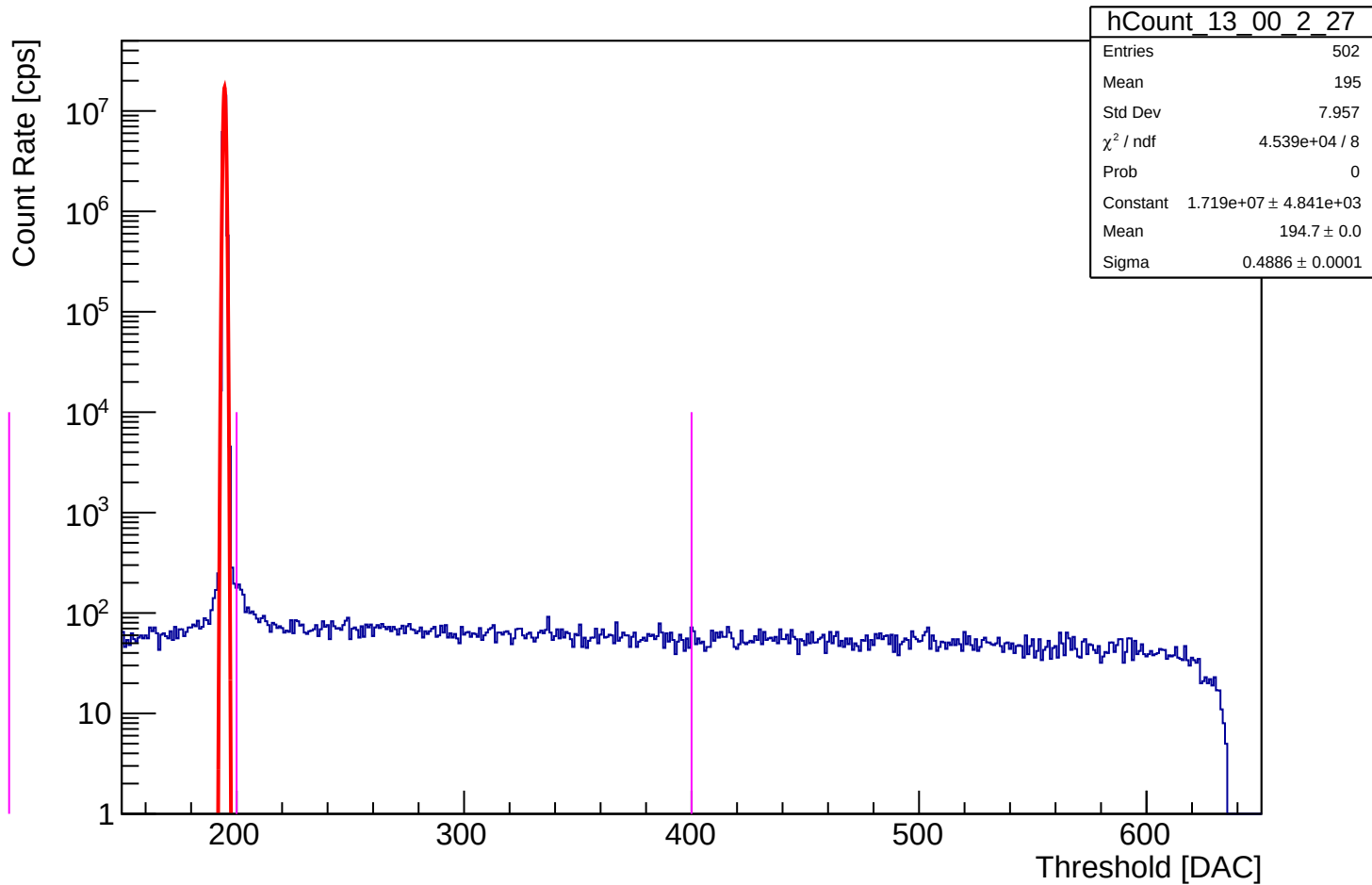
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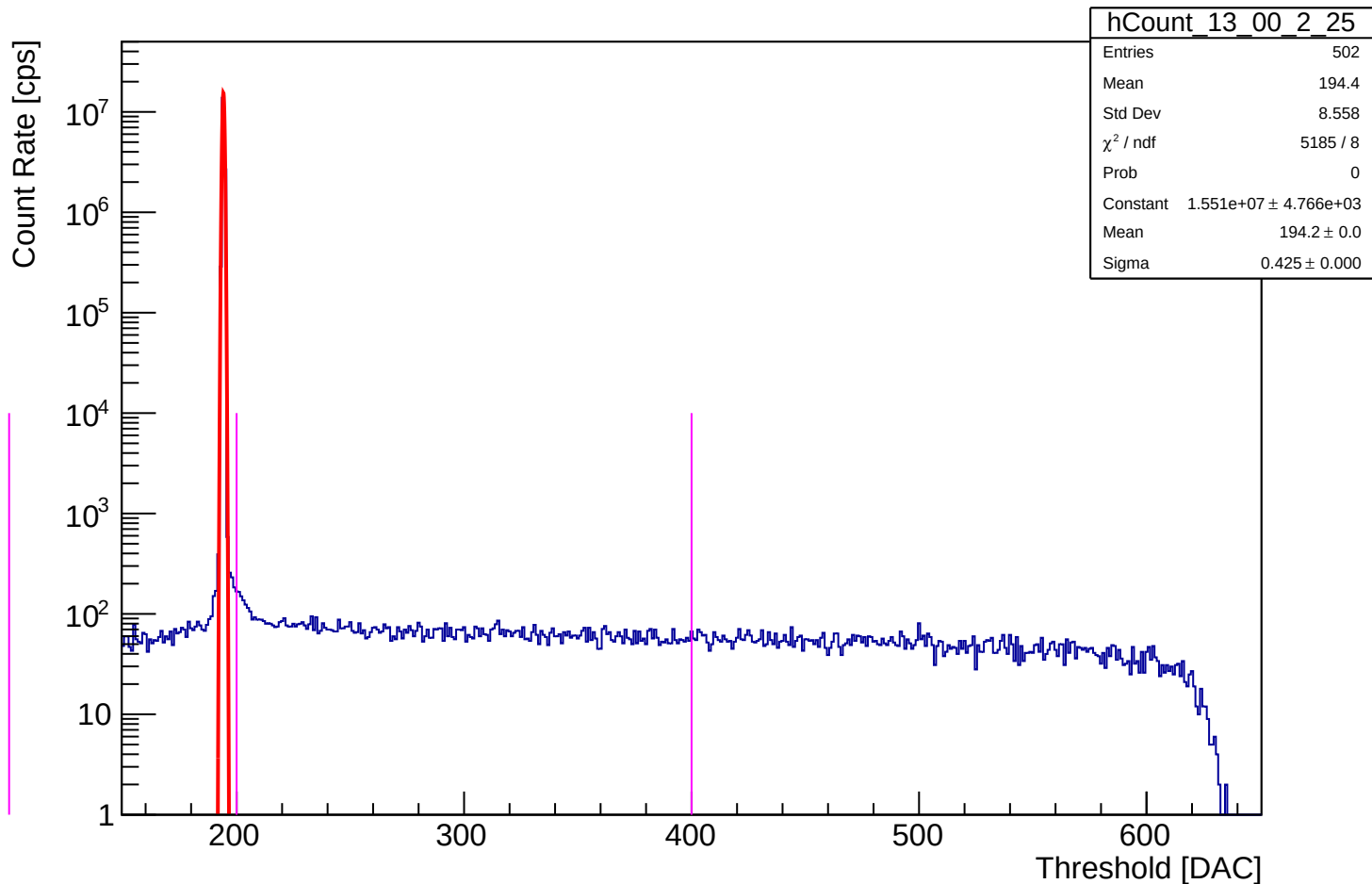
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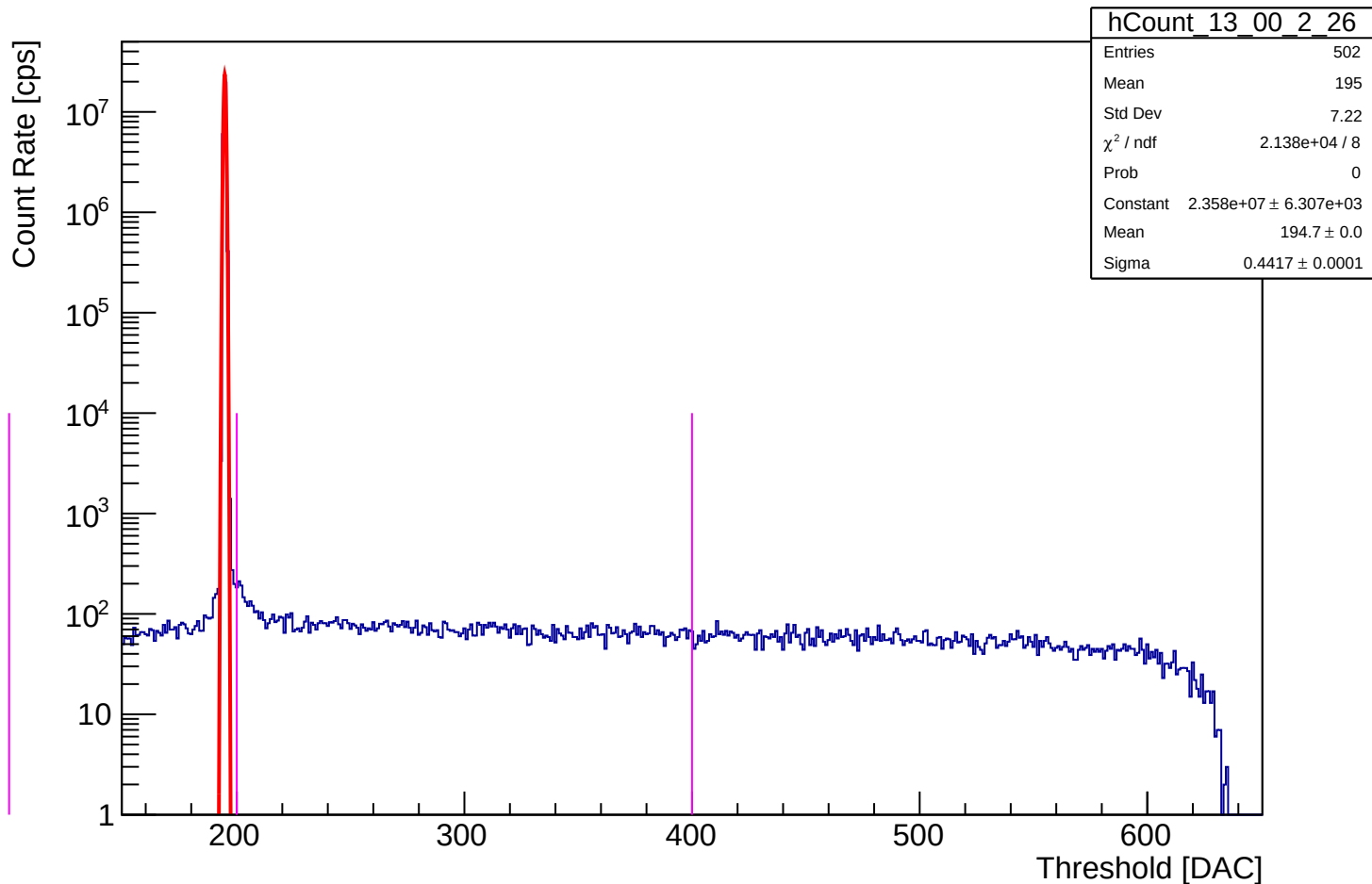
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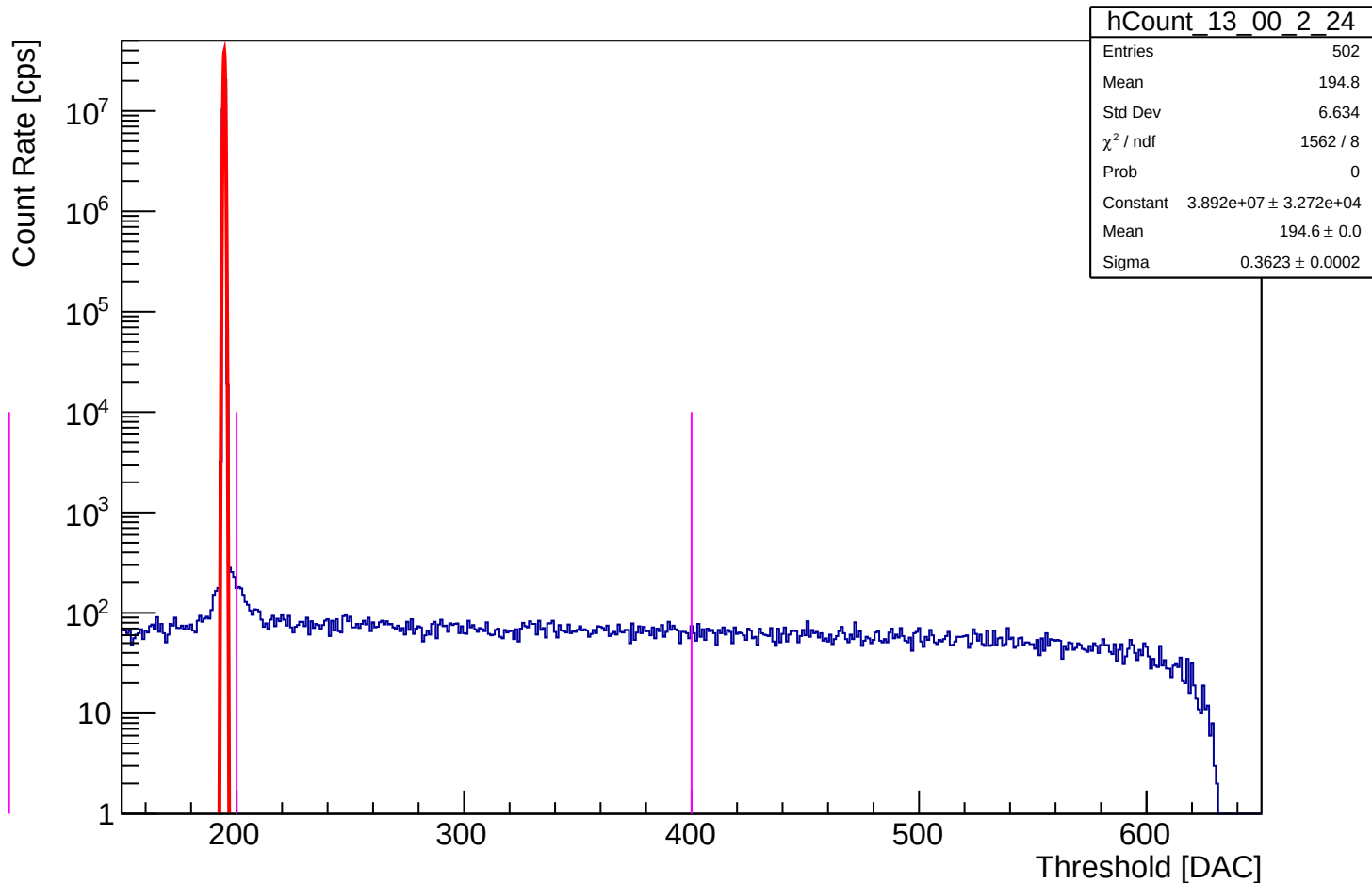
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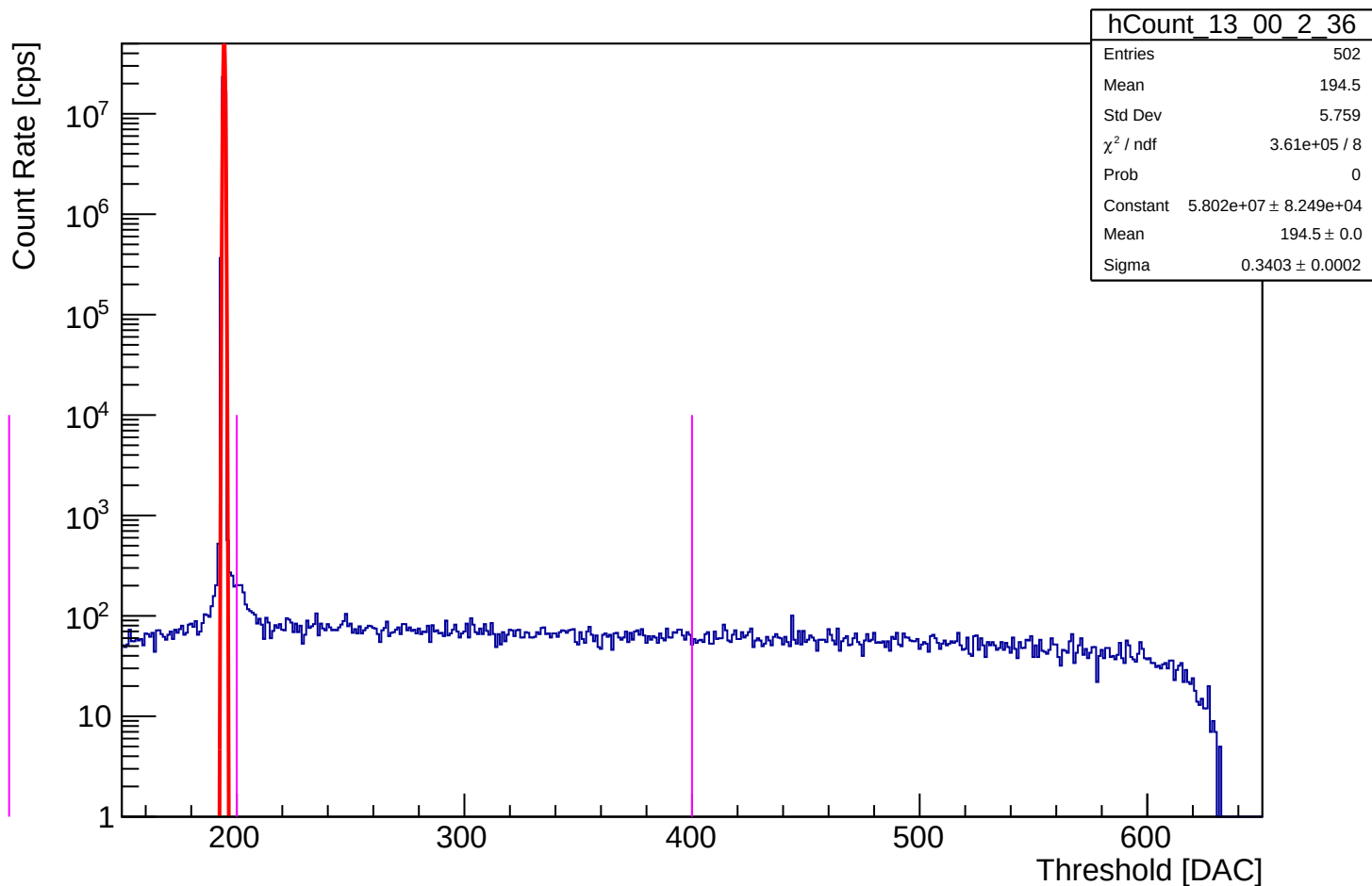
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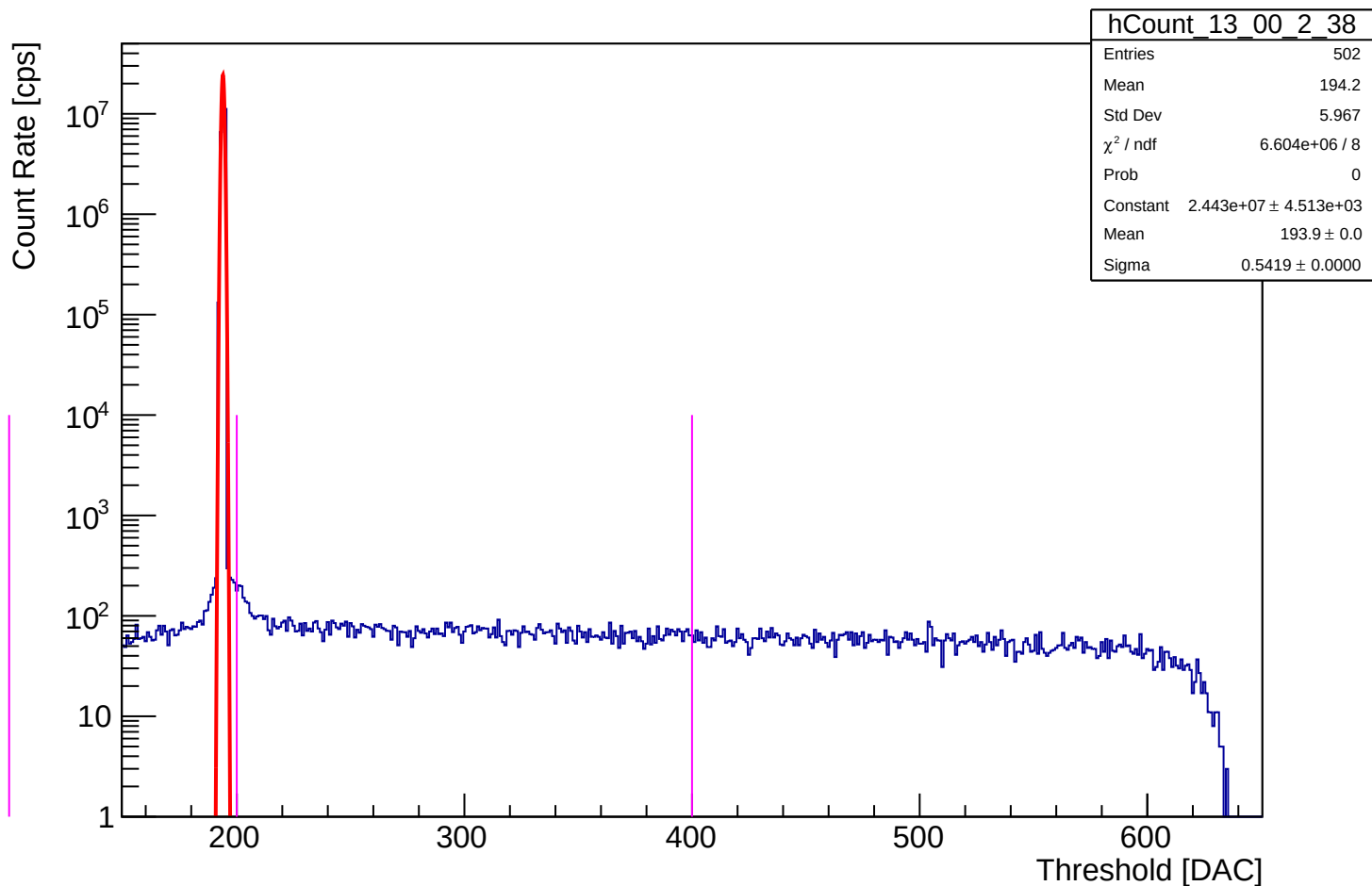
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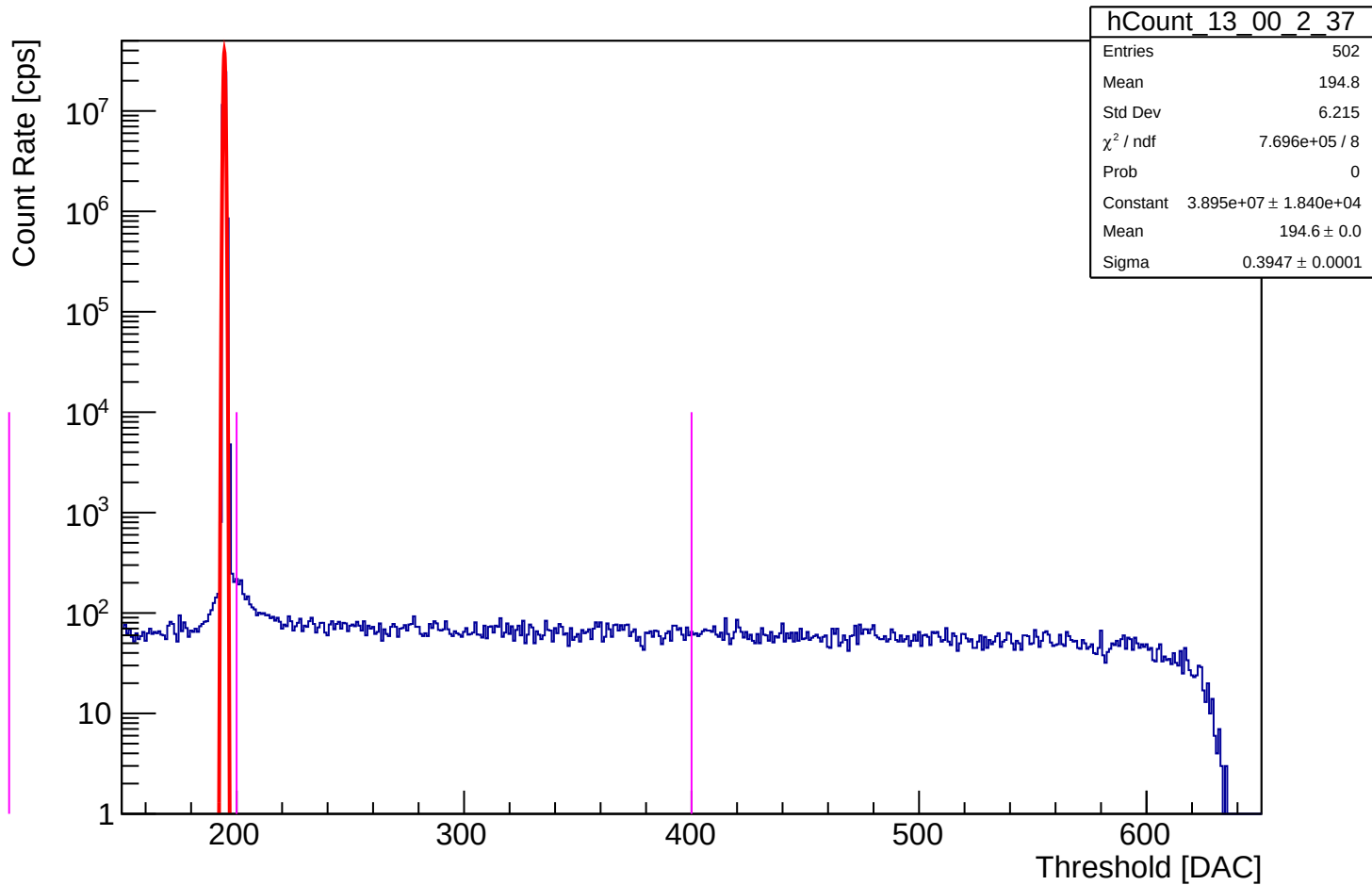
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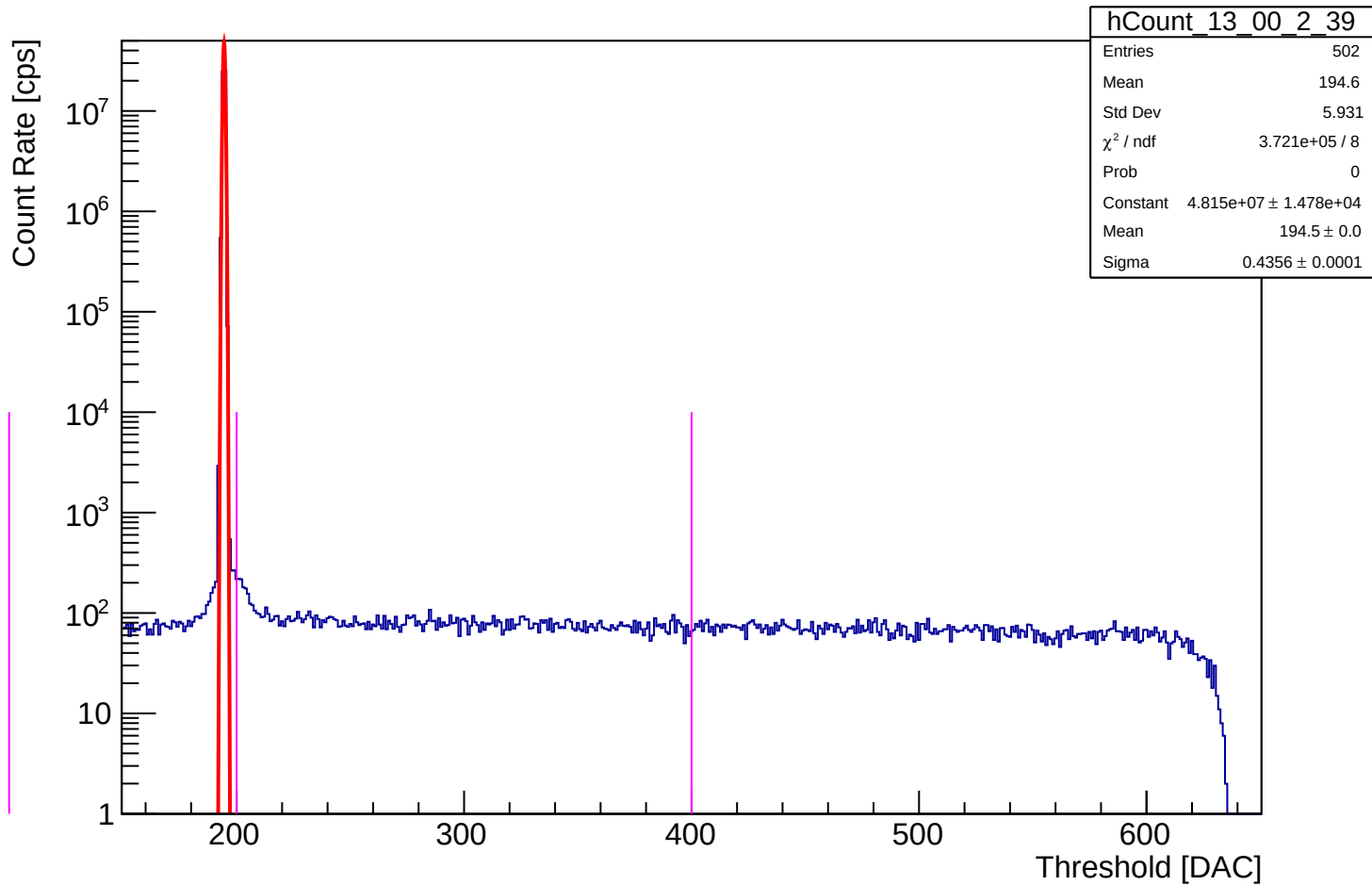
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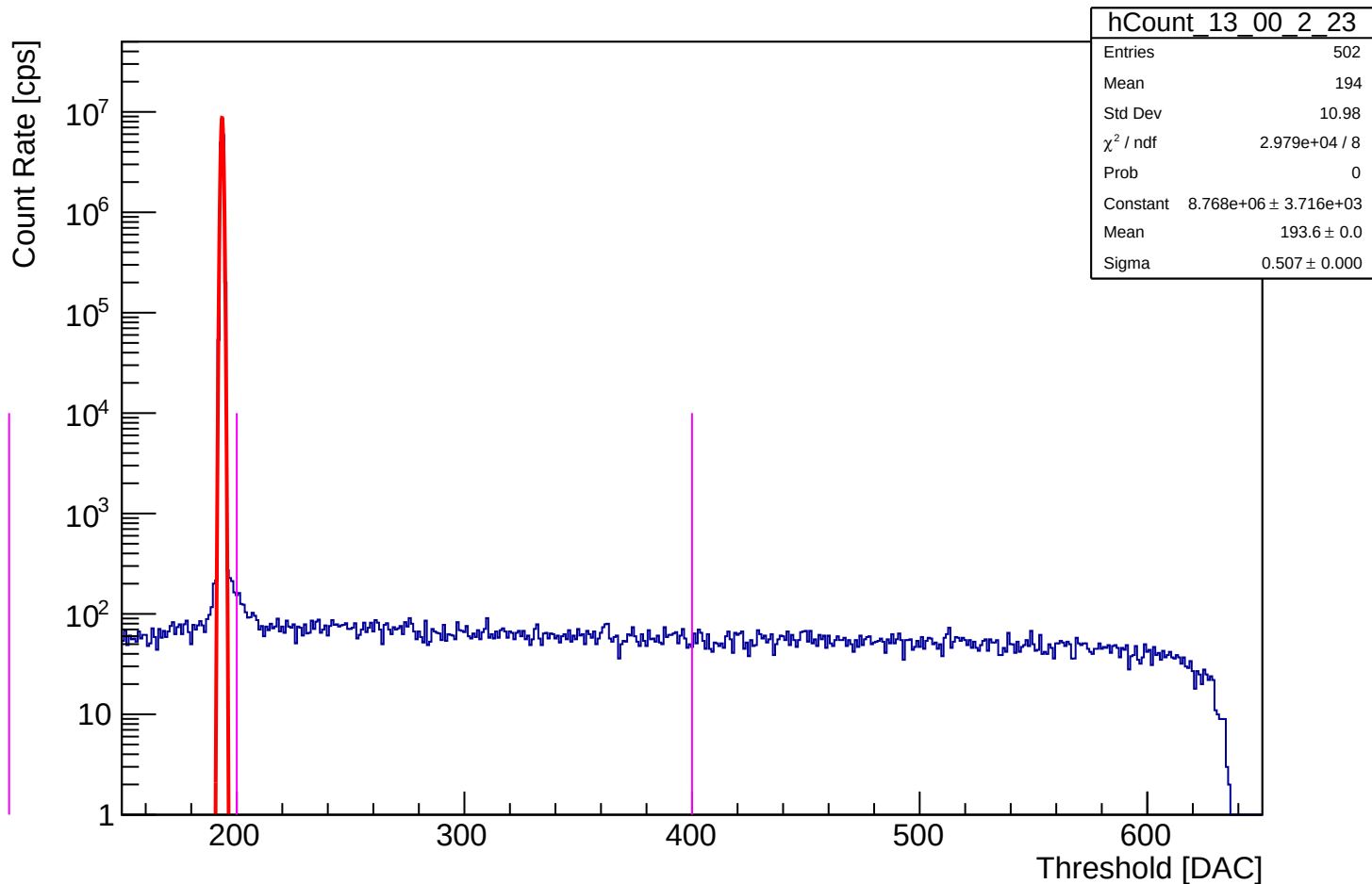
Row 1 Tile 1 Pmt 3 Pixel 15 Slot 13 Fiber 0 Asic 2 Channel 37



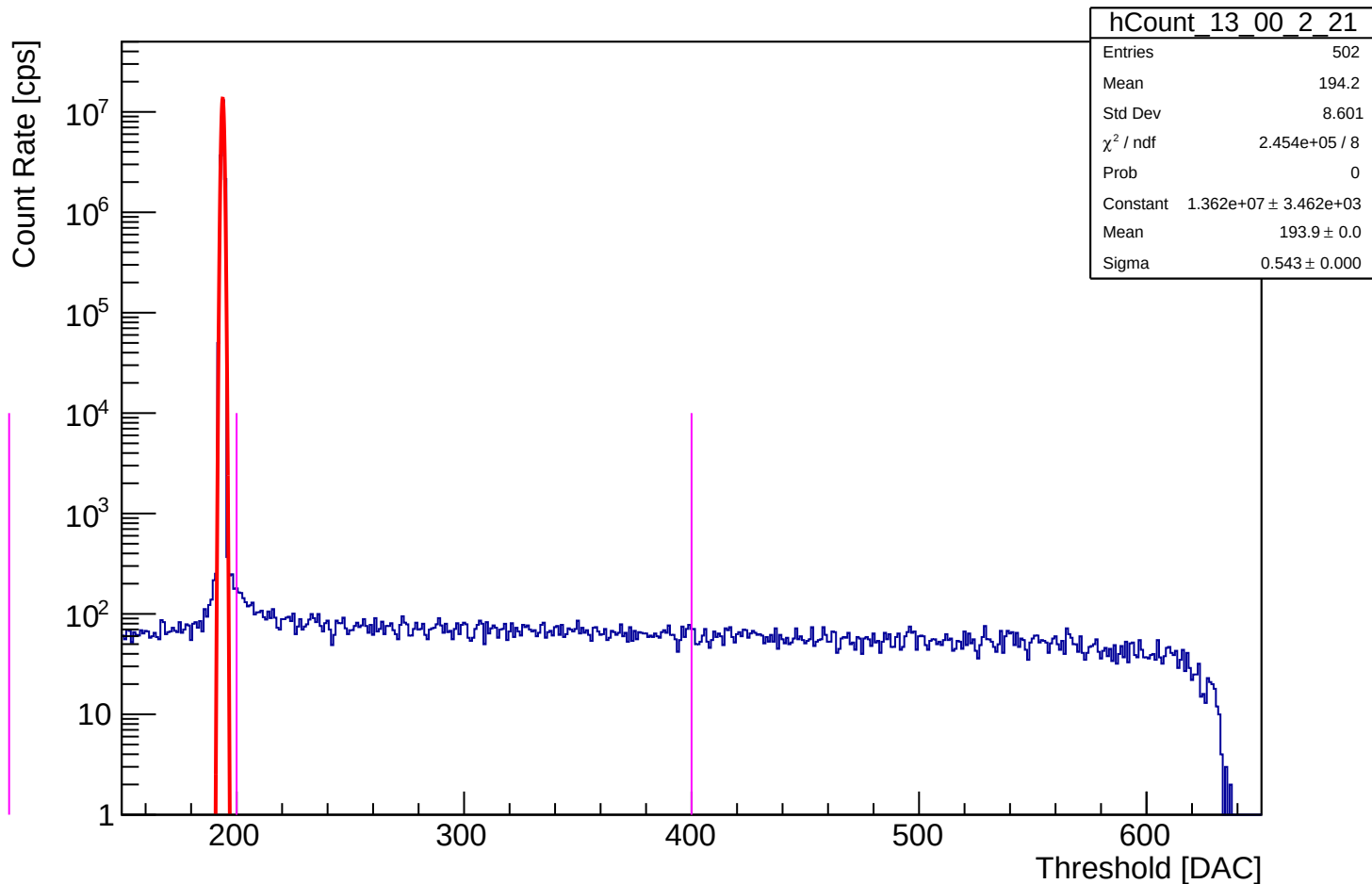
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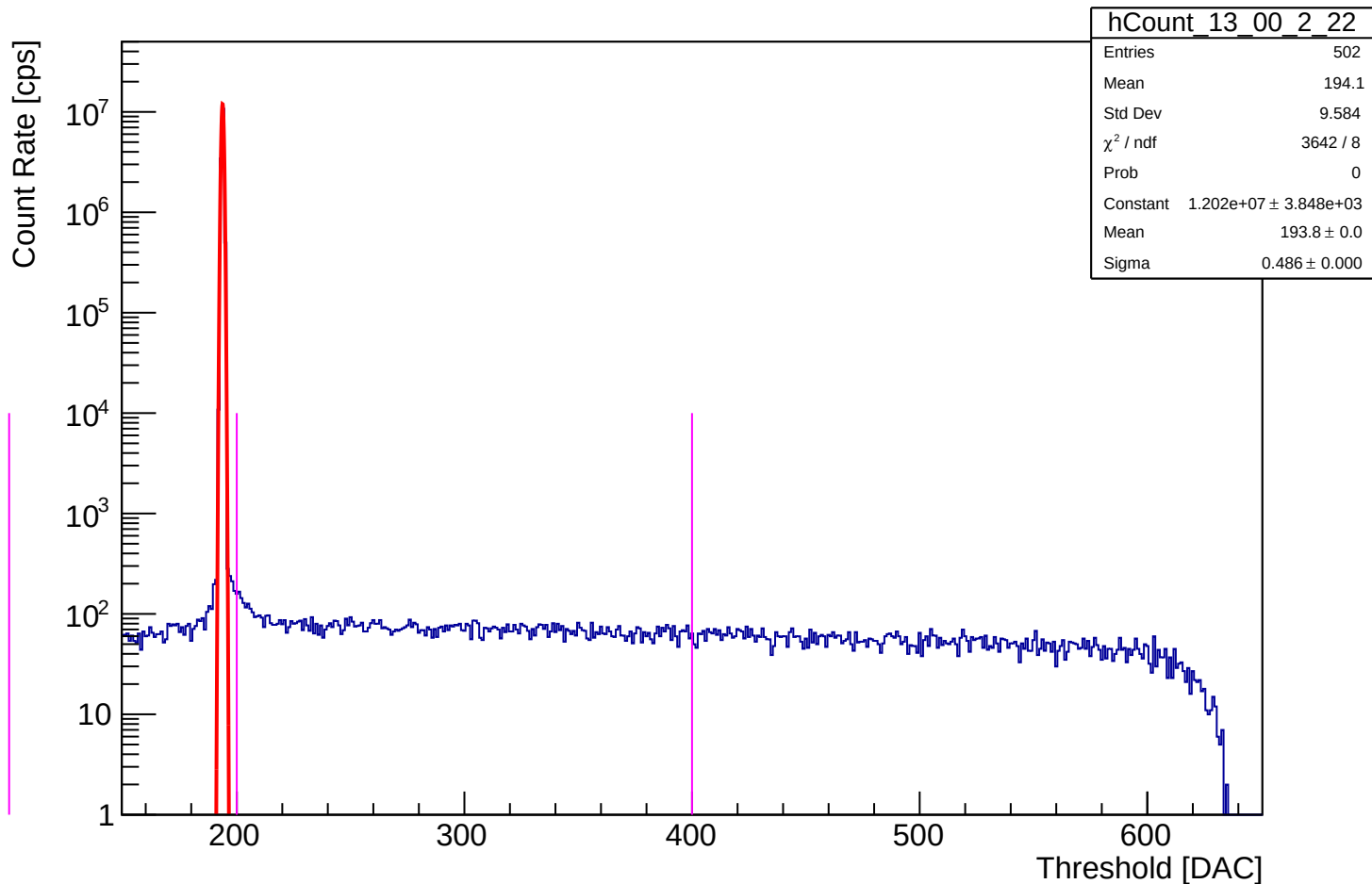
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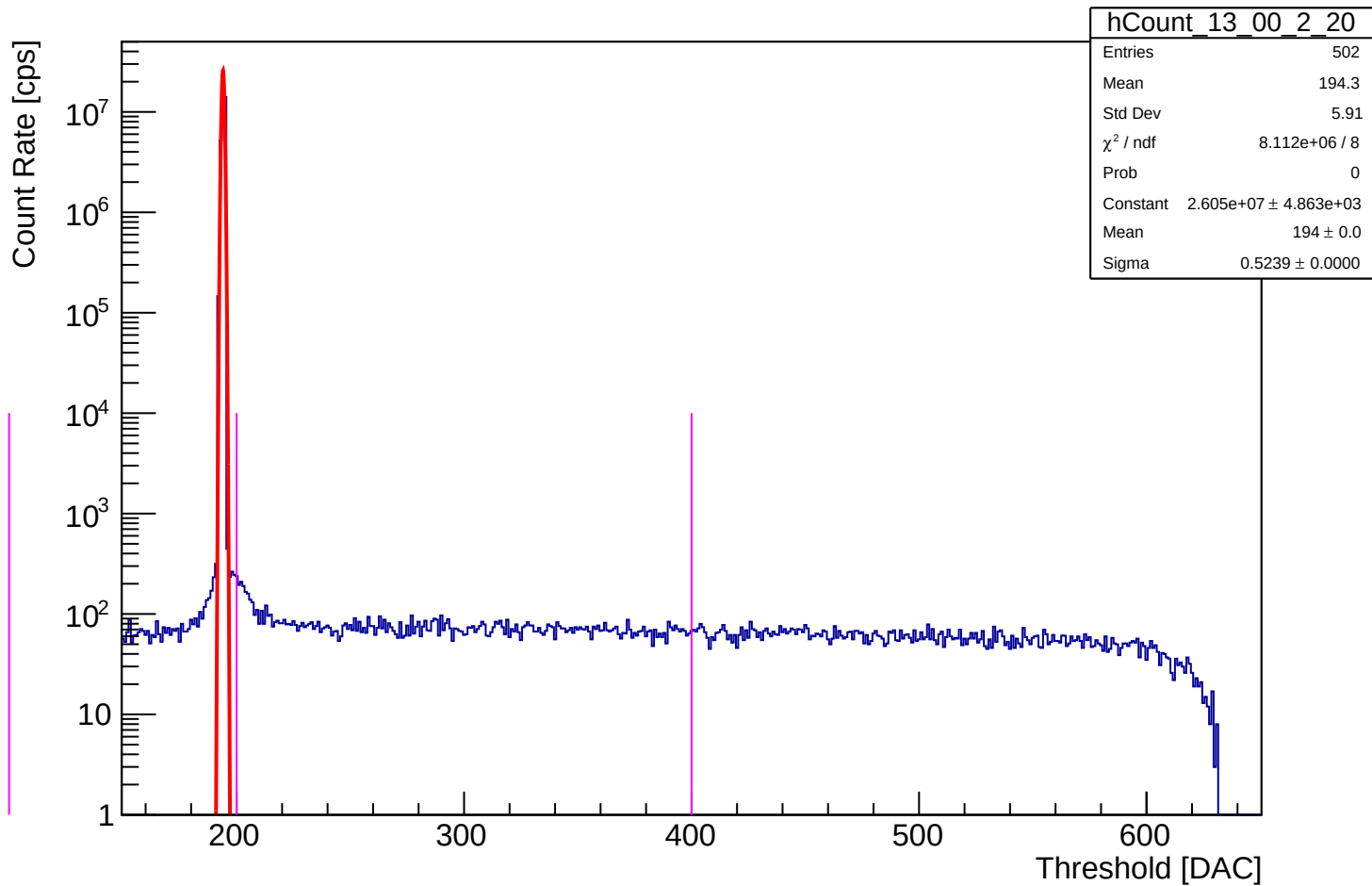
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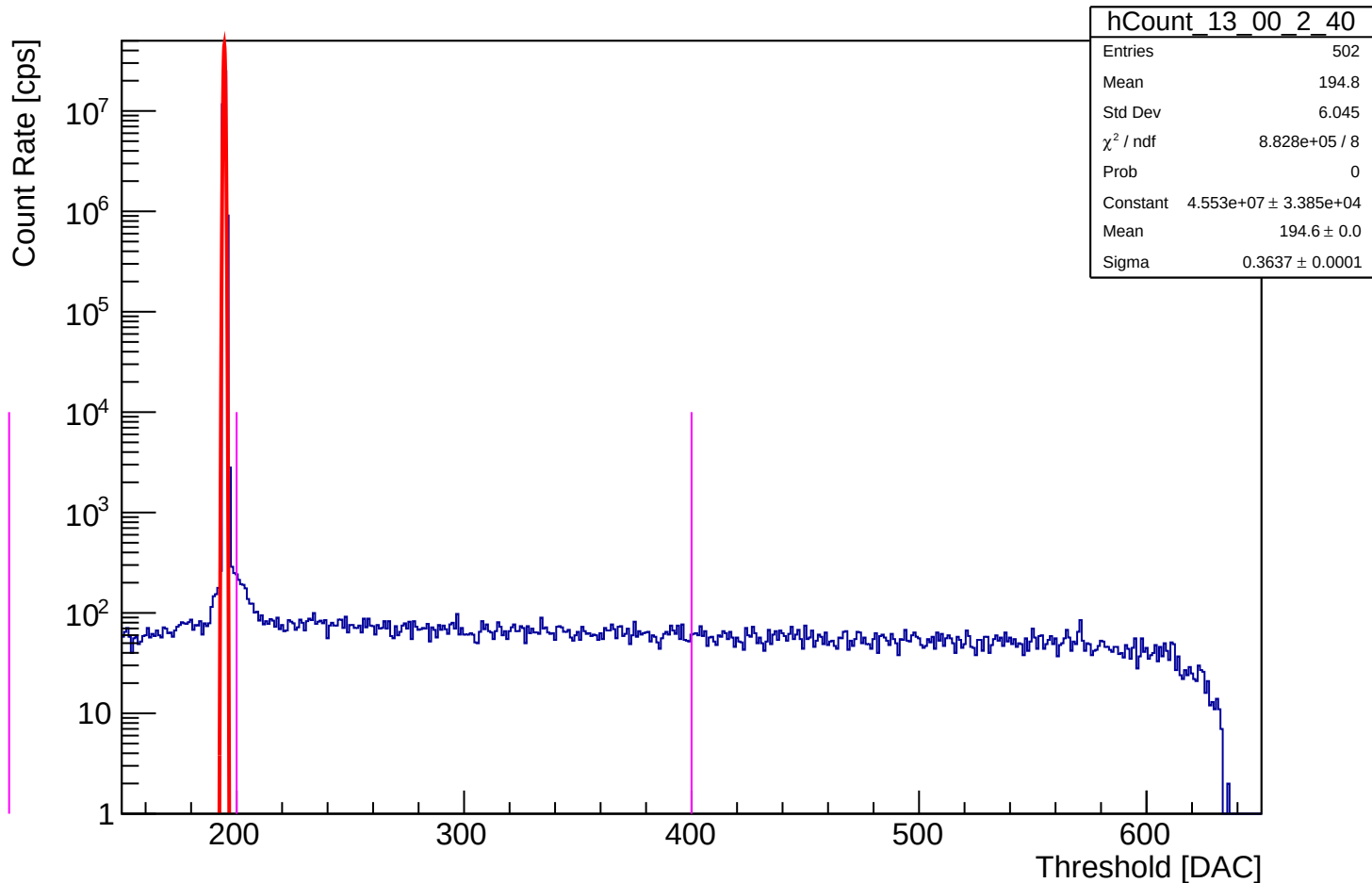
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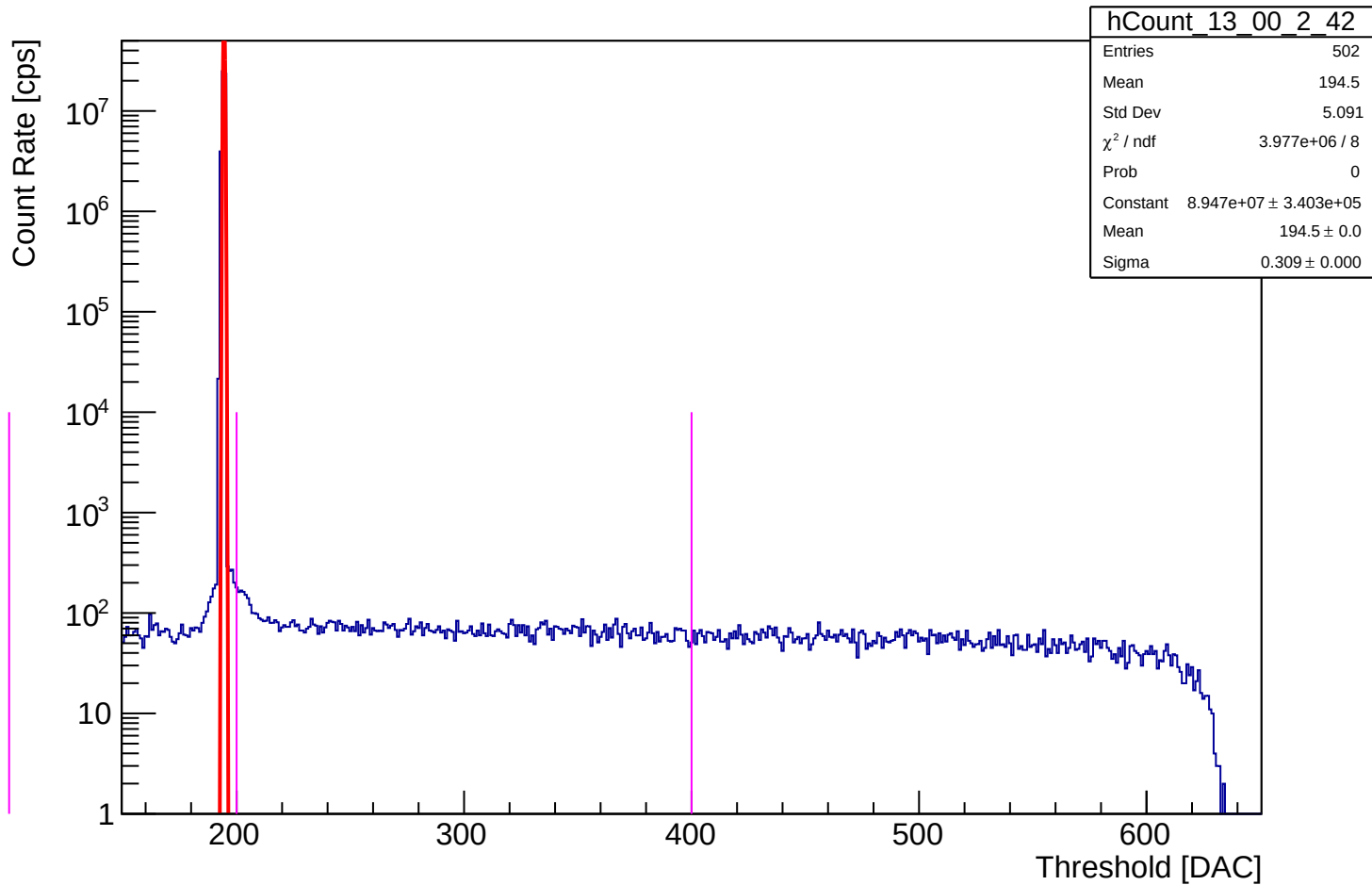
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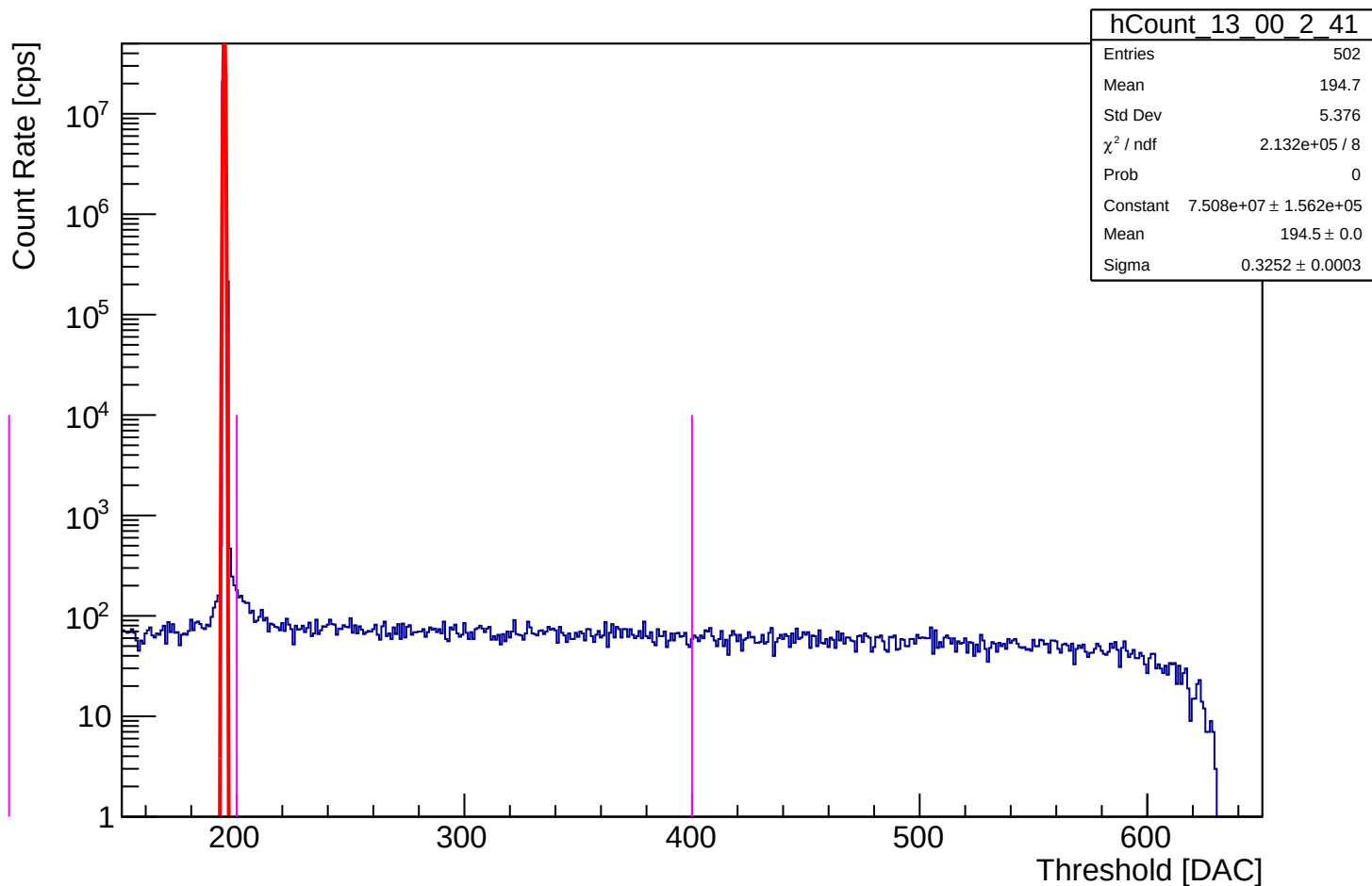
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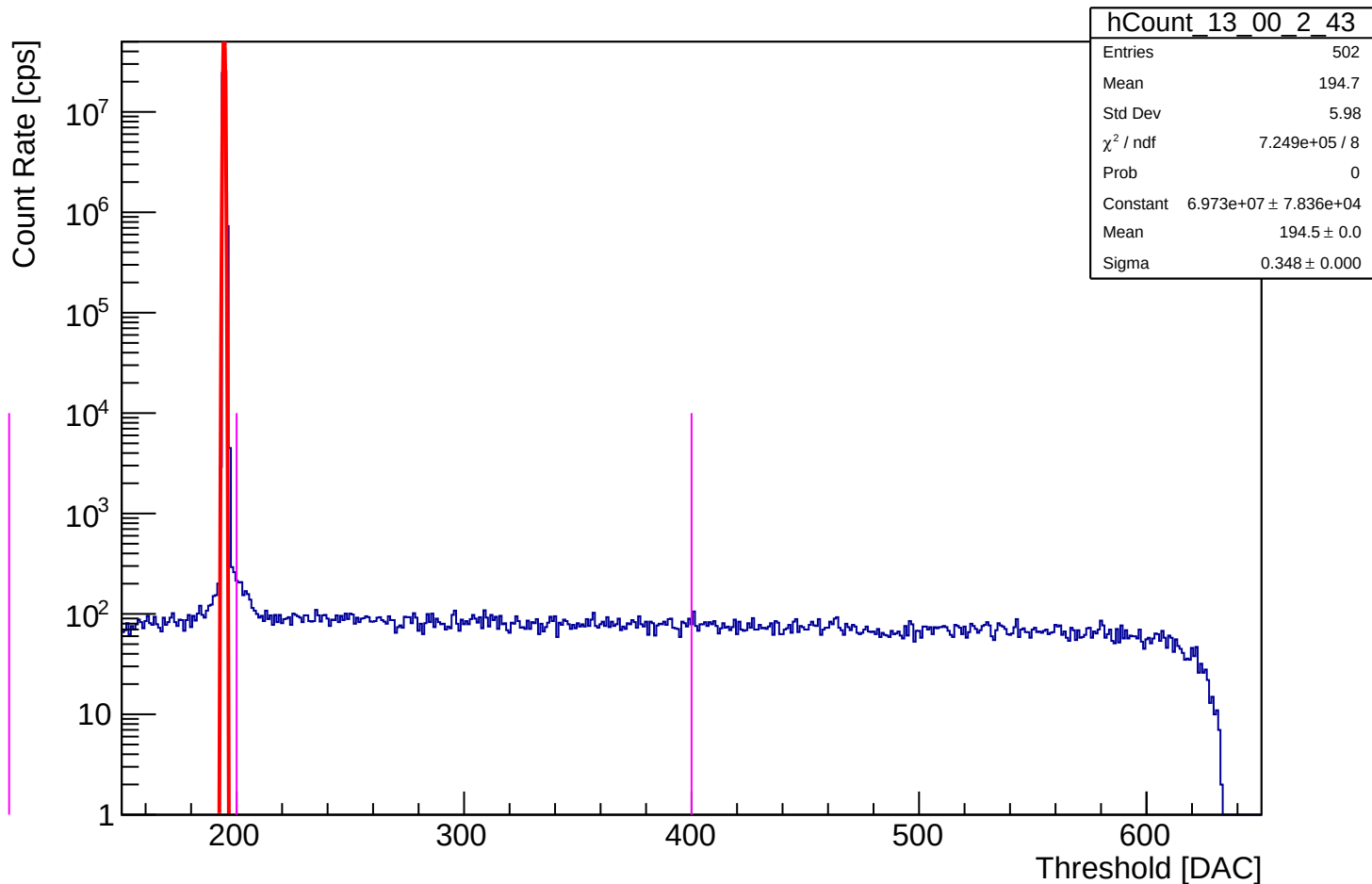
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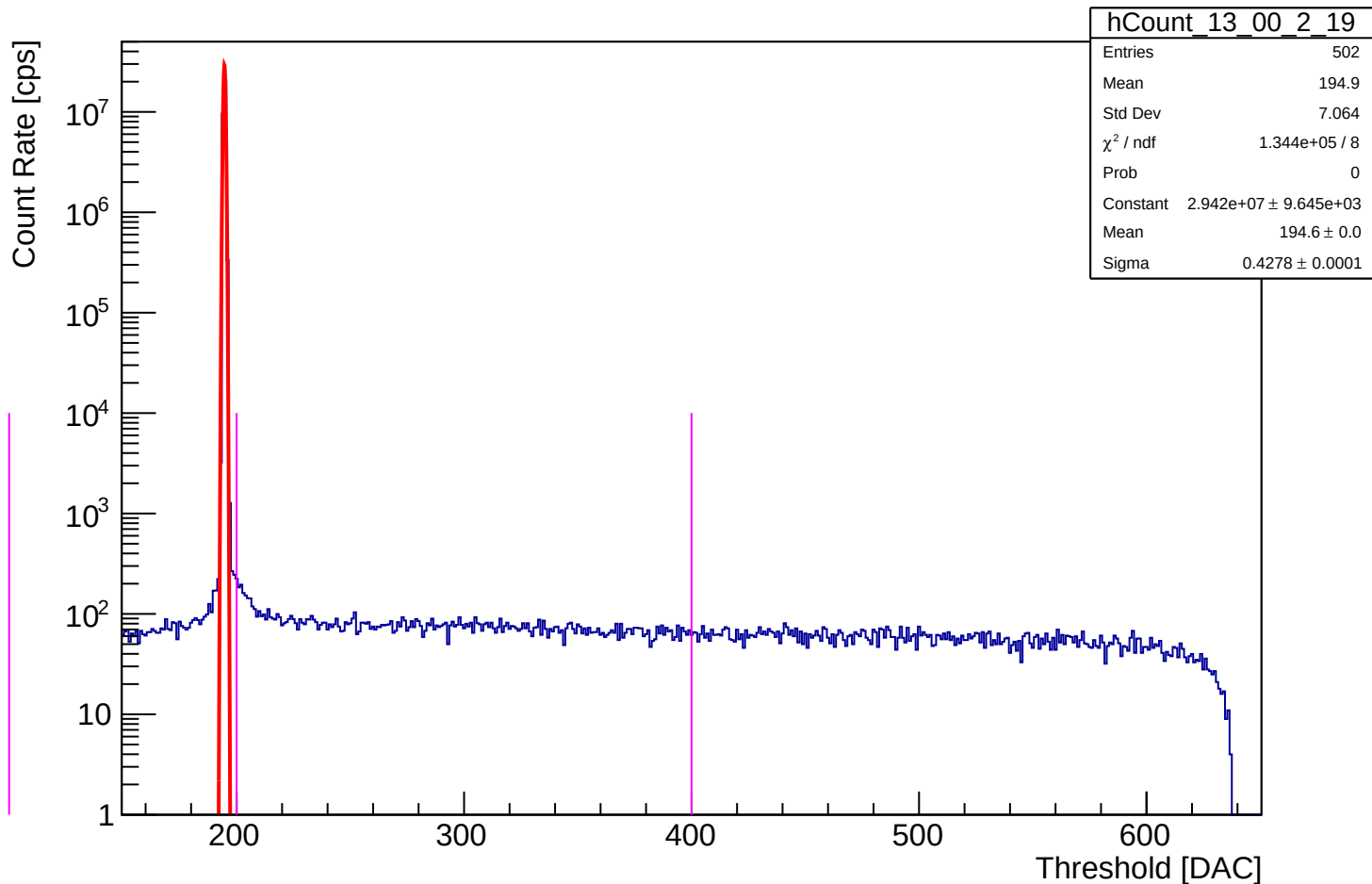
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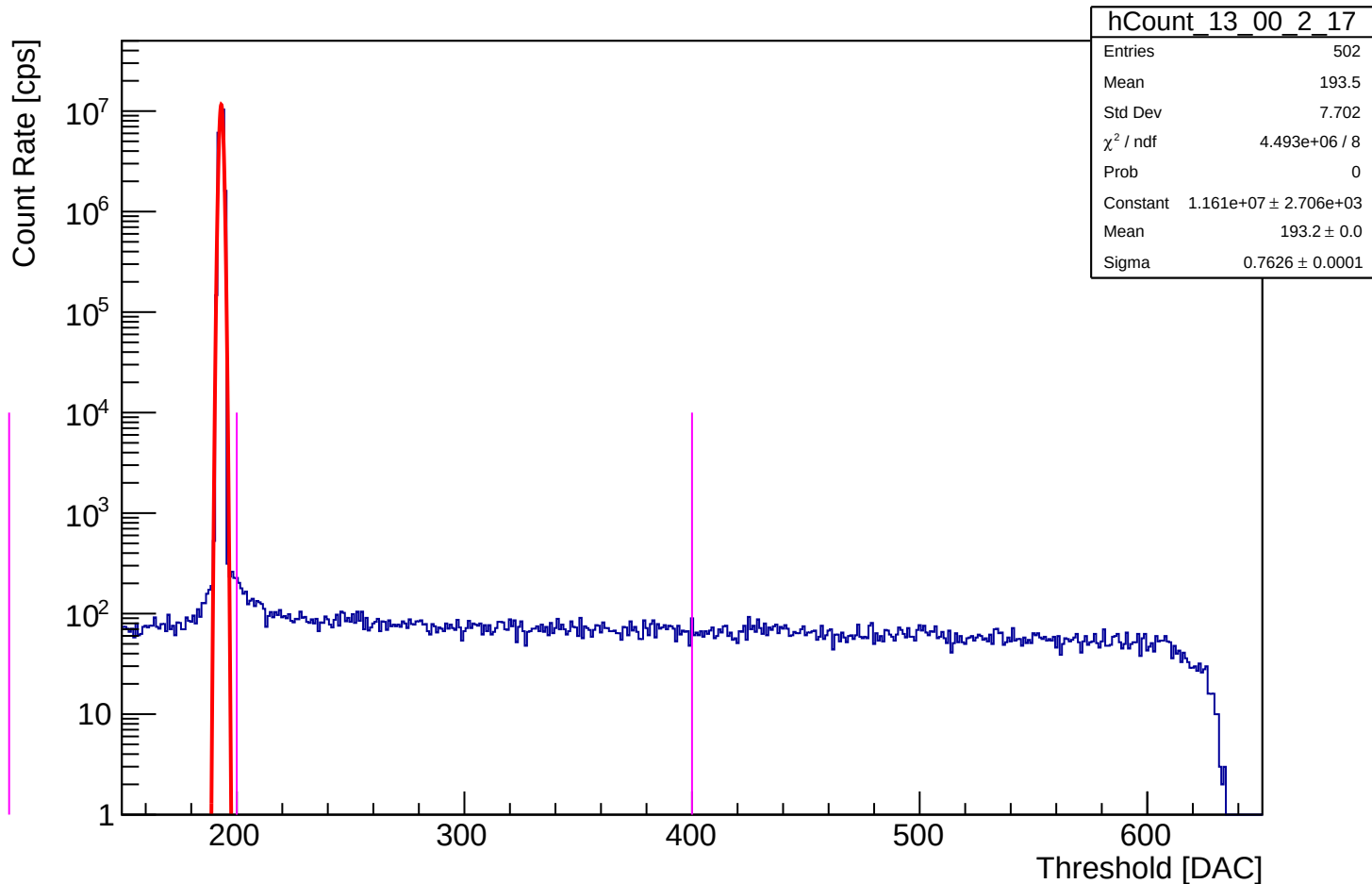
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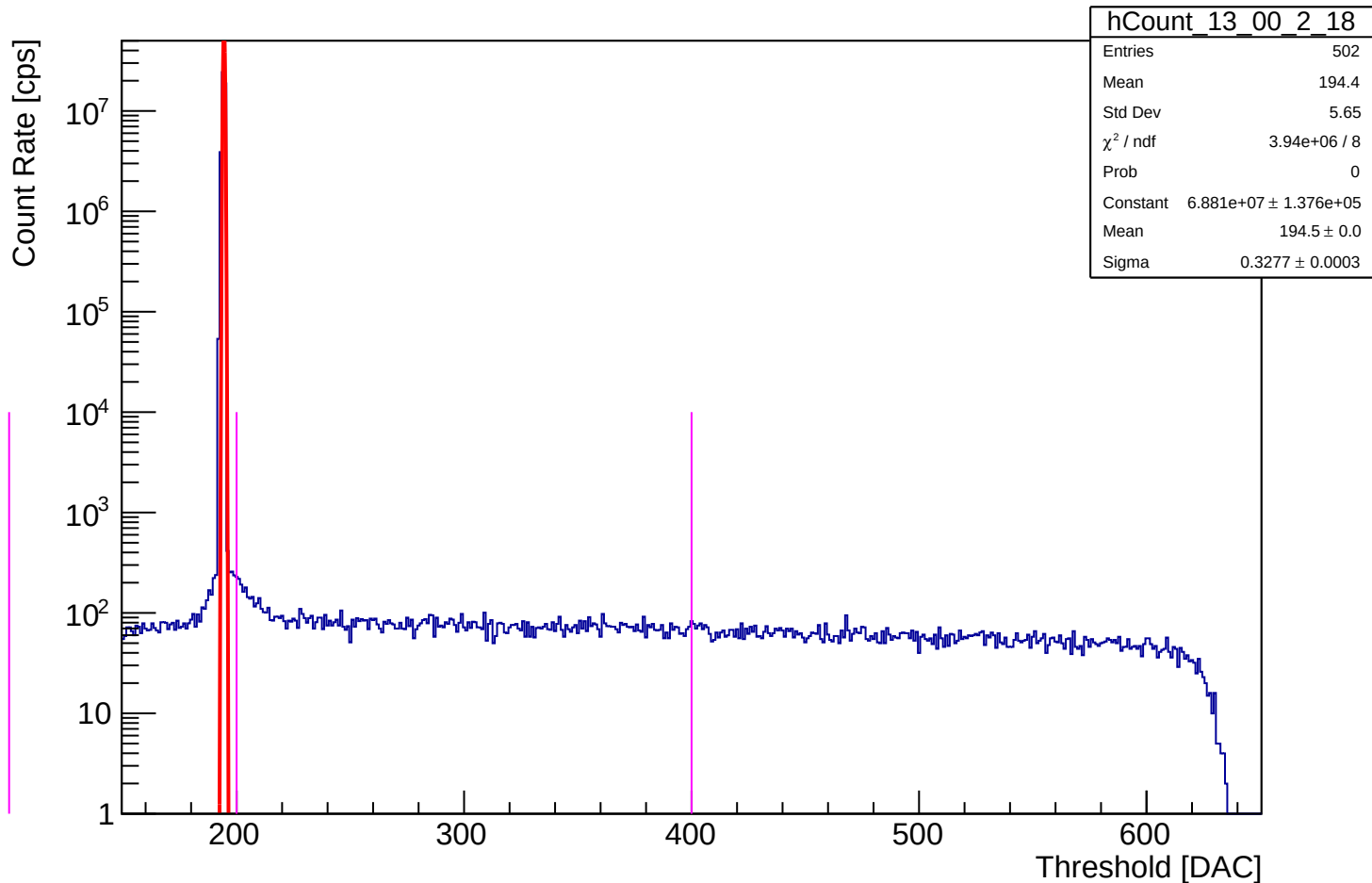
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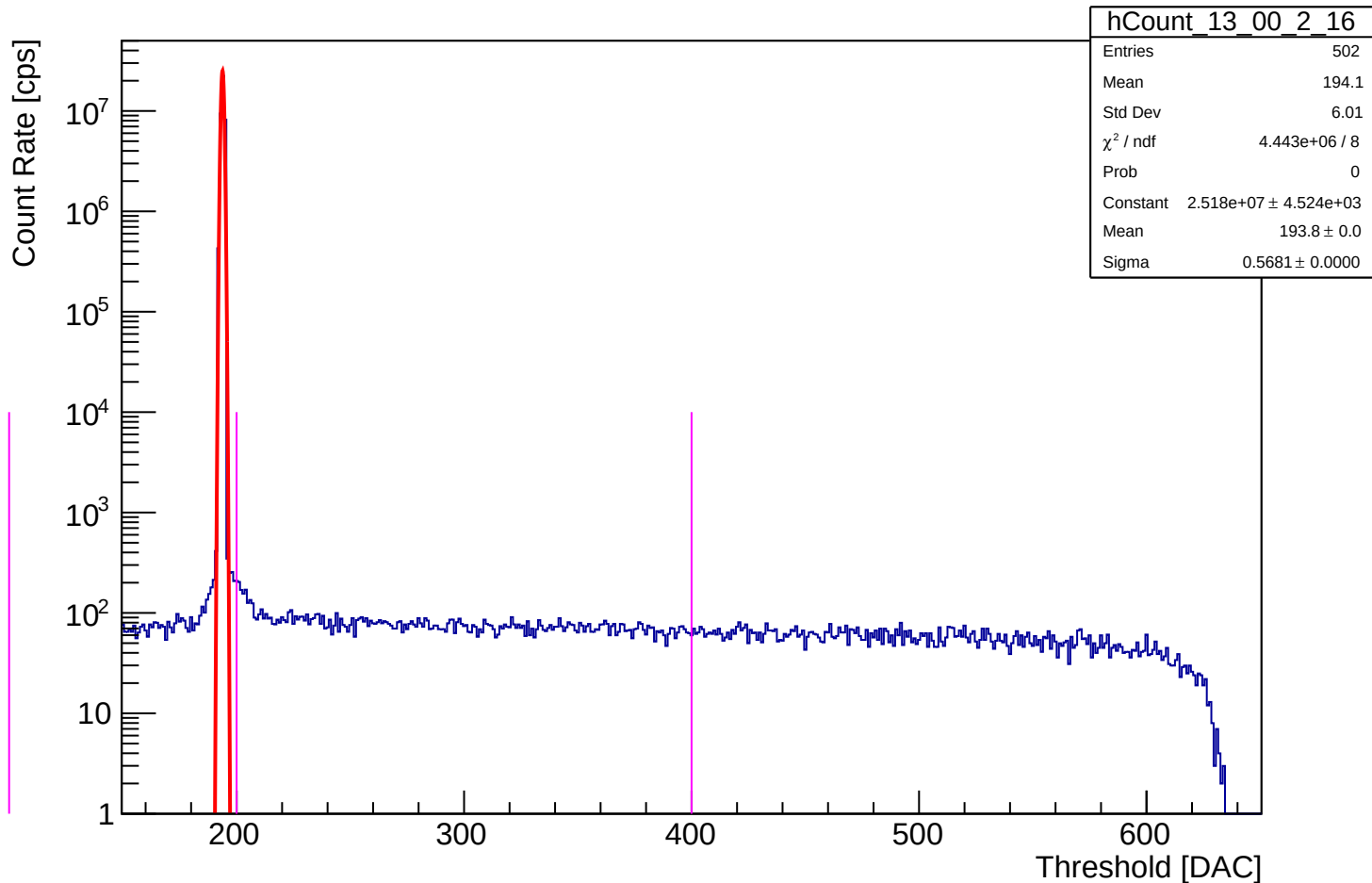
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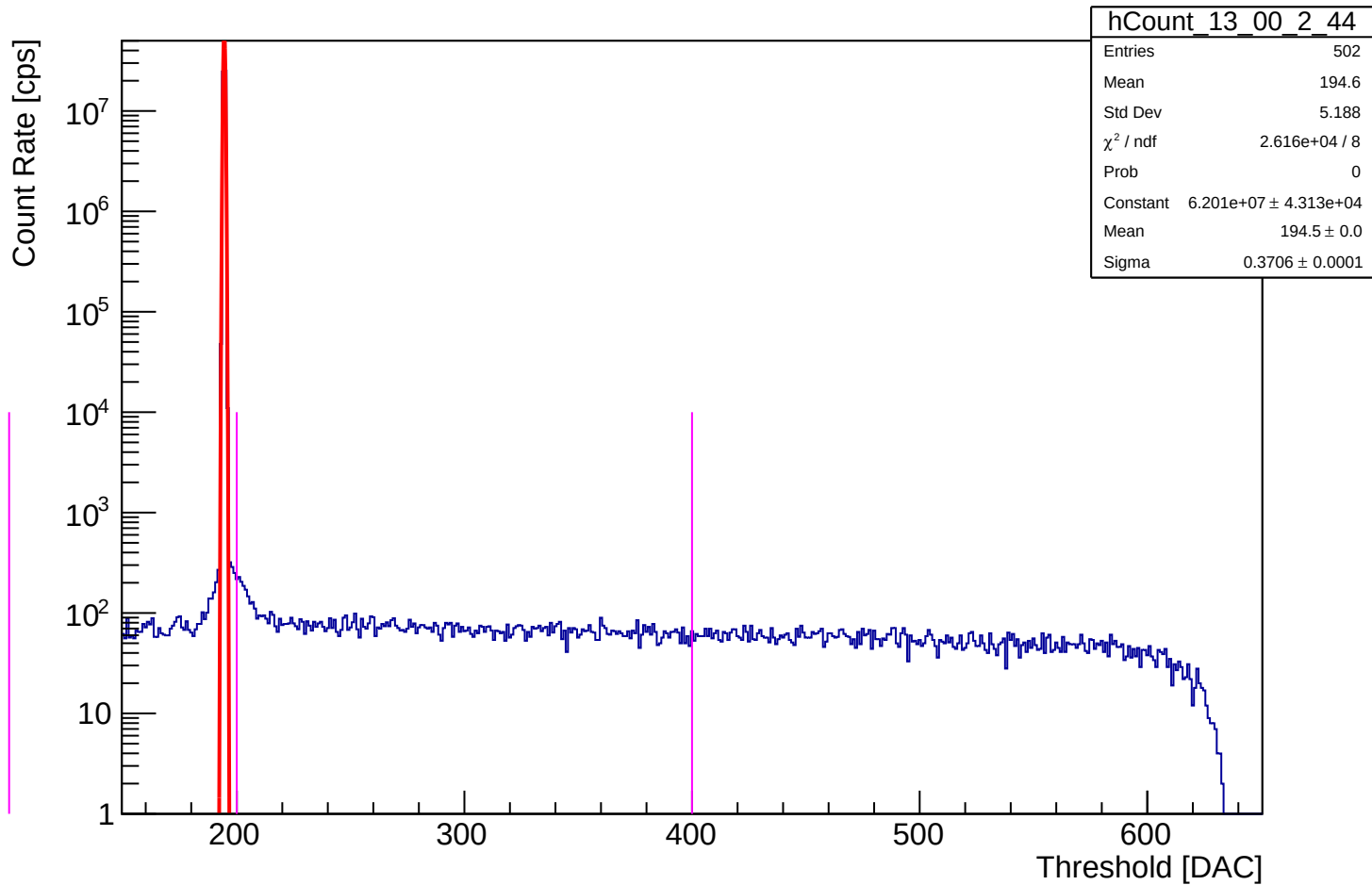
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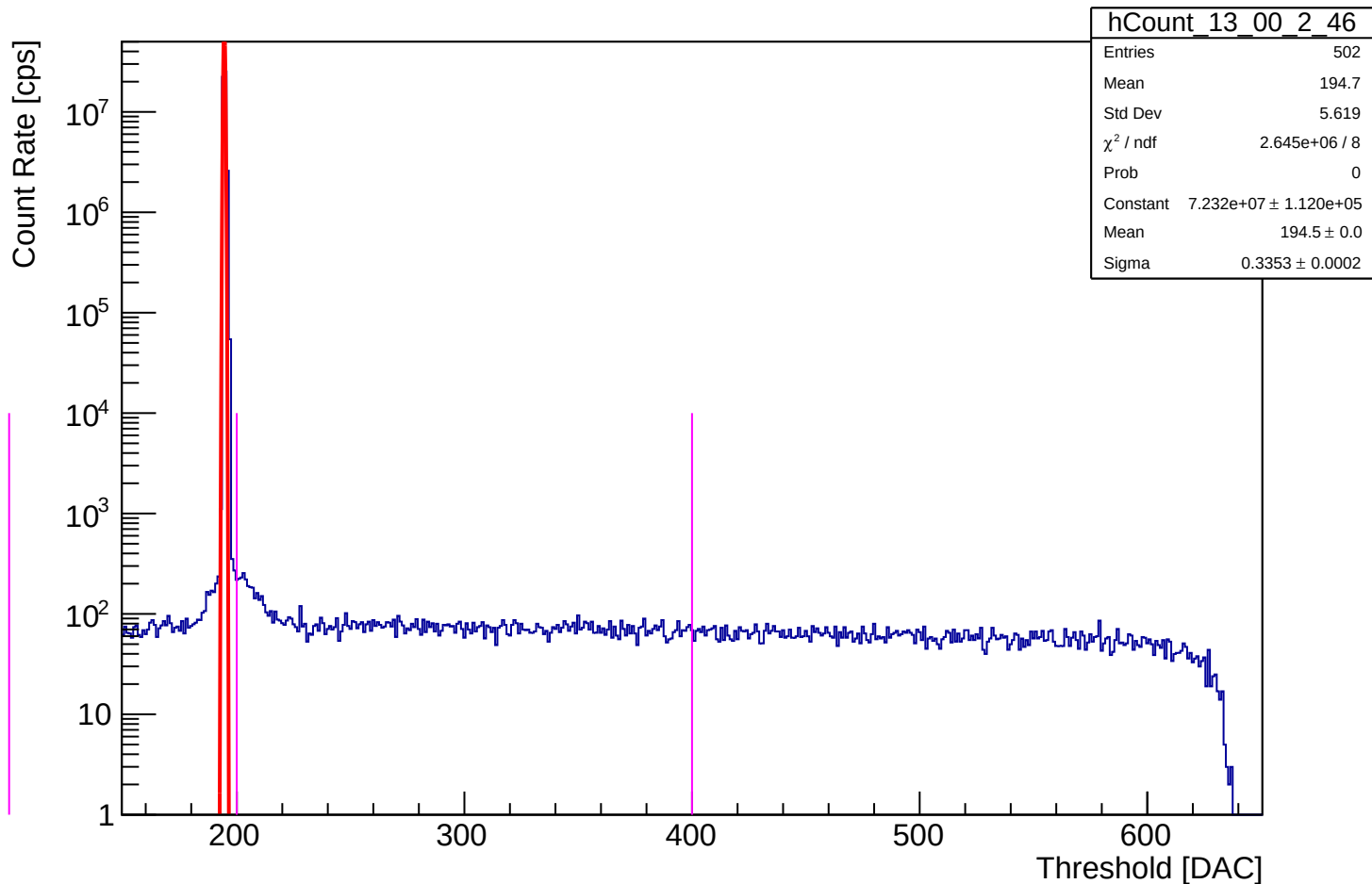
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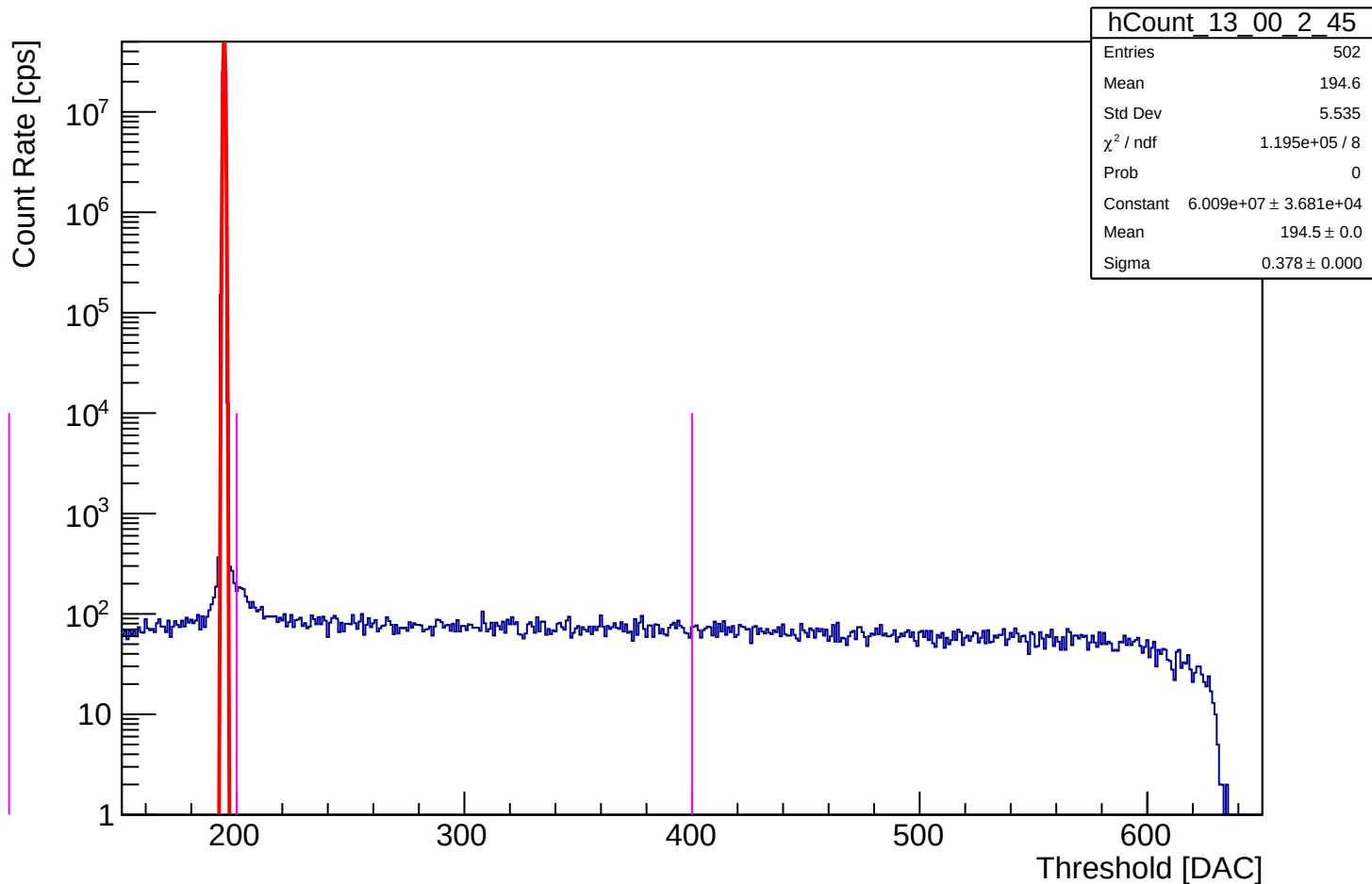
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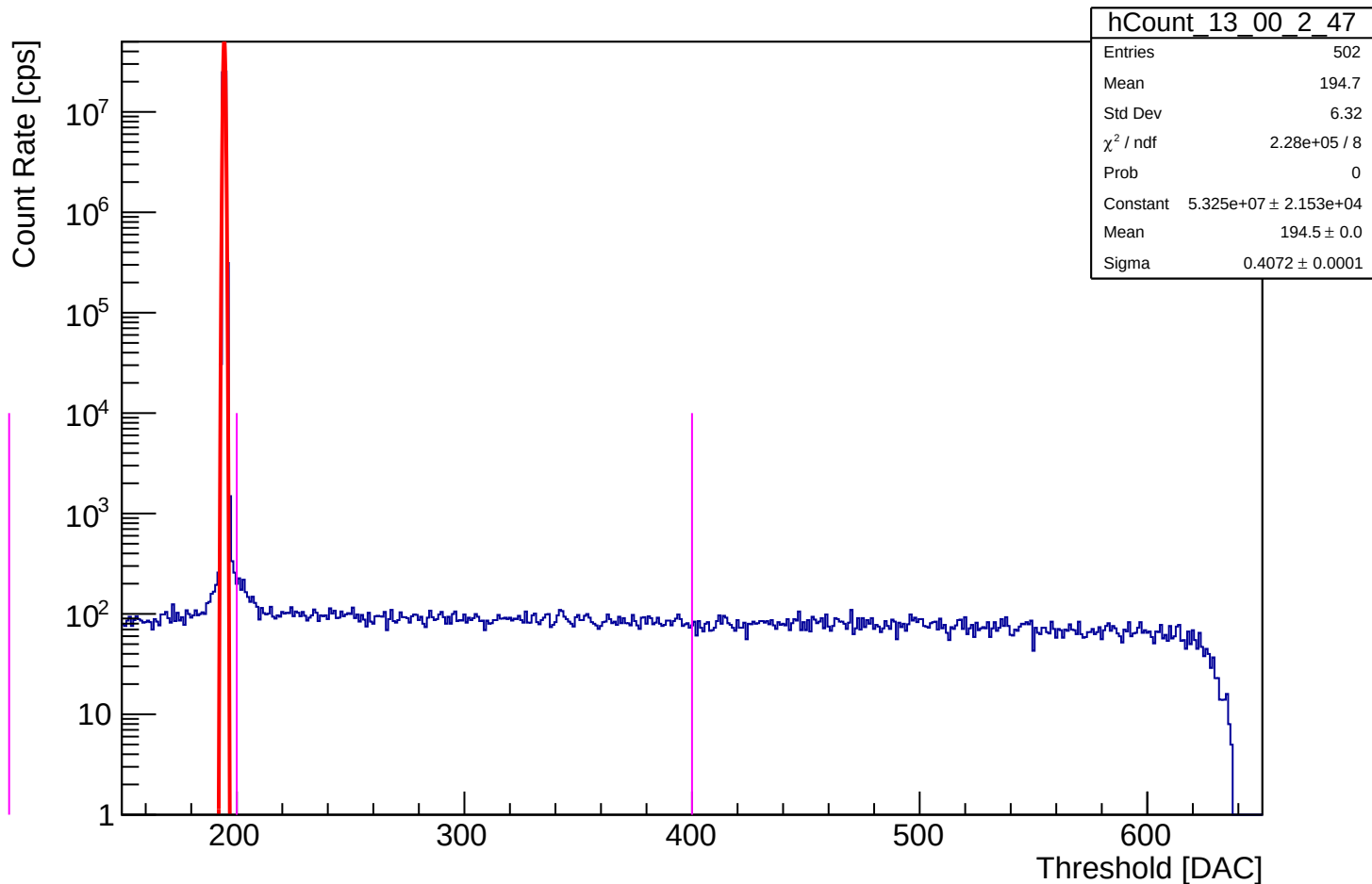
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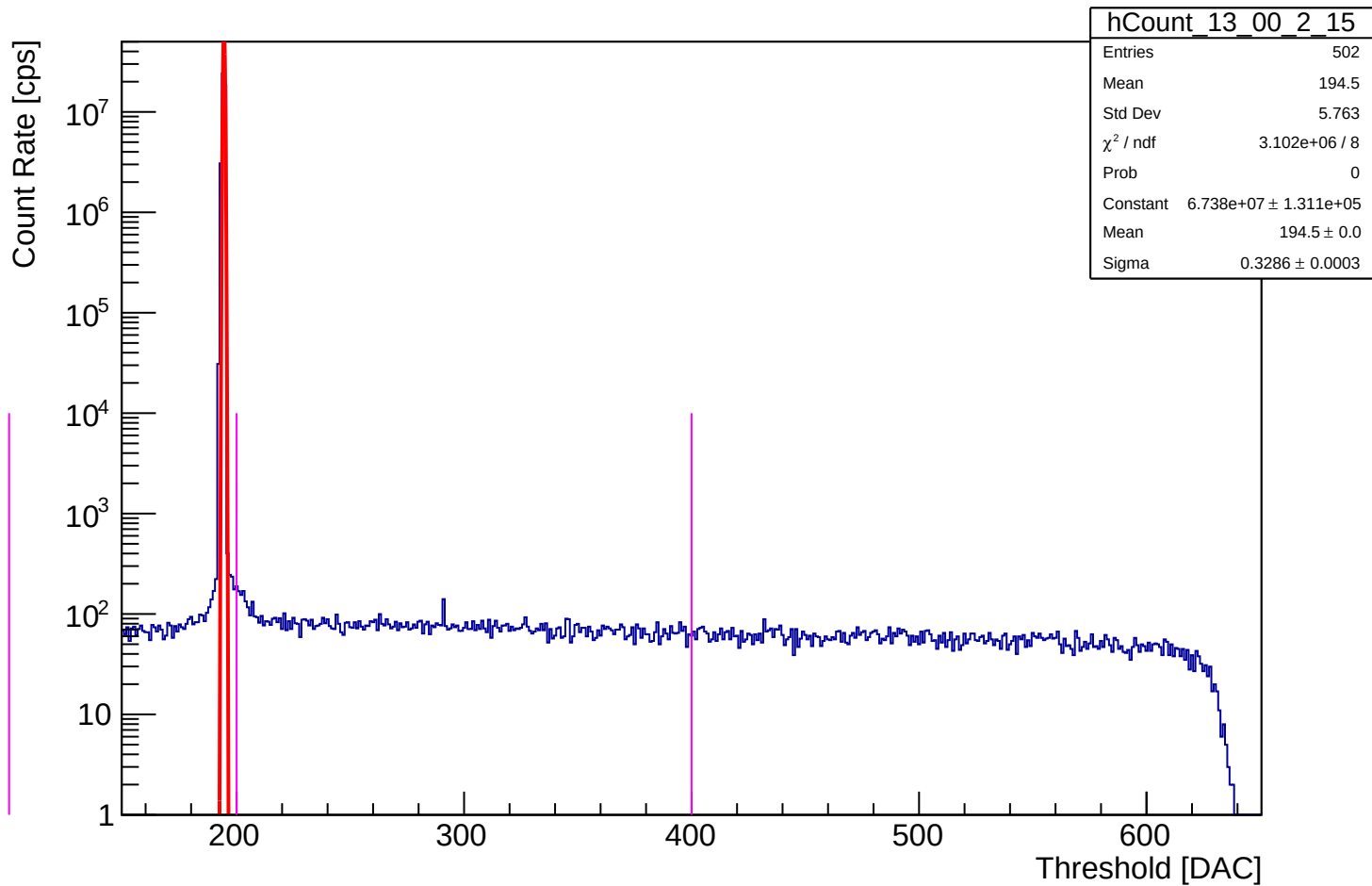
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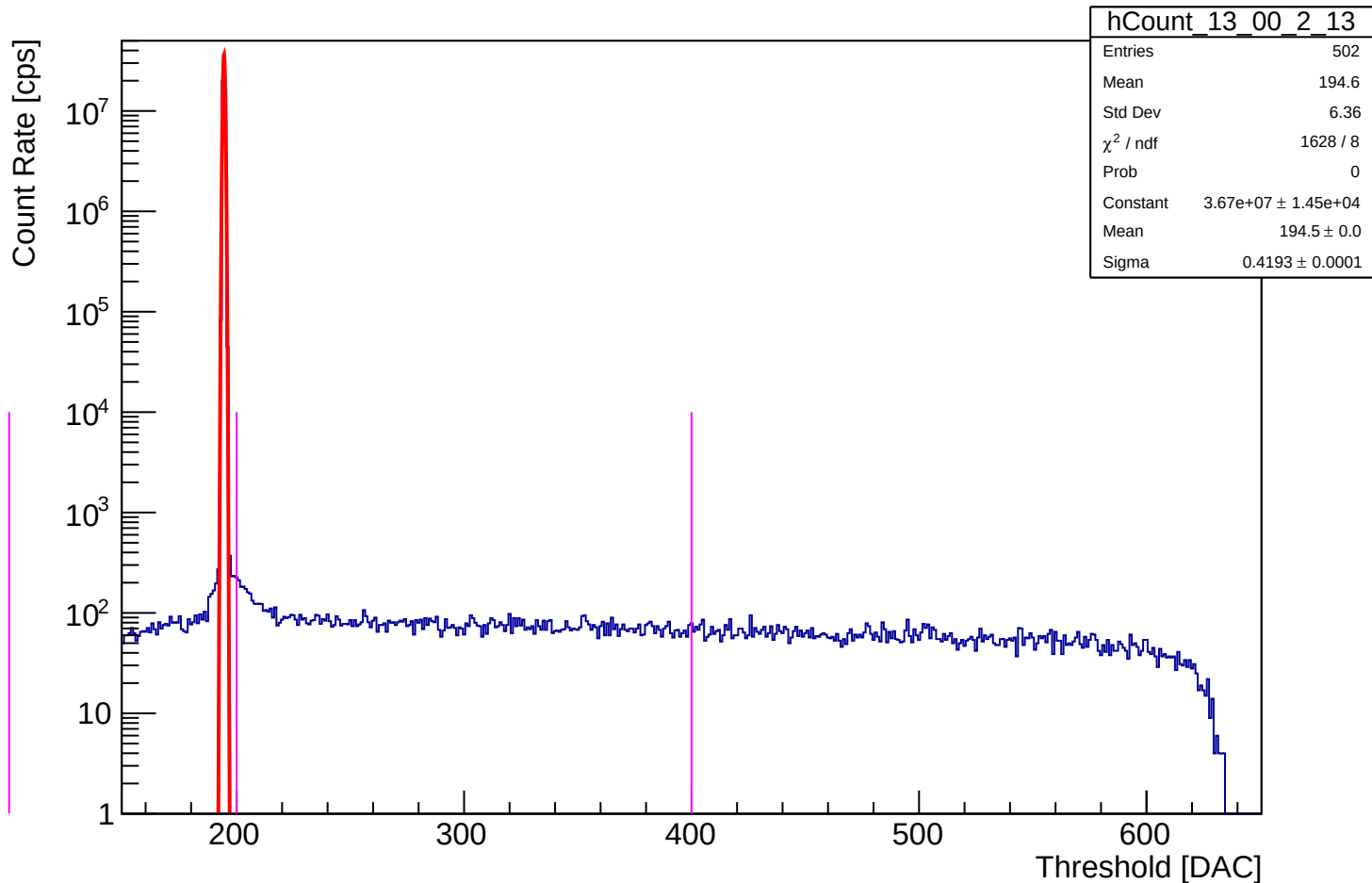
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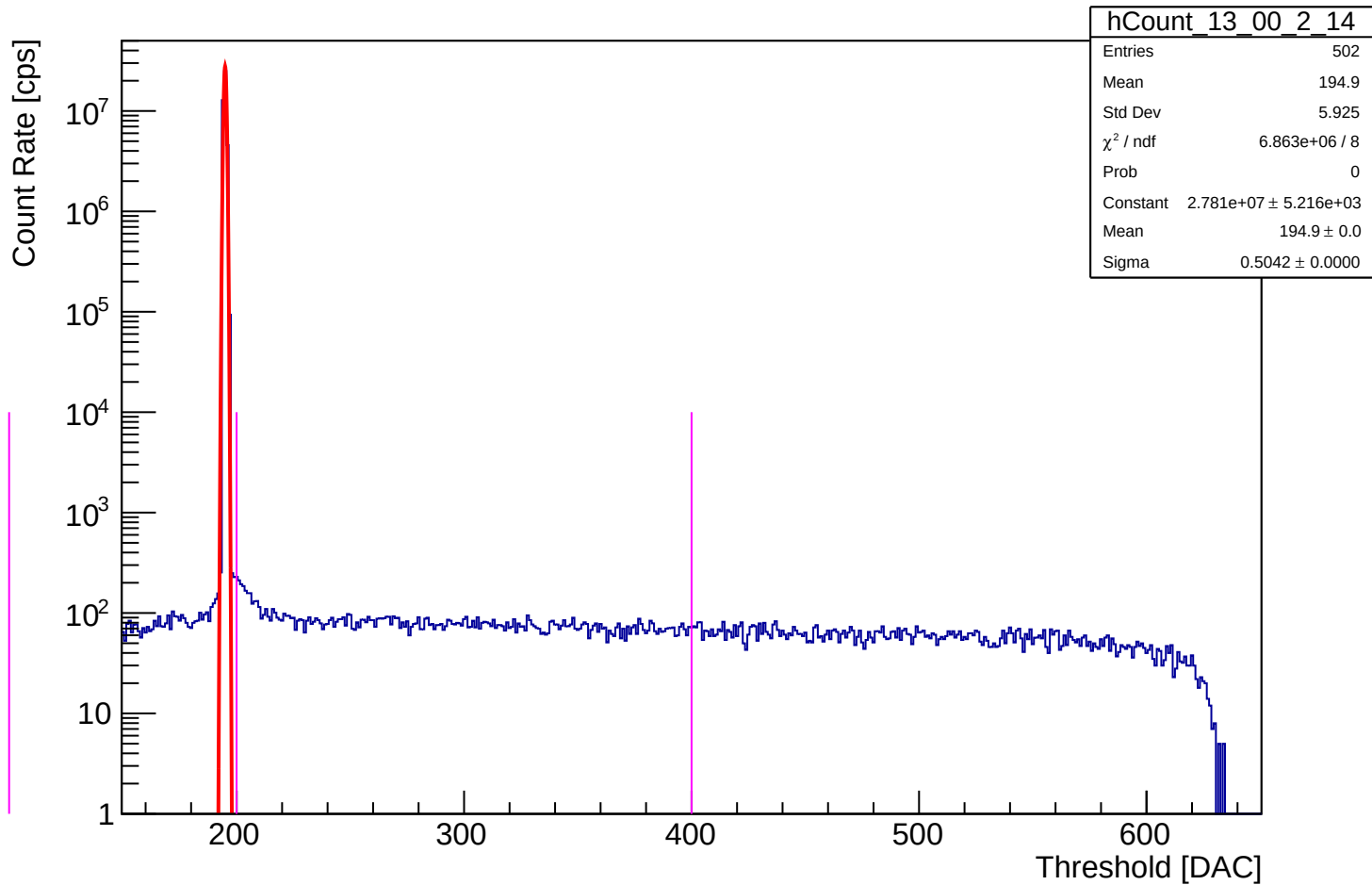
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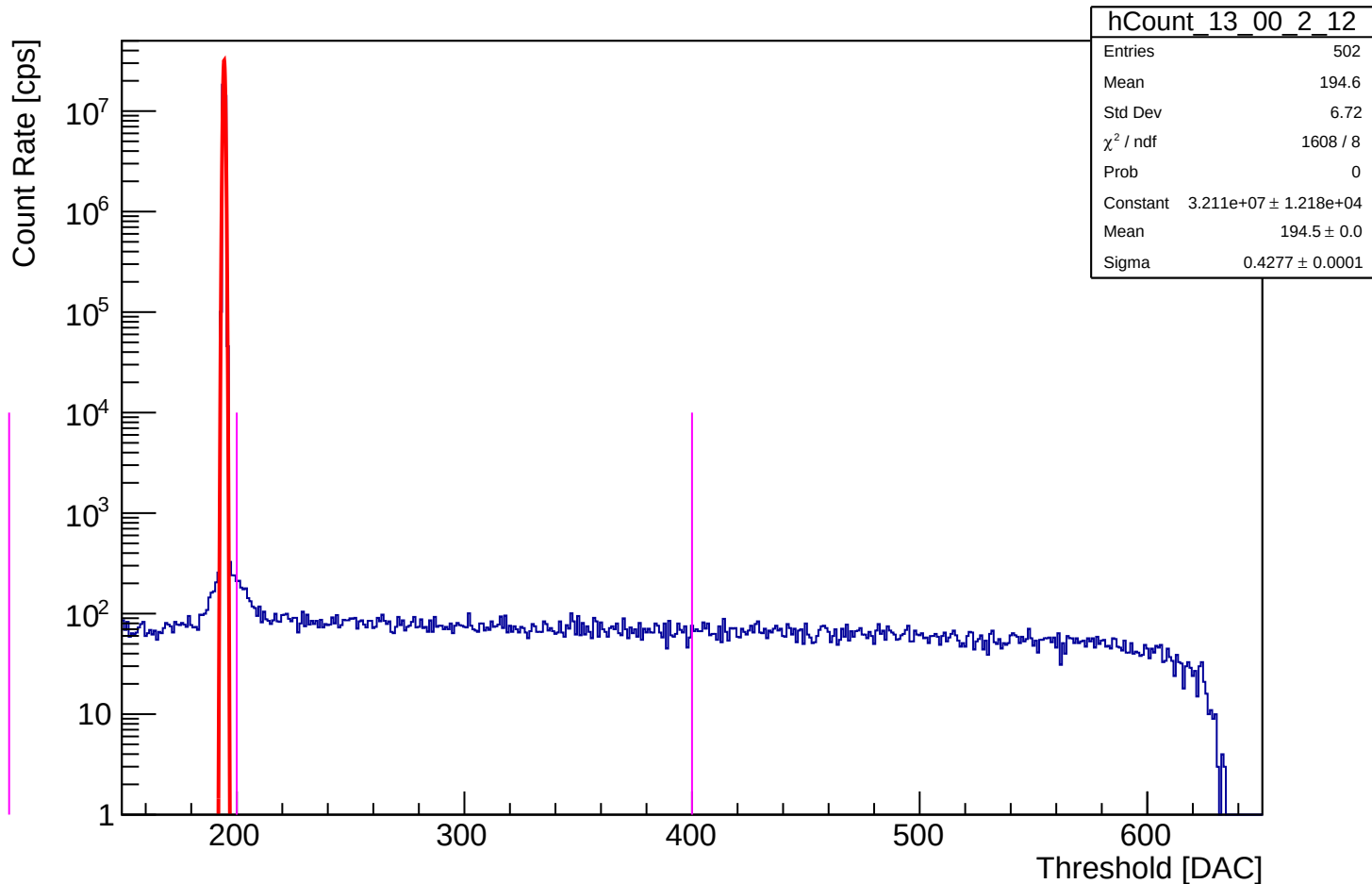
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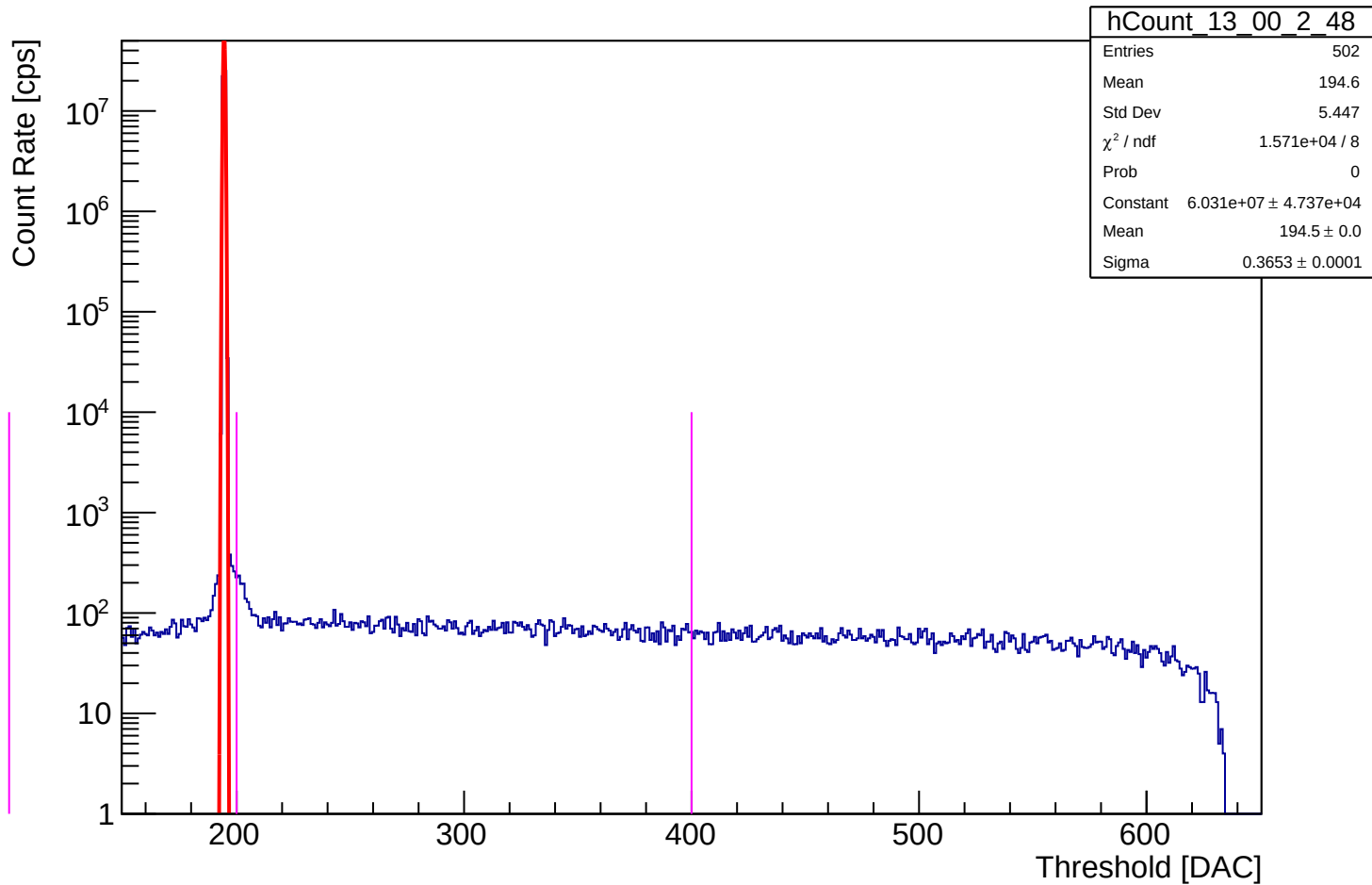
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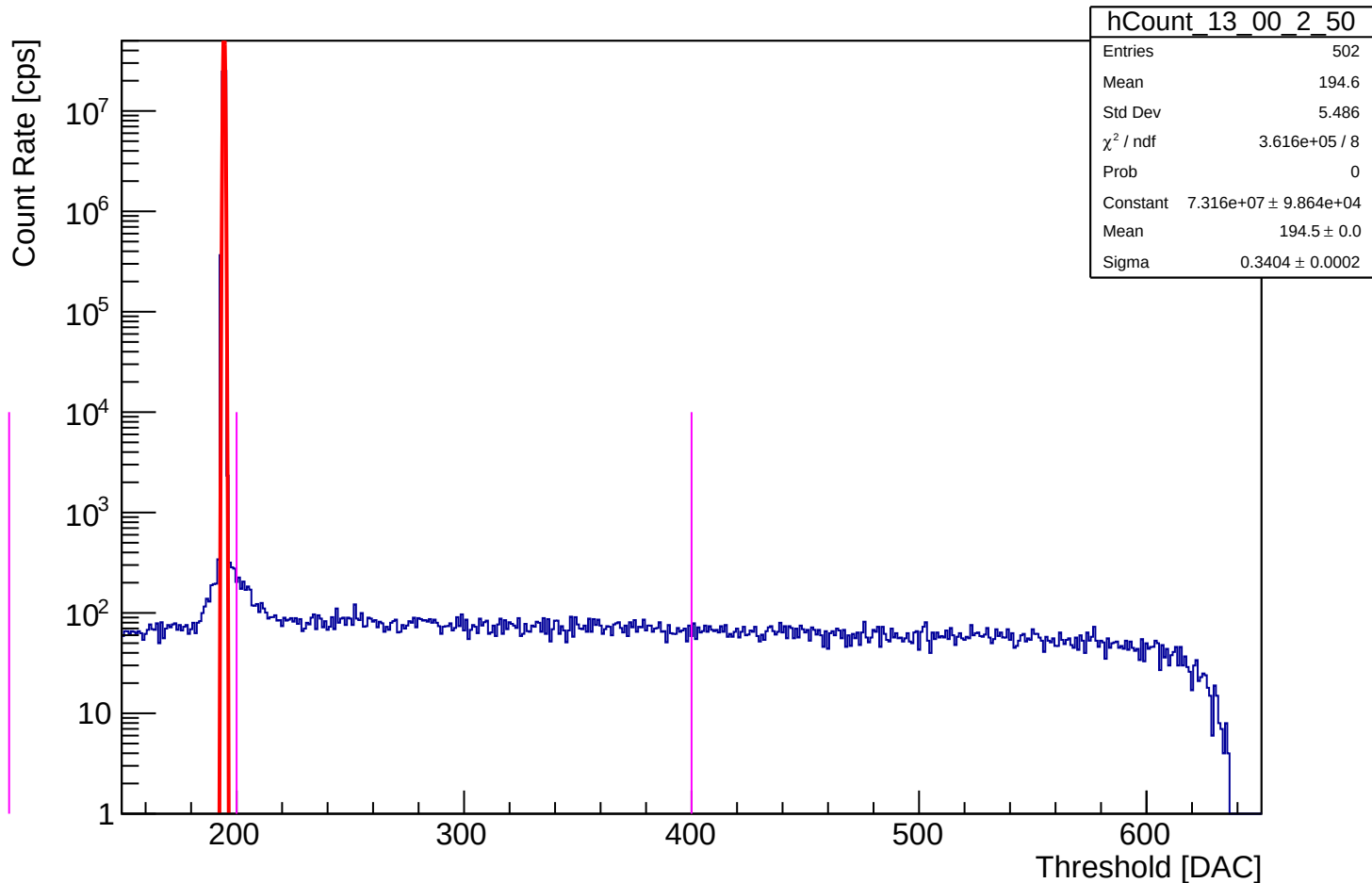
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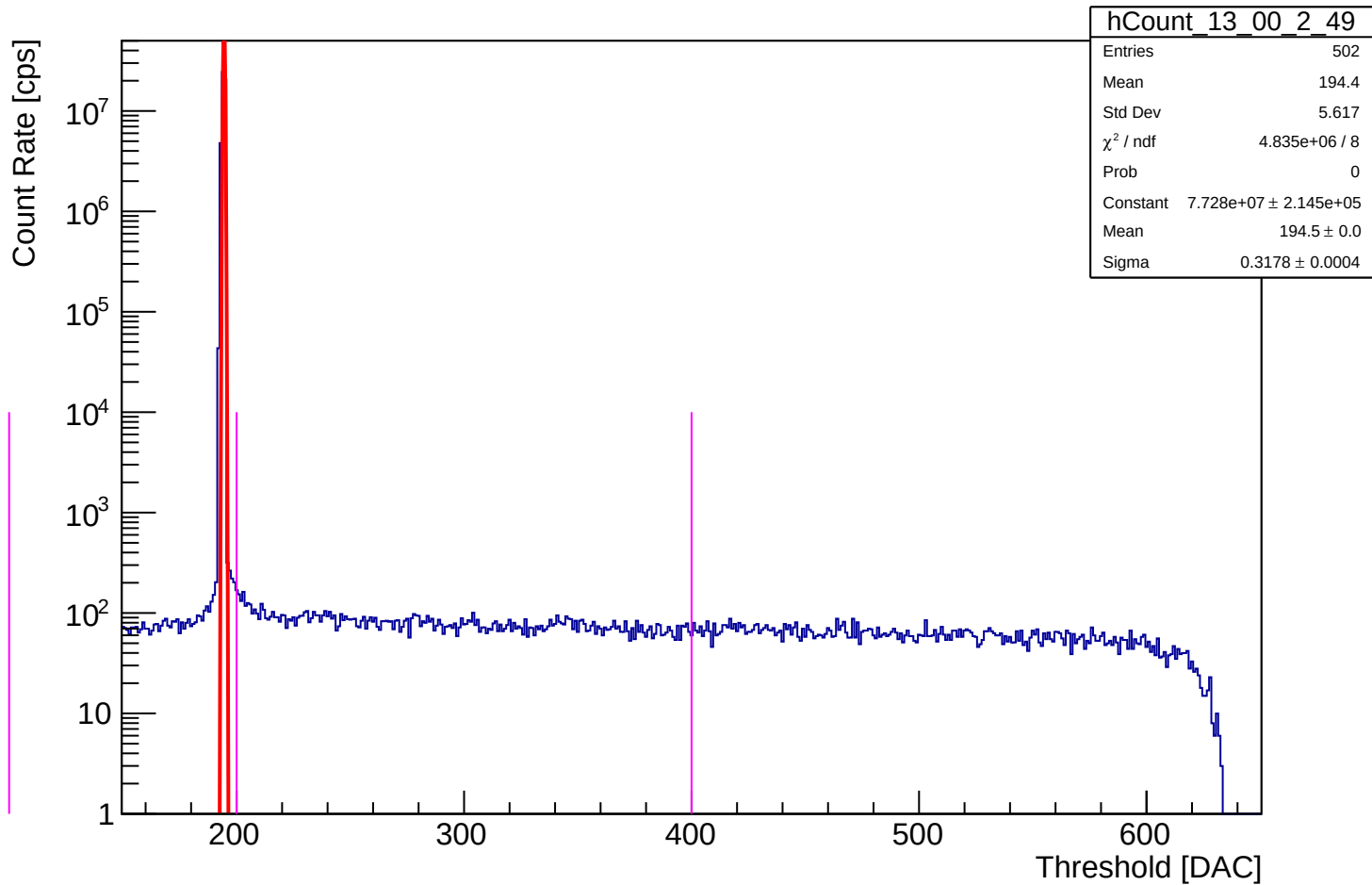
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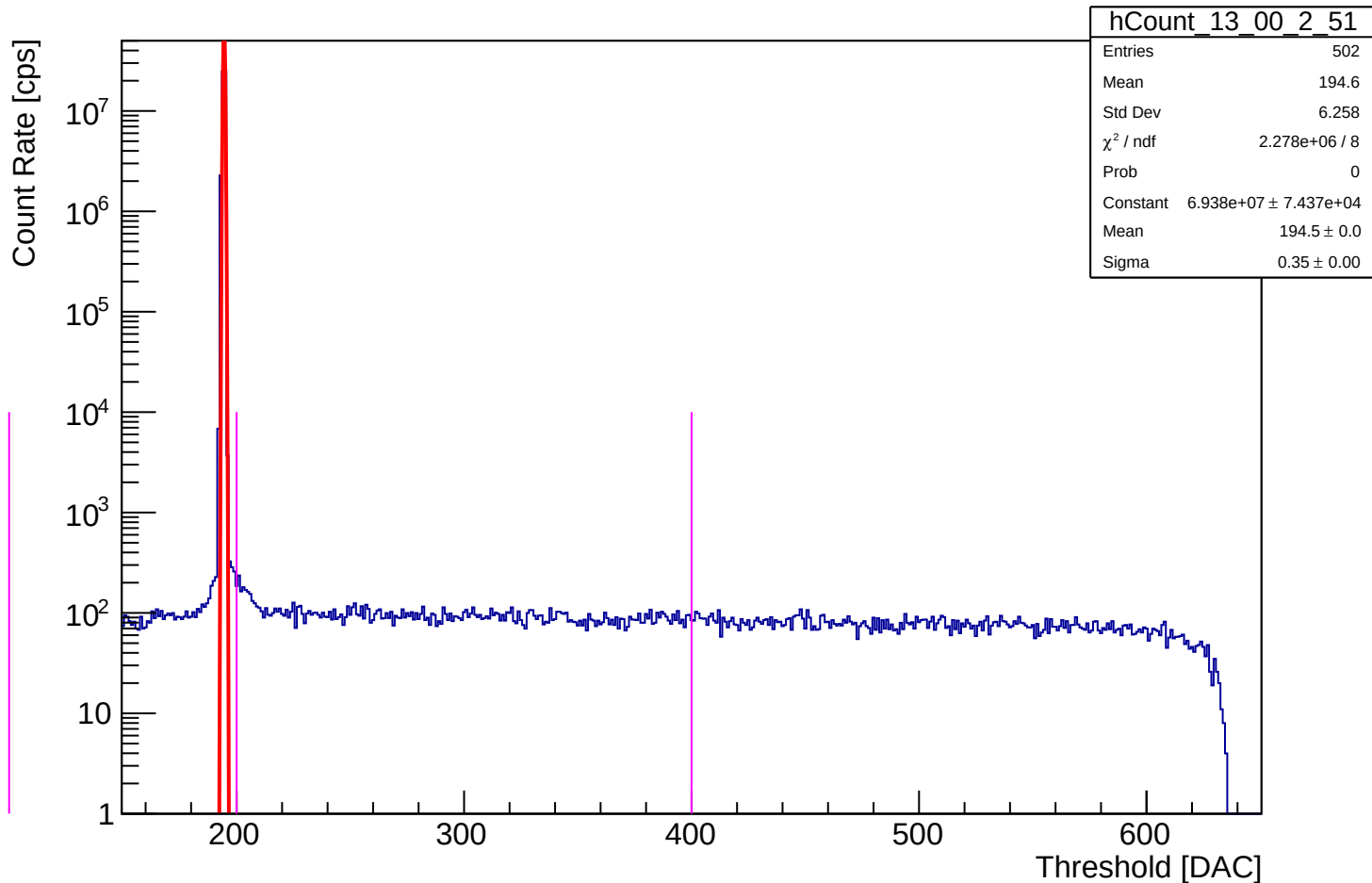
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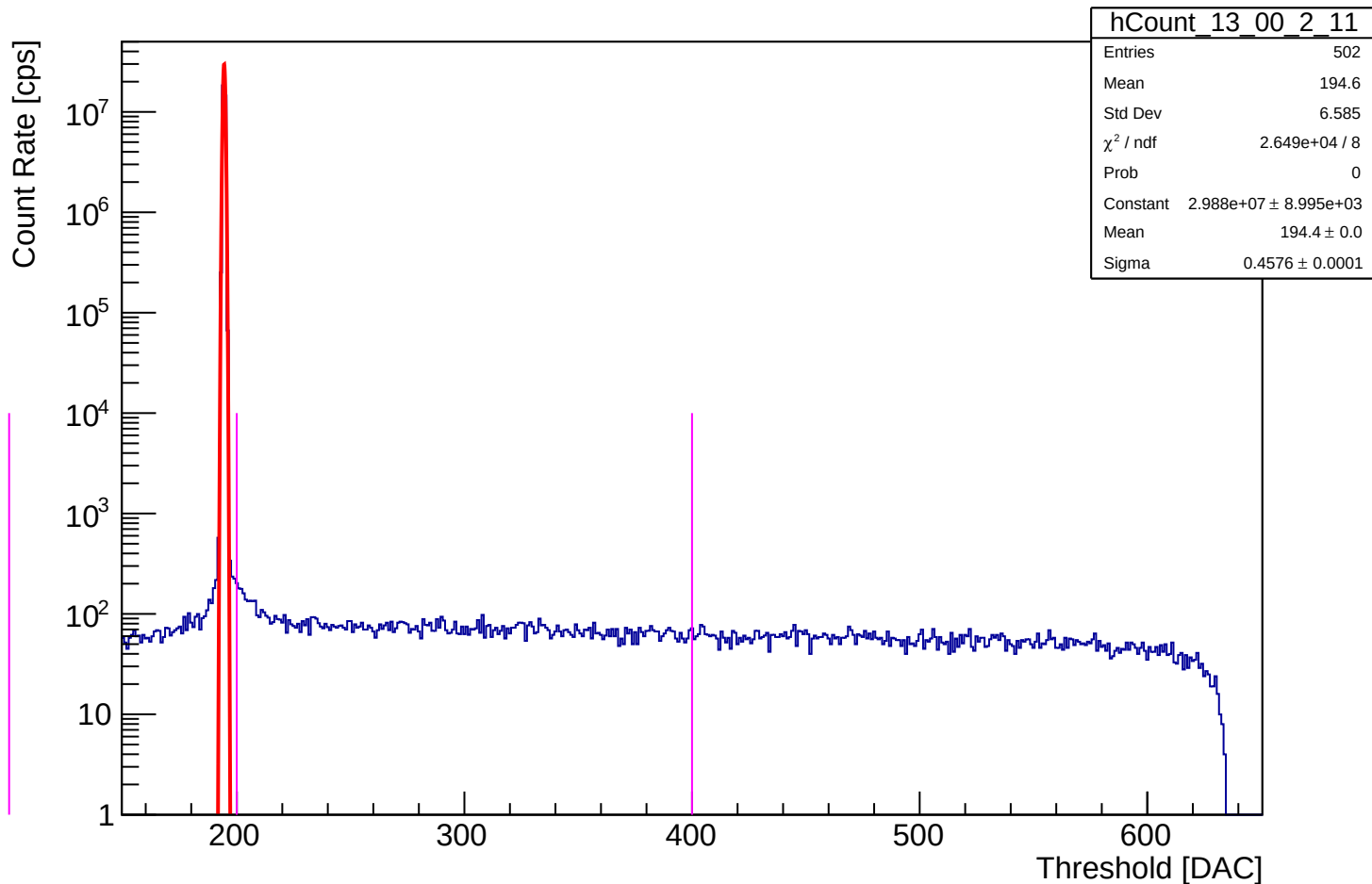
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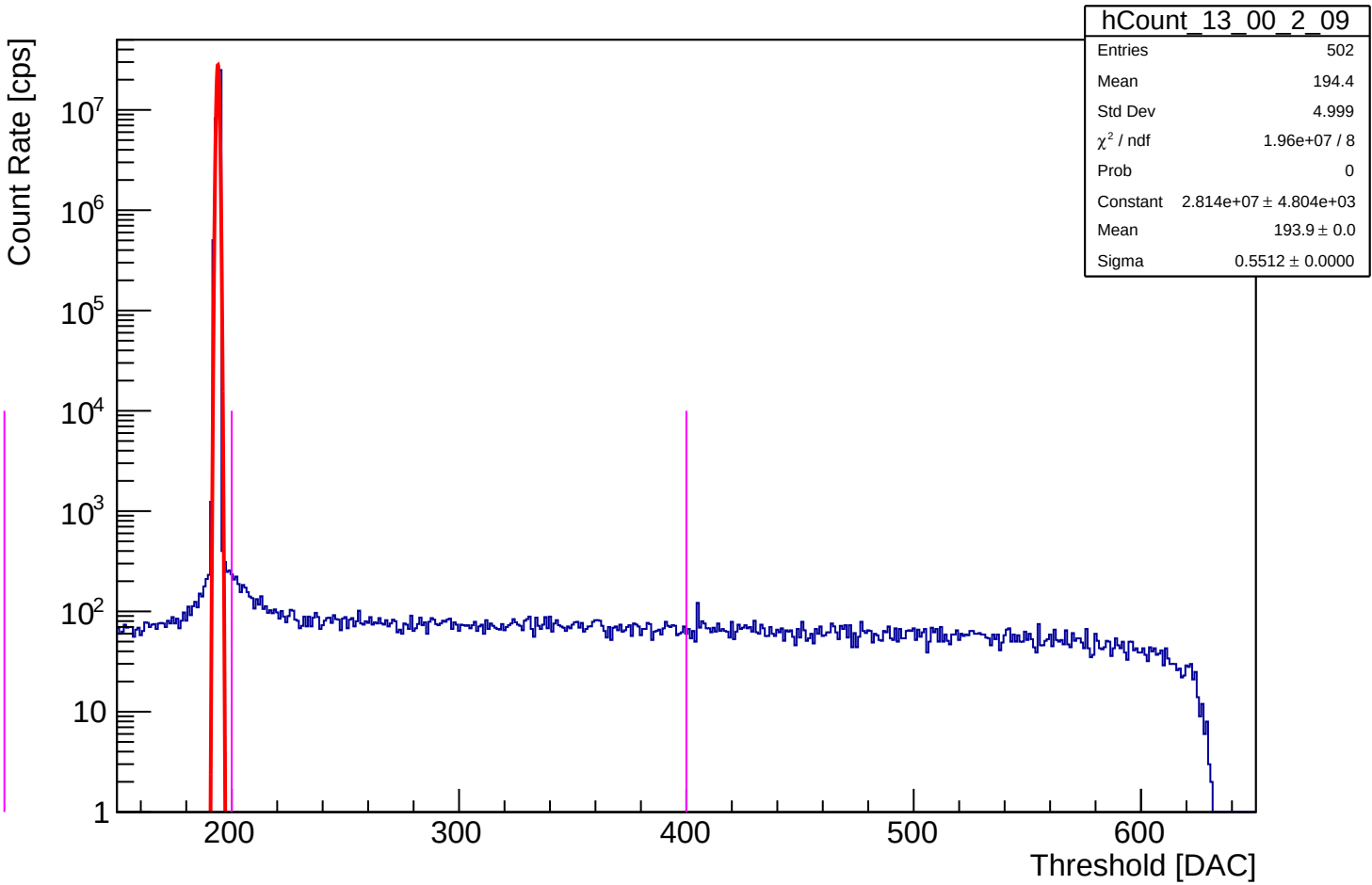


Row 1 Tile 1 Pmt 3 Pixel 40 Slot 13 Fiber 0 Asic 2 Channel 51

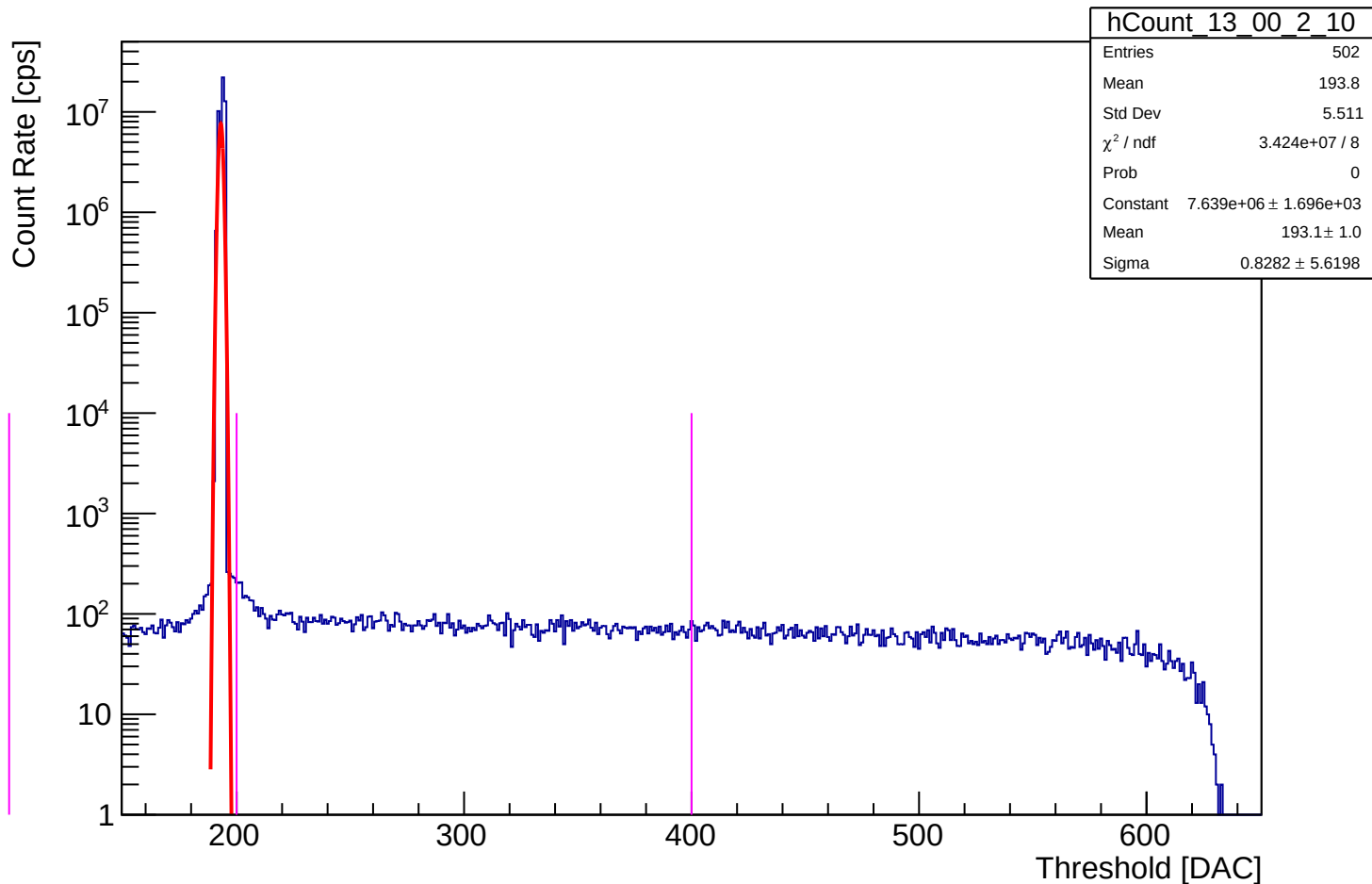


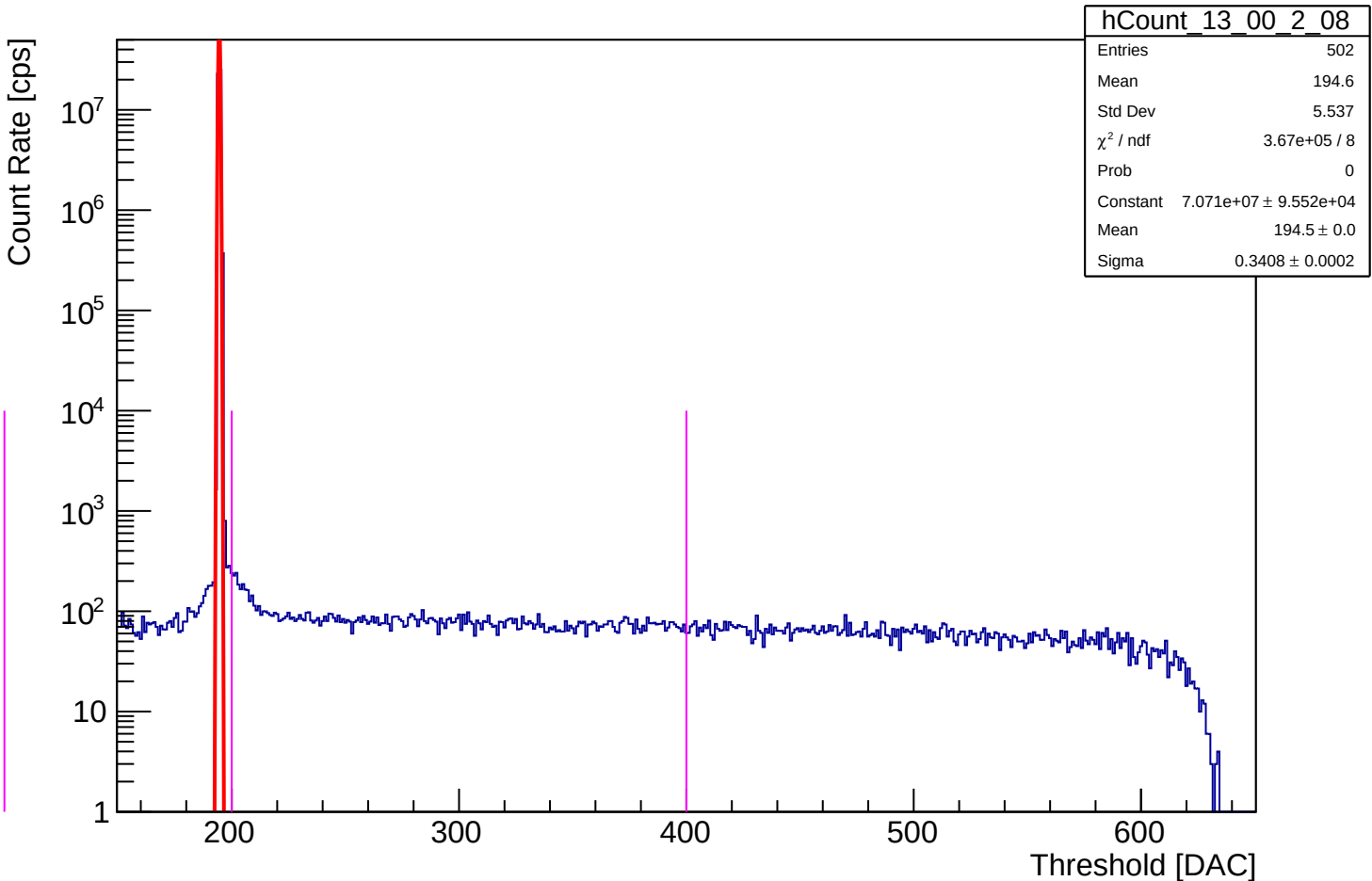
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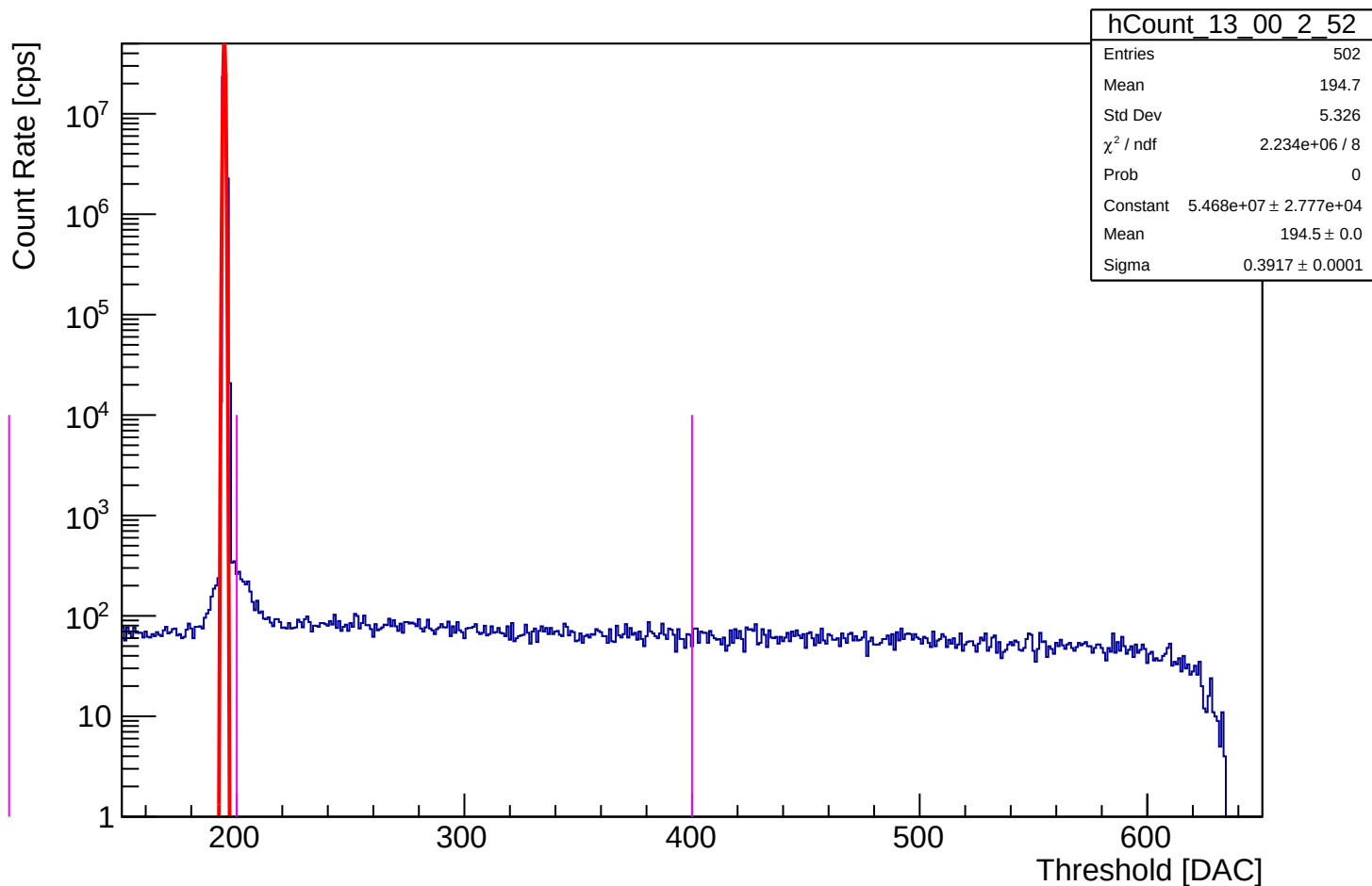


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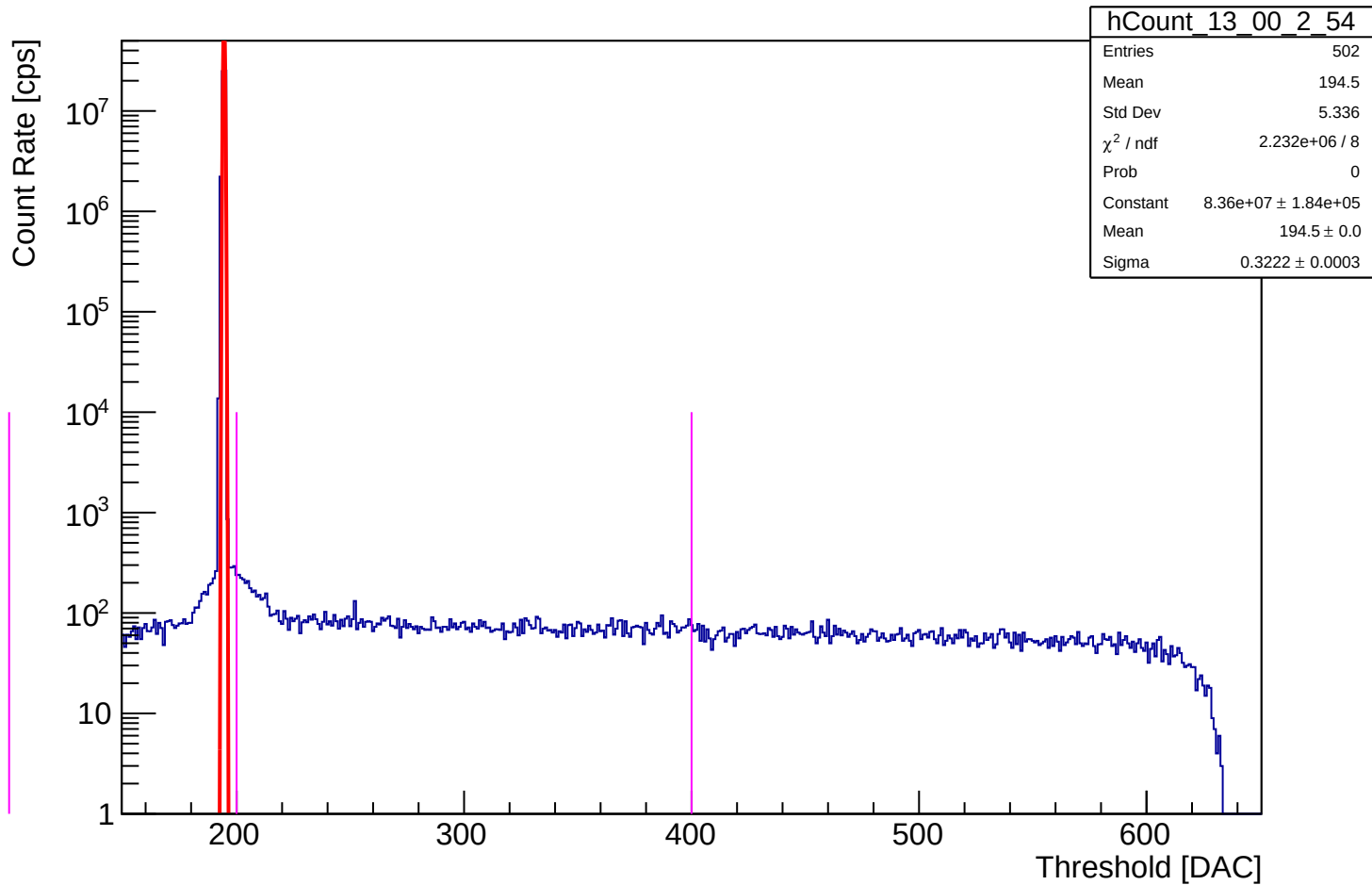




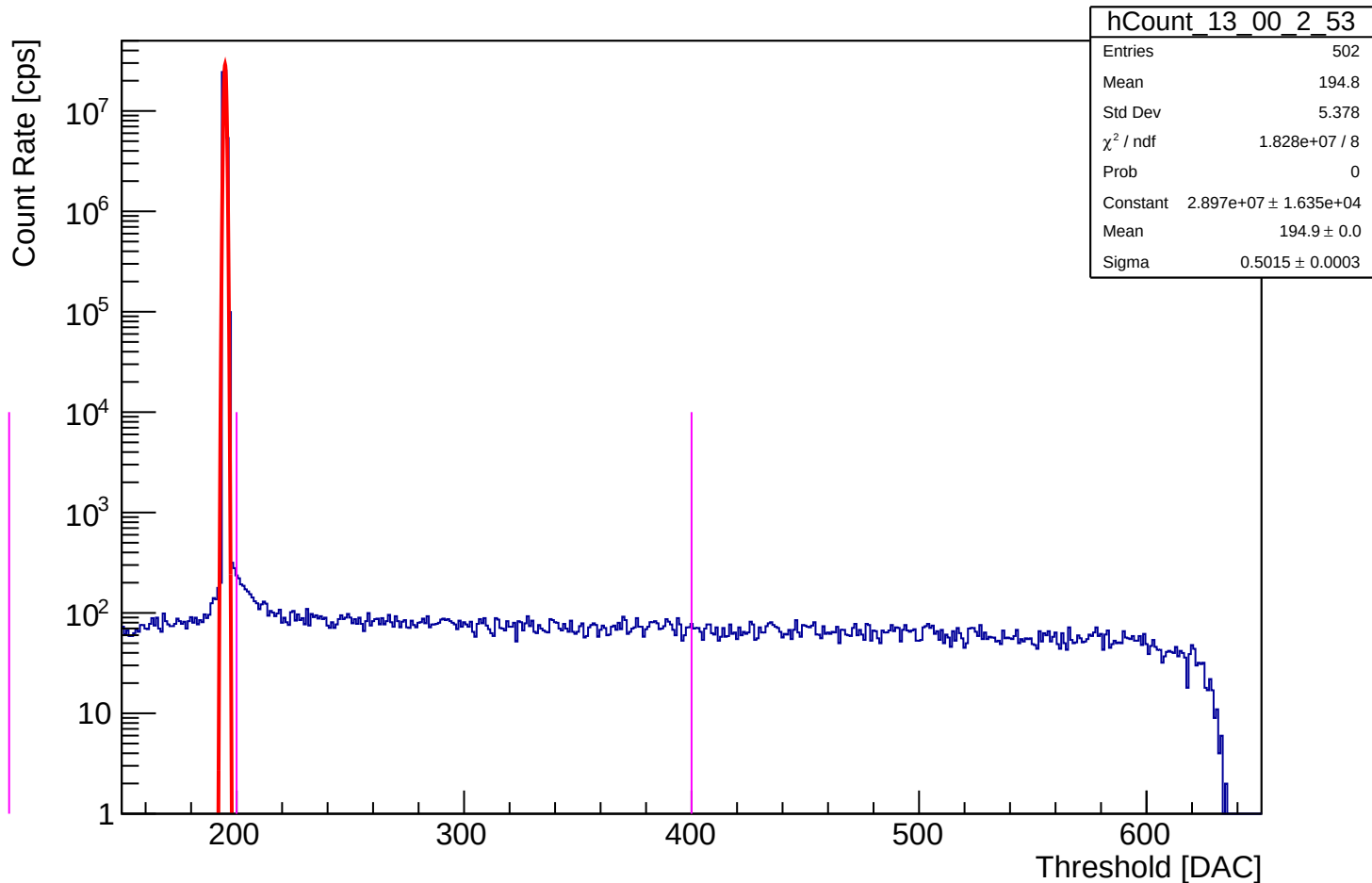
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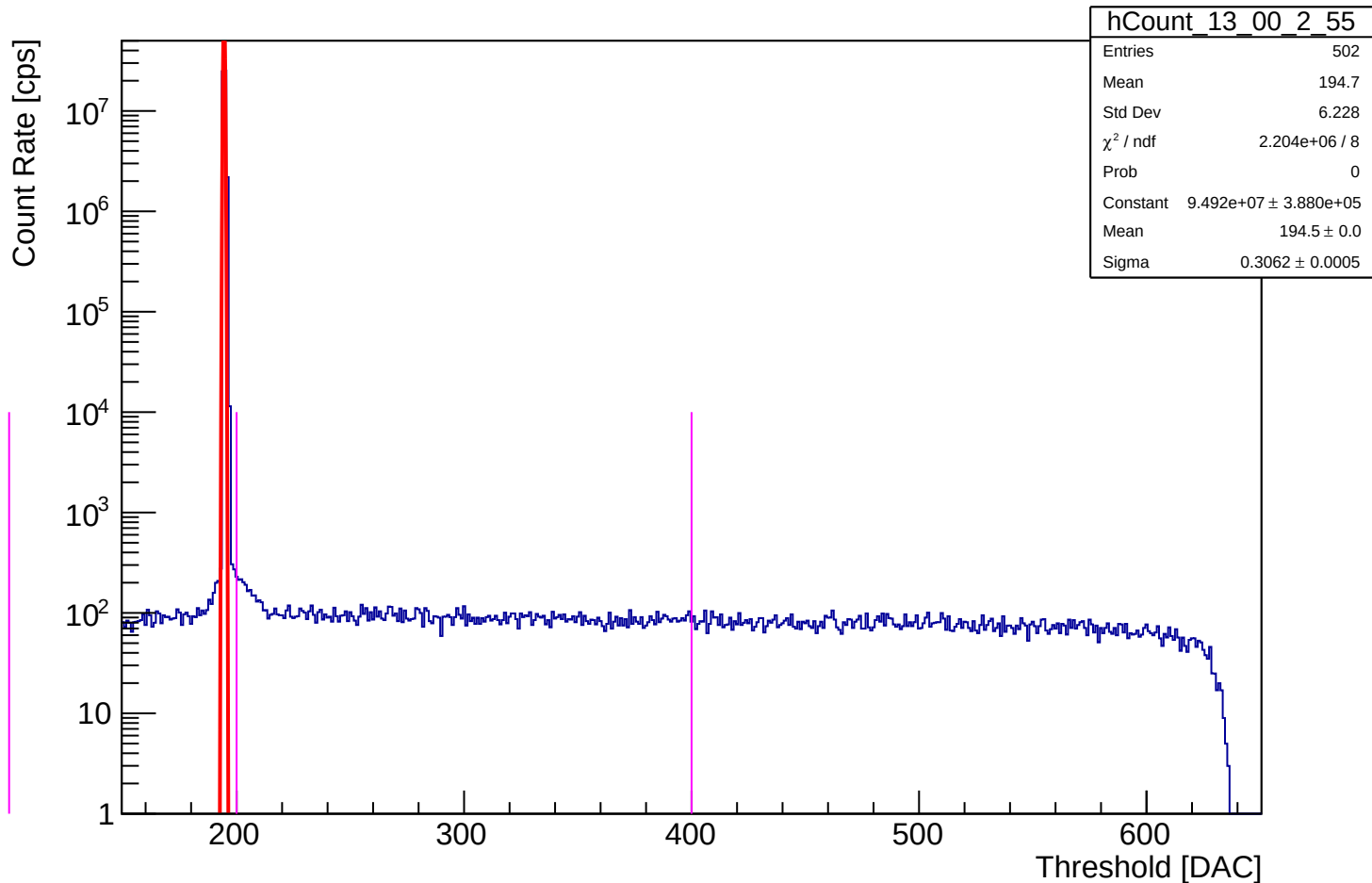
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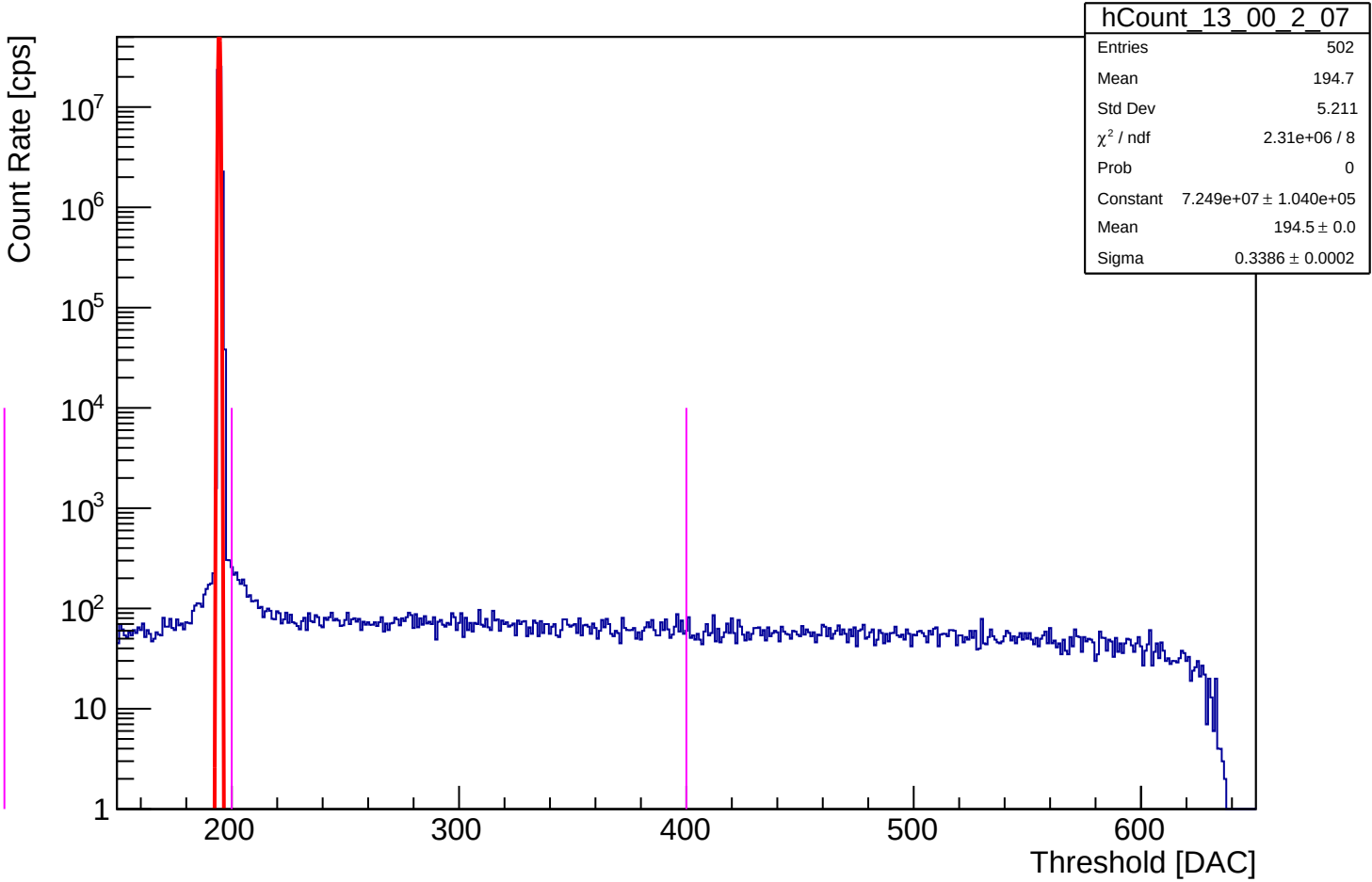


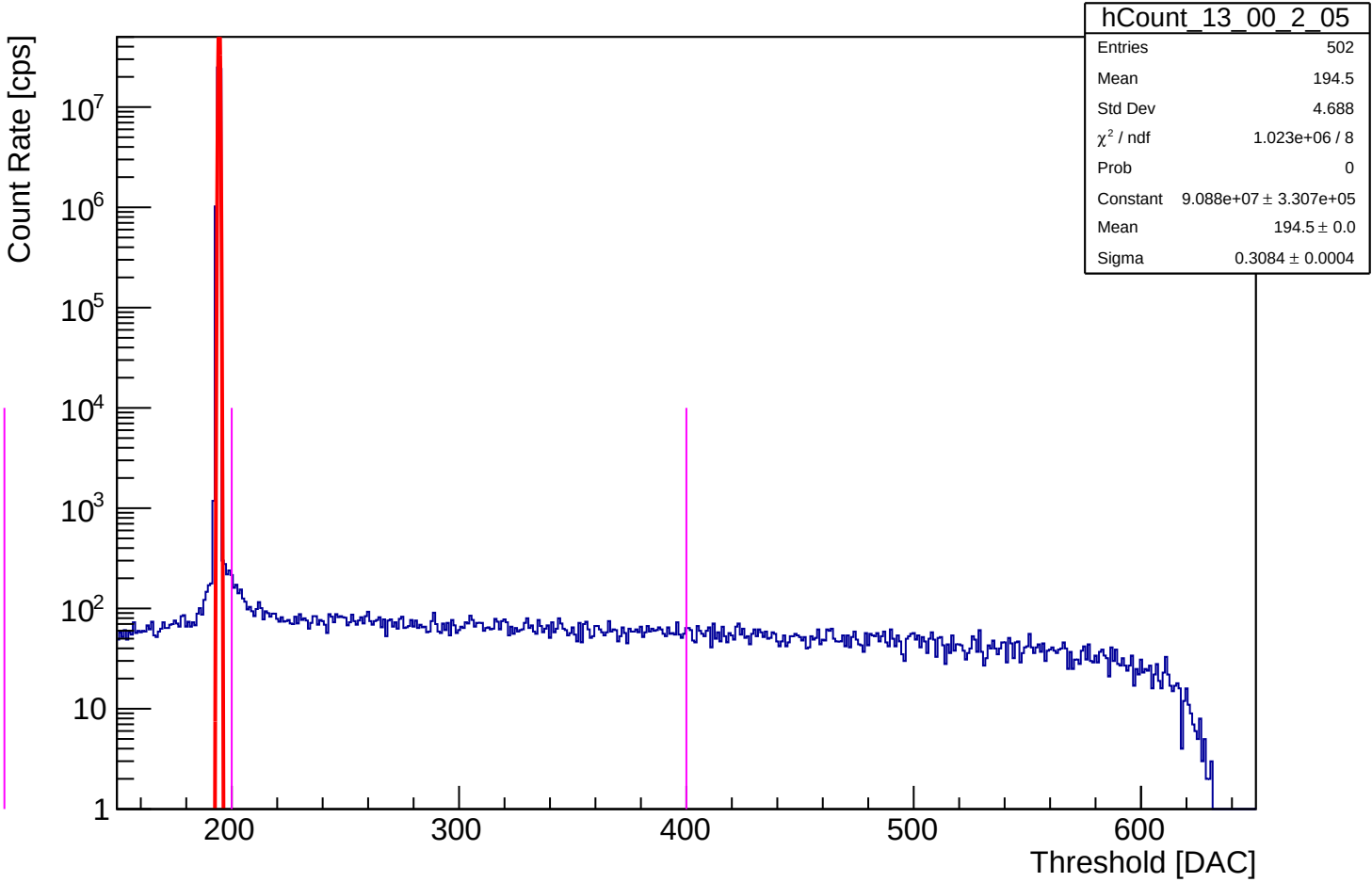
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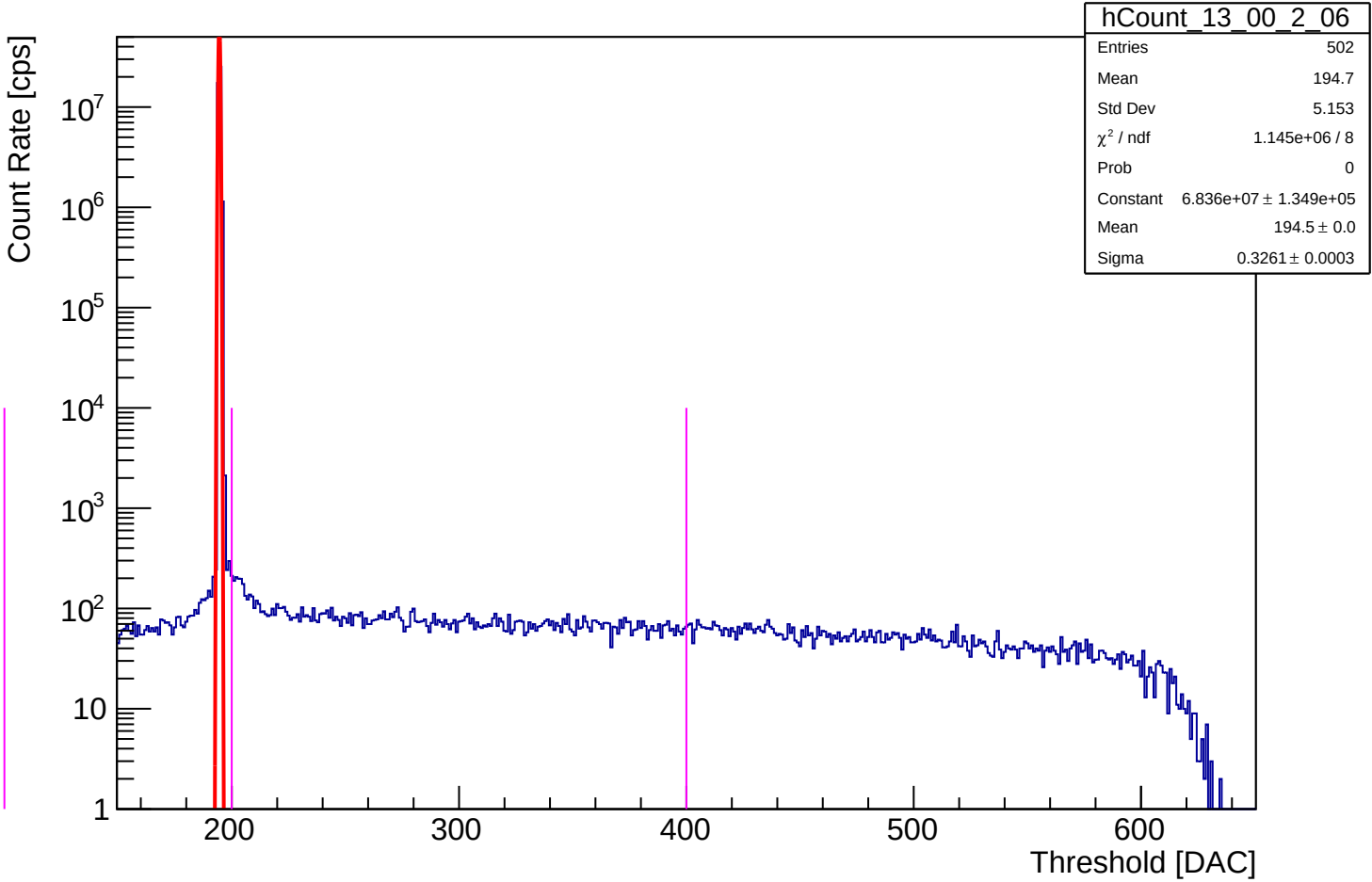


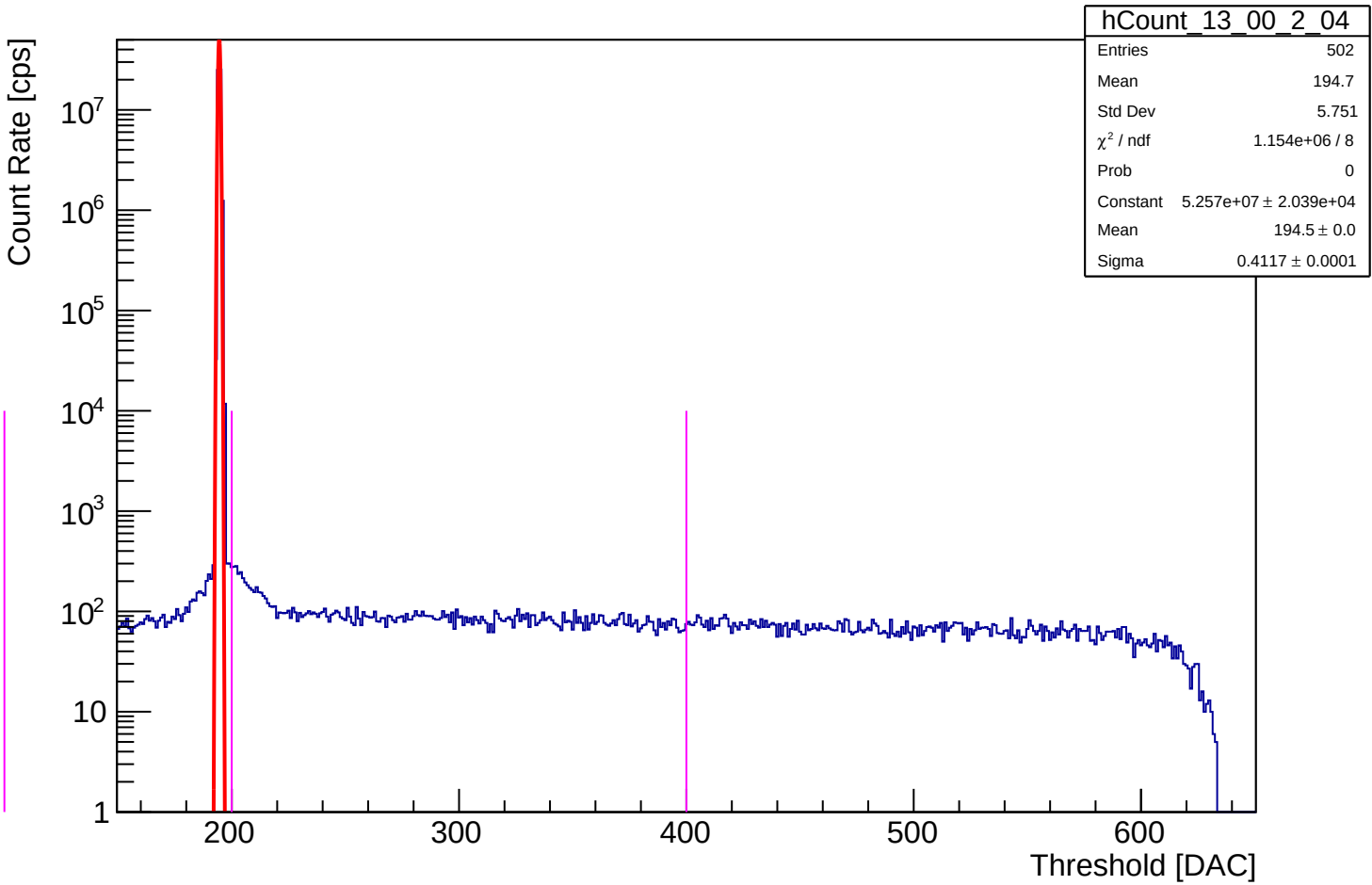
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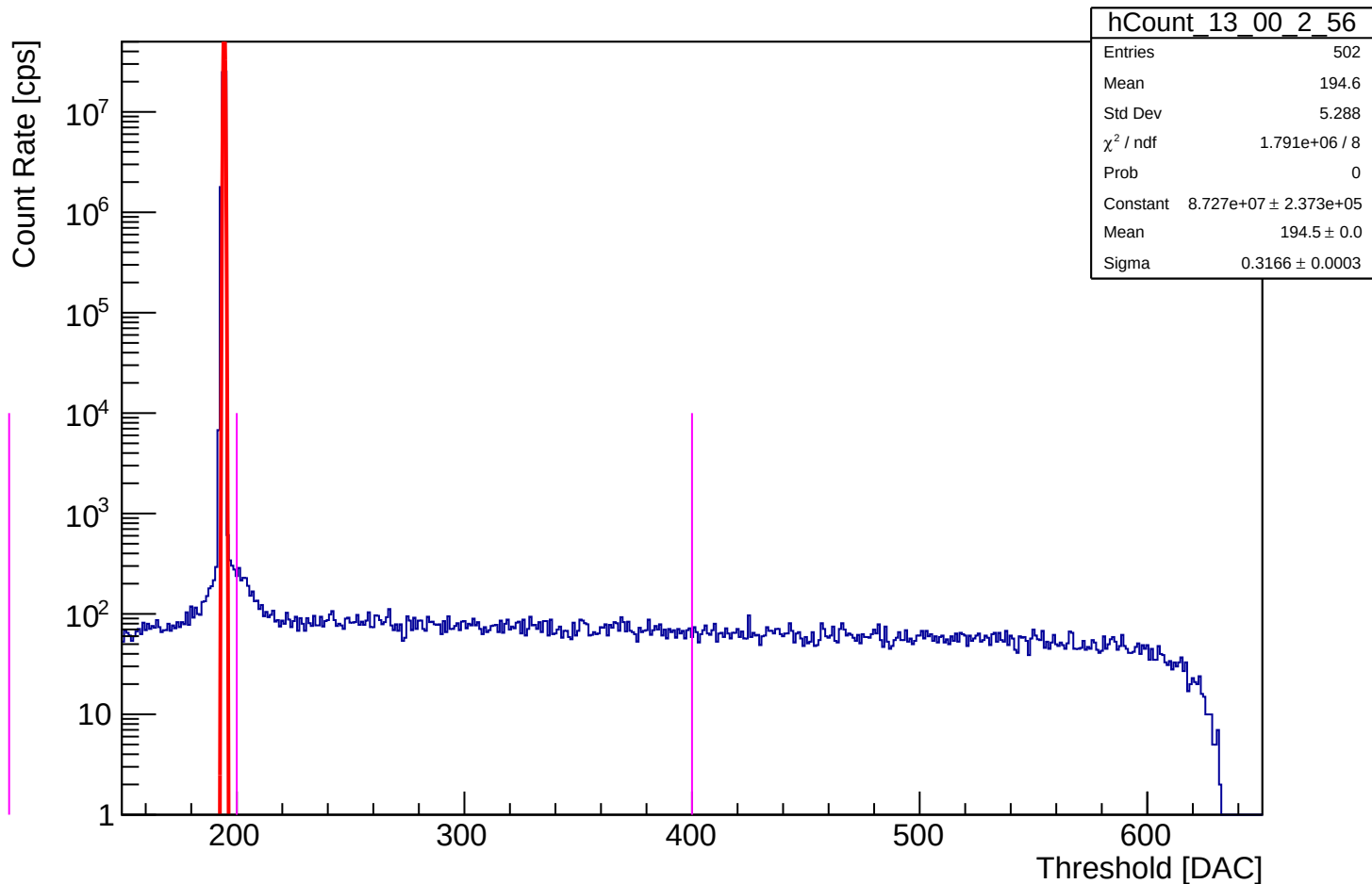




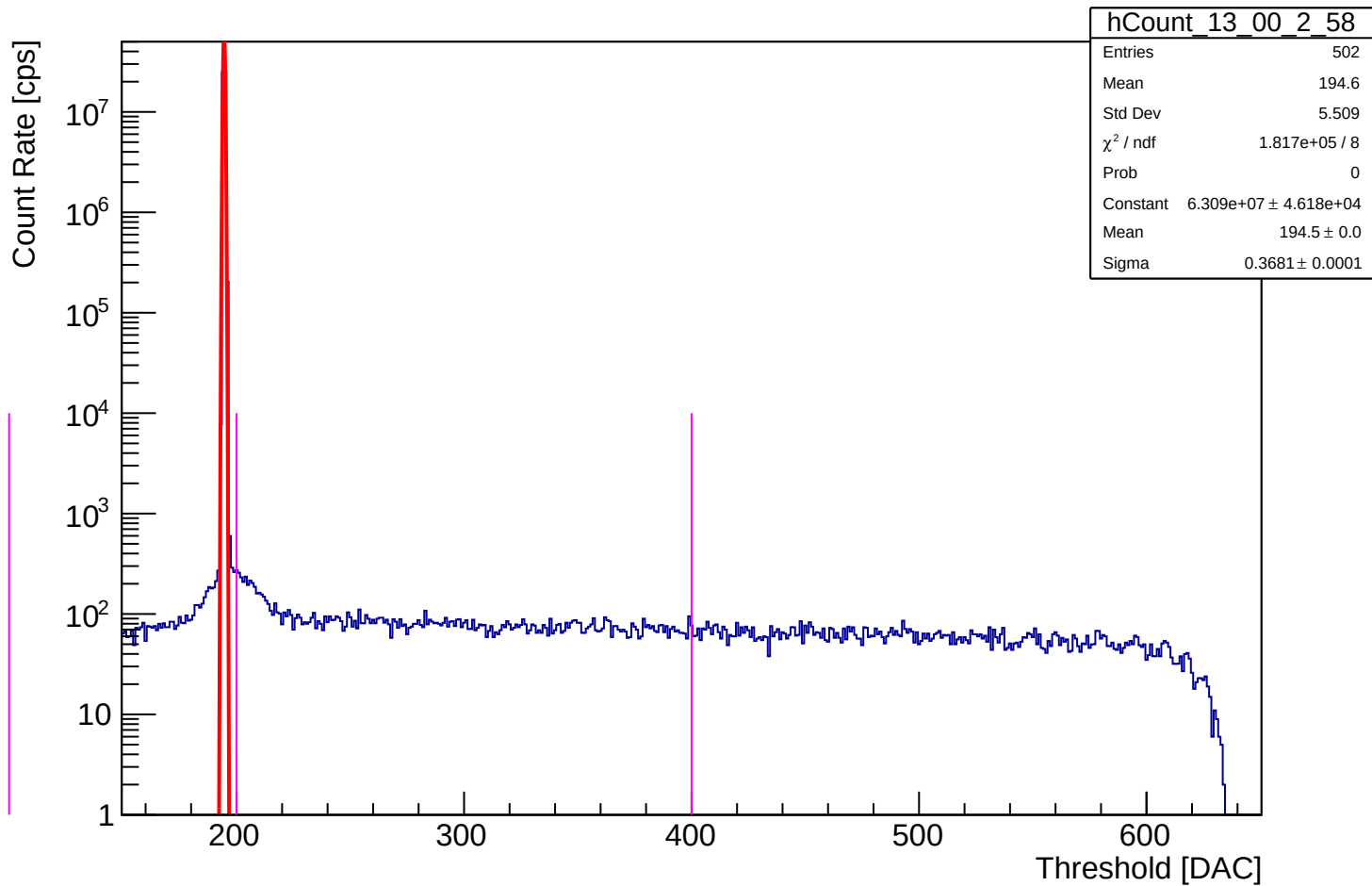




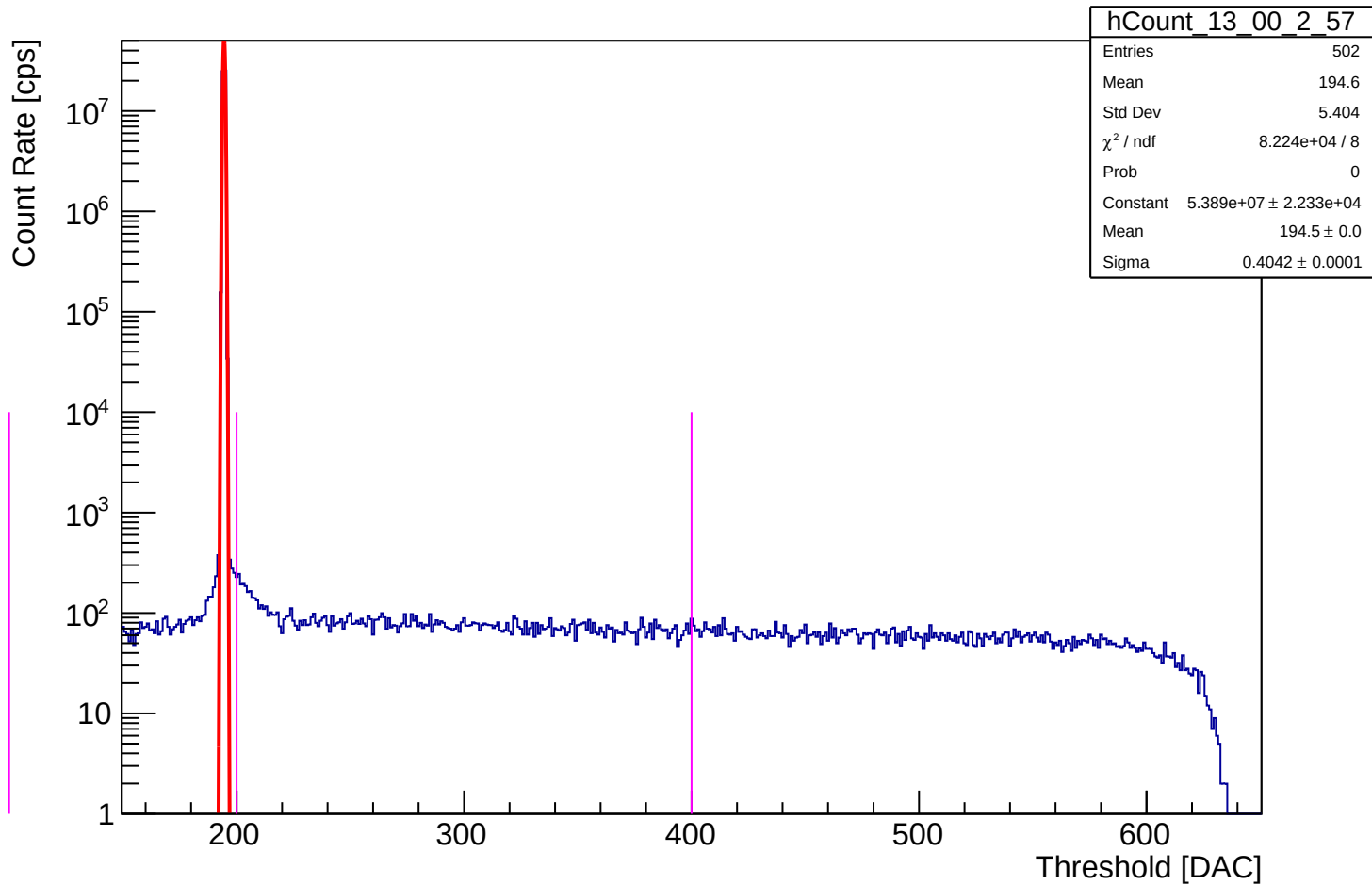
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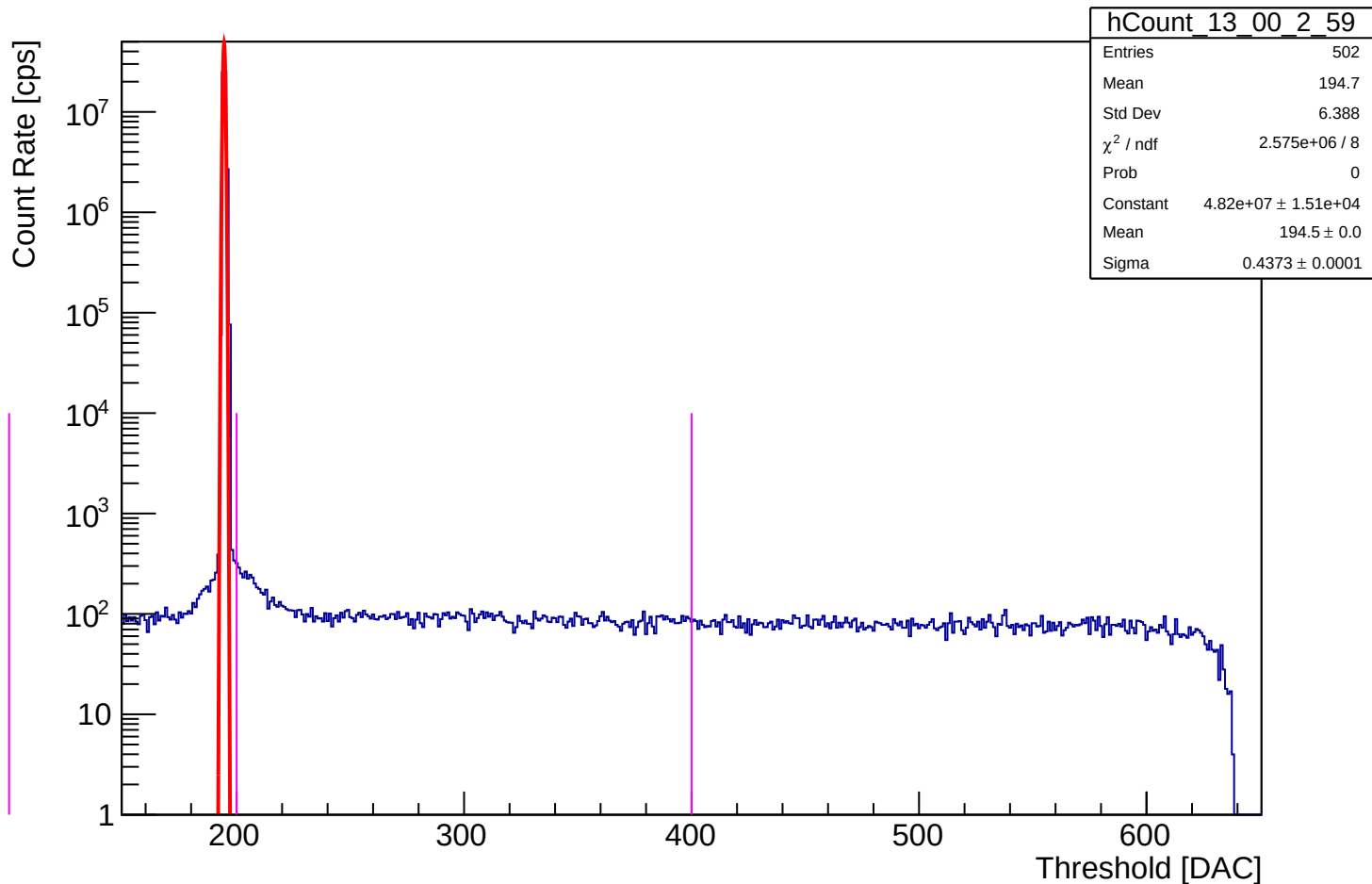
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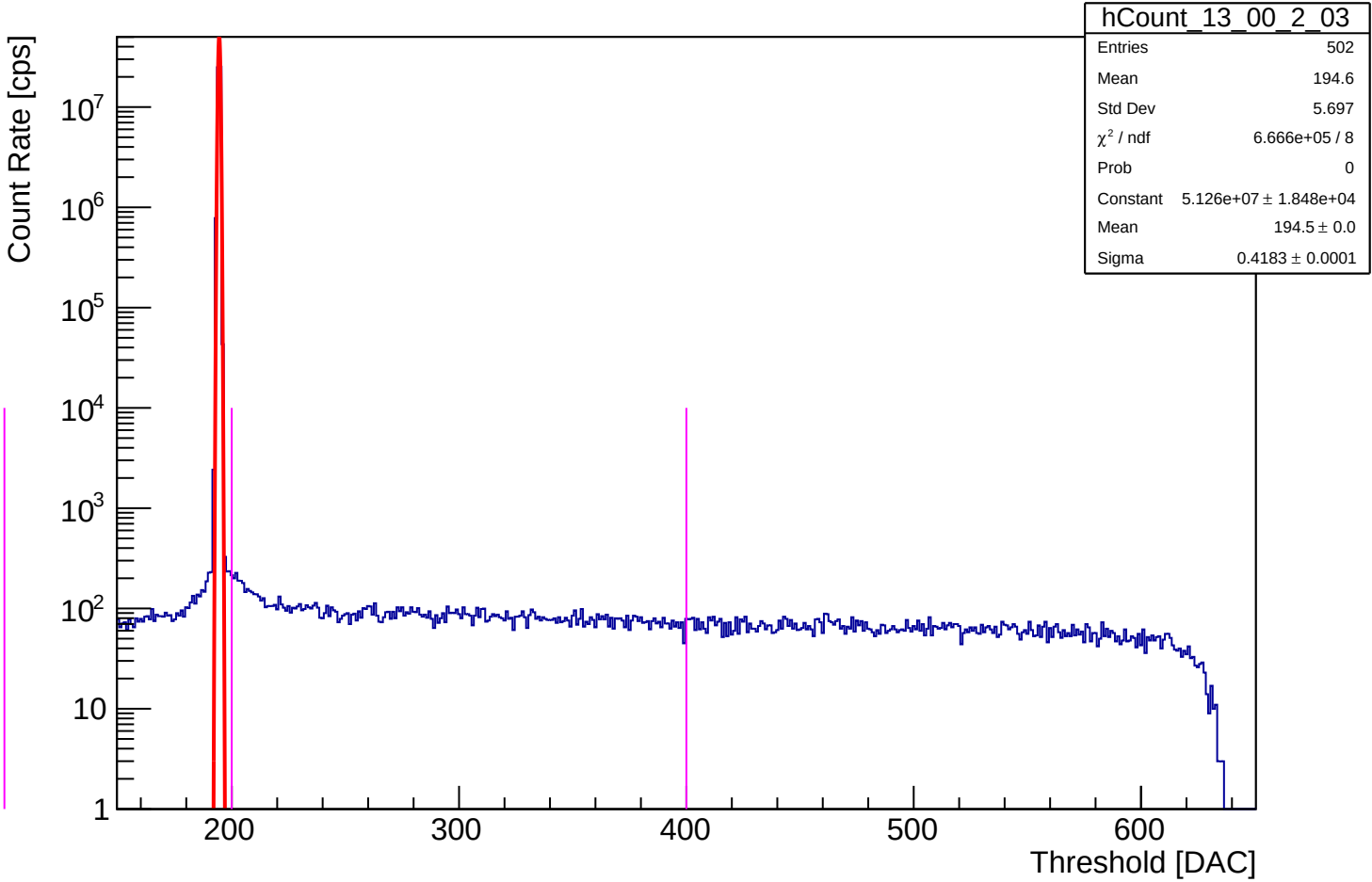


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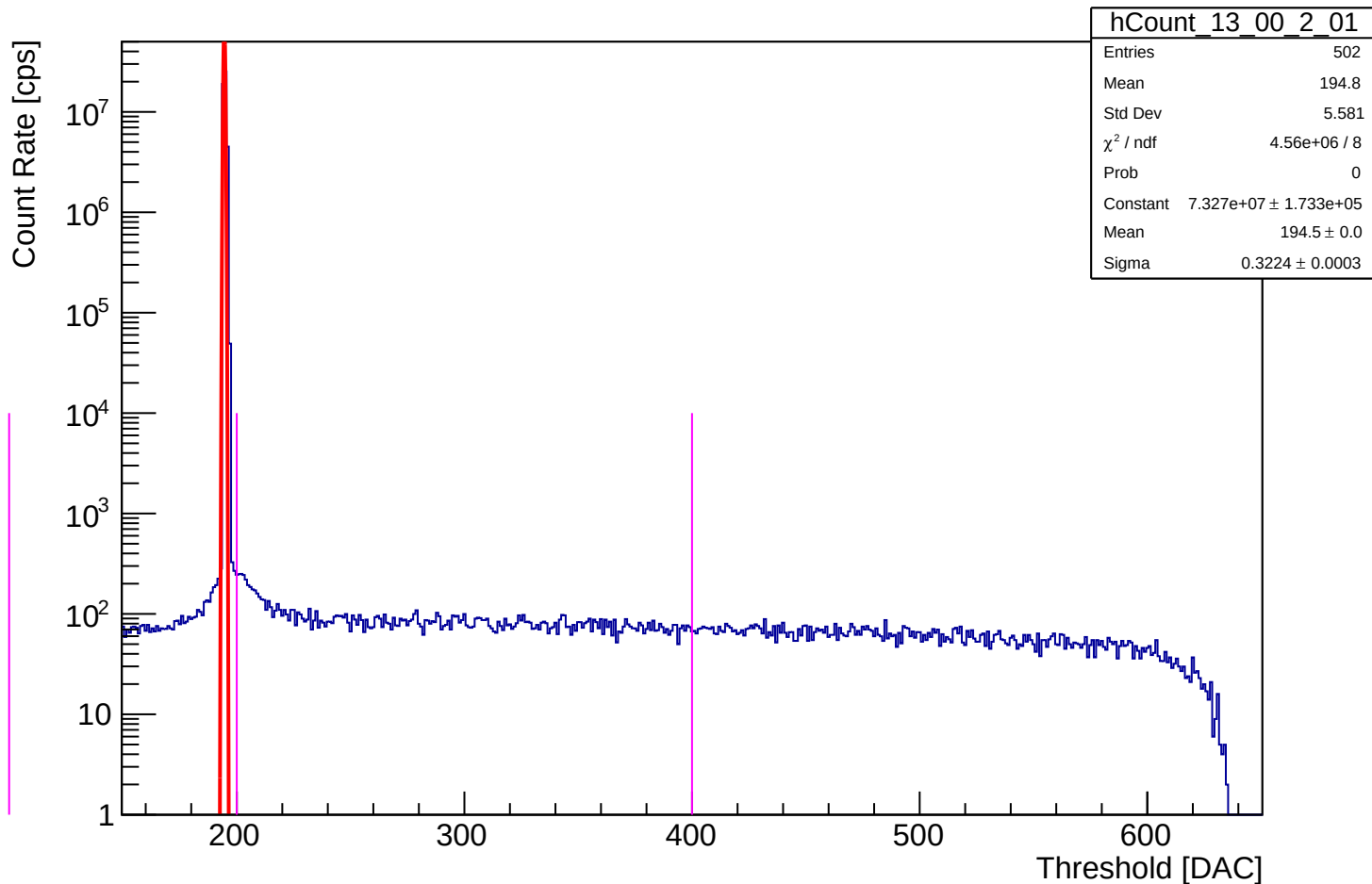


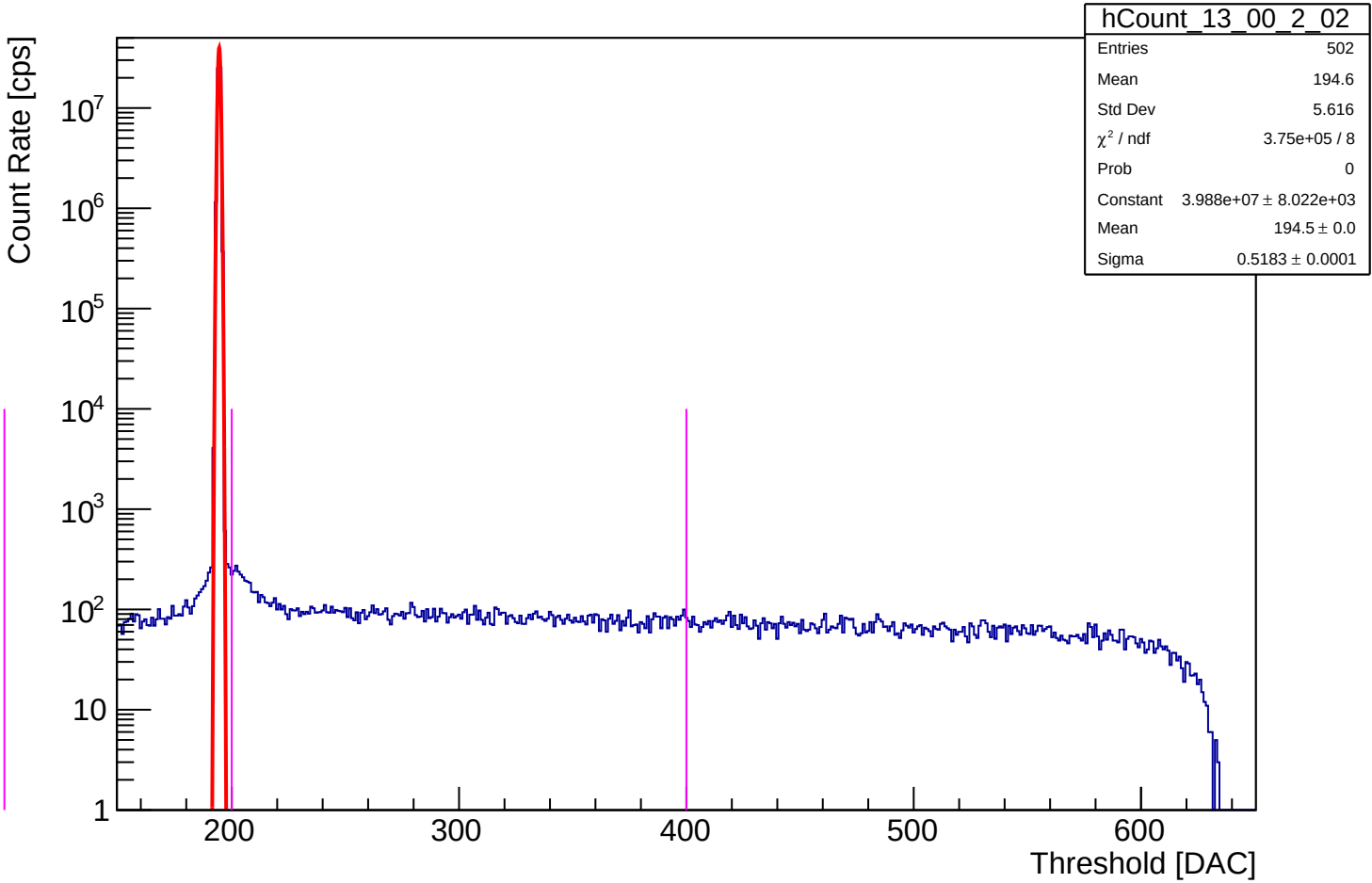
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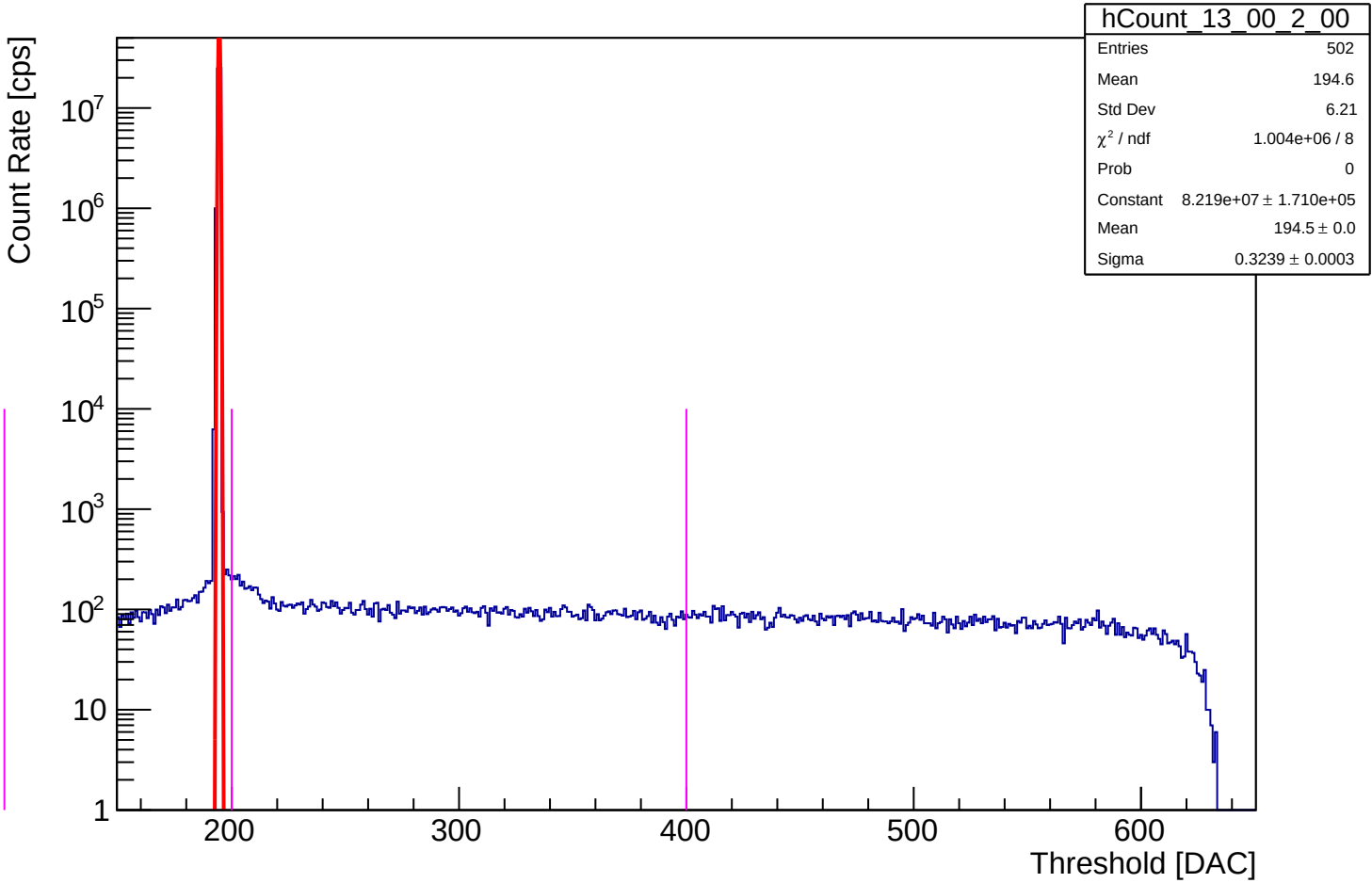




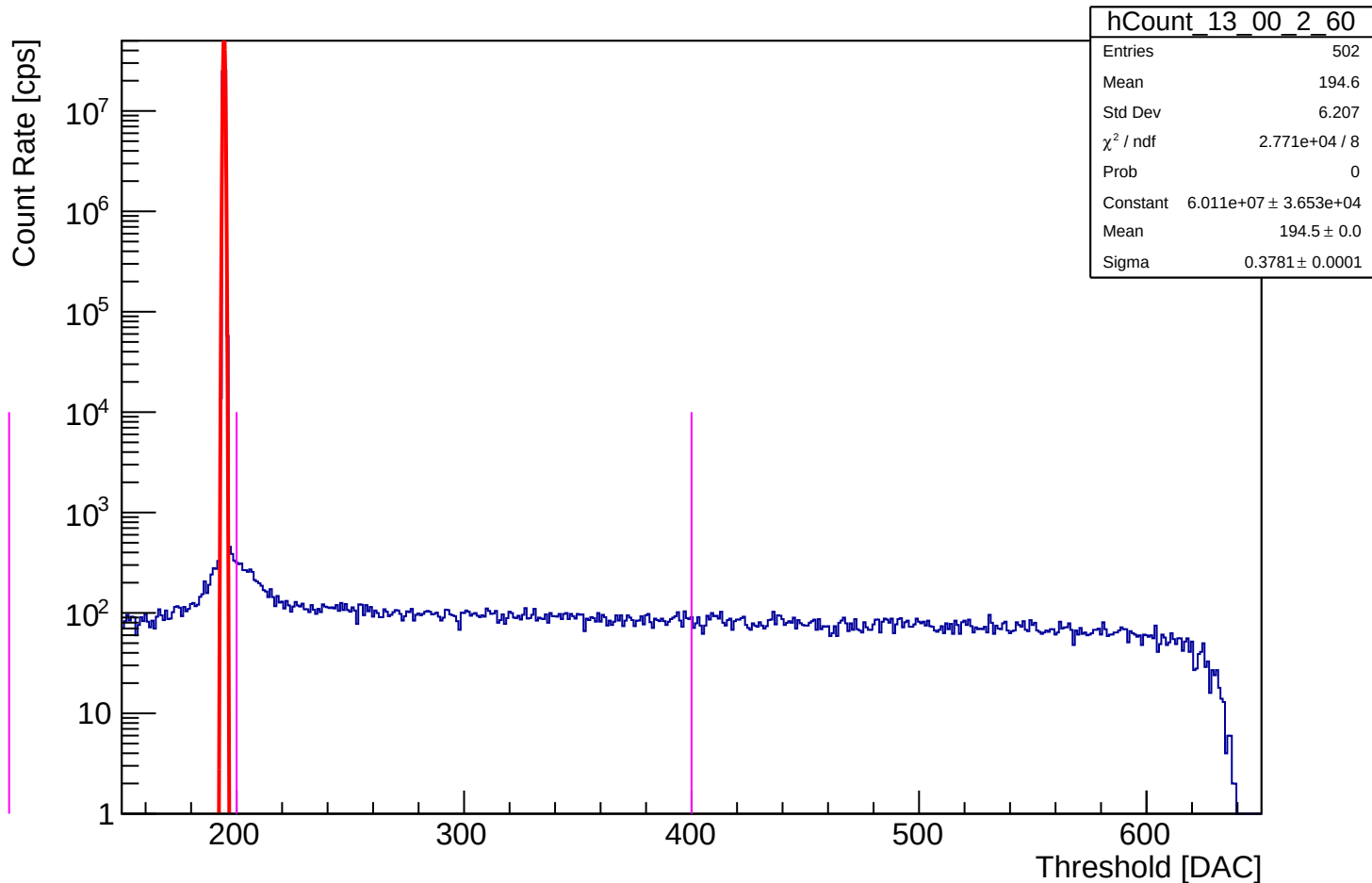
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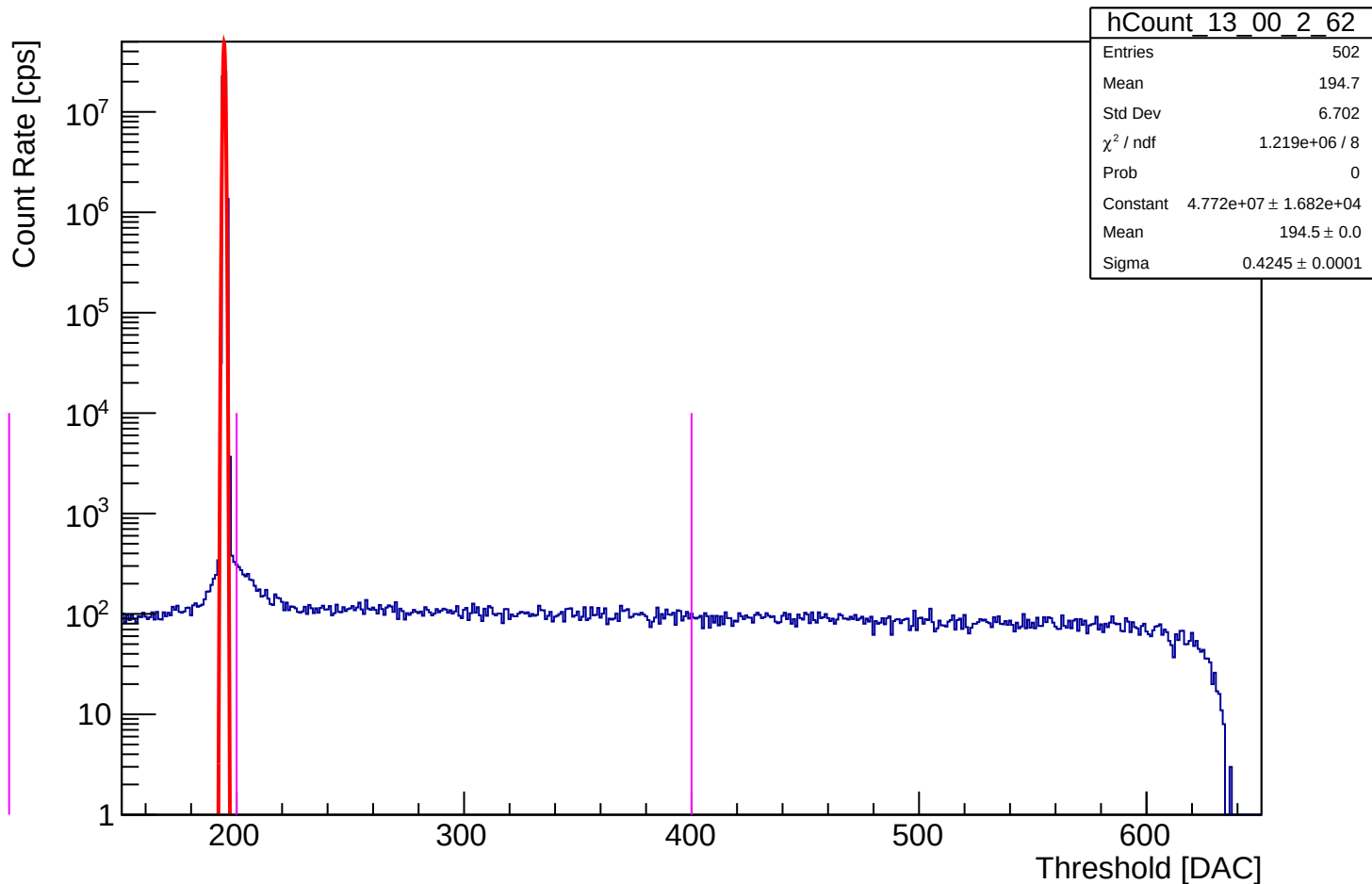




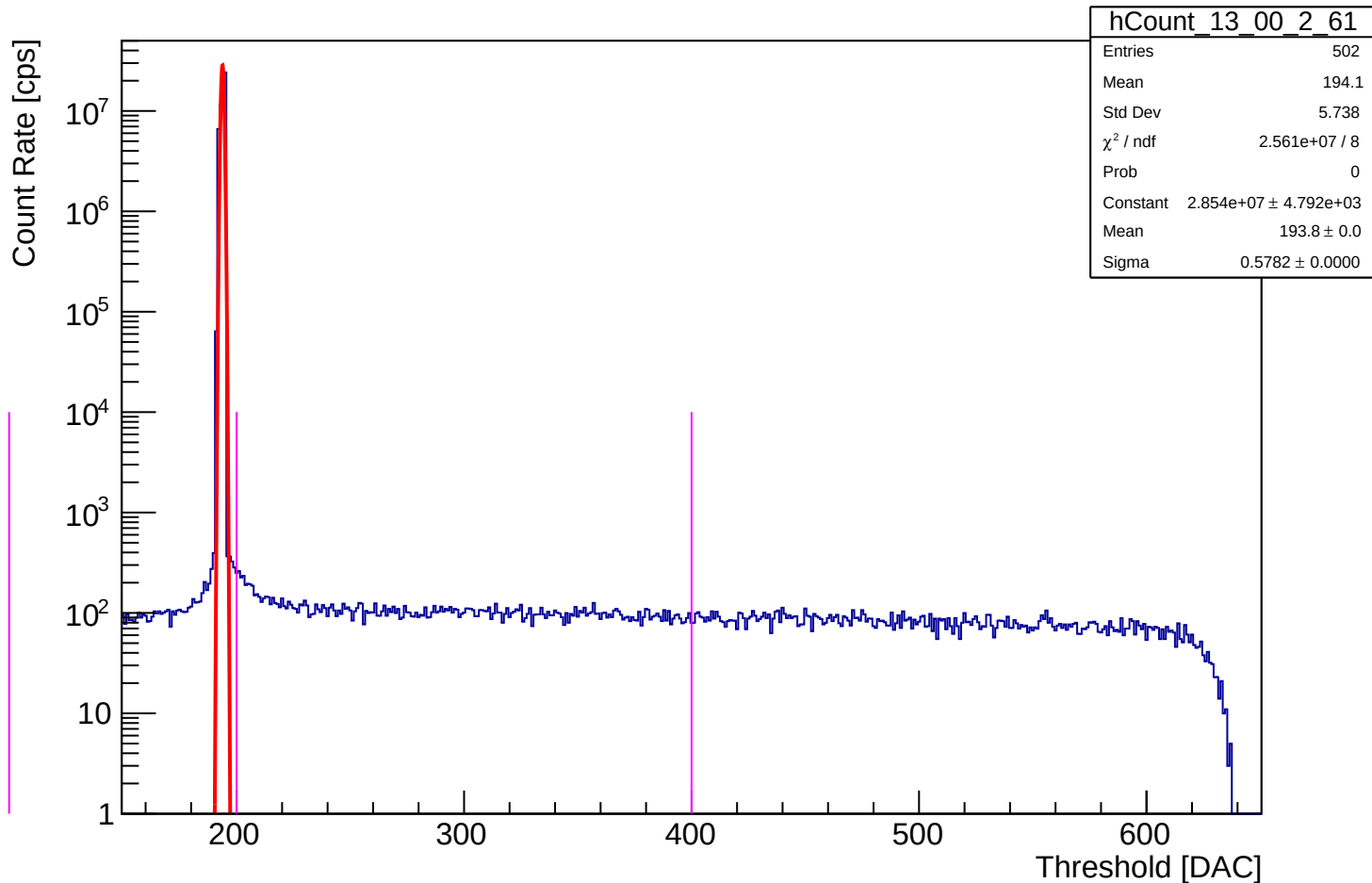
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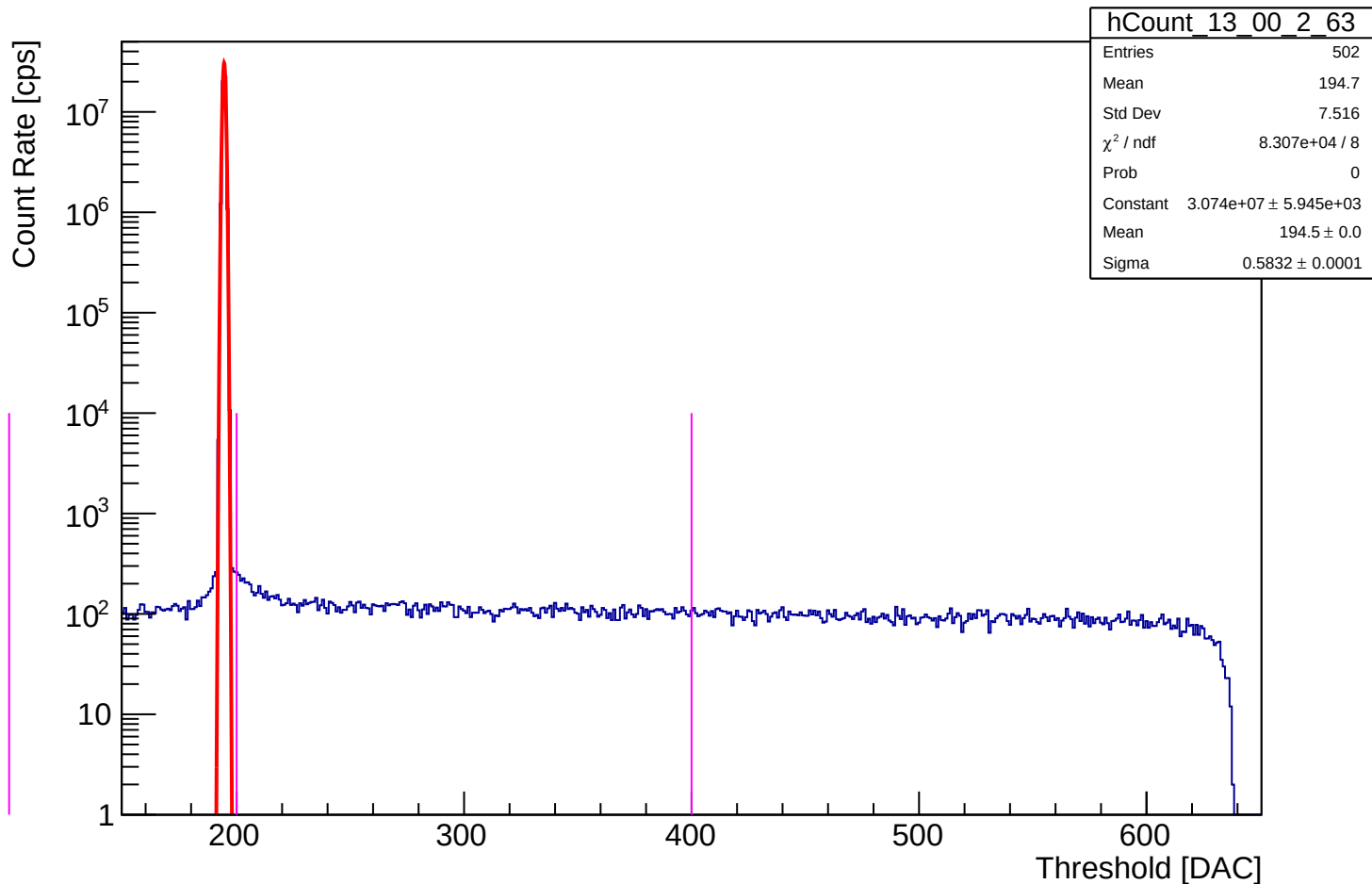
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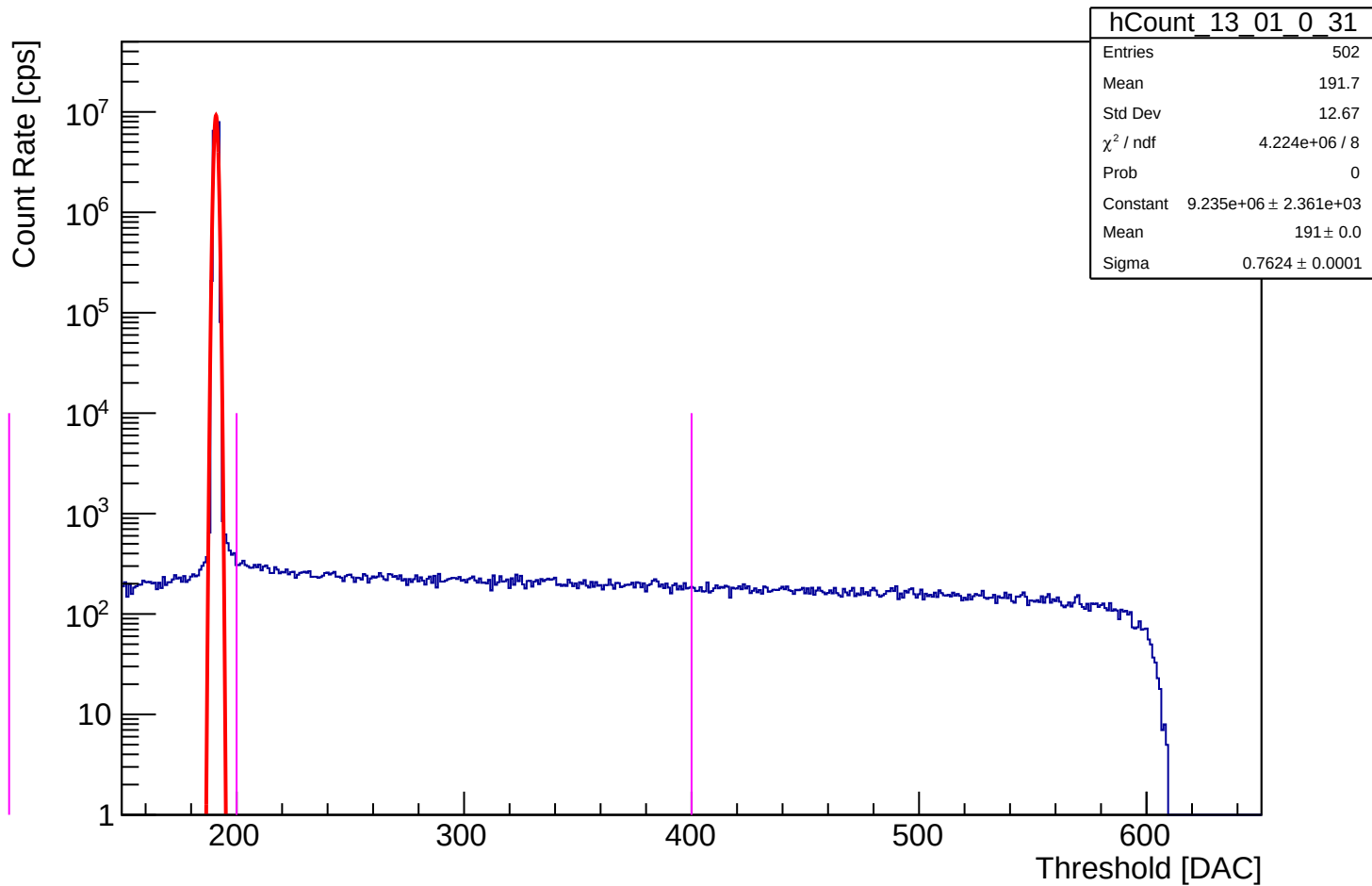
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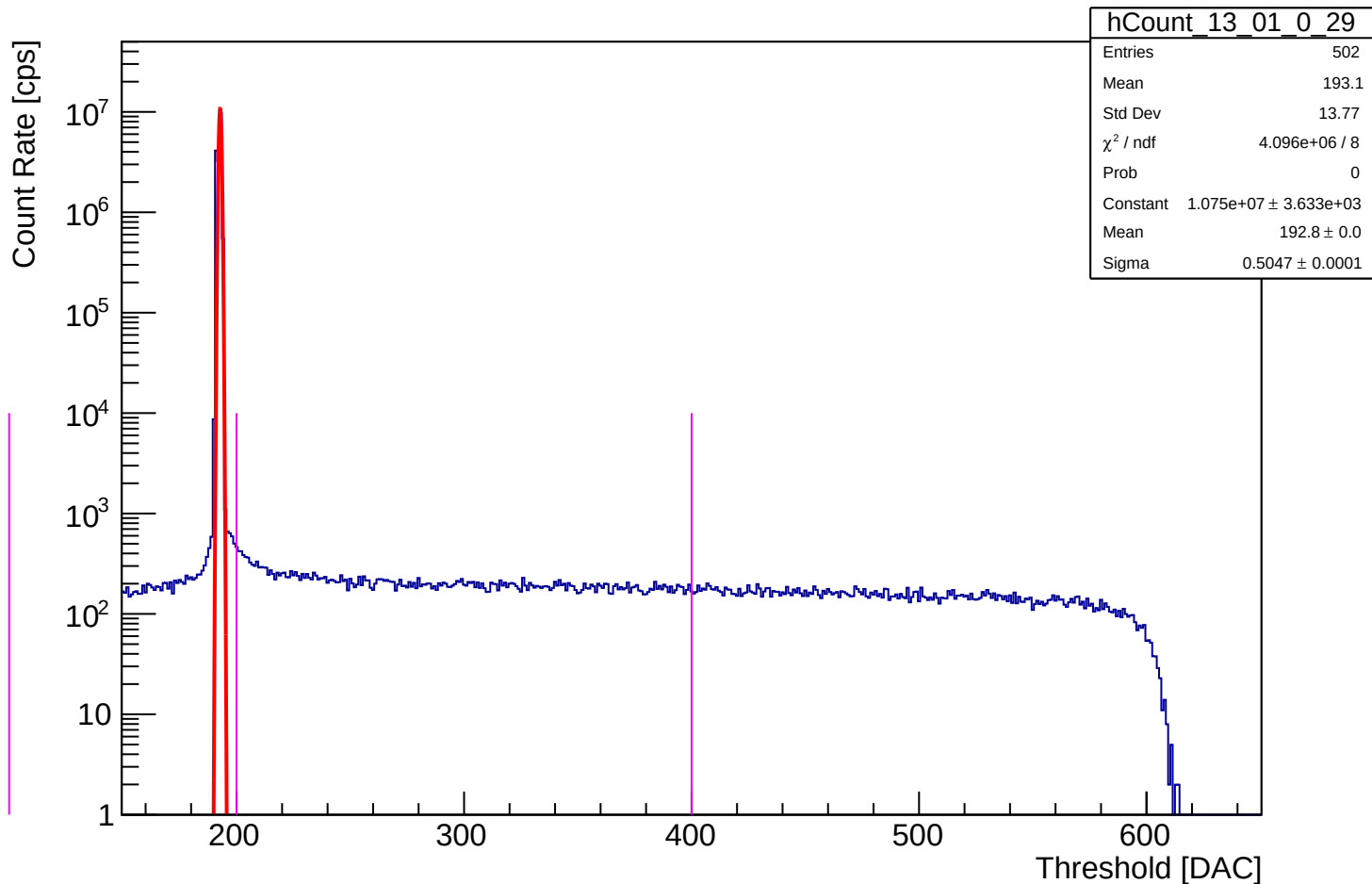
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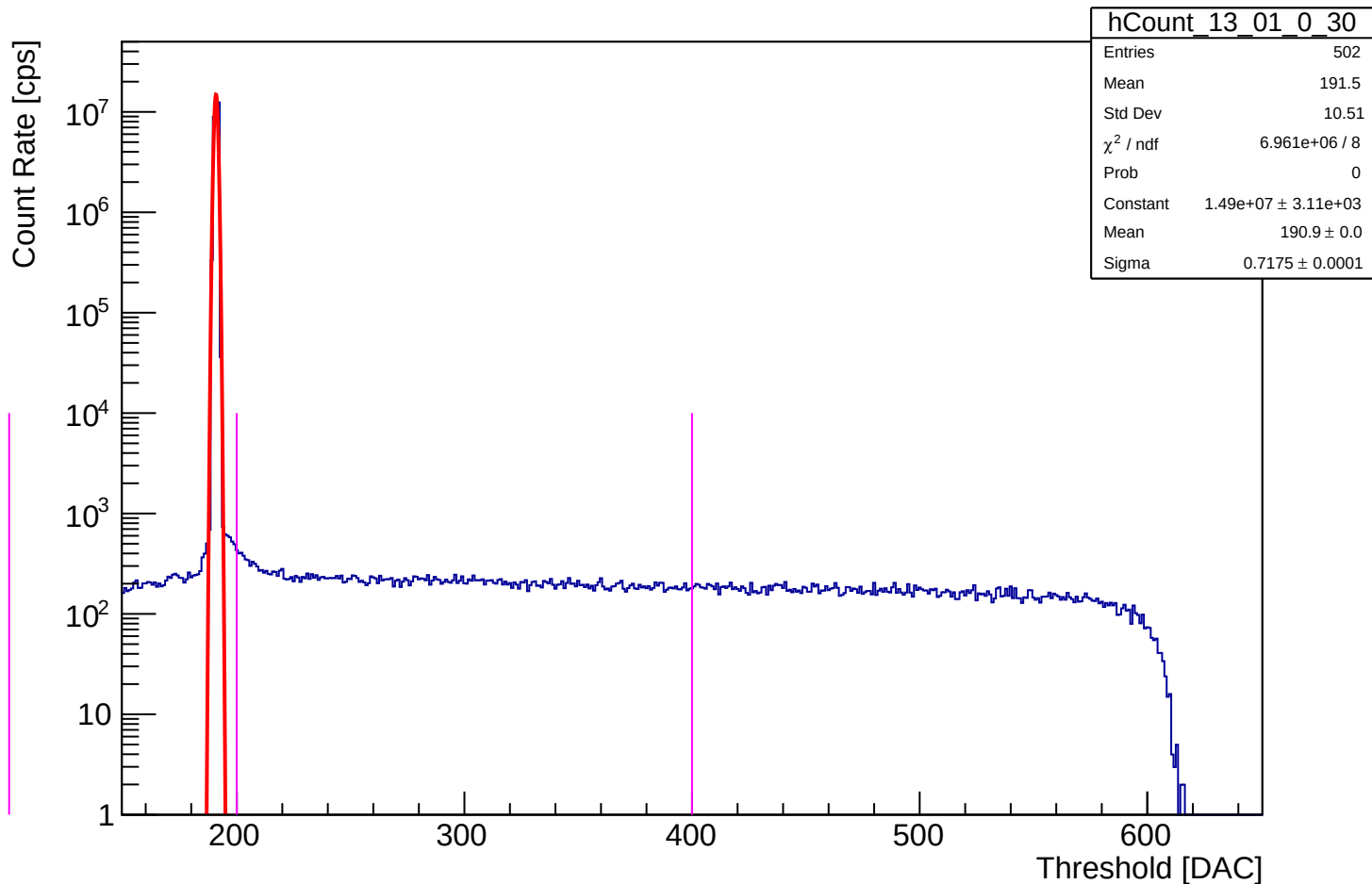
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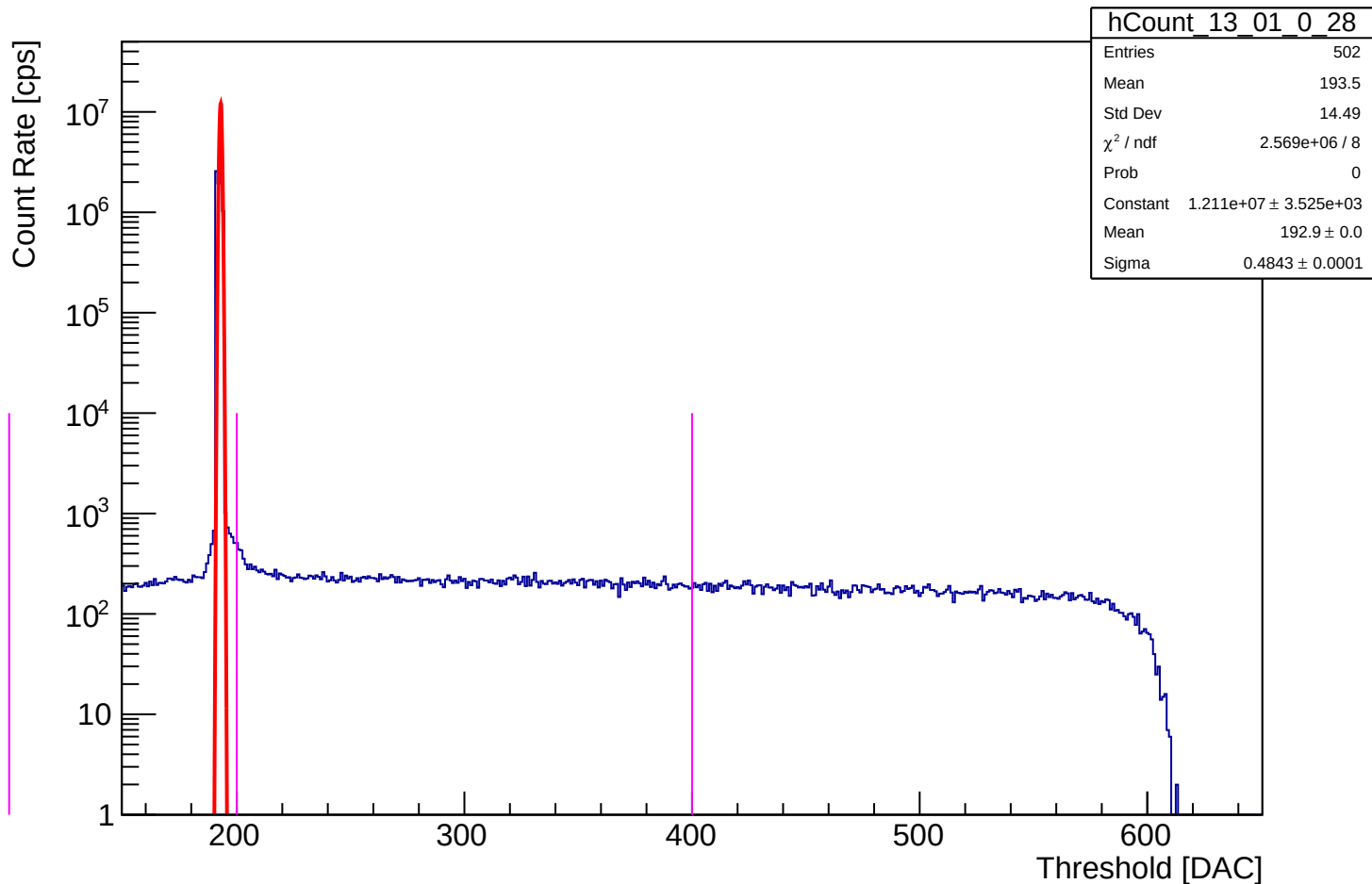
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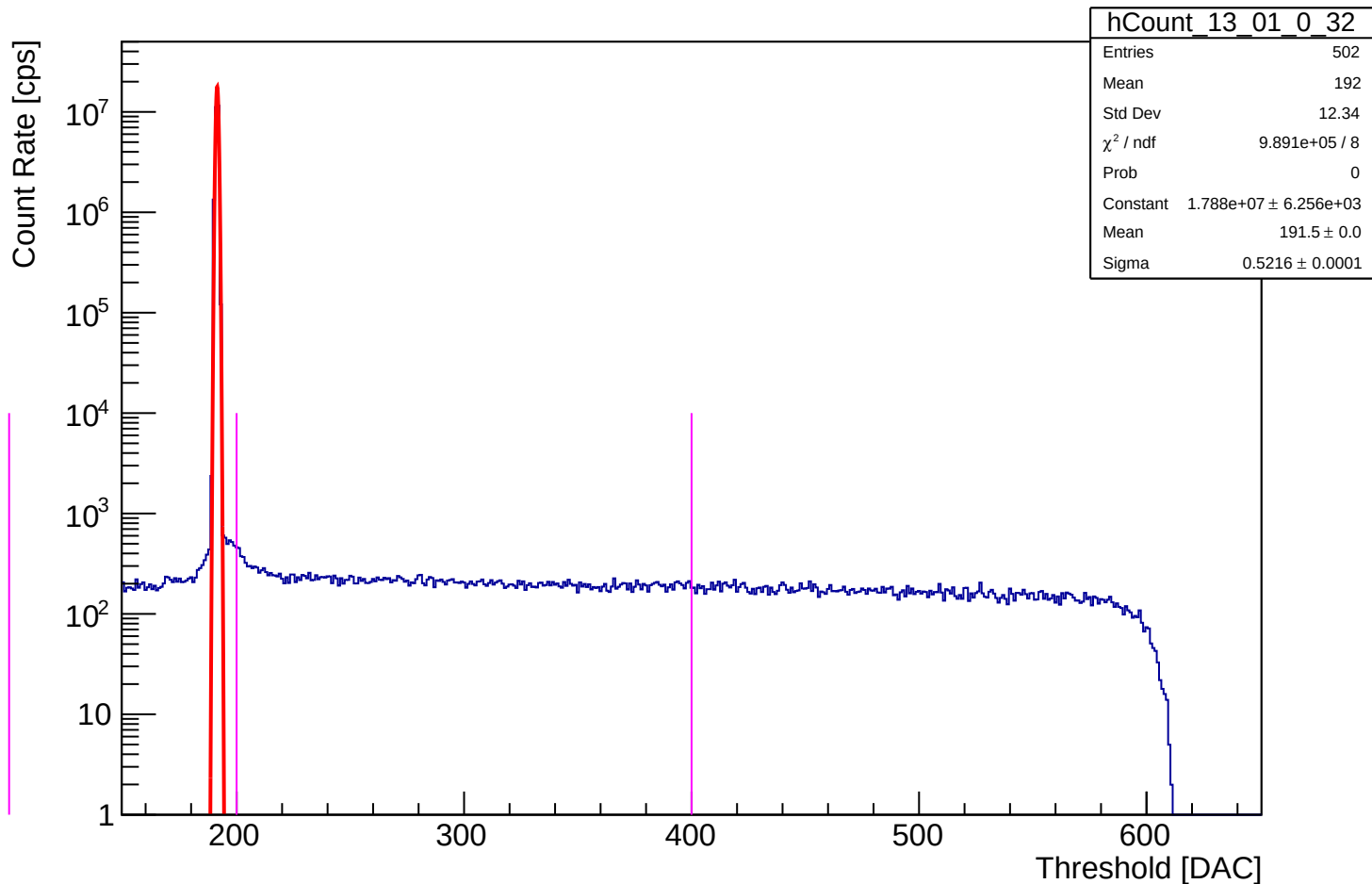
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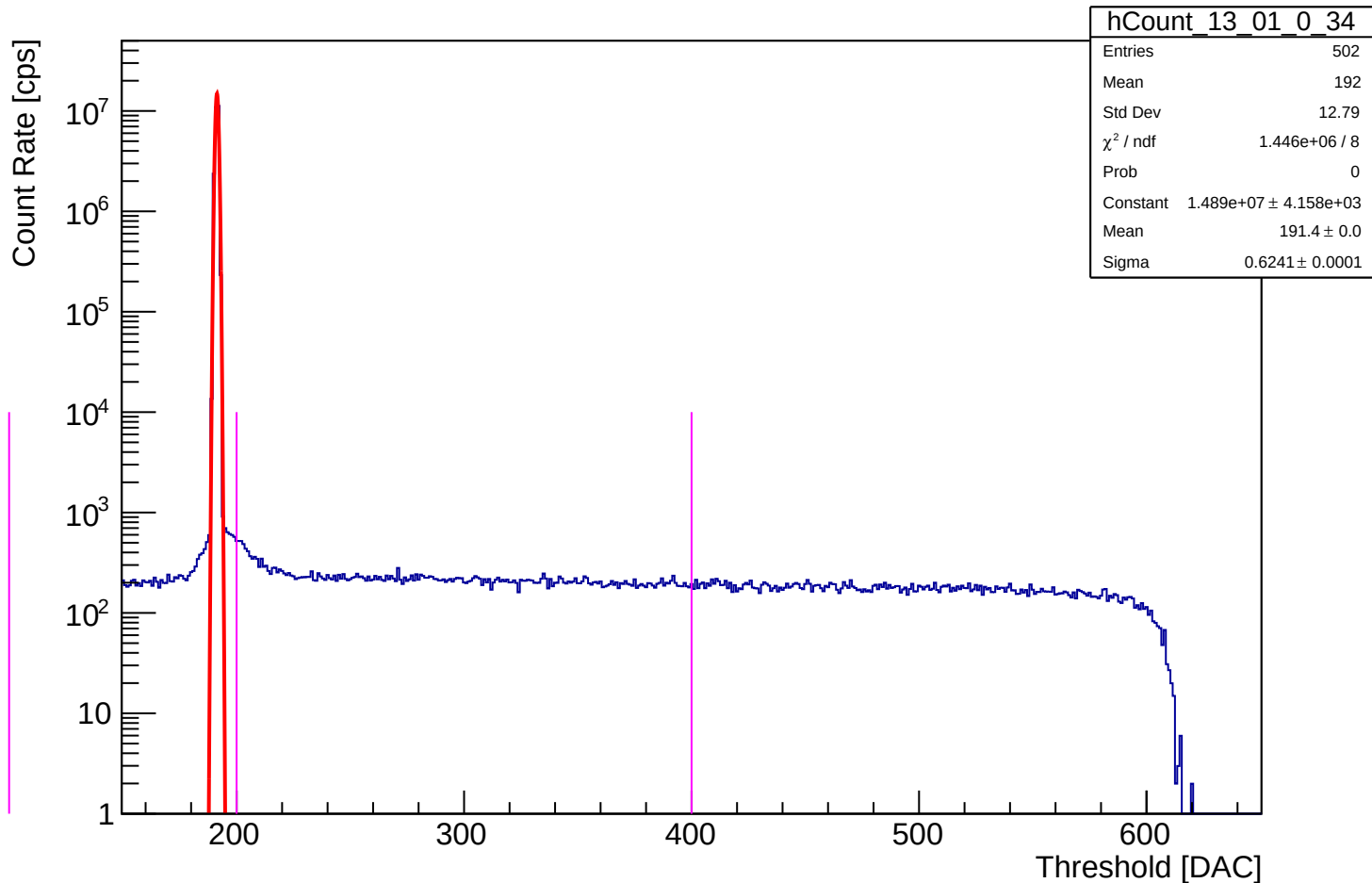
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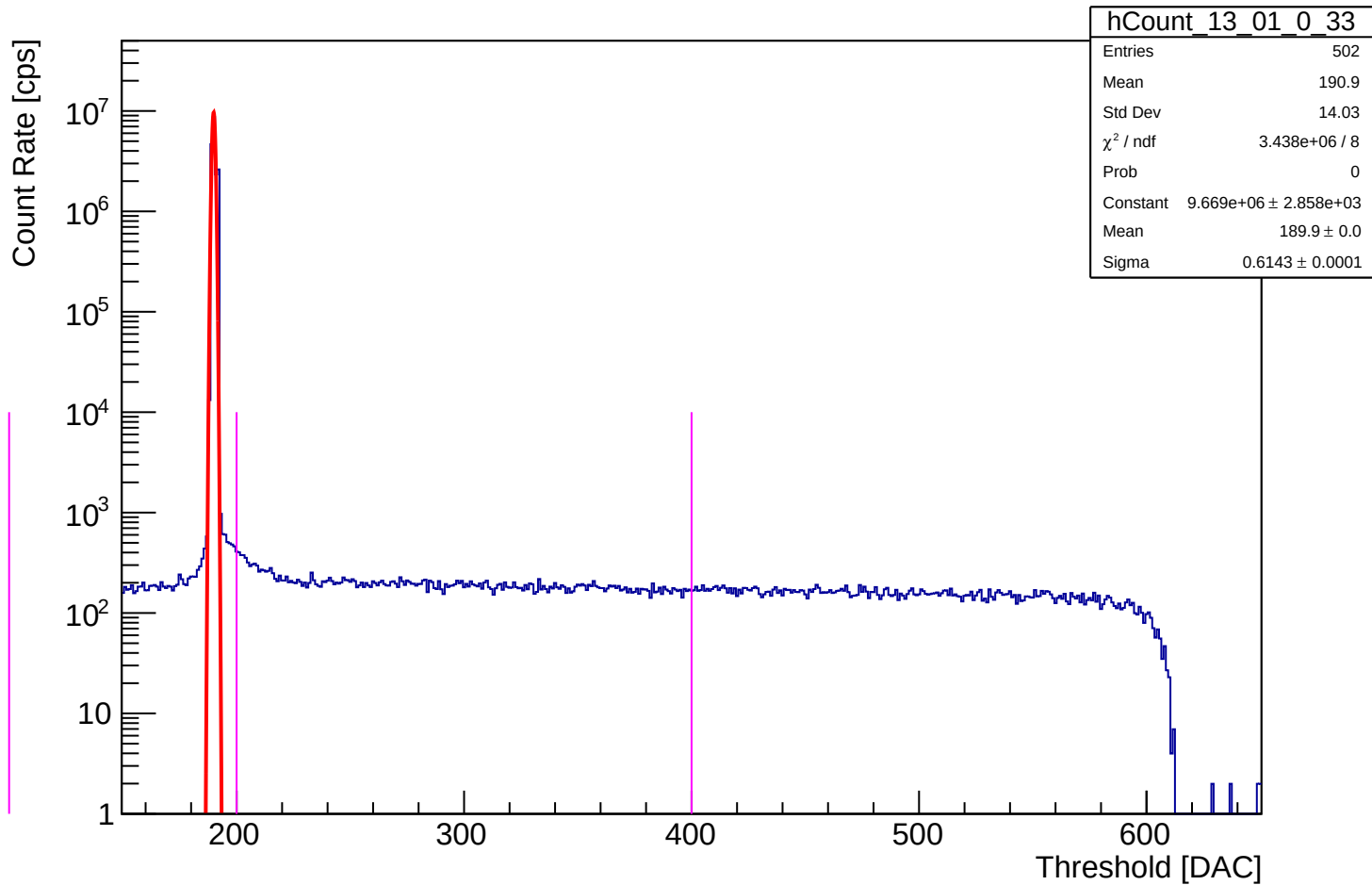
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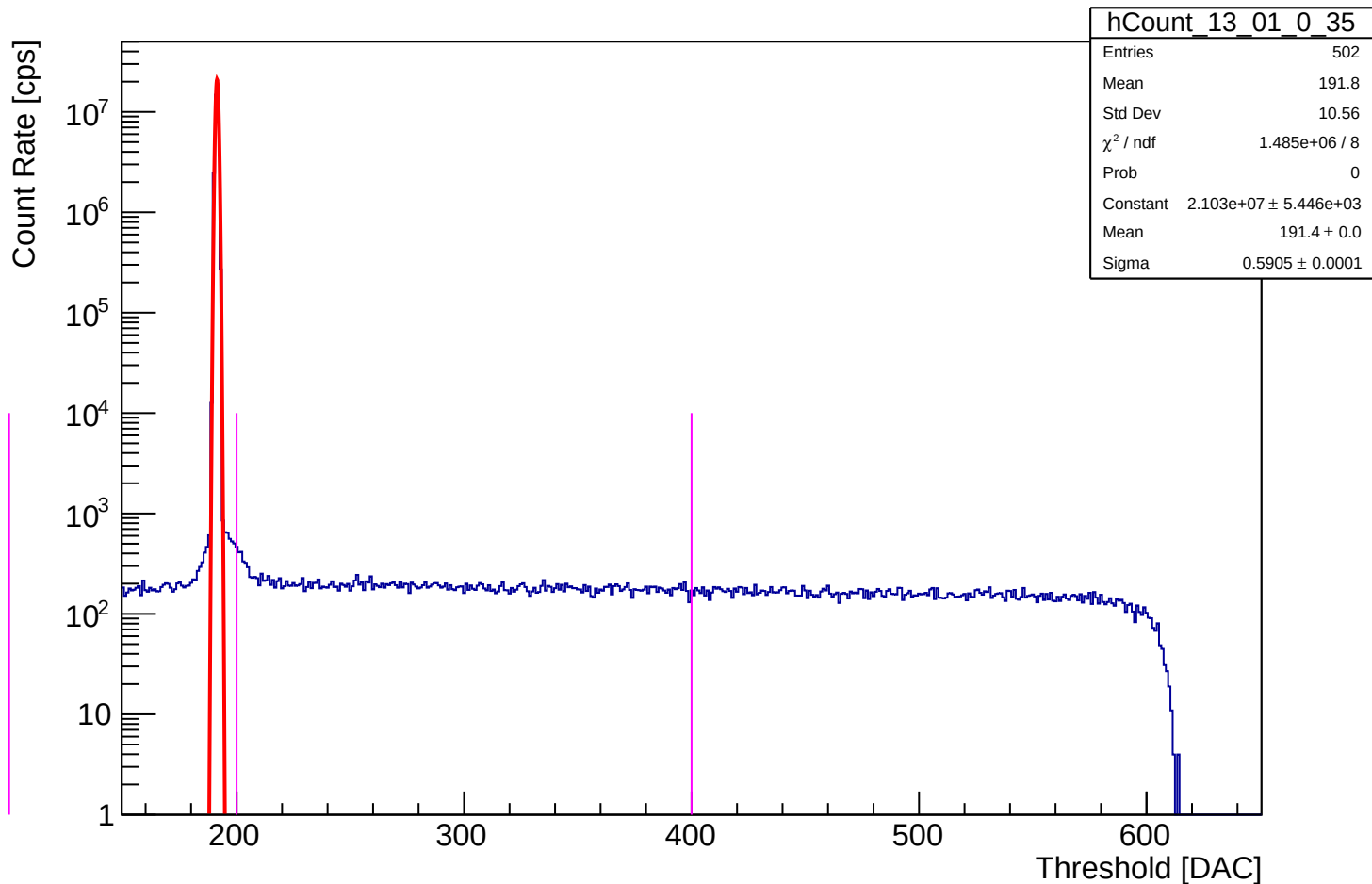
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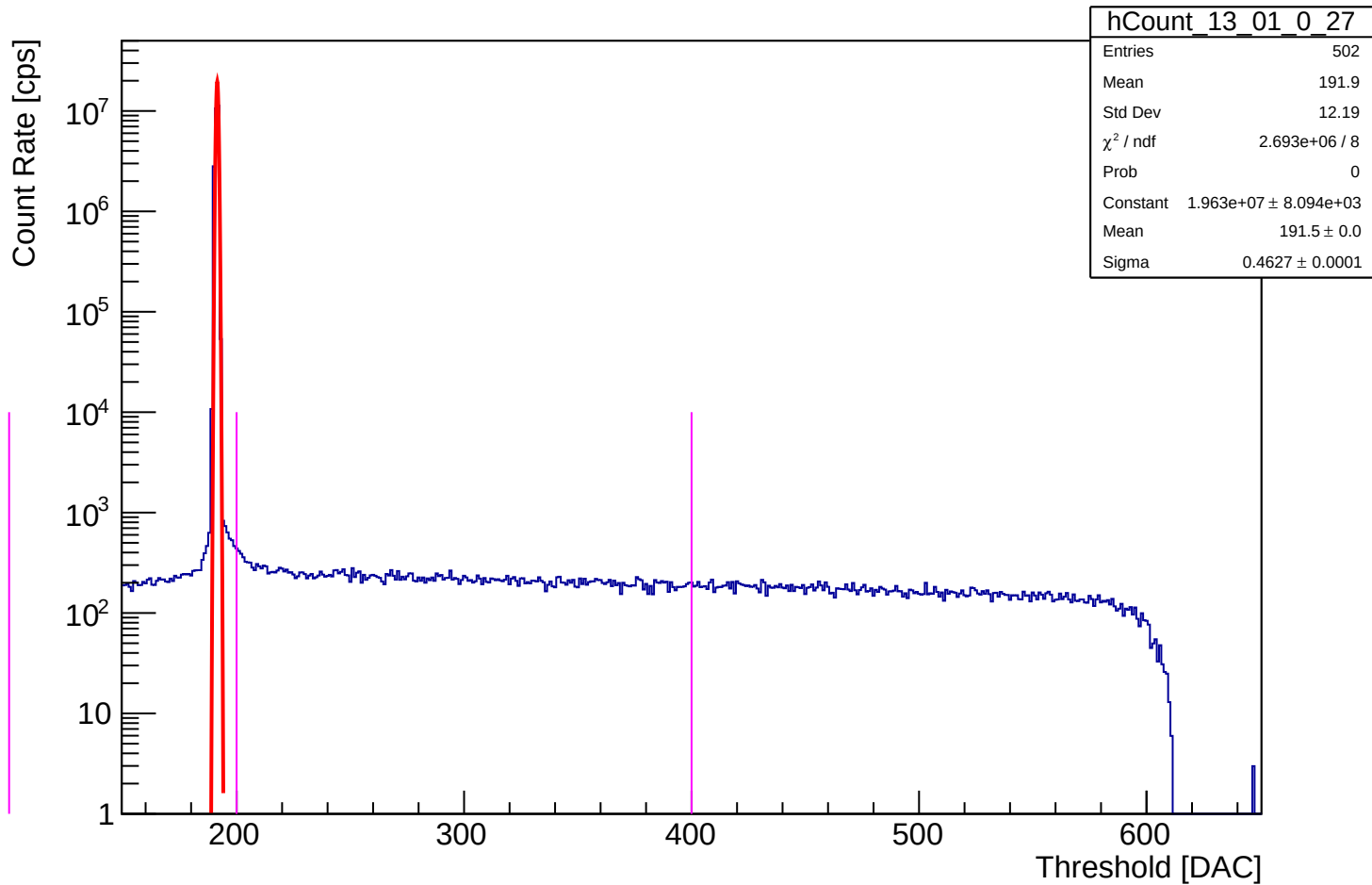
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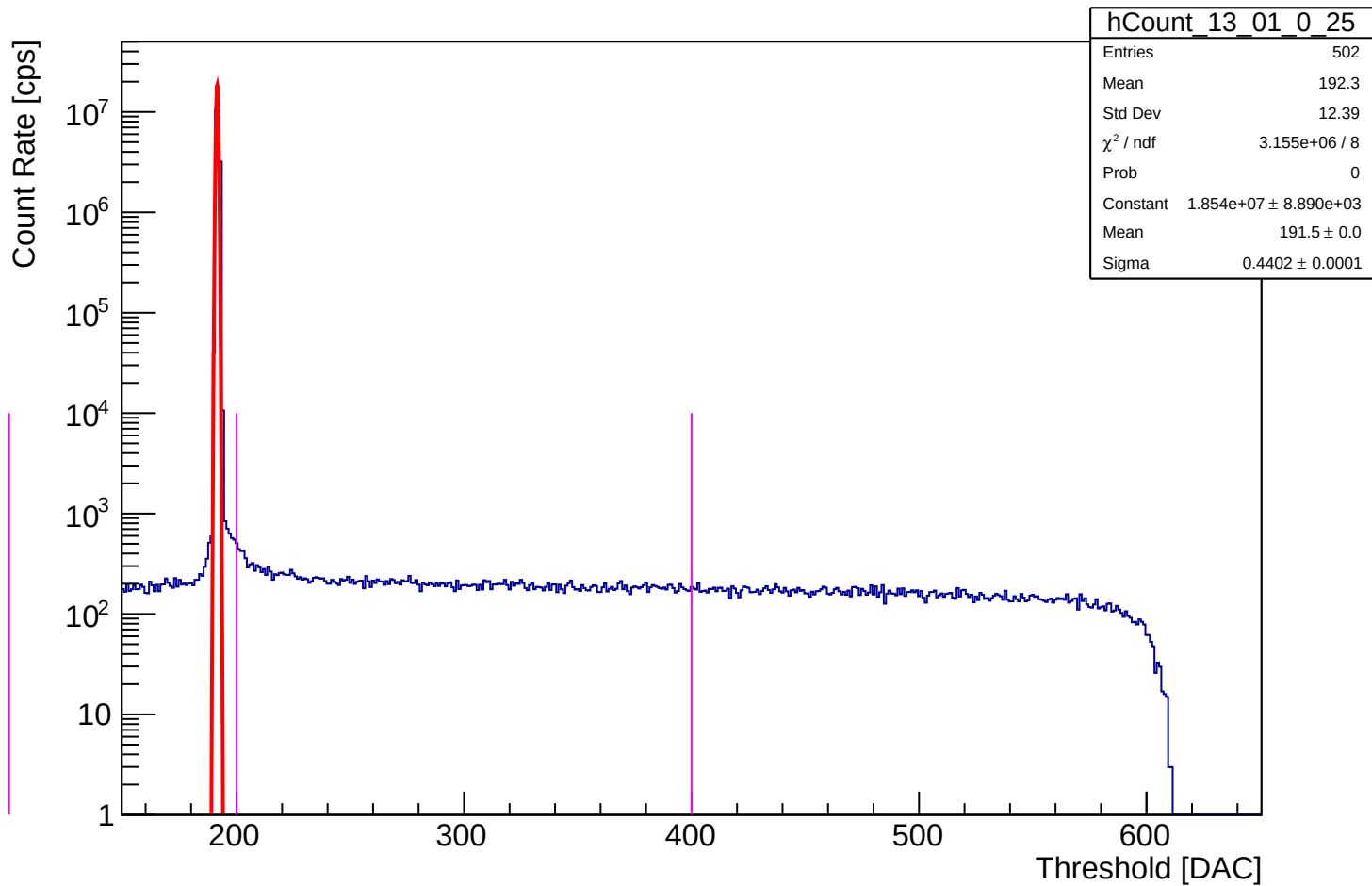
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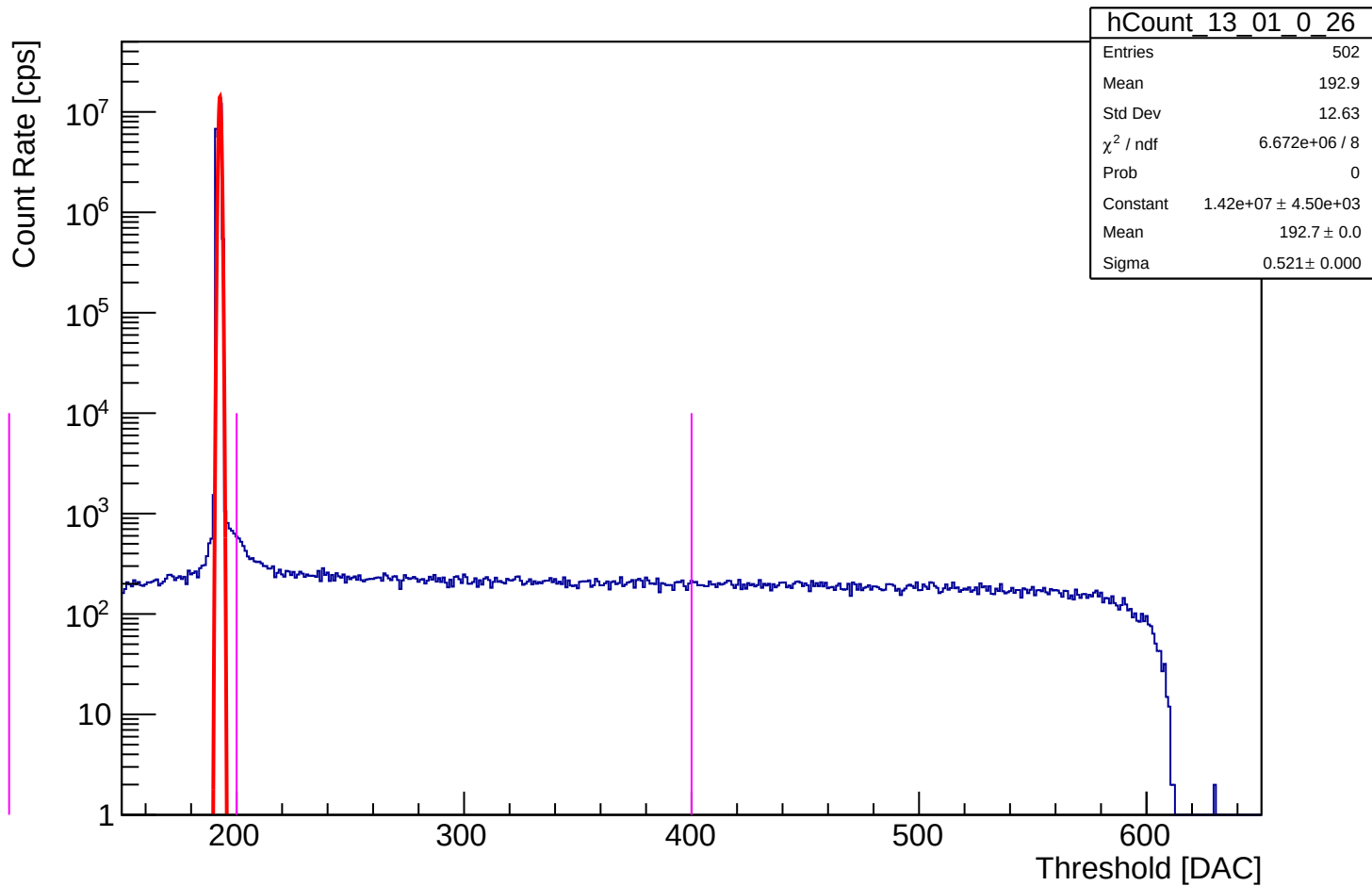
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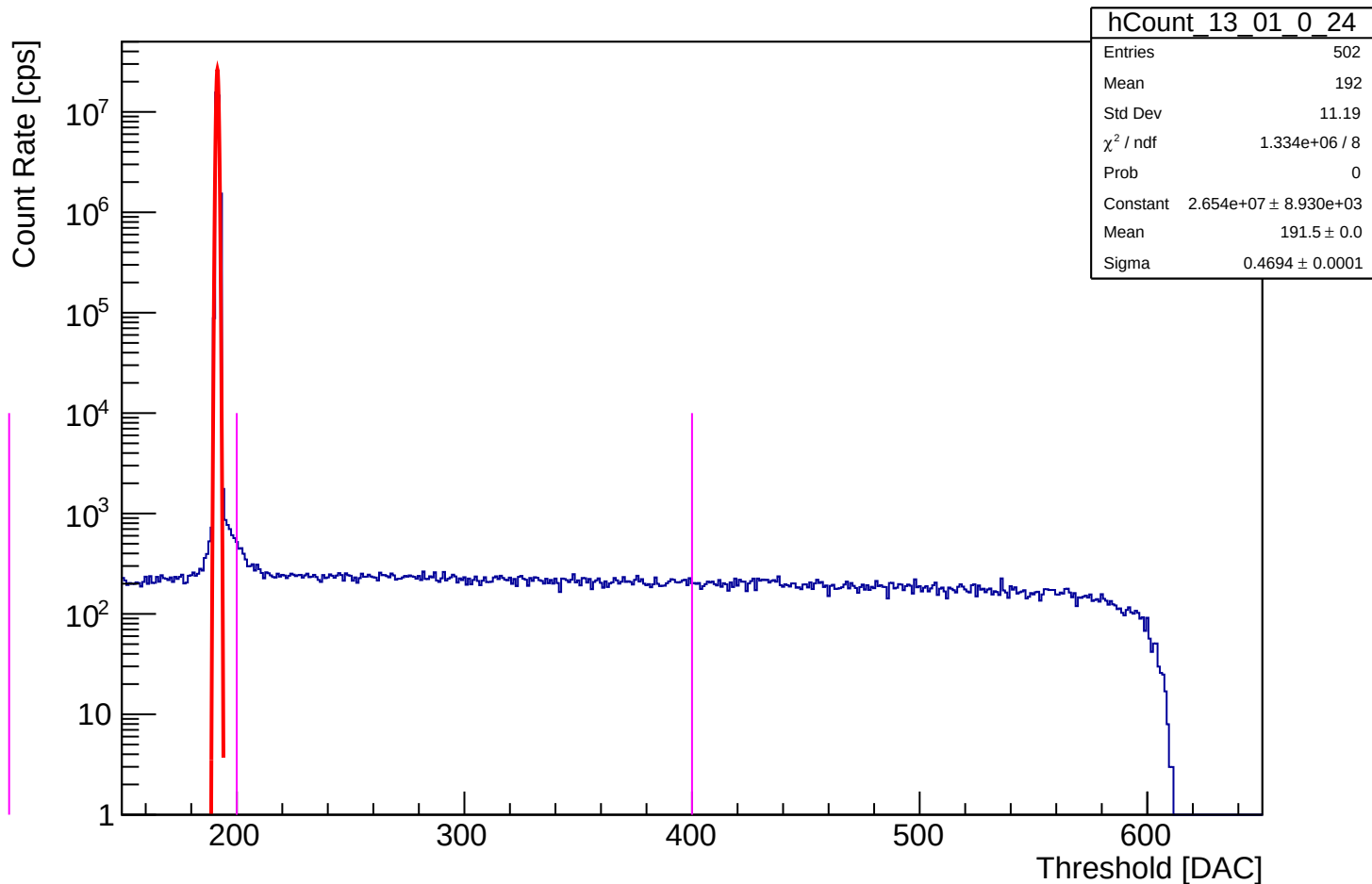
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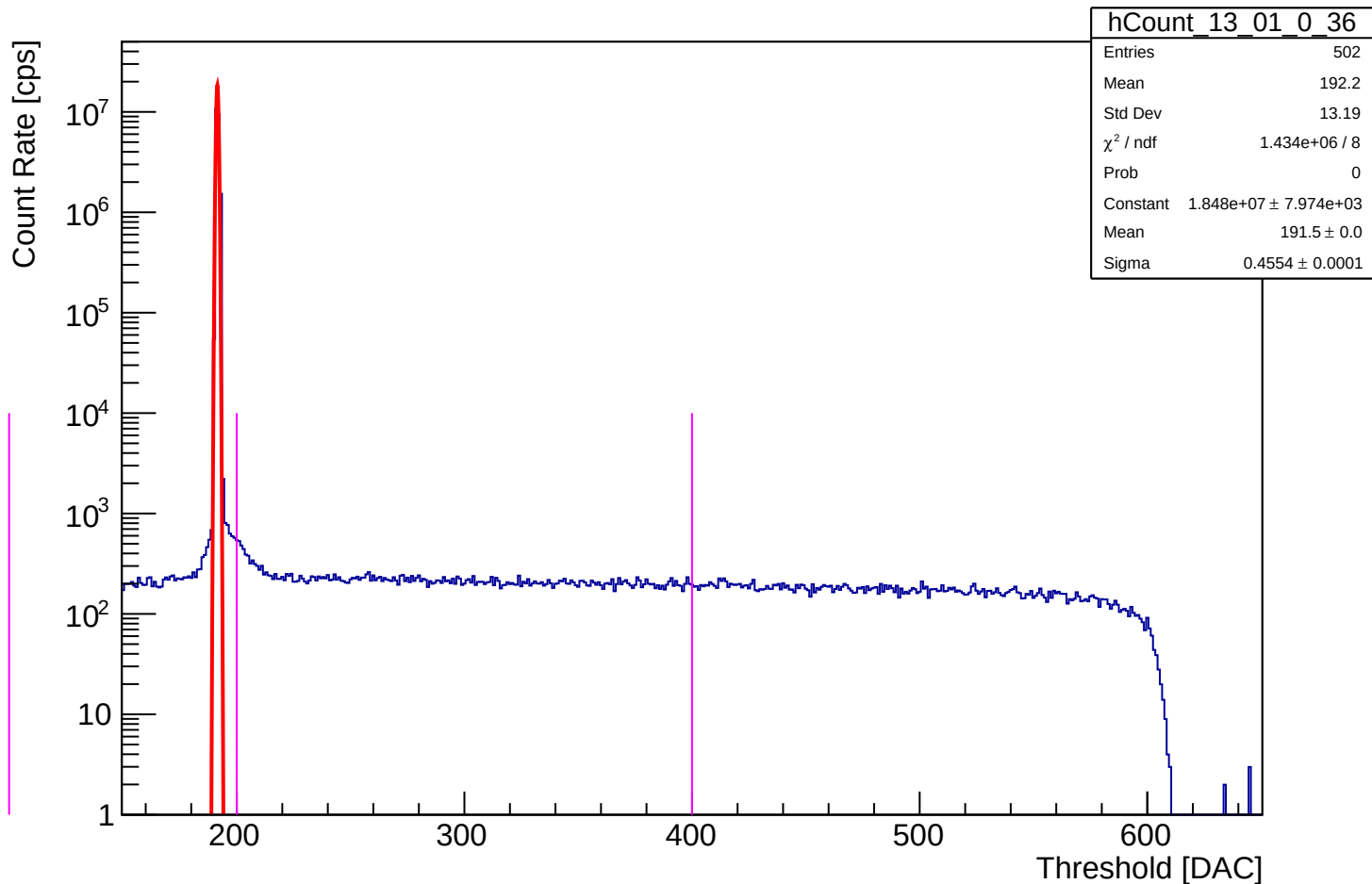
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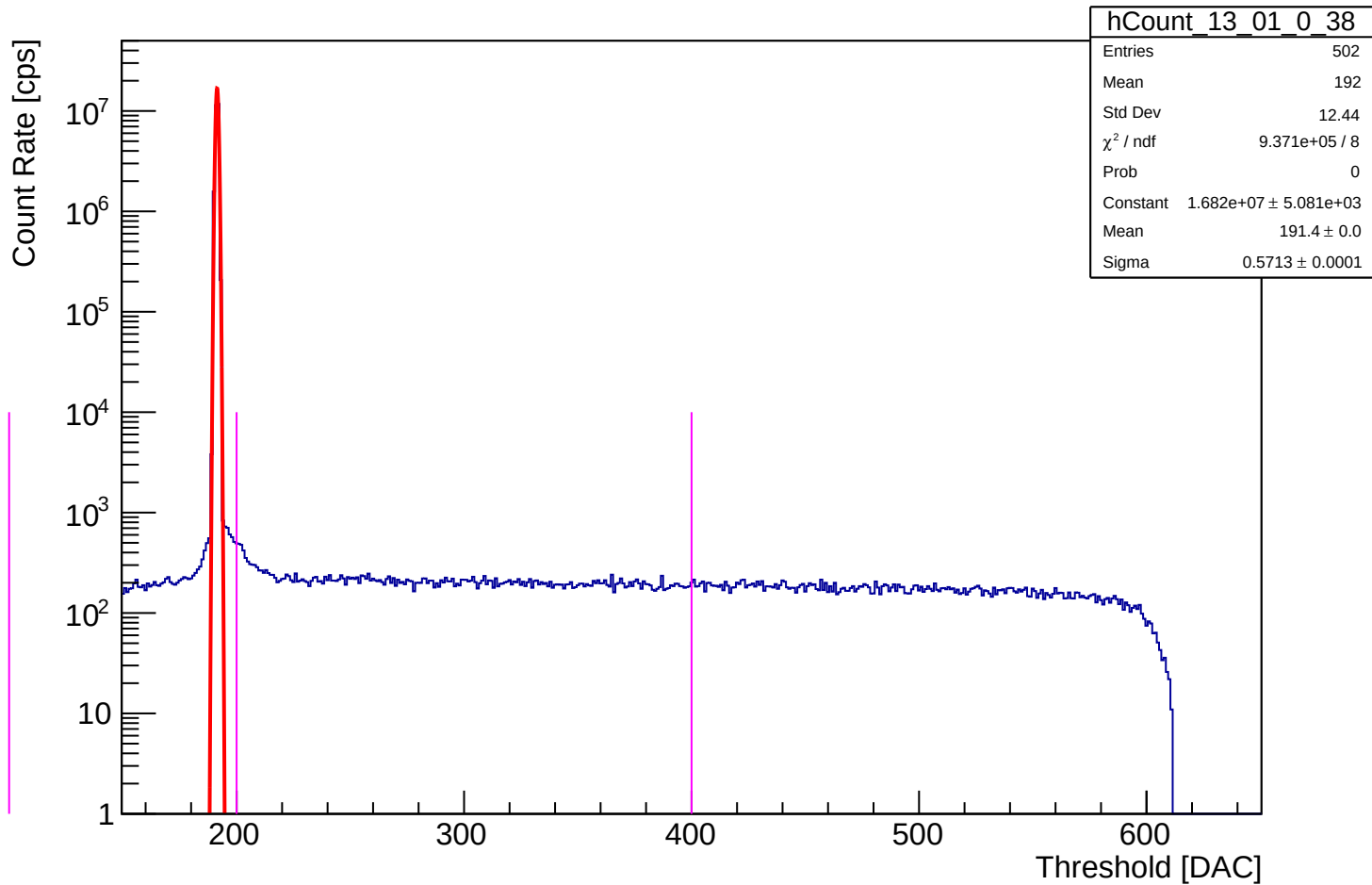
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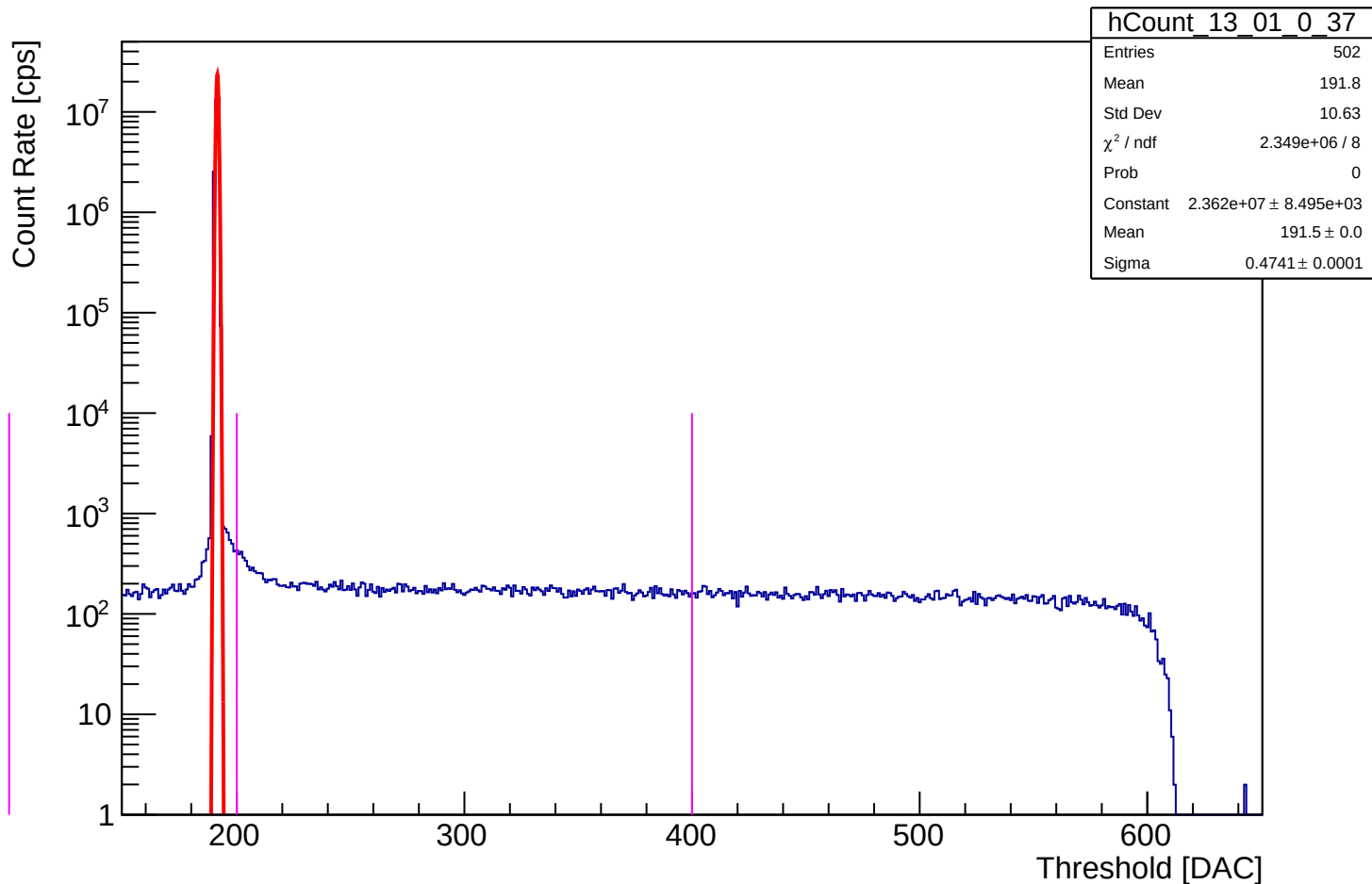
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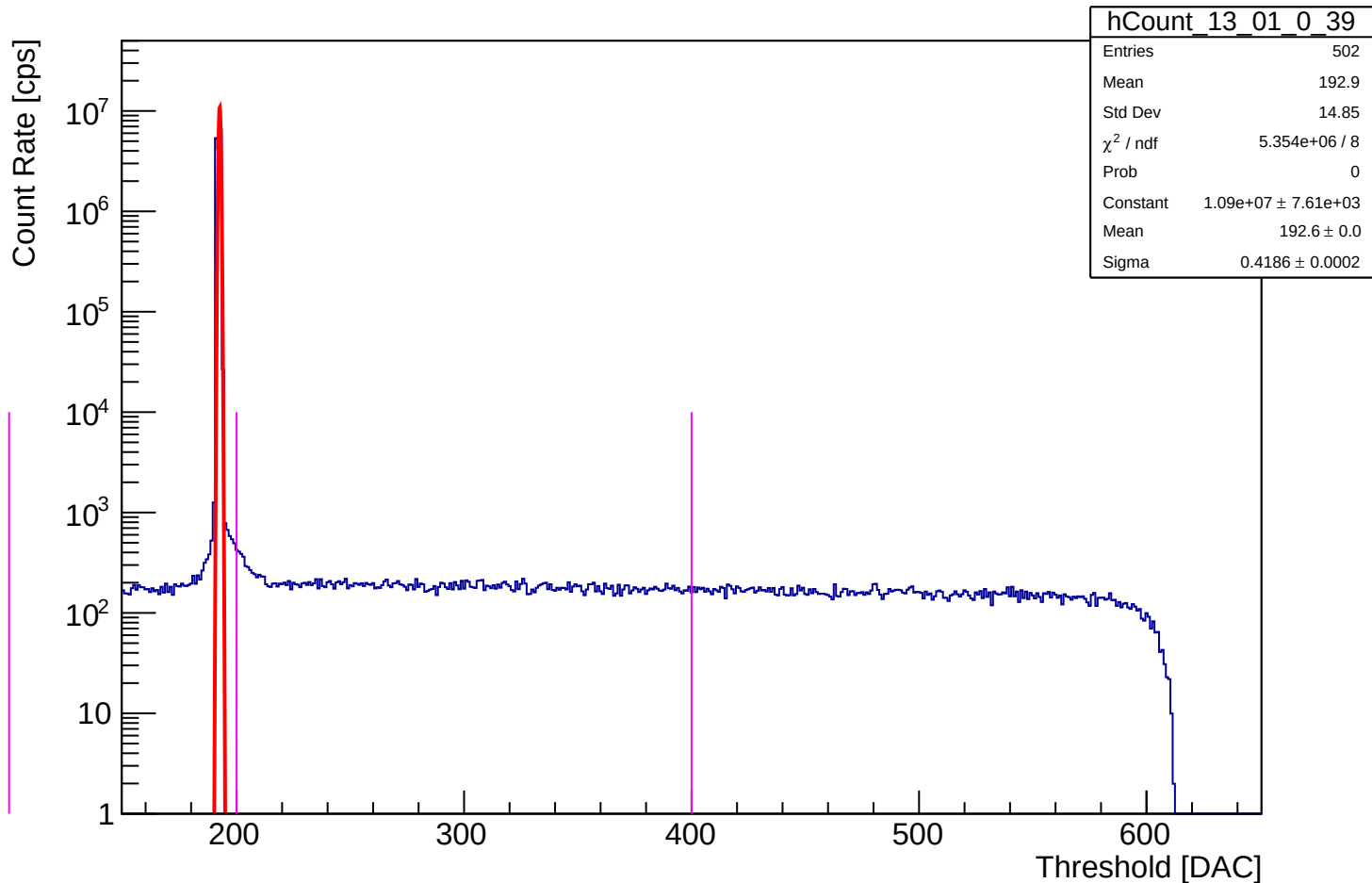
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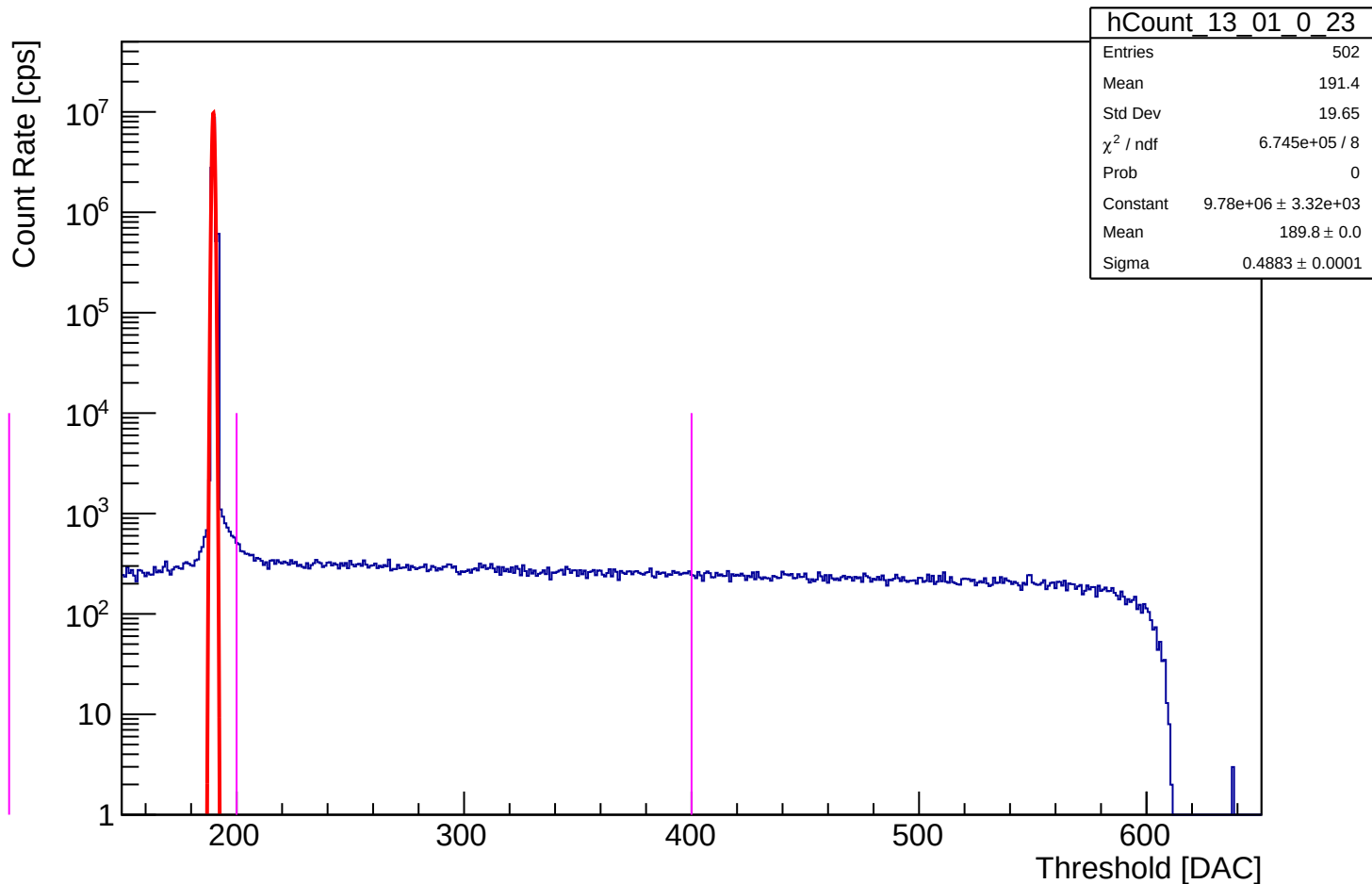
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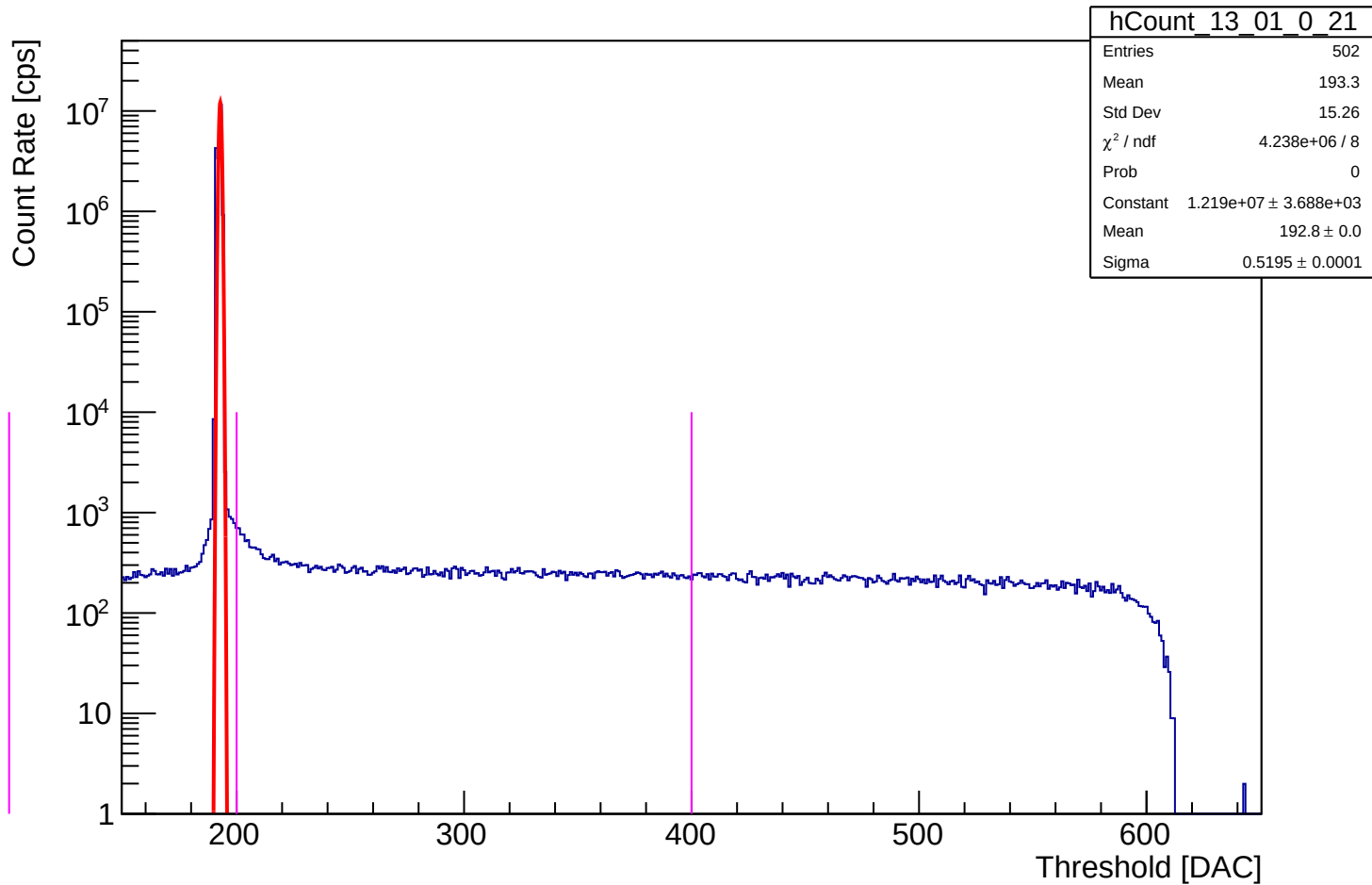
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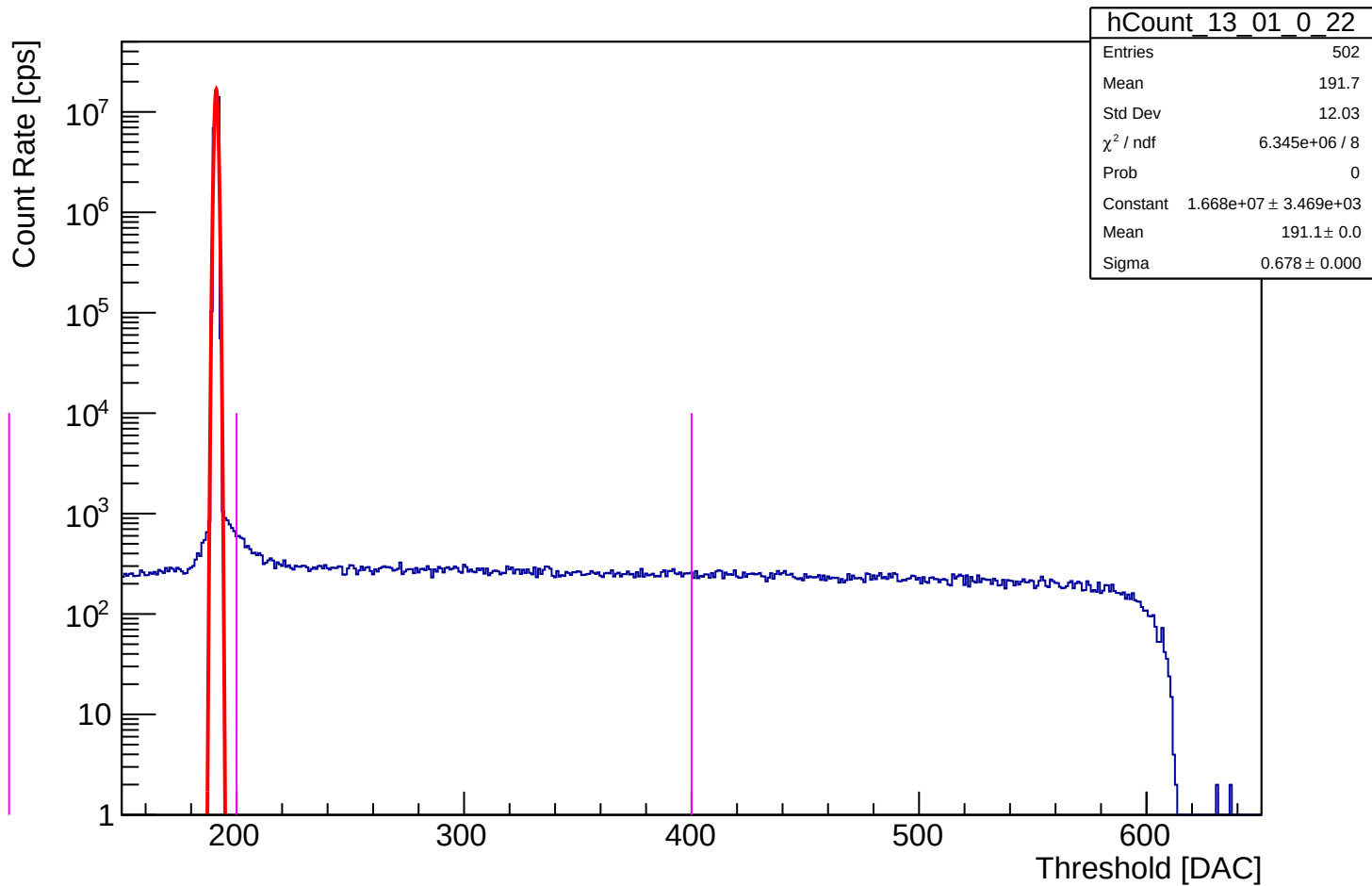
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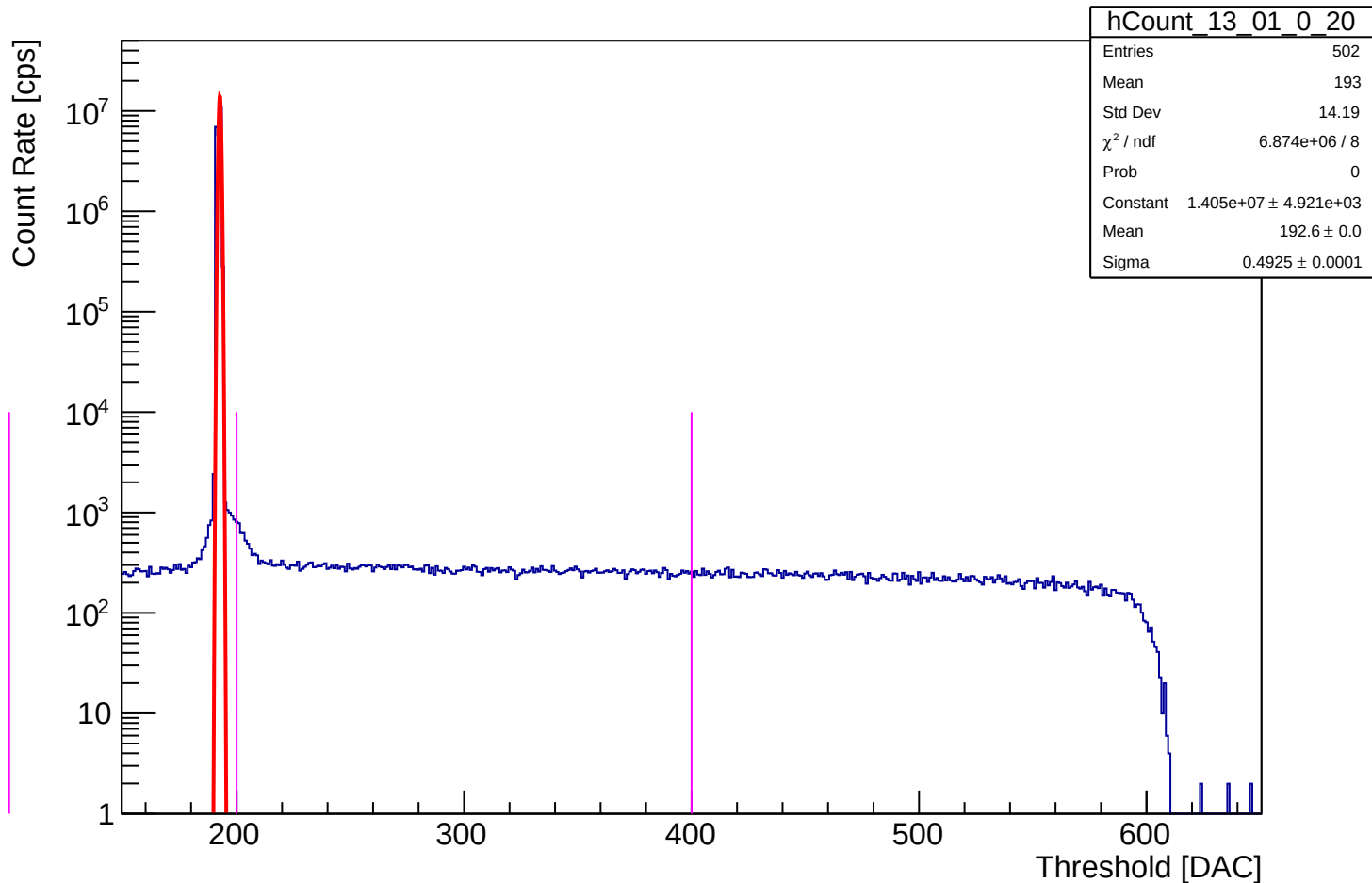
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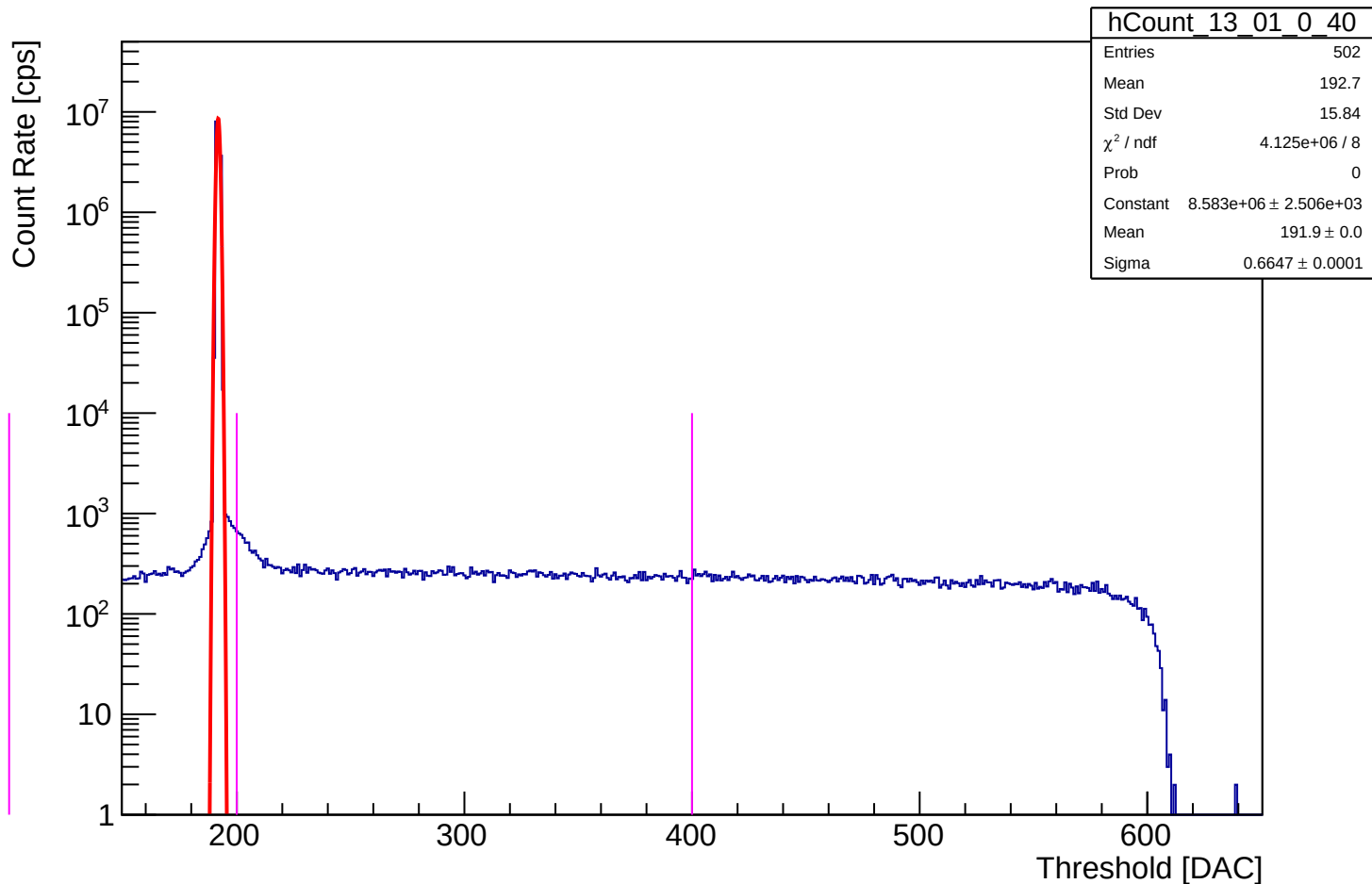
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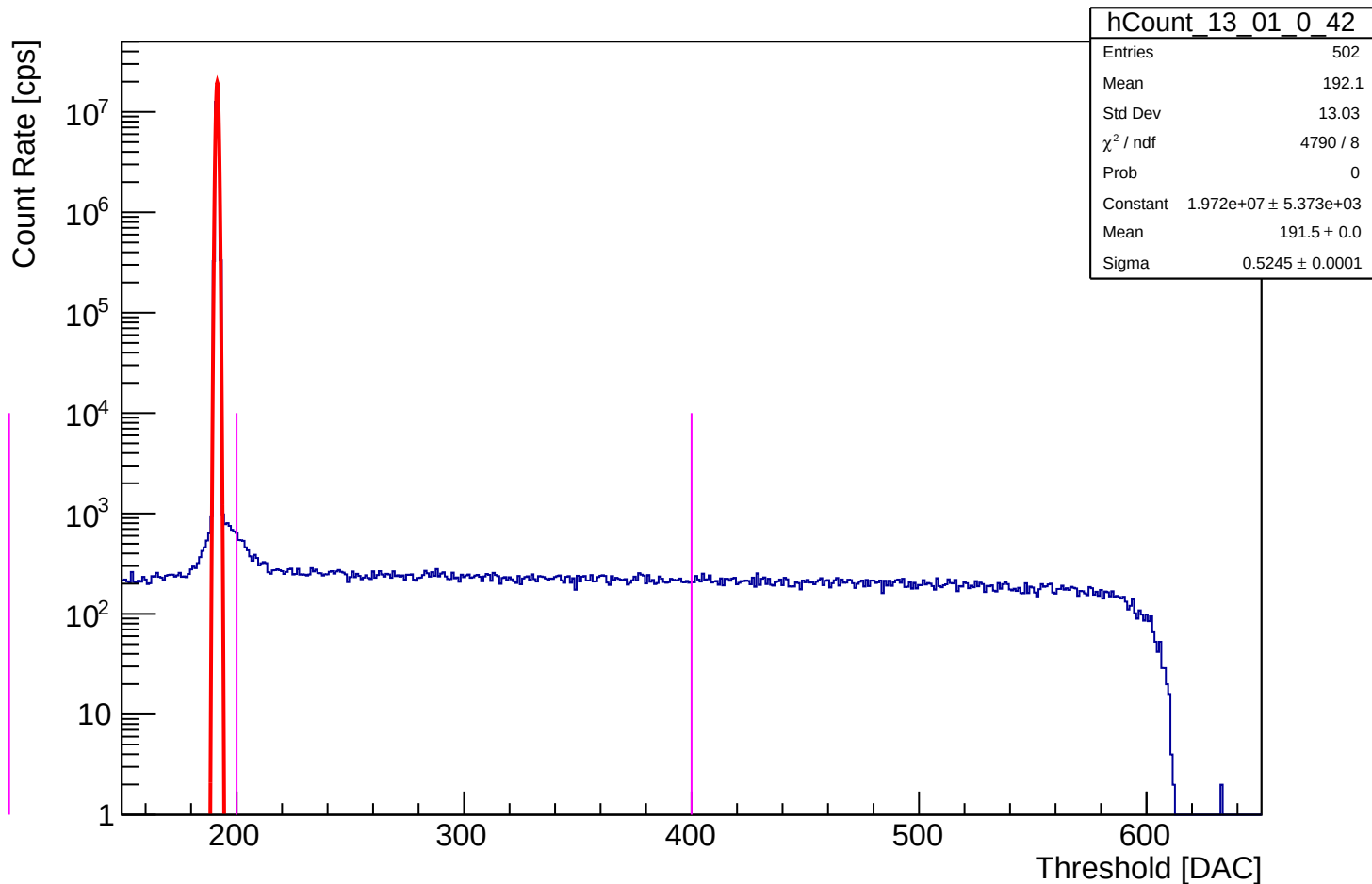
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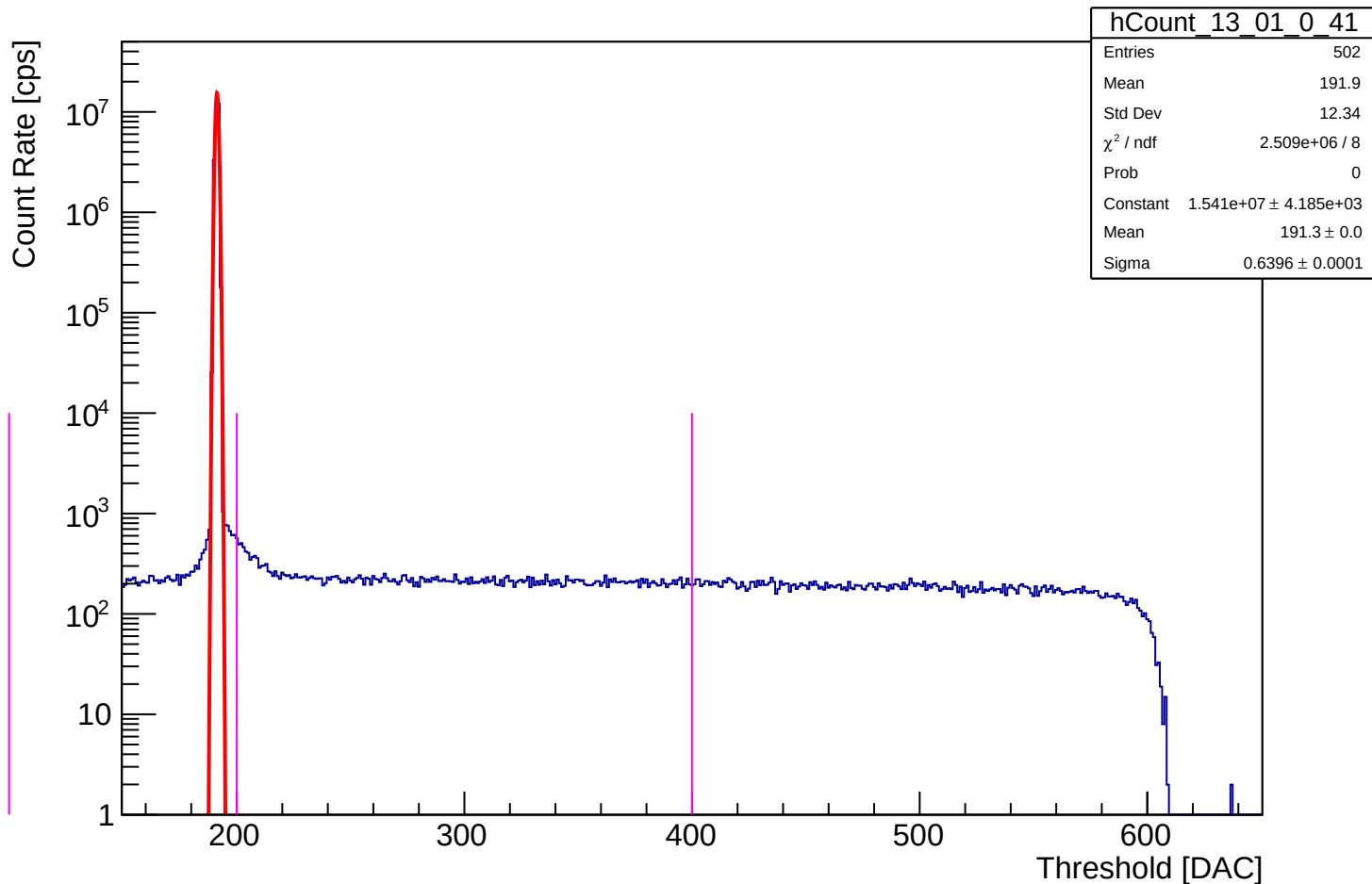
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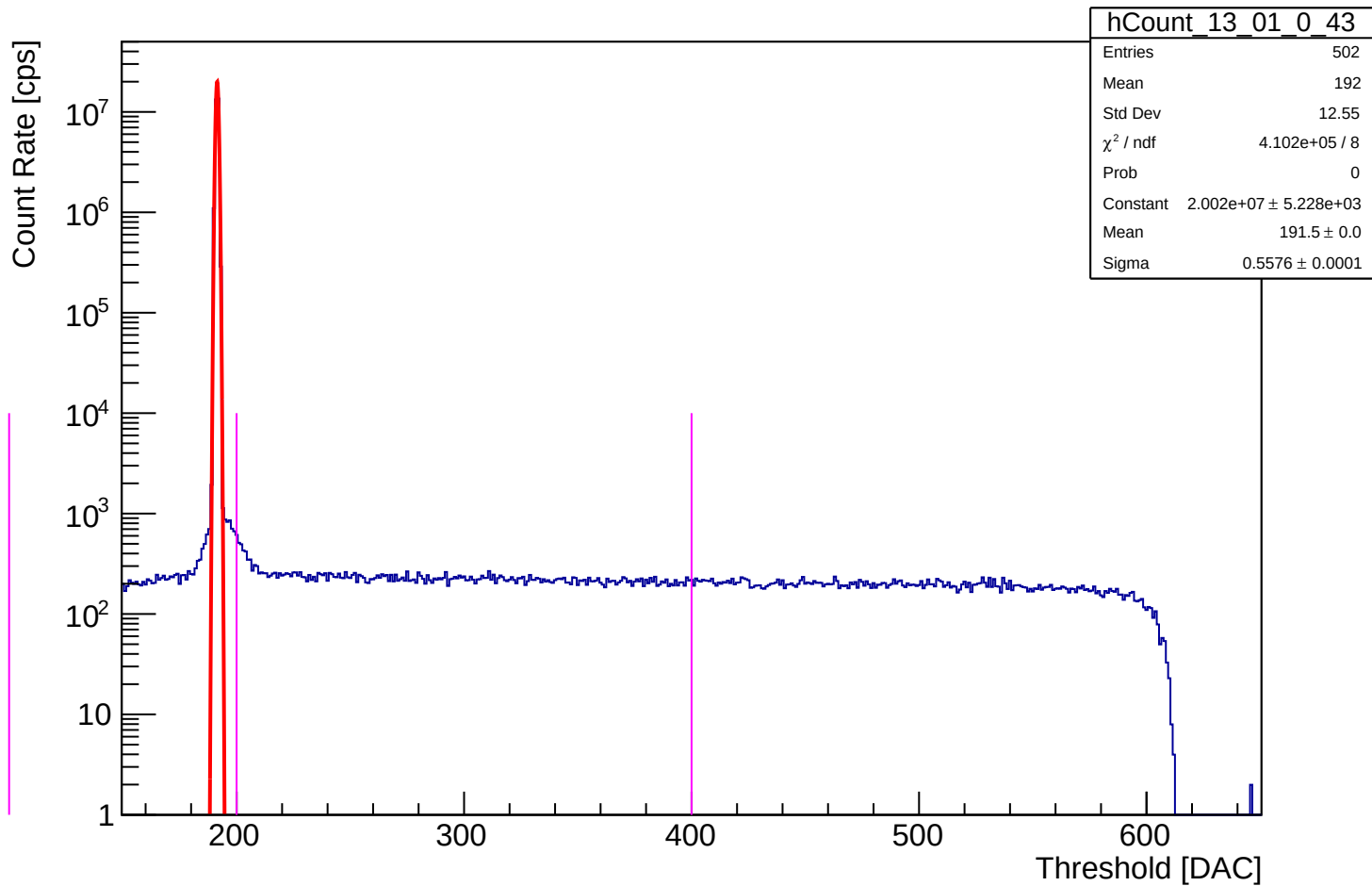
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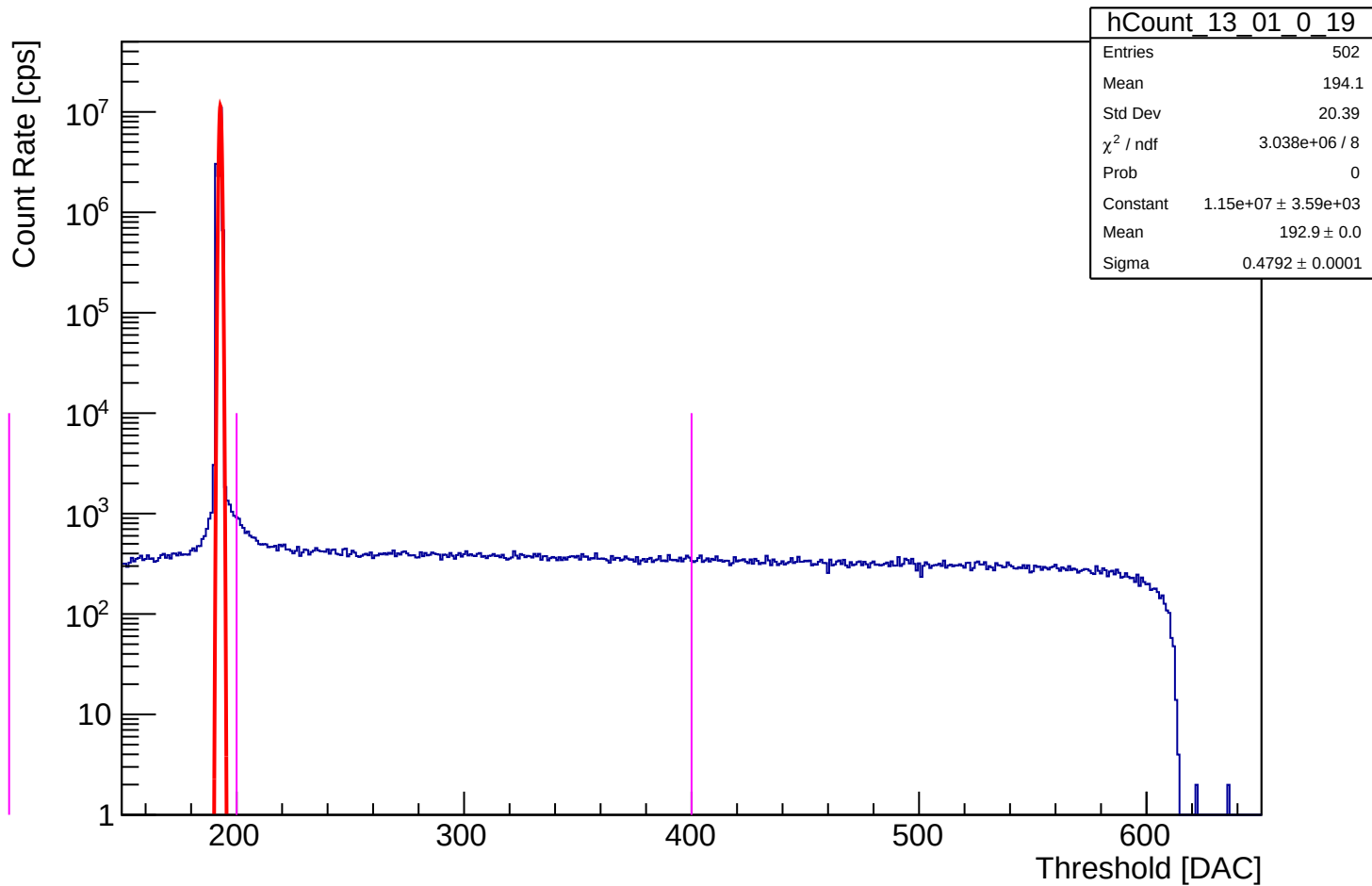
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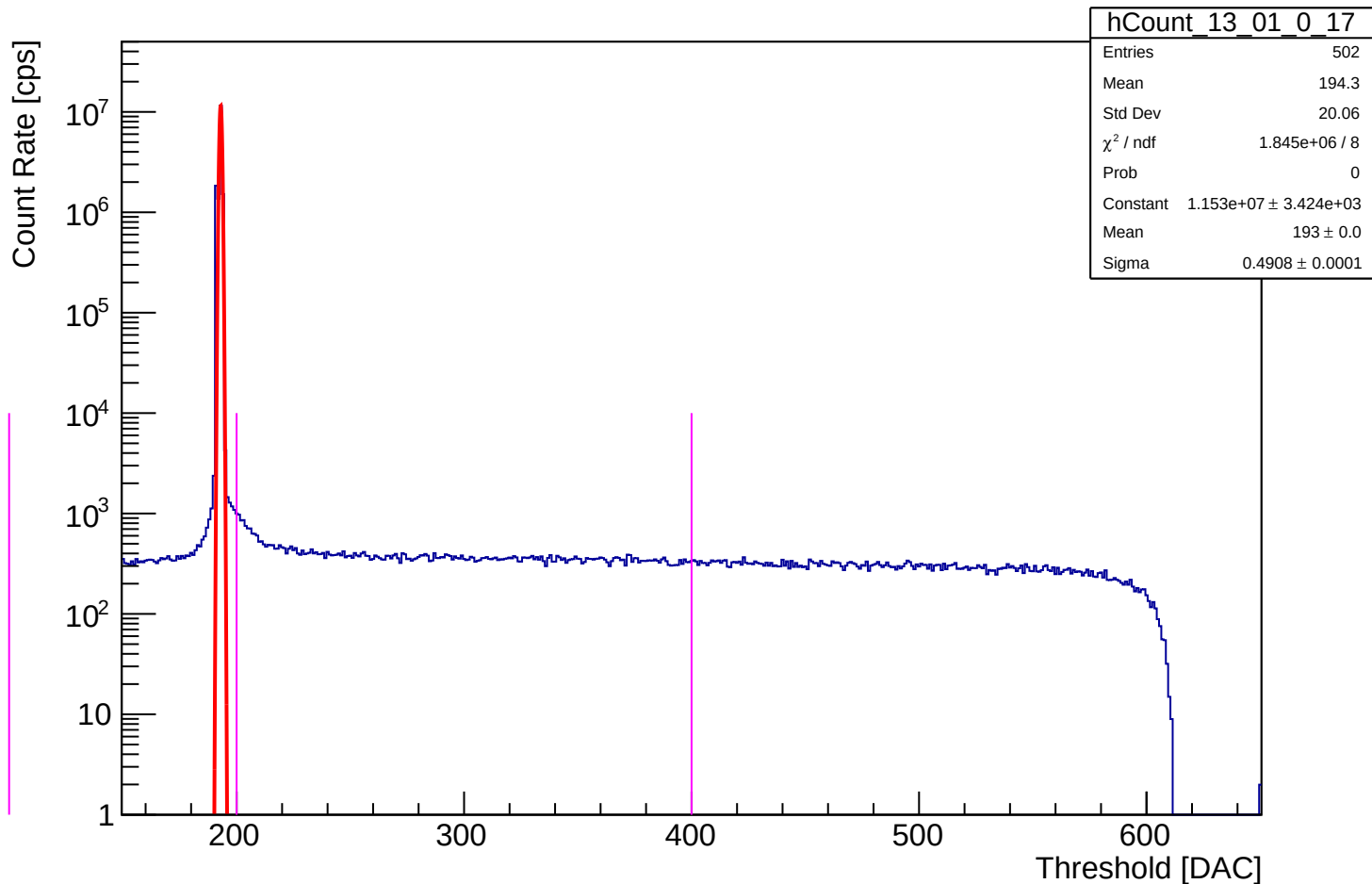
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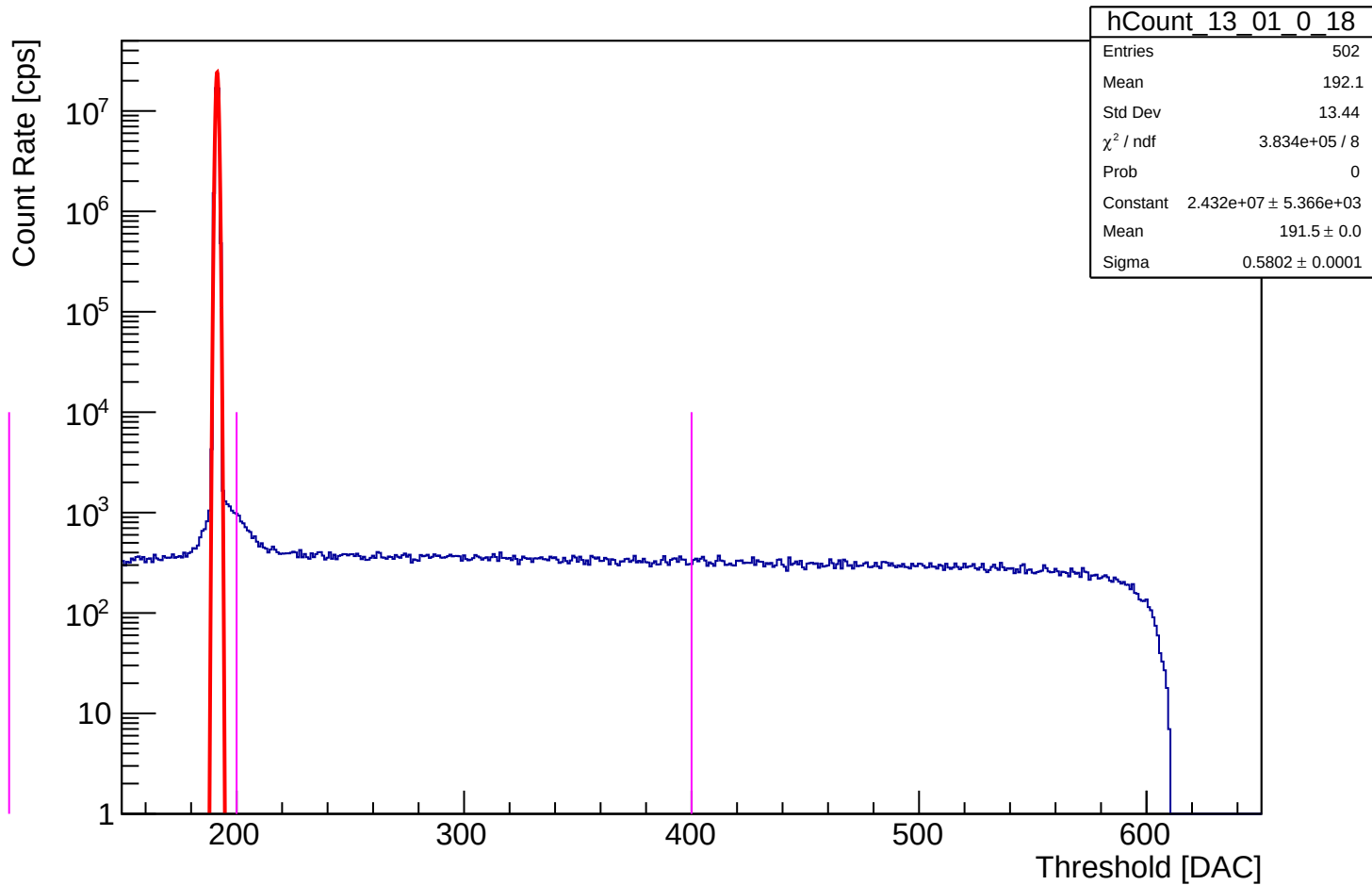
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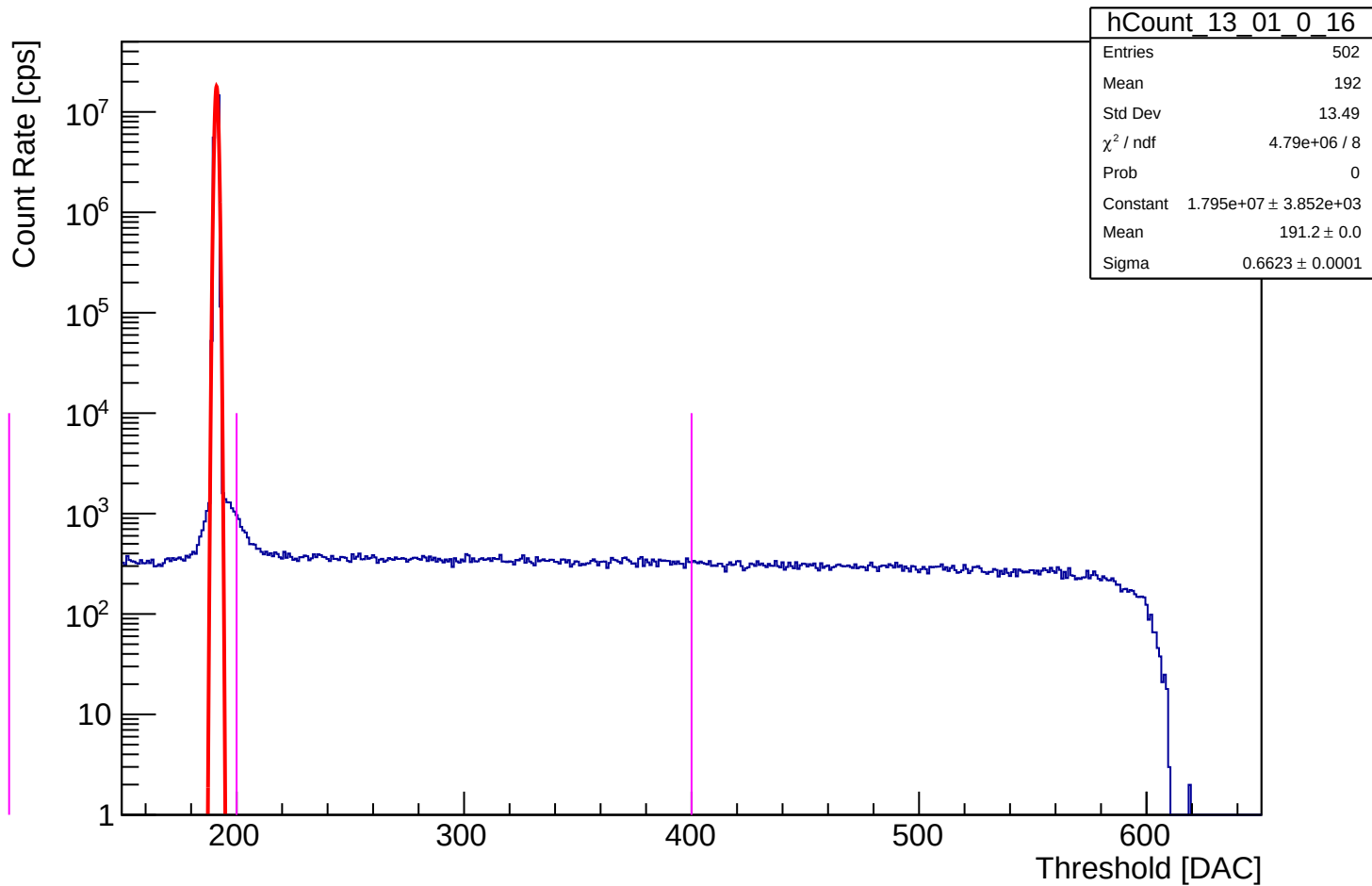
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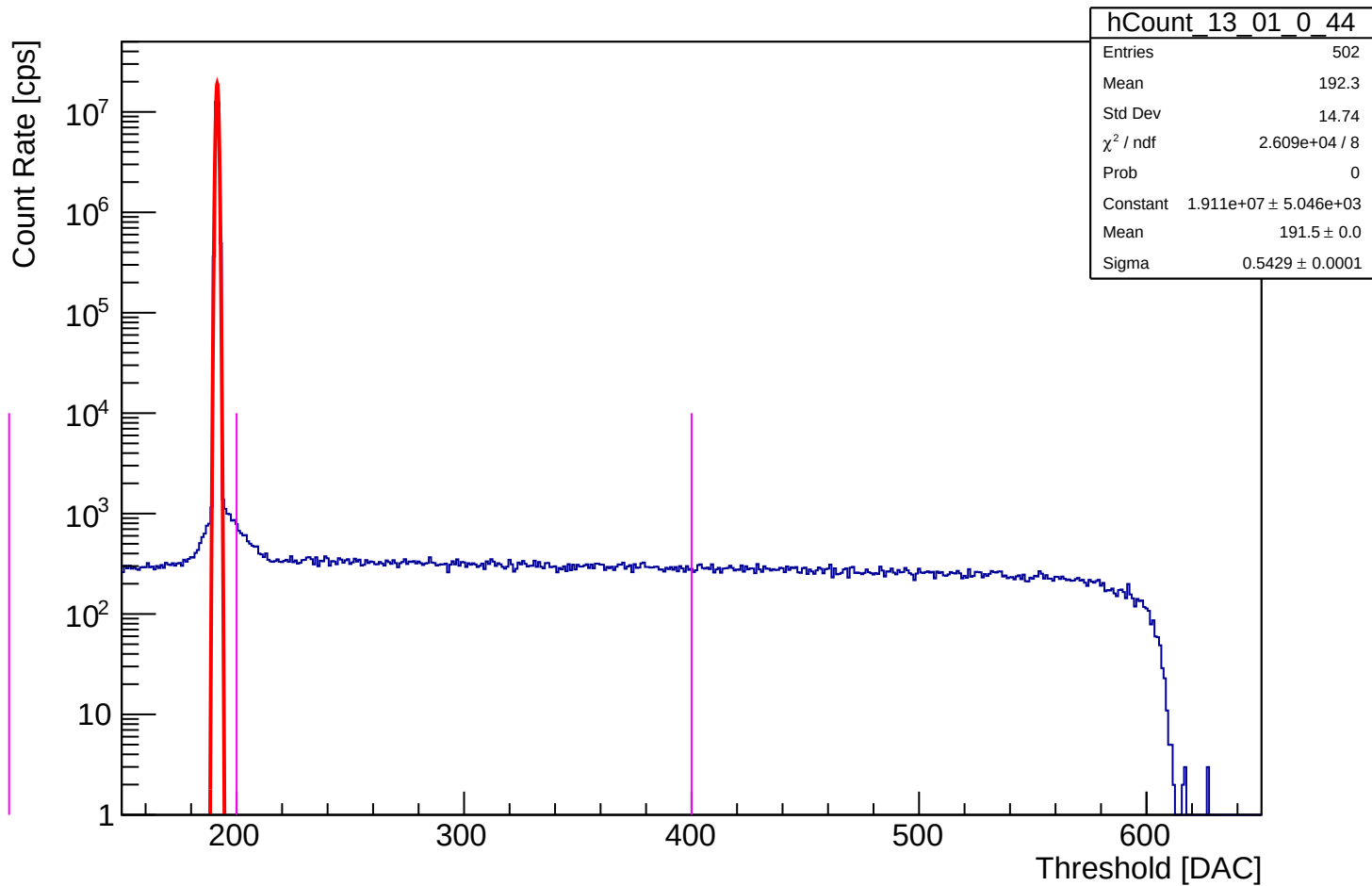
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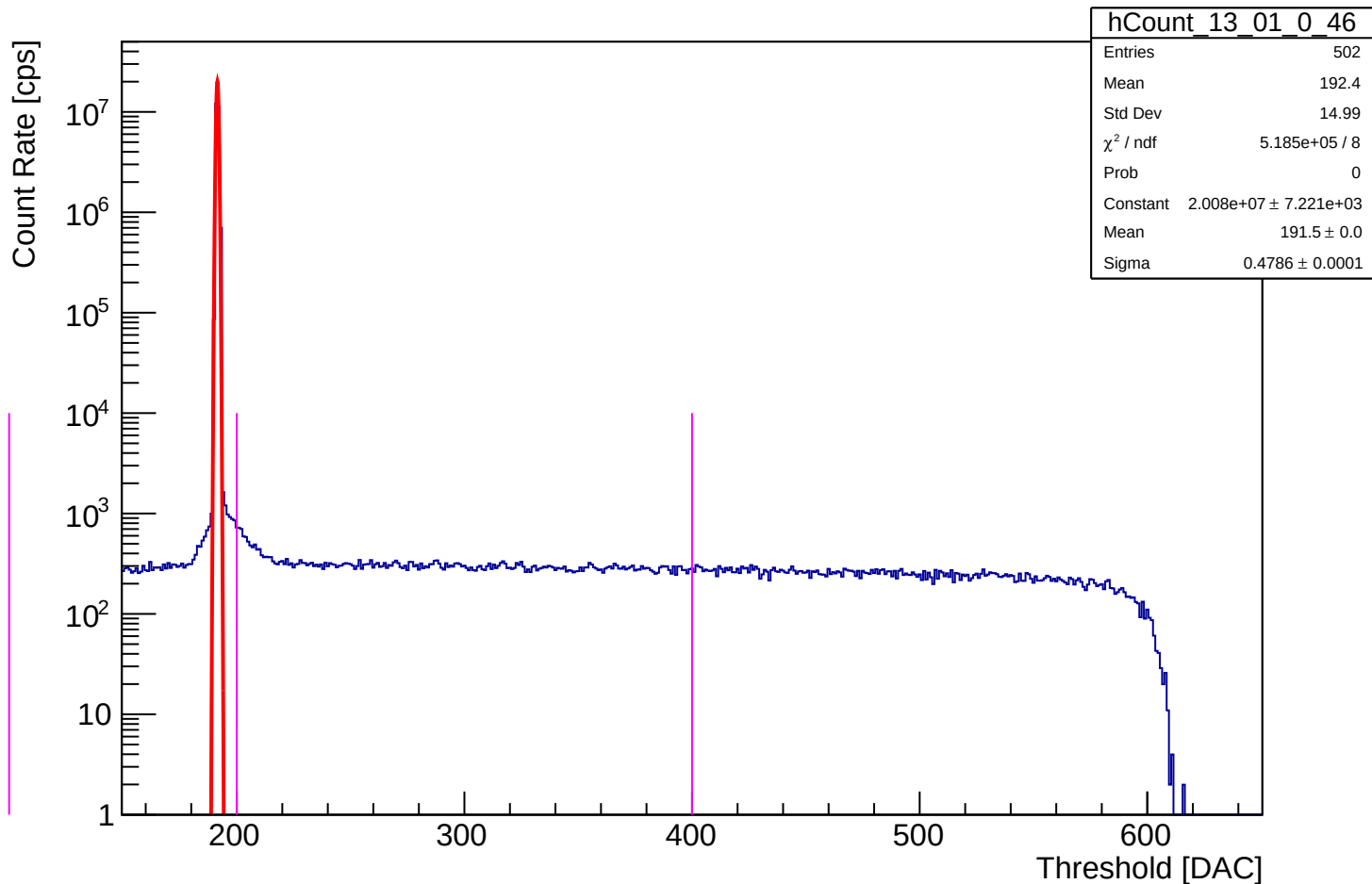
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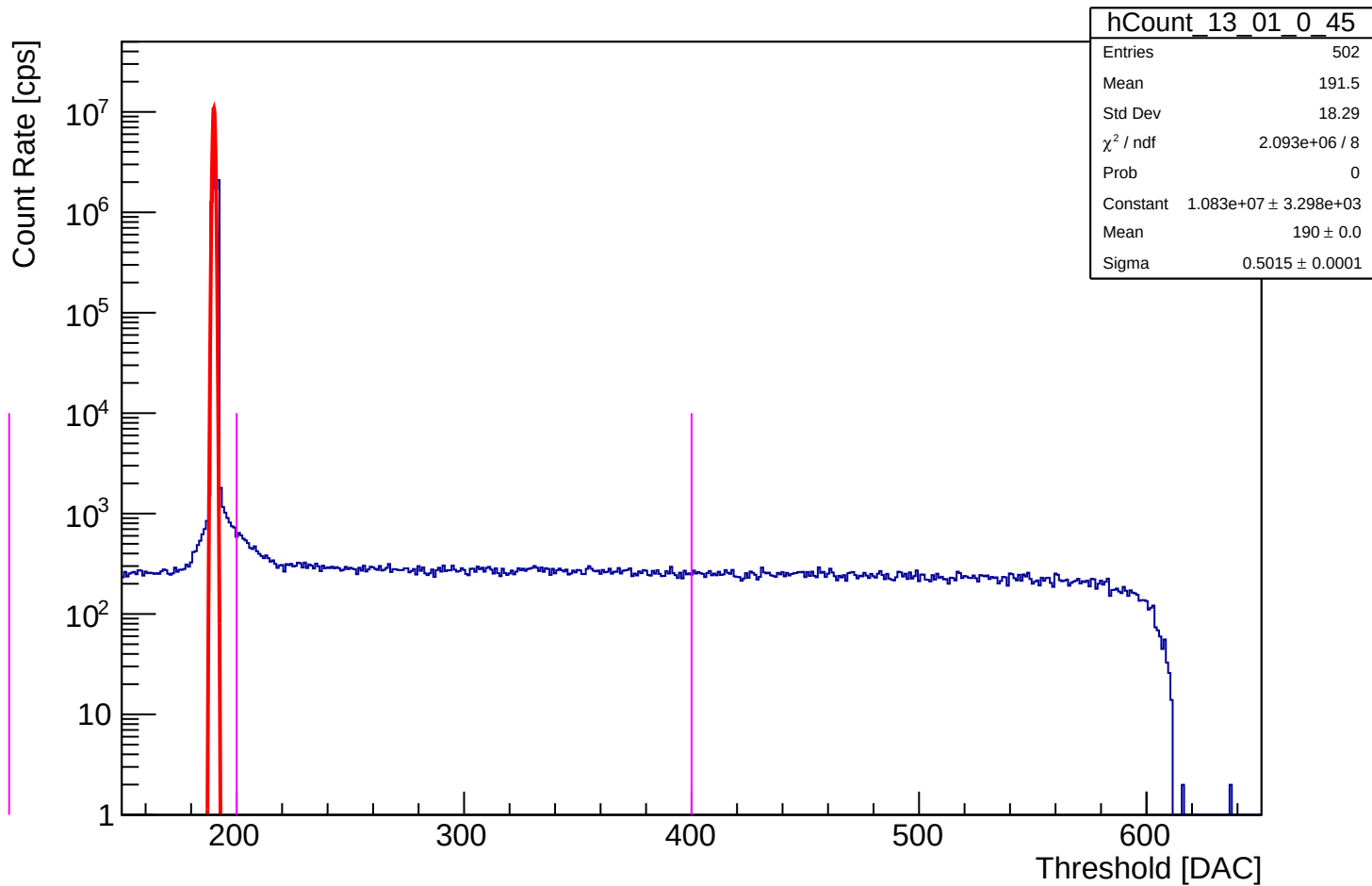
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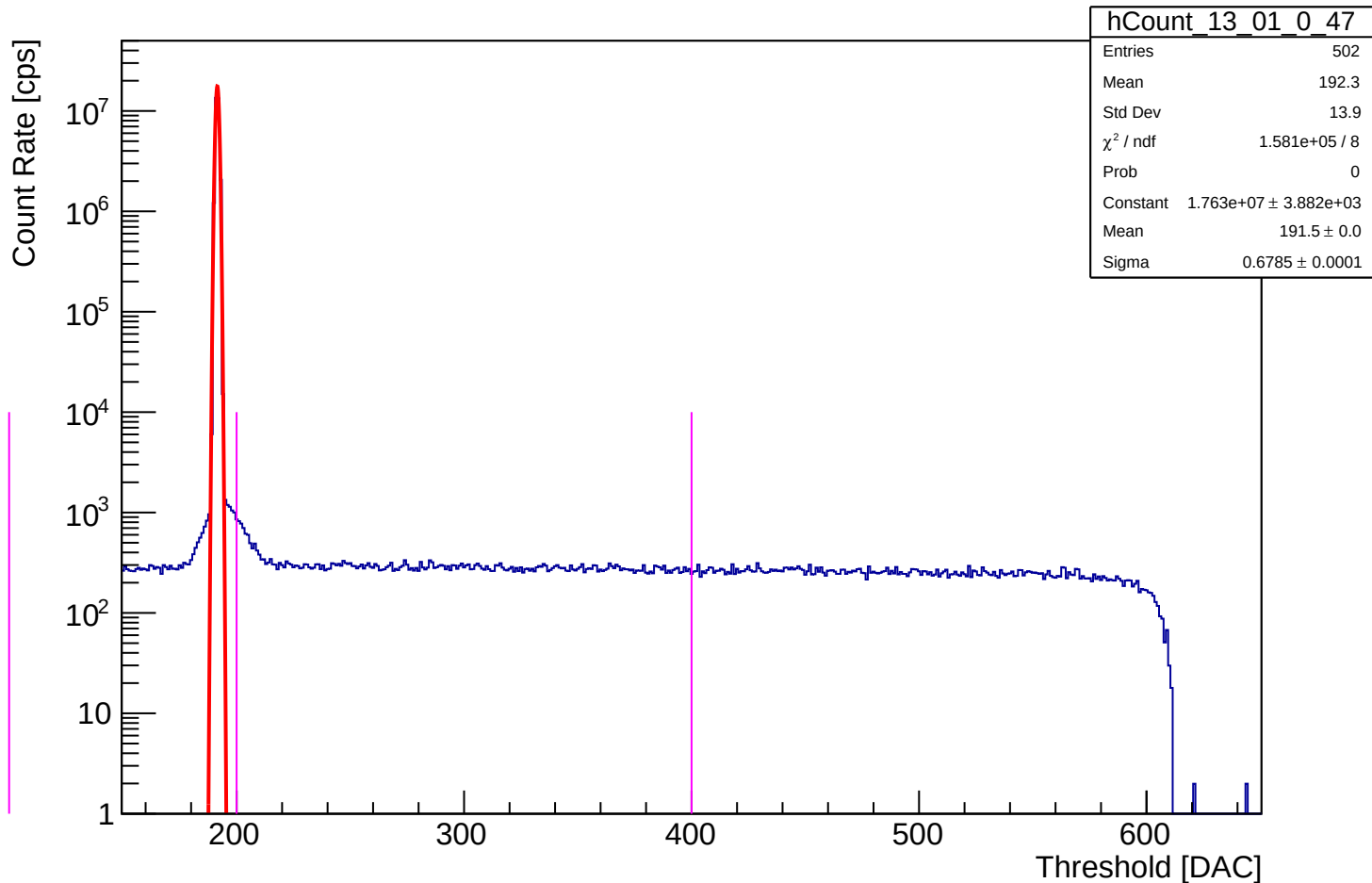
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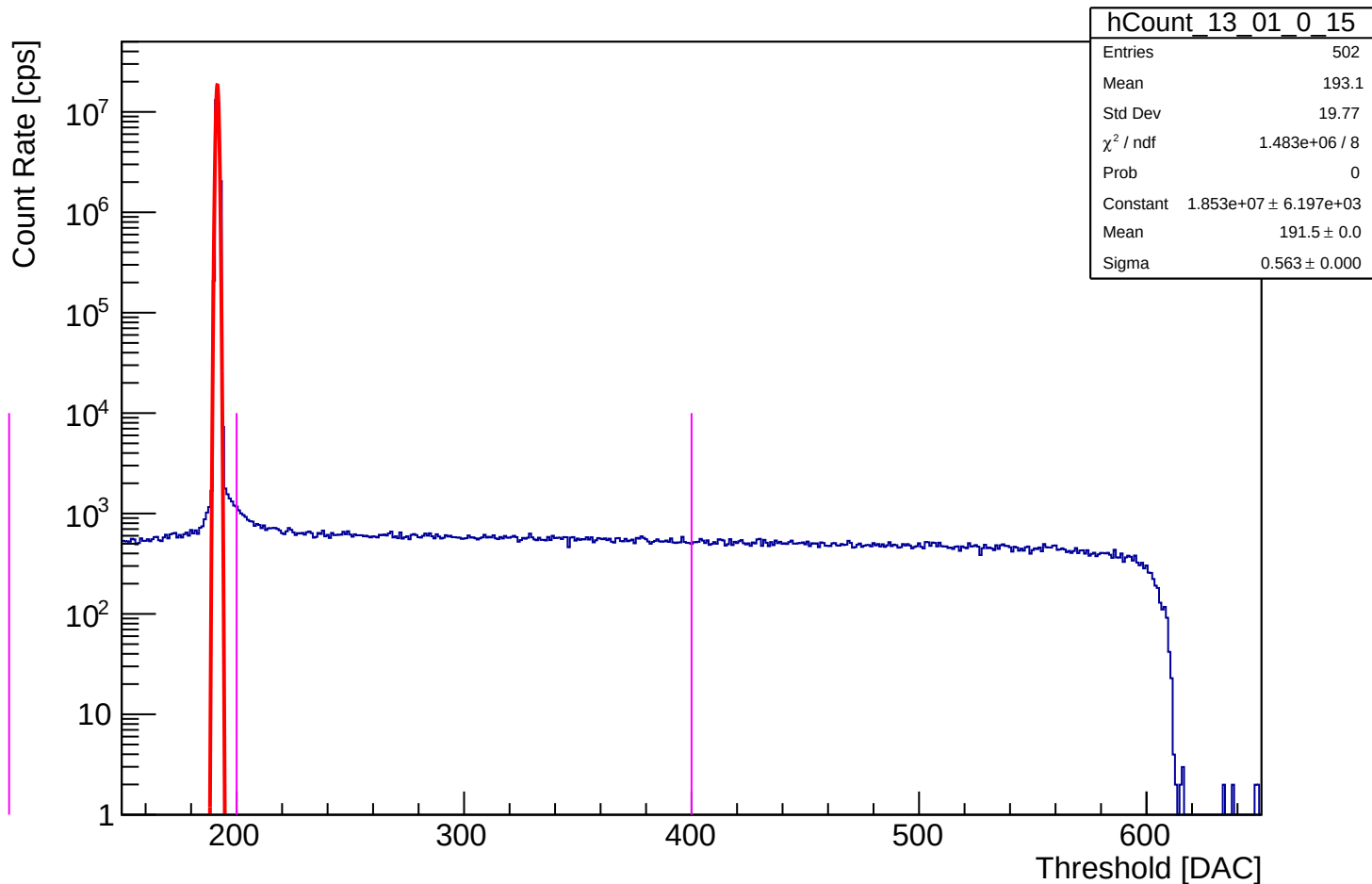
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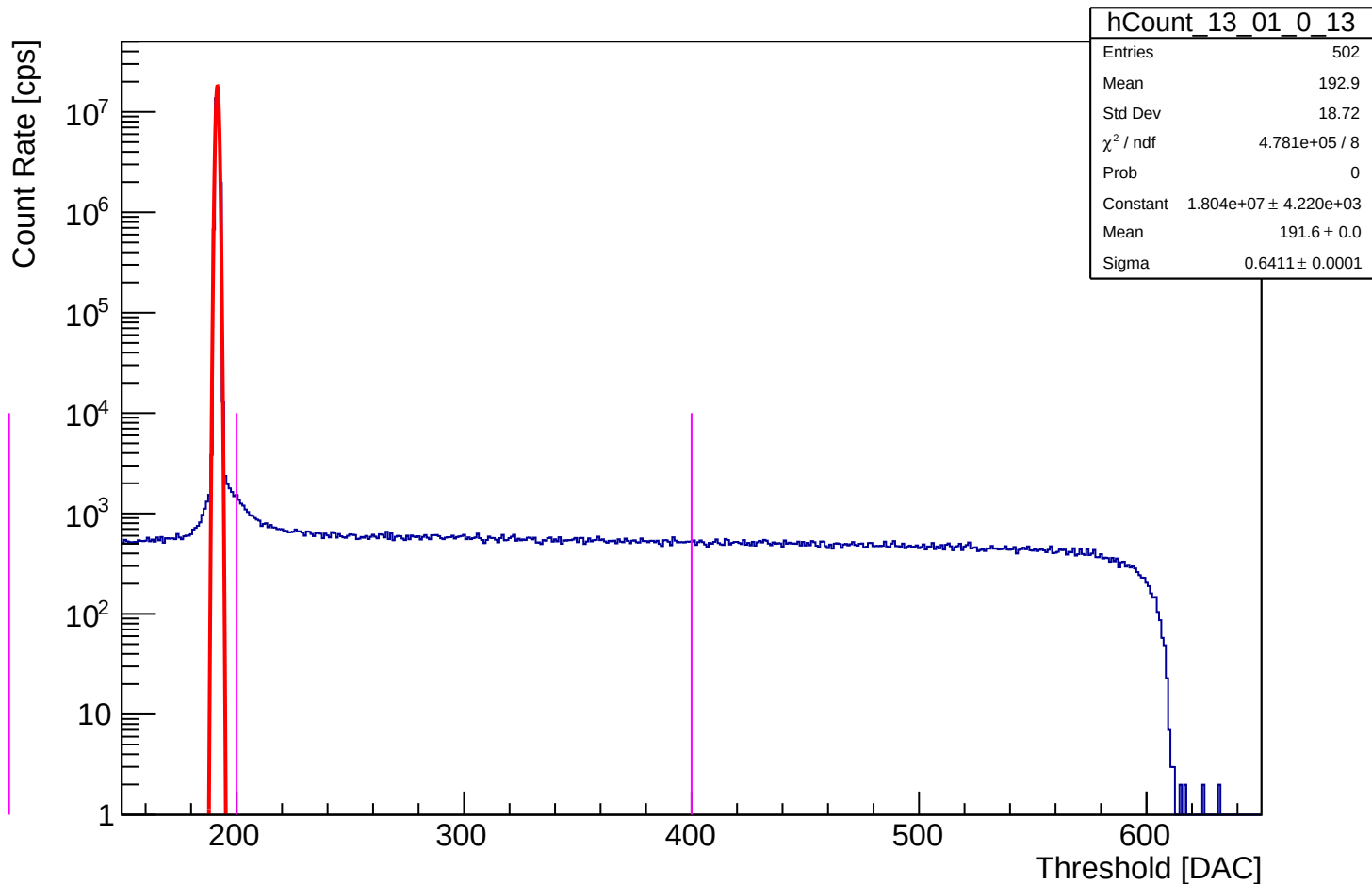
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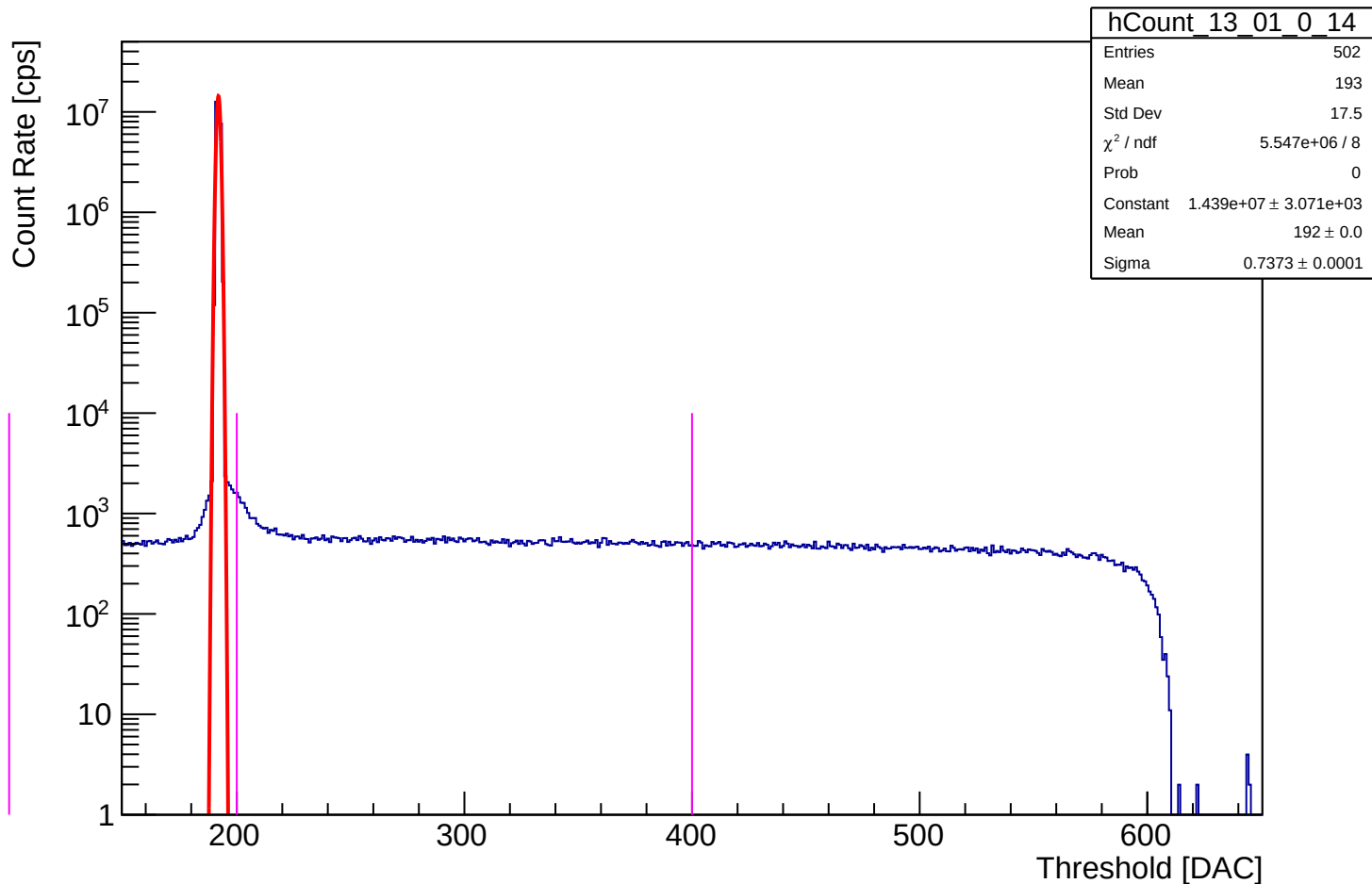
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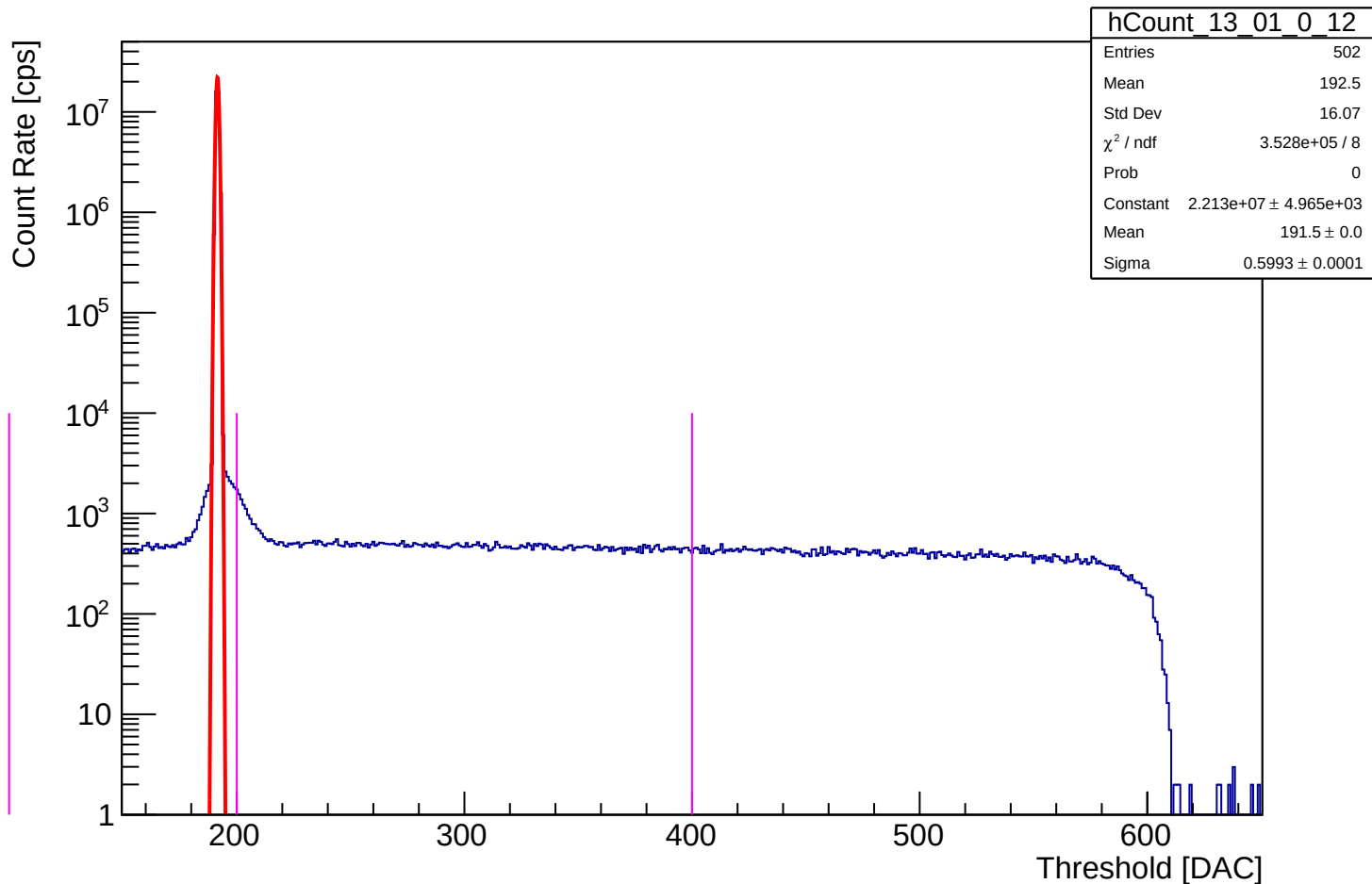
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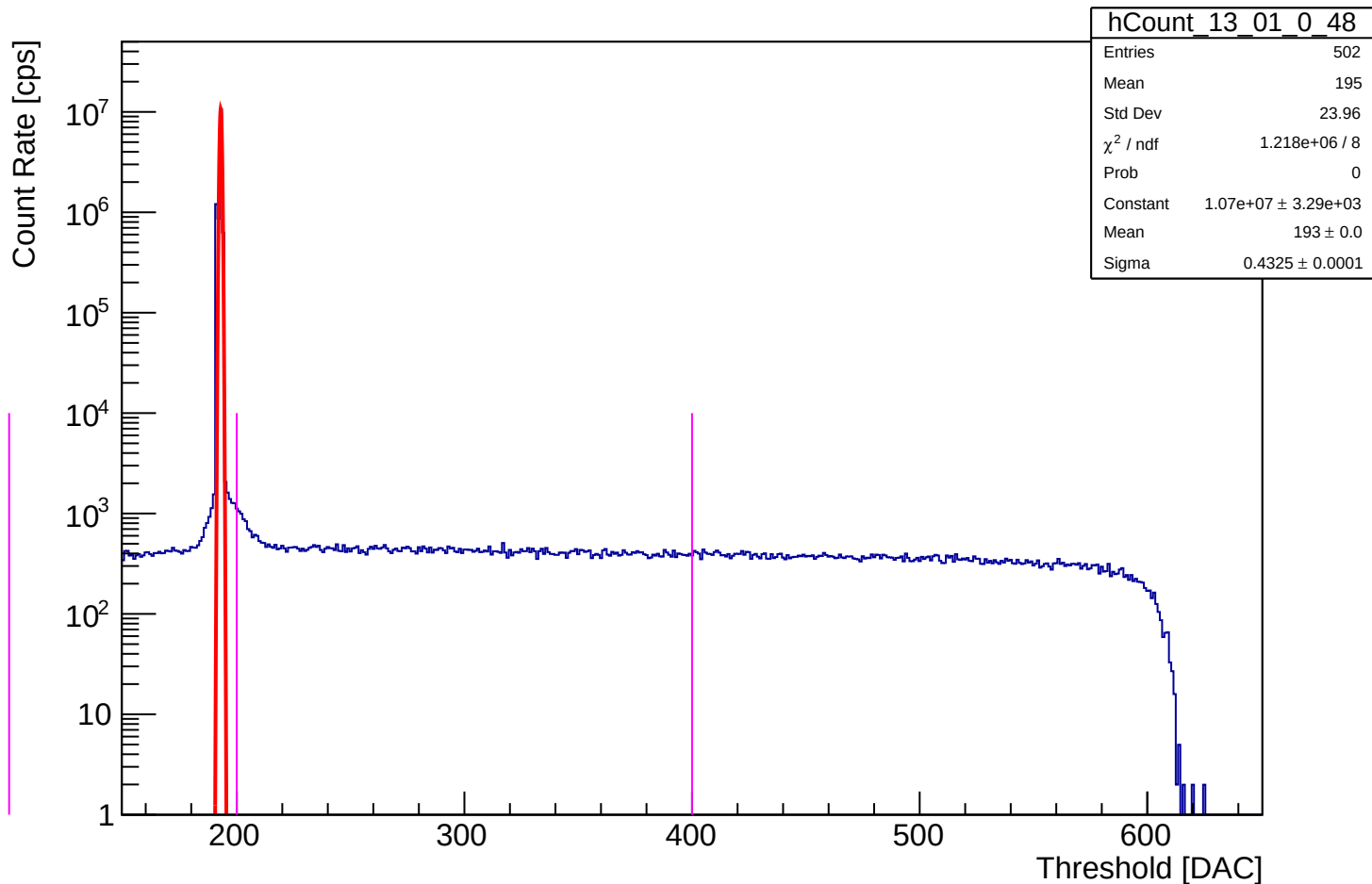
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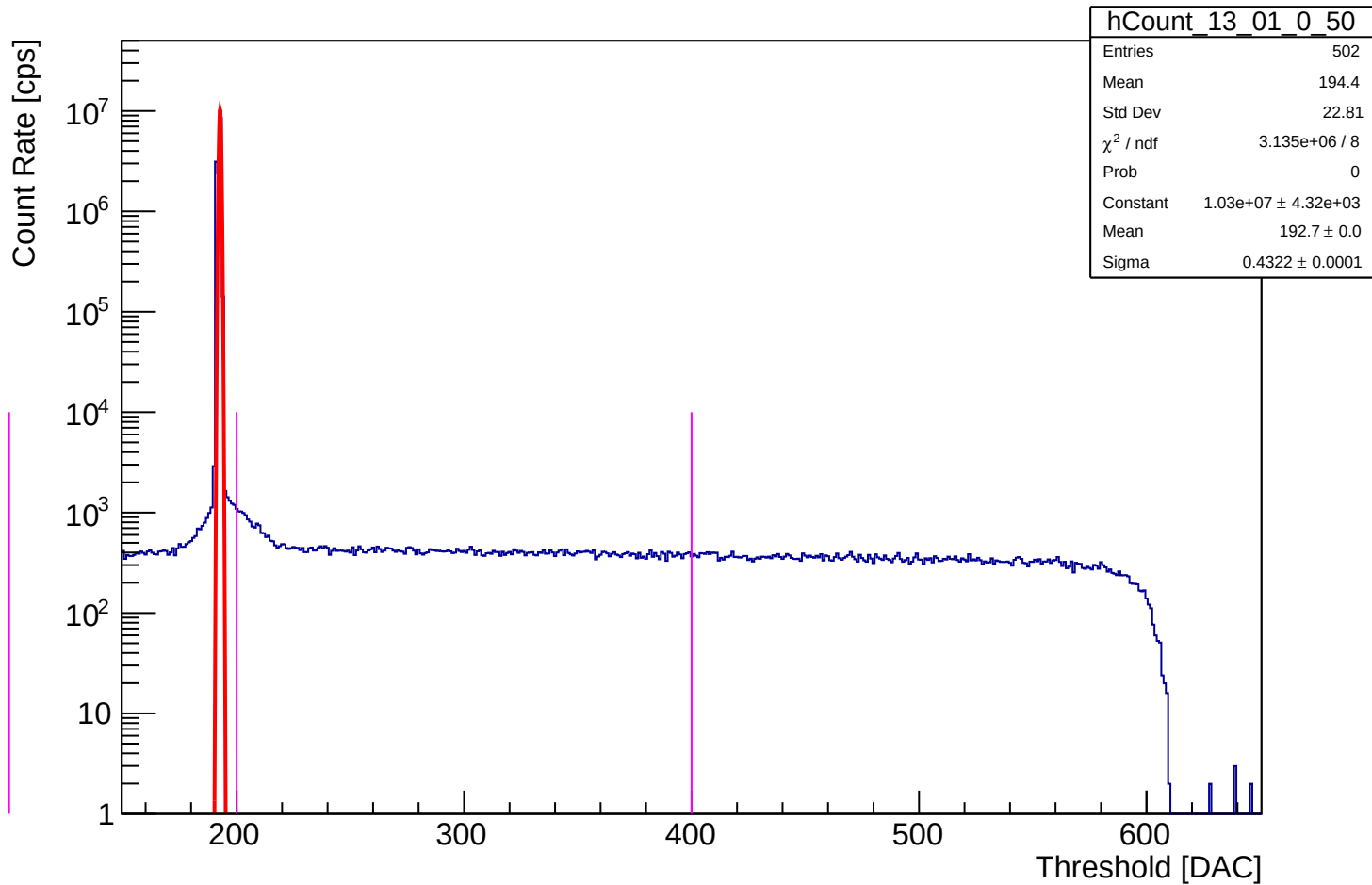
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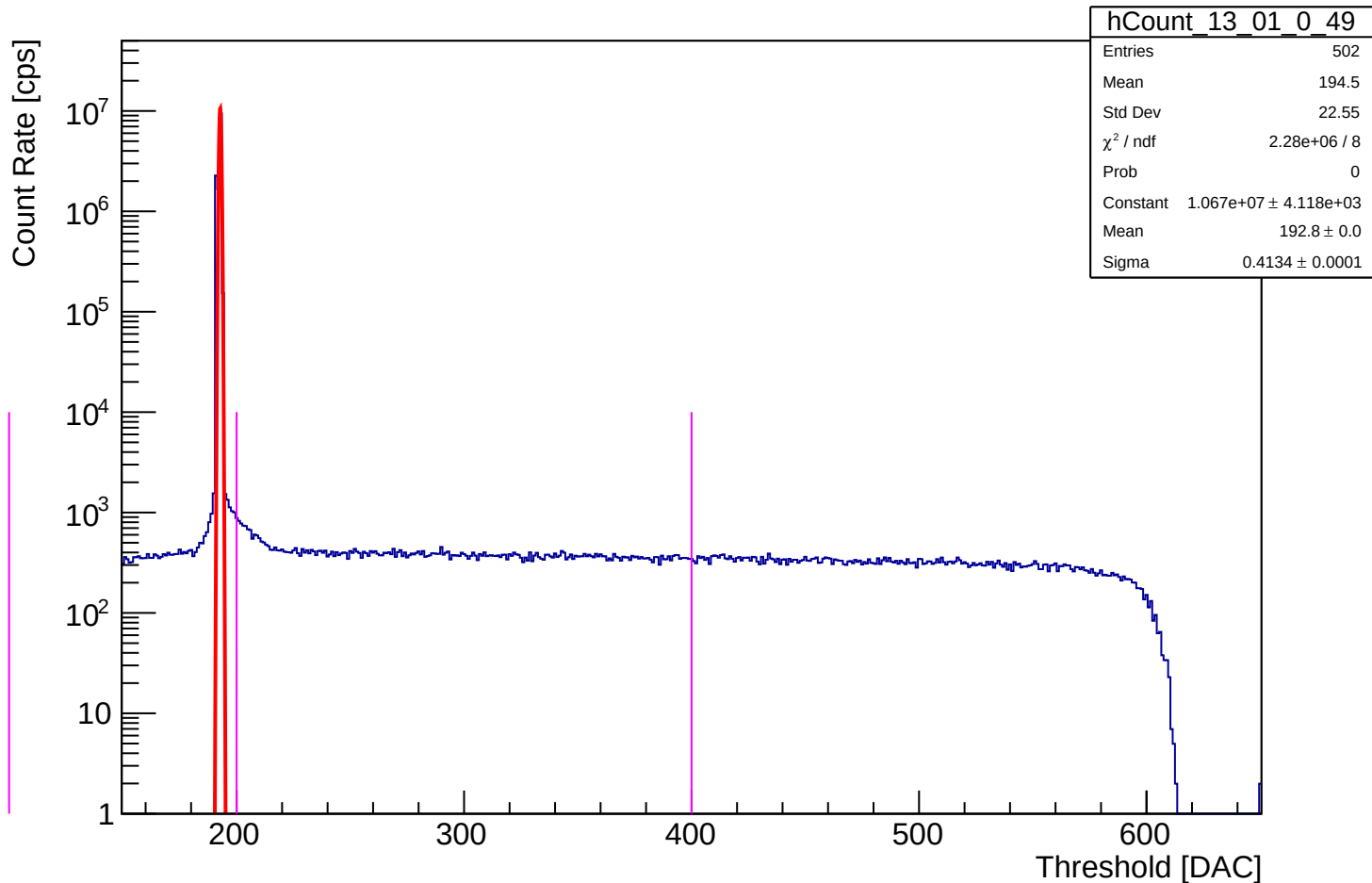
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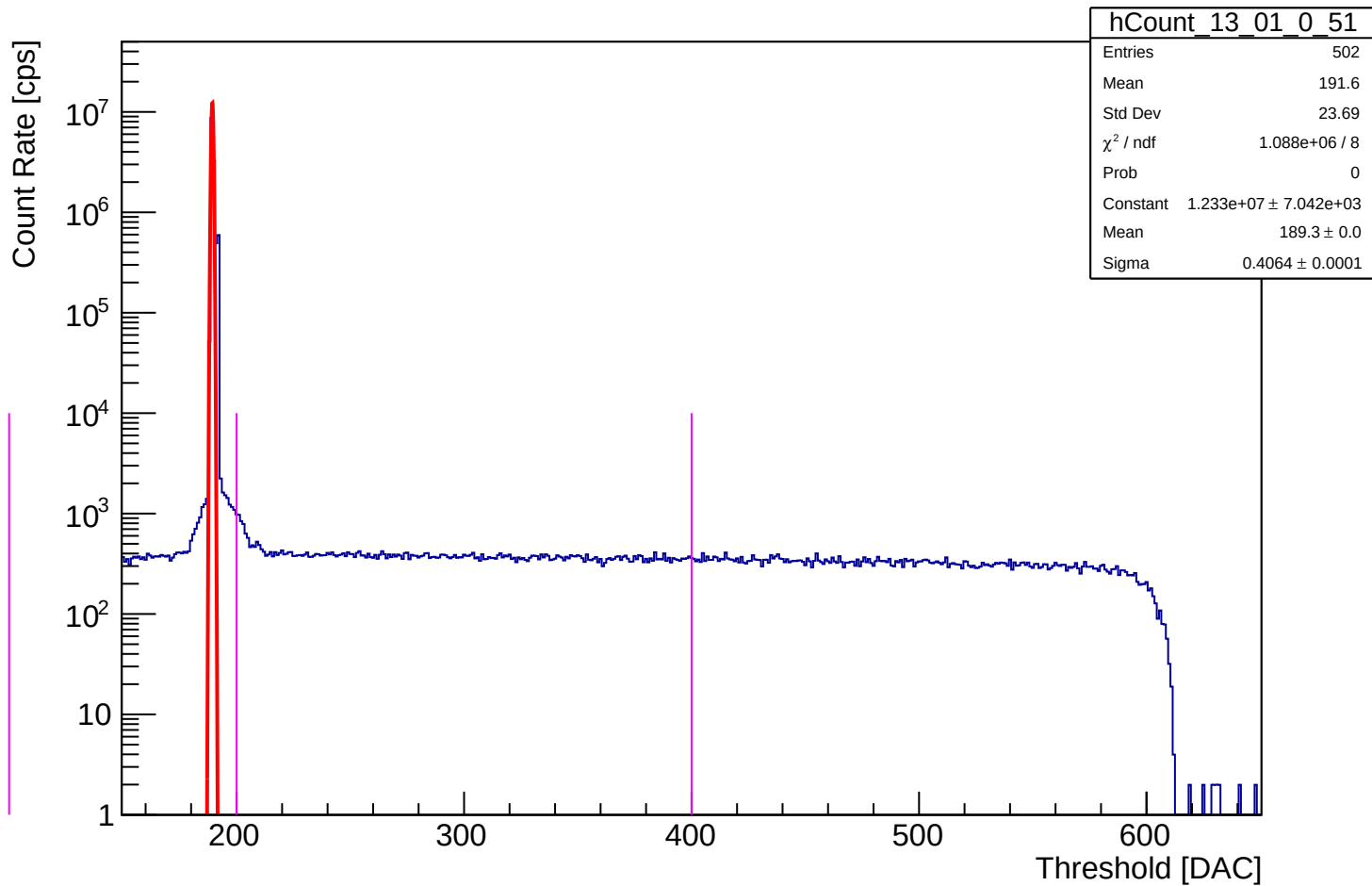
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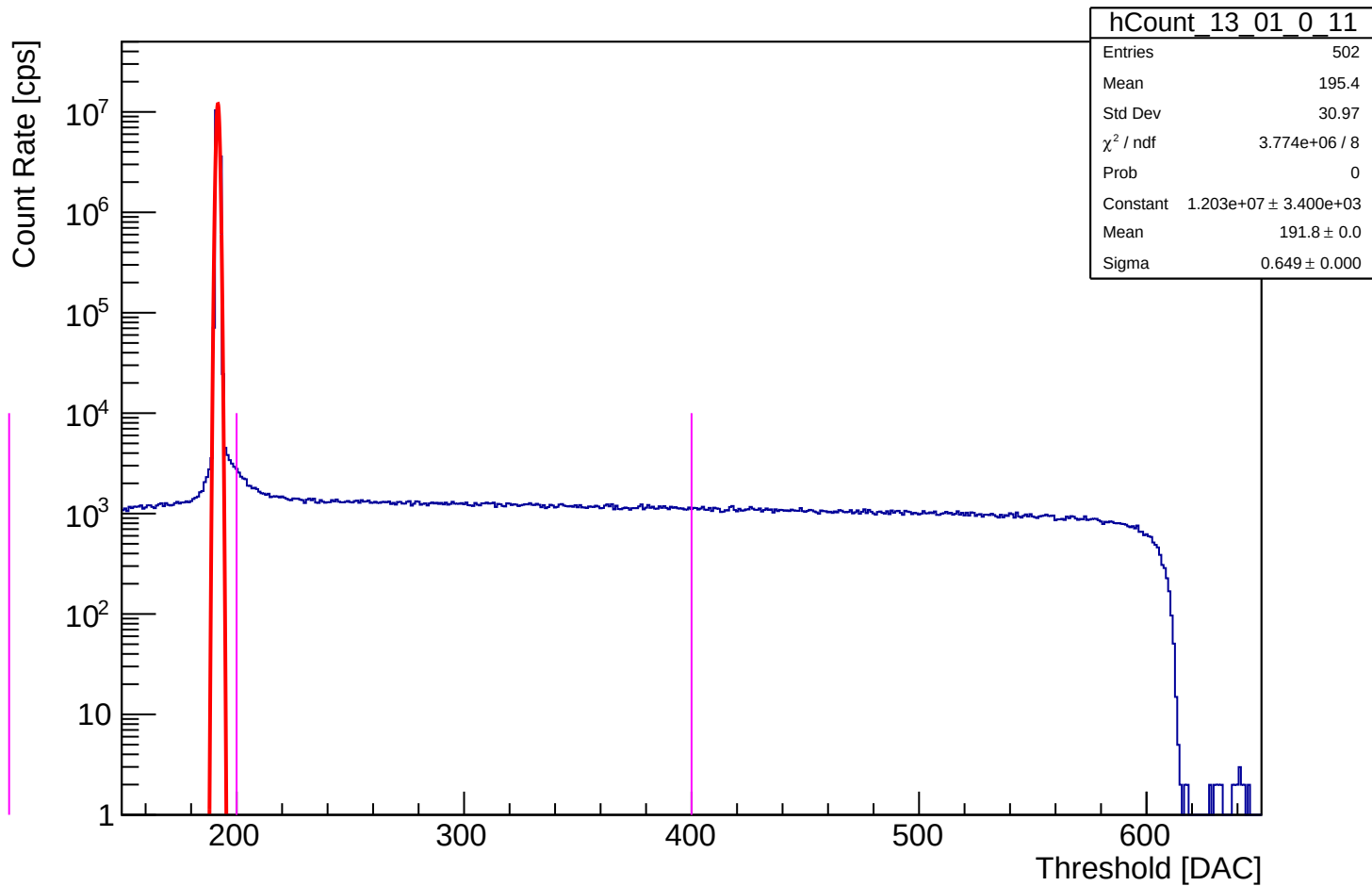
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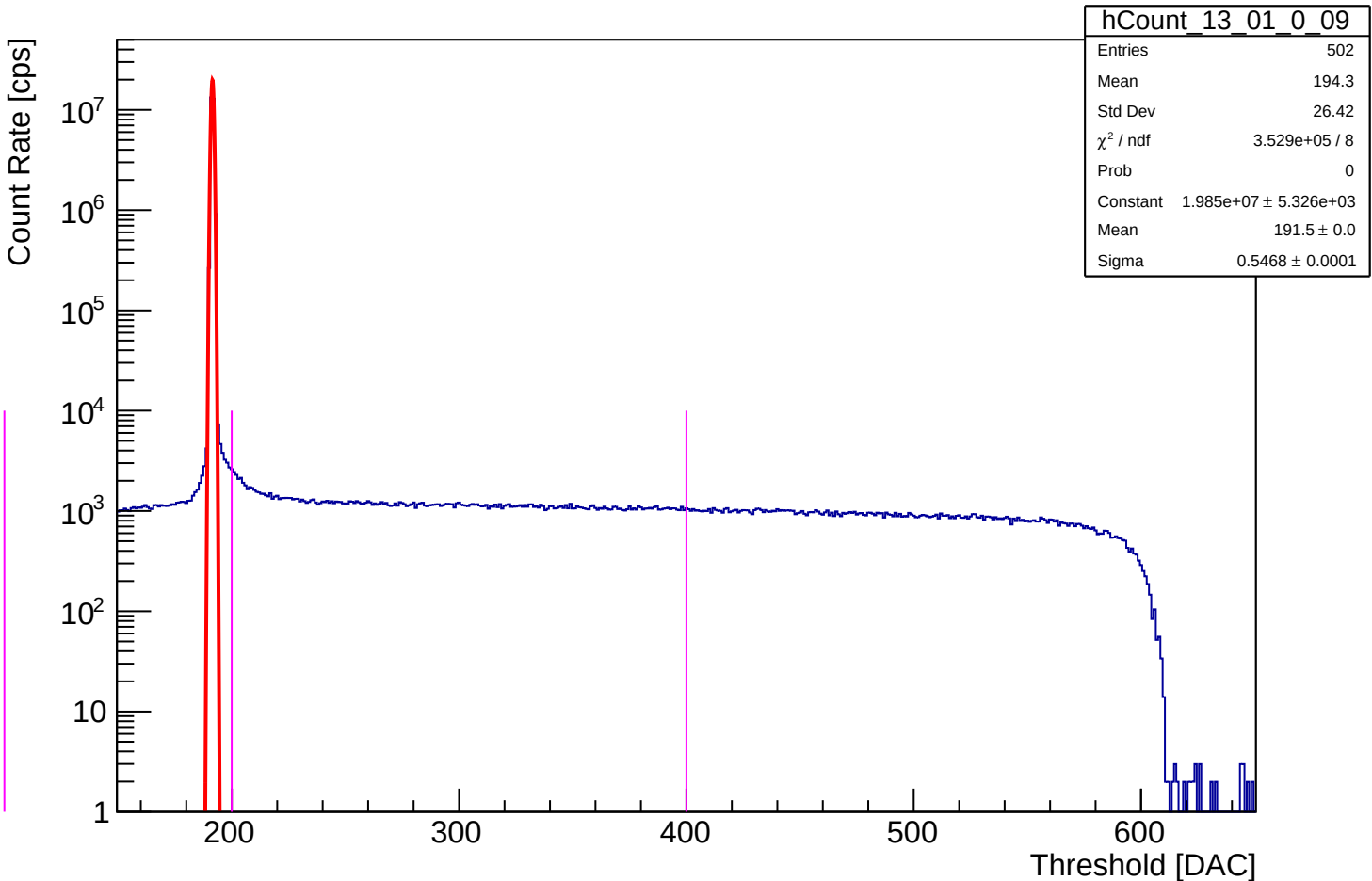


Row 1 Tile 1 Pmt 4 Pixel 40 Slot 13 Fiber 1 Asic 0 Channel 51

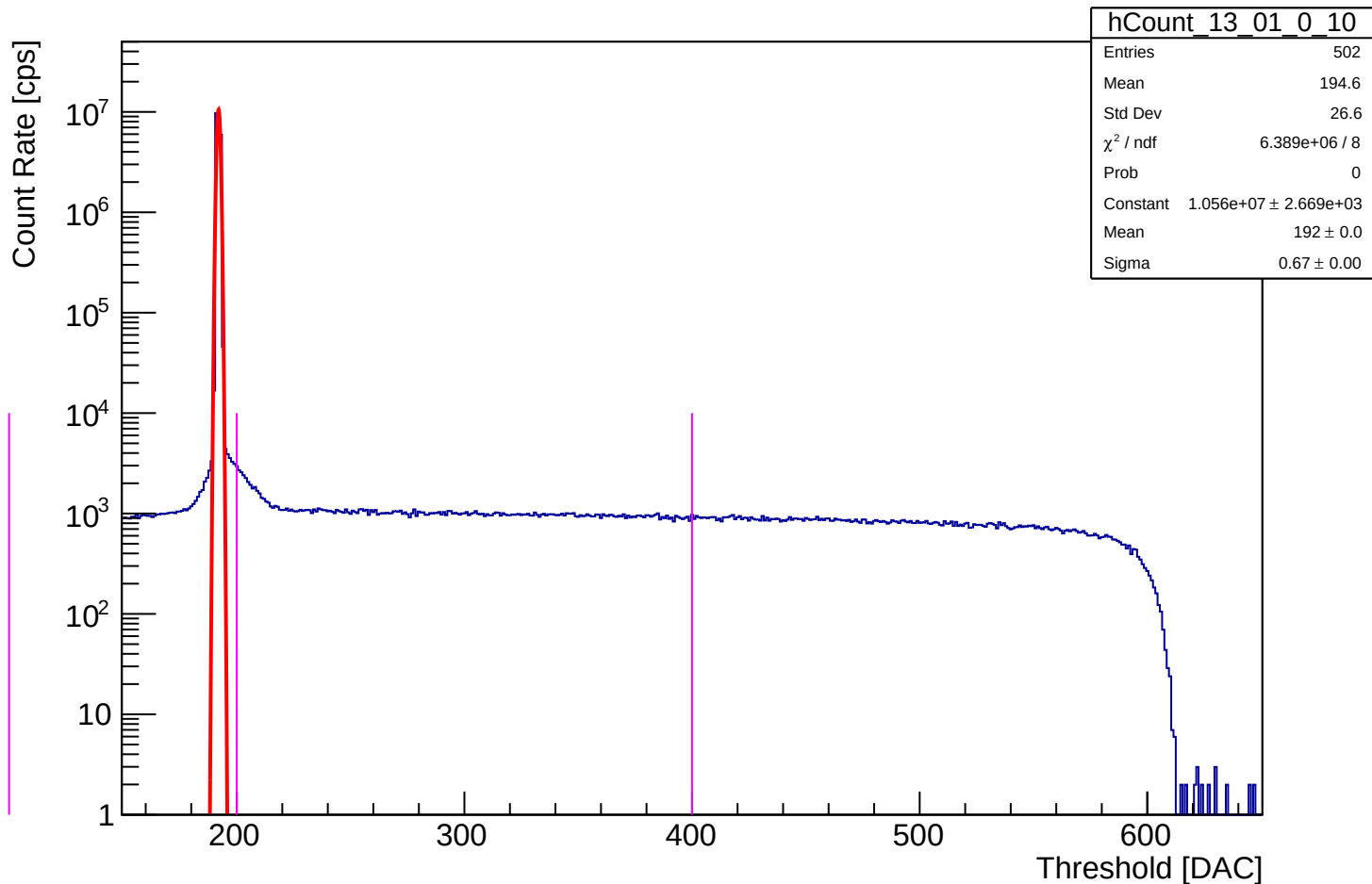


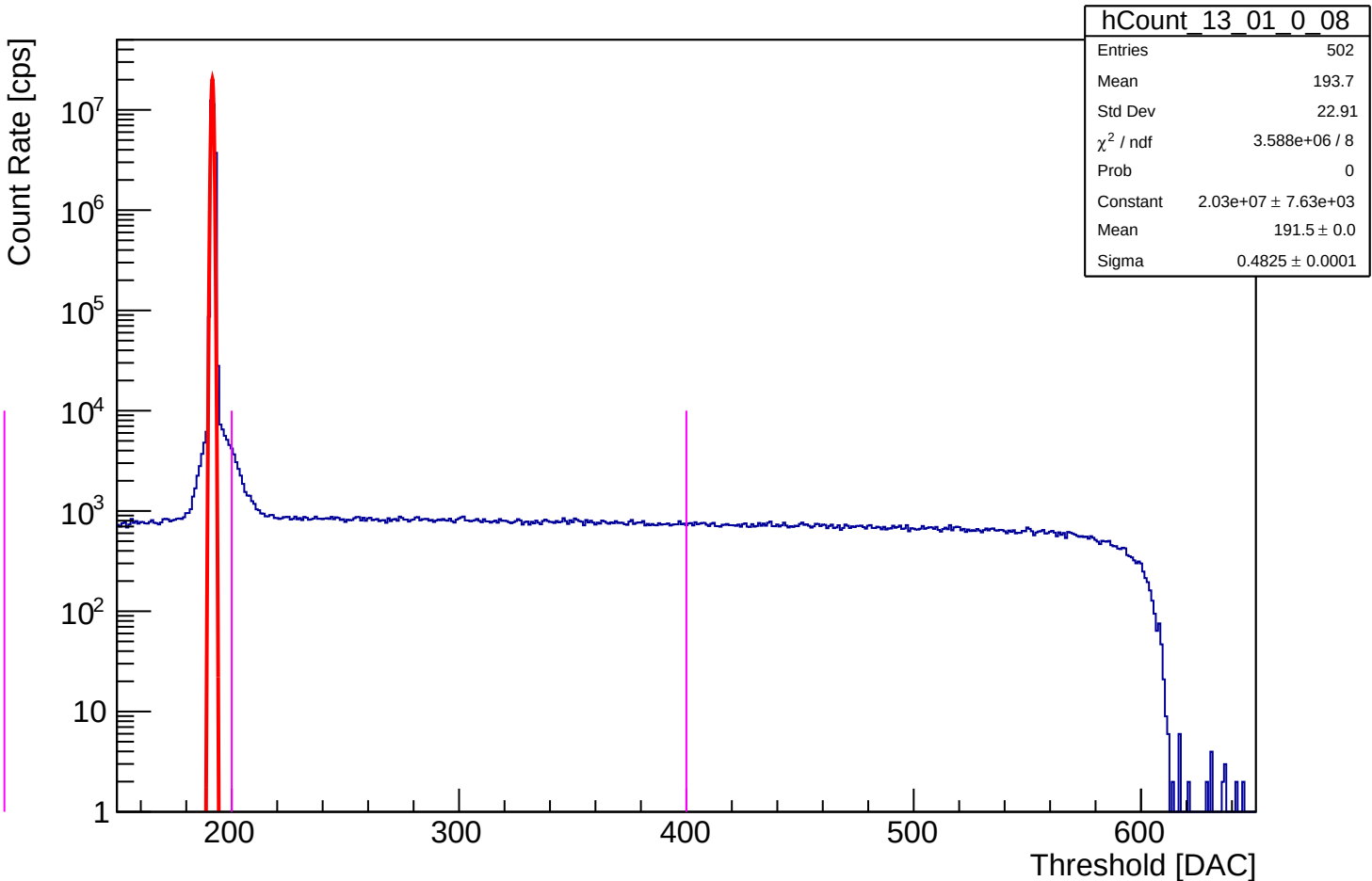
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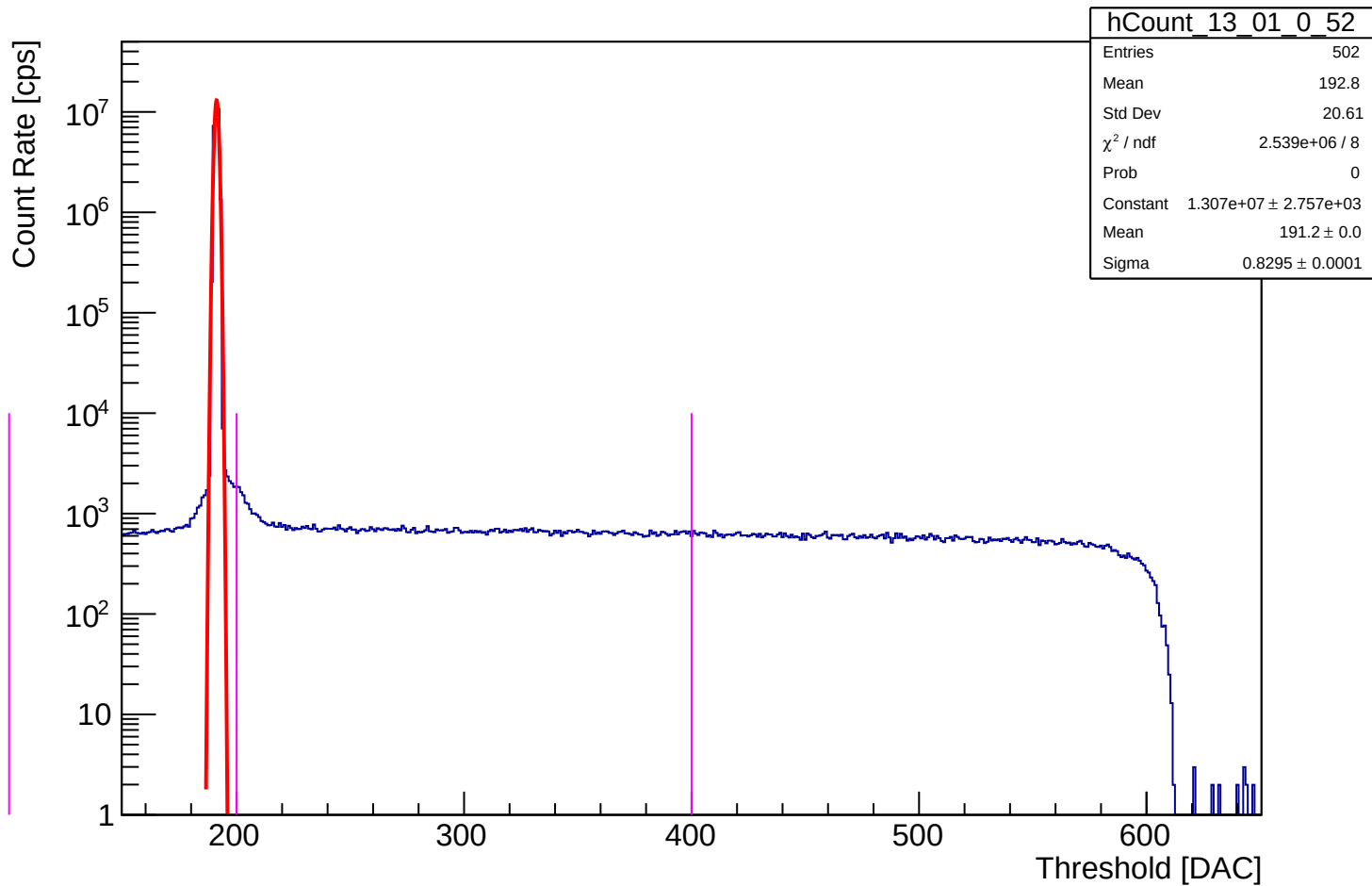


Row 1 Tile 1 Pmt 4 Pixel 43 Slot 13 Fiber 1 Asic 0 Channel 10

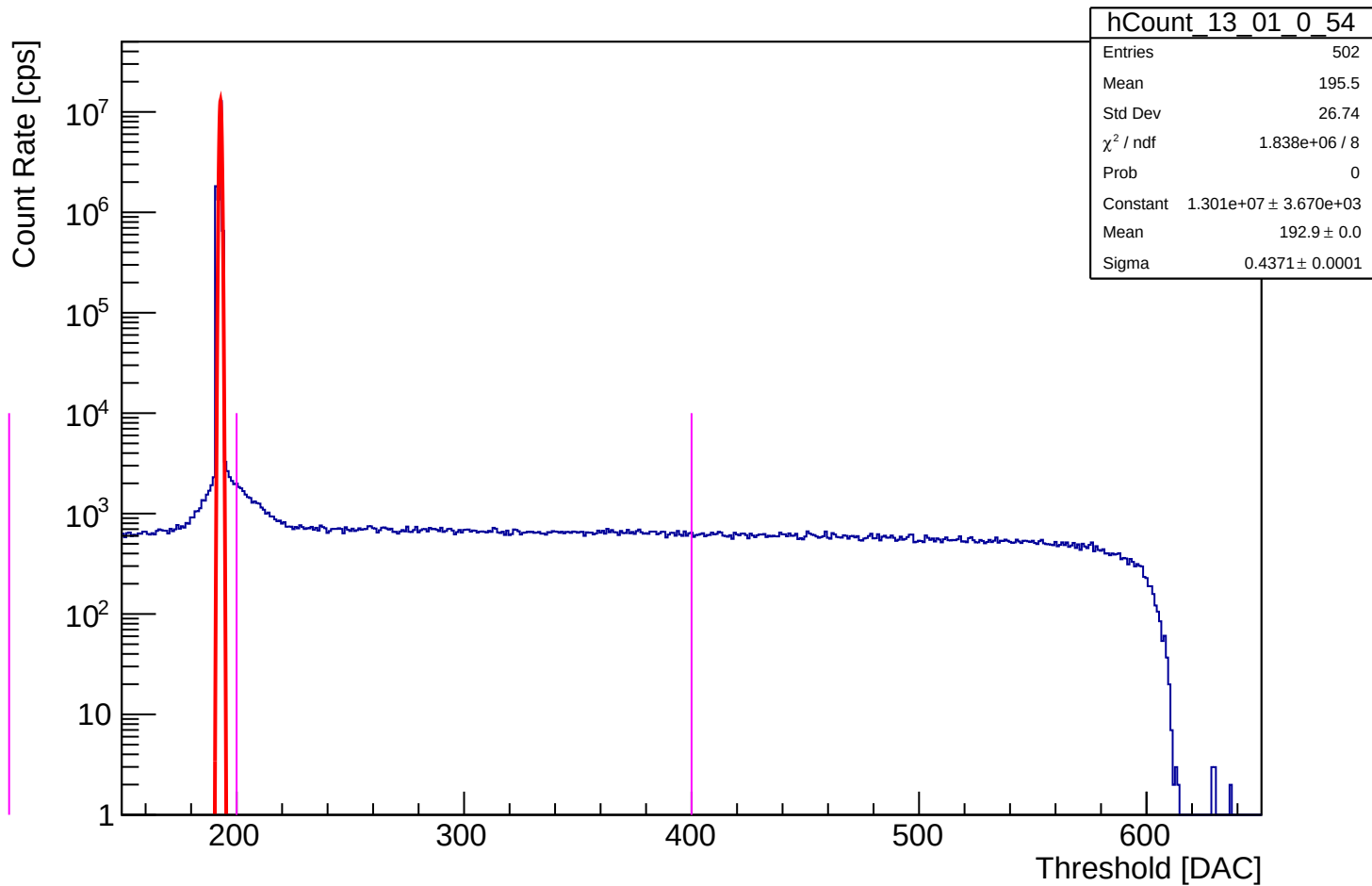




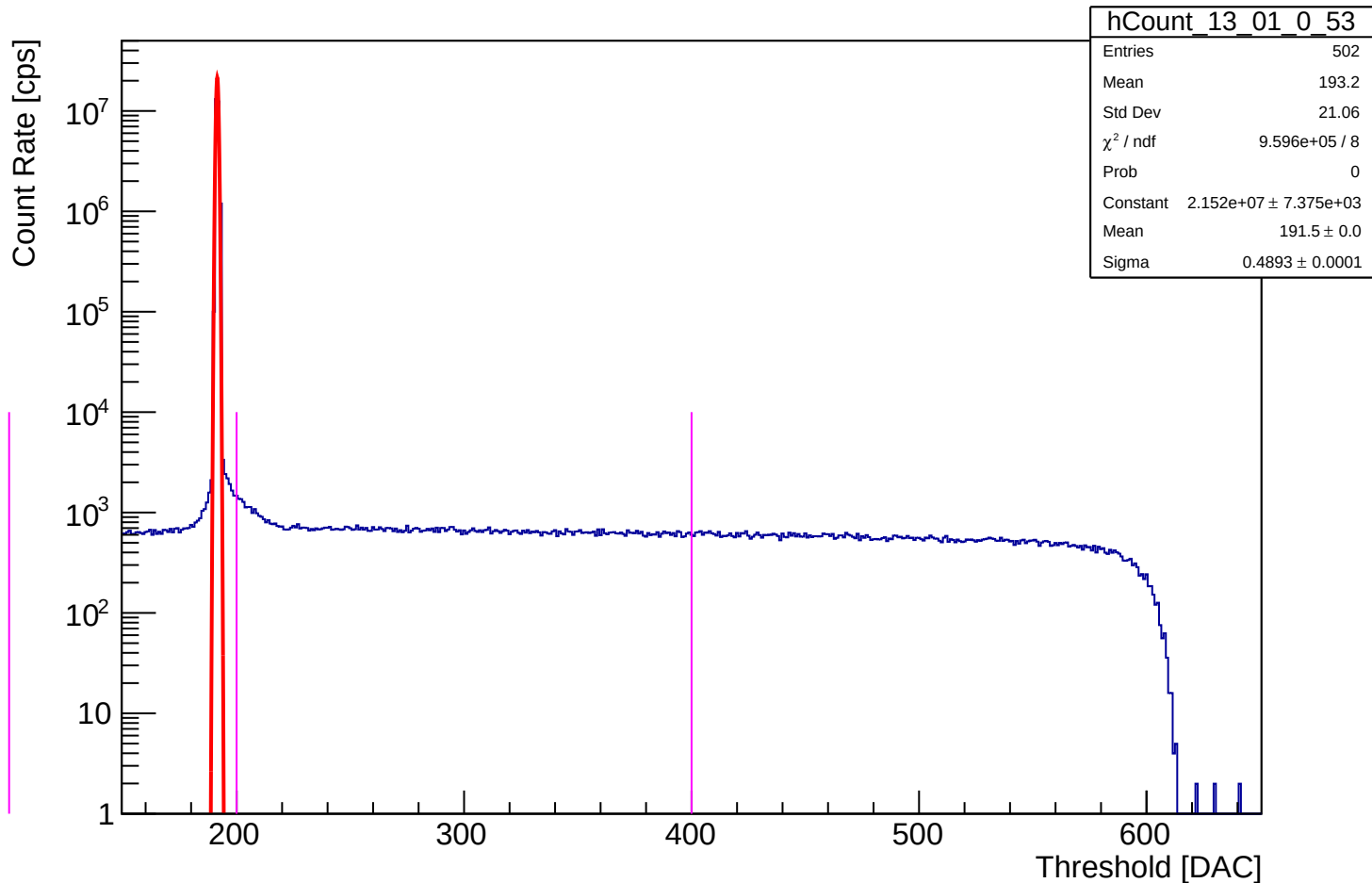
Row 1 Tile 1 Pmt 4 Pixel 45 Slot 13 Fiber 1 Asic 0 Channel 52



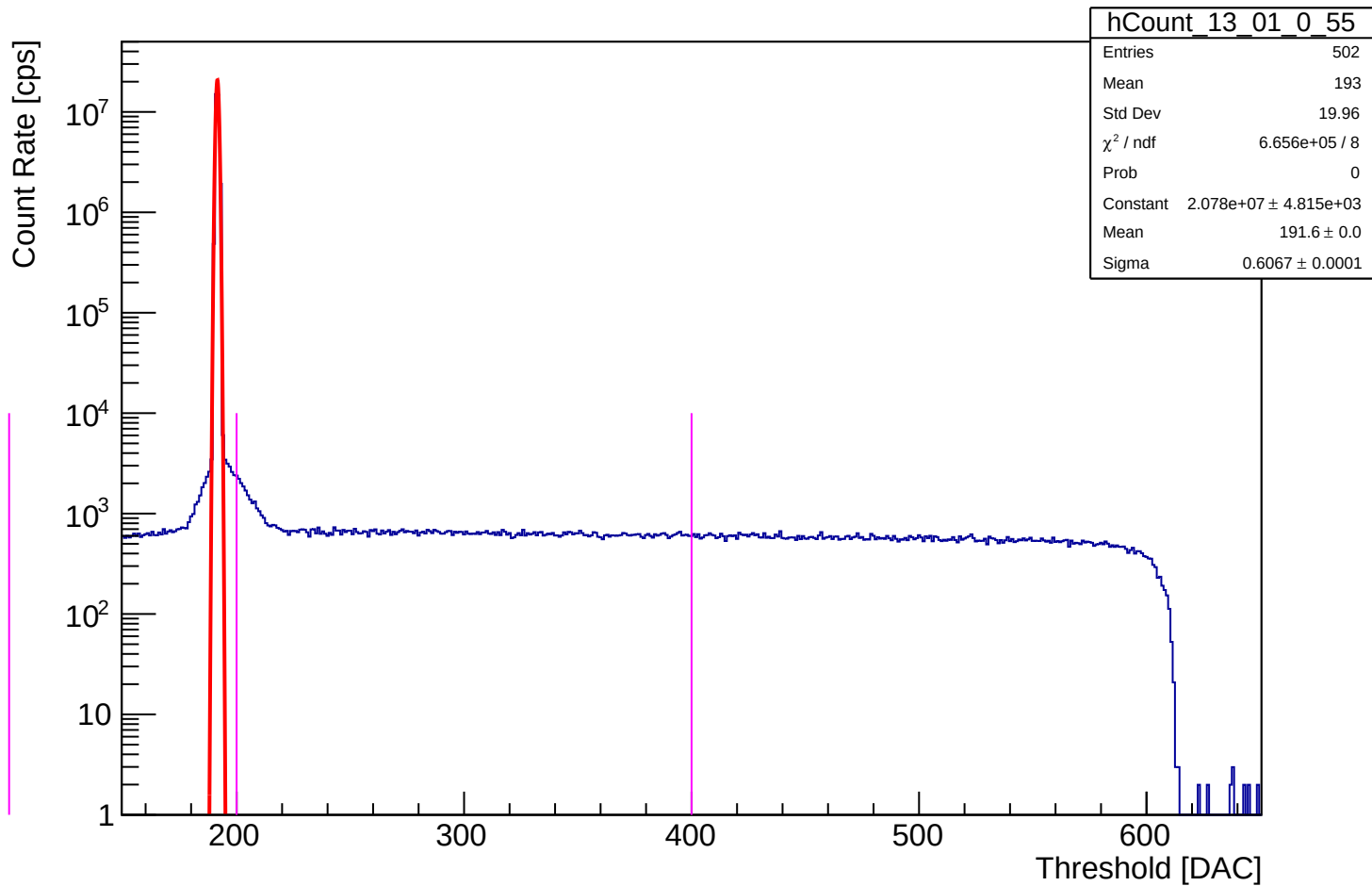
Row 1 Tile 1 Pmt 4 Pixel 46 Slot 13 Fiber 1 Asic 0 Channel 54

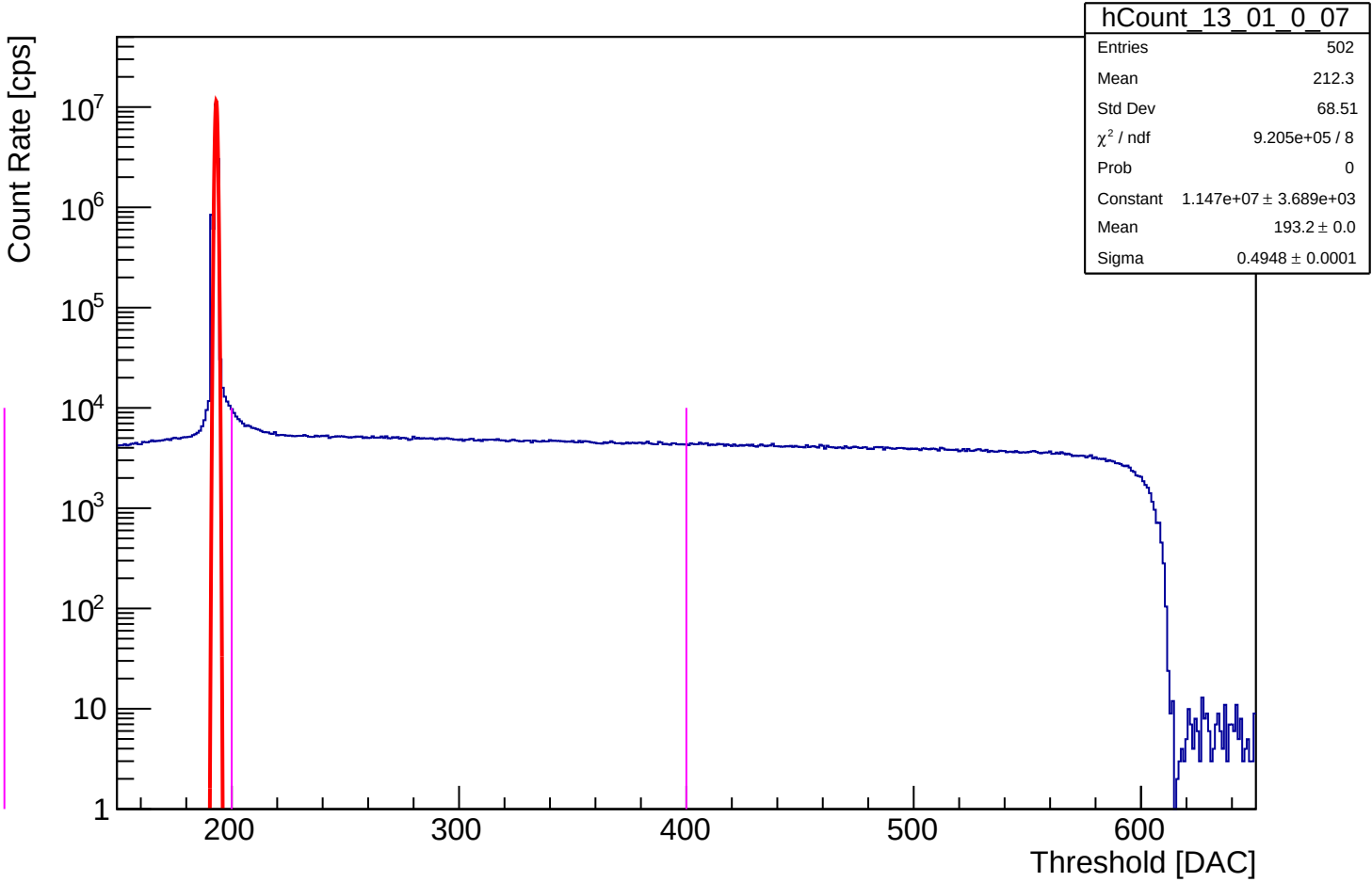


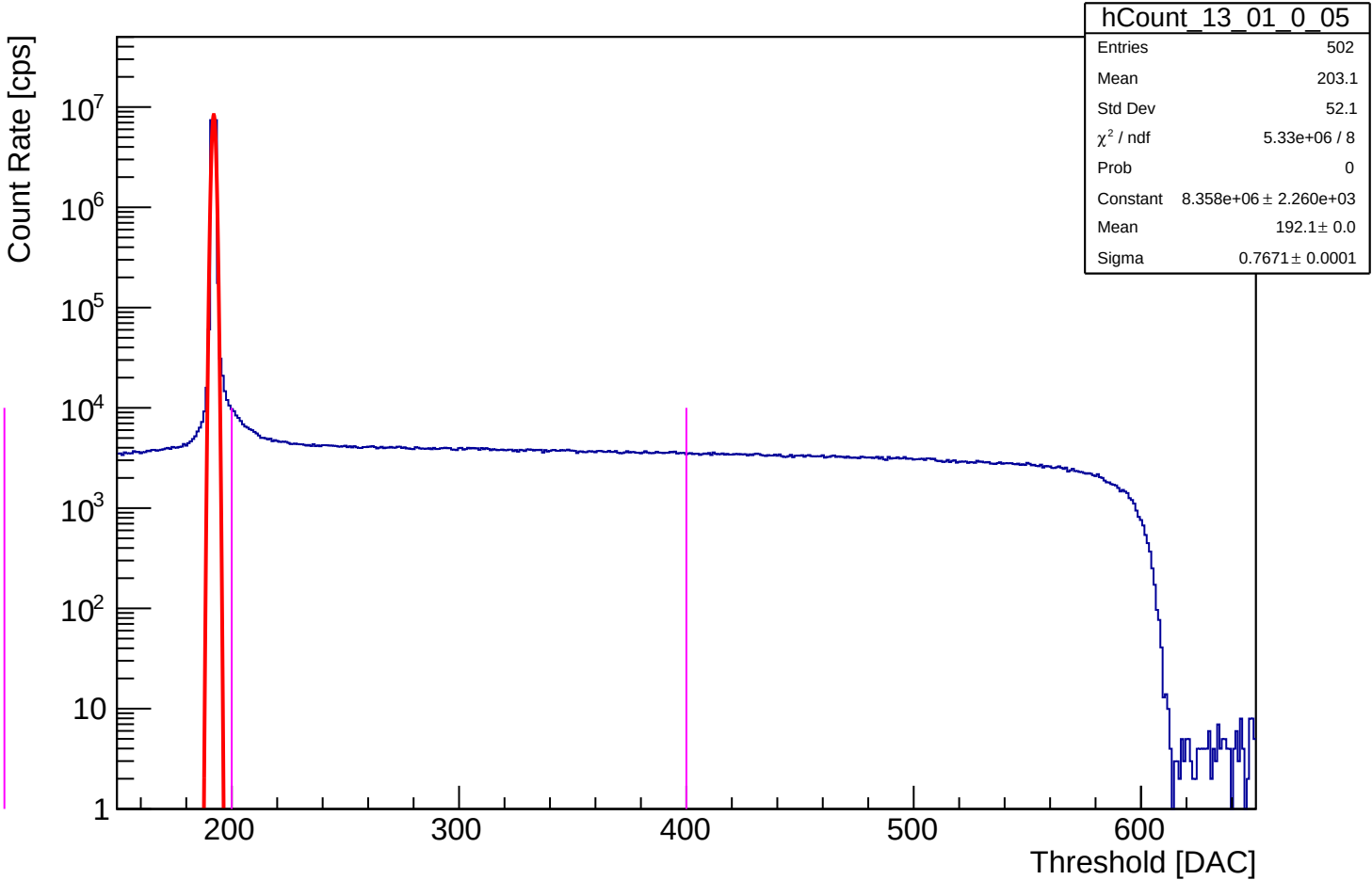
Row 1 Tile 1 Pmt 4 Pixel 47 Slot 13 Fiber 1 Asic 0 Channel 53

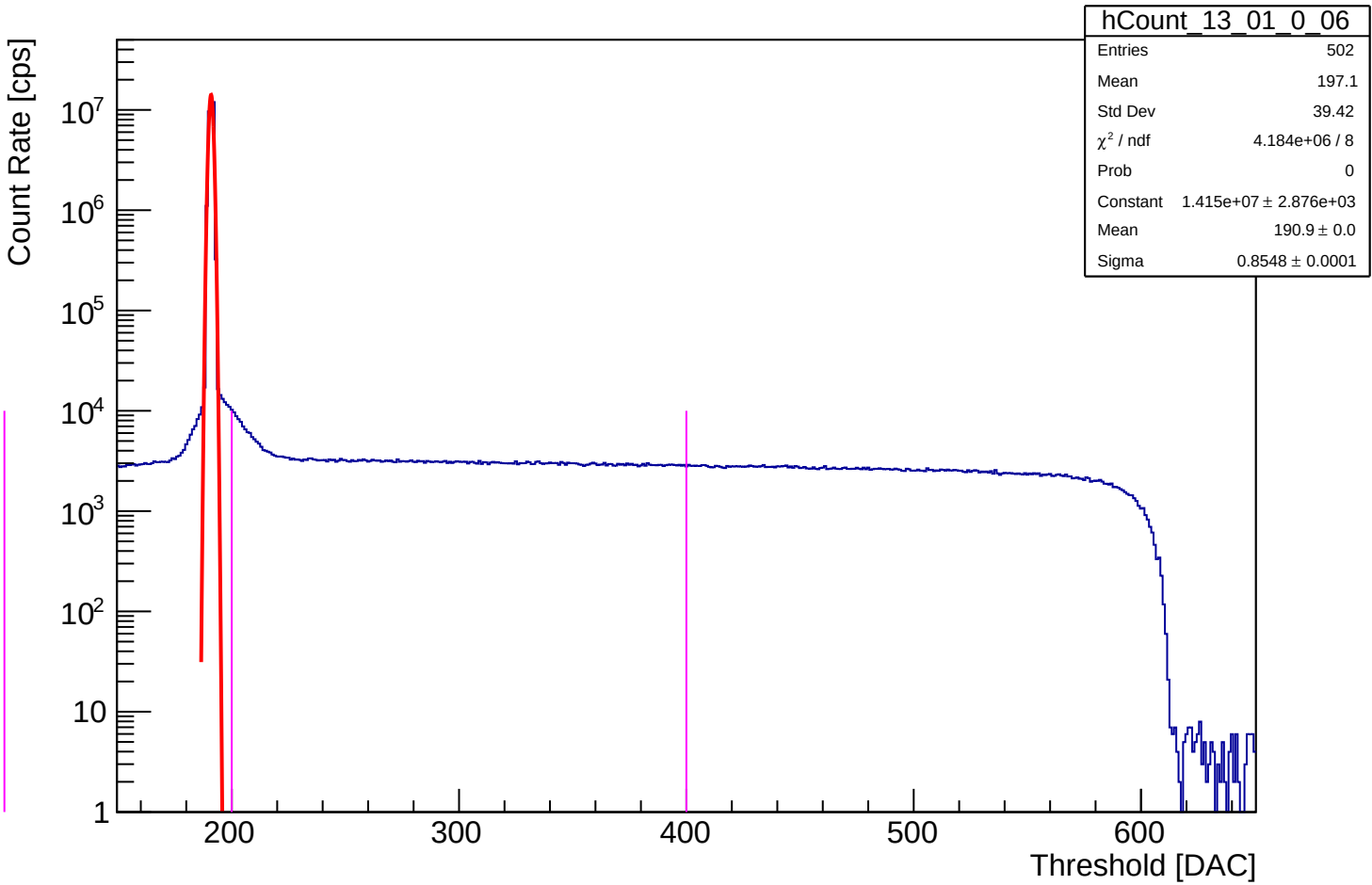


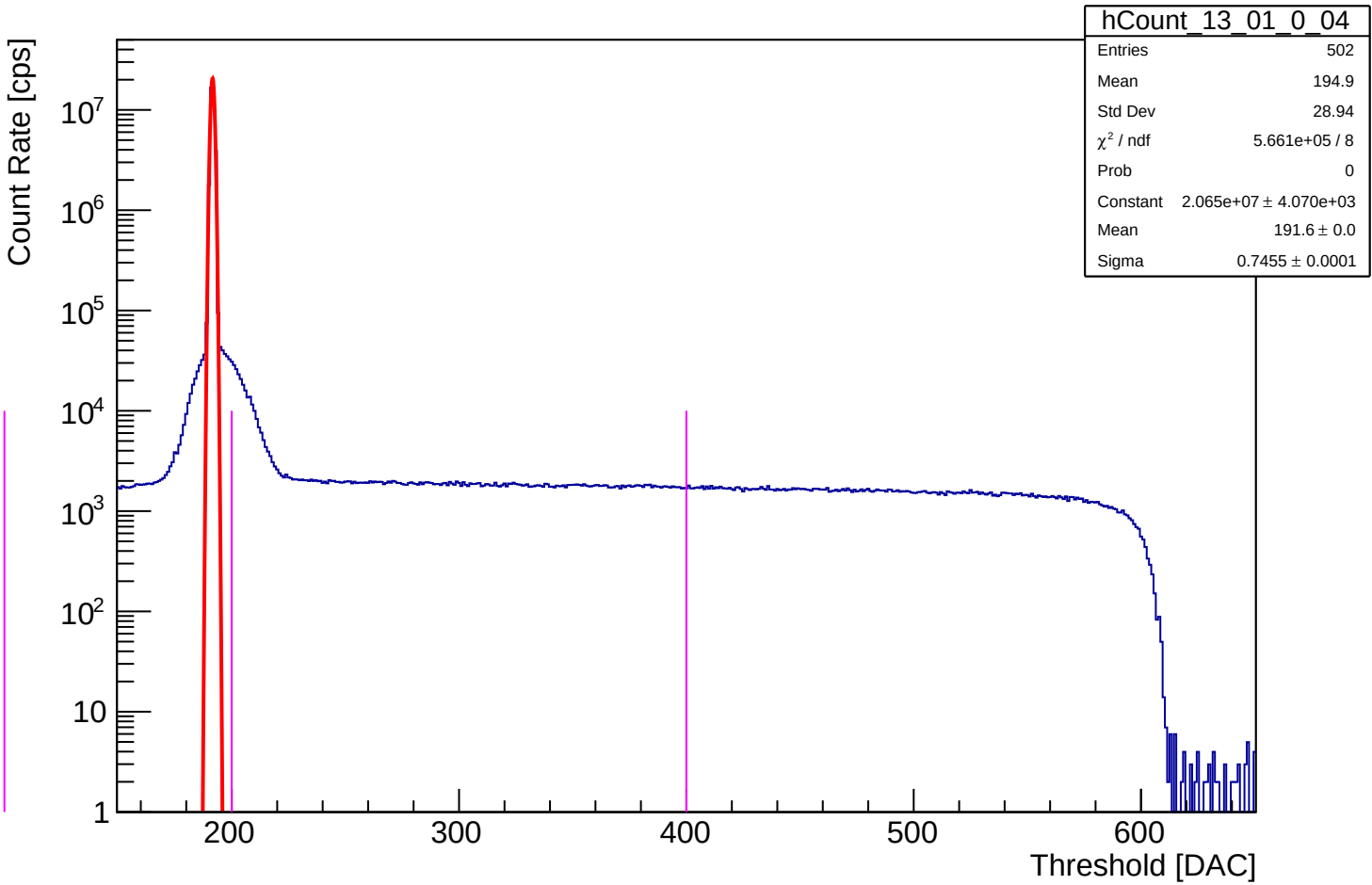
Row 1 Tile 1 Pmt 4 Pixel 48 Slot 13 Fiber 1 Asic 0 Channel 55



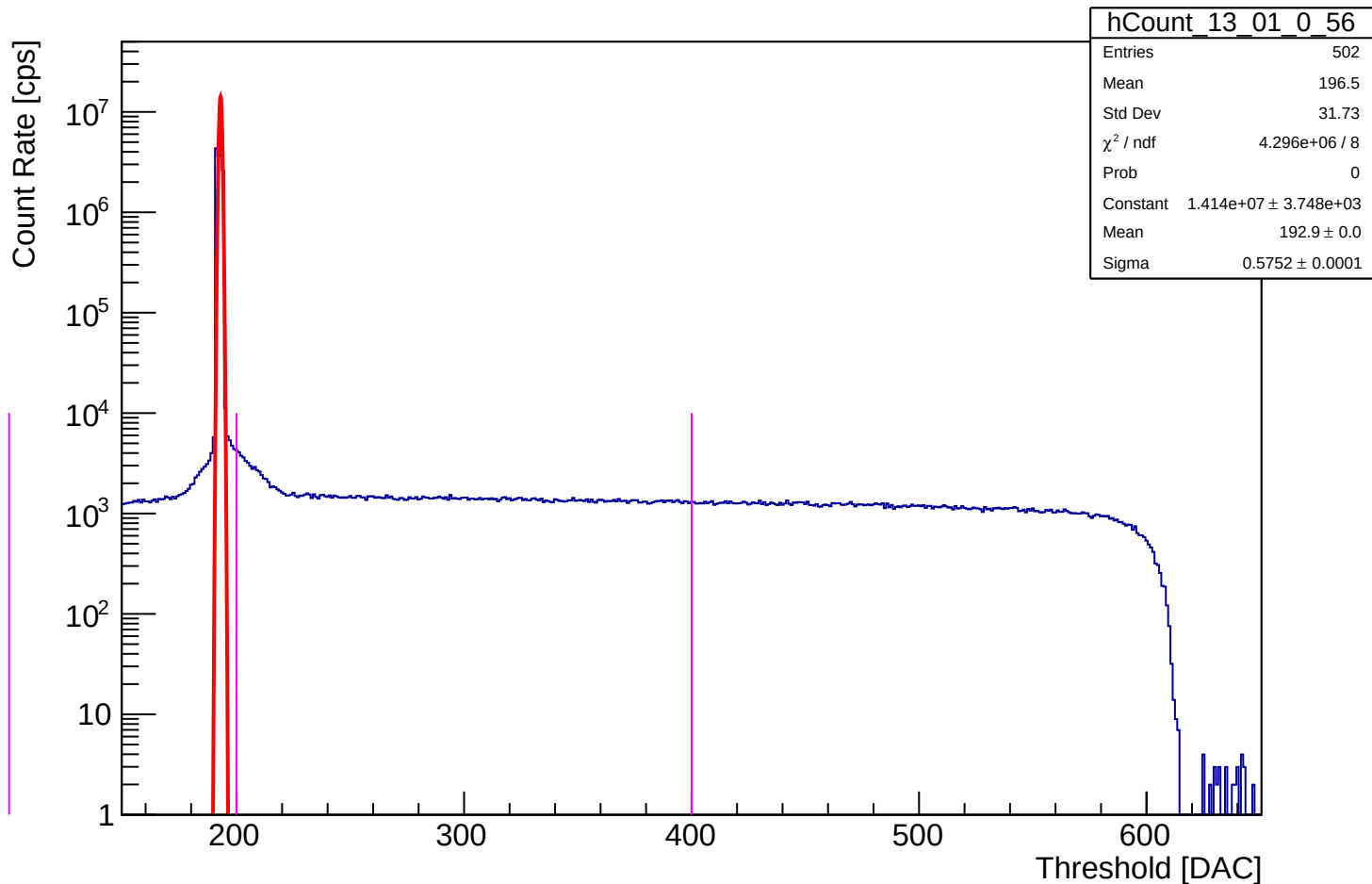




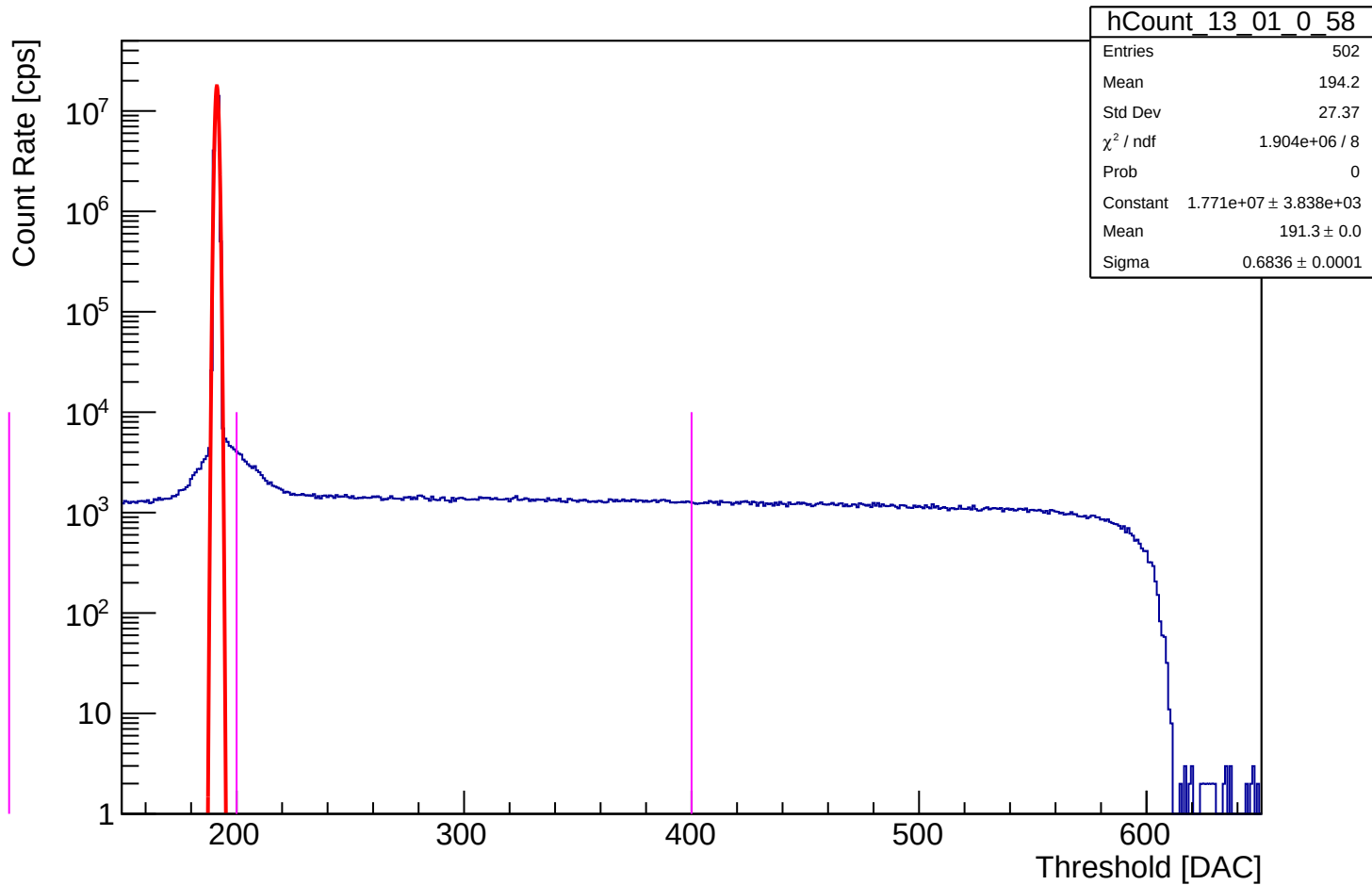




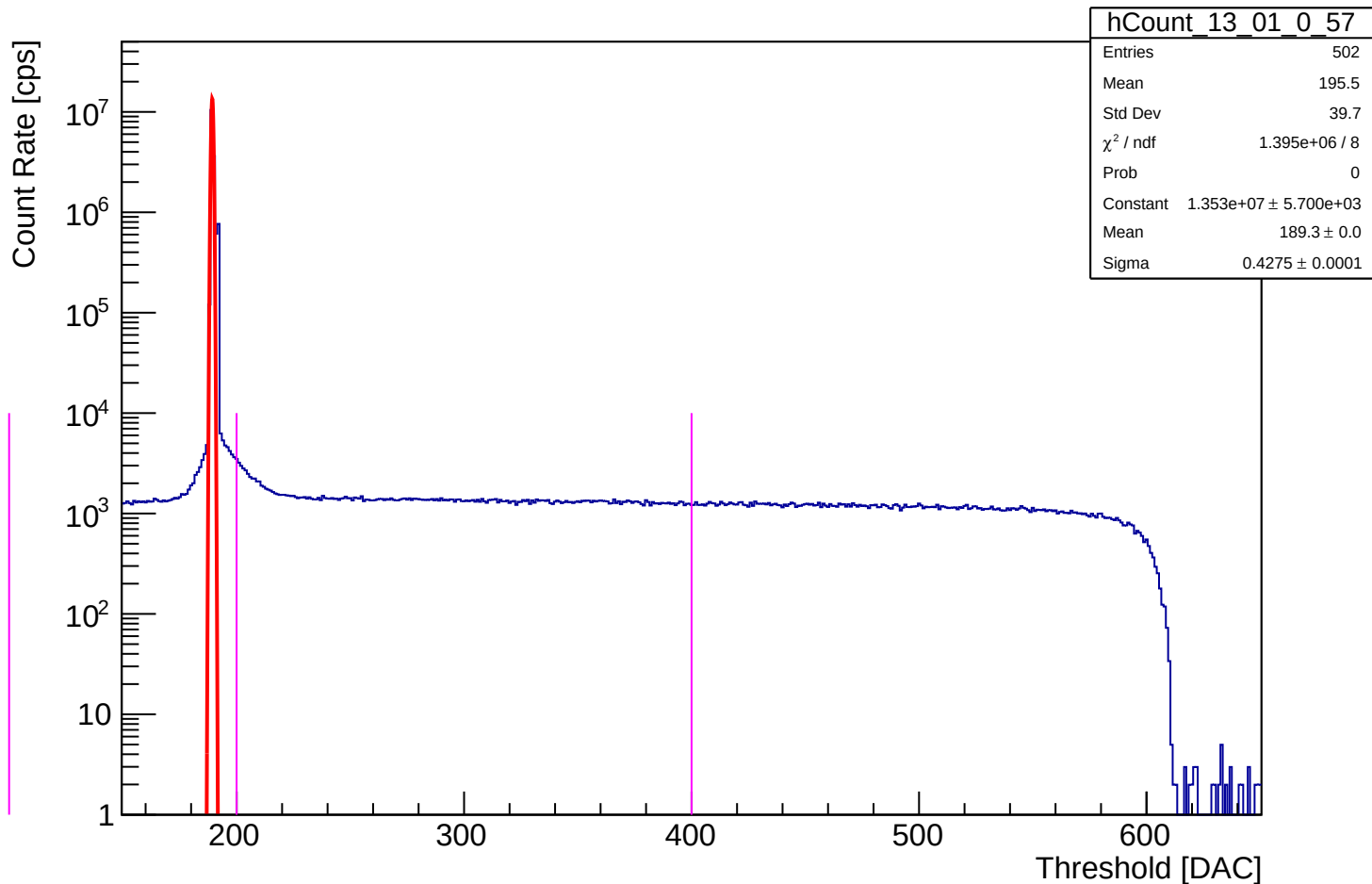
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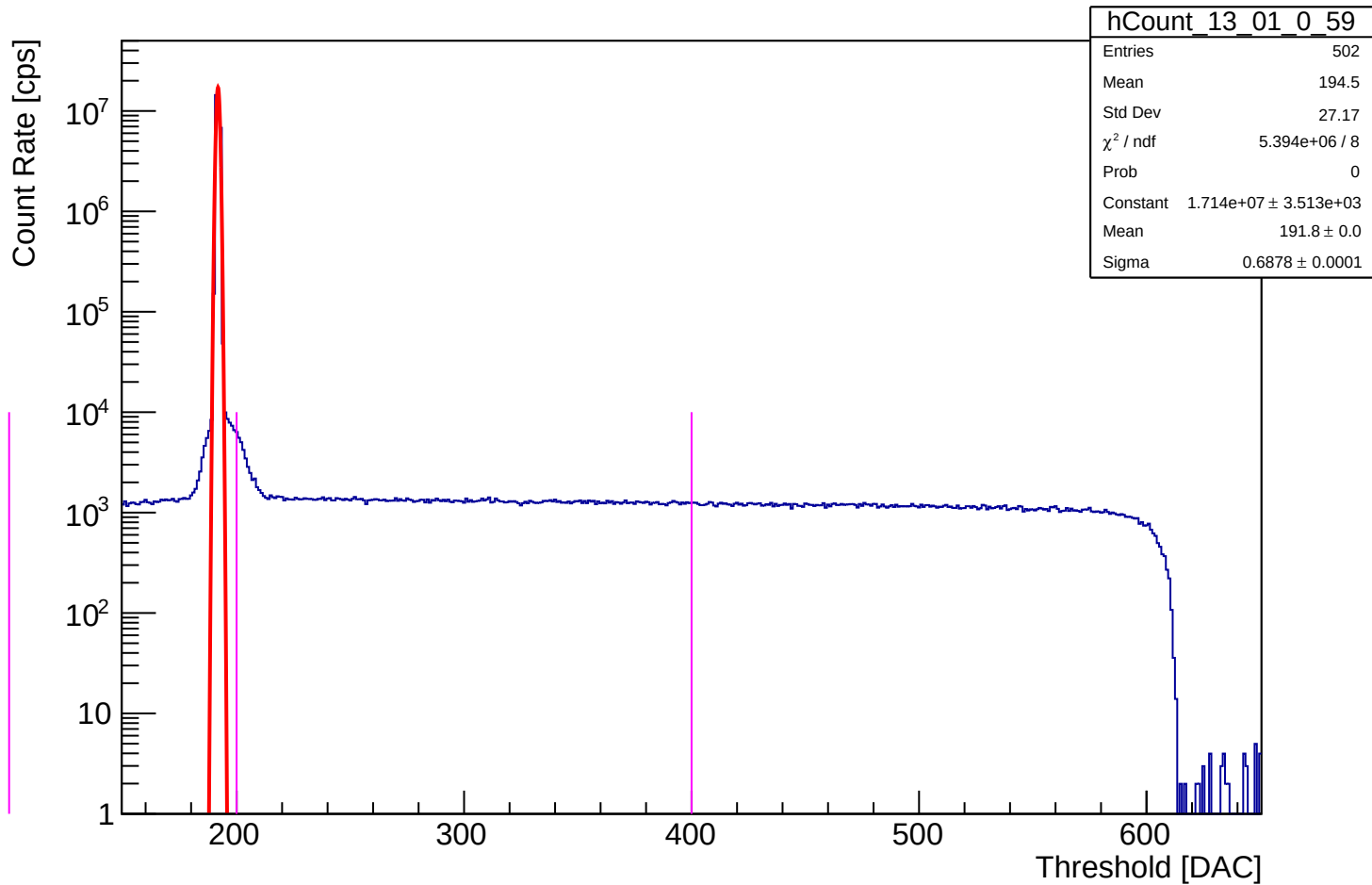
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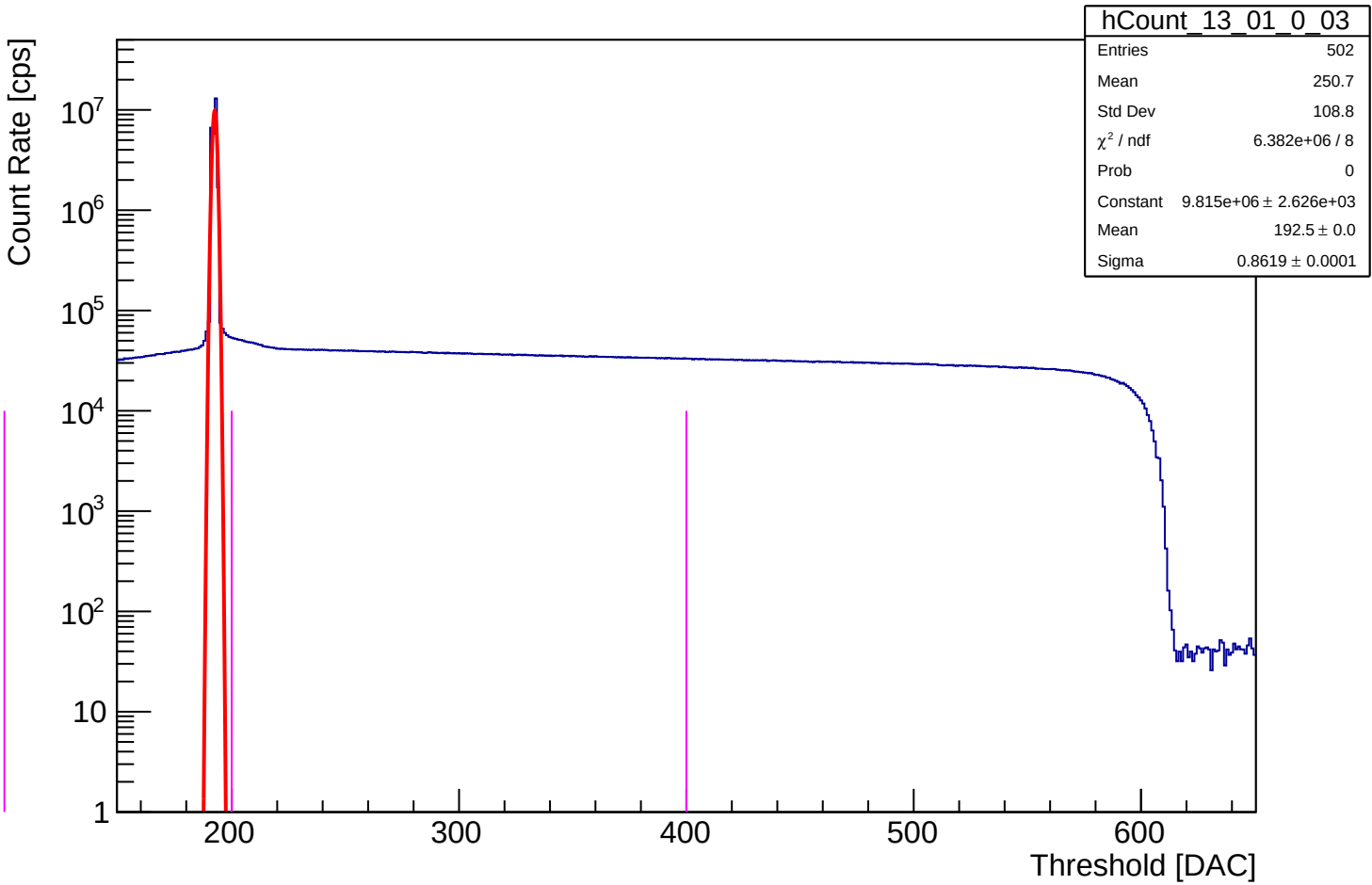


Row 1 Tile 1 Pmt 4 Pixel 55 Slot 13 Fiber 1 Asic 0 Channel 57

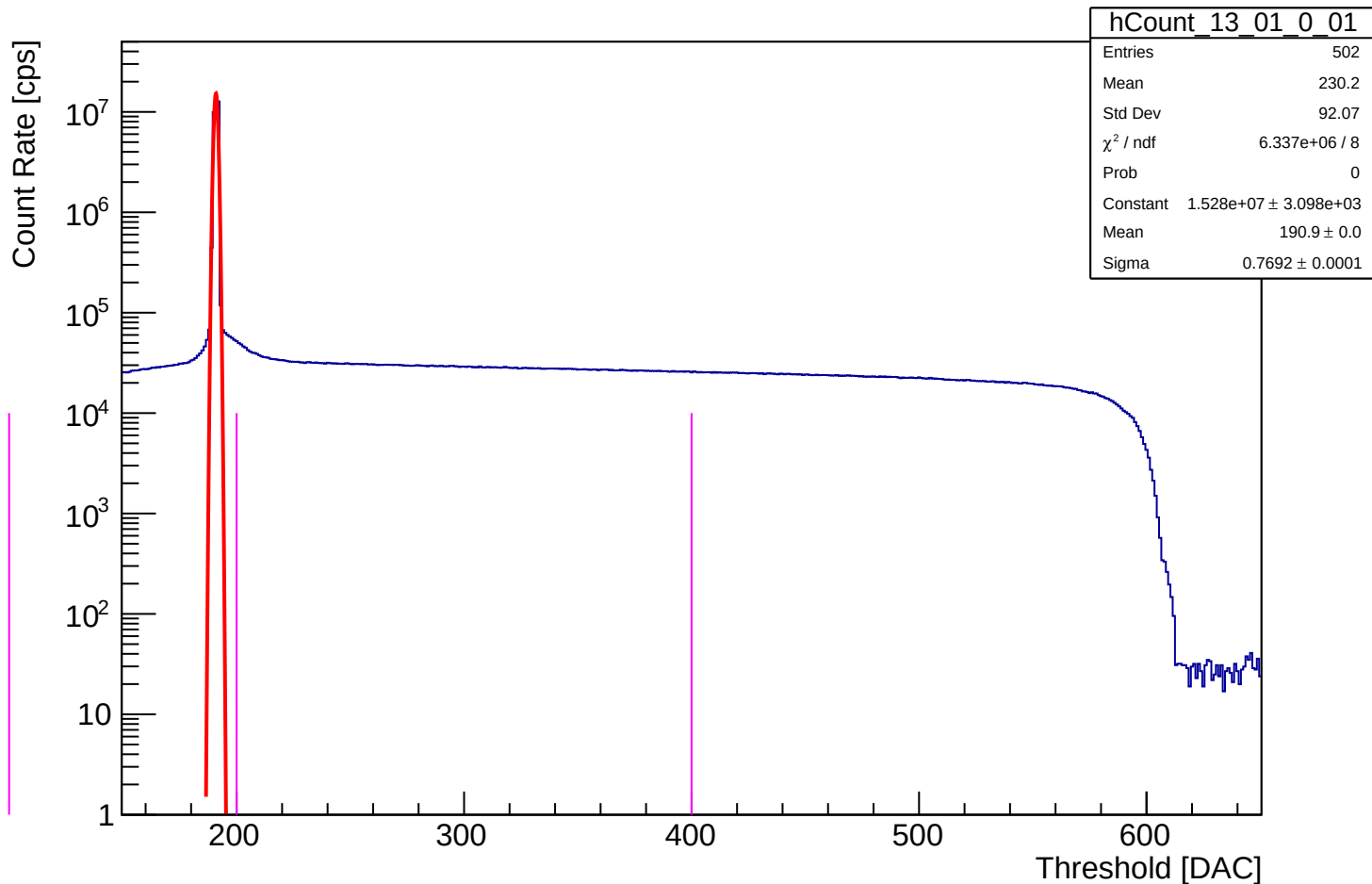


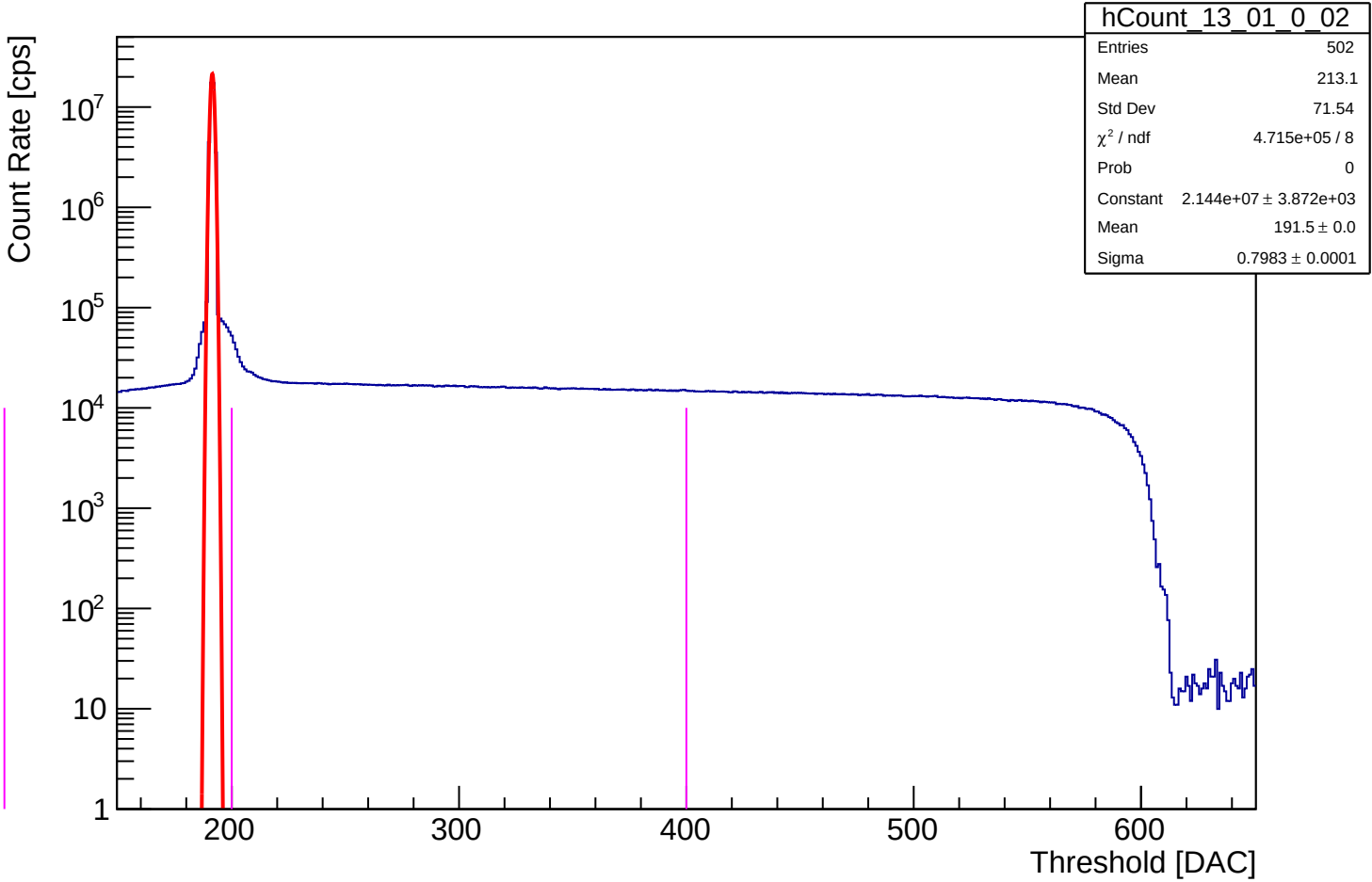
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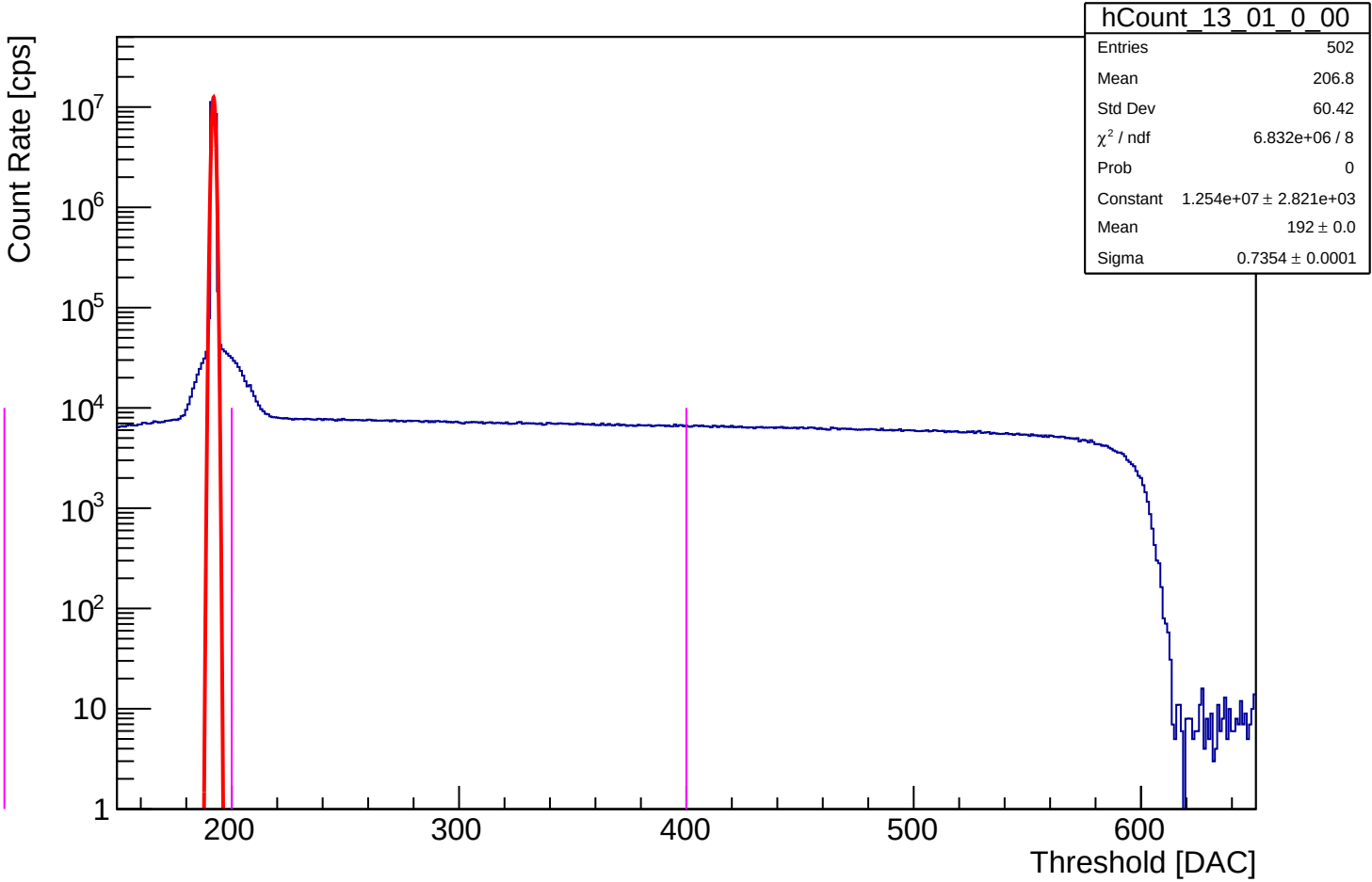




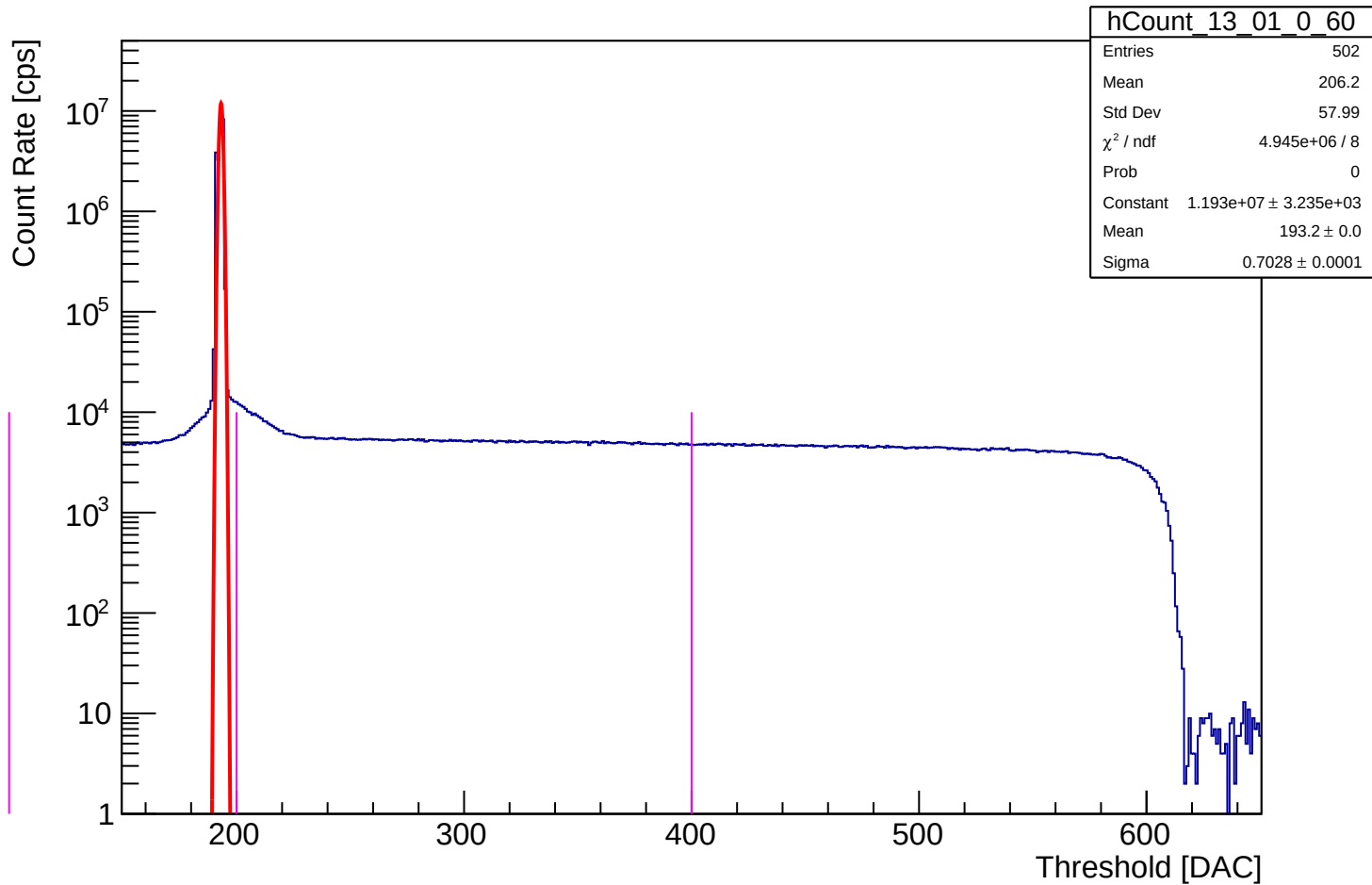
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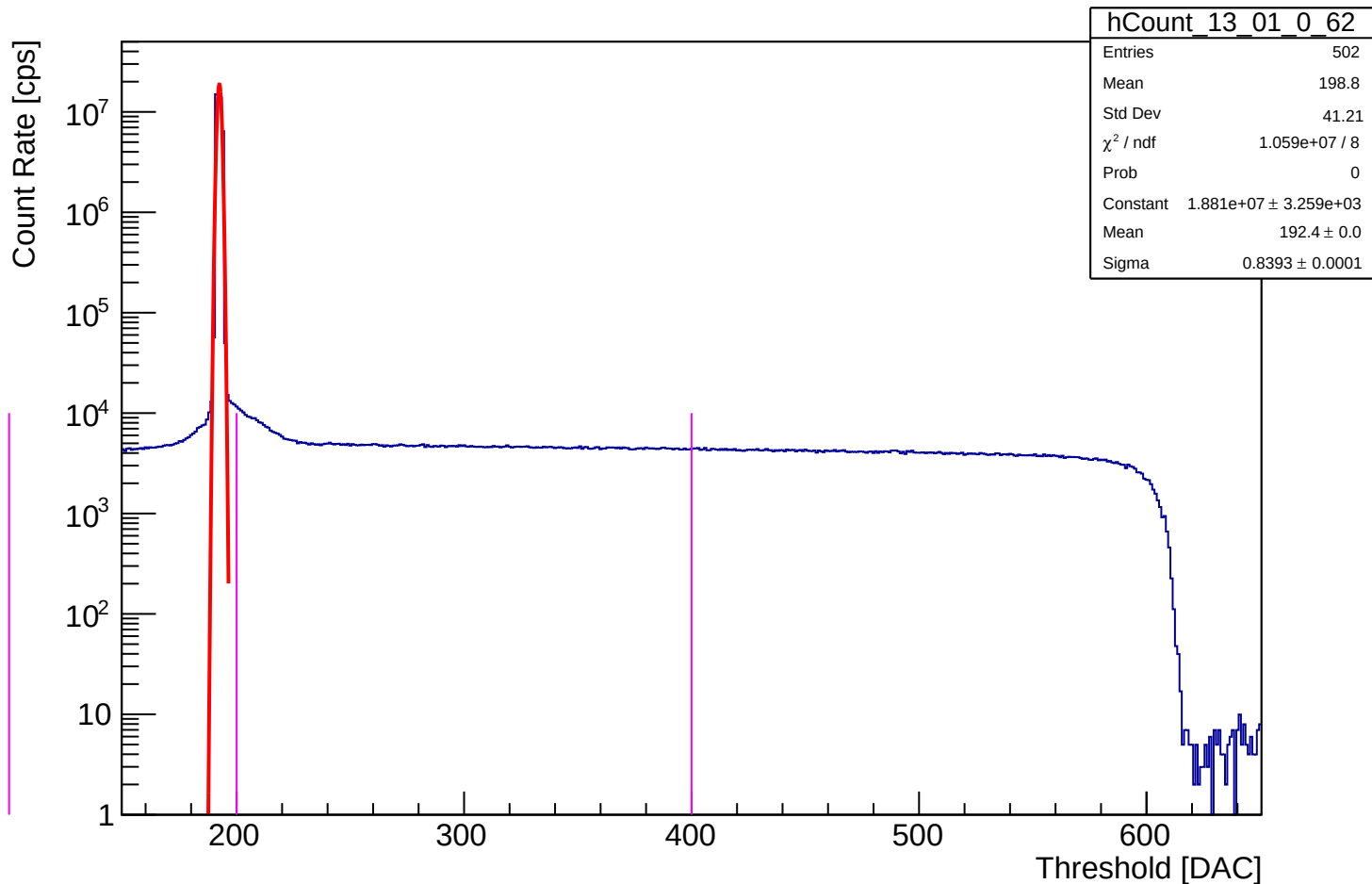




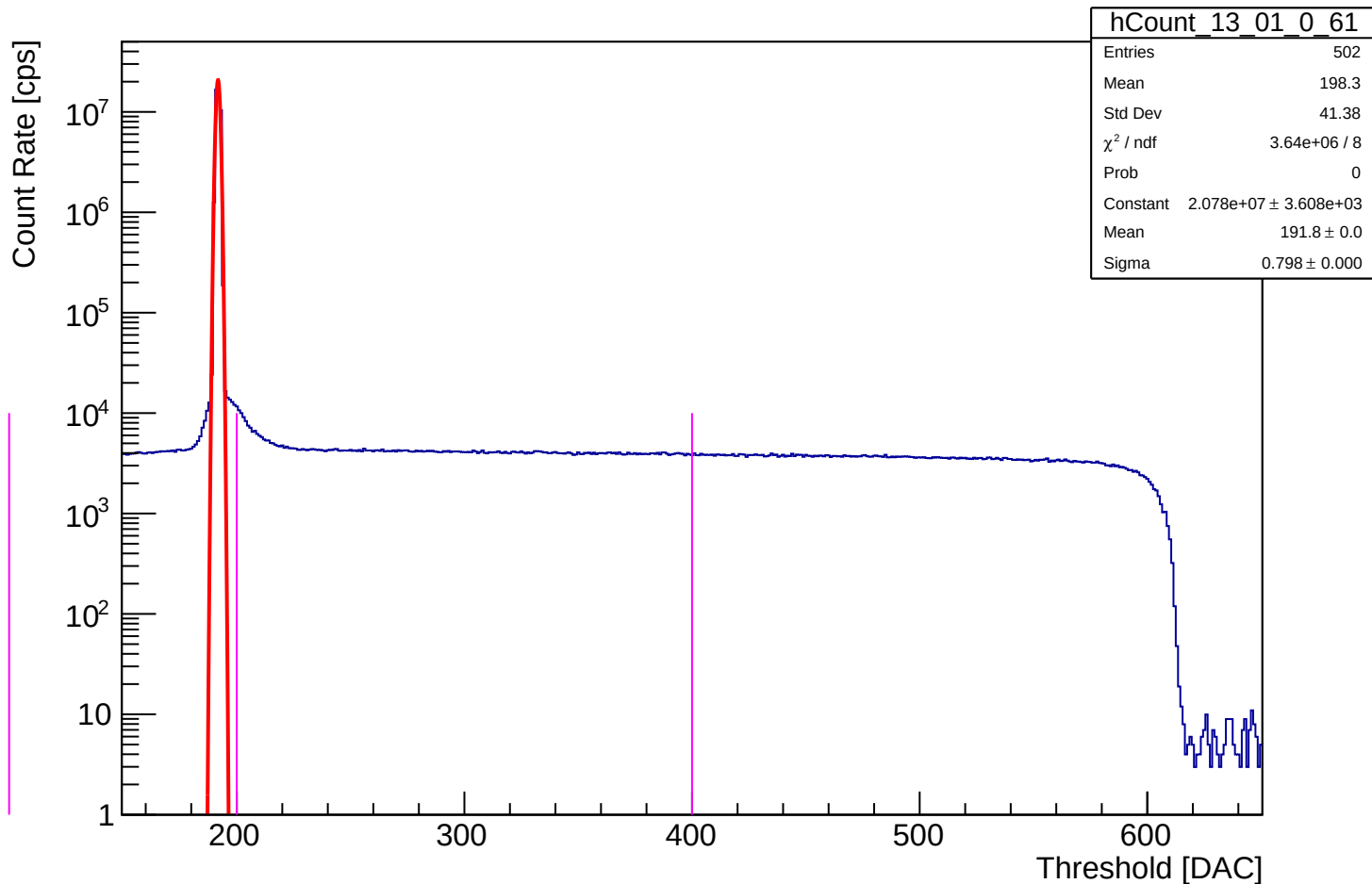
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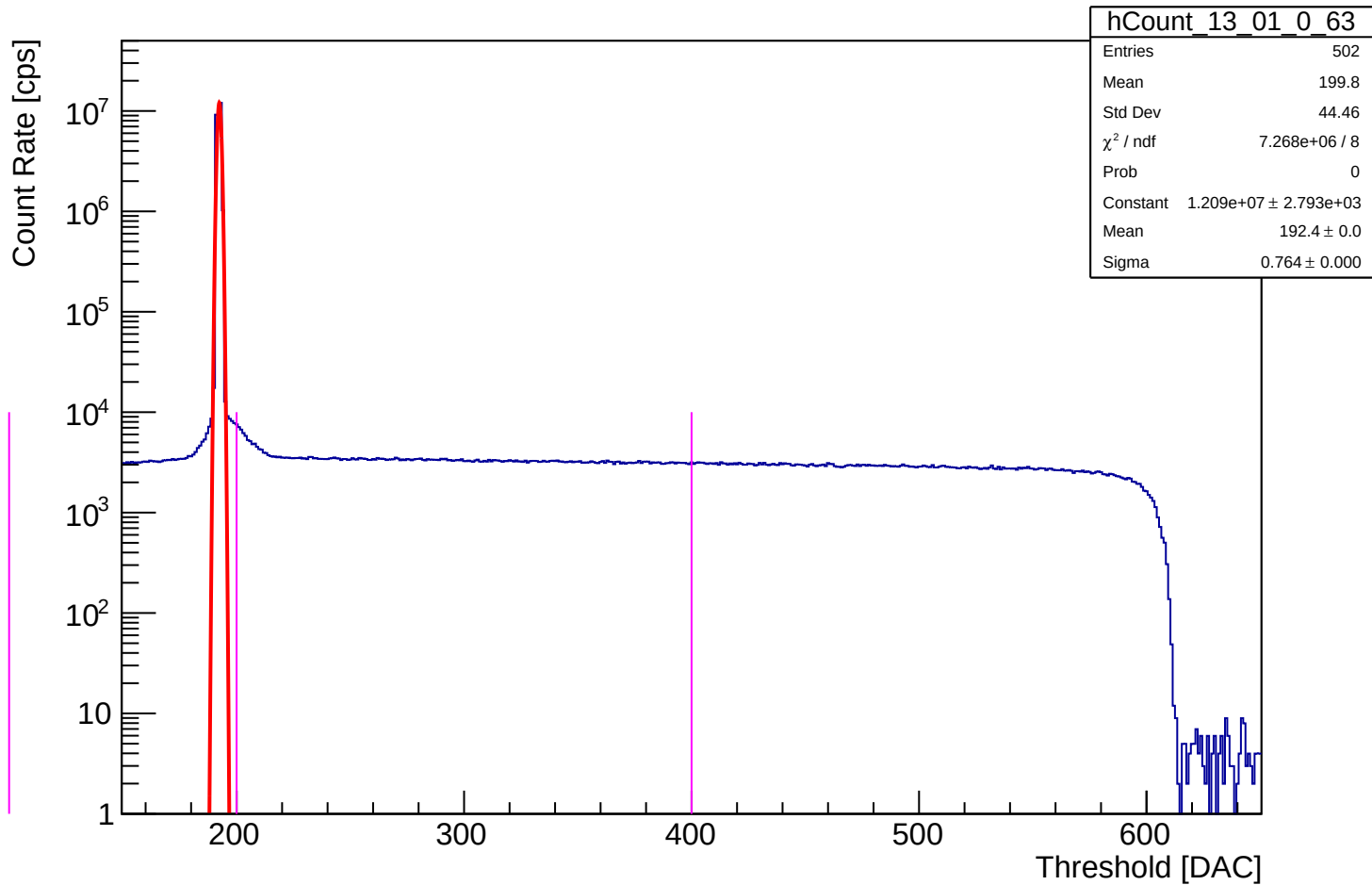
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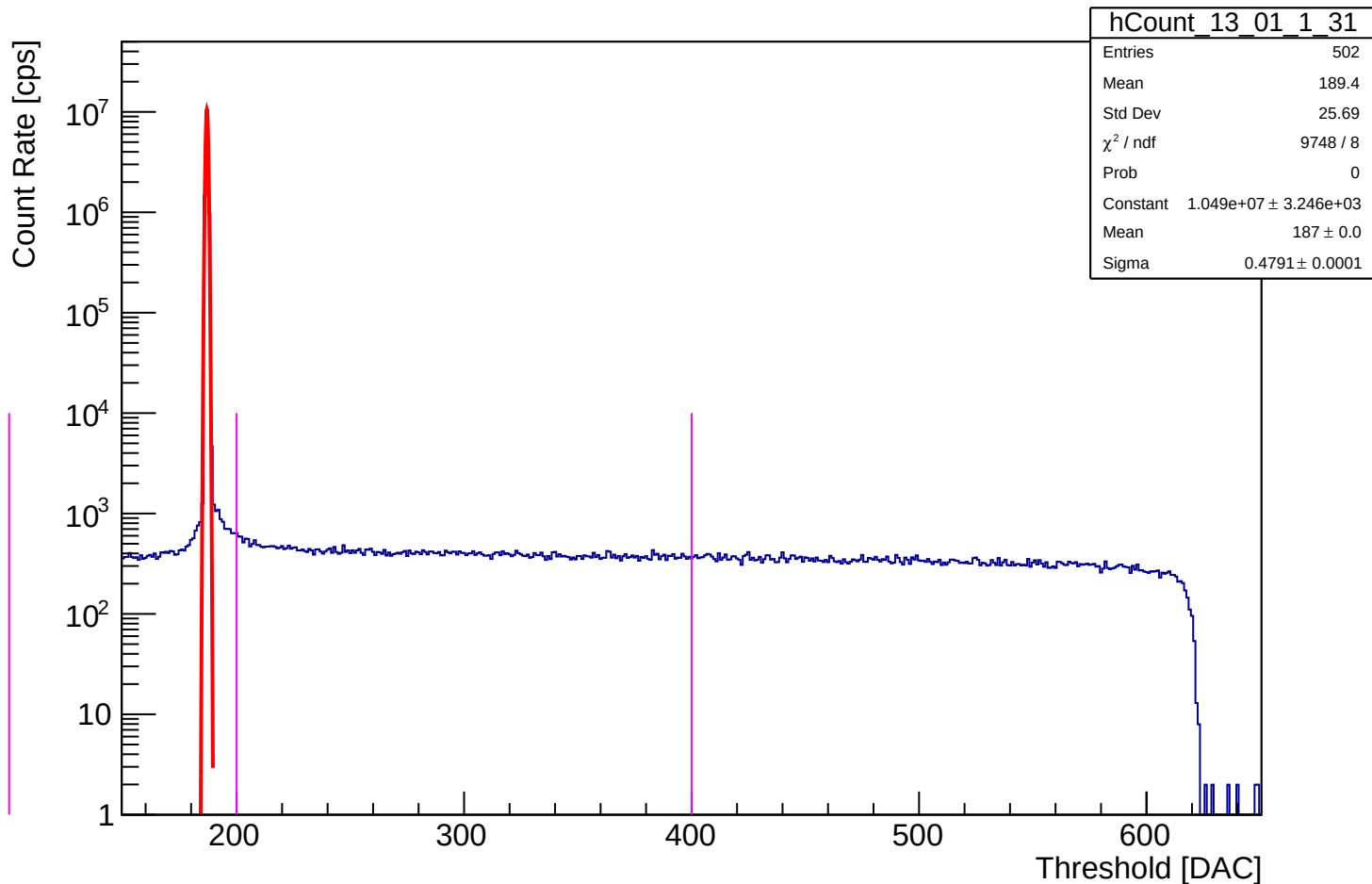
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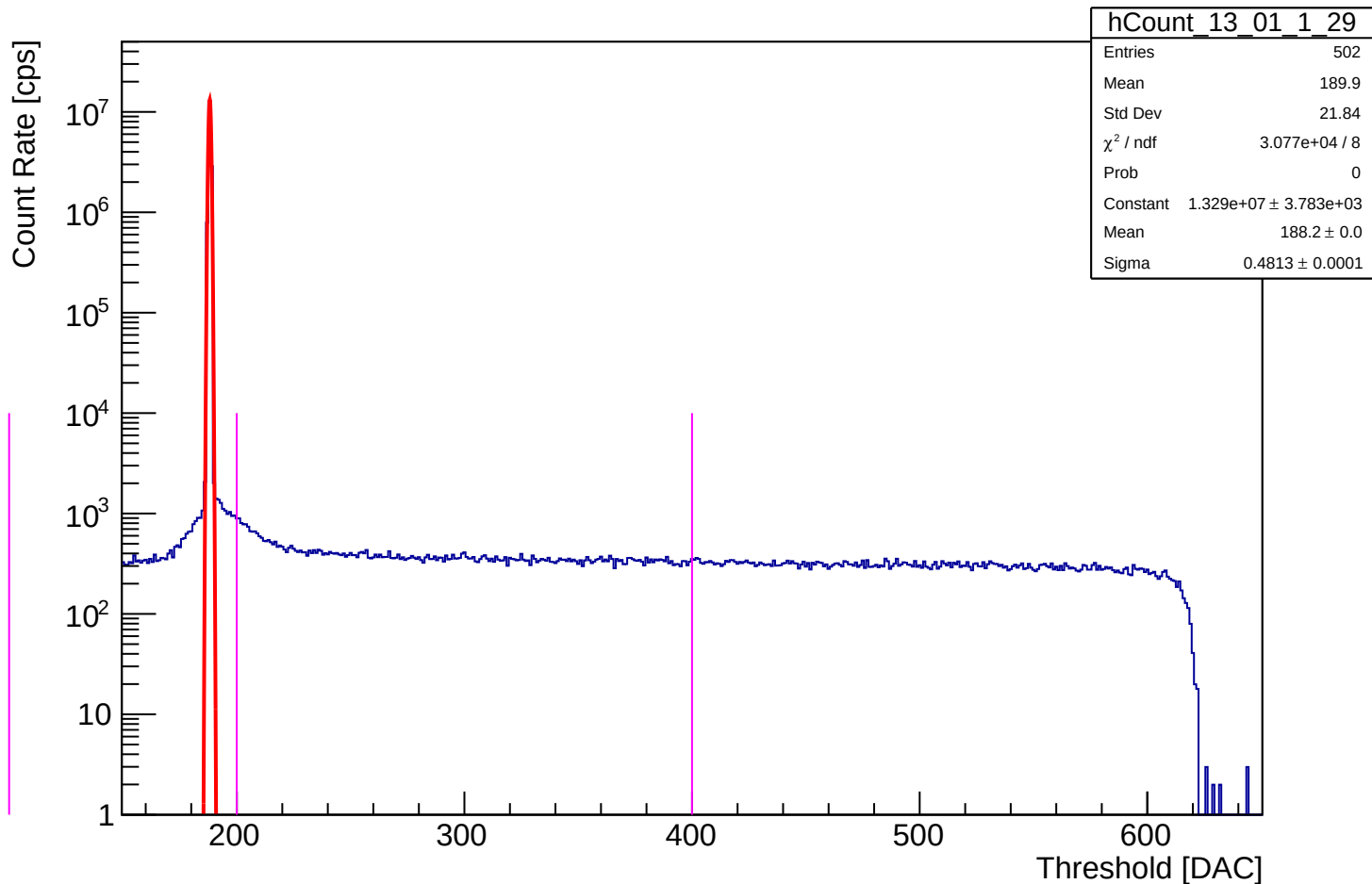
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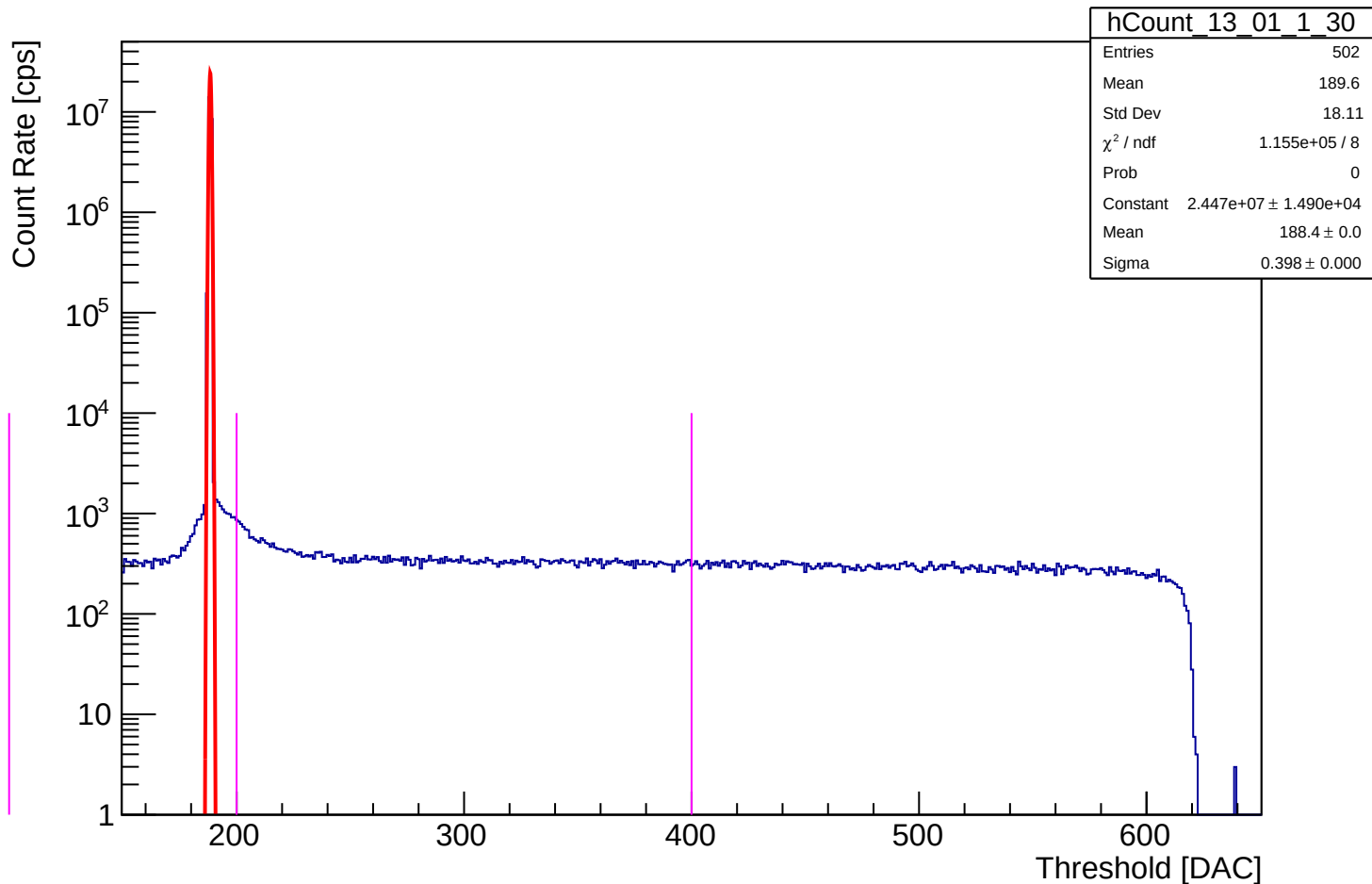
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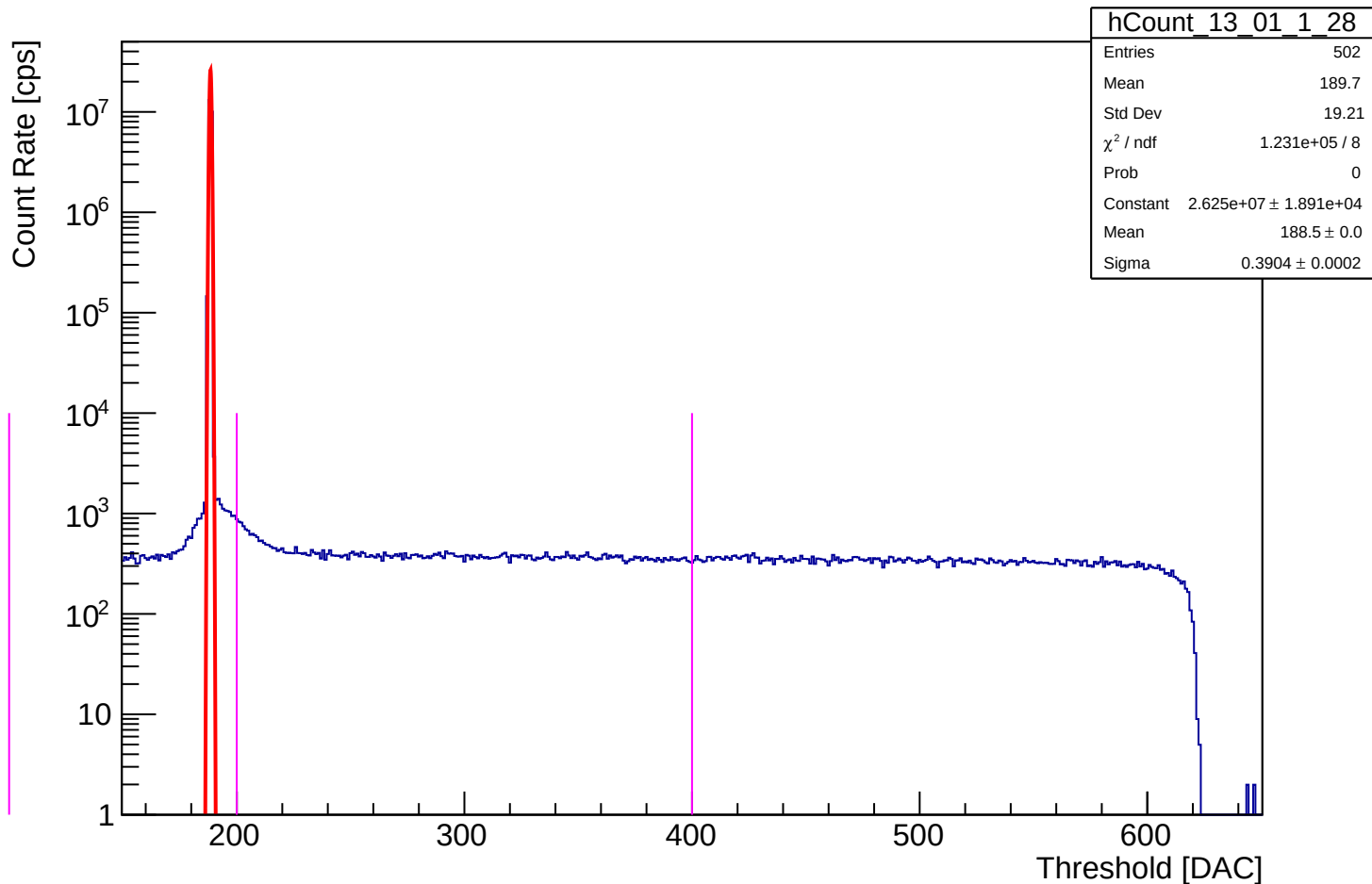
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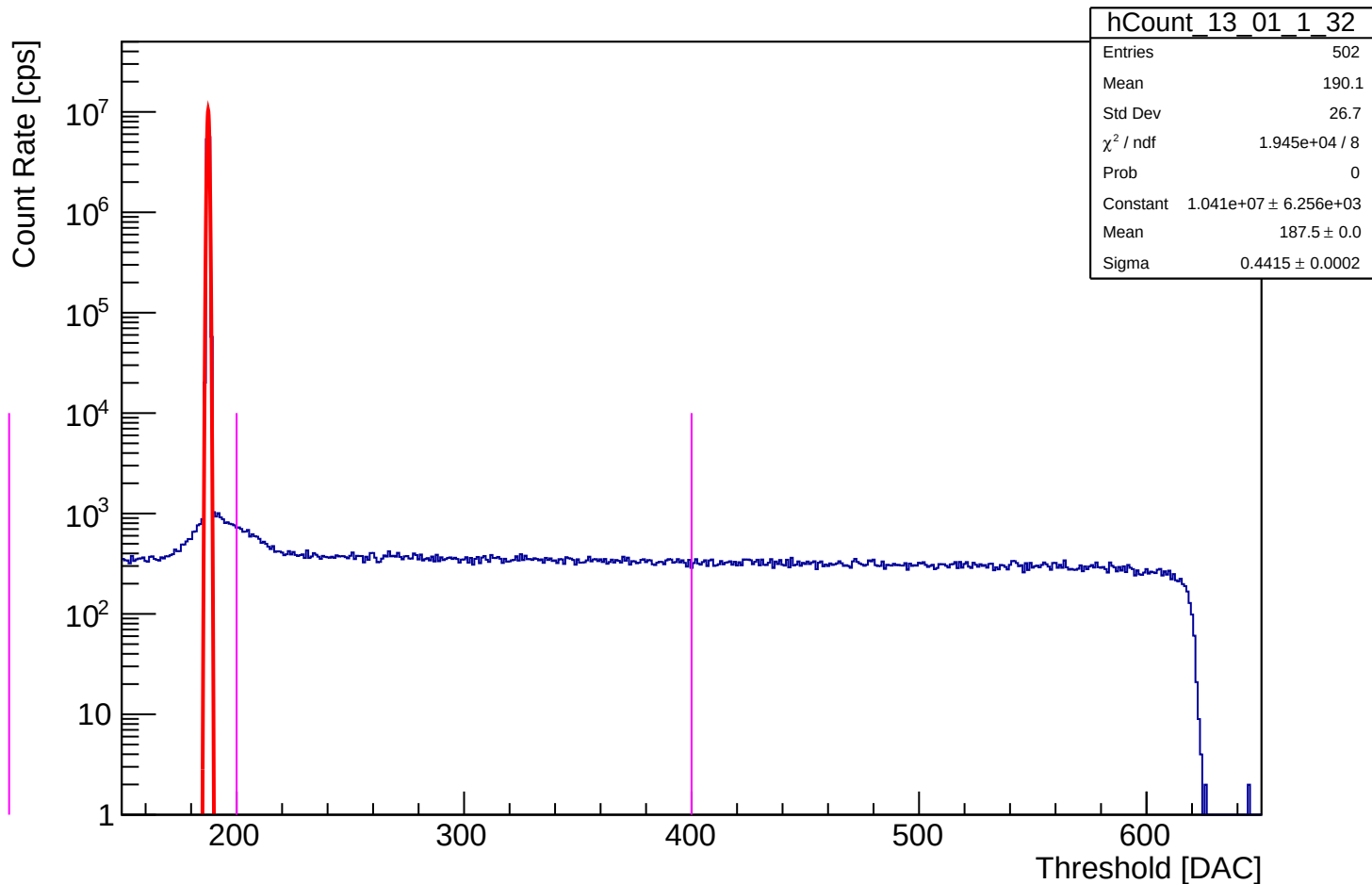
Row 1 Tile 1 Pmt 5 Pixel 3 Slot 13 Fiber 1 Asic 1 Channel 30



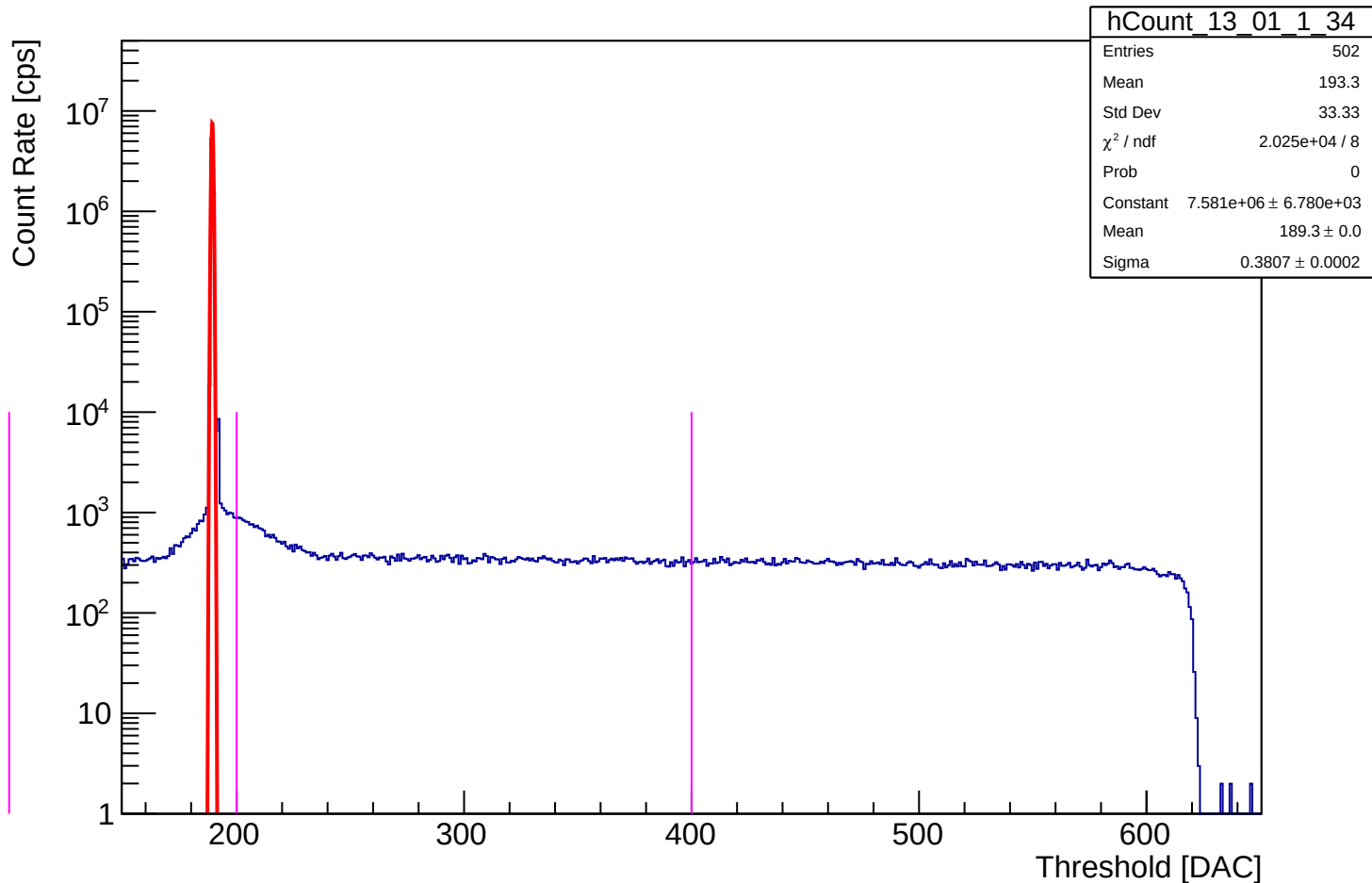
Row 1 Tile 1 Pmt 5 Pixel 4 Slot 13 Fiber 1 Asic 1 Channel 28



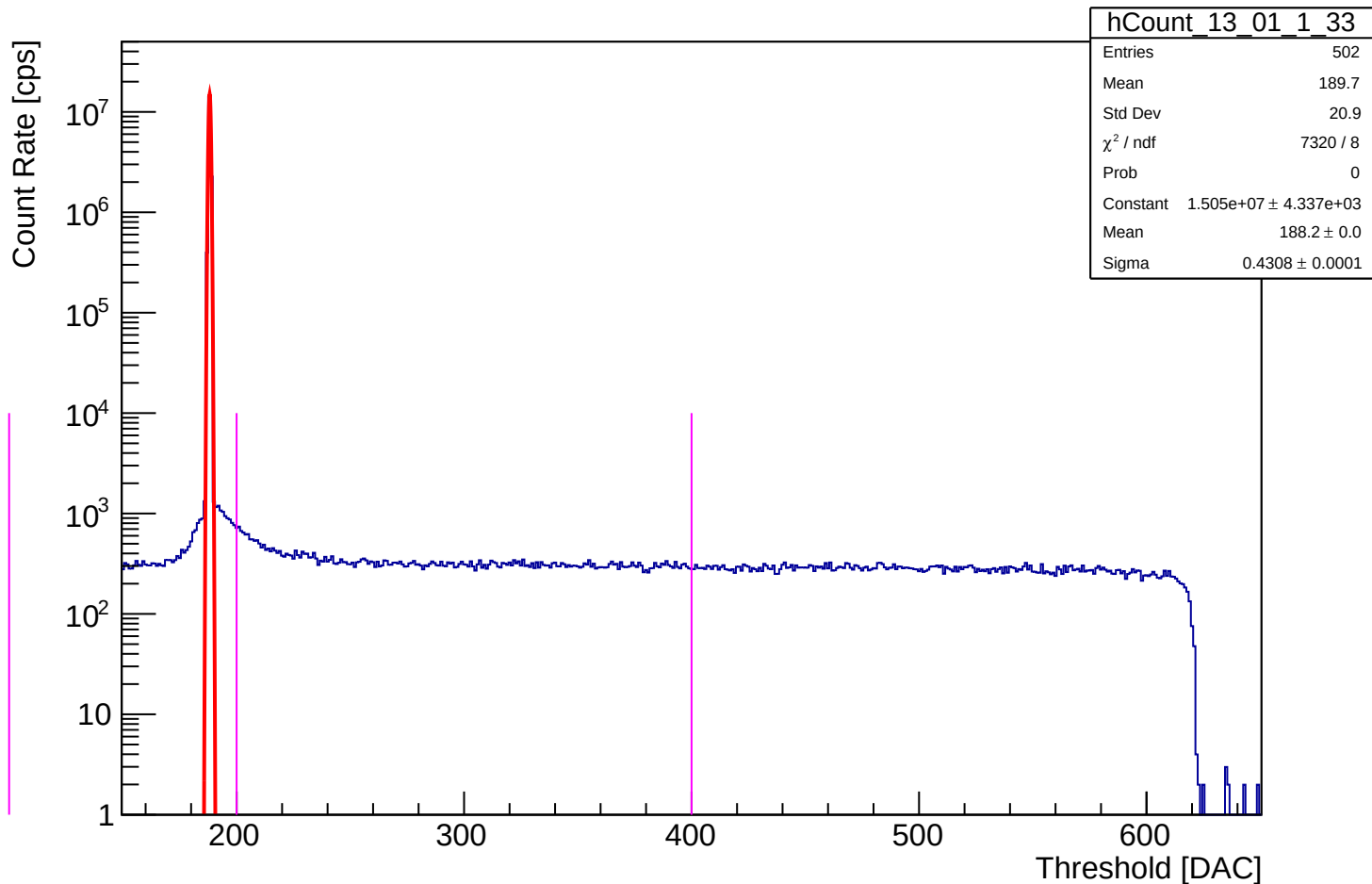
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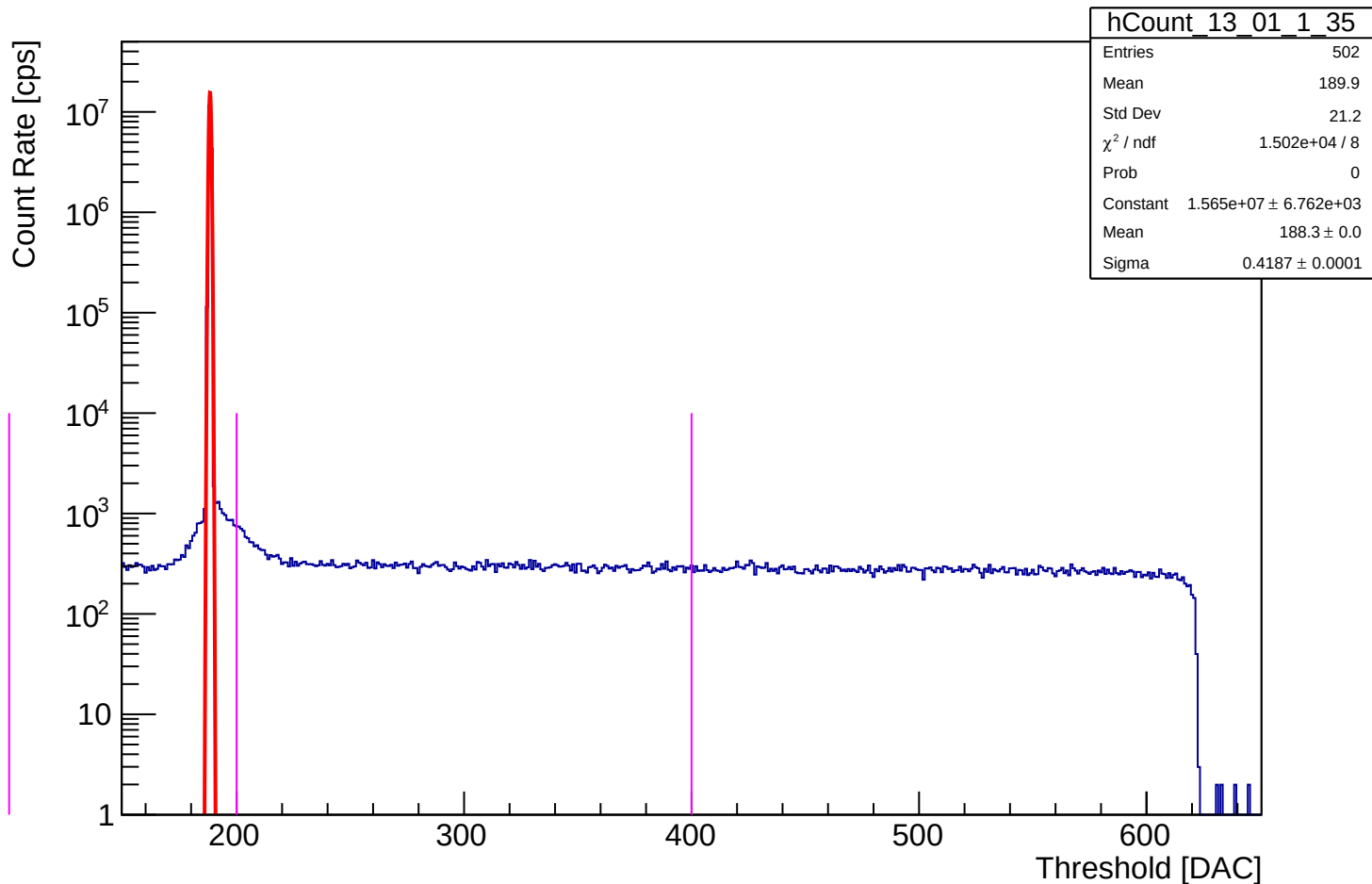
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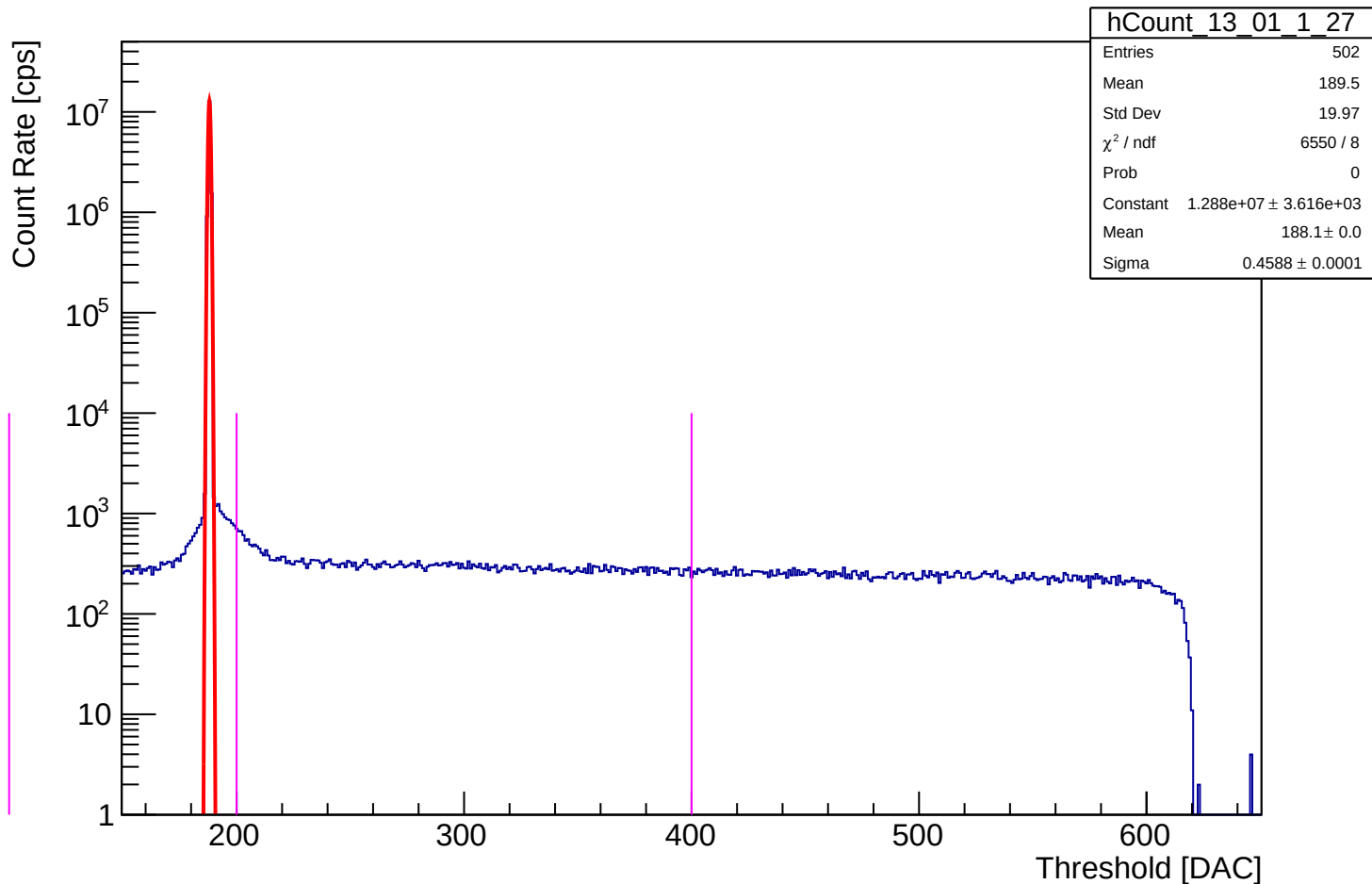
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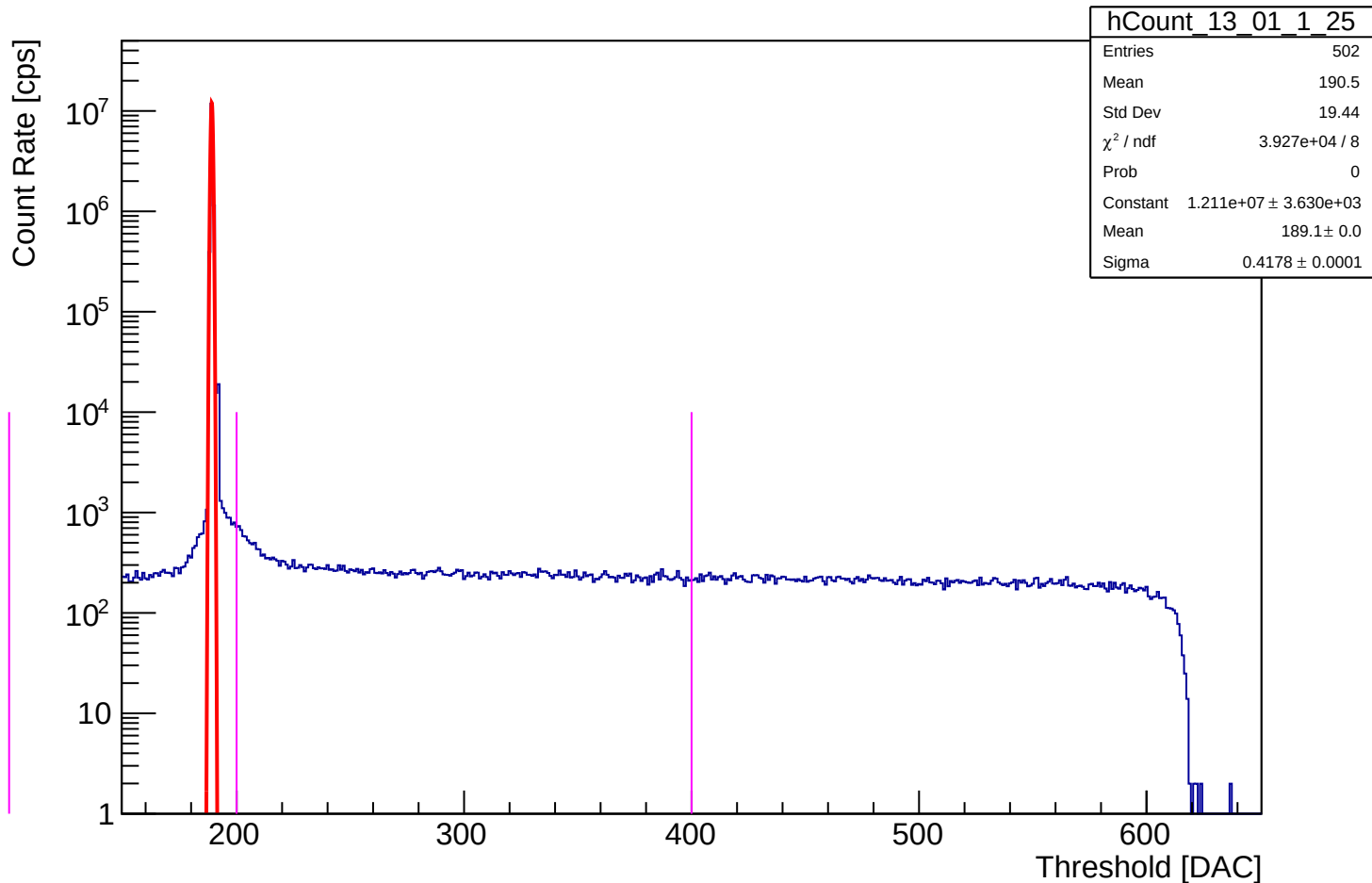
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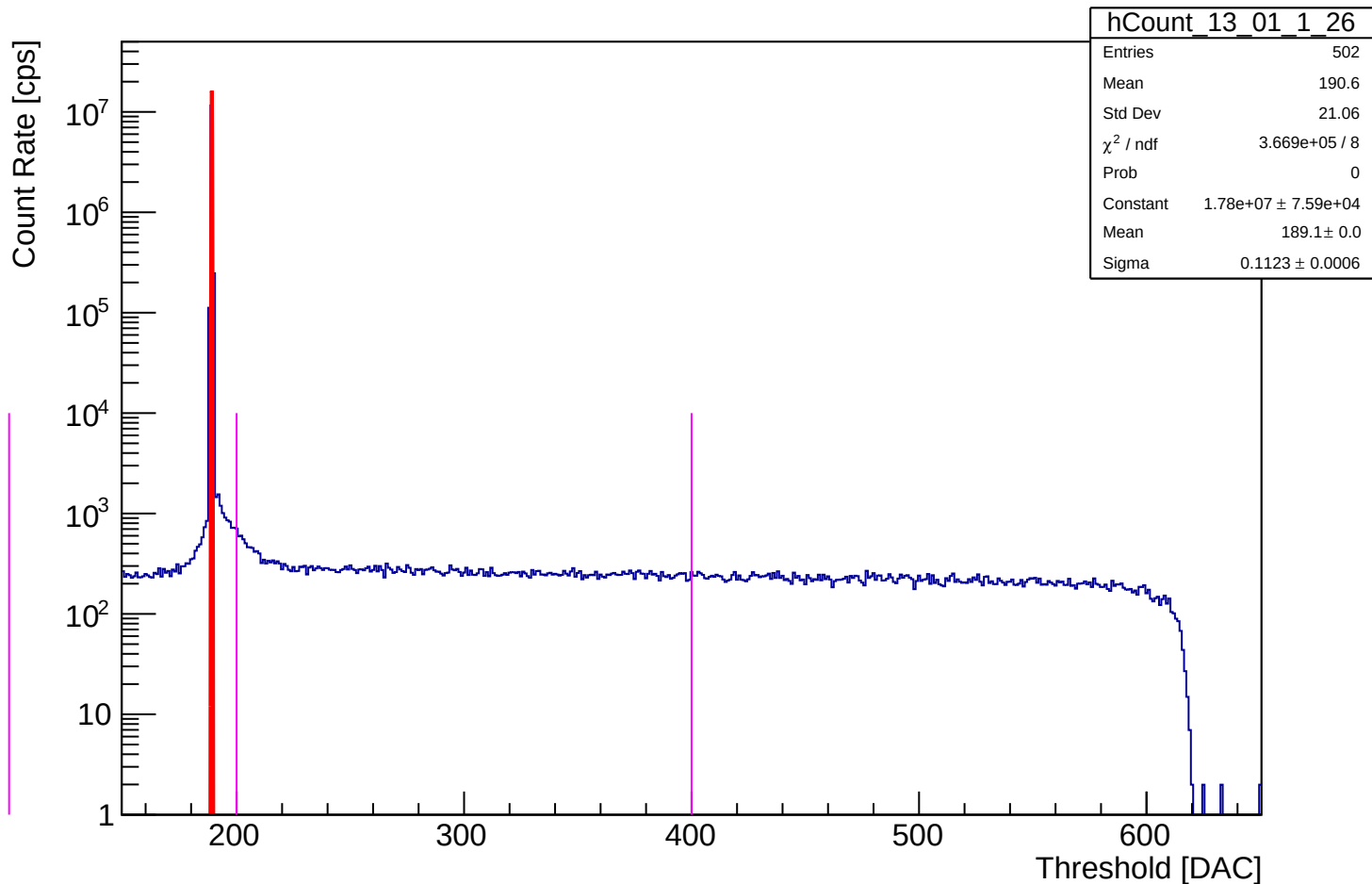
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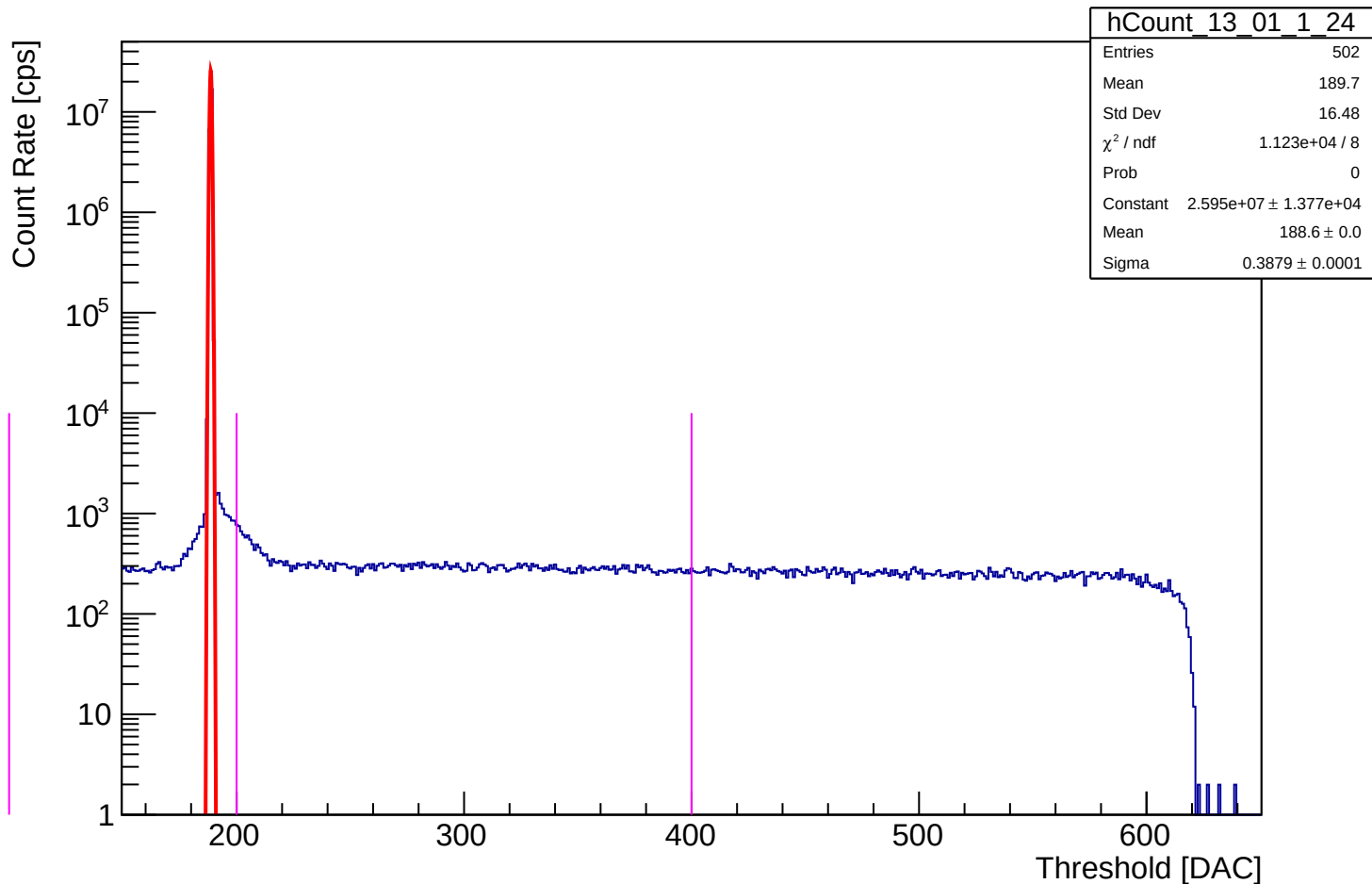
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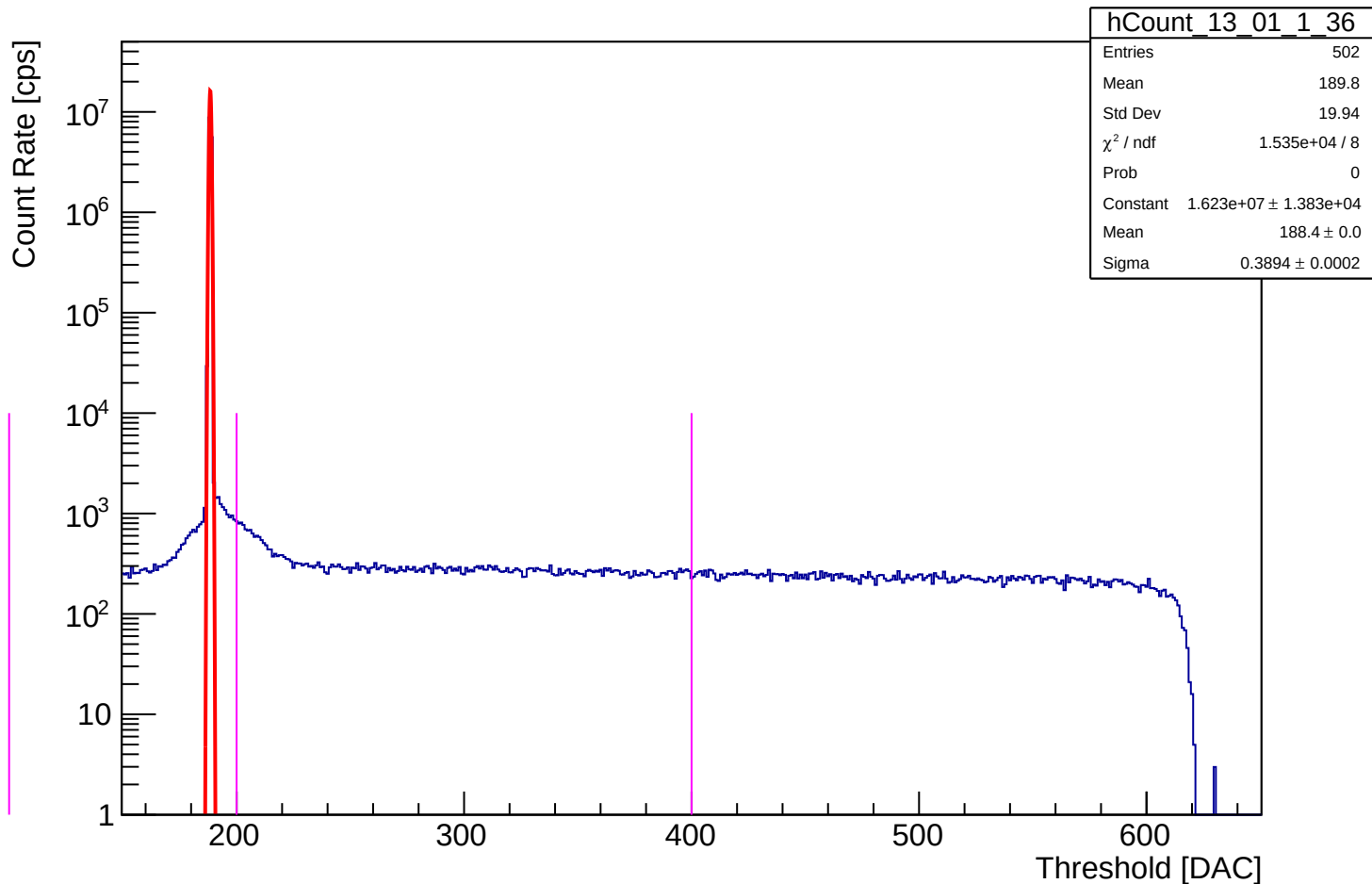
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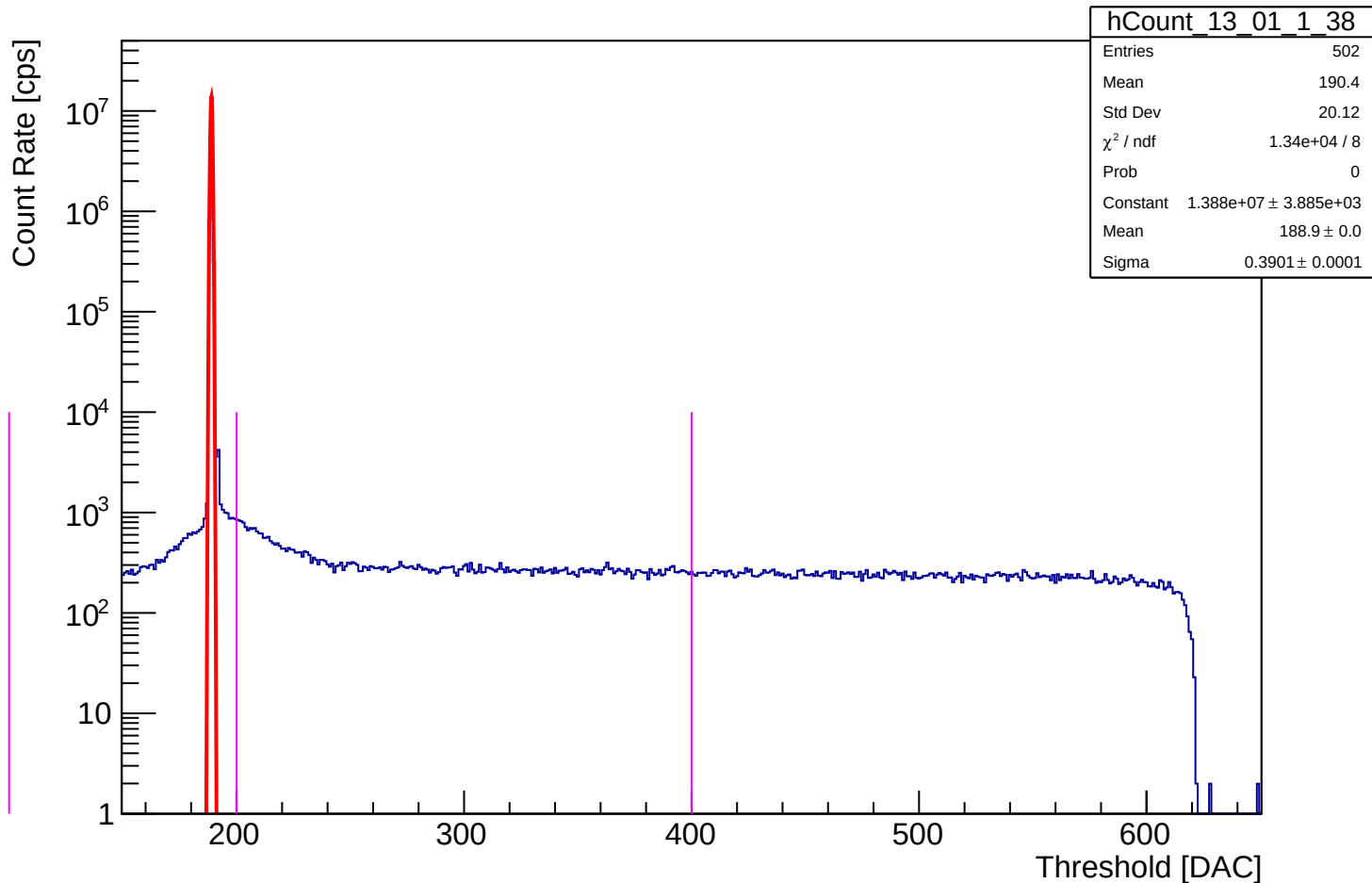
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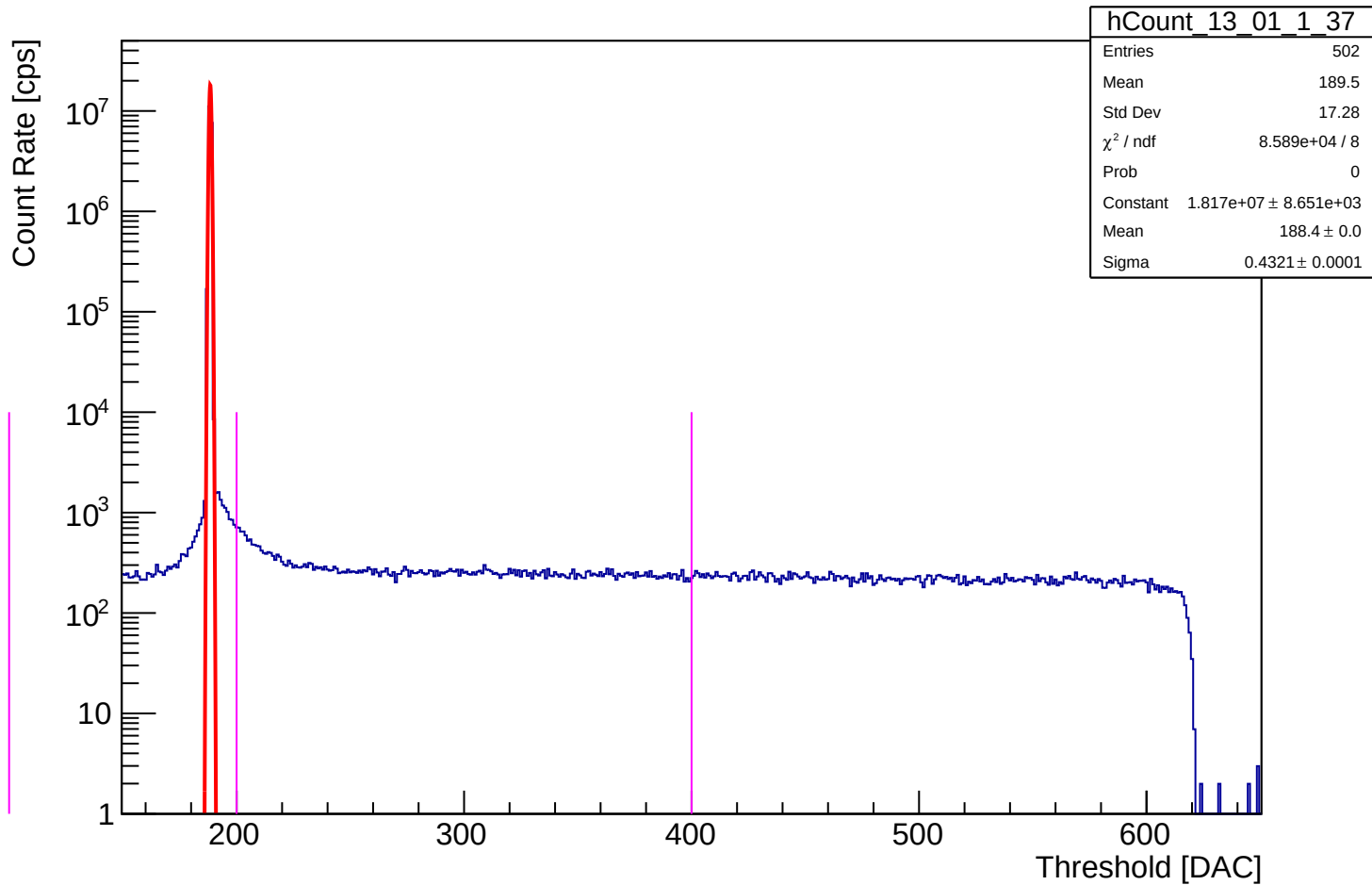
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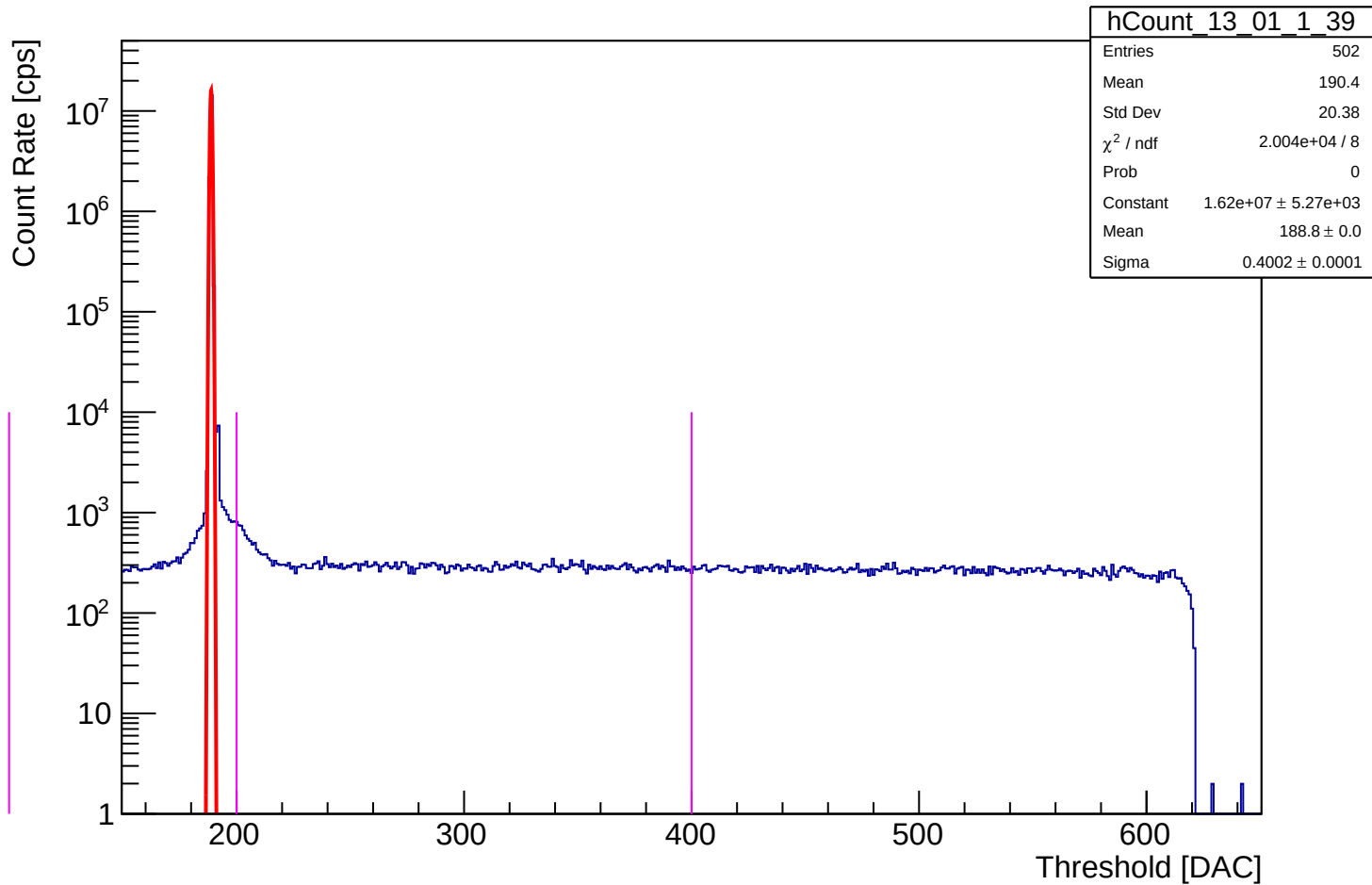
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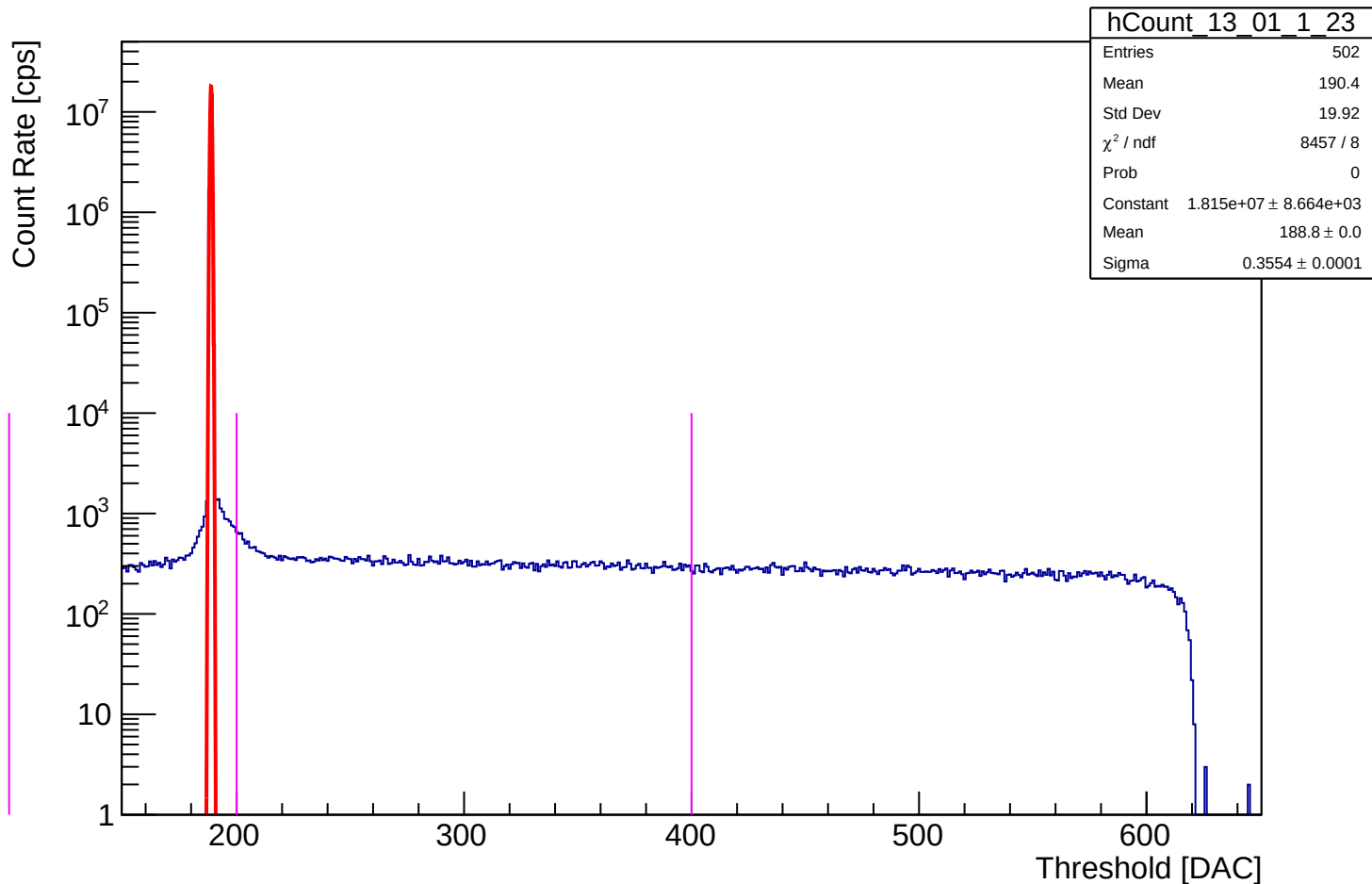
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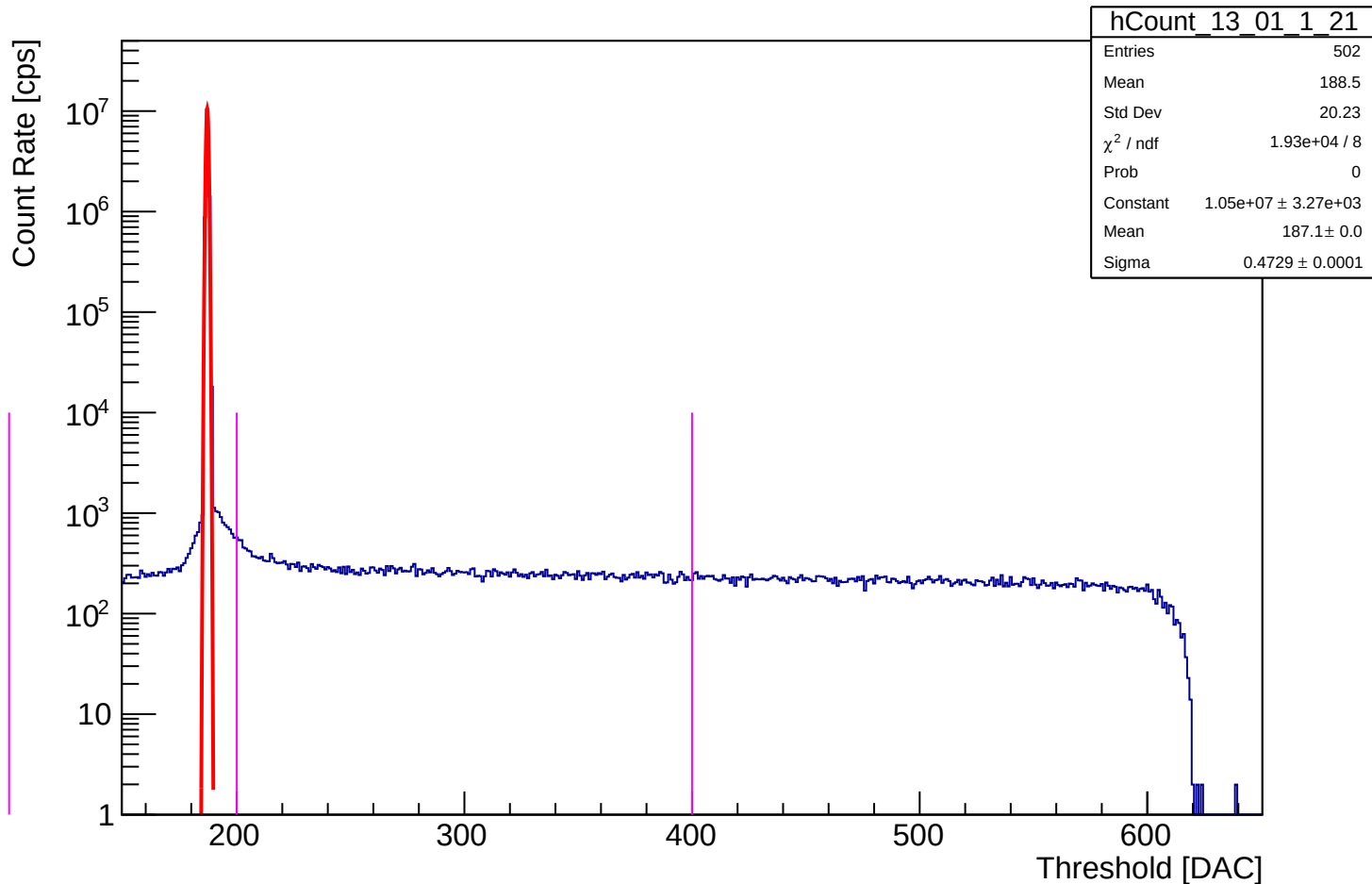
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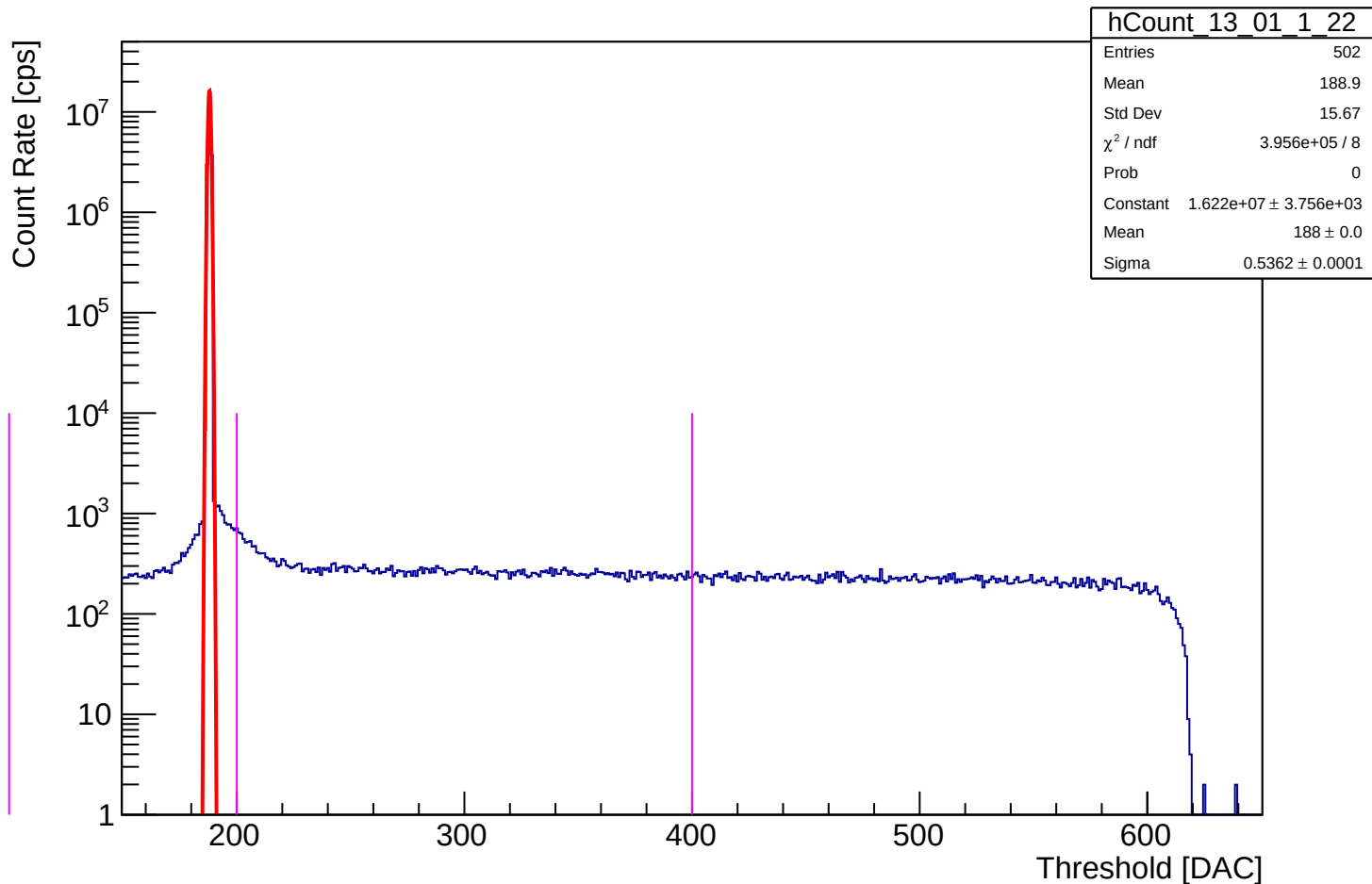
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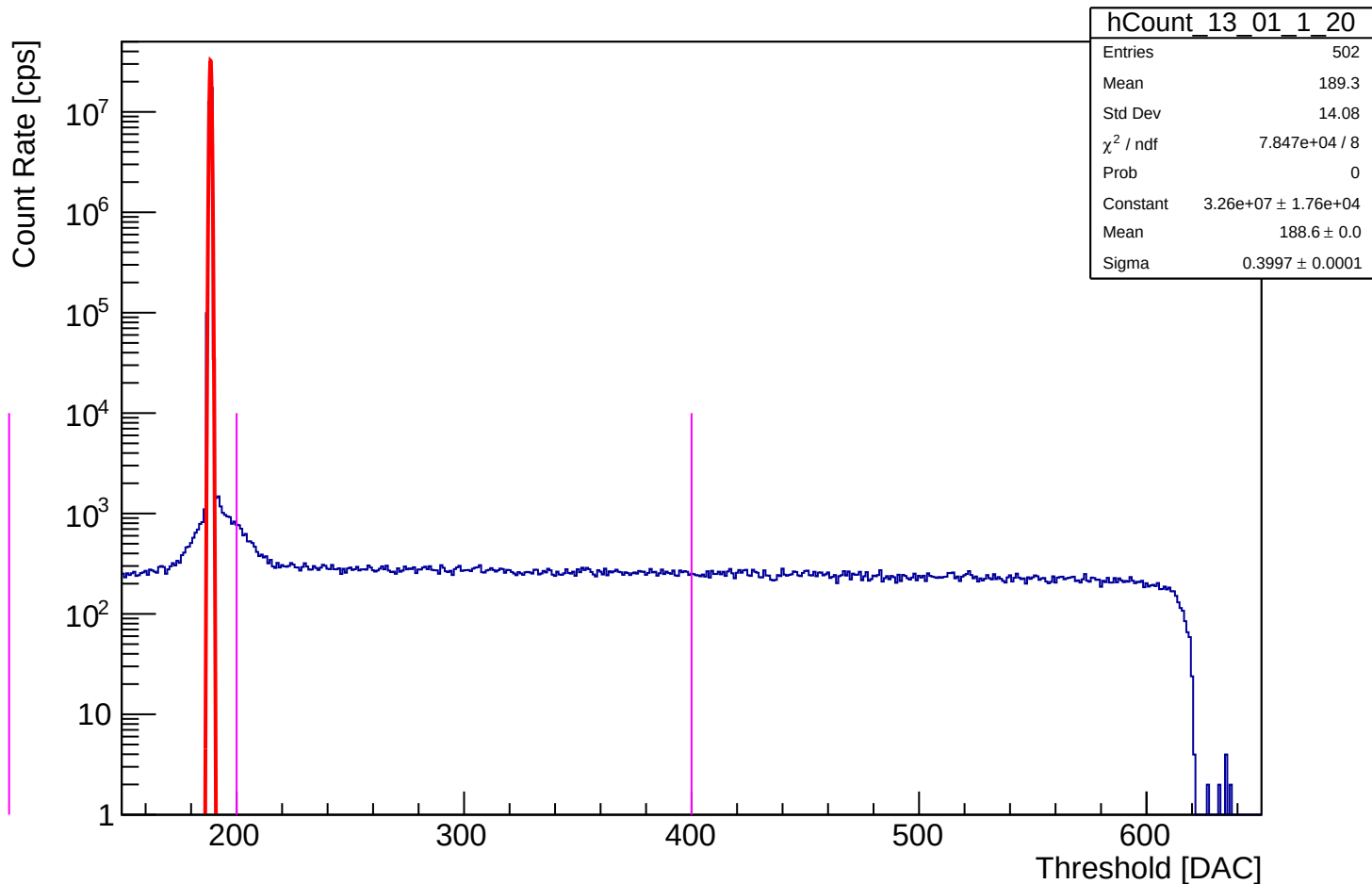
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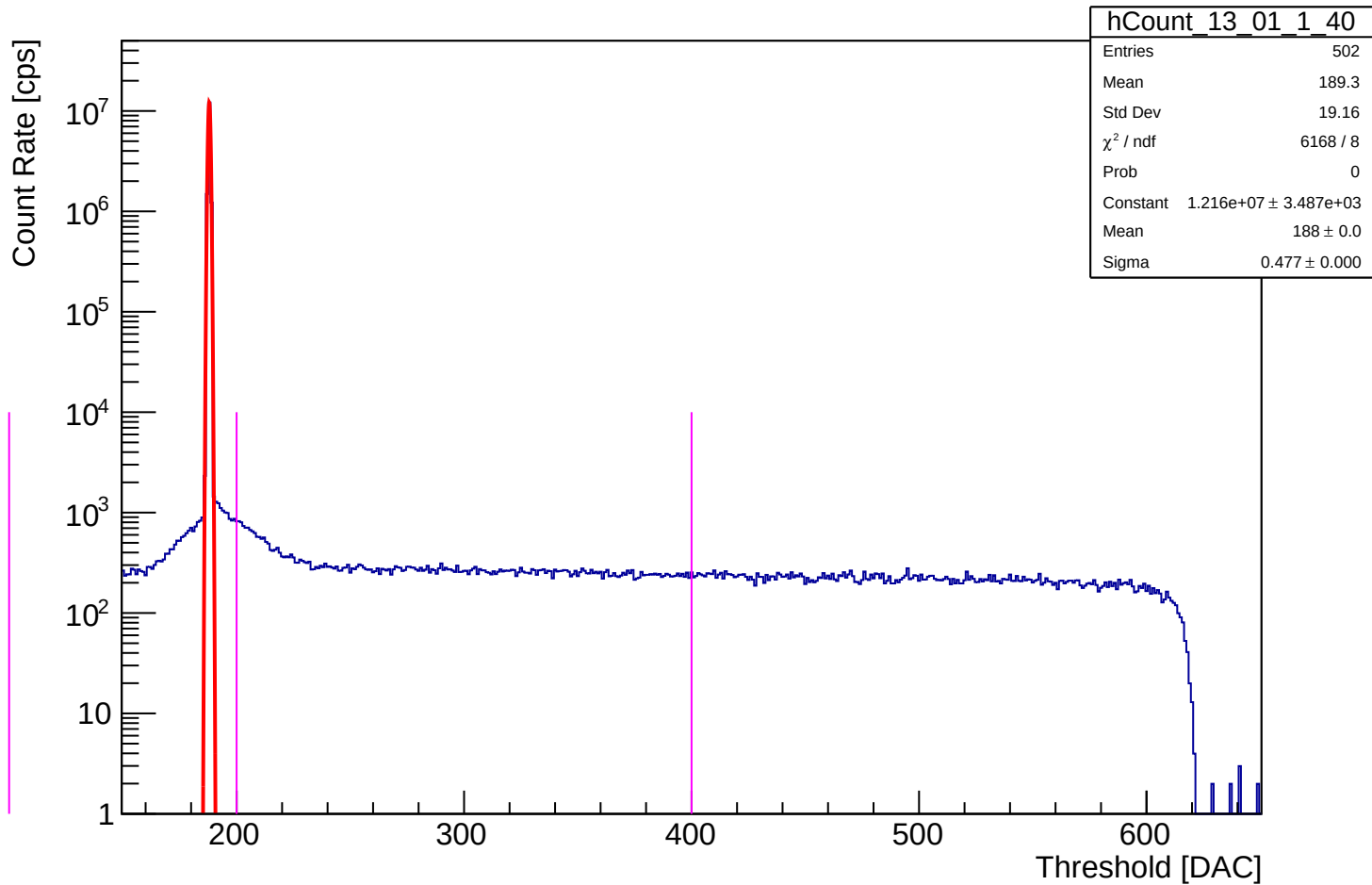
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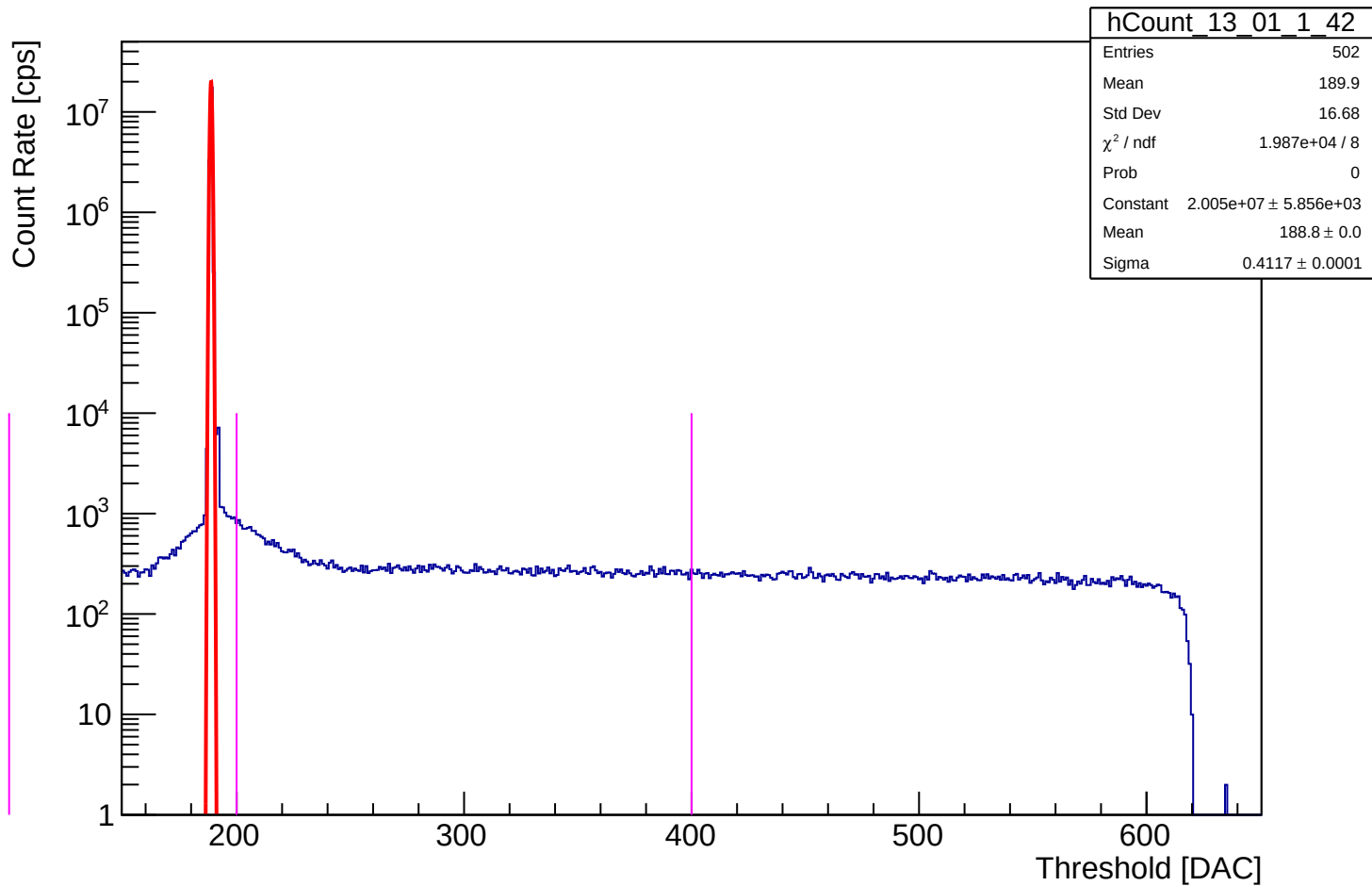
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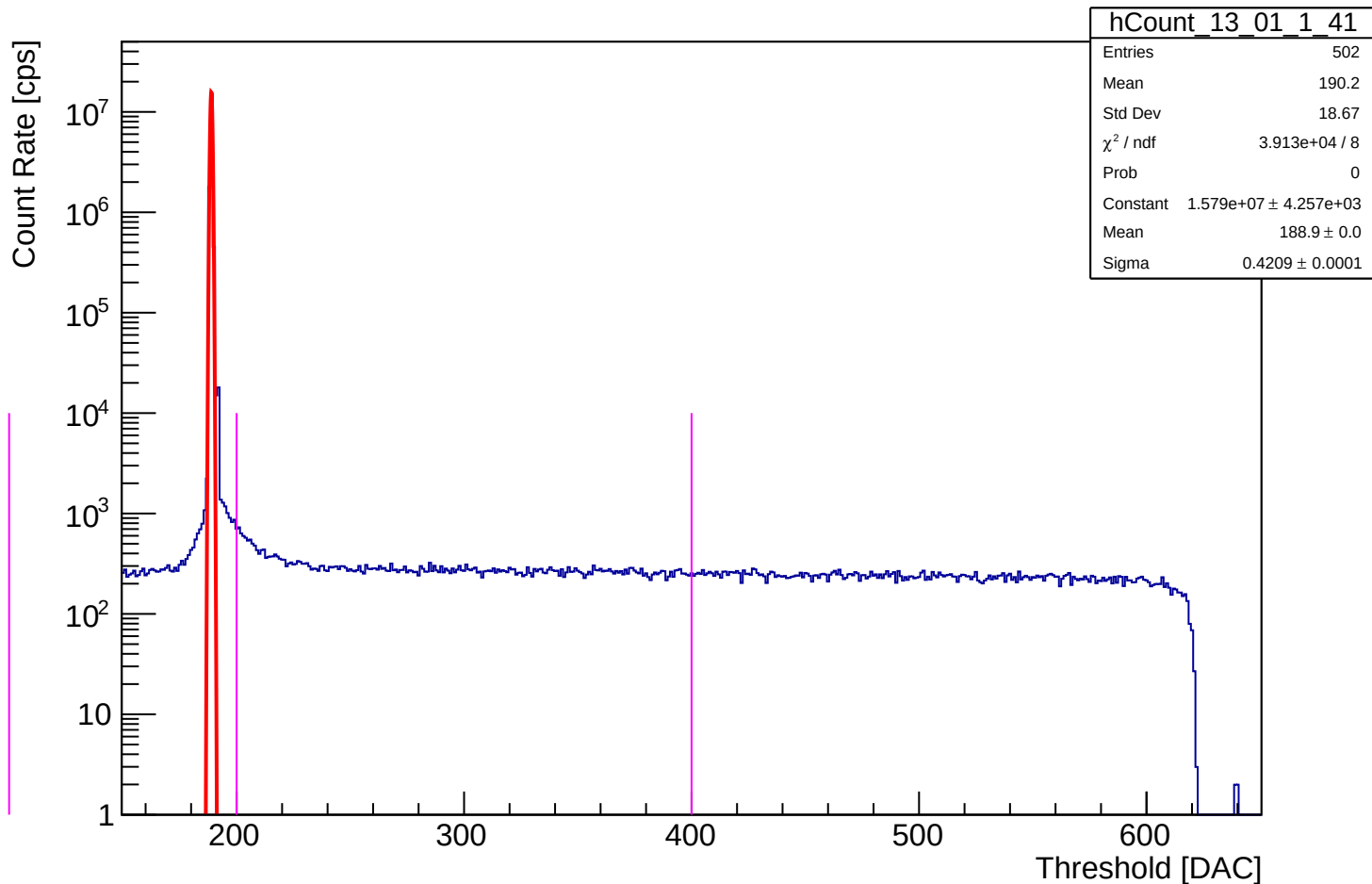
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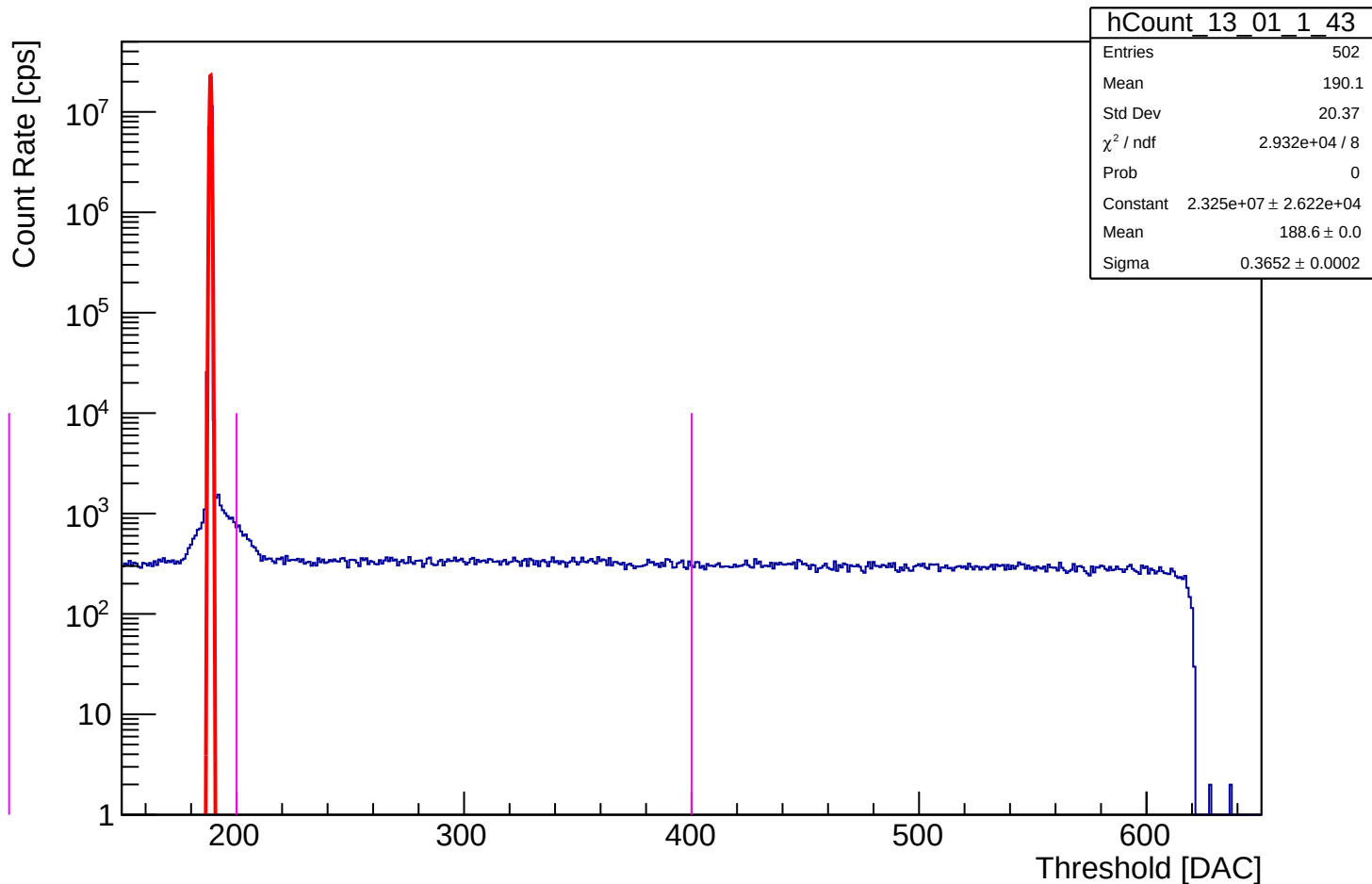
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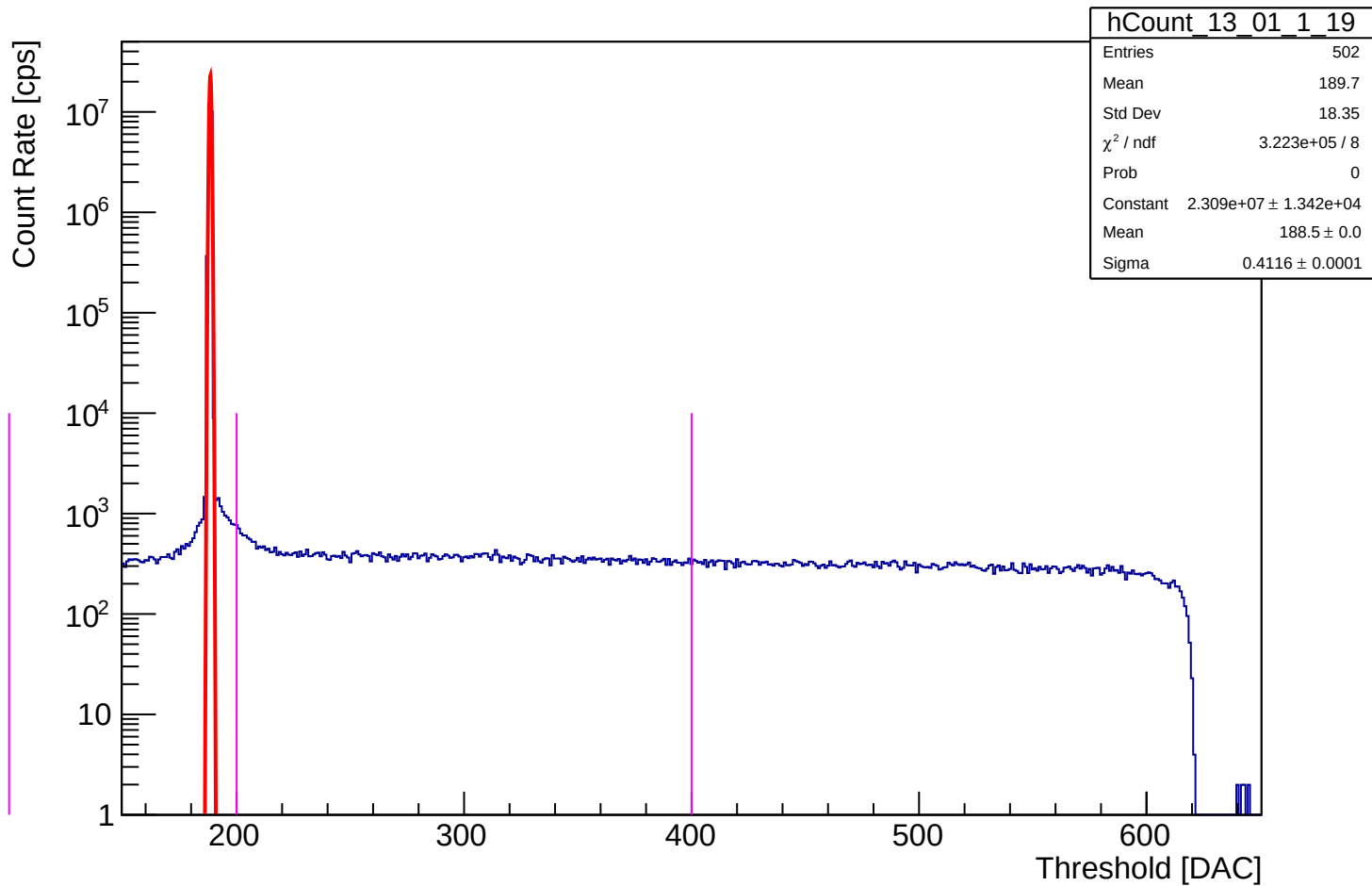
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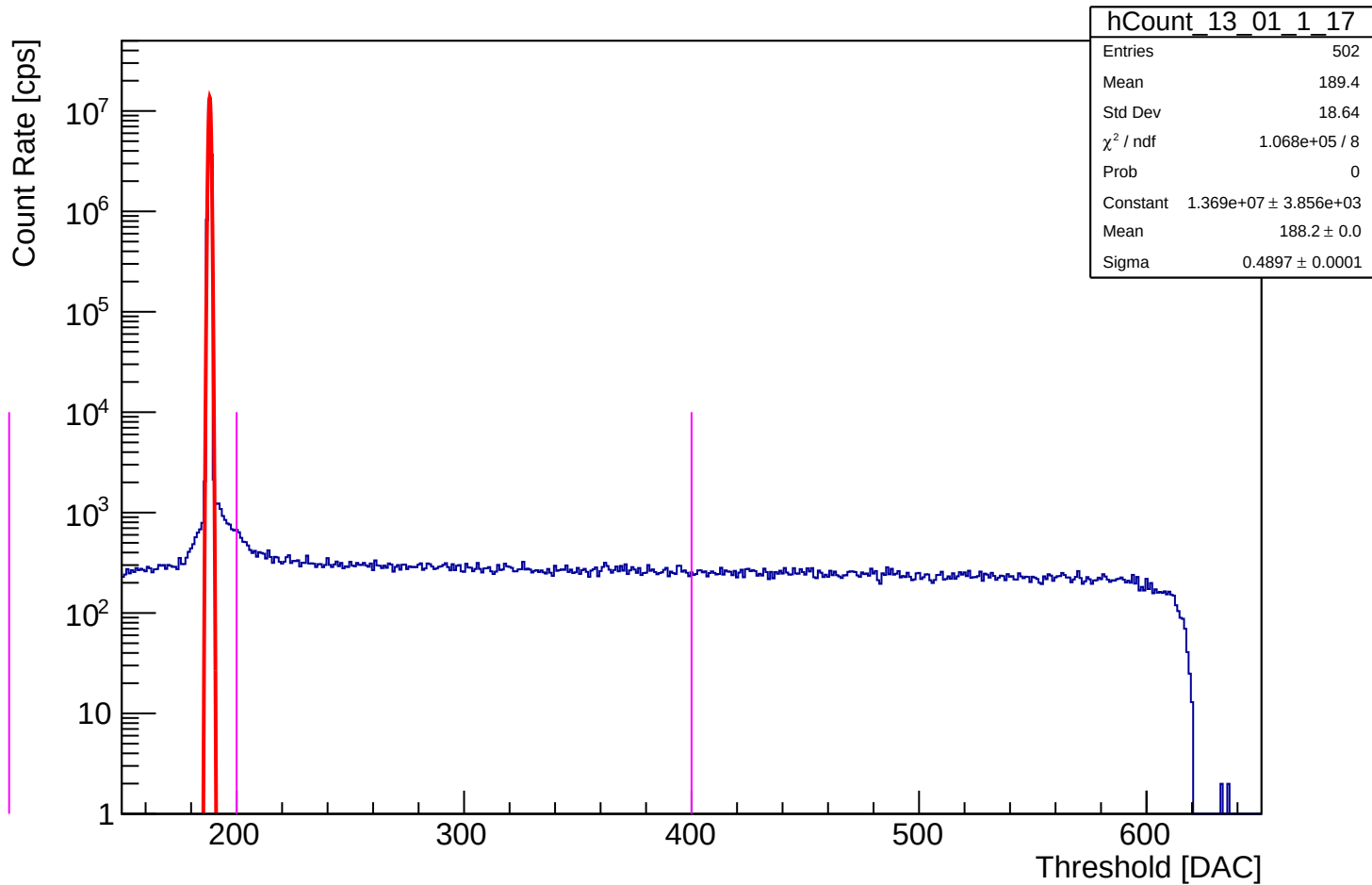
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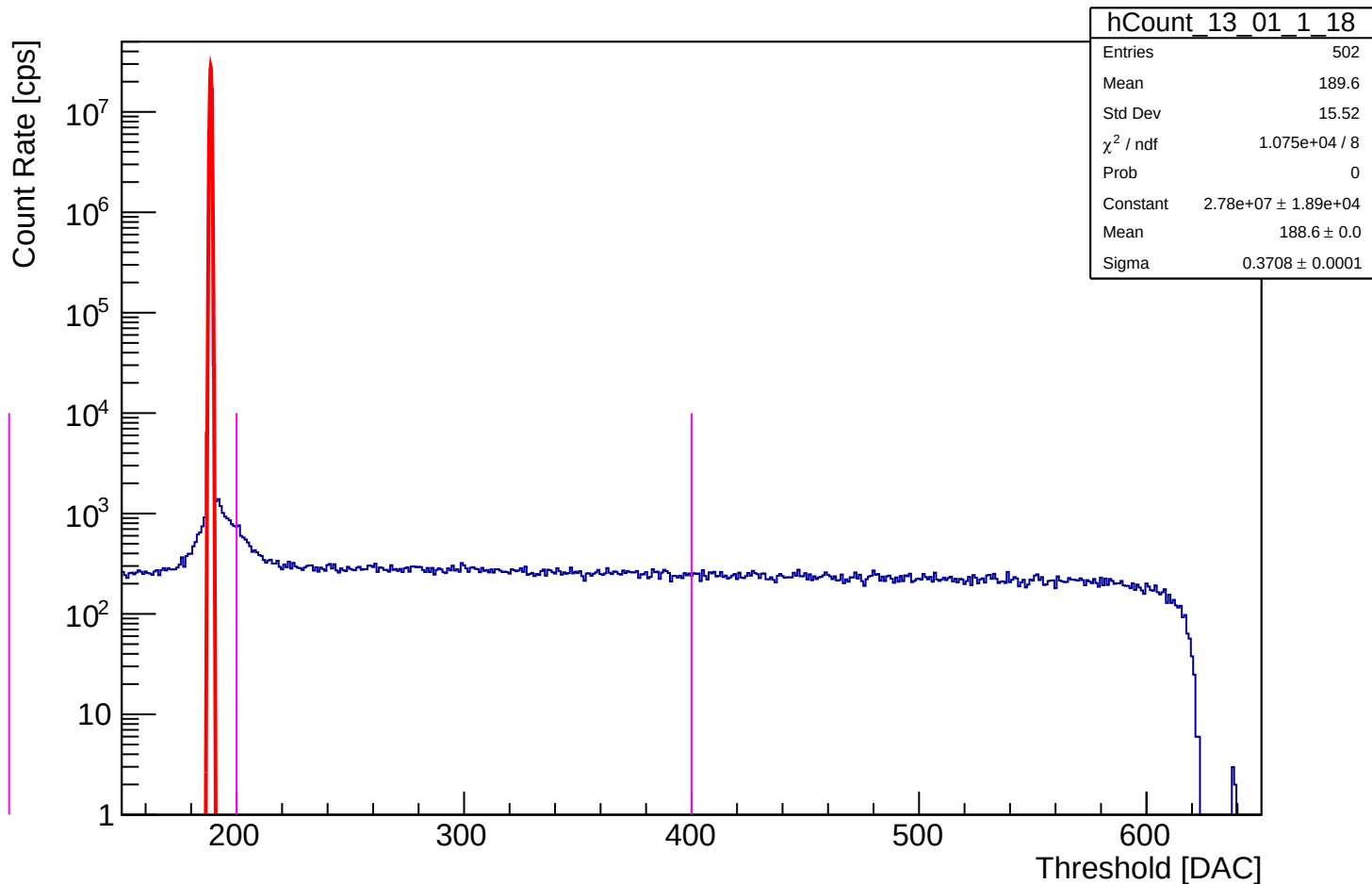
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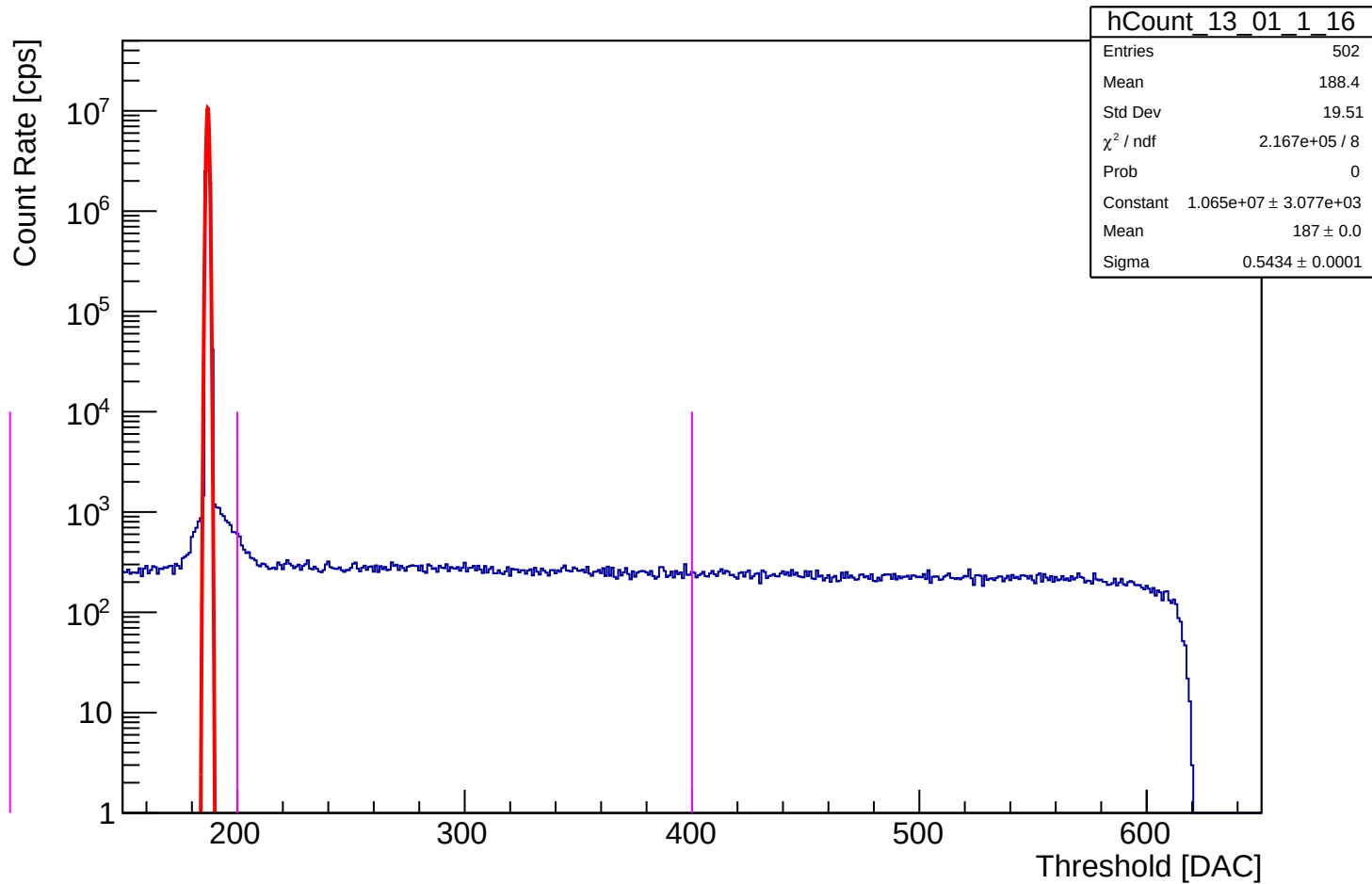
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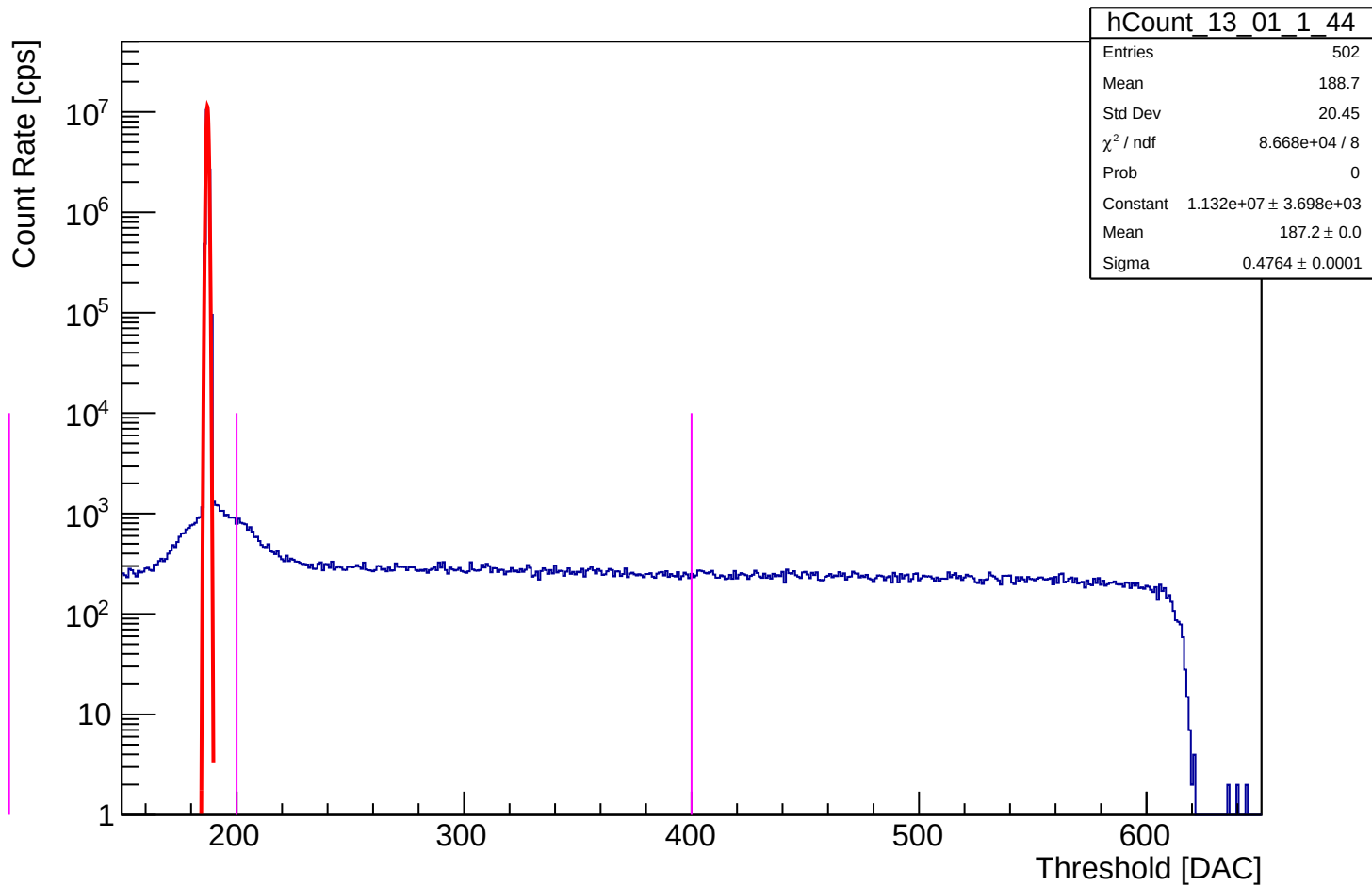
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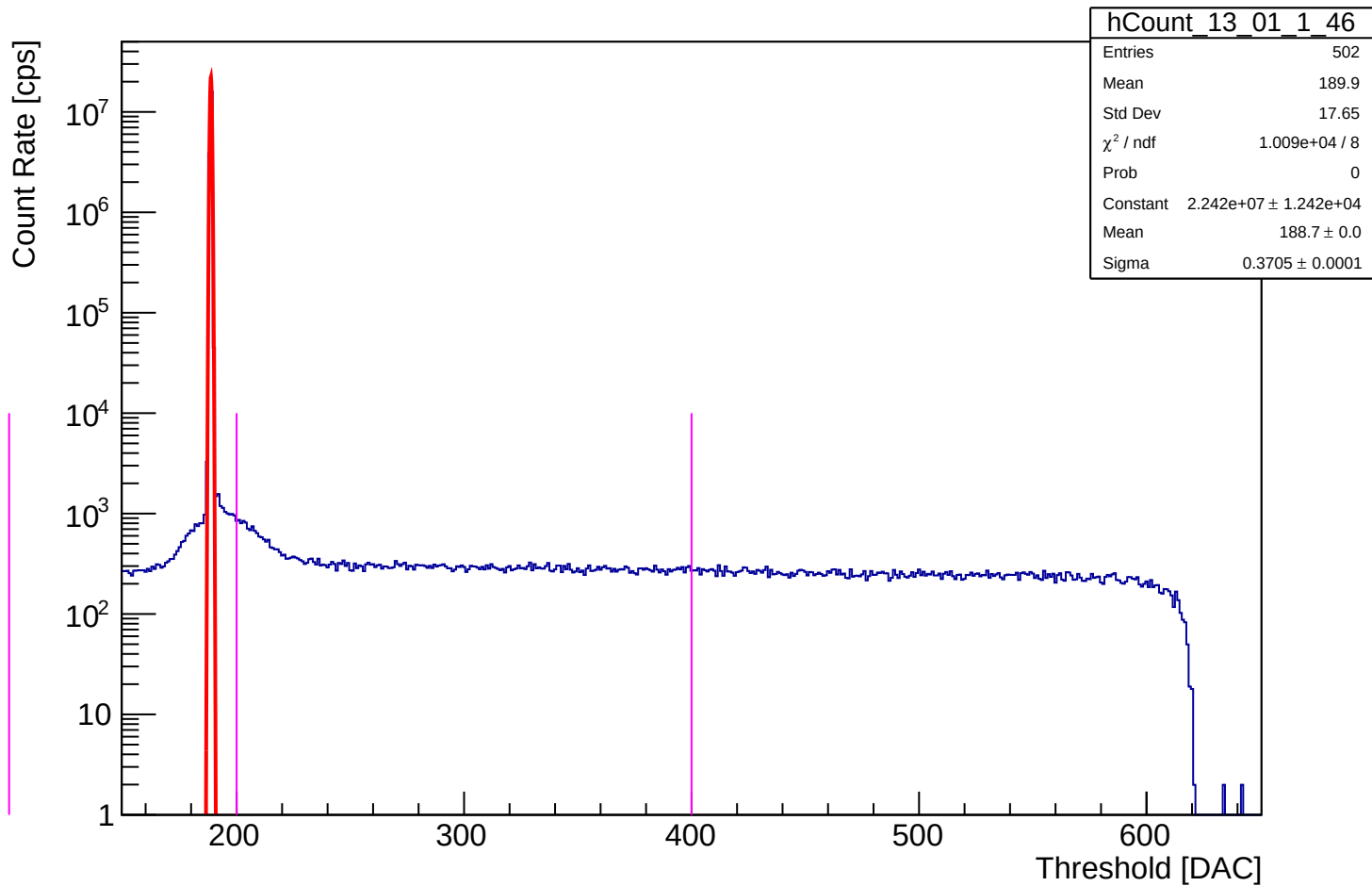
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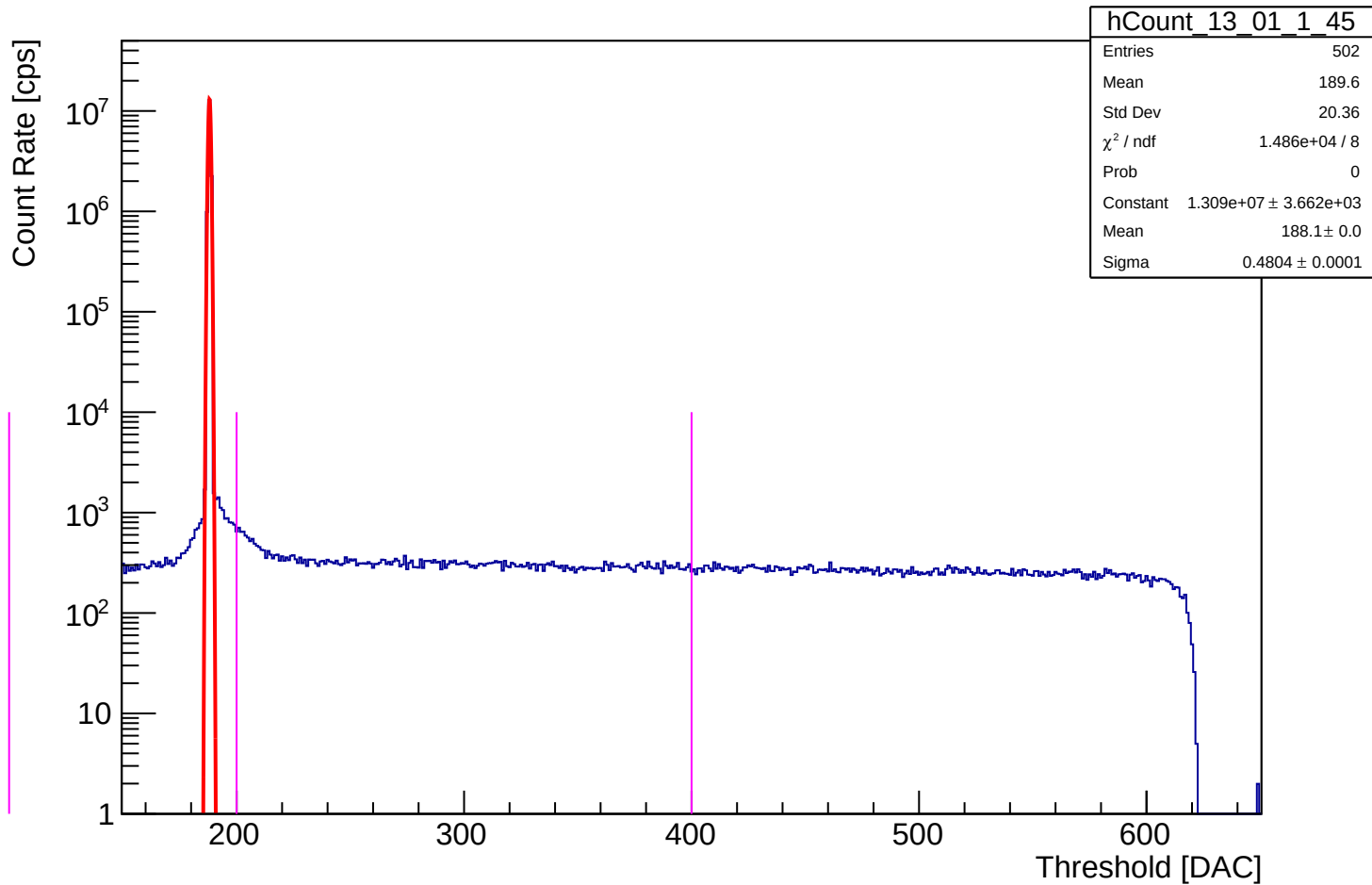
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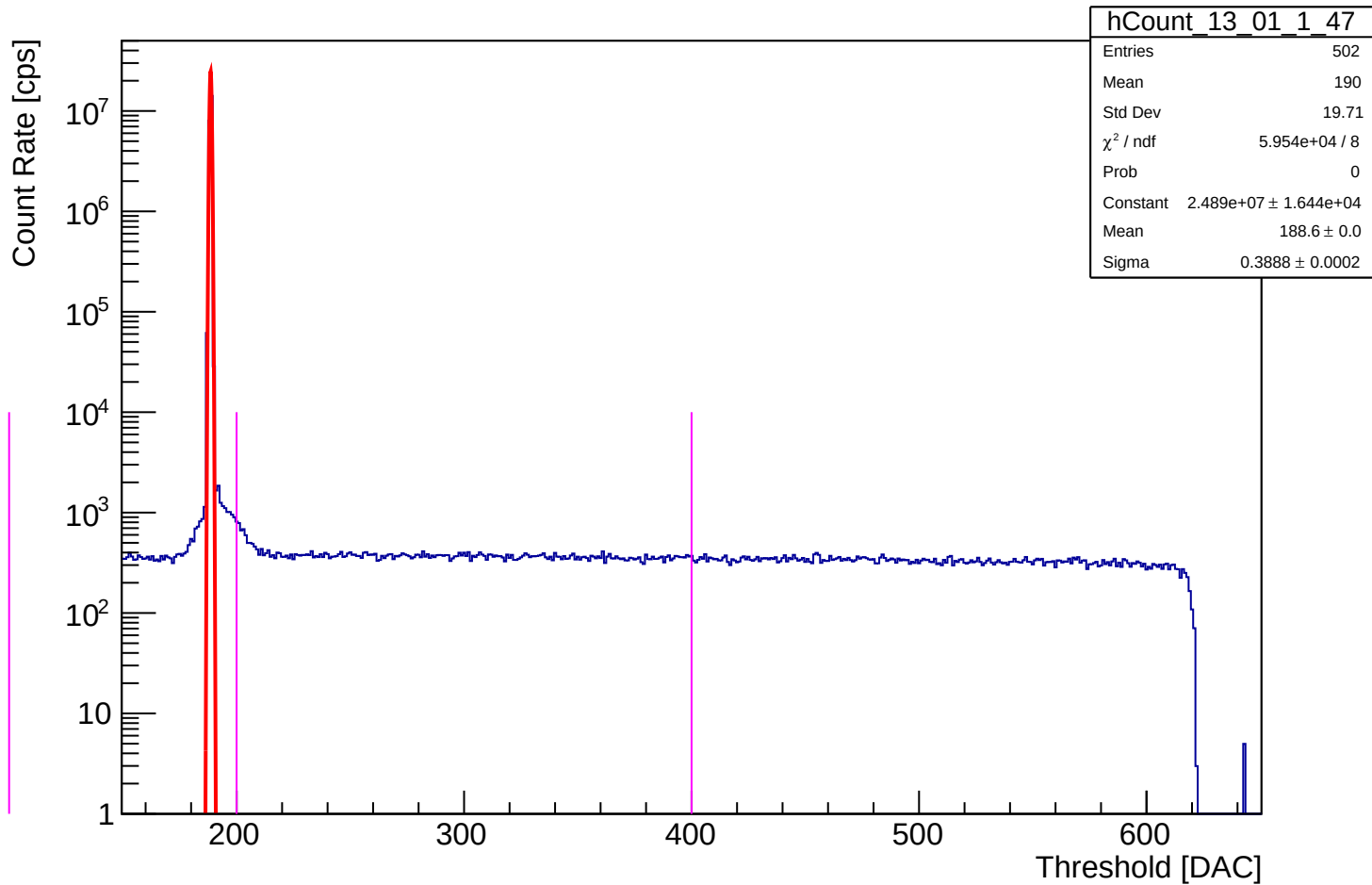
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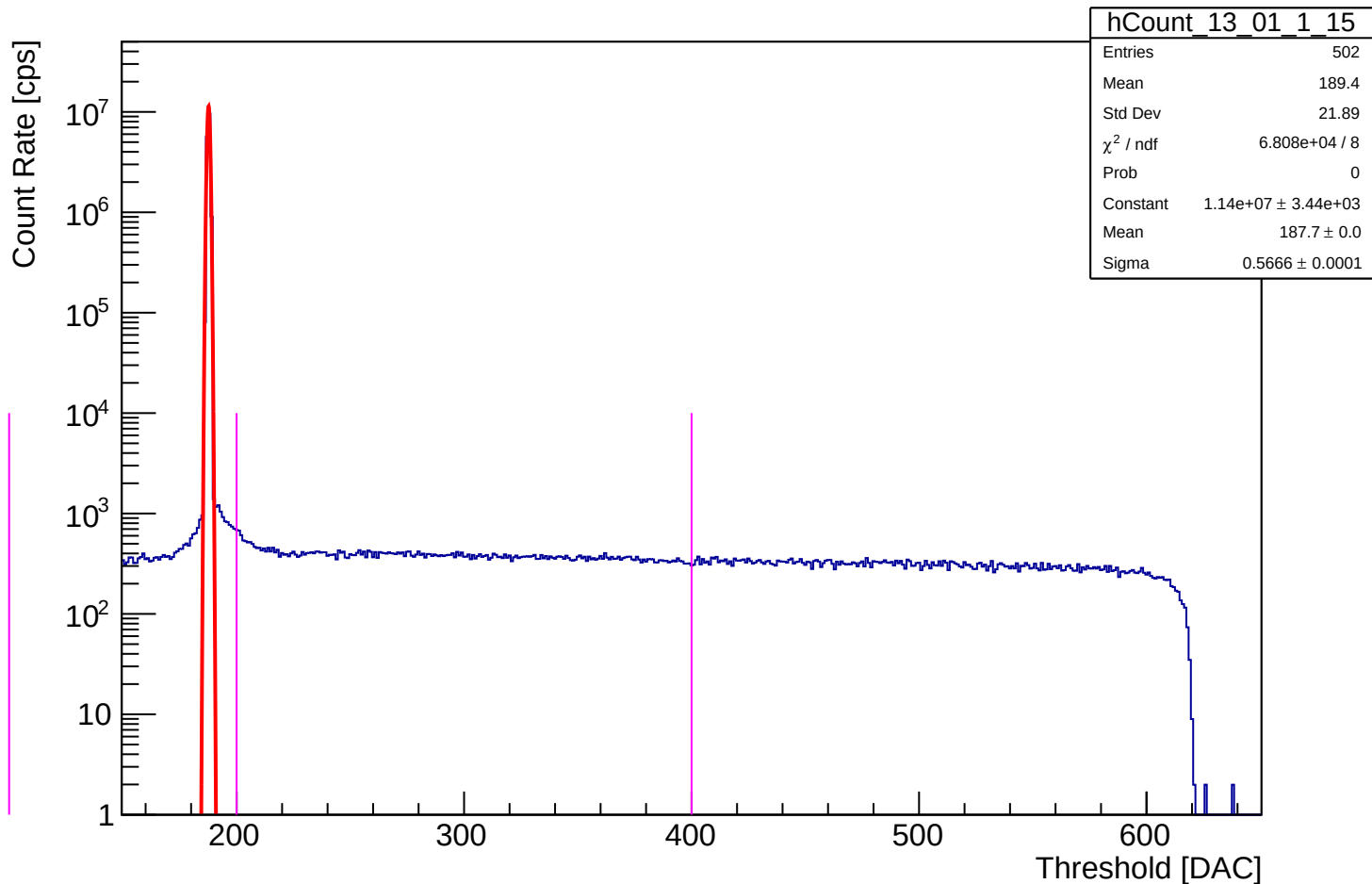
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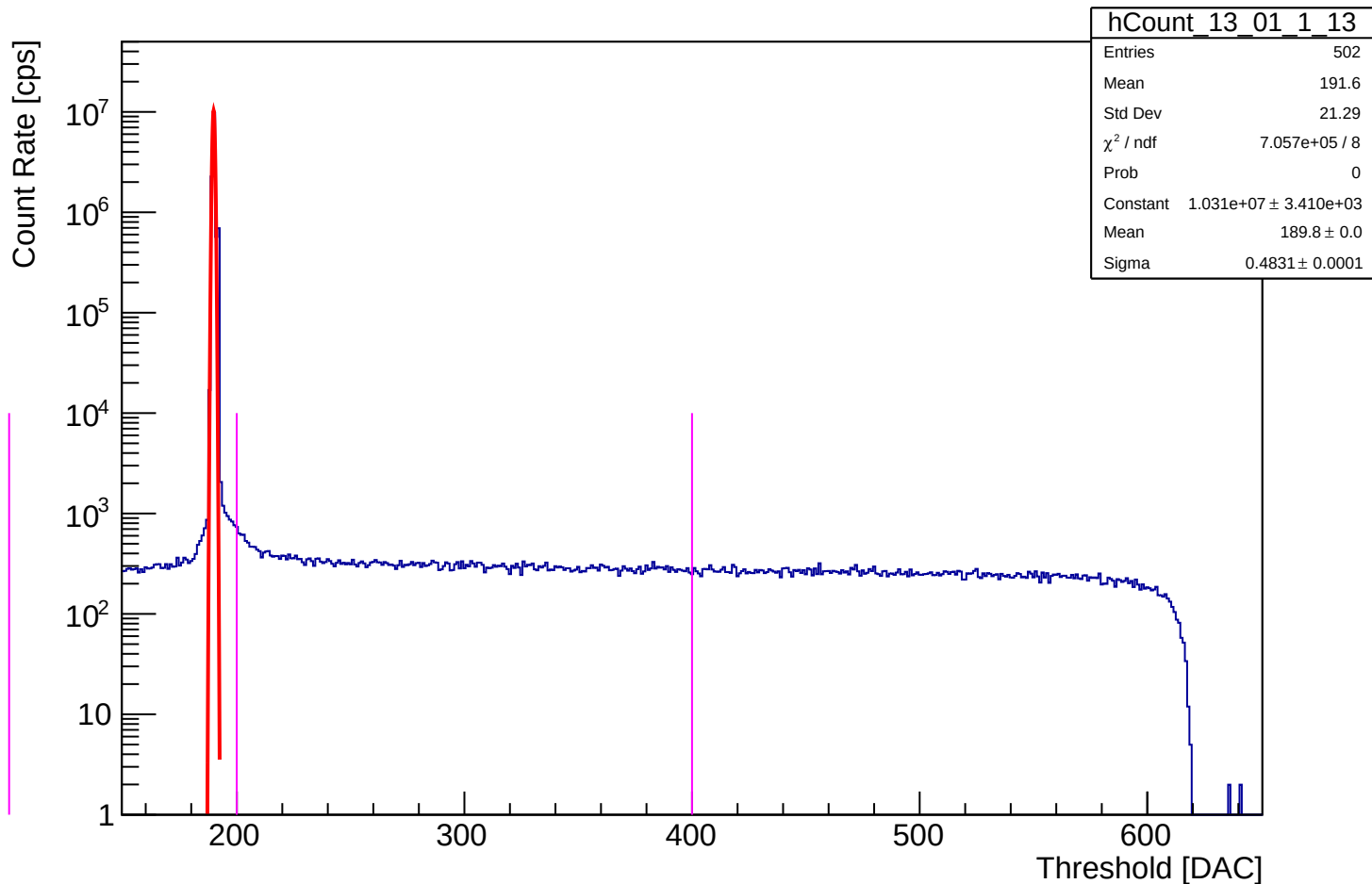
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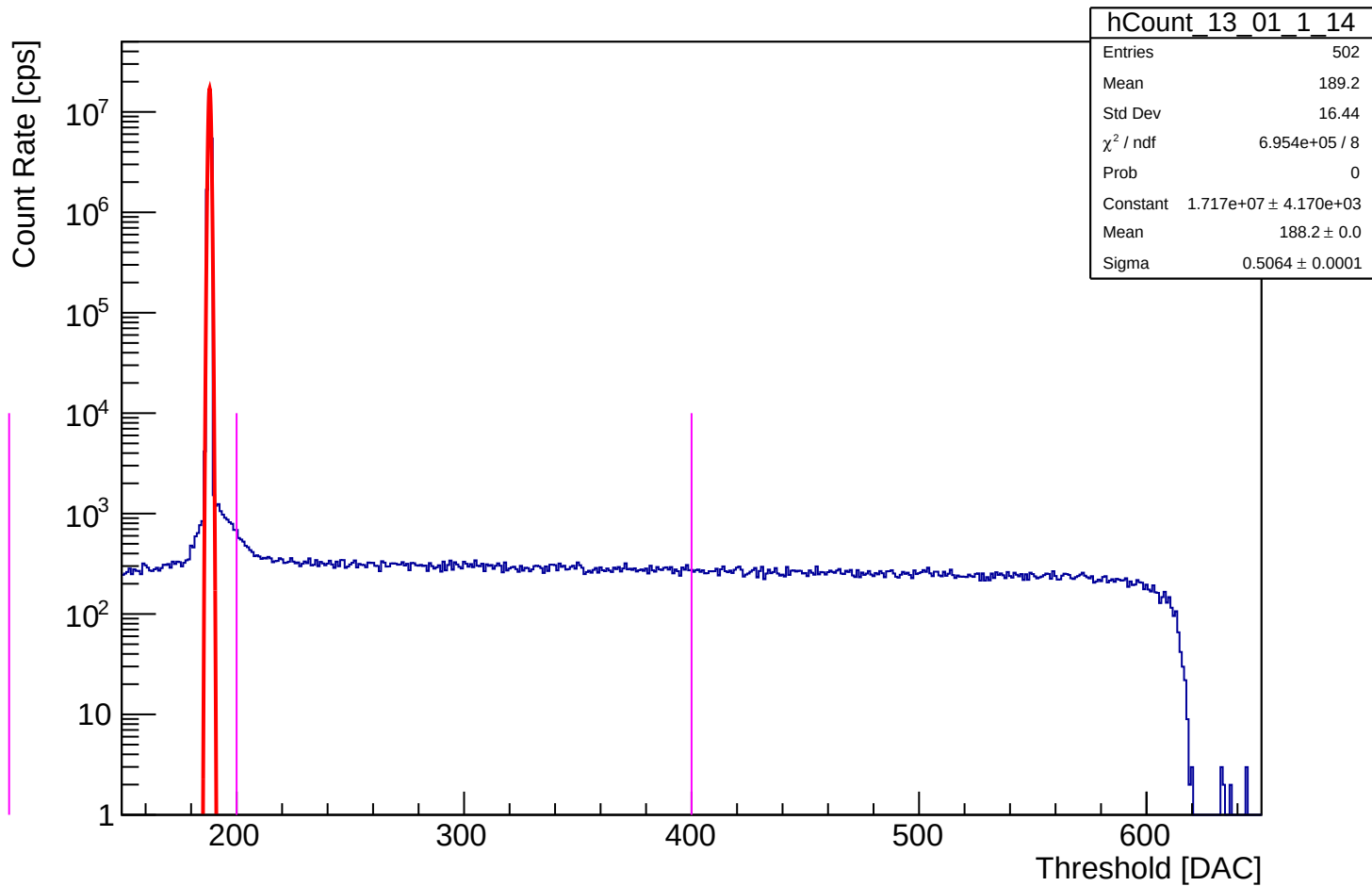
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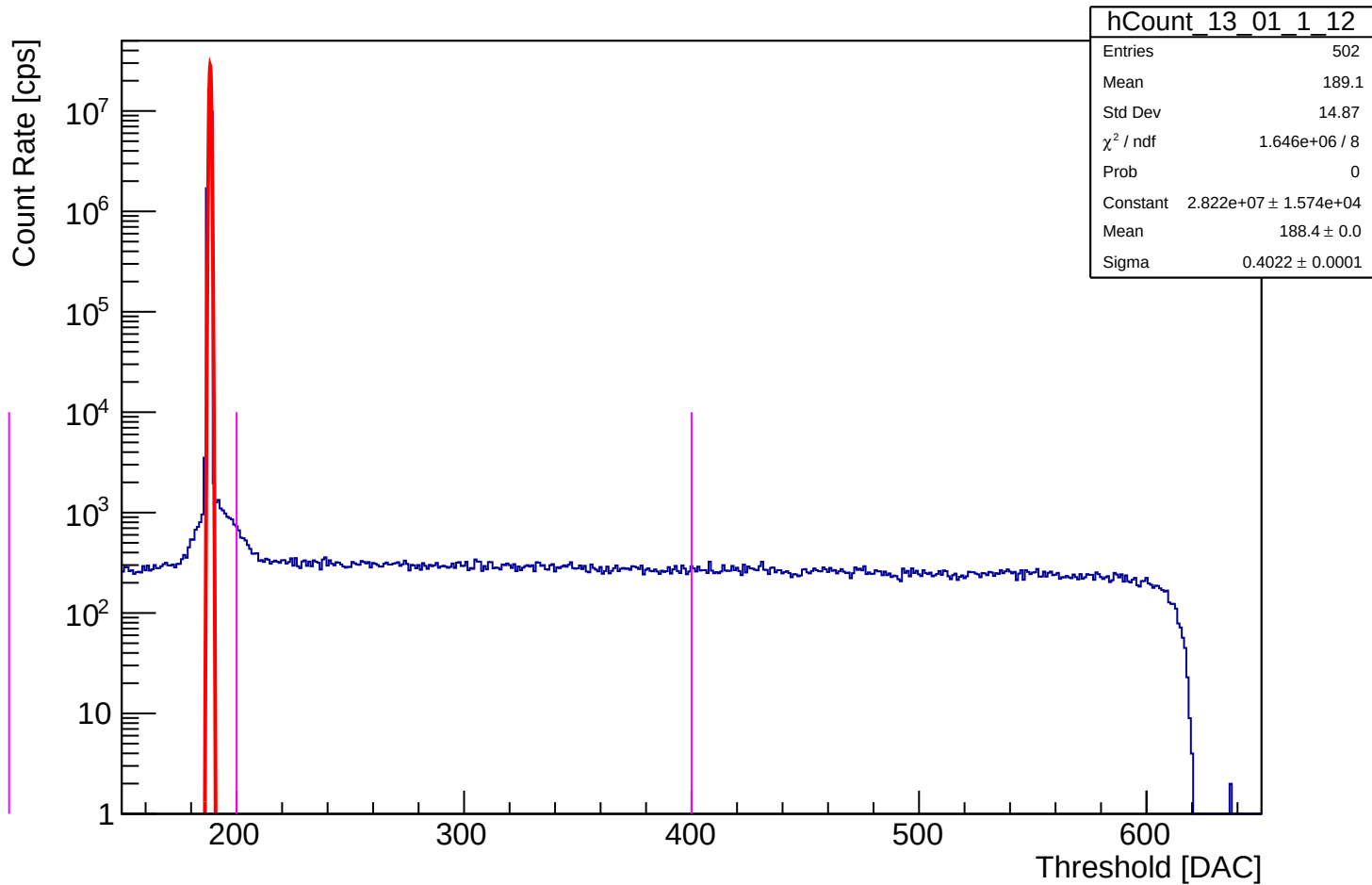
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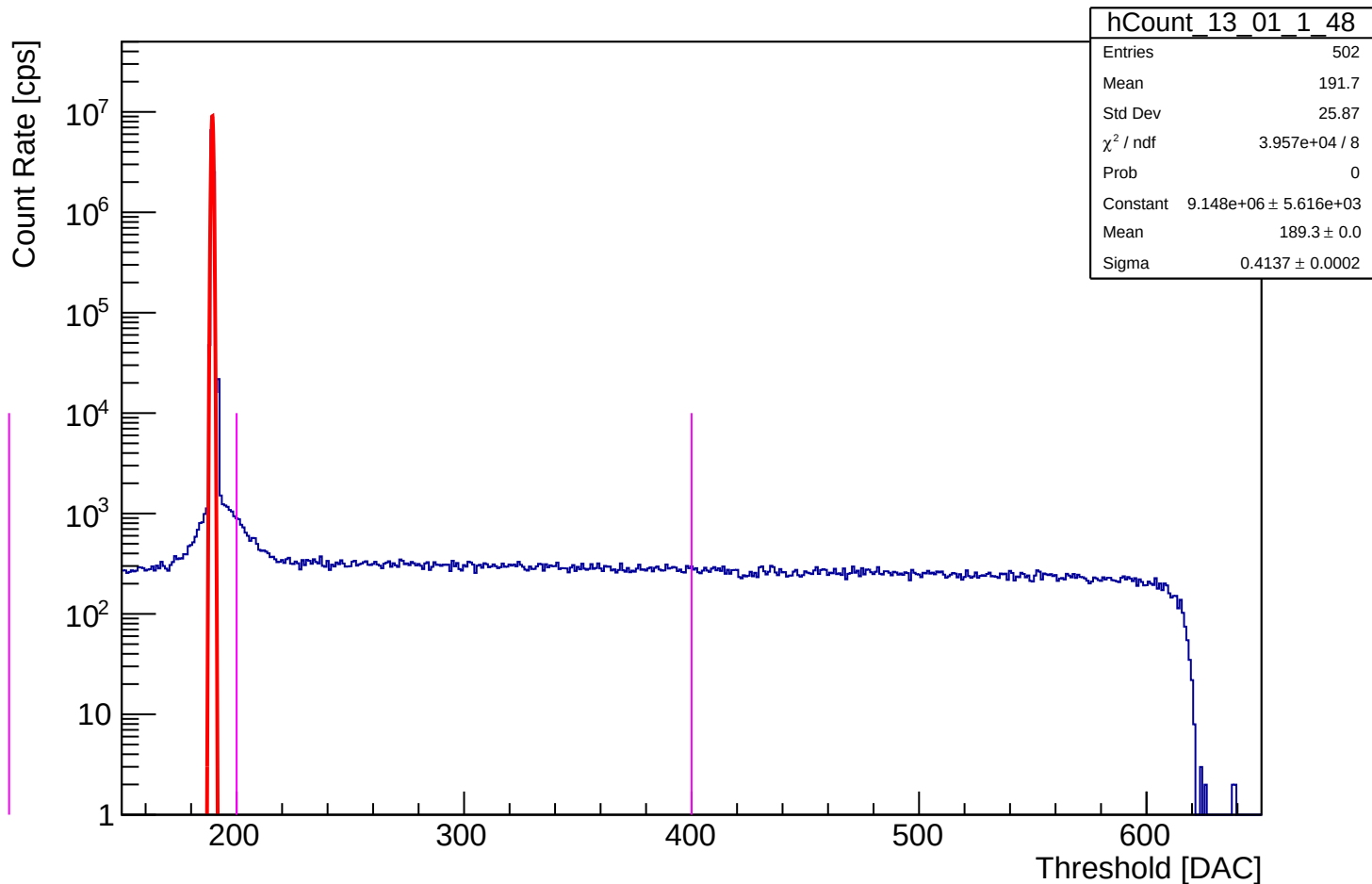
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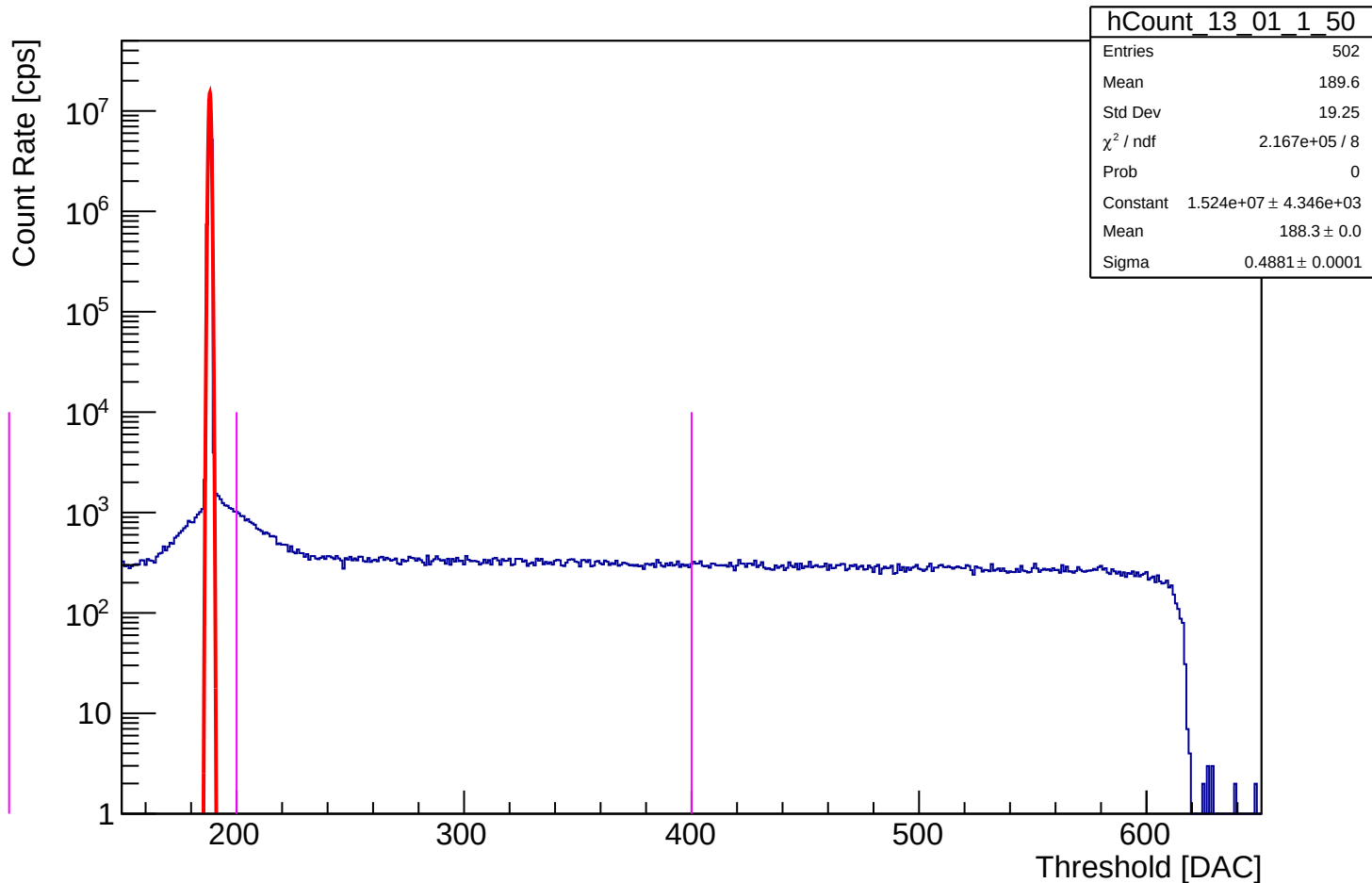
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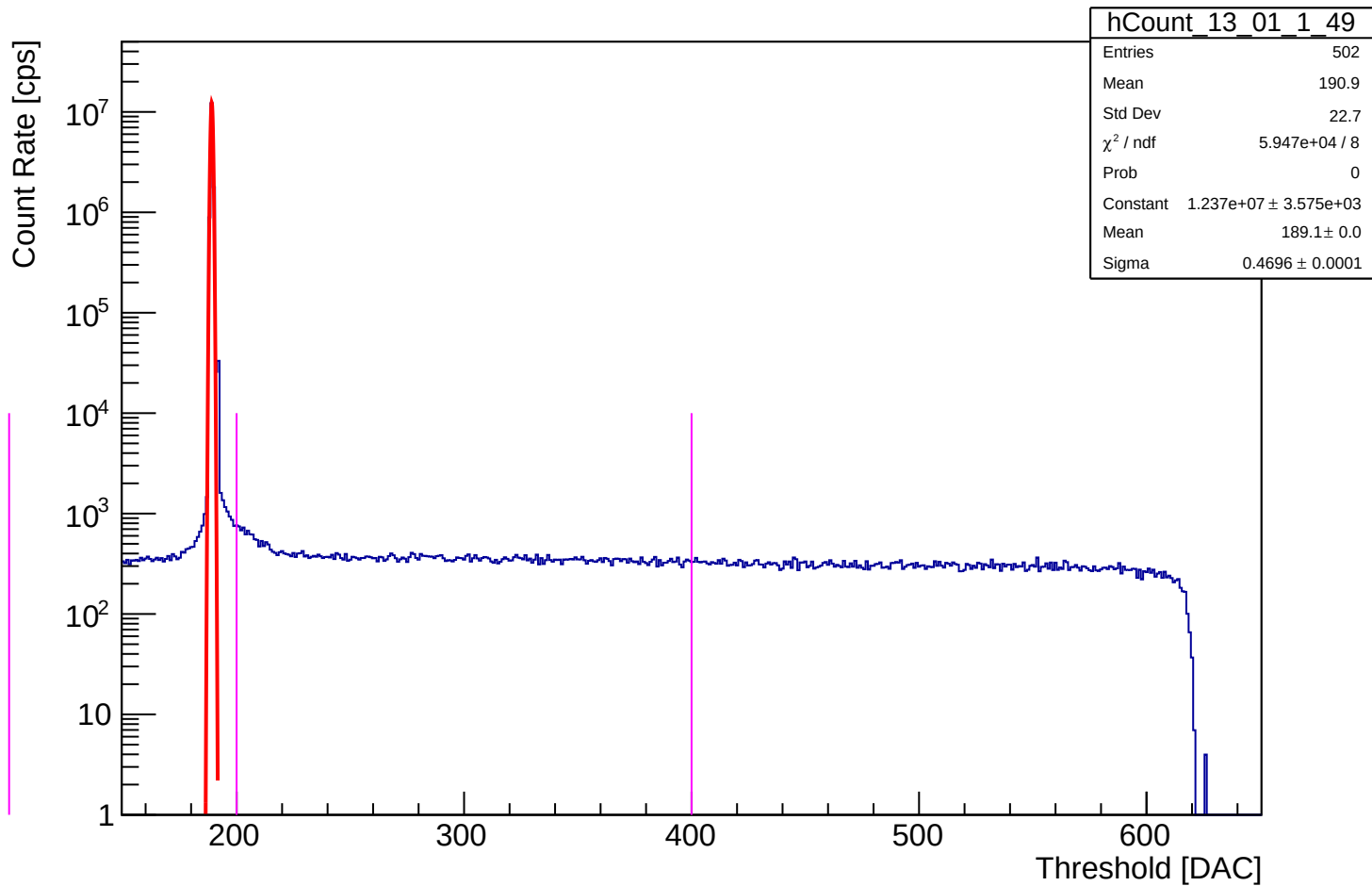
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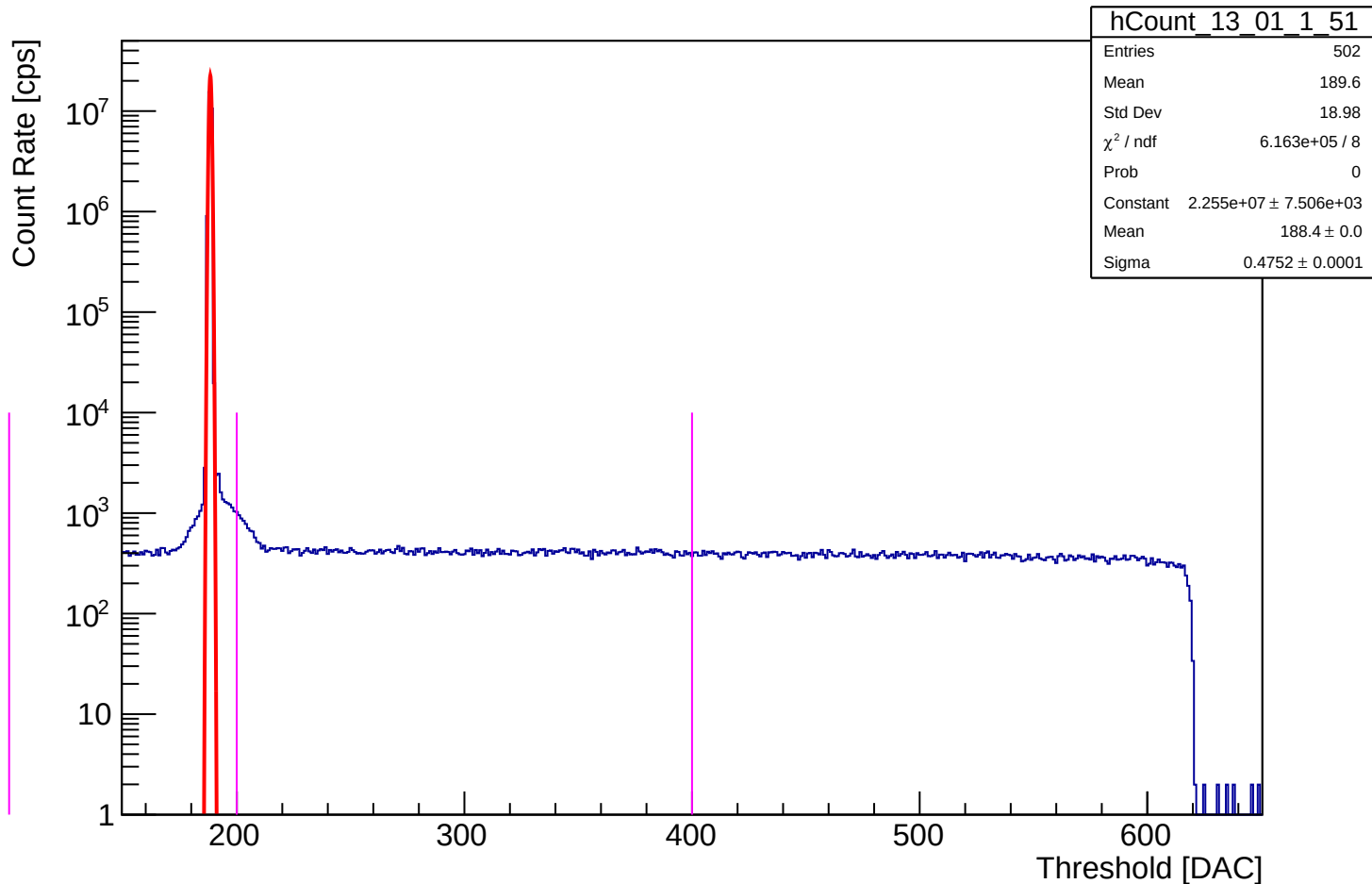
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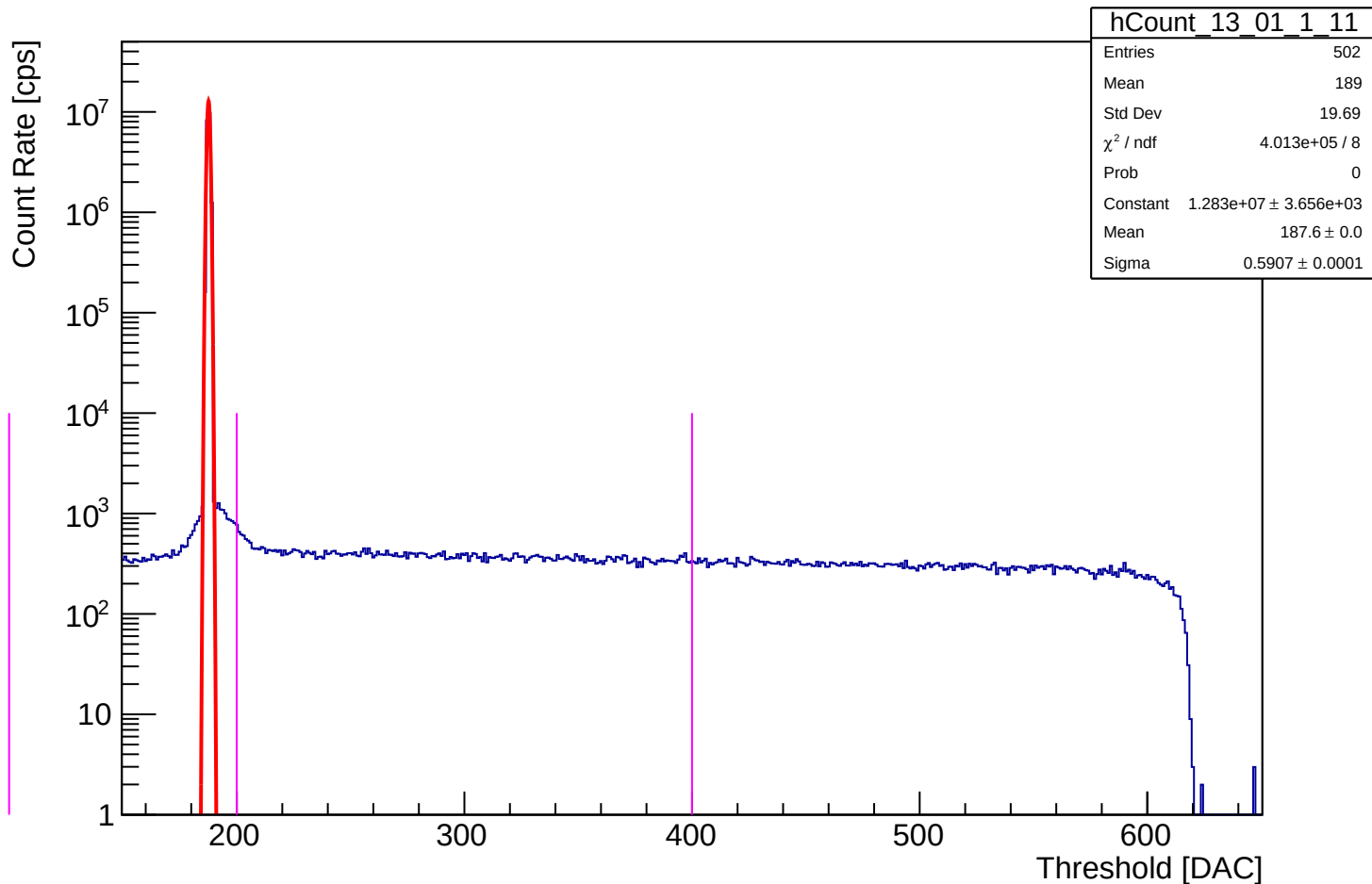
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Row 1 Tile 1 Pmt 5 Pixel 40 Slot 13 Fiber 1 Asic 1 Channel 51

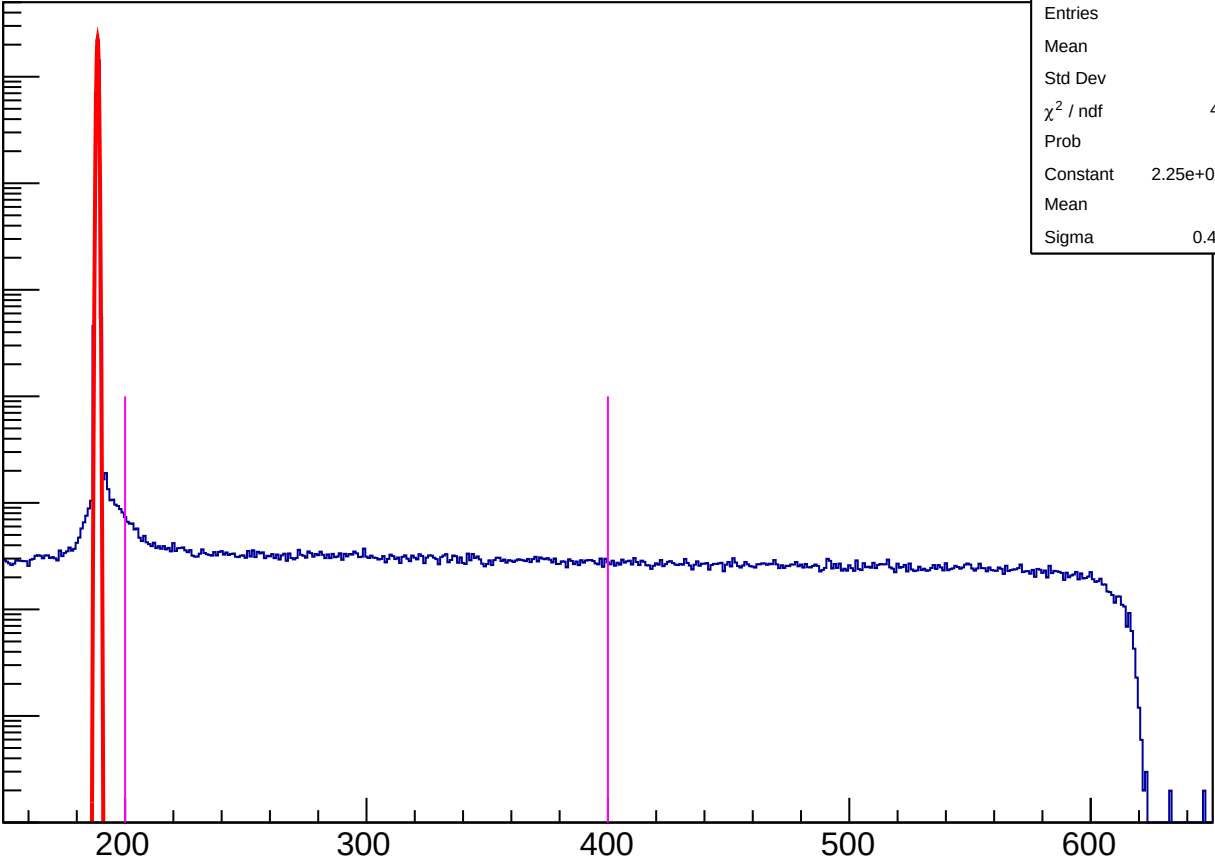


Row 1 Tile 1 Pmt 5 Pixel 41 Slot 13 Fiber 1 Asic 1 Channel 11



Count Rate [cps]

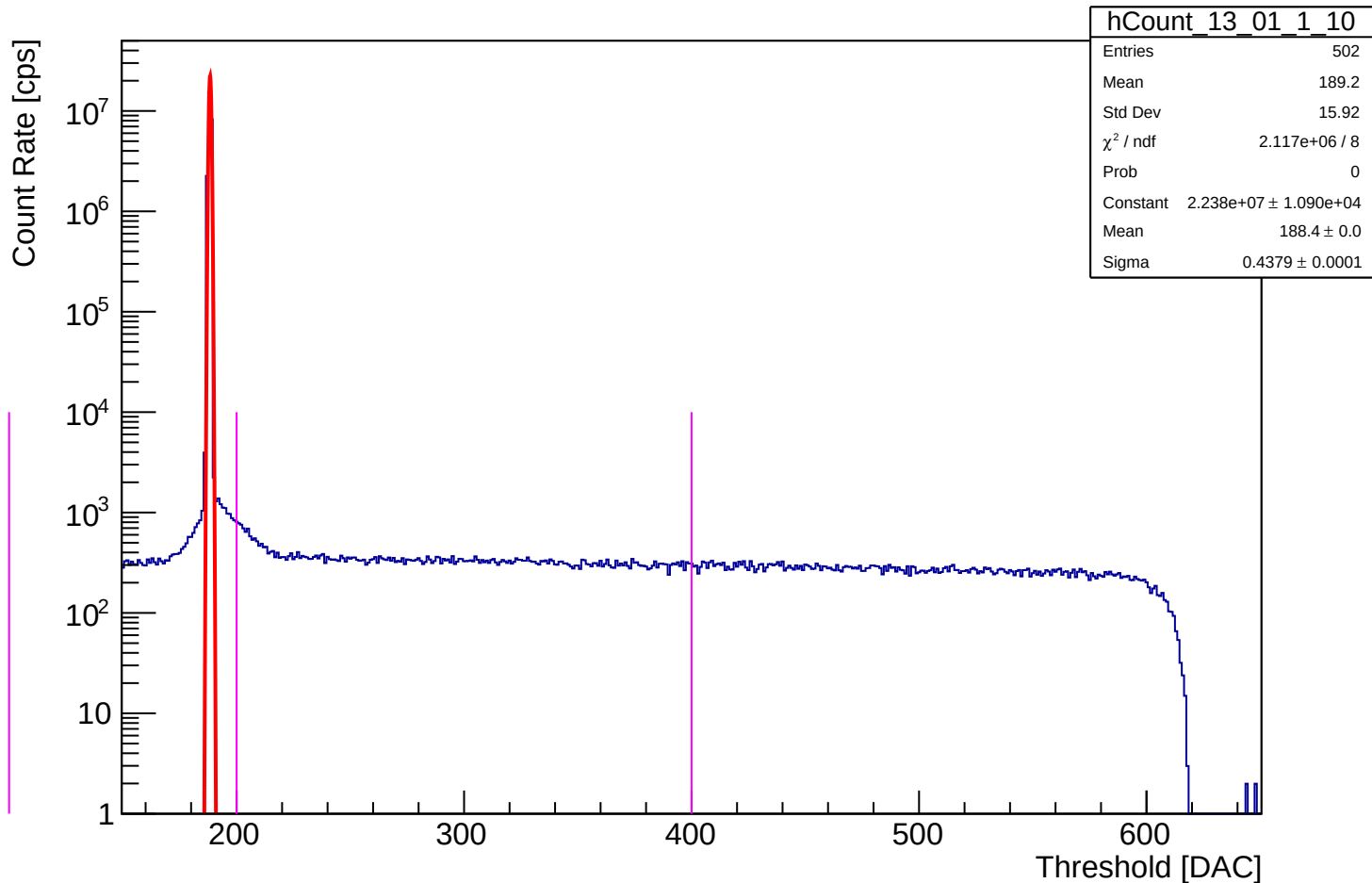
10⁷
10⁶
10⁵
10⁴
10³
10²
10
1

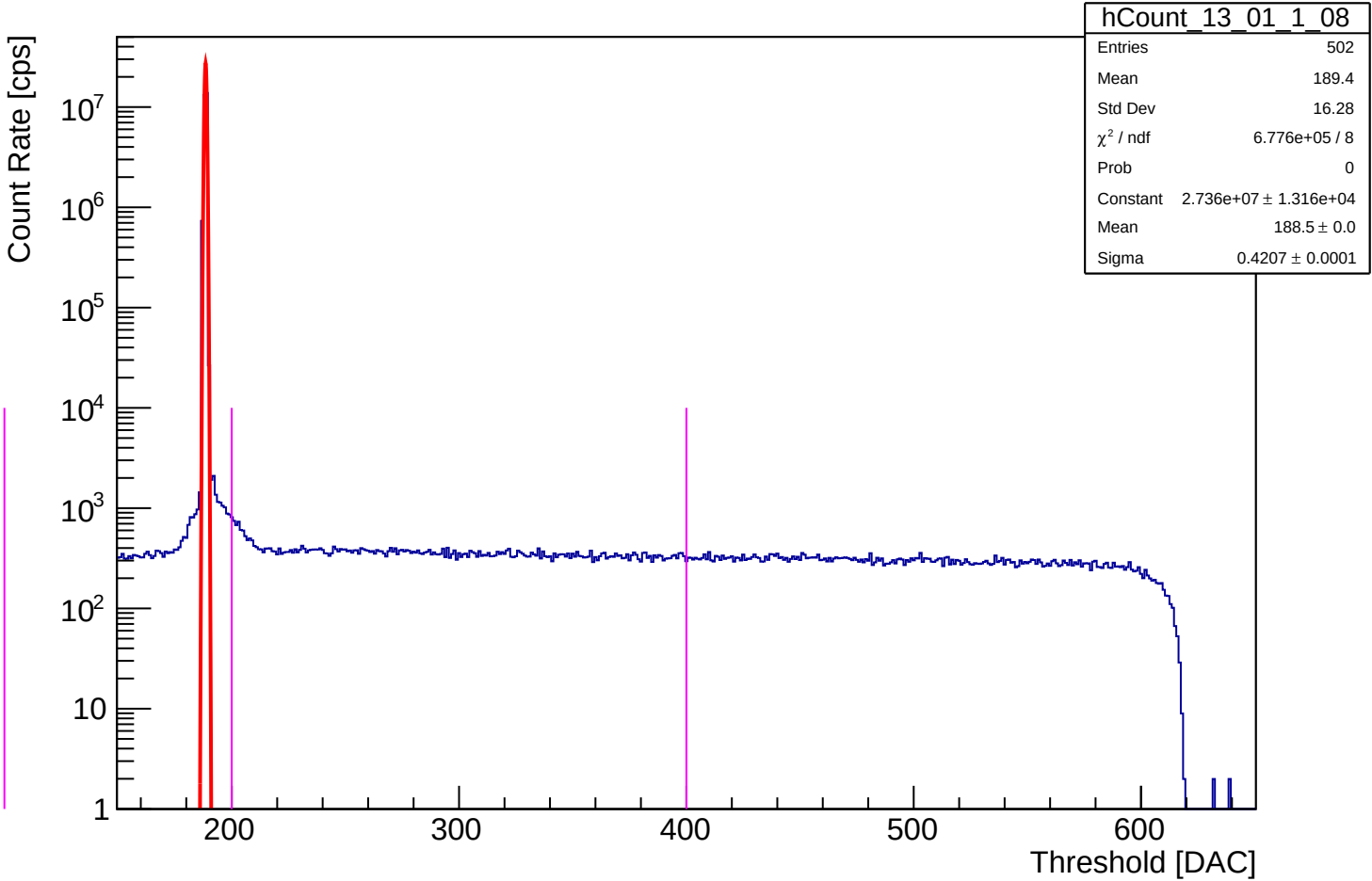


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Std Dev	17.12
χ^2 / ndf	4.225e+04 / 8
Prob	0
Constant	$2.25\text{e}+07 \pm 1.17\text{e}+04$
Mean	188.6 ± 0.0
Sigma	0.4022 ± 0.0001

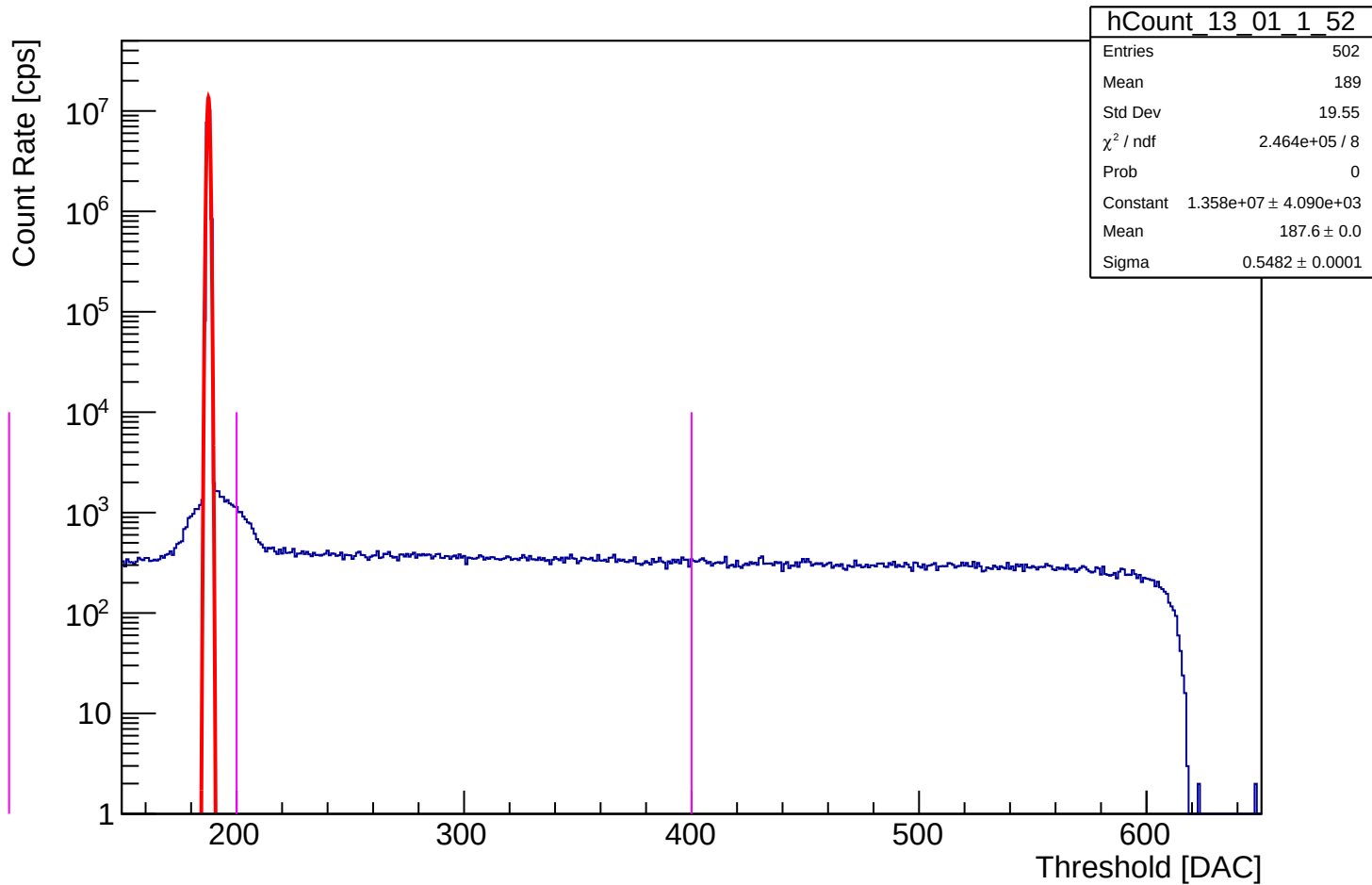
Threshold [DAC]

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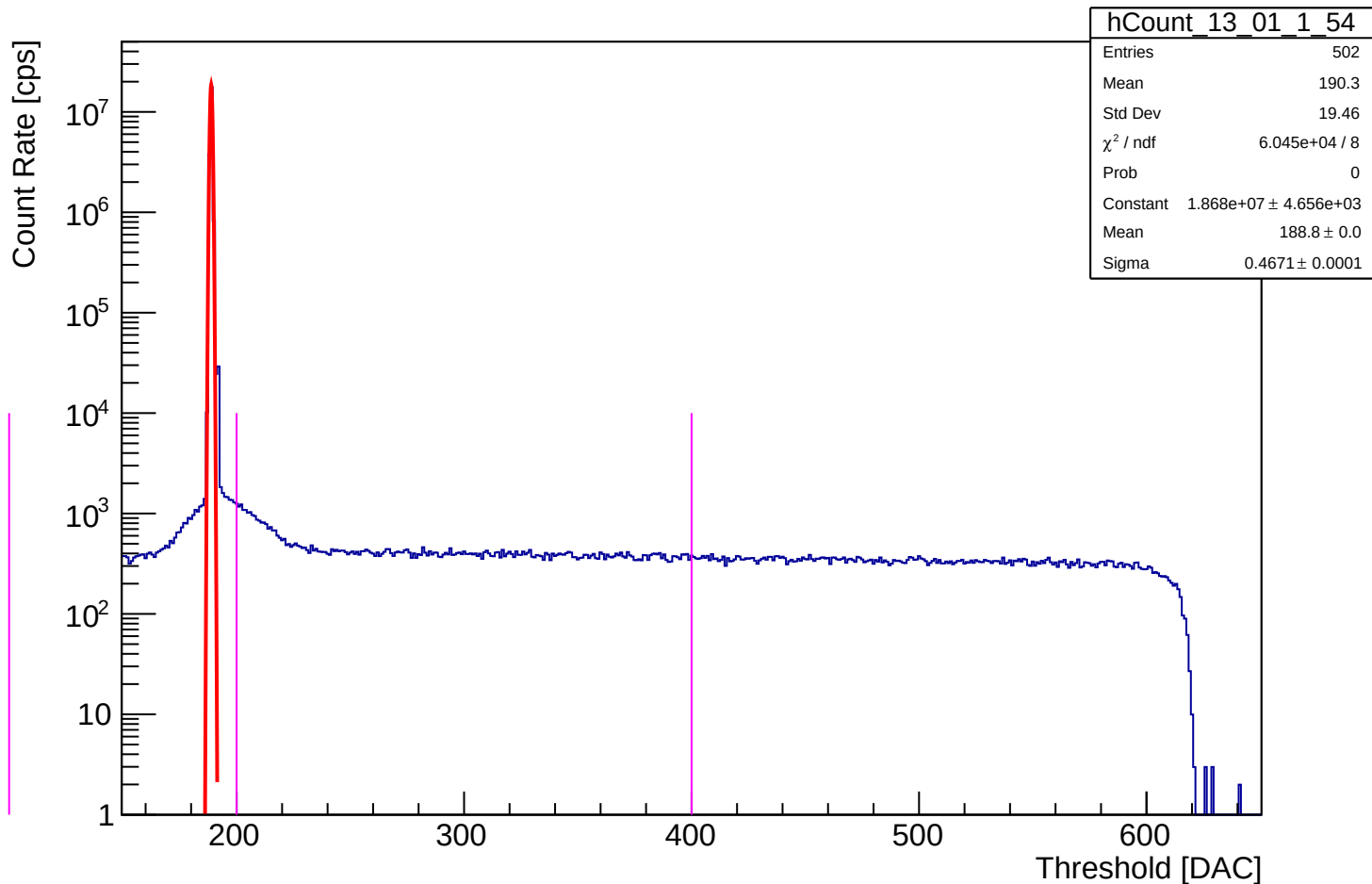




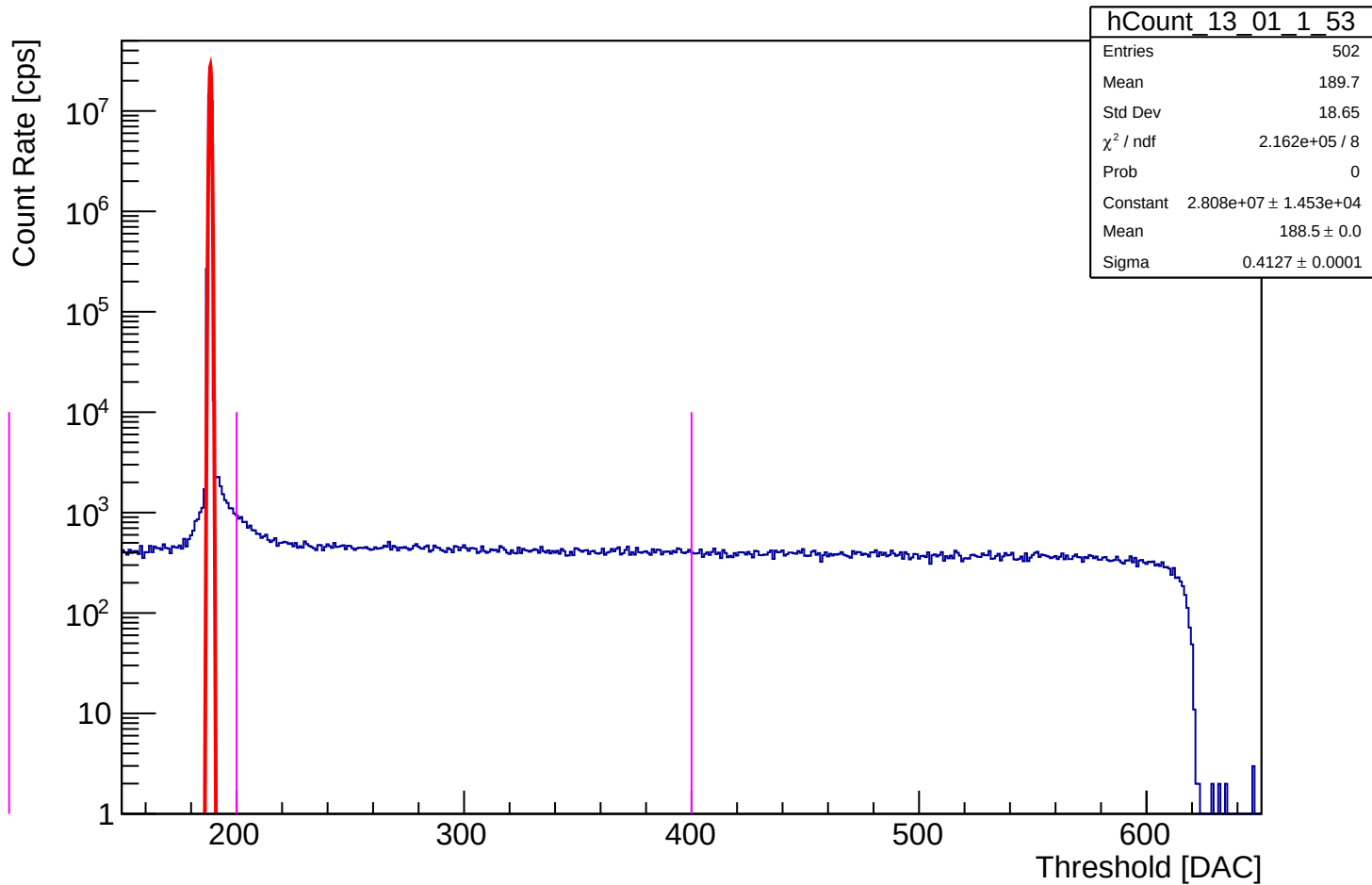
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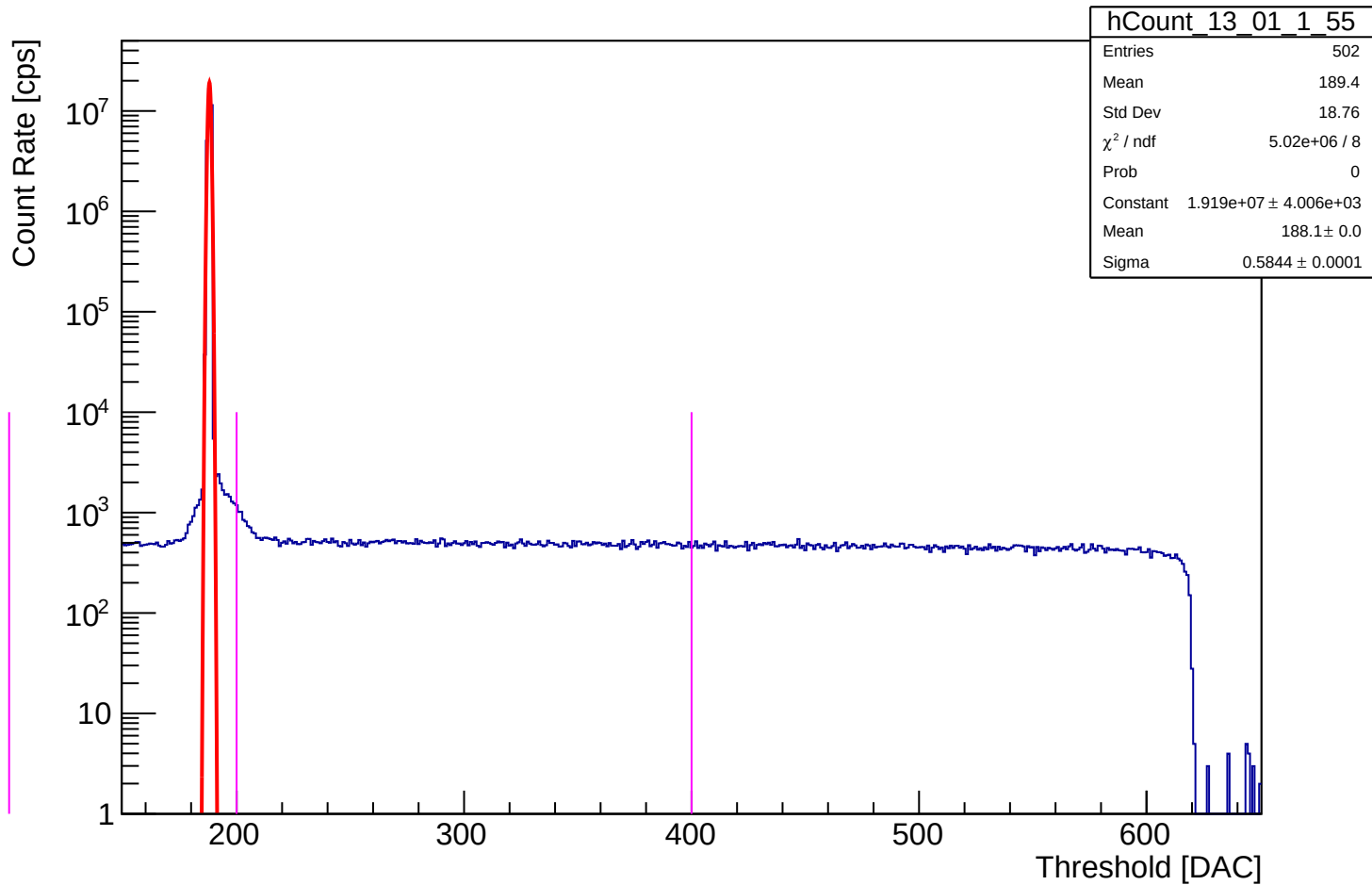
Row 1 Tile 1 Pmt 5 Pixel 46 Slot 13 Fiber 1 Asic 1 Channel 54

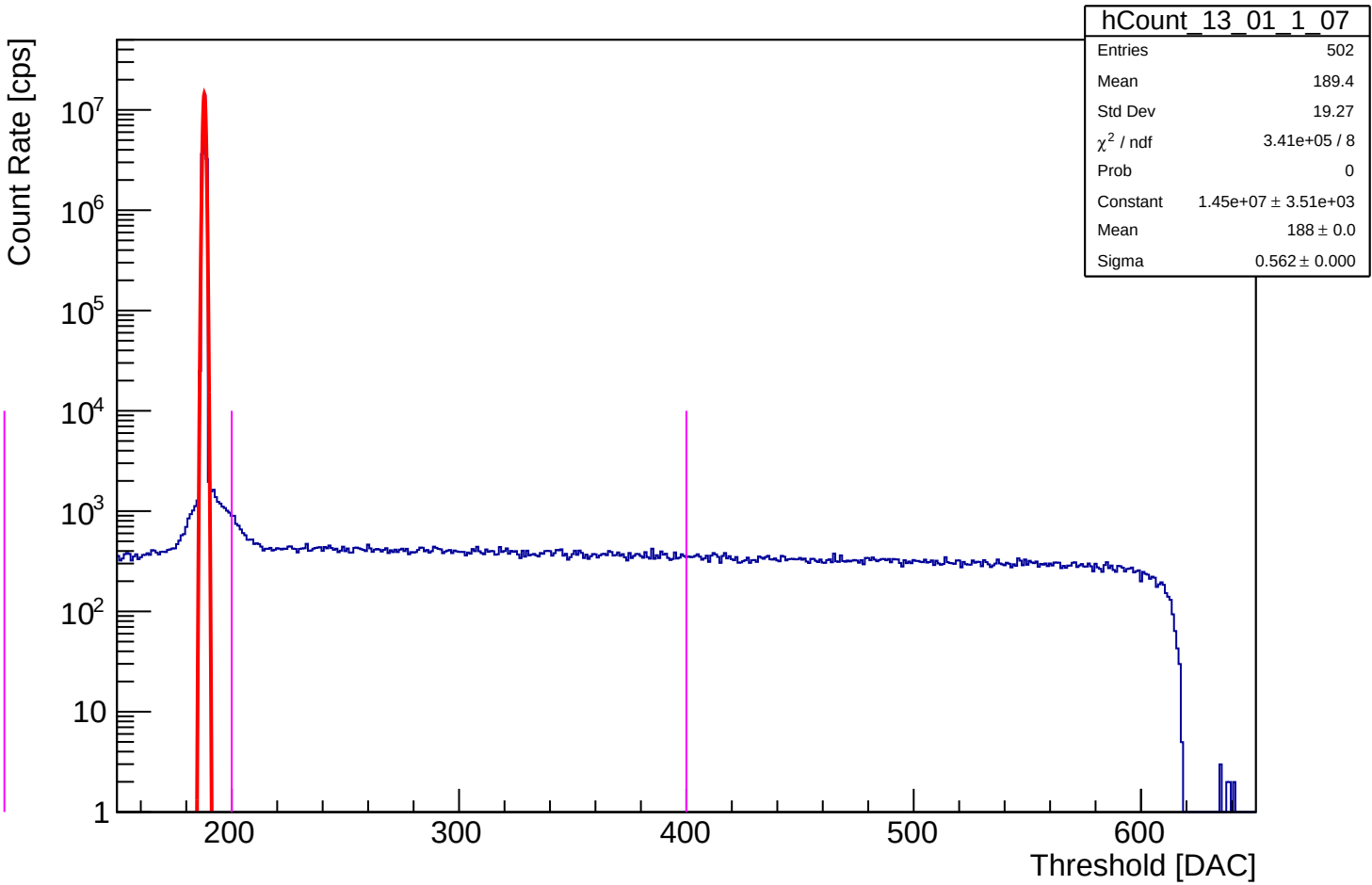


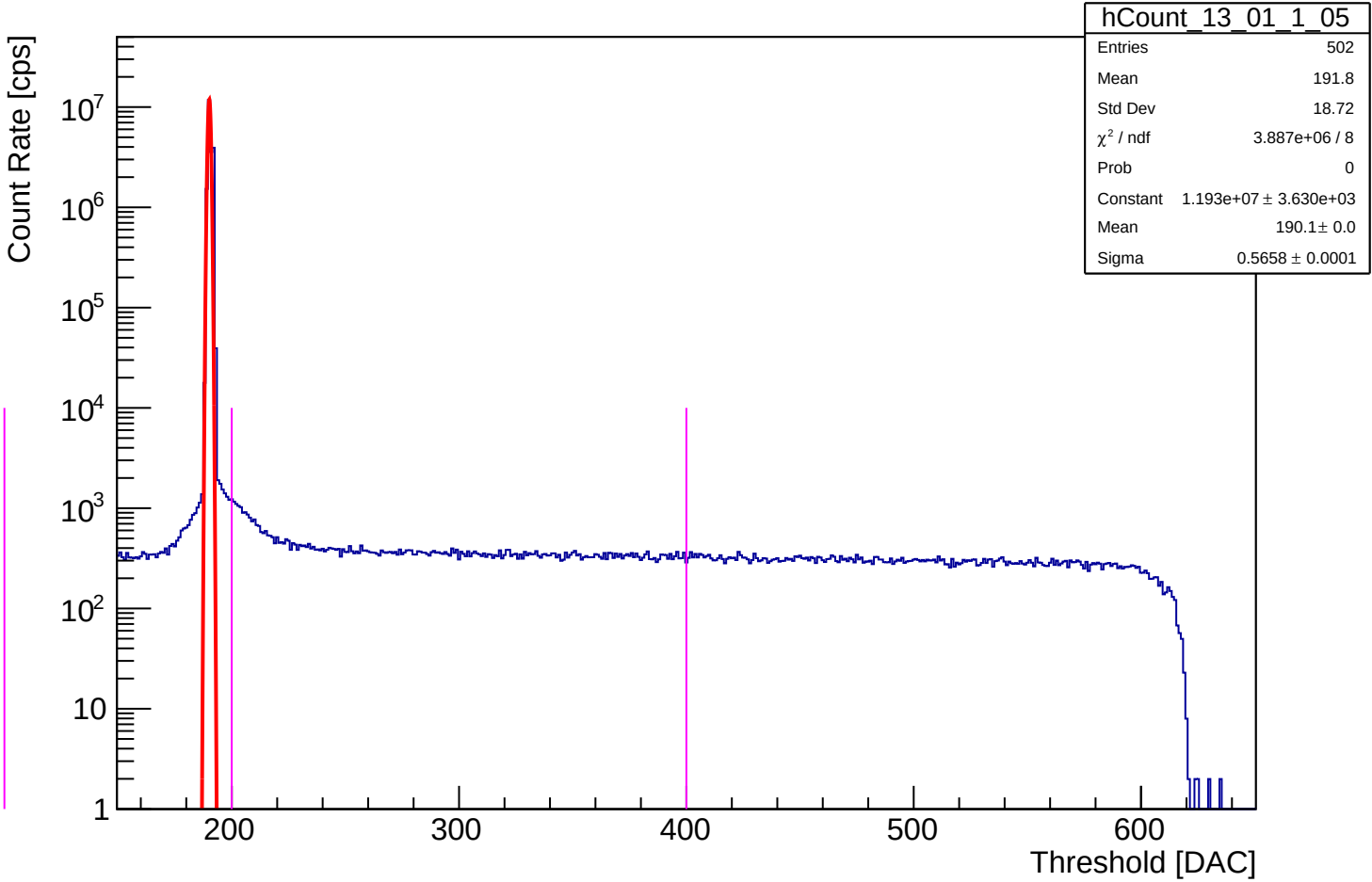
Row 1 Tile 1 Pmt 5 Pixel 47 Slot 13 Fiber 1 Asic 1 Channel 53

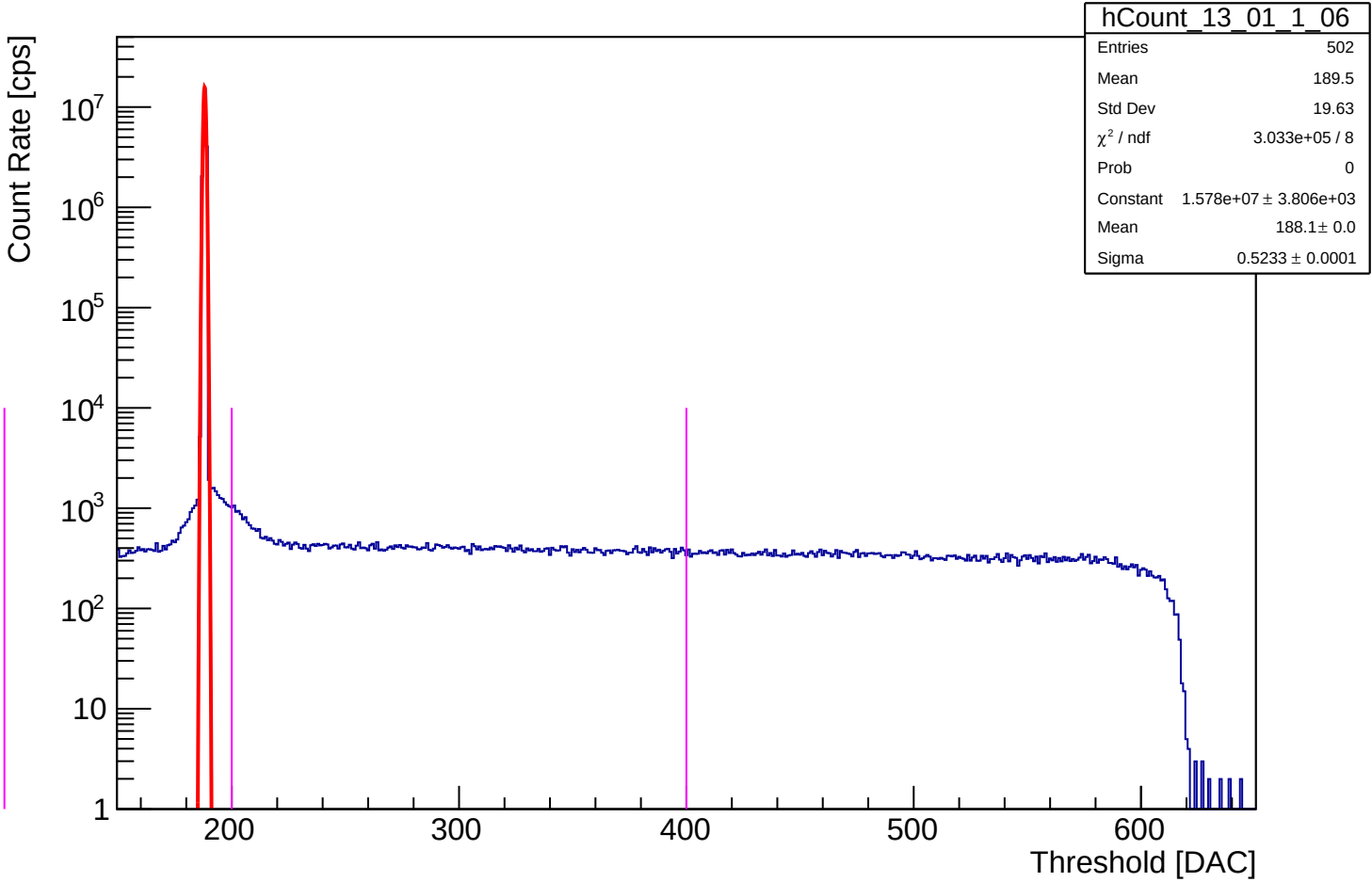


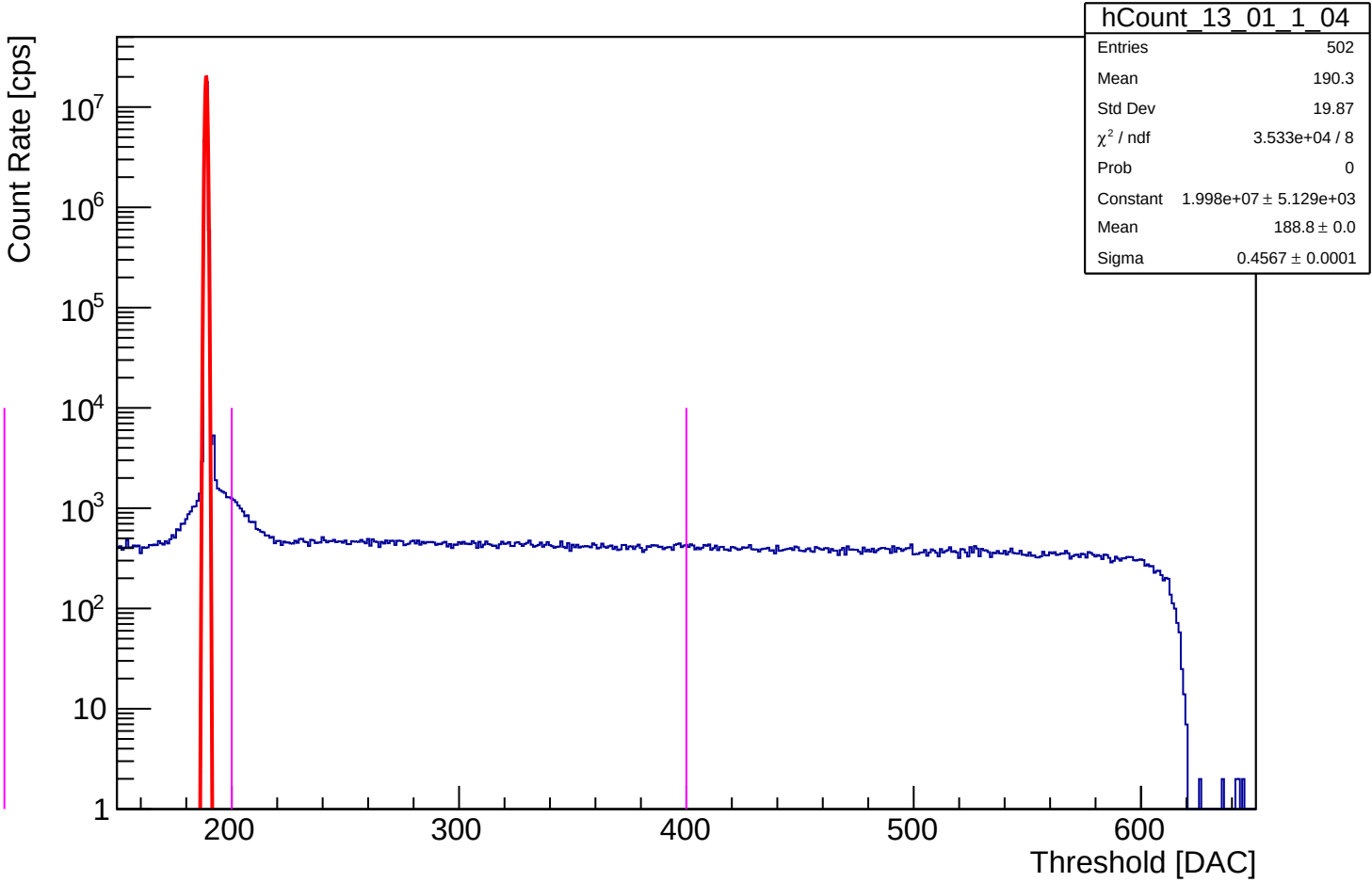
Row 1 Tile 1 Pmt 5 Pixel 48 Slot 13 Fiber 1 Asic 1 Channel 55



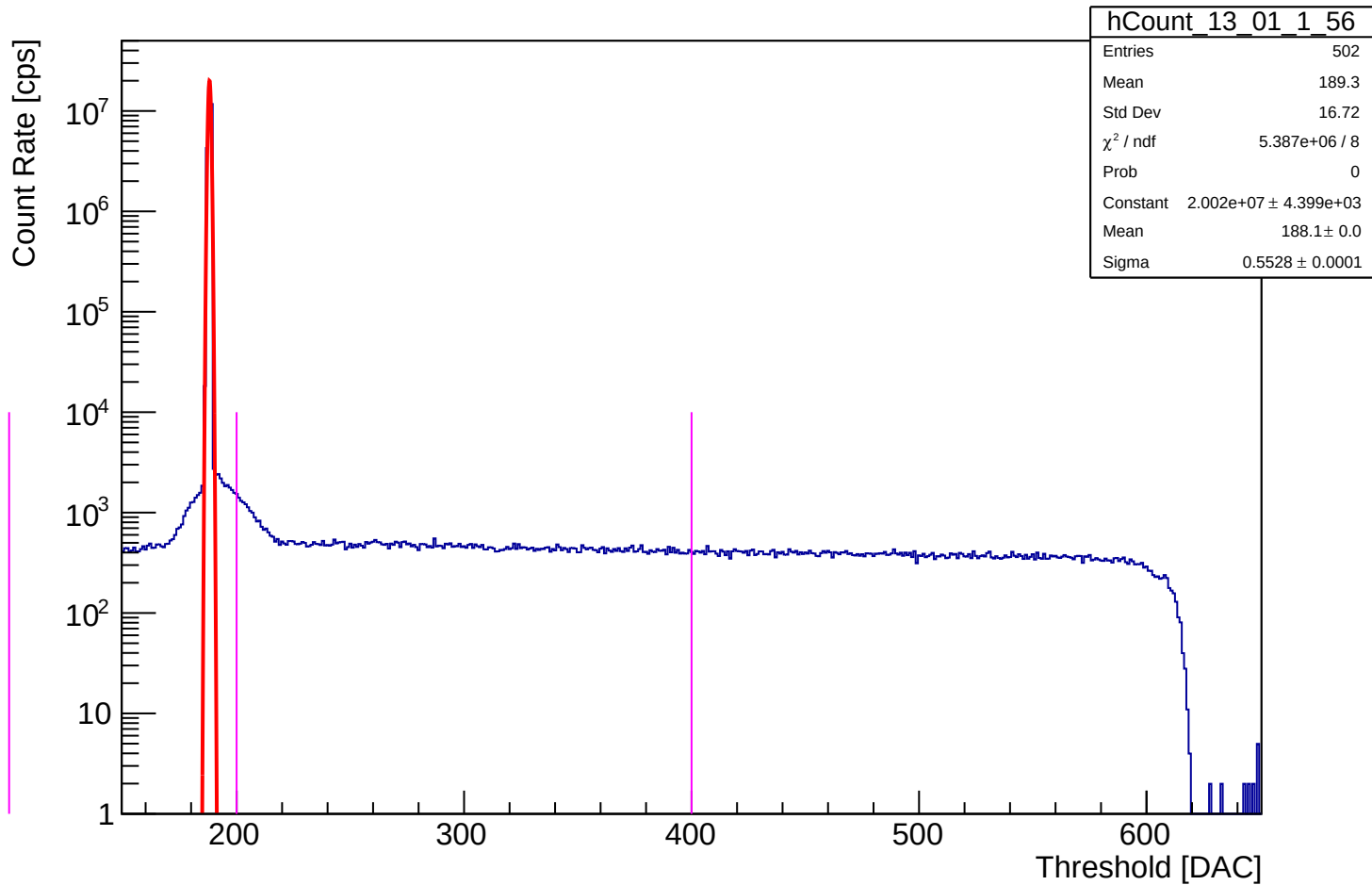




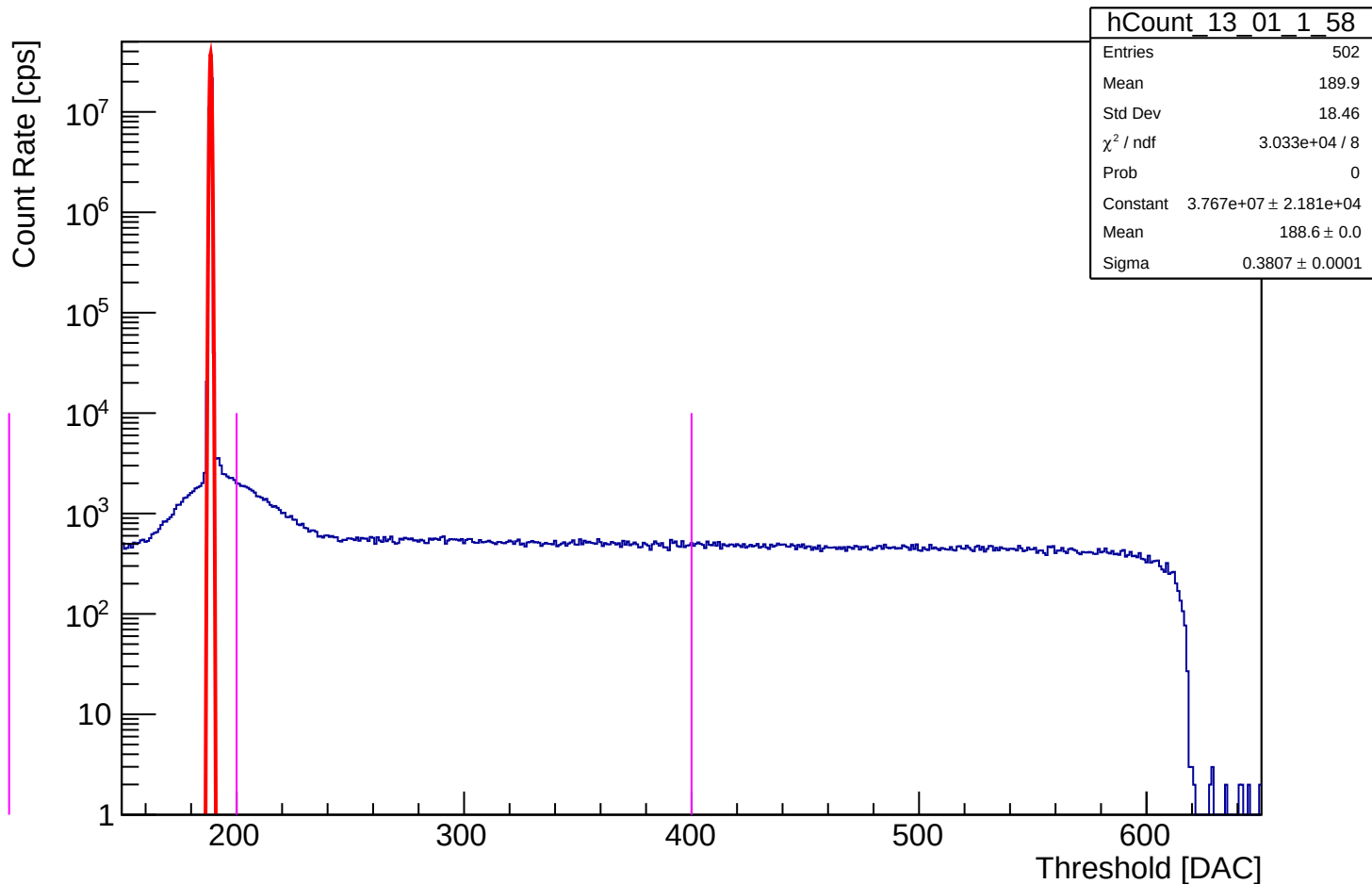




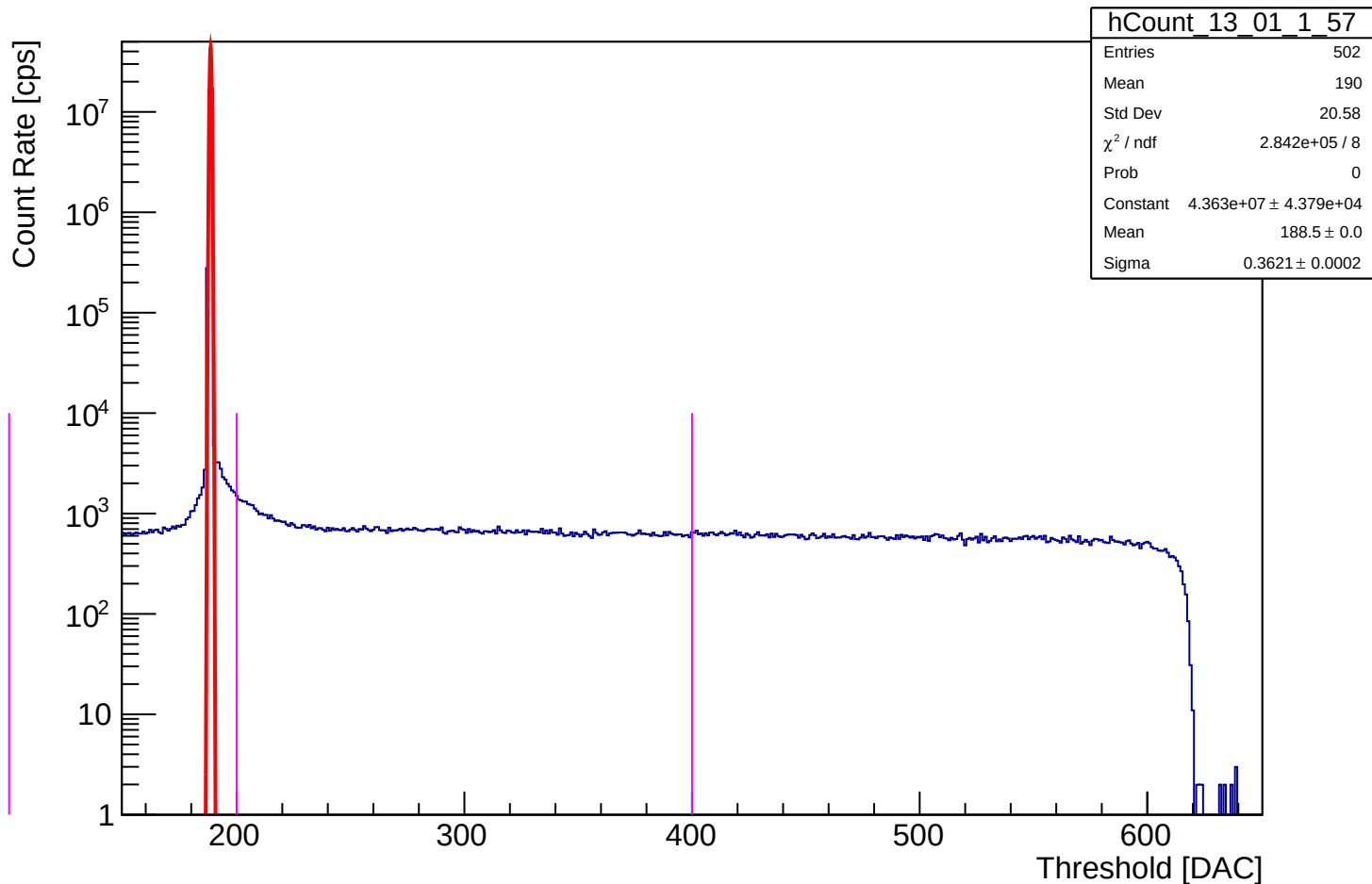
Row 1 Tile 1 Pmt 5 Pixel 53 Slot 13 Fiber 1 Asic 1 Channel 56

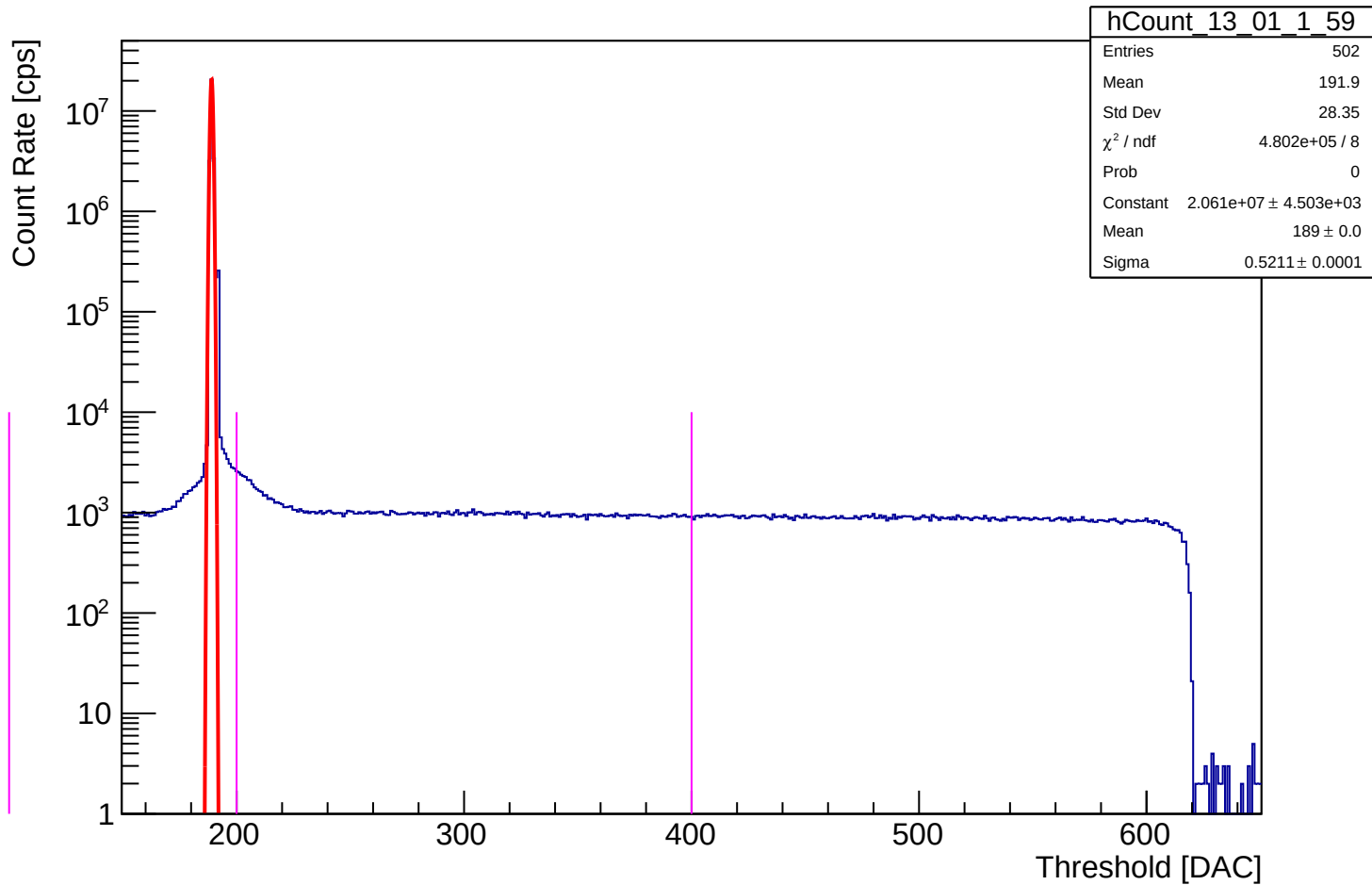


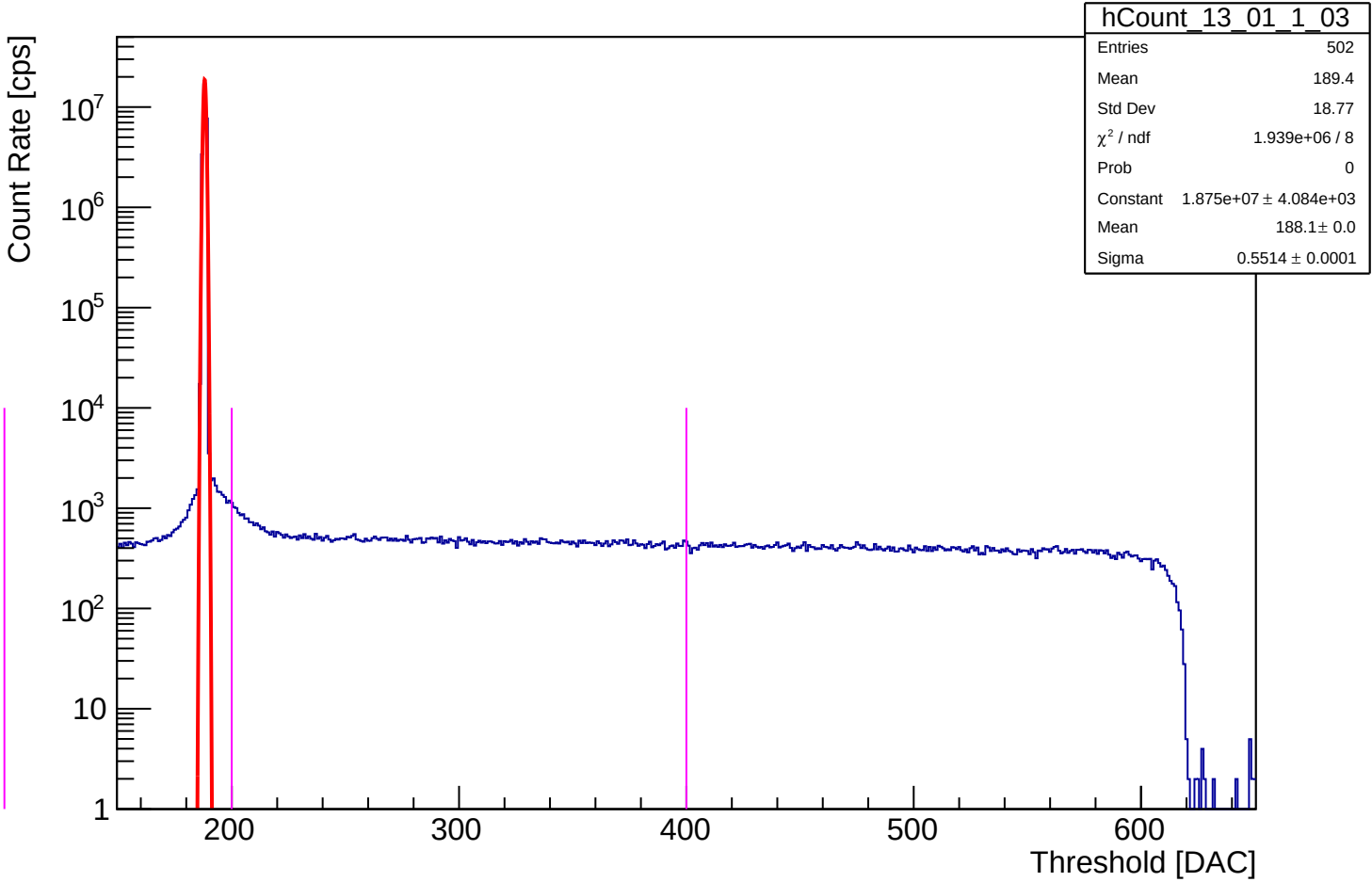
Row 1 Tile 1 Pmt 5 Pixel 54 Slot 13 Fiber 1 Asic 1 Channel 58



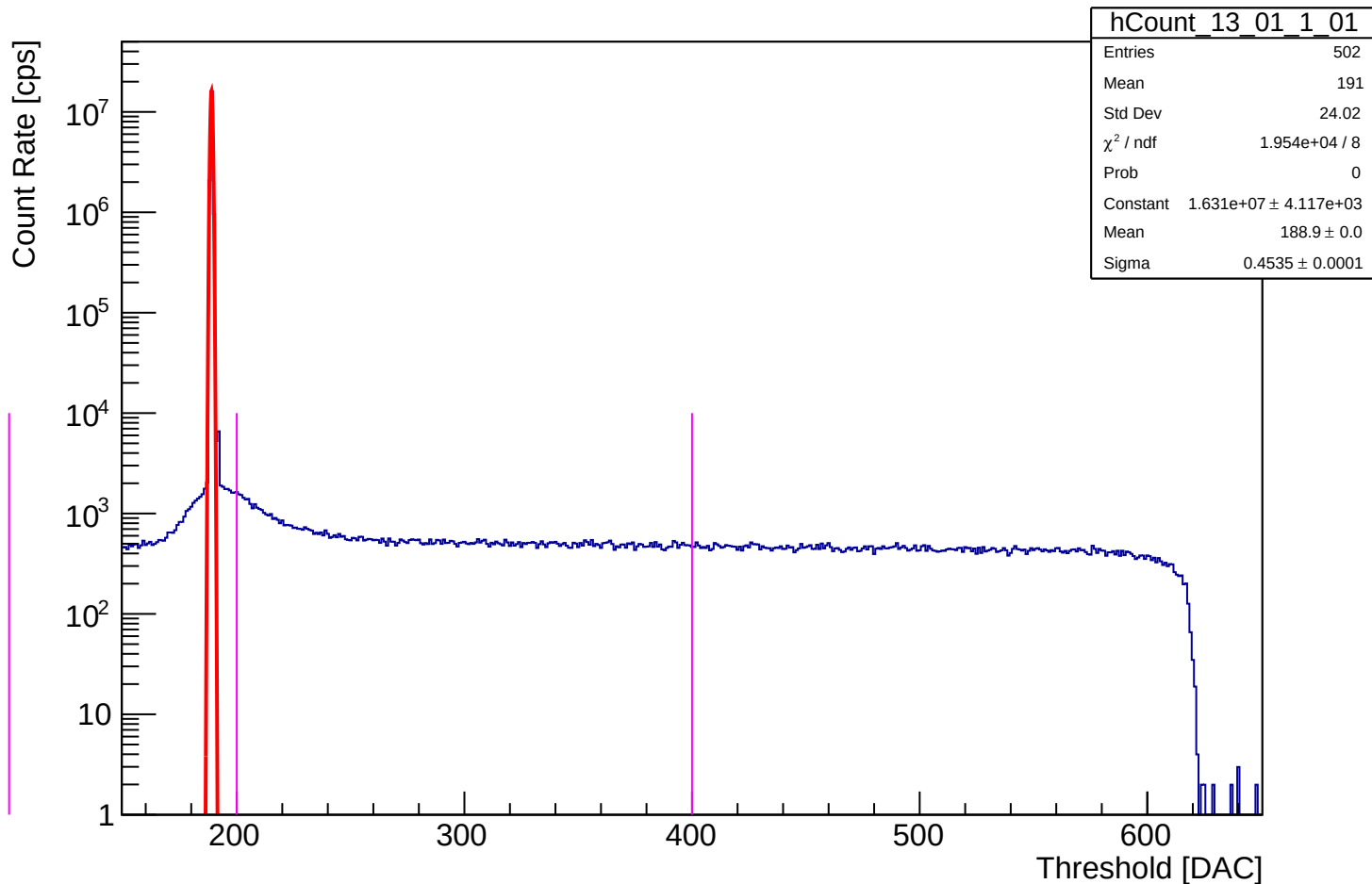
Row 1 Tile 1 Pmt 5 Pixel 55 Slot 13 Fiber 1 Asic 1 Channel 57

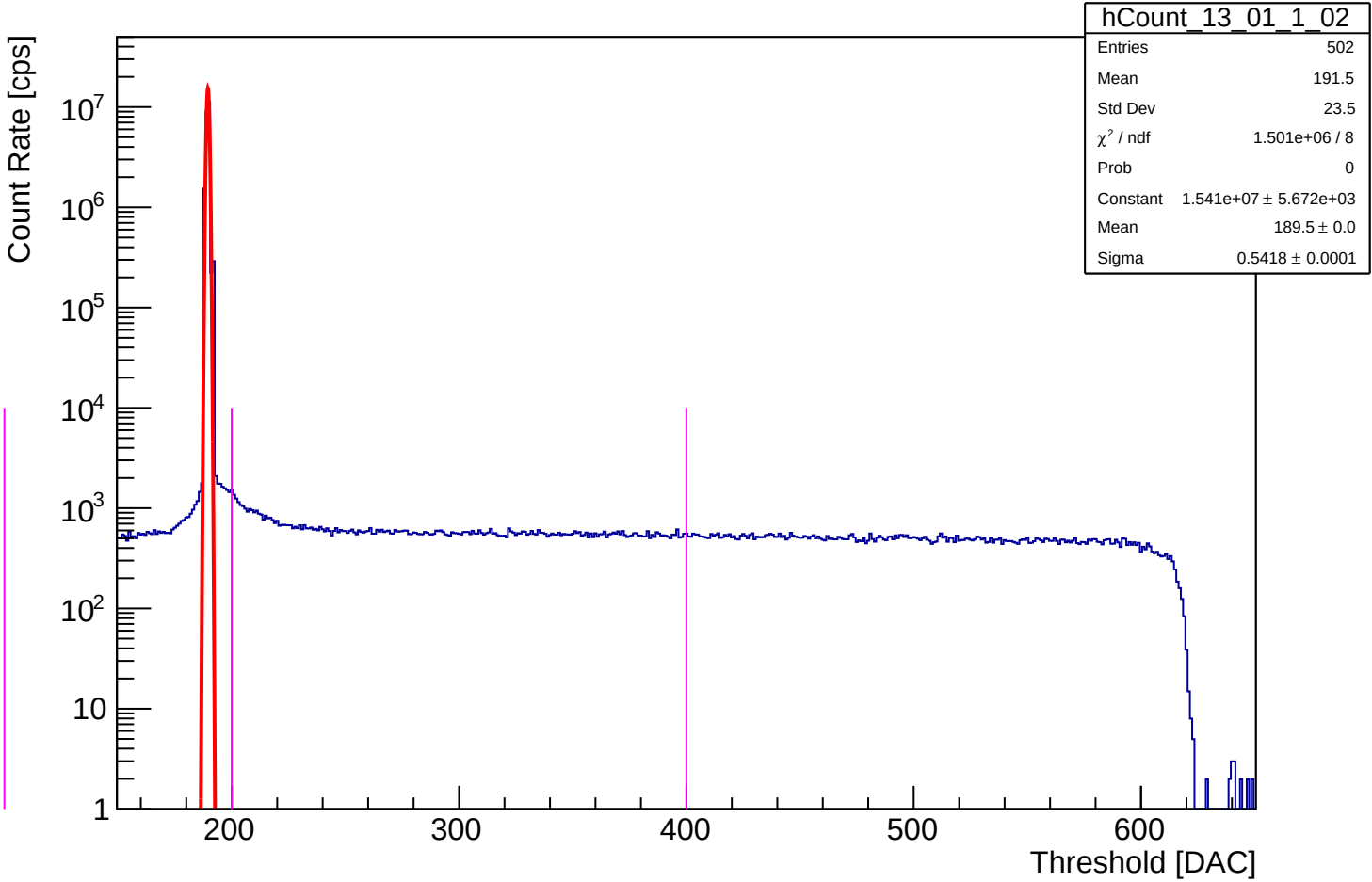






Row 1 Tile 1 Pmt 5 Pixel 58 Slot 13 Fiber 1 Asic 1 Channel 1





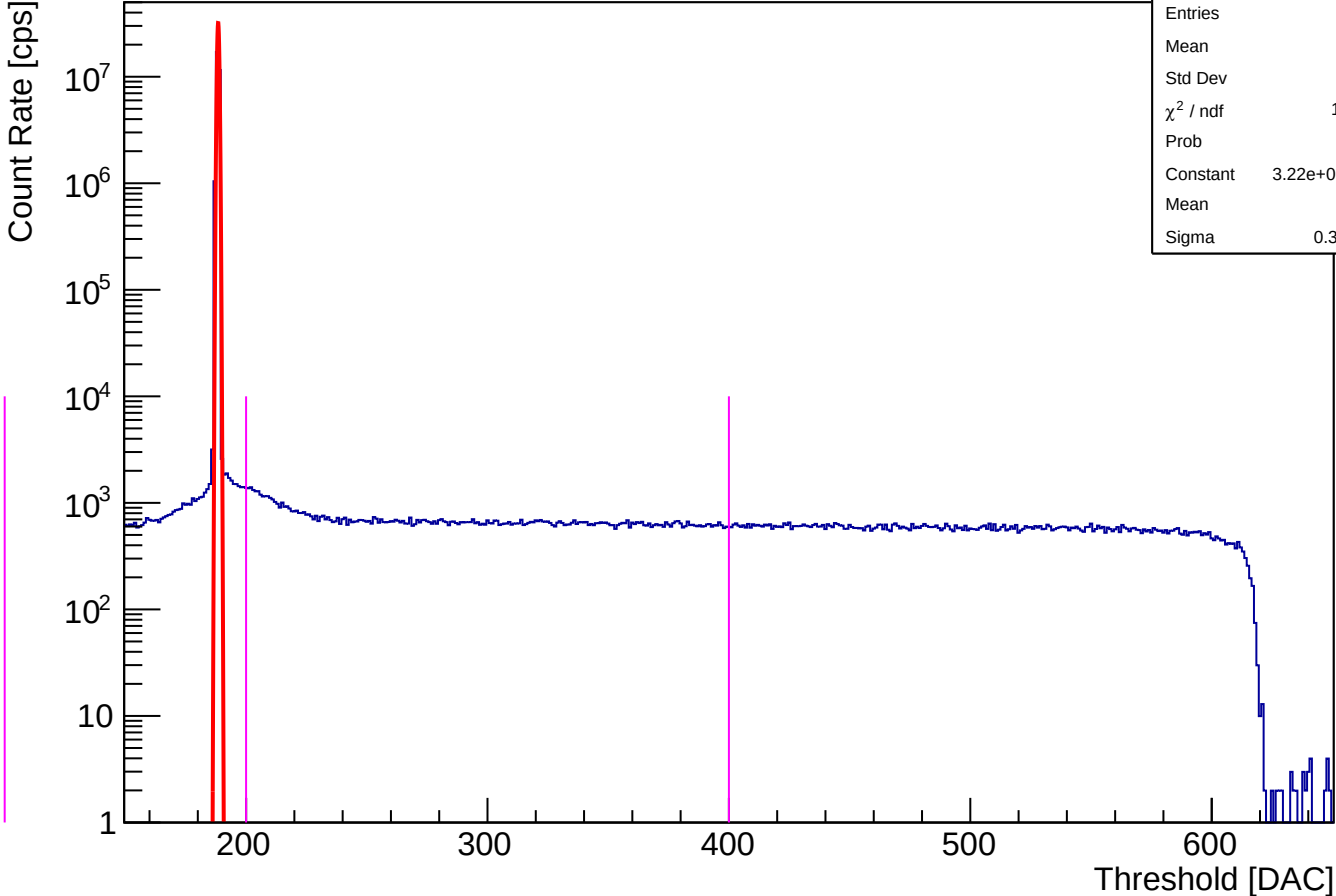
Count Rate [cps]

10⁷
10⁶
10⁵
10⁴
10³
10²
10
1

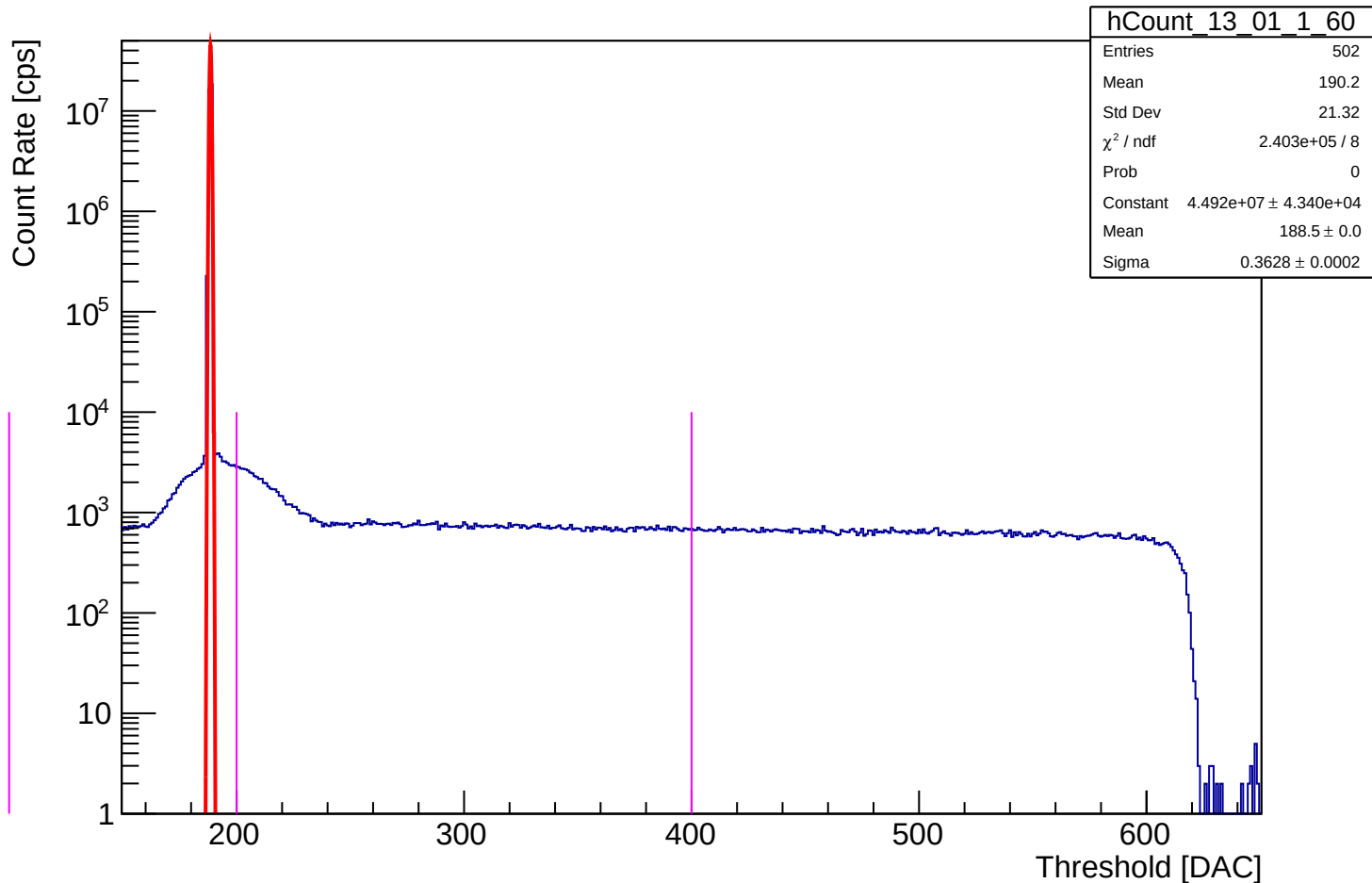
200 300 400 500 600

Threshold [DAC]

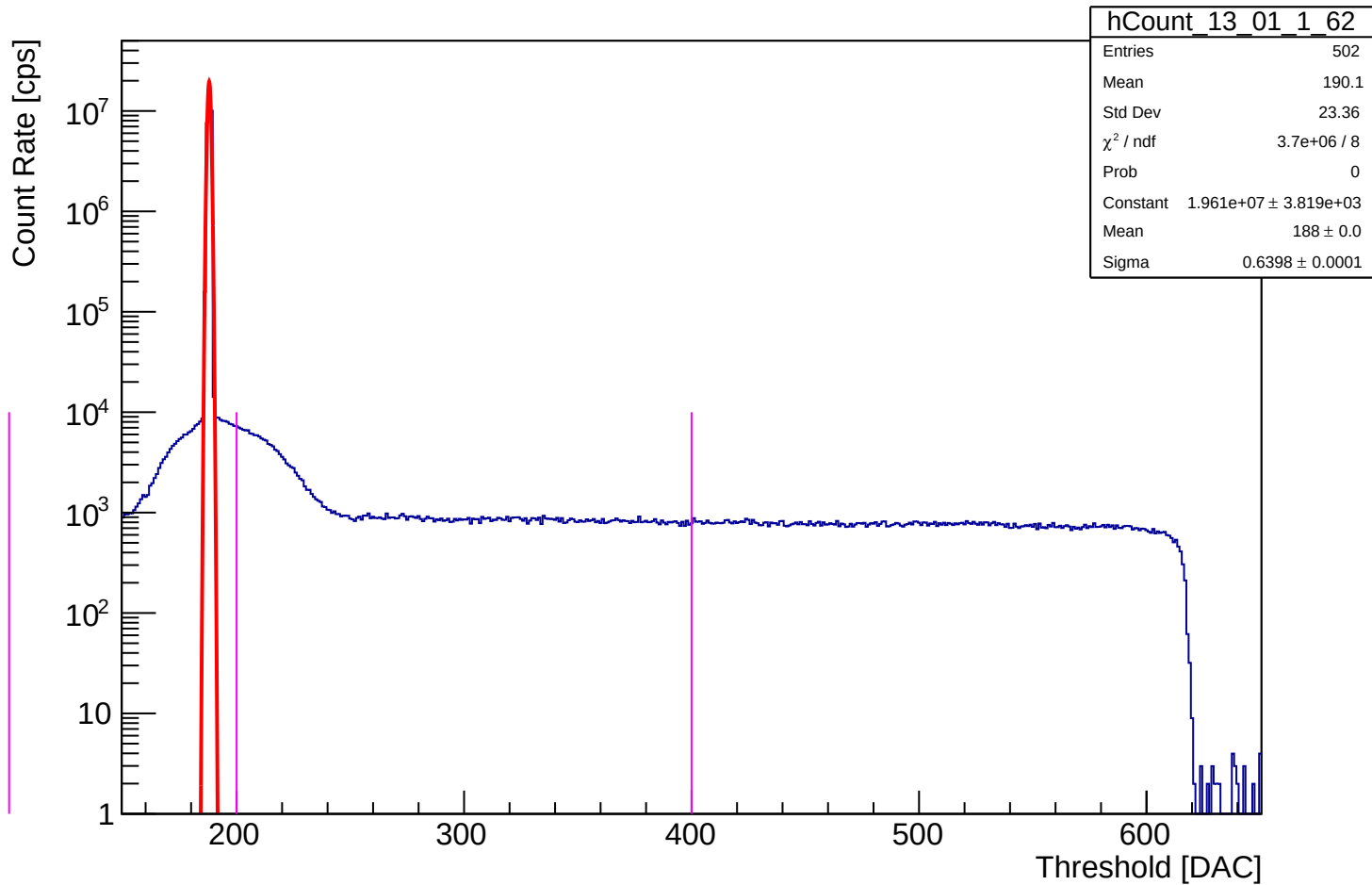
hCount_13_01_1_00	
Entries	502
Mean	190.1
Std Dev	22.13
χ^2 / ndf	1.014e+06 / 8
Prob	0
Constant	3.22e+07 $\pm$ 2.04e+04
Mean	188.4 $\pm$ 0.0
Sigma	0.3909 $\pm$ 0.0001



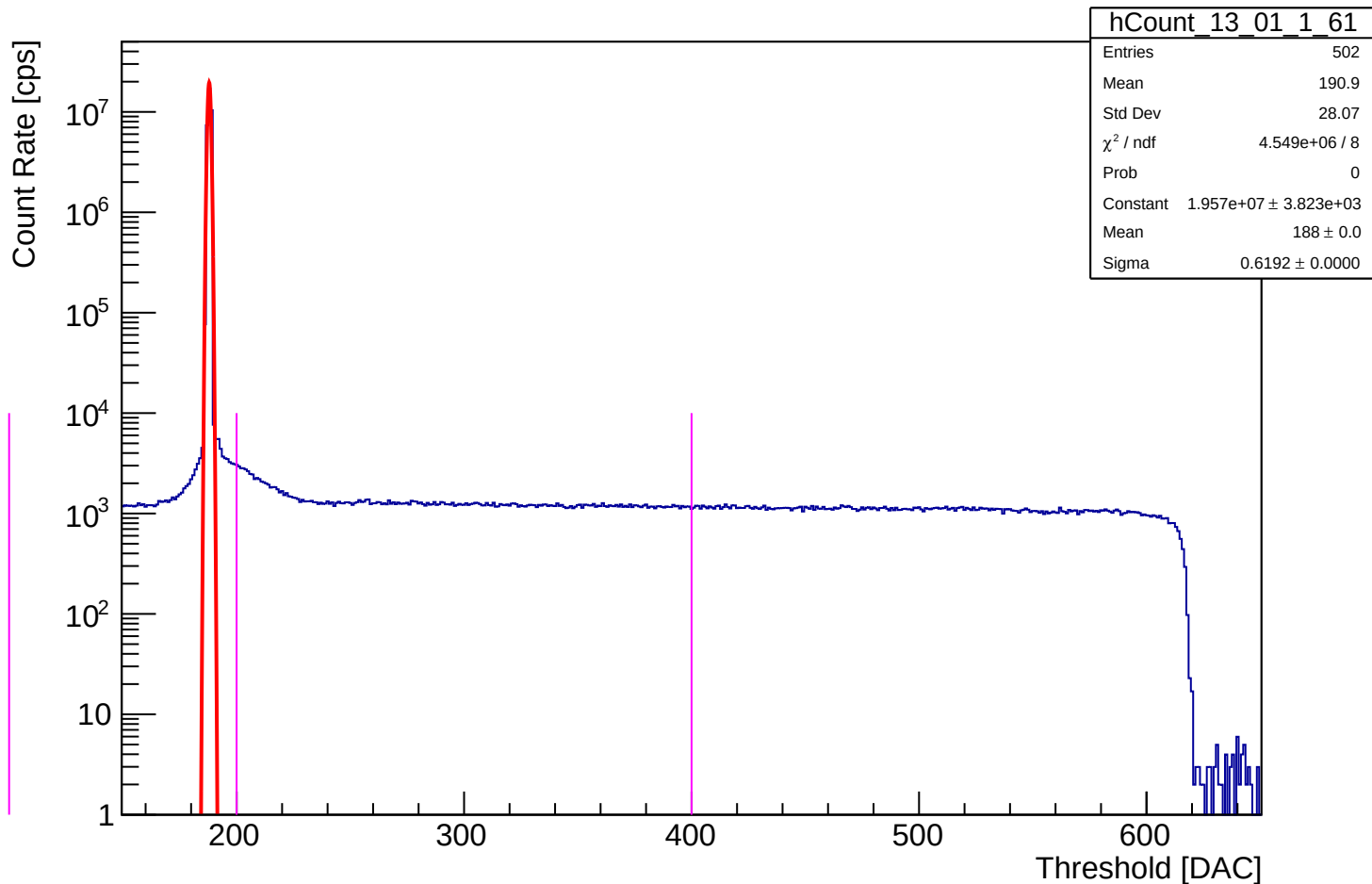
Row 1 Tile 1 Pmt 5 Pixel 61 Slot 13 Fiber 1 Asic 1 Channel 60



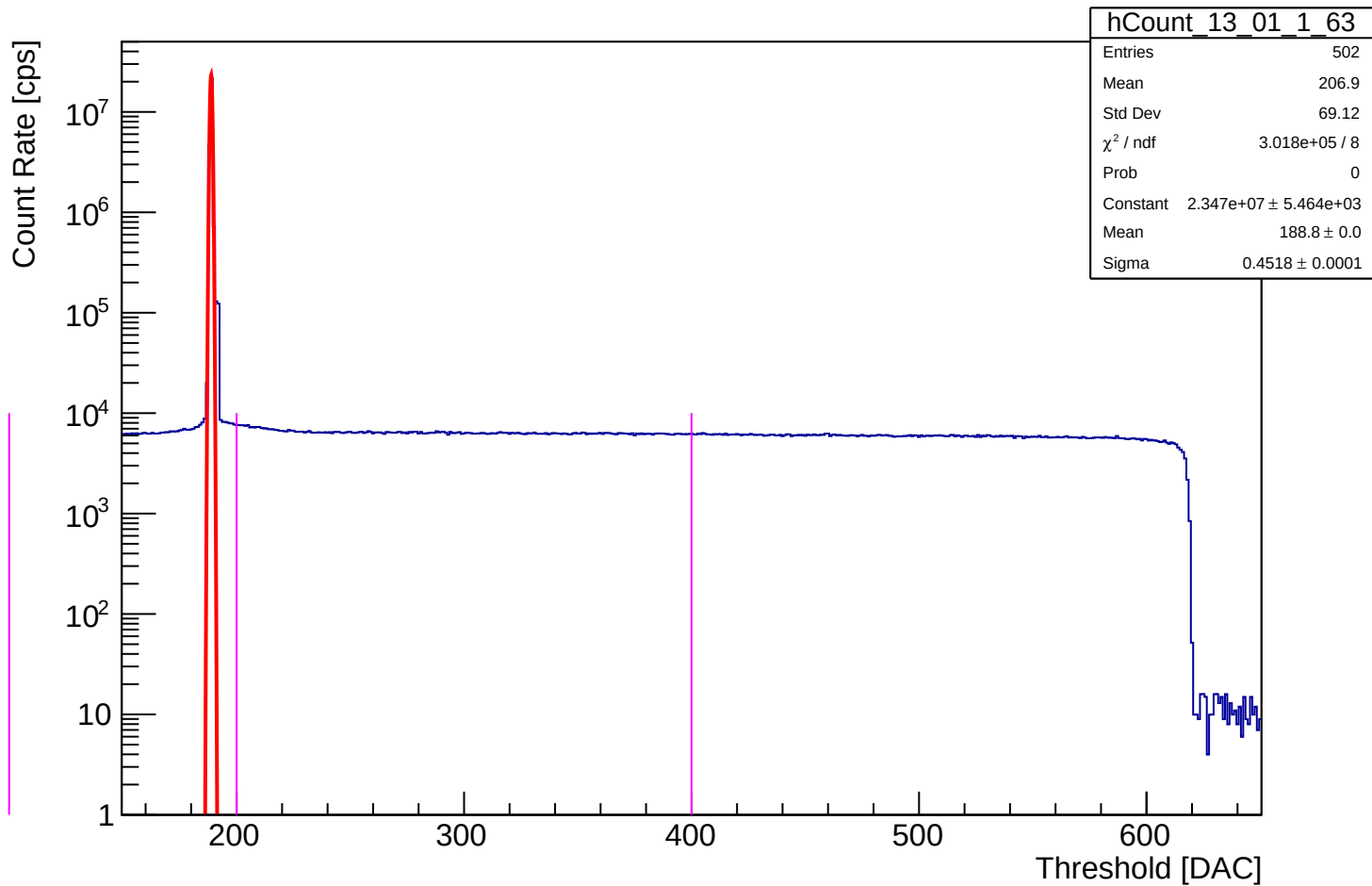
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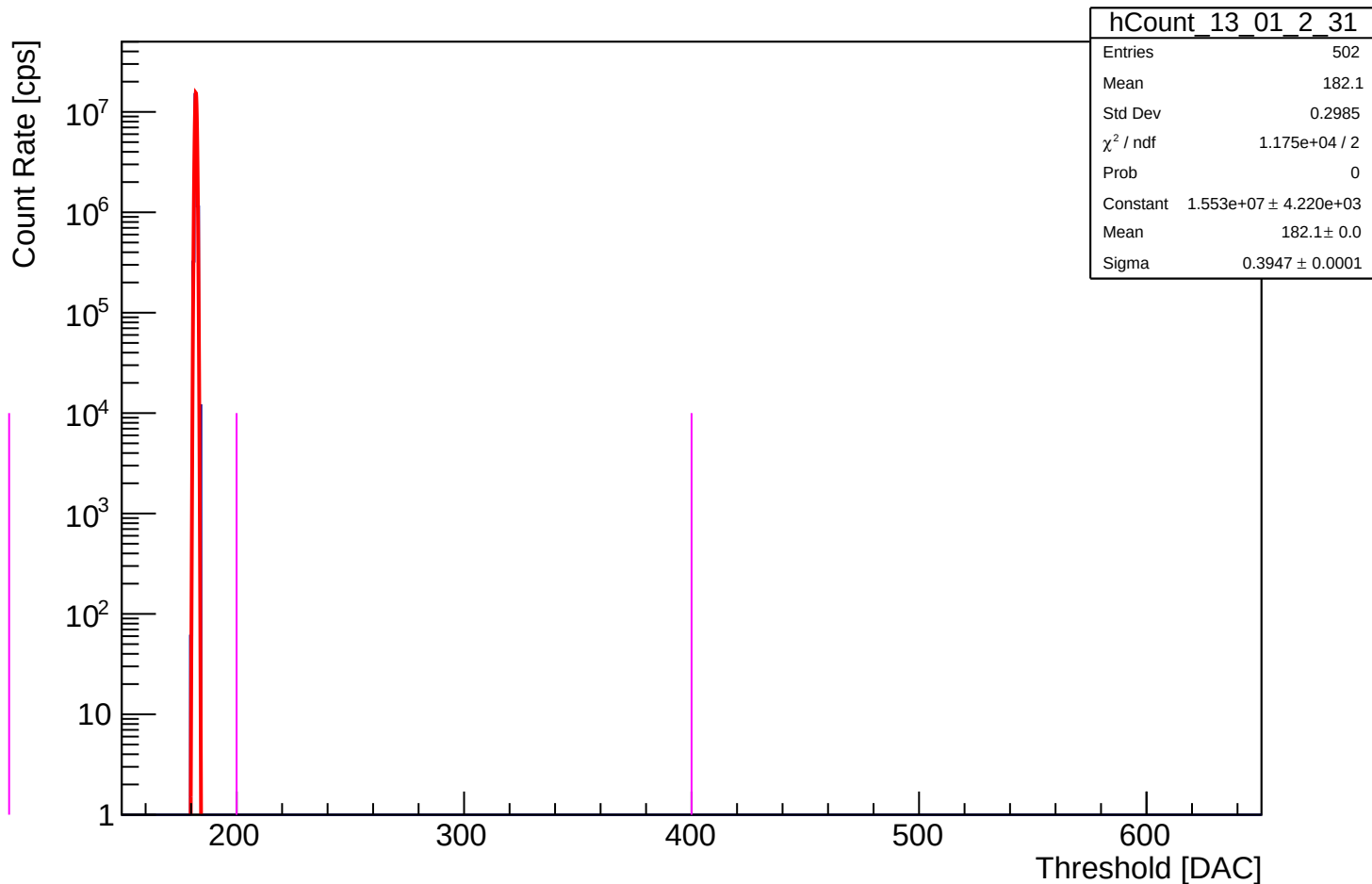
Row 1 Tile 1 Pmt 5 Pixel 63 Slot 13 Fiber 1 Asic 1 Channel 61



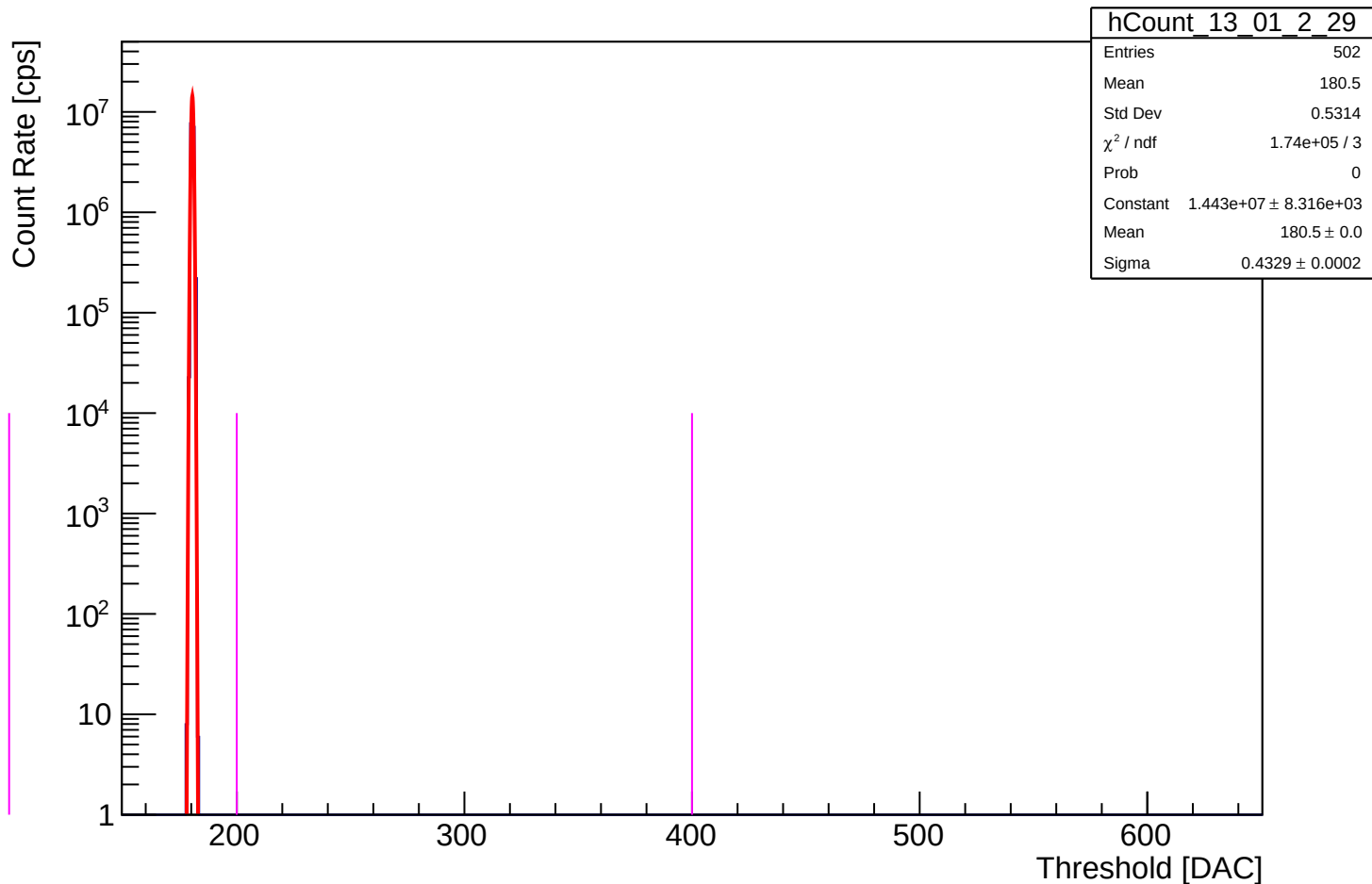
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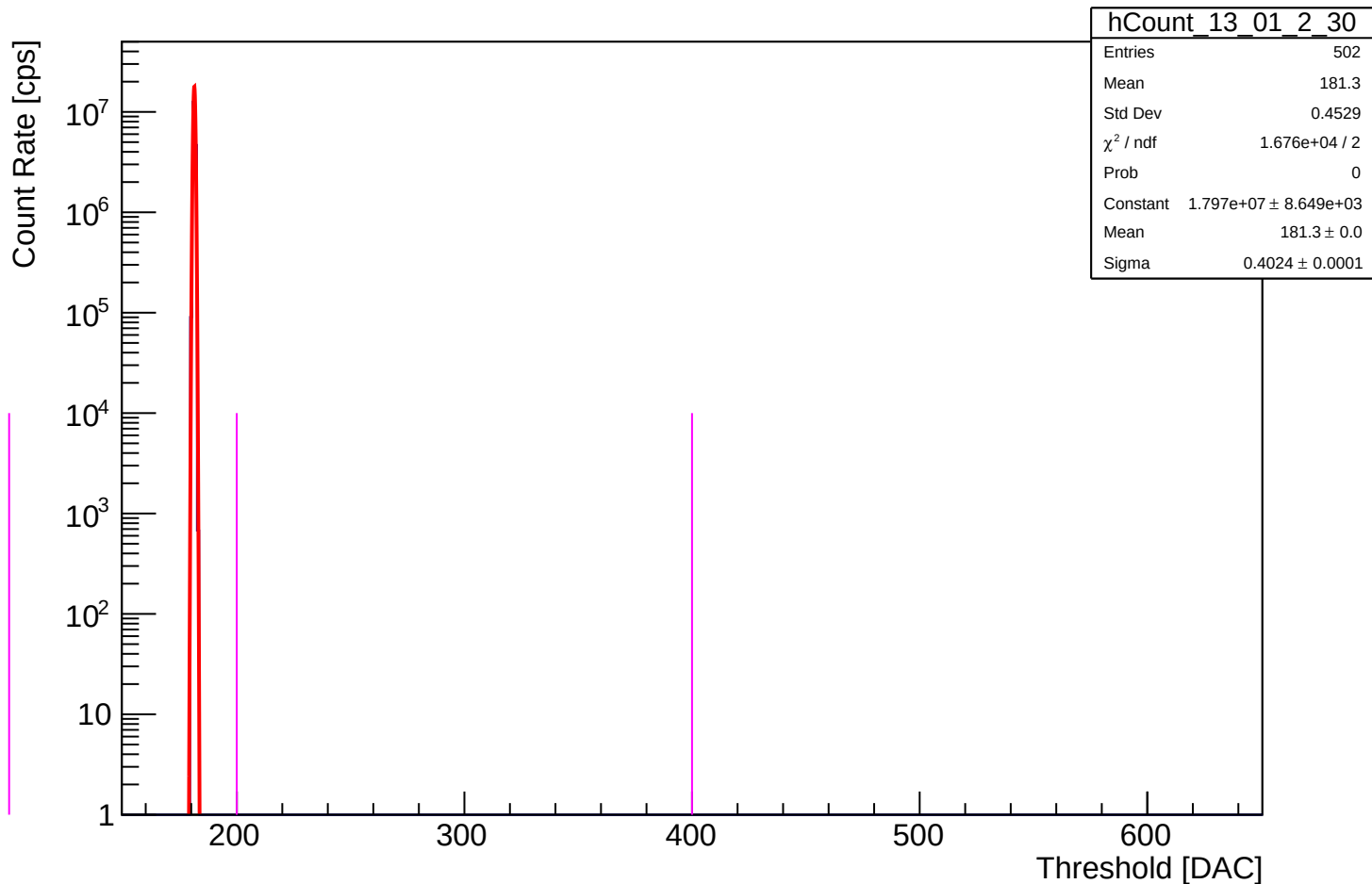
Row 1 Tile 1 Pmt 6 Pixel 1 Slot 13 Fiber 1 Asic 2 Channel 31



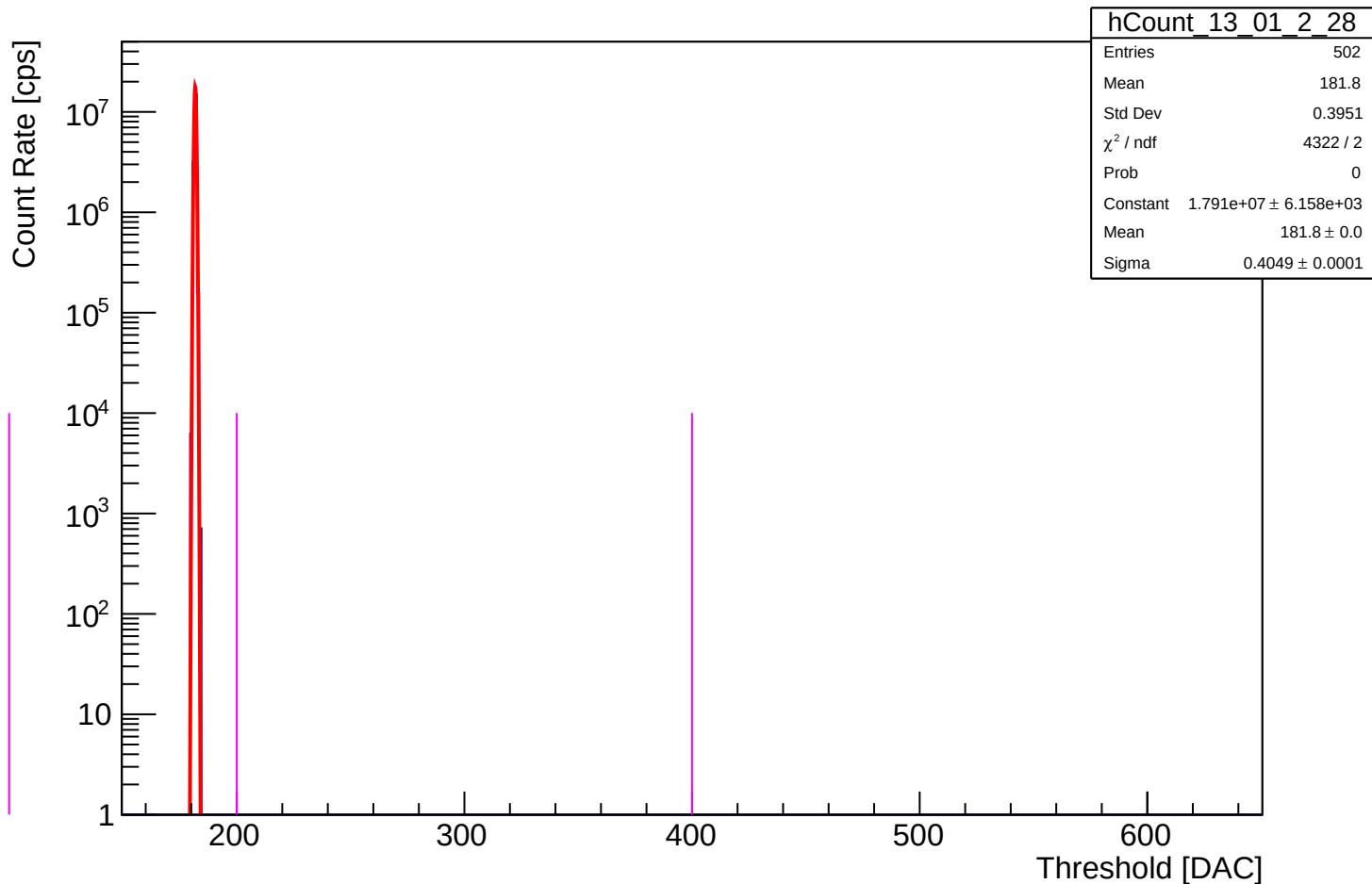
Row 1 Tile 1 Pmt 6 Pixel 2 Slot 13 Fiber 1 Asic 2 Channel 29



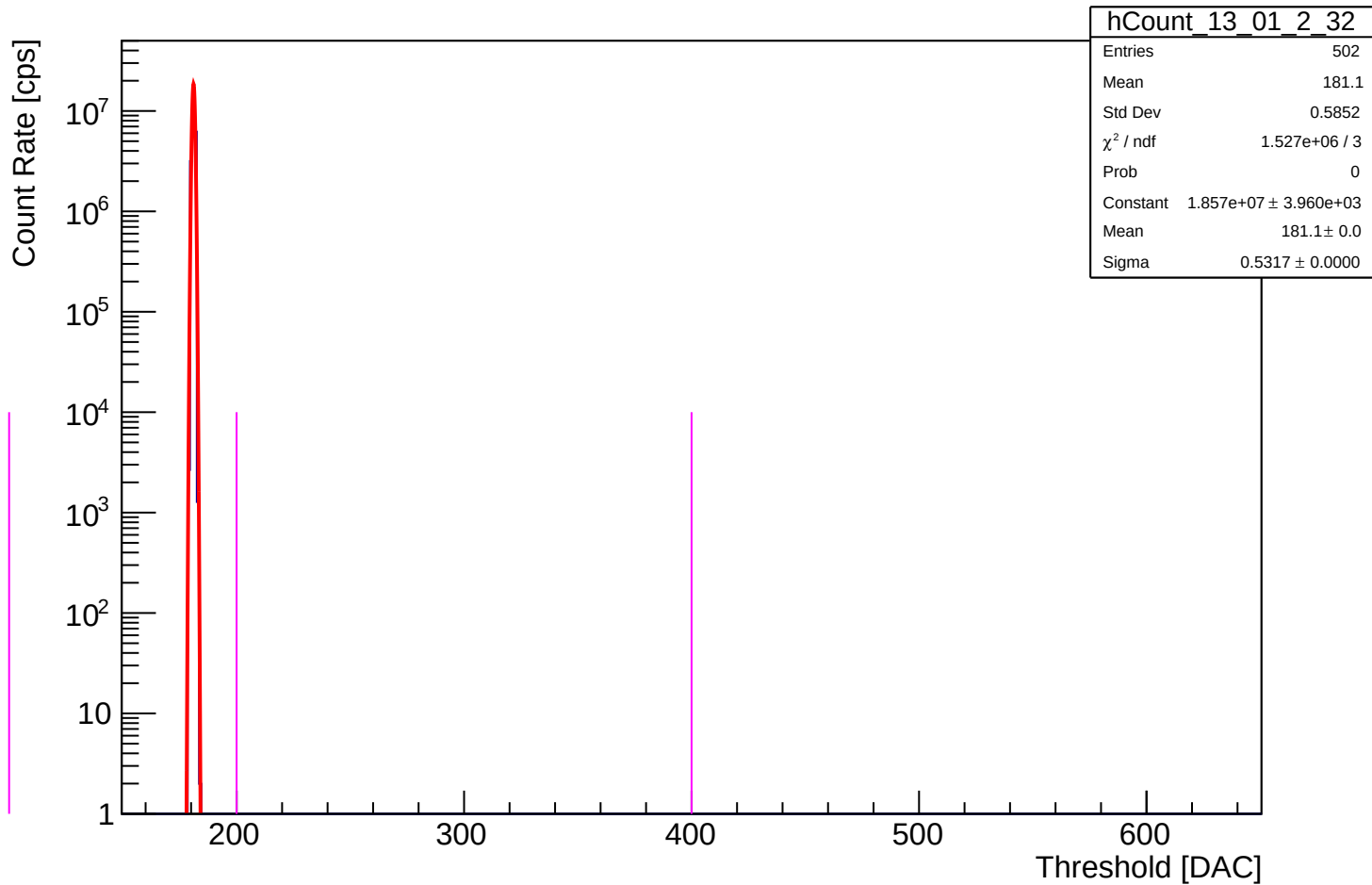
Row 1 Tile 1 Pmt 6 Pixel 3 Slot 13 Fiber 1 Asic 2 Channel 30



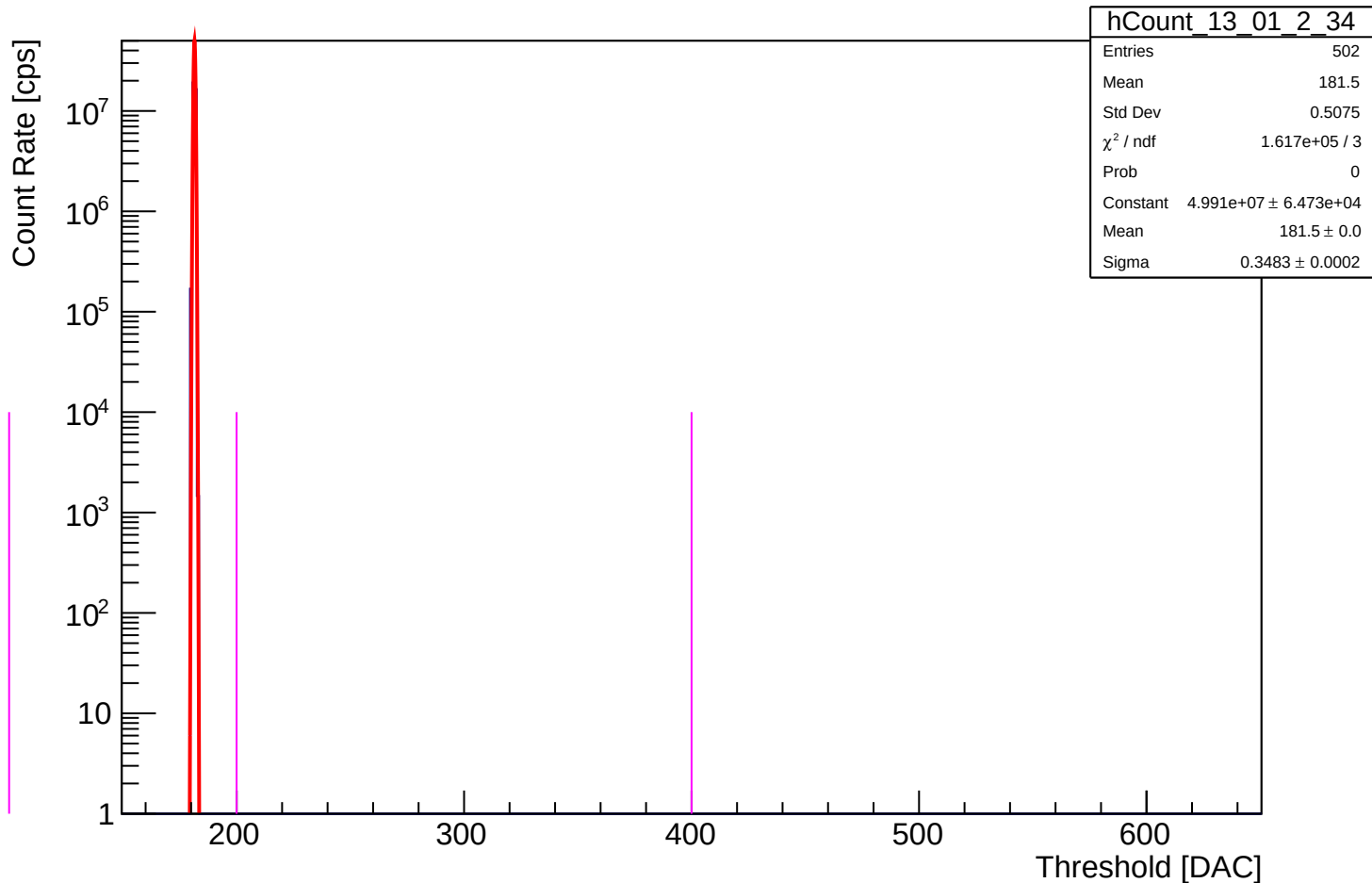
Row 1 Tile 1 Pmt 6 Pixel 4 Slot 13 Fiber 1 Asic 2 Channel 28



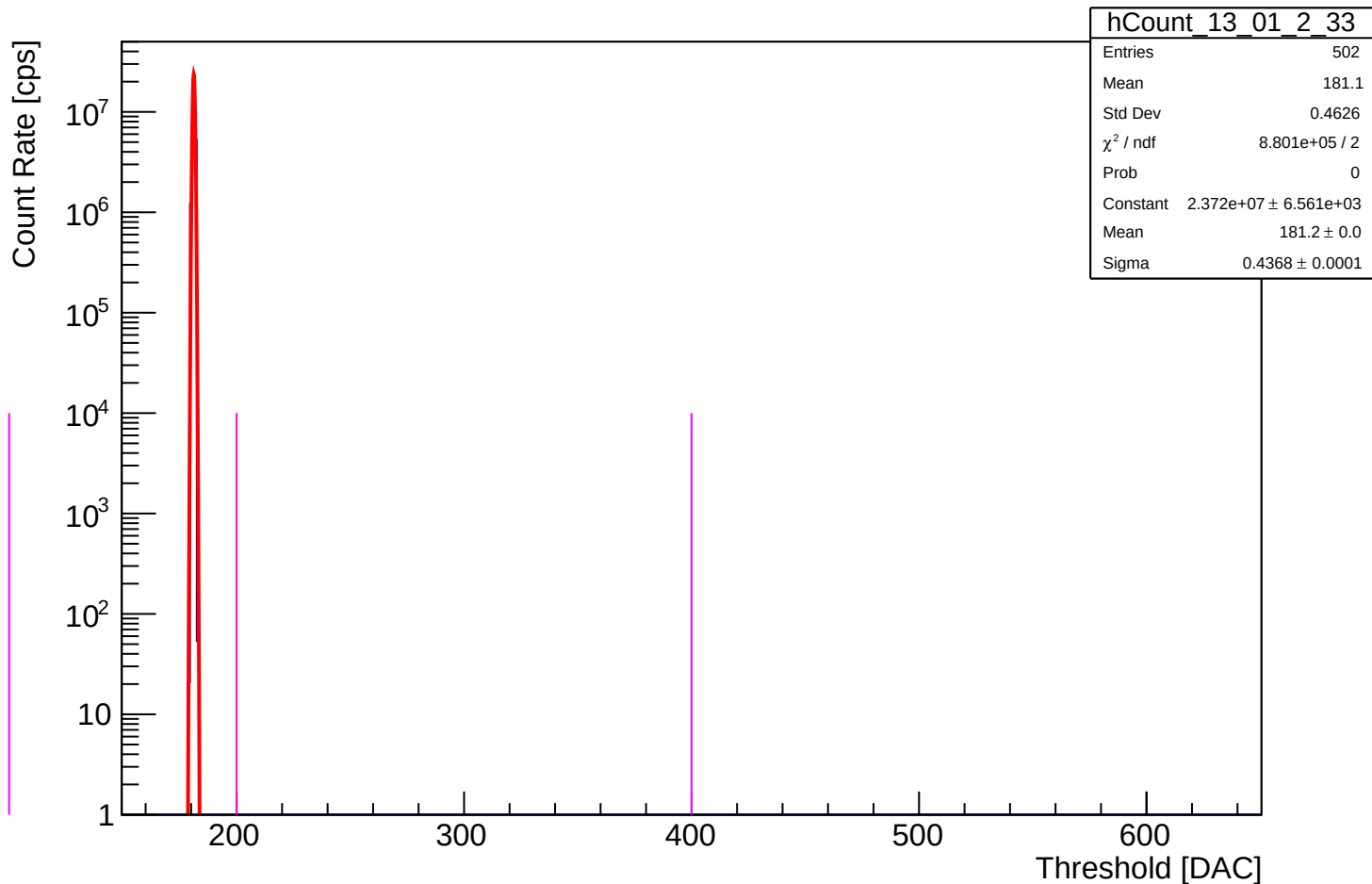
Row 1 Tile 1 Pmt 6 Pixel 5 Slot 13 Fiber 1 Asic 2 Channel 32



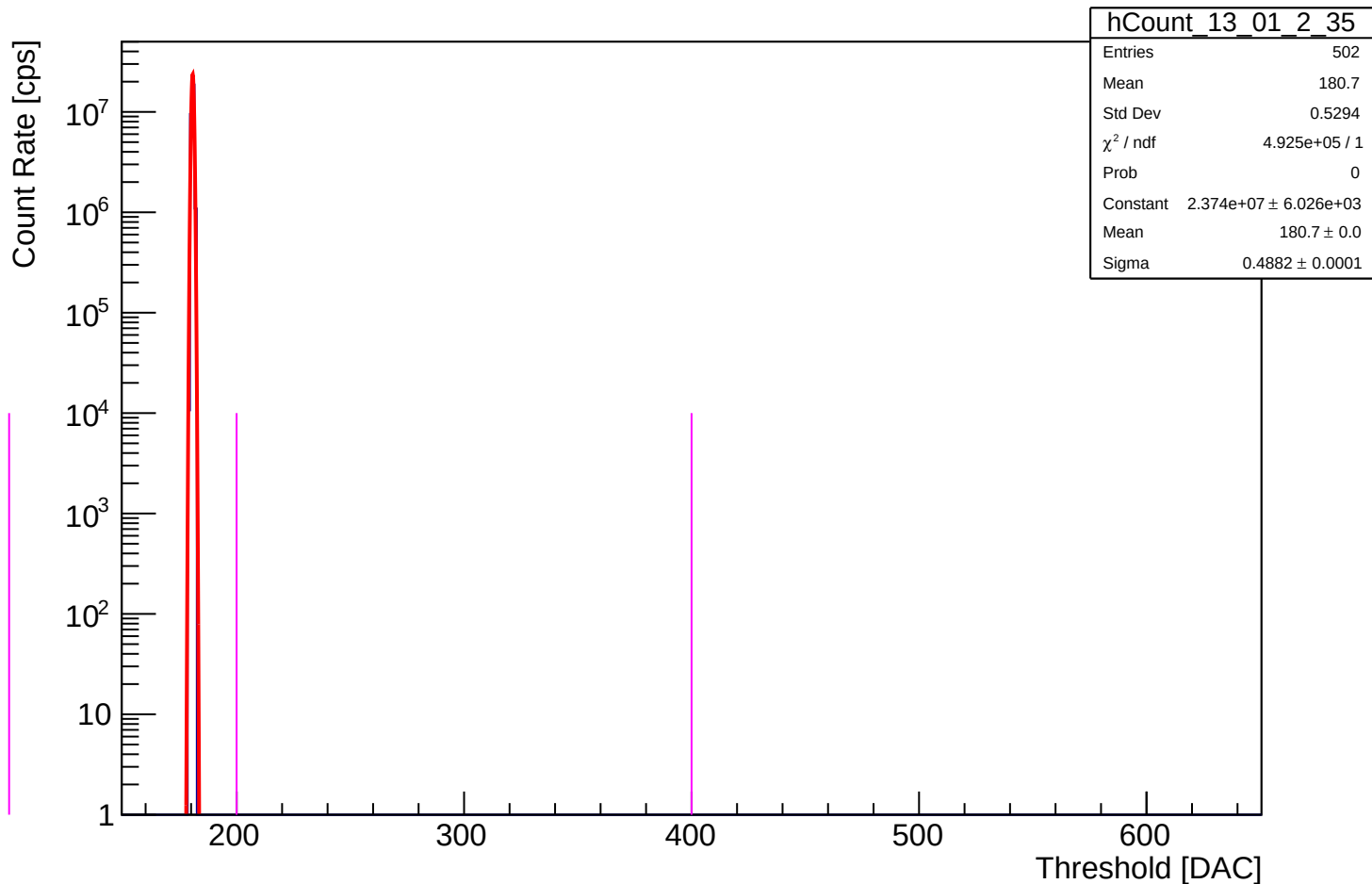
Row 1 Tile 1 Pmt 6 Pixel 6 Slot 13 Fiber 1 Asic 2 Channel 34



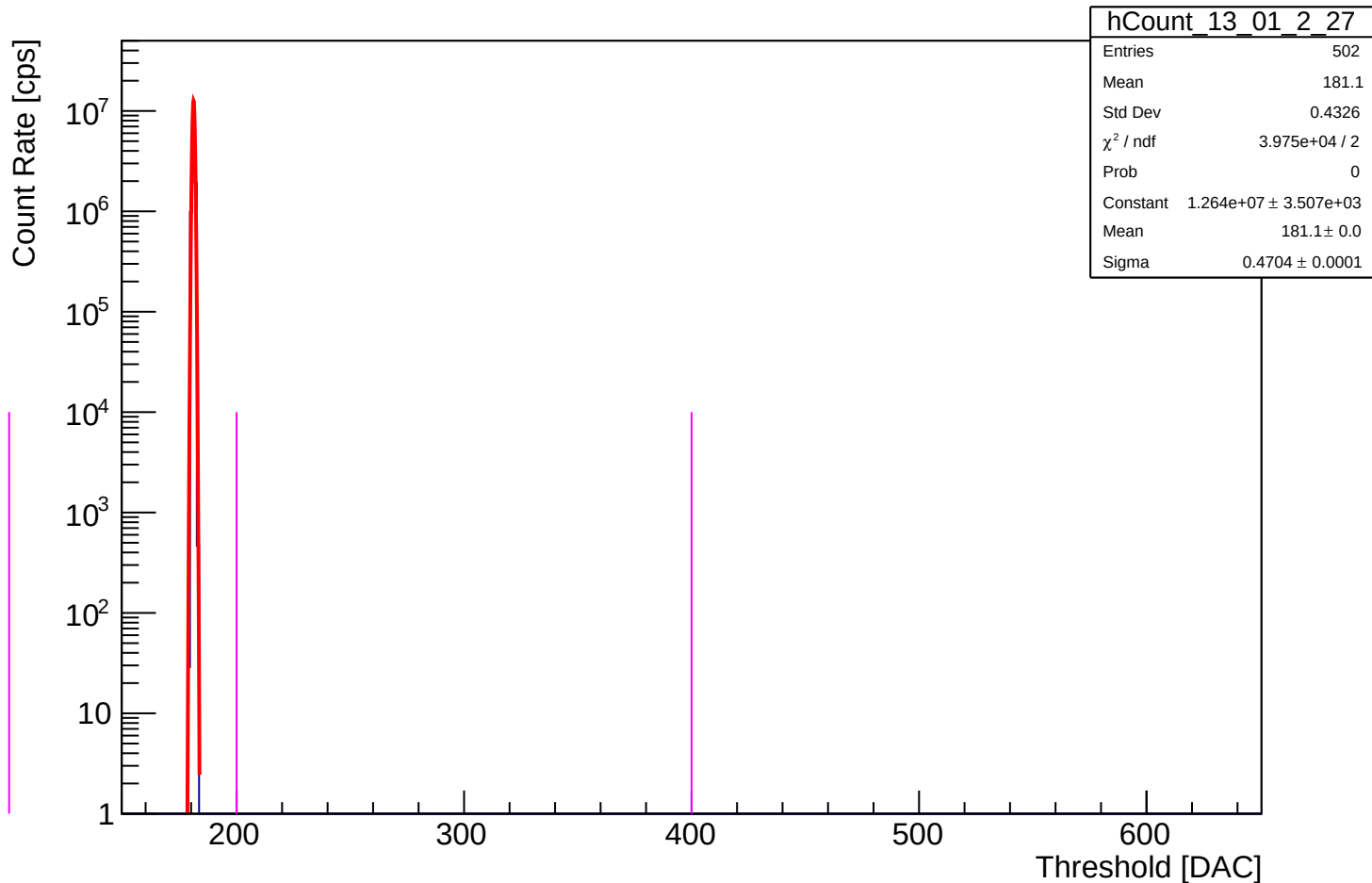
Row 1 Tile 1 Pmt 6 Pixel 7 Slot 13 Fiber 1 Asic 2 Channel 33



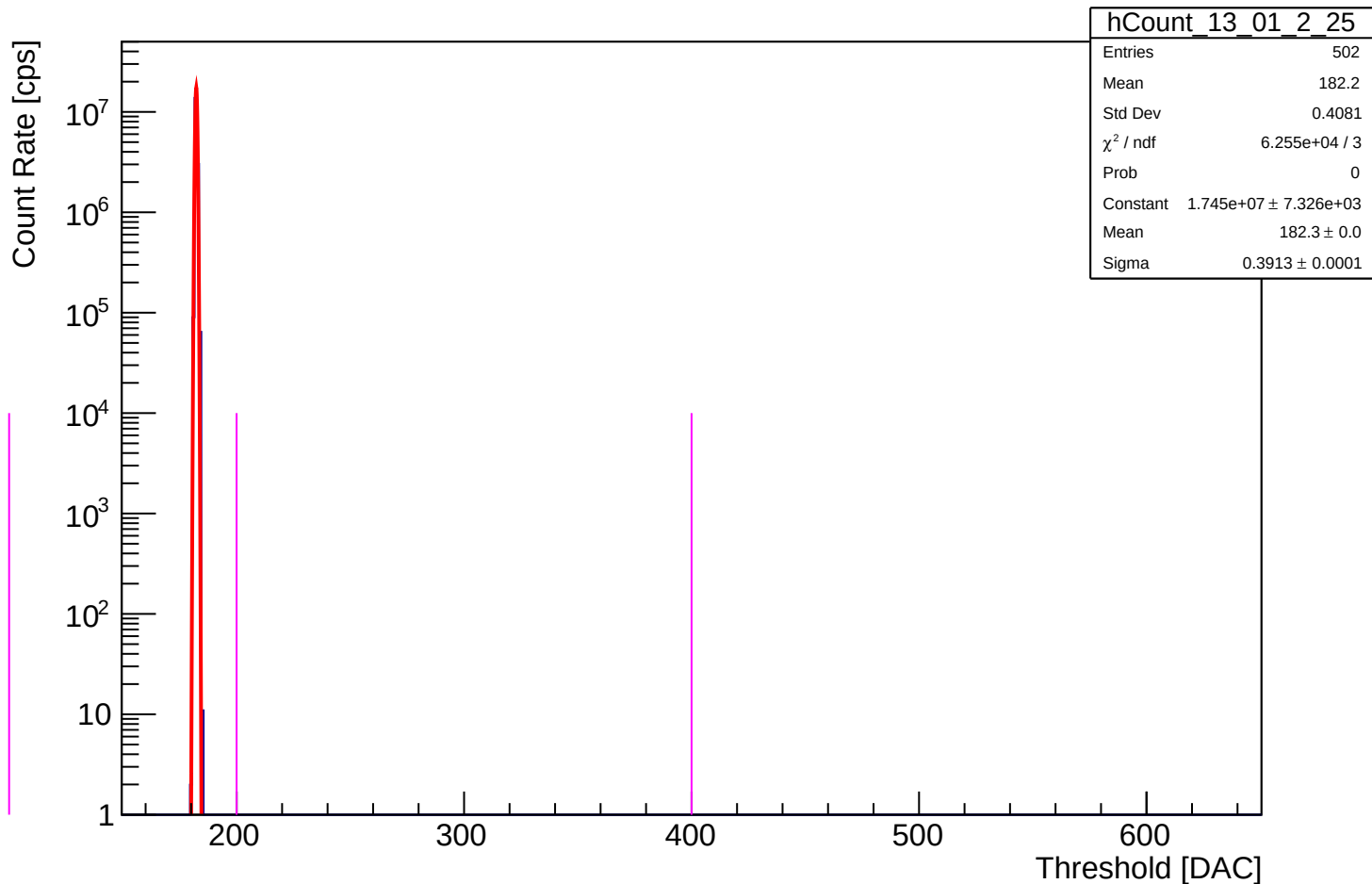
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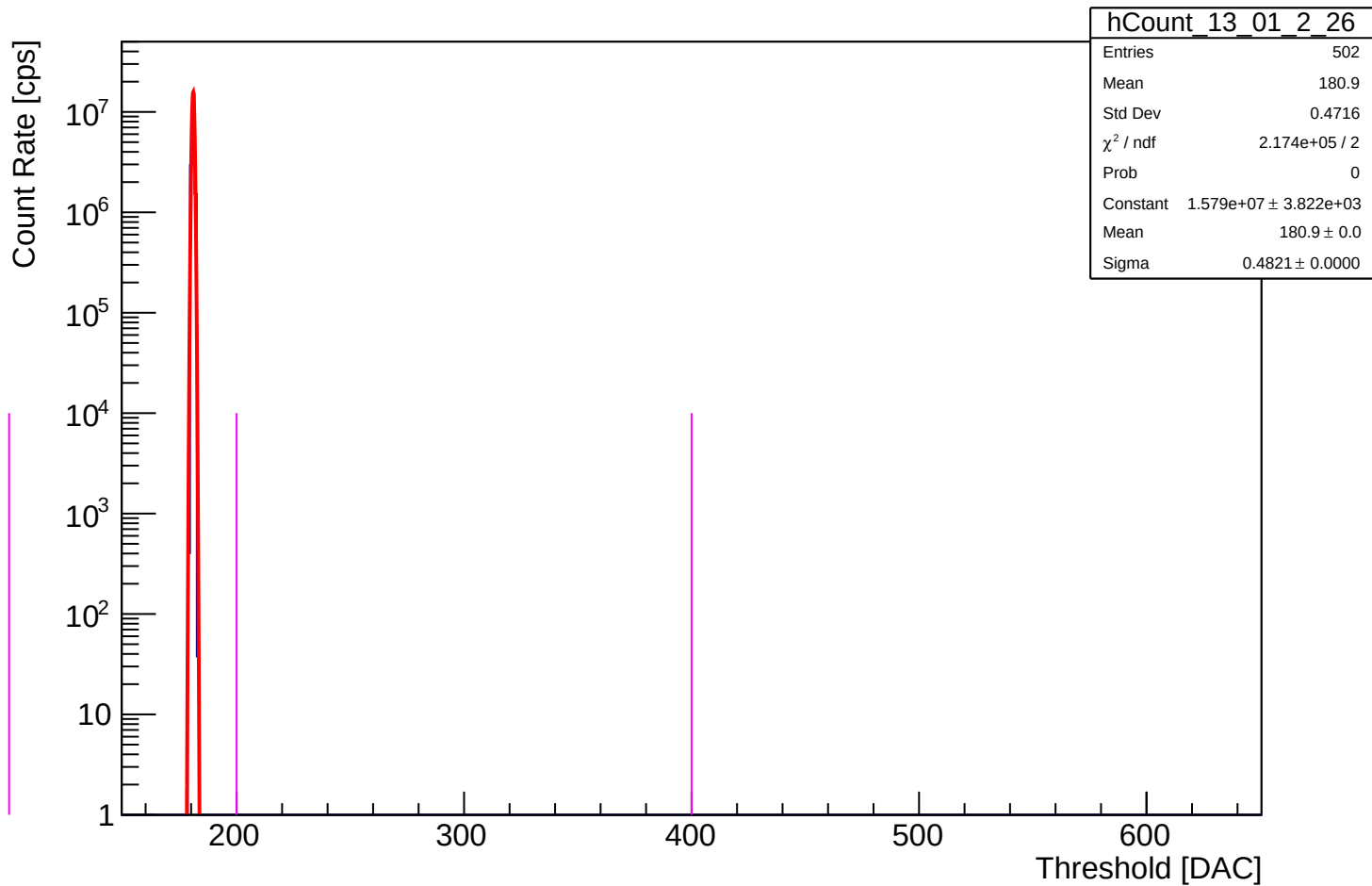
Row 1 Tile 1 Pmt 6 Pixel 9 Slot 13 Fiber 1 Asic 2 Channel 27



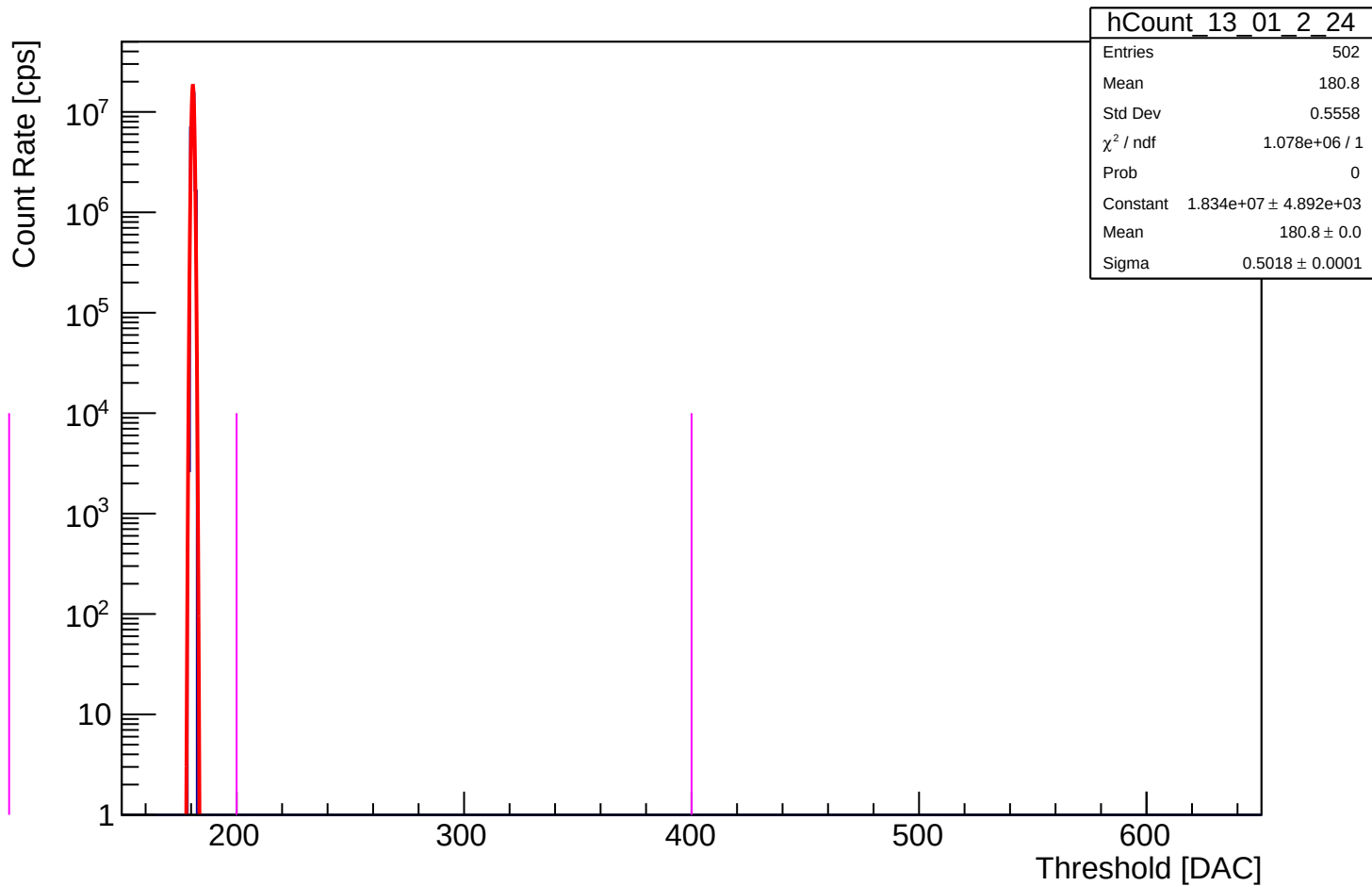
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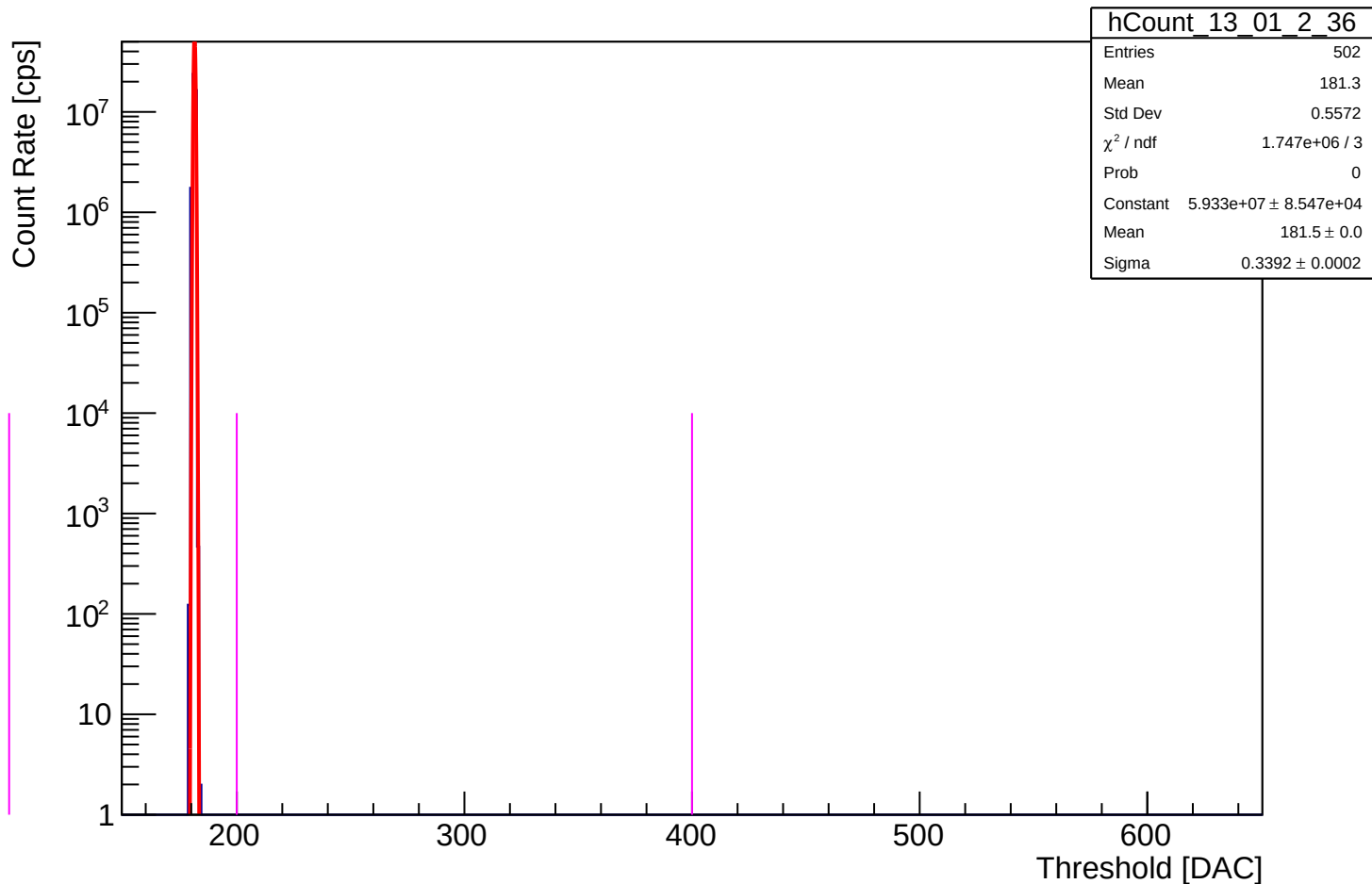
Row 1 Tile 1 Pmt 6 Pixel 11 Slot 13 Fiber 1 Asic 2 Channel 26



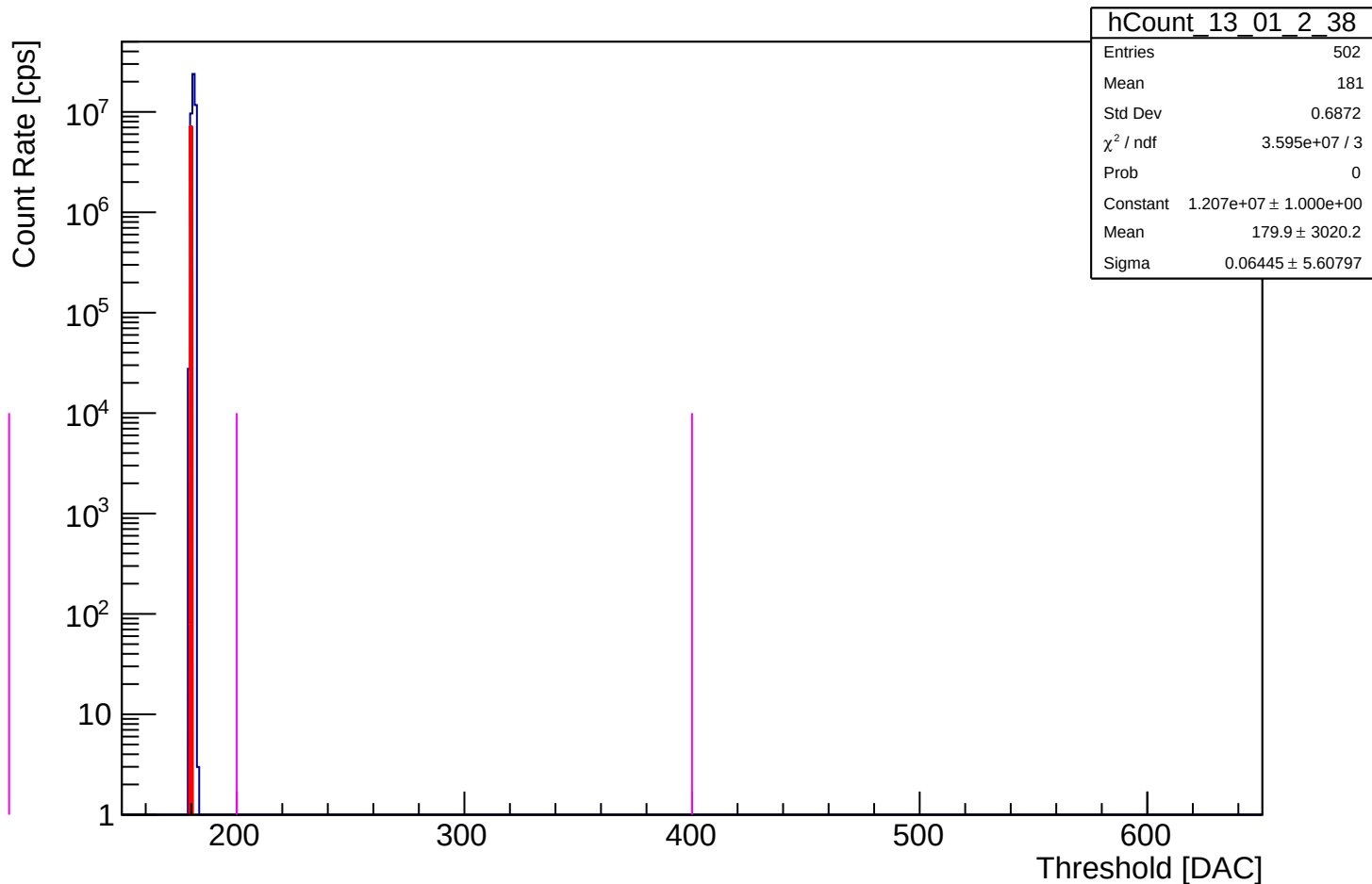
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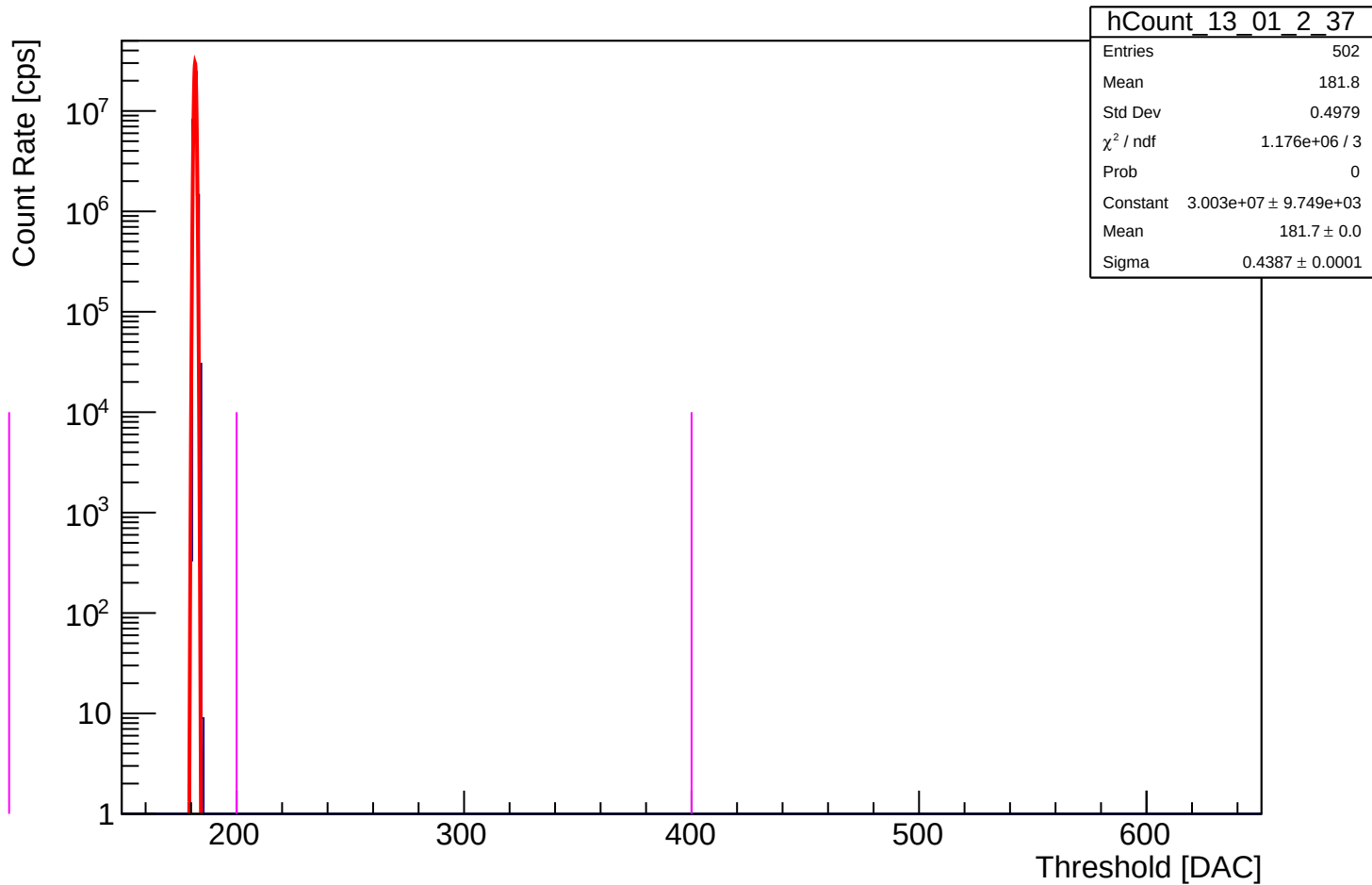
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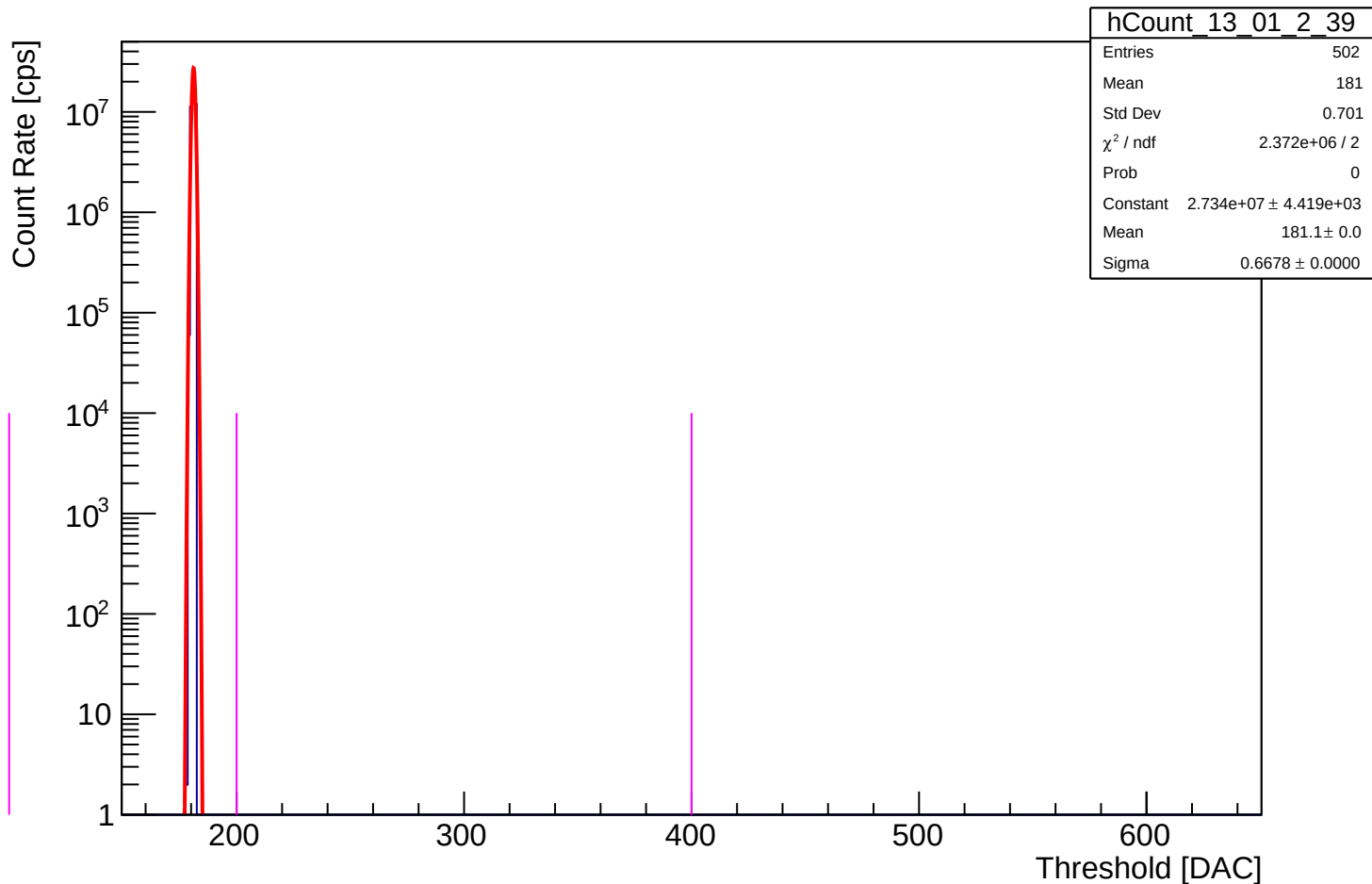
Row 1 Tile 1 Pmt 6 Pixel 14 Slot 13 Fiber 1 Asic 2 Channel 38



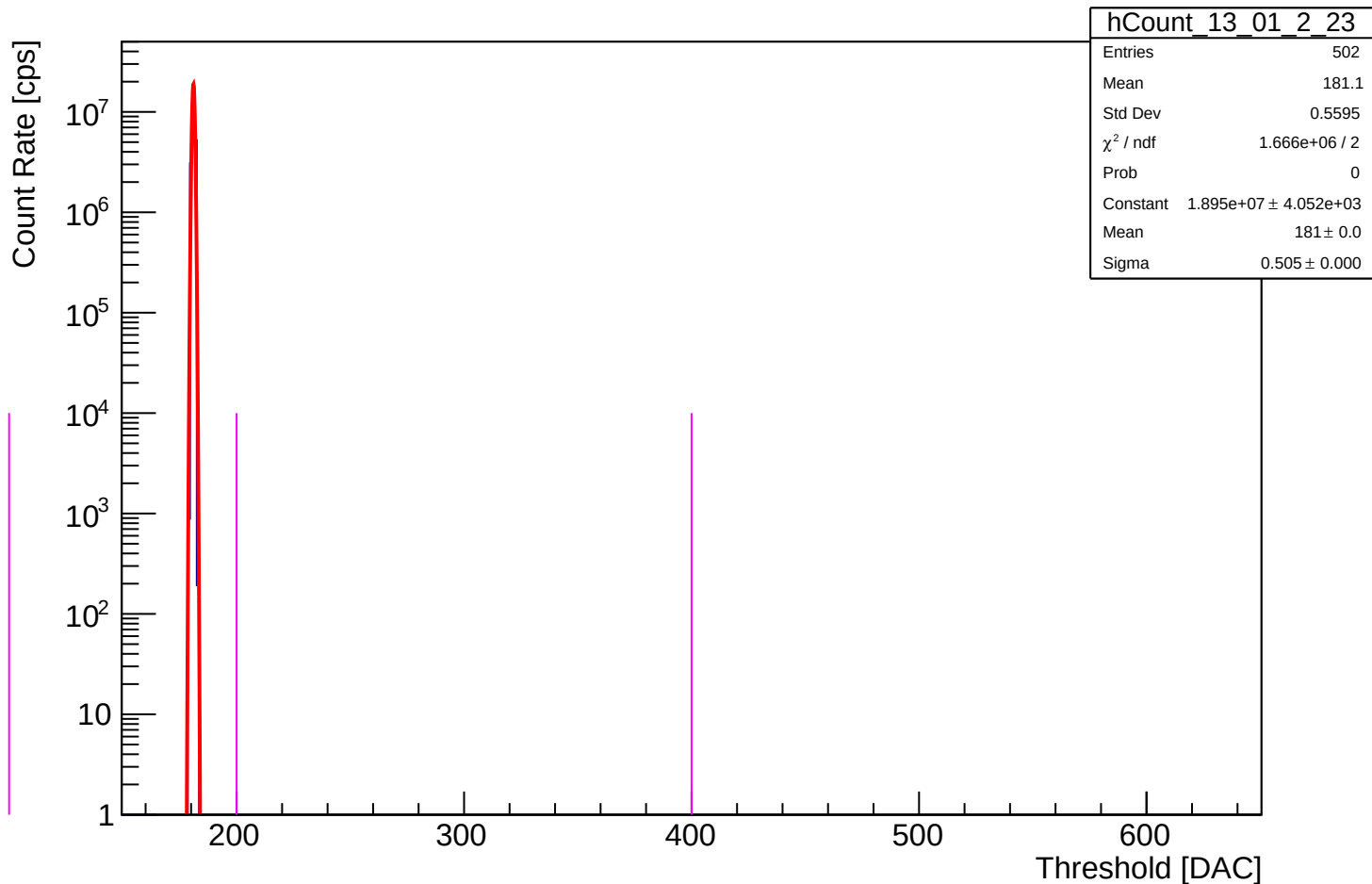
Row 1 Tile 1 Pmt 6 Pixel 15 Slot 13 Fiber 1 Asic 2 Channel 37



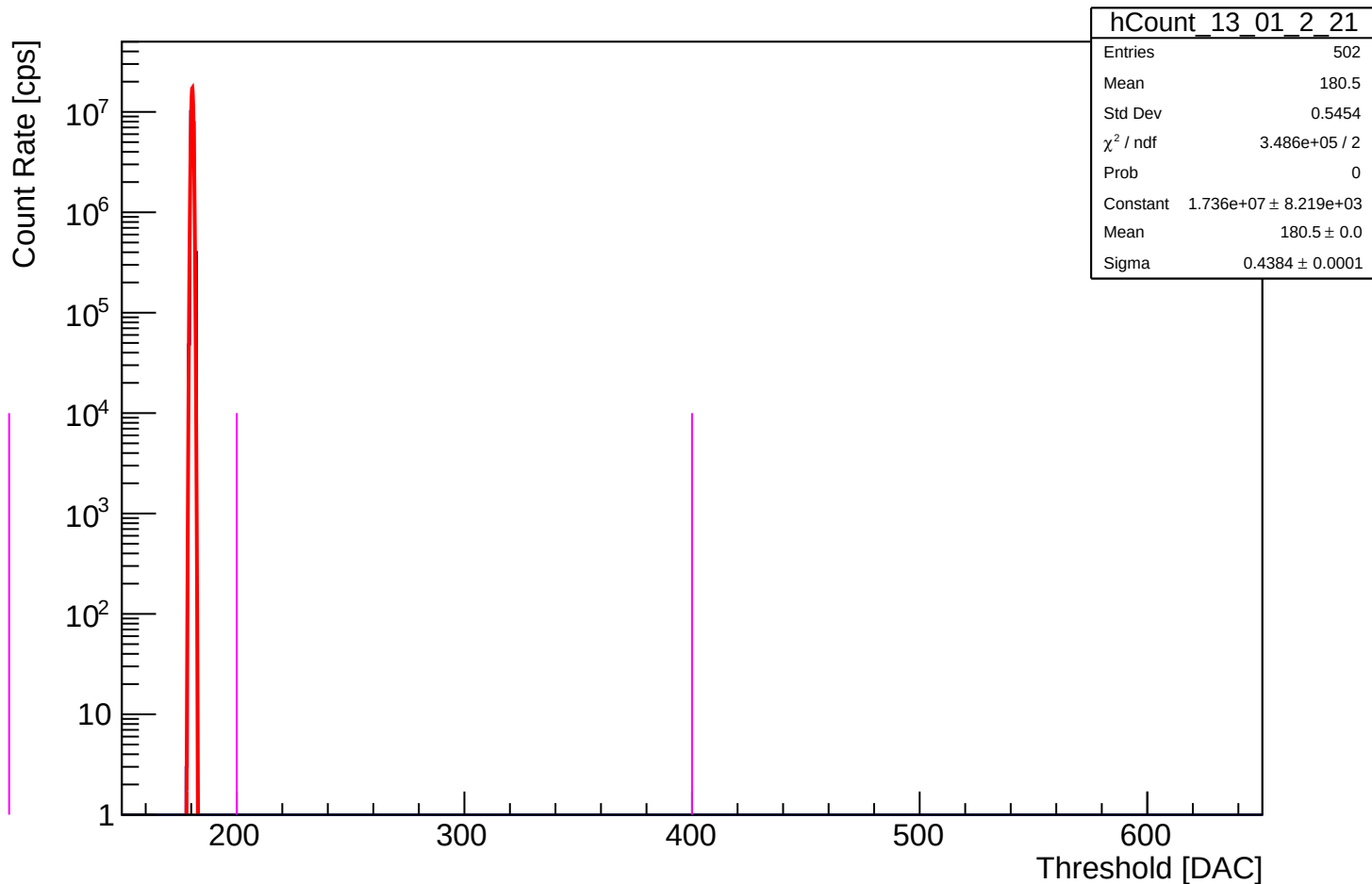
Row 1 Tile 1 Pmt 6 Pixel 16 Slot 13 Fiber 1 Asic 2 Channel 39



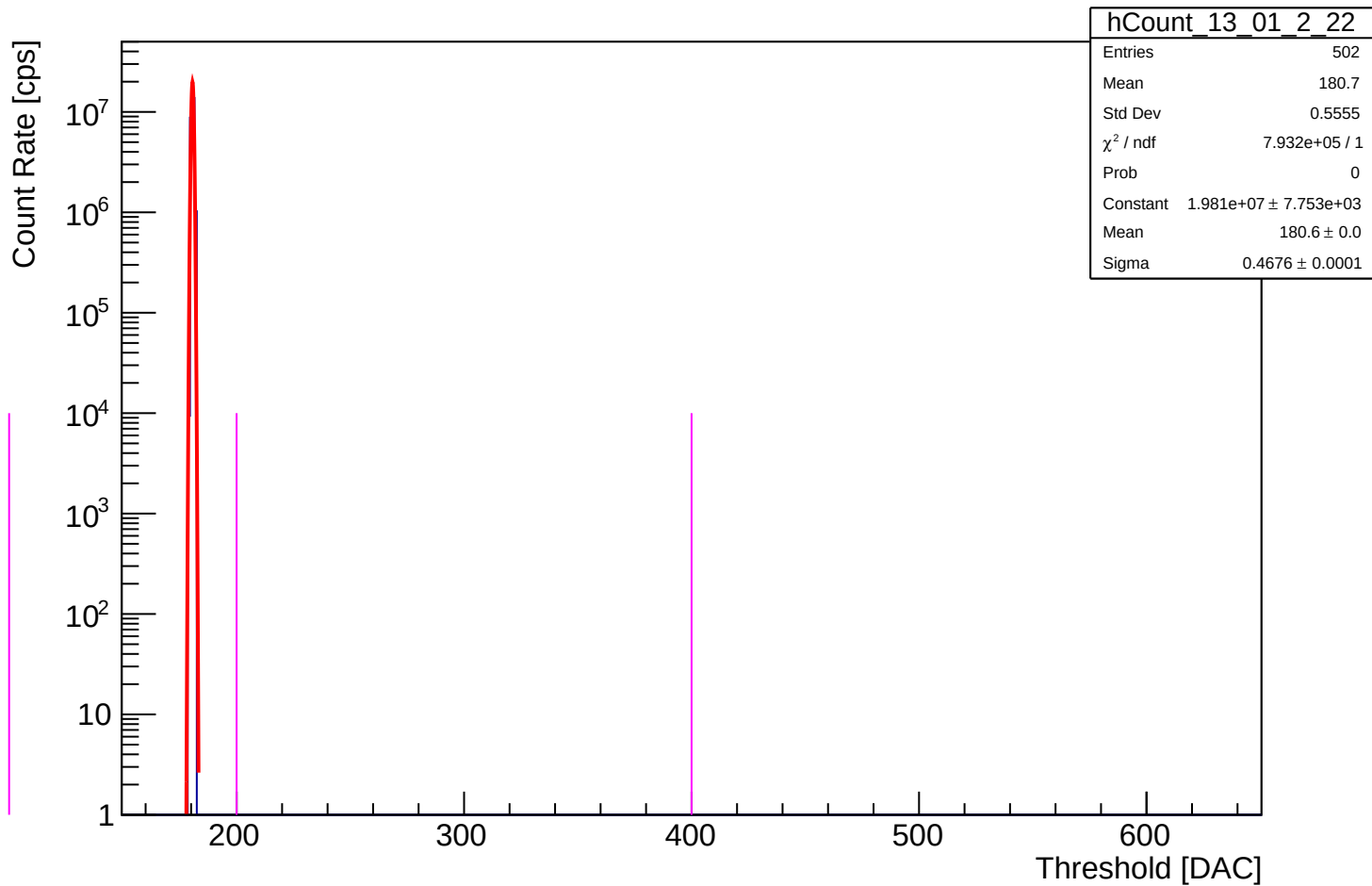
Row 1 Tile 1 Pmt 6 Pixel 17 Slot 13 Fiber 1 Asic 2 Channel 23



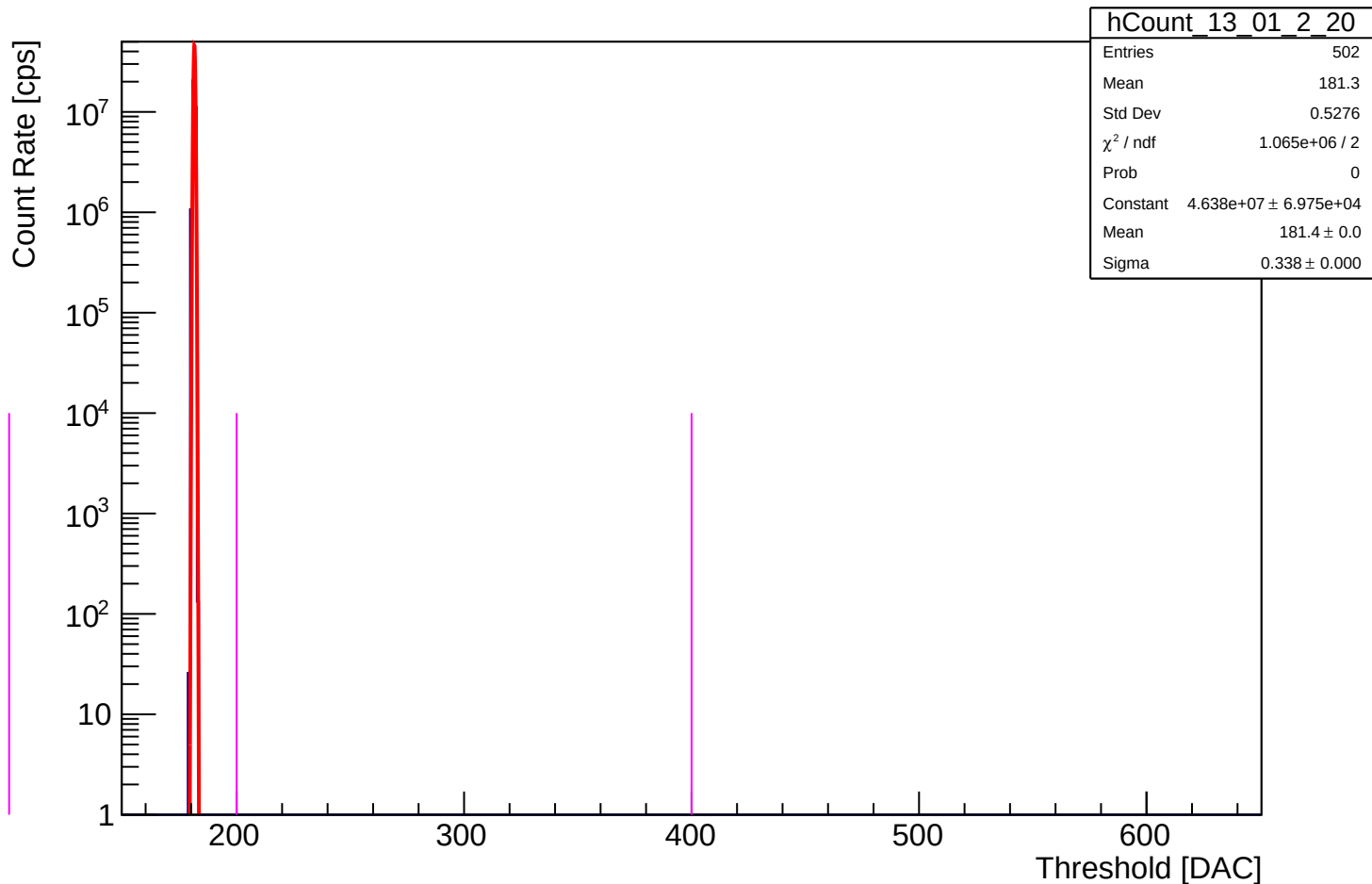
Row 1 Tile 1 Pmt 6 Pixel 18 Slot 13 Fiber 1 Asic 2 Channel 21



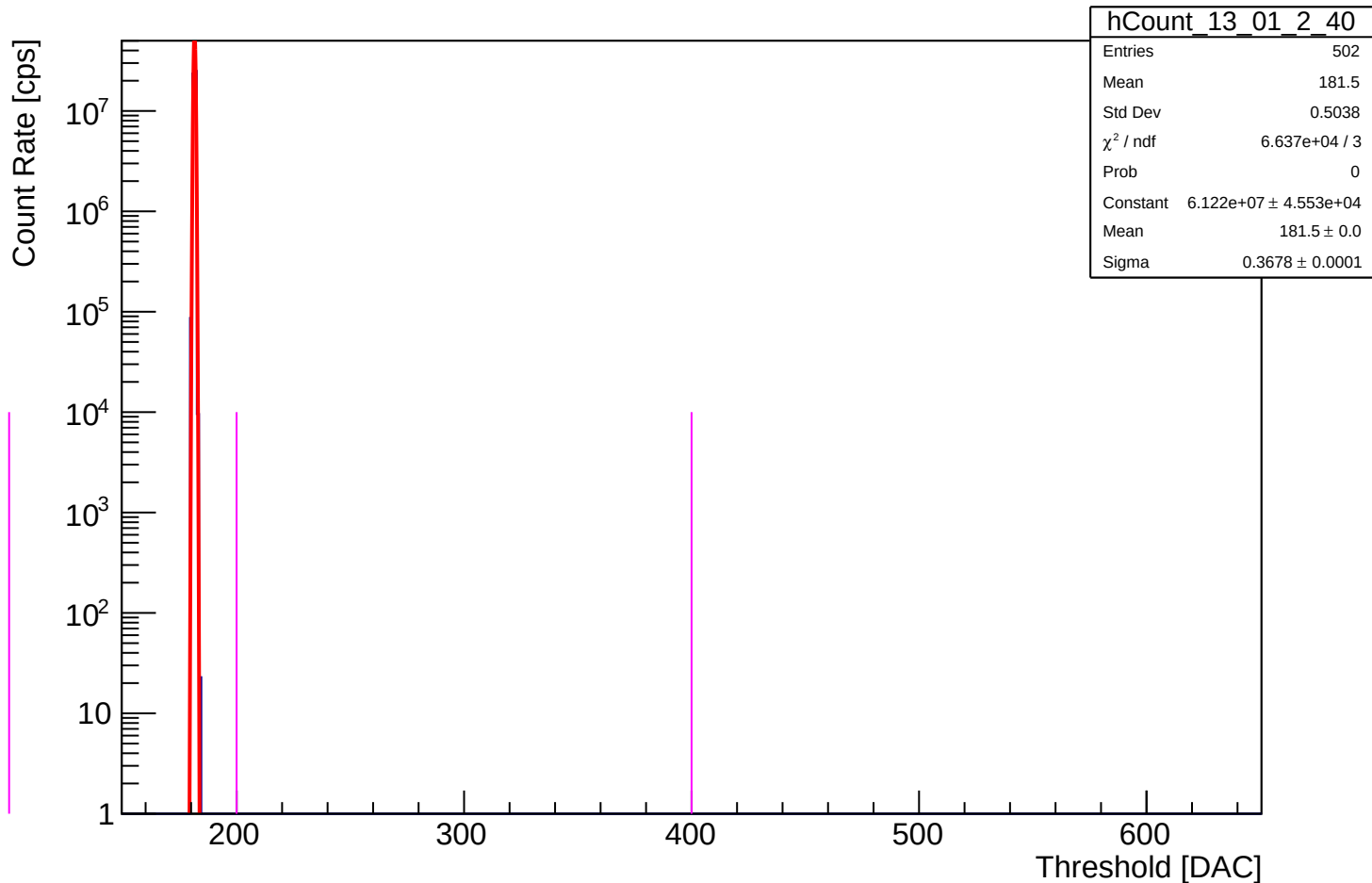
Row 1 Tile 1 Pmt 6 Pixel 19 Slot 13 Fiber 1 Asic 2 Channel 22



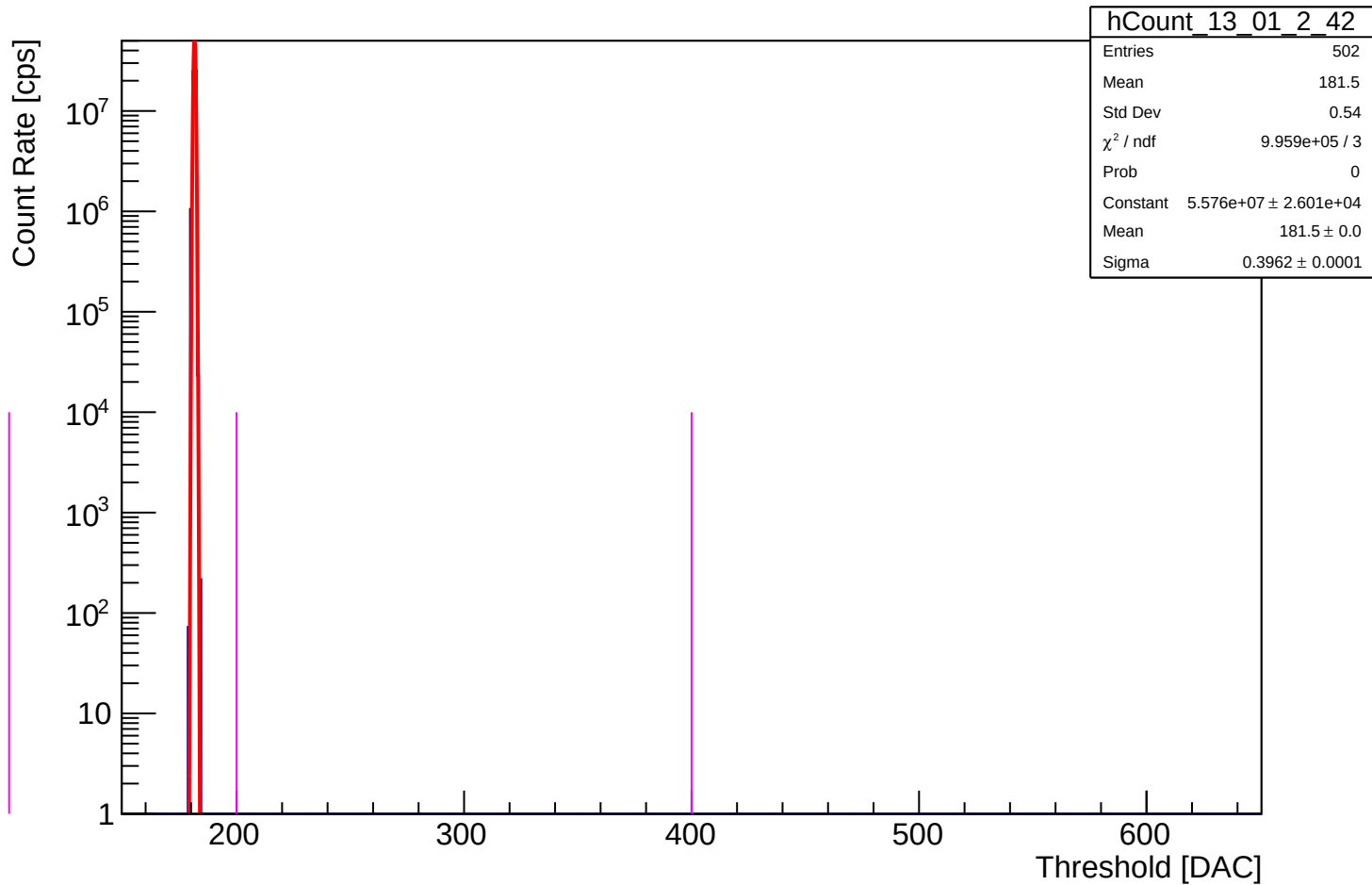
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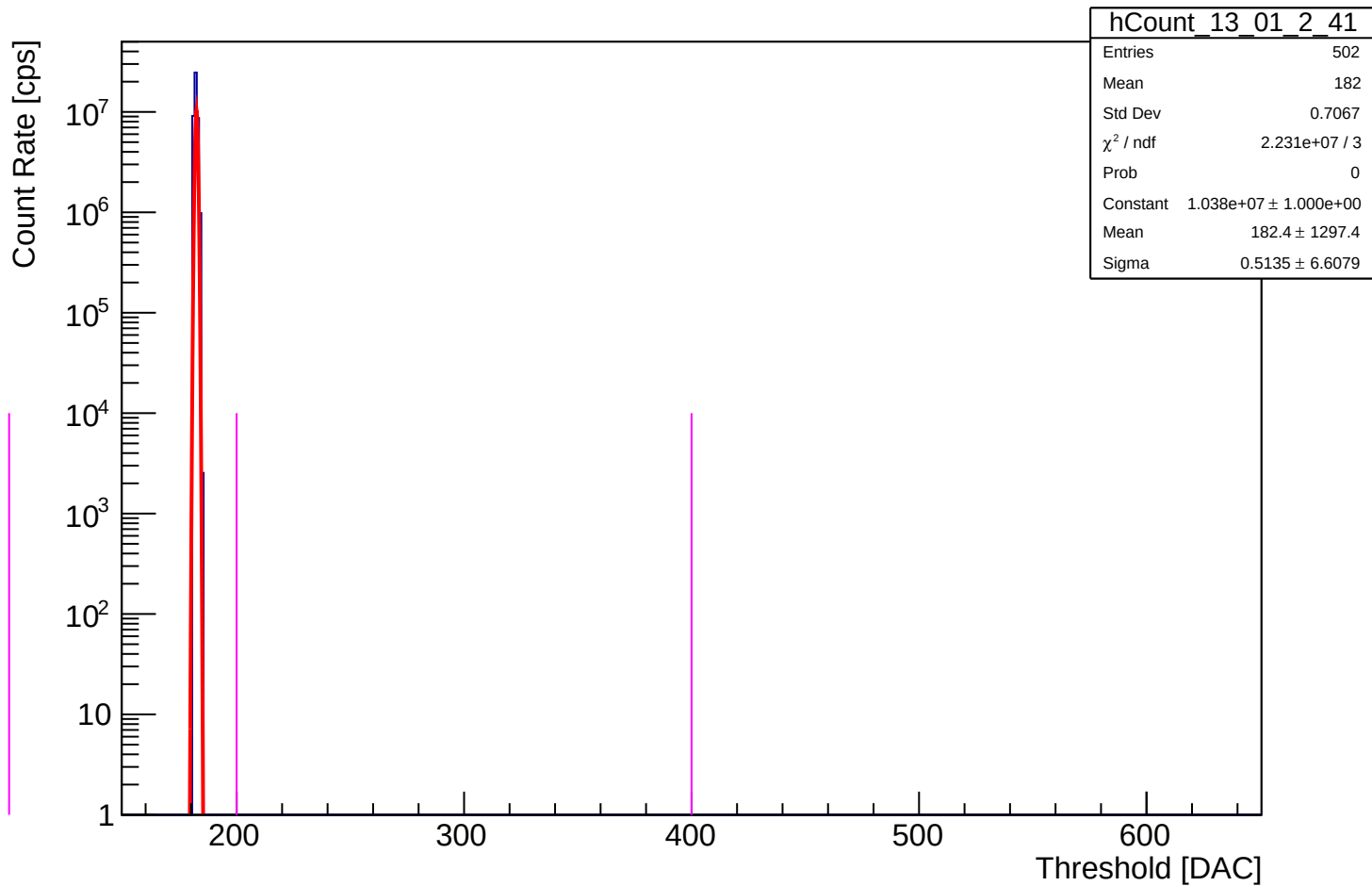
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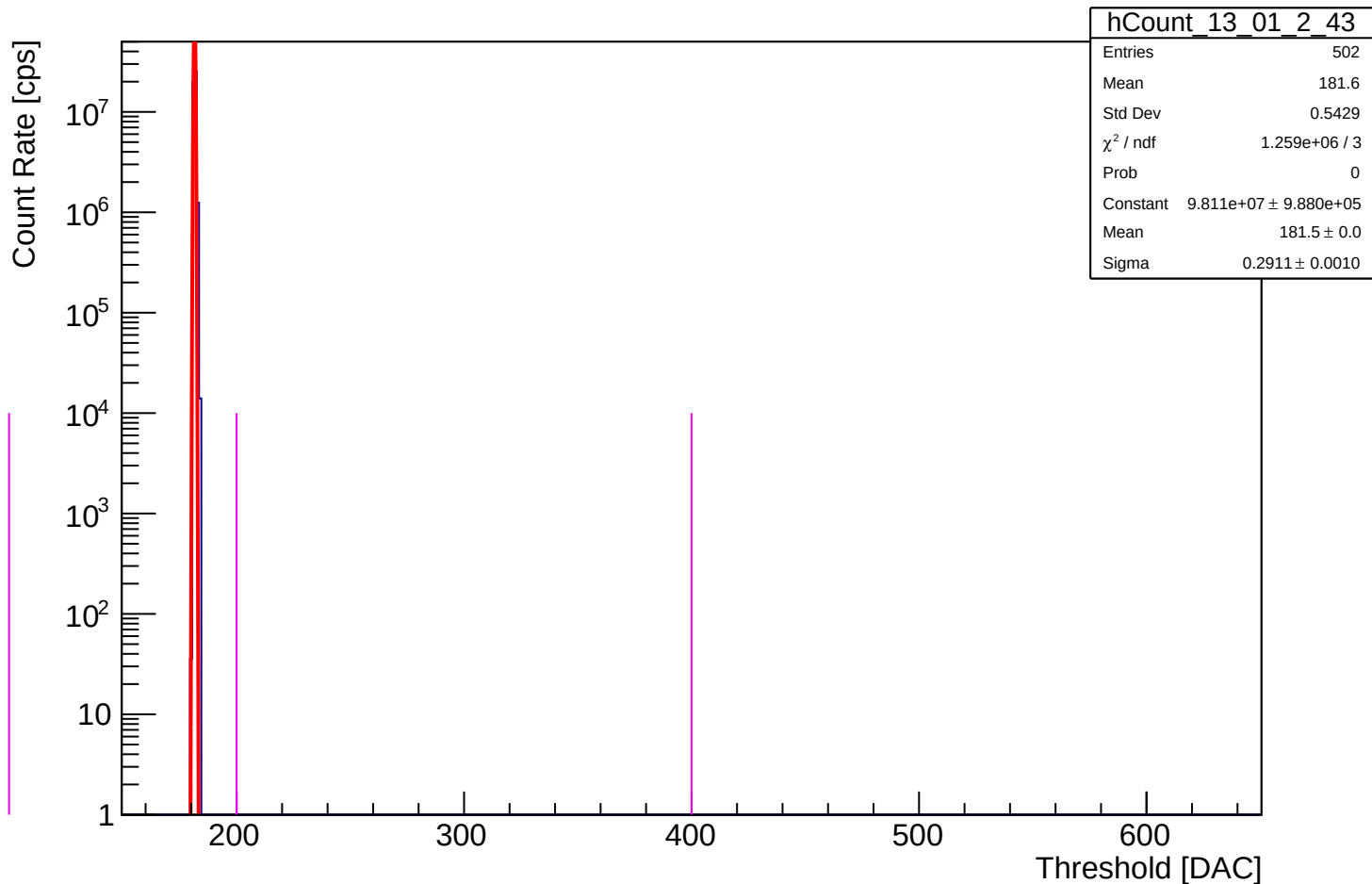
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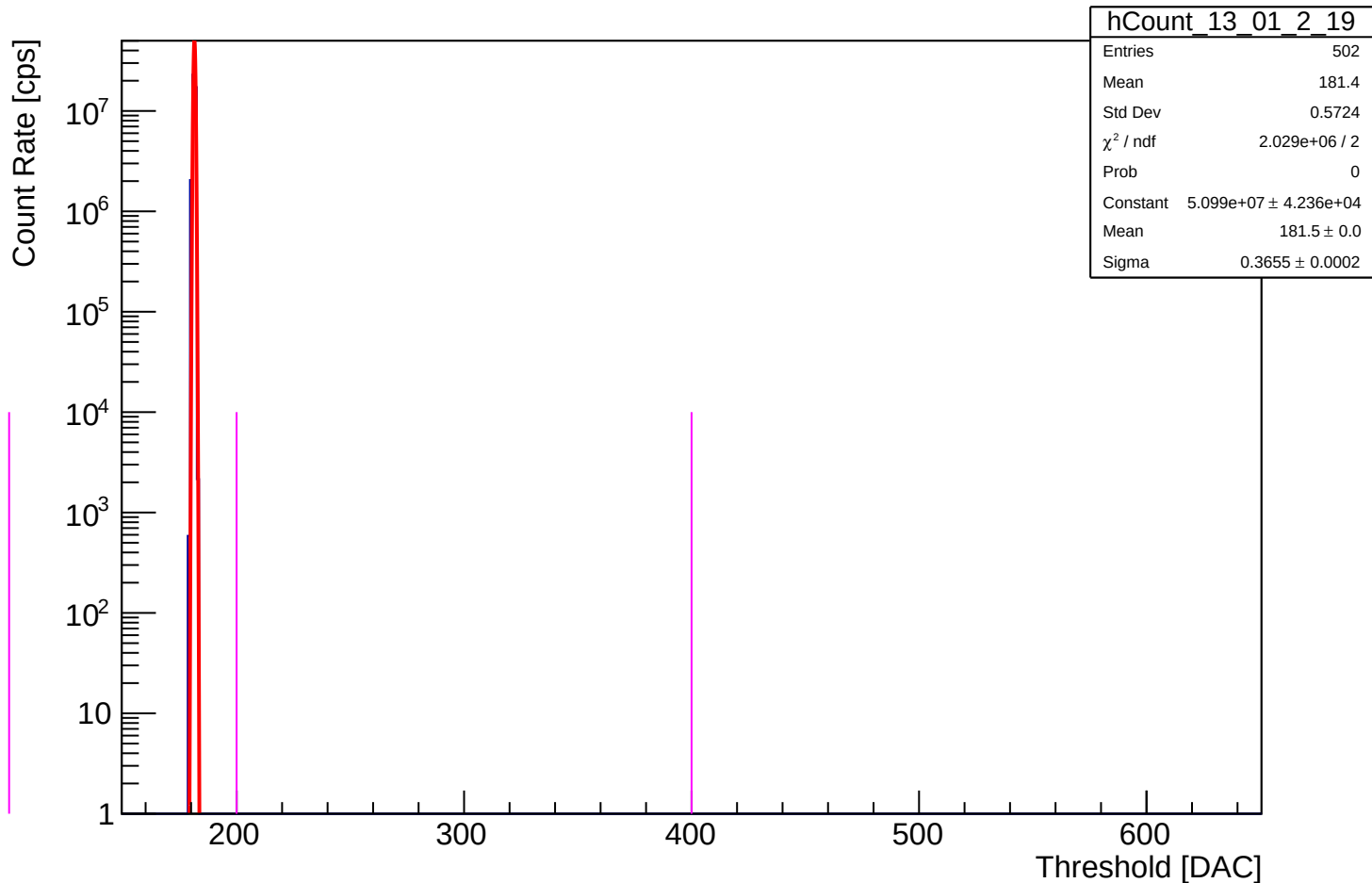
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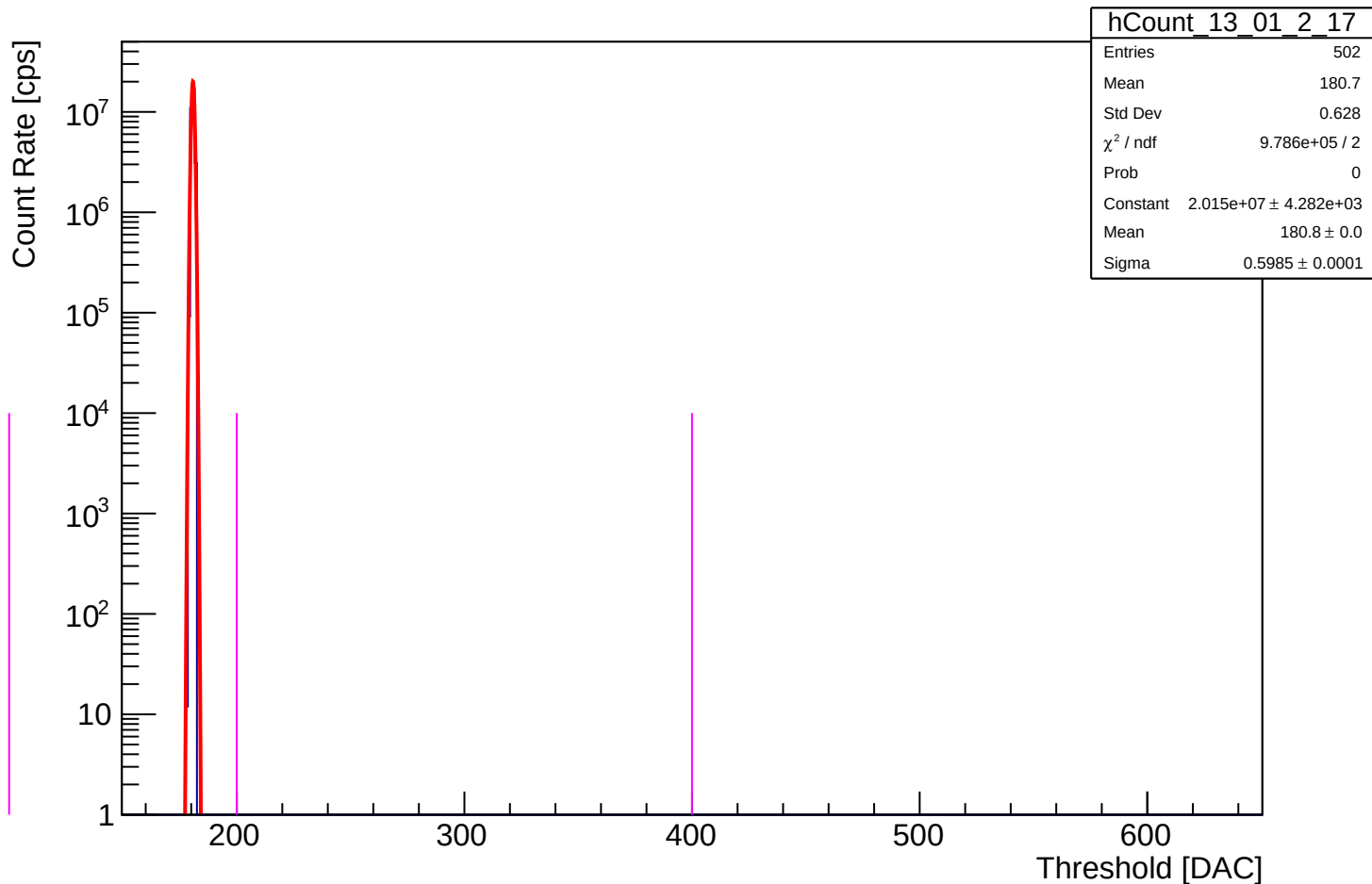


Row 1 Tile 1 Pmt 6 Pixel 24 Slot 13 Fiber 1 Asic 2 Channel 43

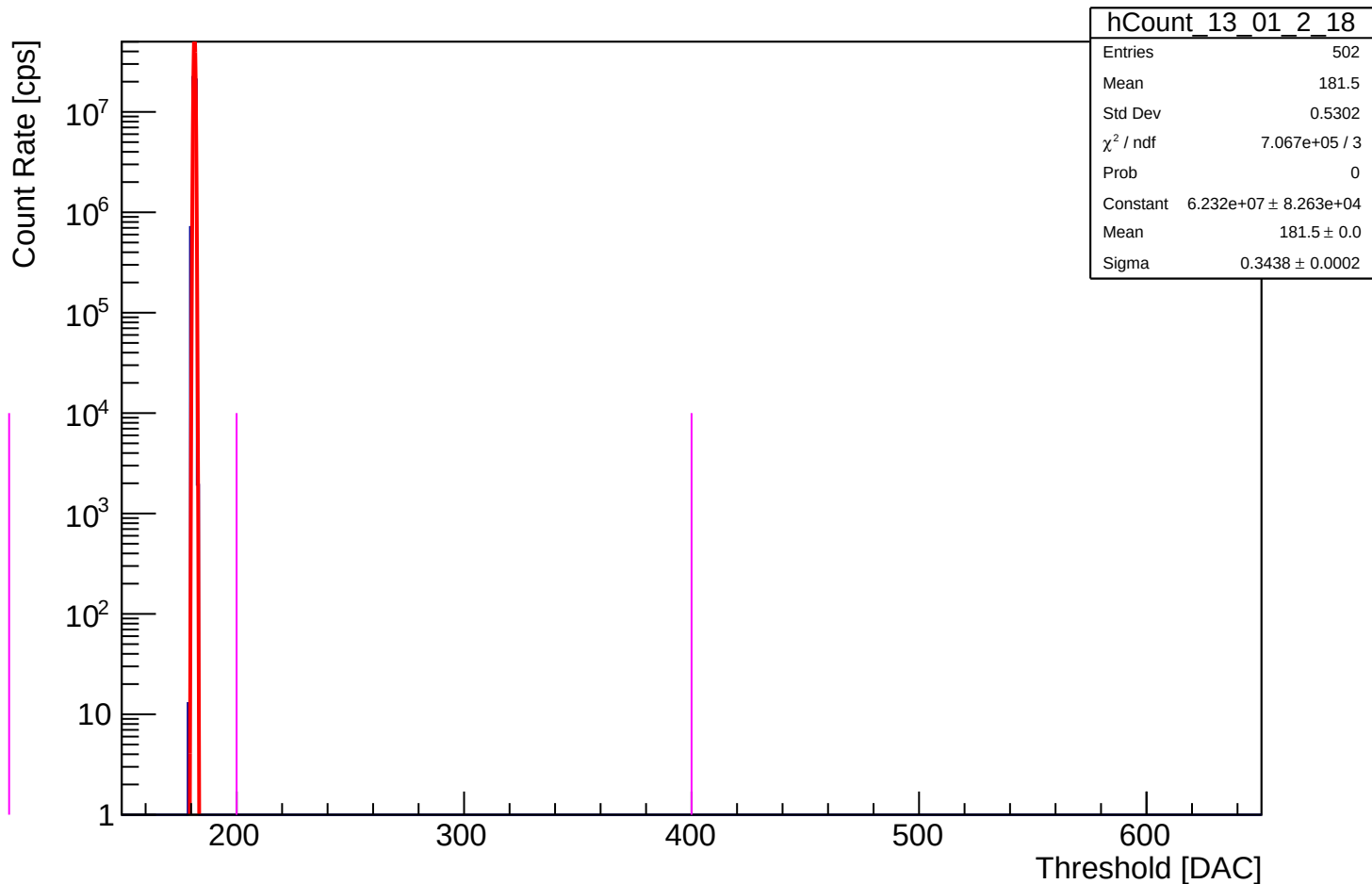


Row 1 Tile 1 Pmt 6 Pixel 25 Slot 13 Fiber 1 Asic 2 Channel 19

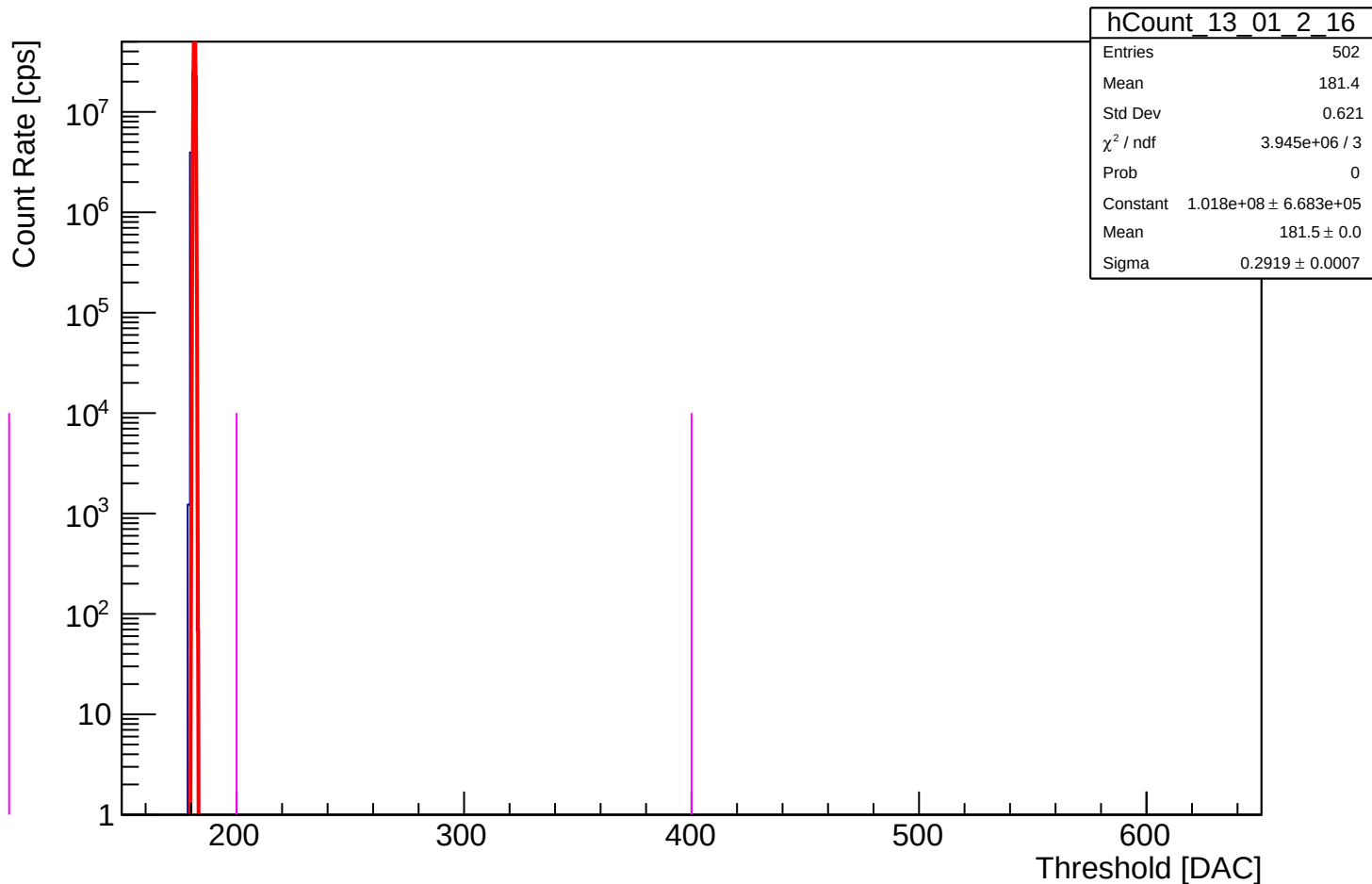




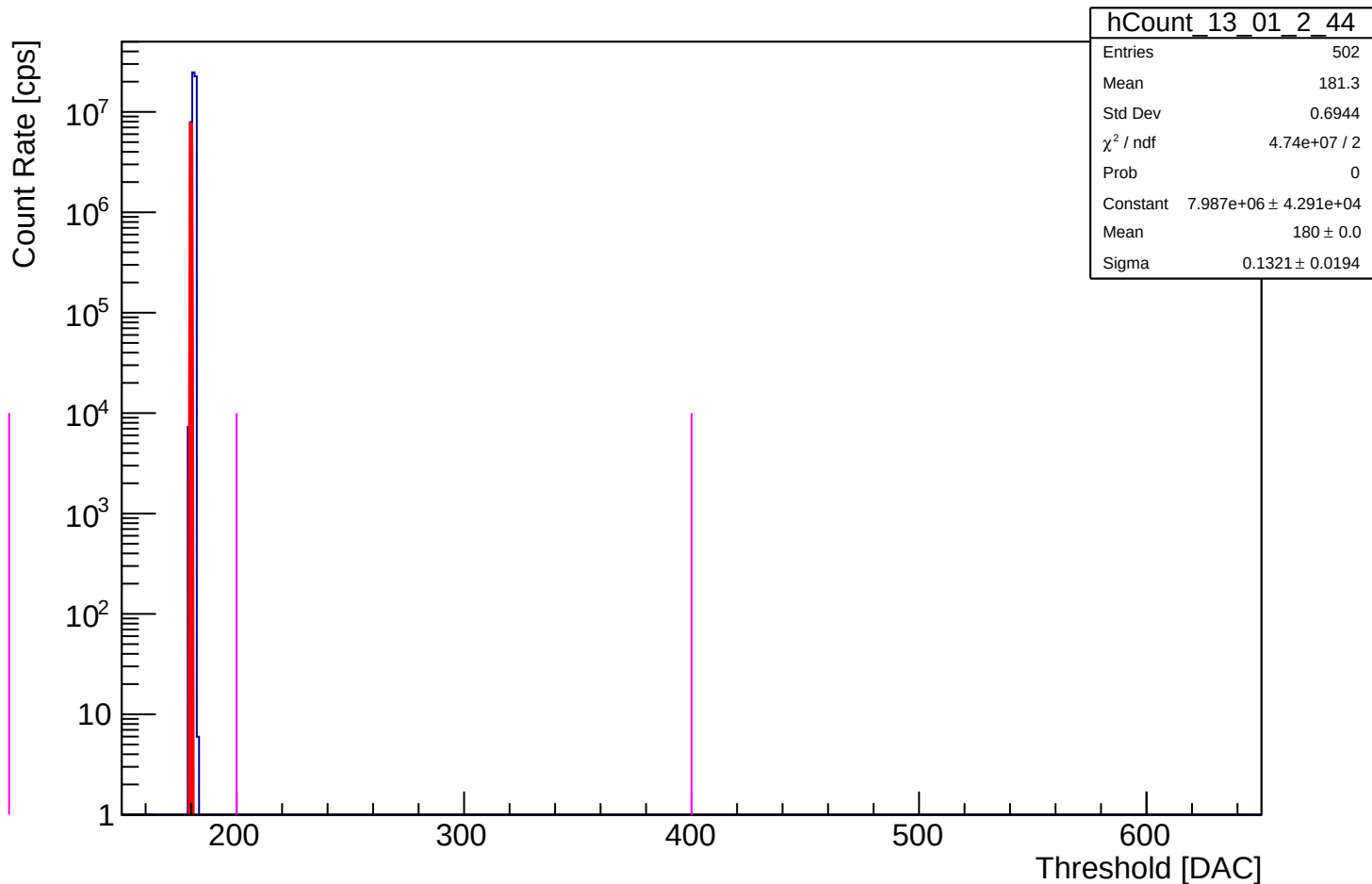
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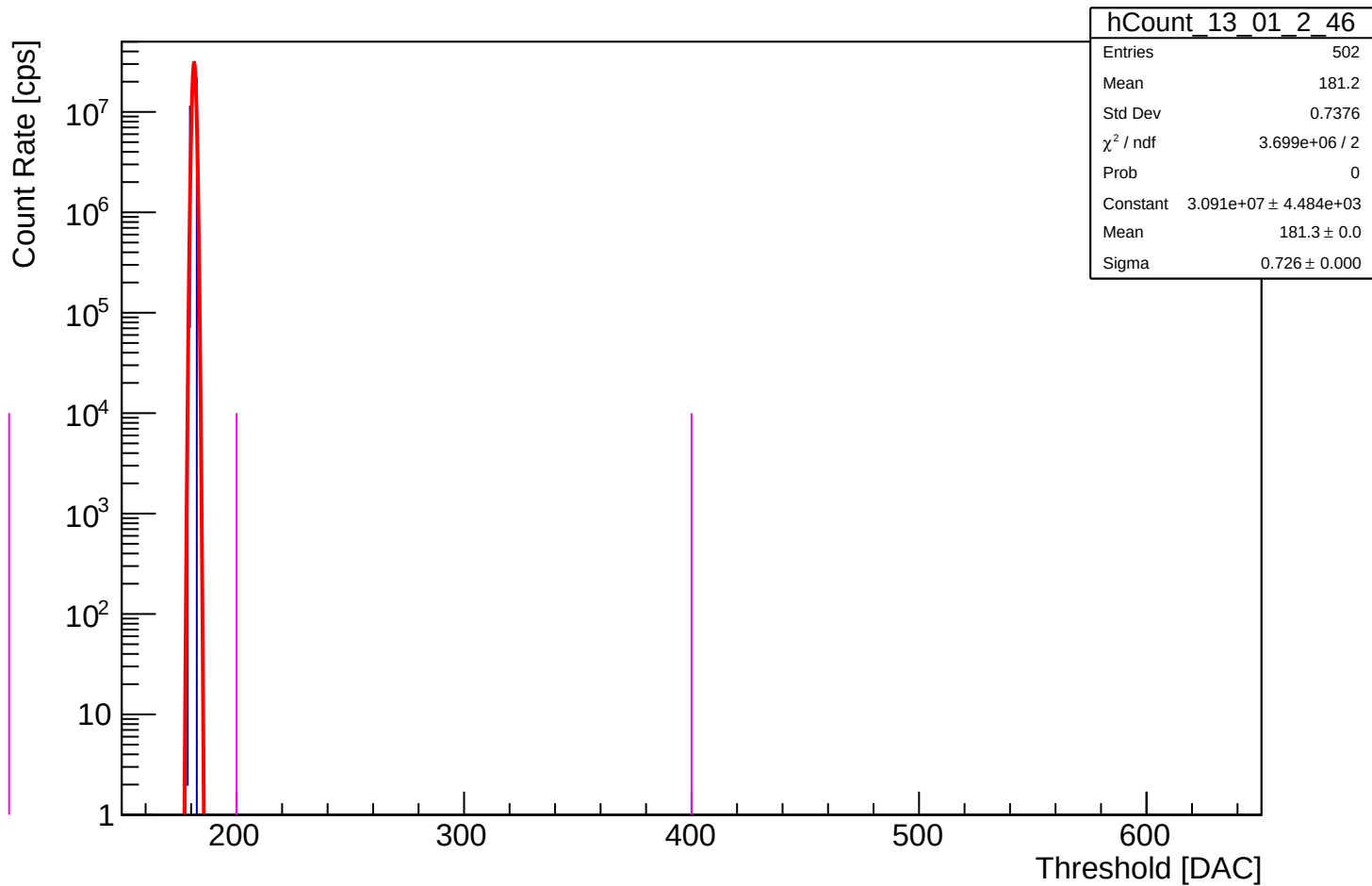
Row 1 Tile 1 Pmt 6 Pixel 28 Slot 13 Fiber 1 Asic 2 Channel 16



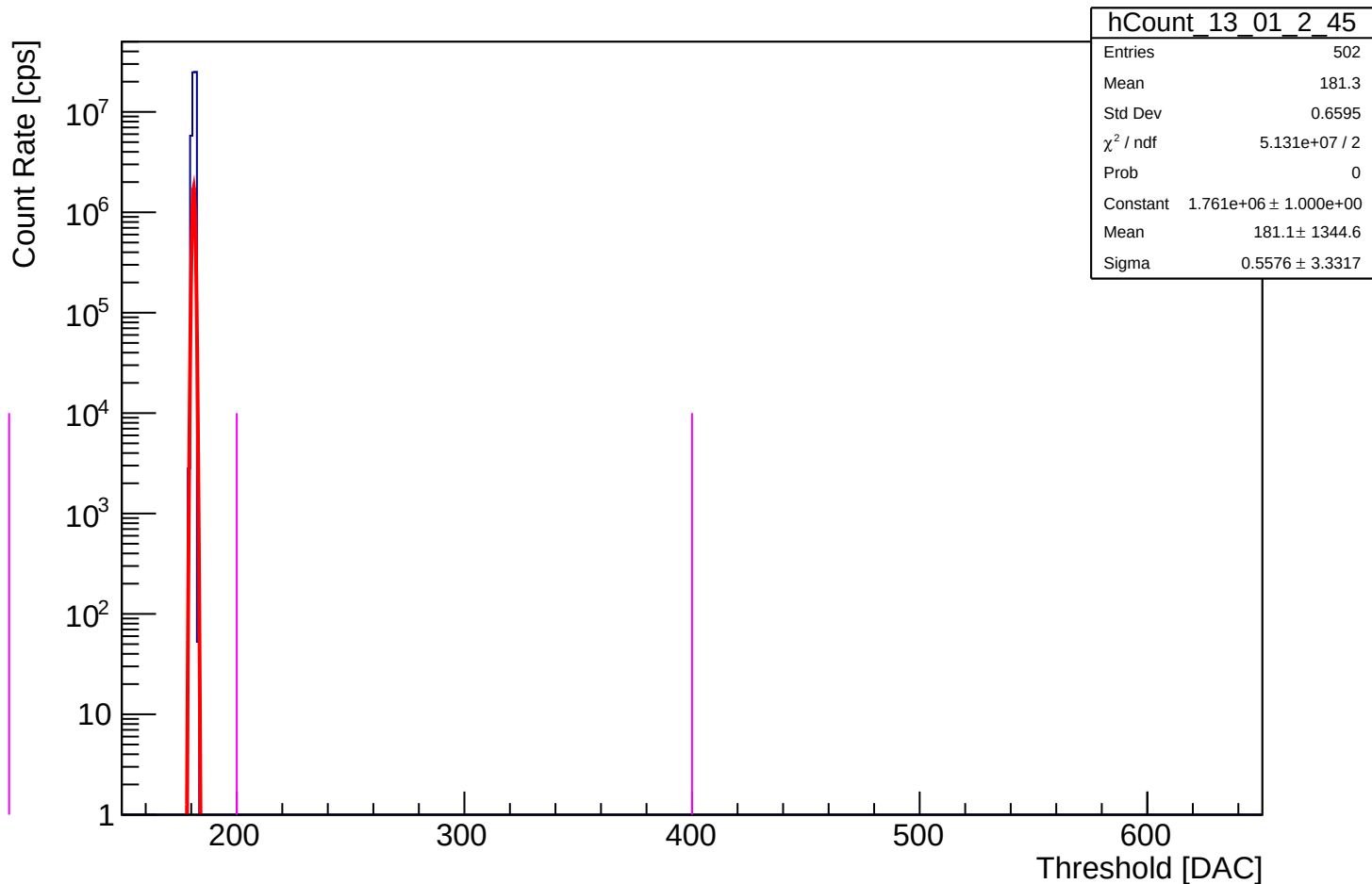
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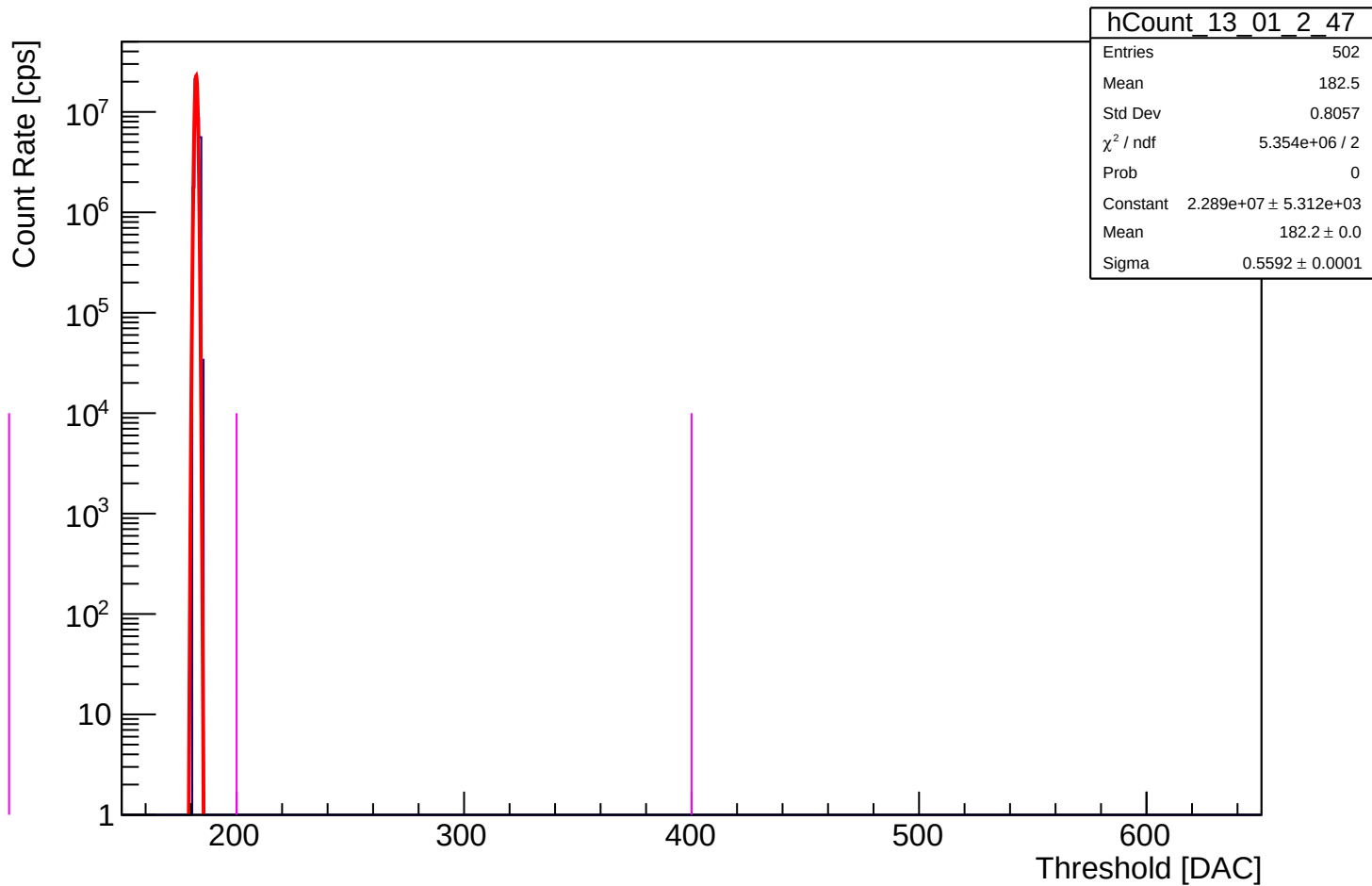
Row 1 Tile 1 Pmt 6 Pixel 30 Slot 13 Fiber 1 Asic 2 Channel 46



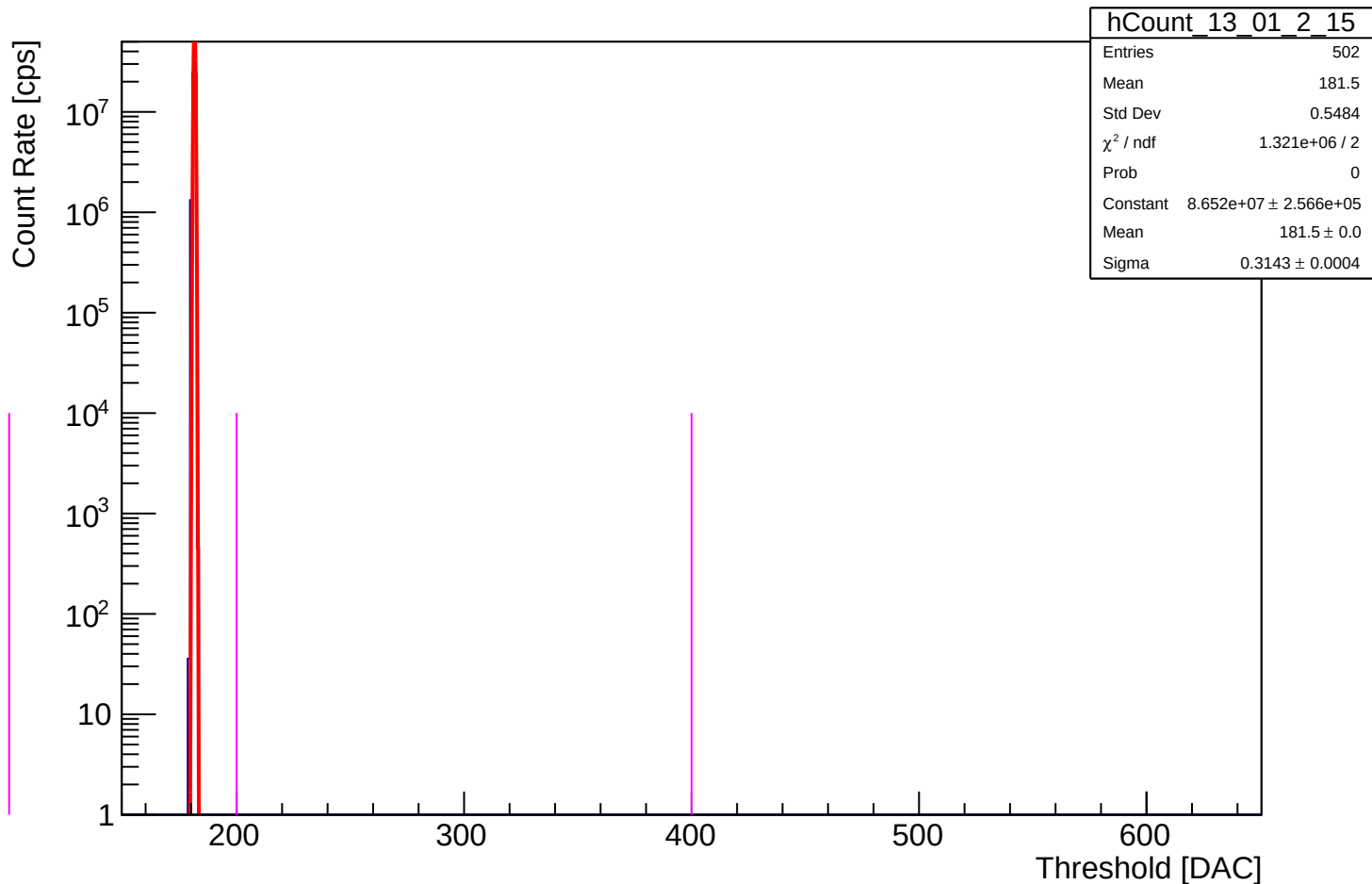
Row 1 Tile 1 Pmt 6 Pixel 31 Slot 13 Fiber 1 Asic 2 Channel 45



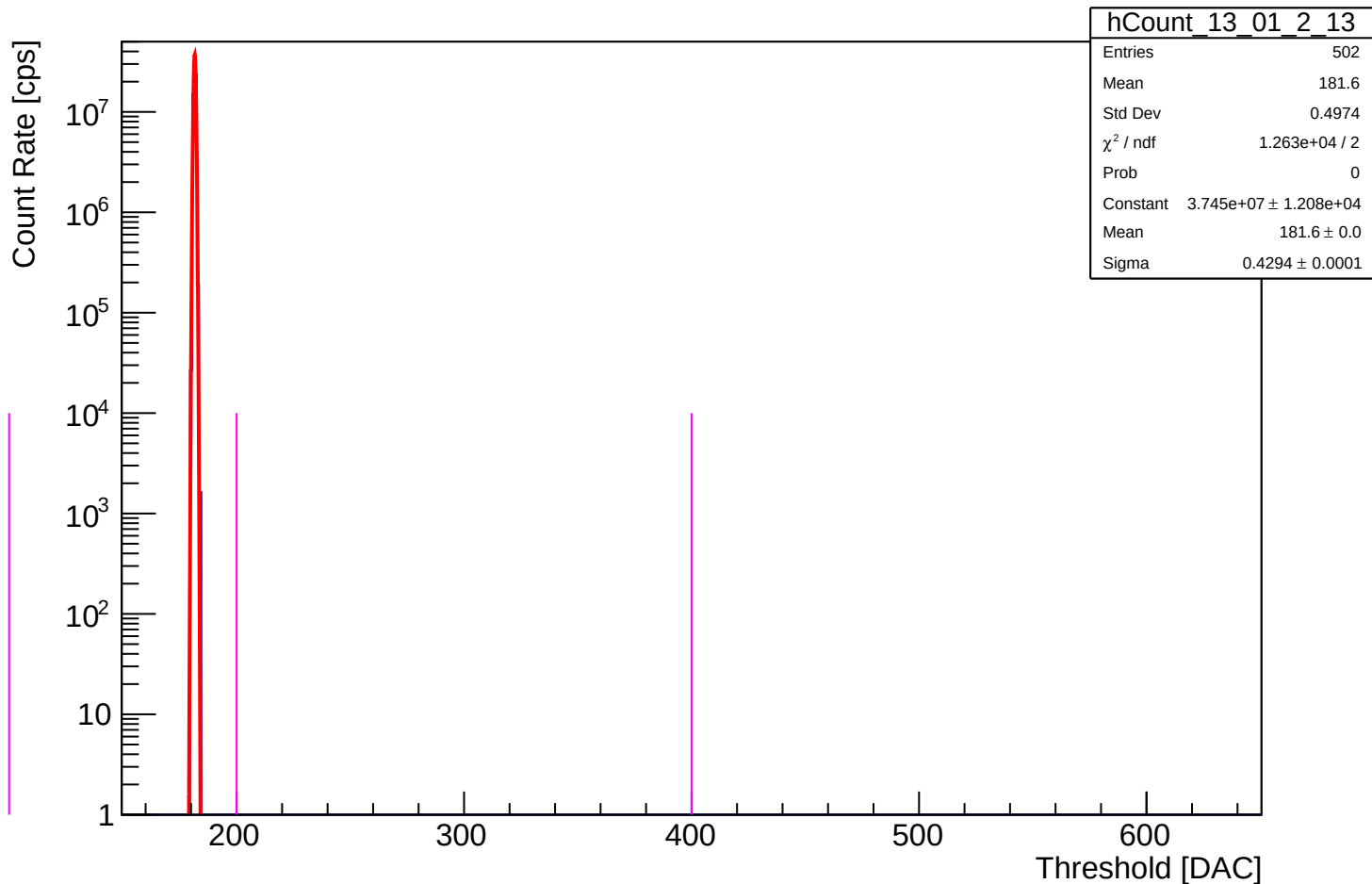
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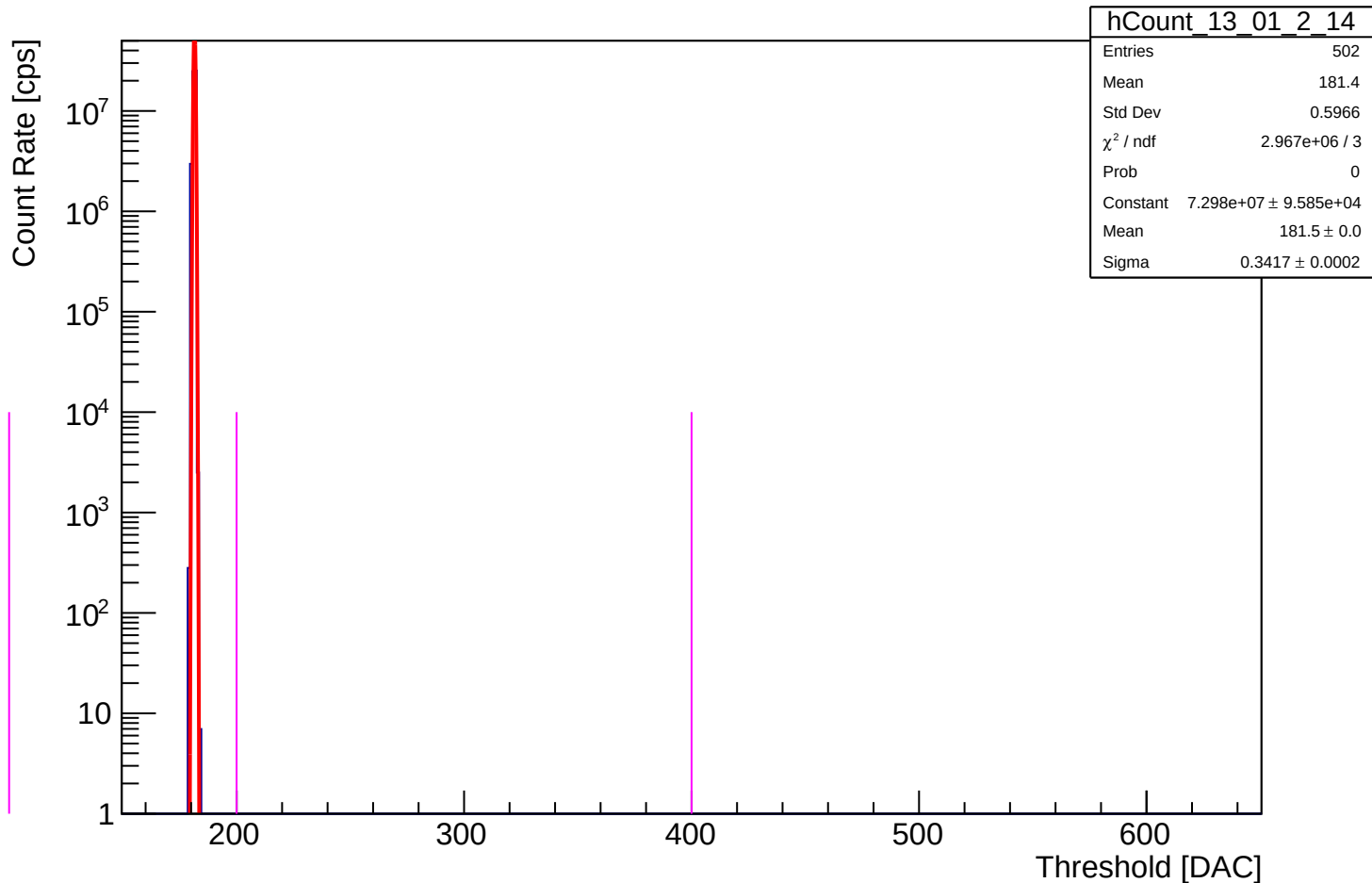
Row 1 Tile 1 Pmt 6 Pixel 33 Slot 13 Fiber 1 Asic 2 Channel 15



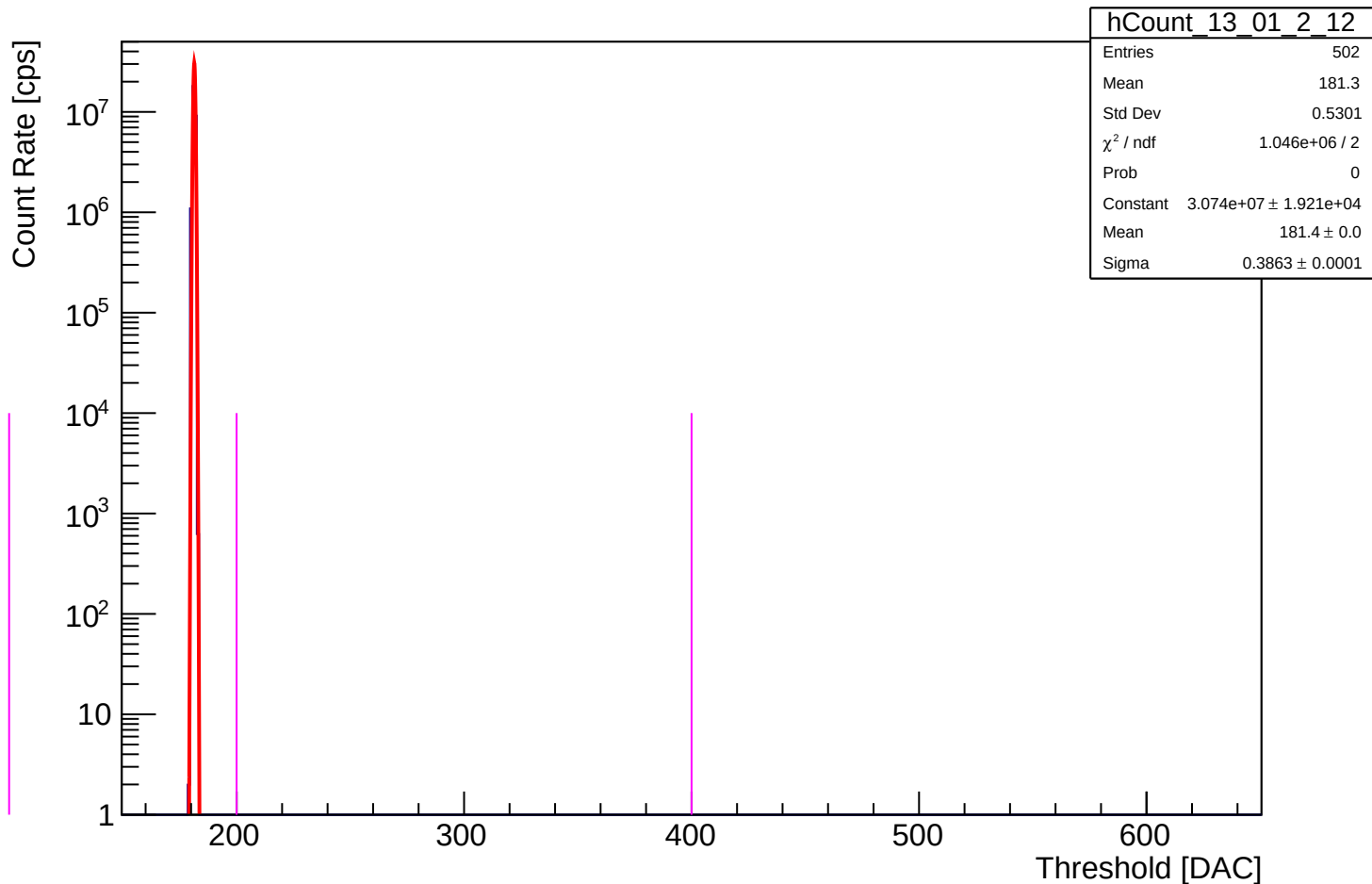
Row 1 Tile 1 Pmt 6 Pixel 34 Slot 13 Fiber 1 Asic 2 Channel 13



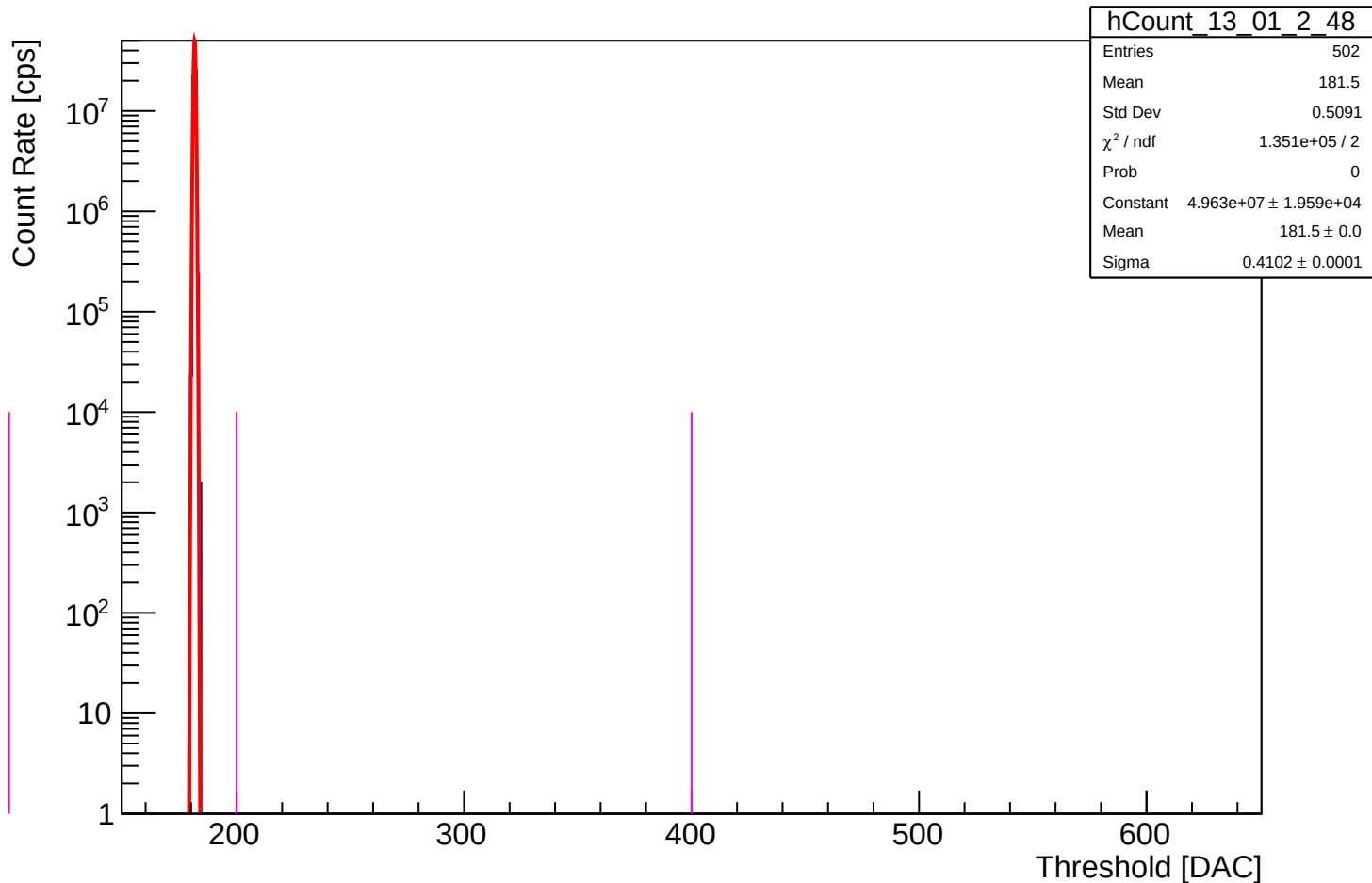
Row 1 Tile 1 Pmt 6 Pixel 35 Slot 13 Fiber 1 Asic 2 Channel 14



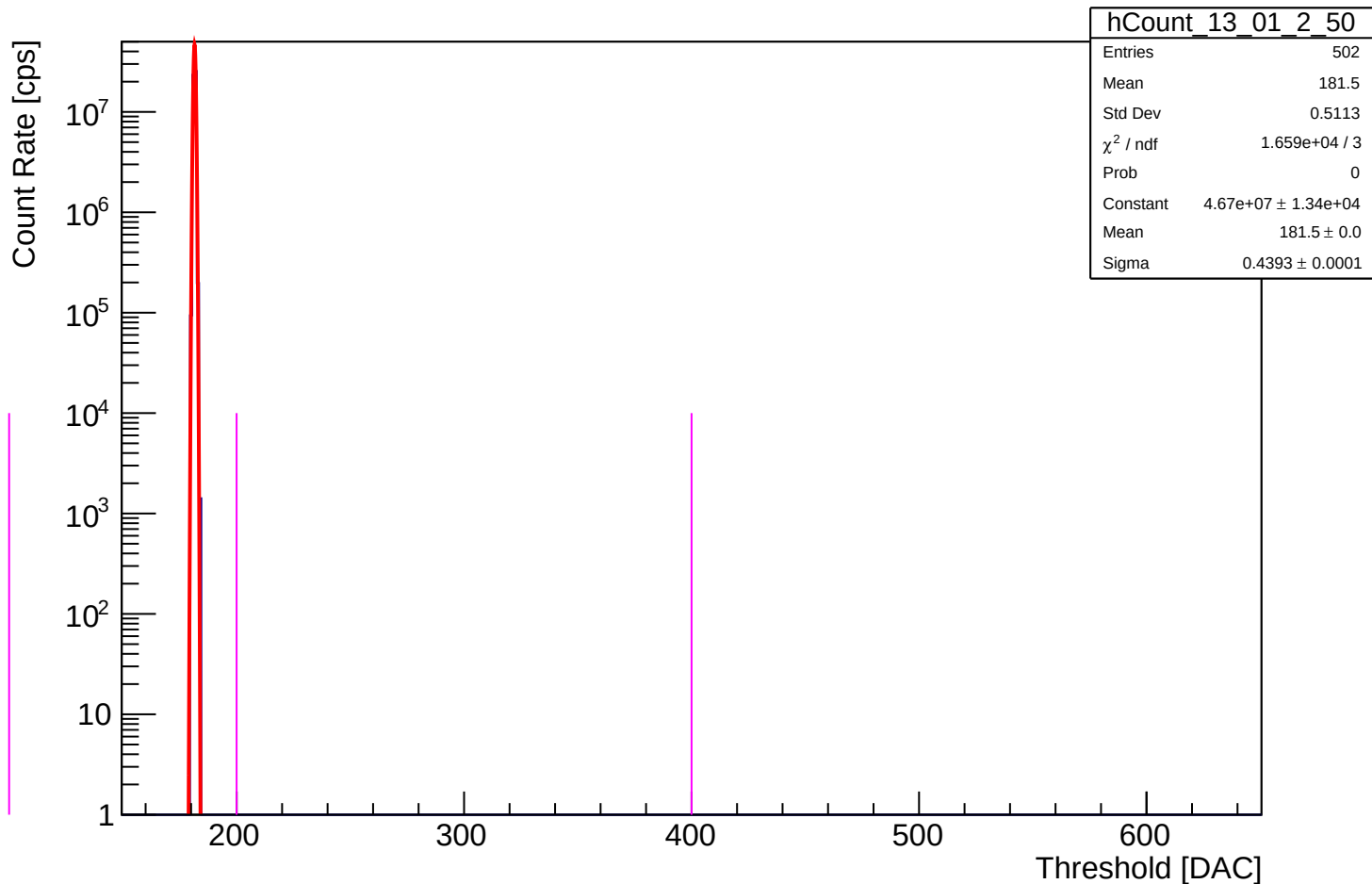
Row 1 Tile 1 Pmt 6 Pixel 36 Slot 13 Fiber 1 Asic 2 Channel 12



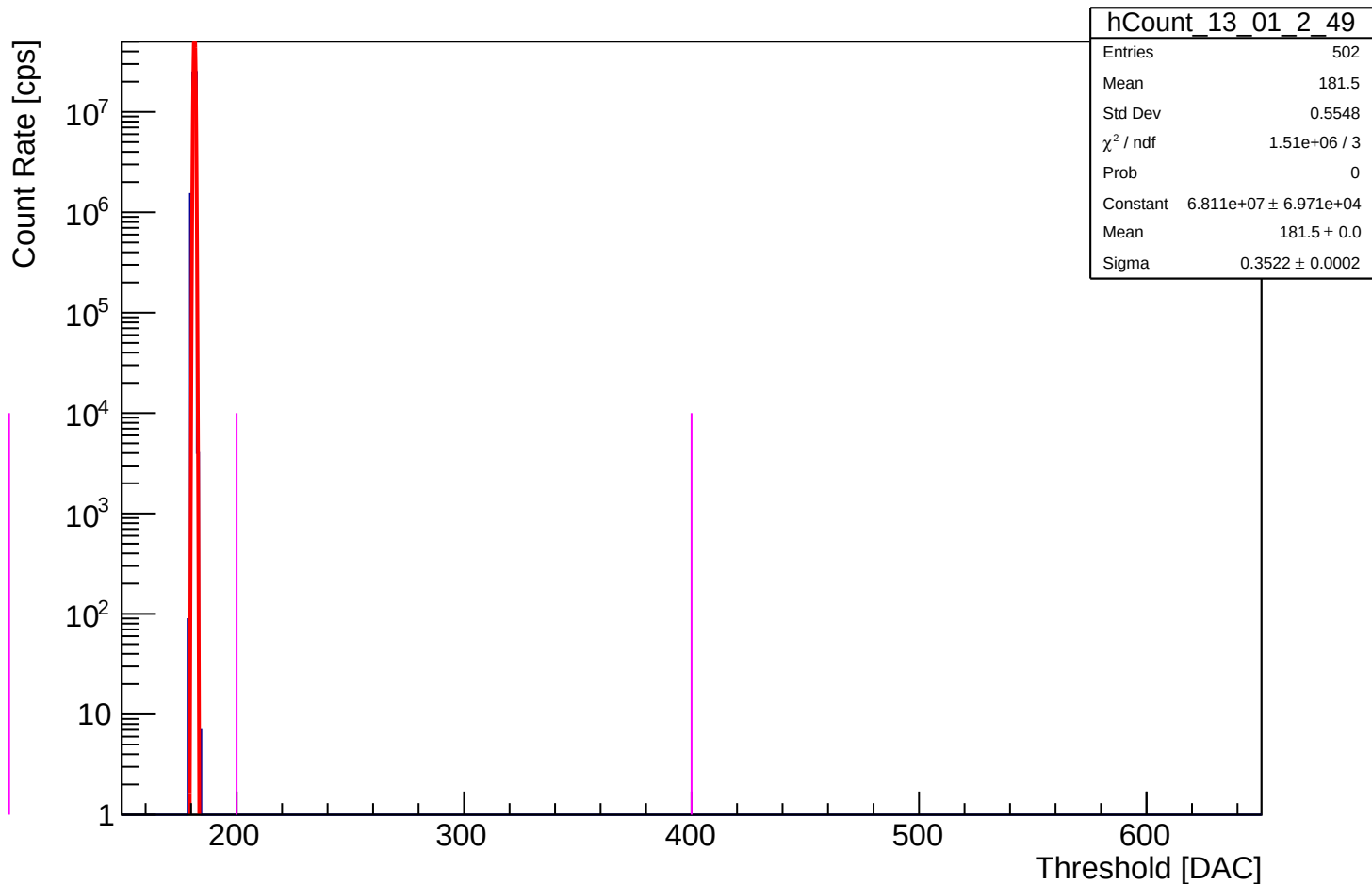
Row 1 Tile 1 Pmt 6 Pixel 37 Slot 13 Fiber 1 Asic 2 Channel 48



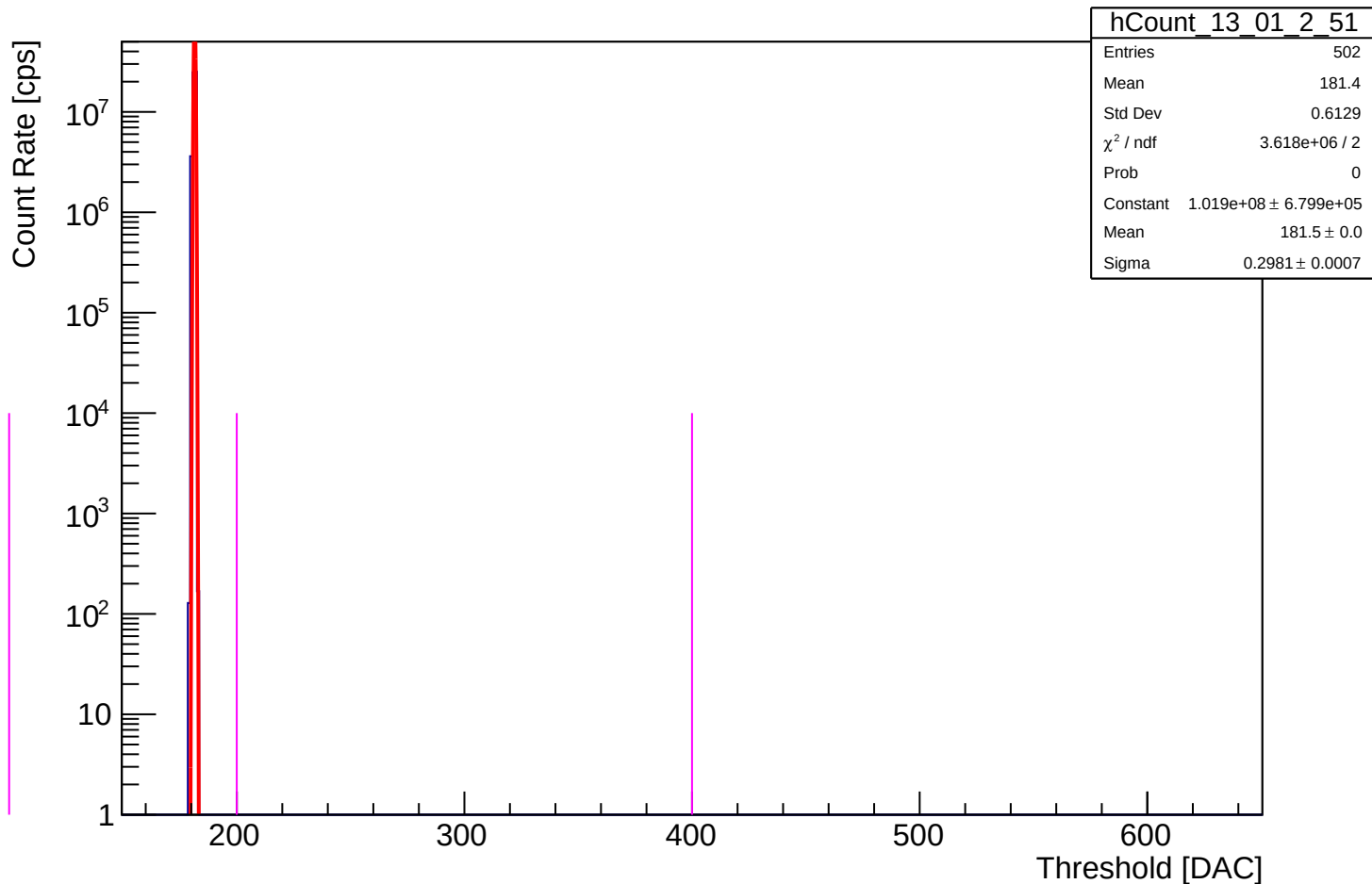
Row 1 Tile 1 Pmt 6 Pixel 38 Slot 13 Fiber 1 Asic 2 Channel 50



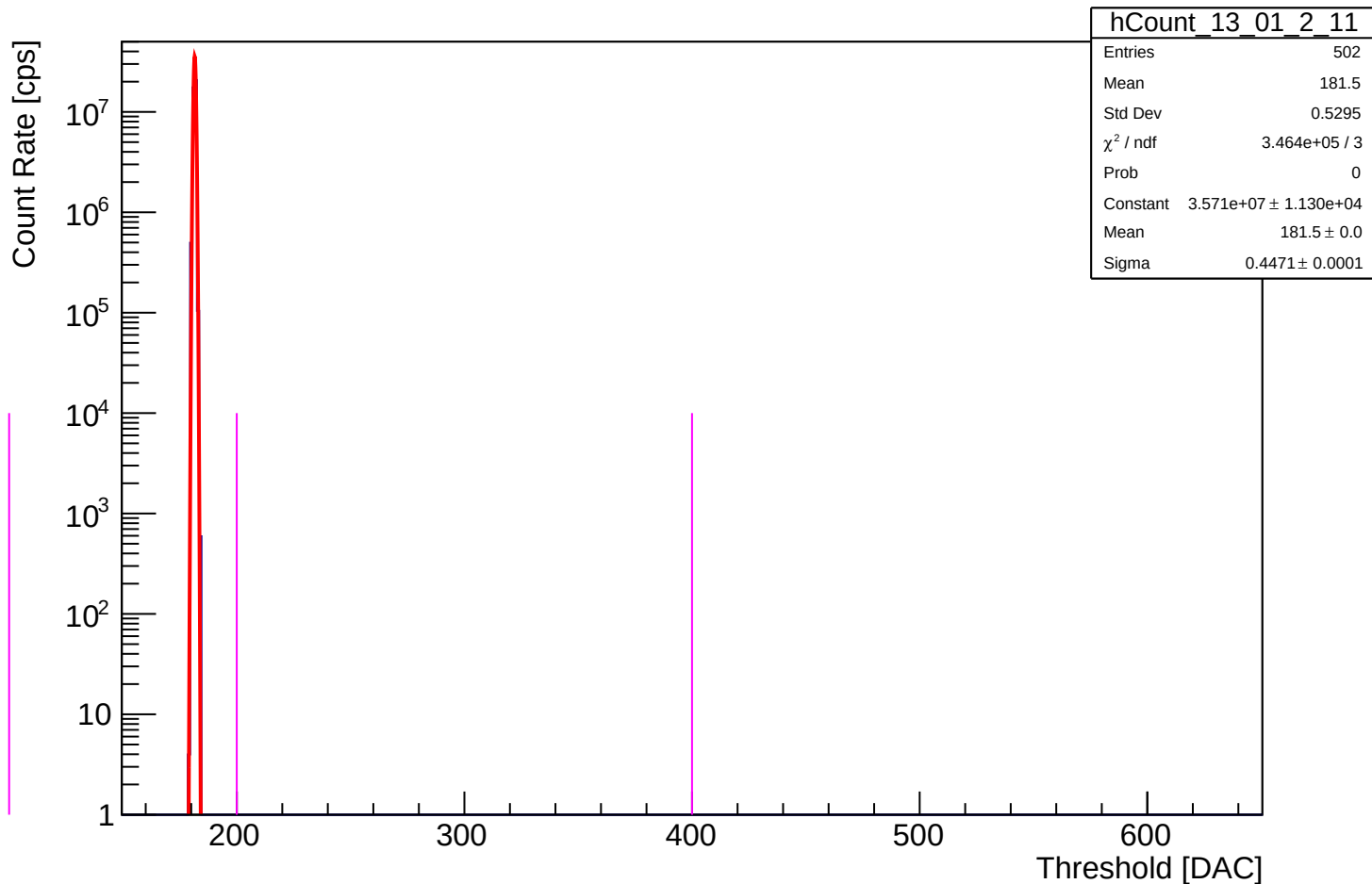
Row 1 Tile 1 Pmt 6 Pixel 39 Slot 13 Fiber 1 Asic 2 Channel 49

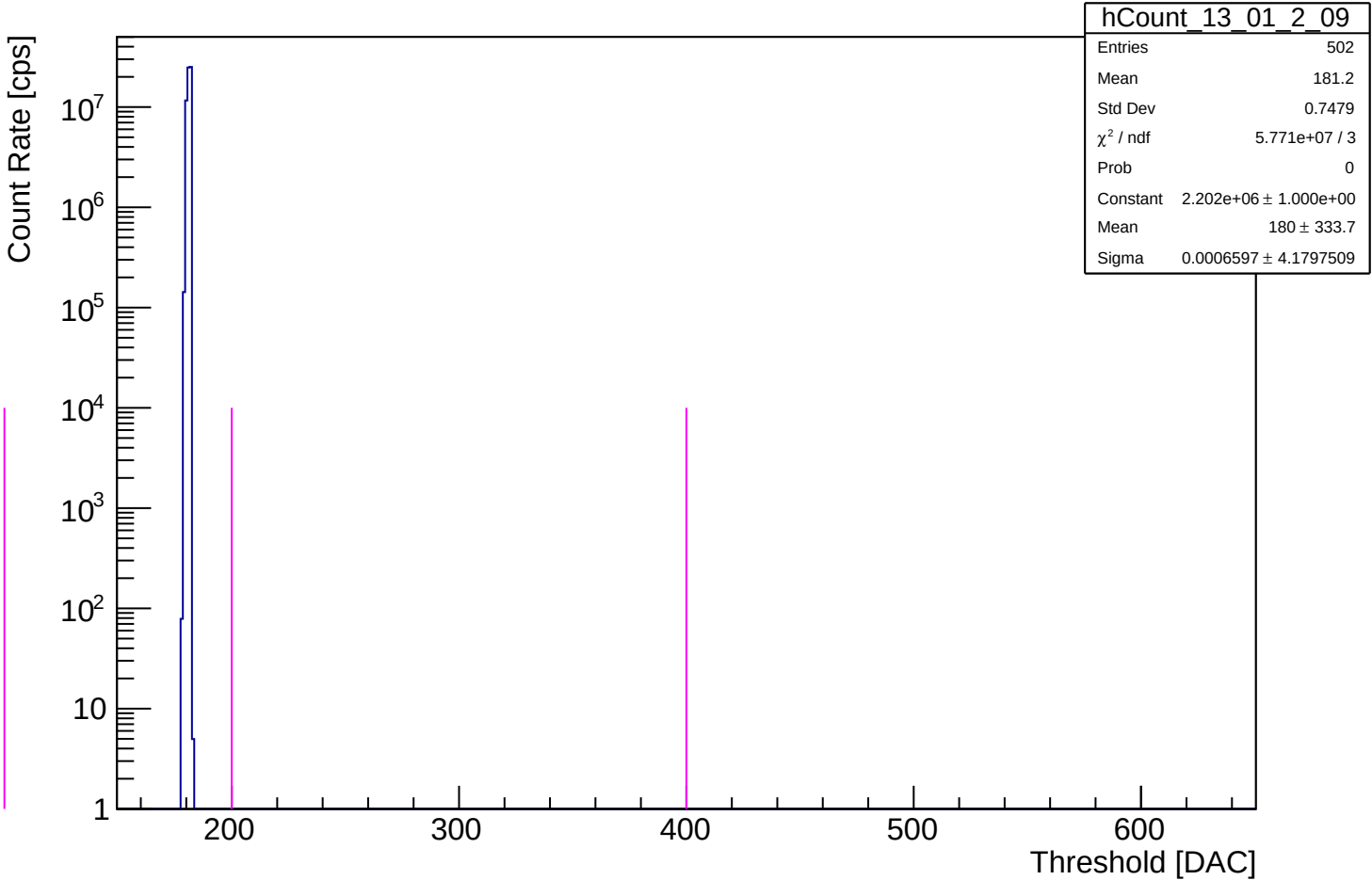


Row 1 Tile 1 Pmt 6 Pixel 40 Slot 13 Fiber 1 Asic 2 Channel 51

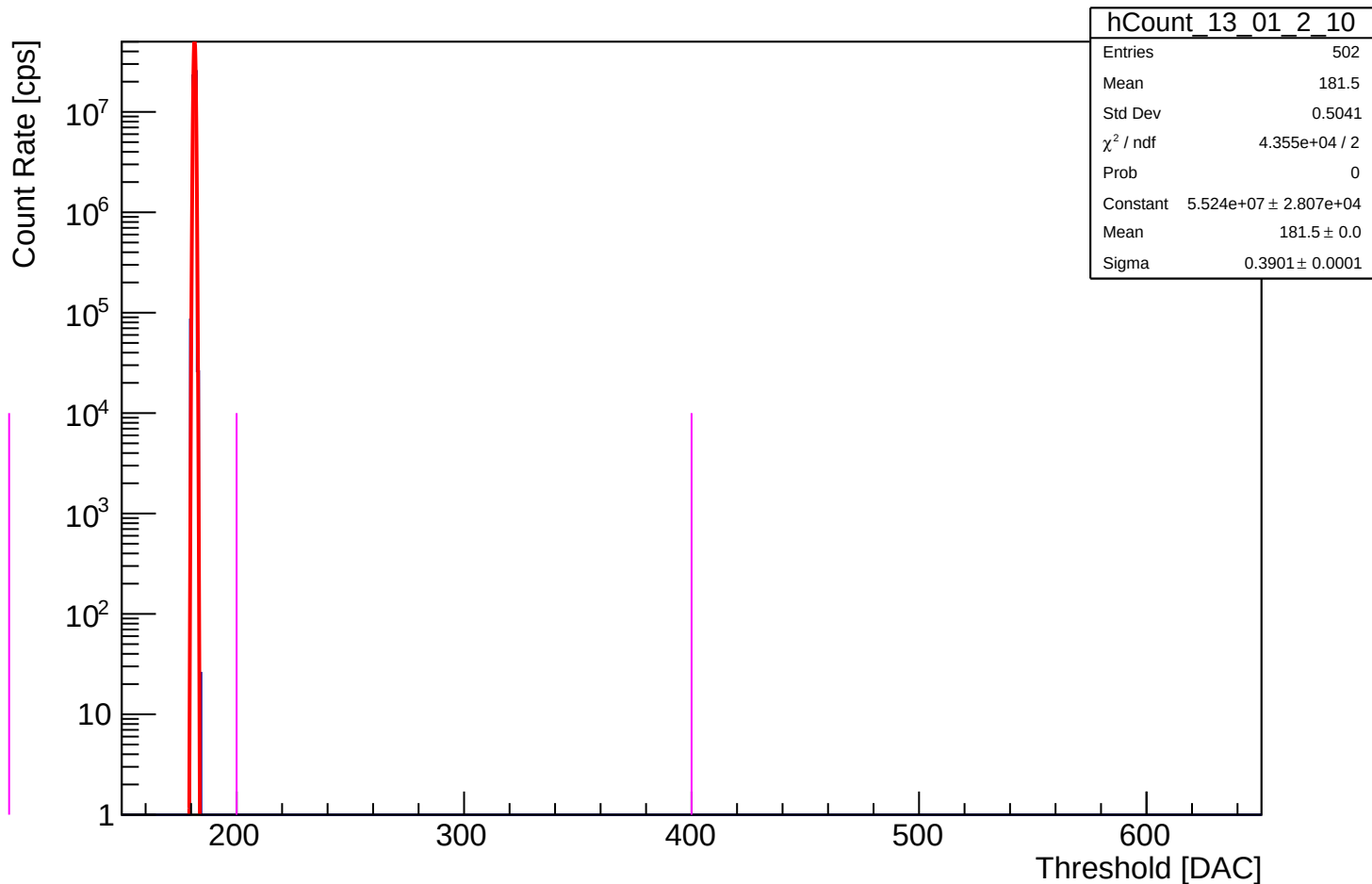


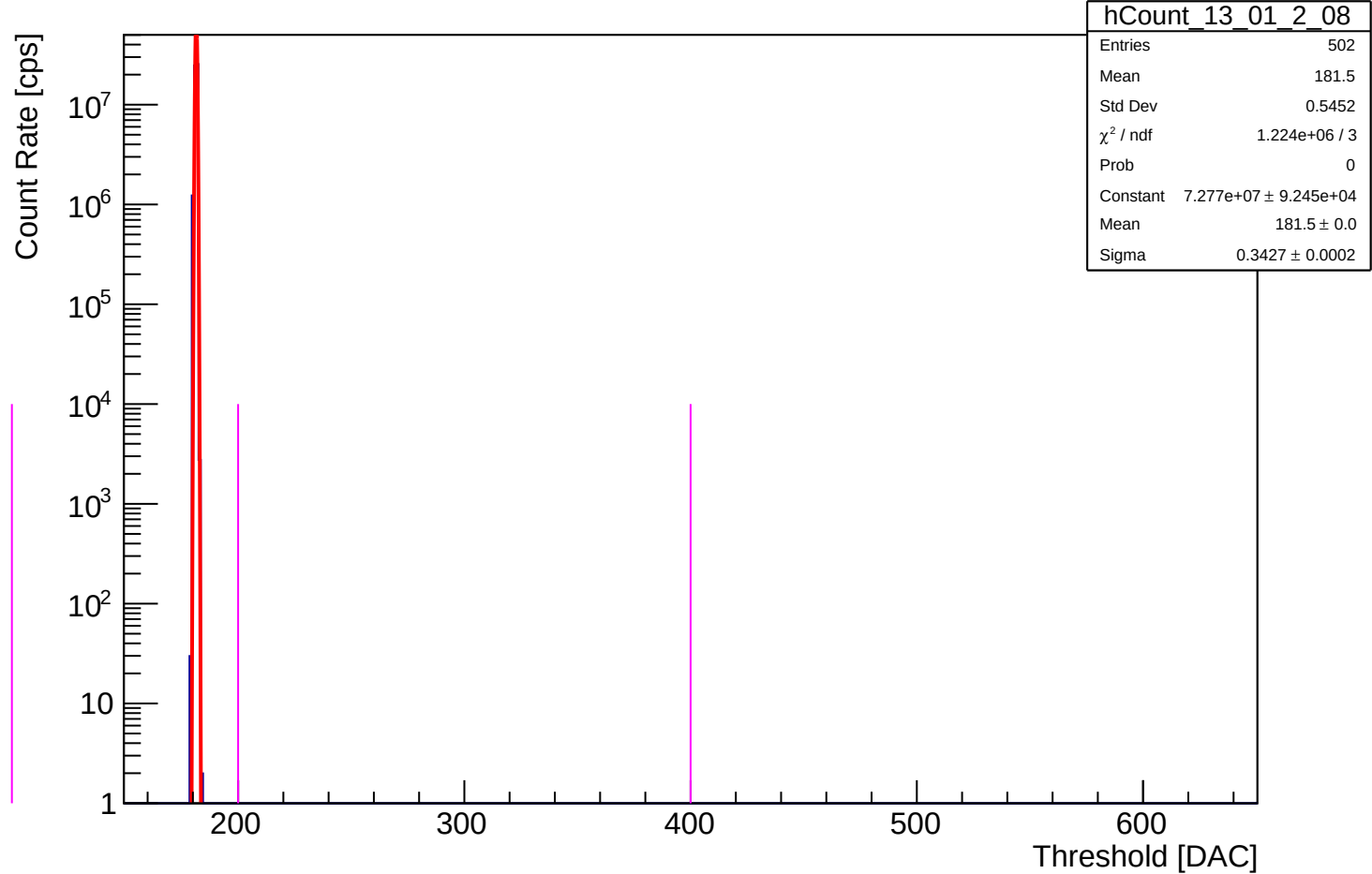
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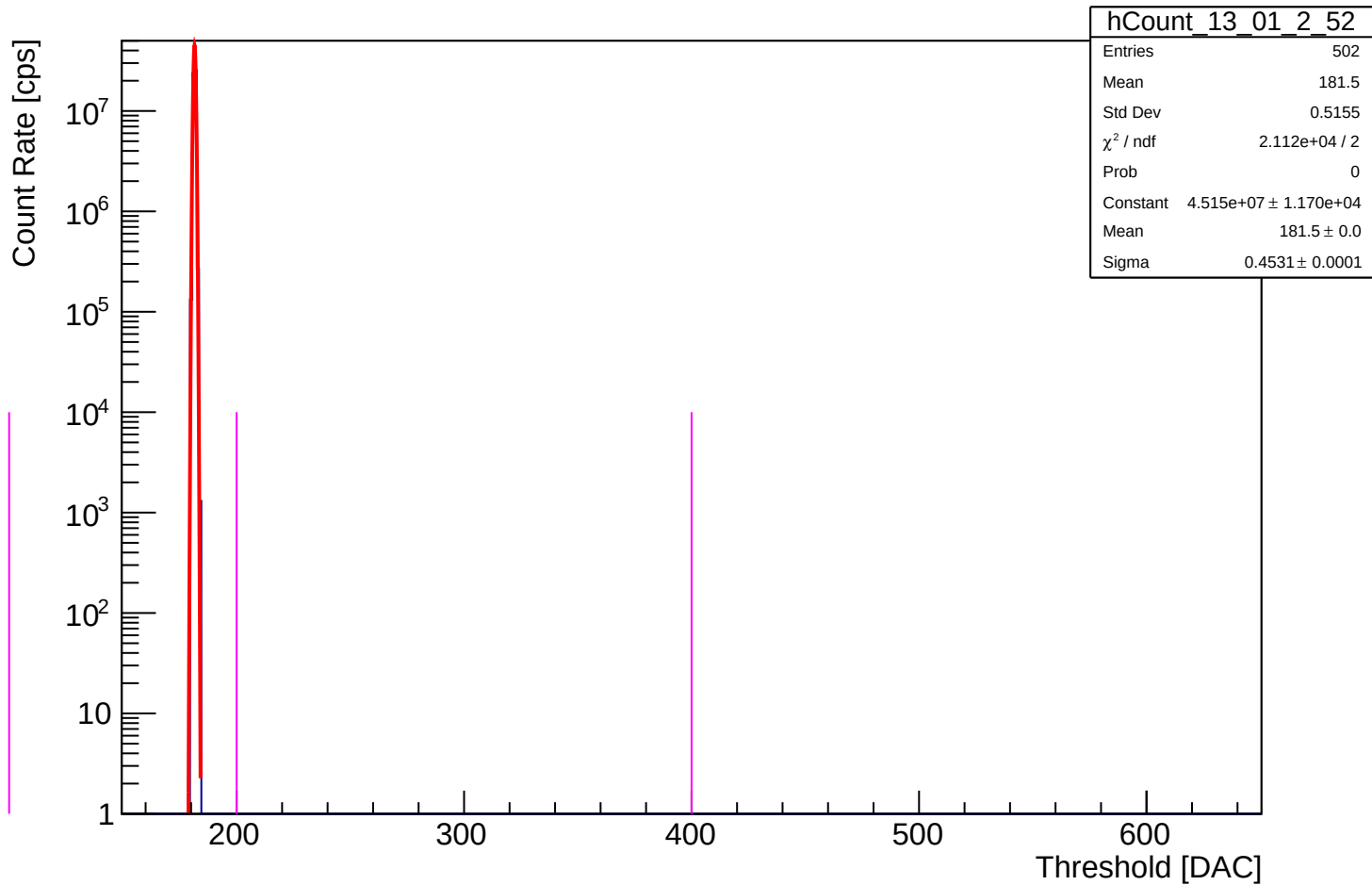


Row 1 Tile 1 Pmt 6 Pixel 43 Slot 13 Fiber 1 Asic 2 Channel 10

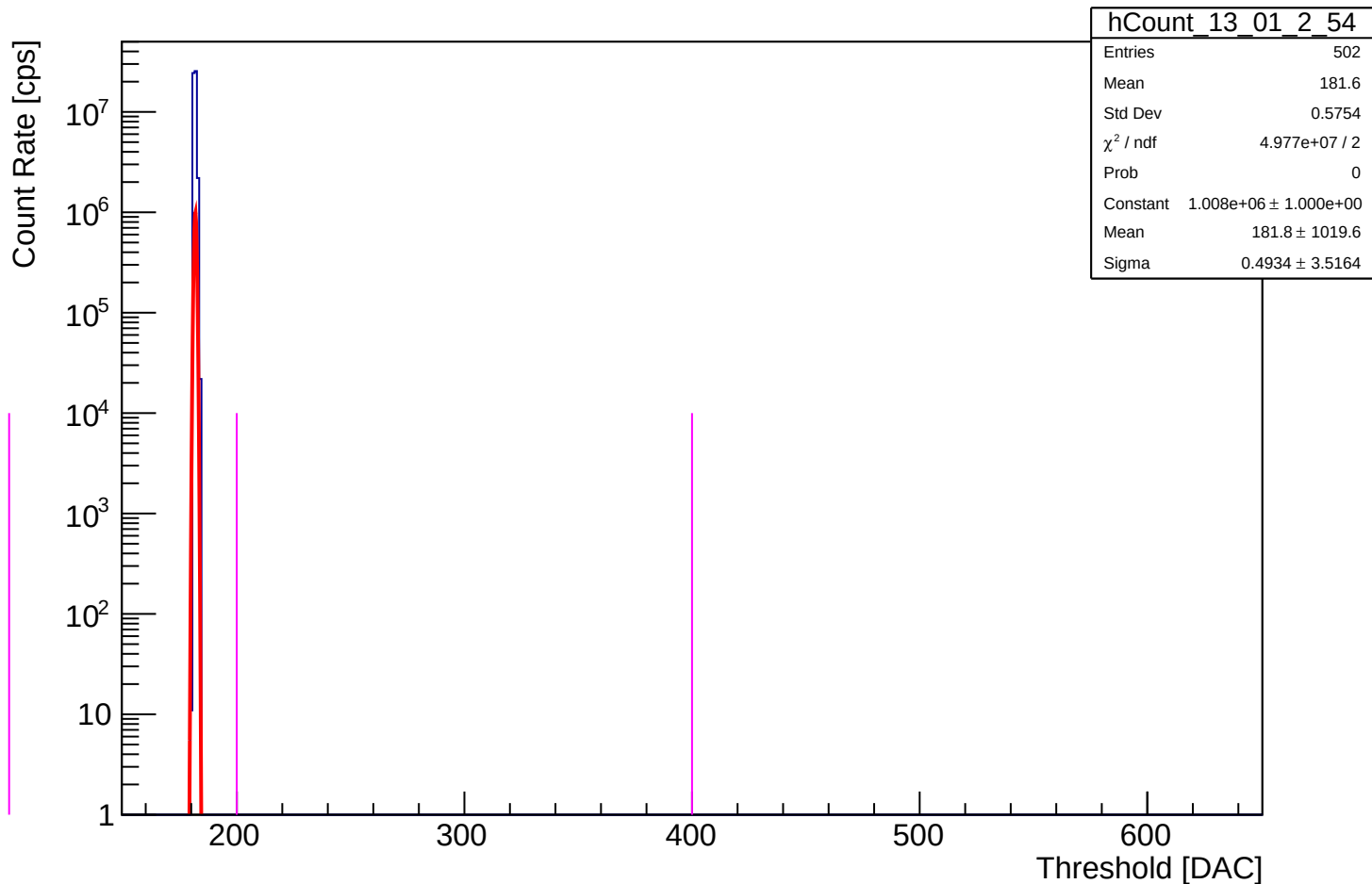




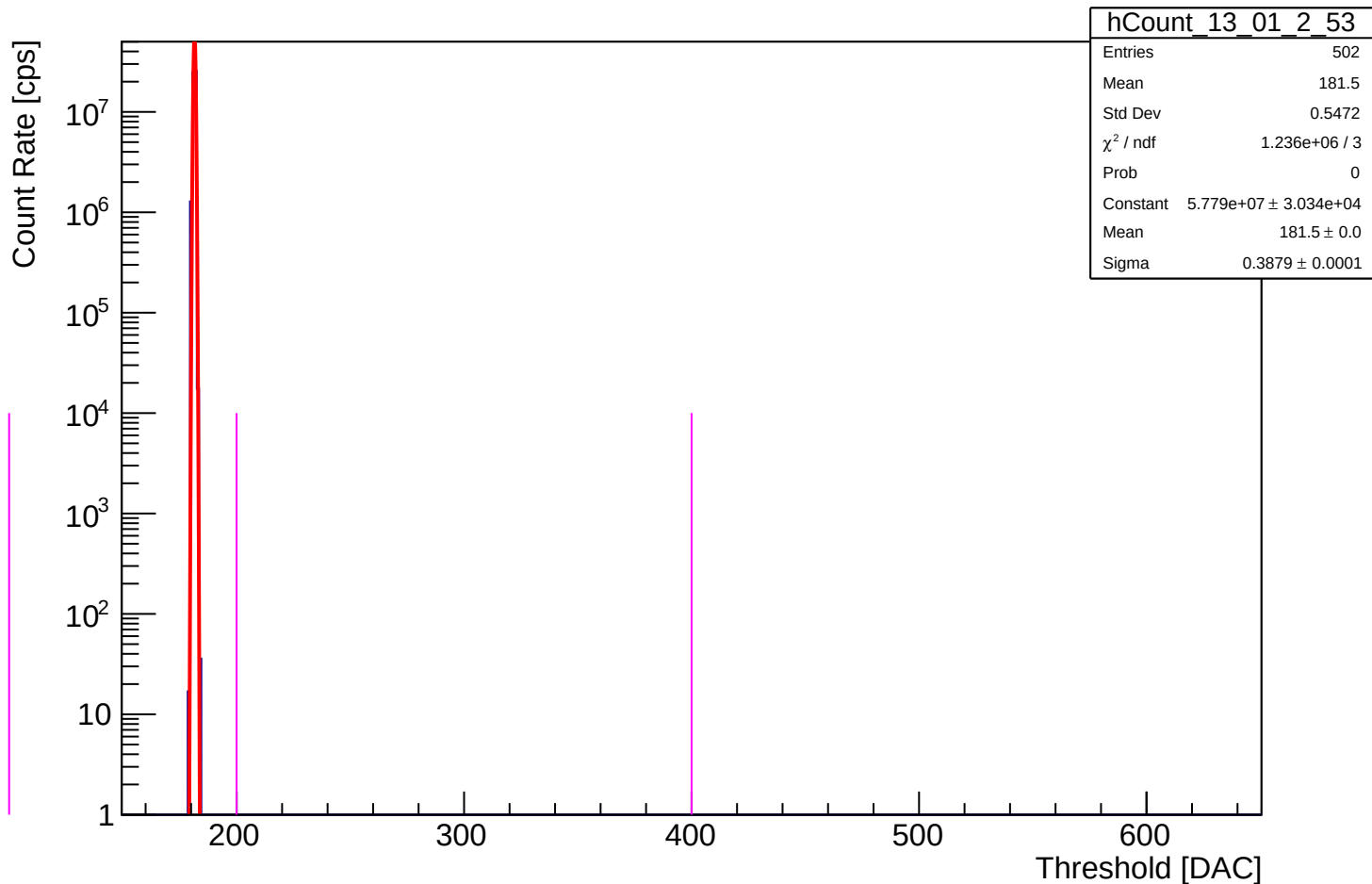
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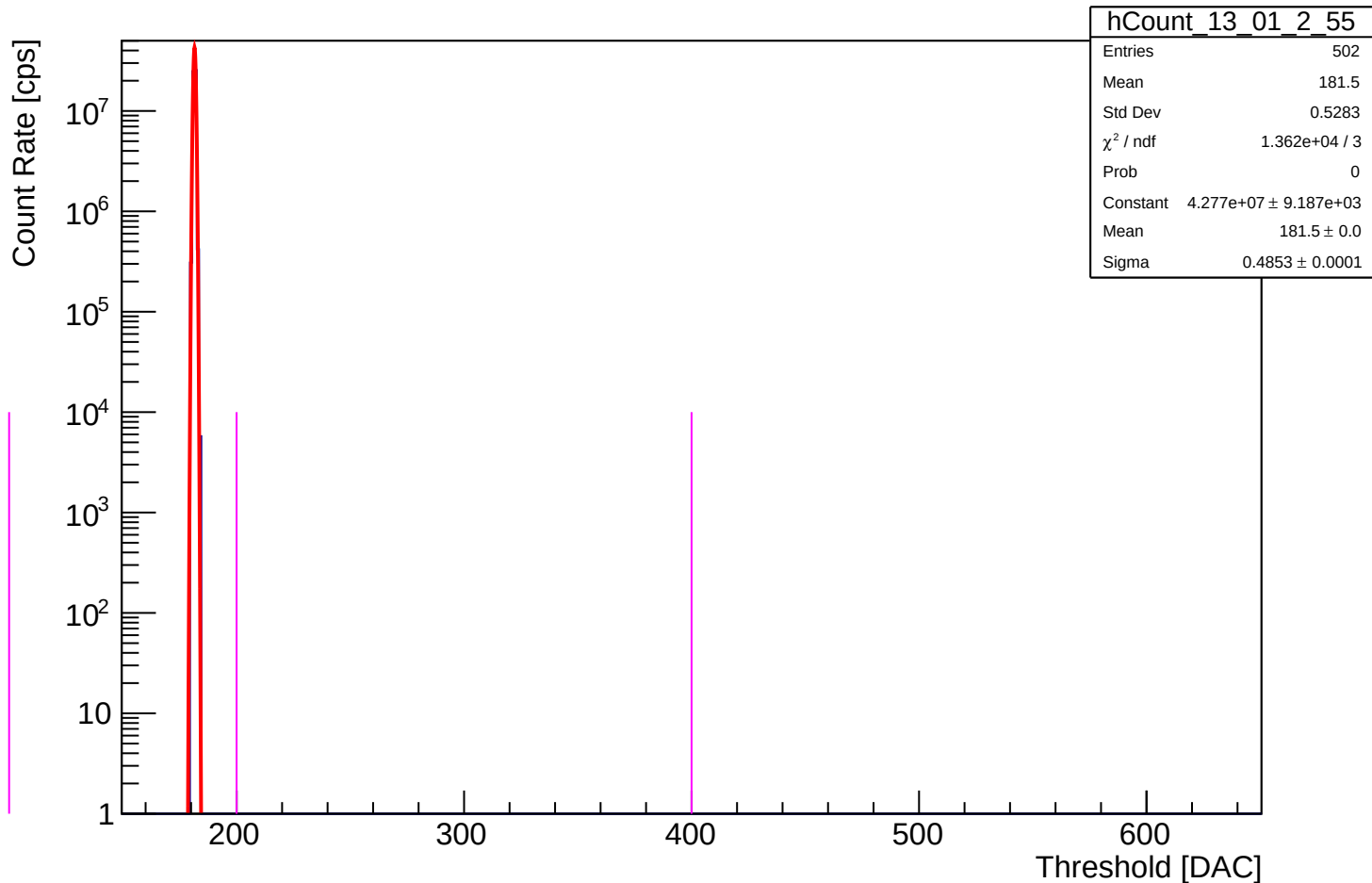
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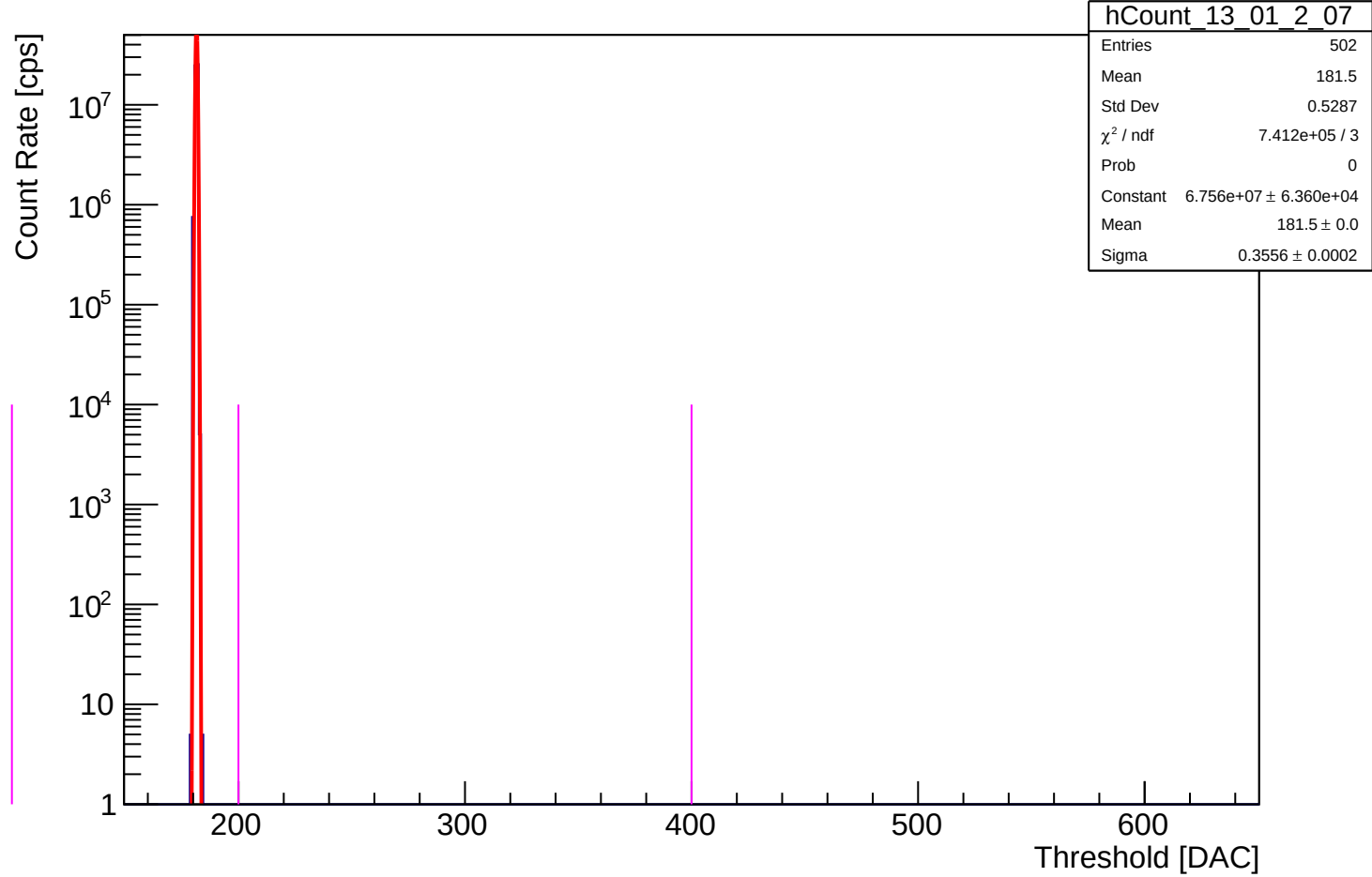


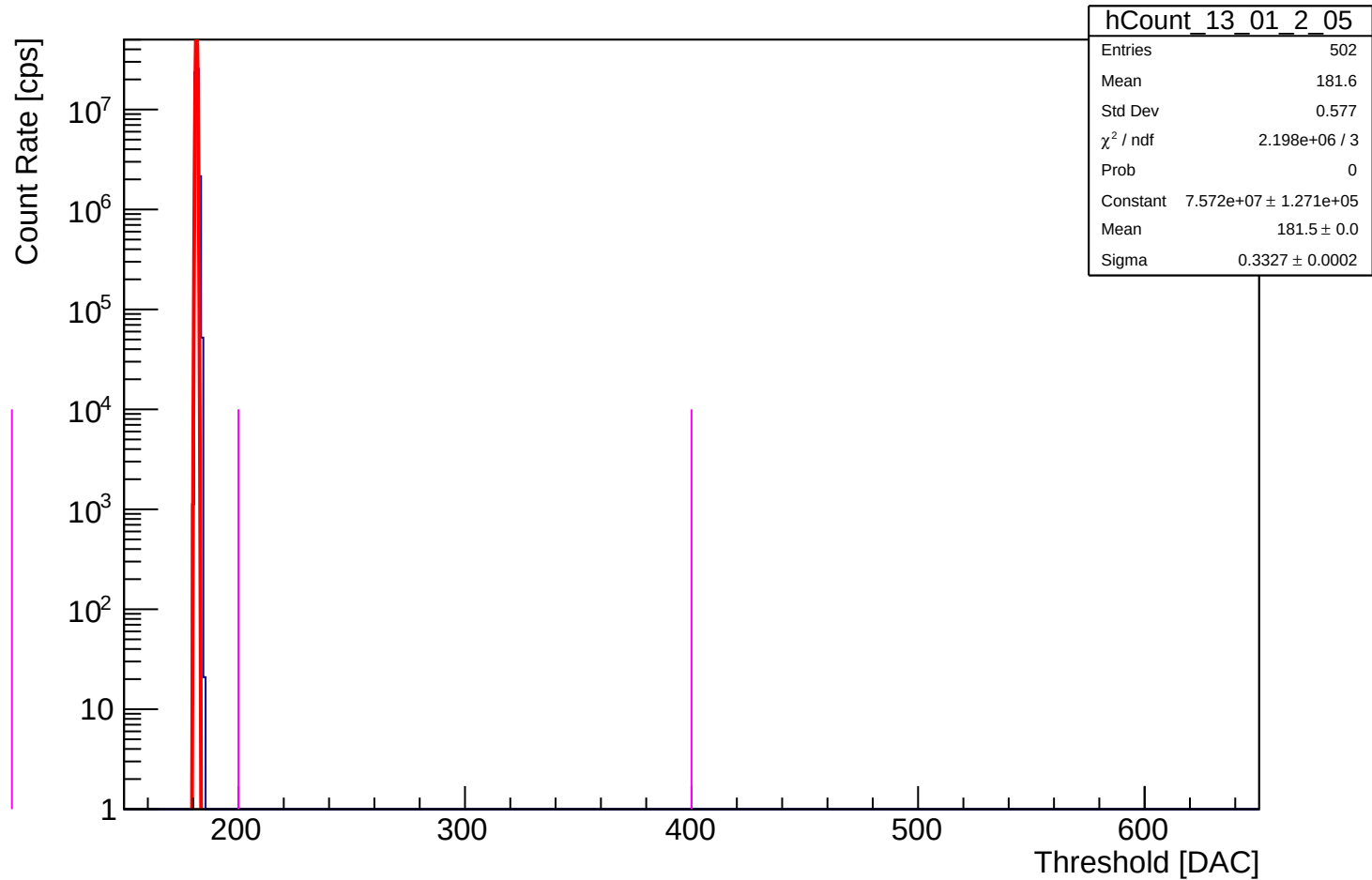
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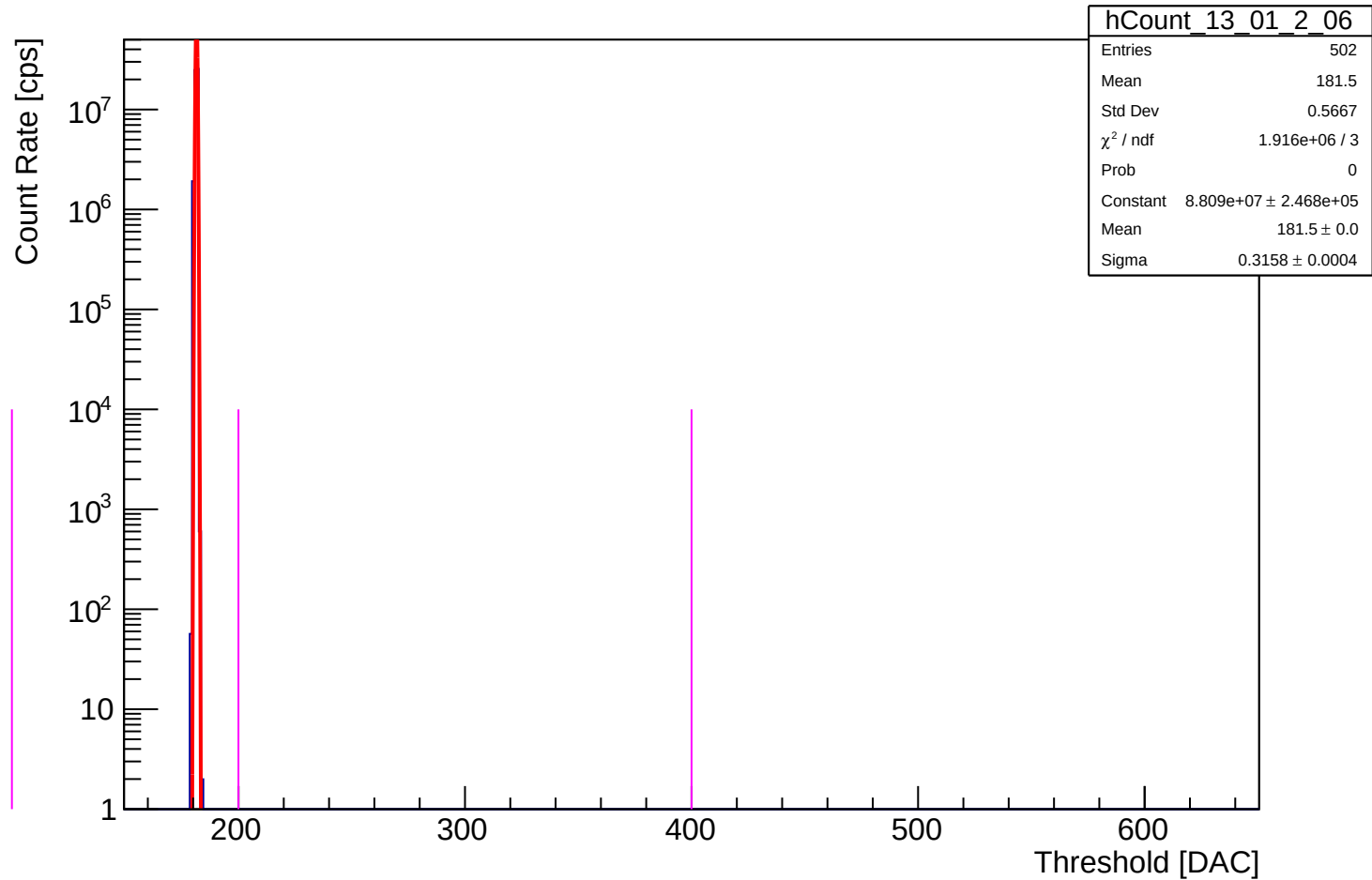


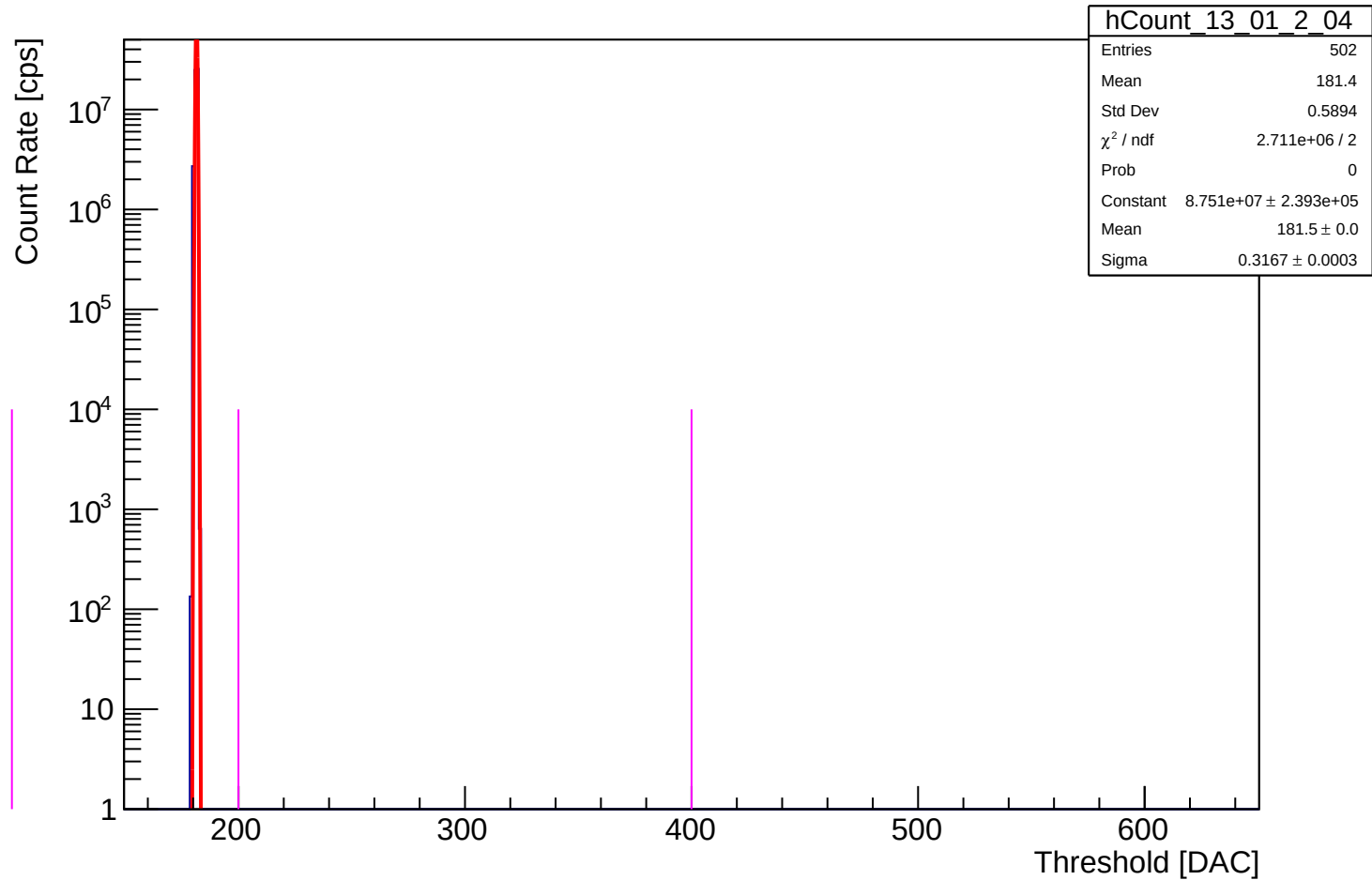
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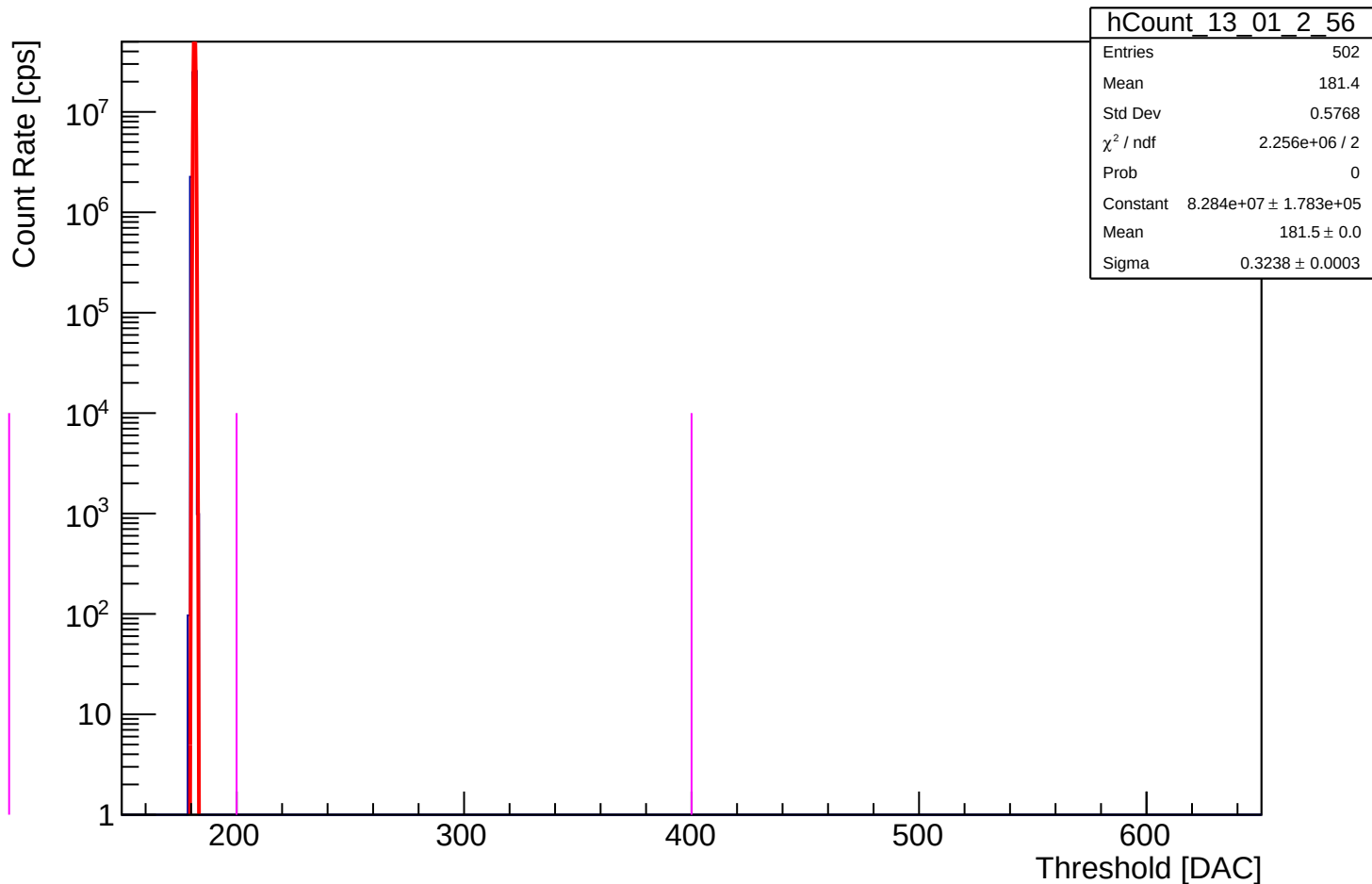




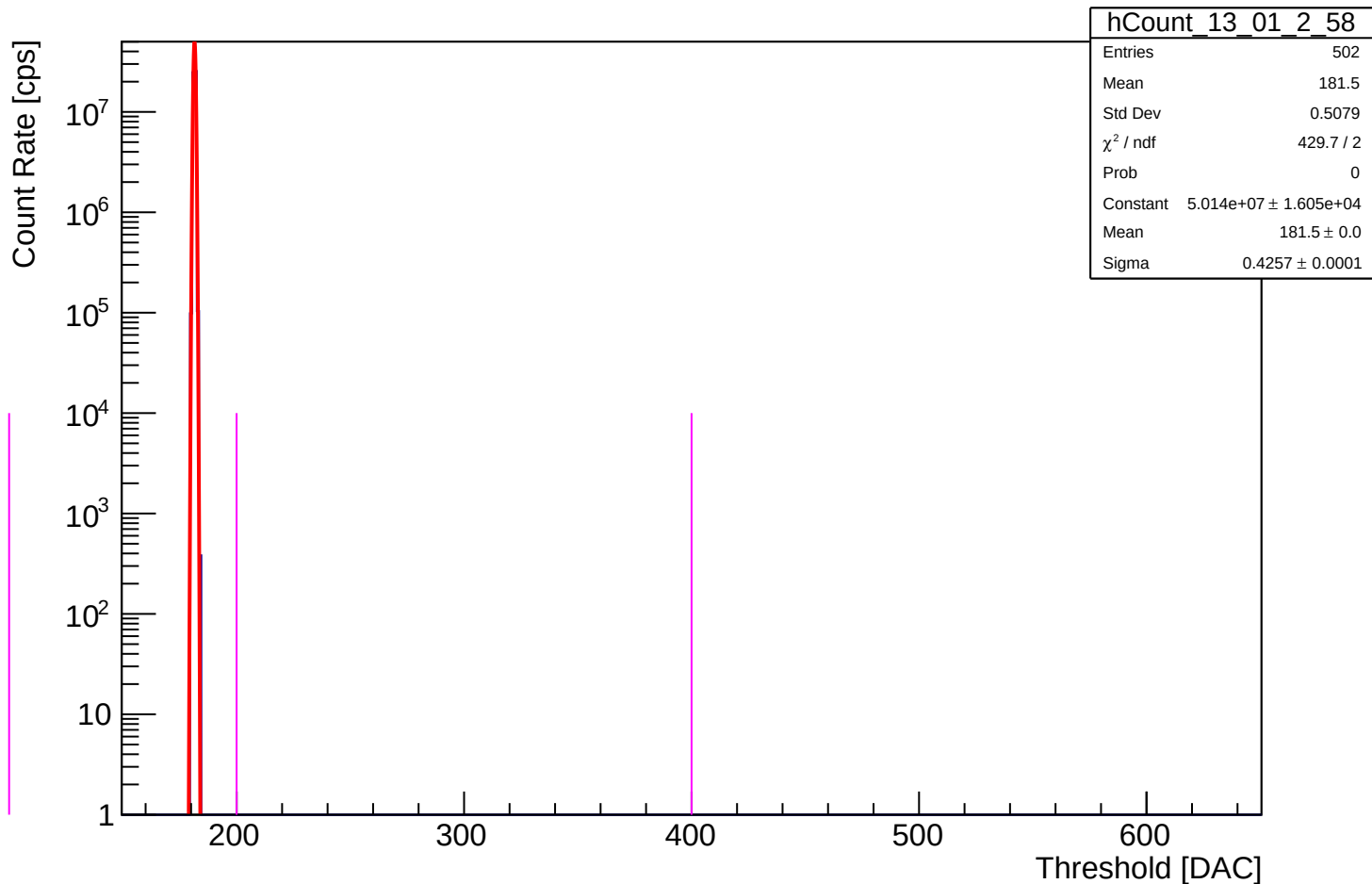




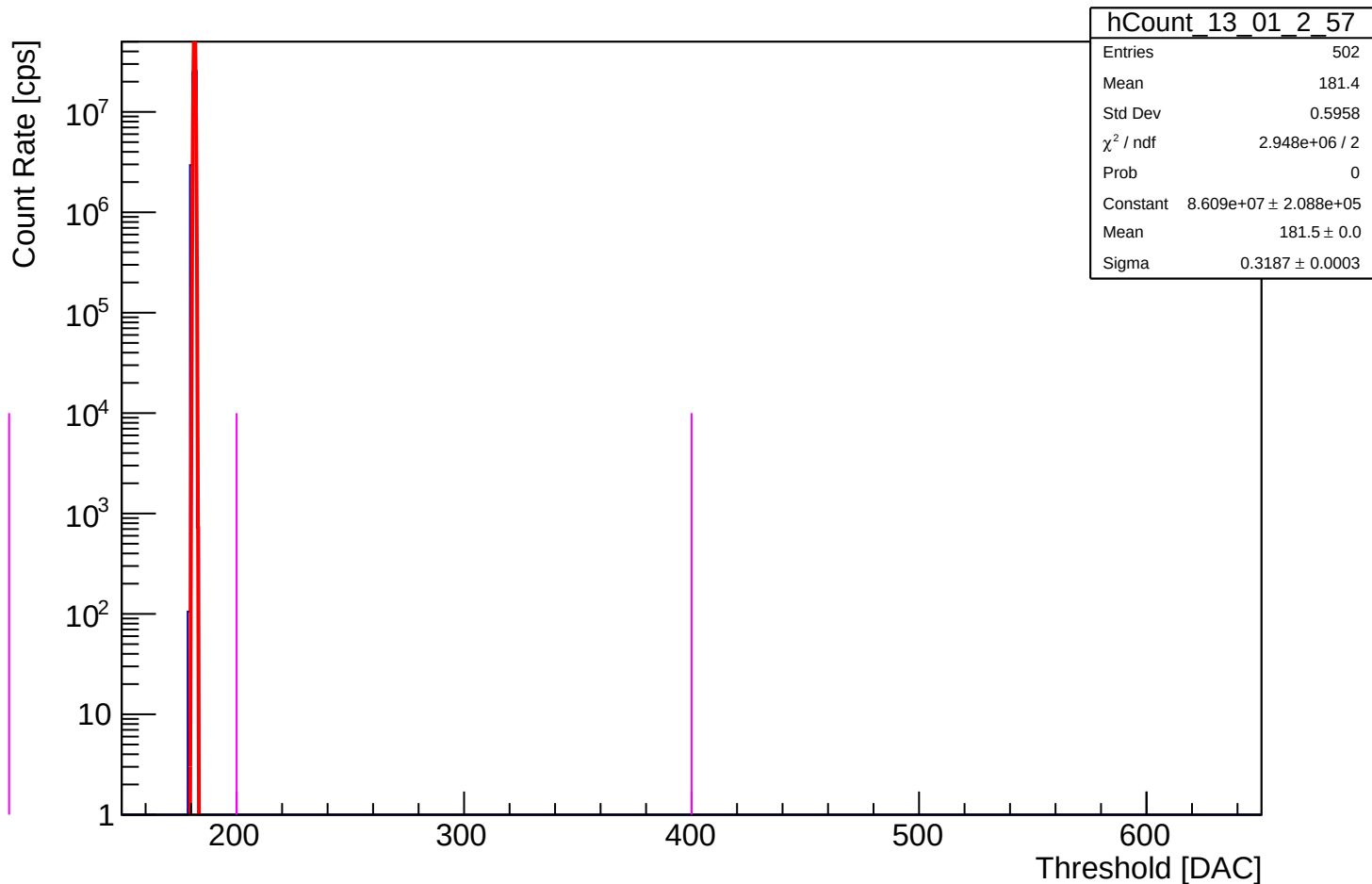
Row 1 Tile 1 Pmt 6 Pixel 53 Slot 13 Fiber 1 Asic 2 Channel 56



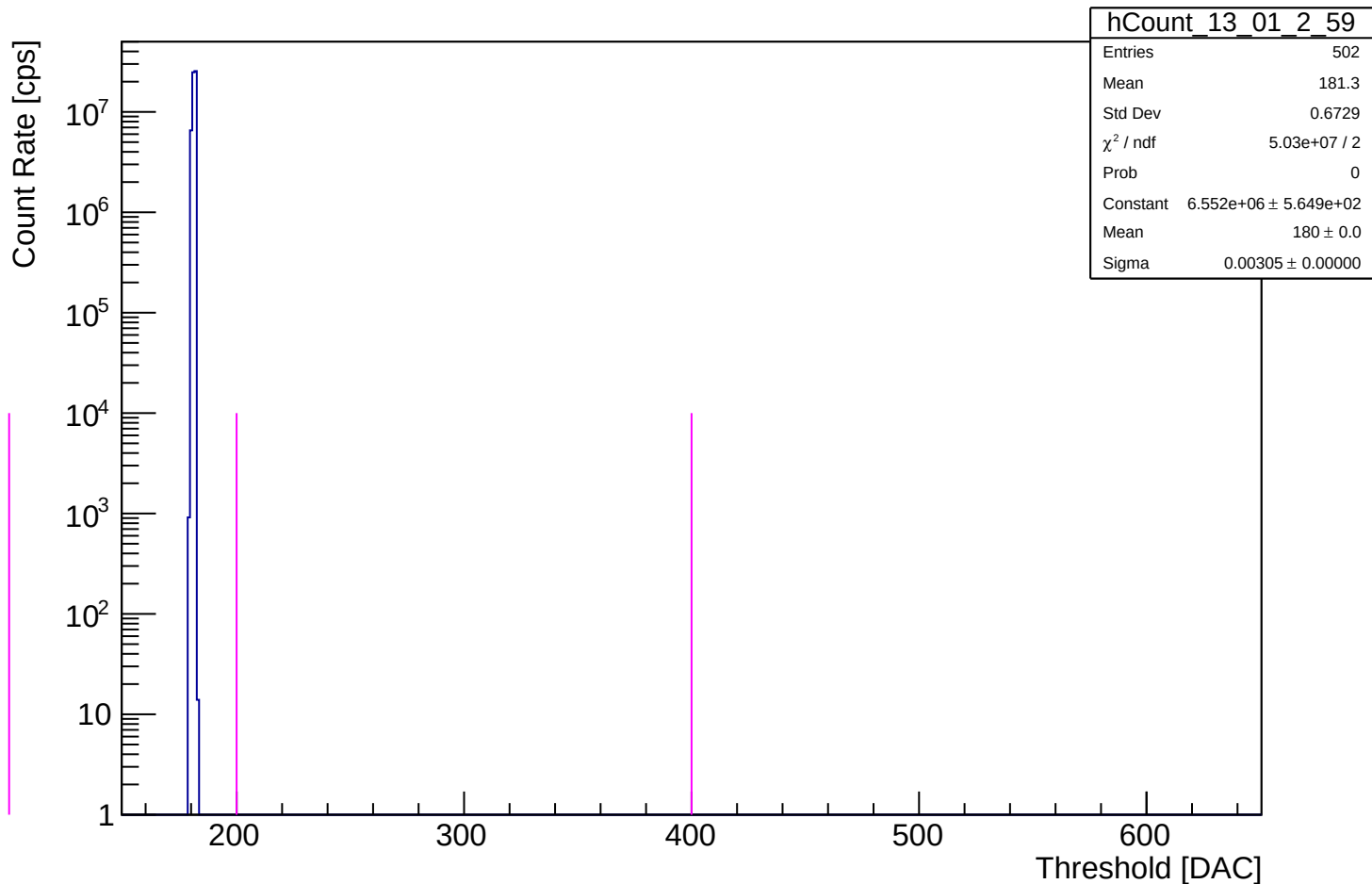
Row 1 Tile 1 Pmt 6 Pixel 54 Slot 13 Fiber 1 Asic 2 Channel 58

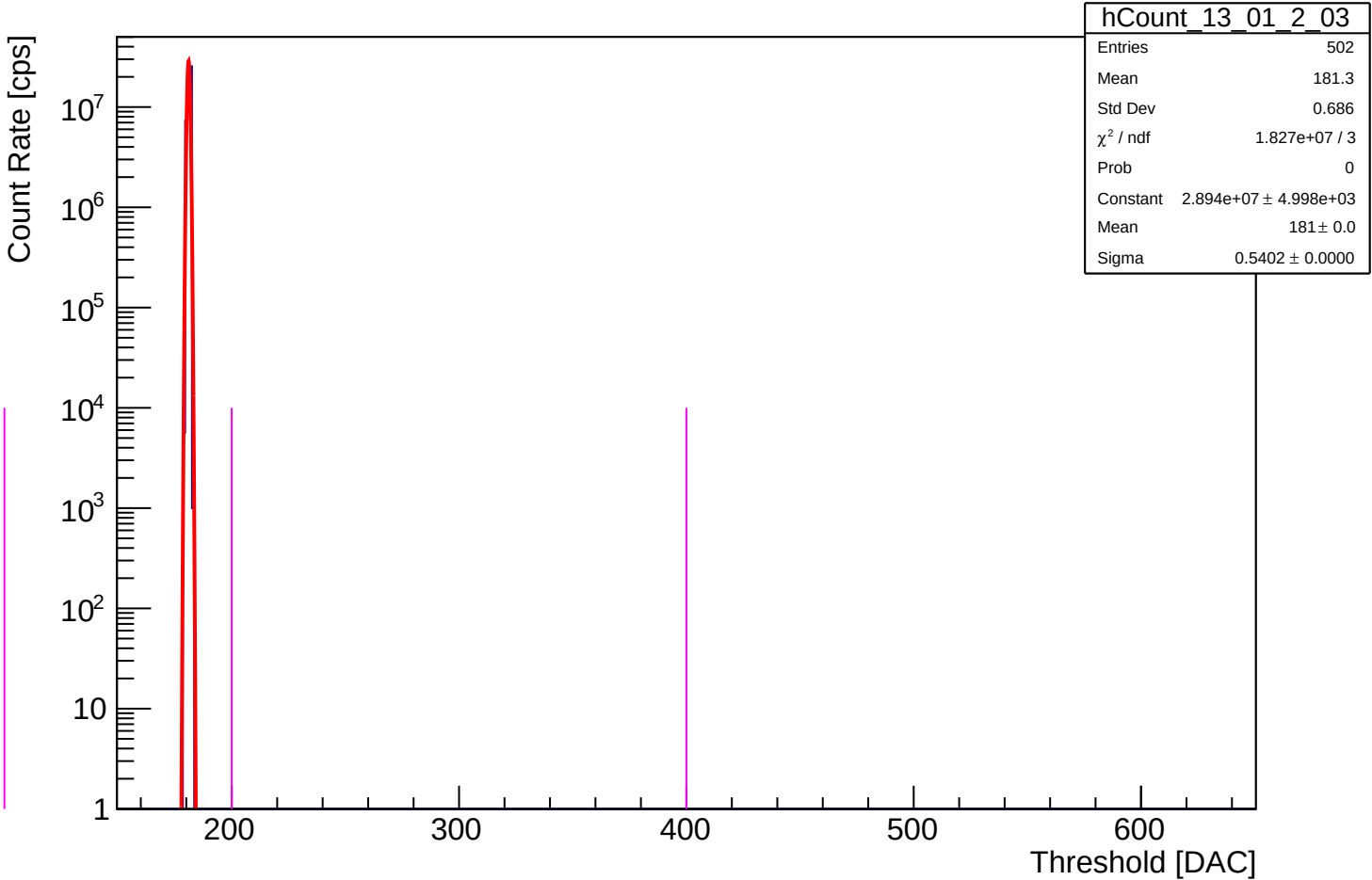


Row 1 Tile 1 Pmt 6 Pixel 55 Slot 13 Fiber 1 Asic 2 Channel 57

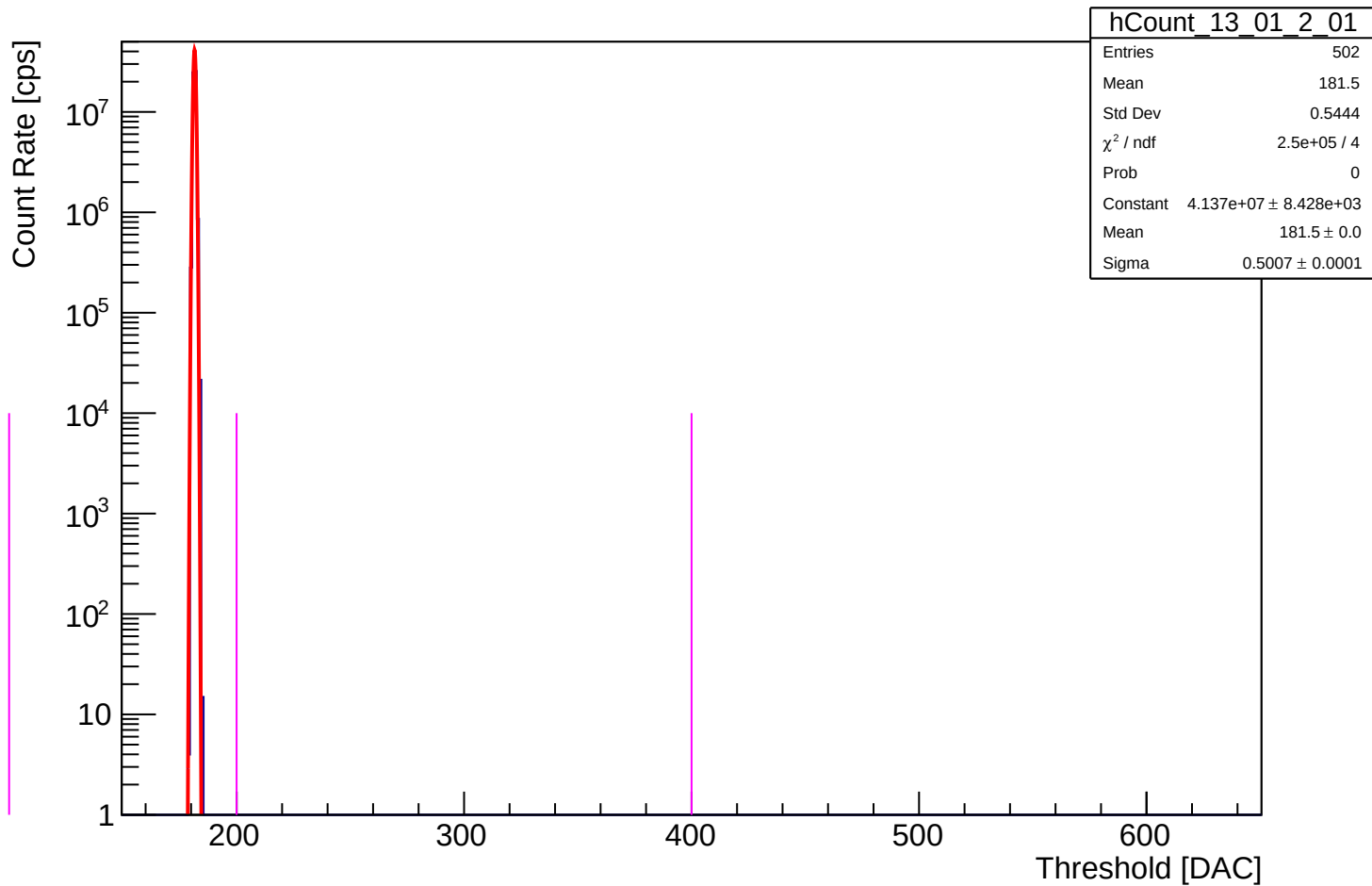


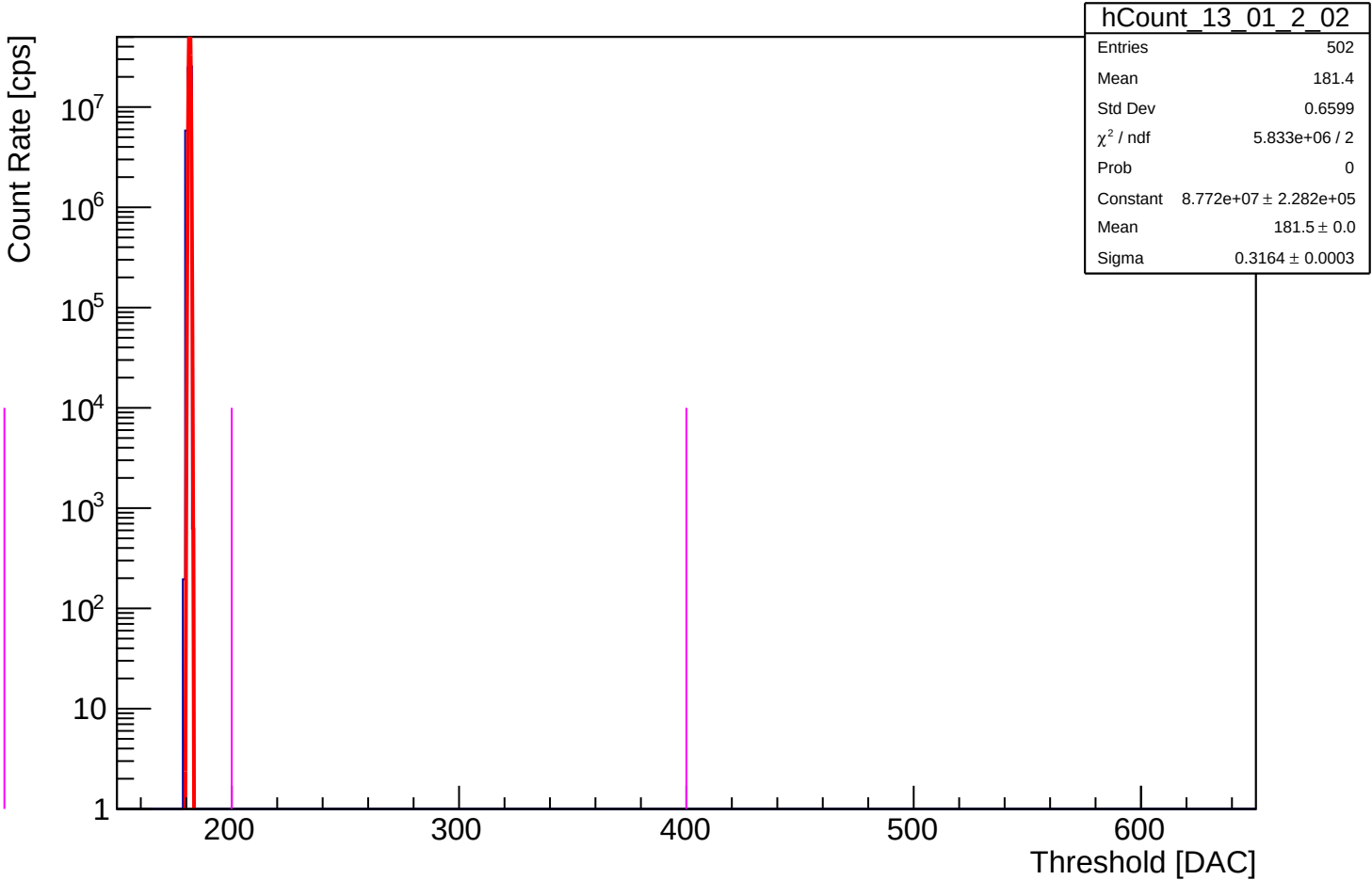
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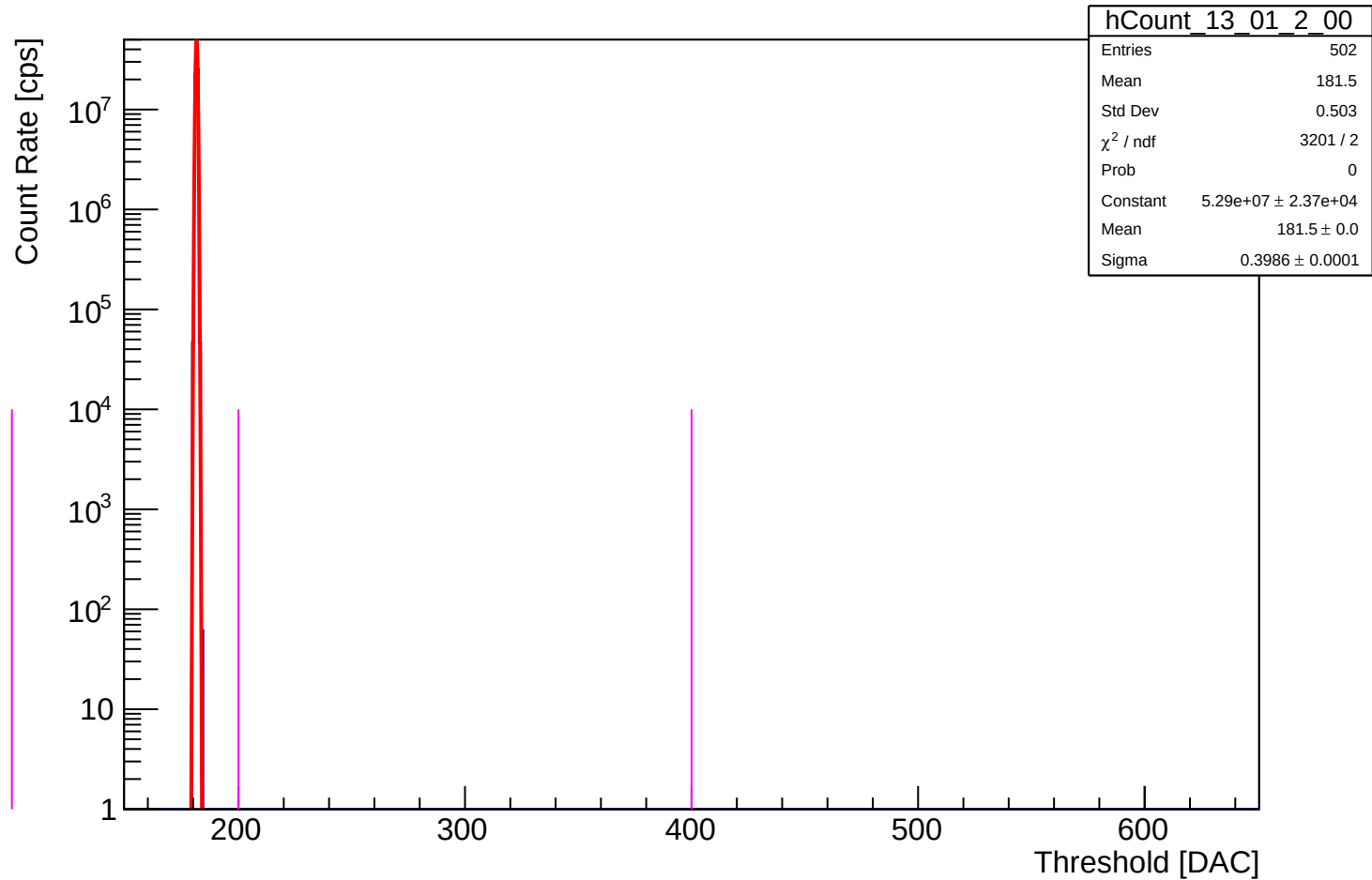




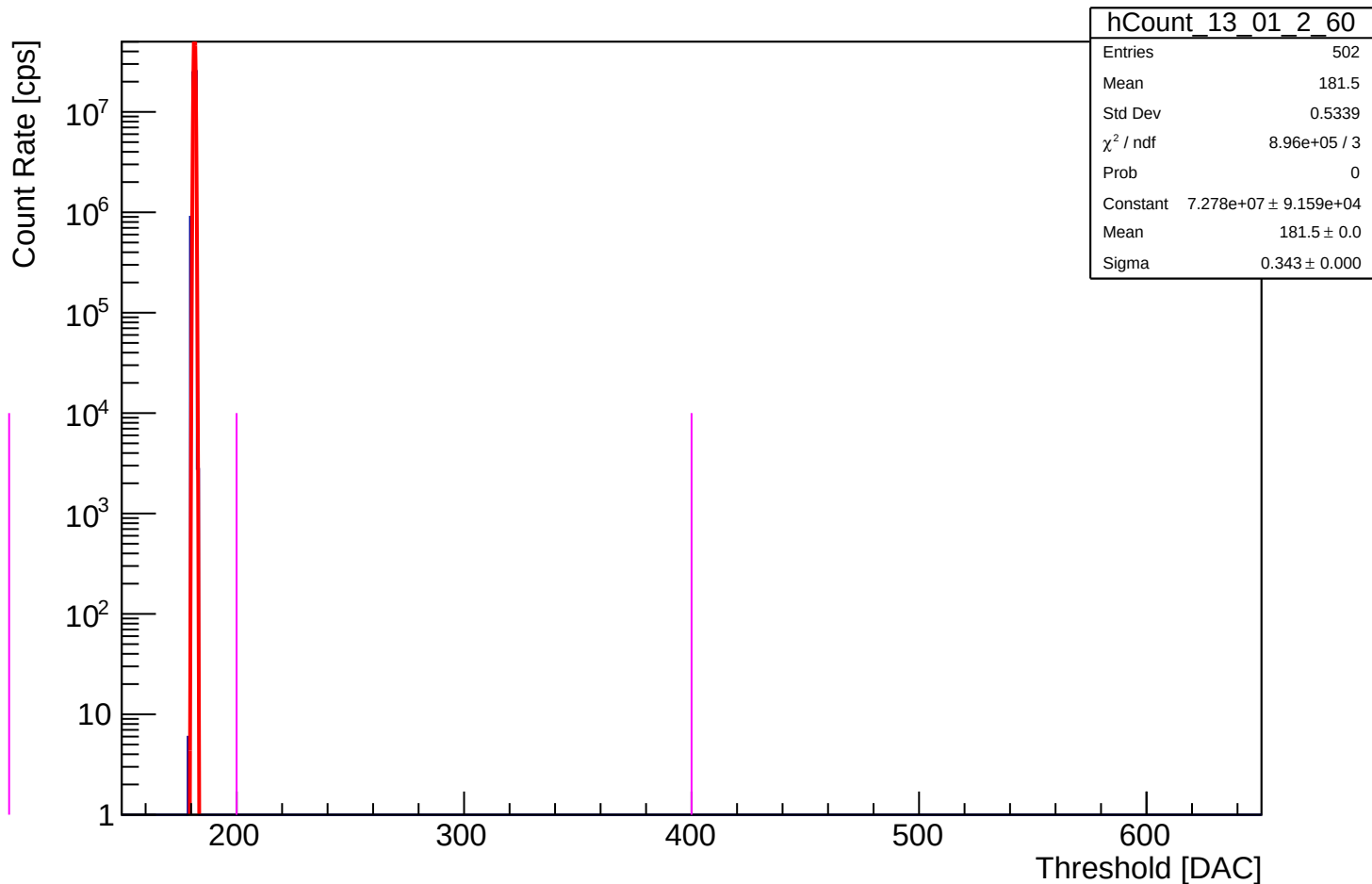
Row 1 Tile 1 Pmt 6 Pixel 58 Slot 13 Fiber 1 Asic 2 Channel 1



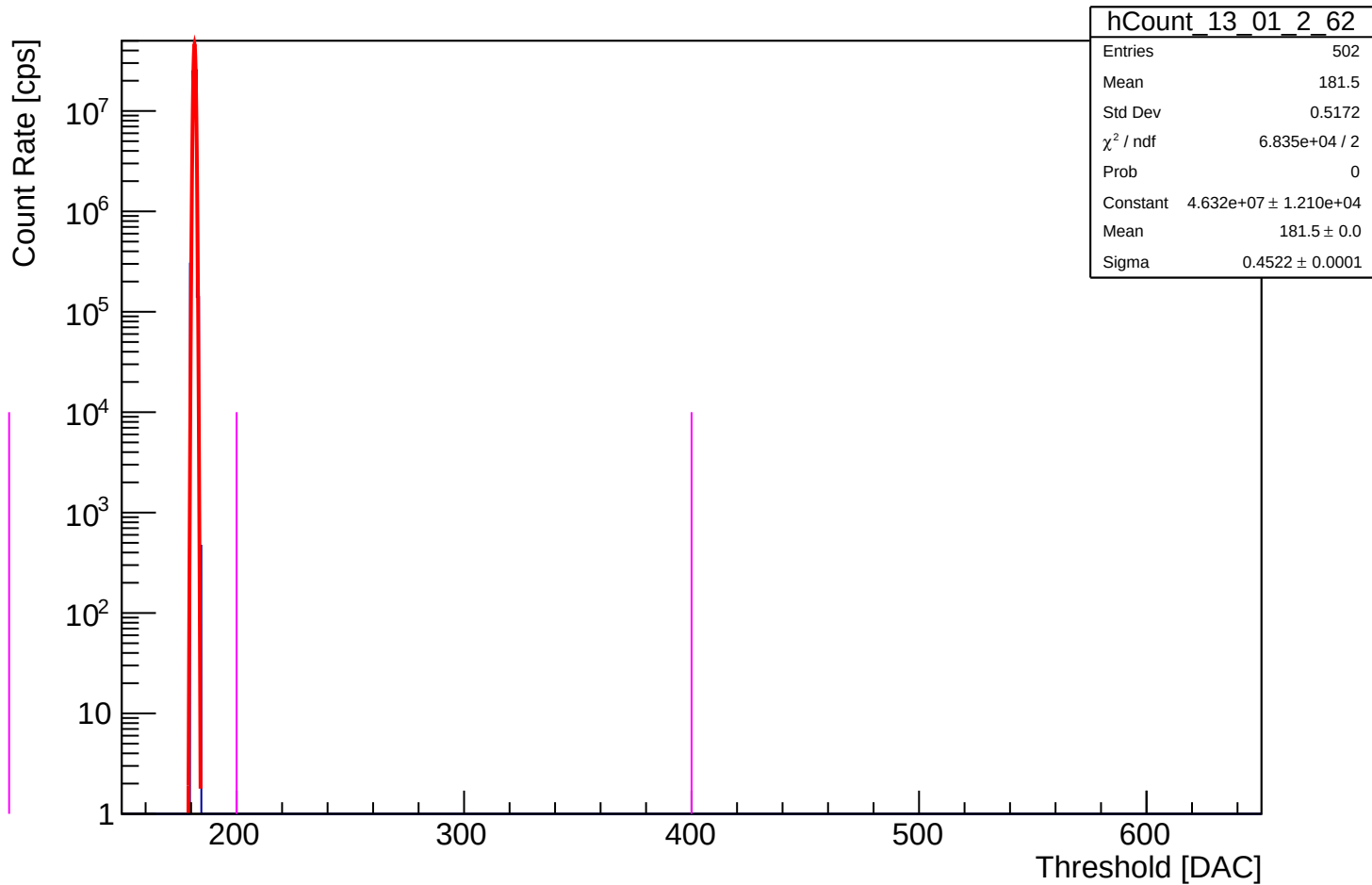




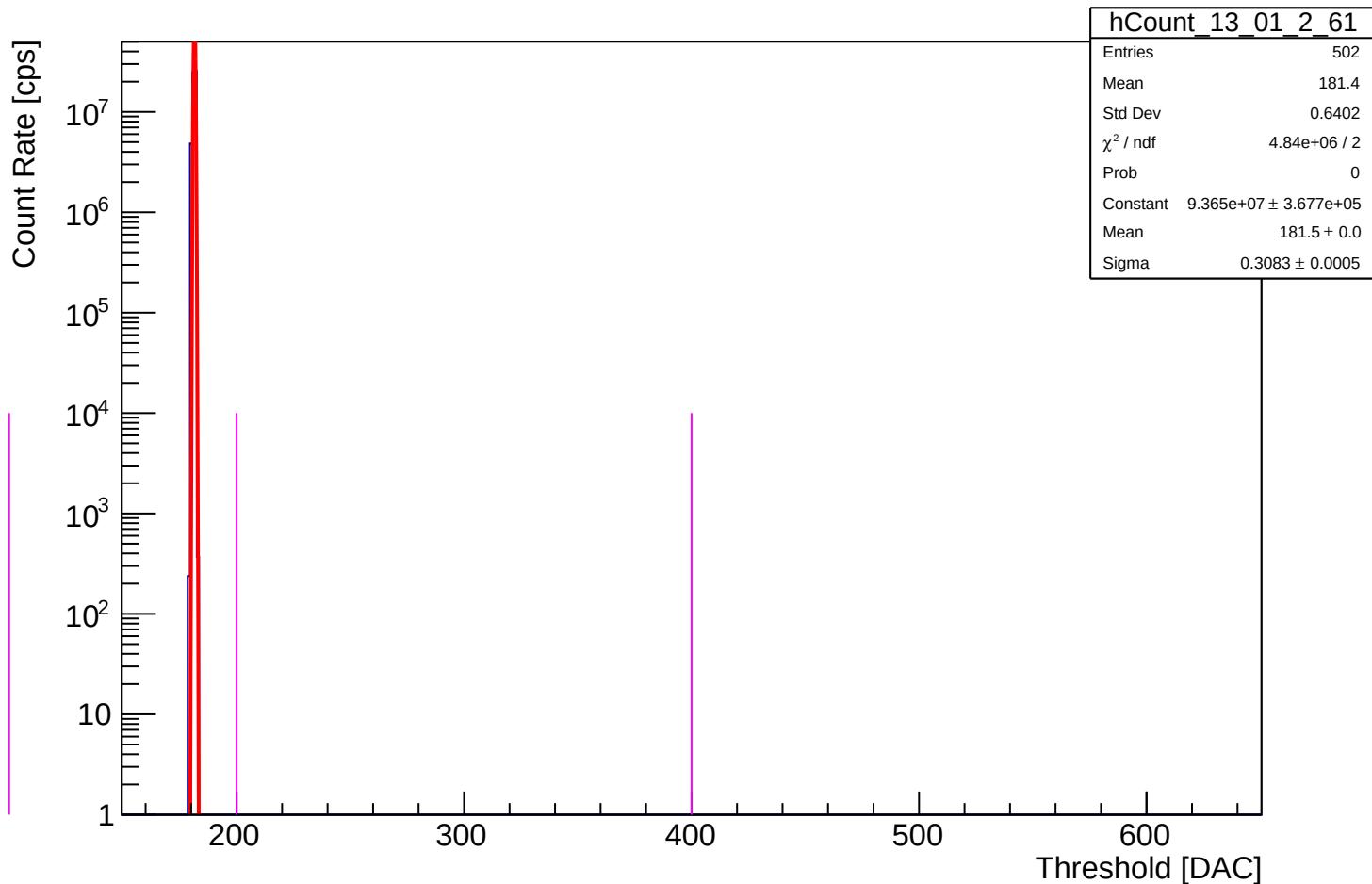
Row 1 Tile 1 Pmt 6 Pixel 61 Slot 13 Fiber 1 Asic 2 Channel 60



Row 1 Tile 1 Pmt 6 Pixel 62 Slot 13 Fiber 1 Asic 2 Channel 62



Row 1 Tile 1 Pmt 6 Pixel 63 Slot 13 Fiber 1 Asic 2 Channel 61



Row 1 Tile 1 Pmt 6 Pixel 64 Slot 13 Fiber 1 Asic 2 Channel 63

