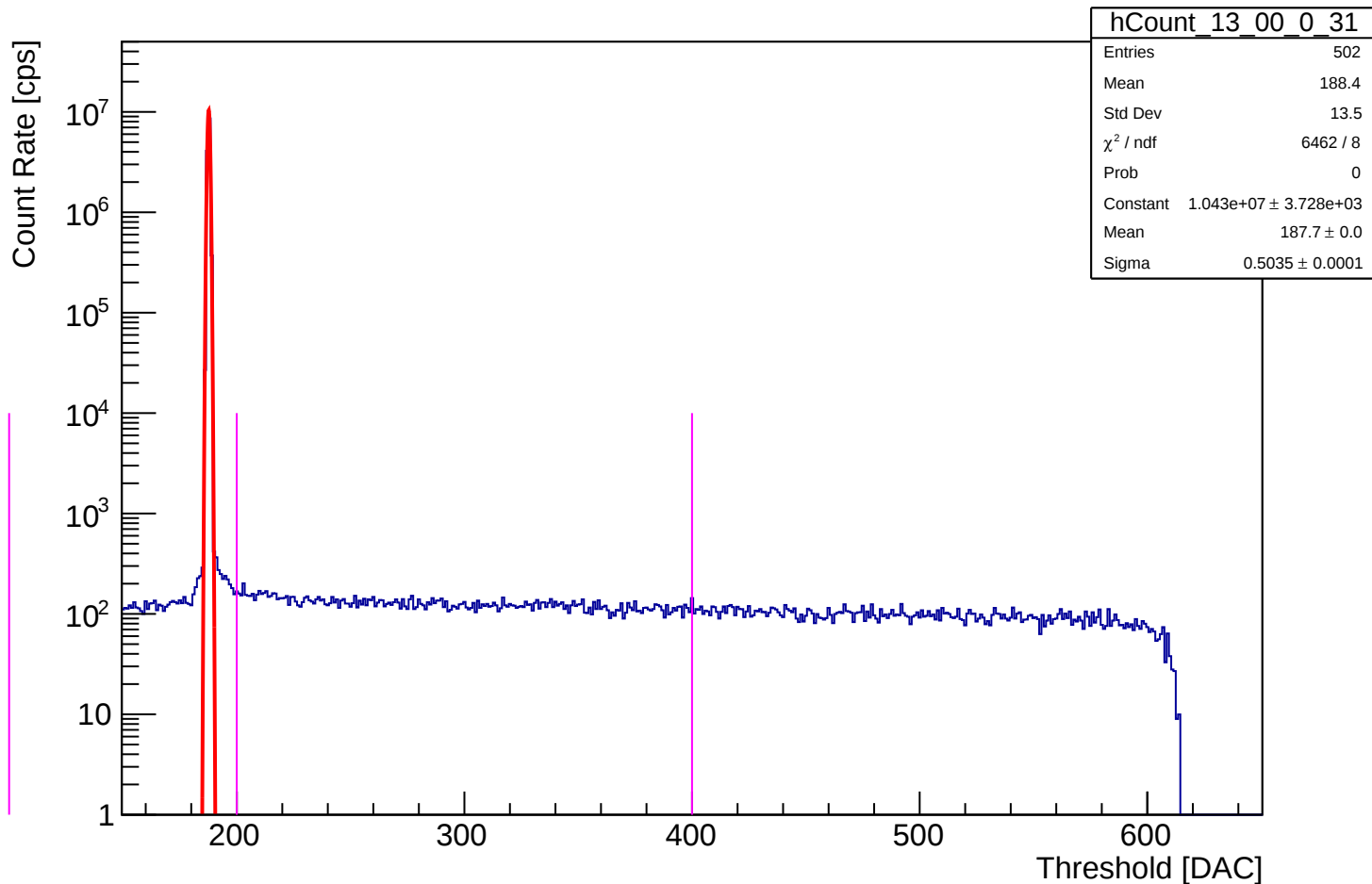
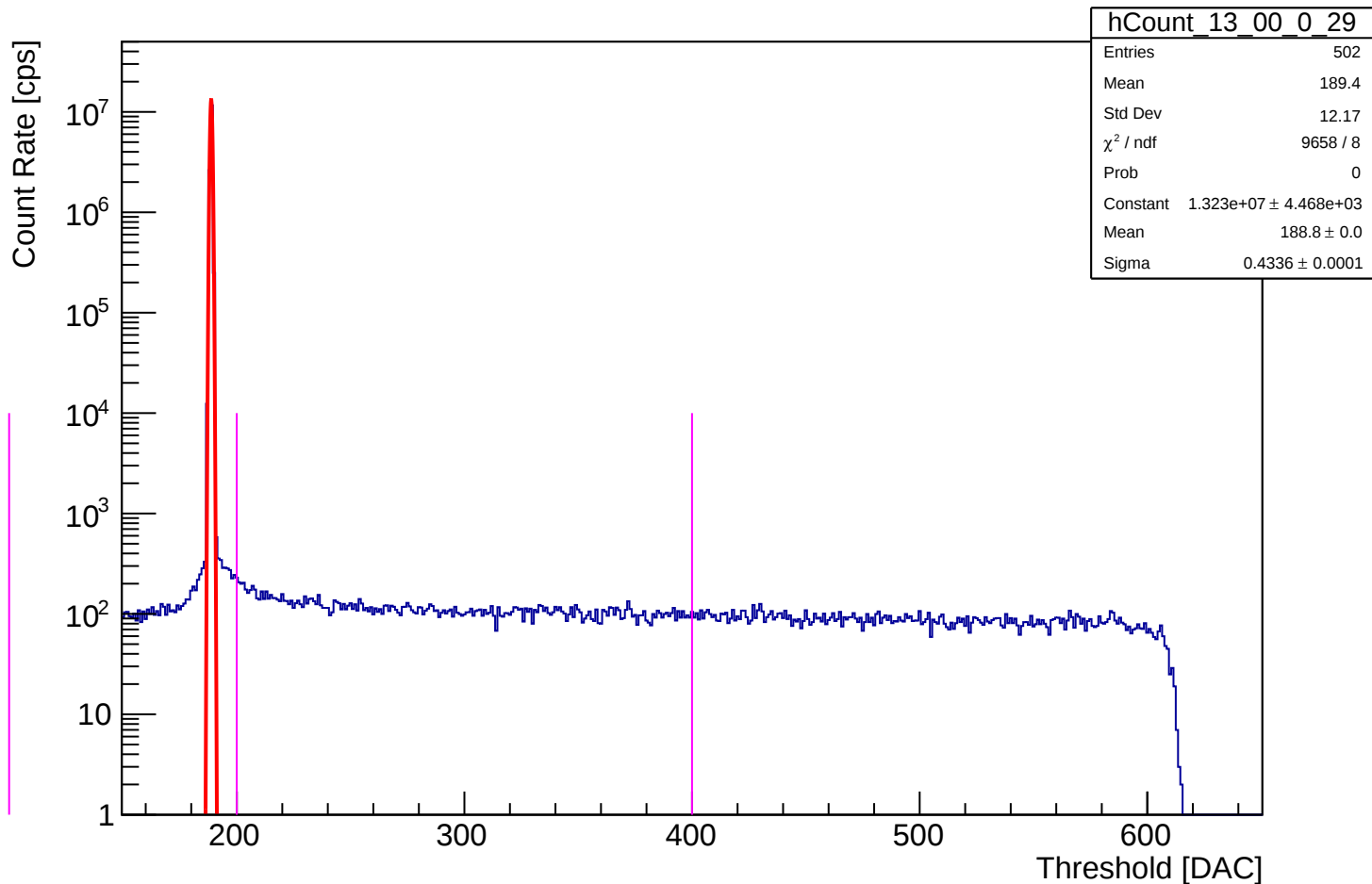


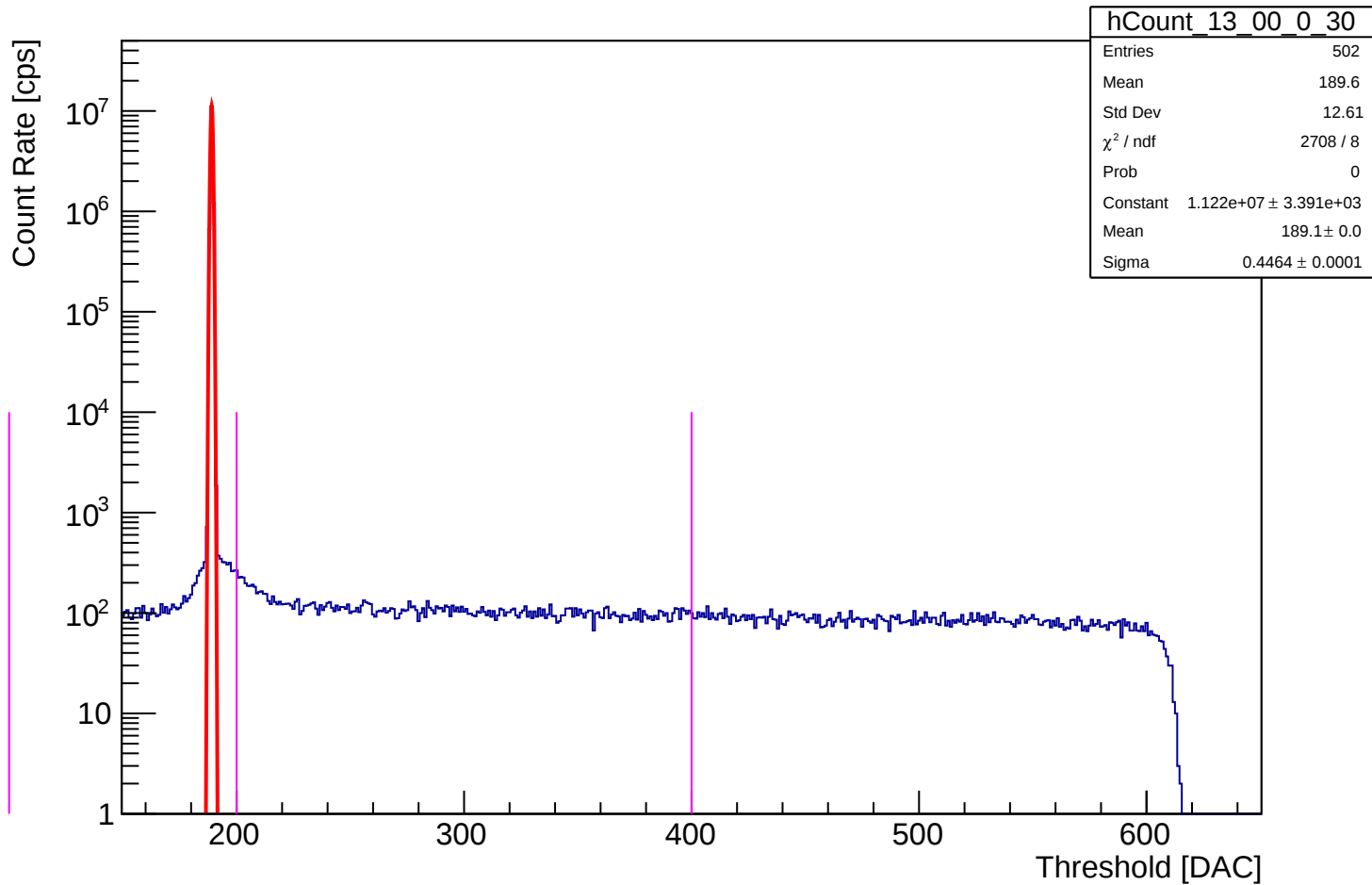
Row 1 Tile 1 Pmt 1 Pixel 1 Slot 13 Fiber 0 Asic 0 Channel 31



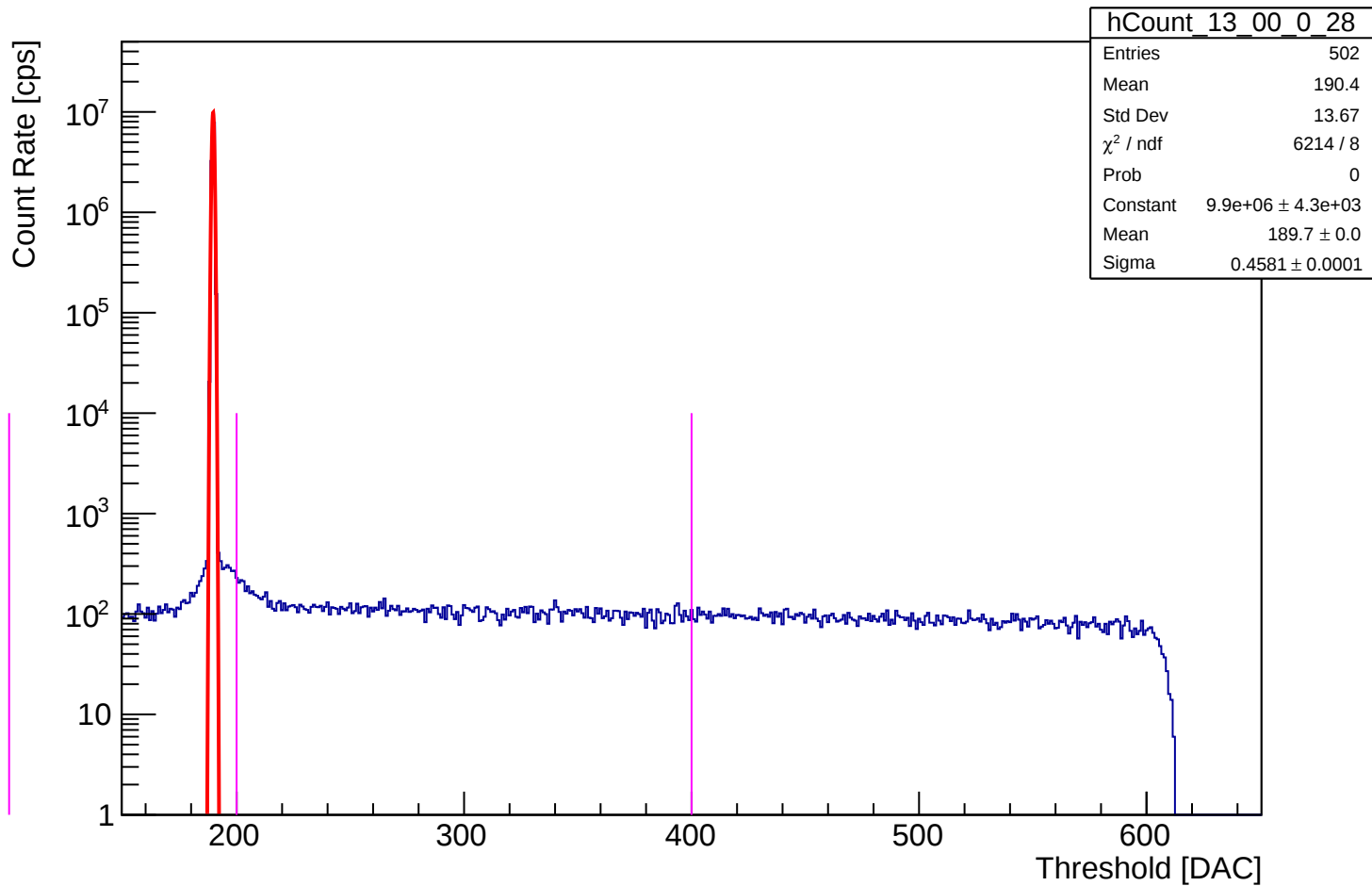
Row 1 Tile 1 Pmt 1 Pixel 2 Slot 13 Fiber 0 Asic 0 Channel 29



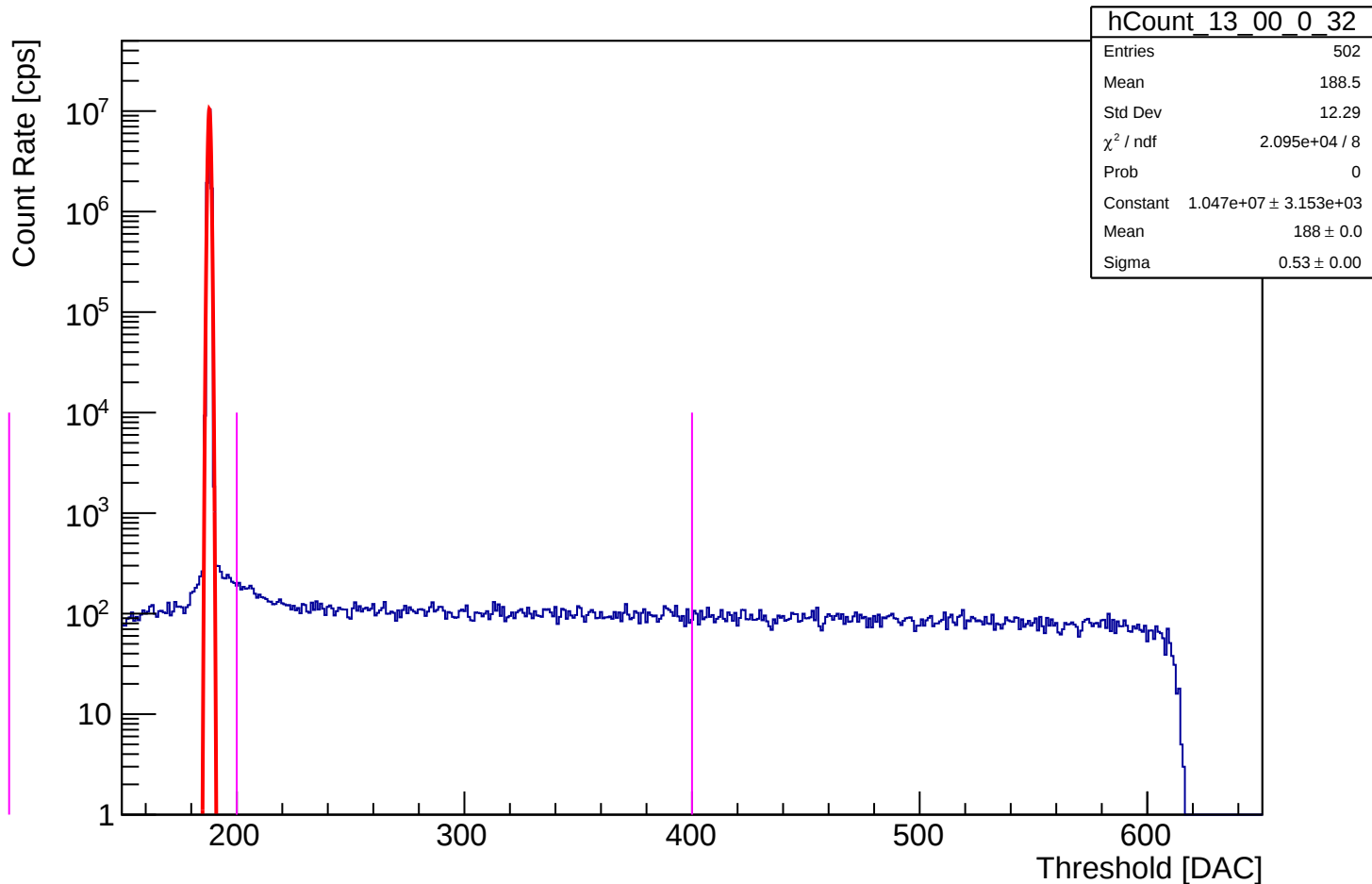
Row 1 Tile 1 Pmt 1 Pixel 3 Slot 13 Fiber 0 Asic 0 Channel 30



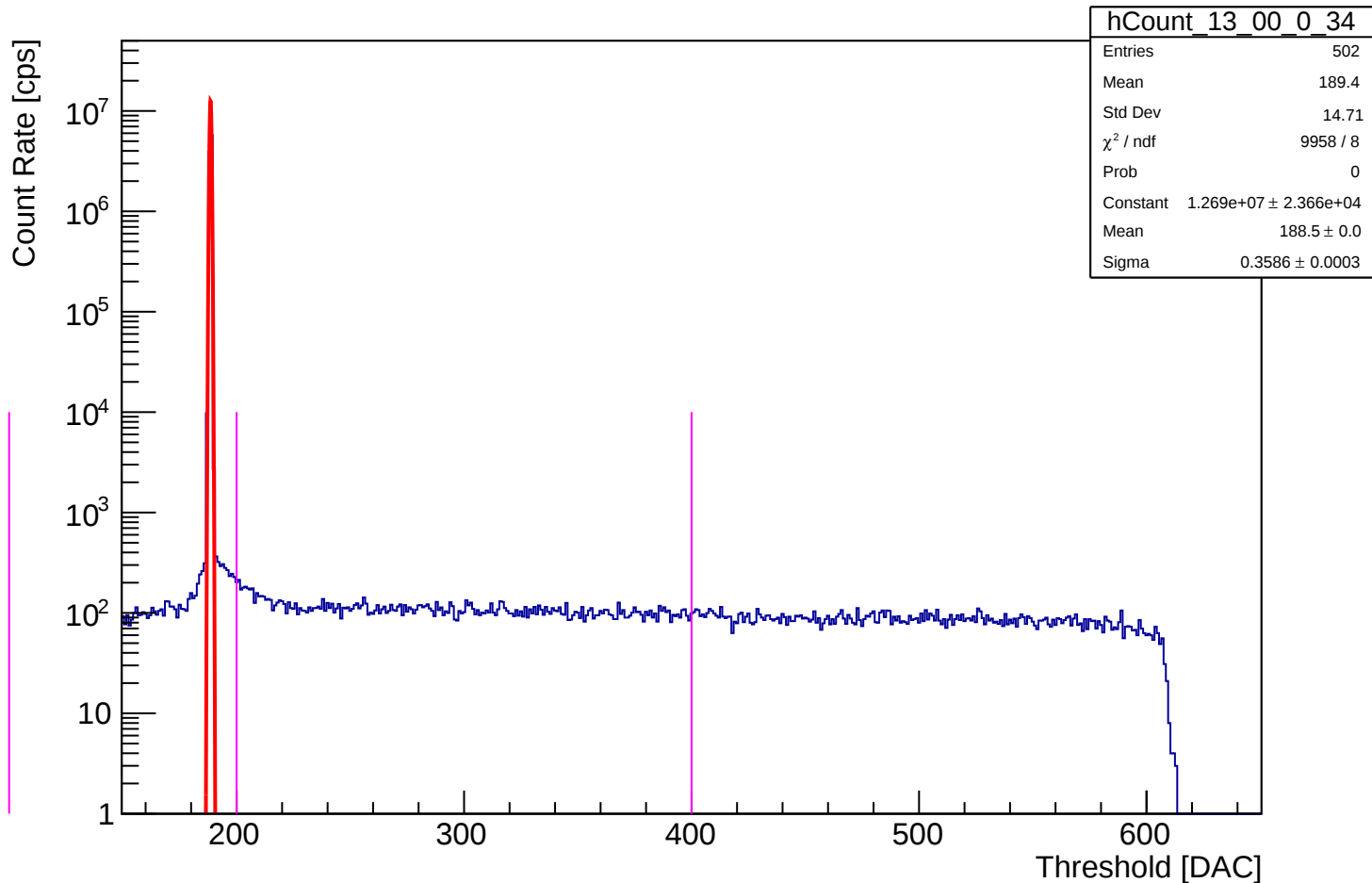
Row 1 Tile 1 Pmt 1 Pixel 4 Slot 13 Fiber 0 Asic 0 Channel 28



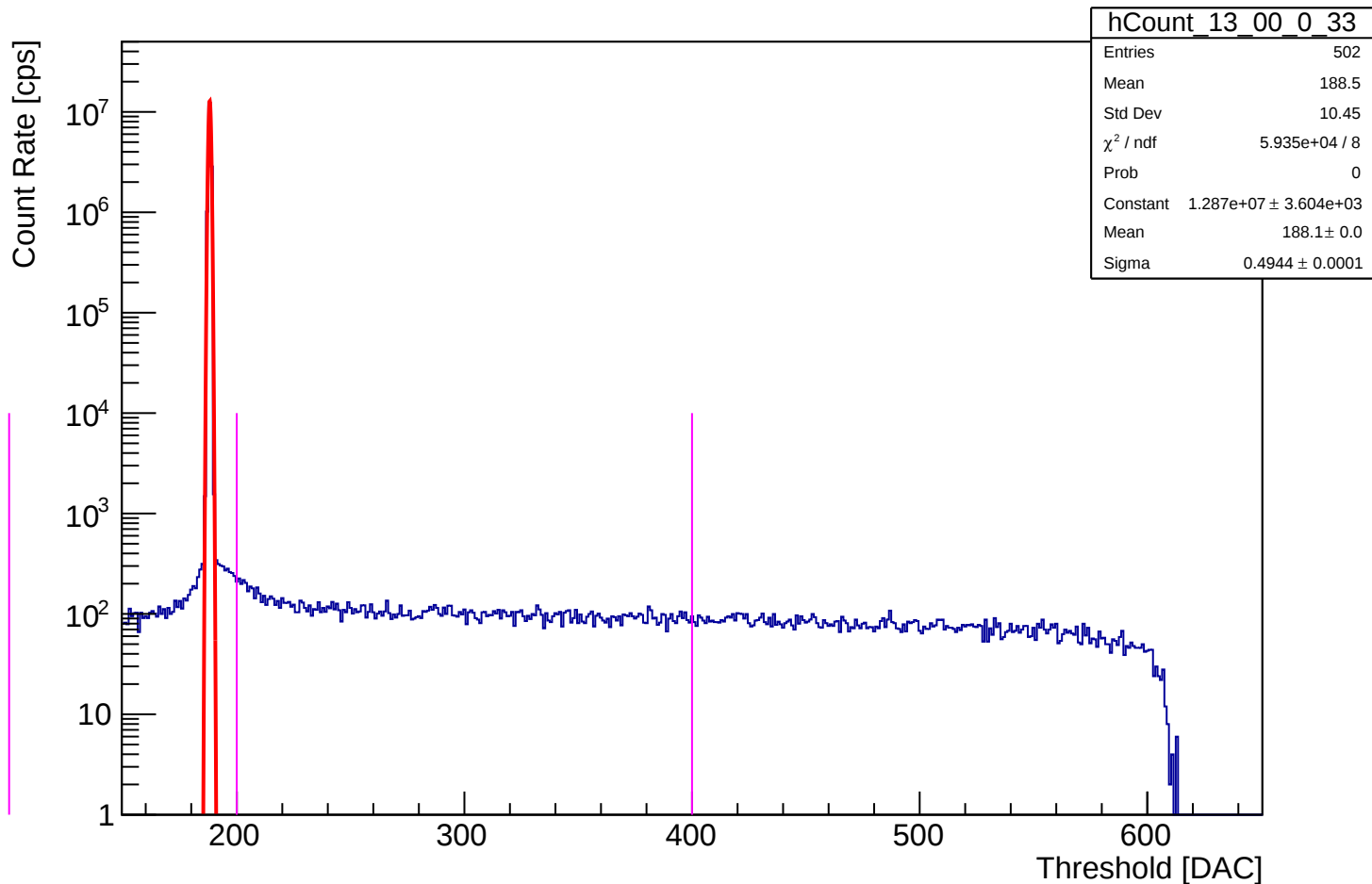
Row 1 Tile 1 Pmt 1 Pixel 5 Slot 13 Fiber 0 Asic 0 Channel 32



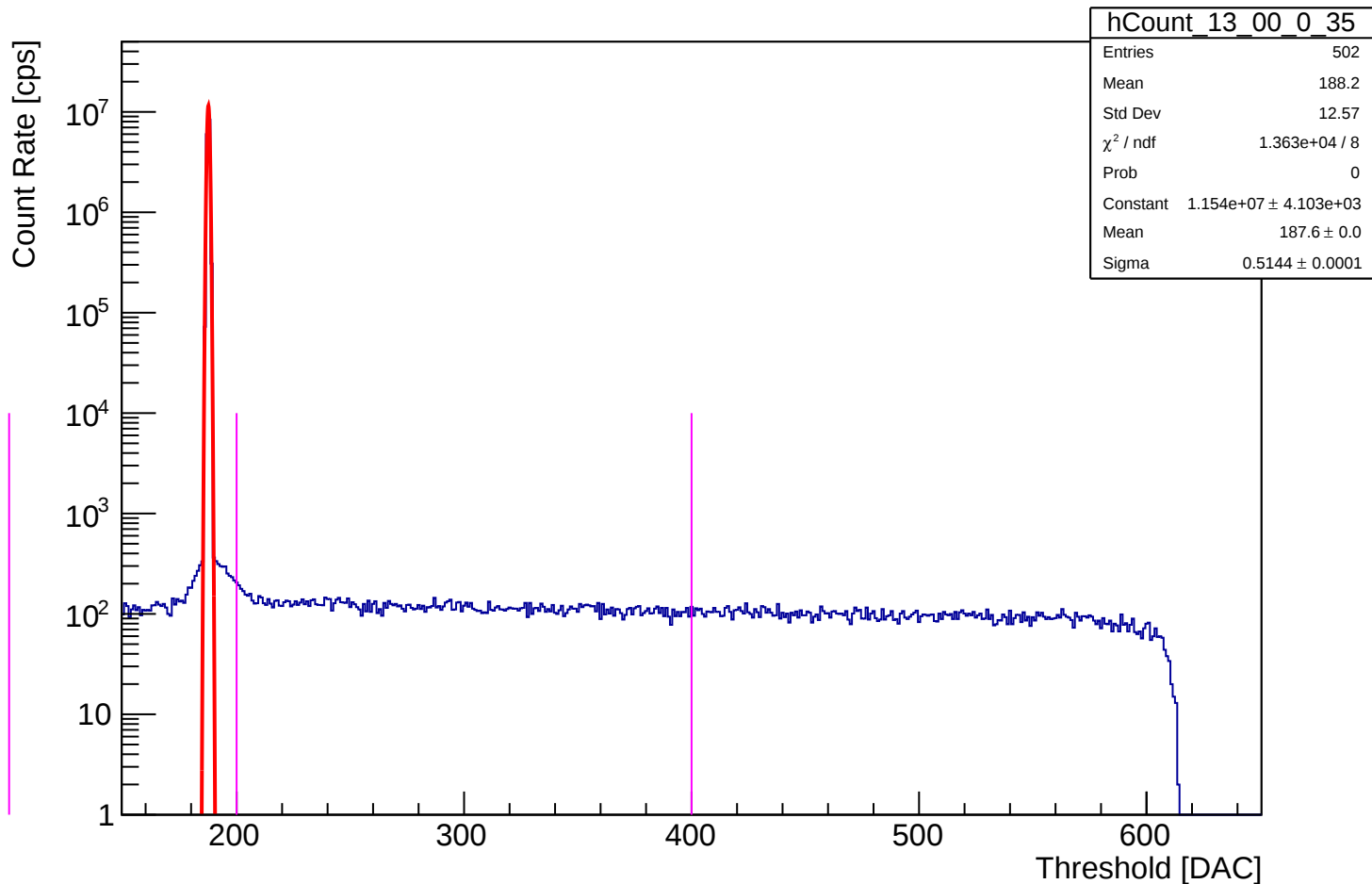
Row 1 Tile 1 Pmt 1 Pixel 6 Slot 13 Fiber 0 Asic 0 Channel 34



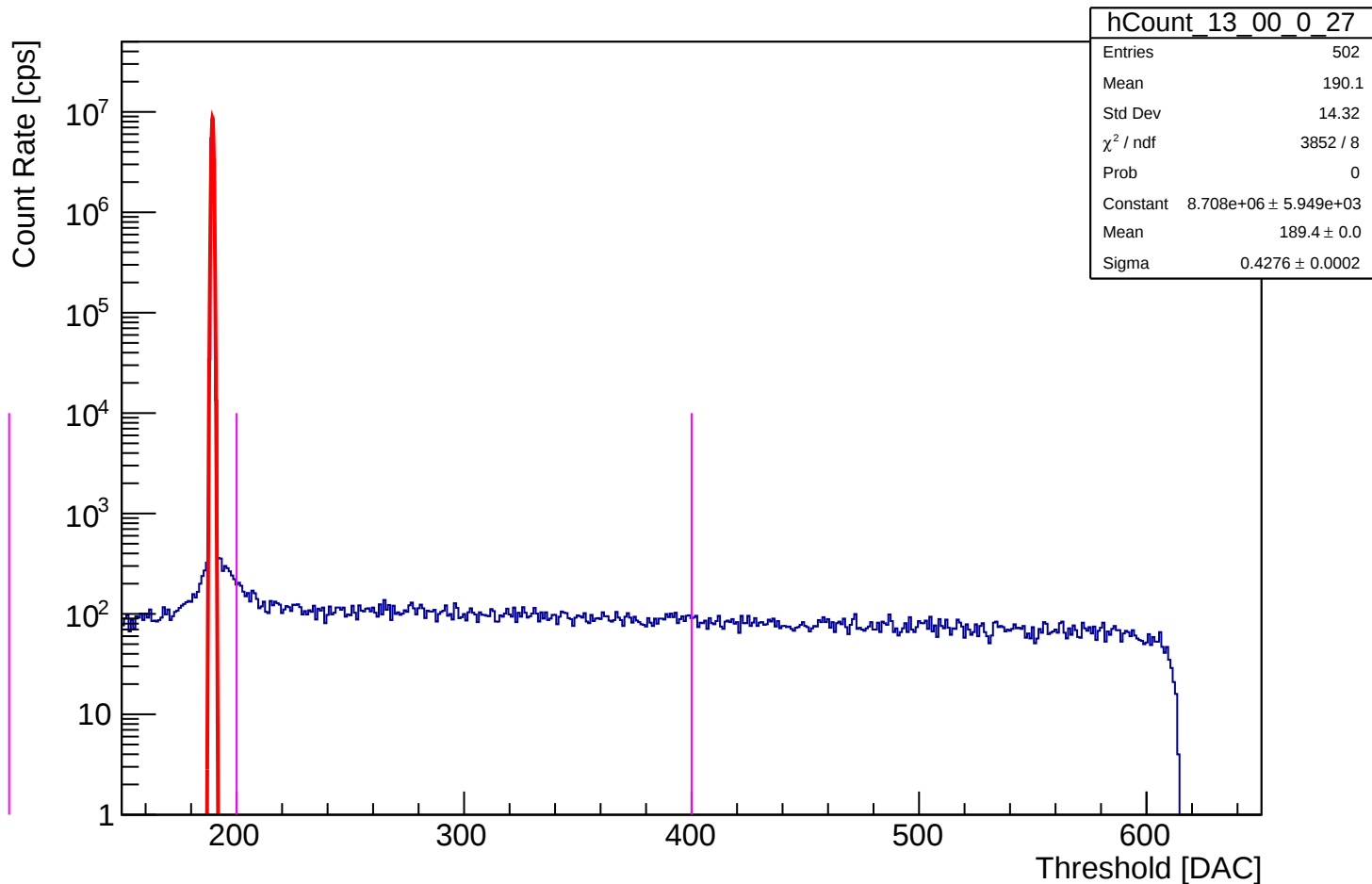
Row 1 Tile 1 Pmt 1 Pixel 7 Slot 13 Fiber 0 Asic 0 Channel 33



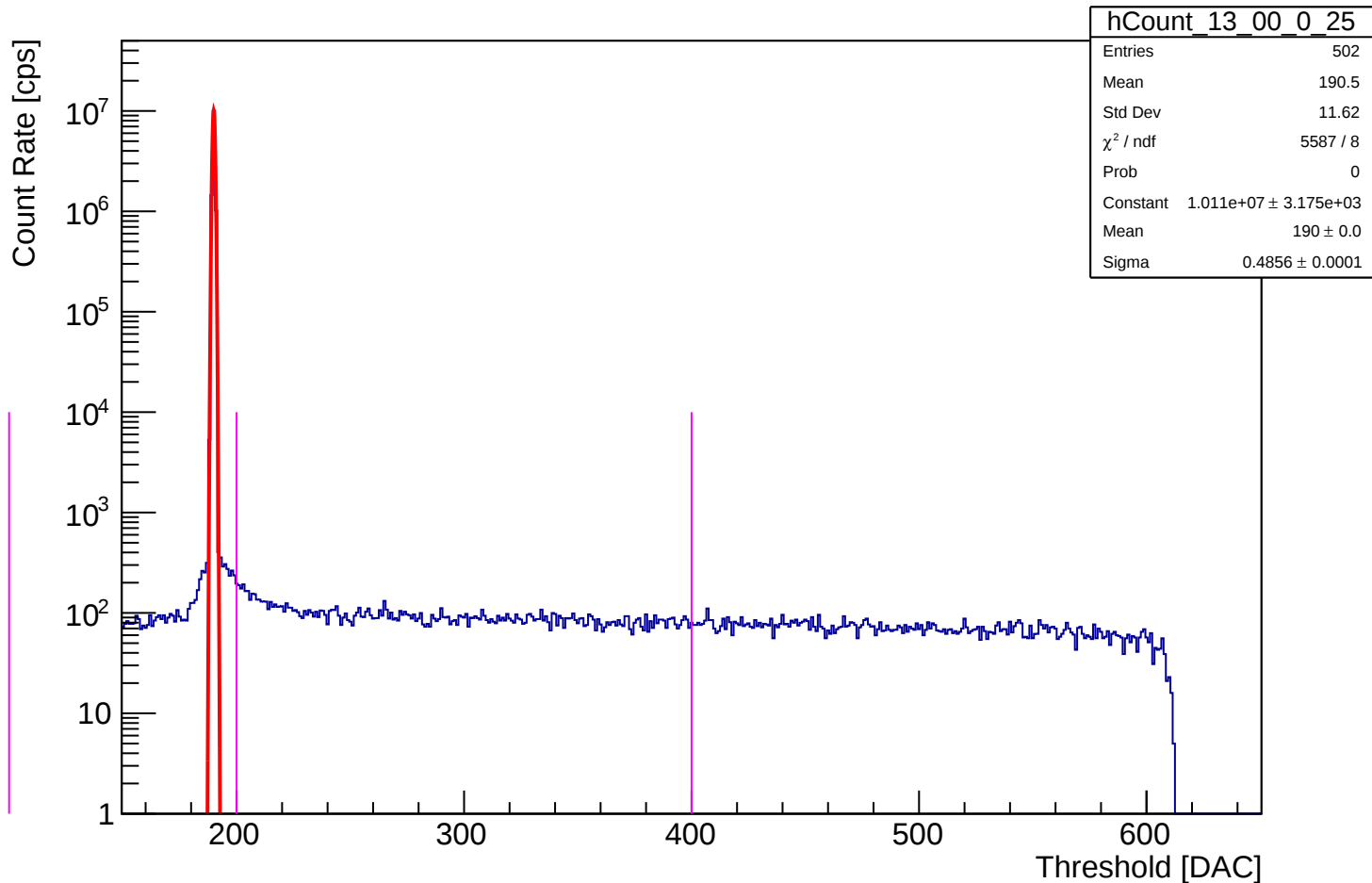
Row 1 Tile 1 Pmt 1 Pixel 8 Slot 13 Fiber 0 Asic 0 Channel 35



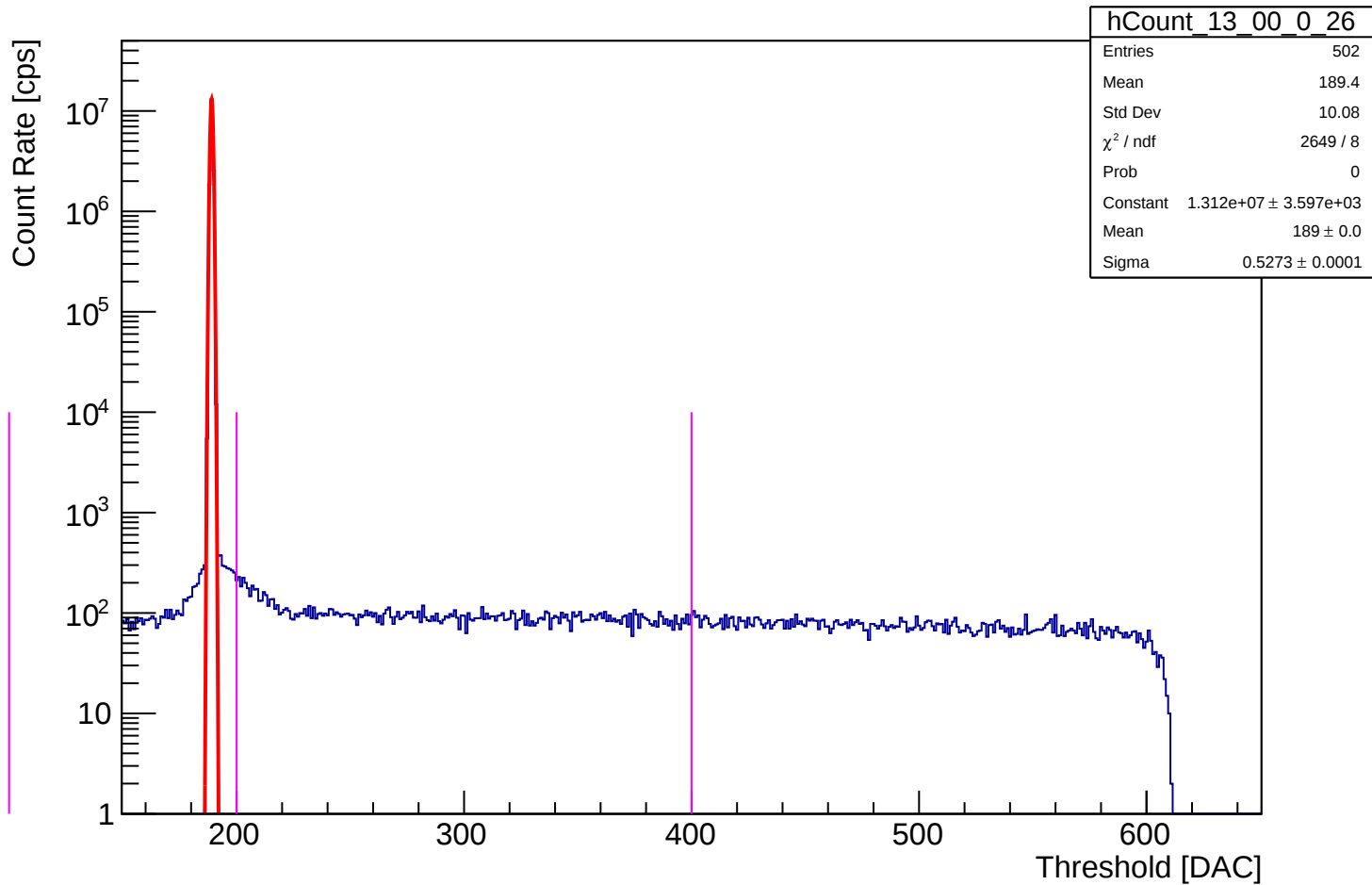
Row 1 Tile 1 Pmt 1 Pixel 9 Slot 13 Fiber 0 Asic 0 Channel 27



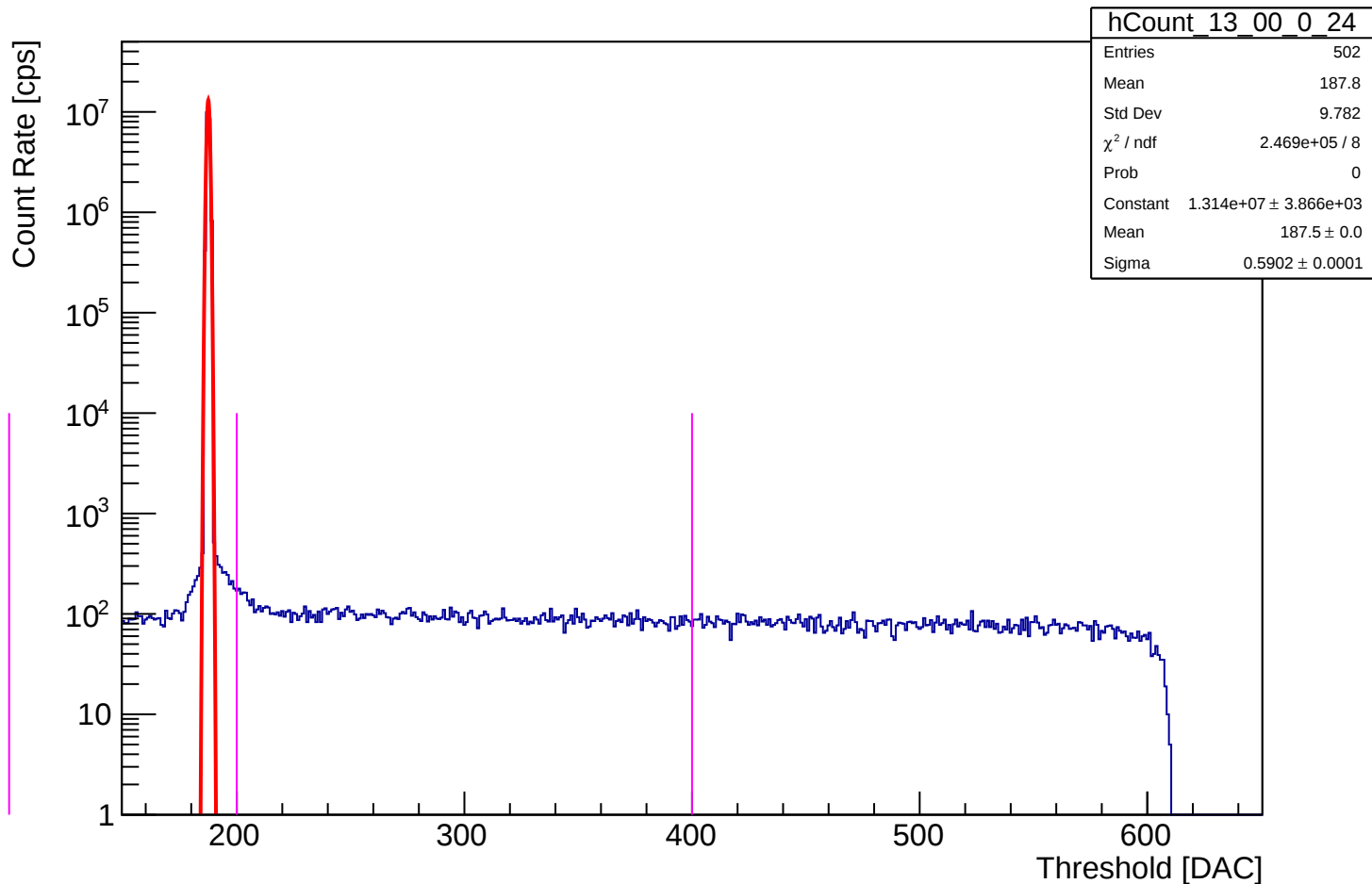
Row 1 Tile 1 Pmt 1 Pixel 10 Slot 13 Fiber 0 Asic 0 Channel 25



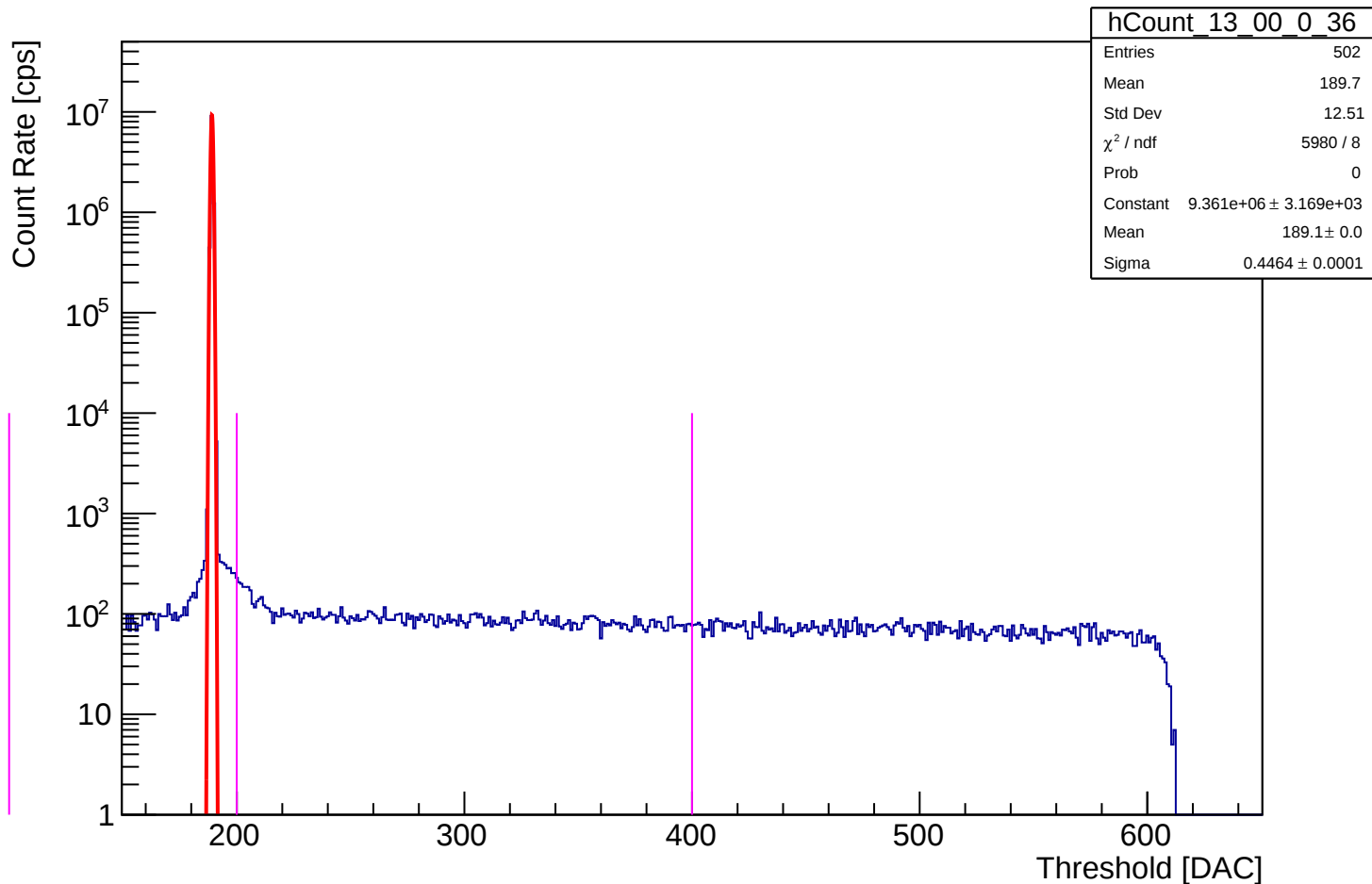
Row 1 Tile 1 Pmt 1 Pixel 11 Slot 13 Fiber 0 Asic 0 Channel 26



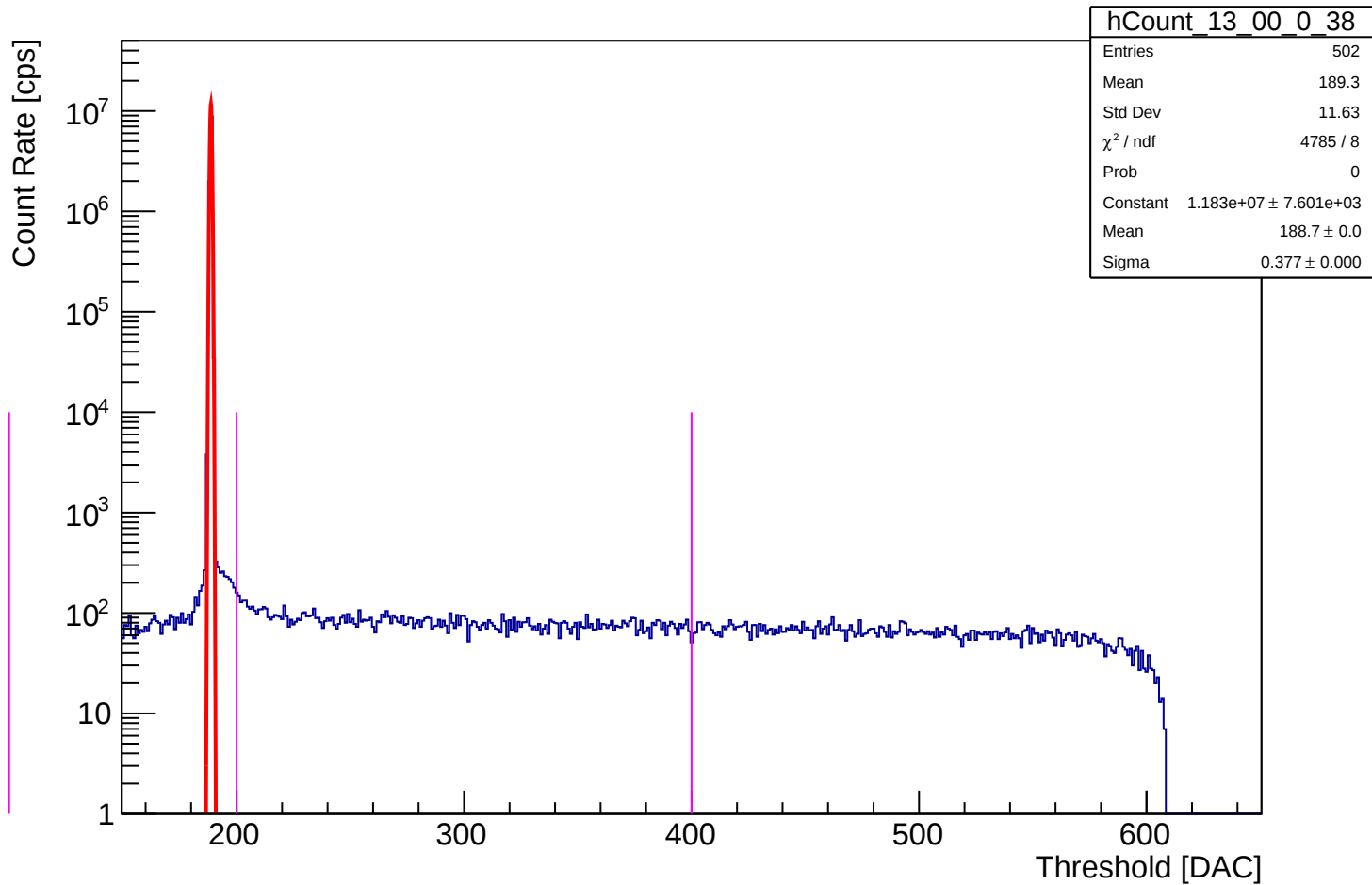
Row 1 Tile 1 Pmt 1 Pixel 12 Slot 13 Fiber 0 Asic 0 Channel 24



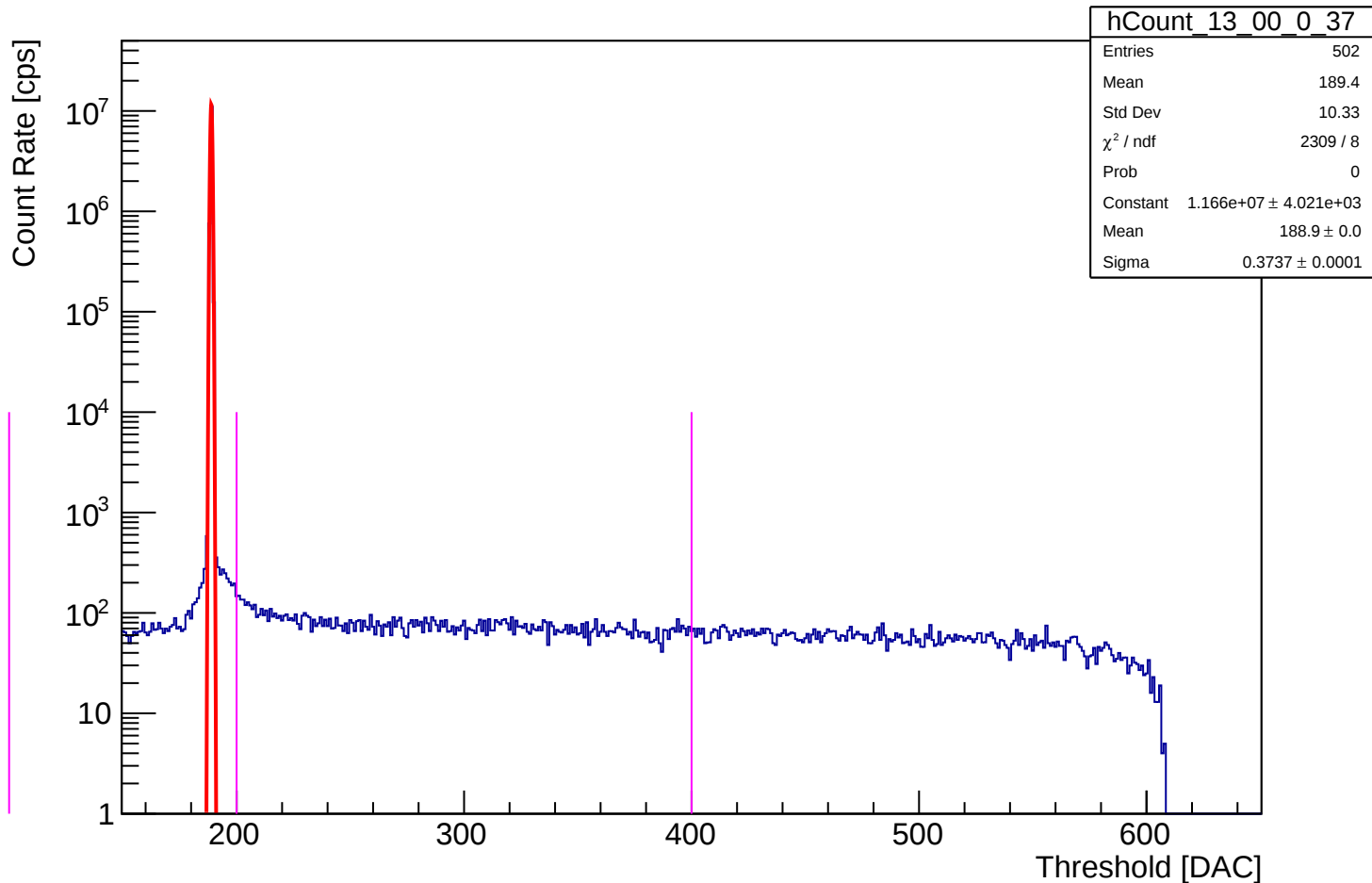
Row 1 Tile 1 Pmt 1 Pixel 13 Slot 13 Fiber 0 Asic 0 Channel 36



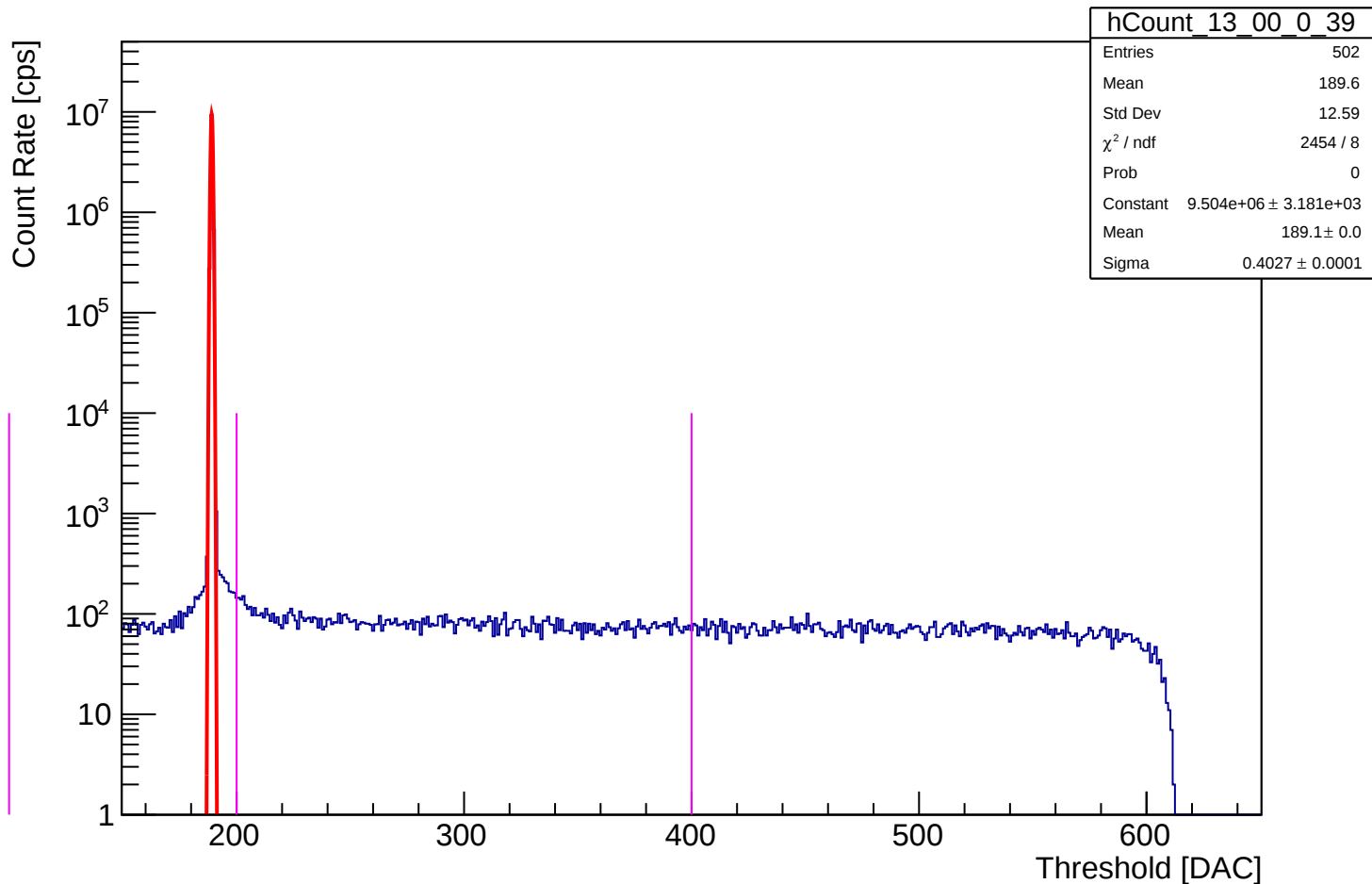
Row 1 Tile 1 Pmt 1 Pixel 14 Slot 13 Fiber 0 Asic 0 Channel 38



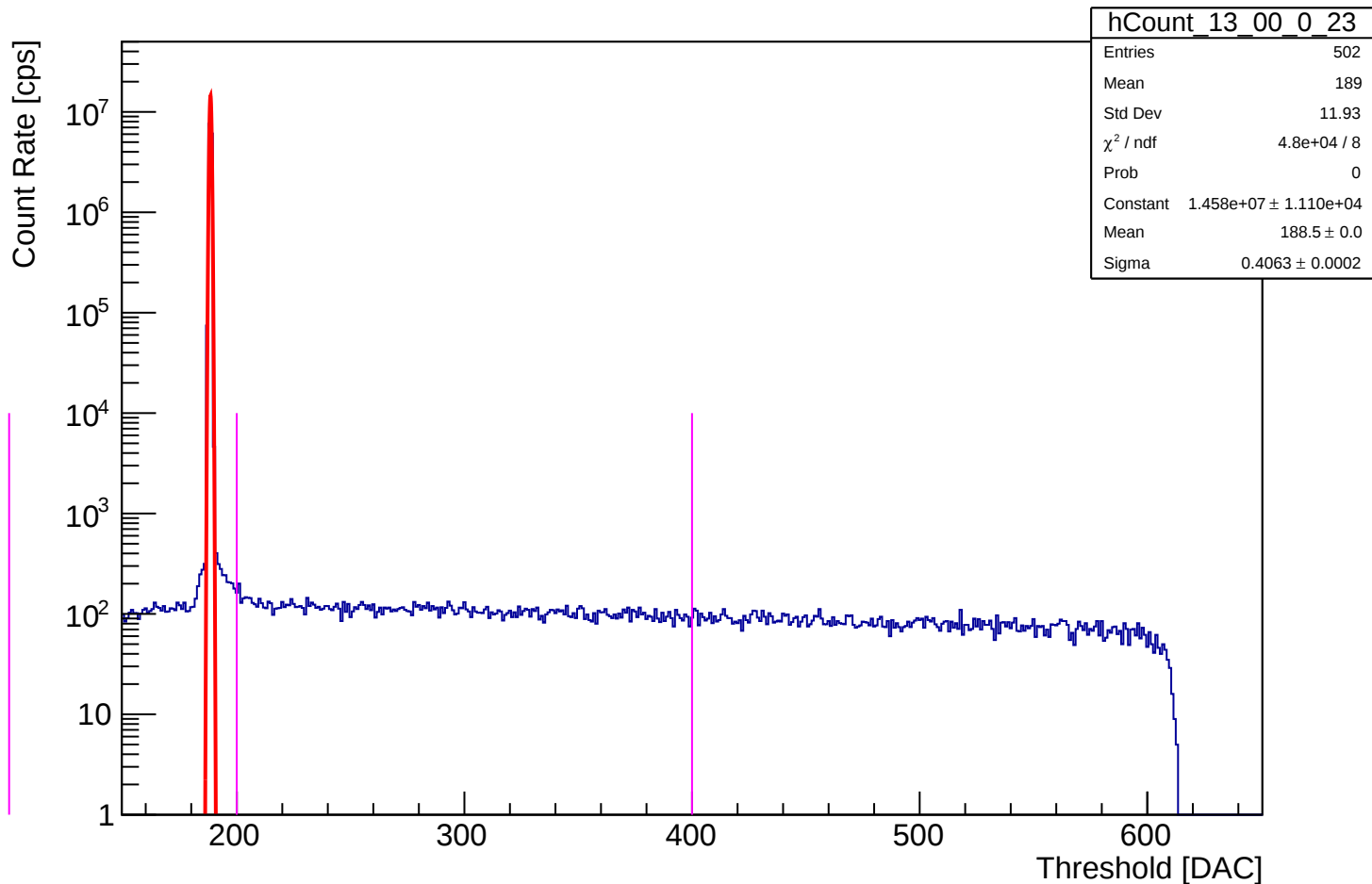
Row 1 Tile 1 Pmt 1 Pixel 15 Slot 13 Fiber 0 Asic 0 Channel 37



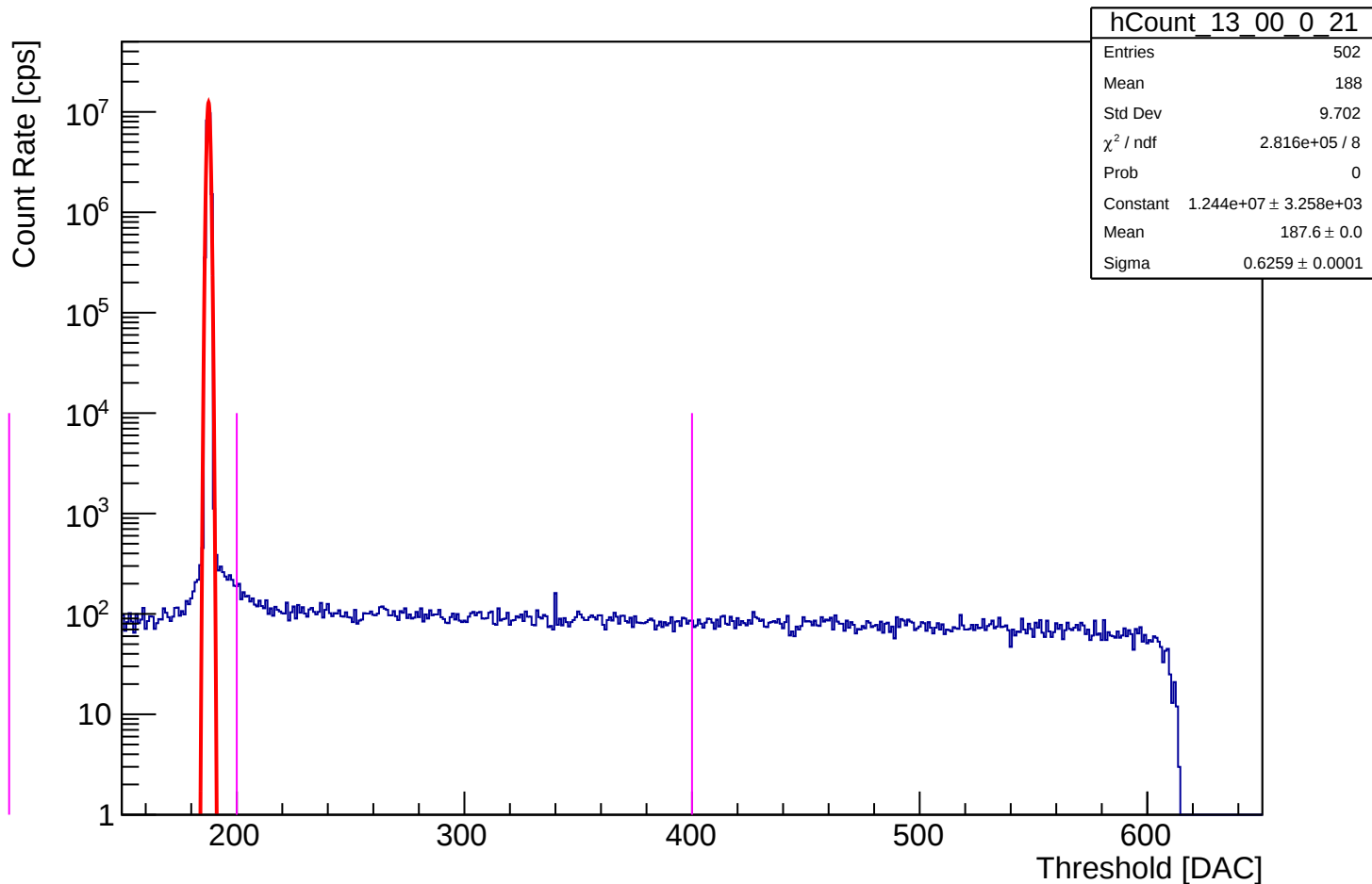
Row 1 Tile 1 Pmt 1 Pixel 16 Slot 13 Fiber 0 Asic 0 Channel 39



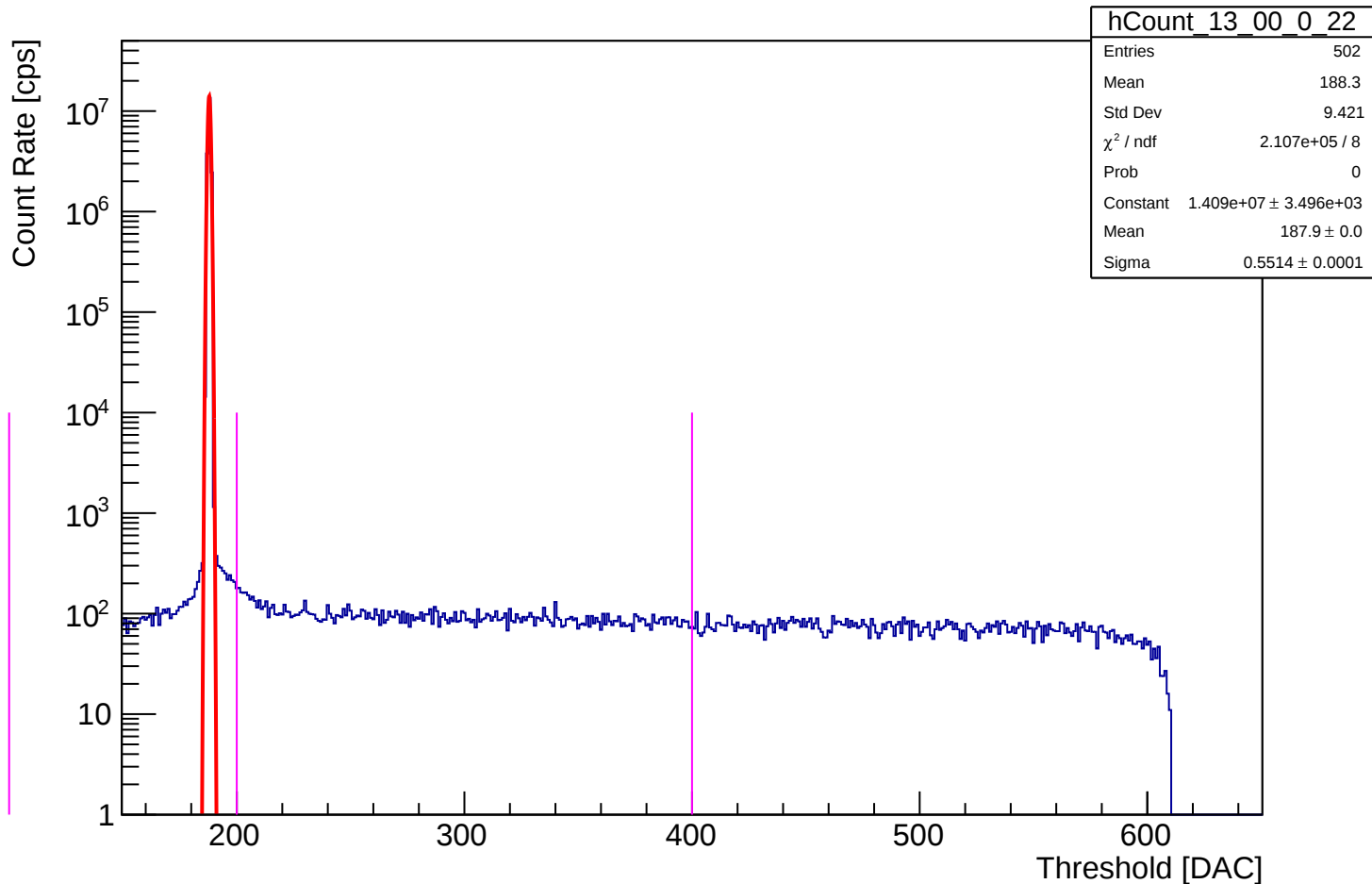
Row 1 Tile 1 Pmt 1 Pixel 17 Slot 13 Fiber 0 Asic 0 Channel 23



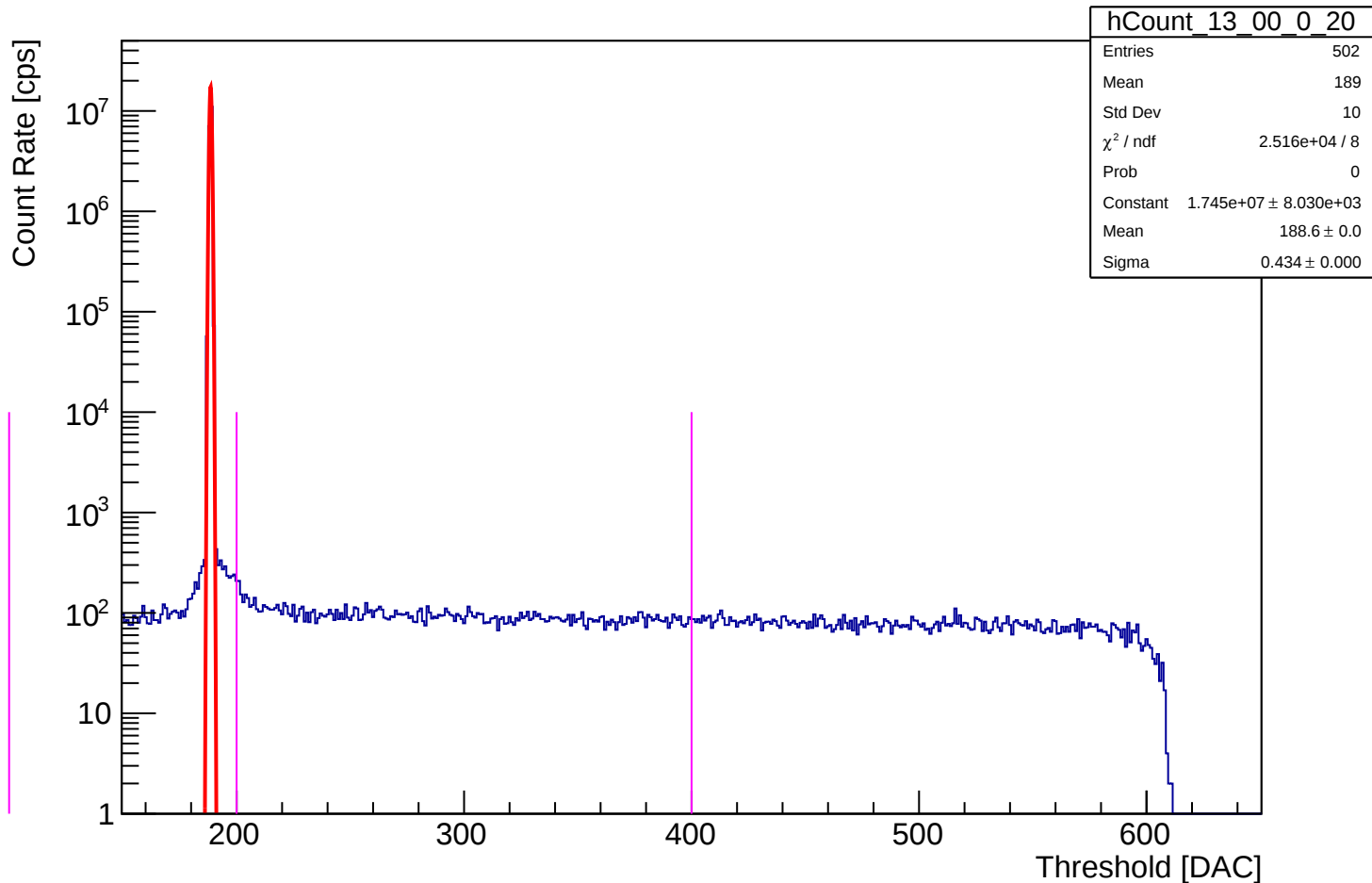
Row 1 Tile 1 Pmt 1 Pixel 18 Slot 13 Fiber 0 Asic 0 Channel 21



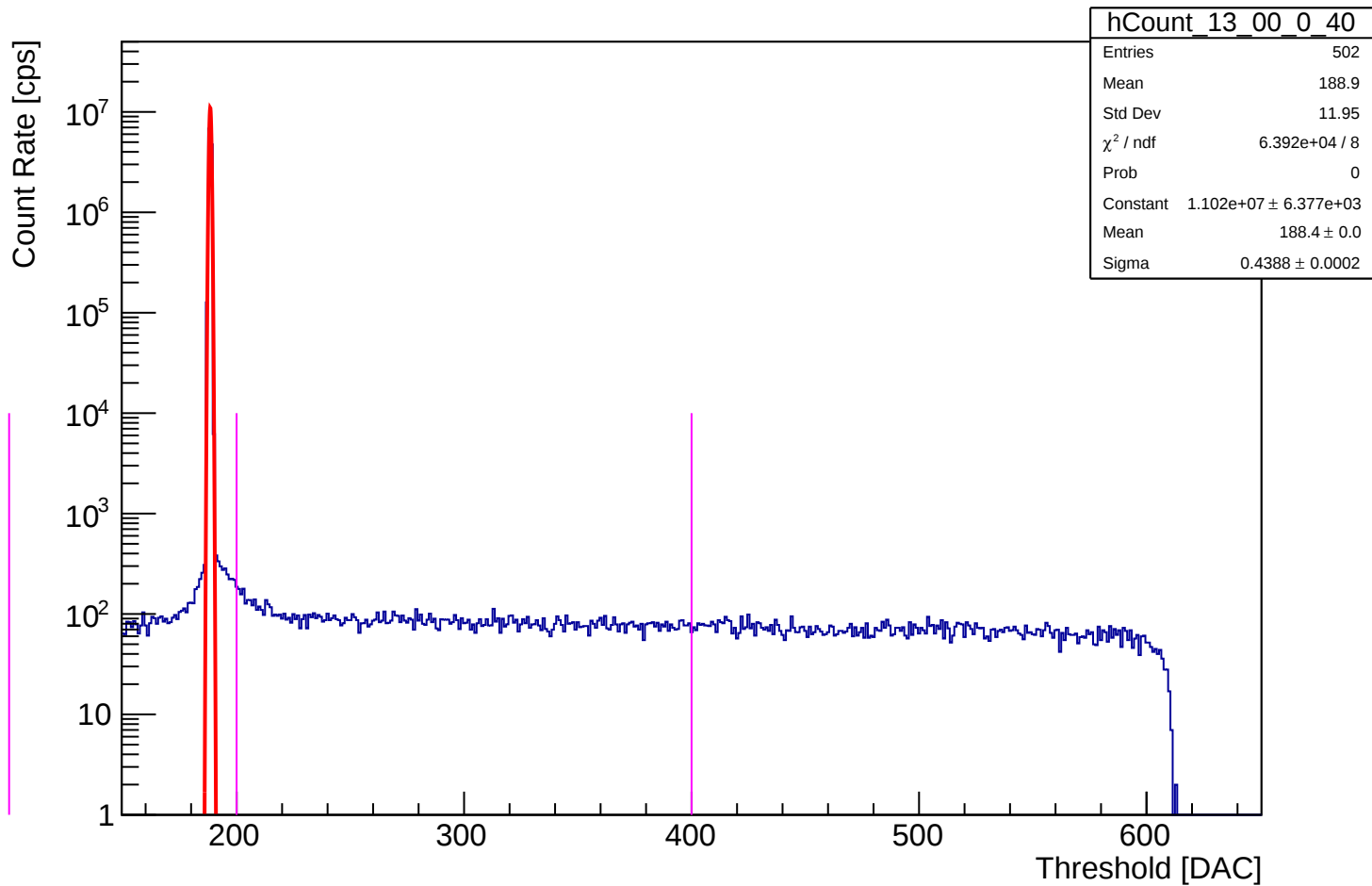
Row 1 Tile 1 Pmt 1 Pixel 19 Slot 13 Fiber 0 Asic 0 Channel 22



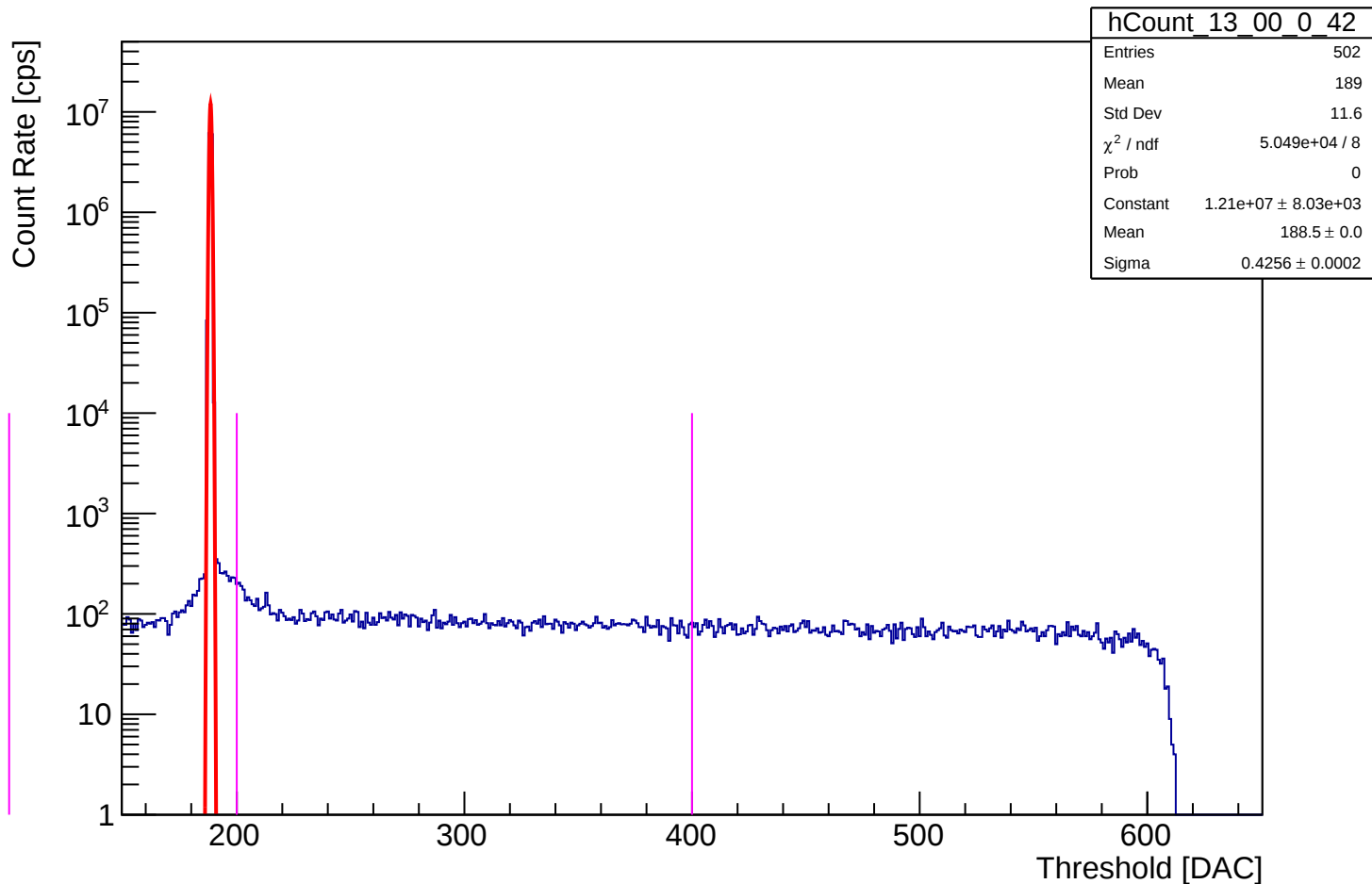
Row 1 Tile 1 Pmt 1 Pixel 20 Slot 13 Fiber 0 Asic 0 Channel 20



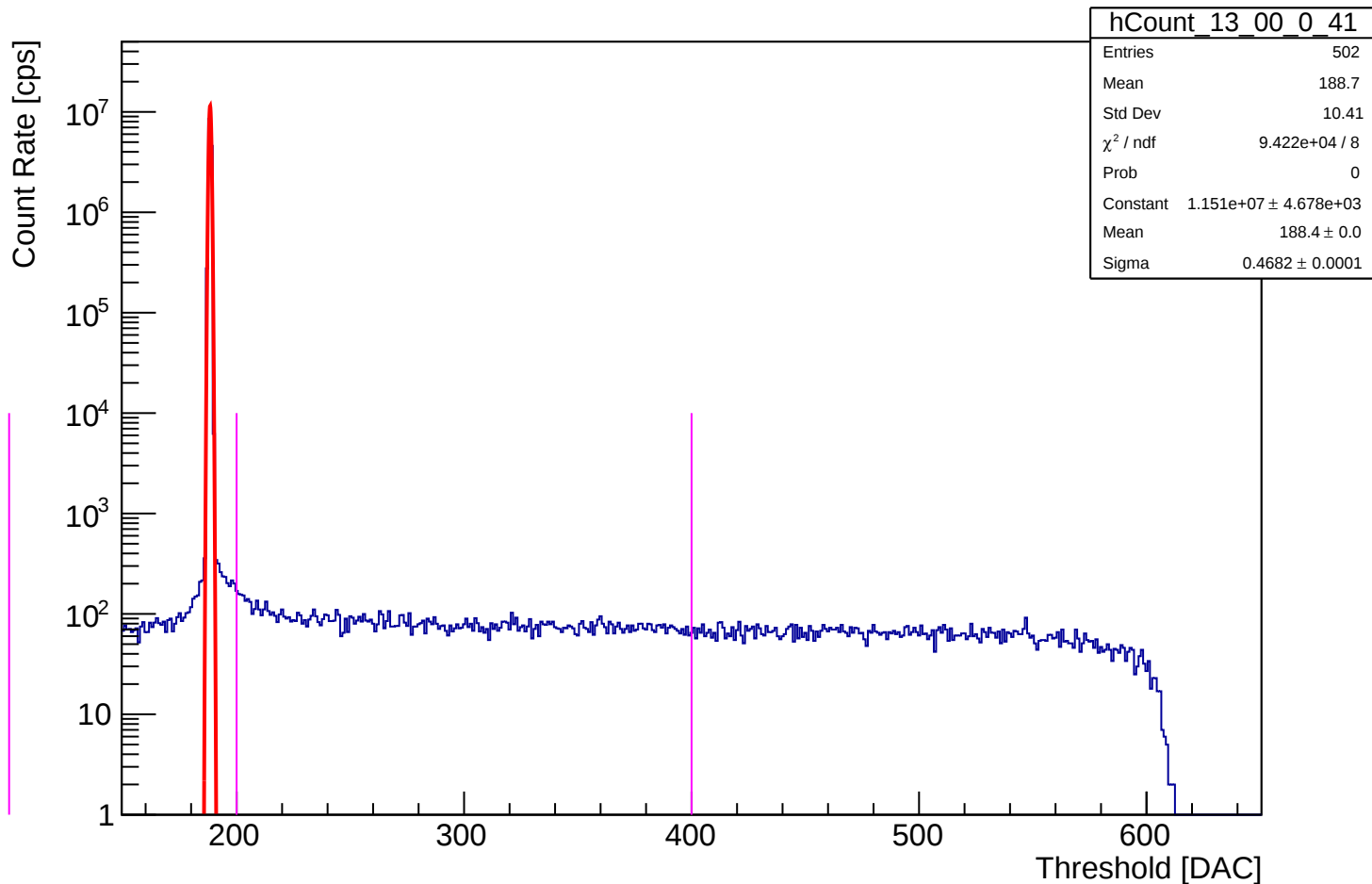
Row 1 Tile 1 Pmt 1 Pixel 21 Slot 13 Fiber 0 Asic 0 Channel 40



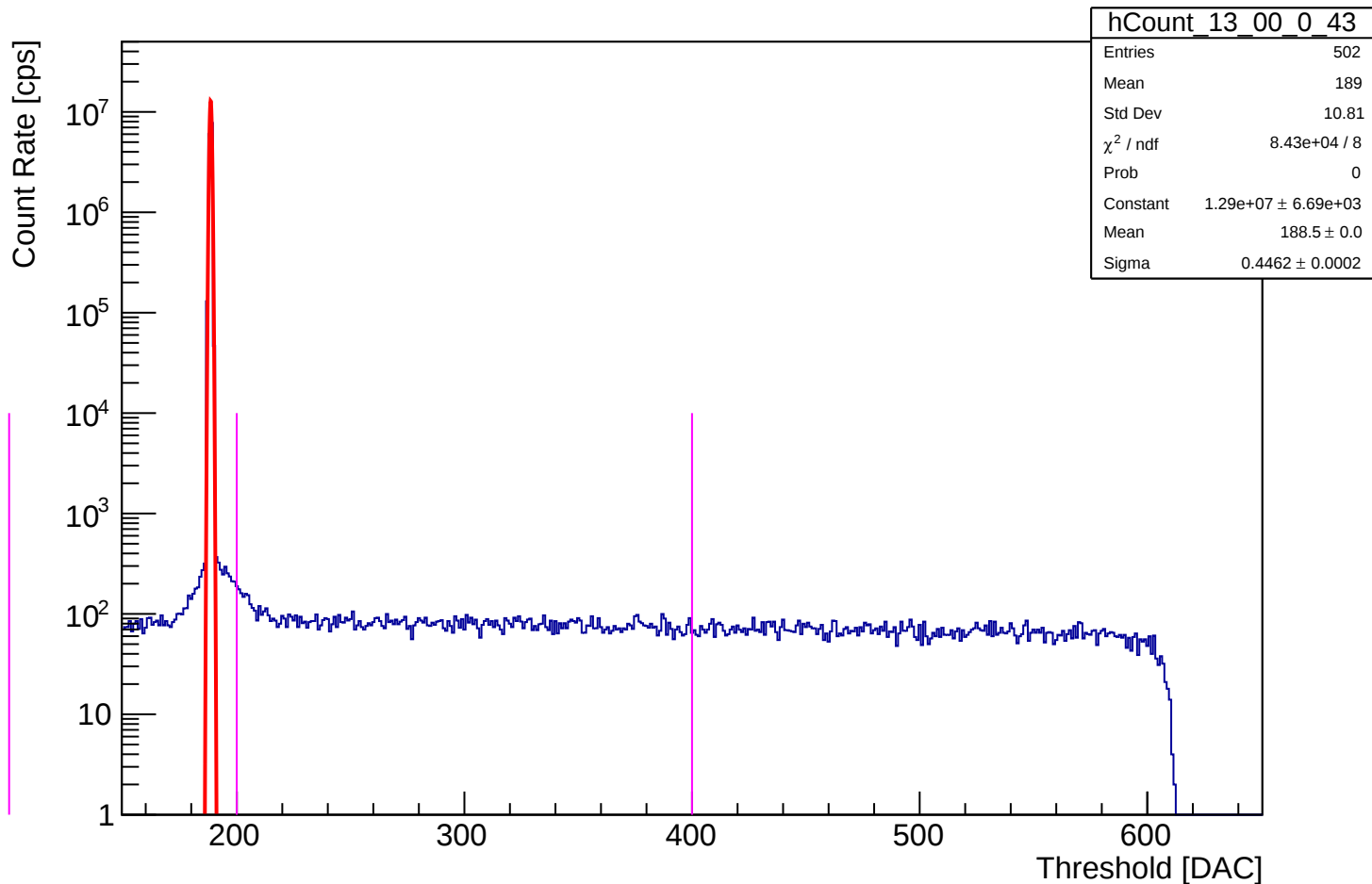
Row 1 Tile 1 Pmt 1 Pixel 22 Slot 13 Fiber 0 Asic 0 Channel 42



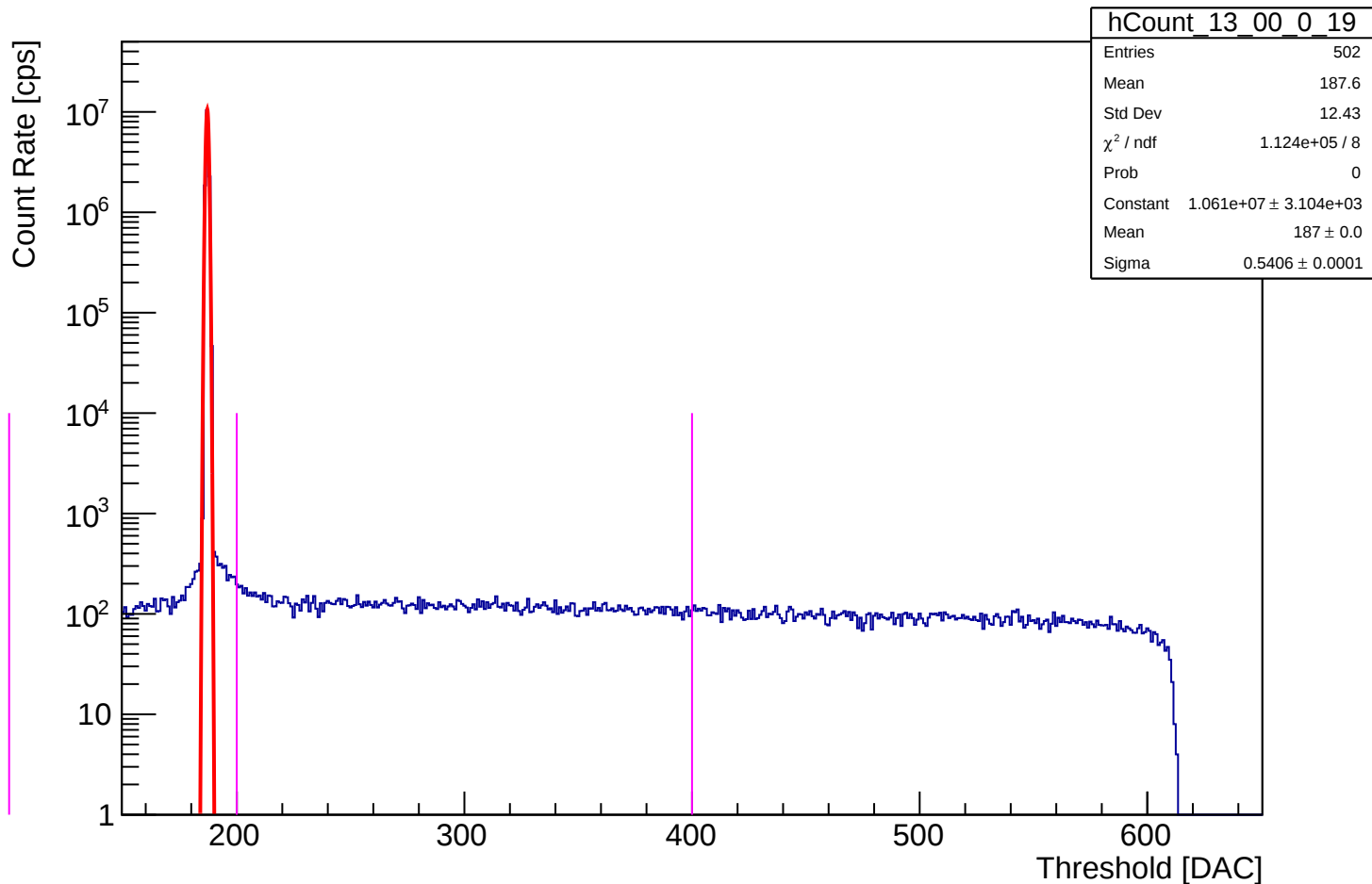
Row 1 Tile 1 Pmt 1 Pixel 23 Slot 13 Fiber 0 Asic 0 Channel 41



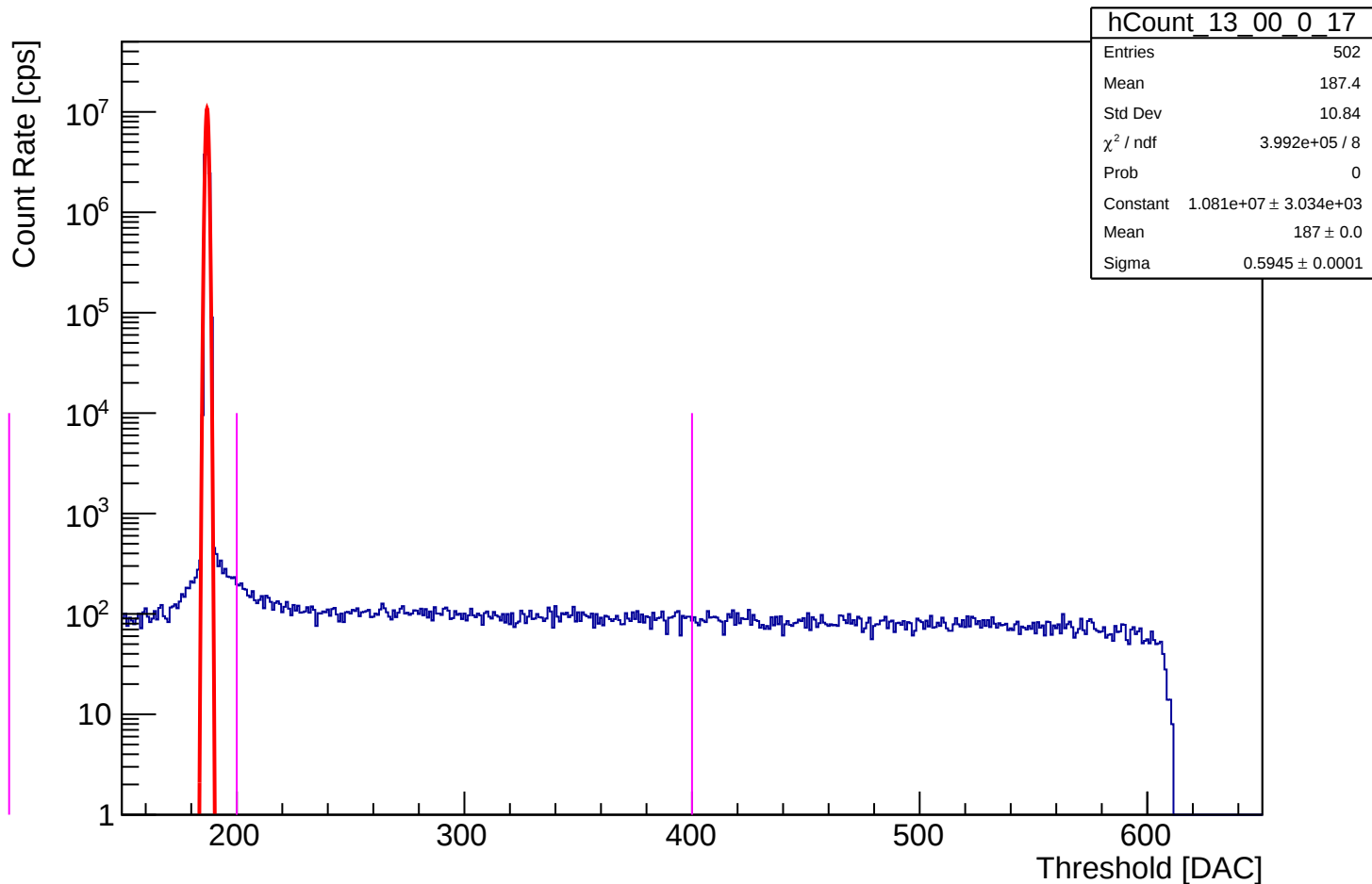
Row 1 Tile 1 Pmt 1 Pixel 24 Slot 13 Fiber 0 Asic 0 Channel 43



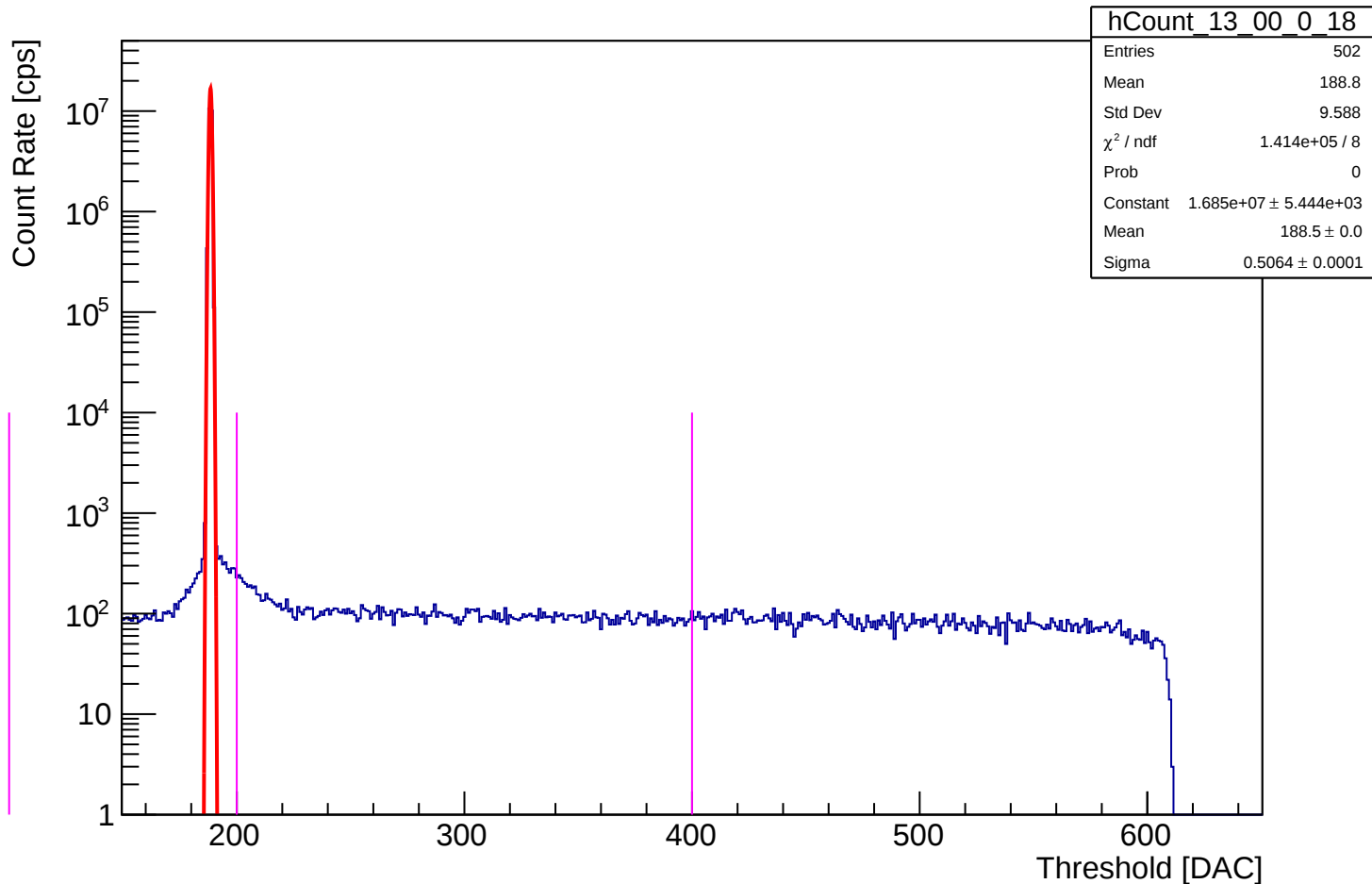
Row 1 Tile 1 Pmt 1 Pixel 25 Slot 13 Fiber 0 Asic 0 Channel 19



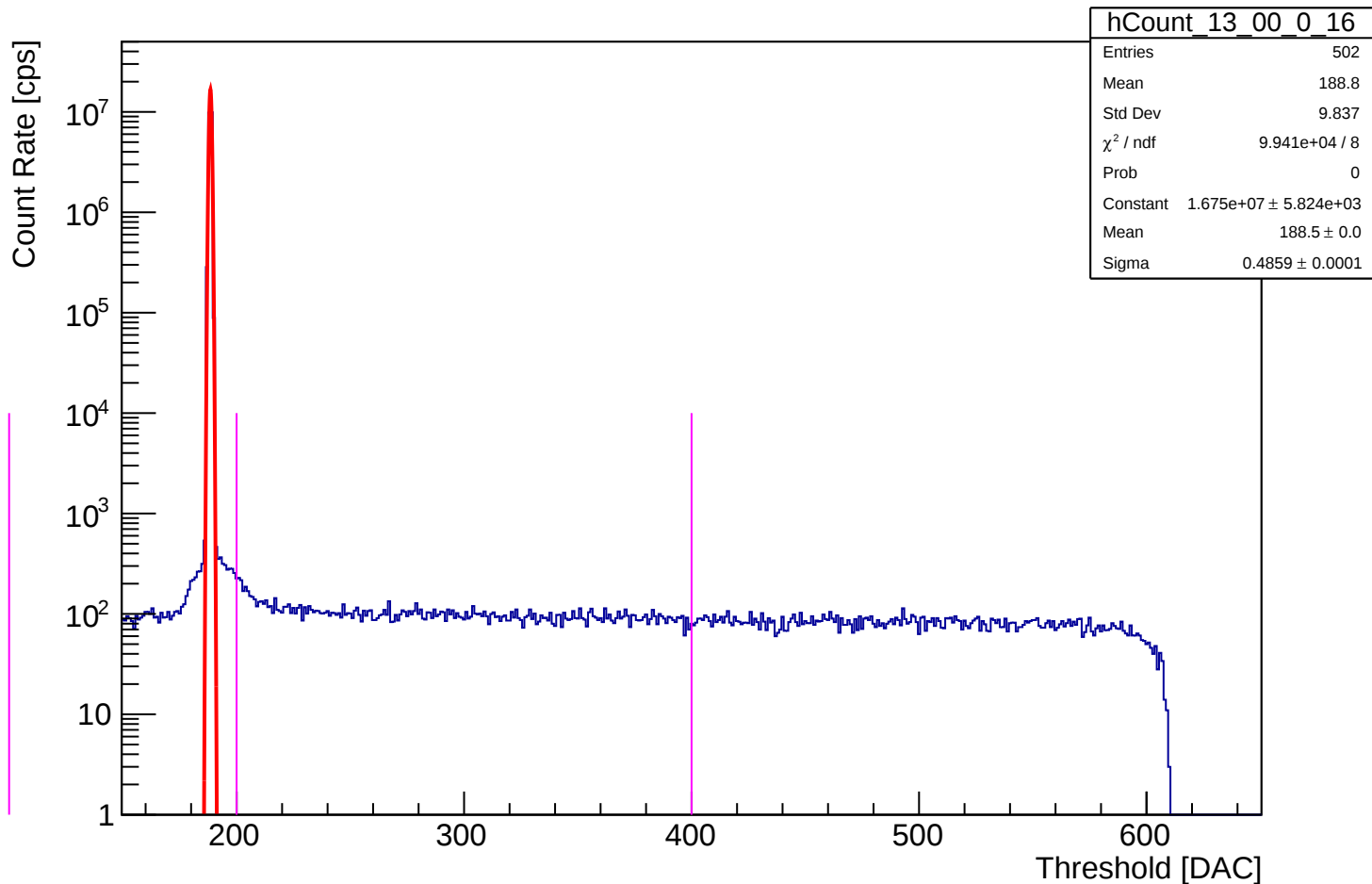
Row 1 Tile 1 Pmt 1 Pixel 26 Slot 13 Fiber 0 Asic 0 Channel 17



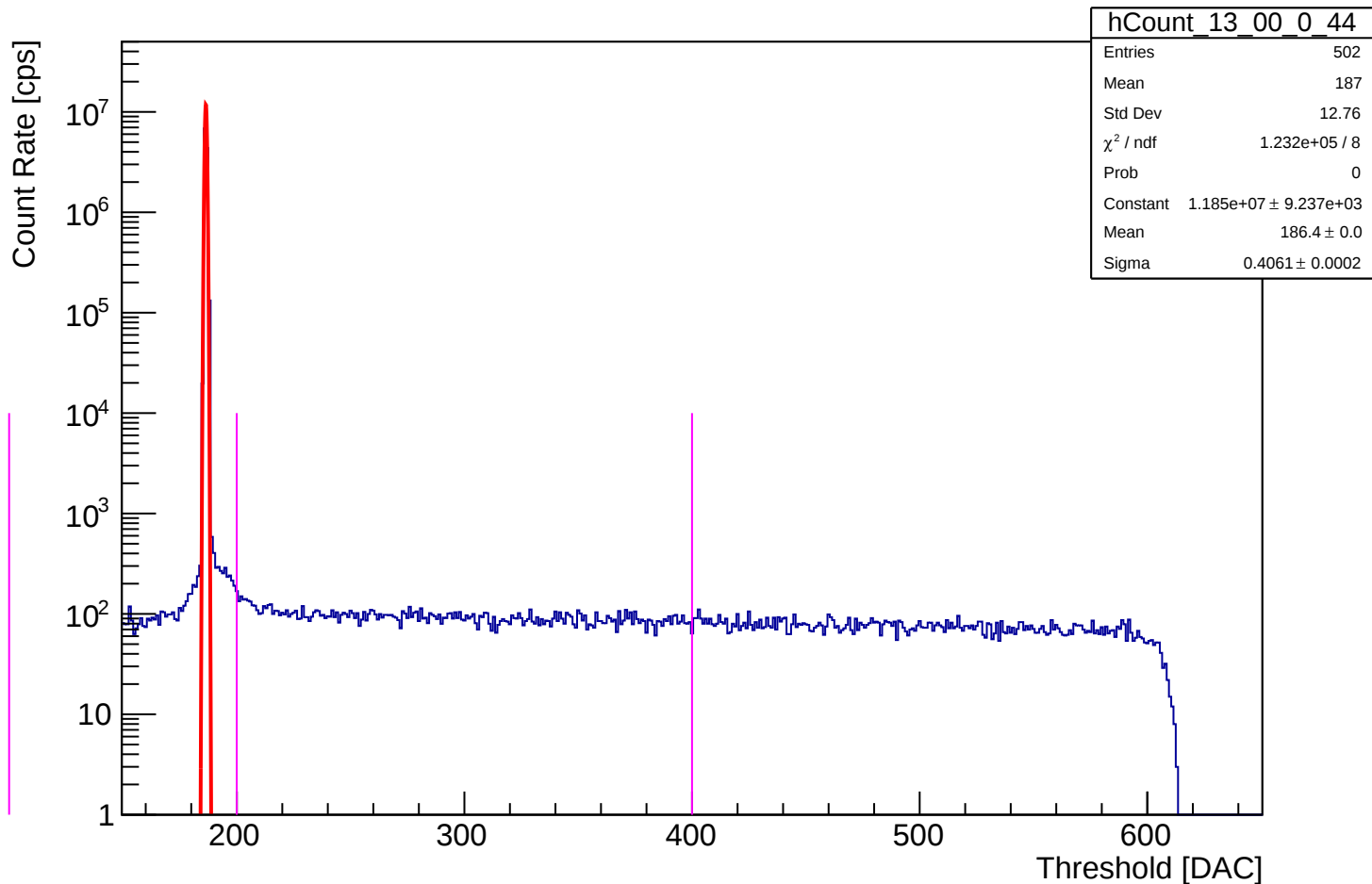
Row 1 Tile 1 Pmt 1 Pixel 27 Slot 13 Fiber 0 Asic 0 Channel 18



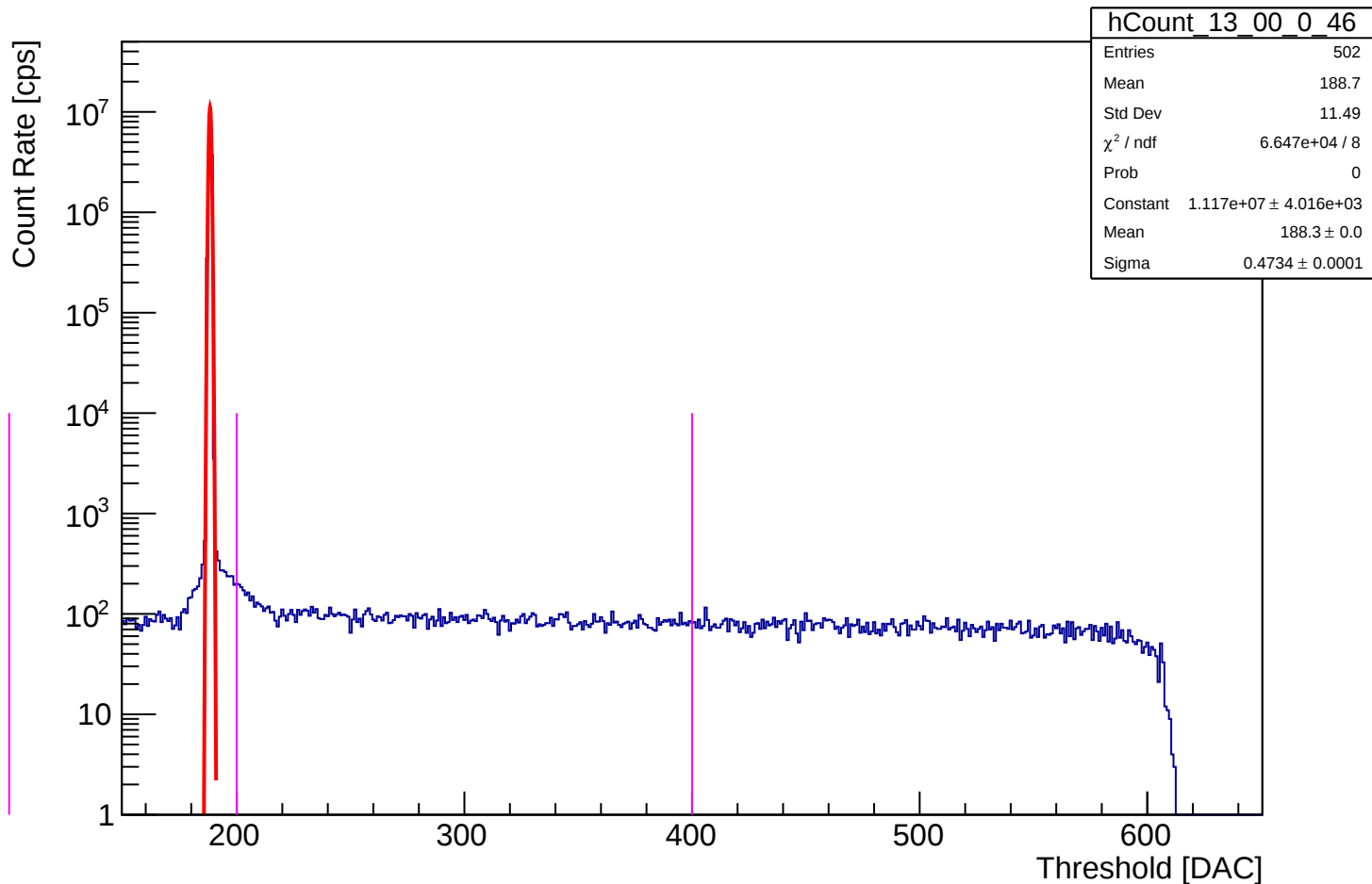
Row 1 Tile 1 Pmt 1 Pixel 28 Slot 13 Fiber 0 Asic 0 Channel 16



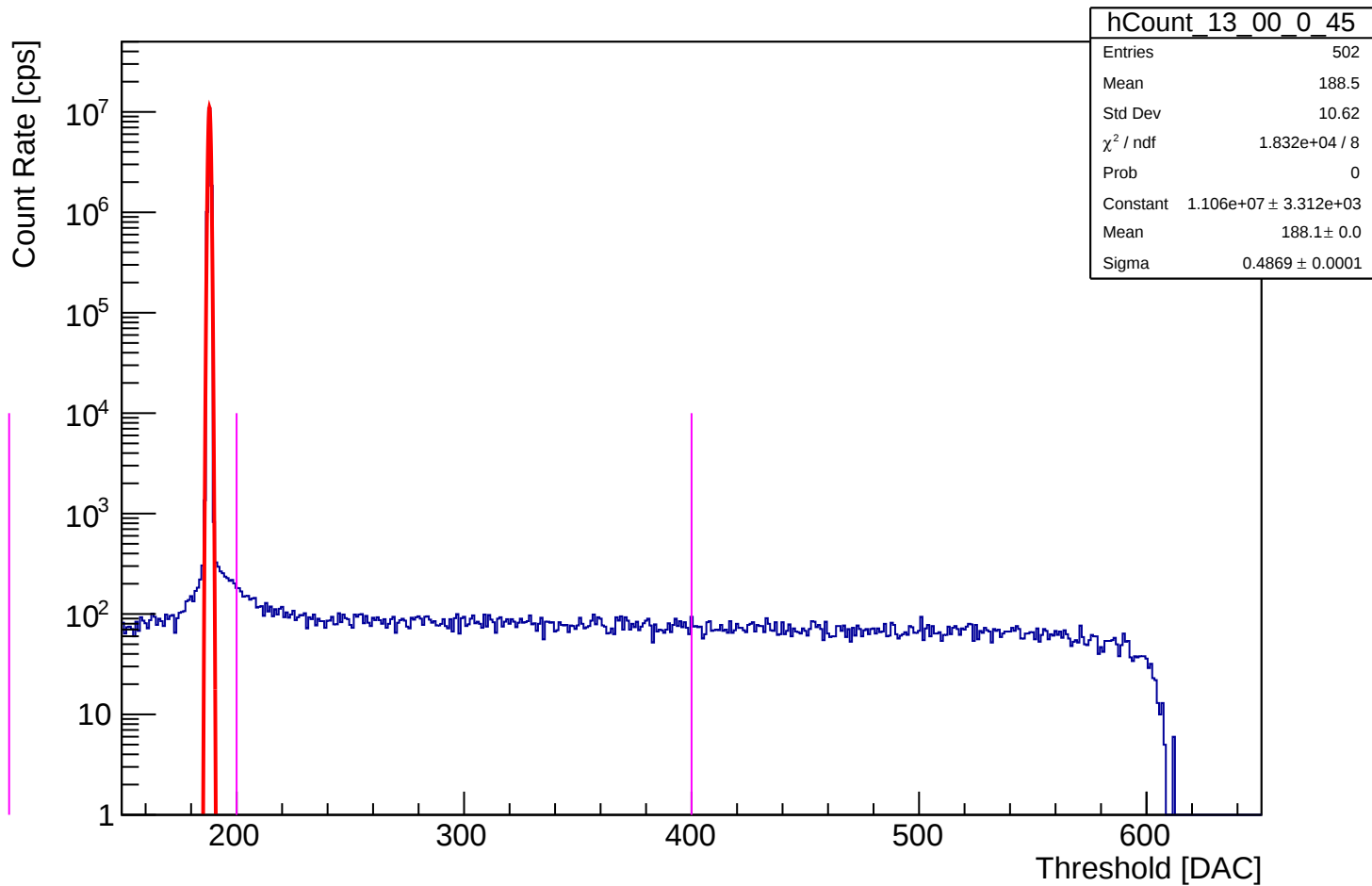
Row 1 Tile 1 Pmt 1 Pixel 29 Slot 13 Fiber 0 Asic 0 Channel 44



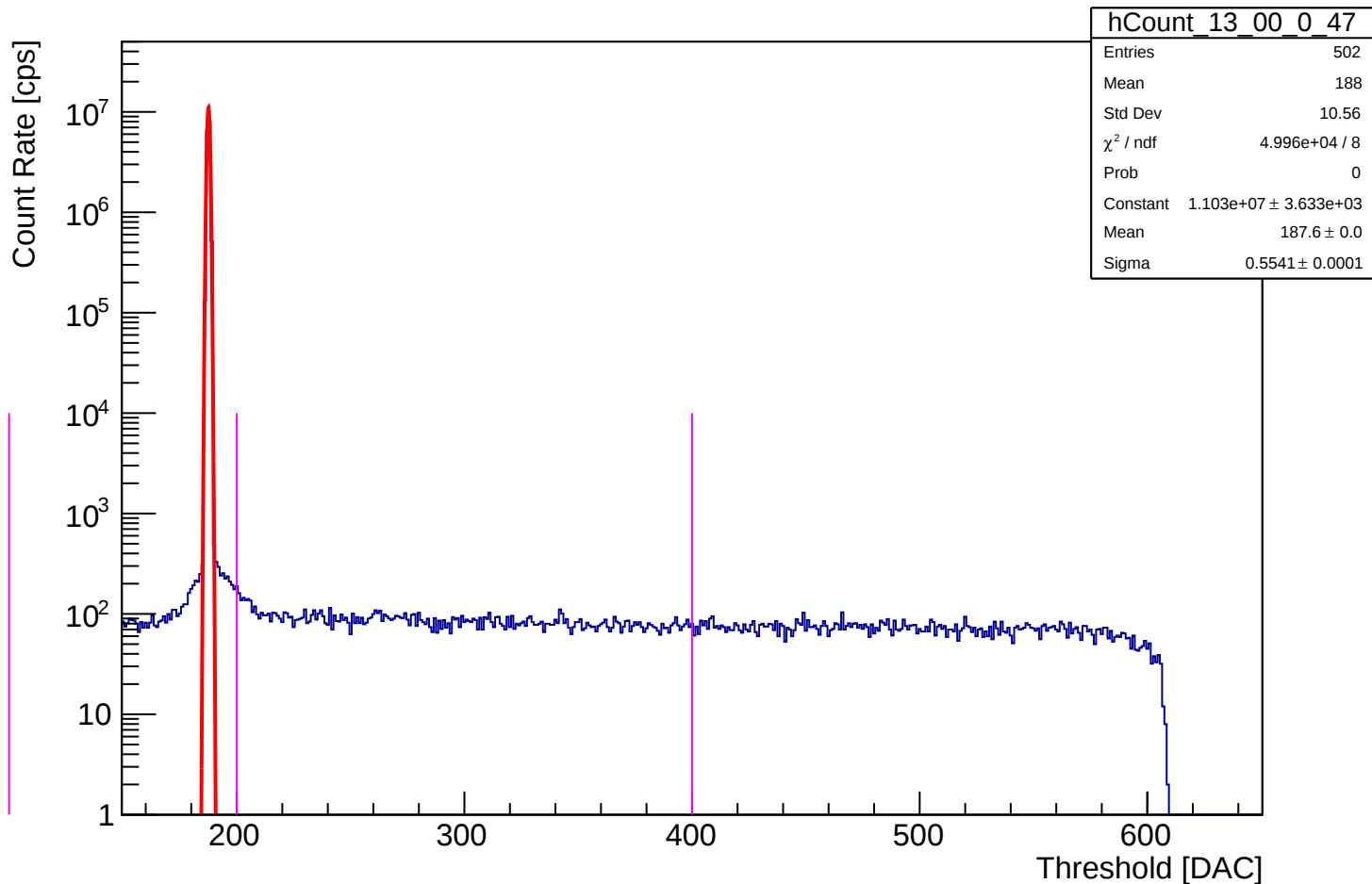
Row 1 Tile 1 Pmt 1 Pixel 30 Slot 13 Fiber 0 Asic 0 Channel 46



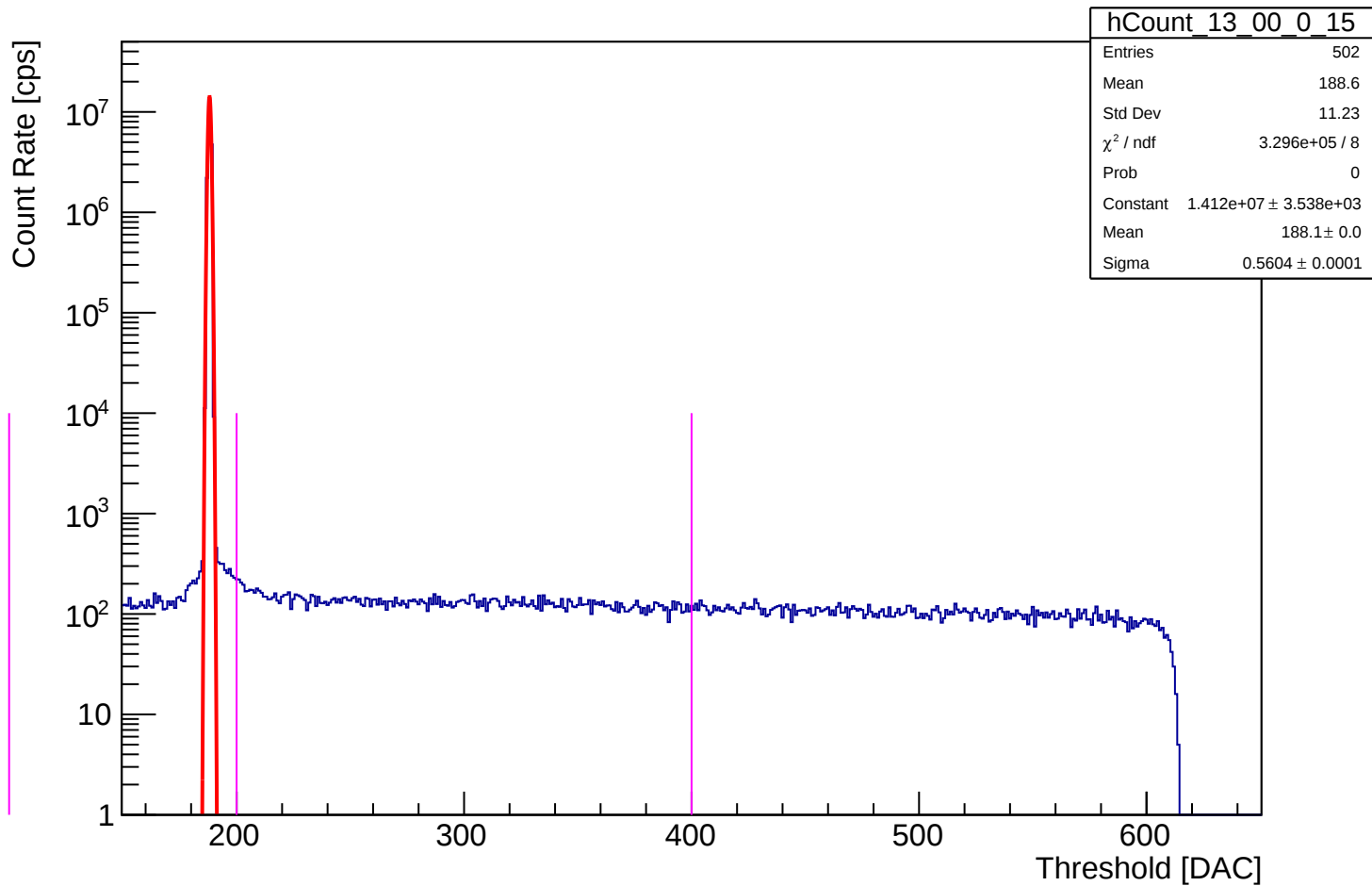
Row 1 Tile 1 Pmt 1 Pixel 31 Slot 13 Fiber 0 Asic 0 Channel 45



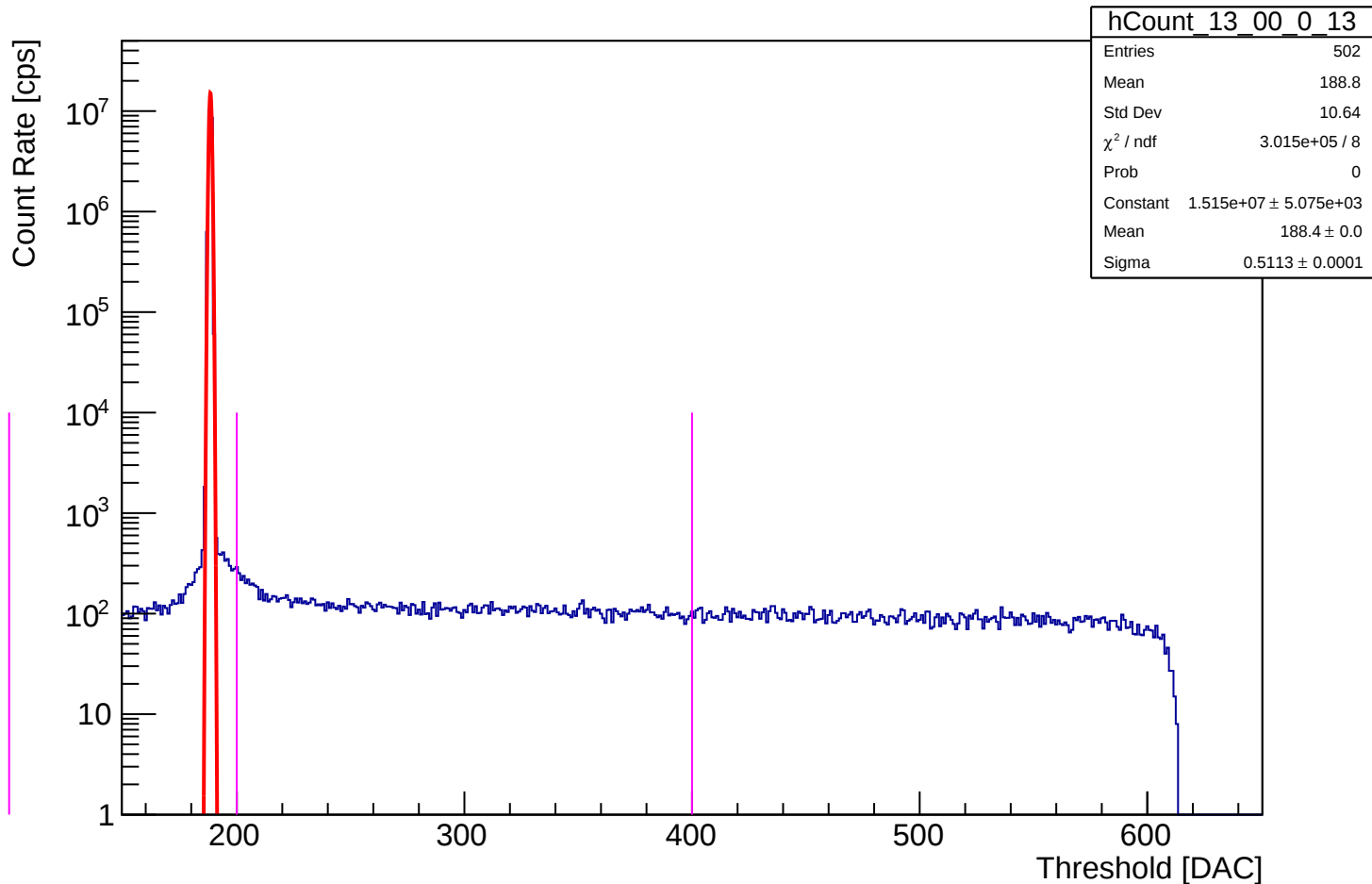
Row 1 Tile 1 Pmt 1 Pixel 32 Slot 13 Fiber 0 Asic 0 Channel 47



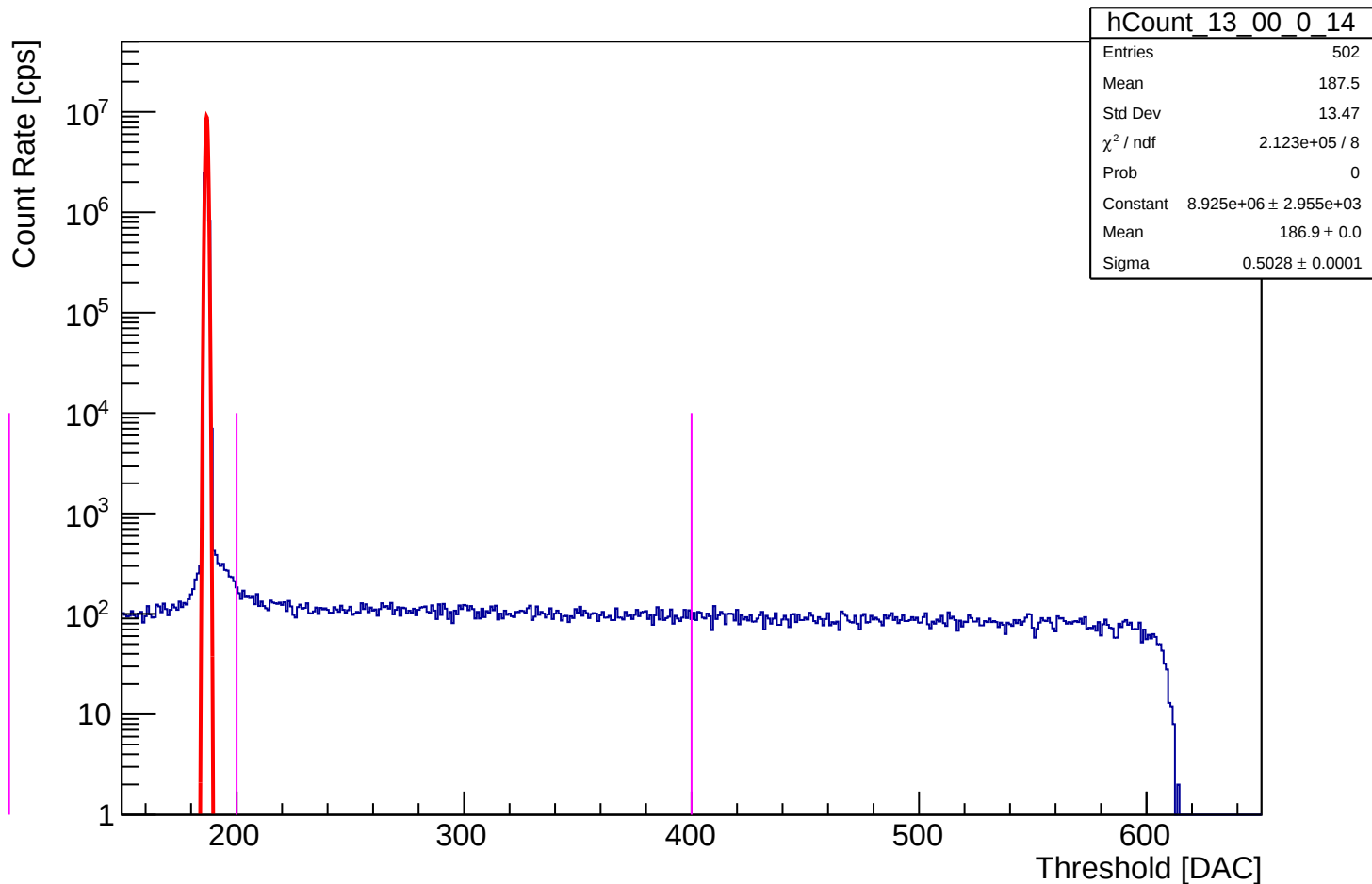
Row 1 Tile 1 Pmt 1 Pixel 33 Slot 13 Fiber 0 Asic 0 Channel 15



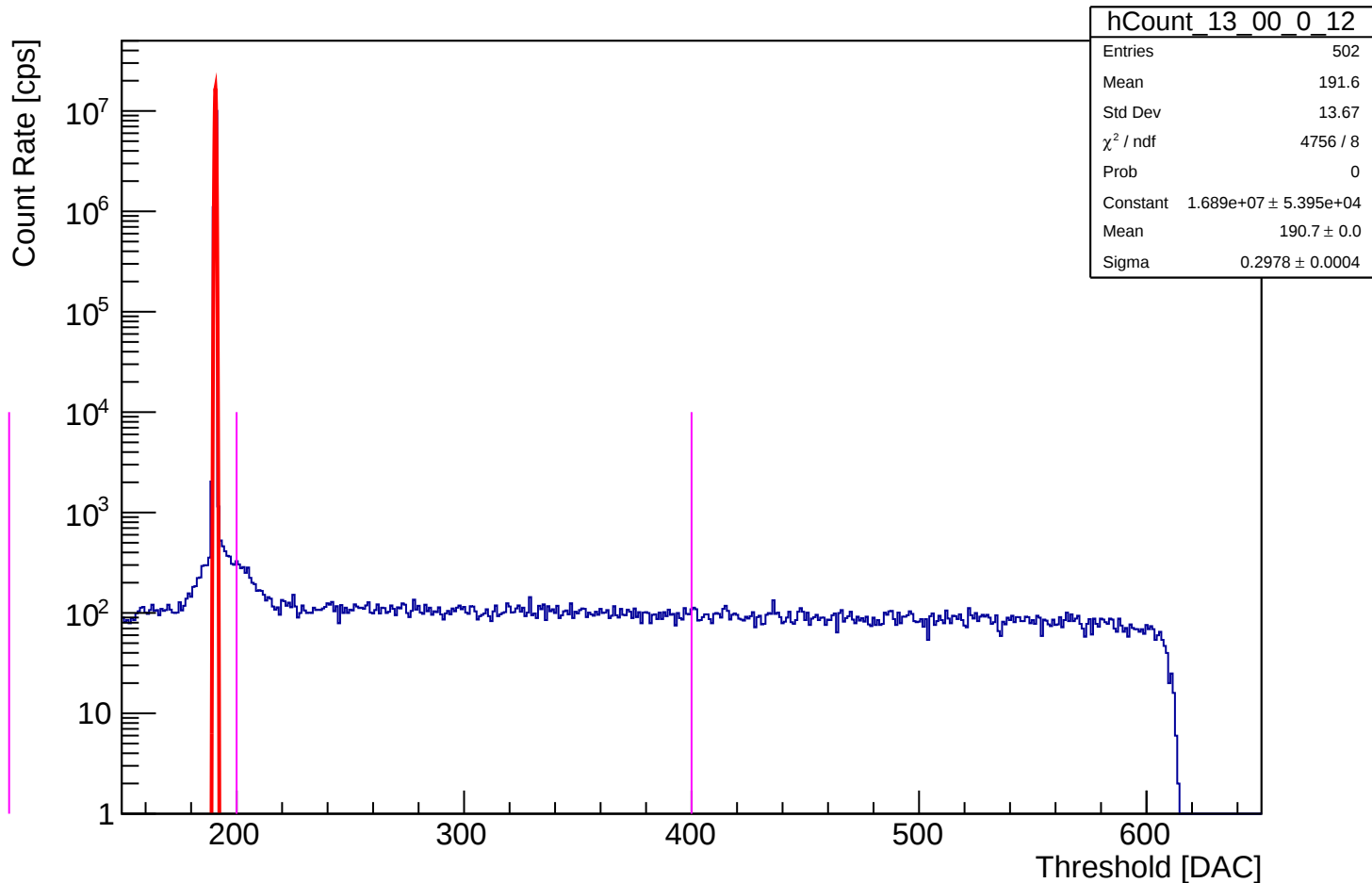
Row 1 Tile 1 Pmt 1 Pixel 34 Slot 13 Fiber 0 Asic 0 Channel 13



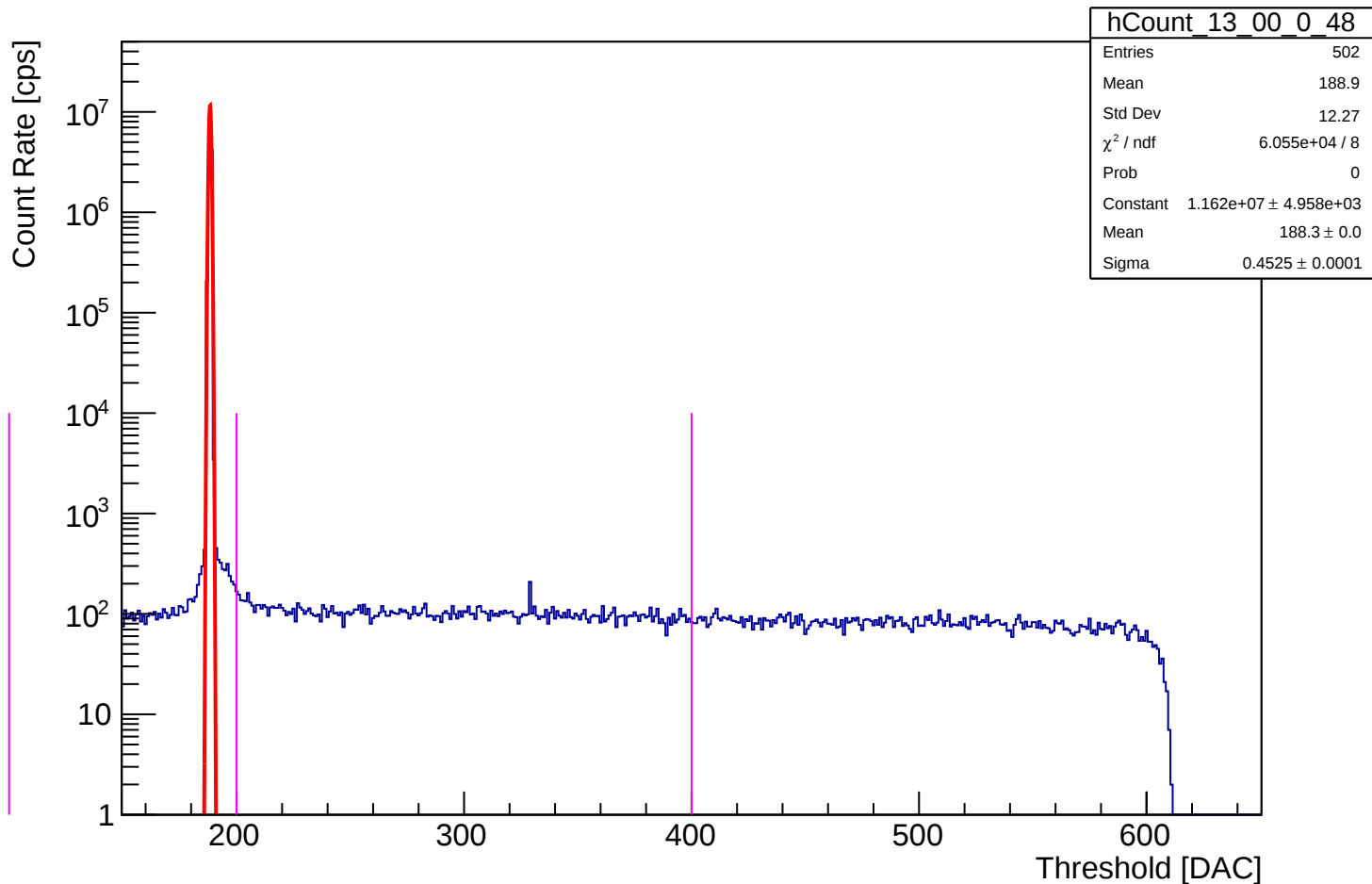
Row 1 Tile 1 Pmt 1 Pixel 35 Slot 13 Fiber 0 Asic 0 Channel 14



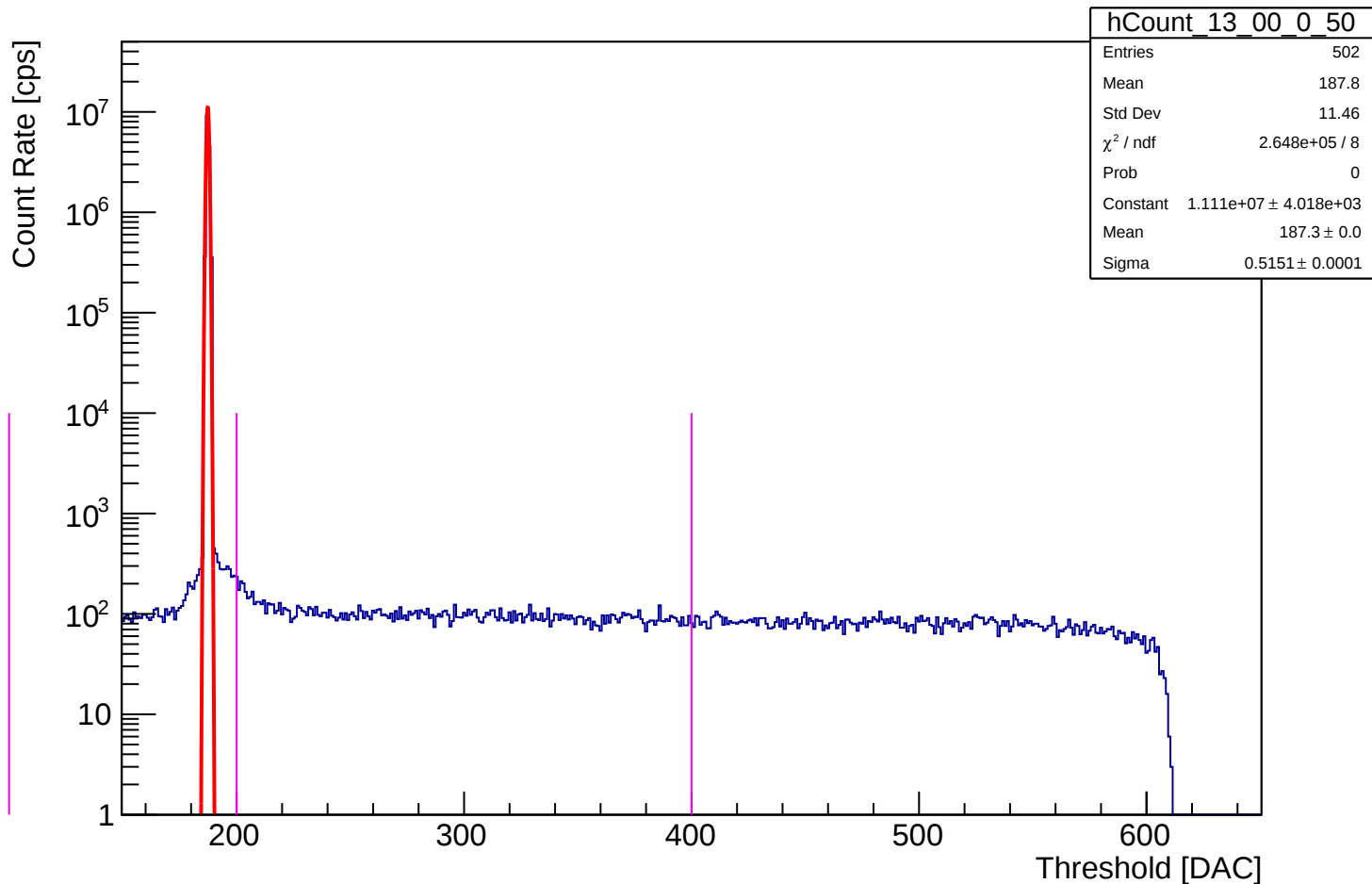
Row 1 Tile 1 Pmt 1 Pixel 36 Slot 13 Fiber 0 Asic 0 Channel 12



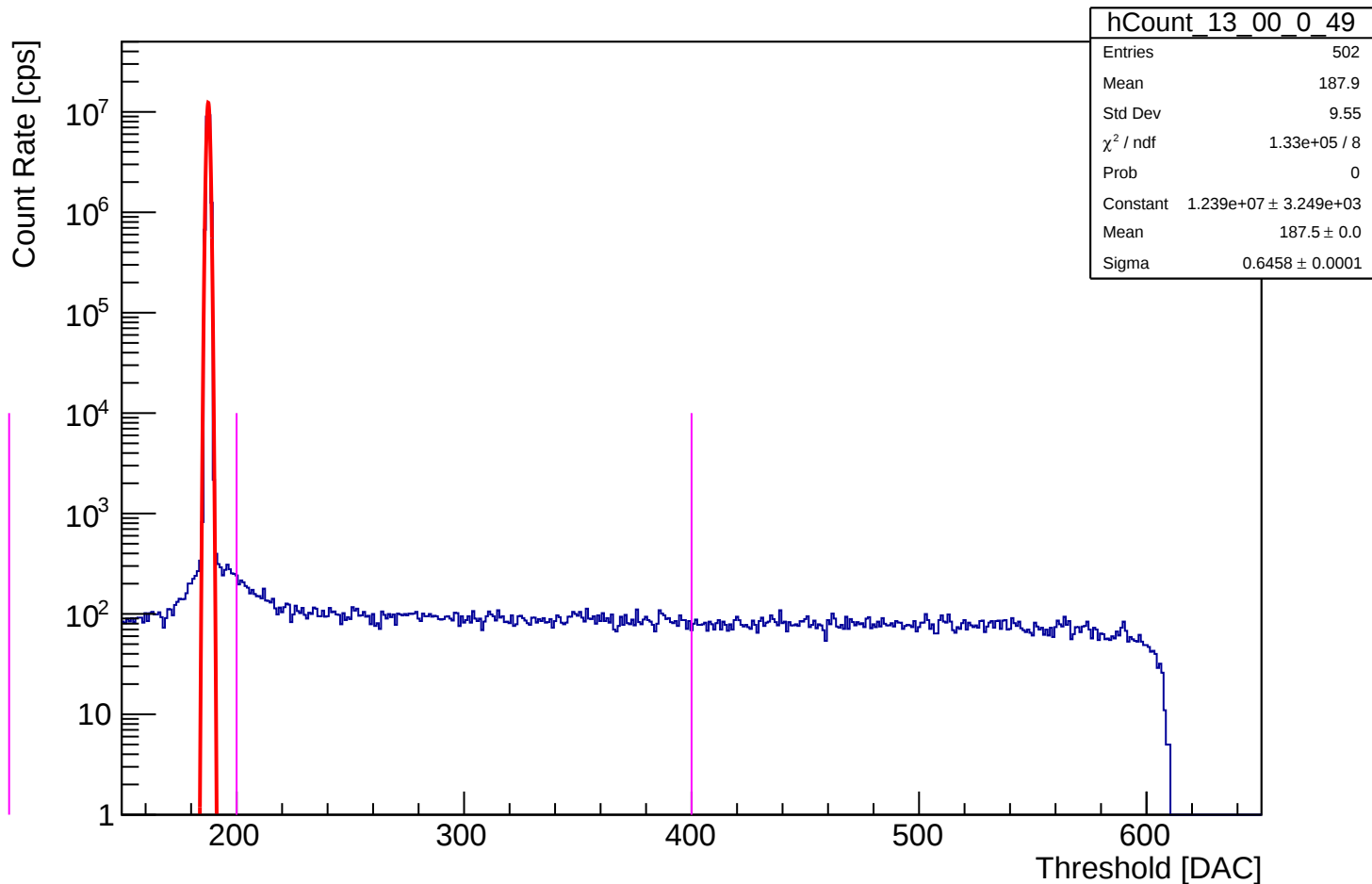
Row 1 Tile 1 Pmt 1 Pixel 37 Slot 13 Fiber 0 Asic 0 Channel 48

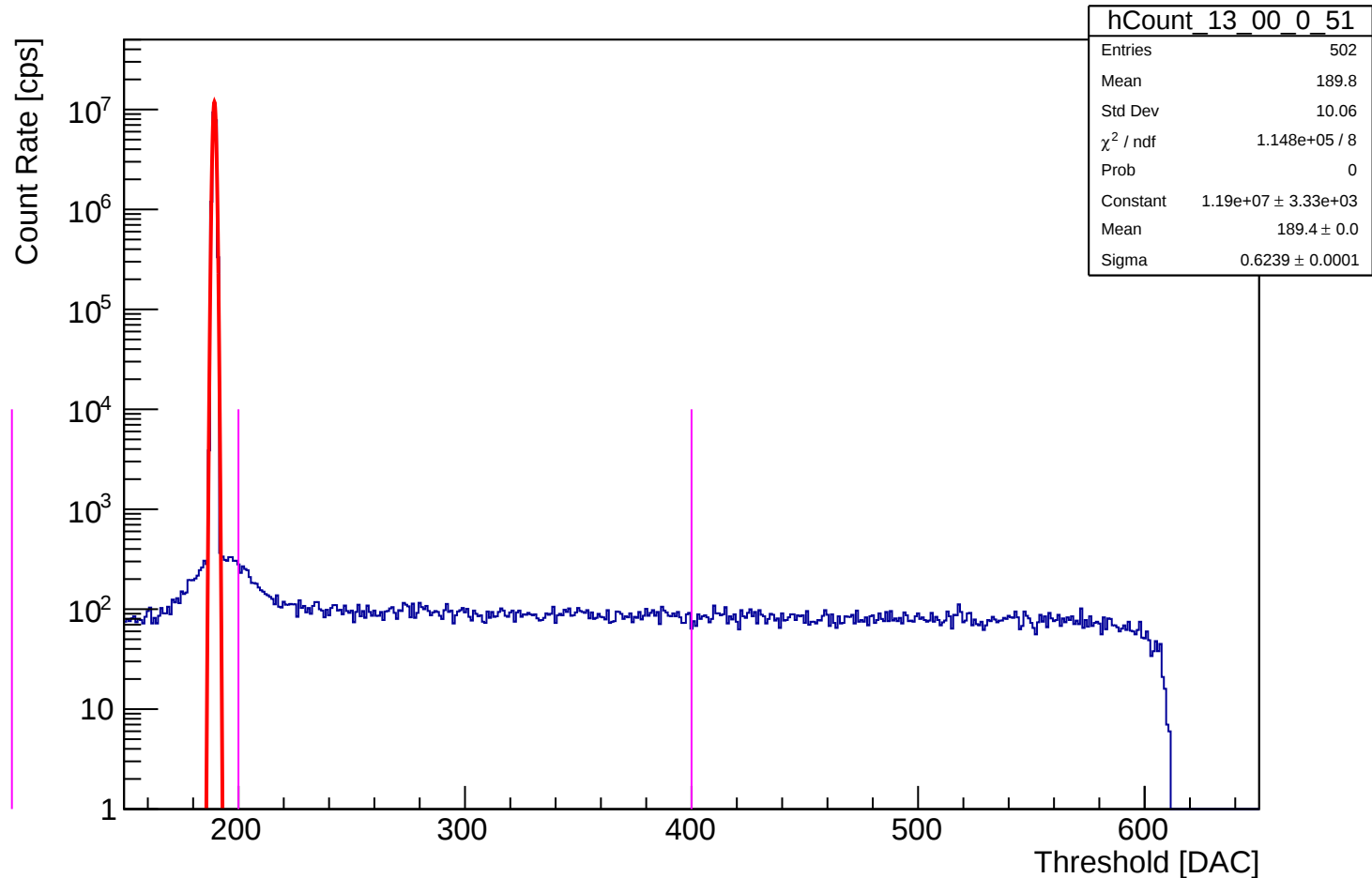


Row 1 Tile 1 Pmt 1 Pixel 38 Slot 13 Fiber 0 Asic 0 Channel 50

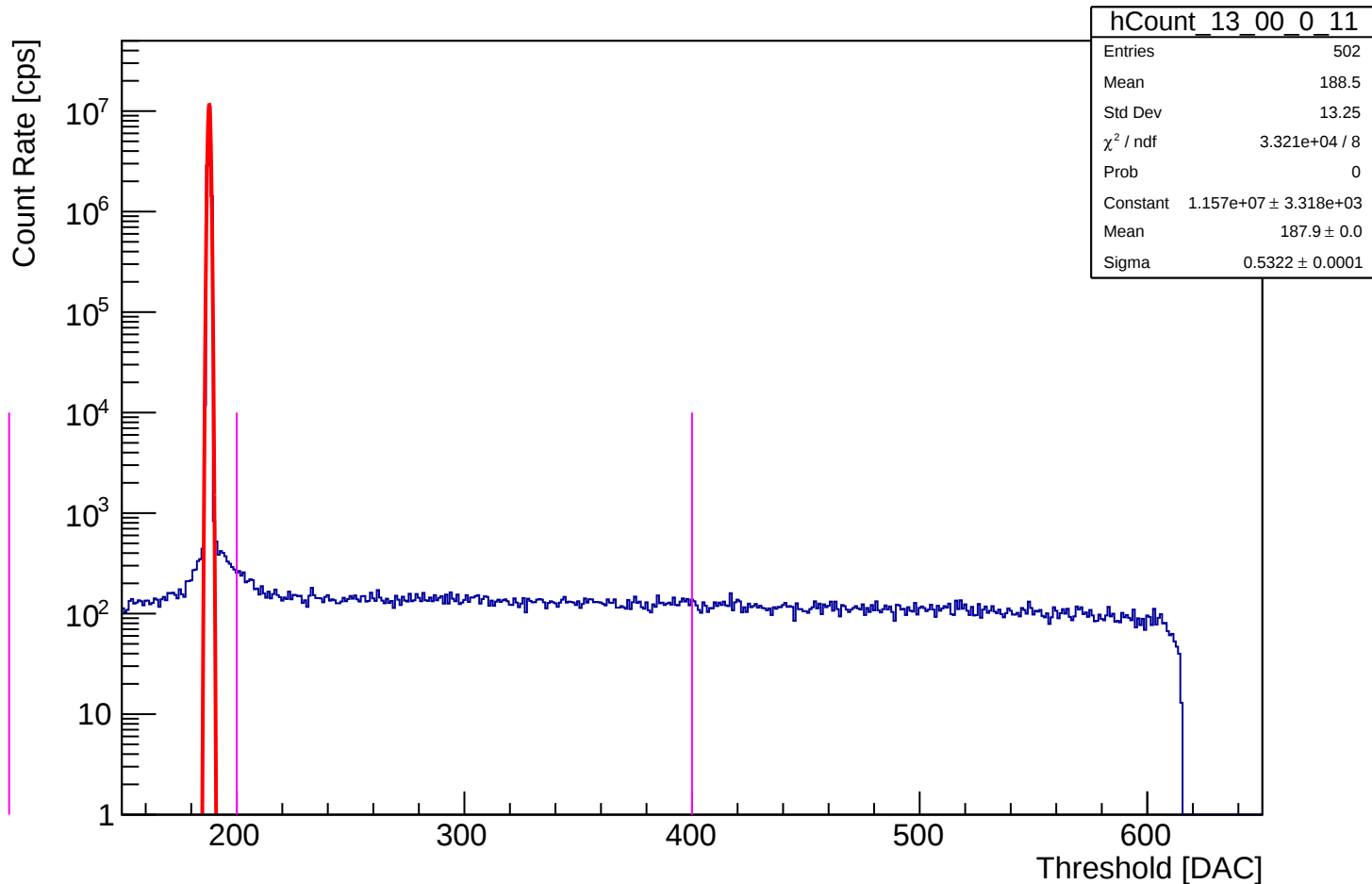


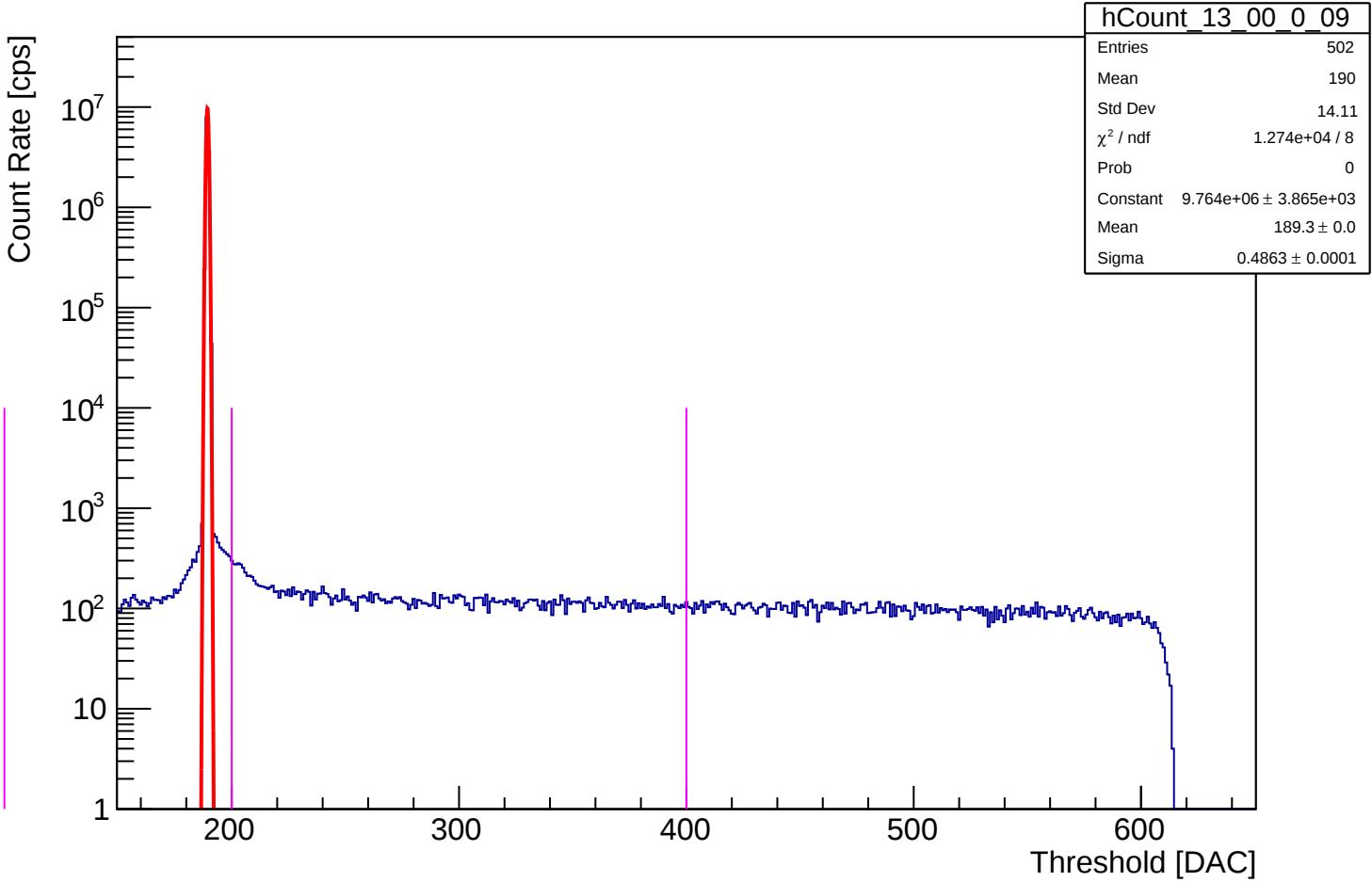
Row 1 Tile 1 Pmt 1 Pixel 39 Slot 13 Fiber 0 Asic 0 Channel 49



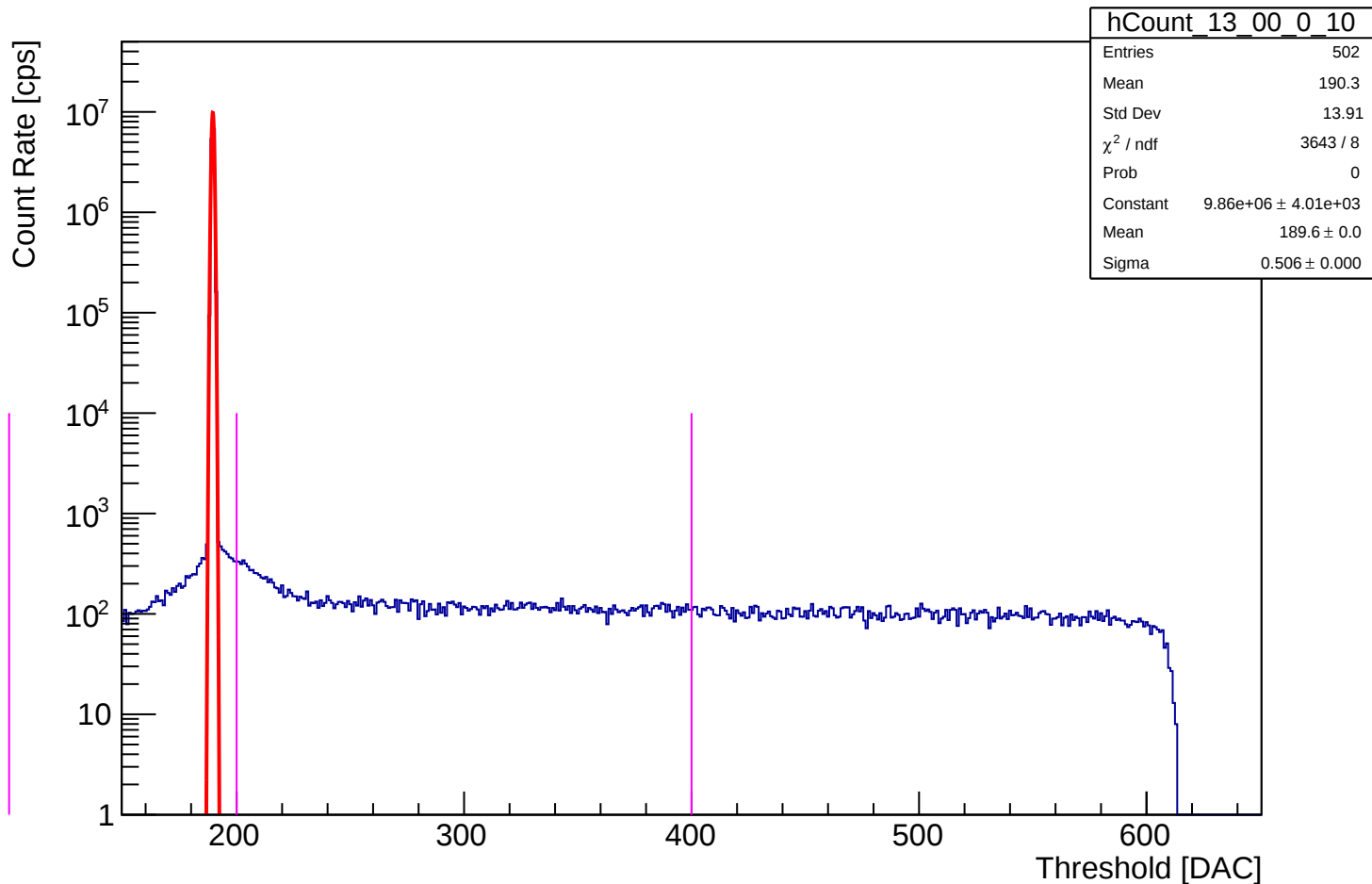


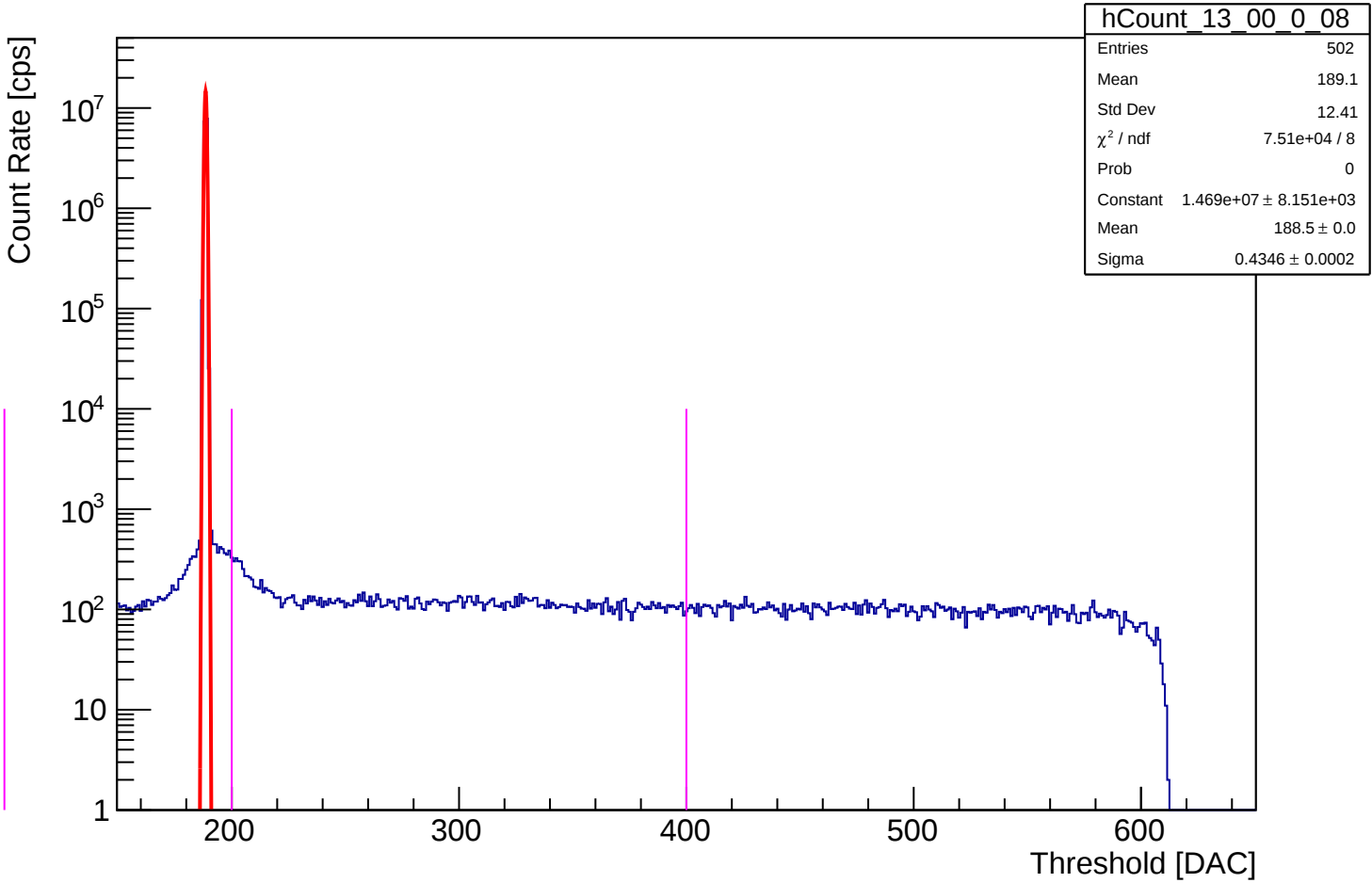
Row 1 Tile 1 Pmt 1 Pixel 41 Slot 13 Fiber 0 Asic 0 Channel 11



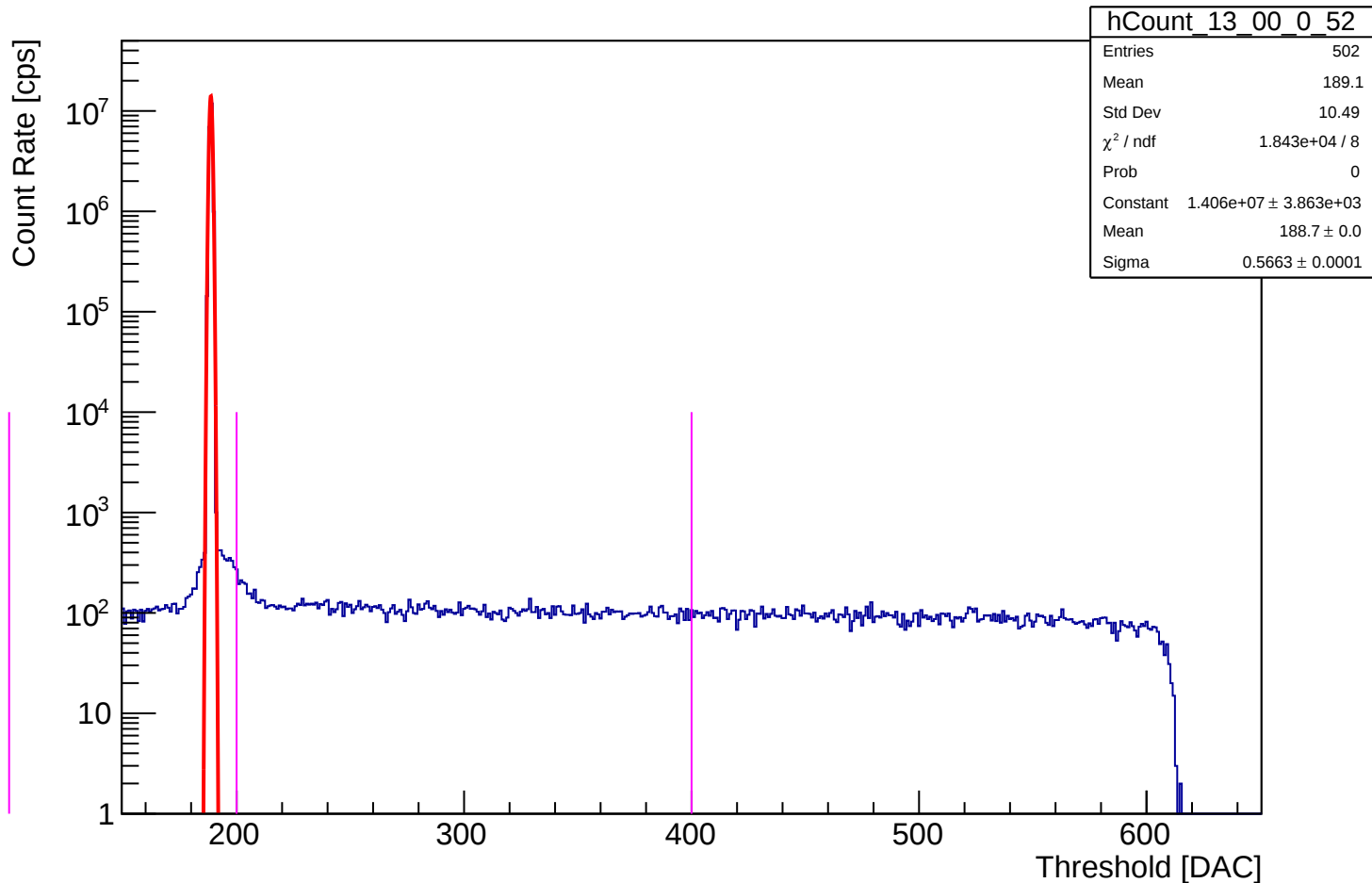


Row 1 Tile 1 Pmt 1 Pixel 43 Slot 13 Fiber 0 Asic 0 Channel 10

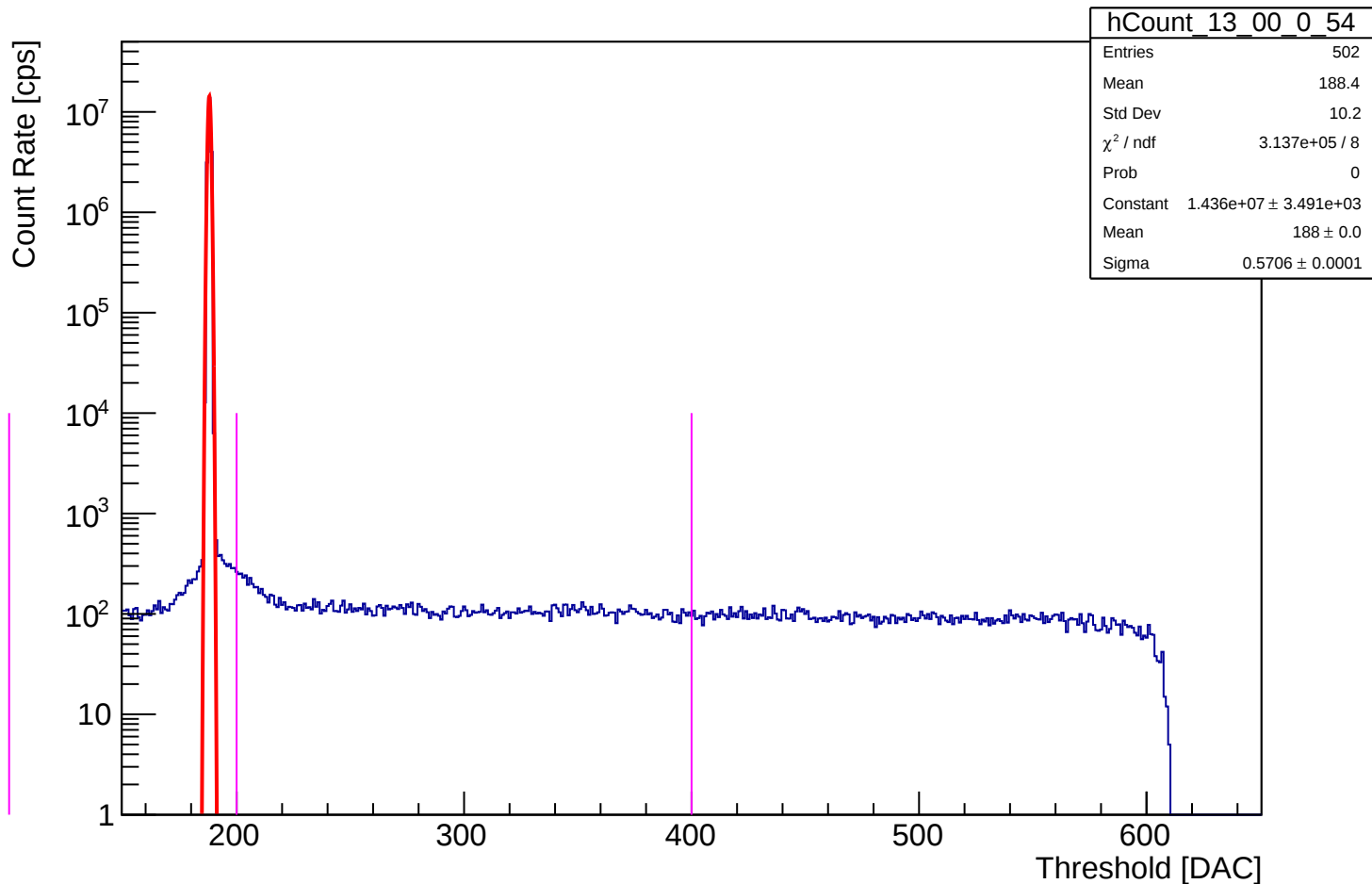




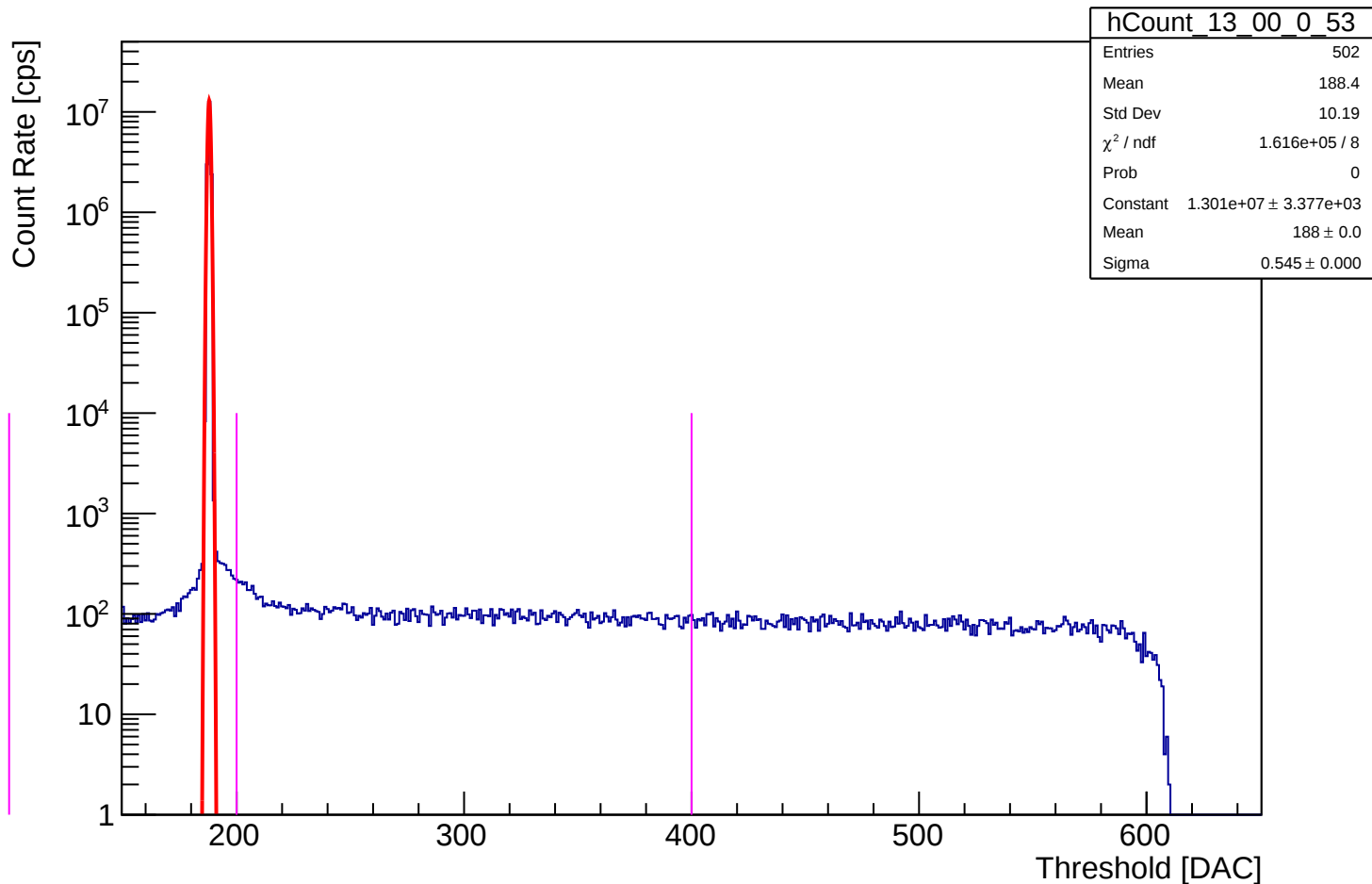
Row 1 Tile 1 Pmt 1 Pixel 45 Slot 13 Fiber 0 Asic 0 Channel 52



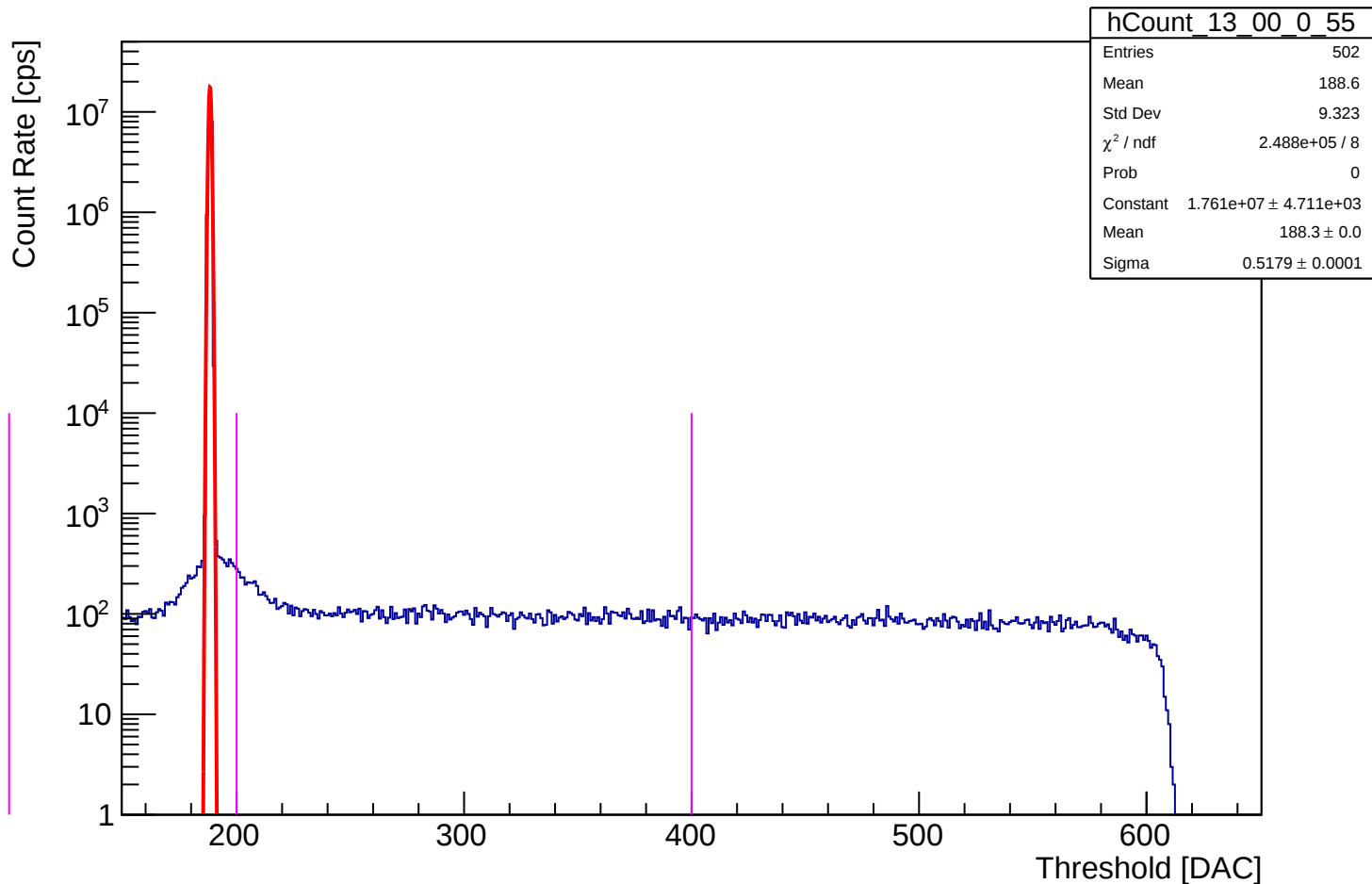
Row 1 Tile 1 Pmt 1 Pixel 46 Slot 13 Fiber 0 Asic 0 Channel 54

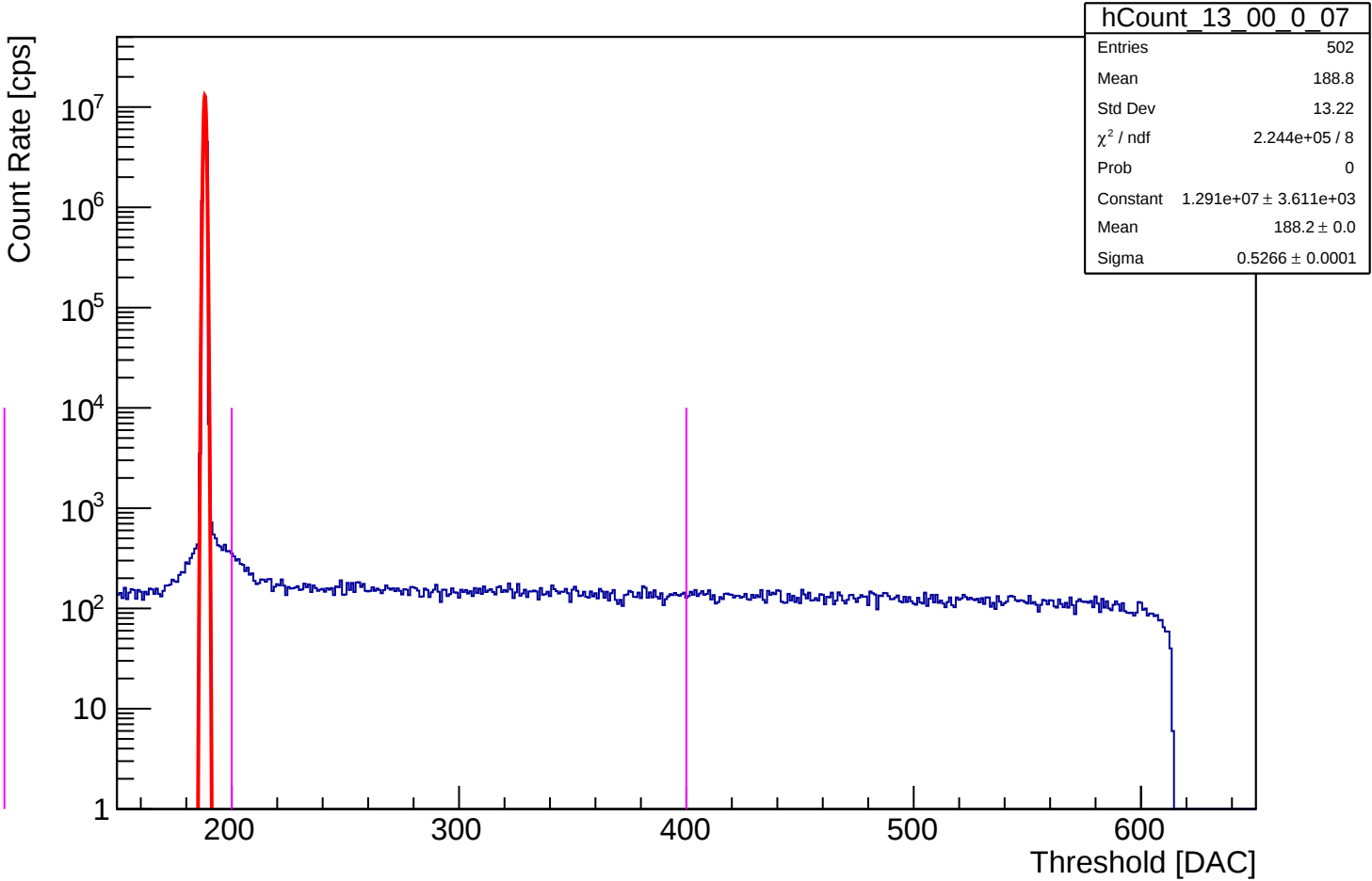


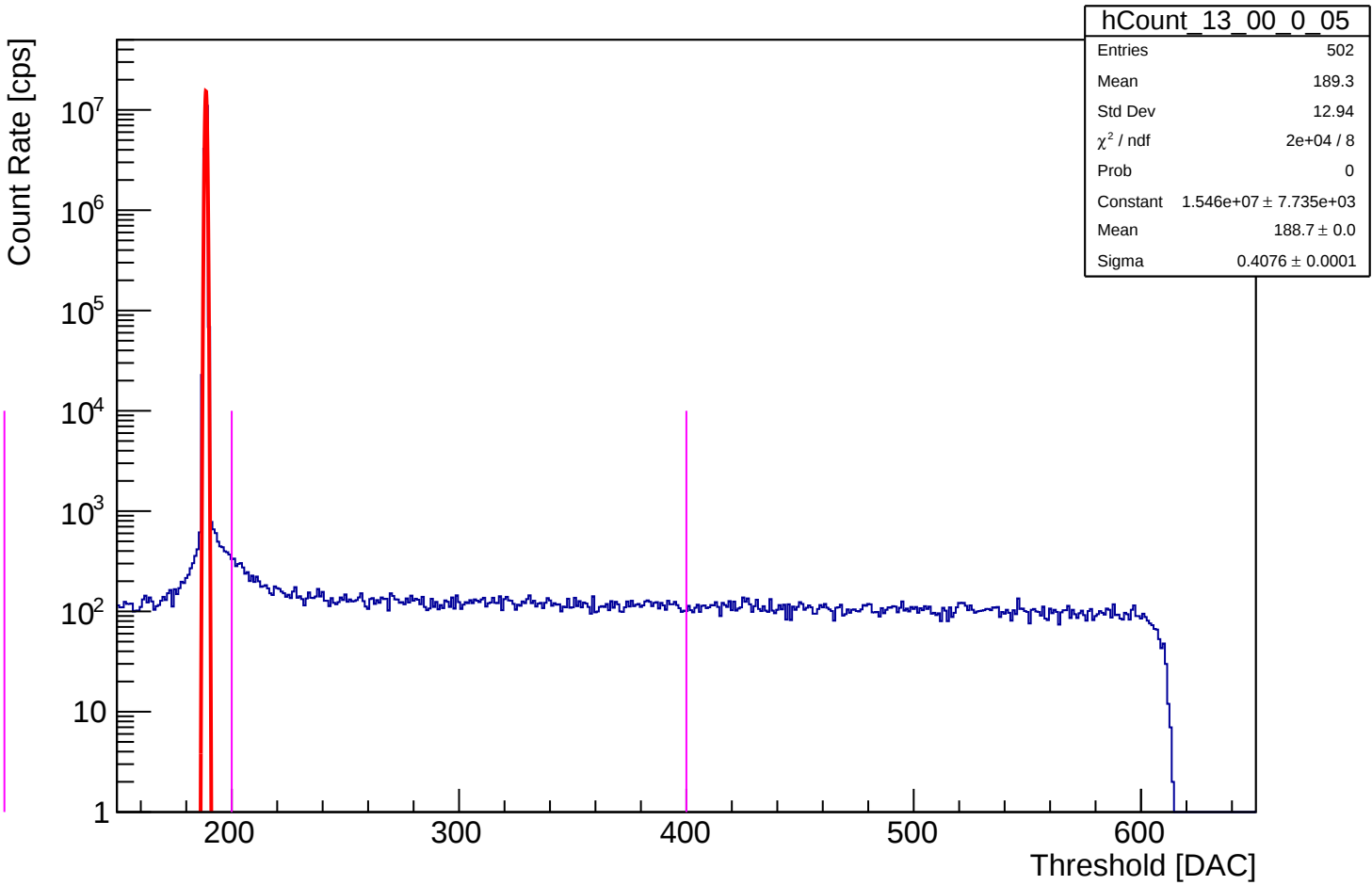
Row 1 Tile 1 Pmt 1 Pixel 47 Slot 13 Fiber 0 Asic 0 Channel 53

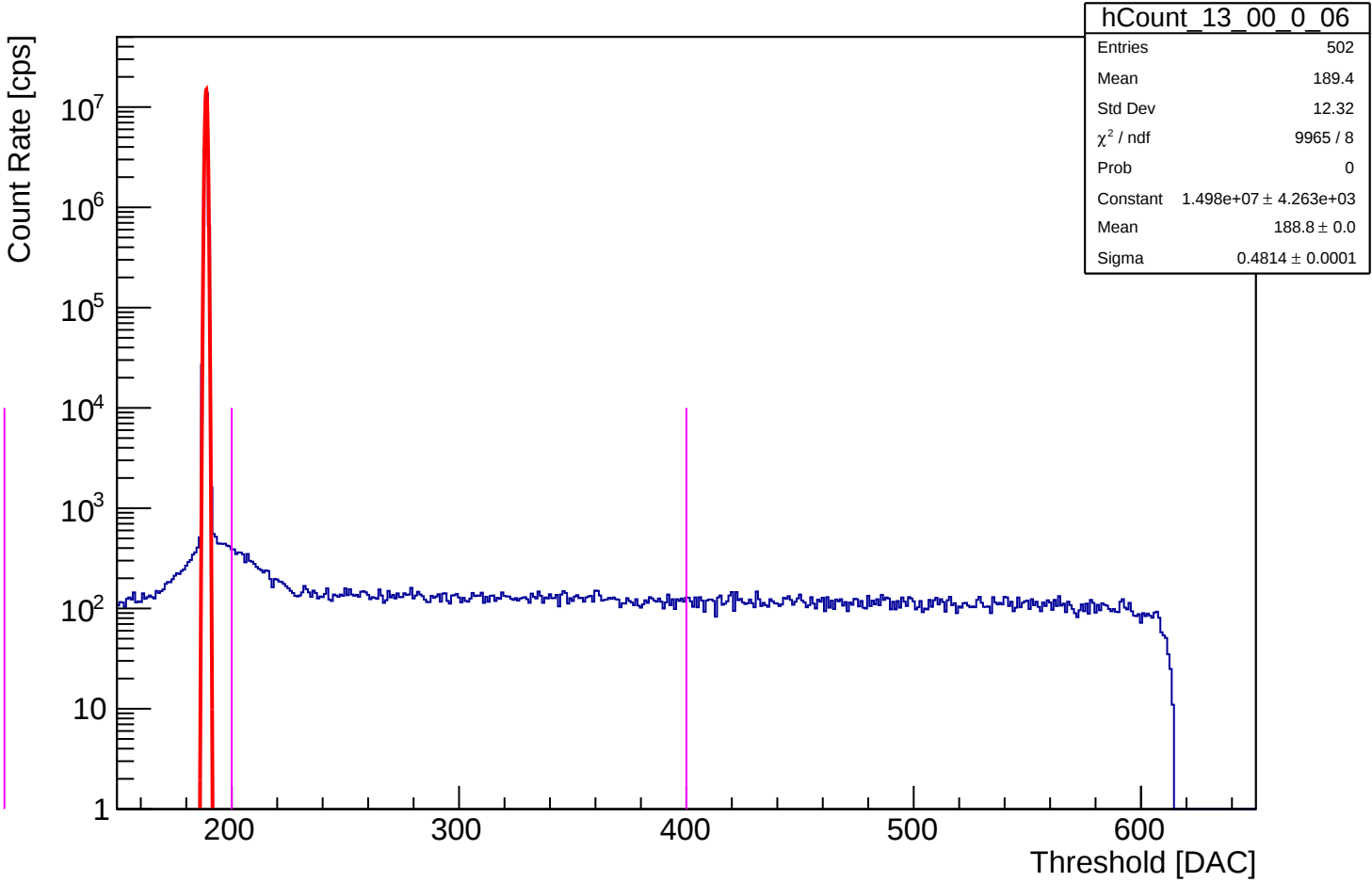


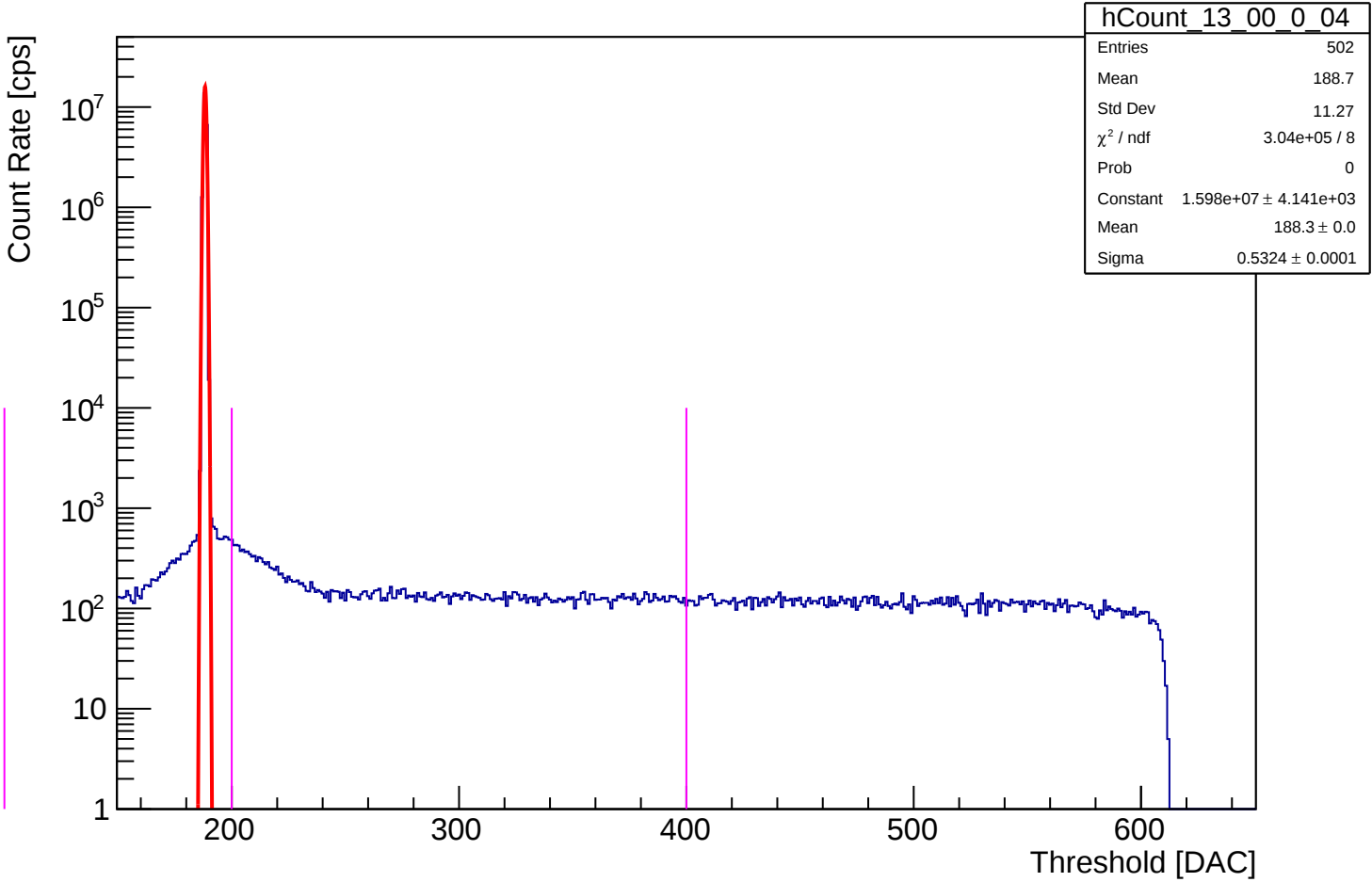
Row 1 Tile 1 Pmt 1 Pixel 48 Slot 13 Fiber 0 Asic 0 Channel 55



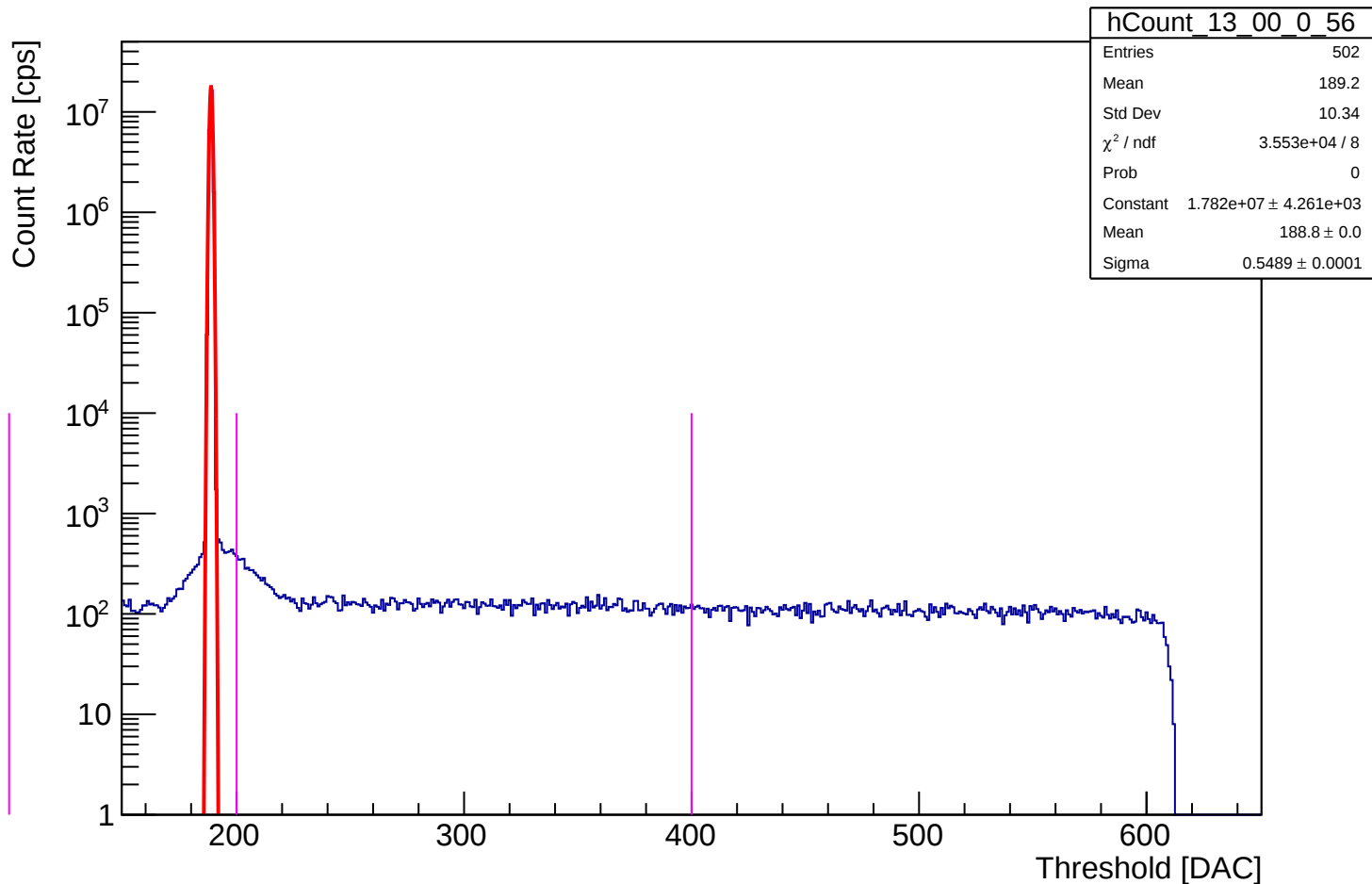




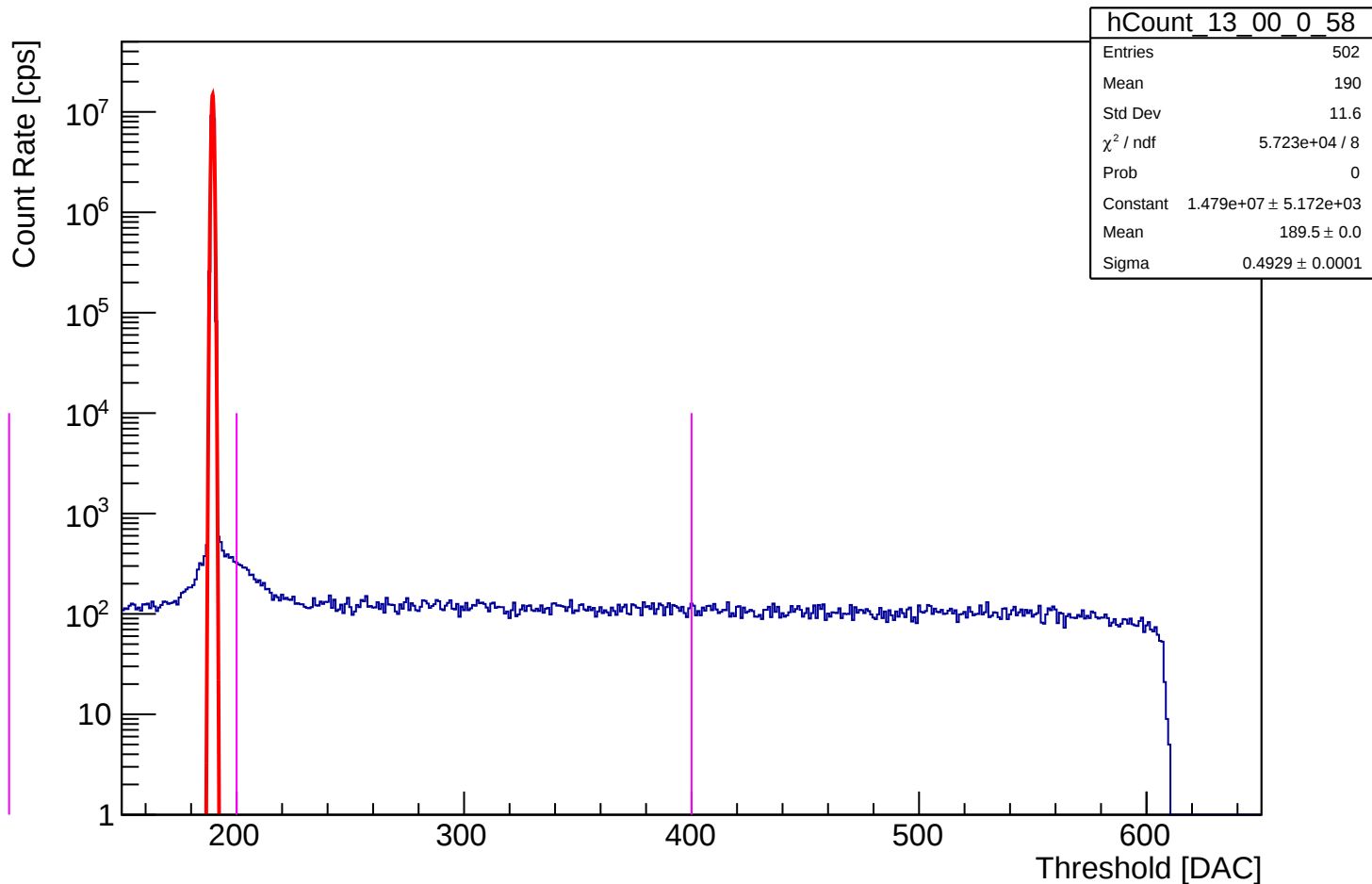




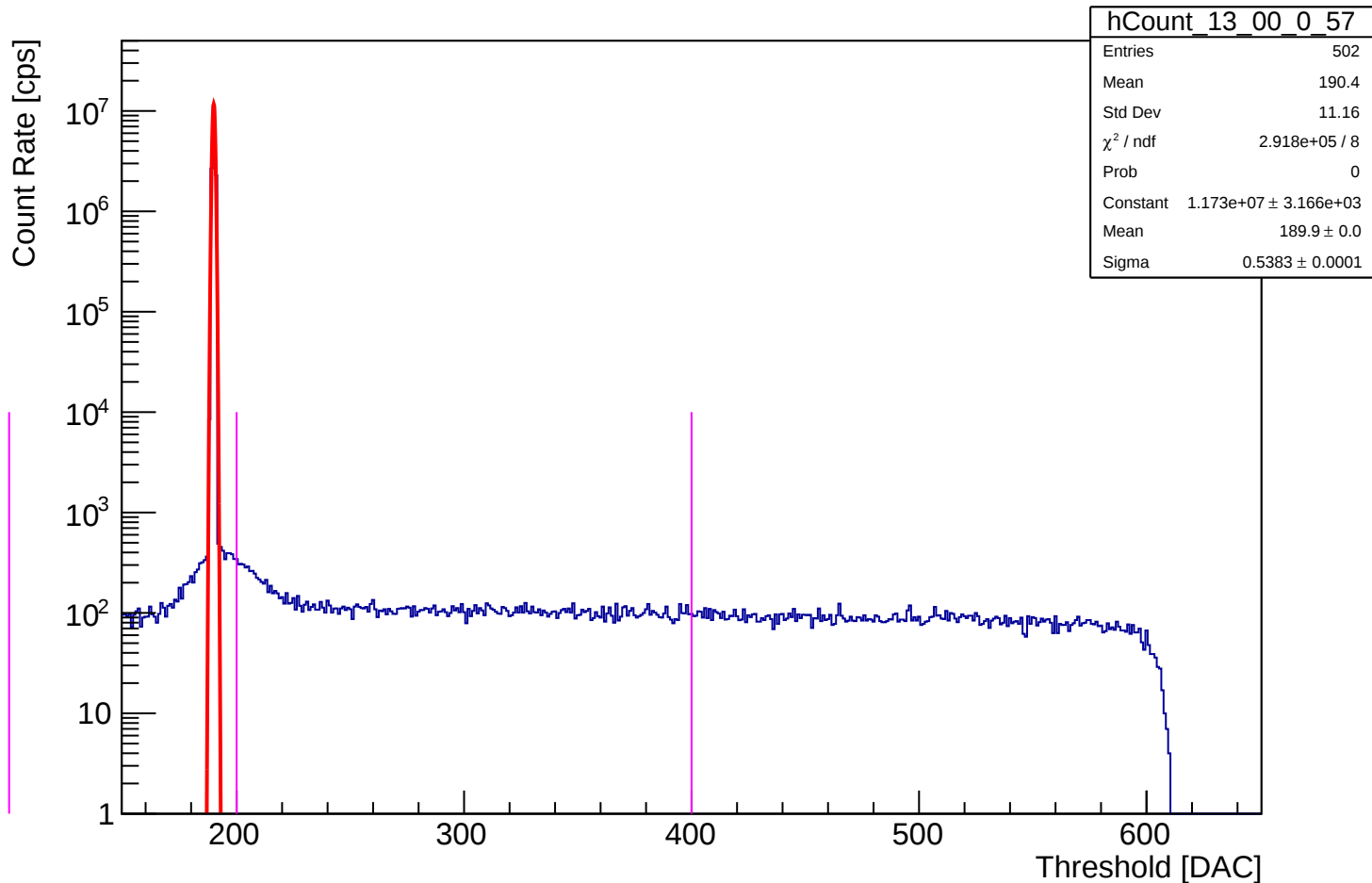
Row 1 Tile 1 Pmt 1 Pixel 53 Slot 13 Fiber 0 Asic 0 Channel 56



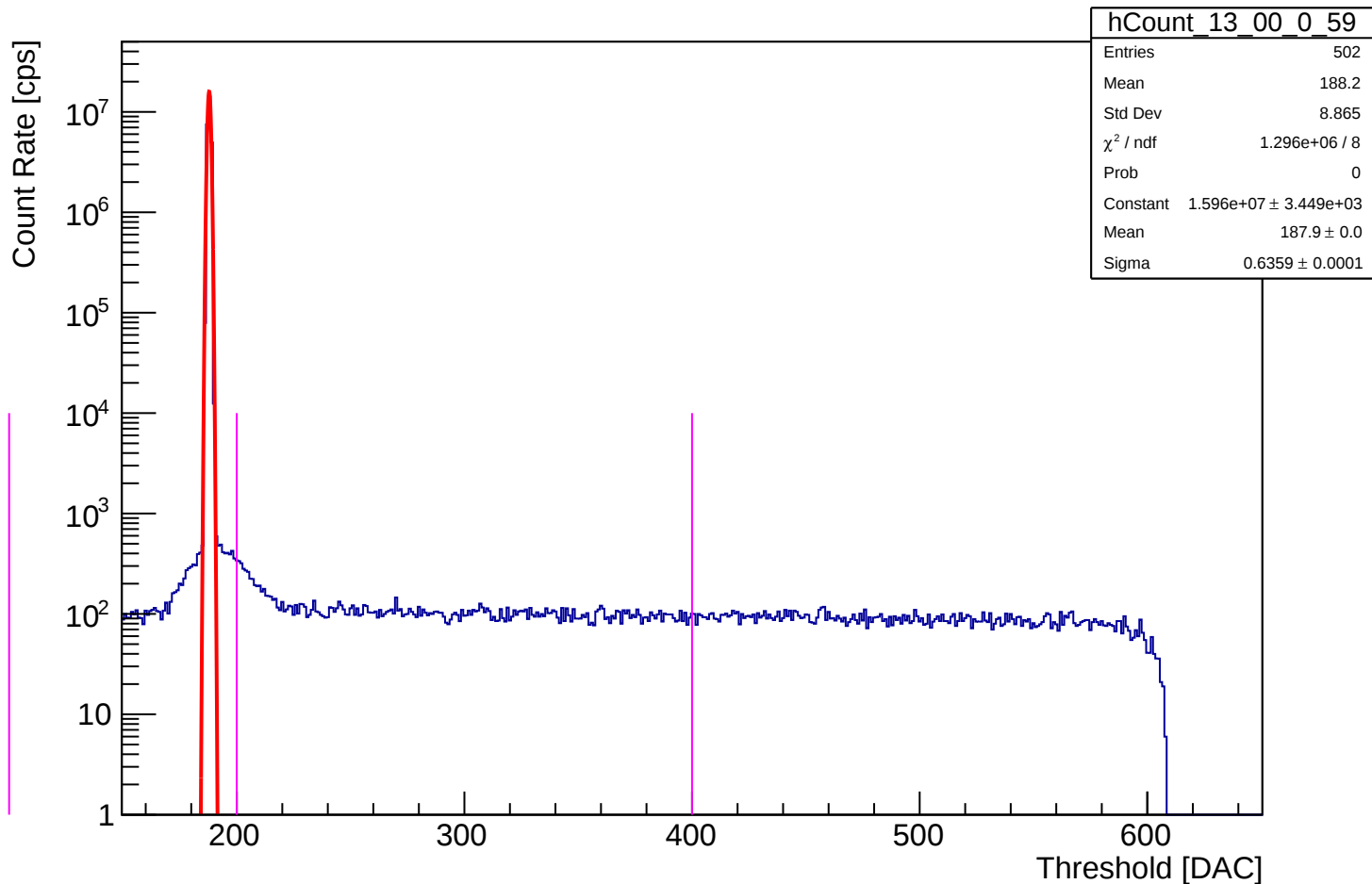
Row 1 Tile 1 Pmt 1 Pixel 54 Slot 13 Fiber 0 Asic 0 Channel 58

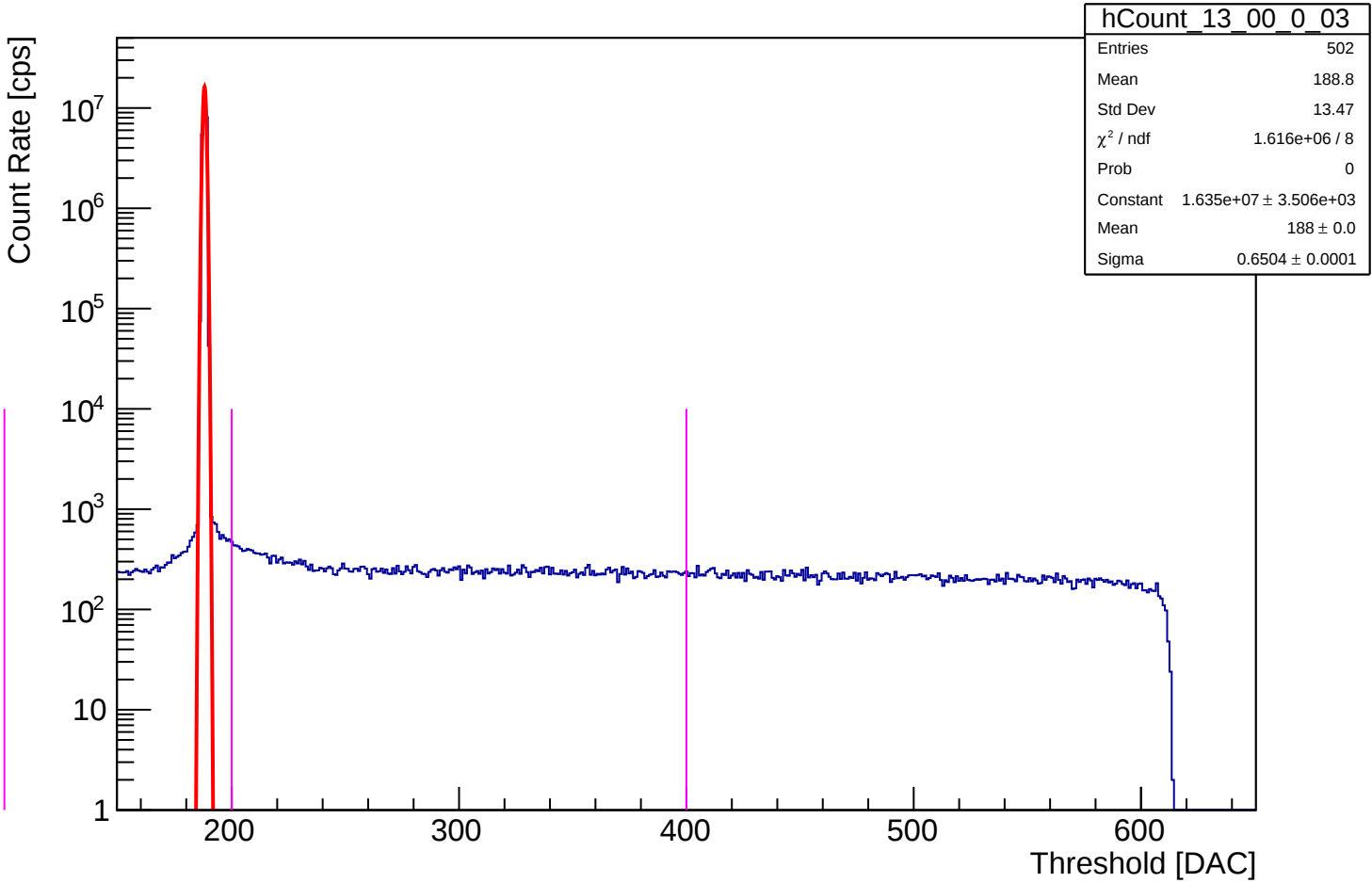


Row 1 Tile 1 Pmt 1 Pixel 55 Slot 13 Fiber 0 Asic 0 Channel 57

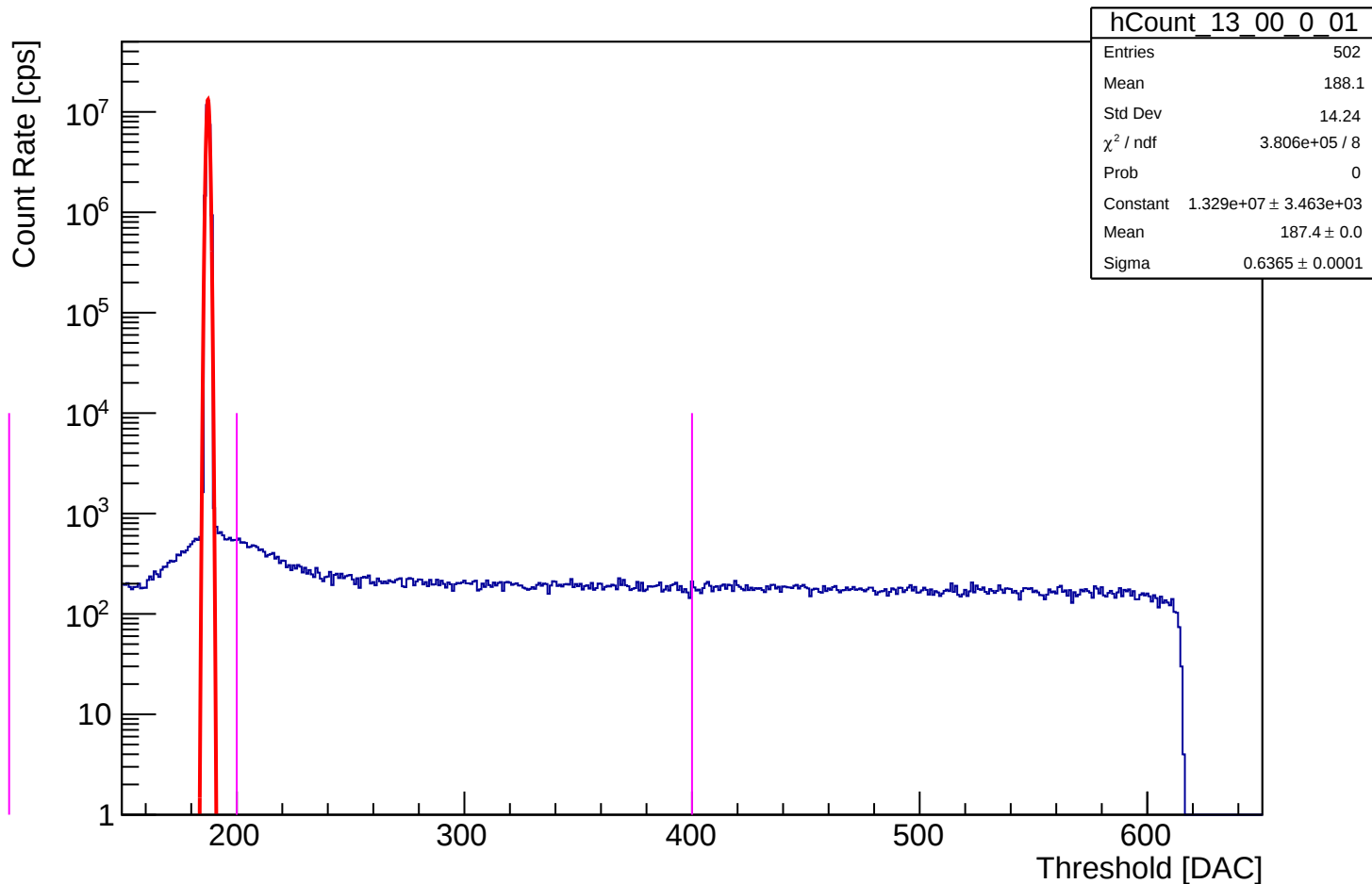


Row 1 Tile 1 Pmt 1 Pixel 56 Slot 13 Fiber 0 Asic 0 Channel 59





Row 1 Tile 1 Pmt 1 Pixel 58 Slot 13 Fiber 0 Asic 0 Channel 1



Count Rate [cps]

10⁷
10⁶
10⁵
10⁴
10³
10²
10
1

200

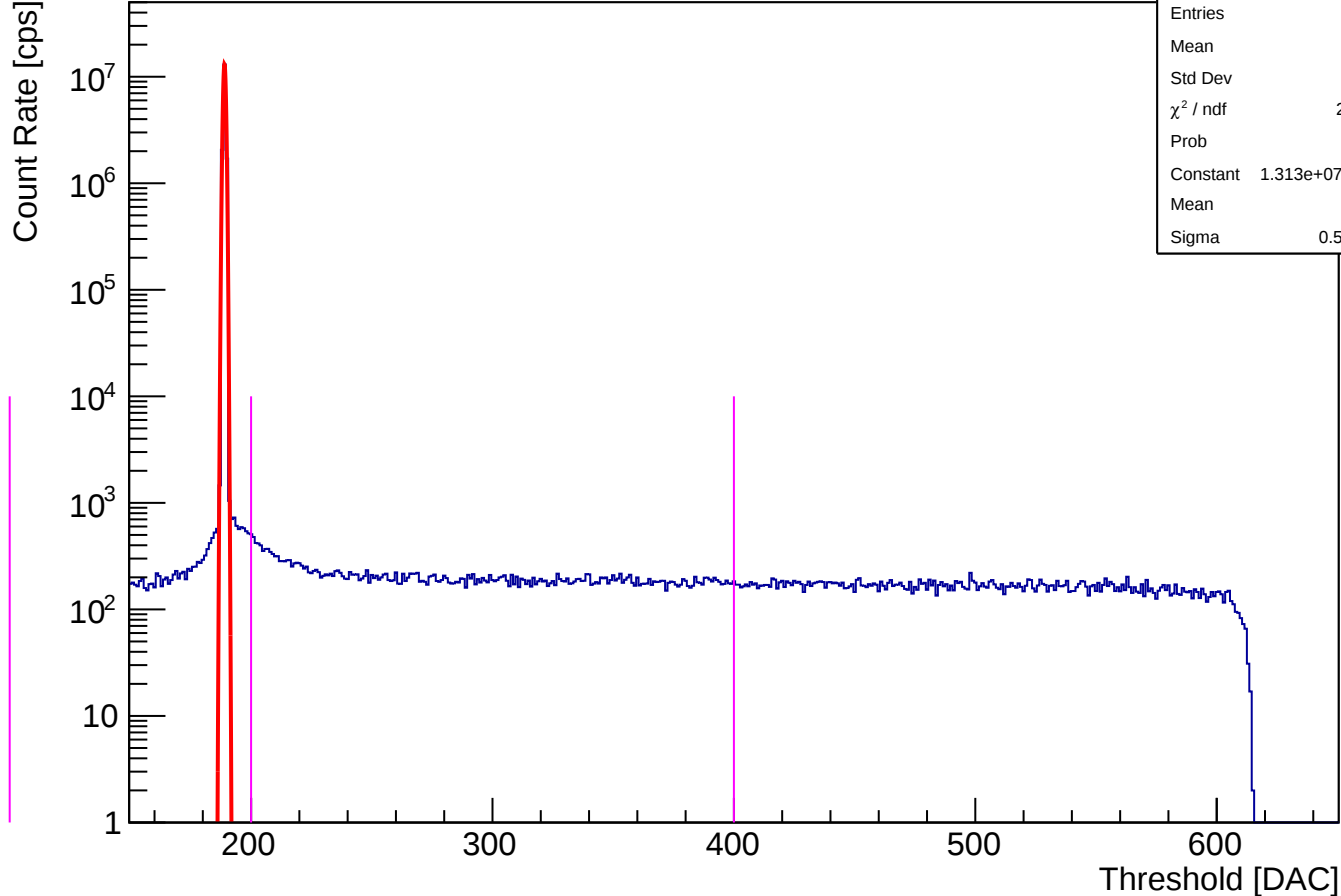
300

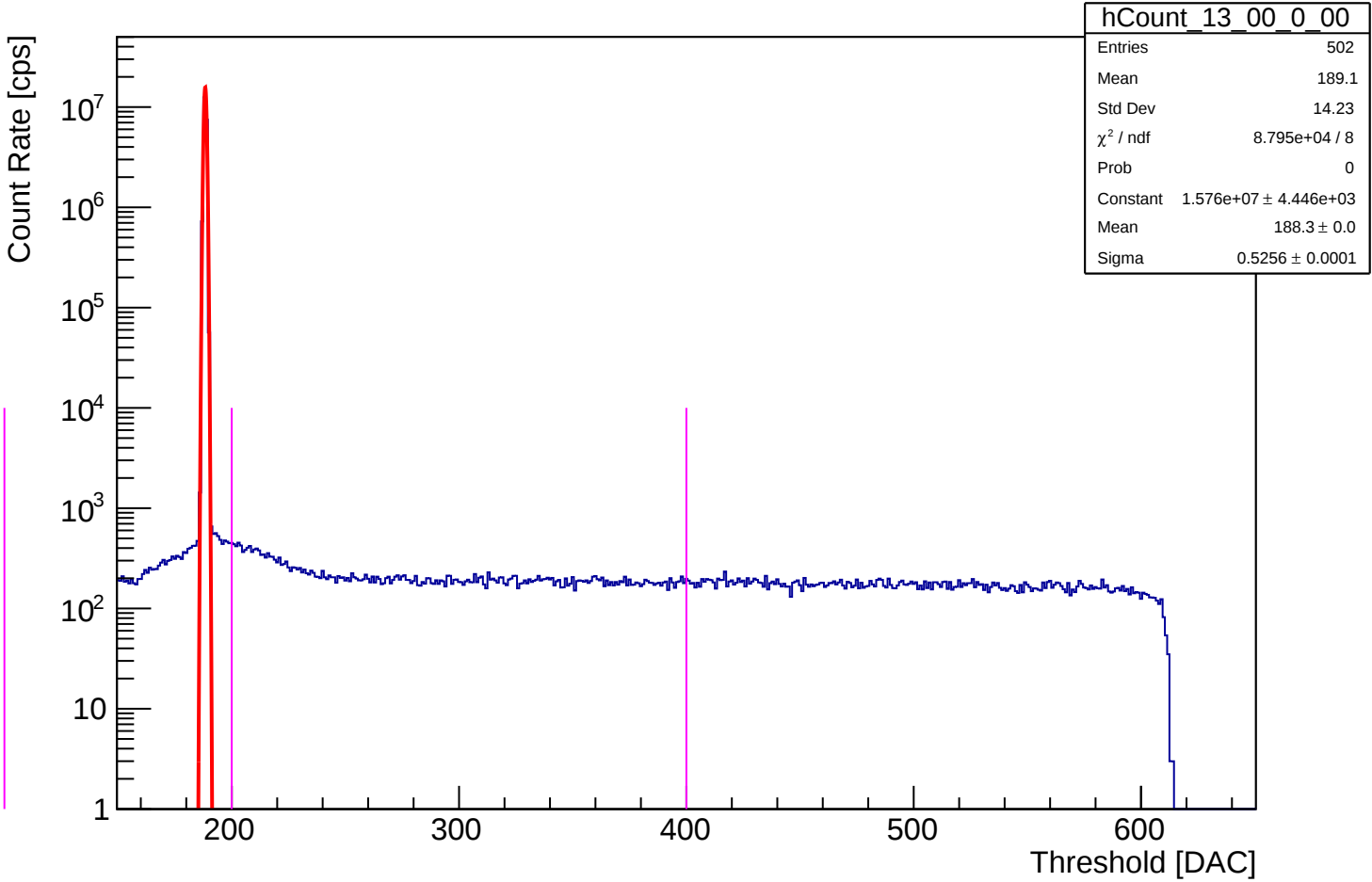
400

500

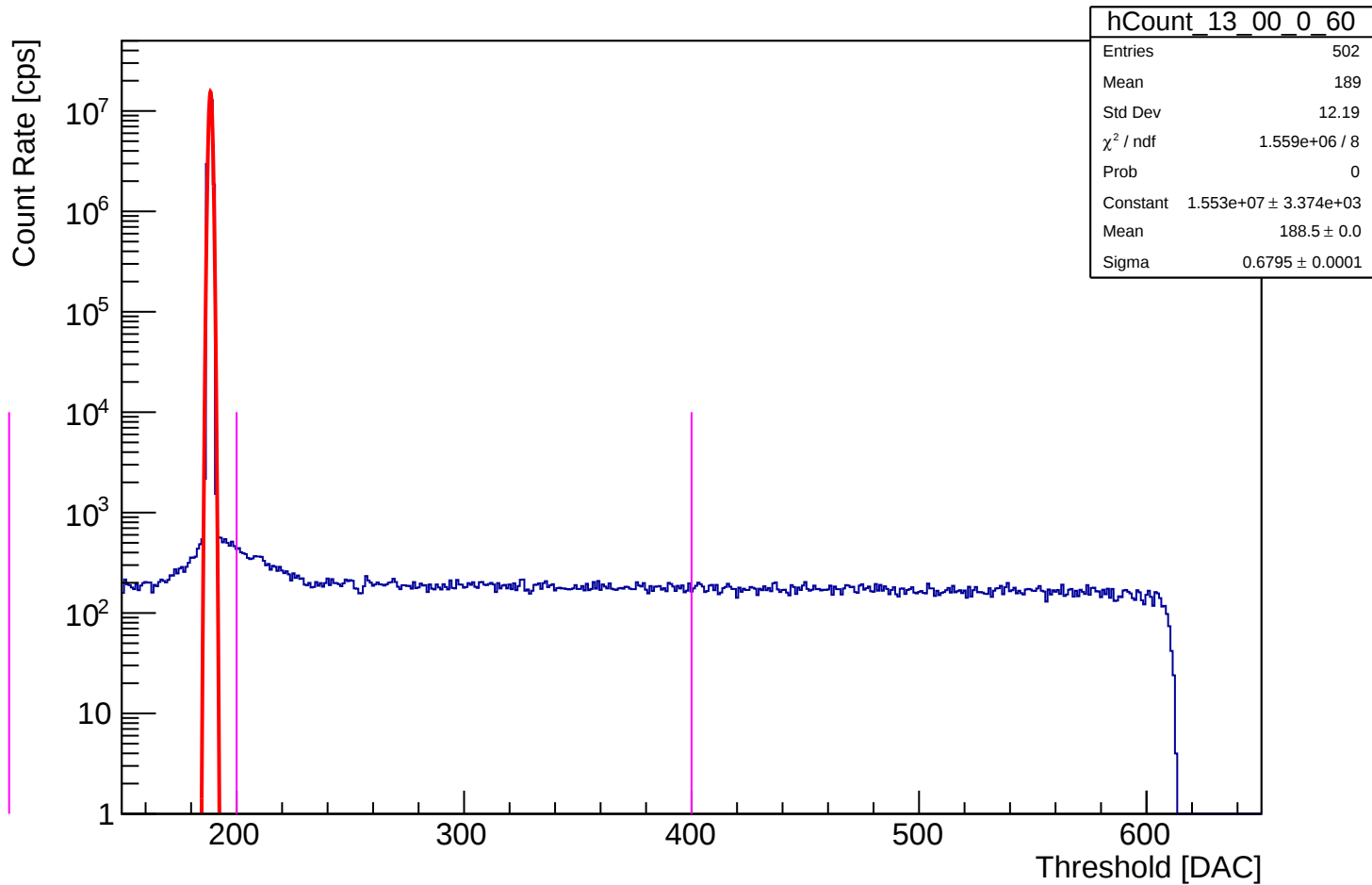
Threshold [DAC]

hCount_13_00_0_02	
Entries	502
Mean	189.9
Std Dev	15.56
χ^2 / ndf	2.914e+04 / 8
Prob	0
Constant	1.313e+07 $\pm$ 3.544e+03
Mean	189 $\pm$ 0.0
Sigma	0.5028 $\pm$ 0.0001

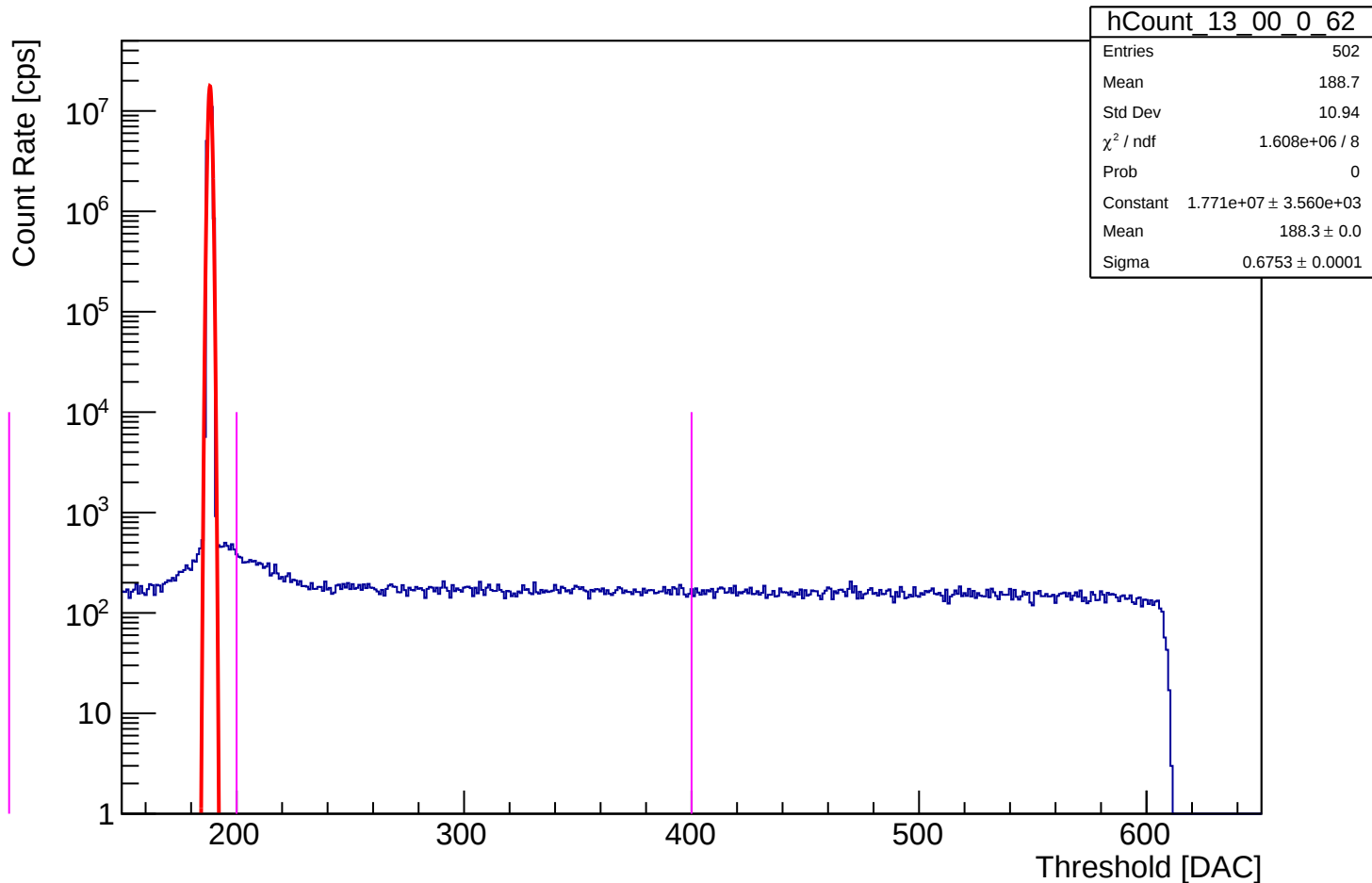




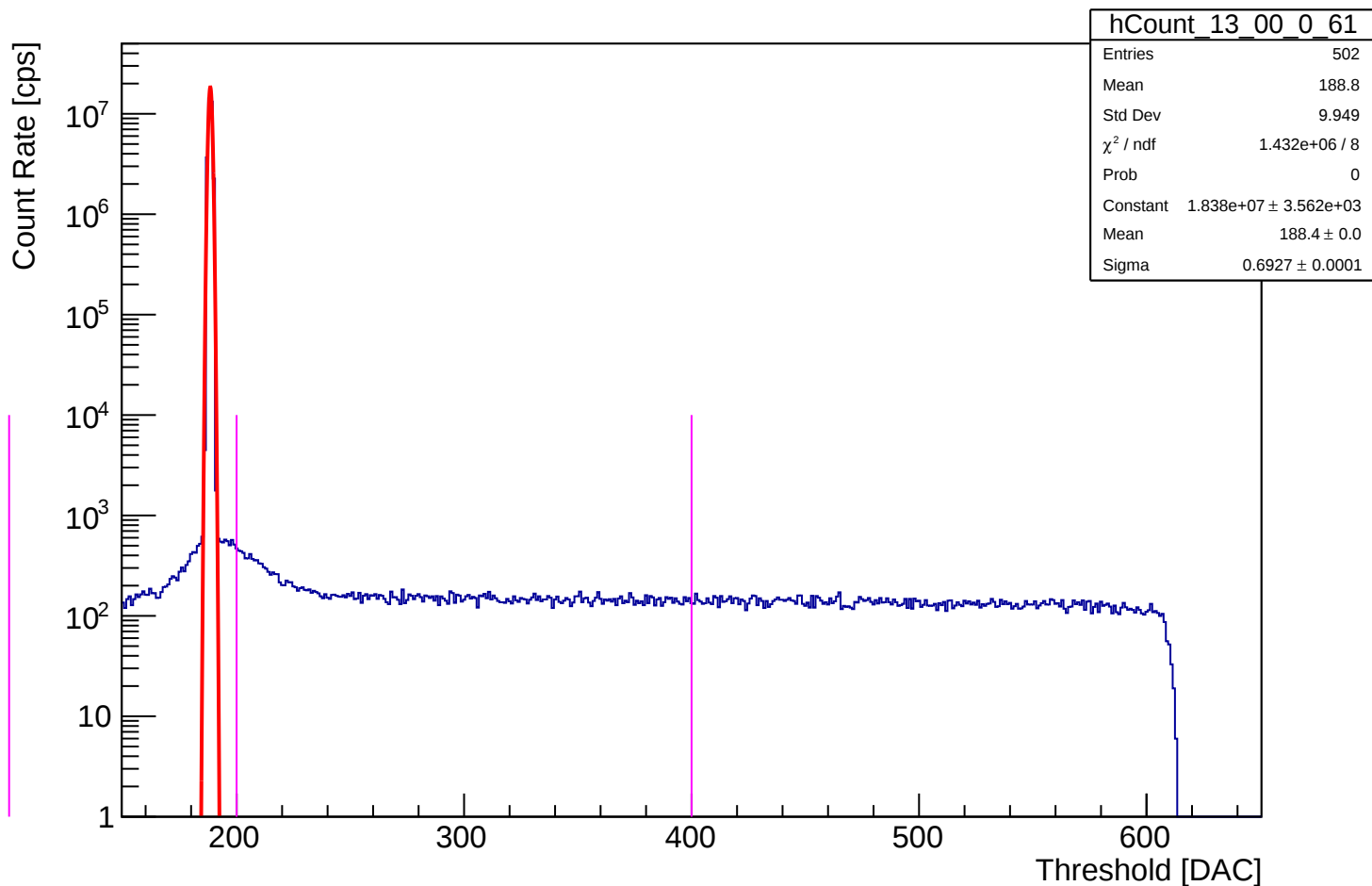
Row 1 Tile 1 Pmt 1 Pixel 61 Slot 13 Fiber 0 Asic 0 Channel 60



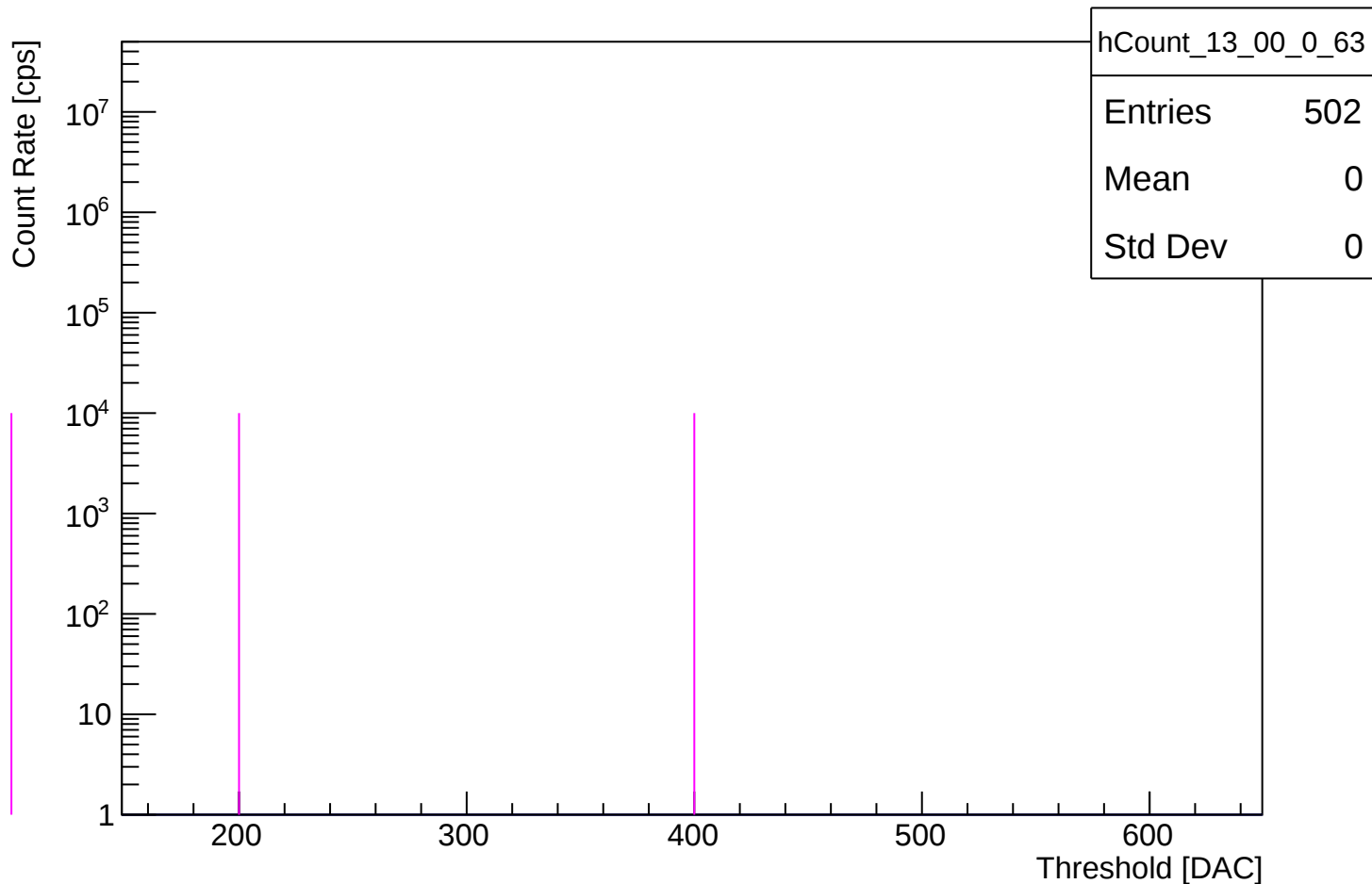
Row 1 Tile 1 Pmt 1 Pixel 62 Slot 13 Fiber 0 Asic 0 Channel 62



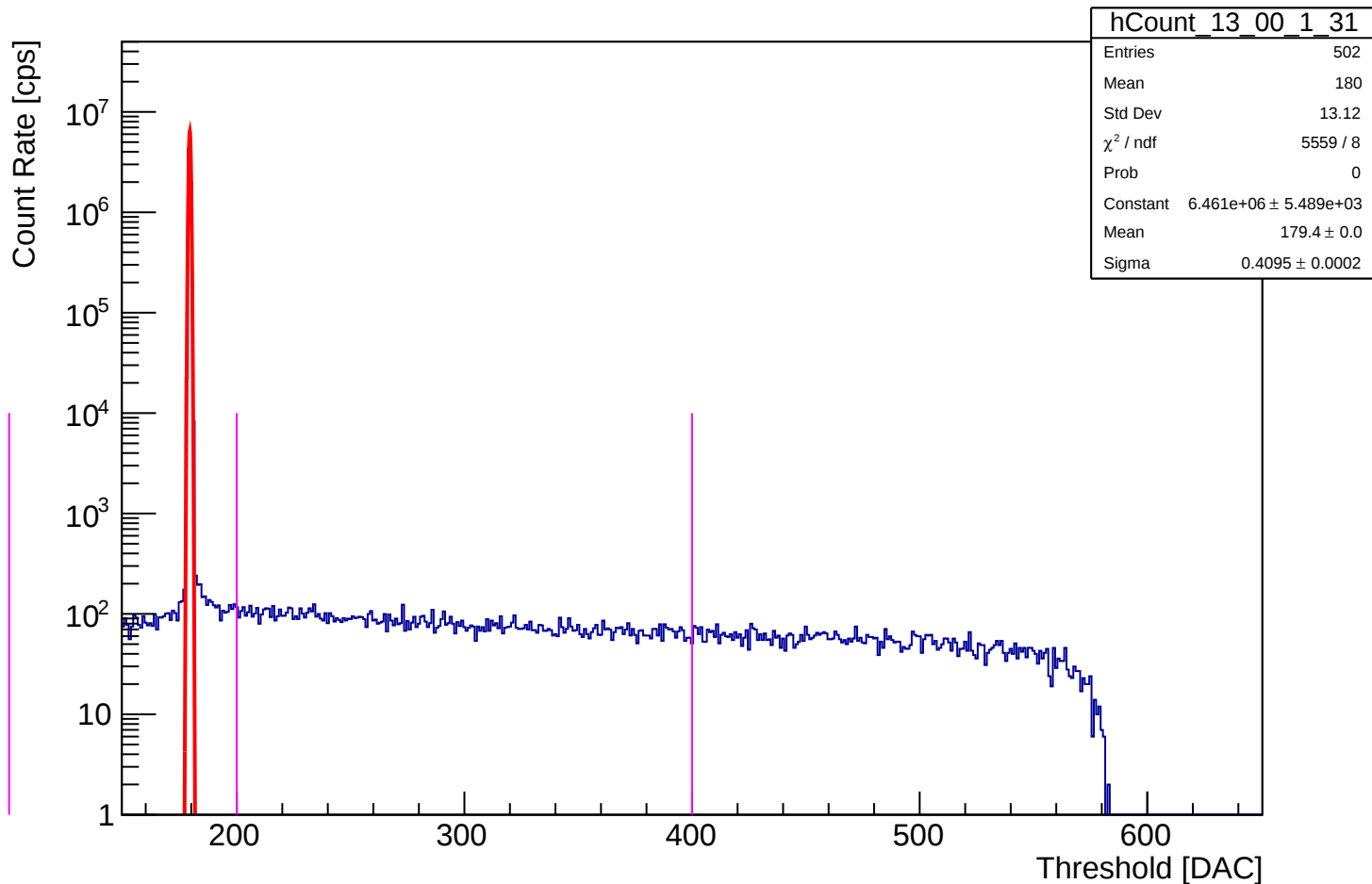
Row 1 Tile 1 Pmt 1 Pixel 63 Slot 13 Fiber 0 Asic 0 Channel 61



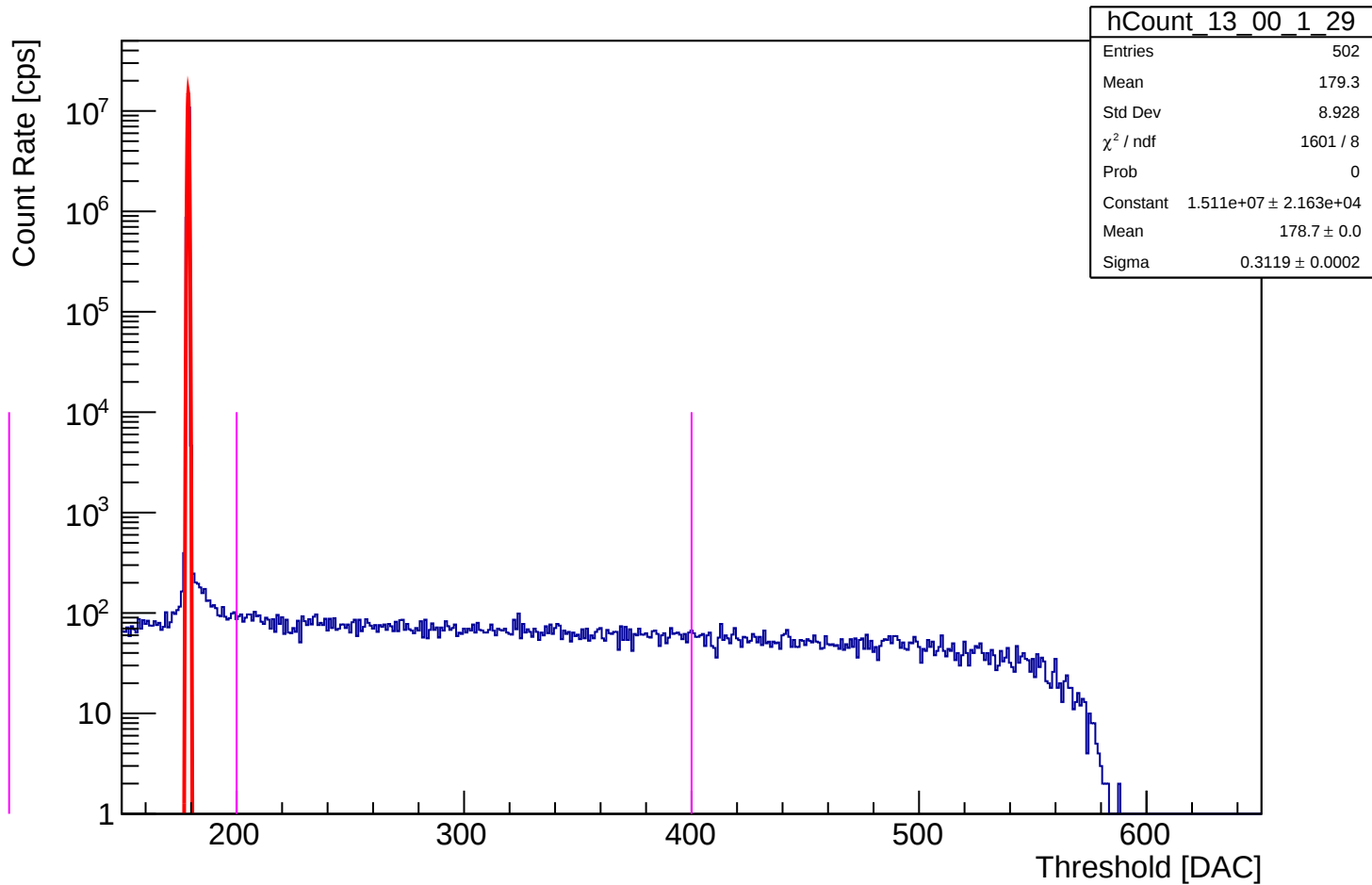
Row 1 Tile 1 Pmt 1 Pixel 64 Slot 13 Fiber 0 Asic 0 Channel 63



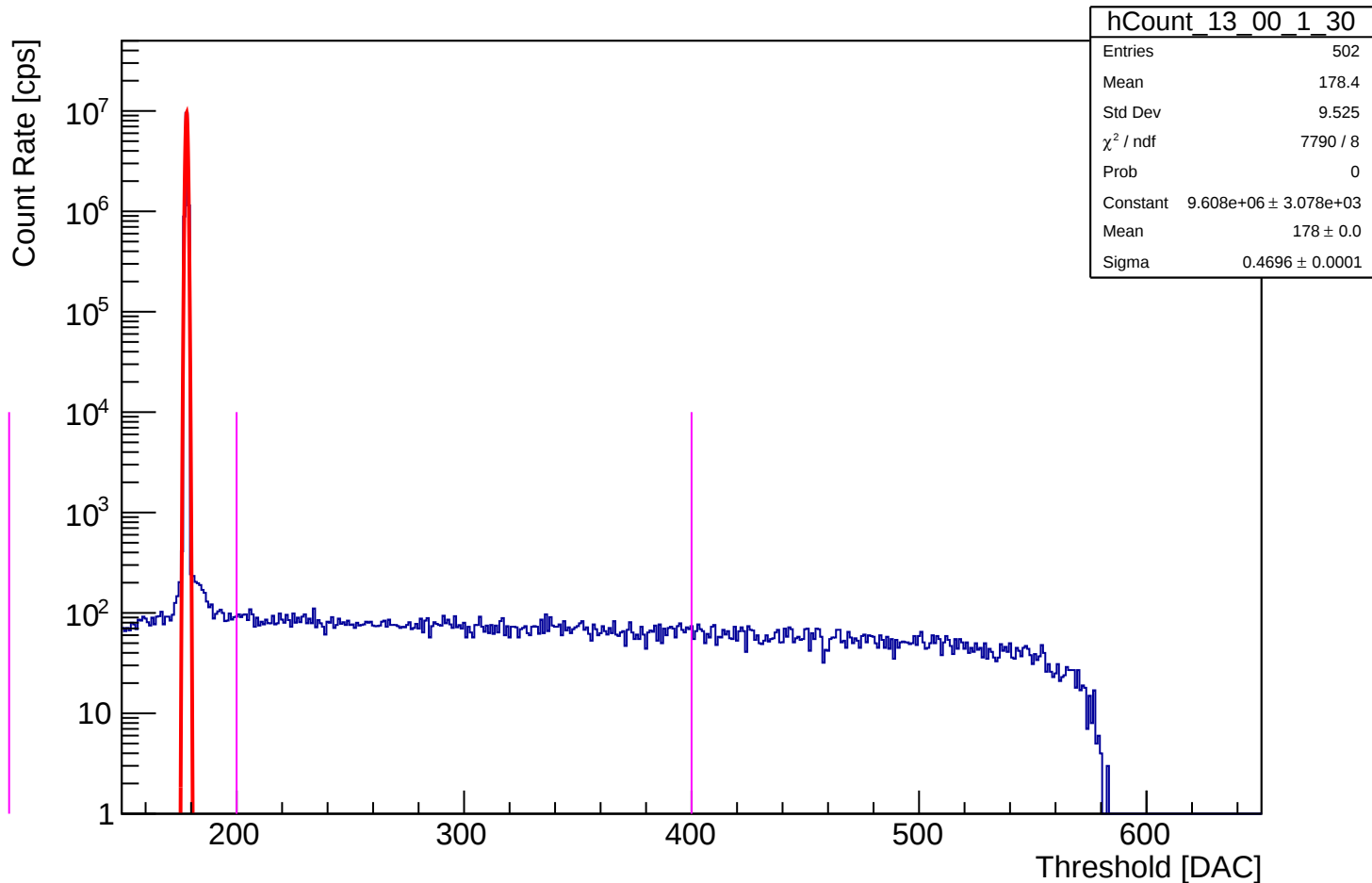
Row 1 Tile 1 Pmt 2 Pixel 1 Slot 13 Fiber 0 Asic 1 Channel 31



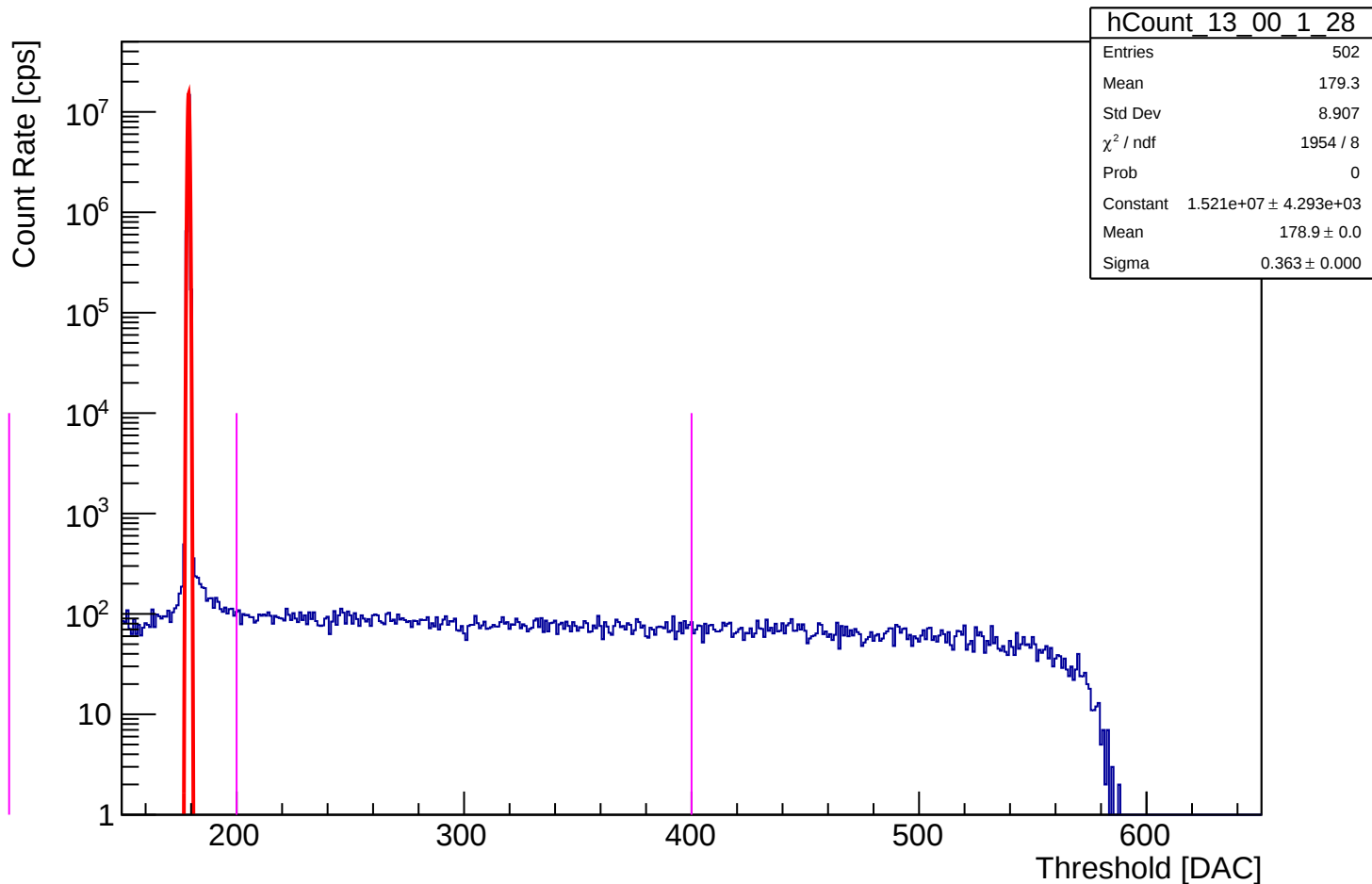
Row 1 Tile 1 Pmt 2 Pixel 2 Slot 13 Fiber 0 Asic 1 Channel 29



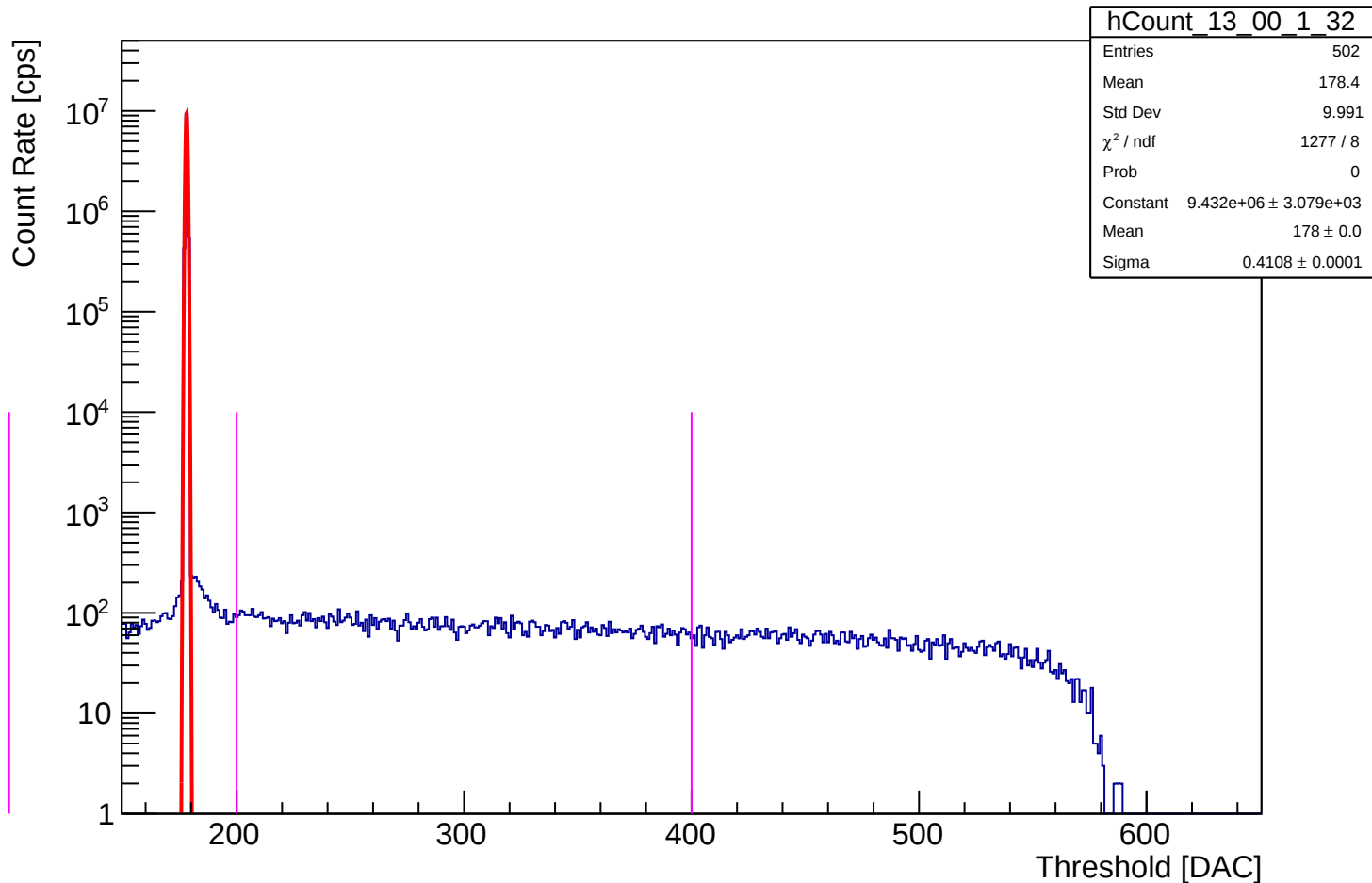
Row 1 Tile 1 Pmt 2 Pixel 3 Slot 13 Fiber 0 Asic 1 Channel 30



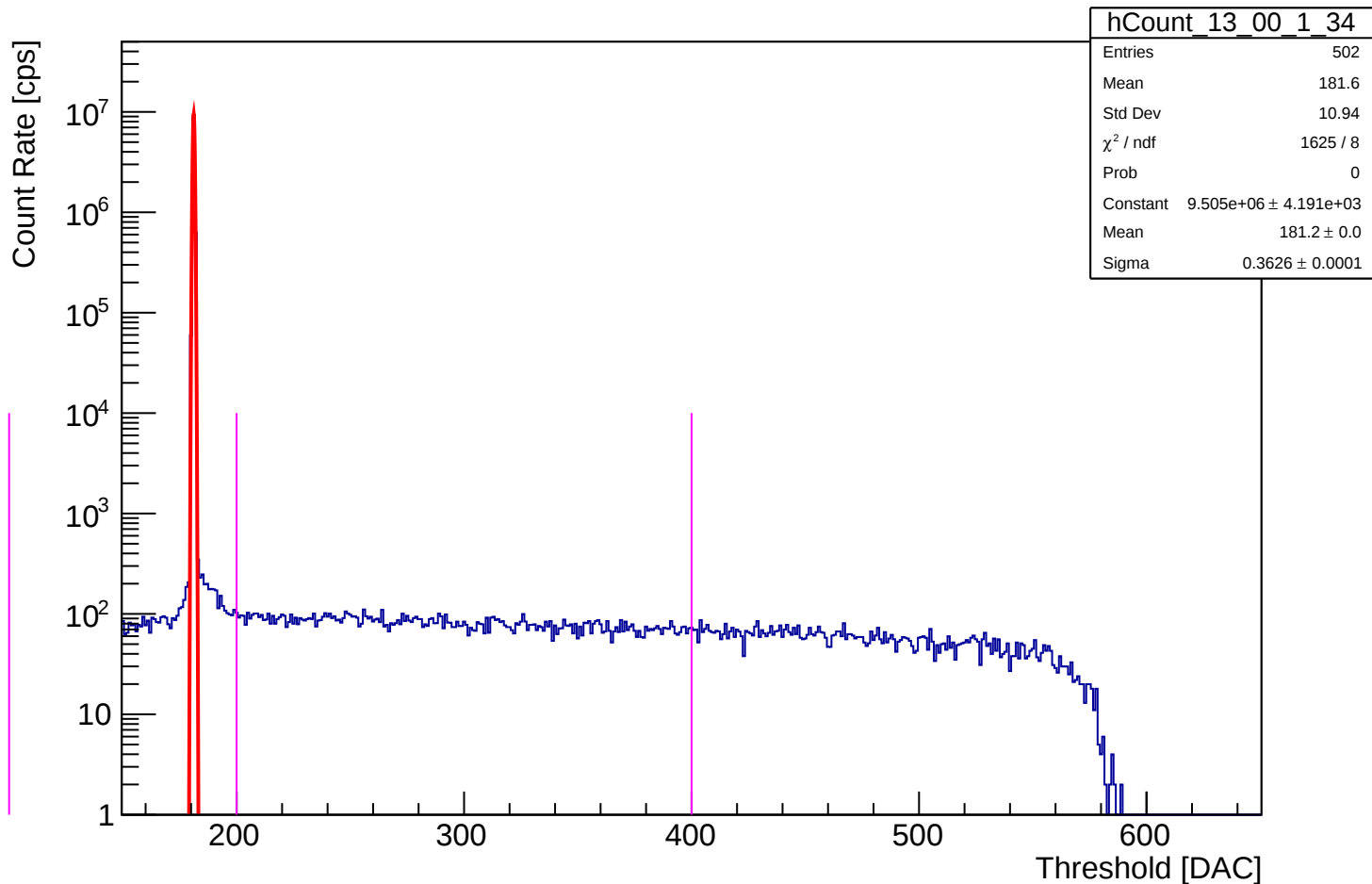
Row 1 Tile 1 Pmt 2 Pixel 4 Slot 13 Fiber 0 Asic 1 Channel 28



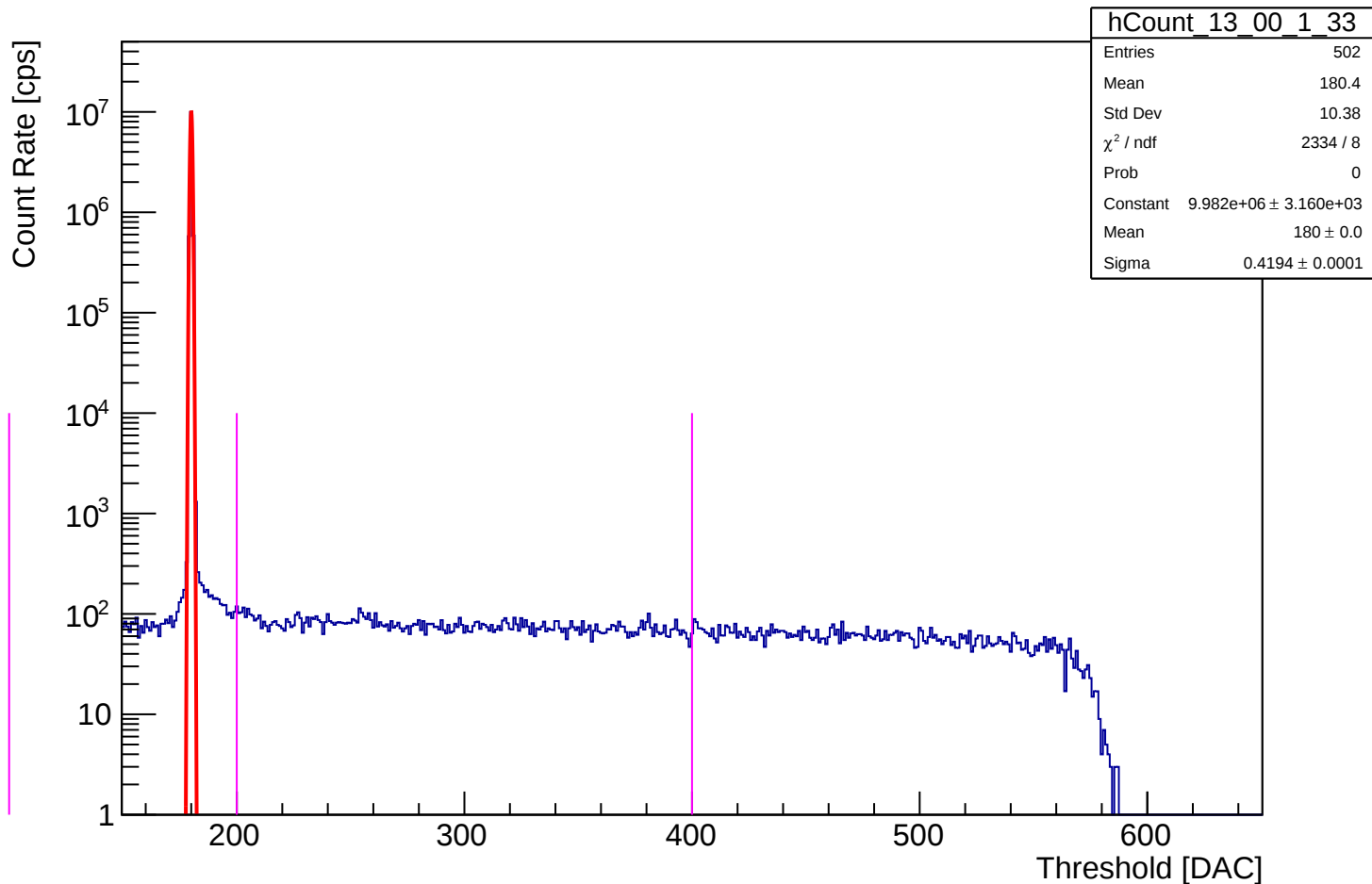
Row 1 Tile 1 Pmt 2 Pixel 5 Slot 13 Fiber 0 Asic 1 Channel 32



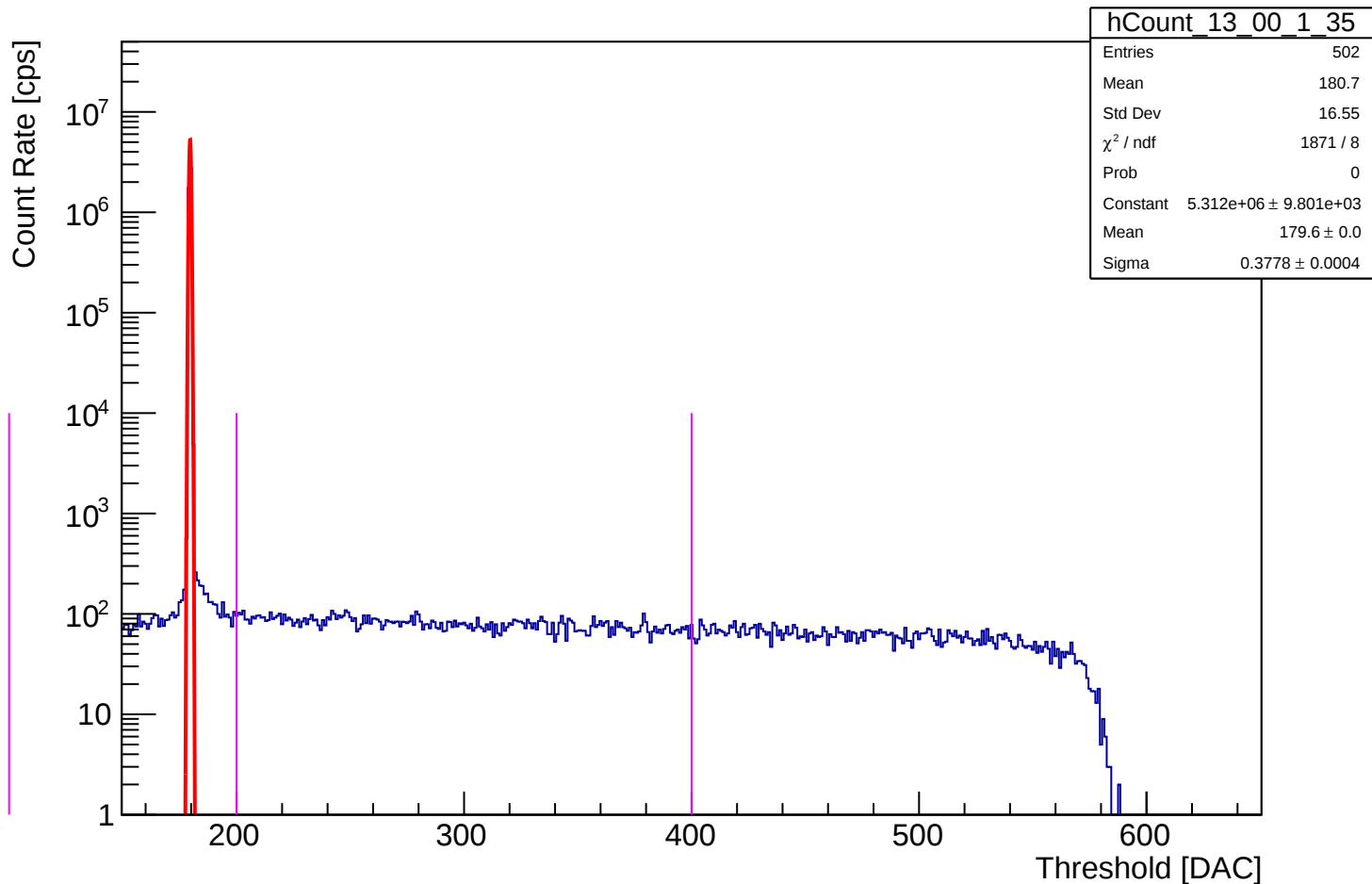
Row 1 Tile 1 Pmt 2 Pixel 6 Slot 13 Fiber 0 Asic 1 Channel 34



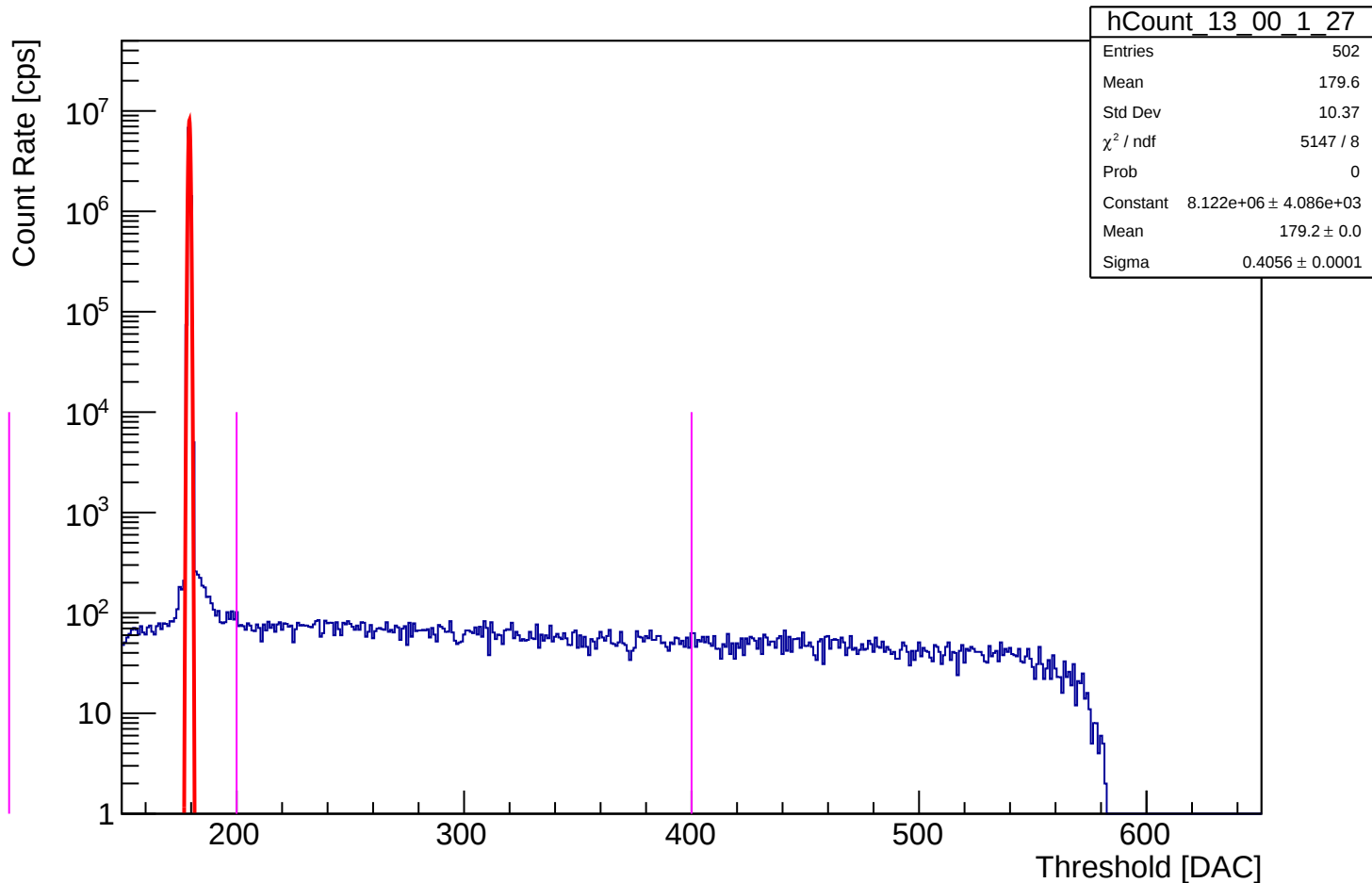
Row 1 Tile 1 Pmt 2 Pixel 7 Slot 13 Fiber 0 Asic 1 Channel 33



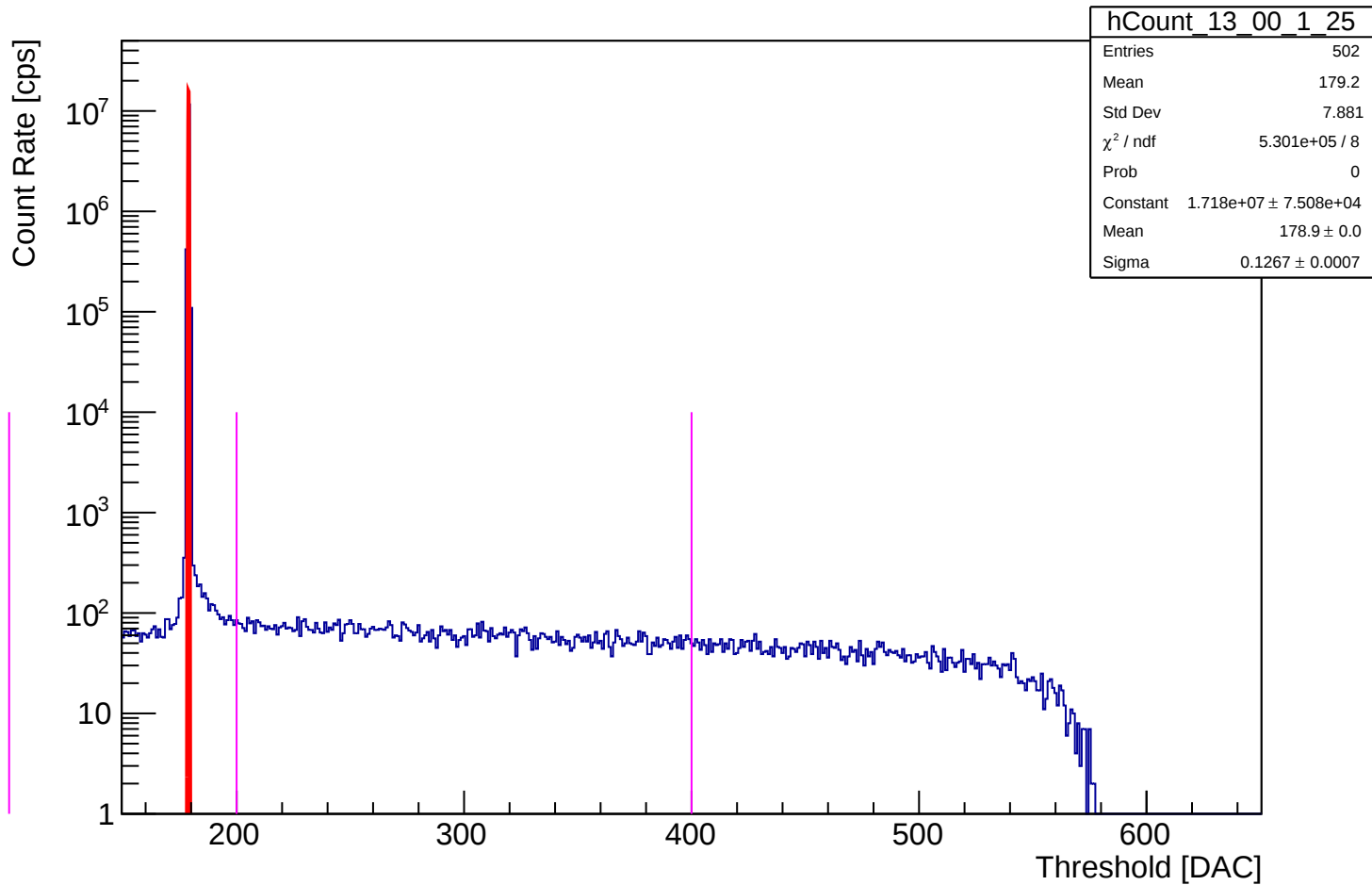
Row 1 Tile 1 Pmt 2 Pixel 8 Slot 13 Fiber 0 Asic 1 Channel 35



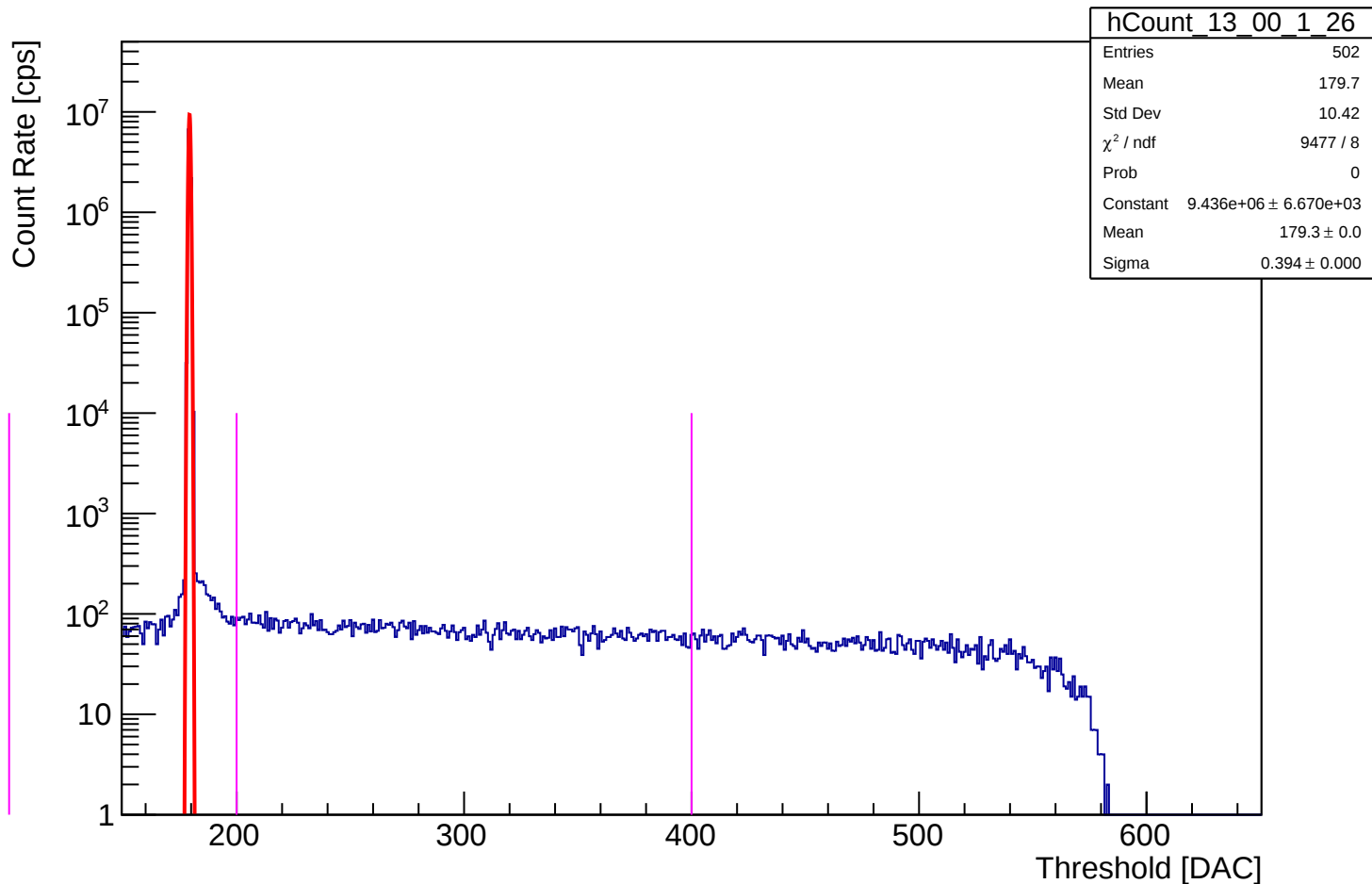
Row 1 Tile 1 Pmt 2 Pixel 9 Slot 13 Fiber 0 Asic 1 Channel 27



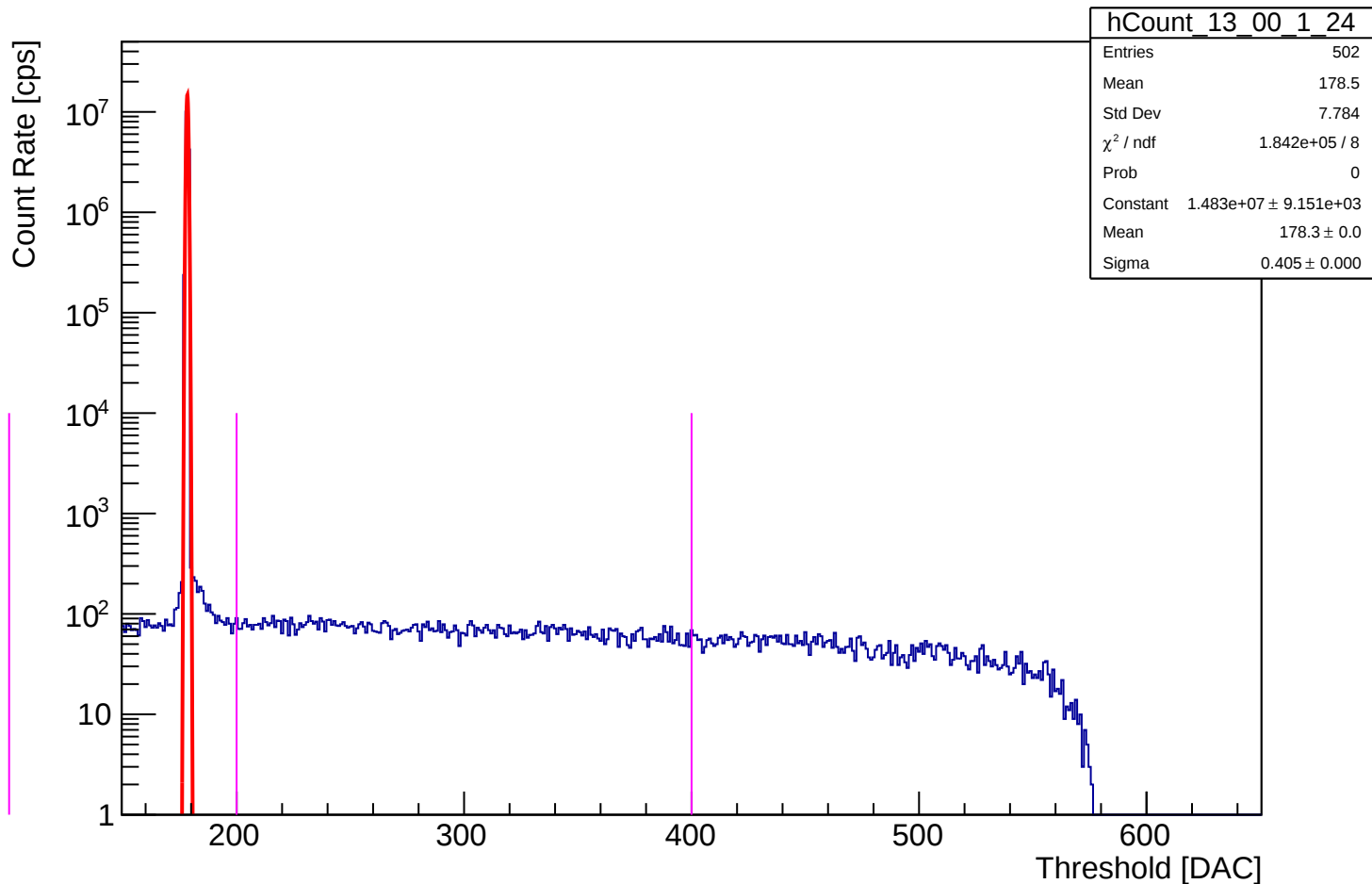
Row 1 Tile 1 Pmt 2 Pixel 10 Slot 13 Fiber 0 Asic 1 Channel 25



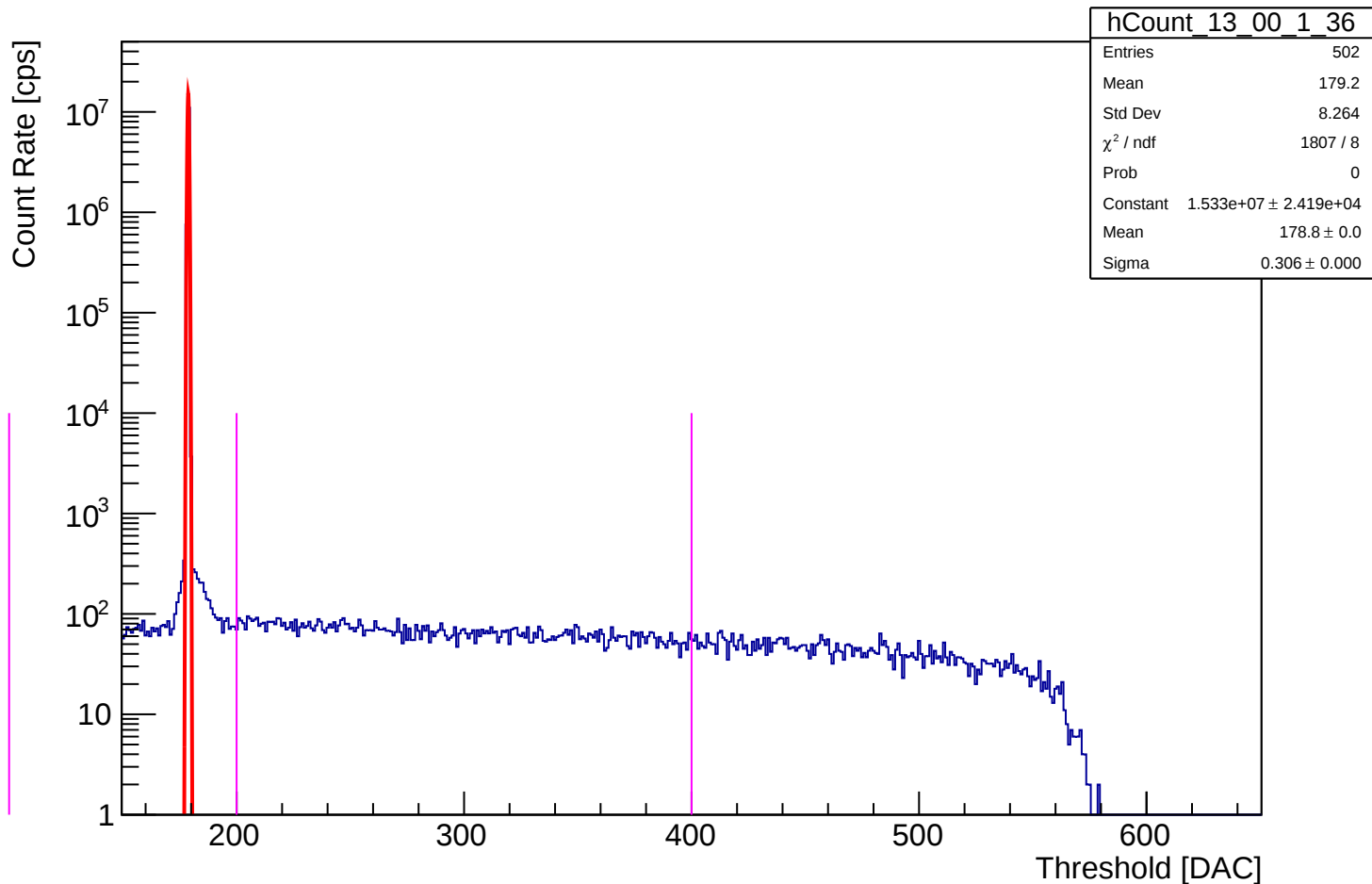
Row 1 Tile 1 Pmt 2 Pixel 11 Slot 13 Fiber 0 Asic 1 Channel 26



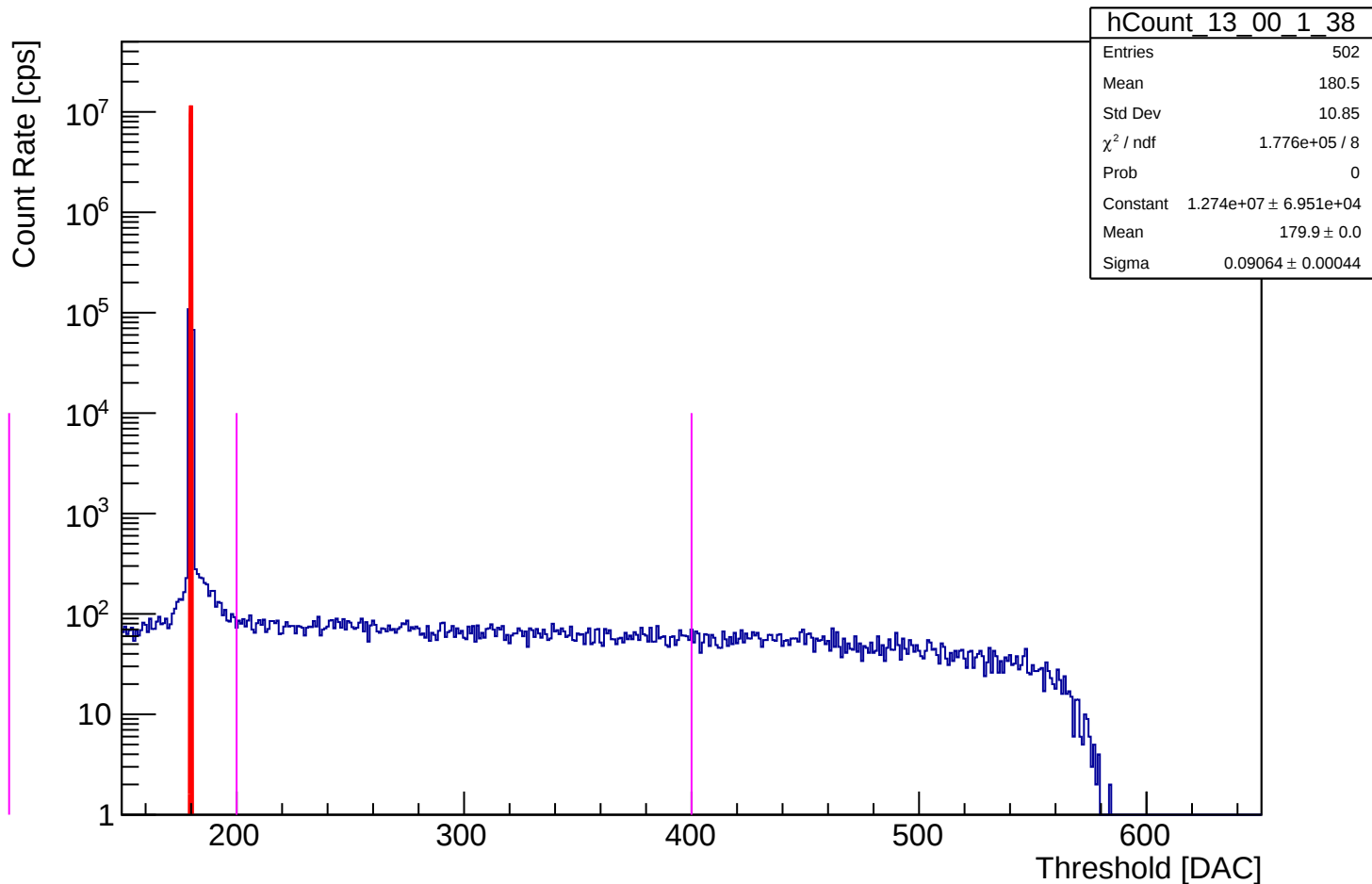
Row 1 Tile 1 Pmt 2 Pixel 12 Slot 13 Fiber 0 Asic 1 Channel 24



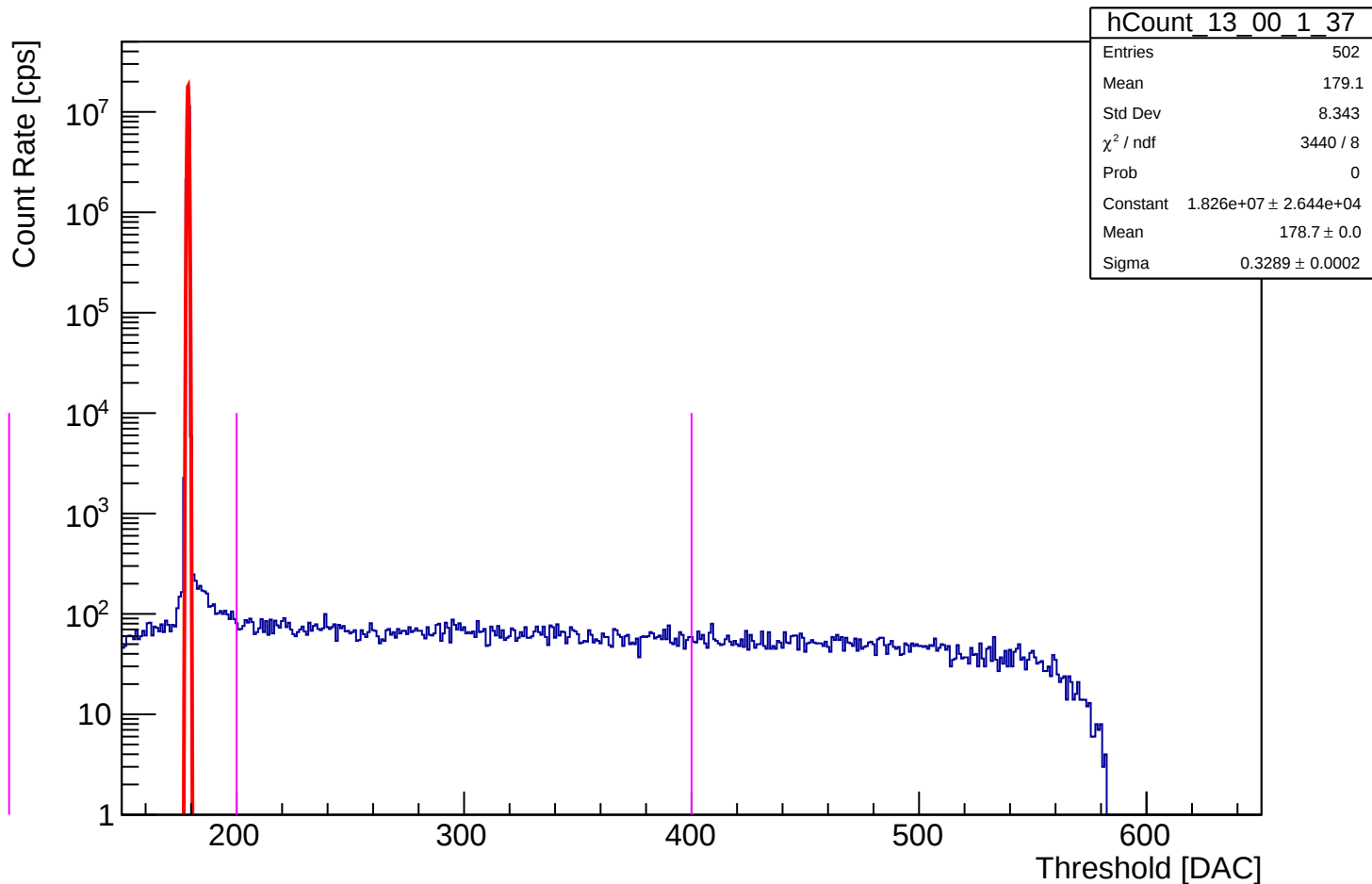
Row 1 Tile 1 Pmt 2 Pixel 13 Slot 13 Fiber 0 Asic 1 Channel 36



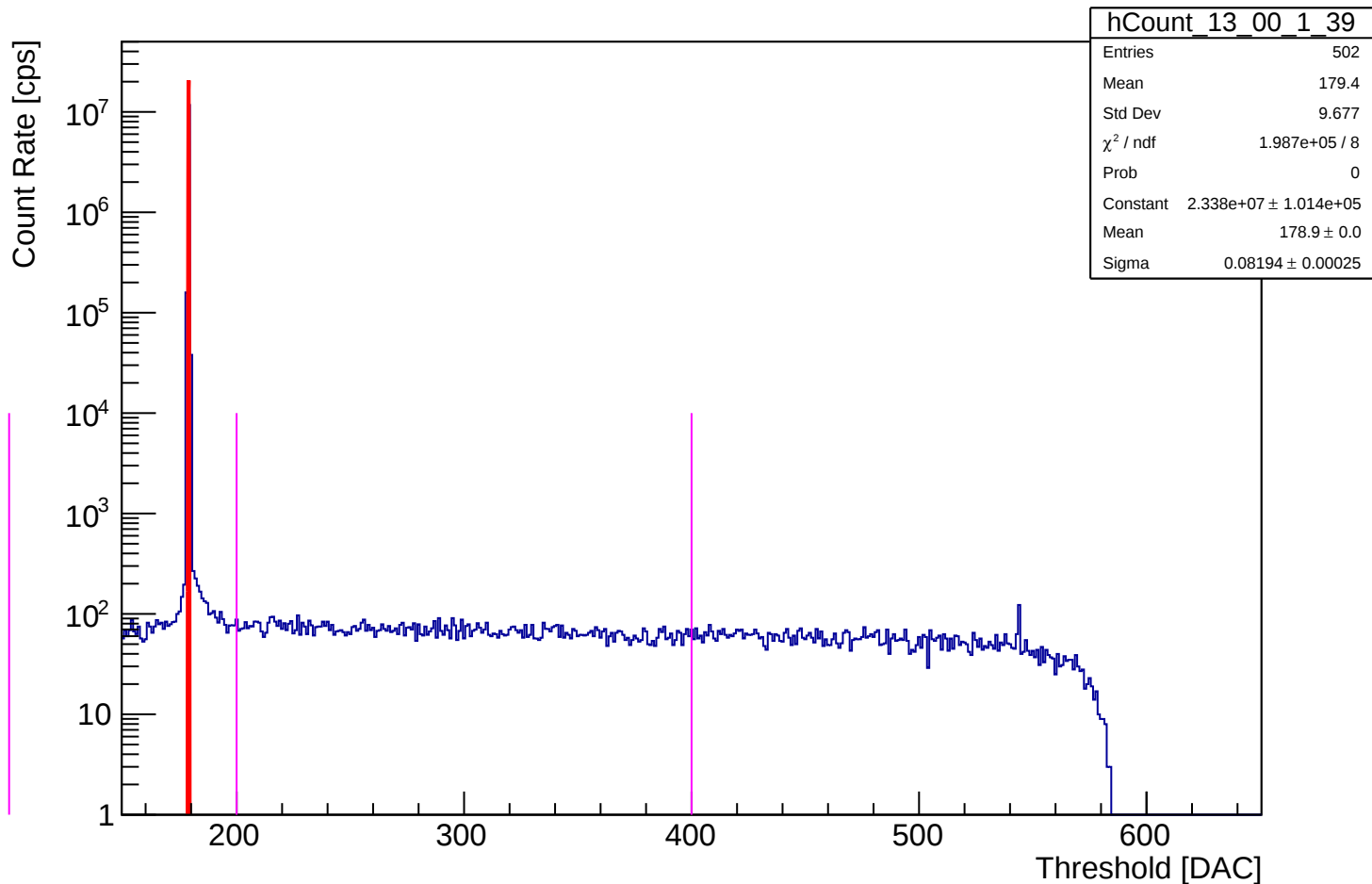
Row 1 Tile 1 Pmt 2 Pixel 14 Slot 13 Fiber 0 Asic 1 Channel 38



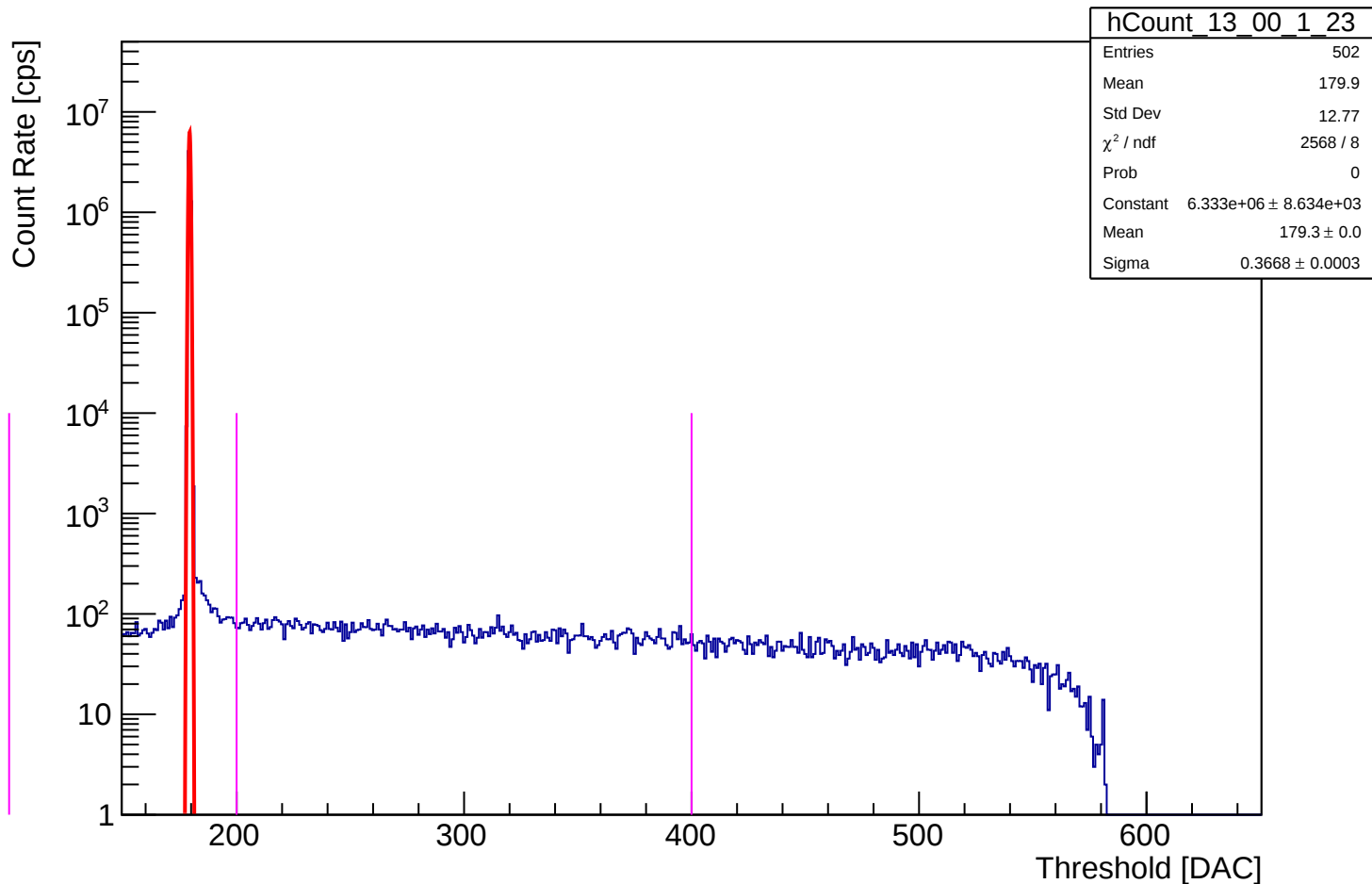
Row 1 Tile 1 Pmt 2 Pixel 15 Slot 13 Fiber 0 Asic 1 Channel 37



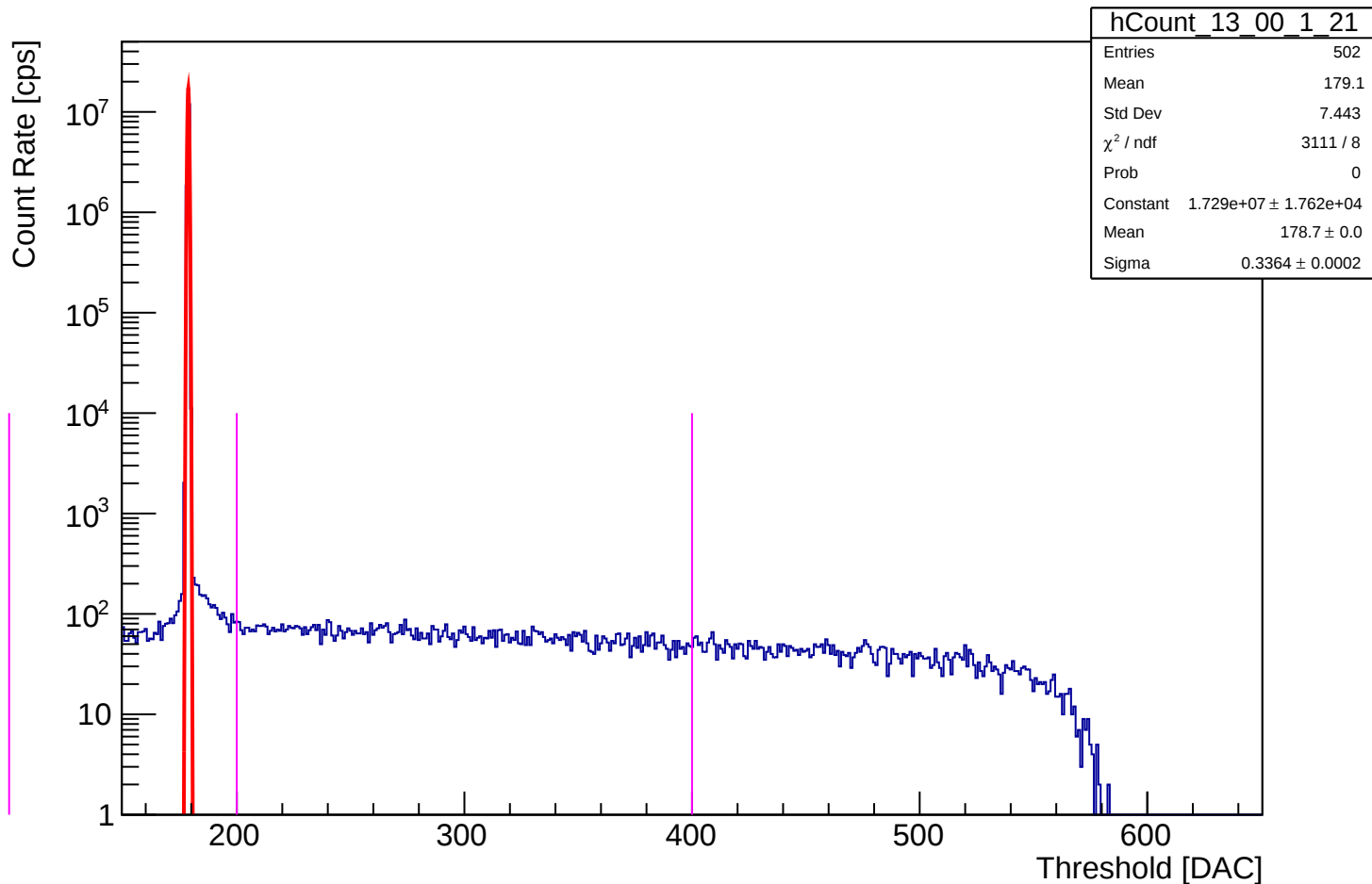
Row 1 Tile 1 Pmt 2 Pixel 16 Slot 13 Fiber 0 Asic 1 Channel 39



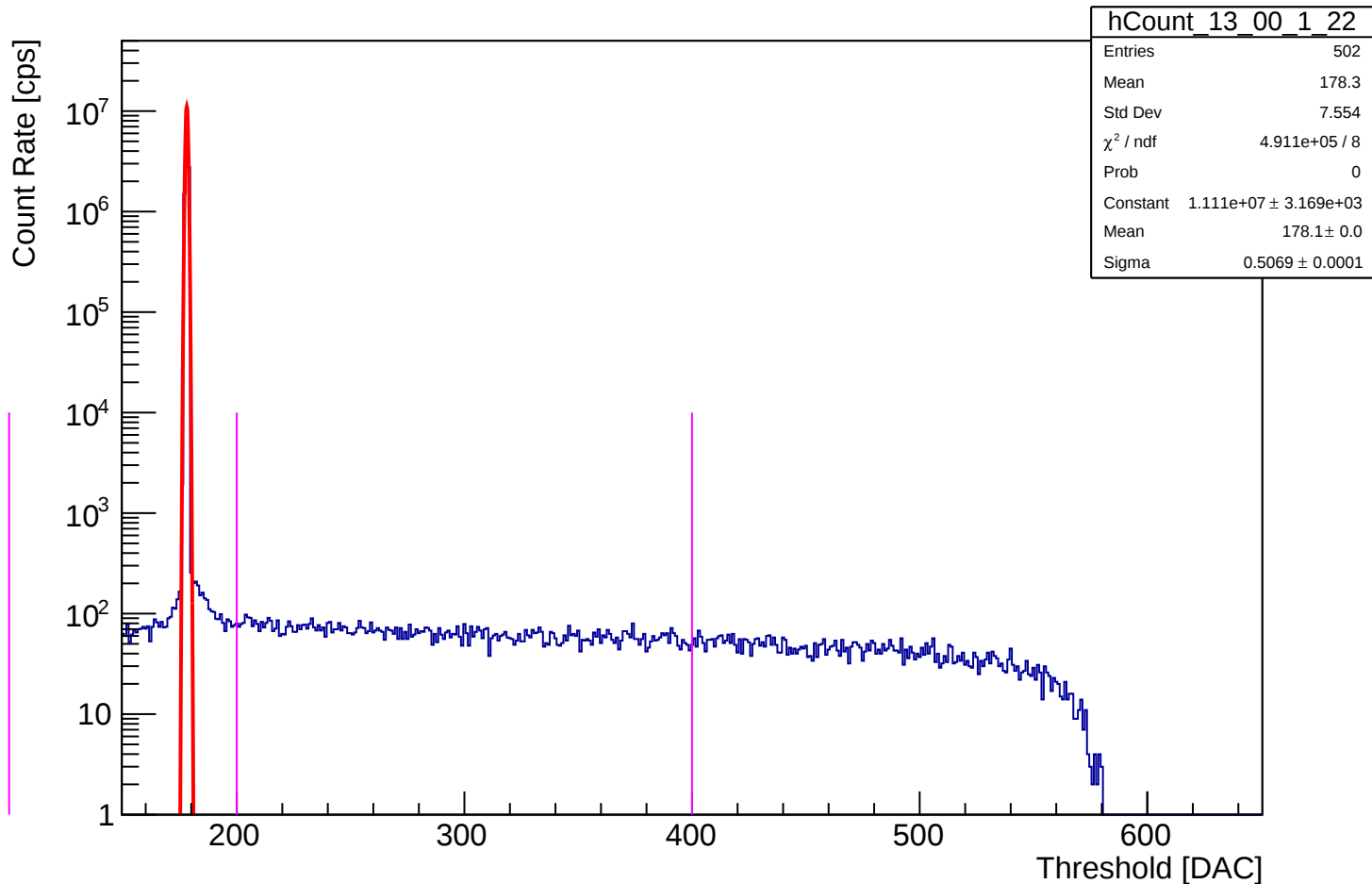
Row 1 Tile 1 Pmt 2 Pixel 17 Slot 13 Fiber 0 Asic 1 Channel 23



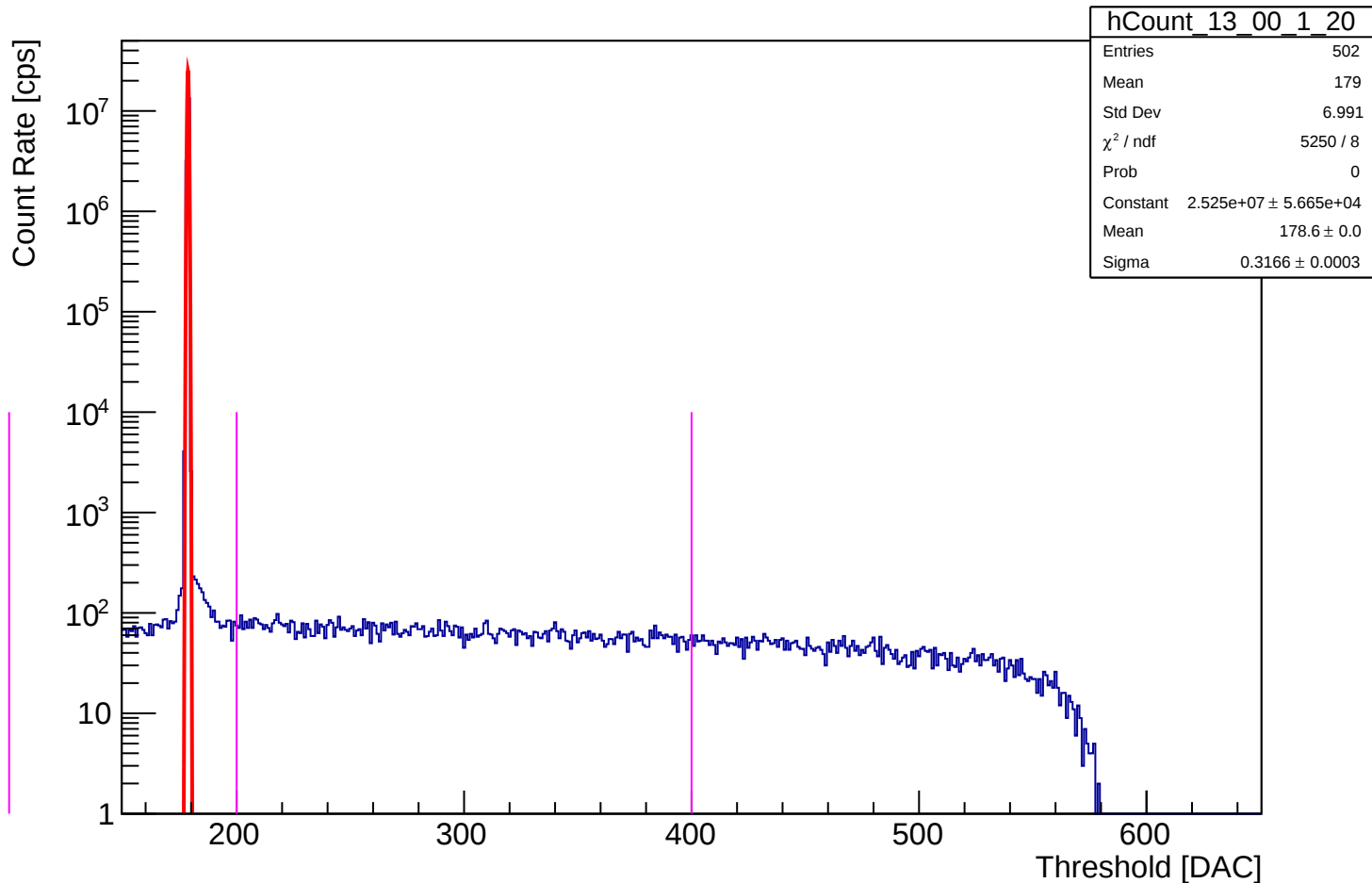
Row 1 Tile 1 Pmt 2 Pixel 18 Slot 13 Fiber 0 Asic 1 Channel 21



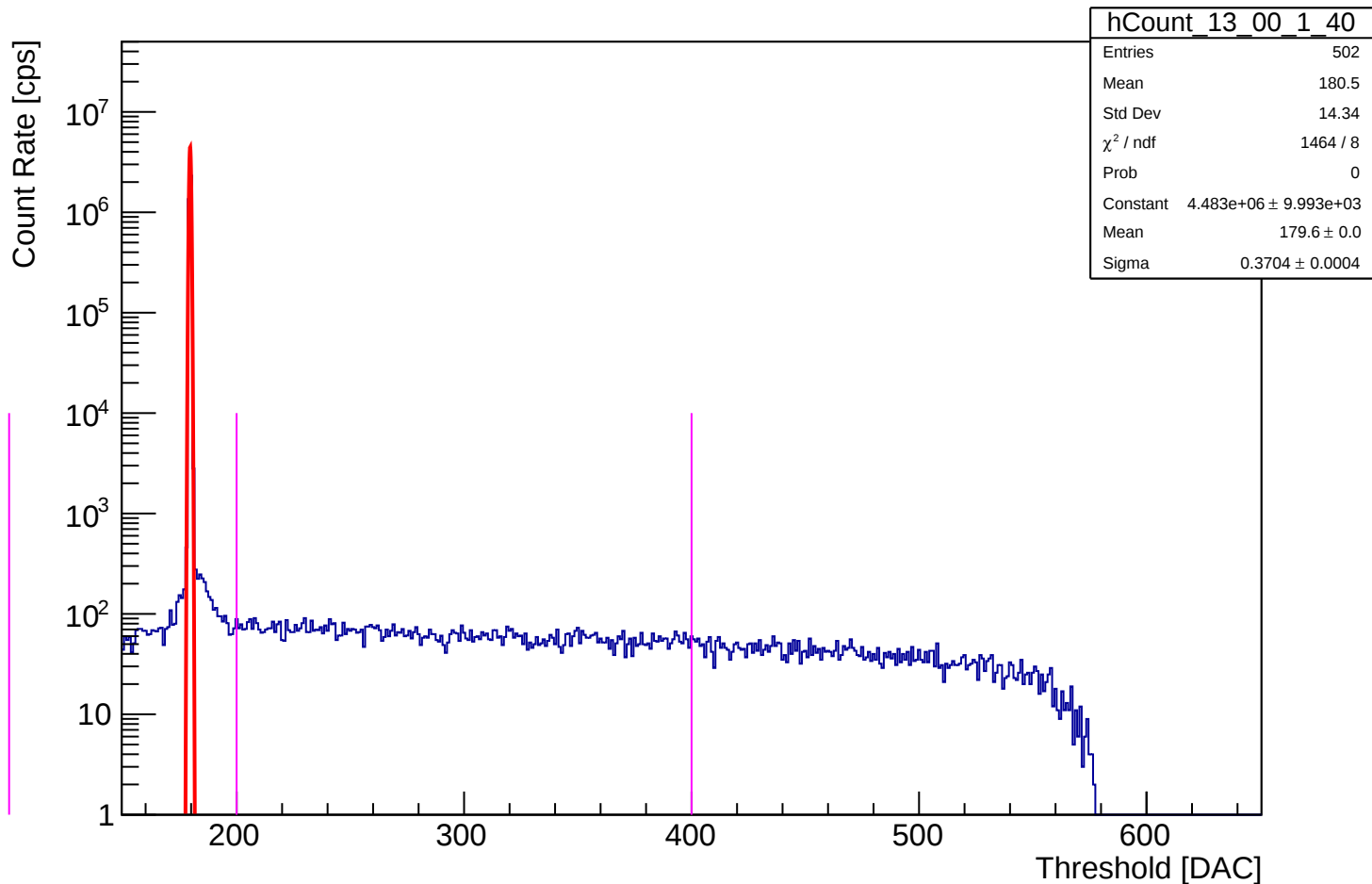
Row 1 Tile 1 Pmt 2 Pixel 19 Slot 13 Fiber 0 Asic 1 Channel 22



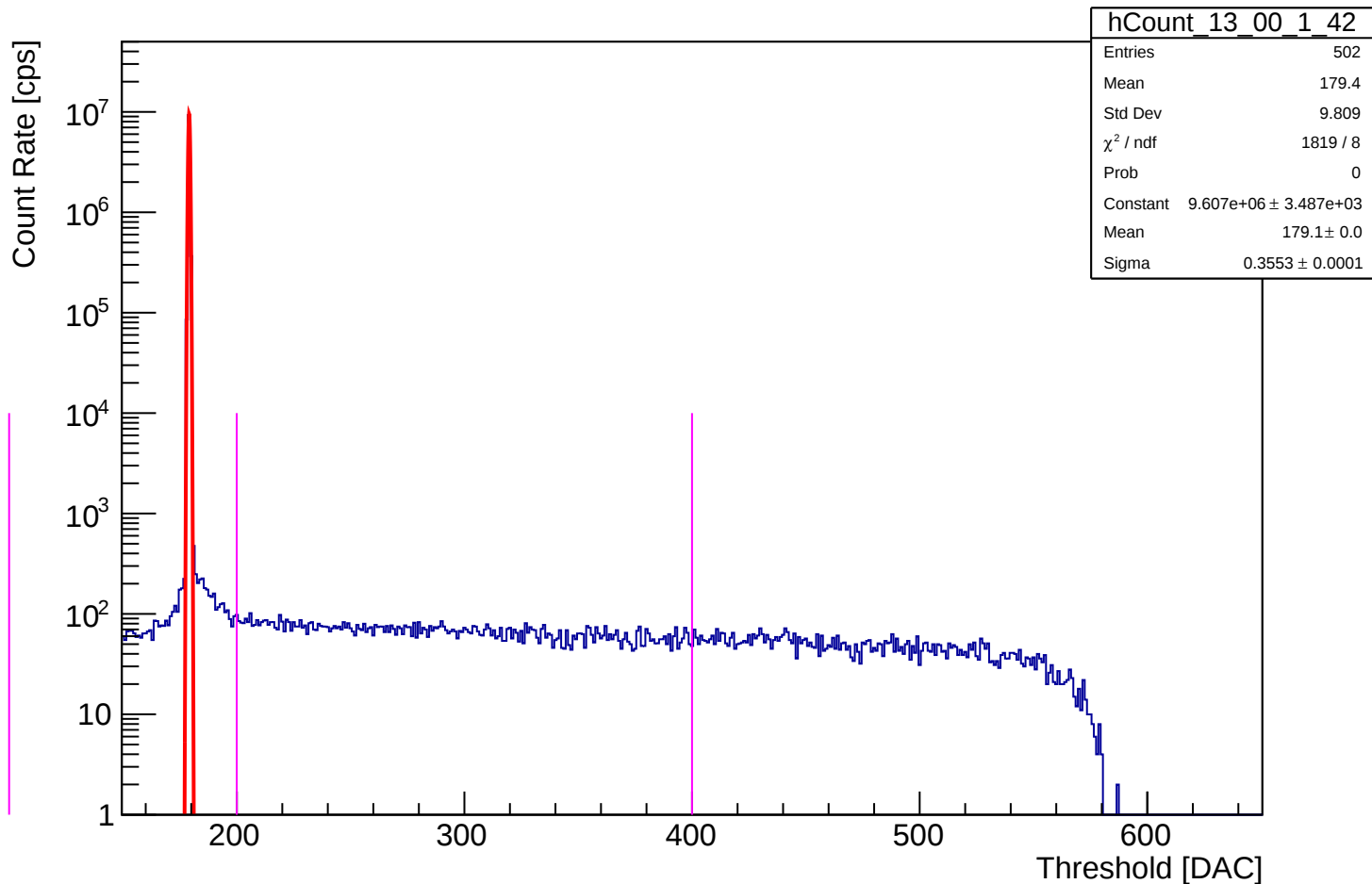
Row 1 Tile 1 Pmt 2 Pixel 20 Slot 13 Fiber 0 Asic 1 Channel 20



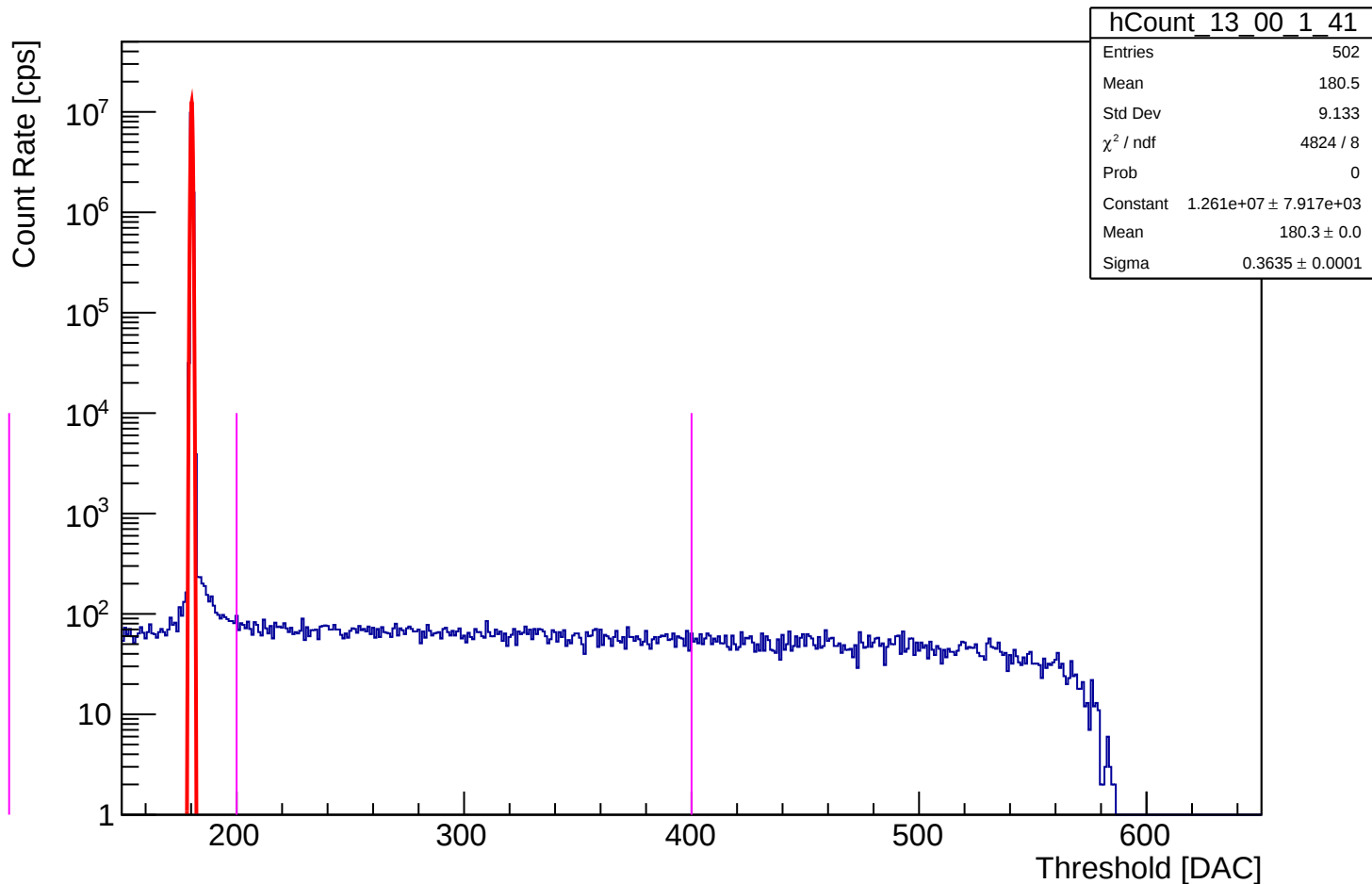
Row 1 Tile 1 Pmt 2 Pixel 21 Slot 13 Fiber 0 Asic 1 Channel 40



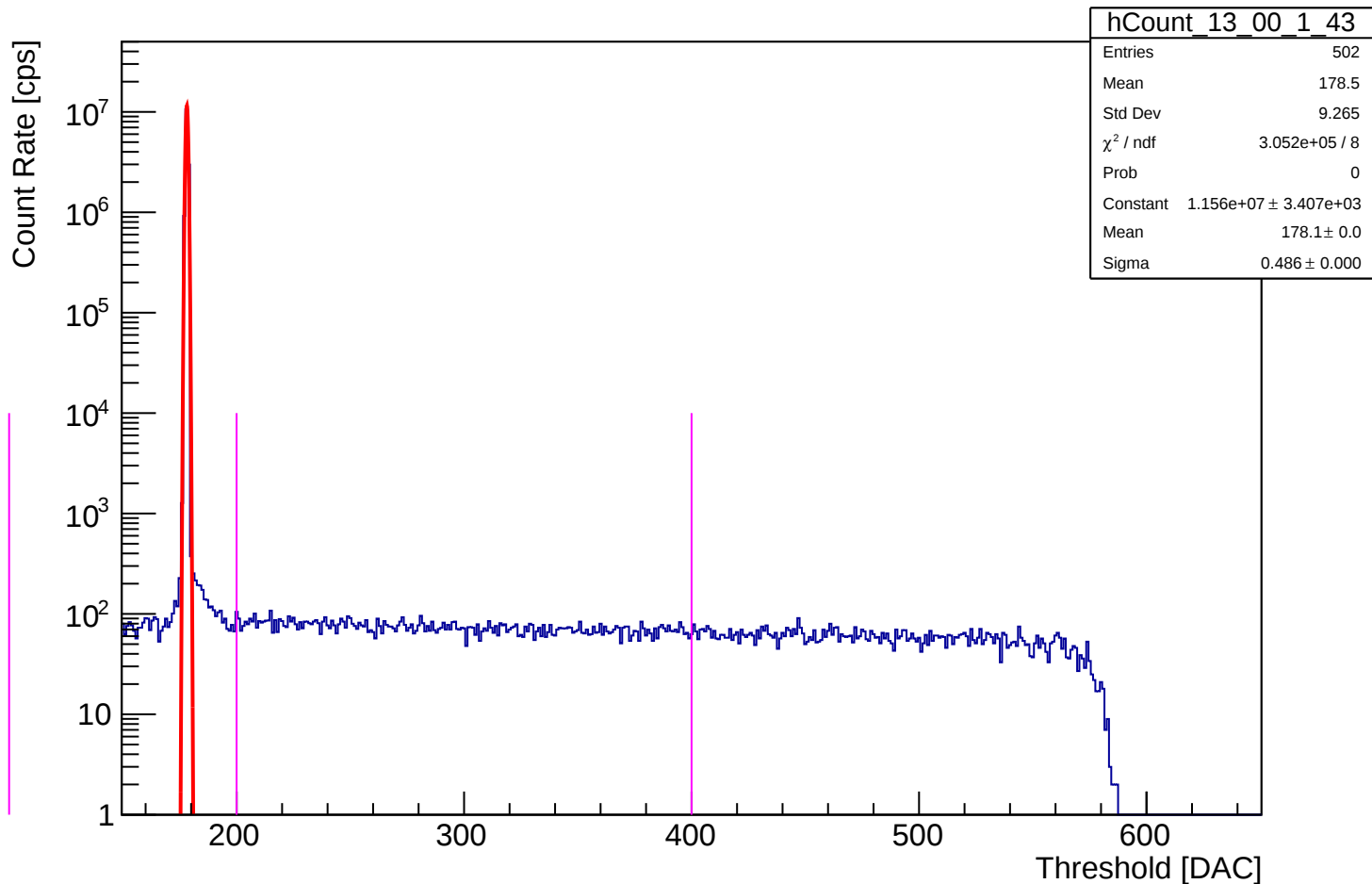
Row 1 Tile 1 Pmt 2 Pixel 22 Slot 13 Fiber 0 Asic 1 Channel 42



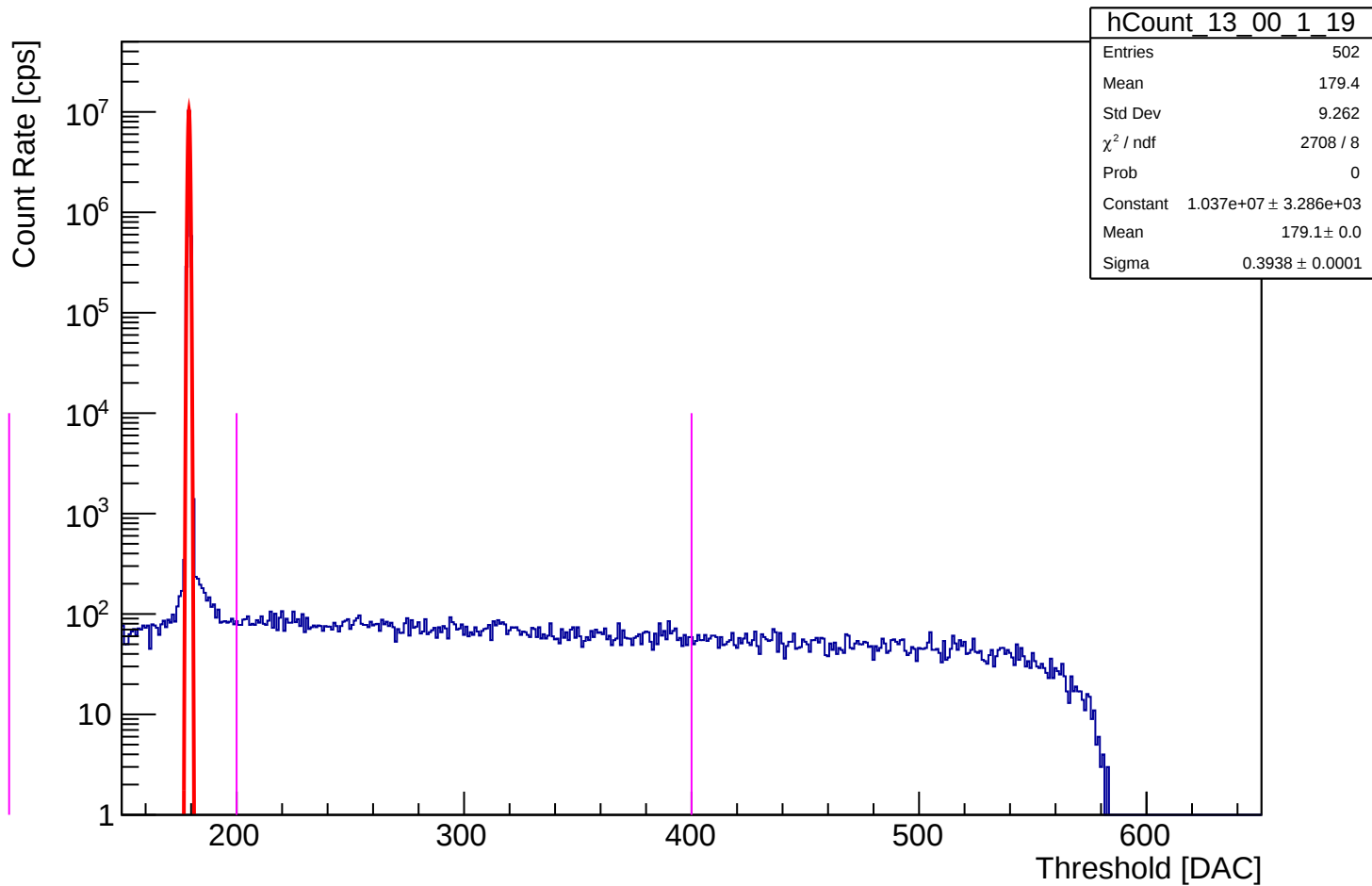
Row 1 Tile 1 Pmt 2 Pixel 23 Slot 13 Fiber 0 Asic 1 Channel 41



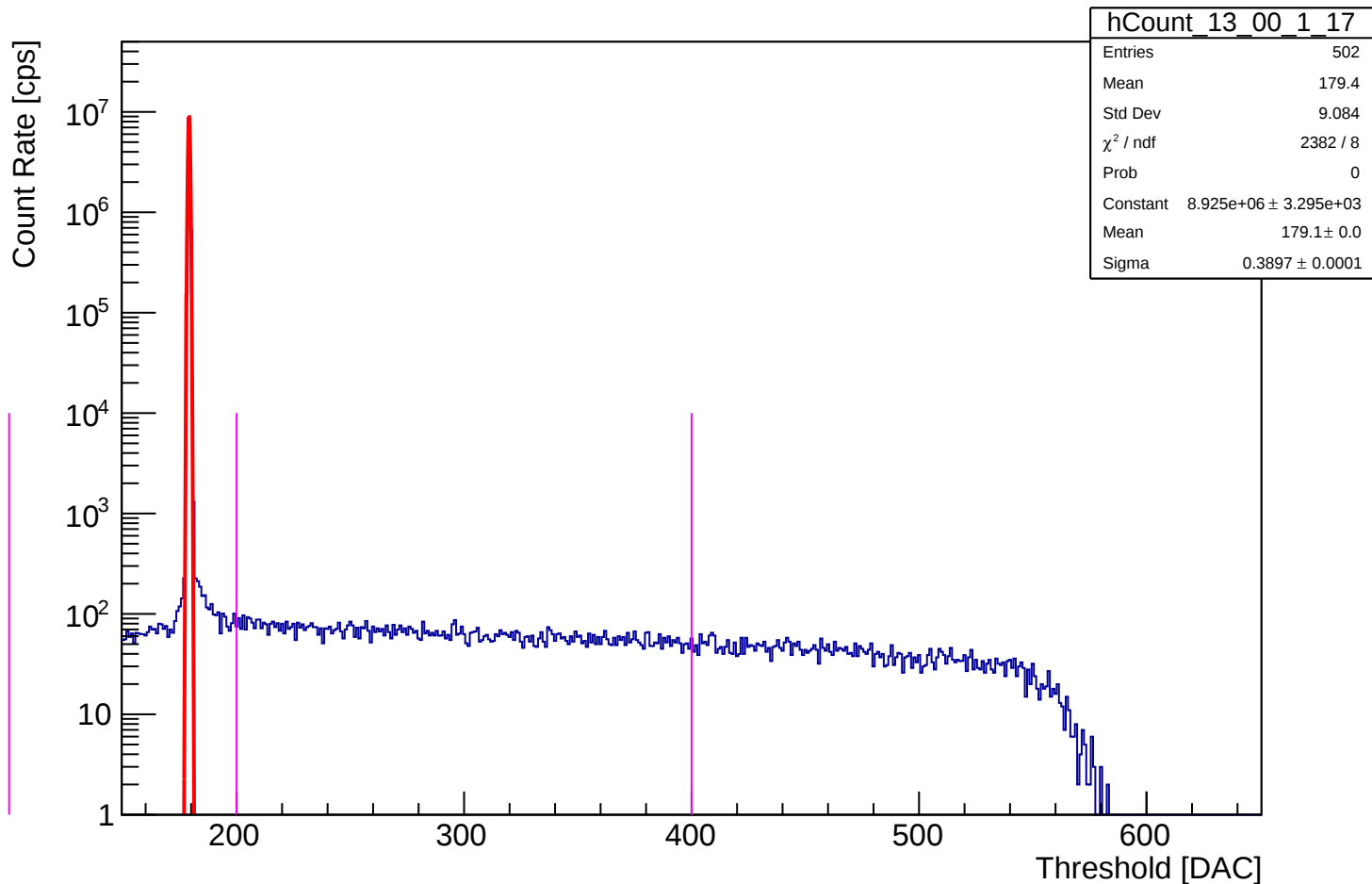
Row 1 Tile 1 Pmt 2 Pixel 24 Slot 13 Fiber 0 Asic 1 Channel 43



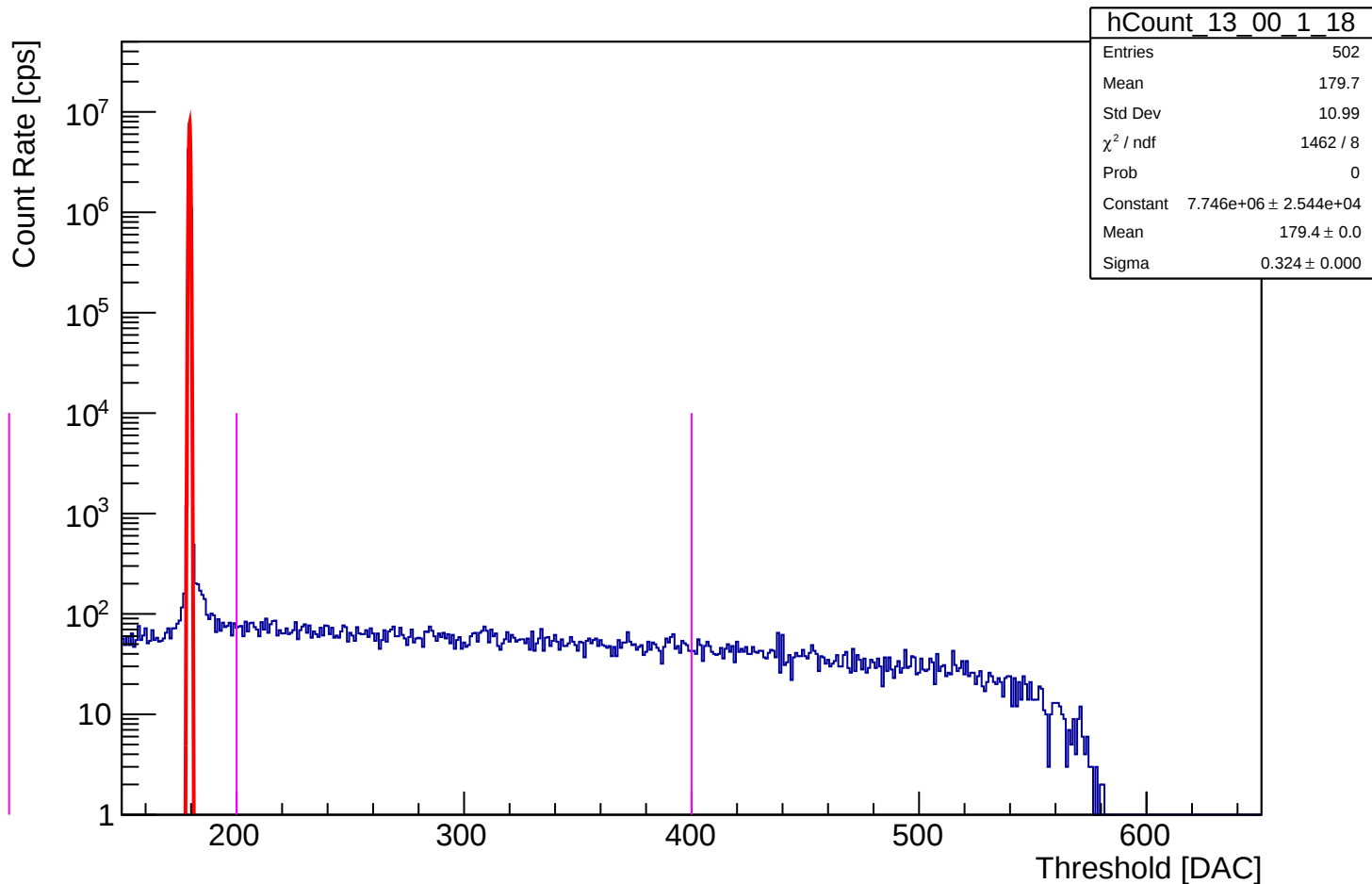
Row 1 Tile 1 Pmt 2 Pixel 25 Slot 13 Fiber 0 Asic 1 Channel 19



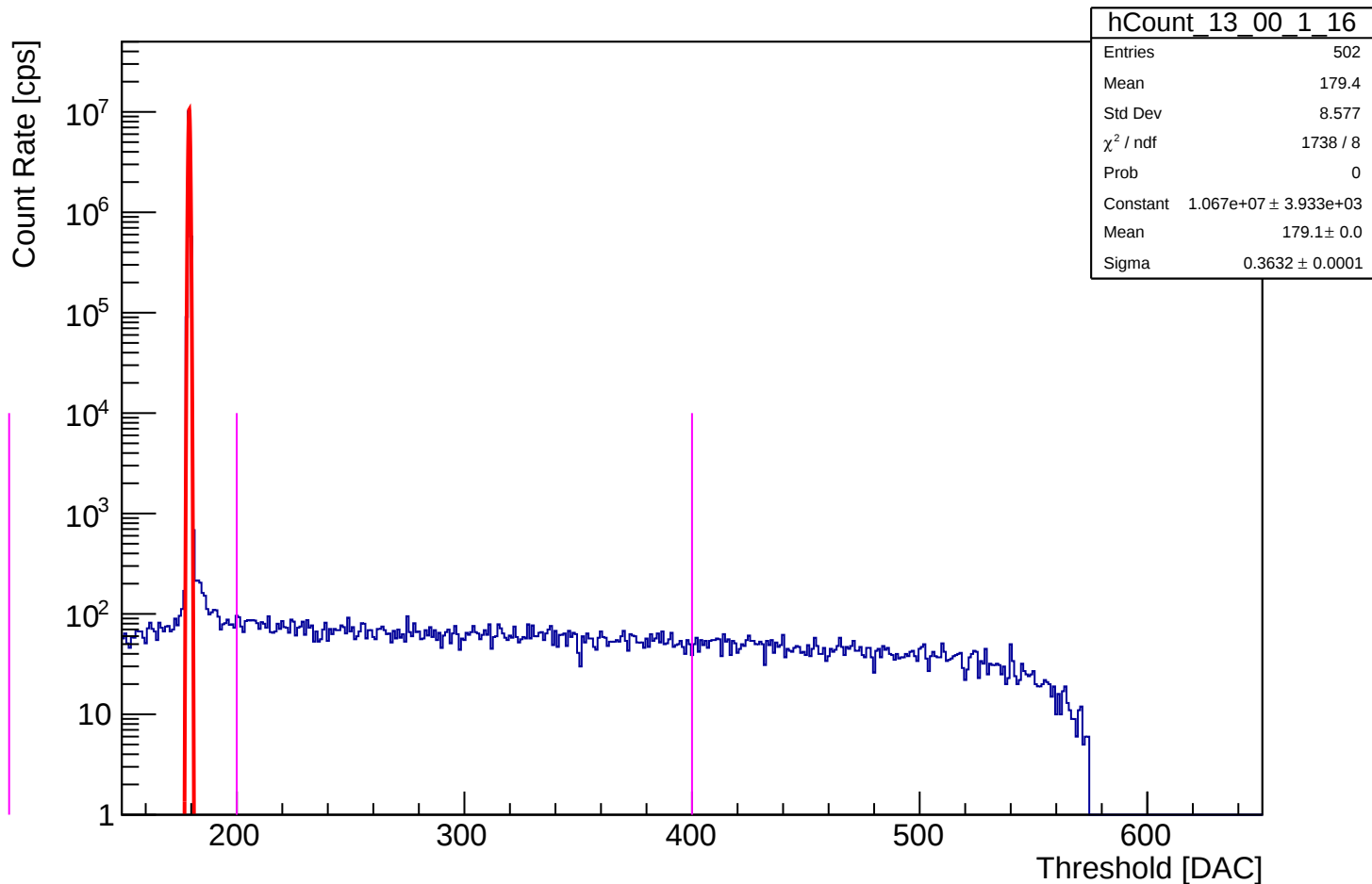
Row 1 Tile 1 Pmt 2 Pixel 26 Slot 13 Fiber 0 Asic 1 Channel 17



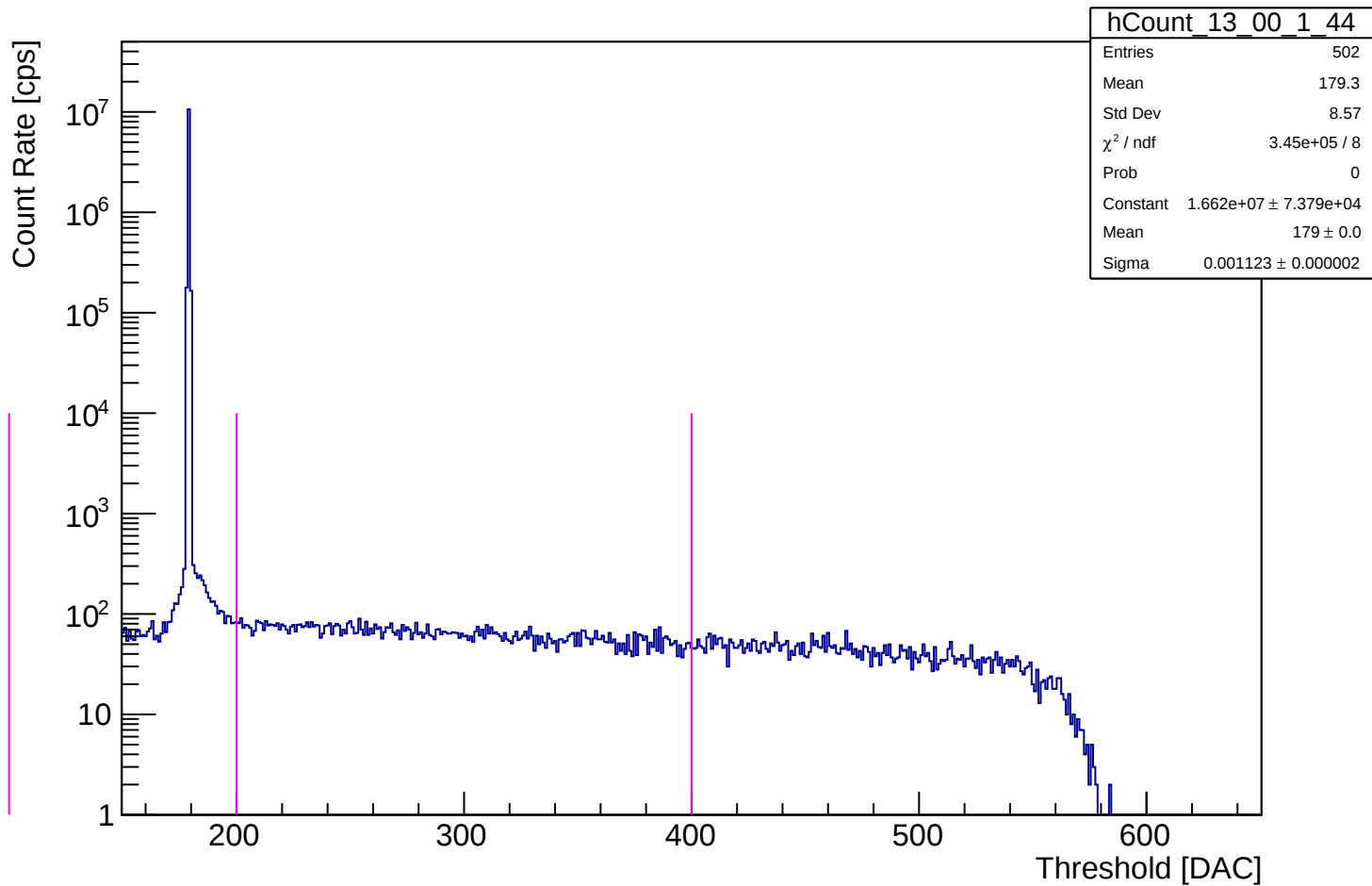
Row 1 Tile 1 Pmt 2 Pixel 27 Slot 13 Fiber 0 Asic 1 Channel 18



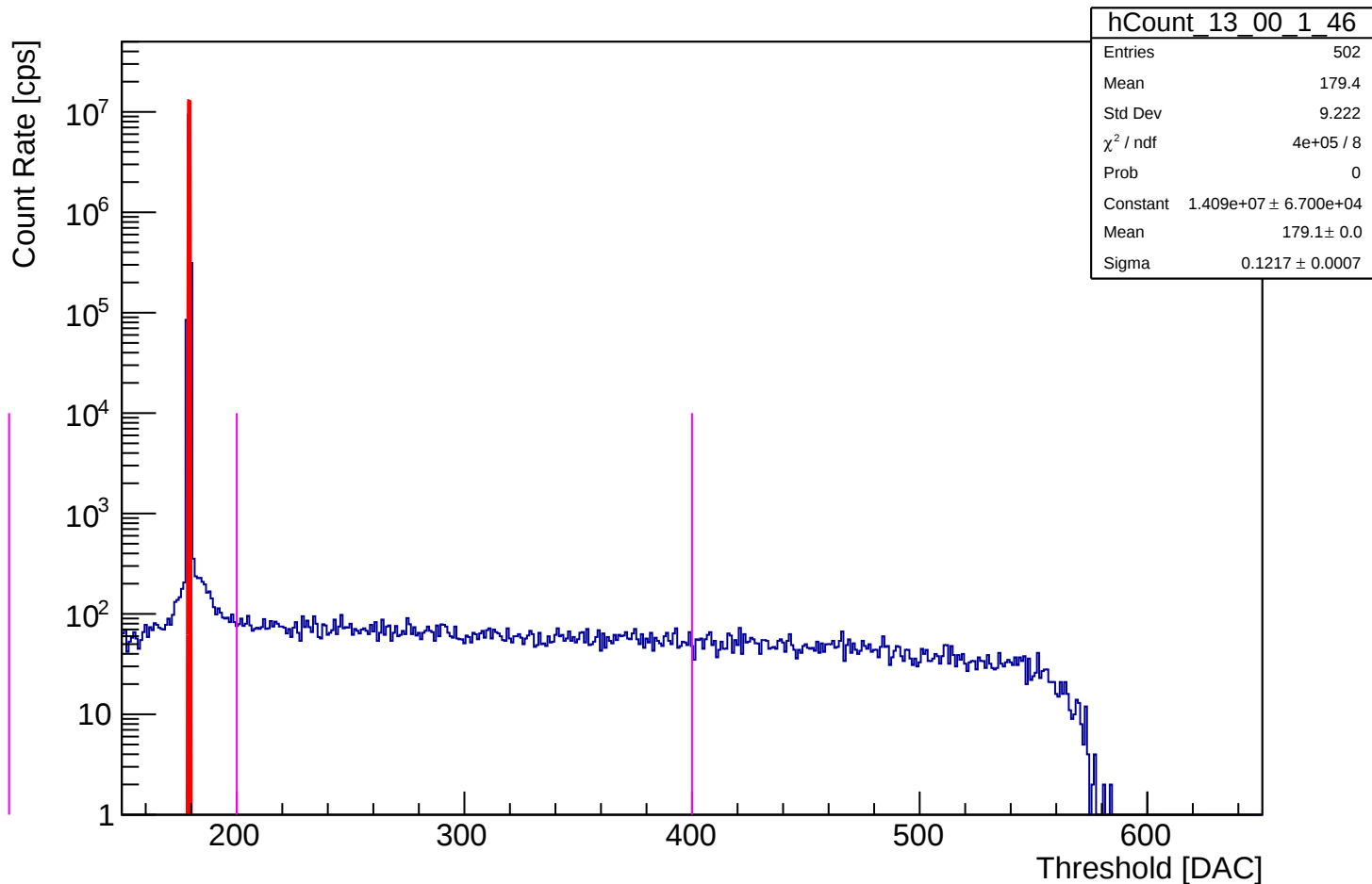
Row 1 Tile 1 Pmt 2 Pixel 28 Slot 13 Fiber 0 Asic 1 Channel 16



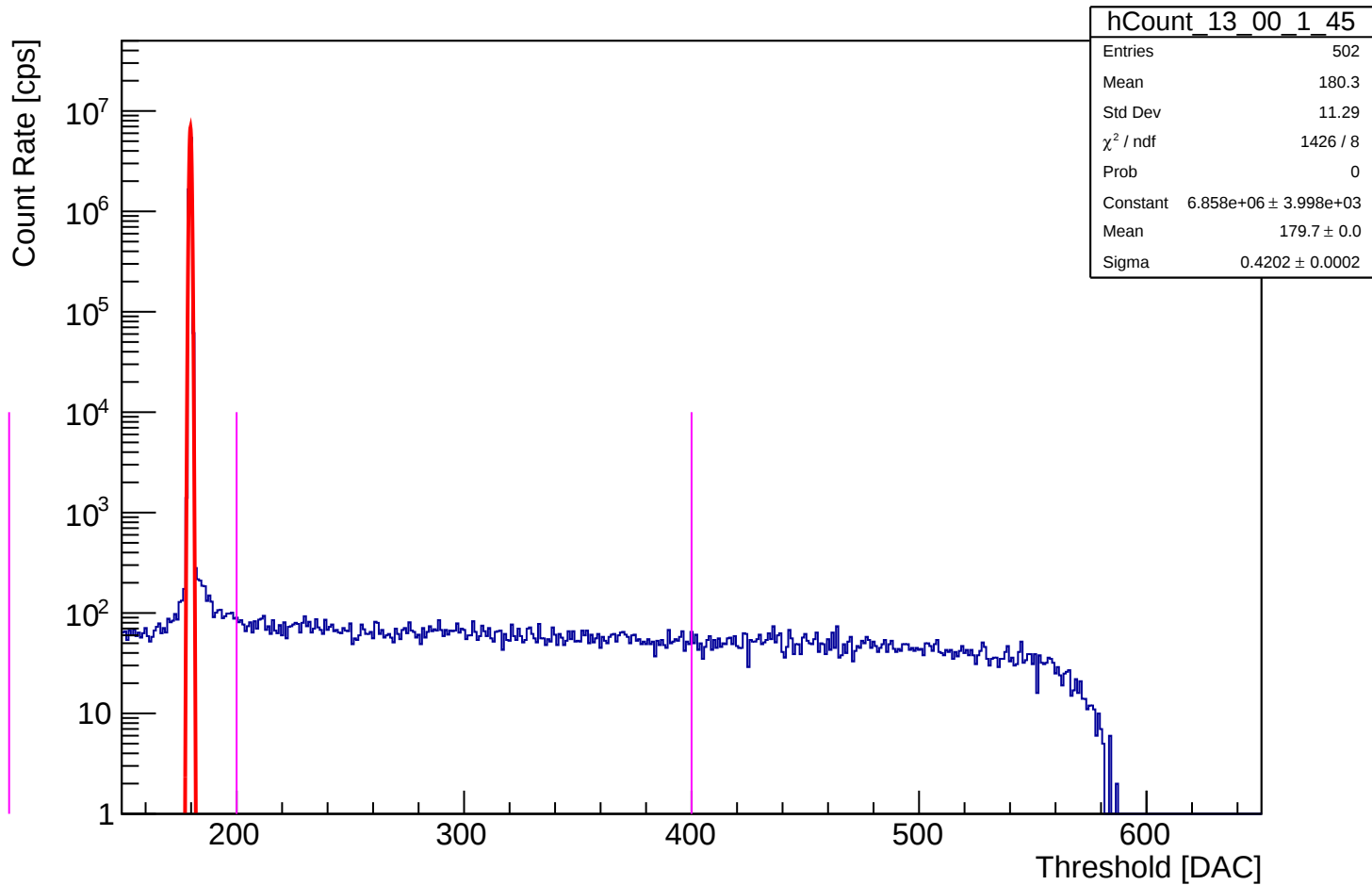
Row 1 Tile 1 Pmt 2 Pixel 29 Slot 13 Fiber 0 Asic 1 Channel 44



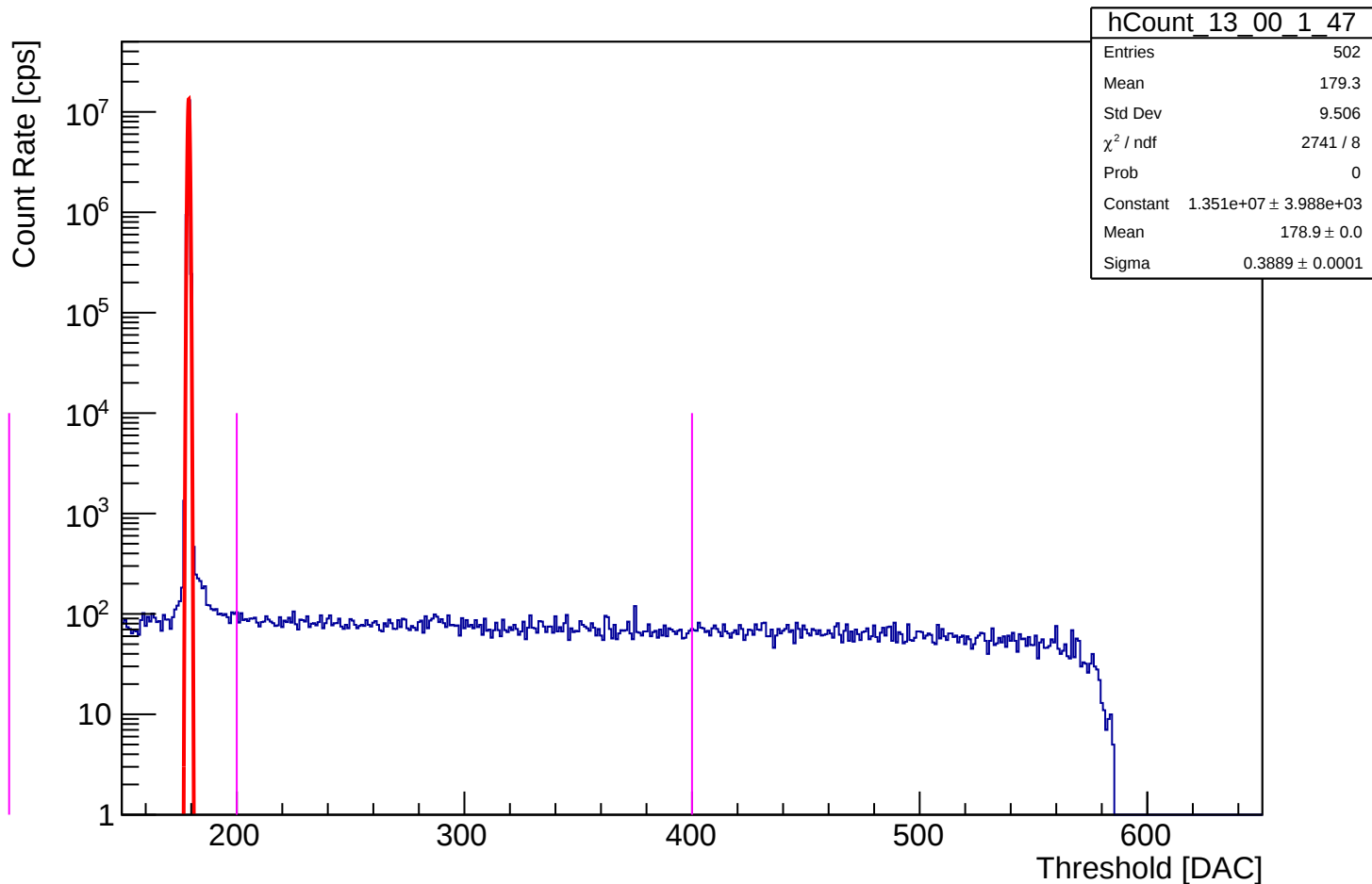
Row 1 Tile 1 Pmt 2 Pixel 30 Slot 13 Fiber 0 Asic 1 Channel 46



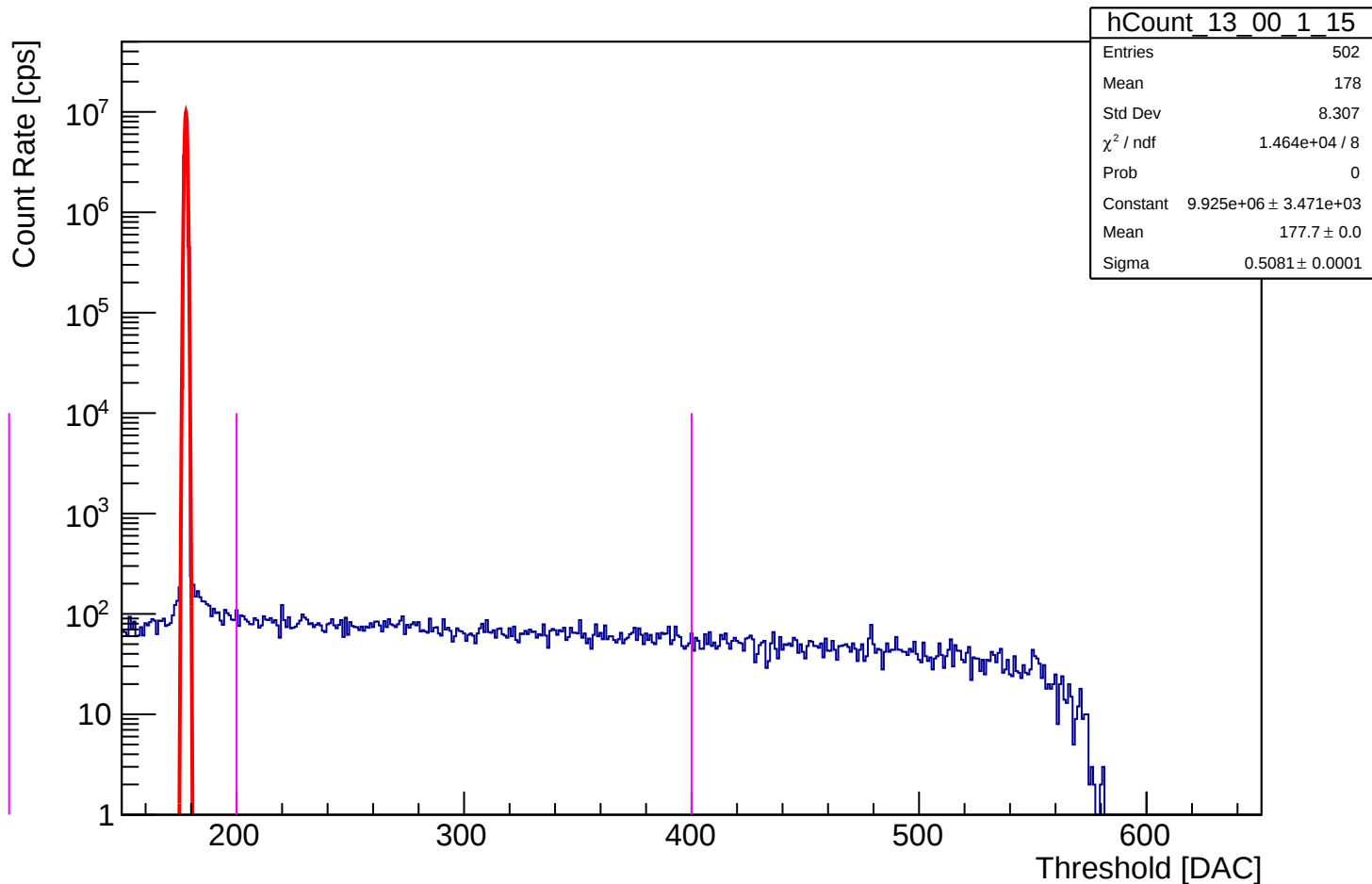
Row 1 Tile 1 Pmt 2 Pixel 31 Slot 13 Fiber 0 Asic 1 Channel 45



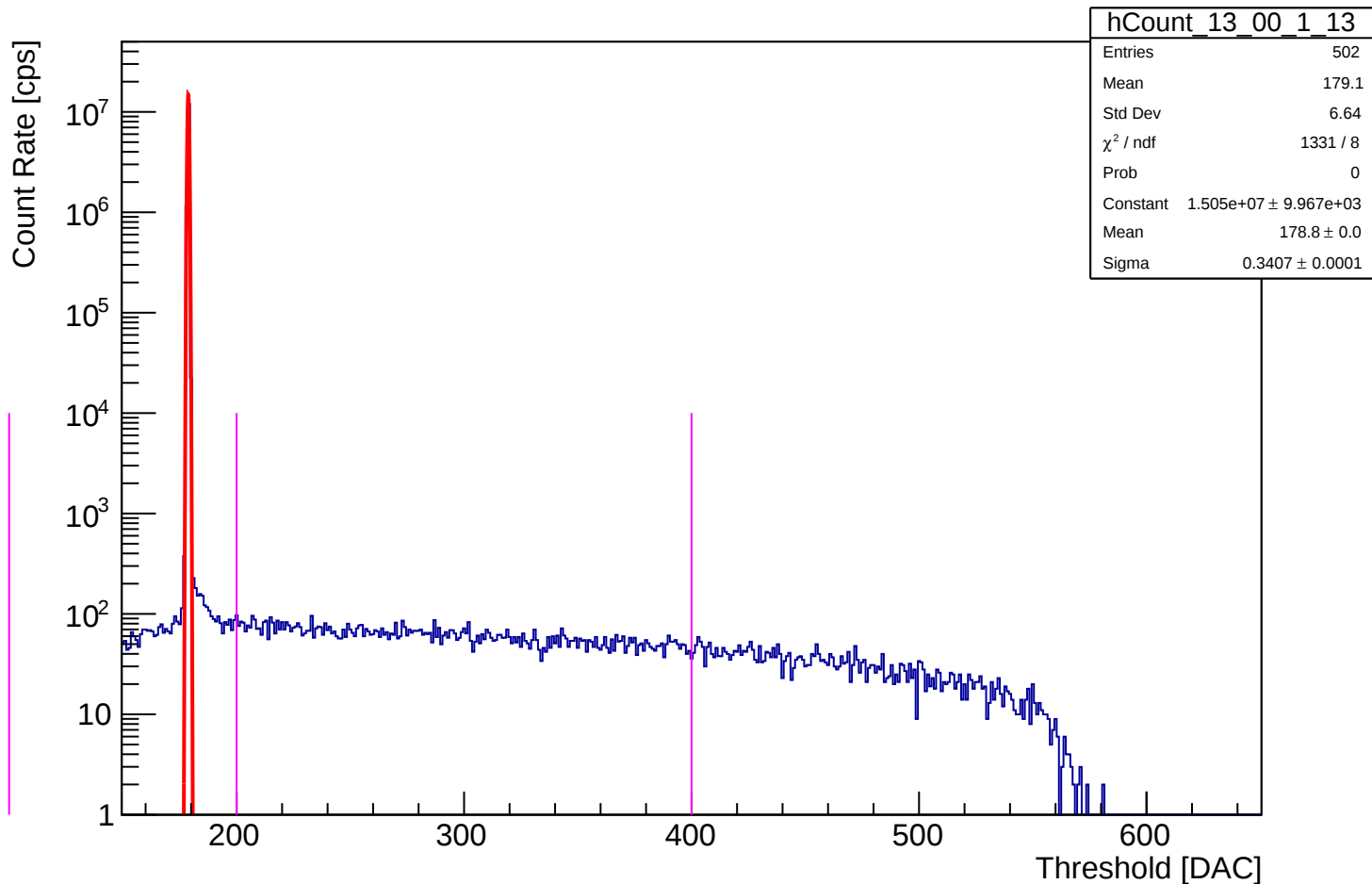
Row 1 Tile 1 Pmt 2 Pixel 32 Slot 13 Fiber 0 Asic 1 Channel 47



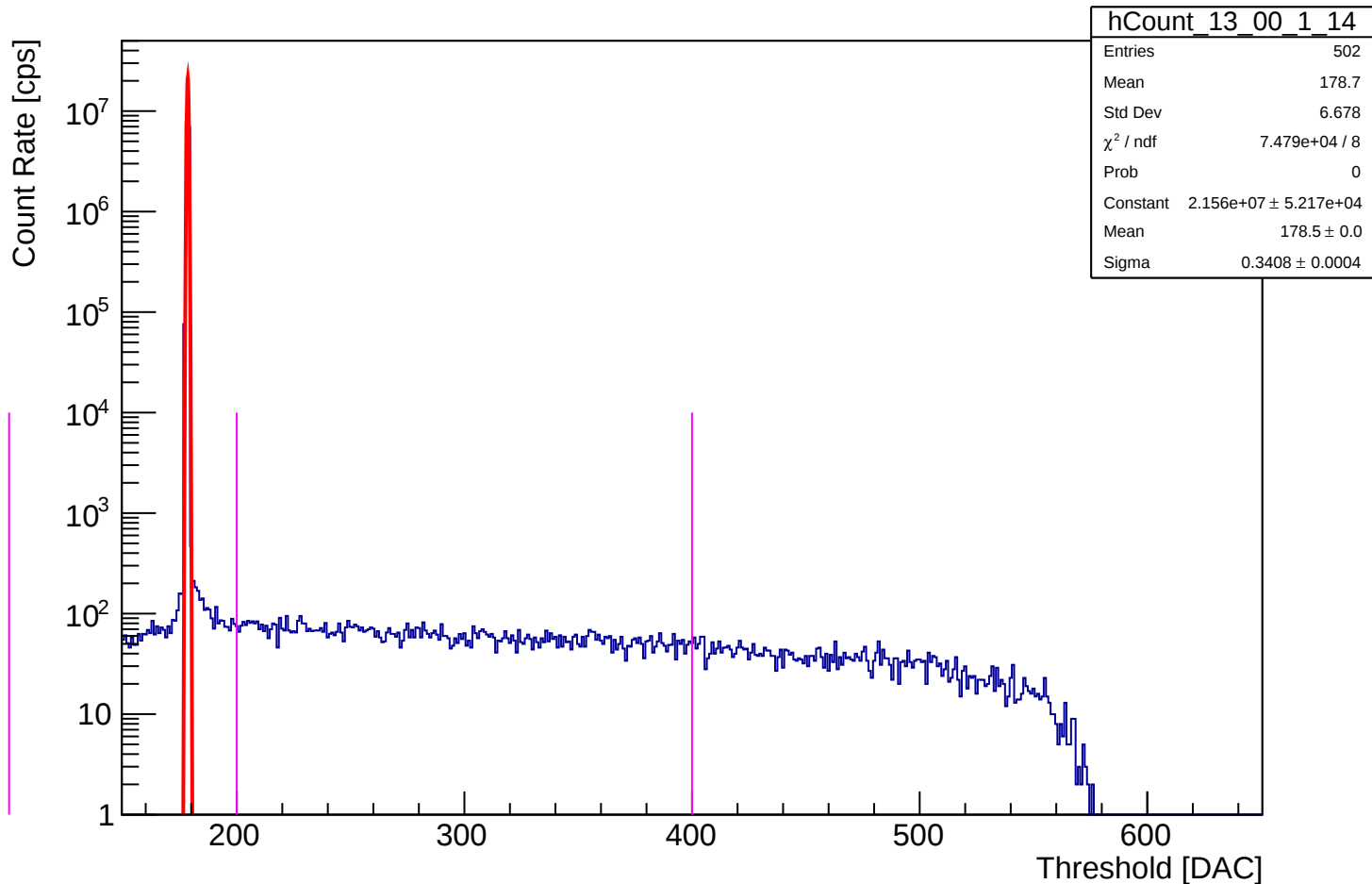
Row 1 Tile 1 Pmt 2 Pixel 33 Slot 13 Fiber 0 Asic 1 Channel 15



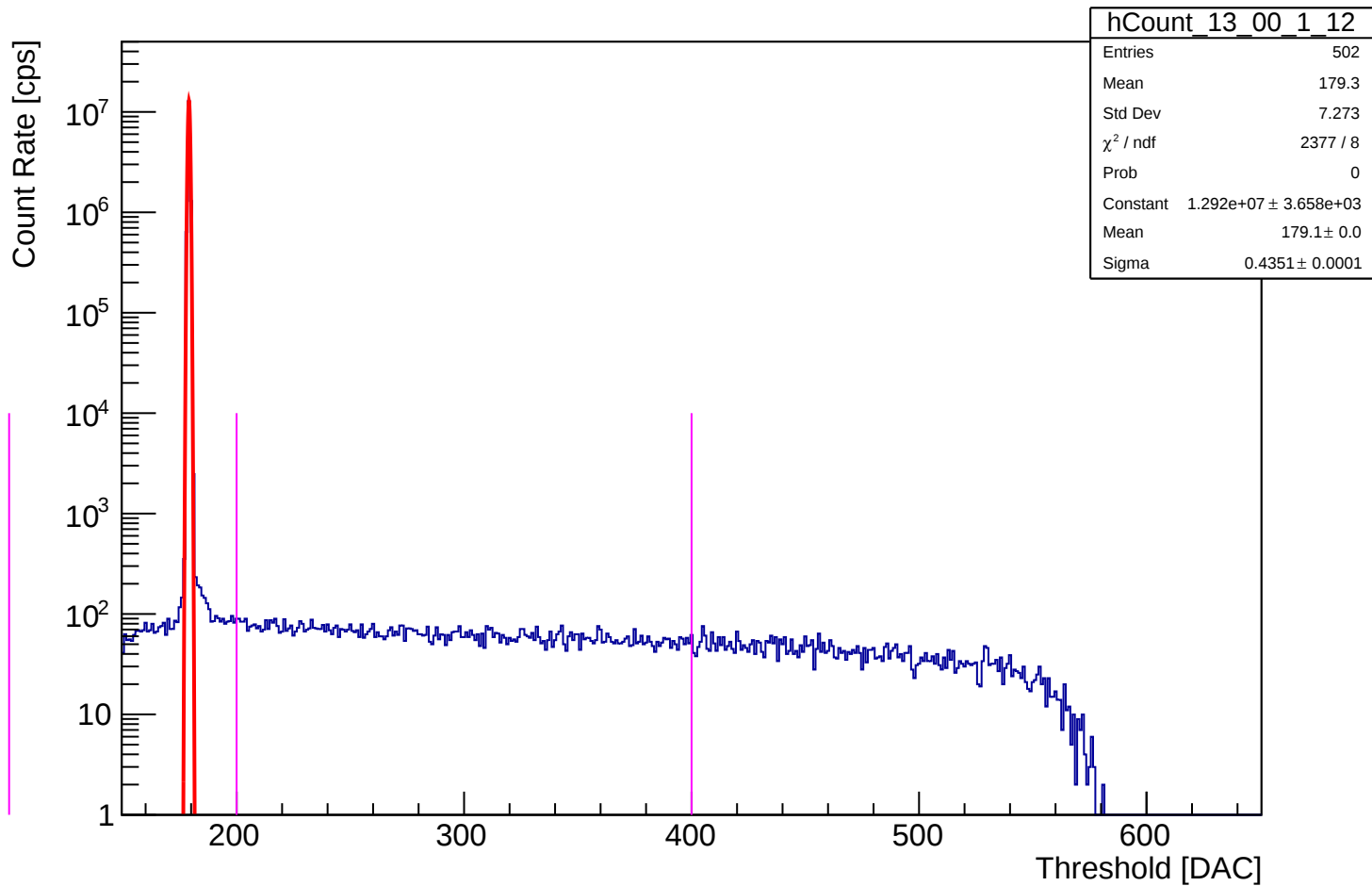
Row 1 Tile 1 Pmt 2 Pixel 34 Slot 13 Fiber 0 Asic 1 Channel 13



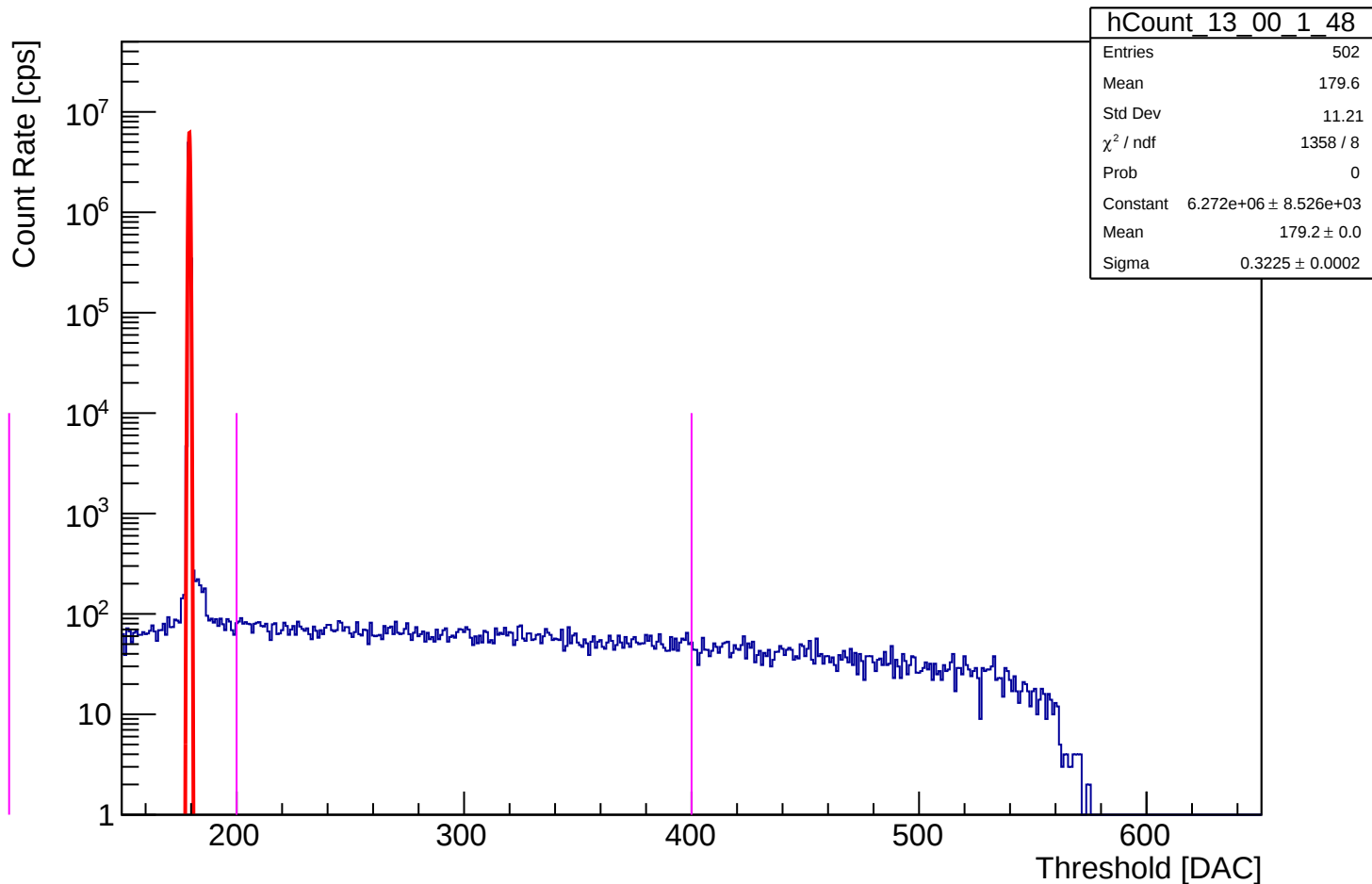
Row 1 Tile 1 Pmt 2 Pixel 35 Slot 13 Fiber 0 Asic 1 Channel 14



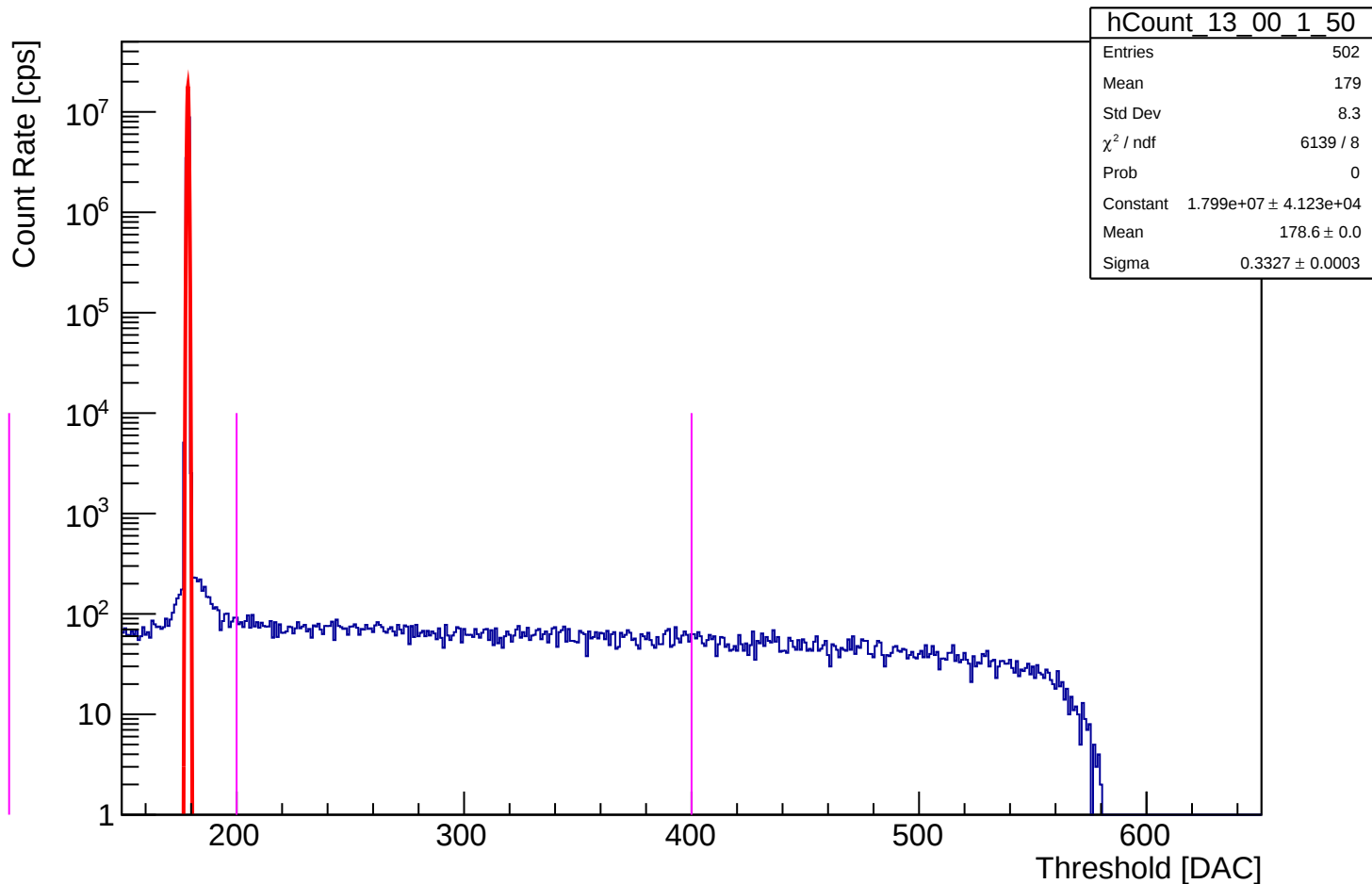
Row 1 Tile 1 Pmt 2 Pixel 36 Slot 13 Fiber 0 Asic 1 Channel 12



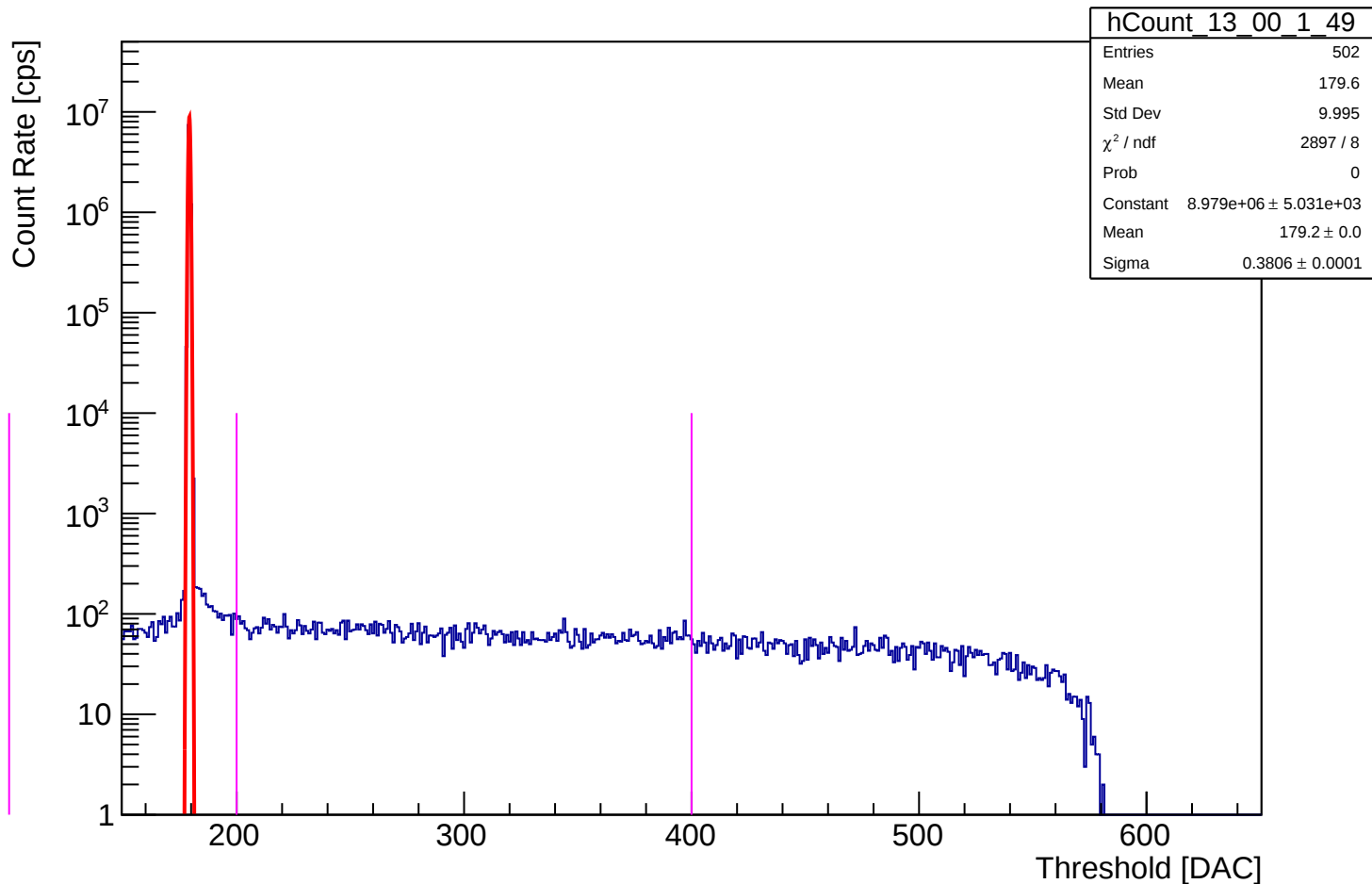
Row 1 Tile 1 Pmt 2 Pixel 37 Slot 13 Fiber 0 Asic 1 Channel 48

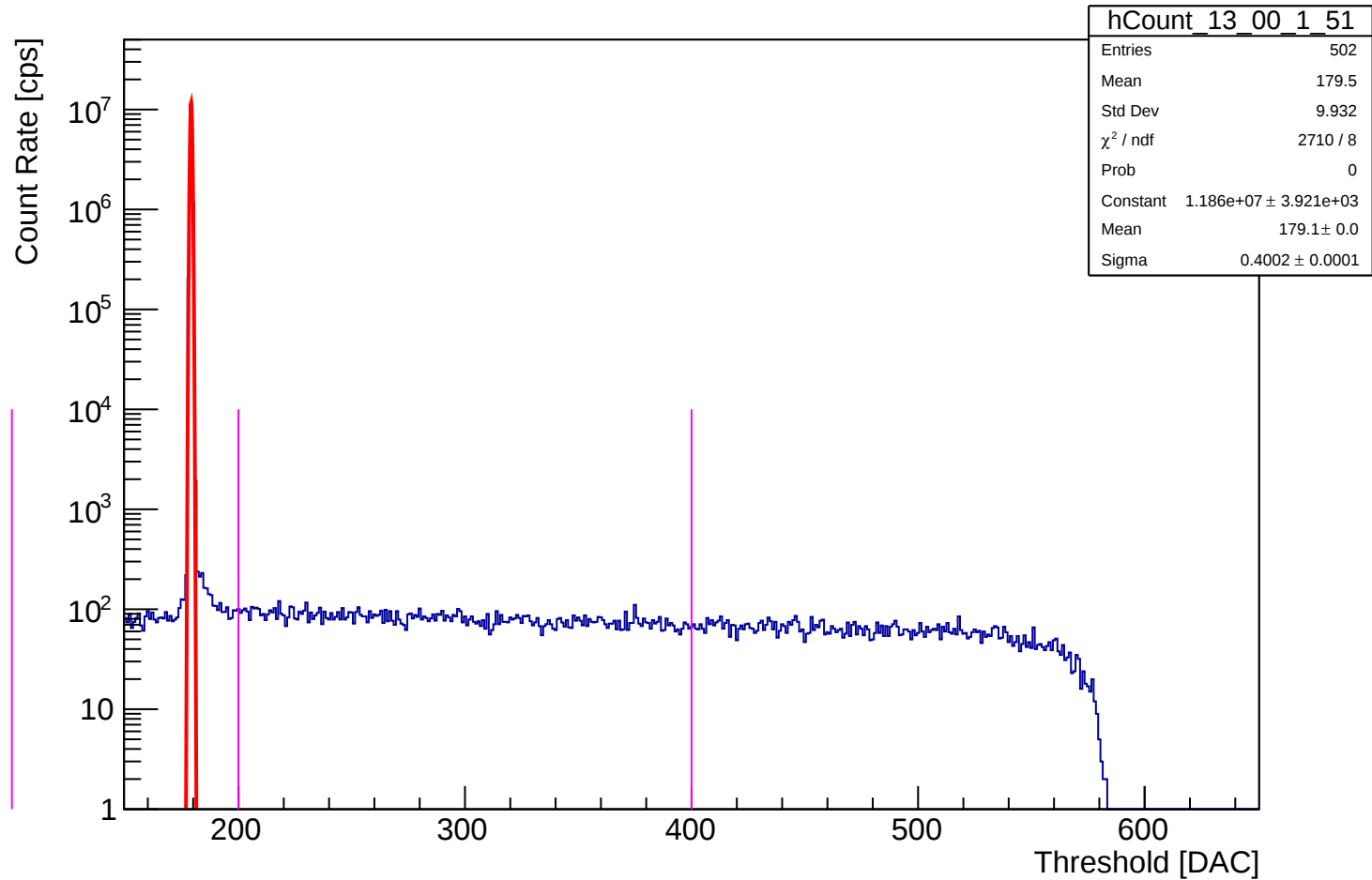


Row 1 Tile 1 Pmt 2 Pixel 38 Slot 13 Fiber 0 Asic 1 Channel 50

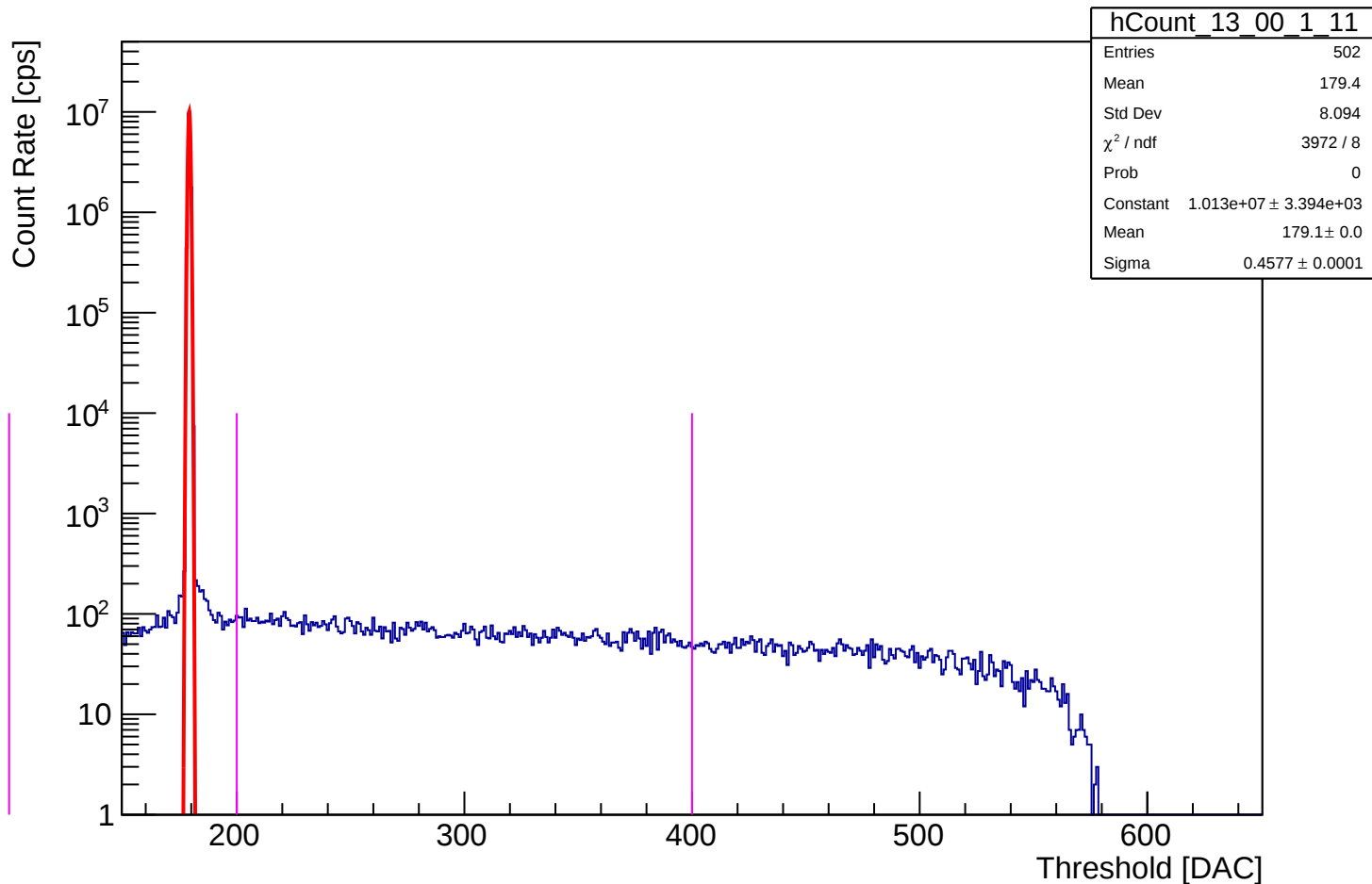


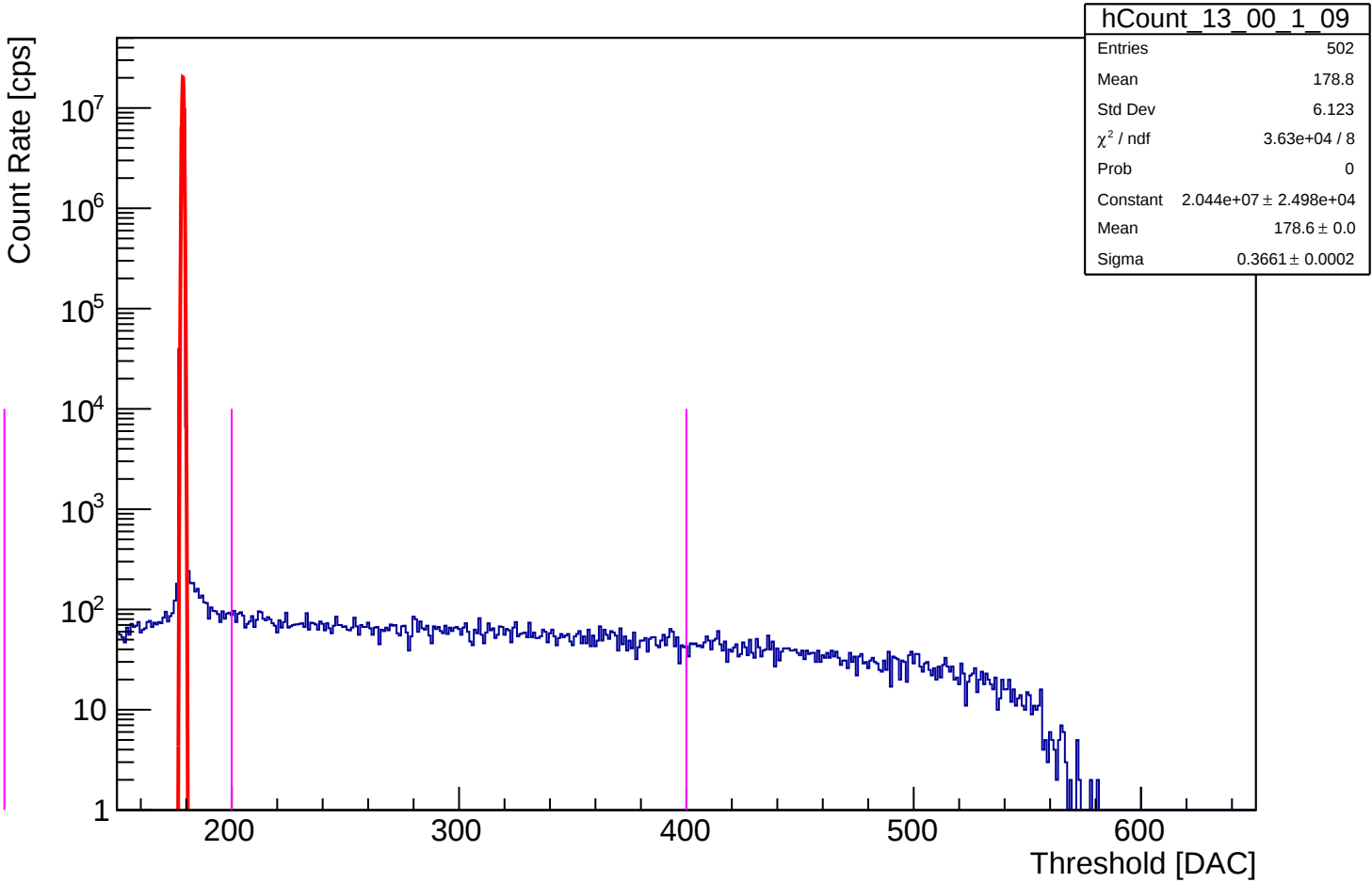
Row 1 Tile 1 Pmt 2 Pixel 39 Slot 13 Fiber 0 Asic 1 Channel 49



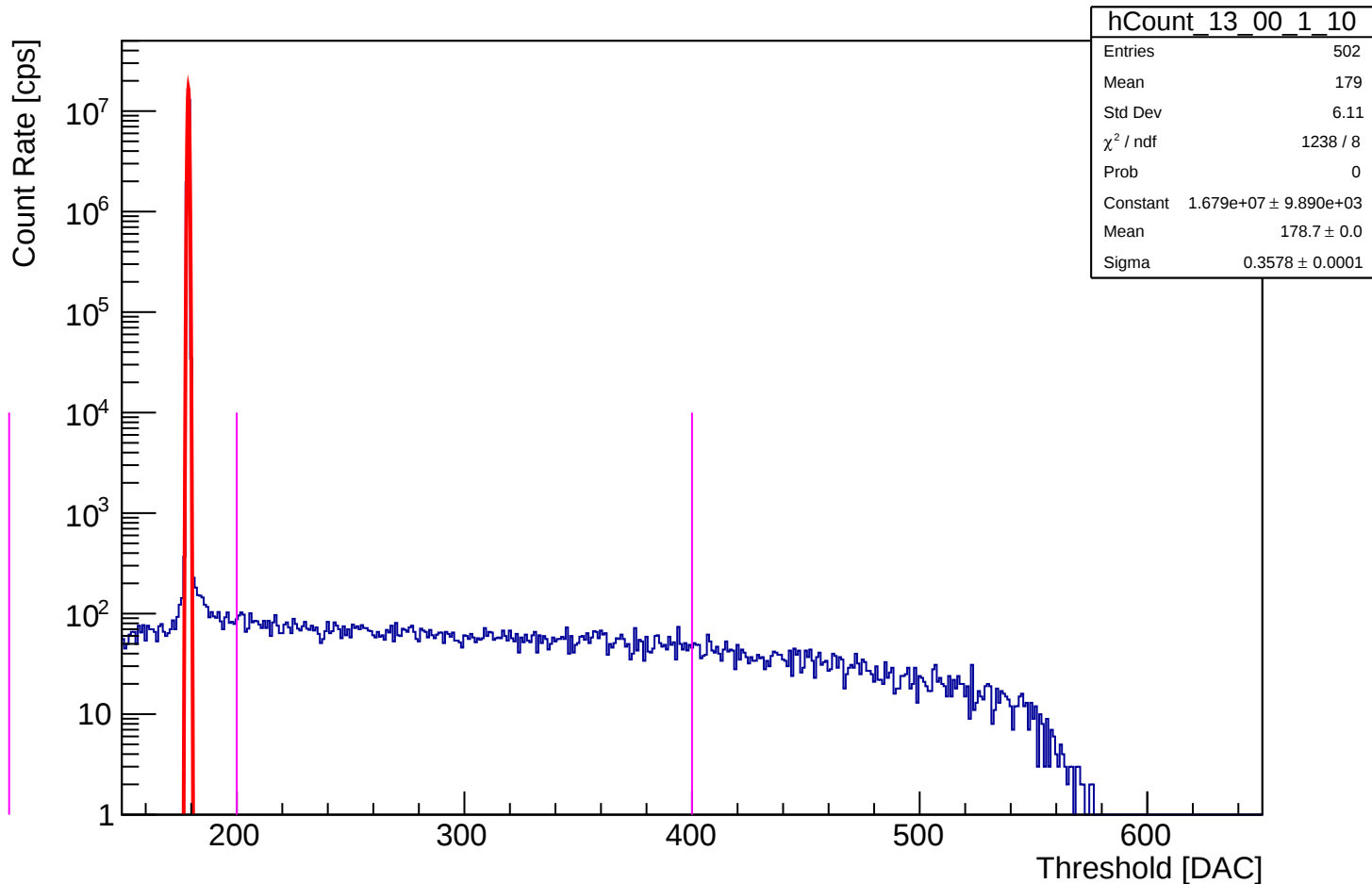


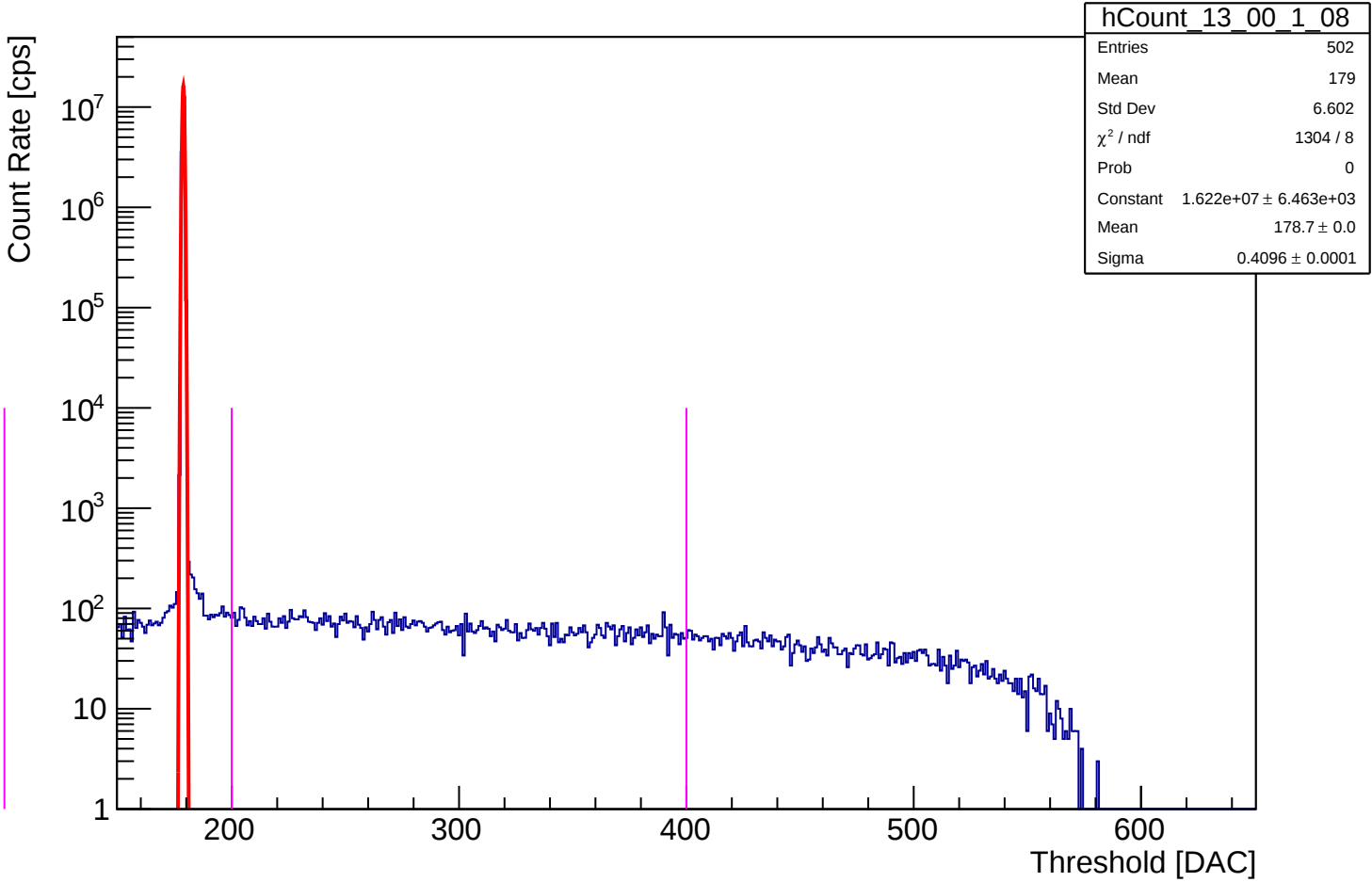
Row 1 Tile 1 Pmt 2 Pixel 41 Slot 13 Fiber 0 Asic 1 Channel 11



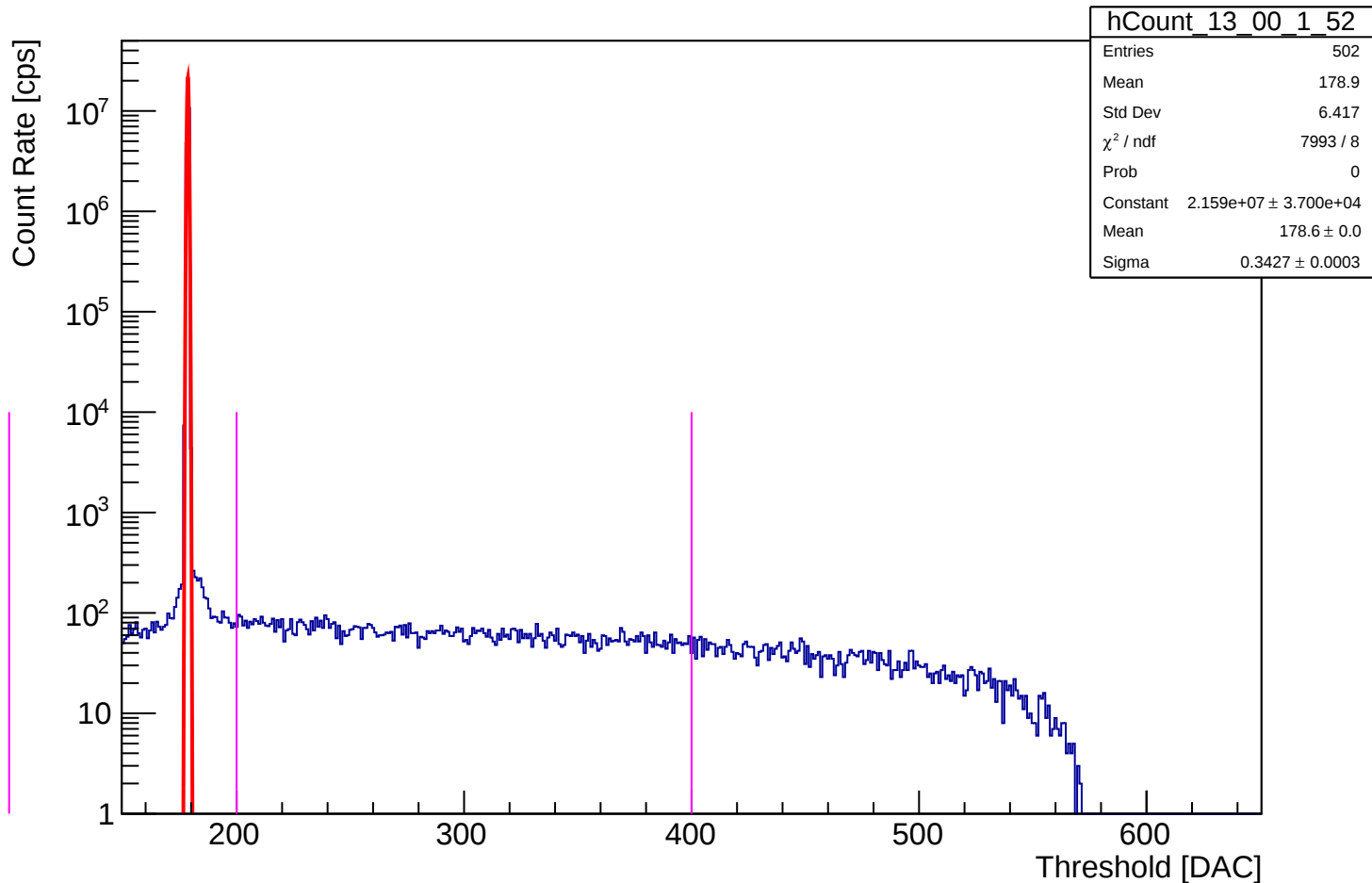


Row 1 Tile 1 Pmt 2 Pixel 43 Slot 13 Fiber 0 Asic 1 Channel 10

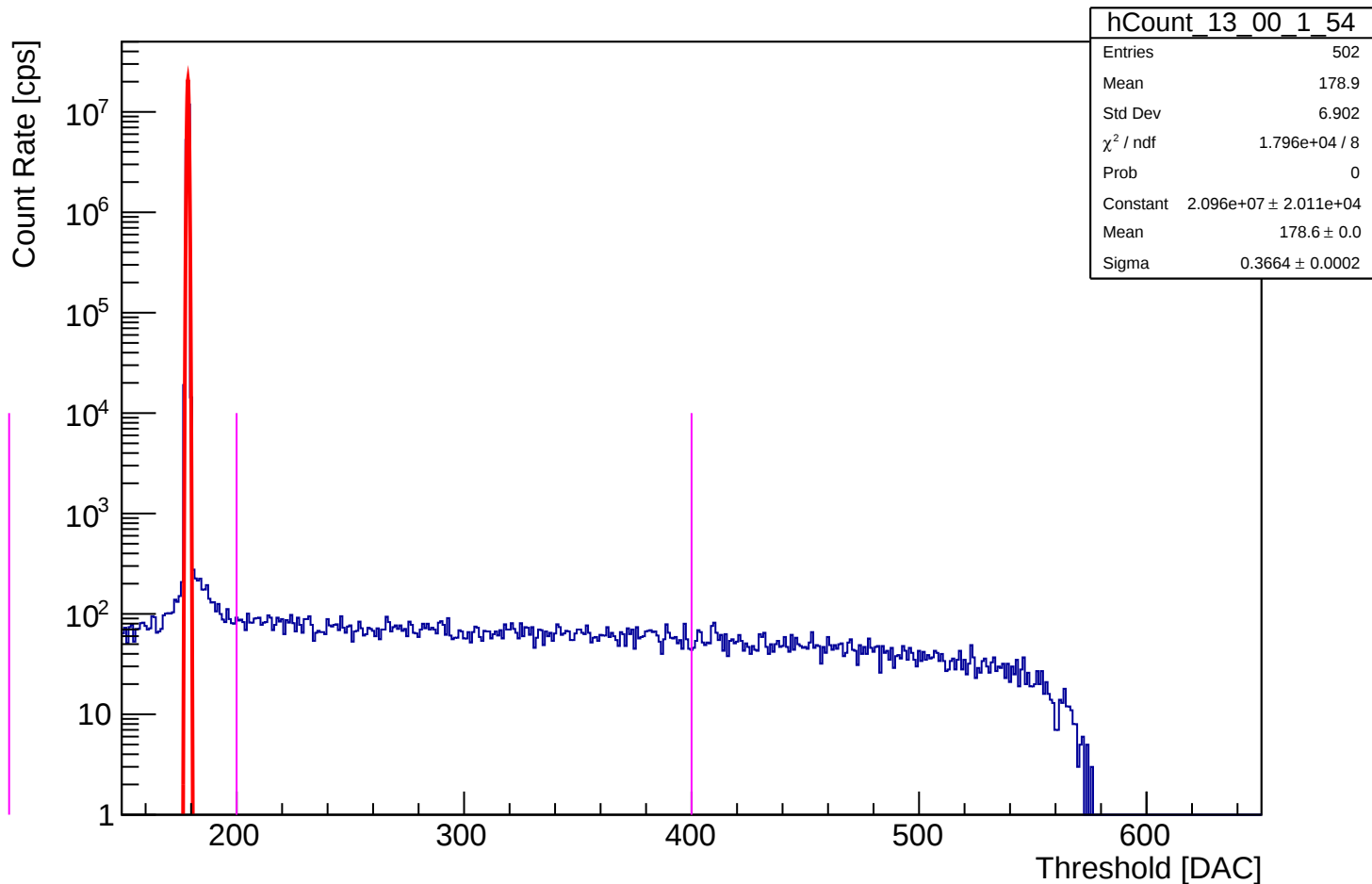




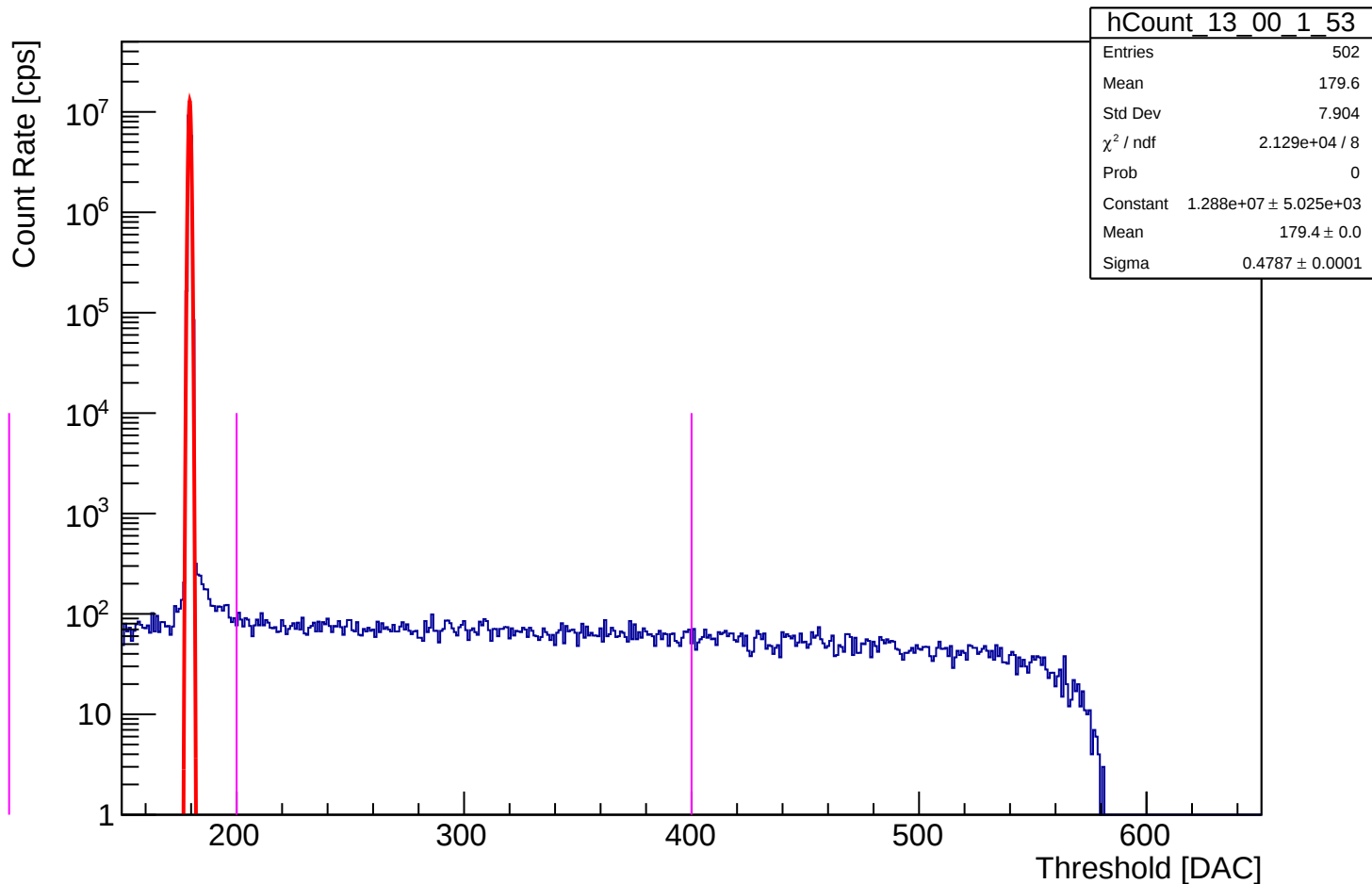
Row 1 Tile 1 Pmt 2 Pixel 45 Slot 13 Fiber 0 Asic 1 Channel 52



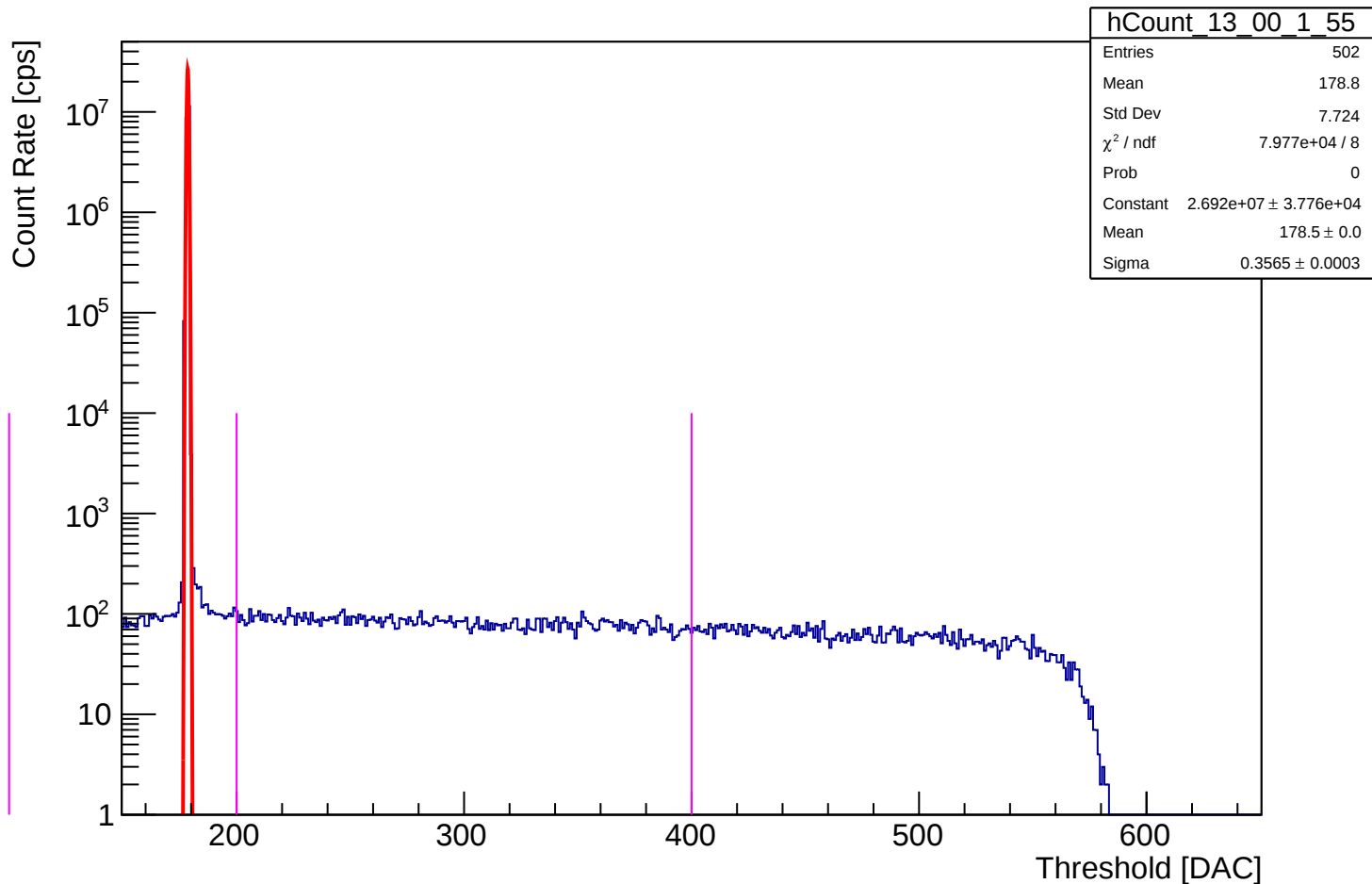
Row 1 Tile 1 Pmt 2 Pixel 46 Slot 13 Fiber 0 Asic 1 Channel 54



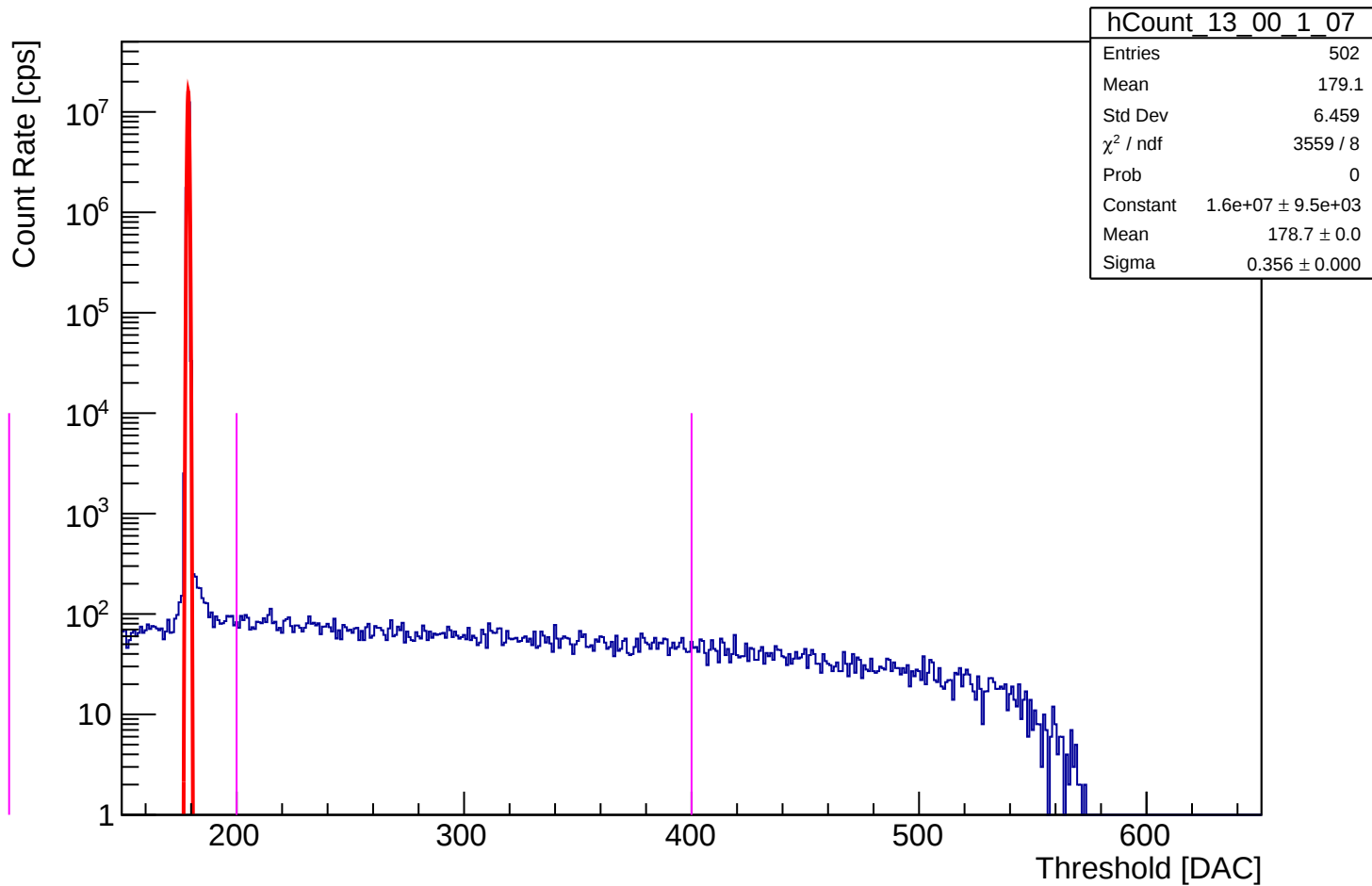
Row 1 Tile 1 Pmt 2 Pixel 47 Slot 13 Fiber 0 Asic 1 Channel 53

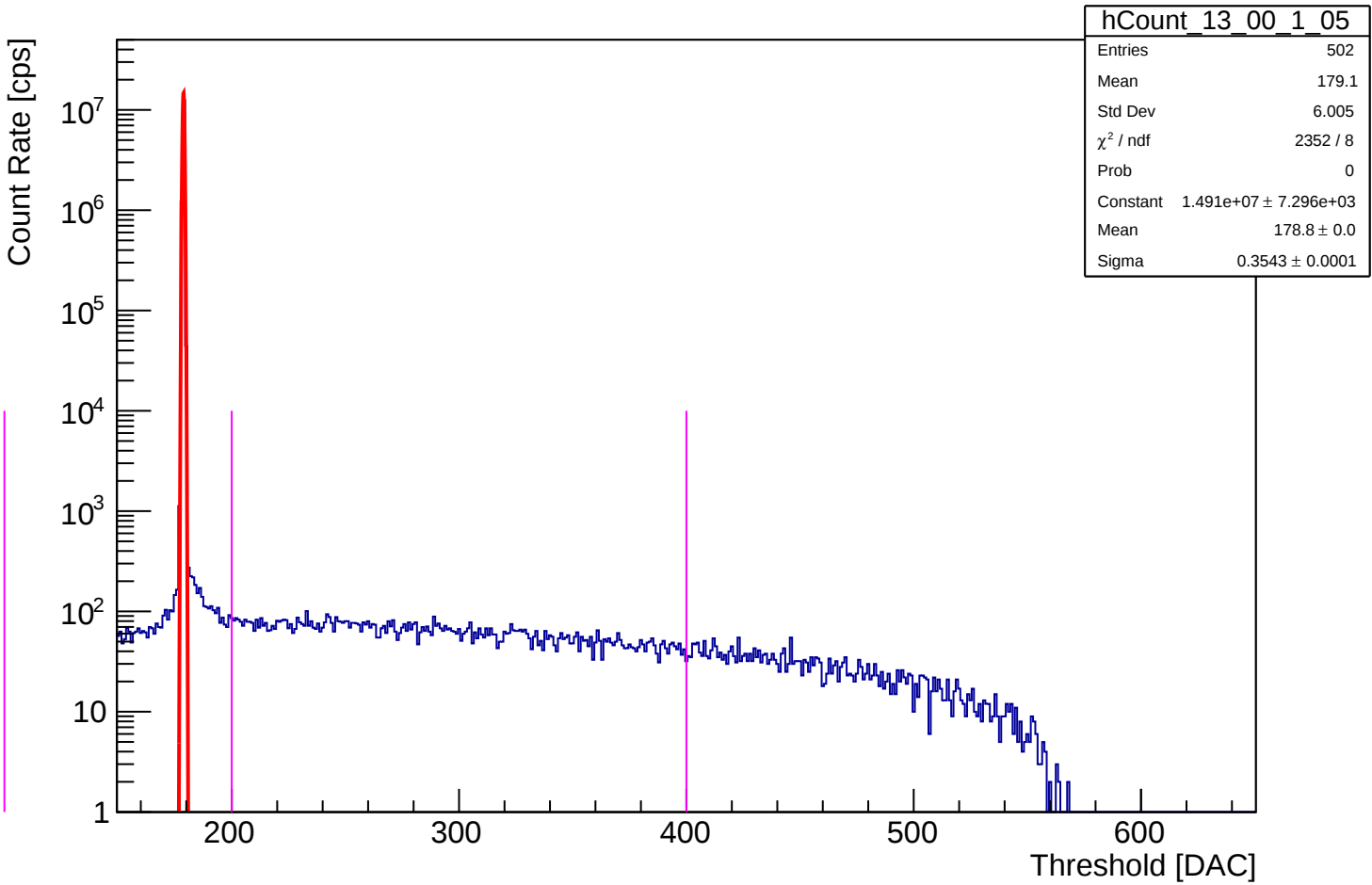


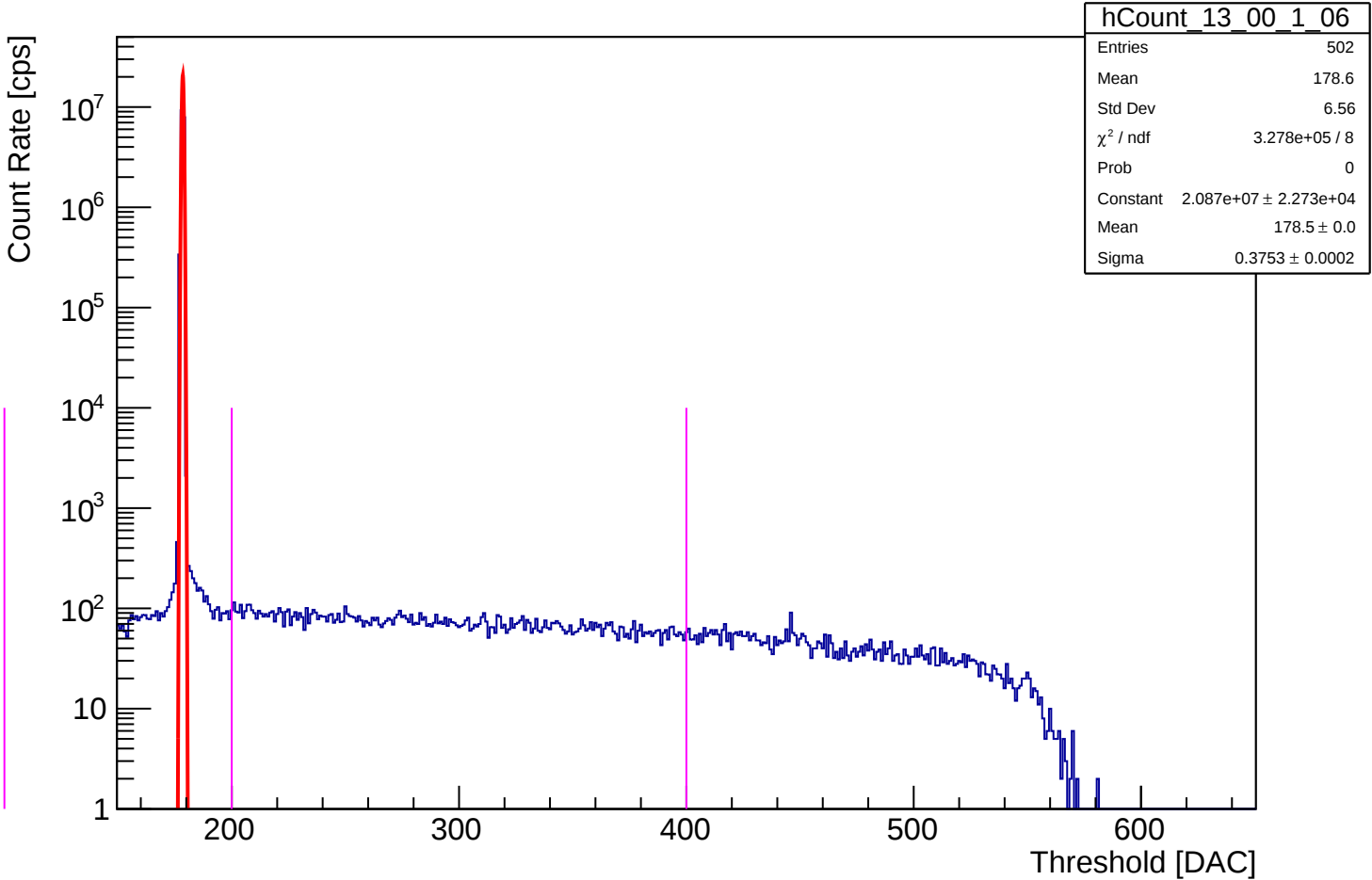
Row 1 Tile 1 Pmt 2 Pixel 48 Slot 13 Fiber 0 Asic 1 Channel 55

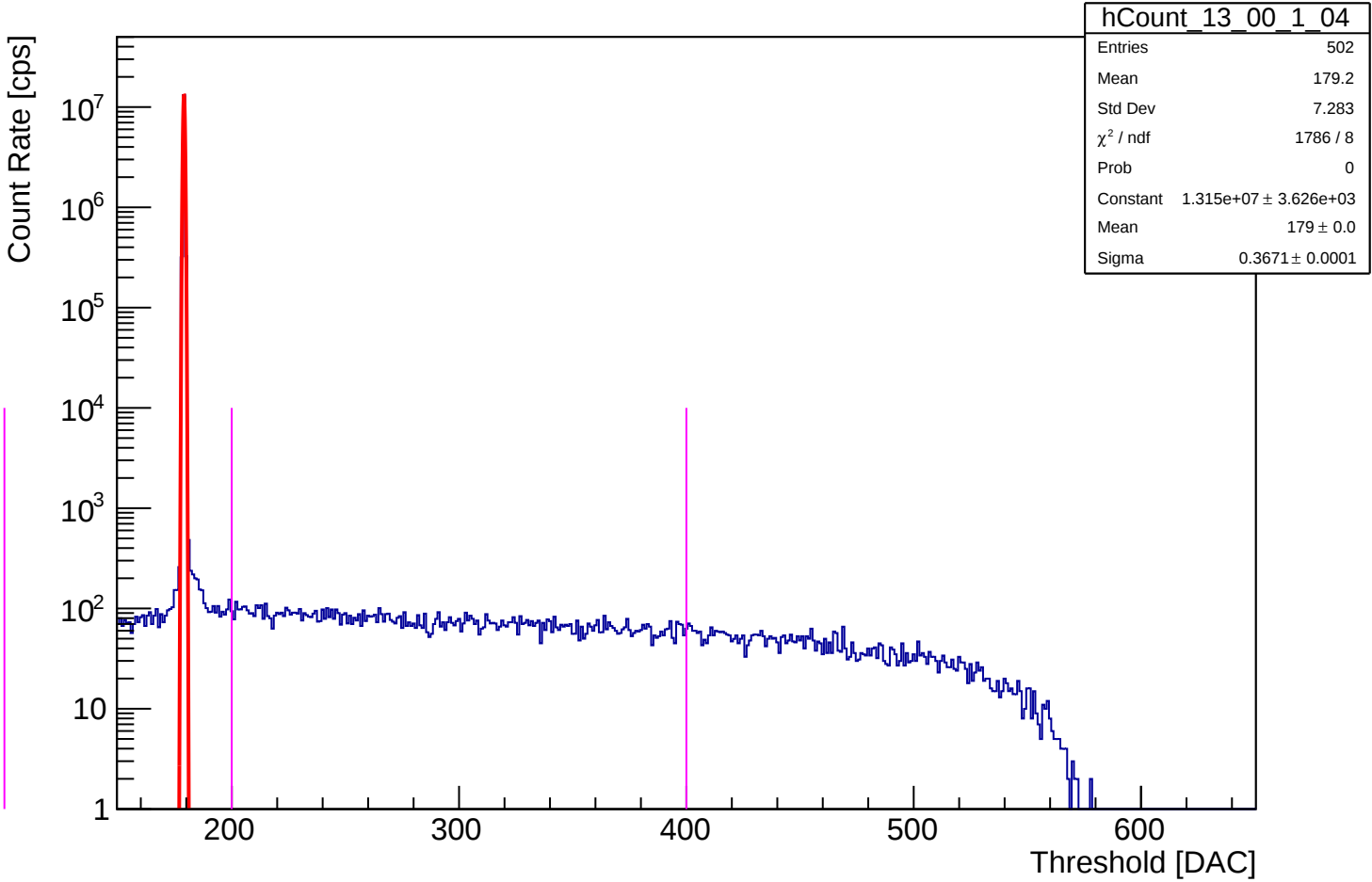


Row 1 Tile 1 Pmt 2 Pixel 49 Slot 13 Fiber 0 Asic 1 Channel 7

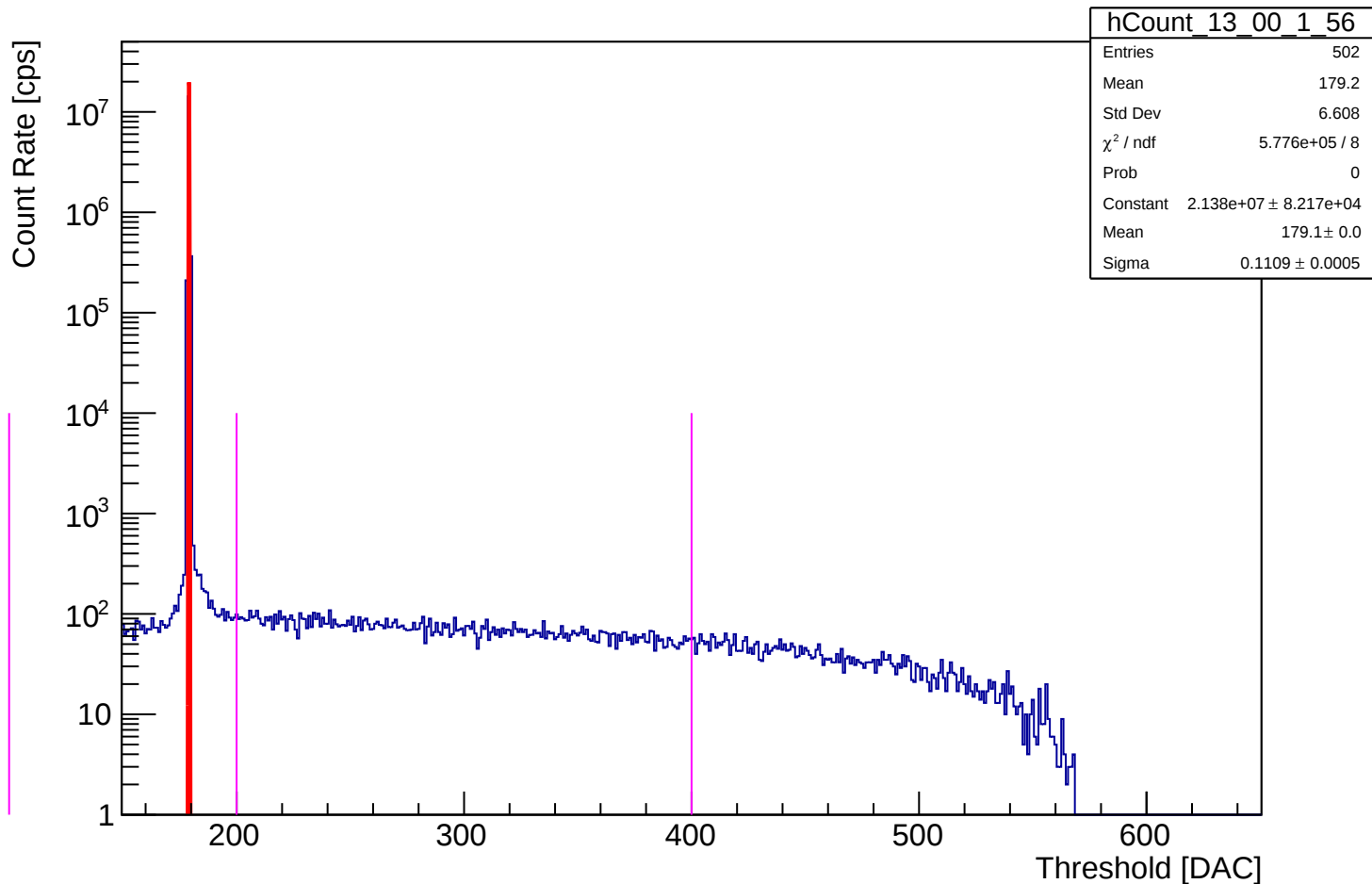




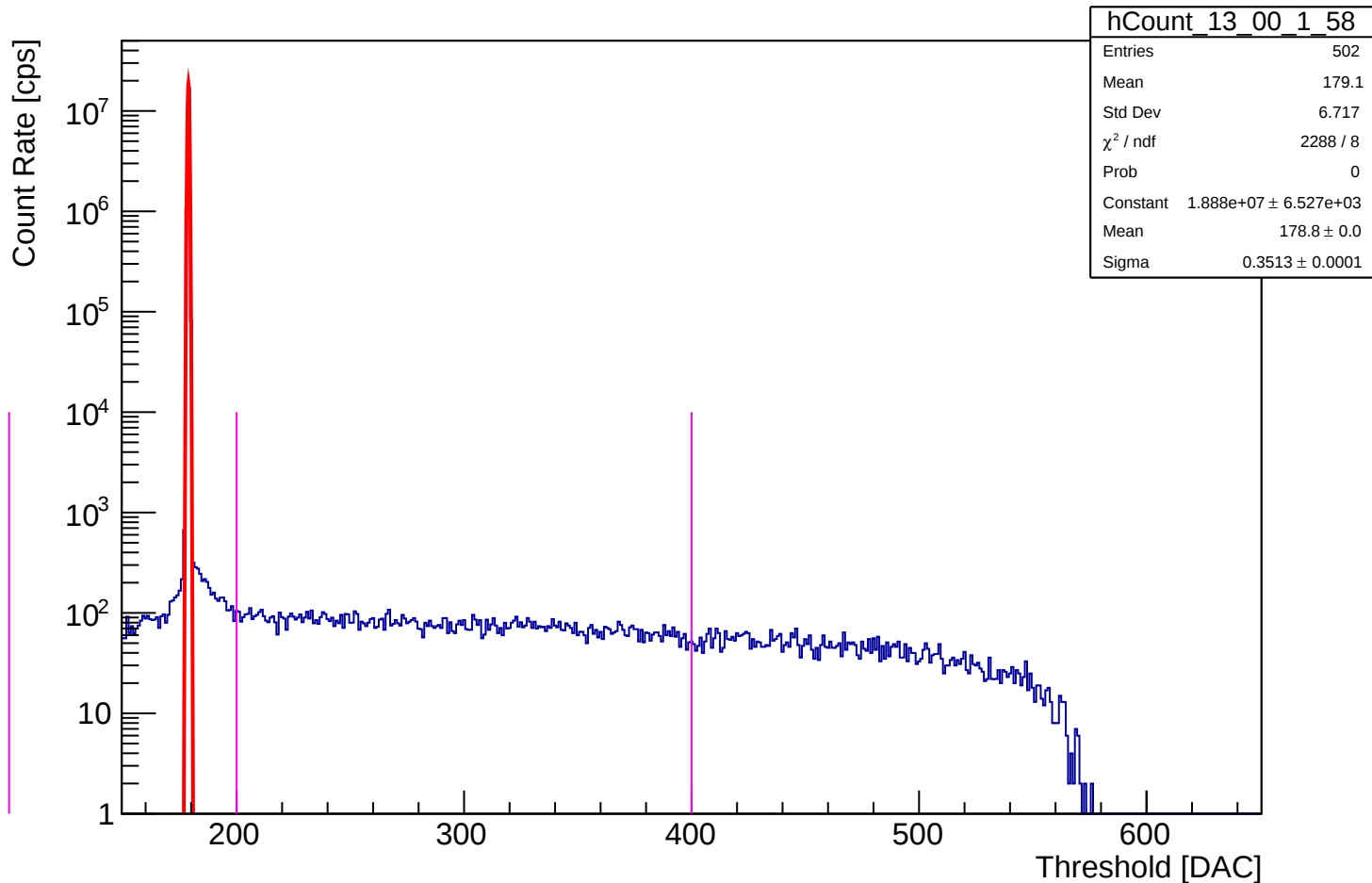




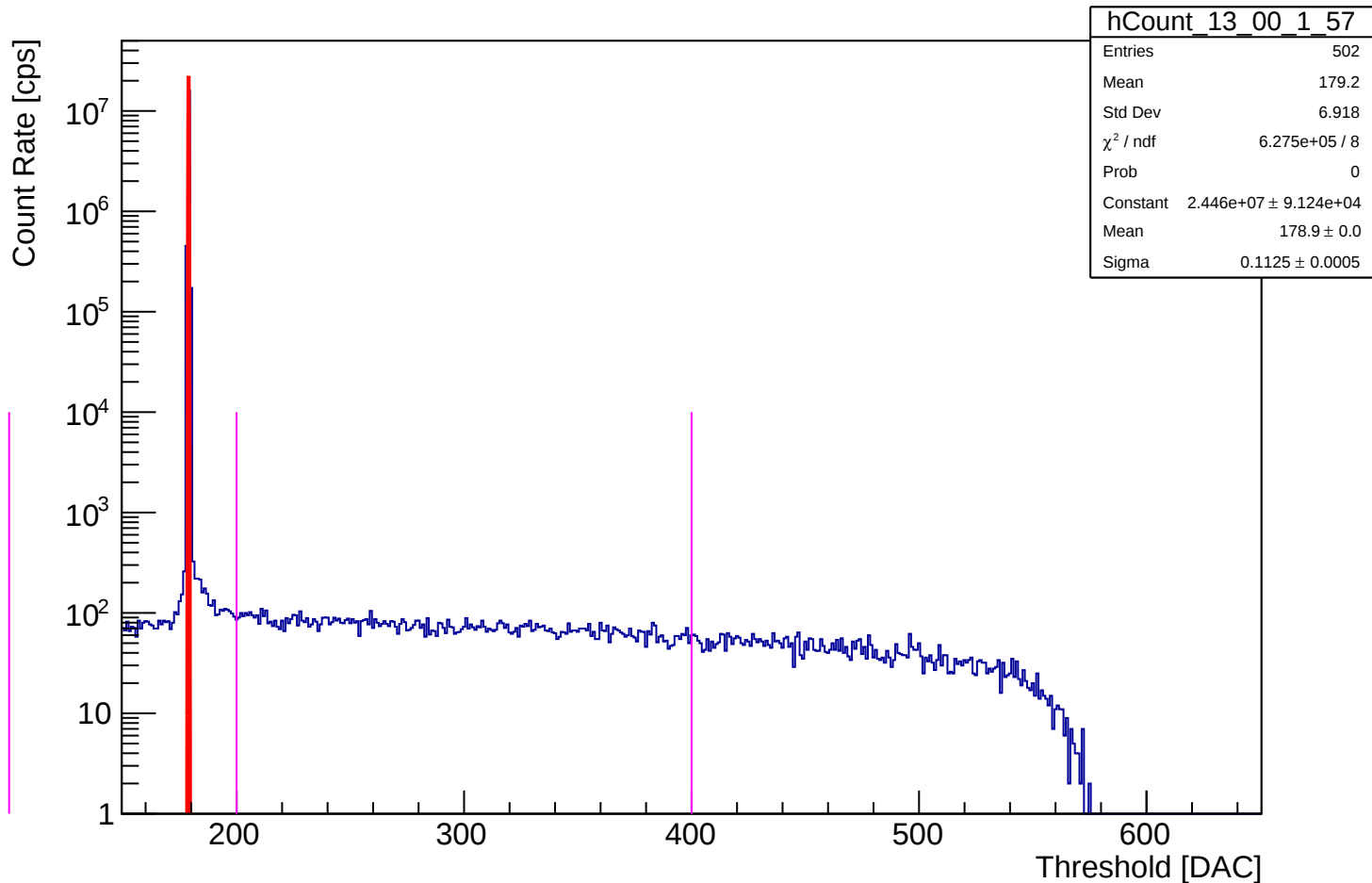
Row 1 Tile 1 Pmt 2 Pixel 53 Slot 13 Fiber 0 Asic 1 Channel 56



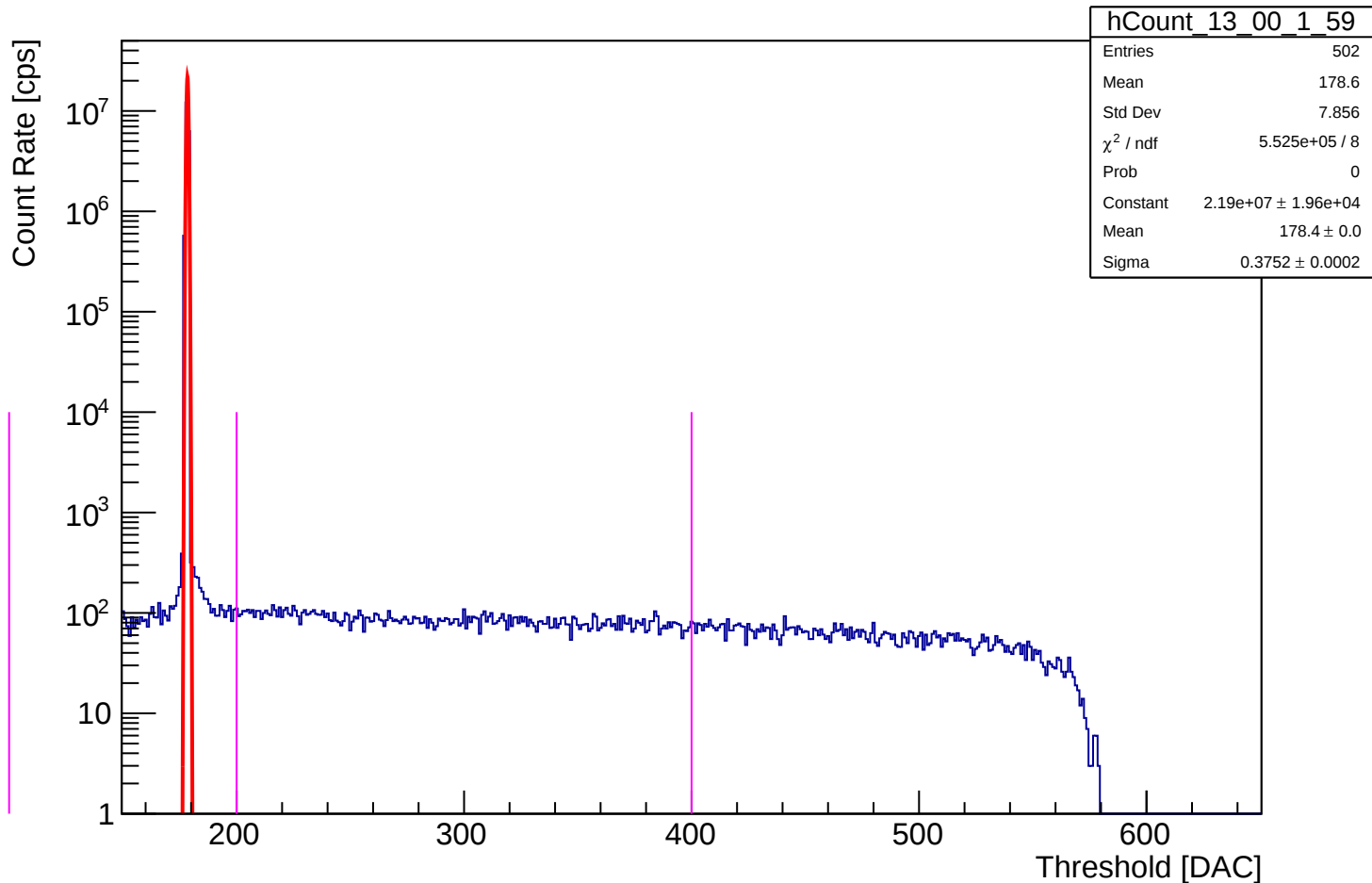
Row 1 Tile 1 Pmt 2 Pixel 54 Slot 13 Fiber 0 Asic 1 Channel 58

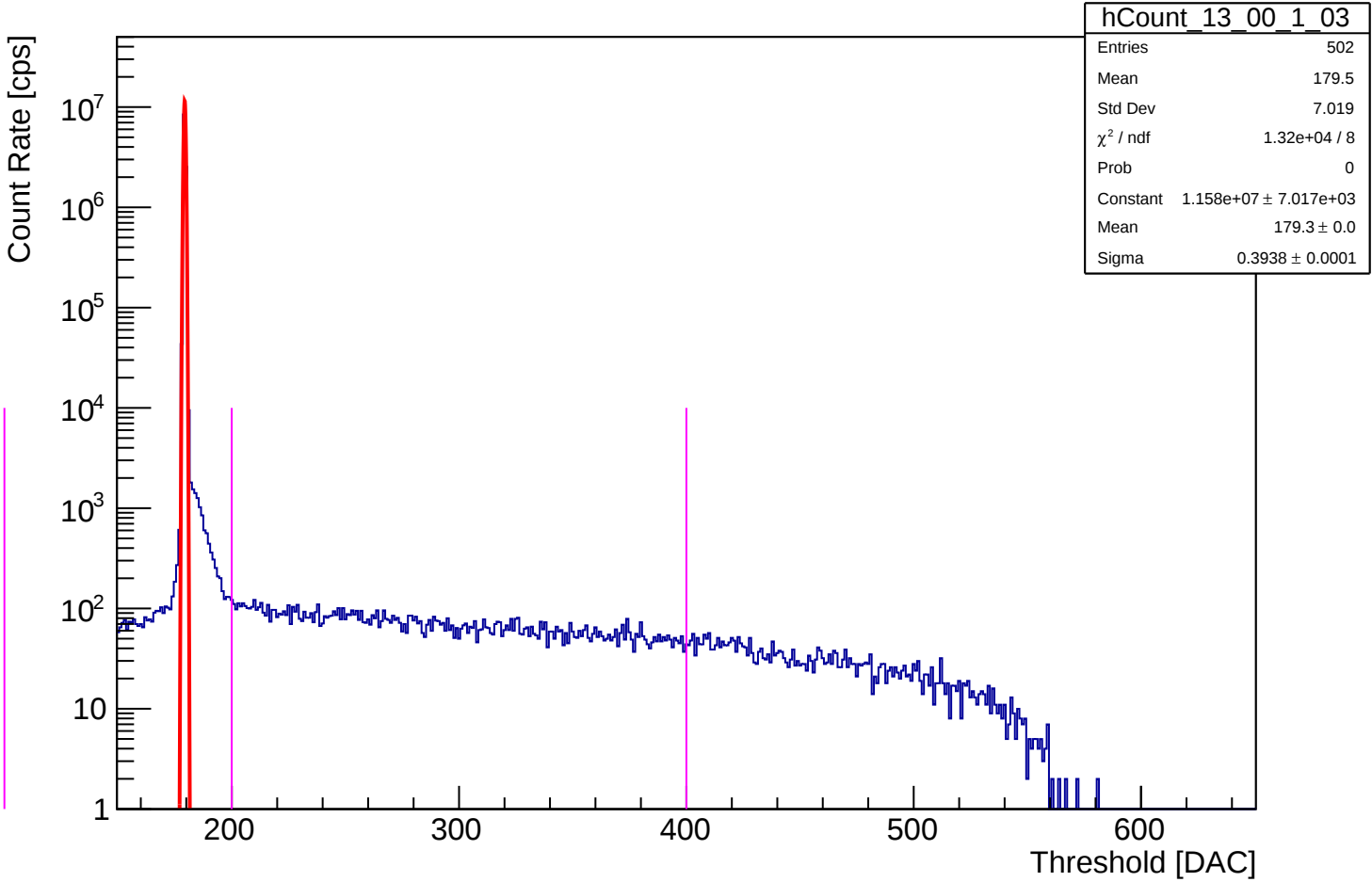


Row 1 Tile 1 Pmt 2 Pixel 55 Slot 13 Fiber 0 Asic 1 Channel 57

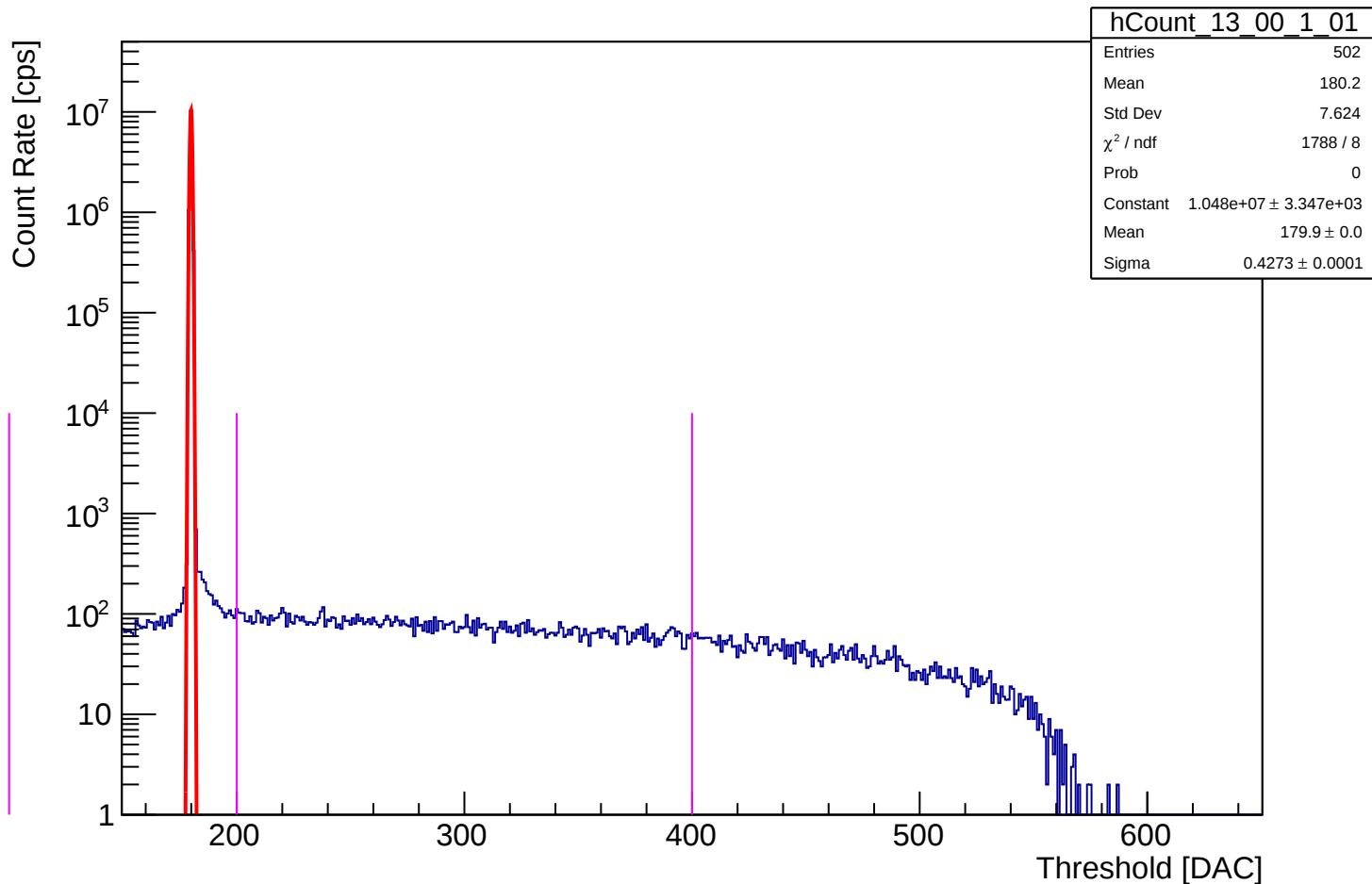


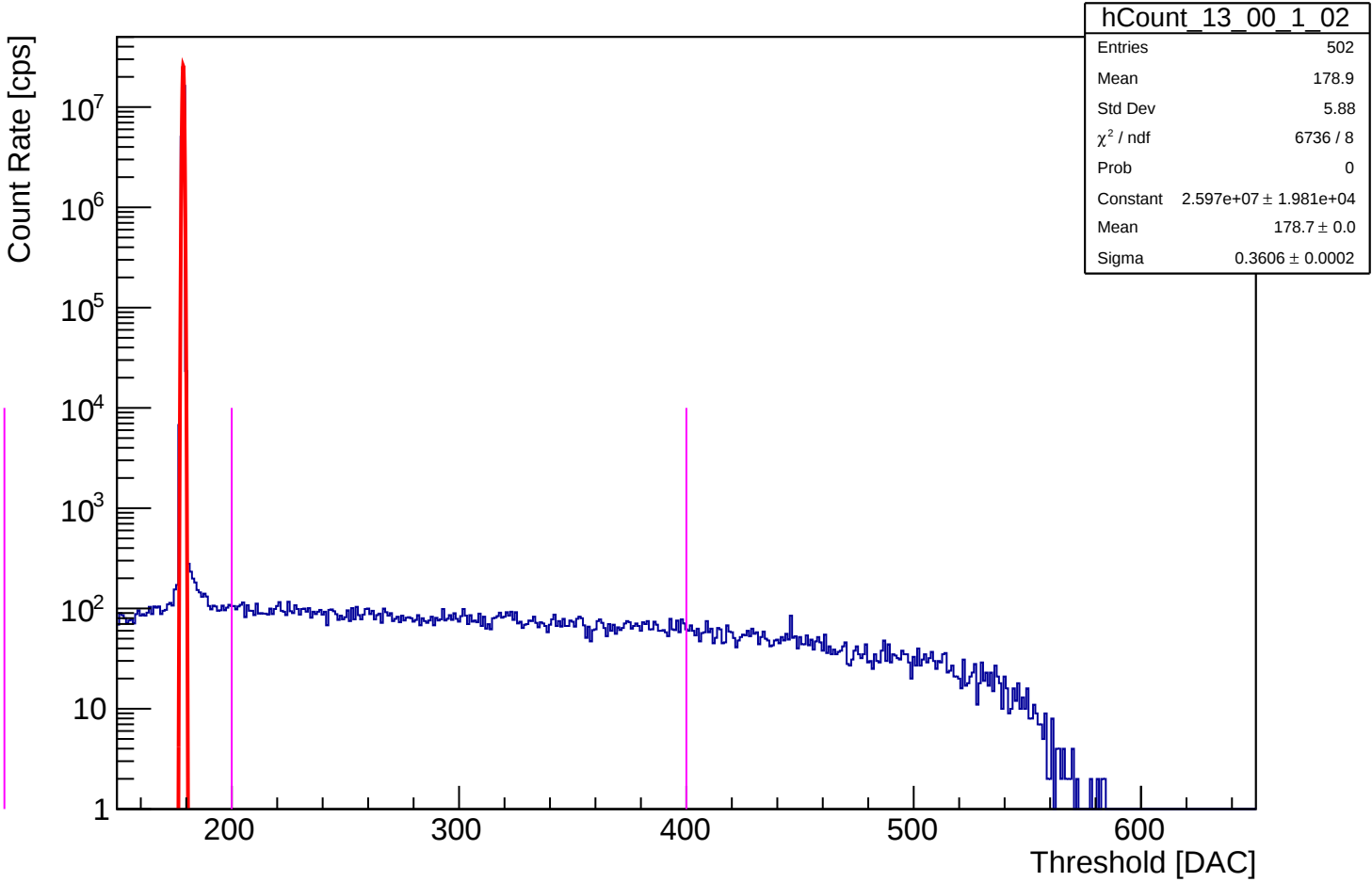
Row 1 Tile 1 Pmt 2 Pixel 56 Slot 13 Fiber 0 Asic 1 Channel 59

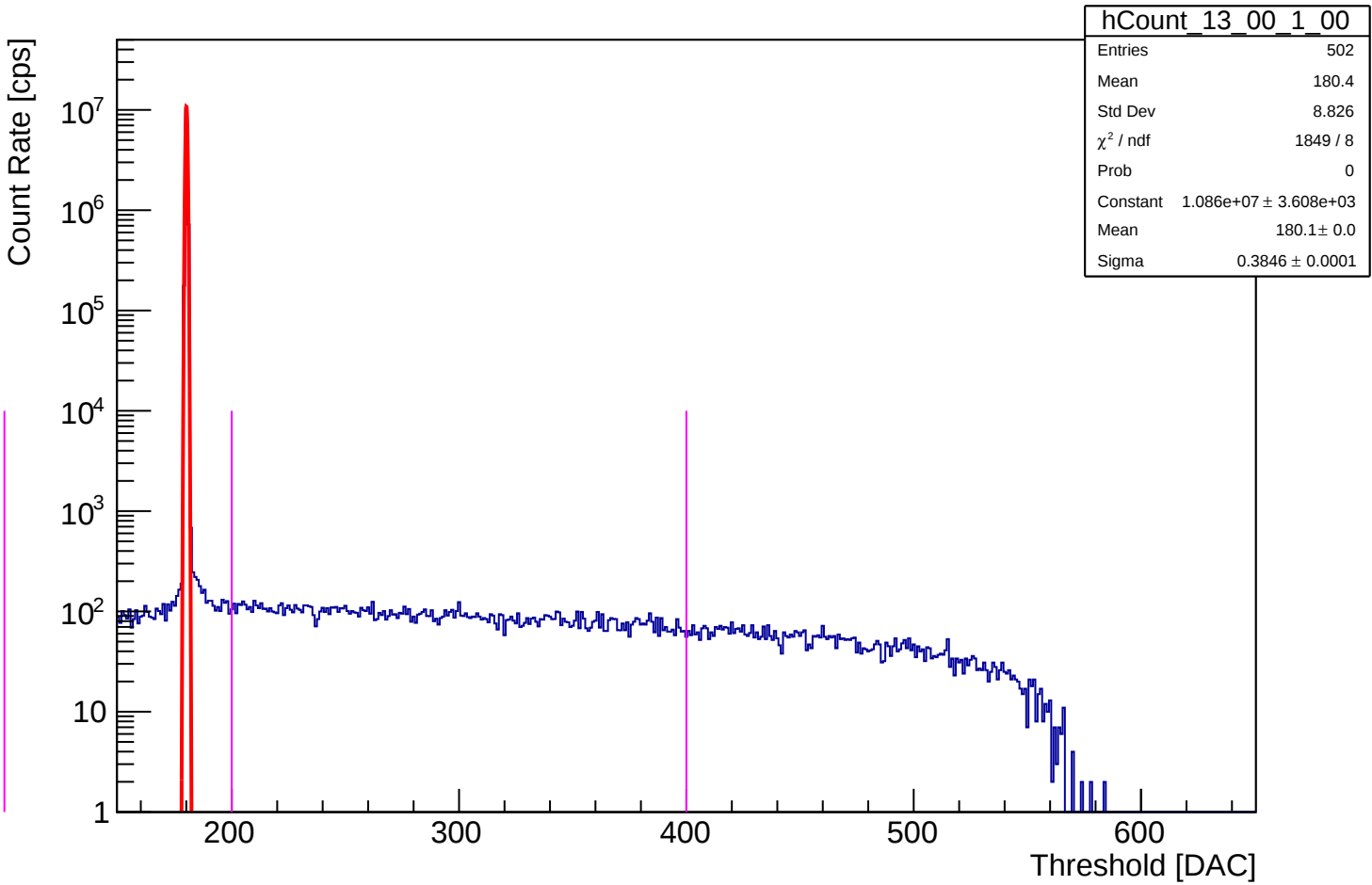




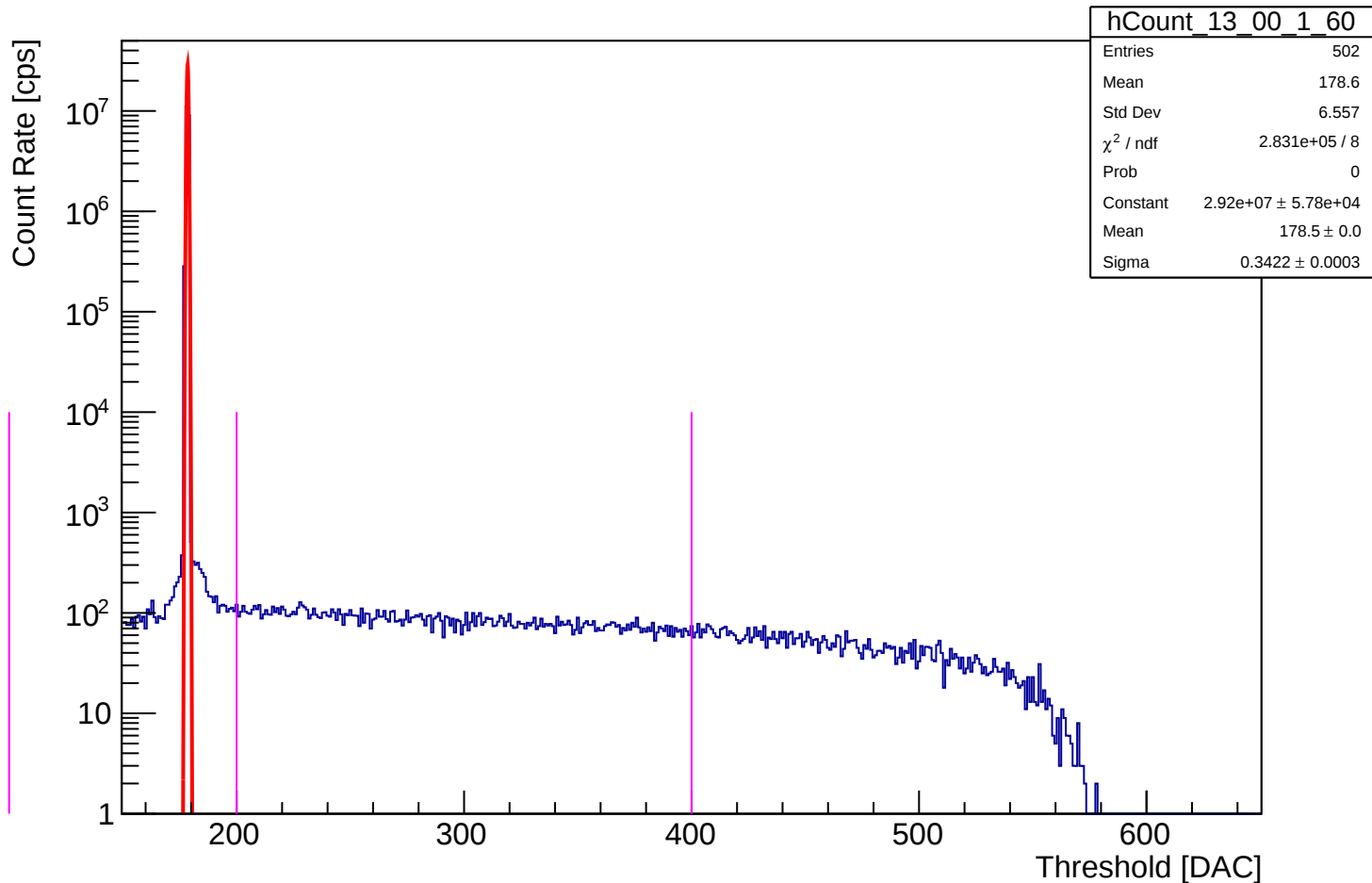
Row 1 Tile 1 Pmt 2 Pixel 58 Slot 13 Fiber 0 Asic 1 Channel 1



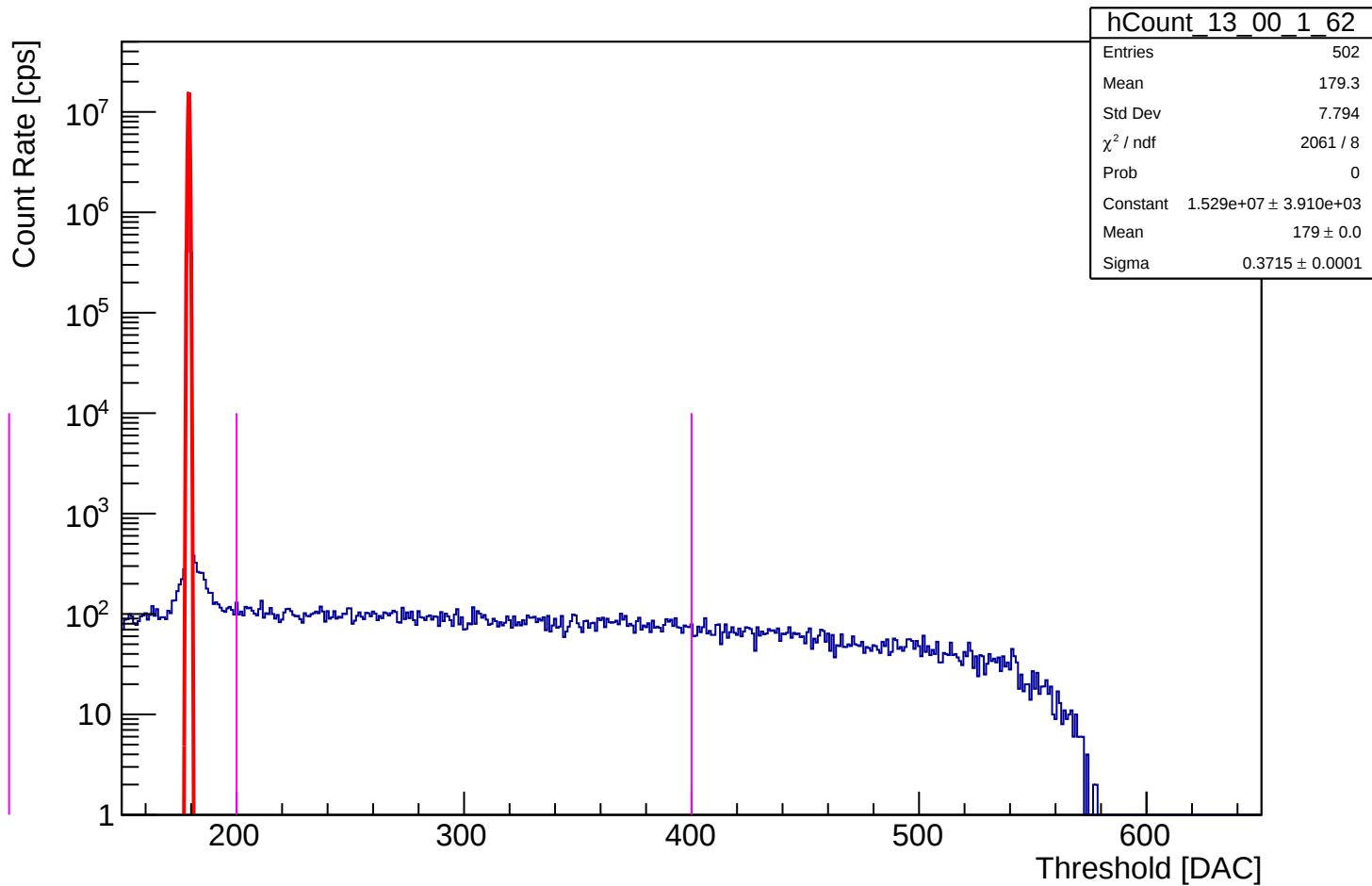




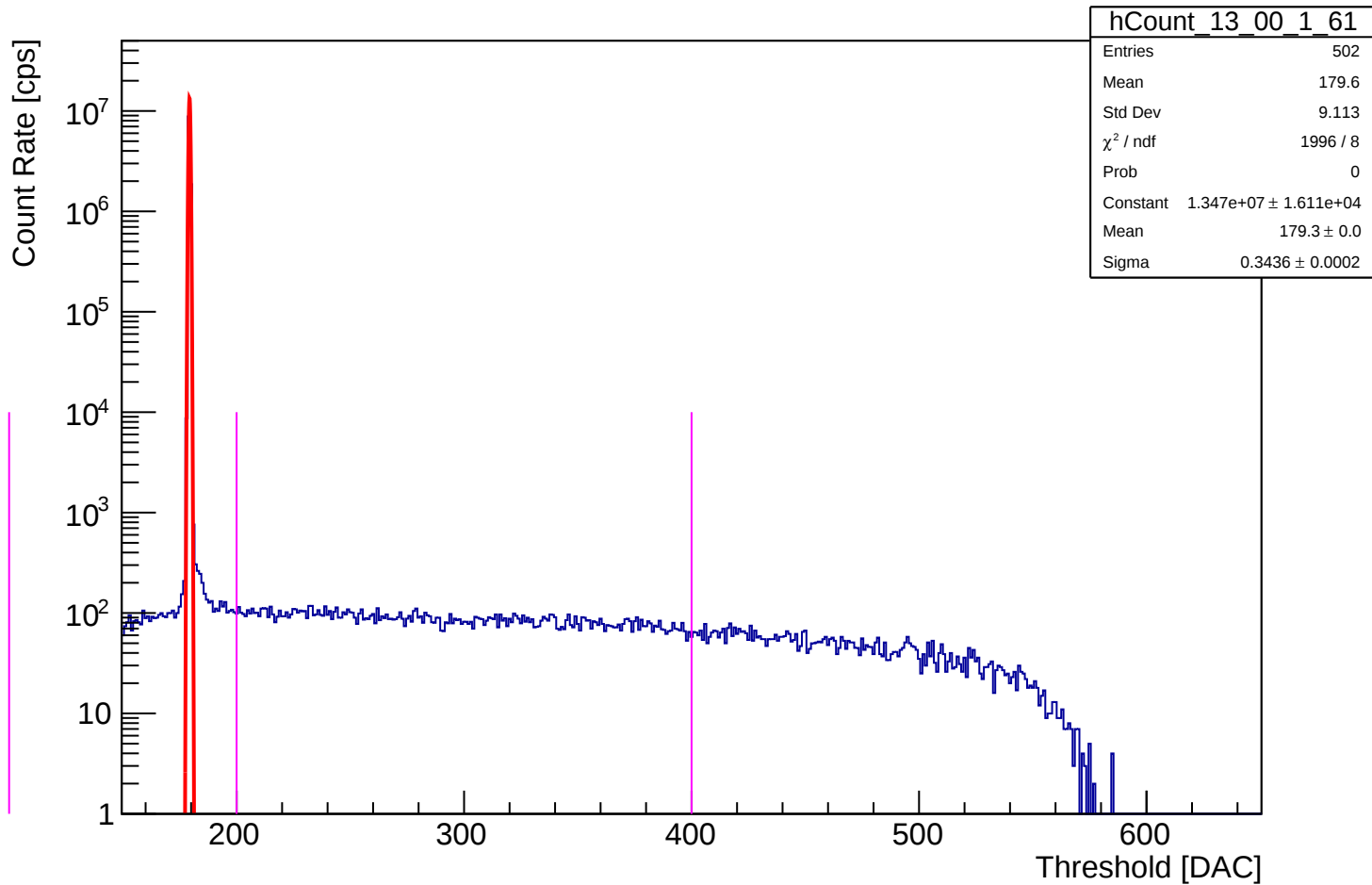
Row 1 Tile 1 Pmt 2 Pixel 61 Slot 13 Fiber 0 Asic 1 Channel 60



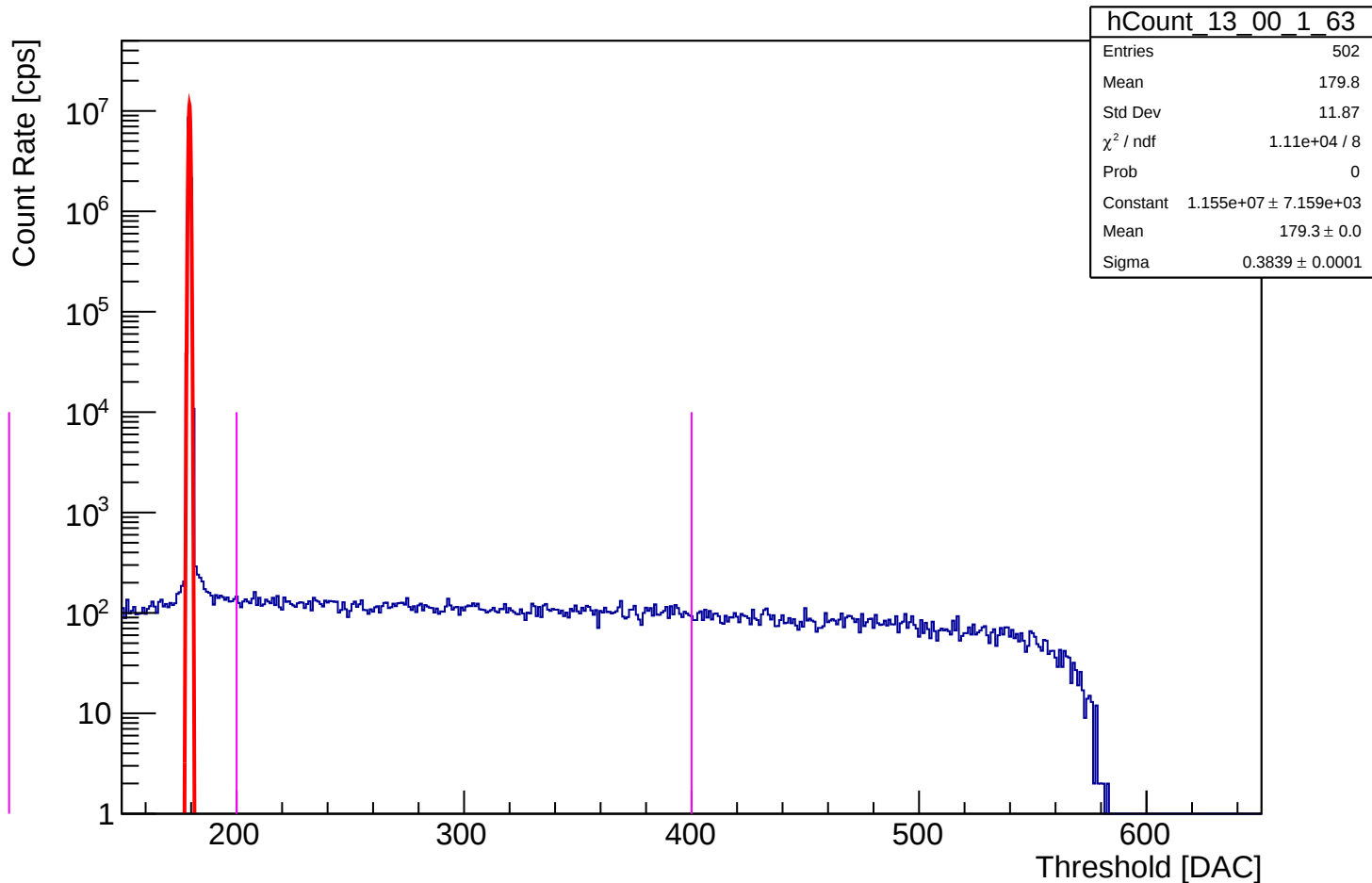
Row 1 Tile 1 Pmt 2 Pixel 62 Slot 13 Fiber 0 Asic 1 Channel 62



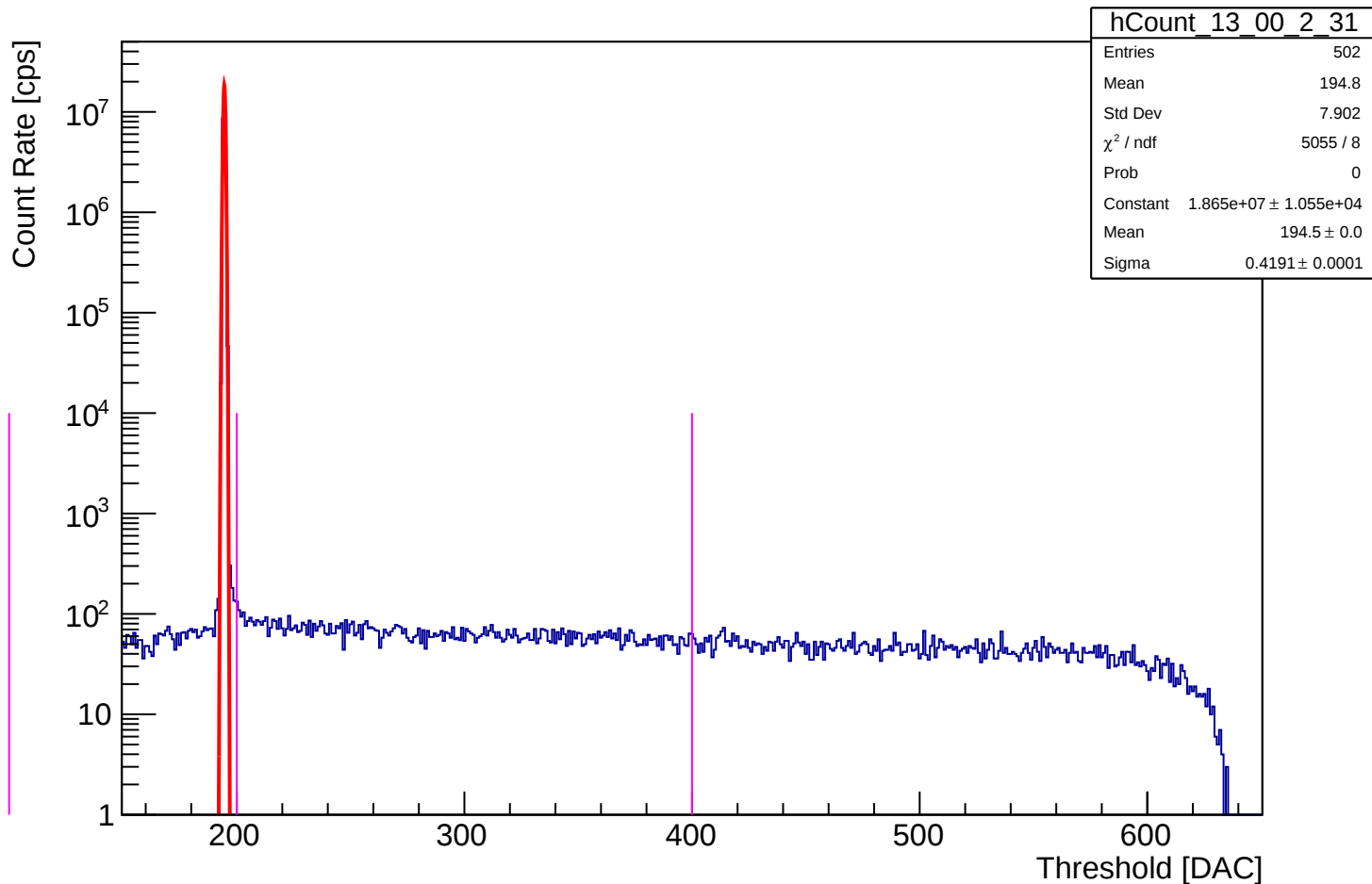
Row 1 Tile 1 Pmt 2 Pixel 63 Slot 13 Fiber 0 Asic 1 Channel 61



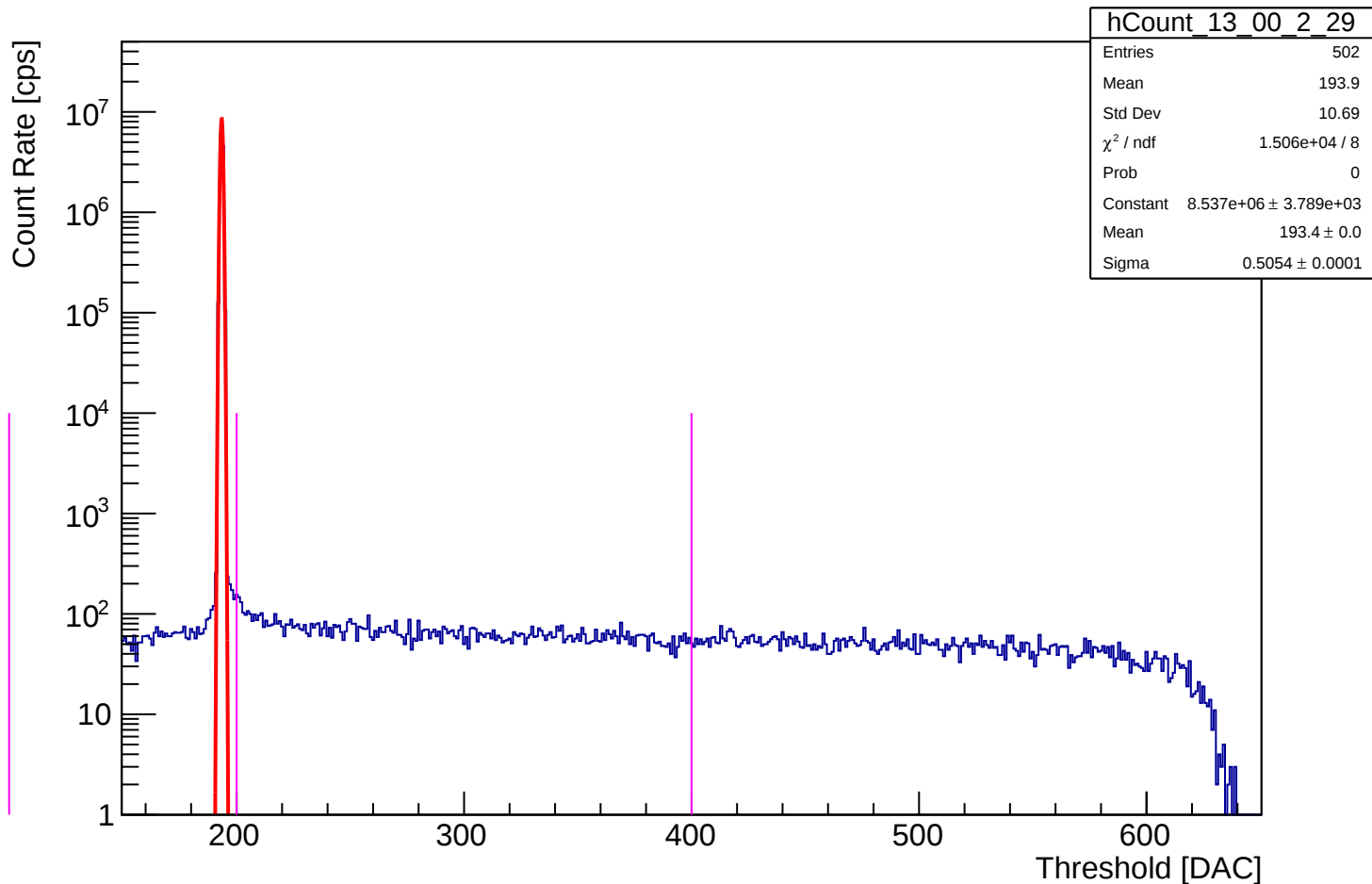
Row 1 Tile 1 Pmt 2 Pixel 64 Slot 13 Fiber 0 Asic 1 Channel 63



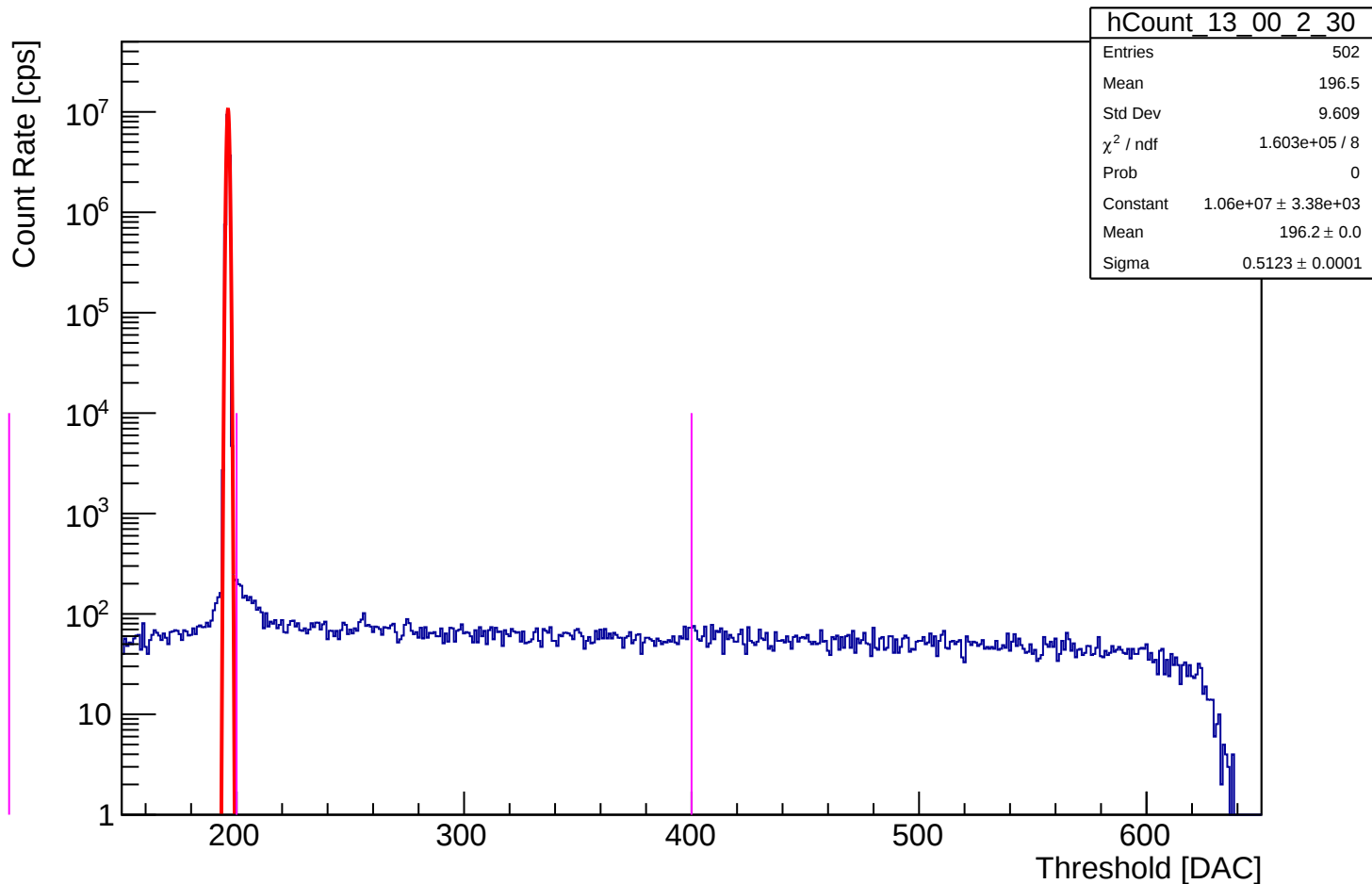
Row 1 Tile 1 Pmt 3 Pixel 1 Slot 13 Fiber 0 Asic 2 Channel 31



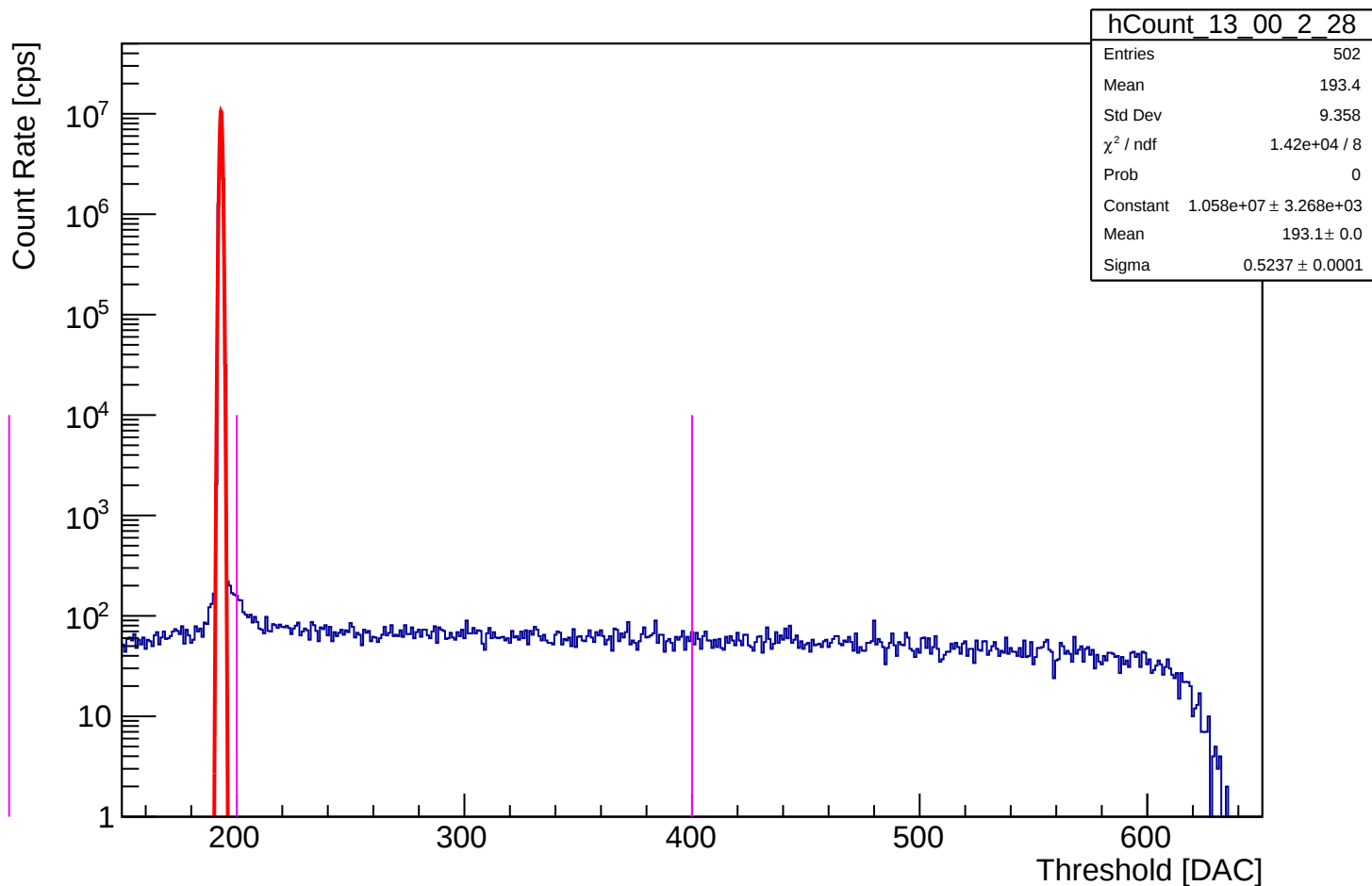
Row 1 Tile 1 Pmt 3 Pixel 2 Slot 13 Fiber 0 Asic 2 Channel 29



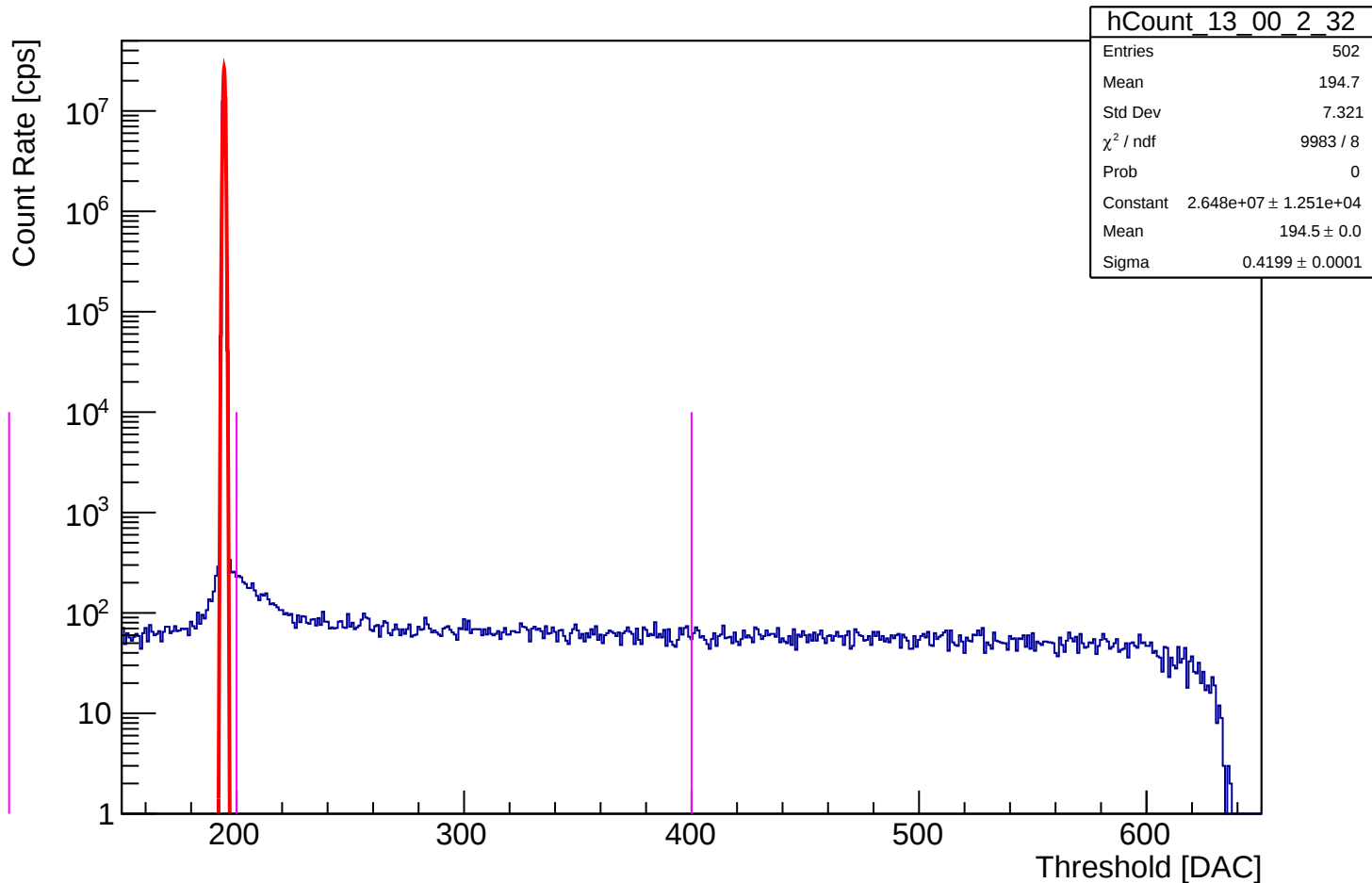
Row 1 Tile 1 Pmt 3 Pixel 3 Slot 13 Fiber 0 Asic 2 Channel 30



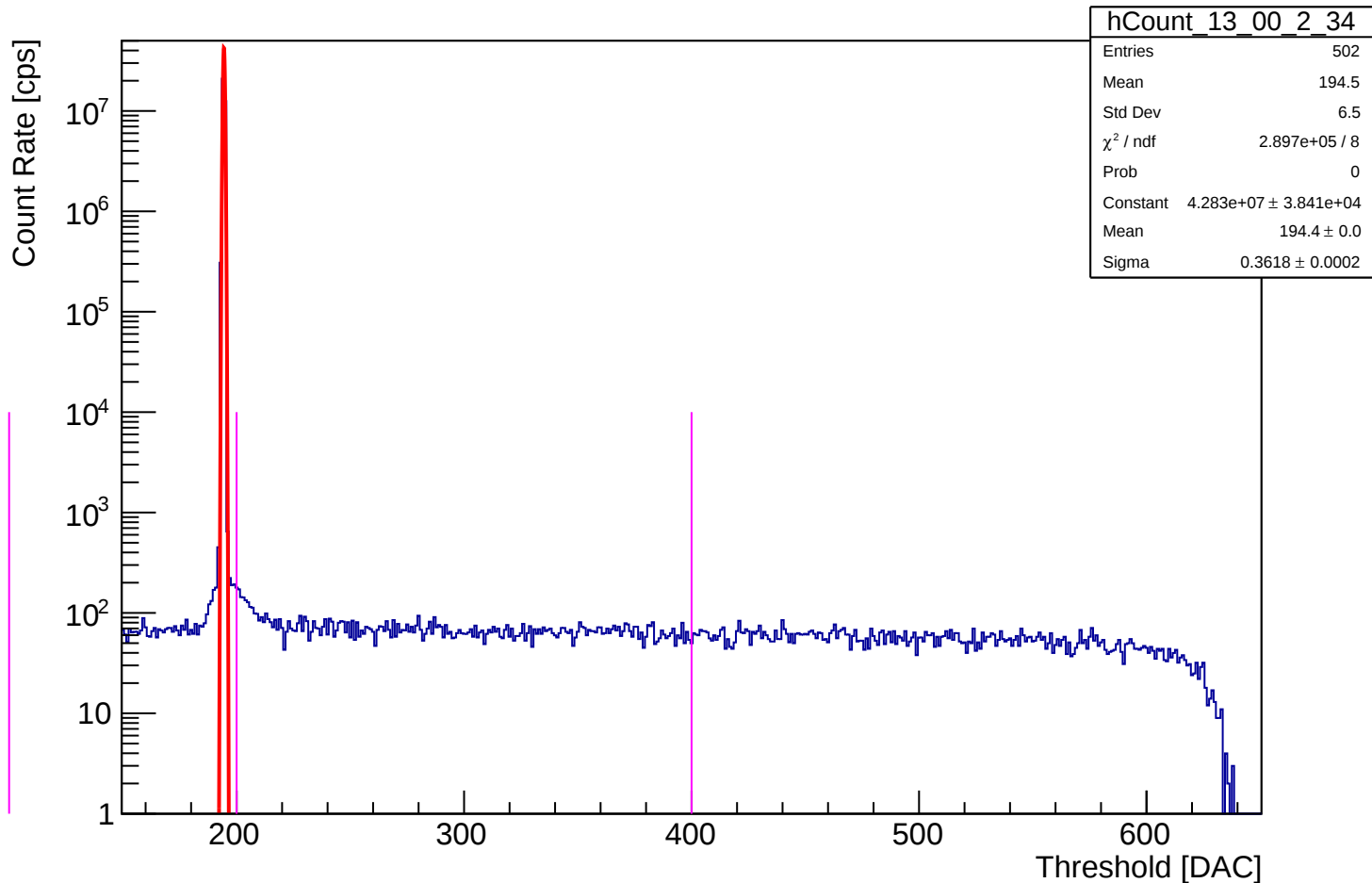
Row 1 Tile 1 Pmt 3 Pixel 4 Slot 13 Fiber 0 Asic 2 Channel 28



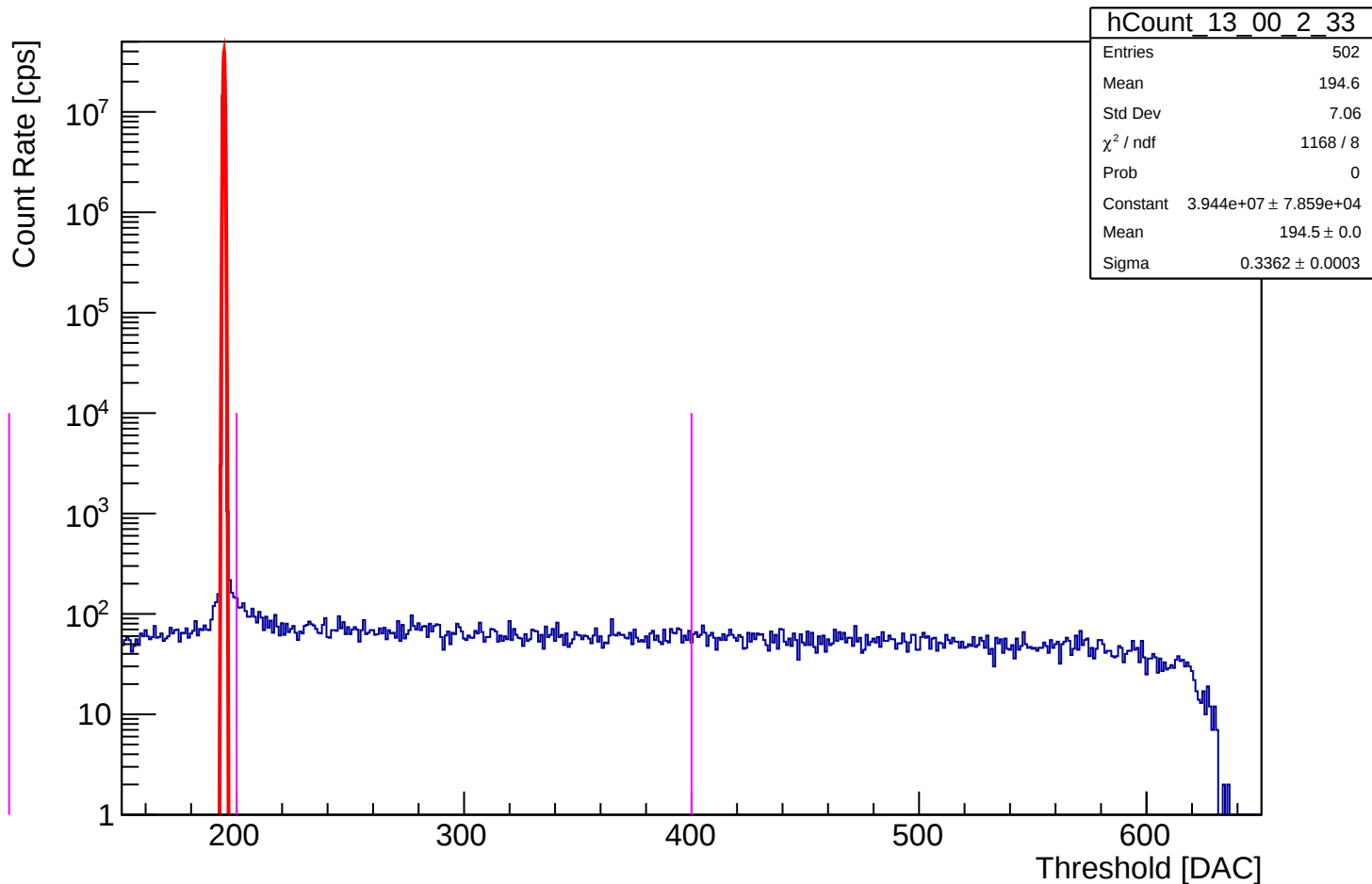
Row 1 Tile 1 Pmt 3 Pixel 5 Slot 13 Fiber 0 Asic 2 Channel 32



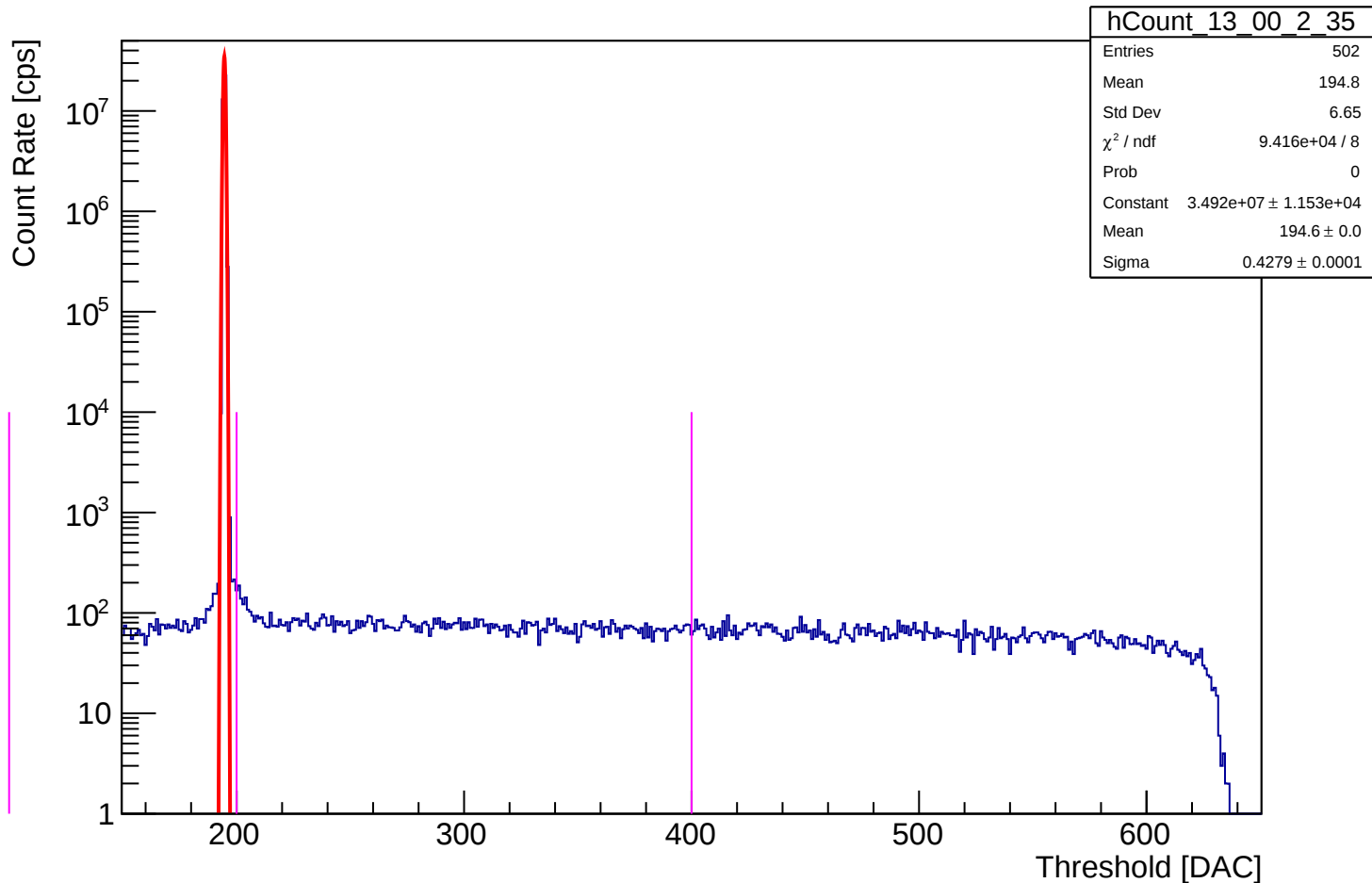
Row 1 Tile 1 Pmt 3 Pixel 6 Slot 13 Fiber 0 Asic 2 Channel 34



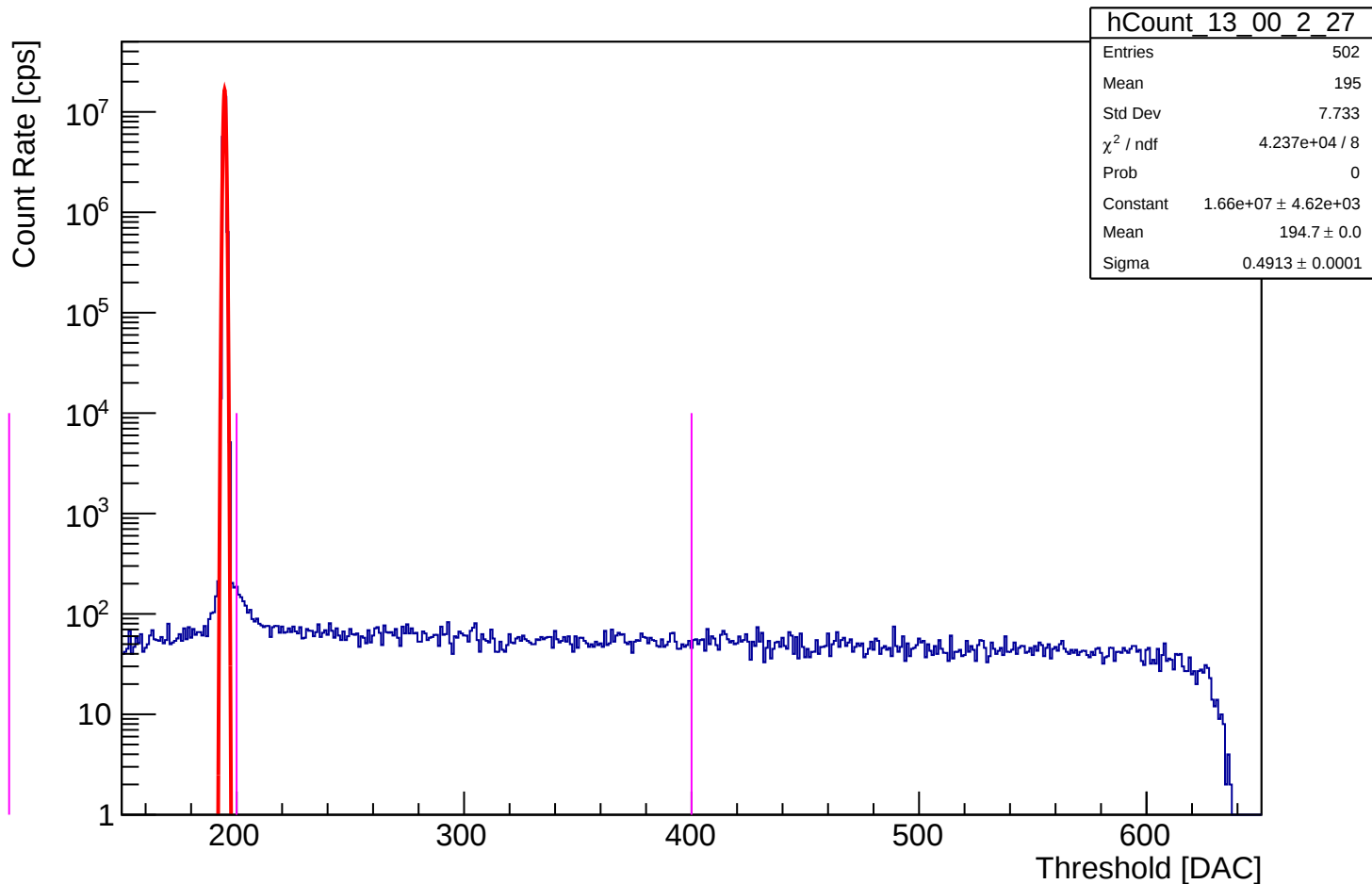
Row 1 Tile 1 Pmt 3 Pixel 7 Slot 13 Fiber 0 Asic 2 Channel 33



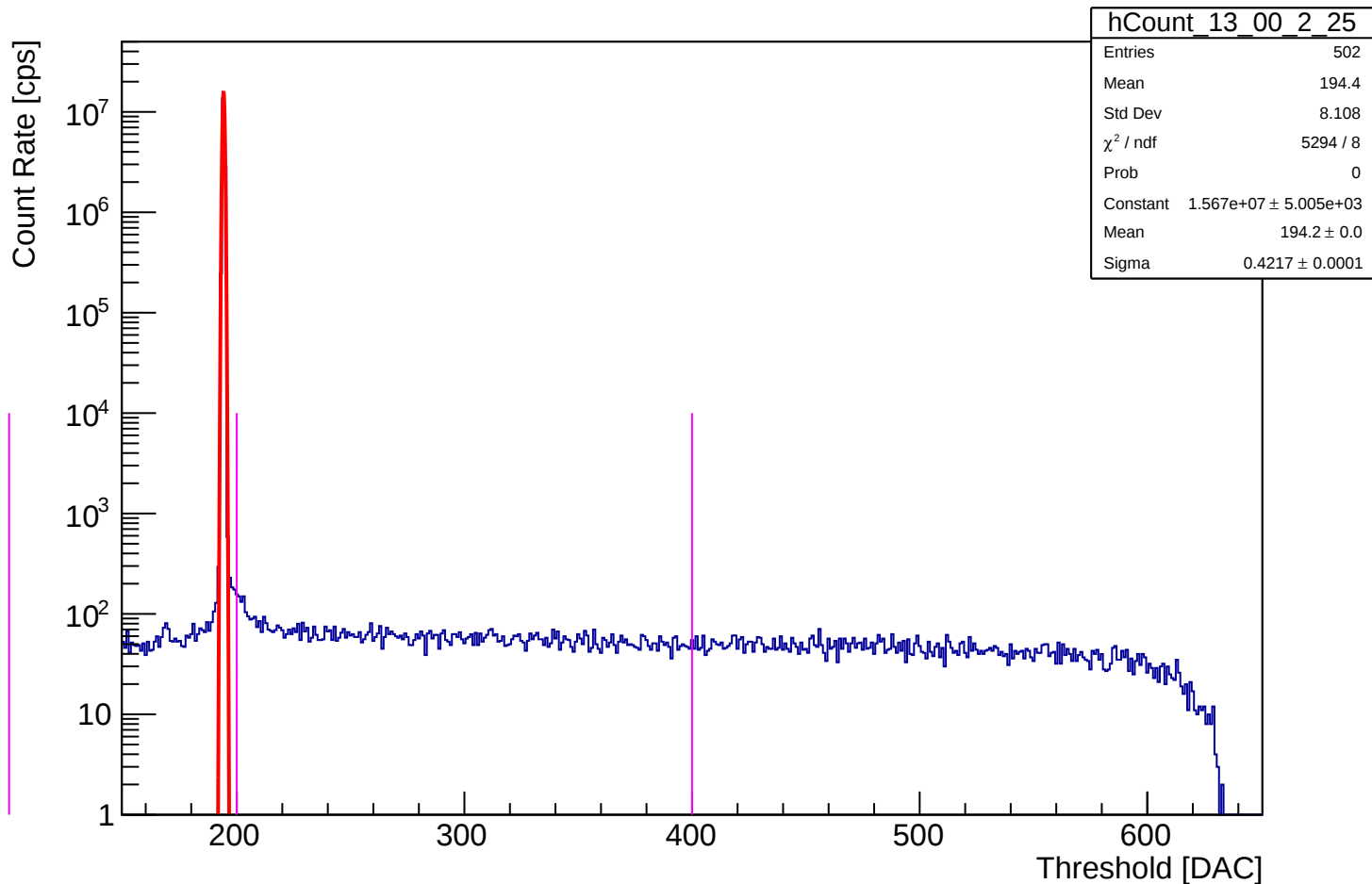
Row 1 Tile 1 Pmt 3 Pixel 8 Slot 13 Fiber 0 Asic 2 Channel 35



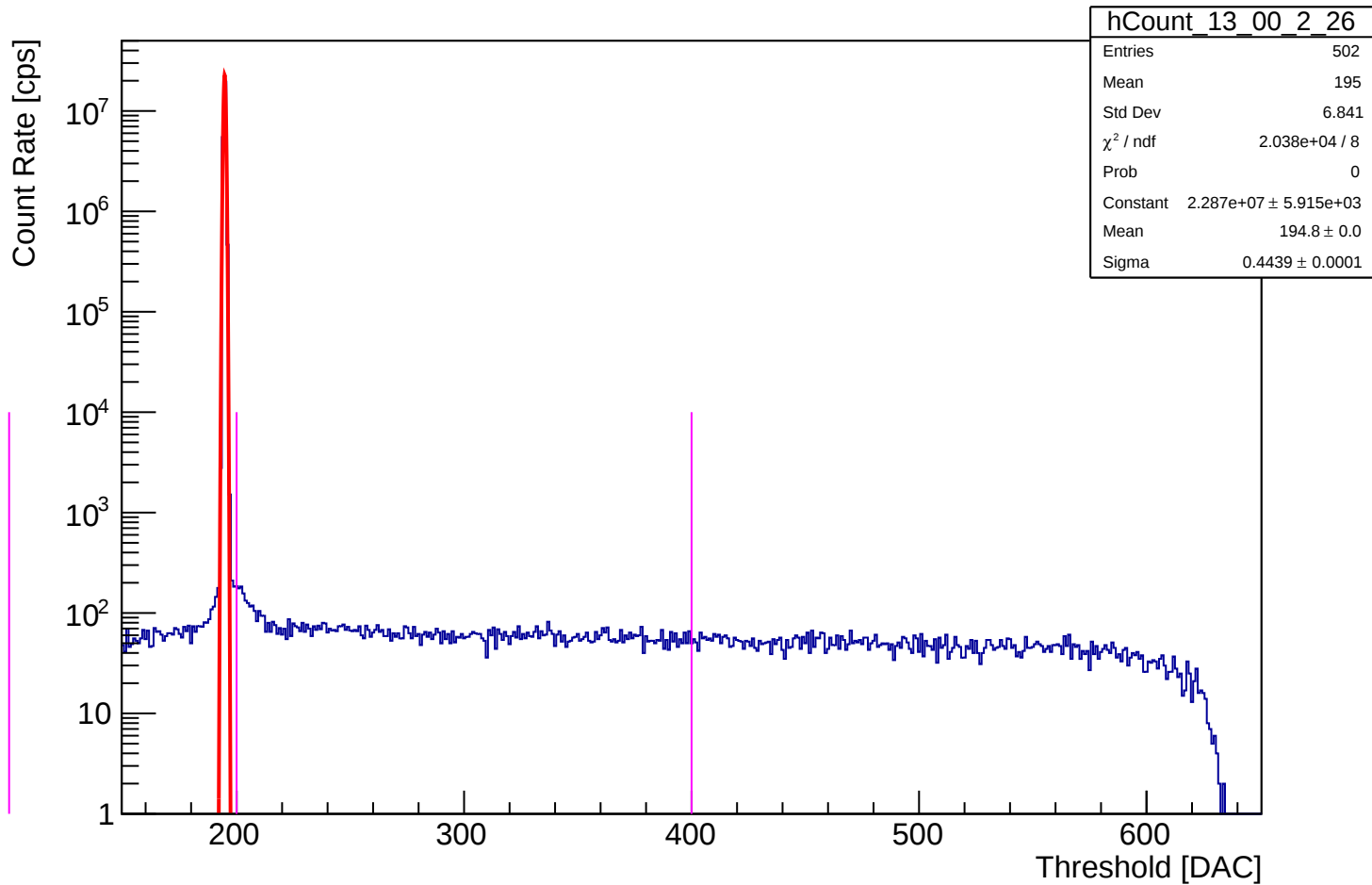
Row 1 Tile 1 Pmt 3 Pixel 9 Slot 13 Fiber 0 Asic 2 Channel 27



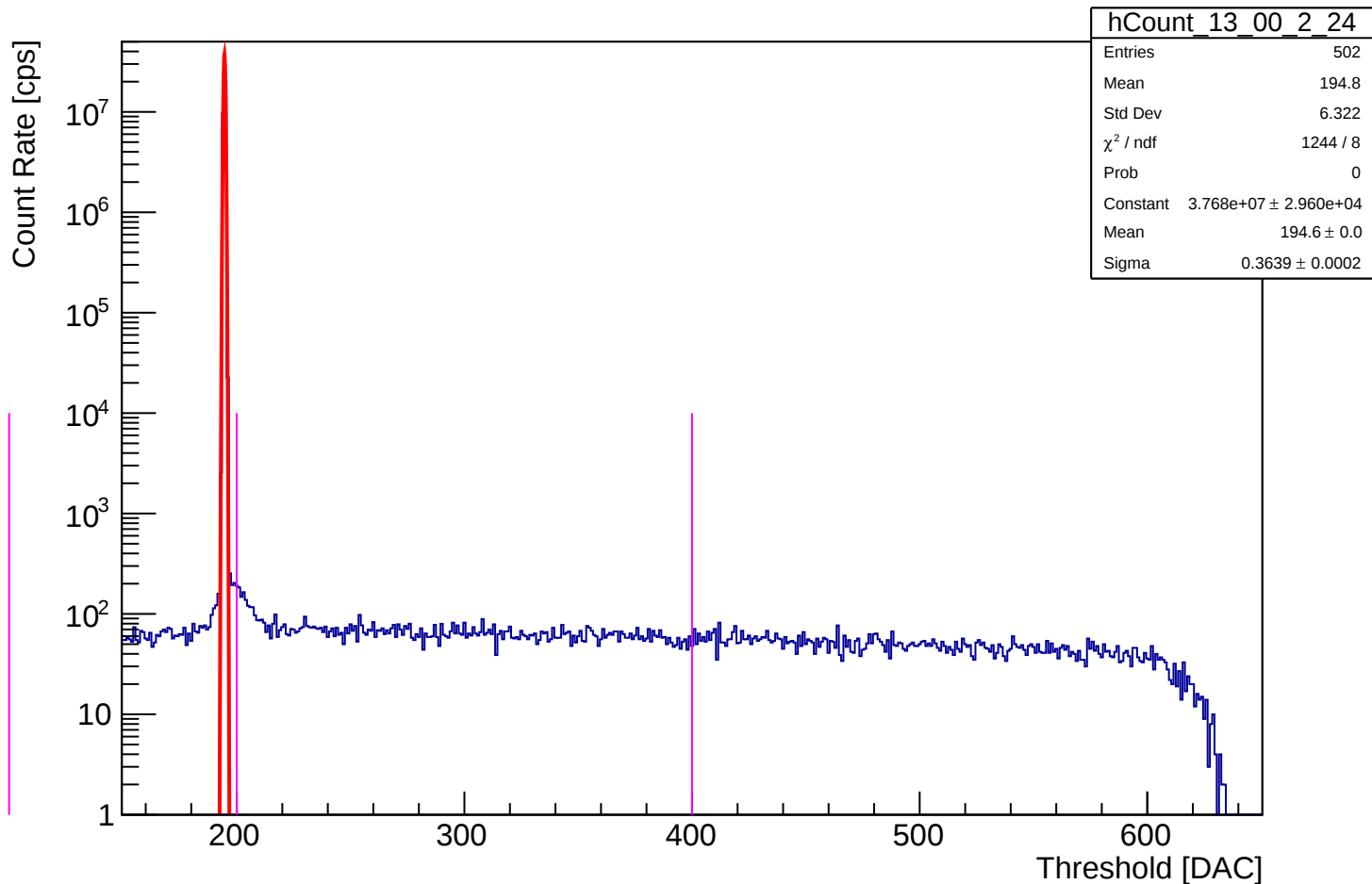
Row 1 Tile 1 Pmt 3 Pixel 10 Slot 13 Fiber 0 Asic 2 Channel 25



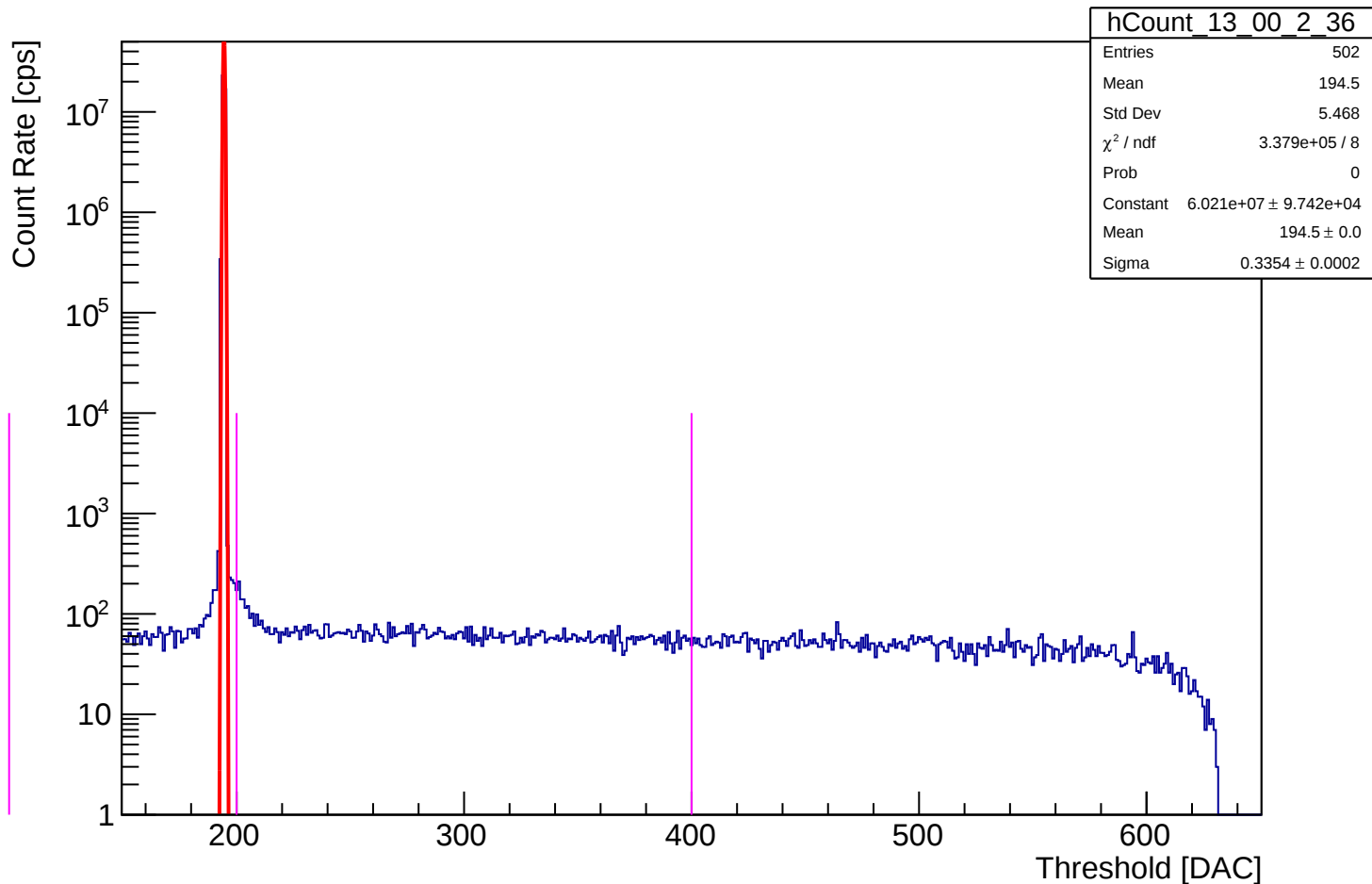
Row 1 Tile 1 Pmt 3 Pixel 11 Slot 13 Fiber 0 Asic 2 Channel 26



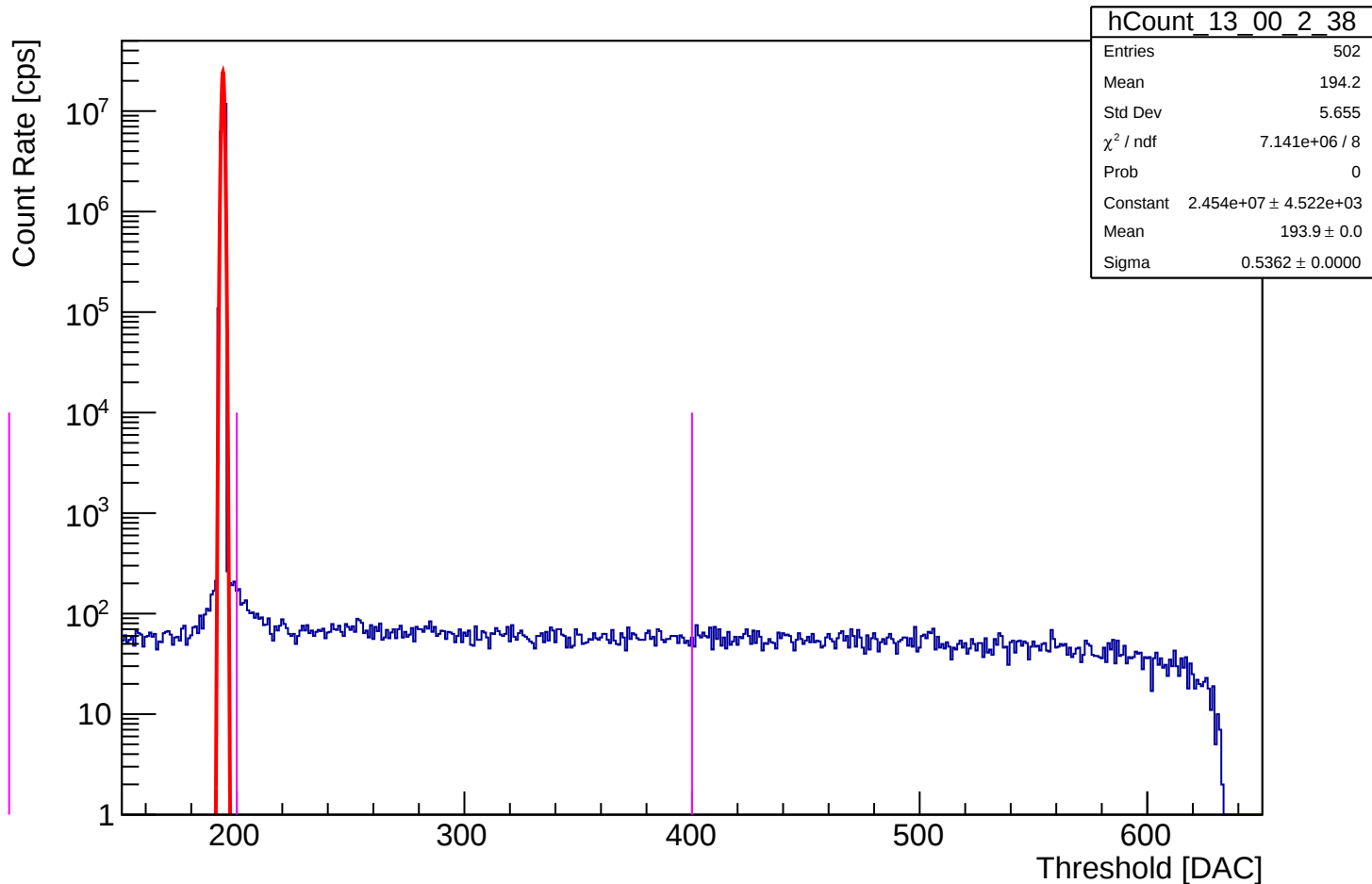
Row 1 Tile 1 Pmt 3 Pixel 12 Slot 13 Fiber 0 Asic 2 Channel 24



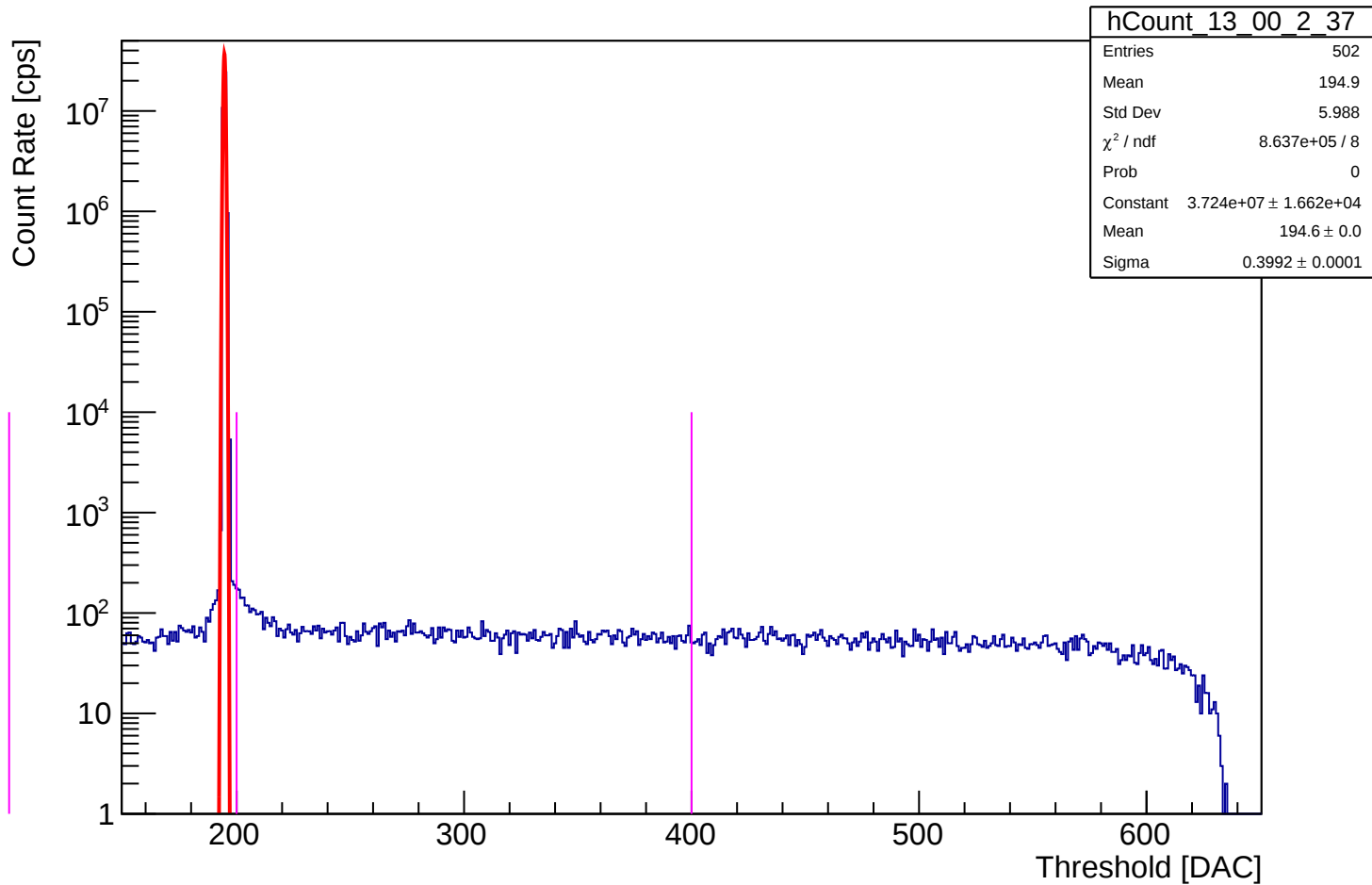
Row 1 Tile 1 Pmt 3 Pixel 13 Slot 13 Fiber 0 Asic 2 Channel 36



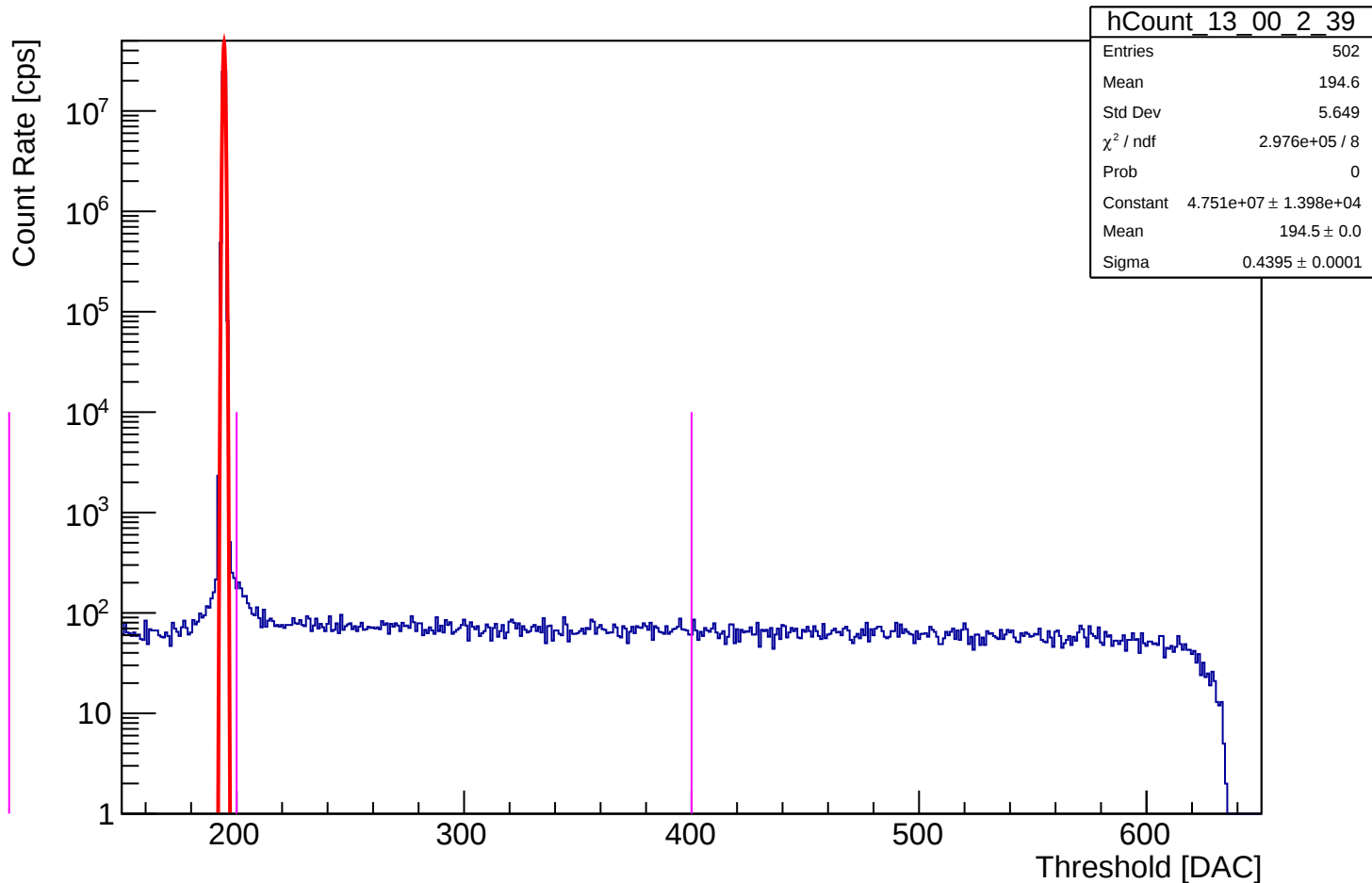
Row 1 Tile 1 Pmt 3 Pixel 14 Slot 13 Fiber 0 Asic 2 Channel 38



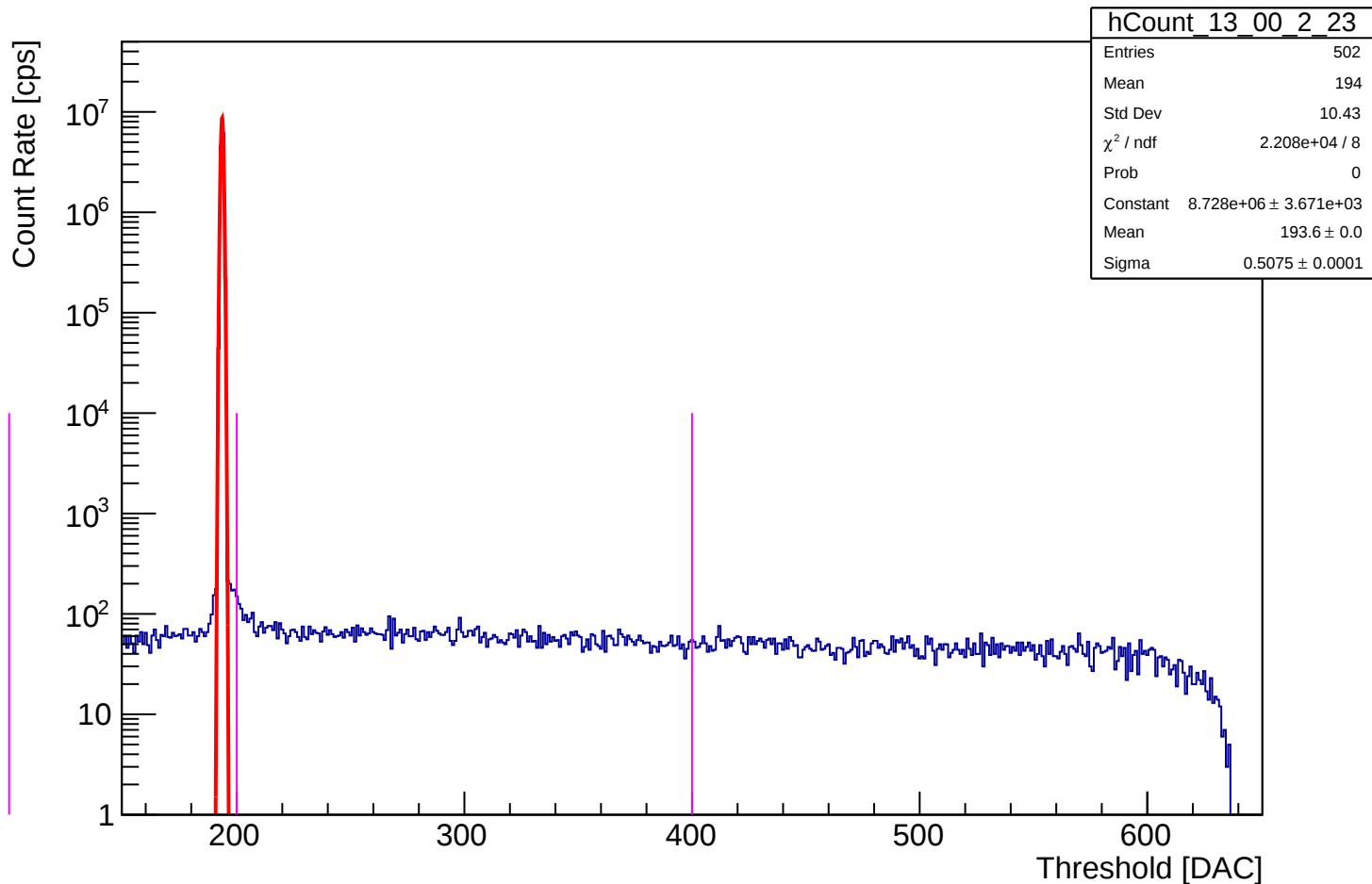
Row 1 Tile 1 Pmt 3 Pixel 15 Slot 13 Fiber 0 Asic 2 Channel 37



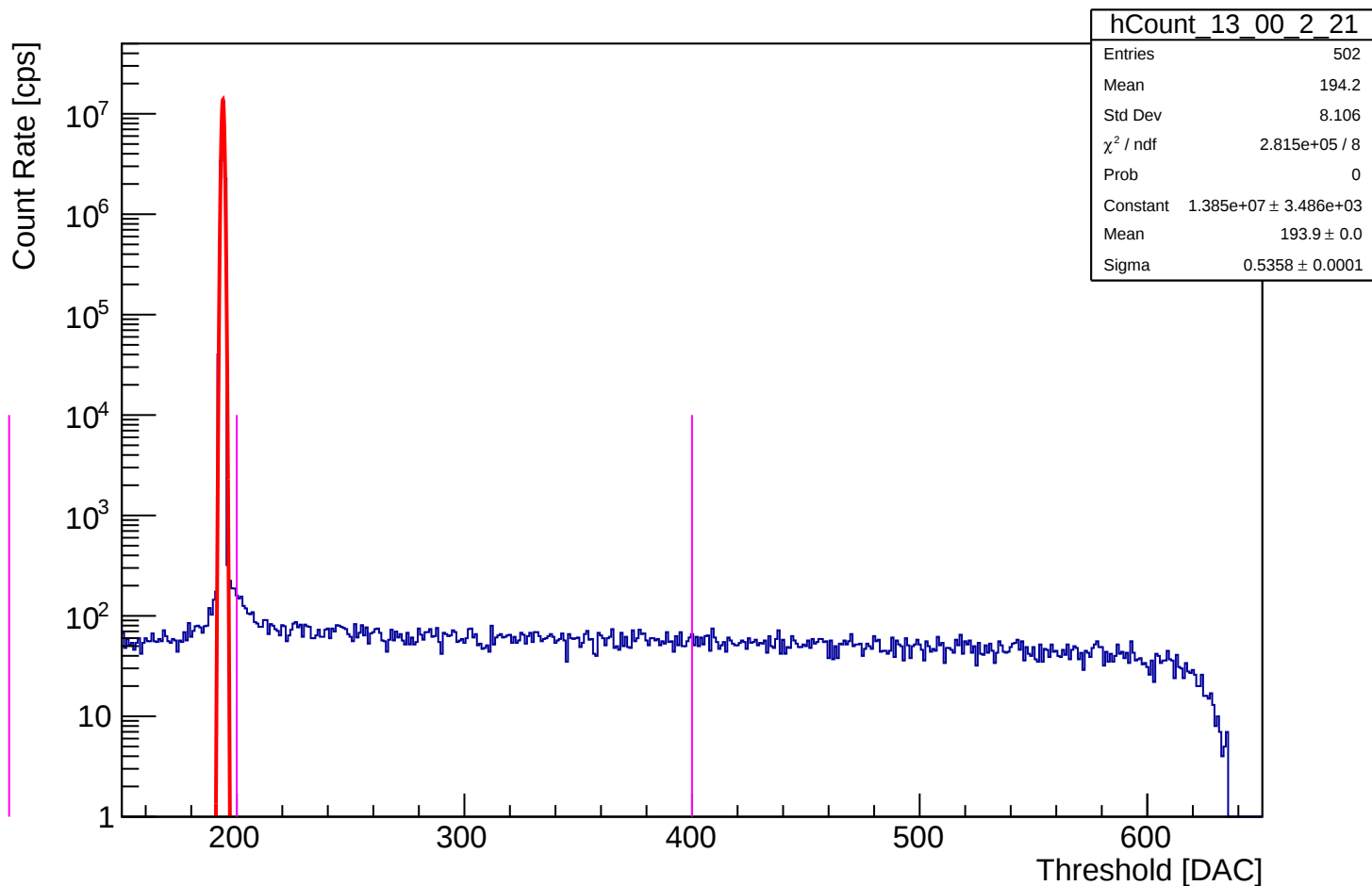
Row 1 Tile 1 Pmt 3 Pixel 16 Slot 13 Fiber 0 Asic 2 Channel 39



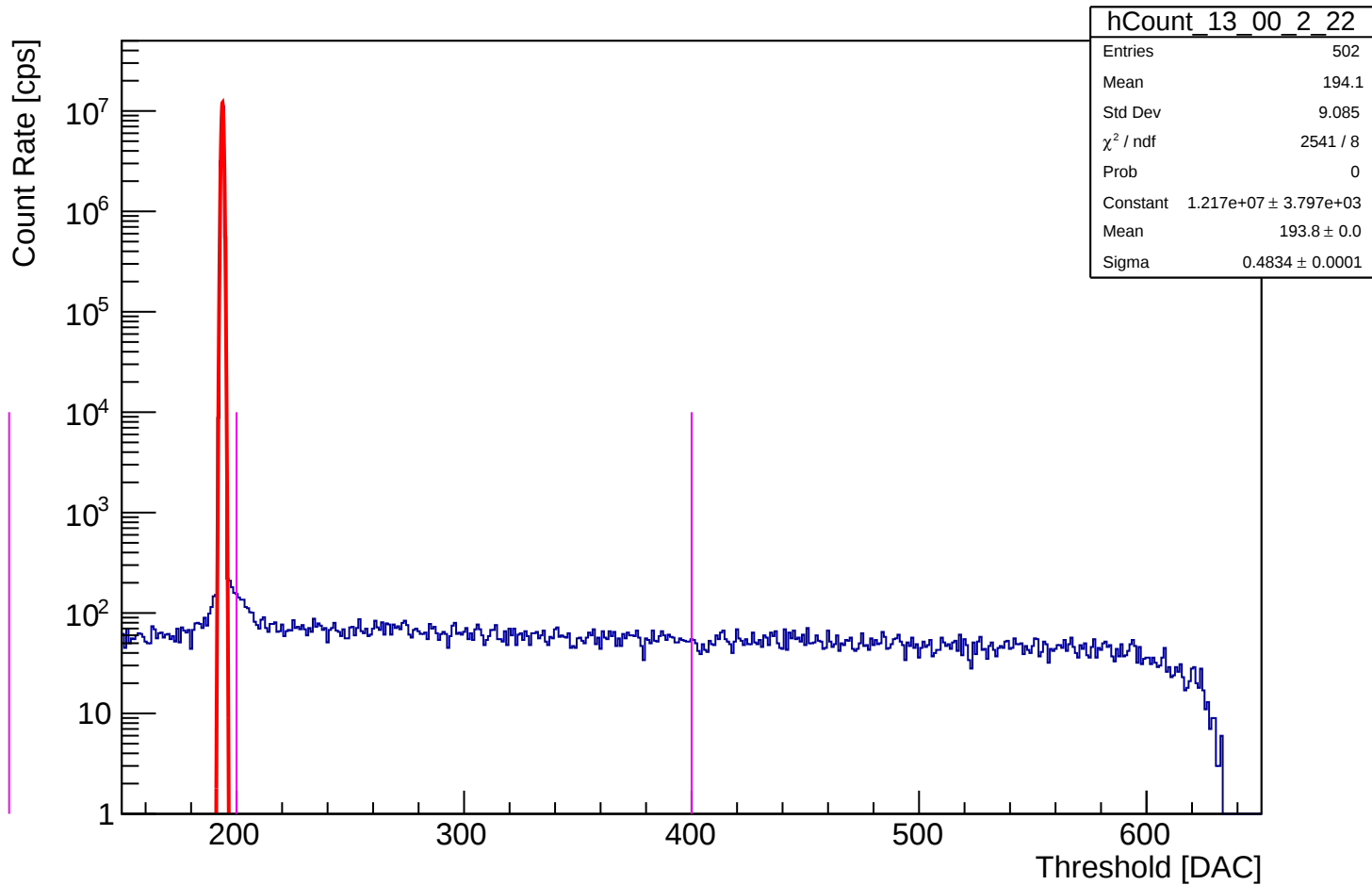
Row 1 Tile 1 Pmt 3 Pixel 17 Slot 13 Fiber 0 Asic 2 Channel 23



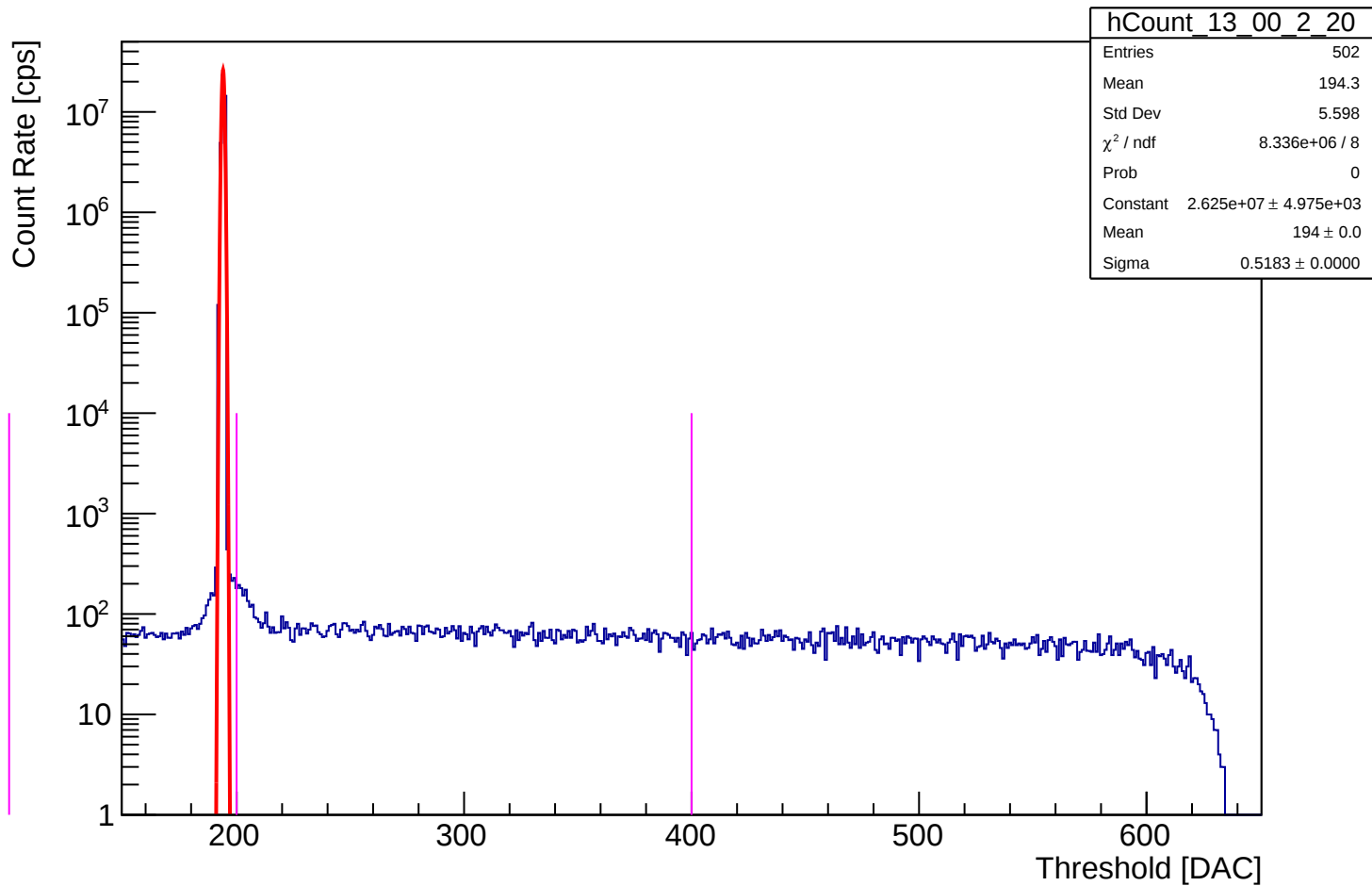
Row 1 Tile 1 Pmt 3 Pixel 18 Slot 13 Fiber 0 Asic 2 Channel 21



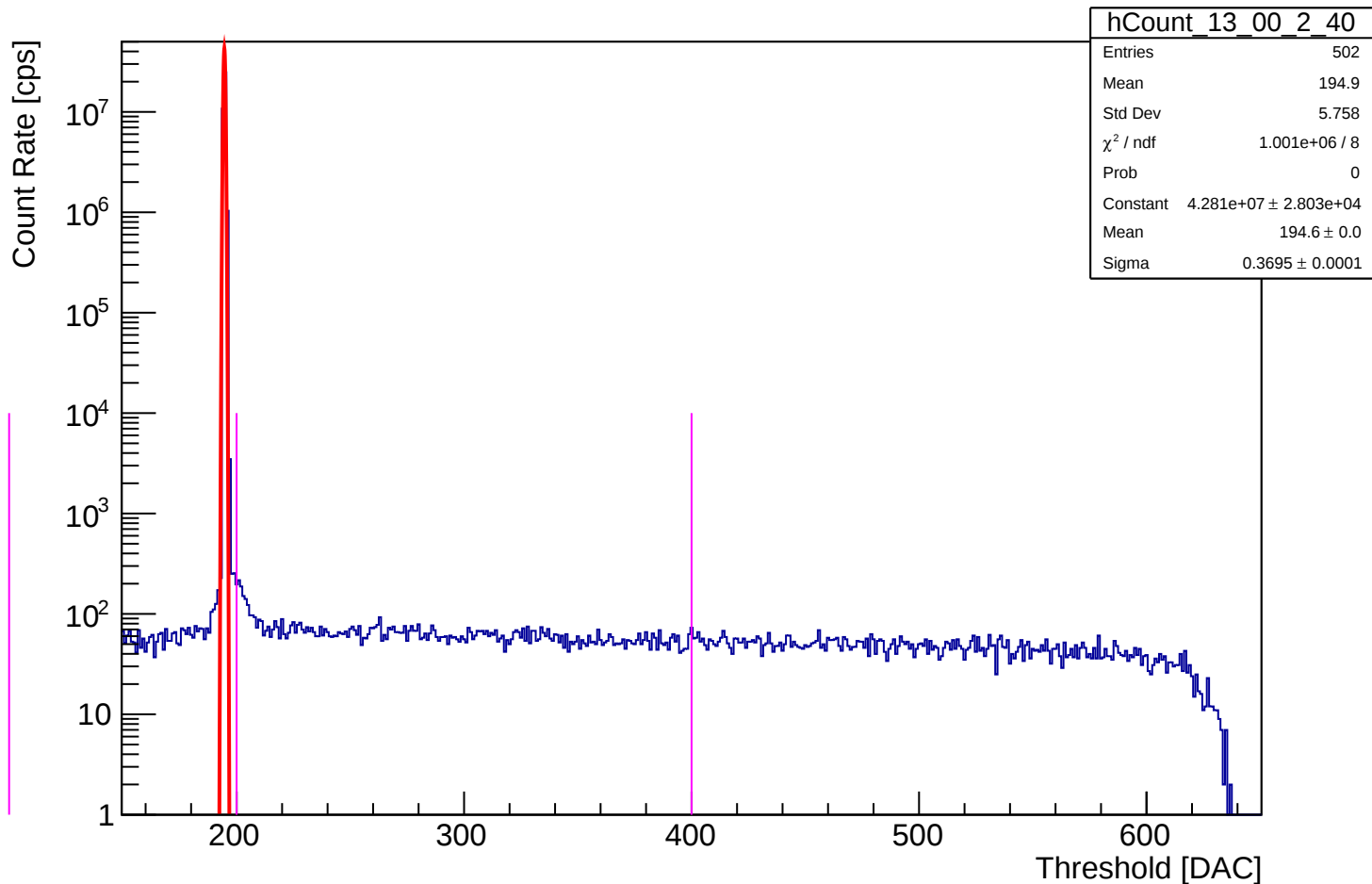
Row 1 Tile 1 Pmt 3 Pixel 19 Slot 13 Fiber 0 Asic 2 Channel 22



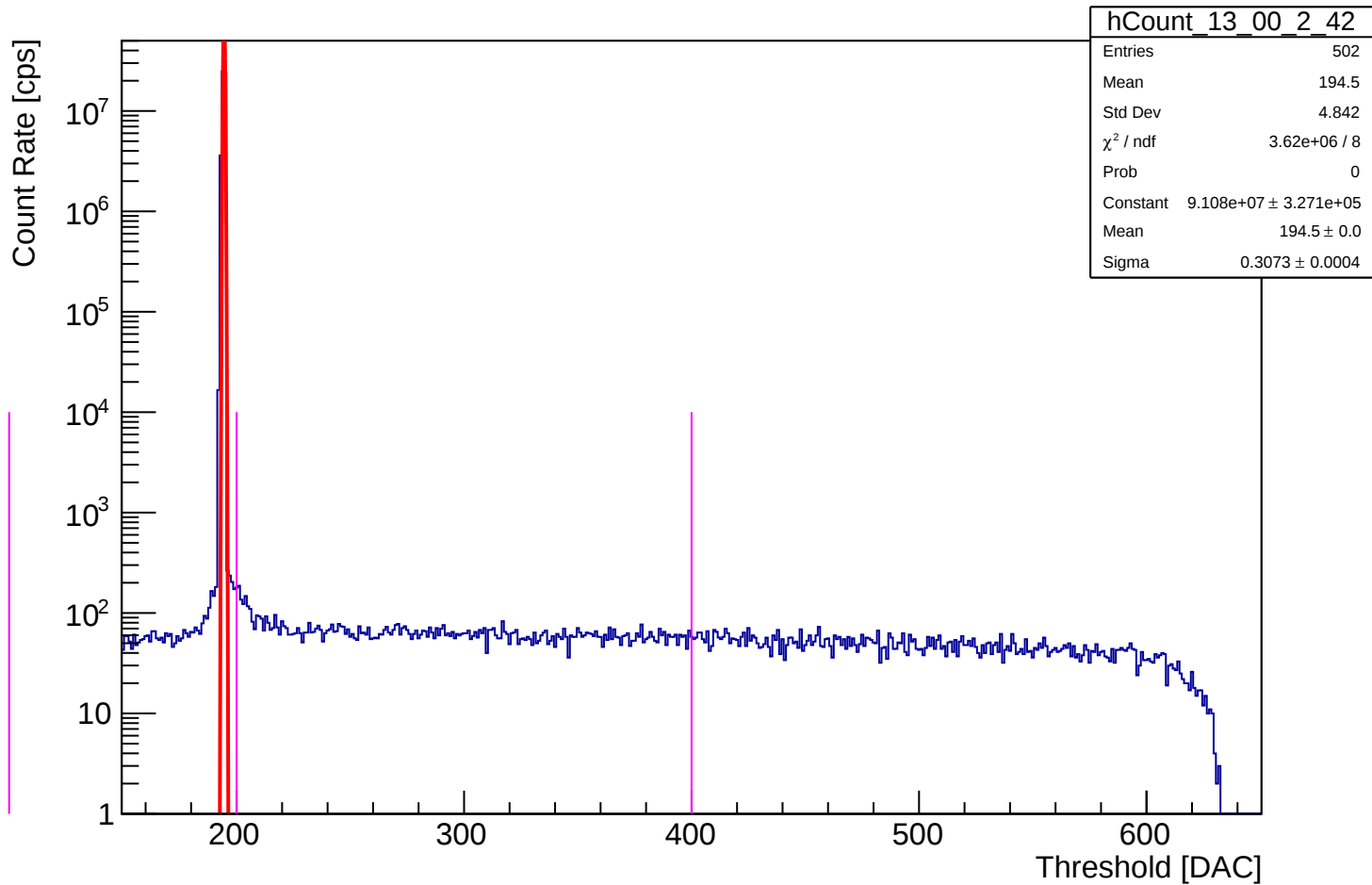
Row 1 Tile 1 Pmt 3 Pixel 20 Slot 13 Fiber 0 Asic 2 Channel 20

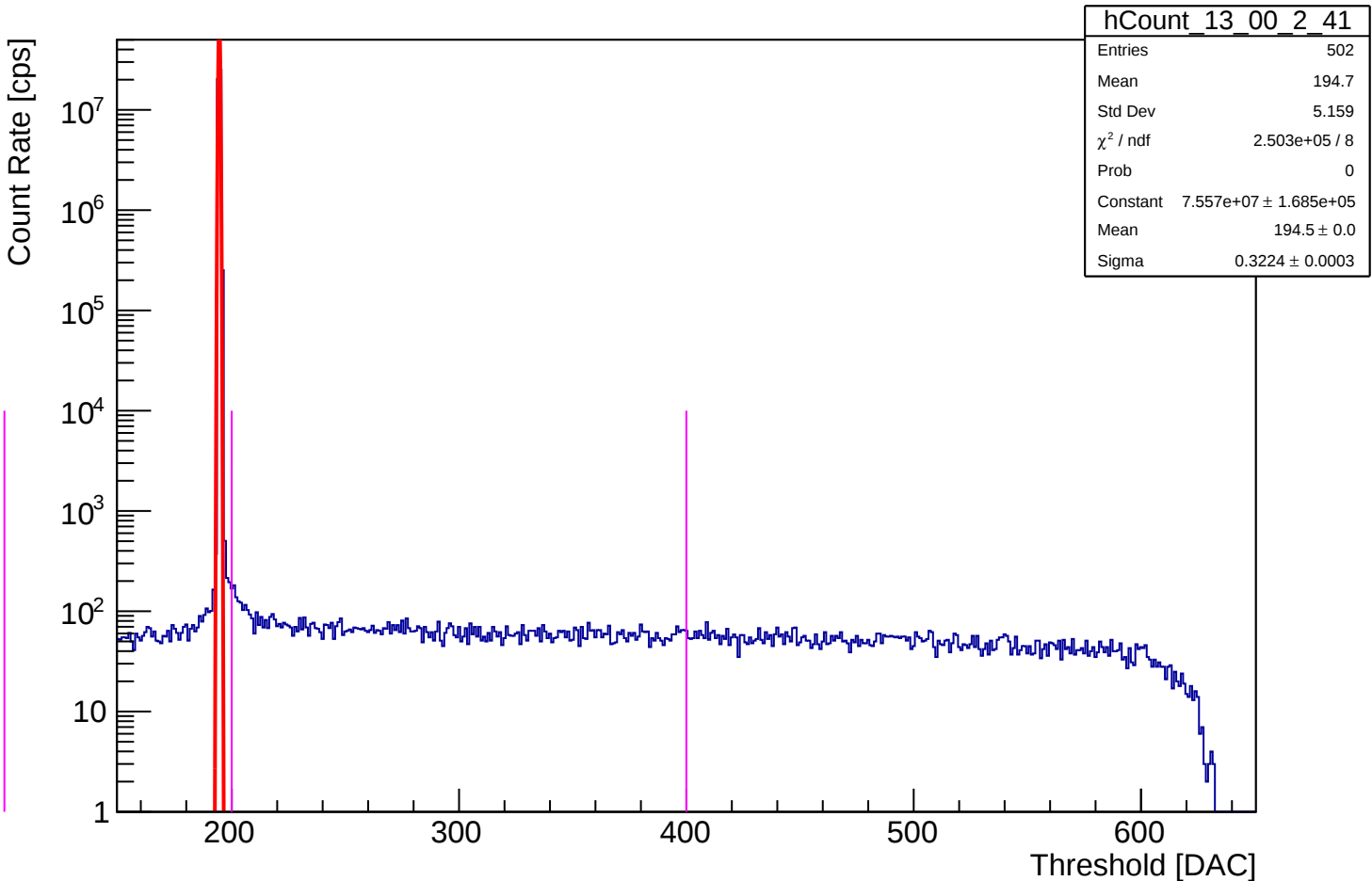


Row 1 Tile 1 Pmt 3 Pixel 21 Slot 13 Fiber 0 Asic 2 Channel 40

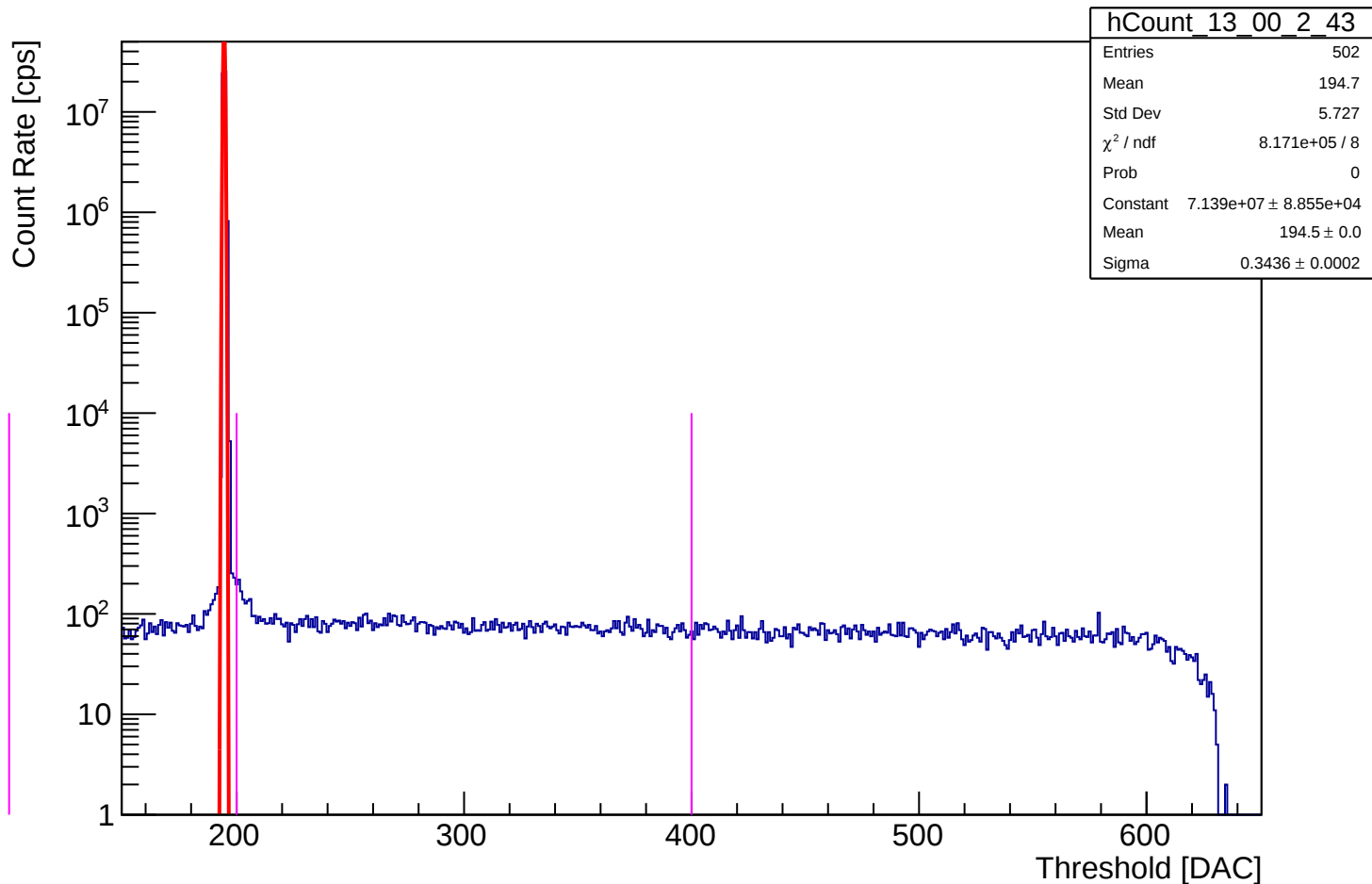


Row 1 Tile 1 Pmt 3 Pixel 22 Slot 13 Fiber 0 Asic 2 Channel 42

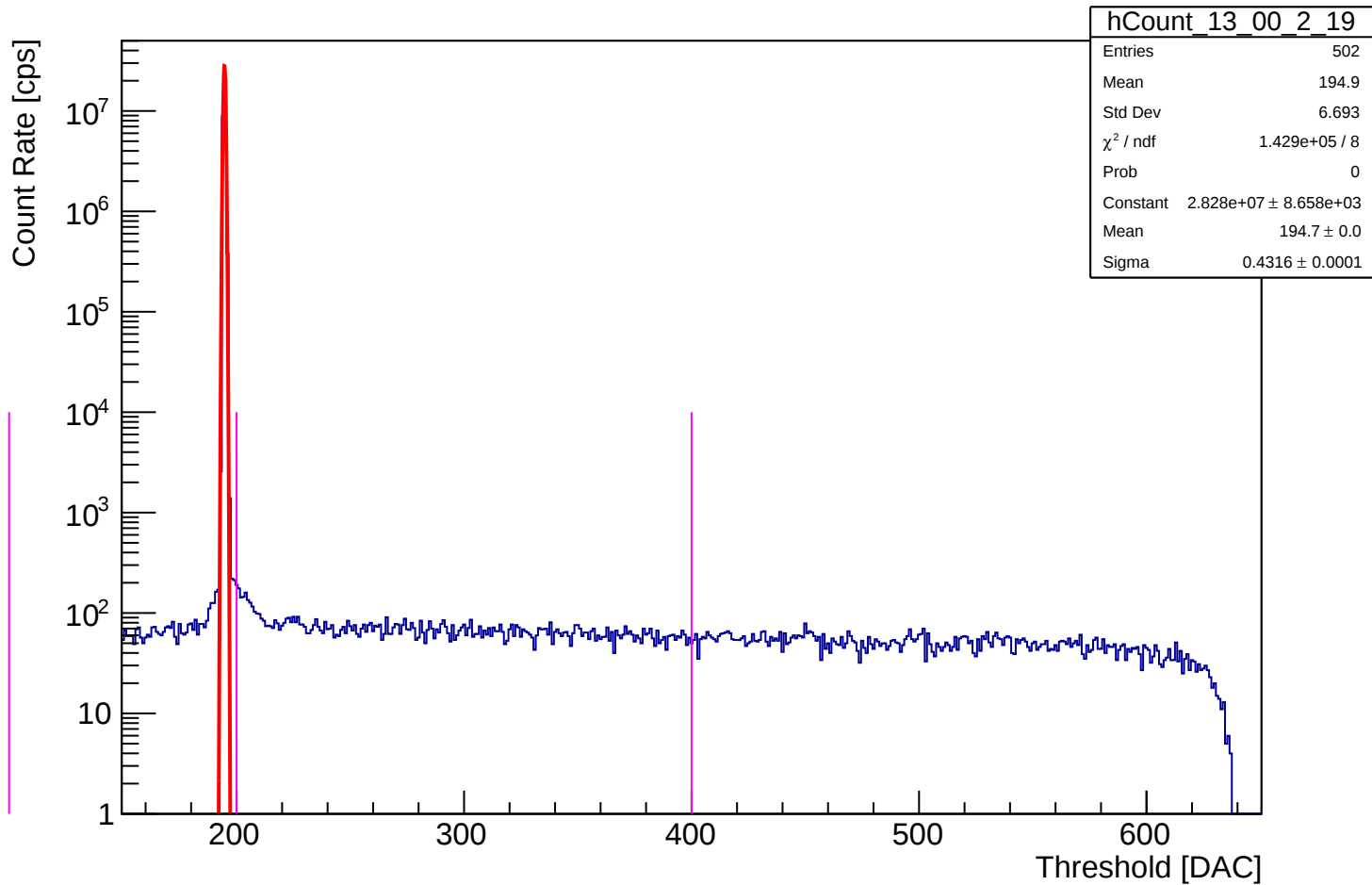




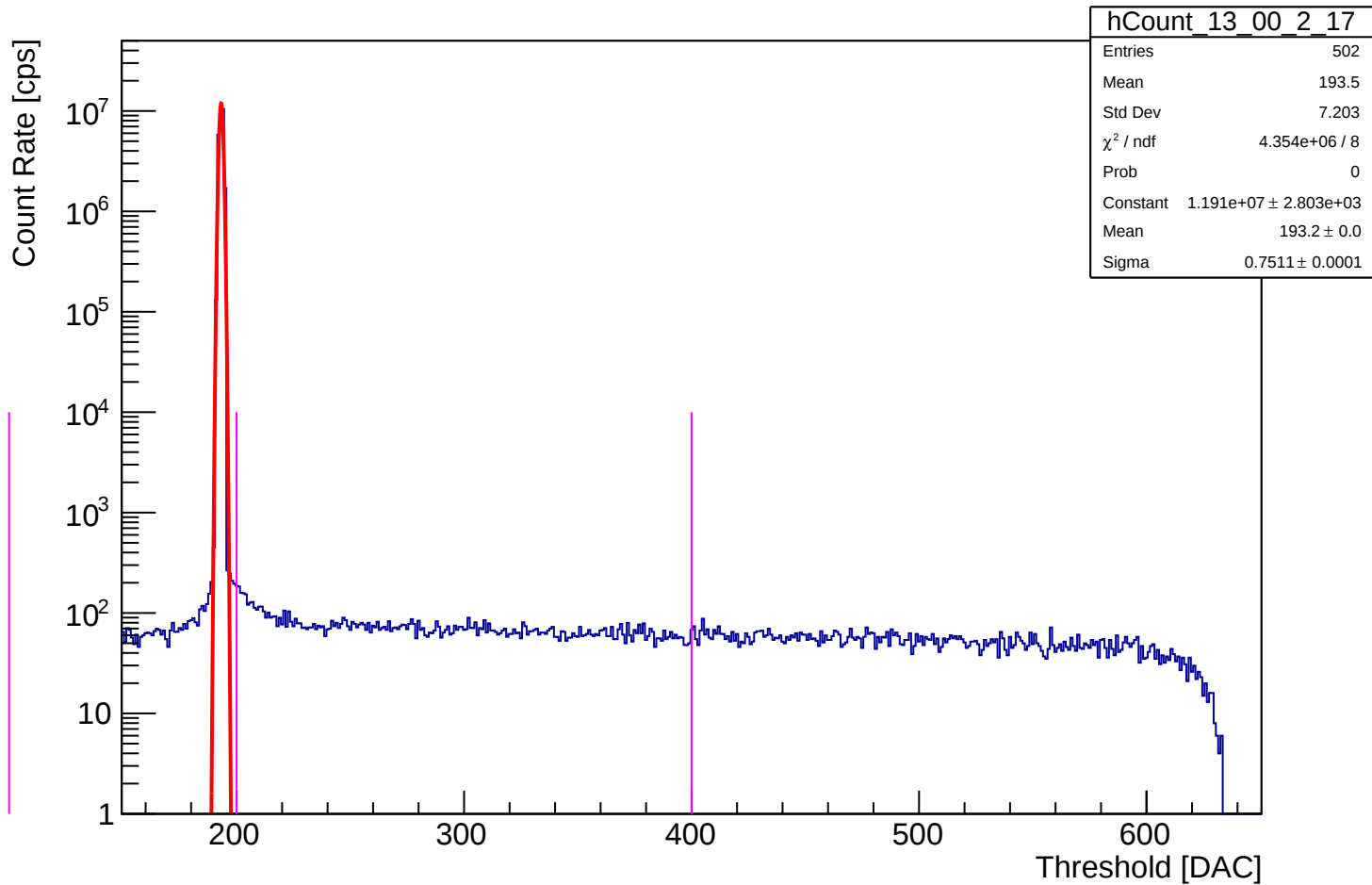
Row 1 Tile 1 Pmt 3 Pixel 24 Slot 13 Fiber 0 Asic 2 Channel 43



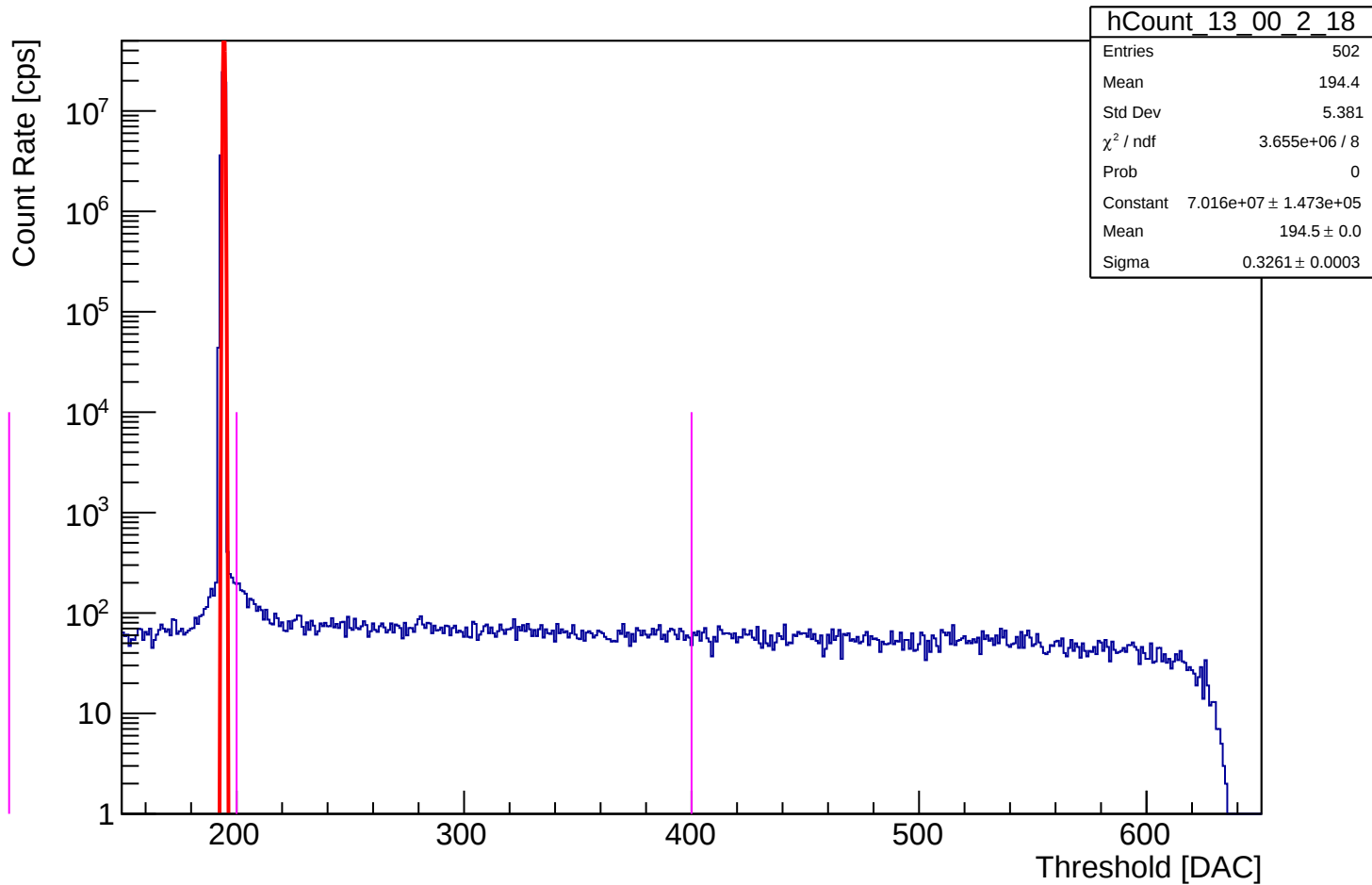
Row 1 Tile 1 Pmt 3 Pixel 25 Slot 13 Fiber 0 Asic 2 Channel 19



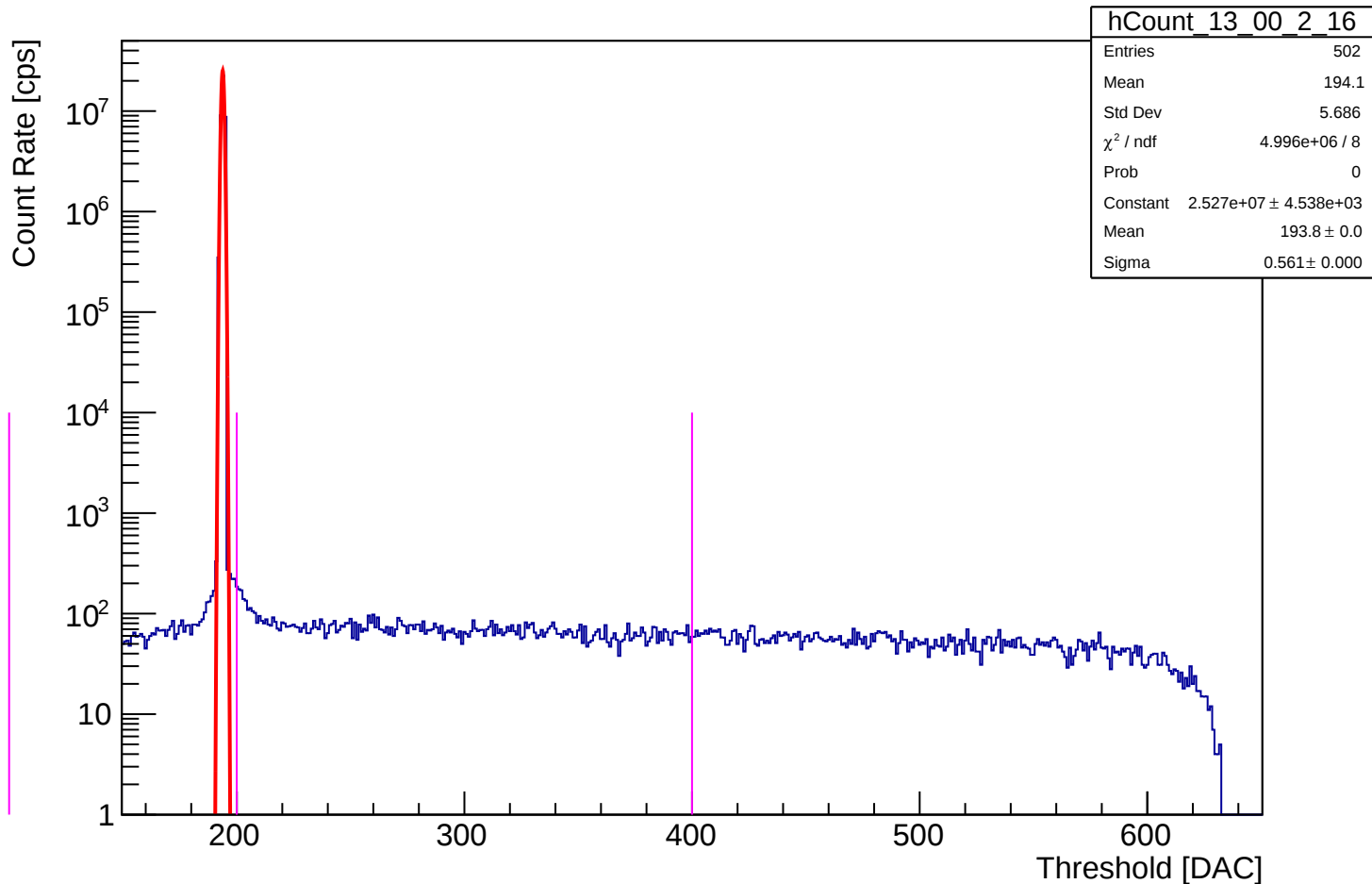
Row 1 Tile 1 Pmt 3 Pixel 26 Slot 13 Fiber 0 Asic 2 Channel 17



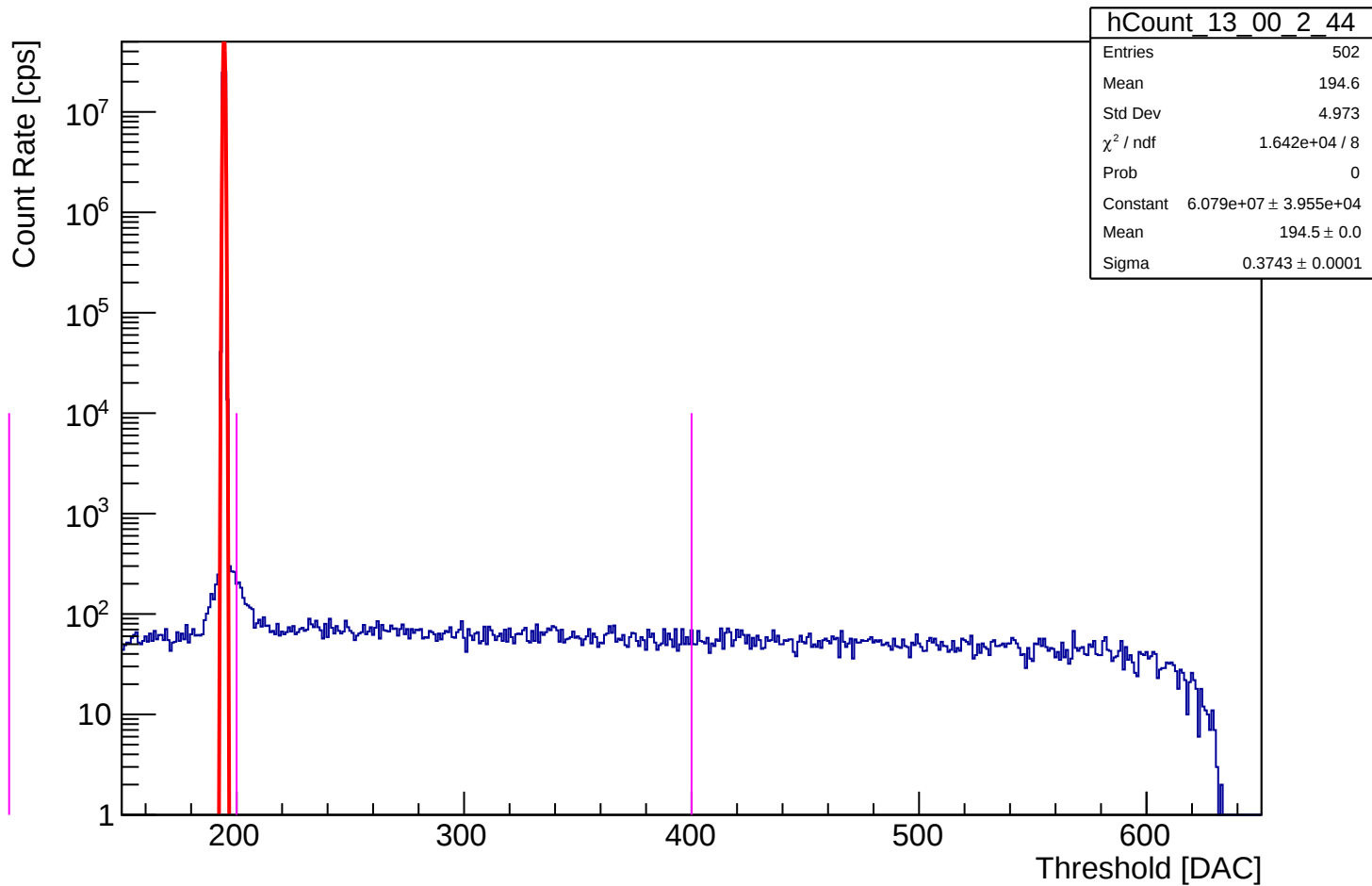
Row 1 Tile 1 Pmt 3 Pixel 27 Slot 13 Fiber 0 Asic 2 Channel 18



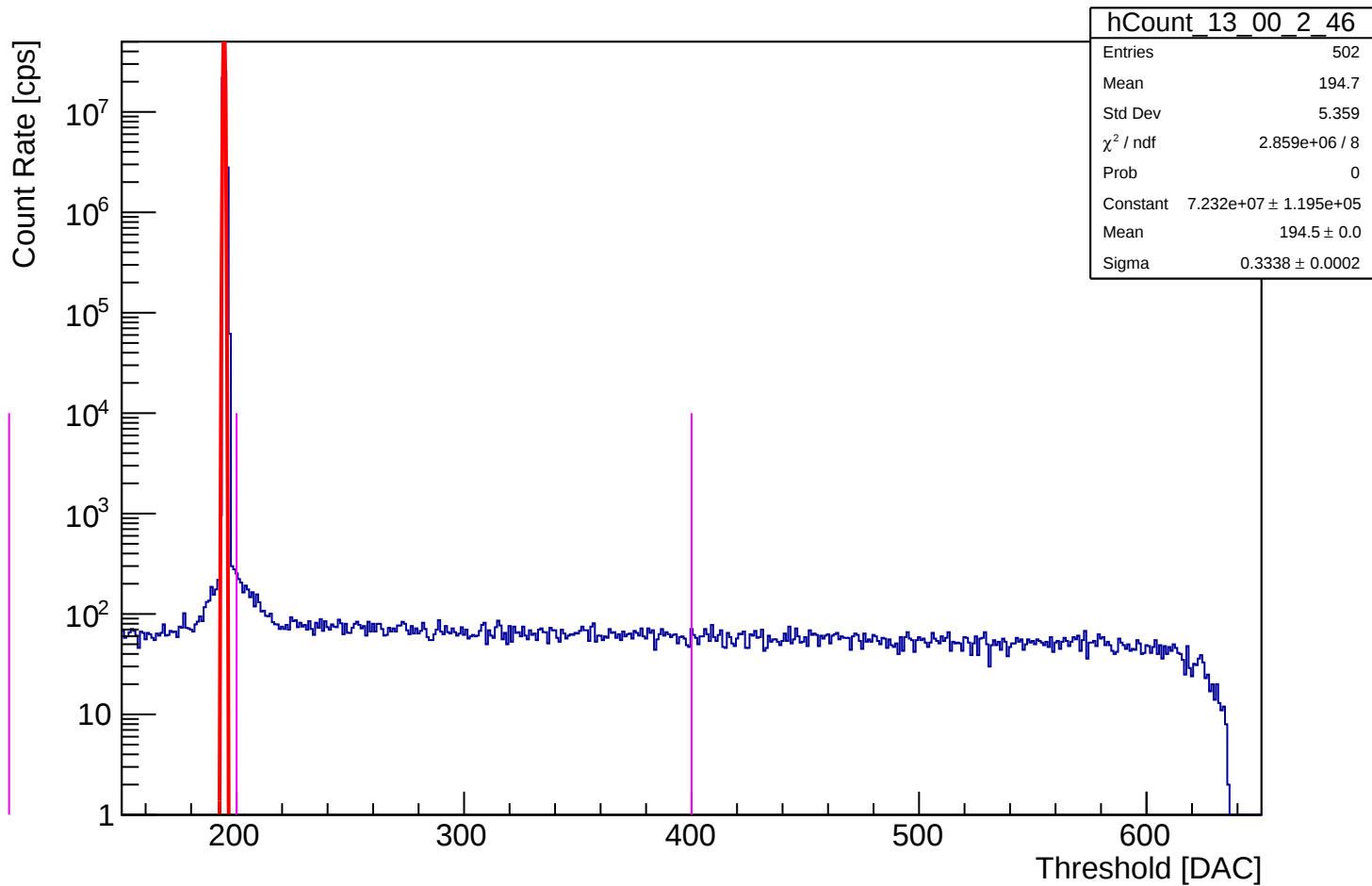
Row 1 Tile 1 Pmt 3 Pixel 28 Slot 13 Fiber 0 Asic 2 Channel 16



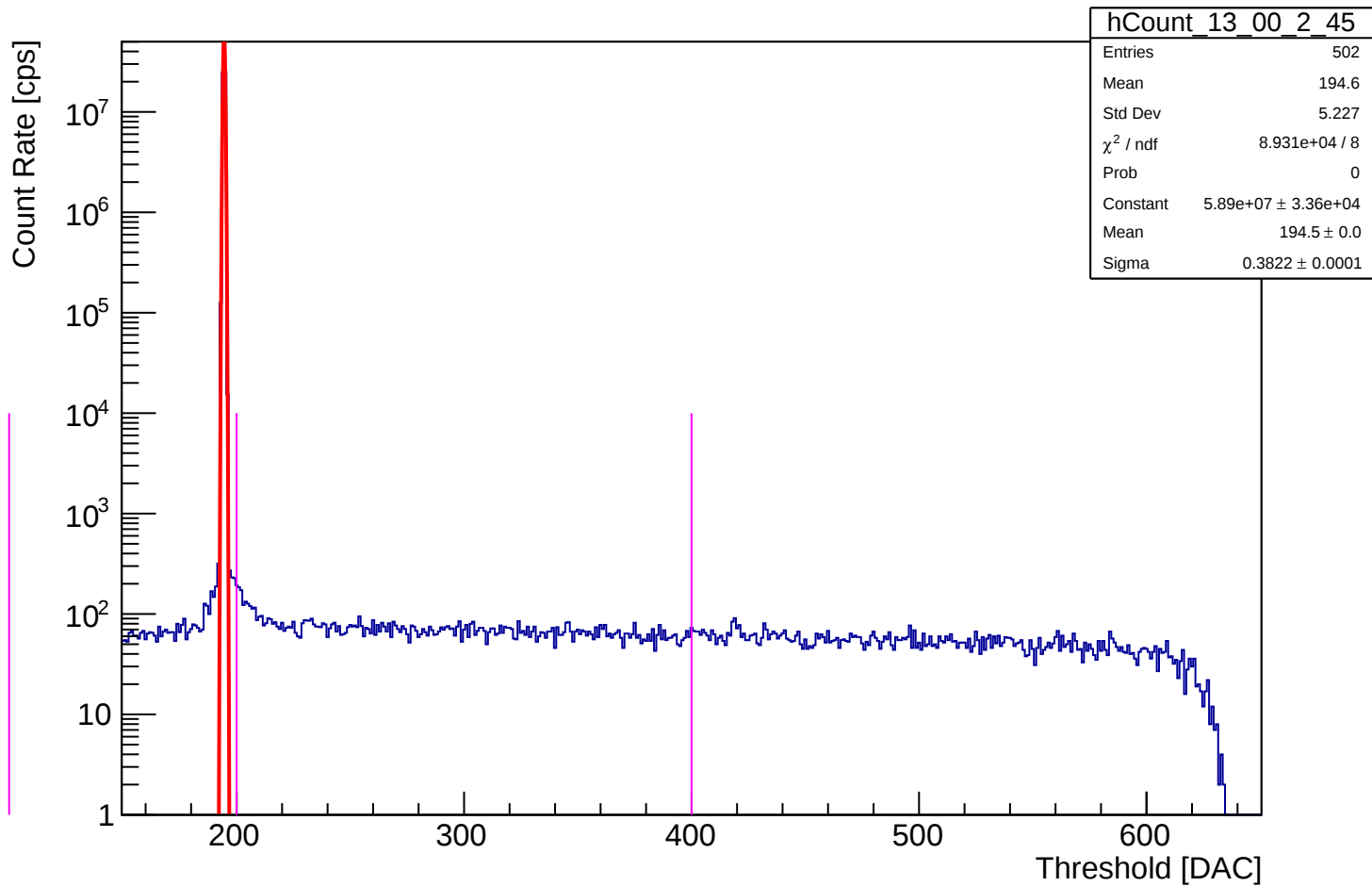
Row 1 Tile 1 Pmt 3 Pixel 29 Slot 13 Fiber 0 Asic 2 Channel 44



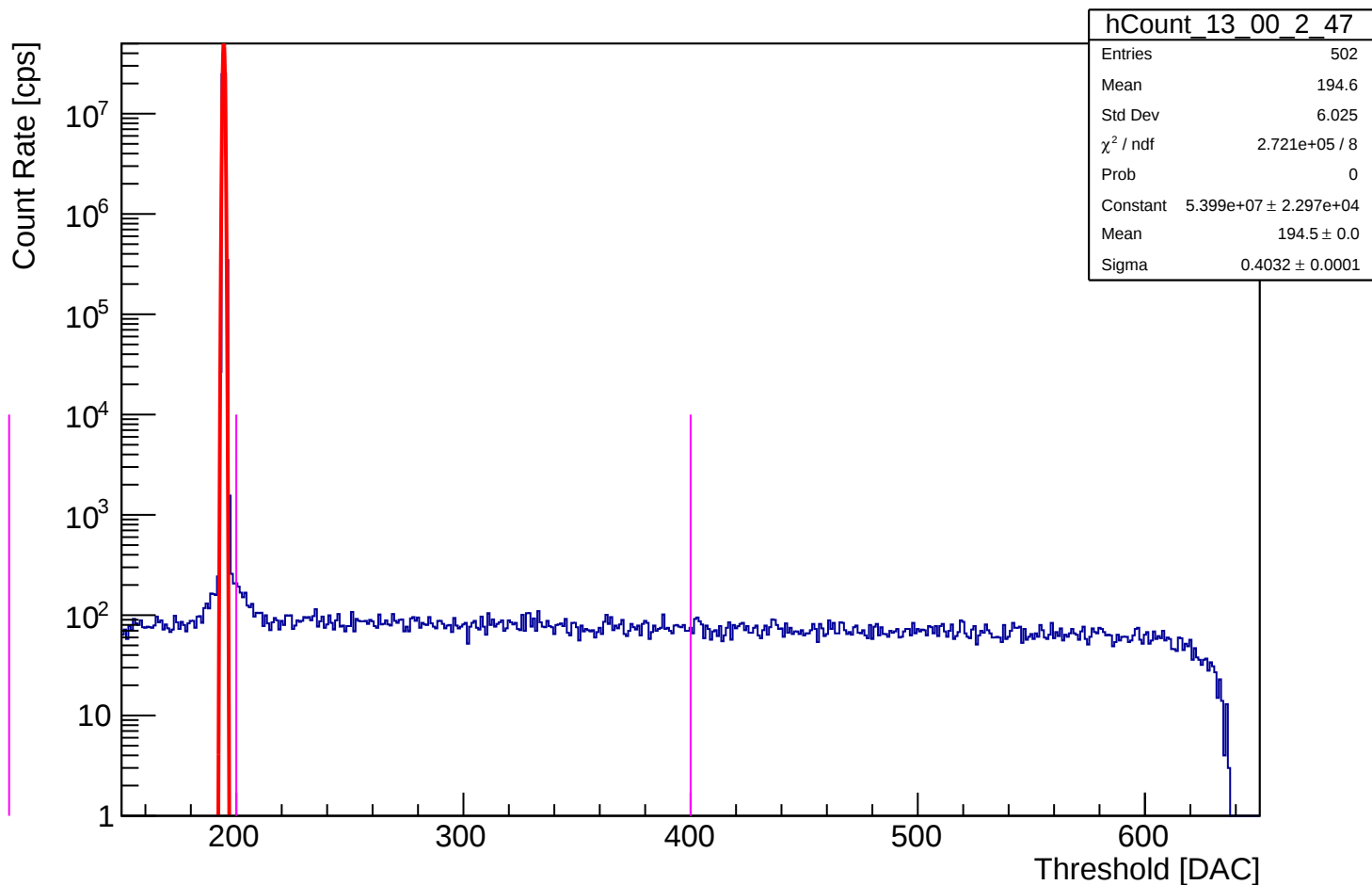
Row 1 Tile 1 Pmt 3 Pixel 30 Slot 13 Fiber 0 Asic 2 Channel 46



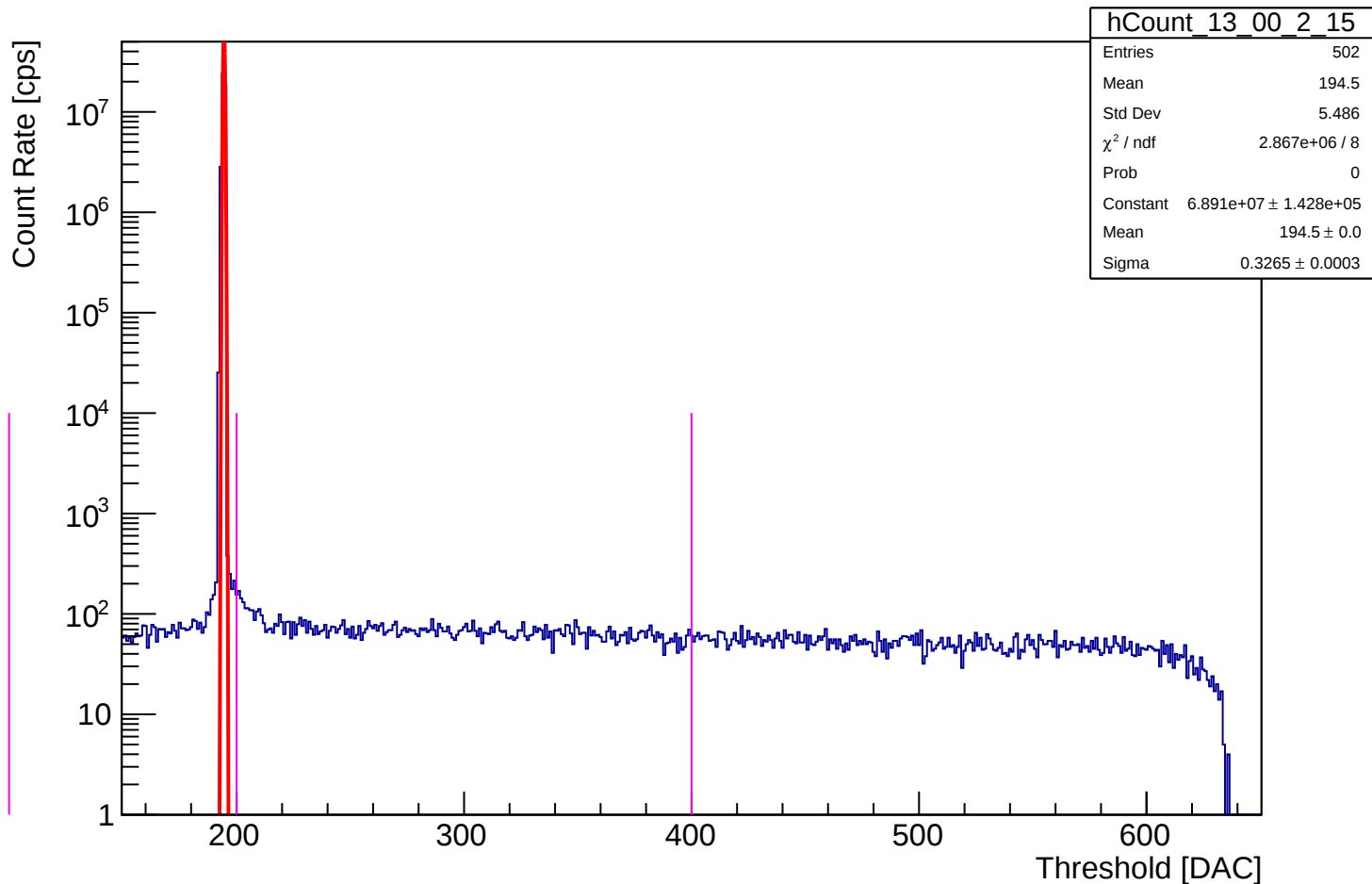
Row 1 Tile 1 Pmt 3 Pixel 31 Slot 13 Fiber 0 Asic 2 Channel 45



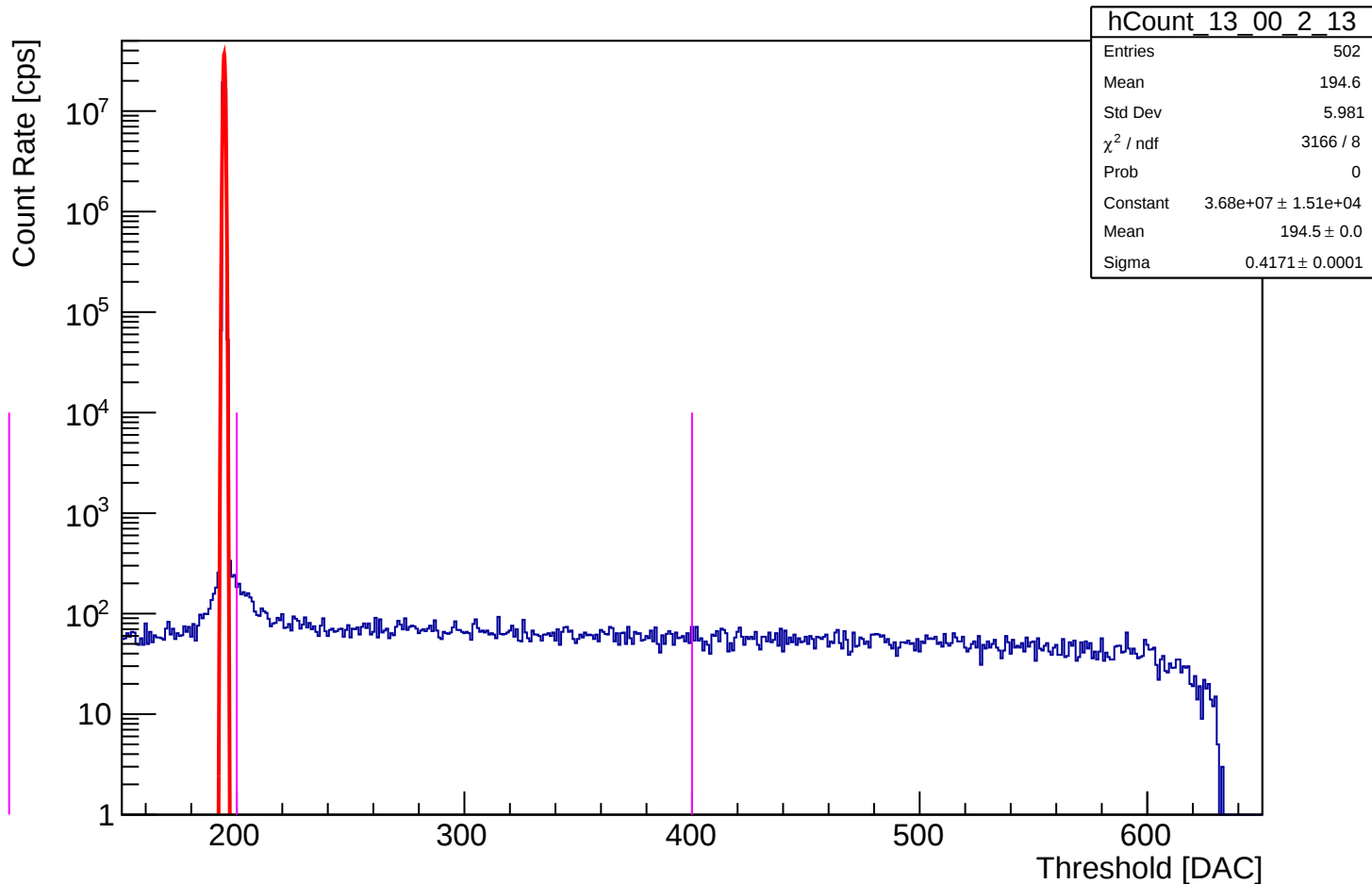
Row 1 Tile 1 Pmt 3 Pixel 32 Slot 13 Fiber 0 Asic 2 Channel 47



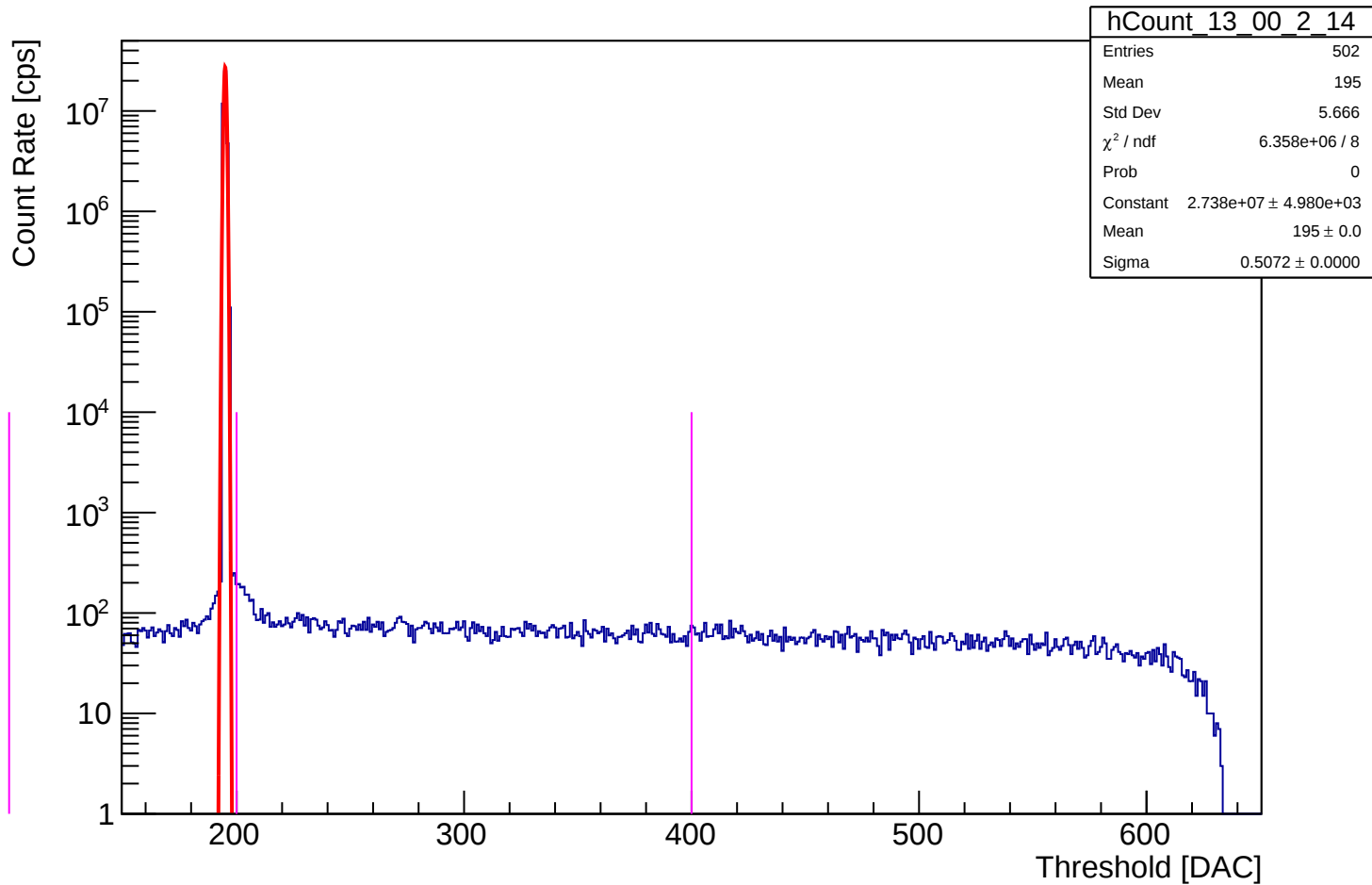
Row 1 Tile 1 Pmt 3 Pixel 33 Slot 13 Fiber 0 Asic 2 Channel 15



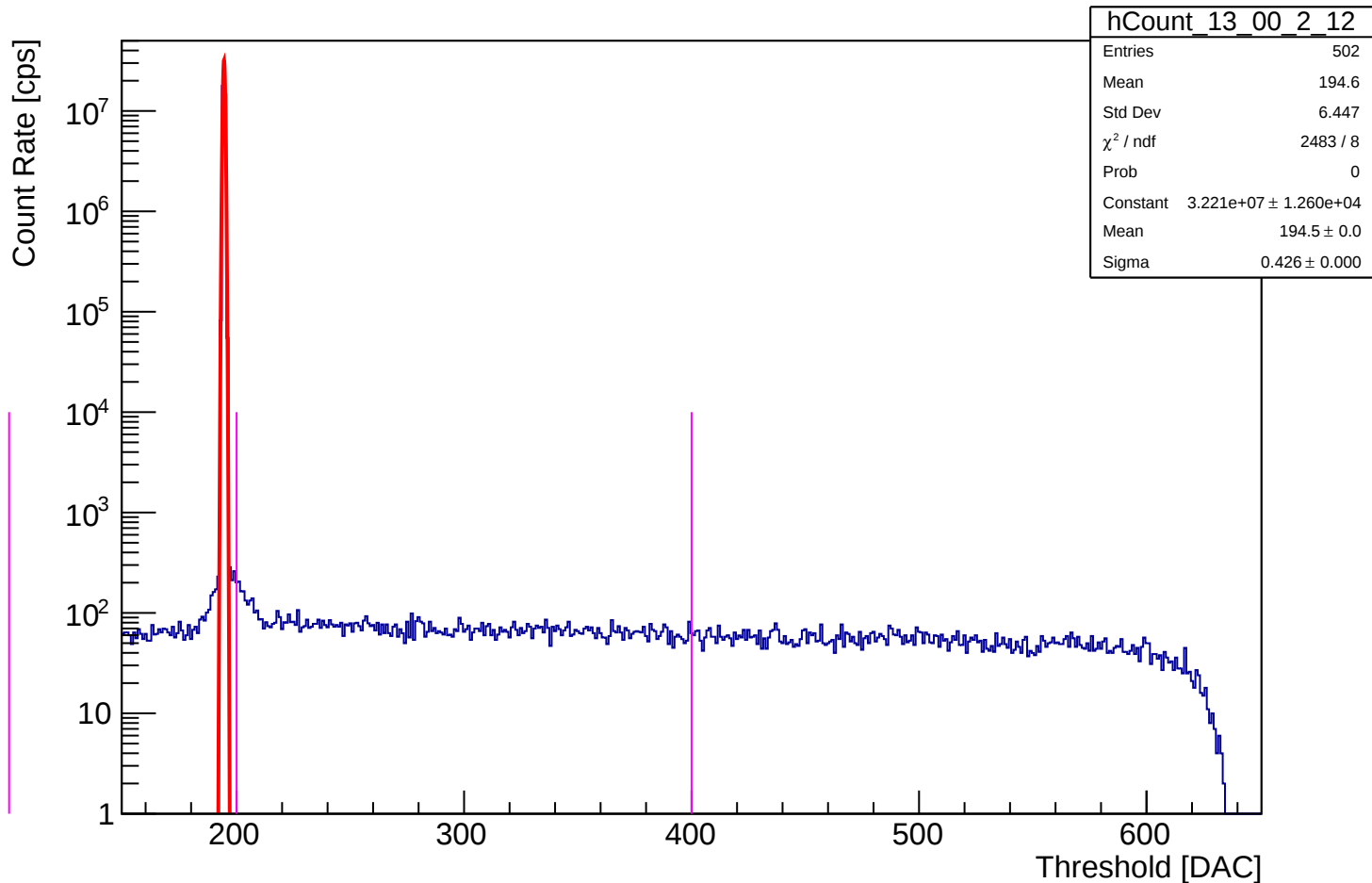
Row 1 Tile 1 Pmt 3 Pixel 34 Slot 13 Fiber 0 Asic 2 Channel 13



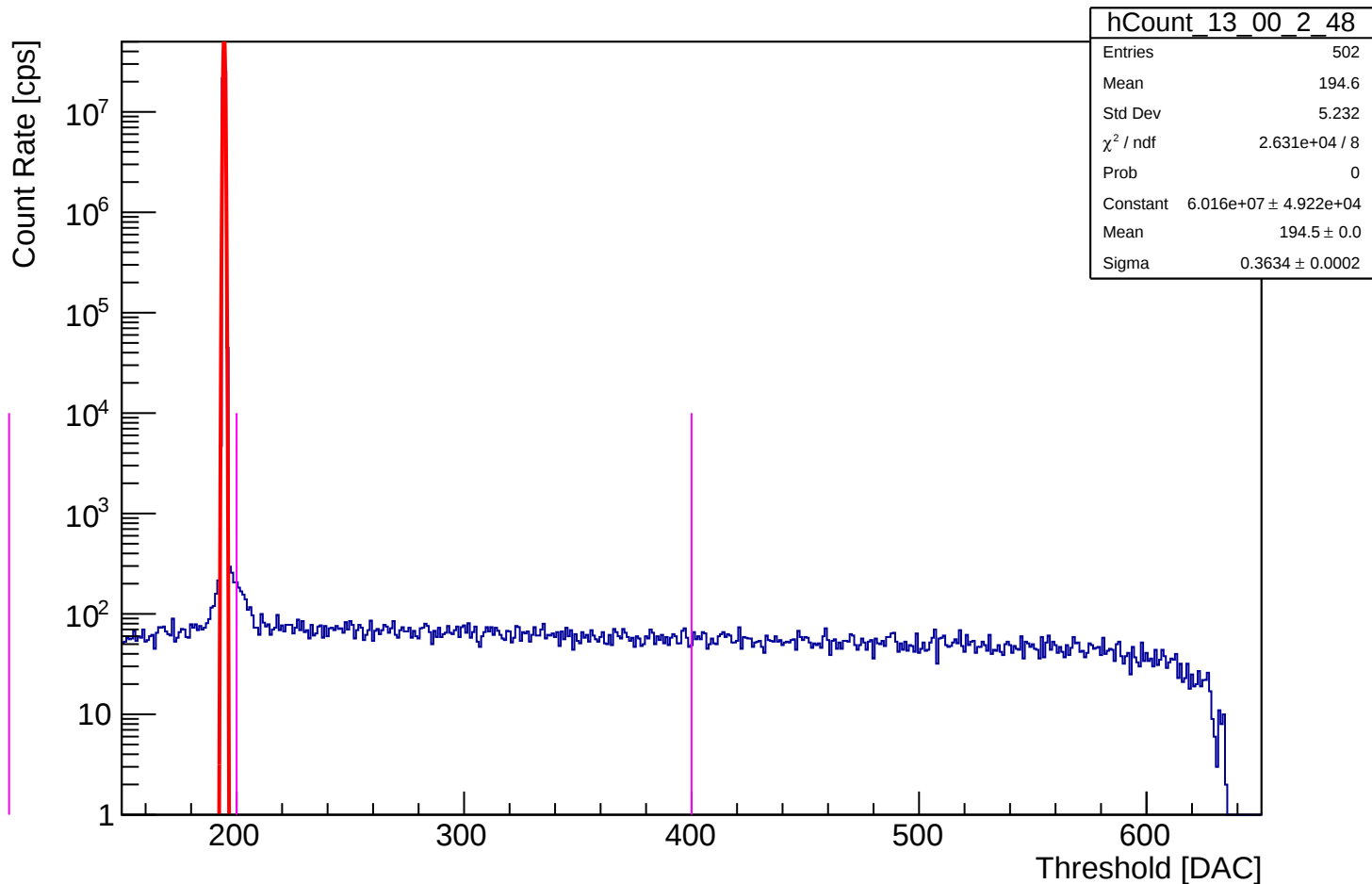
Row 1 Tile 1 Pmt 3 Pixel 35 Slot 13 Fiber 0 Asic 2 Channel 14



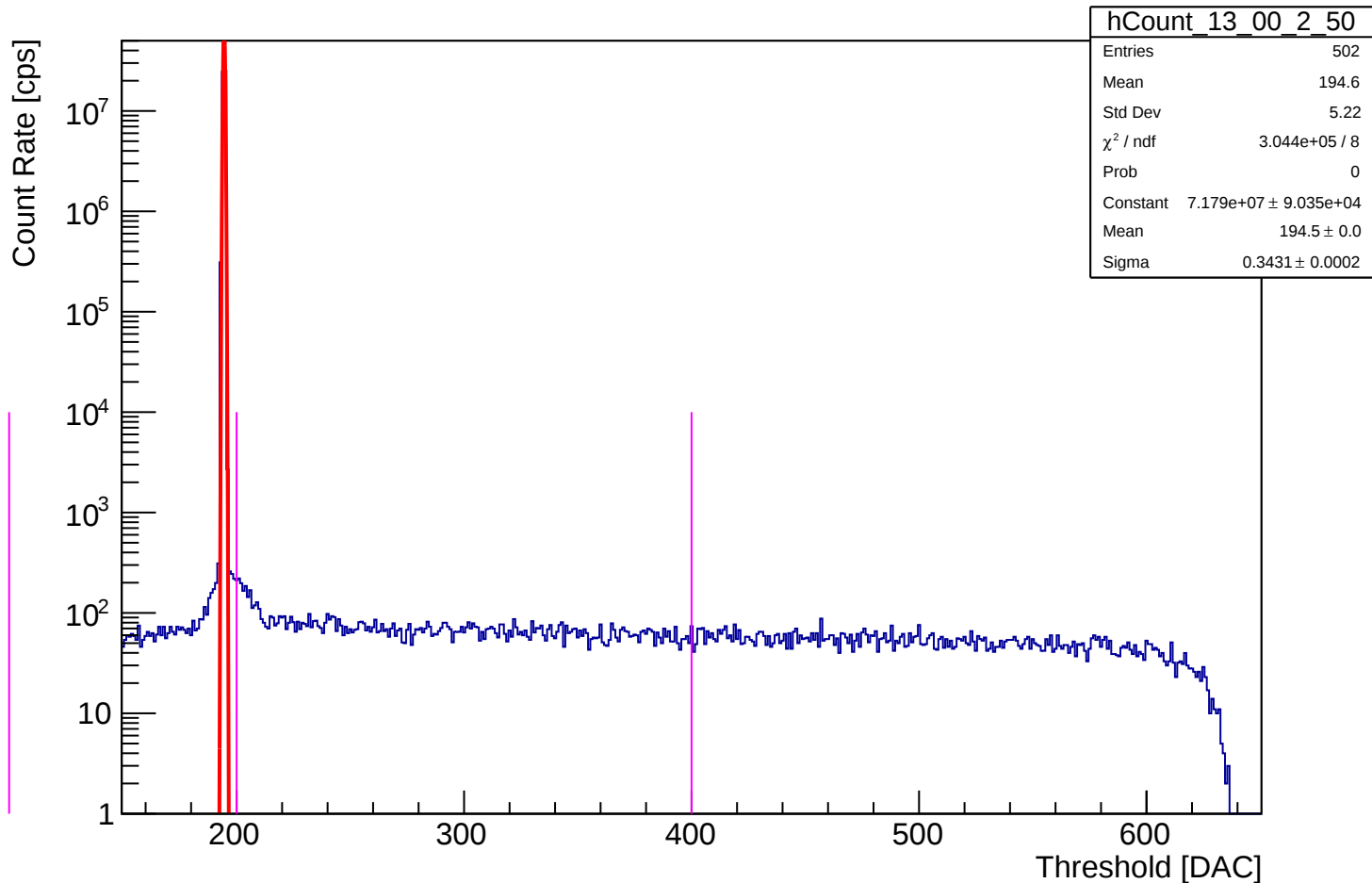
Row 1 Tile 1 Pmt 3 Pixel 36 Slot 13 Fiber 0 Asic 2 Channel 12



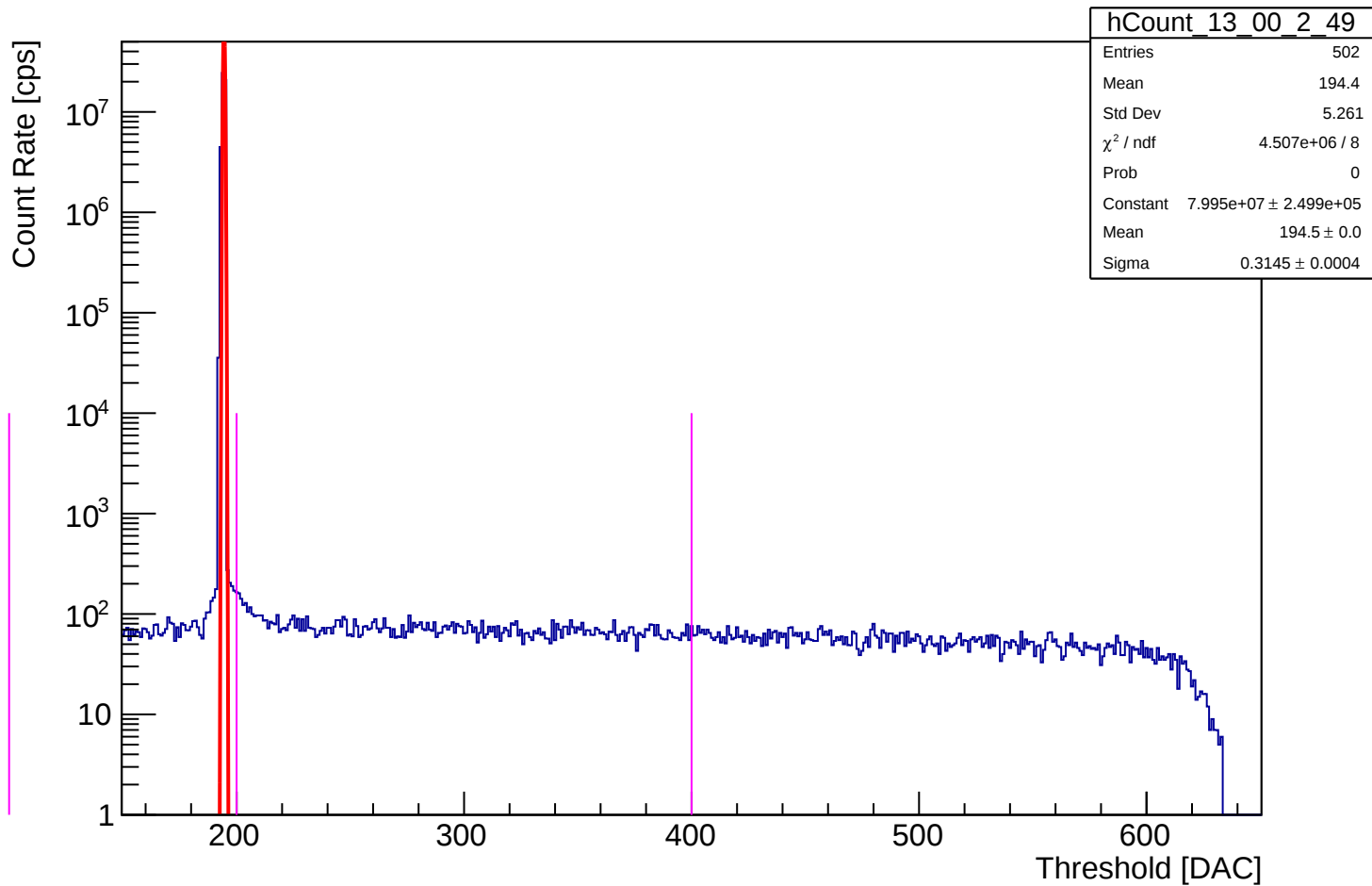
Row 1 Tile 1 Pmt 3 Pixel 37 Slot 13 Fiber 0 Asic 2 Channel 48



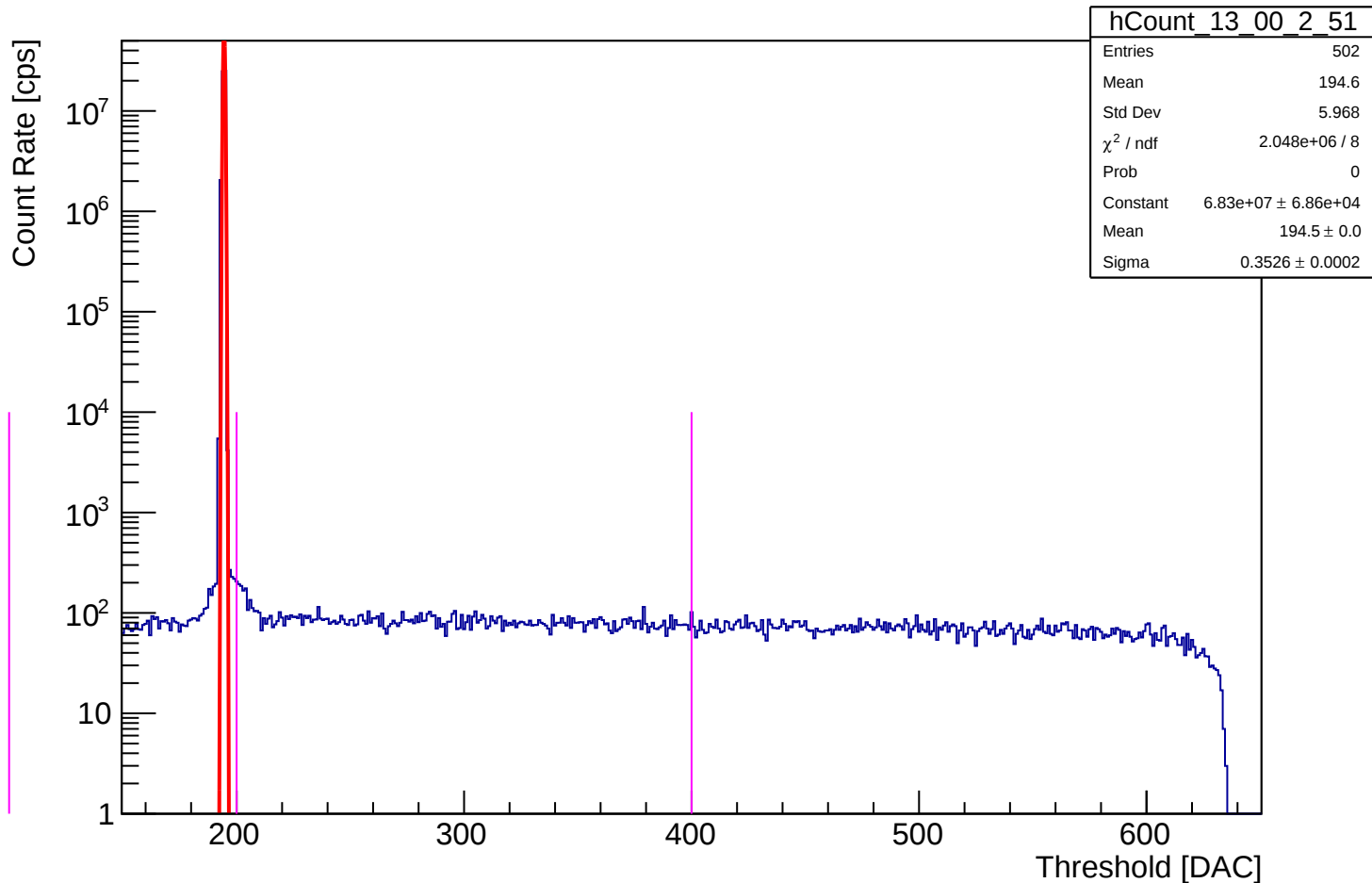
Row 1 Tile 1 Pmt 3 Pixel 38 Slot 13 Fiber 0 Asic 2 Channel 50



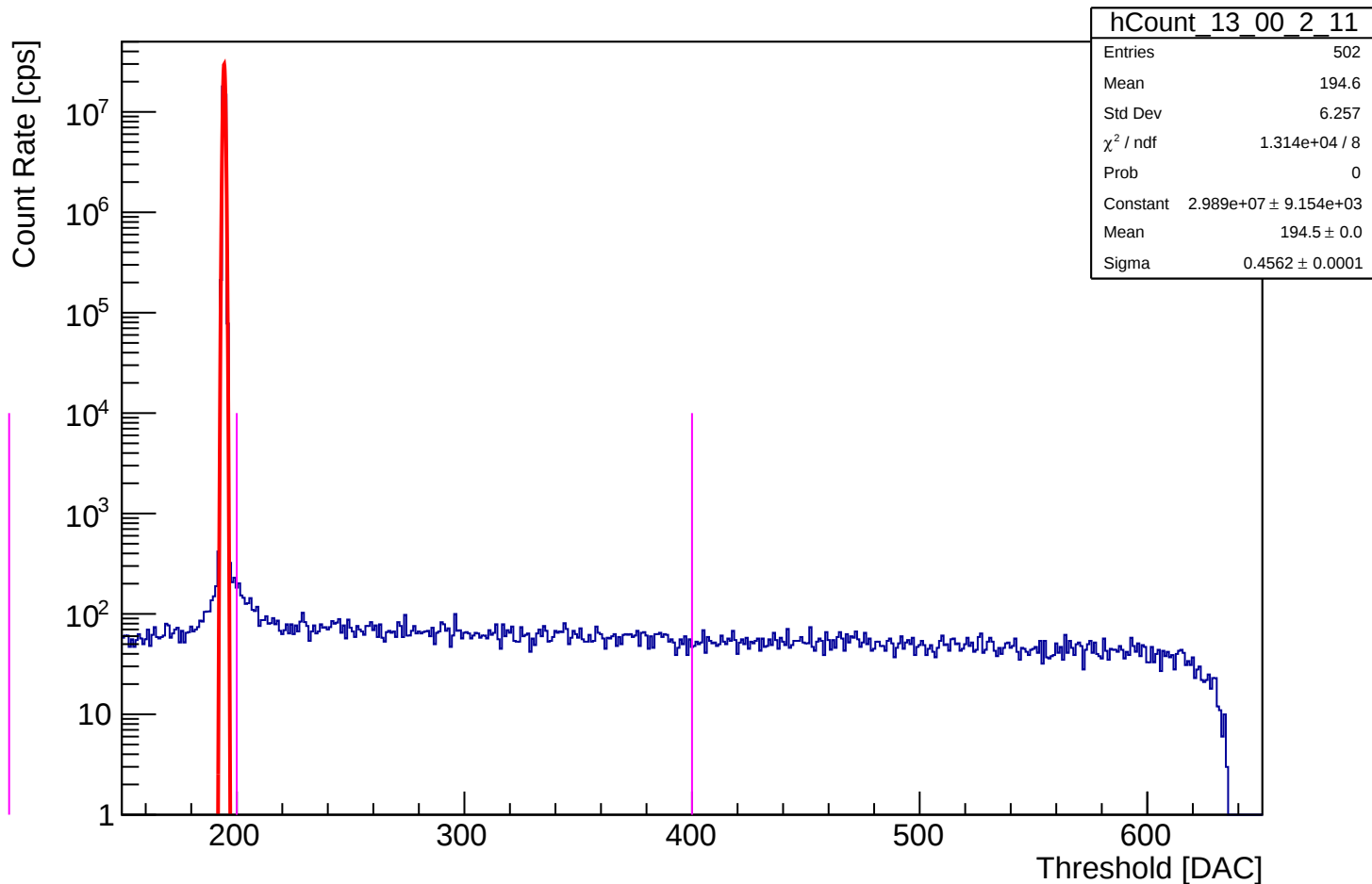
Row 1 Tile 1 Pmt 3 Pixel 39 Slot 13 Fiber 0 Asic 2 Channel 49

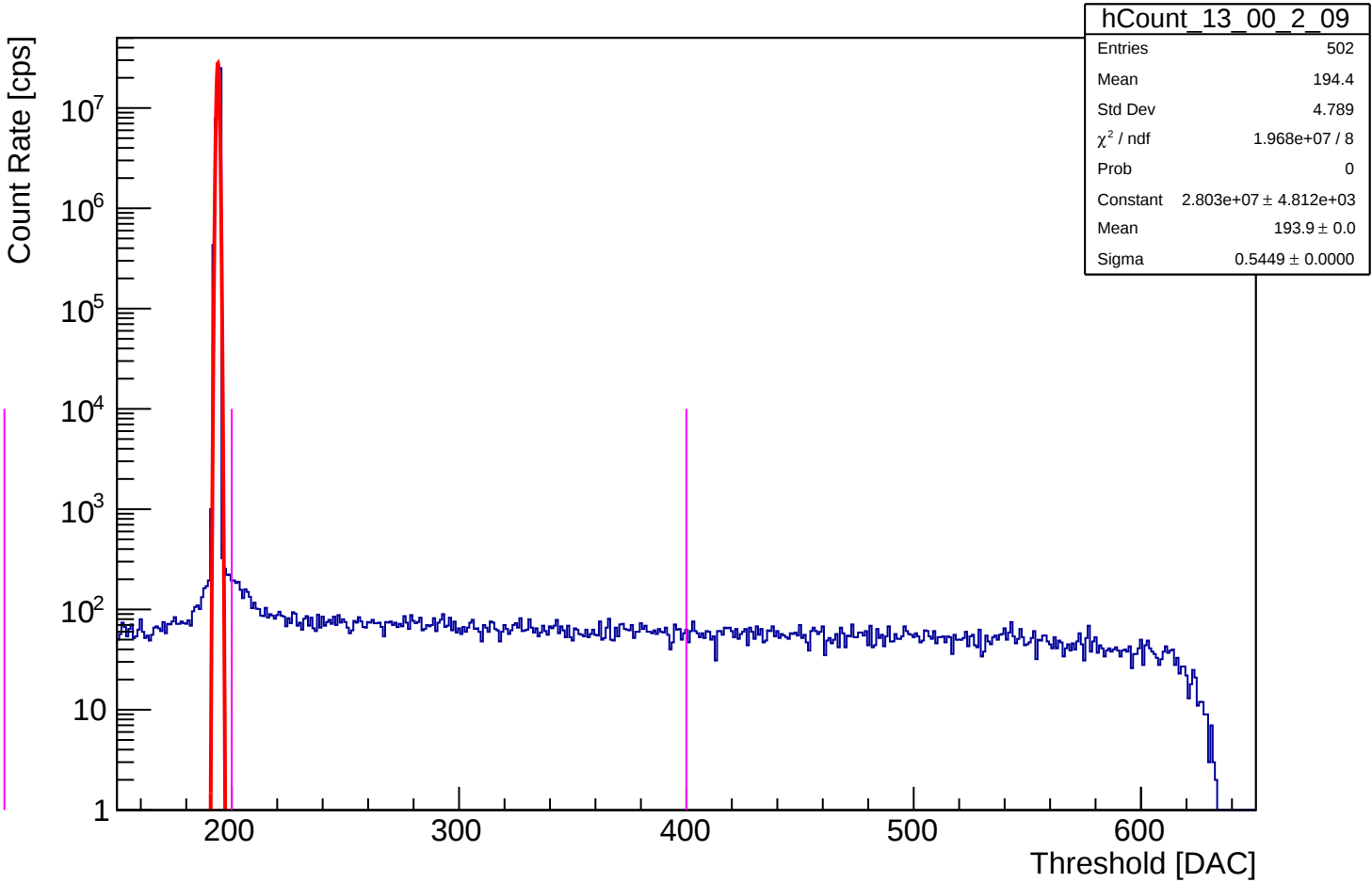


Row 1 Tile 1 Pmt 3 Pixel 40 Slot 13 Fiber 0 Asic 2 Channel 51

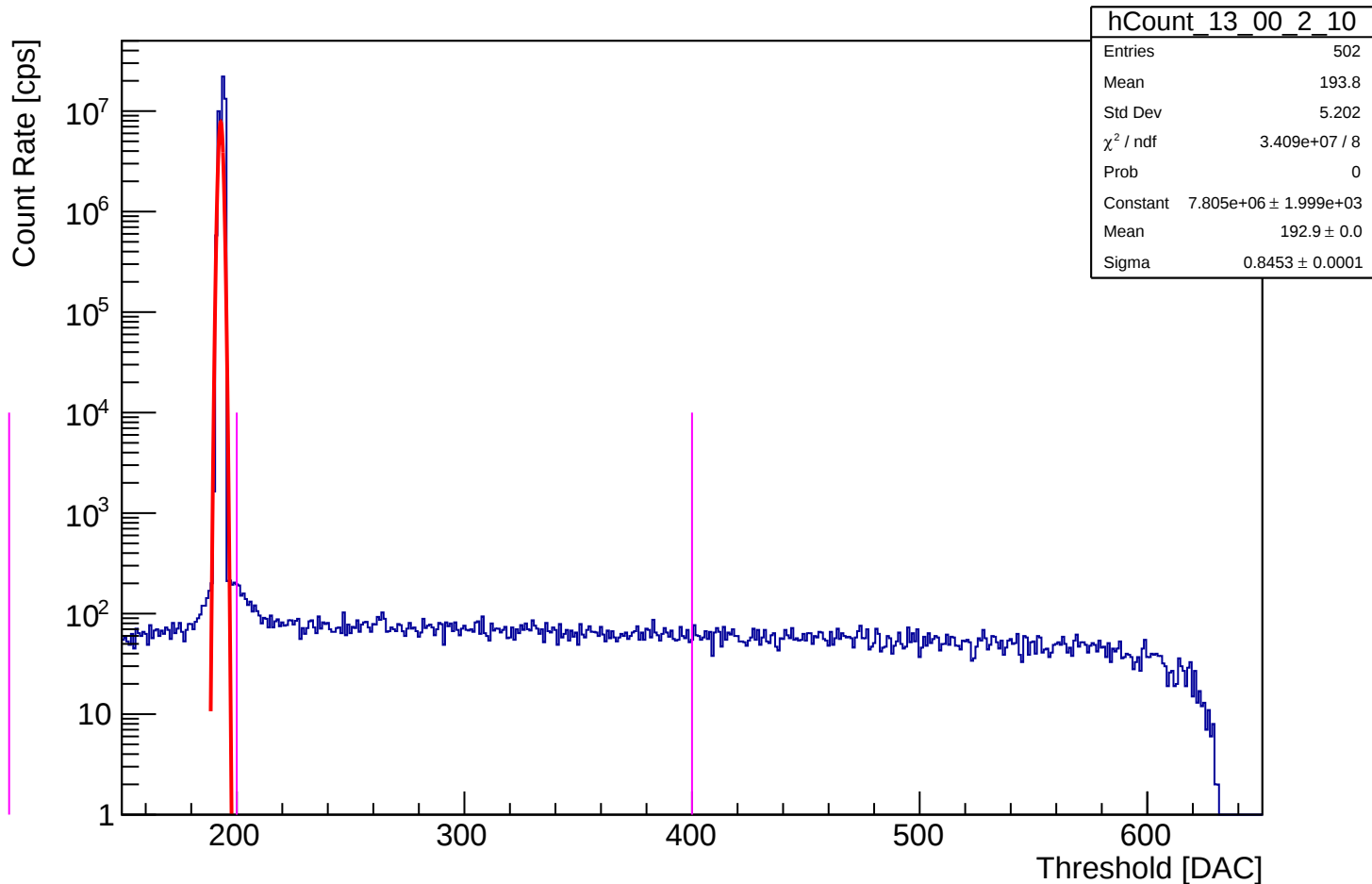


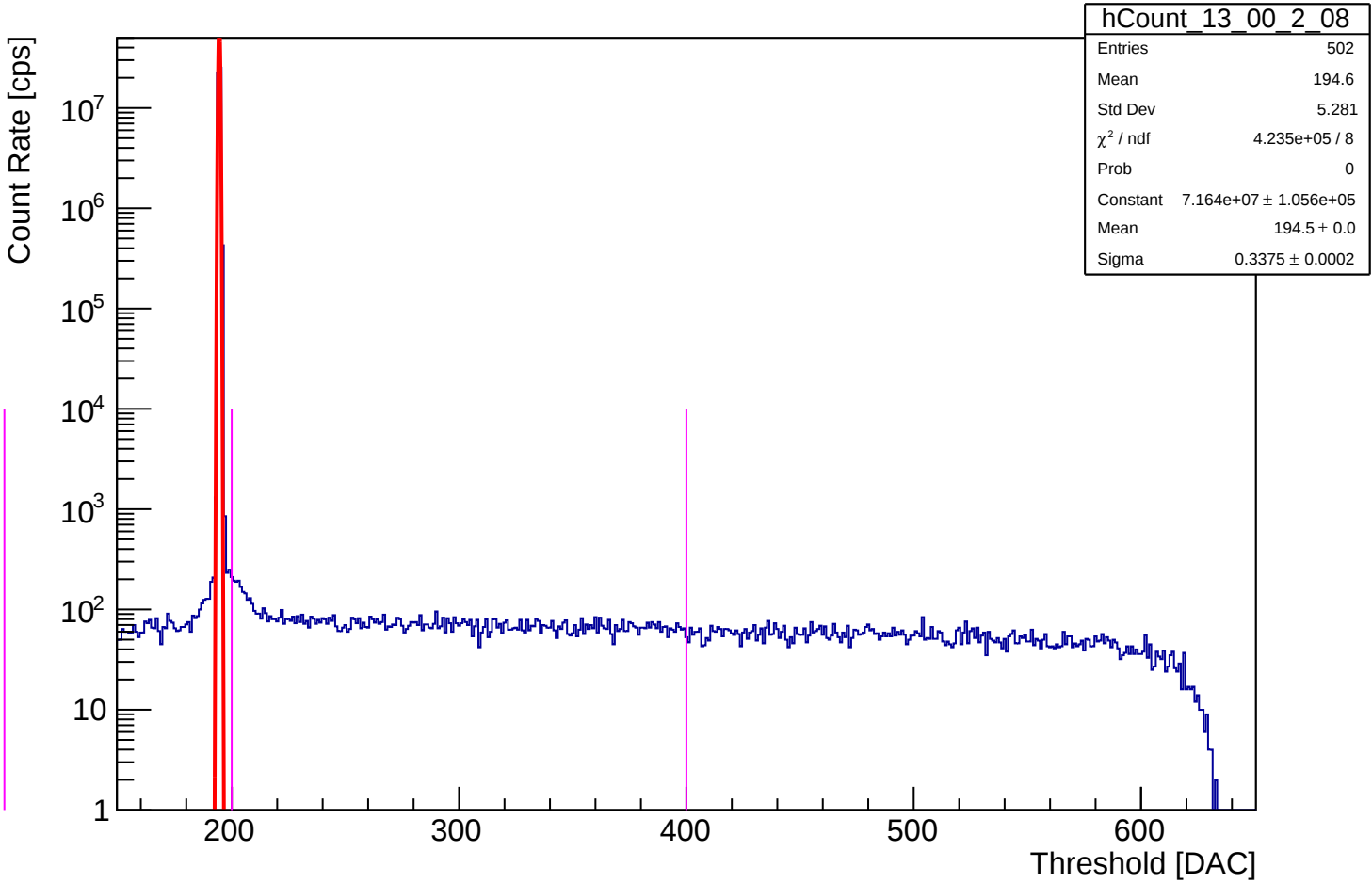
Row 1 Tile 1 Pmt 3 Pixel 41 Slot 13 Fiber 0 Asic 2 Channel 11



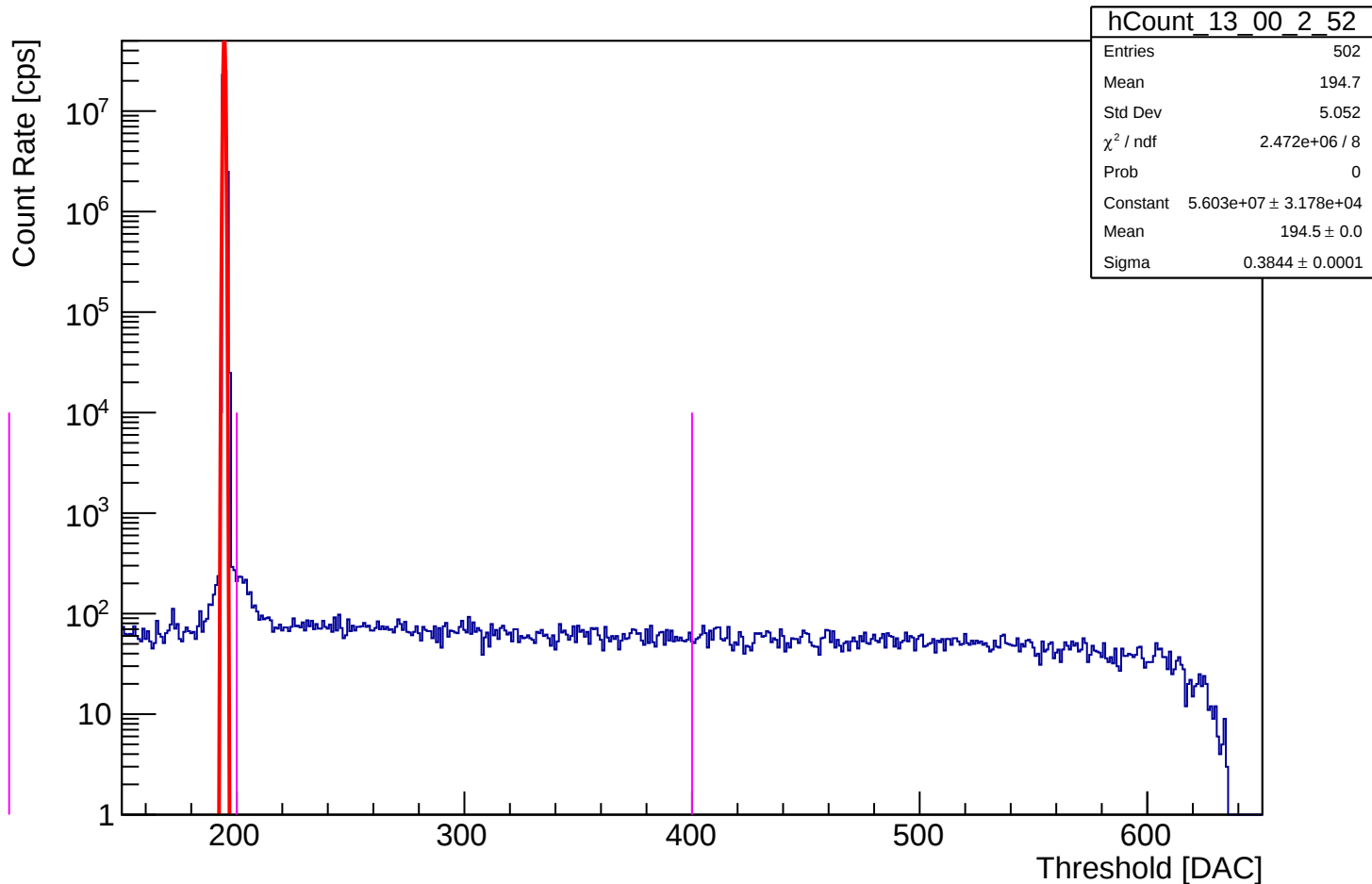


Row 1 Tile 1 Pmt 3 Pixel 43 Slot 13 Fiber 0 Asic 2 Channel 10

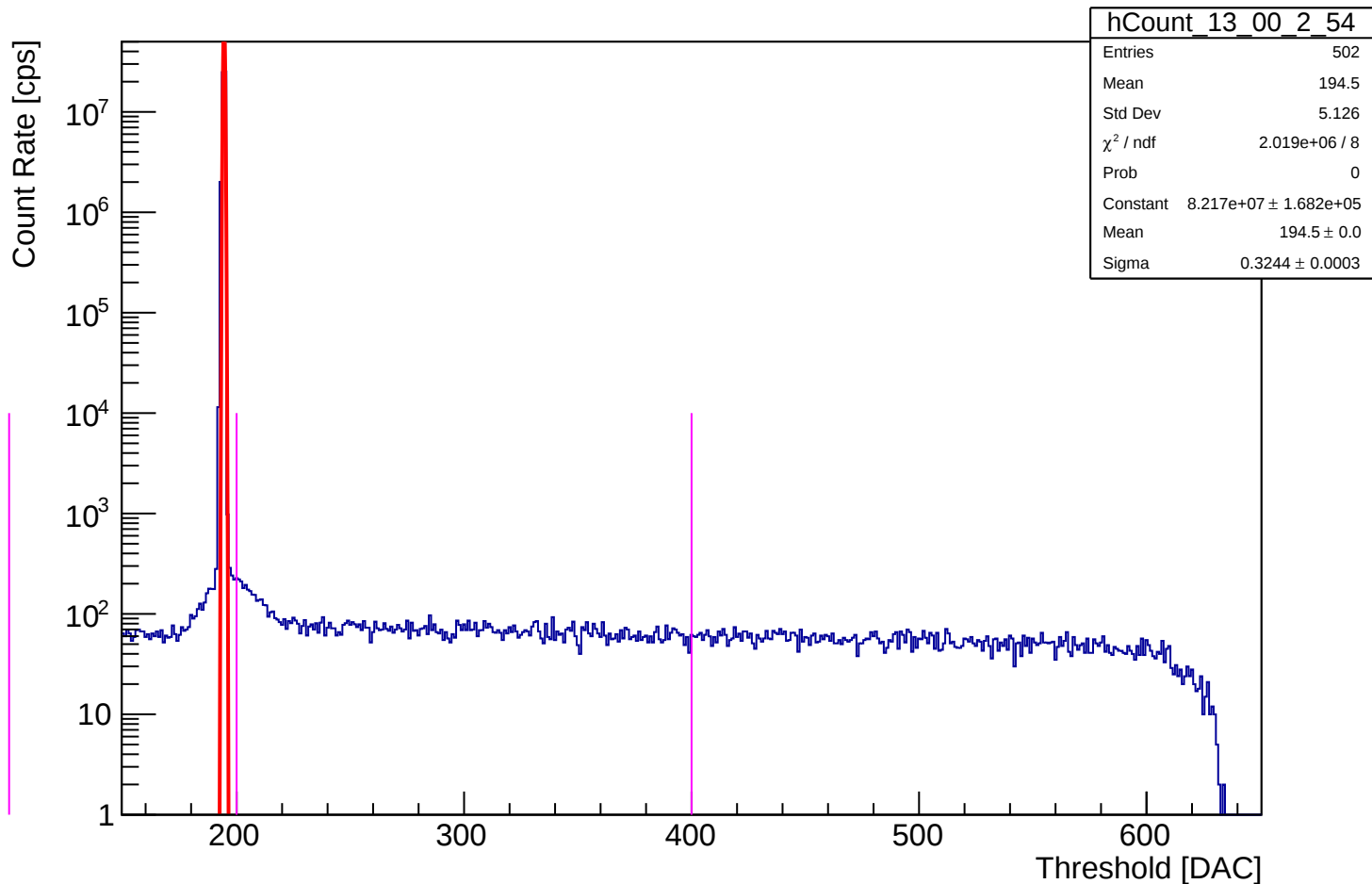




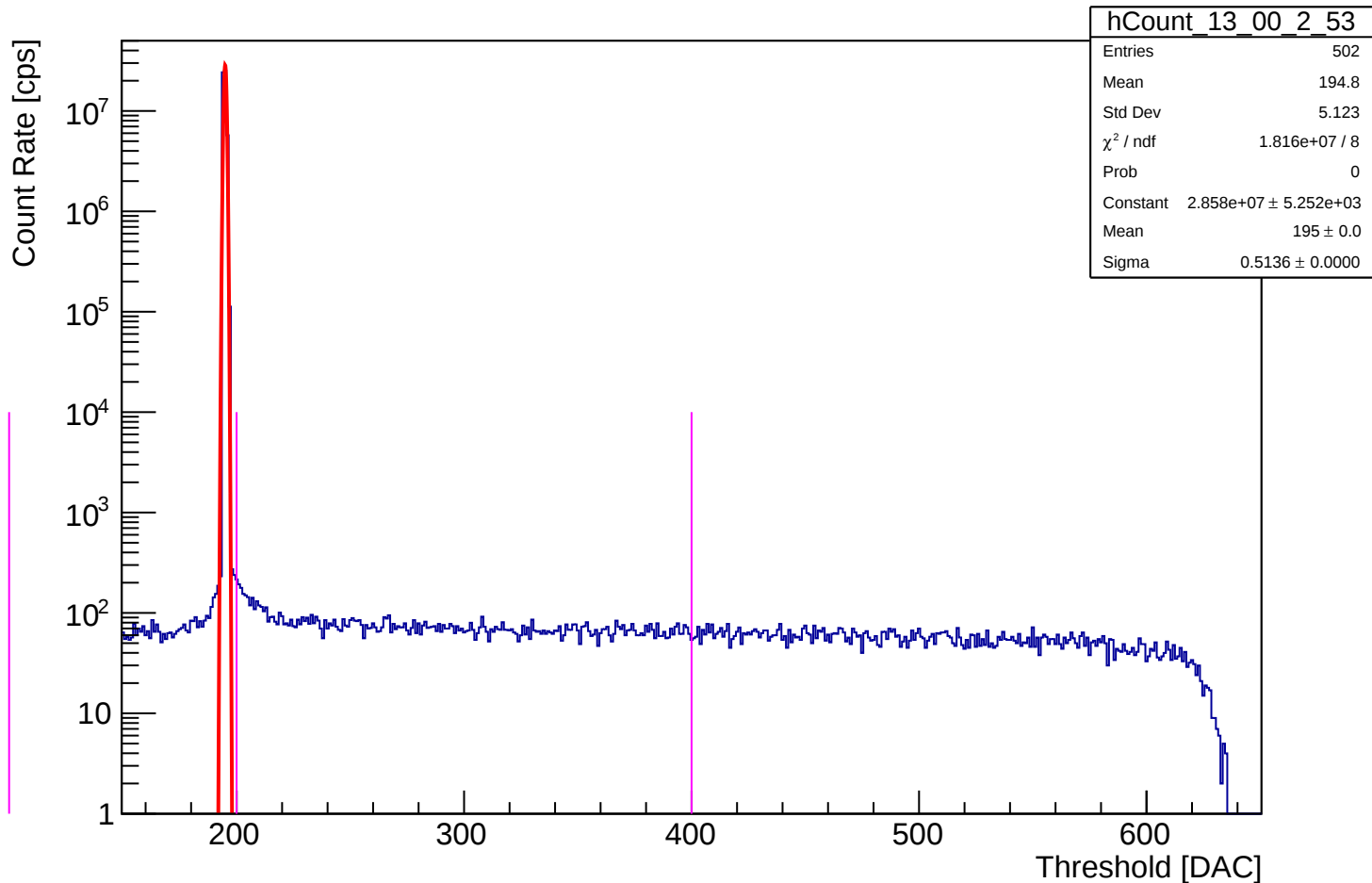
Row 1 Tile 1 Pmt 3 Pixel 45 Slot 13 Fiber 0 Asic 2 Channel 52



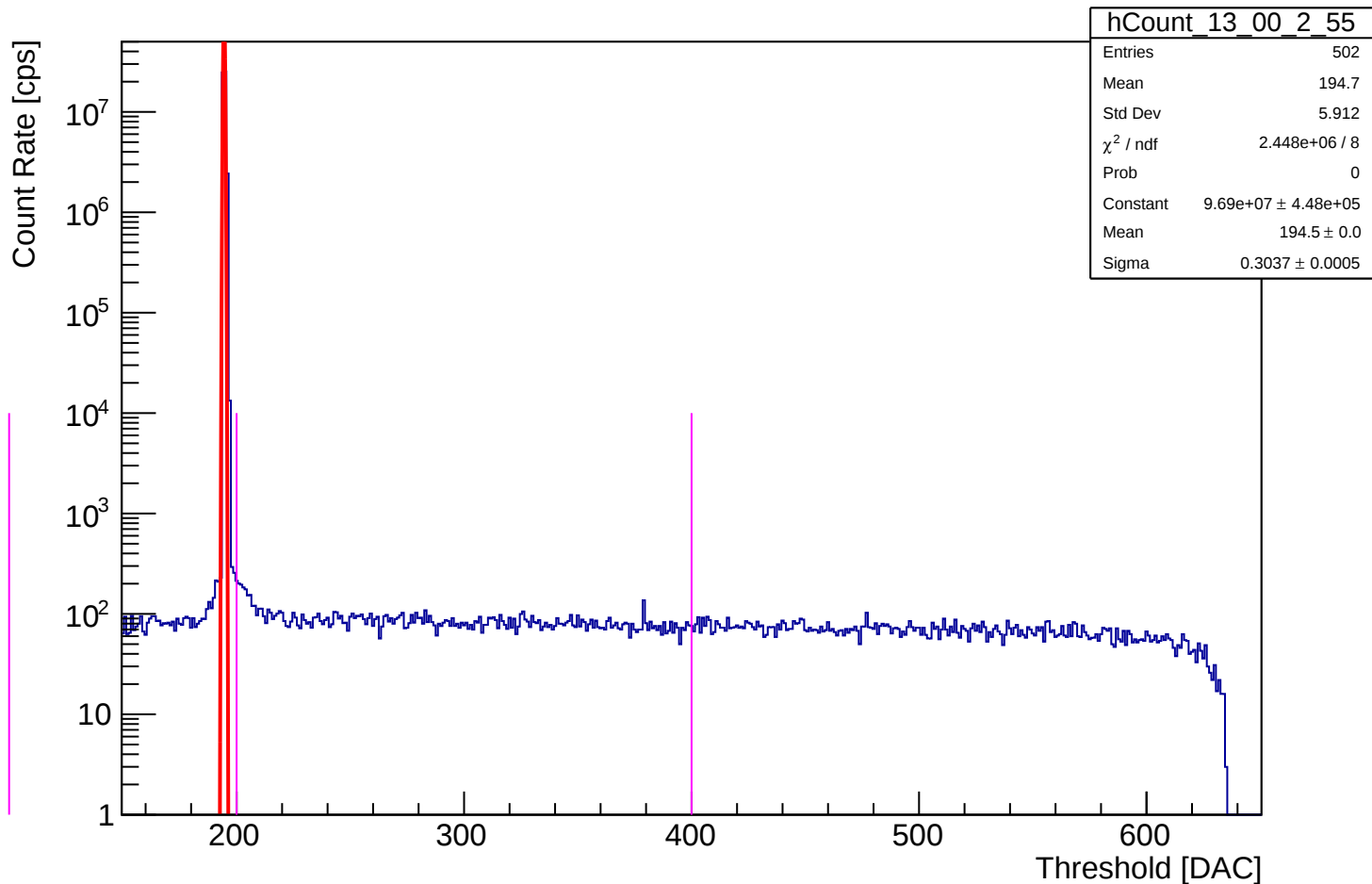
Row 1 Tile 1 Pmt 3 Pixel 46 Slot 13 Fiber 0 Asic 2 Channel 54

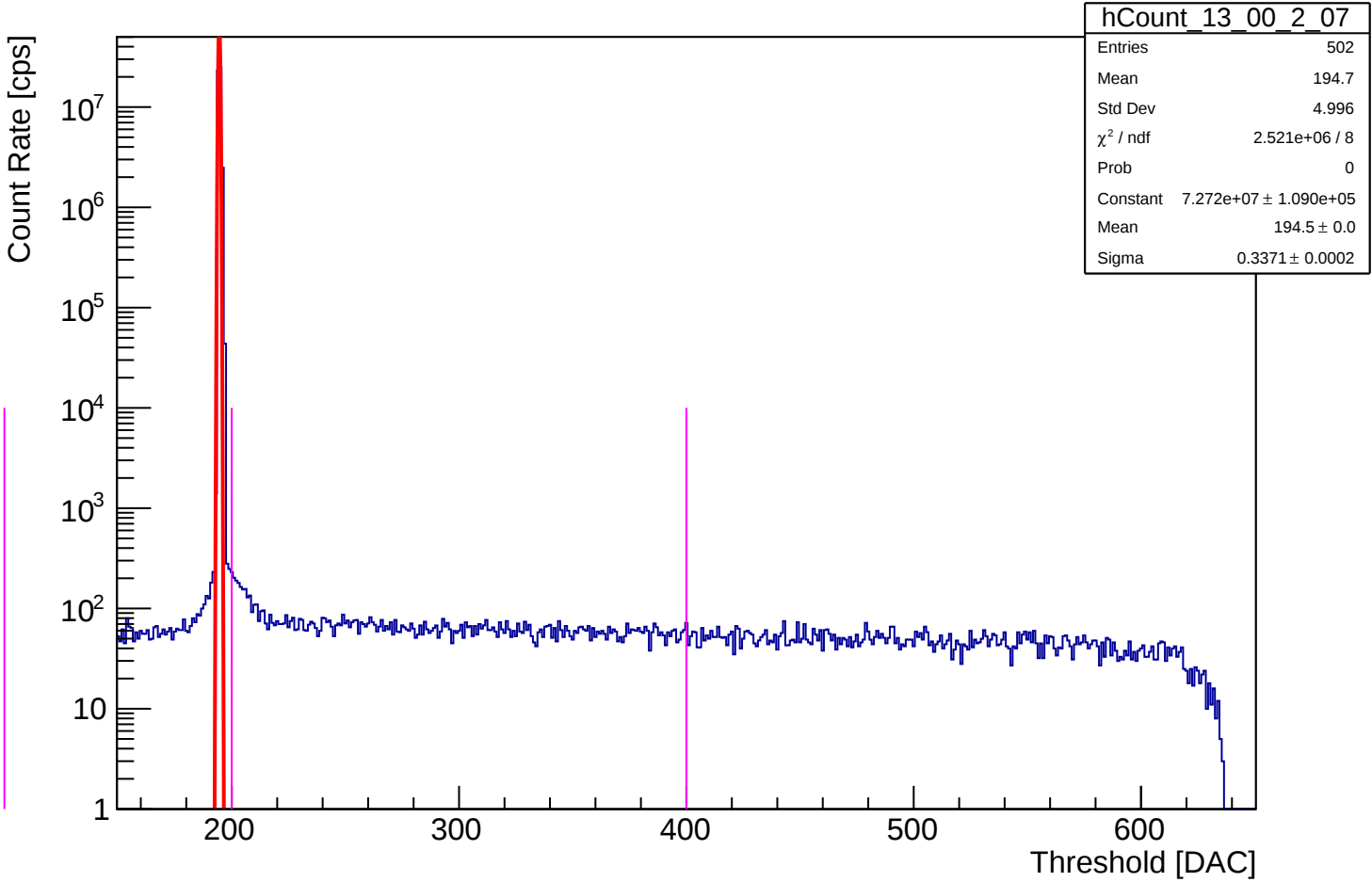


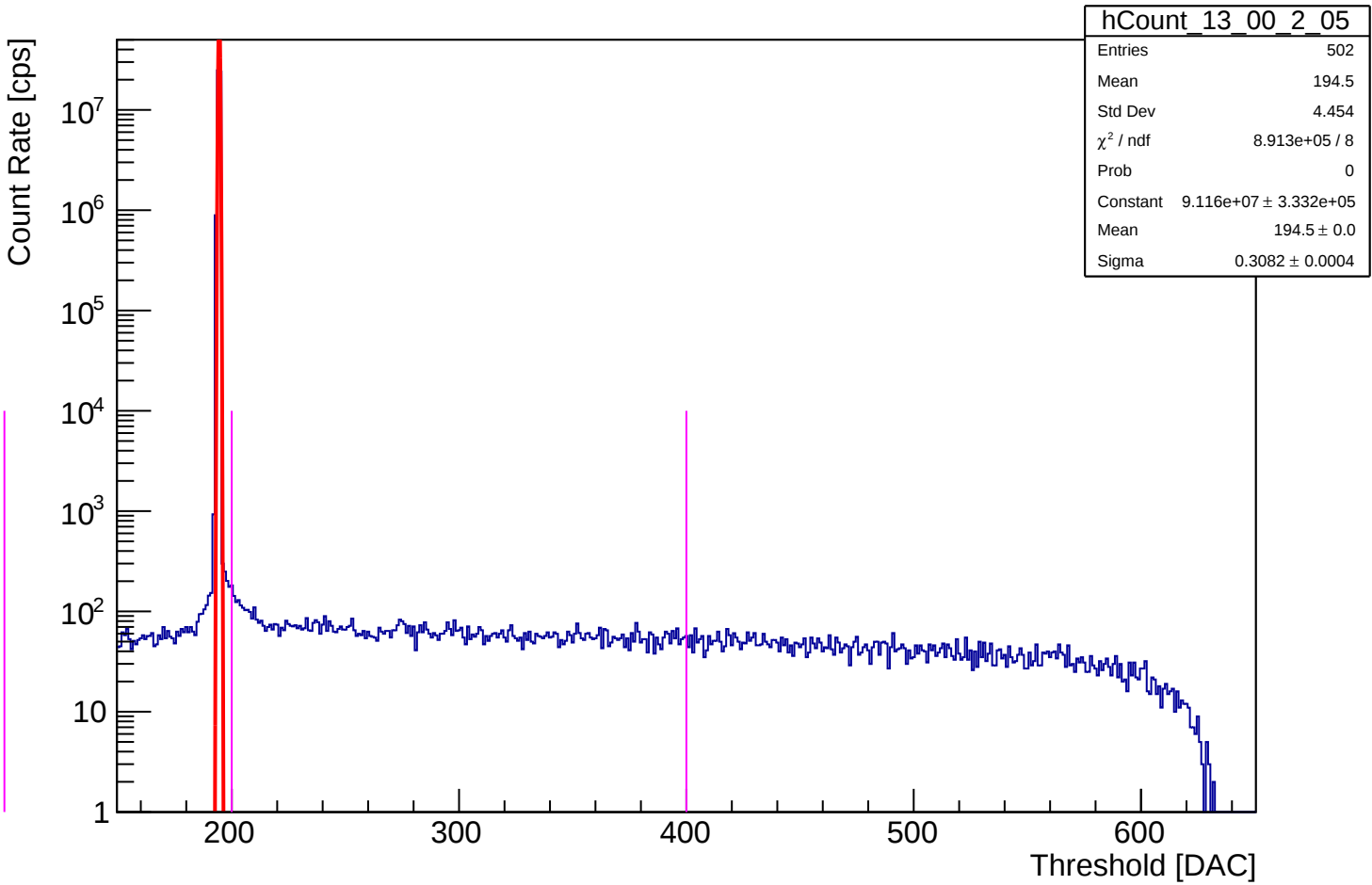
Row 1 Tile 1 Pmt 3 Pixel 47 Slot 13 Fiber 0 Asic 2 Channel 53

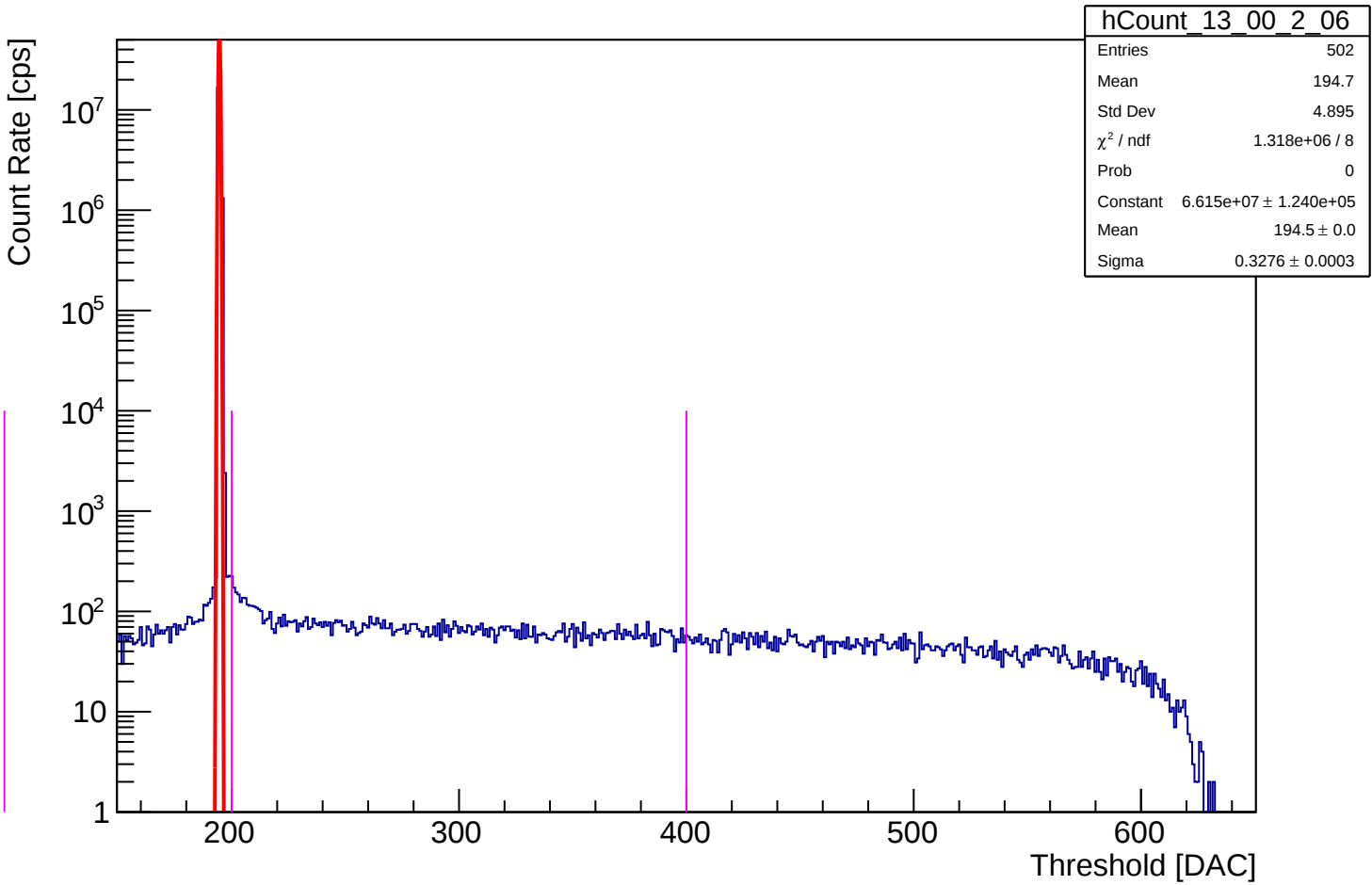


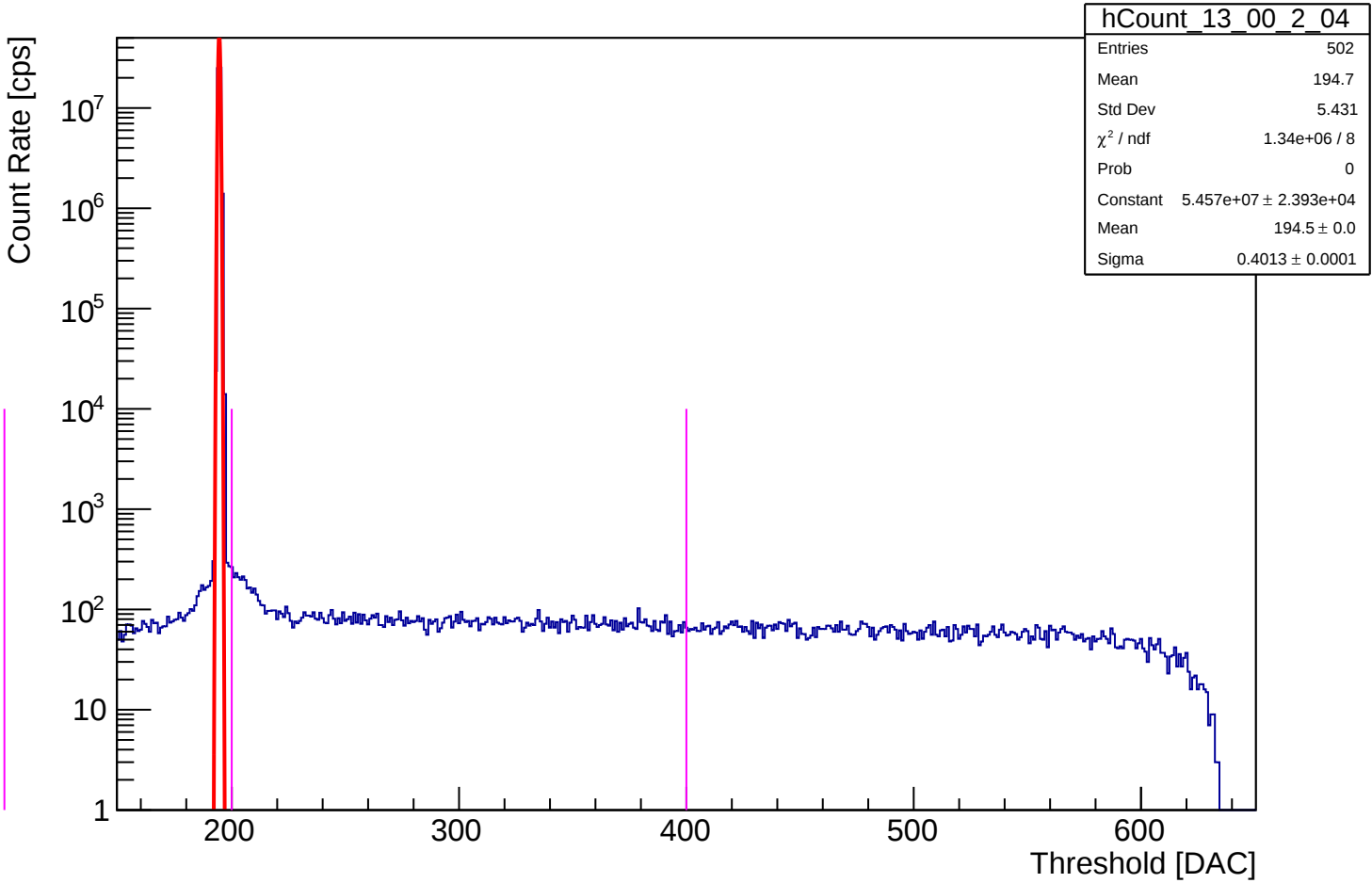
Row 1 Tile 1 Pmt 3 Pixel 48 Slot 13 Fiber 0 Asic 2 Channel 55



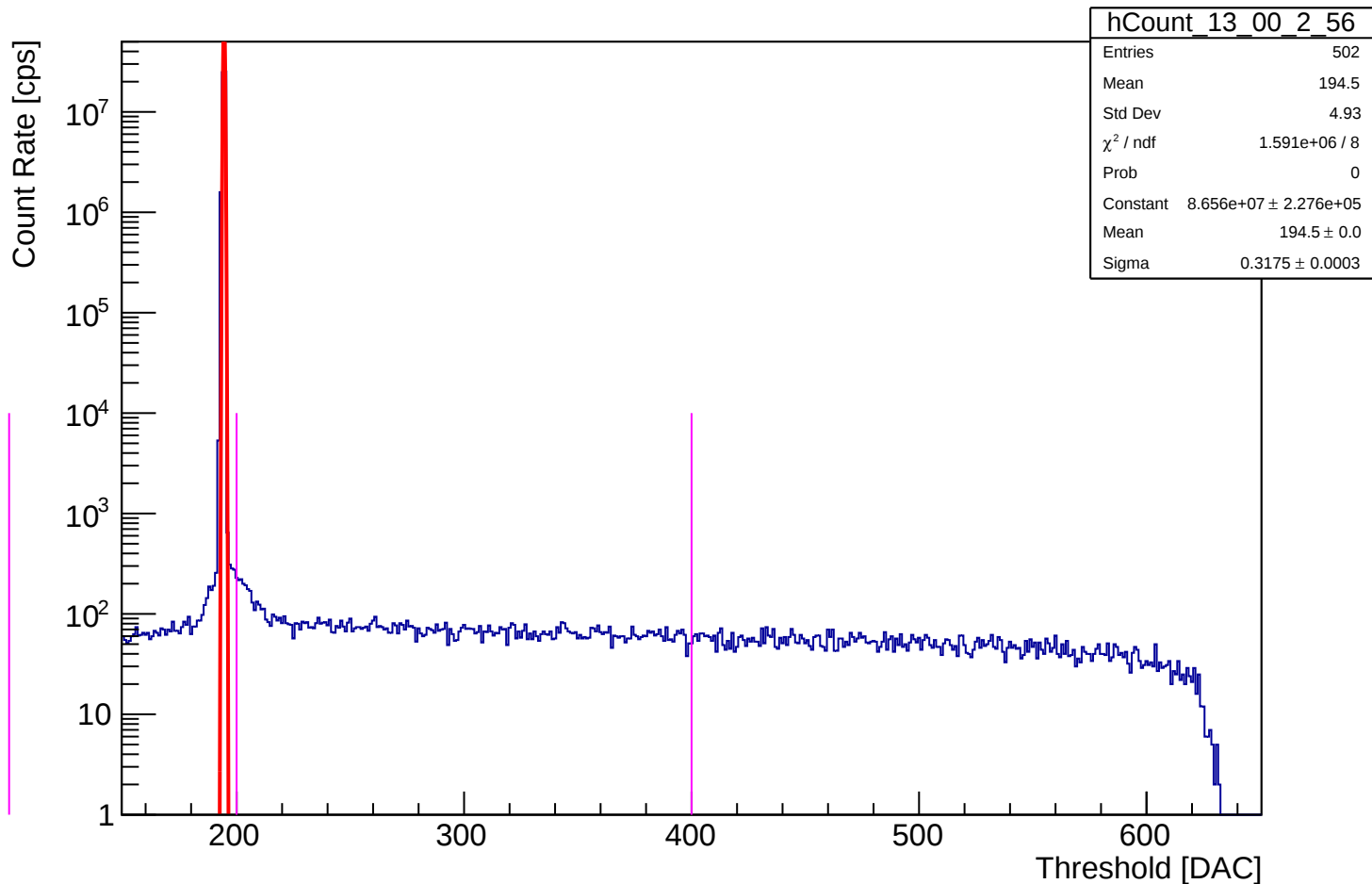




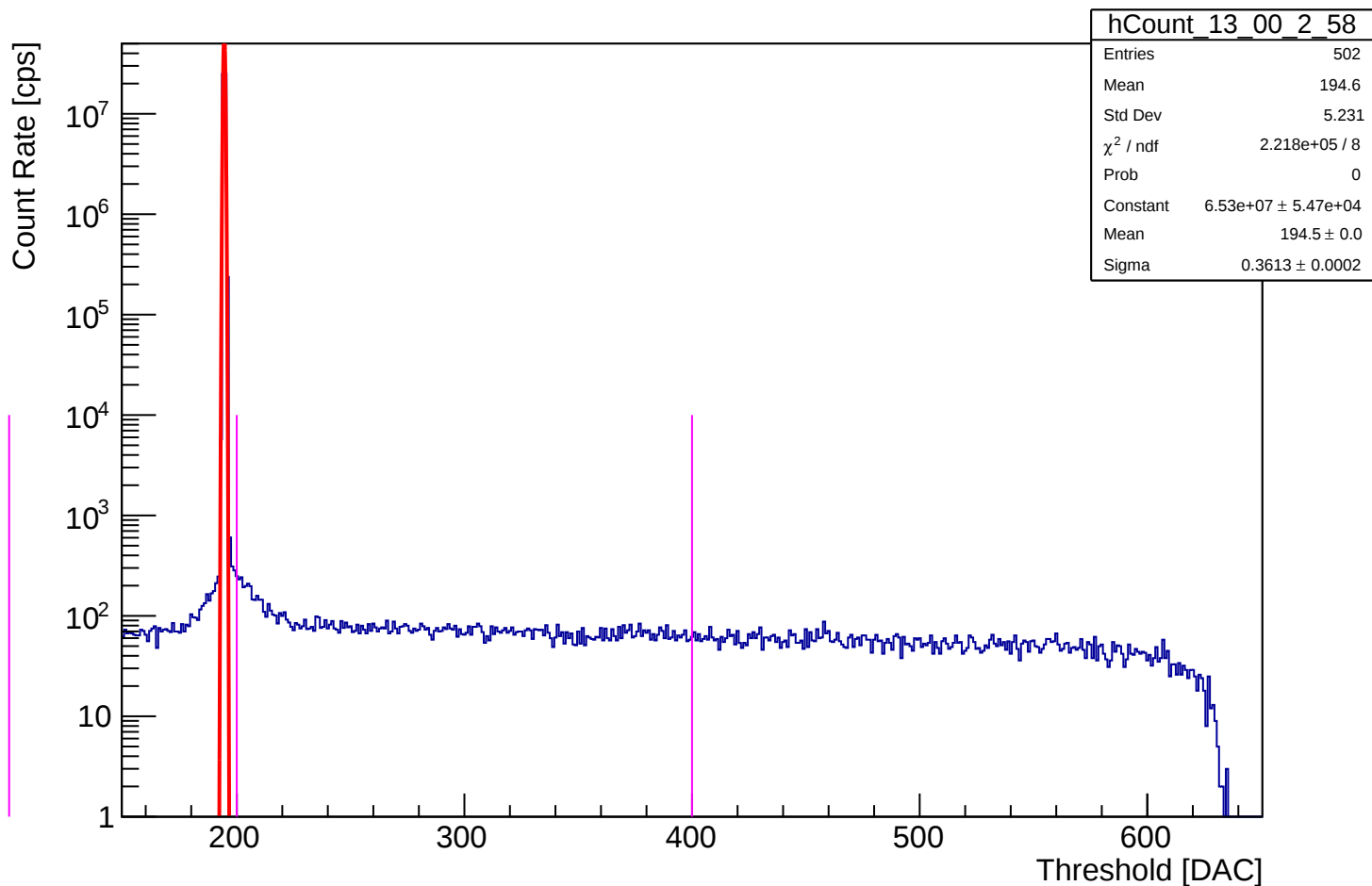




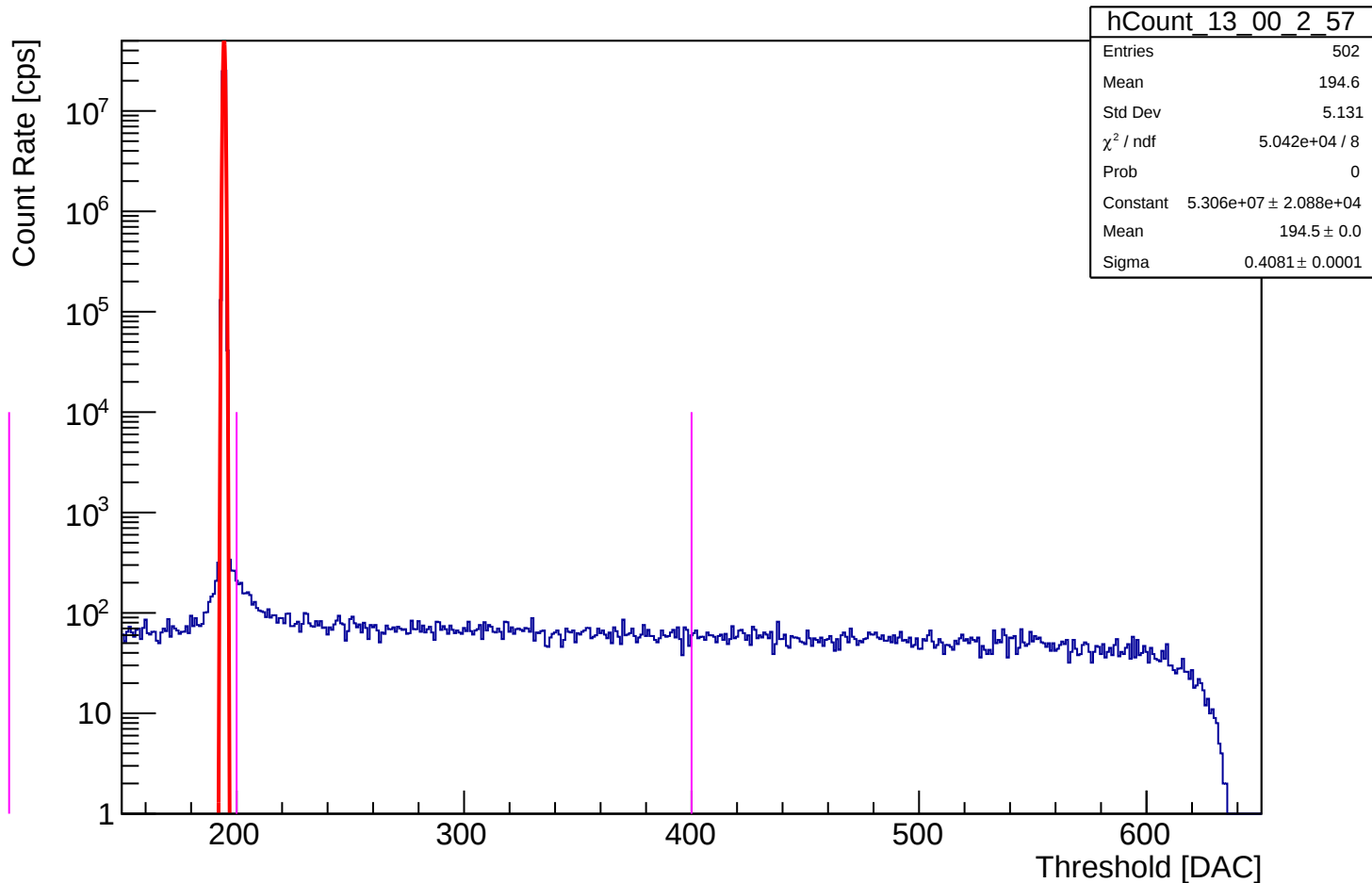
Row 1 Tile 1 Pmt 3 Pixel 53 Slot 13 Fiber 0 Asic 2 Channel 56



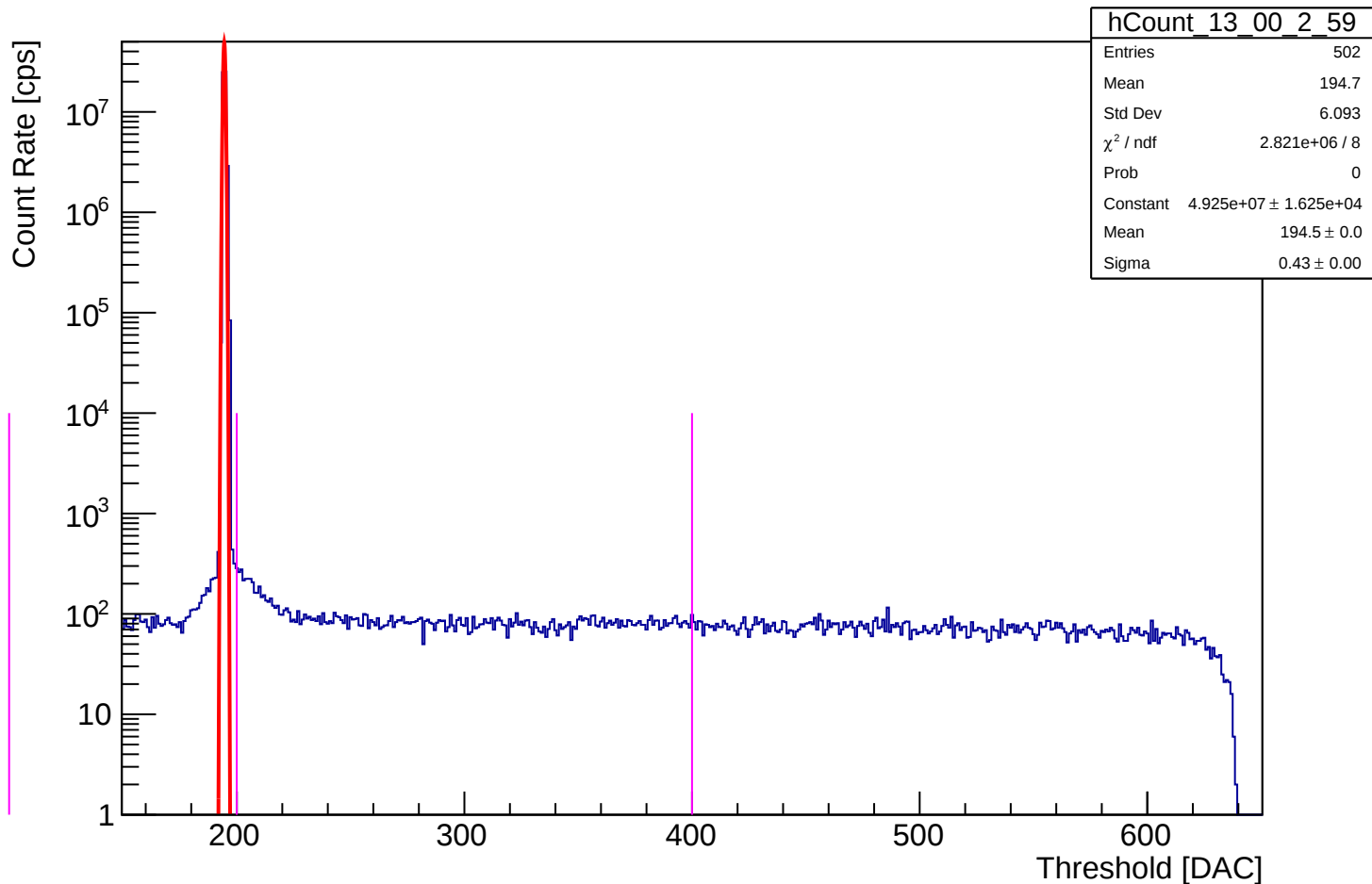
Row 1 Tile 1 Pmt 3 Pixel 54 Slot 13 Fiber 0 Asic 2 Channel 58

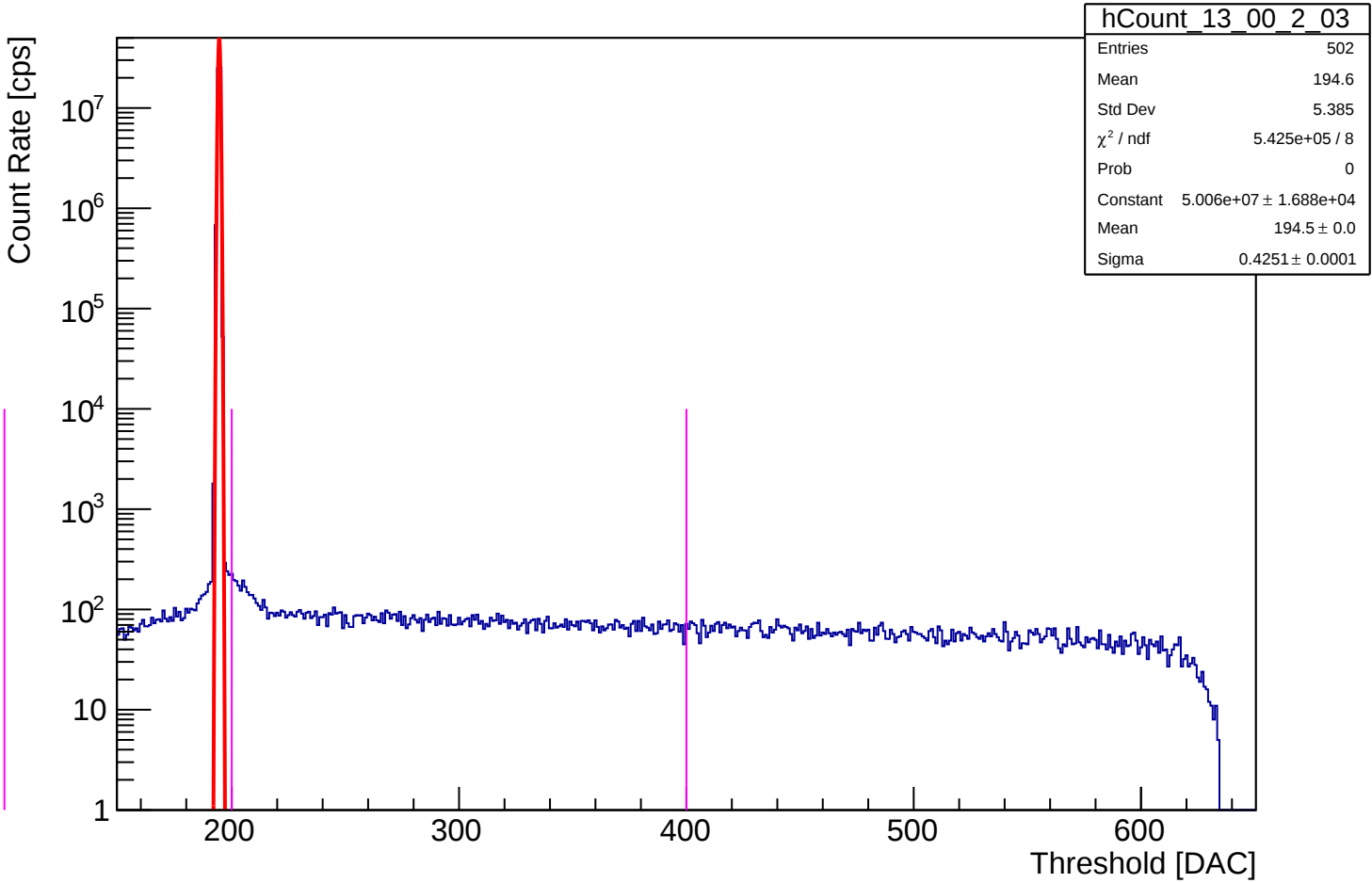


Row 1 Tile 1 Pmt 3 Pixel 55 Slot 13 Fiber 0 Asic 2 Channel 57

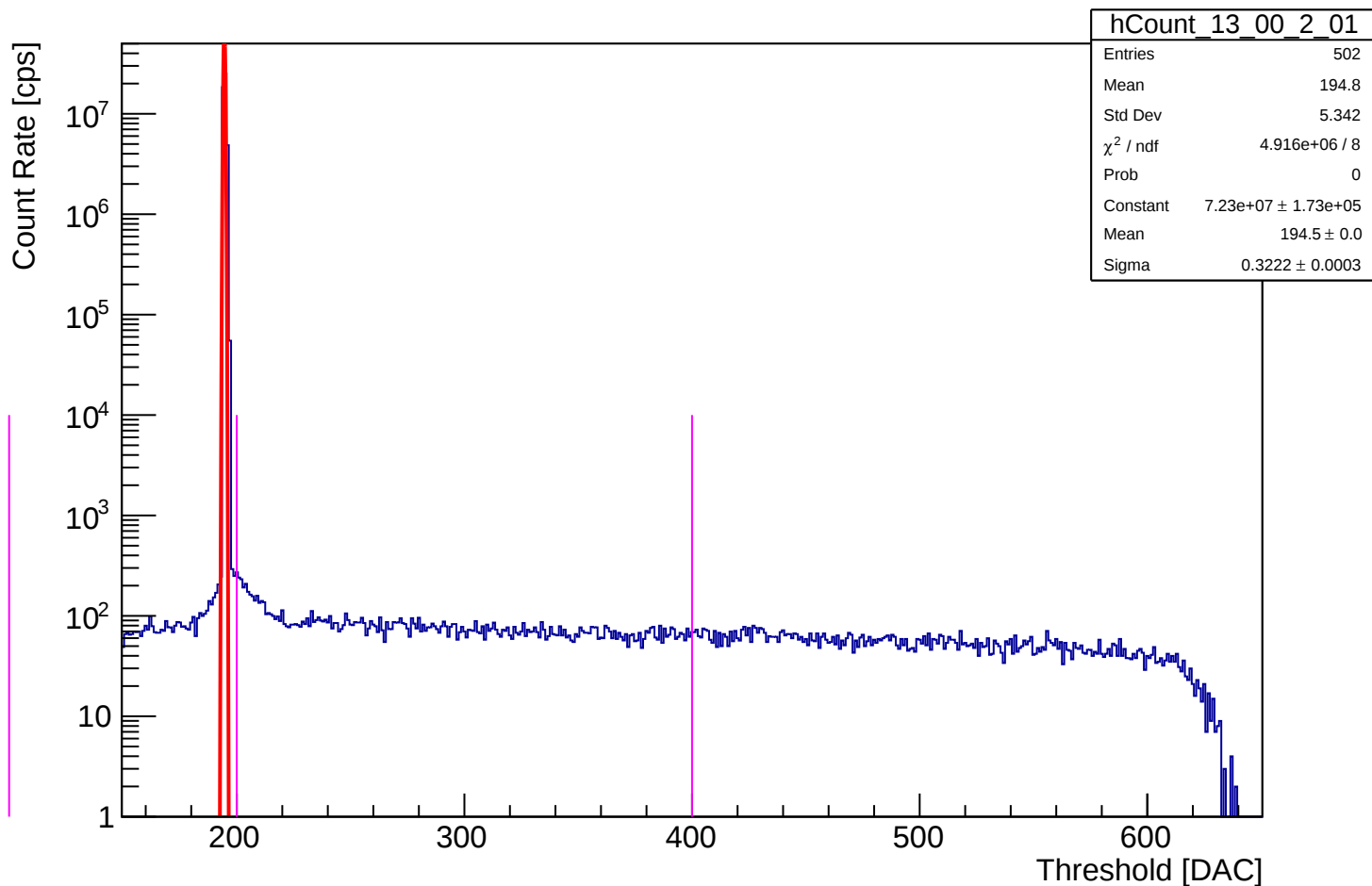


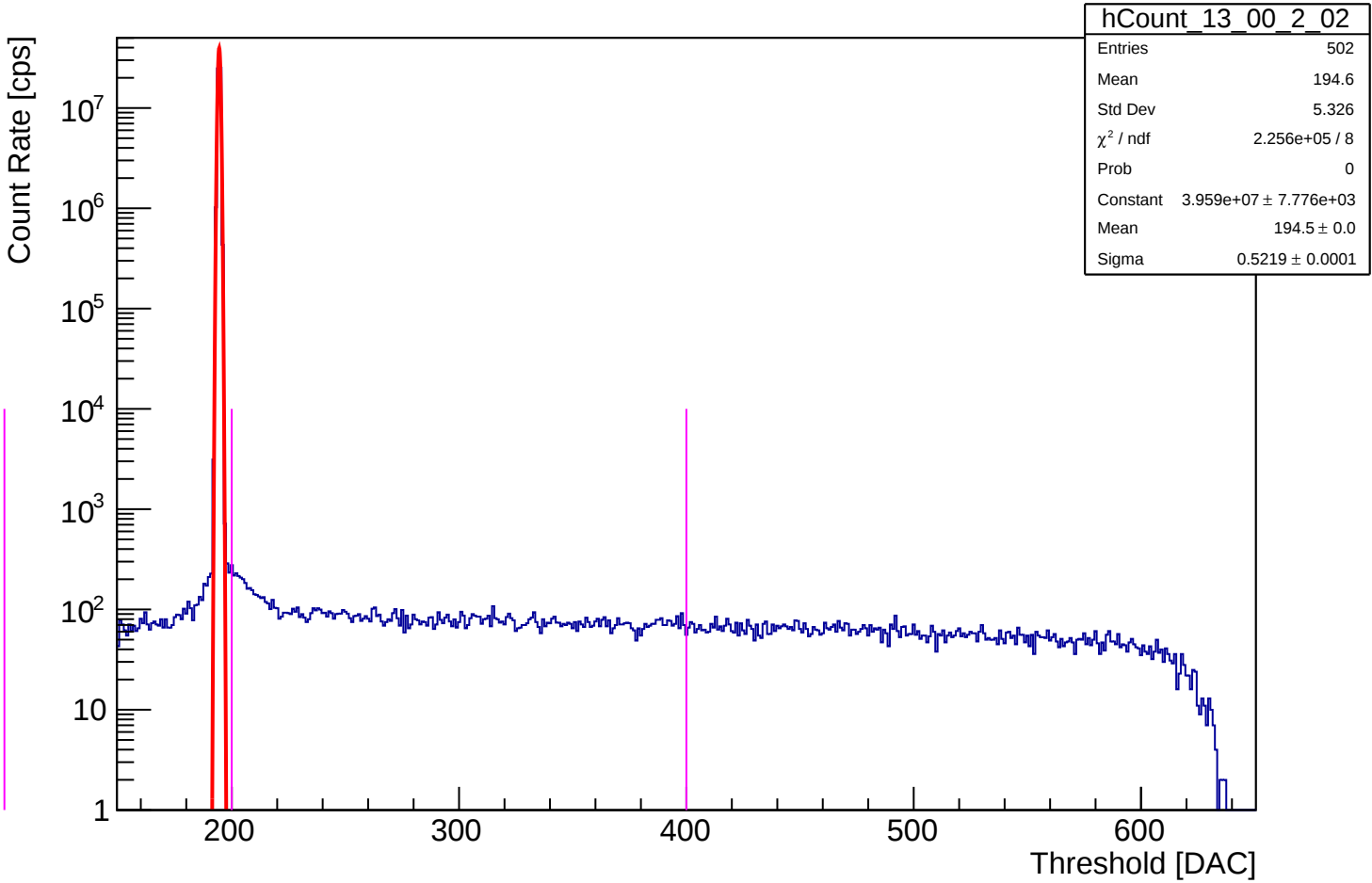
Row 1 Tile 1 Pmt 3 Pixel 56 Slot 13 Fiber 0 Asic 2 Channel 59

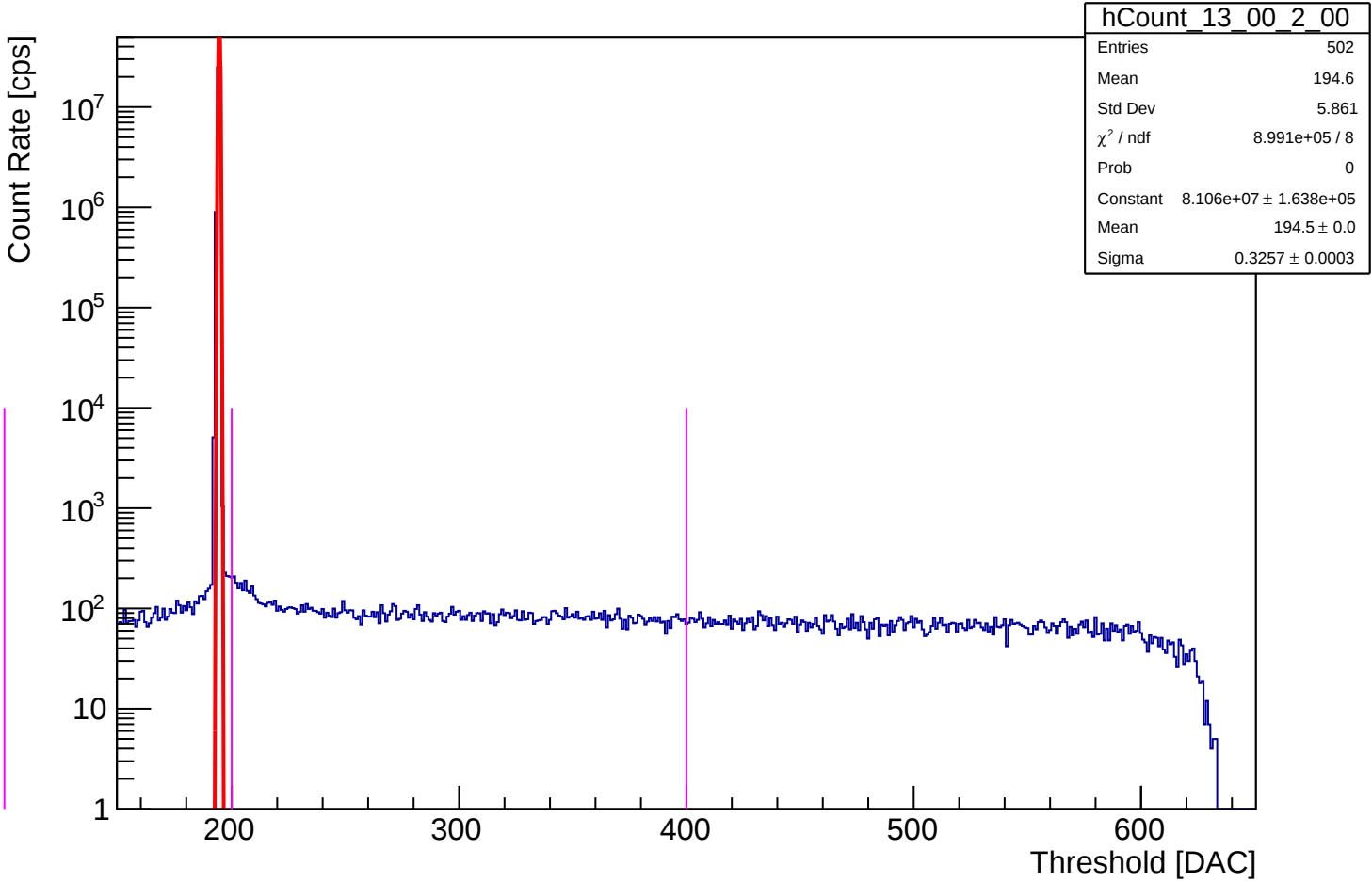




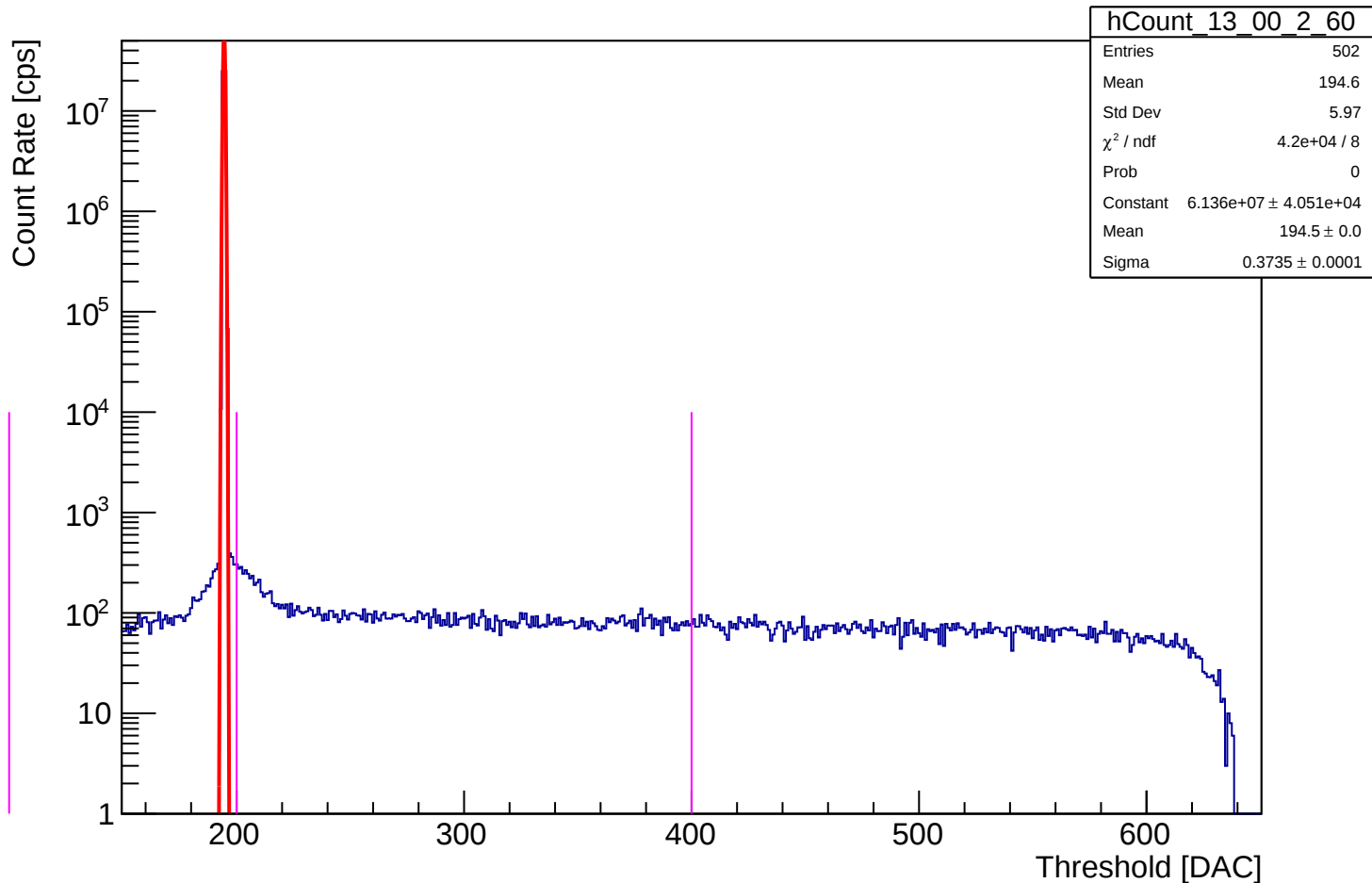
Row 1 Tile 1 Pmt 3 Pixel 58 Slot 13 Fiber 0 Asic 2 Channel 1



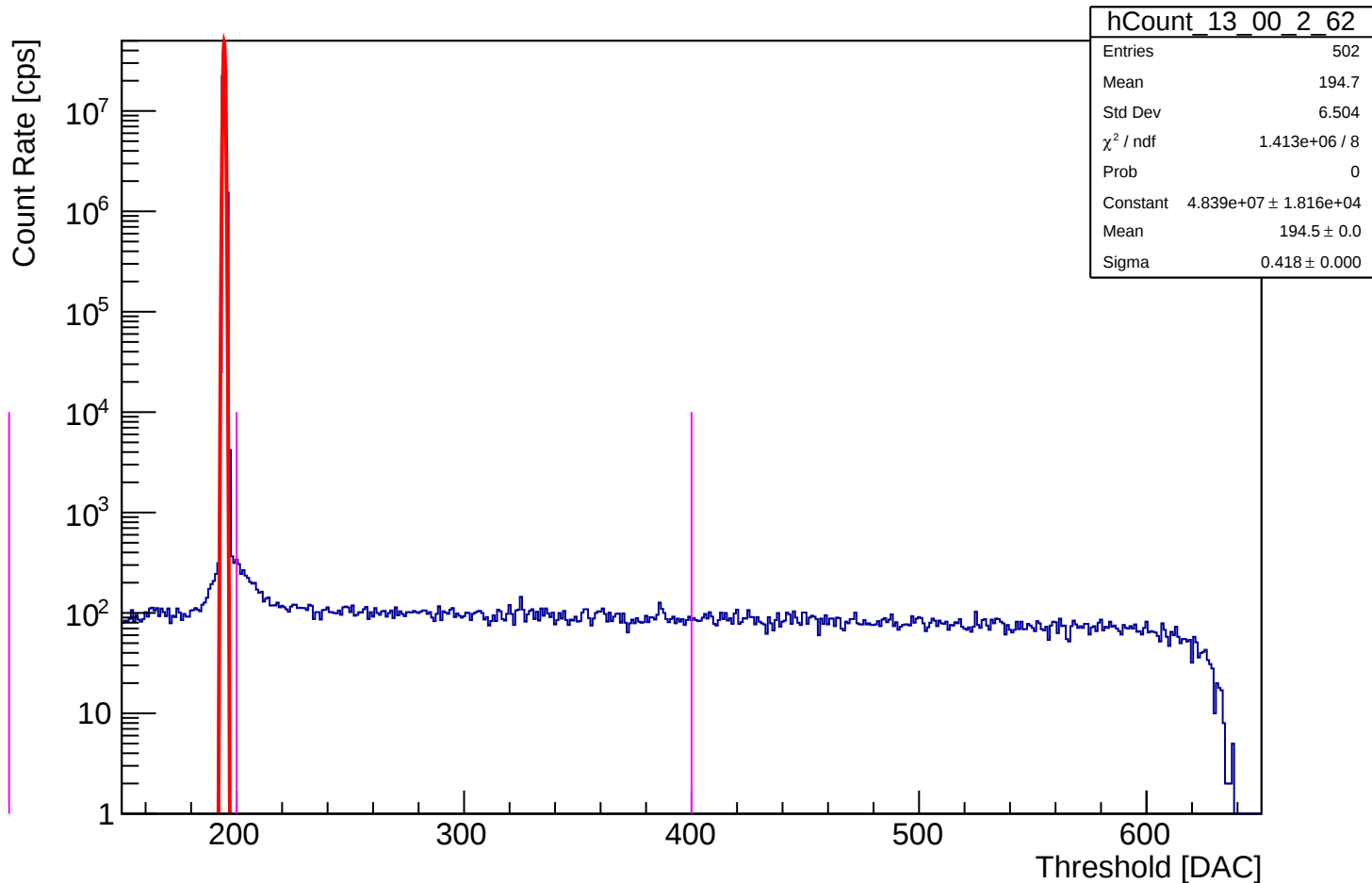




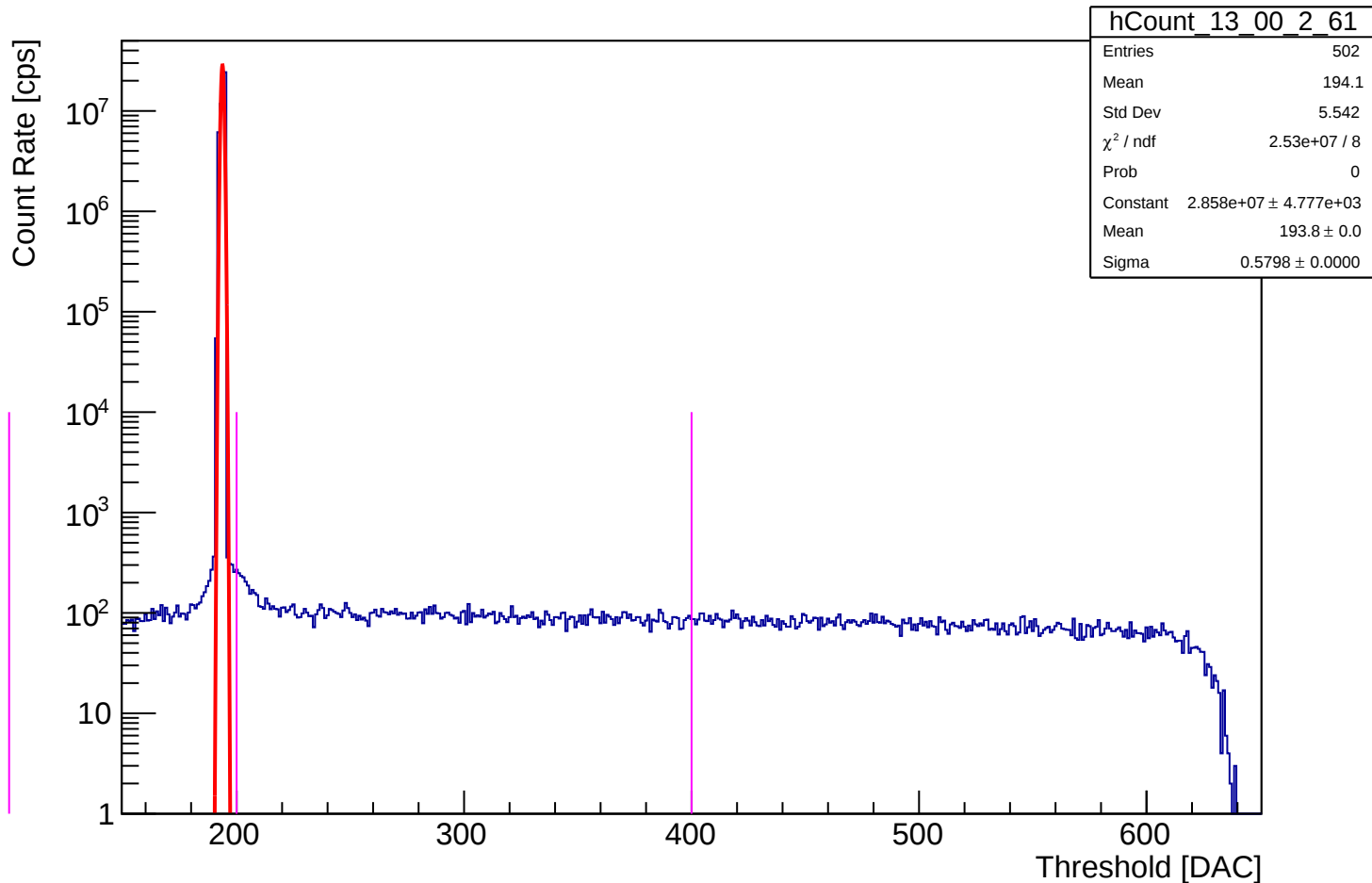
Row 1 Tile 1 Pmt 3 Pixel 61 Slot 13 Fiber 0 Asic 2 Channel 60



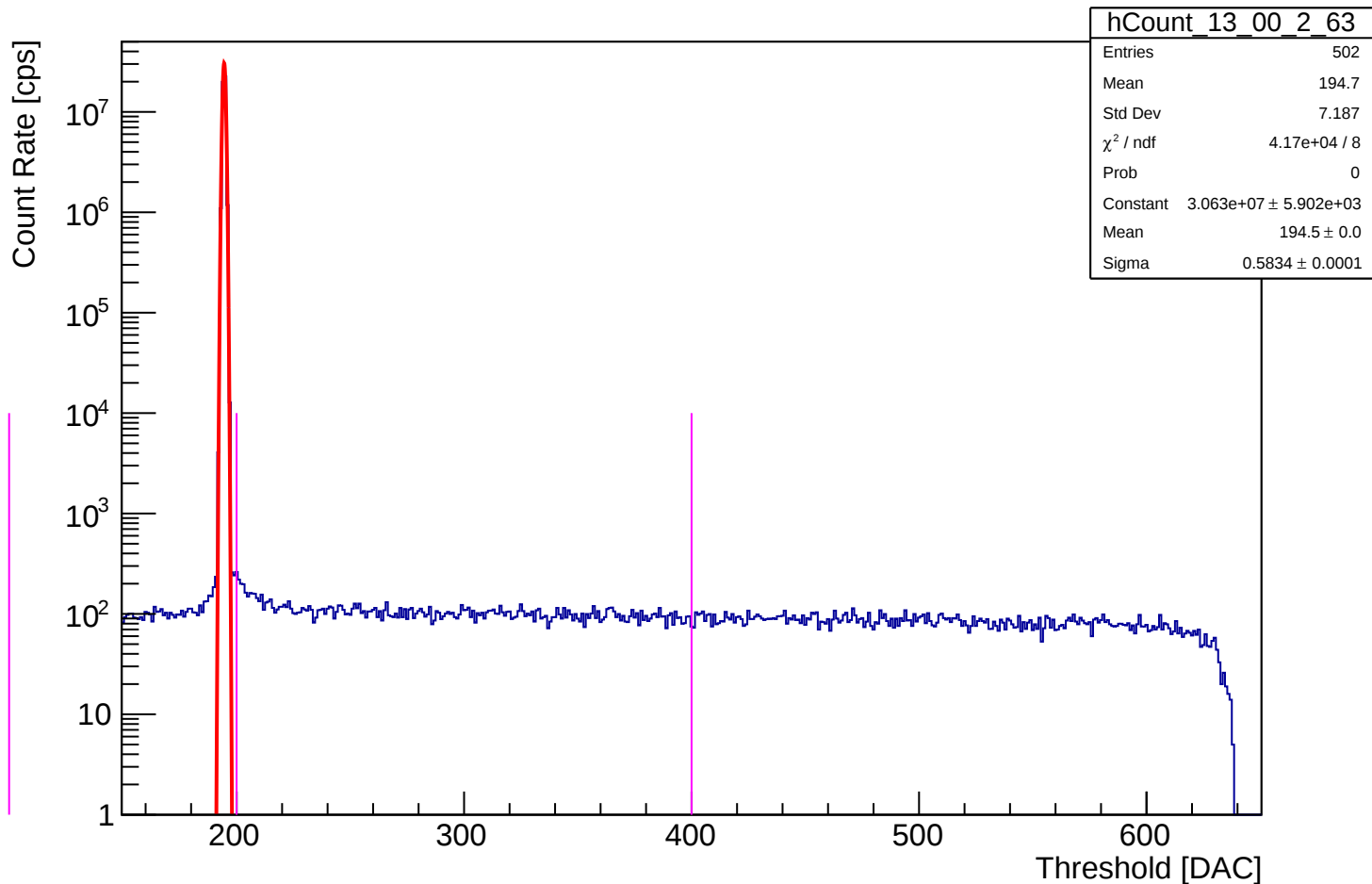
Row 1 Tile 1 Pmt 3 Pixel 62 Slot 13 Fiber 0 Asic 2 Channel 62



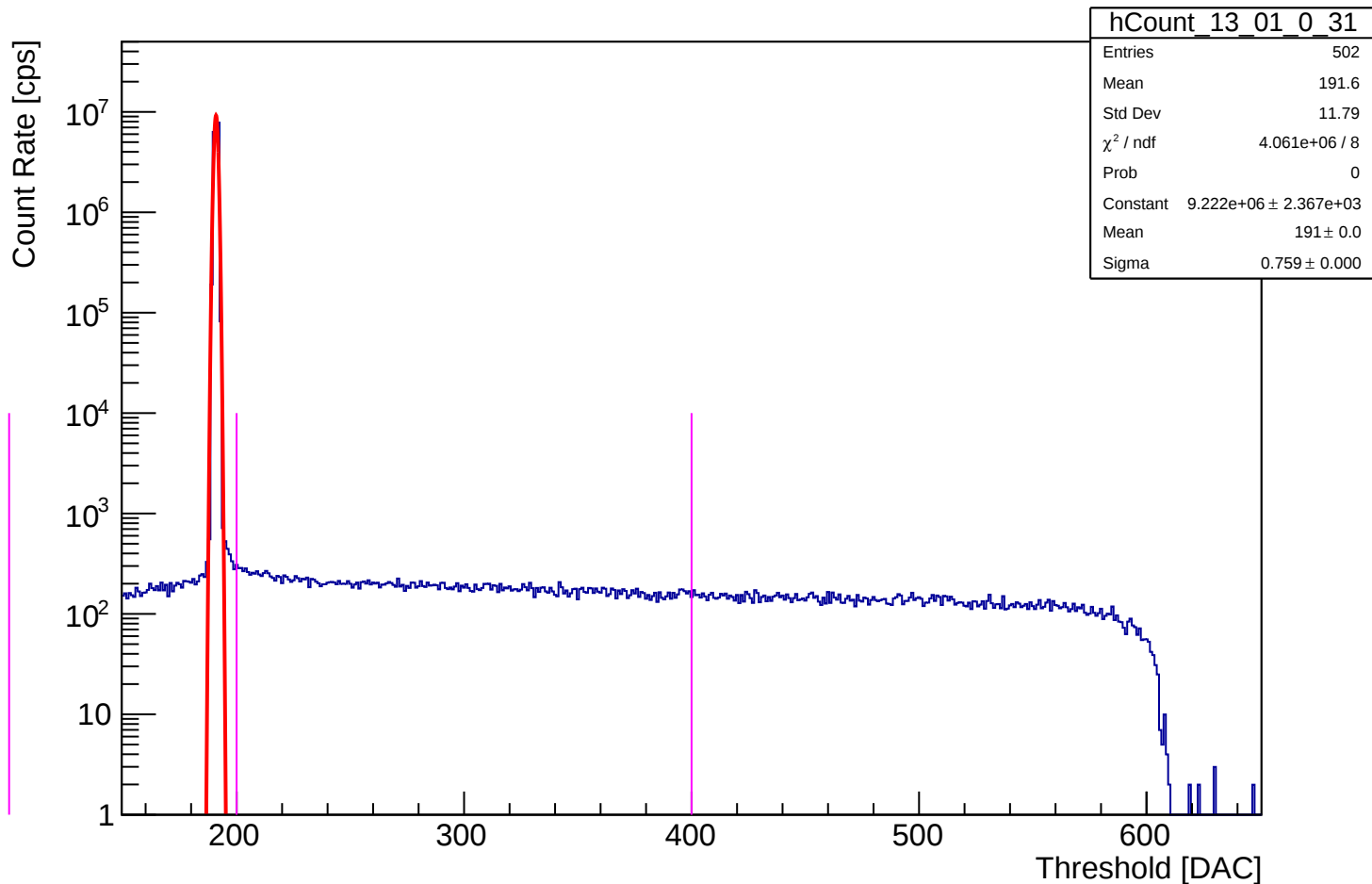
Row 1 Tile 1 Pmt 3 Pixel 63 Slot 13 Fiber 0 Asic 2 Channel 61



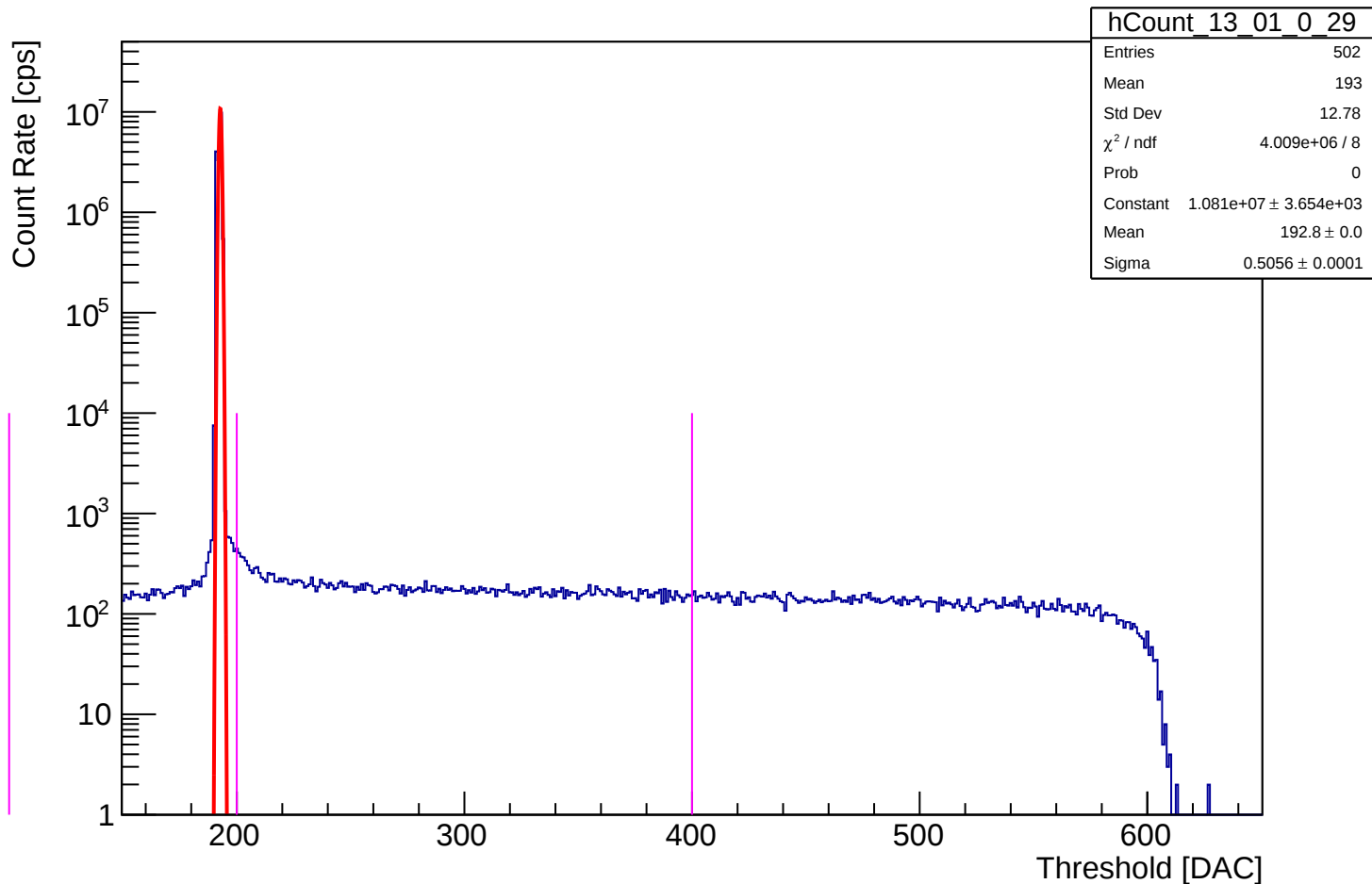
Row 1 Tile 1 Pmt 3 Pixel 64 Slot 13 Fiber 0 Asic 2 Channel 63



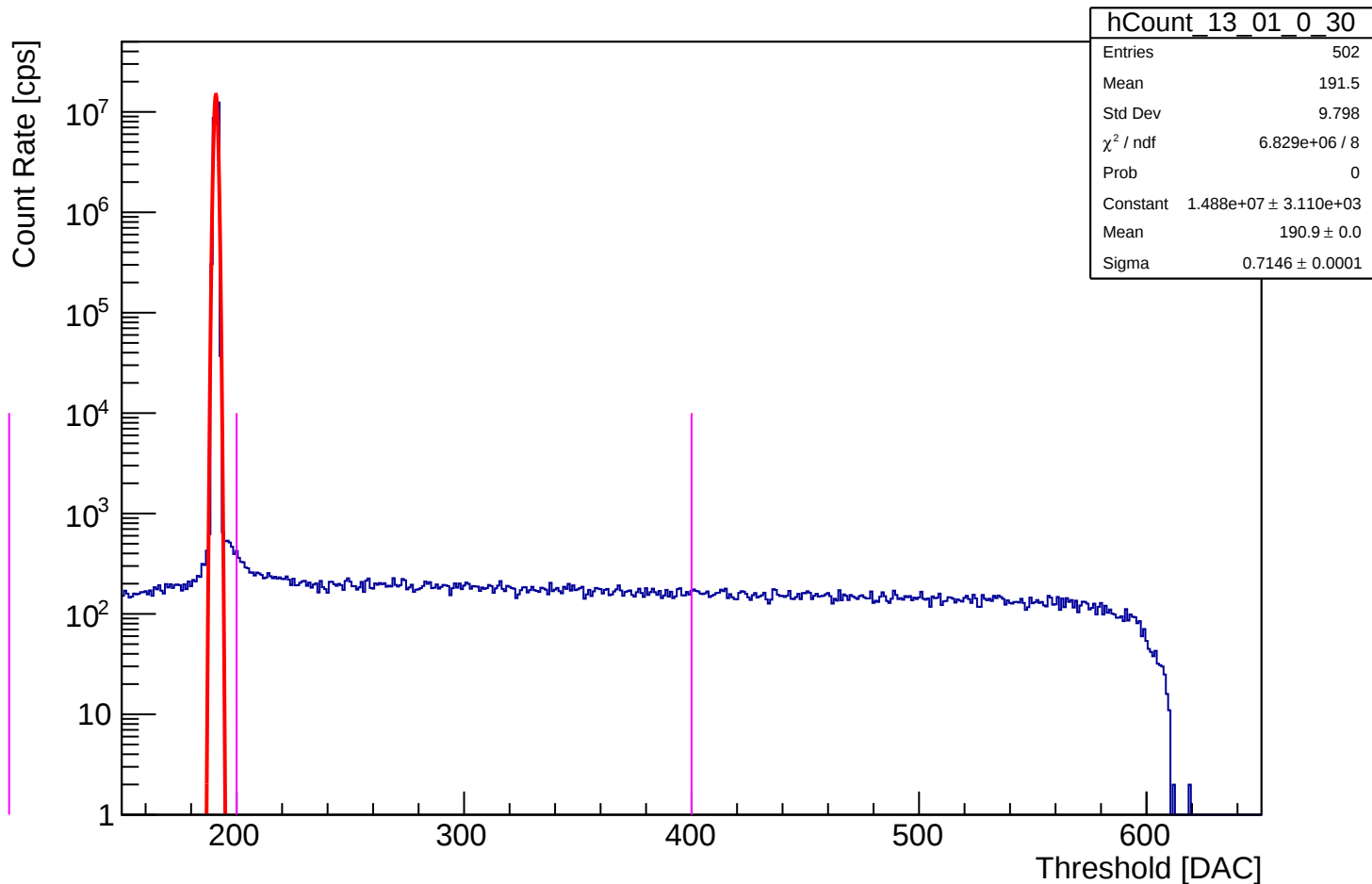
Row 1 Tile 1 Pmt 4 Pixel 1 Slot 13 Fiber 1 Asic 0 Channel 31



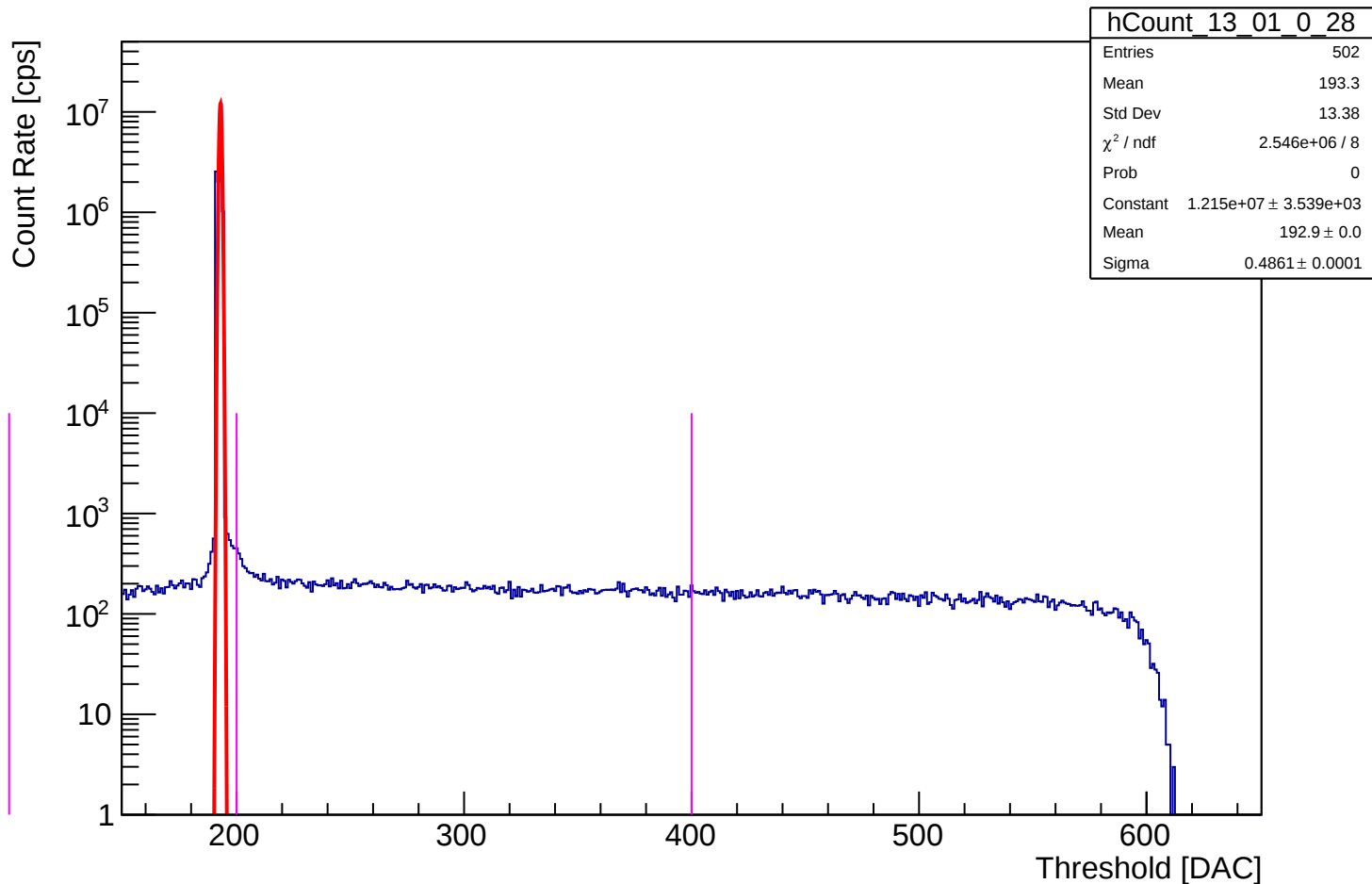
Row 1 Tile 1 Pmt 4 Pixel 2 Slot 13 Fiber 1 Asic 0 Channel 29



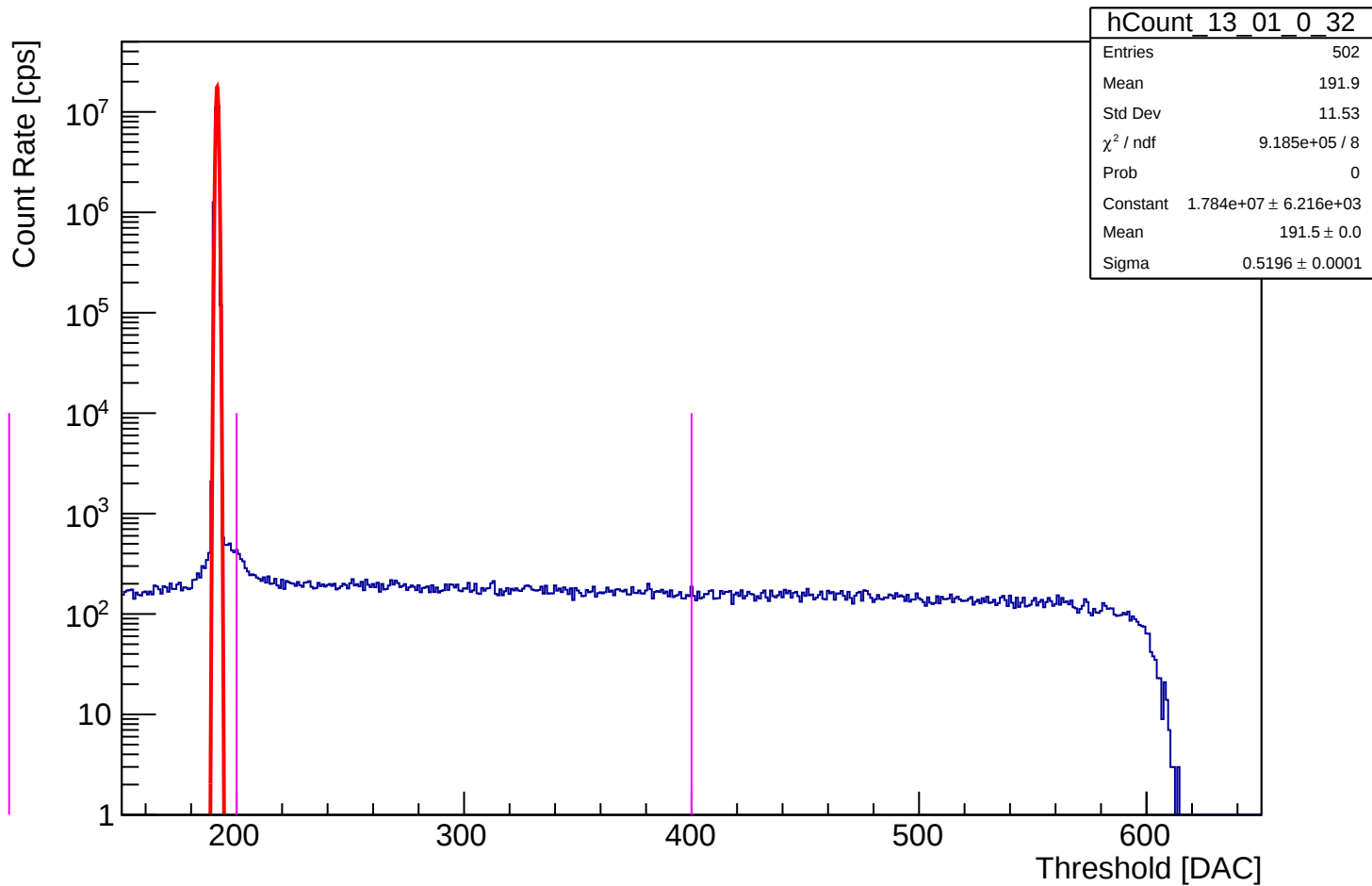
Row 1 Tile 1 Pmt 4 Pixel 3 Slot 13 Fiber 1 Asic 0 Channel 30



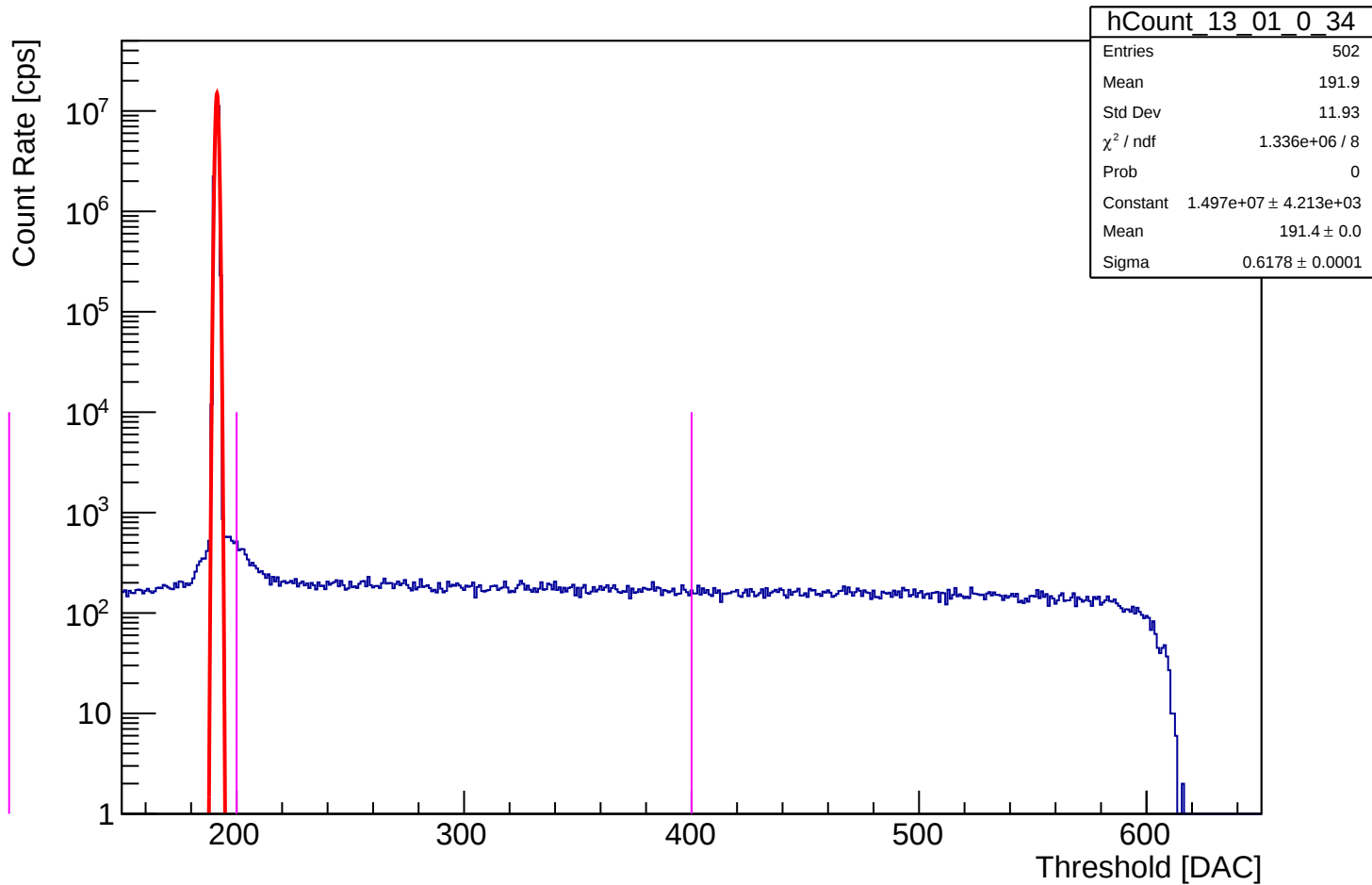
Row 1 Tile 1 Pmt 4 Pixel 4 Slot 13 Fiber 1 Asic 0 Channel 28



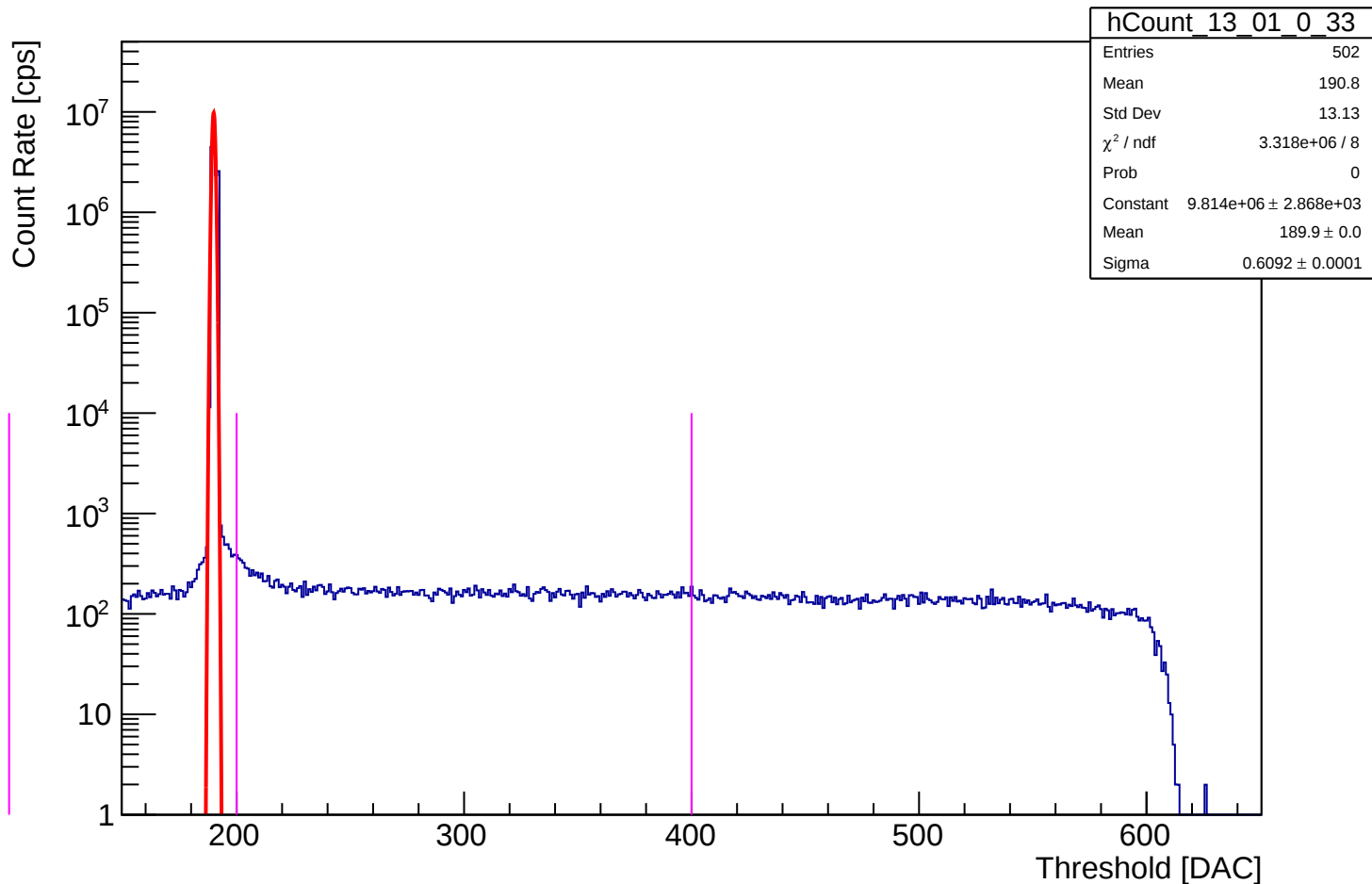
Row 1 Tile 1 Pmt 4 Pixel 5 Slot 13 Fiber 1 Asic 0 Channel 32



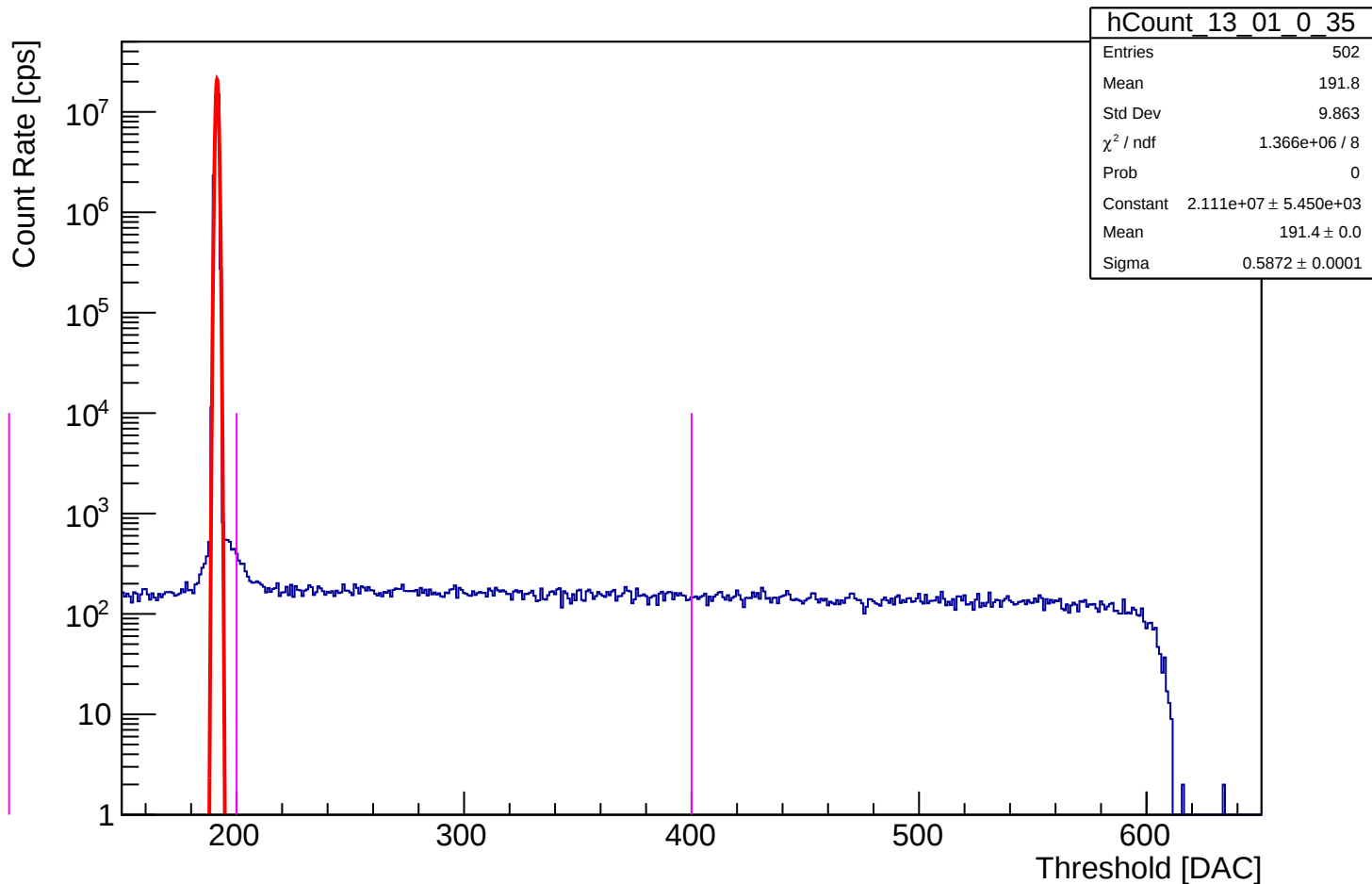
Row 1 Tile 1 Pmt 4 Pixel 6 Slot 13 Fiber 1 Asic 0 Channel 34



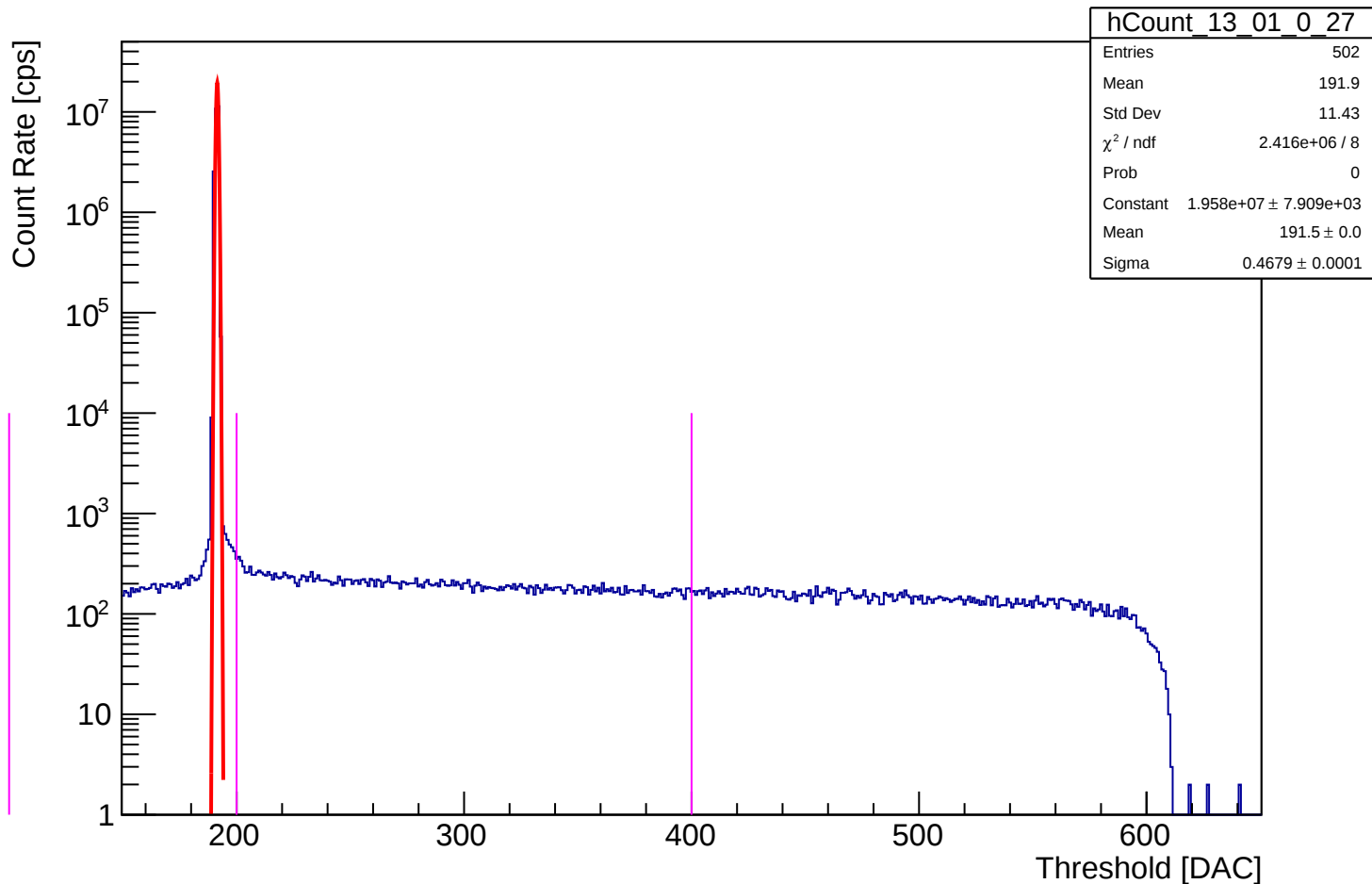
Row 1 Tile 1 Pmt 4 Pixel 7 Slot 13 Fiber 1 Asic 0 Channel 33



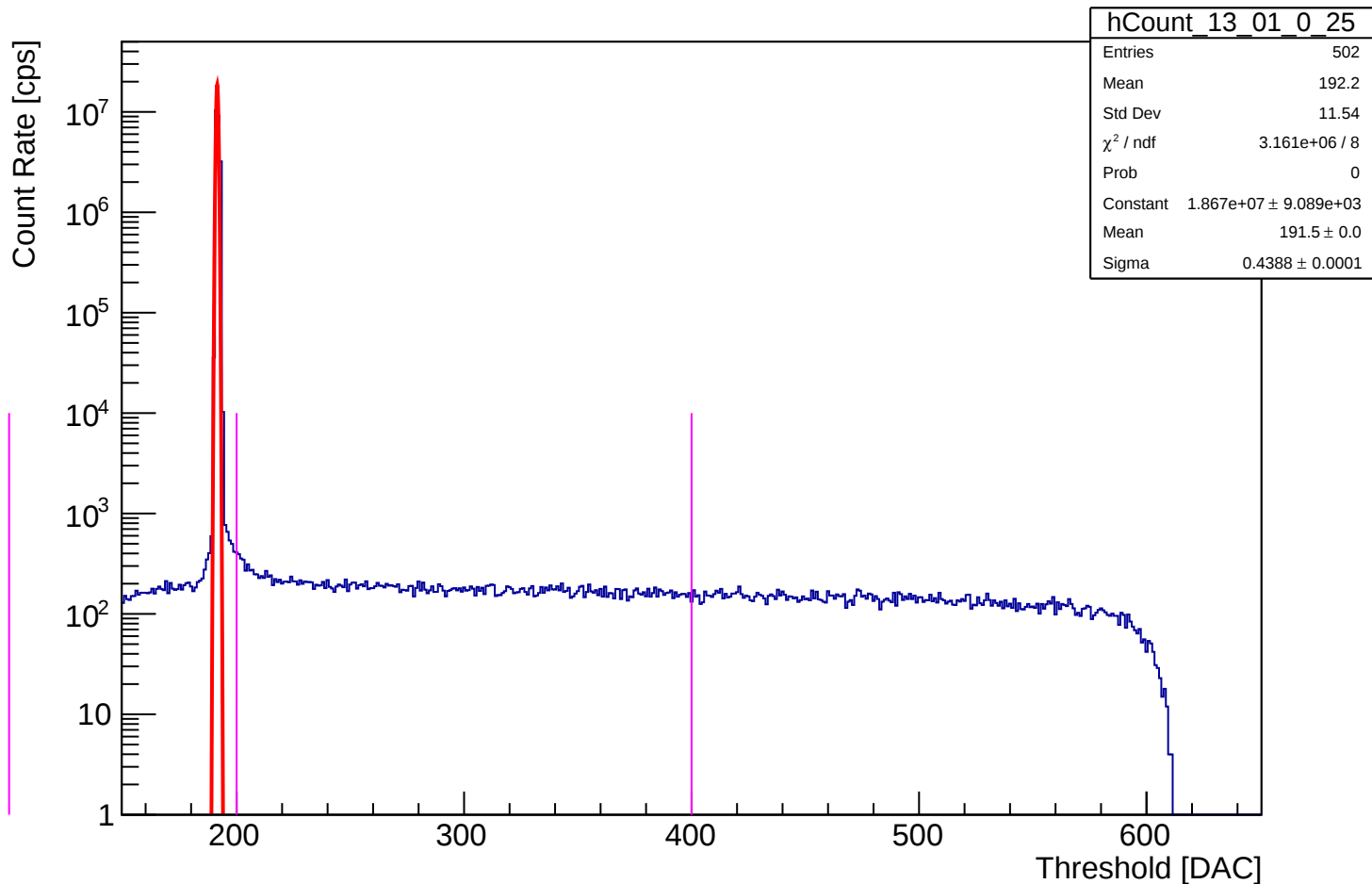
Row 1 Tile 1 Pmt 4 Pixel 8 Slot 13 Fiber 1 Asic 0 Channel 35



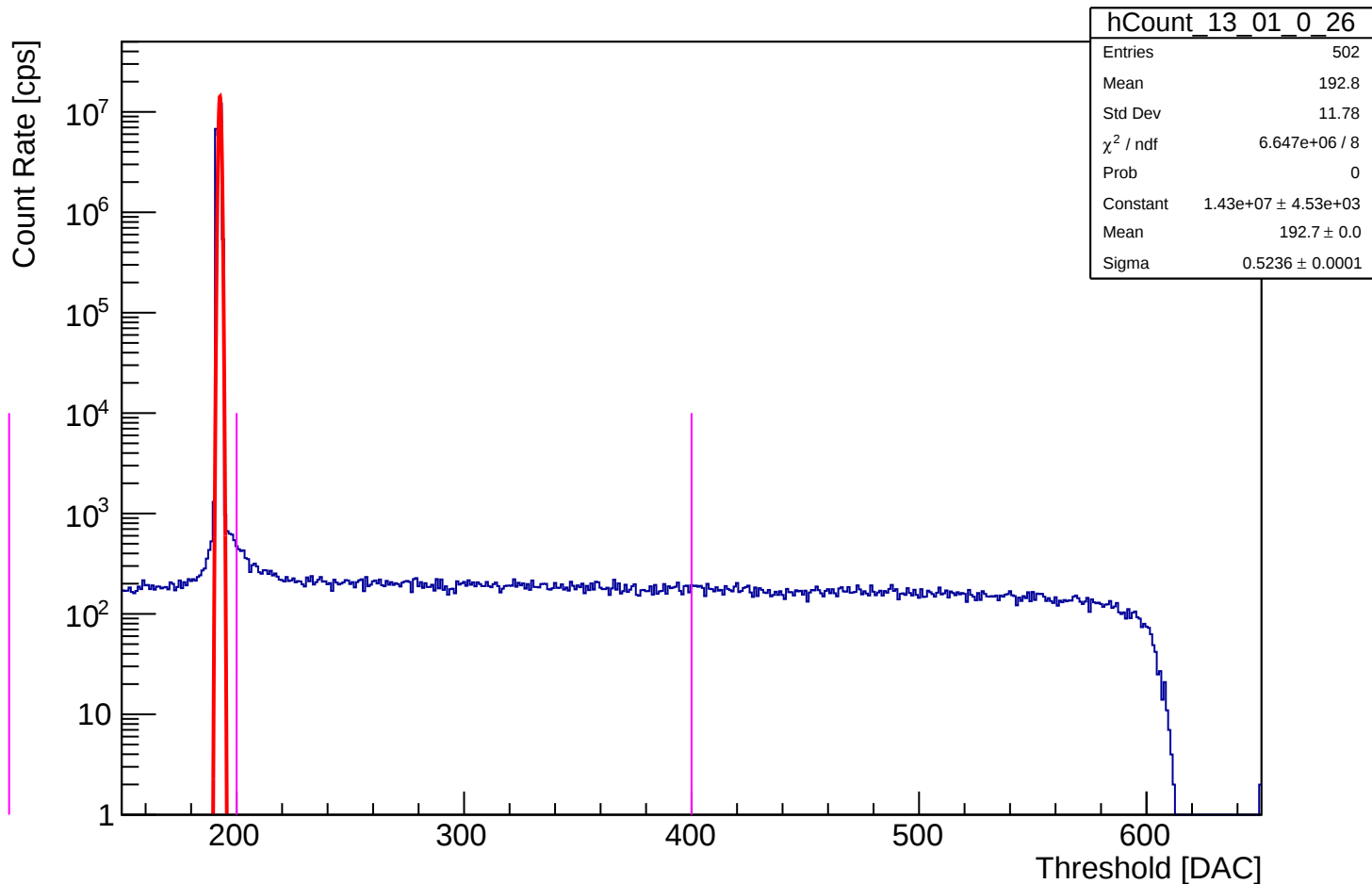
Row 1 Tile 1 Pmt 4 Pixel 9 Slot 13 Fiber 1 Asic 0 Channel 27



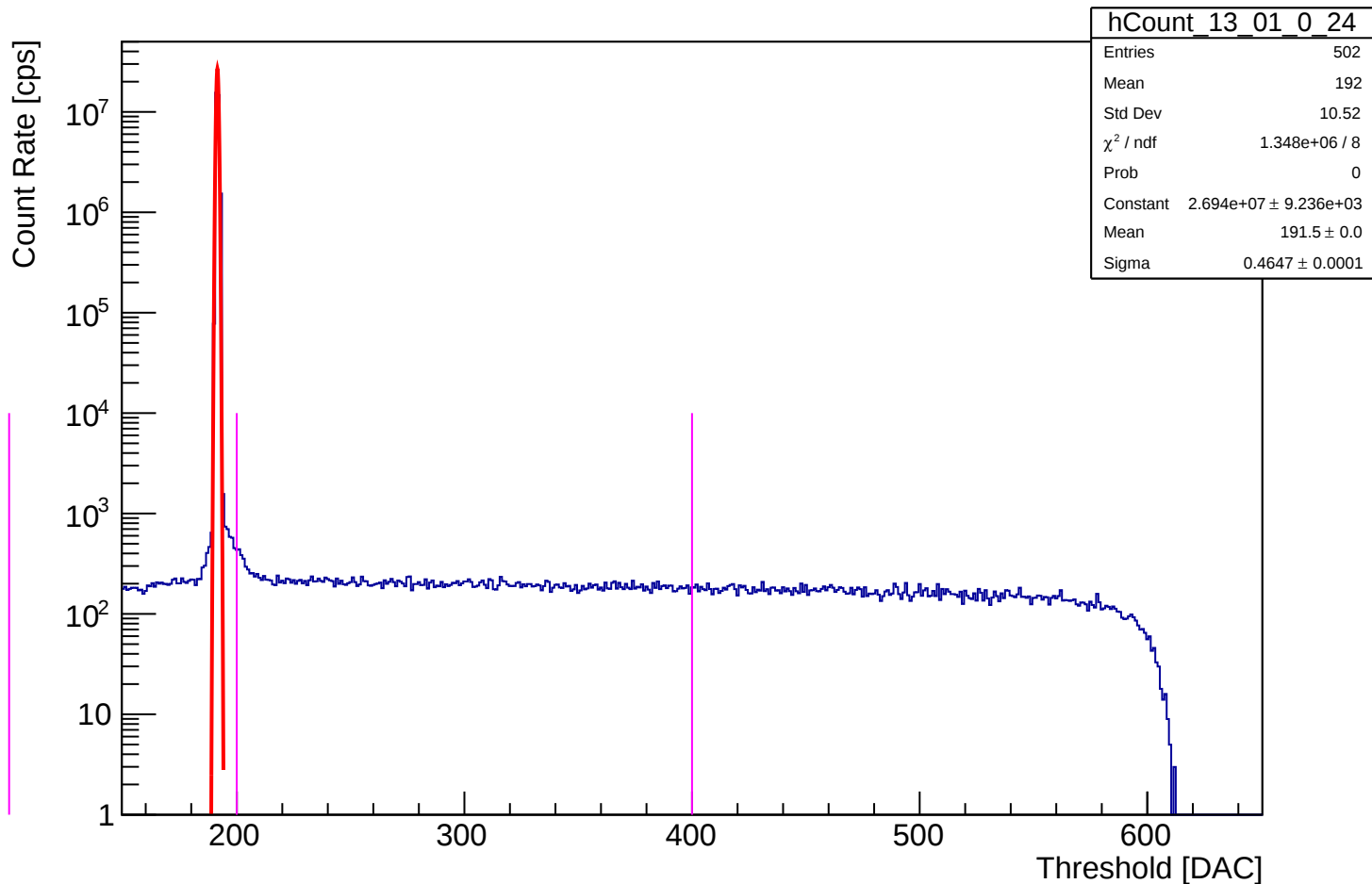
Row 1 Tile 1 Pmt 4 Pixel 10 Slot 13 Fiber 1 Asic 0 Channel 25



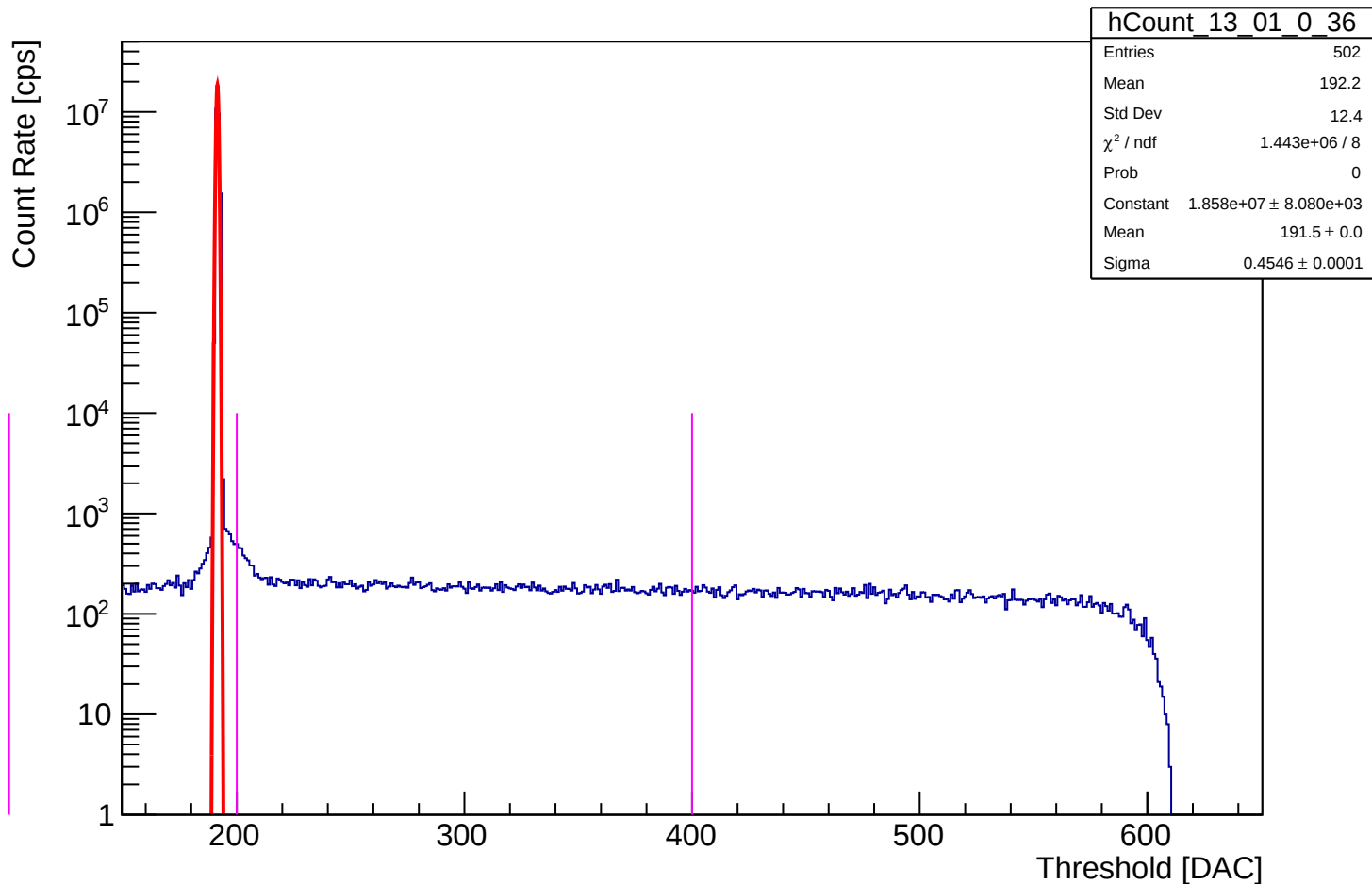
Row 1 Tile 1 Pmt 4 Pixel 11 Slot 13 Fiber 1 Asic 0 Channel 26



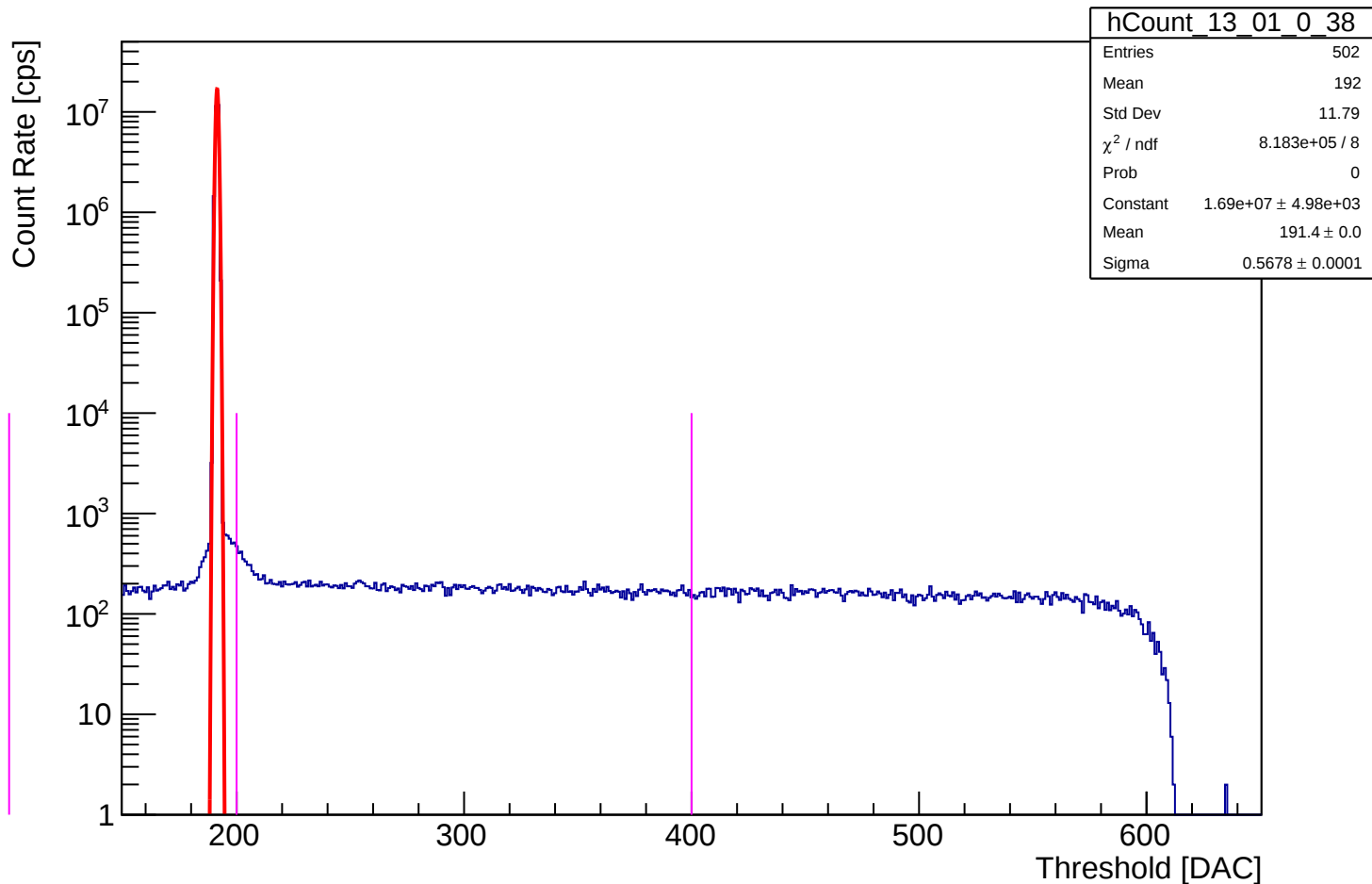
Row 1 Tile 1 Pmt 4 Pixel 12 Slot 13 Fiber 1 Asic 0 Channel 24



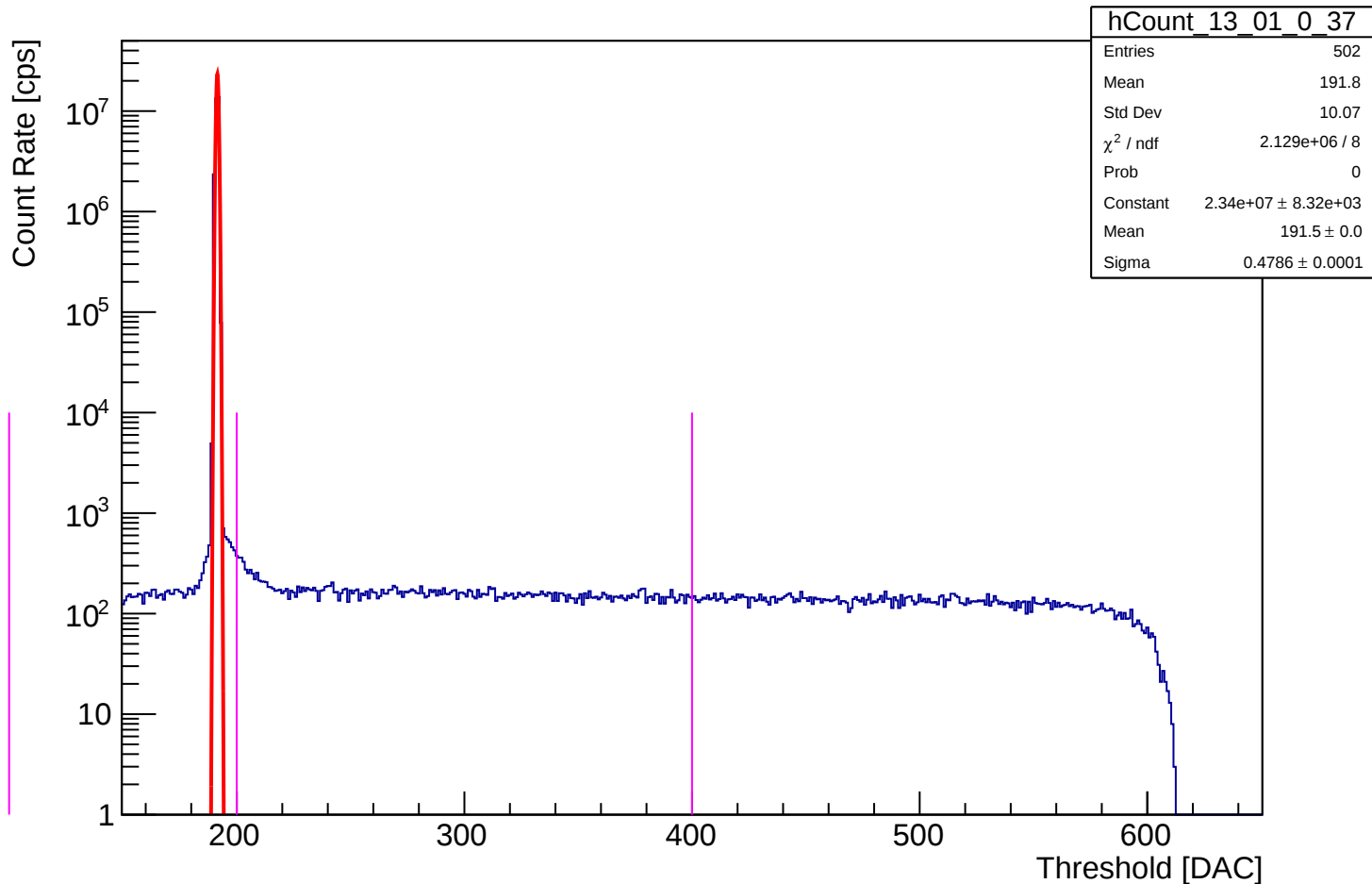
Row 1 Tile 1 Pmt 4 Pixel 13 Slot 13 Fiber 1 Asic 0 Channel 36



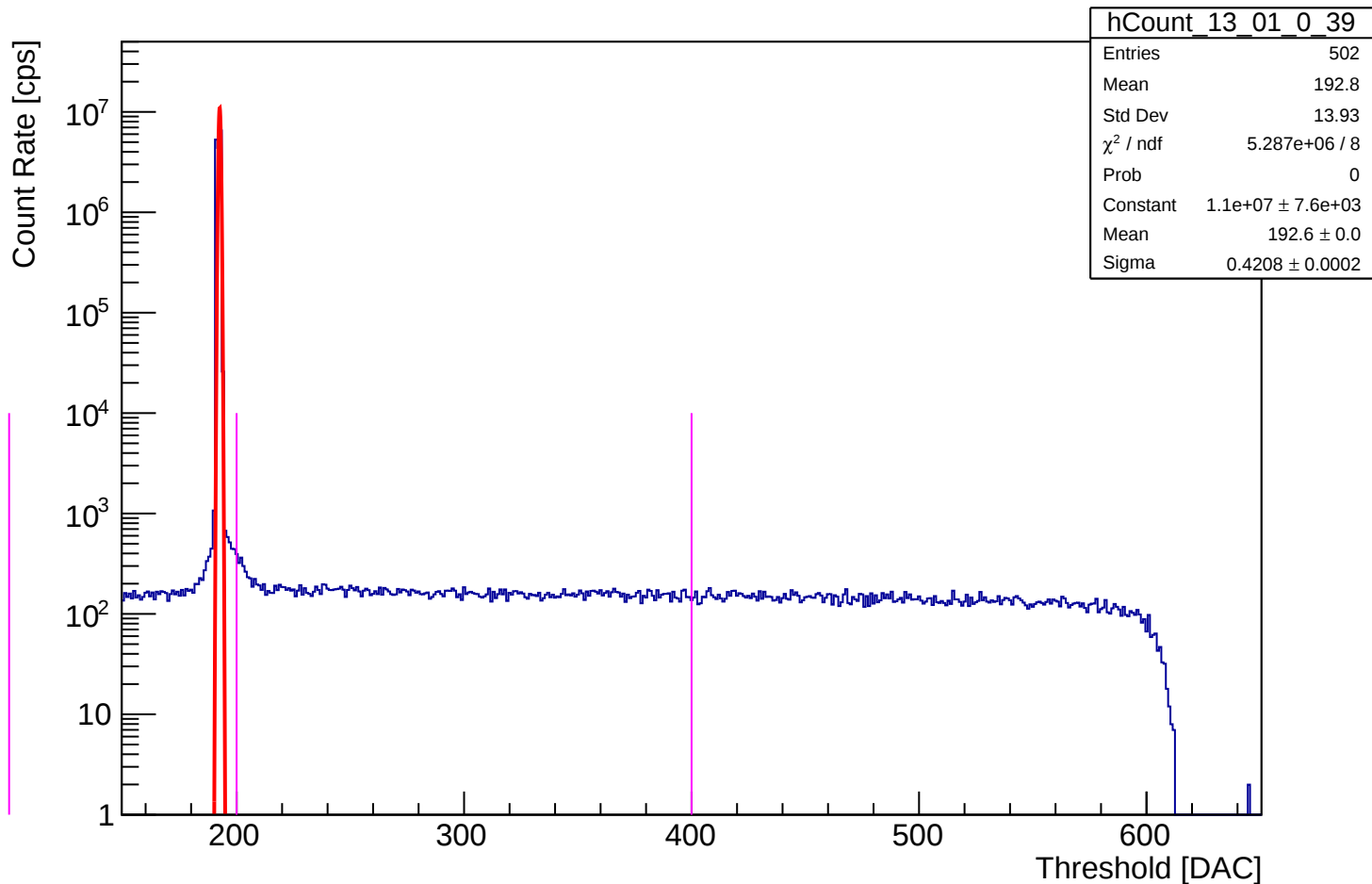
Row 1 Tile 1 Pmt 4 Pixel 14 Slot 13 Fiber 1 Asic 0 Channel 38



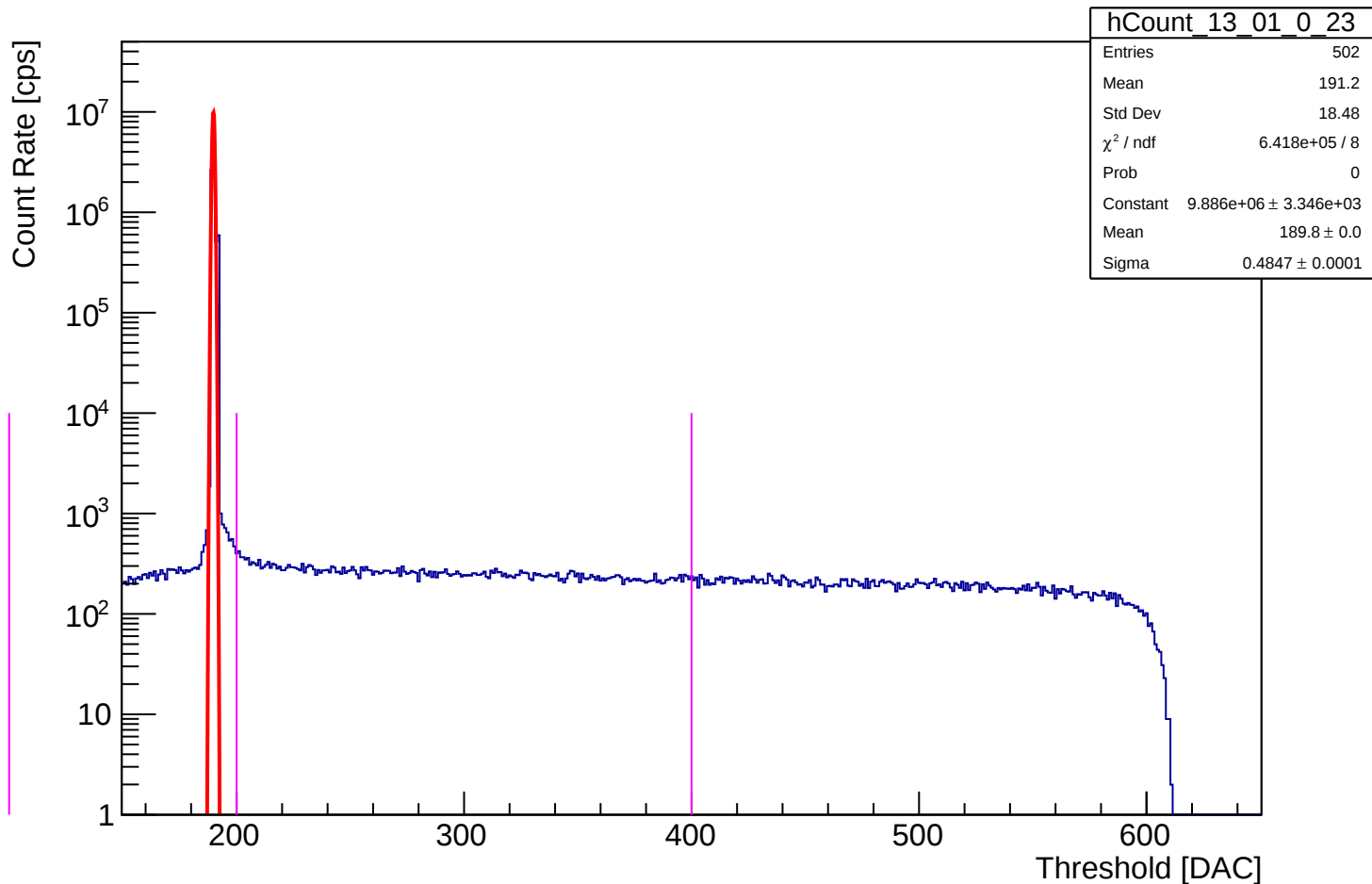
Row 1 Tile 1 Pmt 4 Pixel 15 Slot 13 Fiber 1 Asic 0 Channel 37



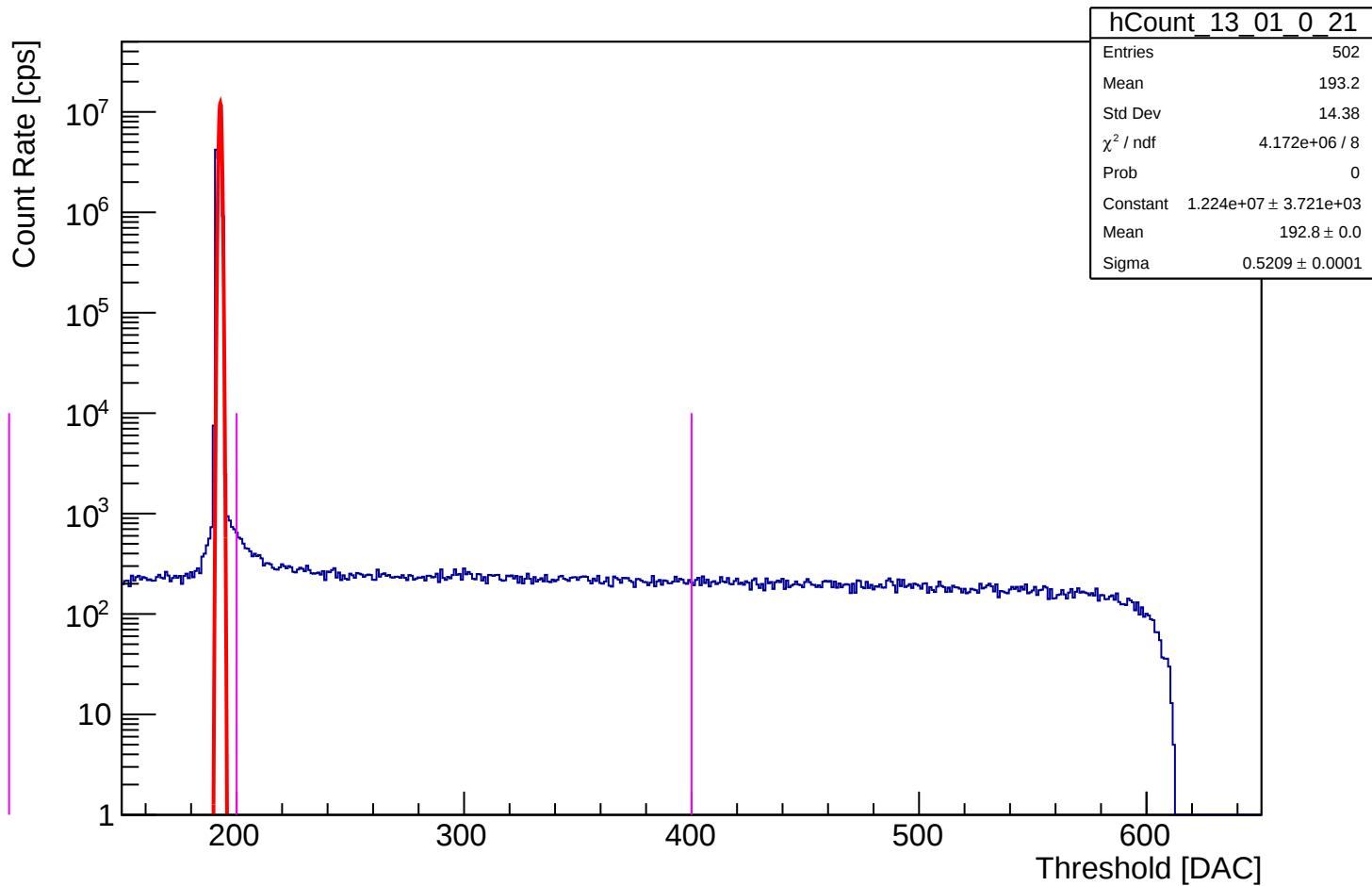
Row 1 Tile 1 Pmt 4 Pixel 16 Slot 13 Fiber 1 Asic 0 Channel 39



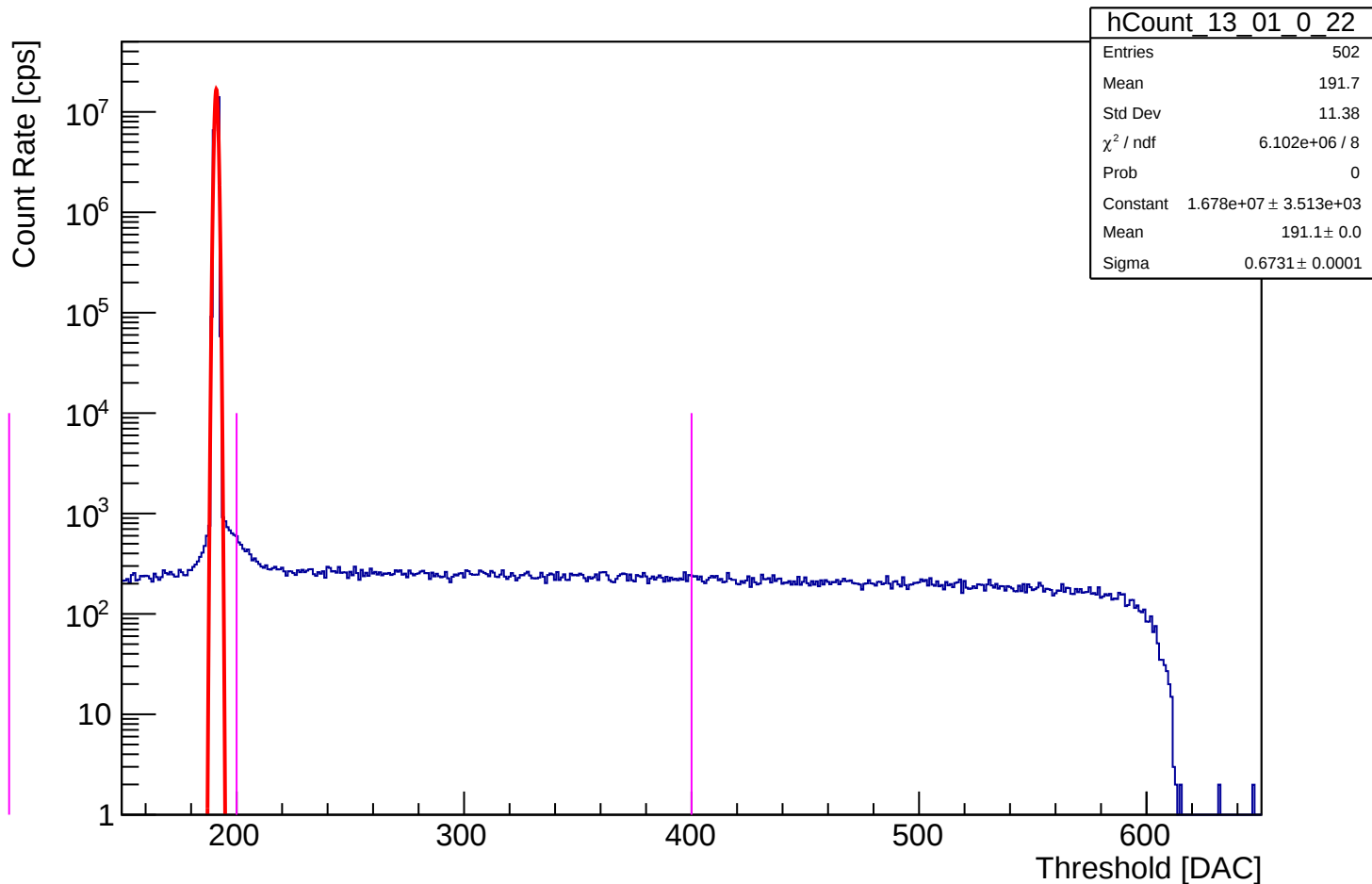
Row 1 Tile 1 Pmt 4 Pixel 17 Slot 13 Fiber 1 Asic 0 Channel 23



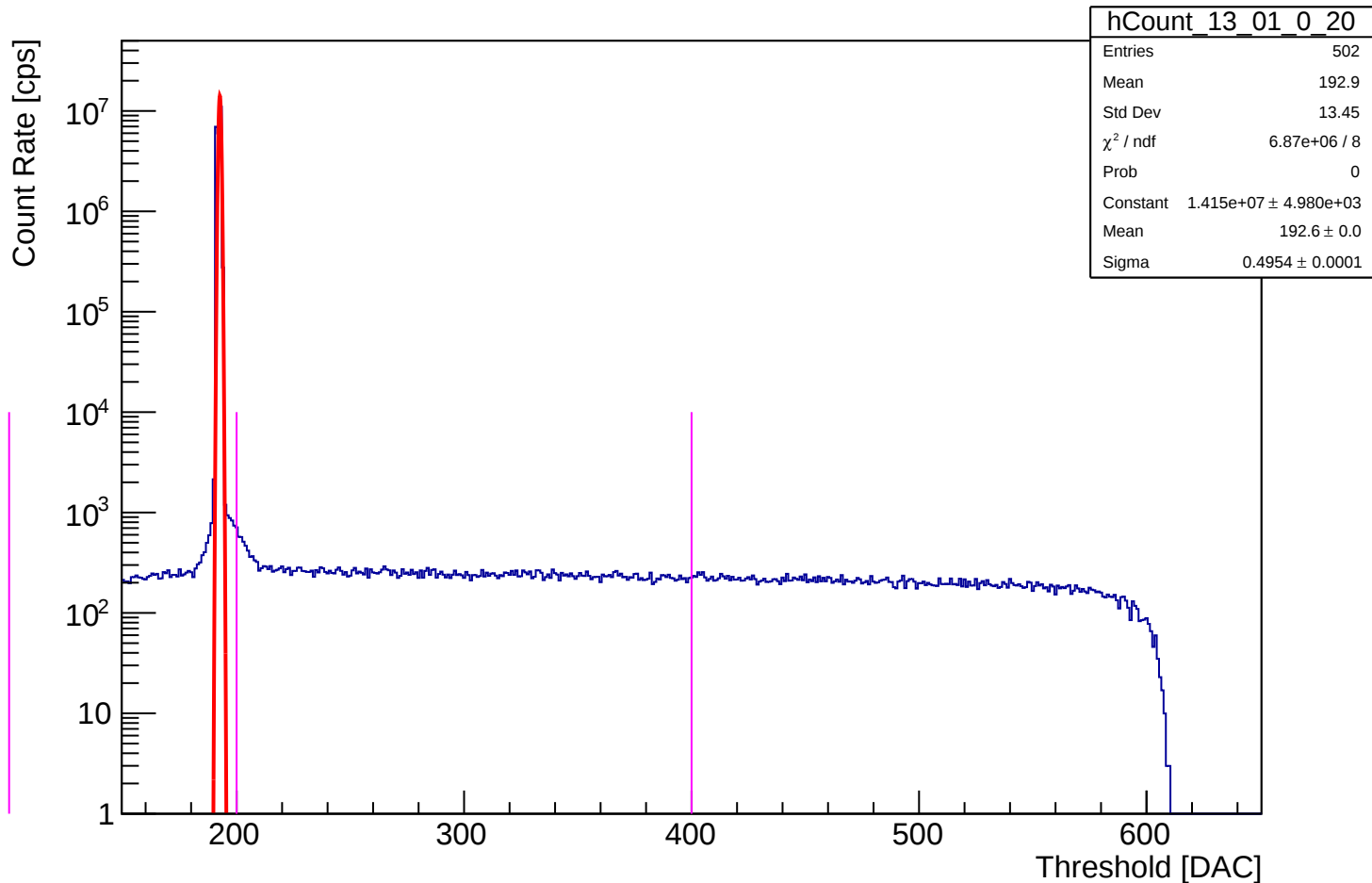
Row 1 Tile 1 Pmt 4 Pixel 18 Slot 13 Fiber 1 Asic 0 Channel 21



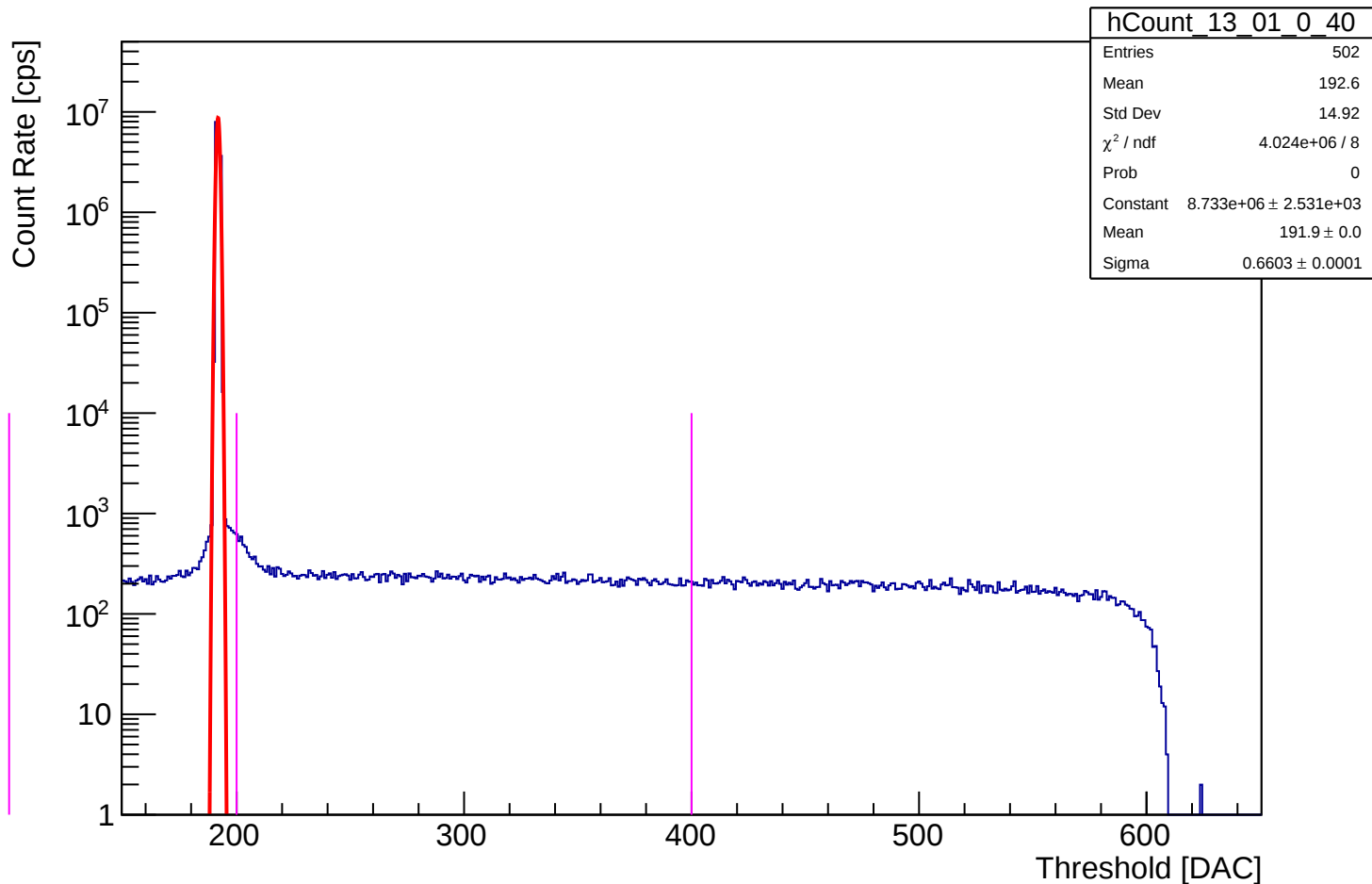
Row 1 Tile 1 Pmt 4 Pixel 19 Slot 13 Fiber 1 Asic 0 Channel 22



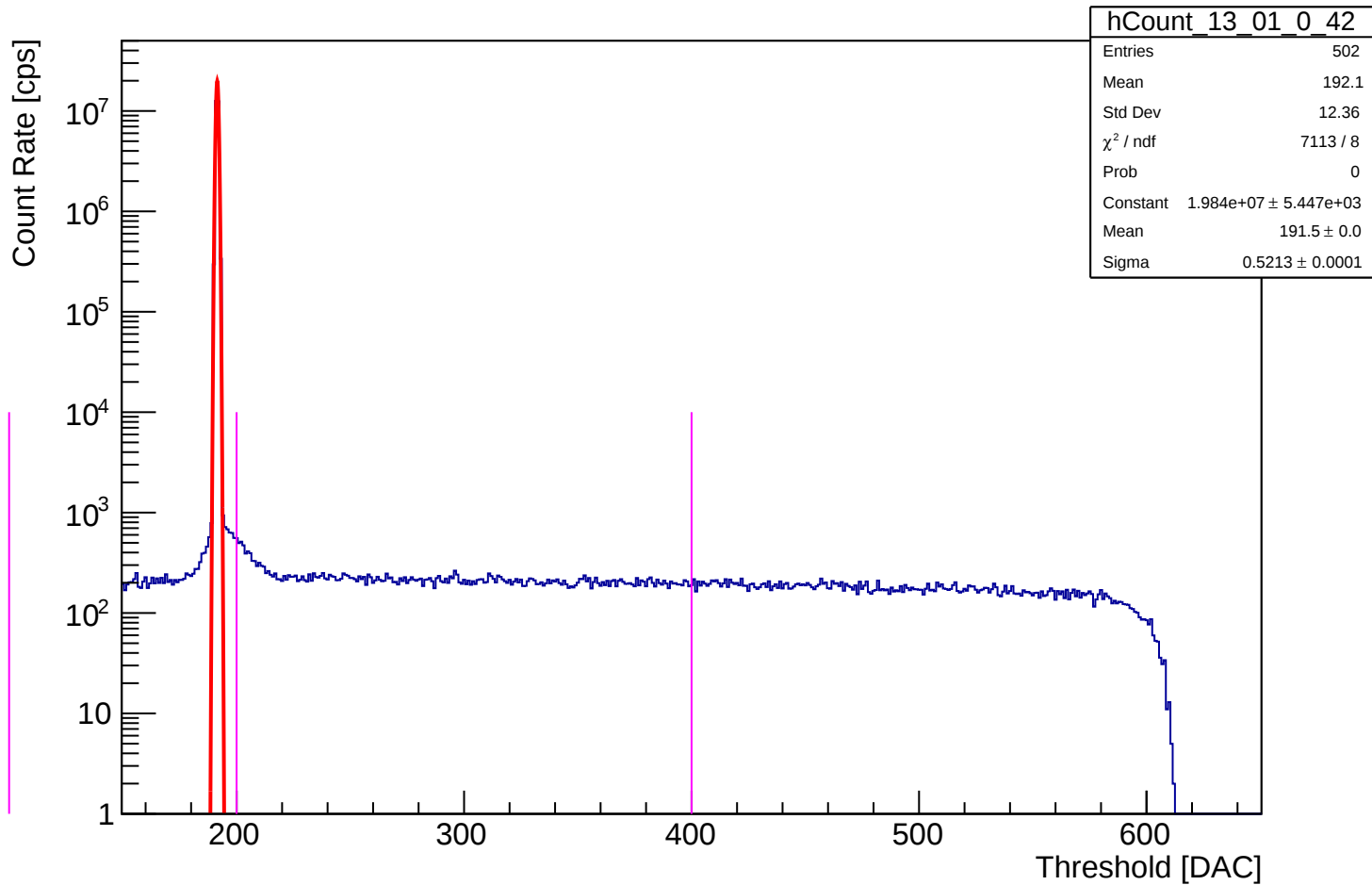
Row 1 Tile 1 Pmt 4 Pixel 20 Slot 13 Fiber 1 Asic 0 Channel 20



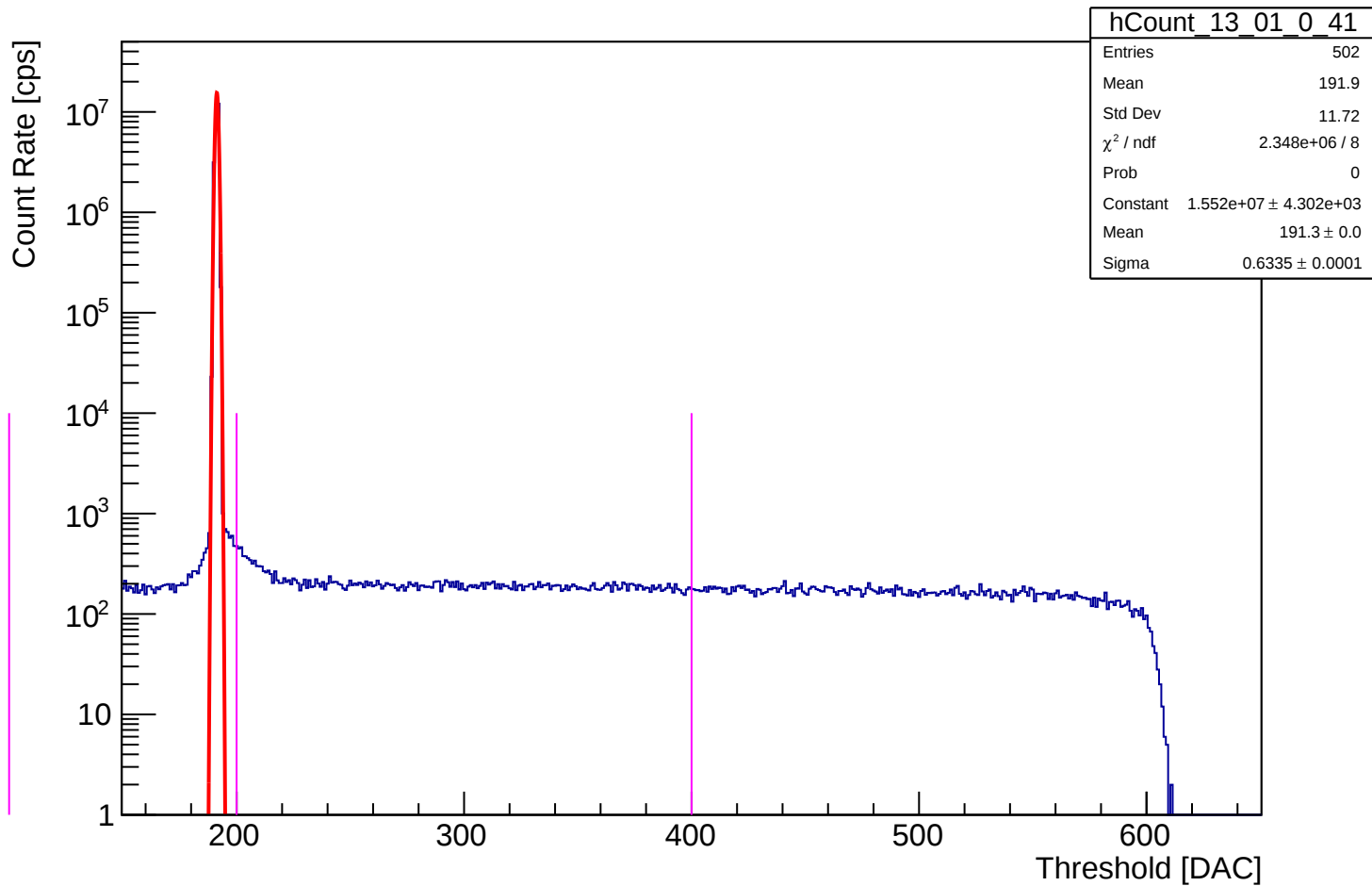
Row 1 Tile 1 Pmt 4 Pixel 21 Slot 13 Fiber 1 Asic 0 Channel 40



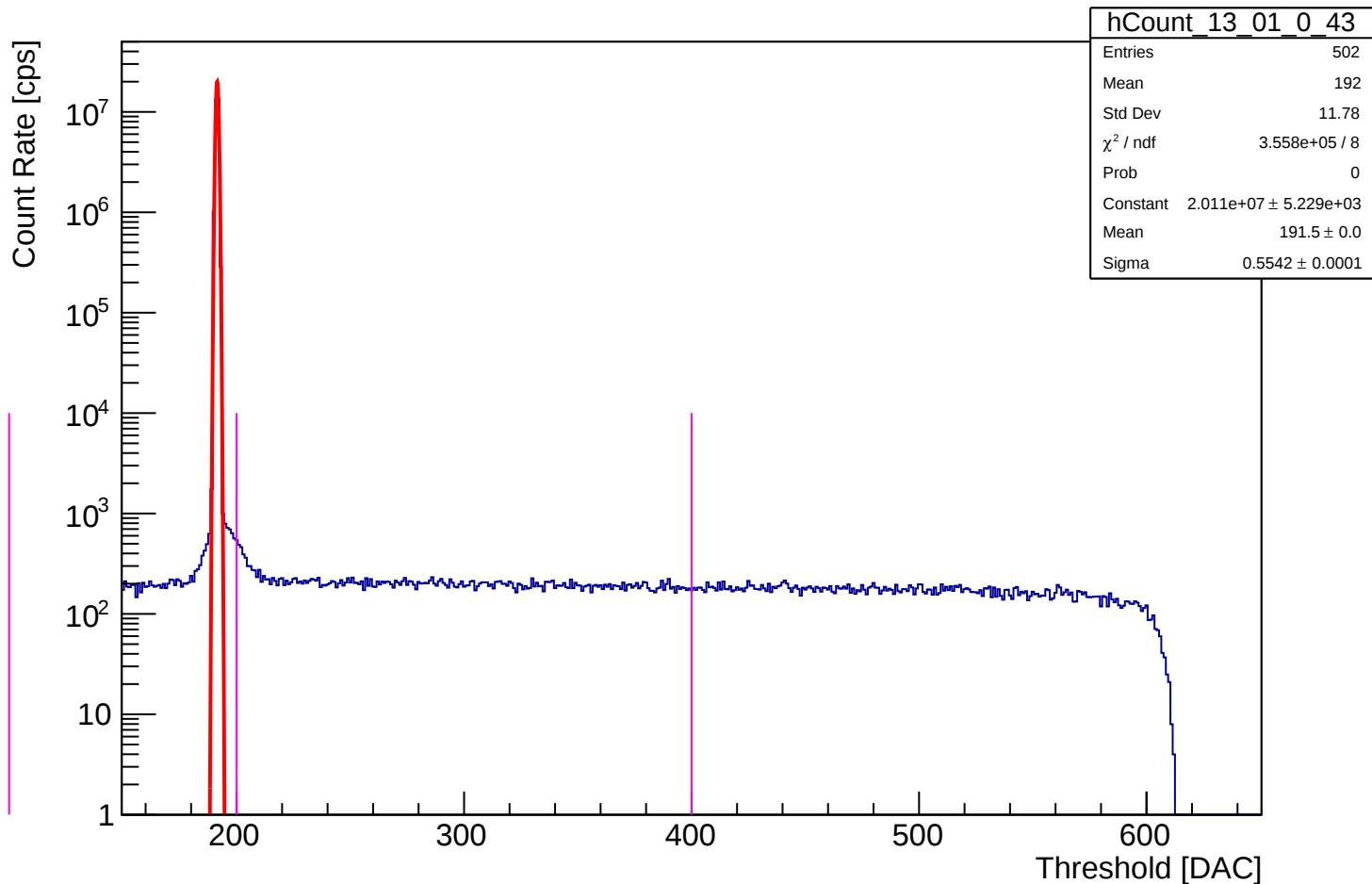
Row 1 Tile 1 Pmt 4 Pixel 22 Slot 13 Fiber 1 Asic 0 Channel 42



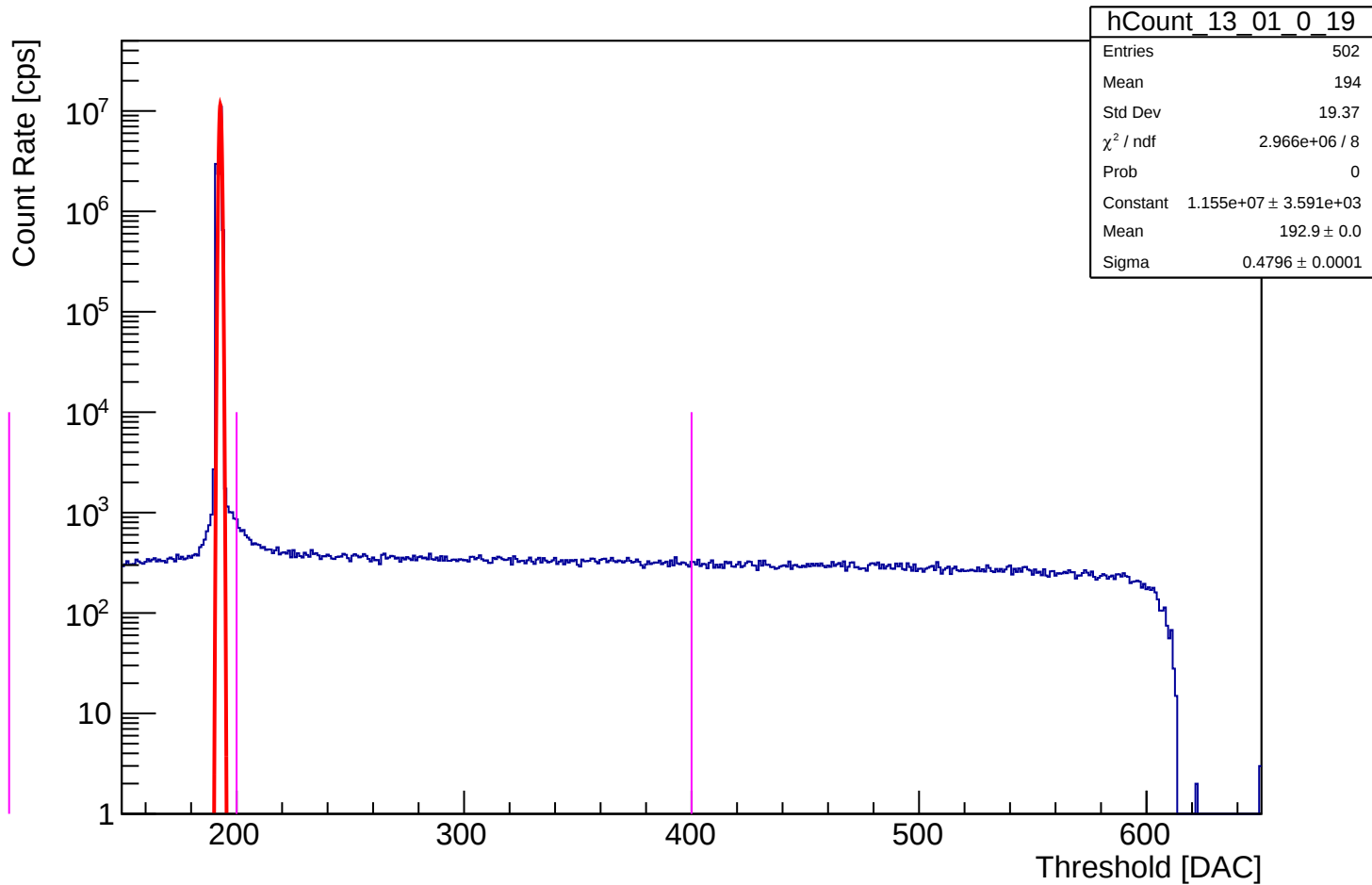
Row 1 Tile 1 Pmt 4 Pixel 23 Slot 13 Fiber 1 Asic 0 Channel 41



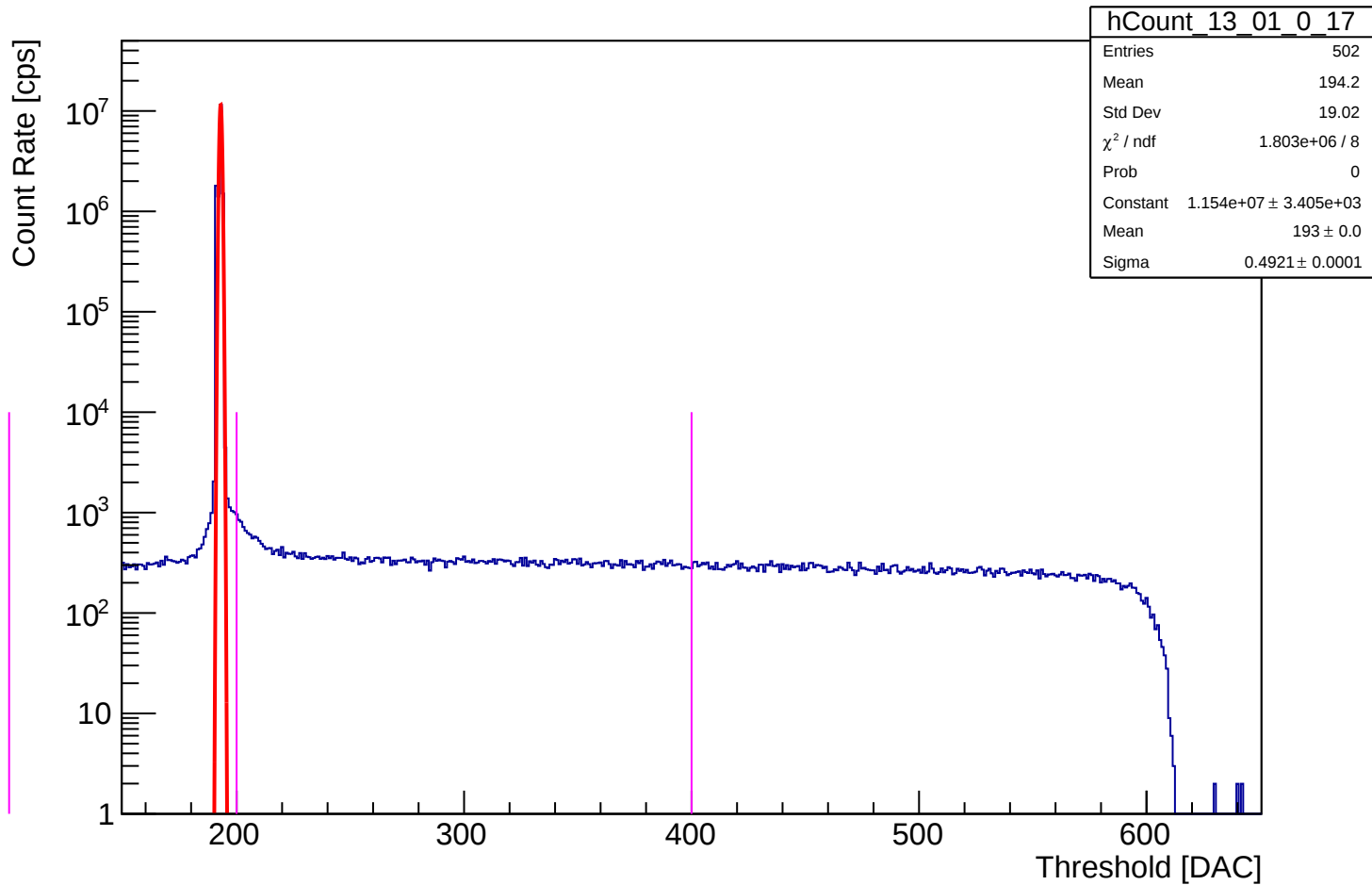
Row 1 Tile 1 Pmt 4 Pixel 24 Slot 13 Fiber 1 Asic 0 Channel 43



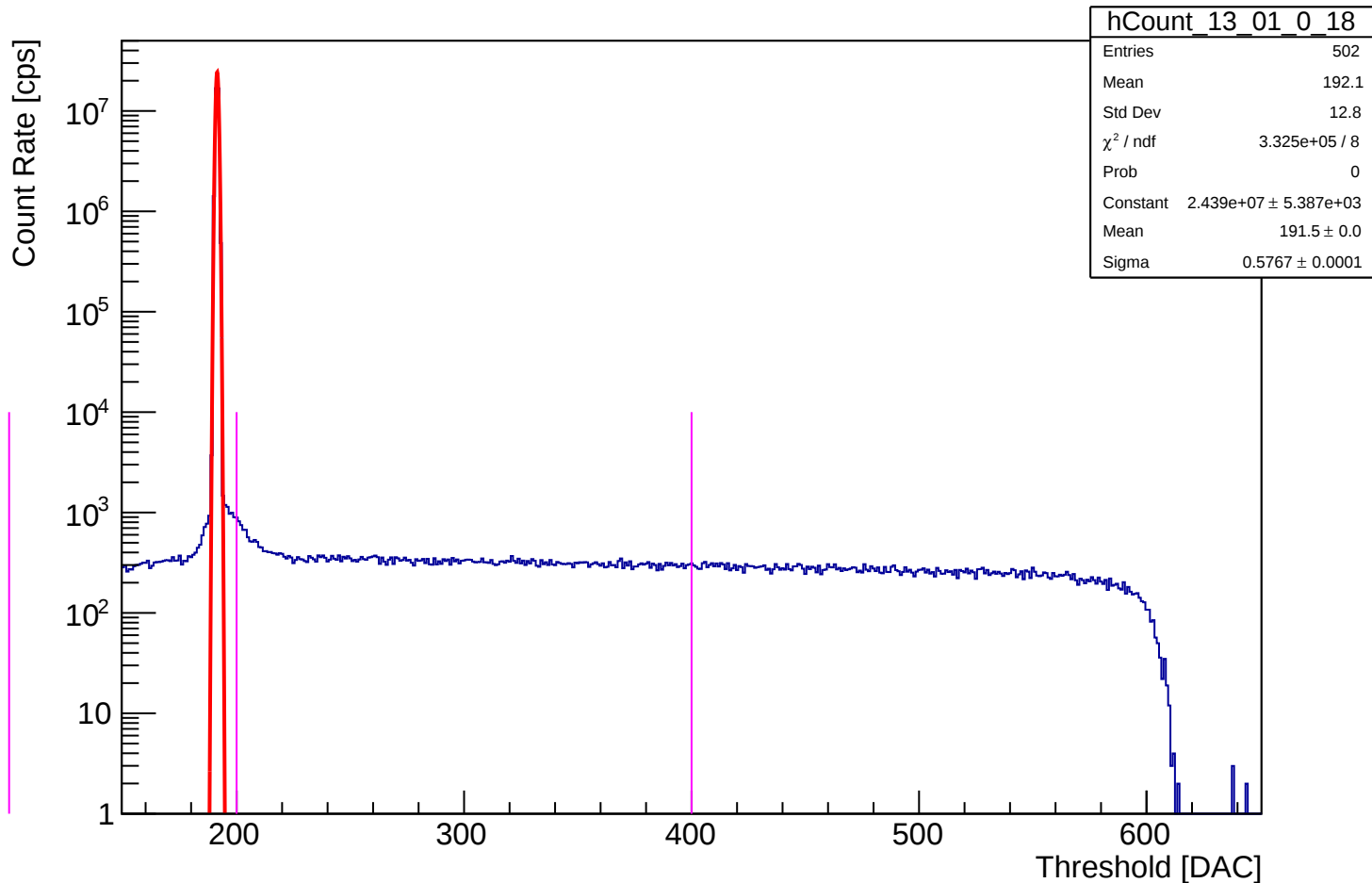
Row 1 Tile 1 Pmt 4 Pixel 25 Slot 13 Fiber 1 Asic 0 Channel 19



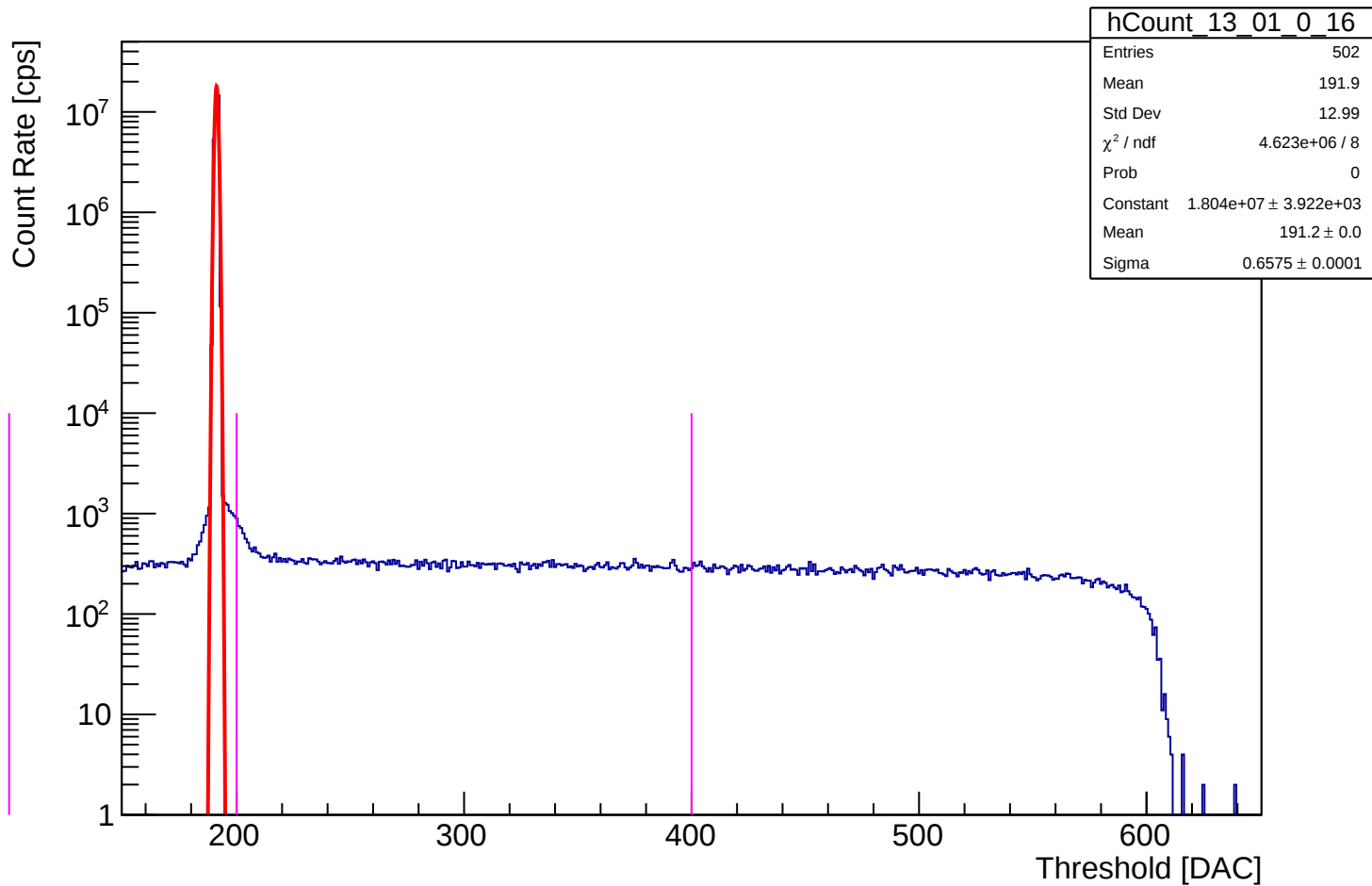
Row 1 Tile 1 Pmt 4 Pixel 26 Slot 13 Fiber 1 Asic 0 Channel 17



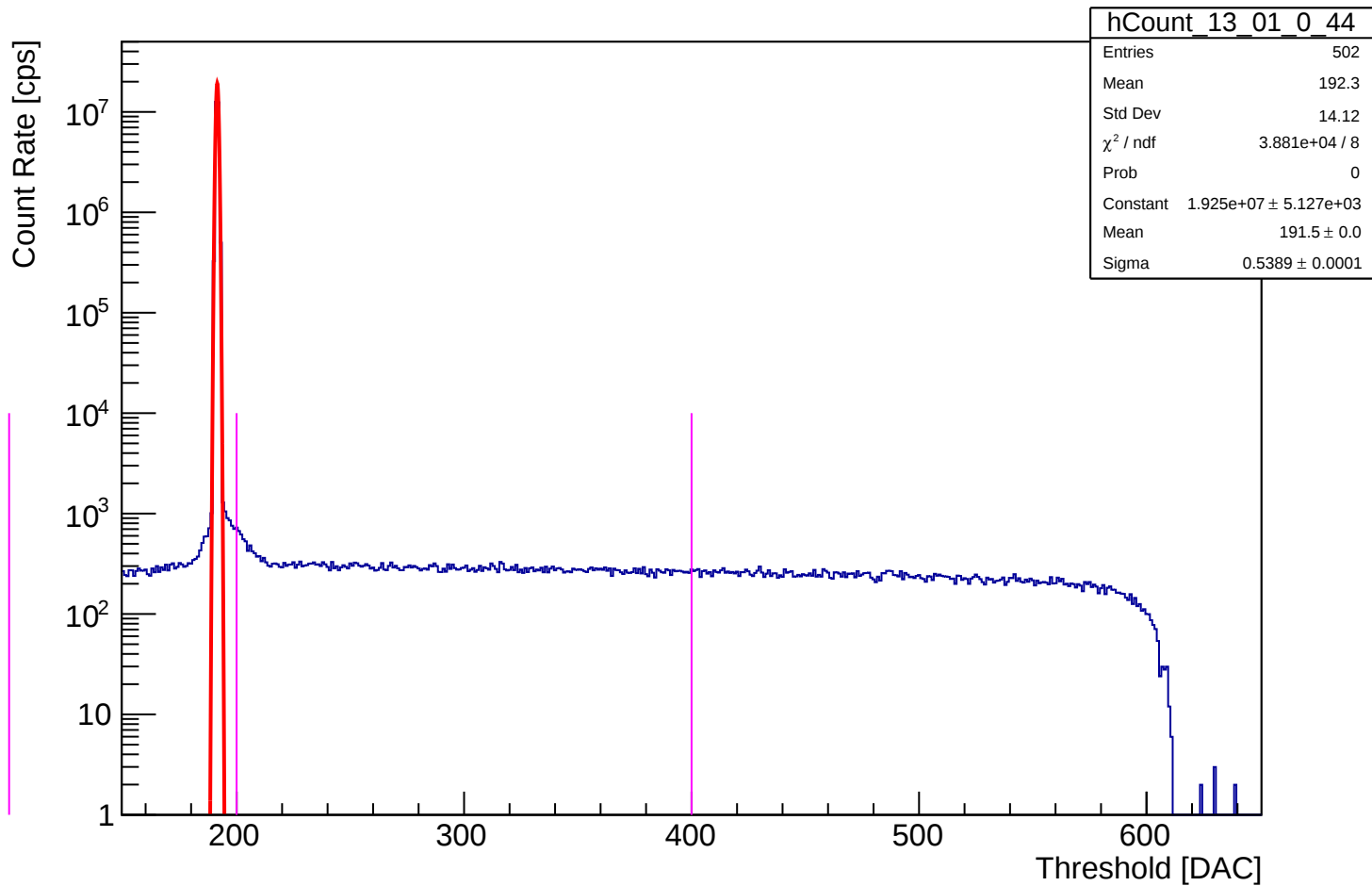
Row 1 Tile 1 Pmt 4 Pixel 27 Slot 13 Fiber 1 Asic 0 Channel 18



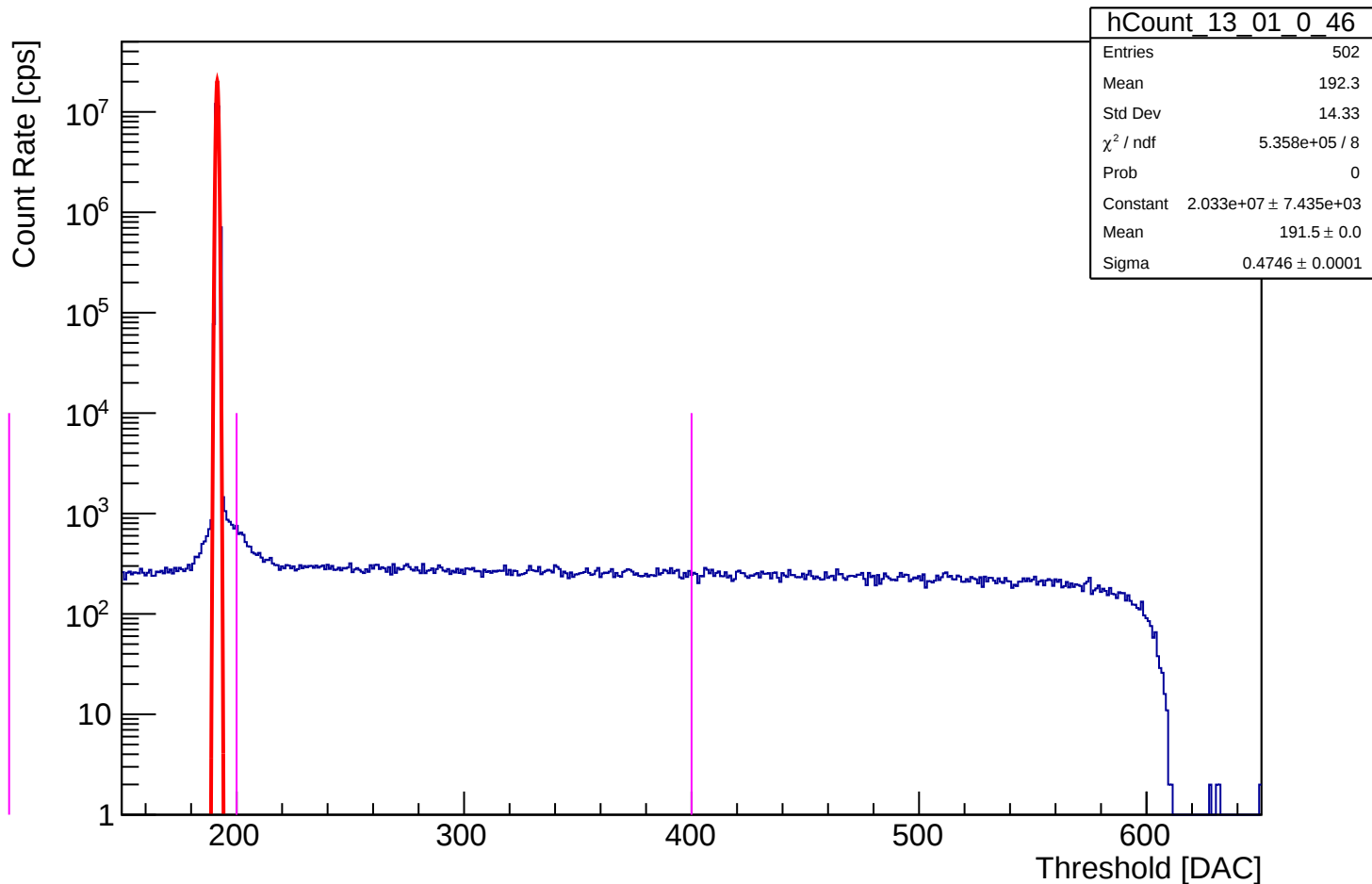
Row 1 Tile 1 Pmt 4 Pixel 28 Slot 13 Fiber 1 Asic 0 Channel 16



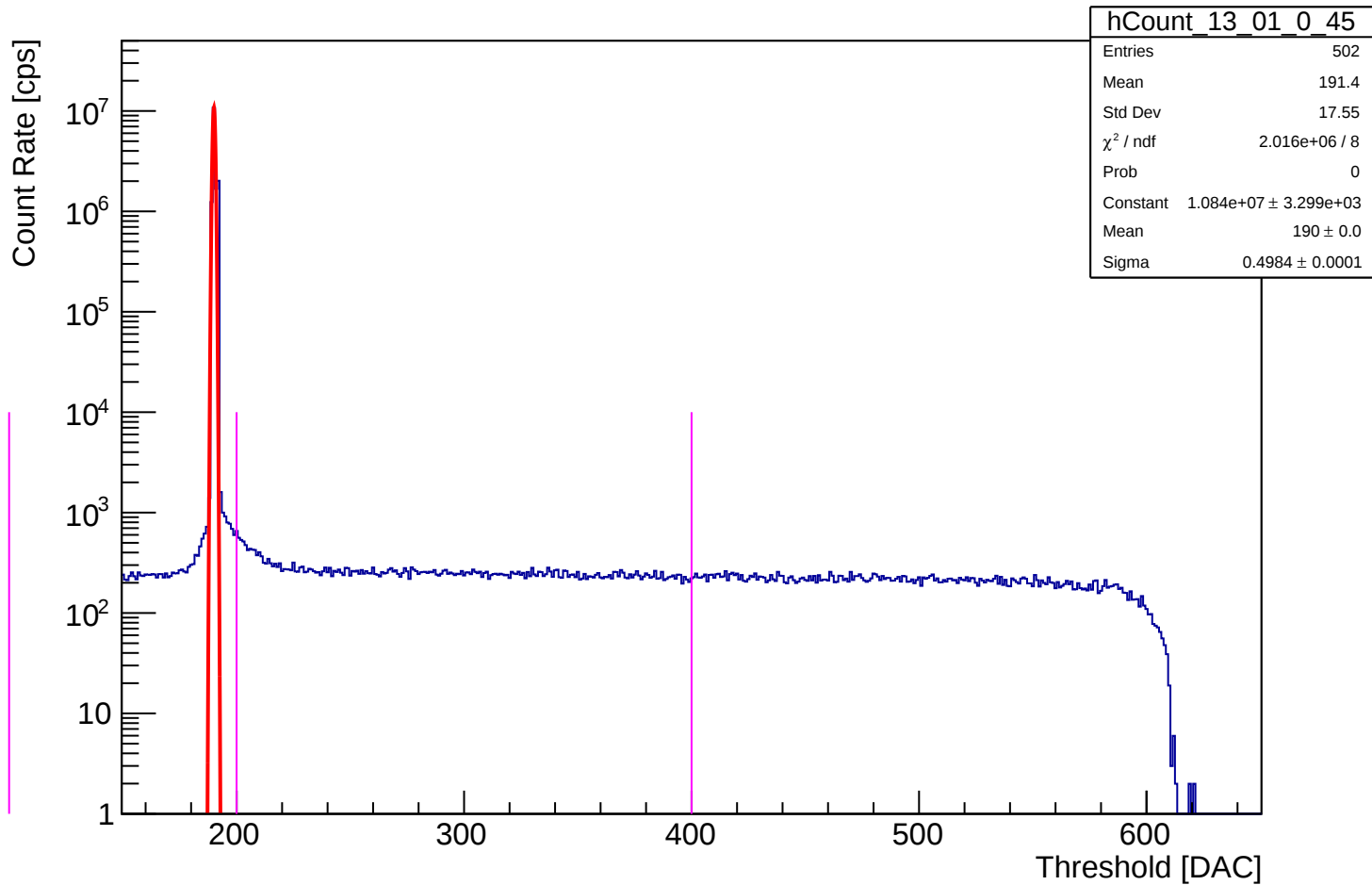
Row 1 Tile 1 Pmt 4 Pixel 29 Slot 13 Fiber 1 Asic 0 Channel 44



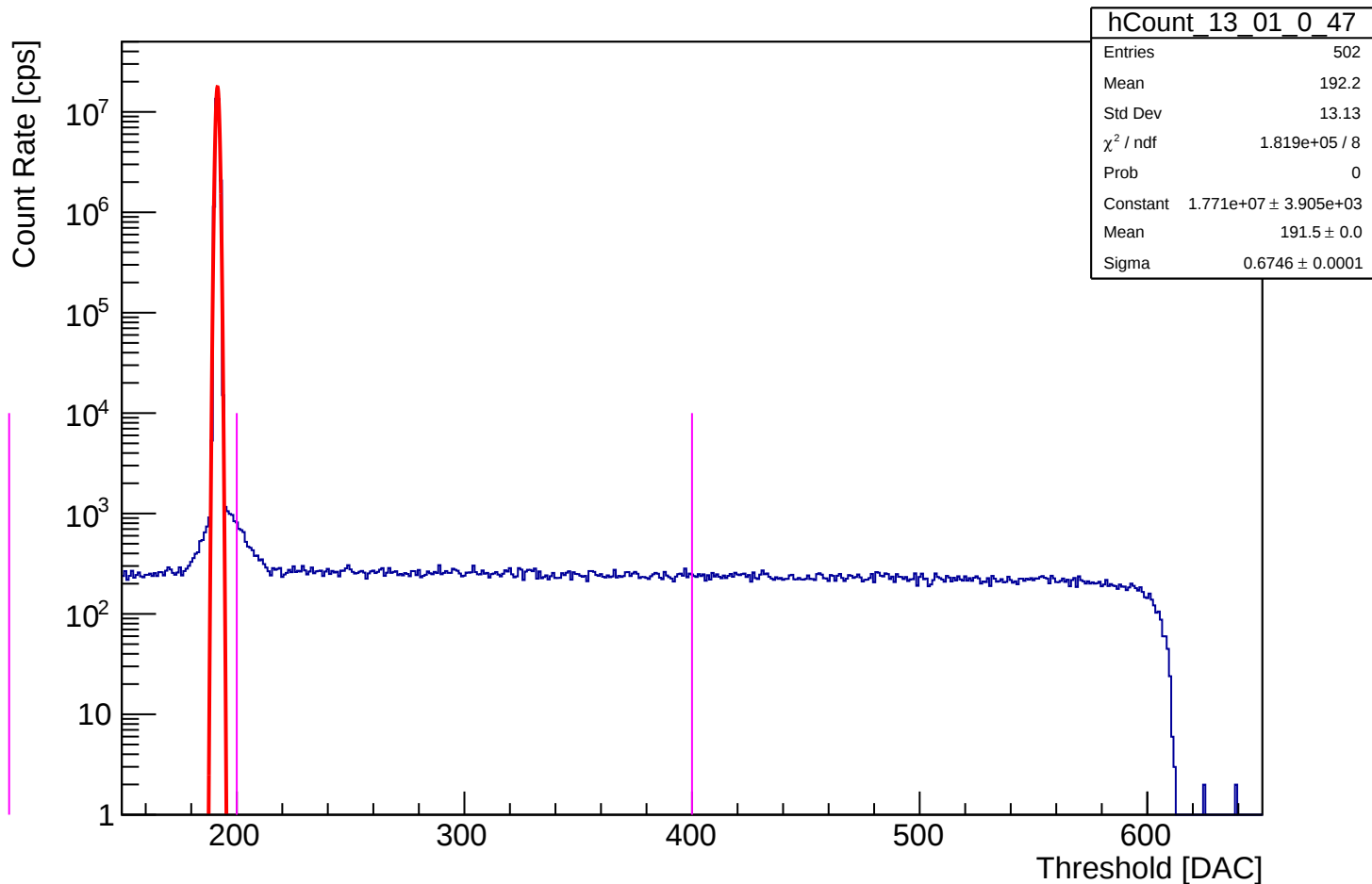
Row 1 Tile 1 Pmt 4 Pixel 30 Slot 13 Fiber 1 Asic 0 Channel 46



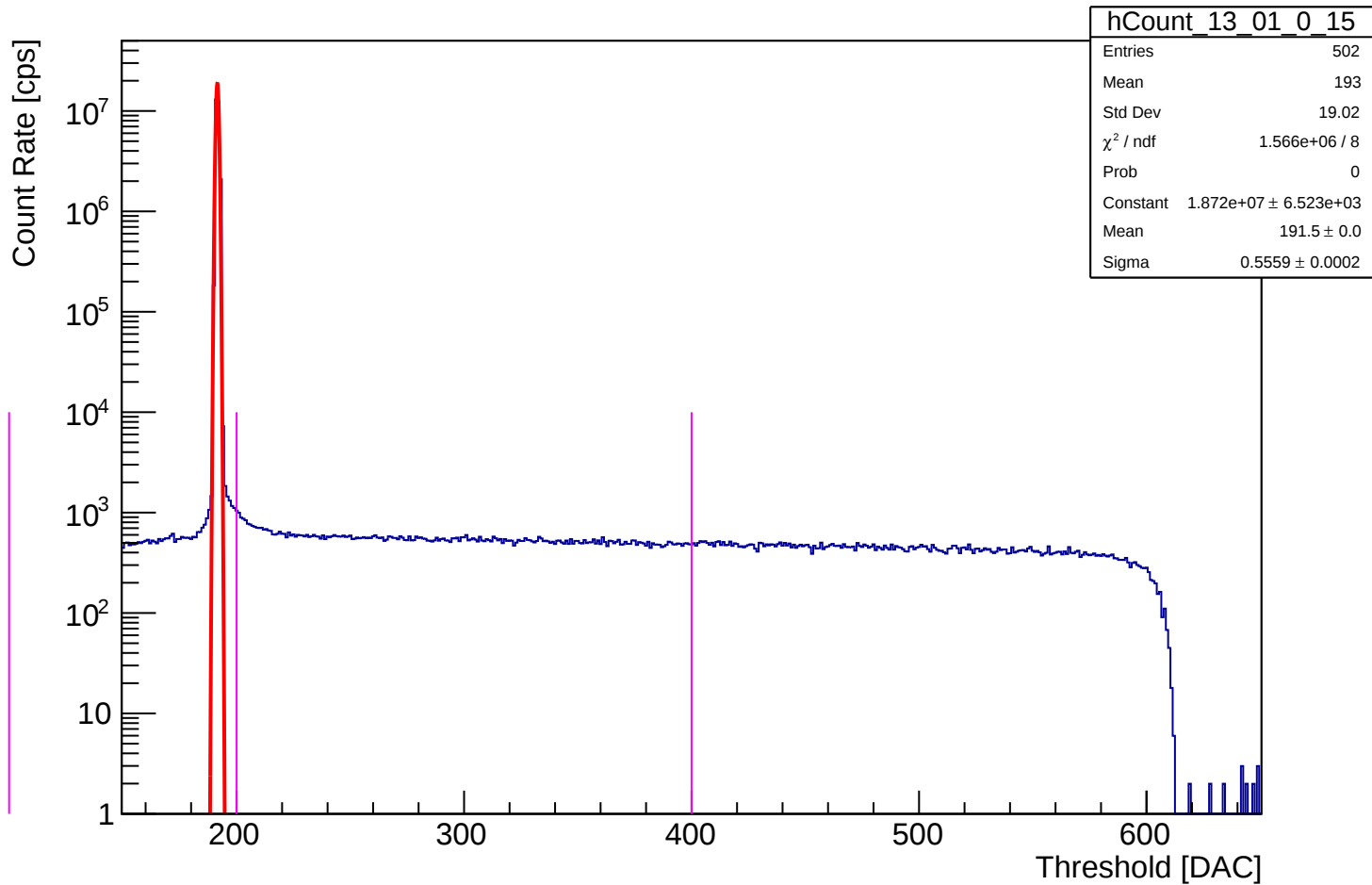
Row 1 Tile 1 Pmt 4 Pixel 31 Slot 13 Fiber 1 Asic 0 Channel 45



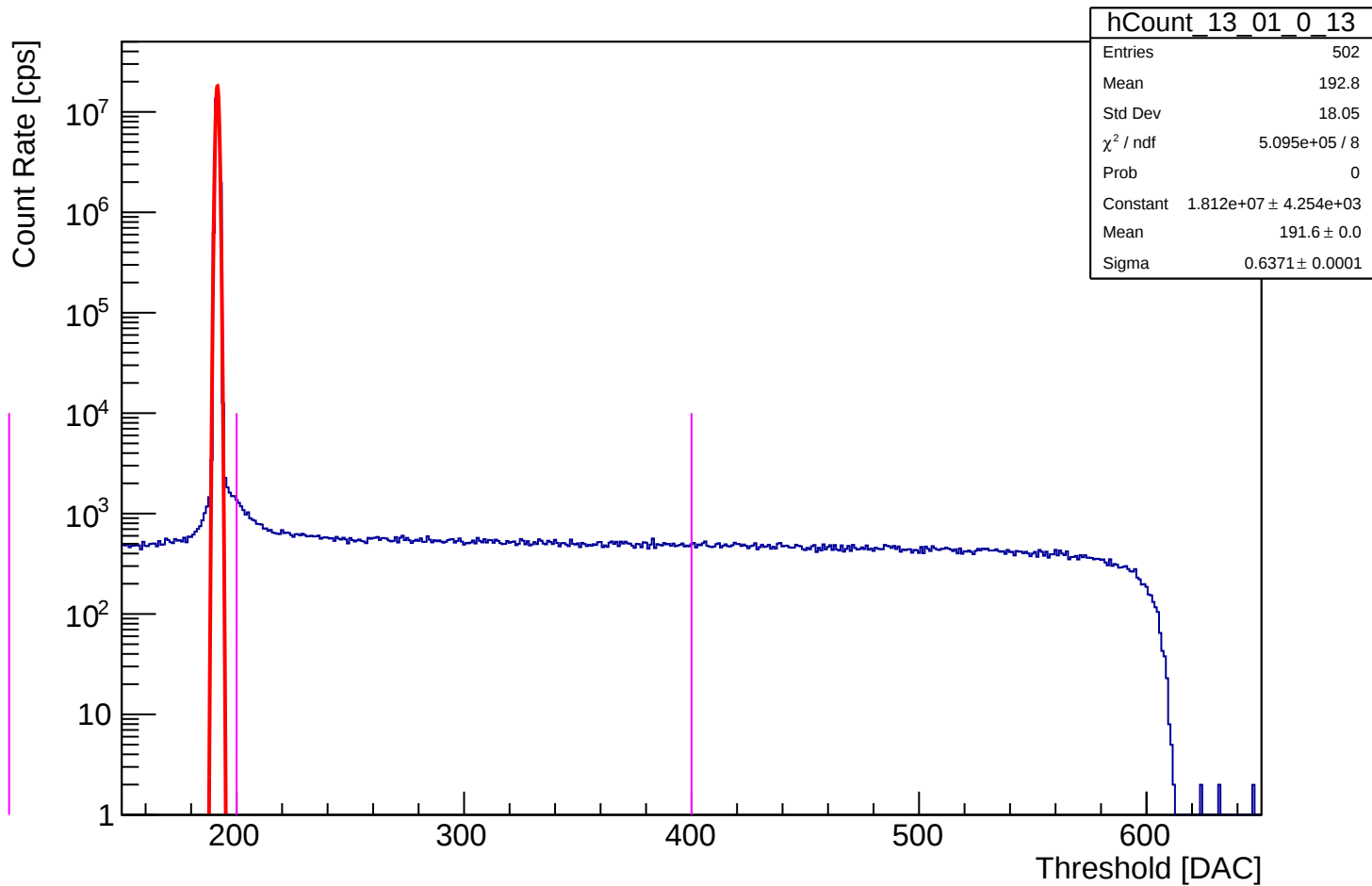
Row 1 Tile 1 Pmt 4 Pixel 32 Slot 13 Fiber 1 Asic 0 Channel 47



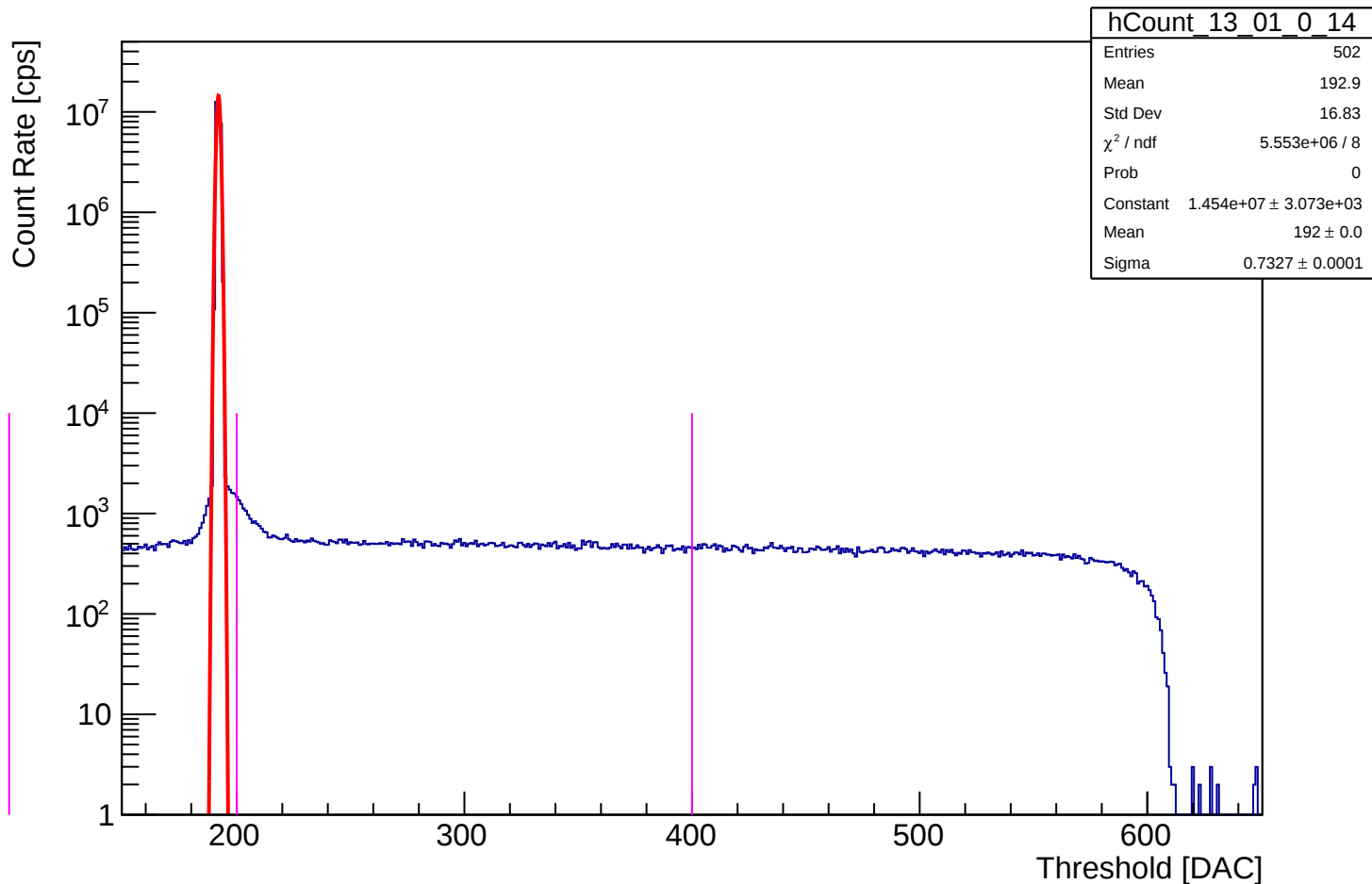
Row 1 Tile 1 Pmt 4 Pixel 33 Slot 13 Fiber 1 Asic 0 Channel 15



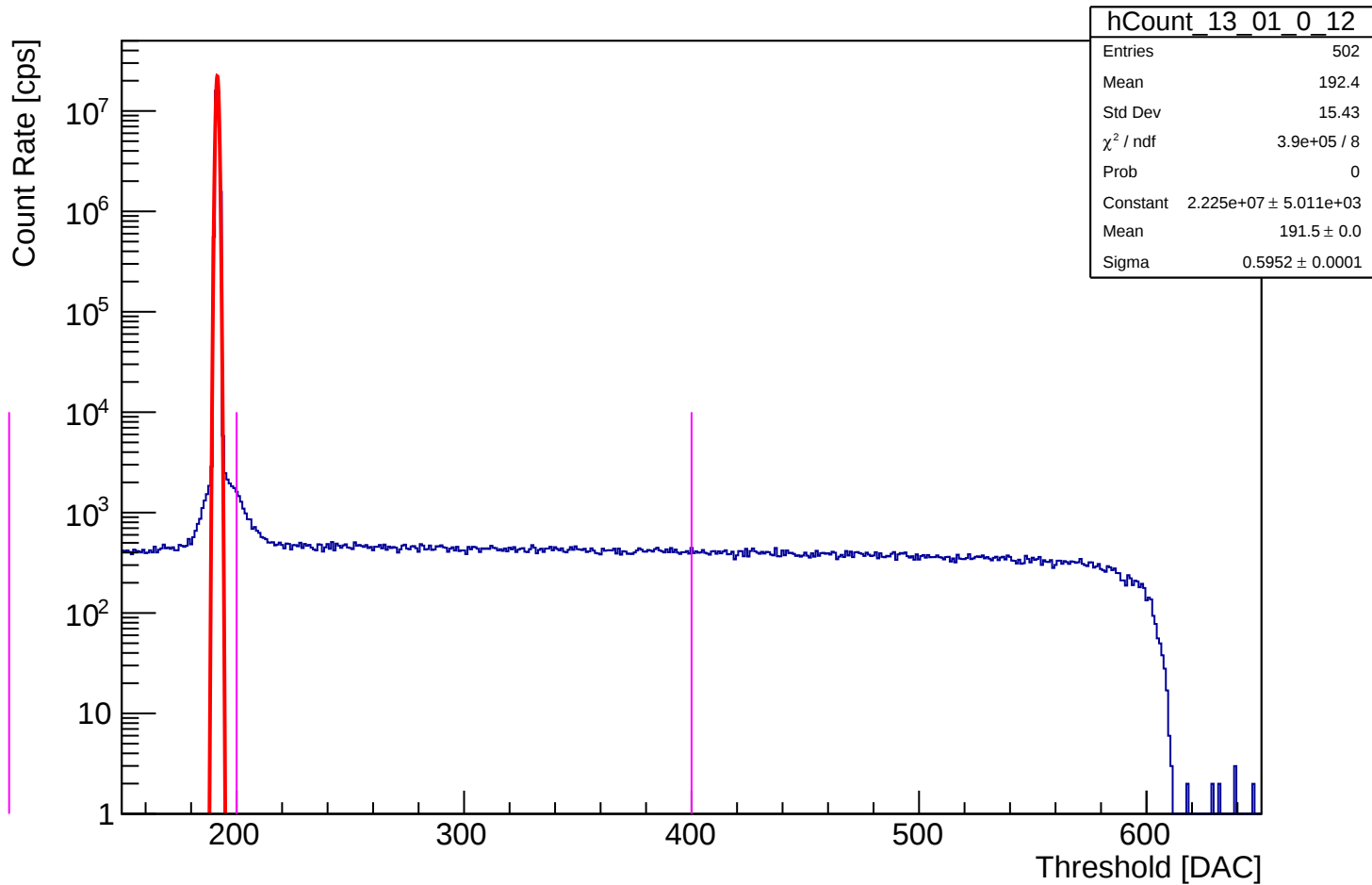
Row 1 Tile 1 Pmt 4 Pixel 34 Slot 13 Fiber 1 Asic 0 Channel 13



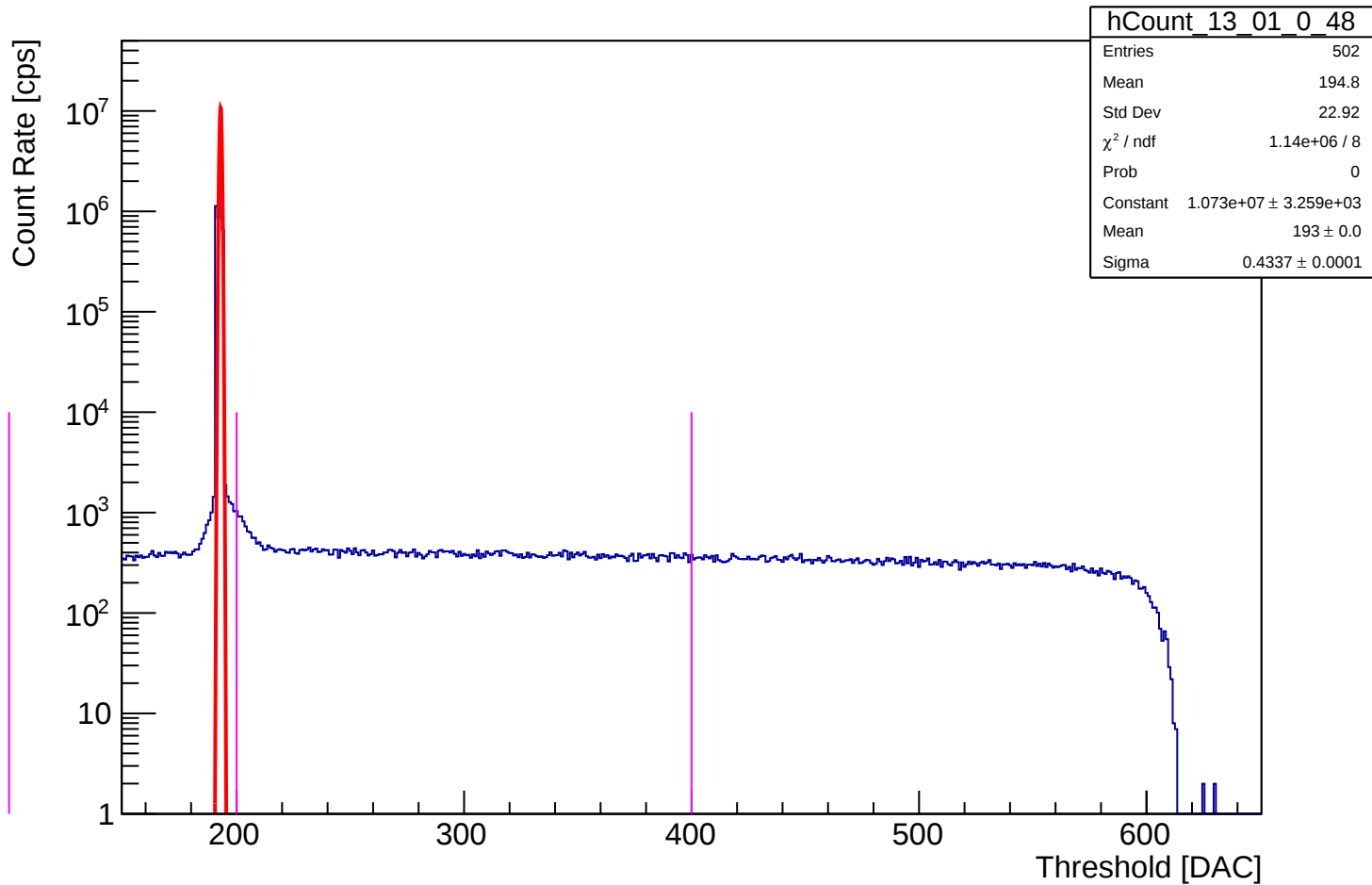
Row 1 Tile 1 Pmt 4 Pixel 35 Slot 13 Fiber 1 Asic 0 Channel 14



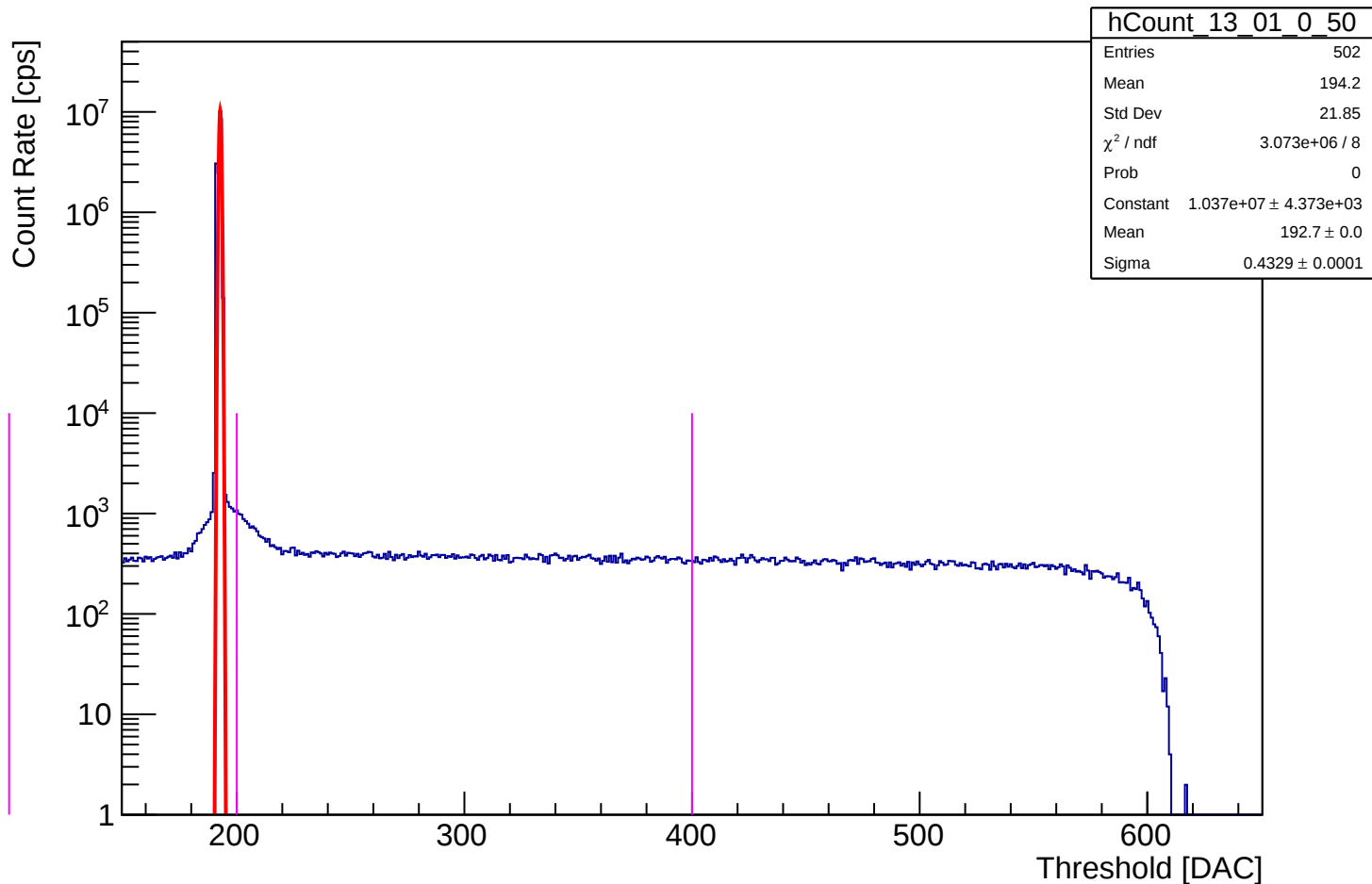
Row 1 Tile 1 Pmt 4 Pixel 36 Slot 13 Fiber 1 Asic 0 Channel 12



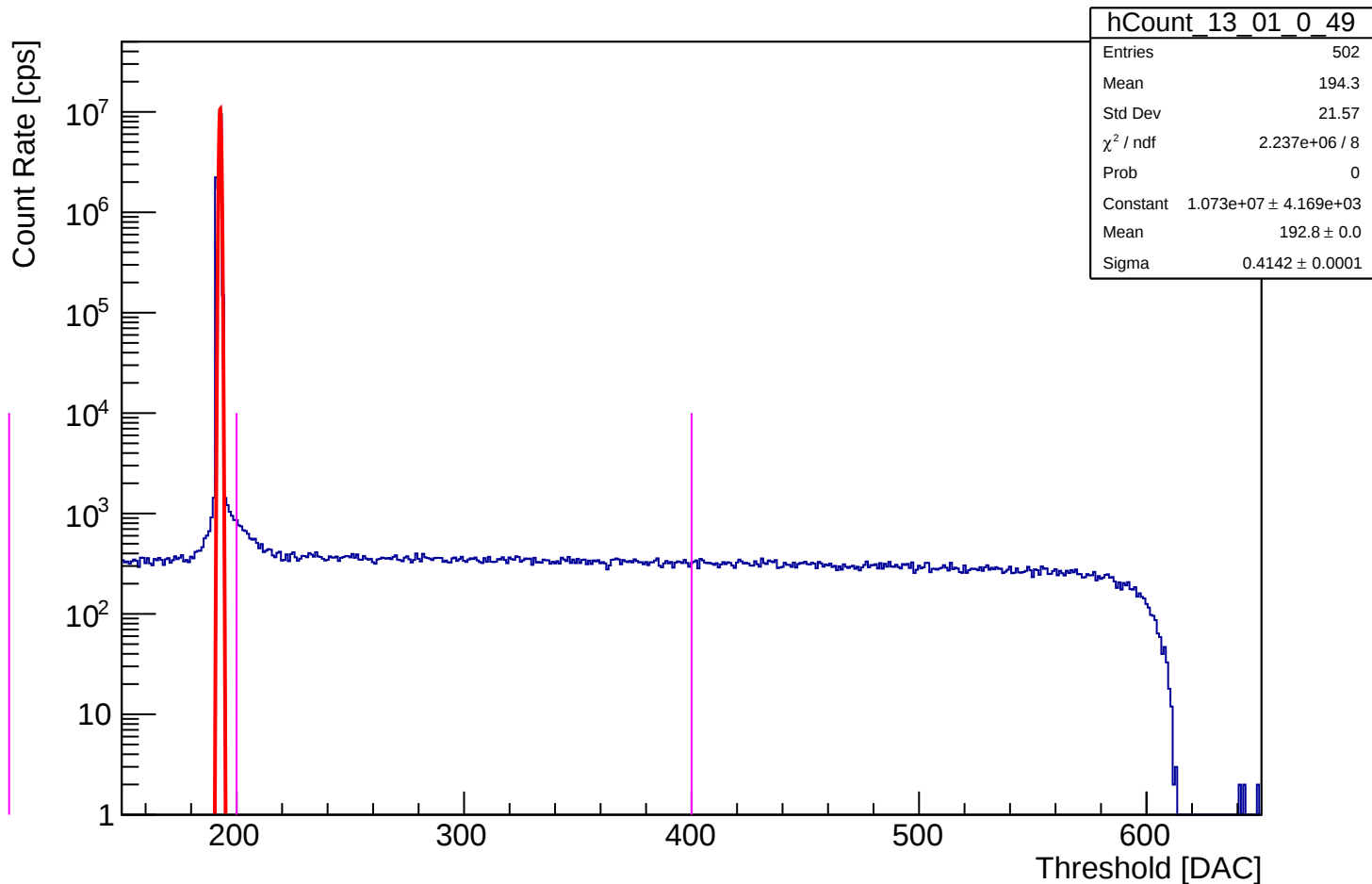
Row 1 Tile 1 Pmt 4 Pixel 37 Slot 13 Fiber 1 Asic 0 Channel 48

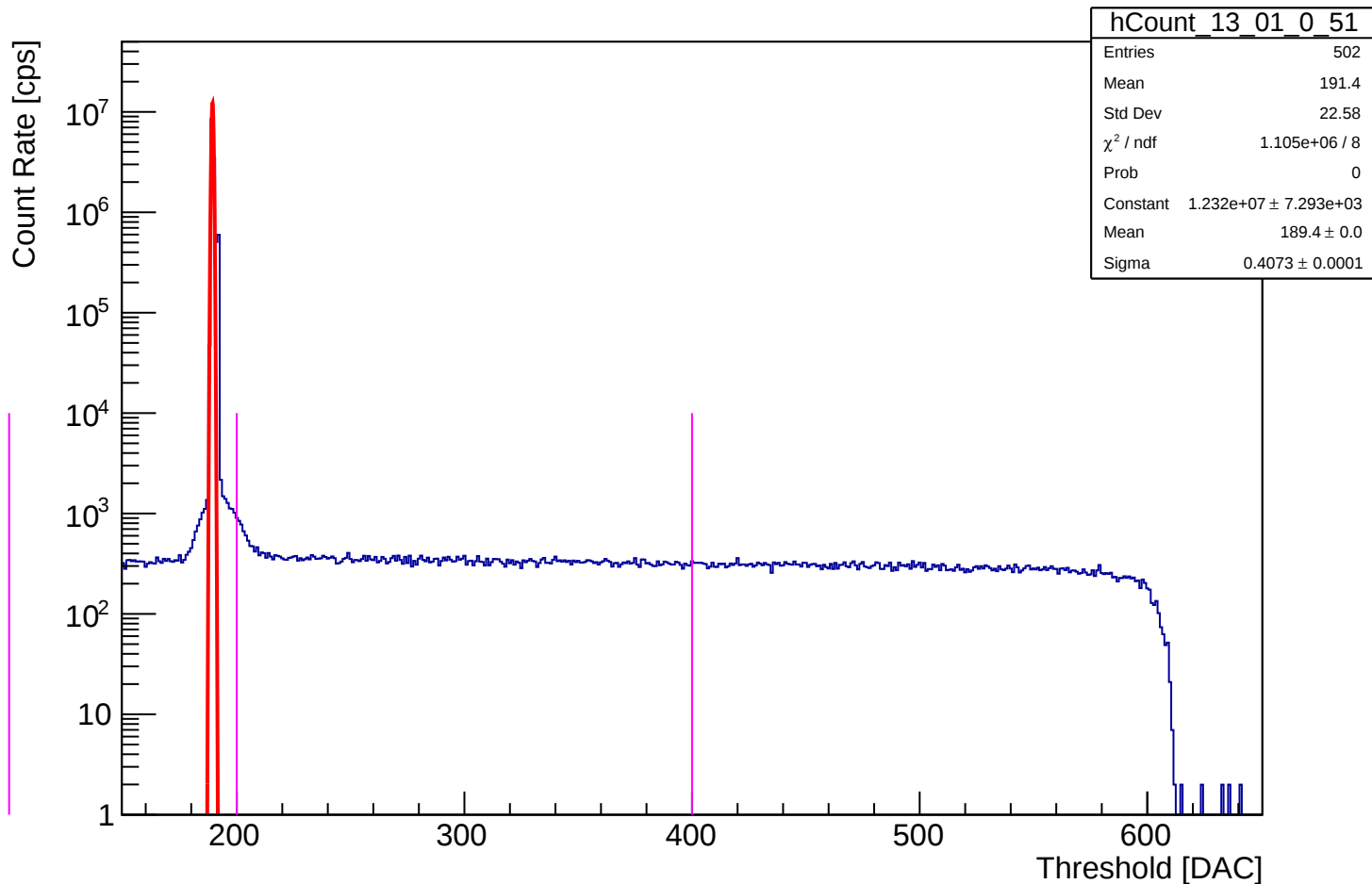


Row 1 Tile 1 Pmt 4 Pixel 38 Slot 13 Fiber 1 Asic 0 Channel 50

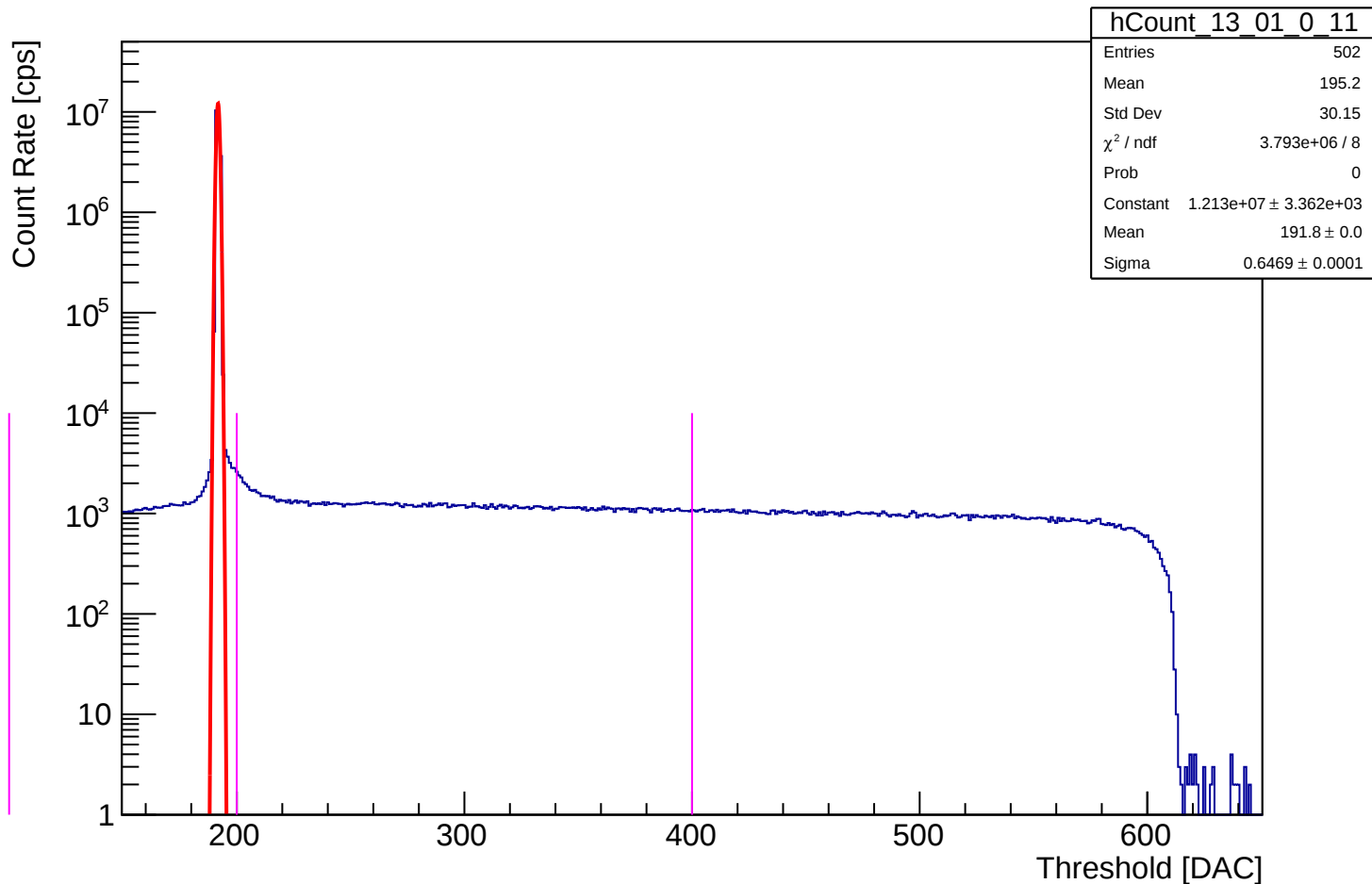


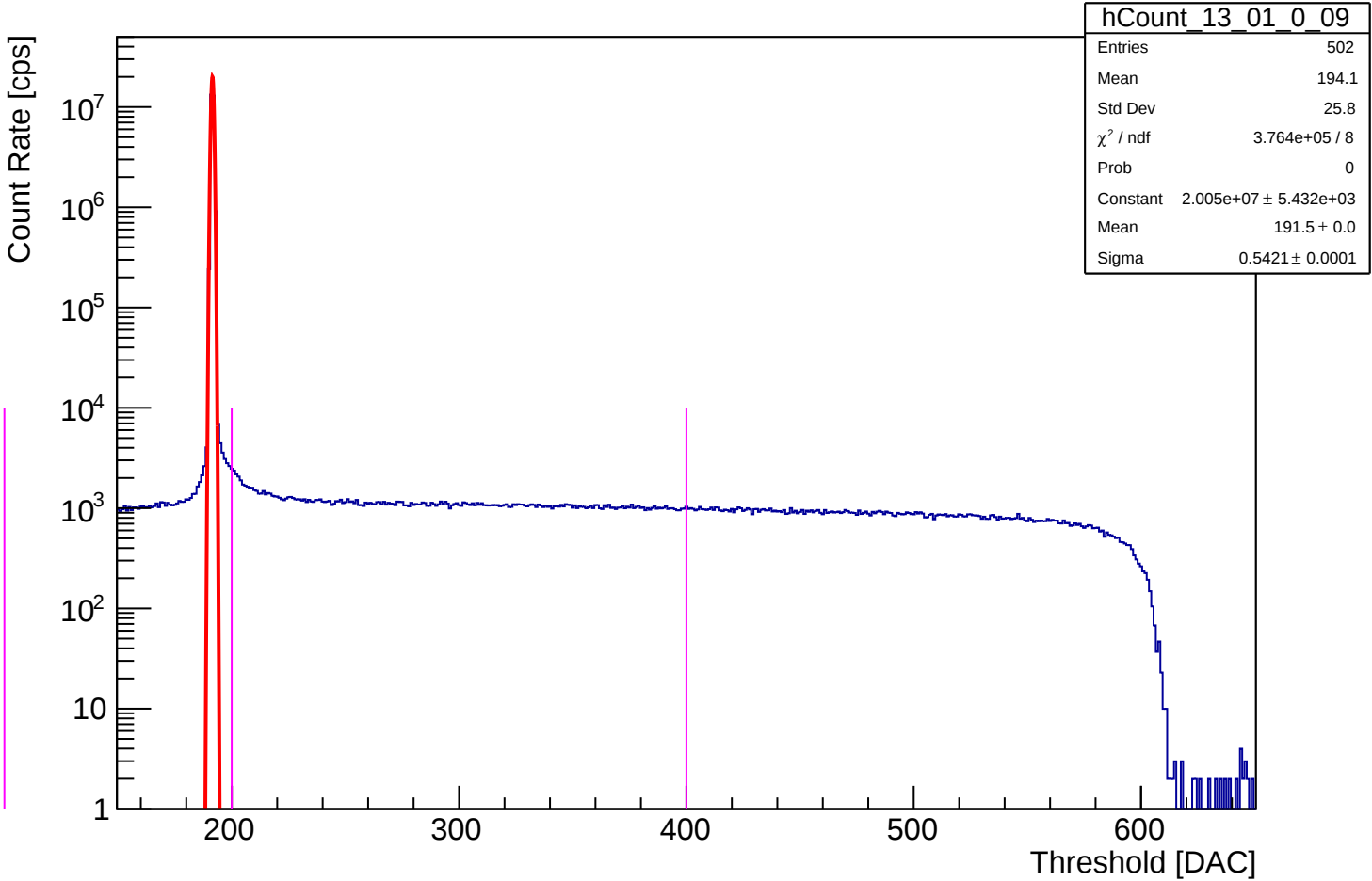
Row 1 Tile 1 Pmt 4 Pixel 39 Slot 13 Fiber 1 Asic 0 Channel 49



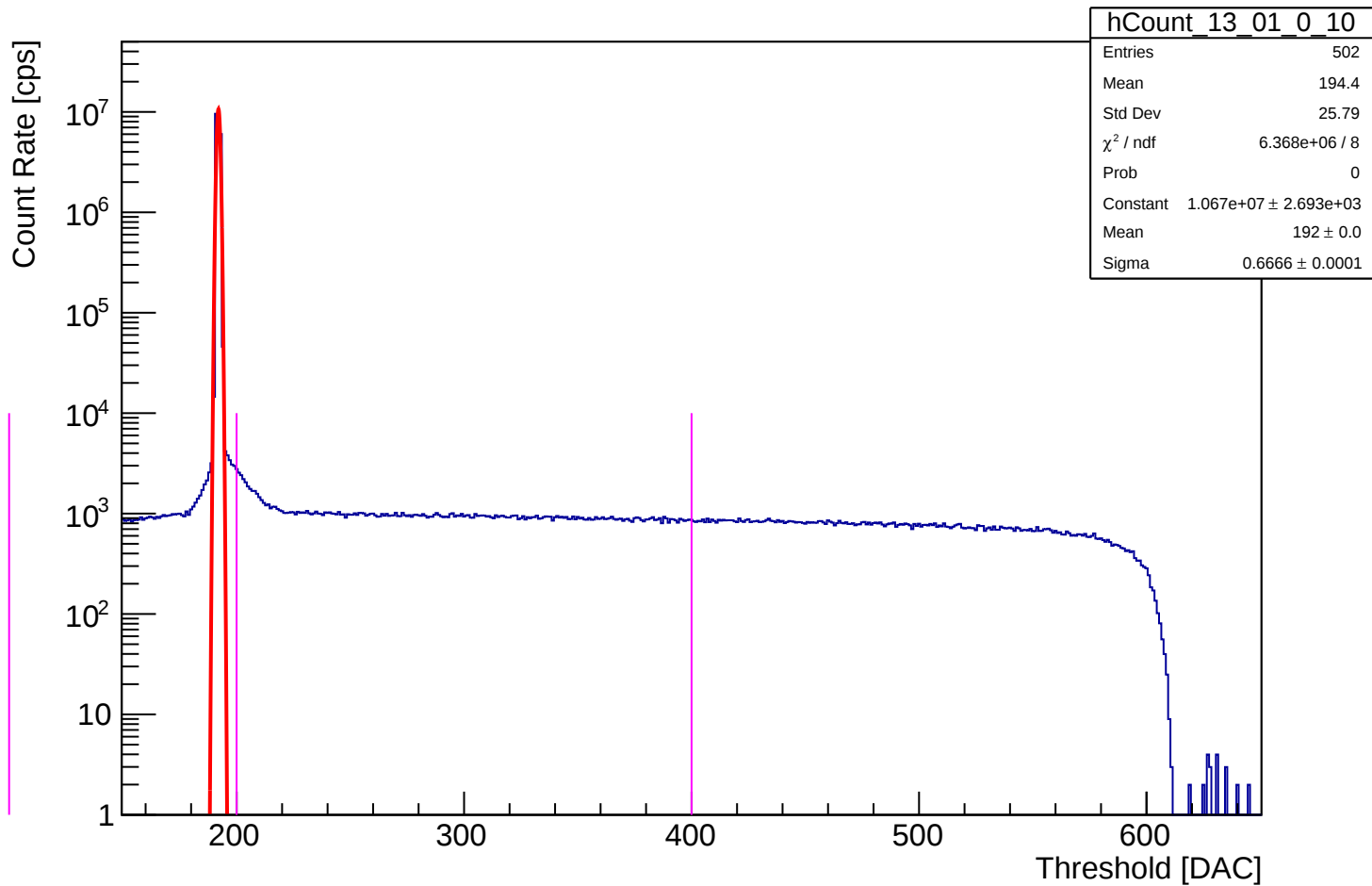


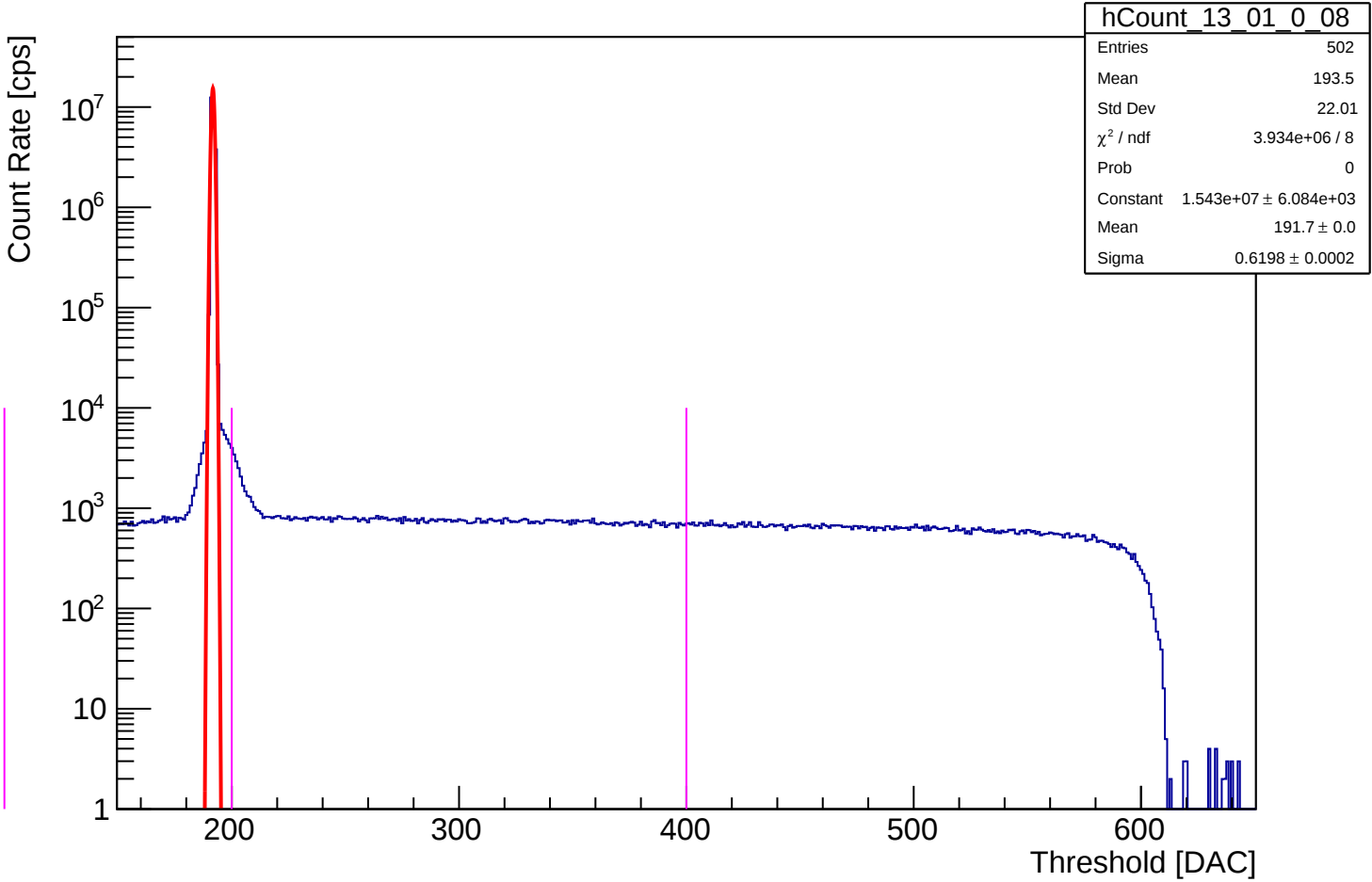
Row 1 Tile 1 Pmt 4 Pixel 41 Slot 13 Fiber 1 Asic 0 Channel 11



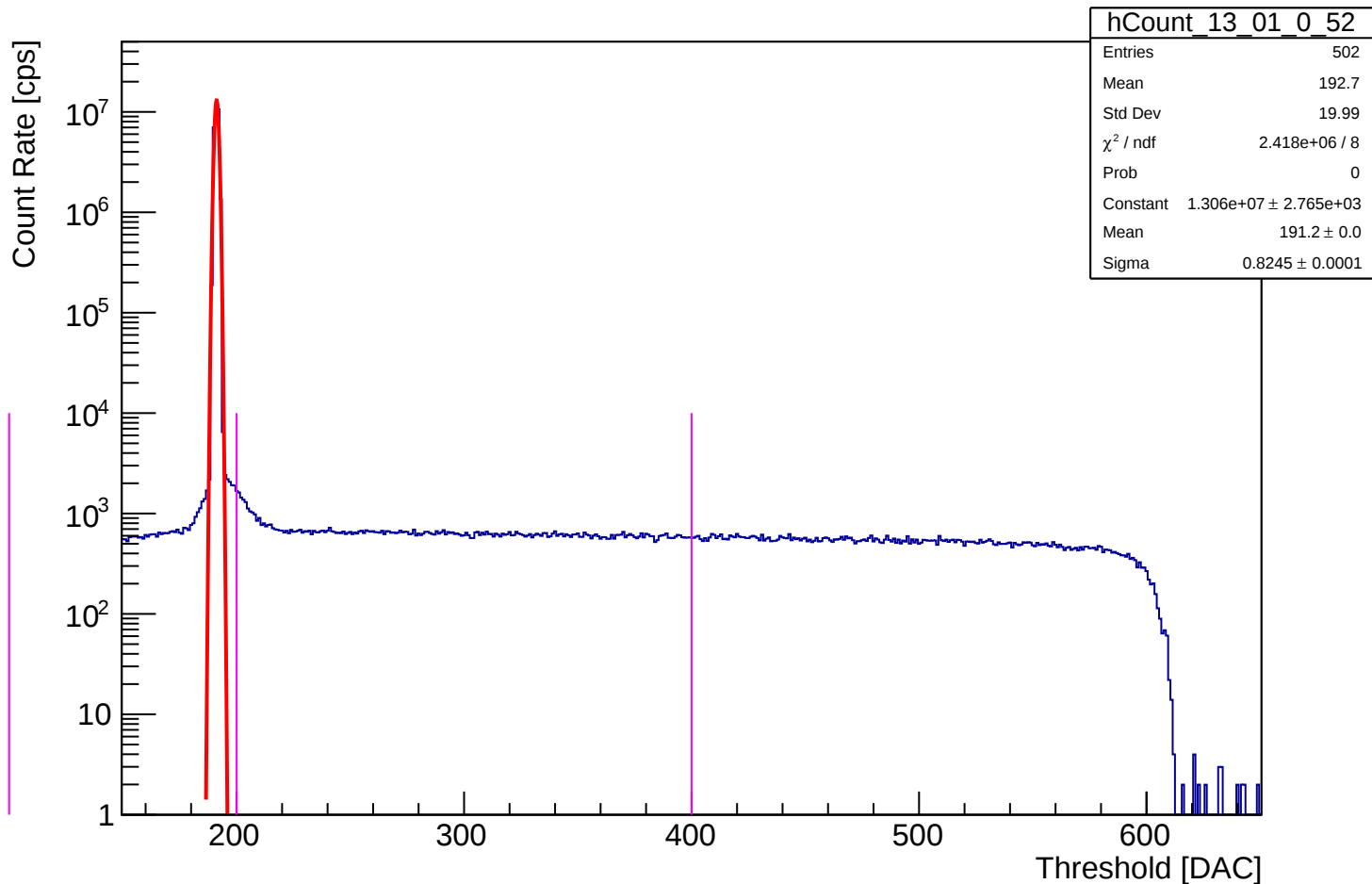


Row 1 Tile 1 Pmt 4 Pixel 43 Slot 13 Fiber 1 Asic 0 Channel 10

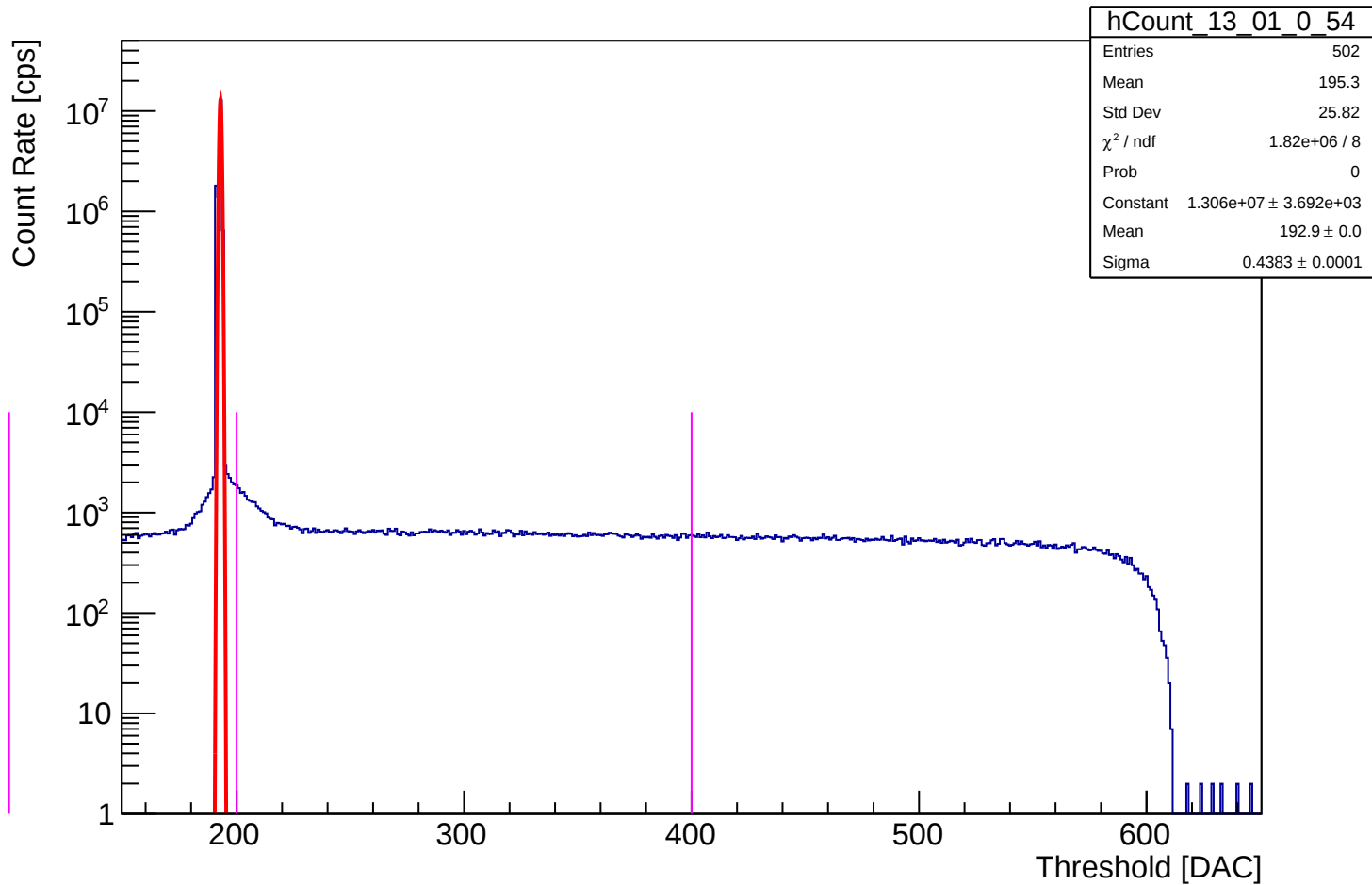




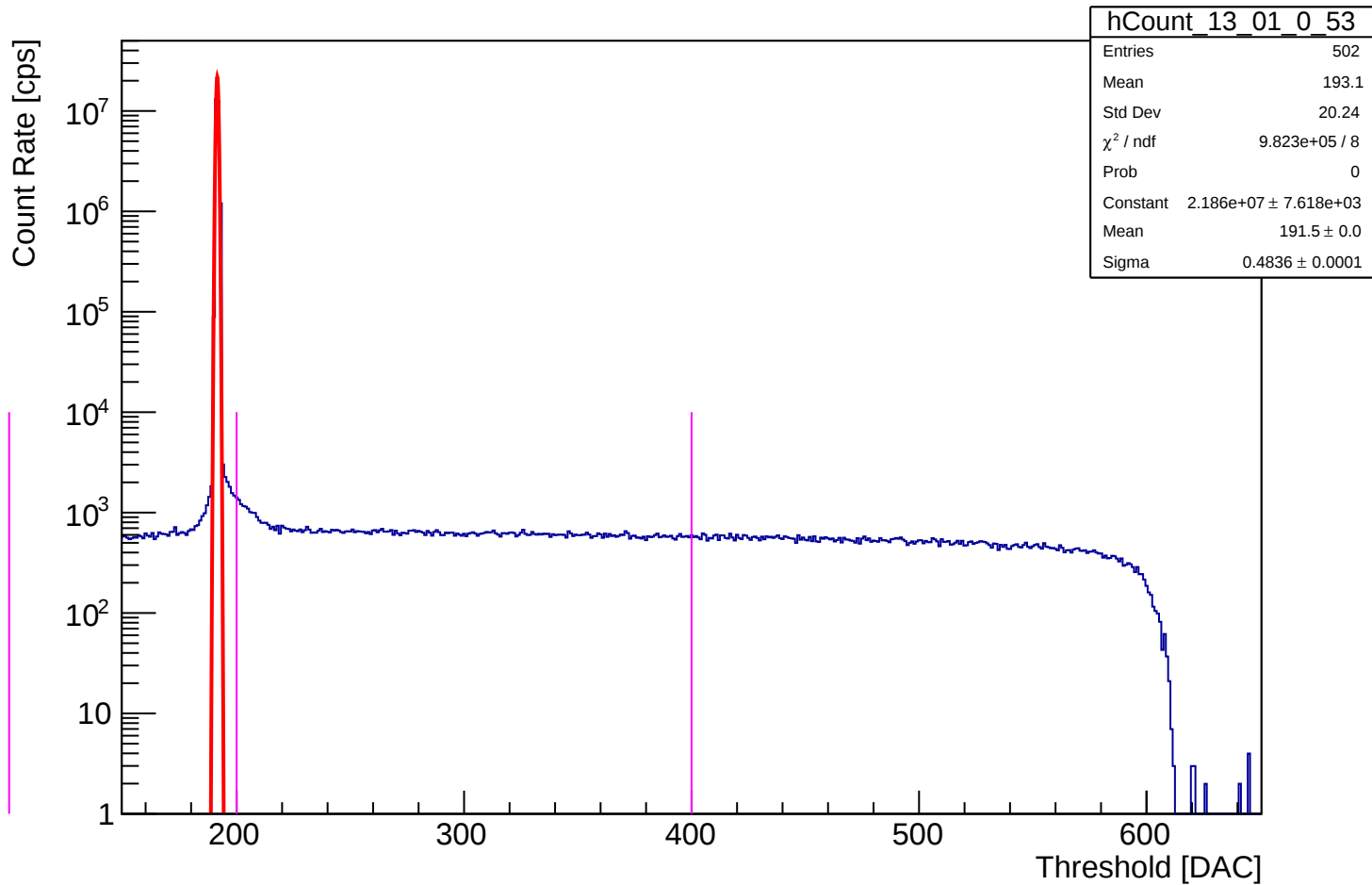
Row 1 Tile 1 Pmt 4 Pixel 45 Slot 13 Fiber 1 Asic 0 Channel 52



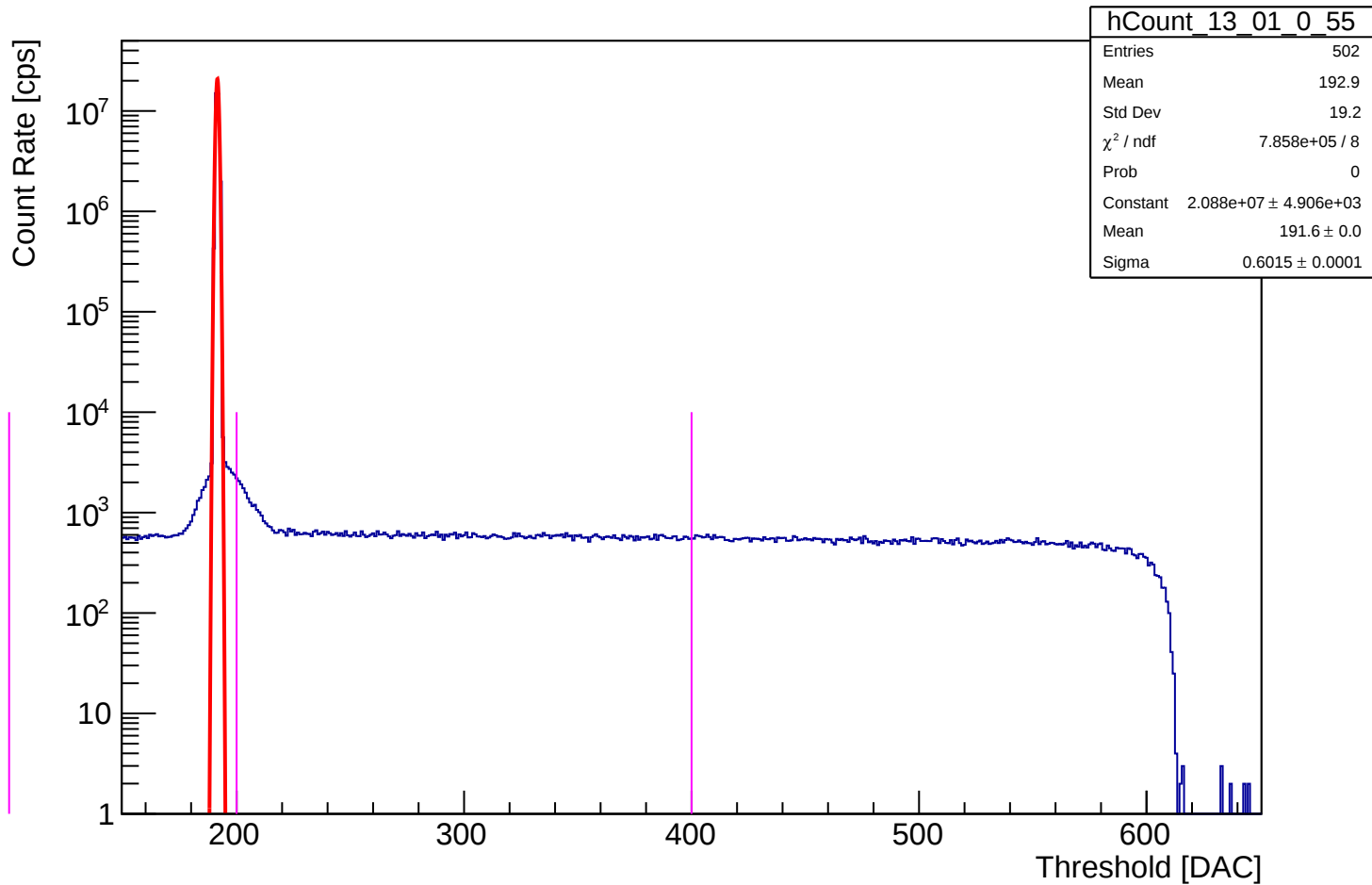
Row 1 Tile 1 Pmt 4 Pixel 46 Slot 13 Fiber 1 Asic 0 Channel 54

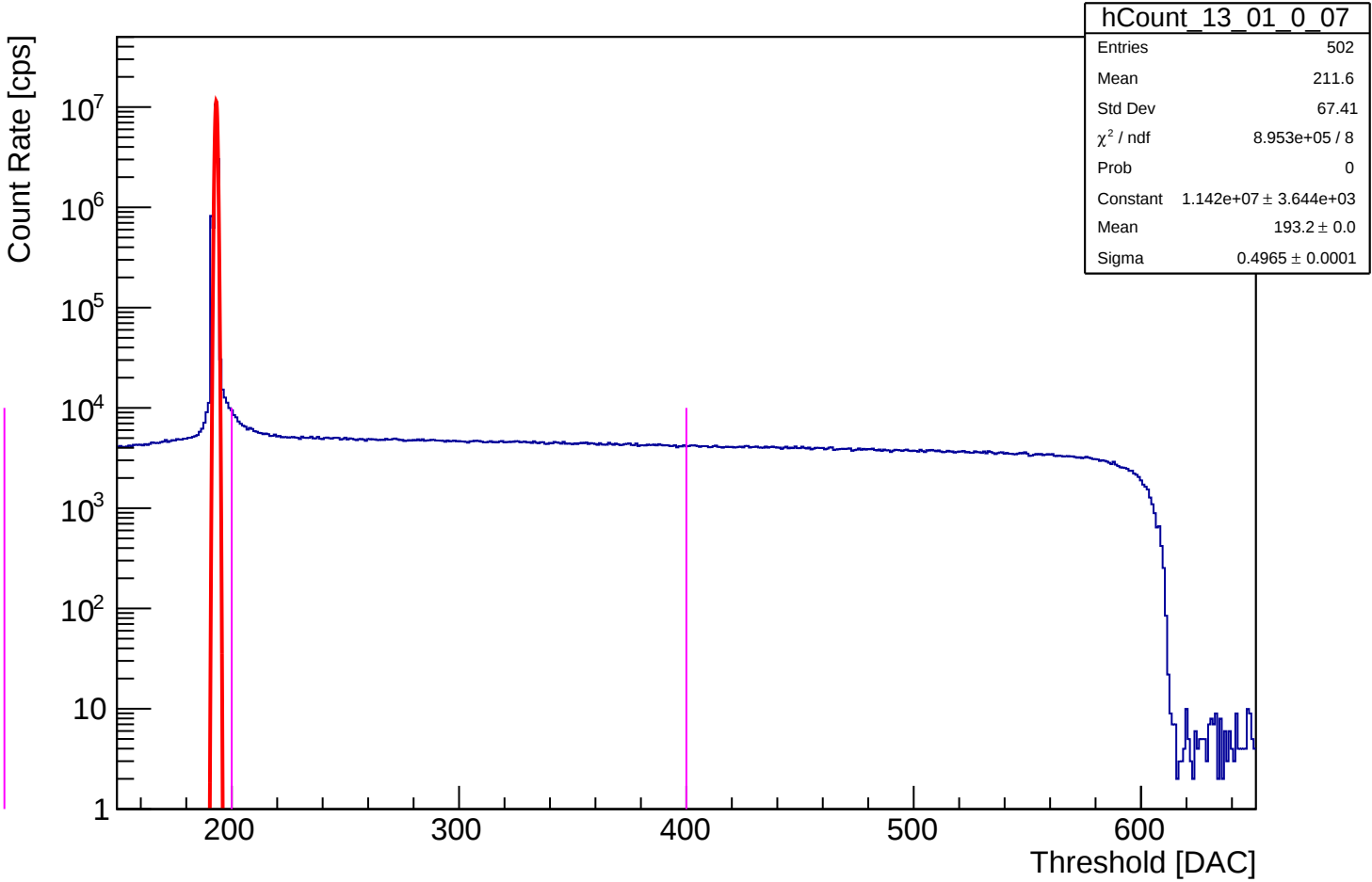


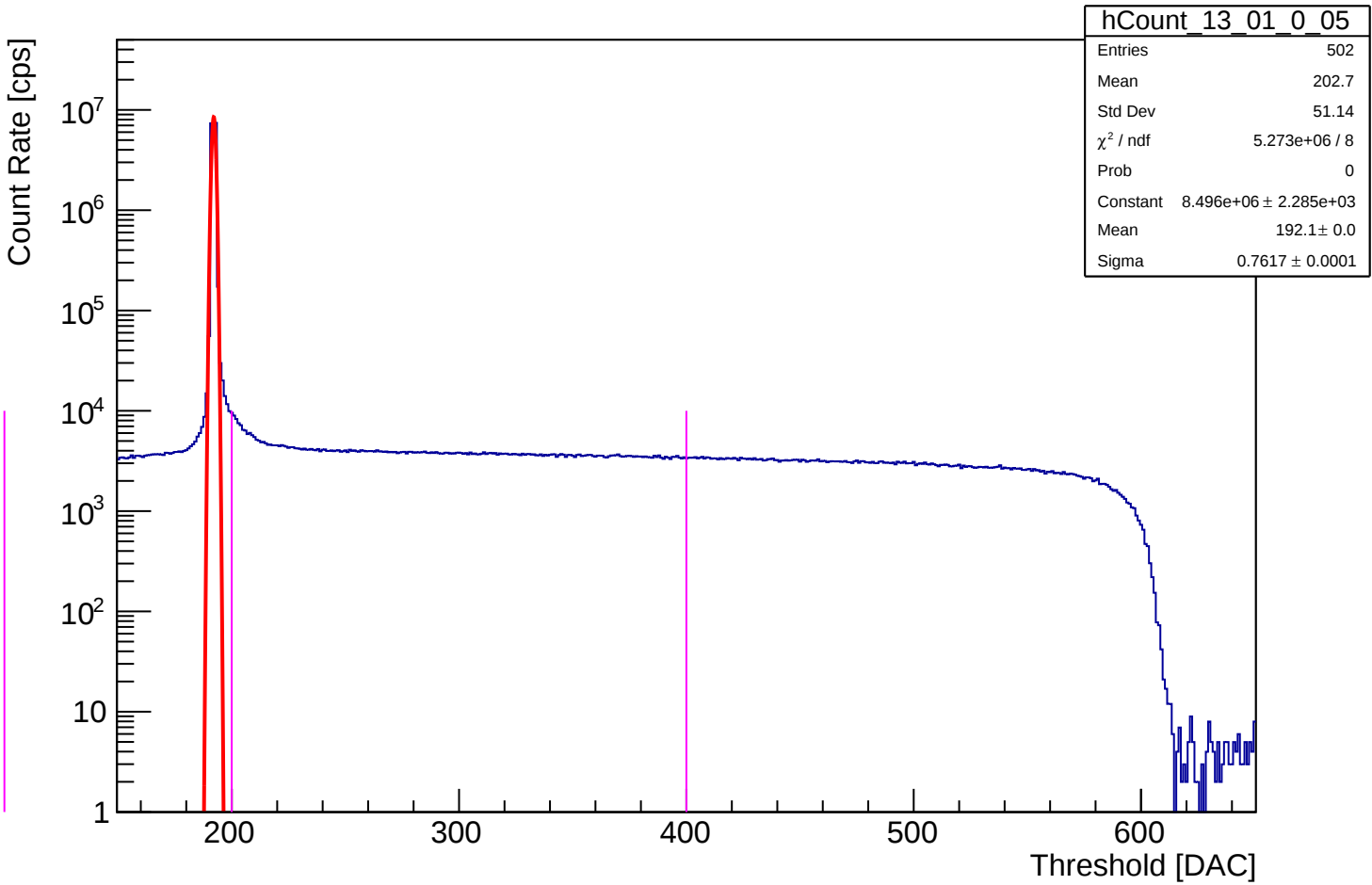
Row 1 Tile 1 Pmt 4 Pixel 47 Slot 13 Fiber 1 Asic 0 Channel 53

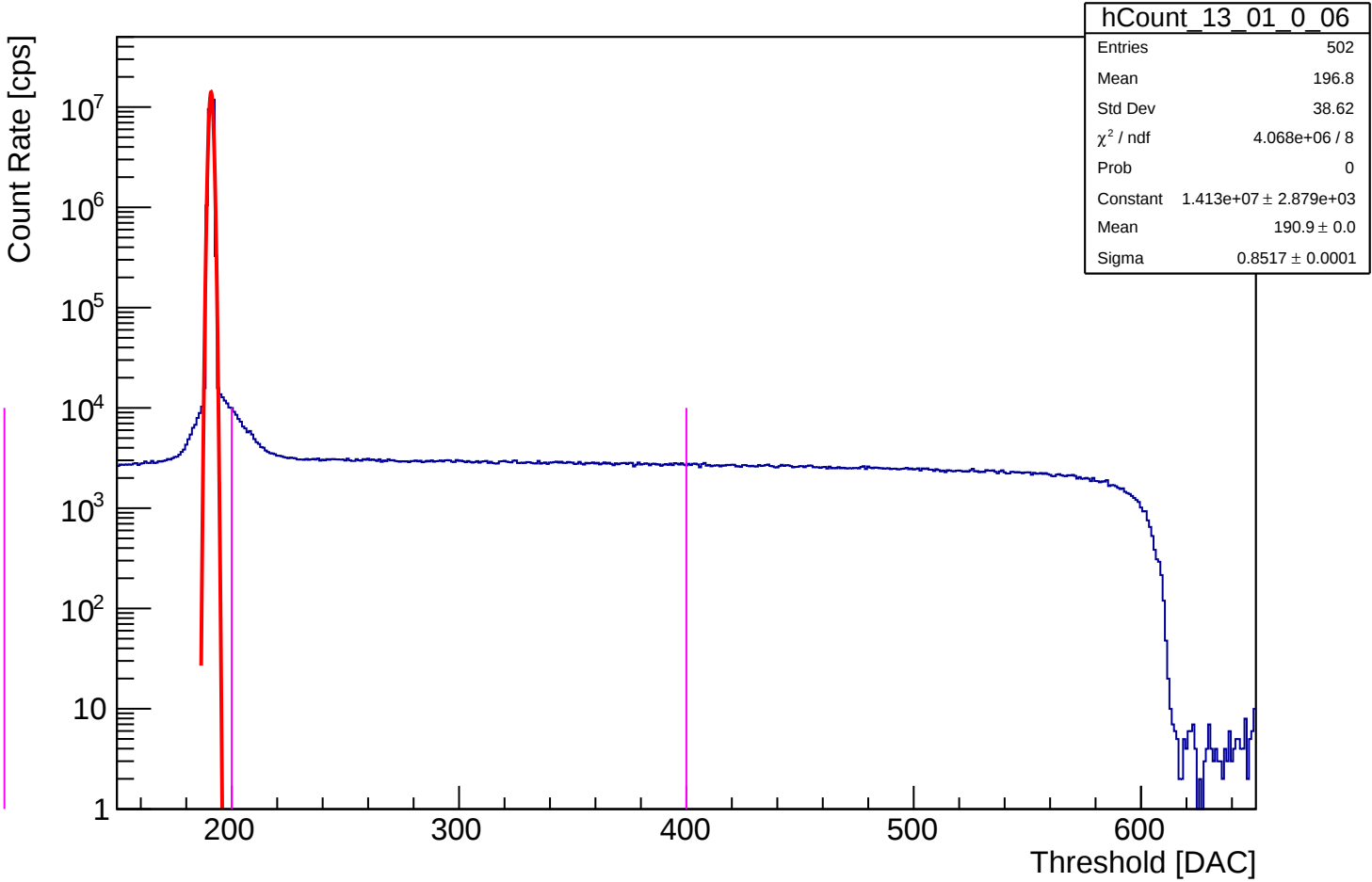


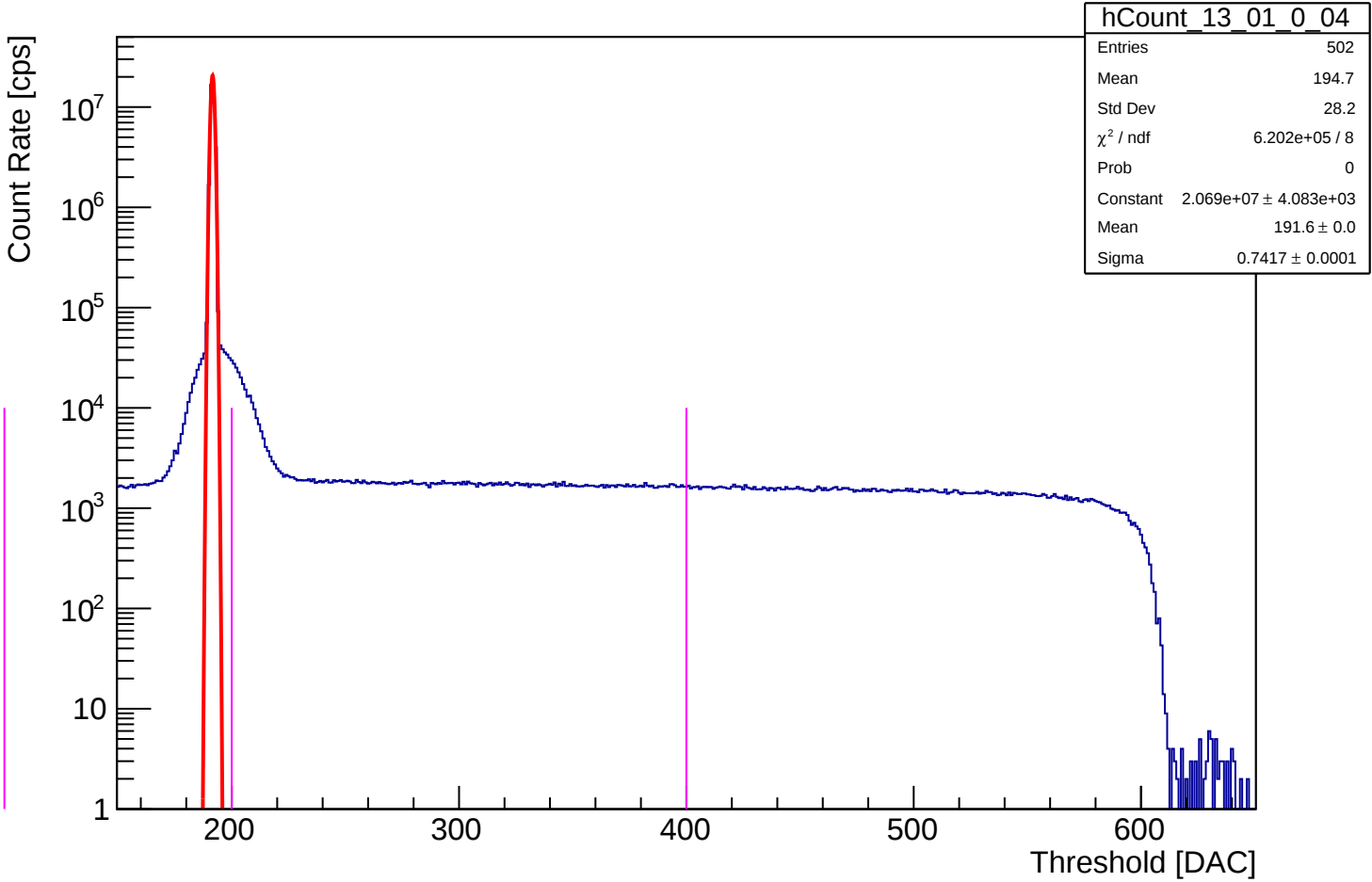
Row 1 Tile 1 Pmt 4 Pixel 48 Slot 13 Fiber 1 Asic 0 Channel 55



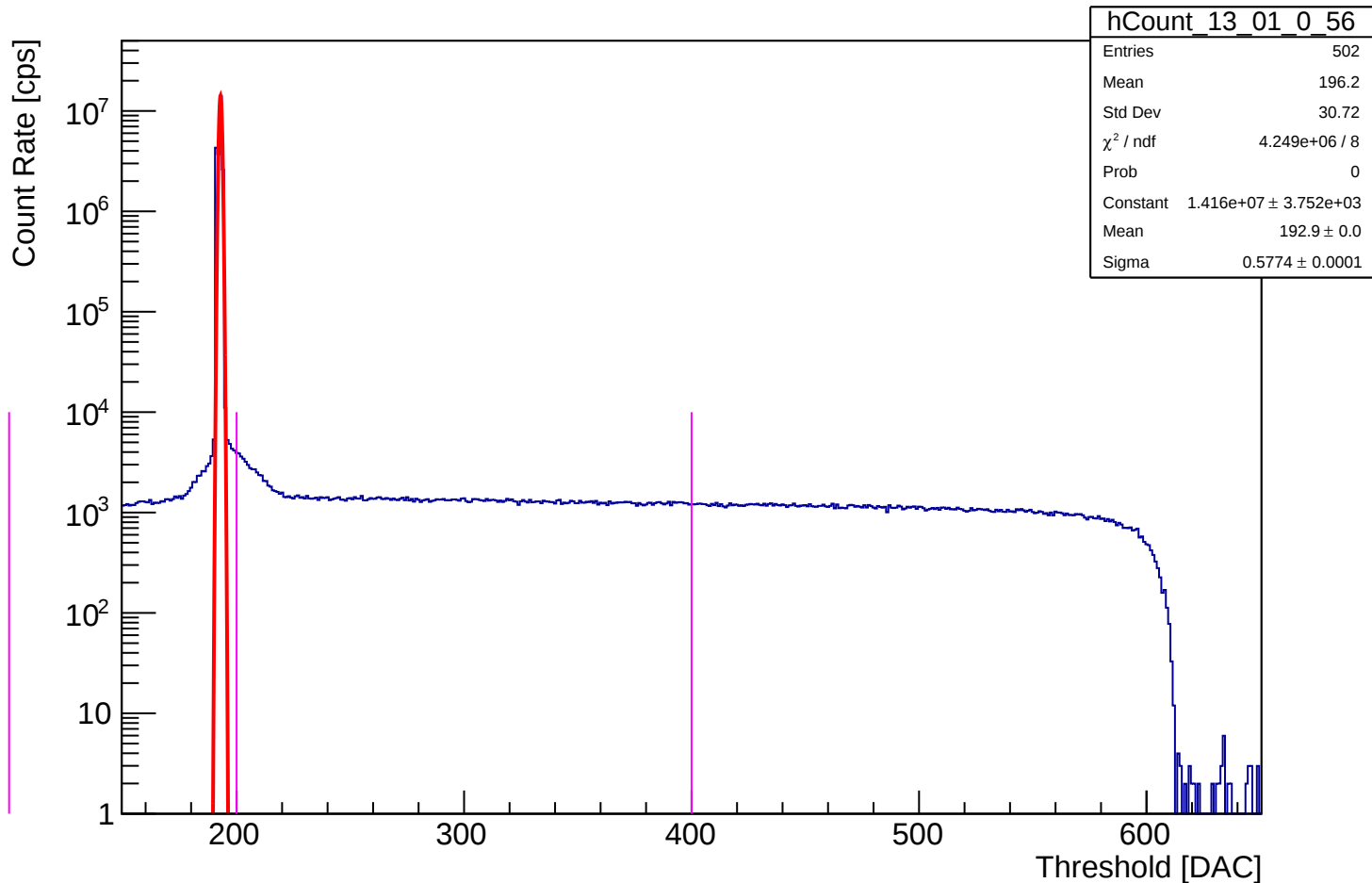




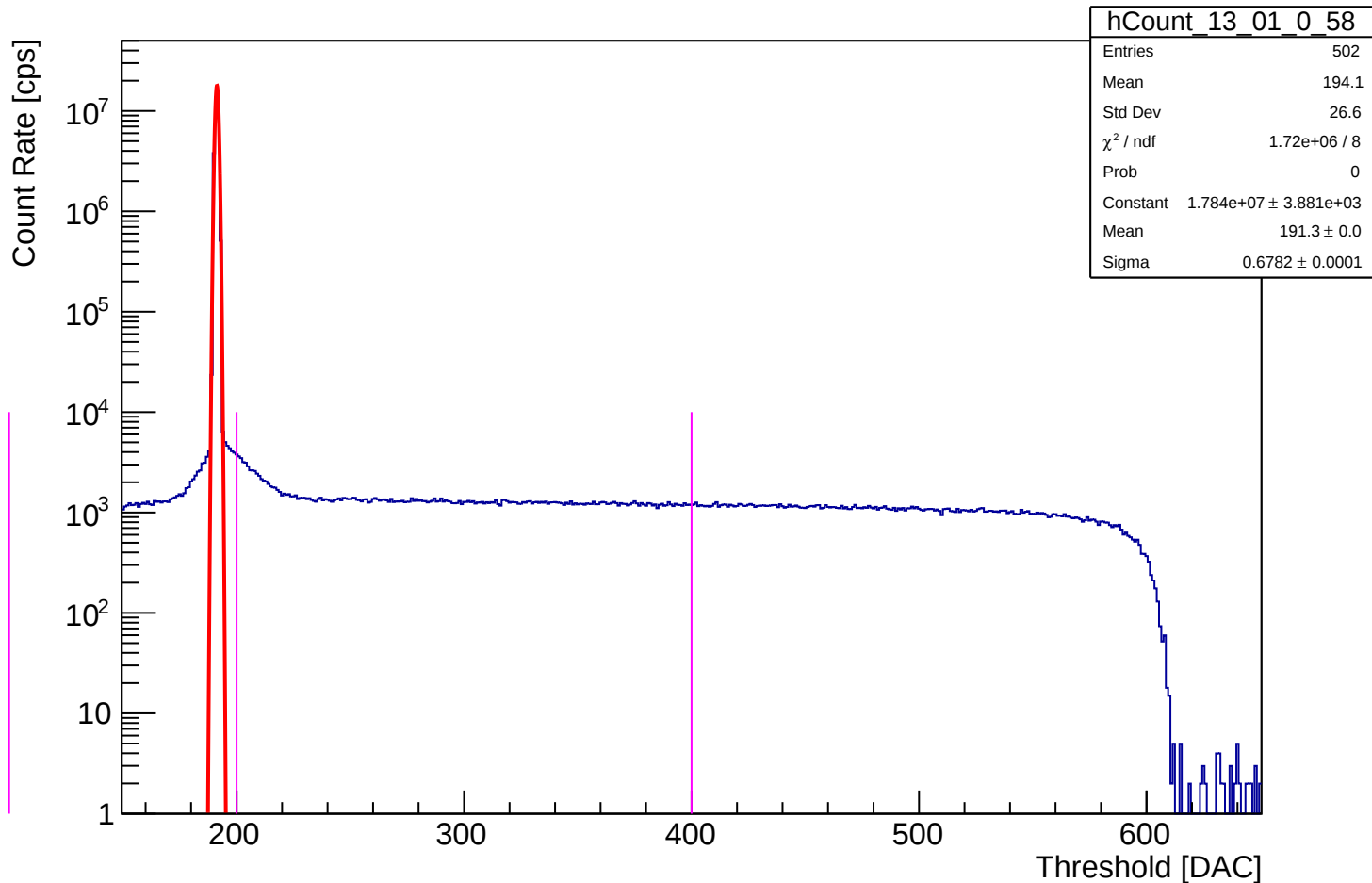




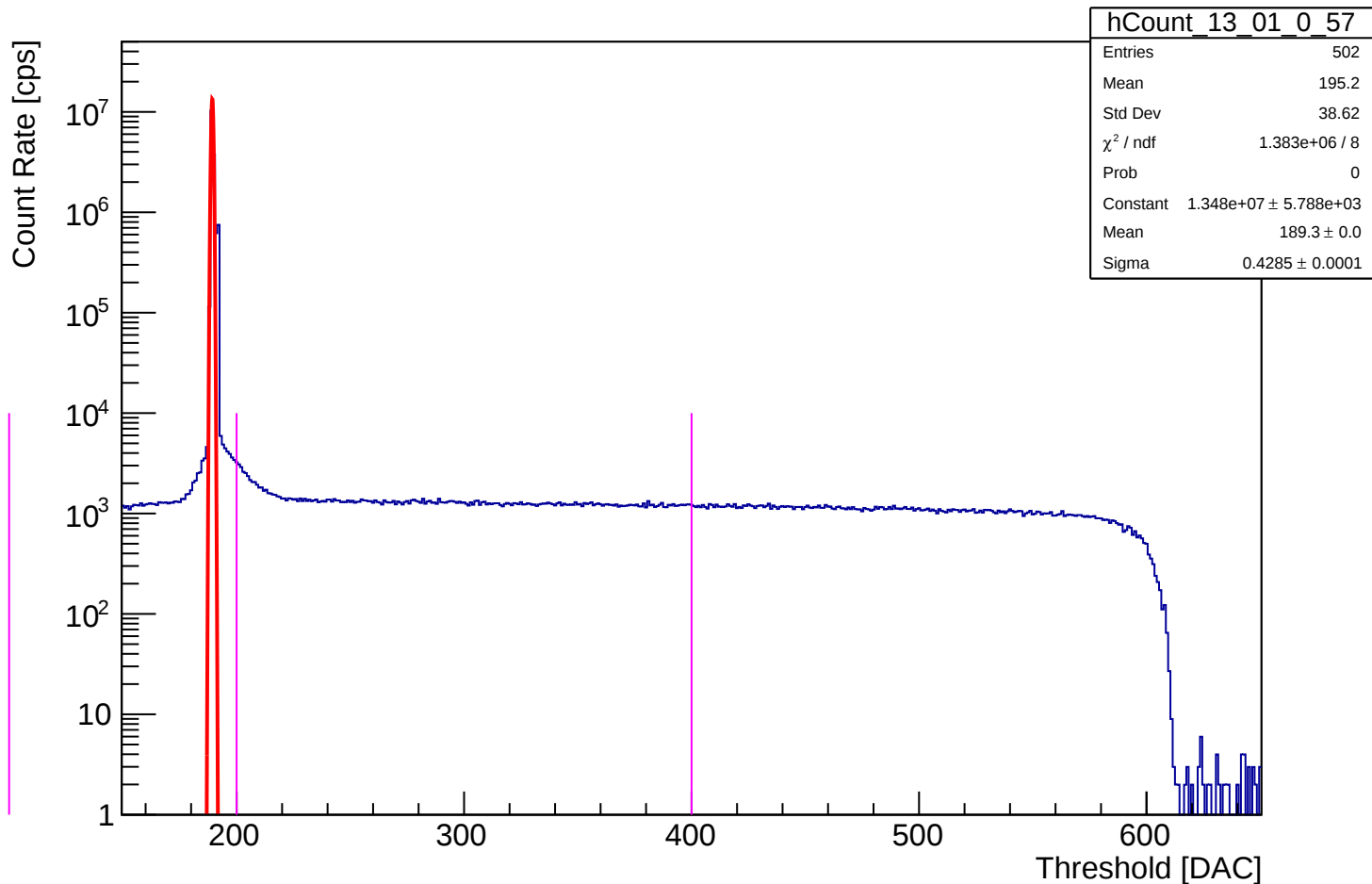
Row 1 Tile 1 Pmt 4 Pixel 53 Slot 13 Fiber 1 Asic 0 Channel 56



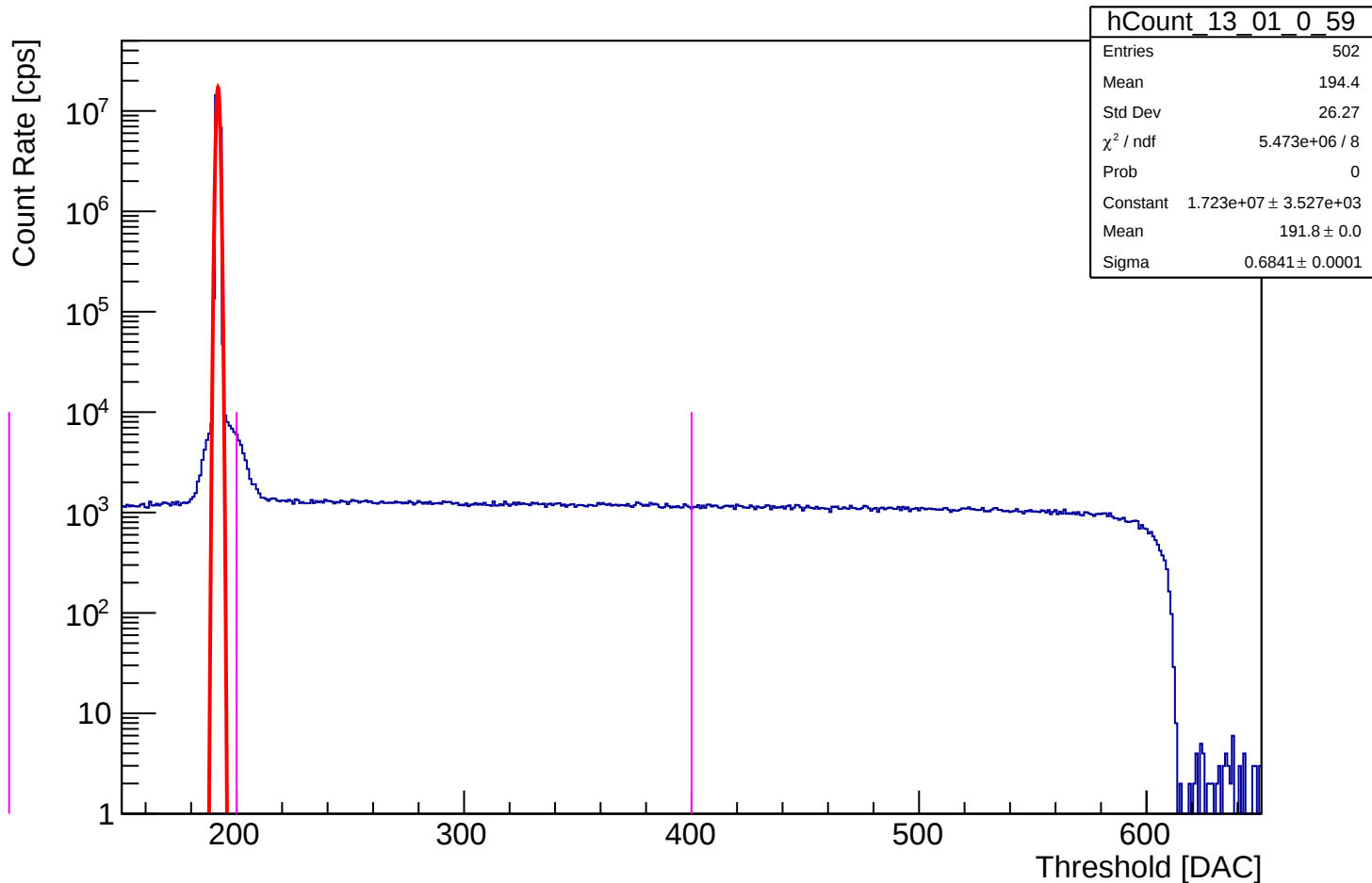
Row 1 Tile 1 Pmt 4 Pixel 54 Slot 13 Fiber 1 Asic 0 Channel 58

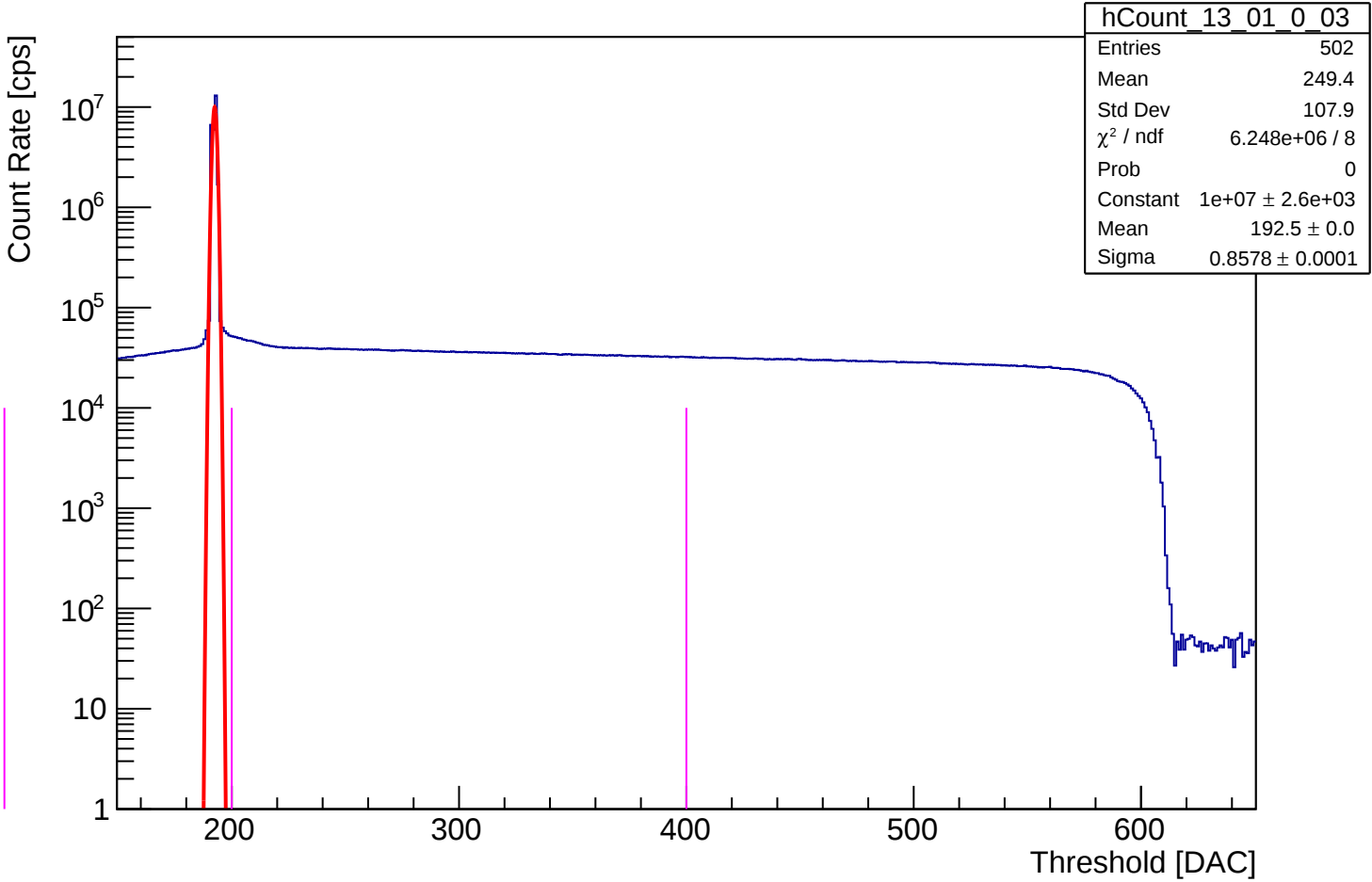


Row 1 Tile 1 Pmt 4 Pixel 55 Slot 13 Fiber 1 Asic 0 Channel 57

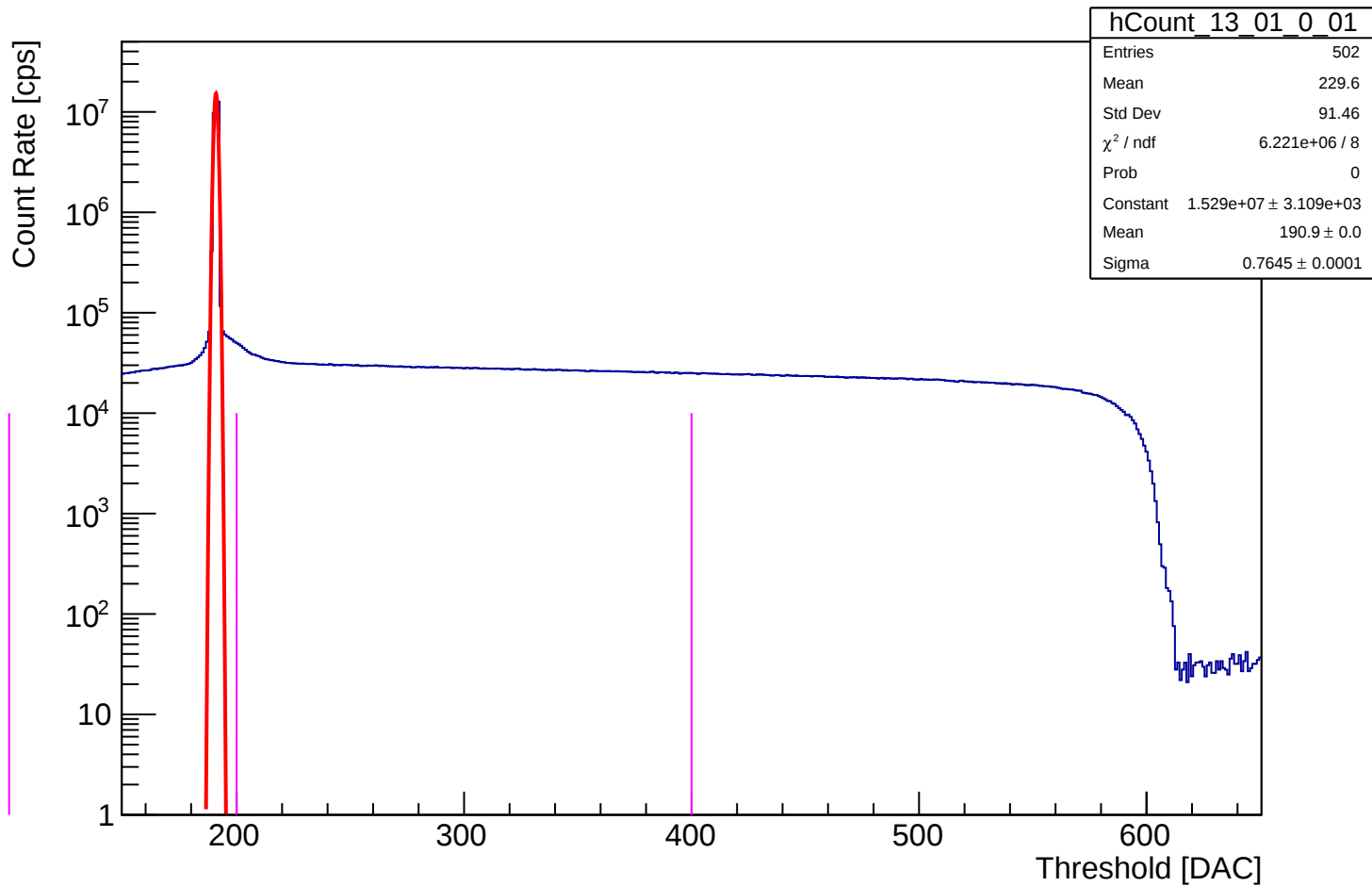


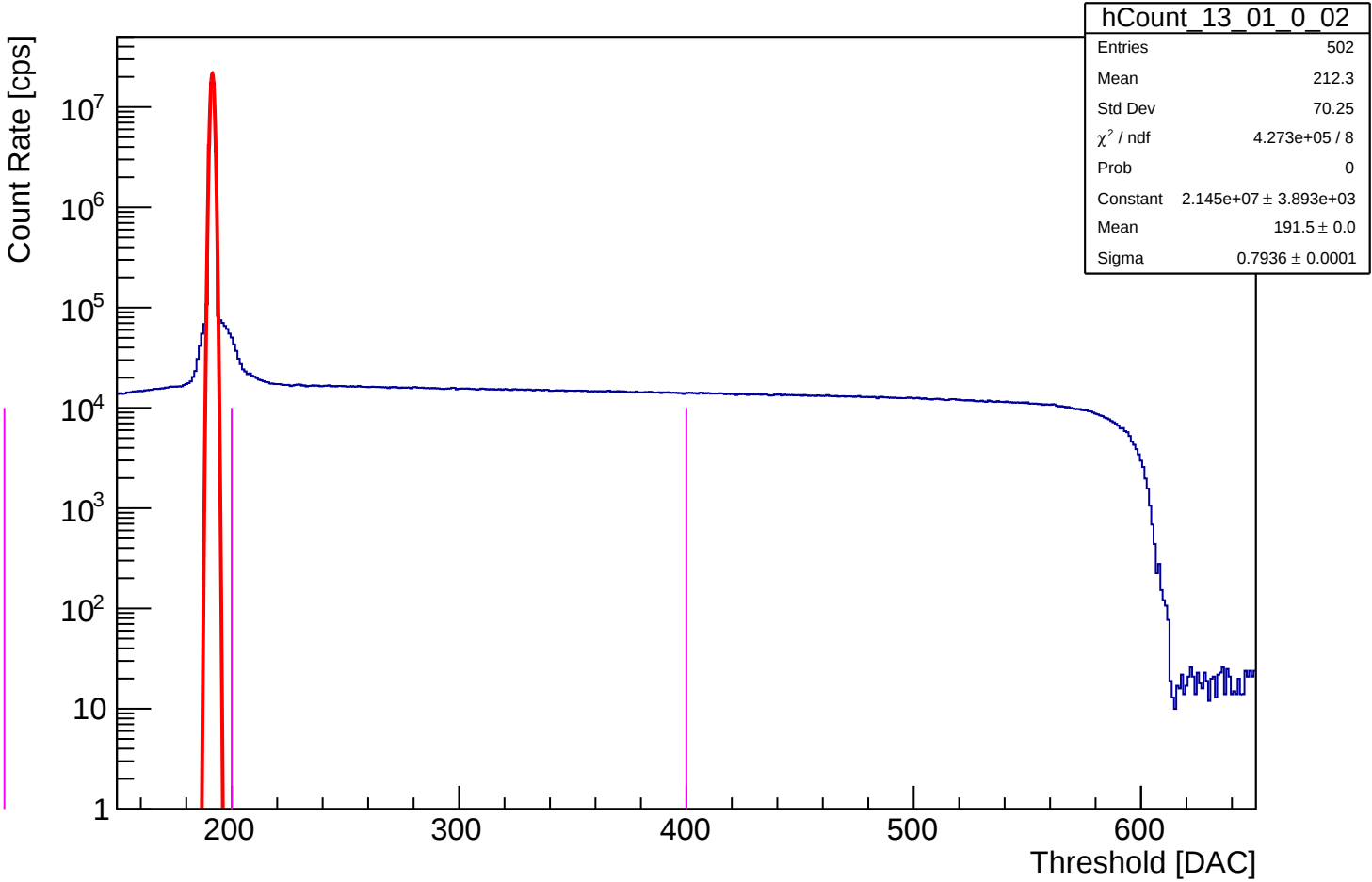
Row 1 Tile 1 Pmt 4 Pixel 56 Slot 13 Fiber 1 Asic 0 Channel 59

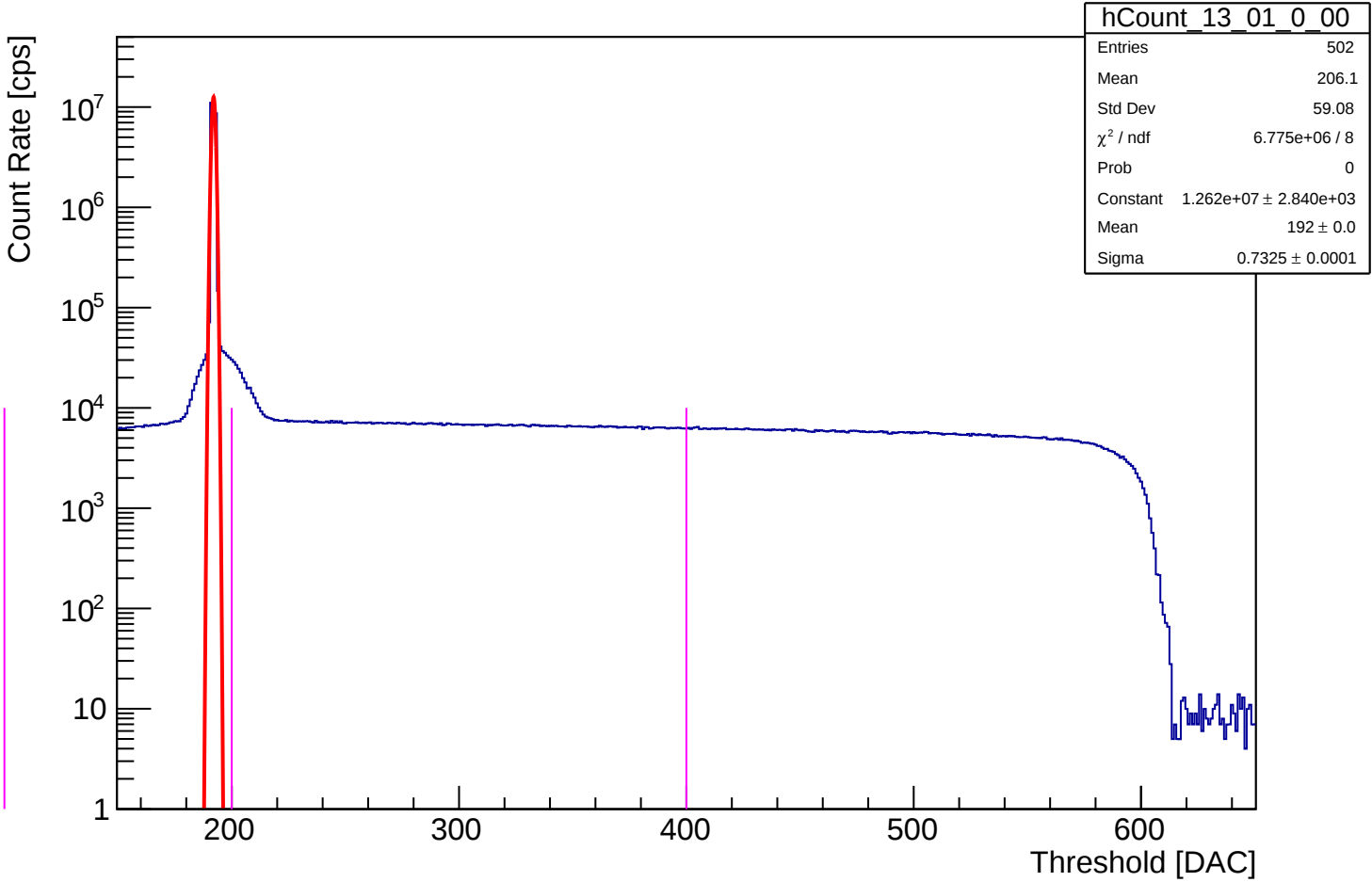




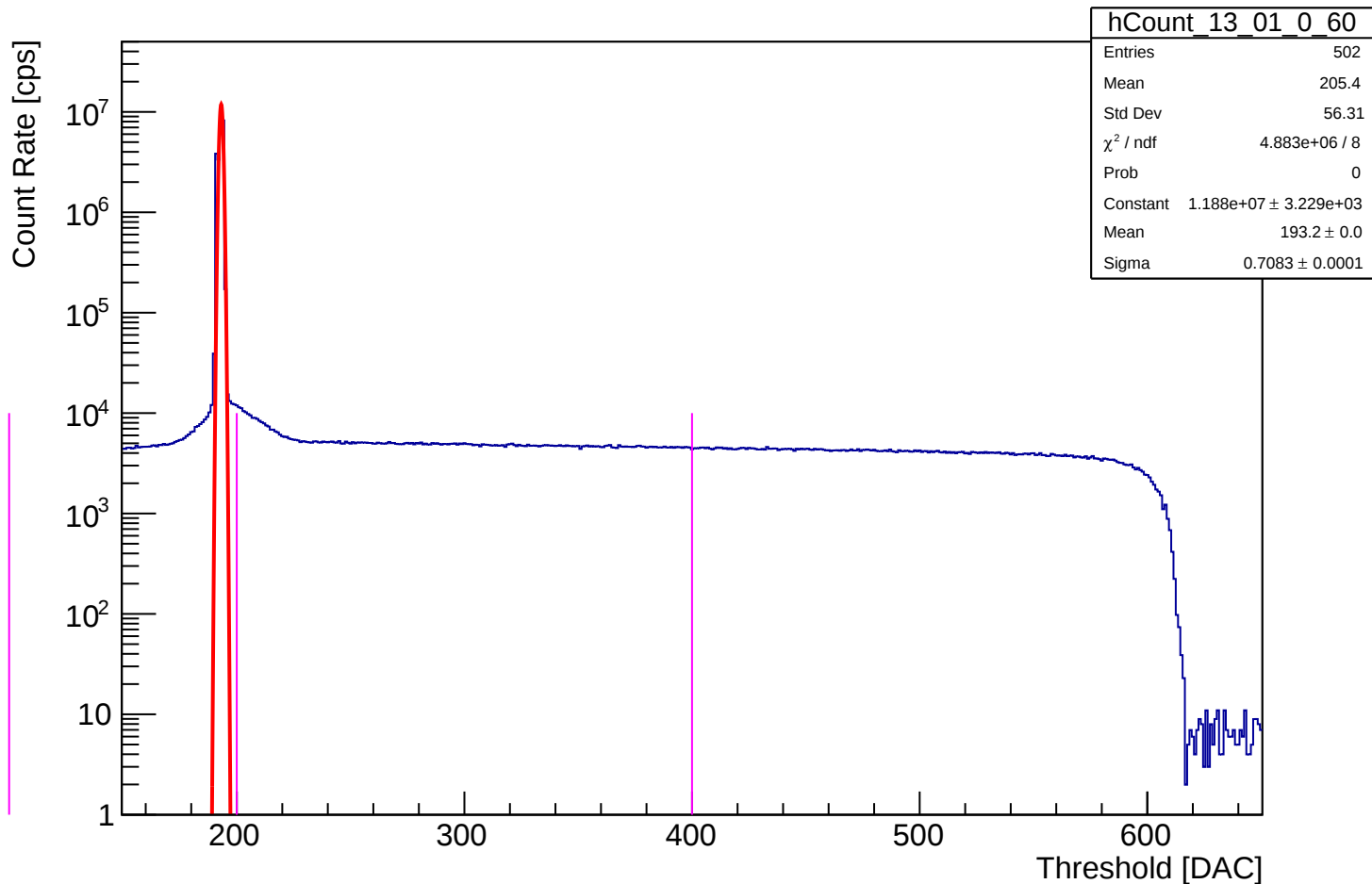
Row 1 Tile 1 Pmt 4 Pixel 58 Slot 13 Fiber 1 Asic 0 Channel 1



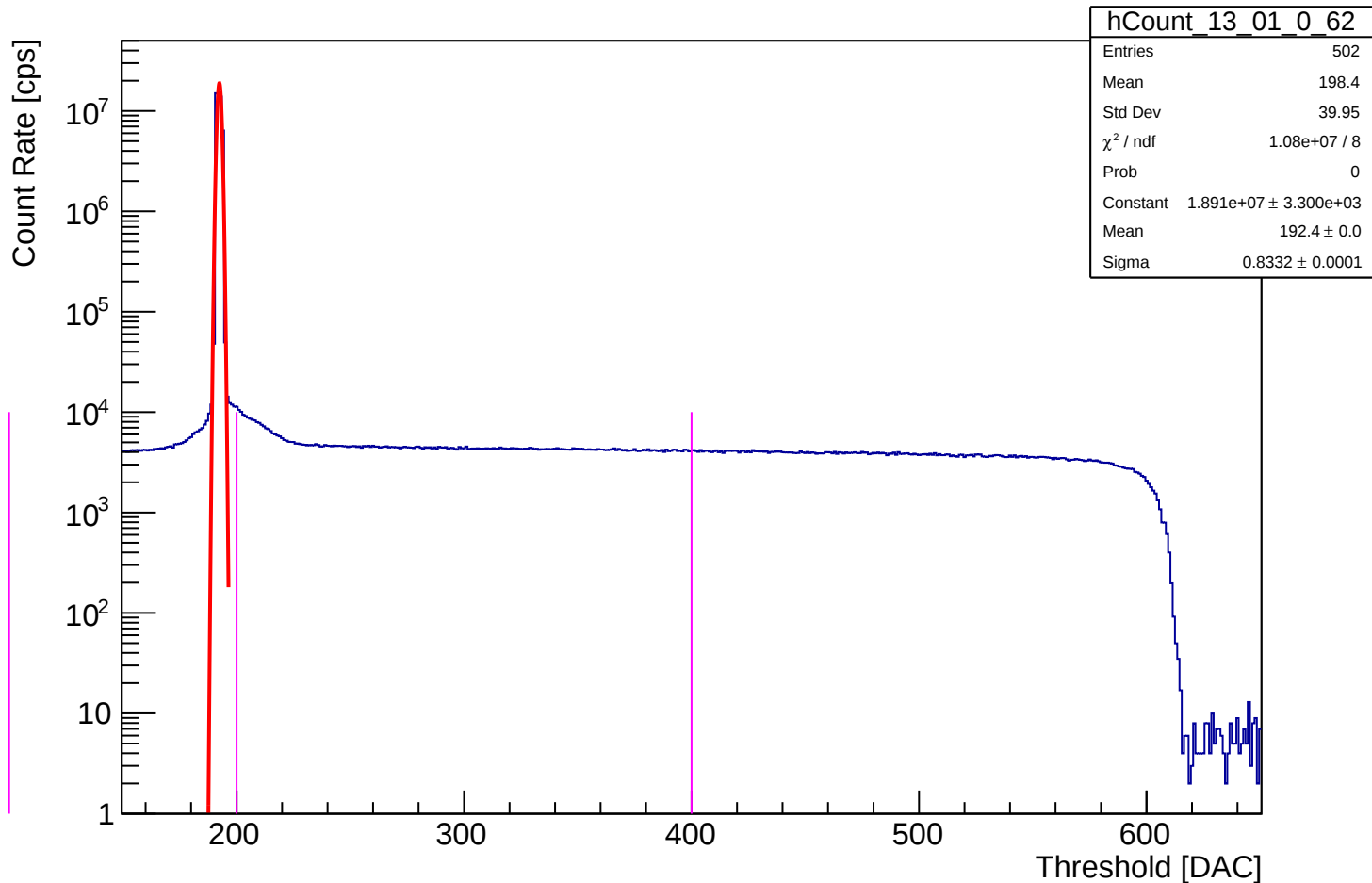




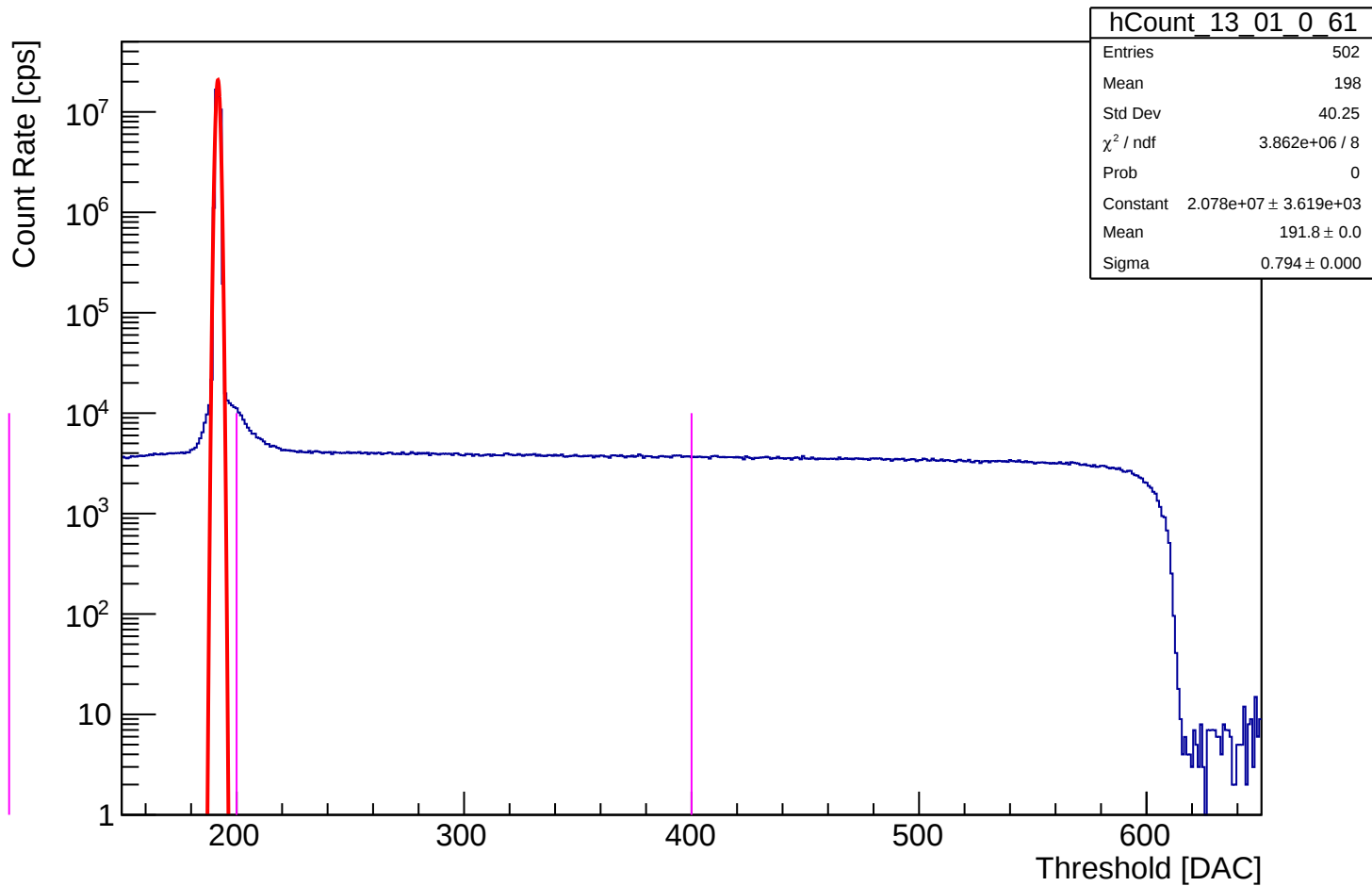
Row 1 Tile 1 Pmt 4 Pixel 61 Slot 13 Fiber 1 Asic 0 Channel 60



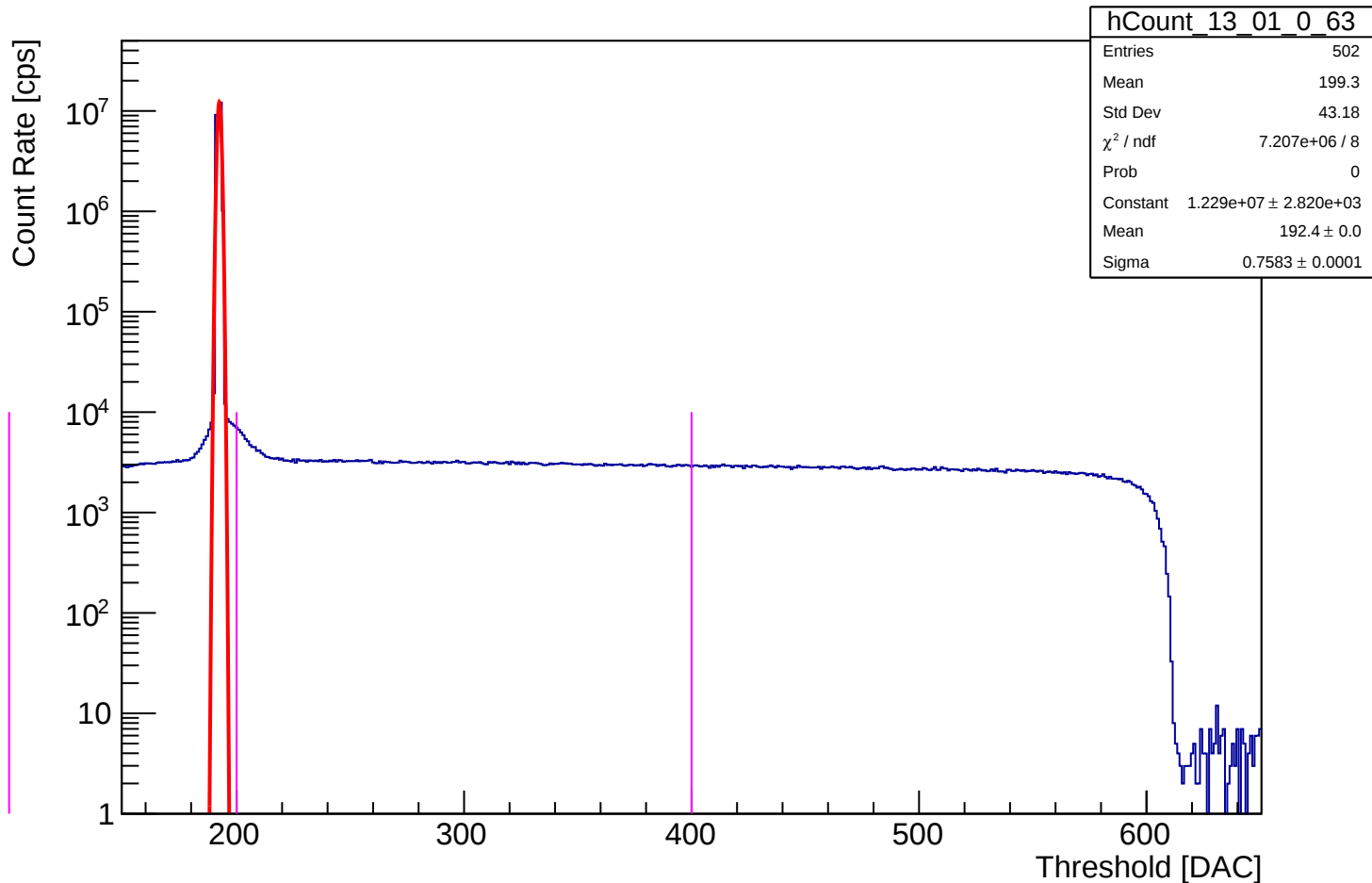
Row 1 Tile 1 Pmt 4 Pixel 62 Slot 13 Fiber 1 Asic 0 Channel 62



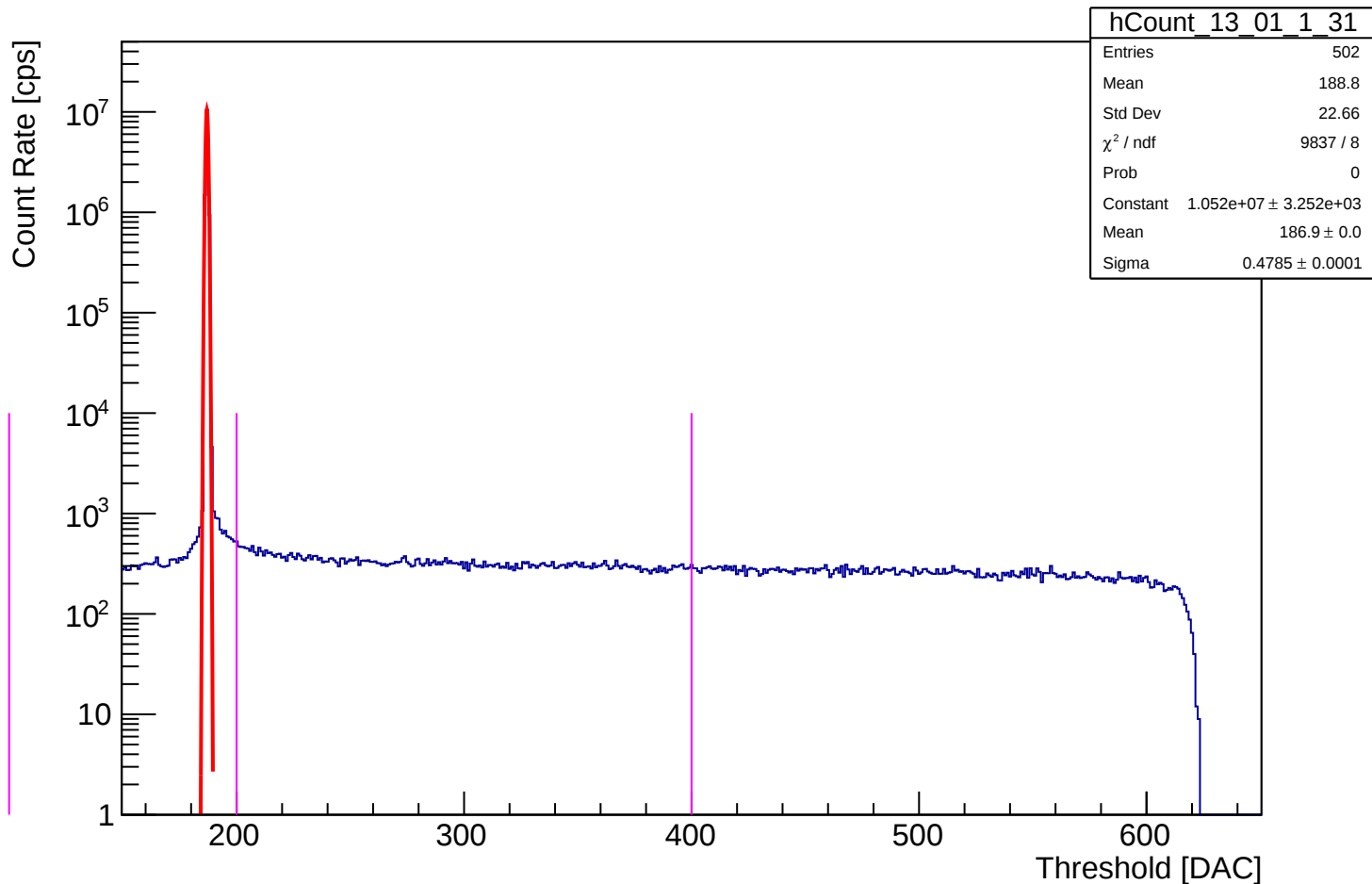
Row 1 Tile 1 Pmt 4 Pixel 63 Slot 13 Fiber 1 Asic 0 Channel 61



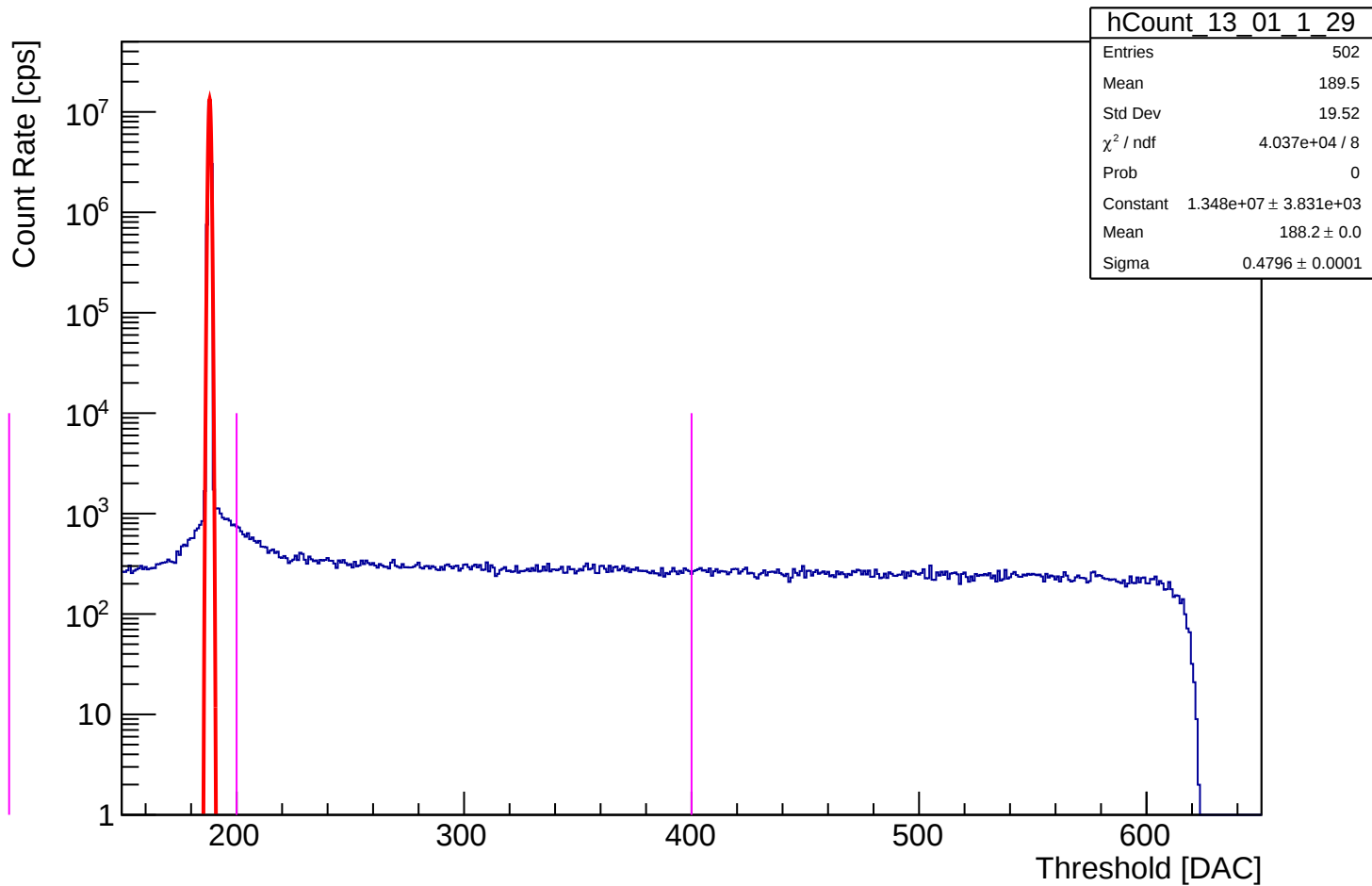
Row 1 Tile 1 Pmt 4 Pixel 64 Slot 13 Fiber 1 Asic 0 Channel 63



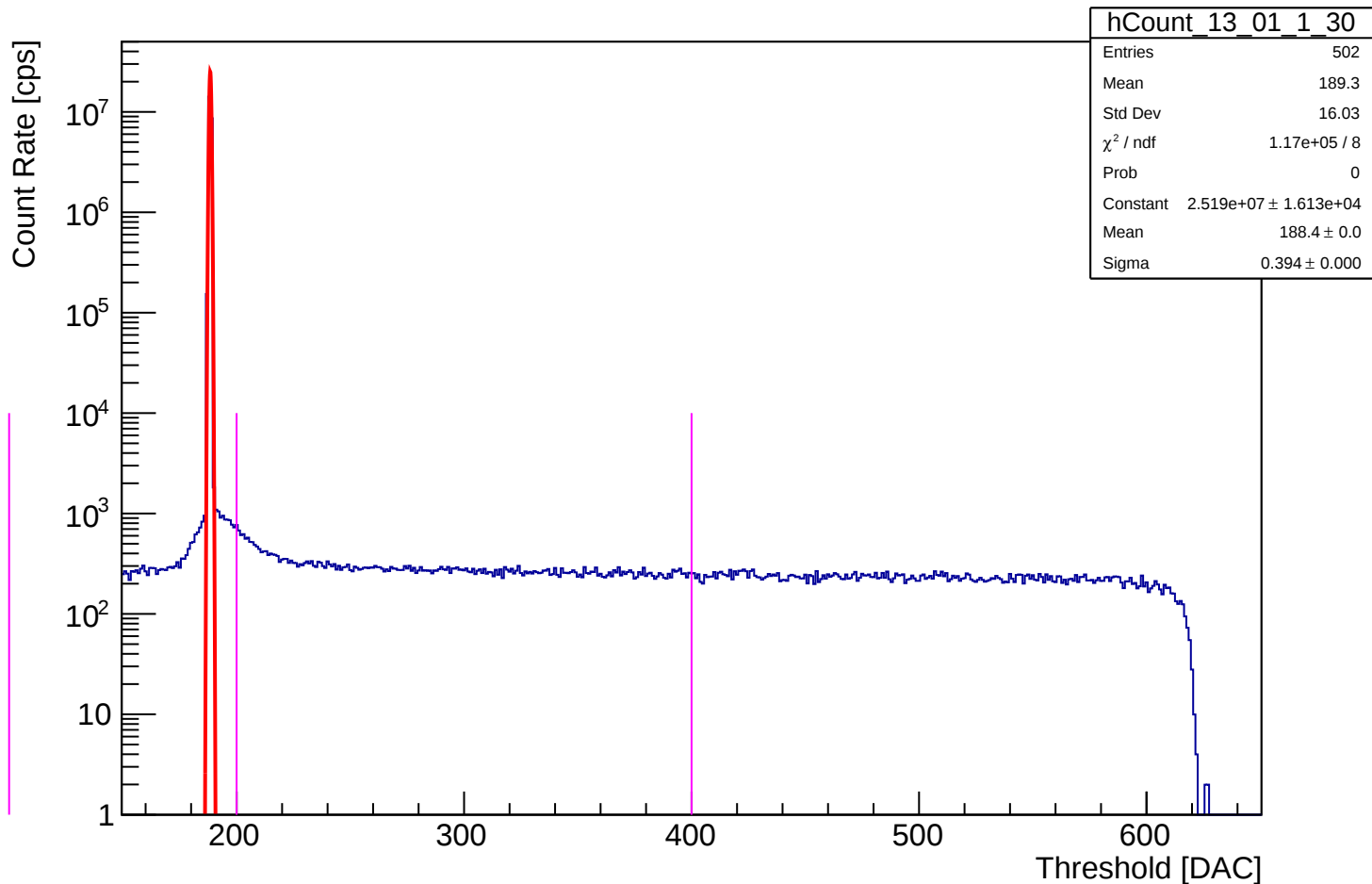
Row 1 Tile 1 Pmt 5 Pixel 1 Slot 13 Fiber 1 Asic 1 Channel 31



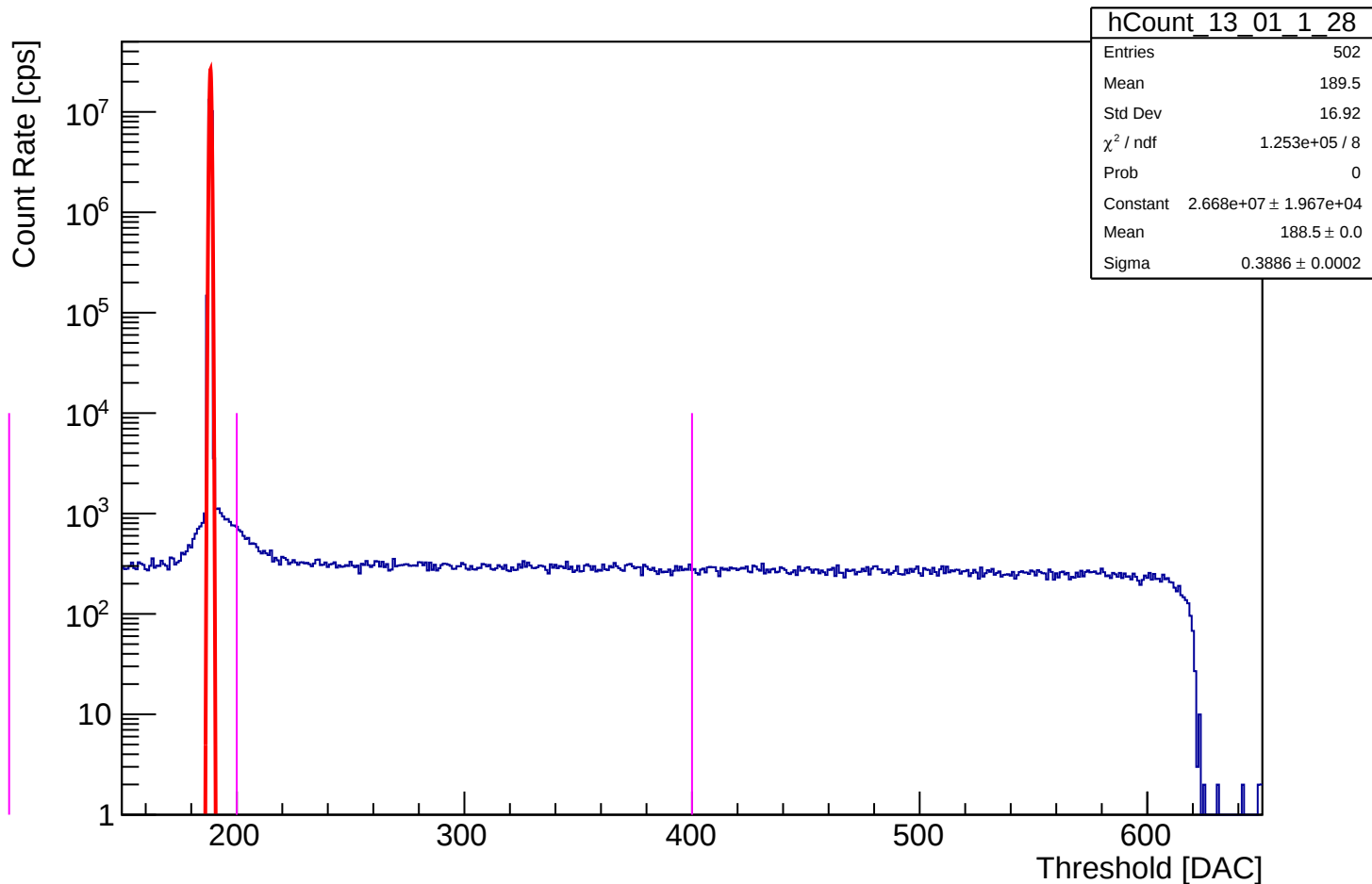
Row 1 Tile 1 Pmt 5 Pixel 2 Slot 13 Fiber 1 Asic 1 Channel 29



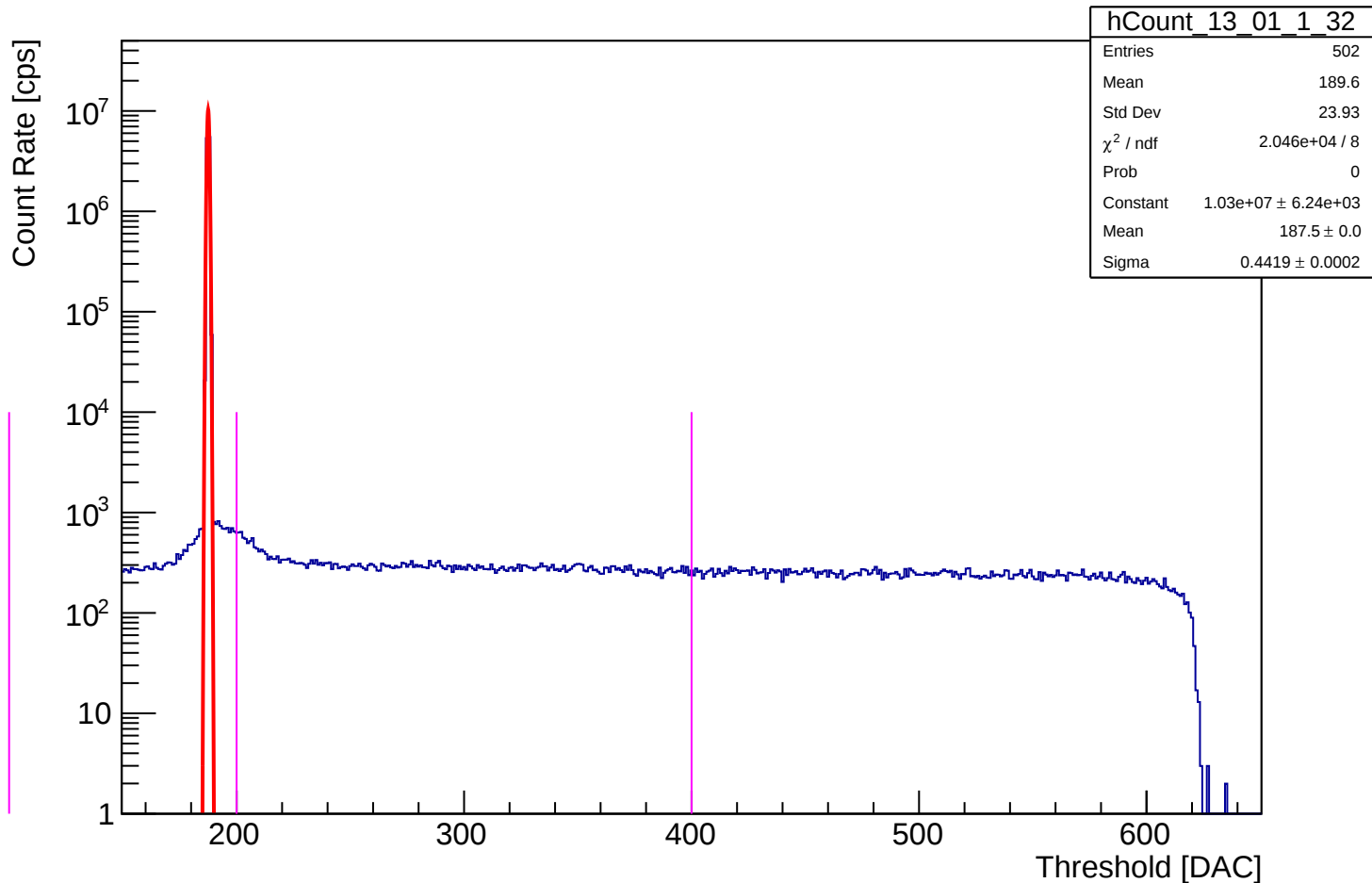
Row 1 Tile 1 Pmt 5 Pixel 3 Slot 13 Fiber 1 Asic 1 Channel 30



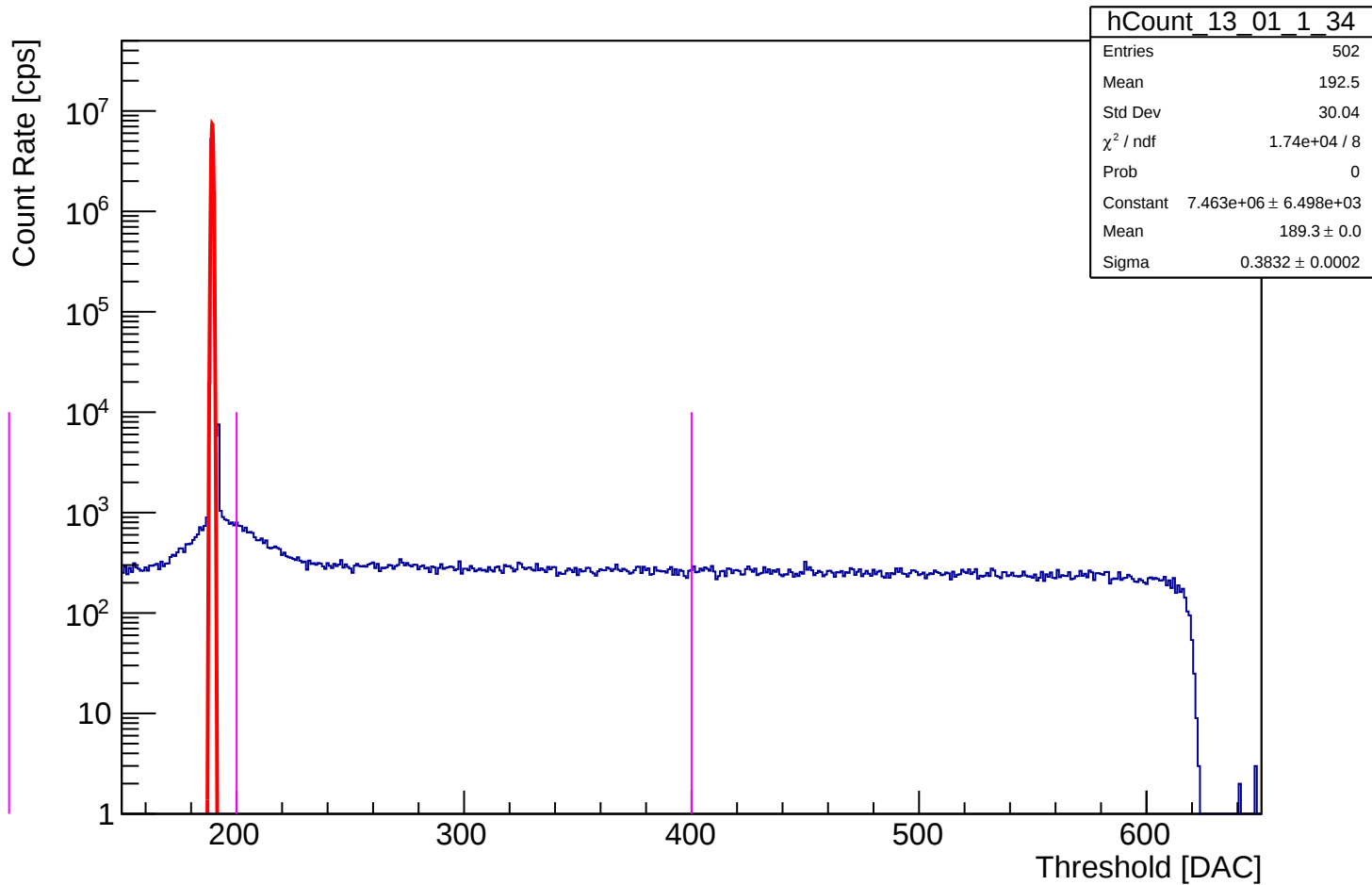
Row 1 Tile 1 Pmt 5 Pixel 4 Slot 13 Fiber 1 Asic 1 Channel 28



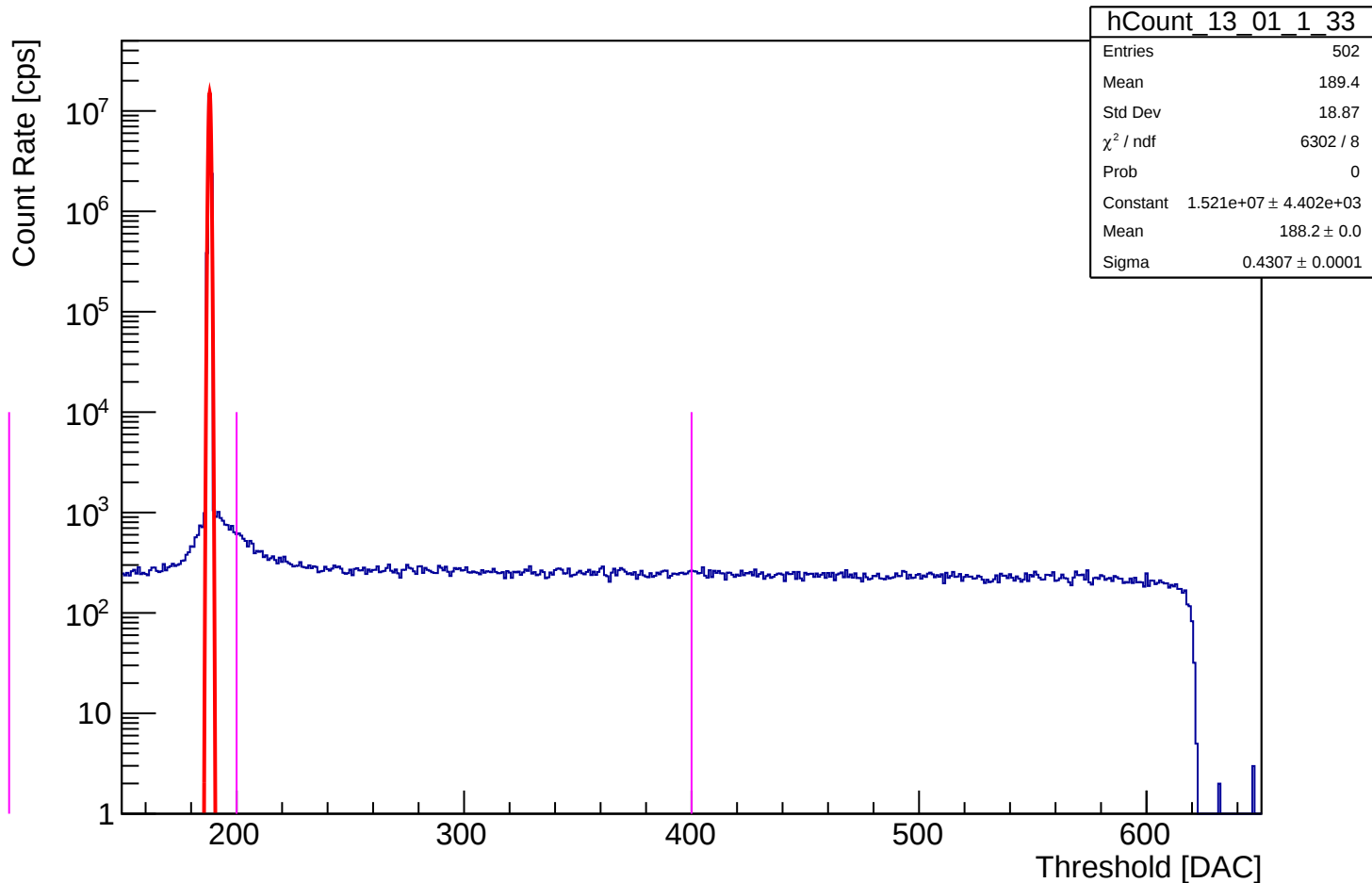
Row 1 Tile 1 Pmt 5 Pixel 5 Slot 13 Fiber 1 Asic 1 Channel 32



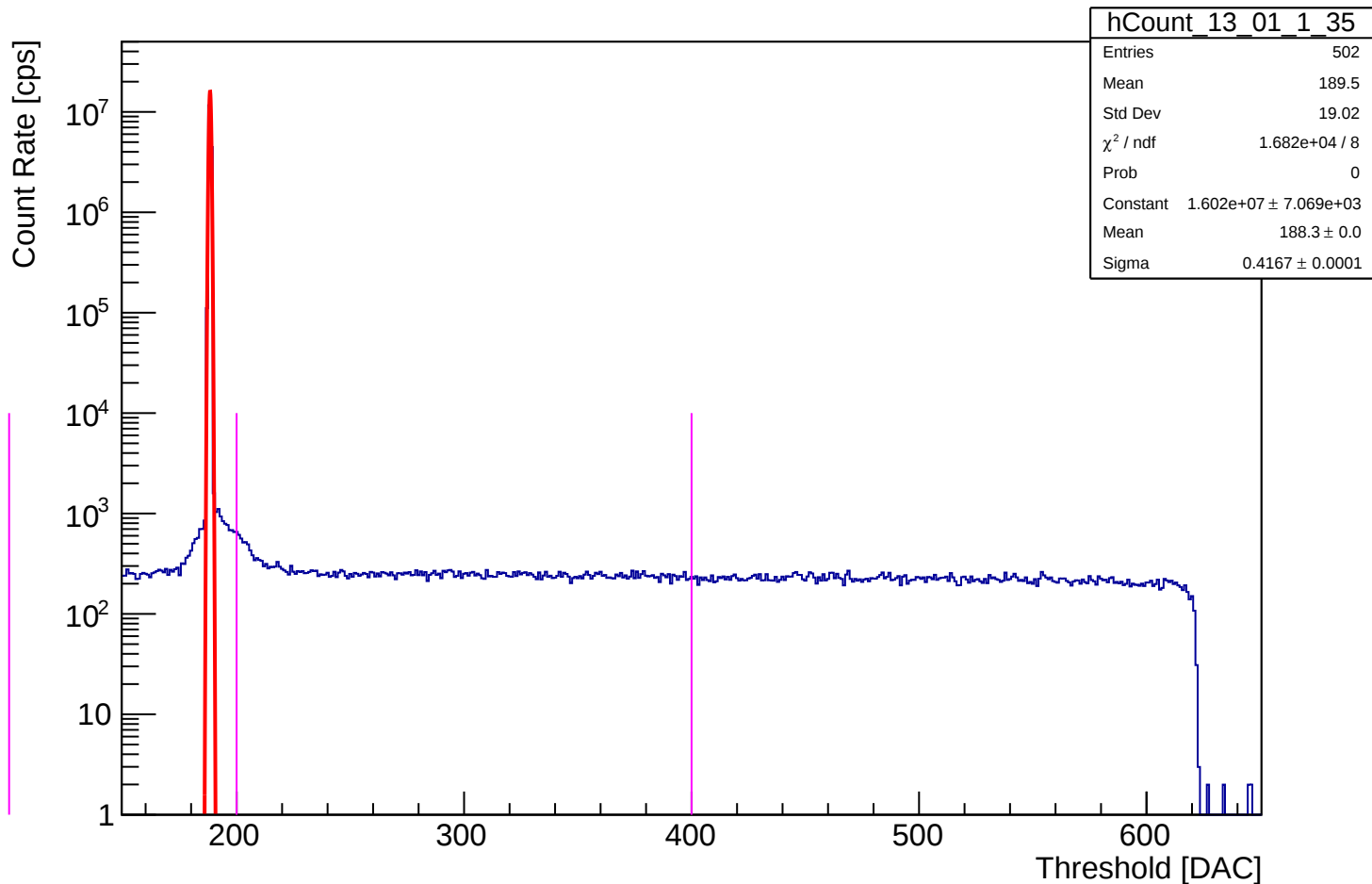
Row 1 Tile 1 Pmt 5 Pixel 6 Slot 13 Fiber 1 Asic 1 Channel 34



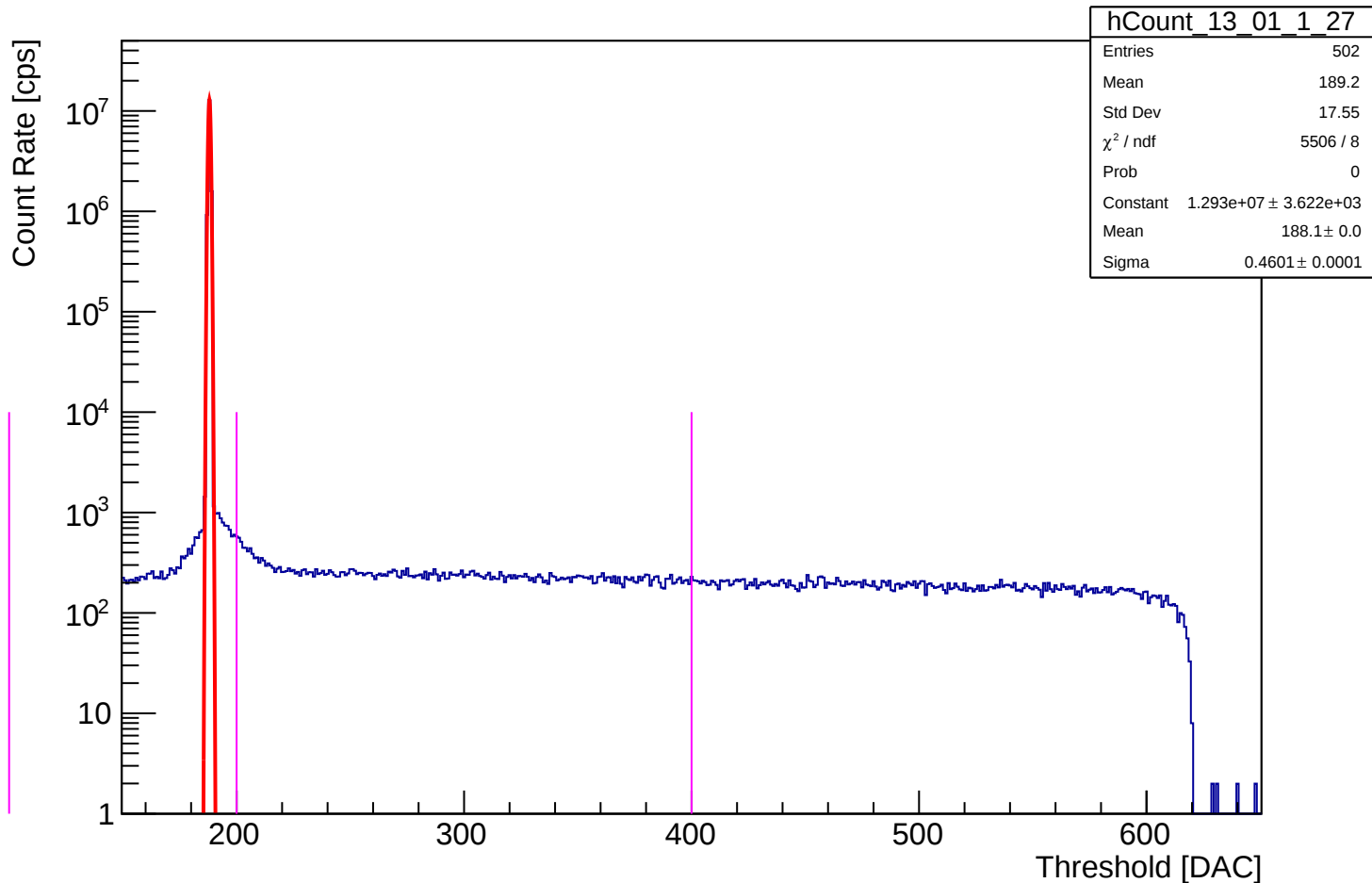
Row 1 Tile 1 Pmt 5 Pixel 7 Slot 13 Fiber 1 Asic 1 Channel 33



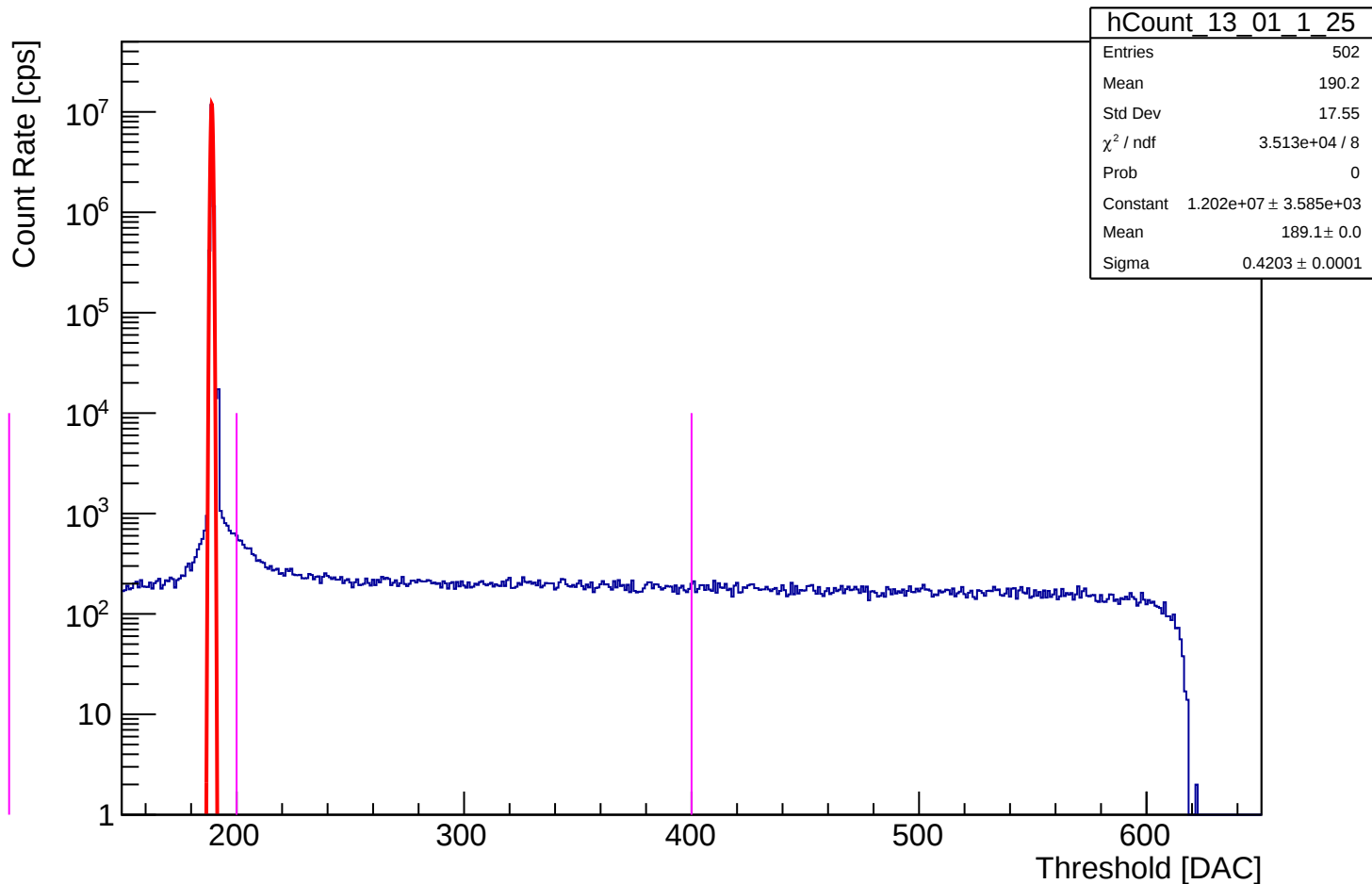
Row 1 Tile 1 Pmt 5 Pixel 8 Slot 13 Fiber 1 Asic 1 Channel 35



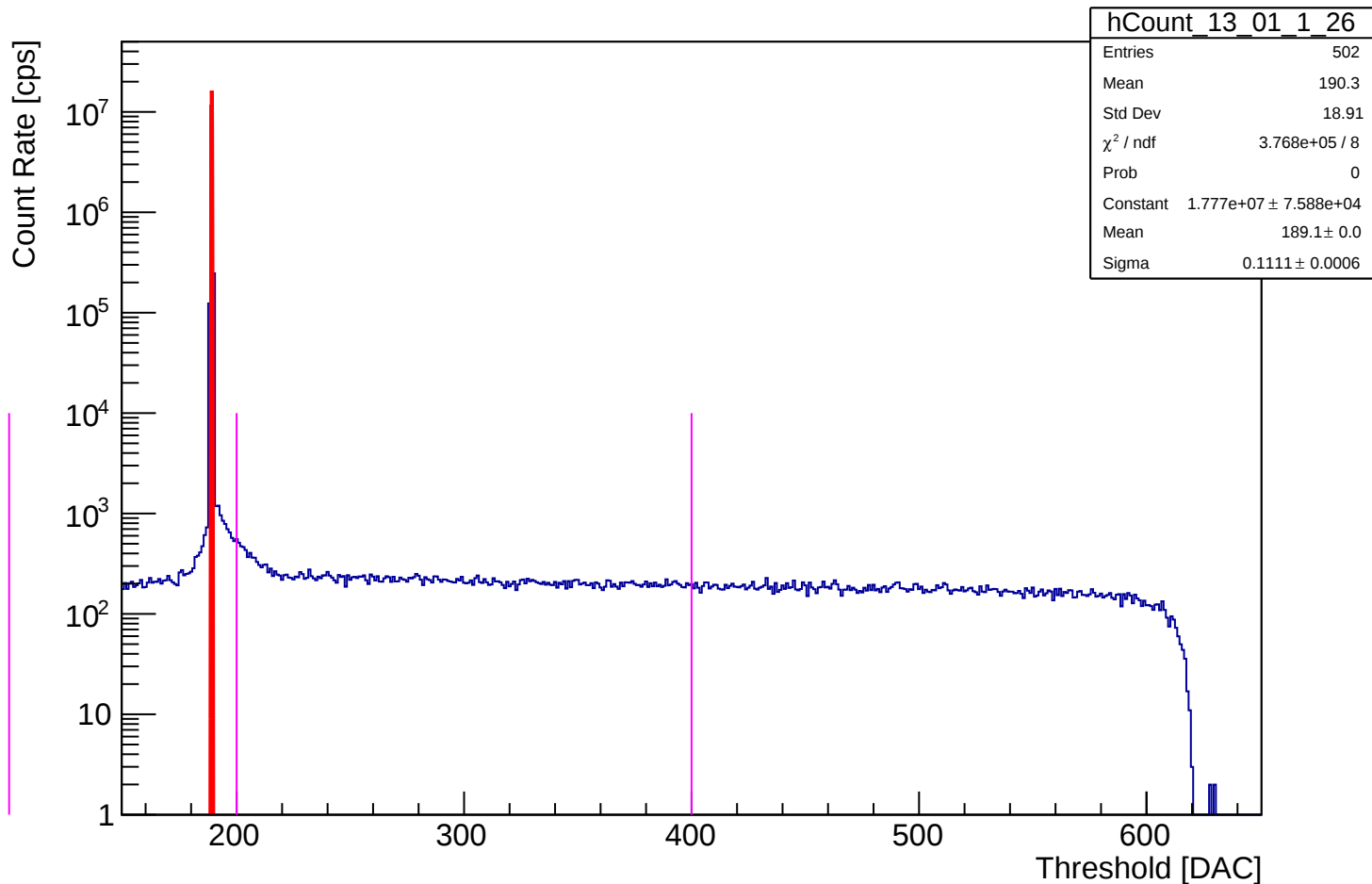
Row 1 Tile 1 Pmt 5 Pixel 9 Slot 13 Fiber 1 Asic 1 Channel 27



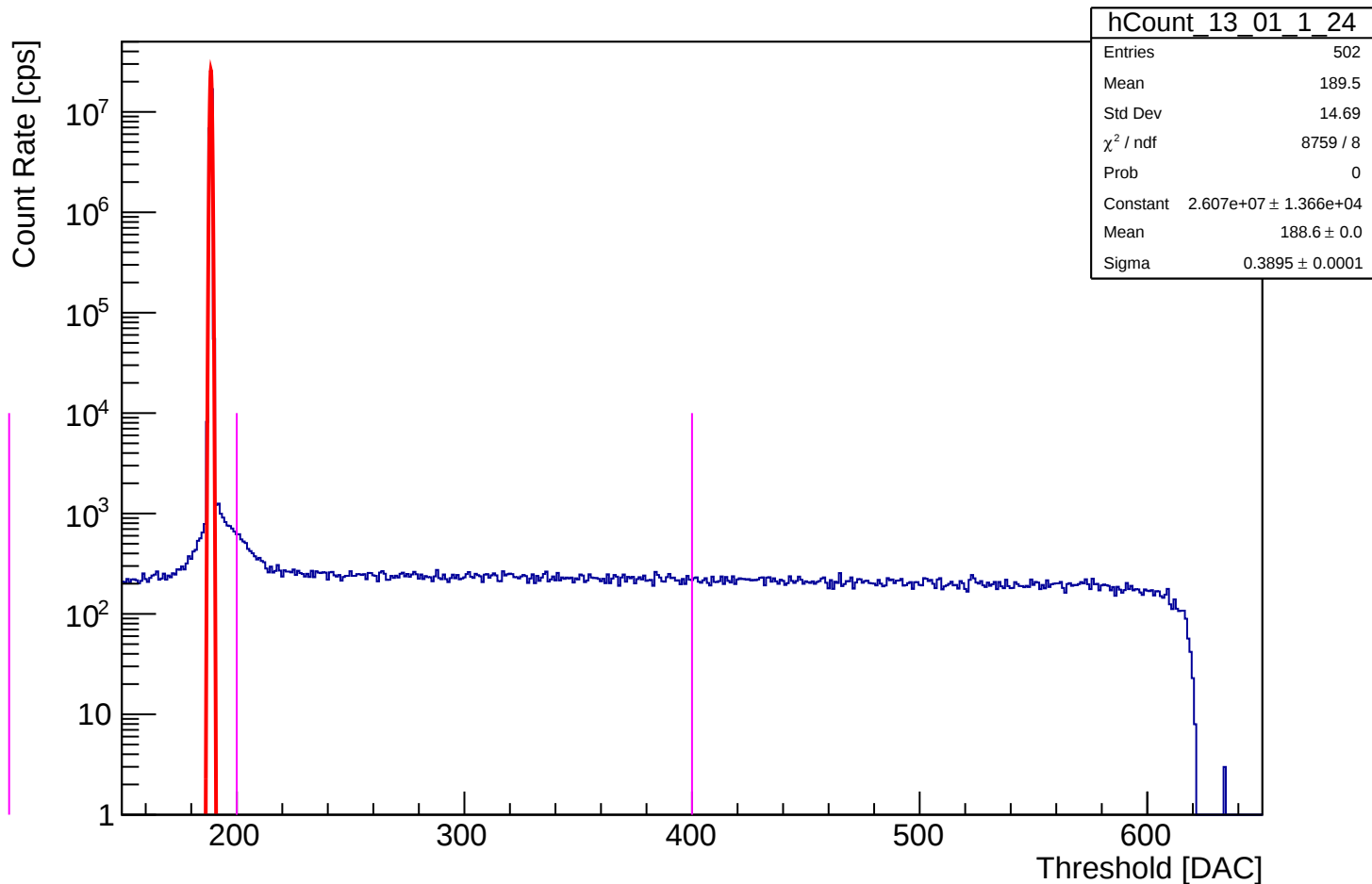
Row 1 Tile 1 Pmt 5 Pixel 10 Slot 13 Fiber 1 Asic 1 Channel 25



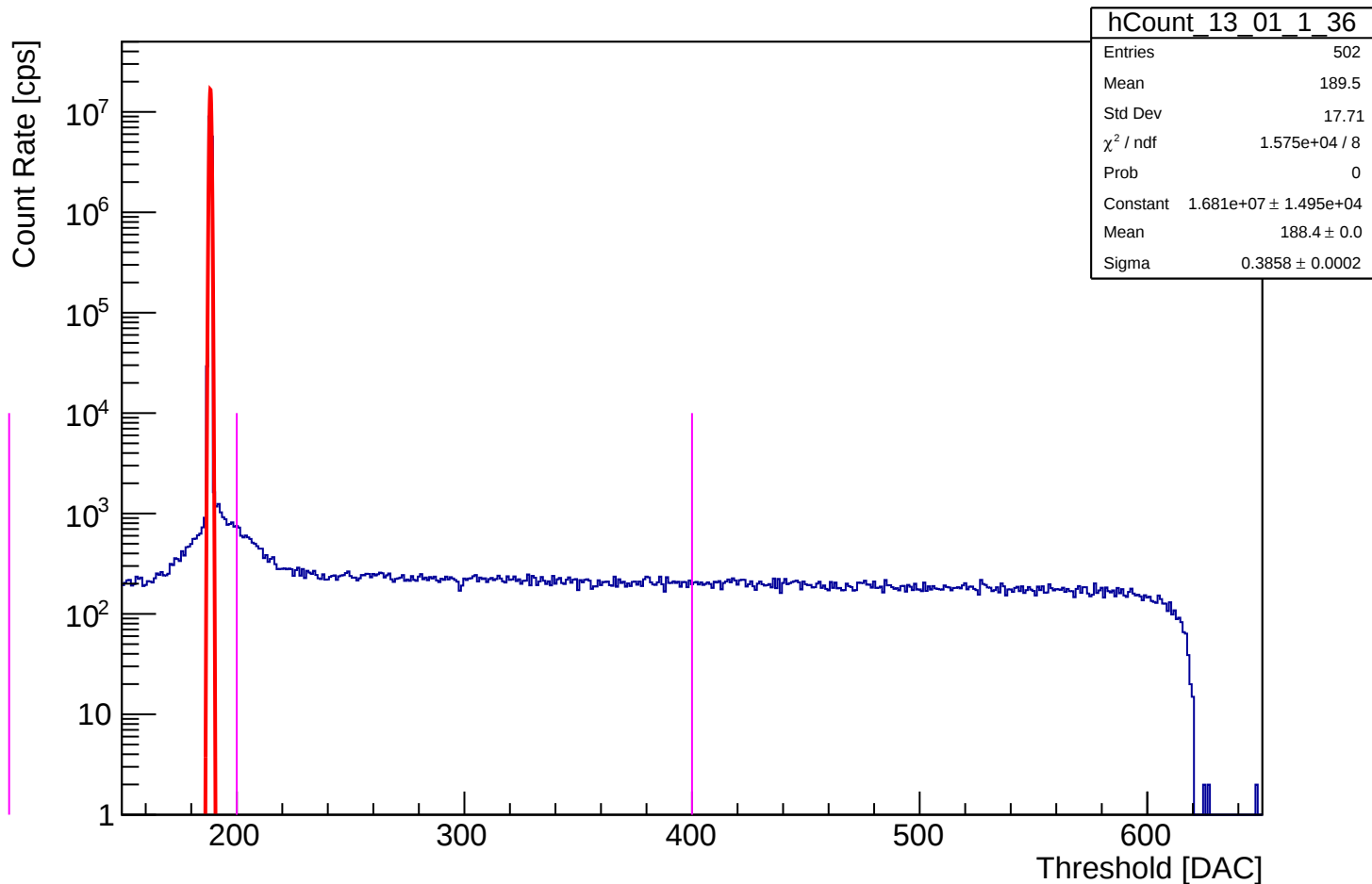
Row 1 Tile 1 Pmt 5 Pixel 11 Slot 13 Fiber 1 Asic 1 Channel 26



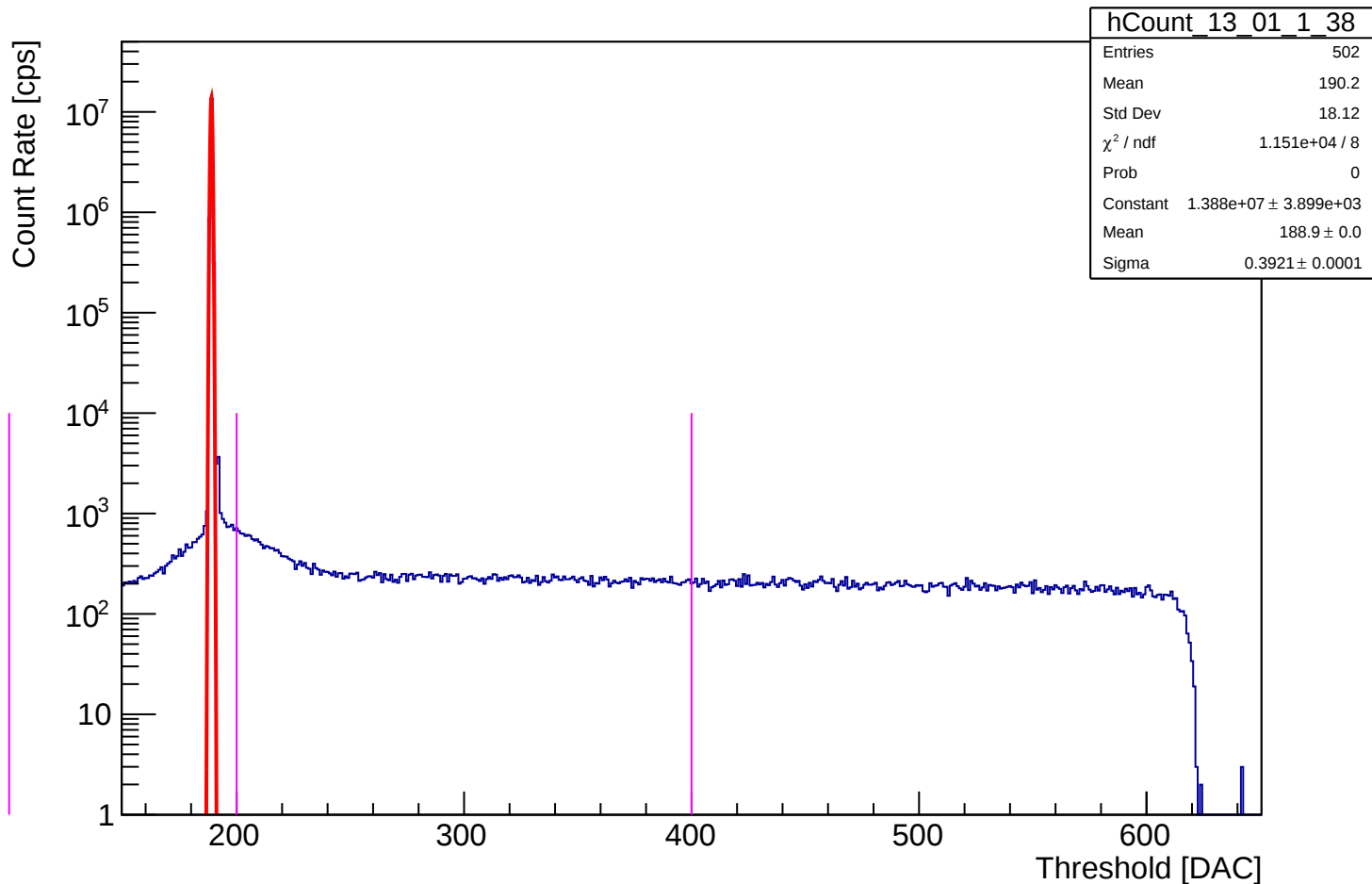
Row 1 Tile 1 Pmt 5 Pixel 12 Slot 13 Fiber 1 Asic 1 Channel 24



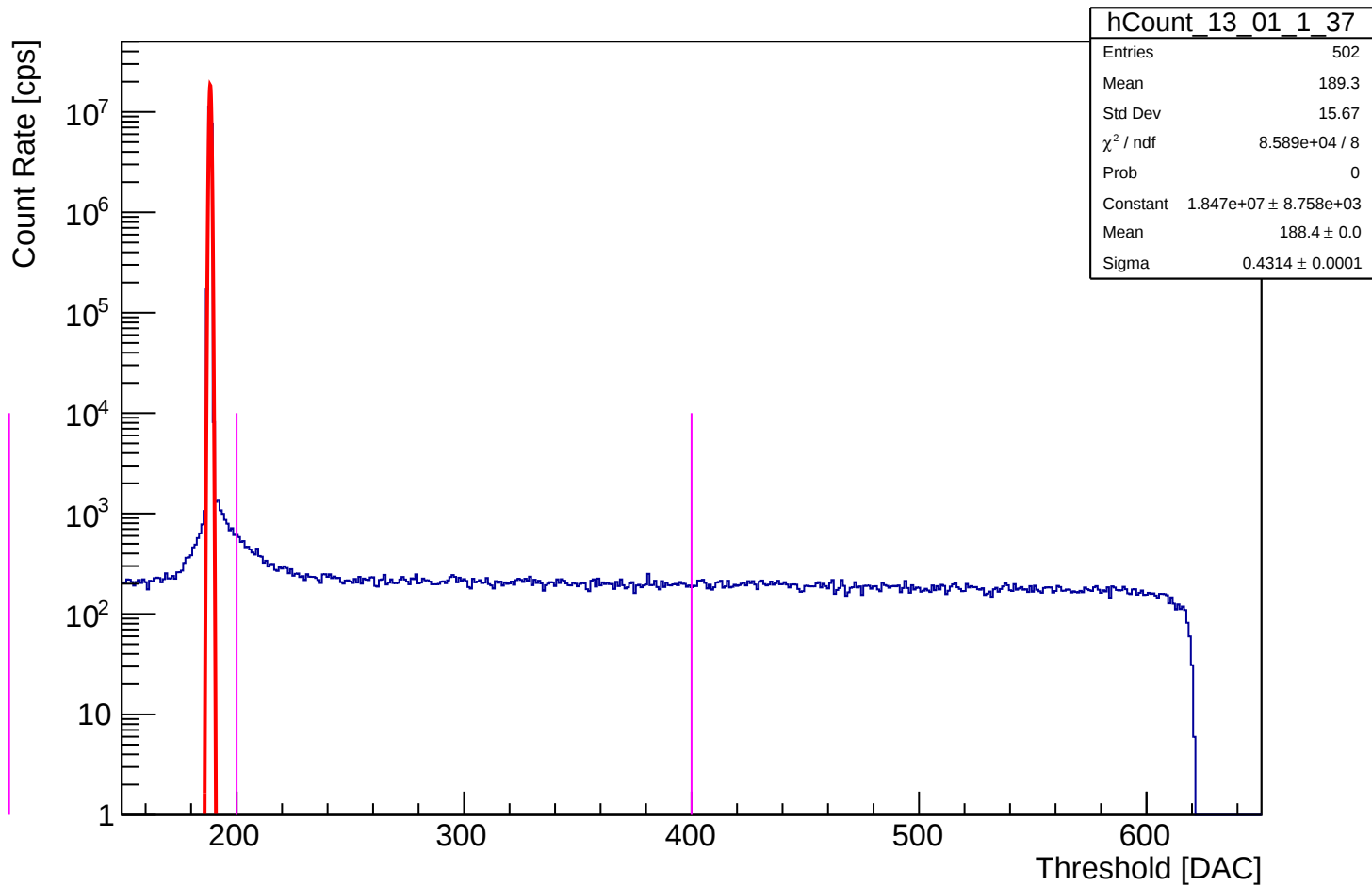
Row 1 Tile 1 Pmt 5 Pixel 13 Slot 13 Fiber 1 Asic 1 Channel 36



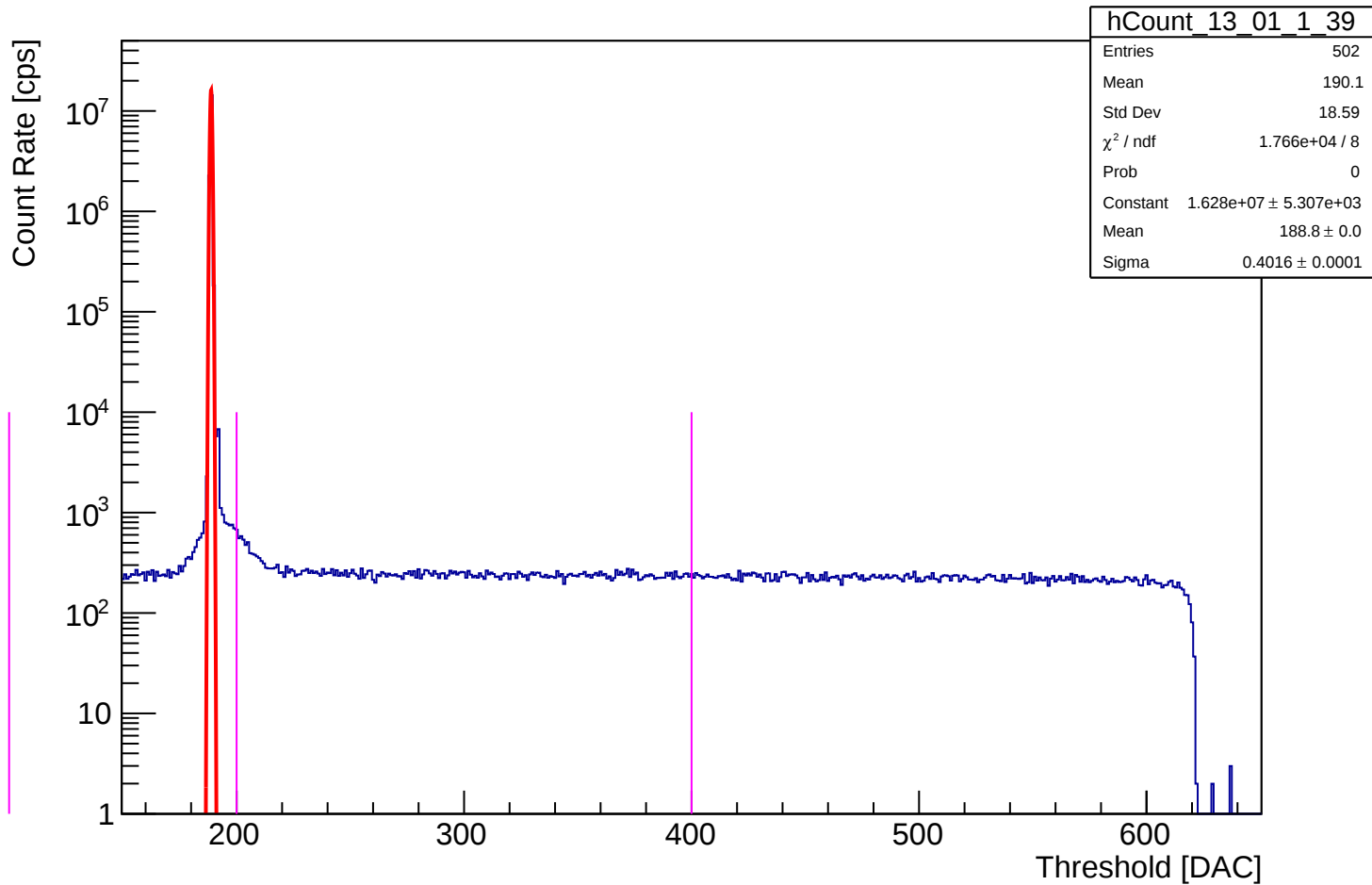
Row 1 Tile 1 Pmt 5 Pixel 14 Slot 13 Fiber 1 Asic 1 Channel 38



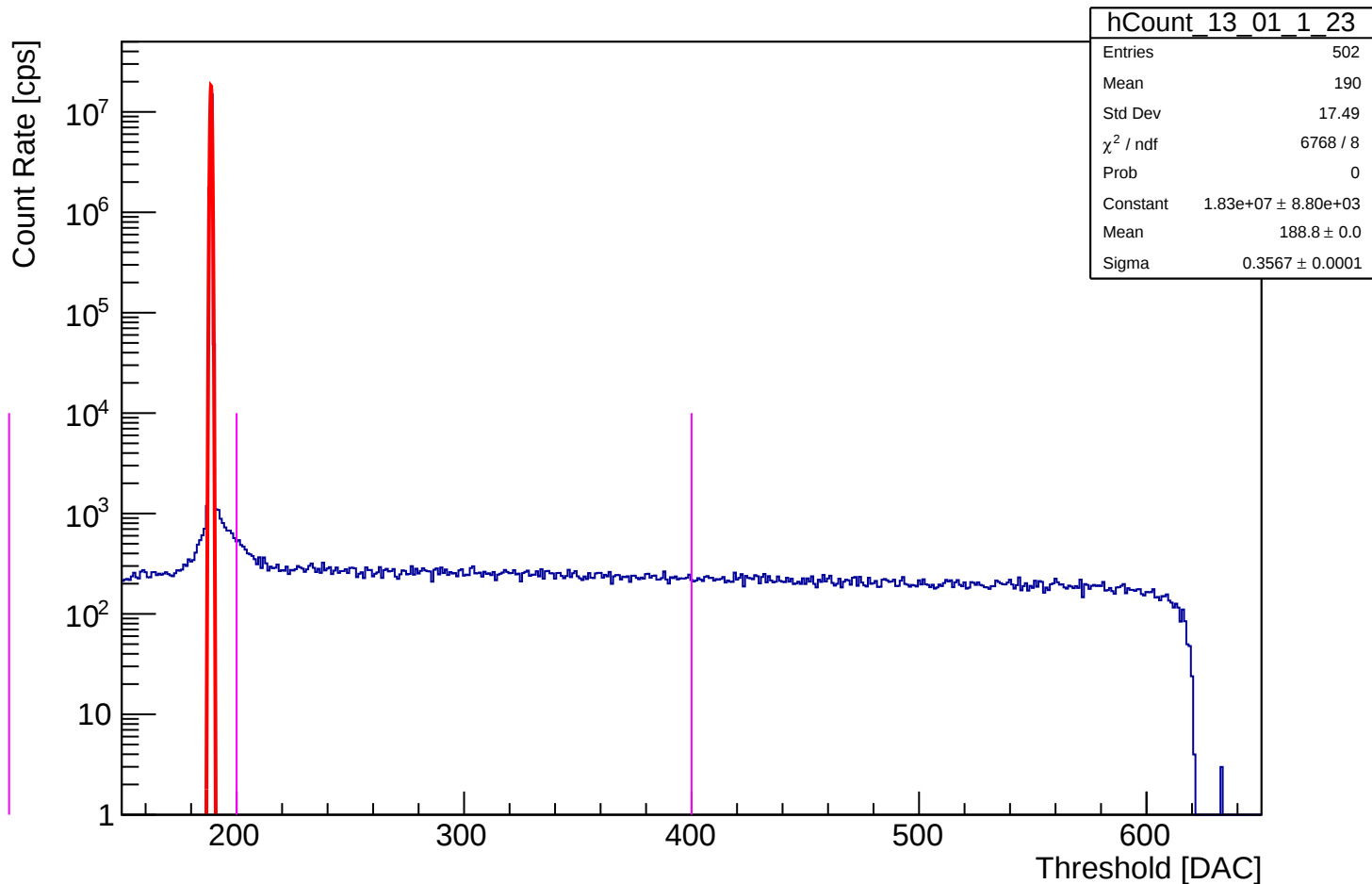
Row 1 Tile 1 Pmt 5 Pixel 15 Slot 13 Fiber 1 Asic 1 Channel 37



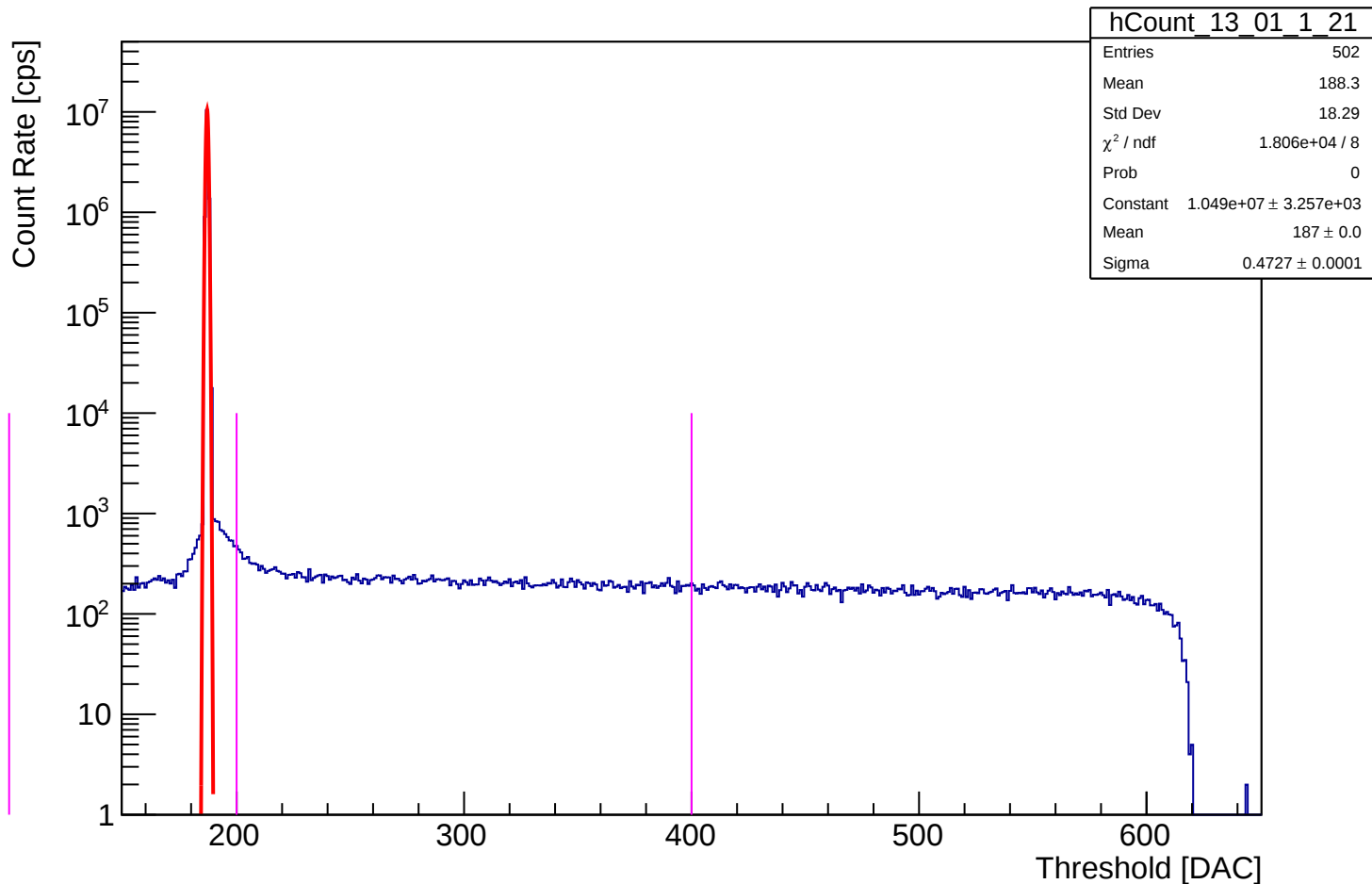
Row 1 Tile 1 Pmt 5 Pixel 16 Slot 13 Fiber 1 Asic 1 Channel 39



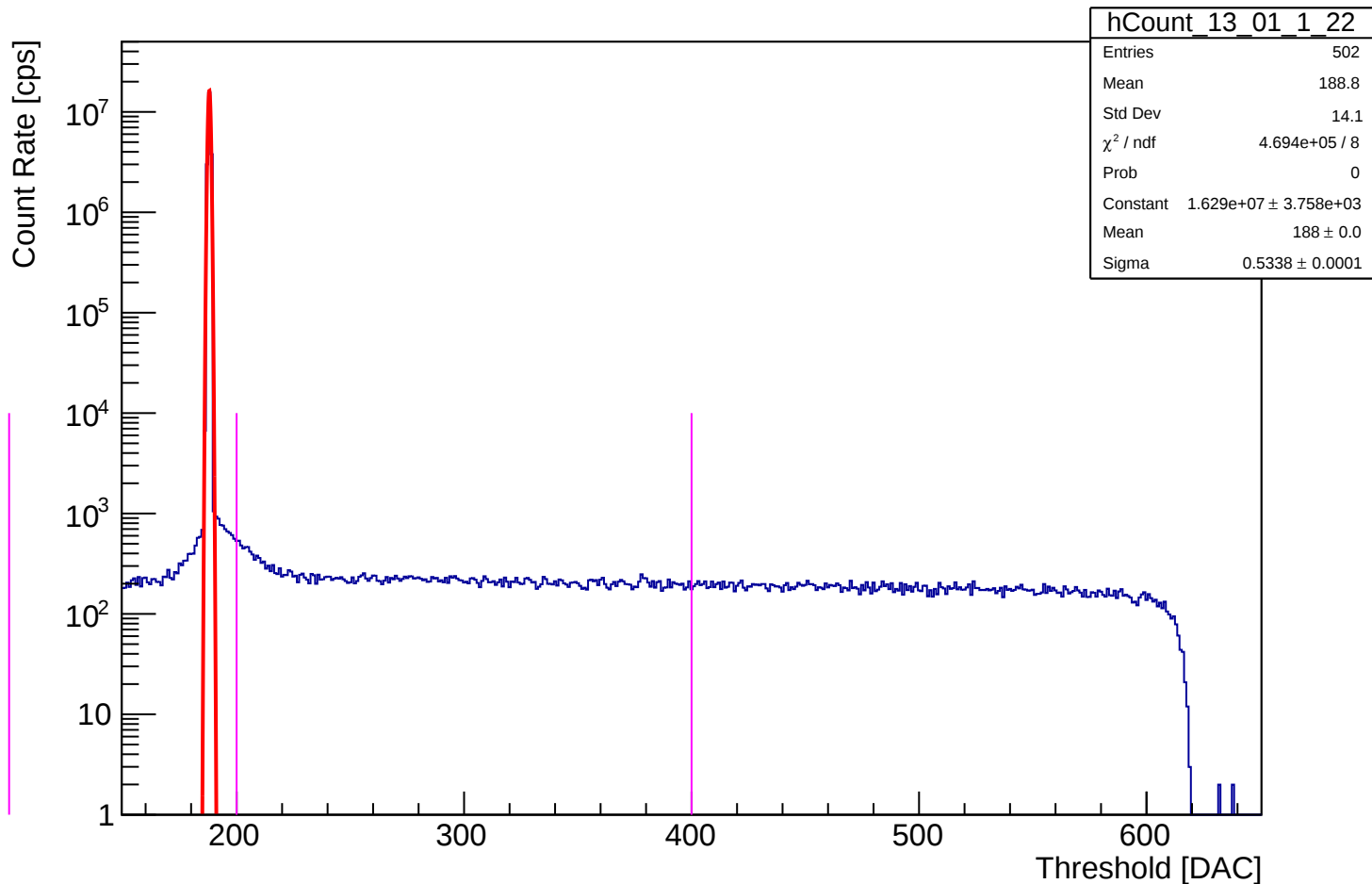
Row 1 Tile 1 Pmt 5 Pixel 17 Slot 13 Fiber 1 Asic 1 Channel 23



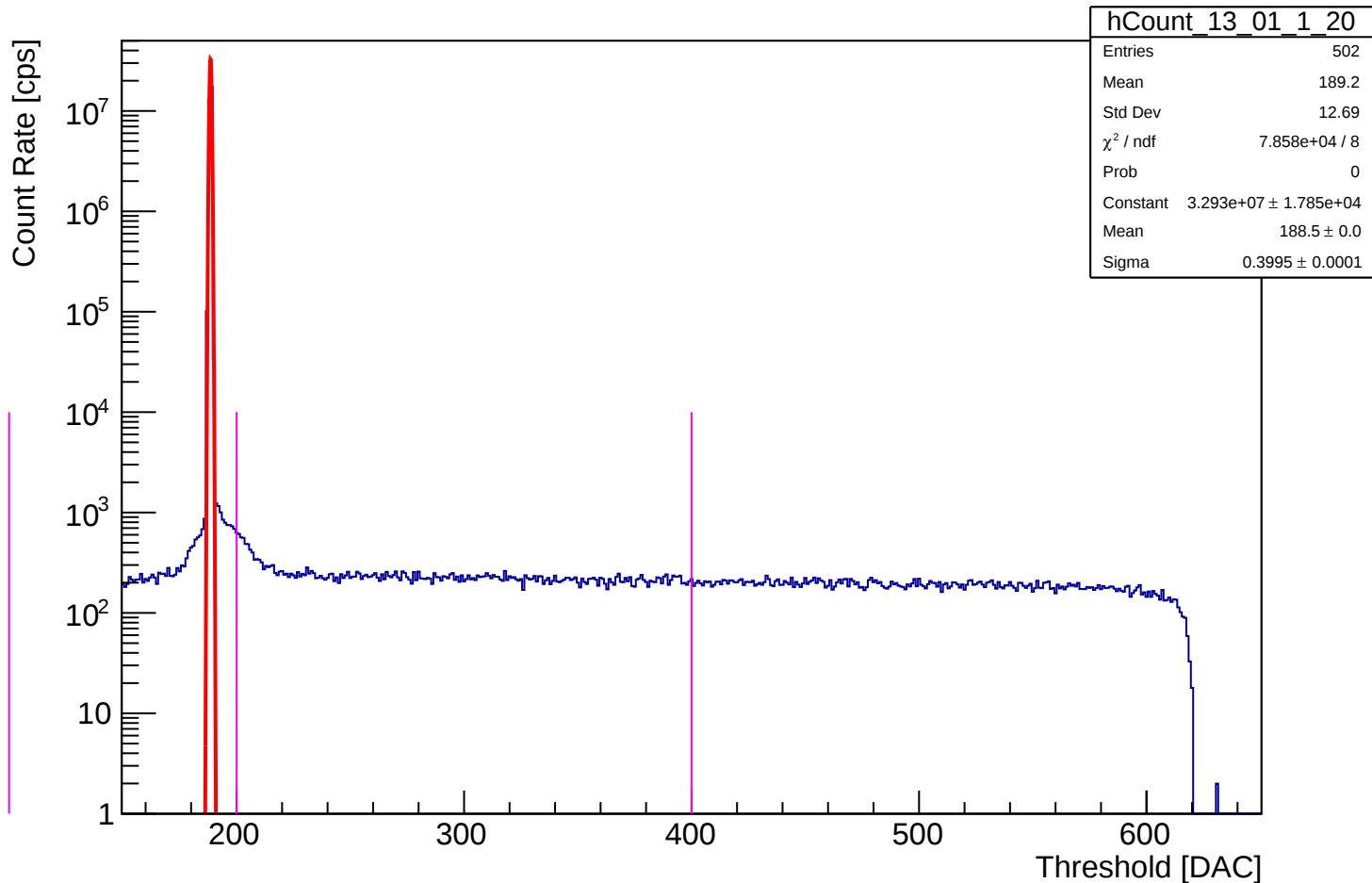
Row 1 Tile 1 Pmt 5 Pixel 18 Slot 13 Fiber 1 Asic 1 Channel 21



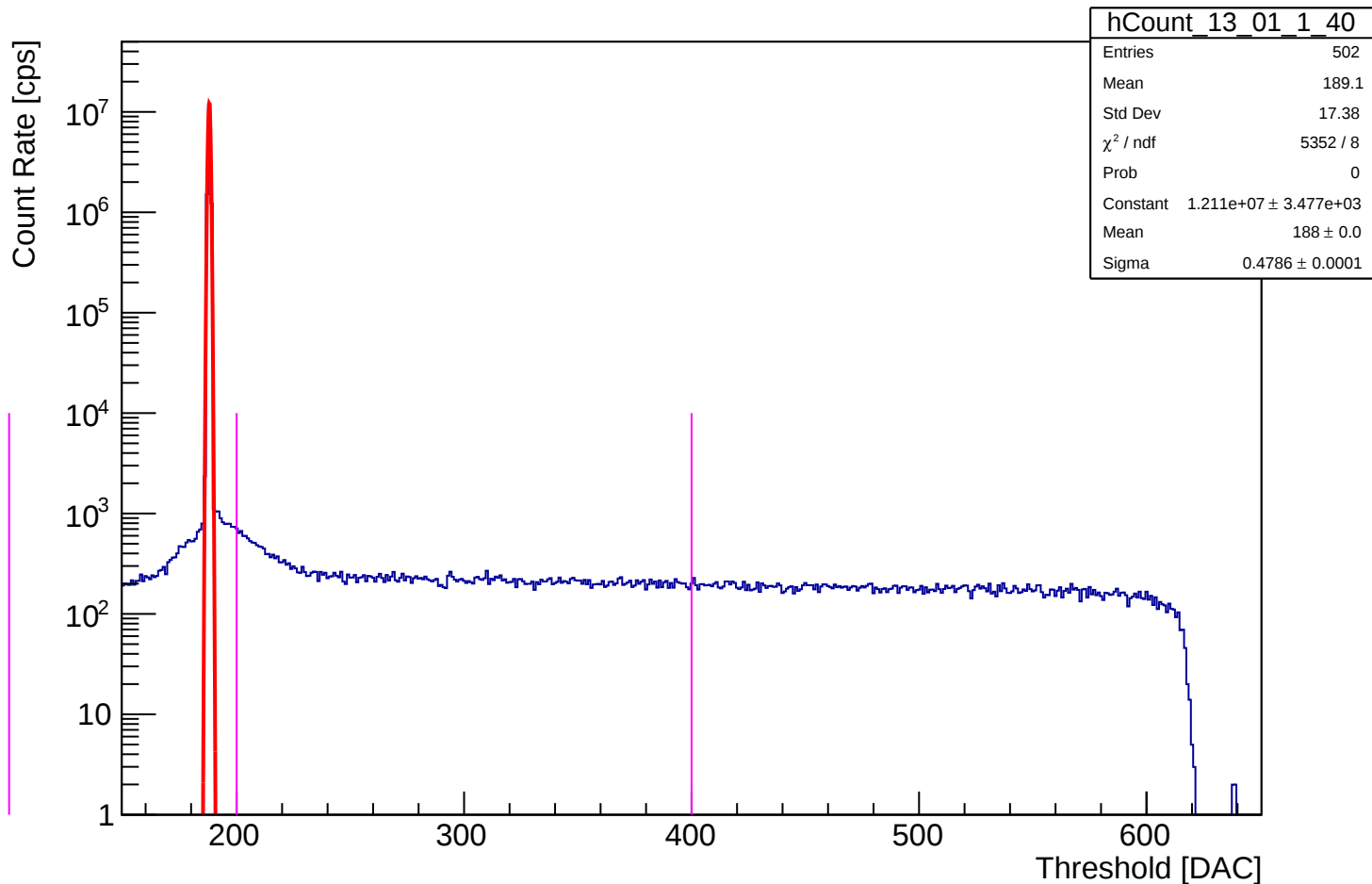
Row 1 Tile 1 Pmt 5 Pixel 19 Slot 13 Fiber 1 Asic 1 Channel 22



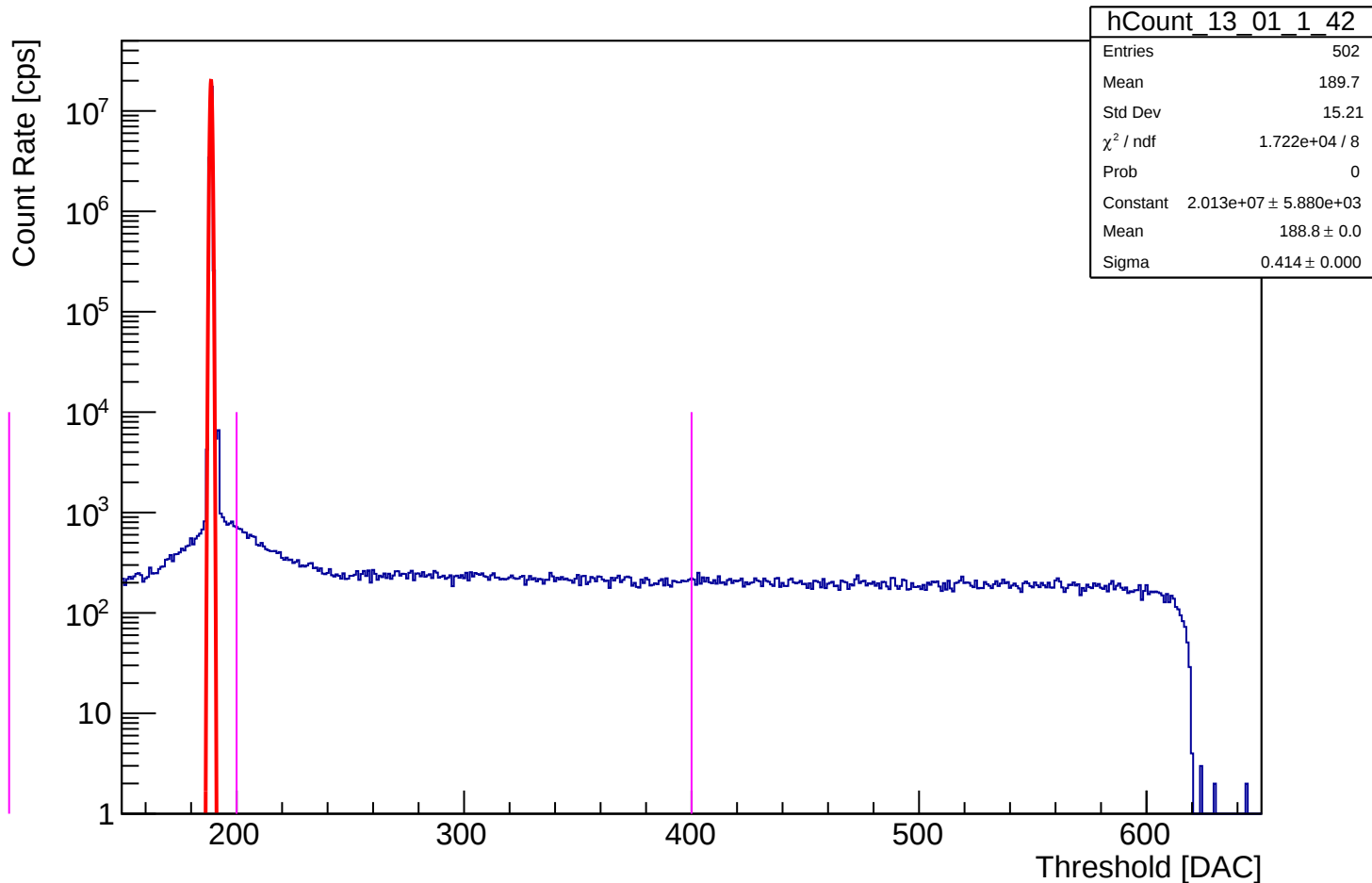
Row 1 Tile 1 Pmt 5 Pixel 20 Slot 13 Fiber 1 Asic 1 Channel 20

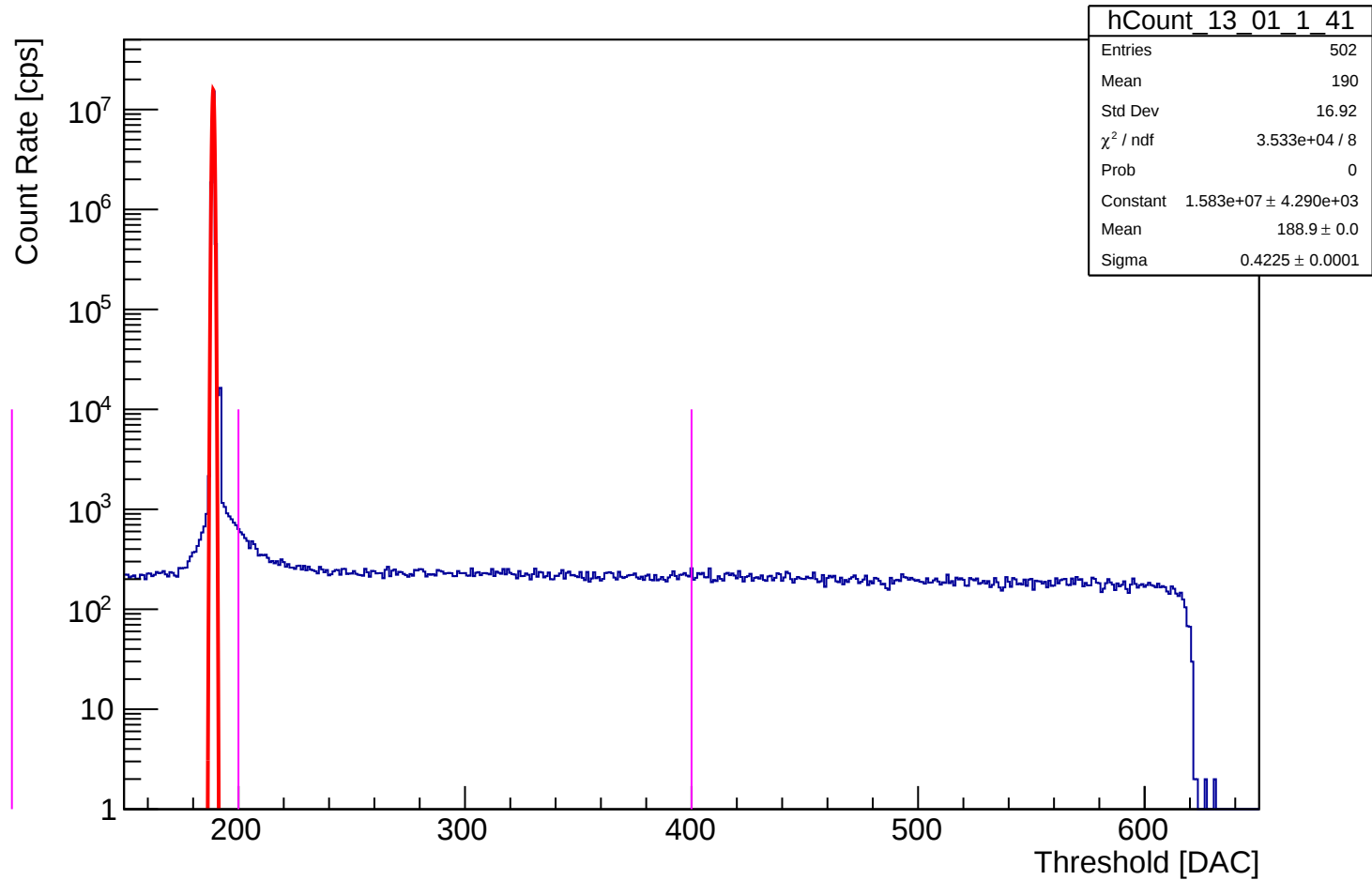


Row 1 Tile 1 Pmt 5 Pixel 21 Slot 13 Fiber 1 Asic 1 Channel 40

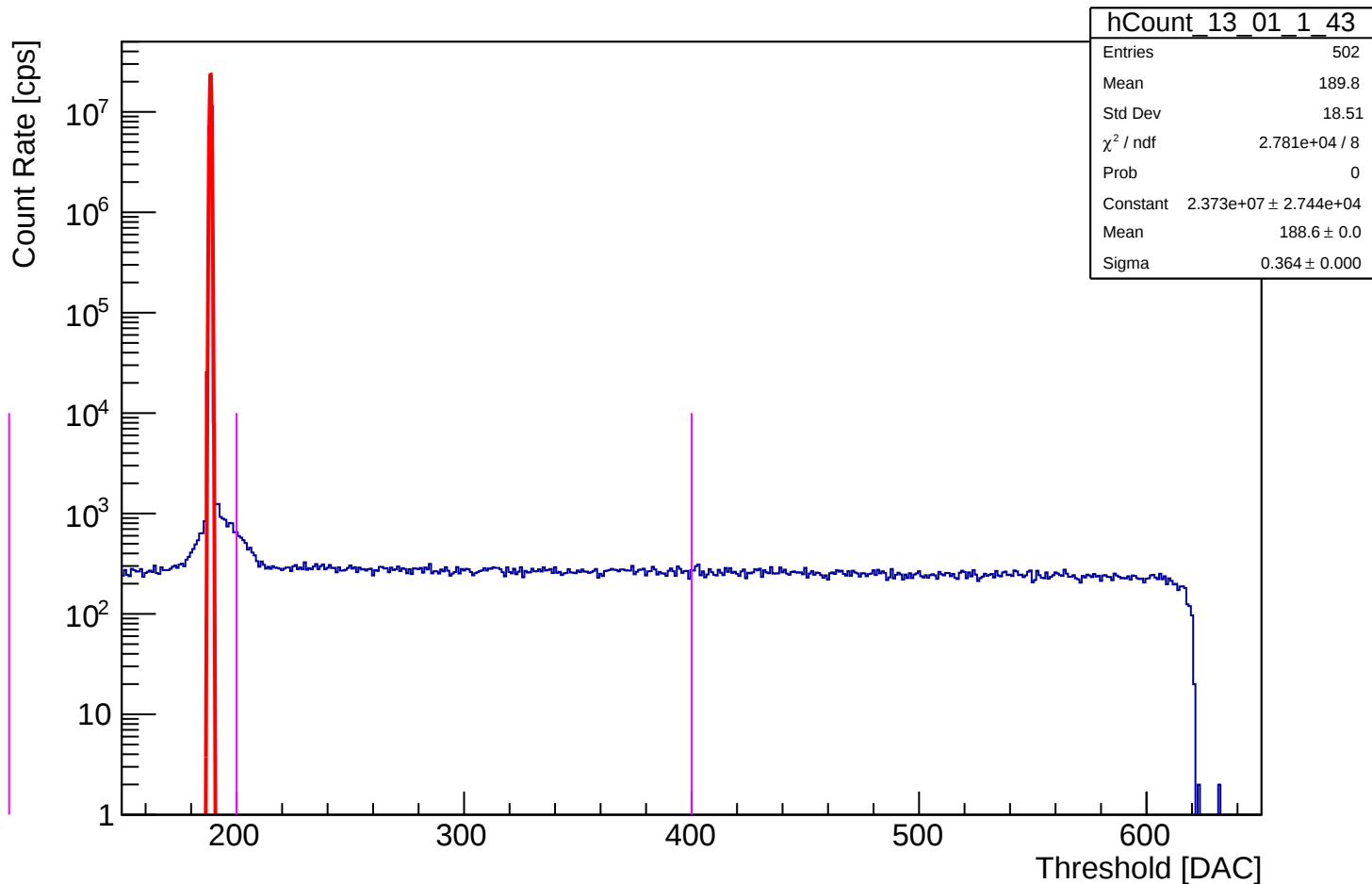


Row 1 Tile 1 Pmt 5 Pixel 22 Slot 13 Fiber 1 Asic 1 Channel 42

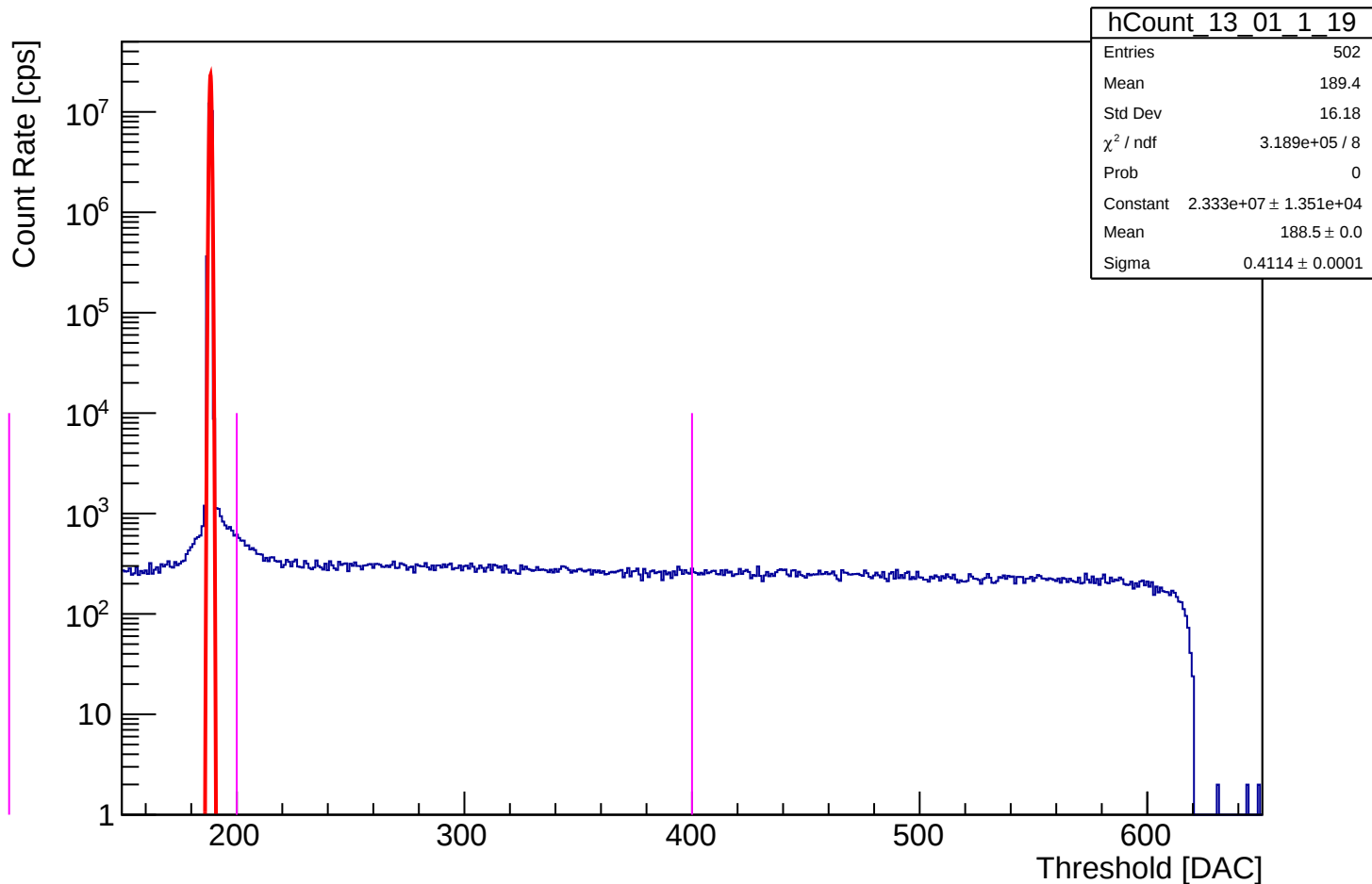




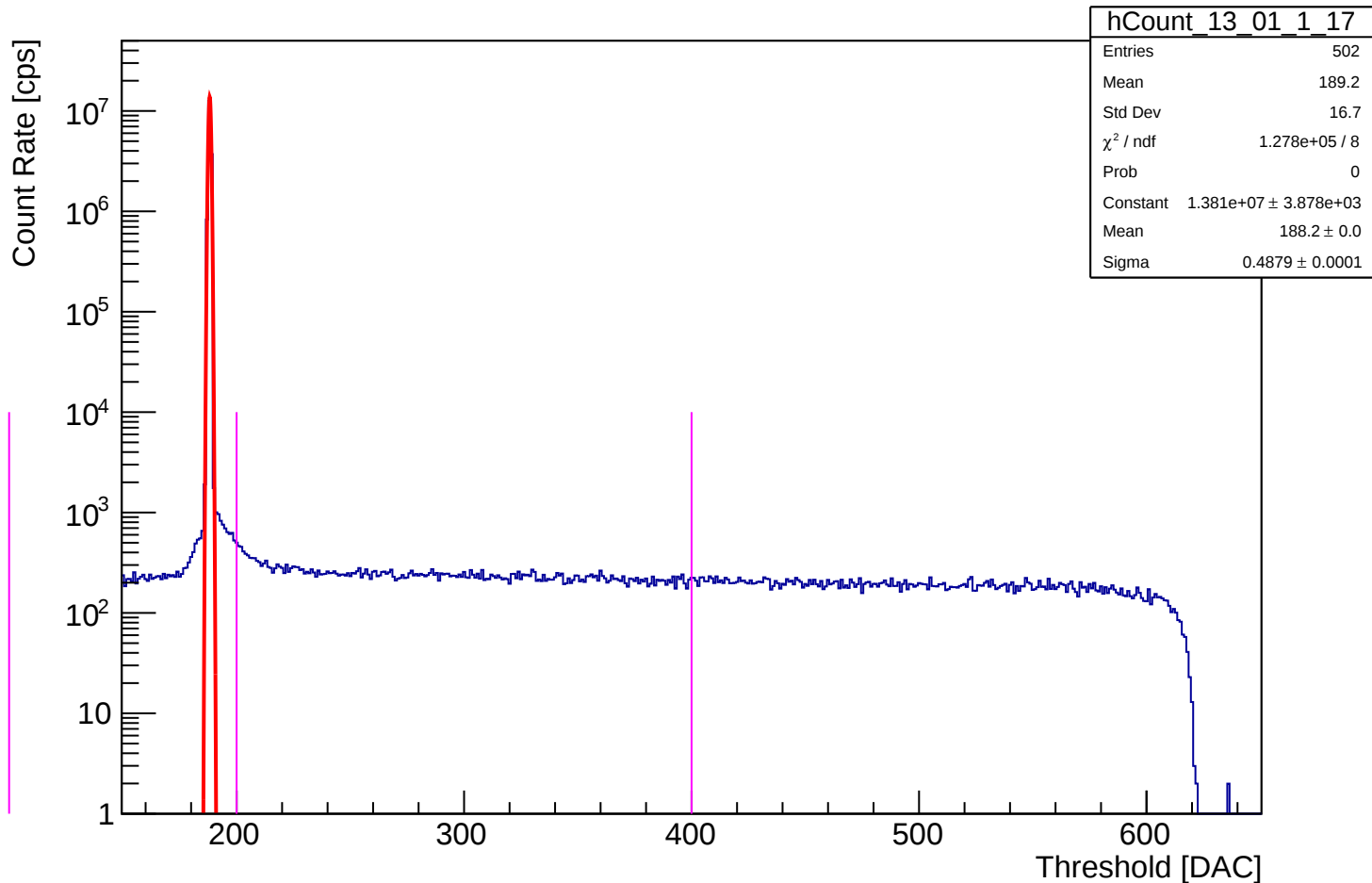
Row 1 Tile 1 Pmt 5 Pixel 24 Slot 13 Fiber 1 Asic 1 Channel 43



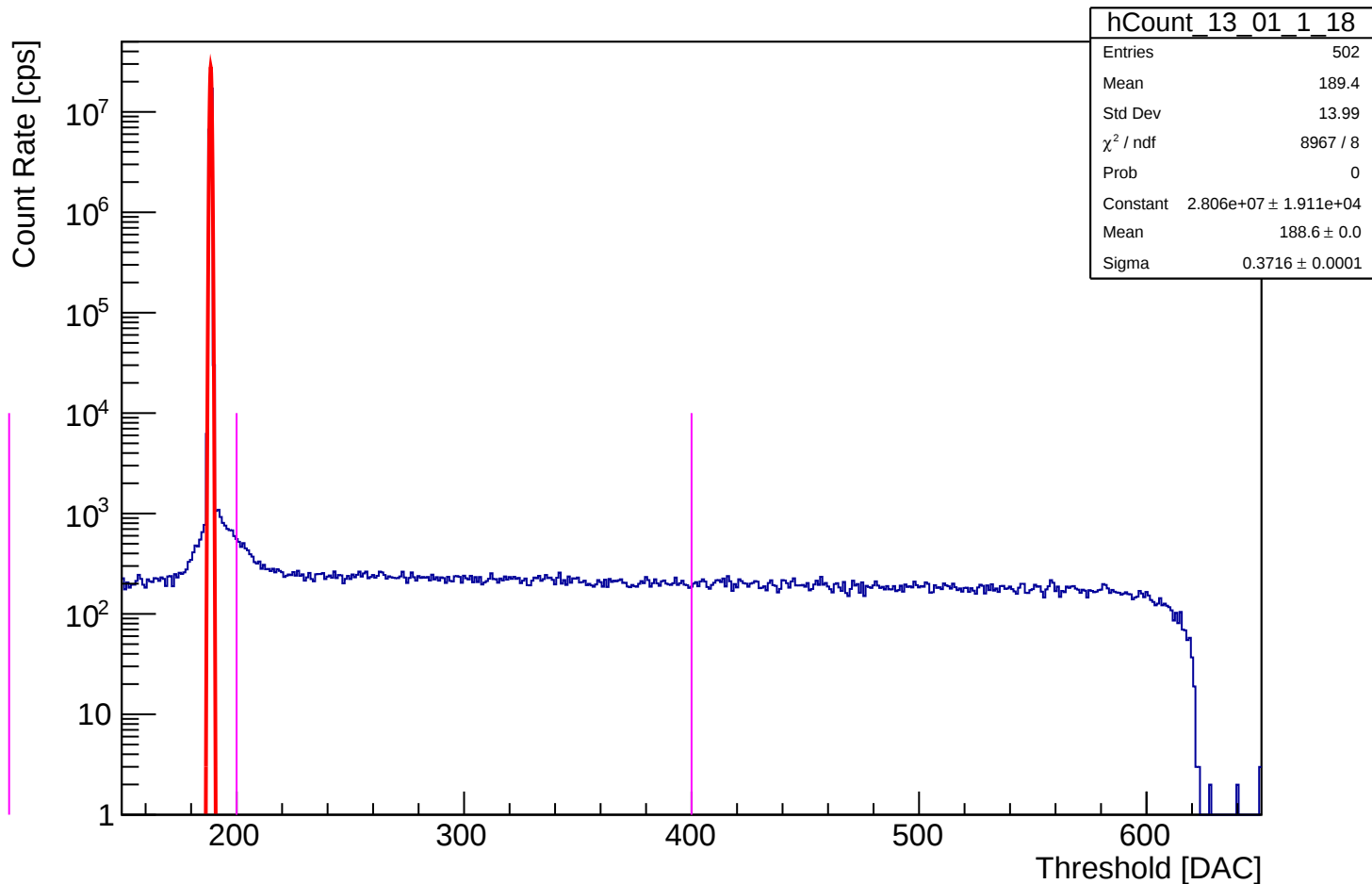
Row 1 Tile 1 Pmt 5 Pixel 25 Slot 13 Fiber 1 Asic 1 Channel 19



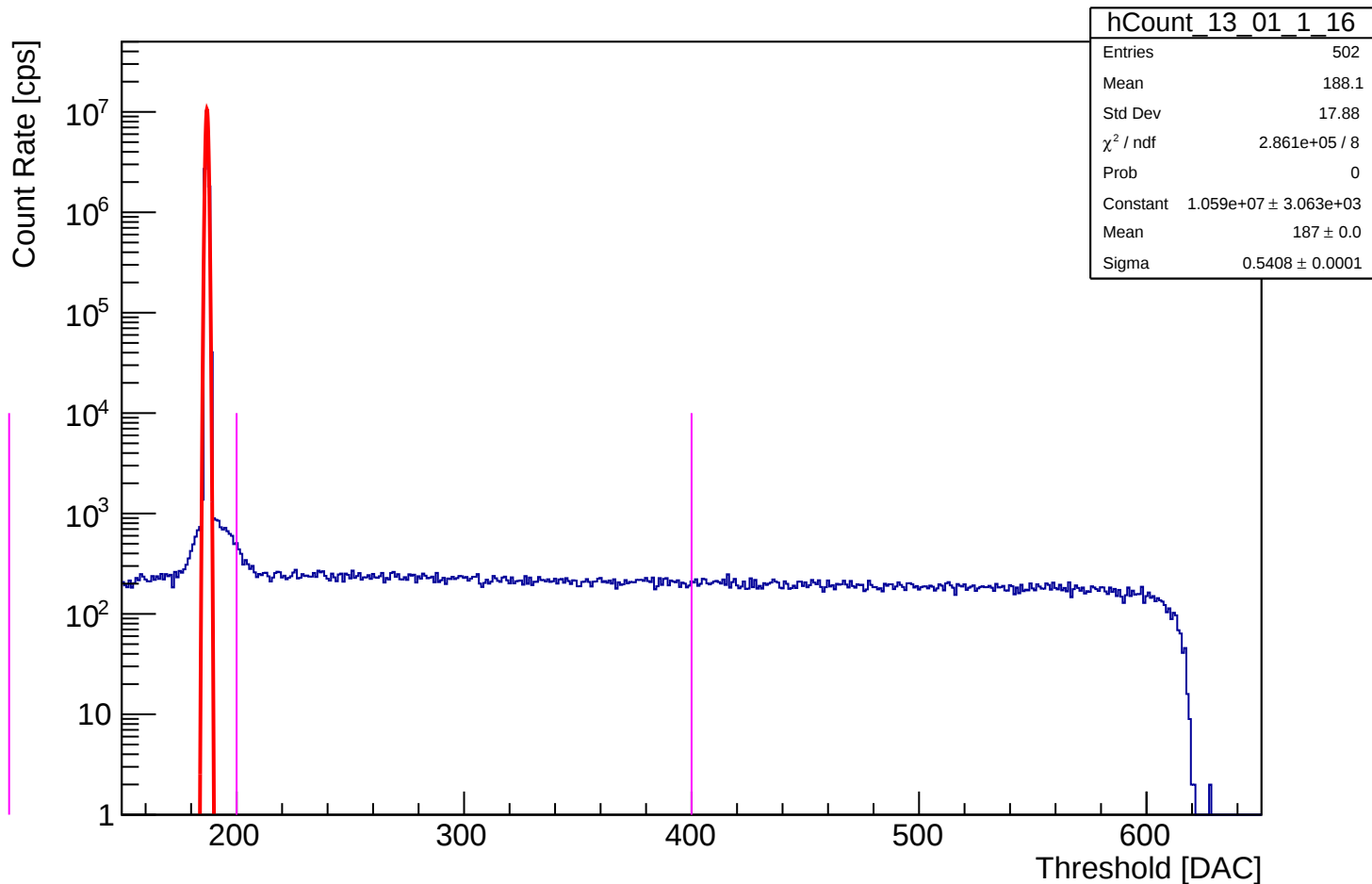
Row 1 Tile 1 Pmt 5 Pixel 26 Slot 13 Fiber 1 Asic 1 Channel 17



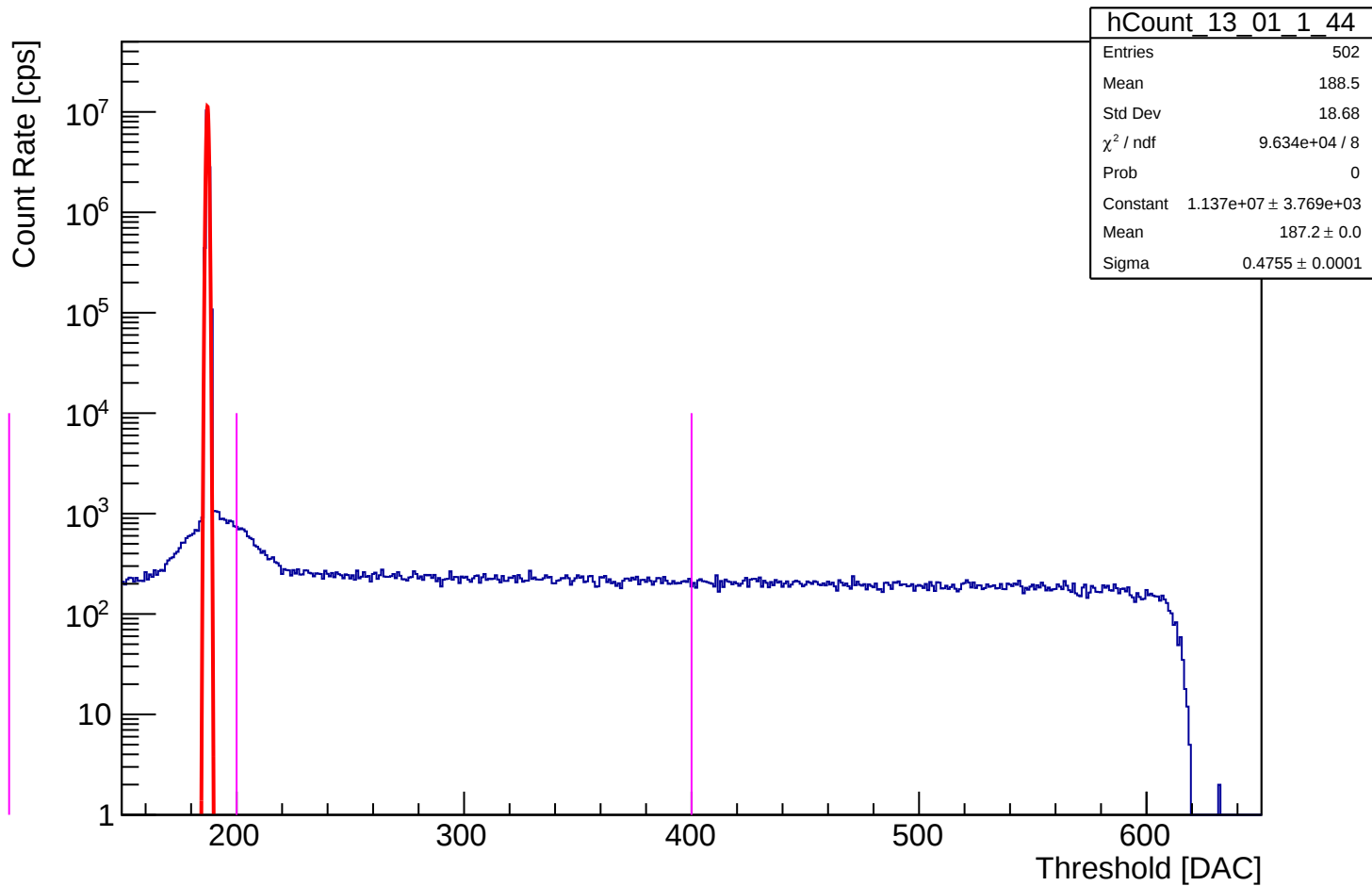
Row 1 Tile 1 Pmt 5 Pixel 27 Slot 13 Fiber 1 Asic 1 Channel 18



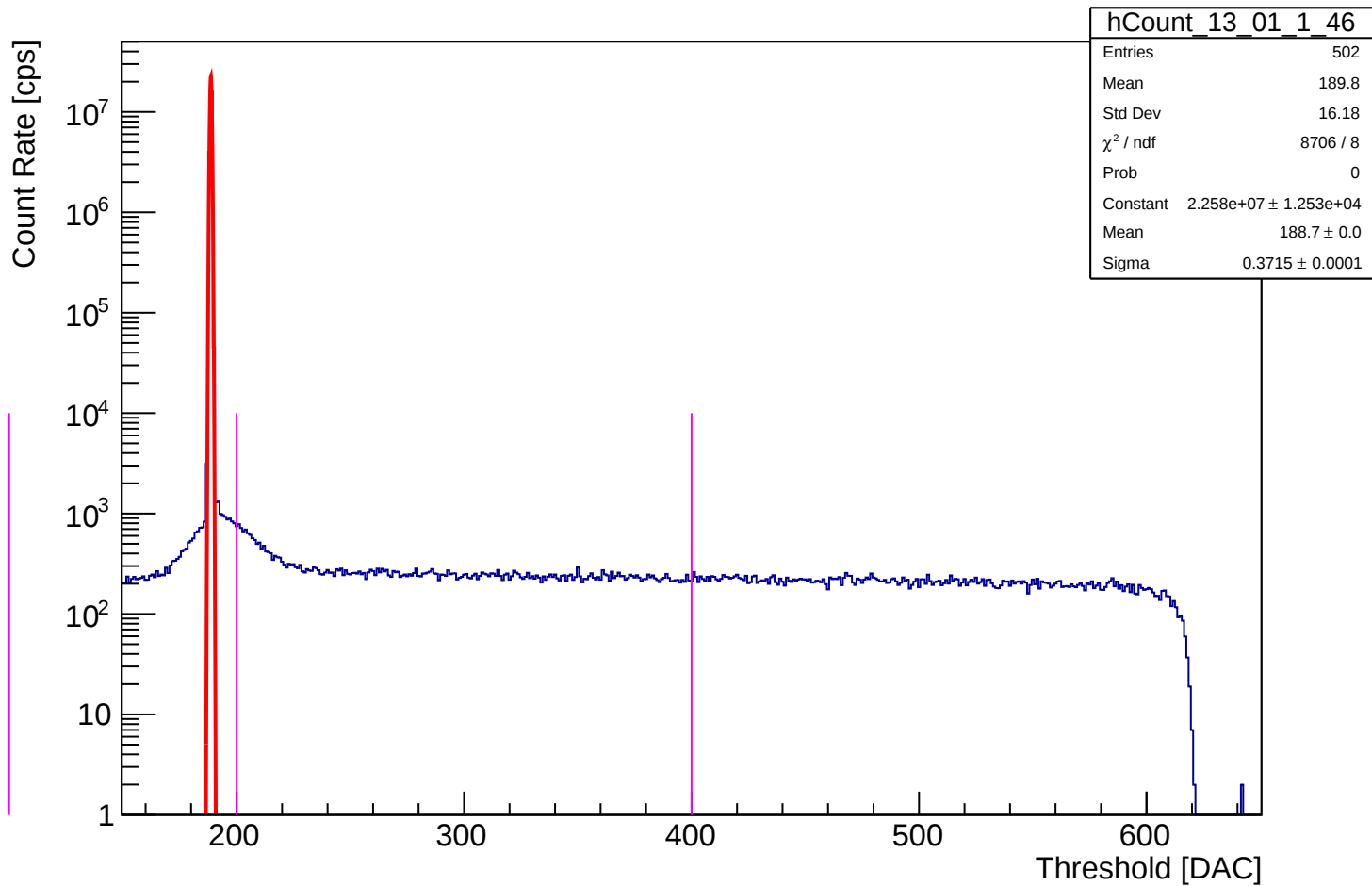
Row 1 Tile 1 Pmt 5 Pixel 28 Slot 13 Fiber 1 Asic 1 Channel 16



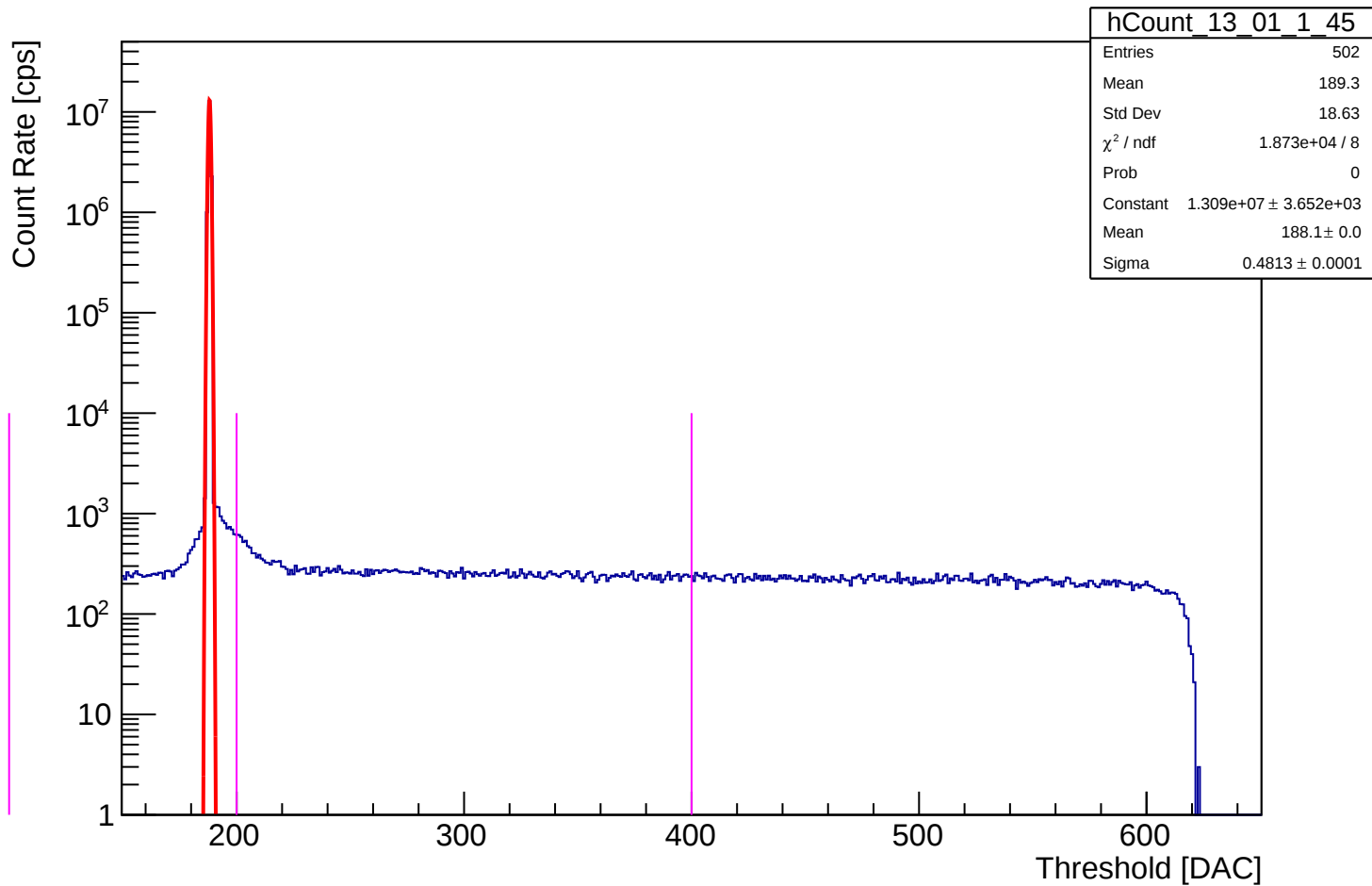
Row 1 Tile 1 Pmt 5 Pixel 29 Slot 13 Fiber 1 Asic 1 Channel 44



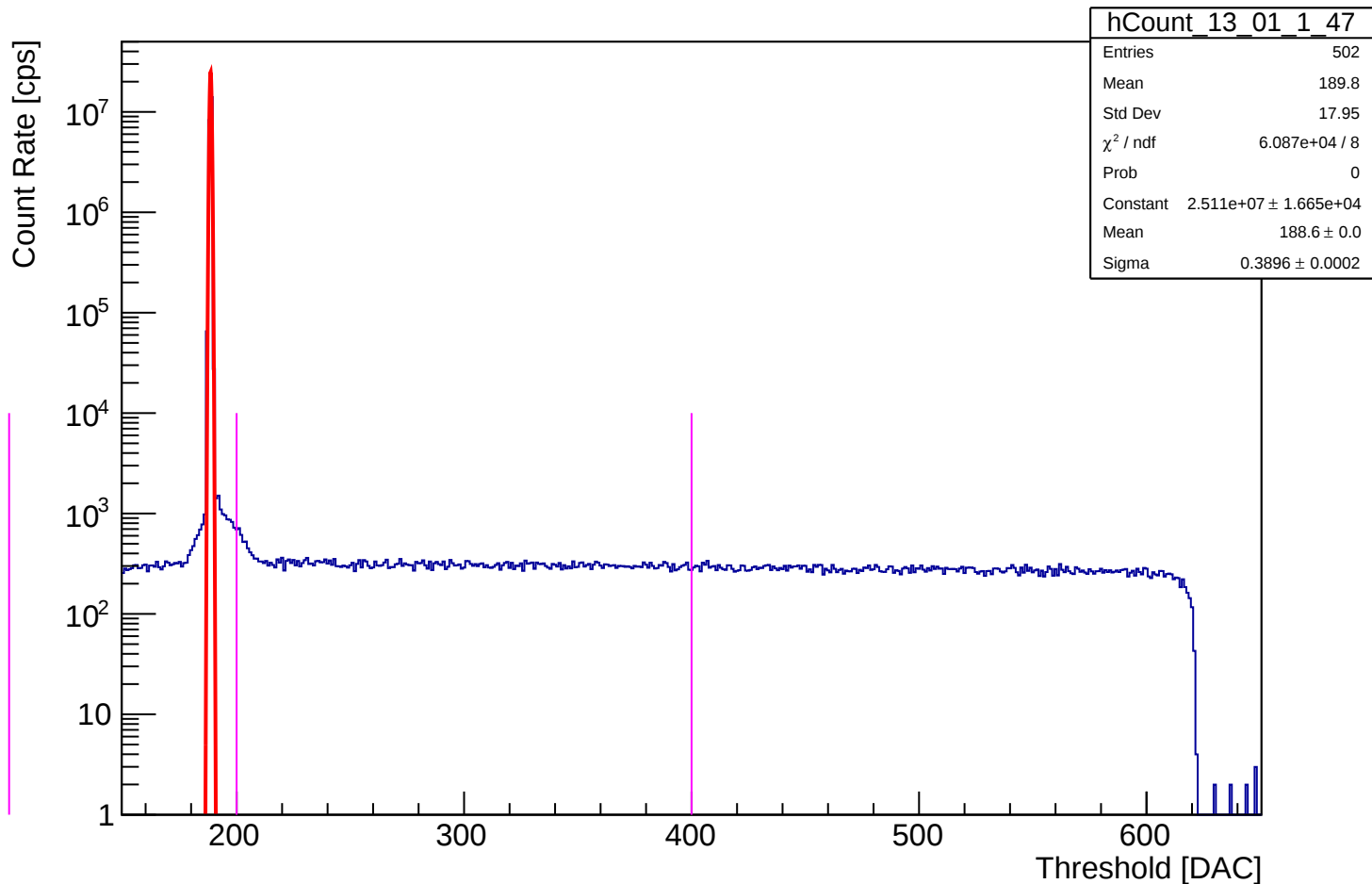
Row 1 Tile 1 Pmt 5 Pixel 30 Slot 13 Fiber 1 Asic 1 Channel 46



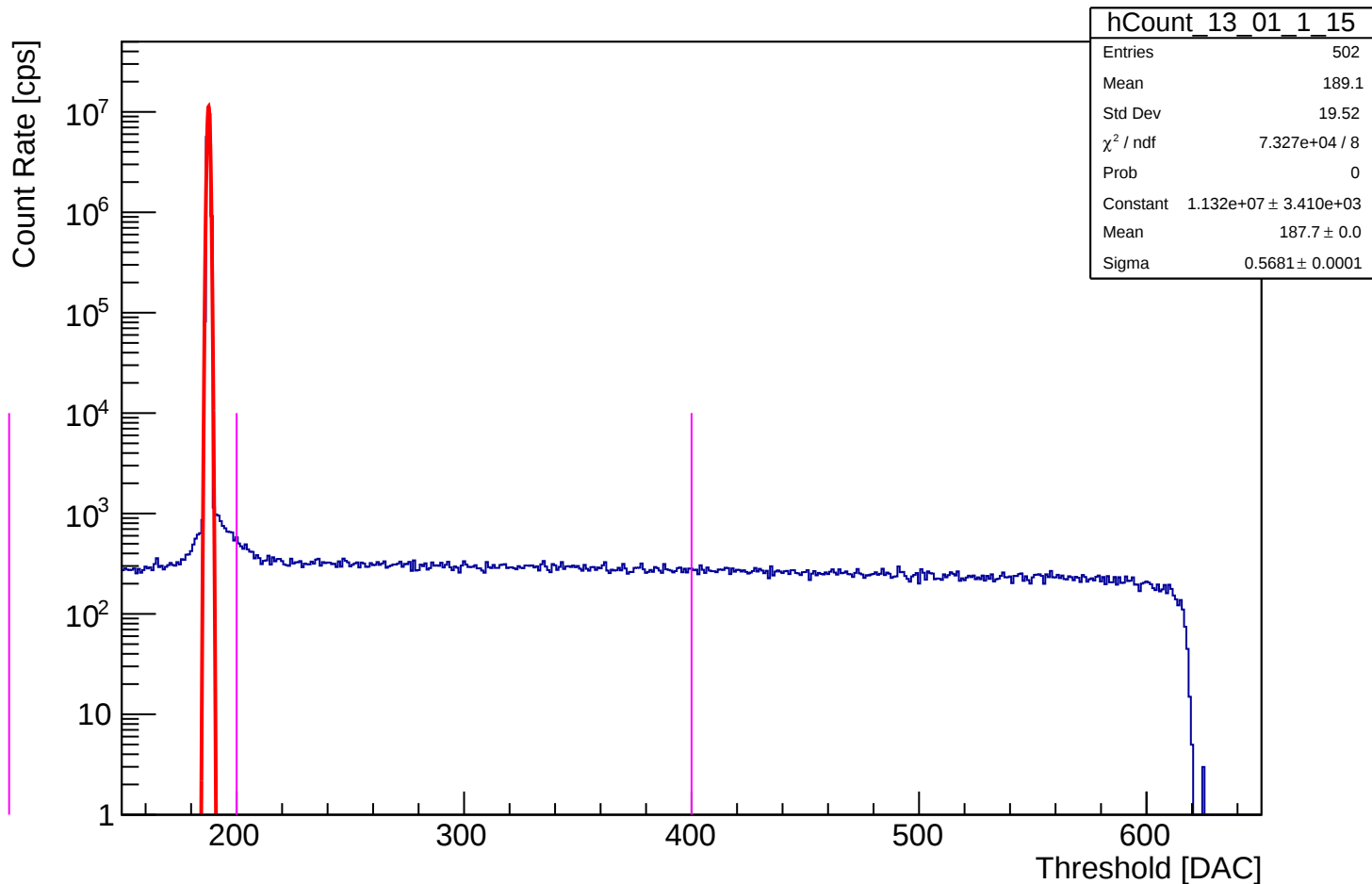
Row 1 Tile 1 Pmt 5 Pixel 31 Slot 13 Fiber 1 Asic 1 Channel 45



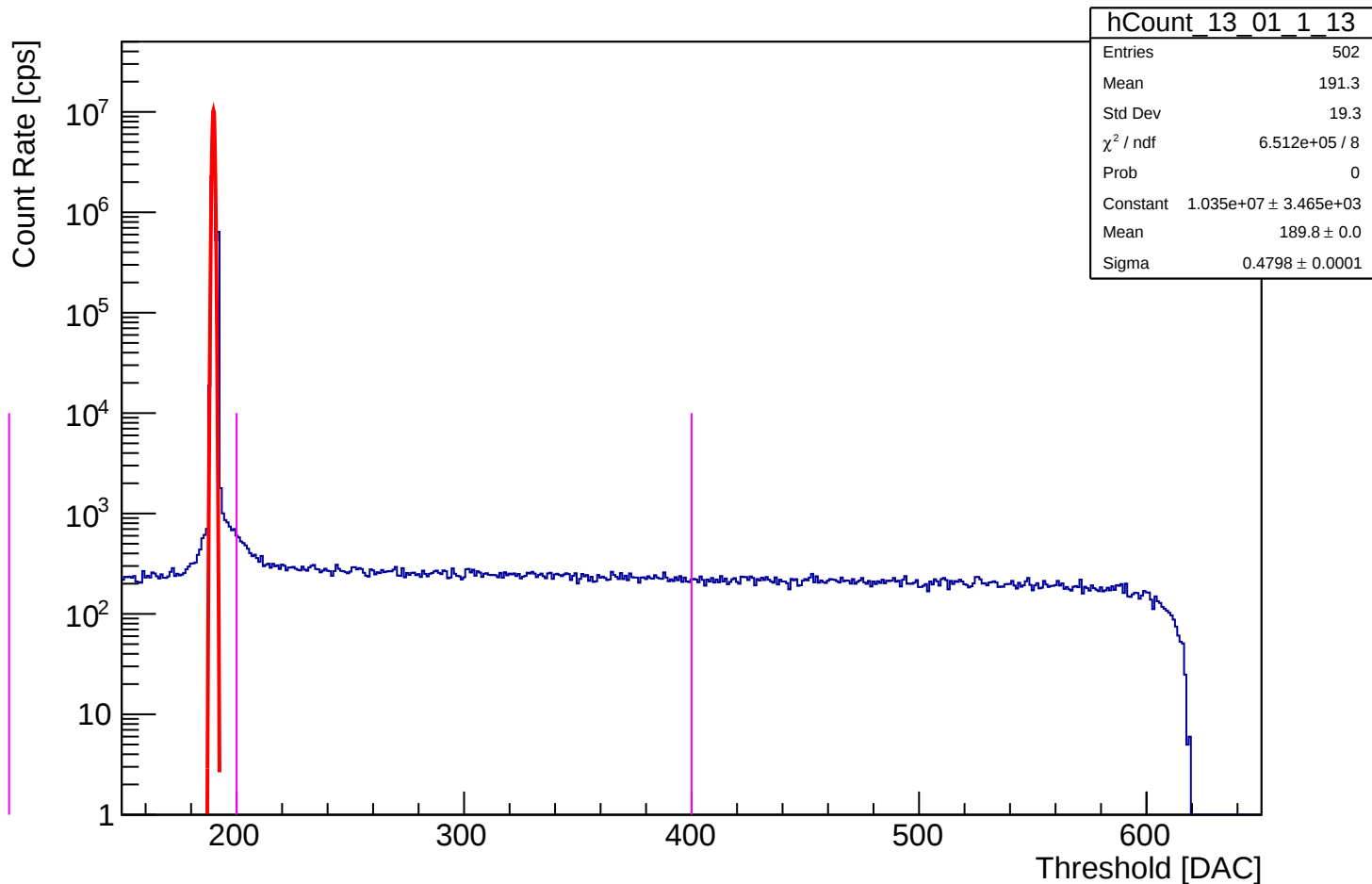
Row 1 Tile 1 Pmt 5 Pixel 32 Slot 13 Fiber 1 Asic 1 Channel 47



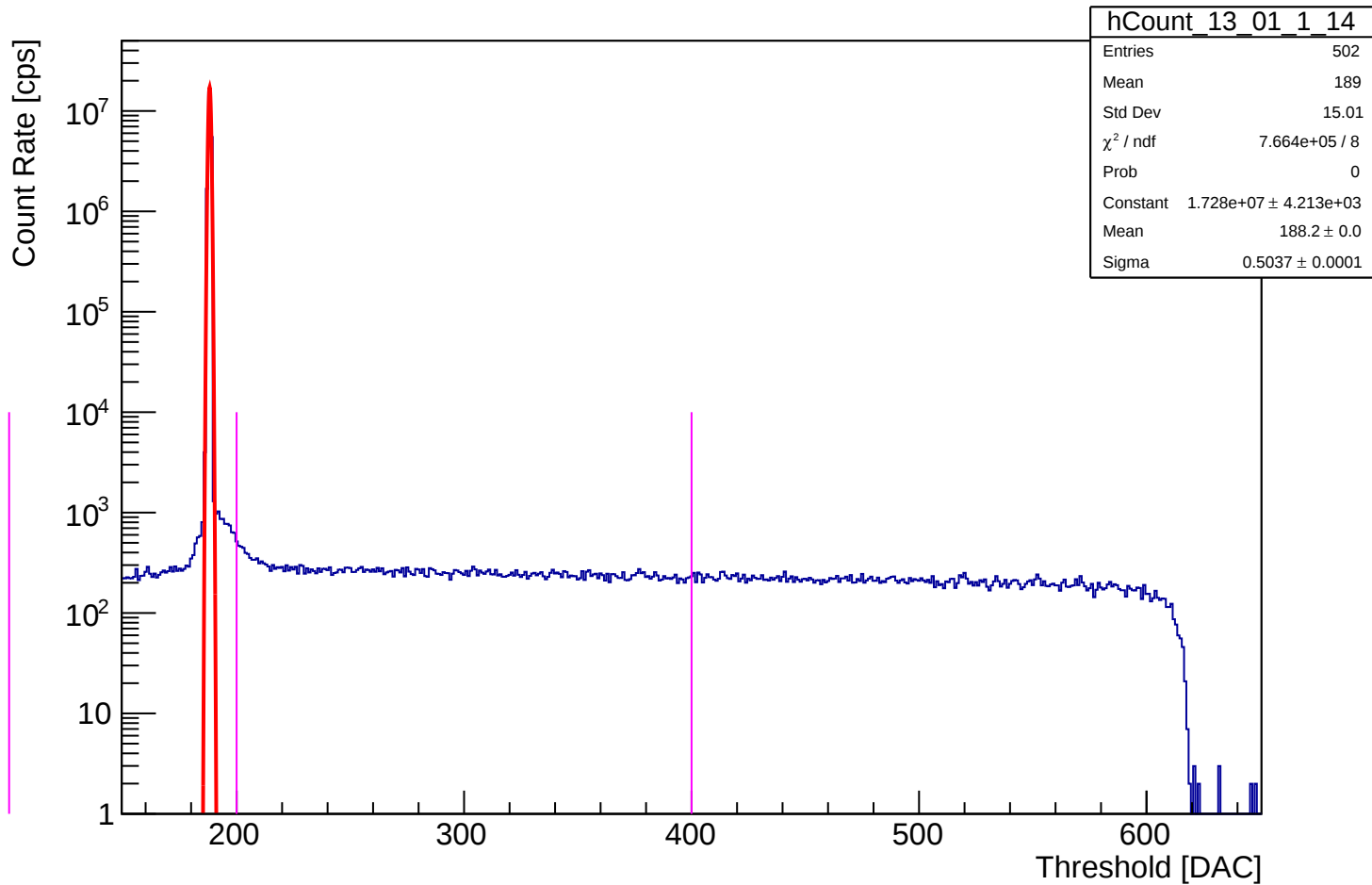
Row 1 Tile 1 Pmt 5 Pixel 33 Slot 13 Fiber 1 Asic 1 Channel 15



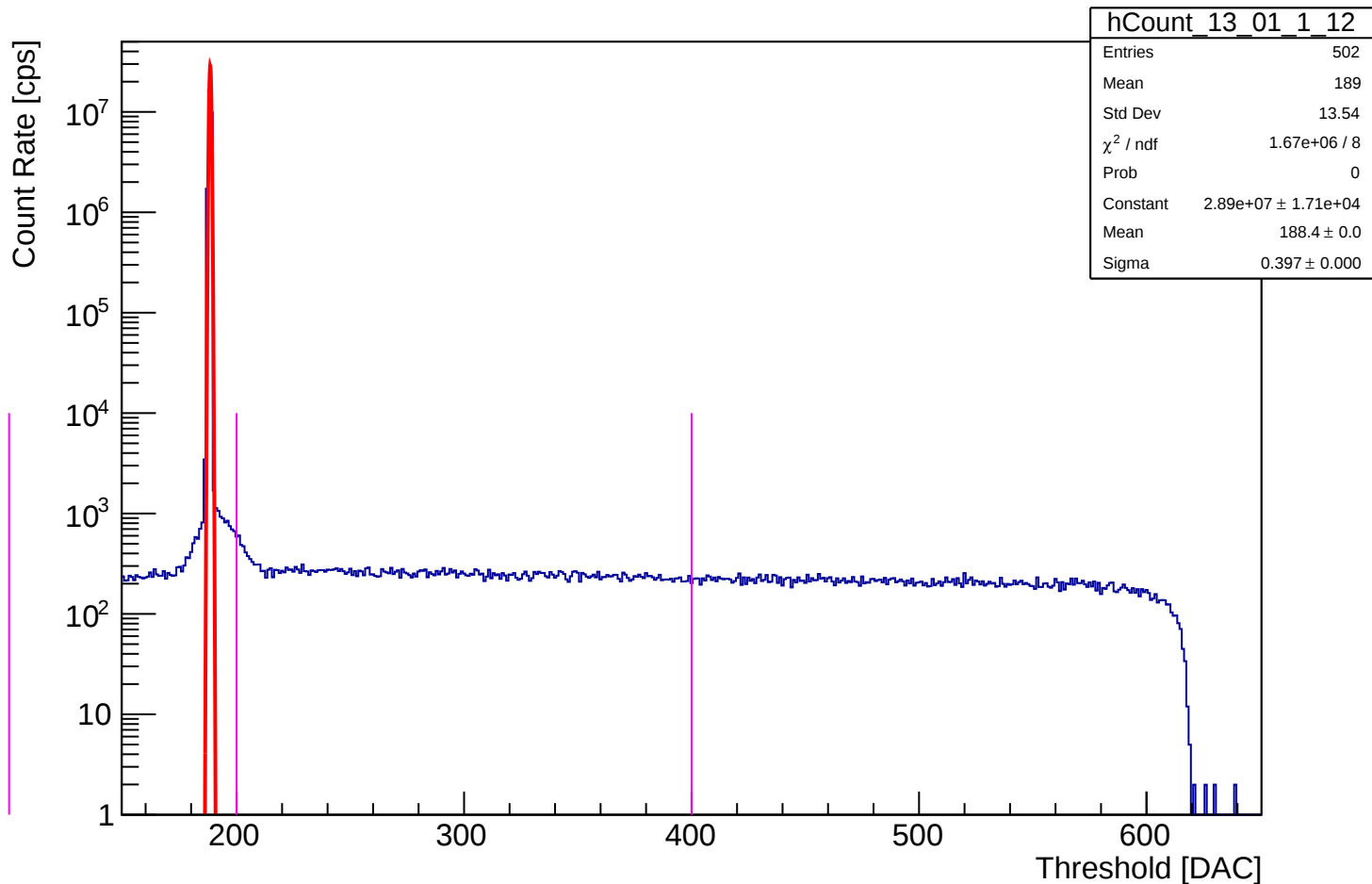
Row 1 Tile 1 Pmt 5 Pixel 34 Slot 13 Fiber 1 Asic 1 Channel 13



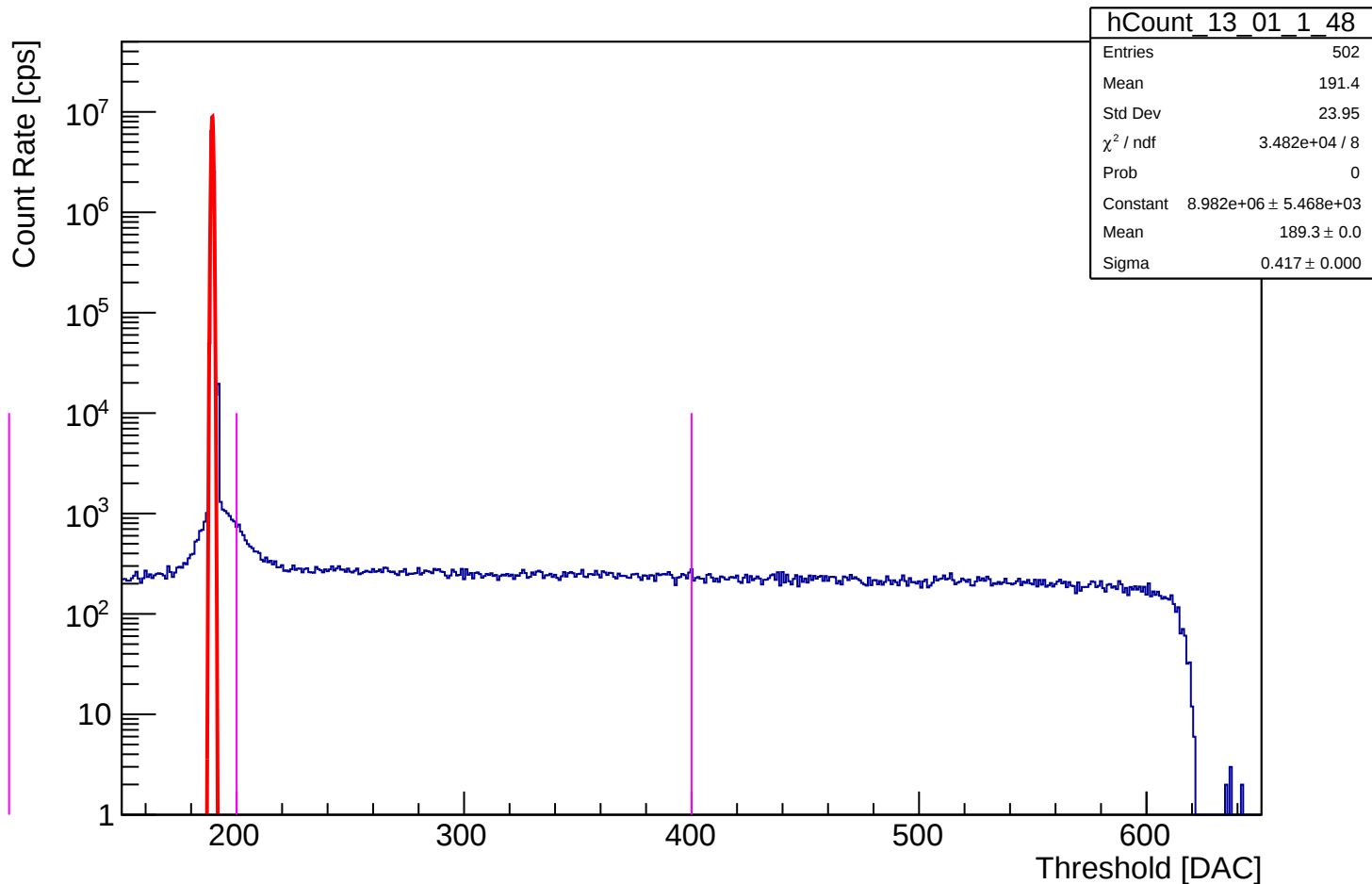
Row 1 Tile 1 Pmt 5 Pixel 35 Slot 13 Fiber 1 Asic 1 Channel 14



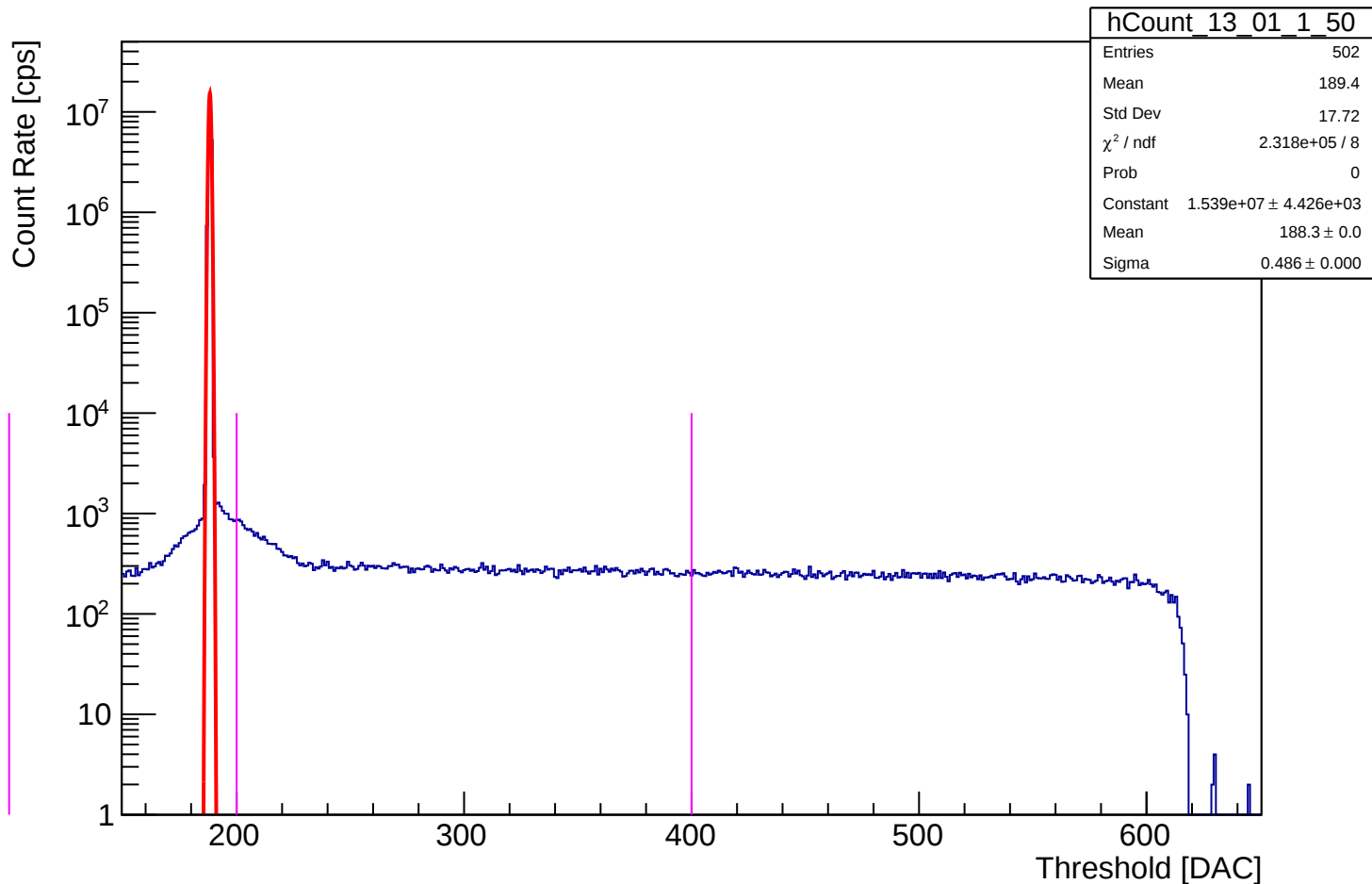
Row 1 Tile 1 Pmt 5 Pixel 36 Slot 13 Fiber 1 Asic 1 Channel 12



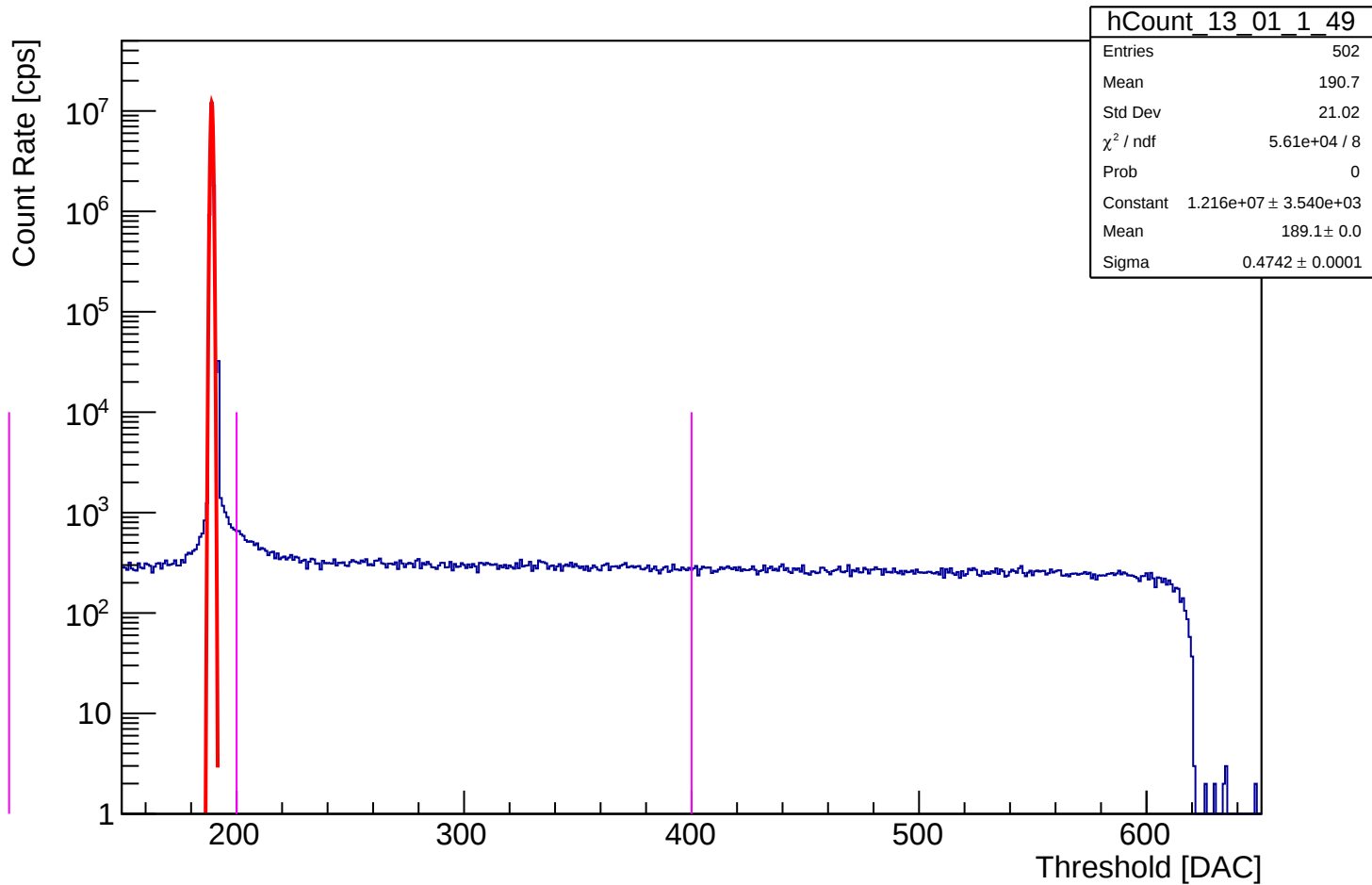
Row 1 Tile 1 Pmt 5 Pixel 37 Slot 13 Fiber 1 Asic 1 Channel 48



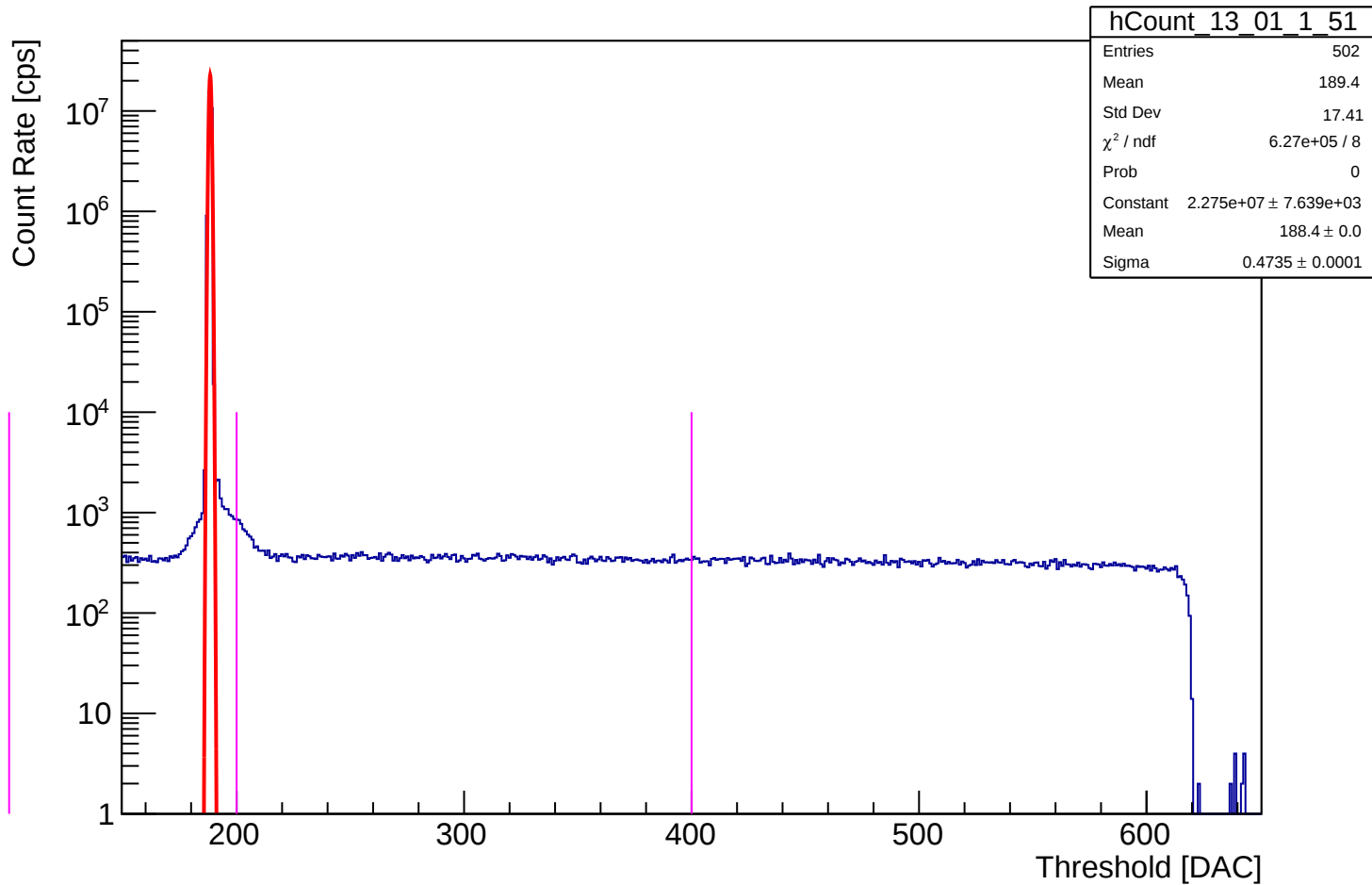
Row 1 Tile 1 Pmt 5 Pixel 38 Slot 13 Fiber 1 Asic 1 Channel 50



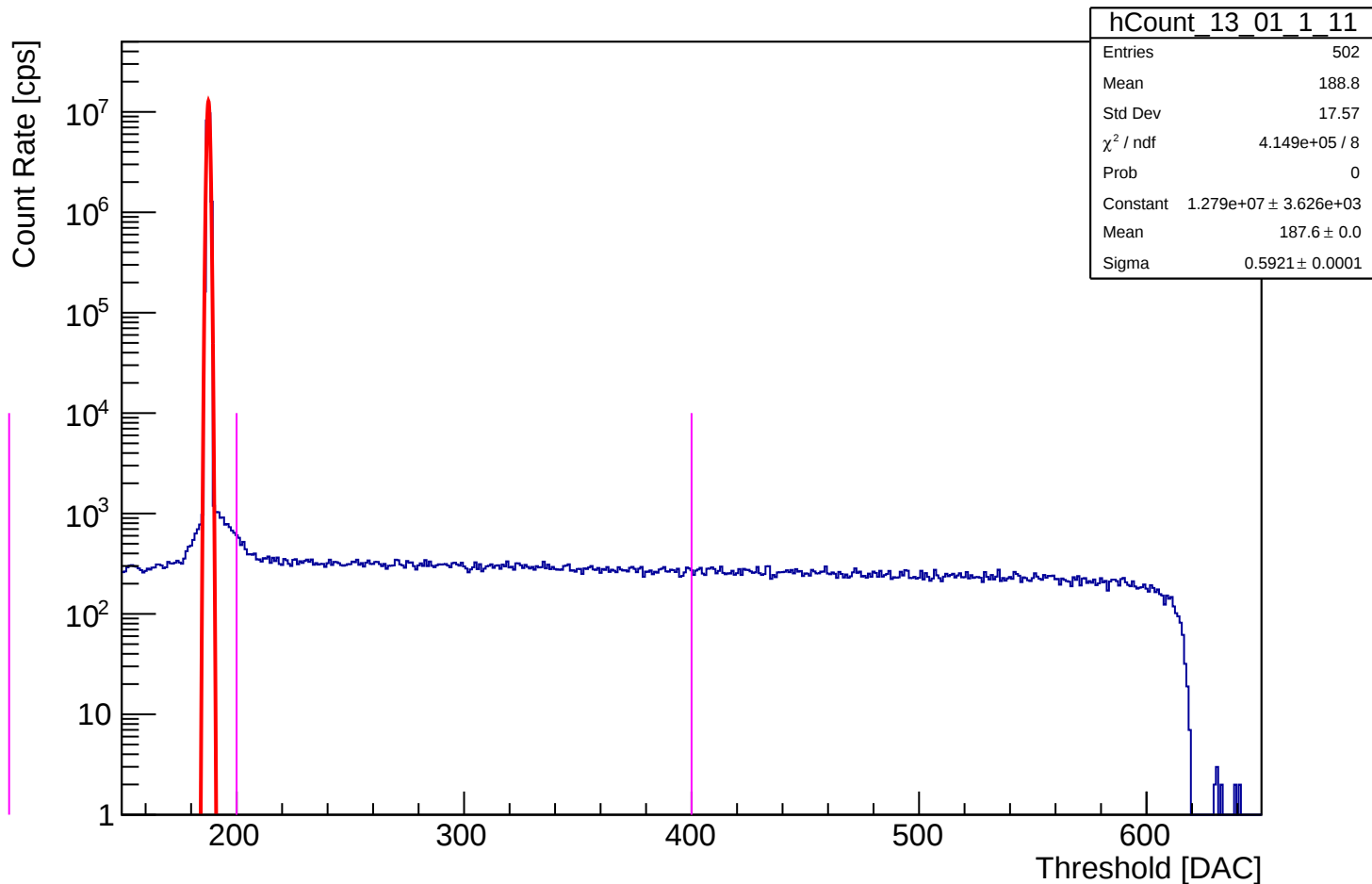
Row 1 Tile 1 Pmt 5 Pixel 39 Slot 13 Fiber 1 Asic 1 Channel 49

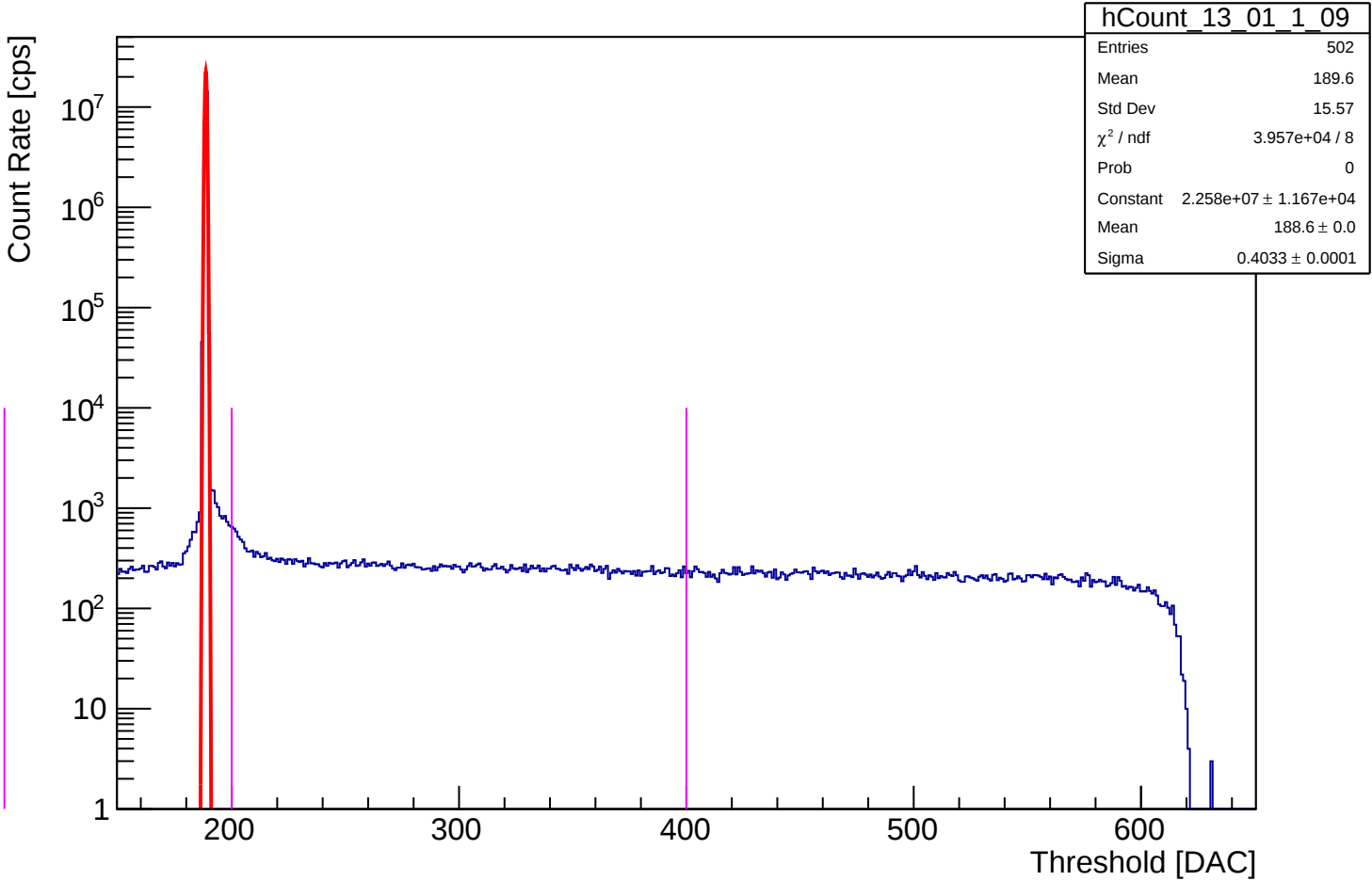


Row 1 Tile 1 Pmt 5 Pixel 40 Slot 13 Fiber 1 Asic 1 Channel 51

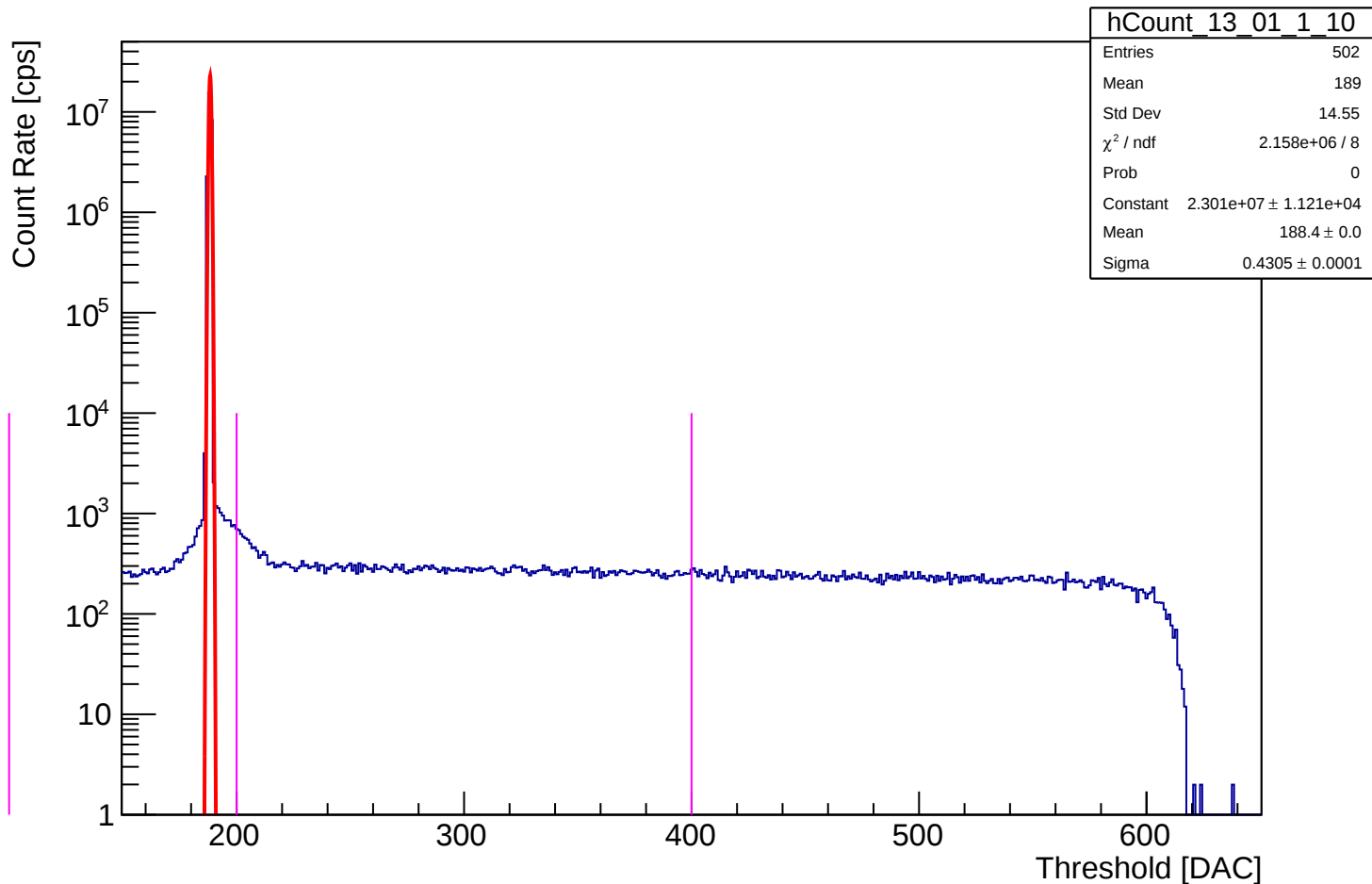


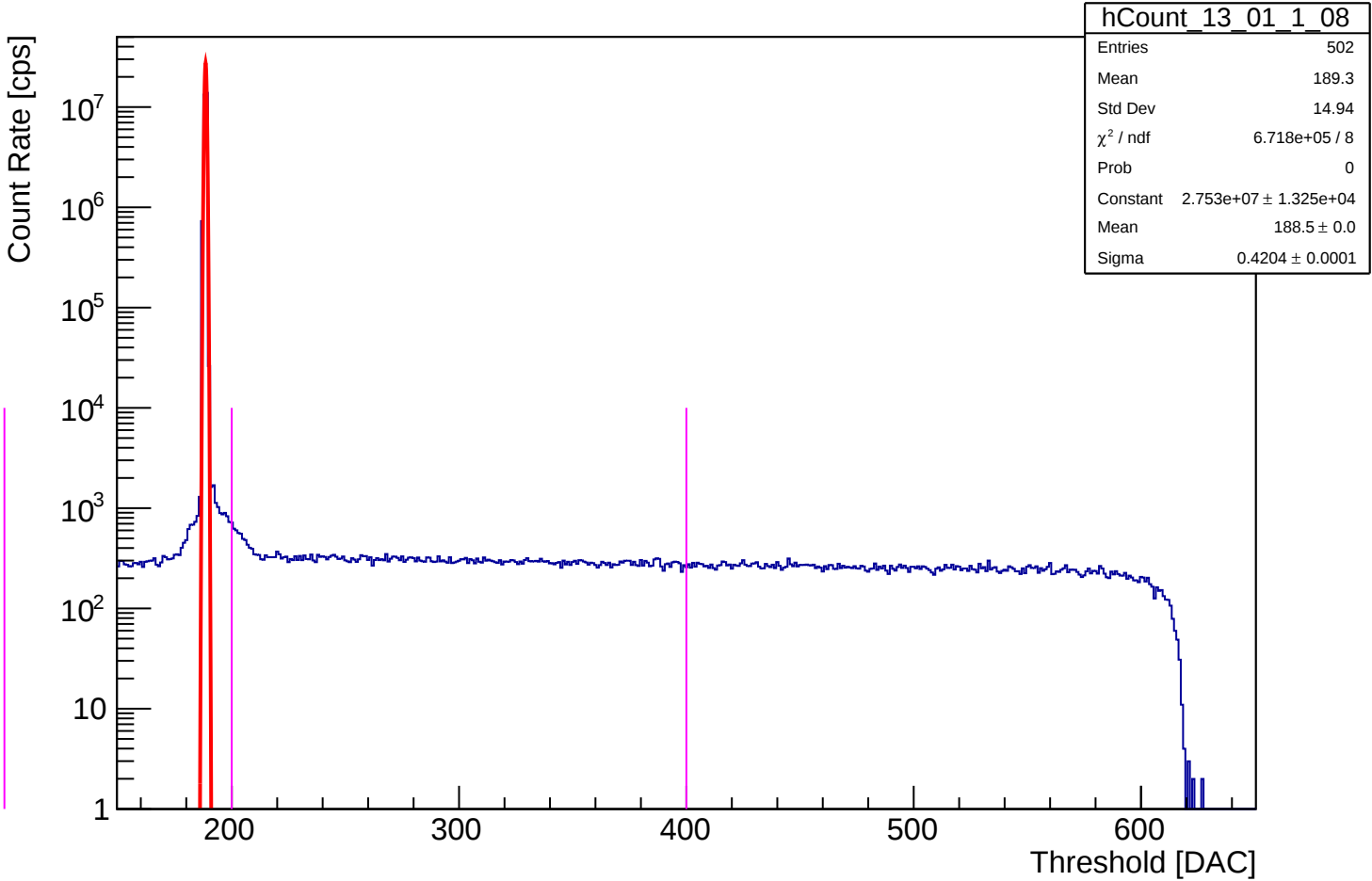
Row 1 Tile 1 Pmt 5 Pixel 41 Slot 13 Fiber 1 Asic 1 Channel 11



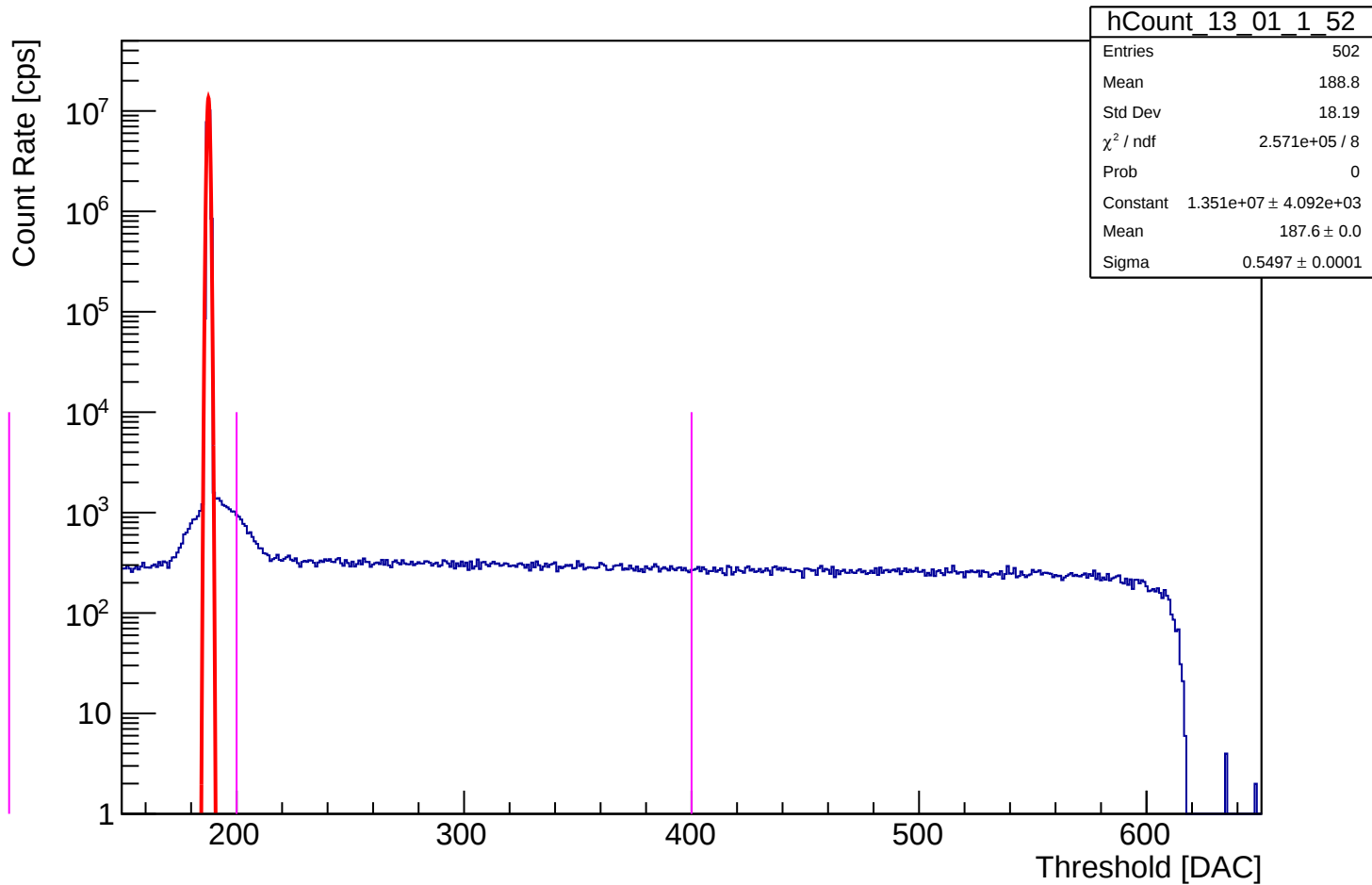


Row 1 Tile 1 Pmt 5 Pixel 43 Slot 13 Fiber 1 Asic 1 Channel 10

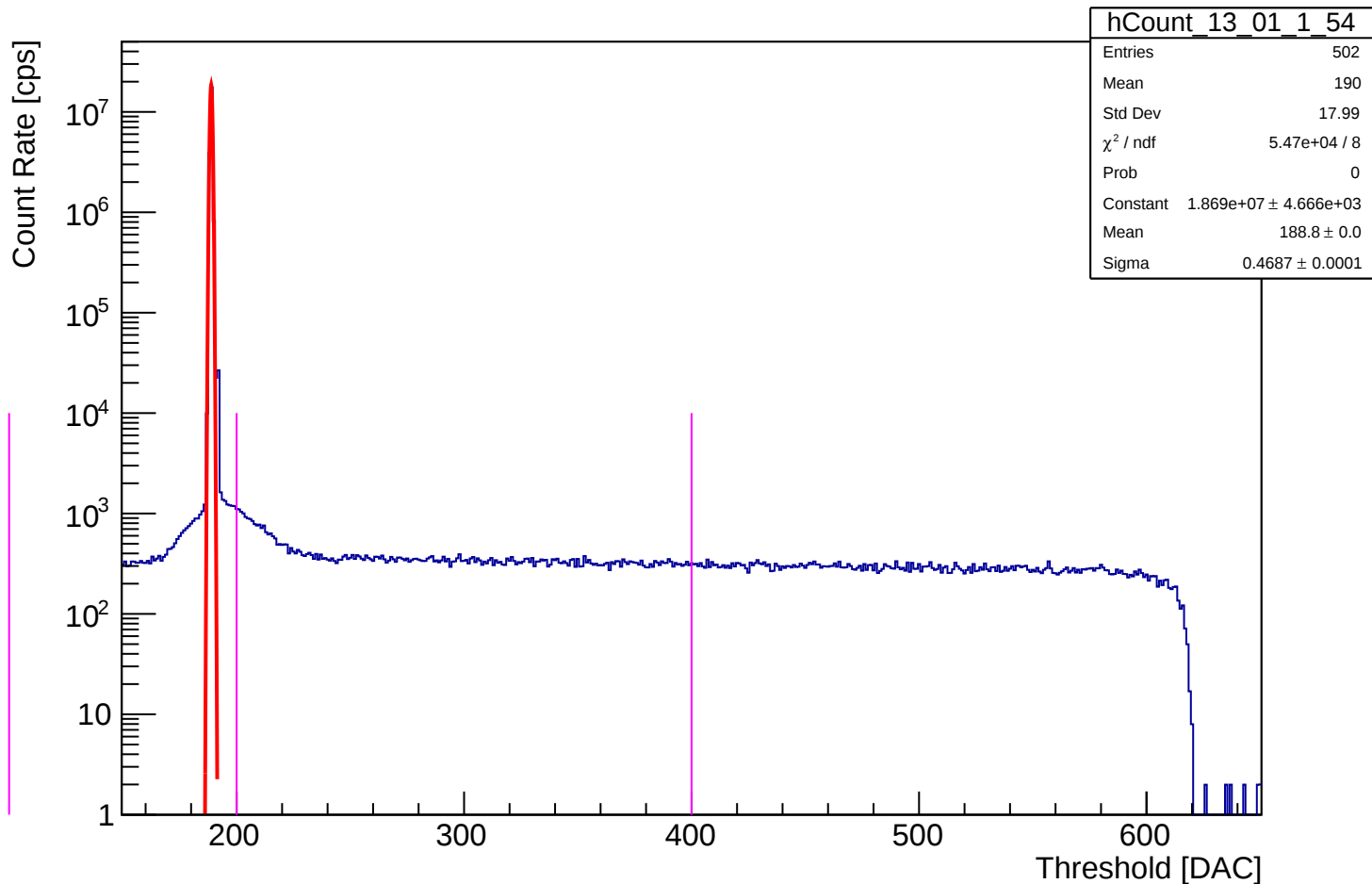




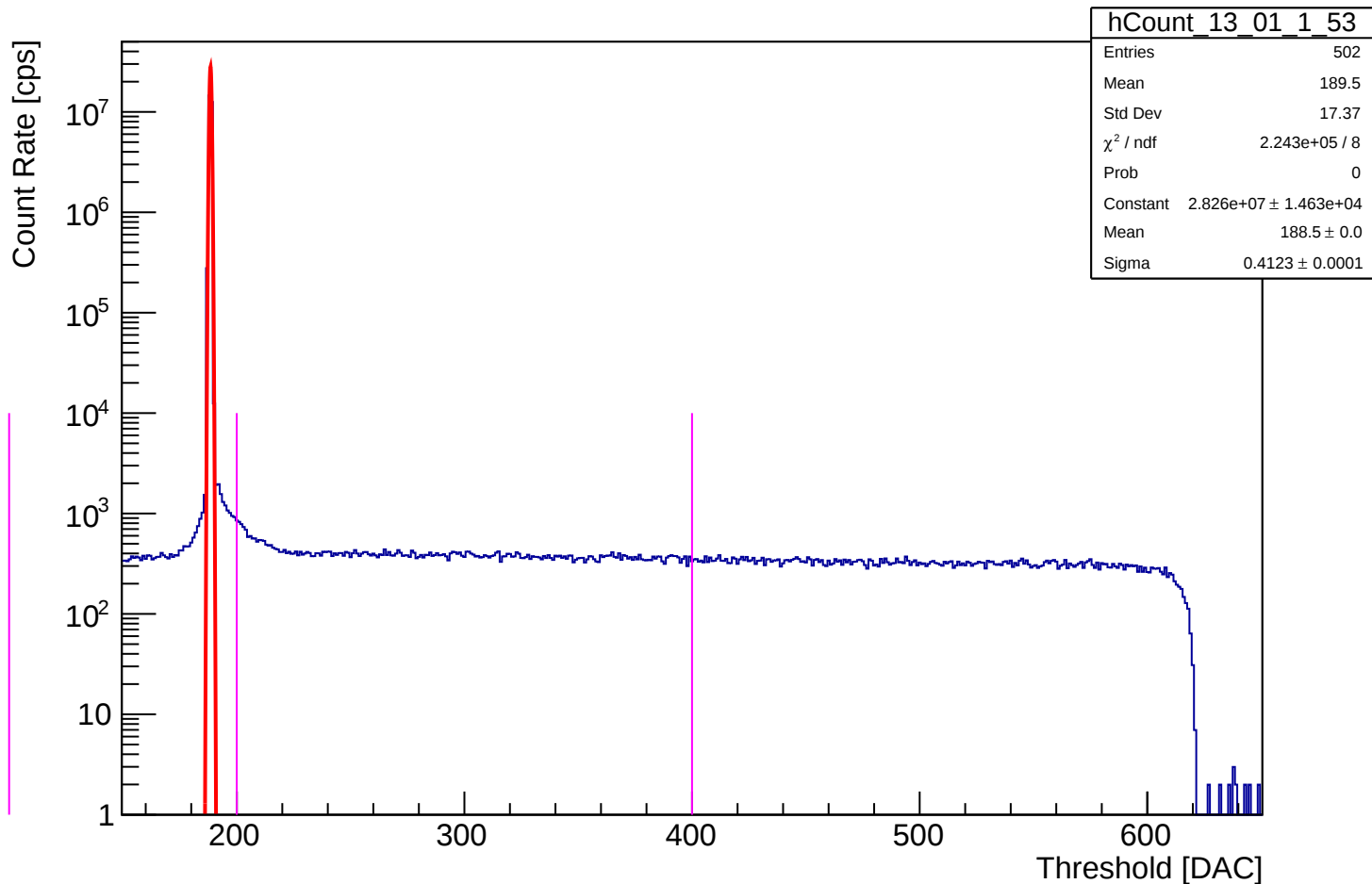
Row 1 Tile 1 Pmt 5 Pixel 45 Slot 13 Fiber 1 Asic 1 Channel 52



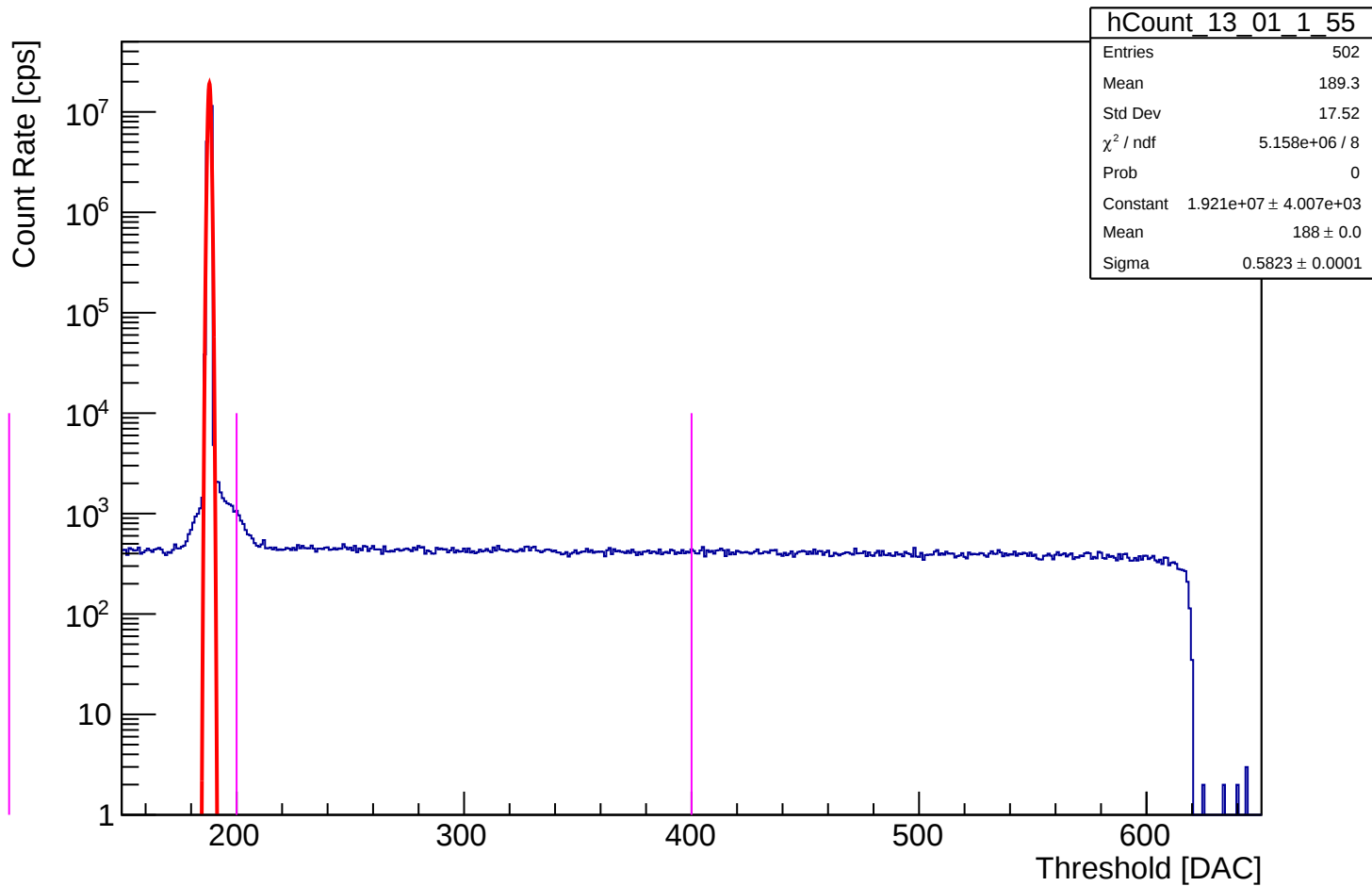
Row 1 Tile 1 Pmt 5 Pixel 46 Slot 13 Fiber 1 Asic 1 Channel 54

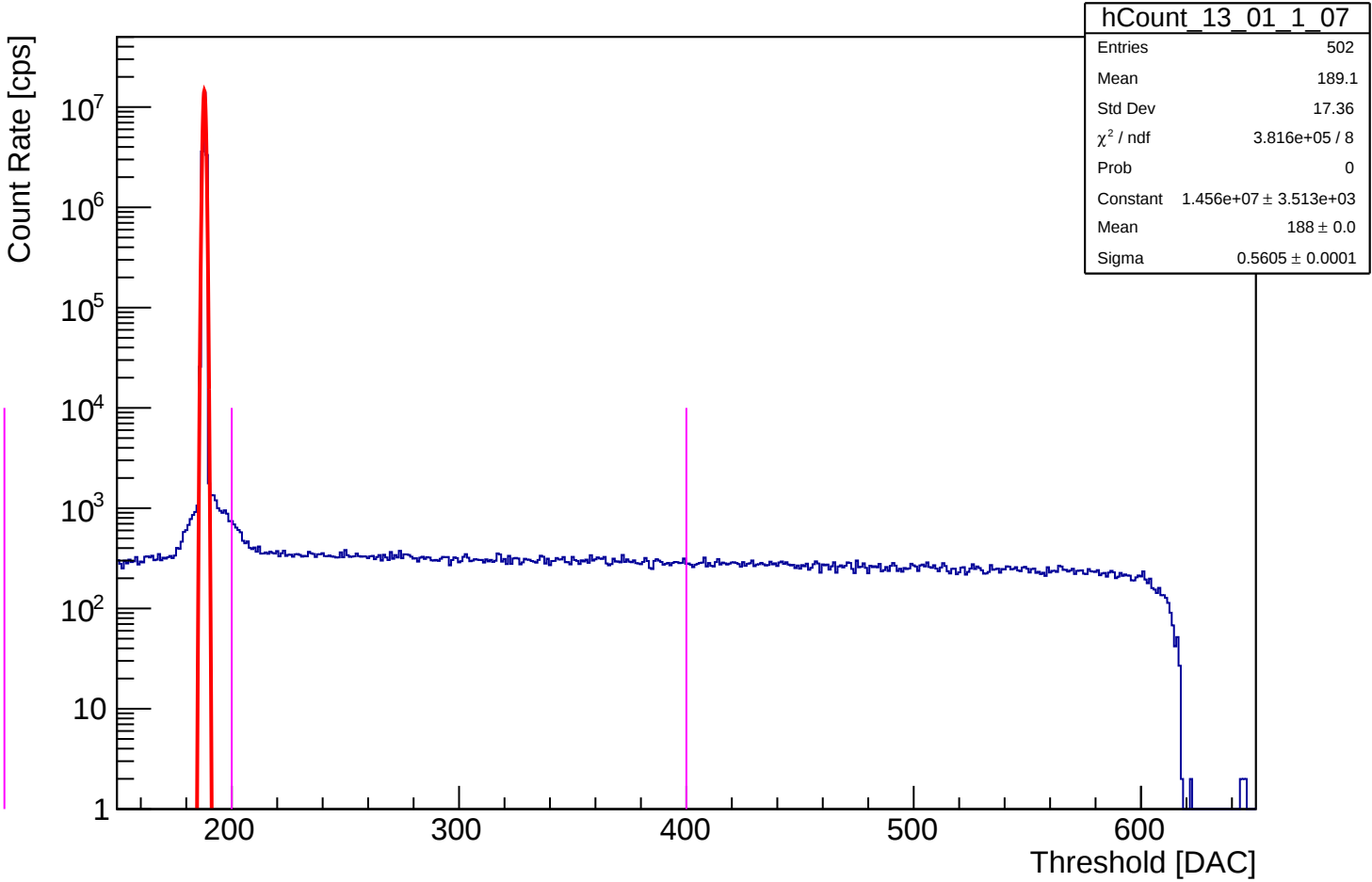


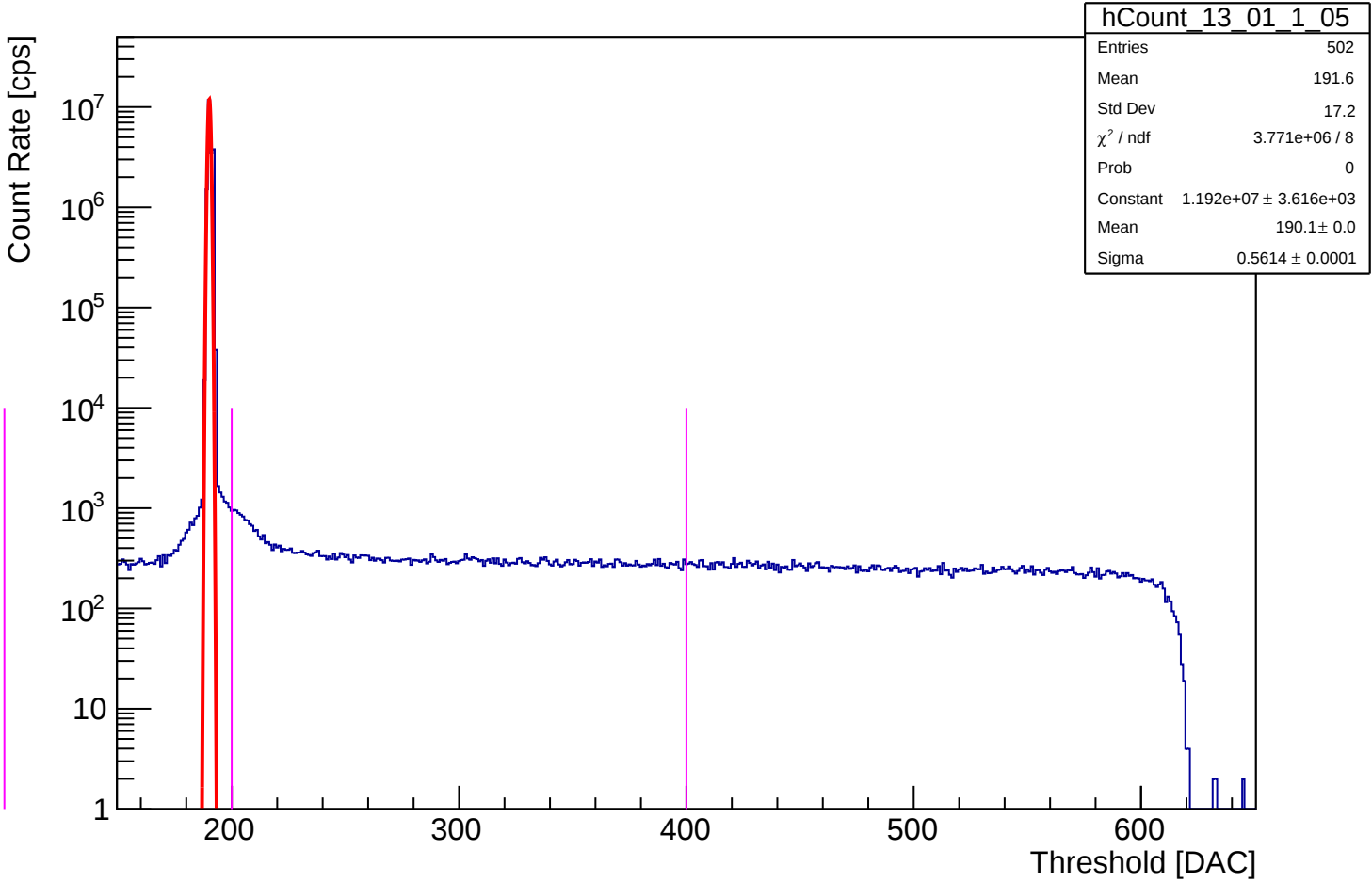
Row 1 Tile 1 Pmt 5 Pixel 47 Slot 13 Fiber 1 Asic 1 Channel 53



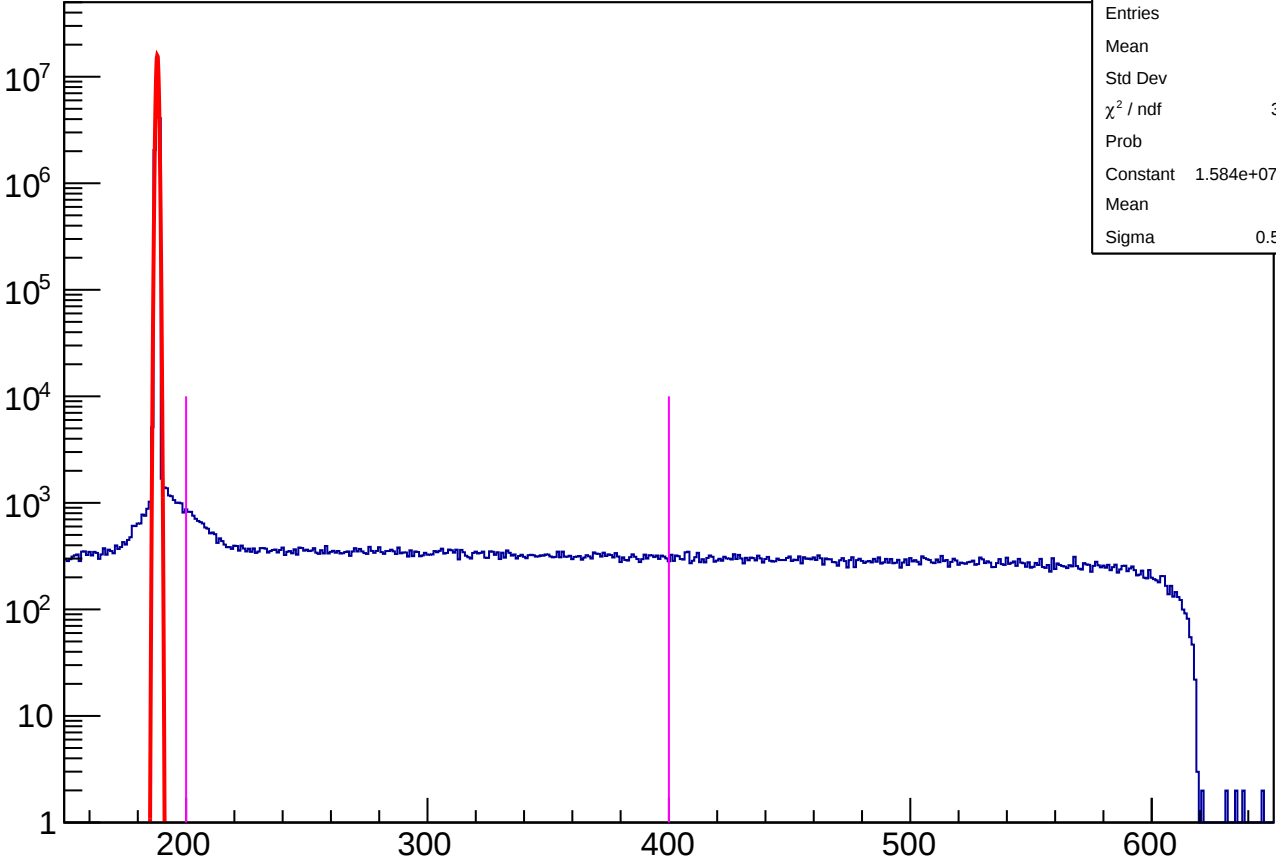
Row 1 Tile 1 Pmt 5 Pixel 48 Slot 13 Fiber 1 Asic 1 Channel 55







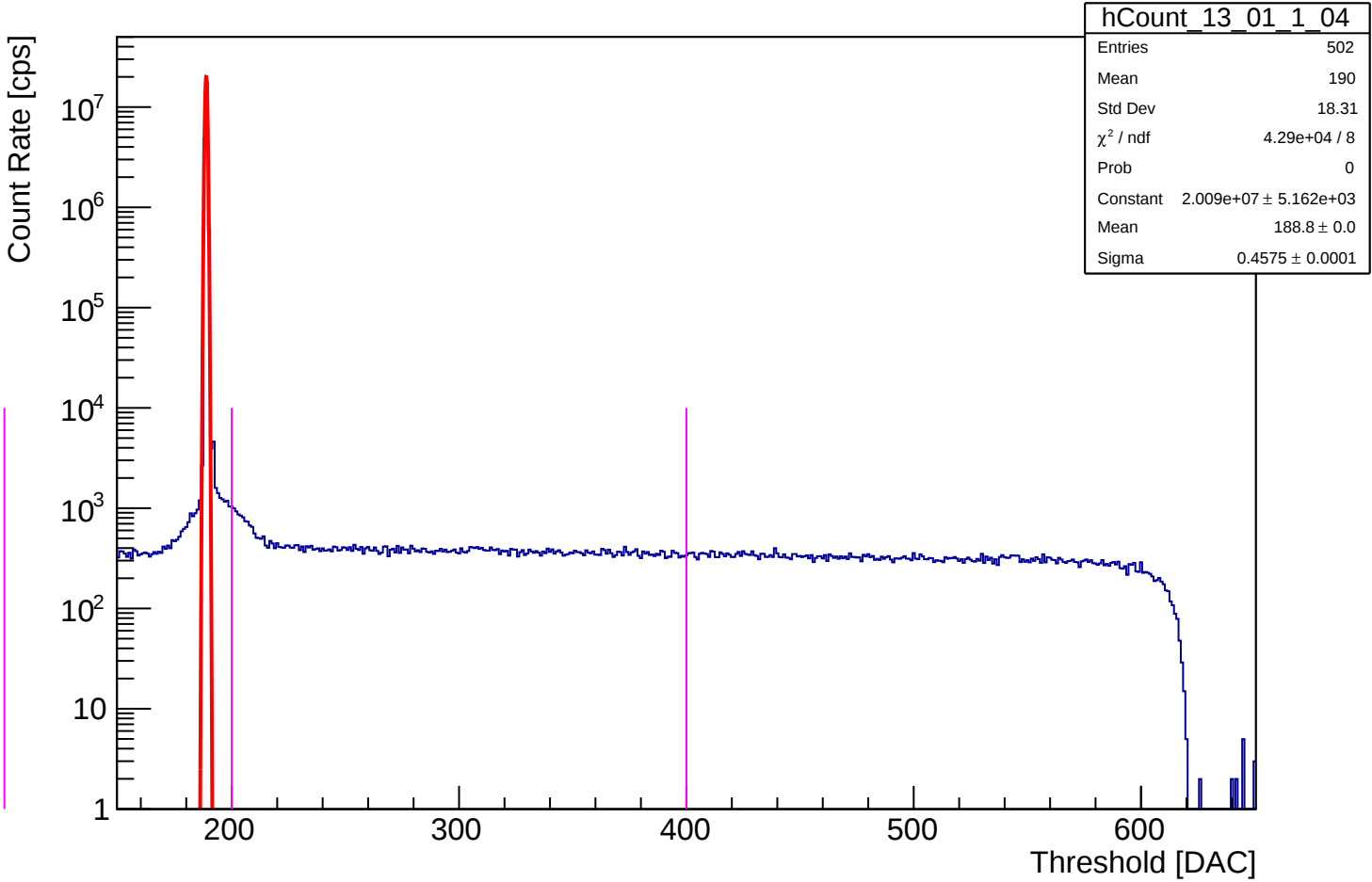
Count Rate [cps]



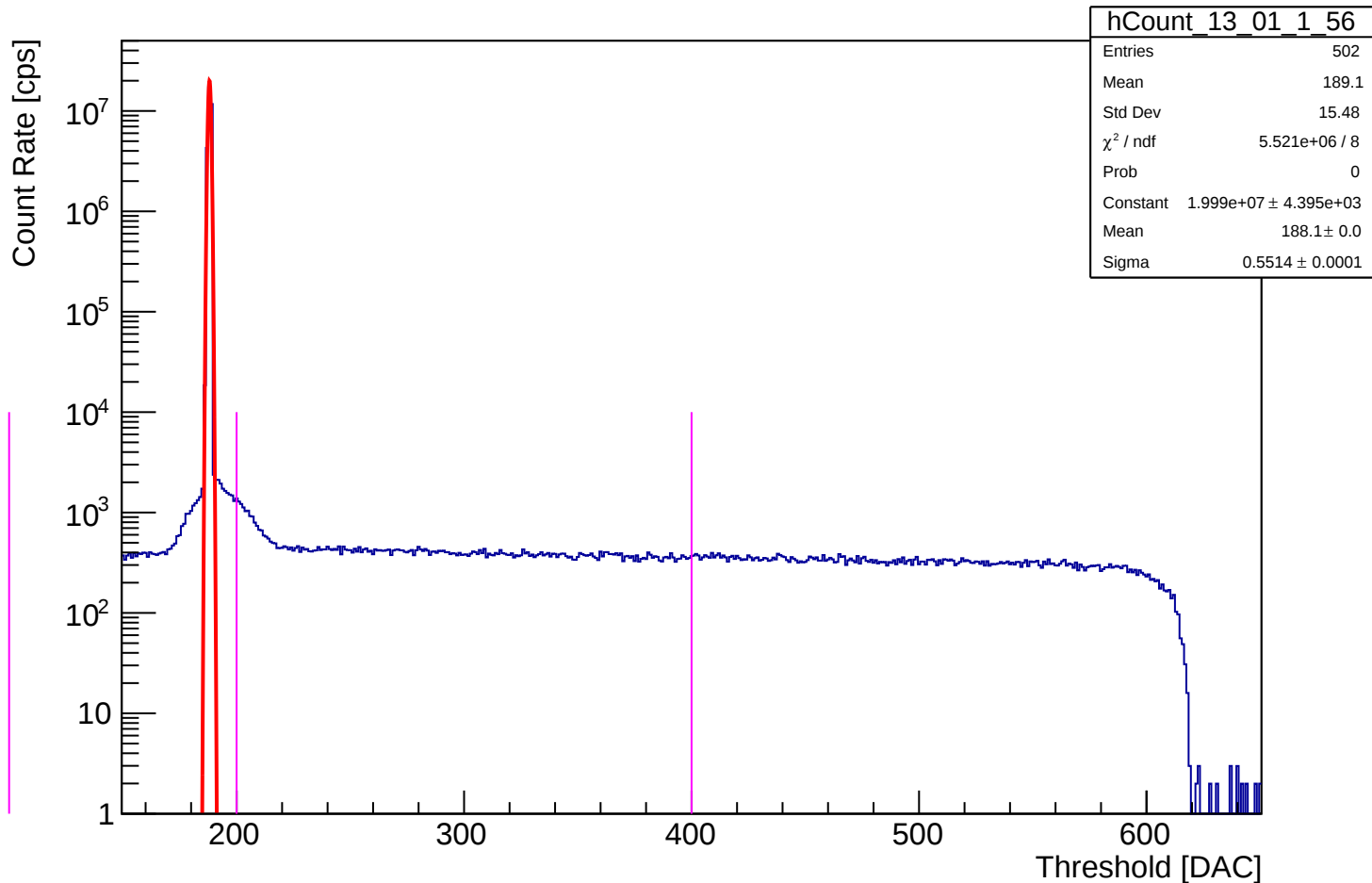
hCount_13_01_1_06

Entries	502
Mean	189.3
Std Dev	17.98
χ^2 / ndf	3.418e+05 / 8
Prob	0
Constant	1.584e+07 ± 3.810e+03
Mean	188.1 ± 0.0
Sigma	0.5221 ± 0.0001

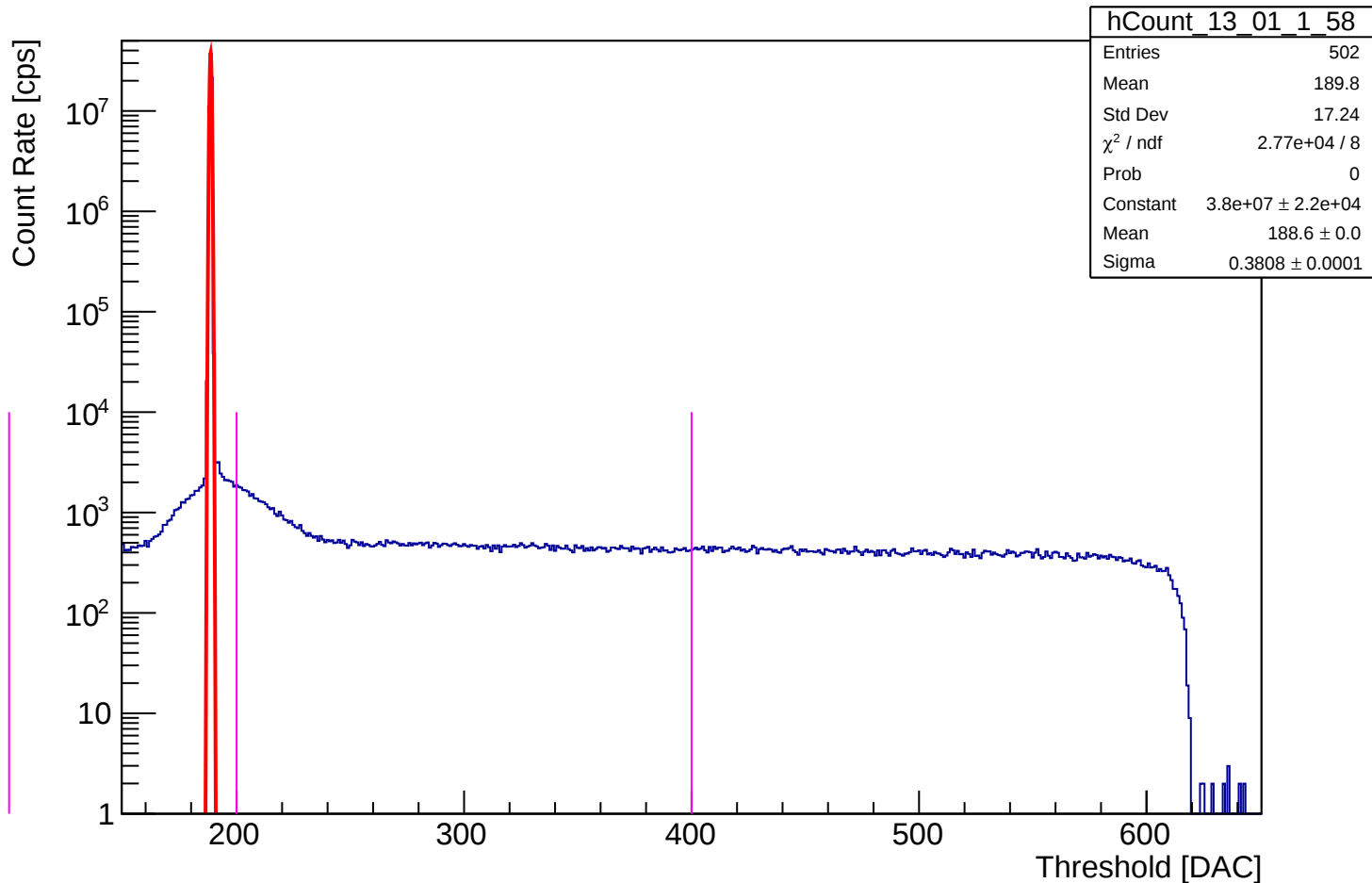
Threshold [DAC]



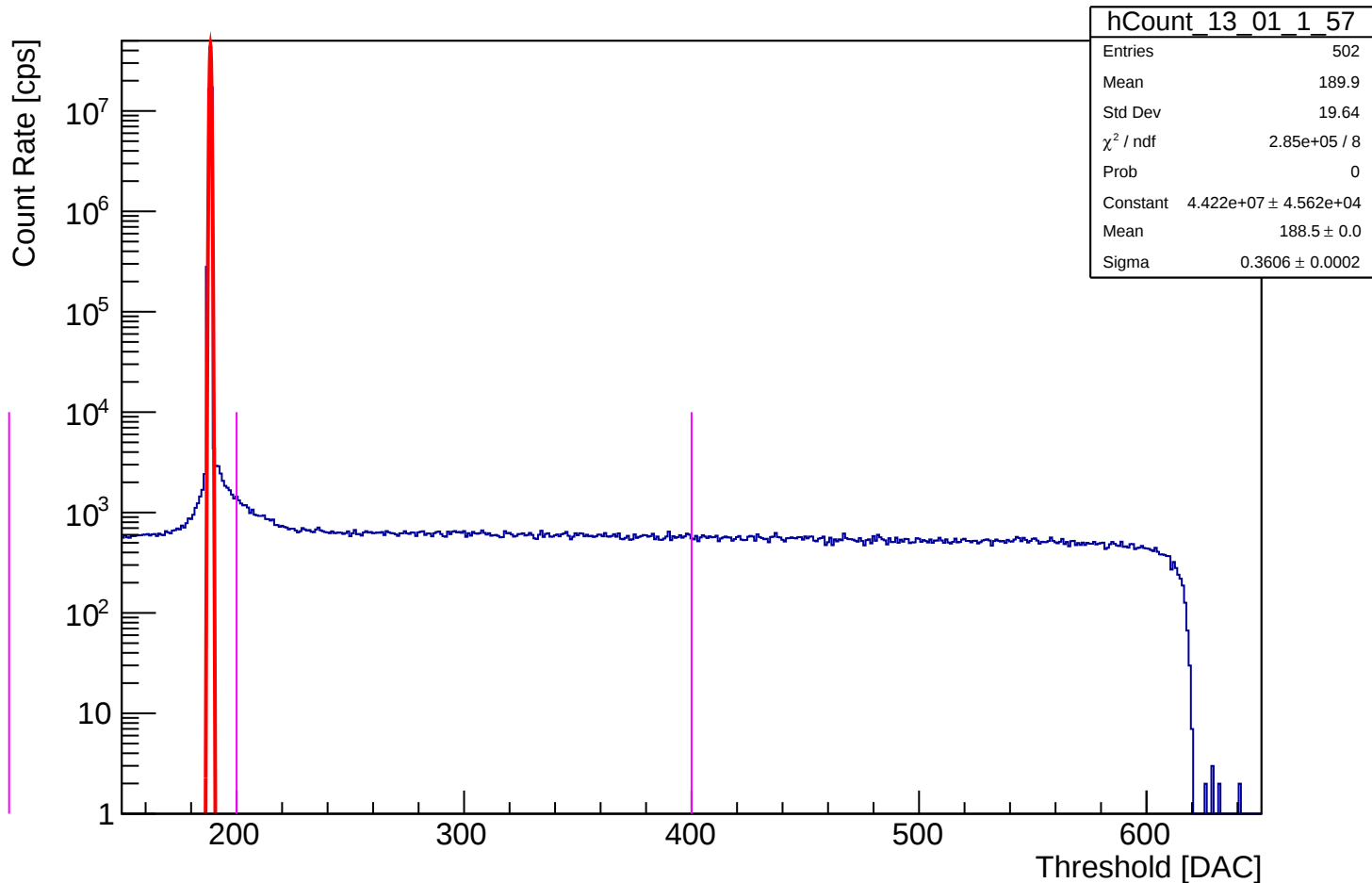
Row 1 Tile 1 Pmt 5 Pixel 53 Slot 13 Fiber 1 Asic 1 Channel 56

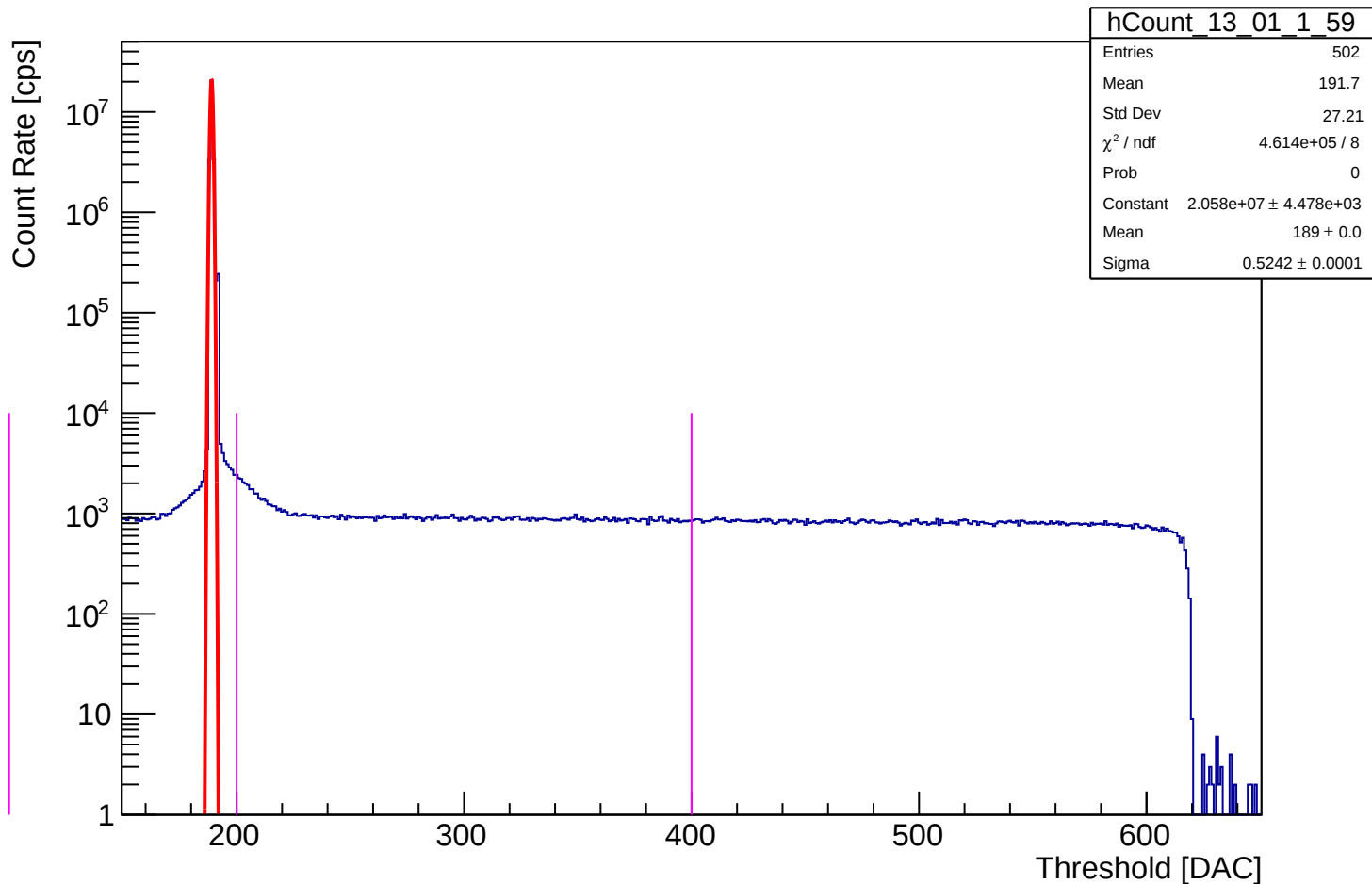


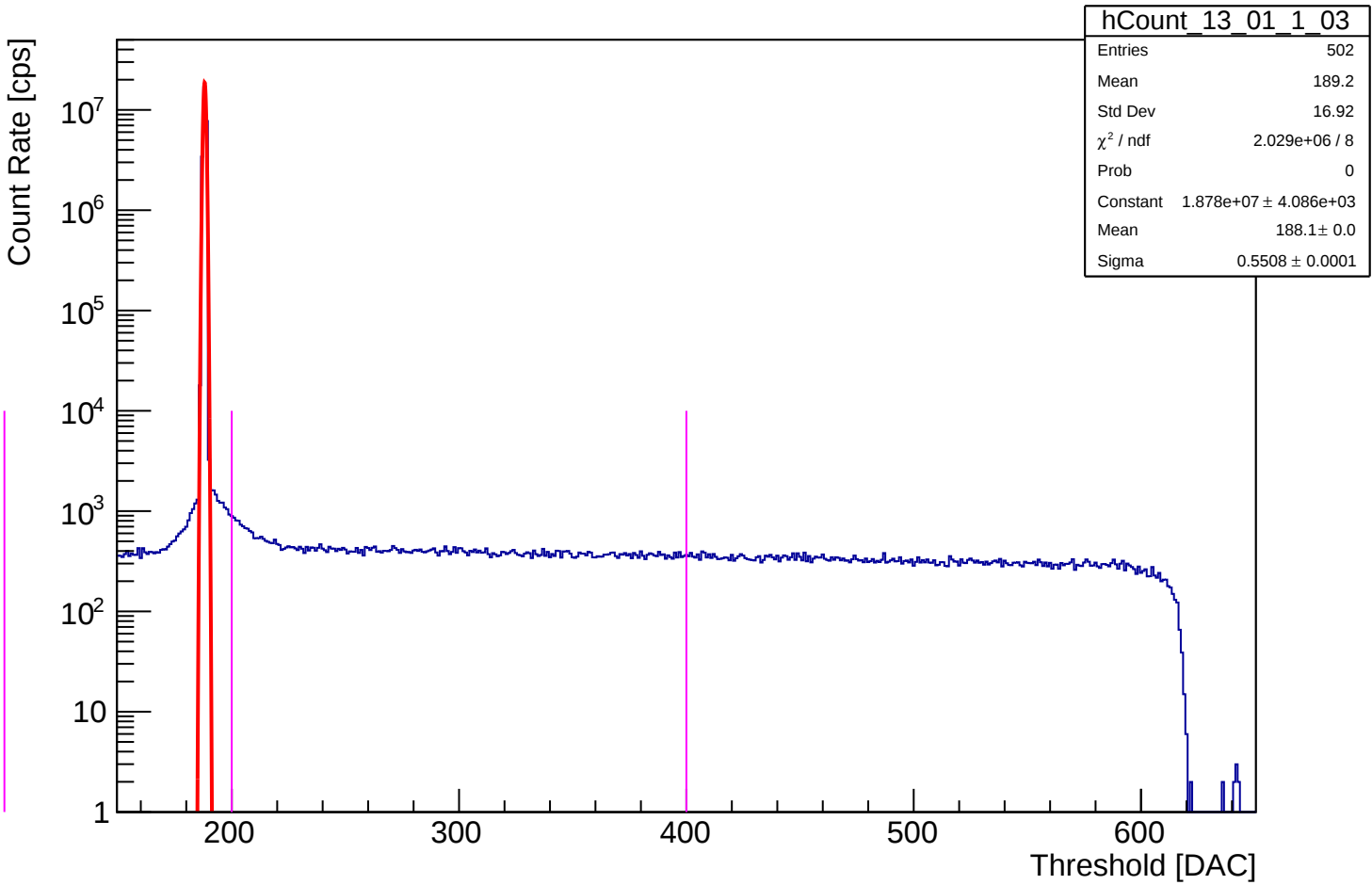
Row 1 Tile 1 Pmt 5 Pixel 54 Slot 13 Fiber 1 Asic 1 Channel 58



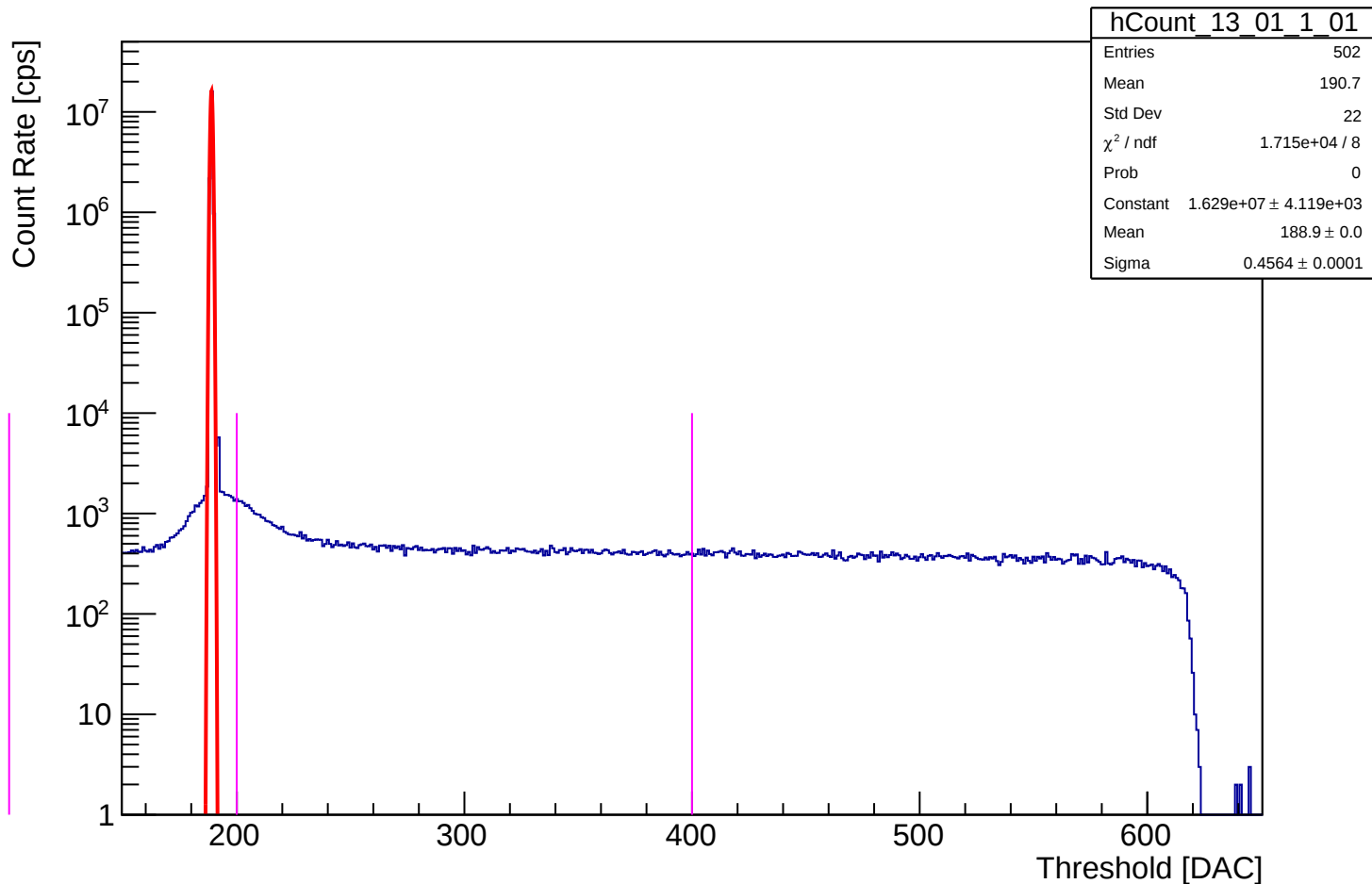
Row 1 Tile 1 Pmt 5 Pixel 55 Slot 13 Fiber 1 Asic 1 Channel 57

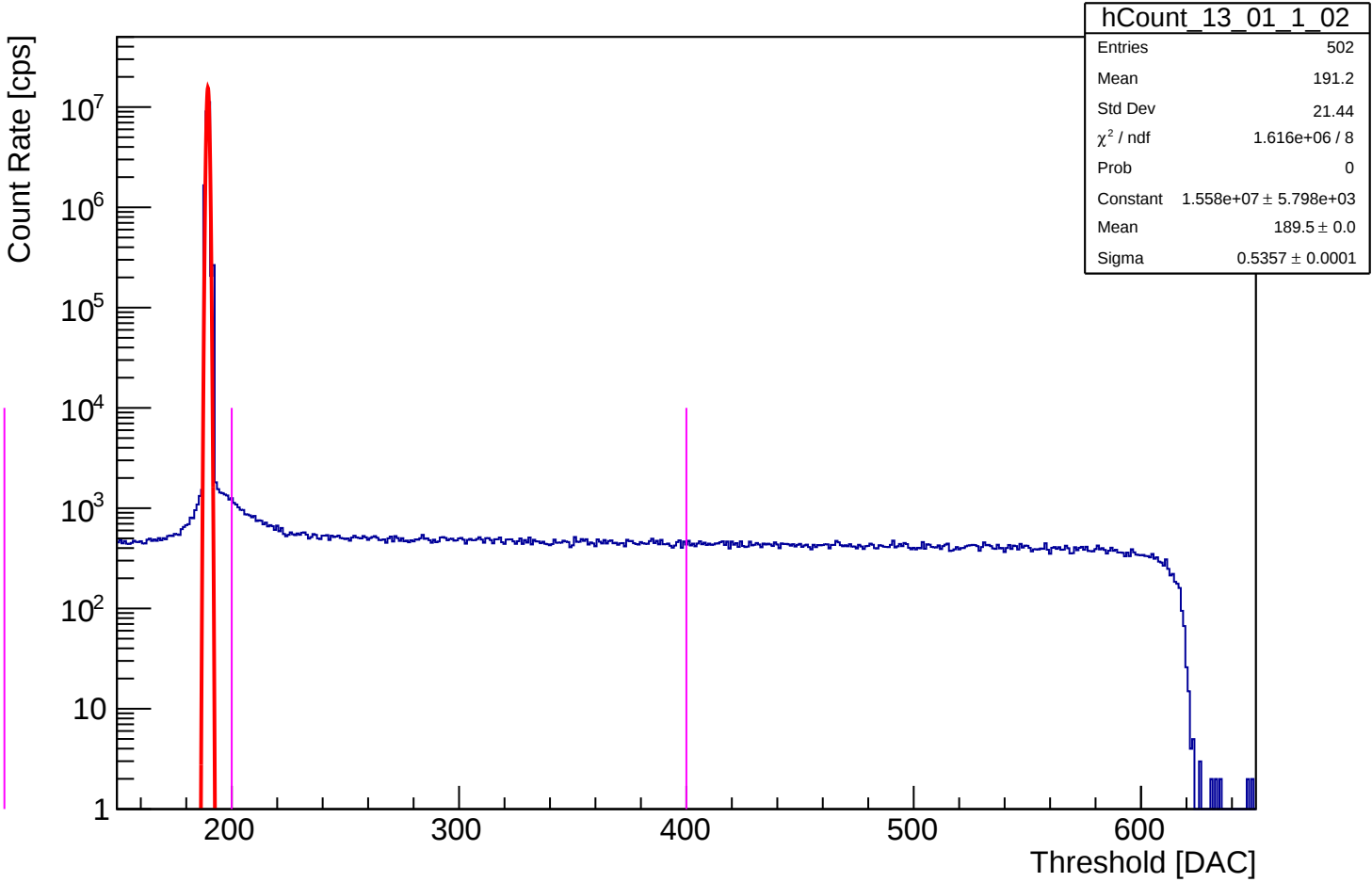


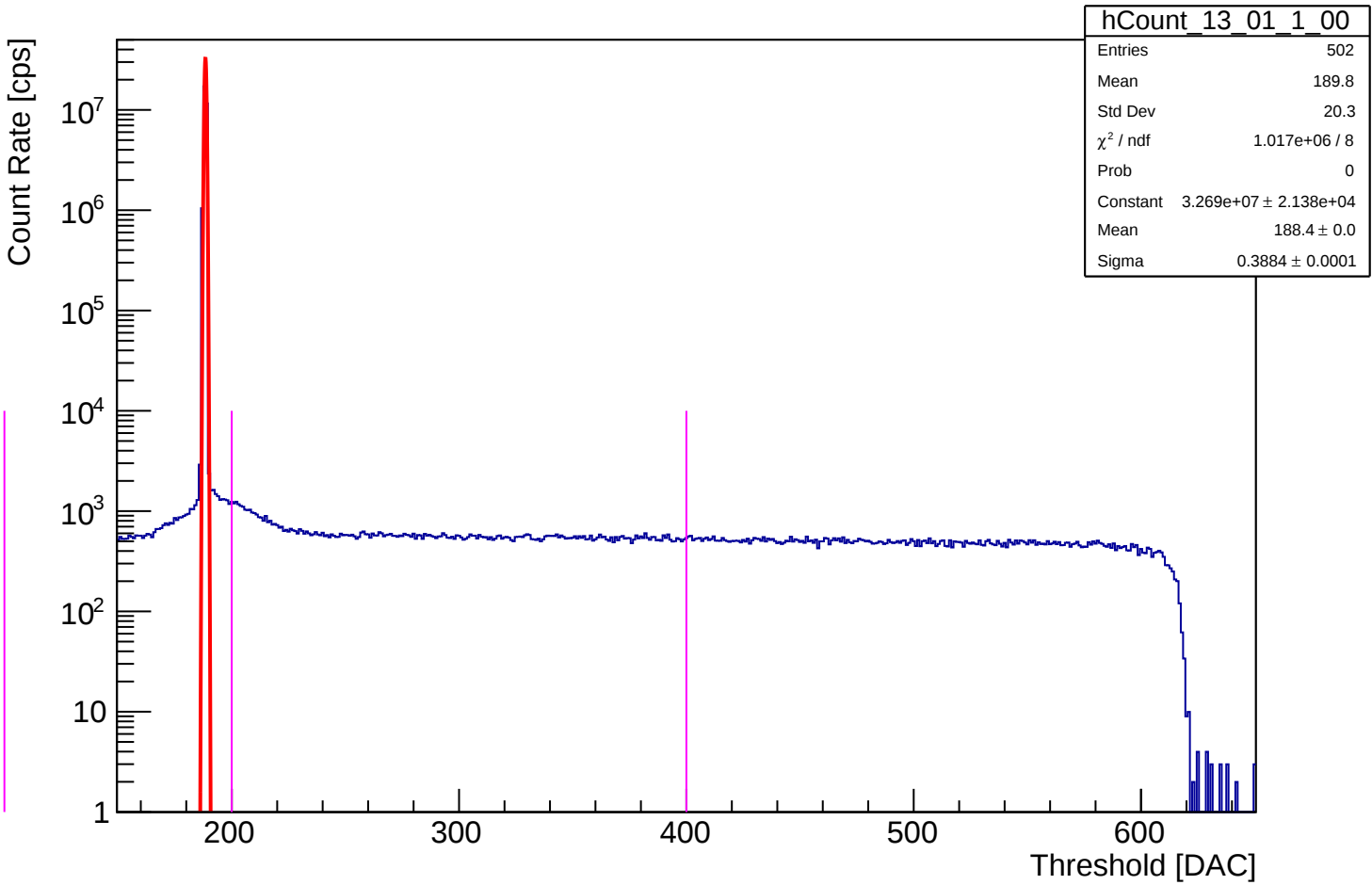




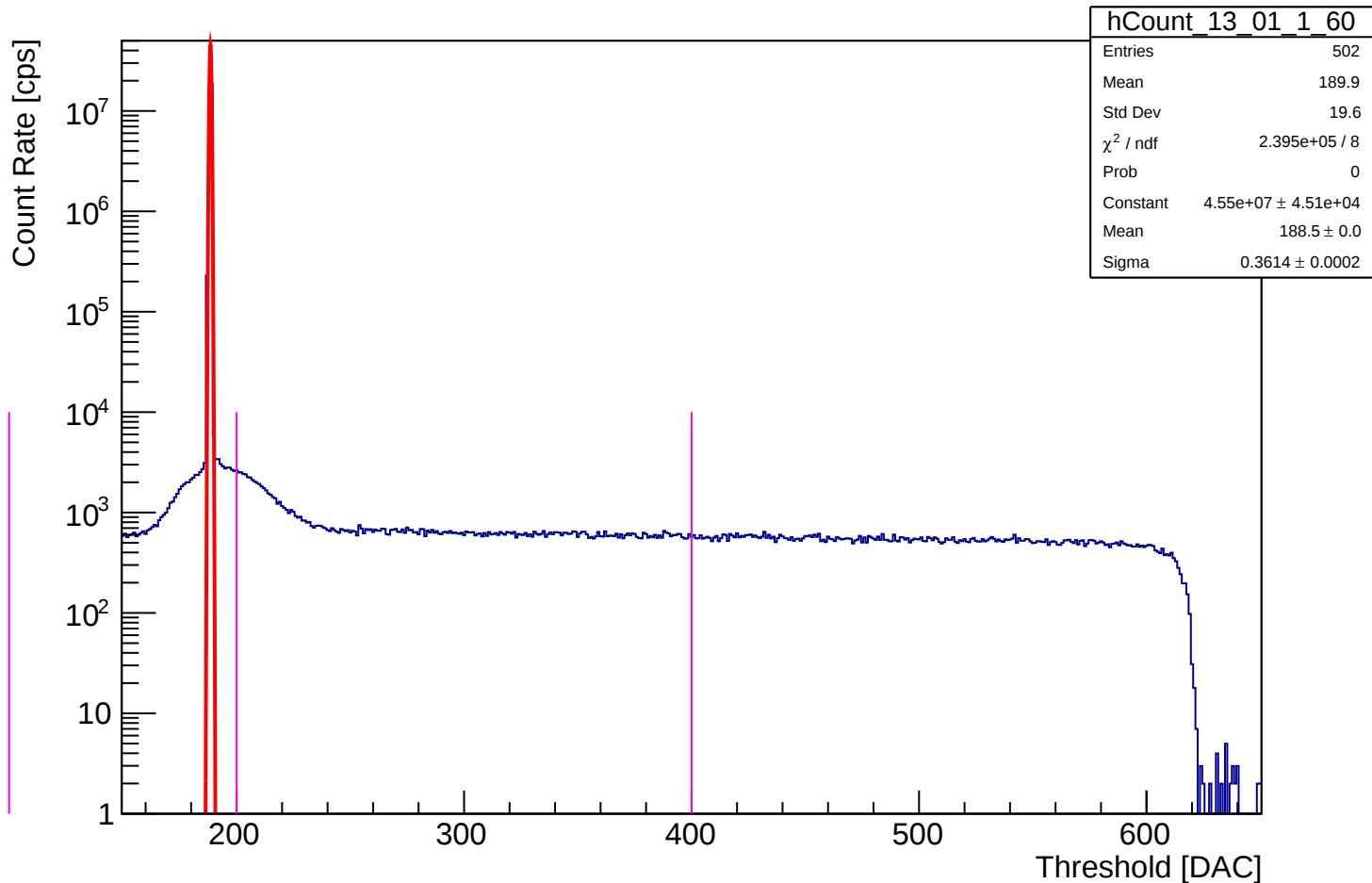
Row 1 Tile 1 Pmt 5 Pixel 58 Slot 13 Fiber 1 Asic 1 Channel 1



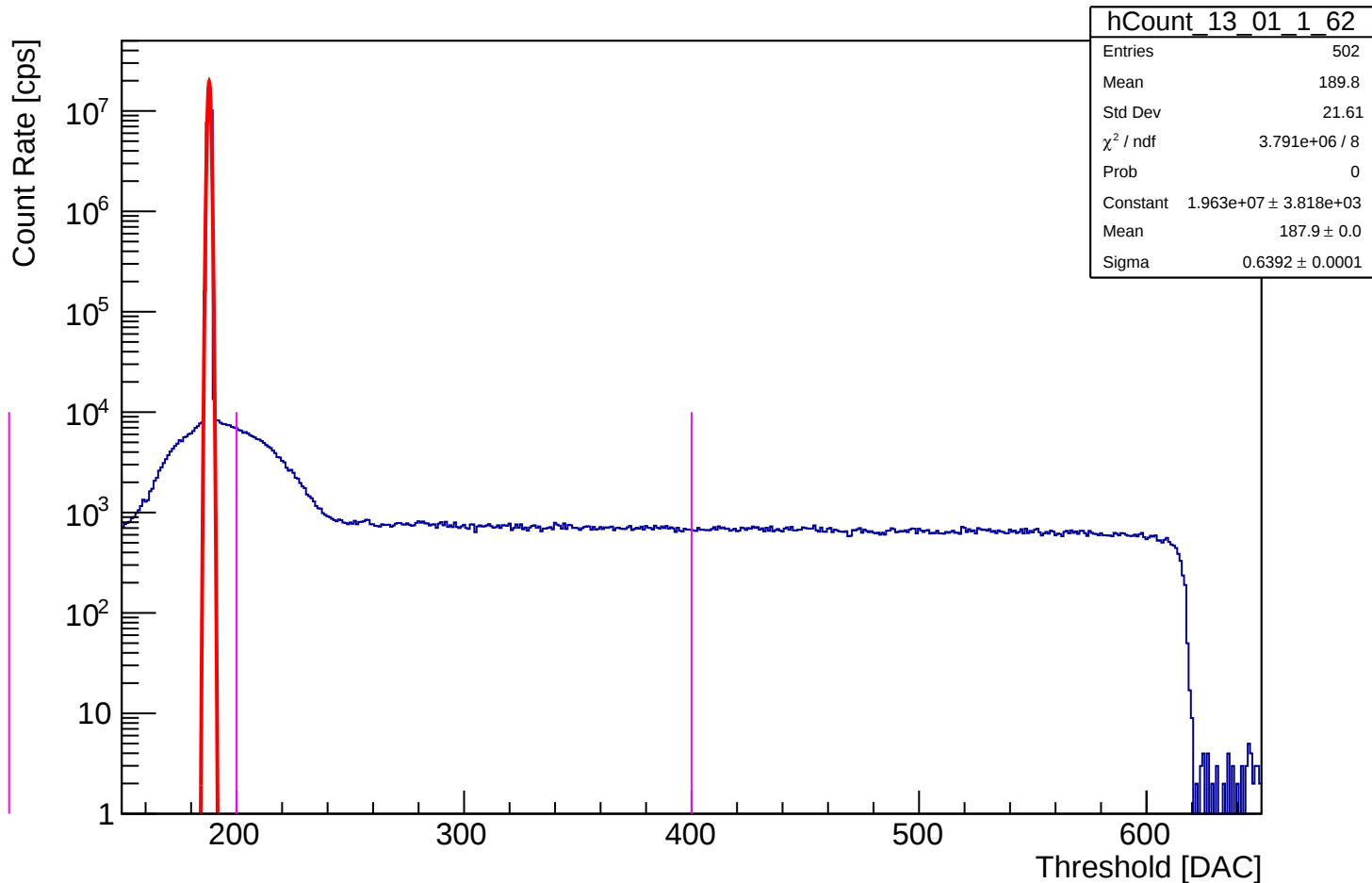




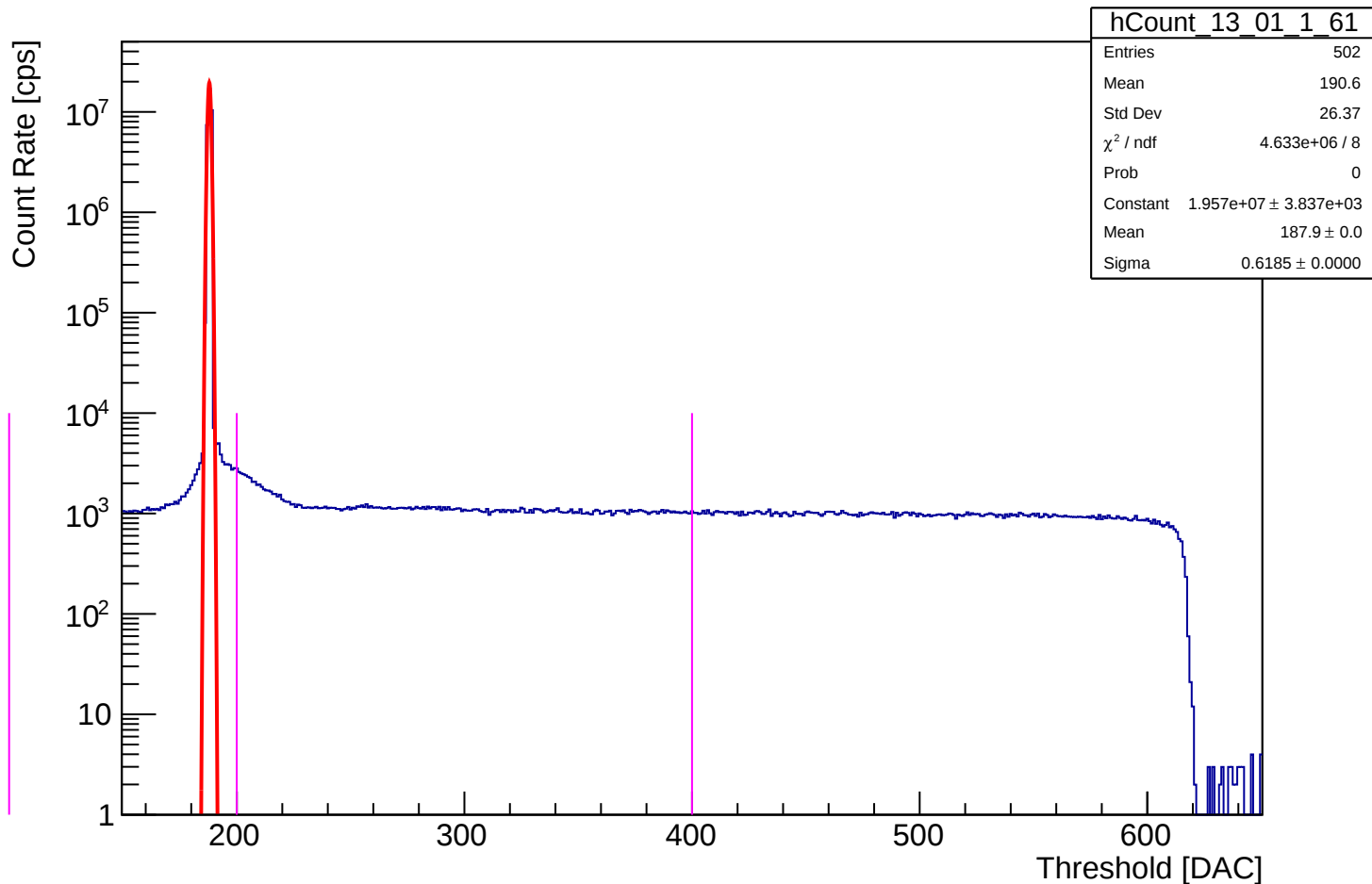
Row 1 Tile 1 Pmt 5 Pixel 61 Slot 13 Fiber 1 Asic 1 Channel 60



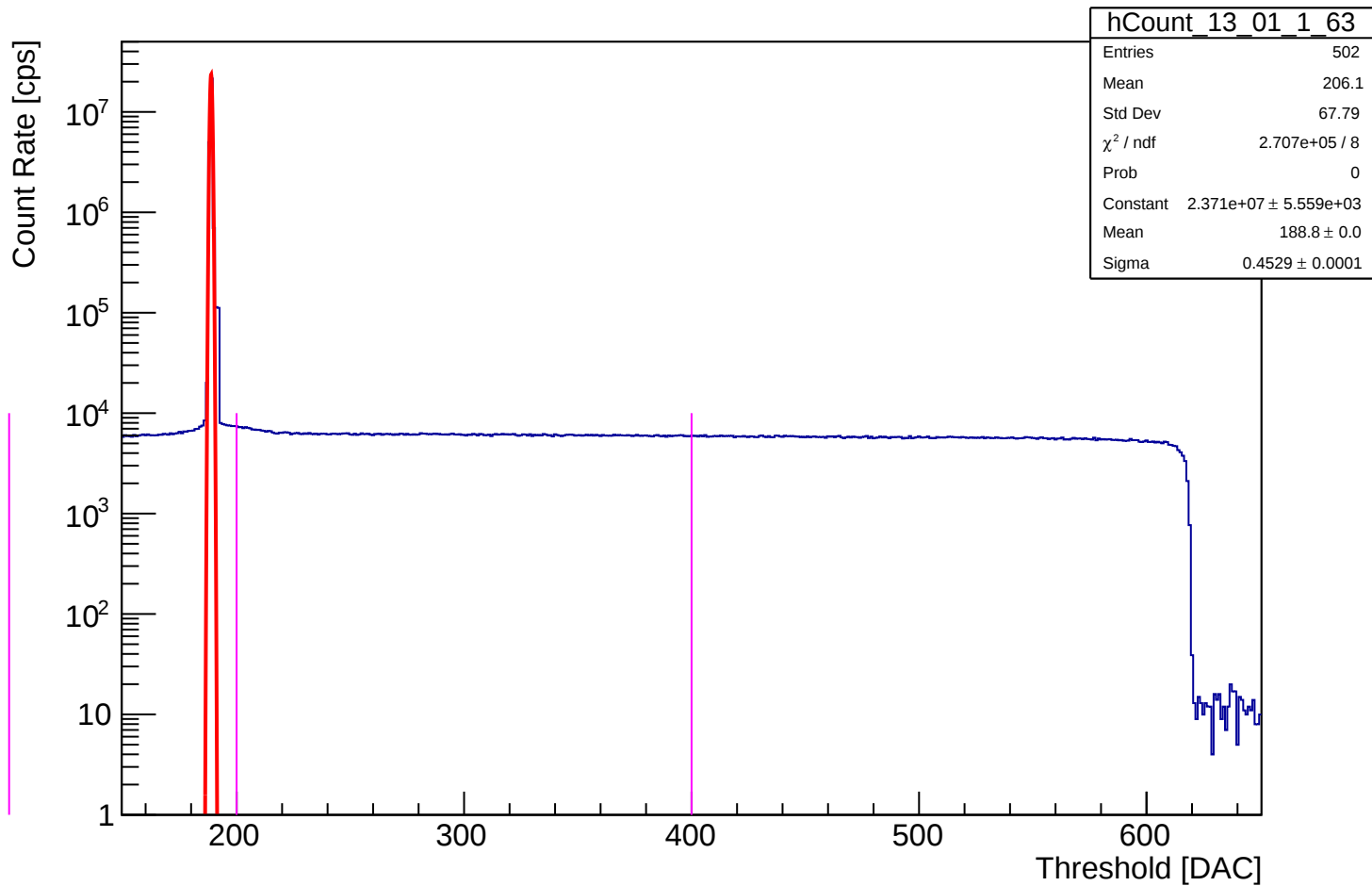
Row 1 Tile 1 Pmt 5 Pixel 62 Slot 13 Fiber 1 Asic 1 Channel 62



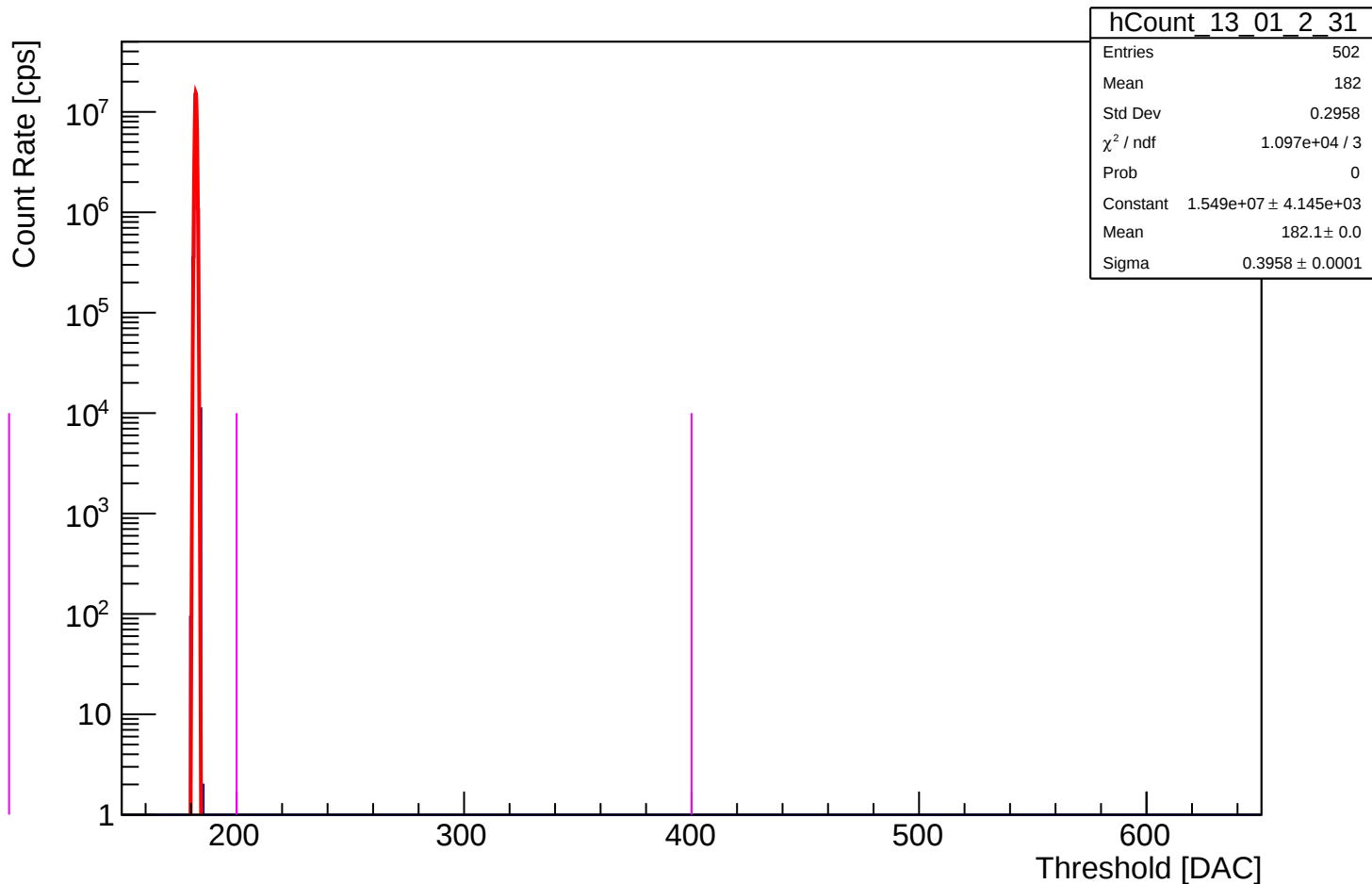
Row 1 Tile 1 Pmt 5 Pixel 63 Slot 13 Fiber 1 Asic 1 Channel 61



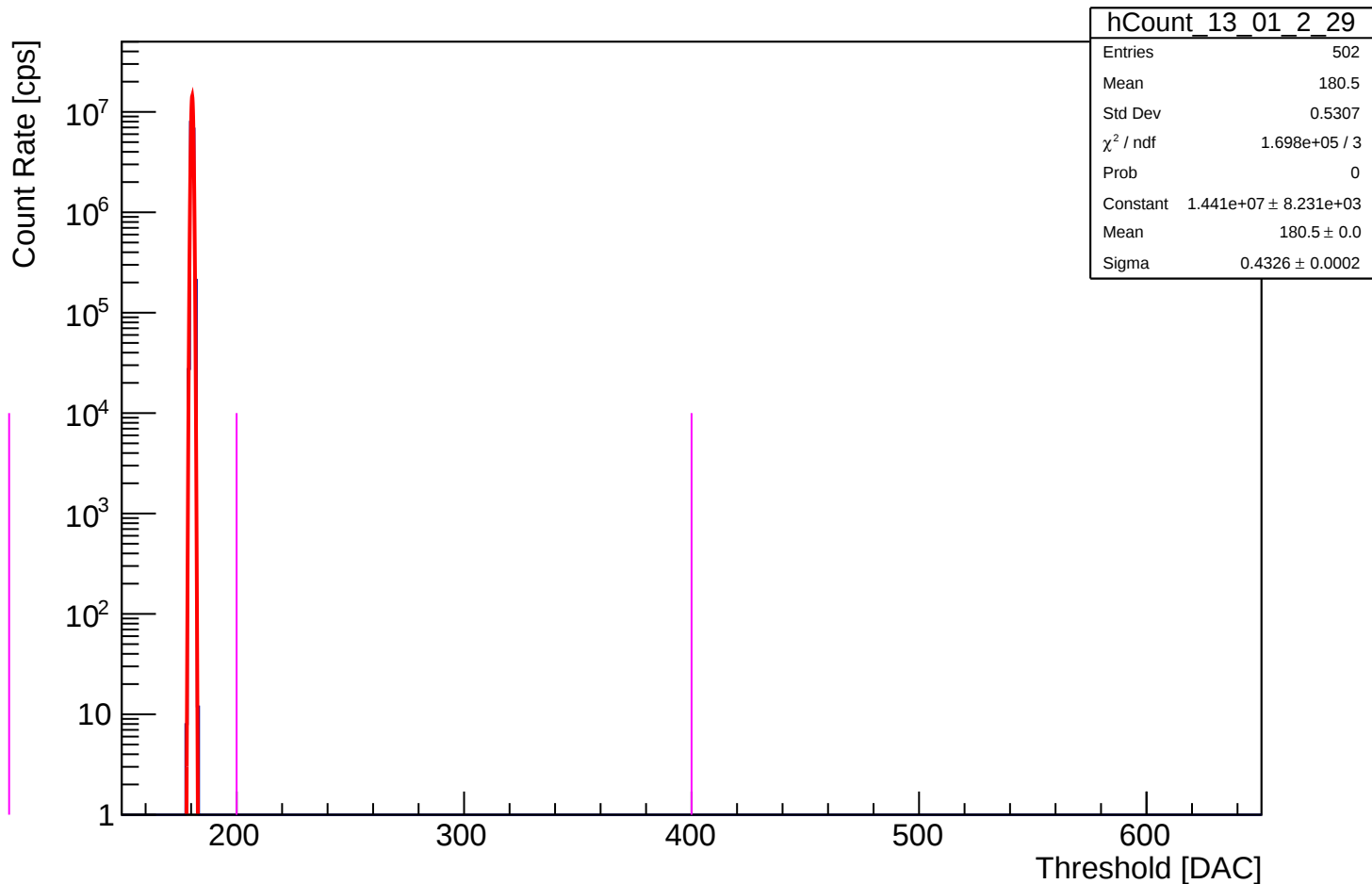
Row 1 Tile 1 Pmt 5 Pixel 64 Slot 13 Fiber 1 Asic 1 Channel 63



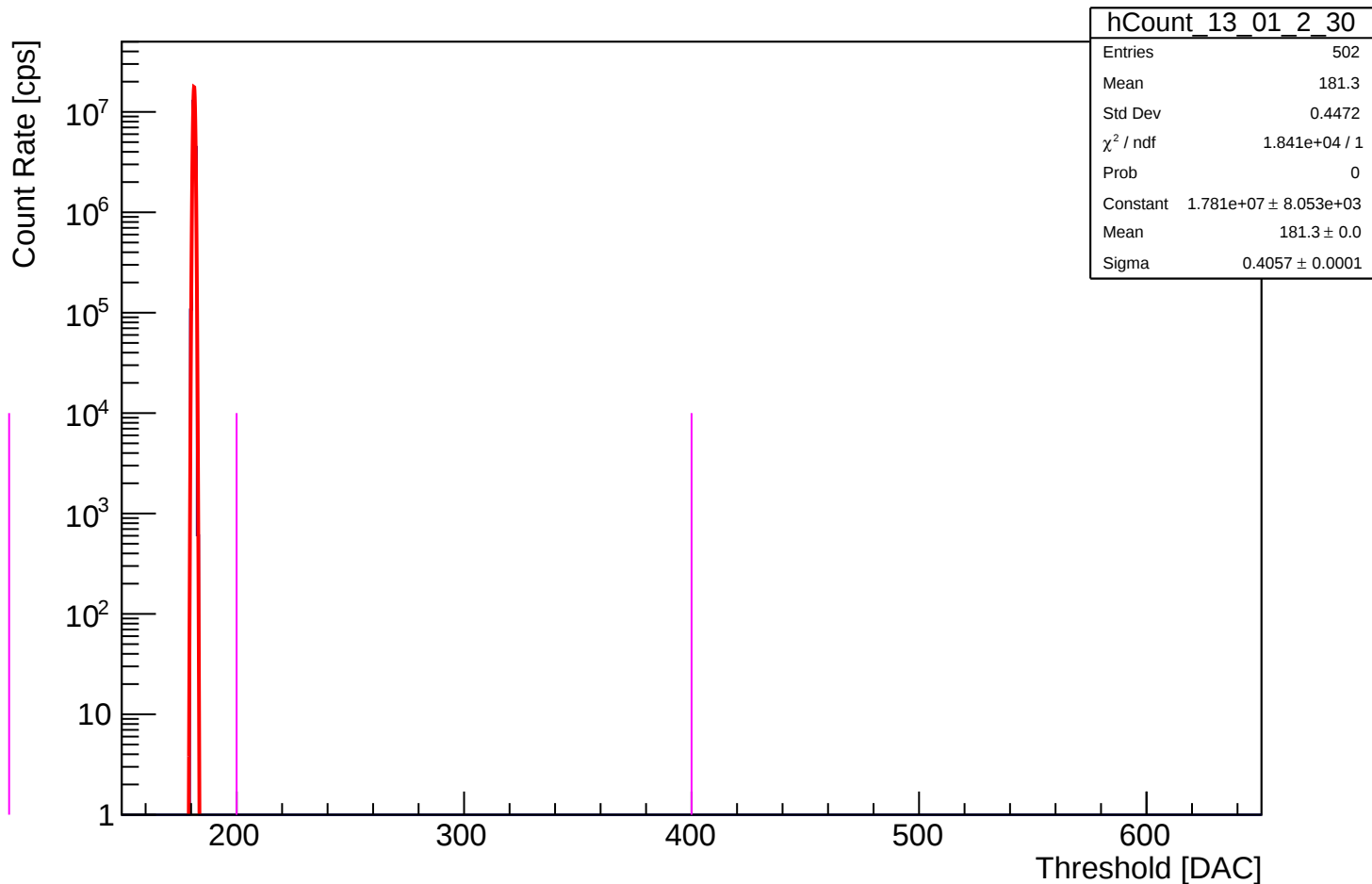
Row 1 Tile 1 Pmt 6 Pixel 1 Slot 13 Fiber 1 Asic 2 Channel 31



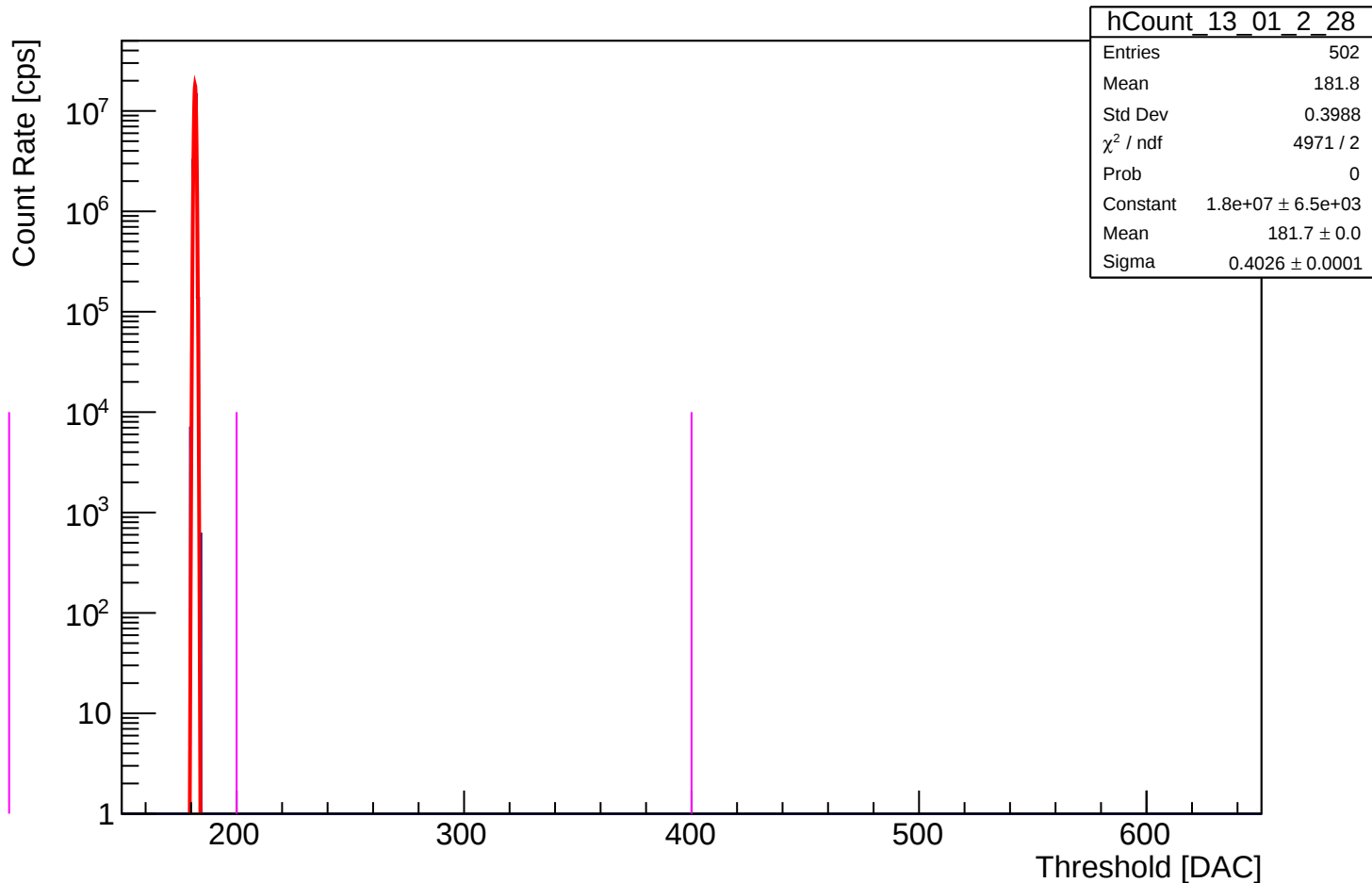
Row 1 Tile 1 Pmt 6 Pixel 2 Slot 13 Fiber 1 Asic 2 Channel 29



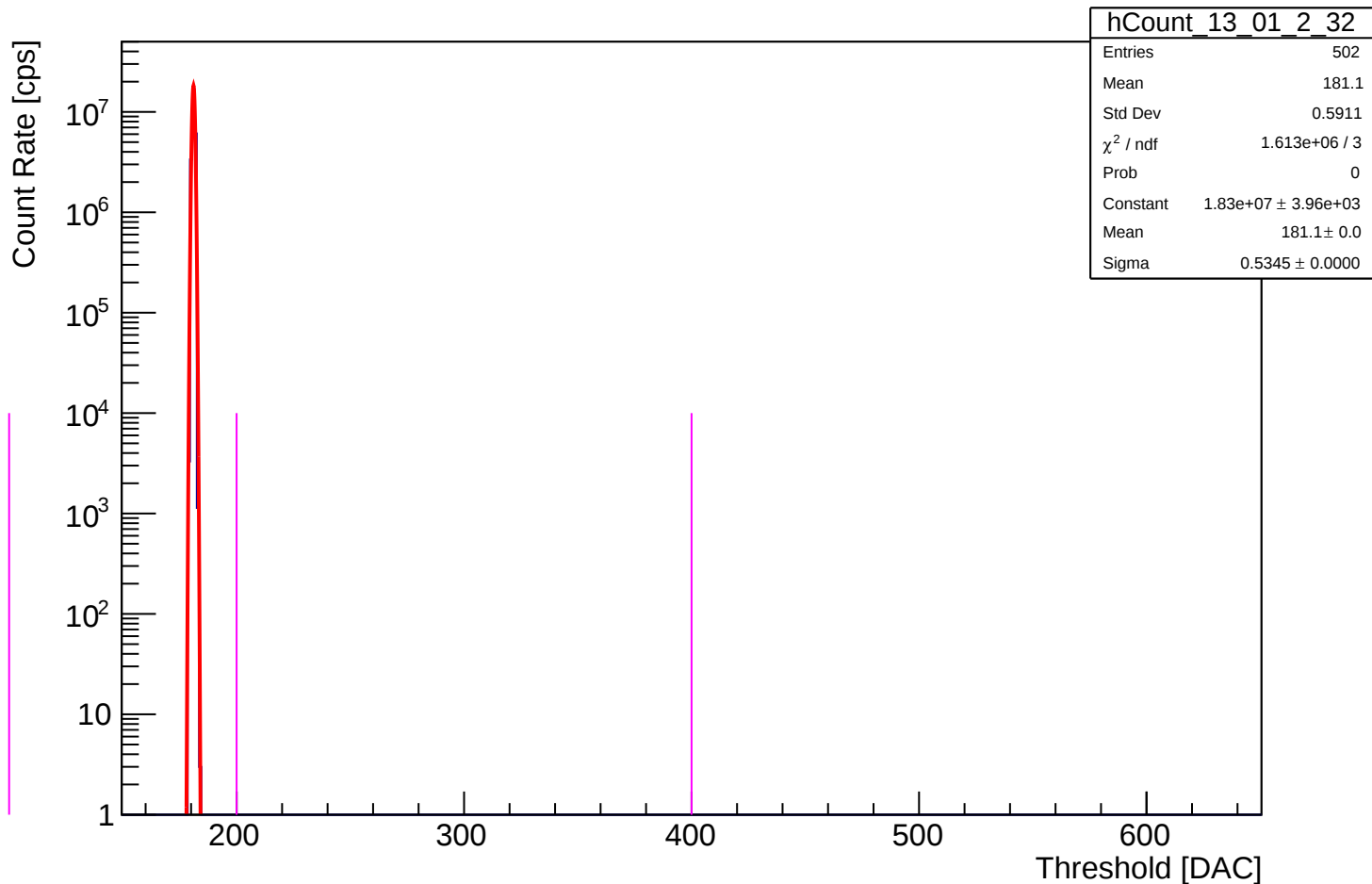
Row 1 Tile 1 Pmt 6 Pixel 3 Slot 13 Fiber 1 Asic 2 Channel 30



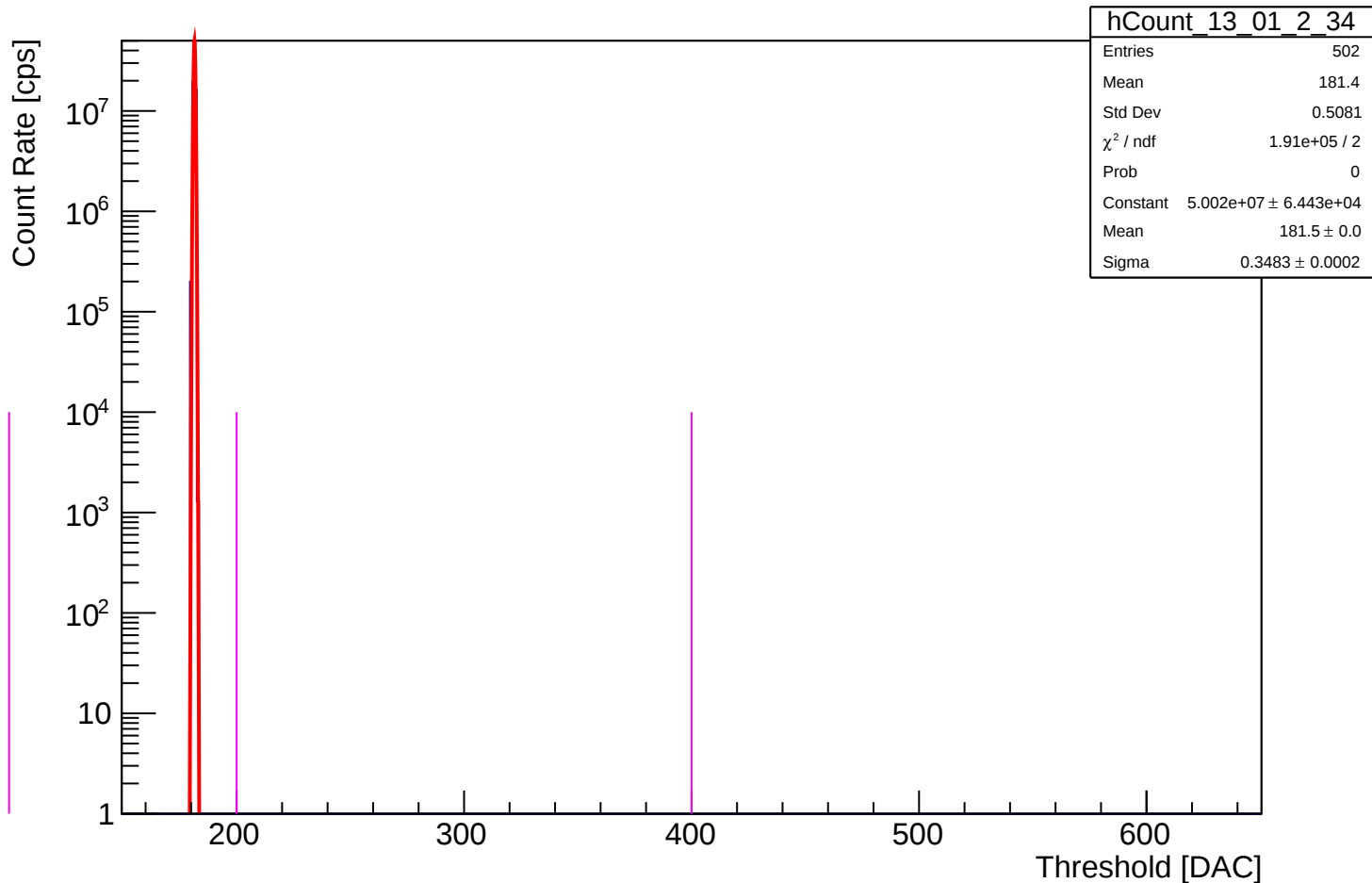
Row 1 Tile 1 Pmt 6 Pixel 4 Slot 13 Fiber 1 Asic 2 Channel 28



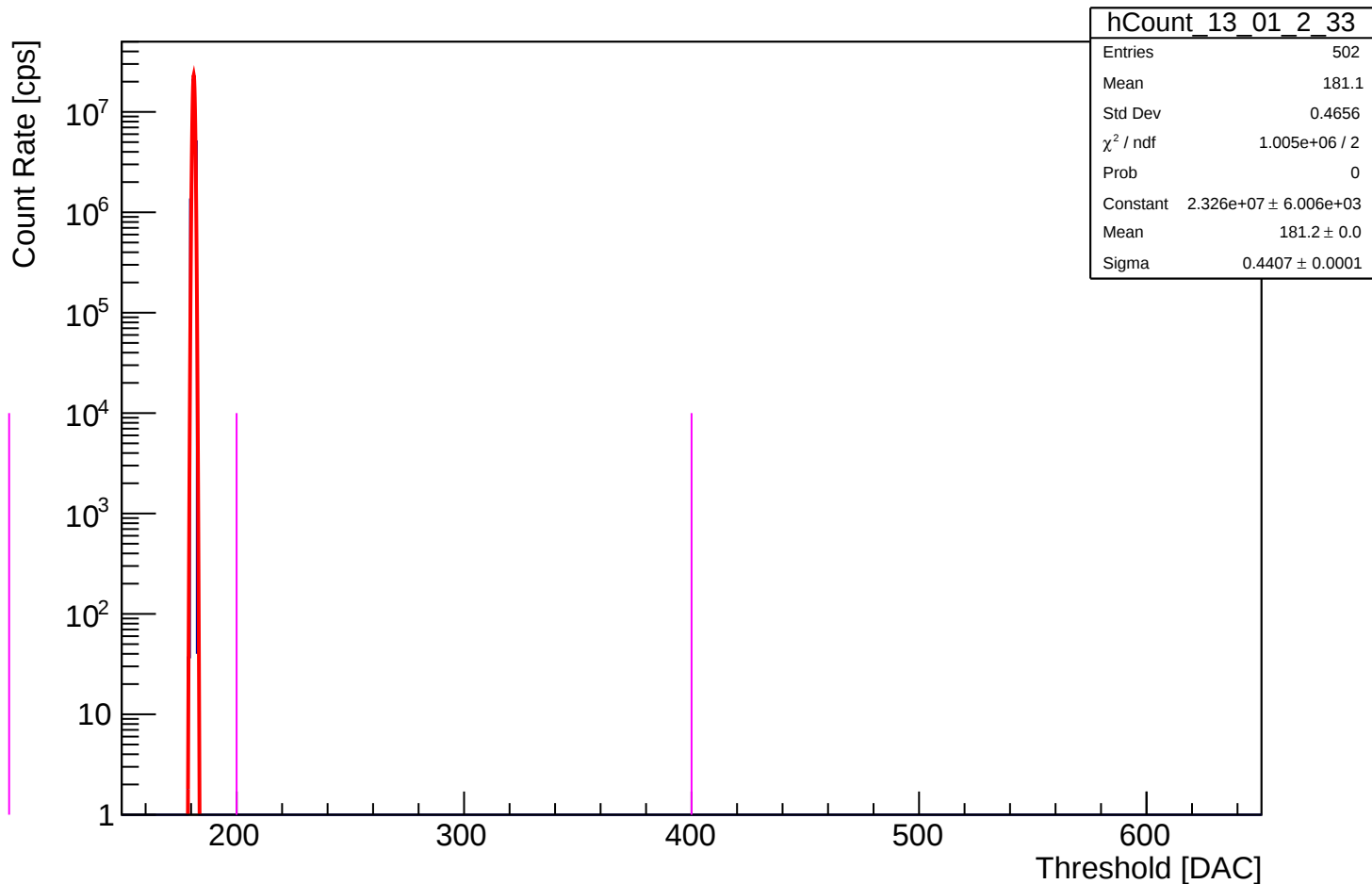
Row 1 Tile 1 Pmt 6 Pixel 5 Slot 13 Fiber 1 Asic 2 Channel 32



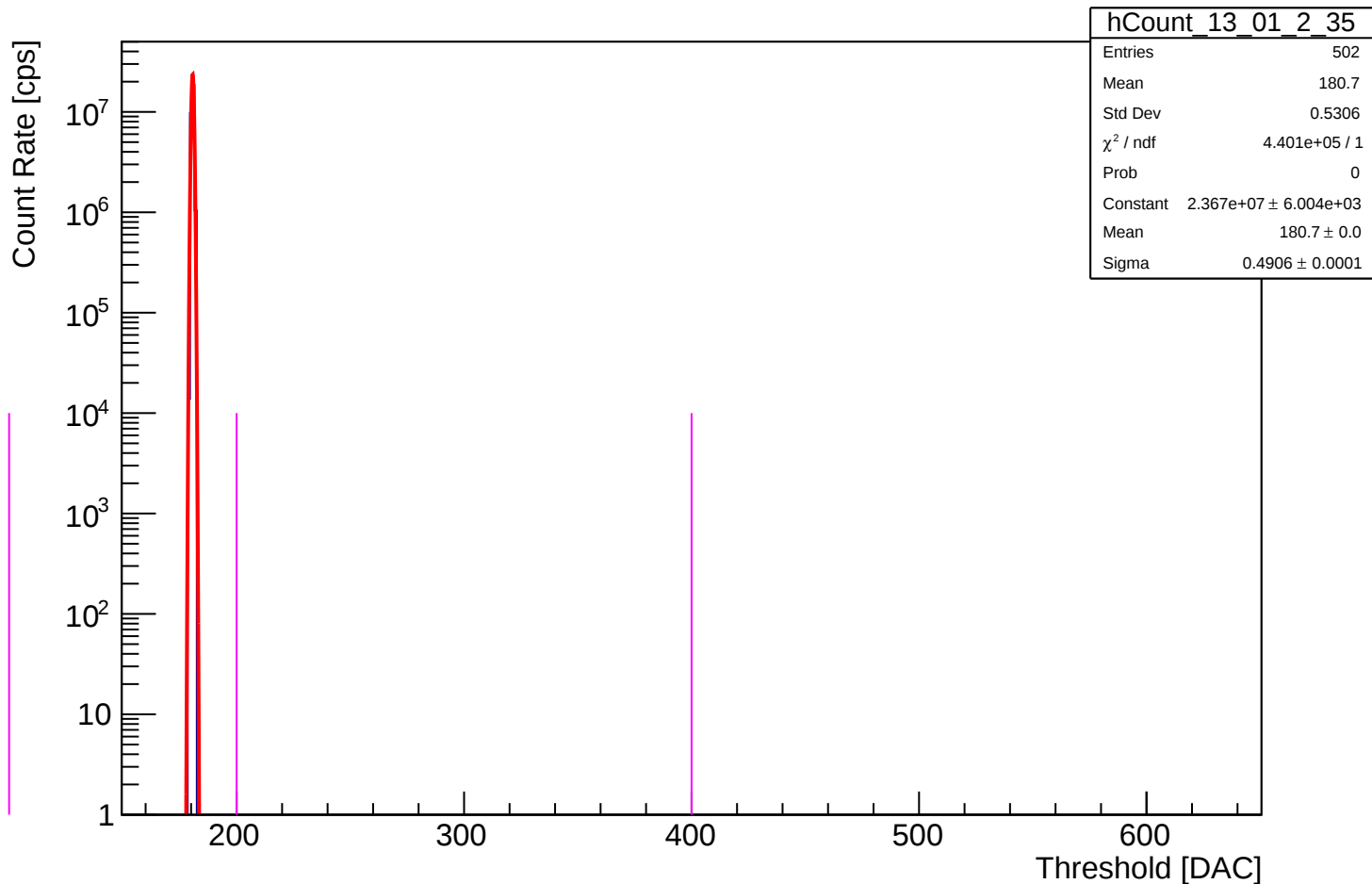
Row 1 Tile 1 Pmt 6 Pixel 6 Slot 13 Fiber 1 Asic 2 Channel 34



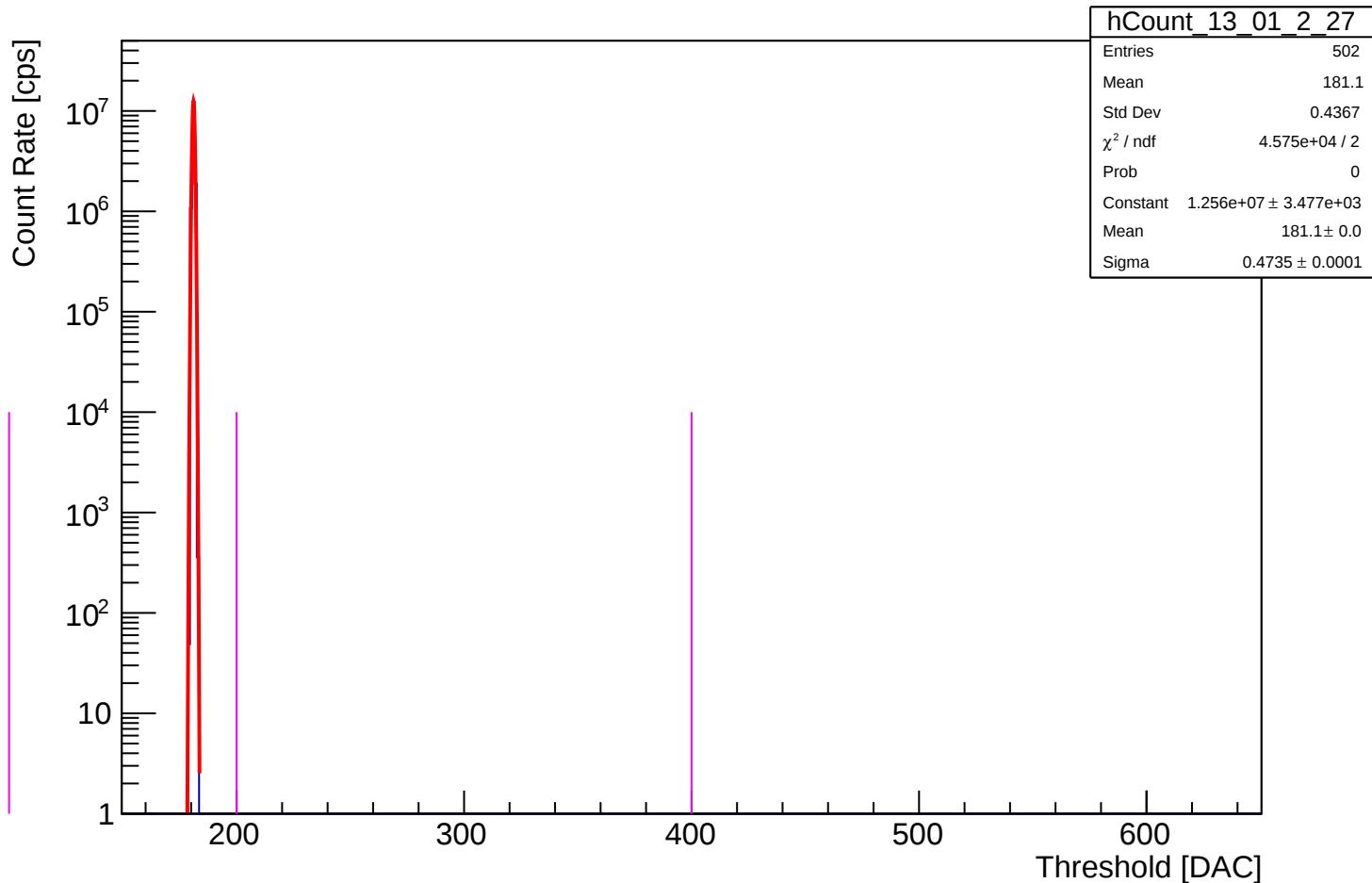
Row 1 Tile 1 Pmt 6 Pixel 7 Slot 13 Fiber 1 Asic 2 Channel 33



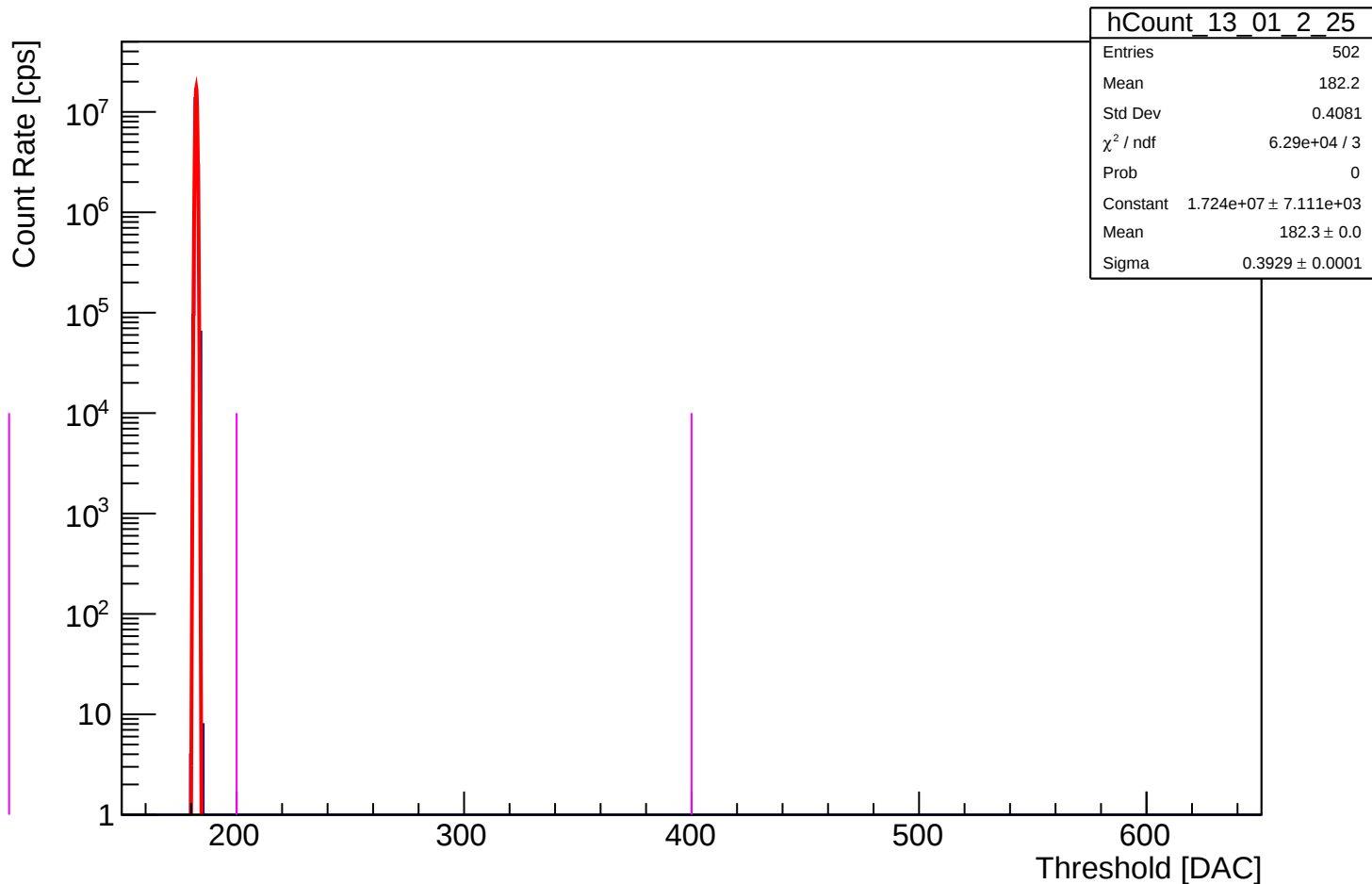
Row 1 Tile 1 Pmt 6 Pixel 8 Slot 13 Fiber 1 Asic 2 Channel 35



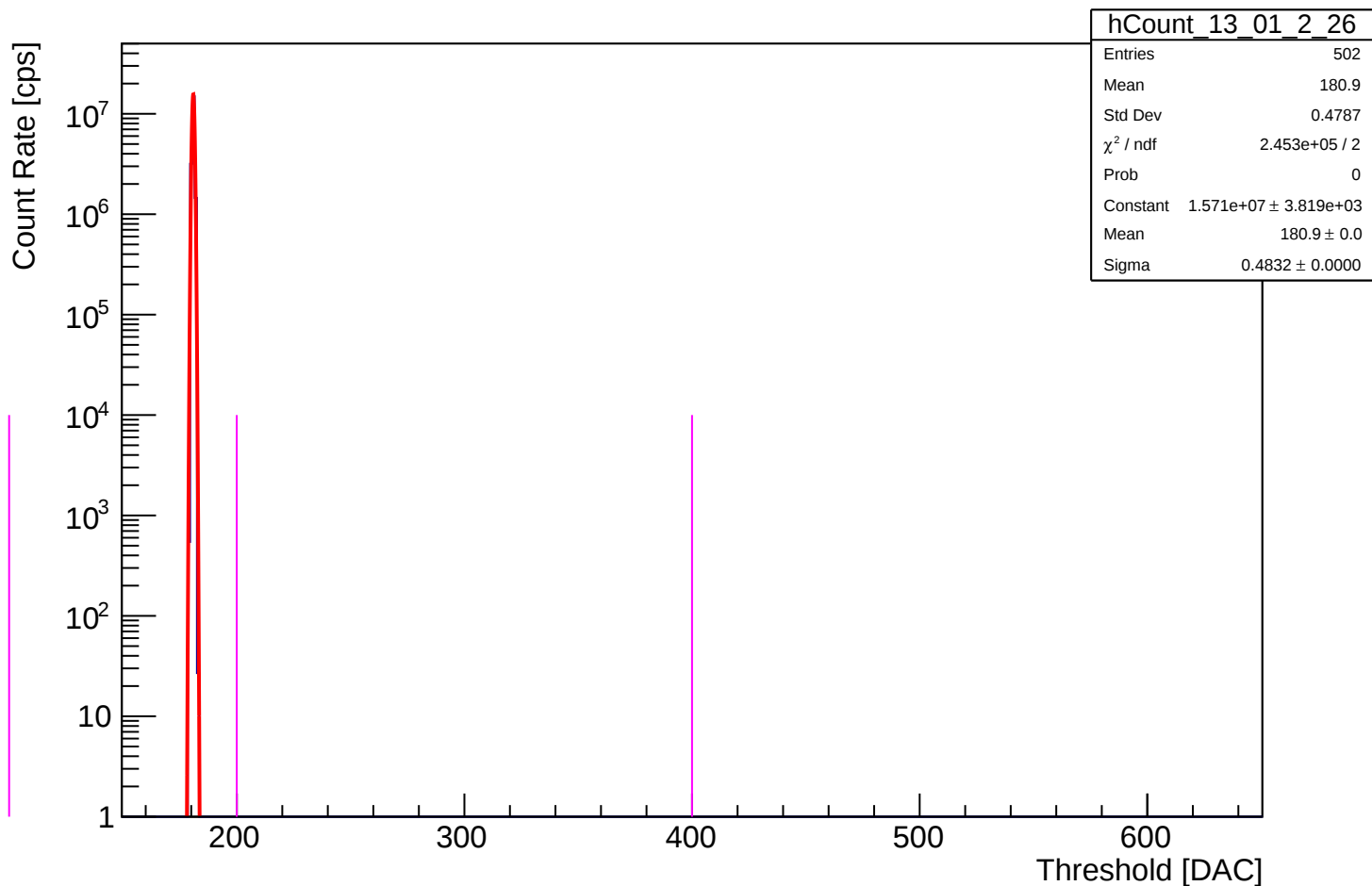
Row 1 Tile 1 Pmt 6 Pixel 9 Slot 13 Fiber 1 Asic 2 Channel 27



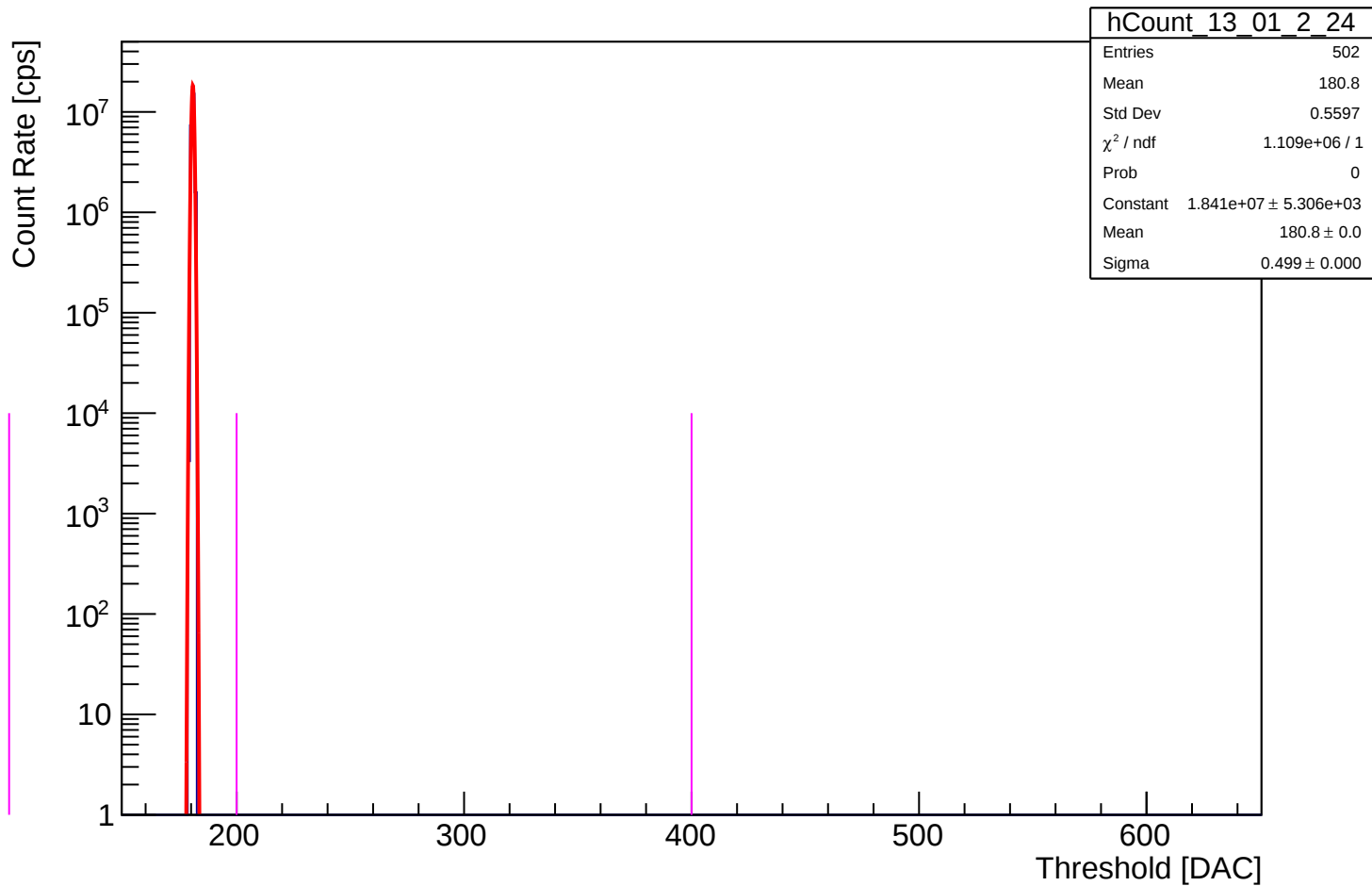
Row 1 Tile 1 Pmt 6 Pixel 10 Slot 13 Fiber 1 Asic 2 Channel 25



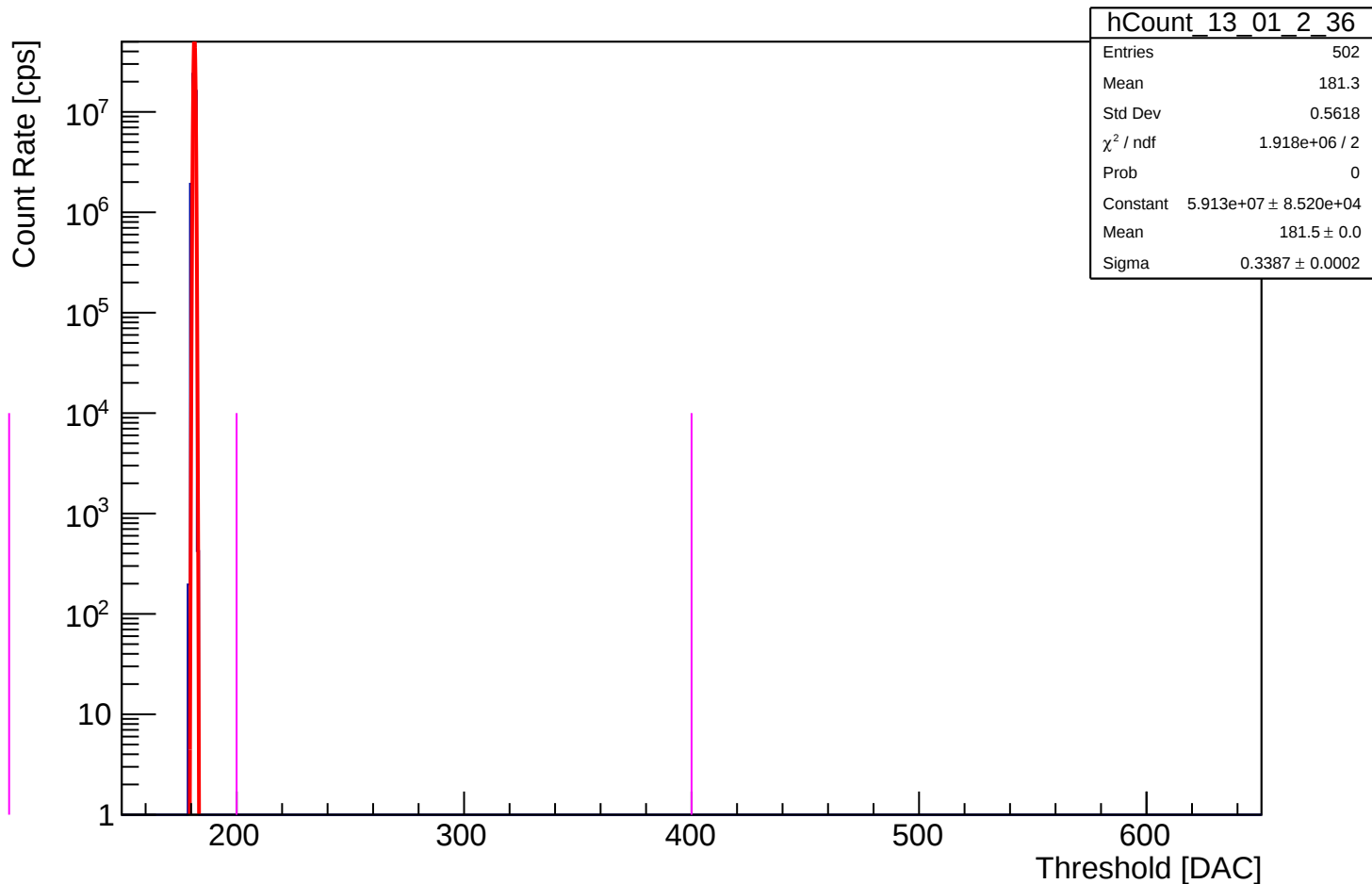
Row 1 Tile 1 Pmt 6 Pixel 11 Slot 13 Fiber 1 Asic 2 Channel 26



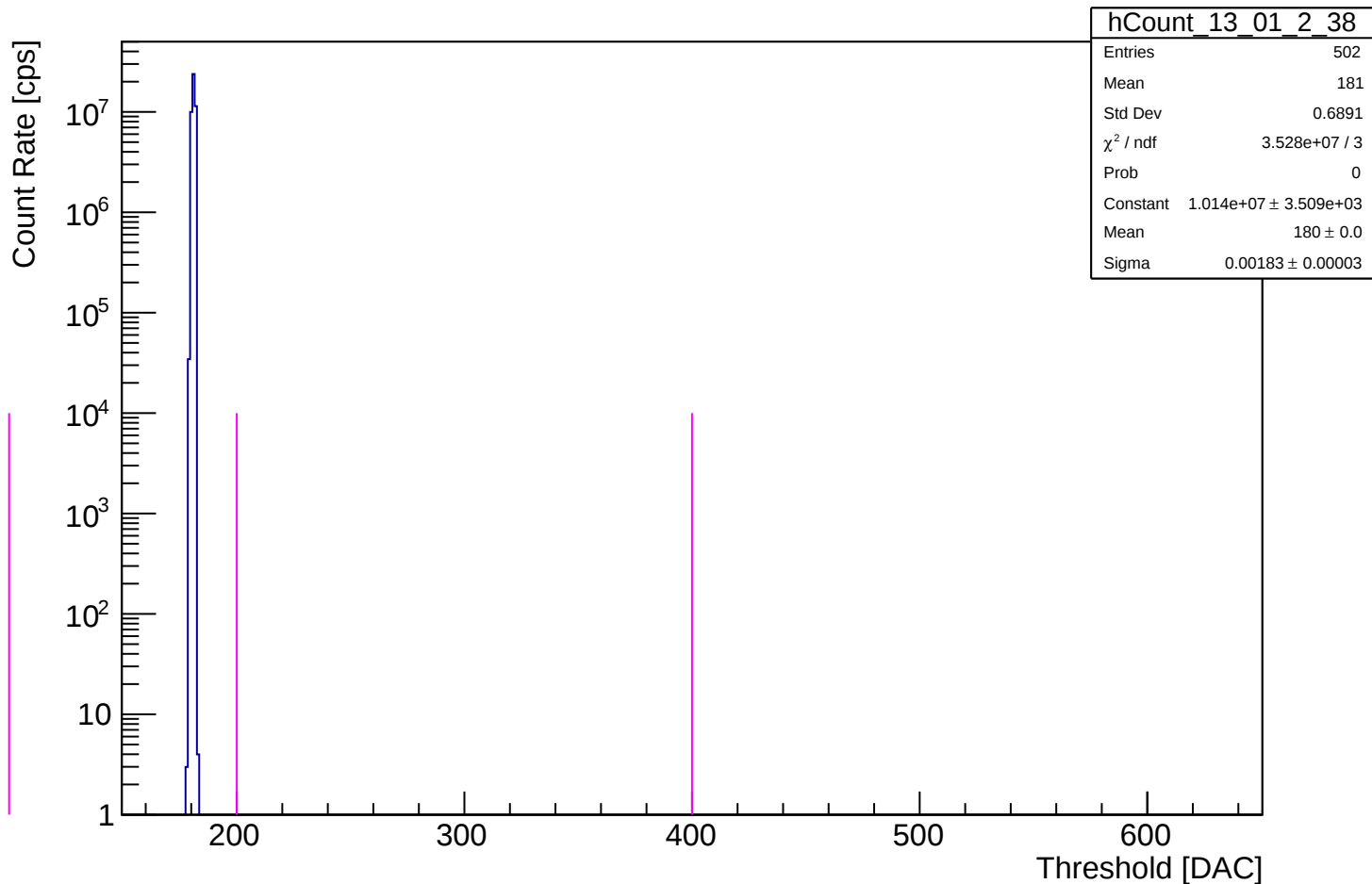
Row 1 Tile 1 Pmt 6 Pixel 12 Slot 13 Fiber 1 Asic 2 Channel 24



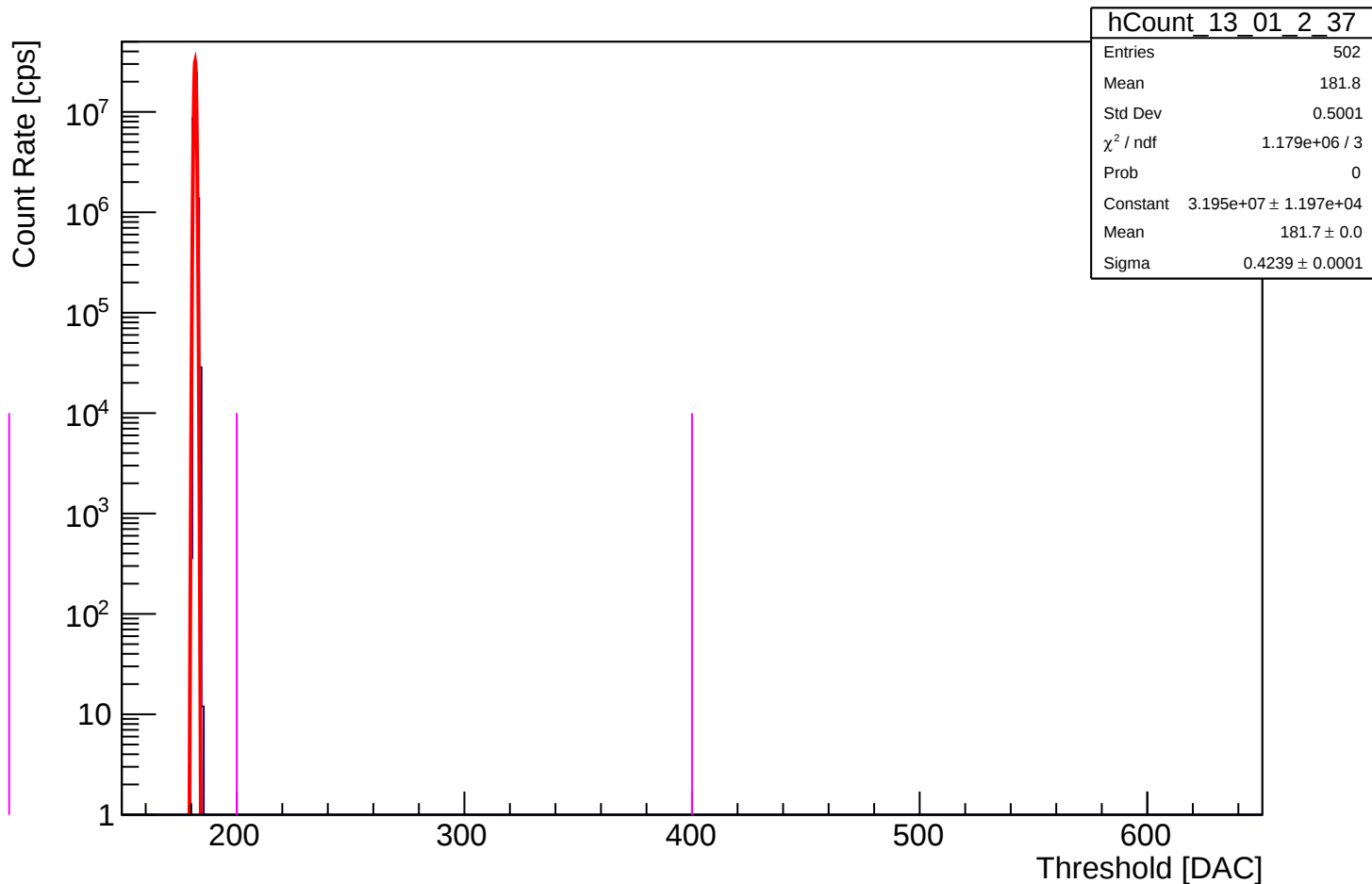
Row 1 Tile 1 Pmt 6 Pixel 13 Slot 13 Fiber 1 Asic 2 Channel 36

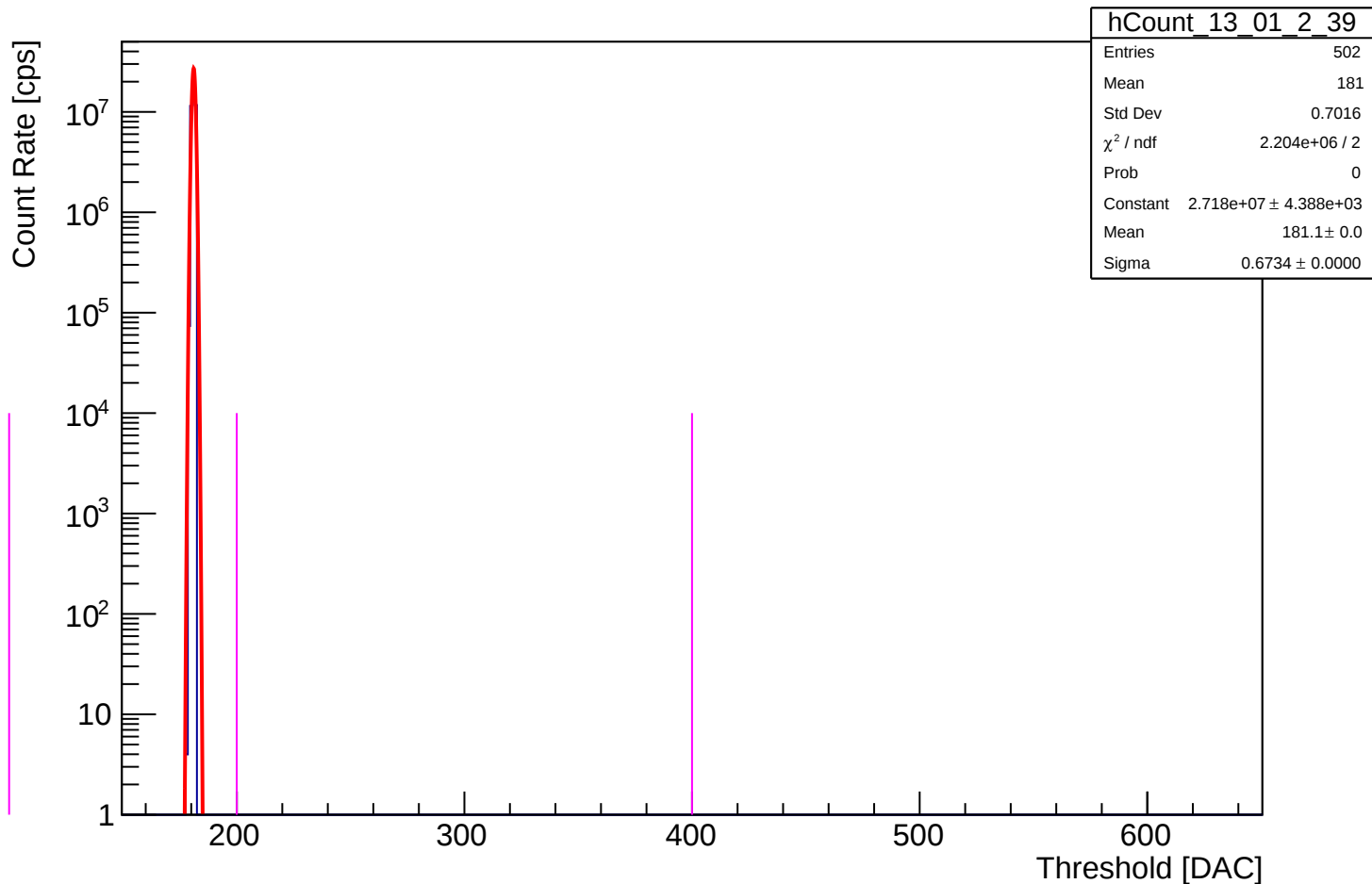


Row 1 Tile 1 Pmt 6 Pixel 14 Slot 13 Fiber 1 Asic 2 Channel 38

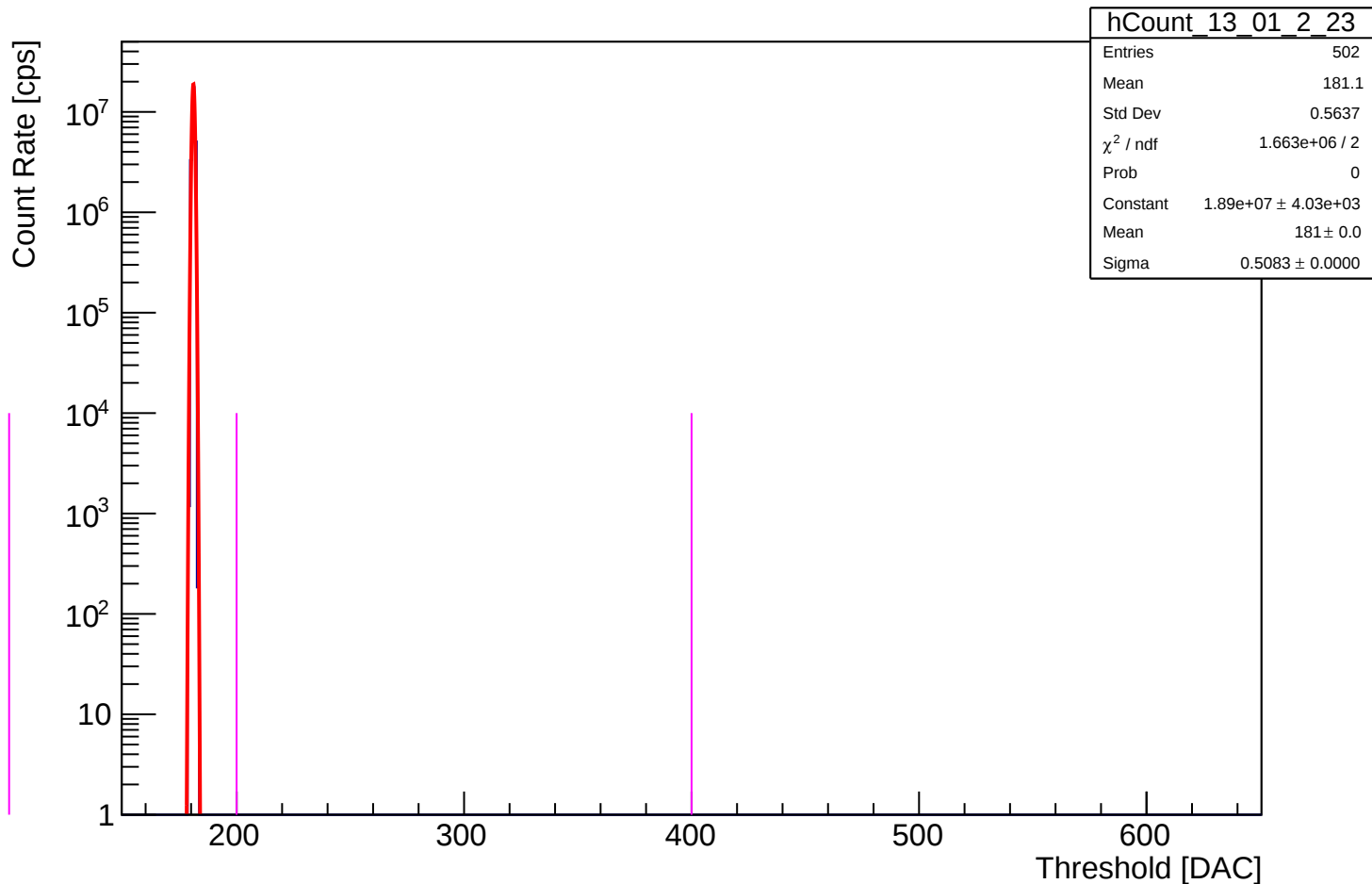


Row 1 Tile 1 Pmt 6 Pixel 15 Slot 13 Fiber 1 Asic 2 Channel 37

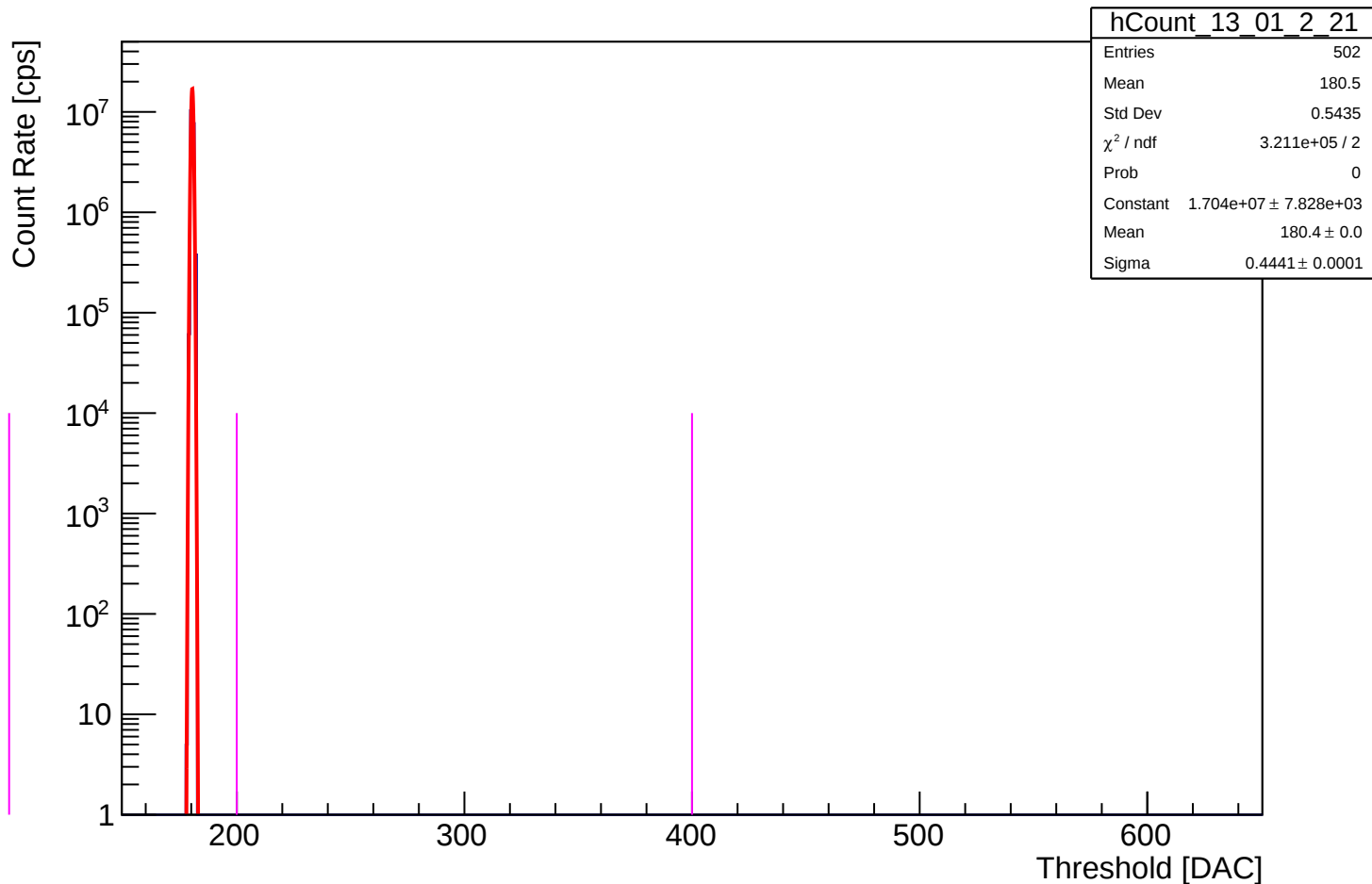




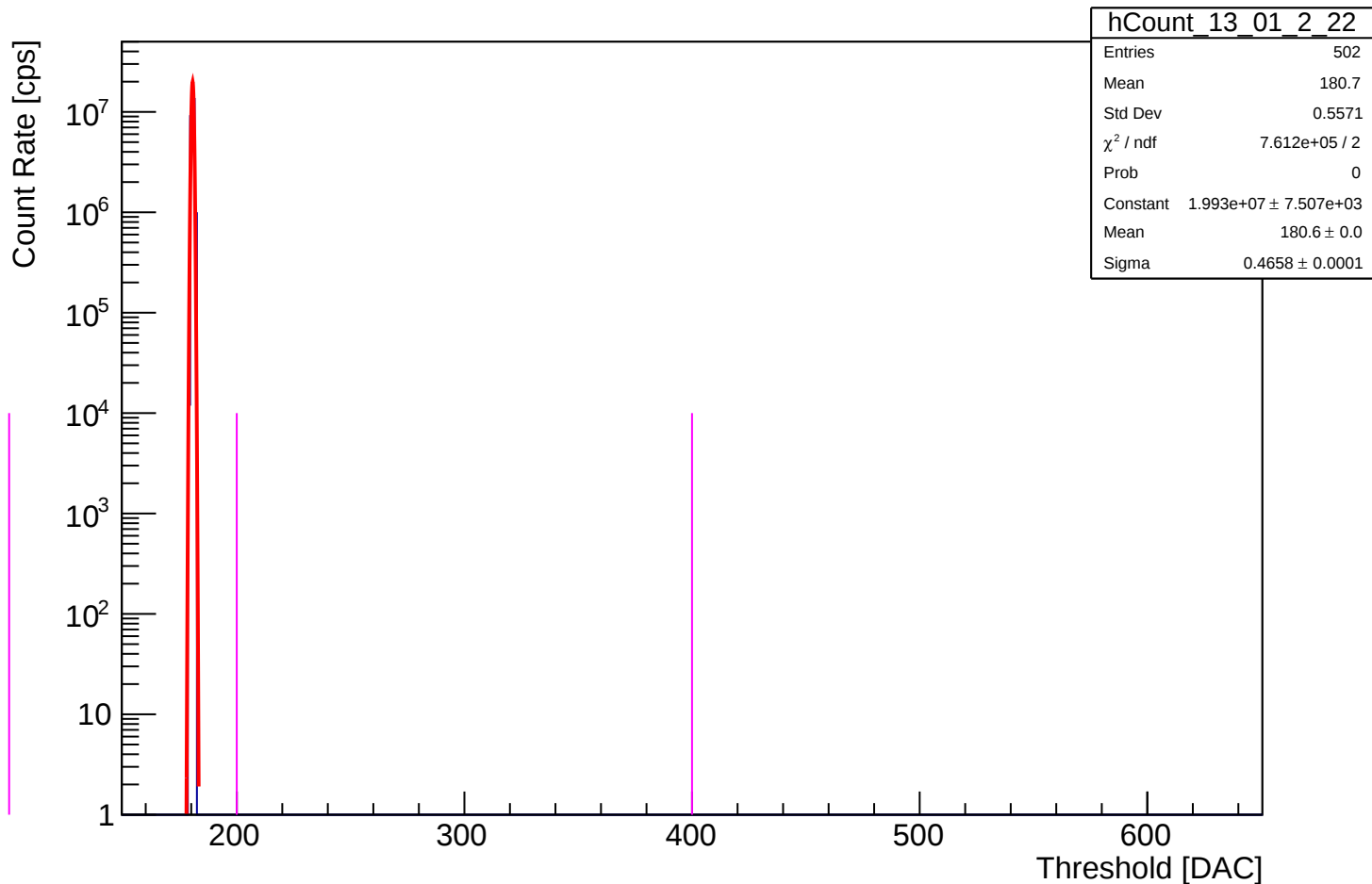
Row 1 Tile 1 Pmt 6 Pixel 17 Slot 13 Fiber 1 Asic 2 Channel 23



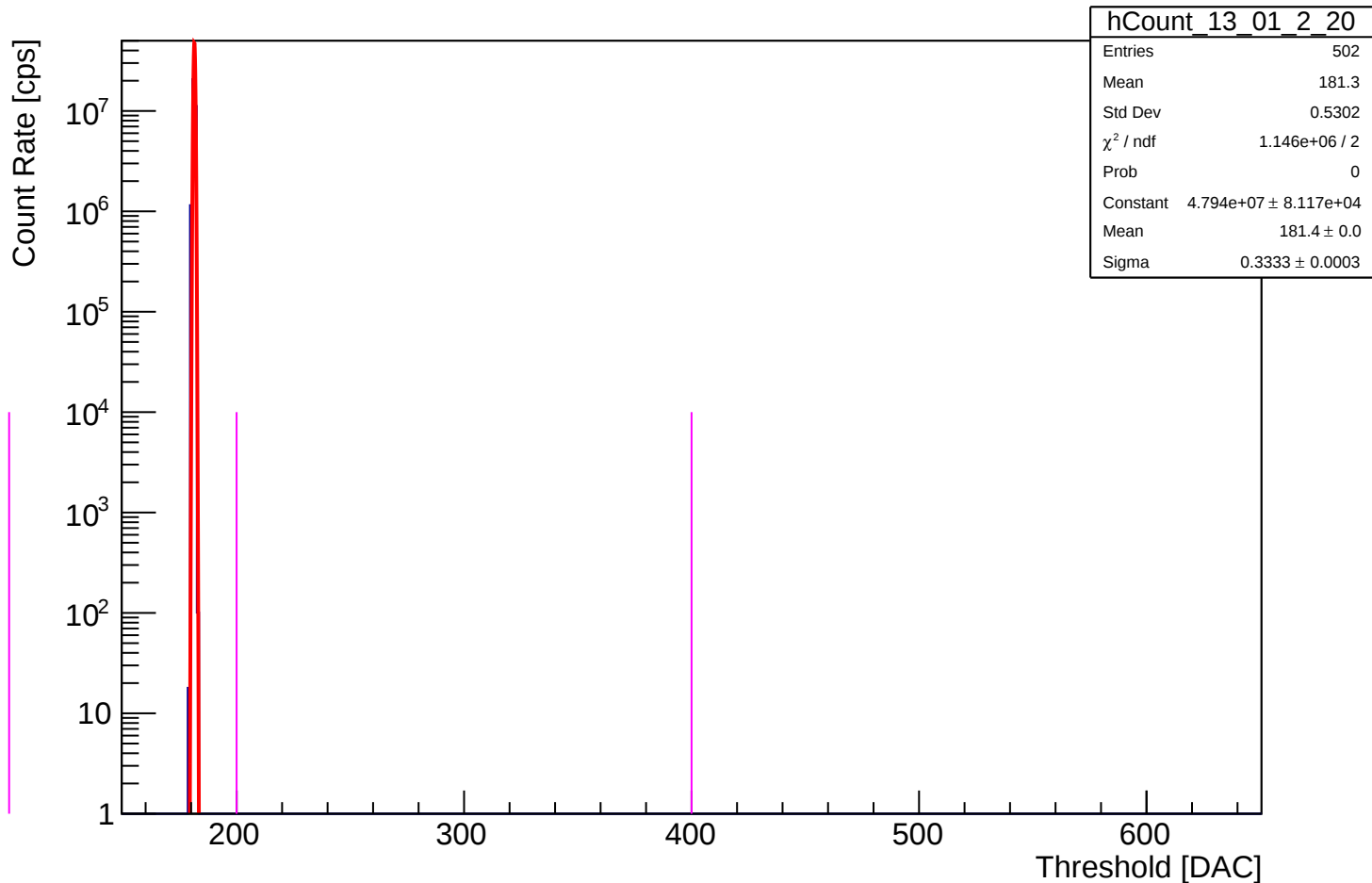
Row 1 Tile 1 Pmt 6 Pixel 18 Slot 13 Fiber 1 Asic 2 Channel 21



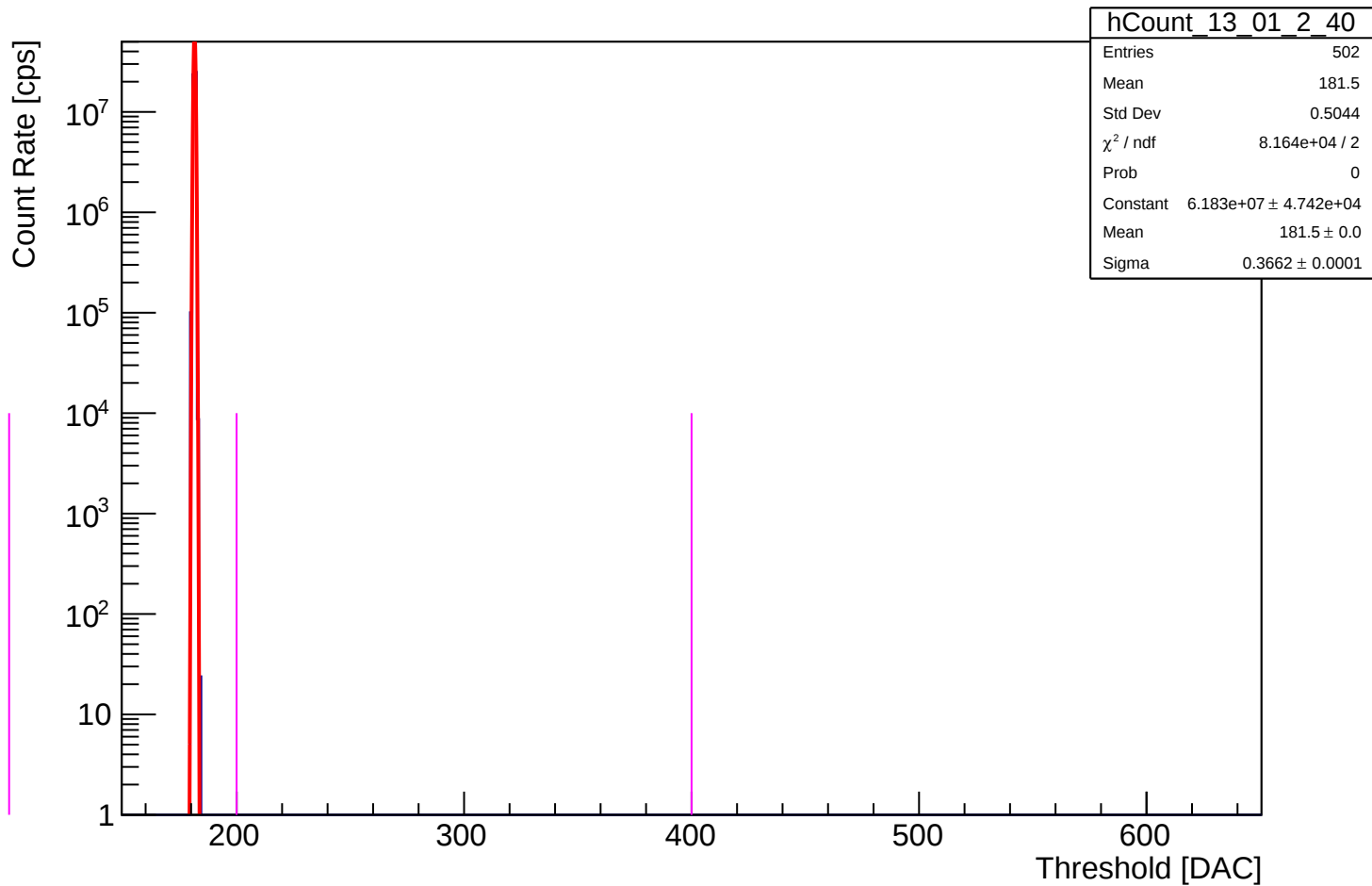
Row 1 Tile 1 Pmt 6 Pixel 19 Slot 13 Fiber 1 Asic 2 Channel 22



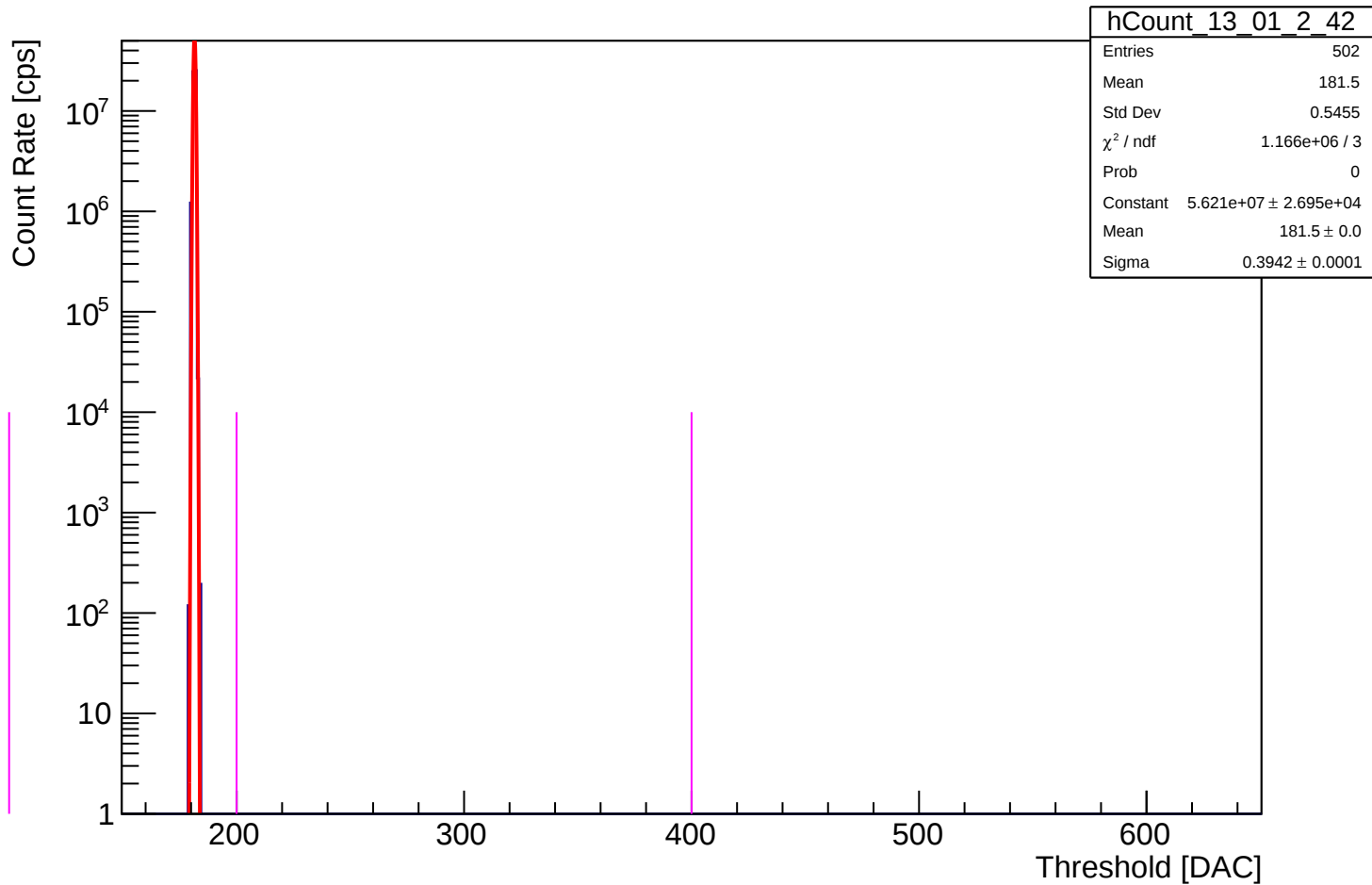
Row 1 Tile 1 Pmt 6 Pixel 20 Slot 13 Fiber 1 Asic 2 Channel 20



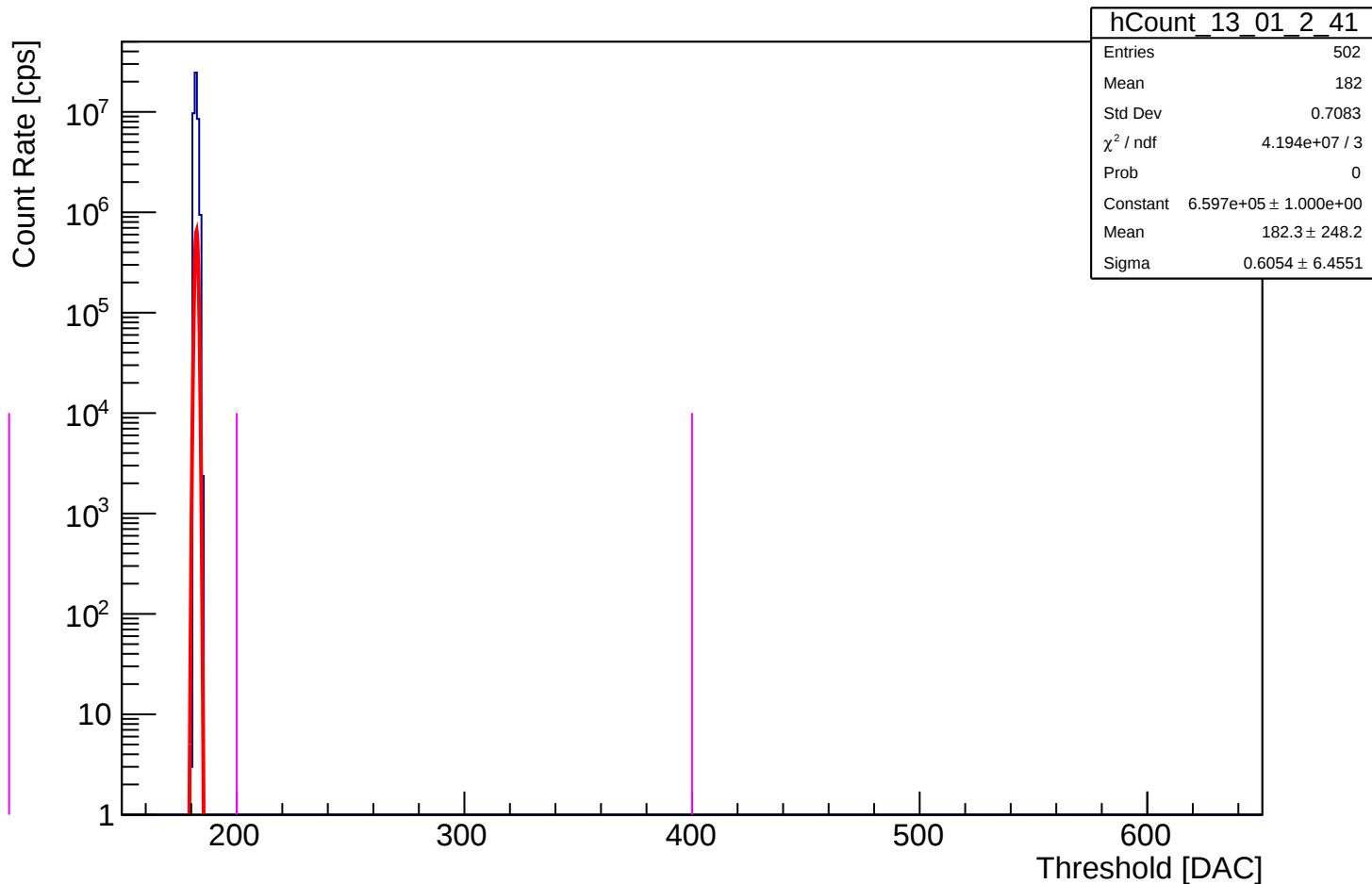
Row 1 Tile 1 Pmt 6 Pixel 21 Slot 13 Fiber 1 Asic 2 Channel 40



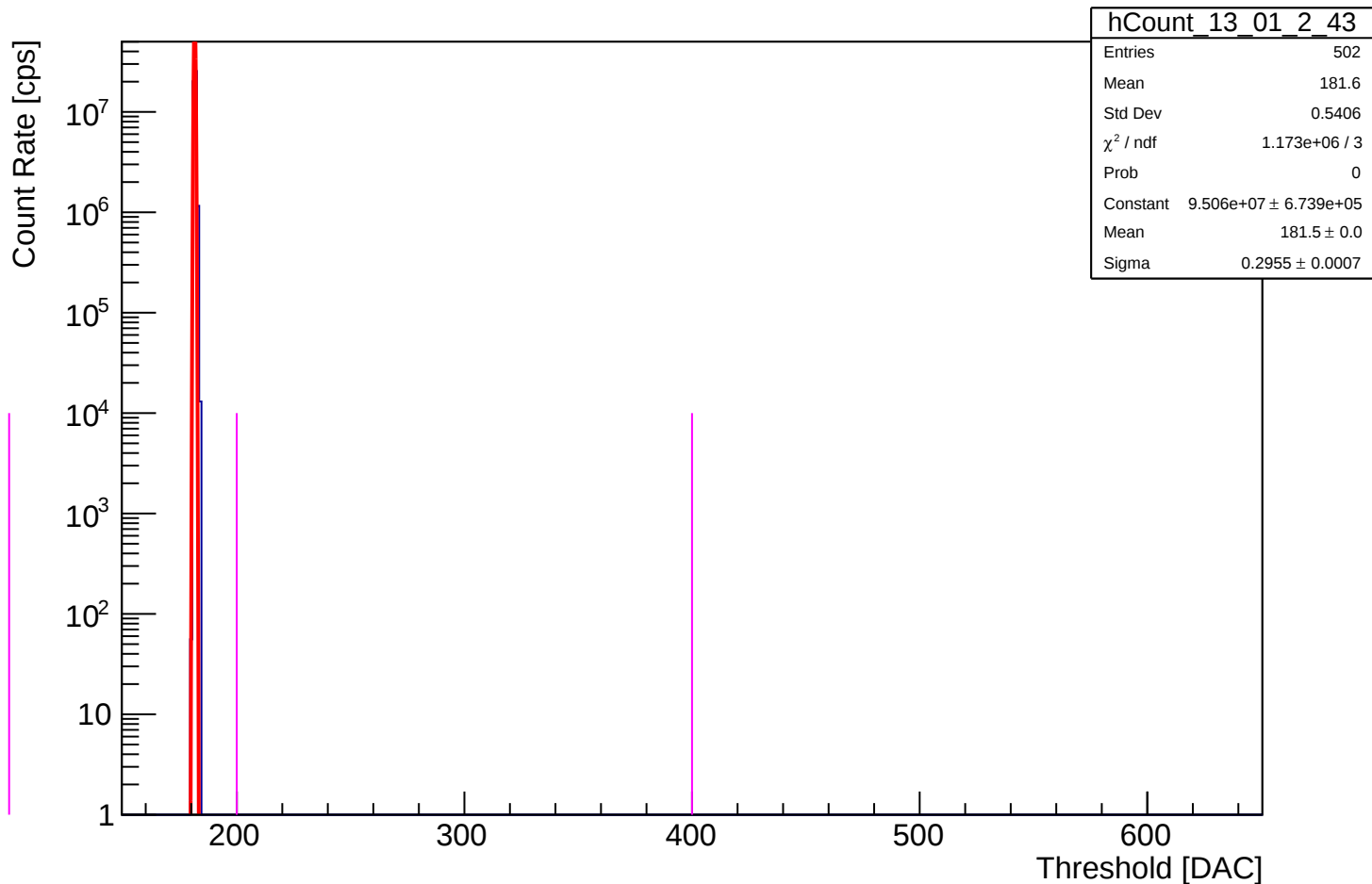
Row 1 Tile 1 Pmt 6 Pixel 22 Slot 13 Fiber 1 Asic 2 Channel 42



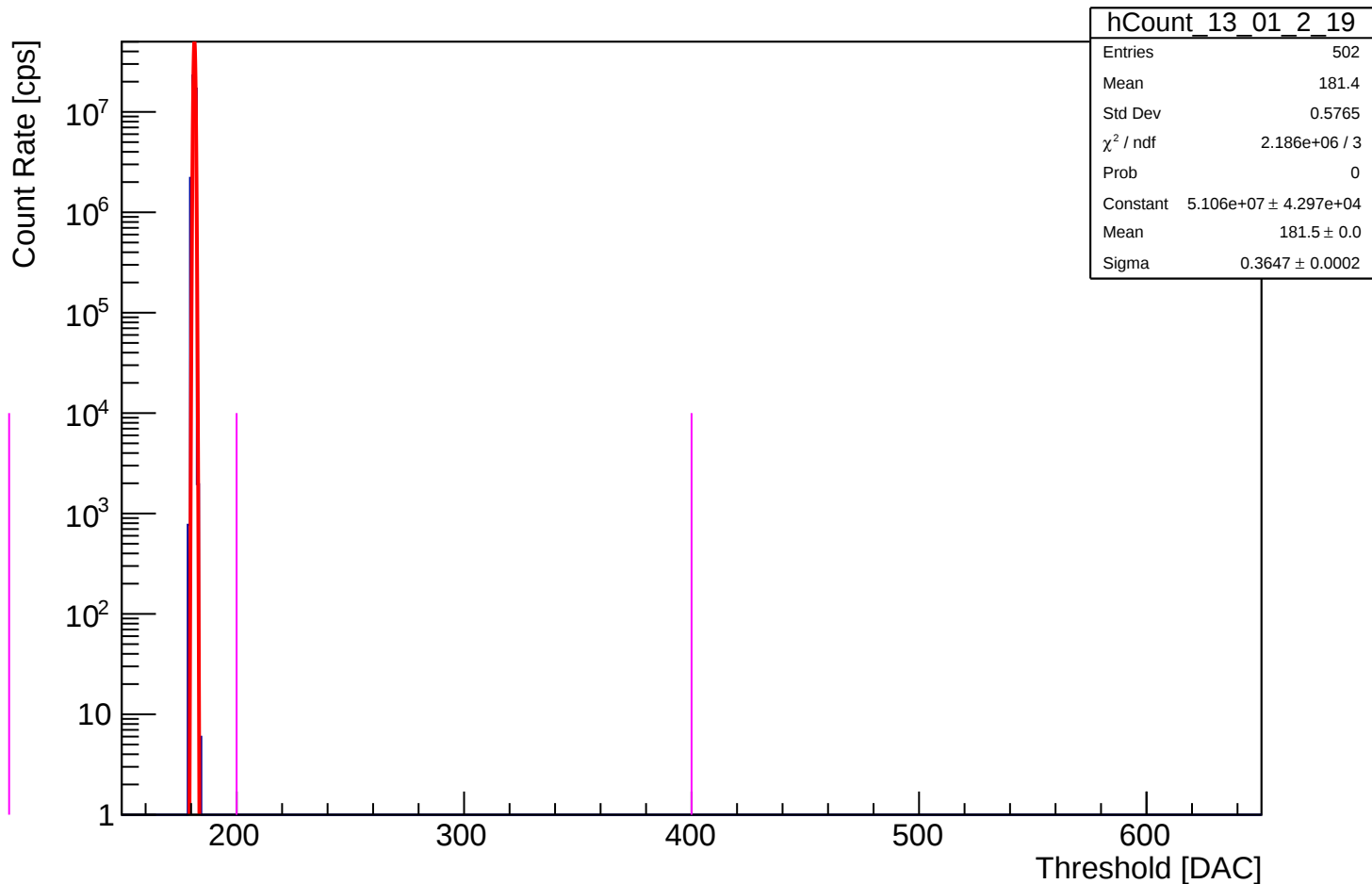
Row 1 Tile 1 Pmt 6 Pixel 23 Slot 13 Fiber 1 Asic 2 Channel 41



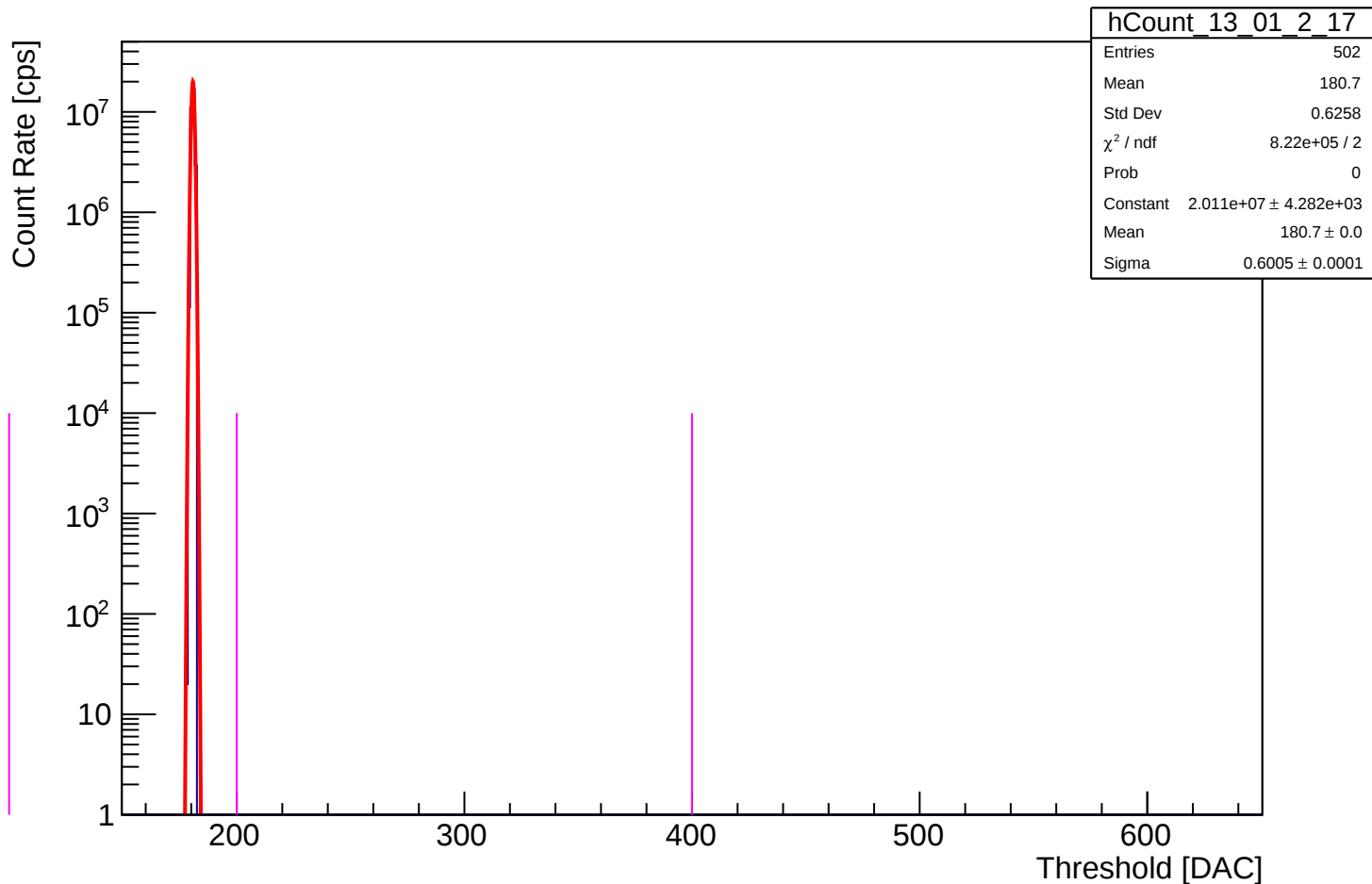
Row 1 Tile 1 Pmt 6 Pixel 24 Slot 13 Fiber 1 Asic 2 Channel 43



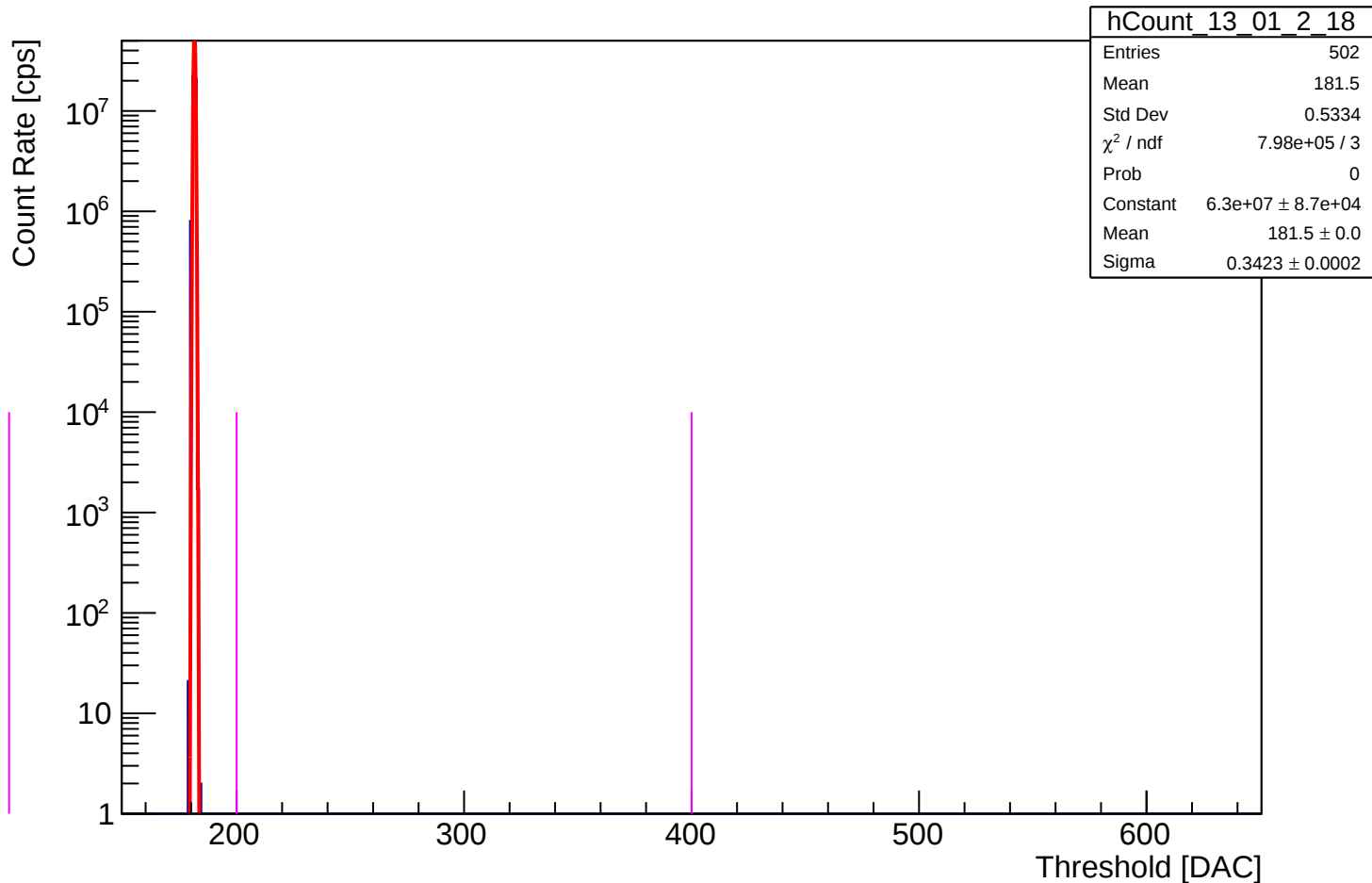
Row 1 Tile 1 Pmt 6 Pixel 25 Slot 13 Fiber 1 Asic 2 Channel 19



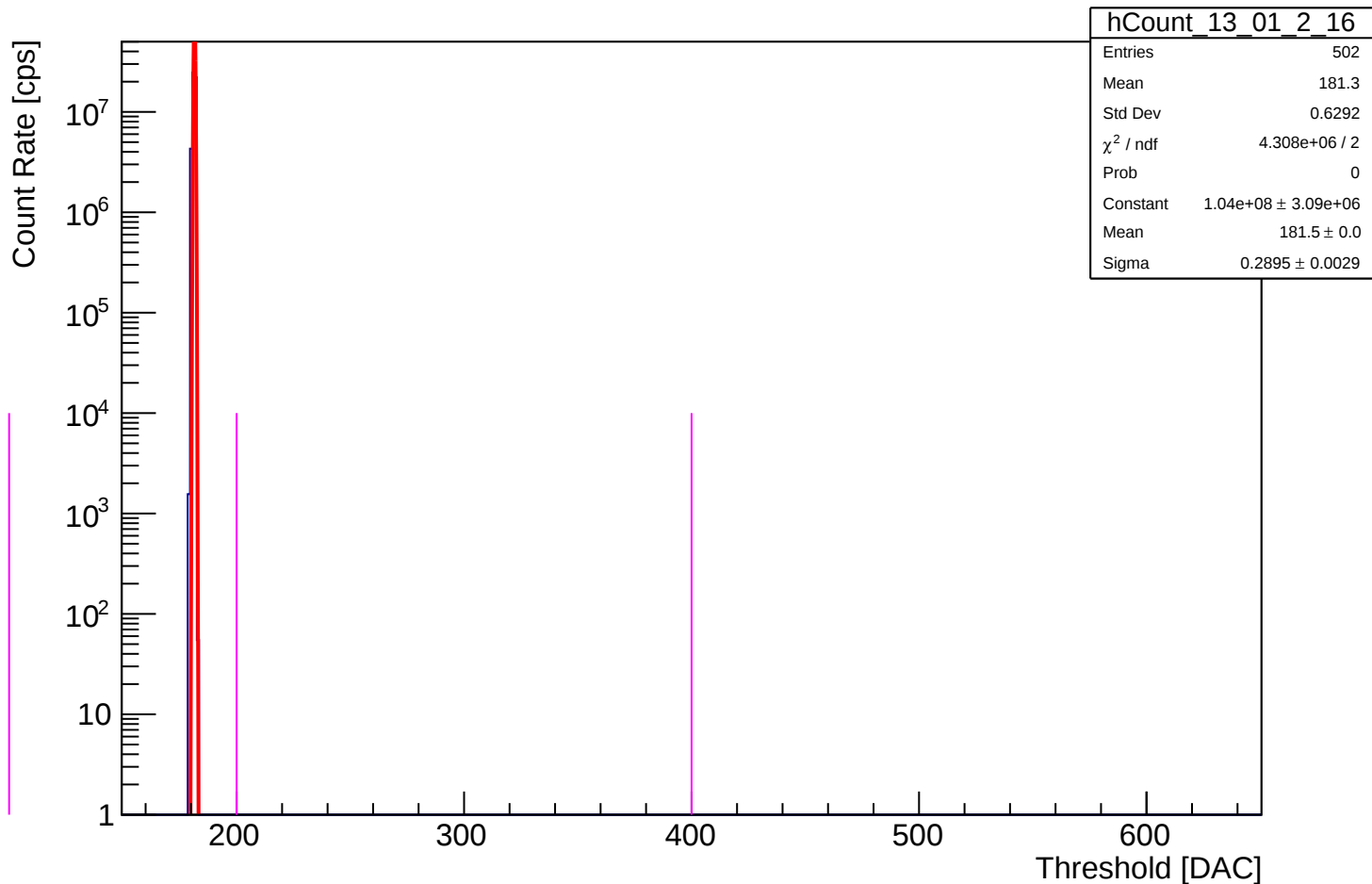
Row 1 Tile 1 Pmt 6 Pixel 26 Slot 13 Fiber 1 Asic 2 Channel 17



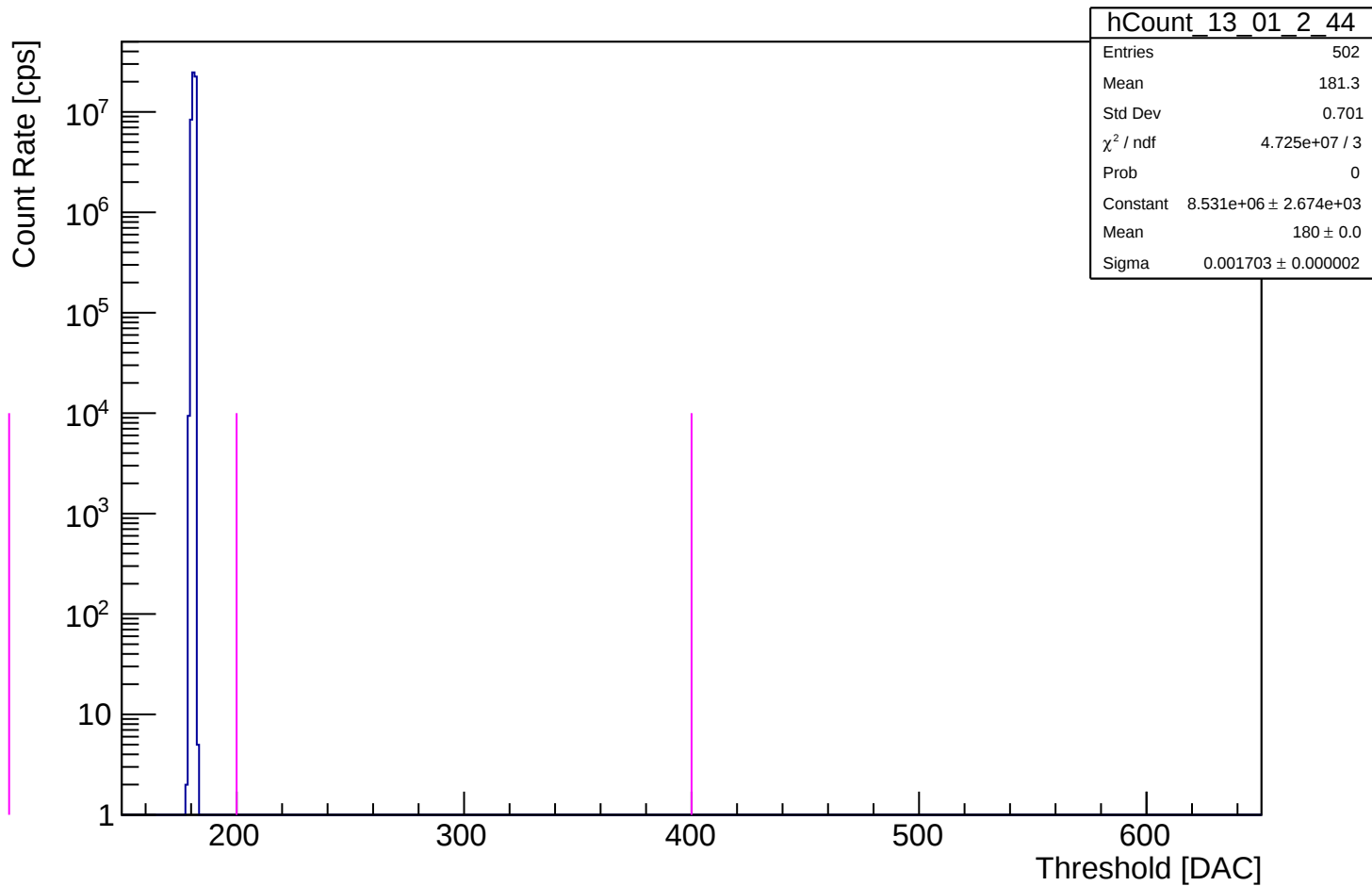
Row 1 Tile 1 Pmt 6 Pixel 27 Slot 13 Fiber 1 Asic 2 Channel 18



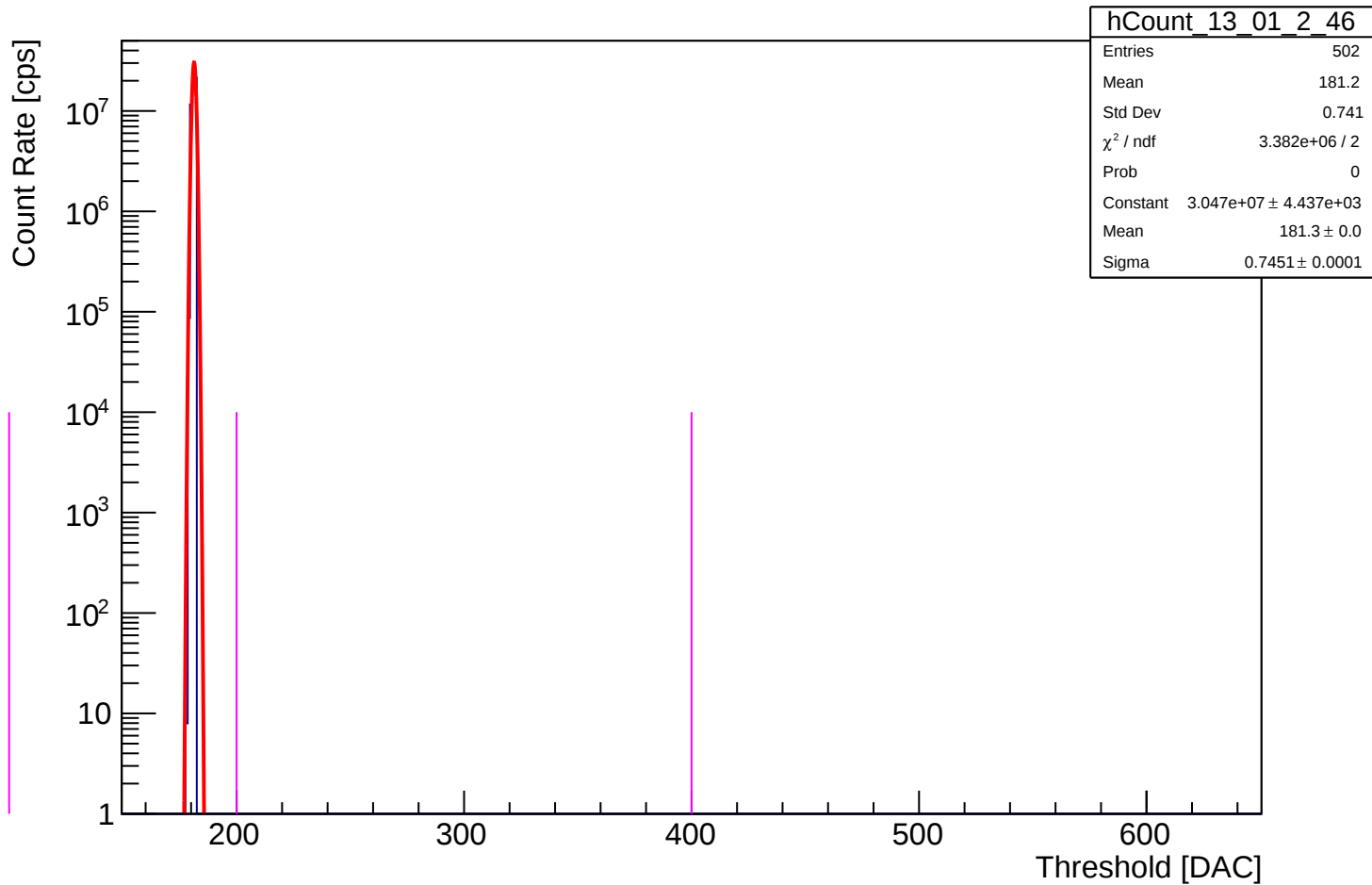
Row 1 Tile 1 Pmt 6 Pixel 28 Slot 13 Fiber 1 Asic 2 Channel 16



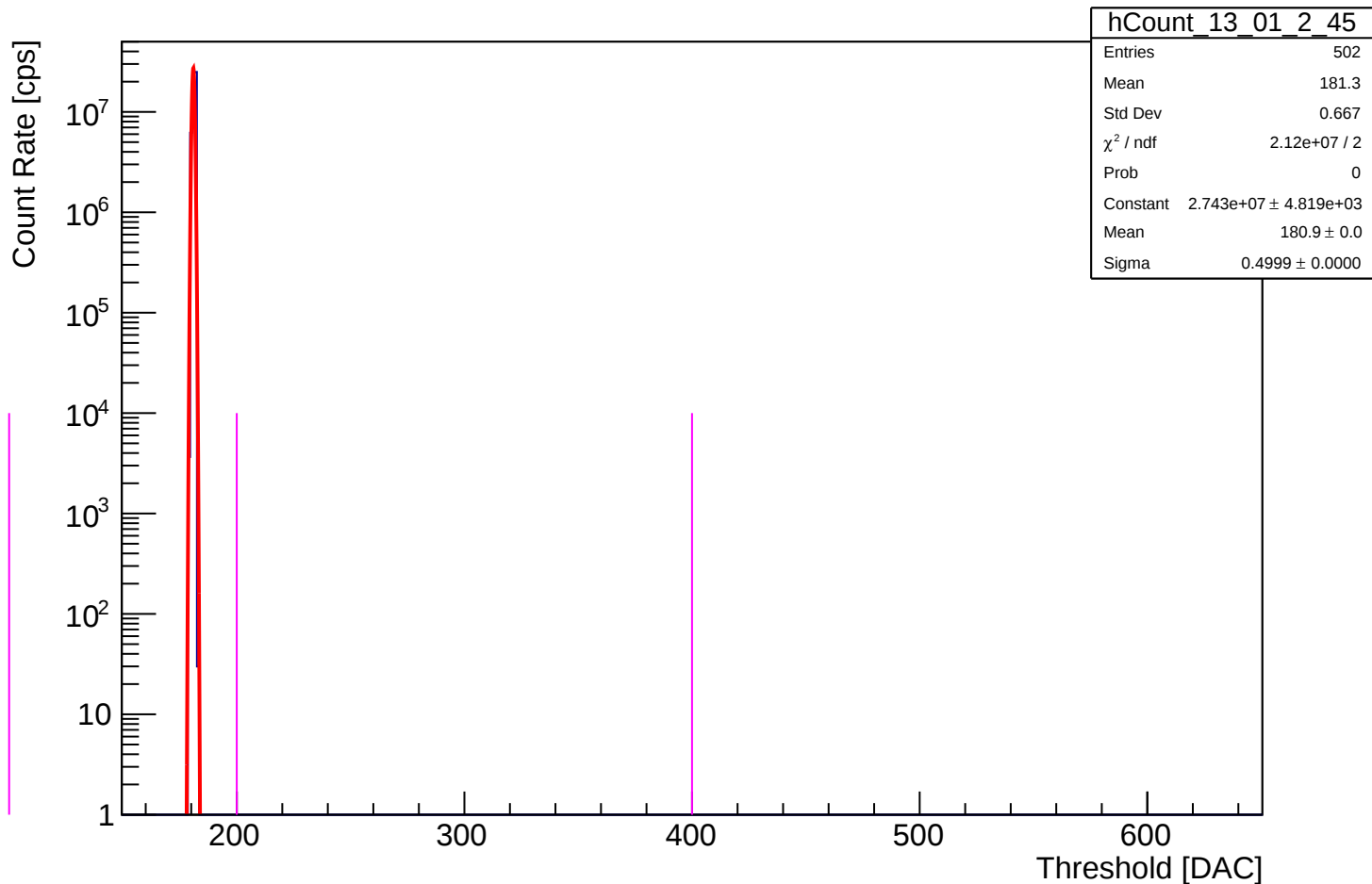
Row 1 Tile 1 Pmt 6 Pixel 29 Slot 13 Fiber 1 Asic 2 Channel 44



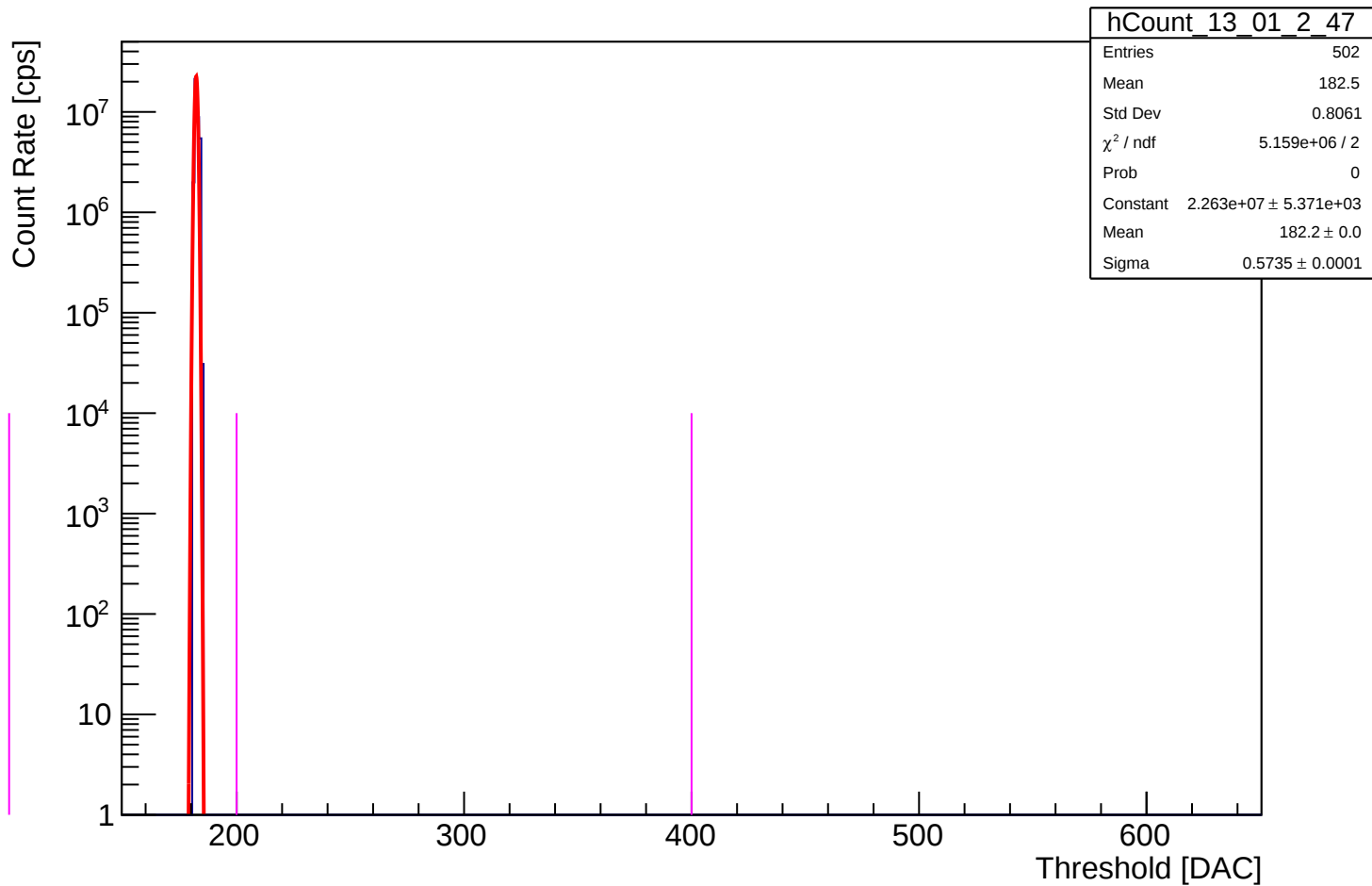
Row 1 Tile 1 Pmt 6 Pixel 30 Slot 13 Fiber 1 Asic 2 Channel 46



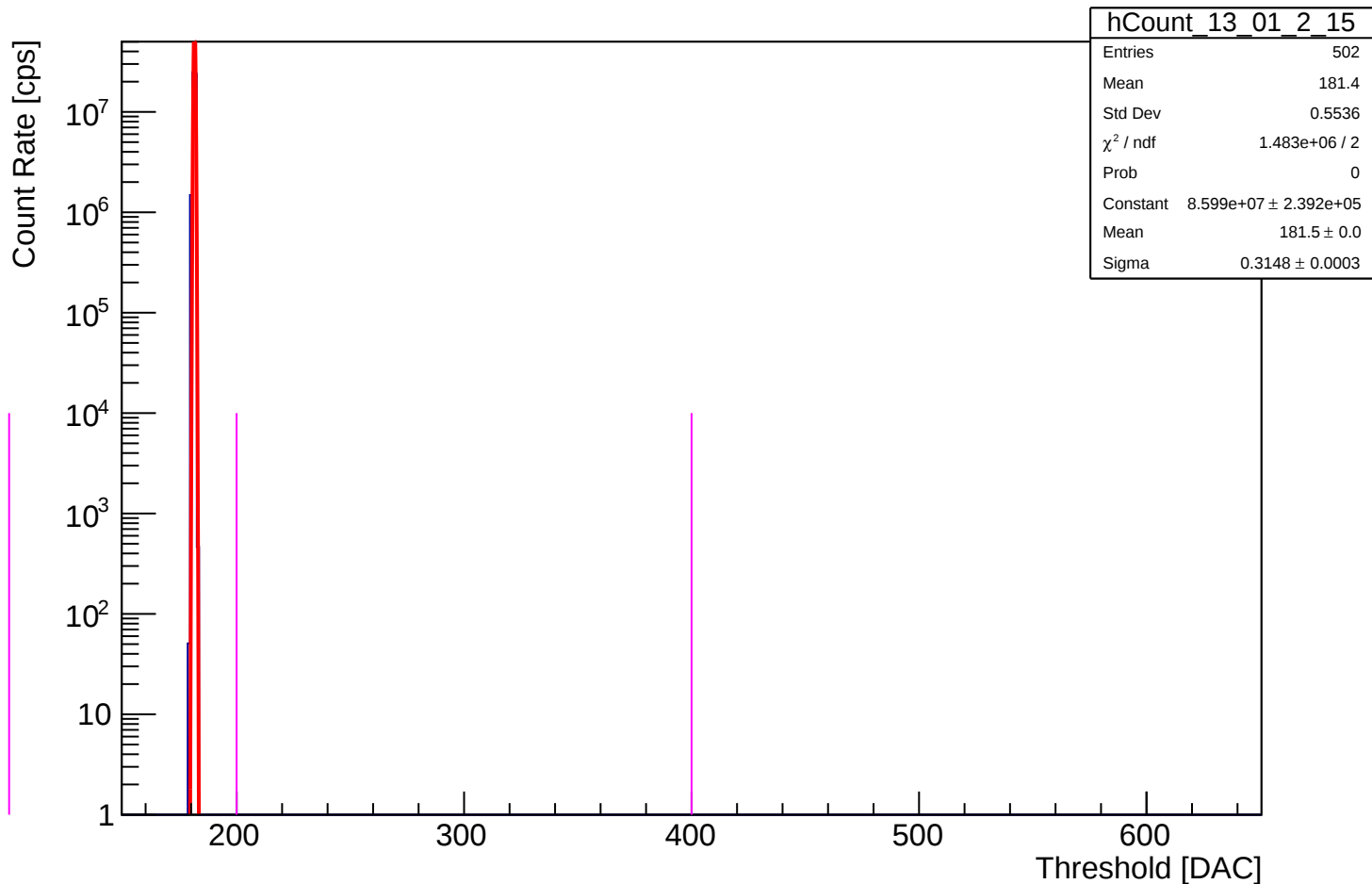
Row 1 Tile 1 Pmt 6 Pixel 31 Slot 13 Fiber 1 Asic 2 Channel 45



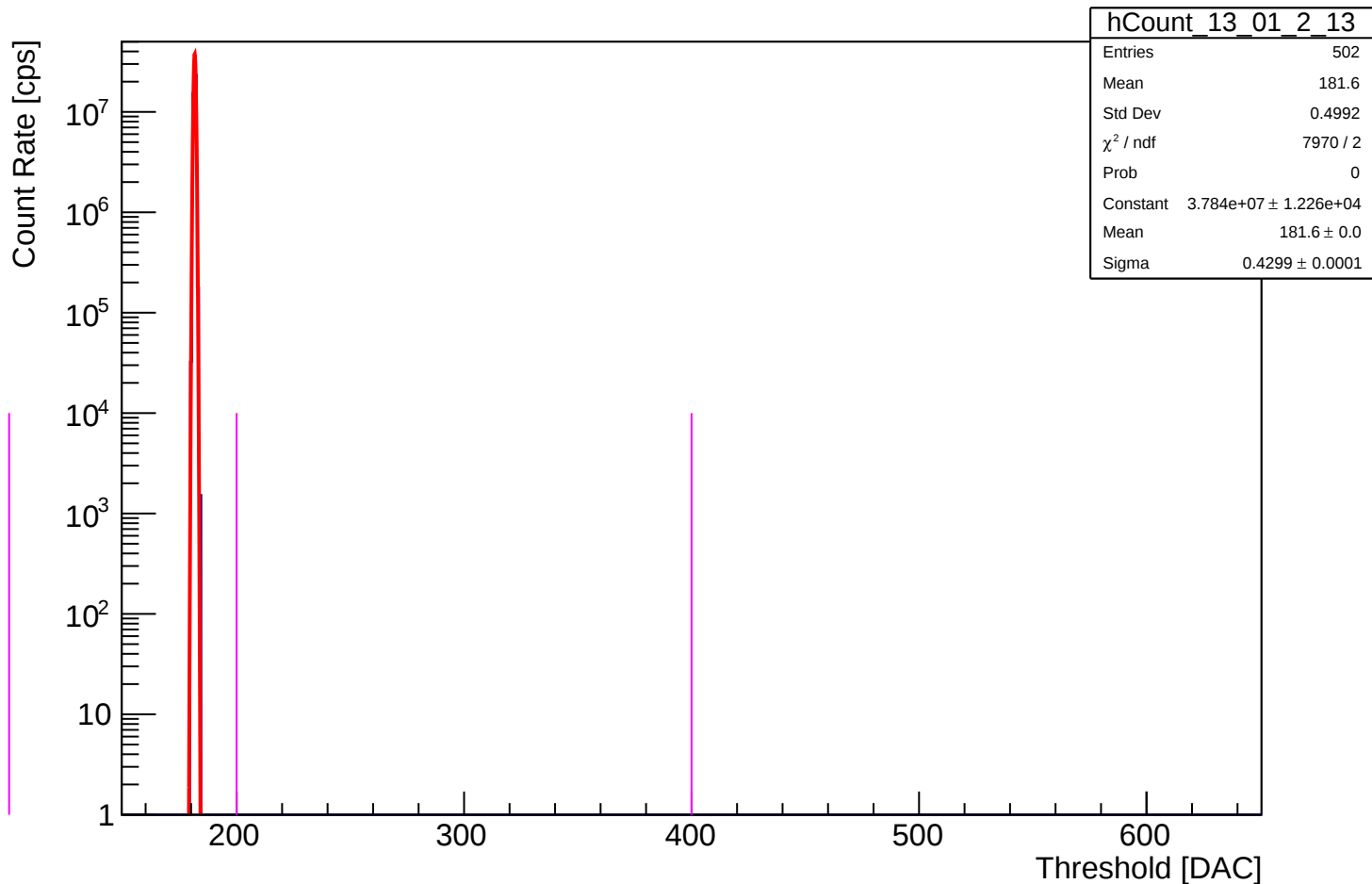
Row 1 Tile 1 Pmt 6 Pixel 32 Slot 13 Fiber 1 Asic 2 Channel 47



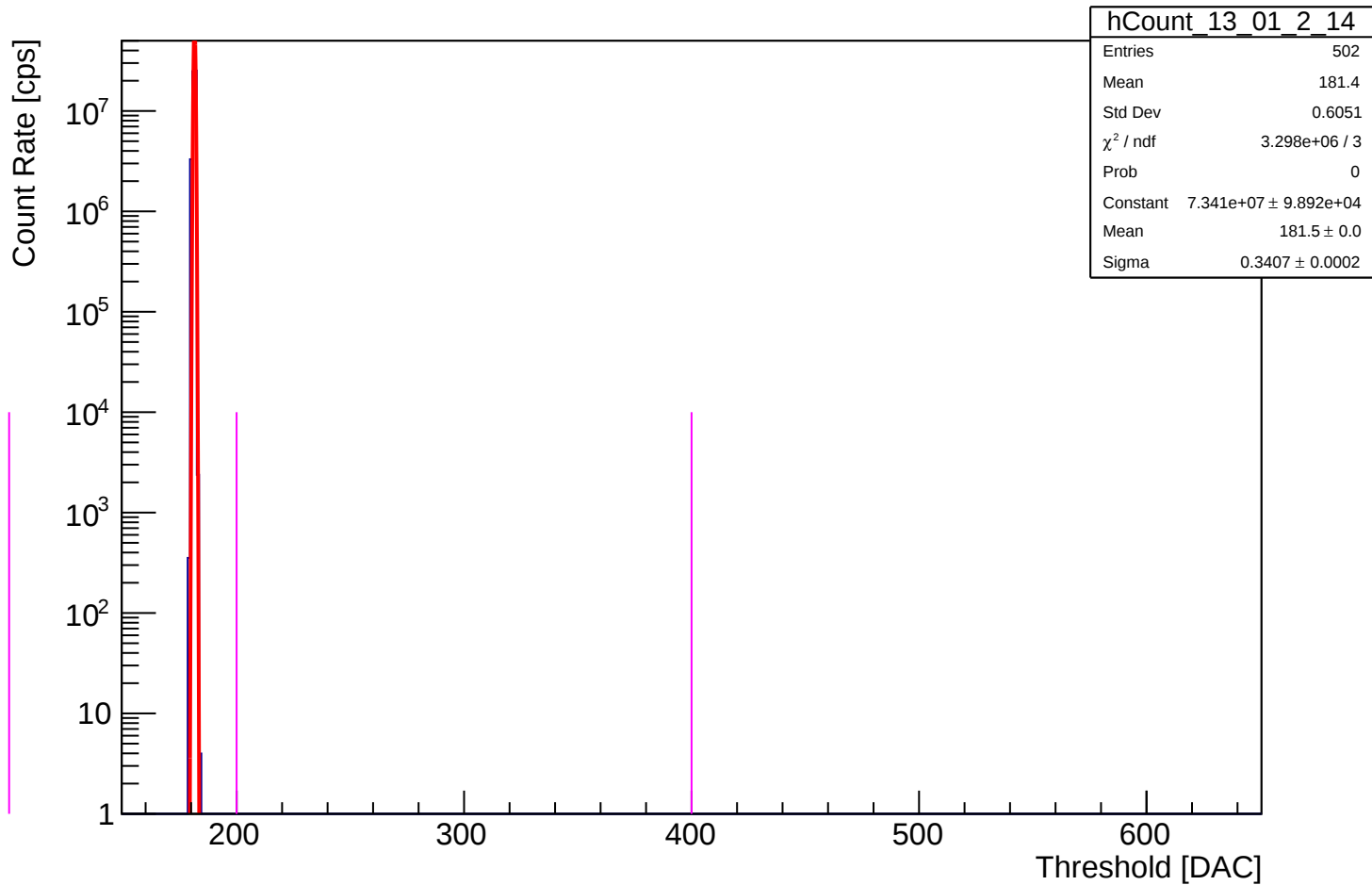
Row 1 Tile 1 Pmt 6 Pixel 33 Slot 13 Fiber 1 Asic 2 Channel 15



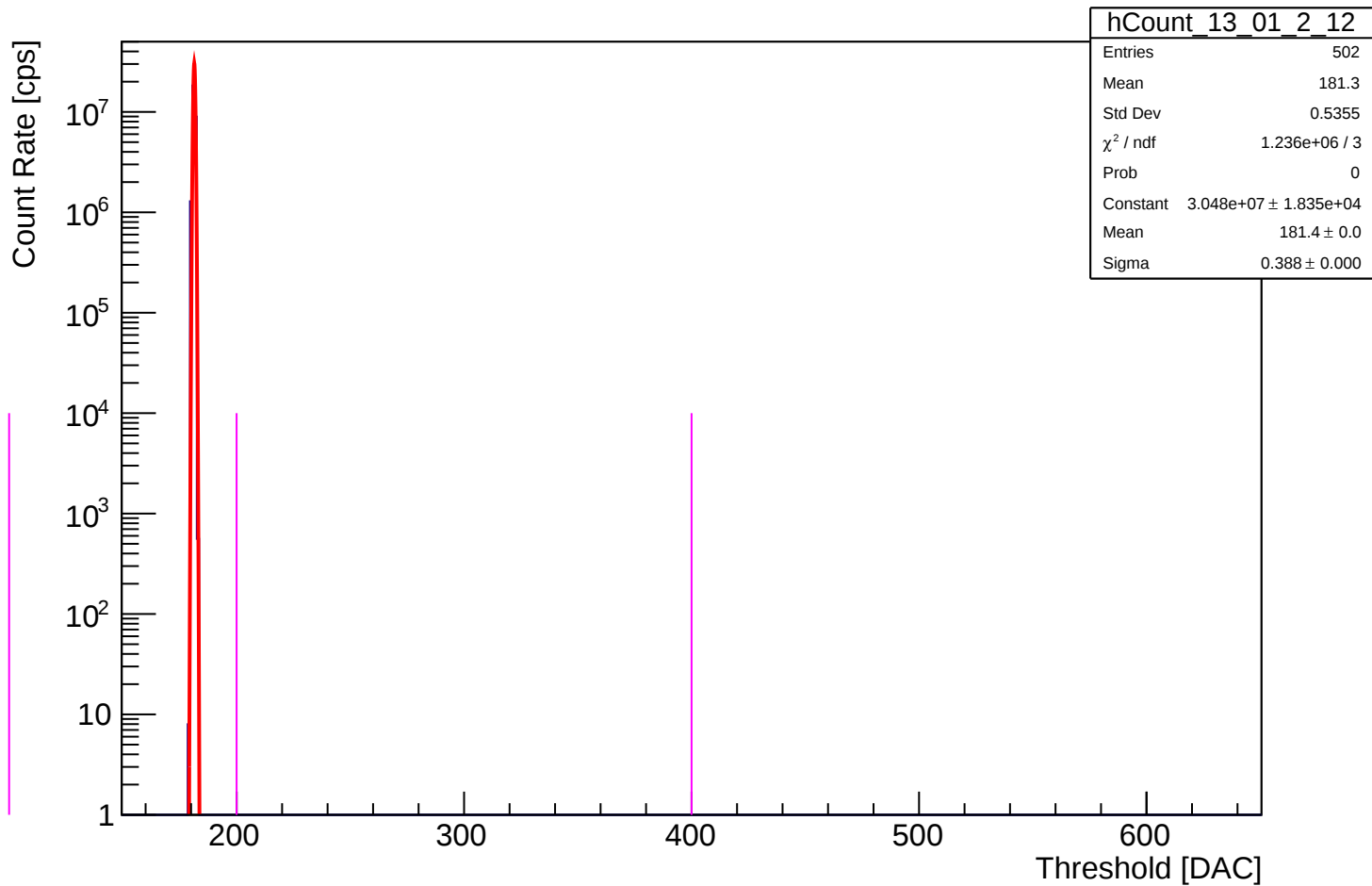
Row 1 Tile 1 Pmt 6 Pixel 34 Slot 13 Fiber 1 Asic 2 Channel 13



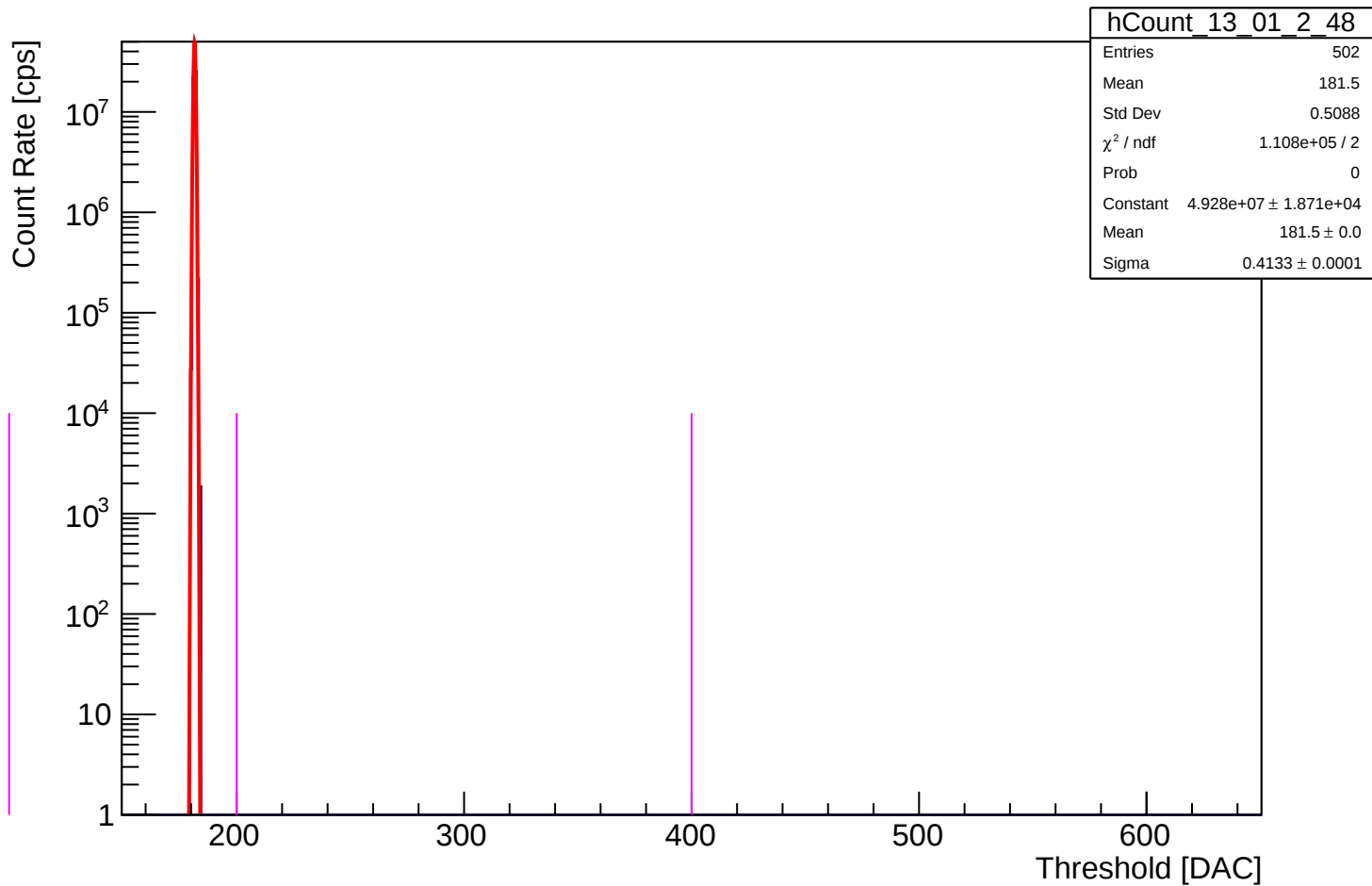
Row 1 Tile 1 Pmt 6 Pixel 35 Slot 13 Fiber 1 Asic 2 Channel 14



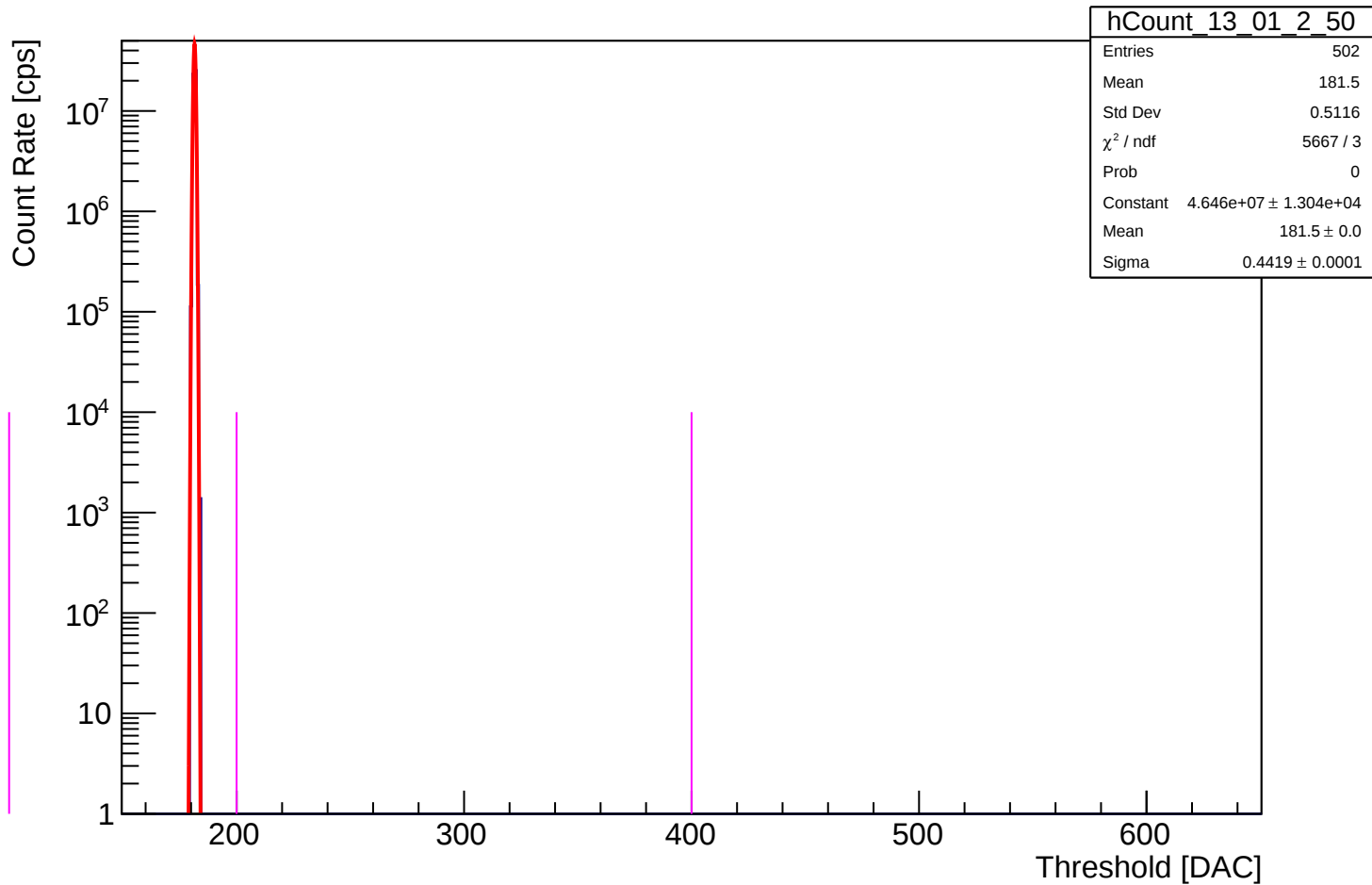
Row 1 Tile 1 Pmt 6 Pixel 36 Slot 13 Fiber 1 Asic 2 Channel 12



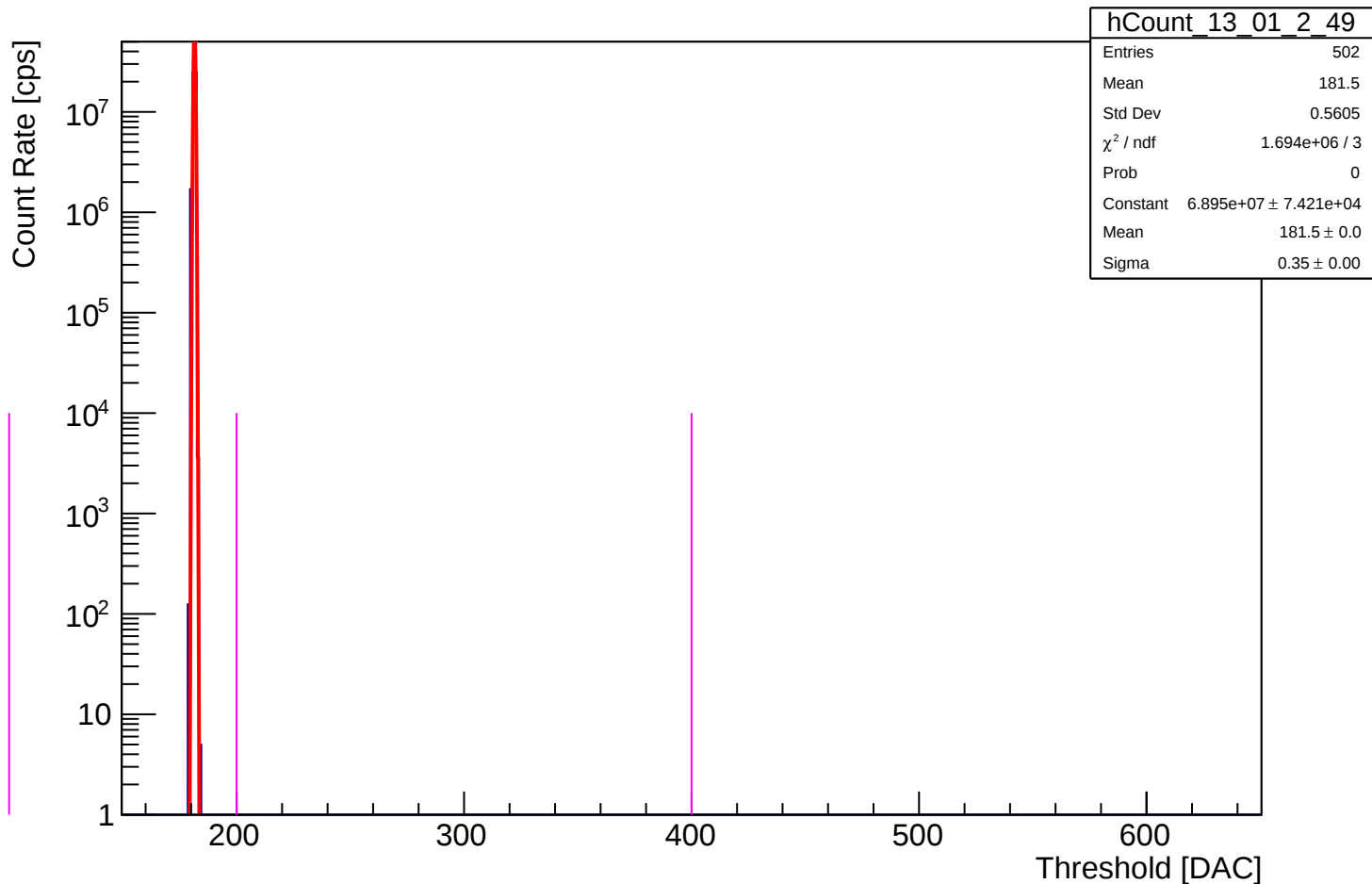
Row 1 Tile 1 Pmt 6 Pixel 37 Slot 13 Fiber 1 Asic 2 Channel 48

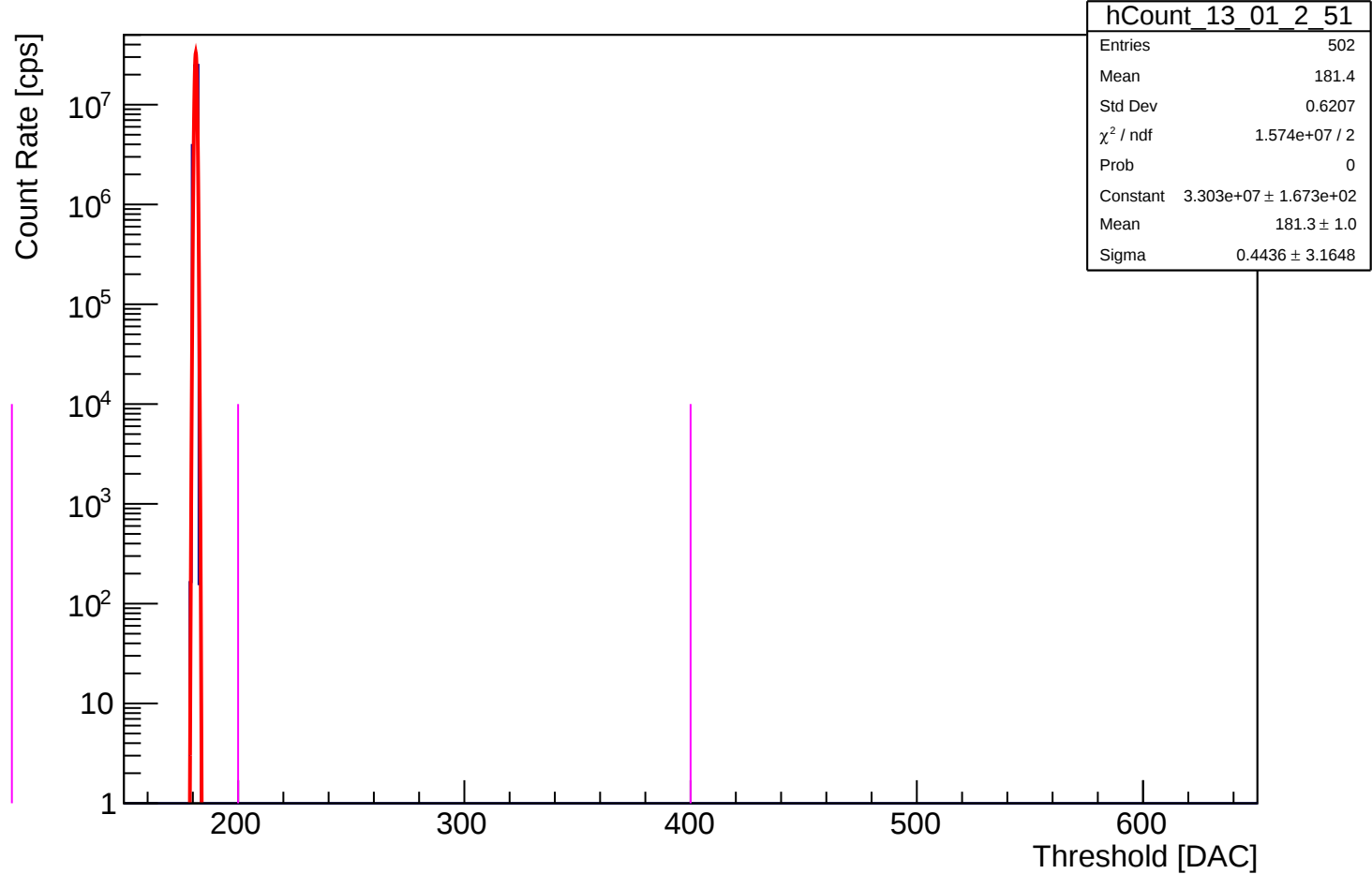


Row 1 Tile 1 Pmt 6 Pixel 38 Slot 13 Fiber 1 Asic 2 Channel 50

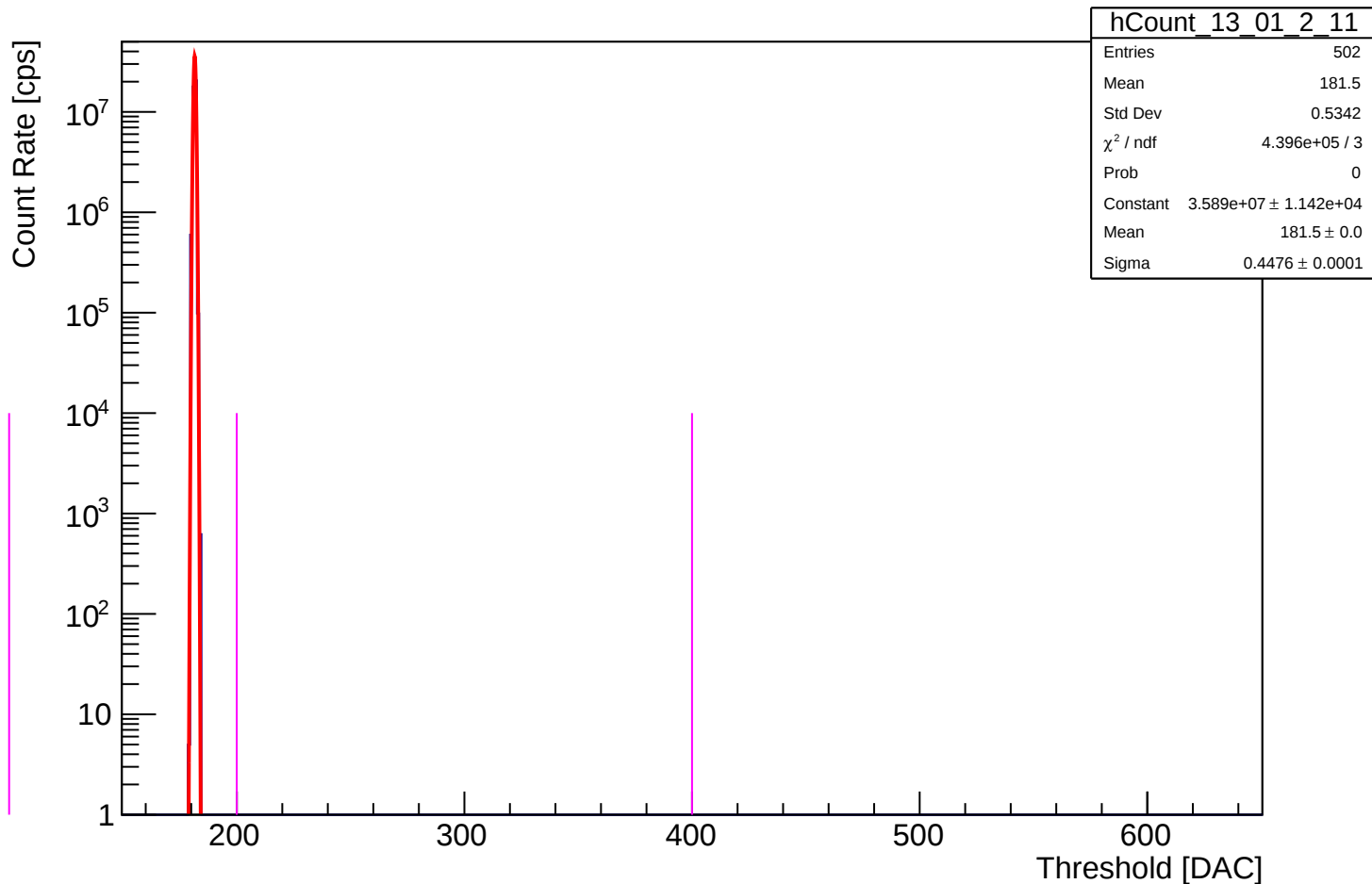


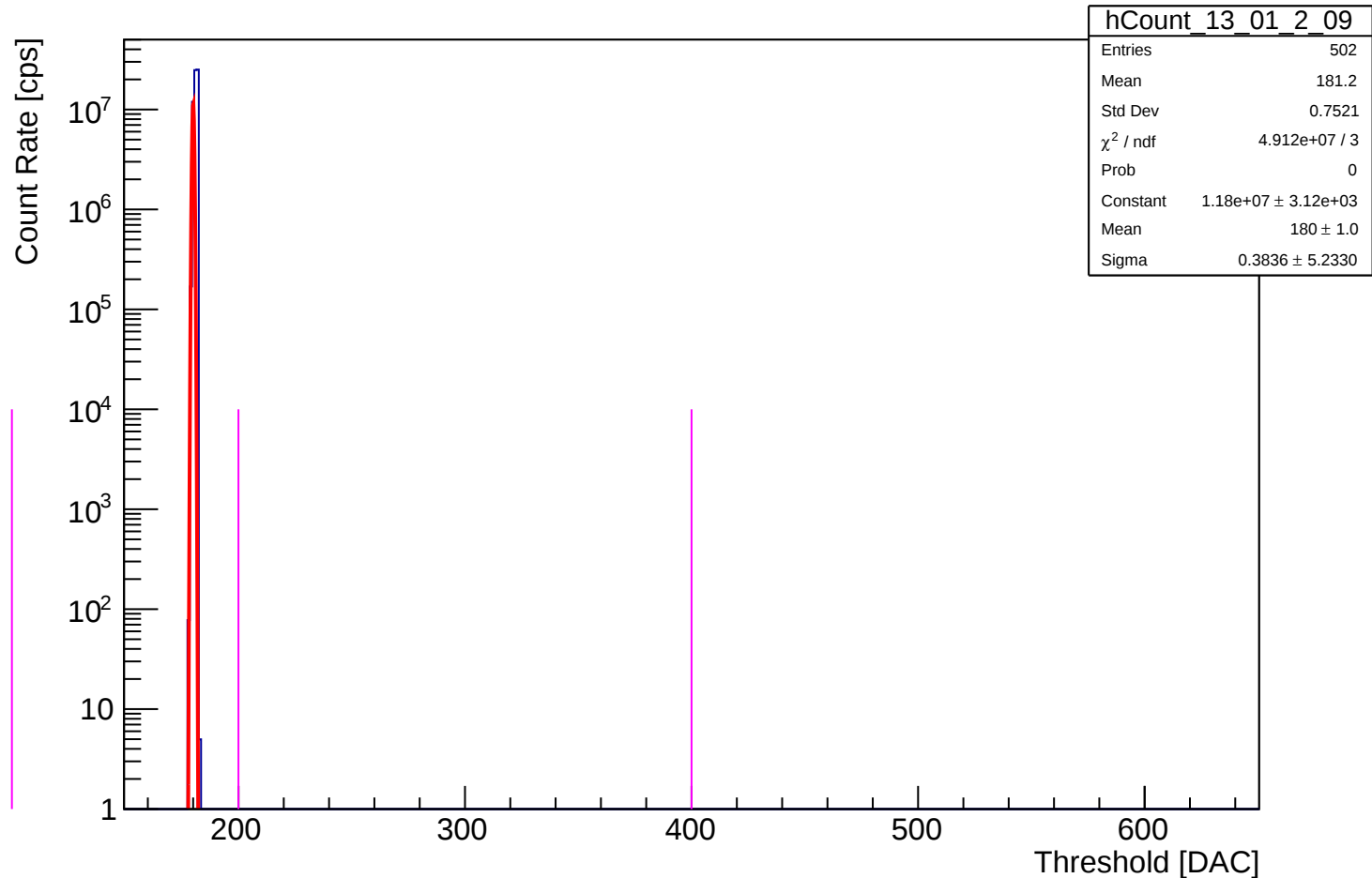
Row 1 Tile 1 Pmt 6 Pixel 39 Slot 13 Fiber 1 Asic 2 Channel 49



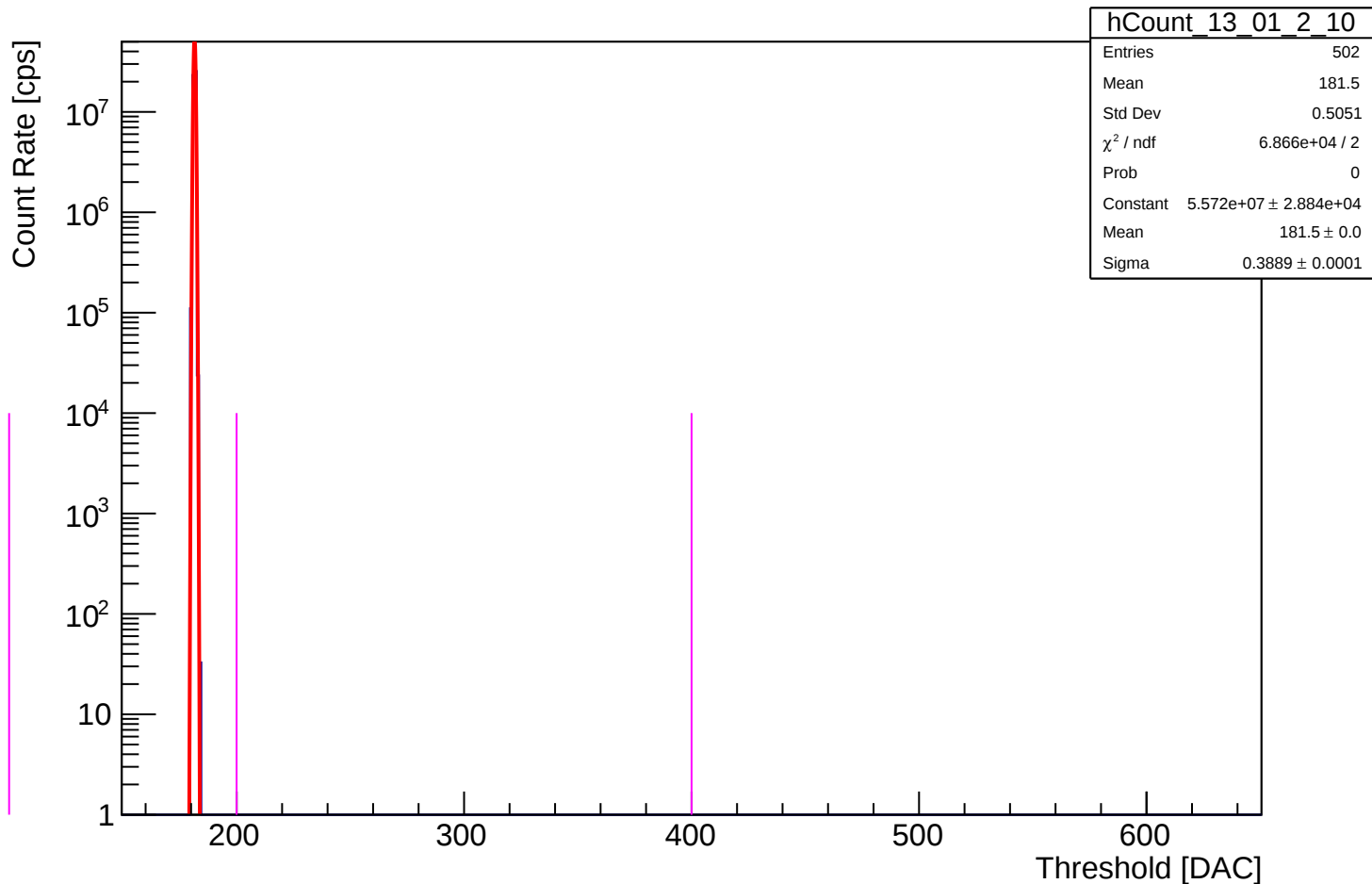


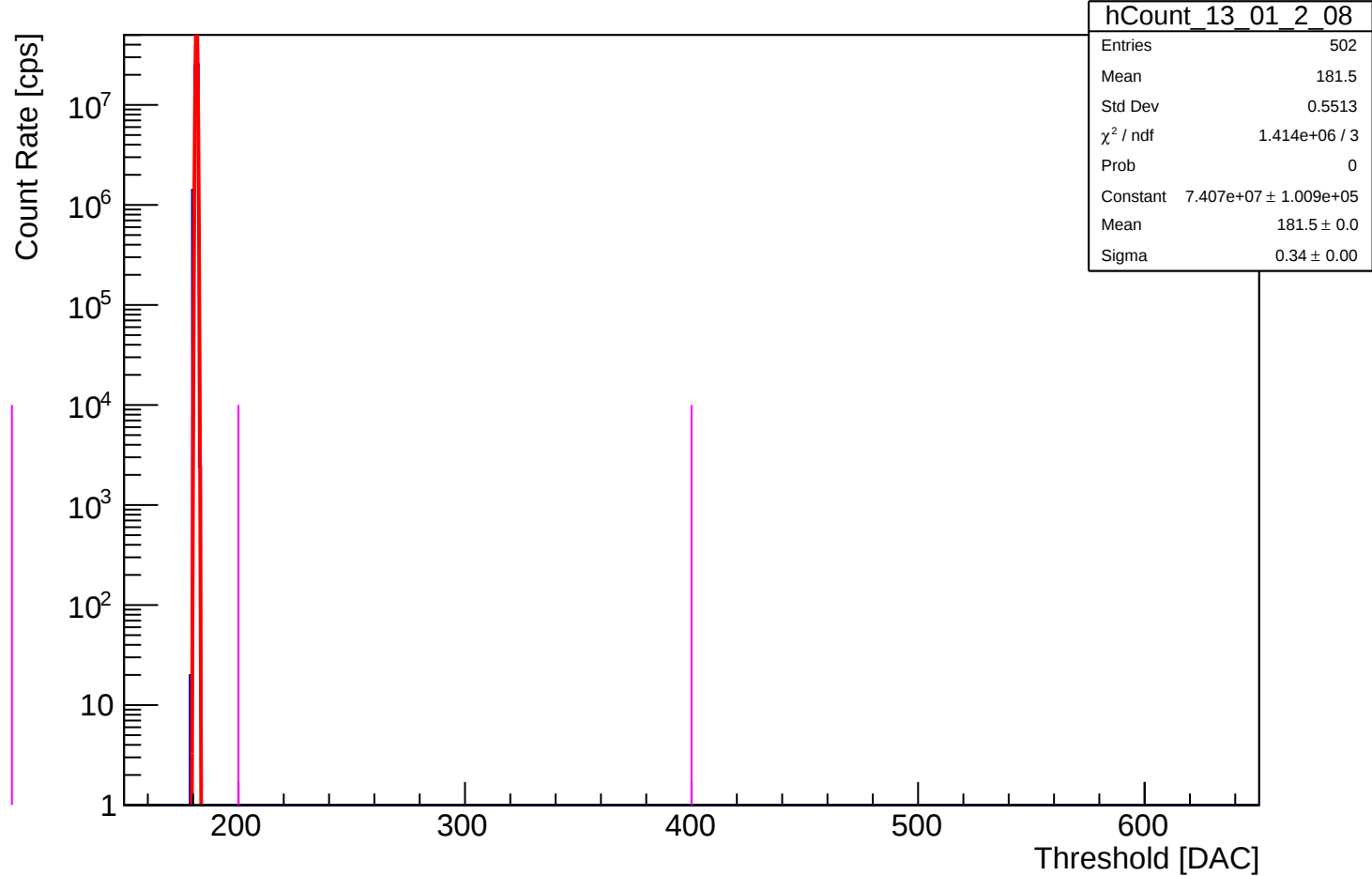
Row 1 Tile 1 Pmt 6 Pixel 41 Slot 13 Fiber 1 Asic 2 Channel 11



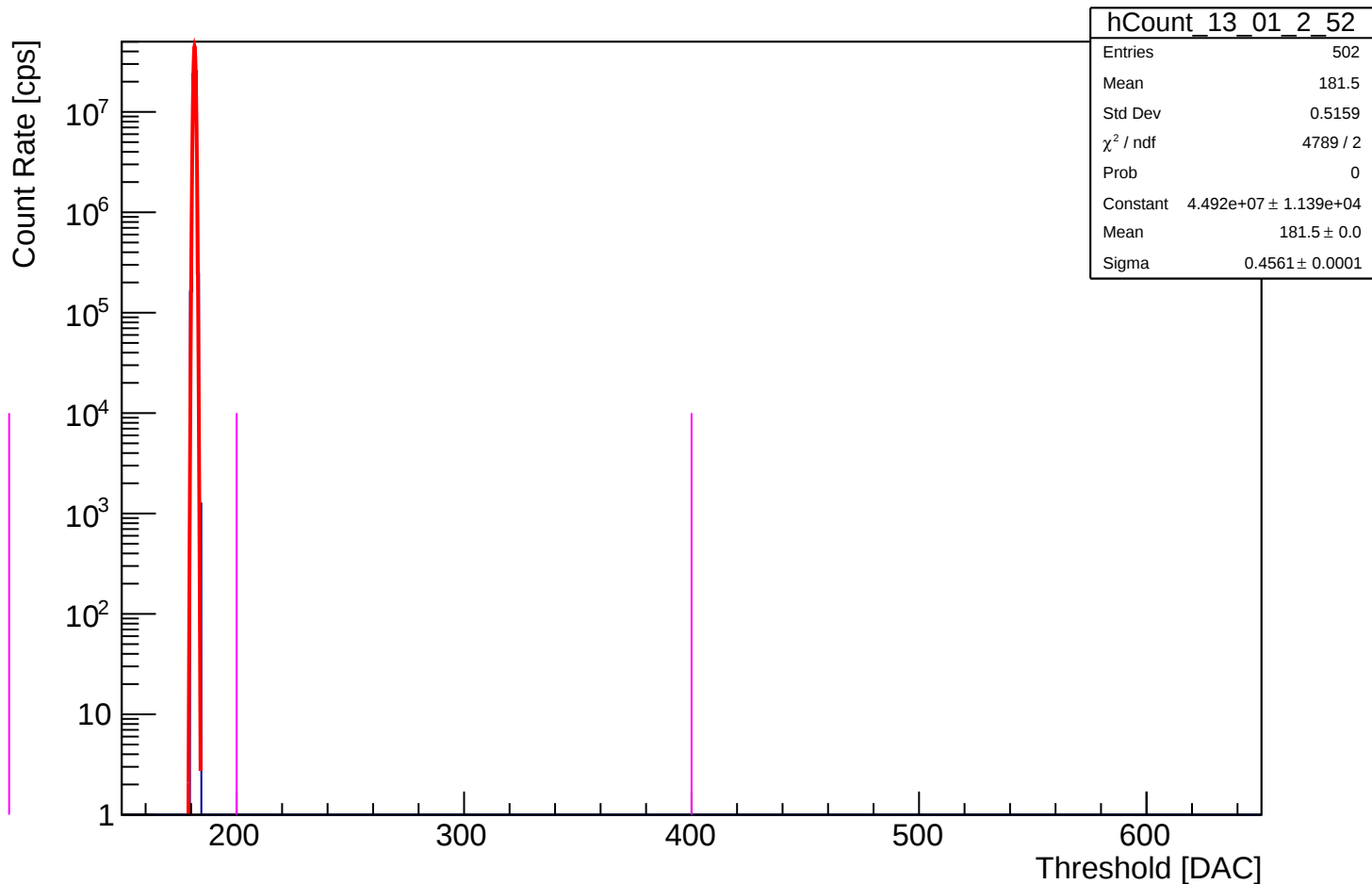


Row 1 Tile 1 Pmt 6 Pixel 43 Slot 13 Fiber 1 Asic 2 Channel 10

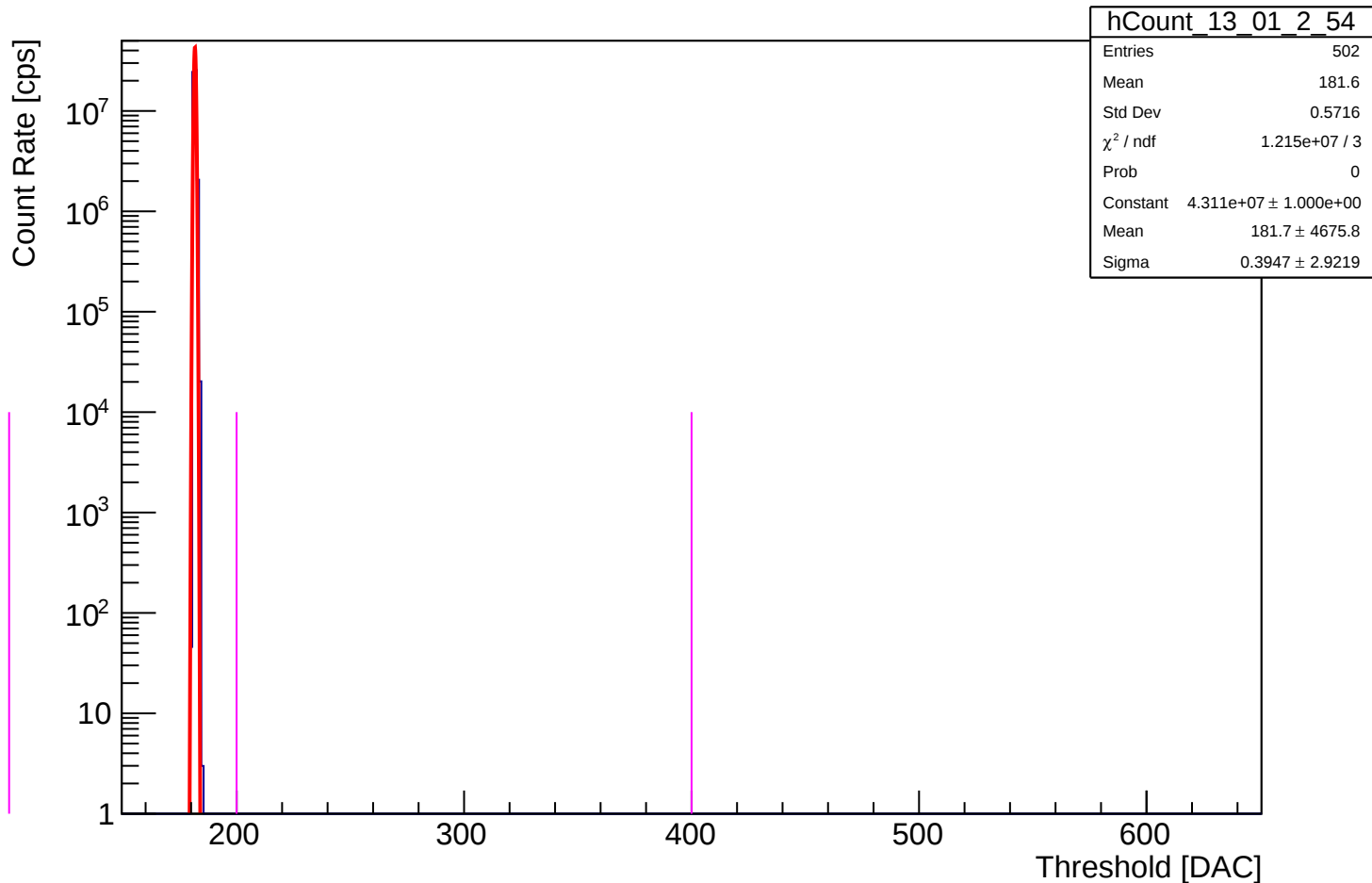




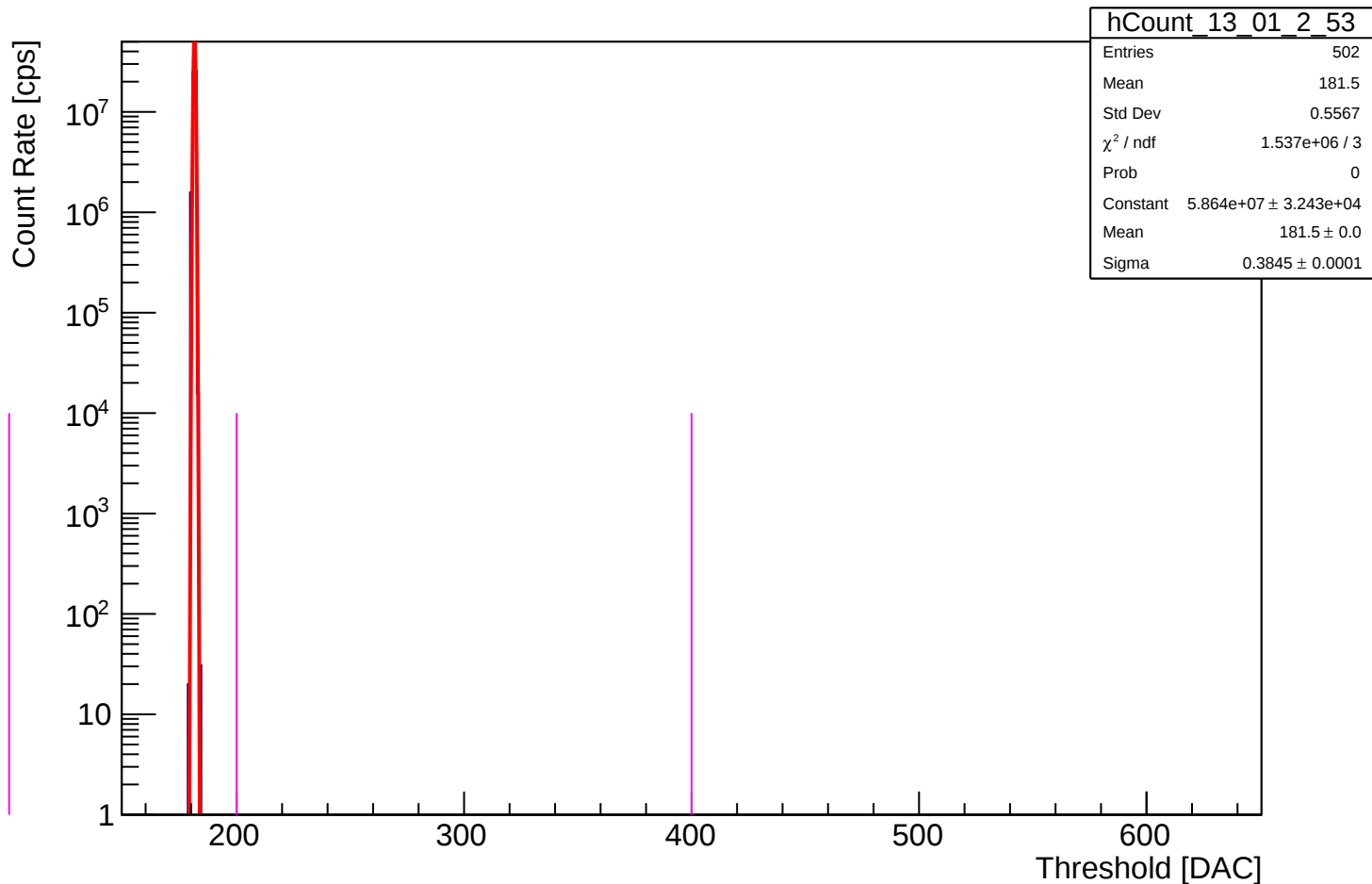
Row 1 Tile 1 Pmt 6 Pixel 45 Slot 13 Fiber 1 Asic 2 Channel 52



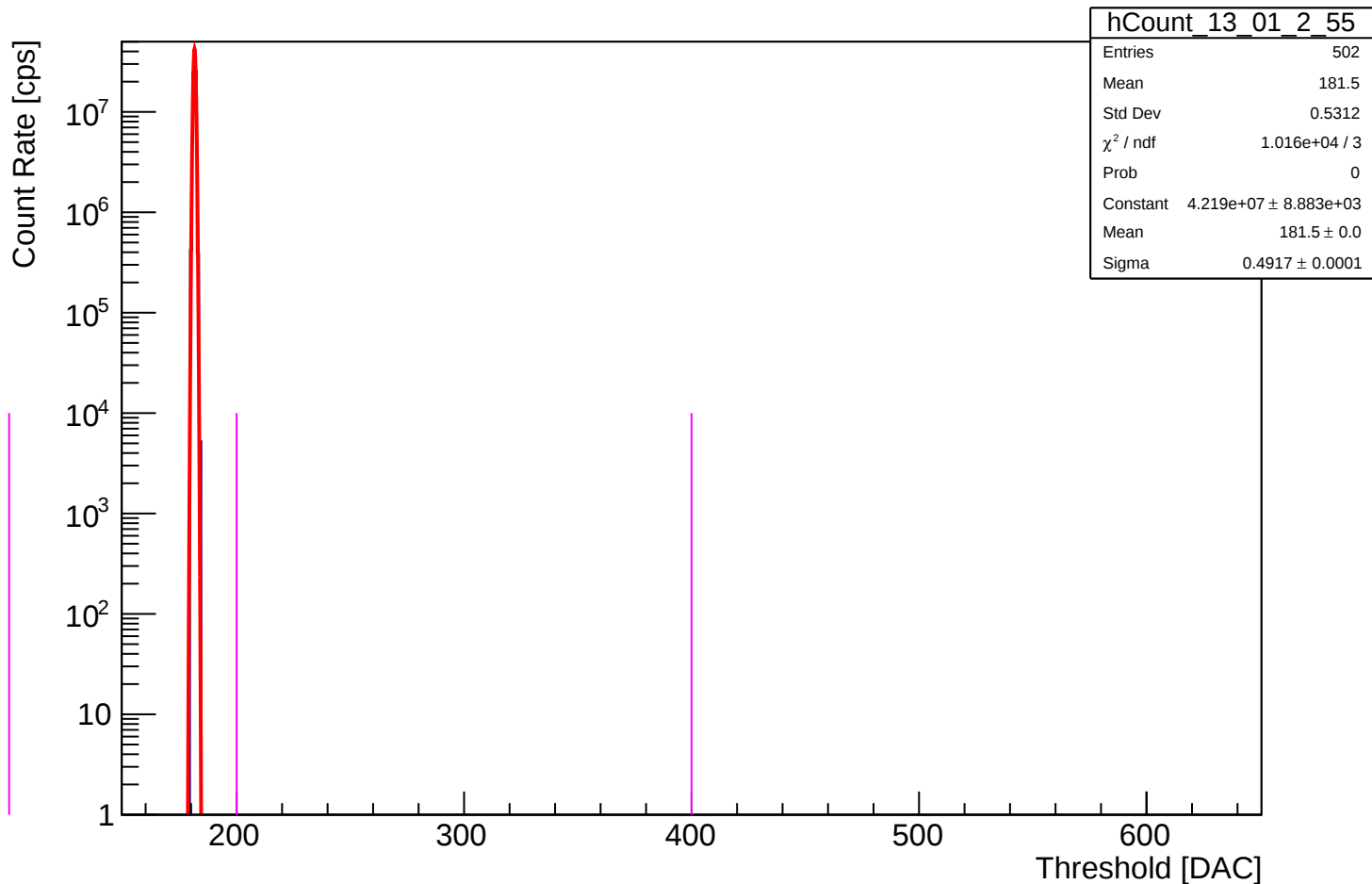
Row 1 Tile 1 Pmt 6 Pixel 46 Slot 13 Fiber 1 Asic 2 Channel 54

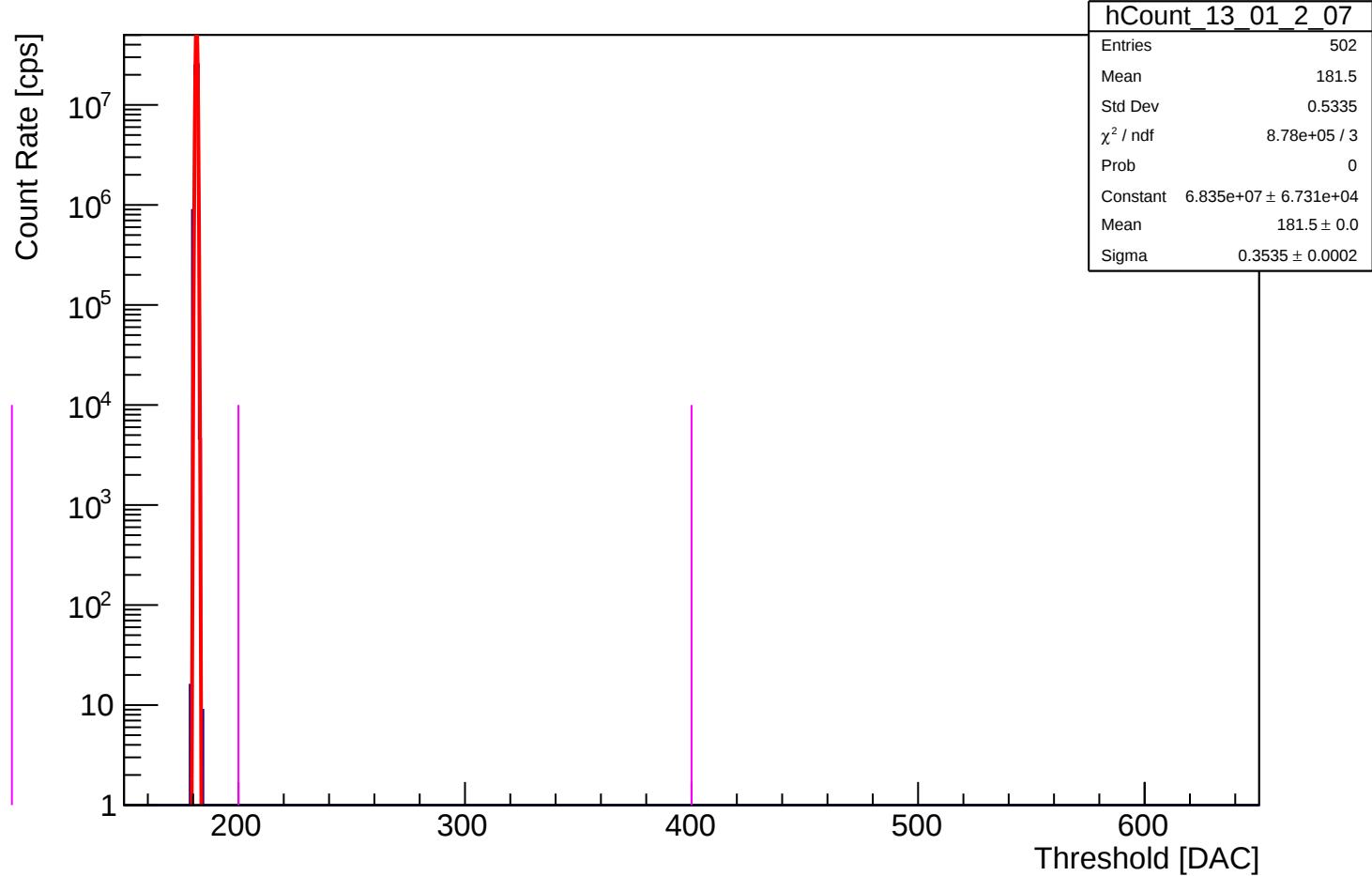


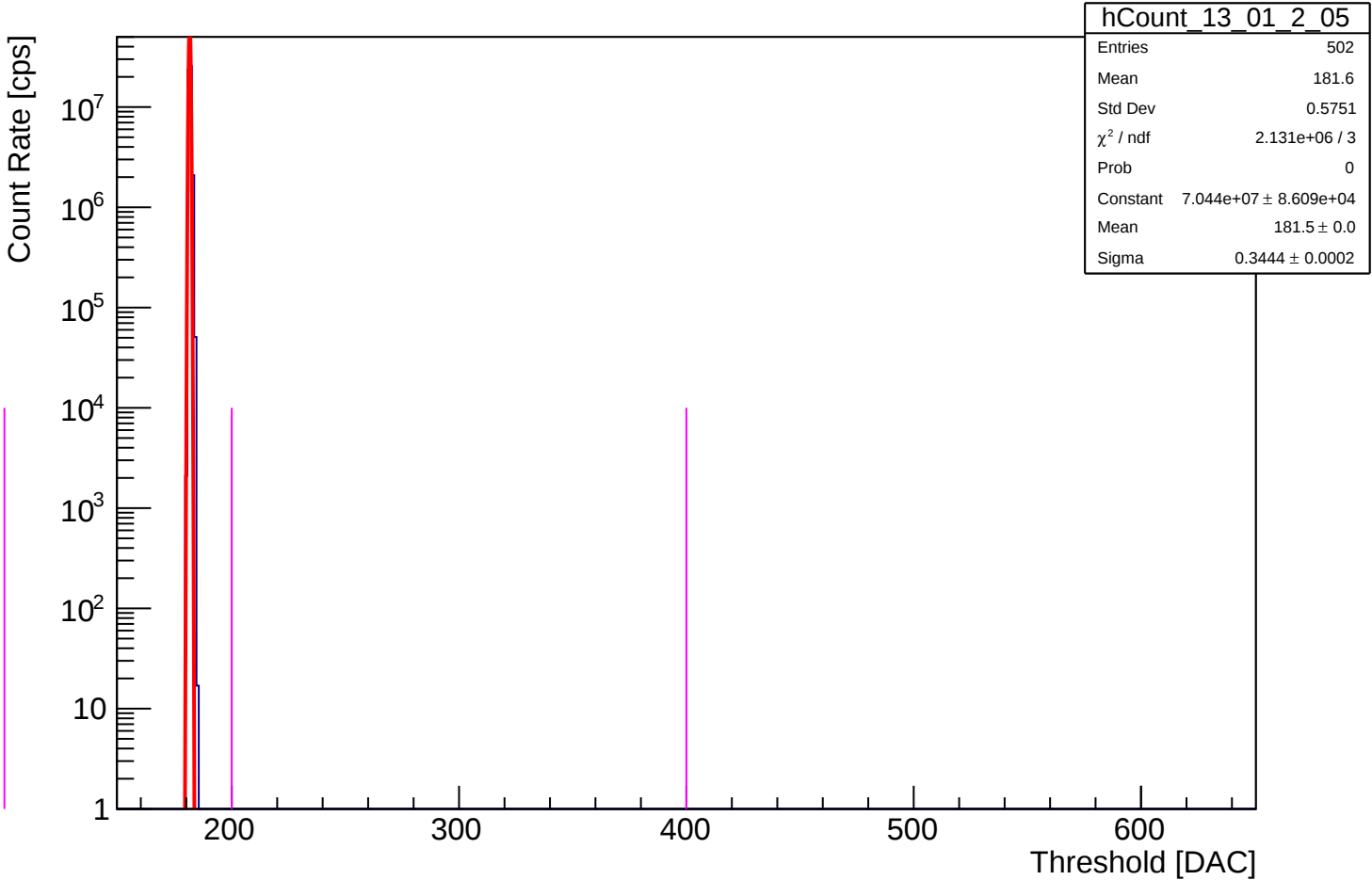
Row 1 Tile 1 Pmt 6 Pixel 47 Slot 13 Fiber 1 Asic 2 Channel 53

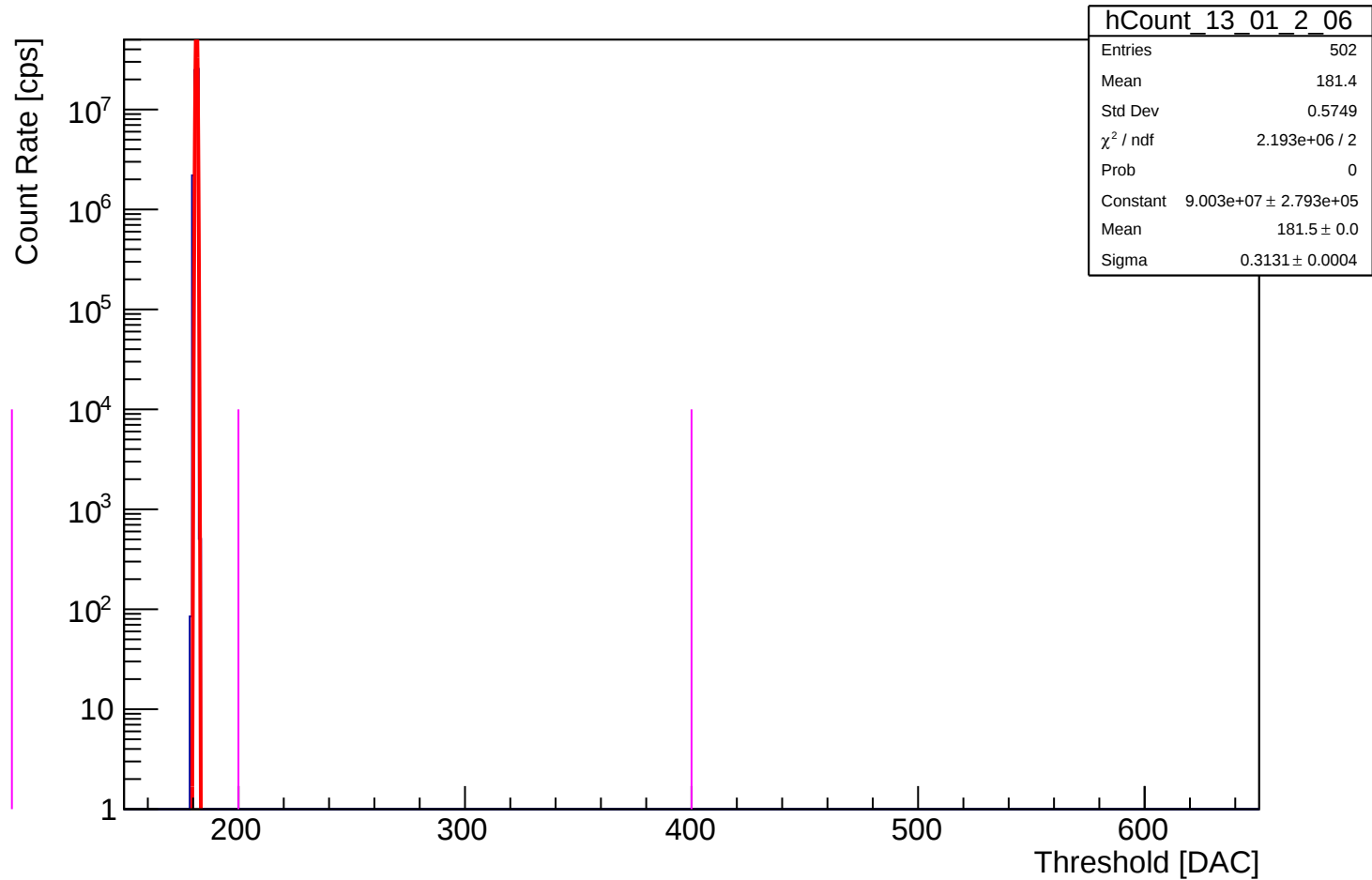


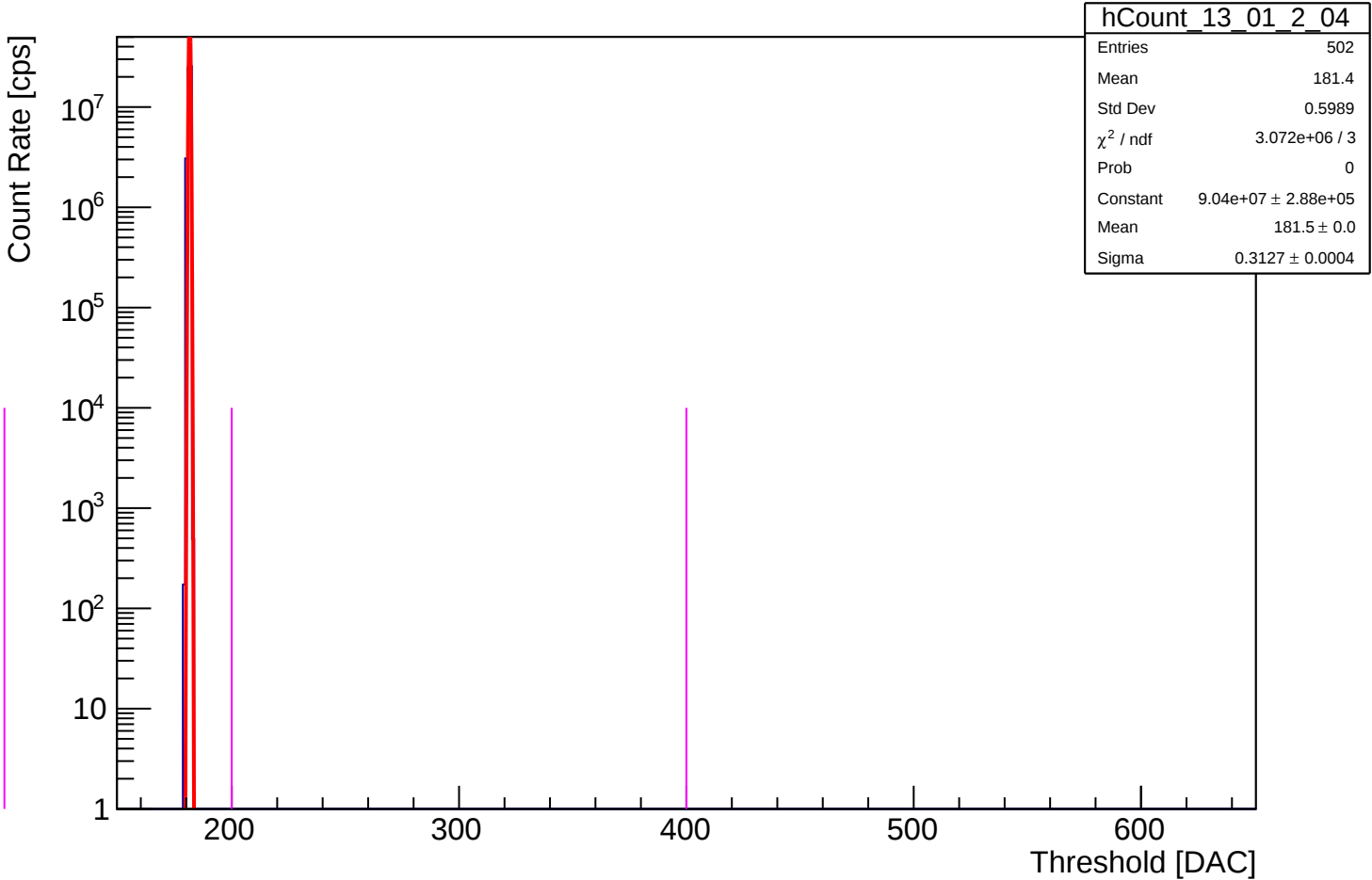
Row 1 Tile 1 Pmt 6 Pixel 48 Slot 13 Fiber 1 Asic 2 Channel 55



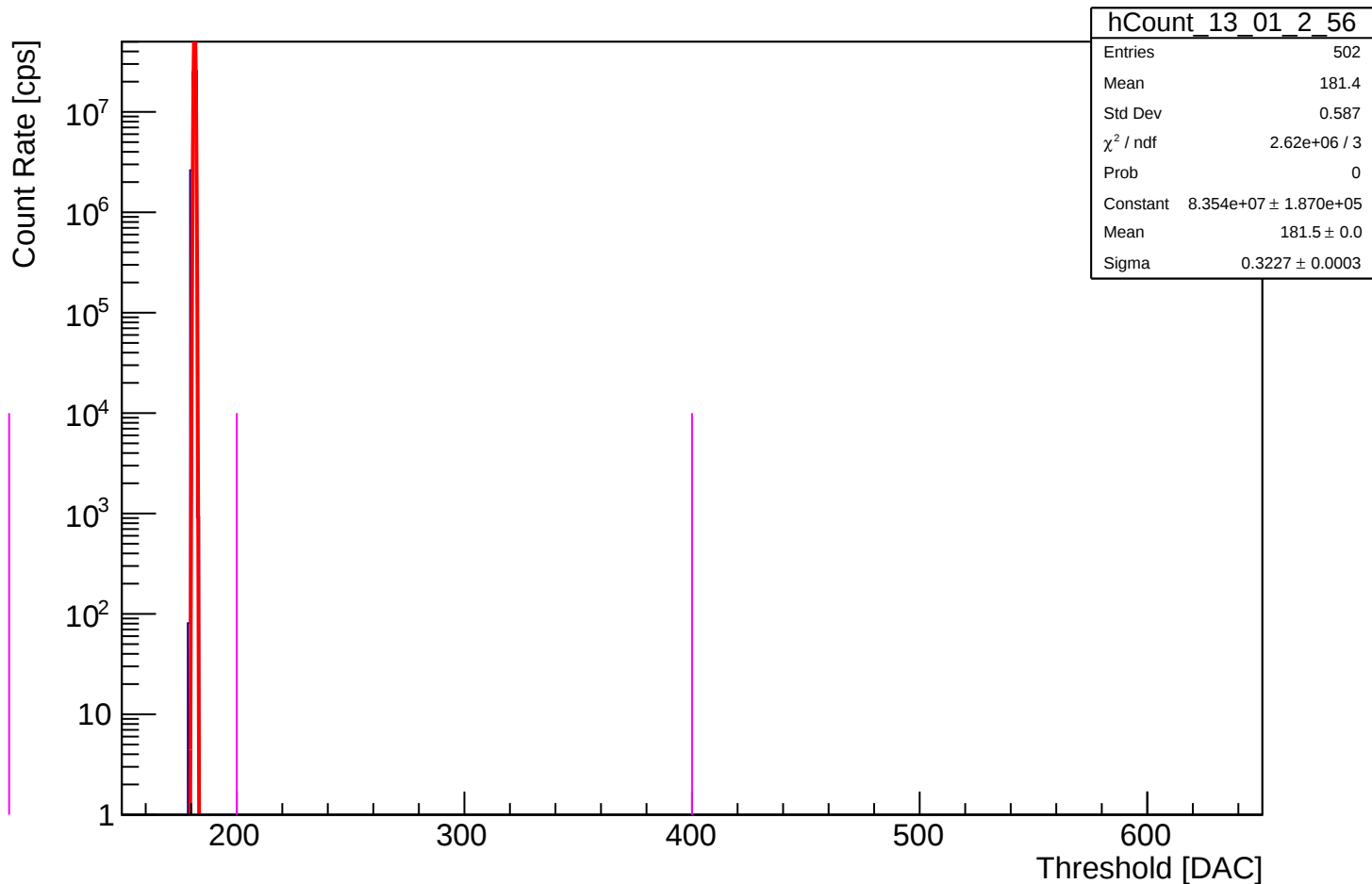




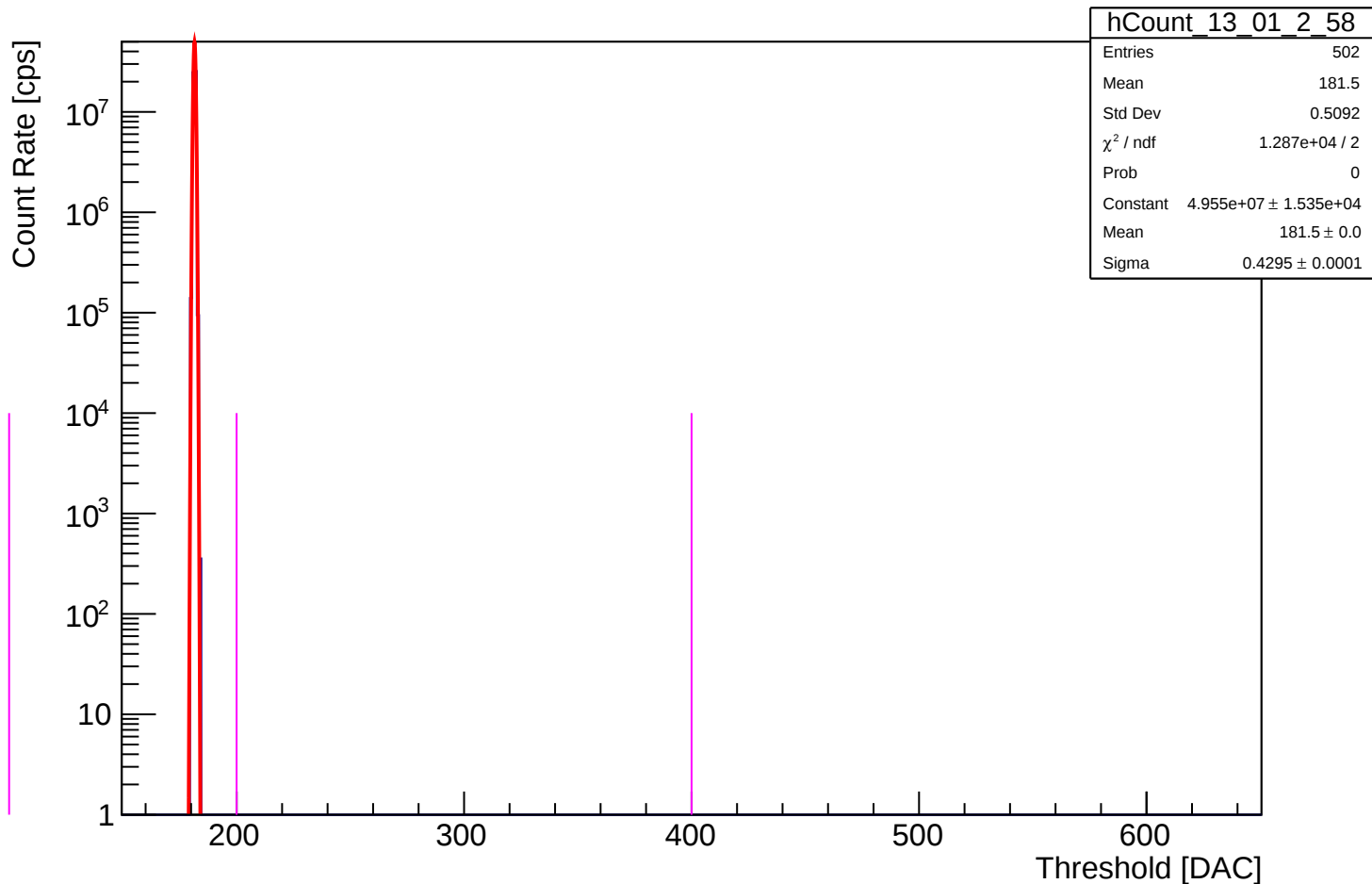




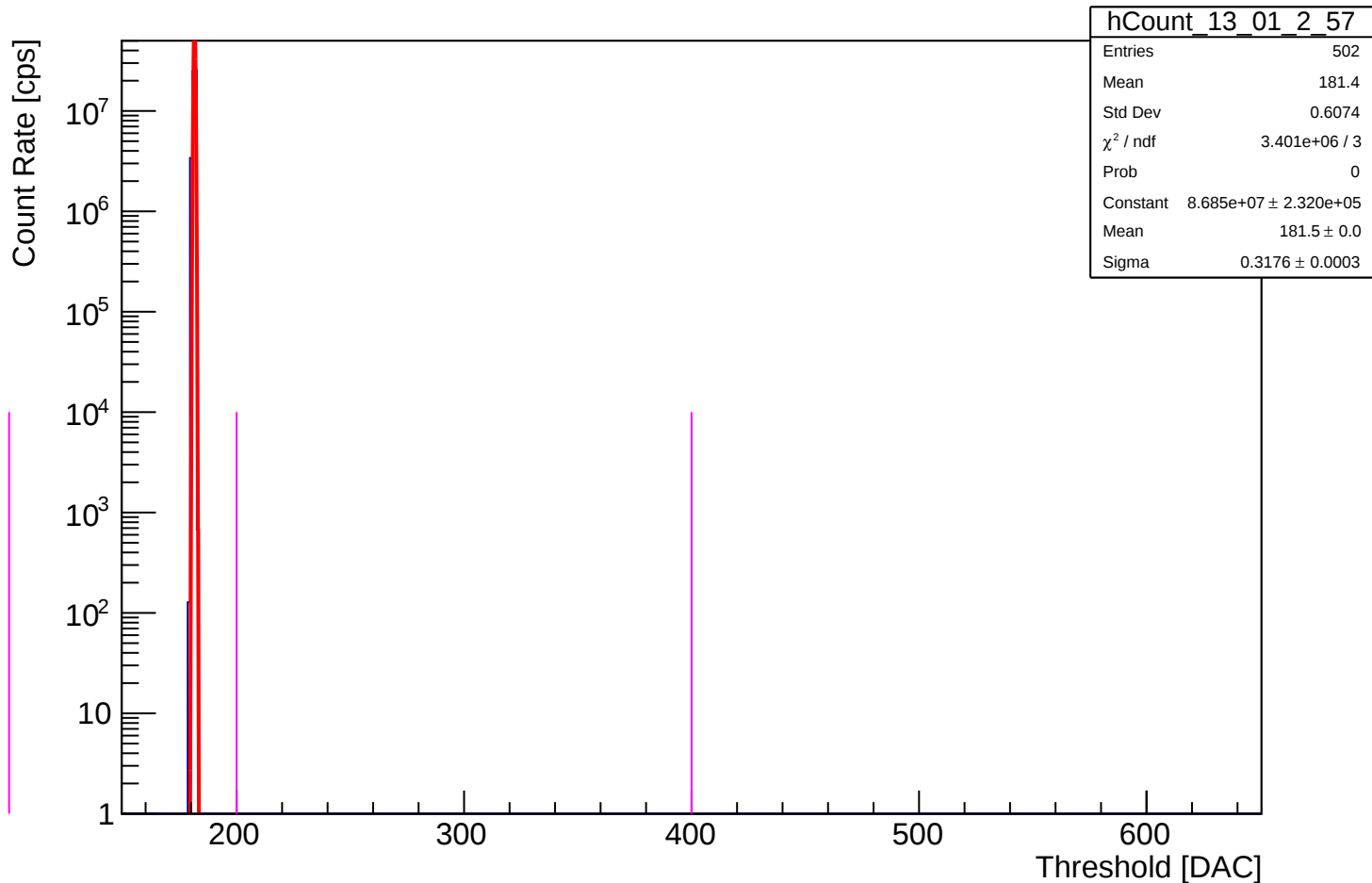
Row 1 Tile 1 Pmt 6 Pixel 53 Slot 13 Fiber 1 Asic 2 Channel 56



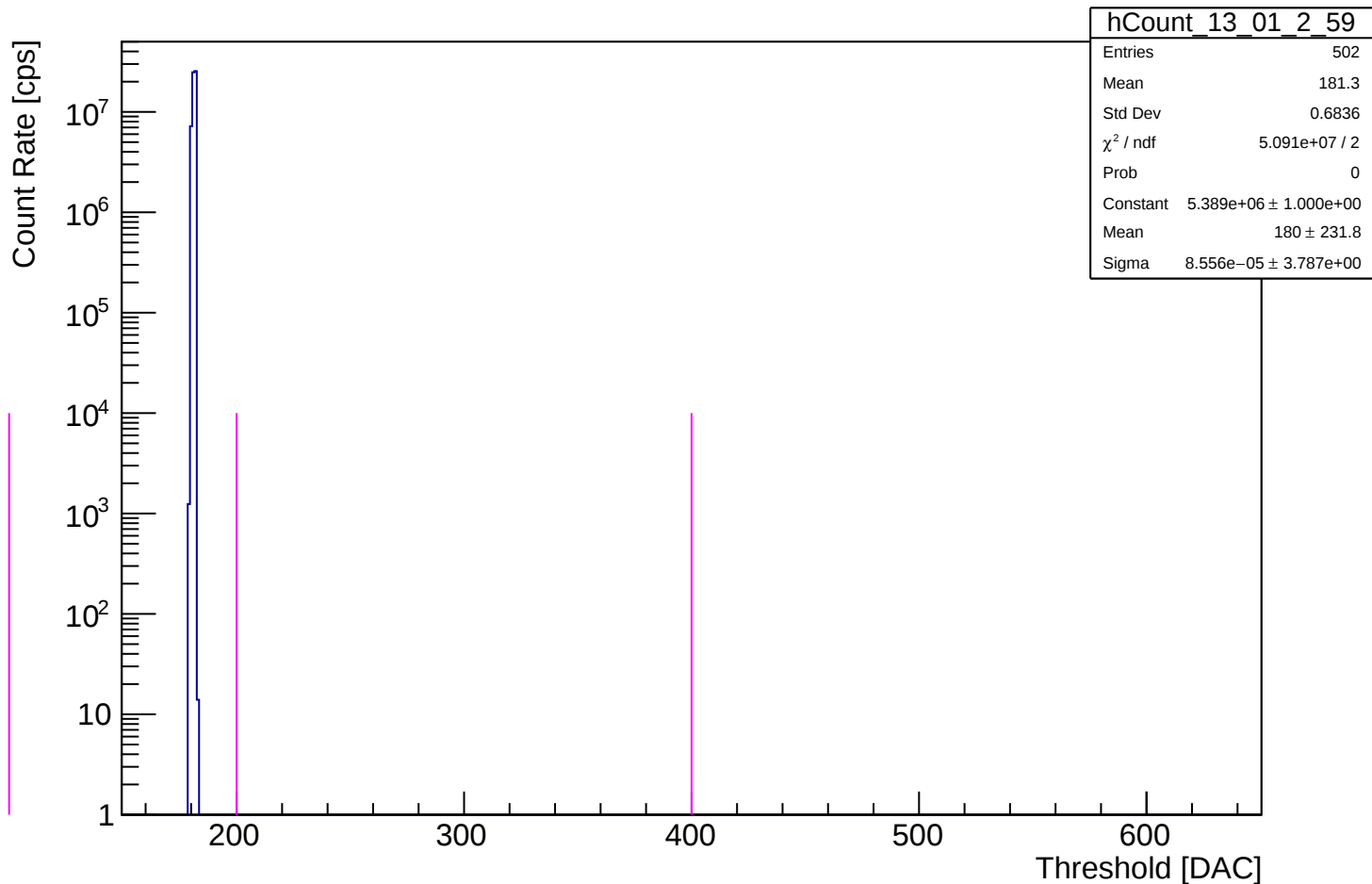
Row 1 Tile 1 Pmt 6 Pixel 54 Slot 13 Fiber 1 Asic 2 Channel 58

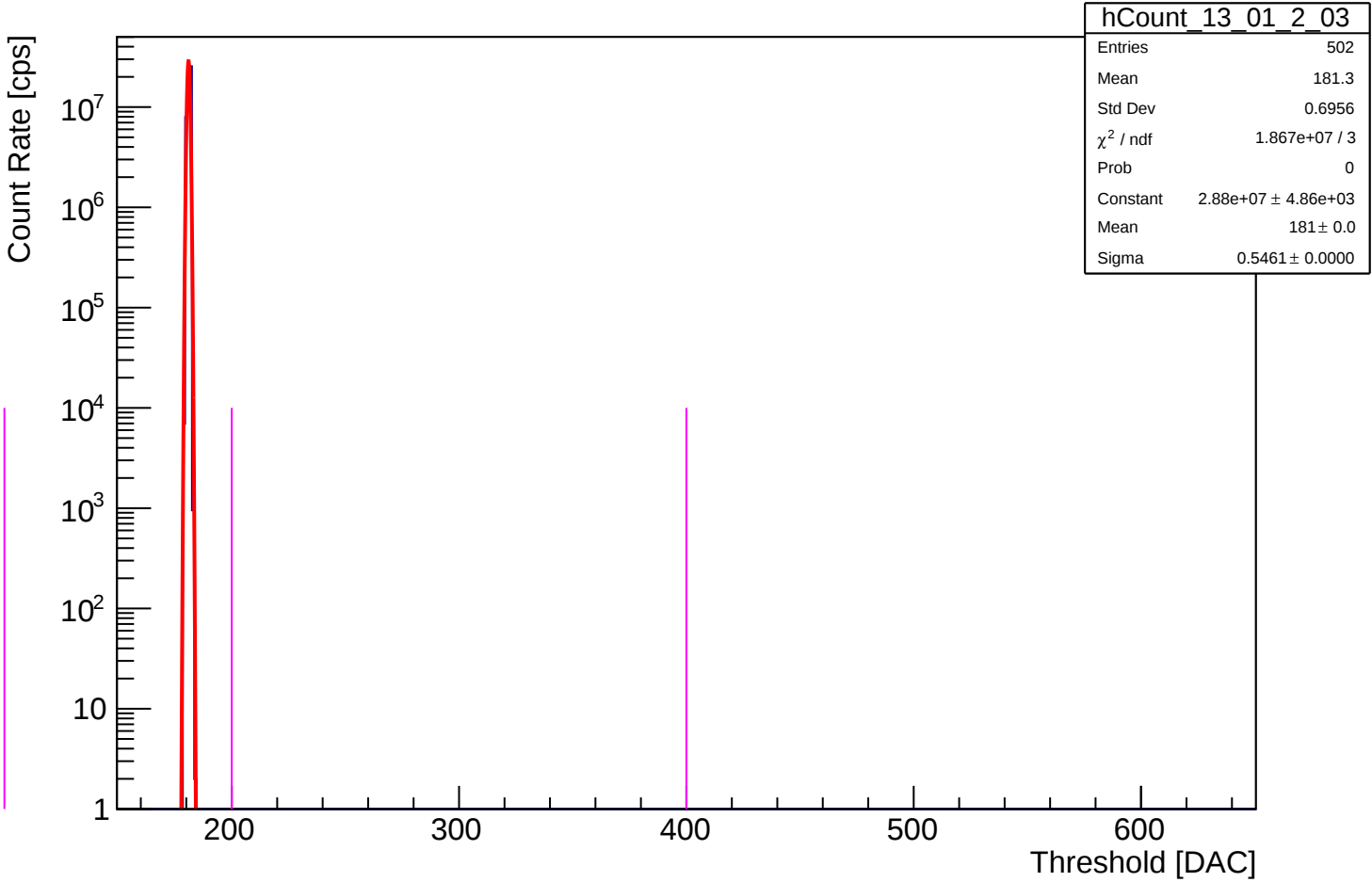


Row 1 Tile 1 Pmt 6 Pixel 55 Slot 13 Fiber 1 Asic 2 Channel 57

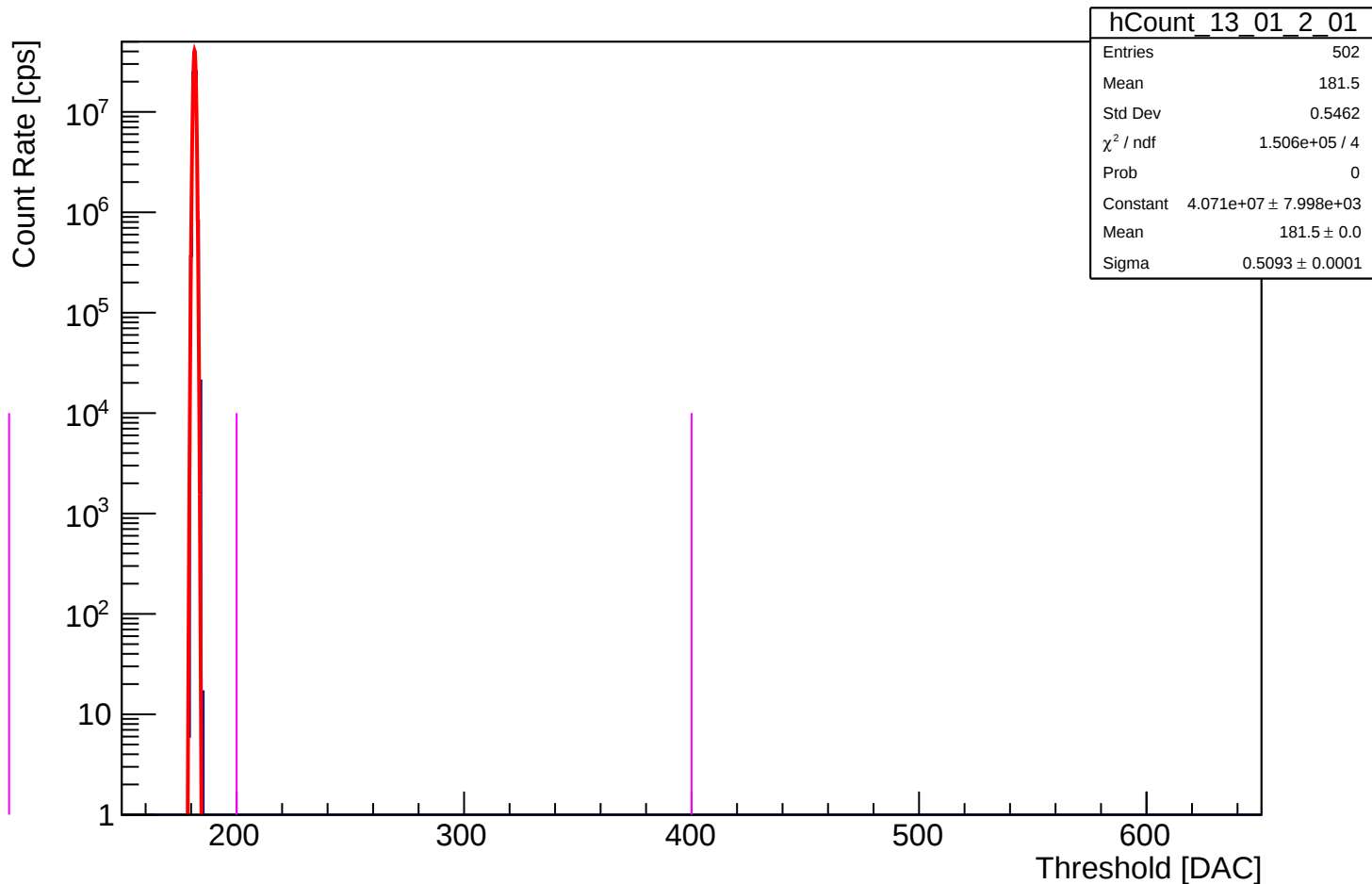


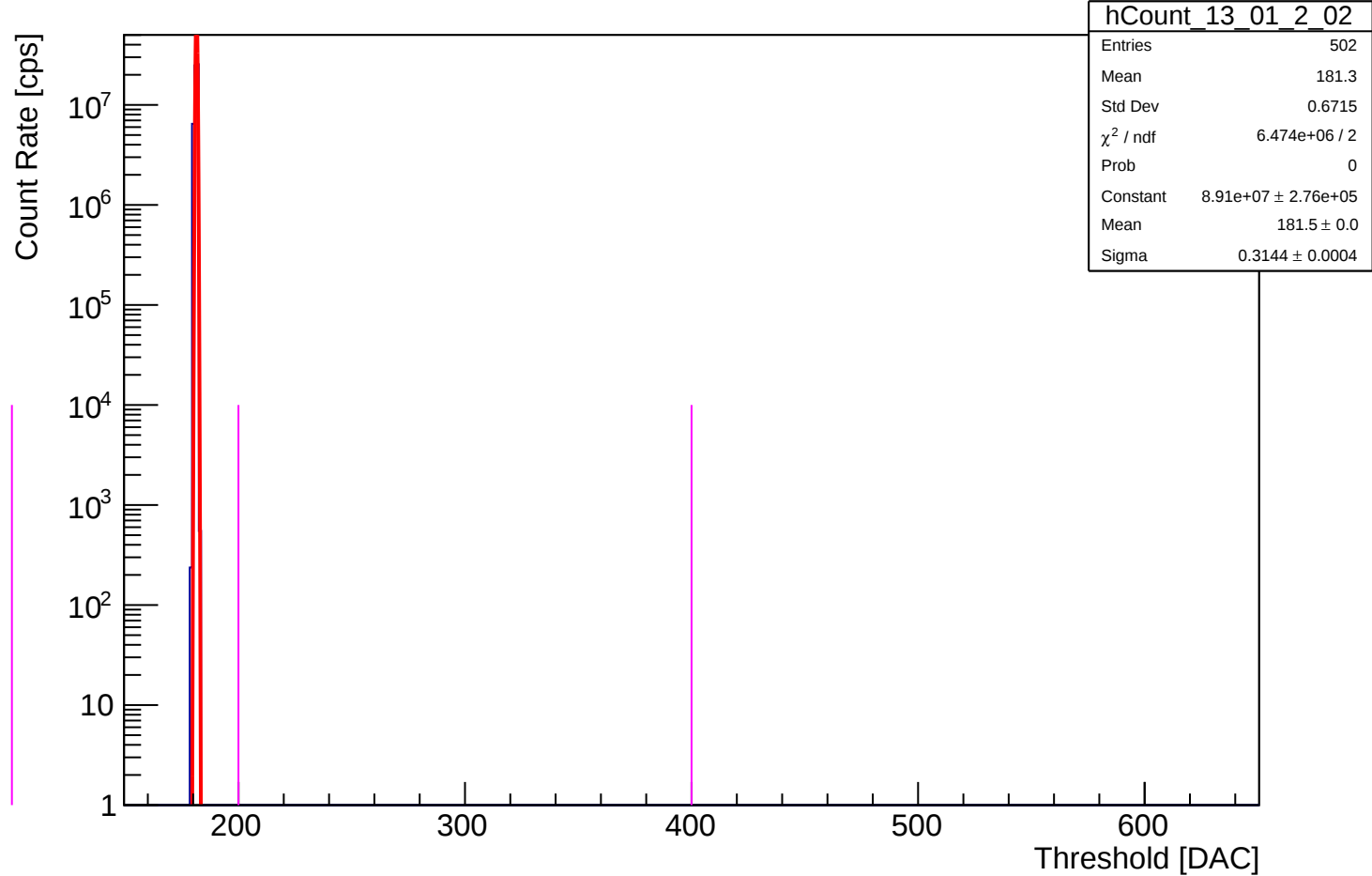
Row 1 Tile 1 Pmt 6 Pixel 56 Slot 13 Fiber 1 Asic 2 Channel 59

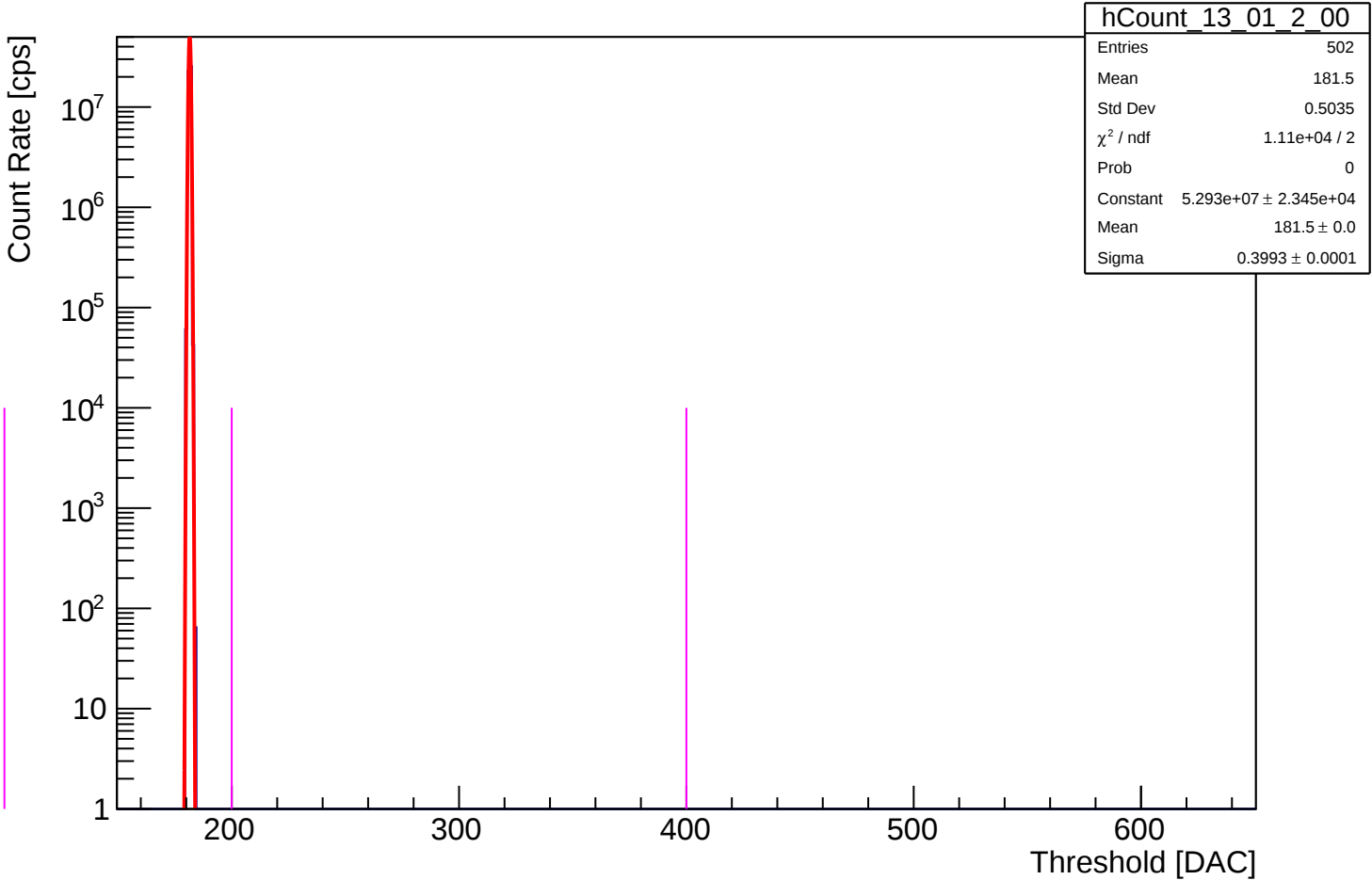




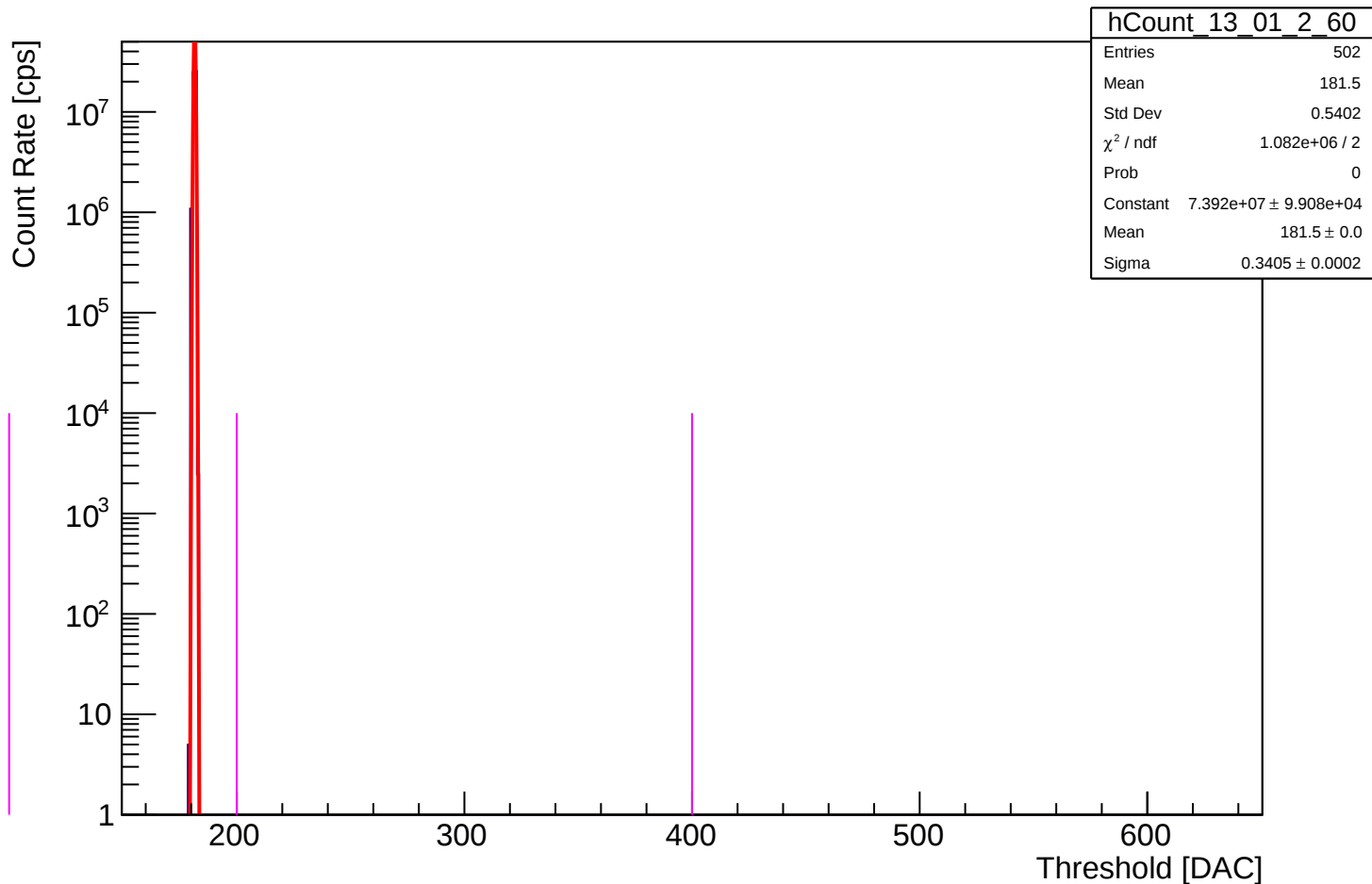
Row 1 Tile 1 Pmt 6 Pixel 58 Slot 13 Fiber 1 Asic 2 Channel 1



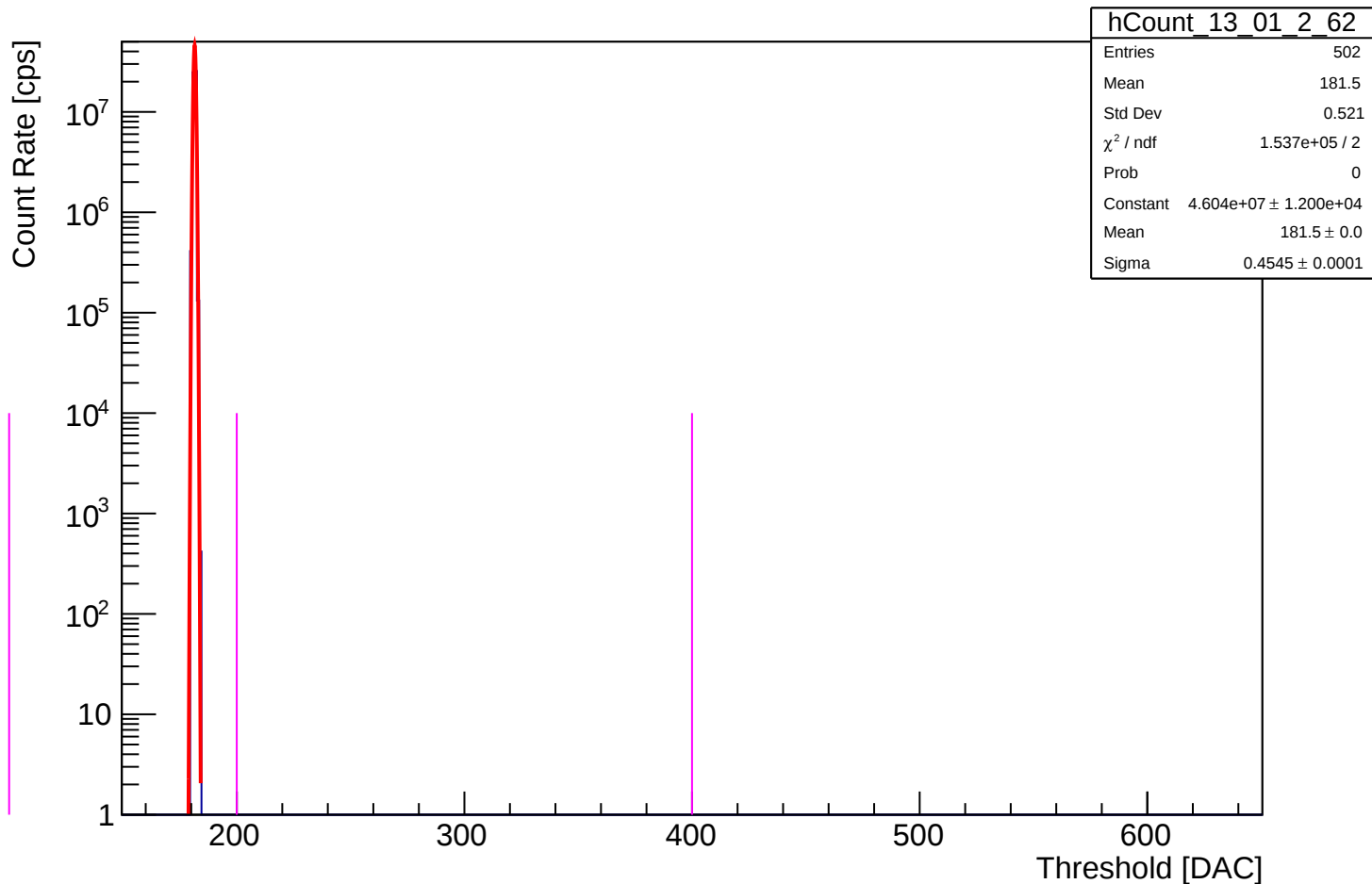


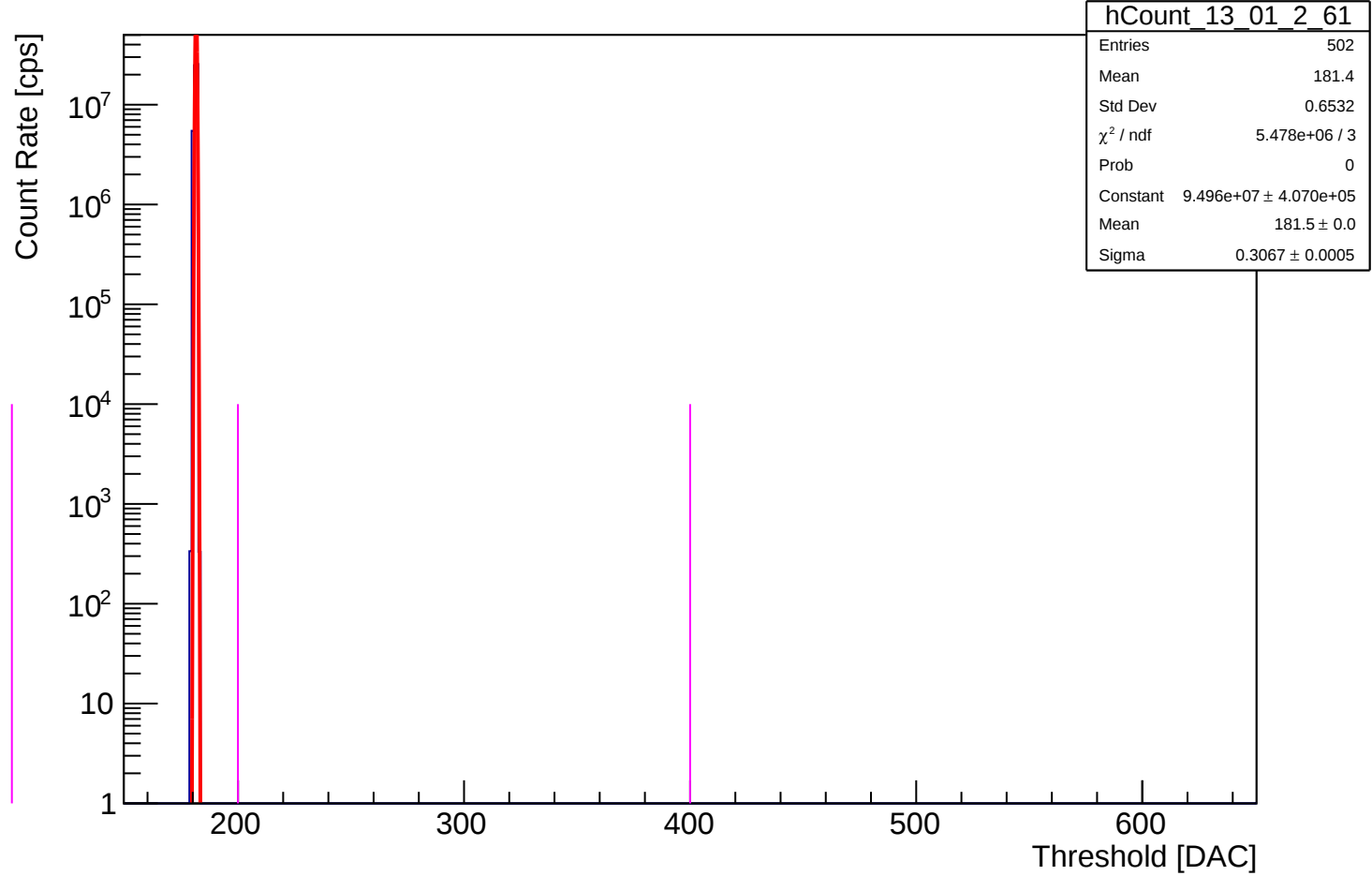


Row 1 Tile 1 Pmt 6 Pixel 61 Slot 13 Fiber 1 Asic 2 Channel 60



Row 1 Tile 1 Pmt 6 Pixel 62 Slot 13 Fiber 1 Asic 2 Channel 62





Row 1 Tile 1 Pmt 6 Pixel 64 Slot 13 Fiber 1 Asic 2 Channel 63

