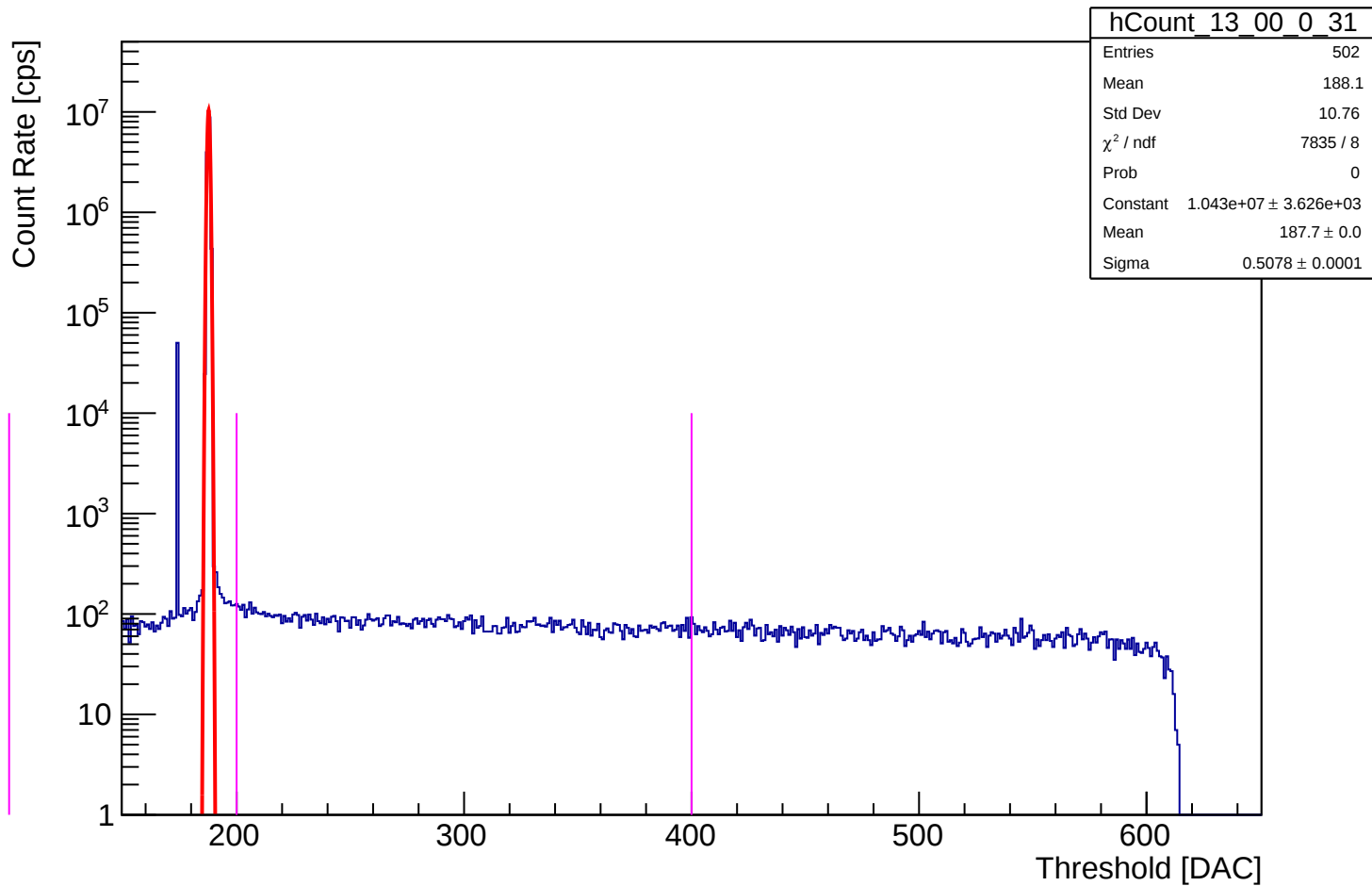
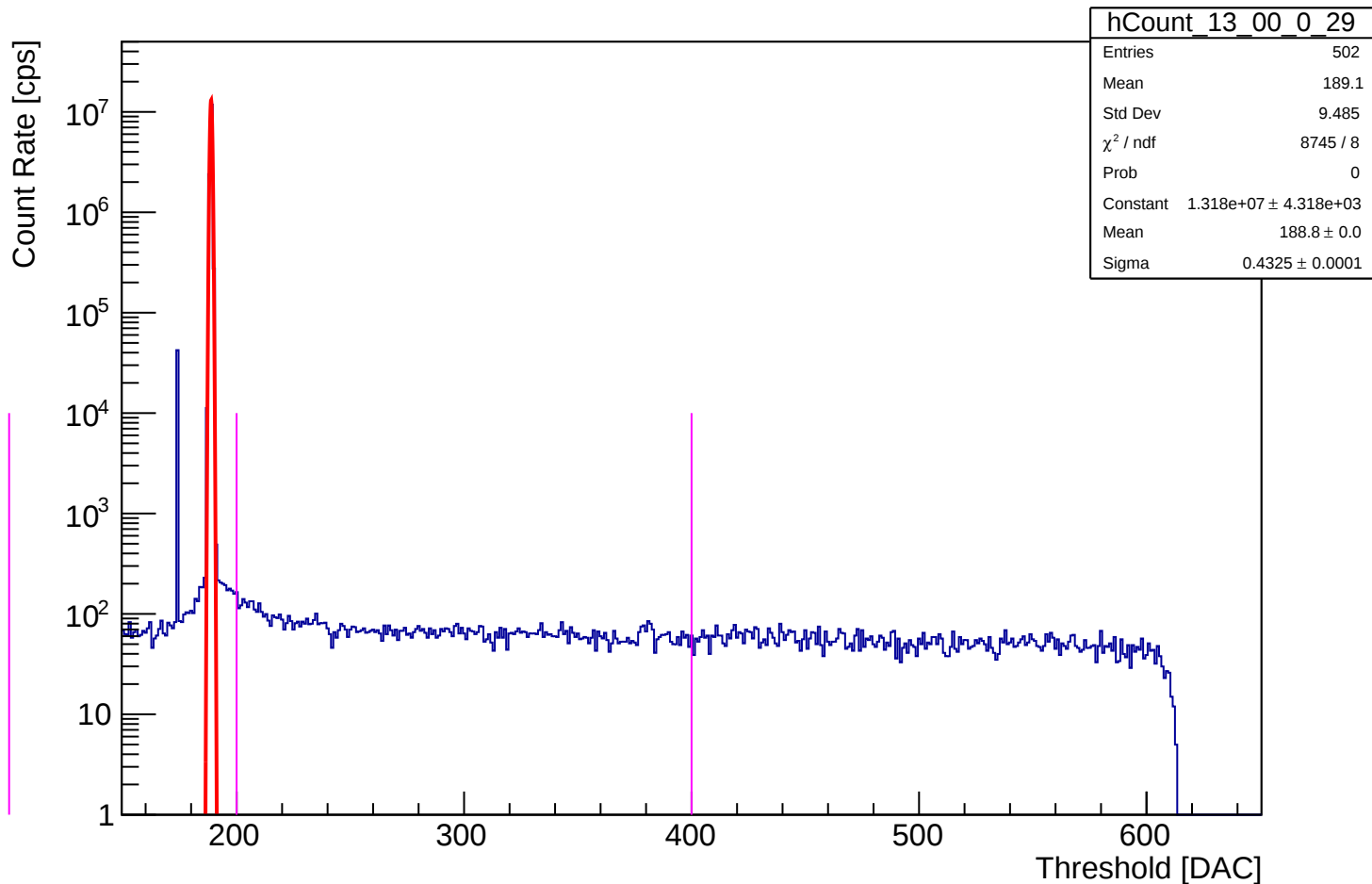


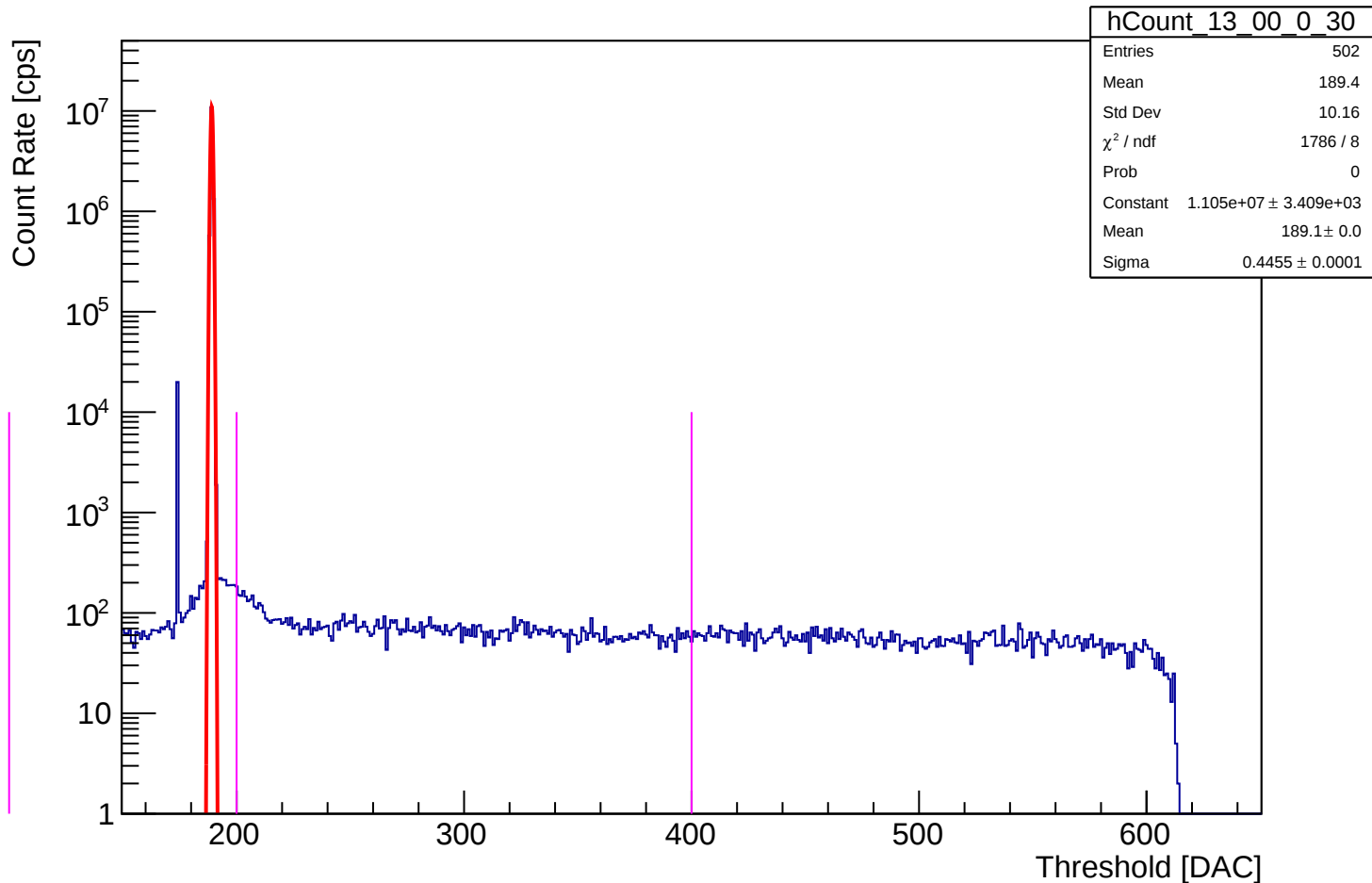
Row 1 Tile 1 Pmt 1 Pixel 1 Slot 13 Fiber 0 Asic 0 Channel 31



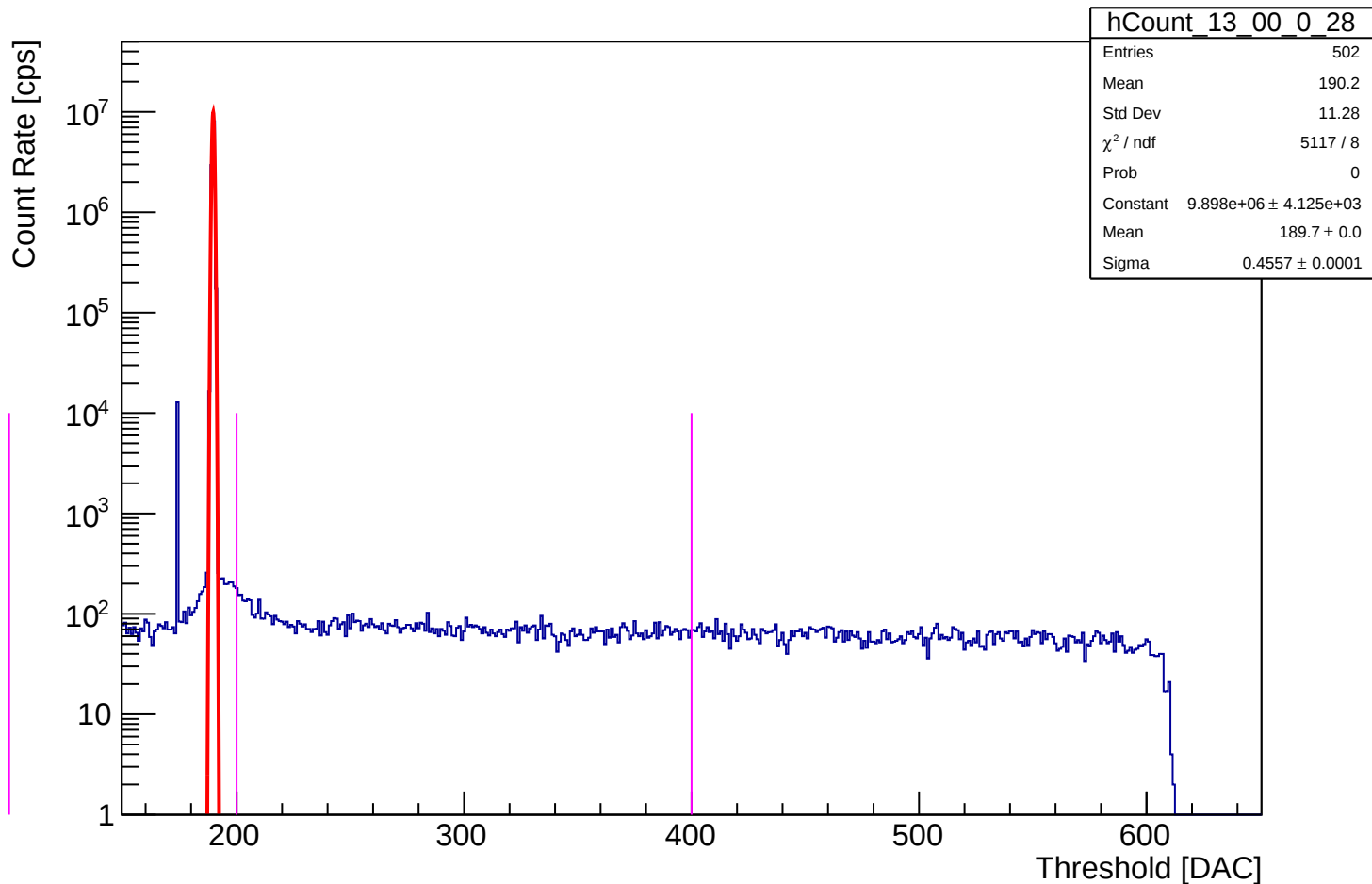
Row 1 Tile 1 Pmt 1 Pixel 2 Slot 13 Fiber 0 Asic 0 Channel 29



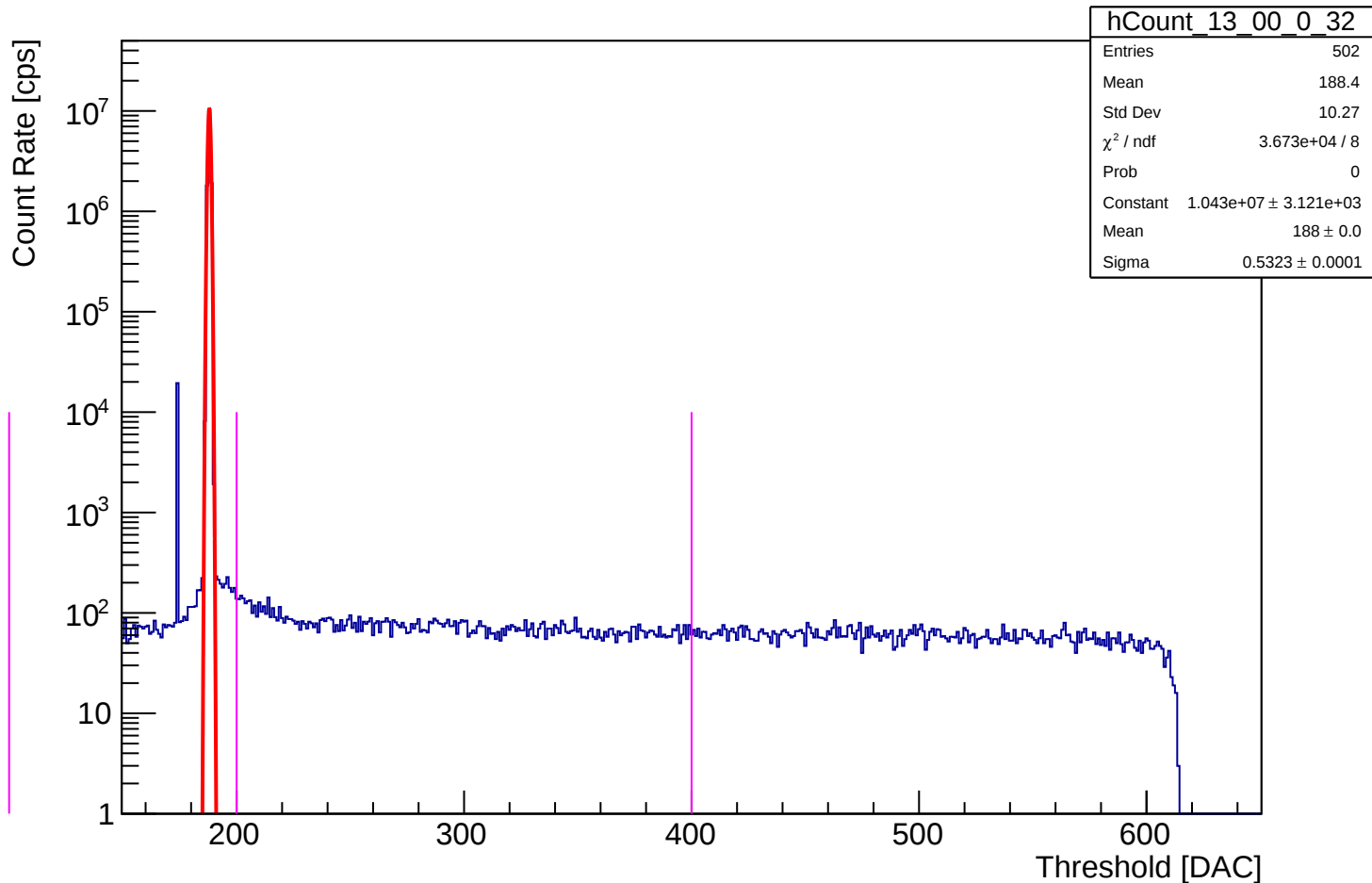
Row 1 Tile 1 Pmt 1 Pixel 3 Slot 13 Fiber 0 Asic 0 Channel 30



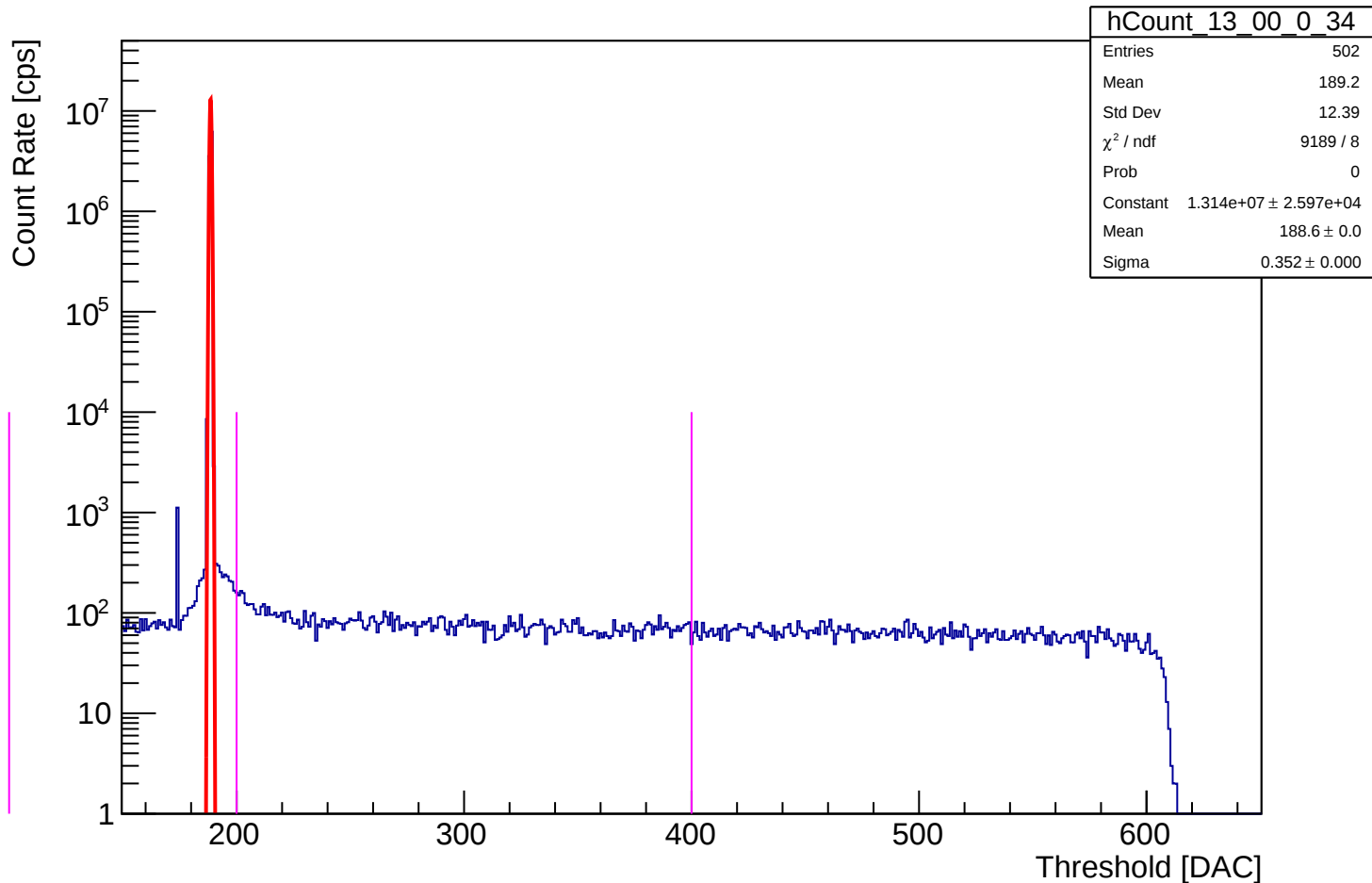
Row 1 Tile 1 Pmt 1 Pixel 4 Slot 13 Fiber 0 Asic 0 Channel 28



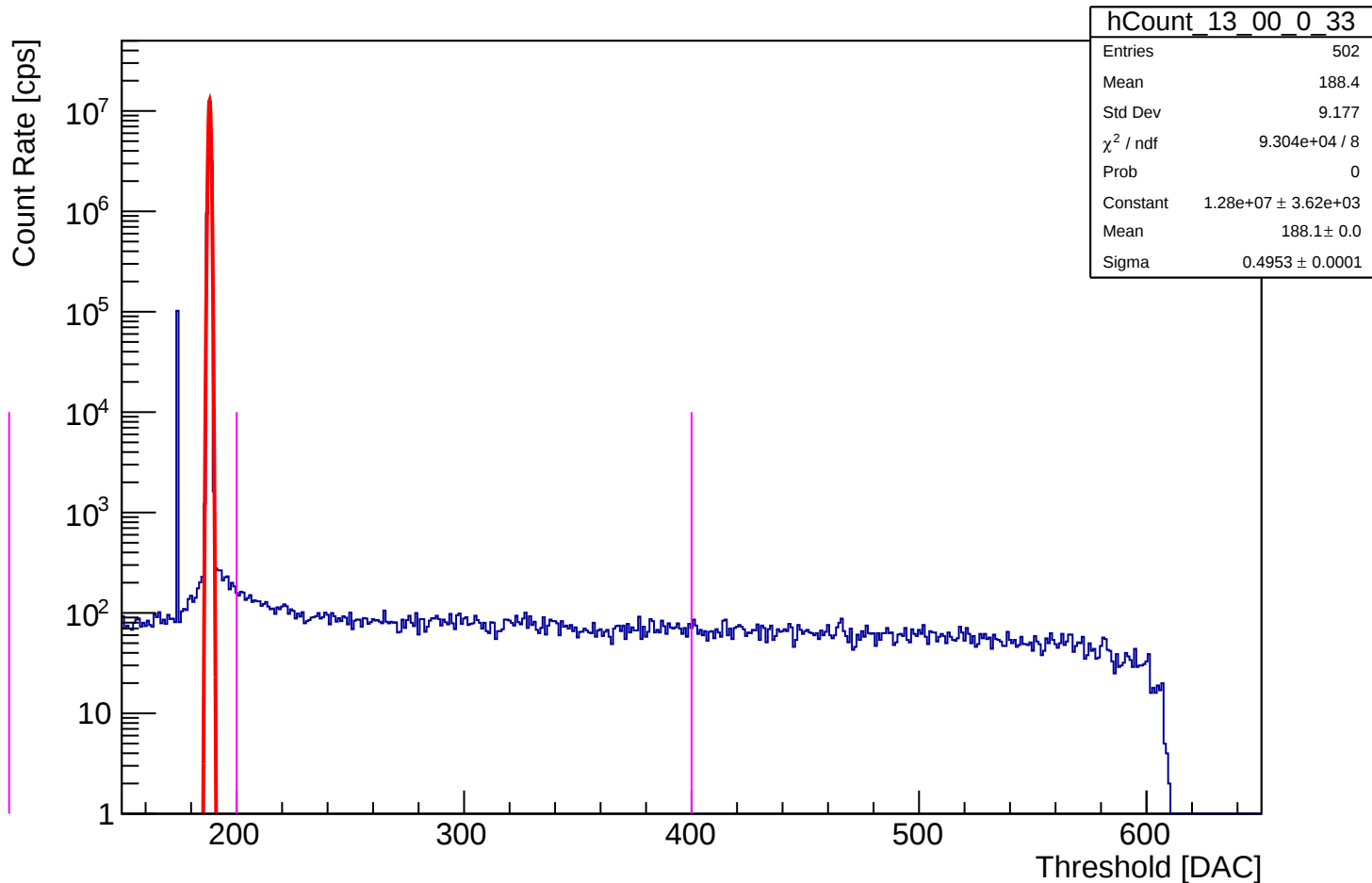
Row 1 Tile 1 Pmt 1 Pixel 5 Slot 13 Fiber 0 Asic 0 Channel 32



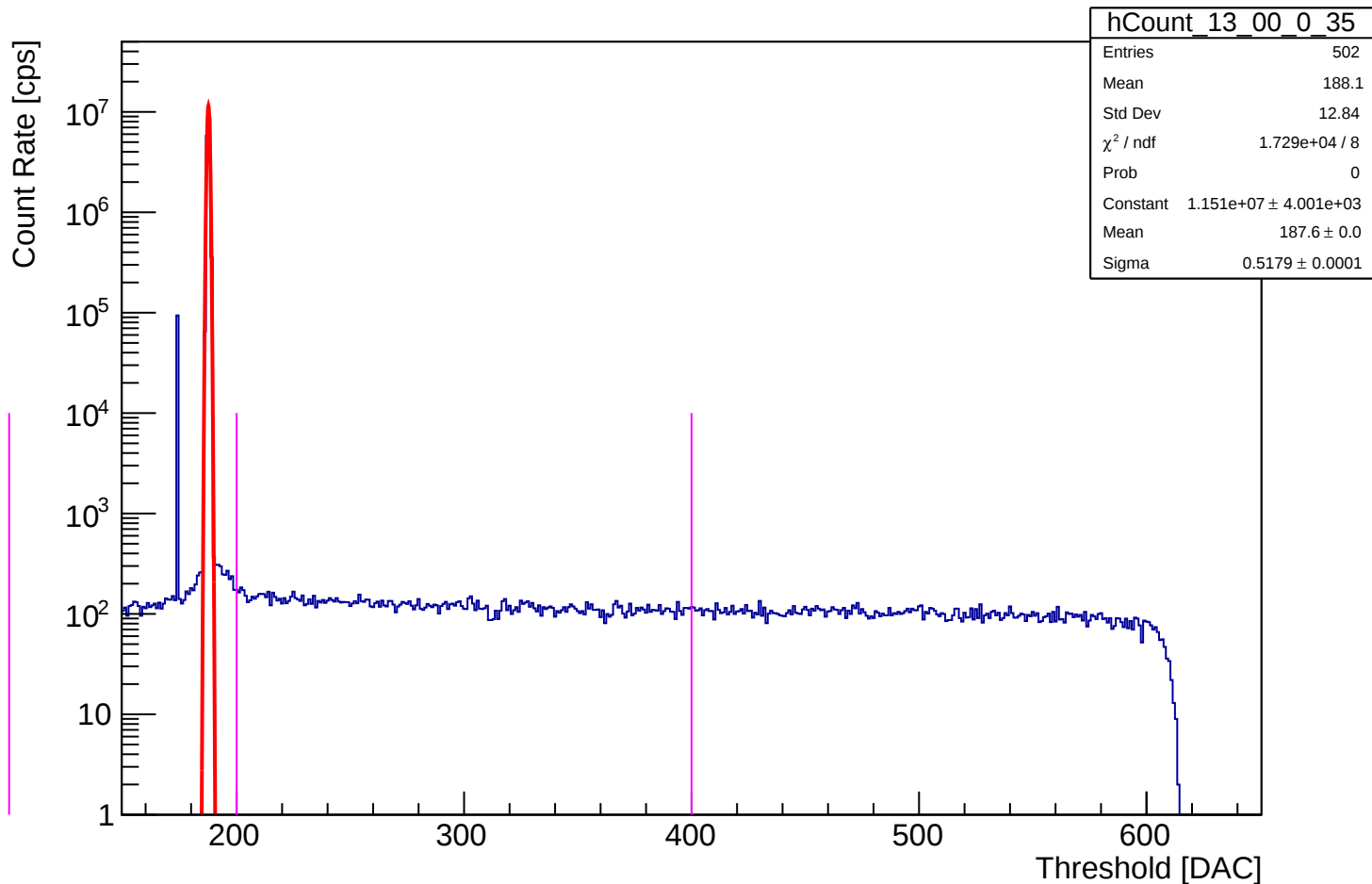
Row 1 Tile 1 Pmt 1 Pixel 6 Slot 13 Fiber 0 Asic 0 Channel 34



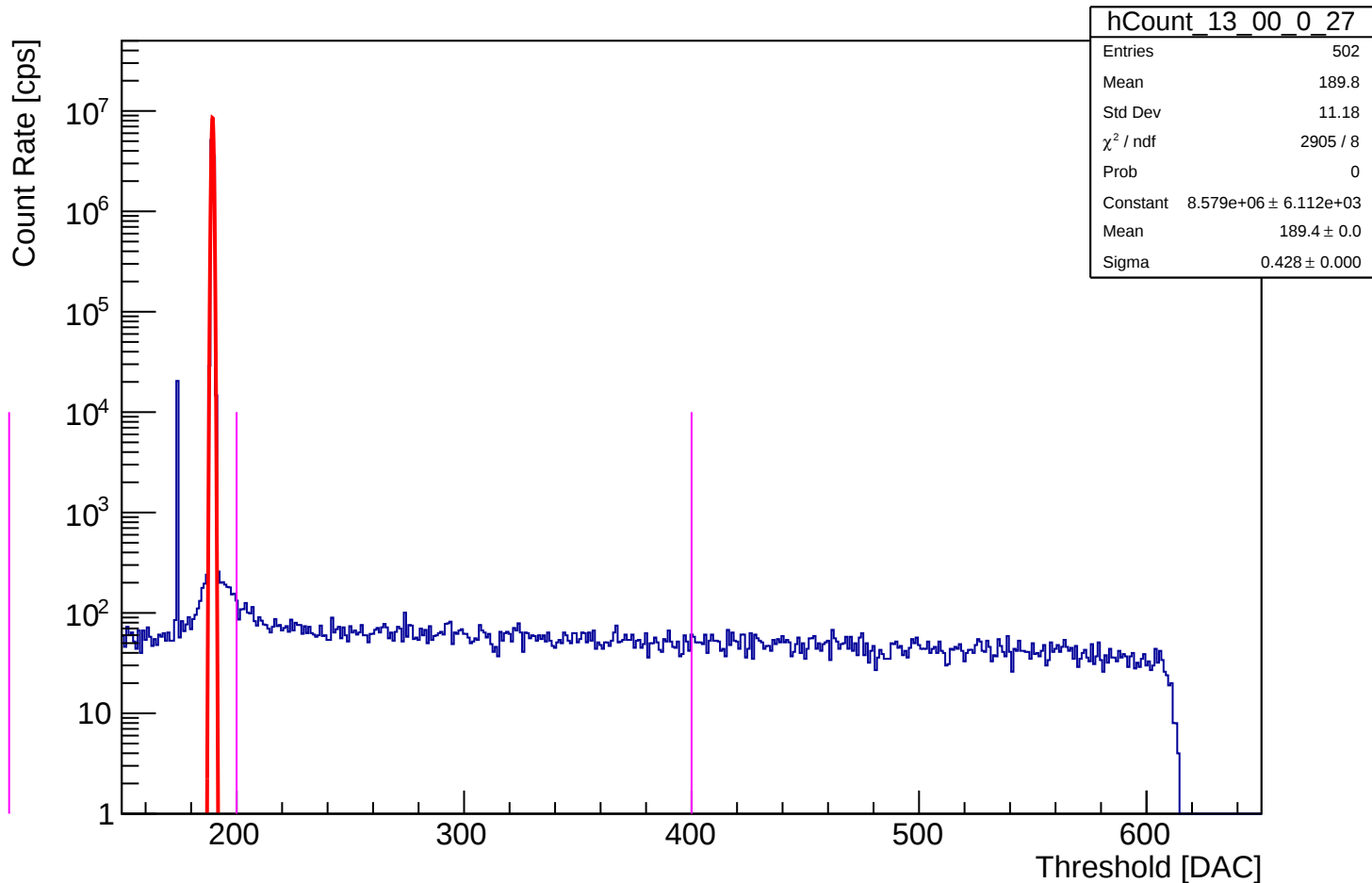
Row 1 Tile 1 Pmt 1 Pixel 7 Slot 13 Fiber 0 Asic 0 Channel 33



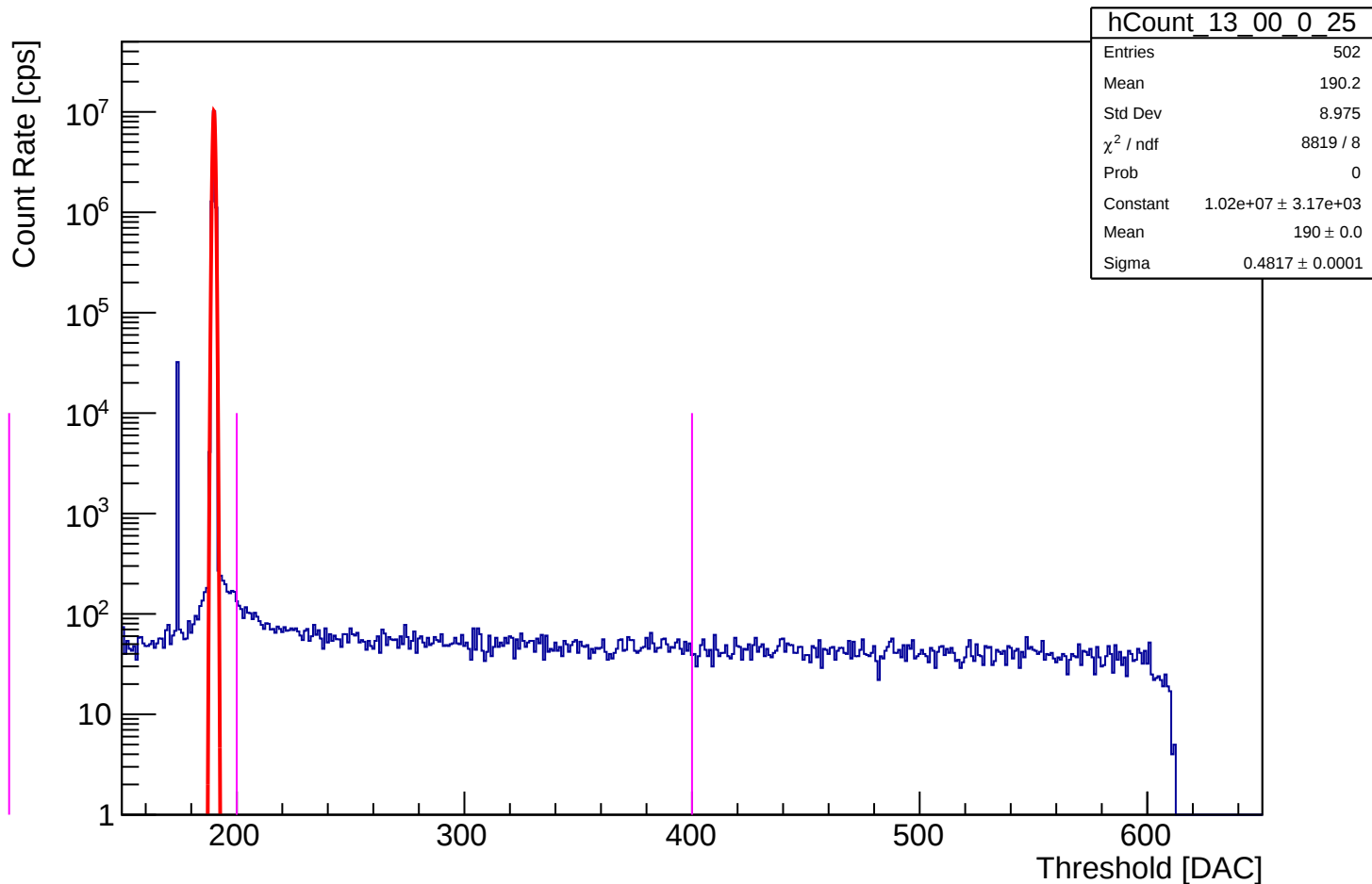
Row 1 Tile 1 Pmt 1 Pixel 8 Slot 13 Fiber 0 Asic 0 Channel 35



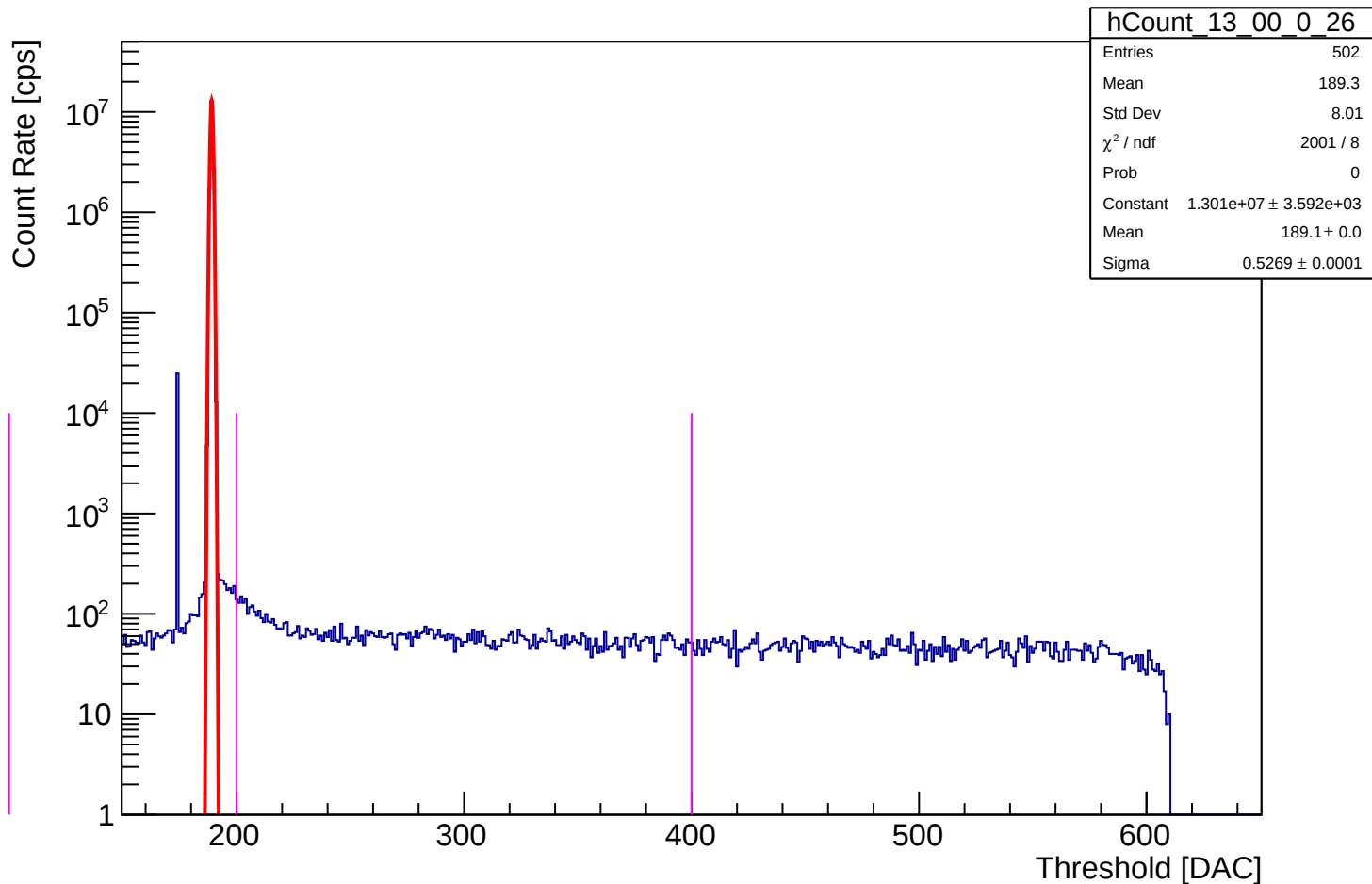
Row 1 Tile 1 Pmt 1 Pixel 9 Slot 13 Fiber 0 Asic 0 Channel 27



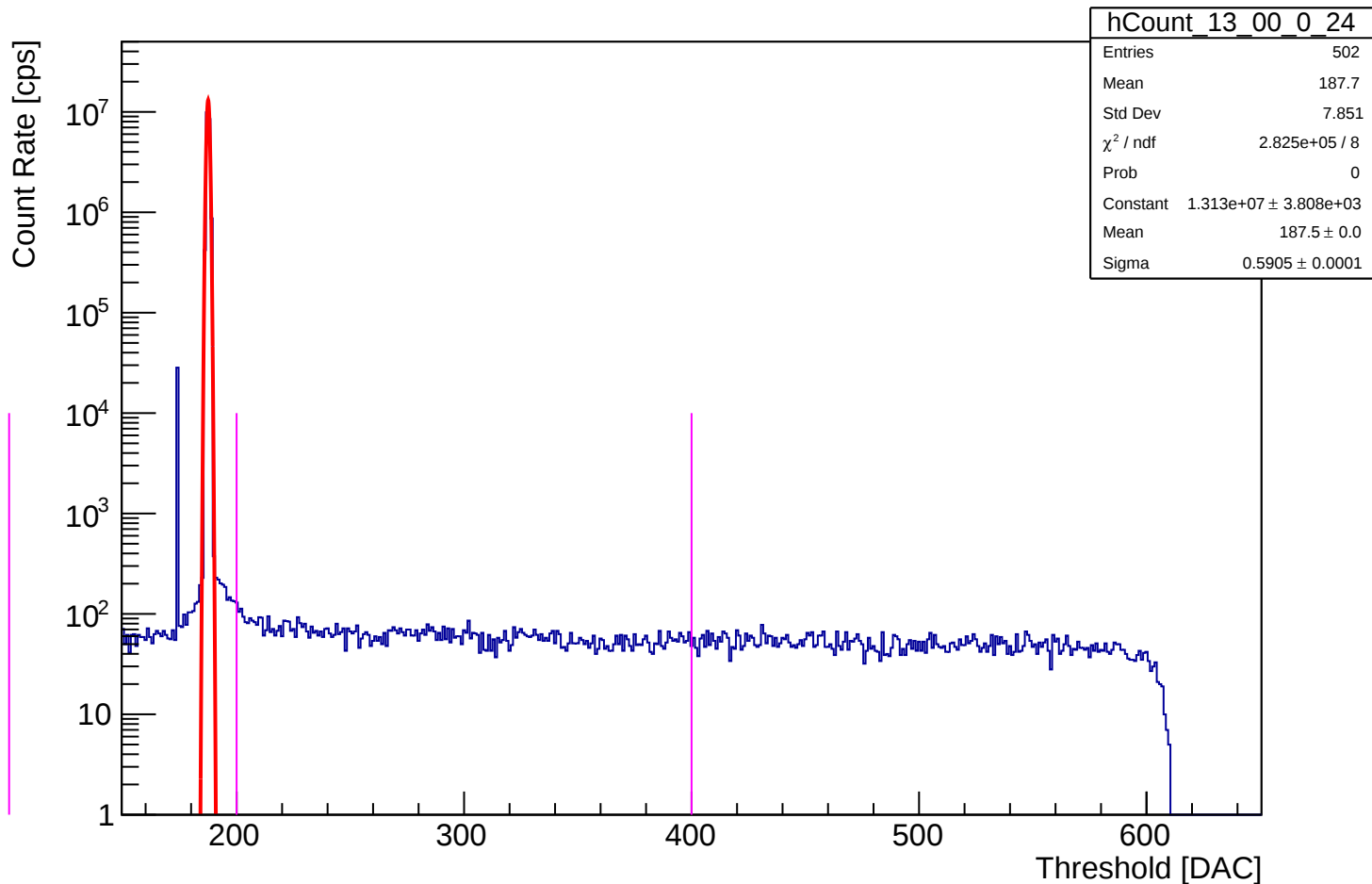
Row 1 Tile 1 Pmt 1 Pixel 10 Slot 13 Fiber 0 Asic 0 Channel 25



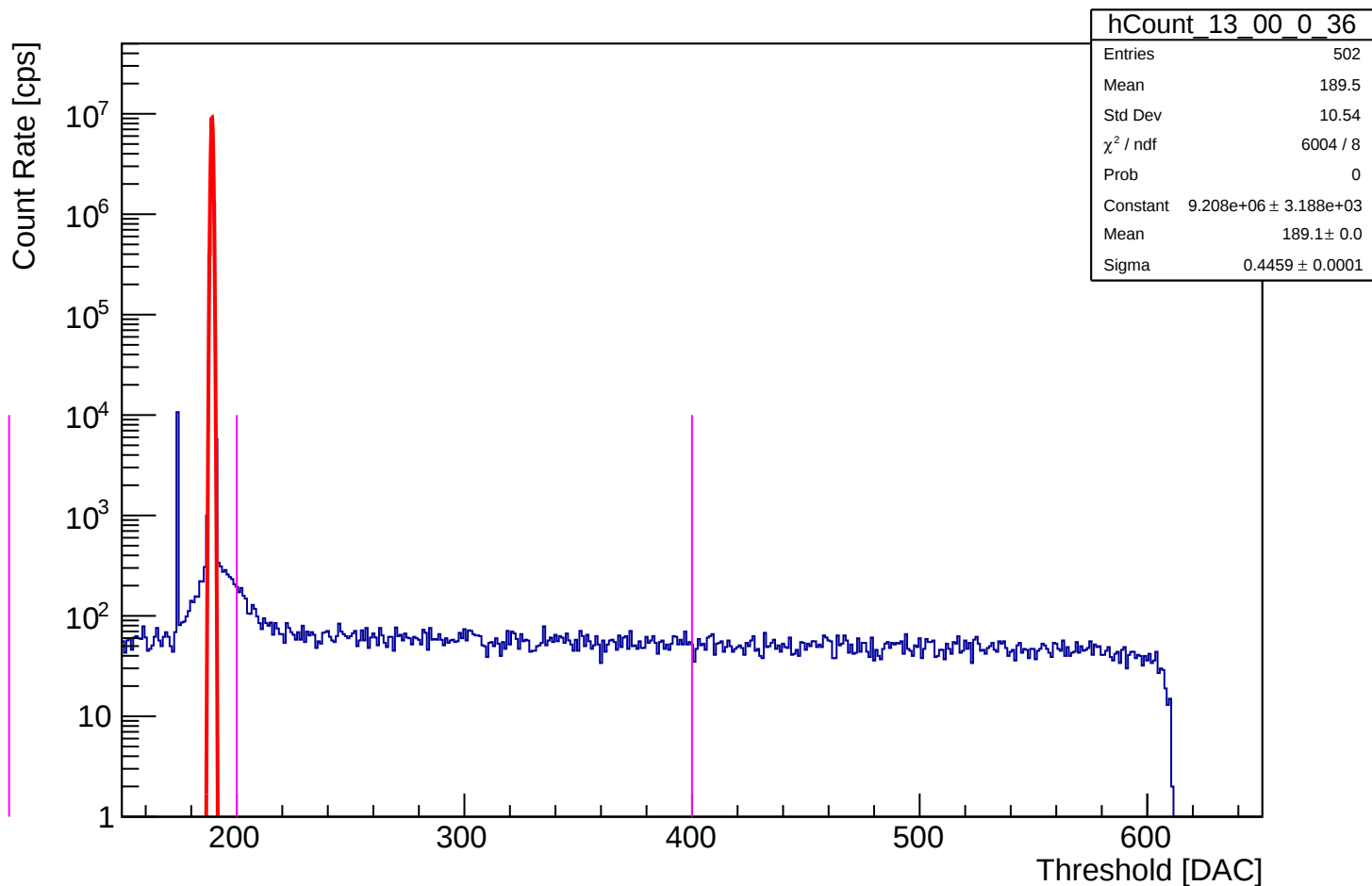
Row 1 Tile 1 Pmt 1 Pixel 11 Slot 13 Fiber 0 Asic 0 Channel 26



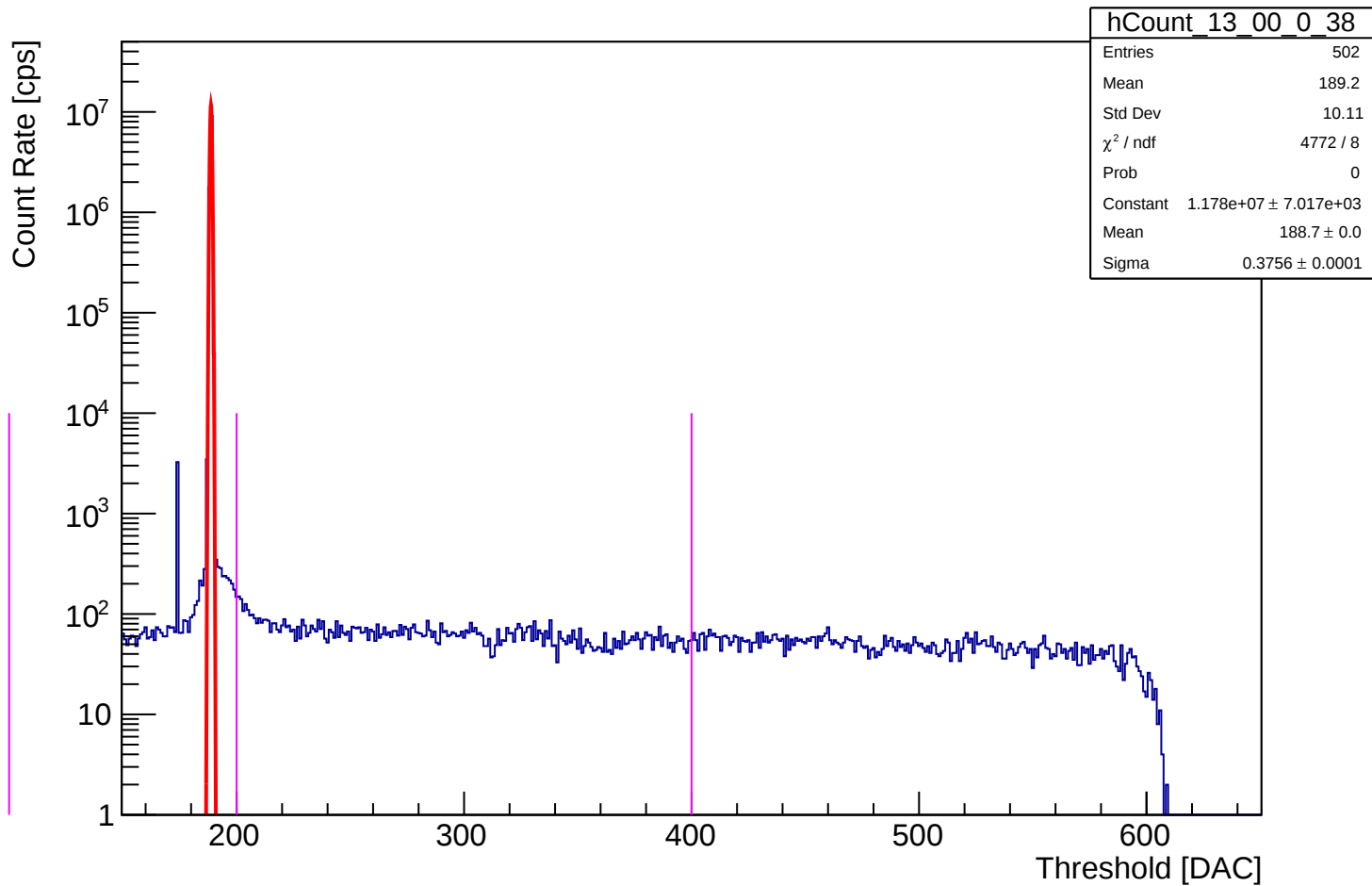
Row 1 Tile 1 Pmt 1 Pixel 12 Slot 13 Fiber 0 Asic 0 Channel 24



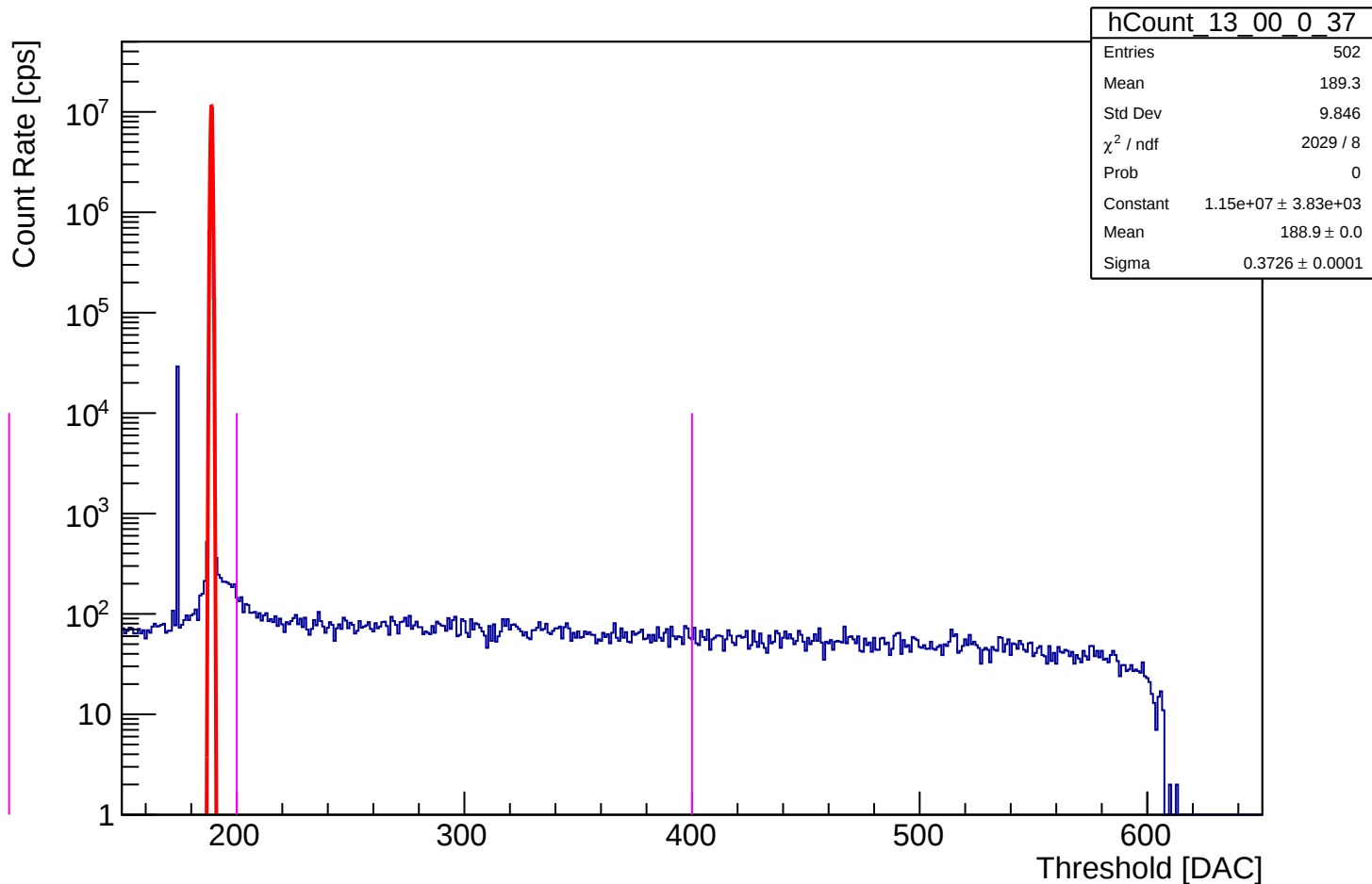
Row 1 Tile 1 Pmt 1 Pixel 13 Slot 13 Fiber 0 Asic 0 Channel 36



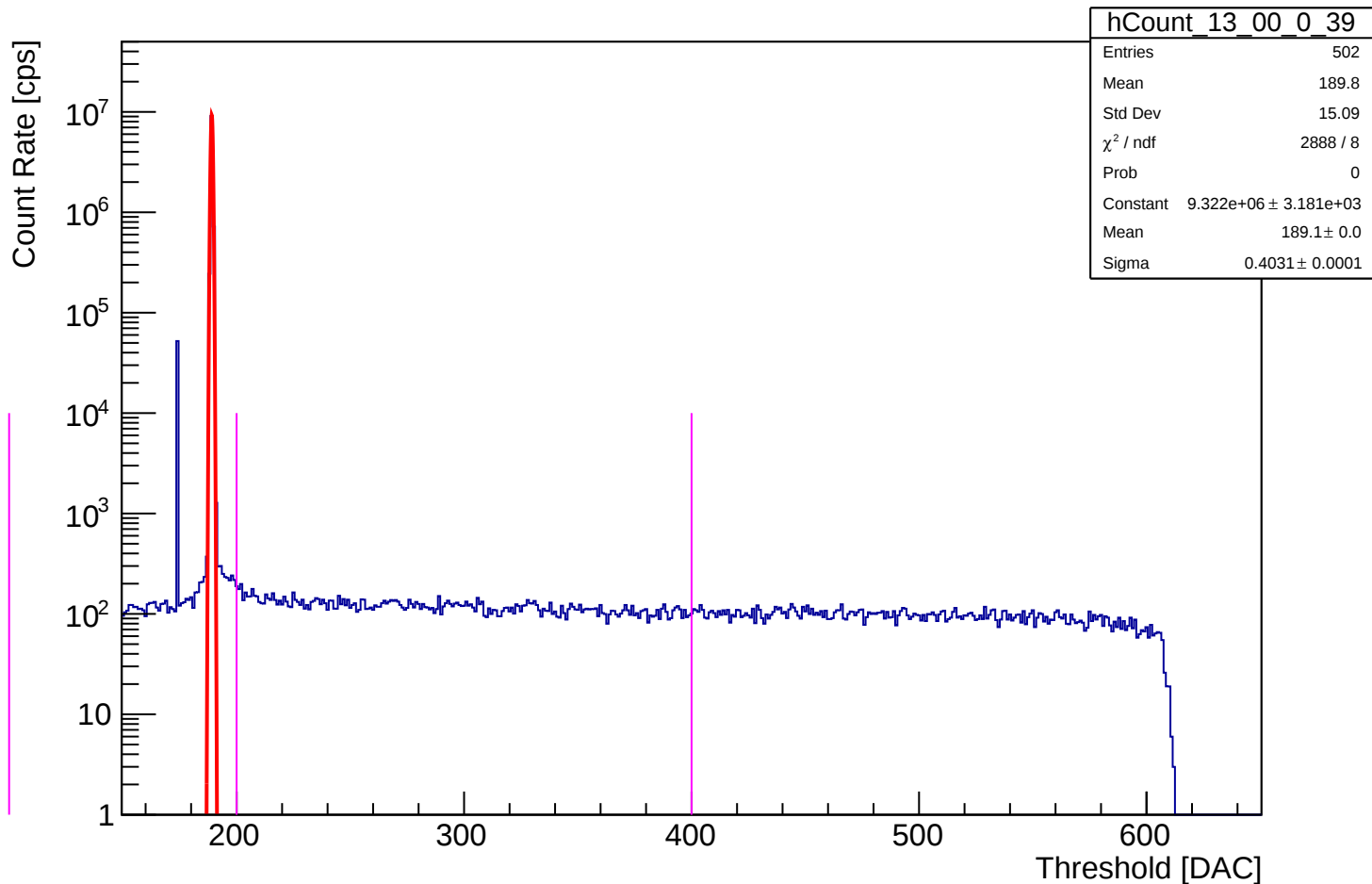
Row 1 Tile 1 Pmt 1 Pixel 14 Slot 13 Fiber 0 Asic 0 Channel 38



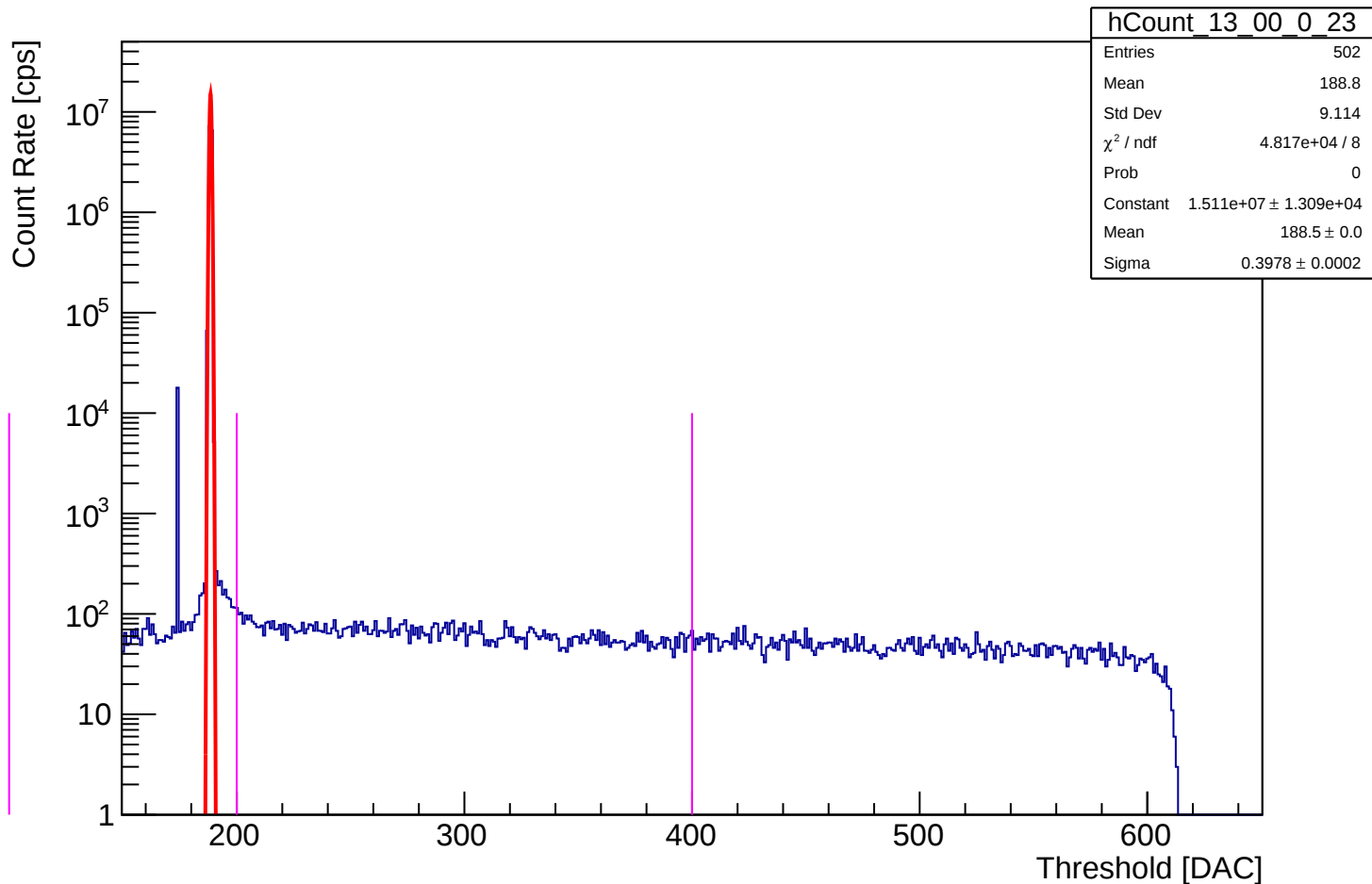
Row 1 Tile 1 Pmt 1 Pixel 15 Slot 13 Fiber 0 Asic 0 Channel 37



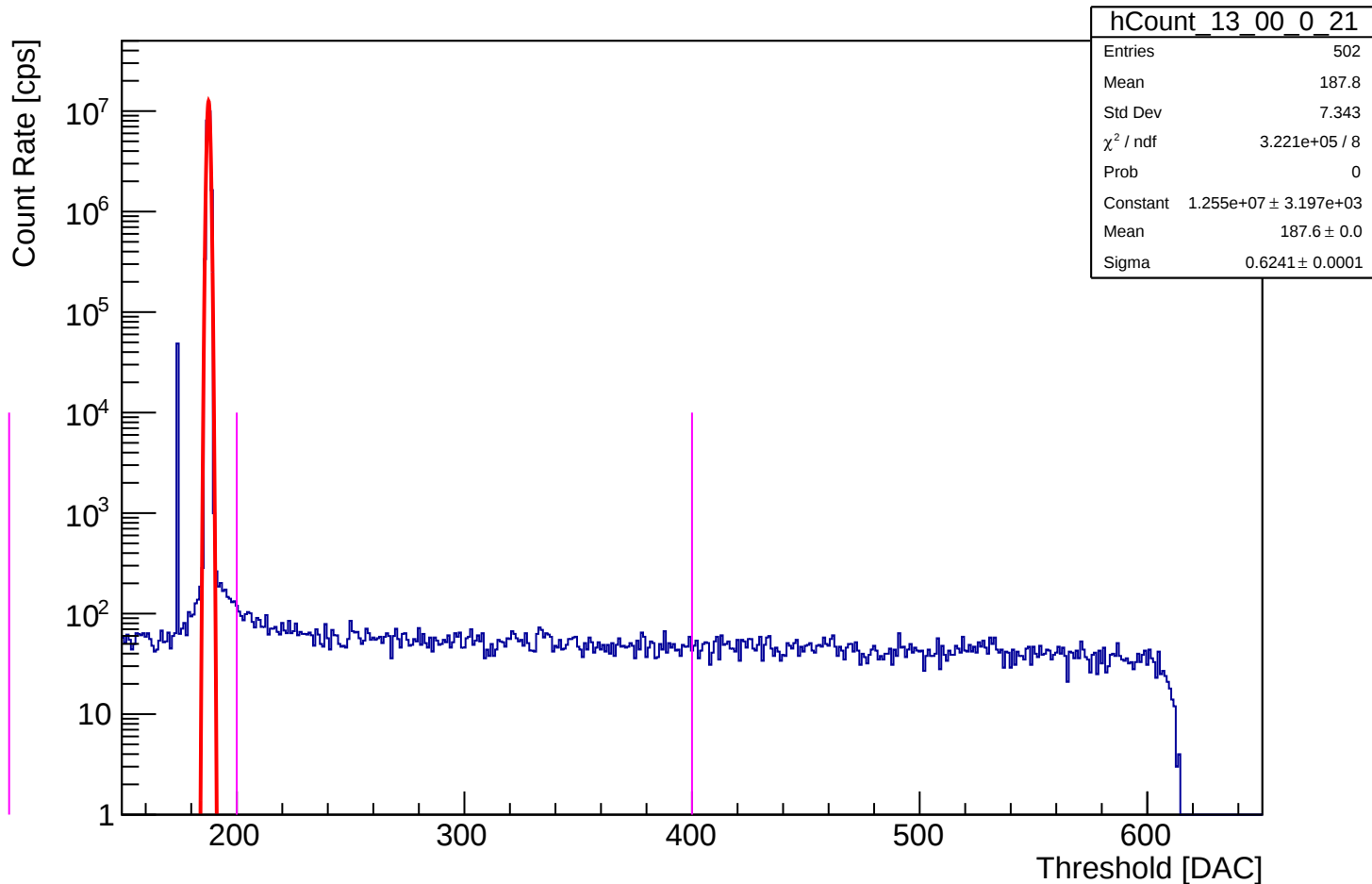
Row 1 Tile 1 Pmt 1 Pixel 16 Slot 13 Fiber 0 Asic 0 Channel 39



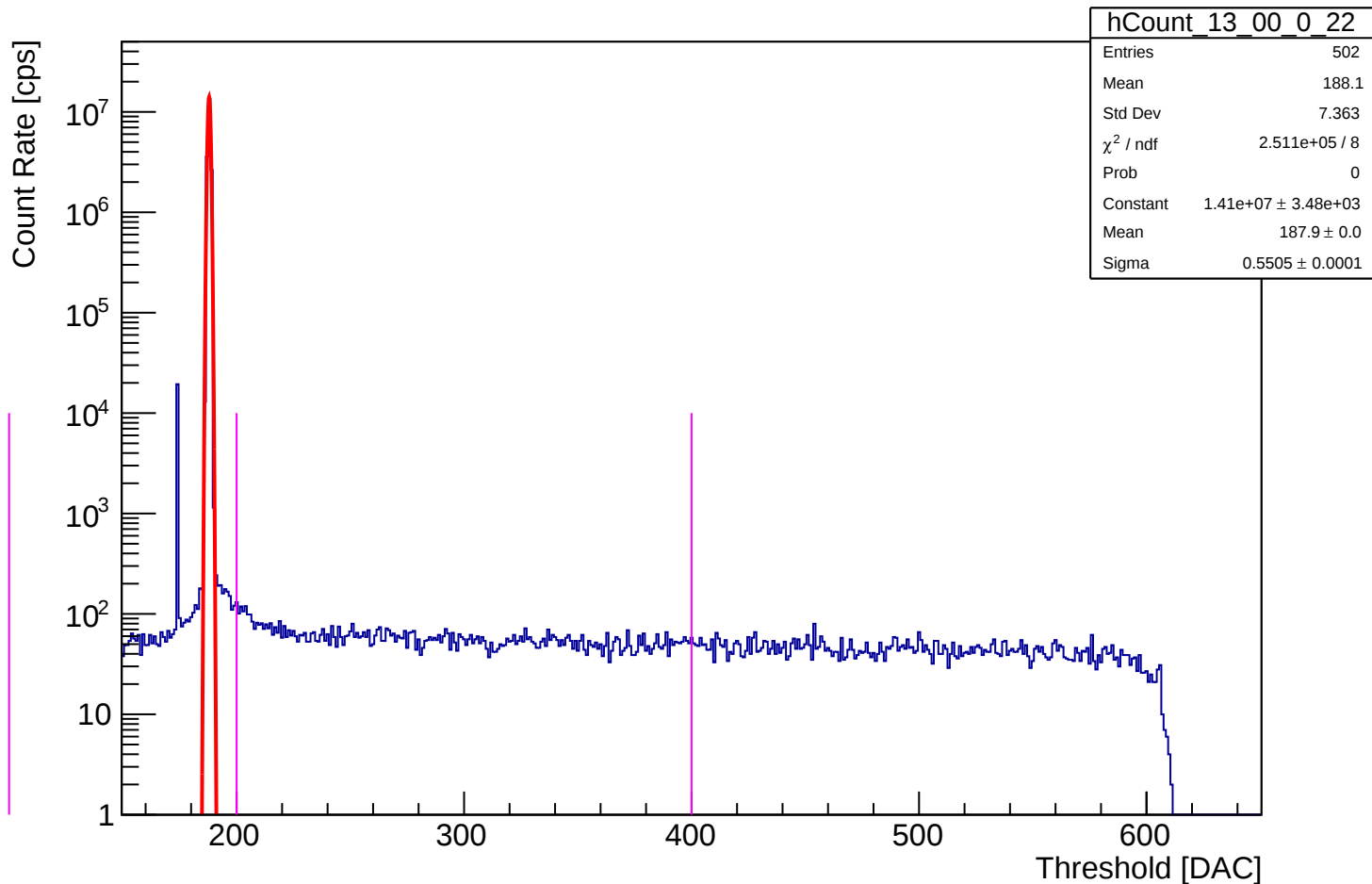
Row 1 Tile 1 Pmt 1 Pixel 17 Slot 13 Fiber 0 Asic 0 Channel 23



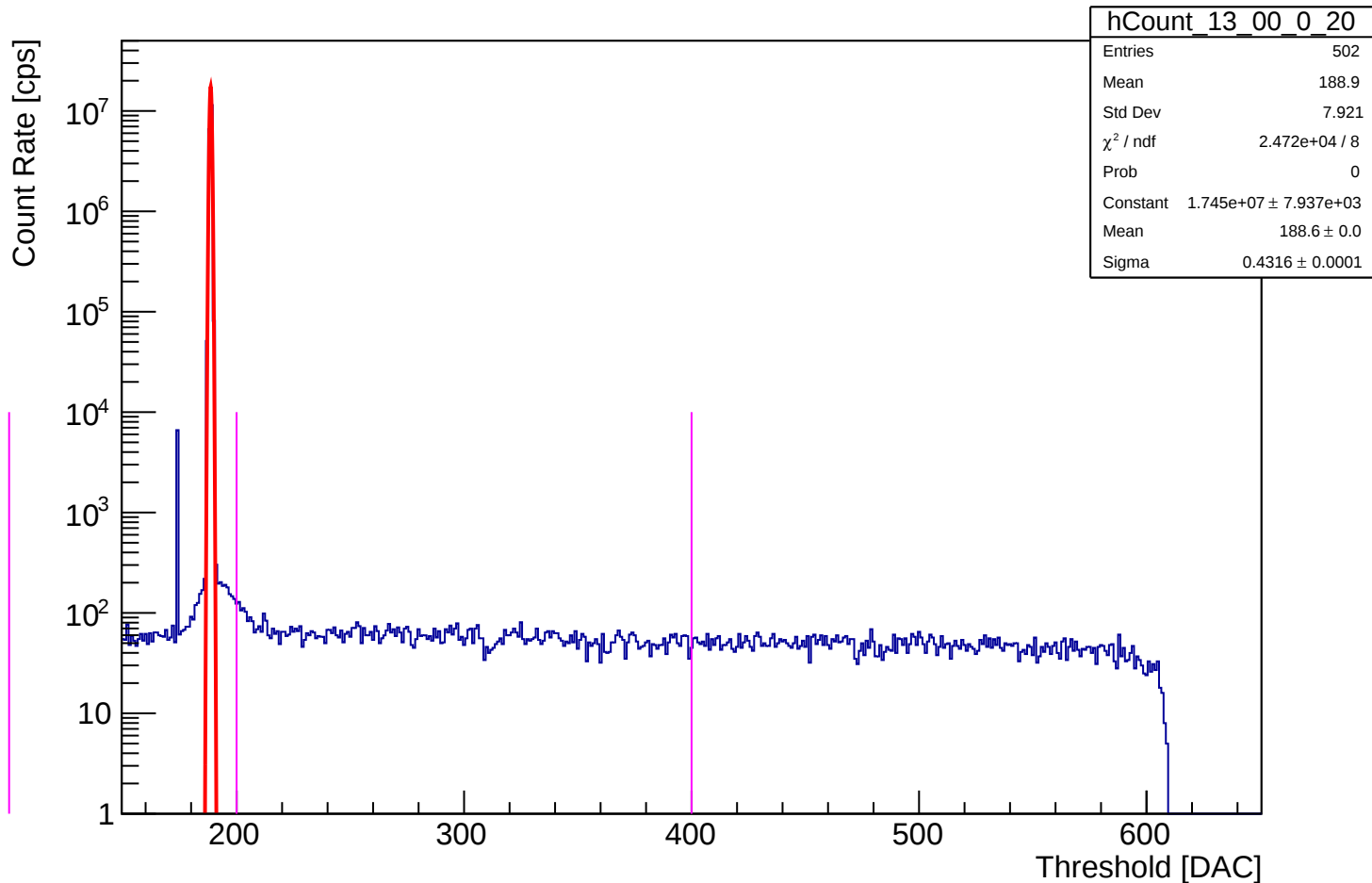
Row 1 Tile 1 Pmt 1 Pixel 18 Slot 13 Fiber 0 Asic 0 Channel 21



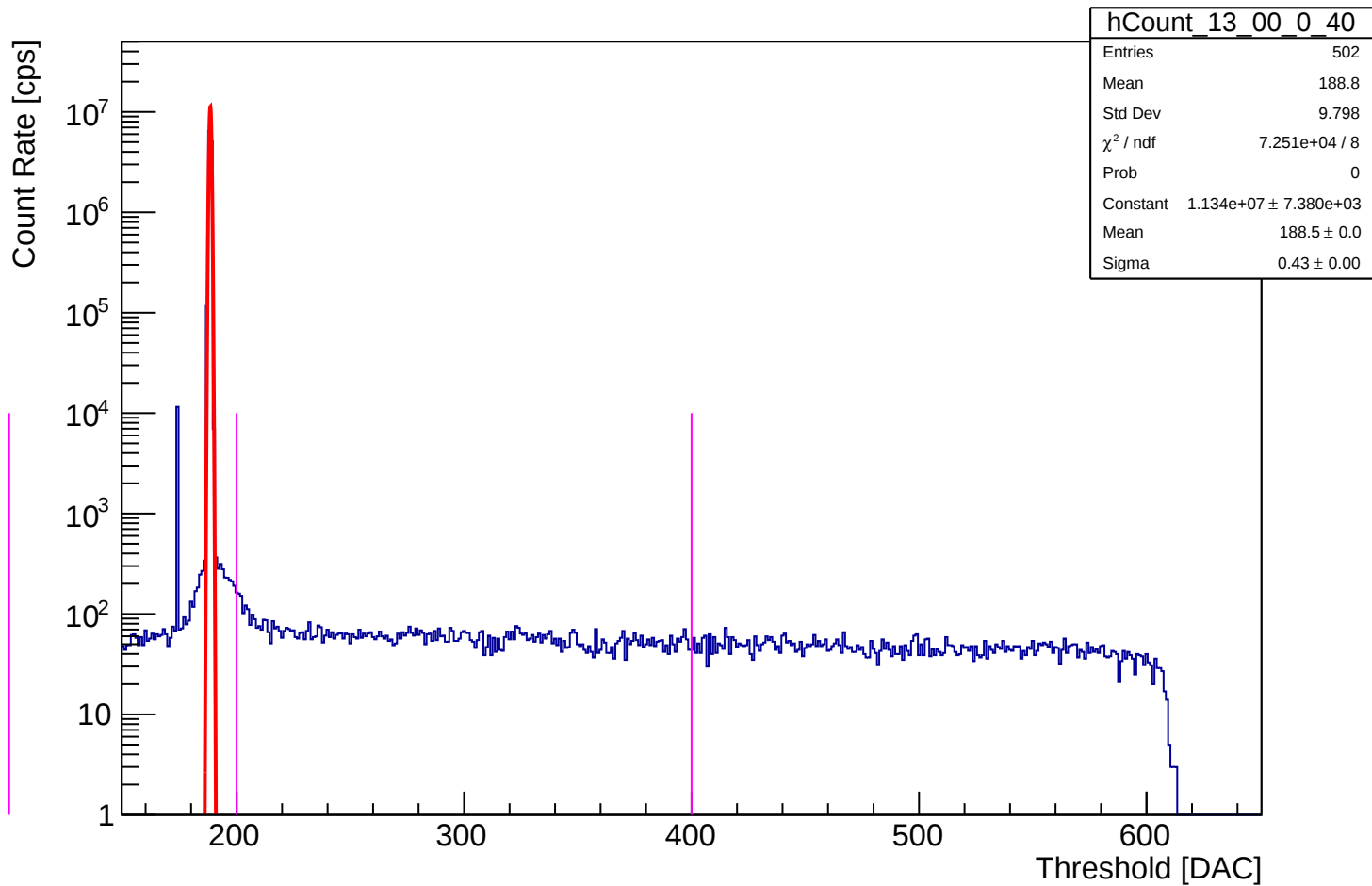
Row 1 Tile 1 Pmt 1 Pixel 19 Slot 13 Fiber 0 Asic 0 Channel 22



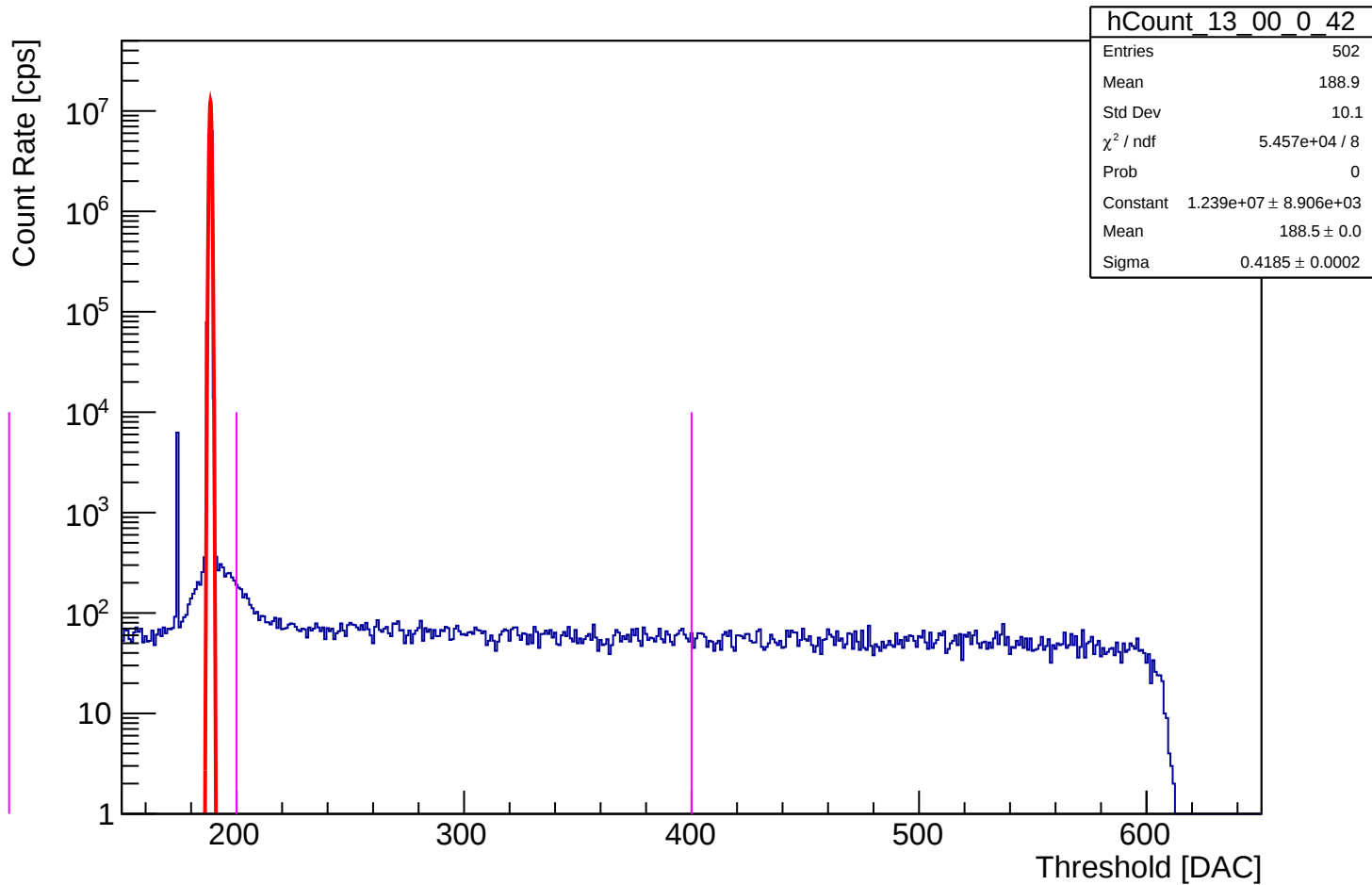
Row 1 Tile 1 Pmt 1 Pixel 20 Slot 13 Fiber 0 Asic 0 Channel 20



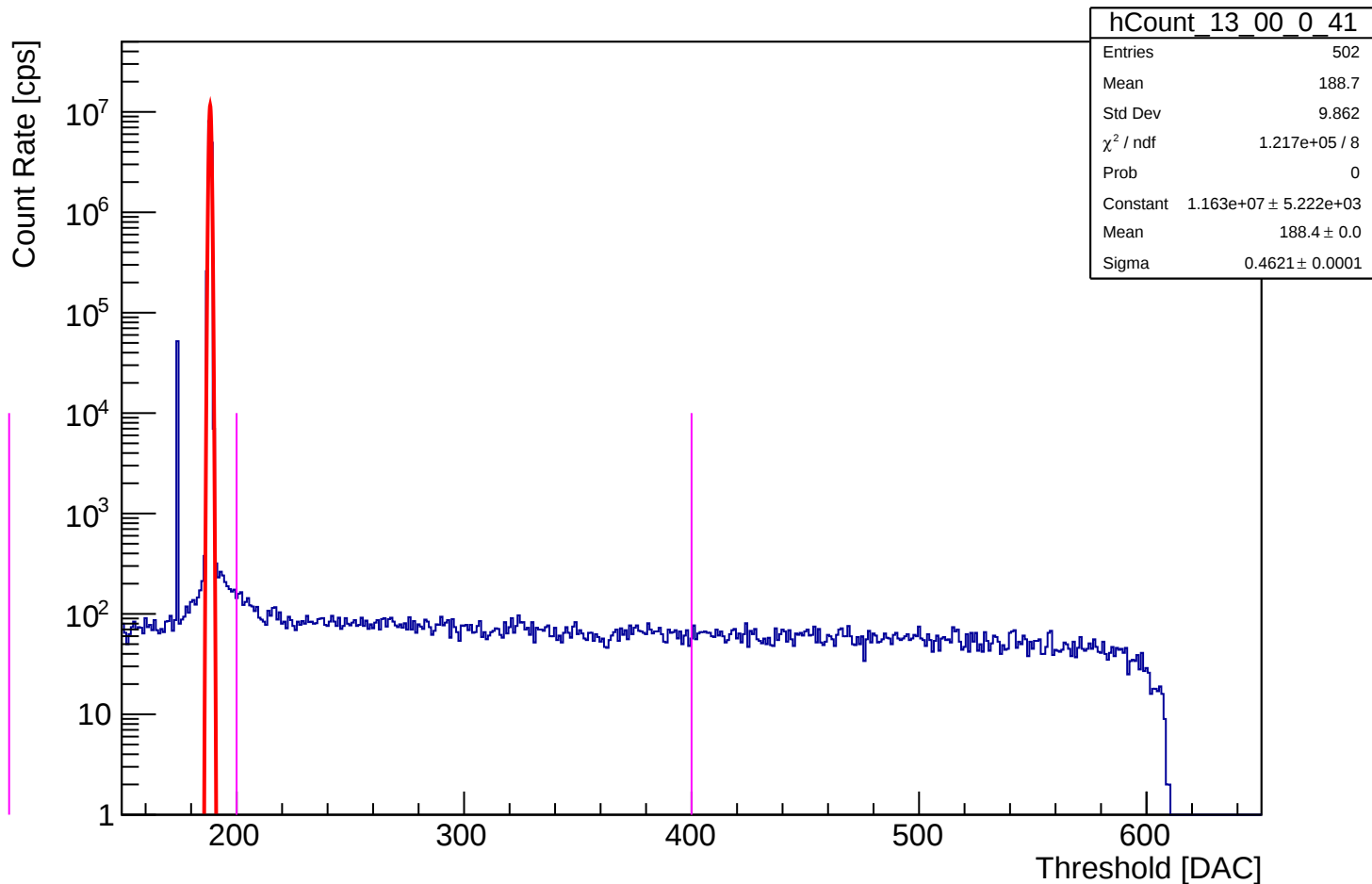
Row 1 Tile 1 Pmt 1 Pixel 21 Slot 13 Fiber 0 Asic 0 Channel 40



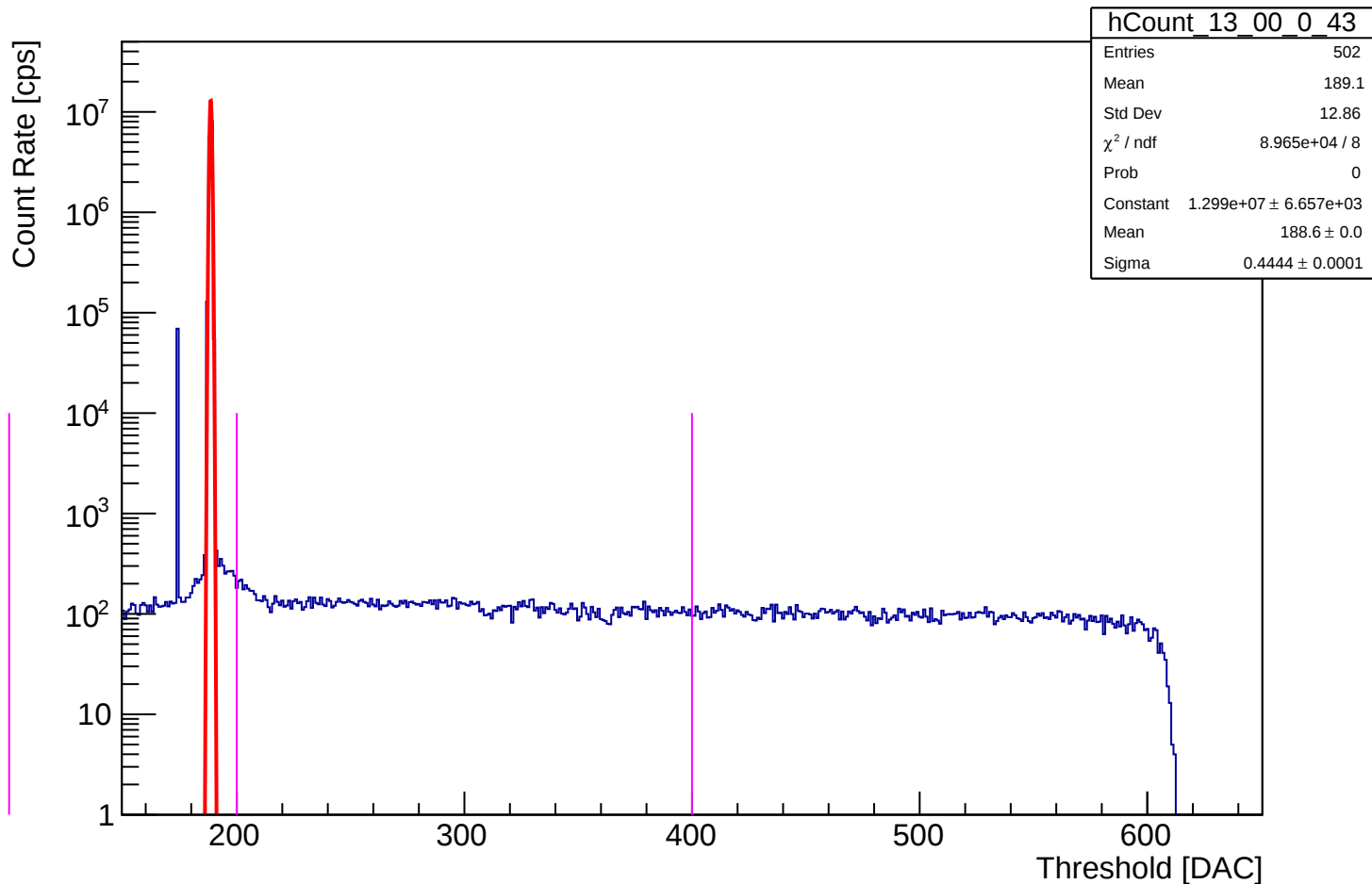
Row 1 Tile 1 Pmt 1 Pixel 22 Slot 13 Fiber 0 Asic 0 Channel 42



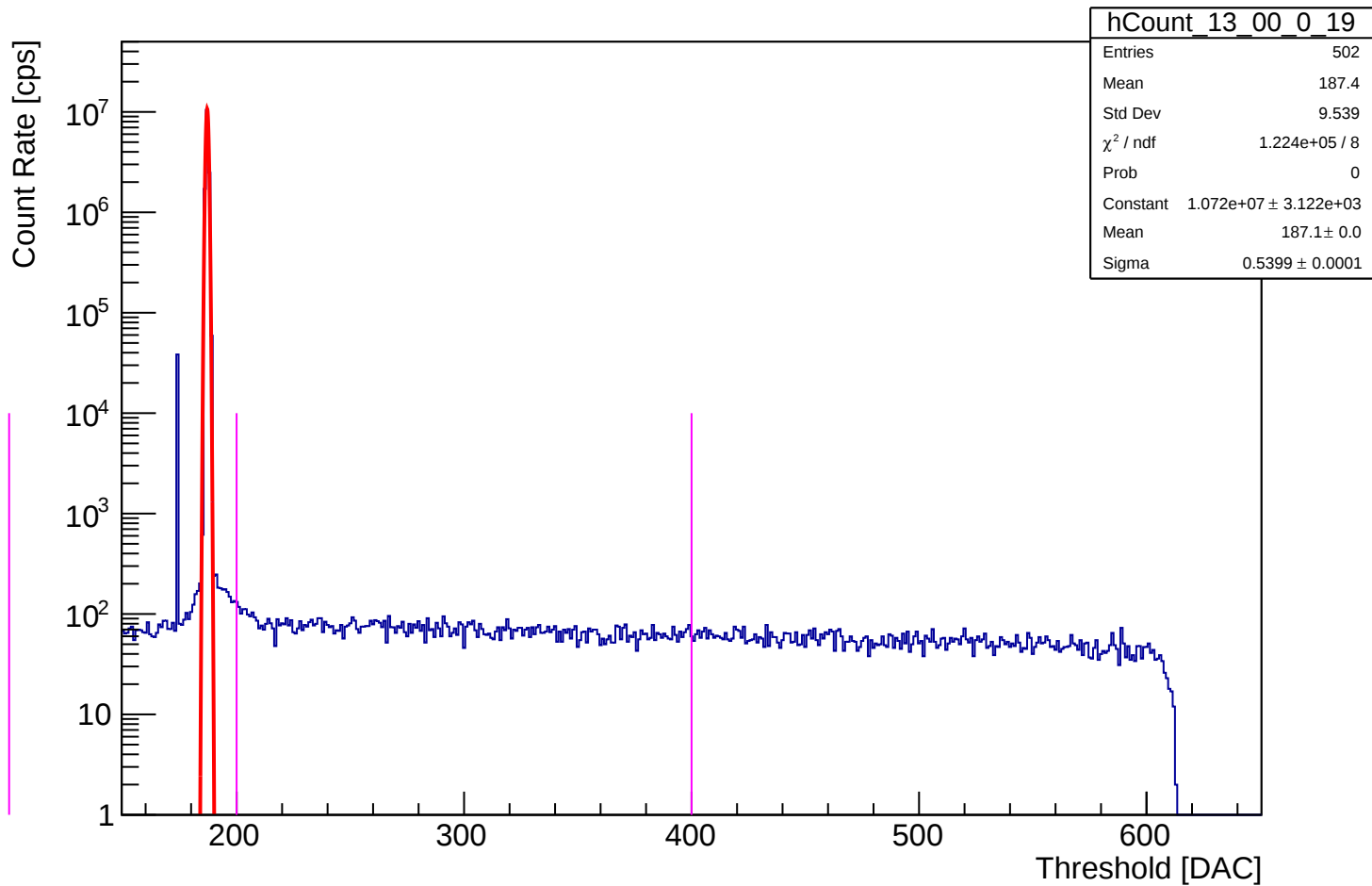
Row 1 Tile 1 Pmt 1 Pixel 23 Slot 13 Fiber 0 Asic 0 Channel 41



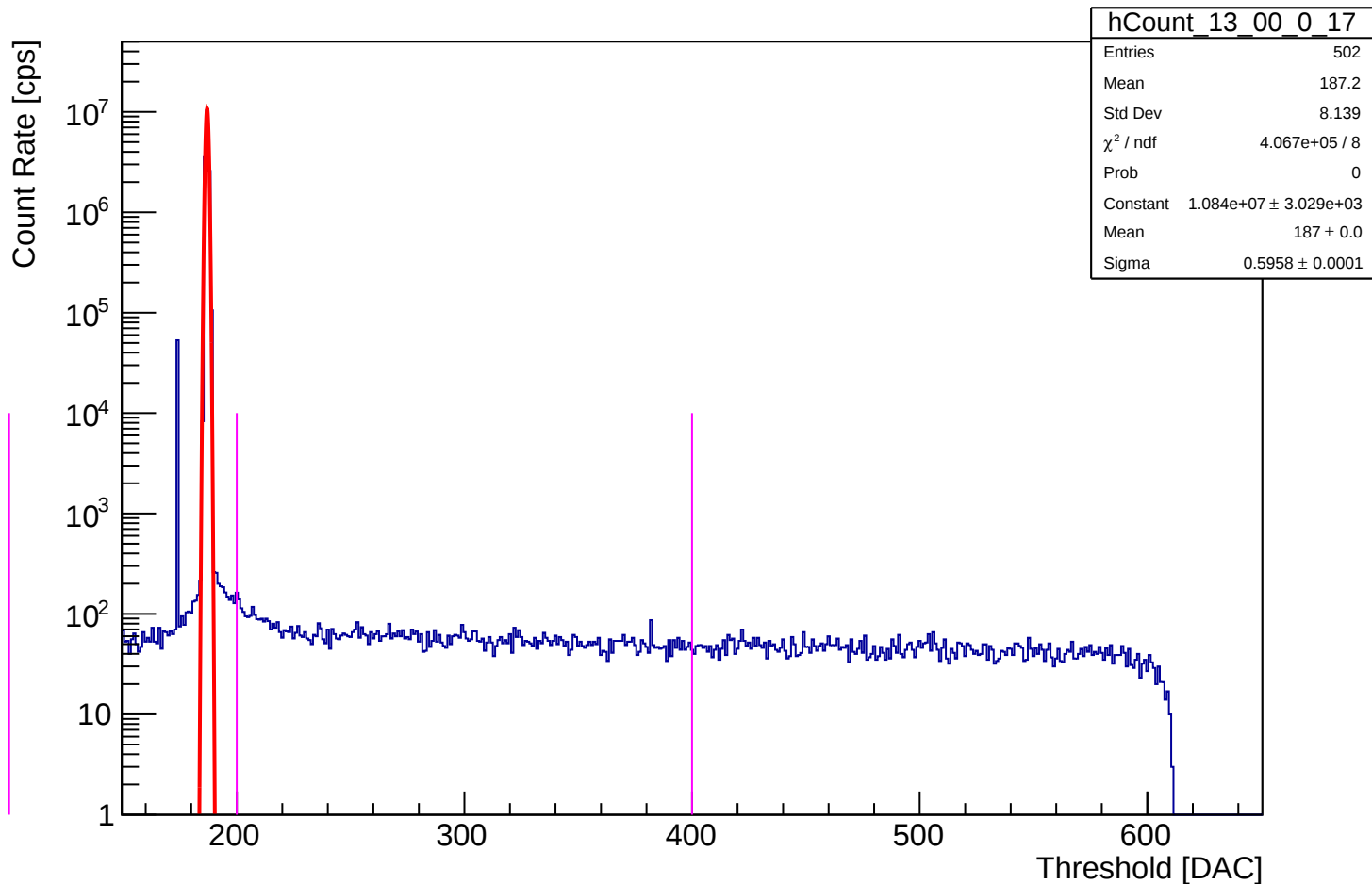
Row 1 Tile 1 Pmt 1 Pixel 24 Slot 13 Fiber 0 Asic 0 Channel 43



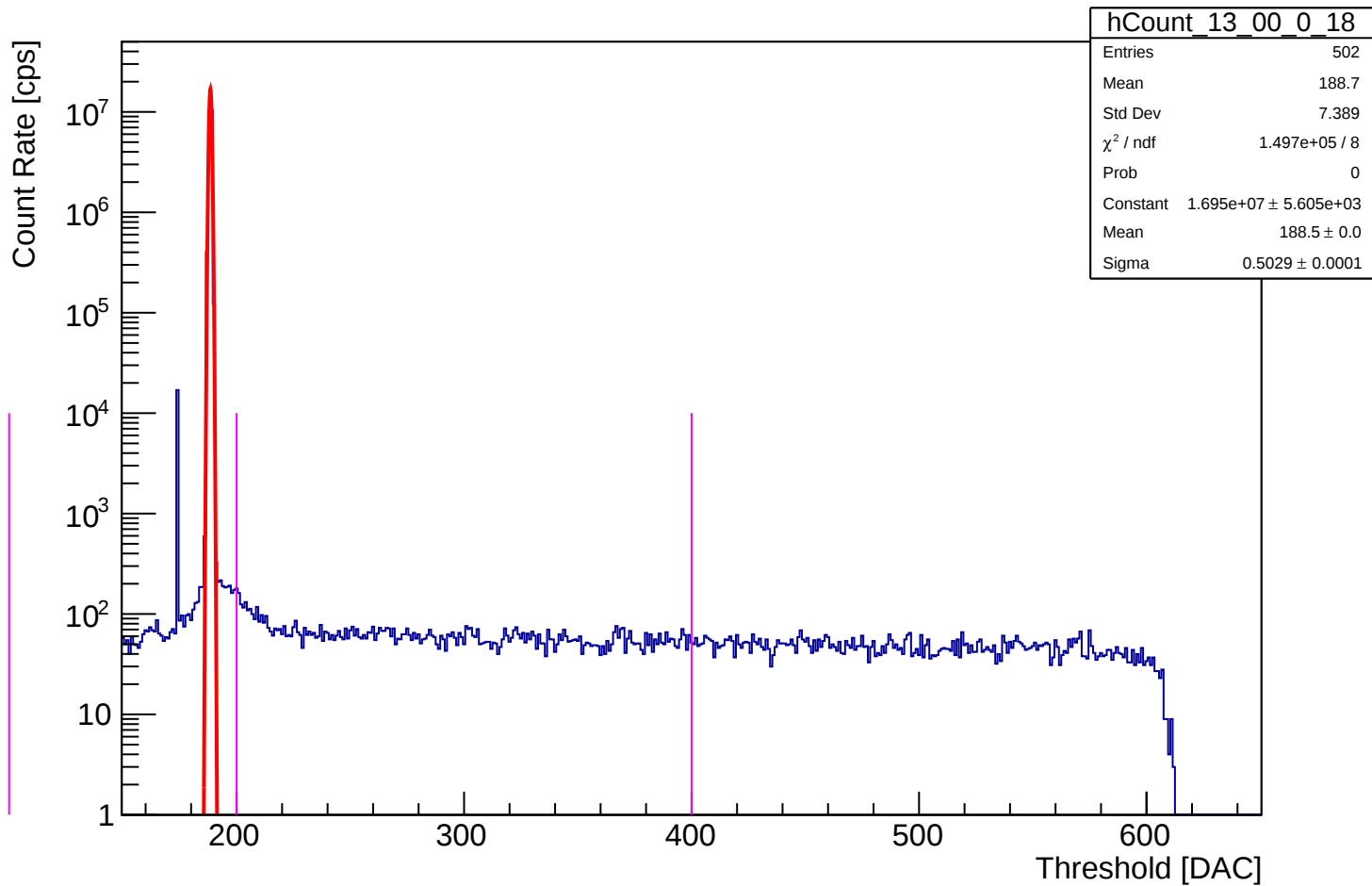
Row 1 Tile 1 Pmt 1 Pixel 25 Slot 13 Fiber 0 Asic 0 Channel 19



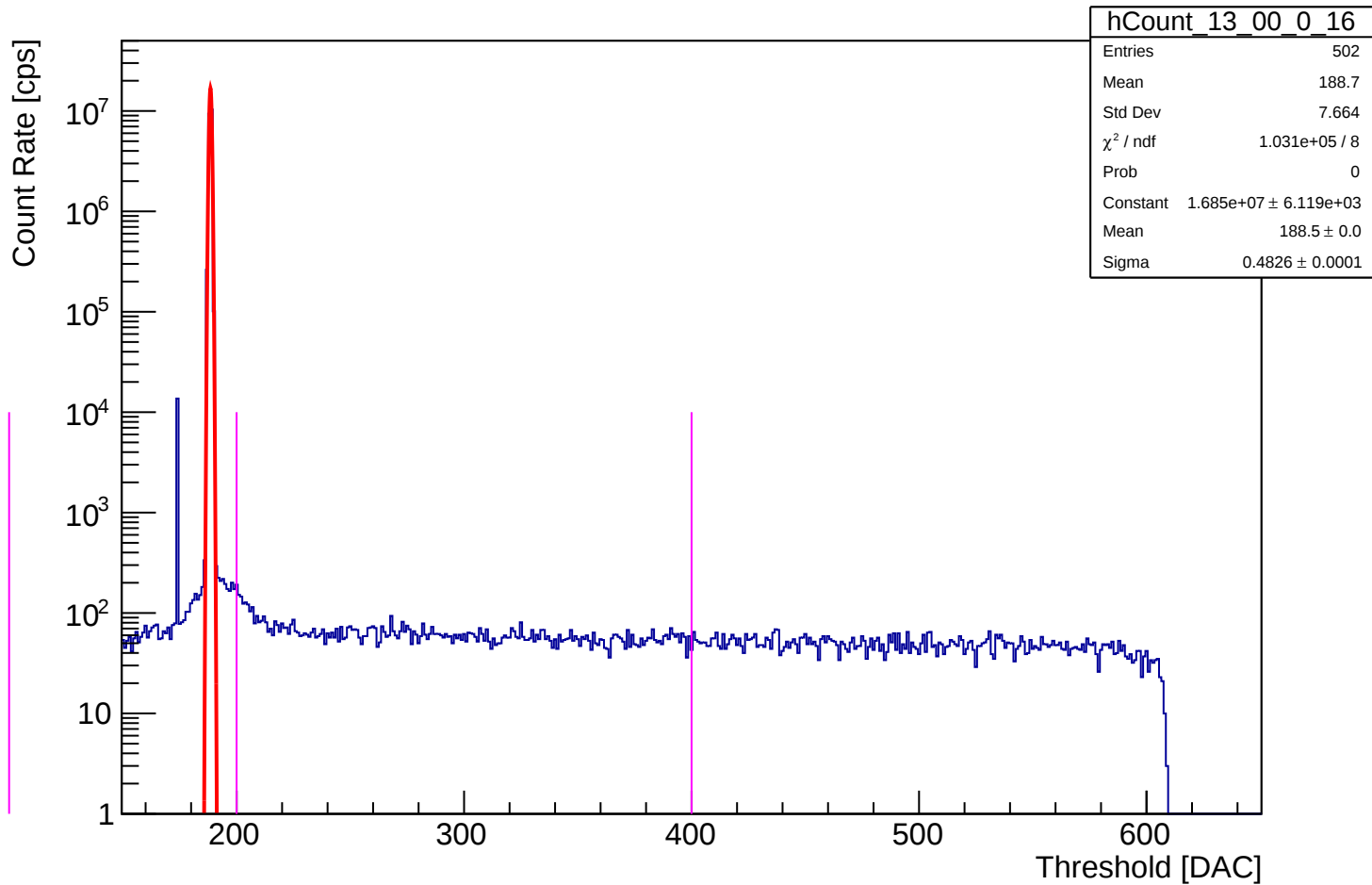
Row 1 Tile 1 Pmt 1 Pixel 26 Slot 13 Fiber 0 Asic 0 Channel 17



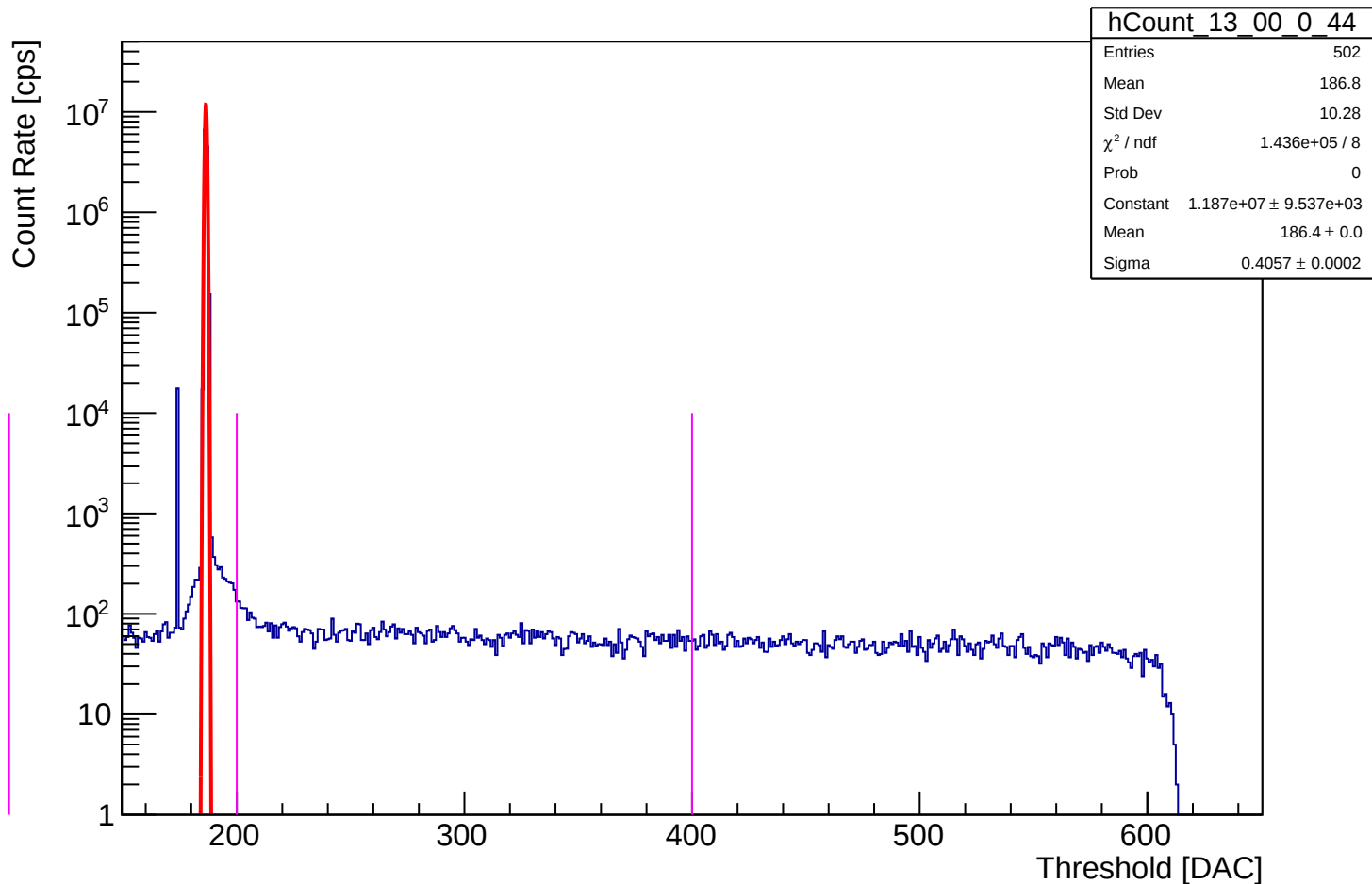
Row 1 Tile 1 Pmt 1 Pixel 27 Slot 13 Fiber 0 Asic 0 Channel 18



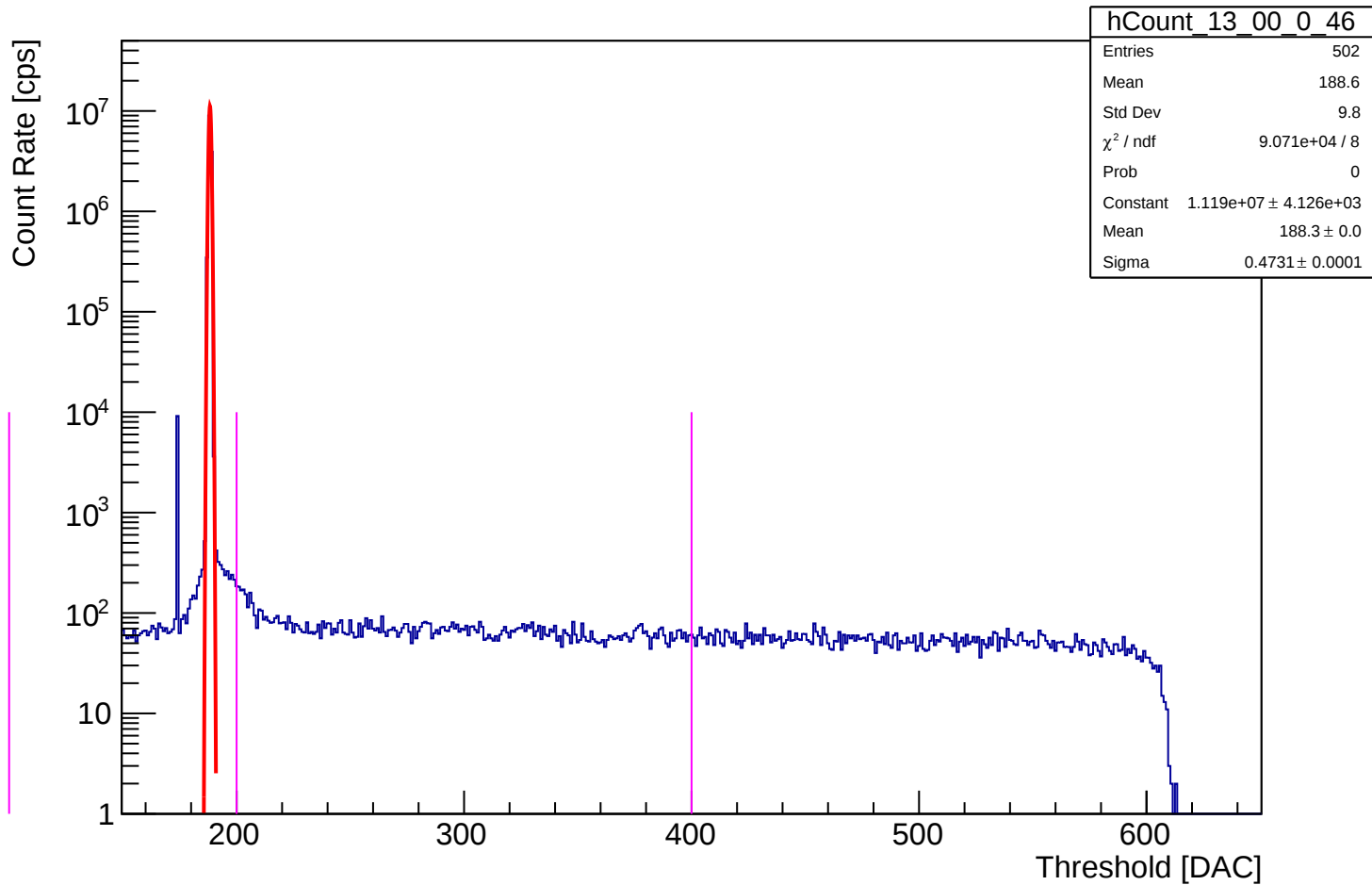
Row 1 Tile 1 Pmt 1 Pixel 28 Slot 13 Fiber 0 Asic 0 Channel 16



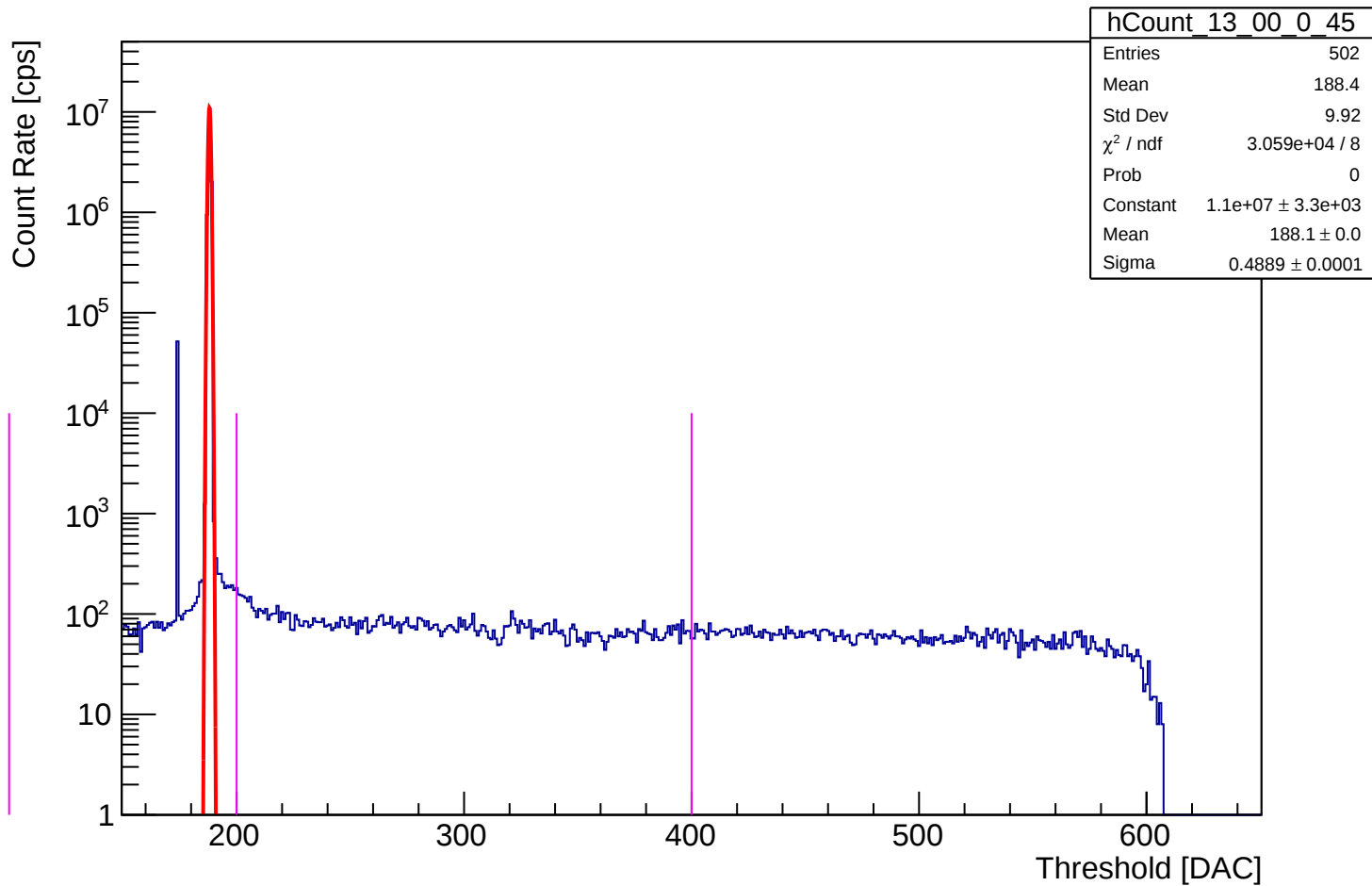
Row 1 Tile 1 Pmt 1 Pixel 29 Slot 13 Fiber 0 Asic 0 Channel 44



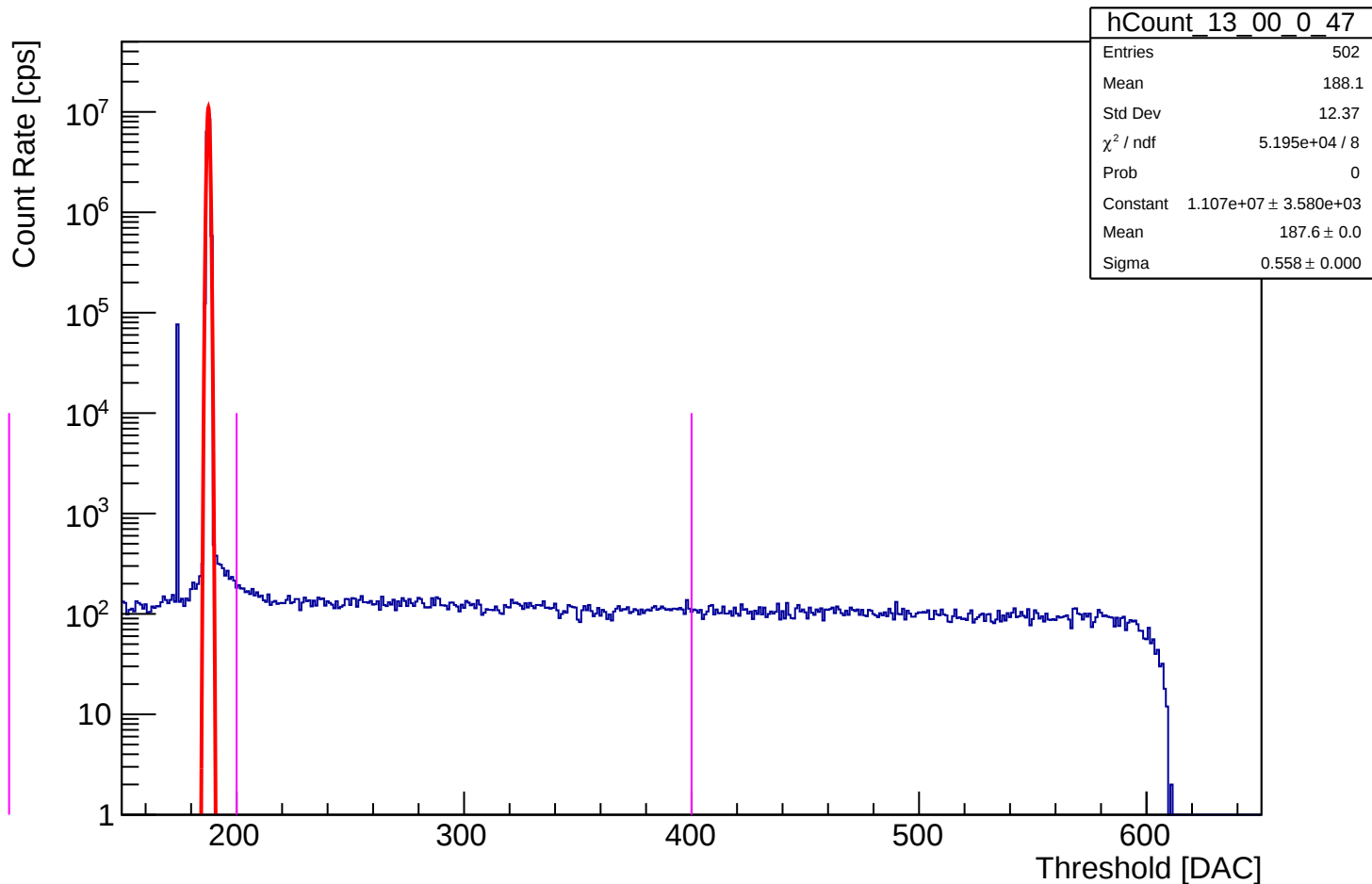
Row 1 Tile 1 Pmt 1 Pixel 30 Slot 13 Fiber 0 Asic 0 Channel 46



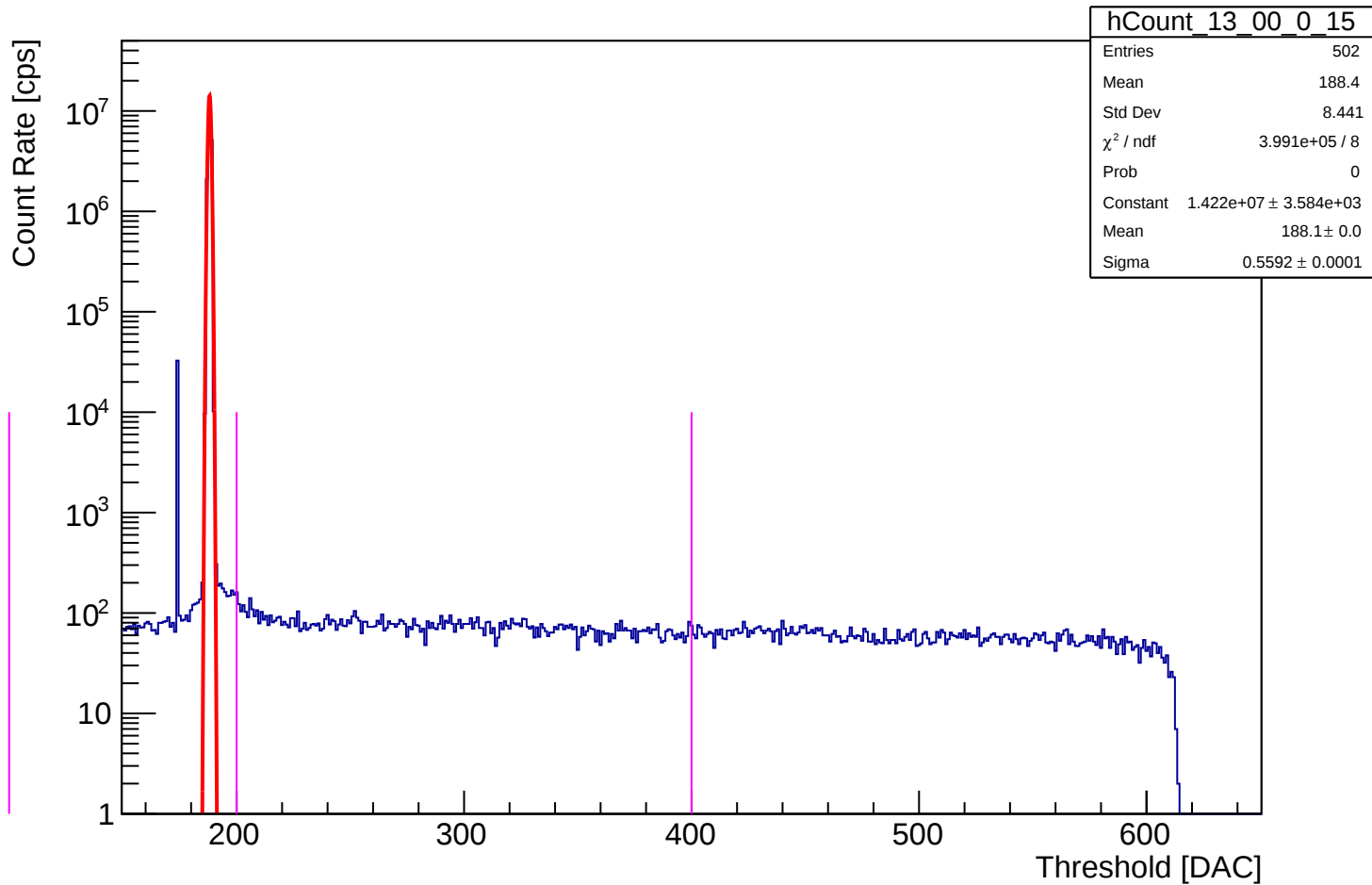
Row 1 Tile 1 Pmt 1 Pixel 31 Slot 13 Fiber 0 Asic 0 Channel 45



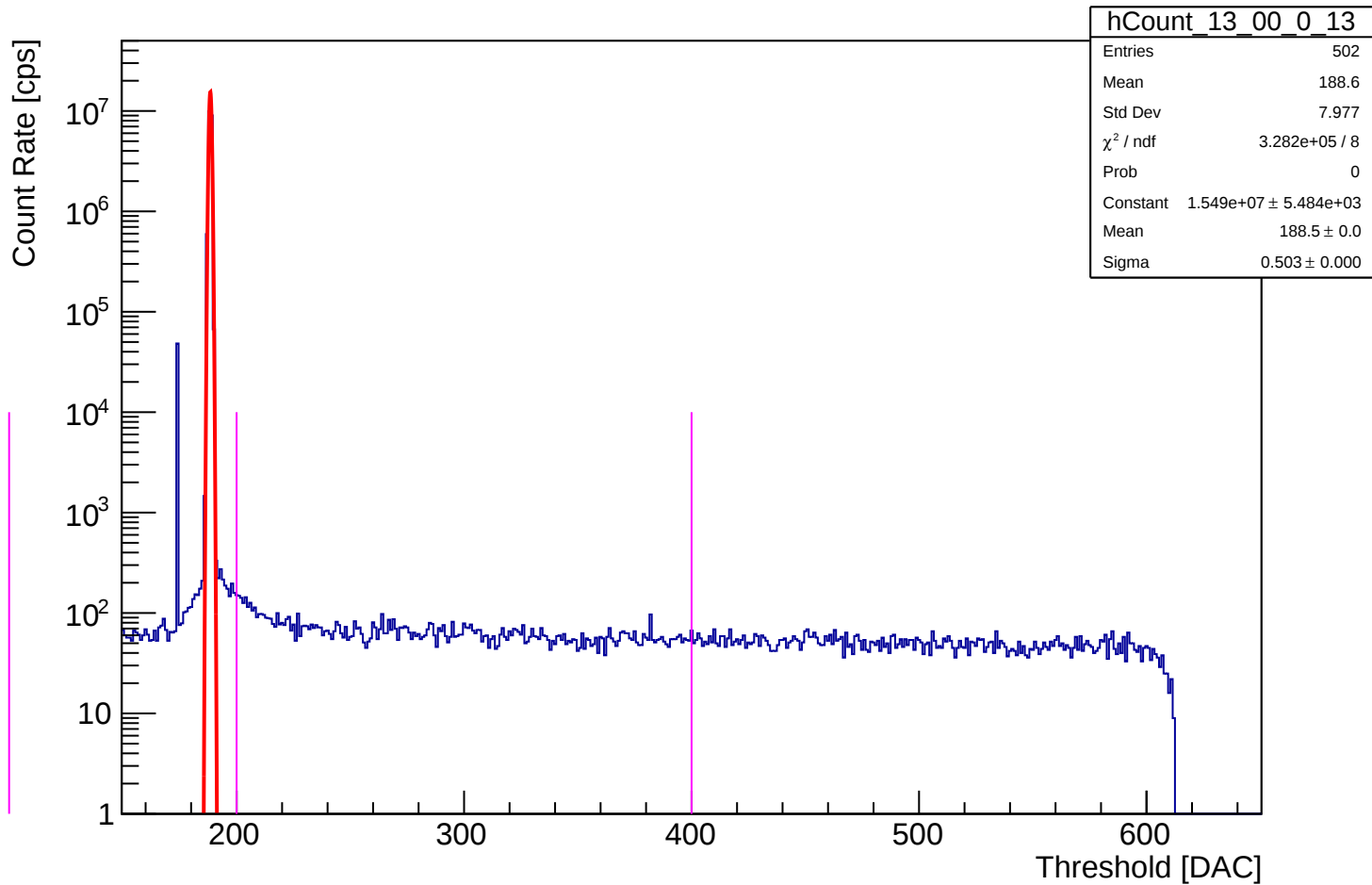
Row 1 Tile 1 Pmt 1 Pixel 32 Slot 13 Fiber 0 Asic 0 Channel 47



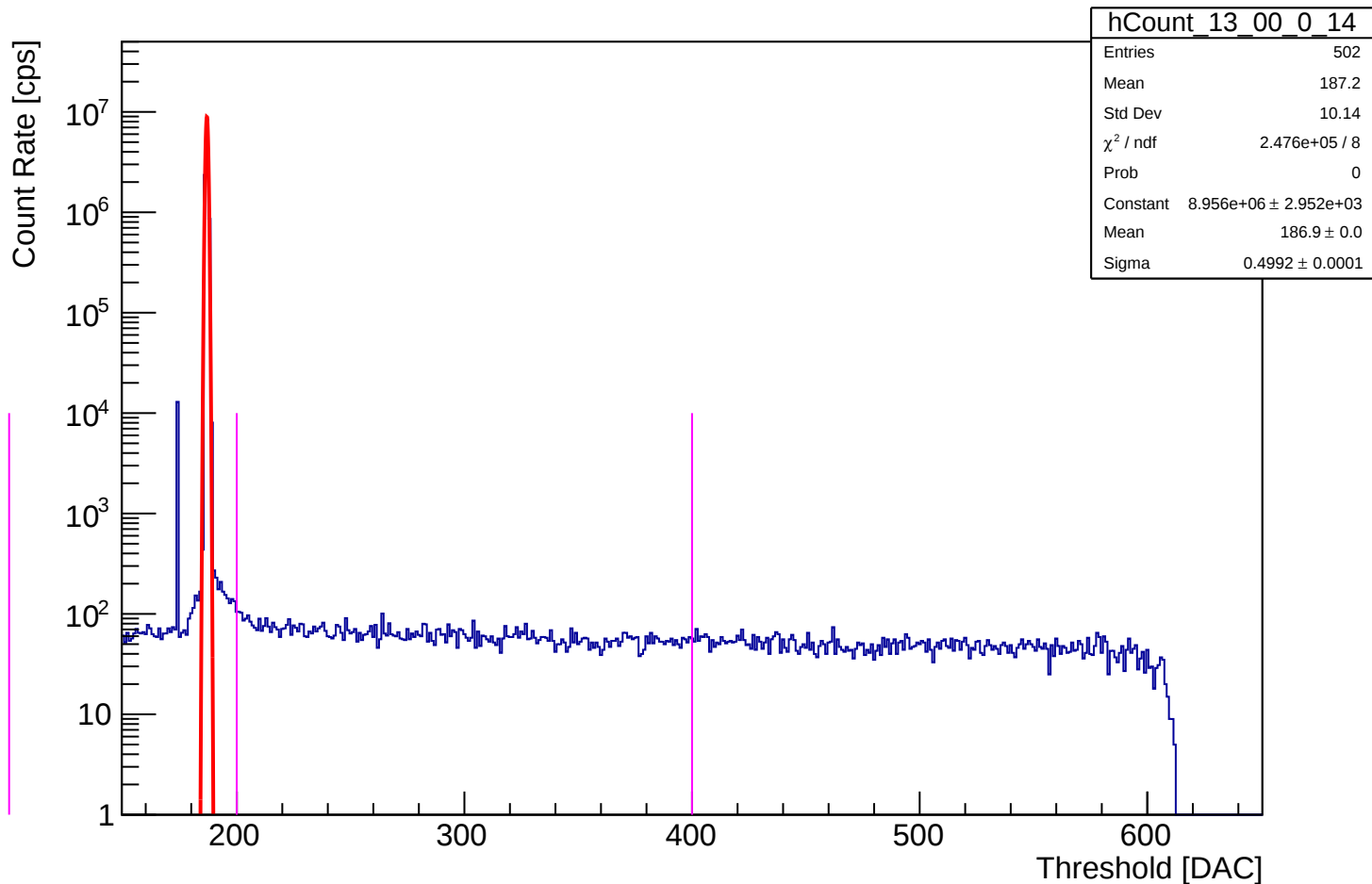
Row 1 Tile 1 Pmt 1 Pixel 33 Slot 13 Fiber 0 Asic 0 Channel 15



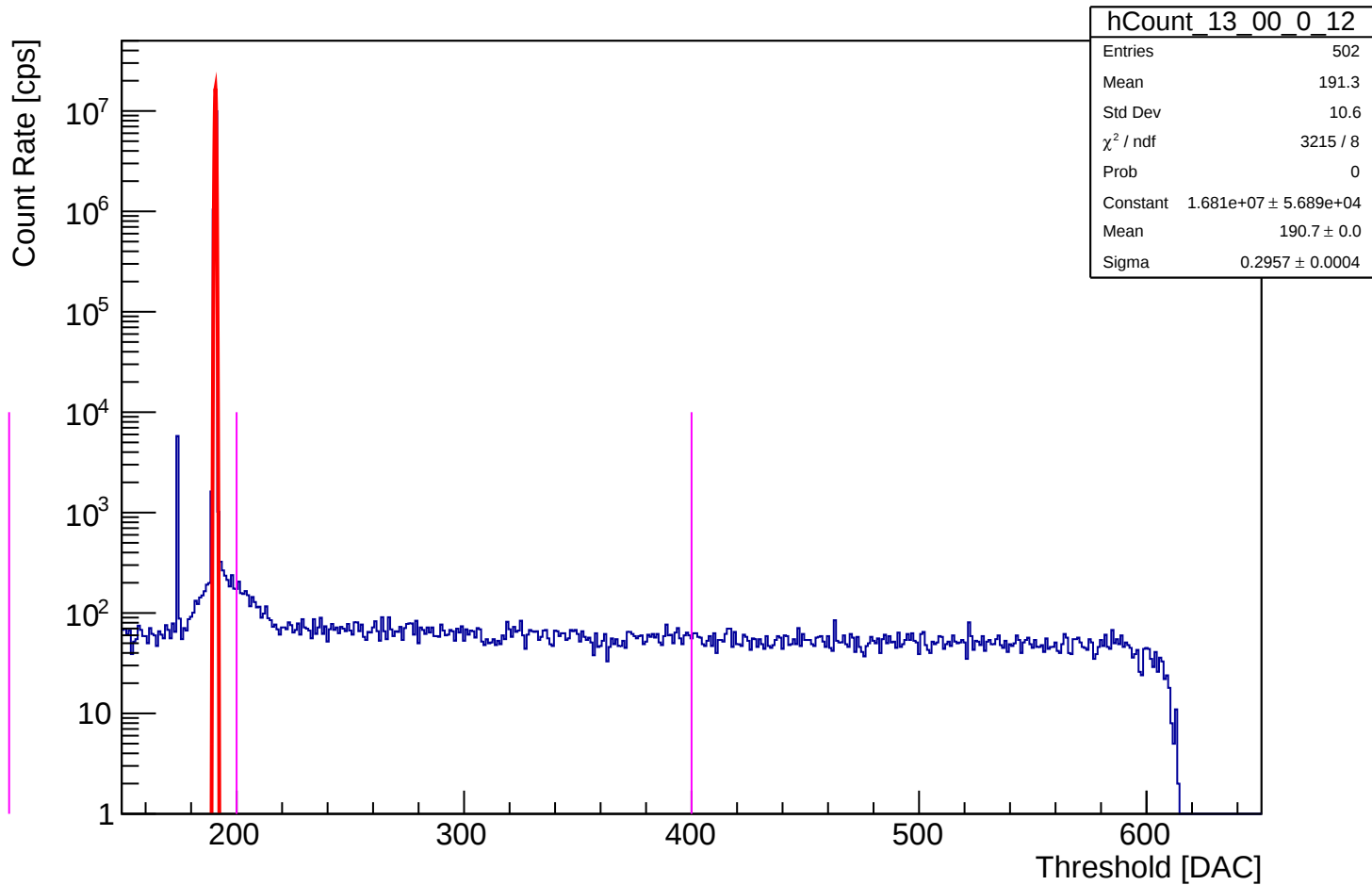
Row 1 Tile 1 Pmt 1 Pixel 34 Slot 13 Fiber 0 Asic 0 Channel 13



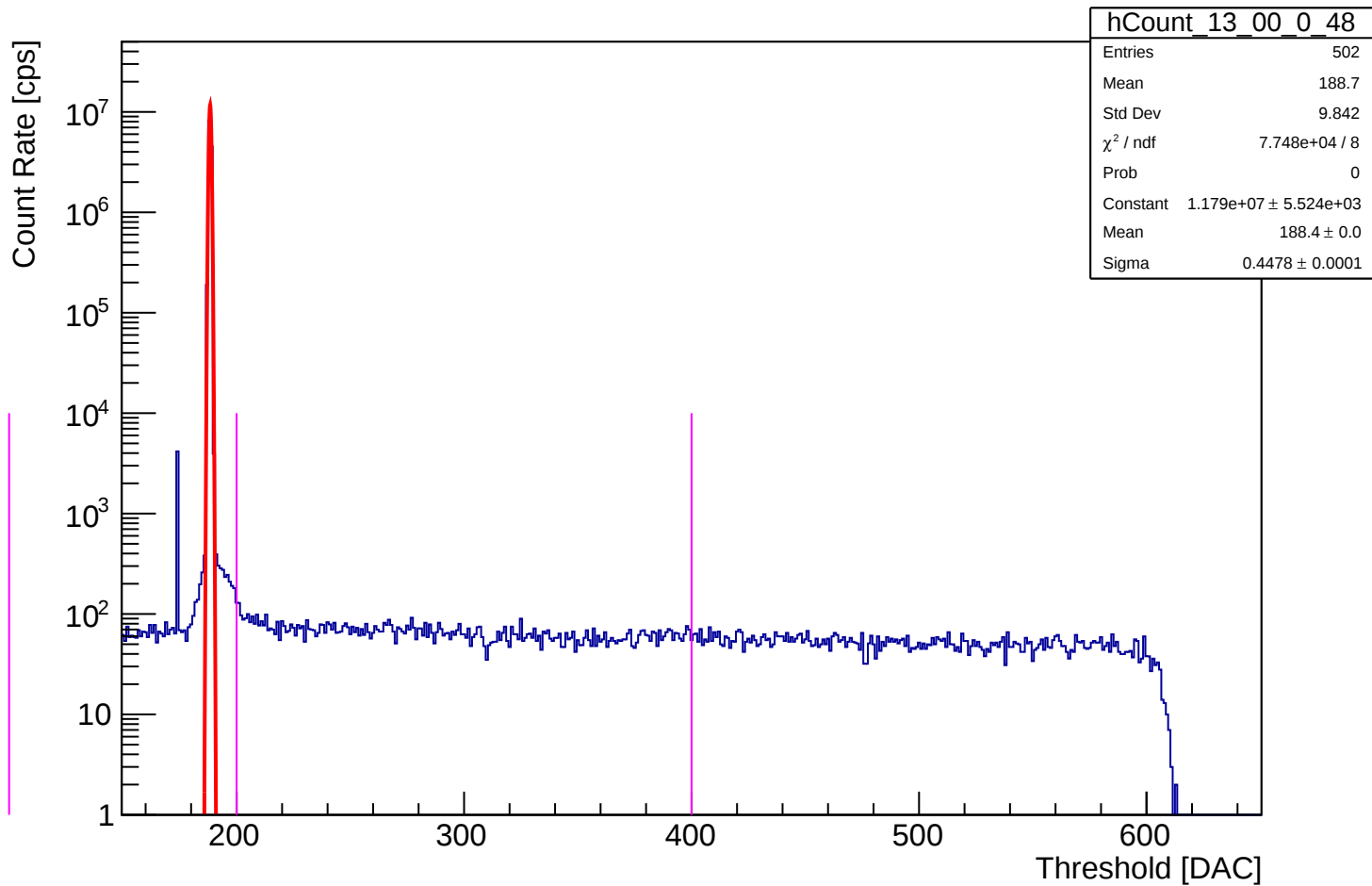
Row 1 Tile 1 Pmt 1 Pixel 35 Slot 13 Fiber 0 Asic 0 Channel 14



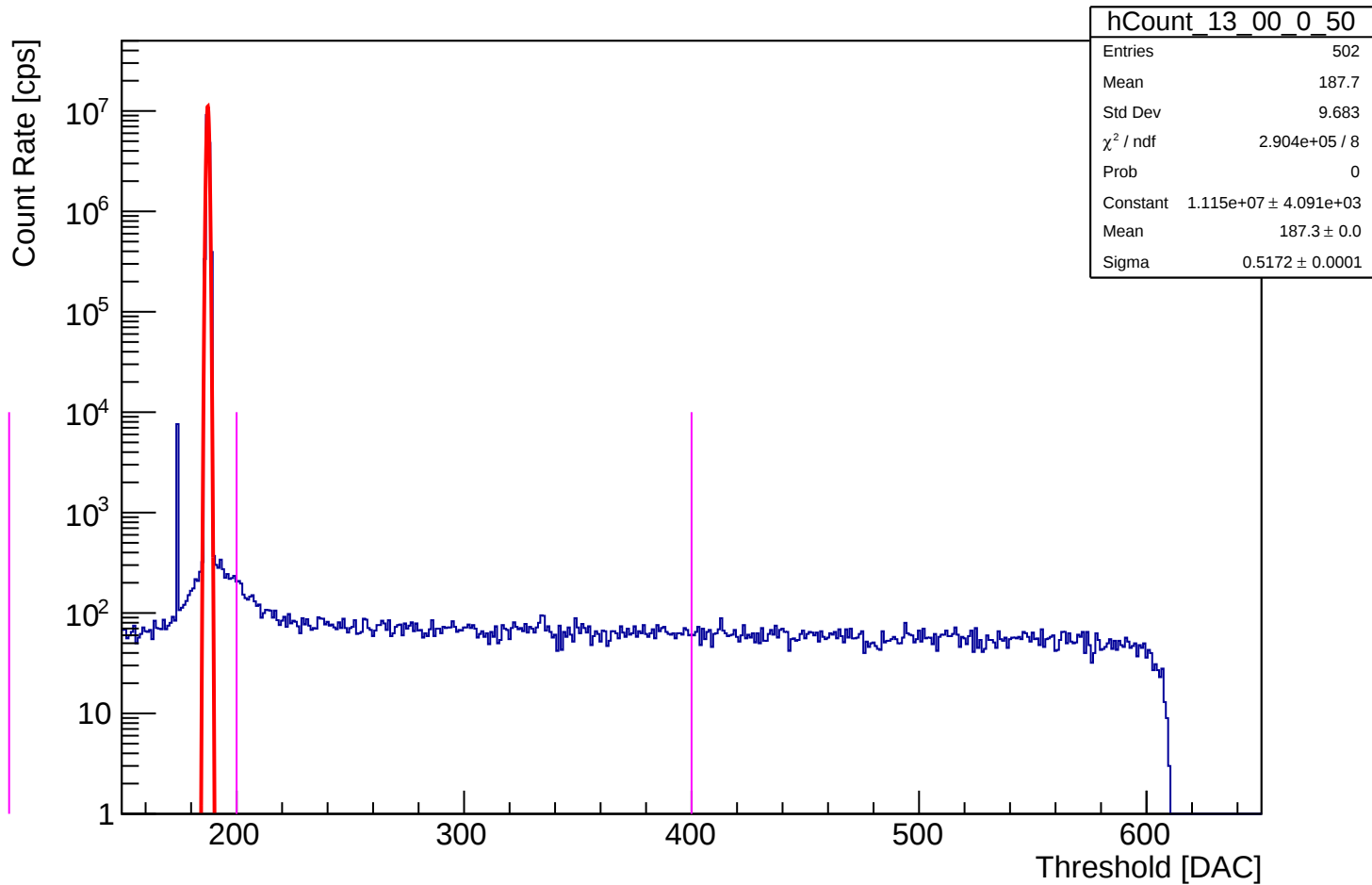
Row 1 Tile 1 Pmt 1 Pixel 36 Slot 13 Fiber 0 Asic 0 Channel 12



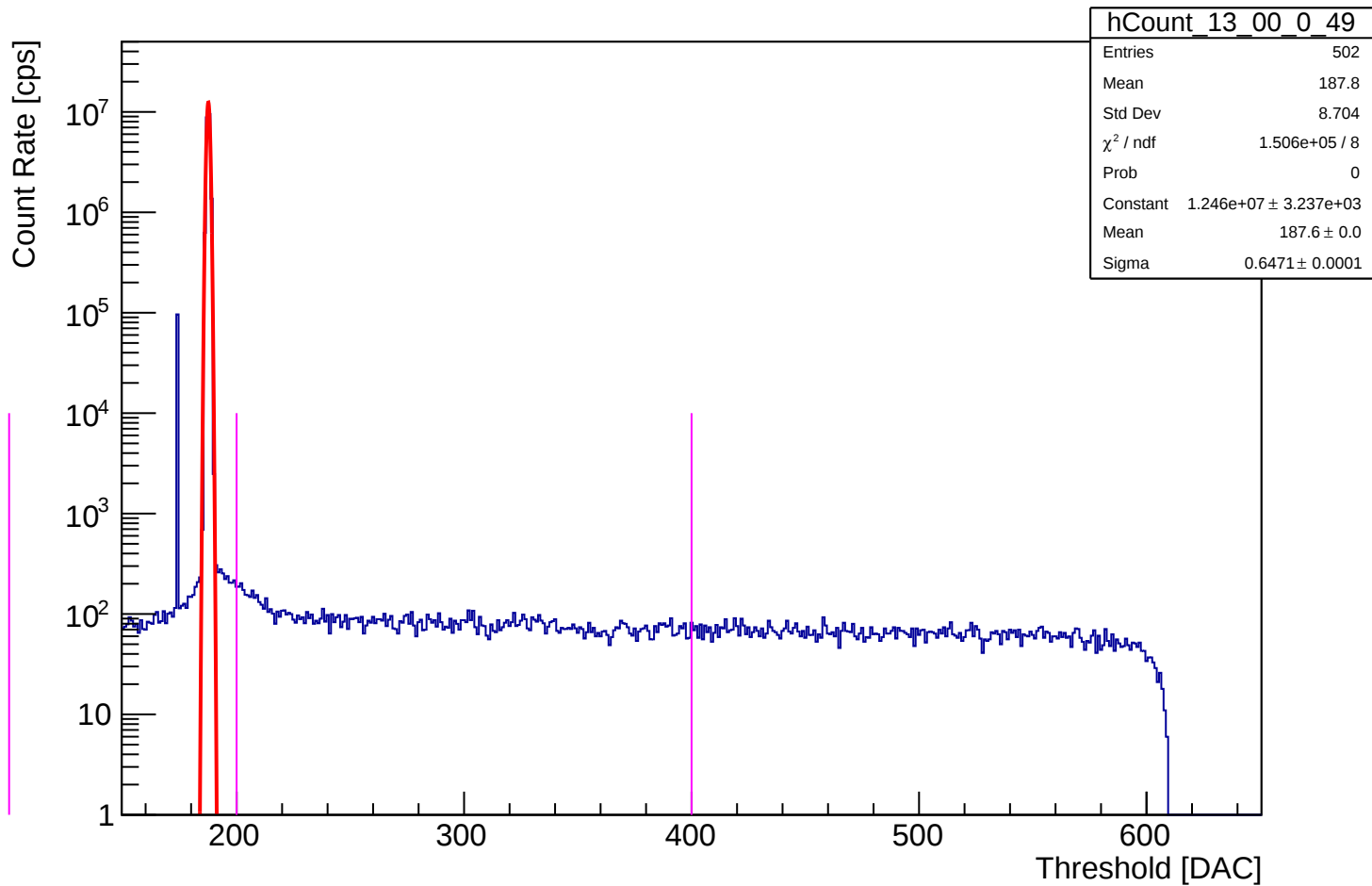
Row 1 Tile 1 Pmt 1 Pixel 37 Slot 13 Fiber 0 Asic 0 Channel 48



Row 1 Tile 1 Pmt 1 Pixel 38 Slot 13 Fiber 0 Asic 0 Channel 50

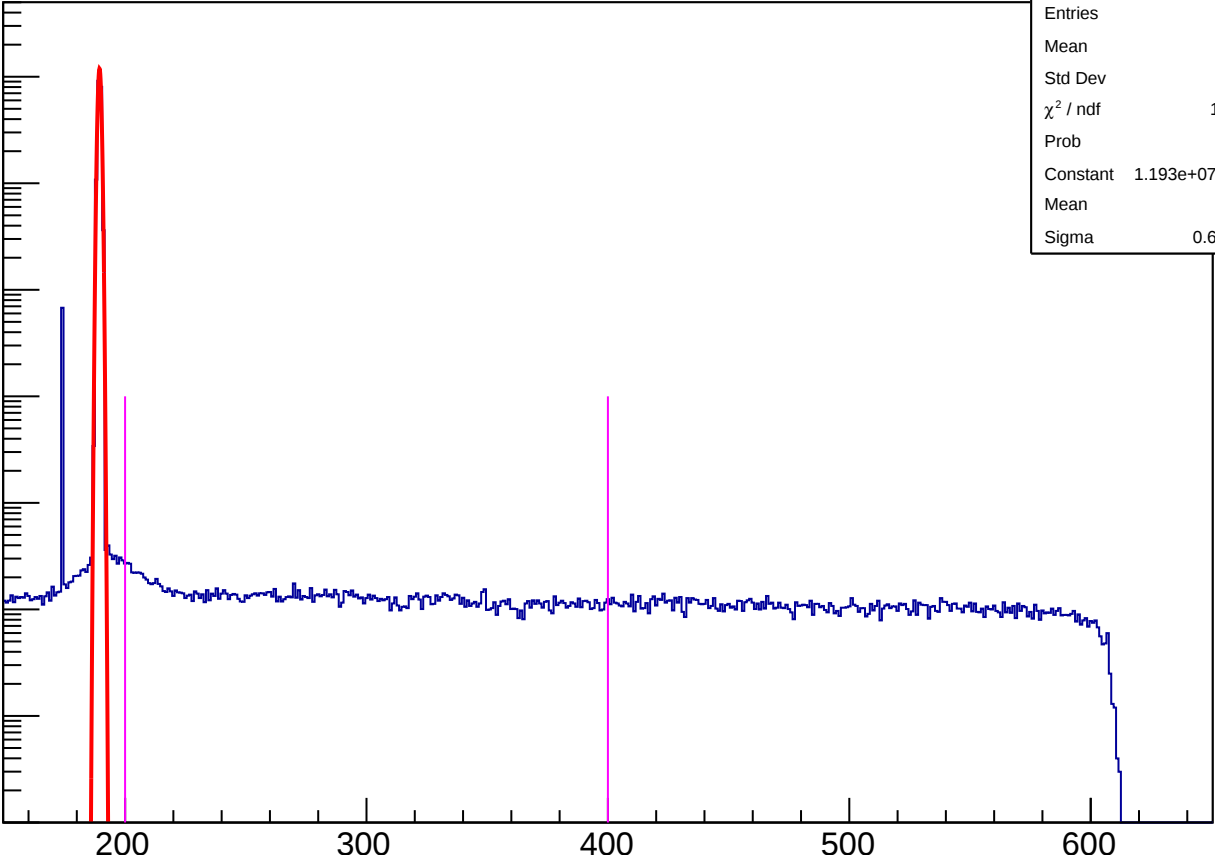


Row 1 Tile 1 Pmt 1 Pixel 39 Slot 13 Fiber 0 Asic 0 Channel 49



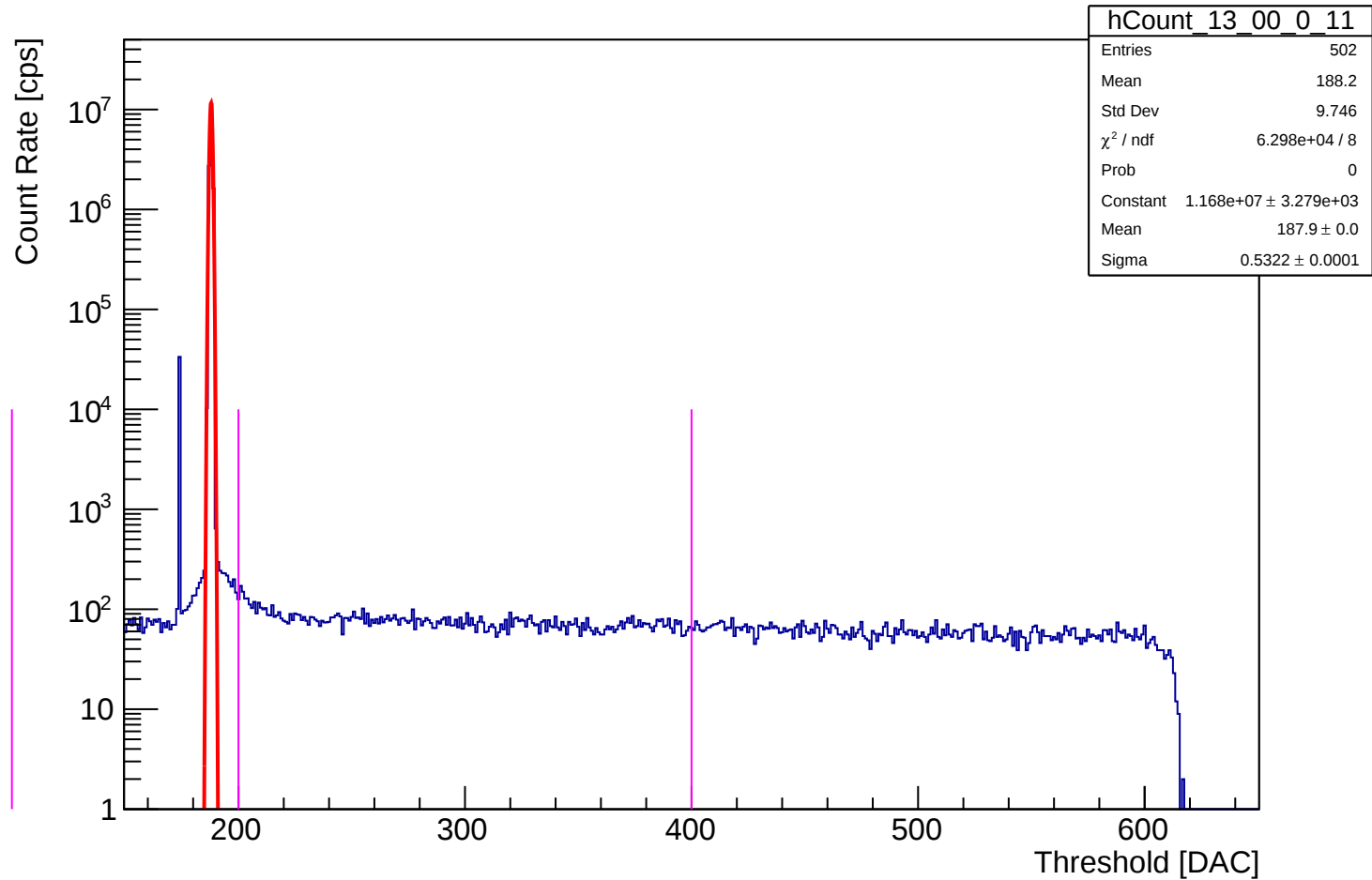
Count Rate [cps]

10⁷
10⁶
10⁵
10⁴
10³
10²
10
1



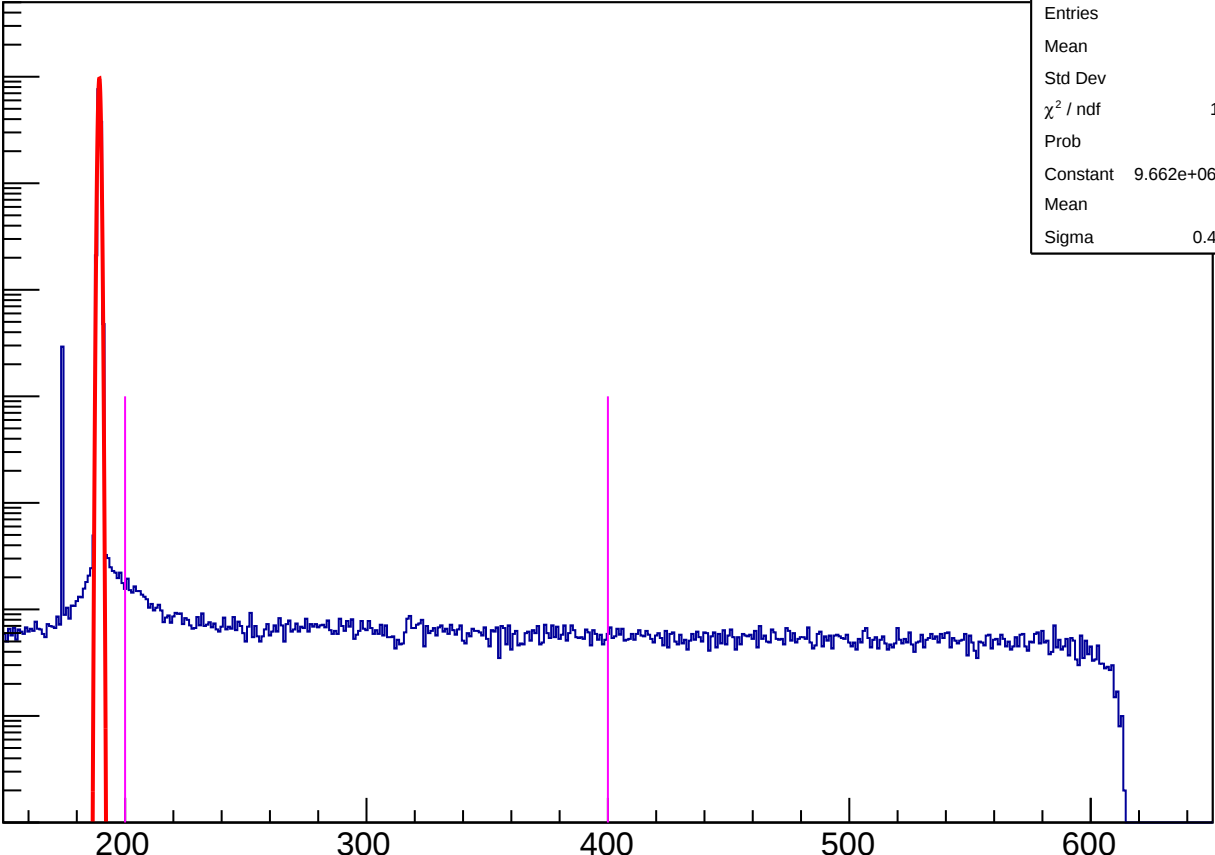
hCount_13_00_0_51	
Entries	502
Mean	189.9
Std Dev	11.61
χ^2 / ndf	1.059e+05 / 8
Prob	0
Constant	1.193e+07 $\pm$ 3.366e+03
Mean	189.4 $\pm$ 0.0
Sigma	0.6207 $\pm$ 0.0001

Threshold [DAC]



Count Rate [cps]

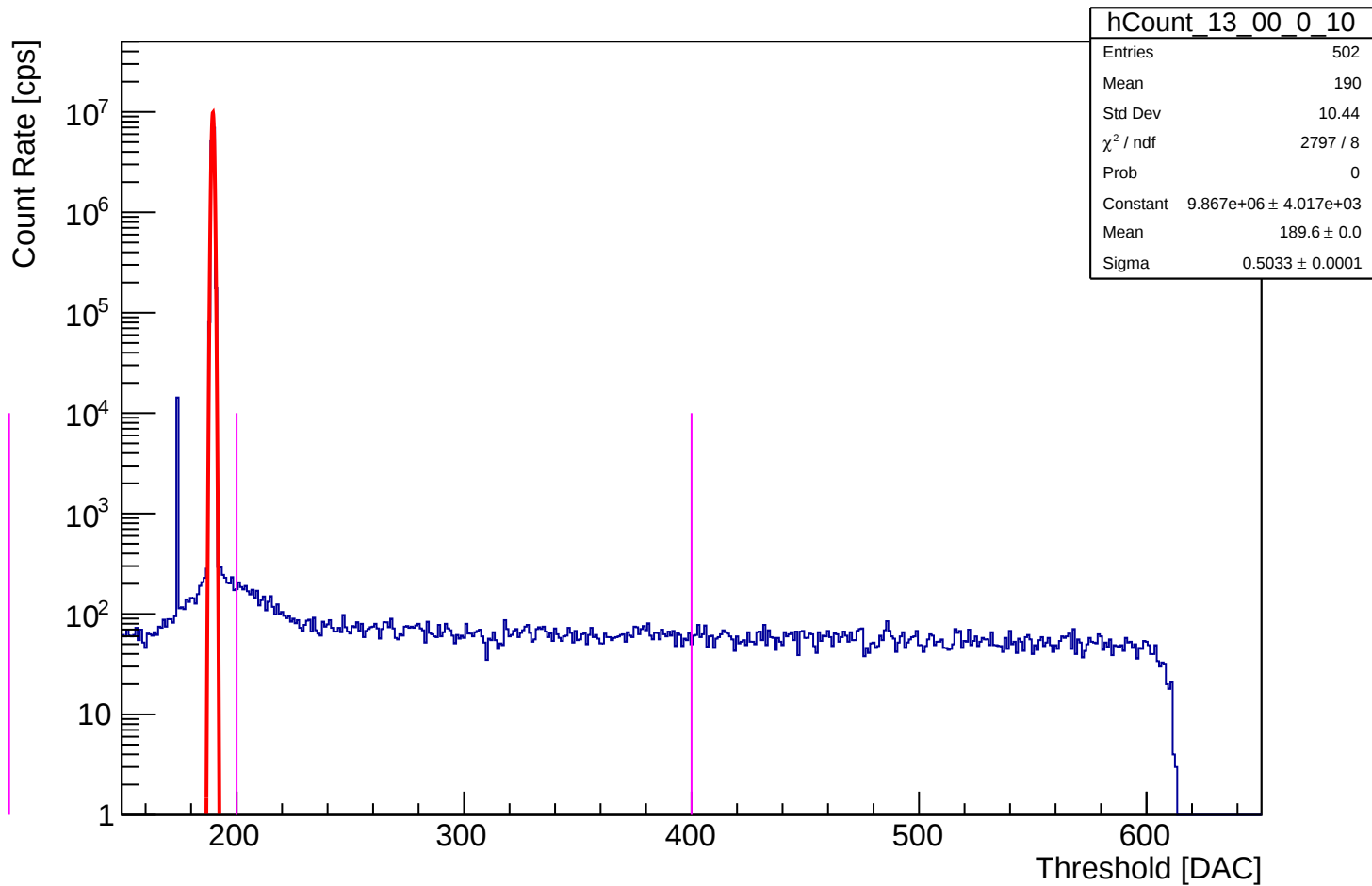
10⁷
10⁶
10⁵
10⁴
10³
10²
10
1

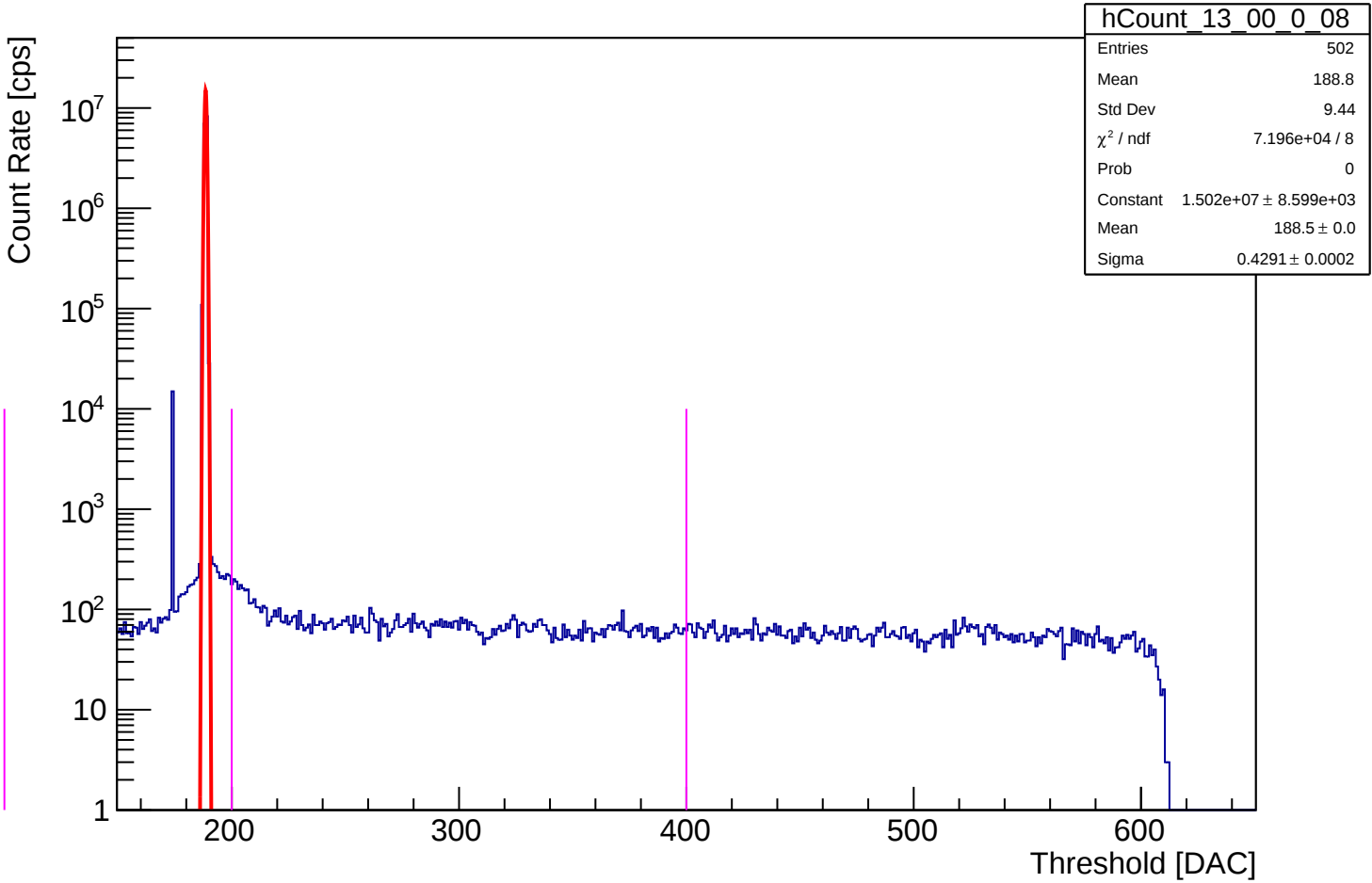


Threshold [DAC]

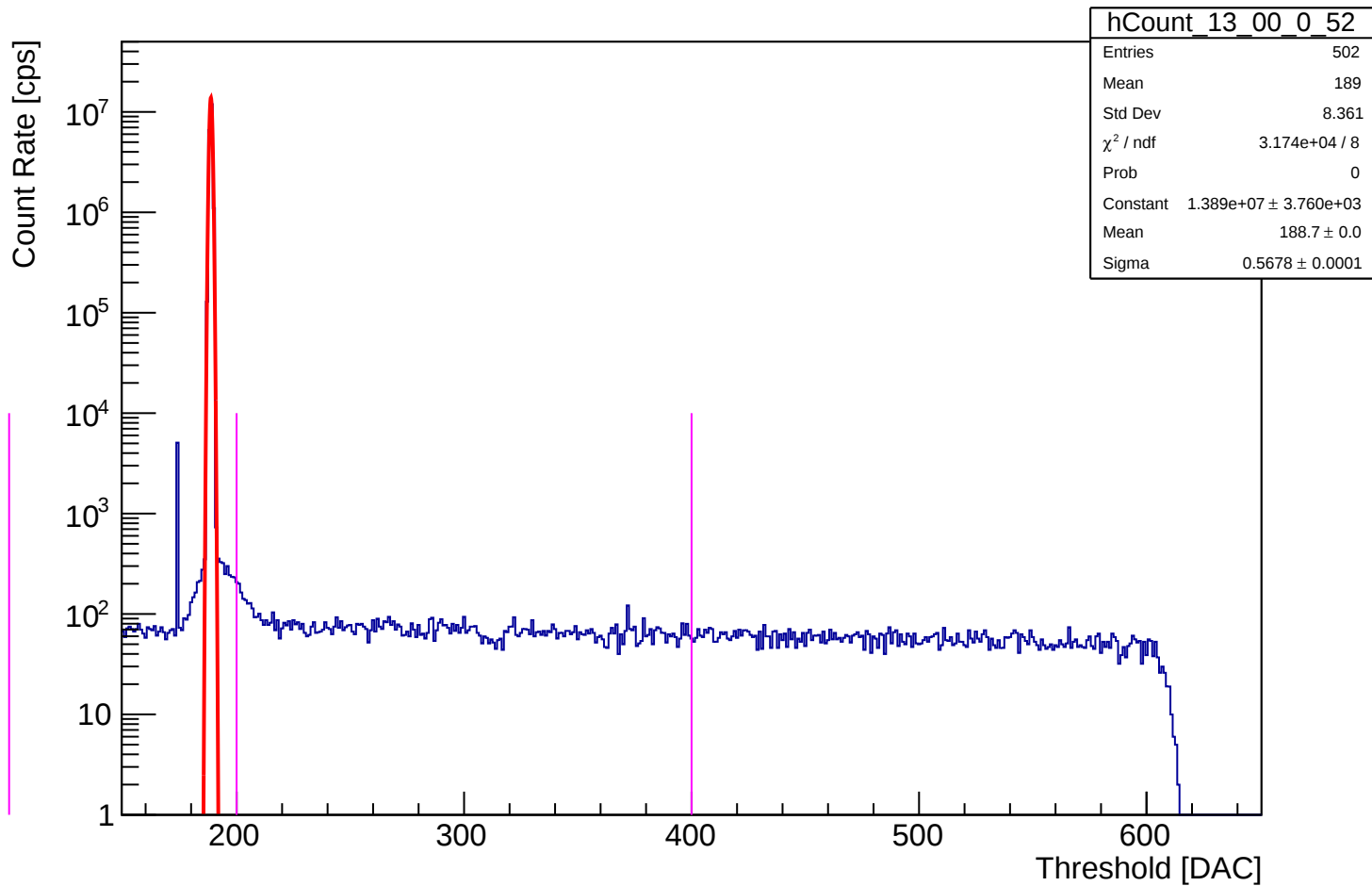
hCount_13_00_0_09	
Entries	502
Mean	189.7
Std Dev	10.48
χ^2 / ndf	1.125e+04 / 8
Prob	0
Constant	9.662e+06 $\pm$ 3.942e+03
Mean	189.3 $\pm$ 0.0
Sigma	0.4863 $\pm$ 0.0001

Row 1 Tile 1 Pmt 1 Pixel 43 Slot 13 Fiber 0 Asic 0 Channel 10

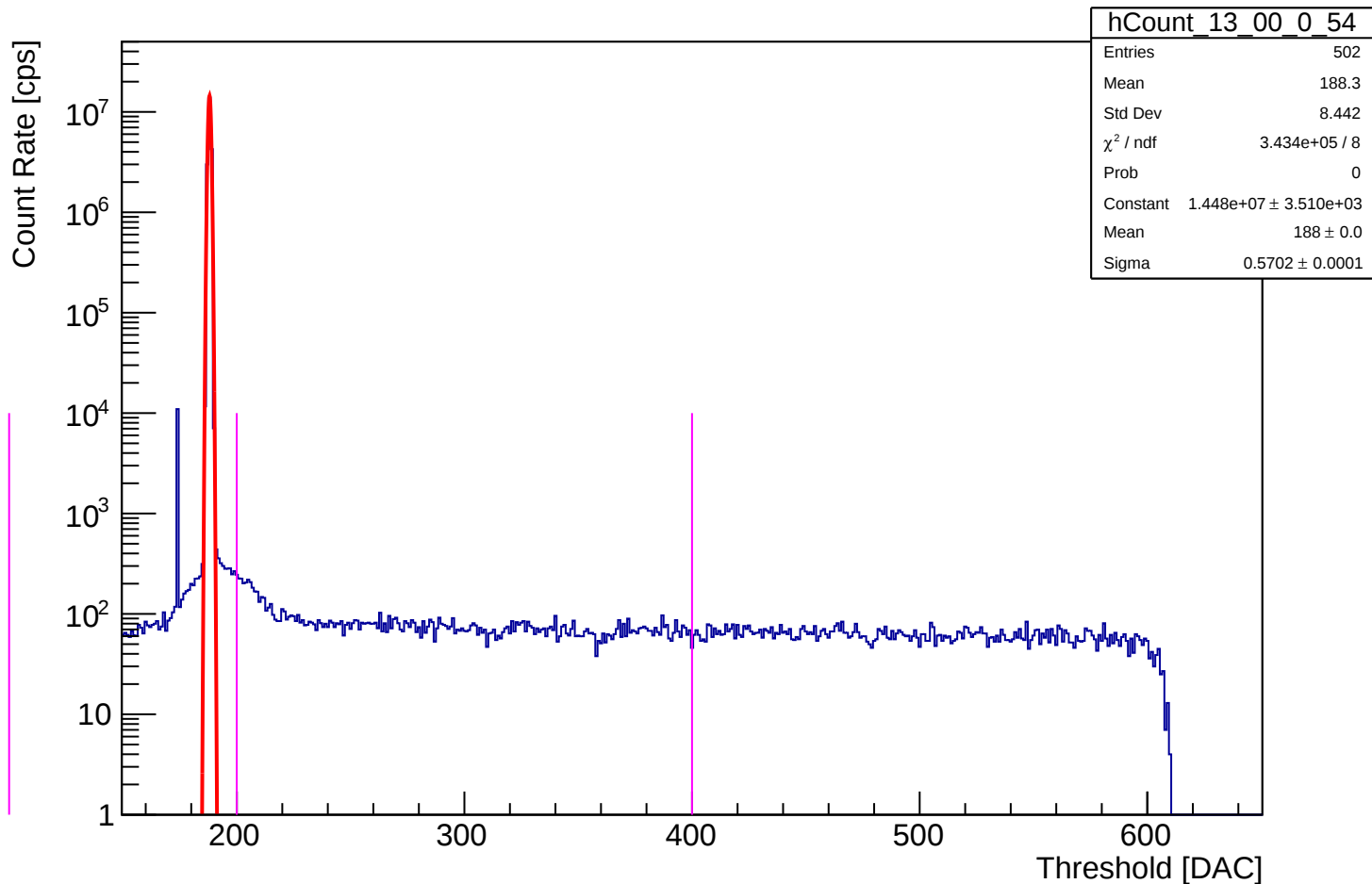




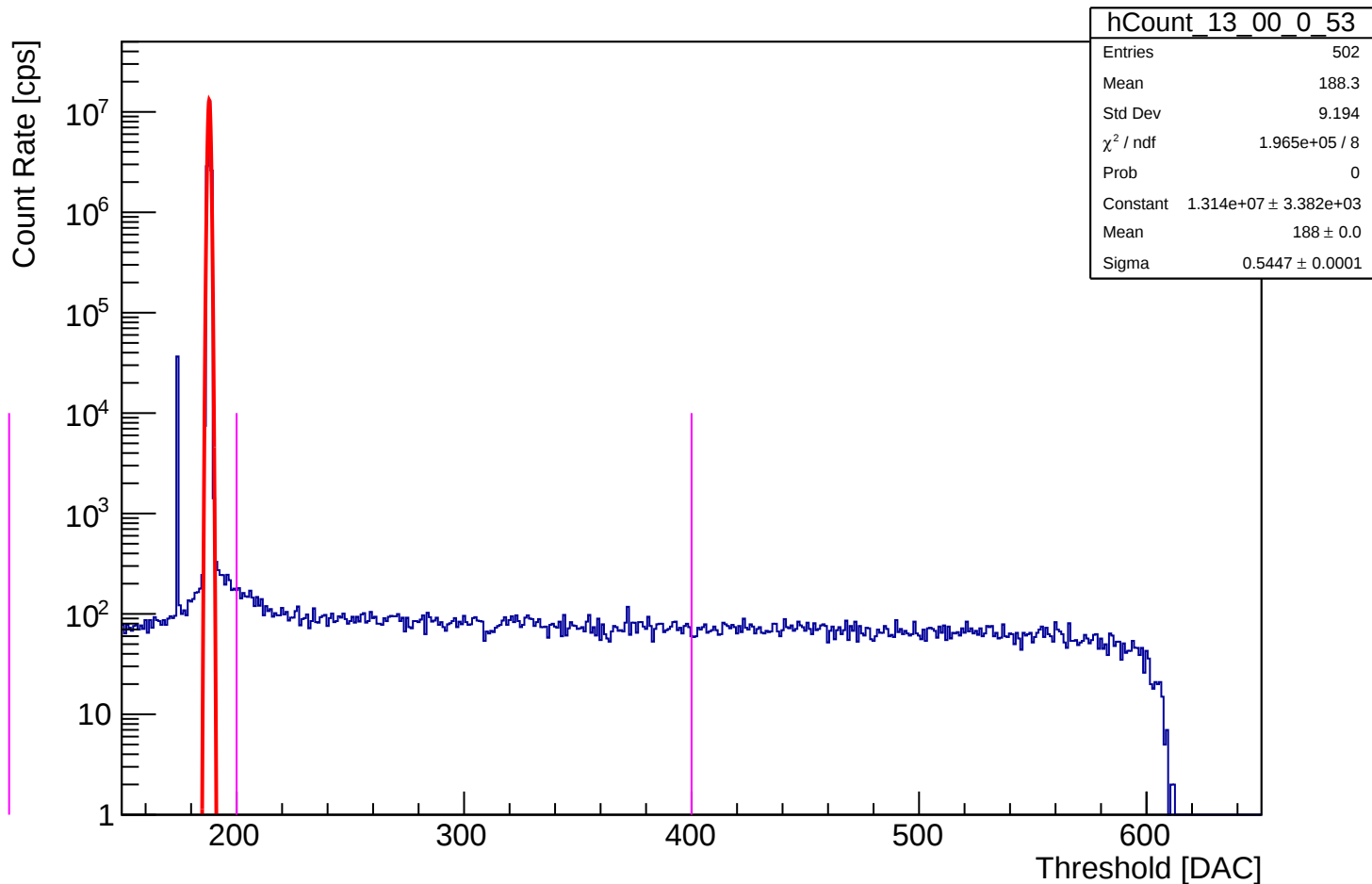
Row 1 Tile 1 Pmt 1 Pixel 45 Slot 13 Fiber 0 Asic 0 Channel 52



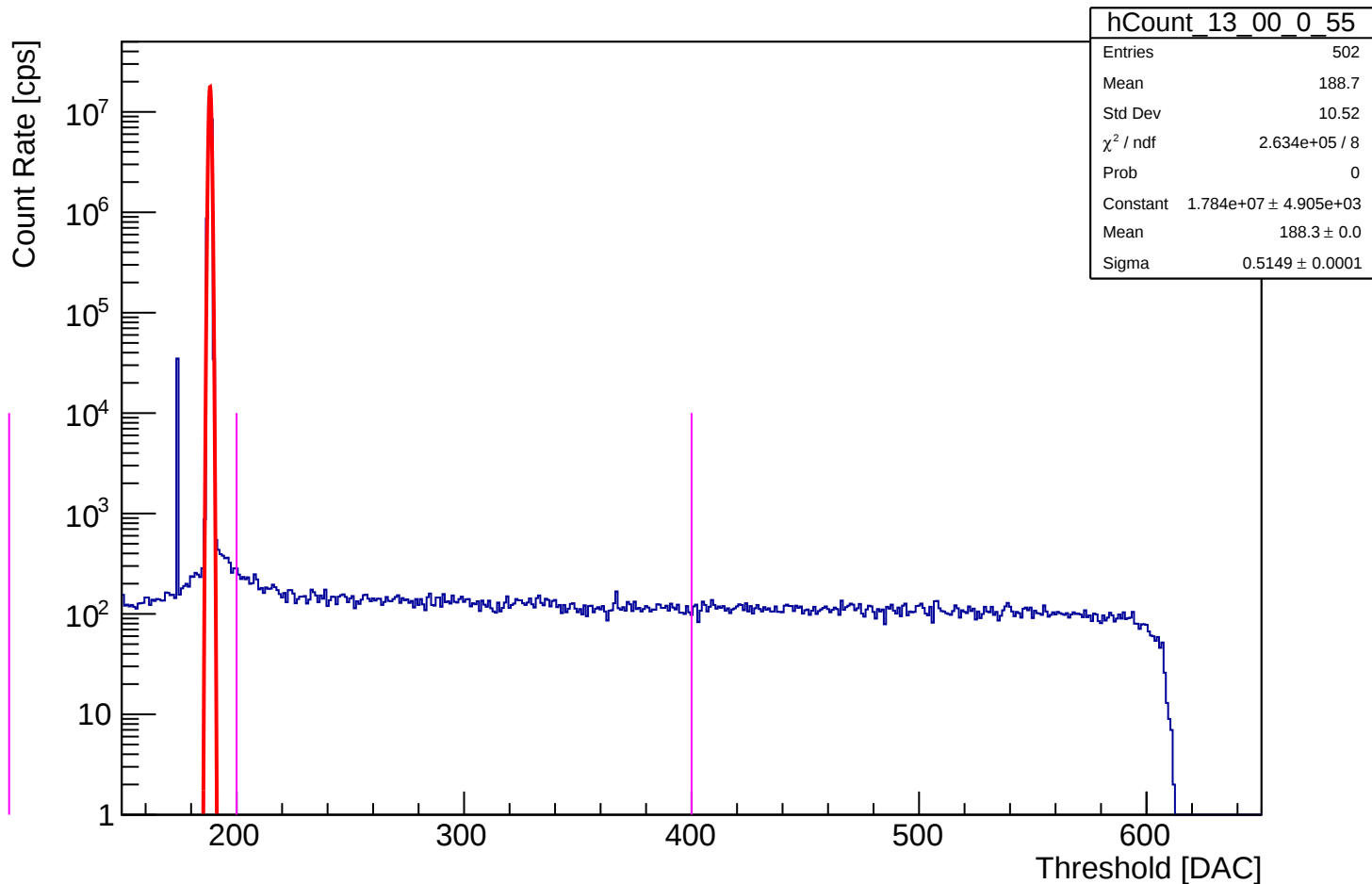
Row 1 Tile 1 Pmt 1 Pixel 46 Slot 13 Fiber 0 Asic 0 Channel 54

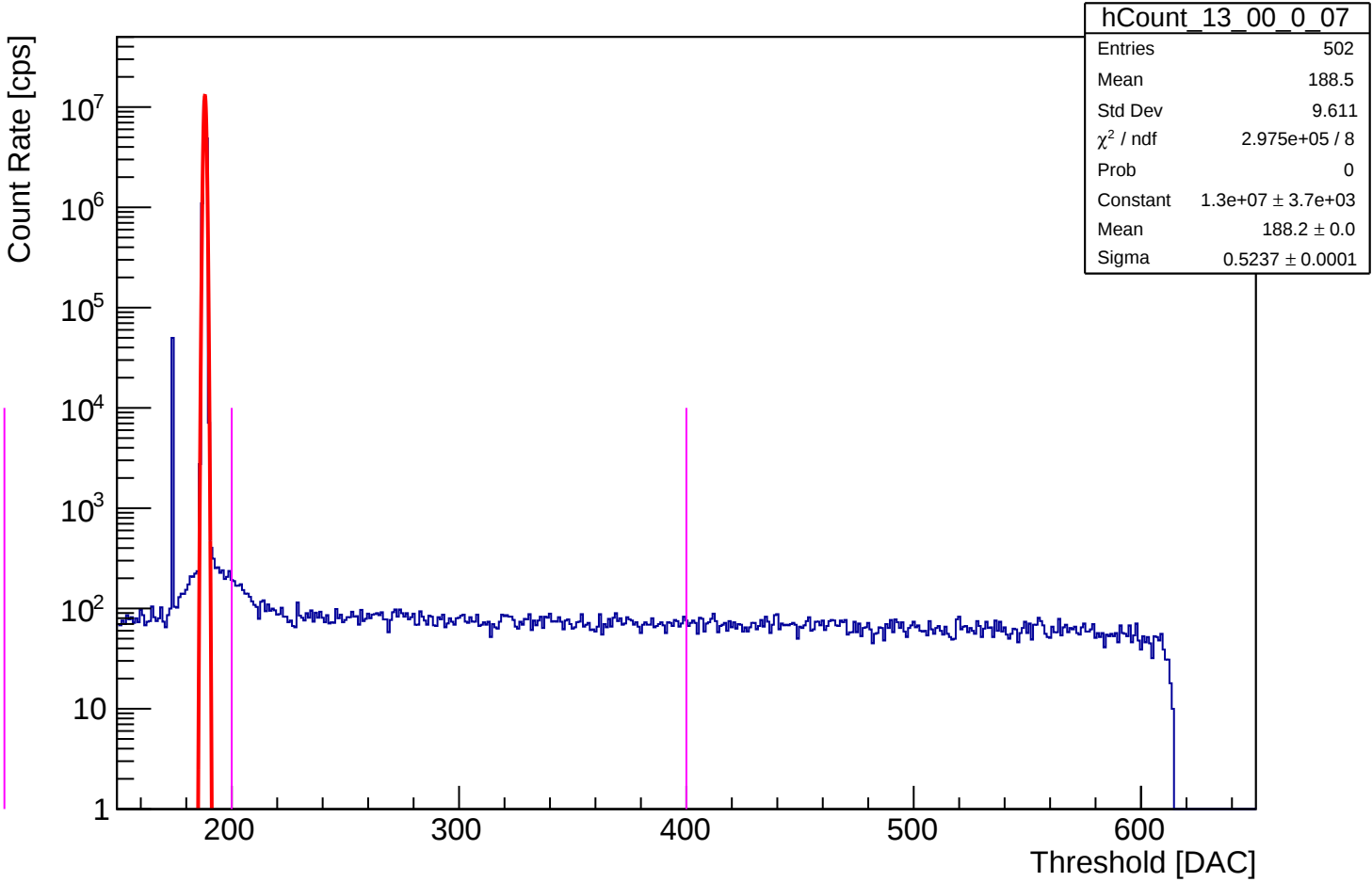


Row 1 Tile 1 Pmt 1 Pixel 47 Slot 13 Fiber 0 Asic 0 Channel 53



Row 1 Tile 1 Pmt 1 Pixel 48 Slot 13 Fiber 0 Asic 0 Channel 55





Count Rate [cps]

10⁷
10⁶
10⁵
10⁴
10³
10²
10
1

200

300

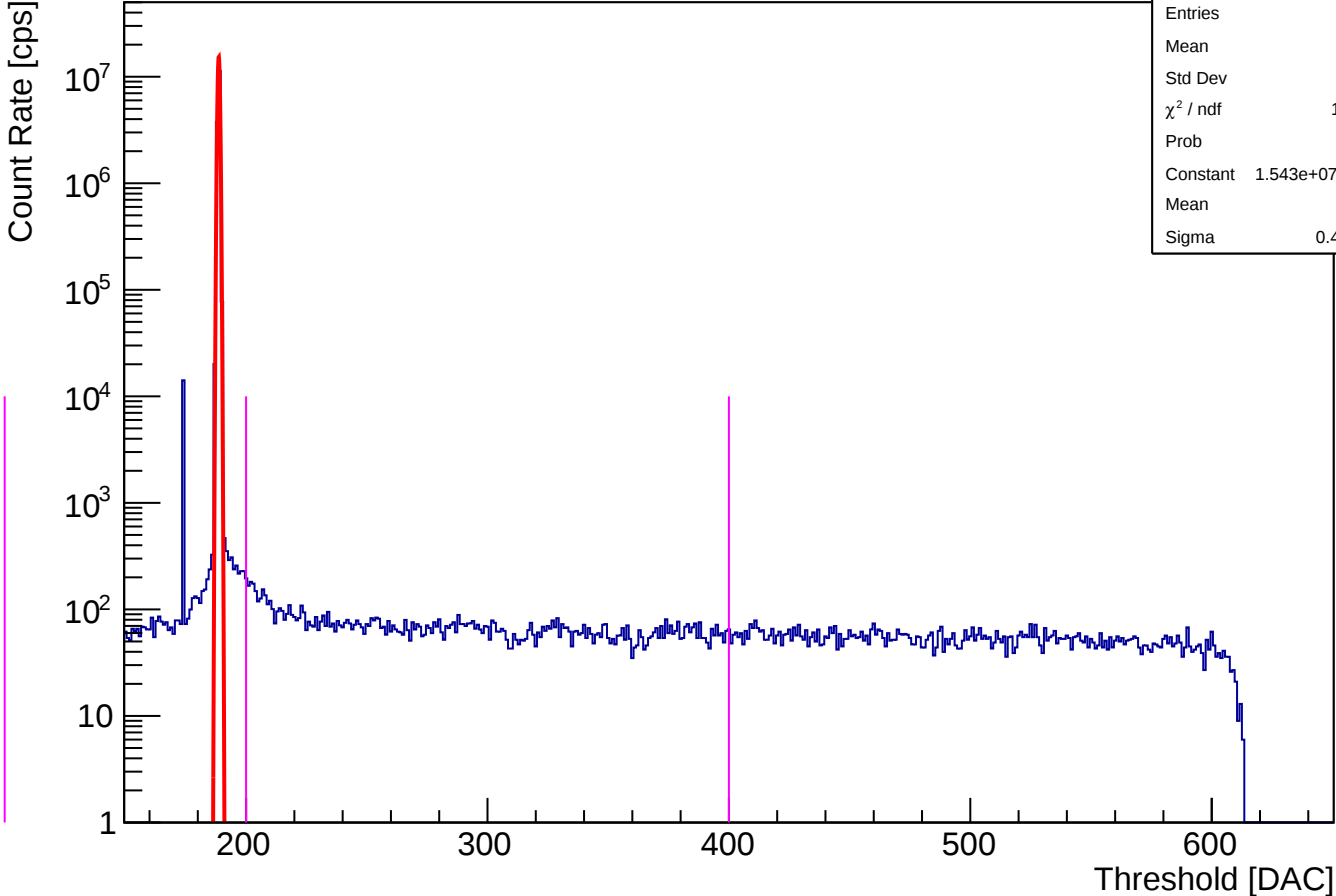
400

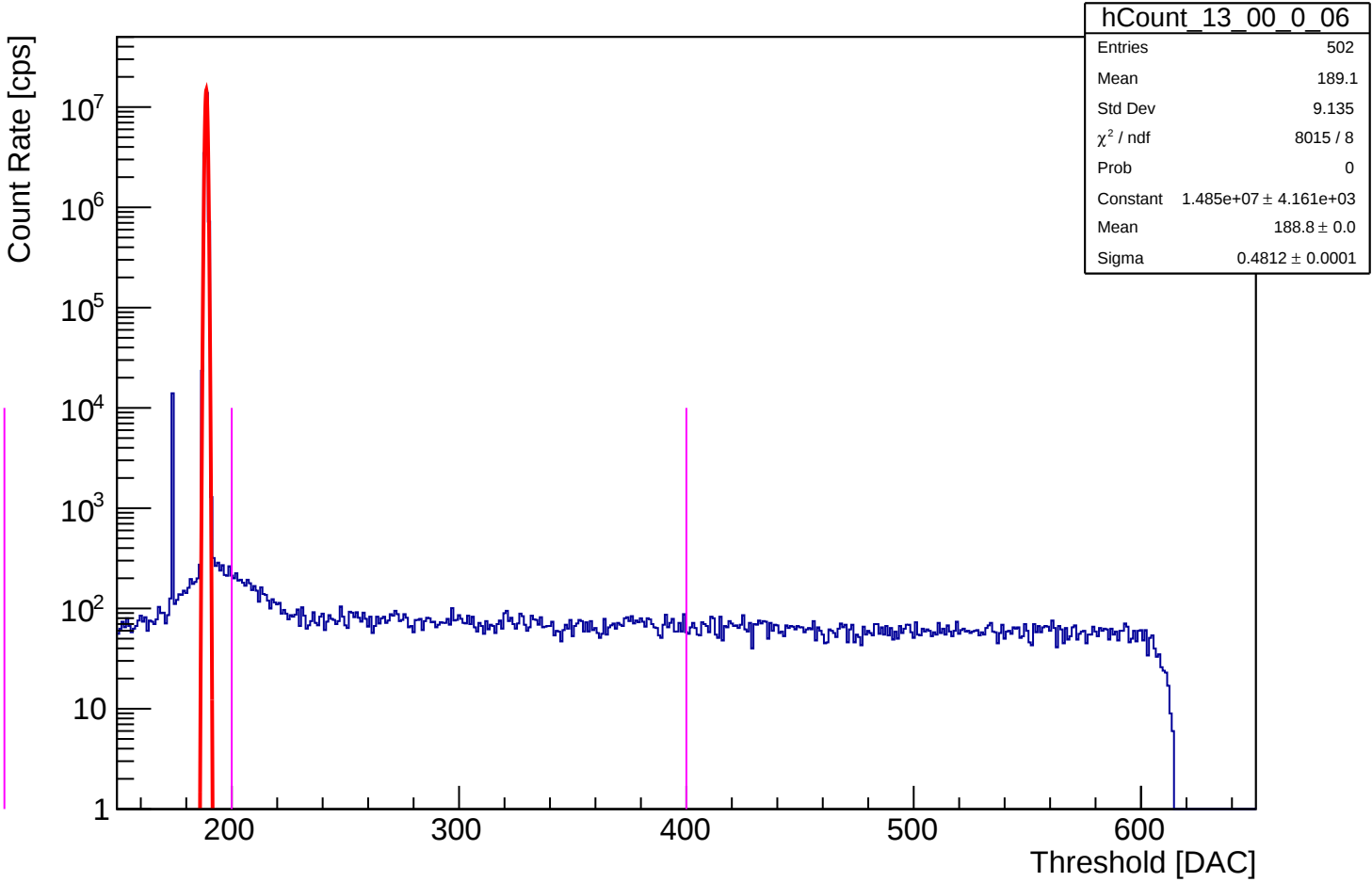
500

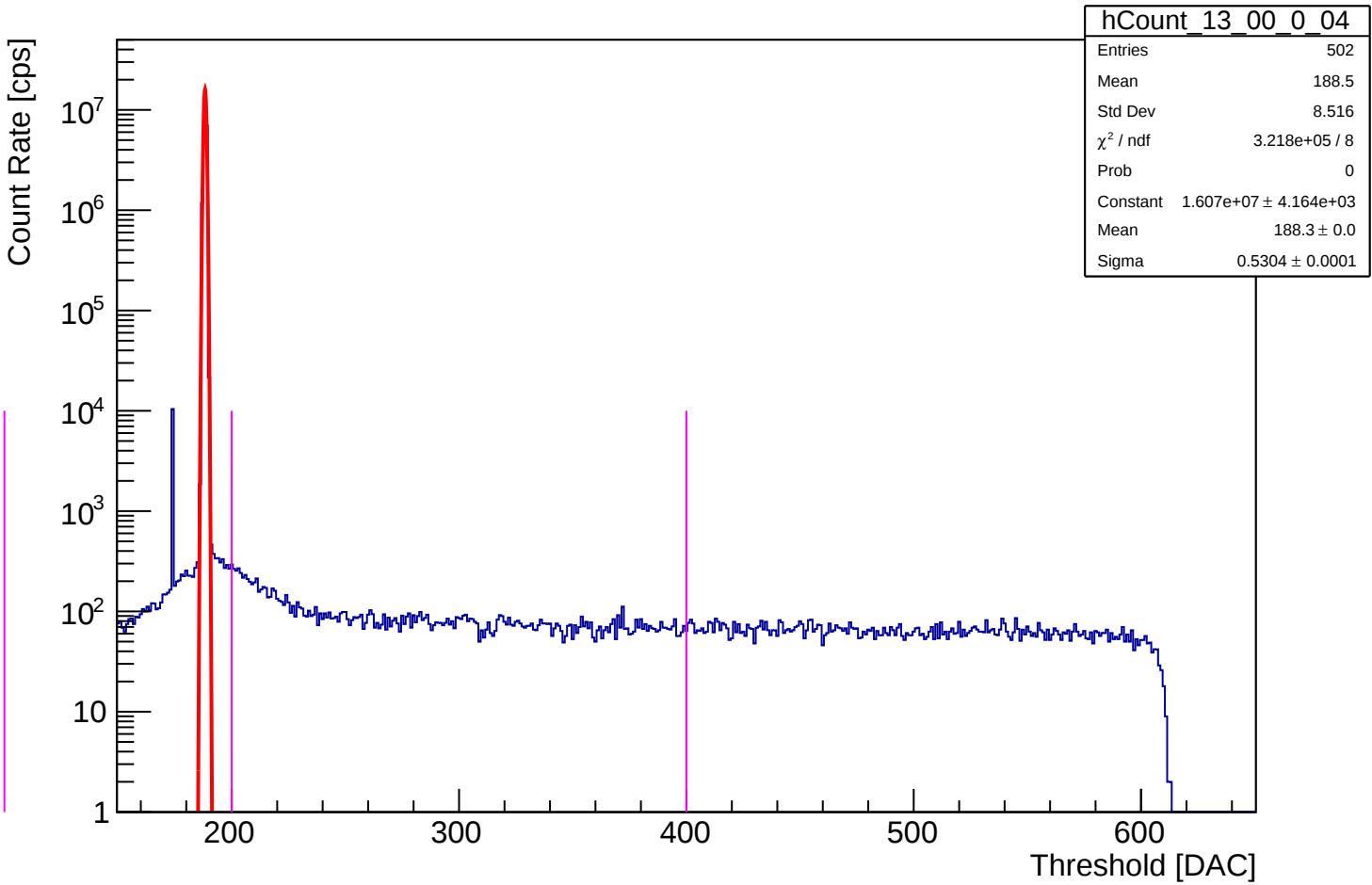
600

Threshold [DAC]

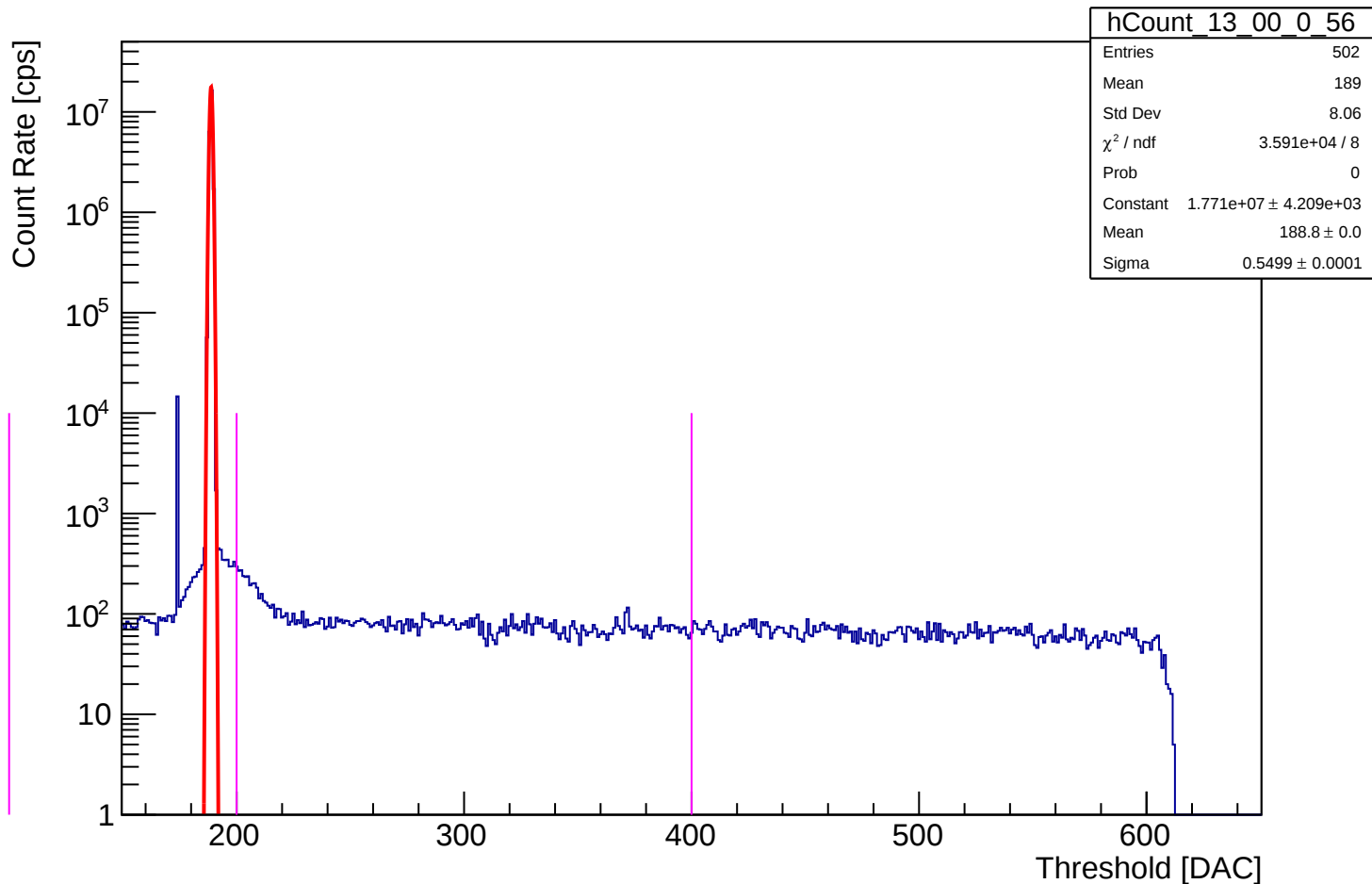
hCount_13_00_0_05	
Entries	502
Mean	189.1
Std Dev	9.277
χ^2 / ndf	1.698e+04 / 8
Prob	0
Constant	1.543e+07 $\pm$ 7.340e+03
Mean	188.7 $\pm$ 0.0
Sigma	0.4061 $\pm$ 0.0001



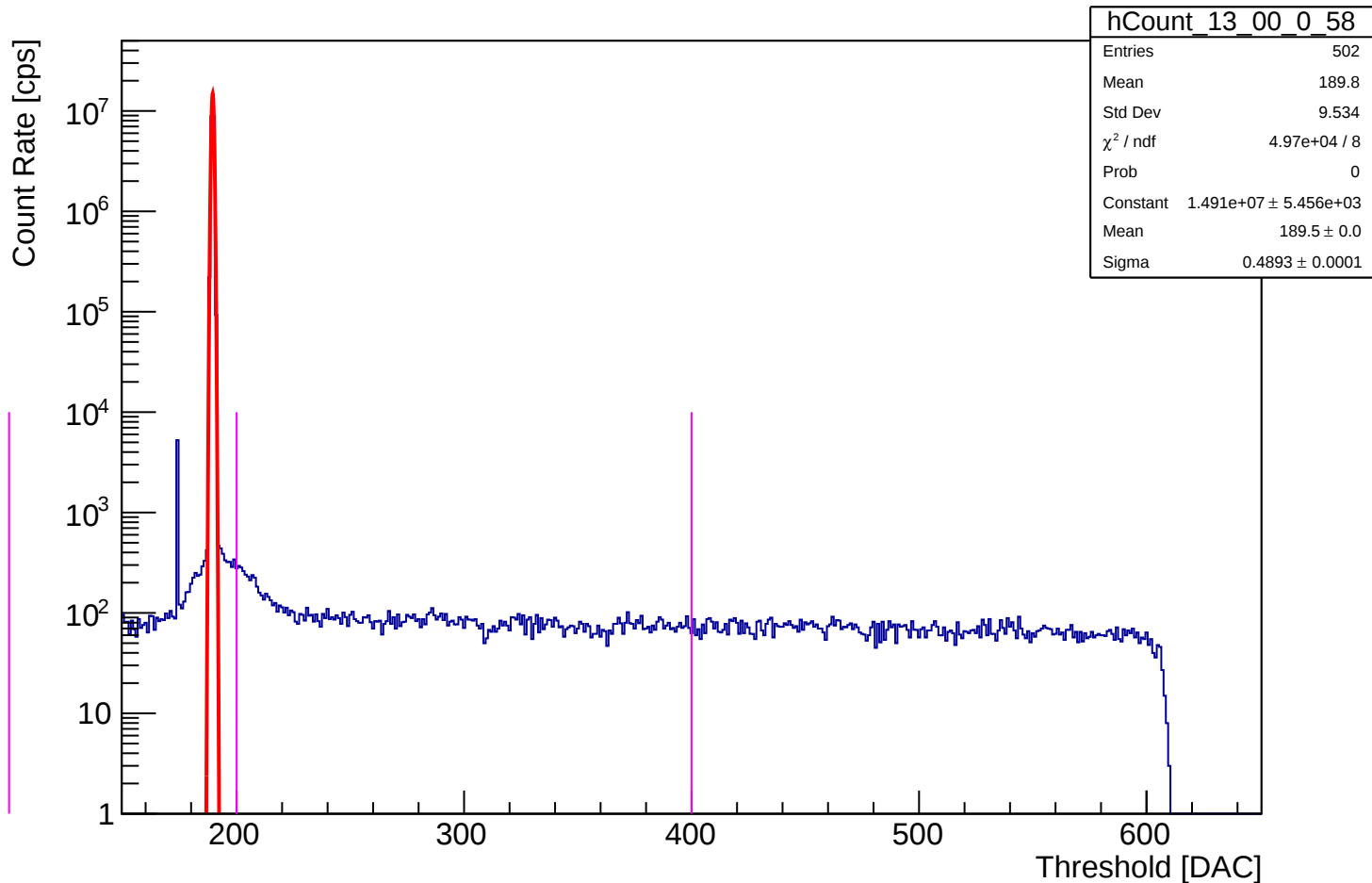




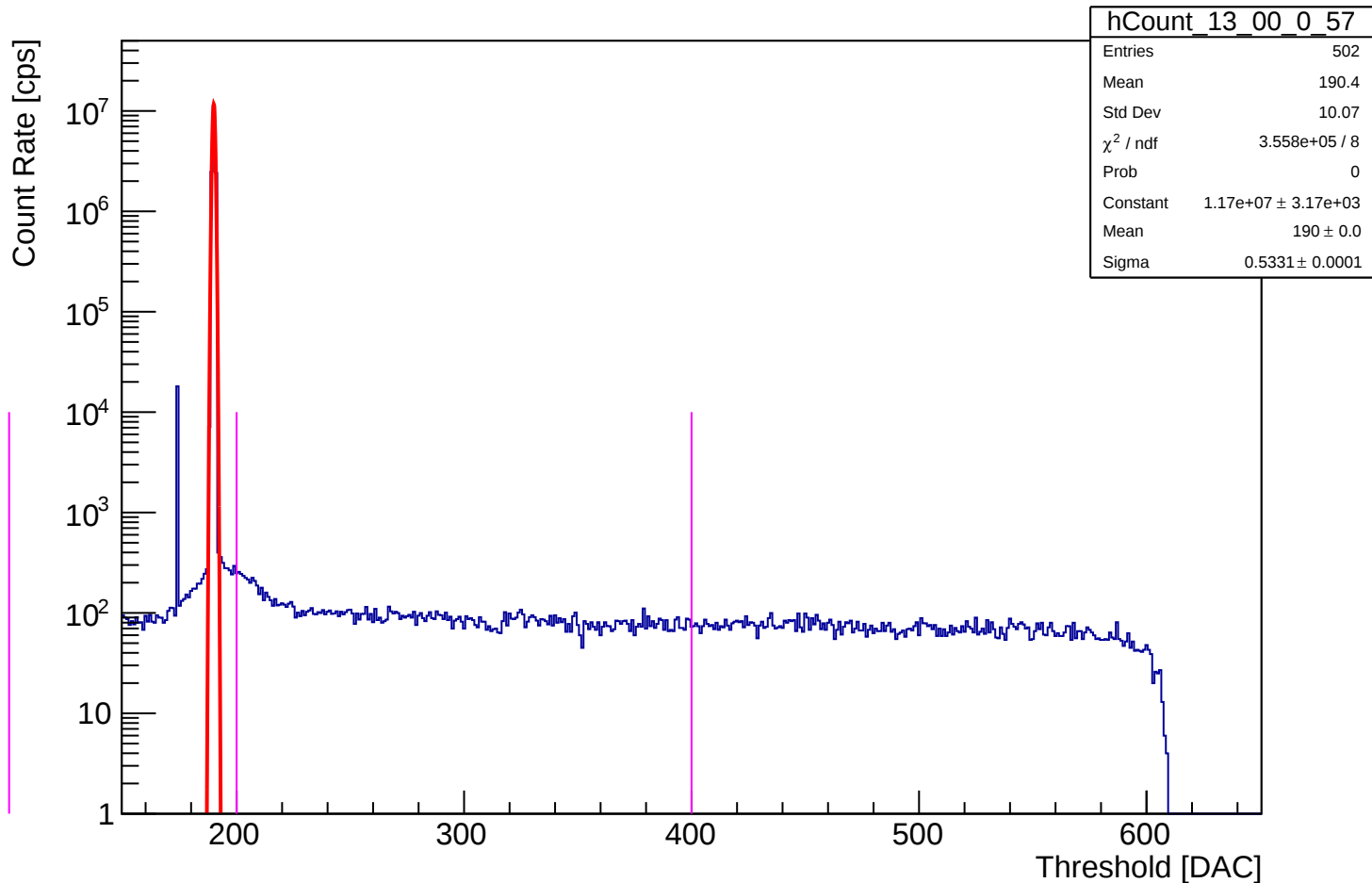
Row 1 Tile 1 Pmt 1 Pixel 53 Slot 13 Fiber 0 Asic 0 Channel 56



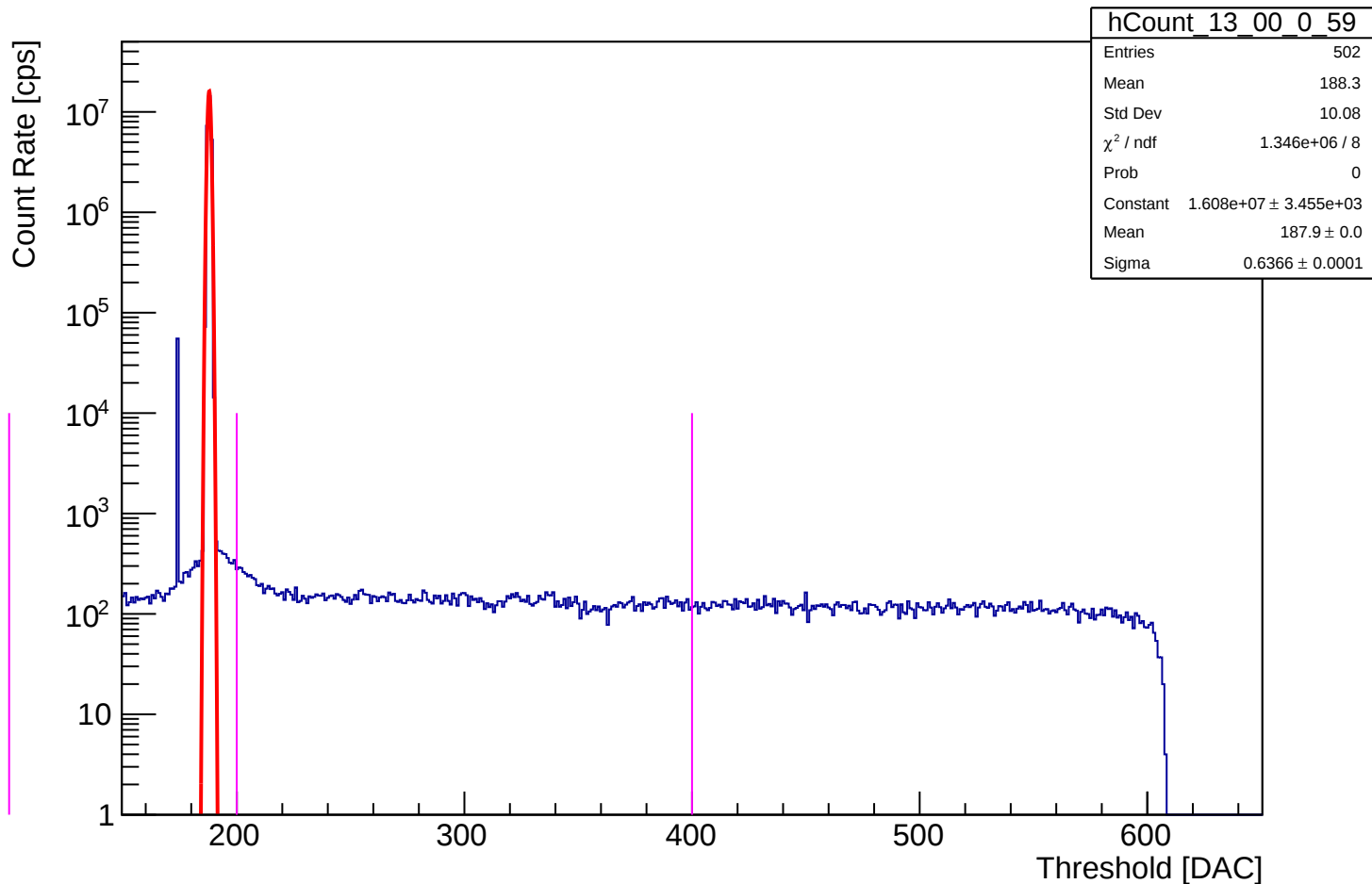
Row 1 Tile 1 Pmt 1 Pixel 54 Slot 13 Fiber 0 Asic 0 Channel 58

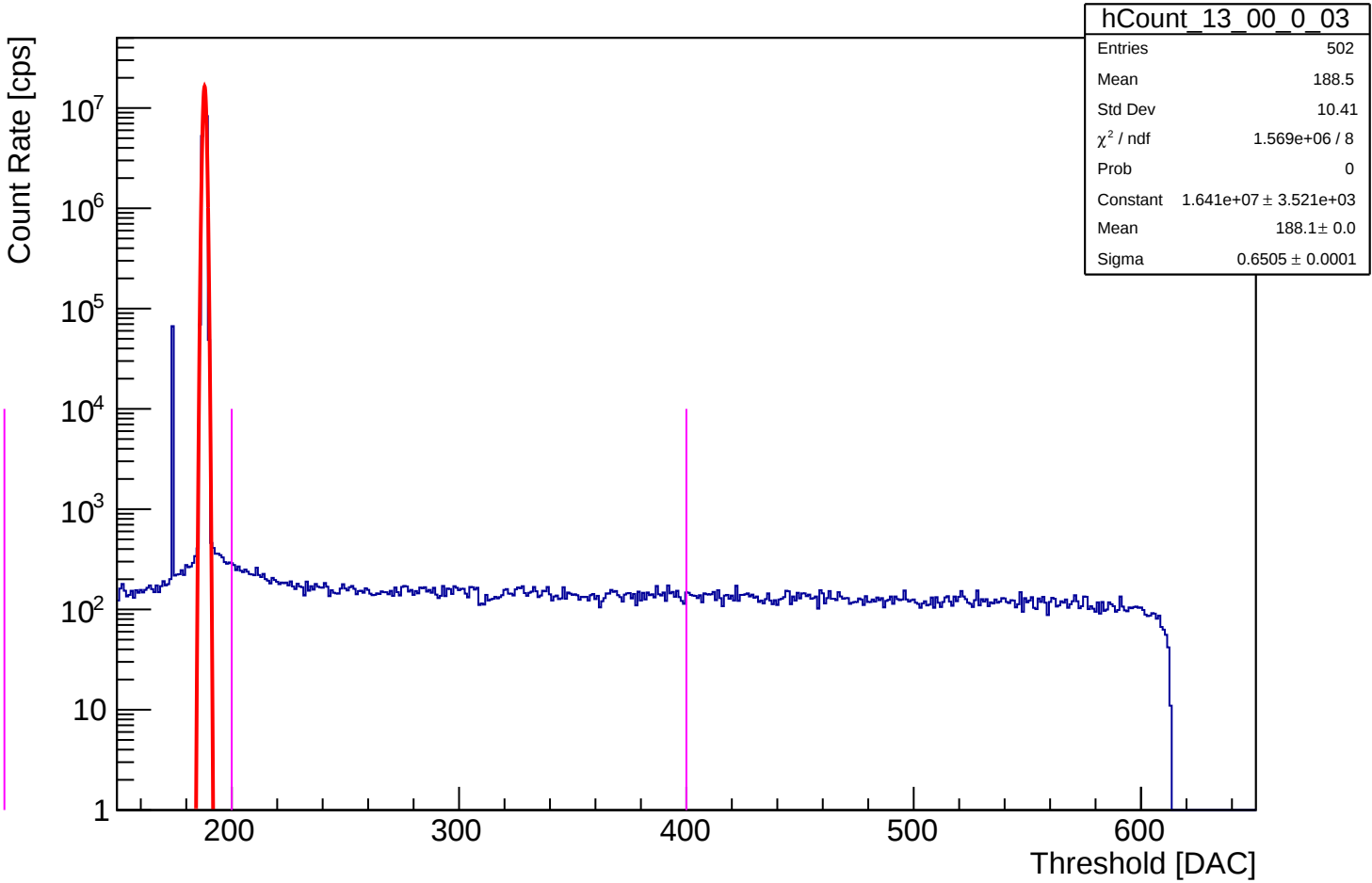


Row 1 Tile 1 Pmt 1 Pixel 55 Slot 13 Fiber 0 Asic 0 Channel 57

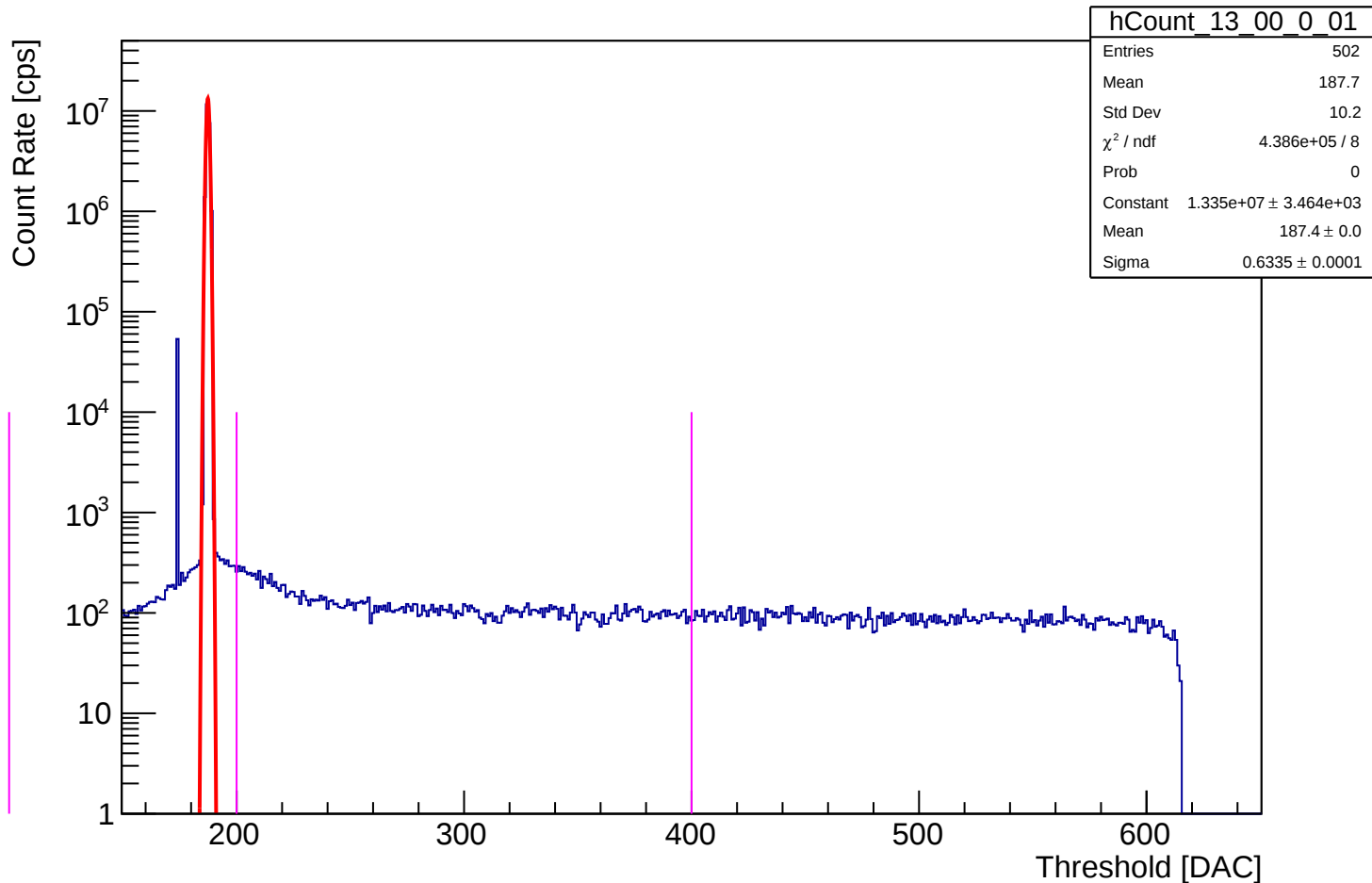


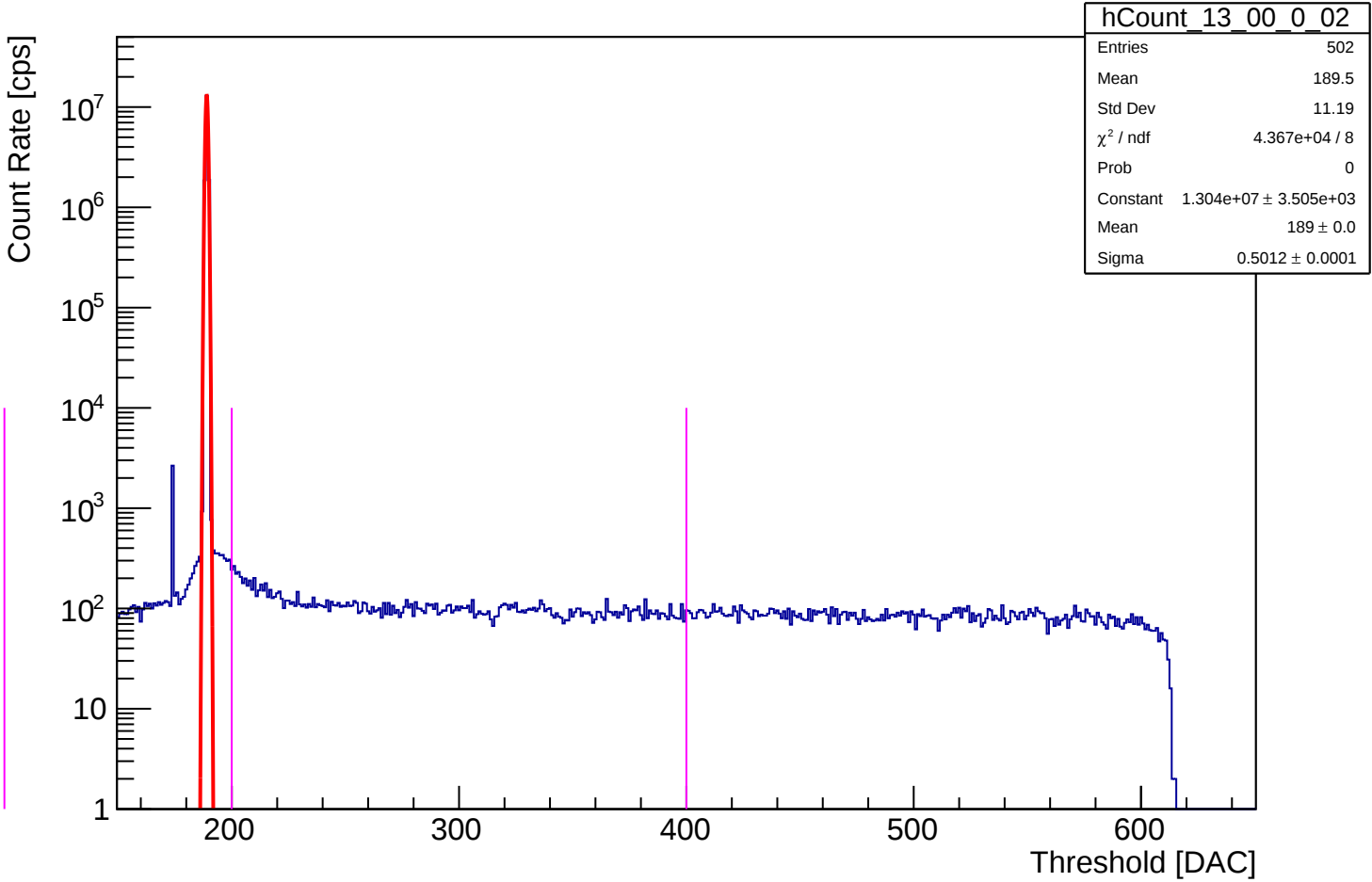
Row 1 Tile 1 Pmt 1 Pixel 56 Slot 13 Fiber 0 Asic 0 Channel 59

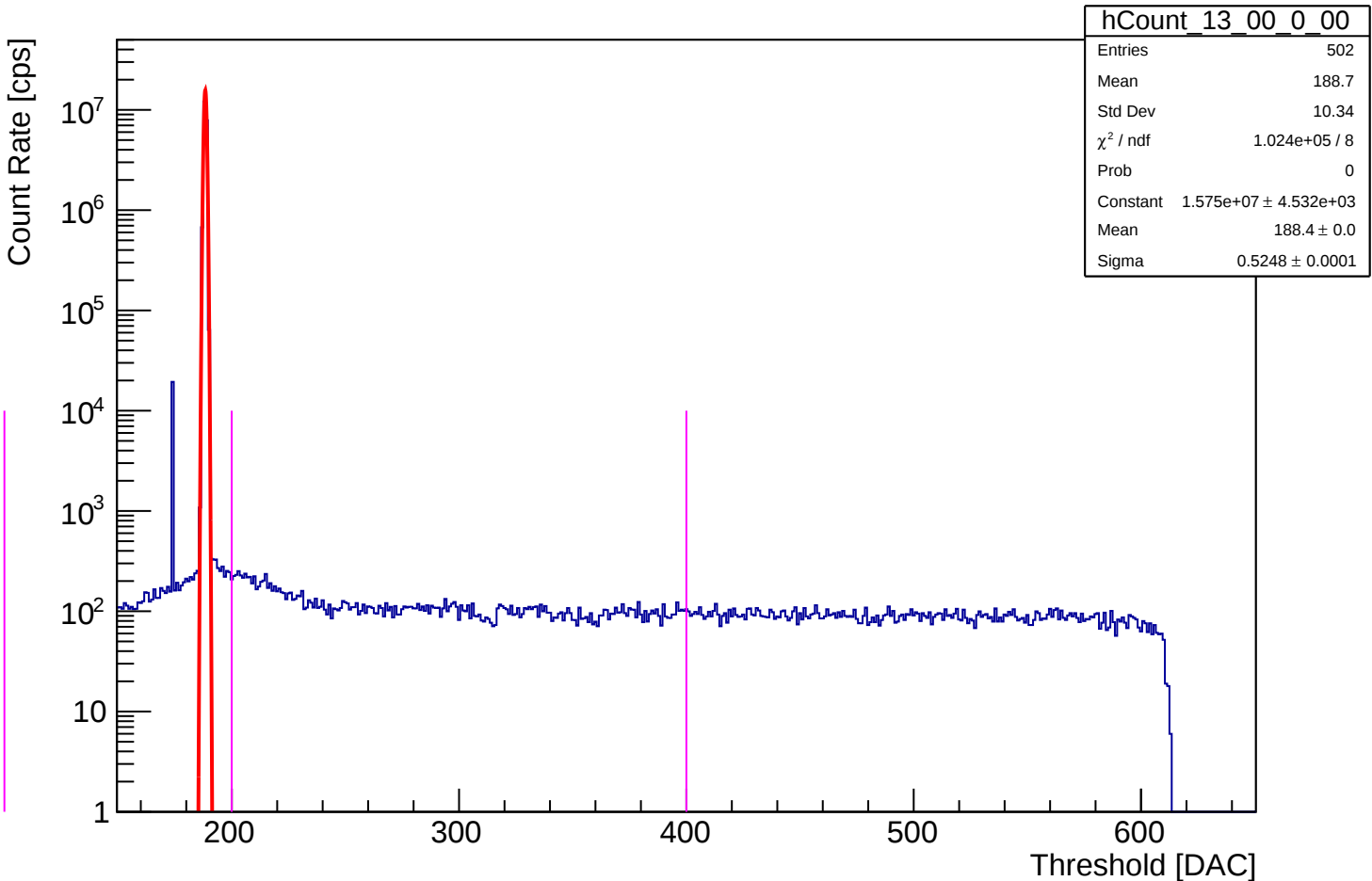




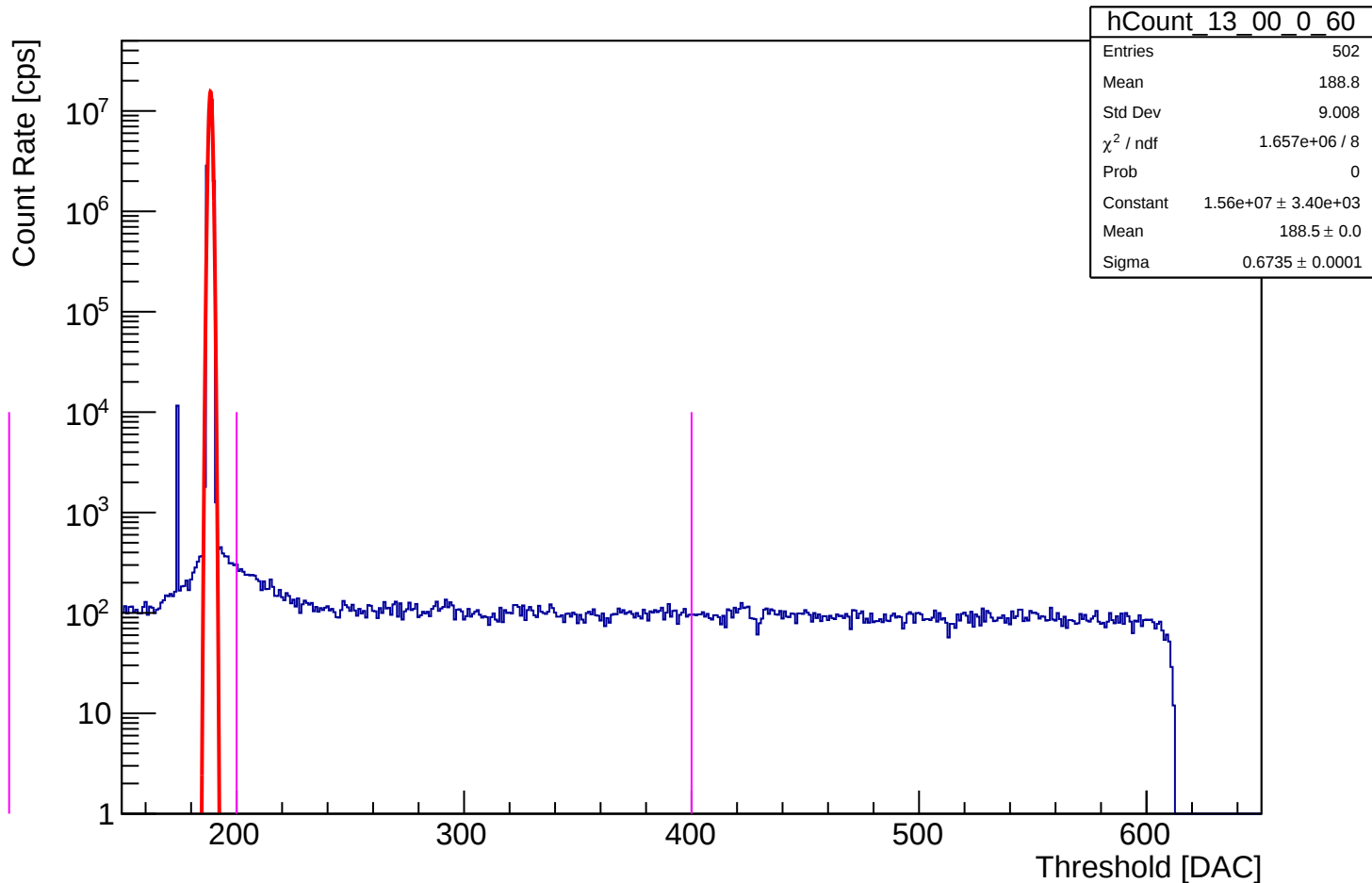
Row 1 Tile 1 Pmt 1 Pixel 58 Slot 13 Fiber 0 Asic 0 Channel 1



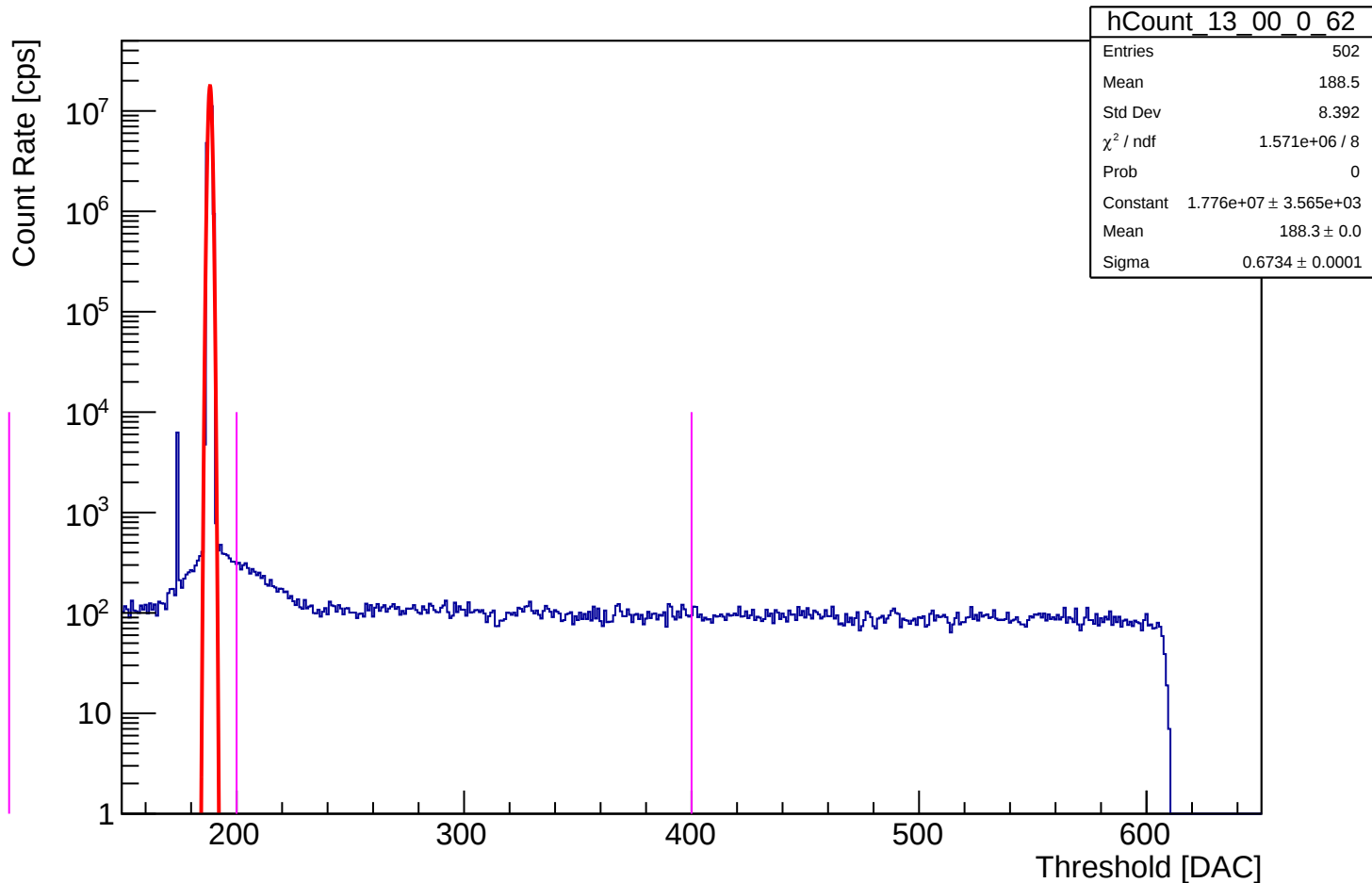




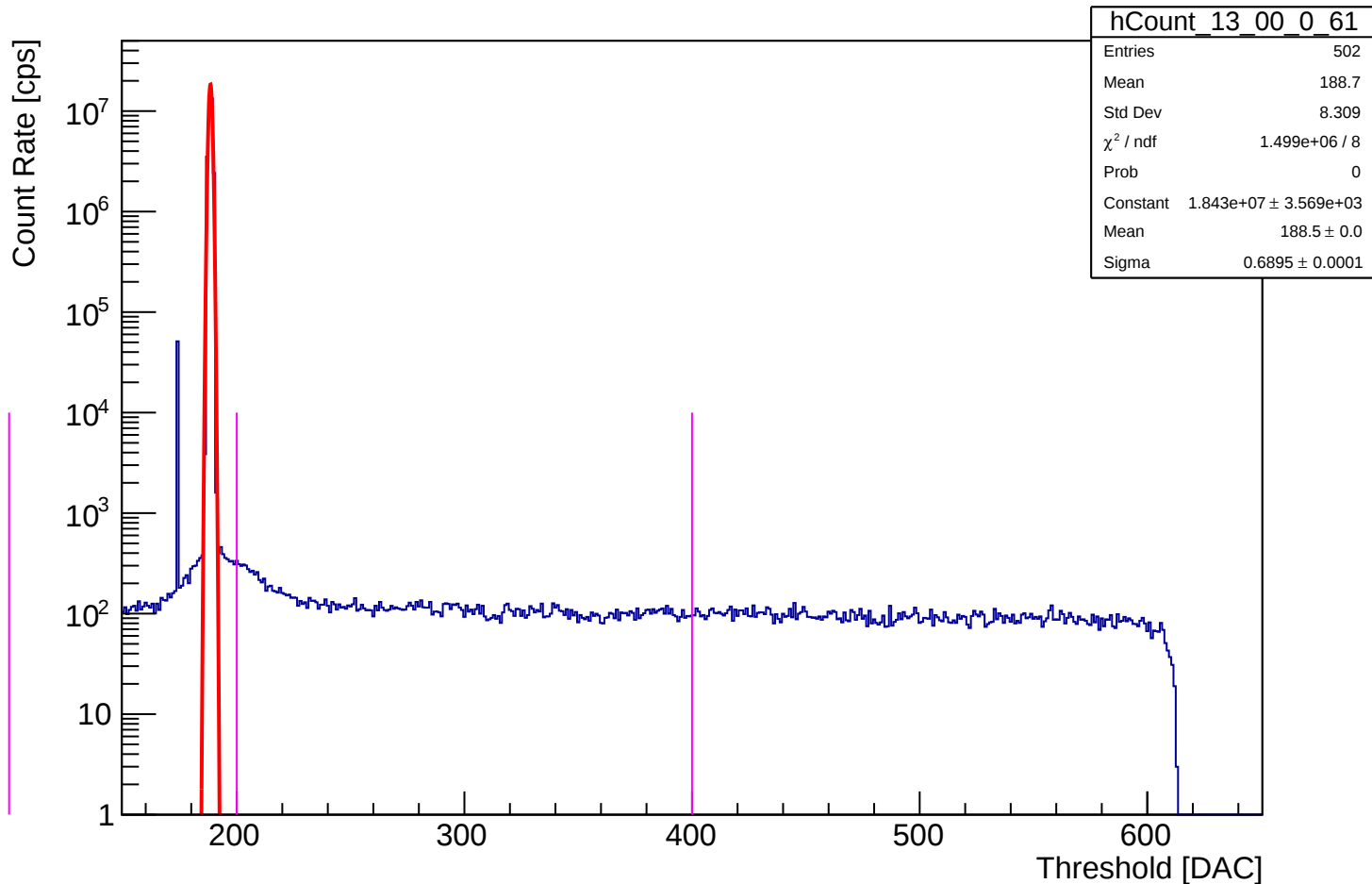
Row 1 Tile 1 Pmt 1 Pixel 61 Slot 13 Fiber 0 Asic 0 Channel 60



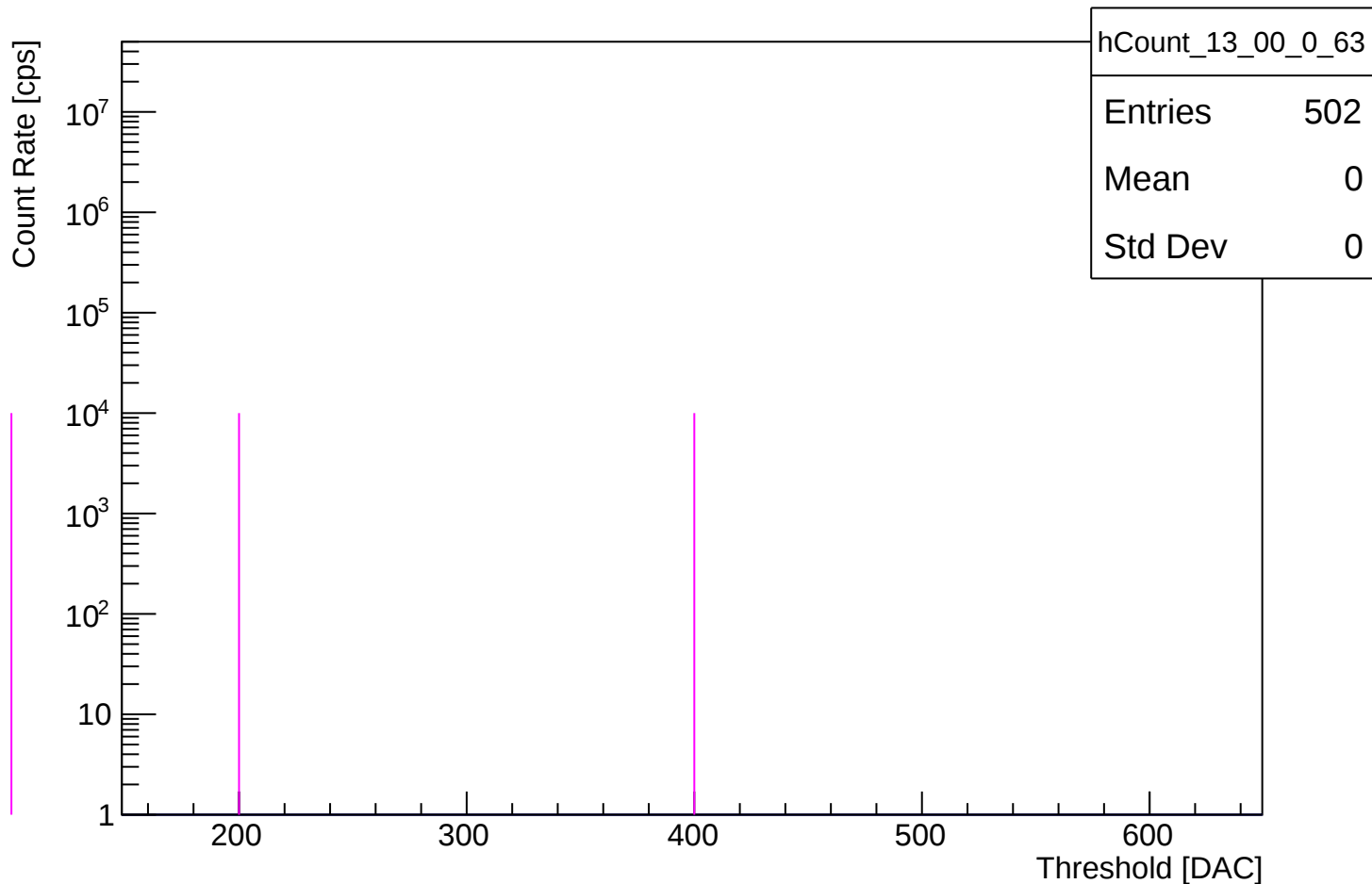
Row 1 Tile 1 Pmt 1 Pixel 62 Slot 13 Fiber 0 Asic 0 Channel 62



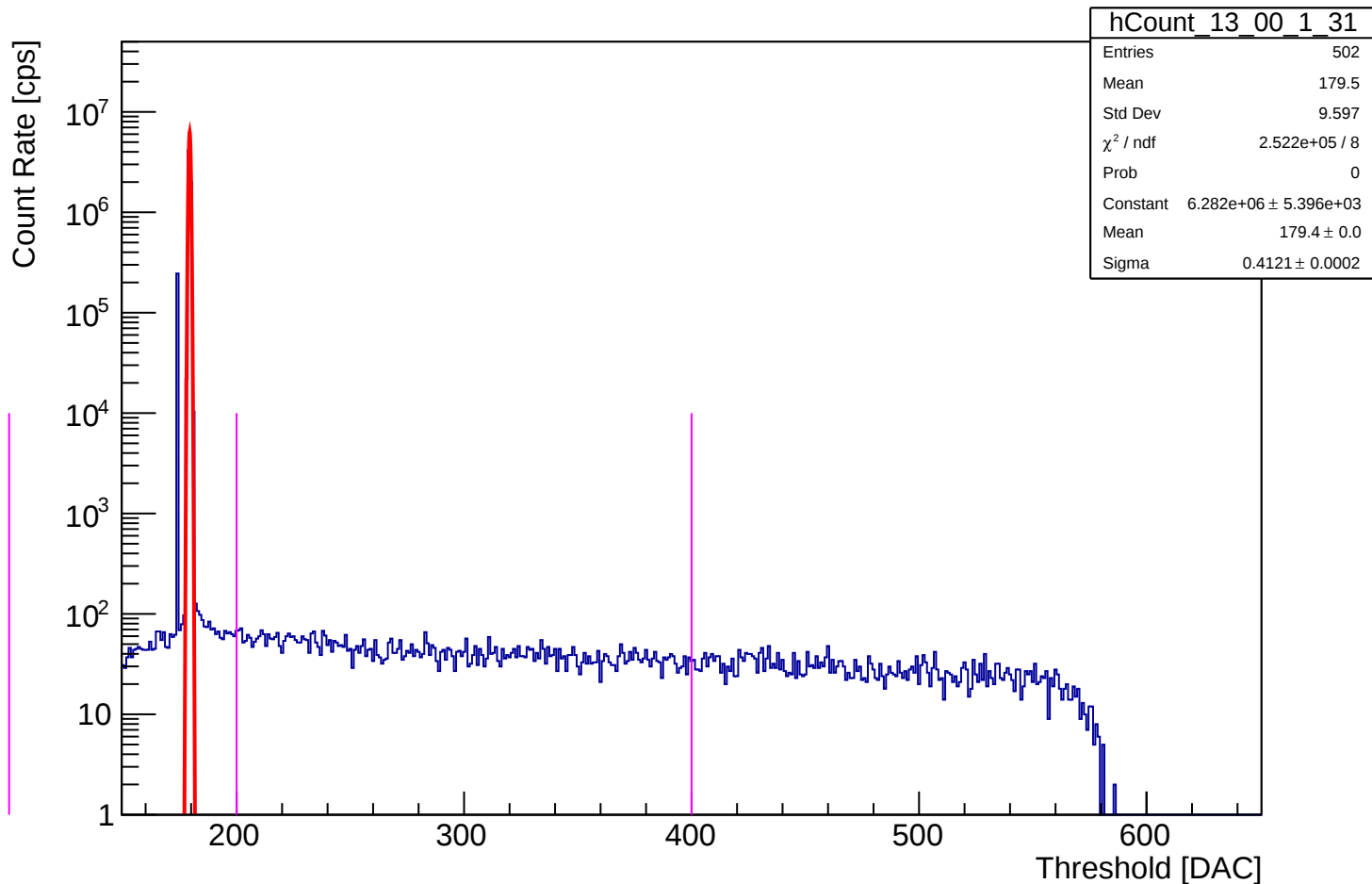
Row 1 Tile 1 Pmt 1 Pixel 63 Slot 13 Fiber 0 Asic 0 Channel 61



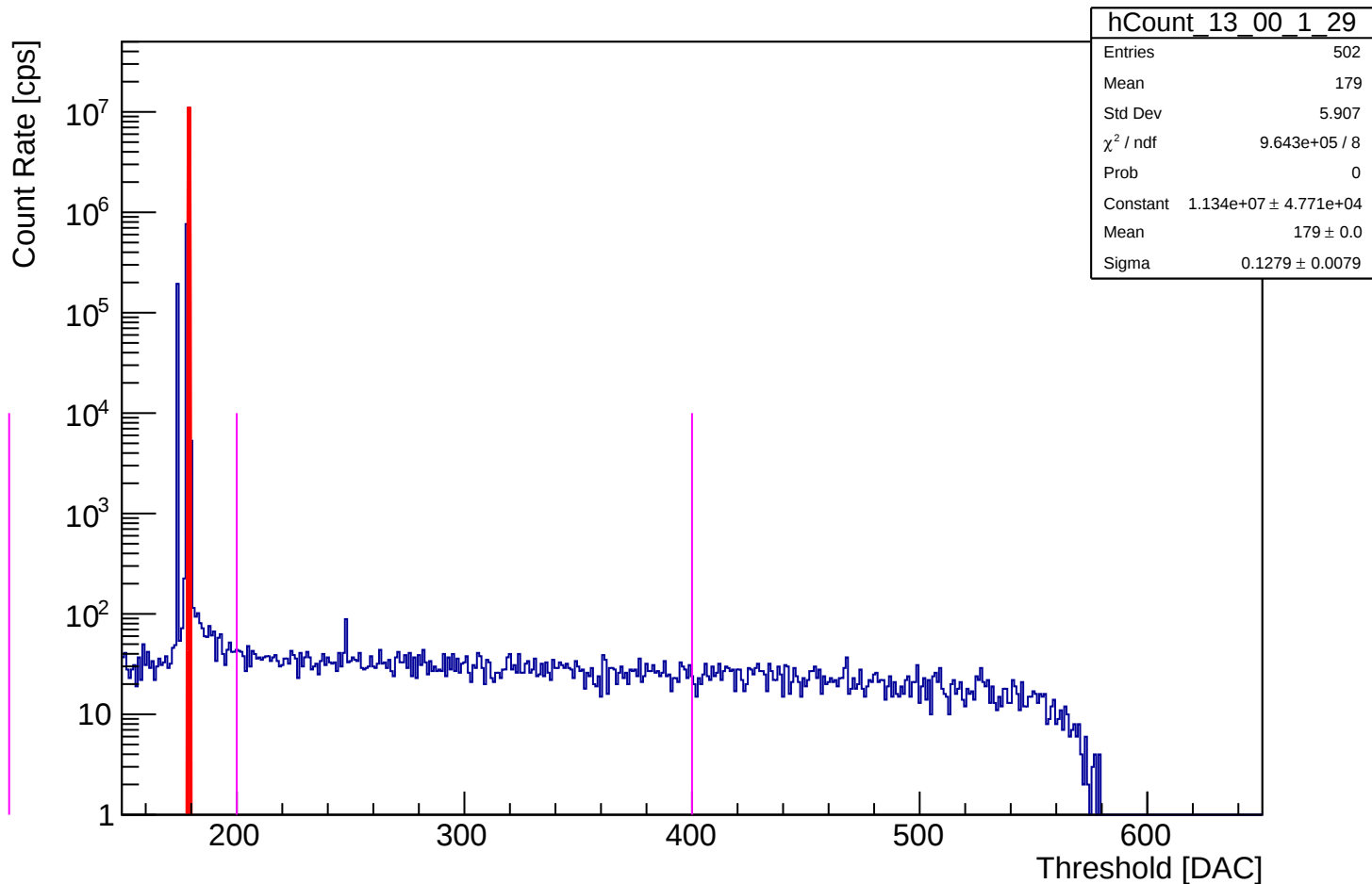
Row 1 Tile 1 Pmt 1 Pixel 64 Slot 13 Fiber 0 Asic 0 Channel 63



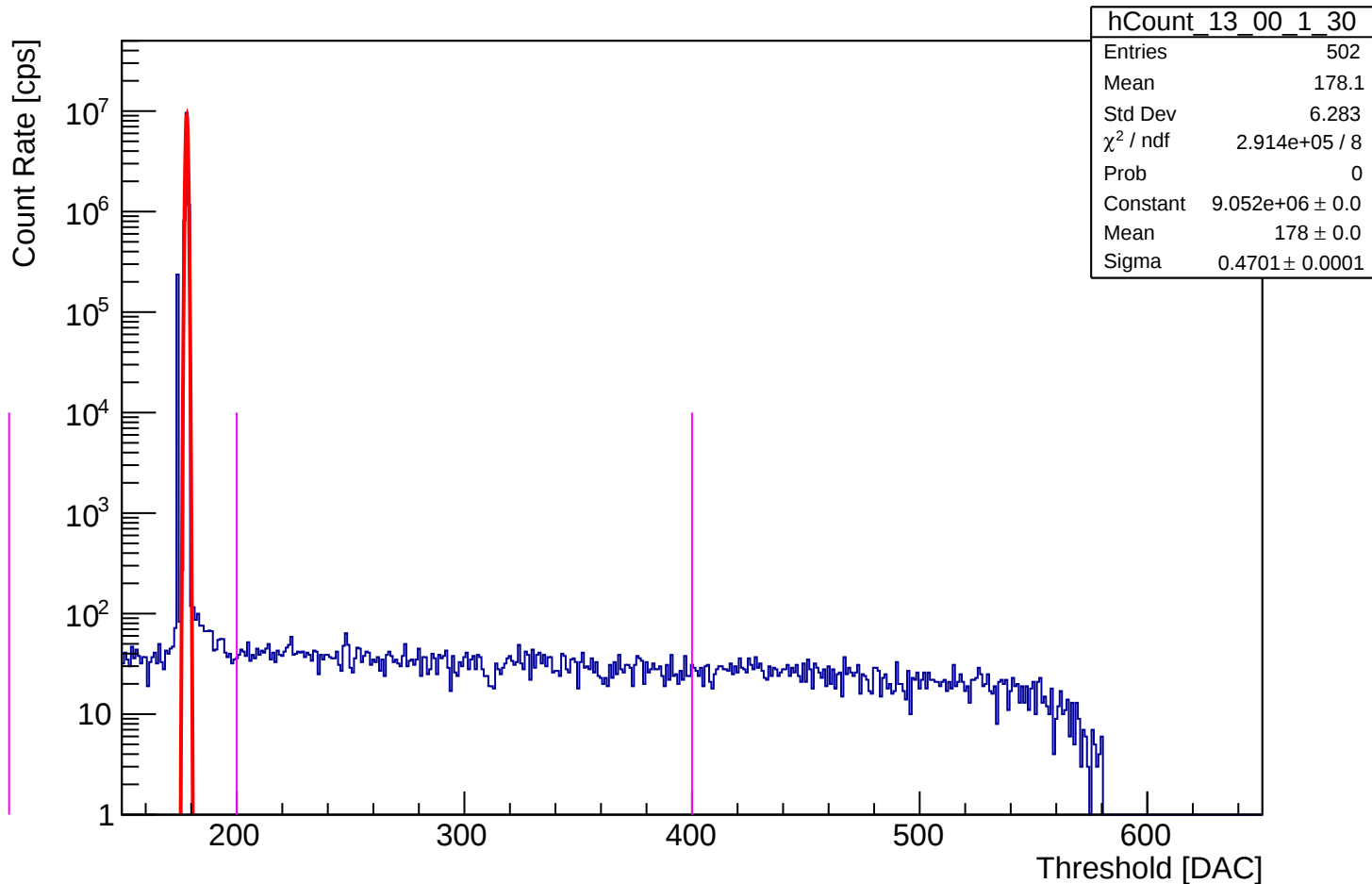
Row 1 Tile 1 Pmt 2 Pixel 1 Slot 13 Fiber 0 Asic 1 Channel 31



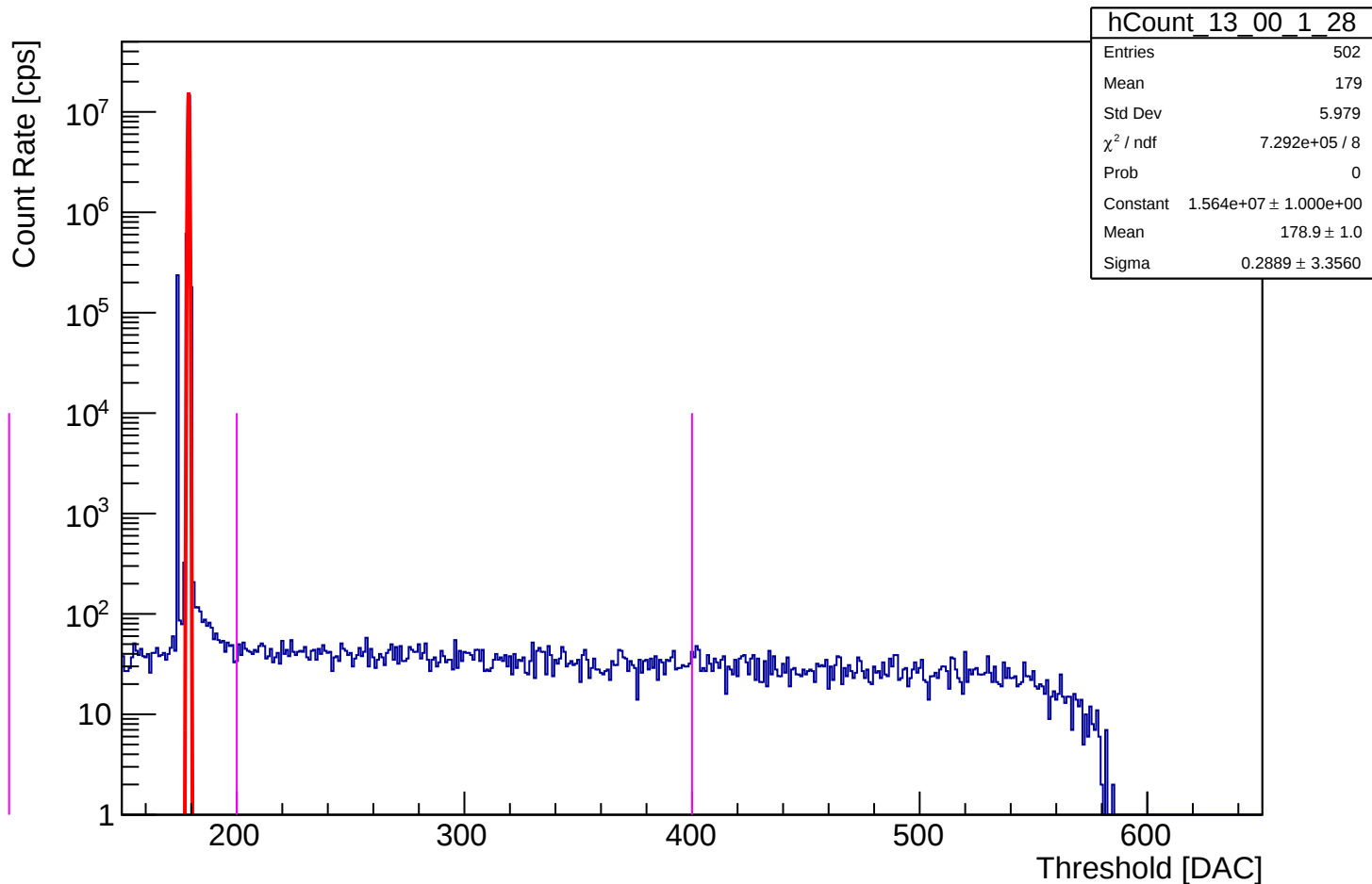
Row 1 Tile 1 Pmt 2 Pixel 2 Slot 13 Fiber 0 Asic 1 Channel 29



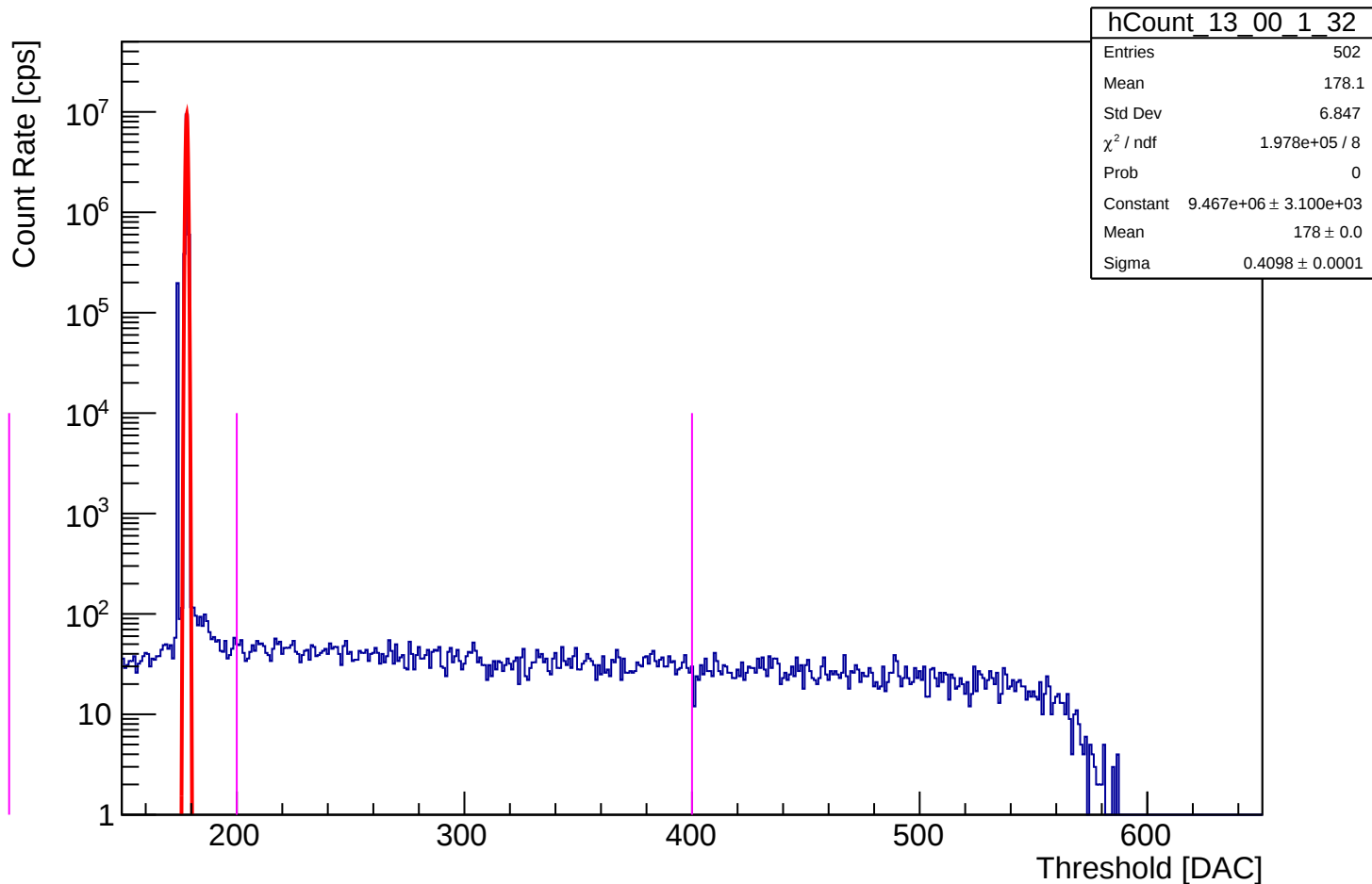
Row 1 Tile 1 Pmt 2 Pixel 3 Slot 13 Fiber 0 Asic 1 Channel 30



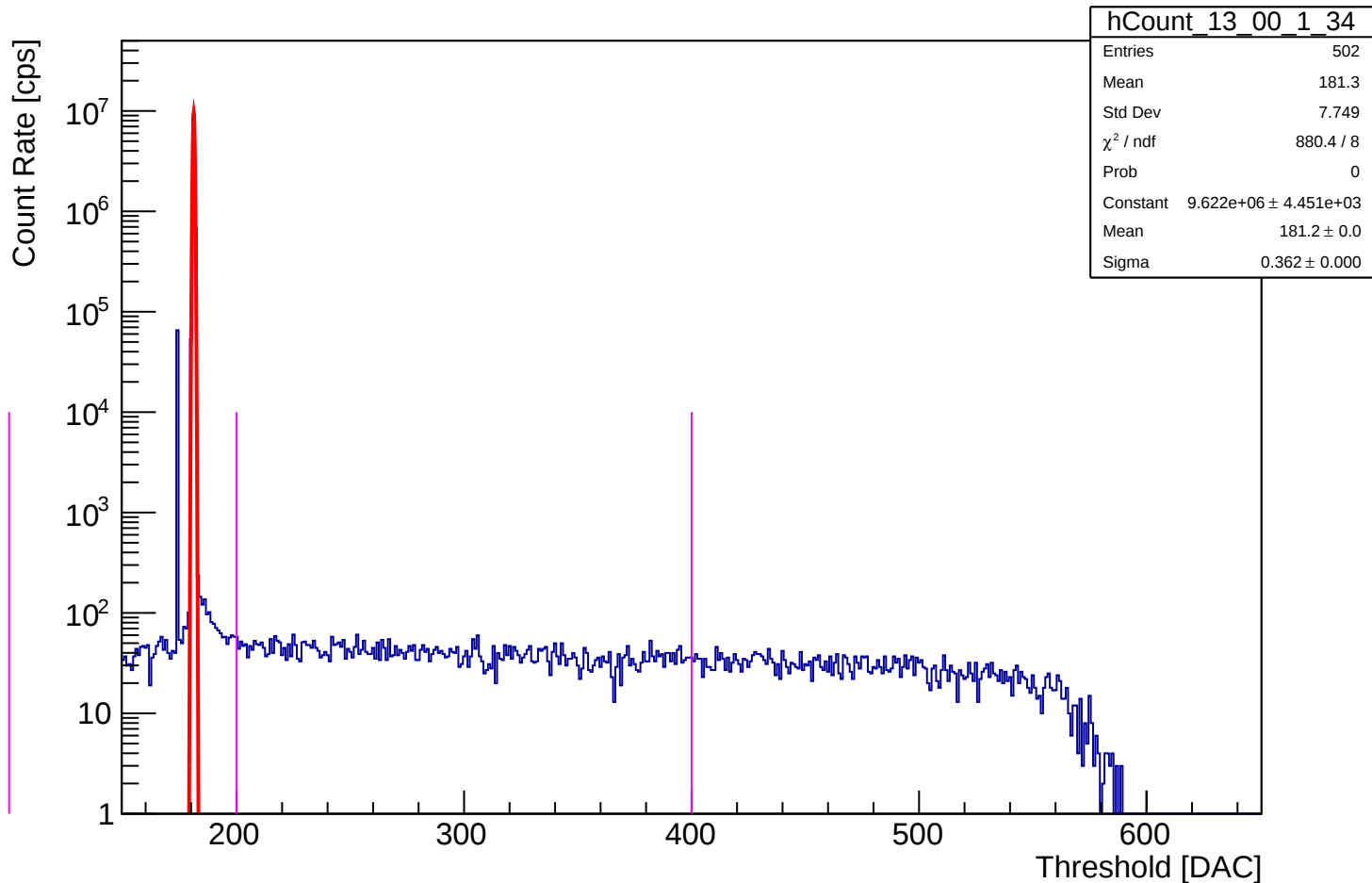
Row 1 Tile 1 Pmt 2 Pixel 4 Slot 13 Fiber 0 Asic 1 Channel 28



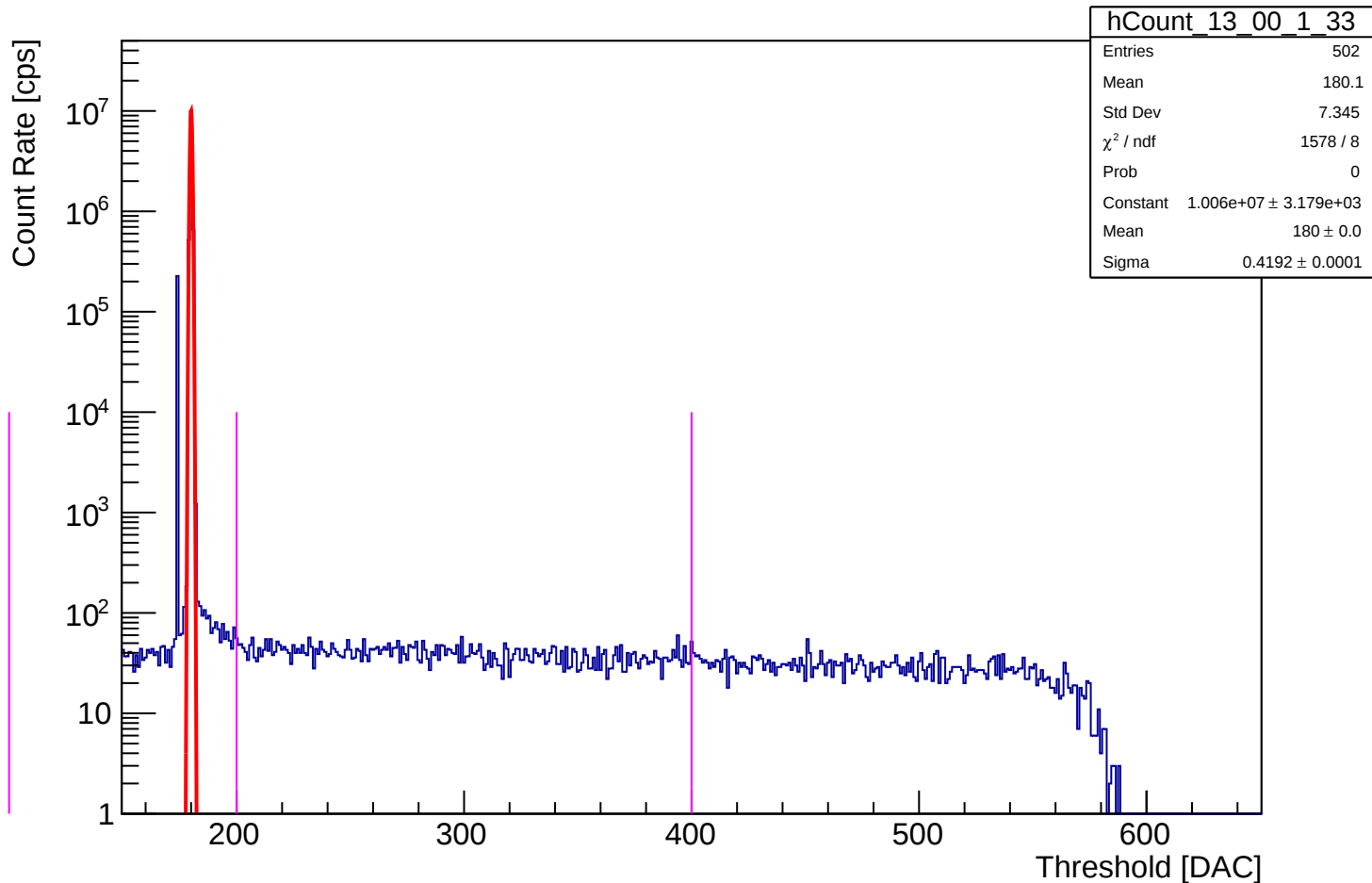
Row 1 Tile 1 Pmt 2 Pixel 5 Slot 13 Fiber 0 Asic 1 Channel 32



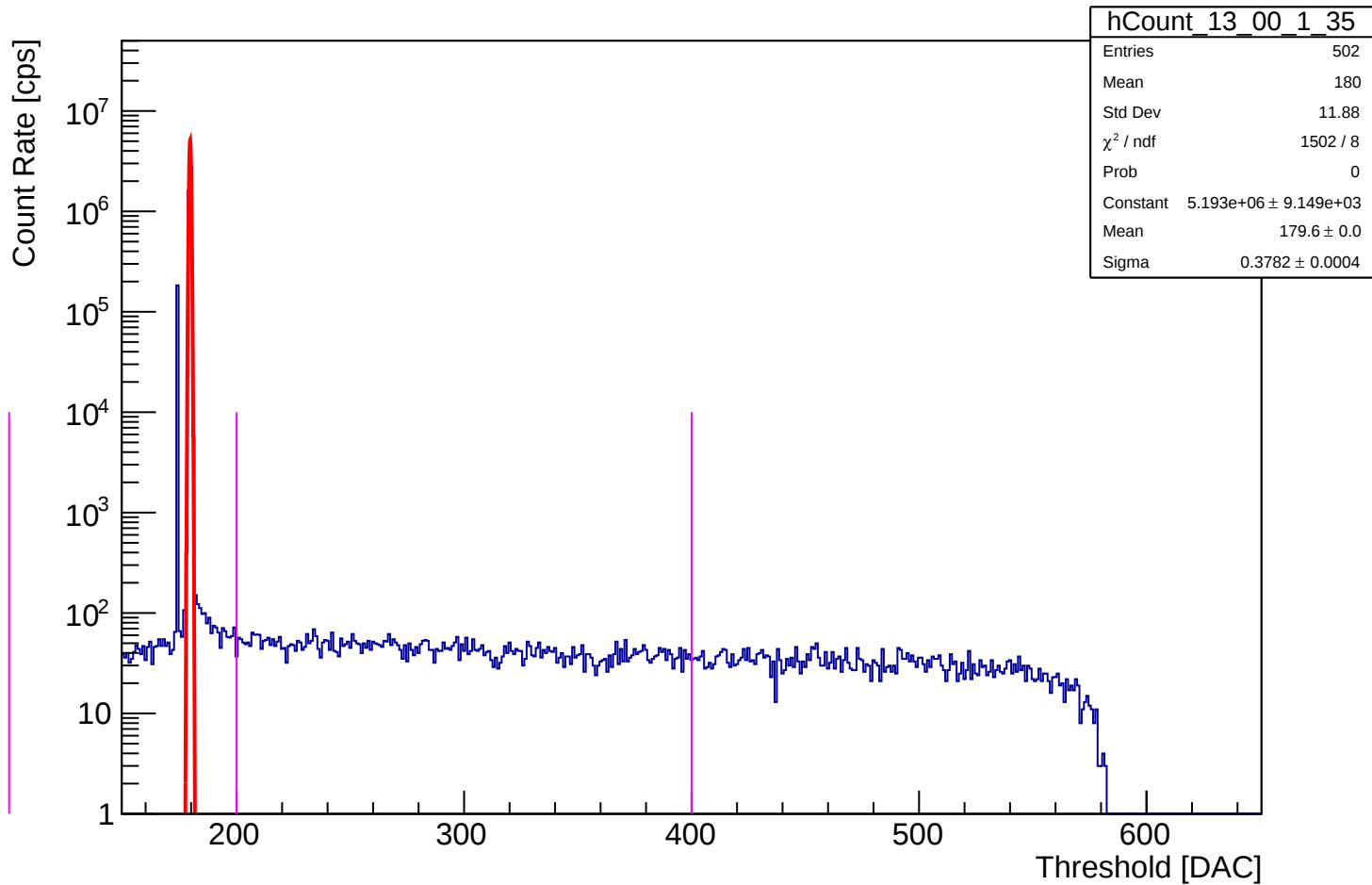
Row 1 Tile 1 Pmt 2 Pixel 6 Slot 13 Fiber 0 Asic 1 Channel 34



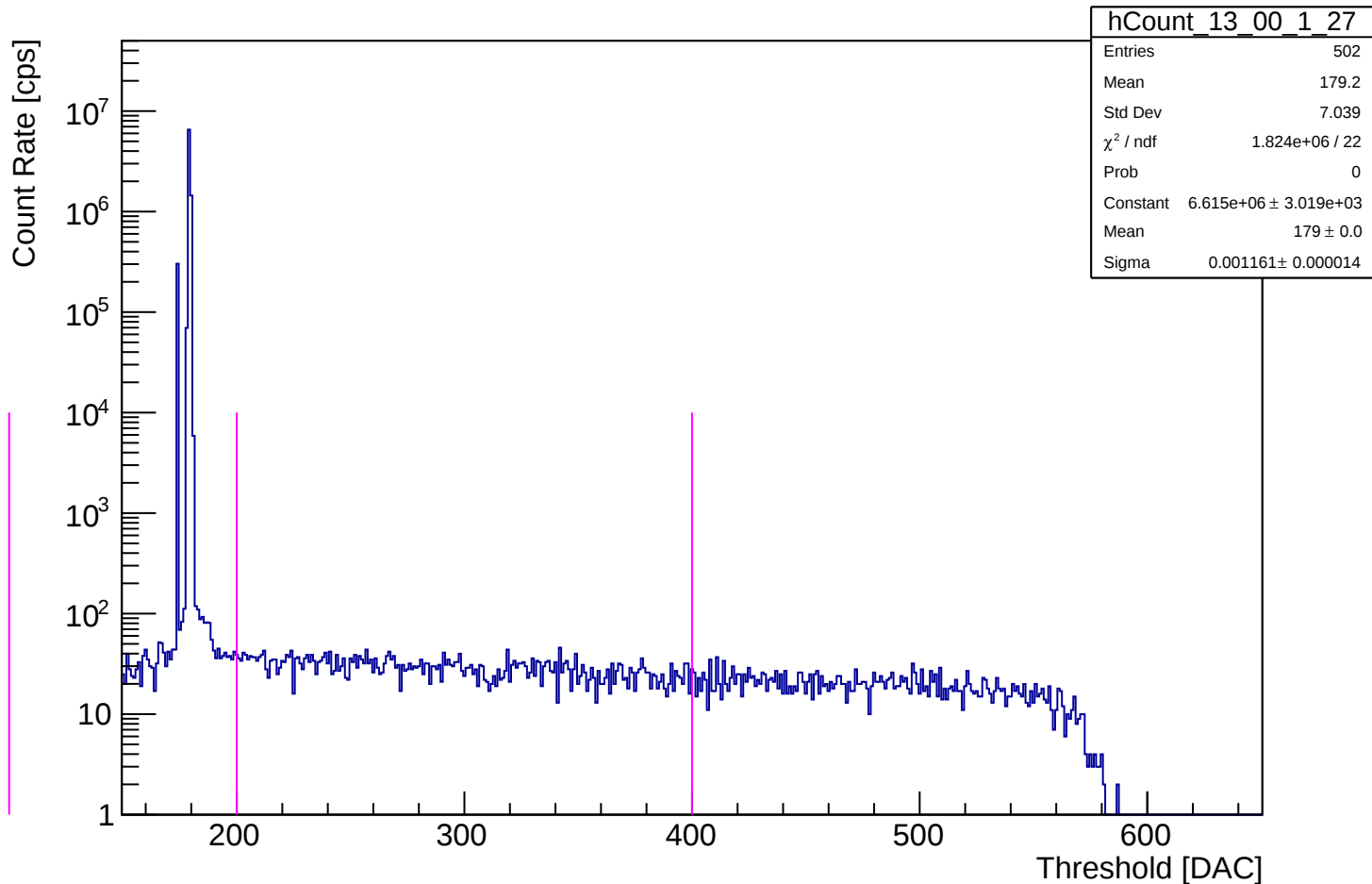
Row 1 Tile 1 Pmt 2 Pixel 7 Slot 13 Fiber 0 Asic 1 Channel 33



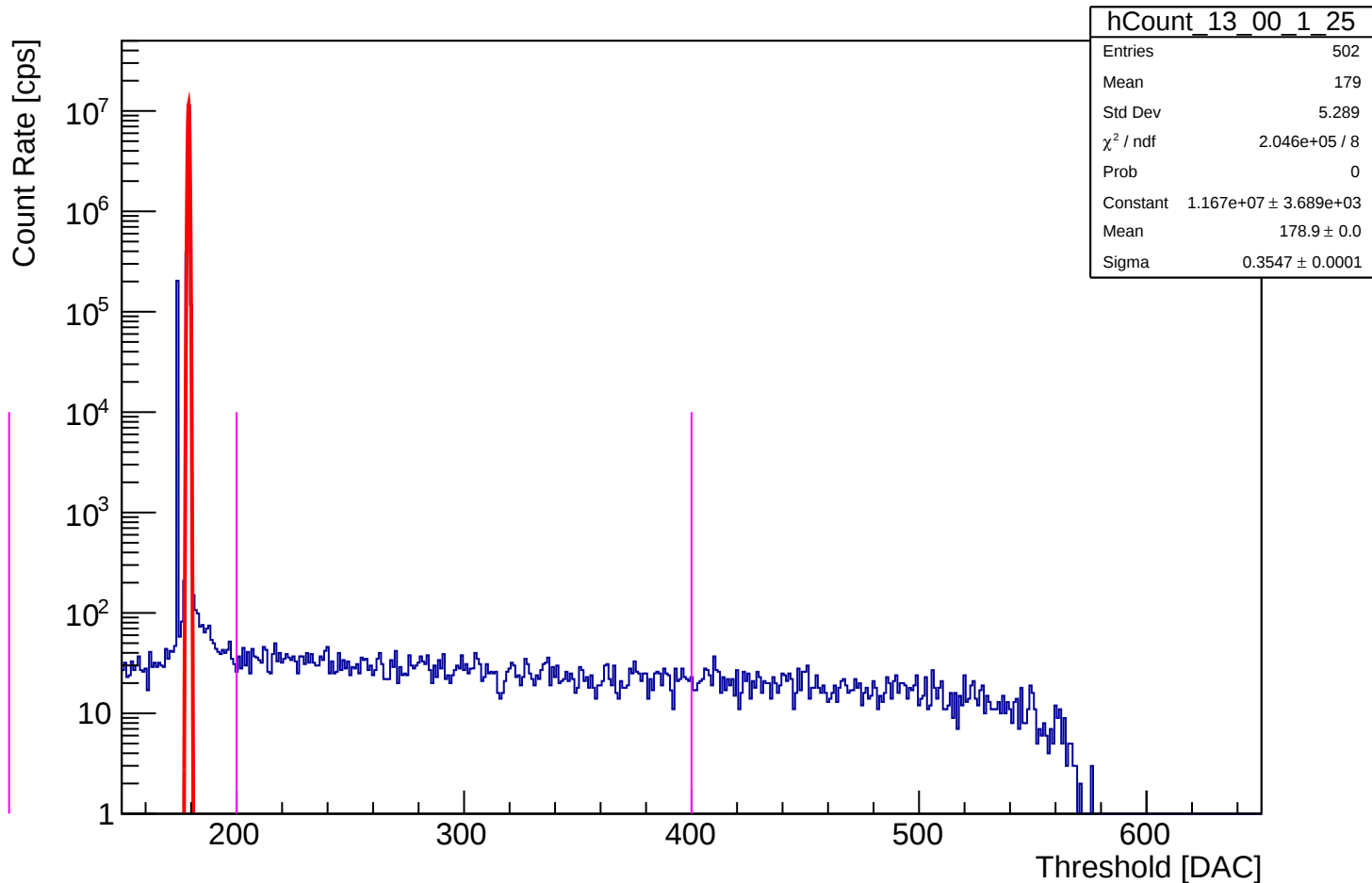
Row 1 Tile 1 Pmt 2 Pixel 8 Slot 13 Fiber 0 Asic 1 Channel 35



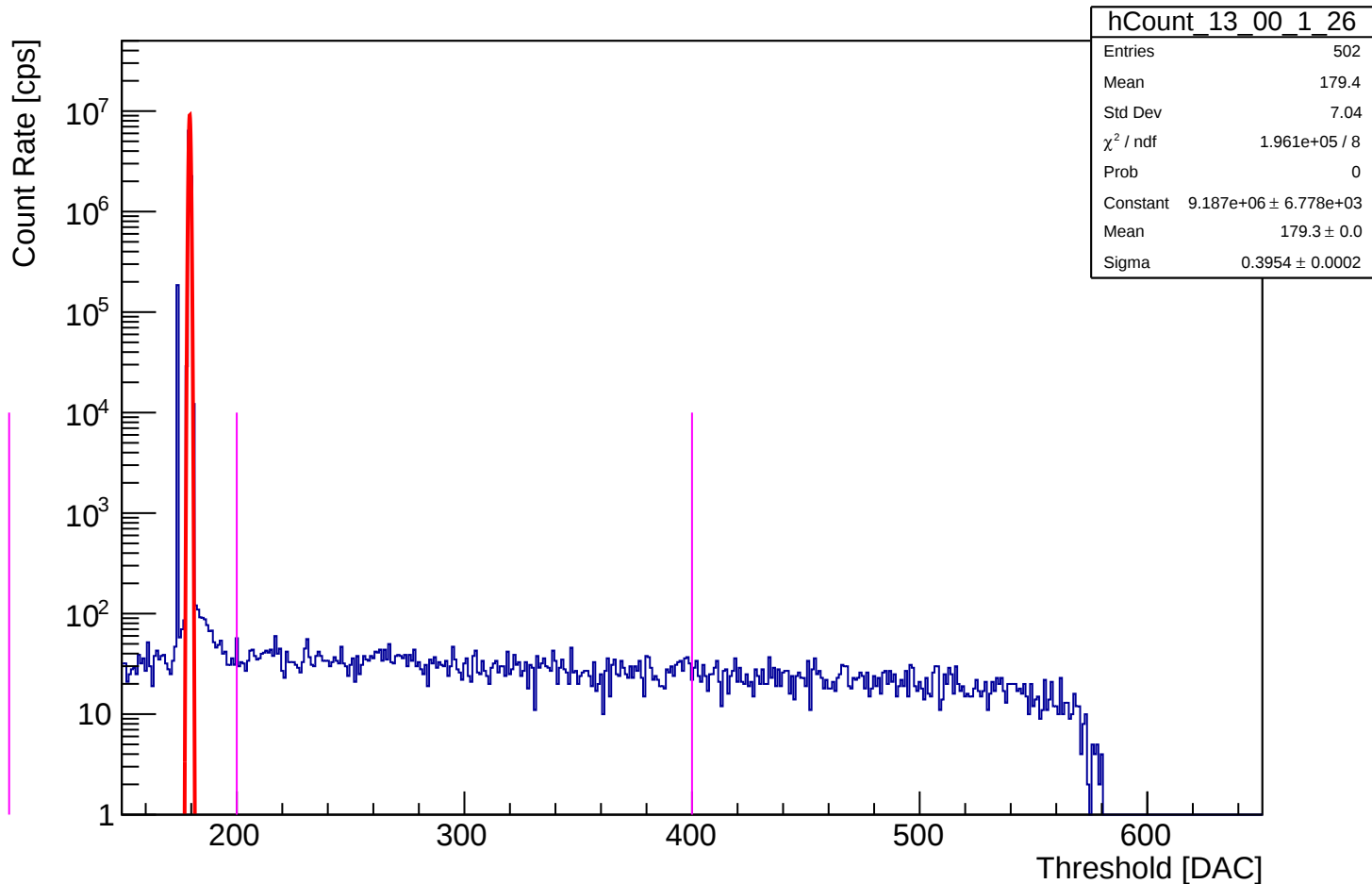
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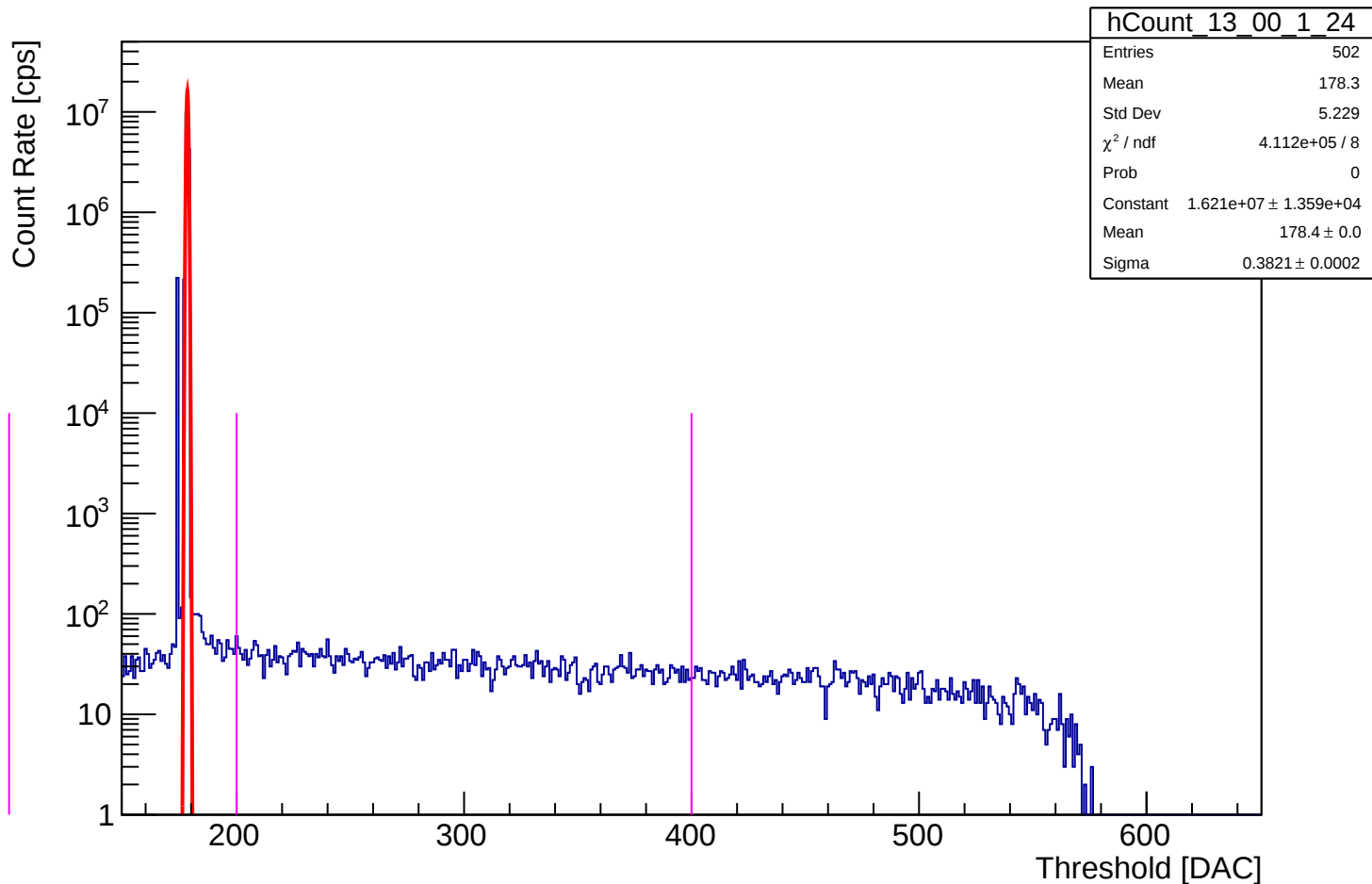
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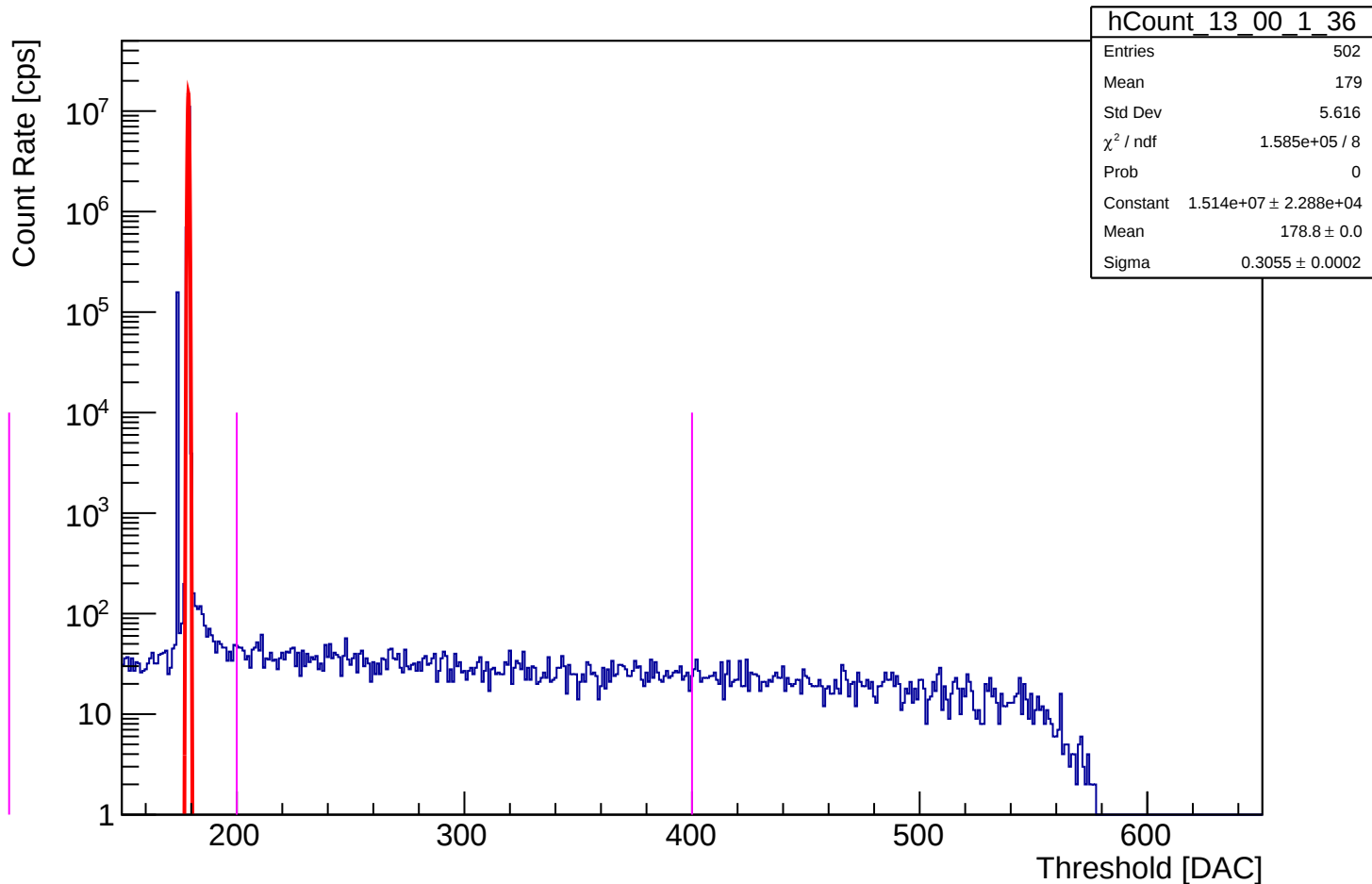
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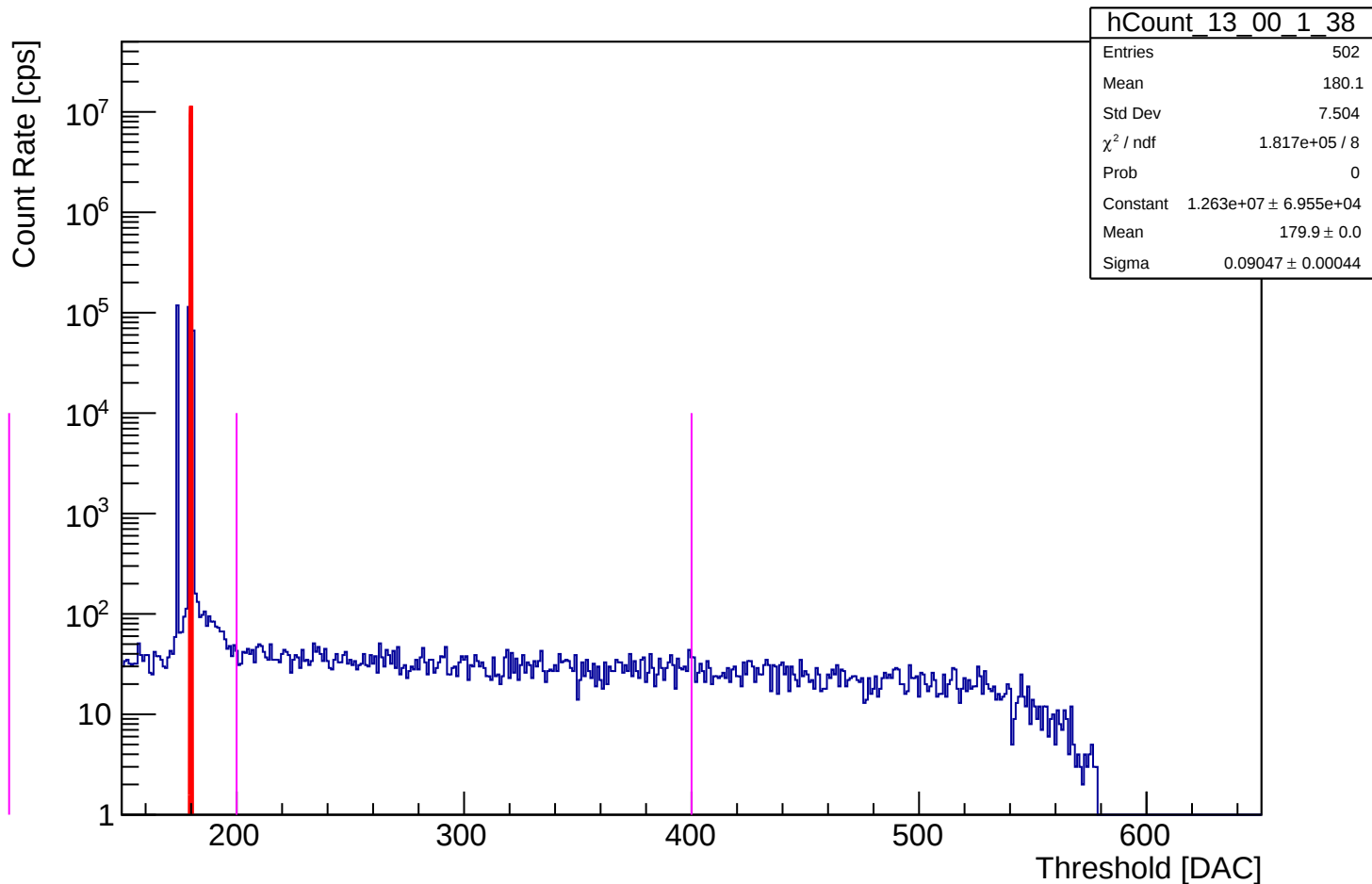
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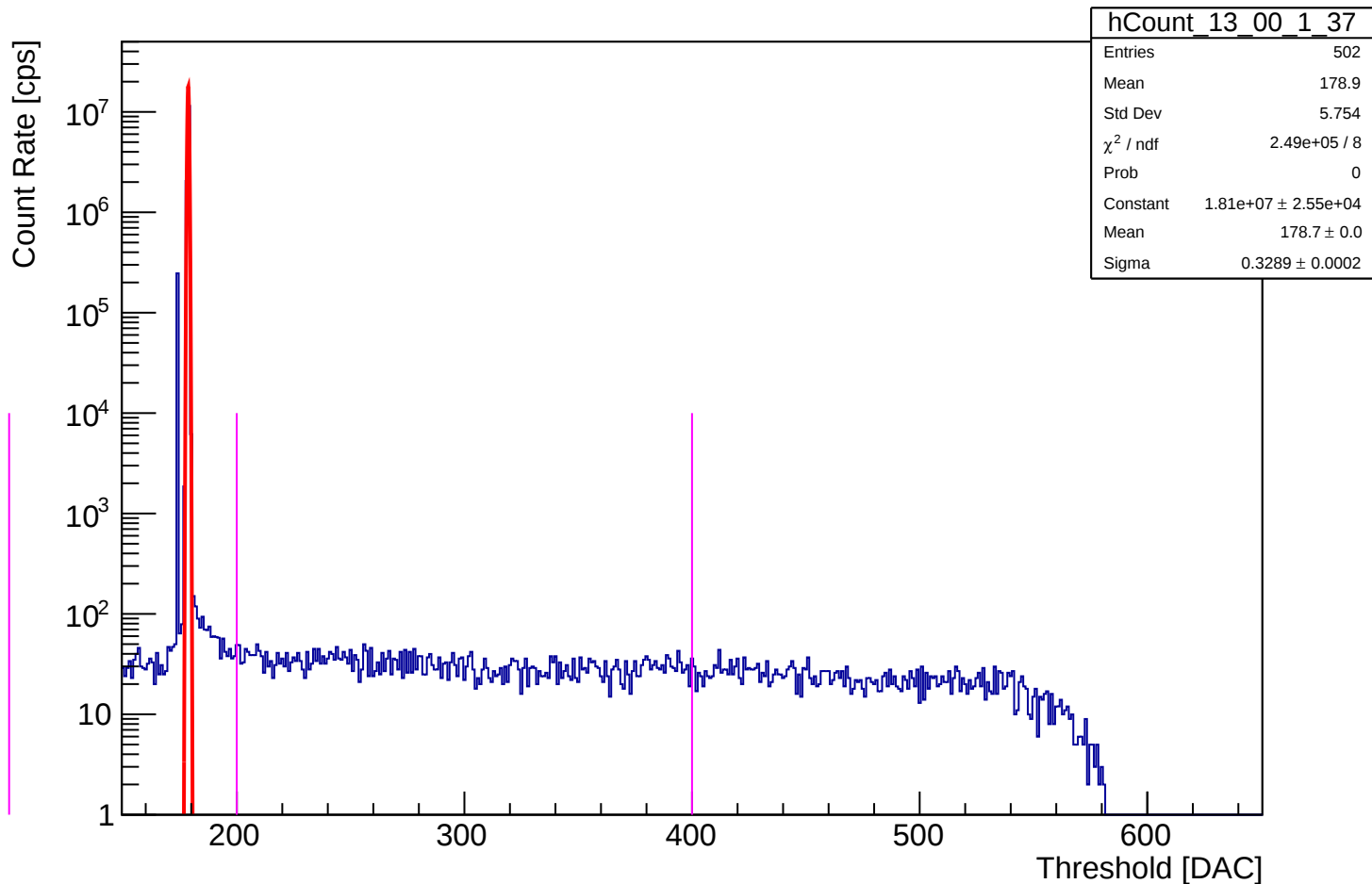
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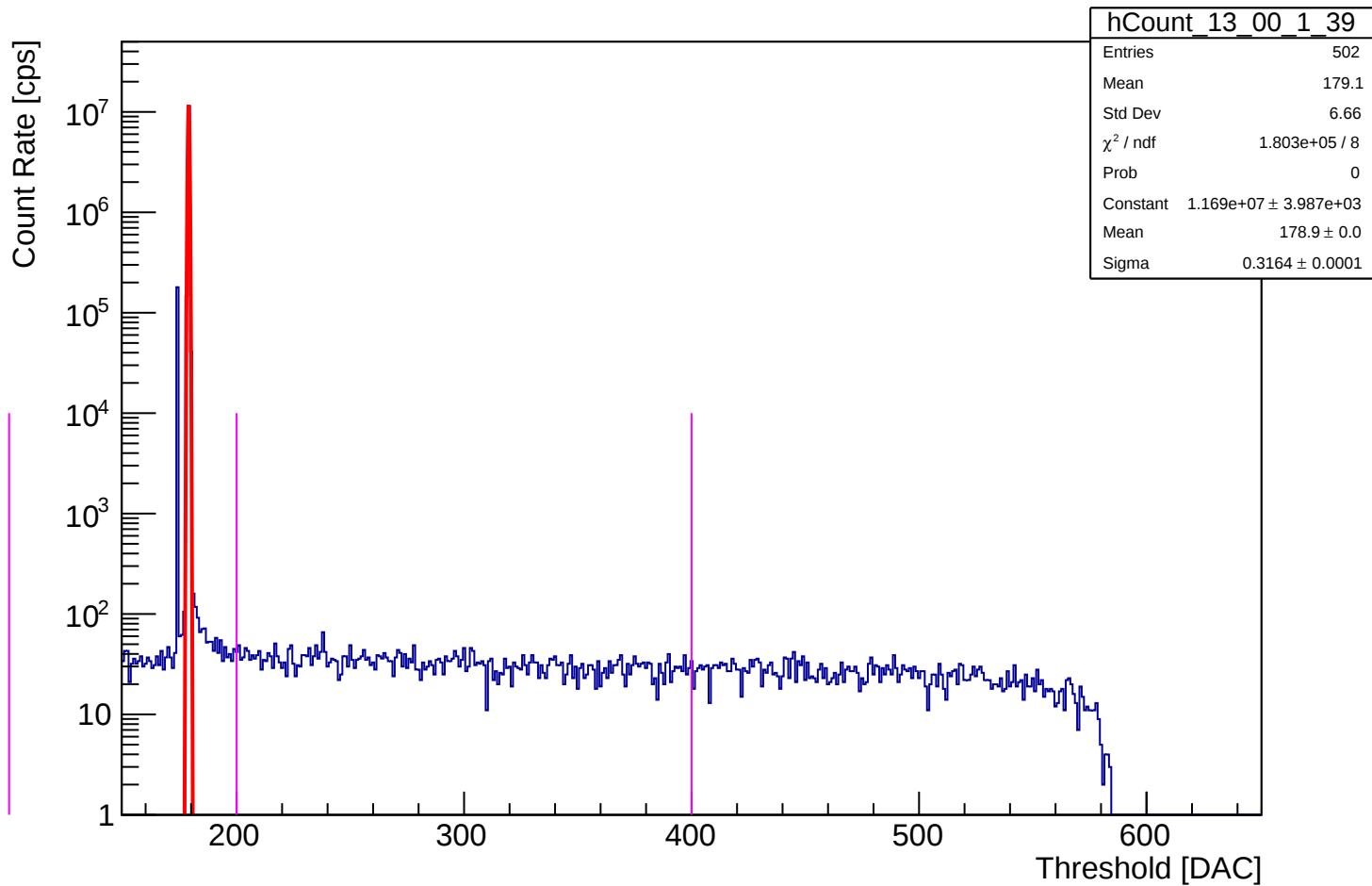
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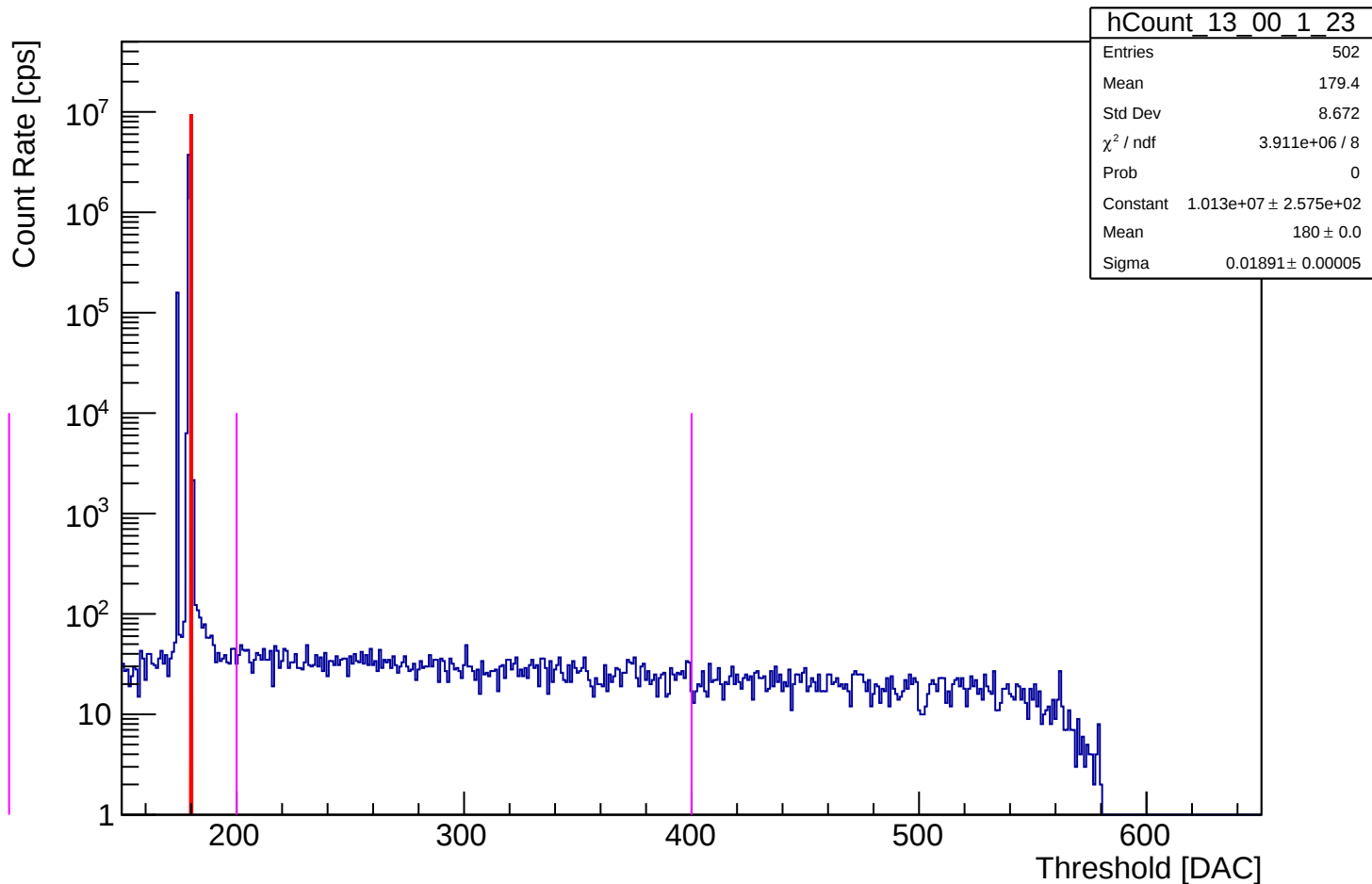
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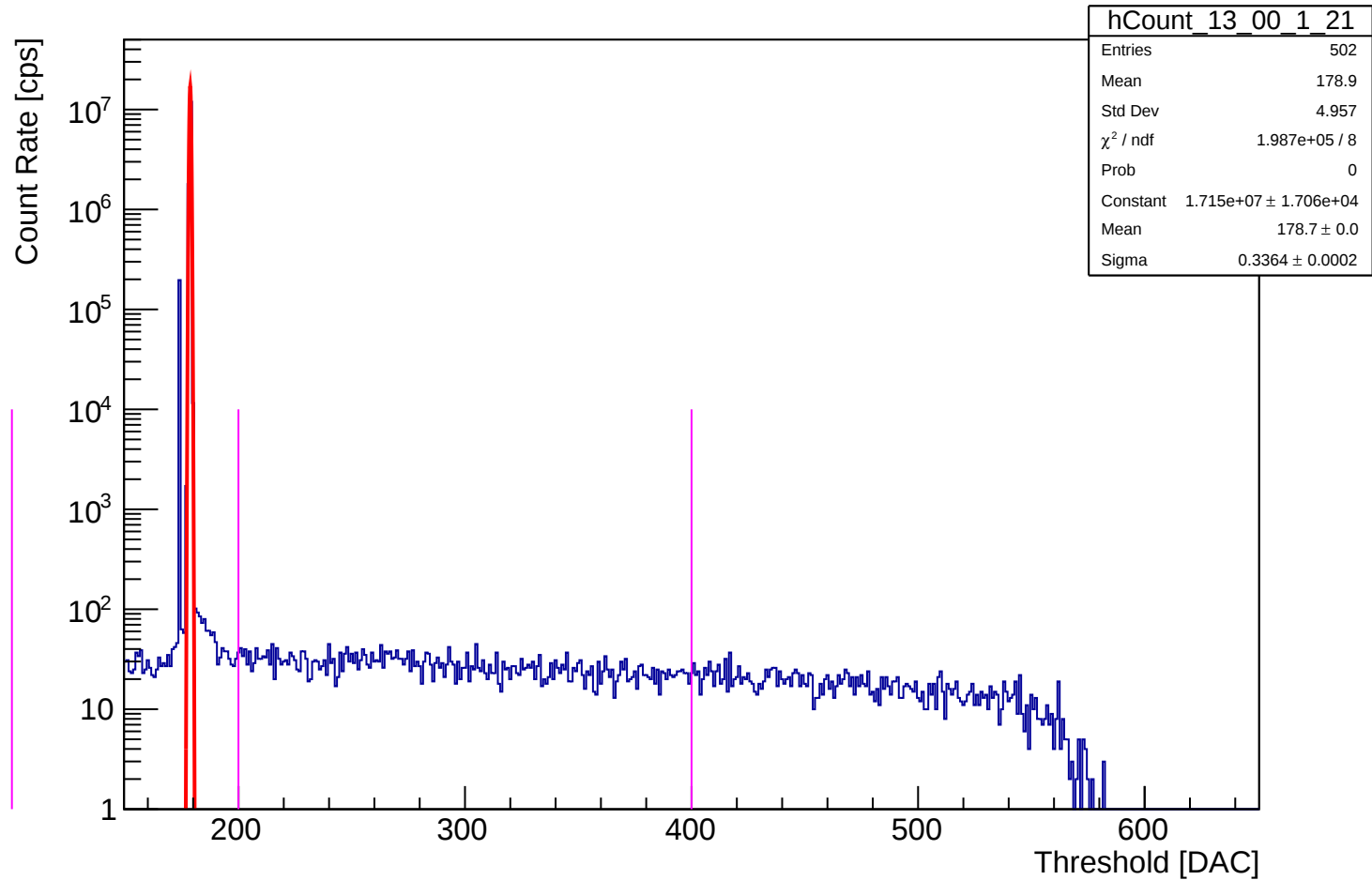


Row 1 Tile 1 Pmt 2 Pixel 16 Slot 13 Fiber 0 Asic 1 Channel 39

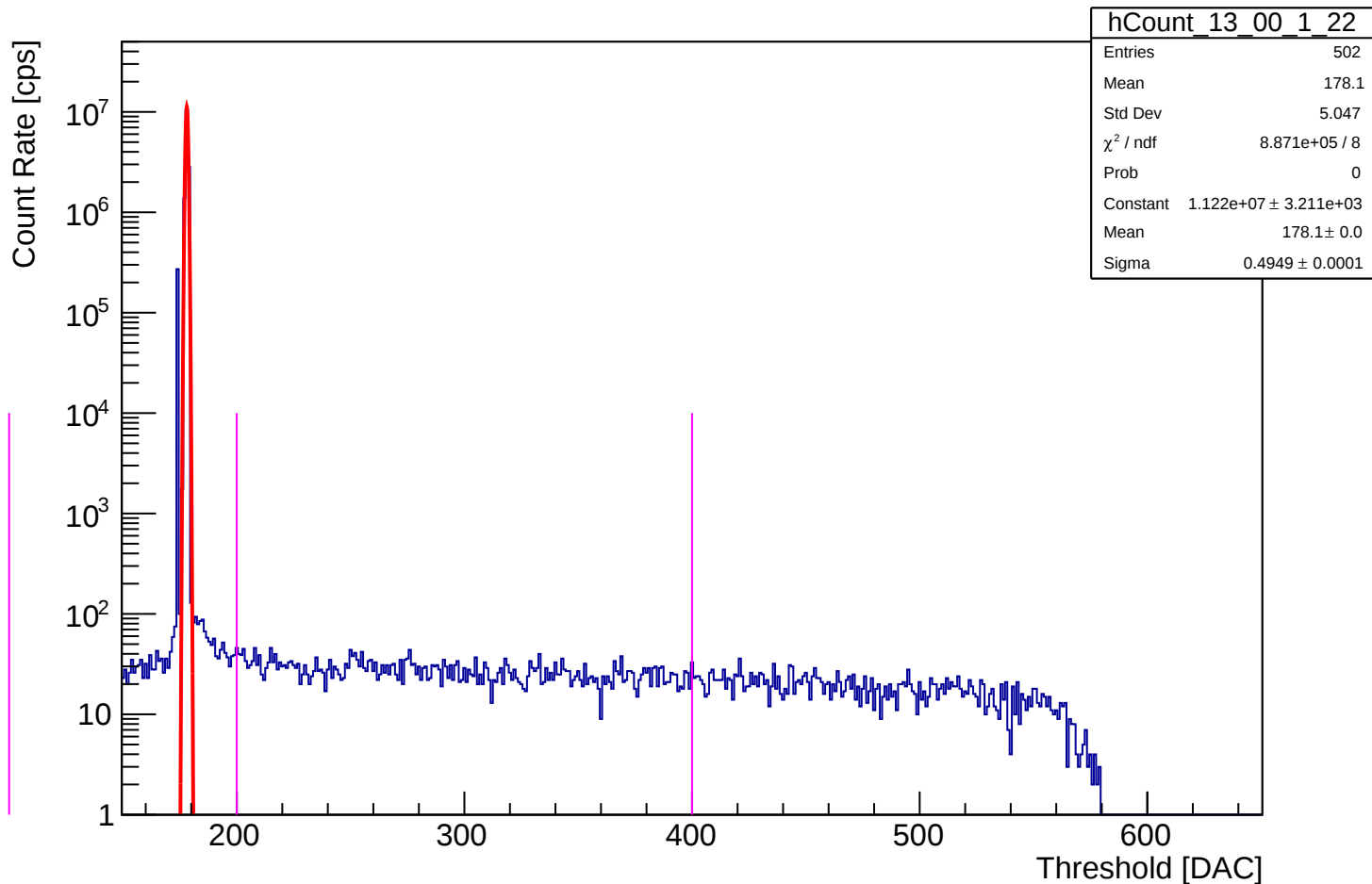


Row 1 Tile 1 Pmt 2 Pixel 17 Slot 13 Fiber 0 Asic 1 Channel 23

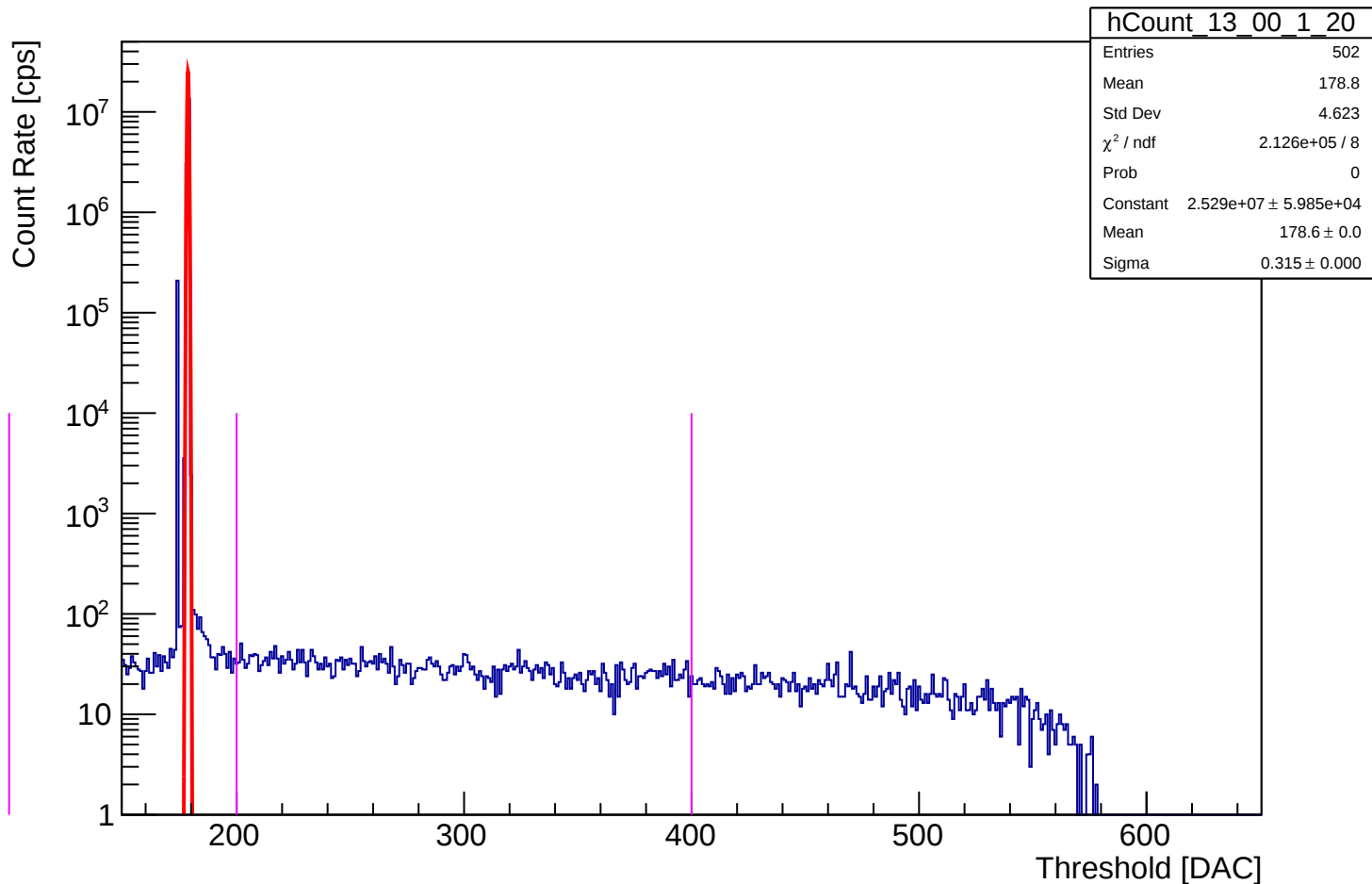




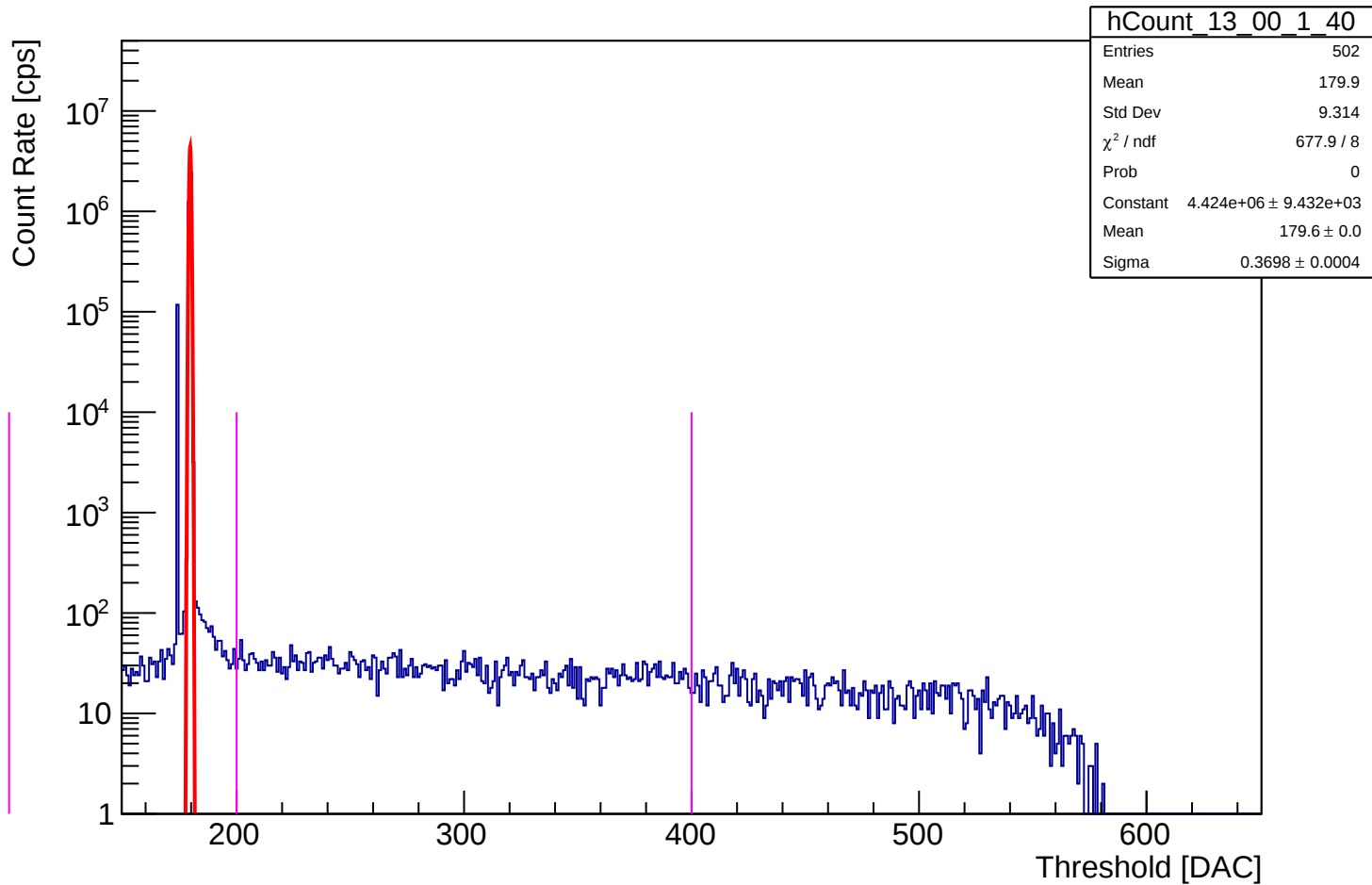
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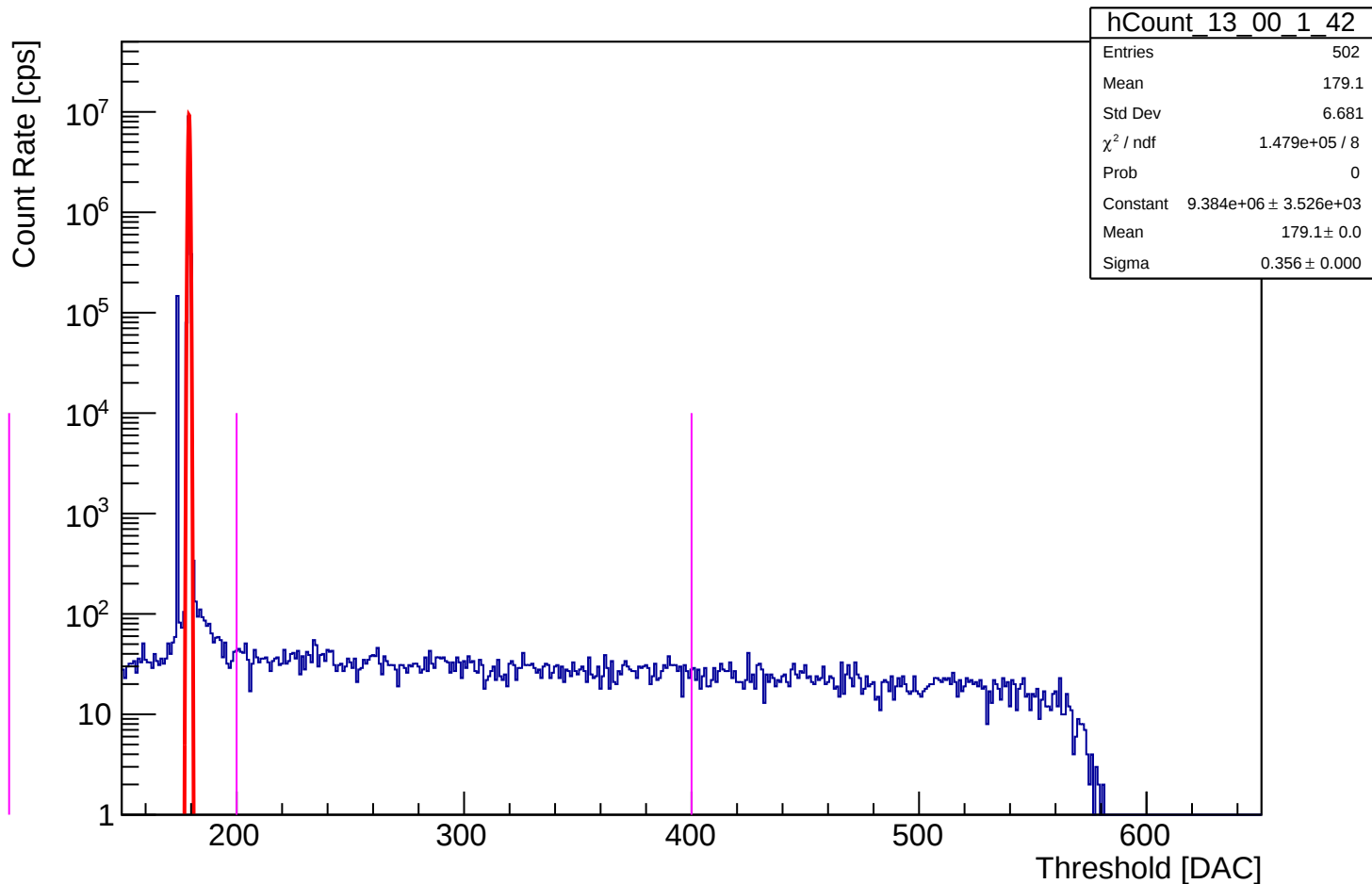
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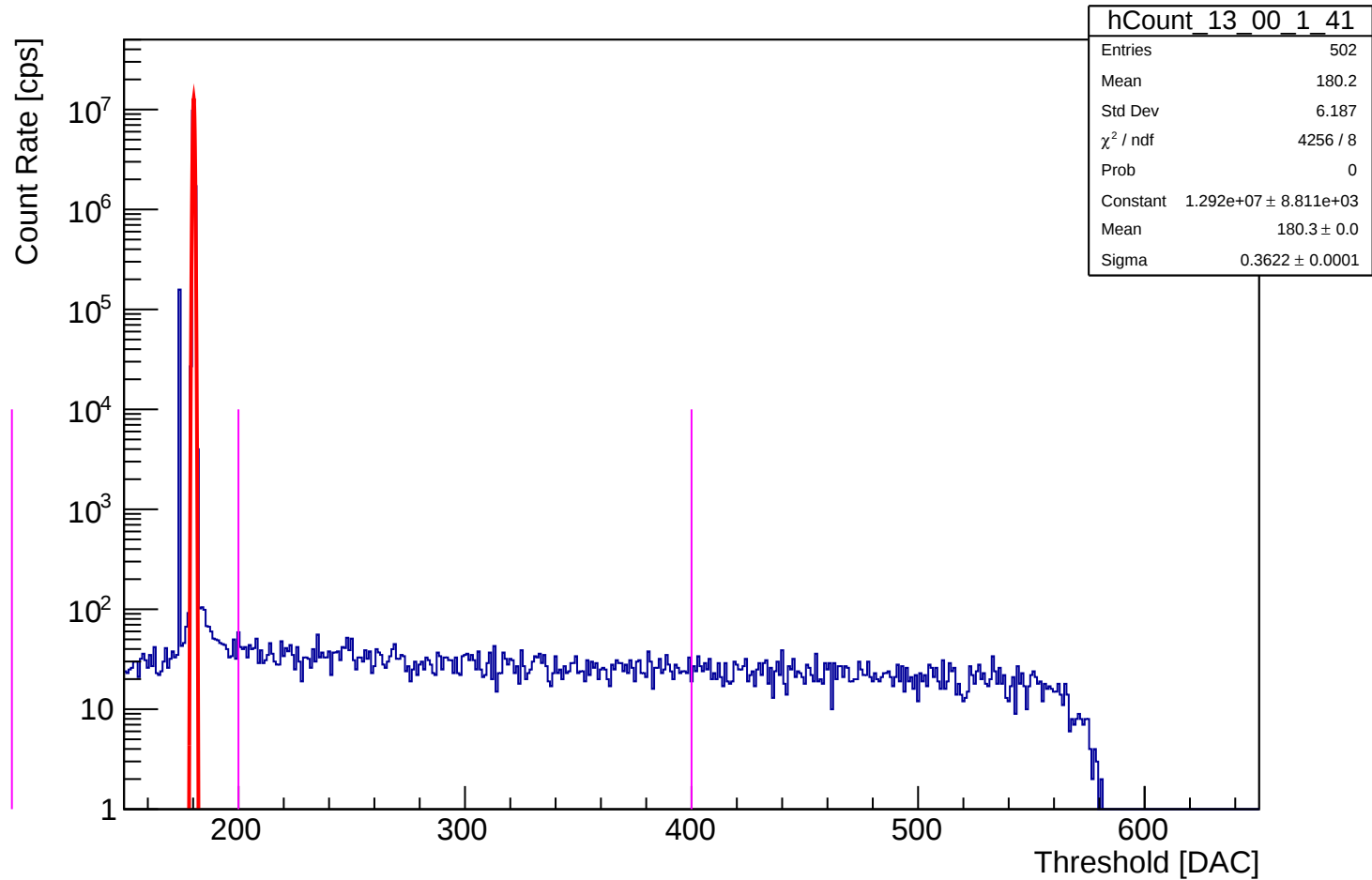


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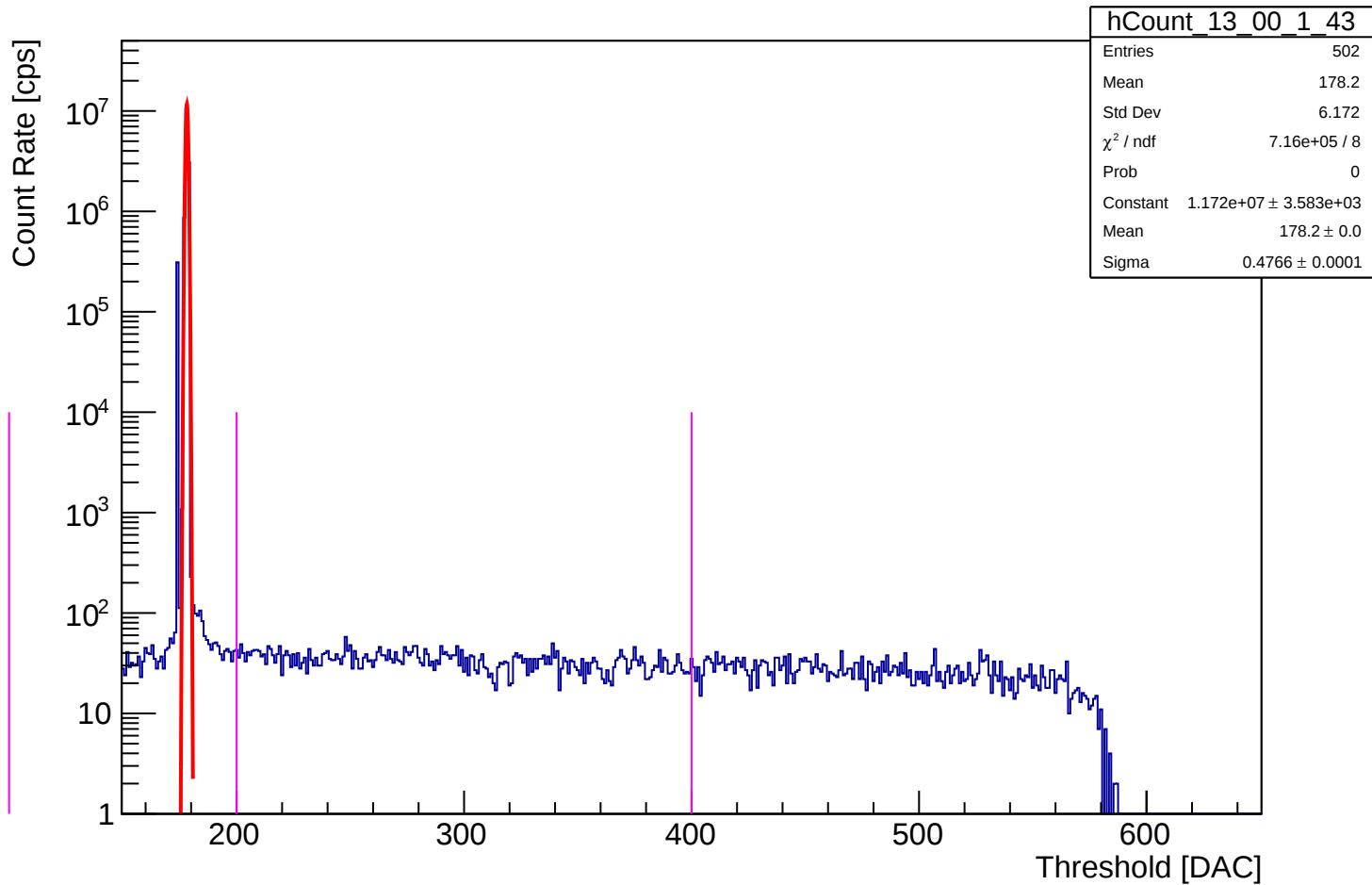


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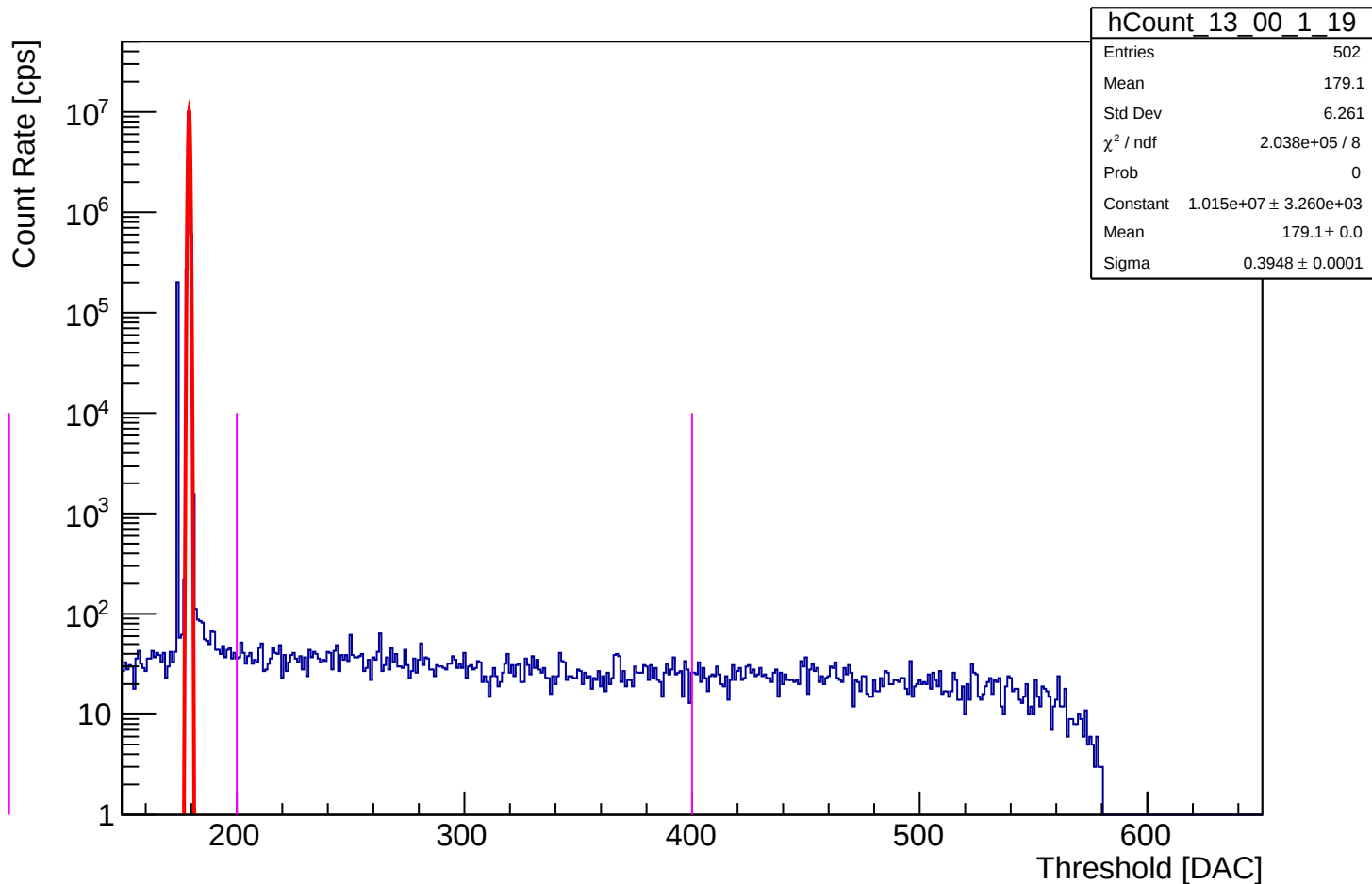




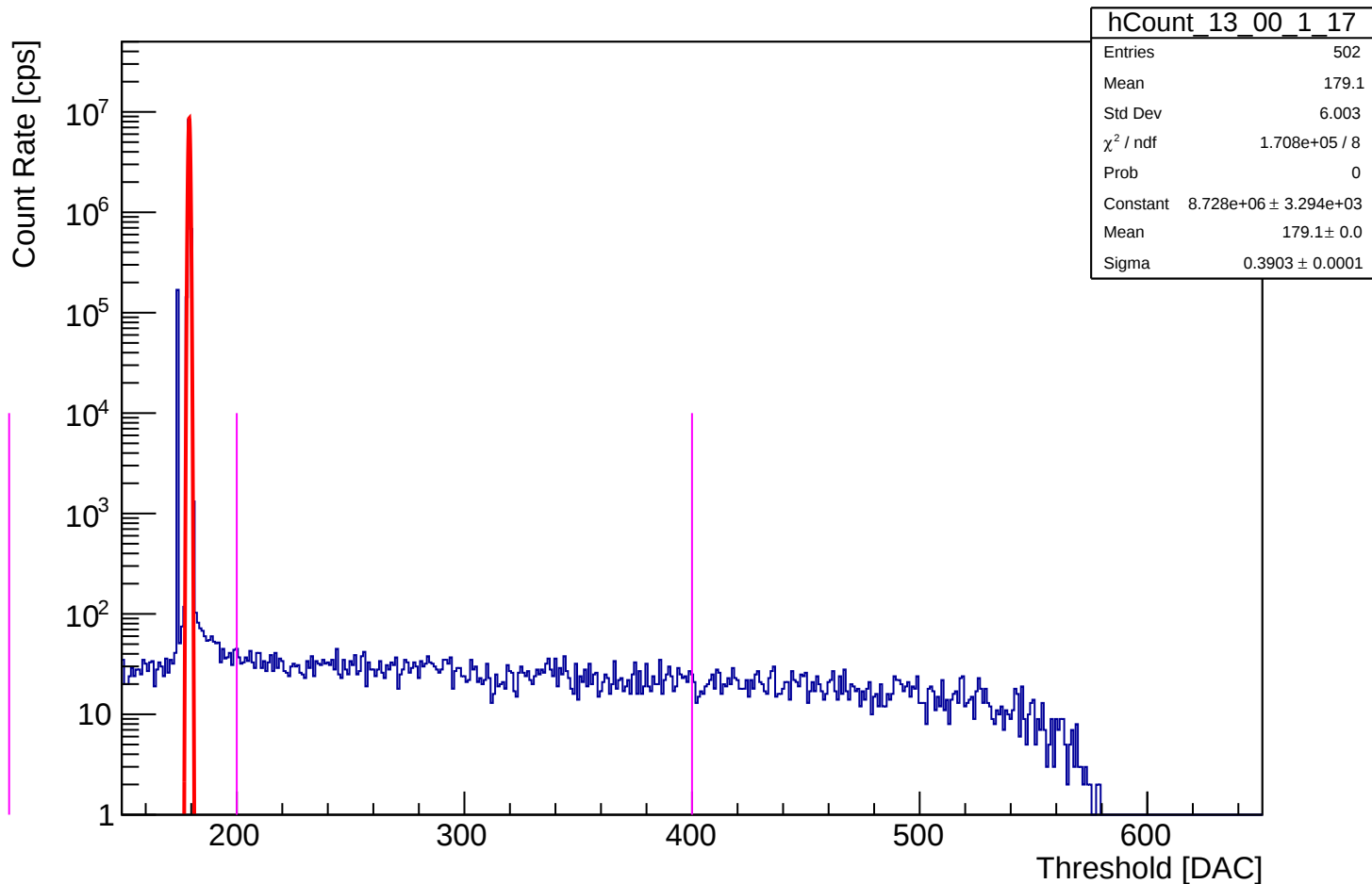
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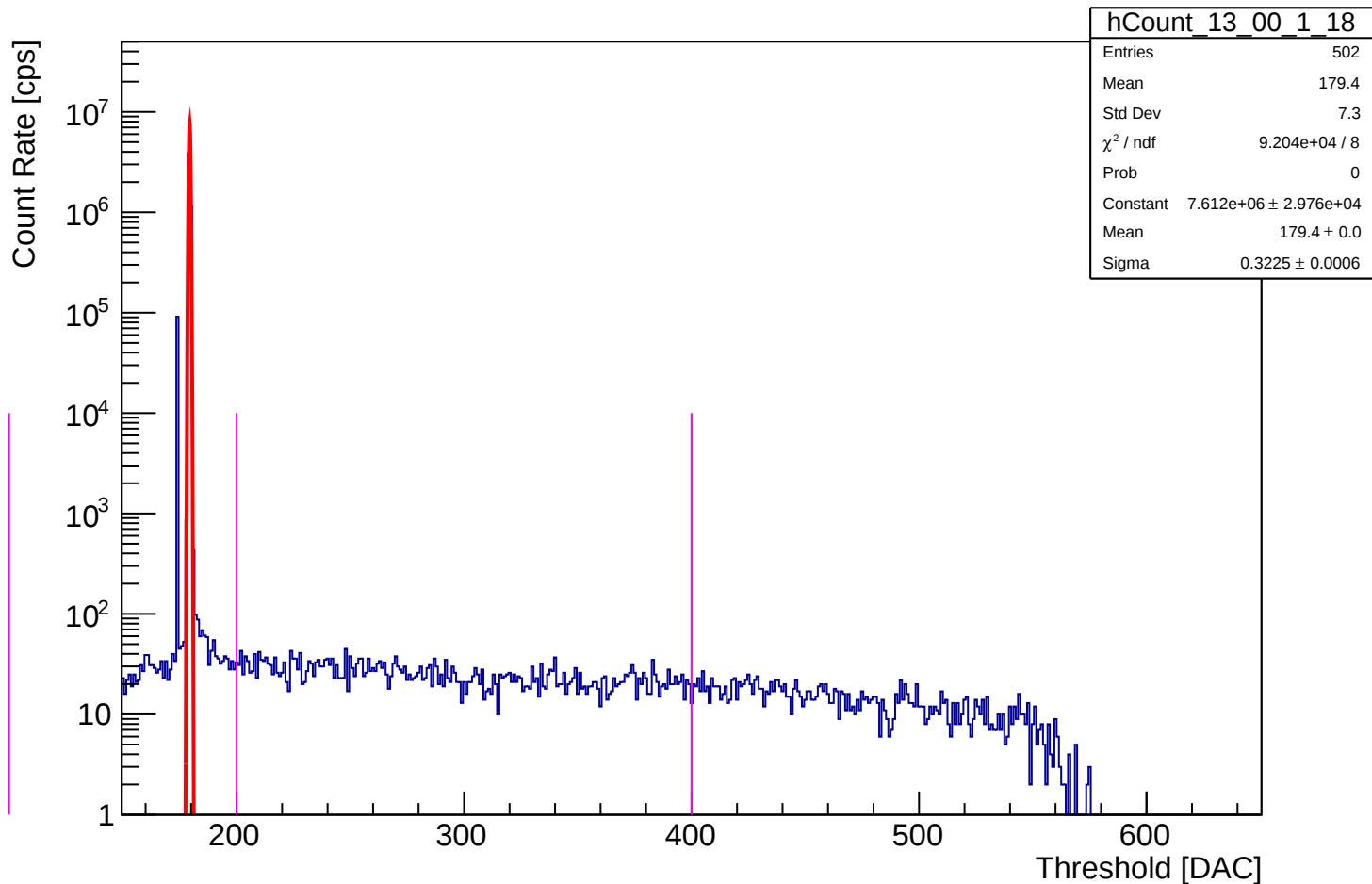
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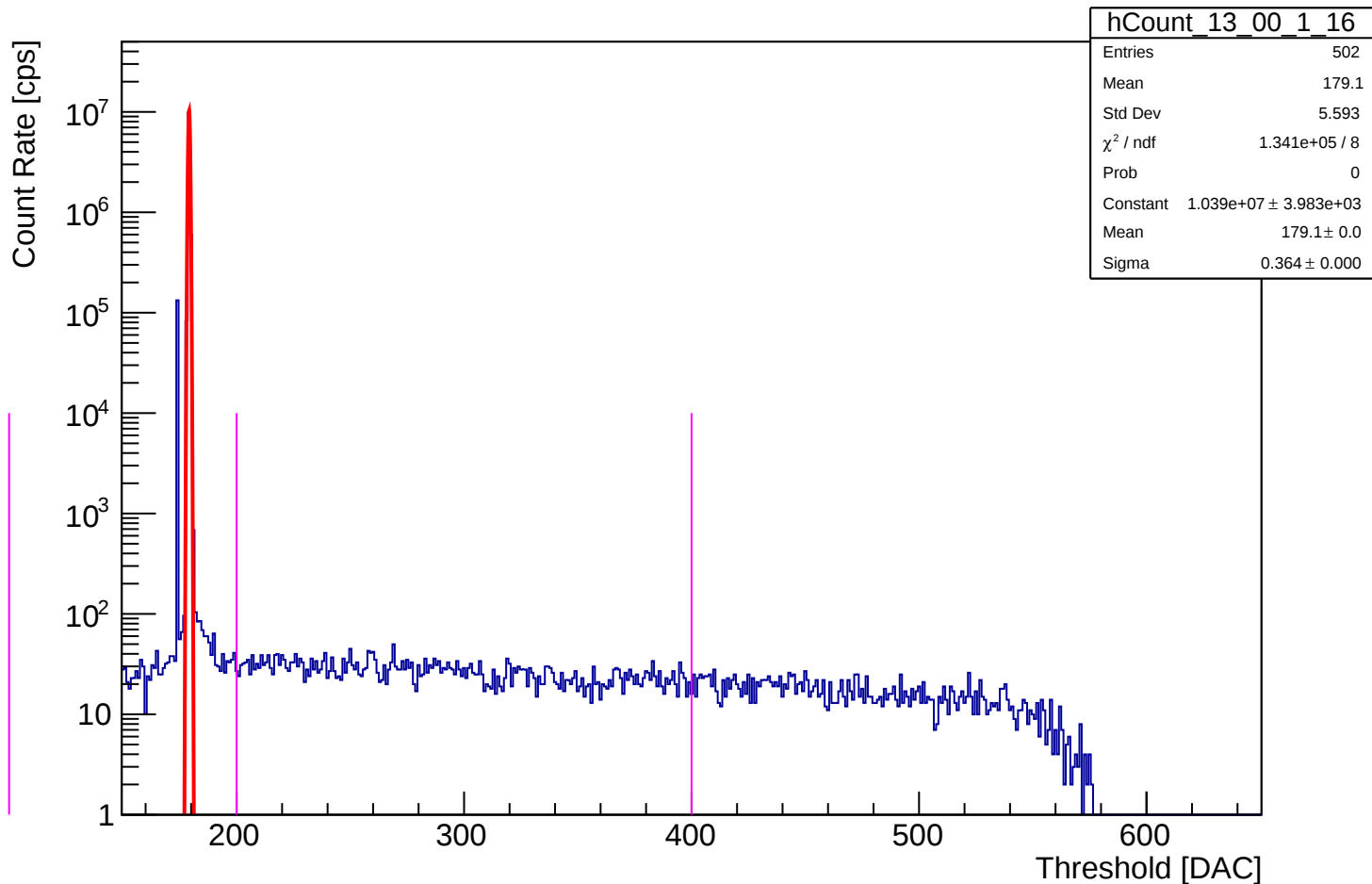
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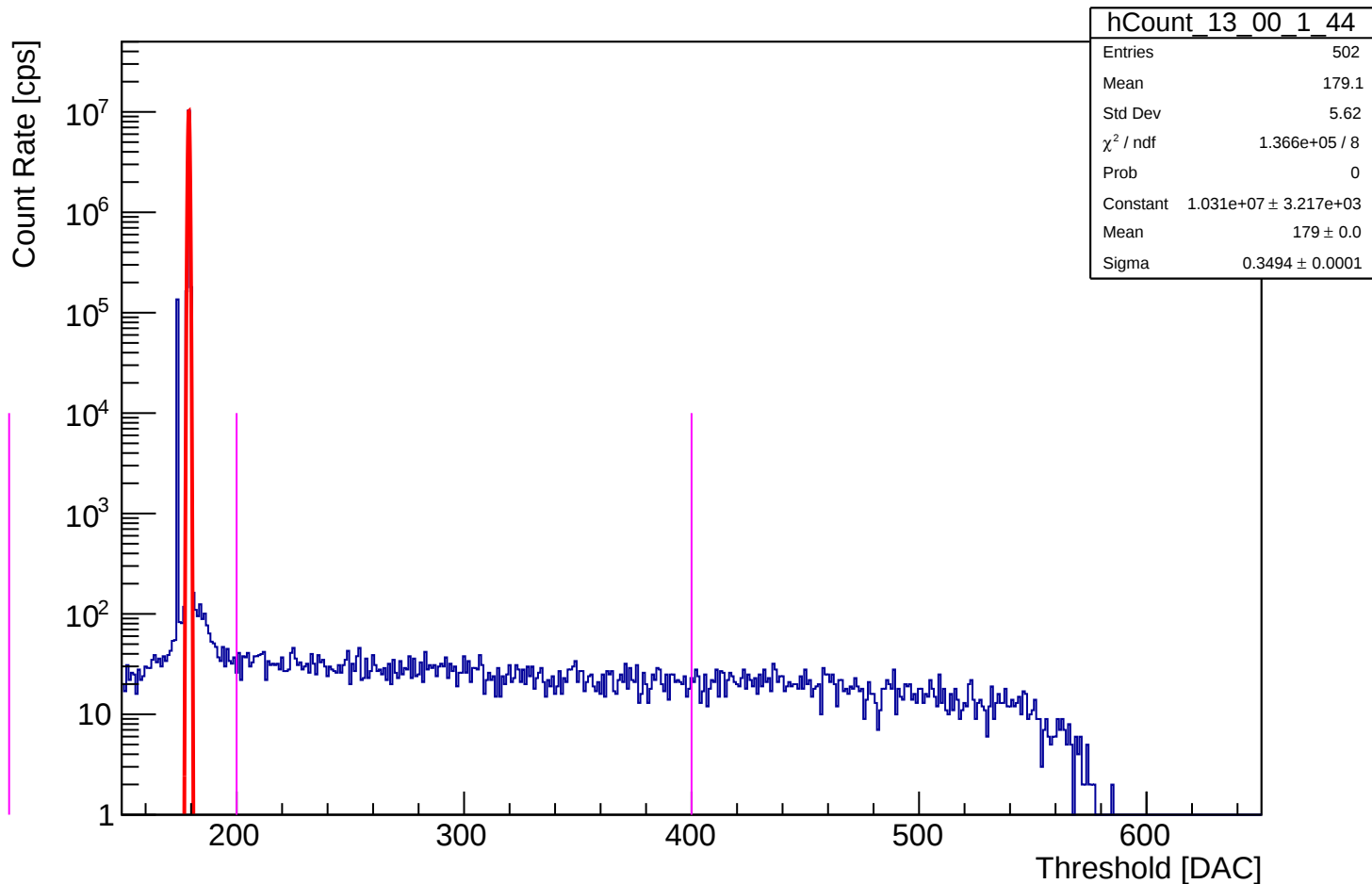
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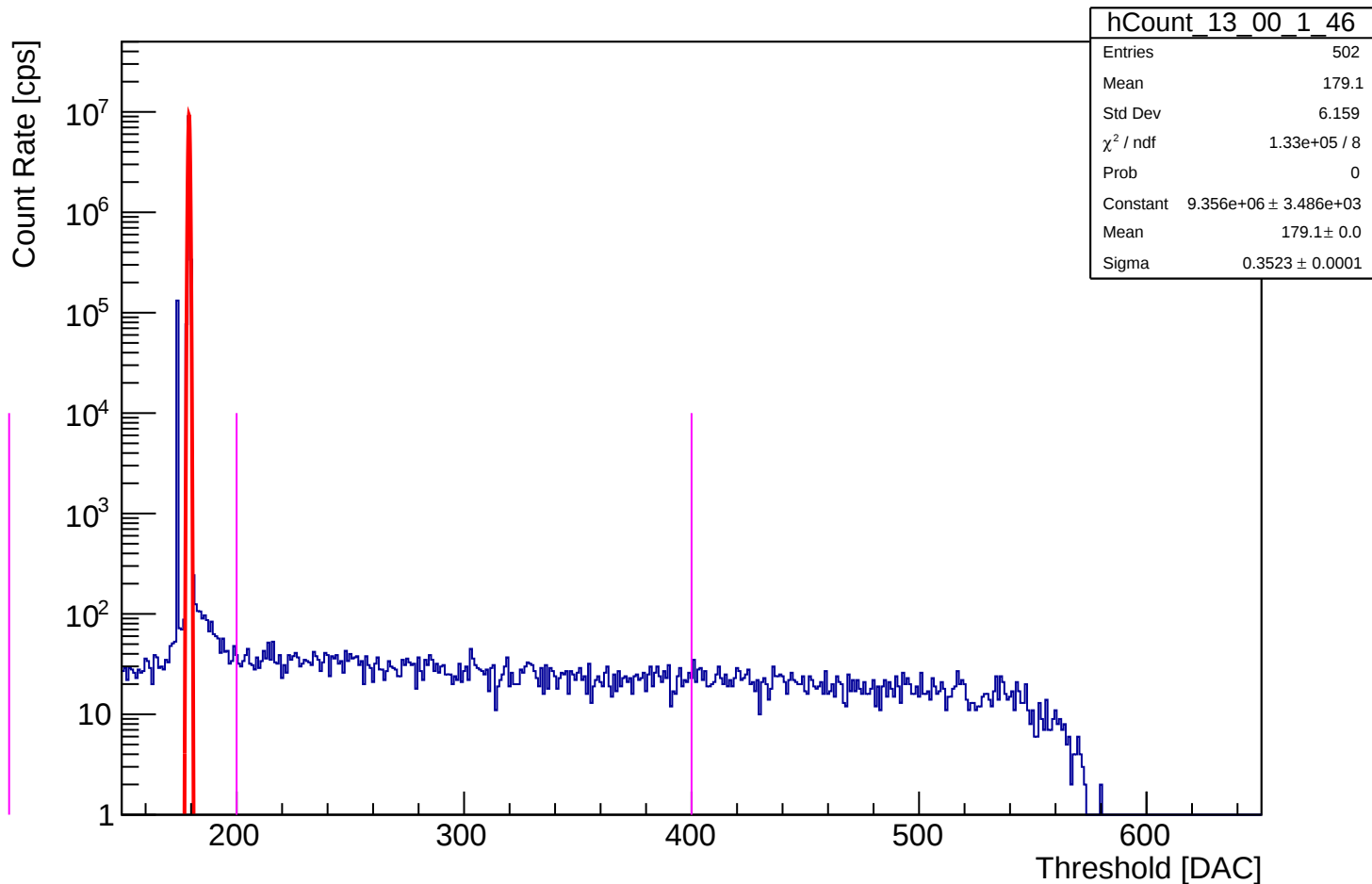
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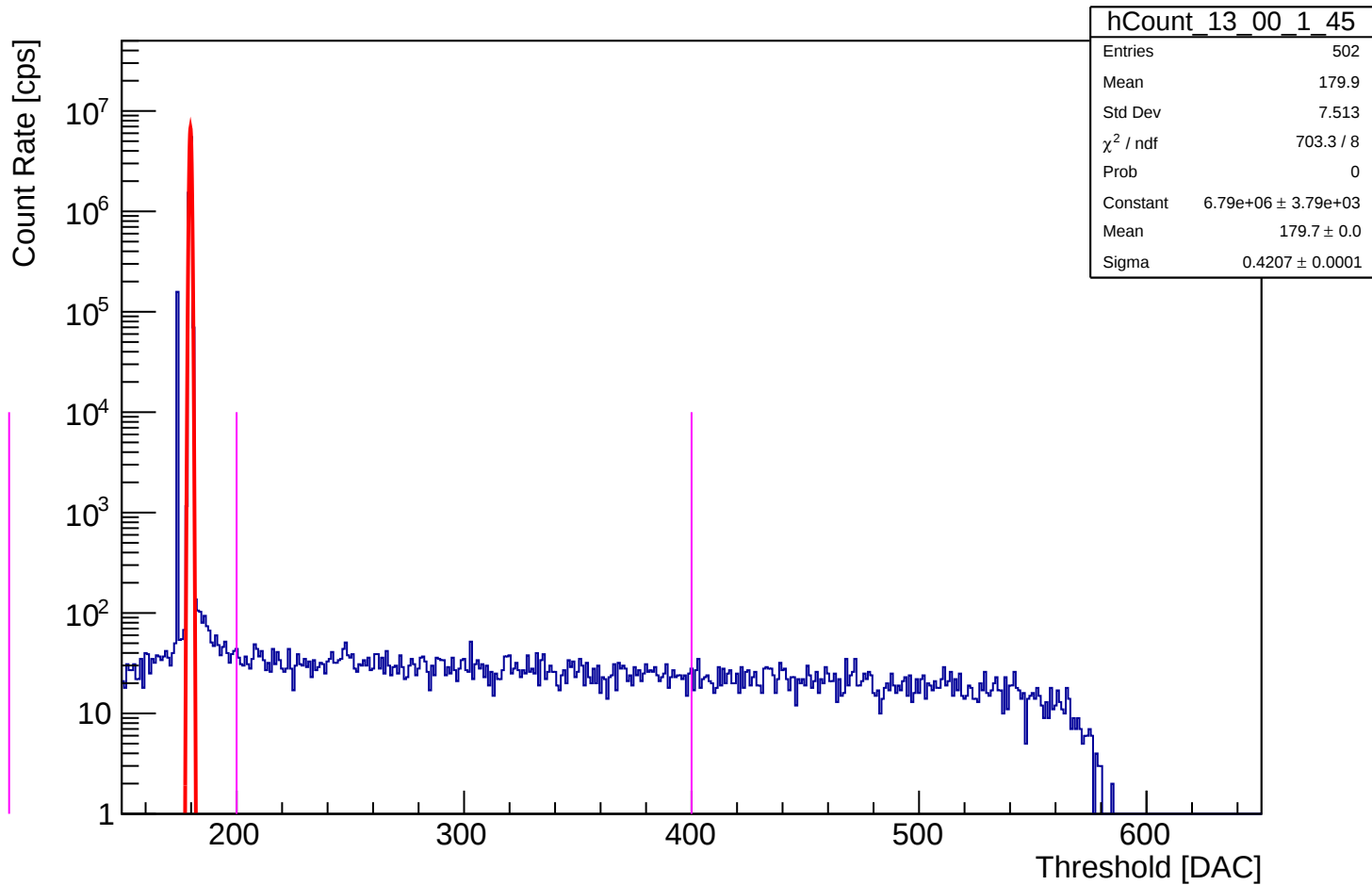
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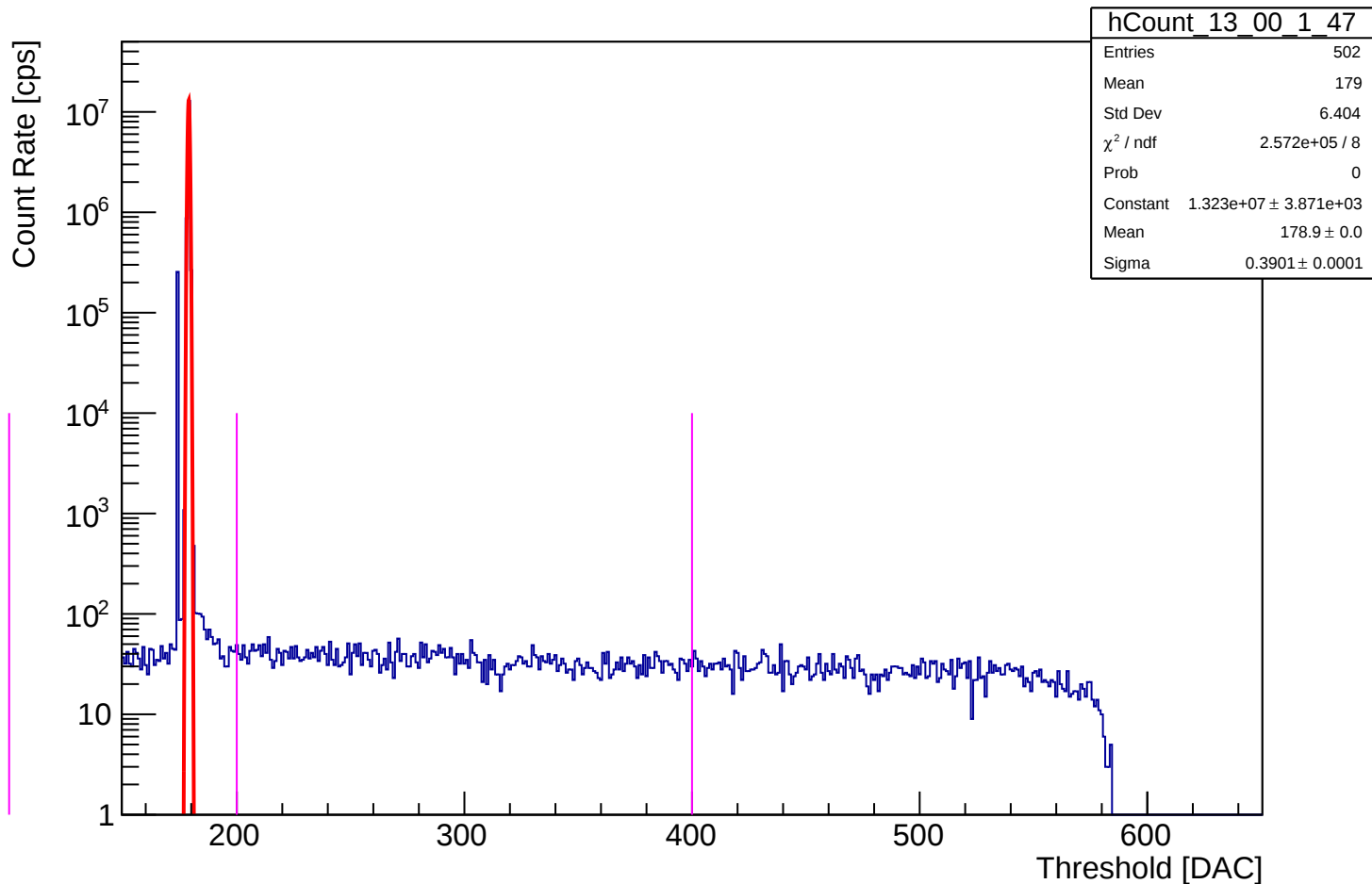
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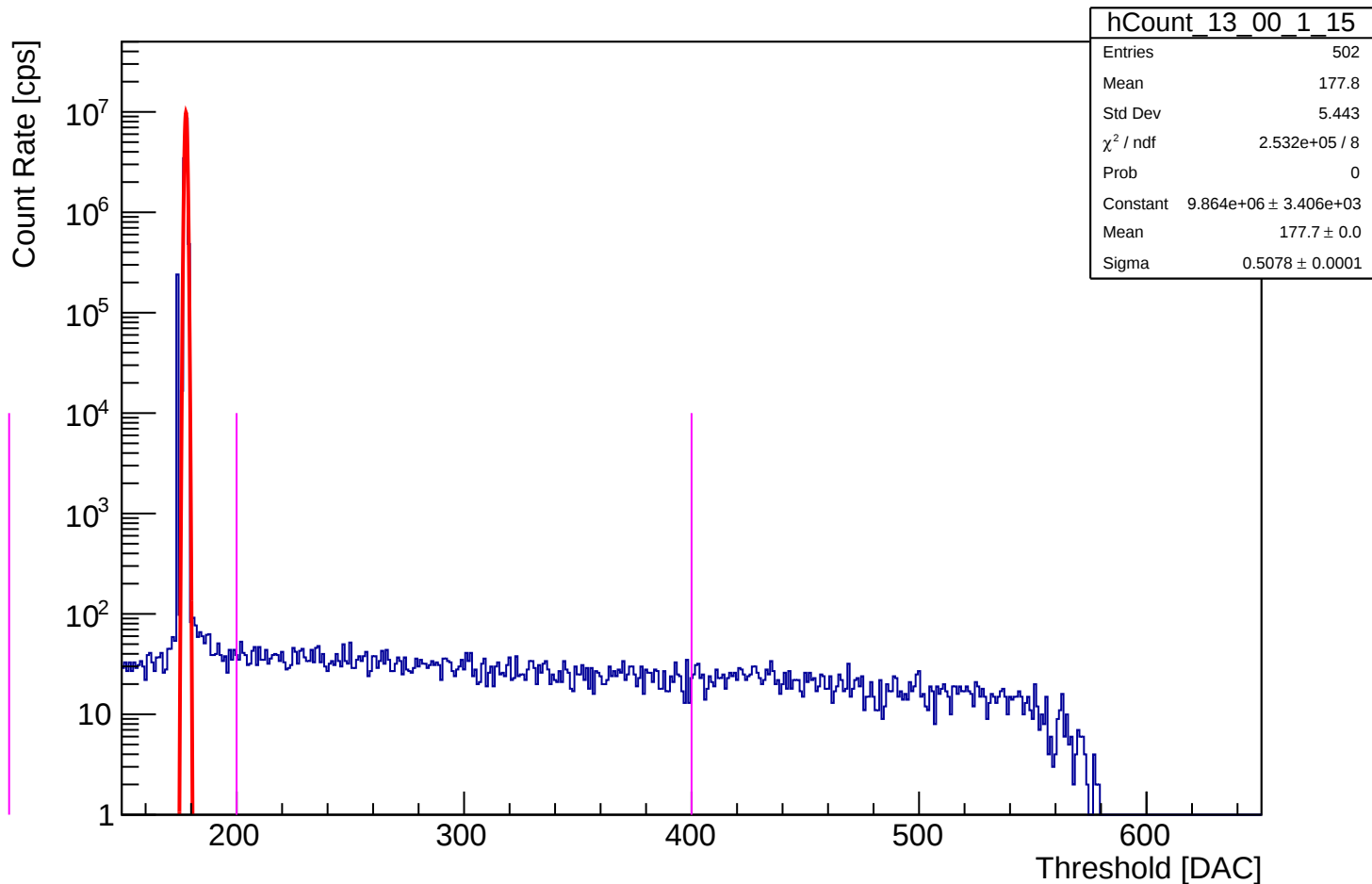
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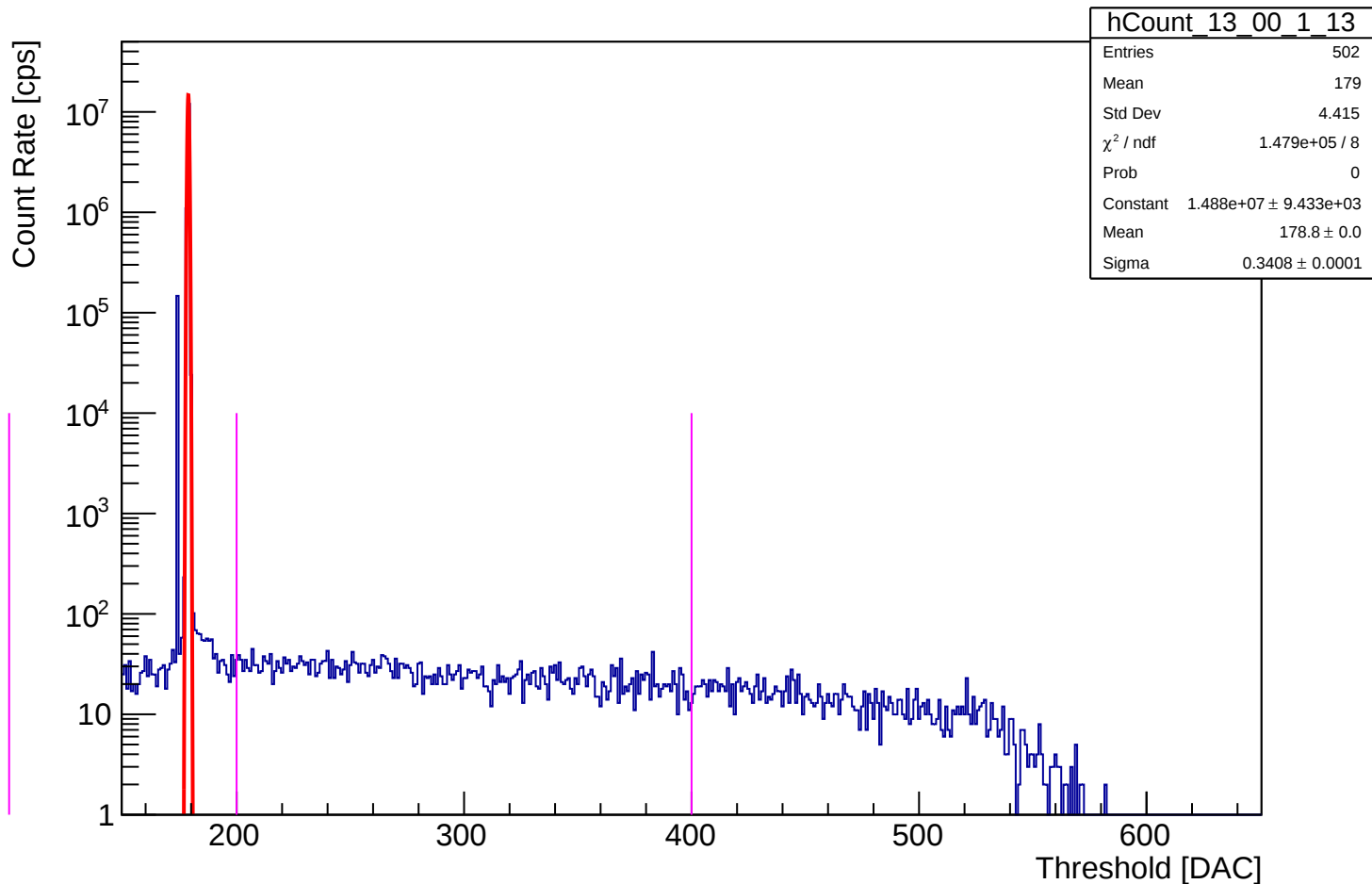
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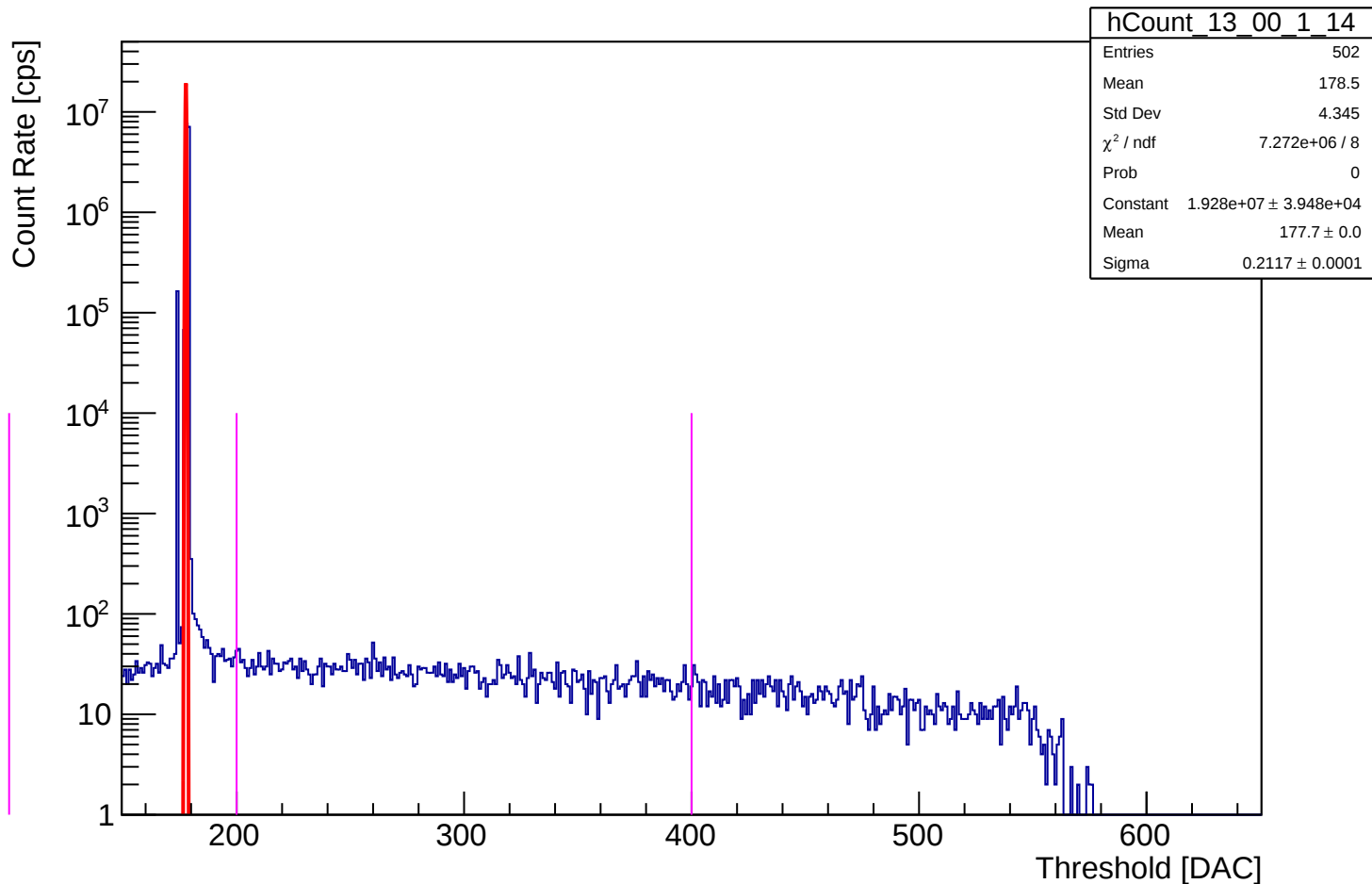
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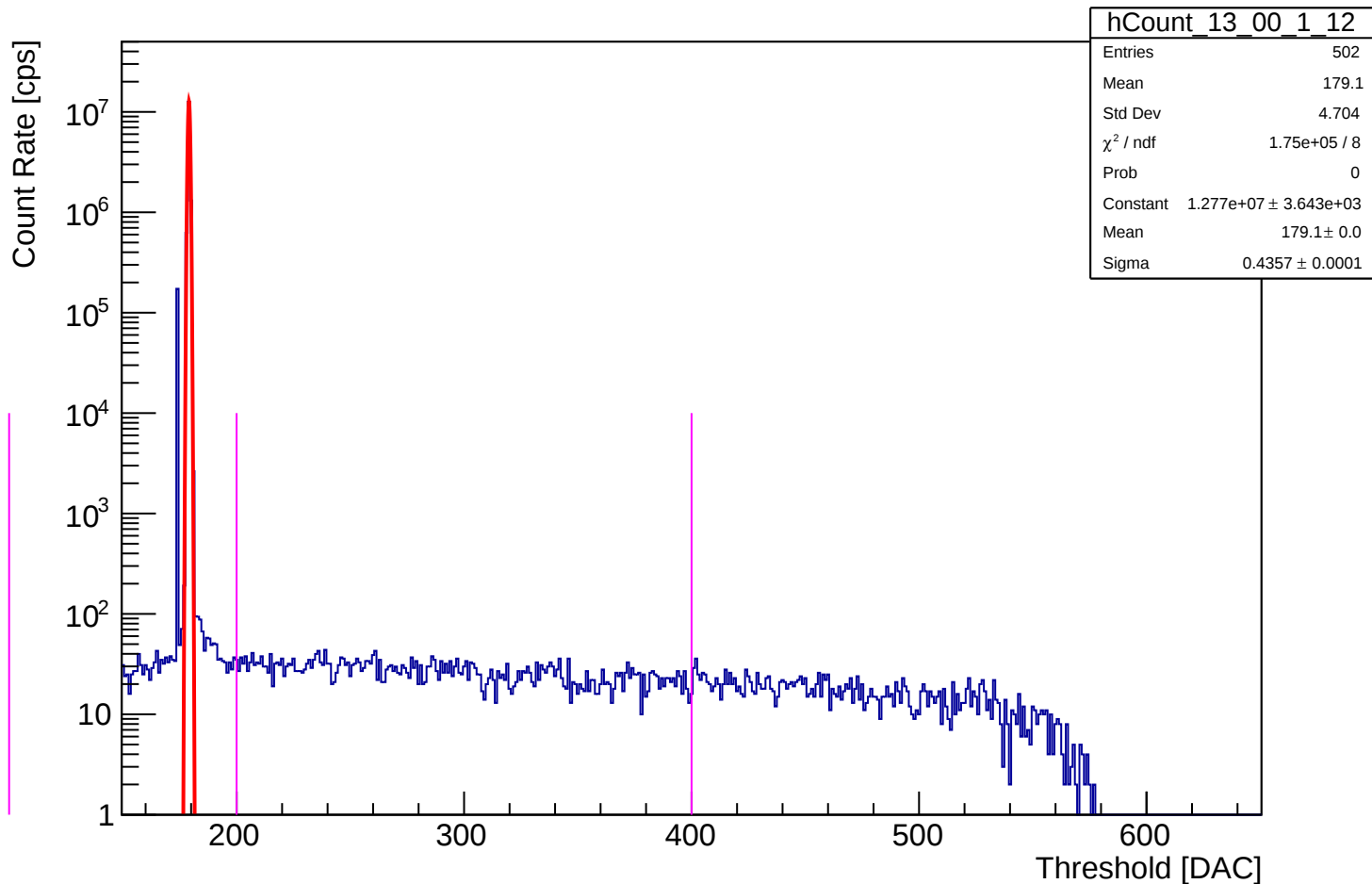
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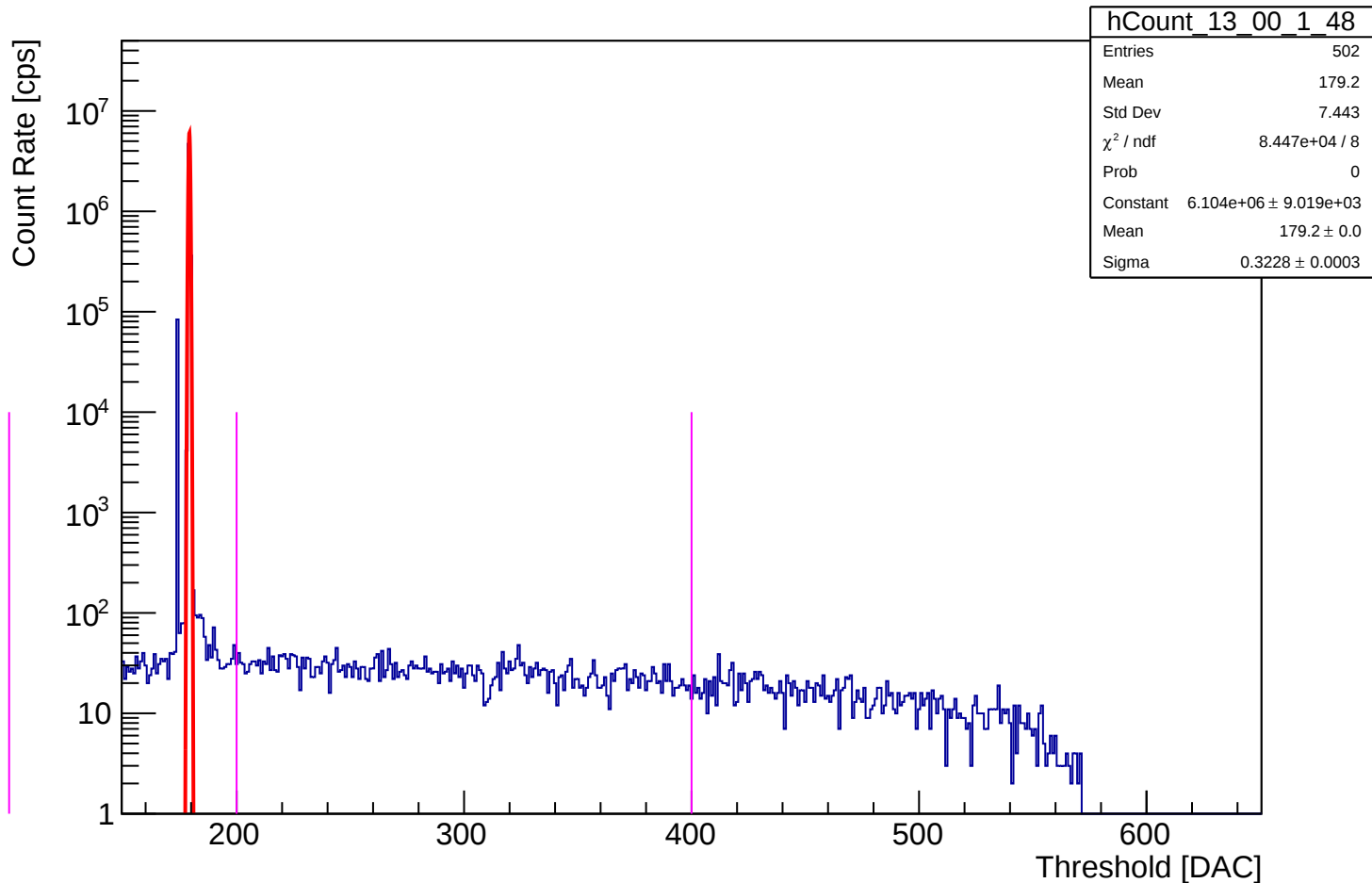
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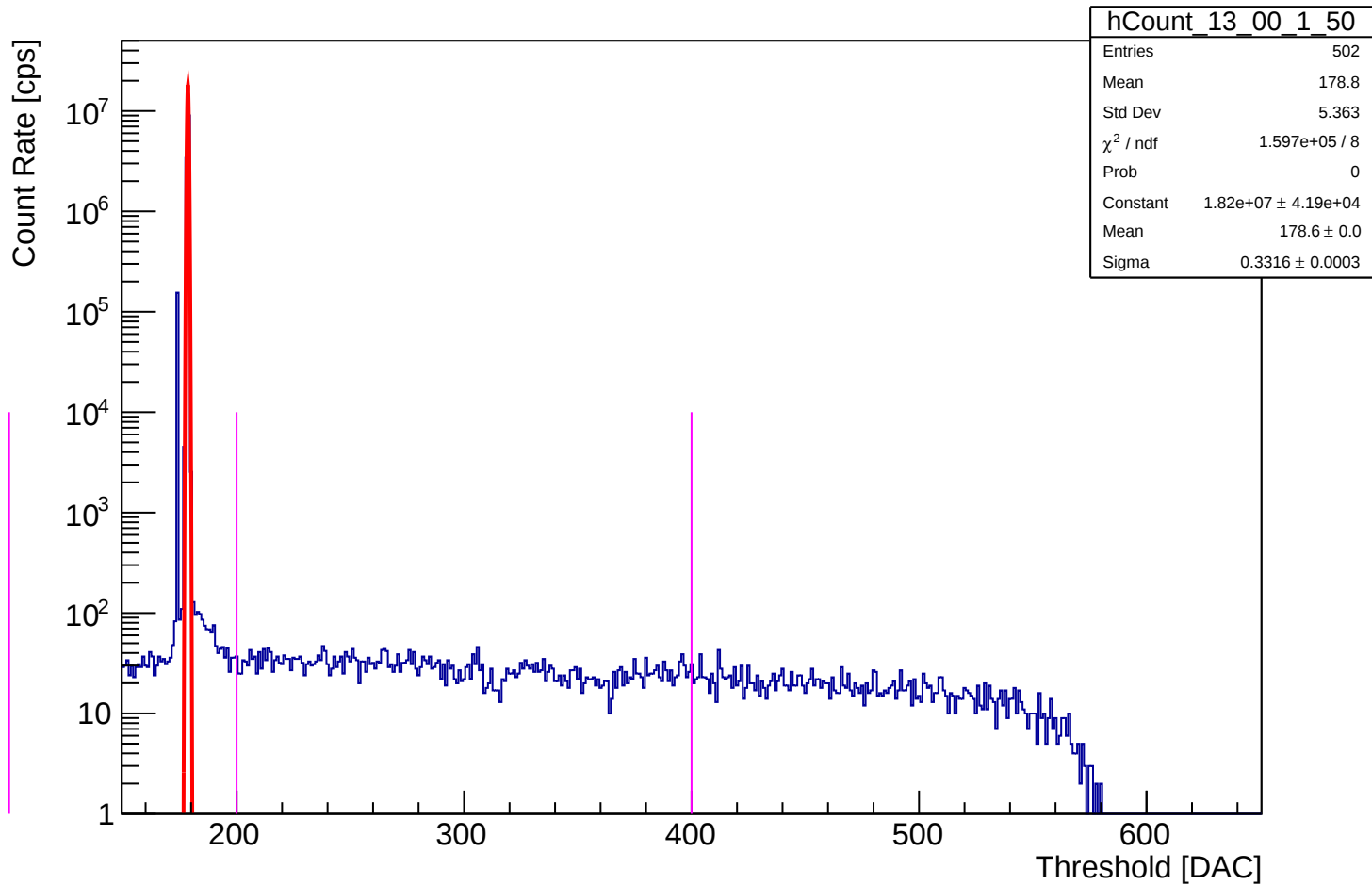
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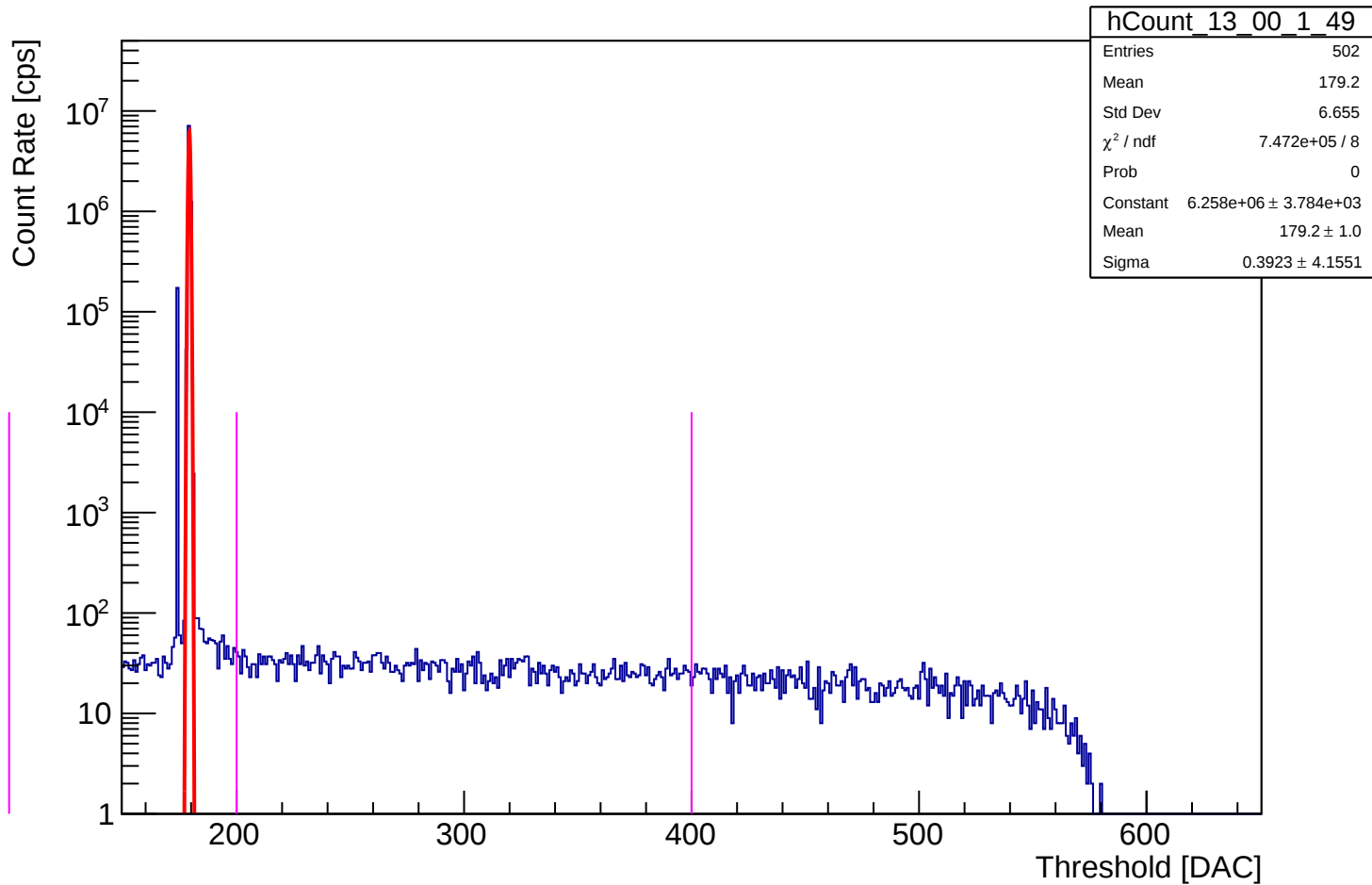
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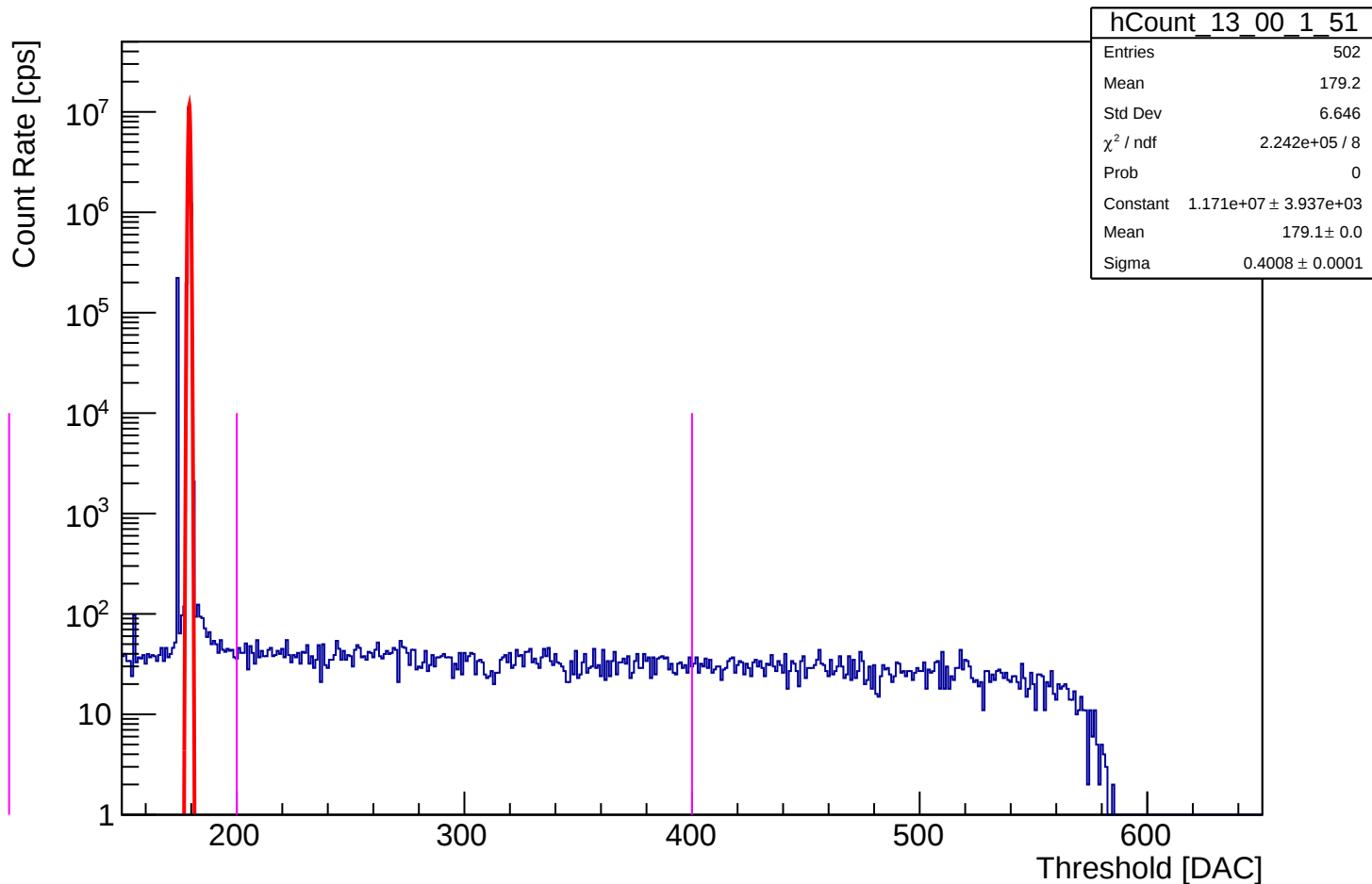
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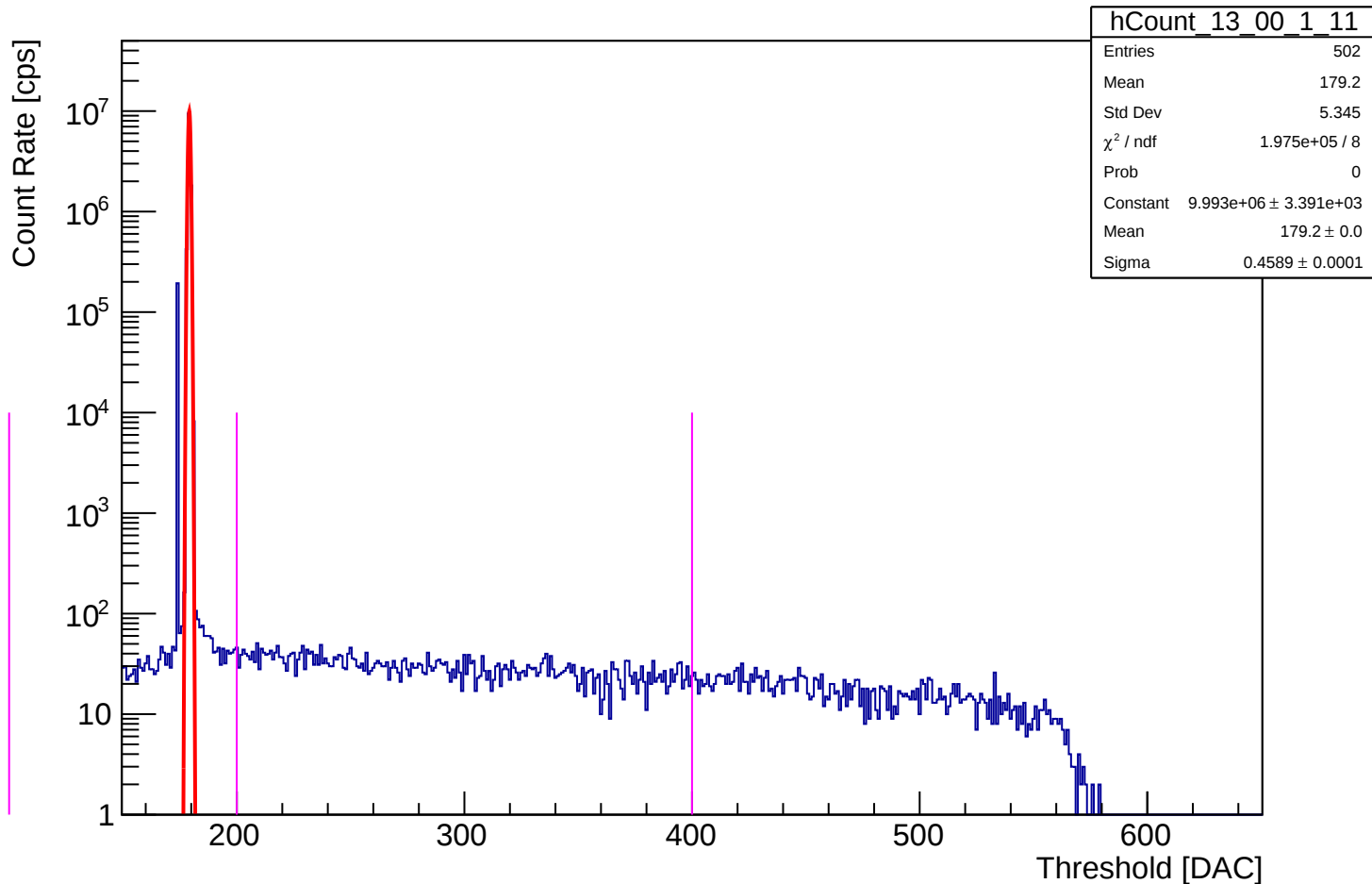
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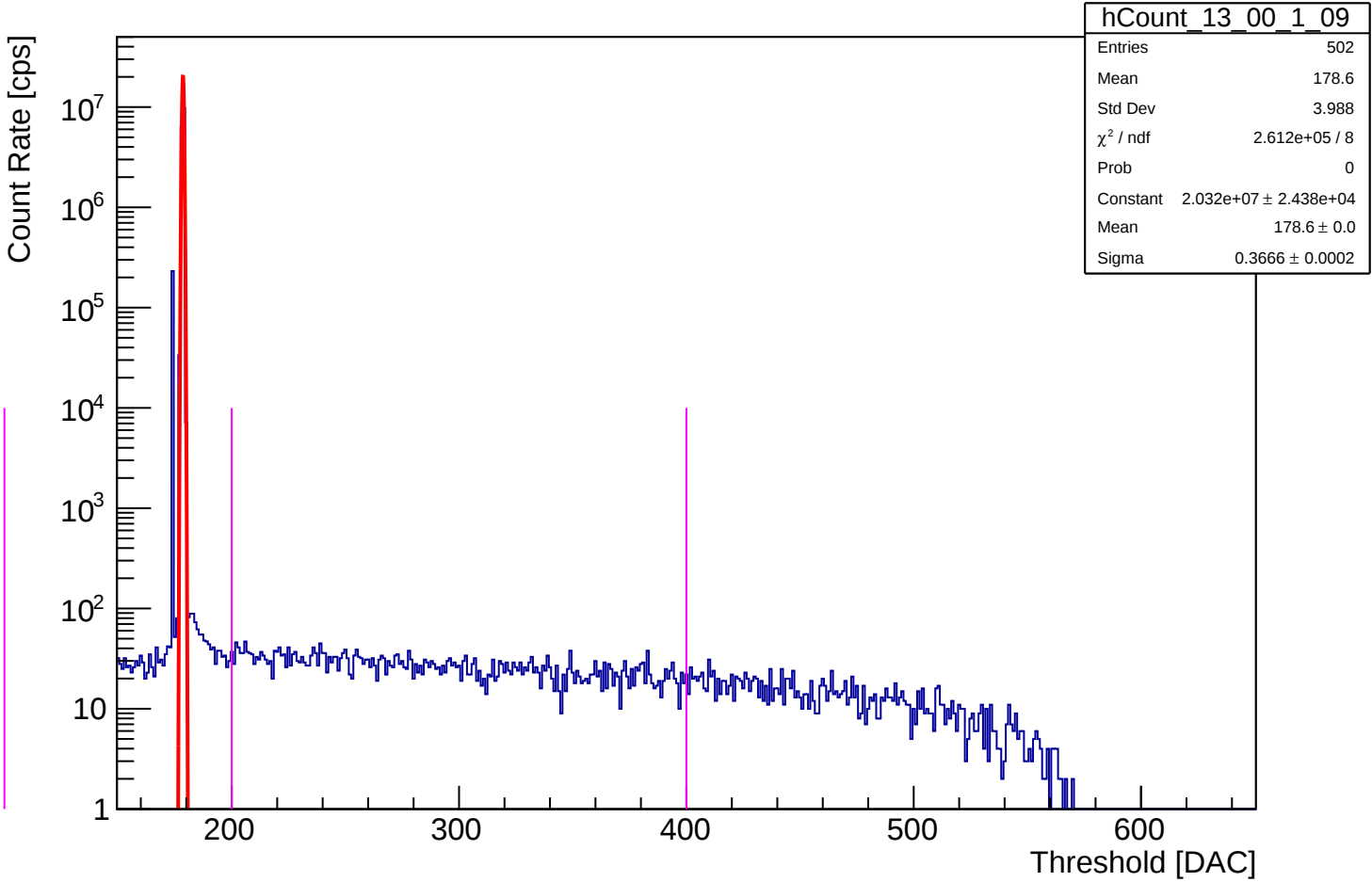


Row 1 Tile 1 Pmt 2 Pixel 40 Slot 13 Fiber 0 Asic 1 Channel 51

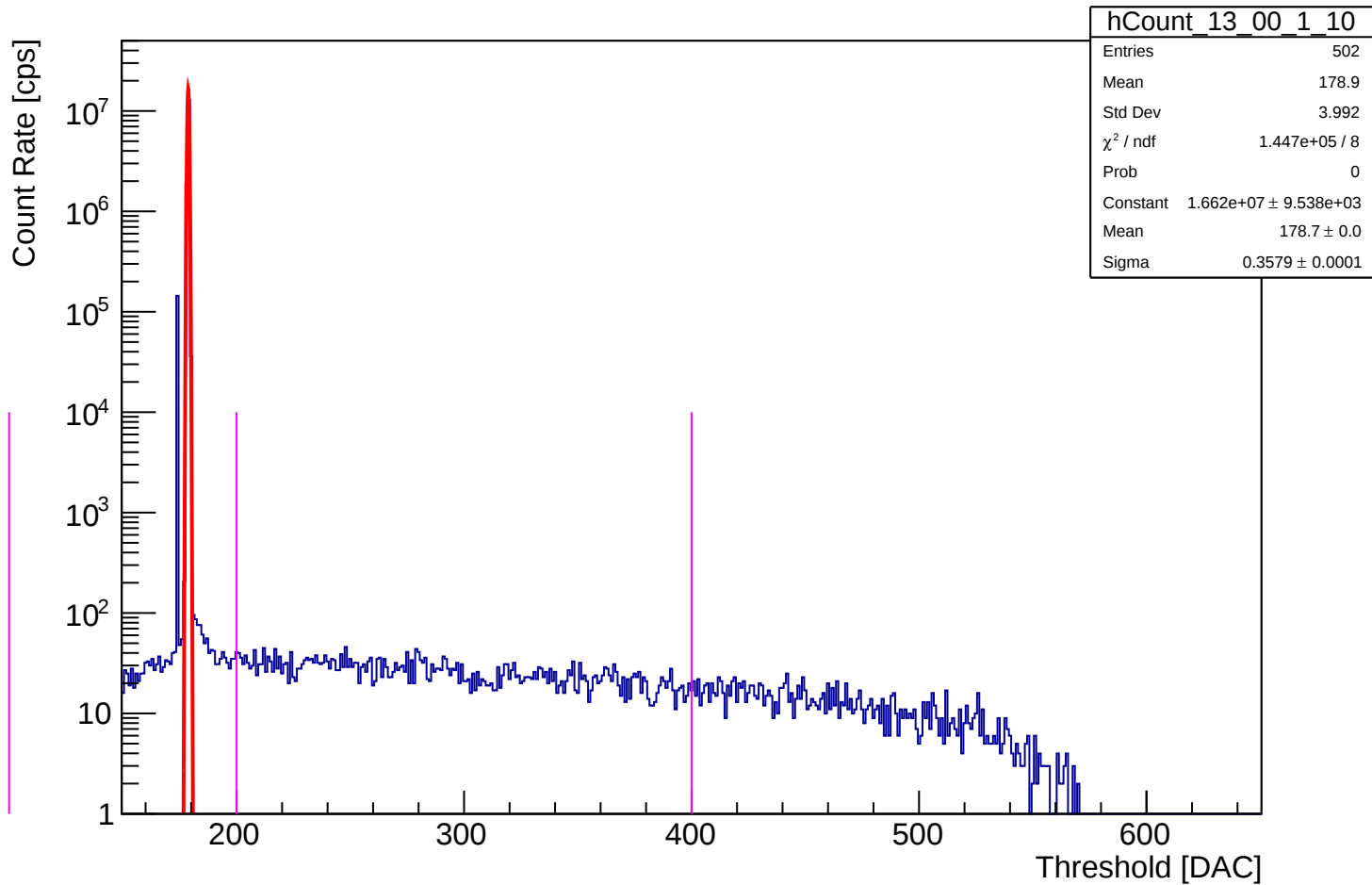


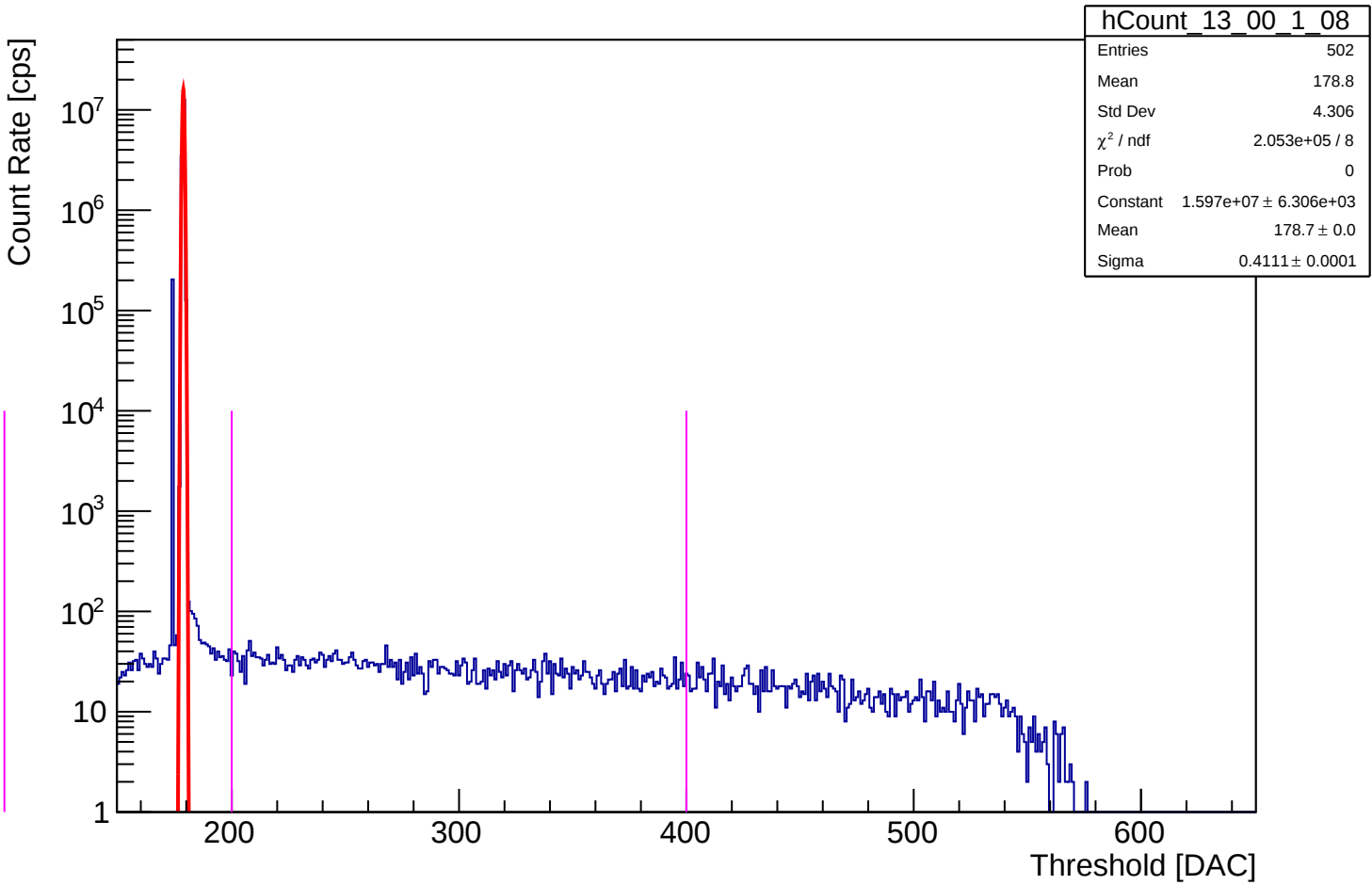
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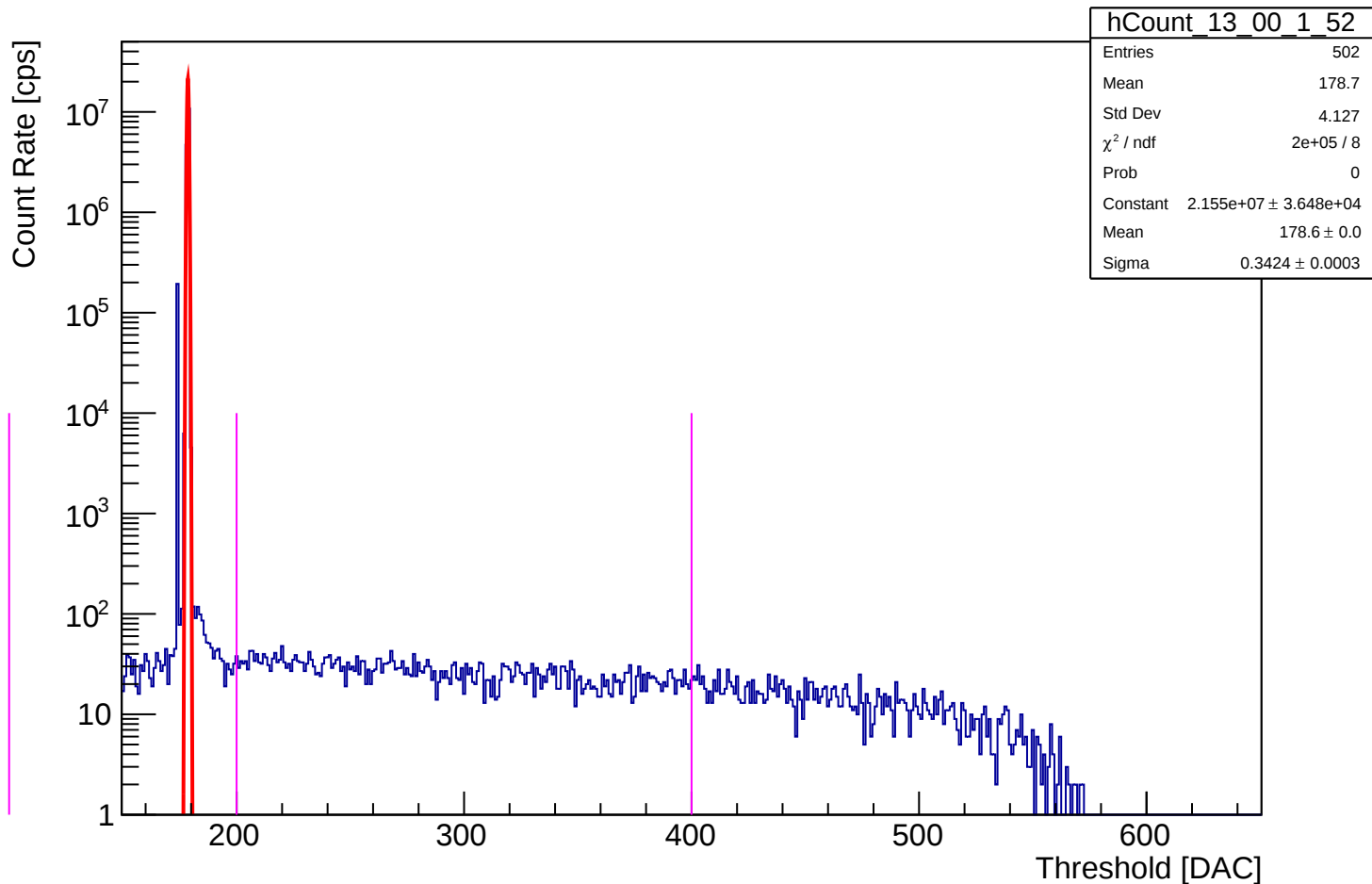


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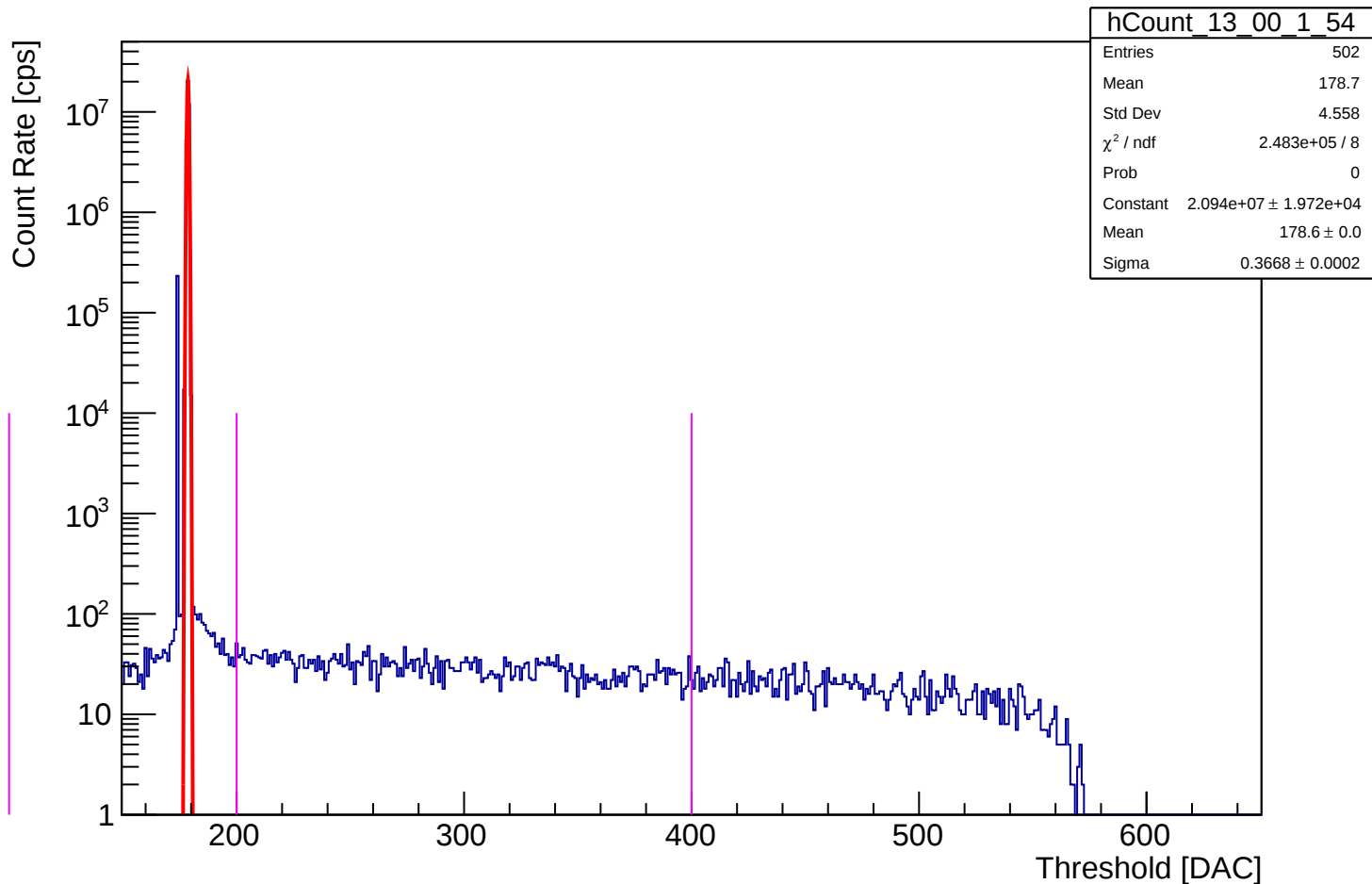




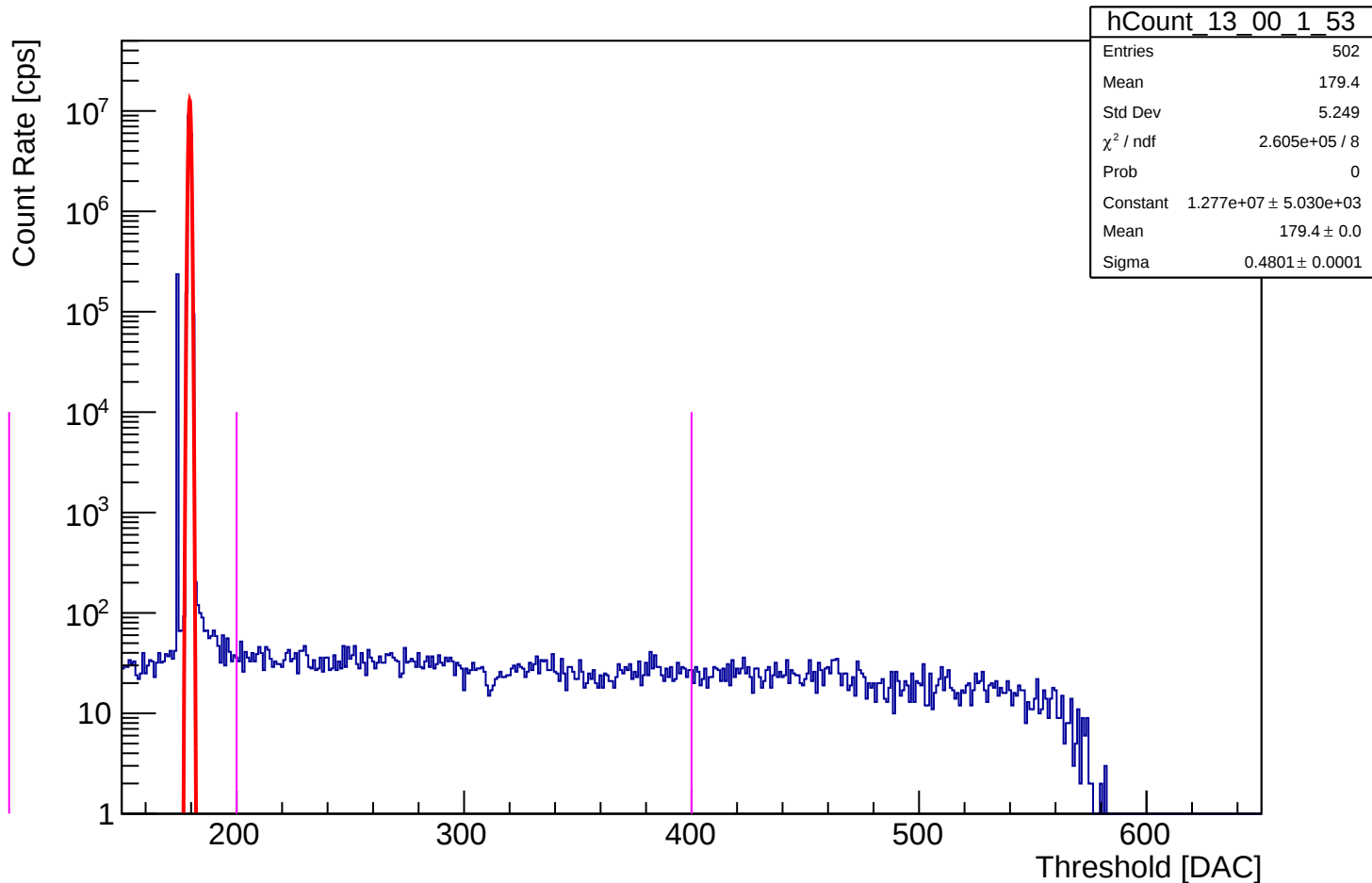
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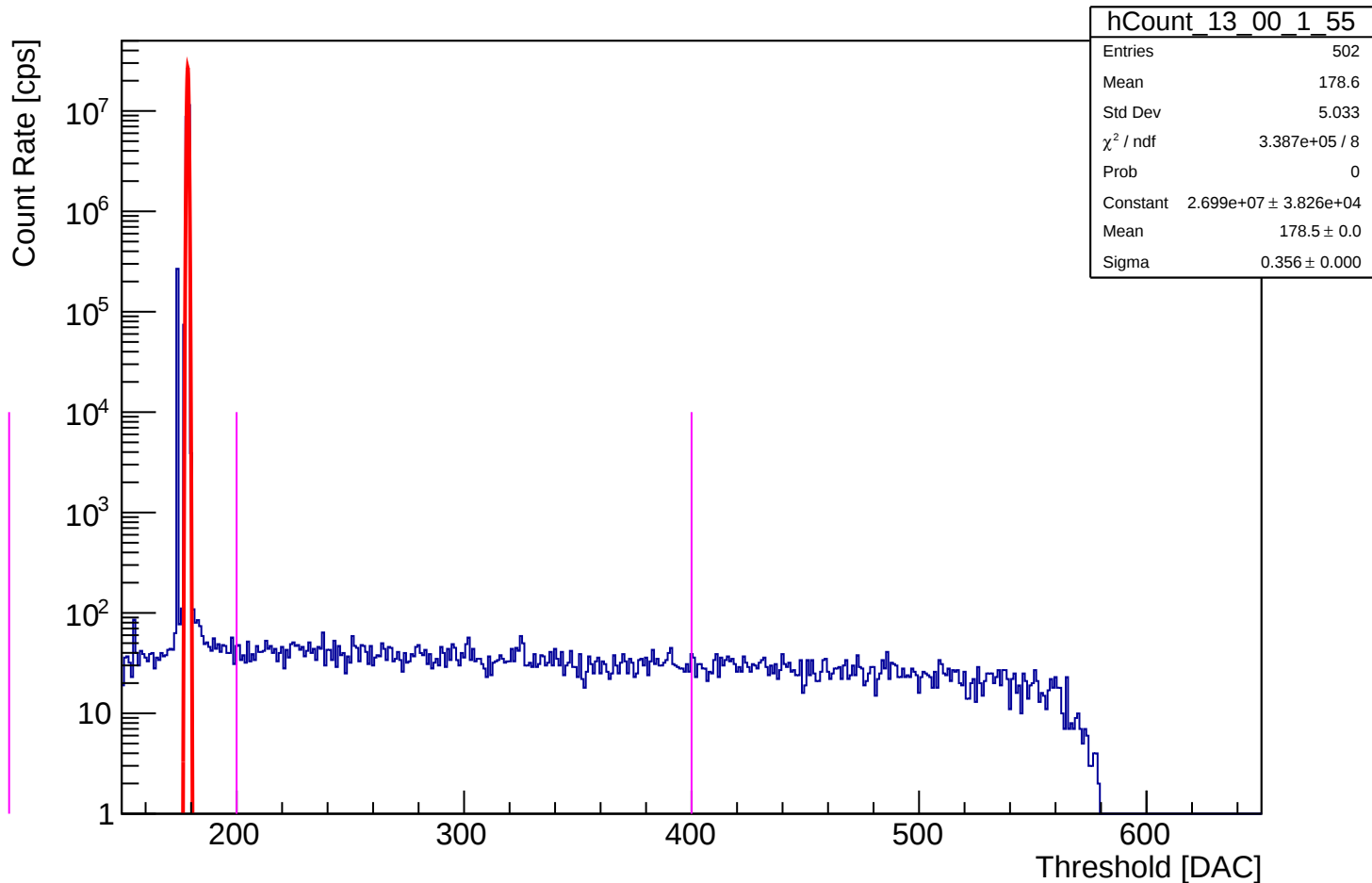
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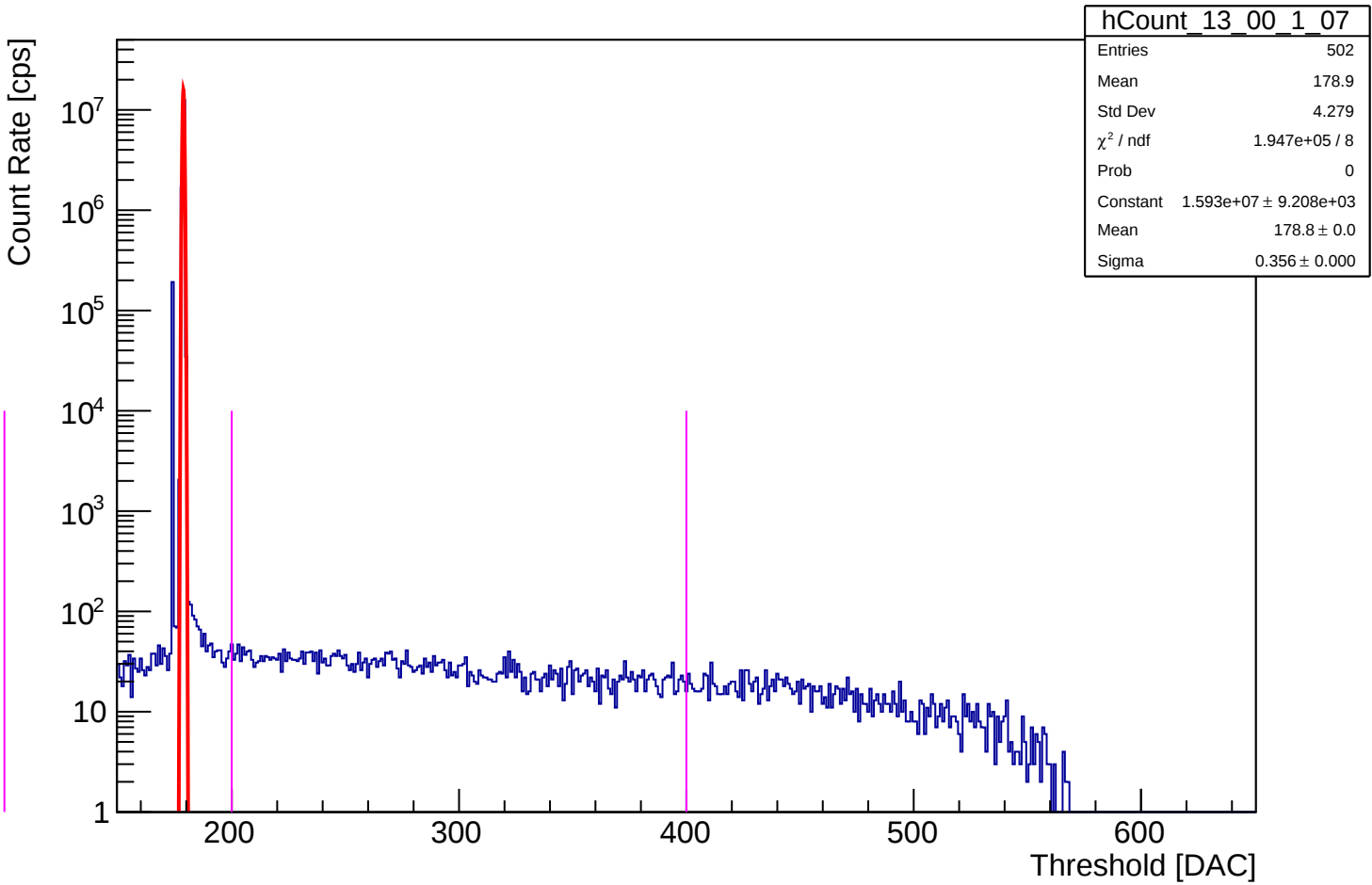


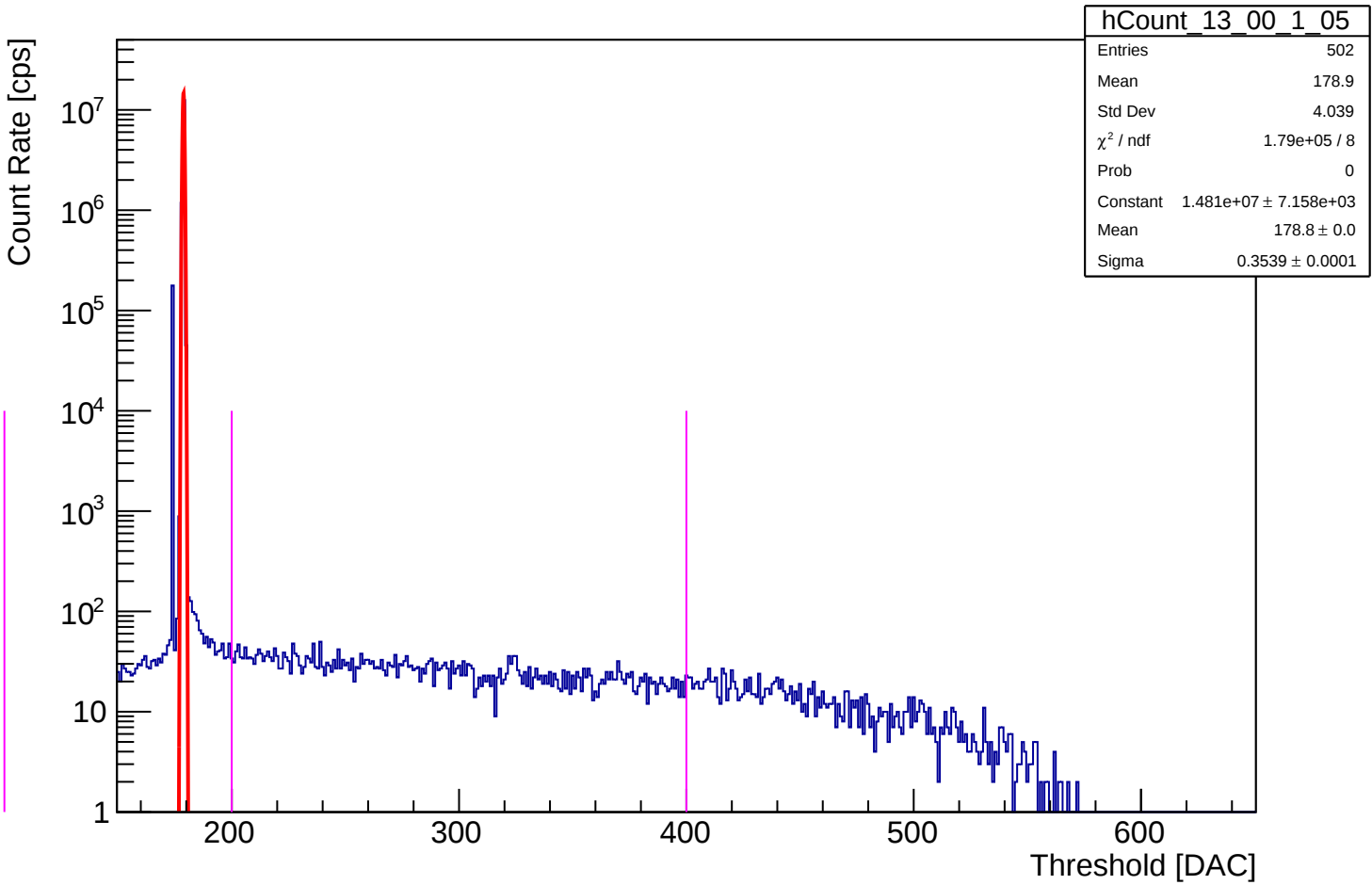
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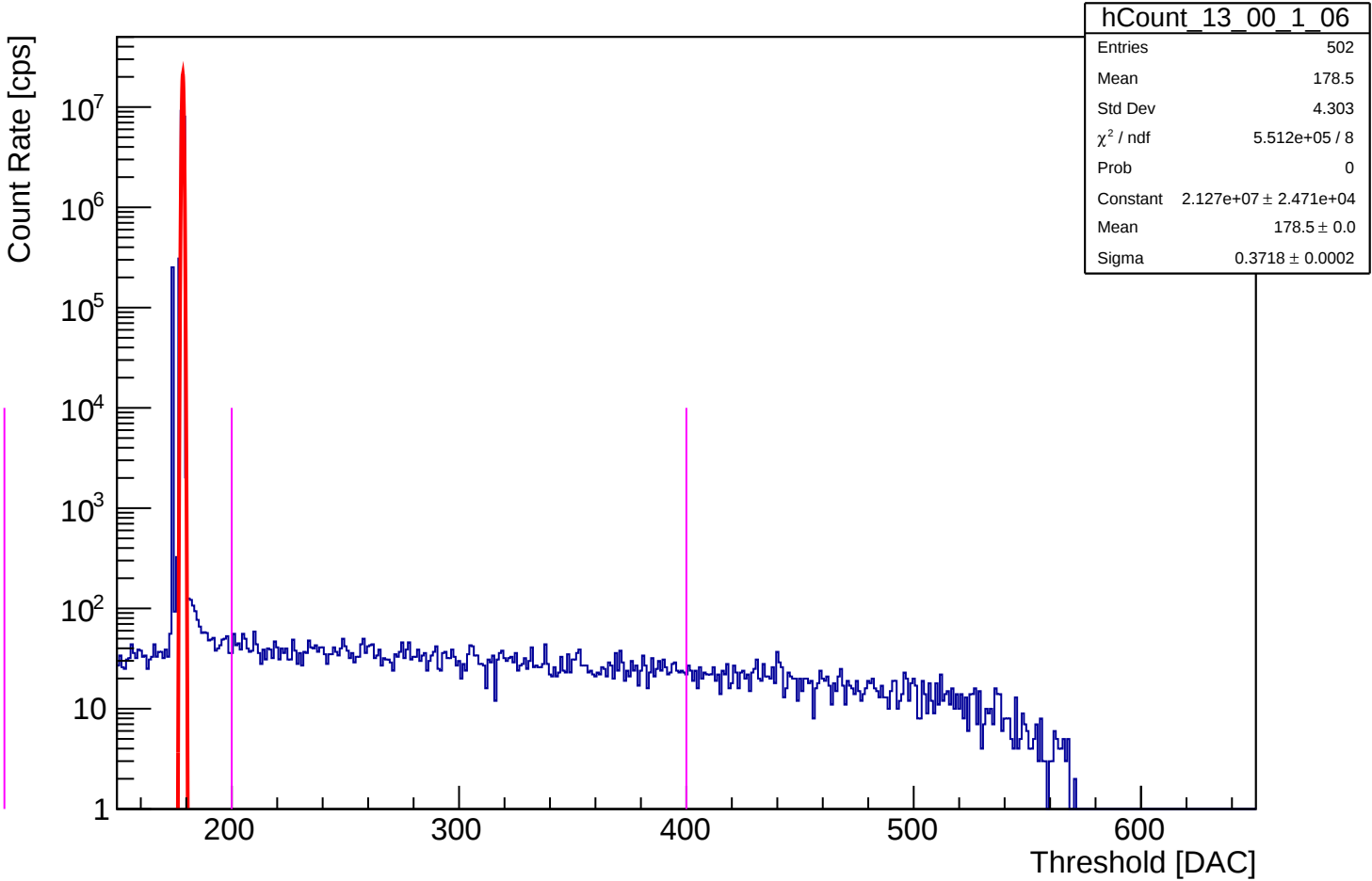


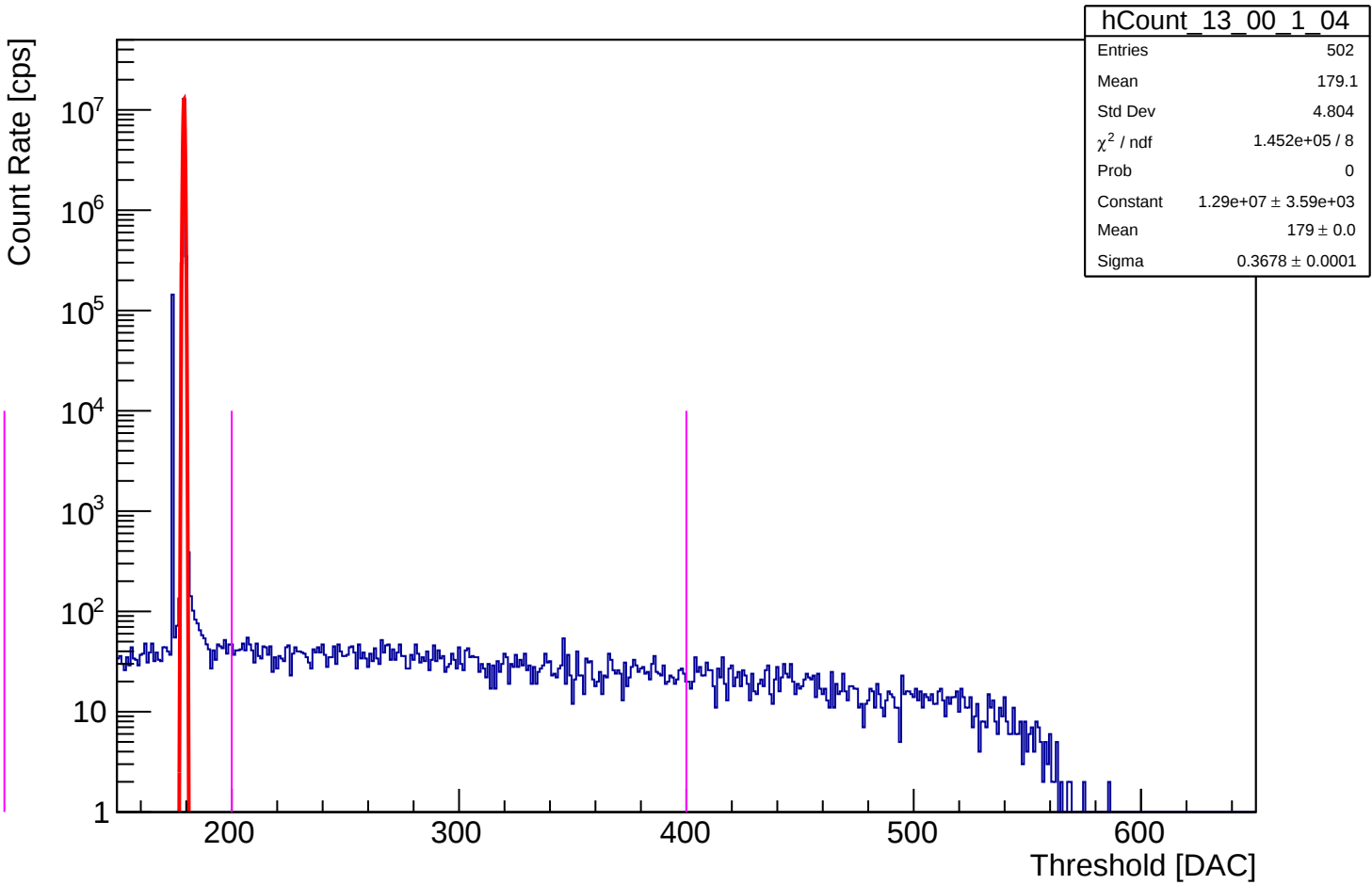
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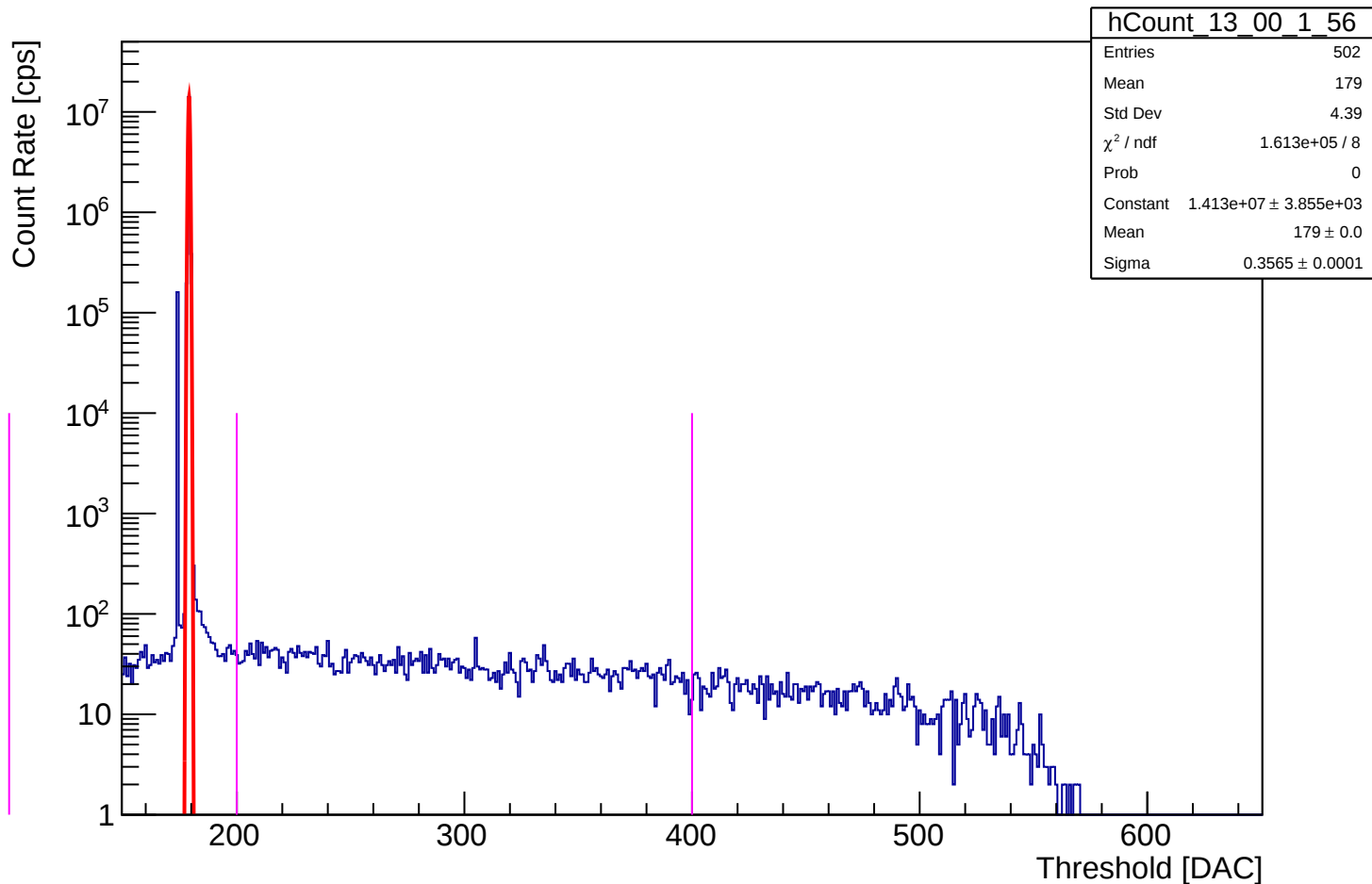




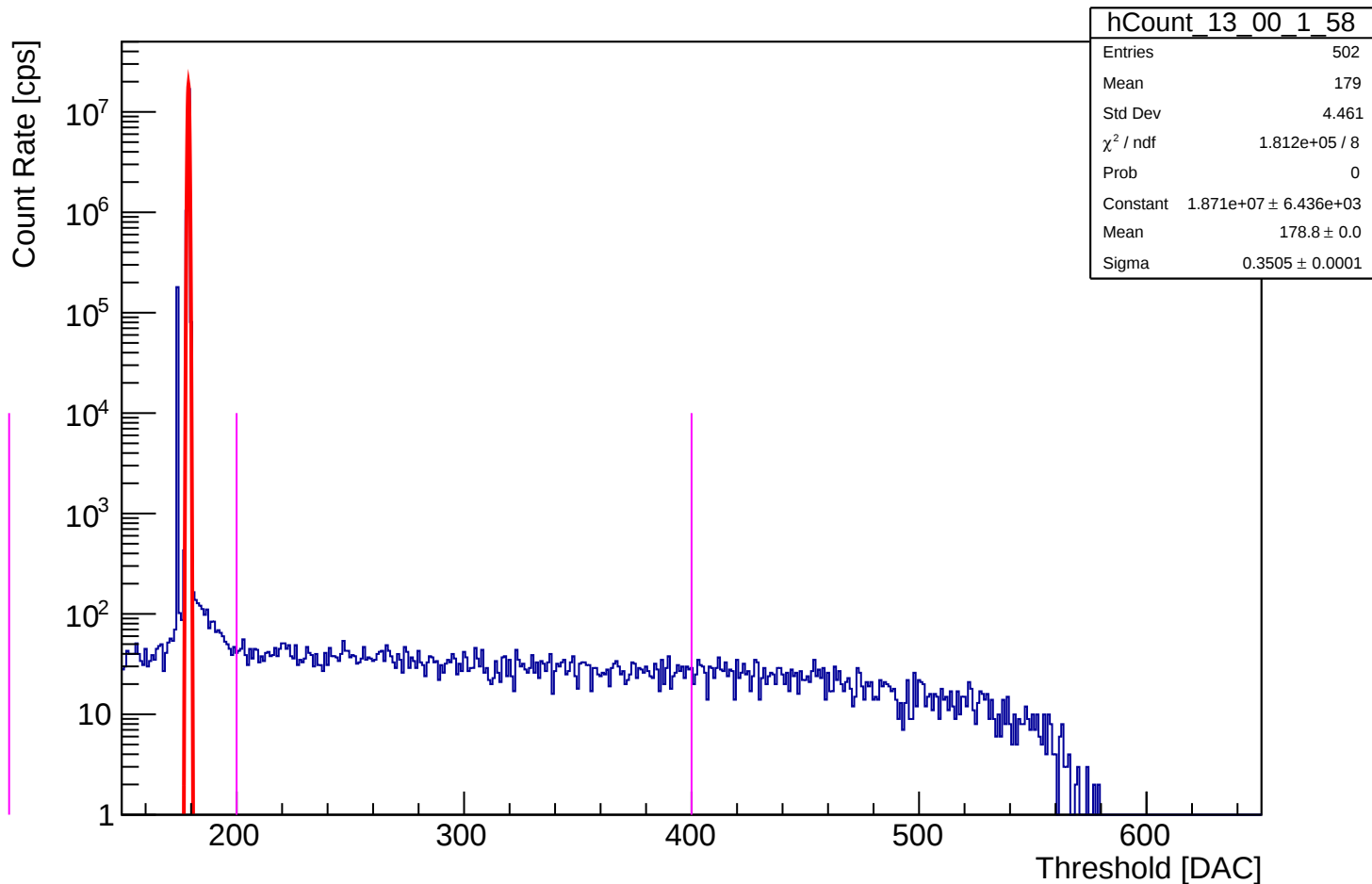




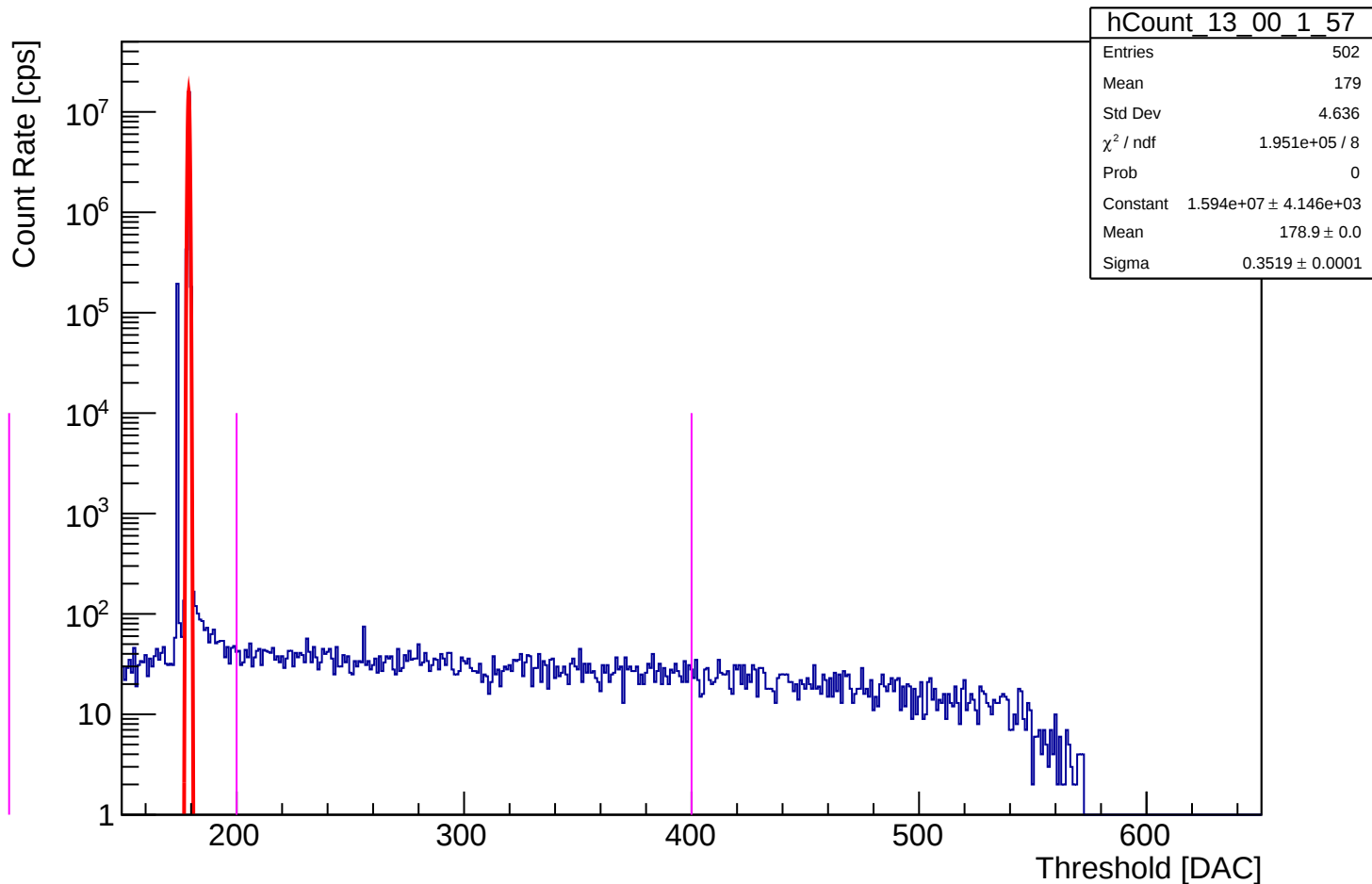
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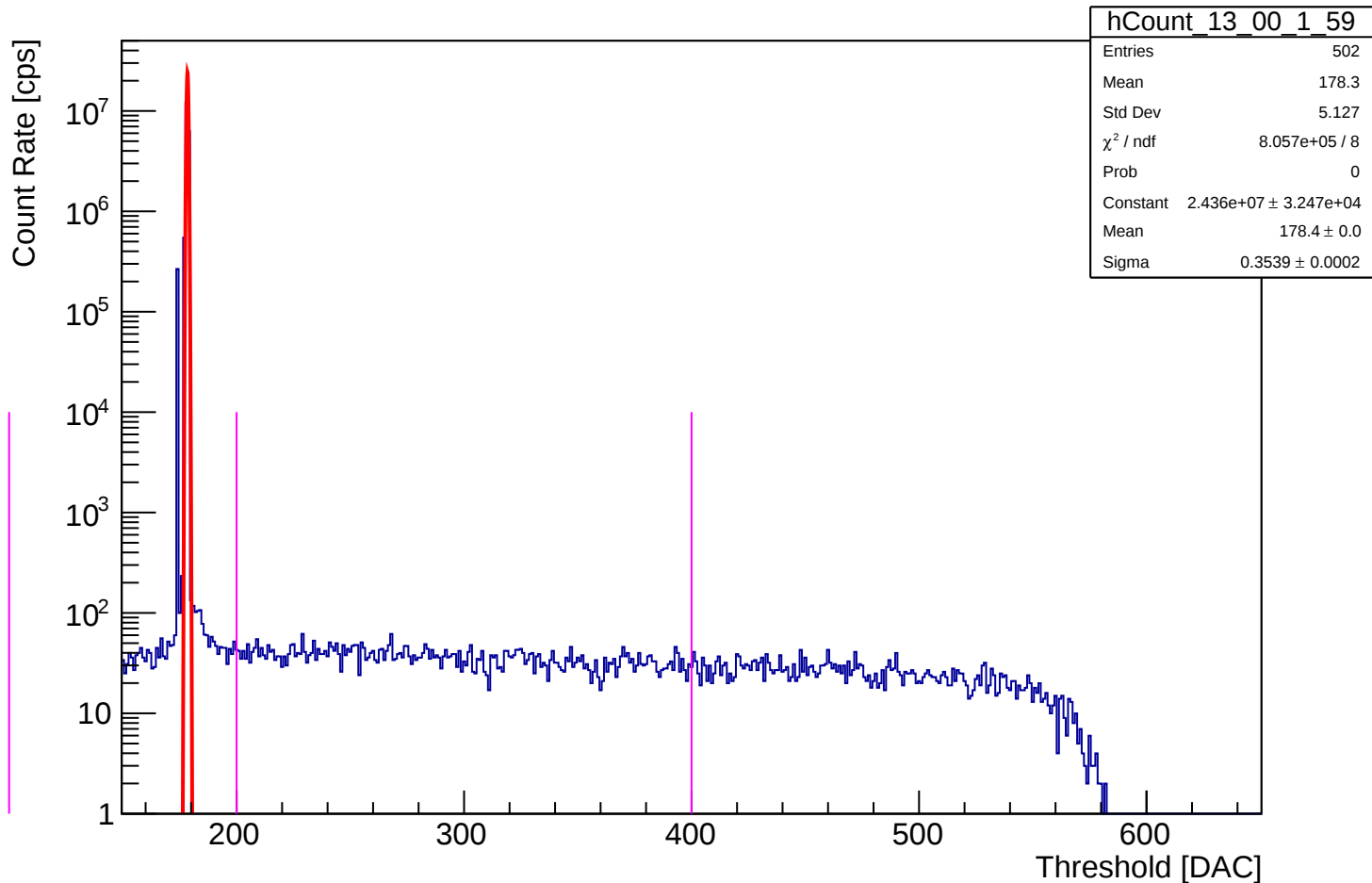
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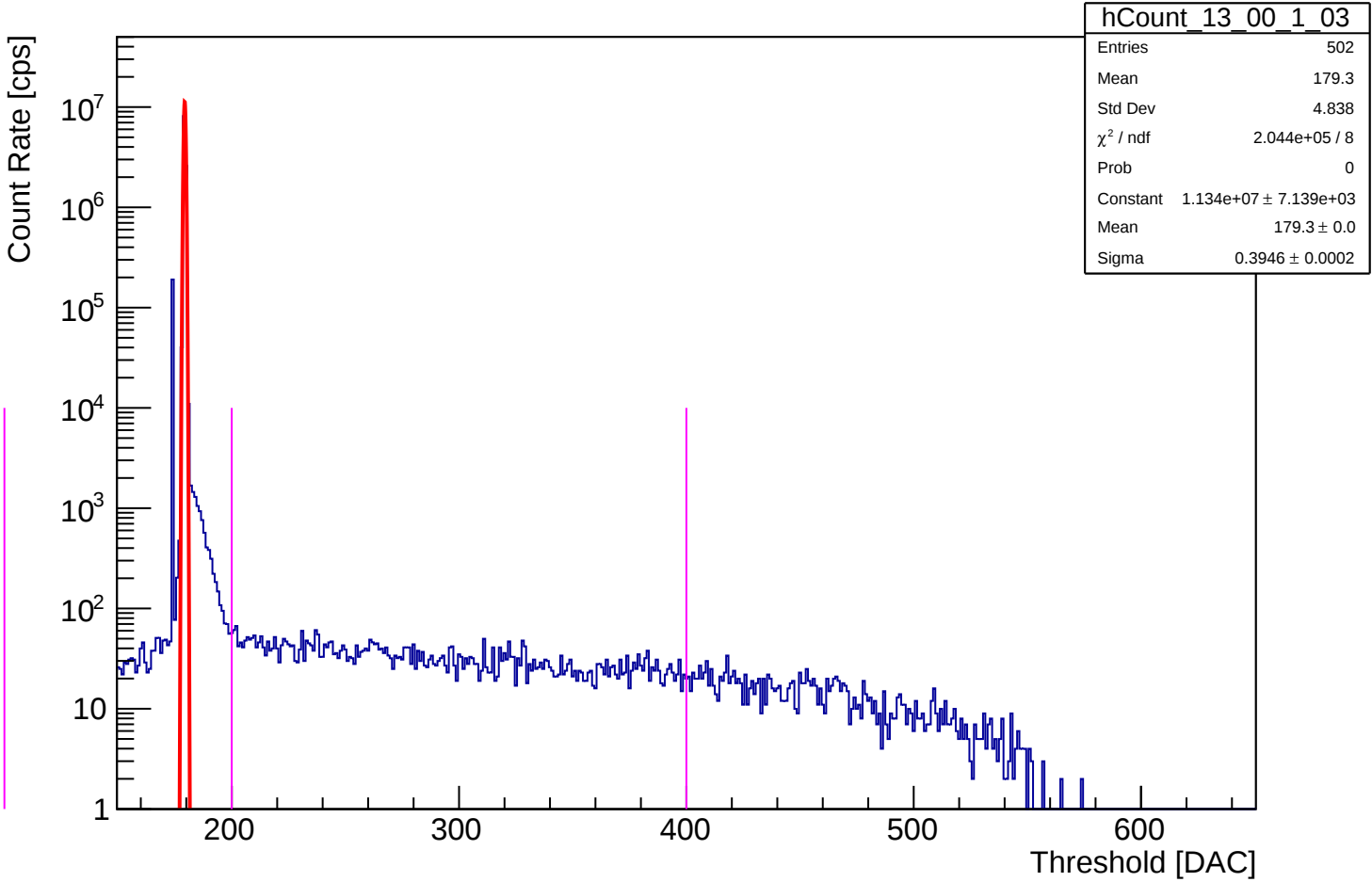


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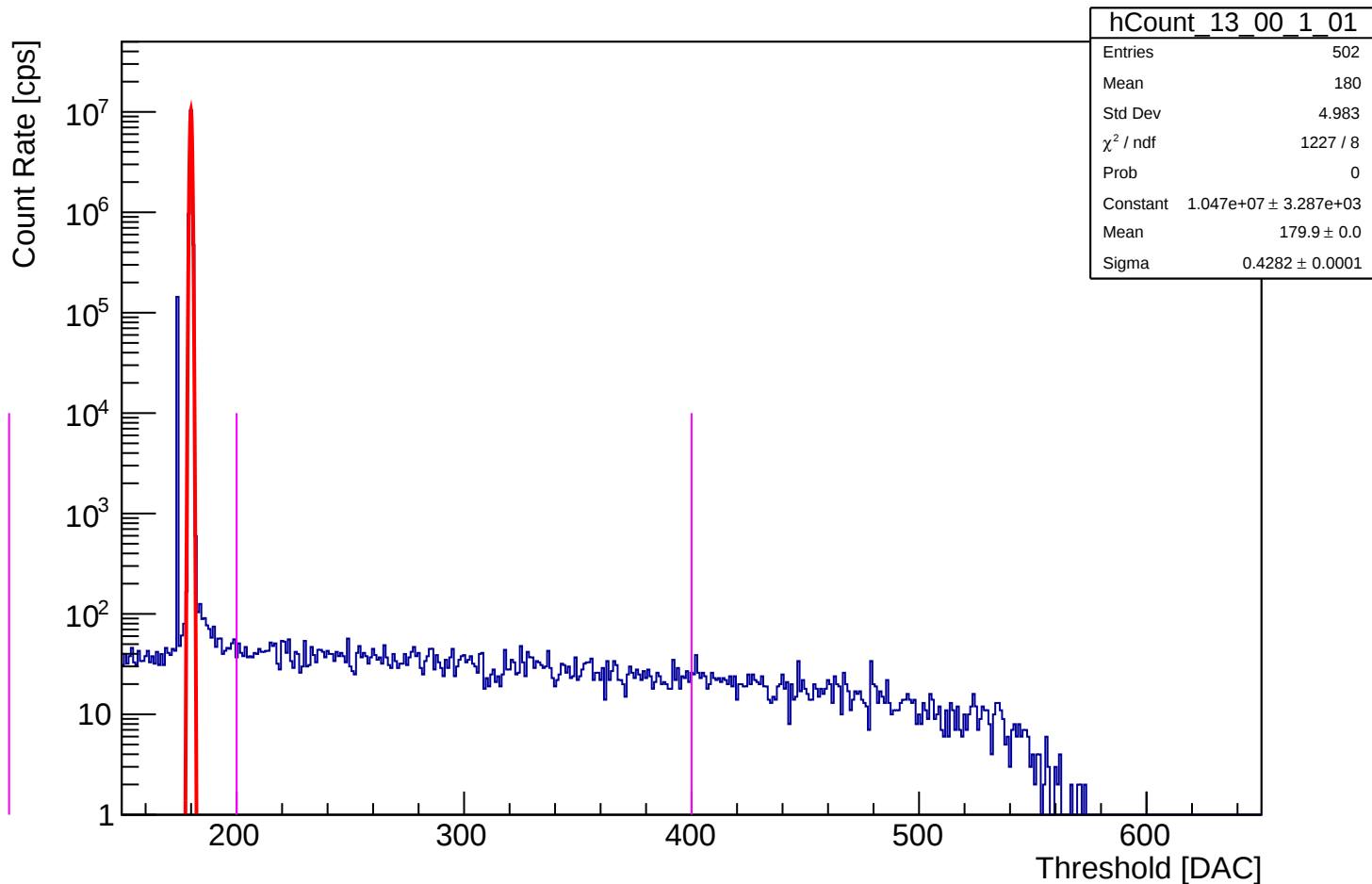


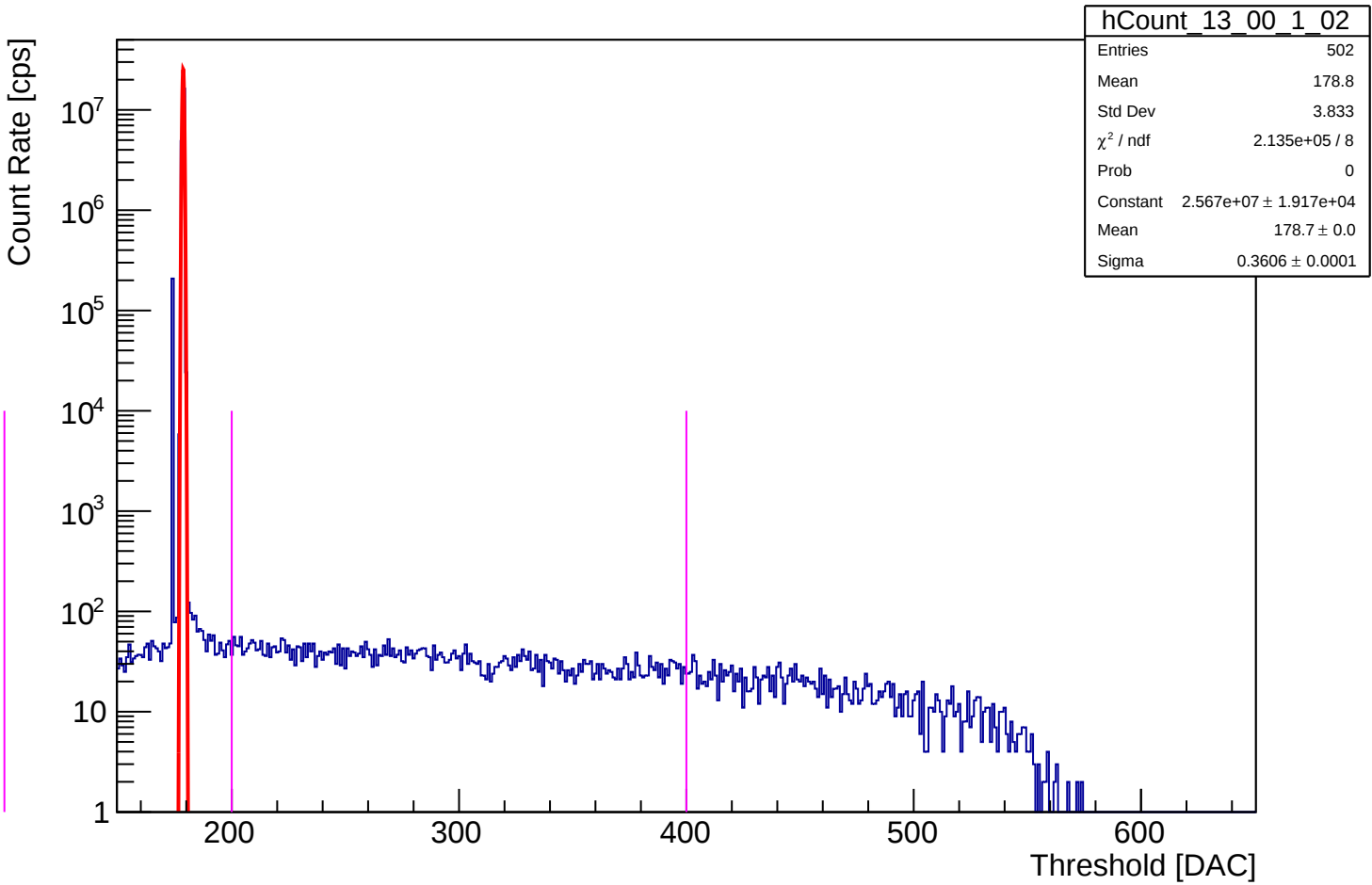
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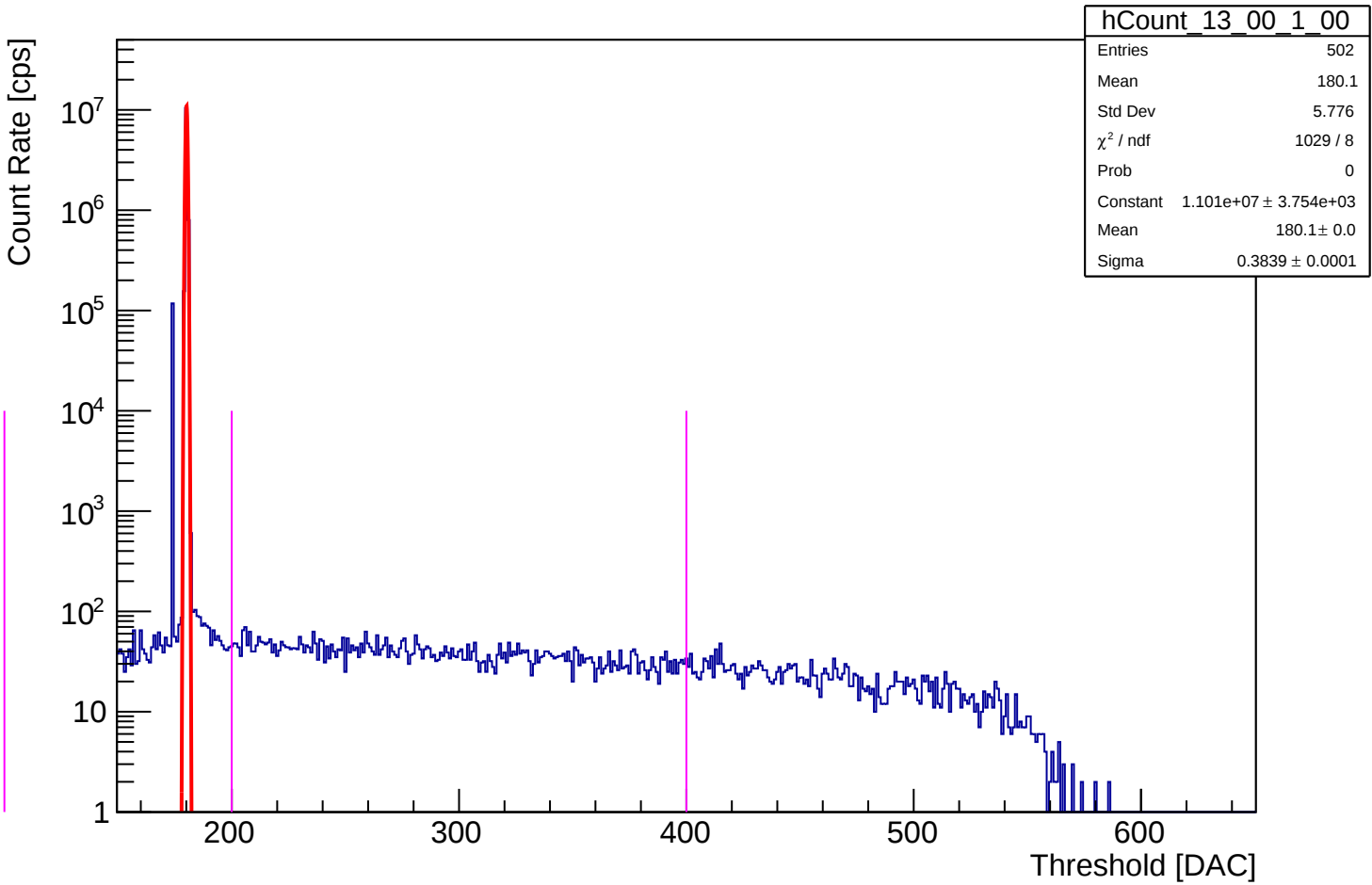




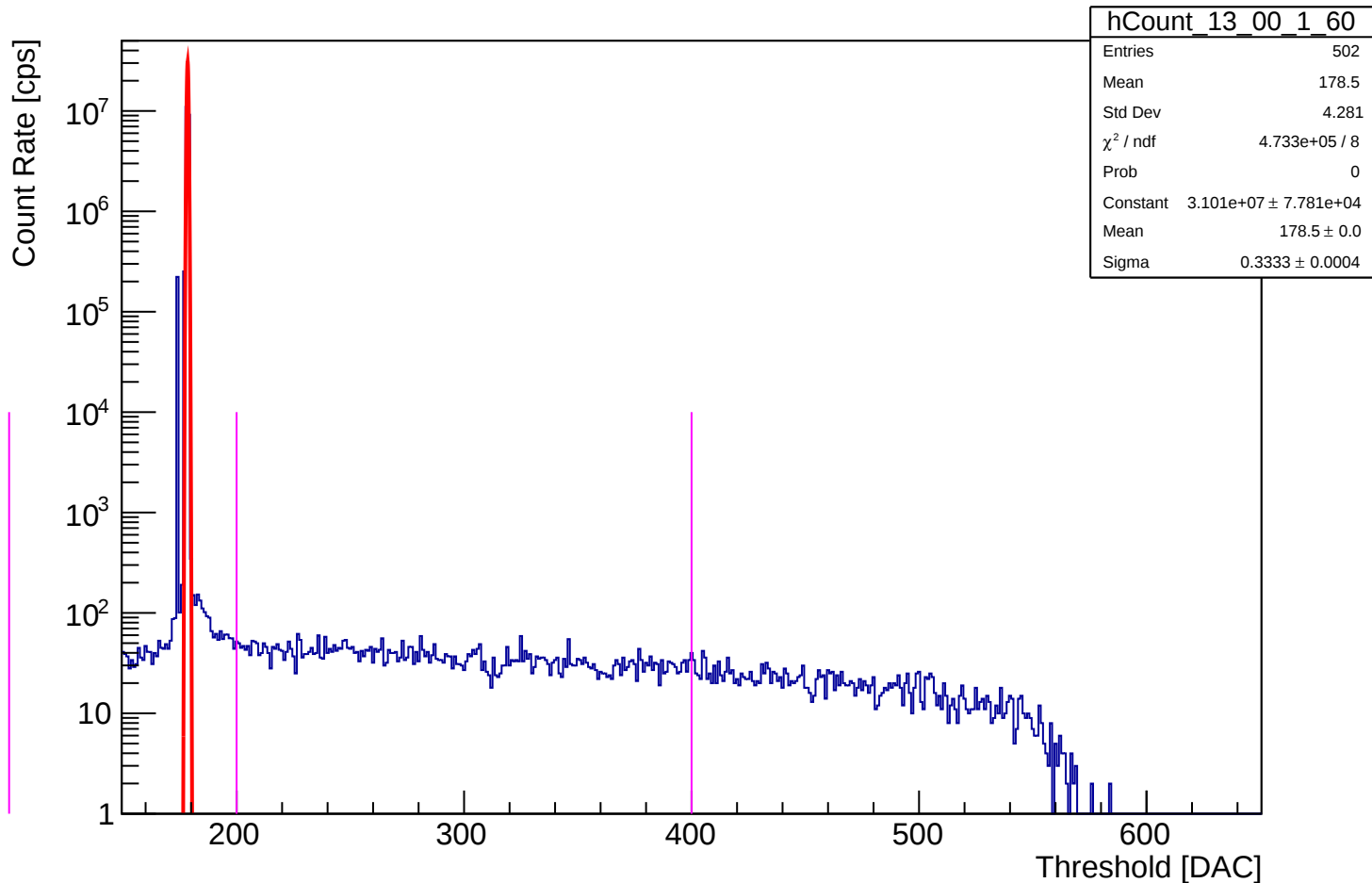
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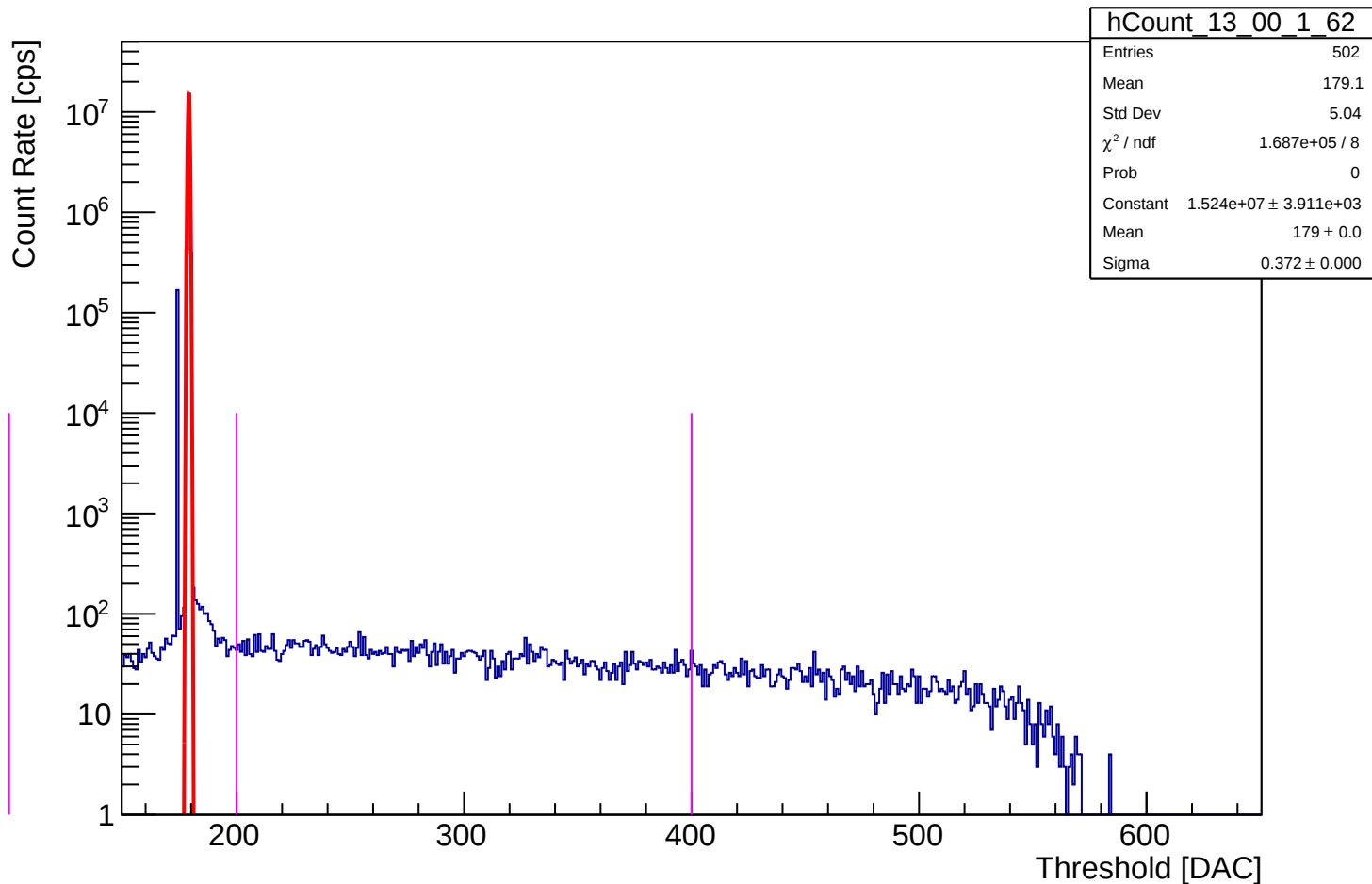




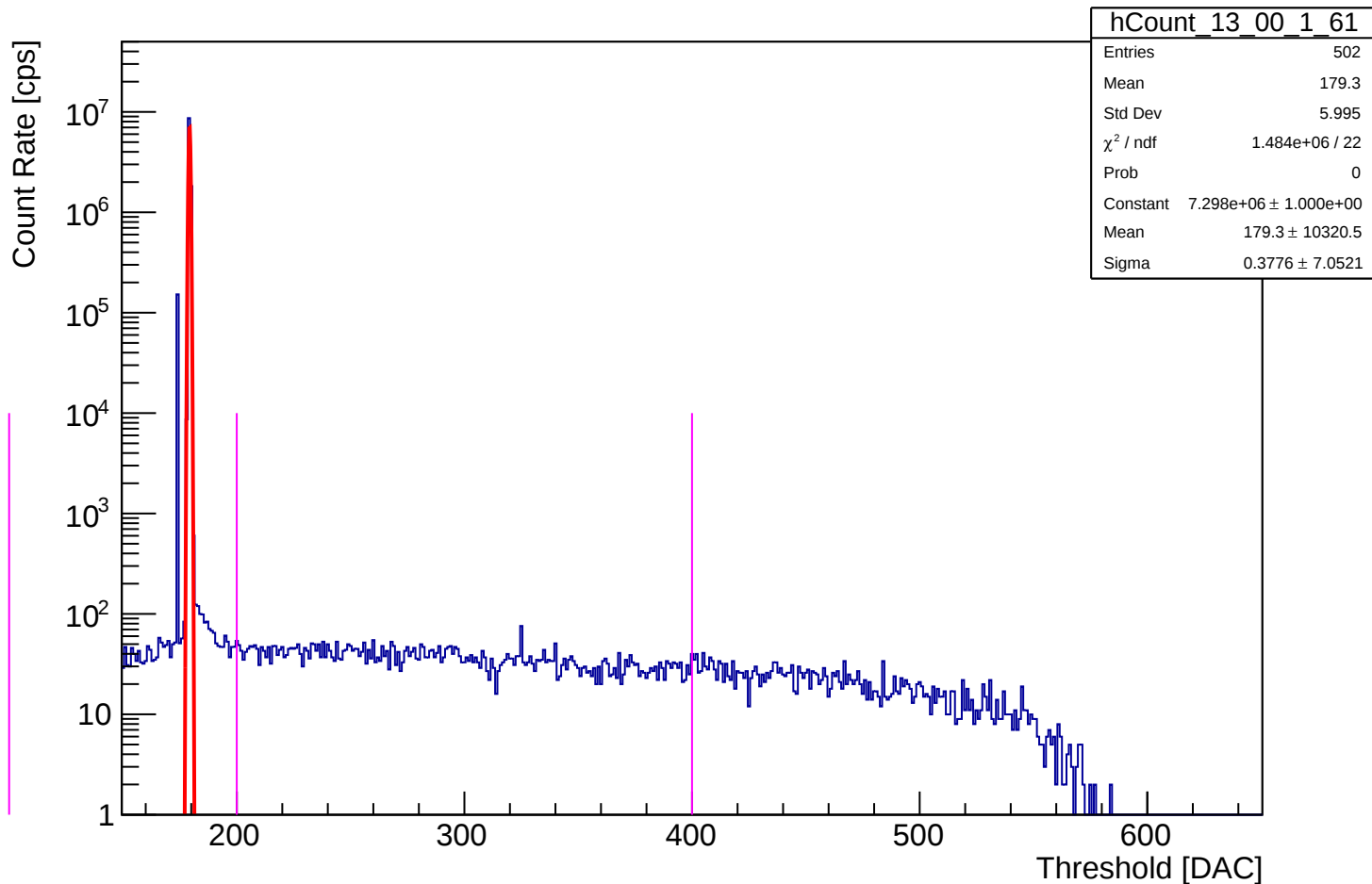
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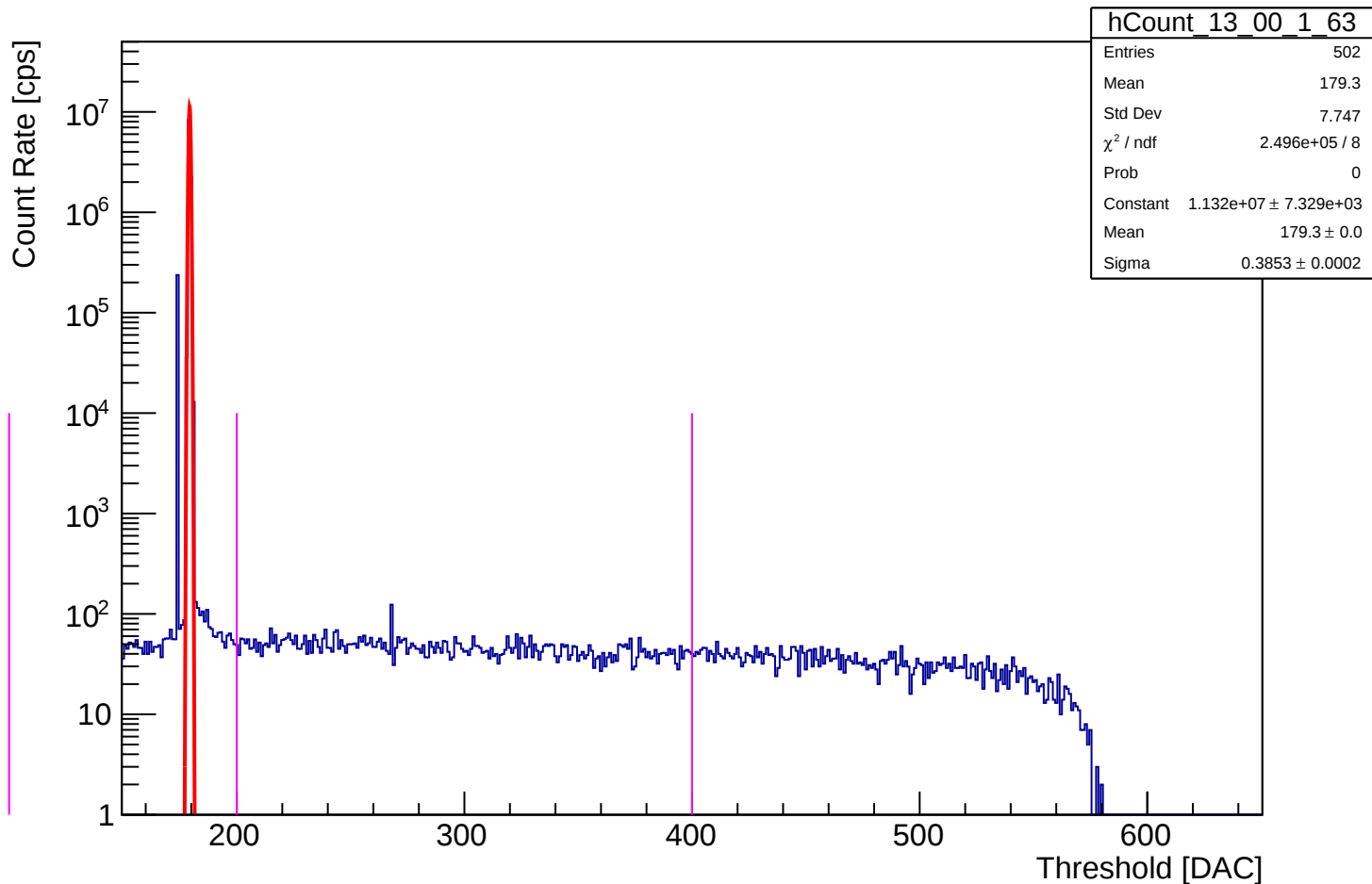
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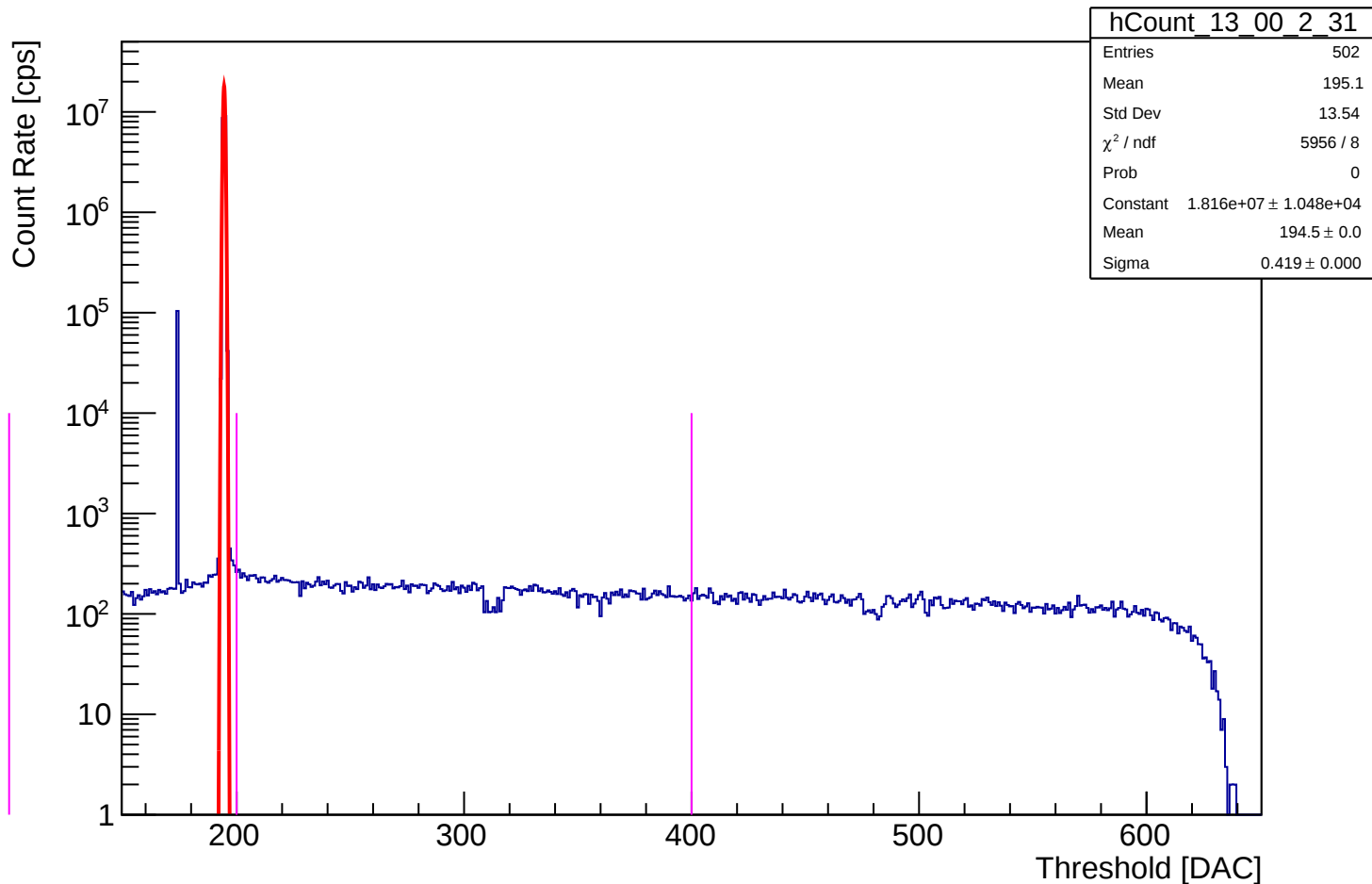
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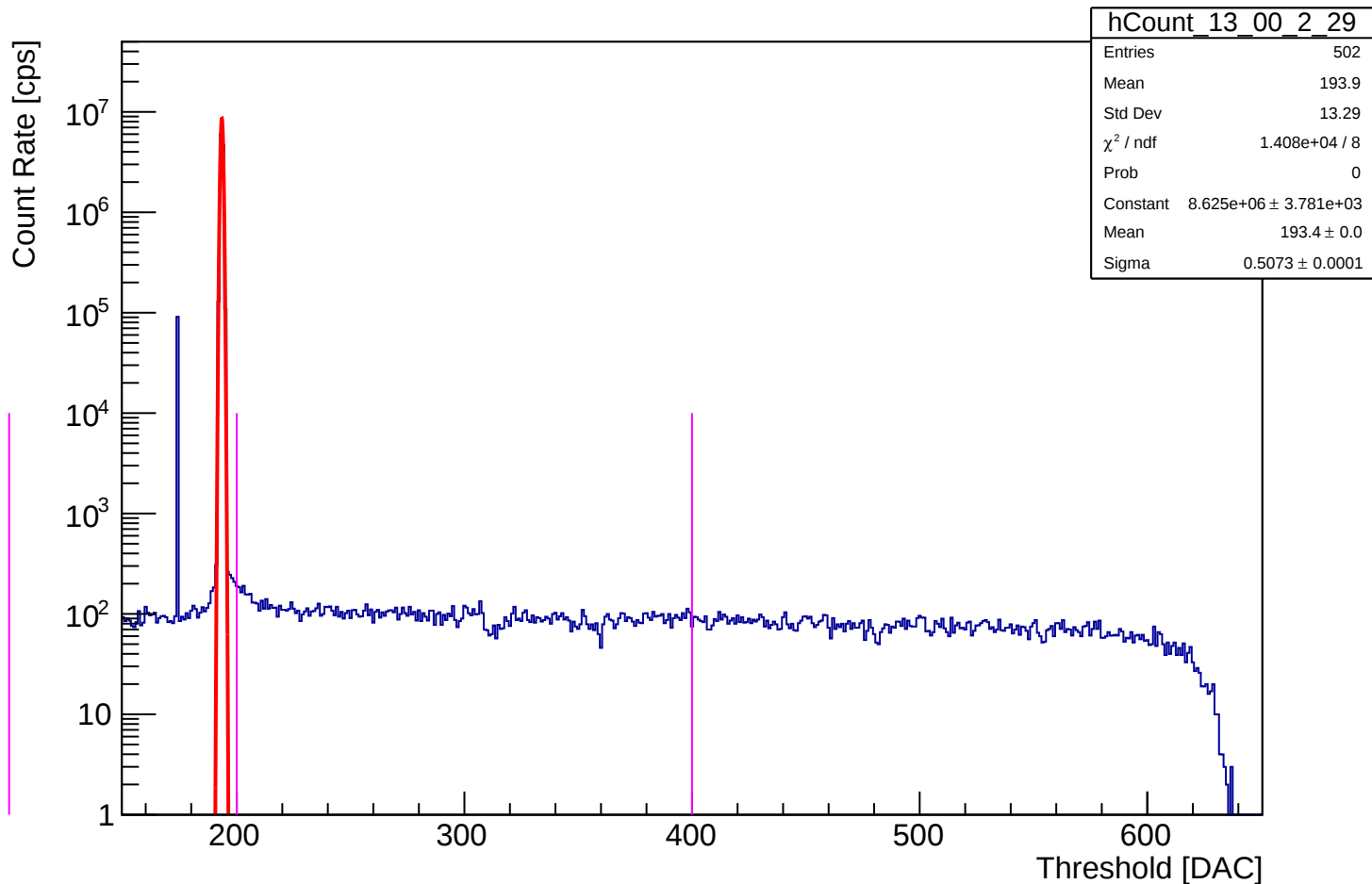
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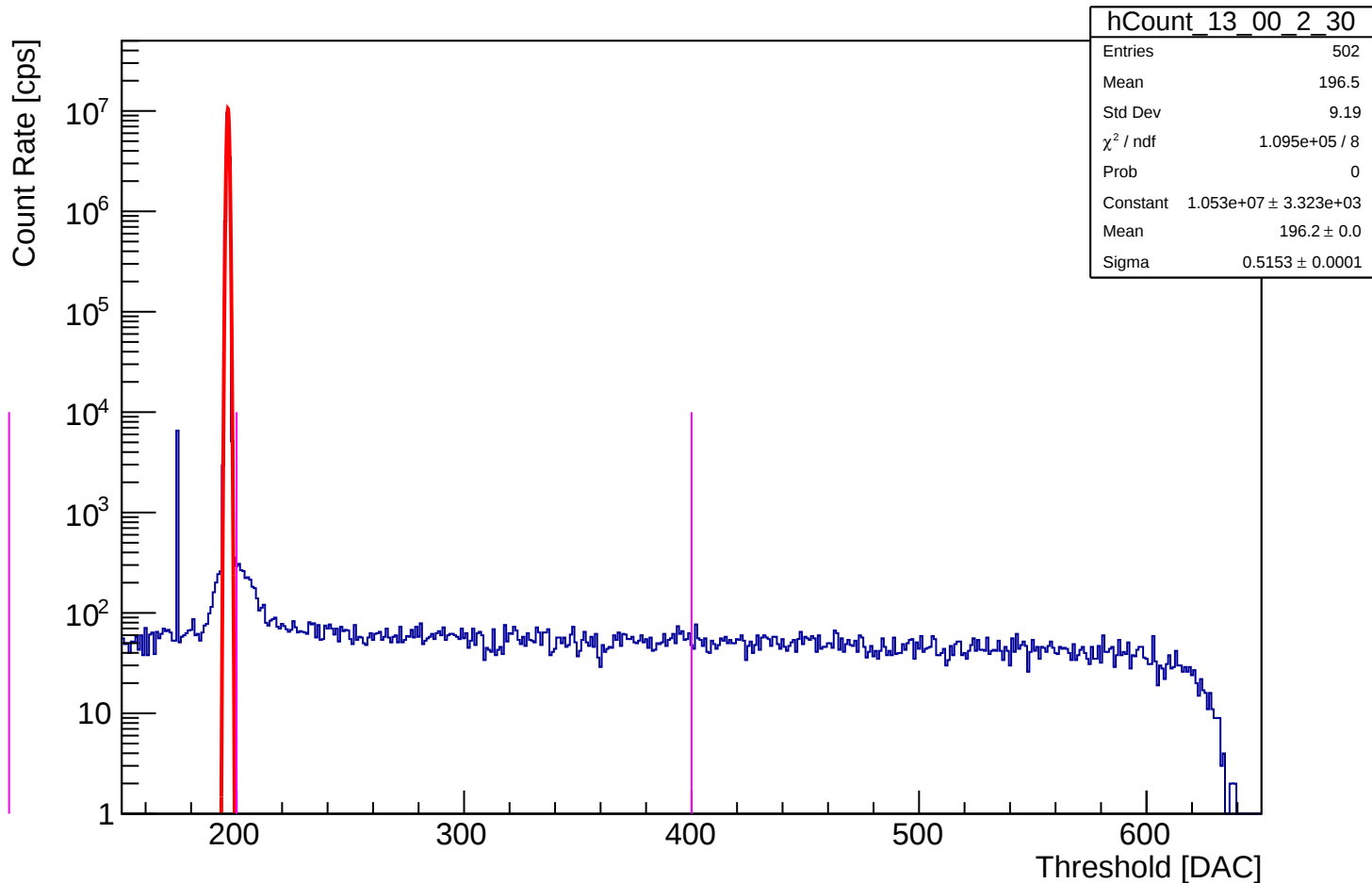
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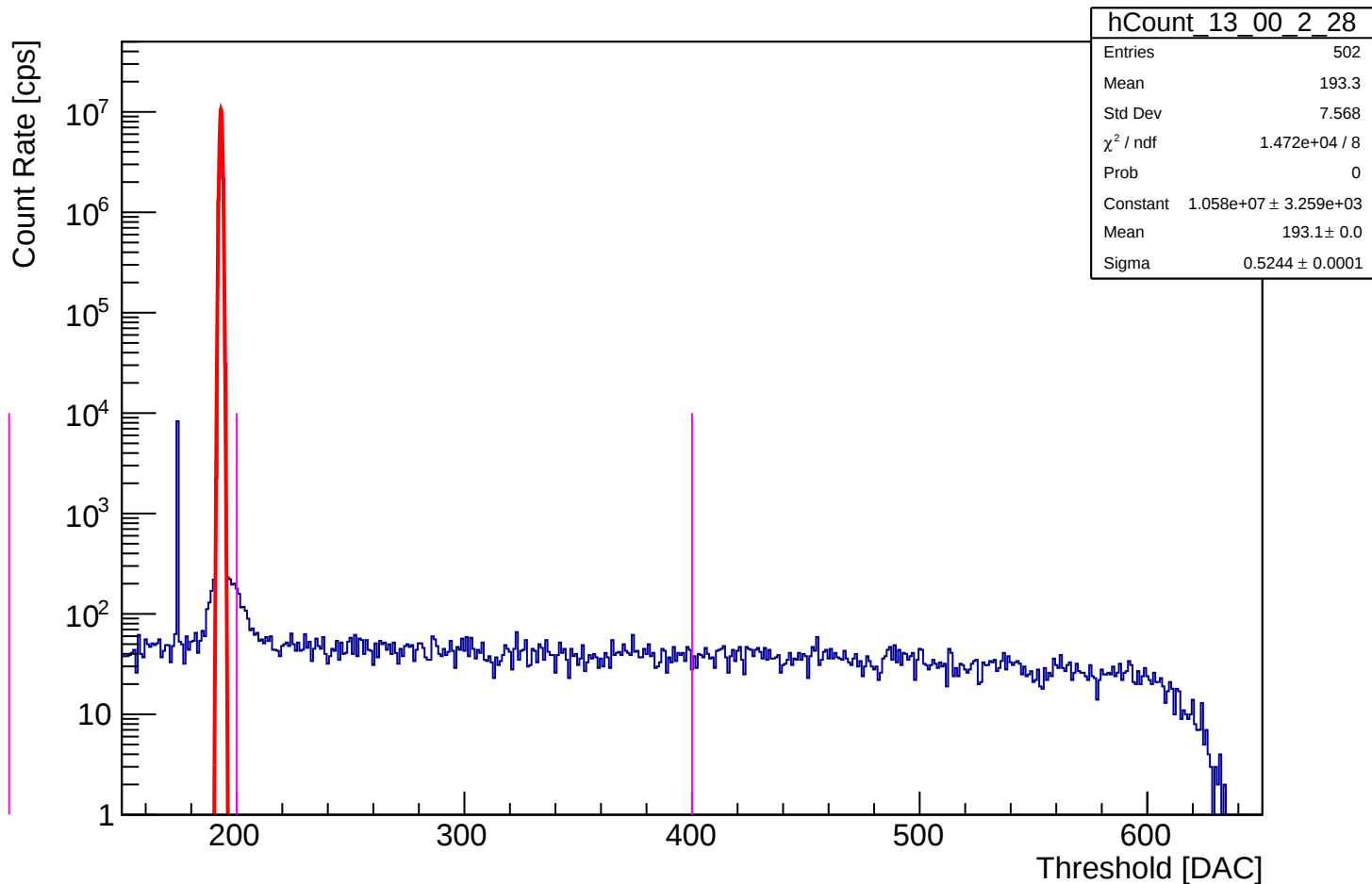
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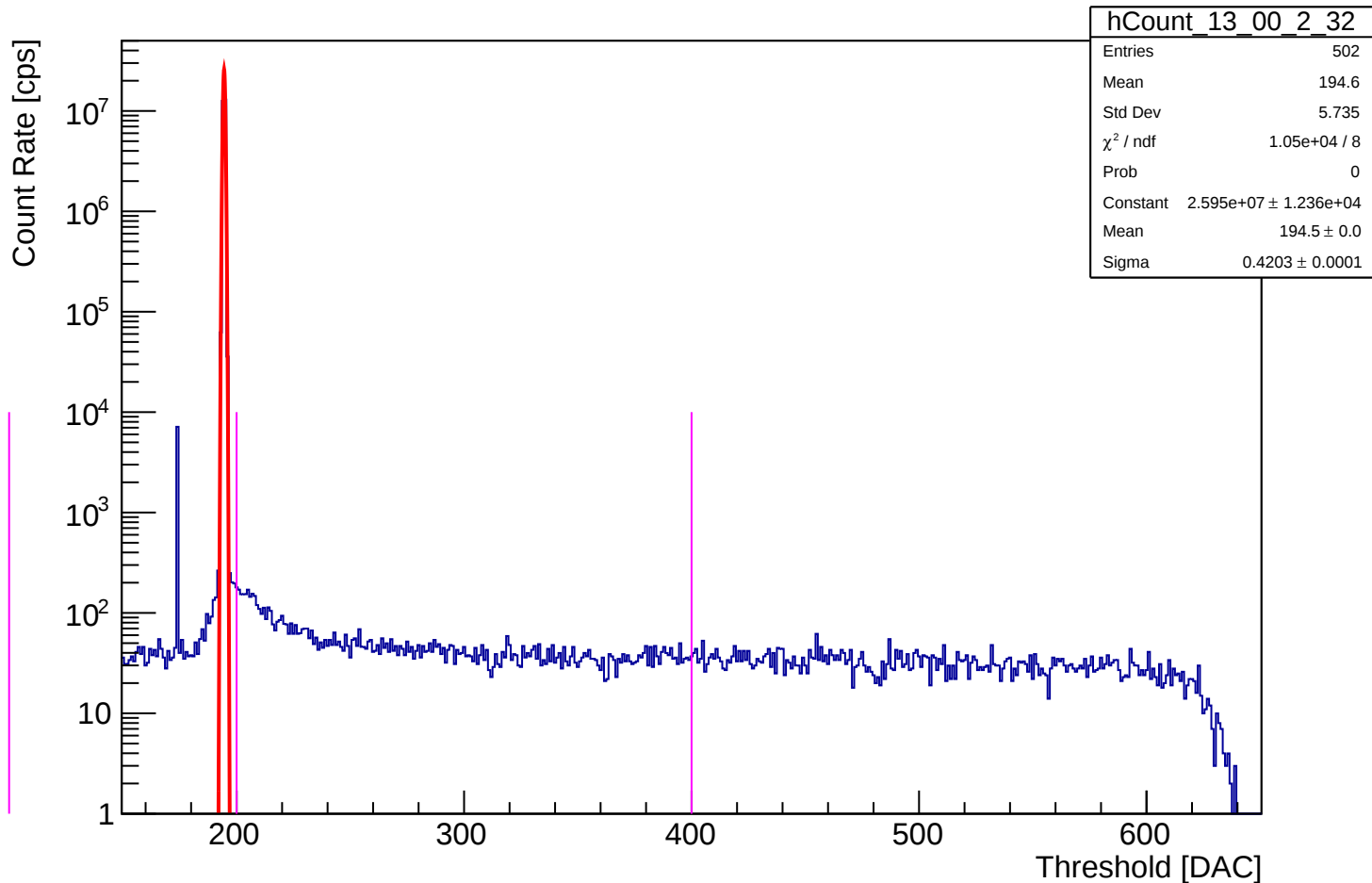
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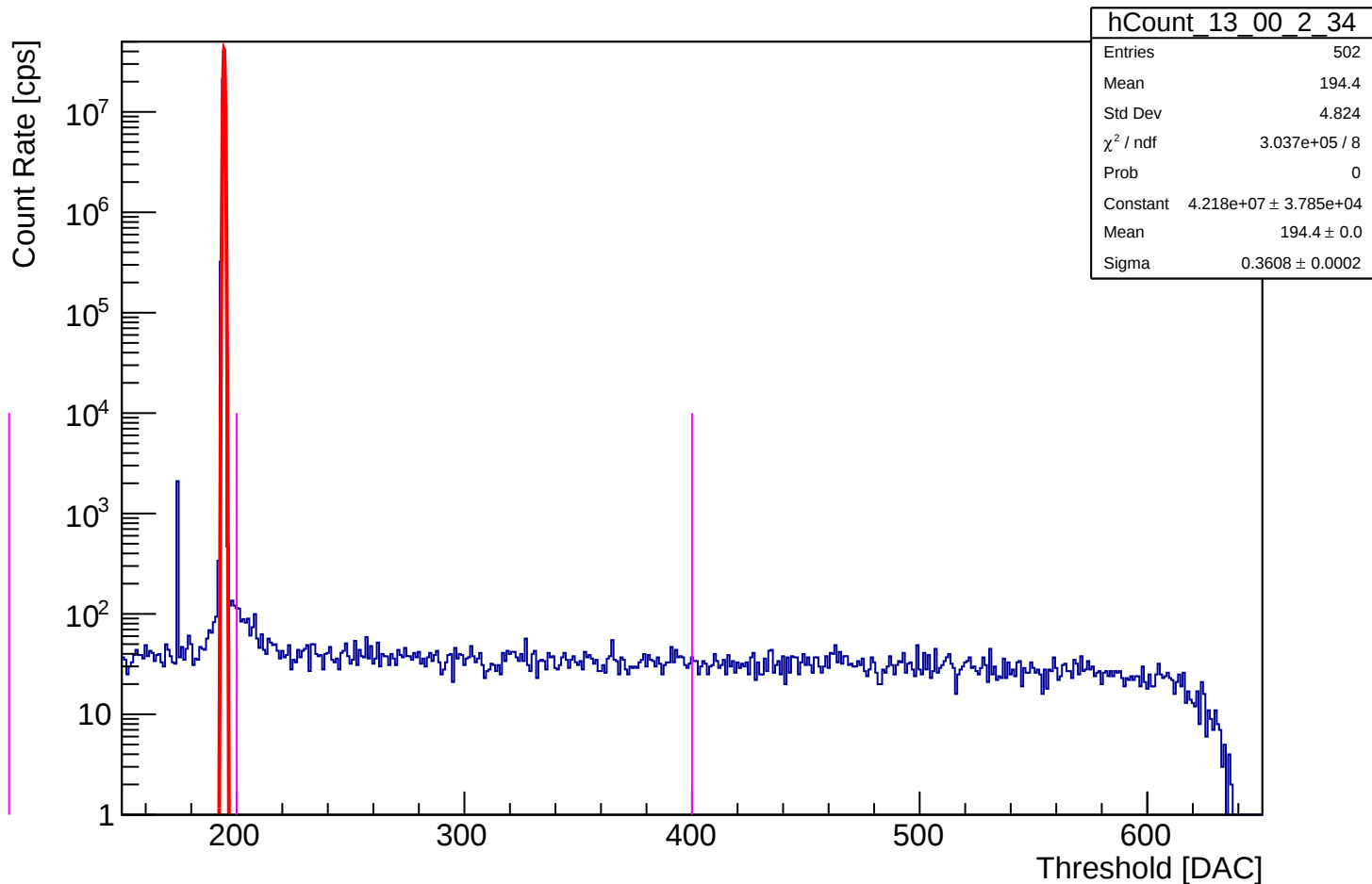
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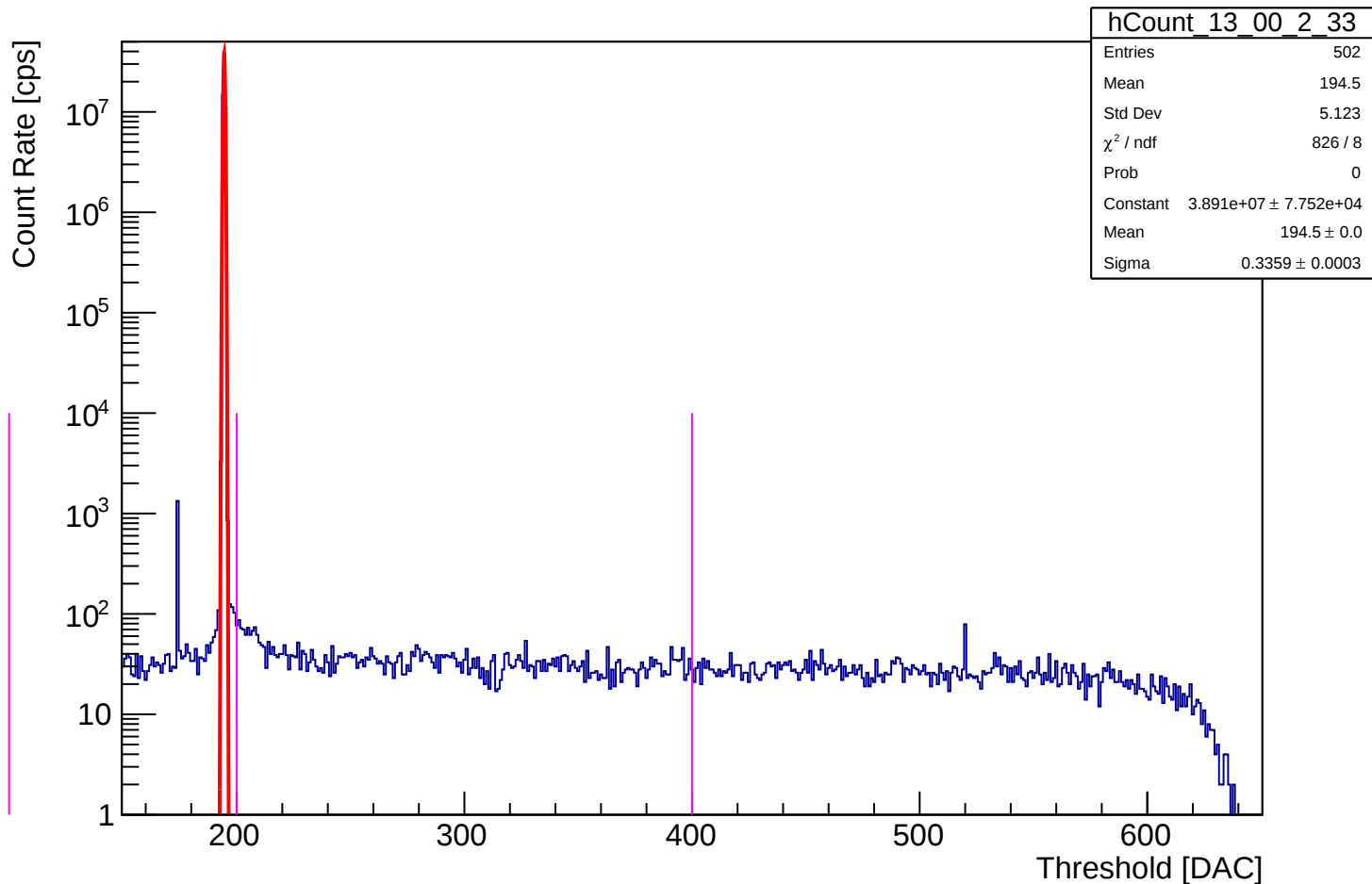
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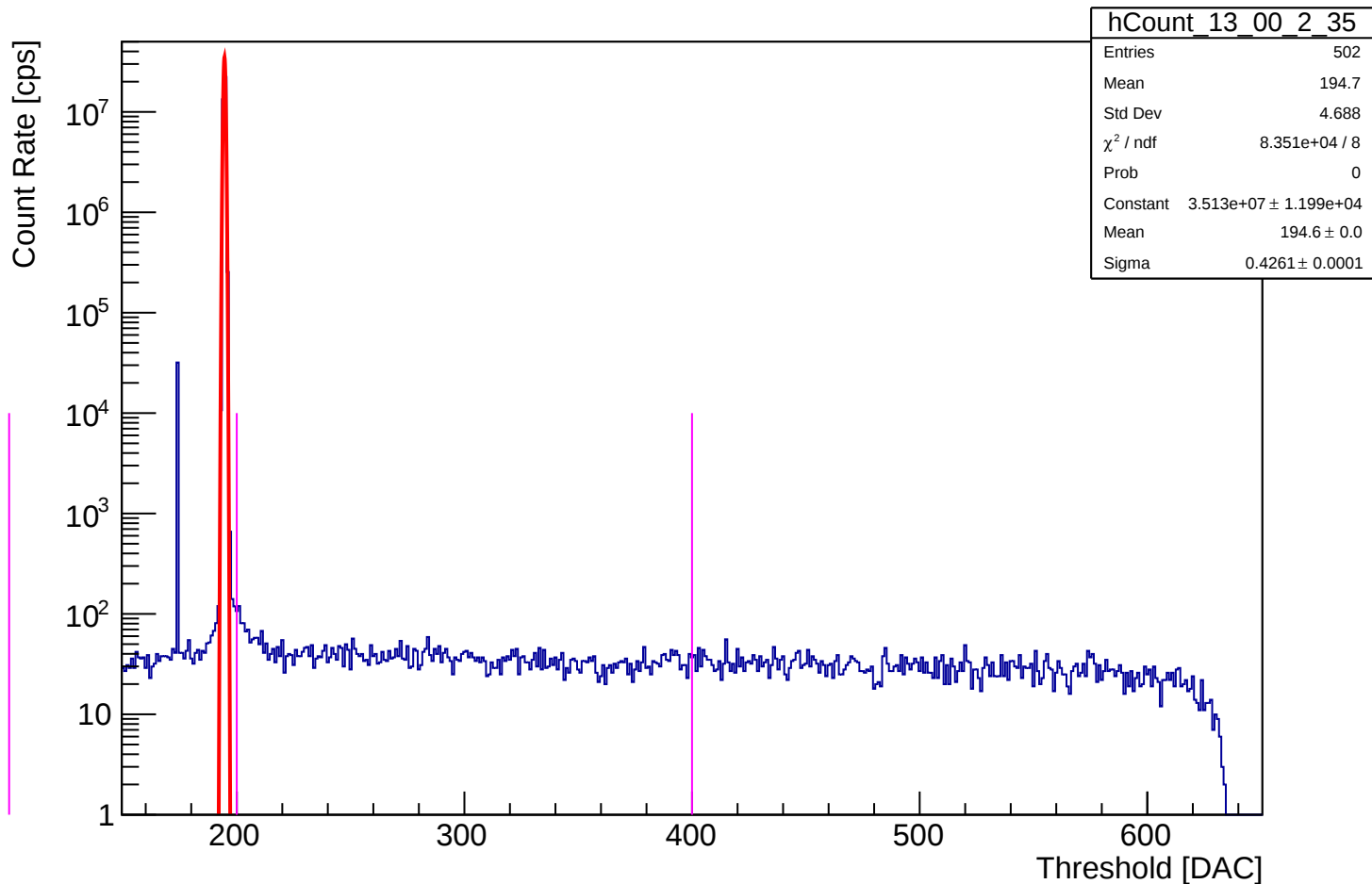
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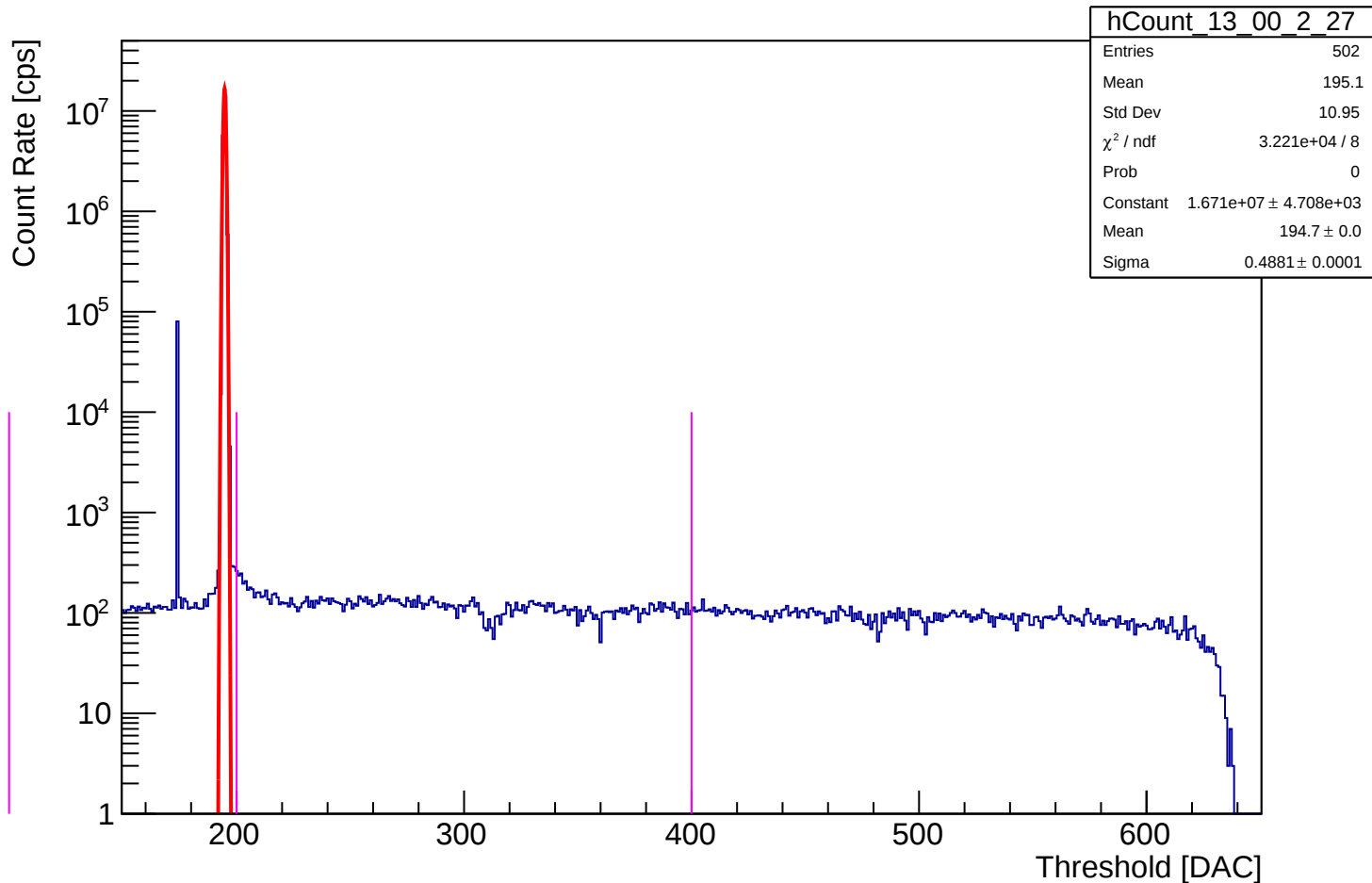
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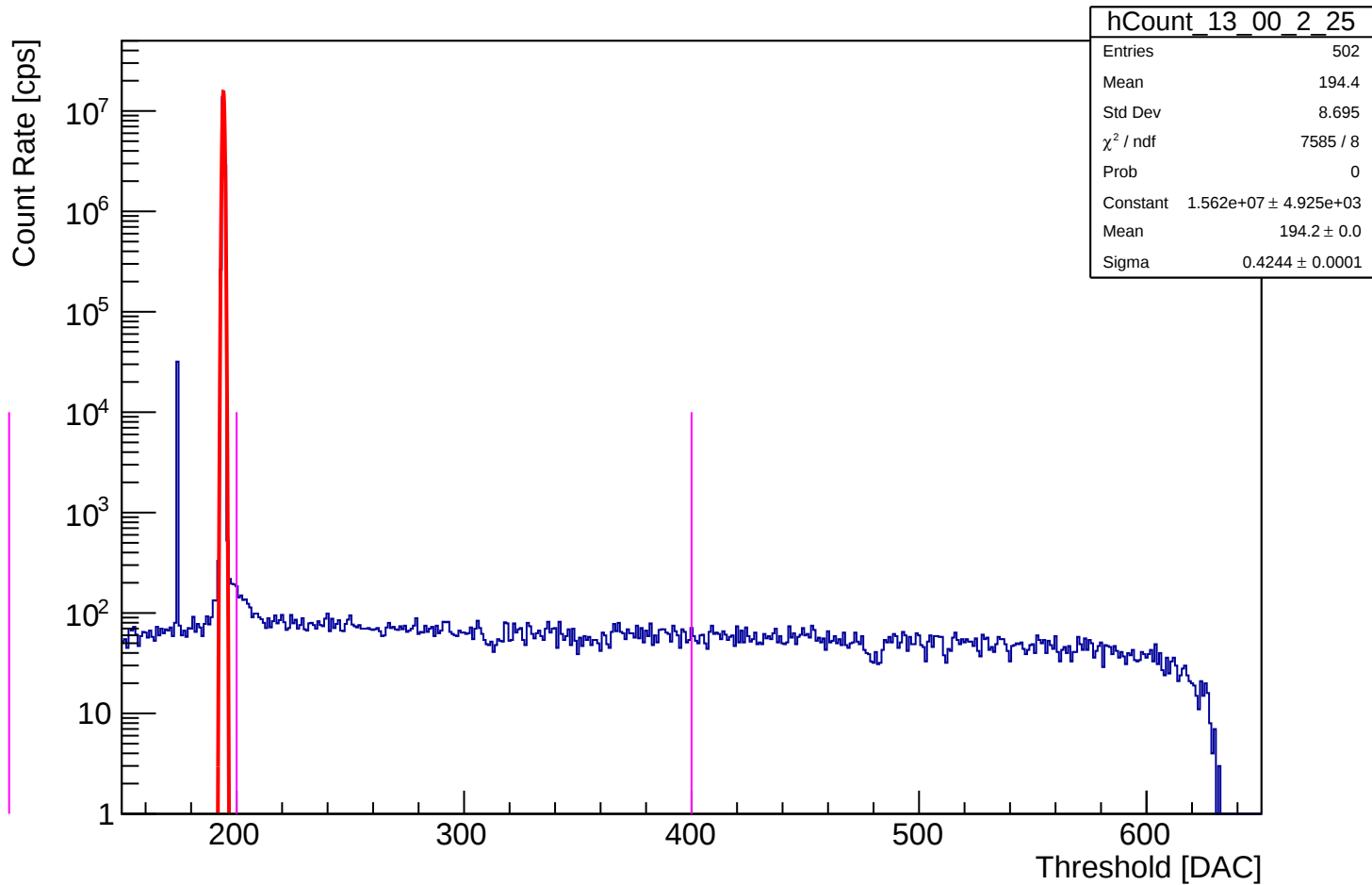
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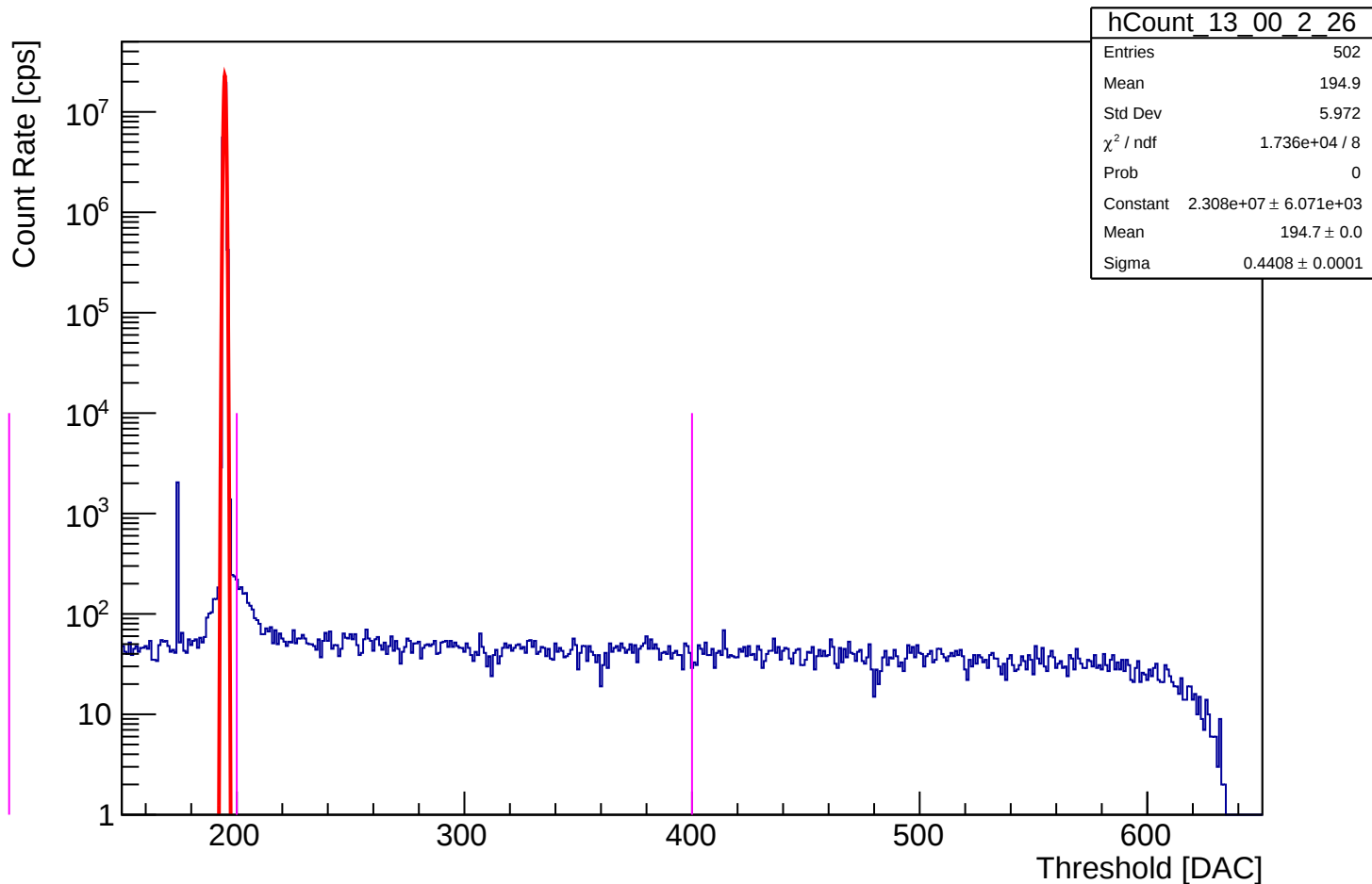
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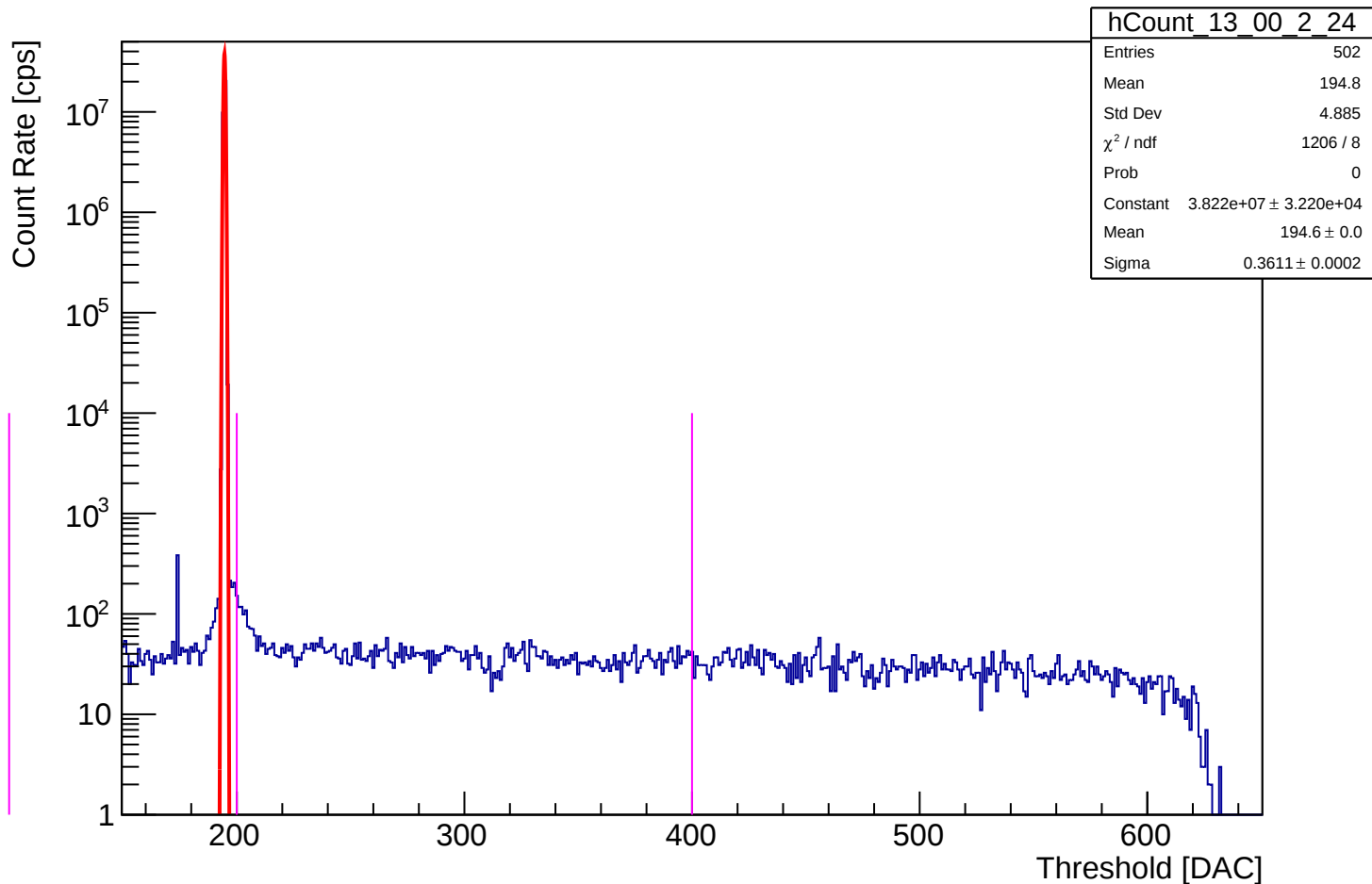
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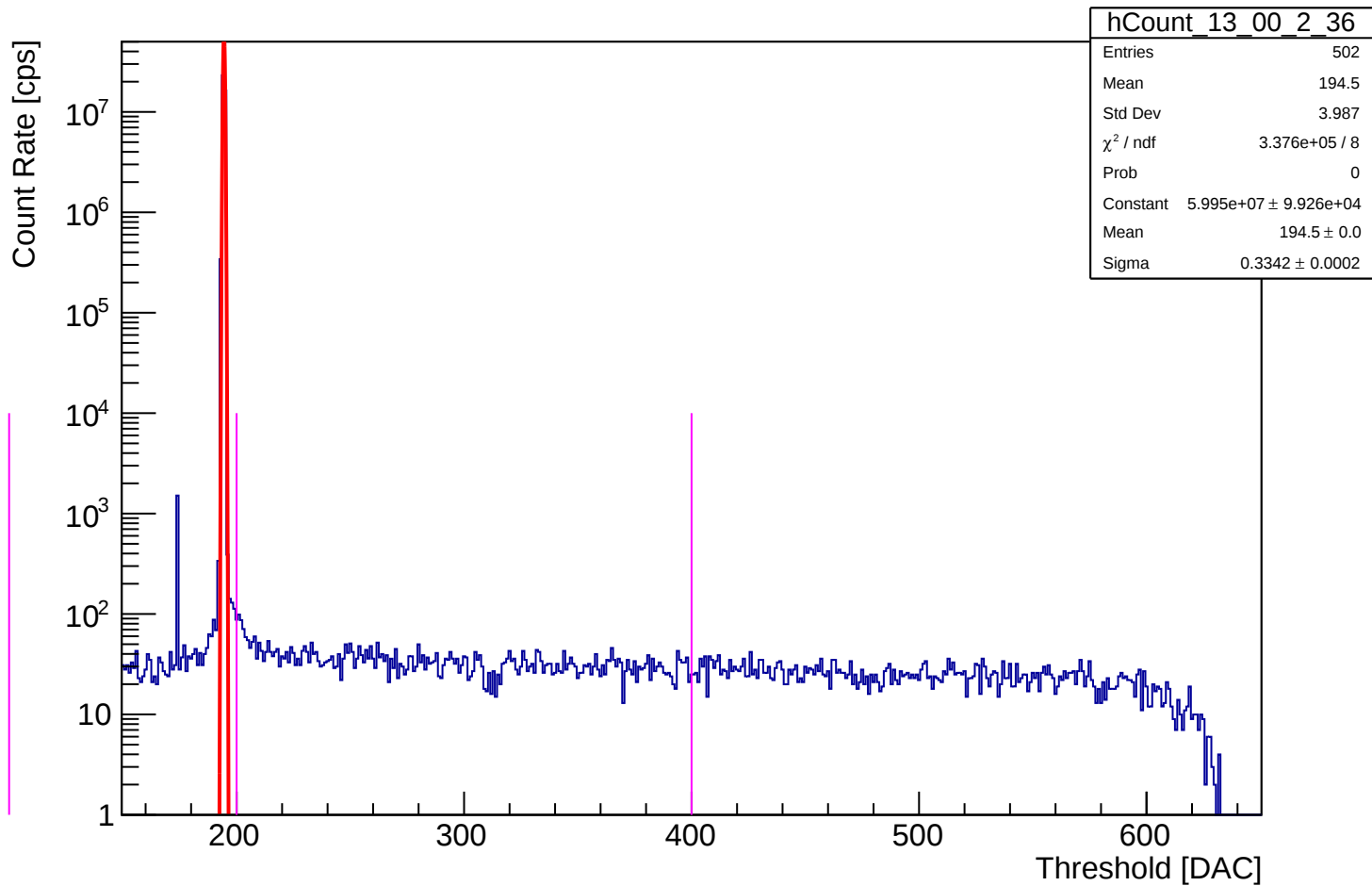
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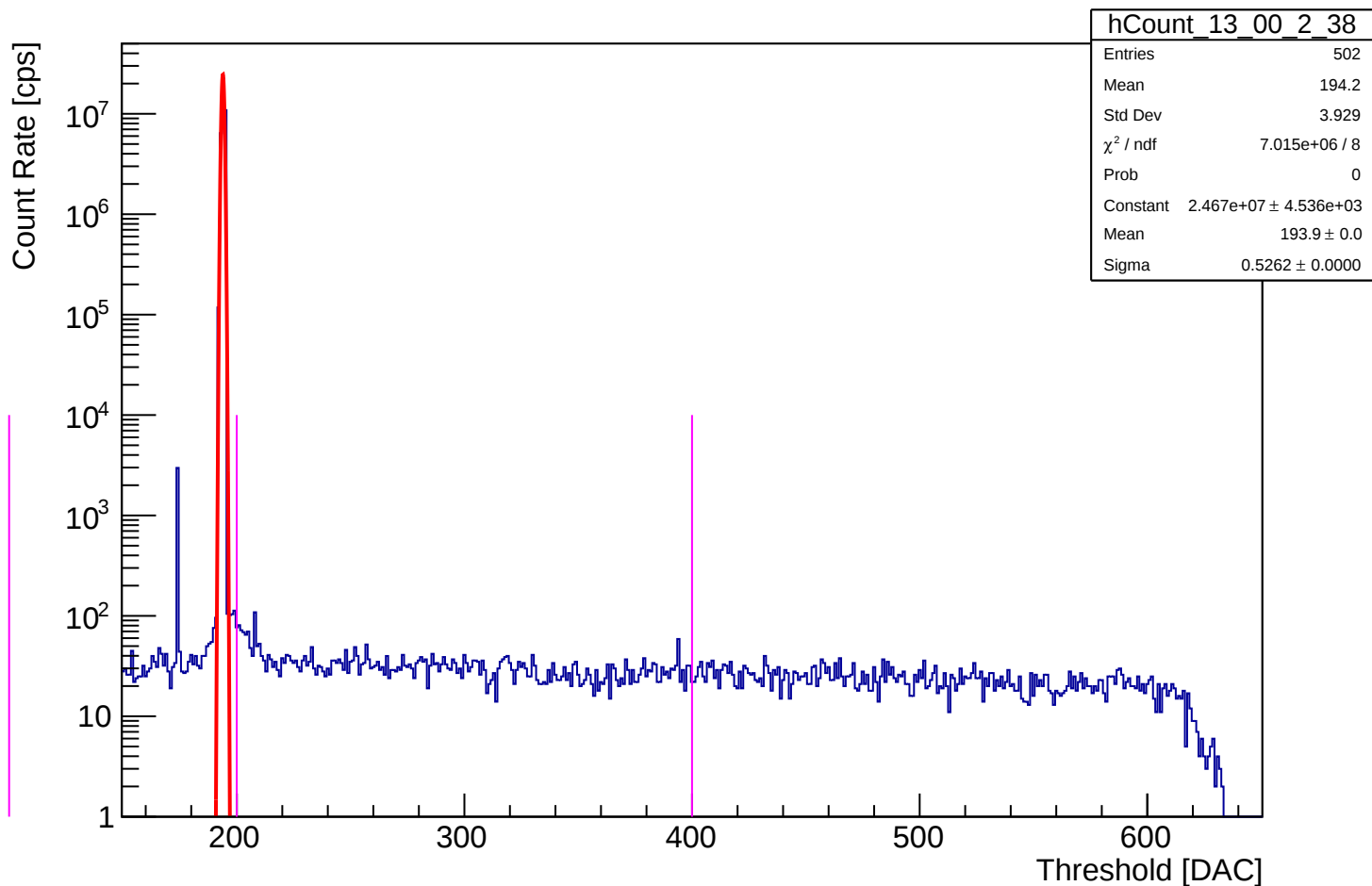
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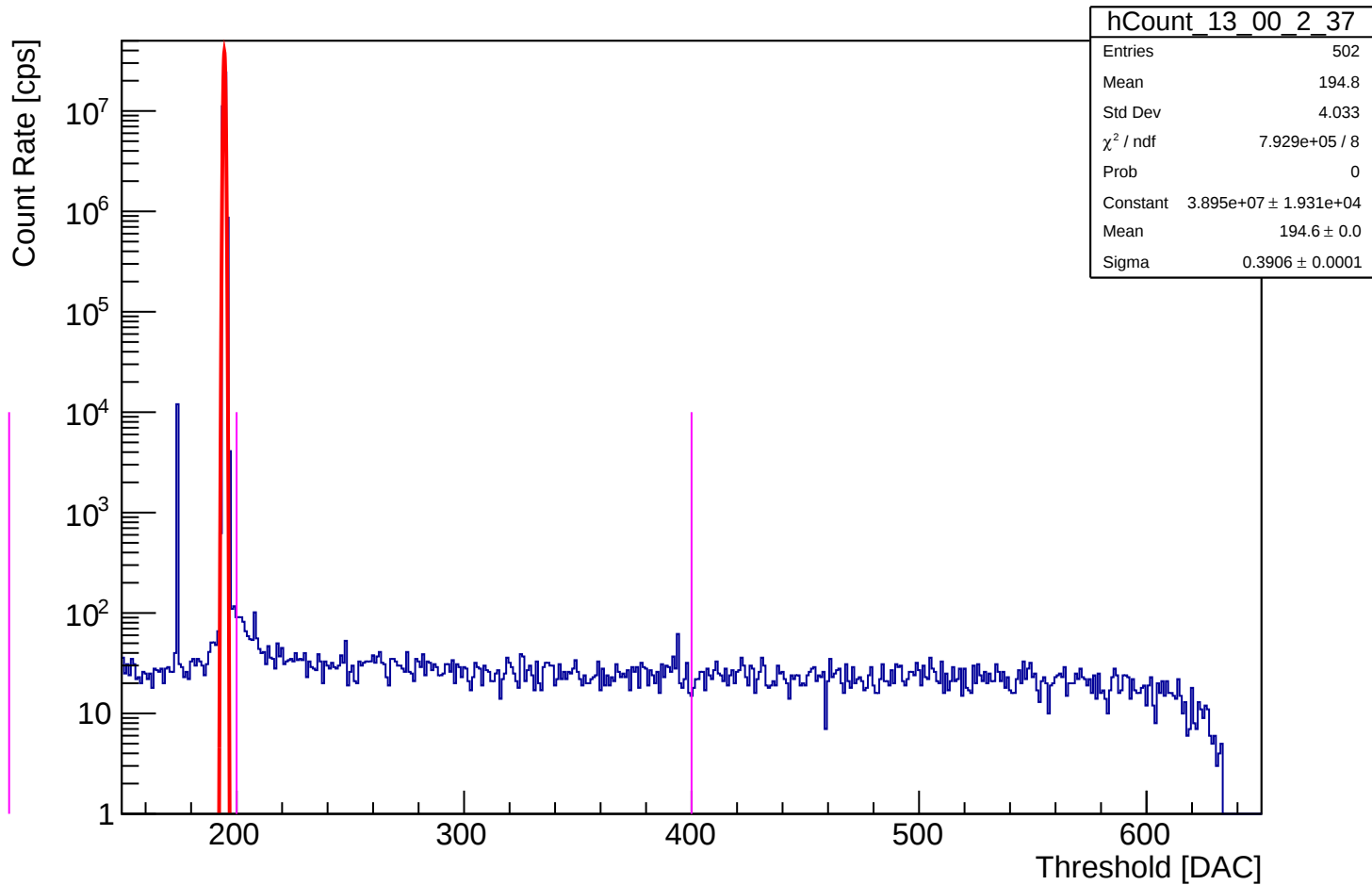
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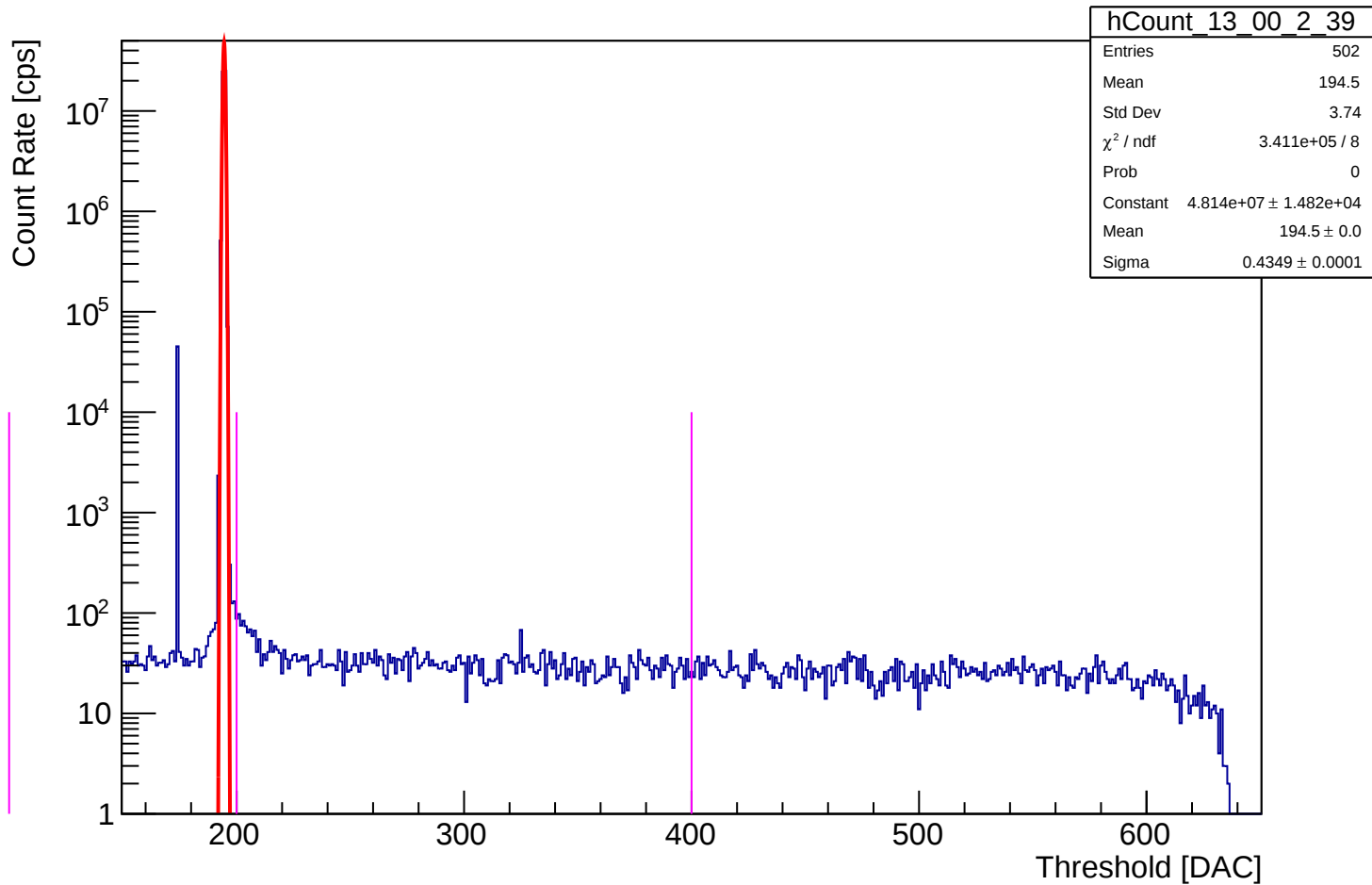
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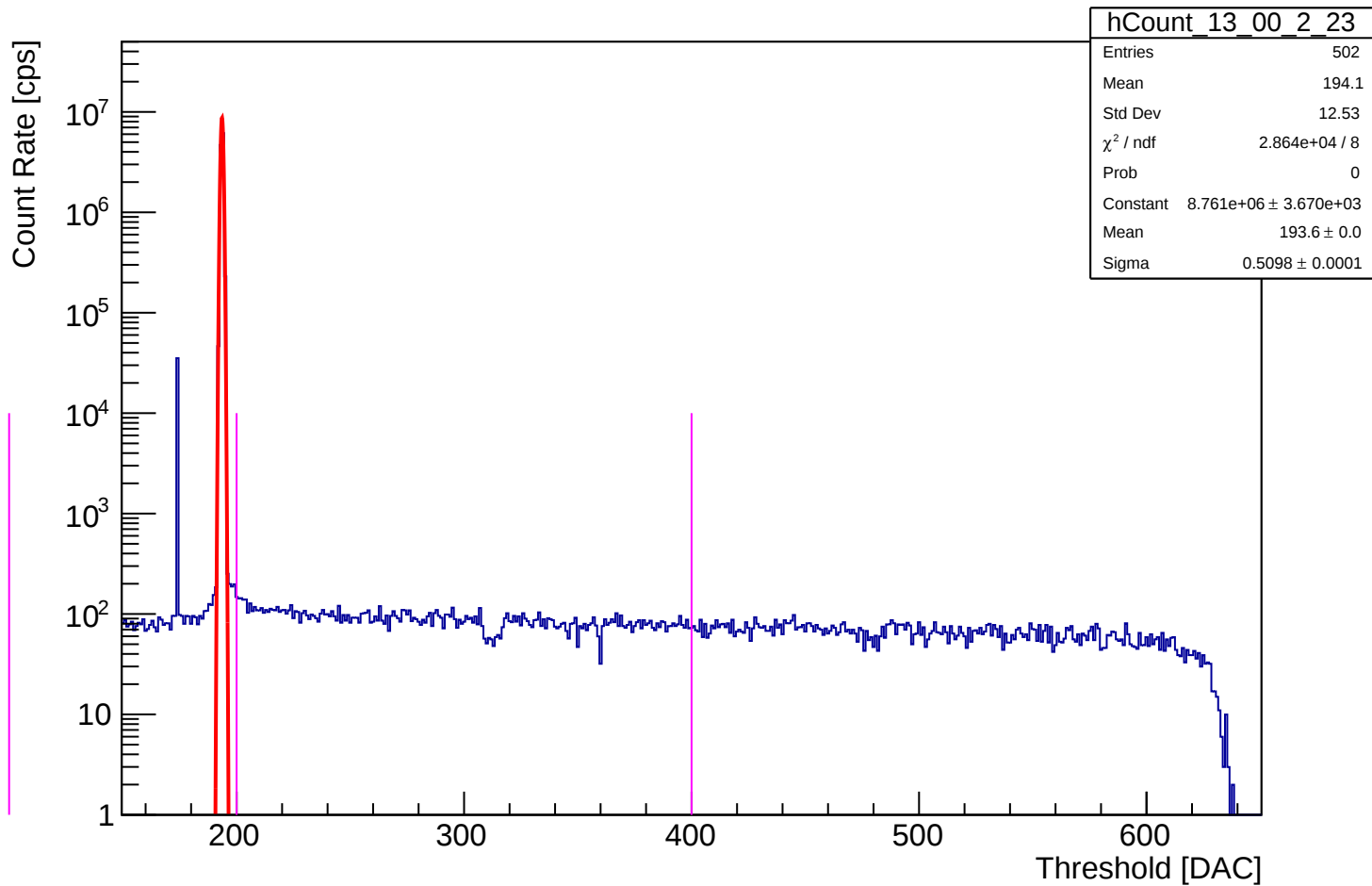
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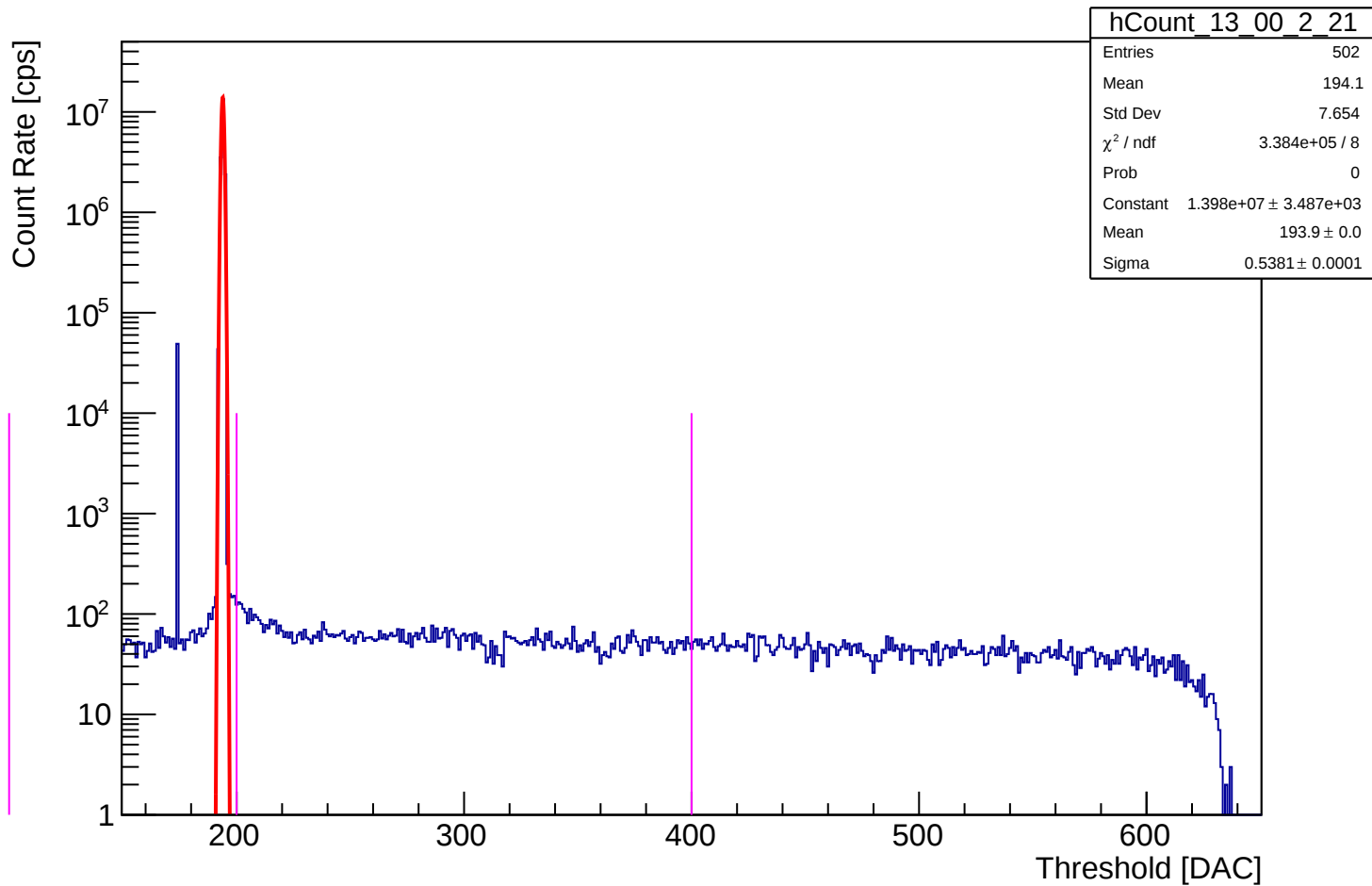
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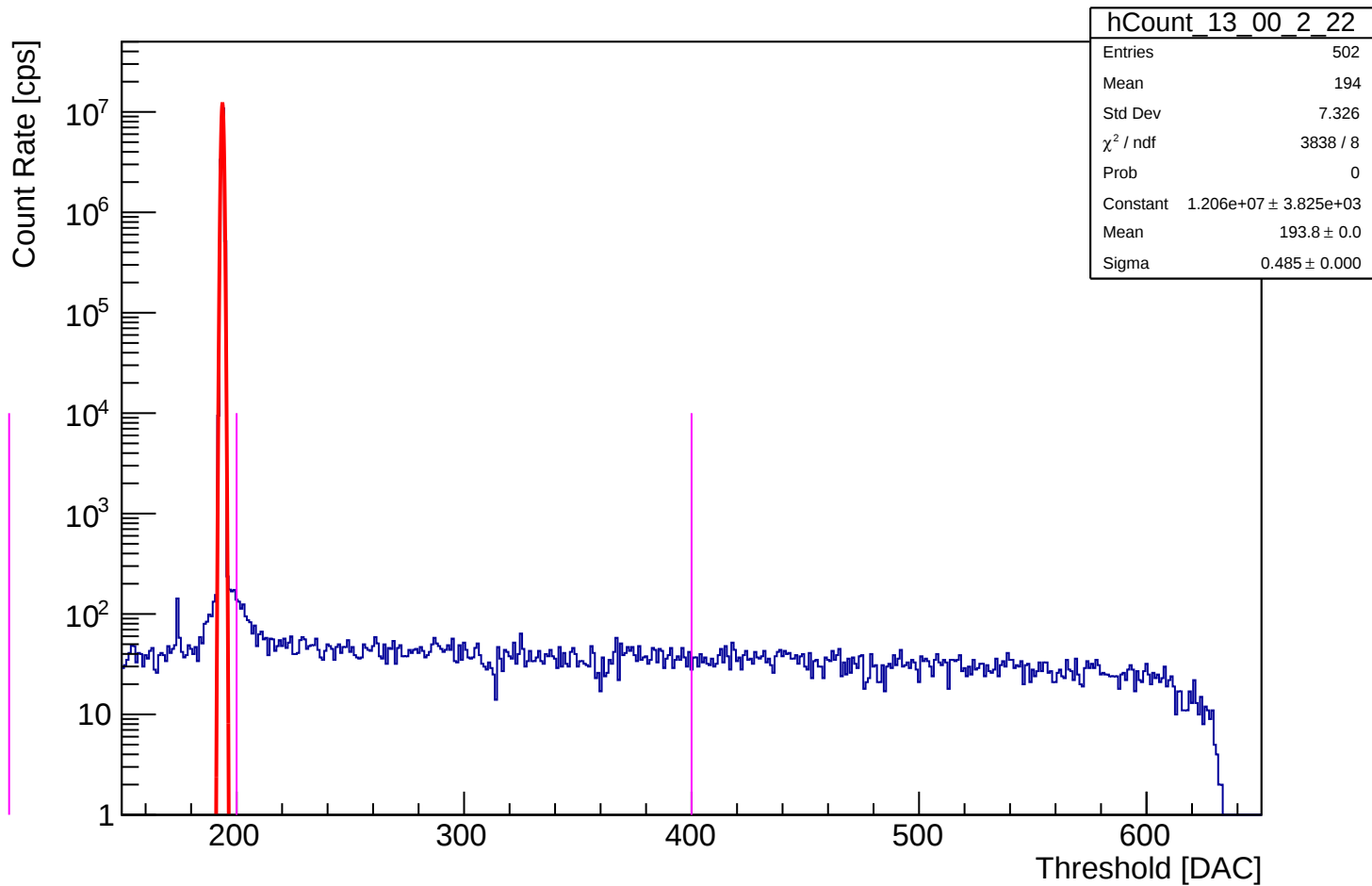
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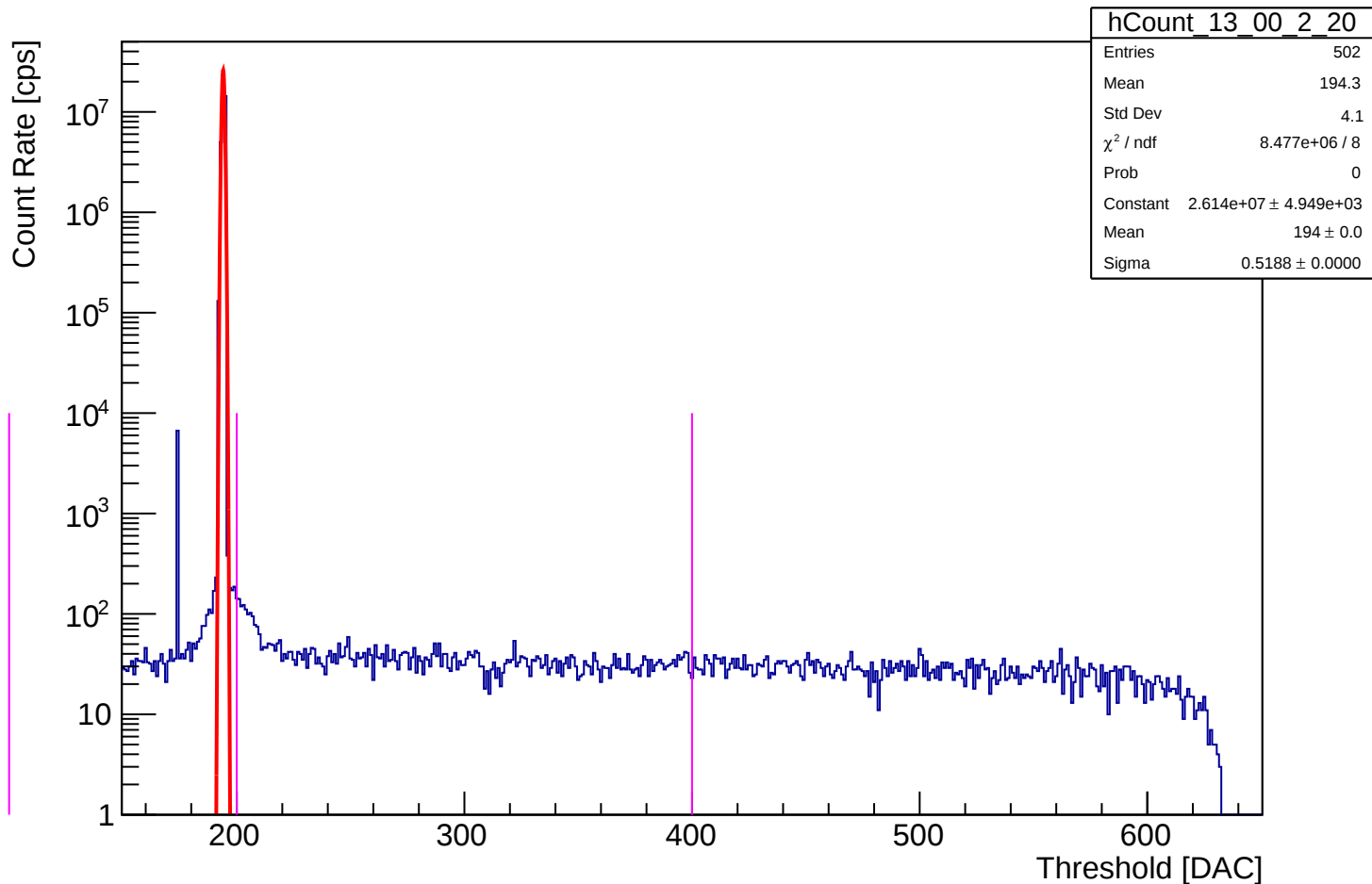
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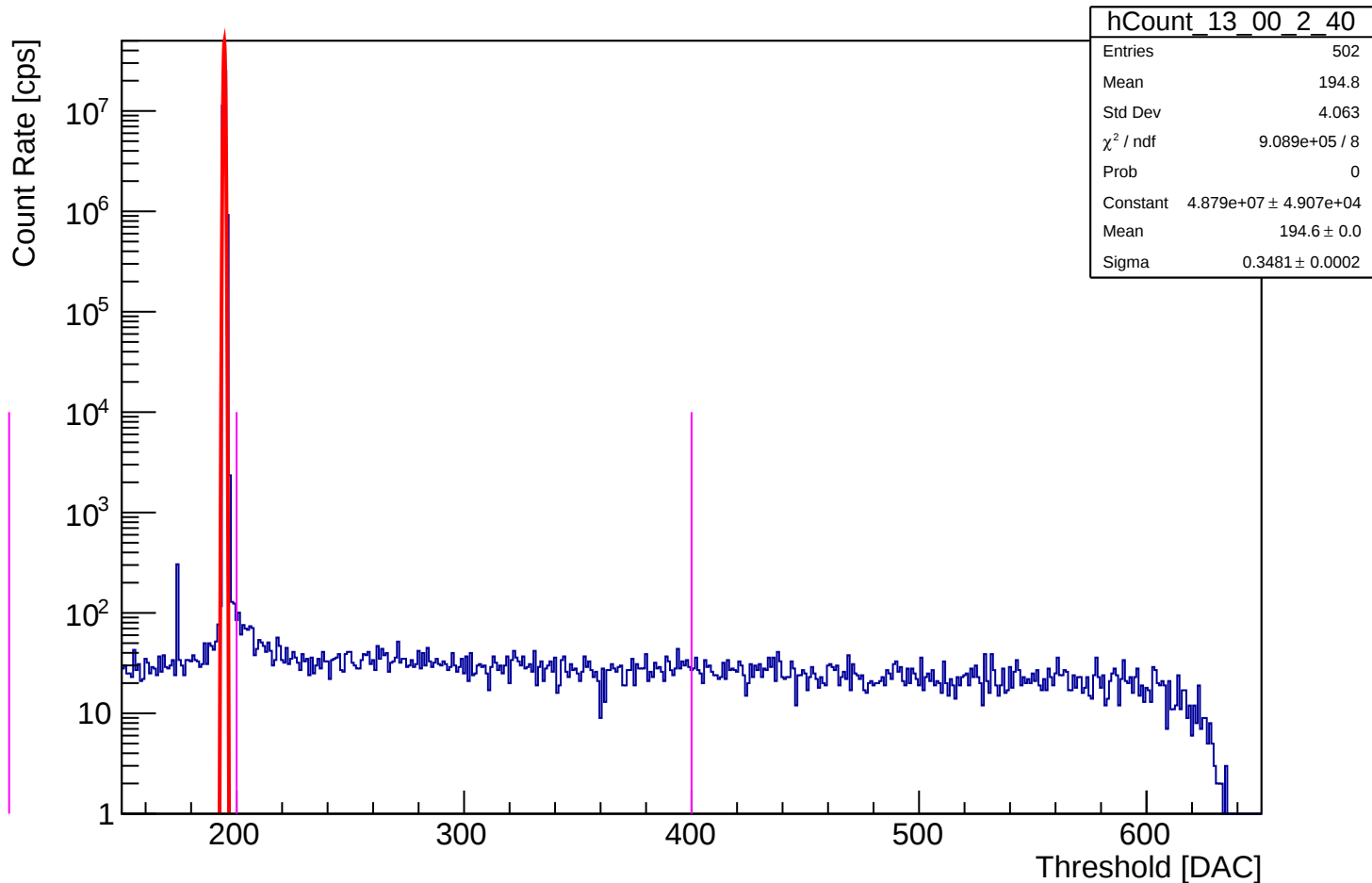
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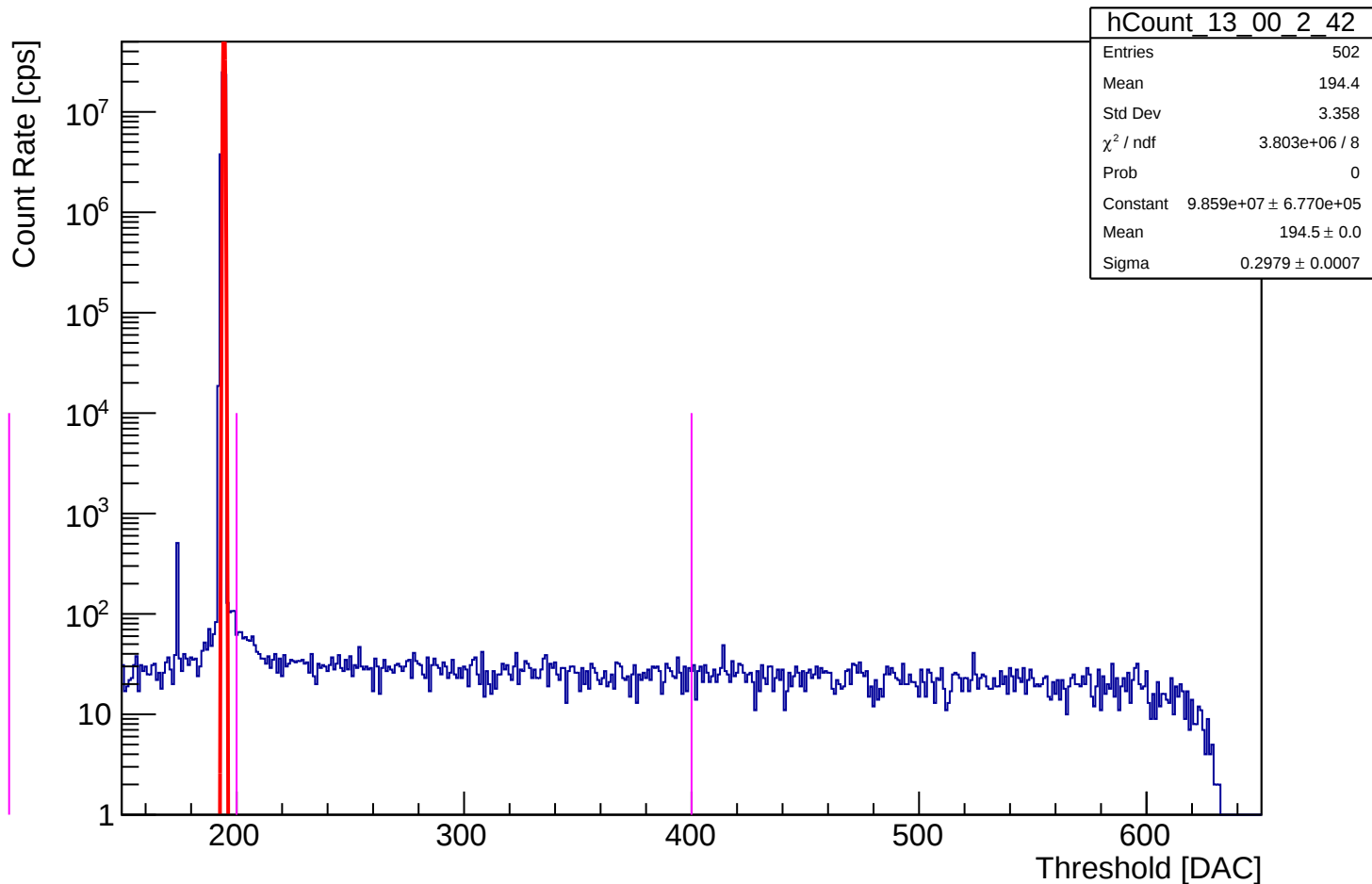
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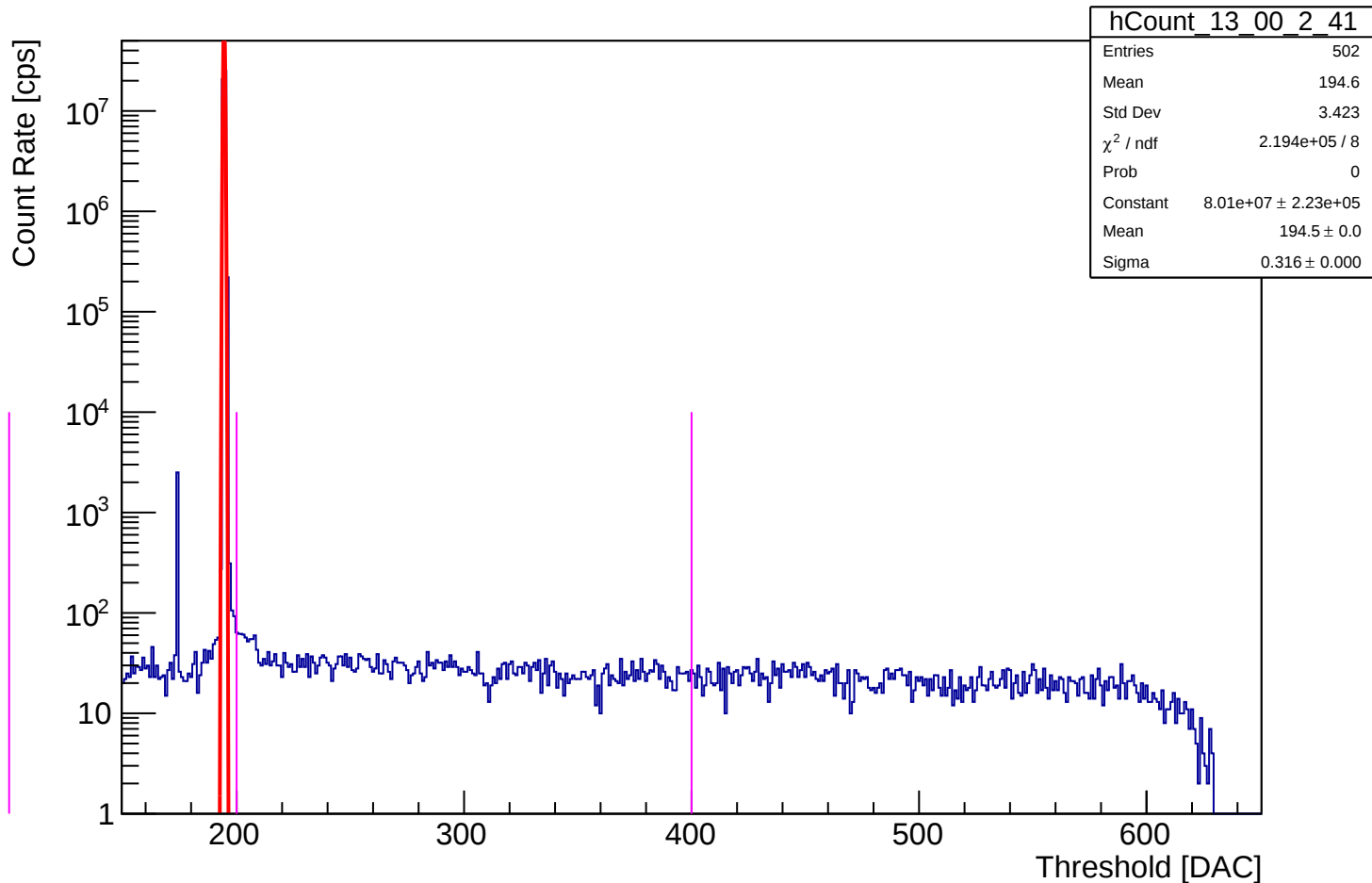
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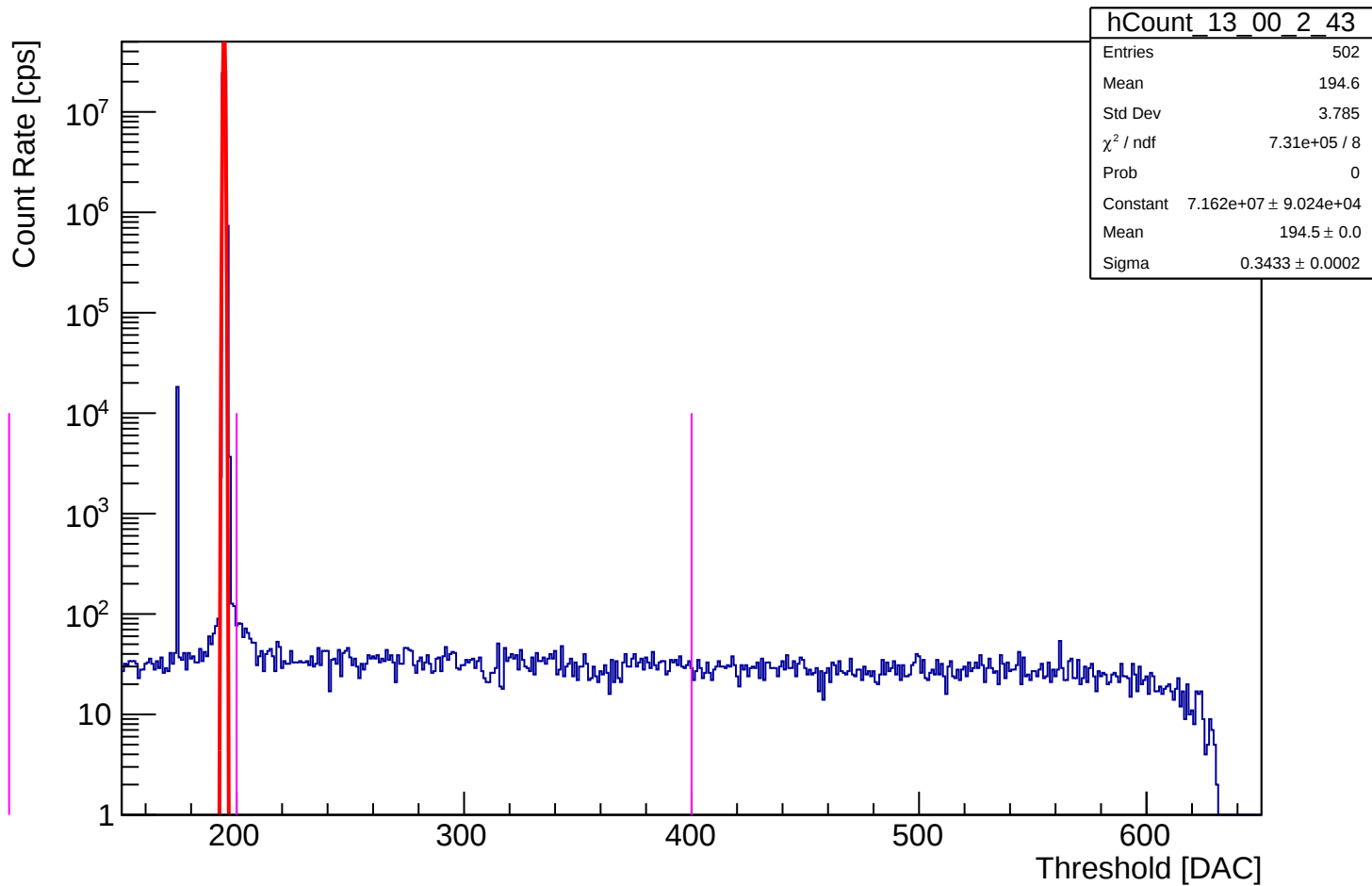
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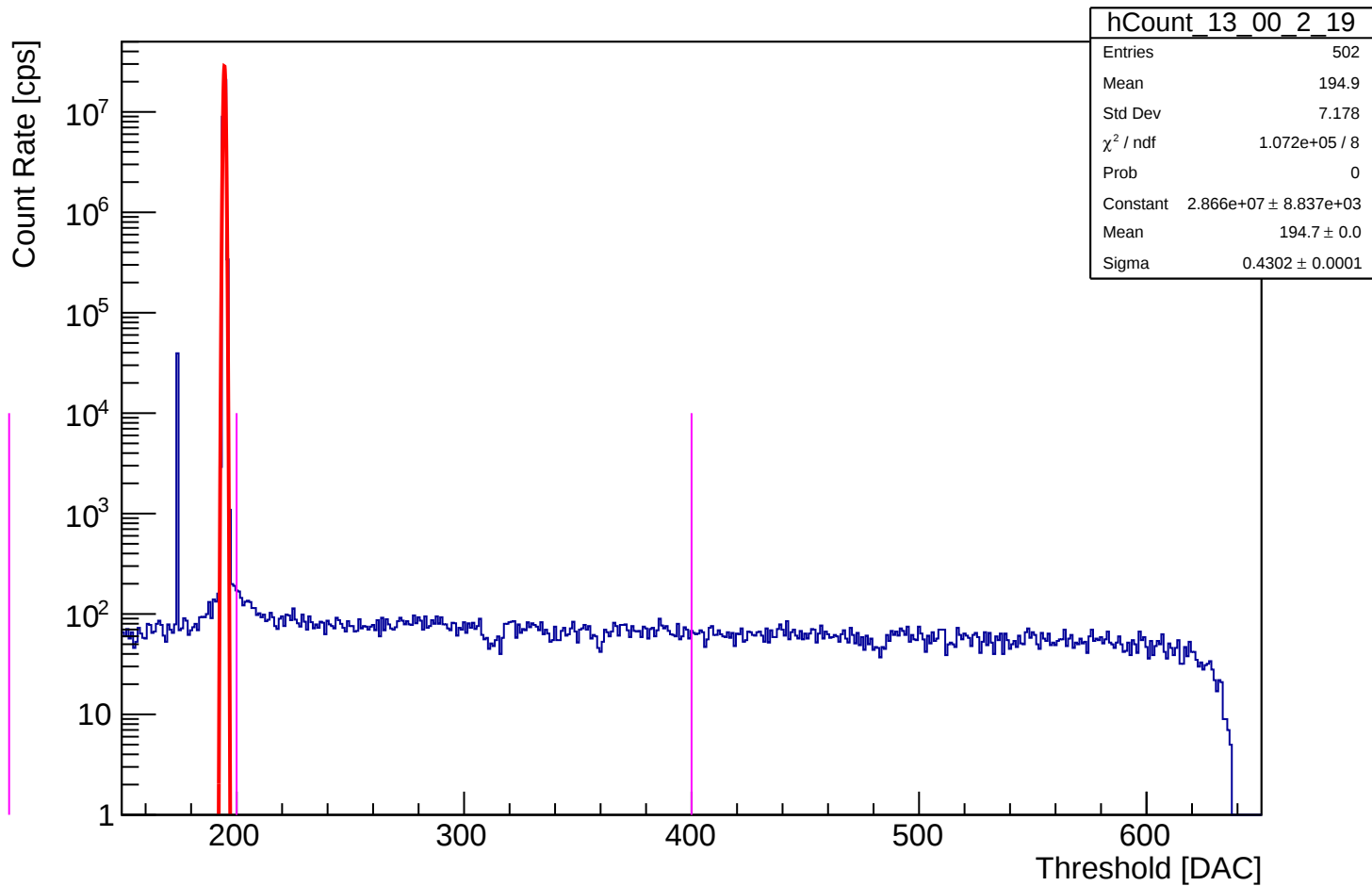
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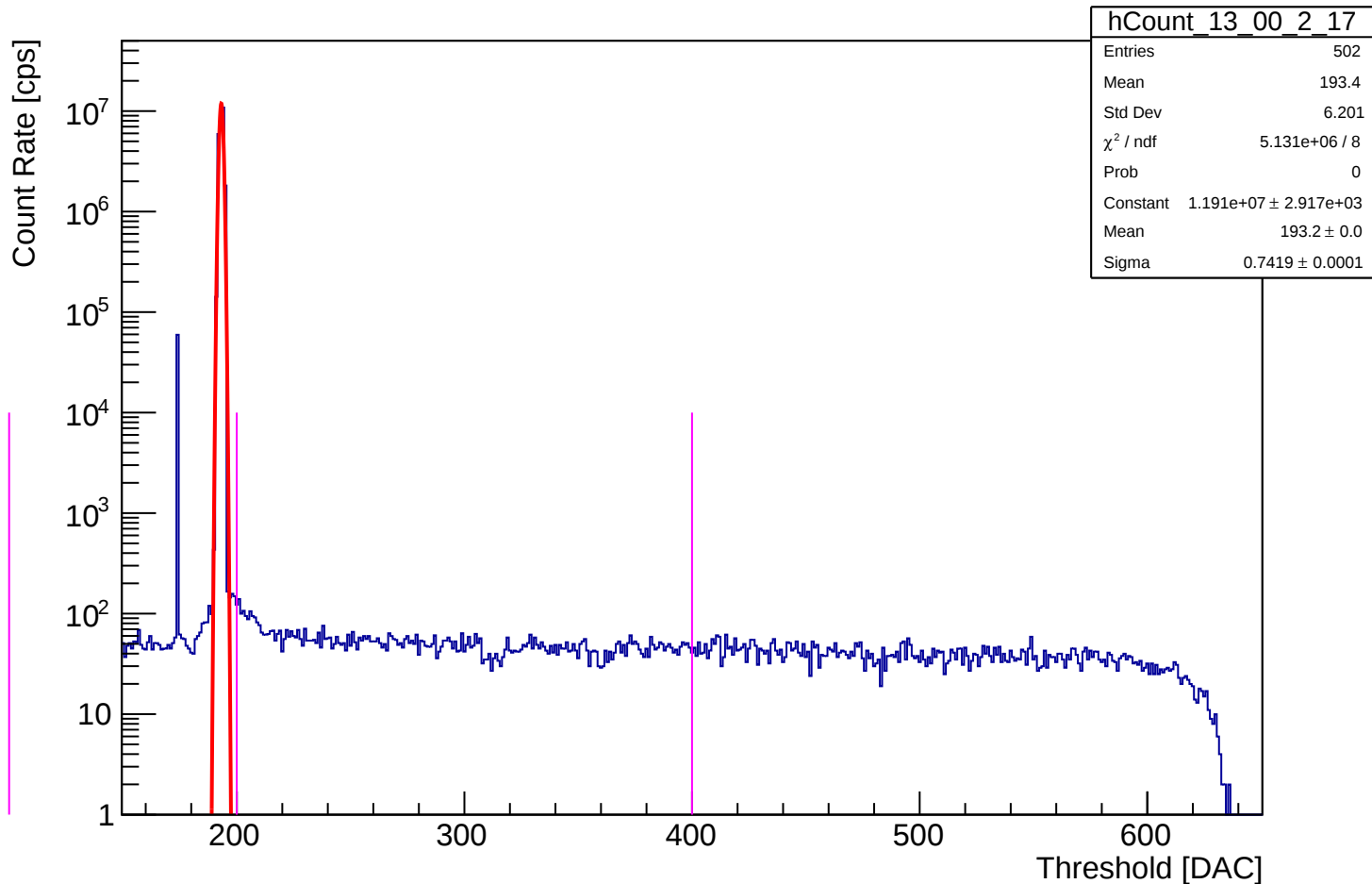
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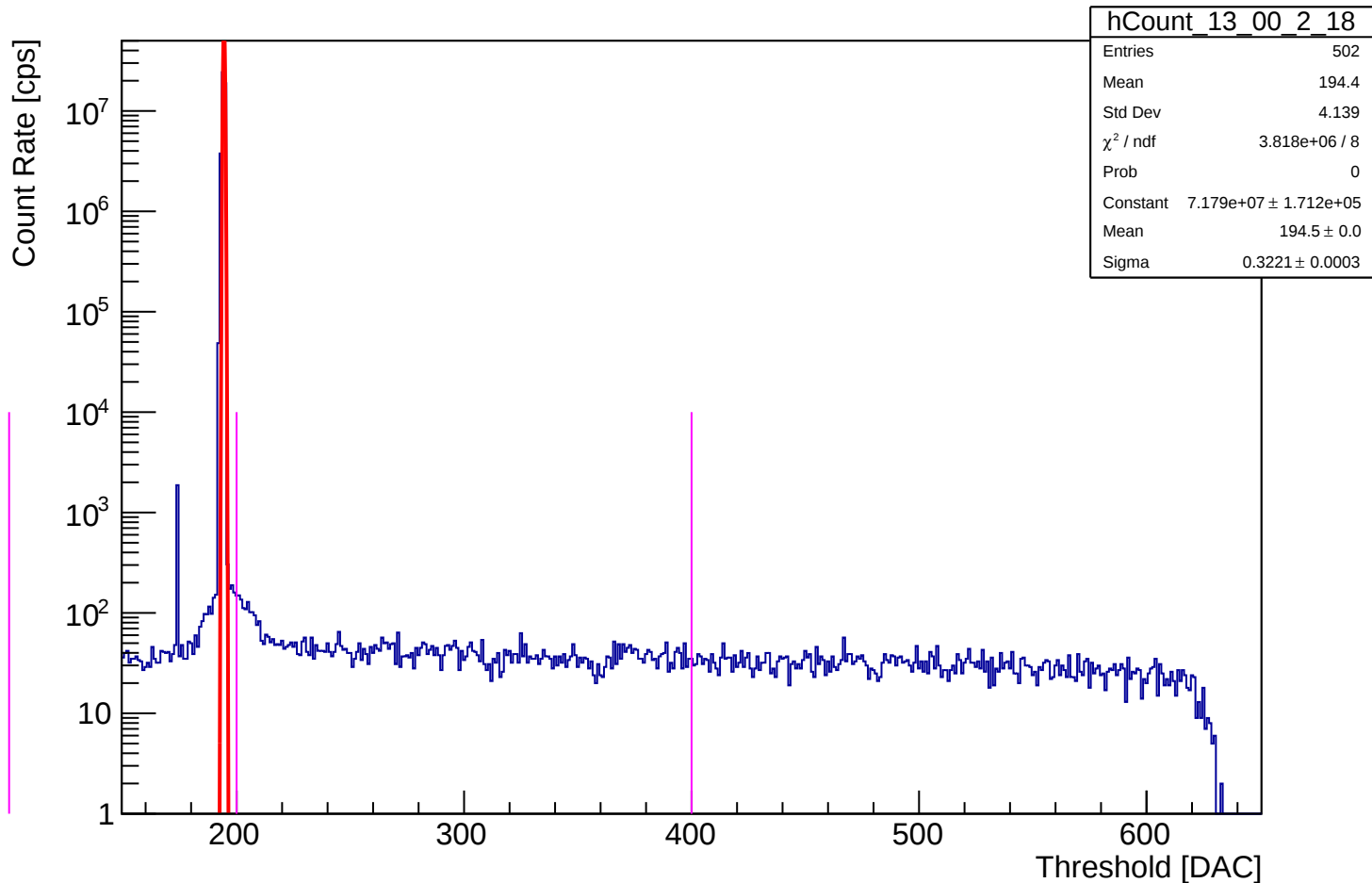
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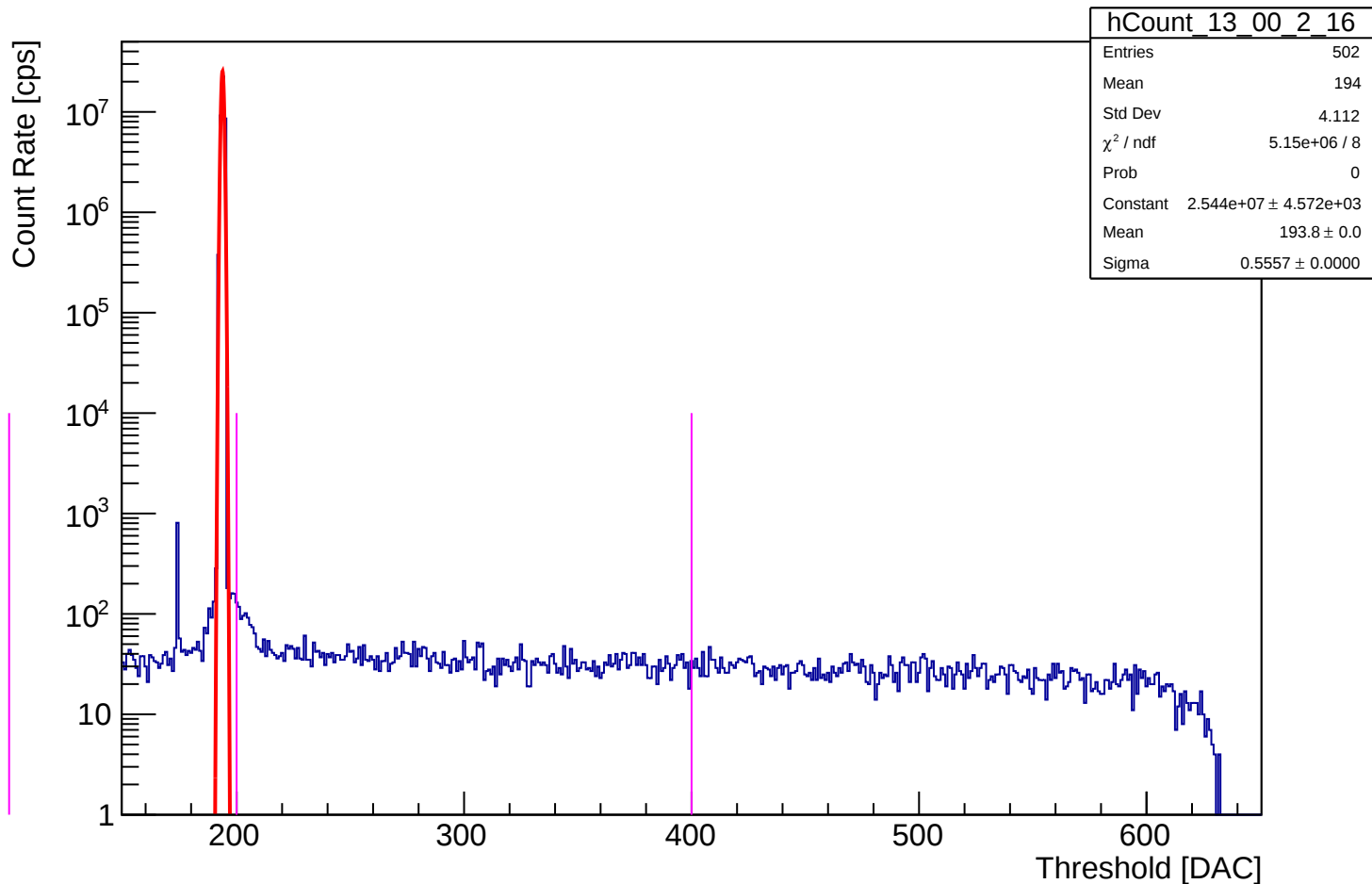
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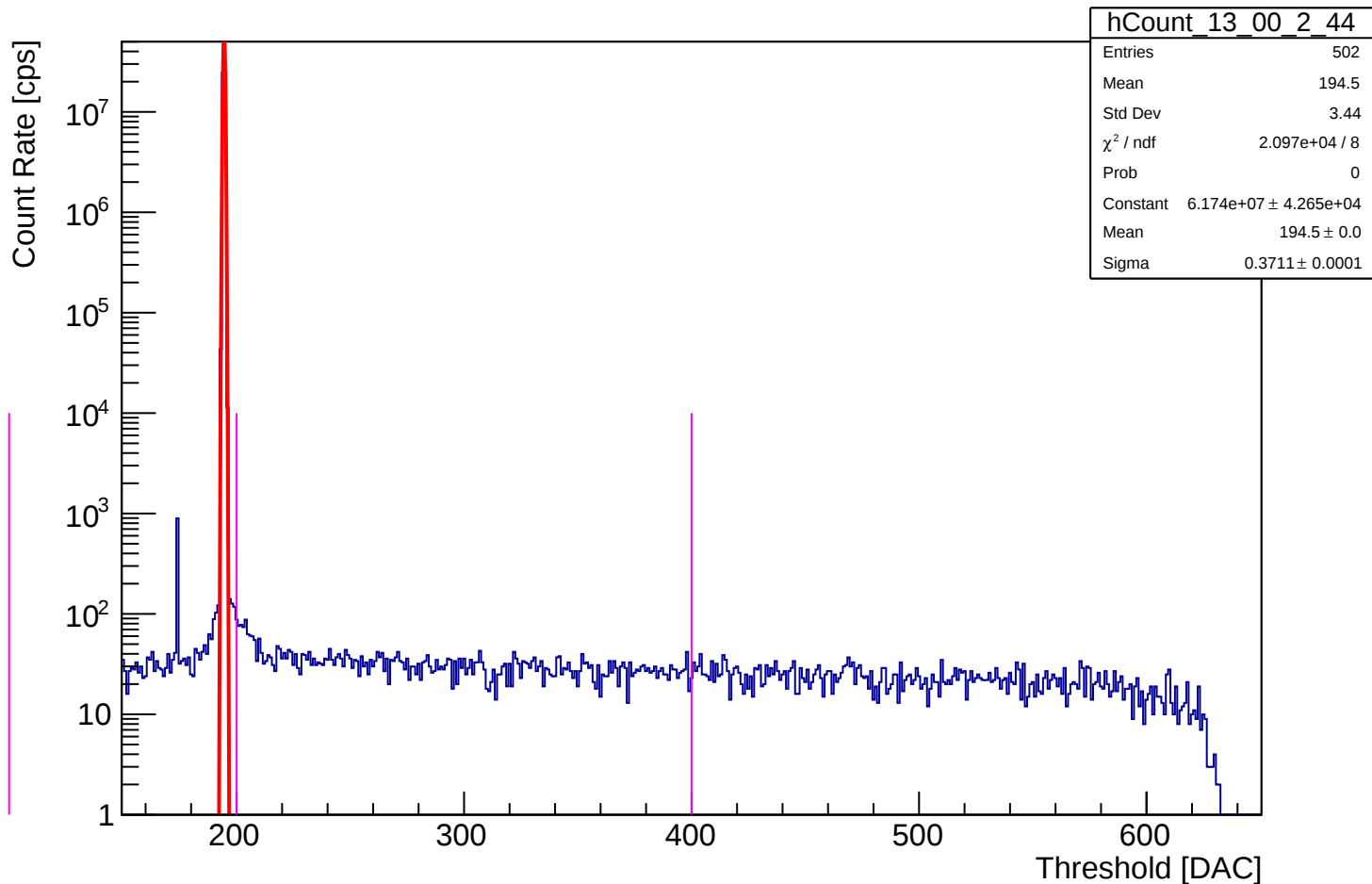
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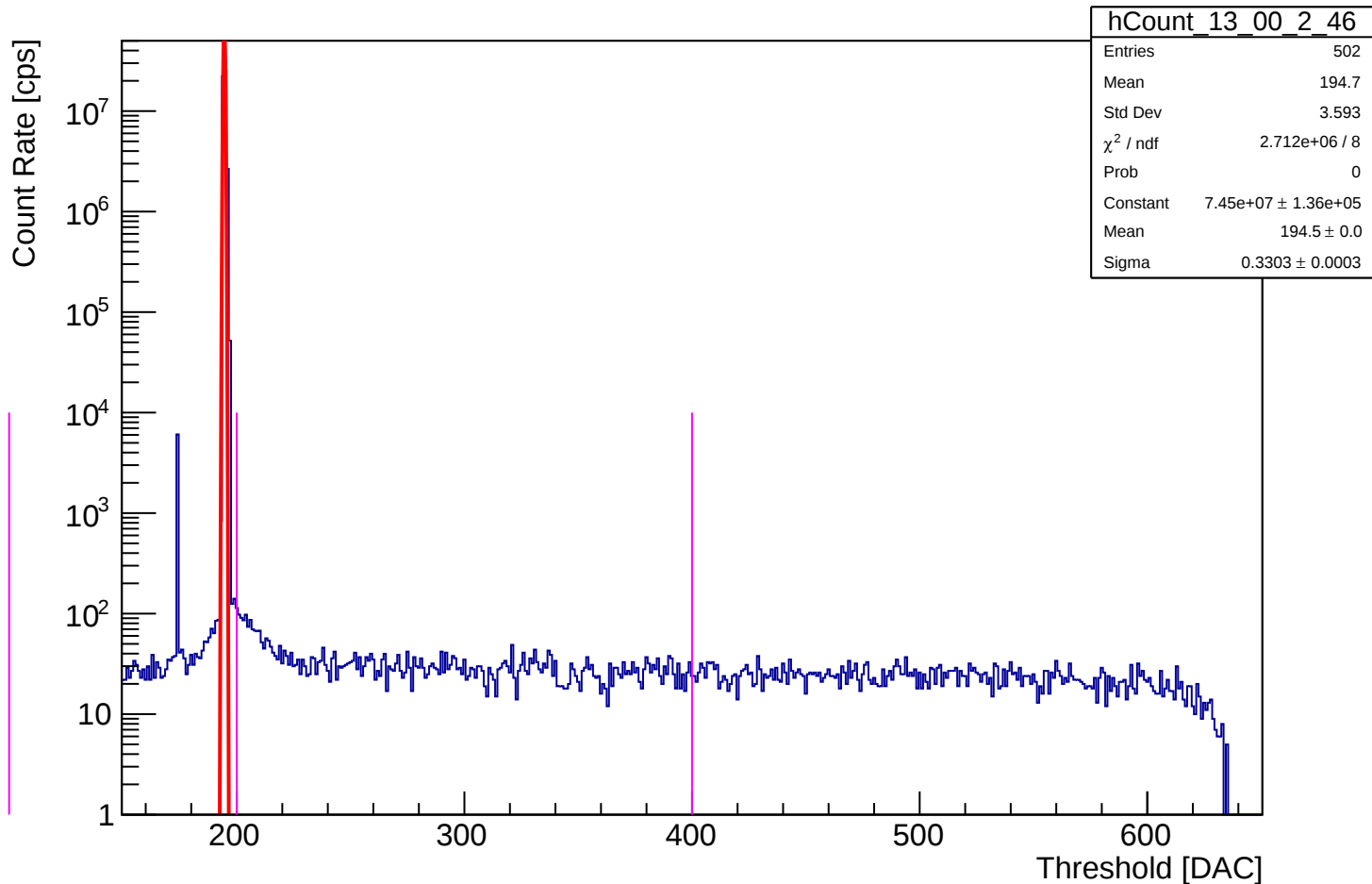
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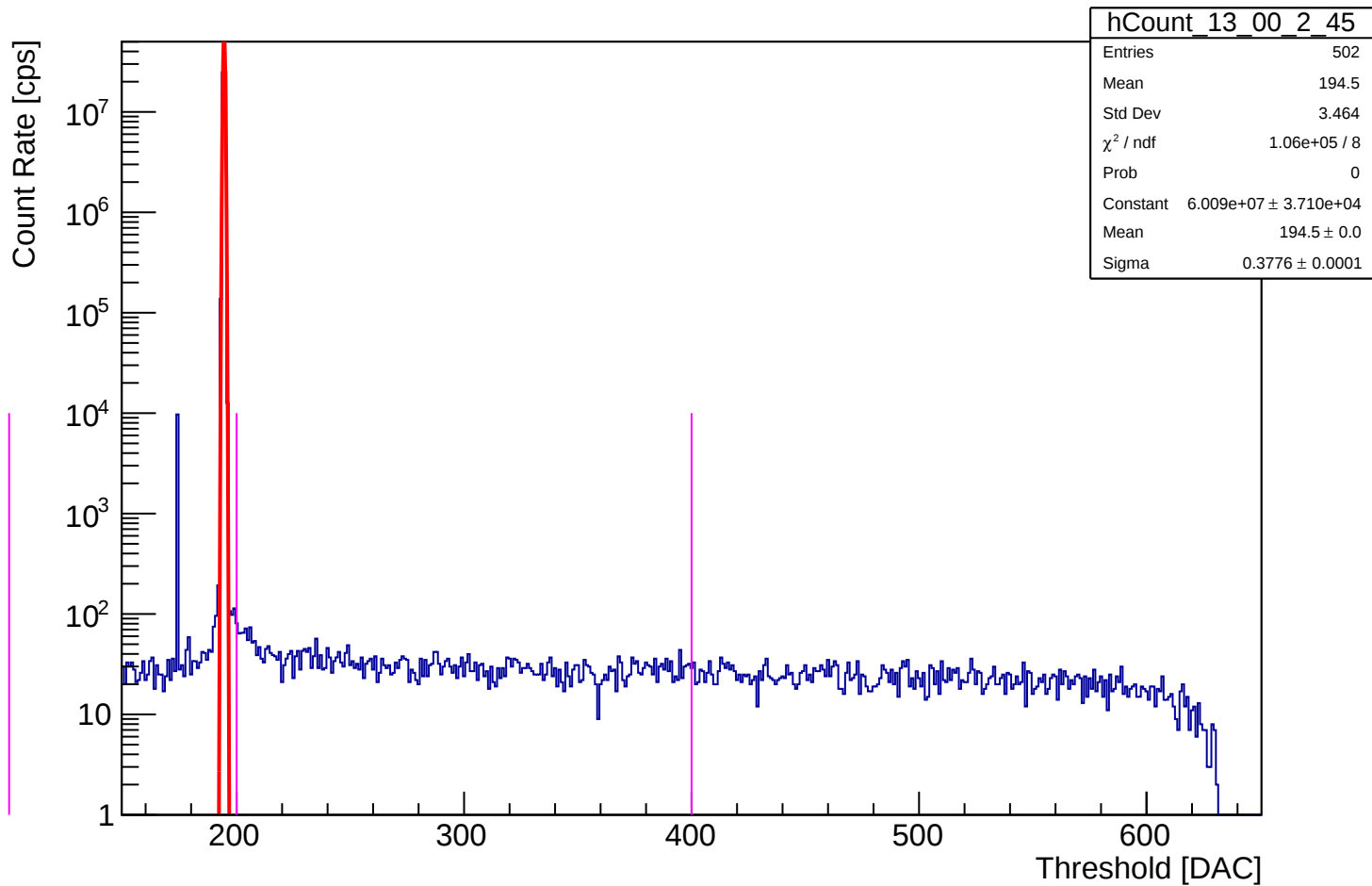
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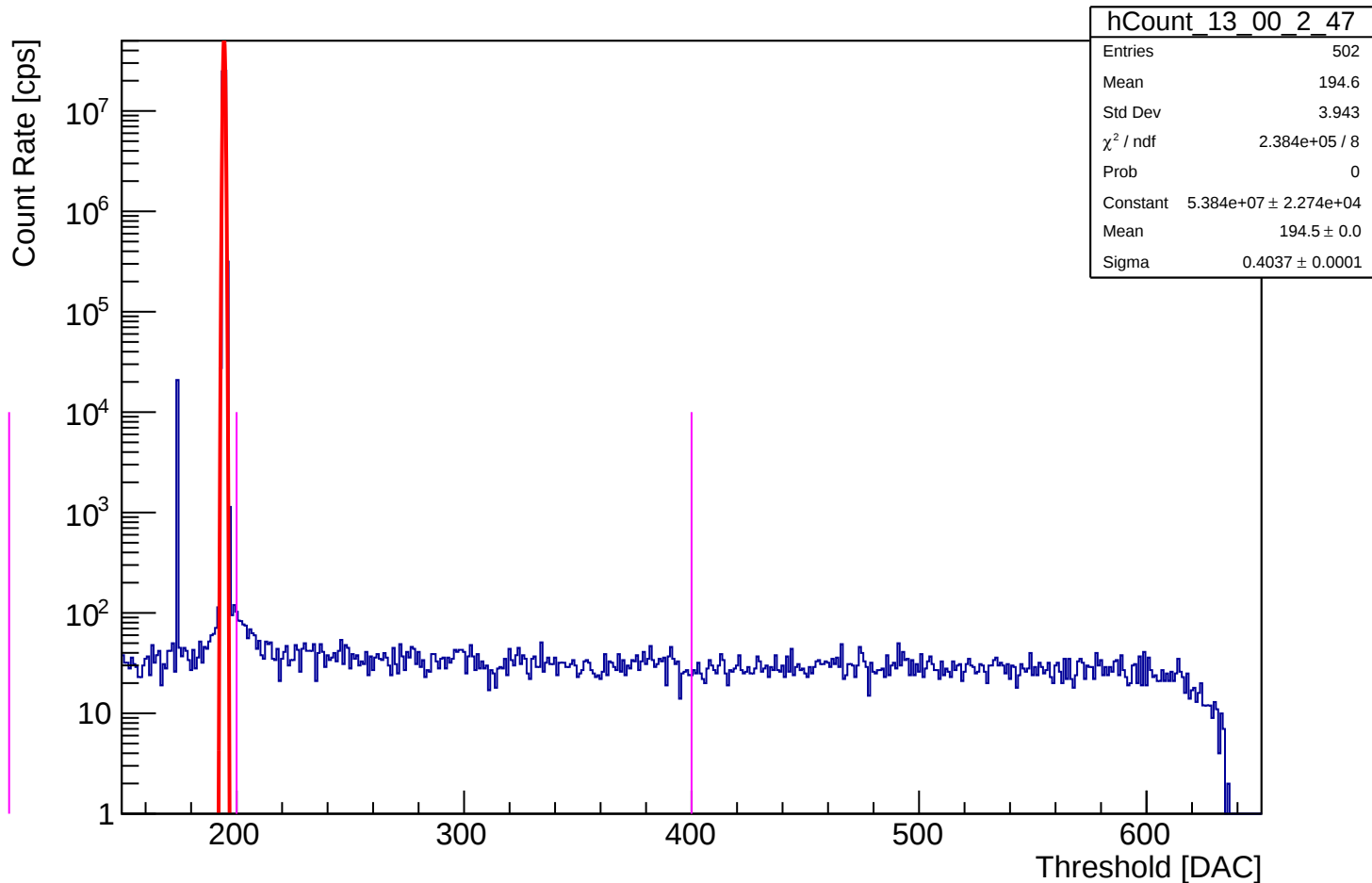
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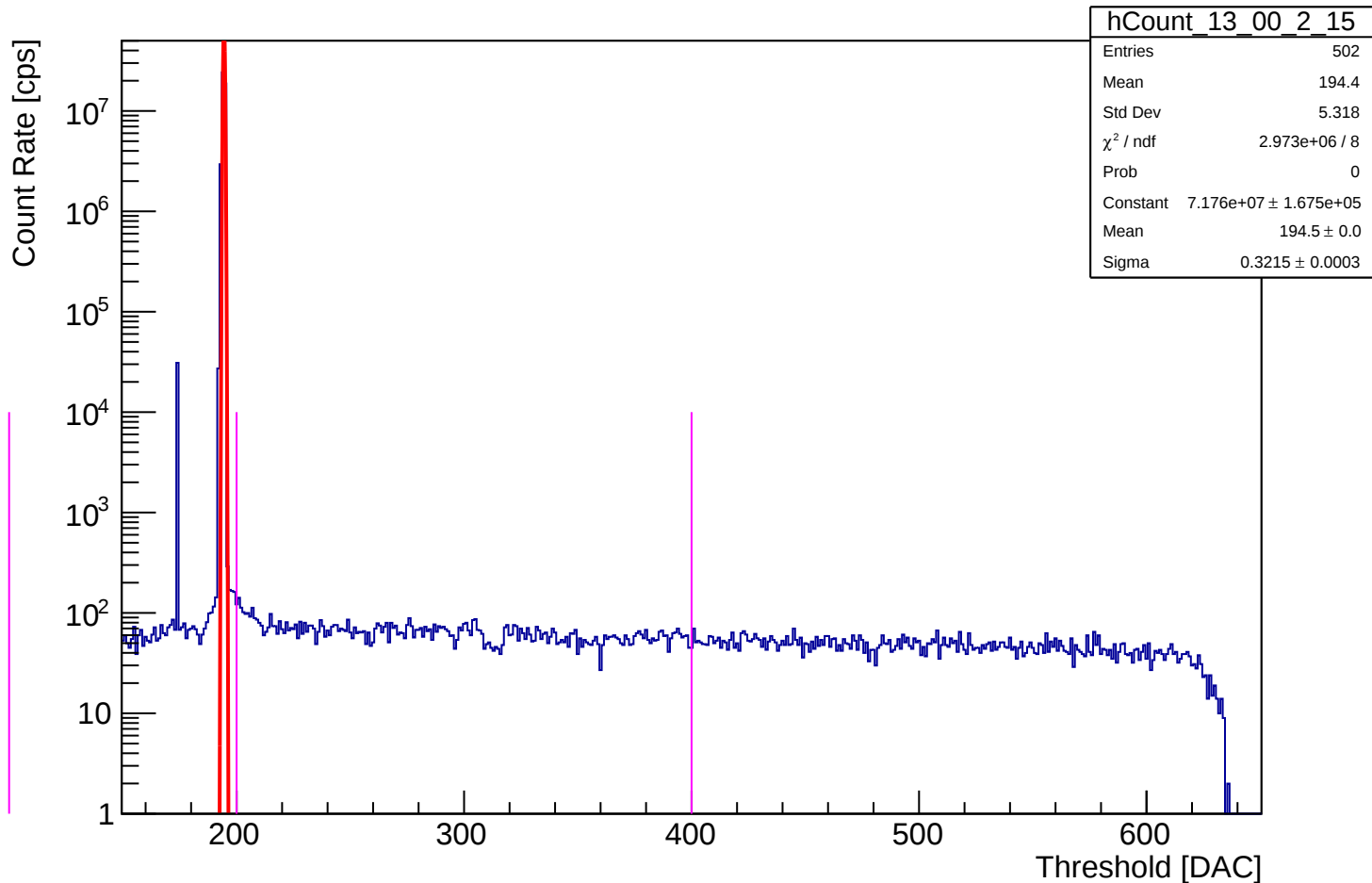
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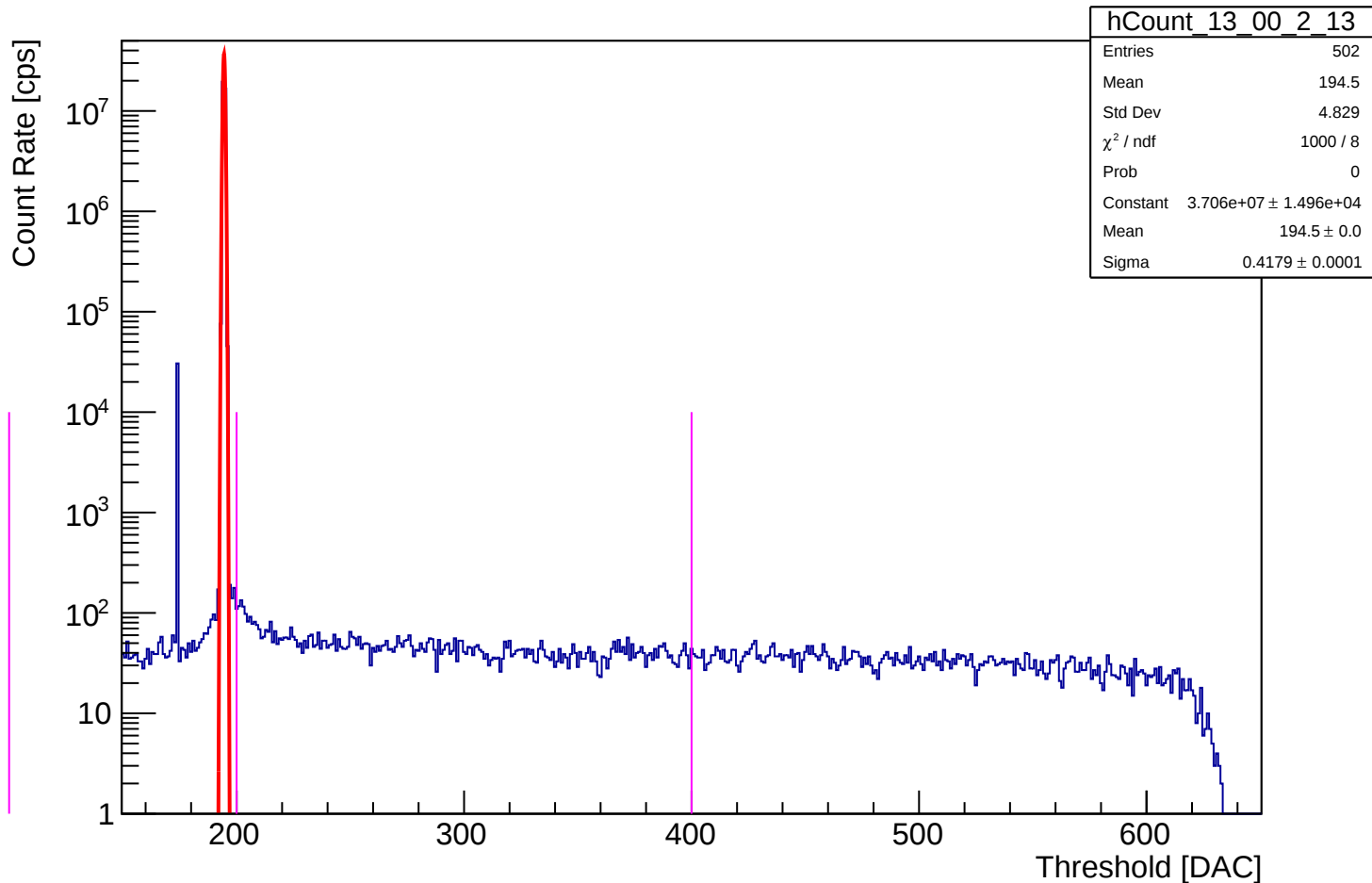
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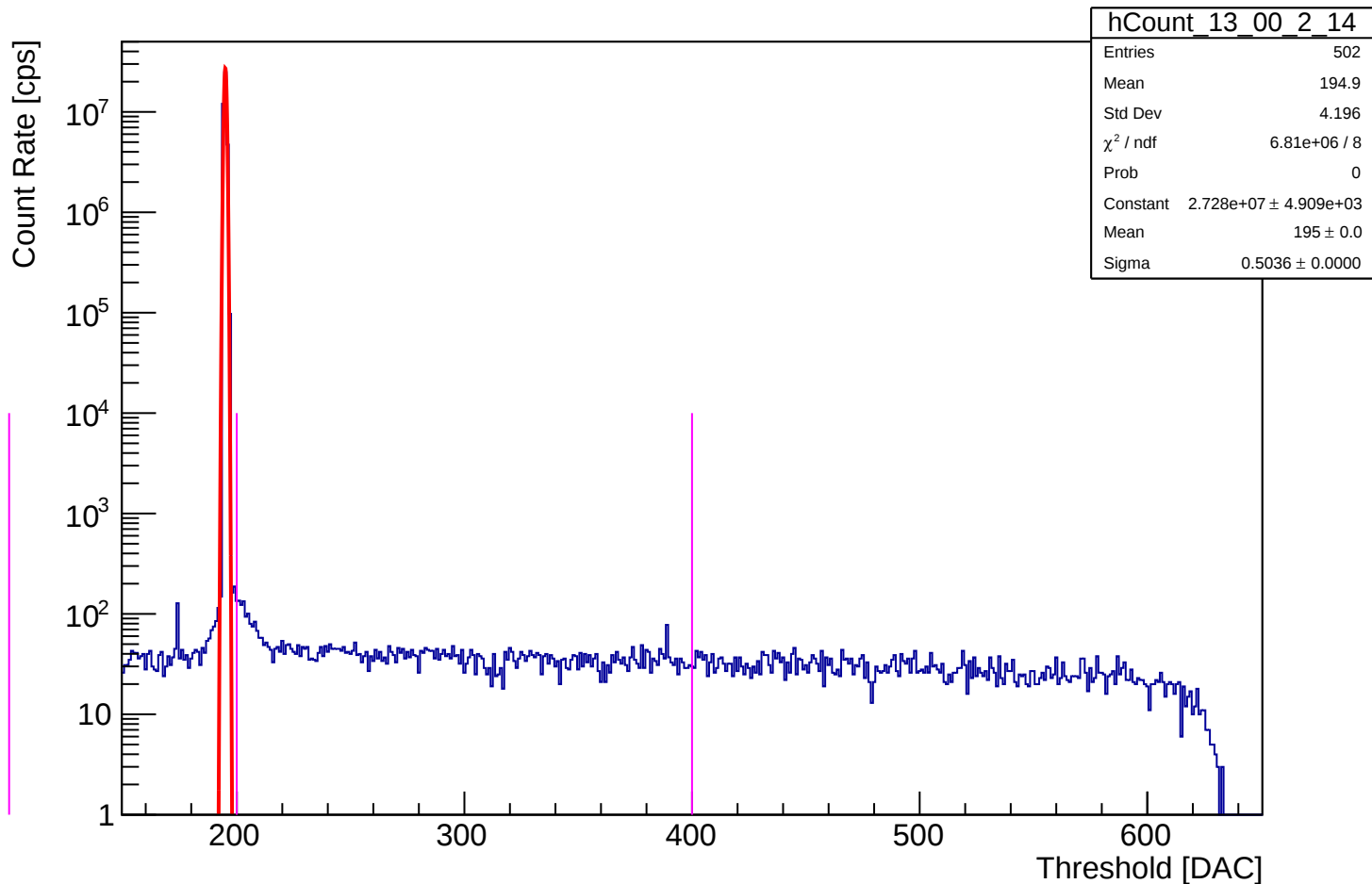
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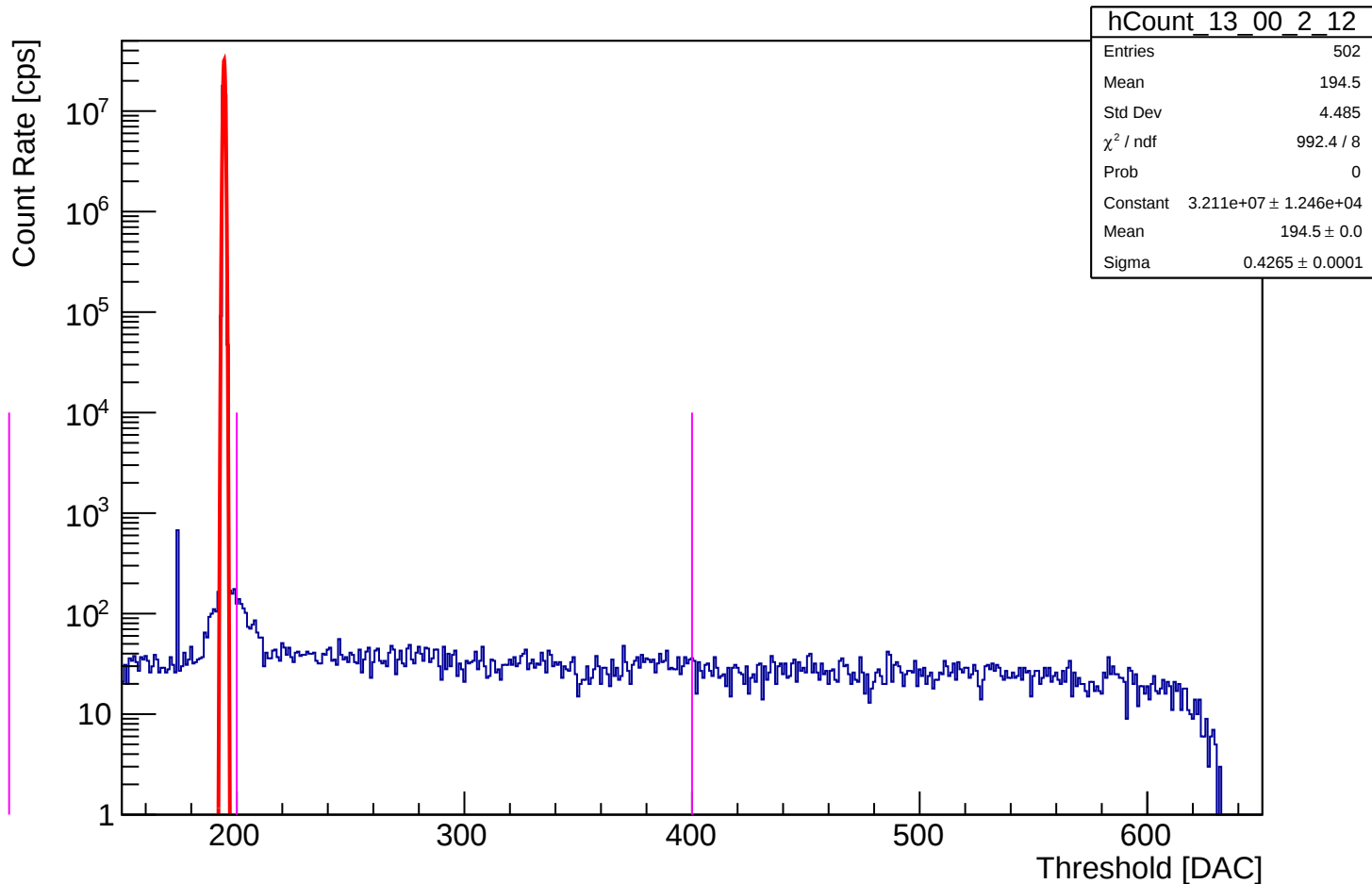
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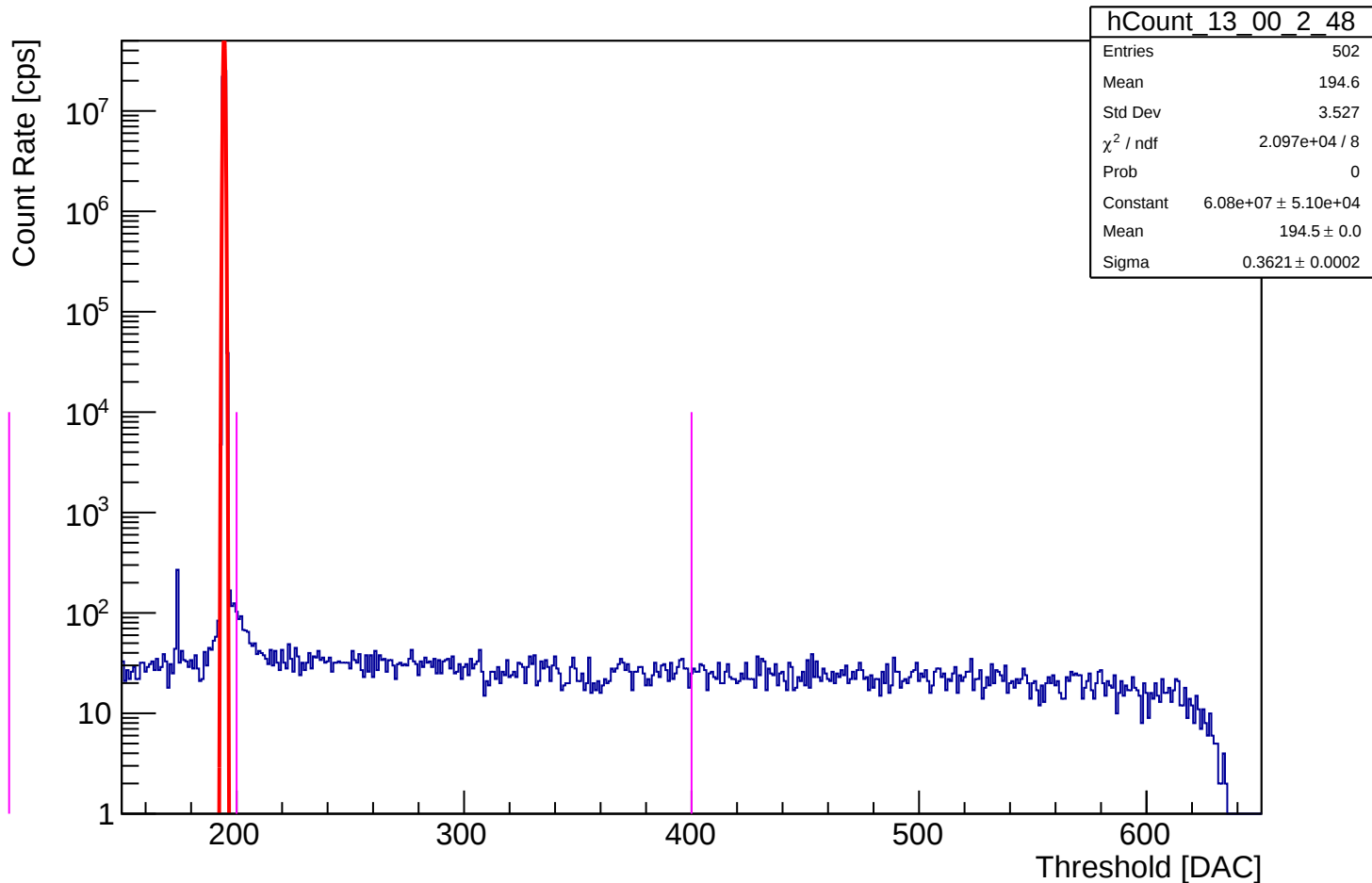
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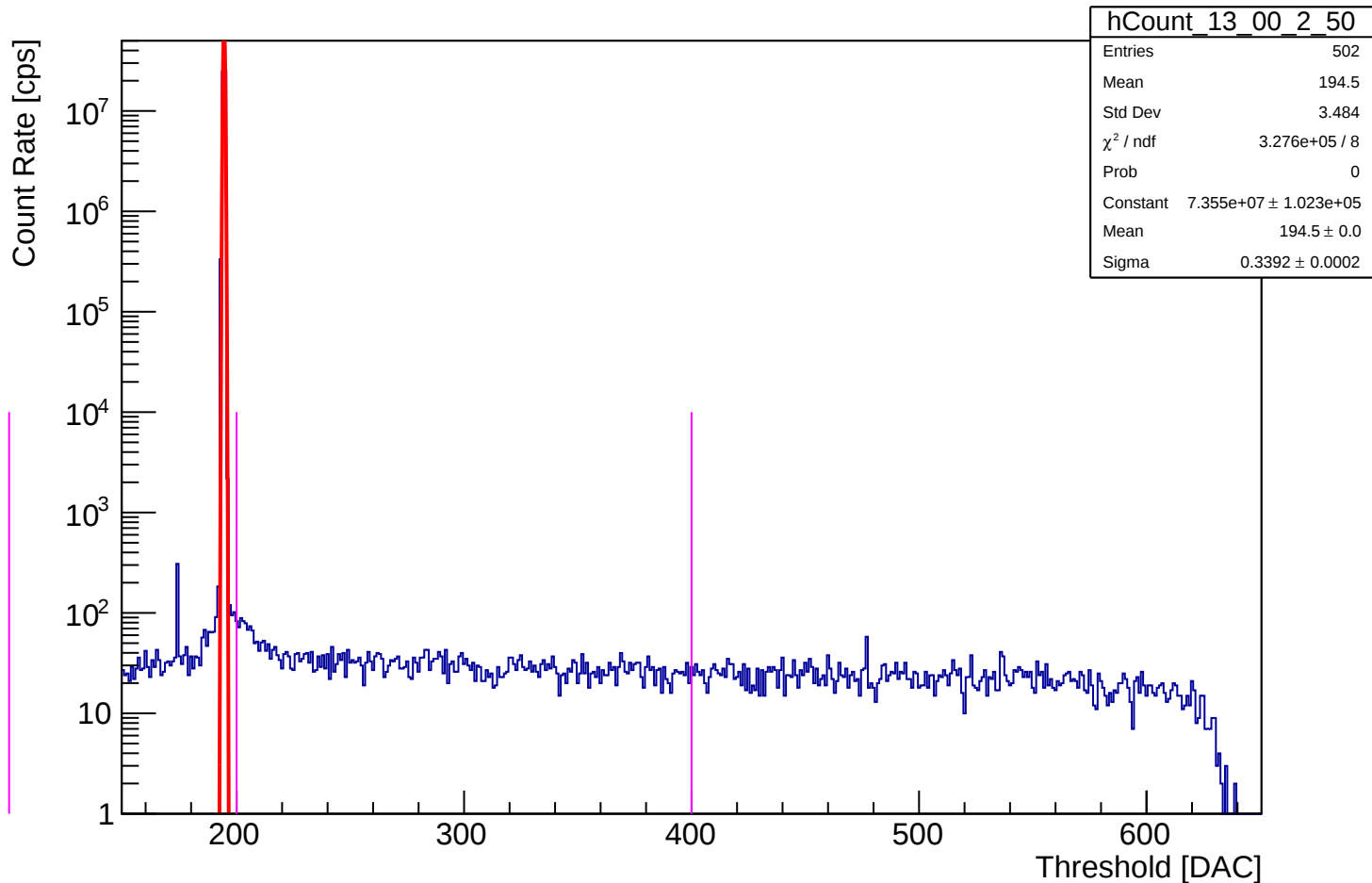
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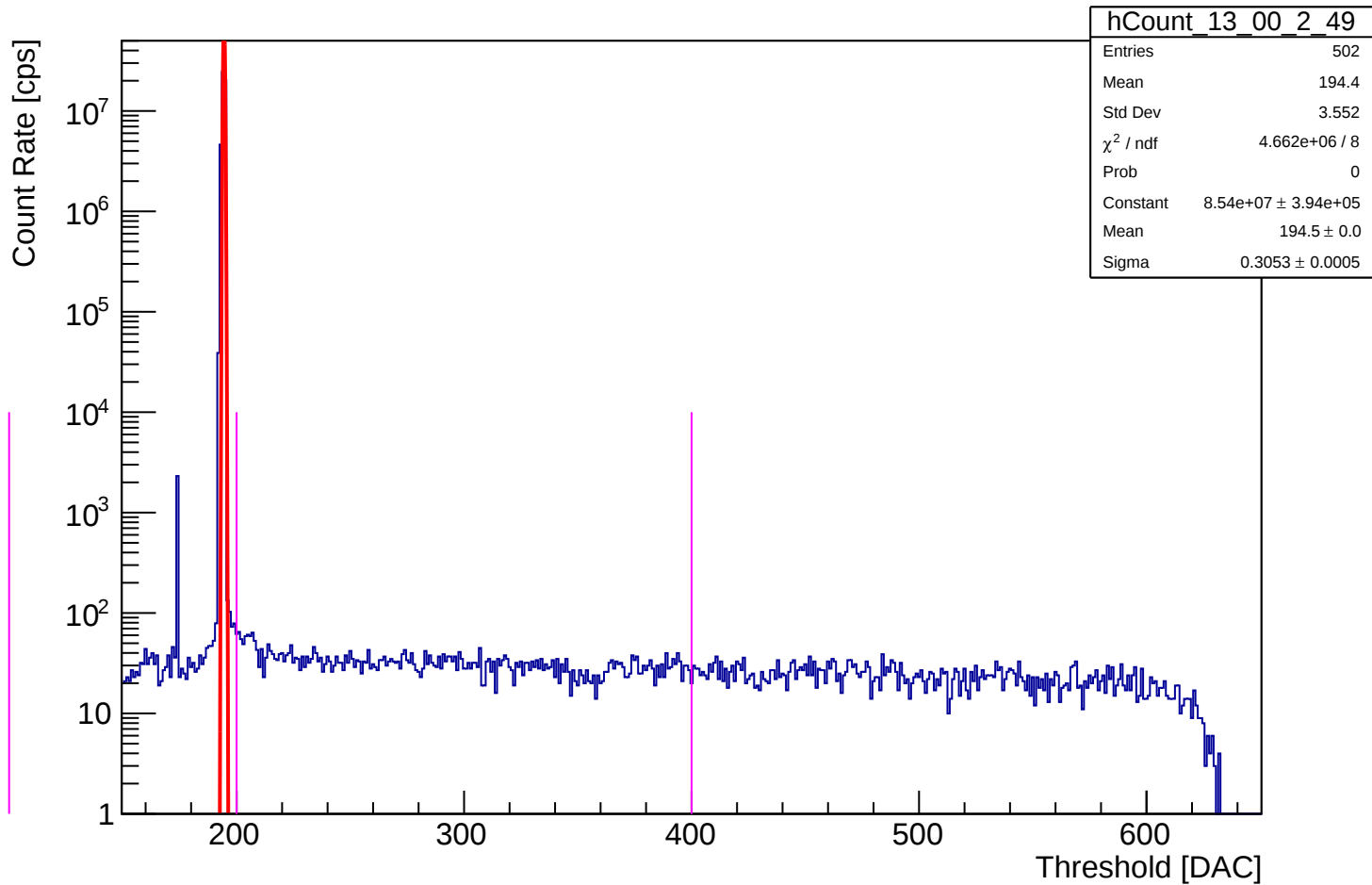
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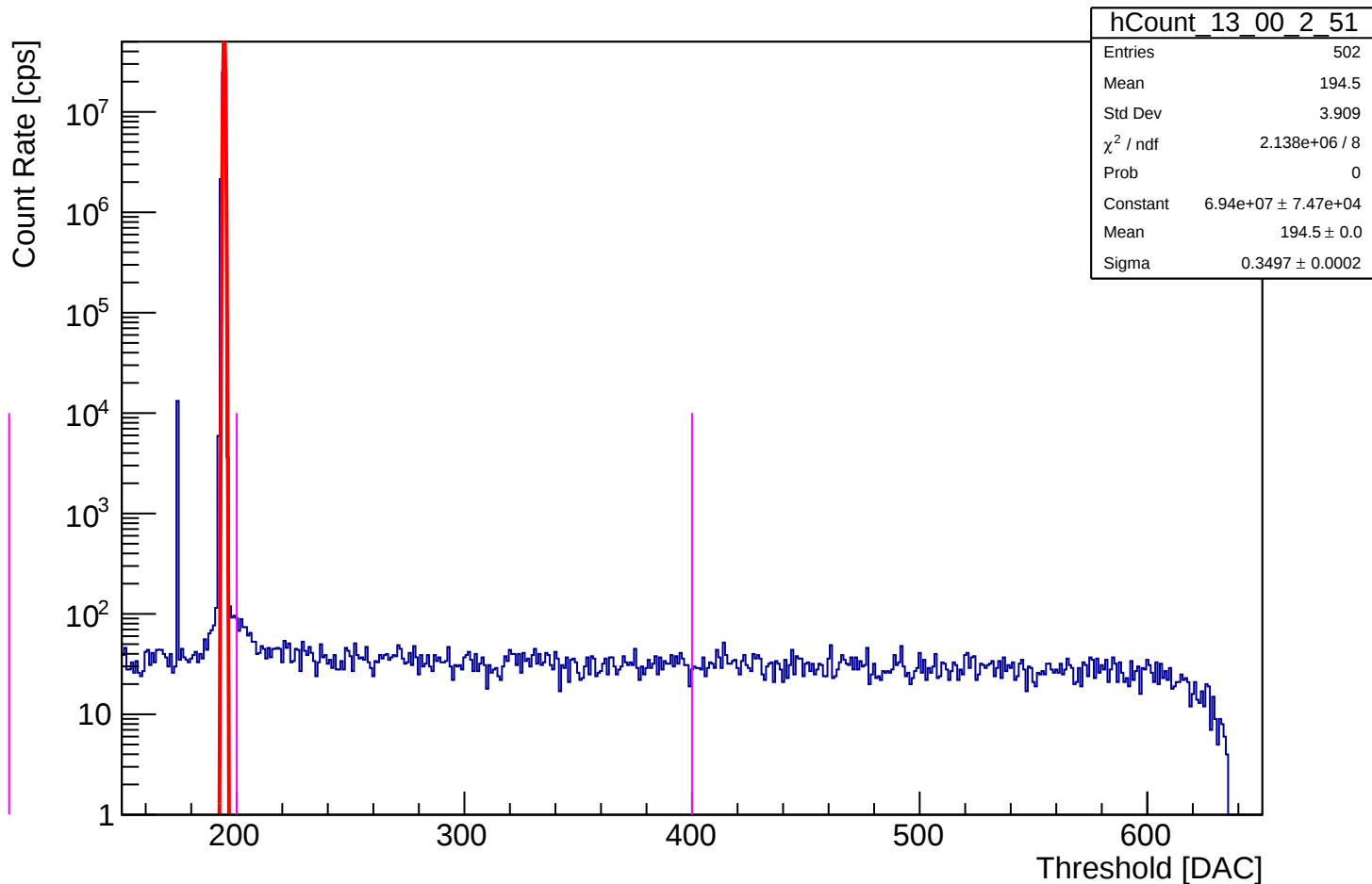
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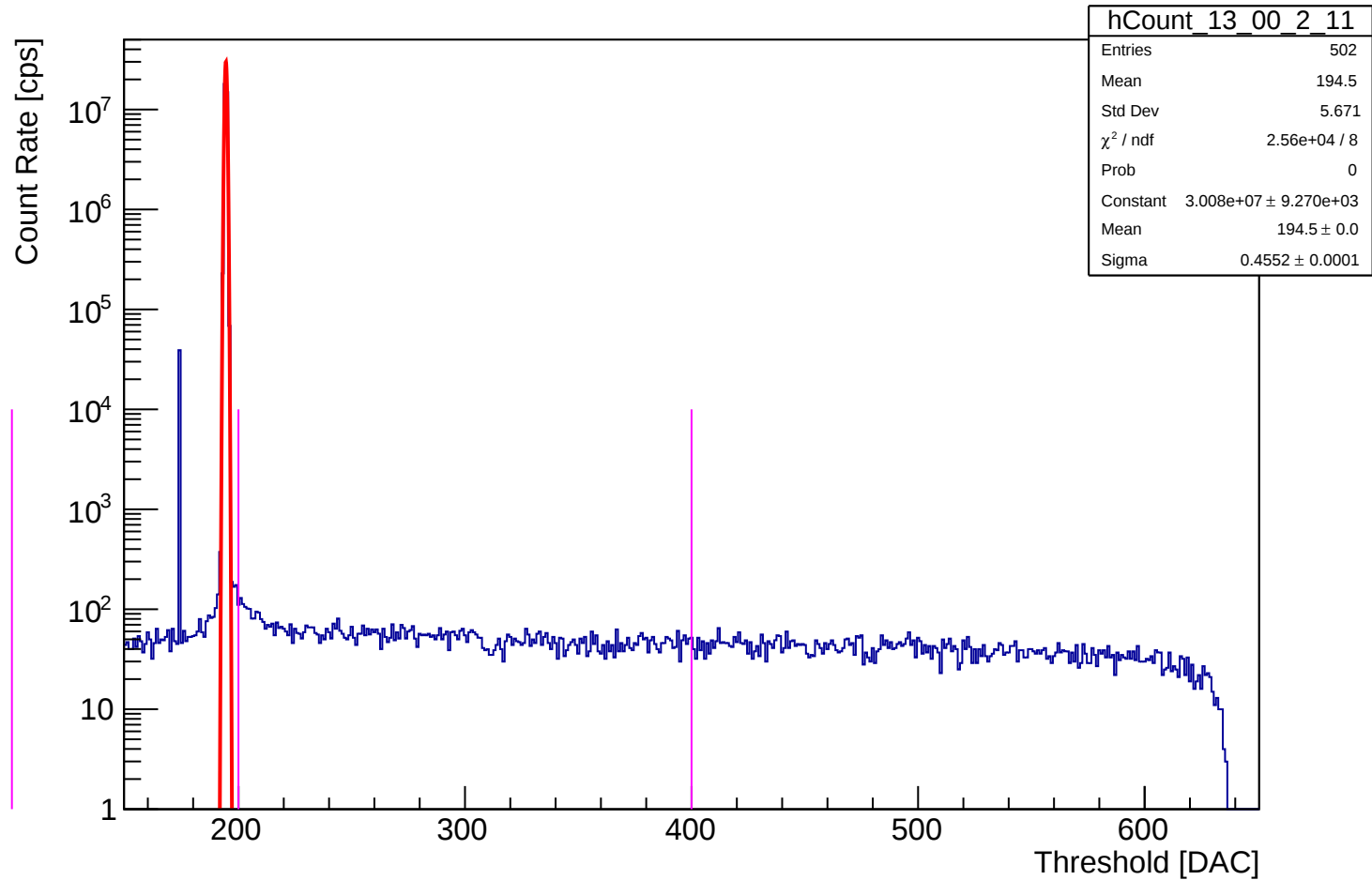


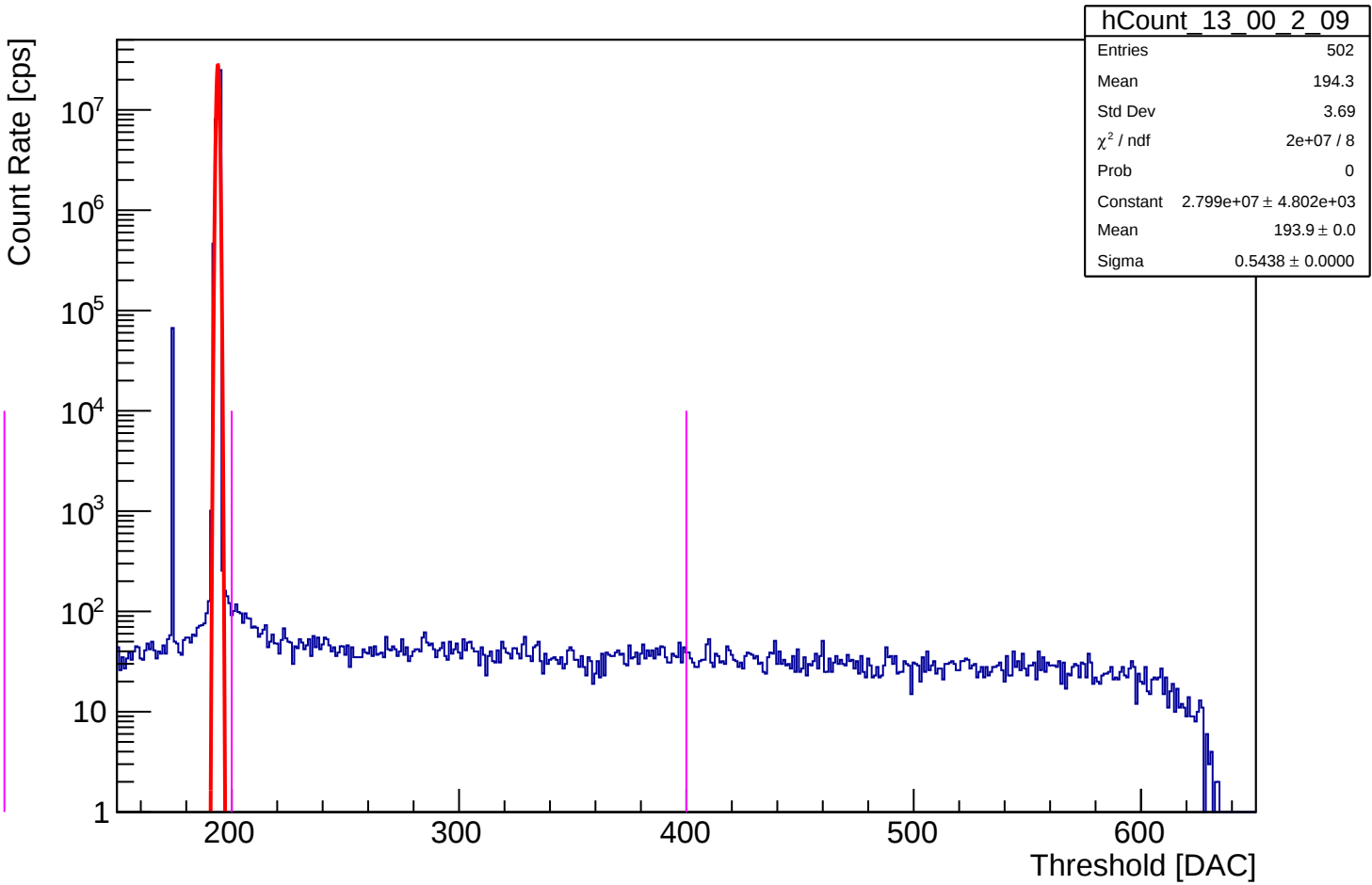
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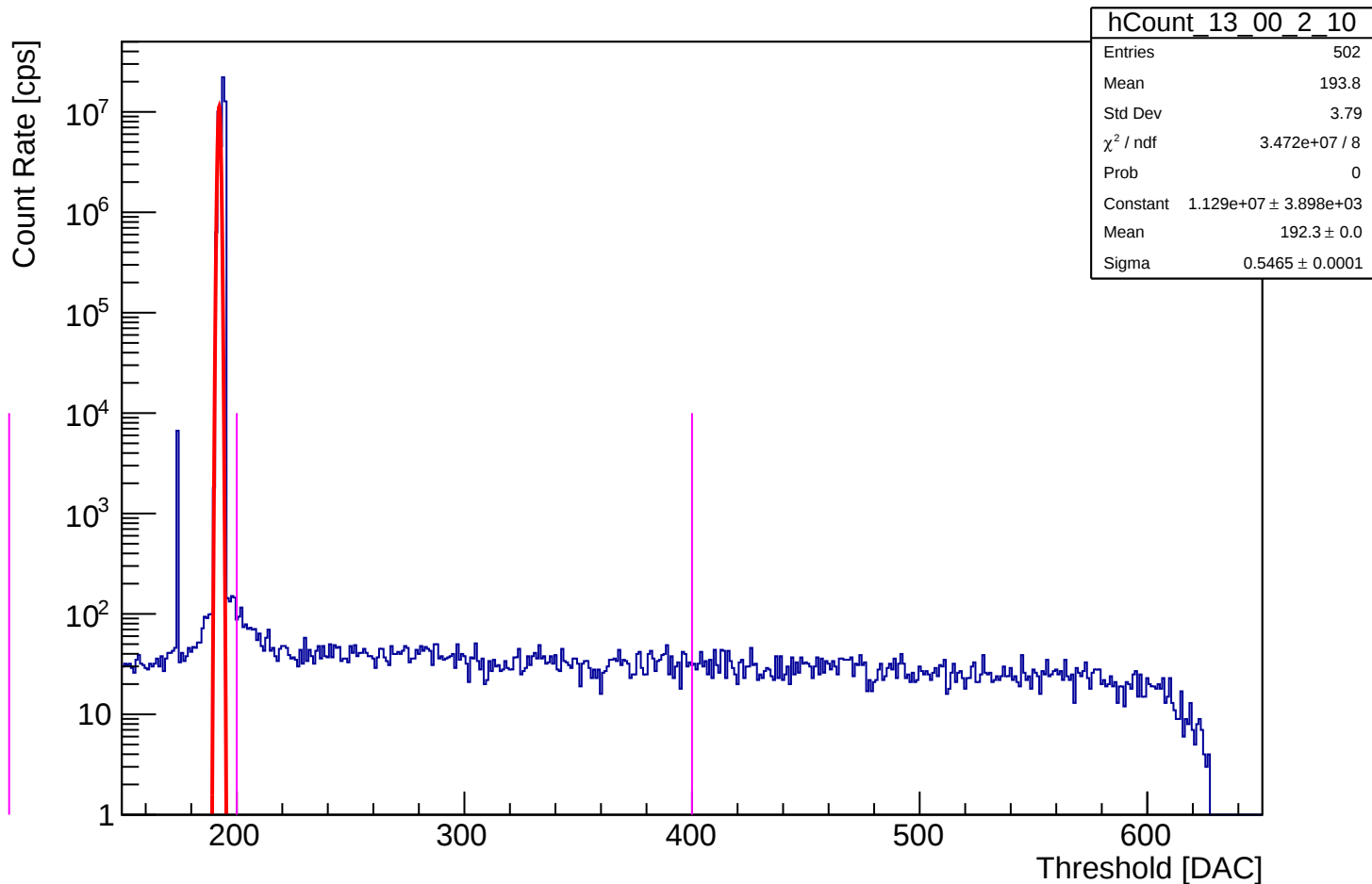
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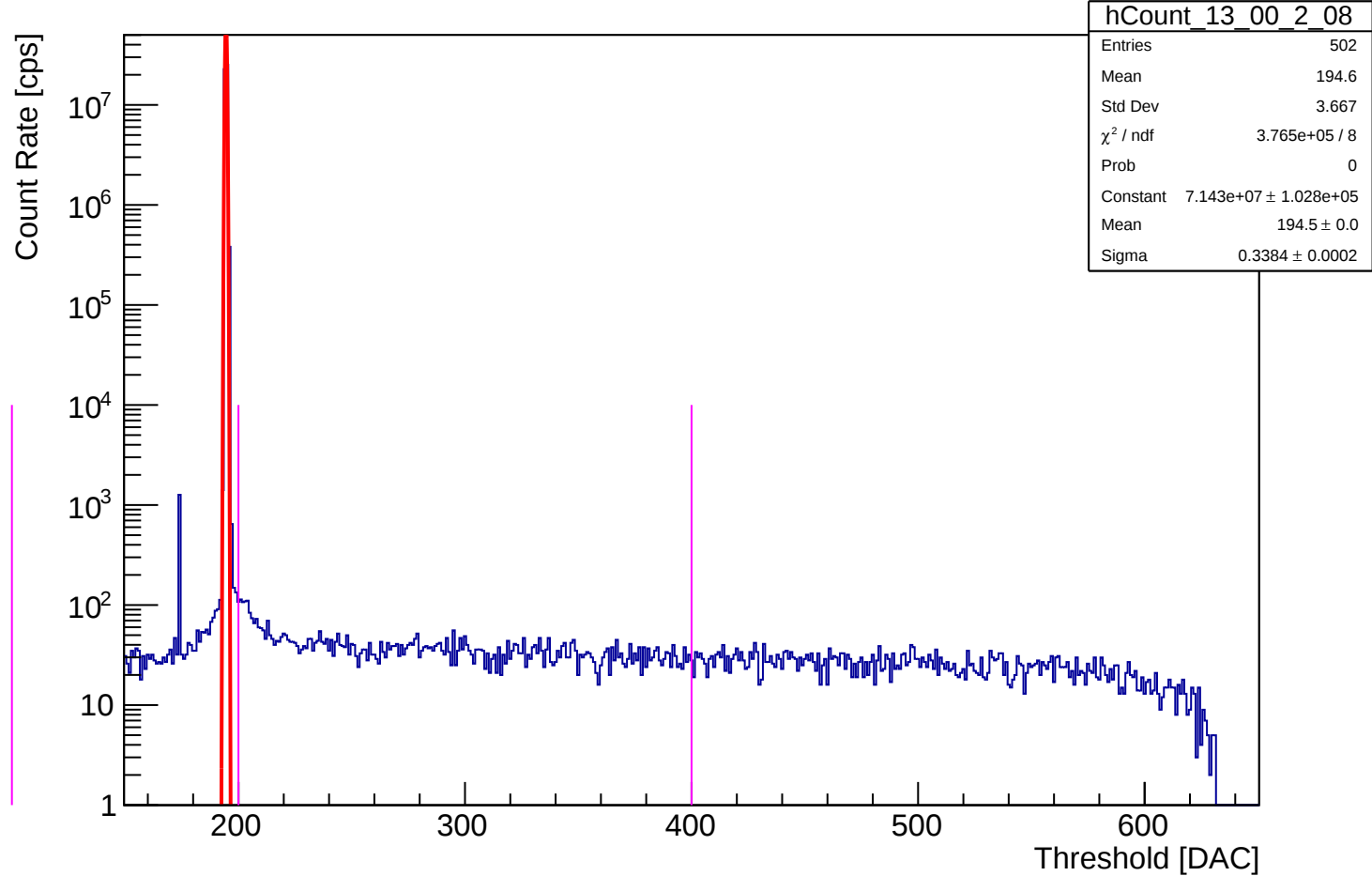




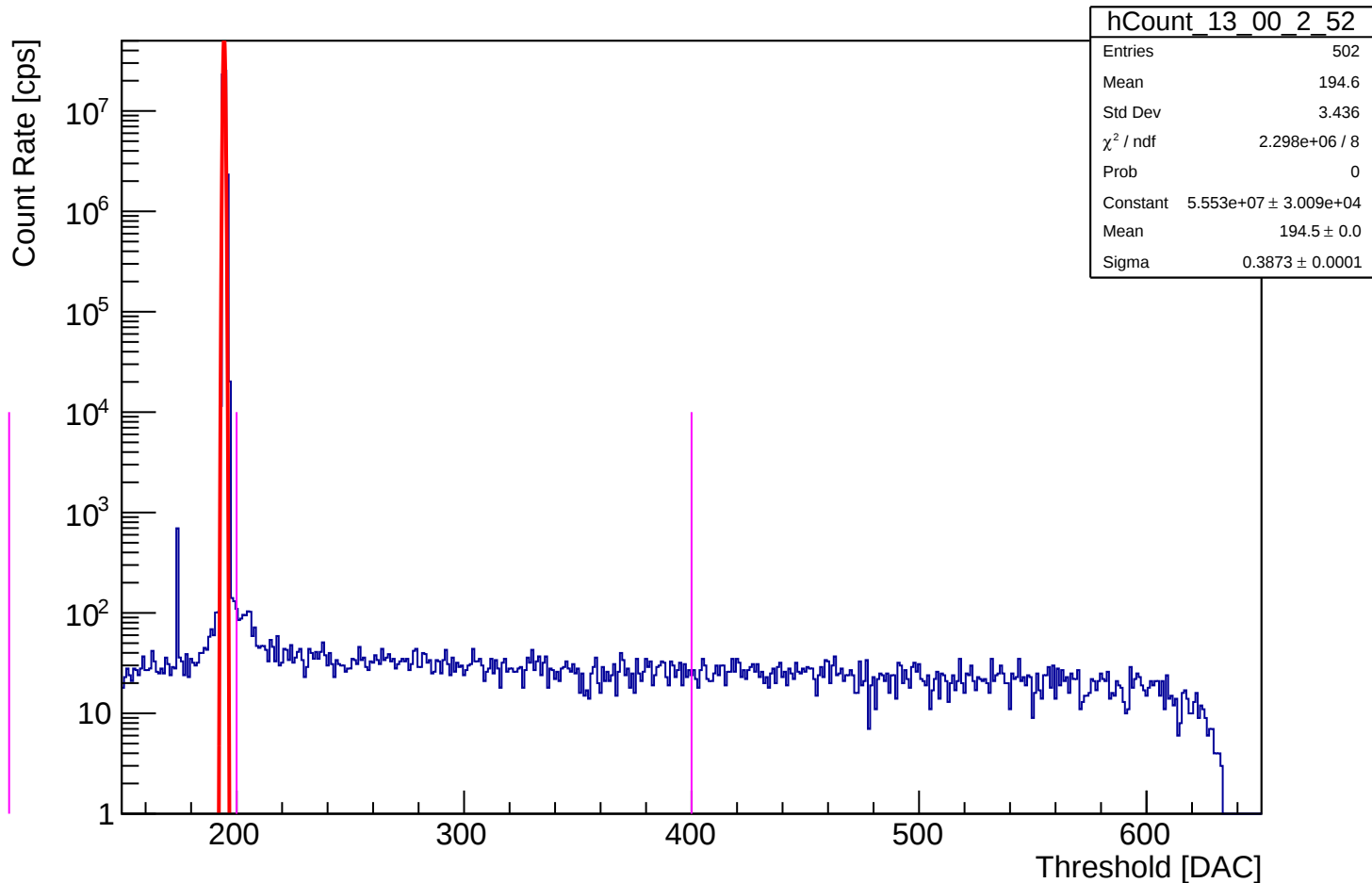


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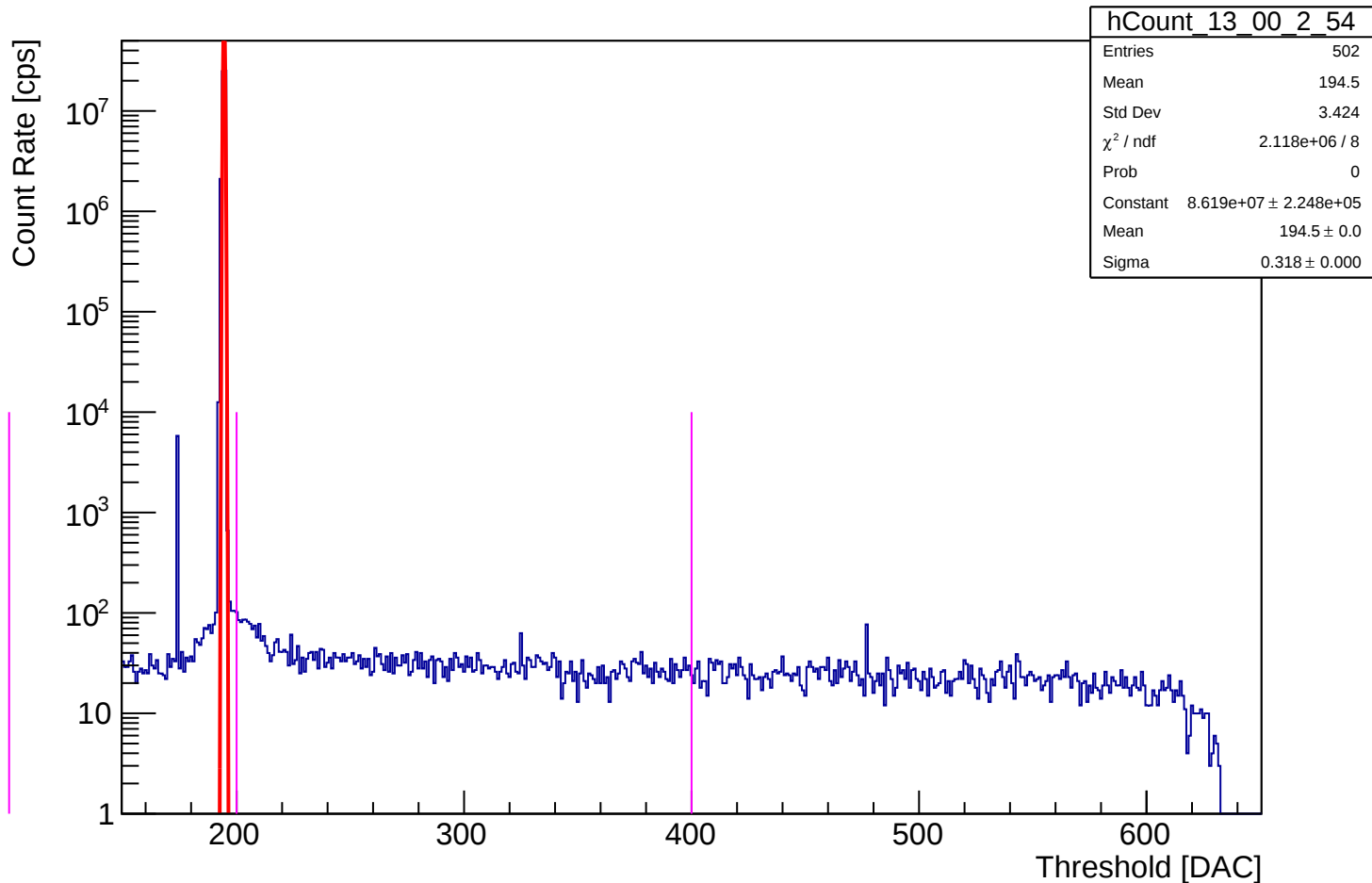




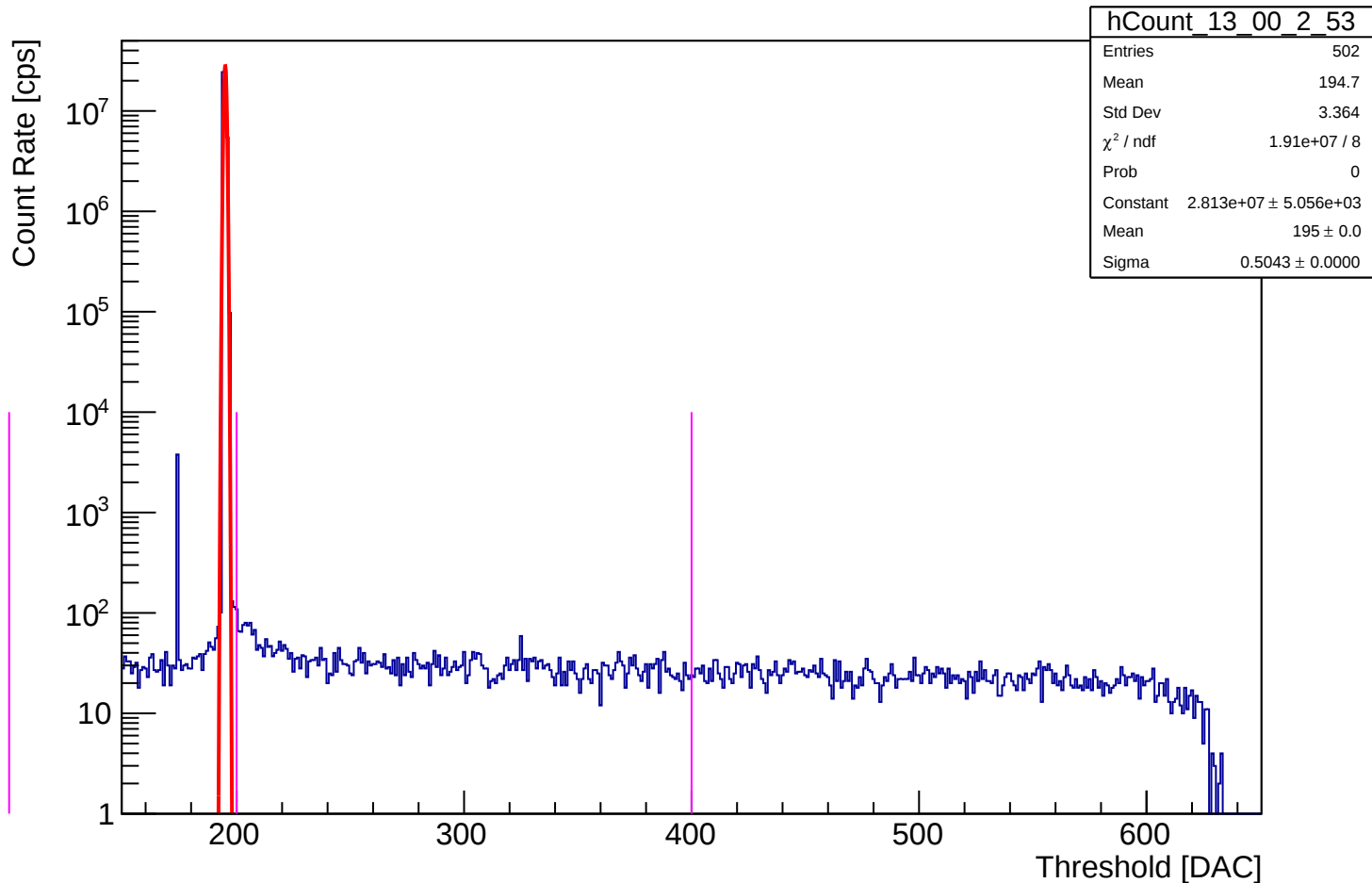
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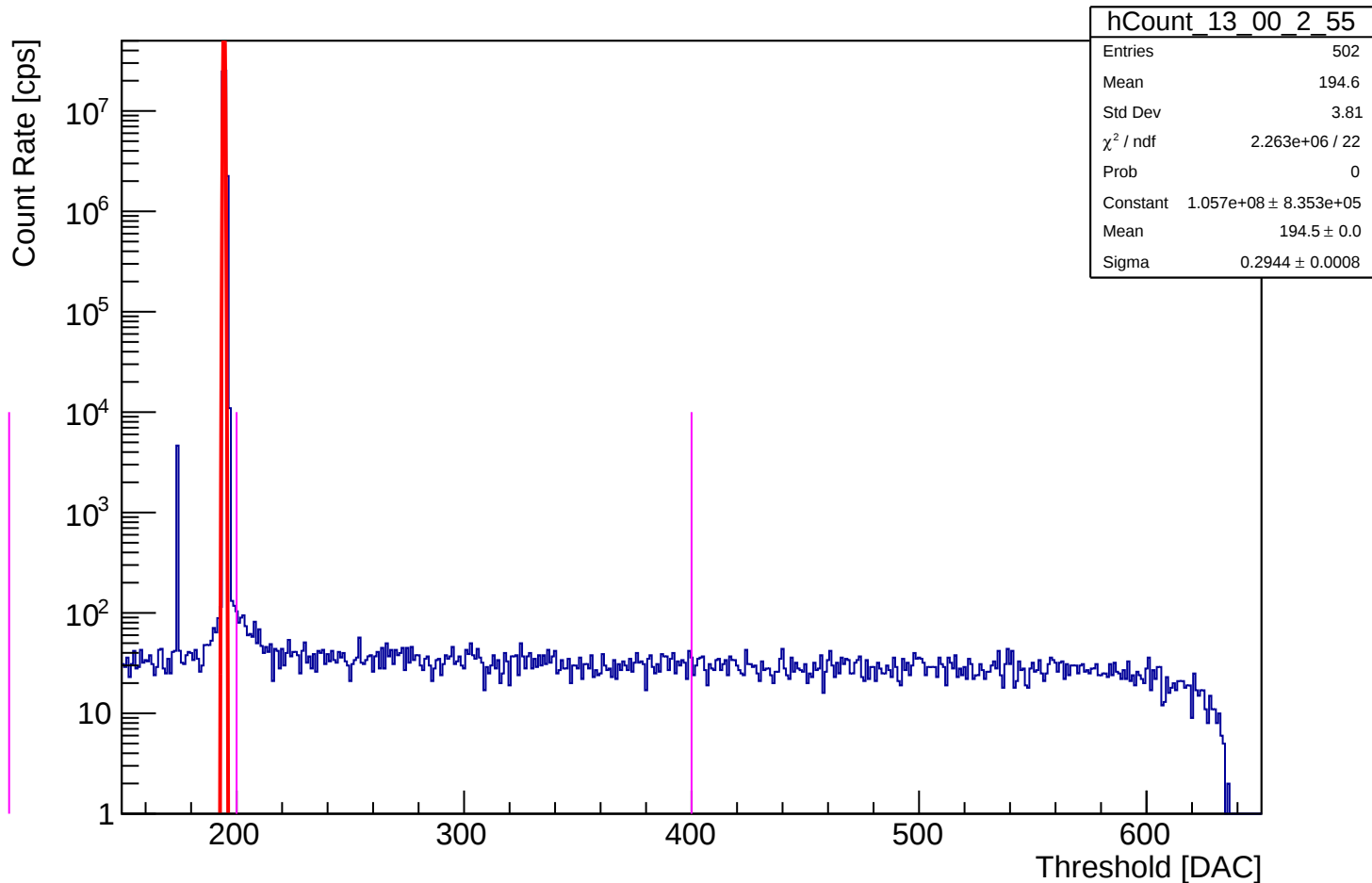
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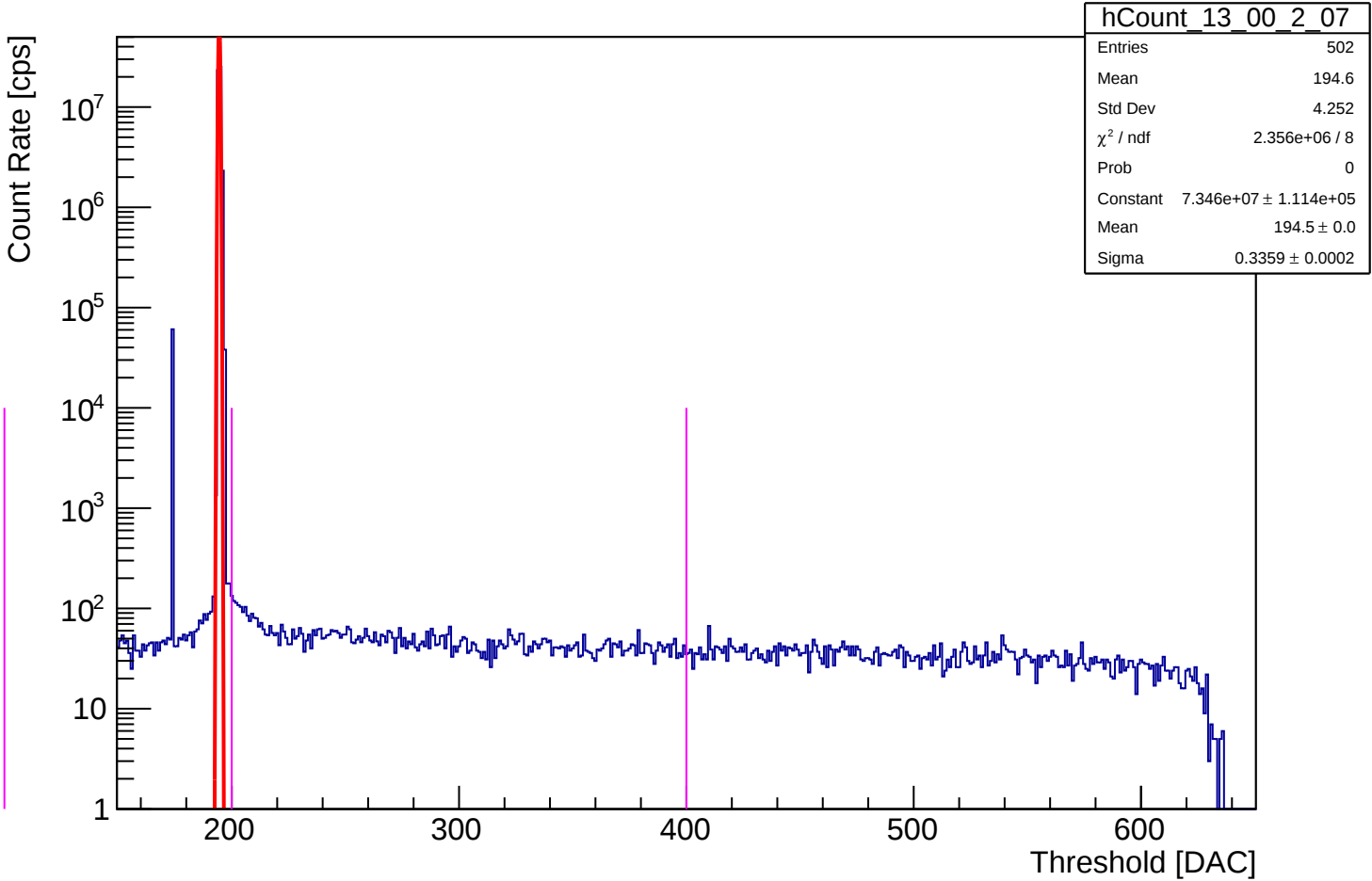


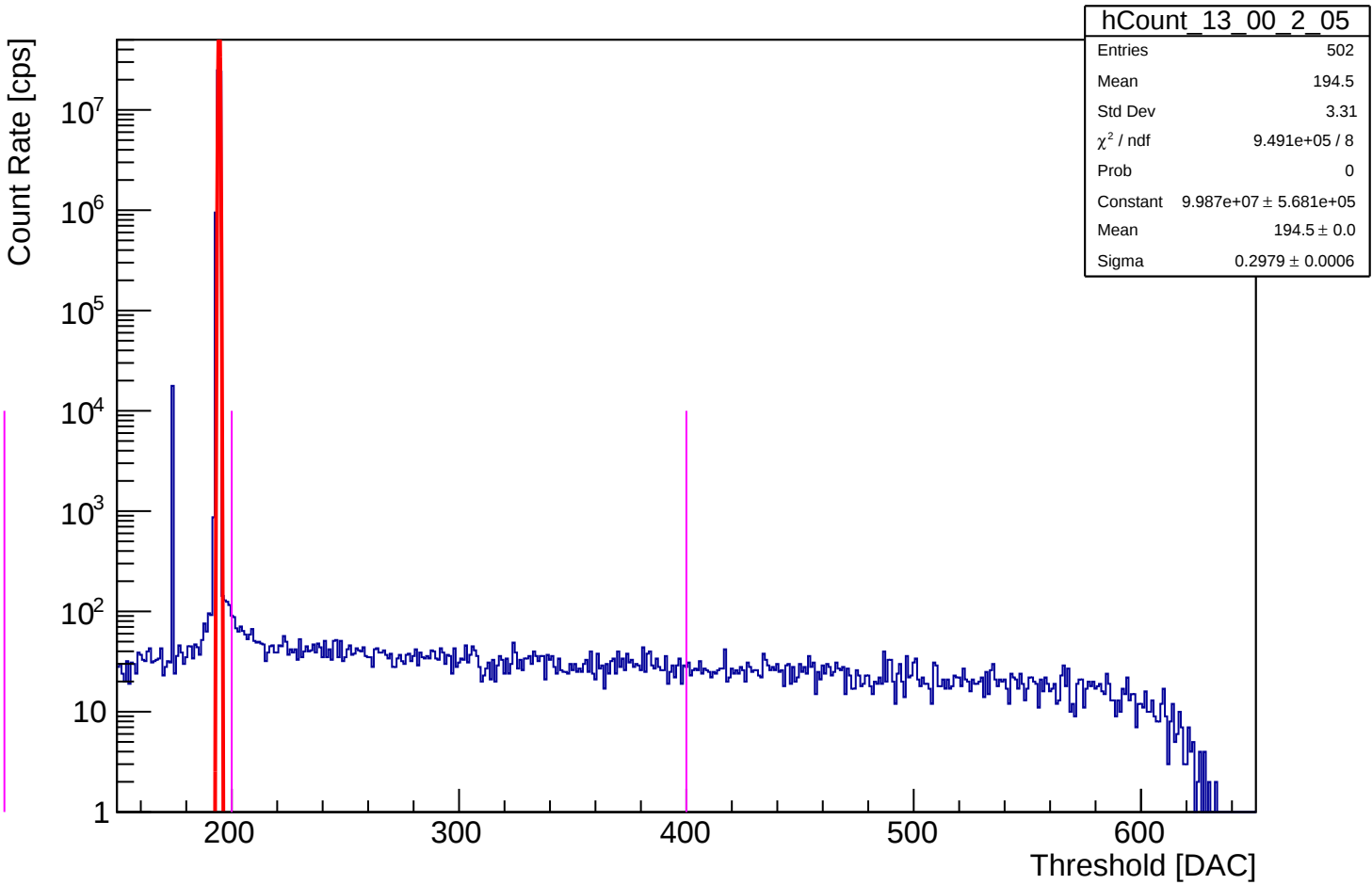
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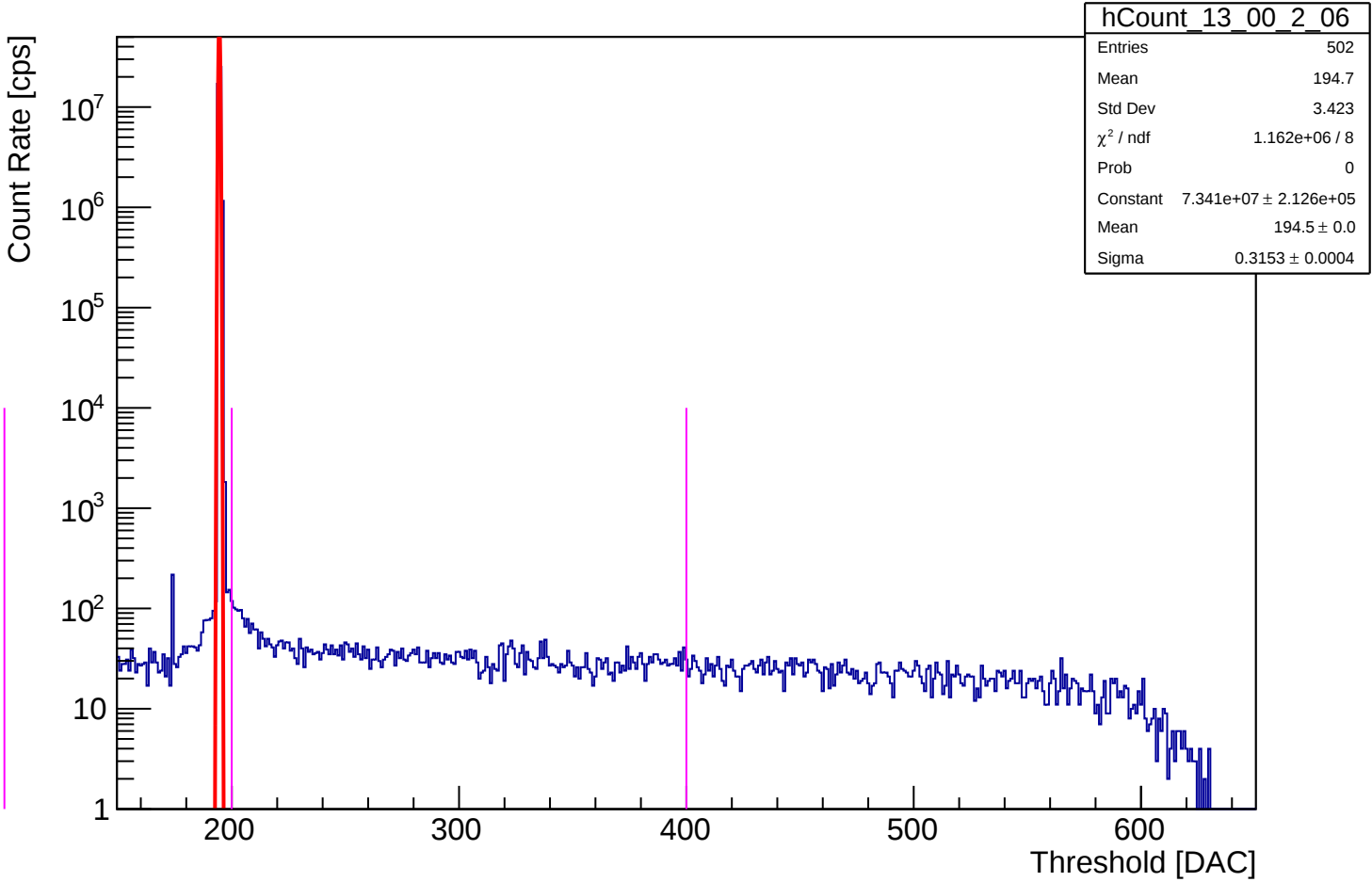


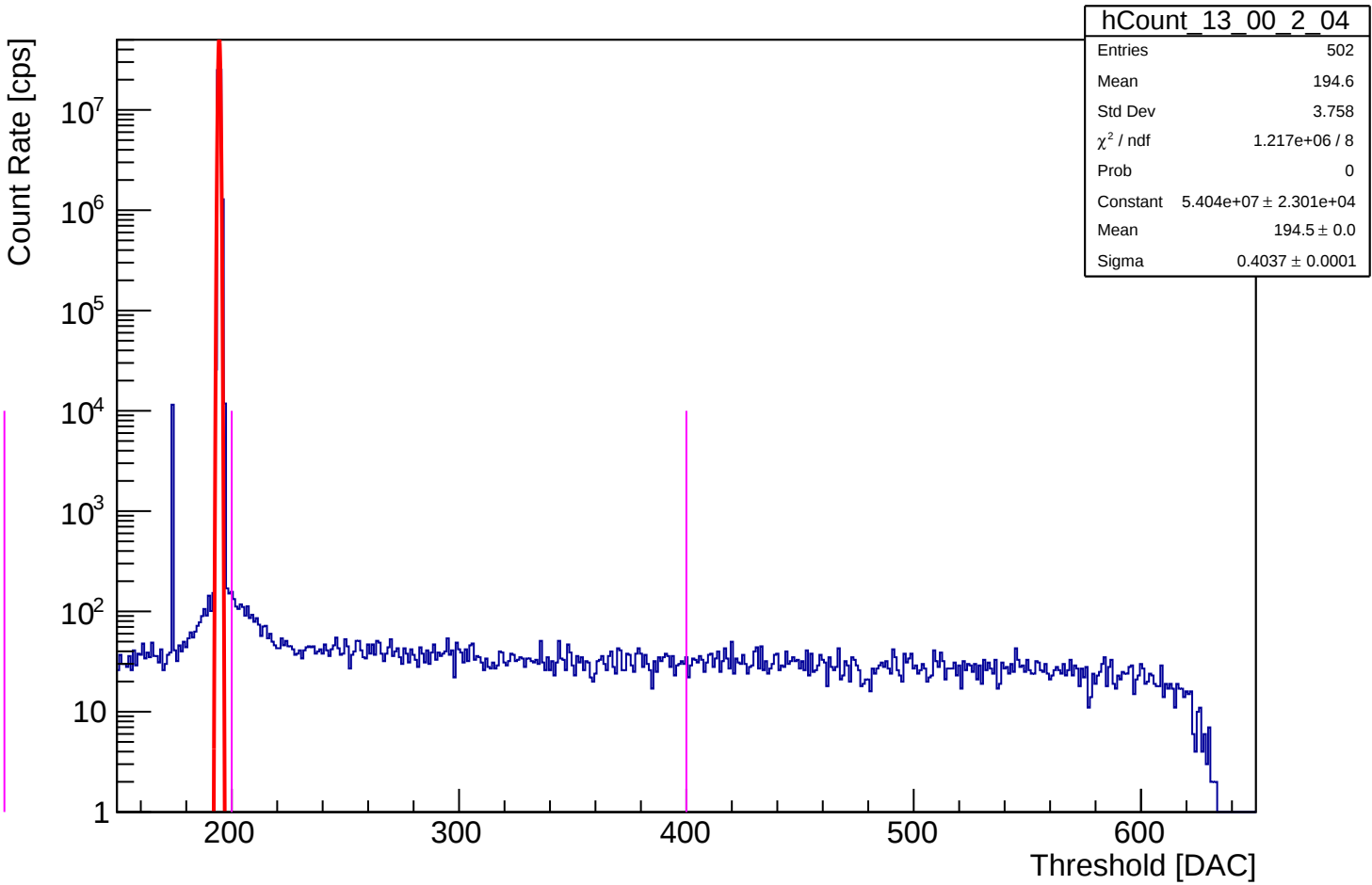
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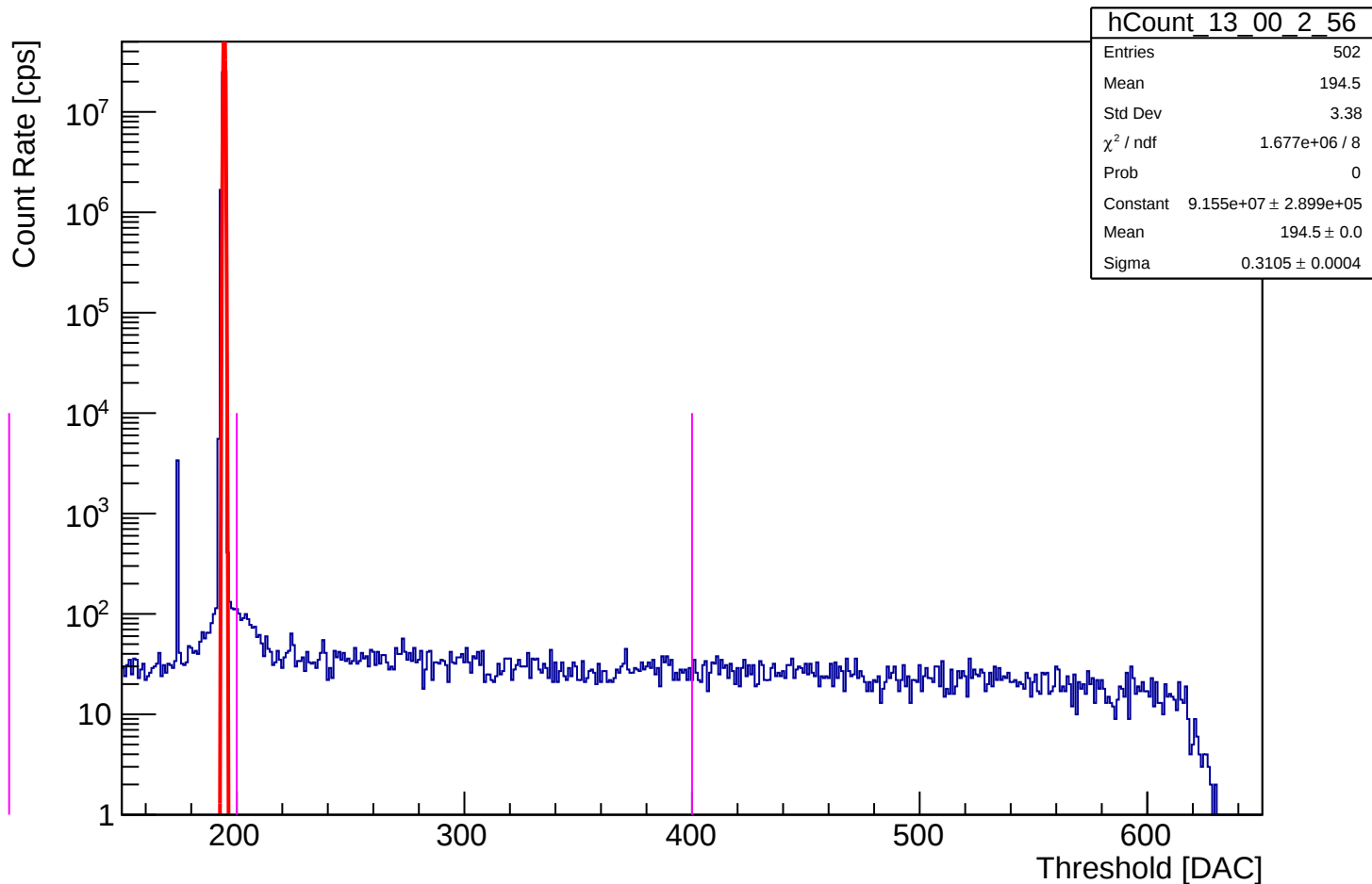




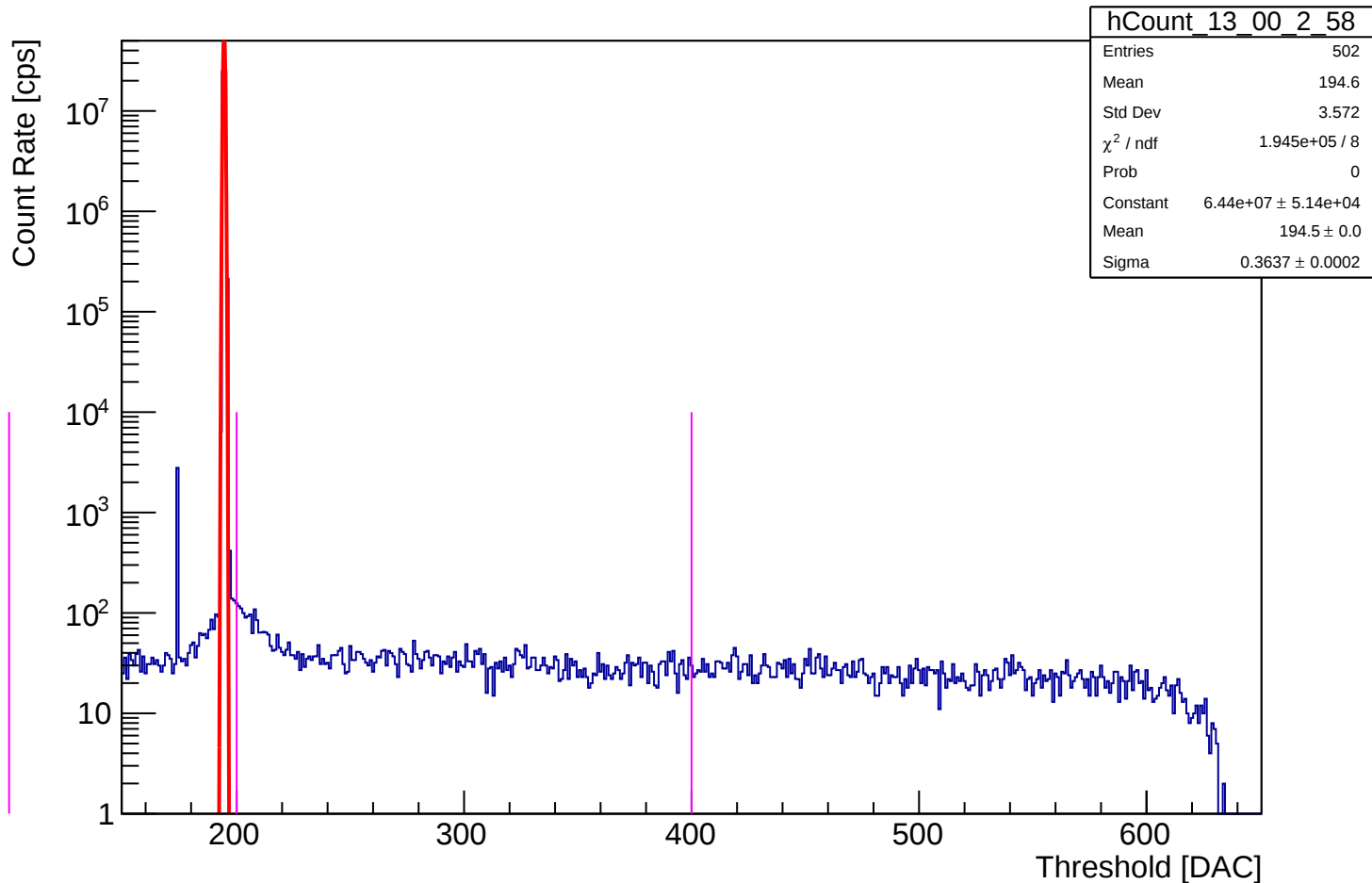




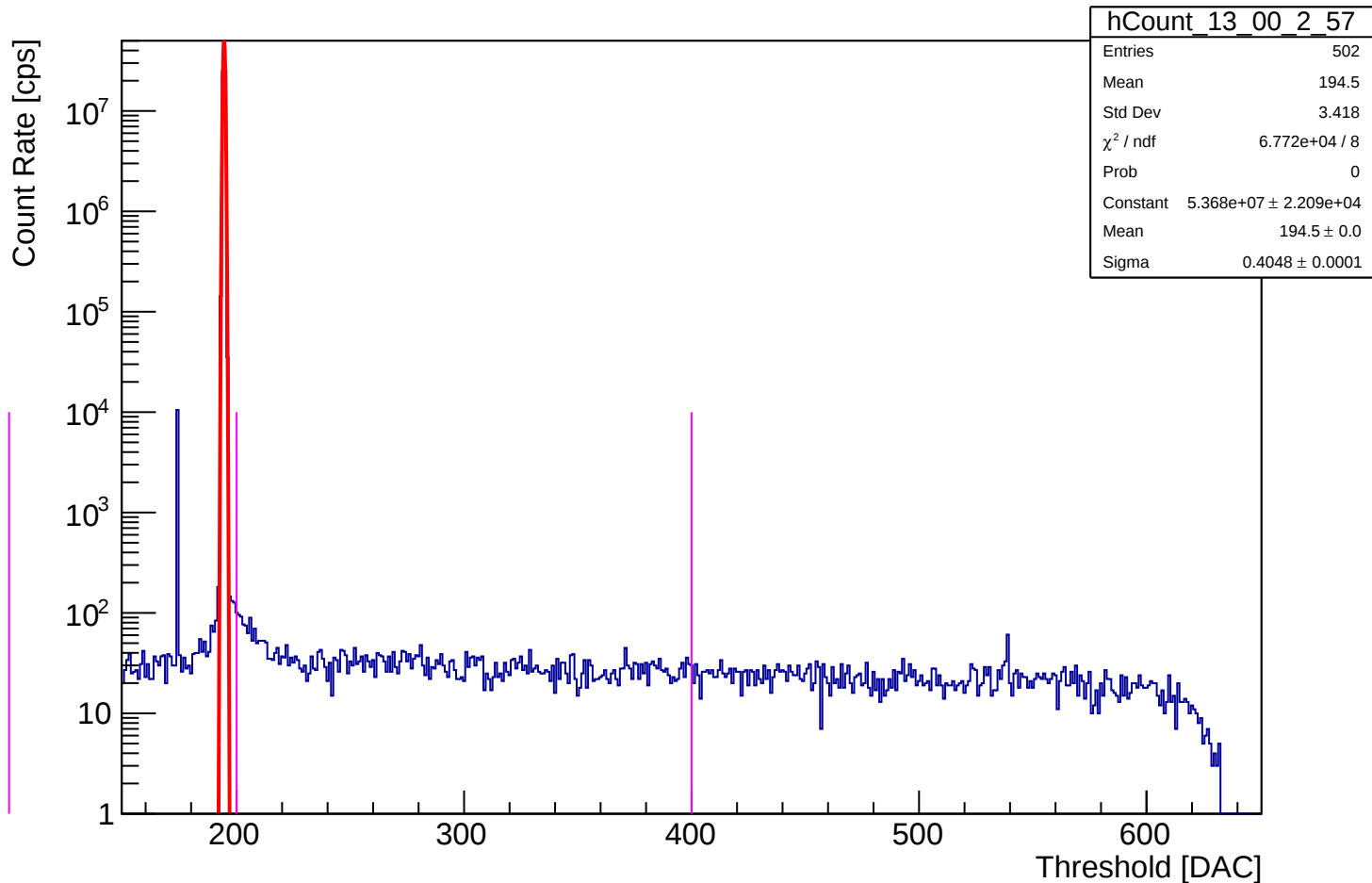
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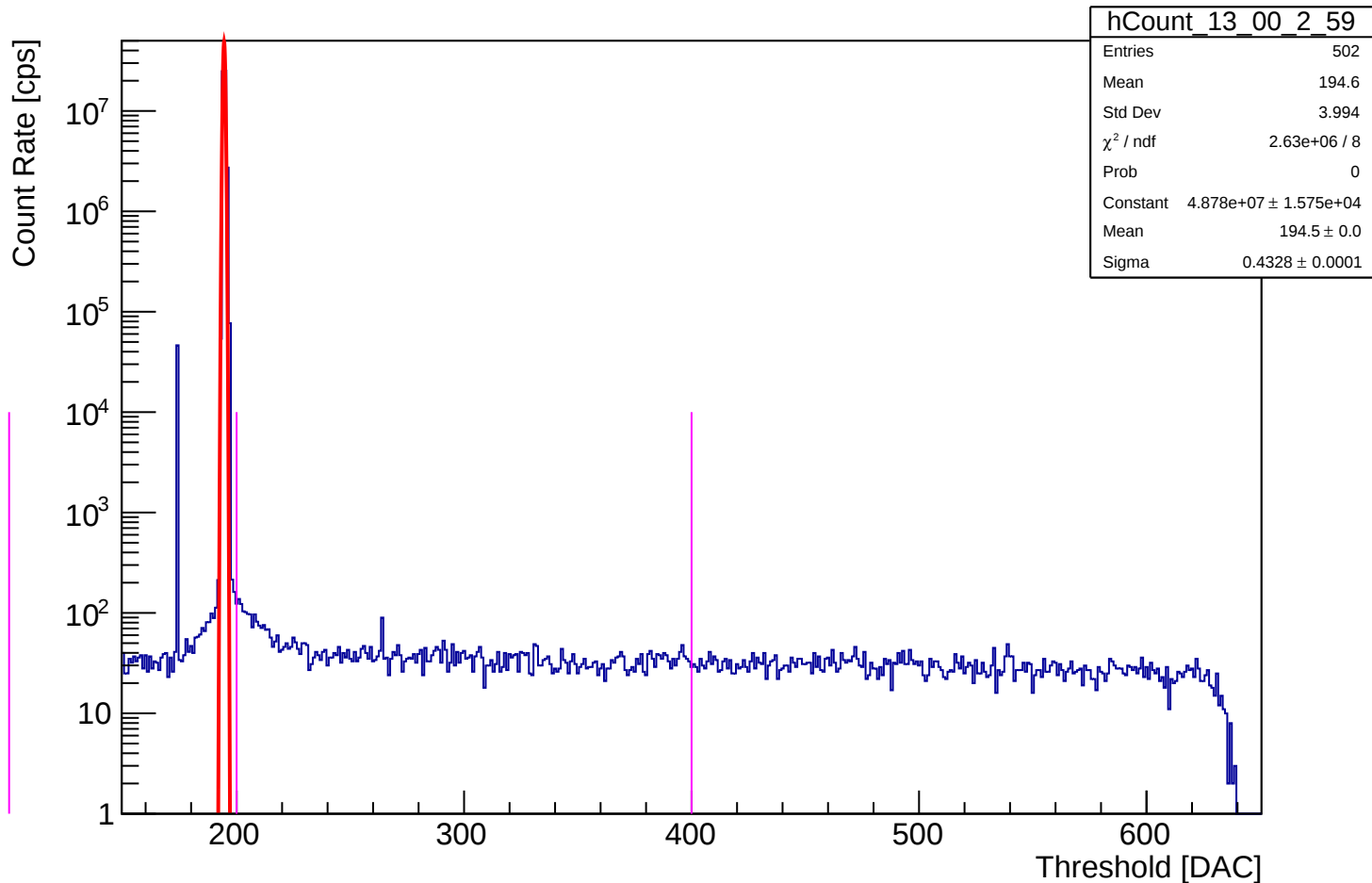
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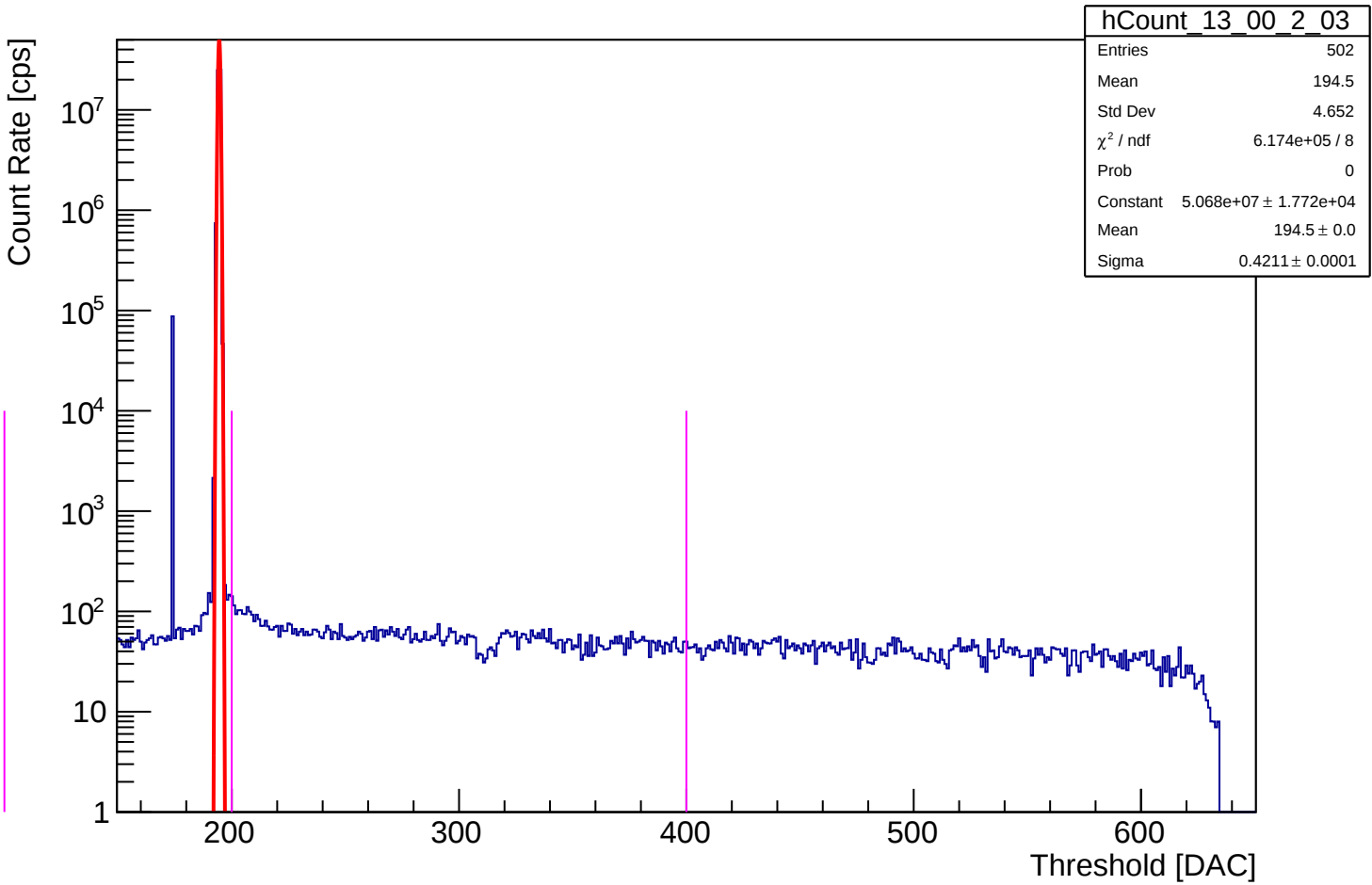


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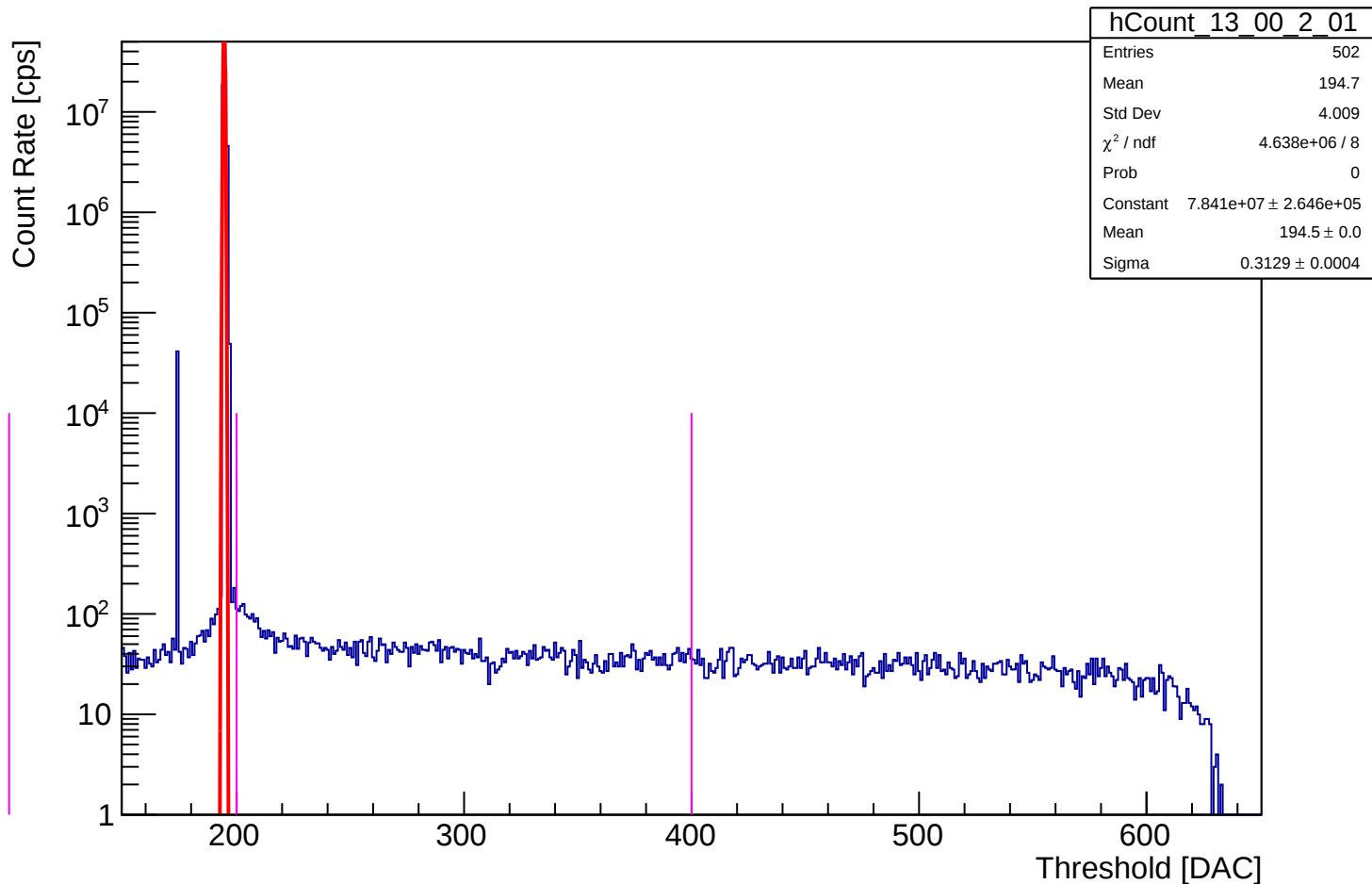


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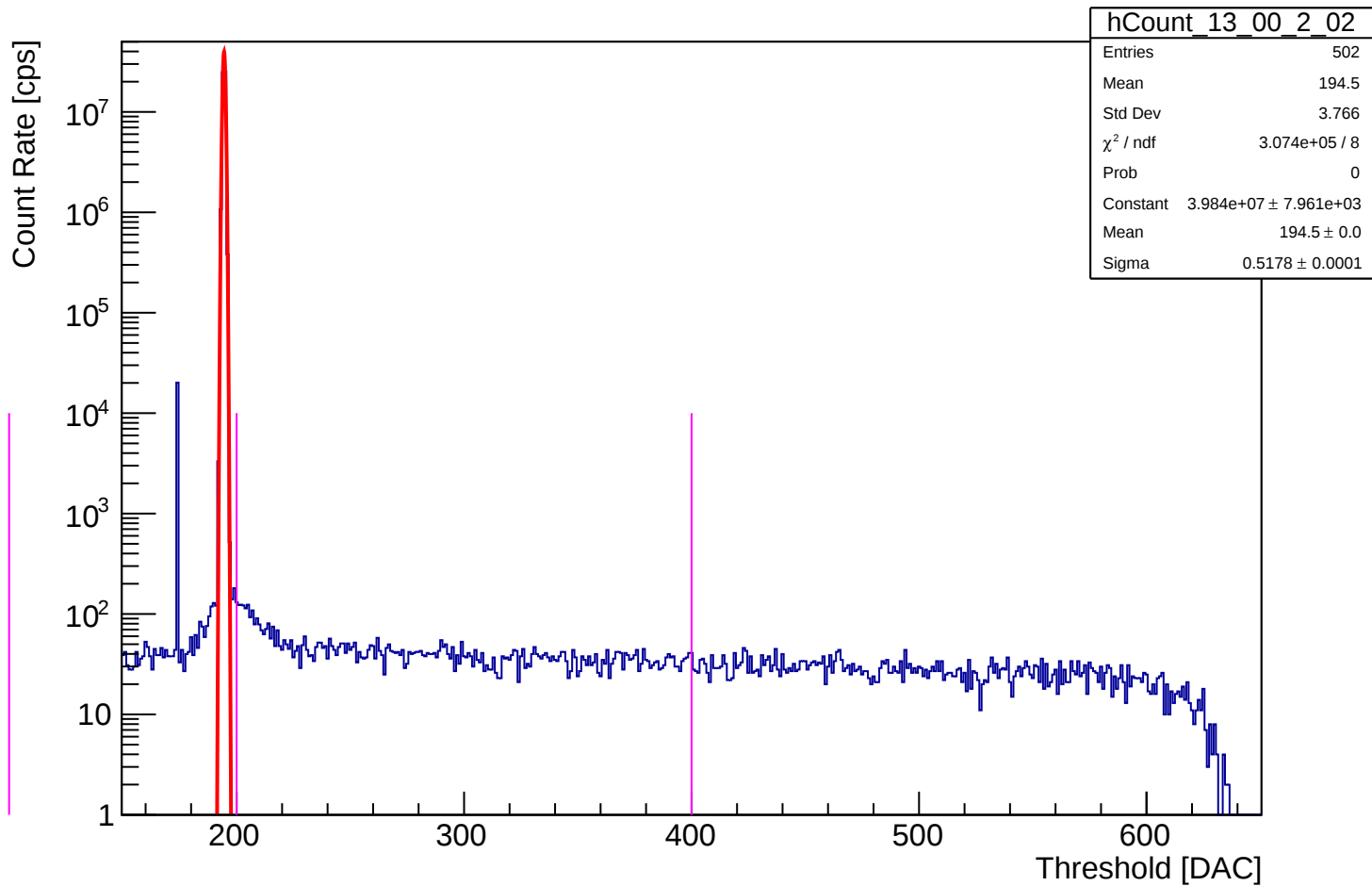


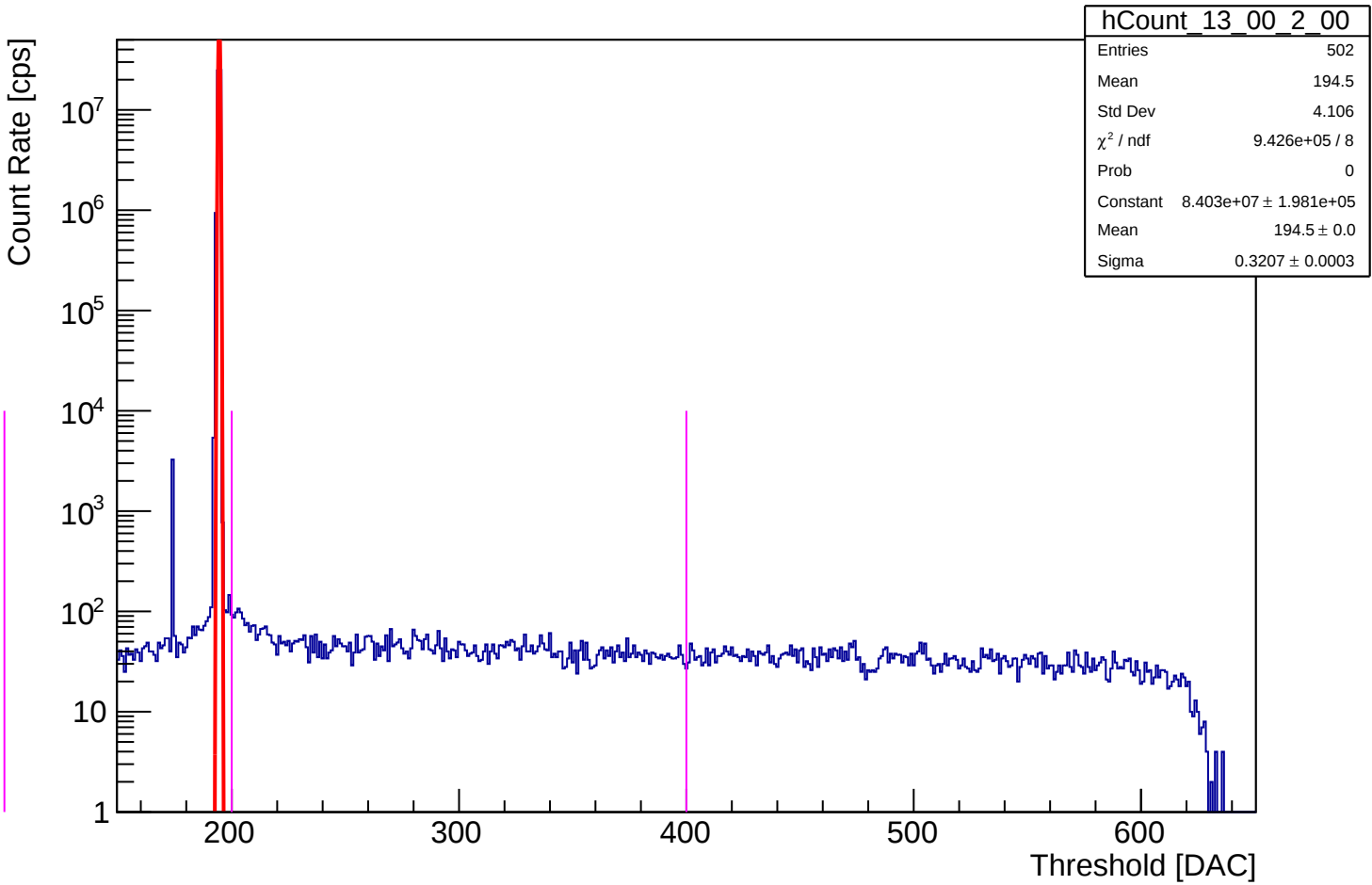


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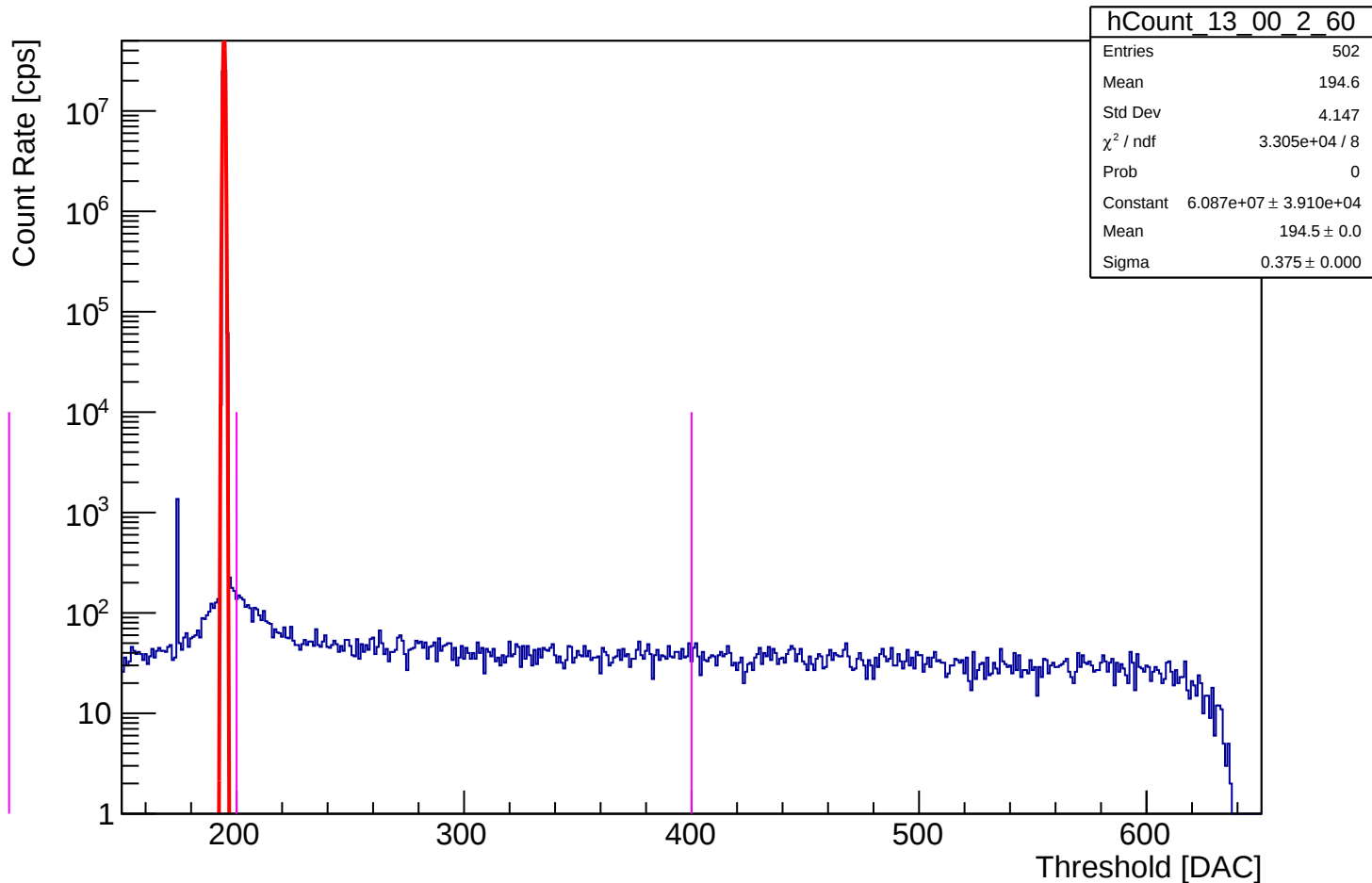


Row 1 Tile 1 Pmt 3 Pixel 59 Slot 13 Fiber 0 Asic 2 Channel 2

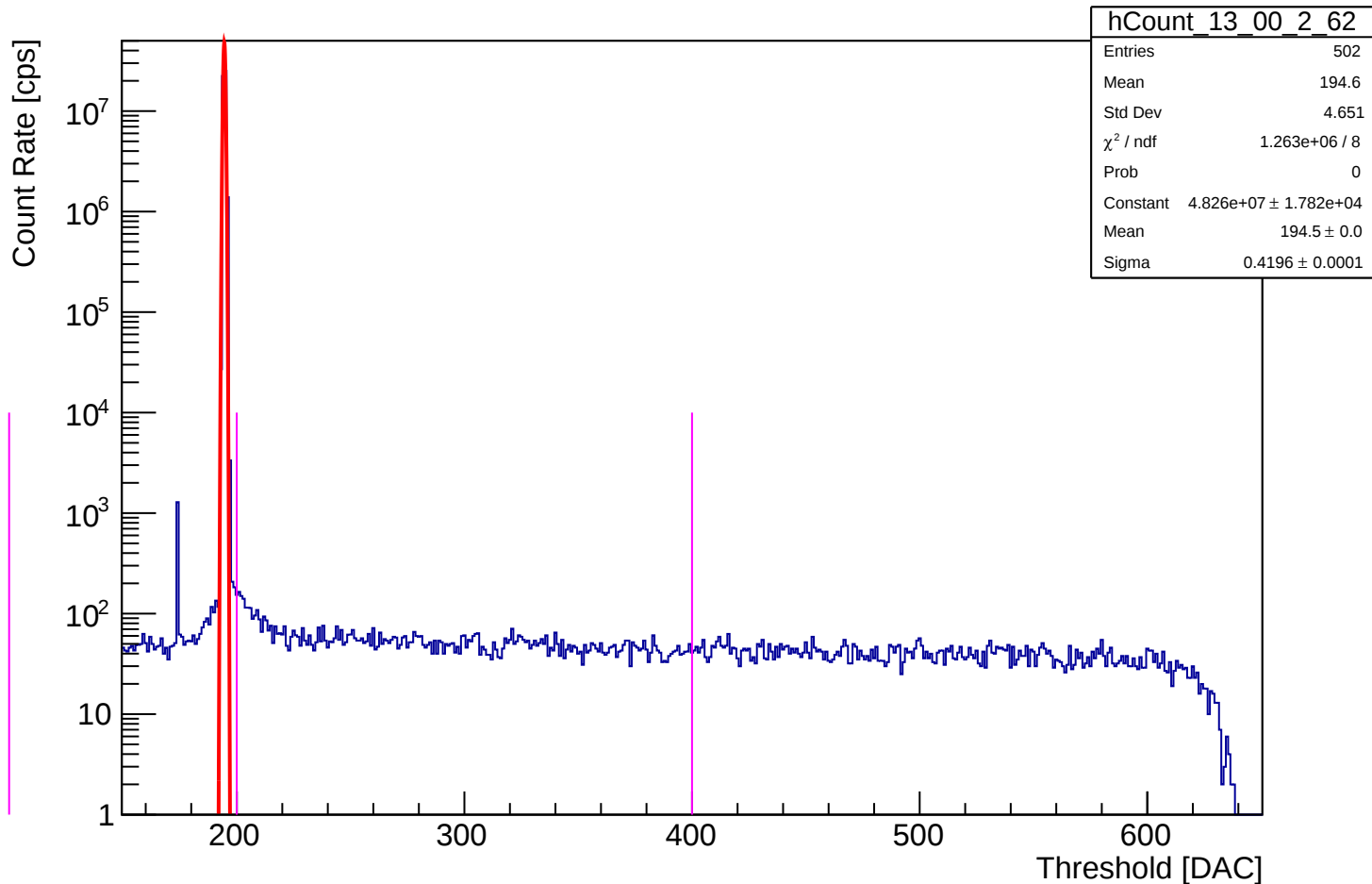




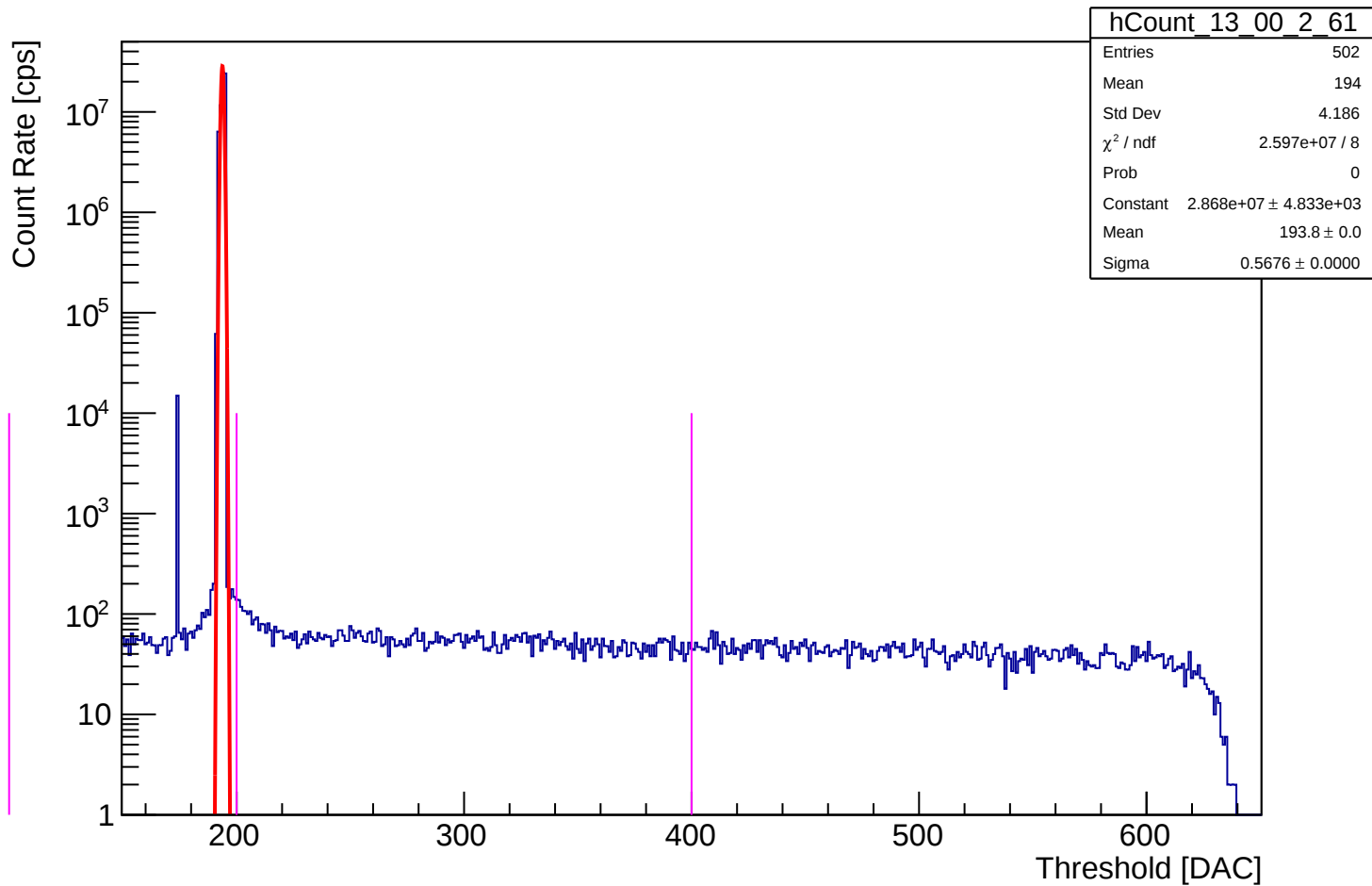
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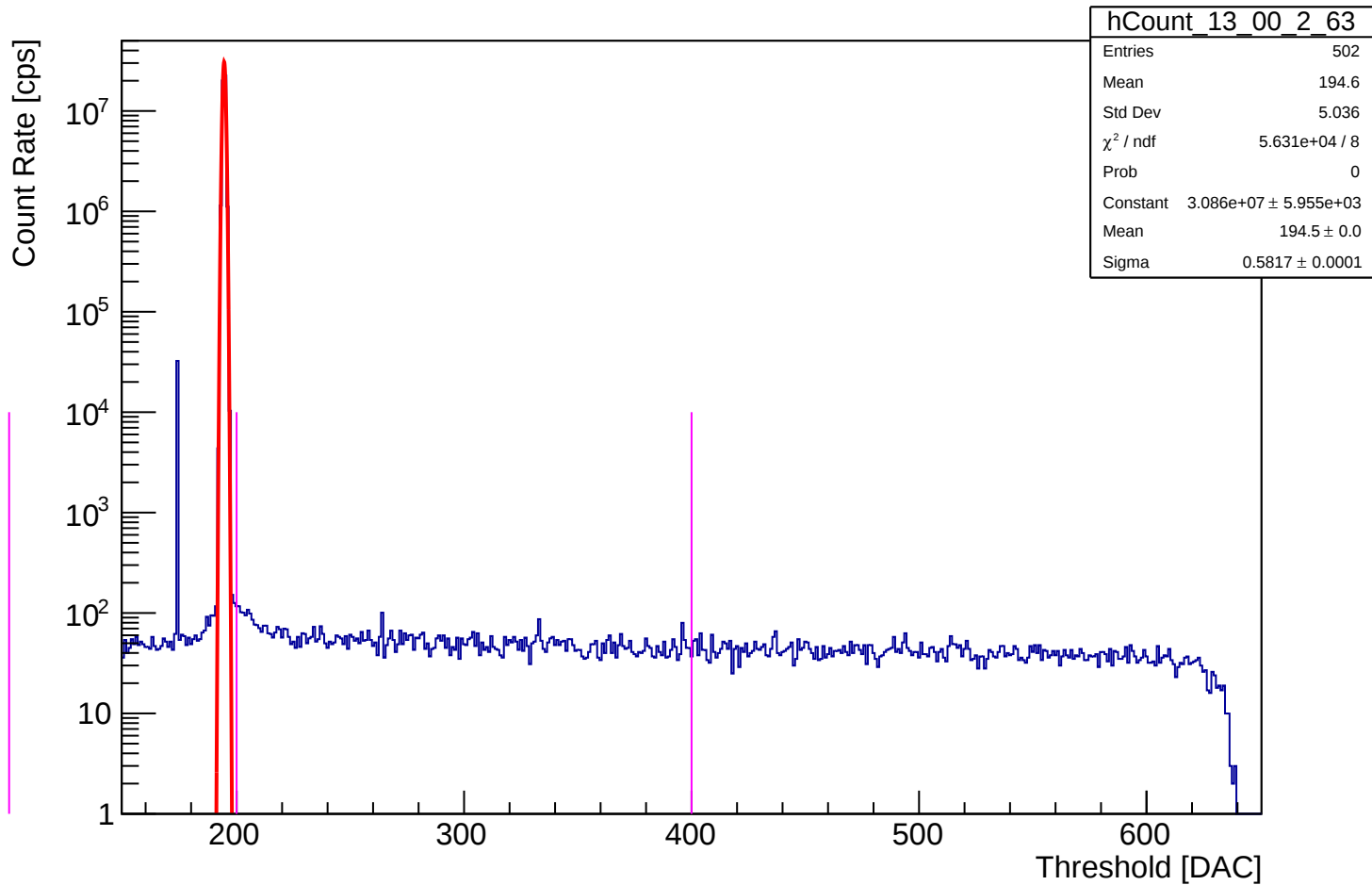
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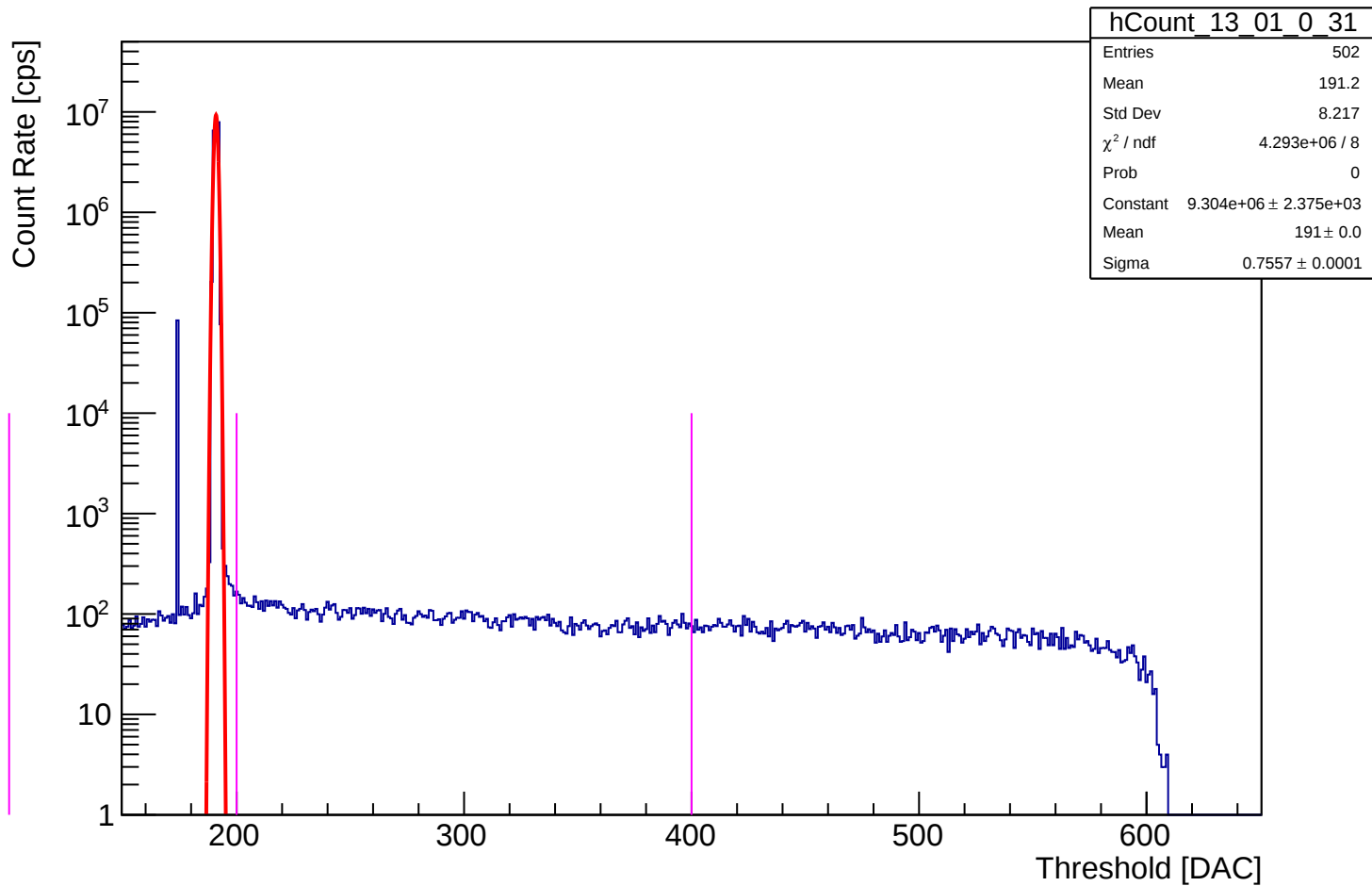
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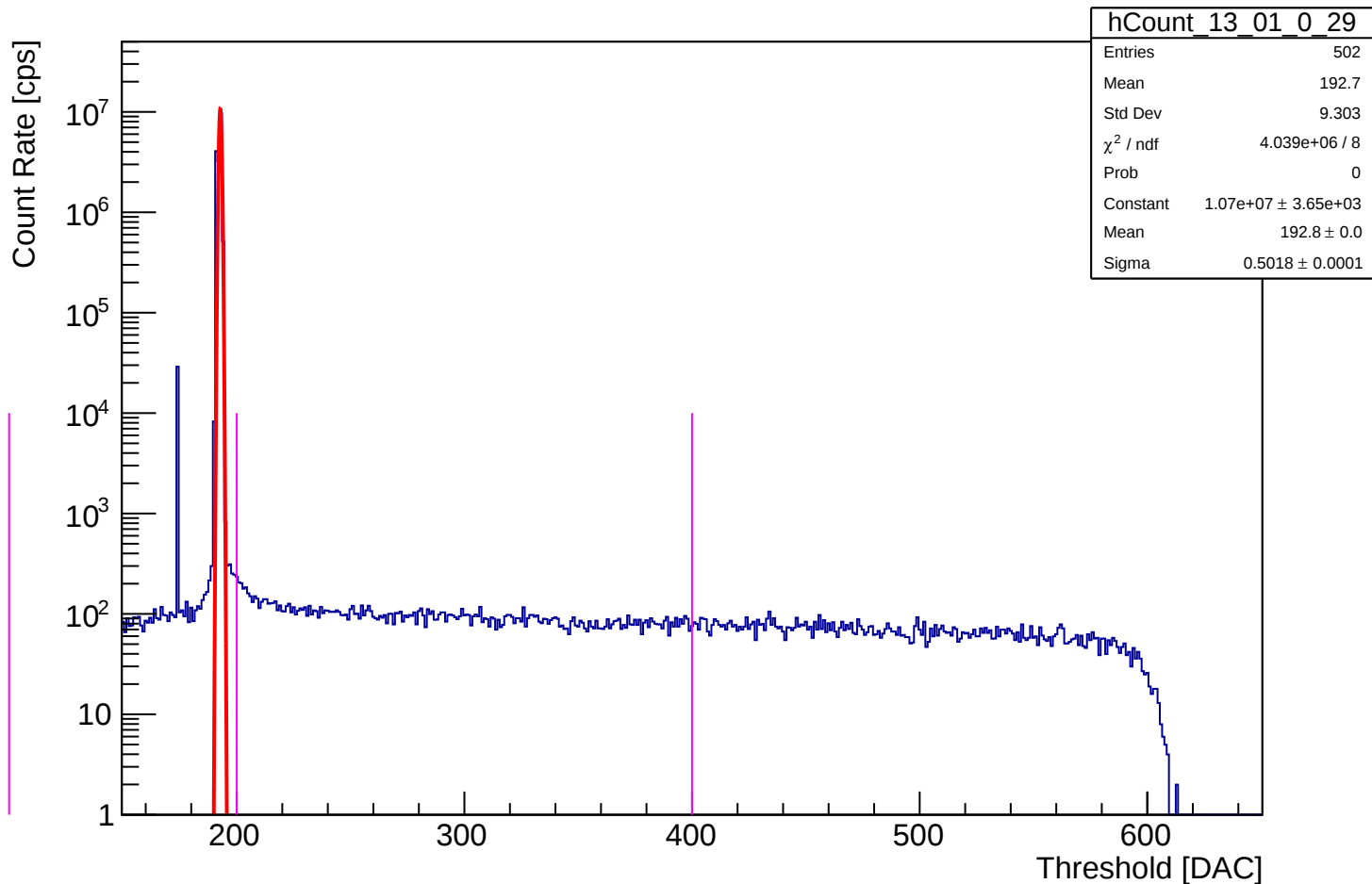
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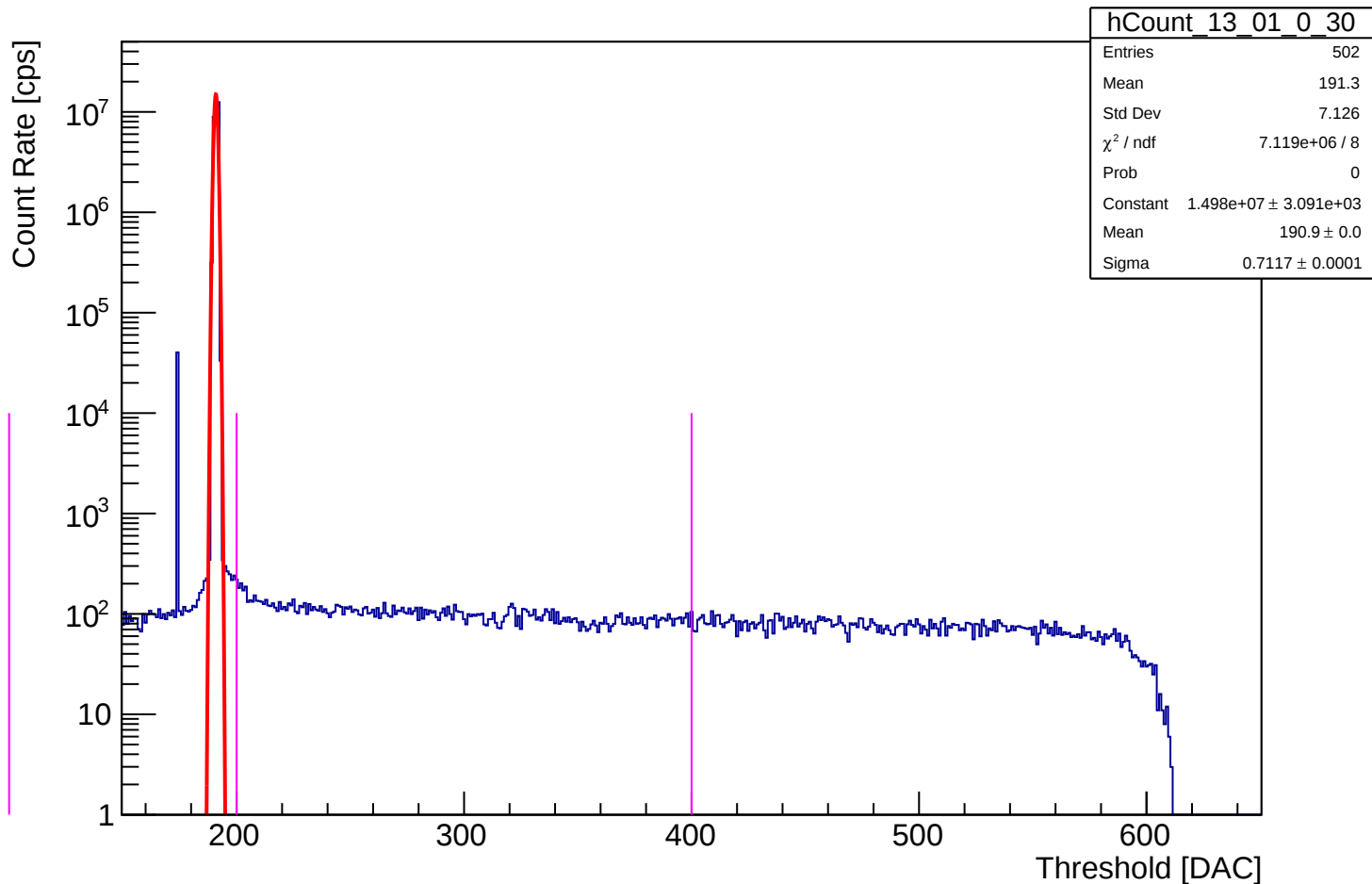
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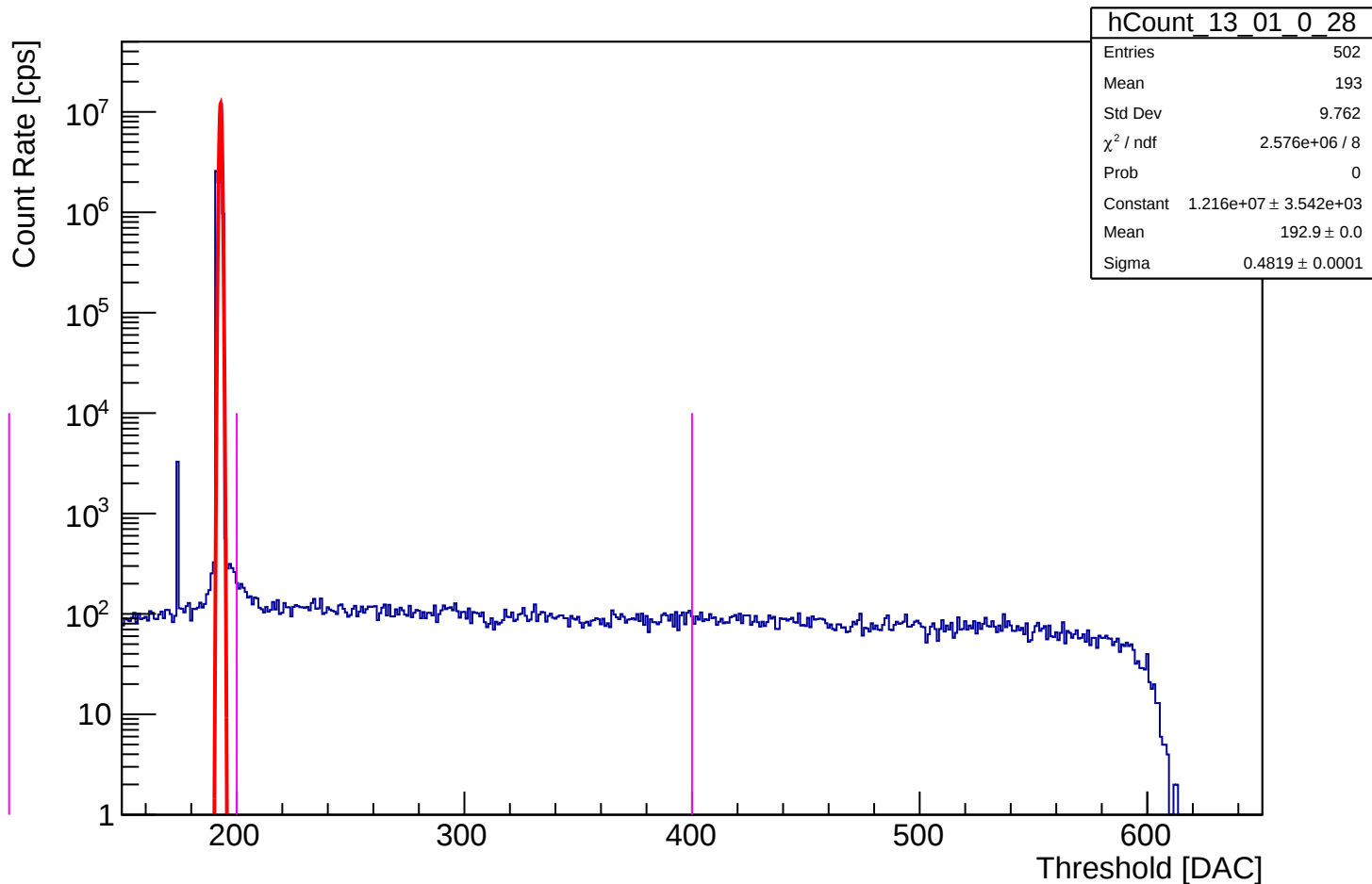
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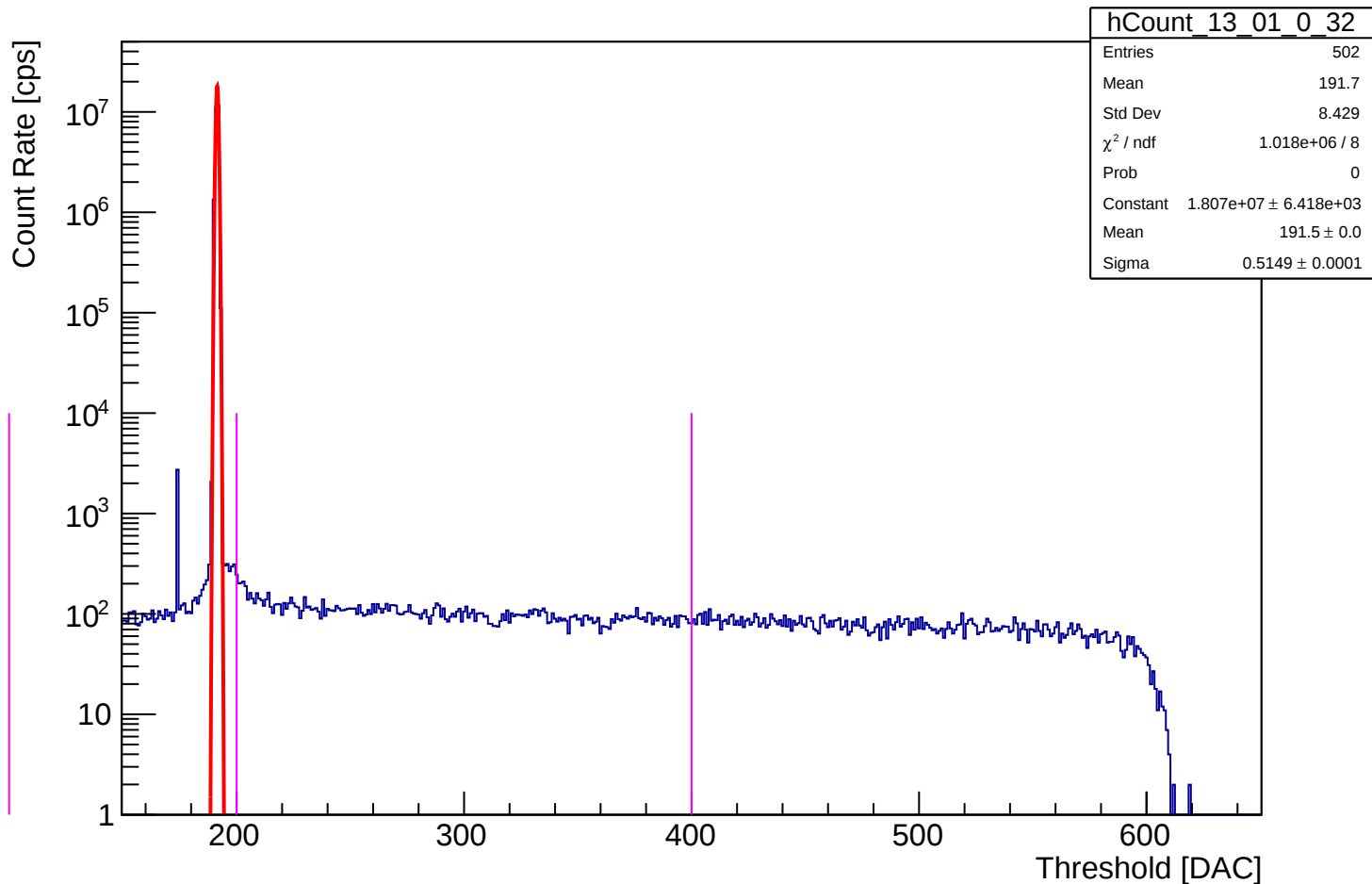
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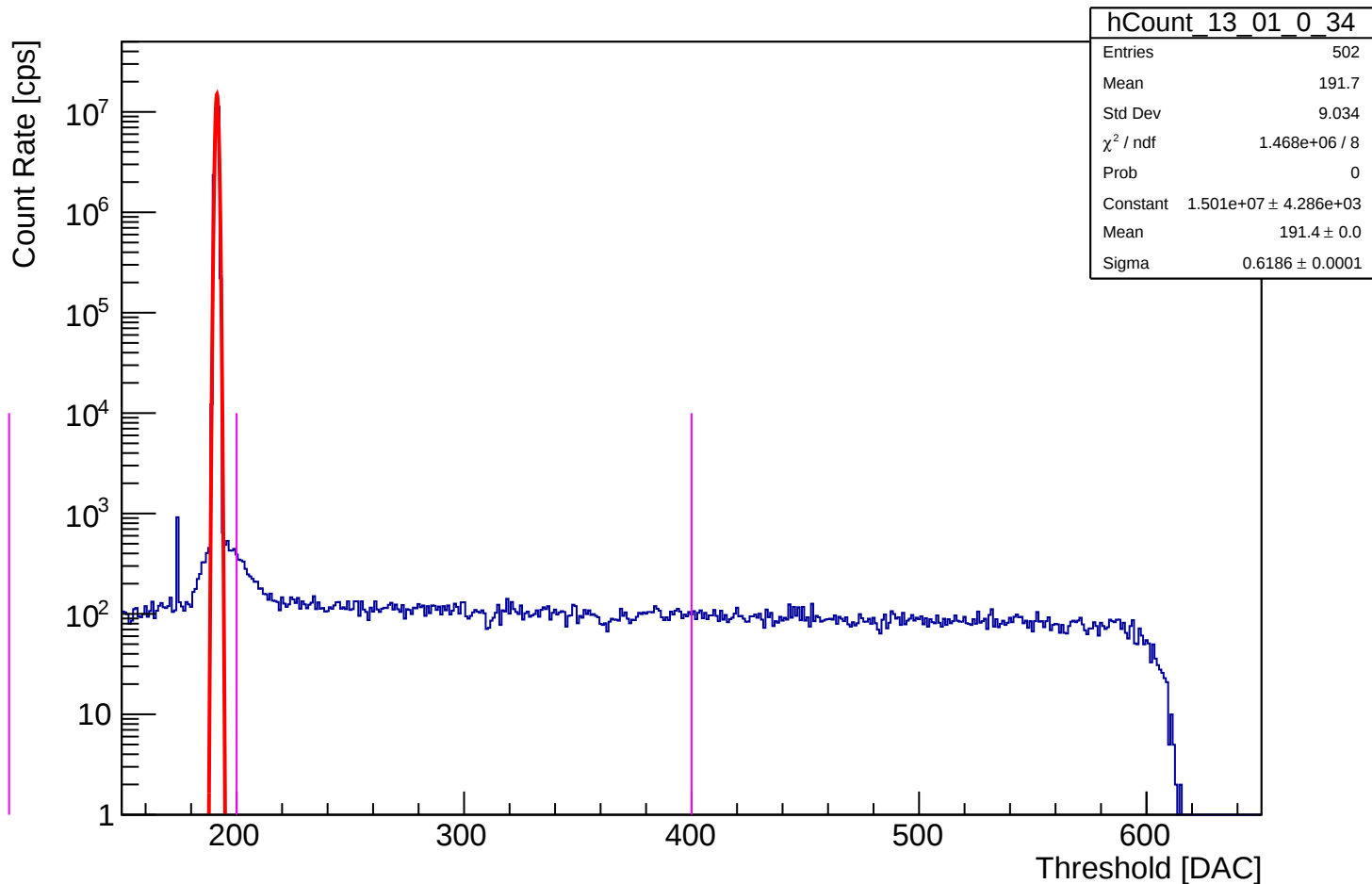
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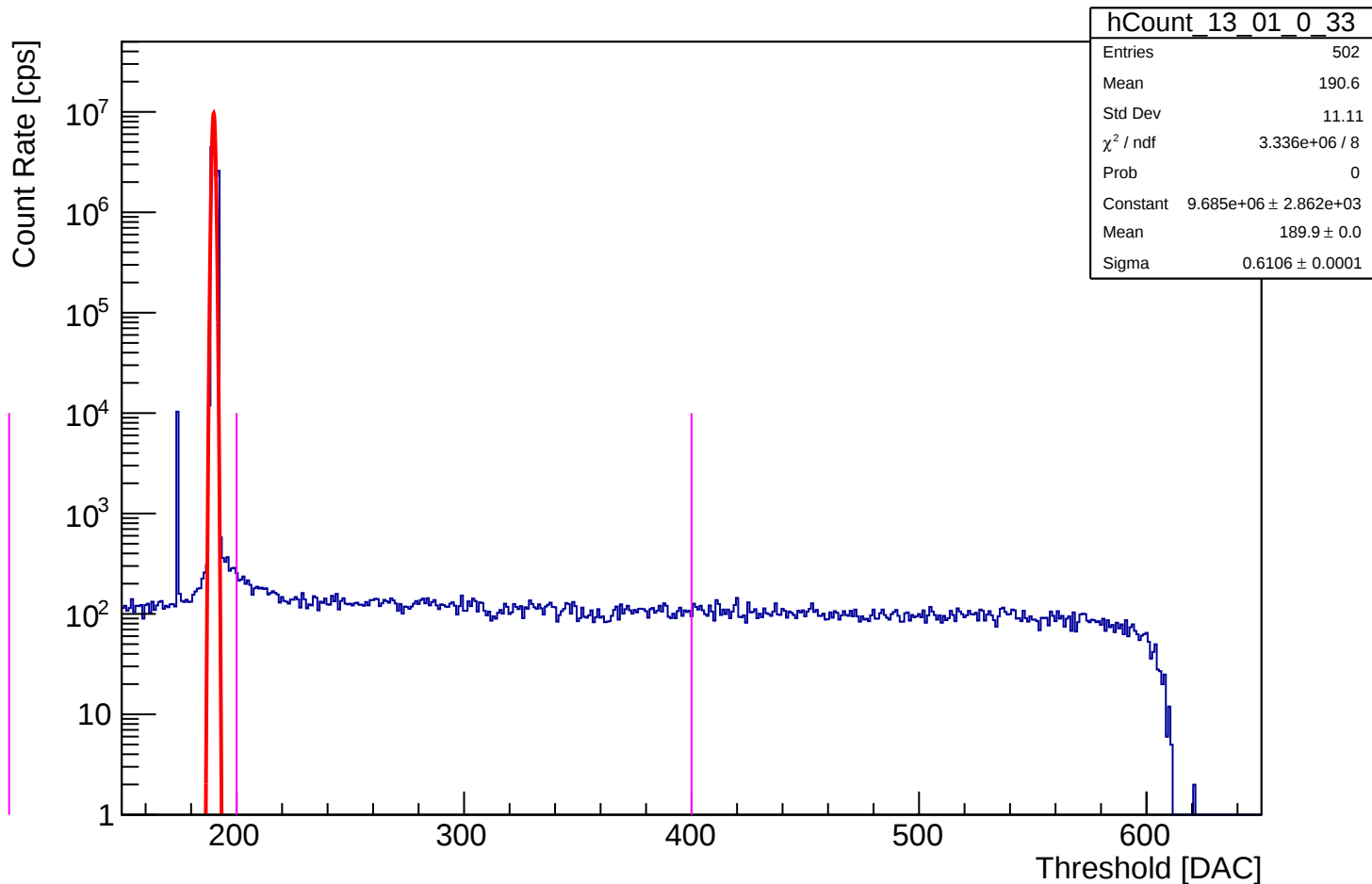
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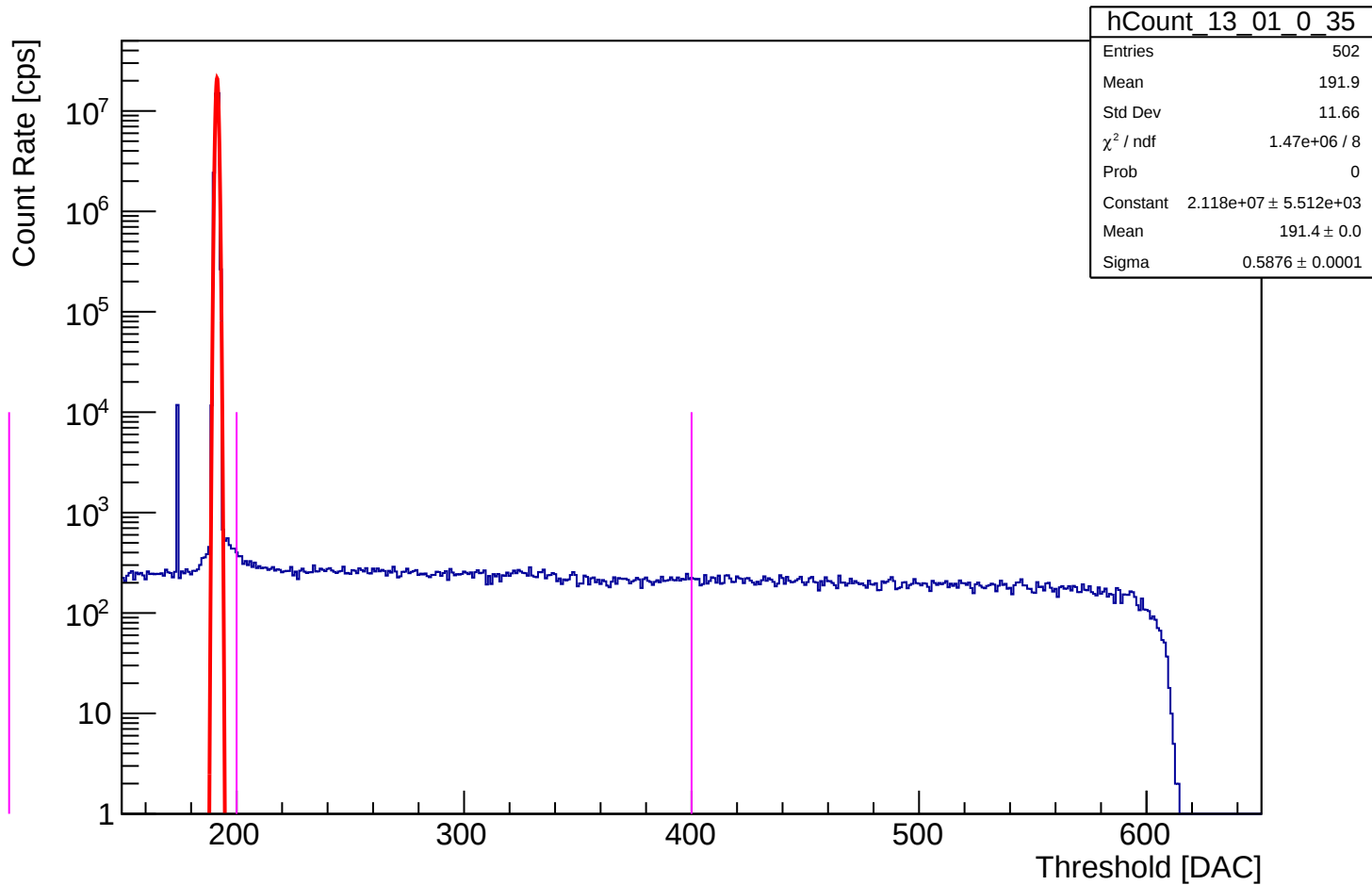
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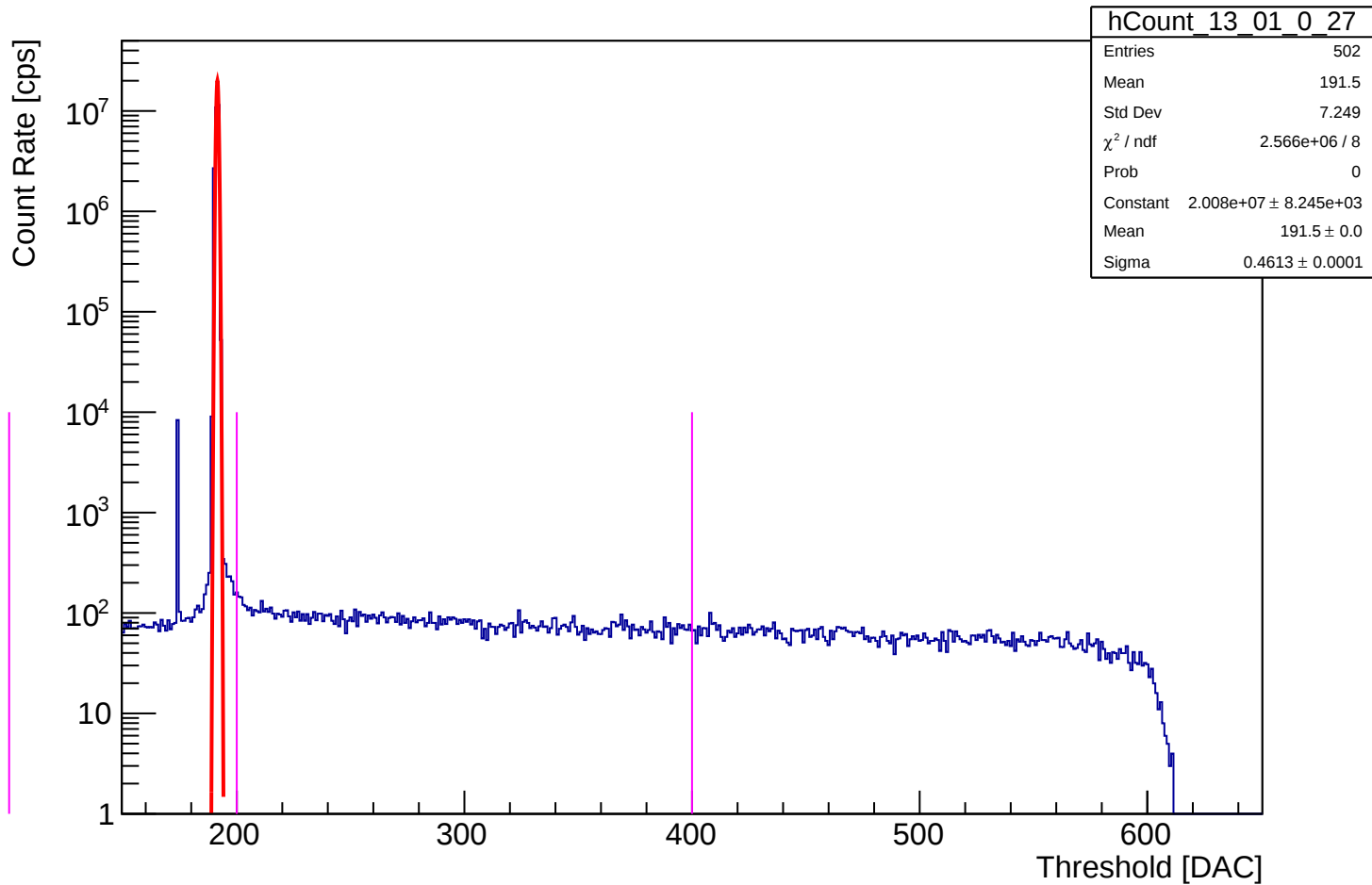
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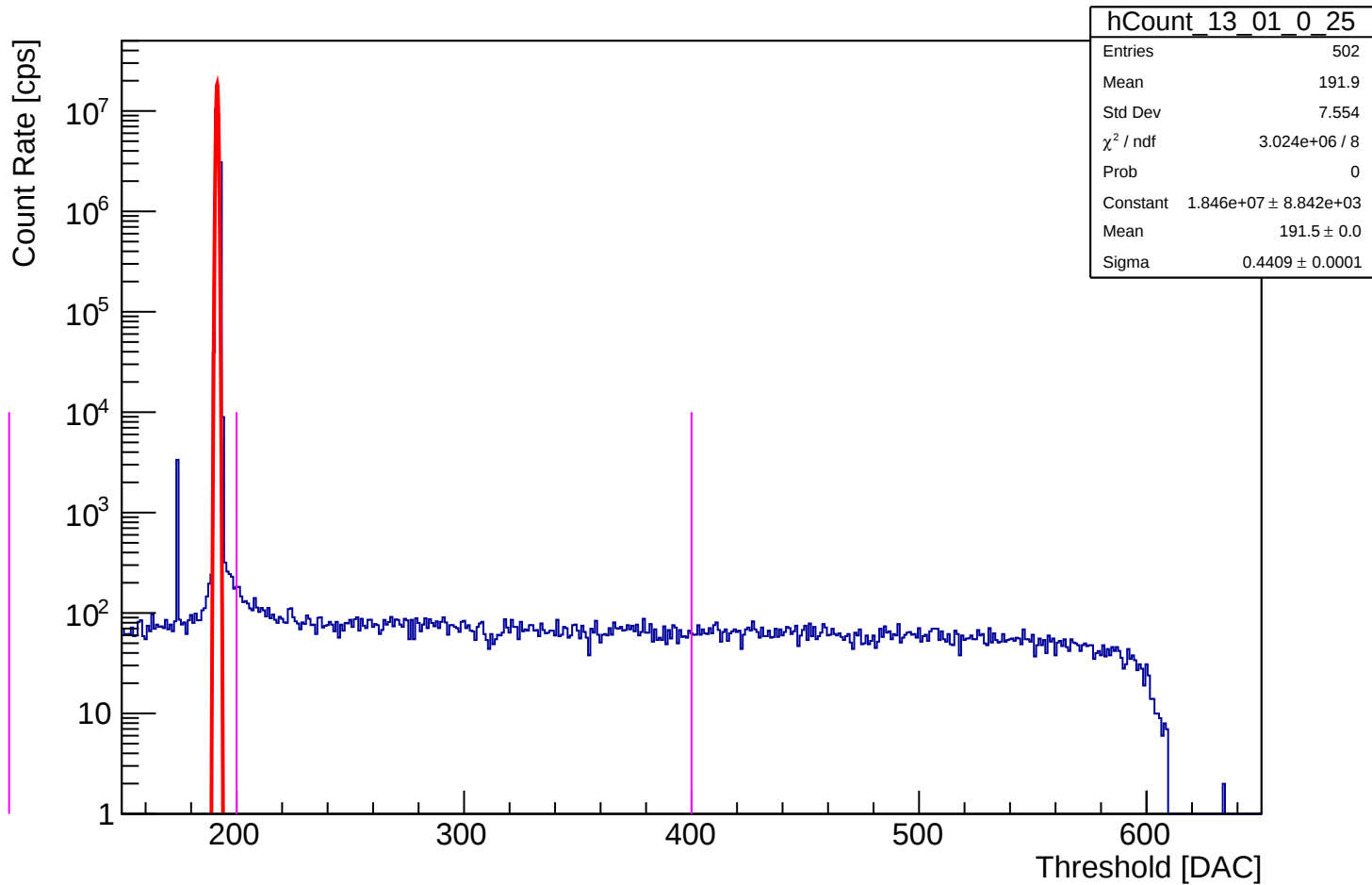
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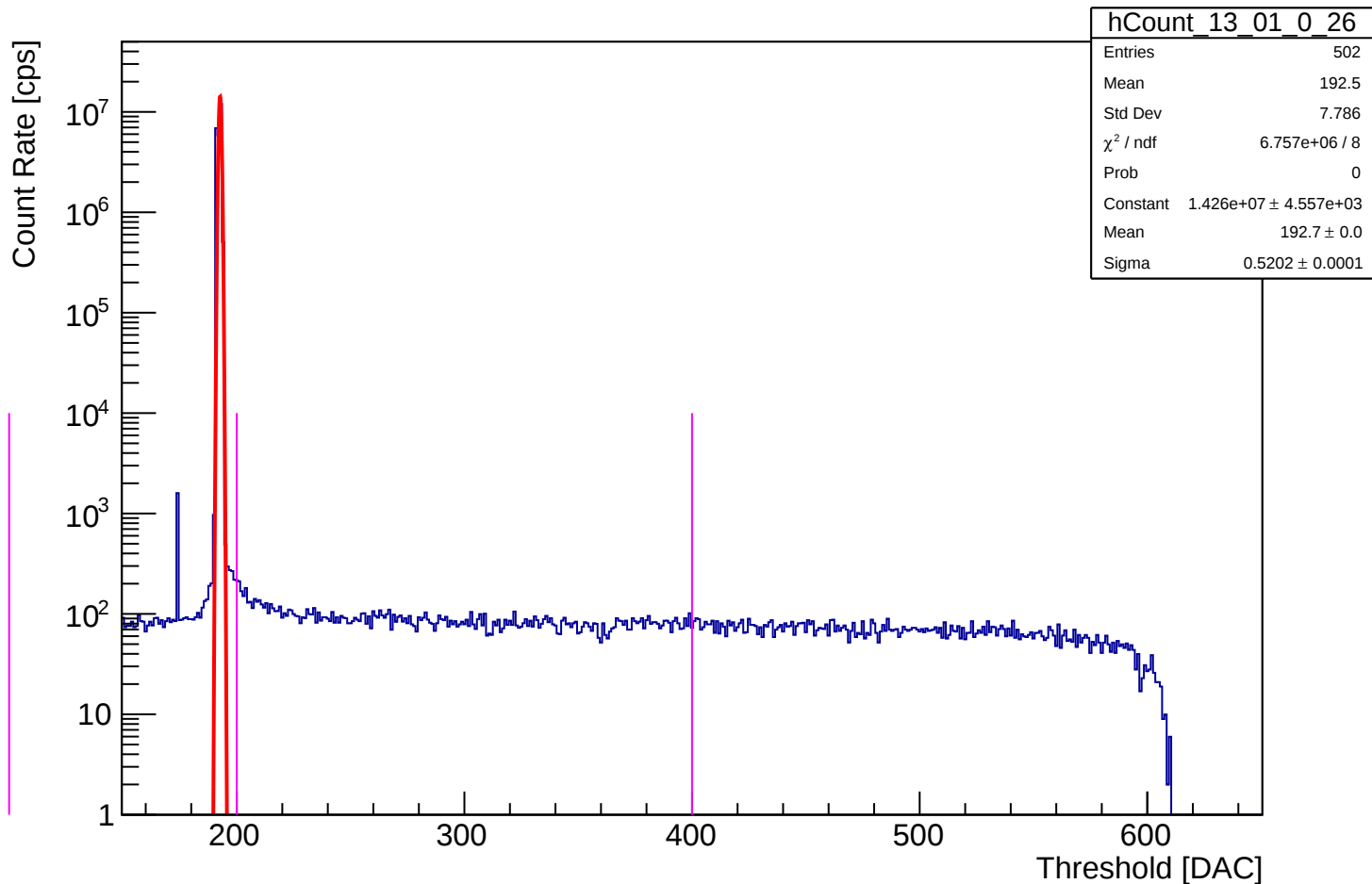
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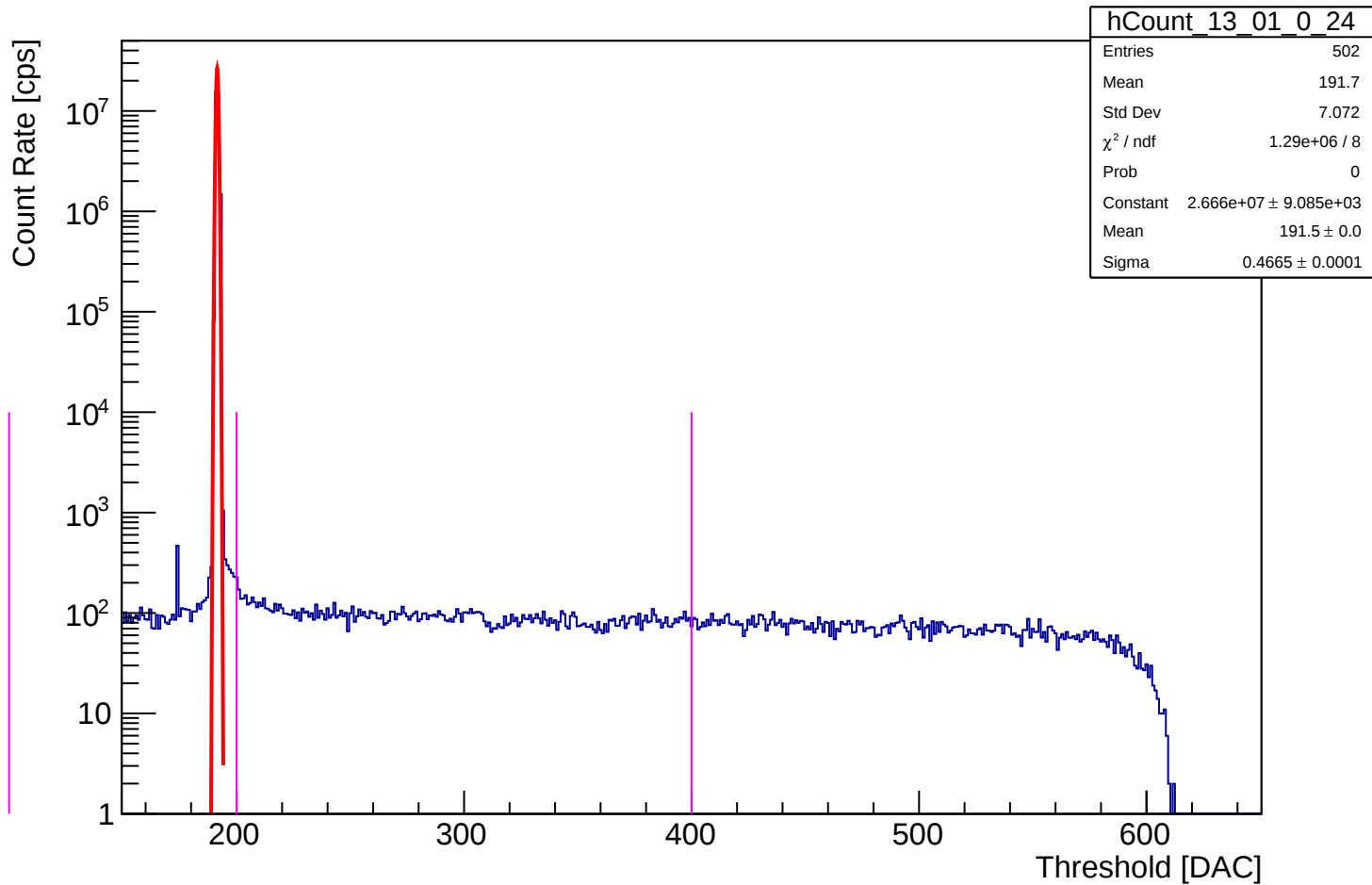
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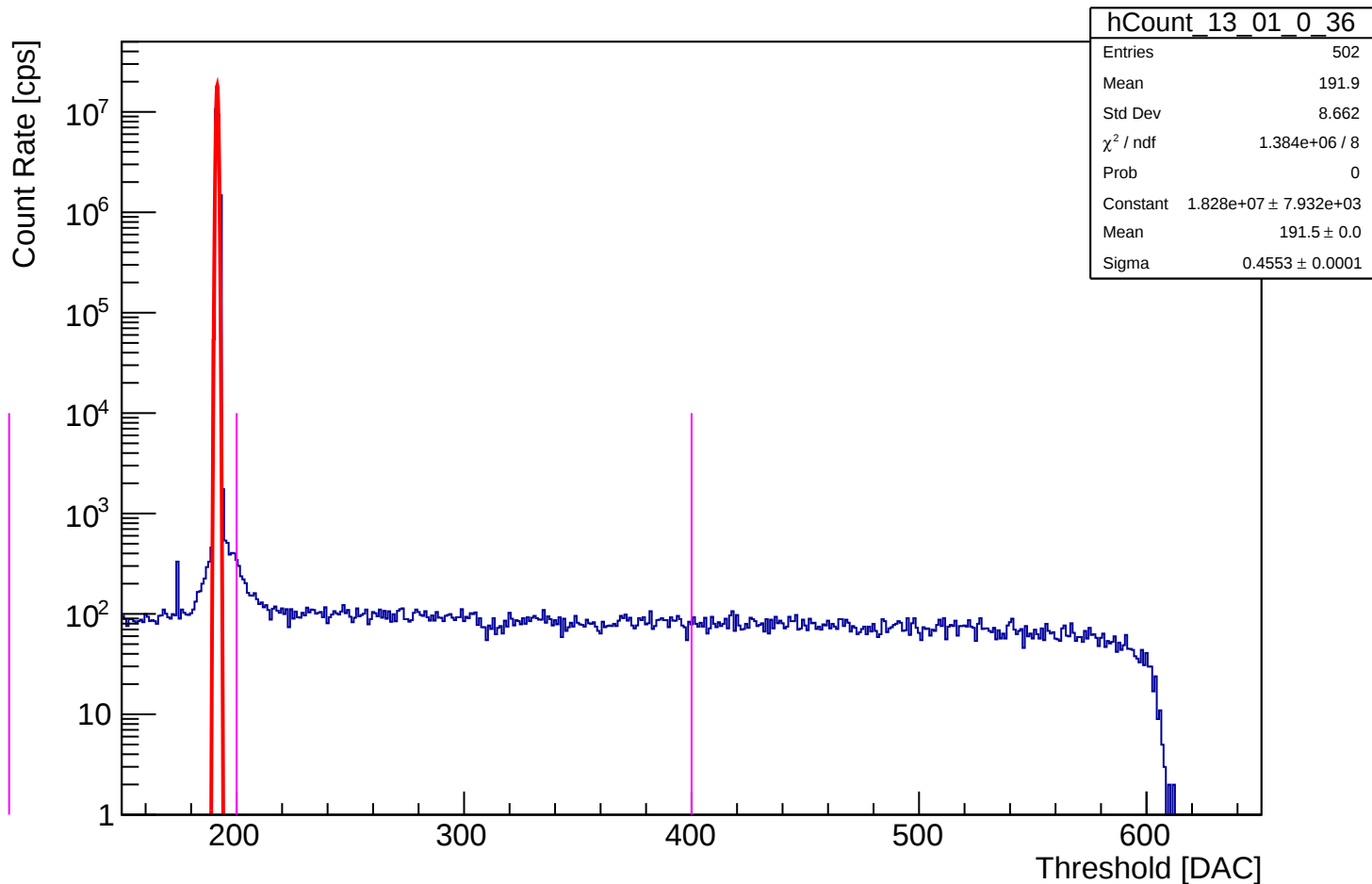
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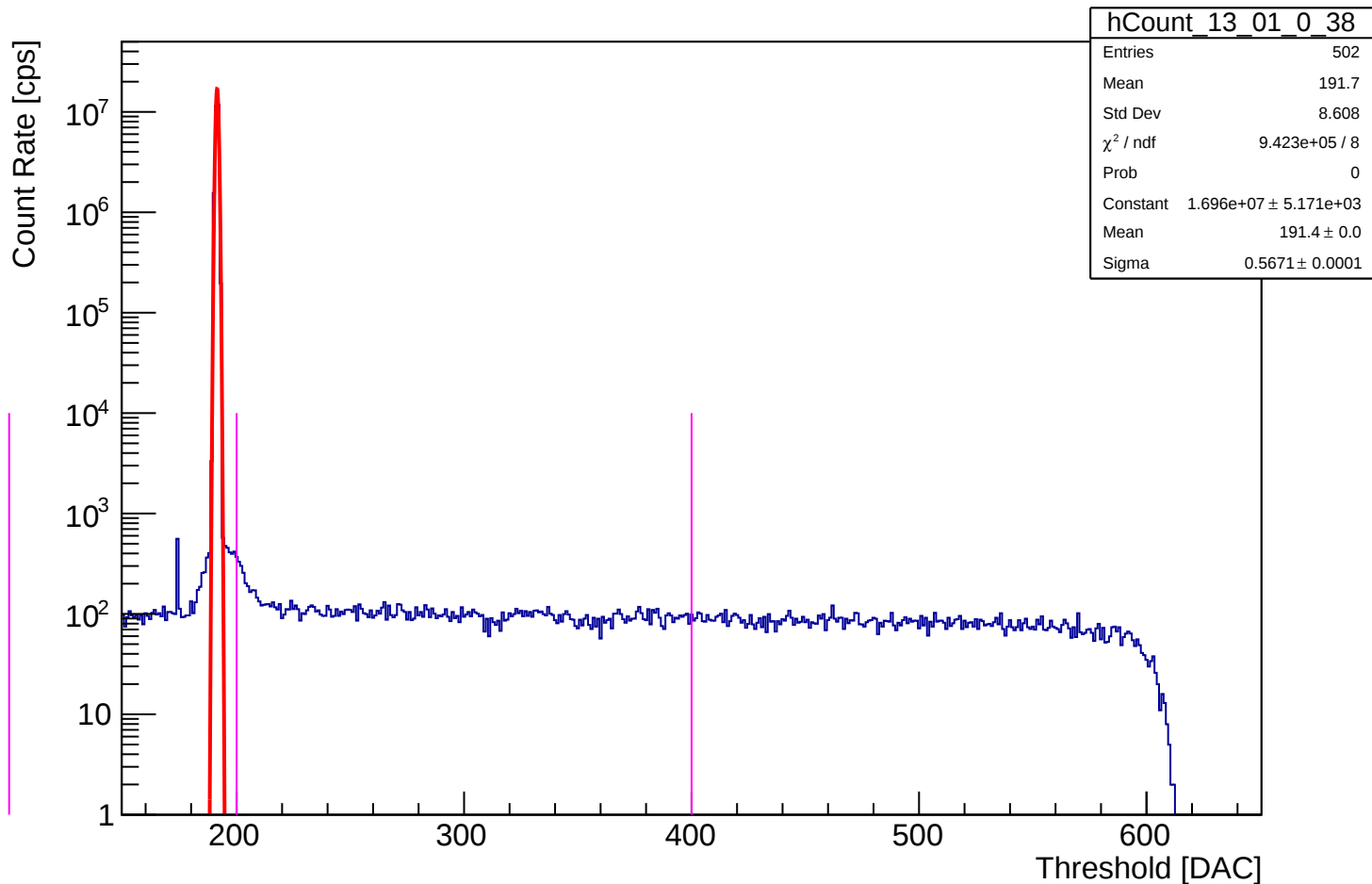
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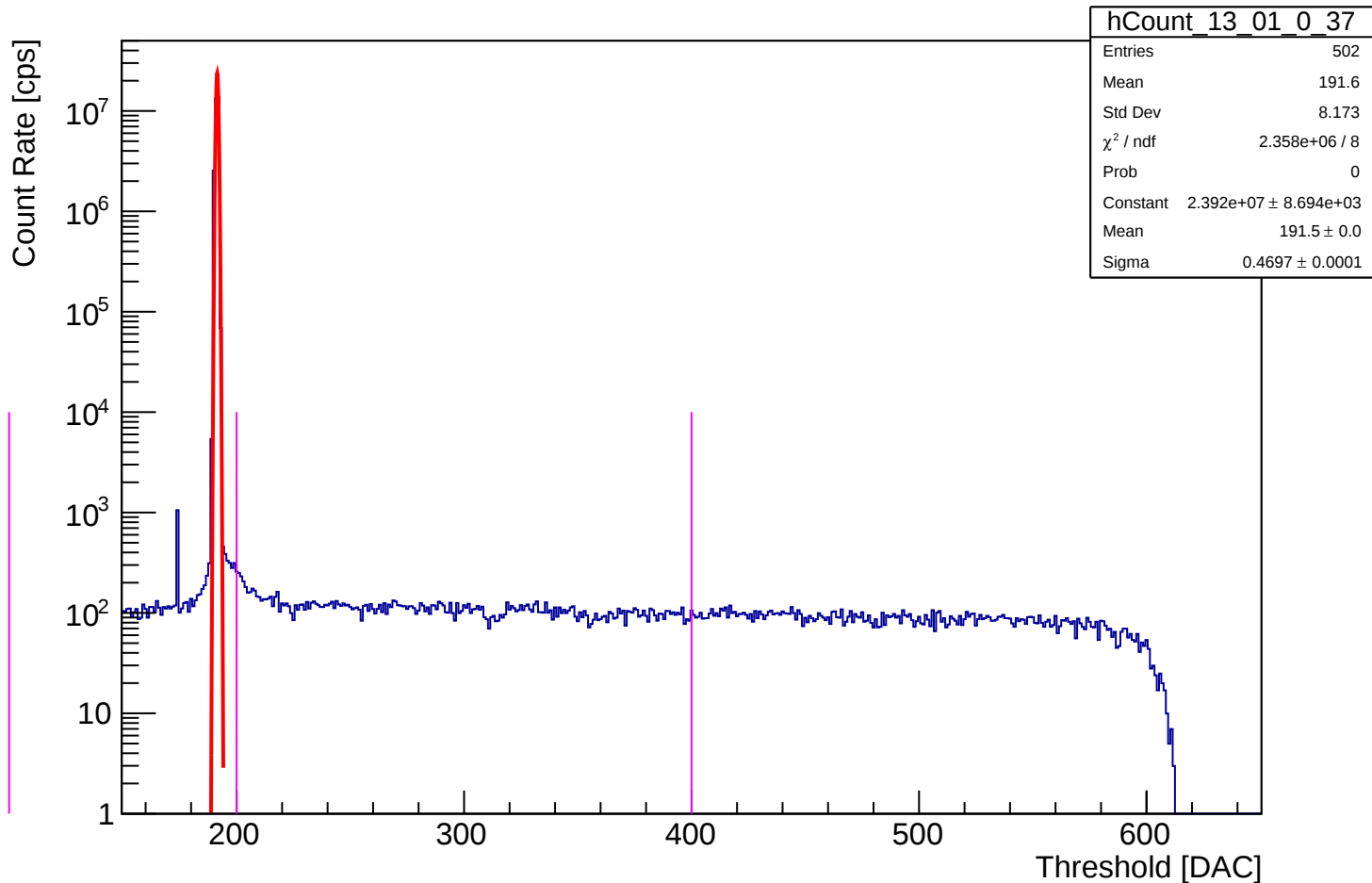
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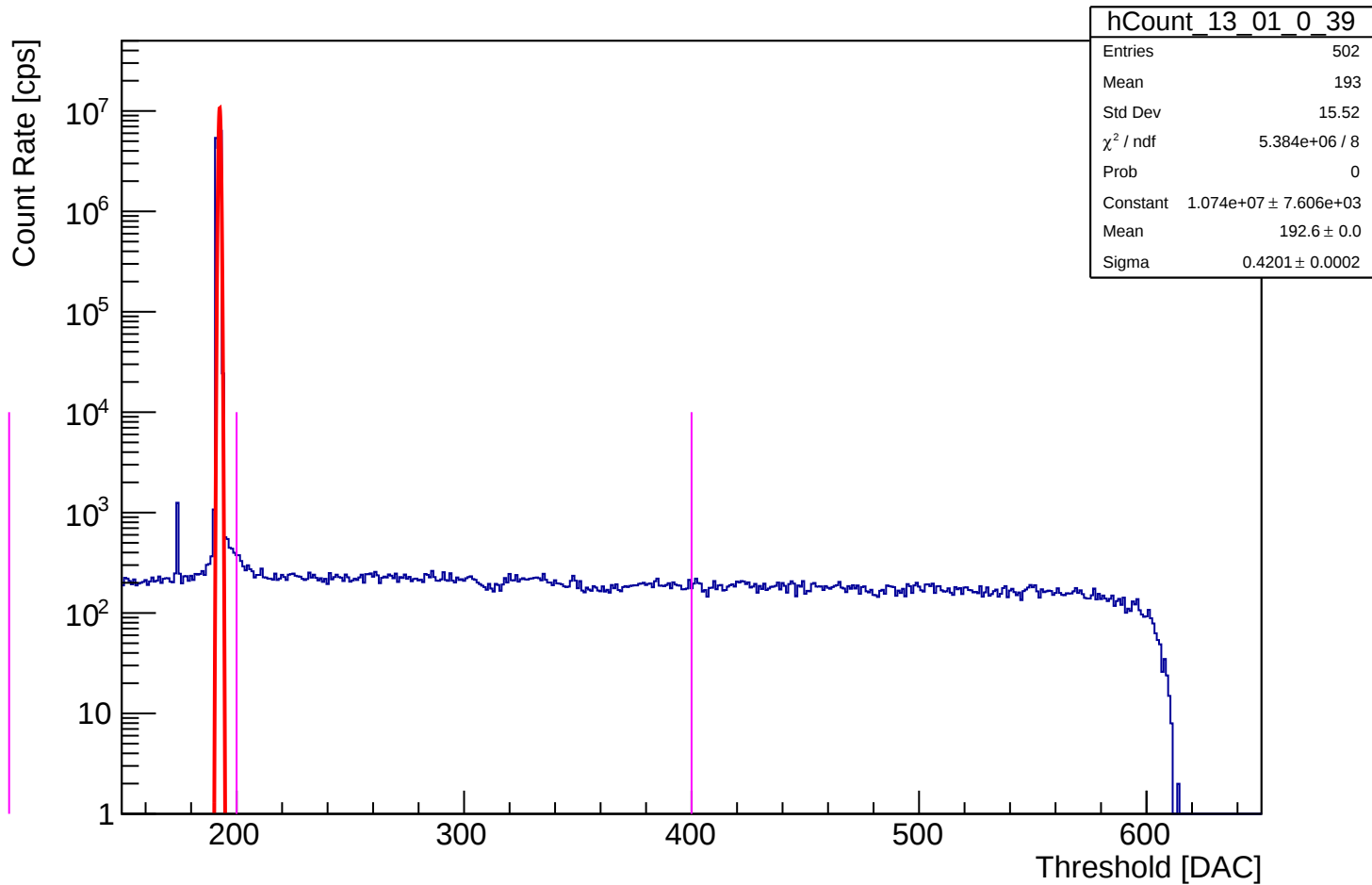
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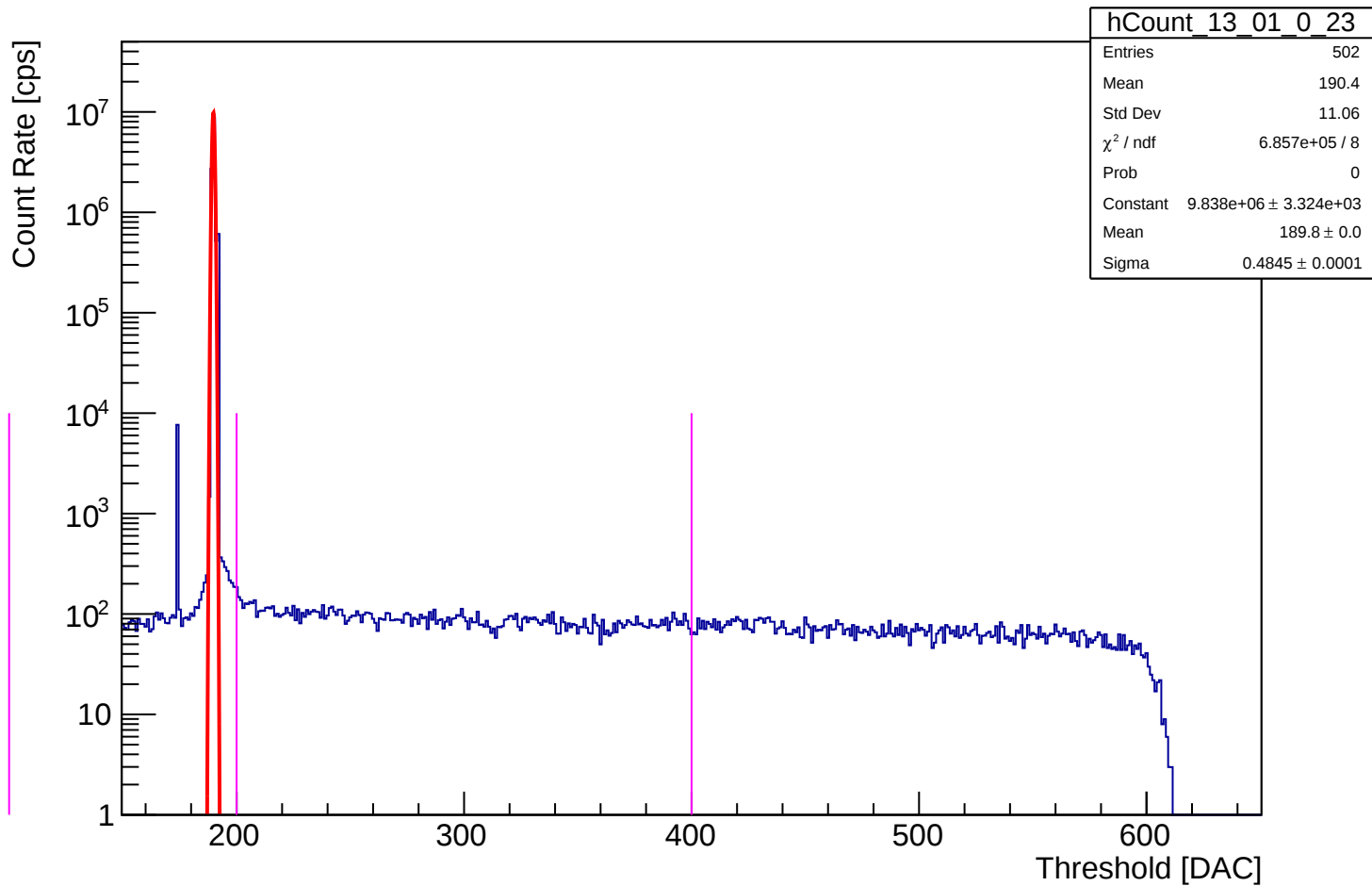
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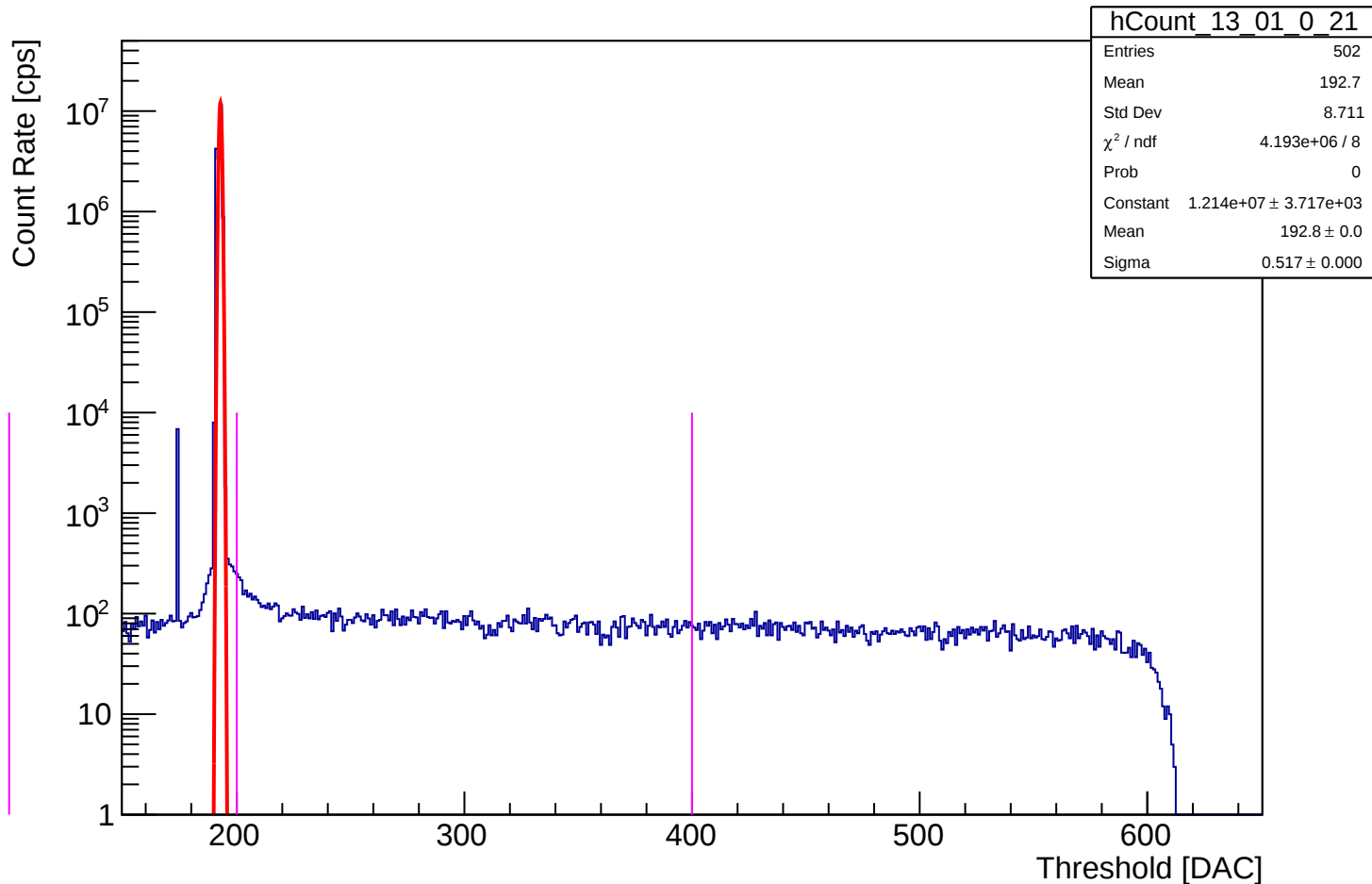
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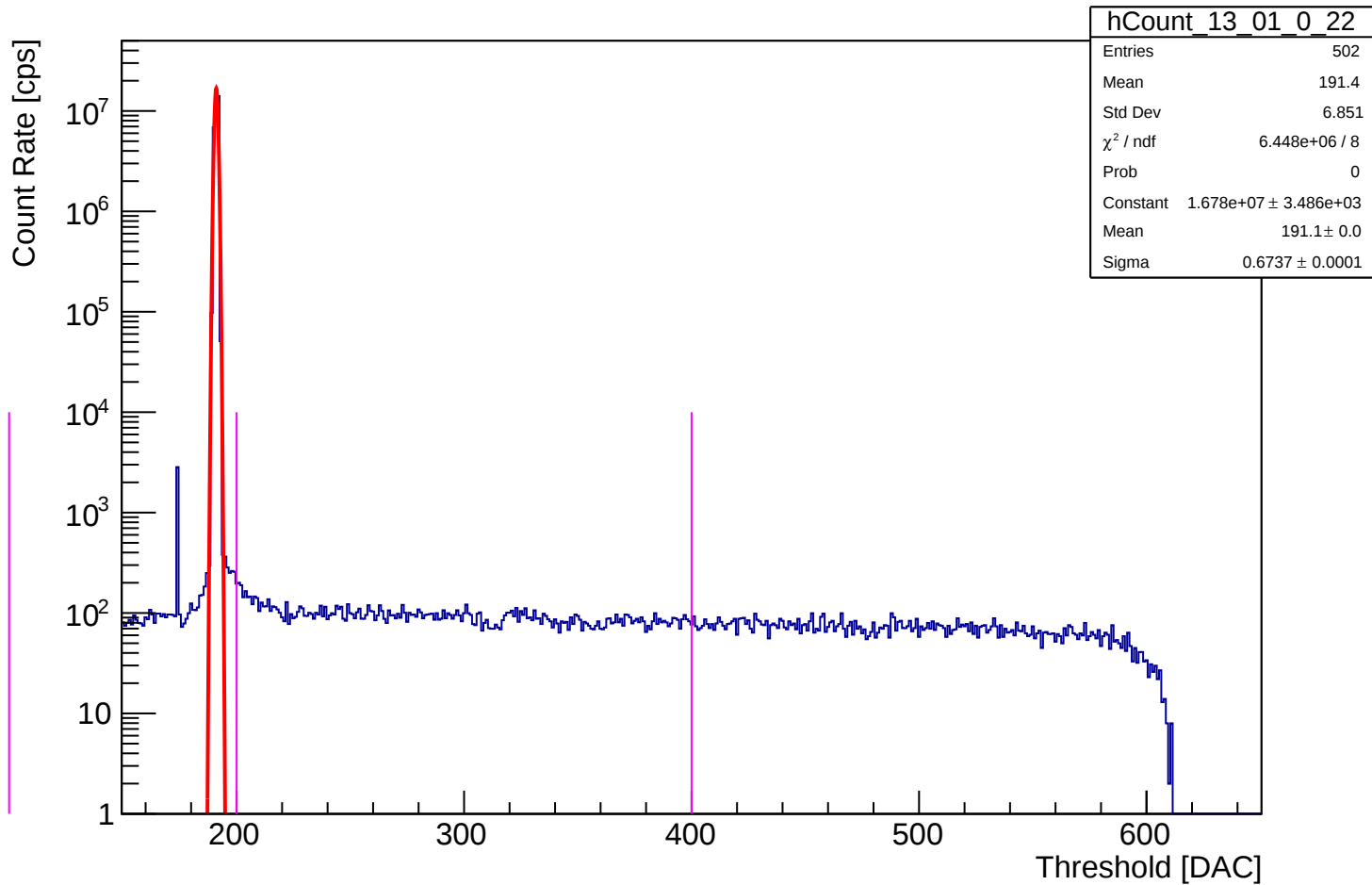
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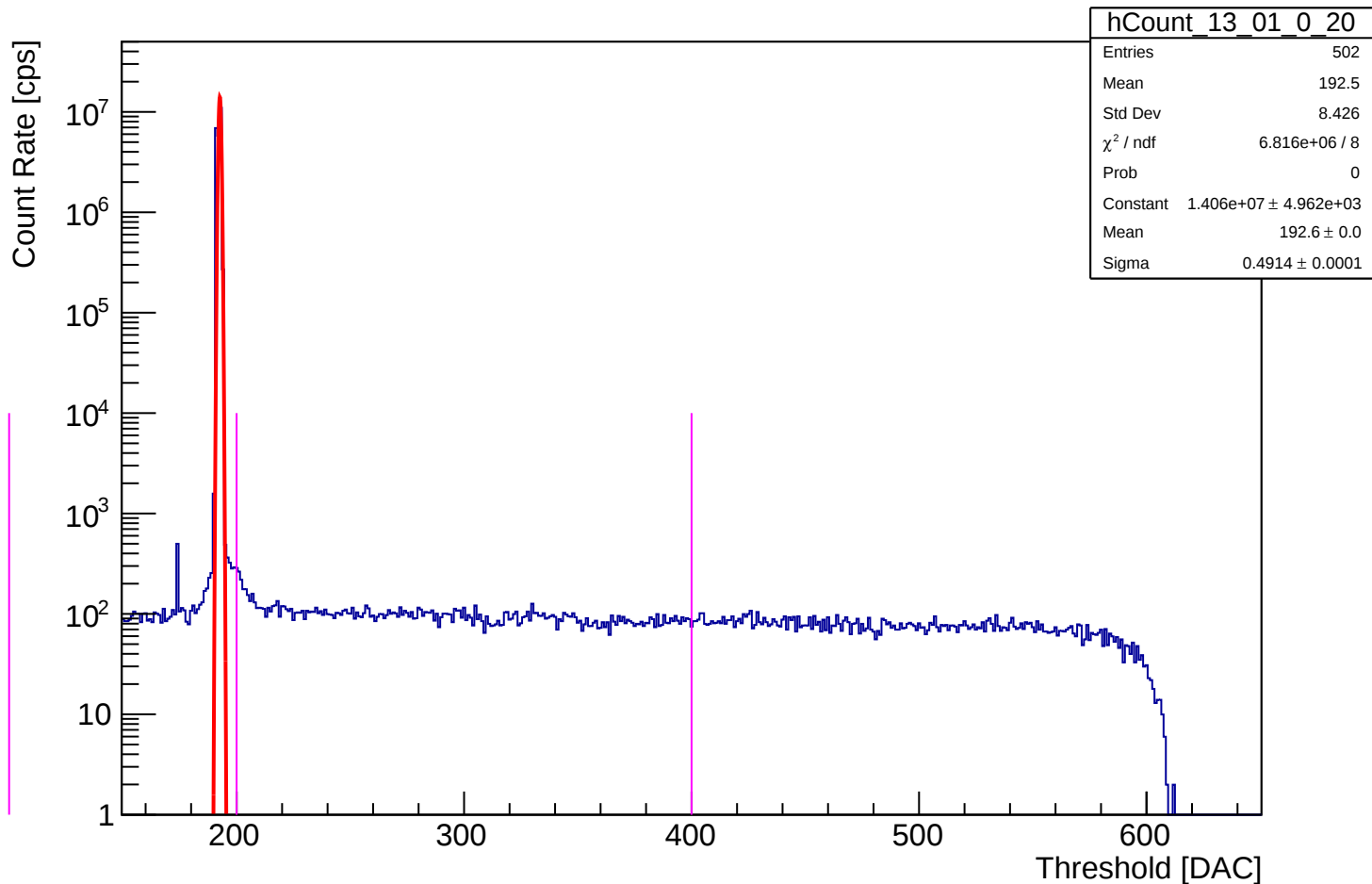
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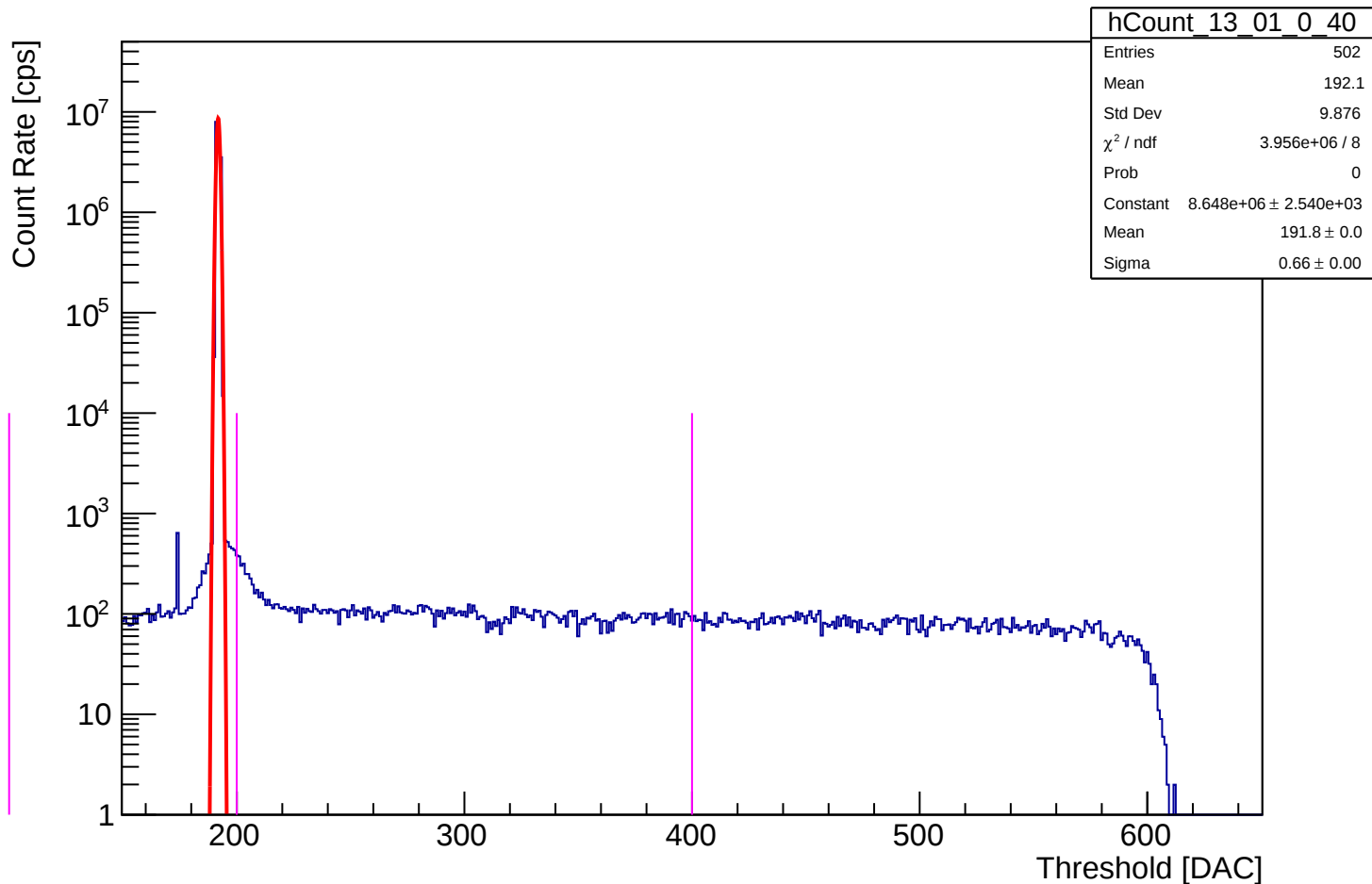
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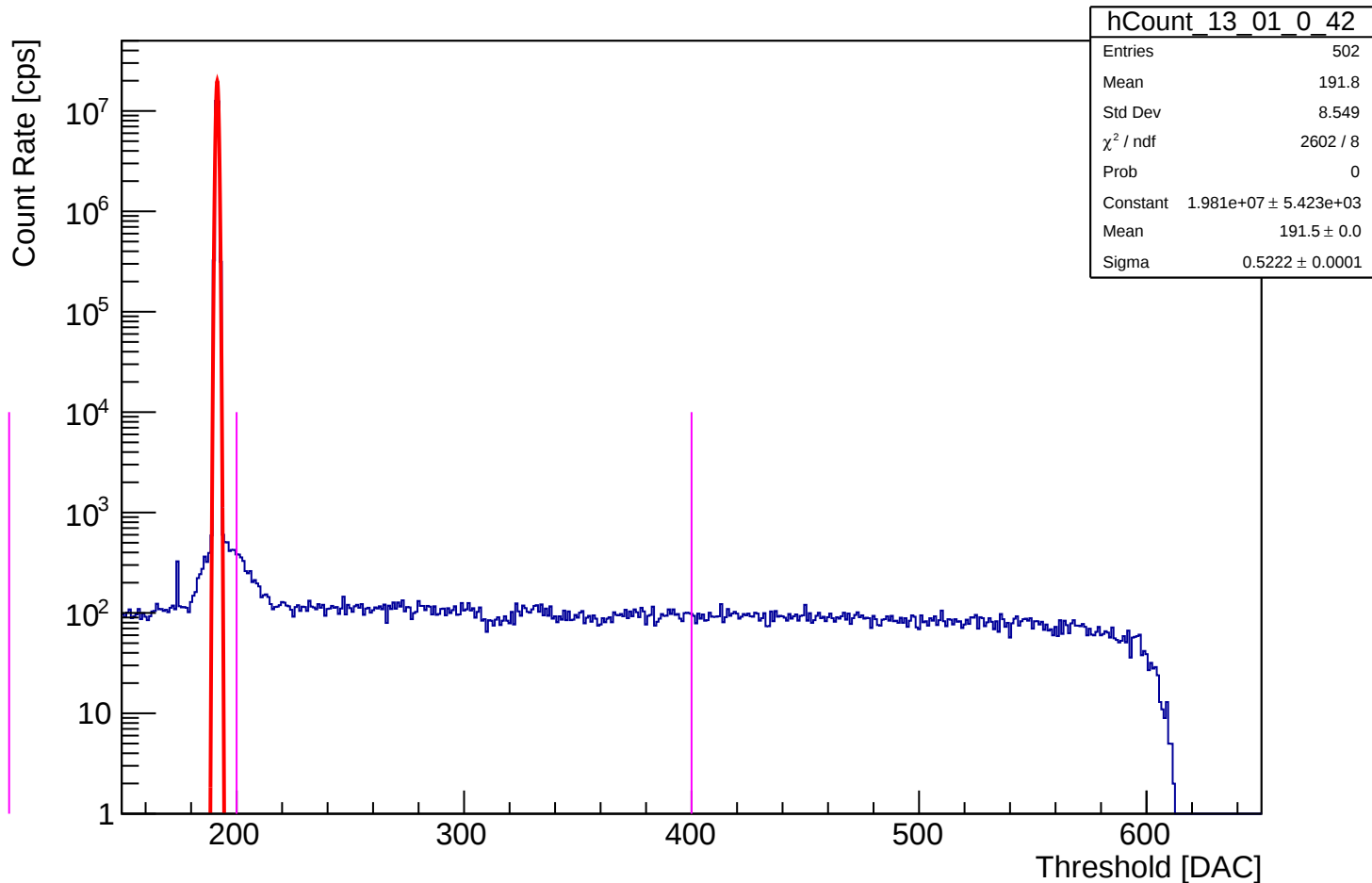
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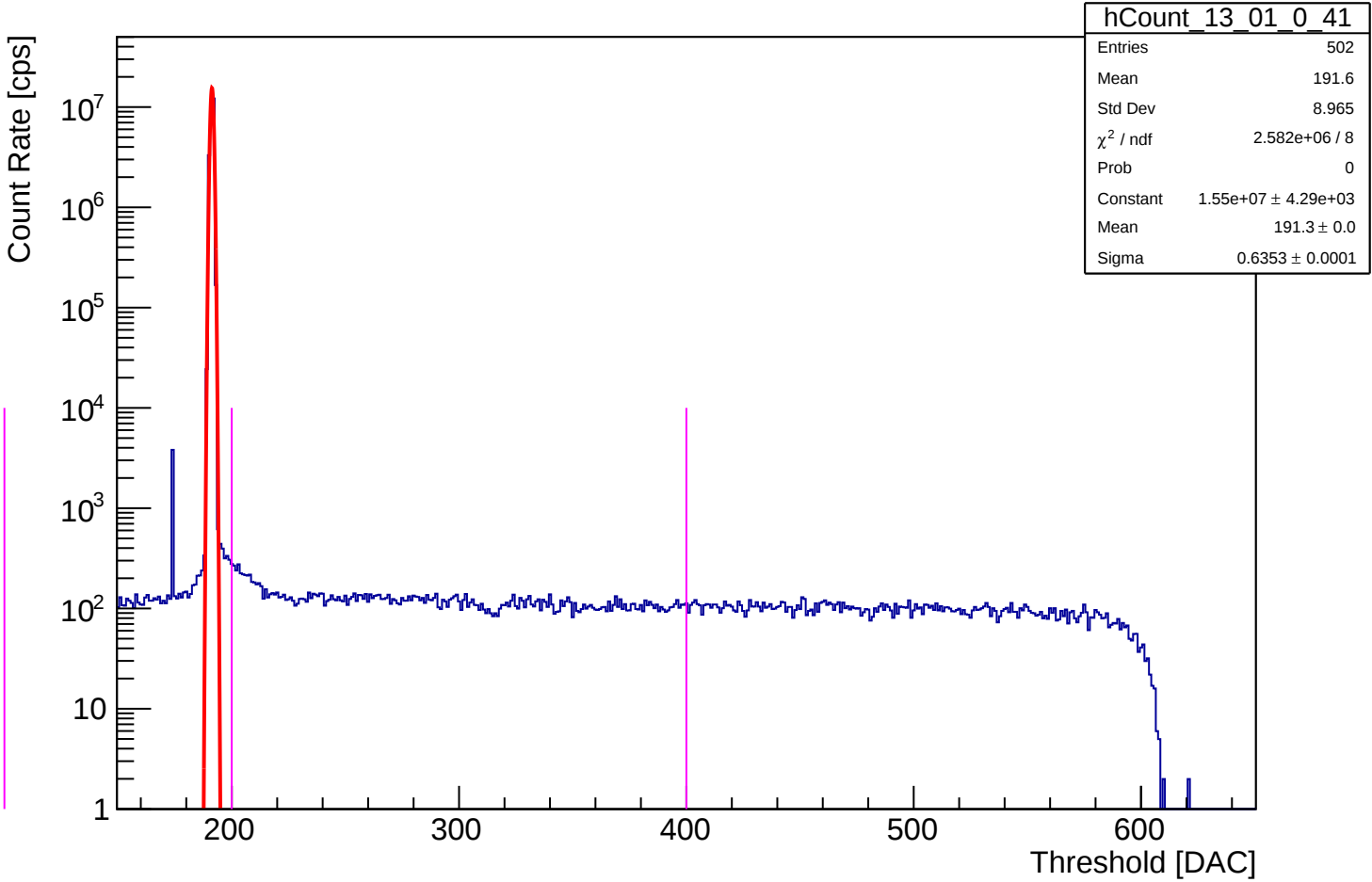


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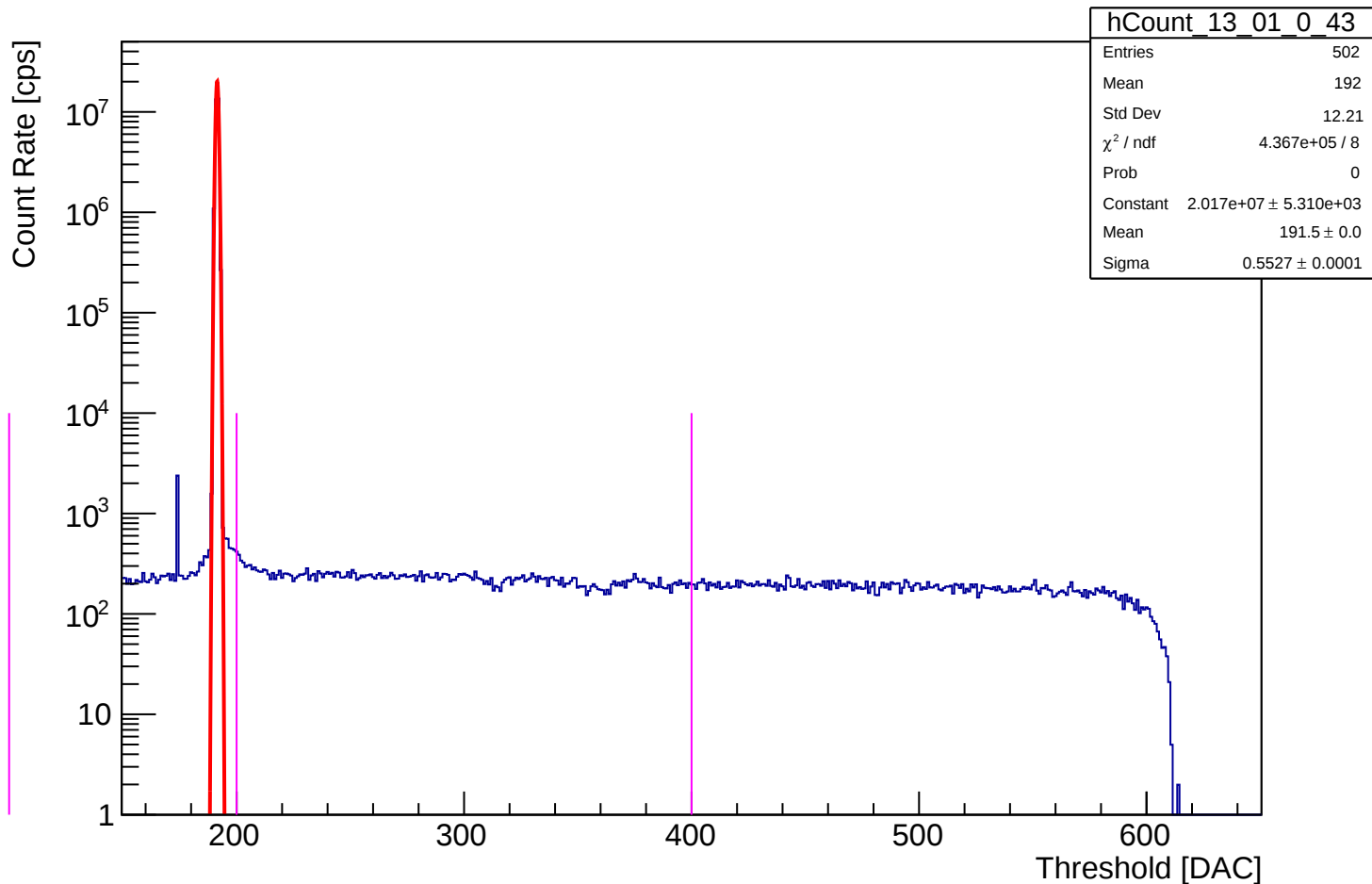


Row 1 Tile 1 Pmt 4 Pixel 22 Slot 13 Fiber 1 Asic 0 Channel 42

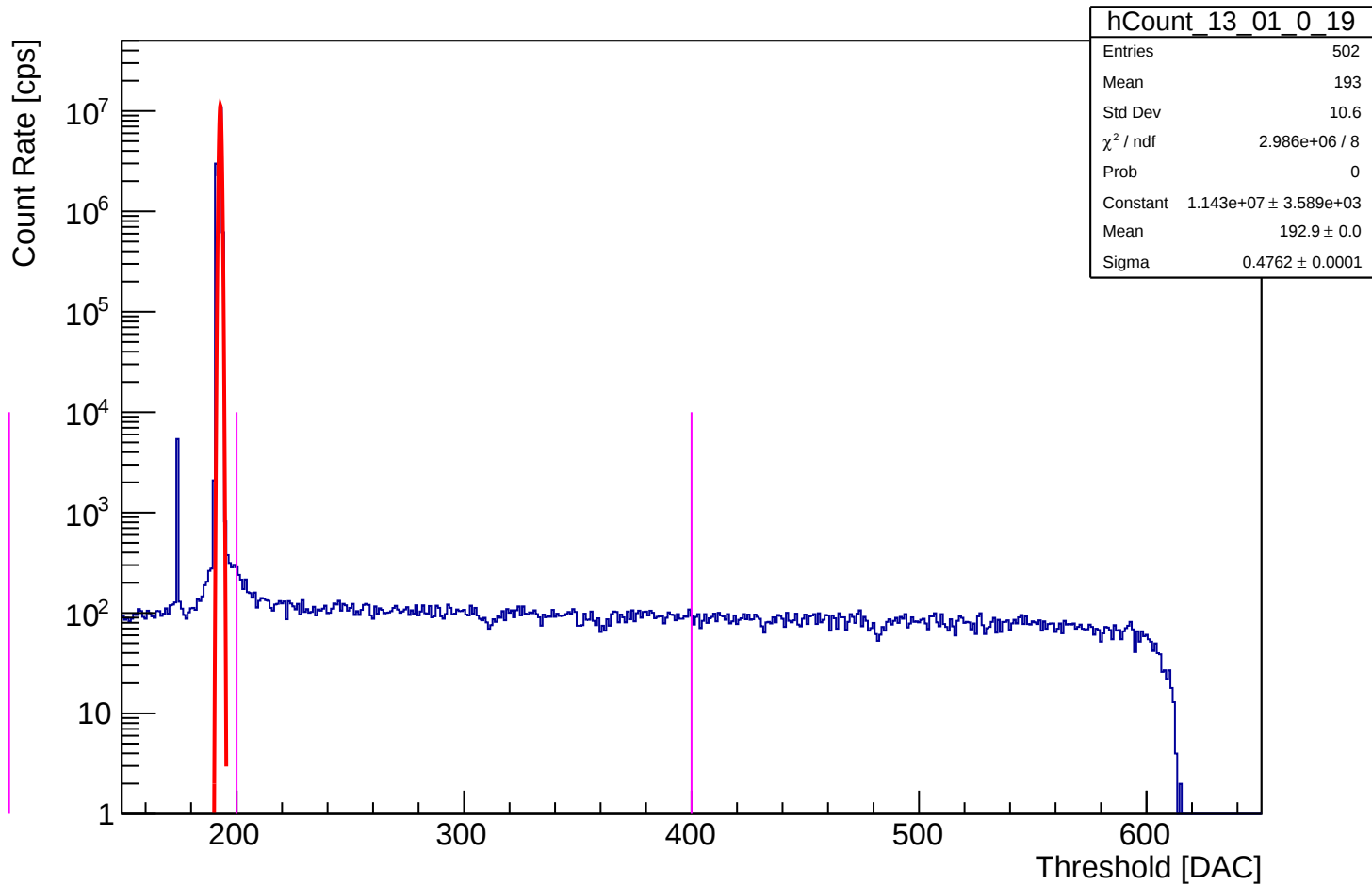




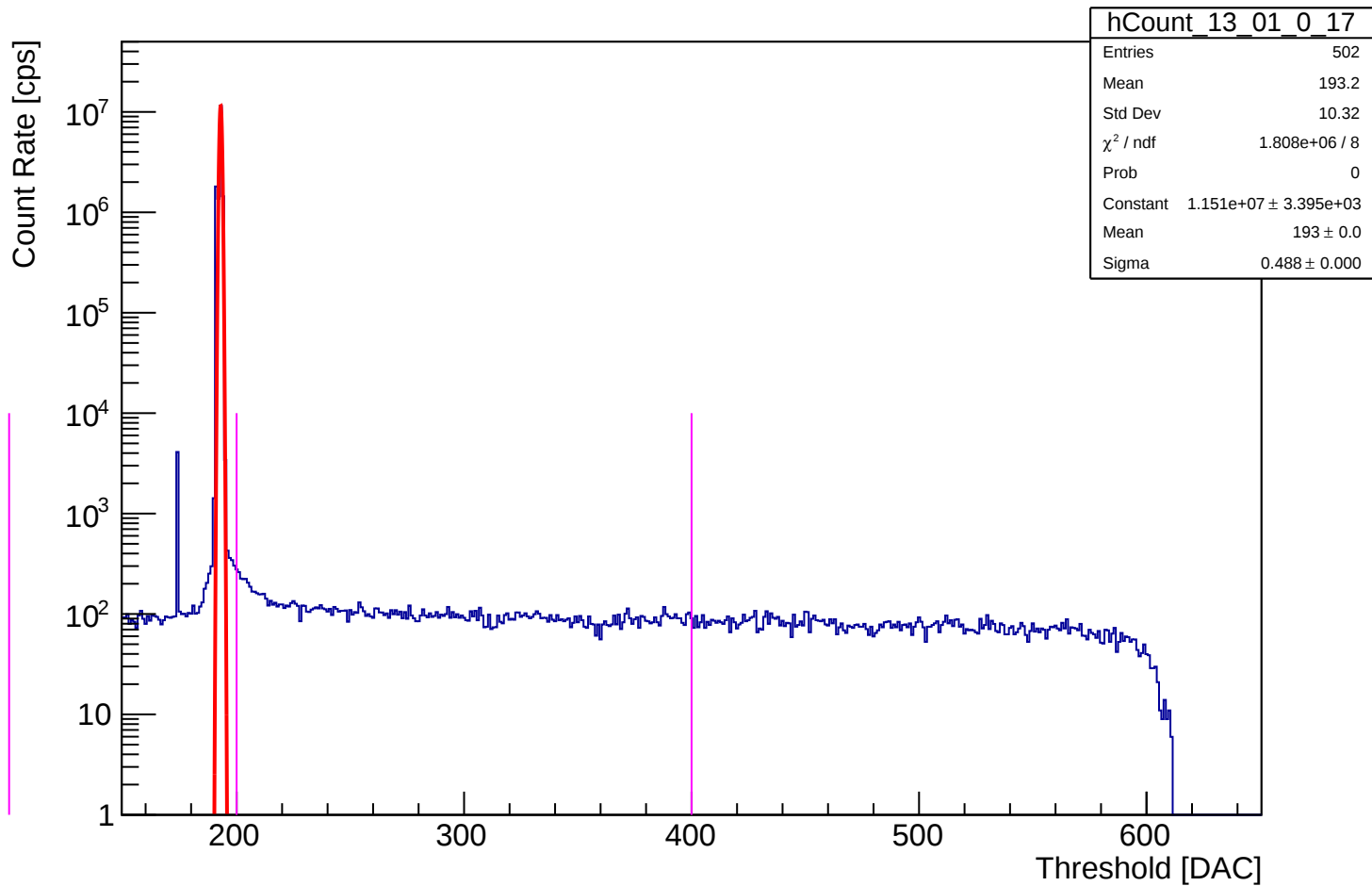
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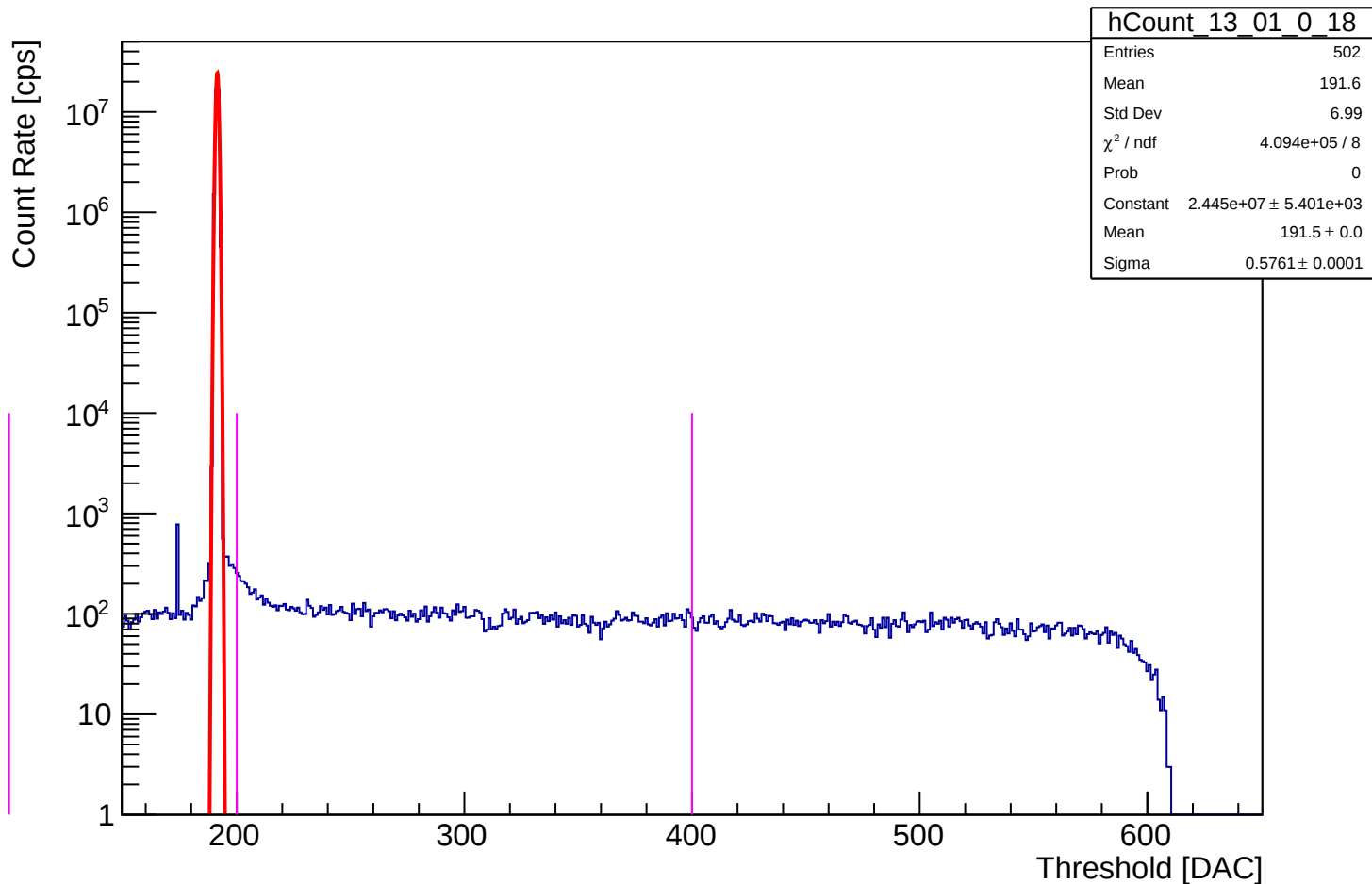
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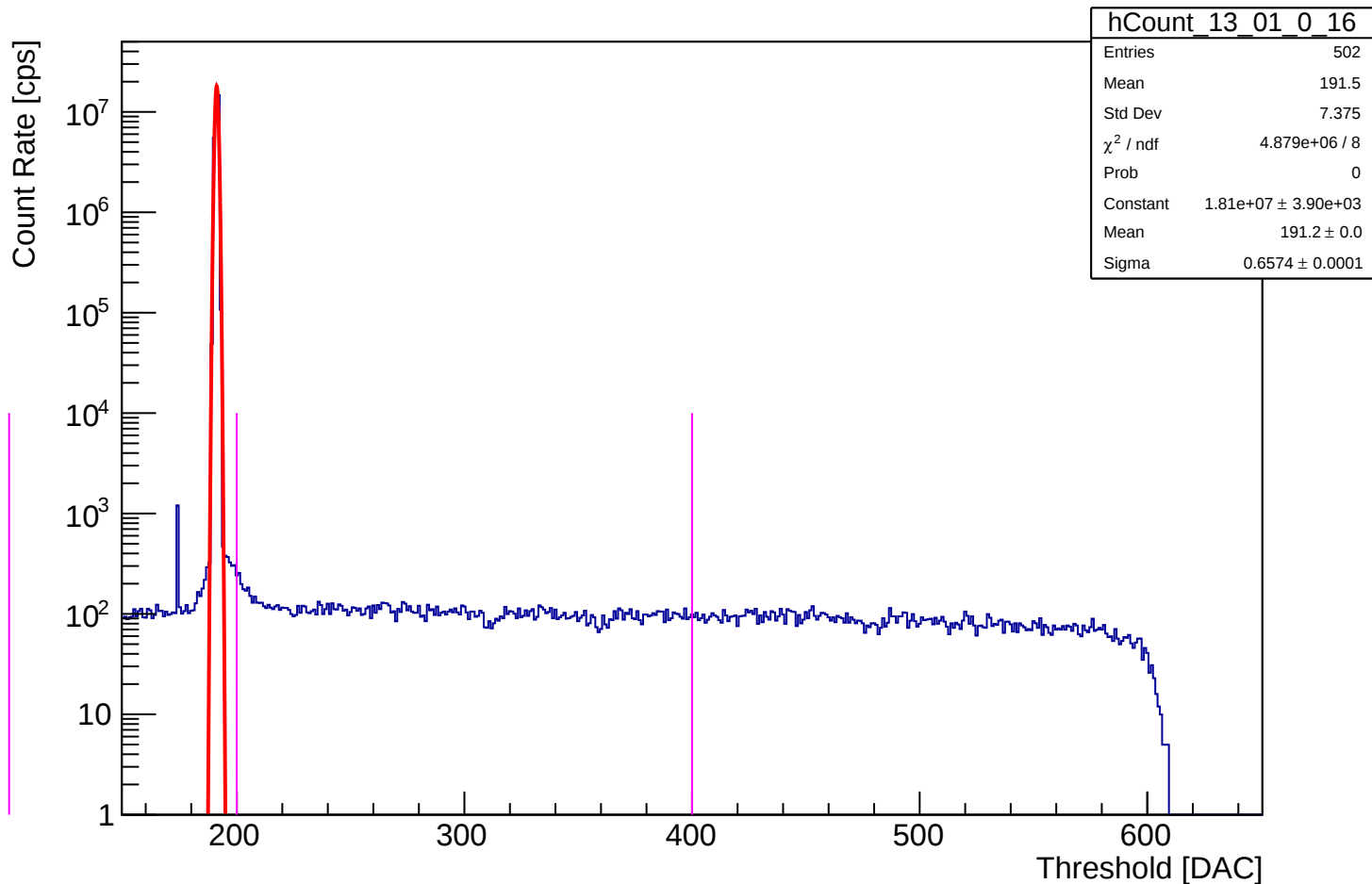
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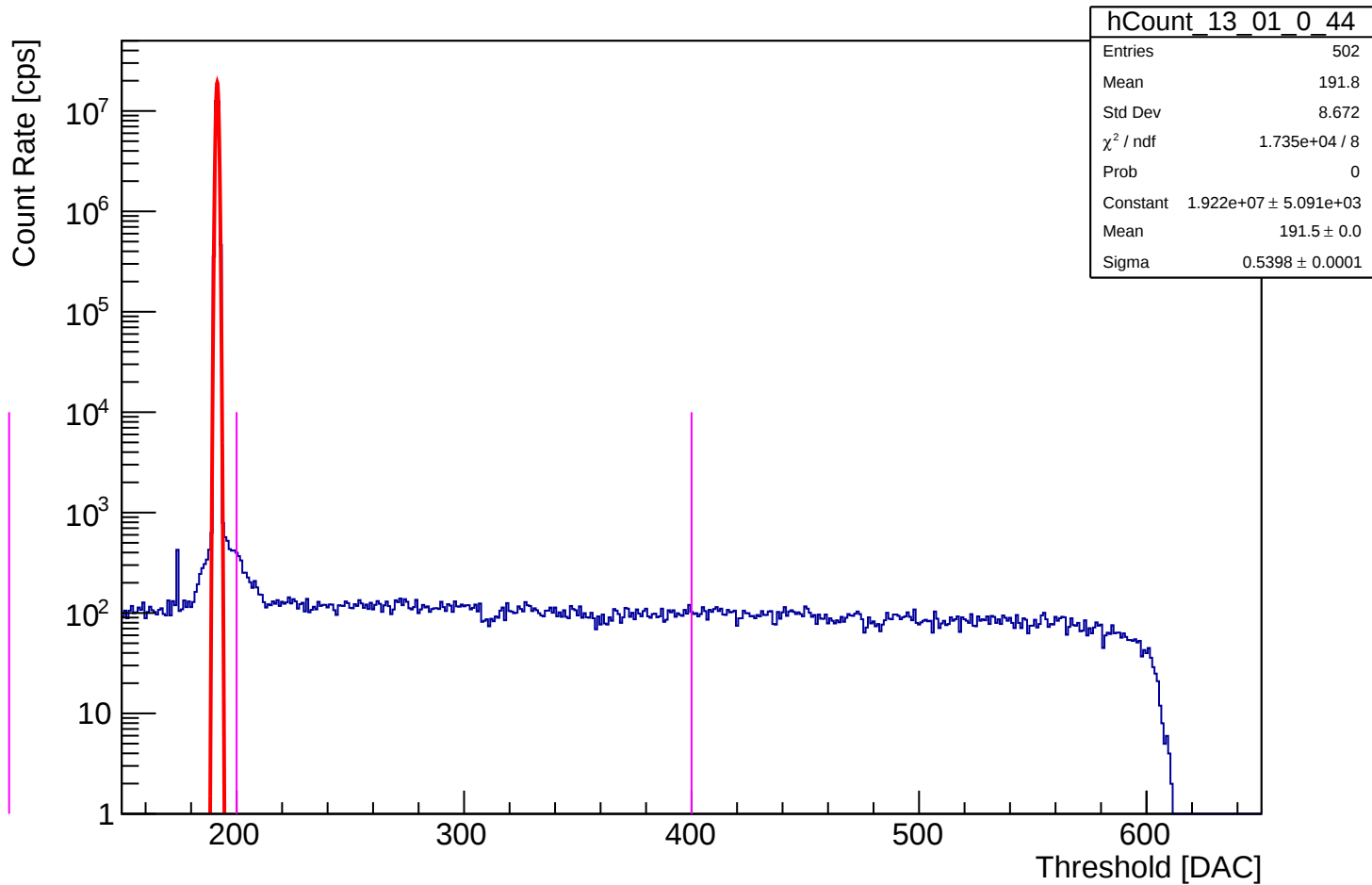
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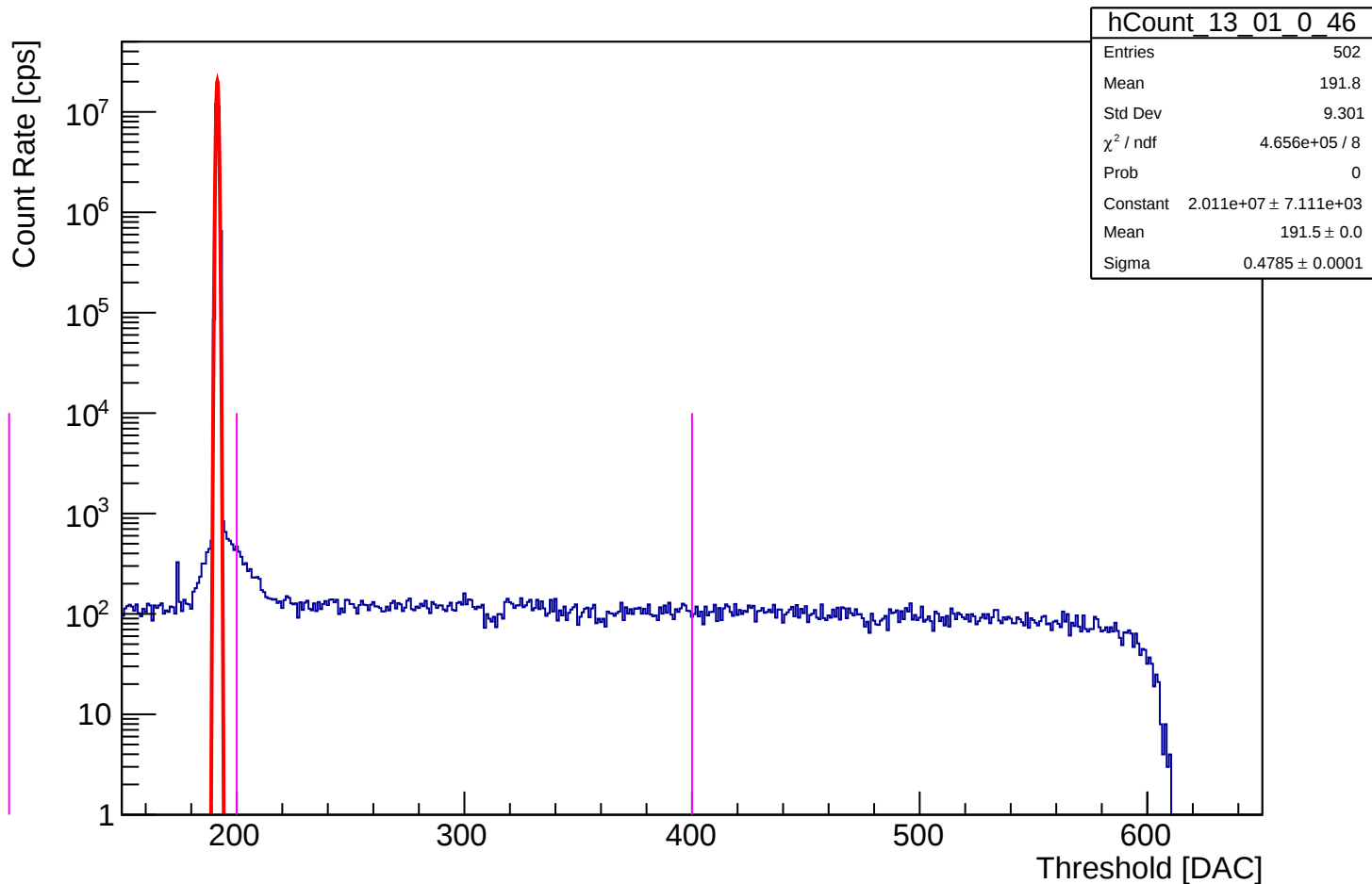
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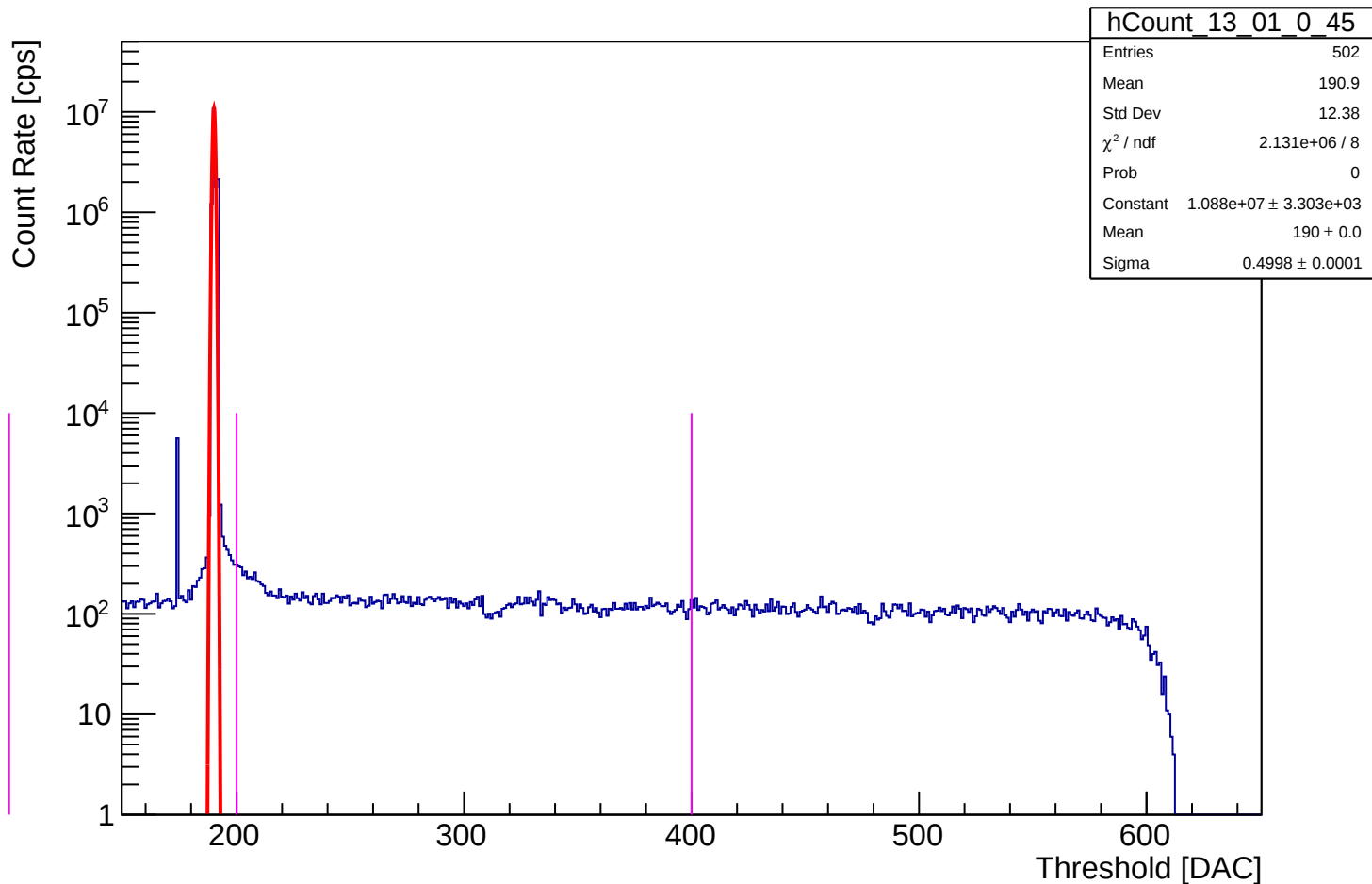
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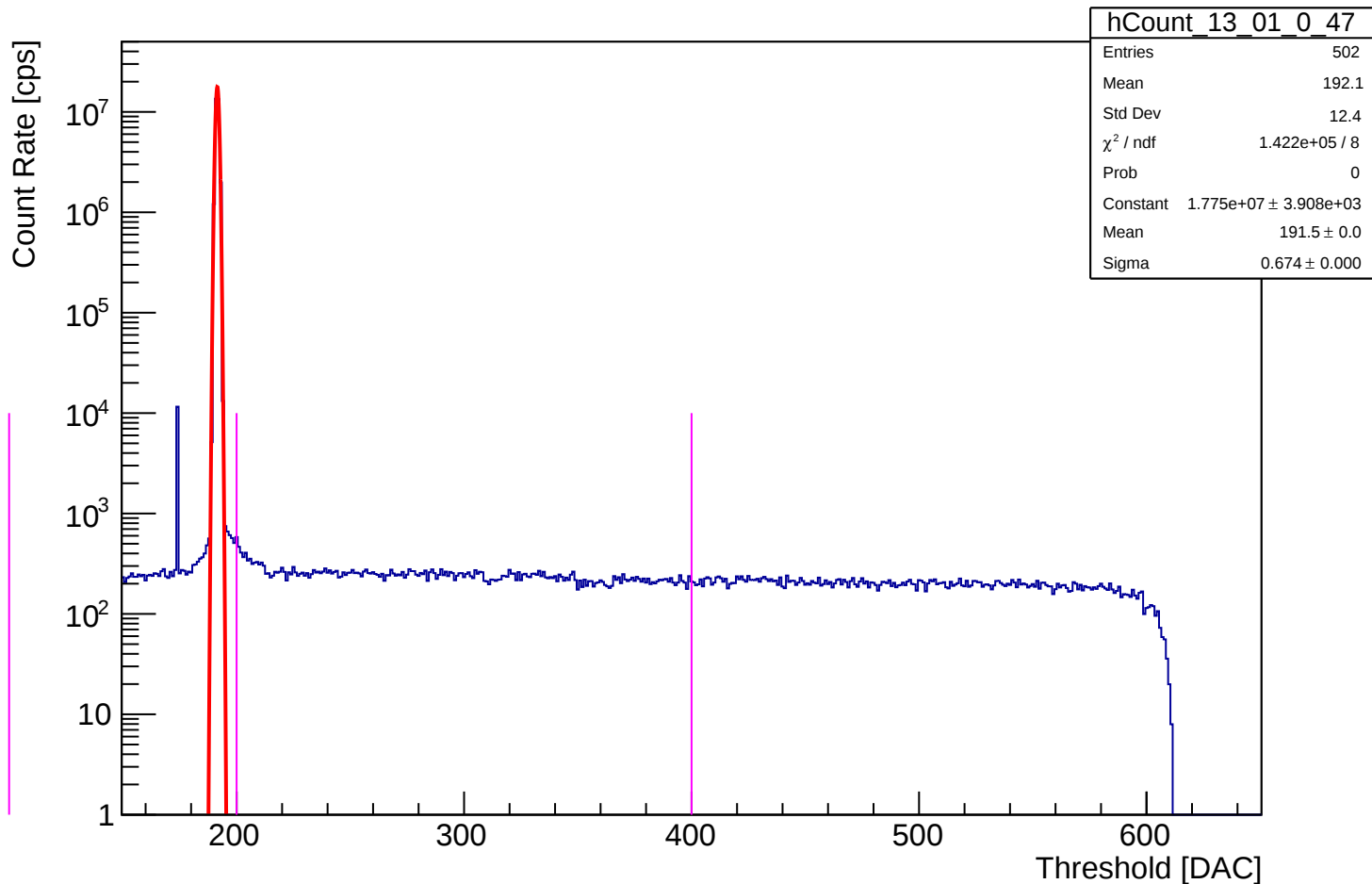
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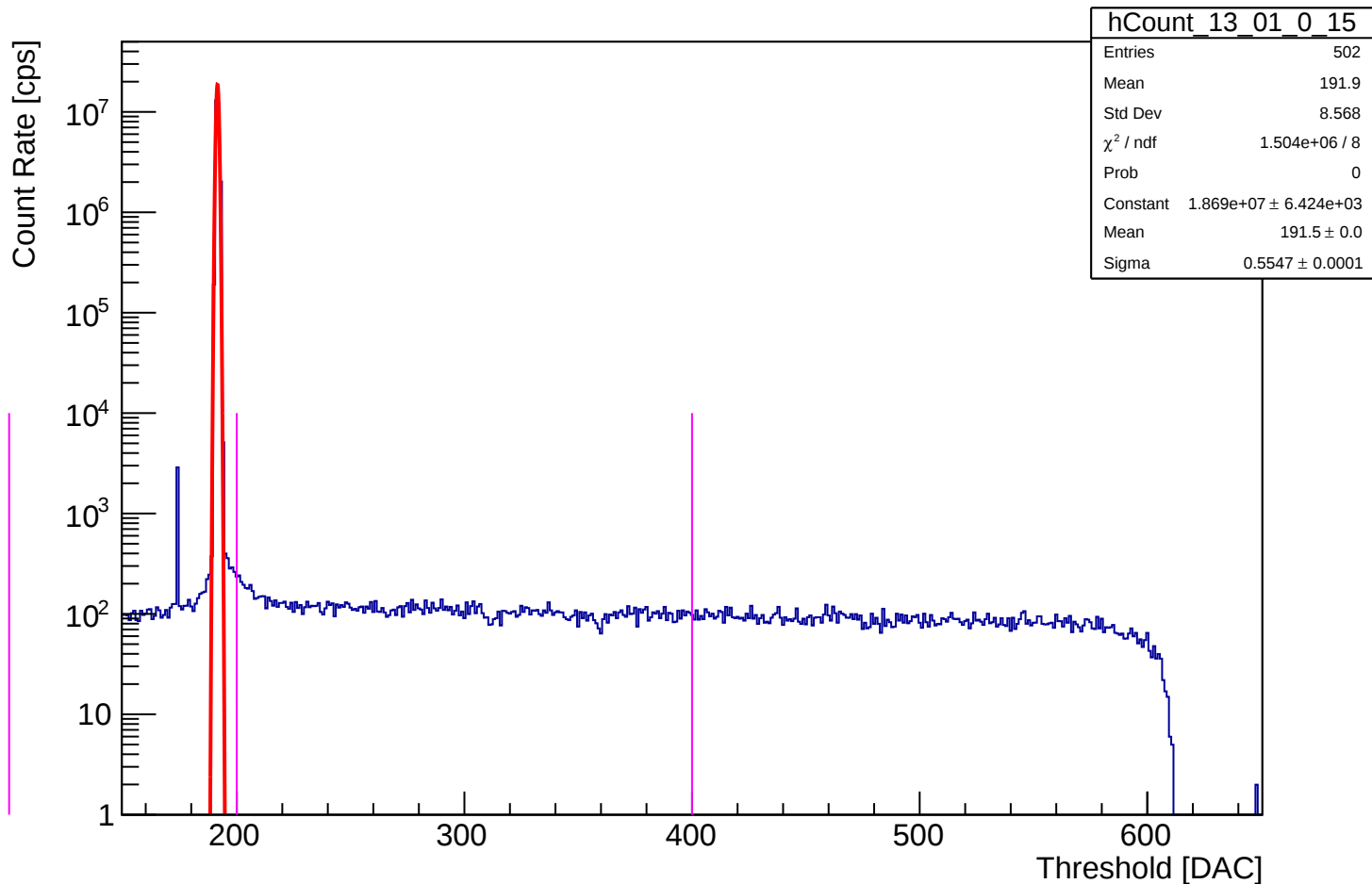
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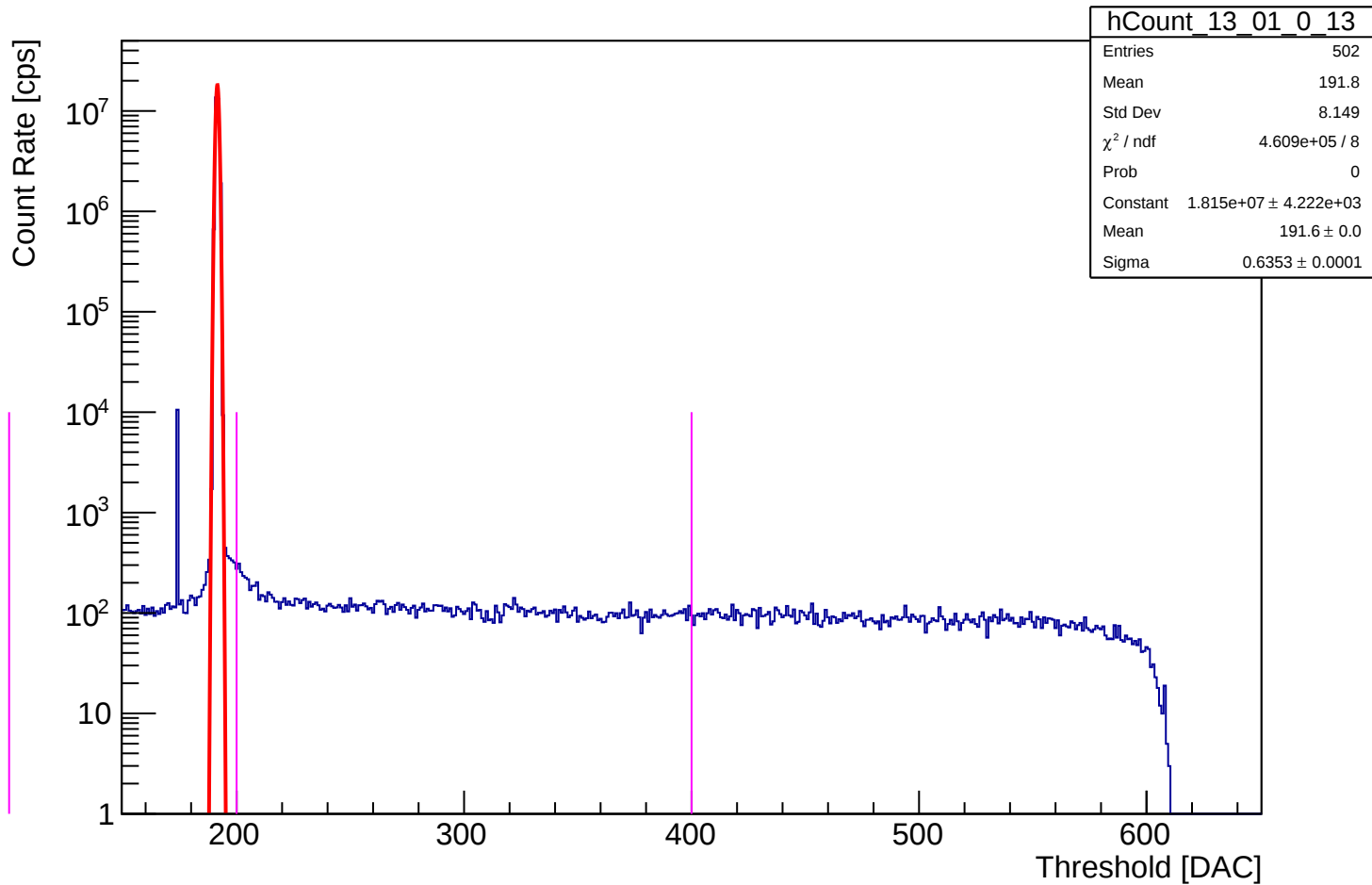
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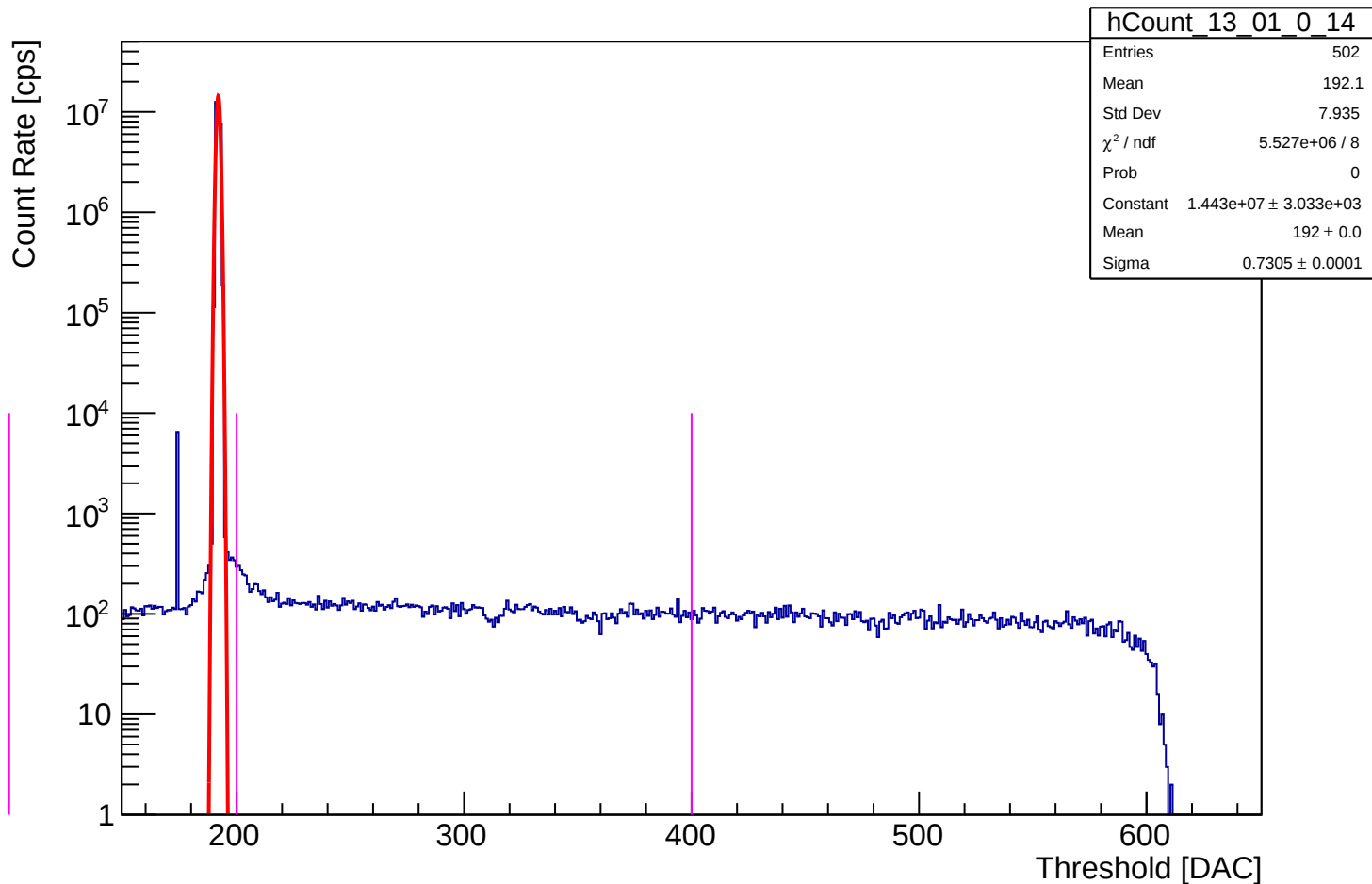
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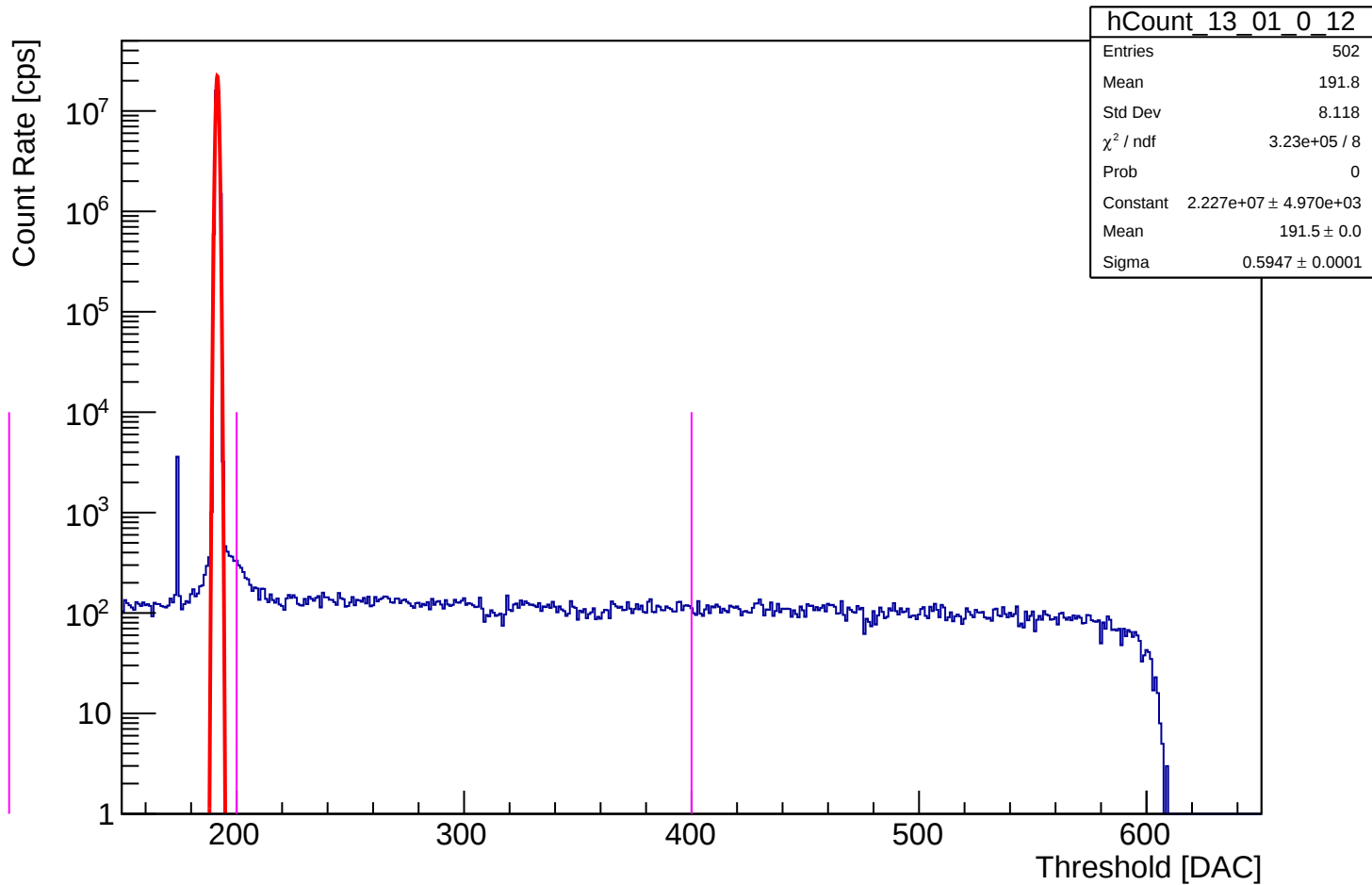
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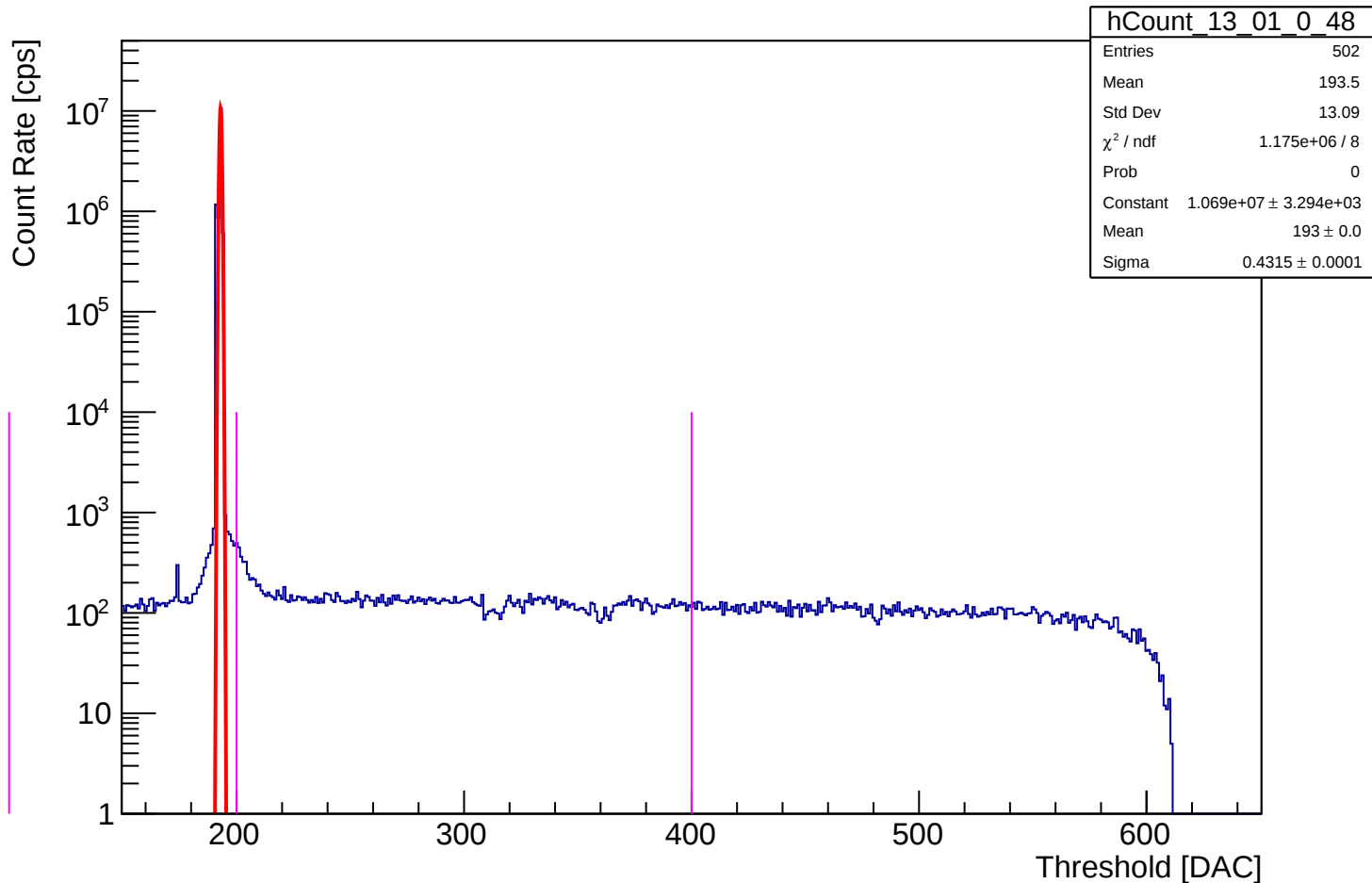
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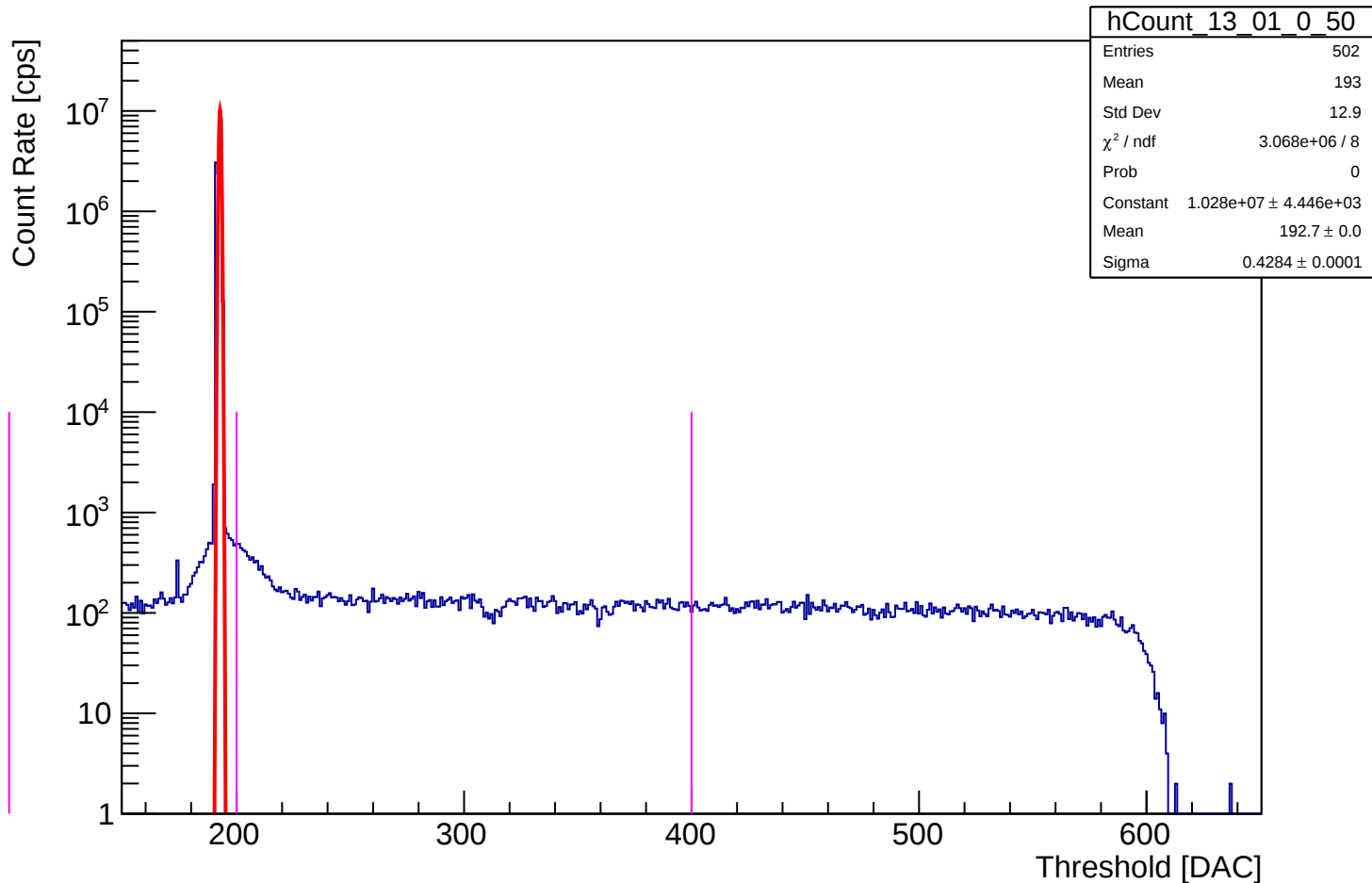
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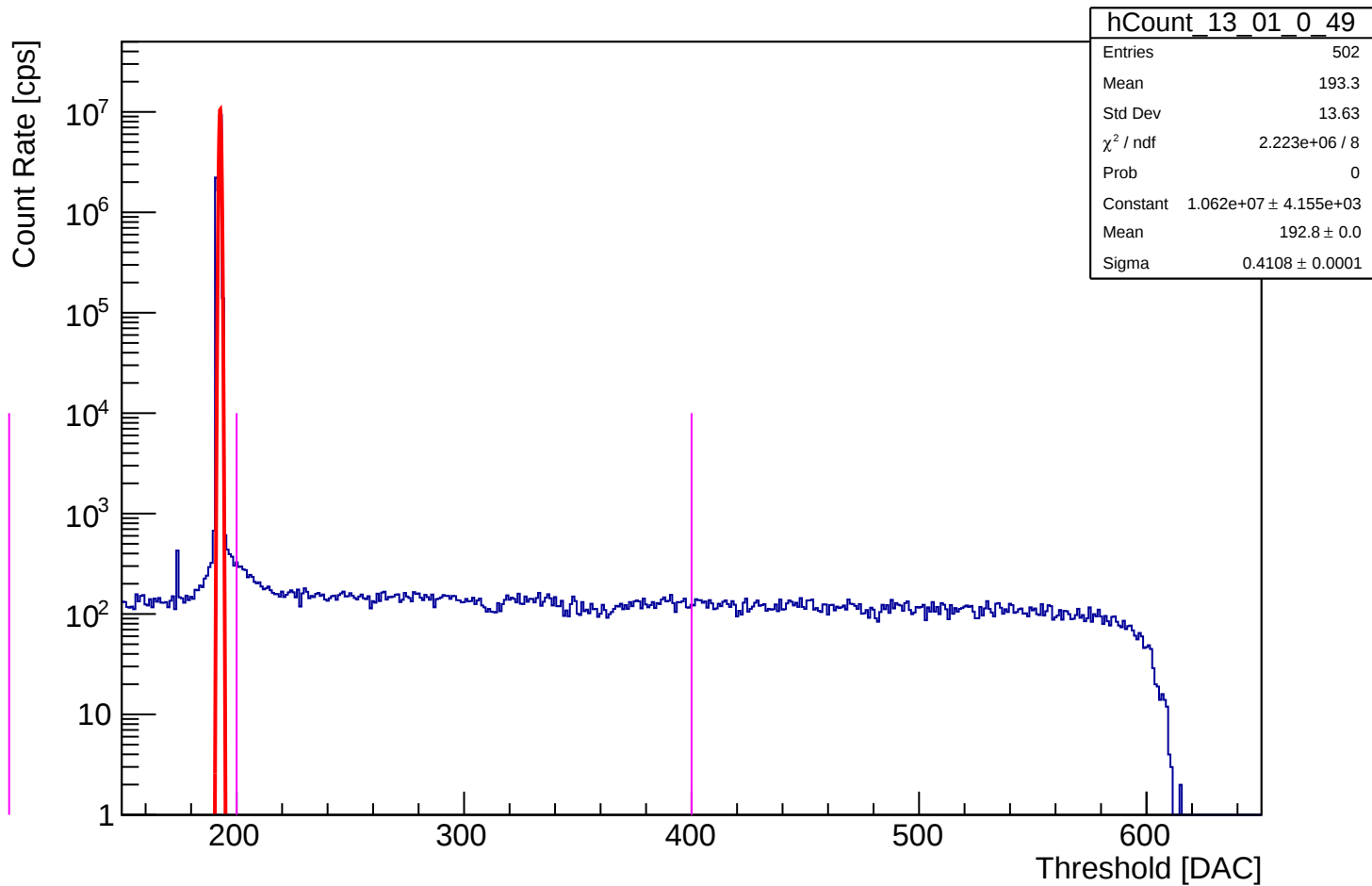
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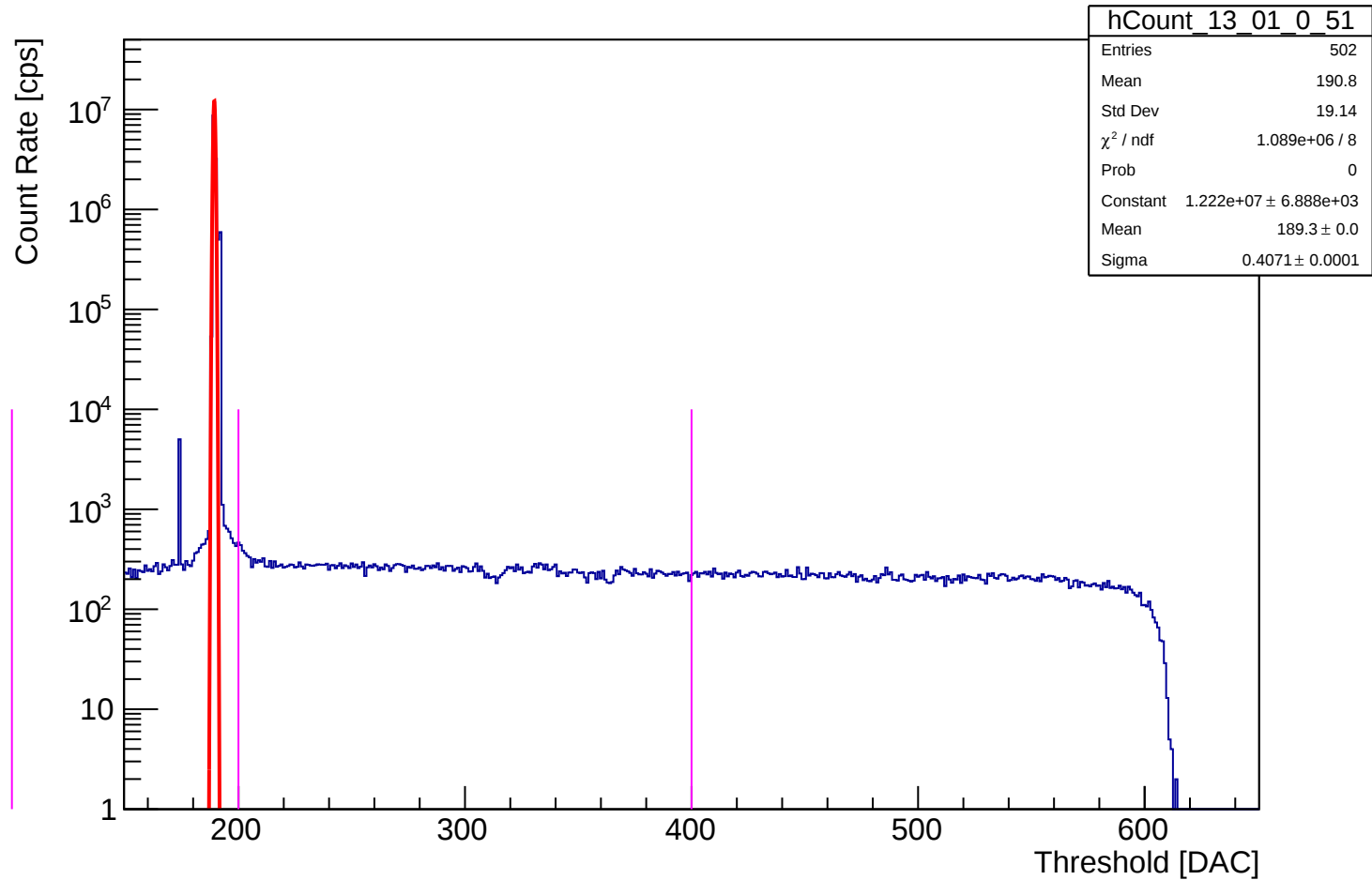


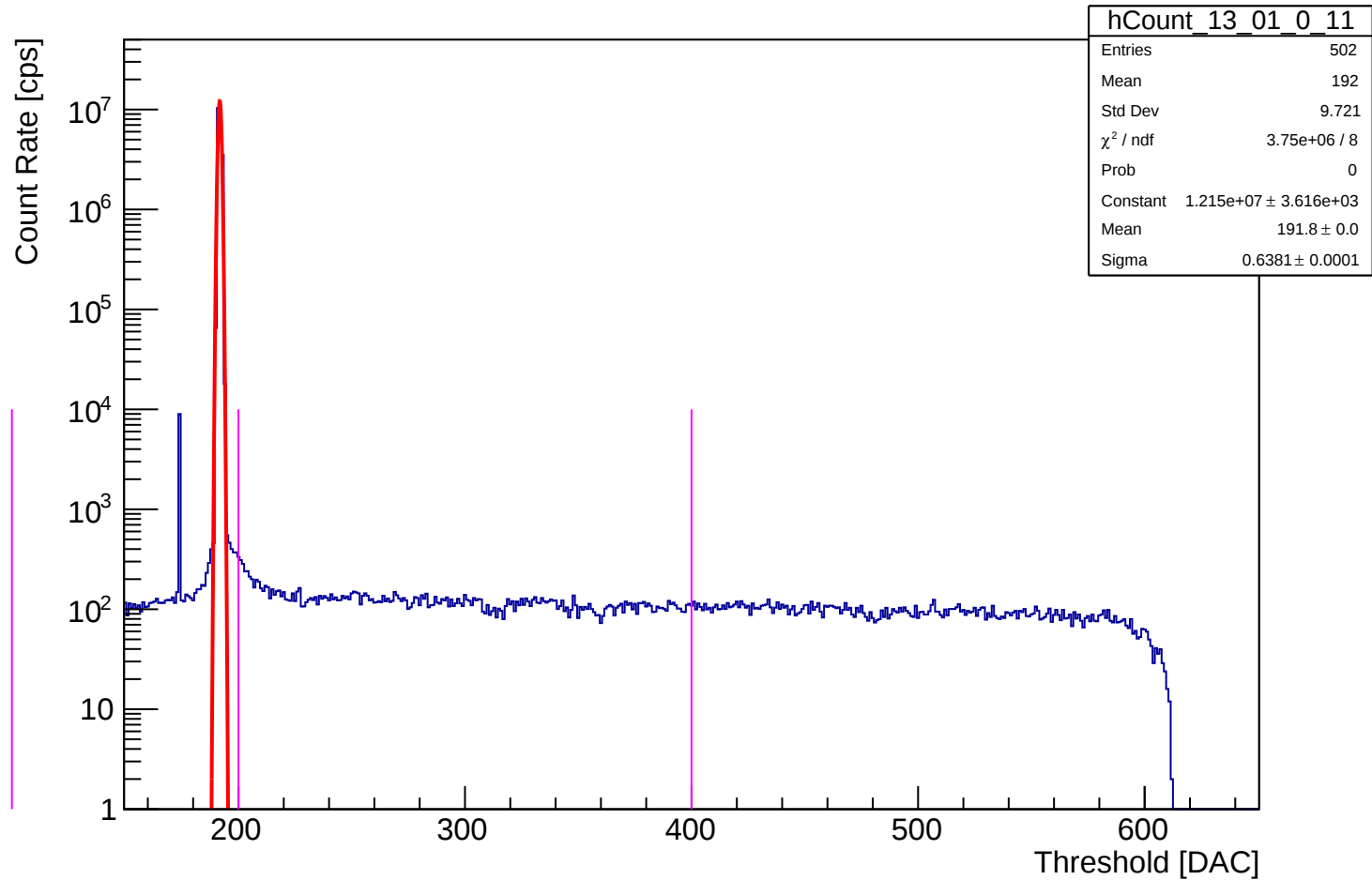
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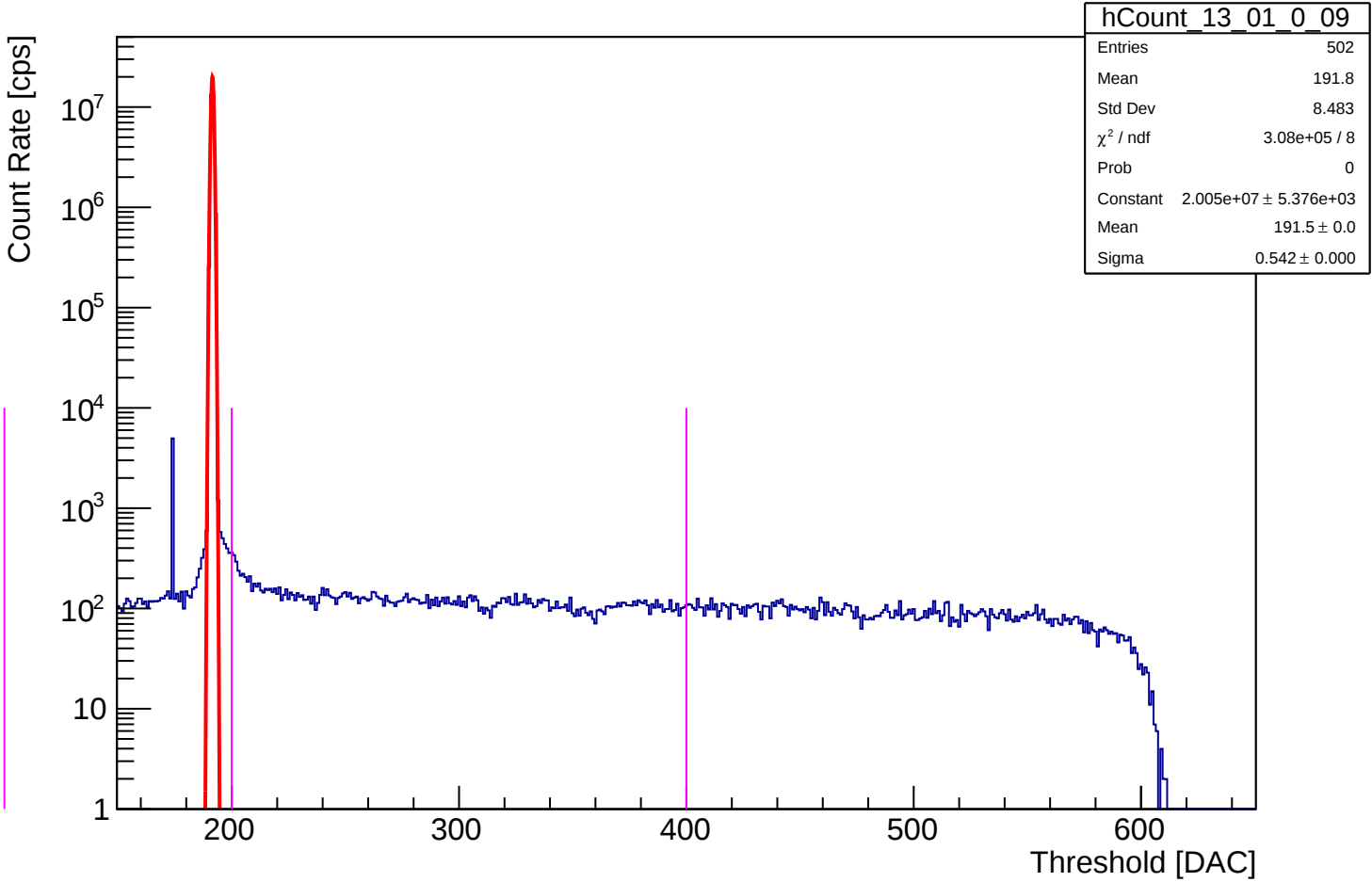


Row 1 Tile 1 Pmt 4 Pixel 39 Slot 13 Fiber 1 Asic 0 Channel 49

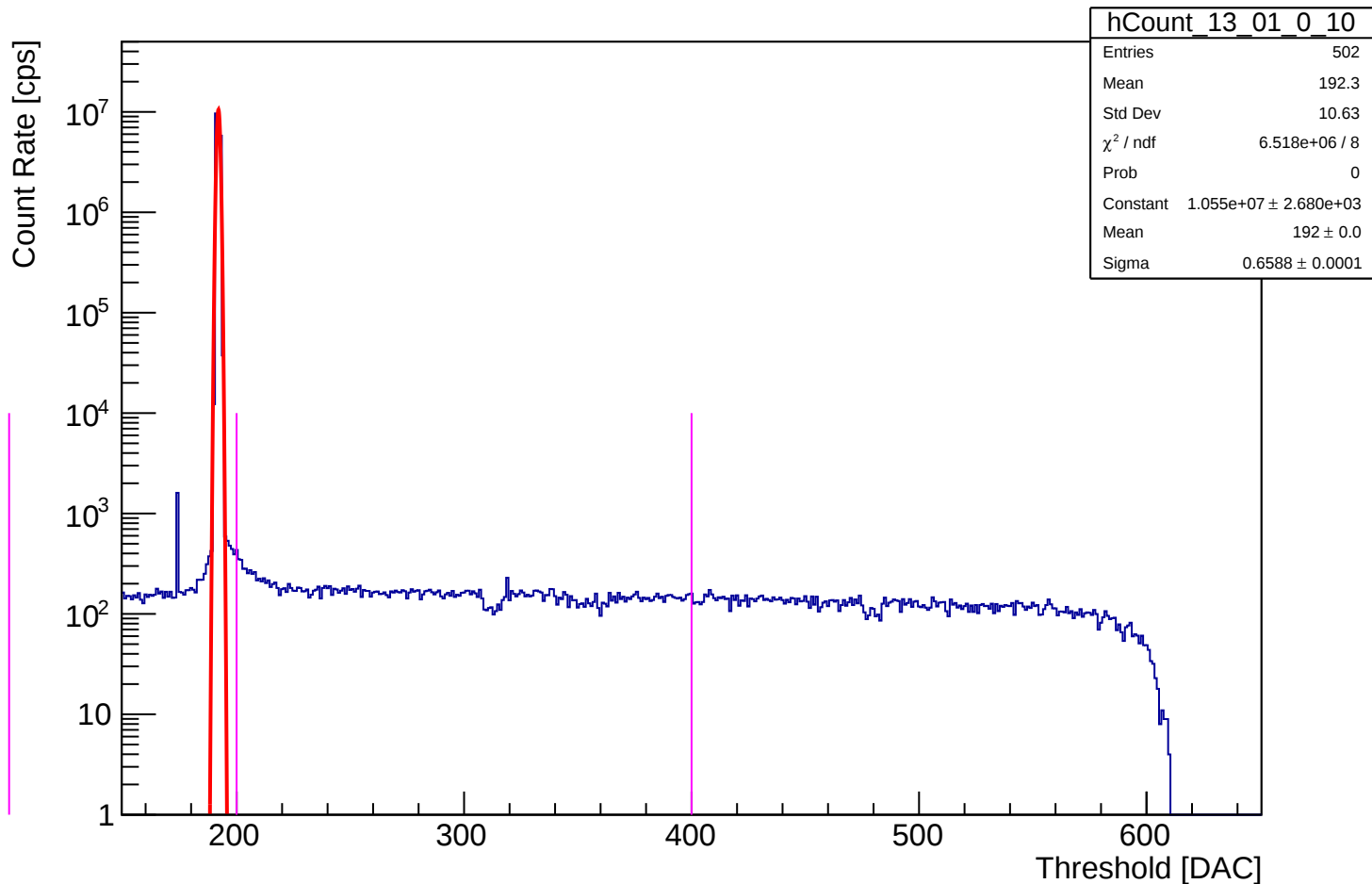


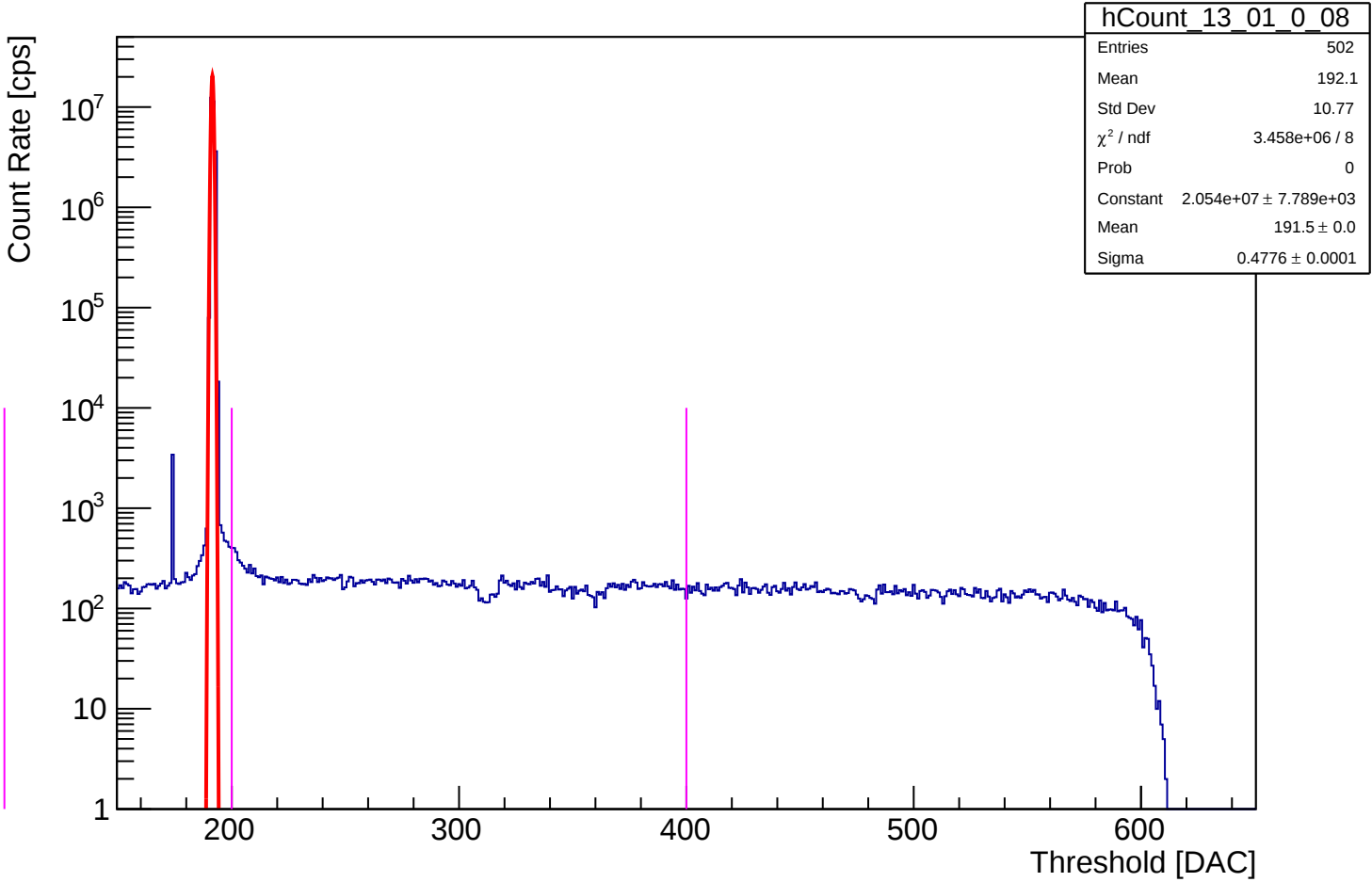




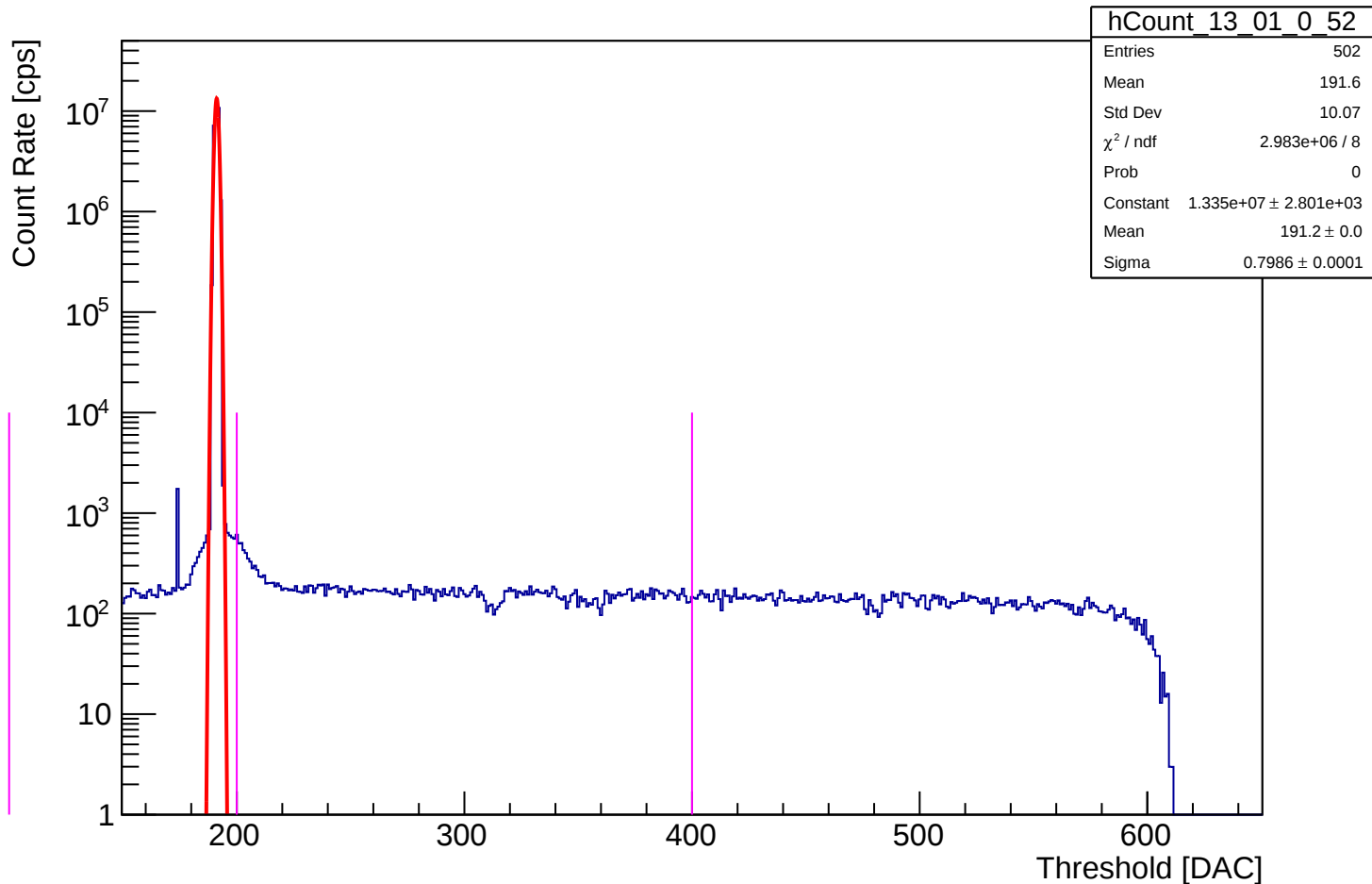


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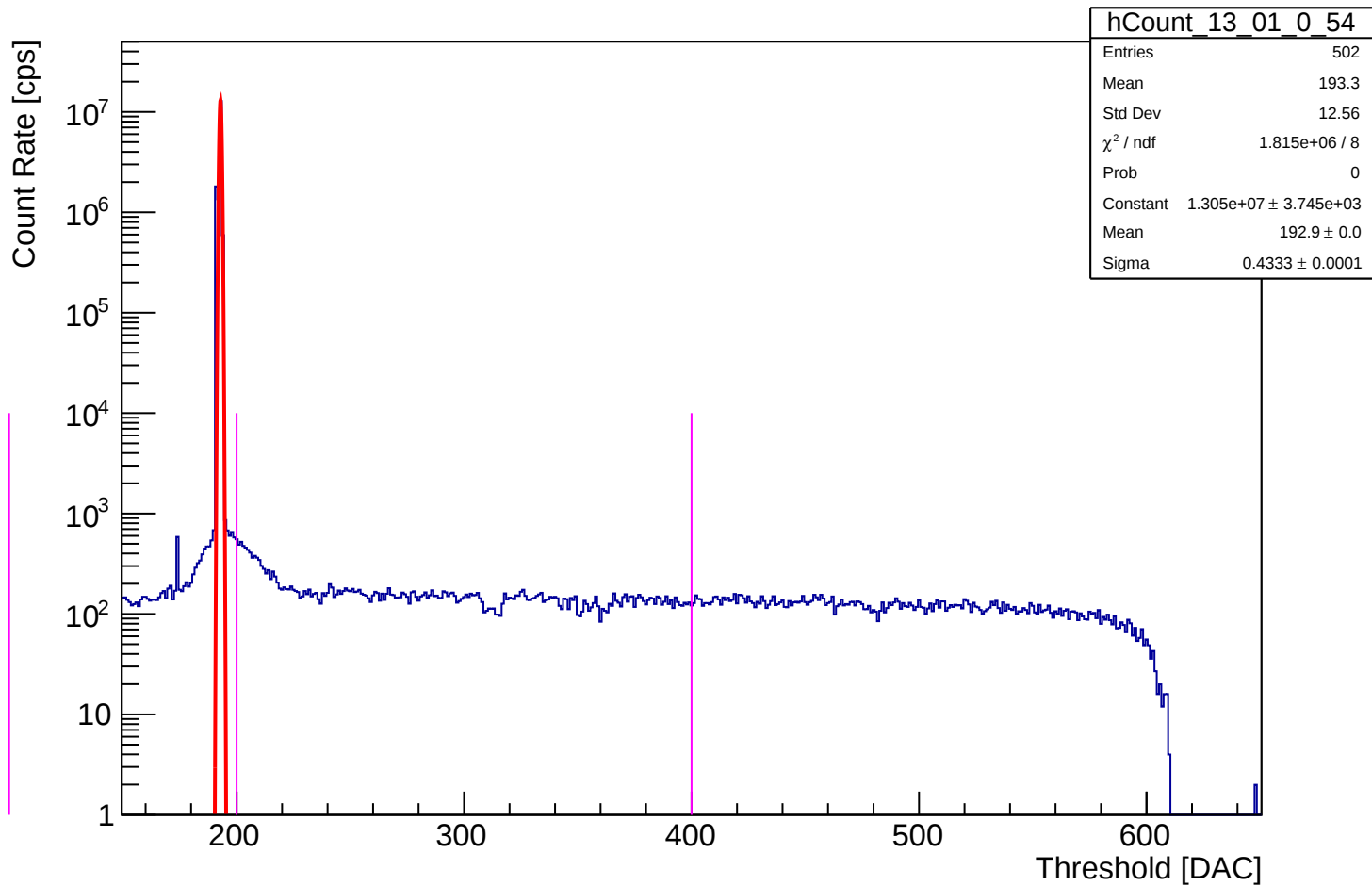




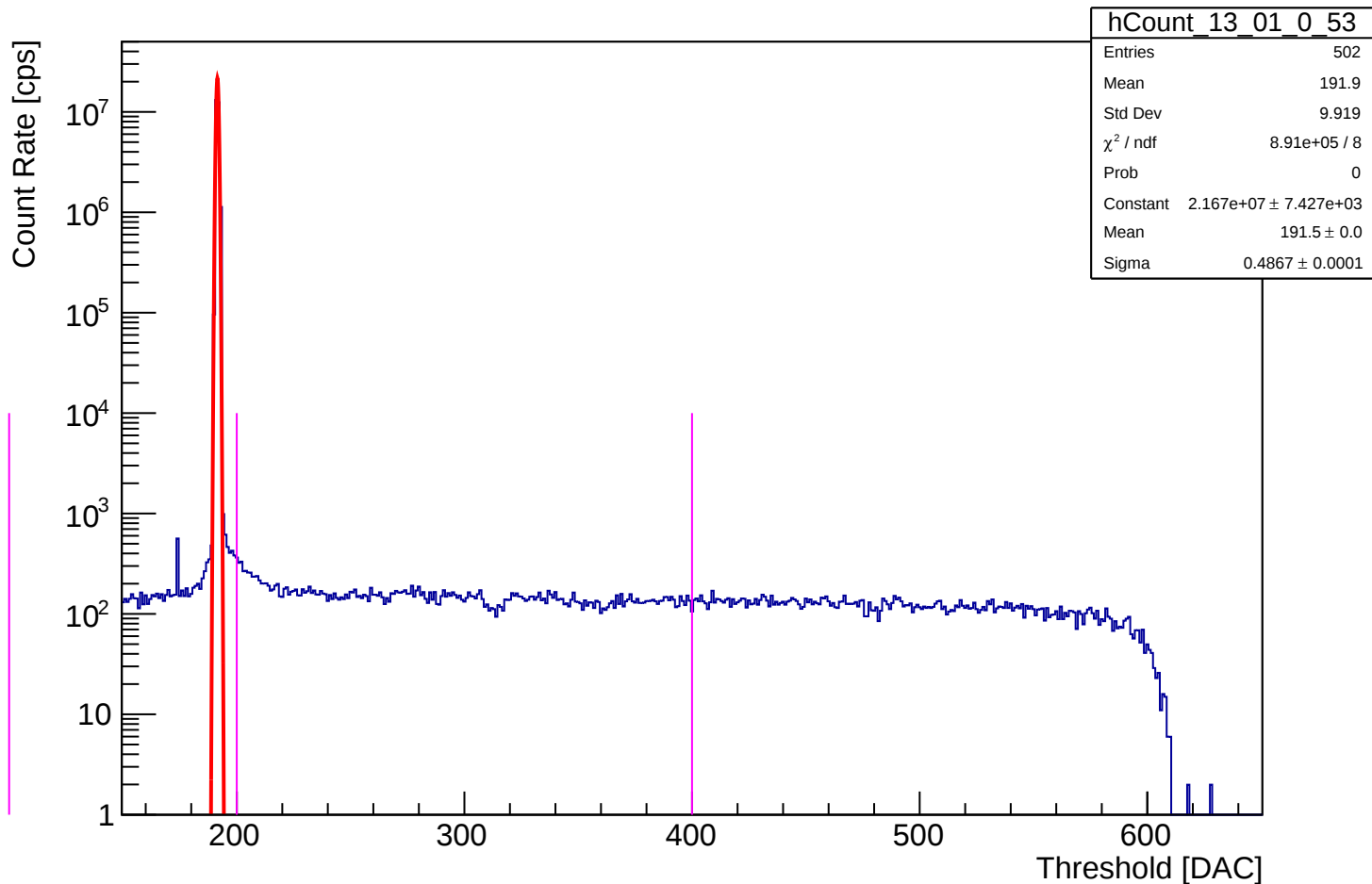
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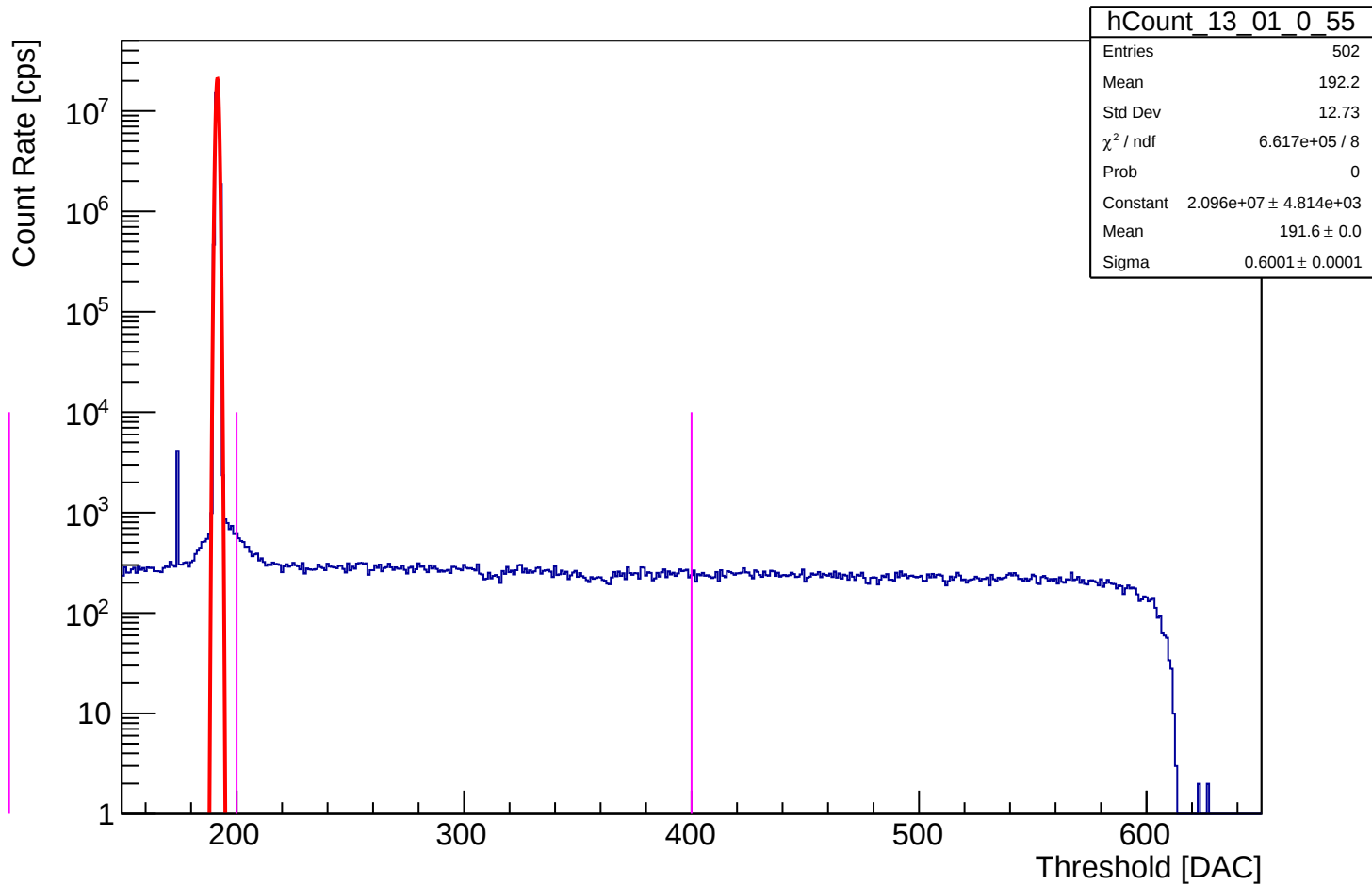
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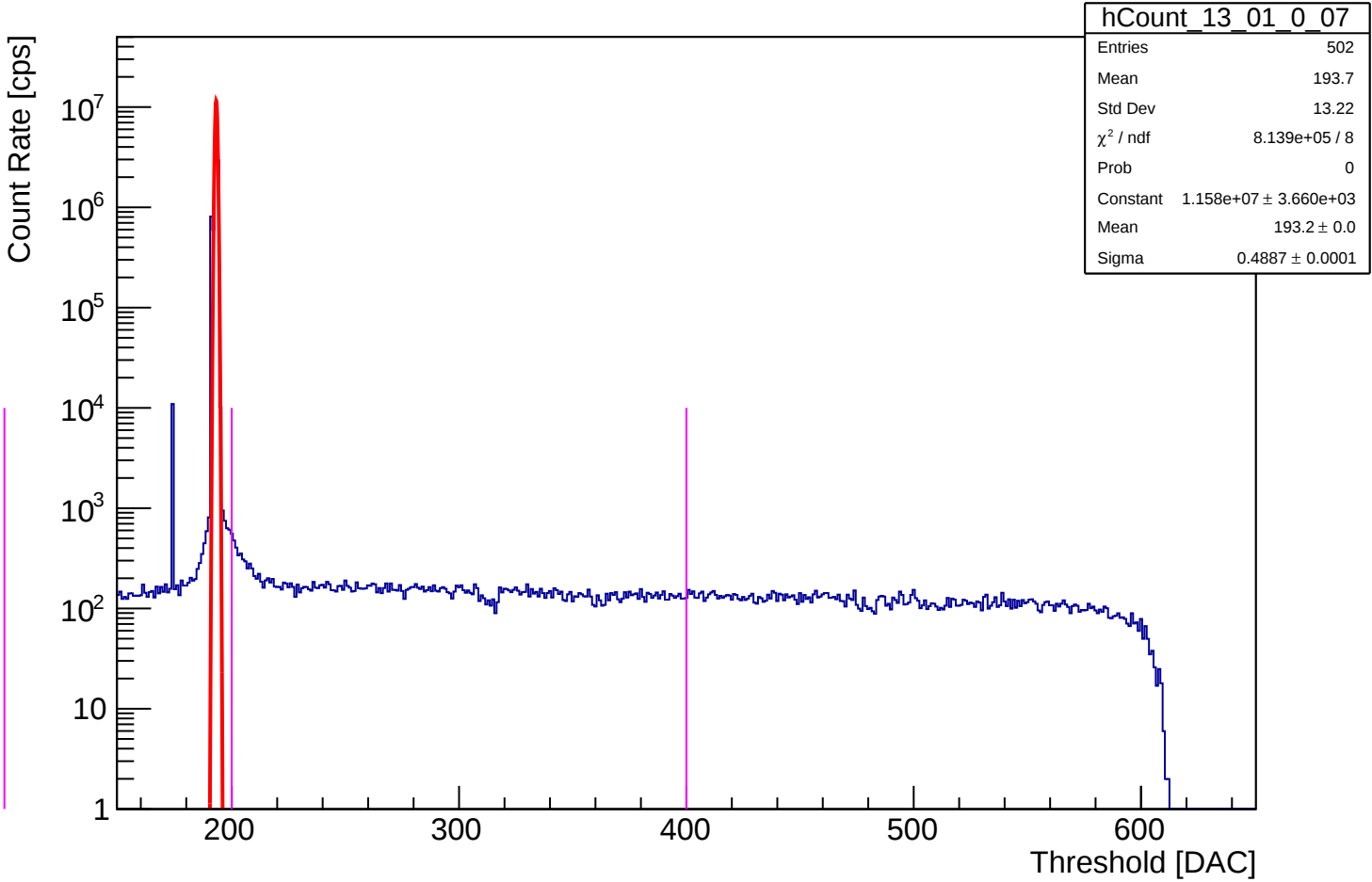


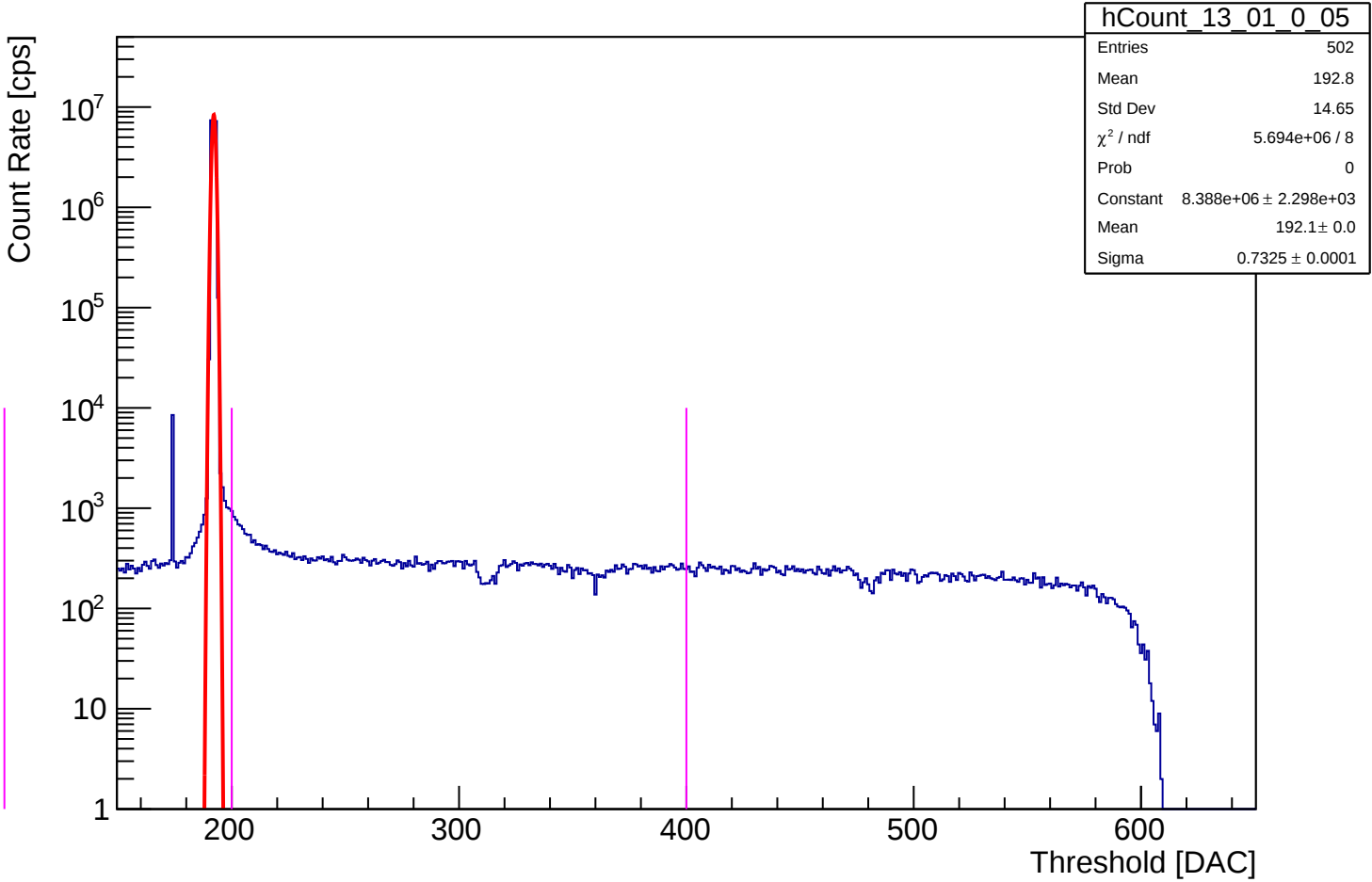
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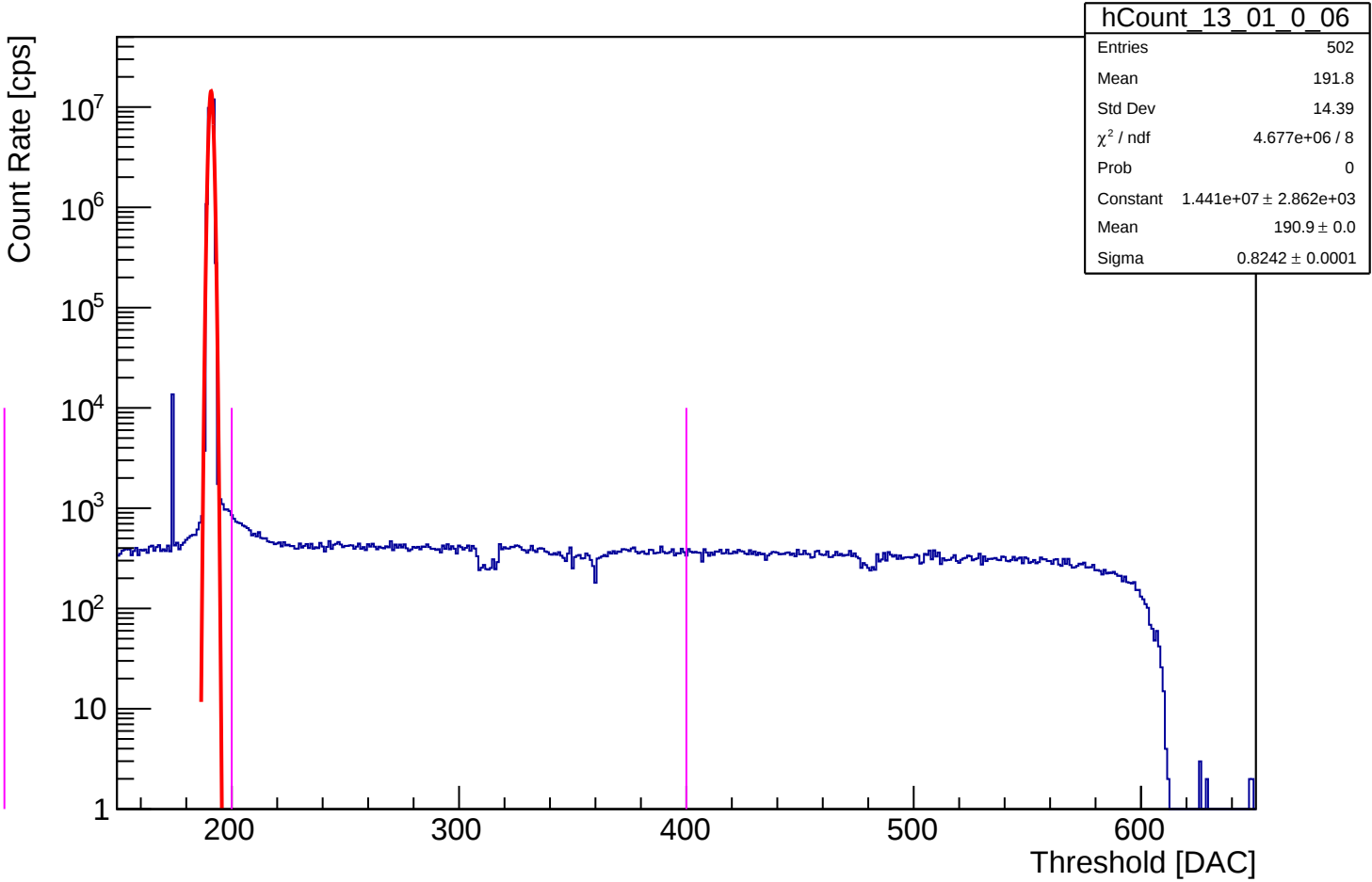


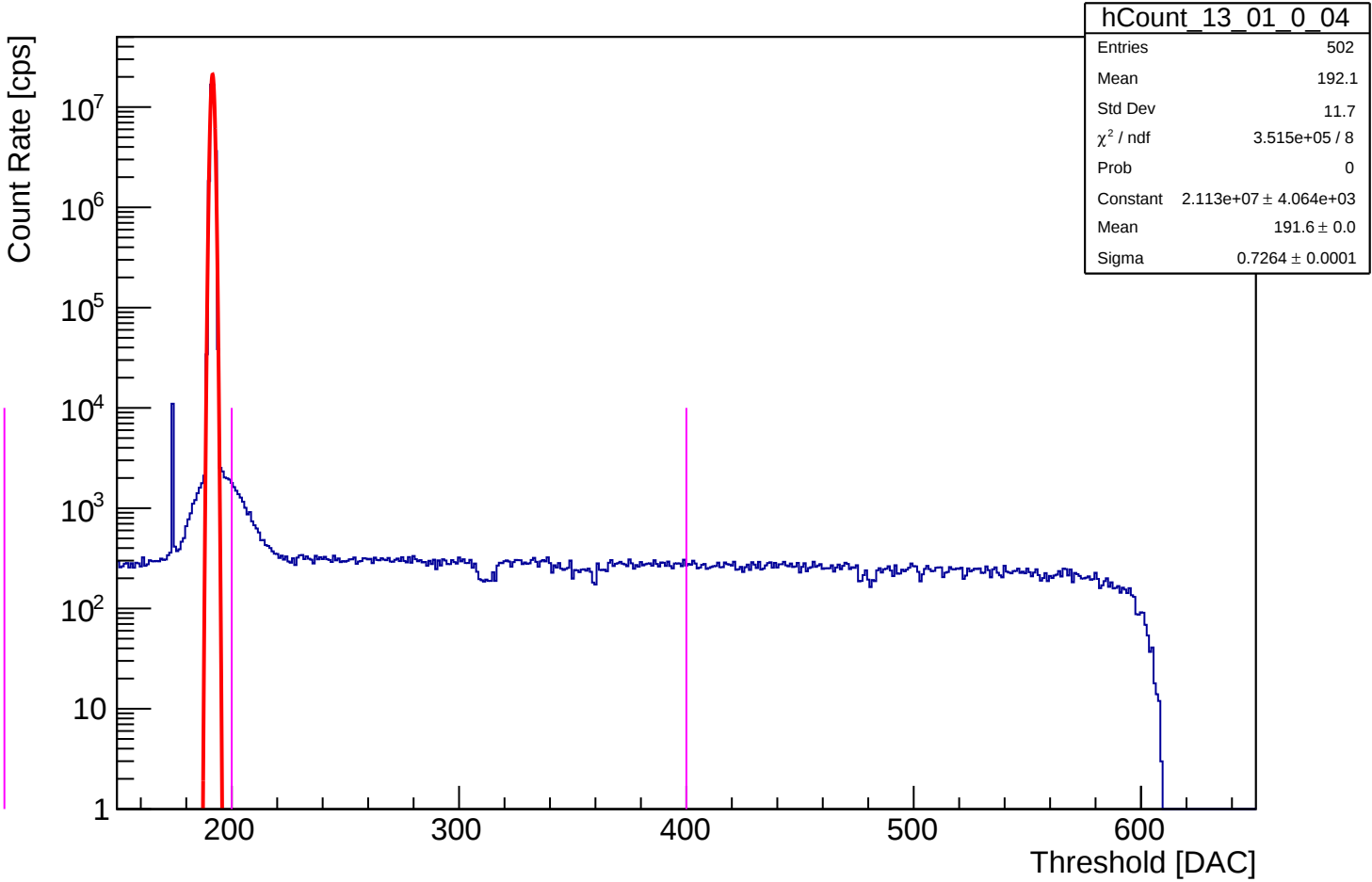
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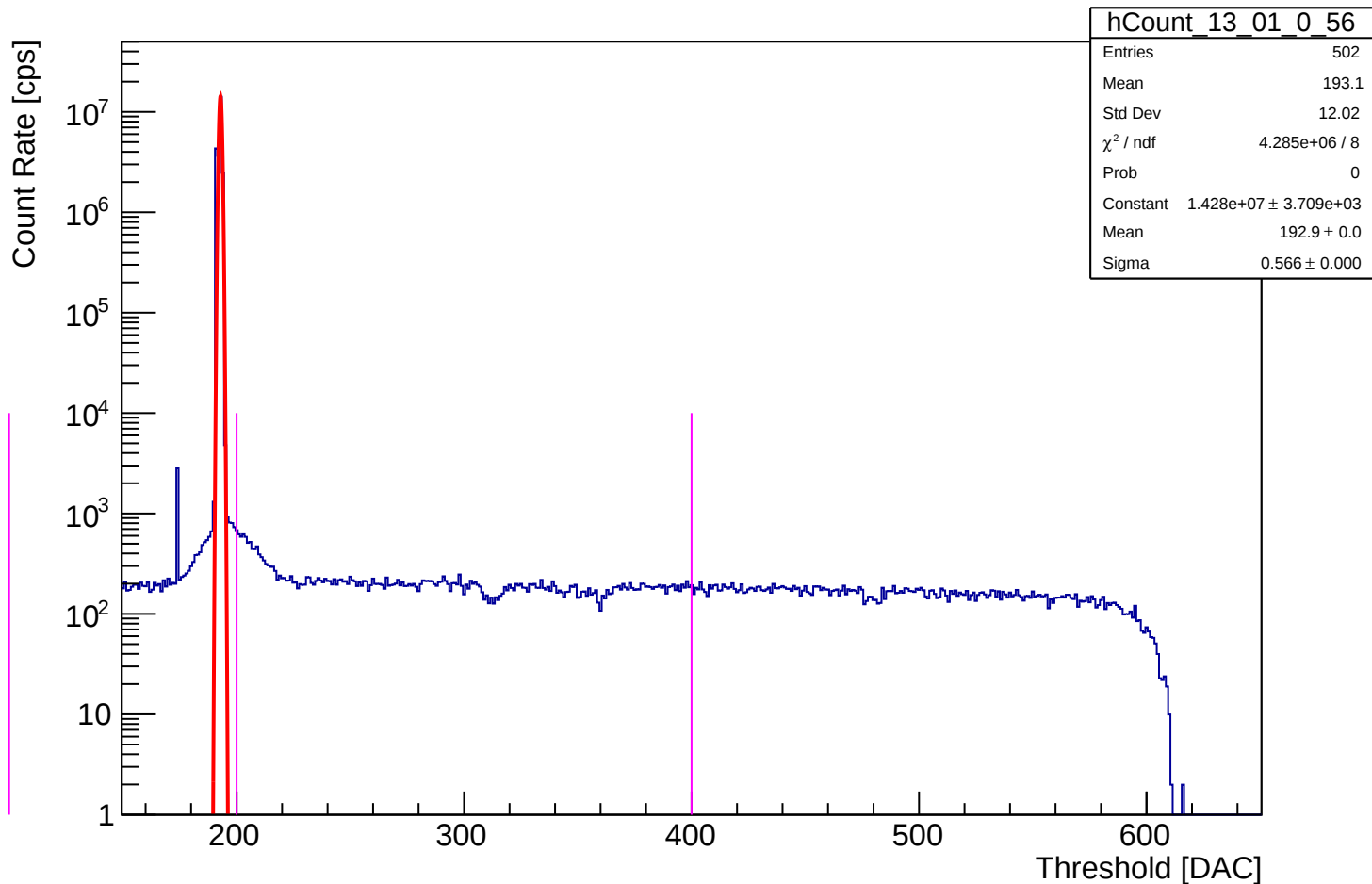




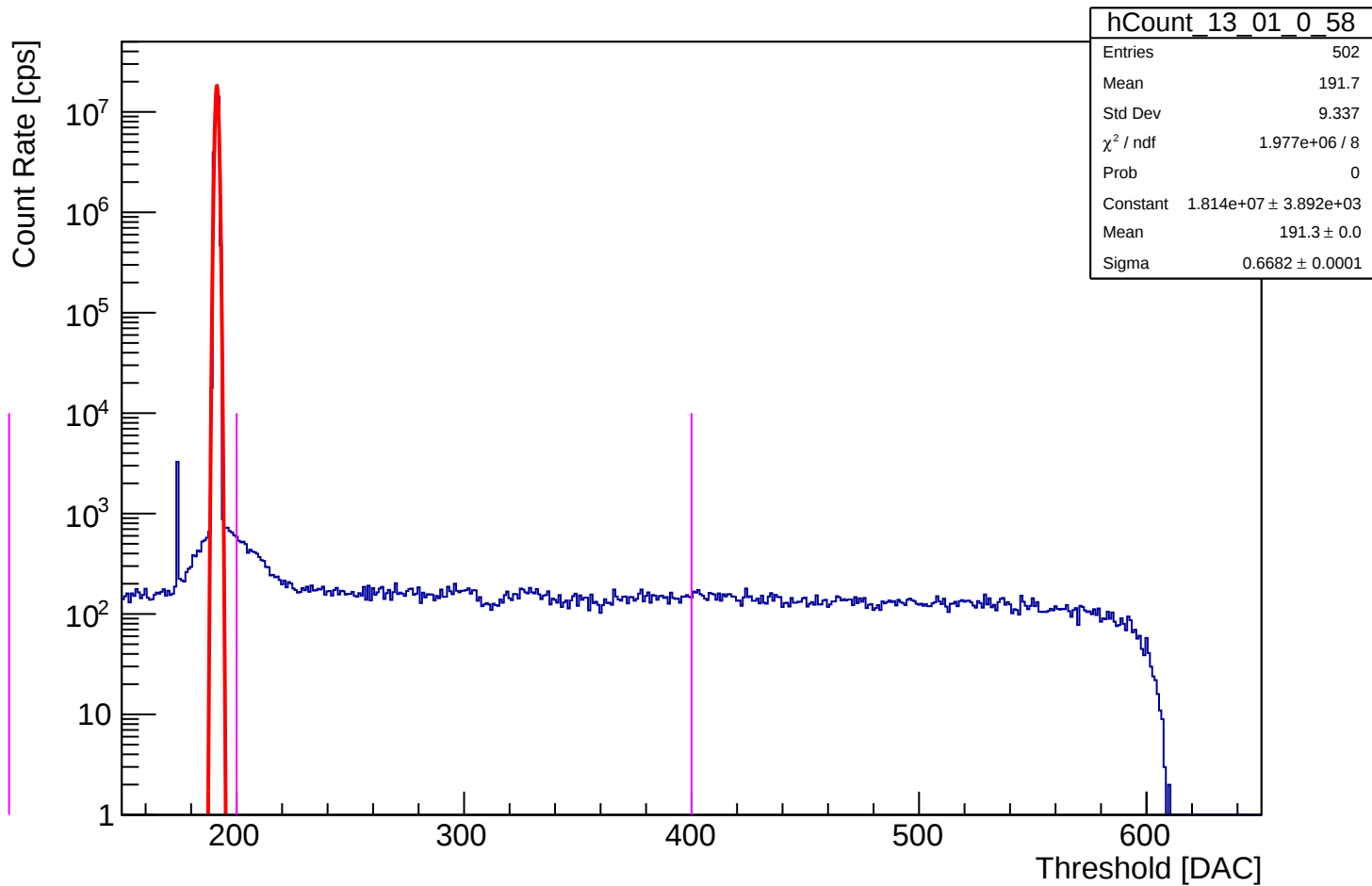




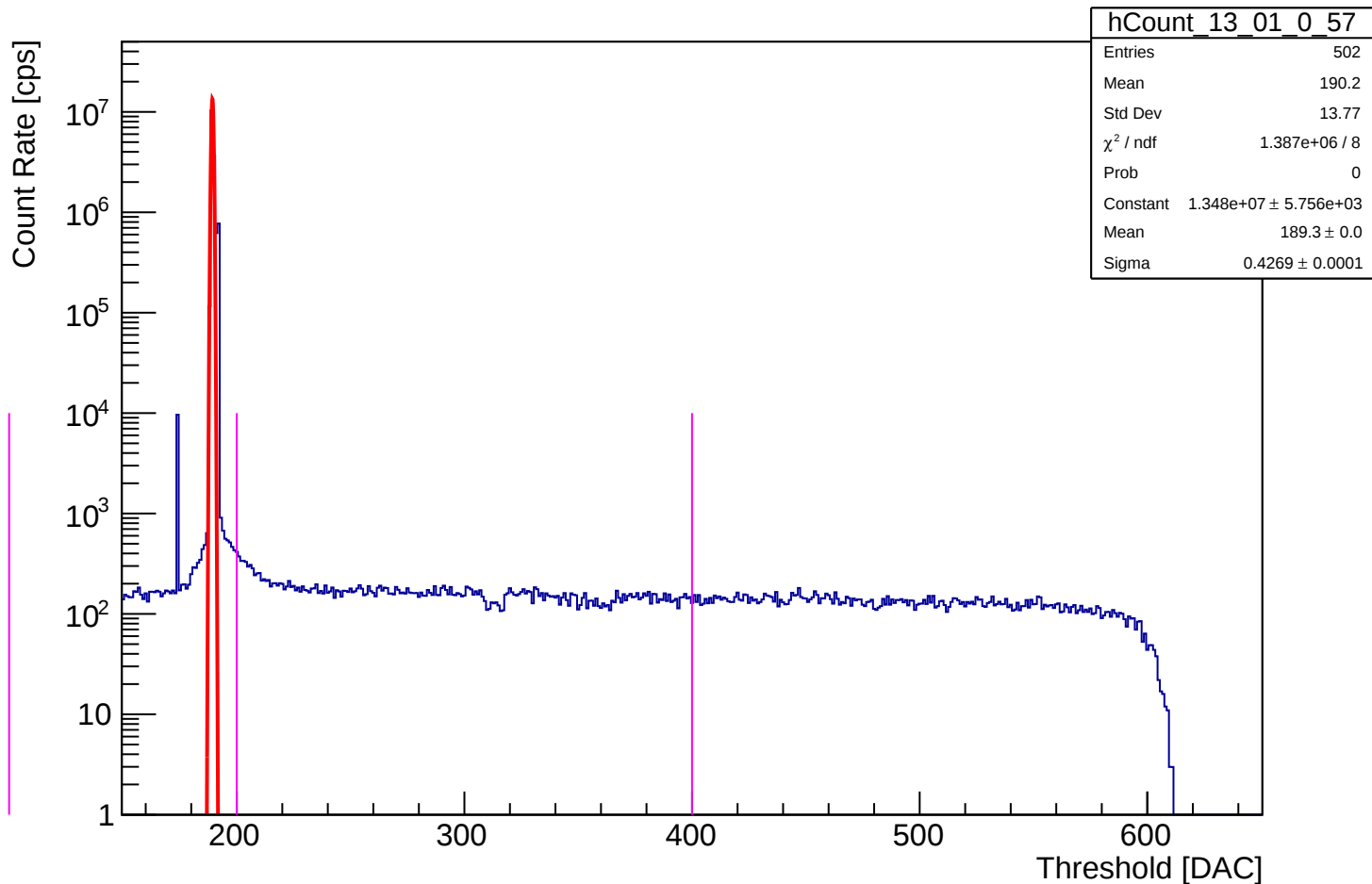
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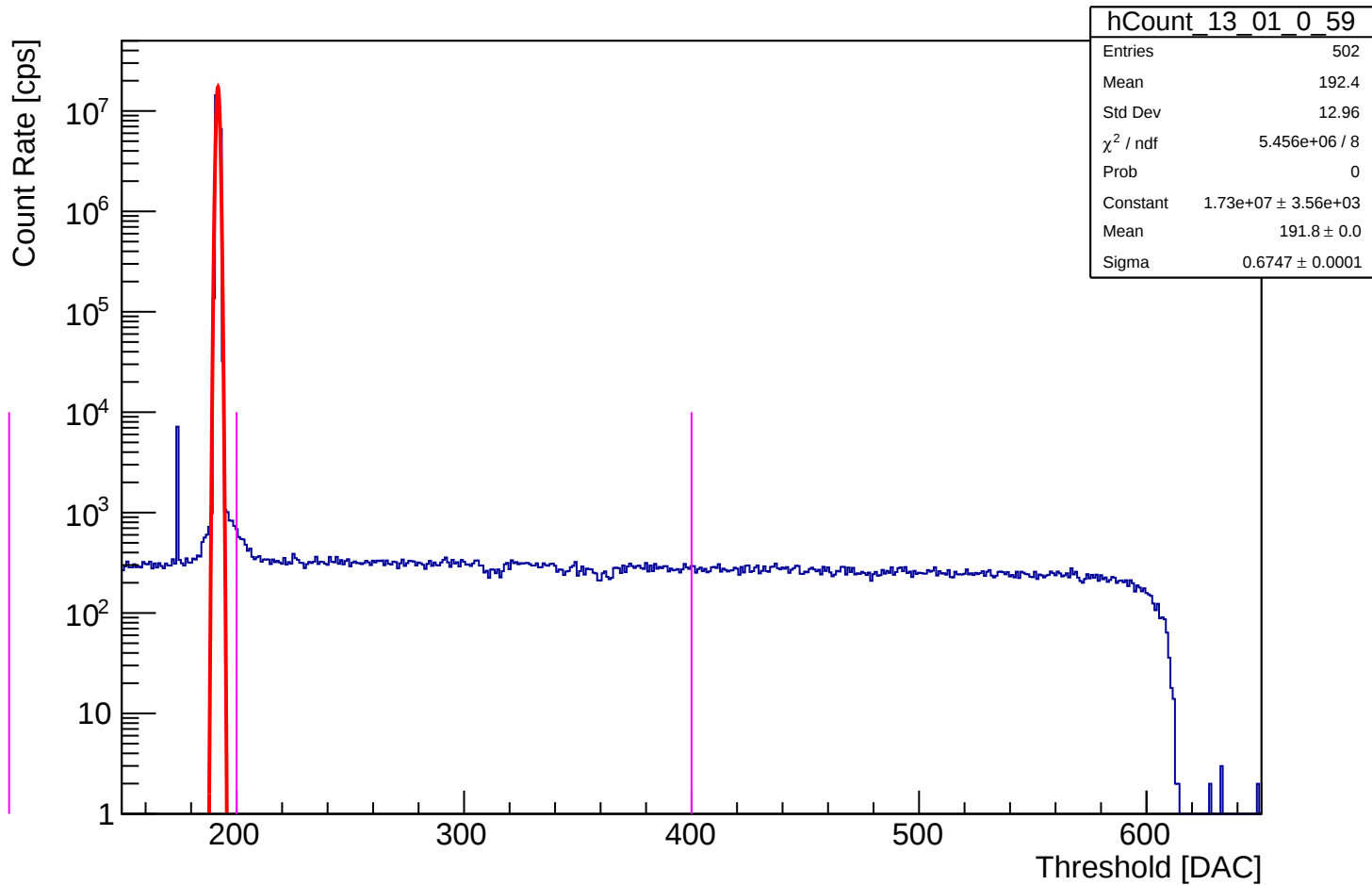
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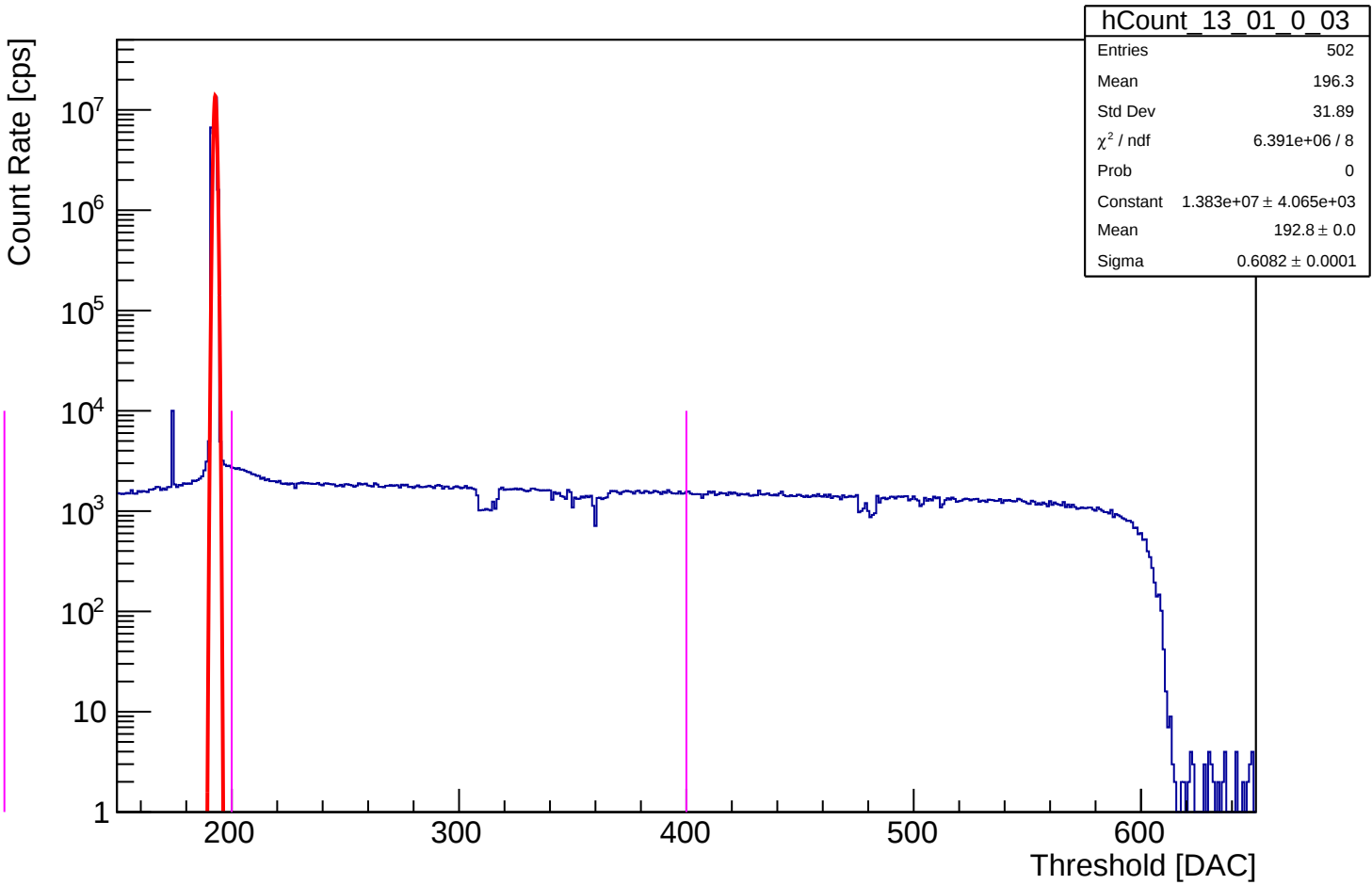


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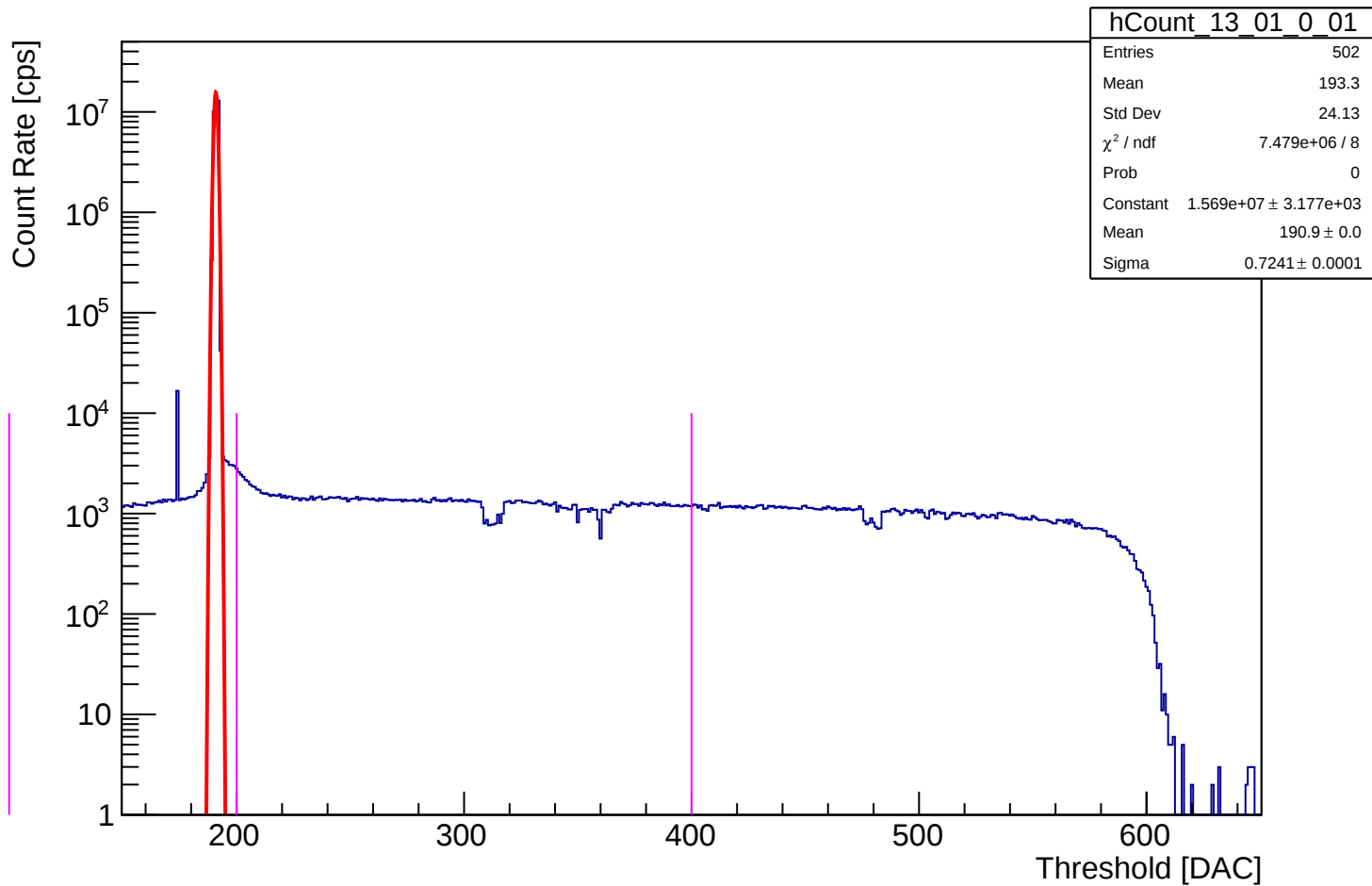


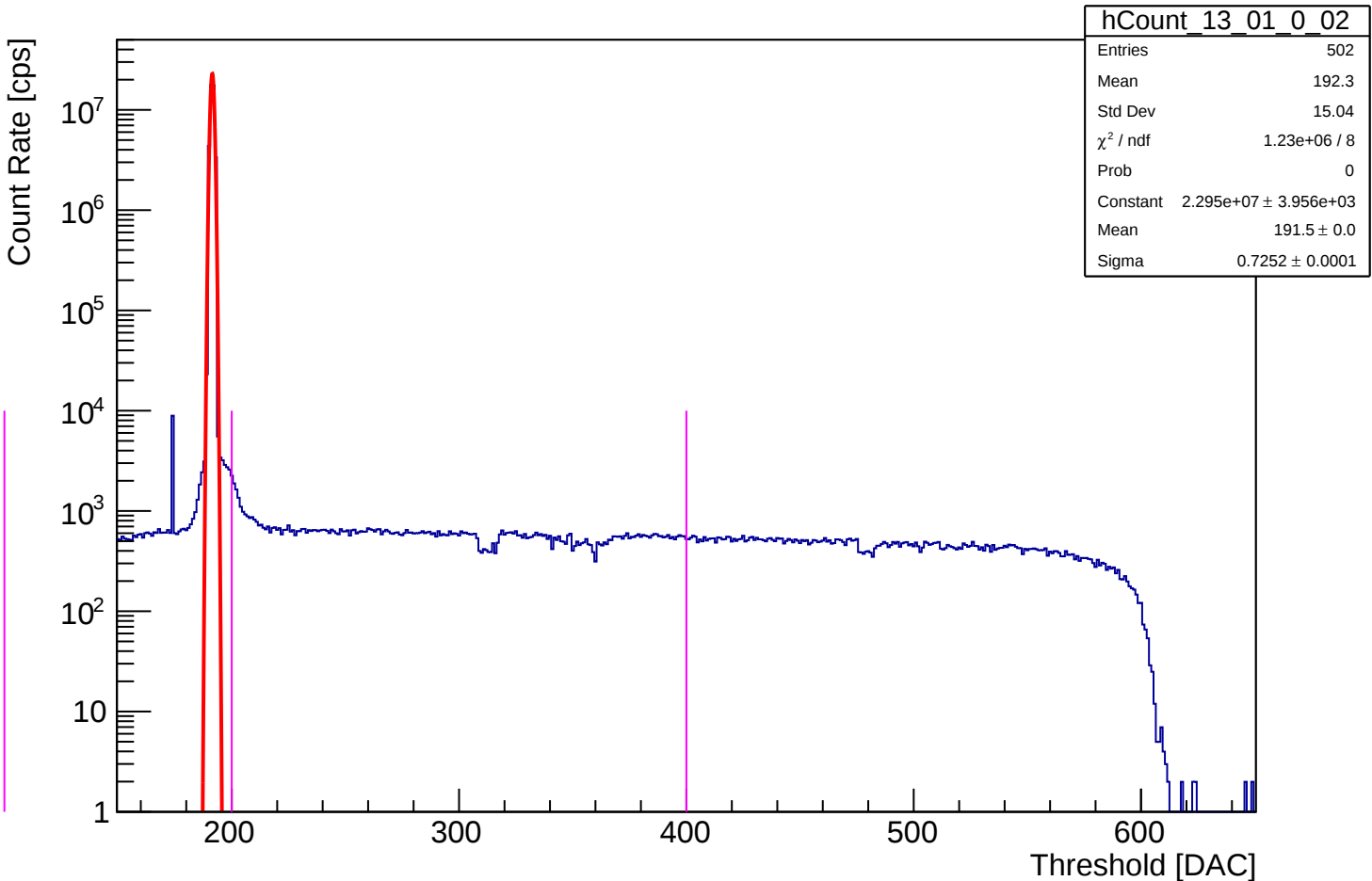
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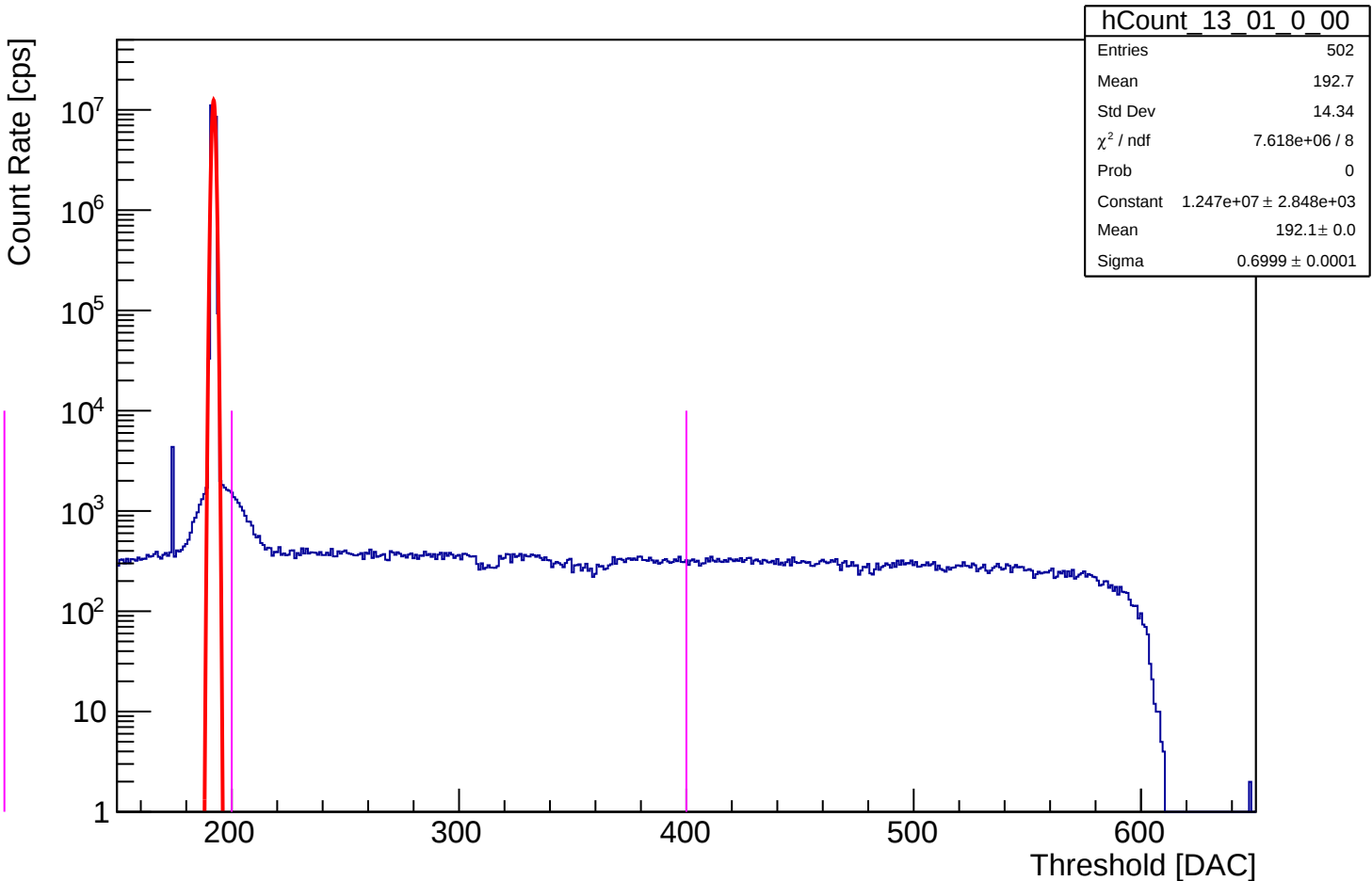




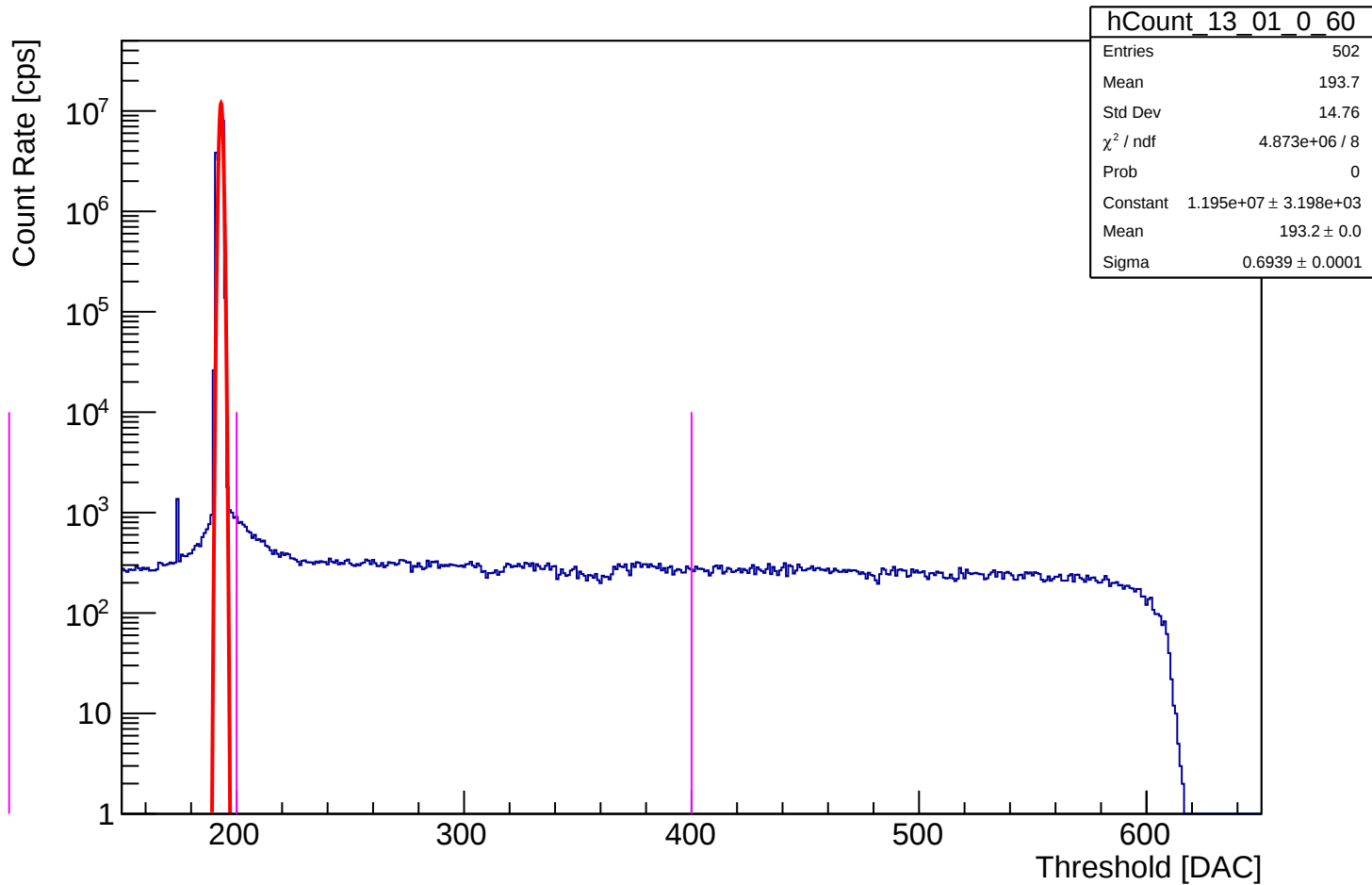
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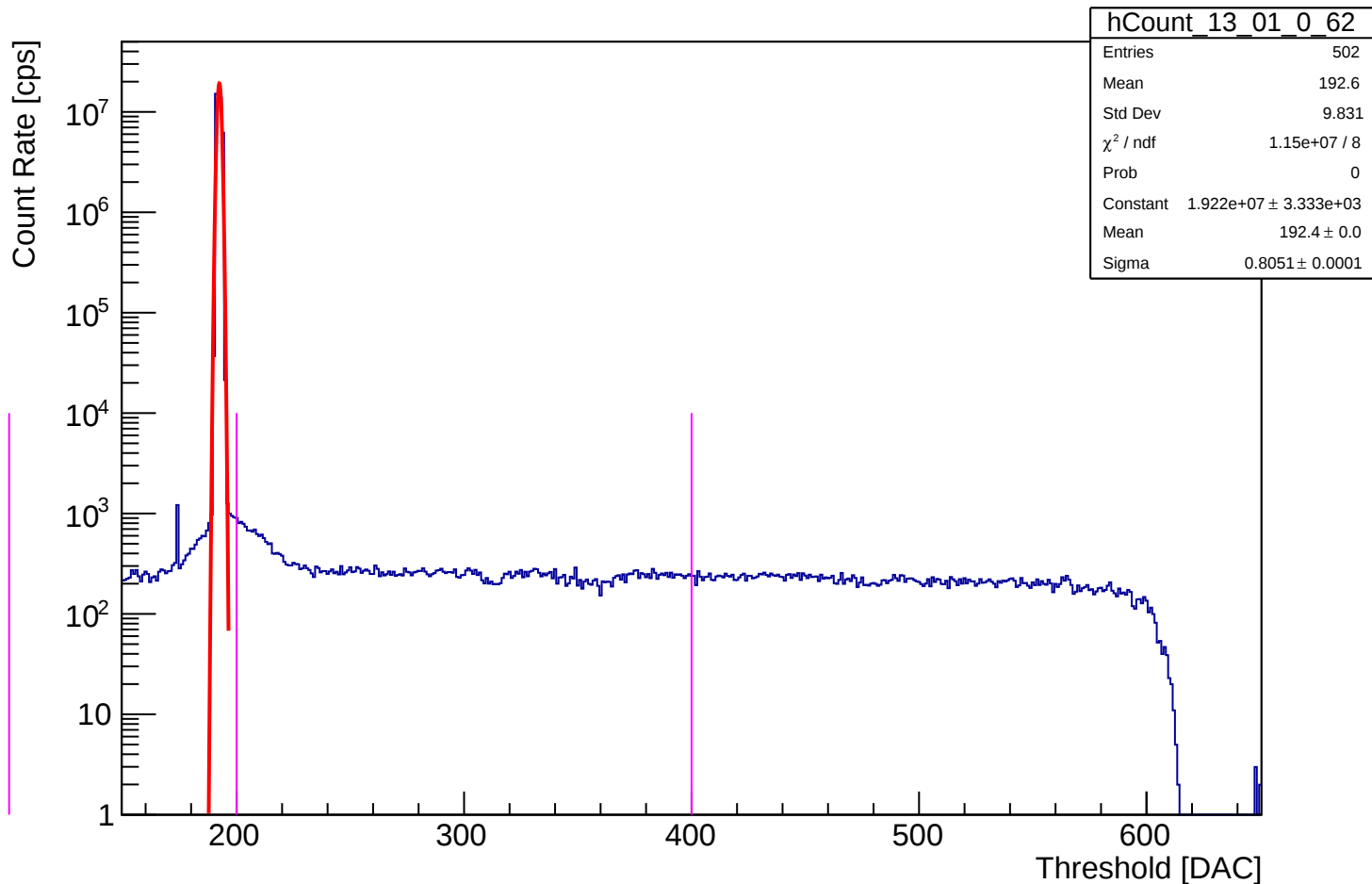




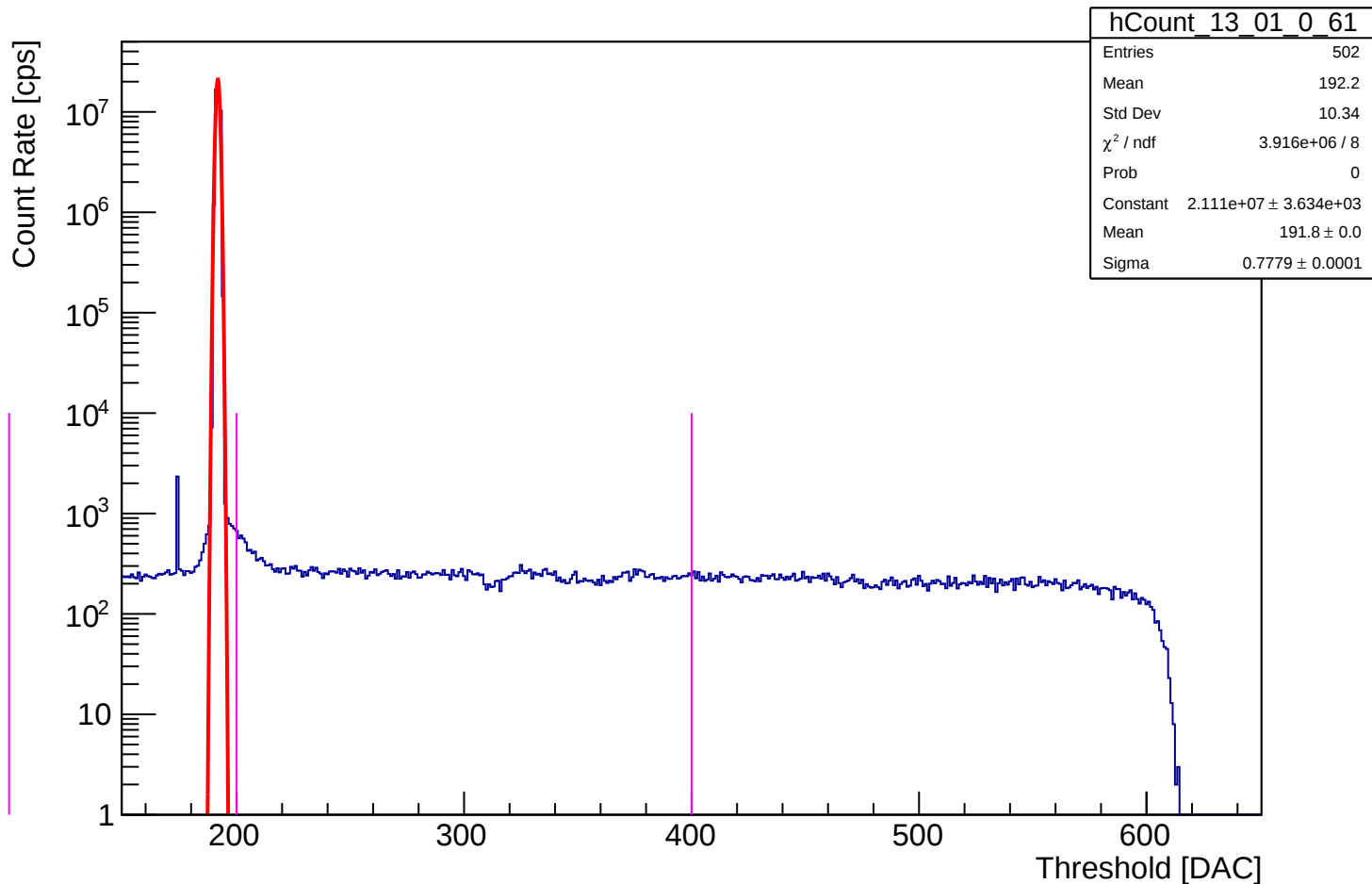
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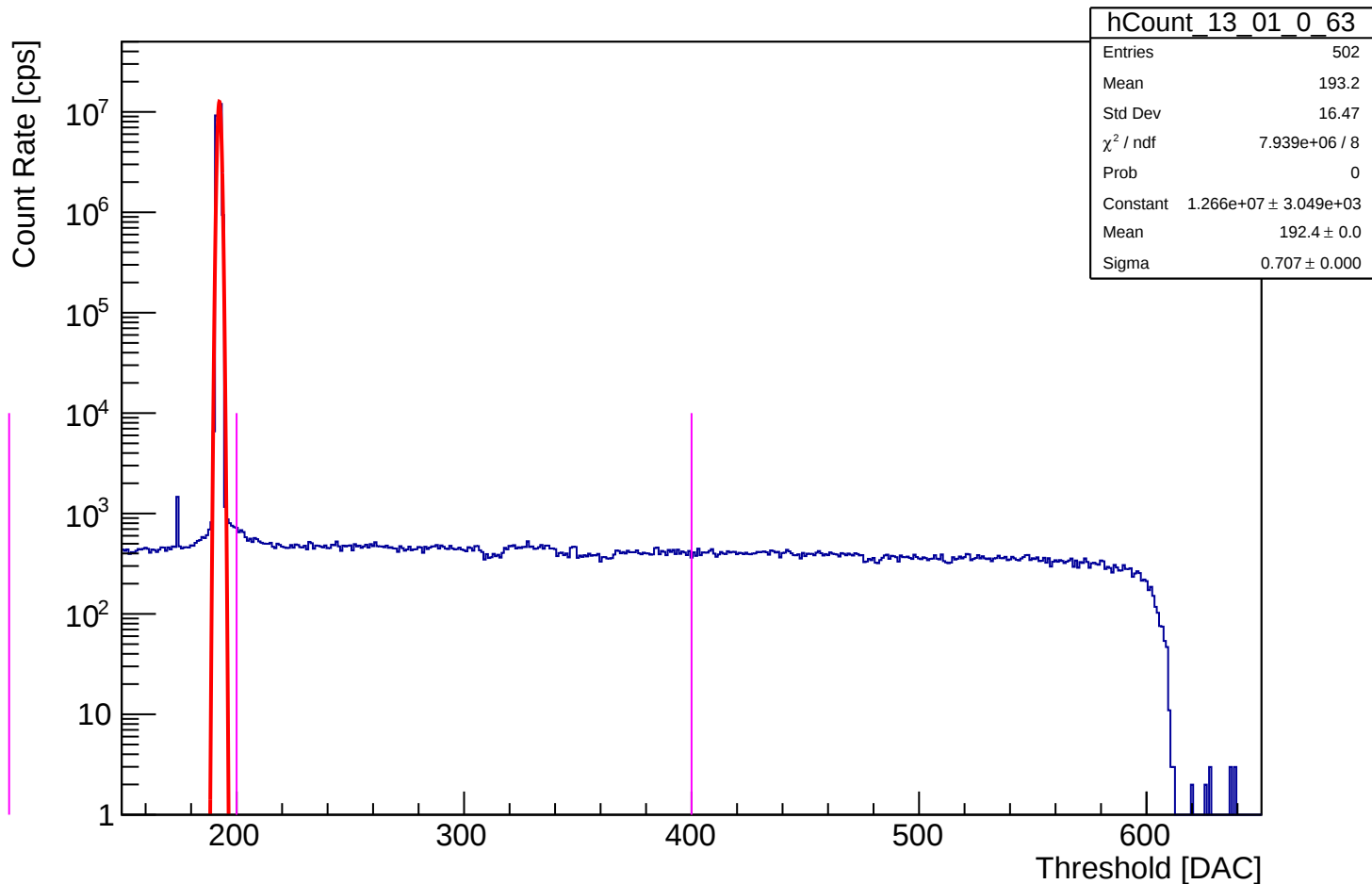
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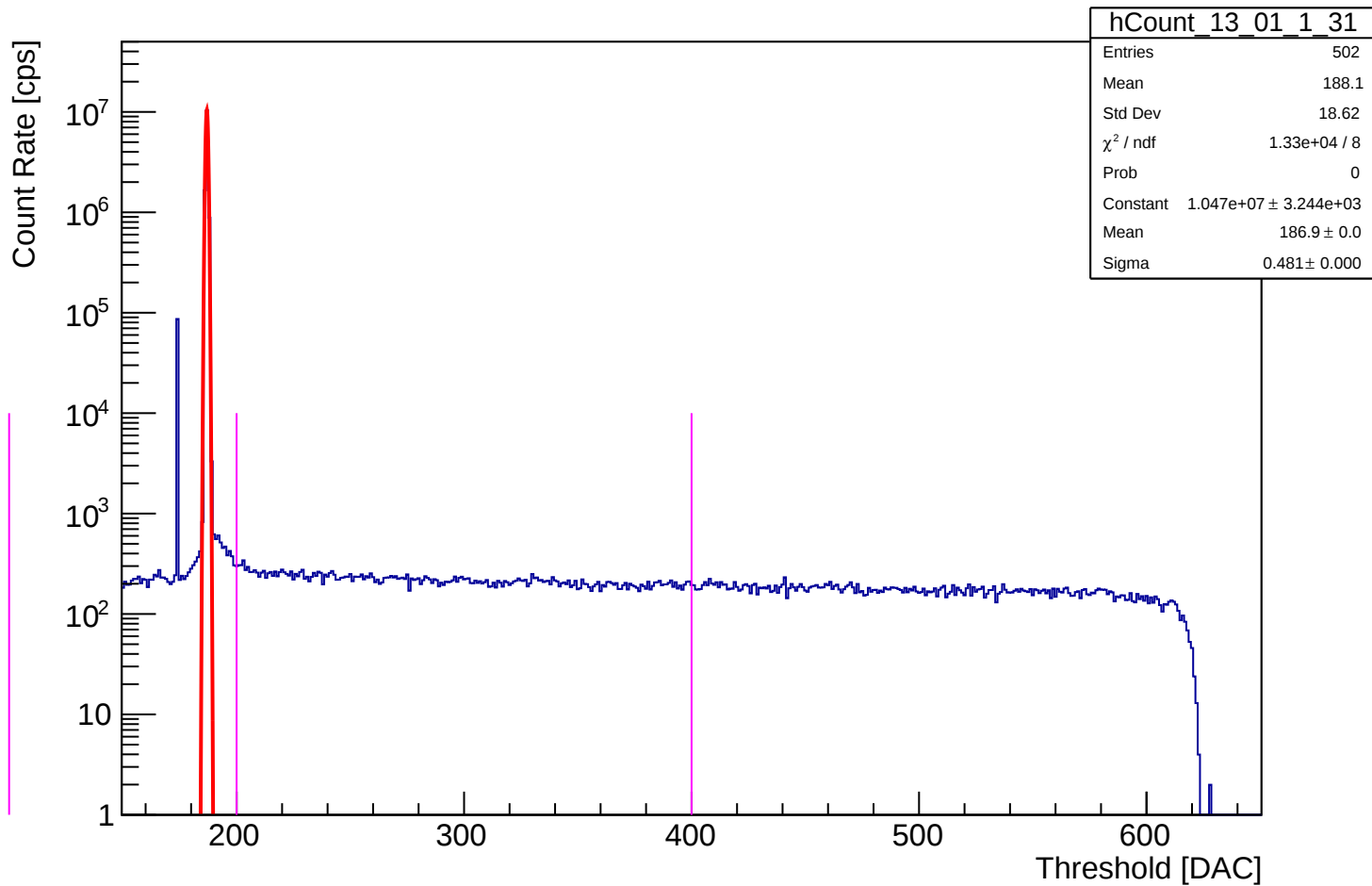
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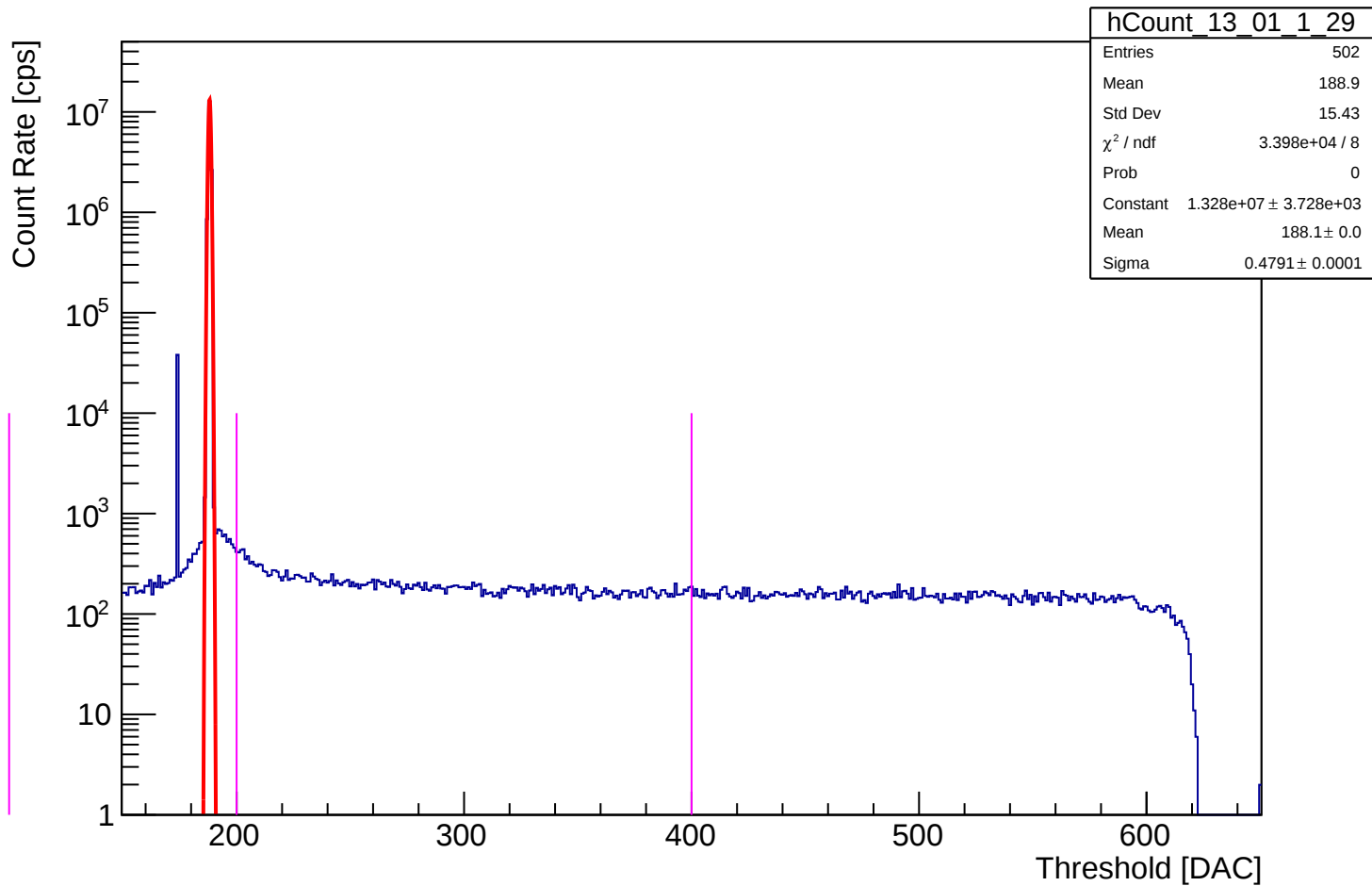
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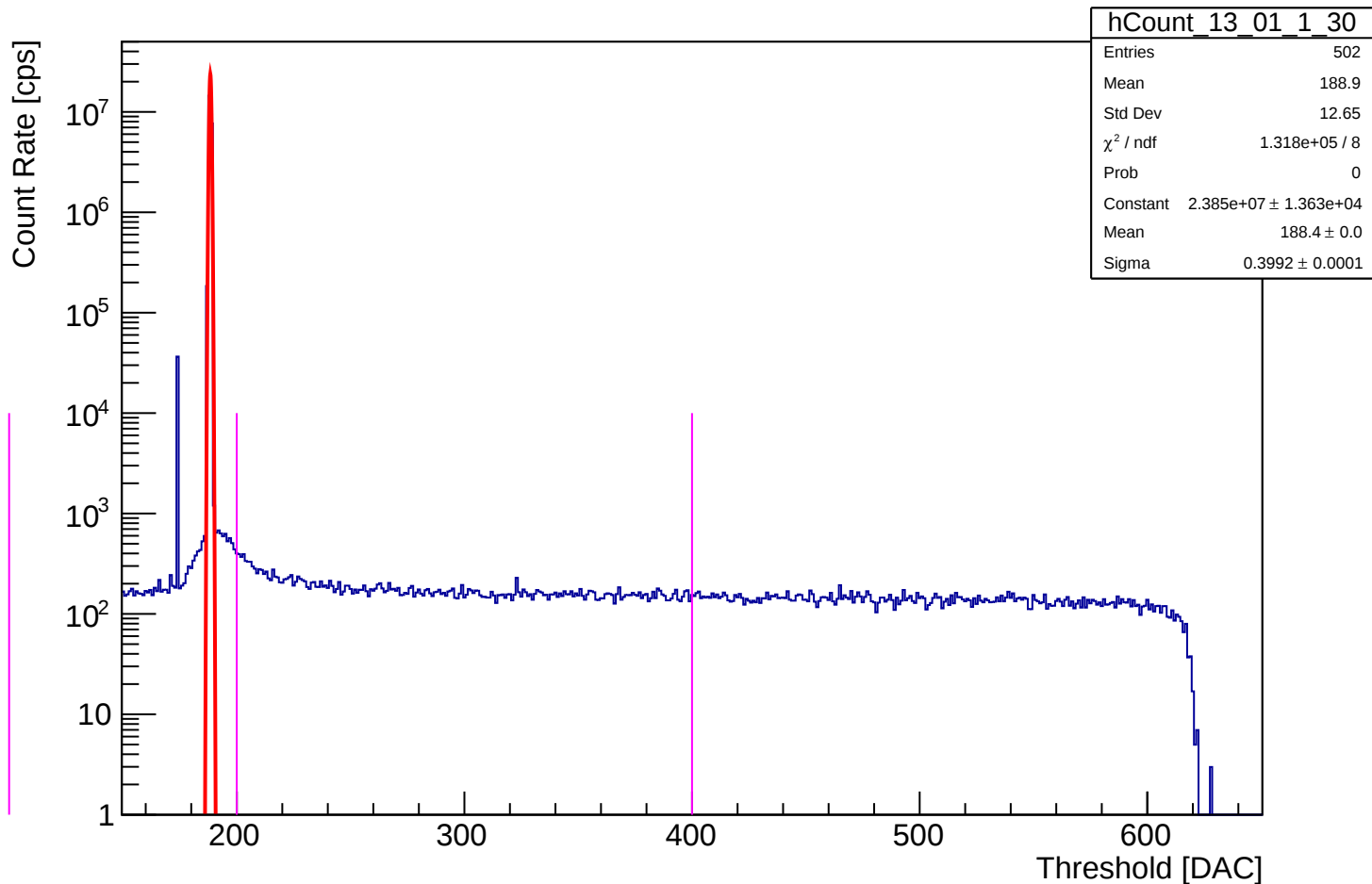
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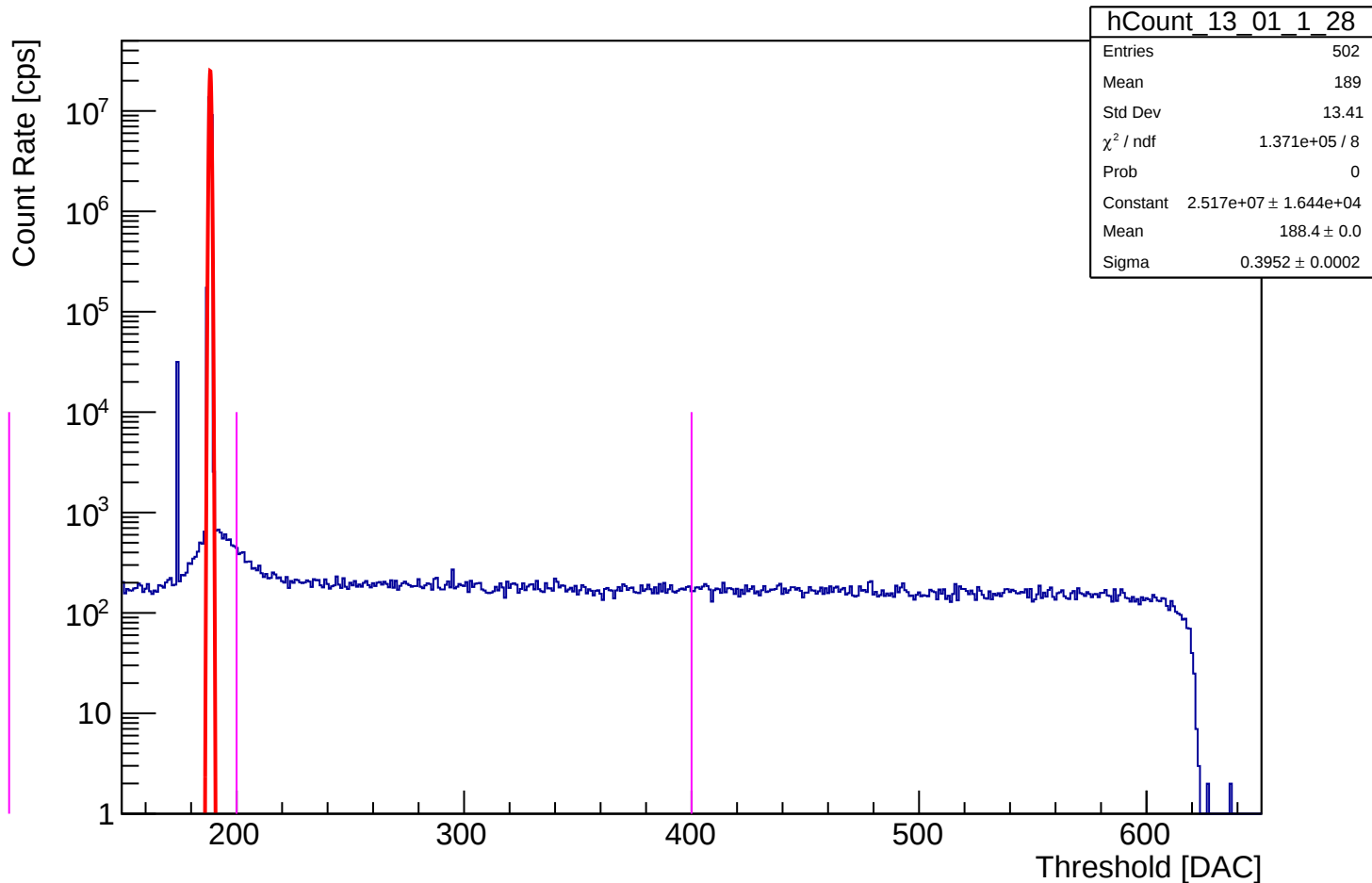
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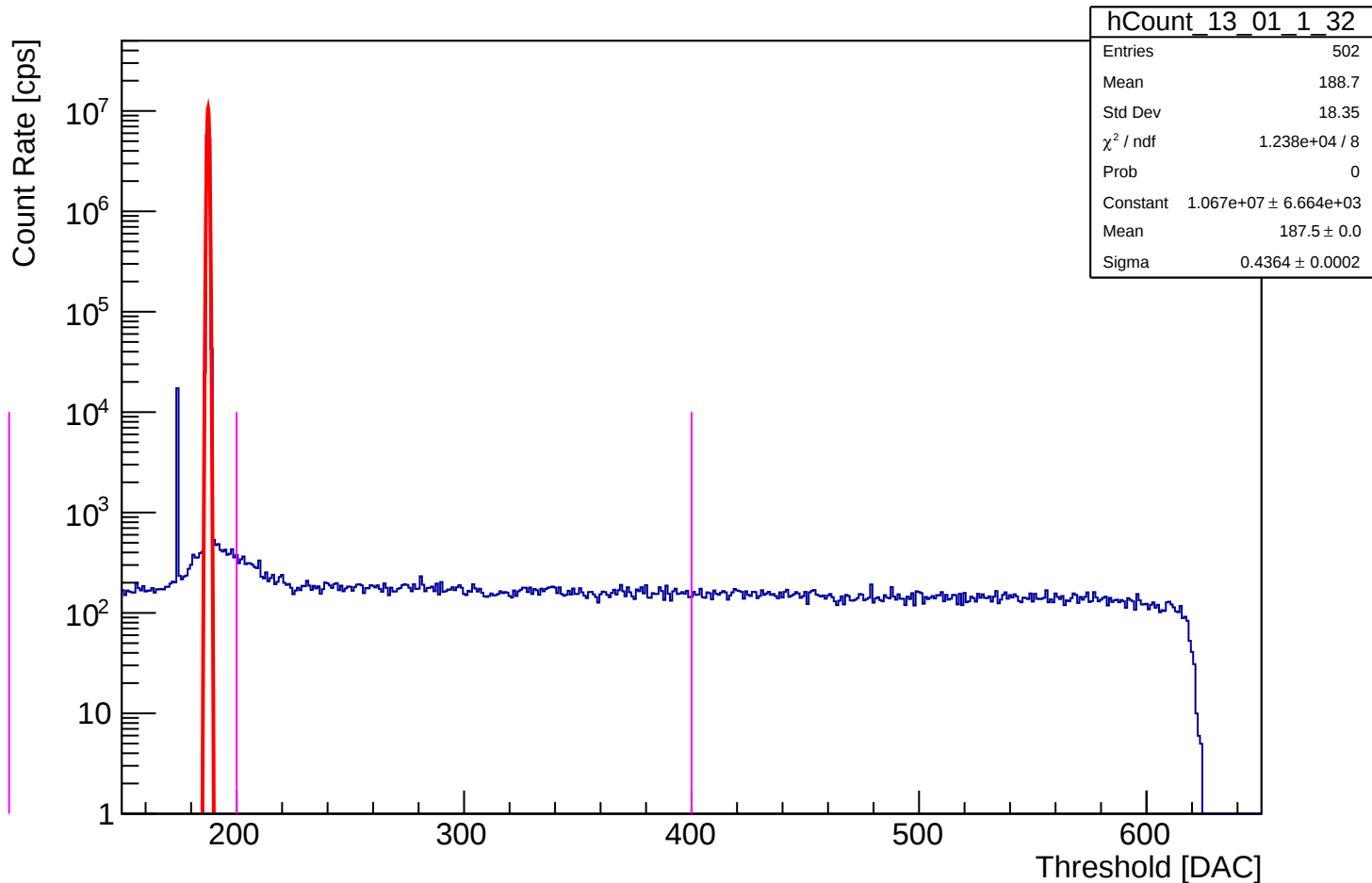
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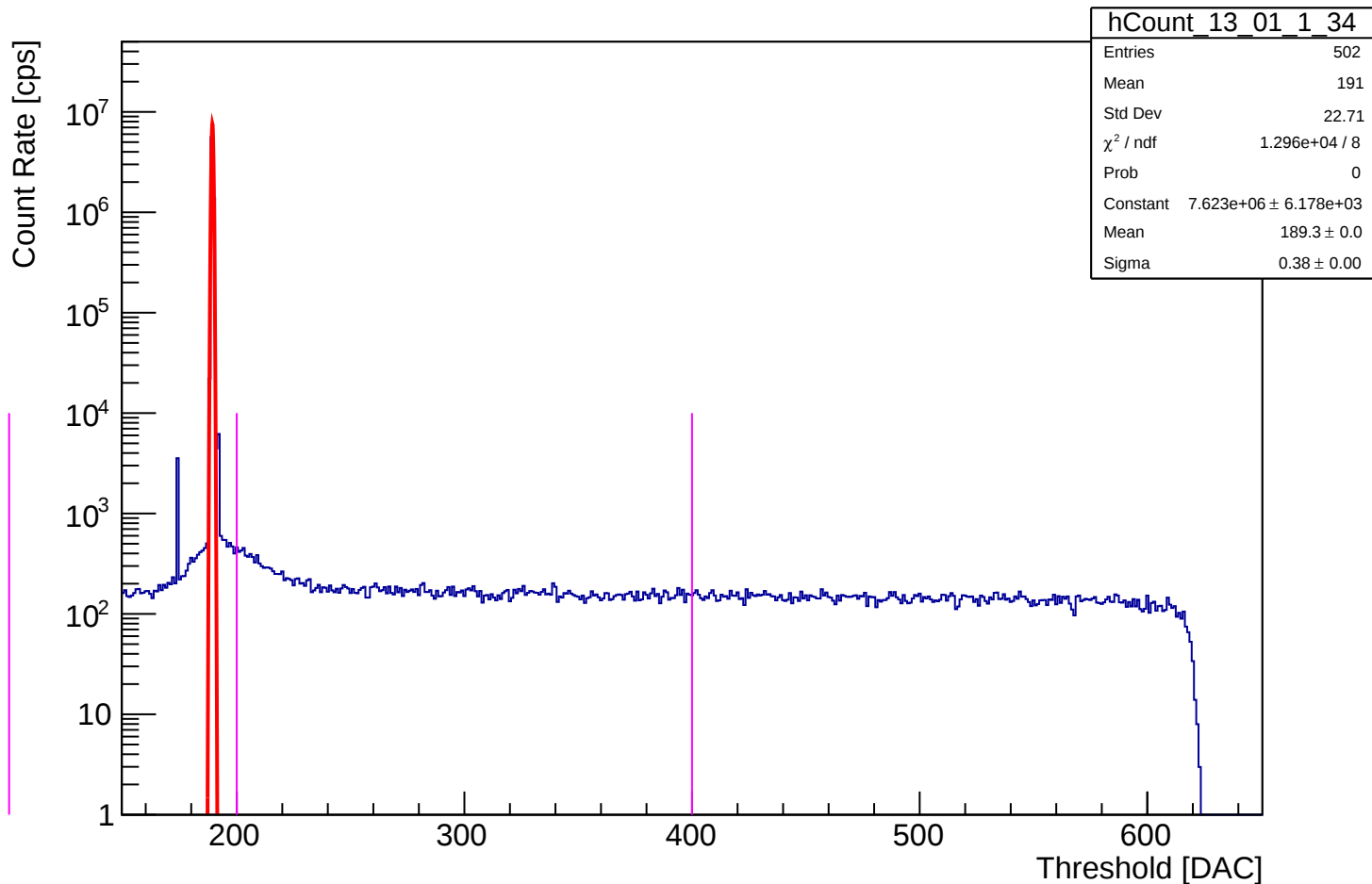


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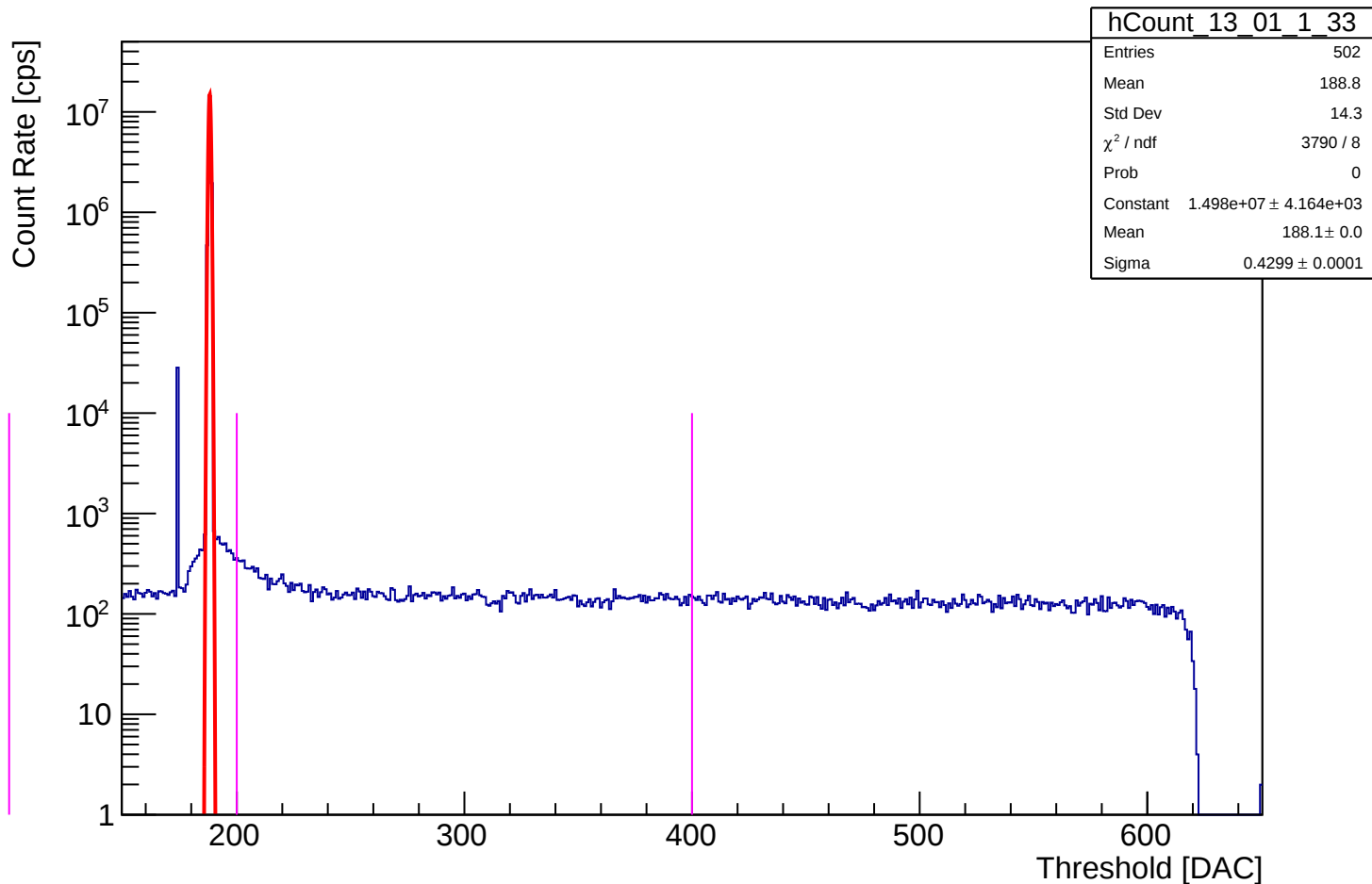


Row 1 Tile 1 Pmt 5 Pixel 5 Slot 13 Fiber 1 Asic 1 Channel 32

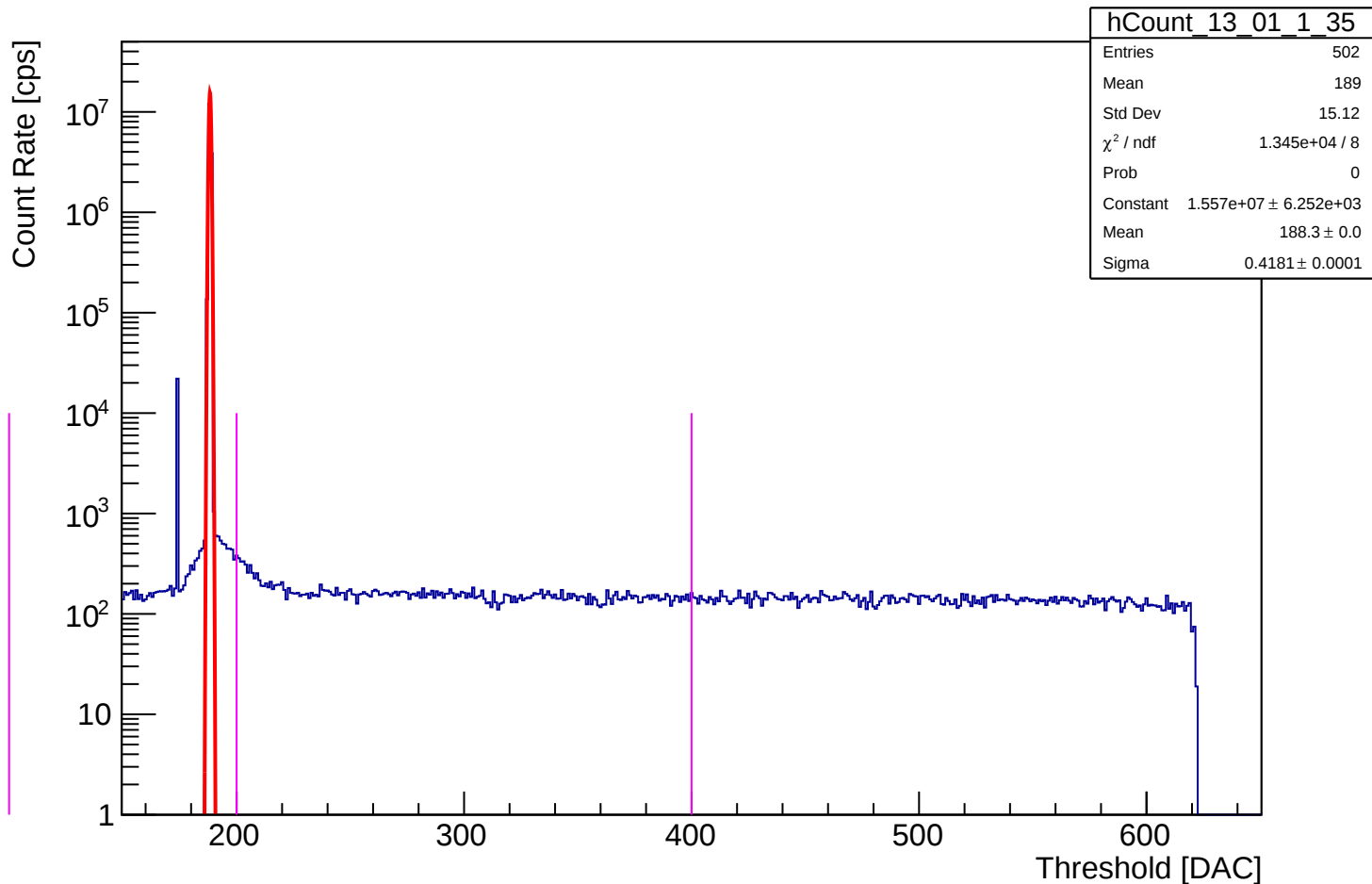




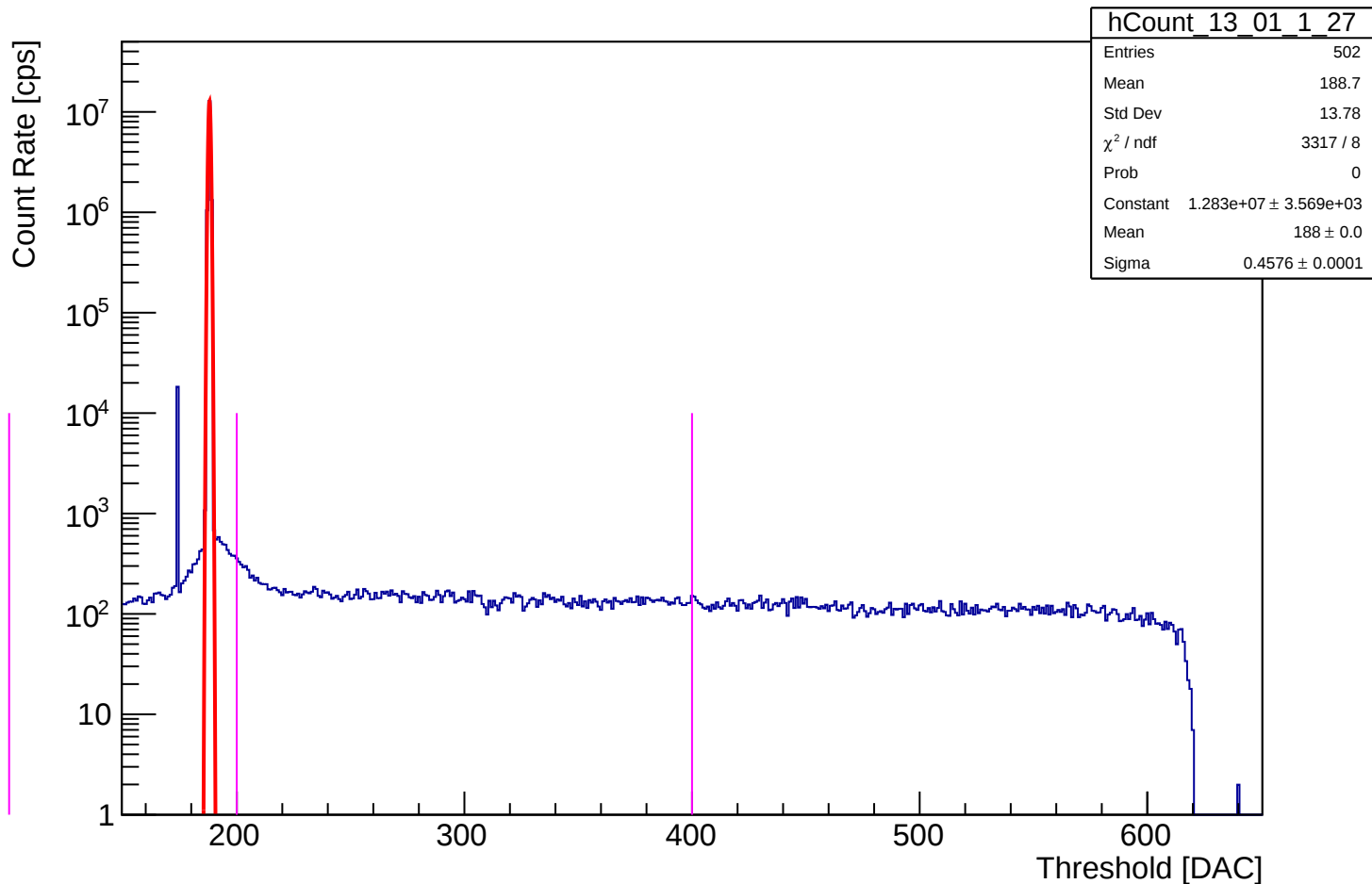
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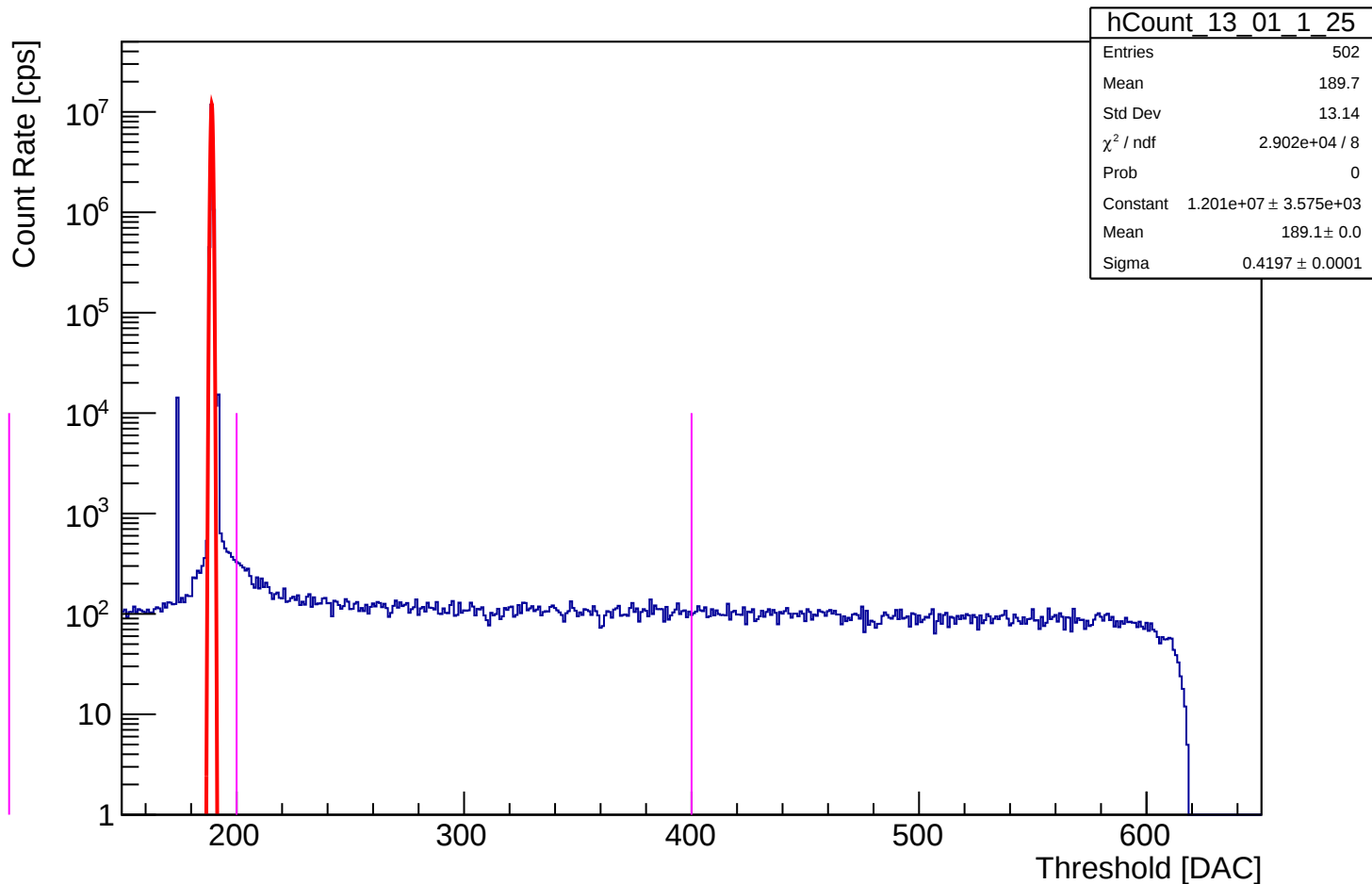
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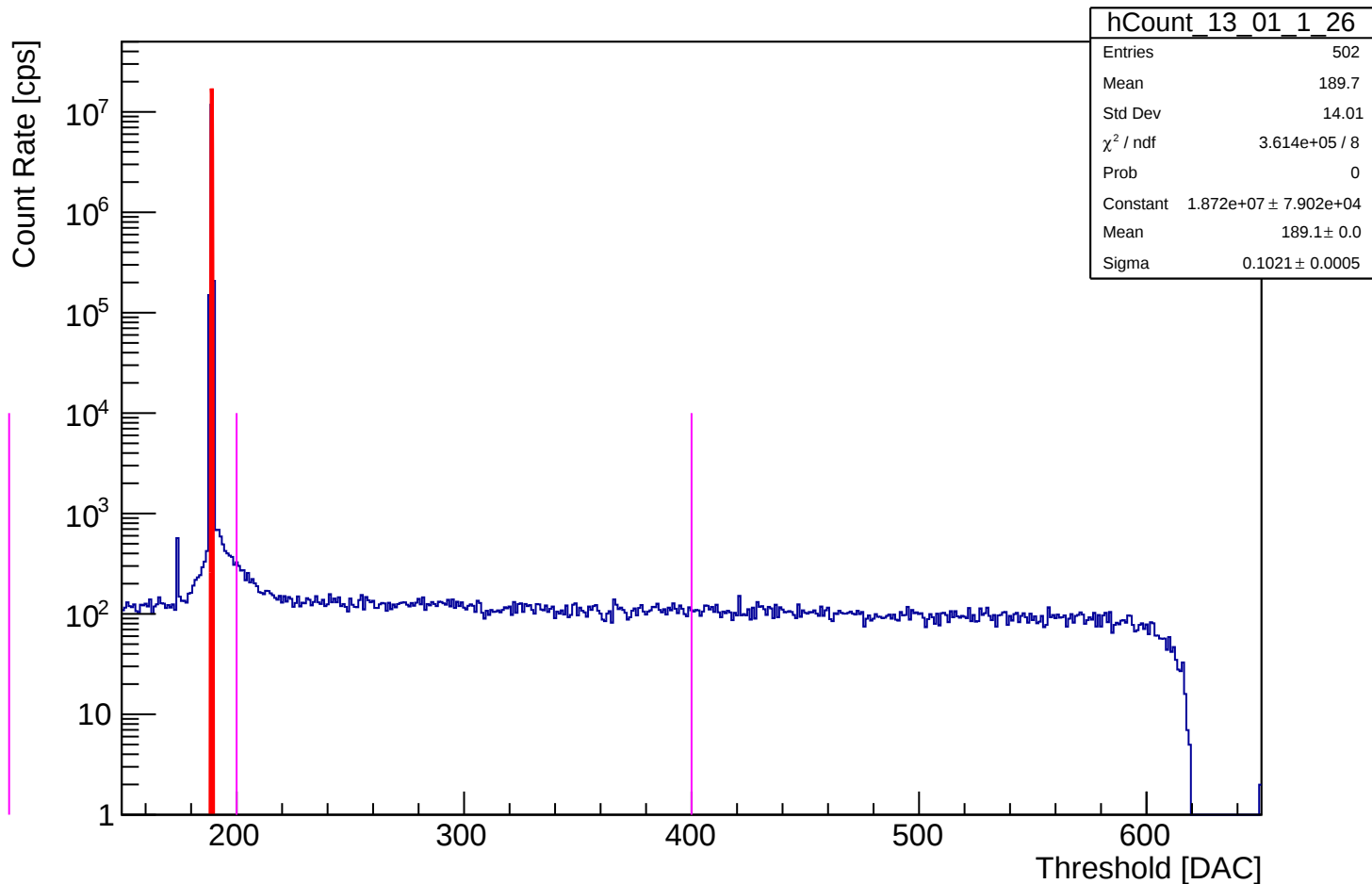
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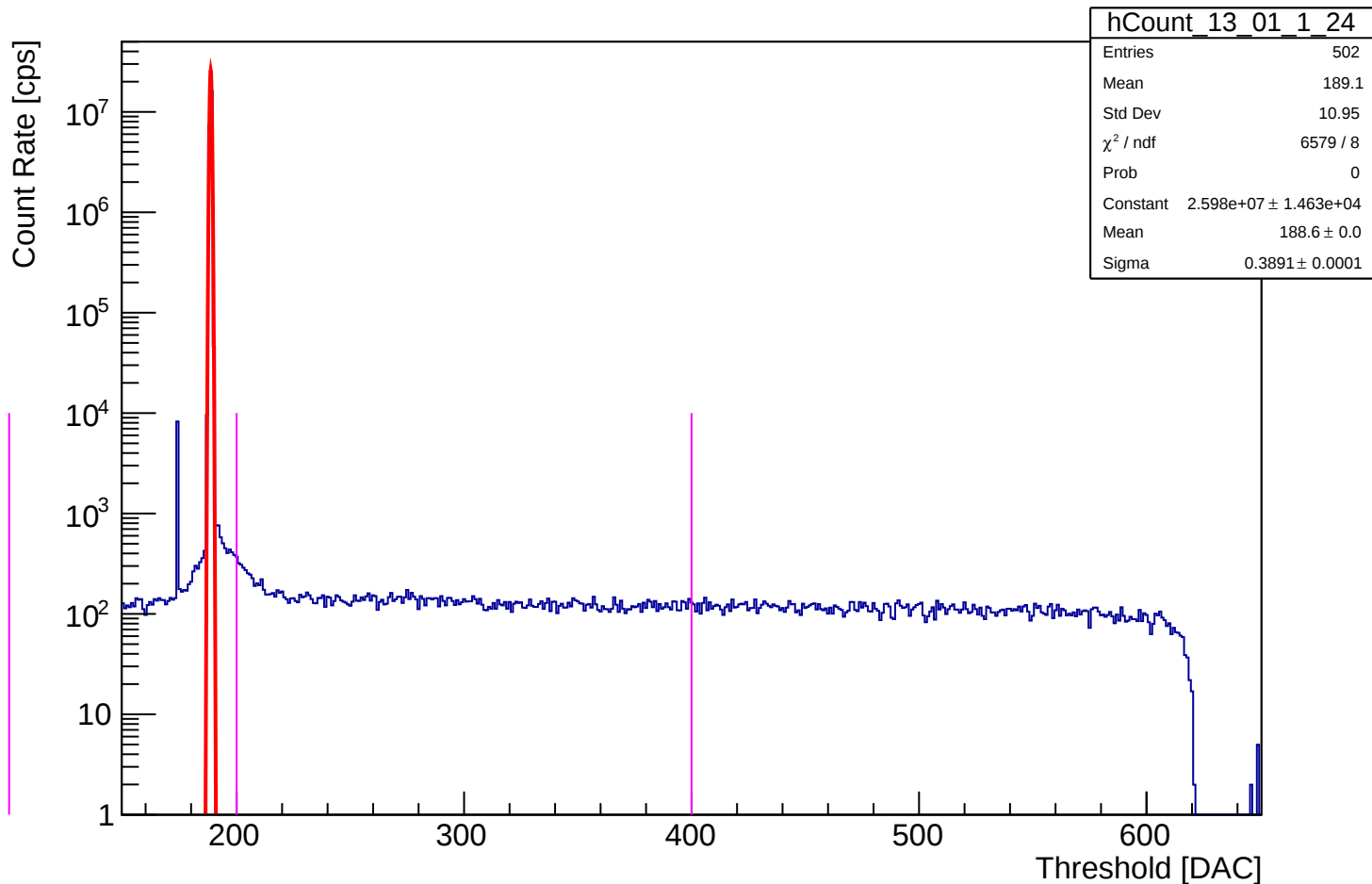
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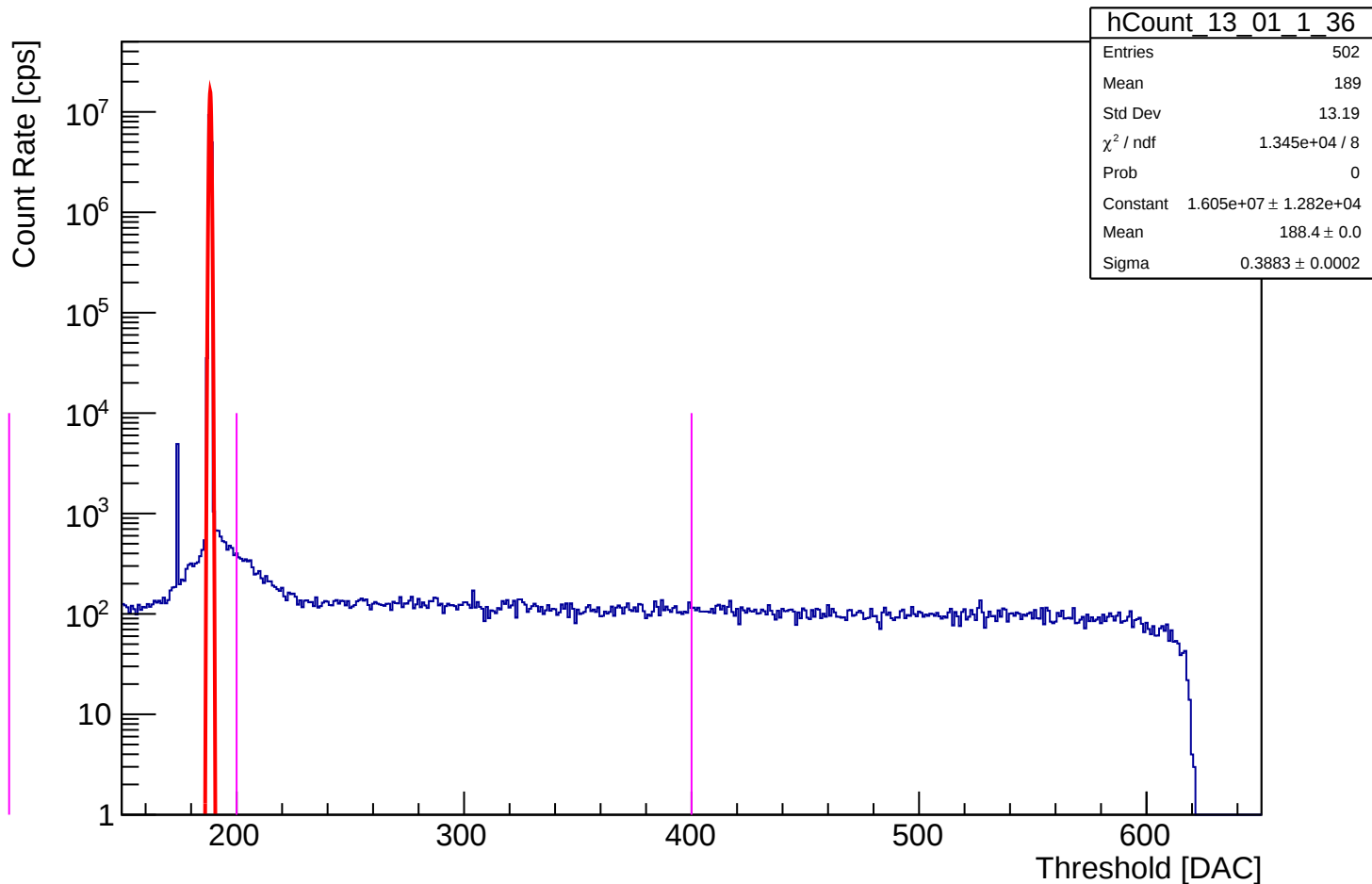
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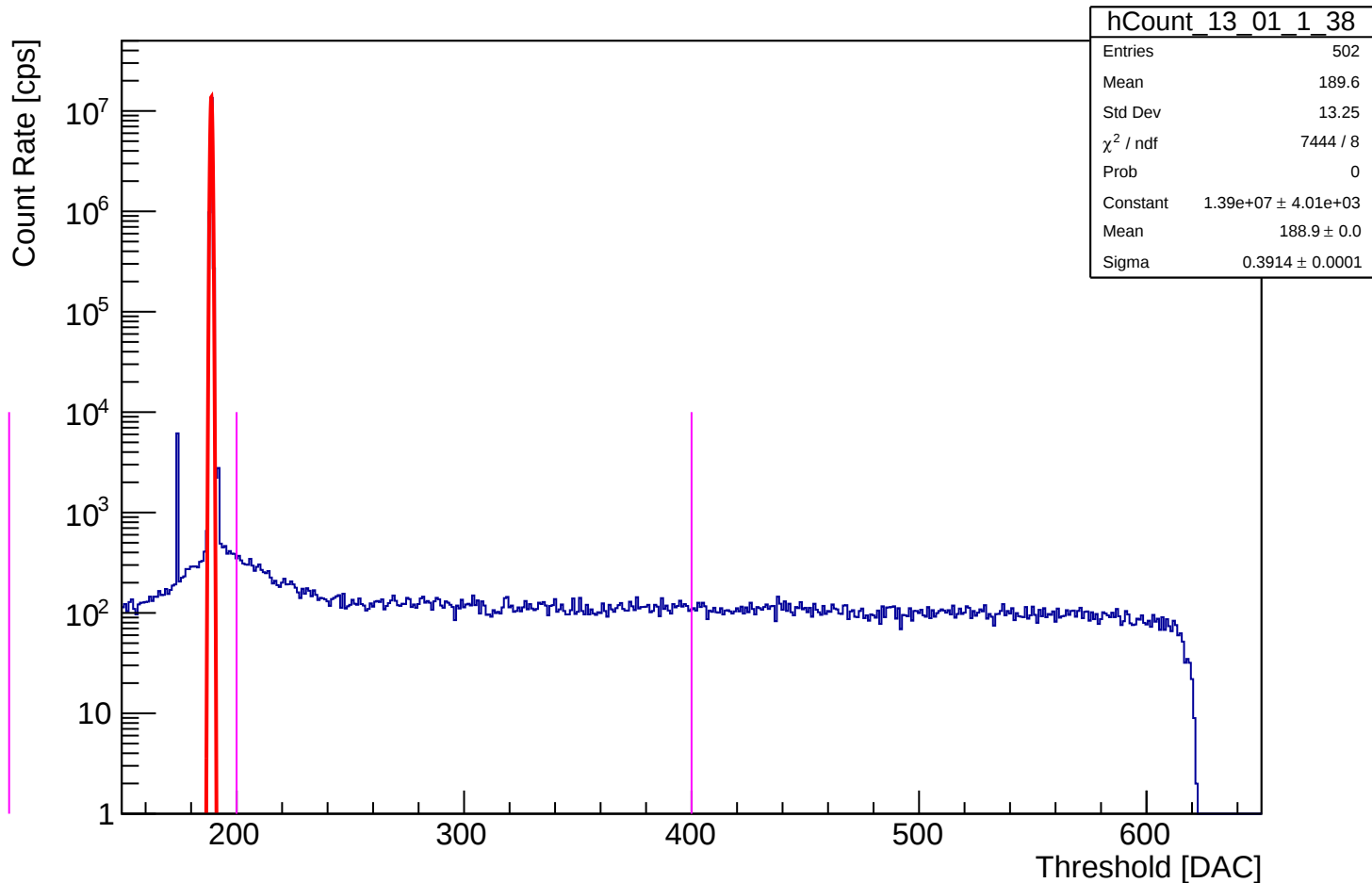
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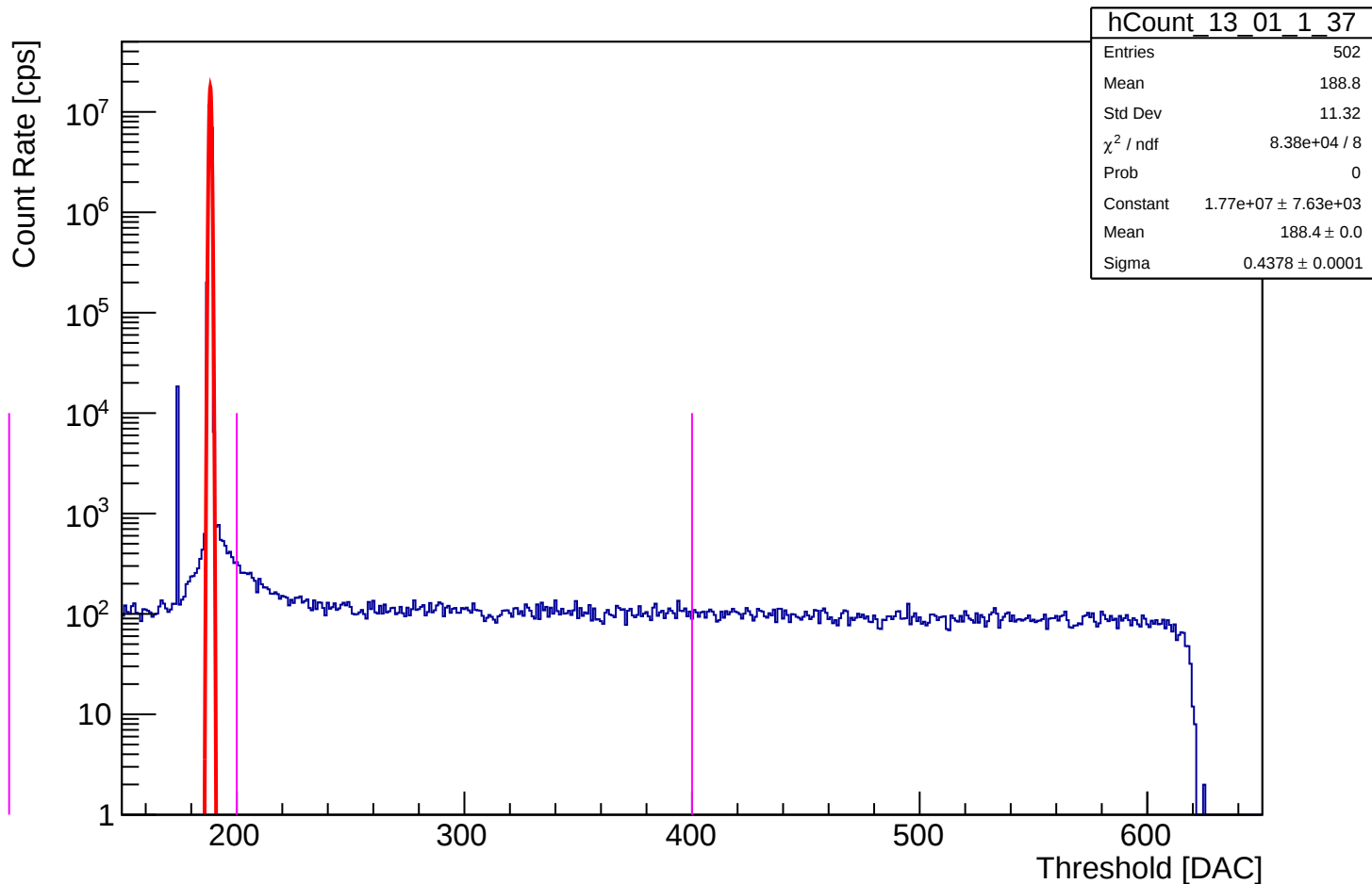
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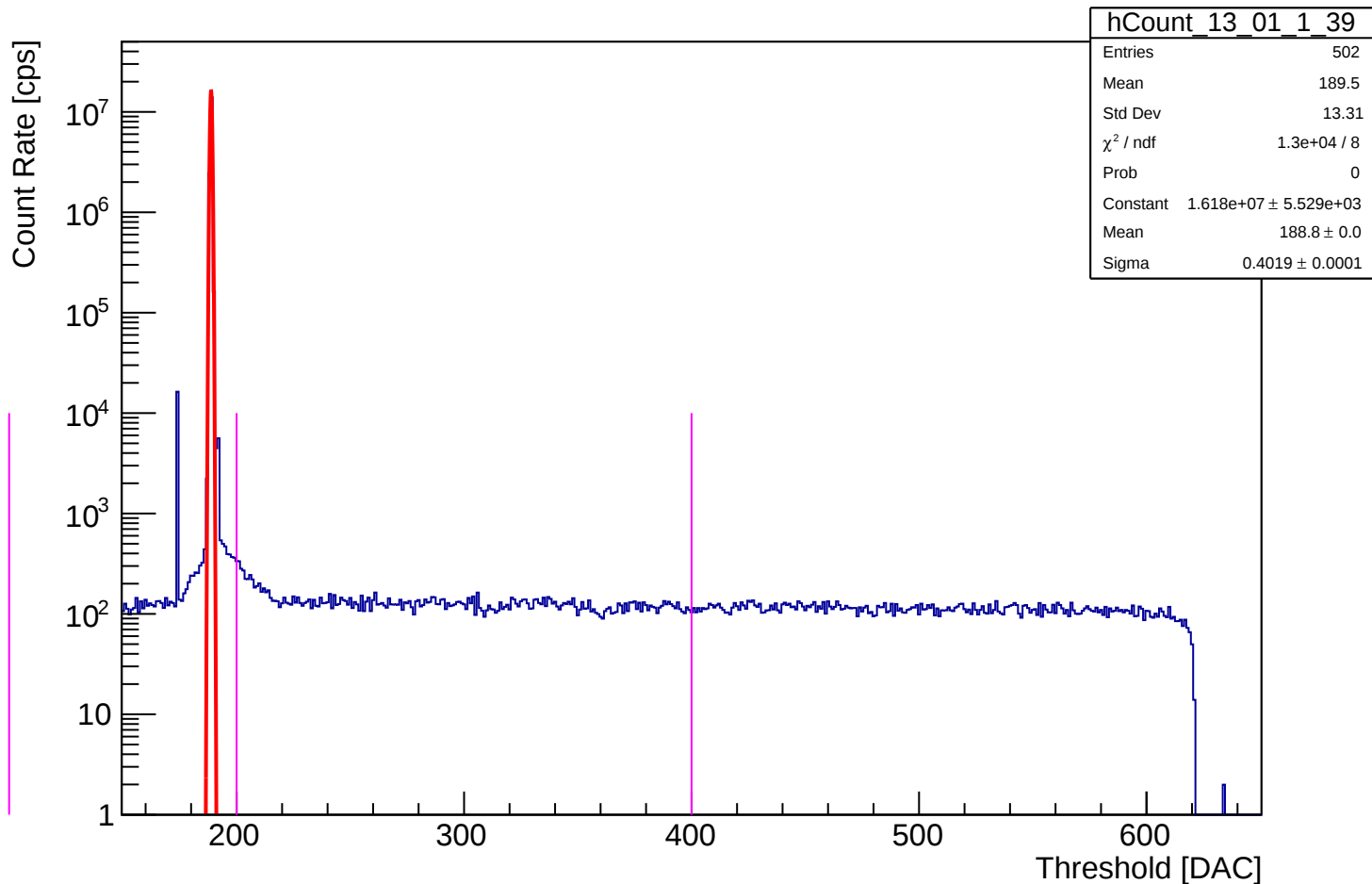
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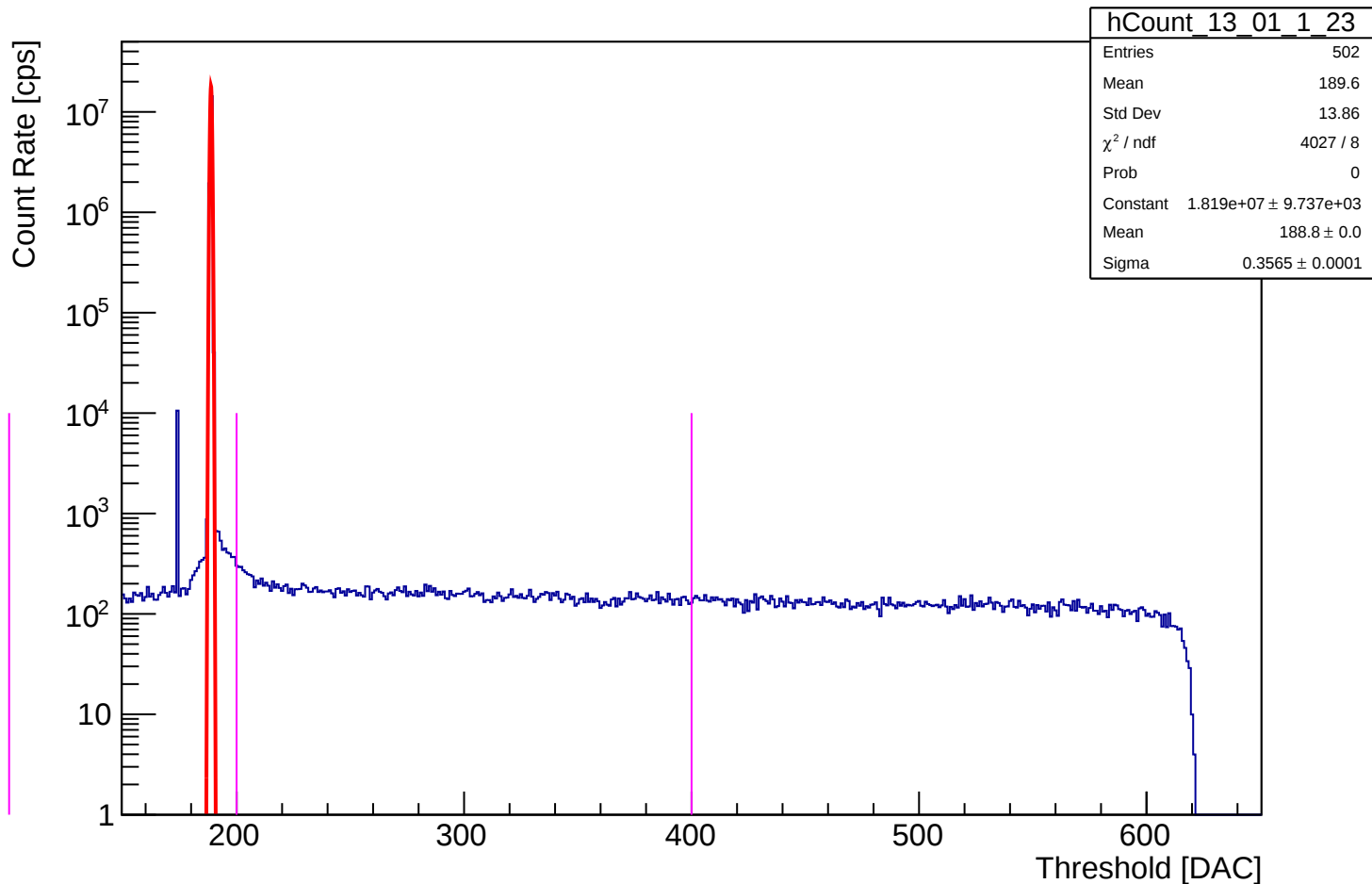
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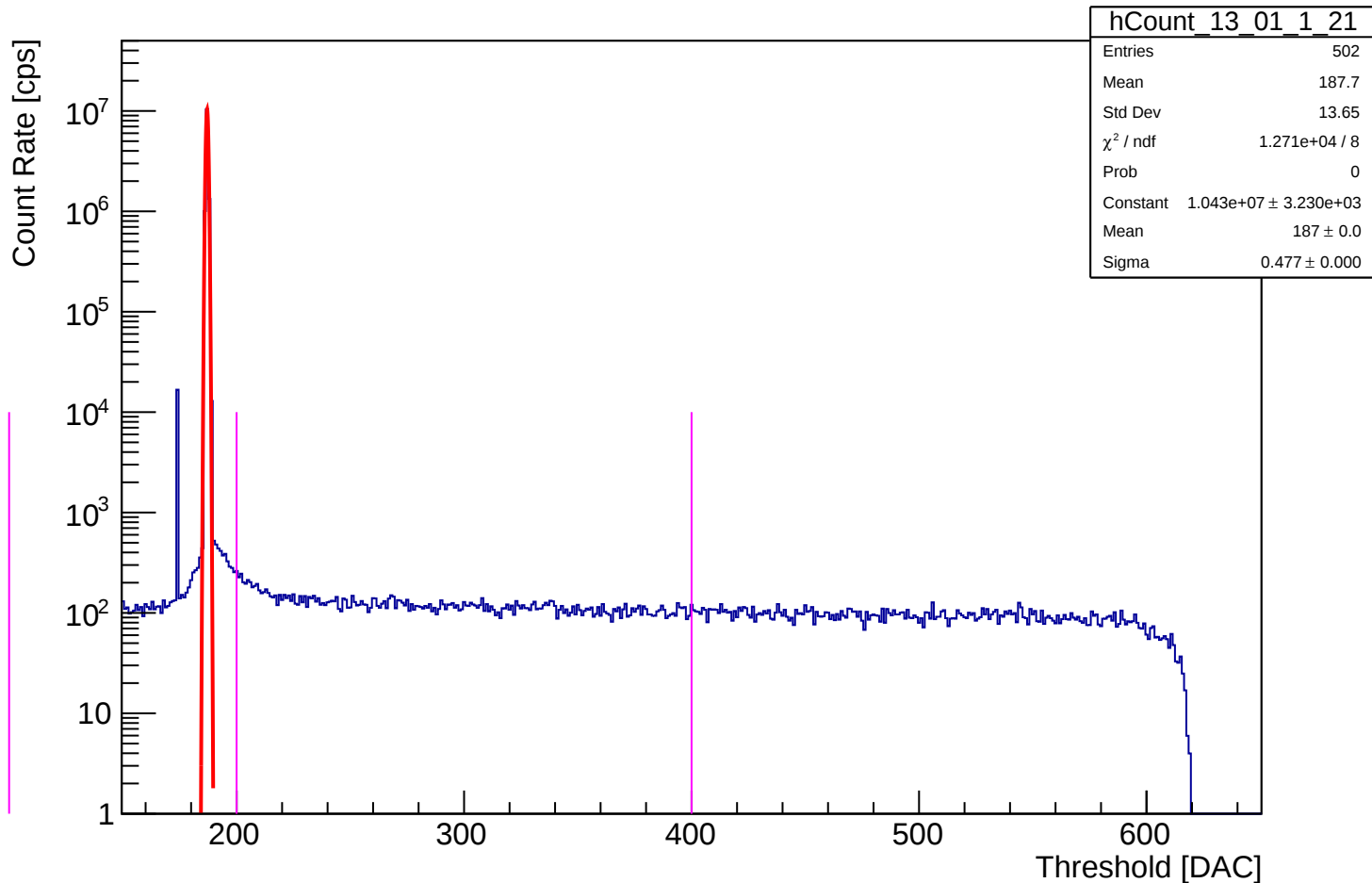
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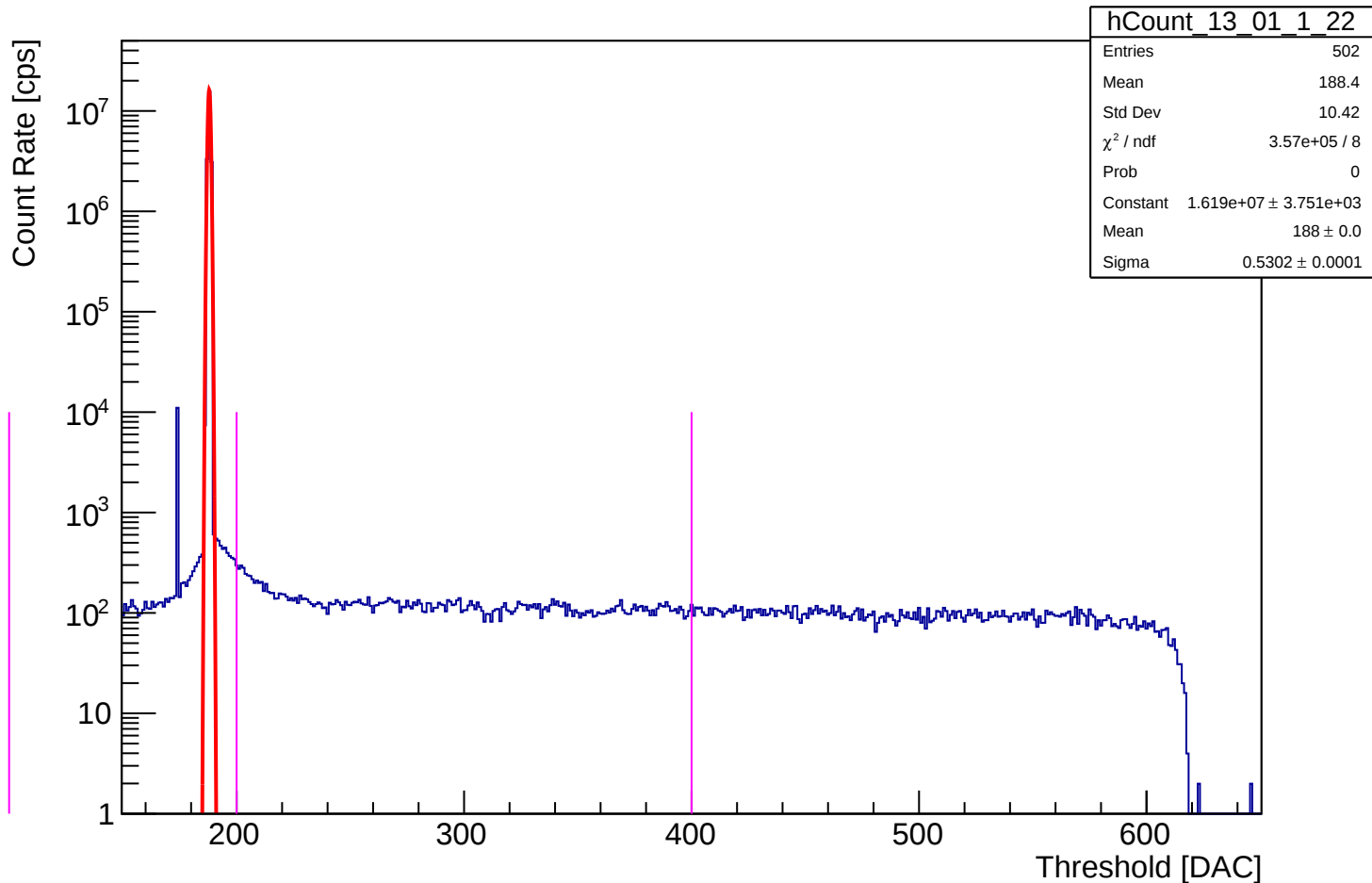
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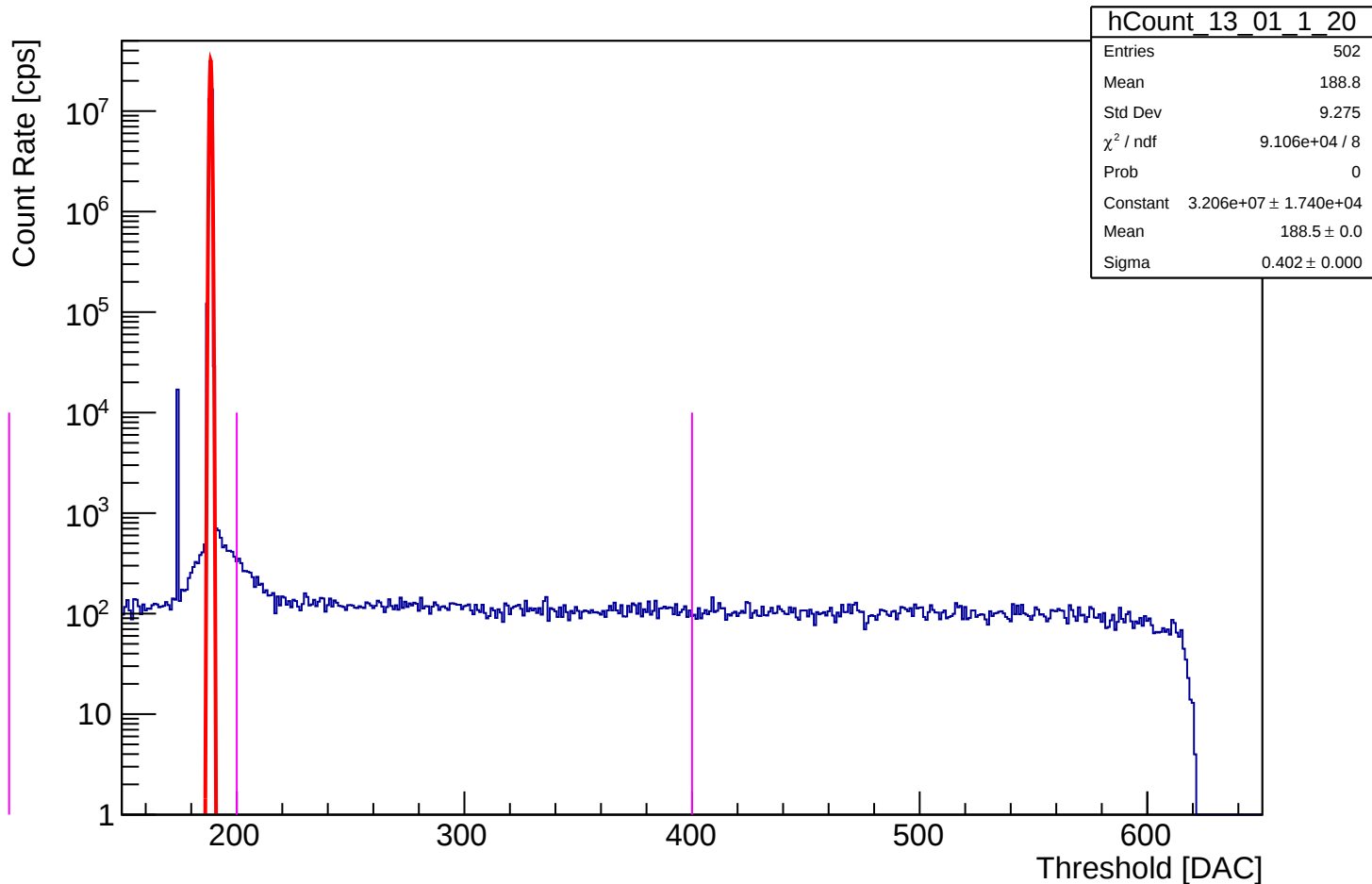
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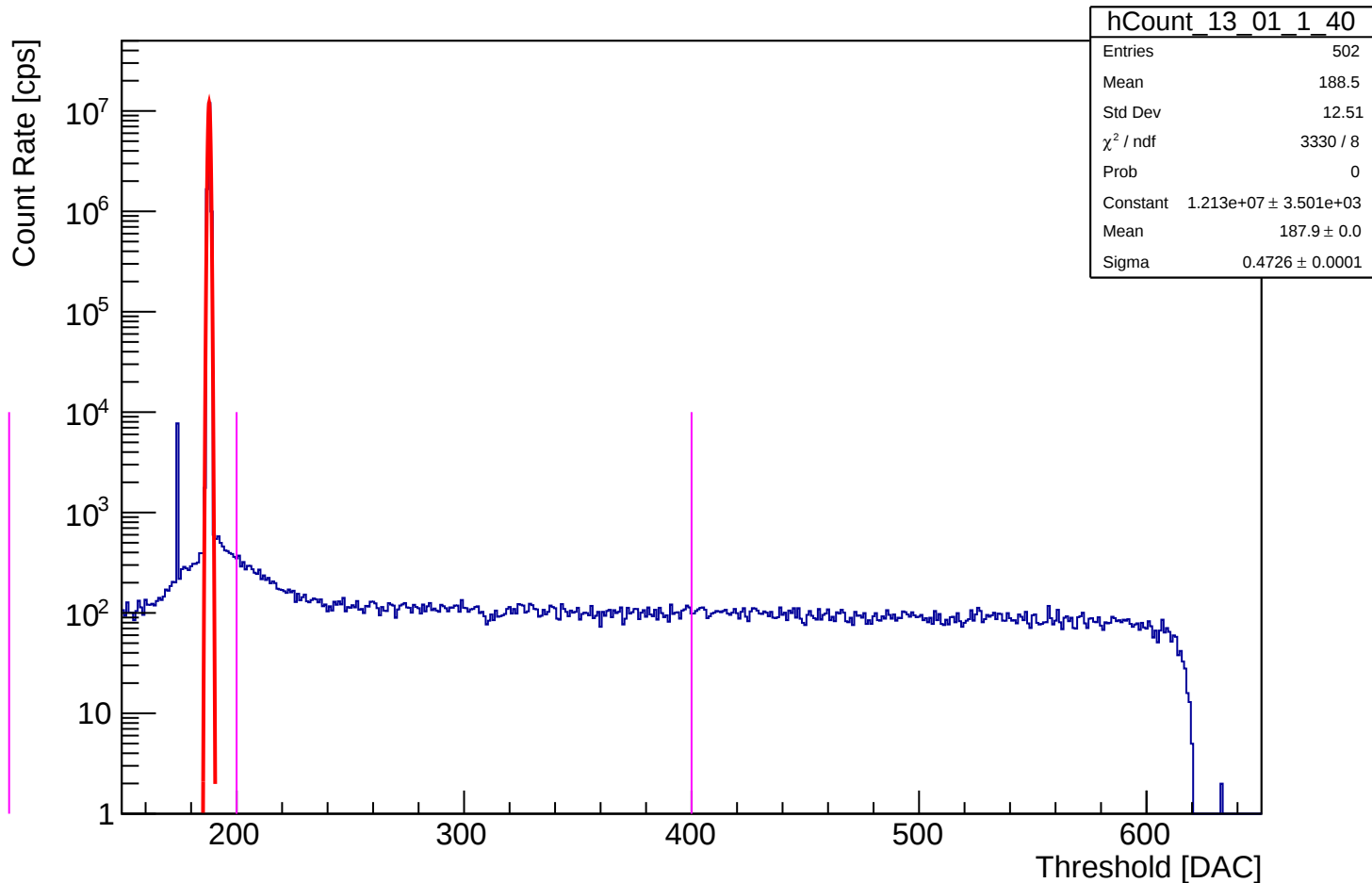
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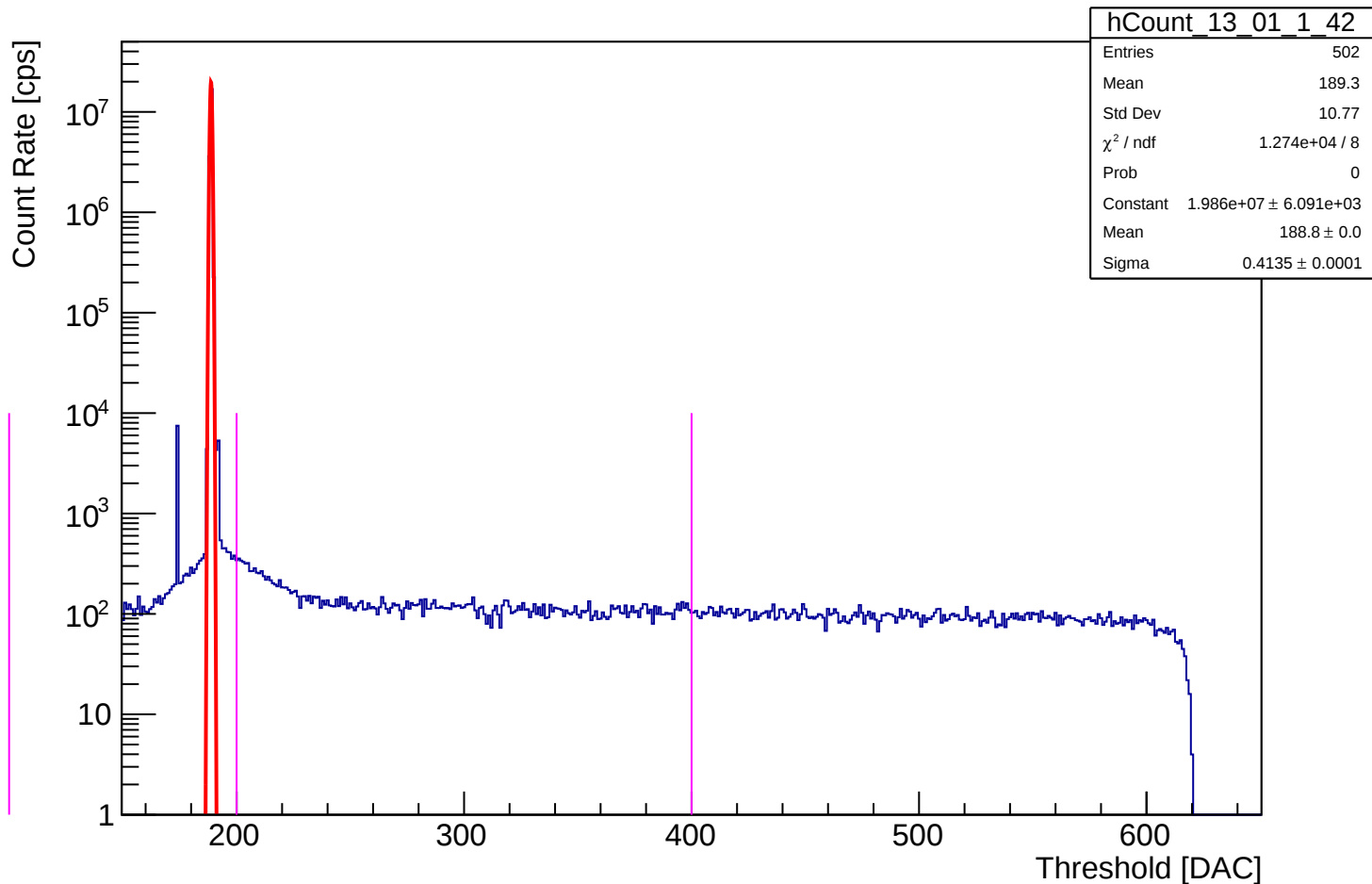
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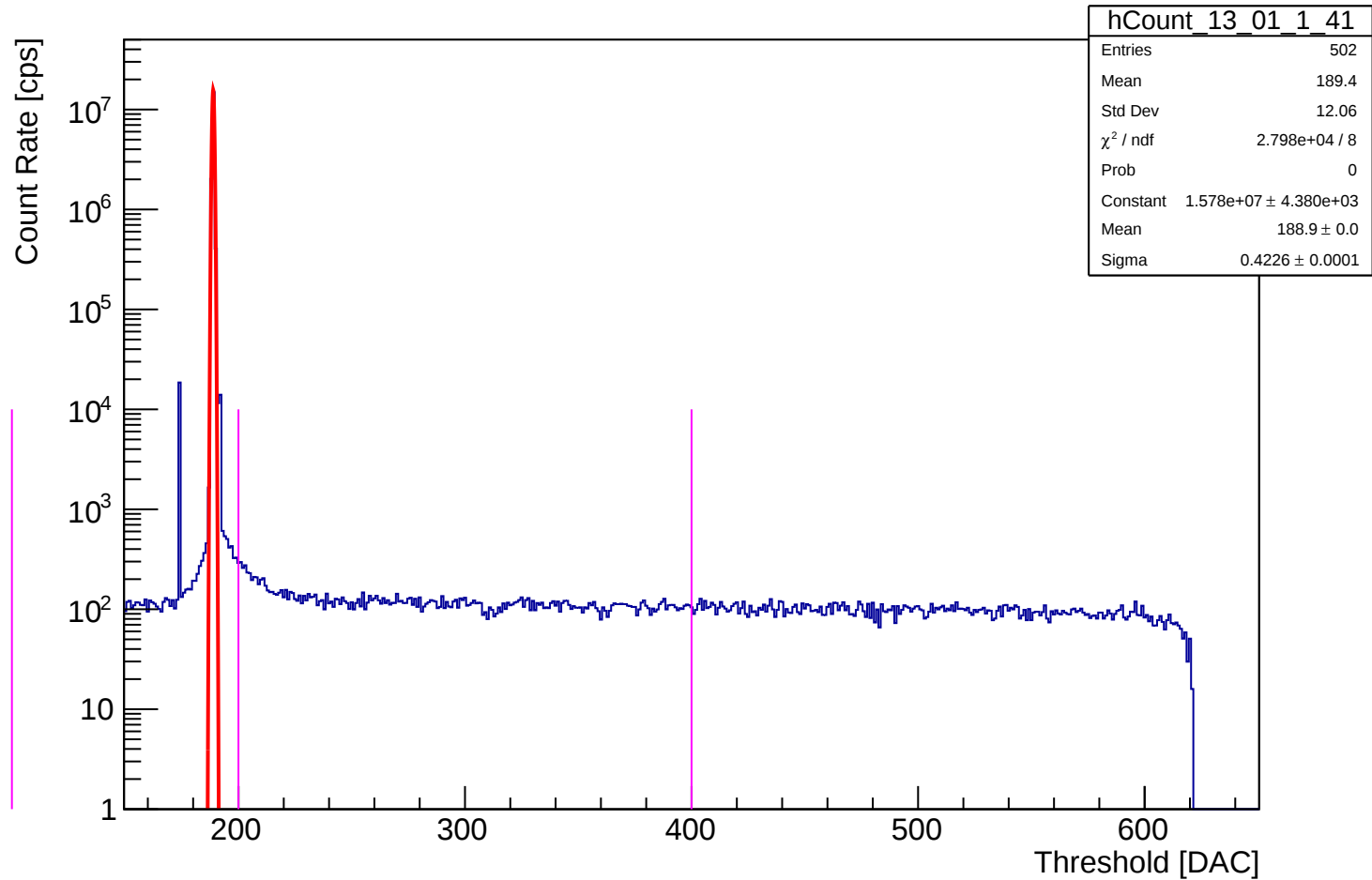


Row 1 Tile 1 Pmt 5 Pixel 21 Slot 13 Fiber 1 Asic 1 Channel 40

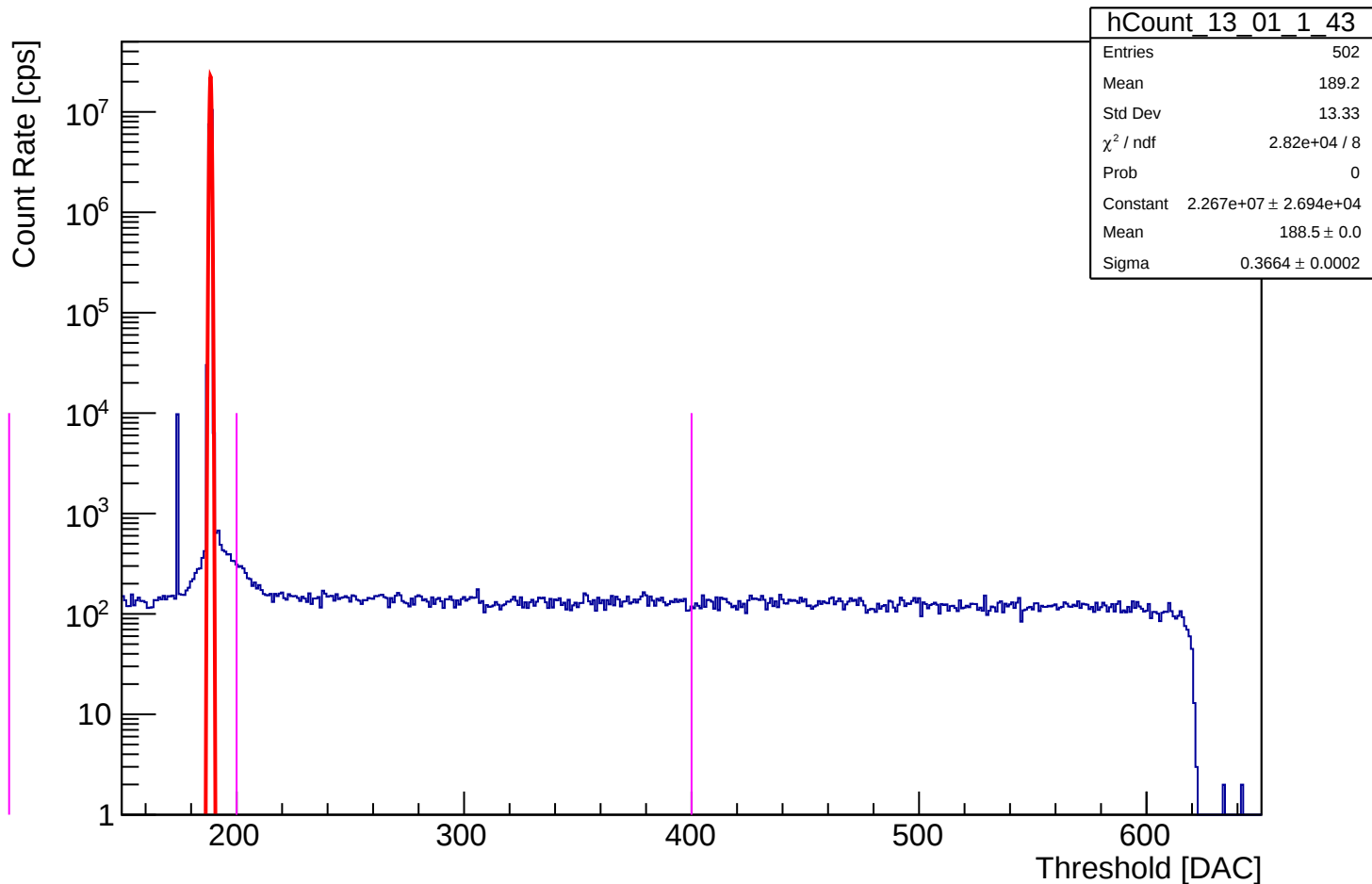


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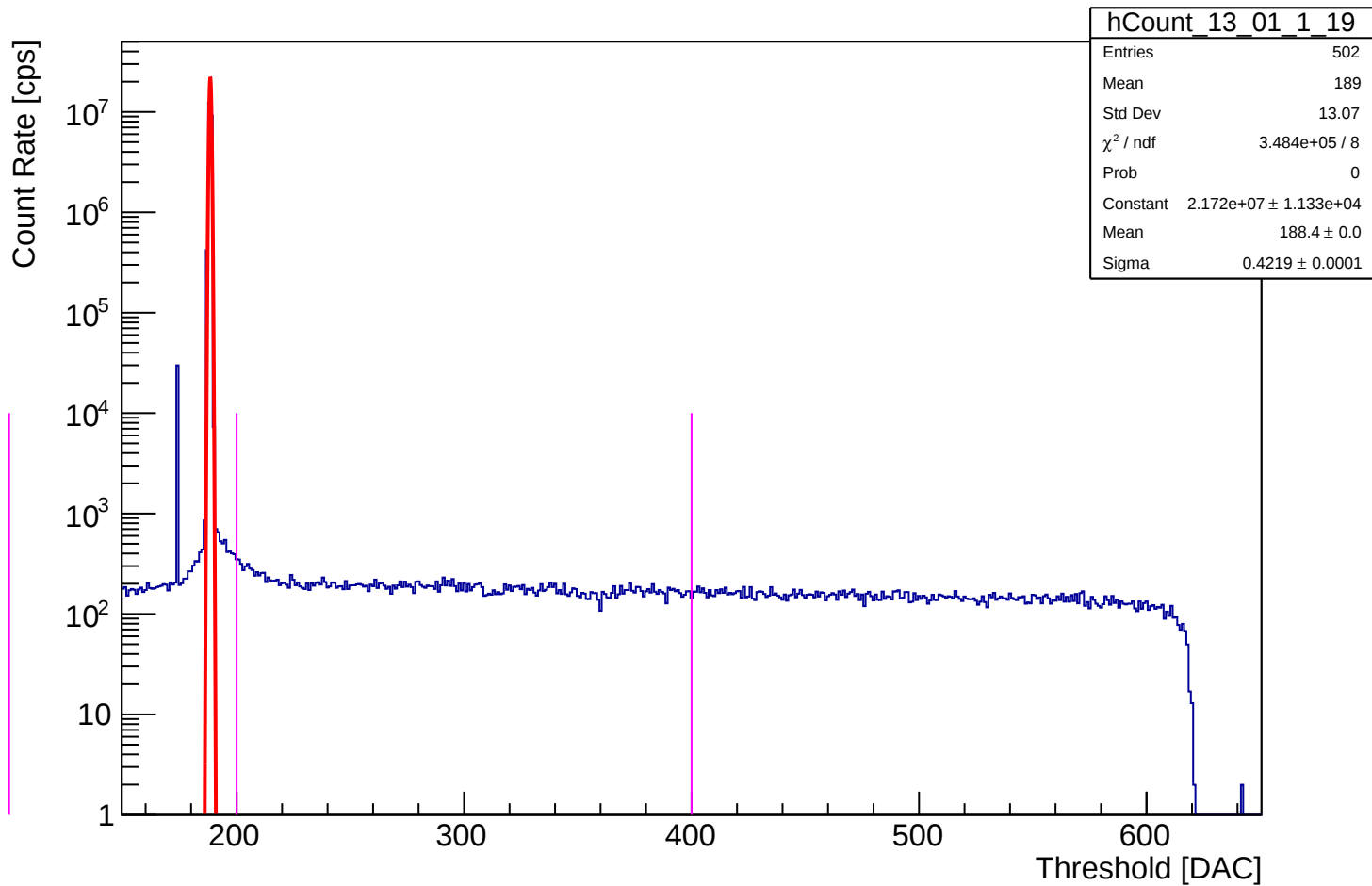




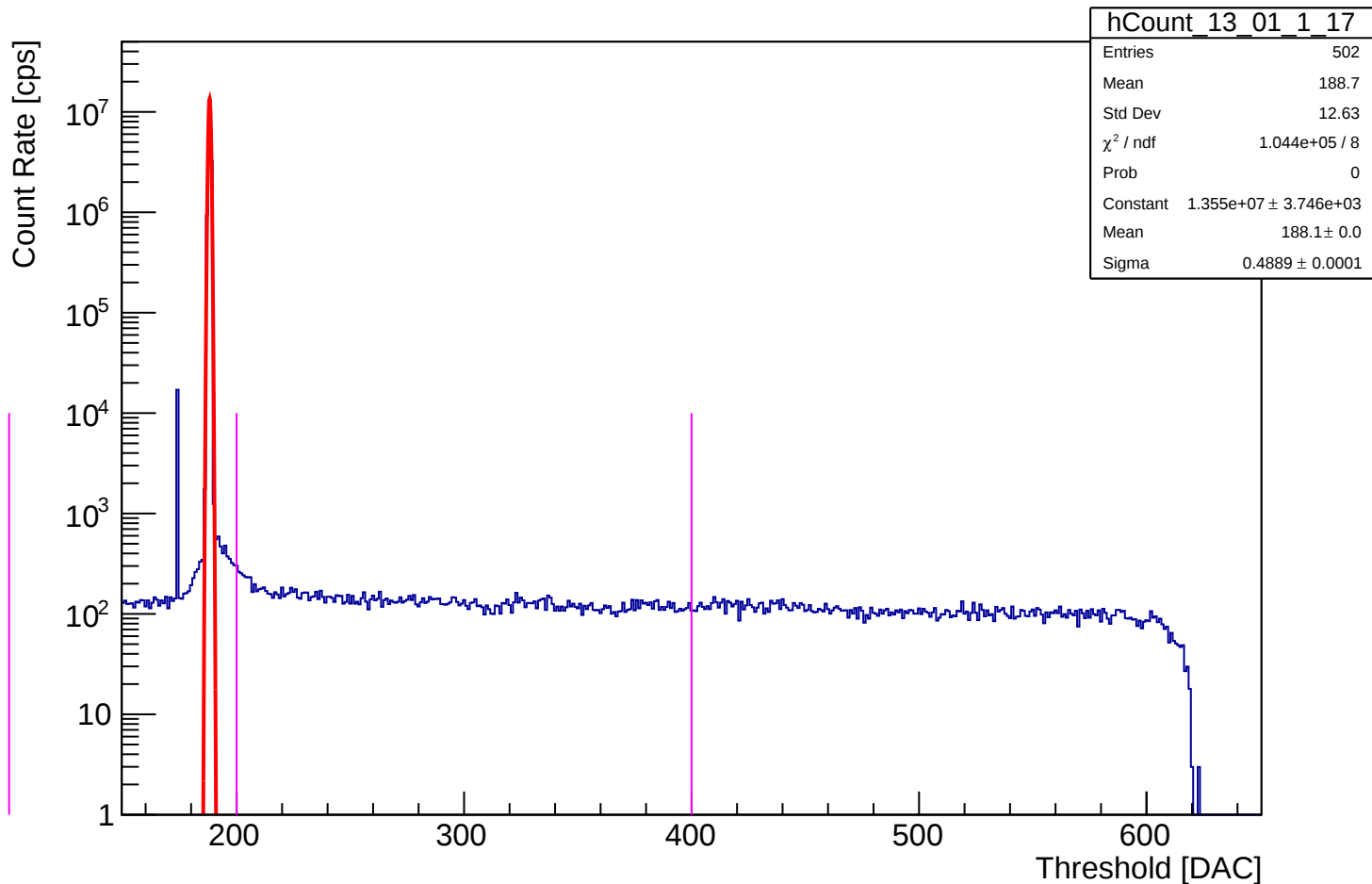
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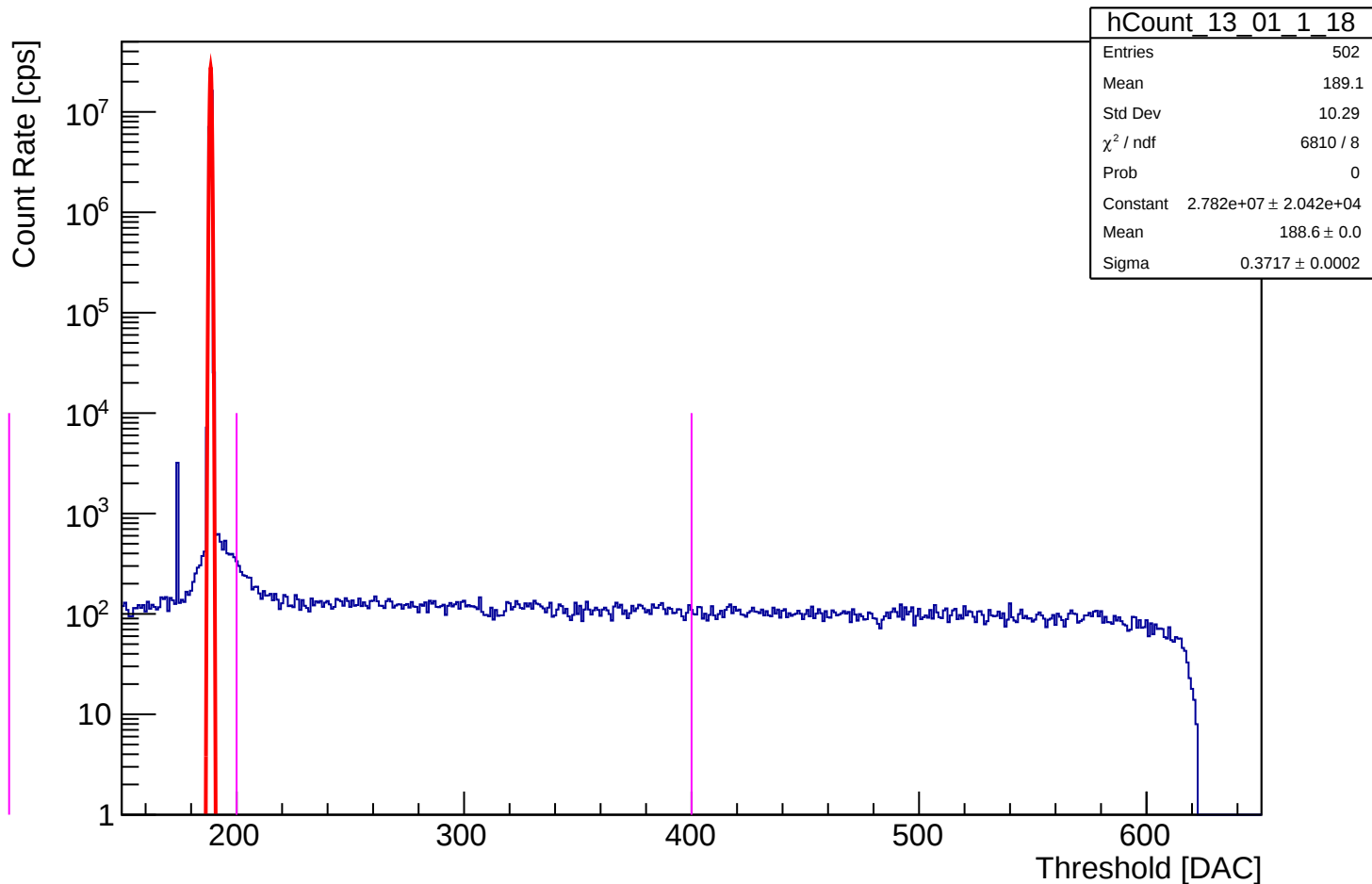
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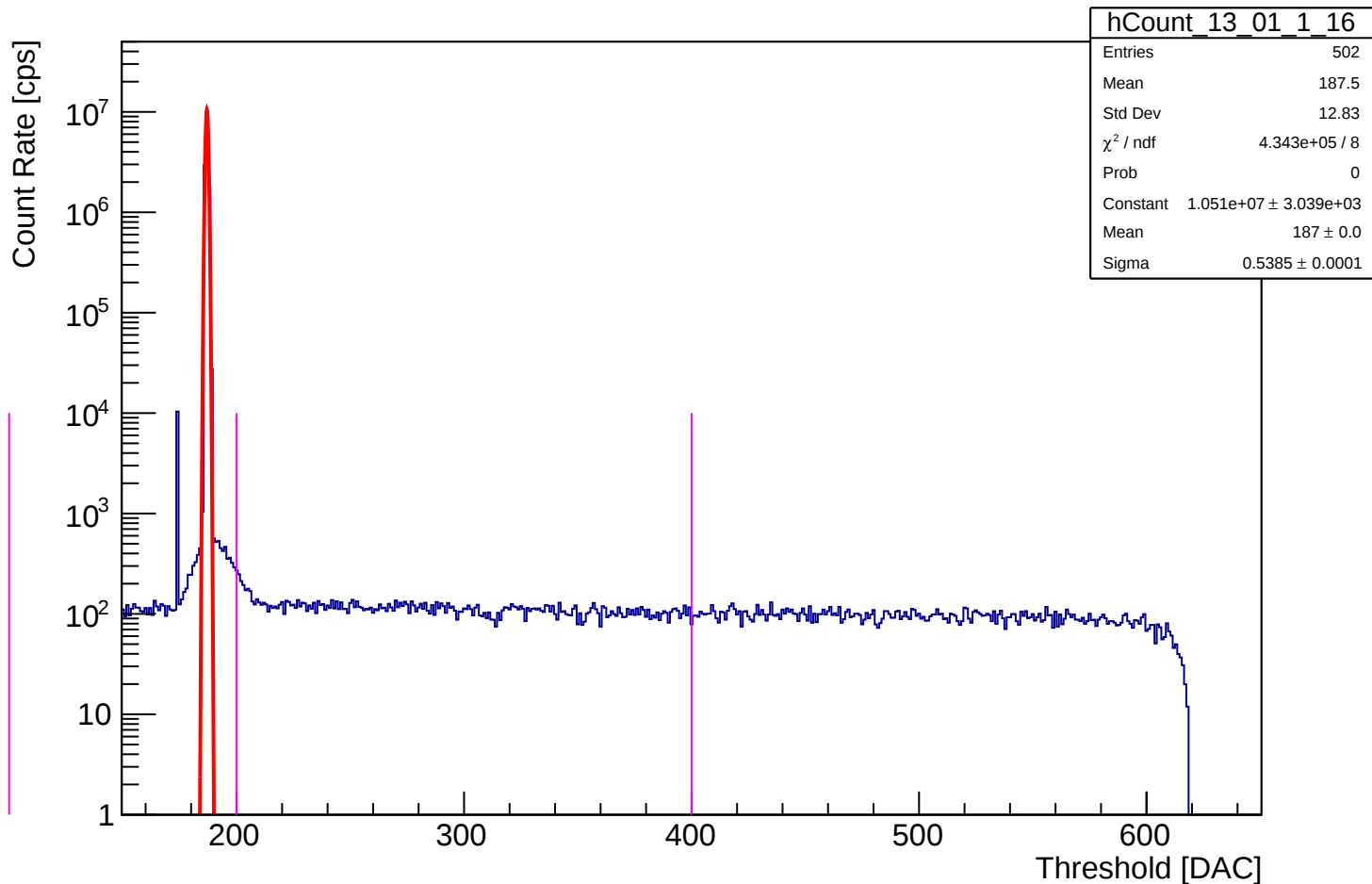
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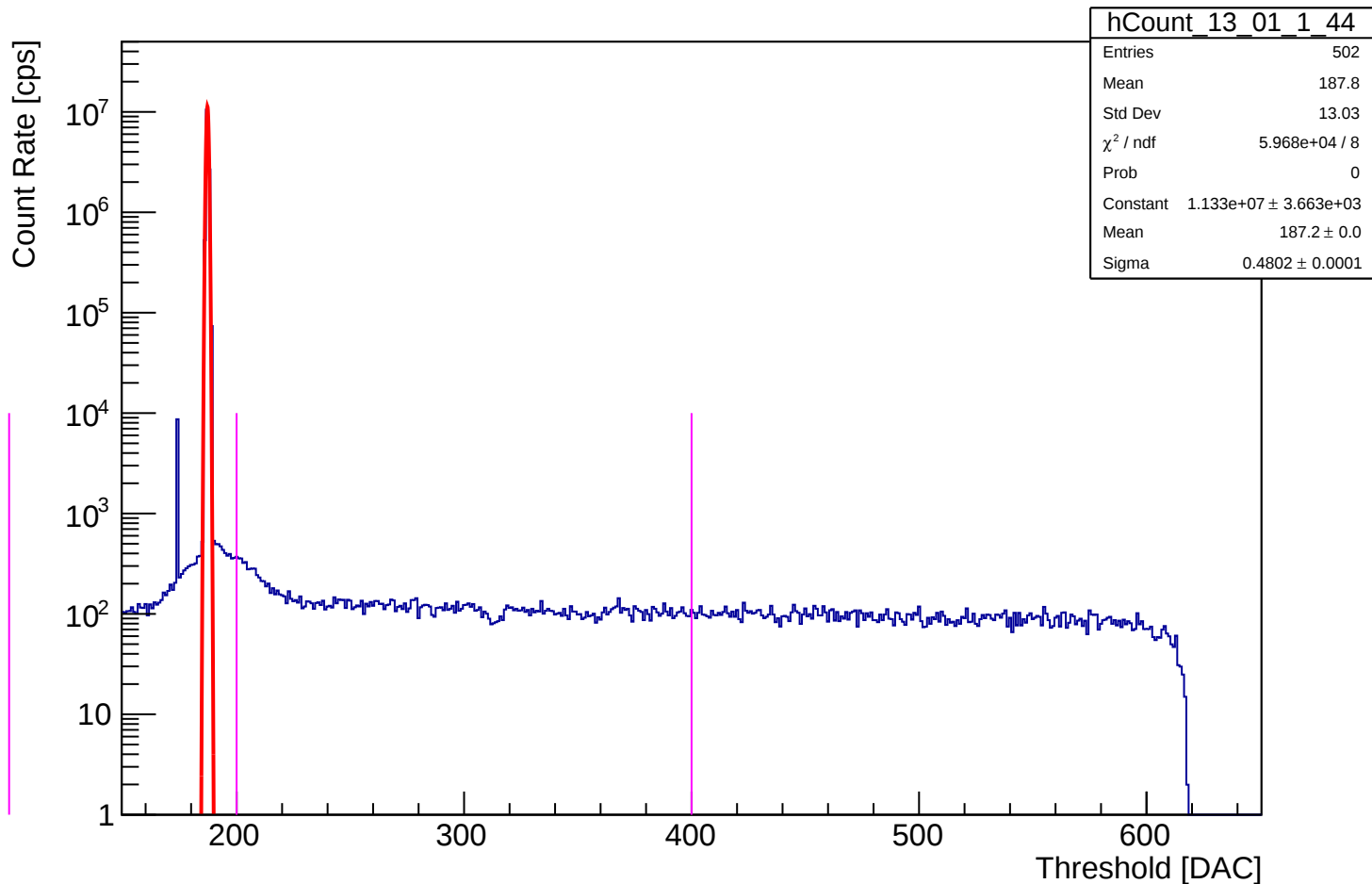
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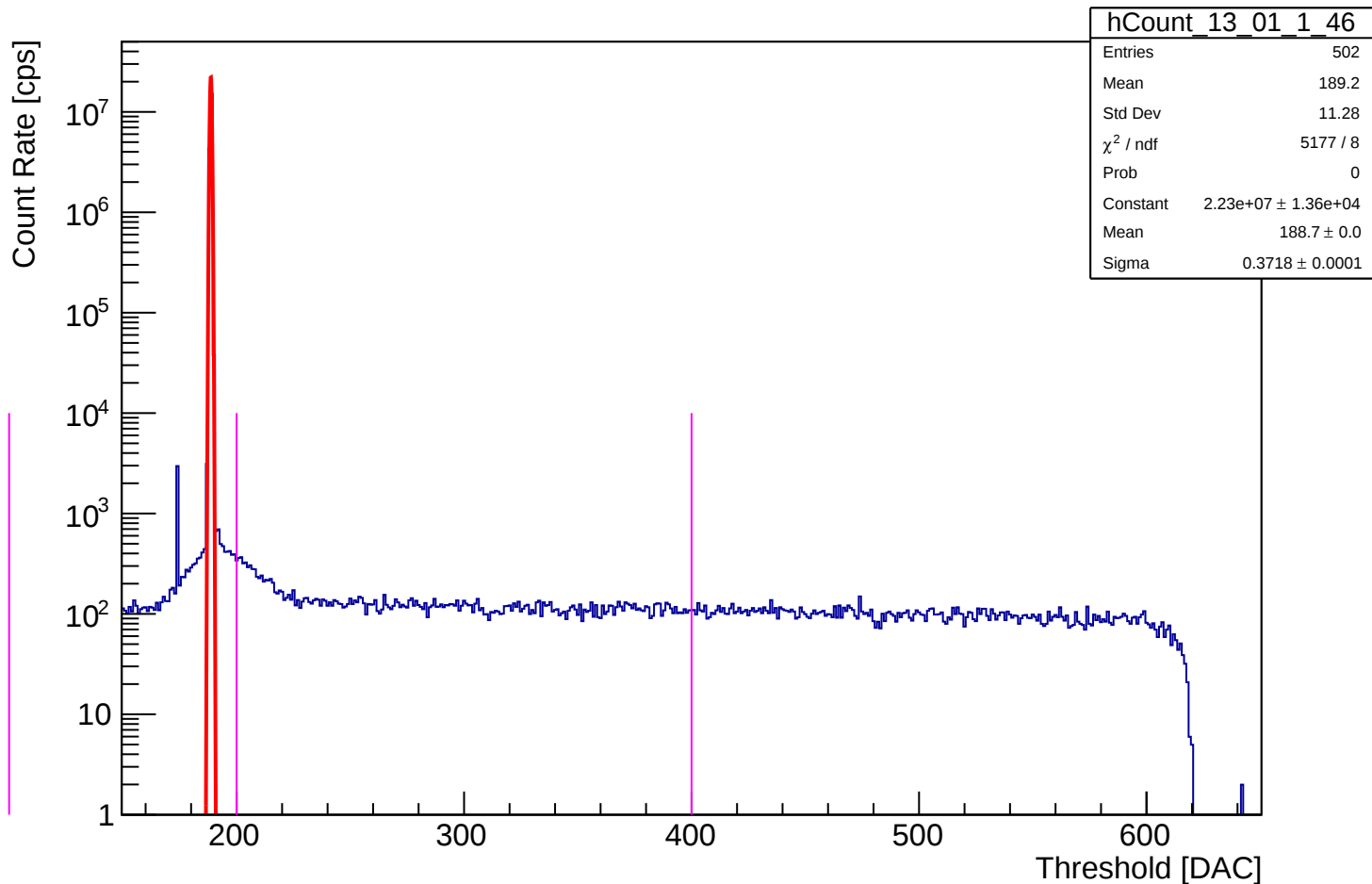
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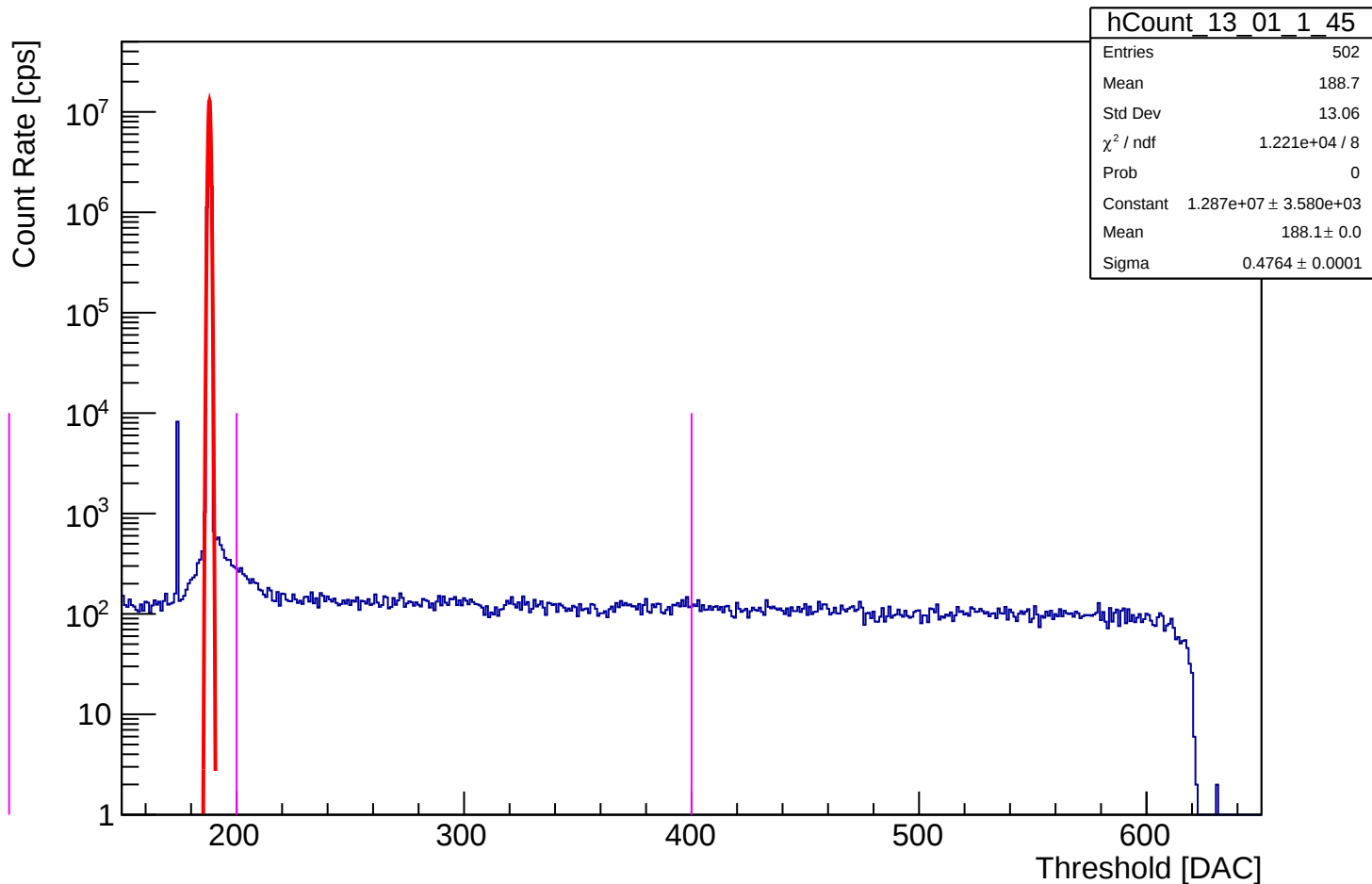
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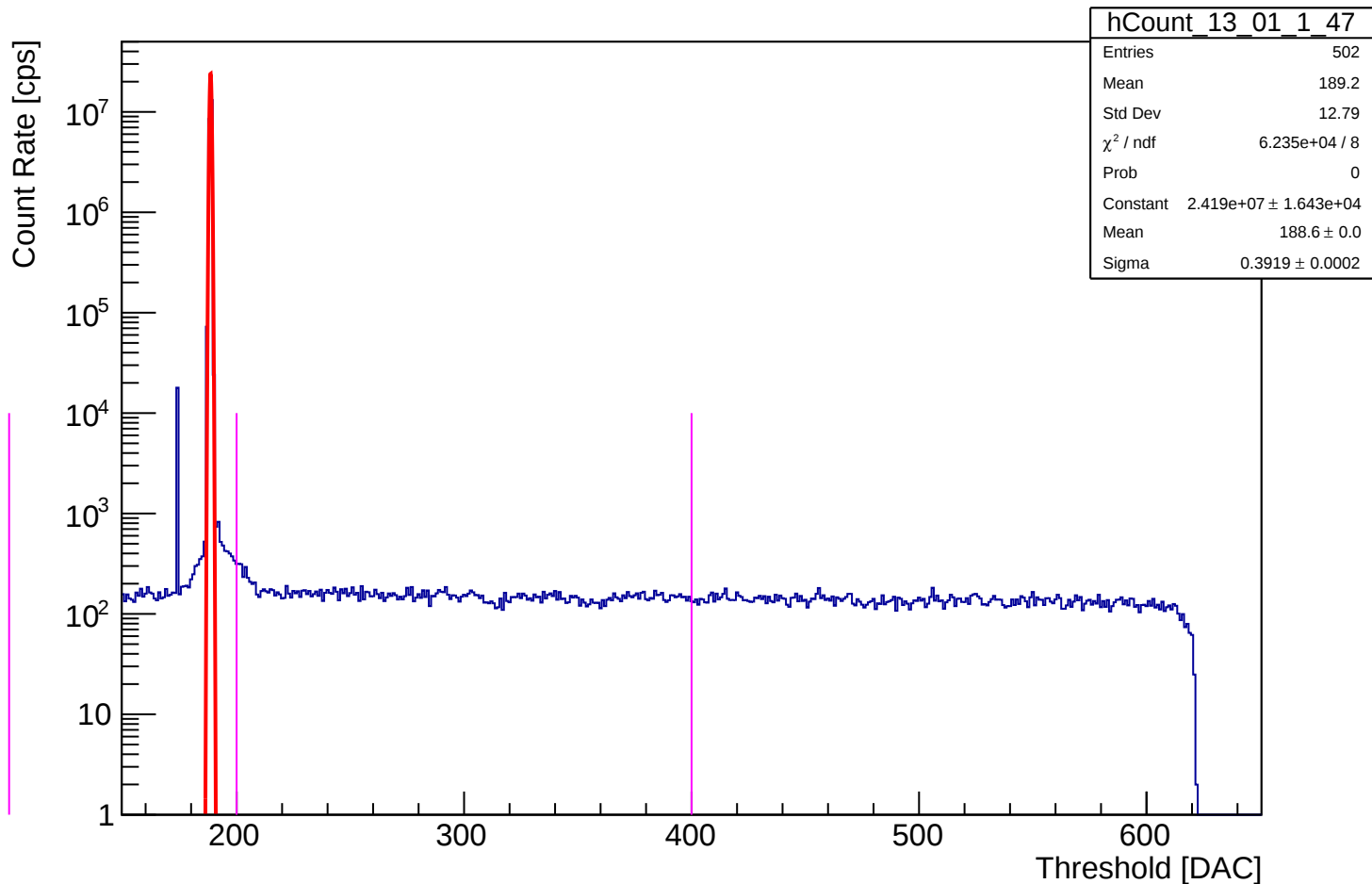
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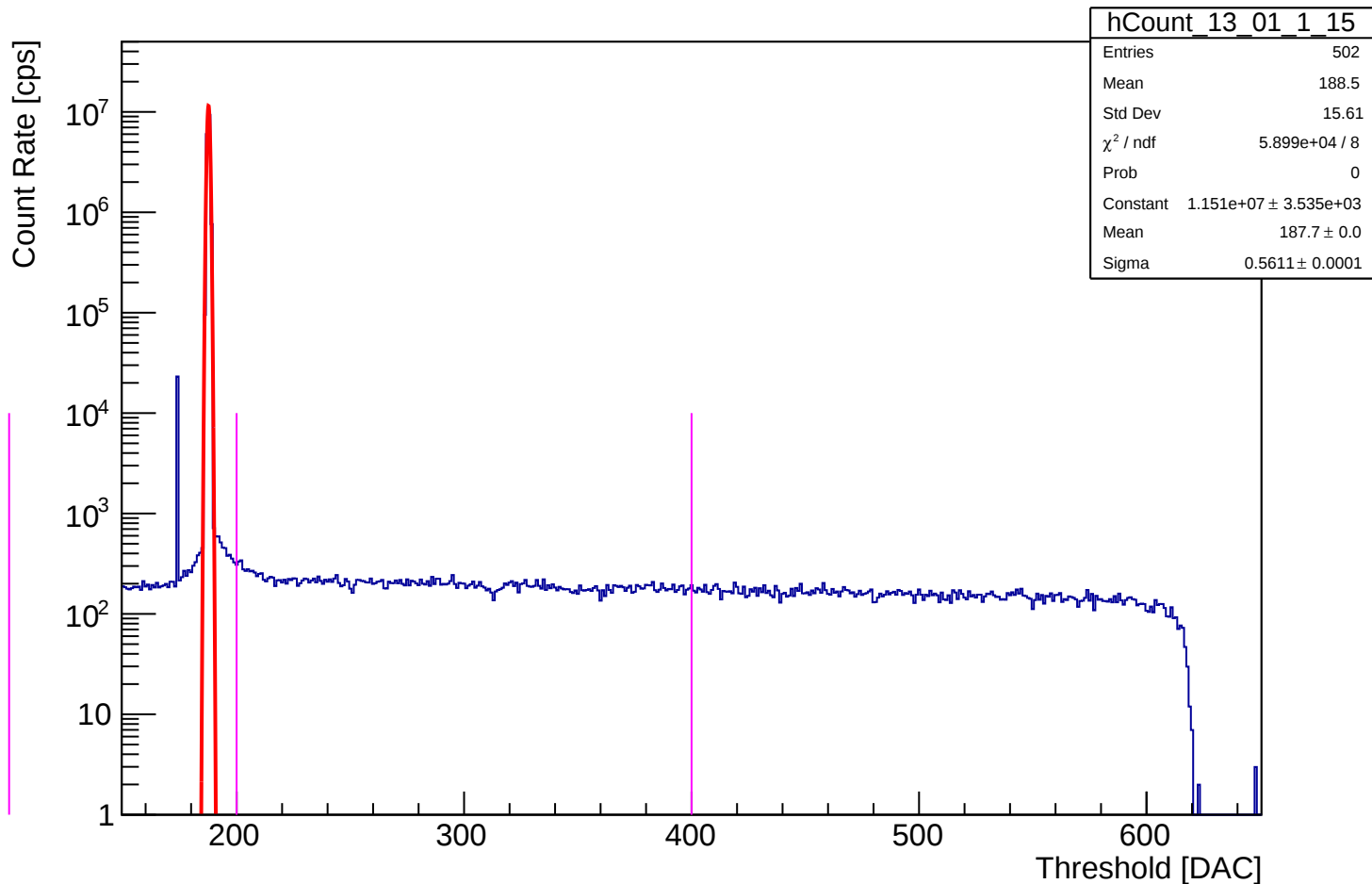
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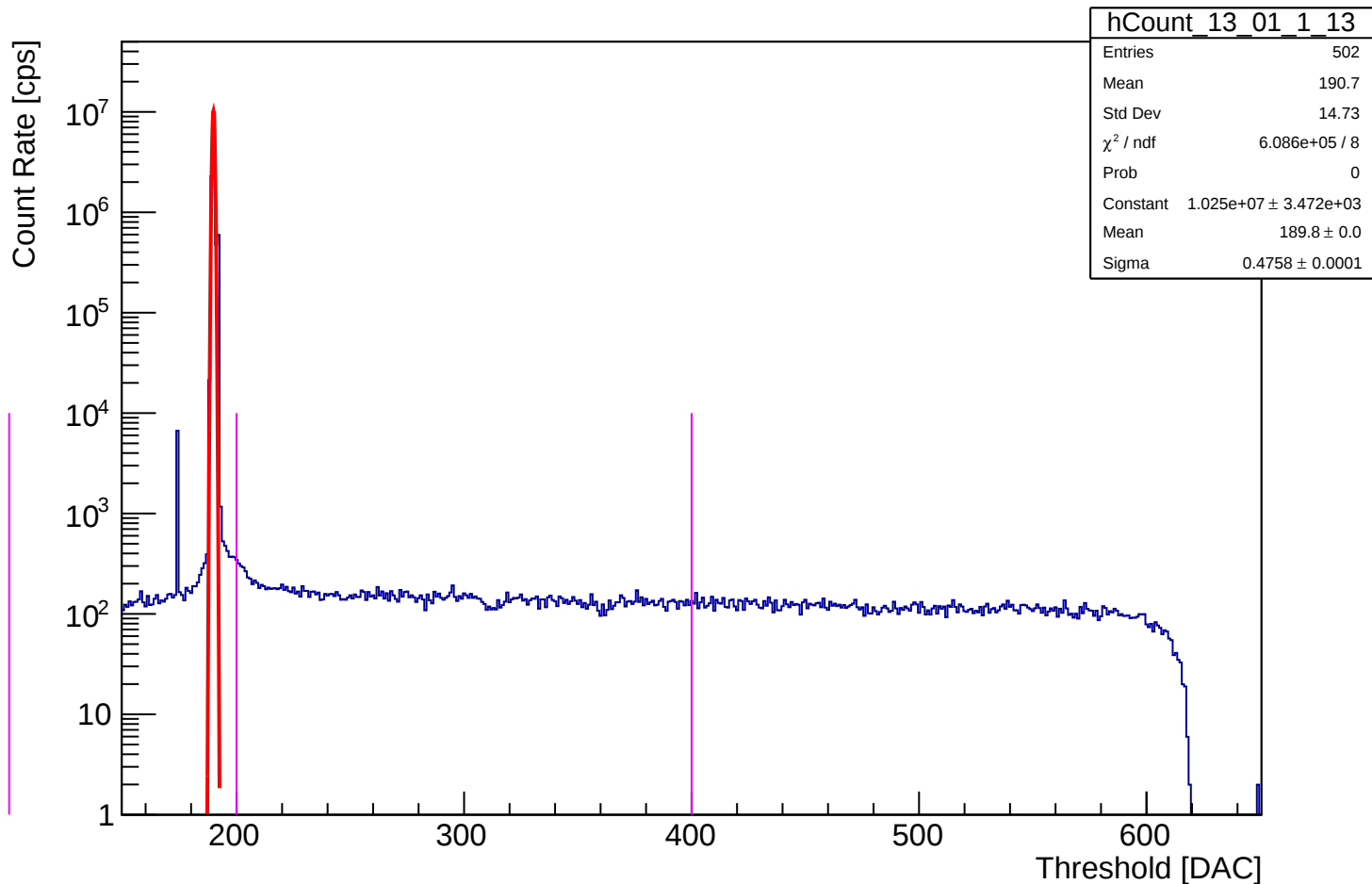
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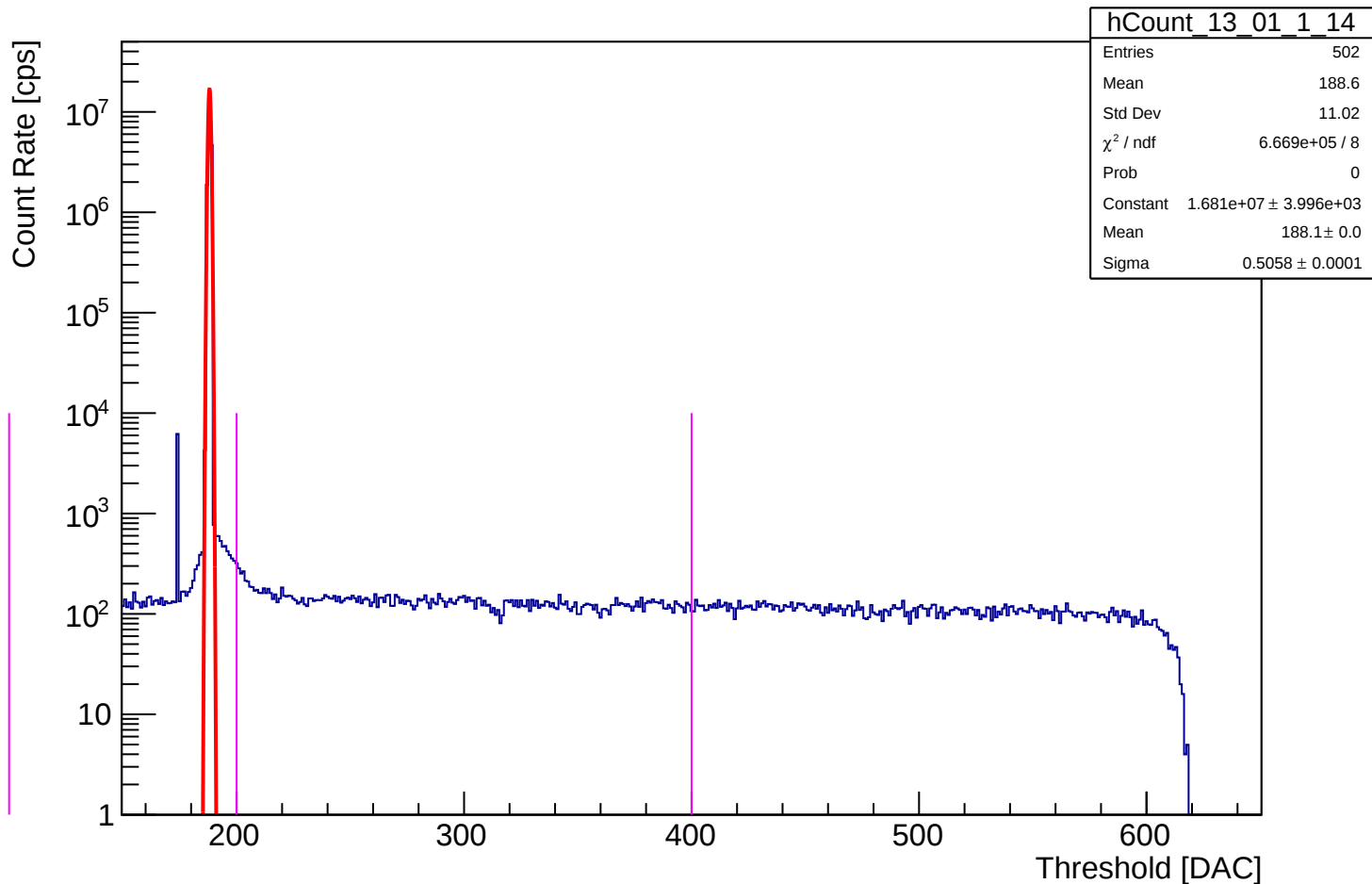
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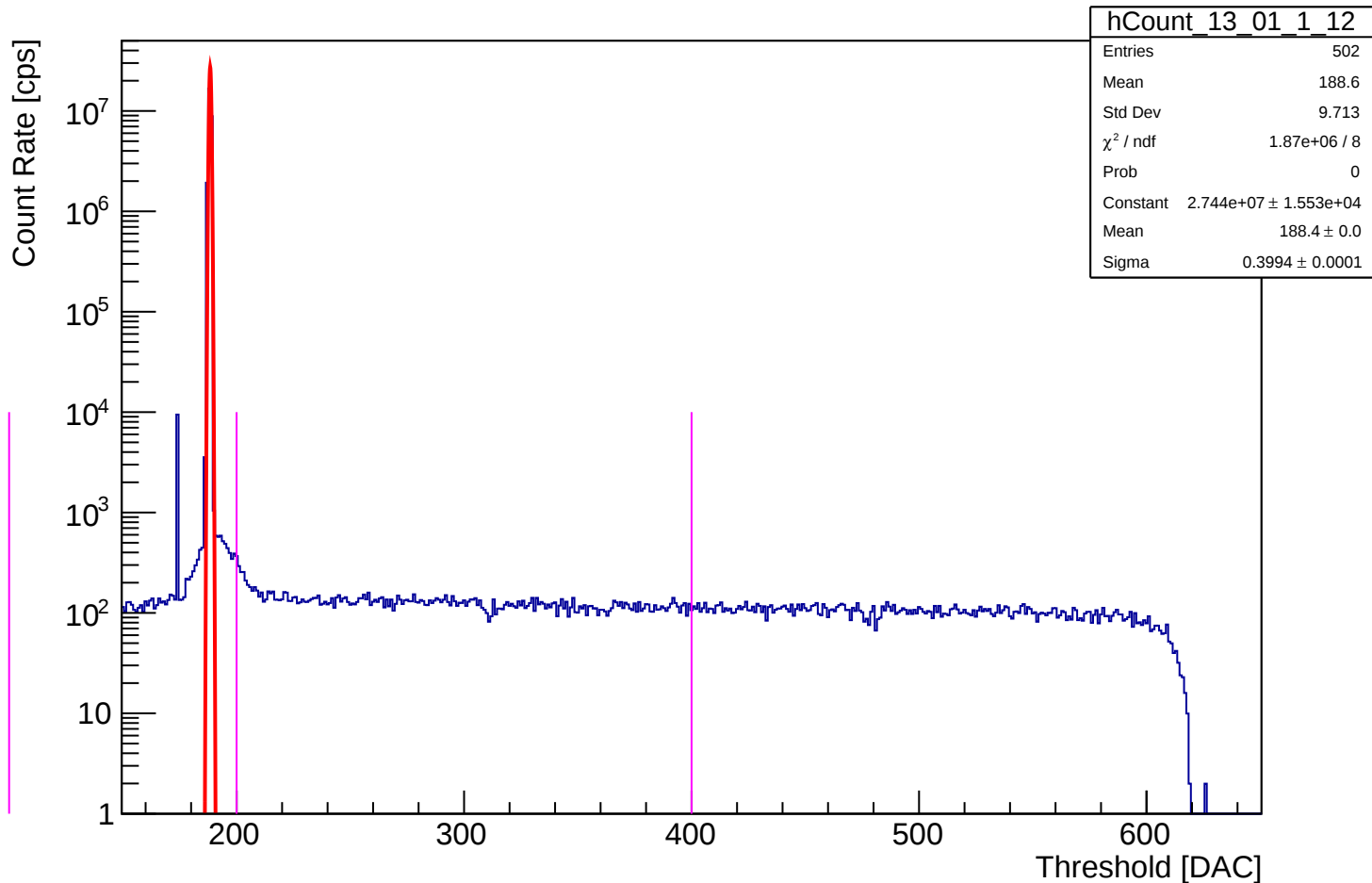
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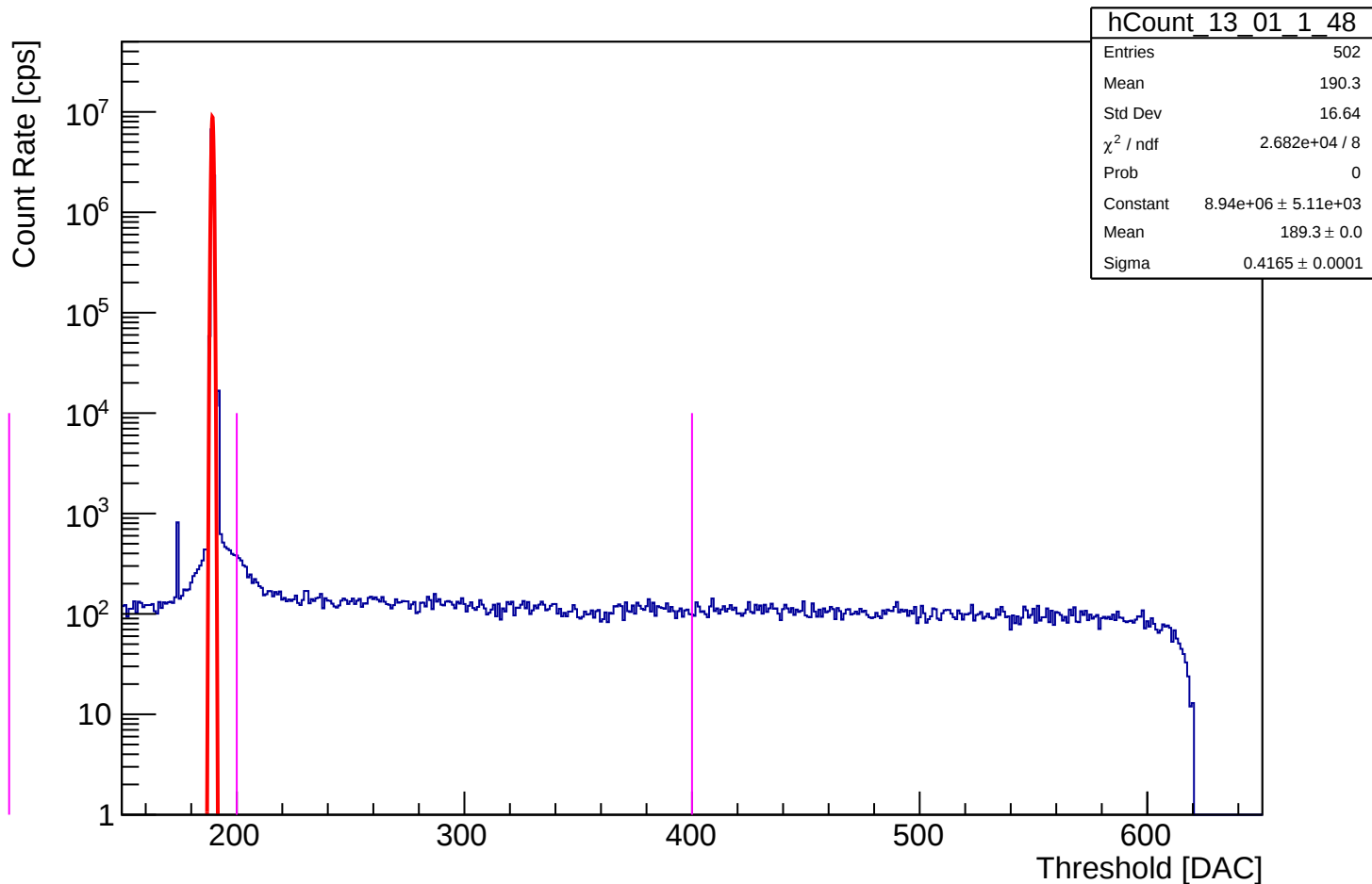
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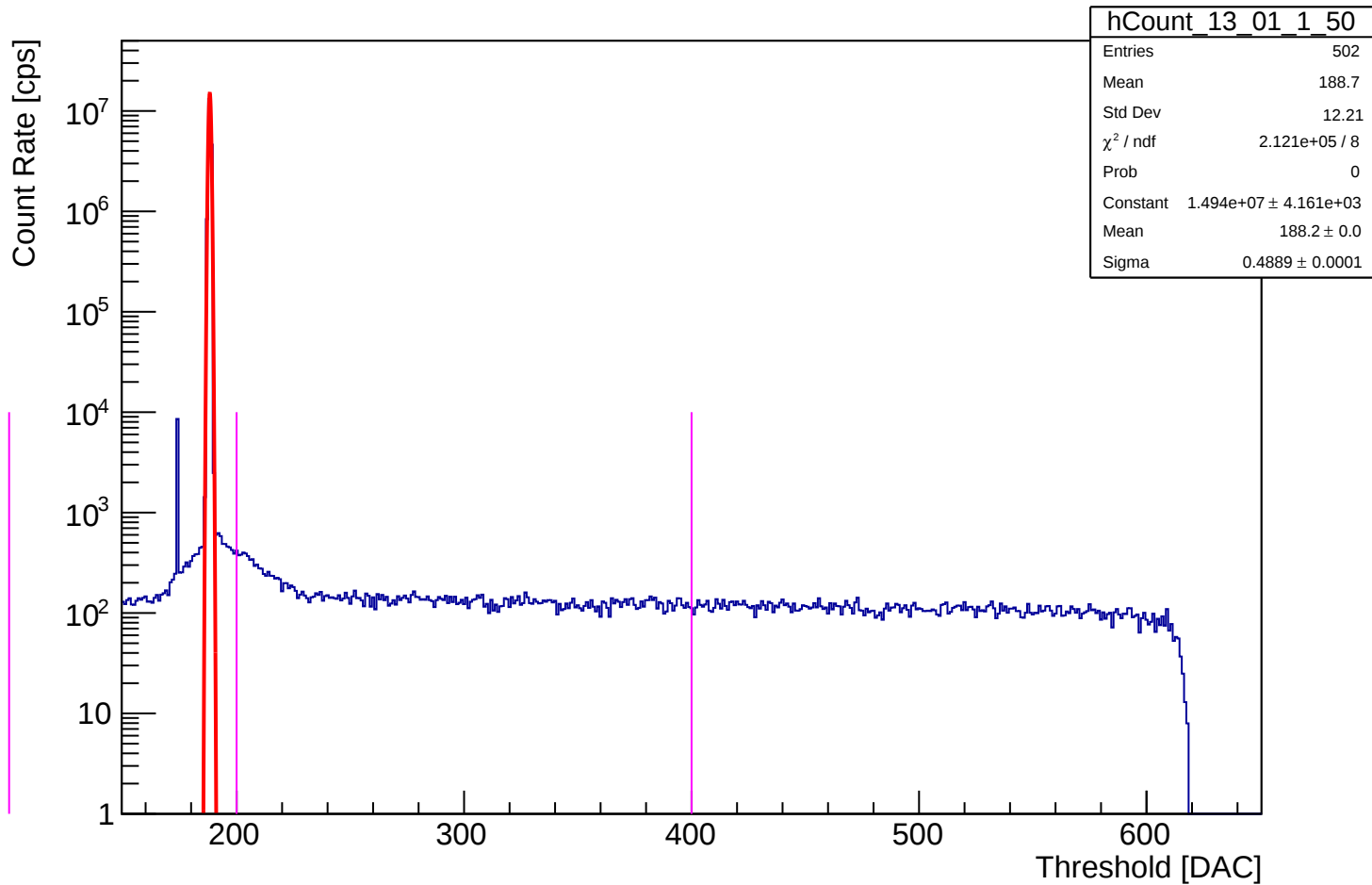
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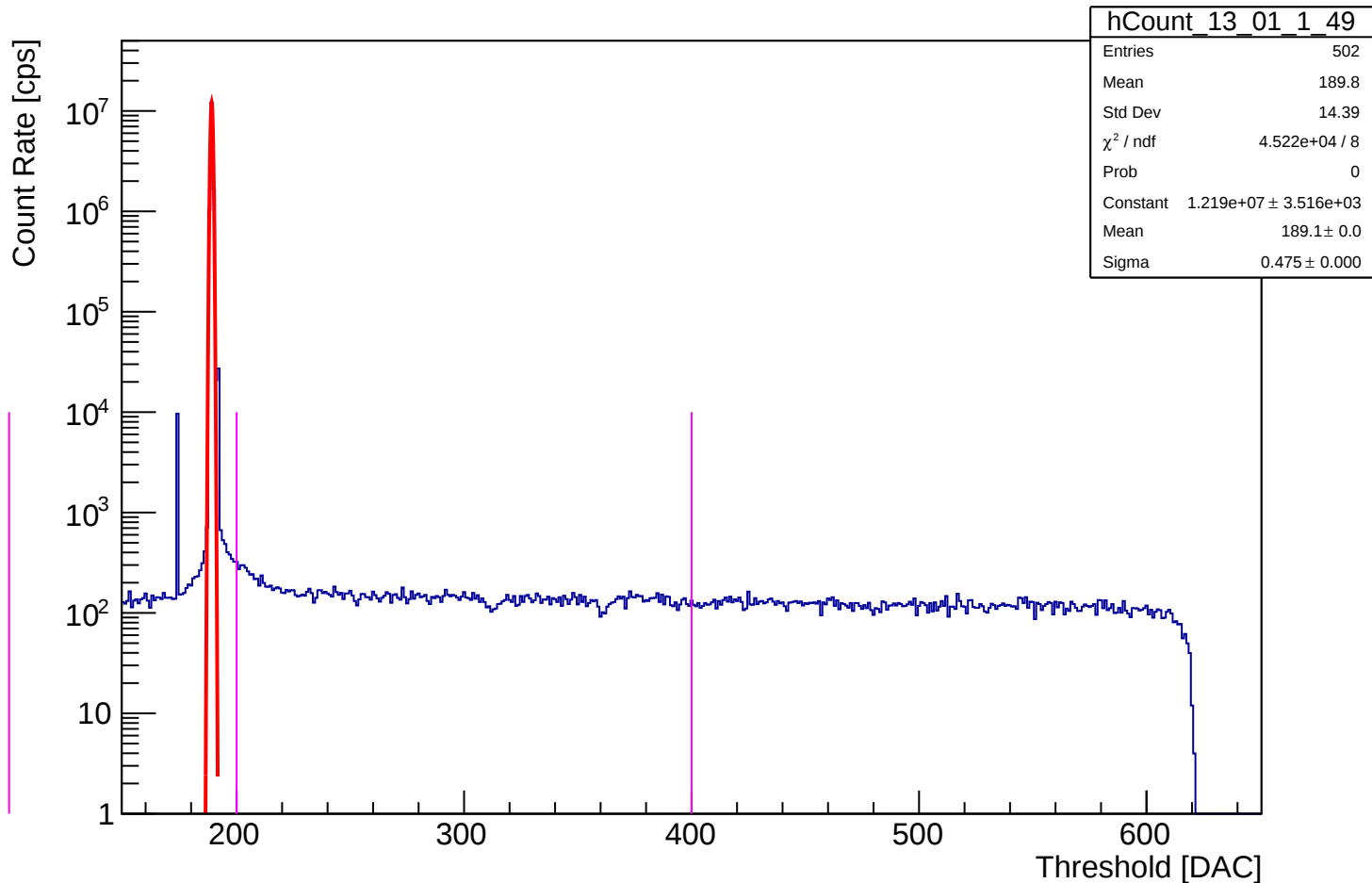
Row 1 Tile 1 Pmt 5 Pixel 37 Slot 13 Fiber 1 Asic 1 Channel 48



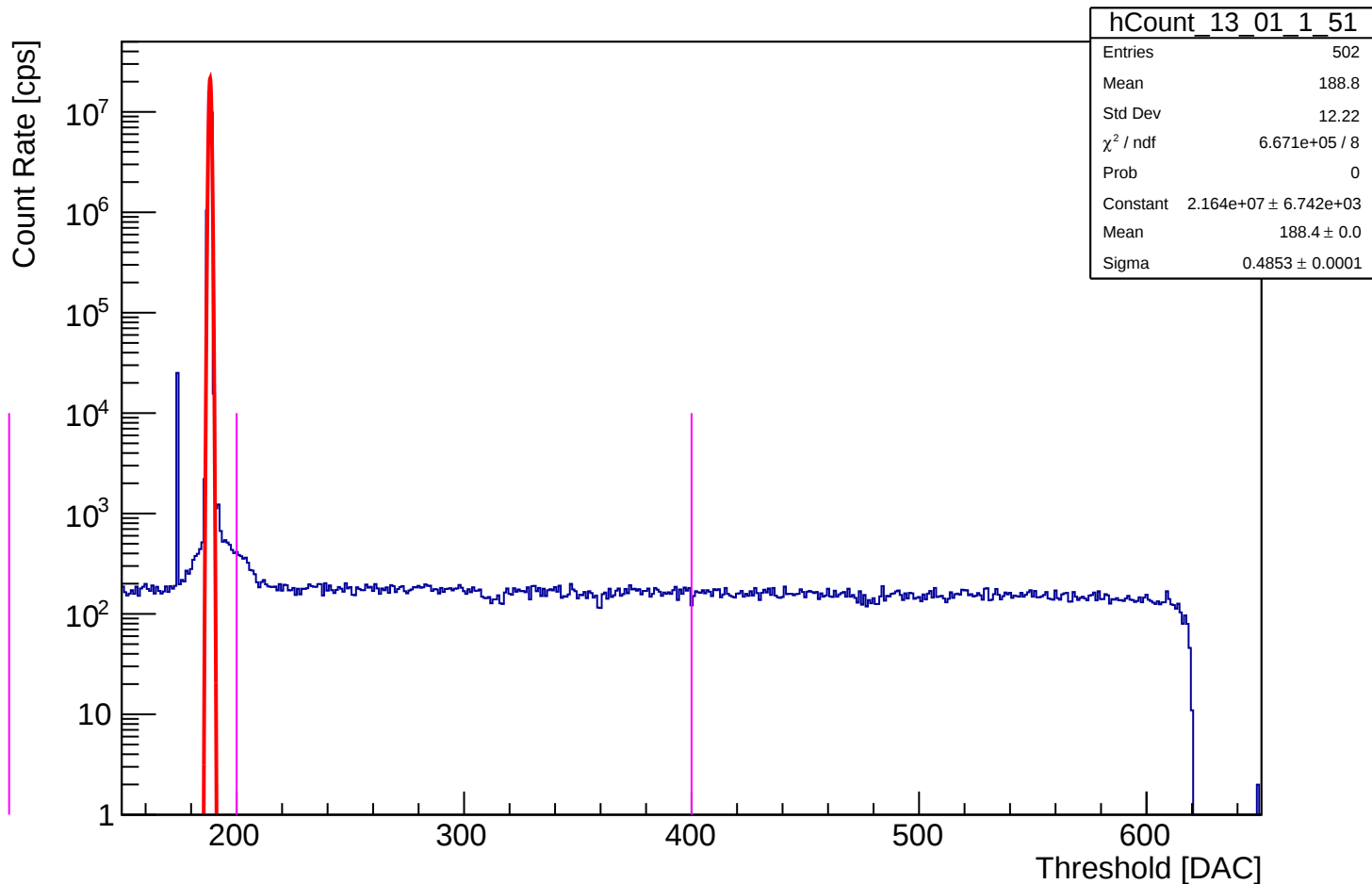
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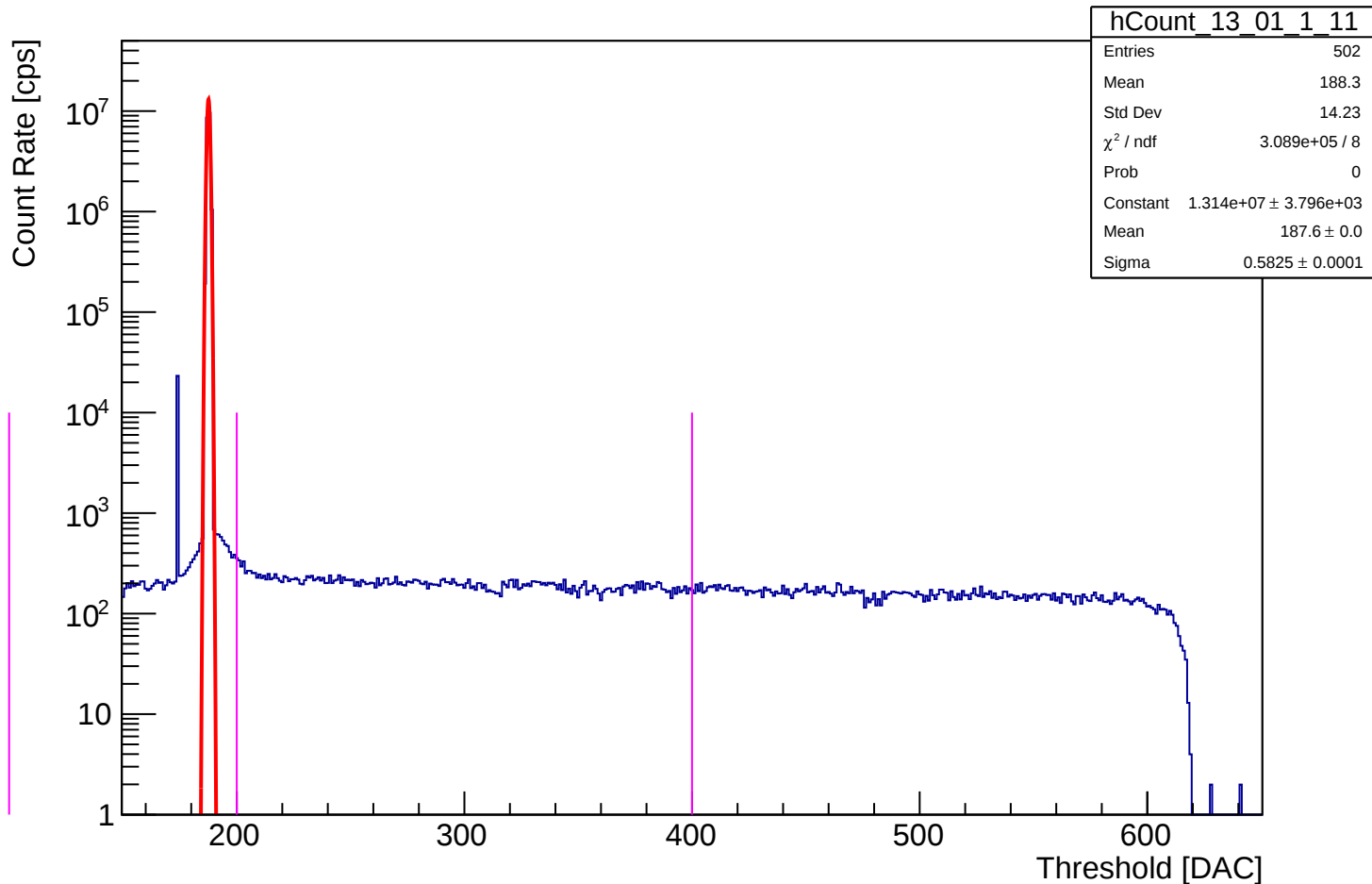
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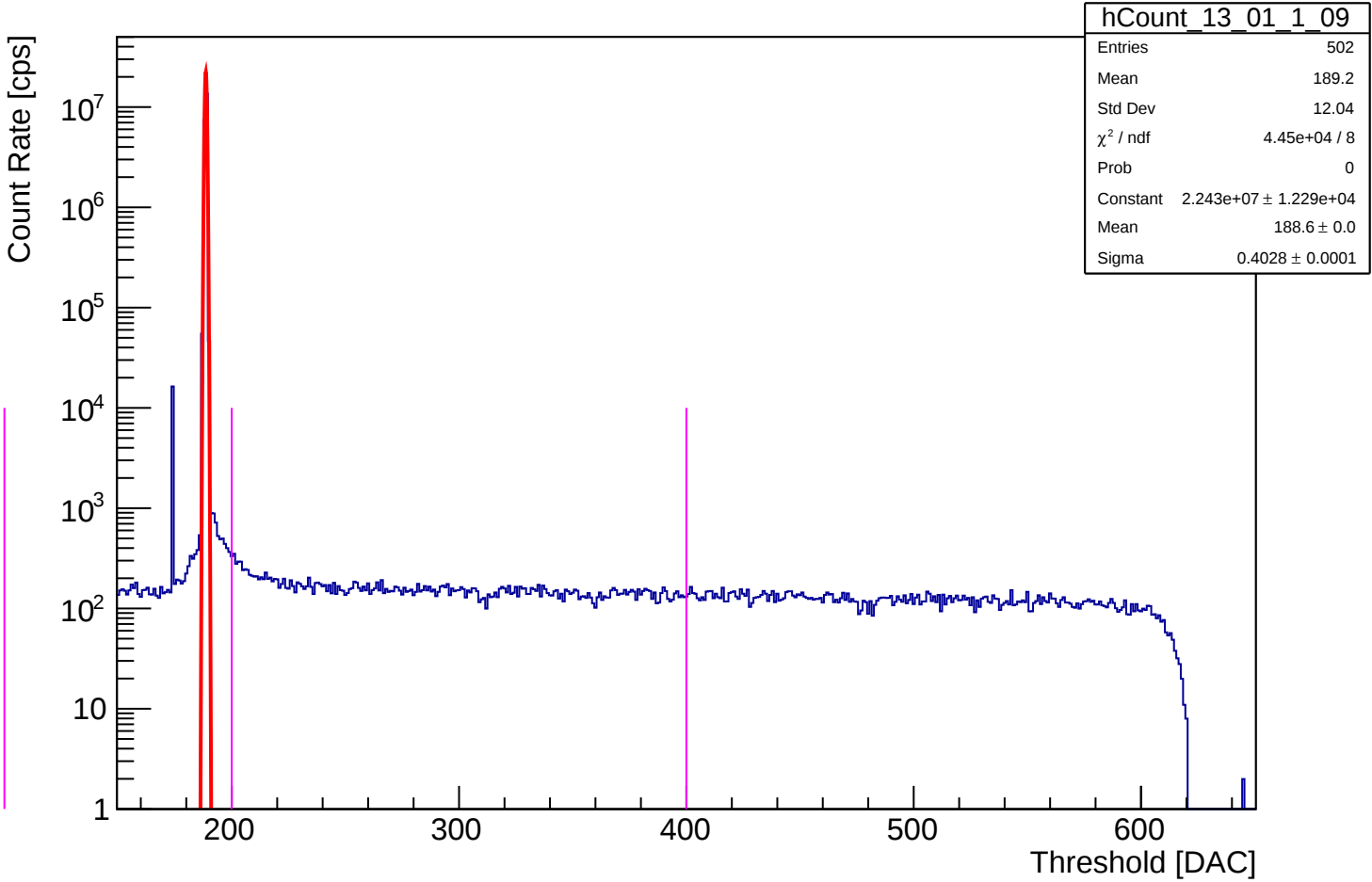


Row 1 Tile 1 Pmt 5 Pixel 40 Slot 13 Fiber 1 Asic 1 Channel 51

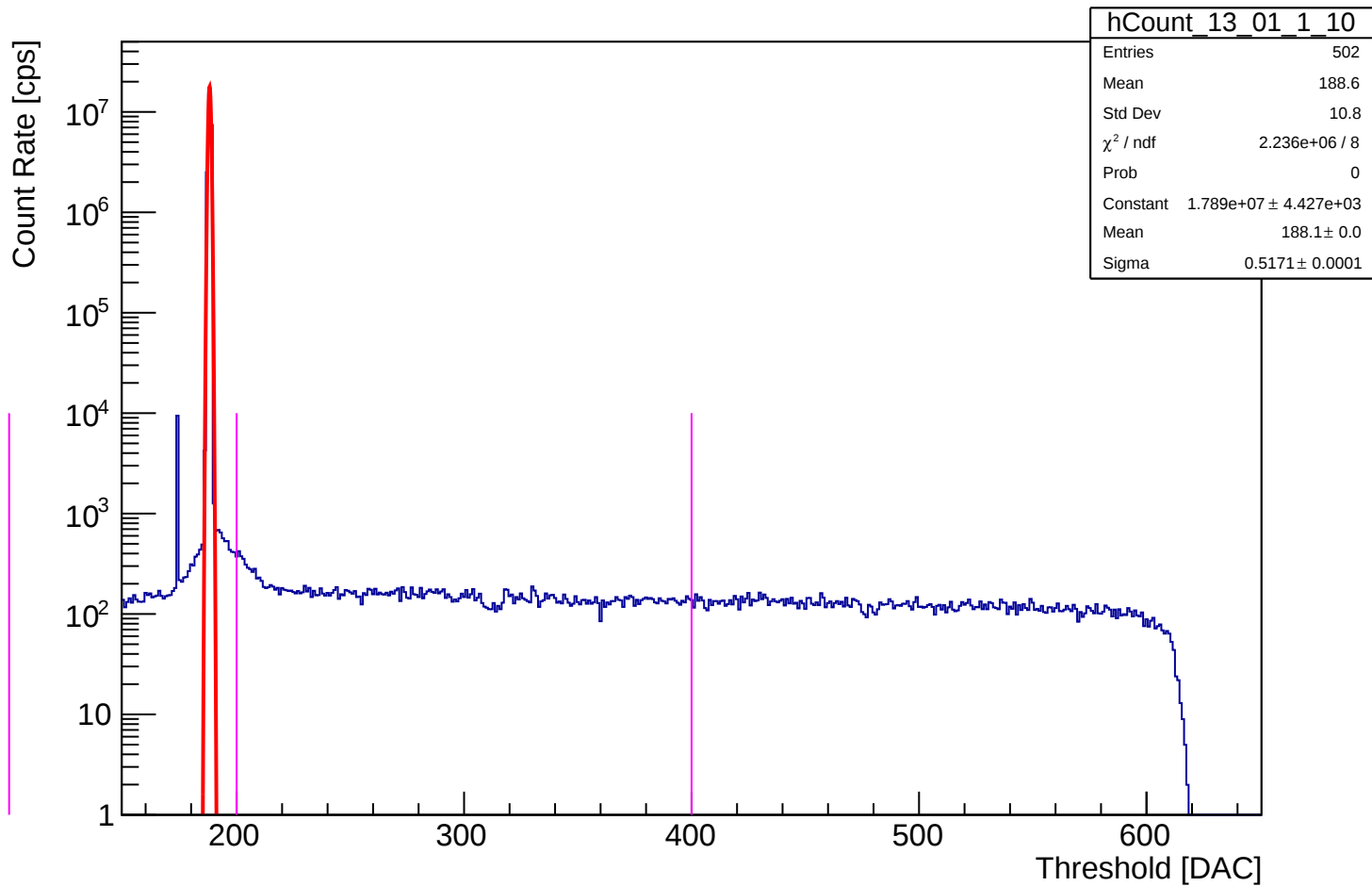


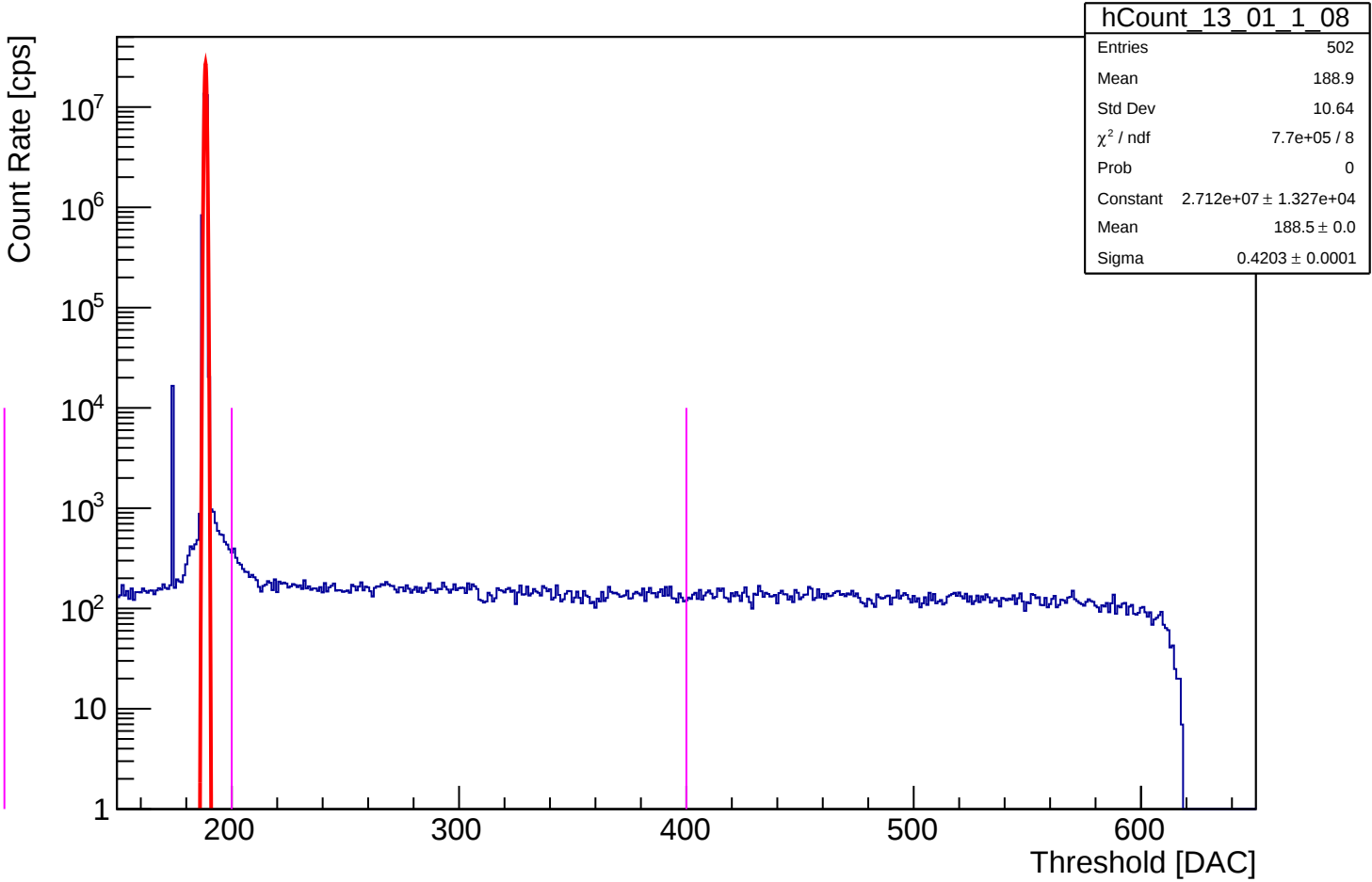
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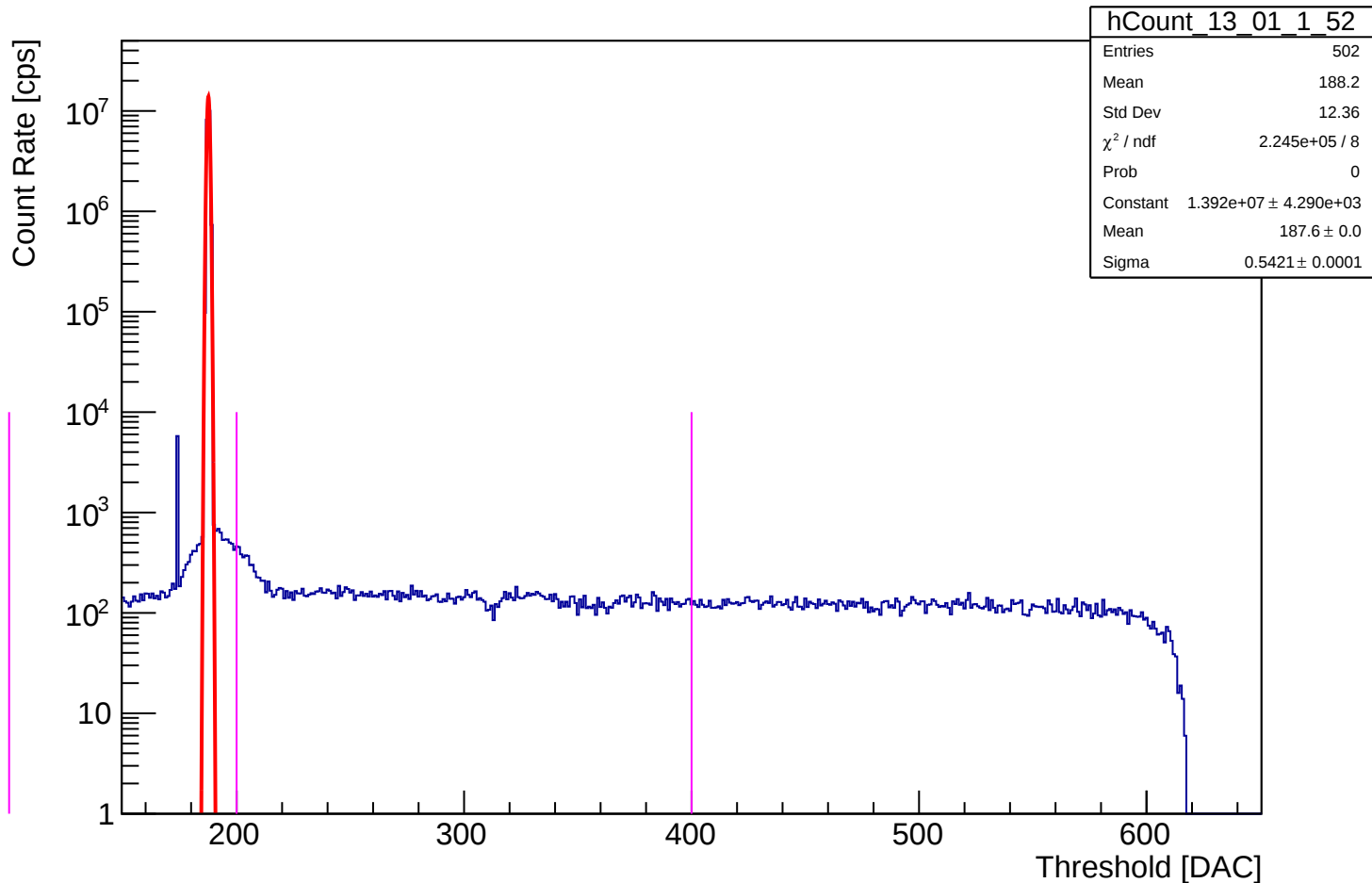


Row 1 Tile 1 Pmt 5 Pixel 43 Slot 13 Fiber 1 Asic 1 Channel 10

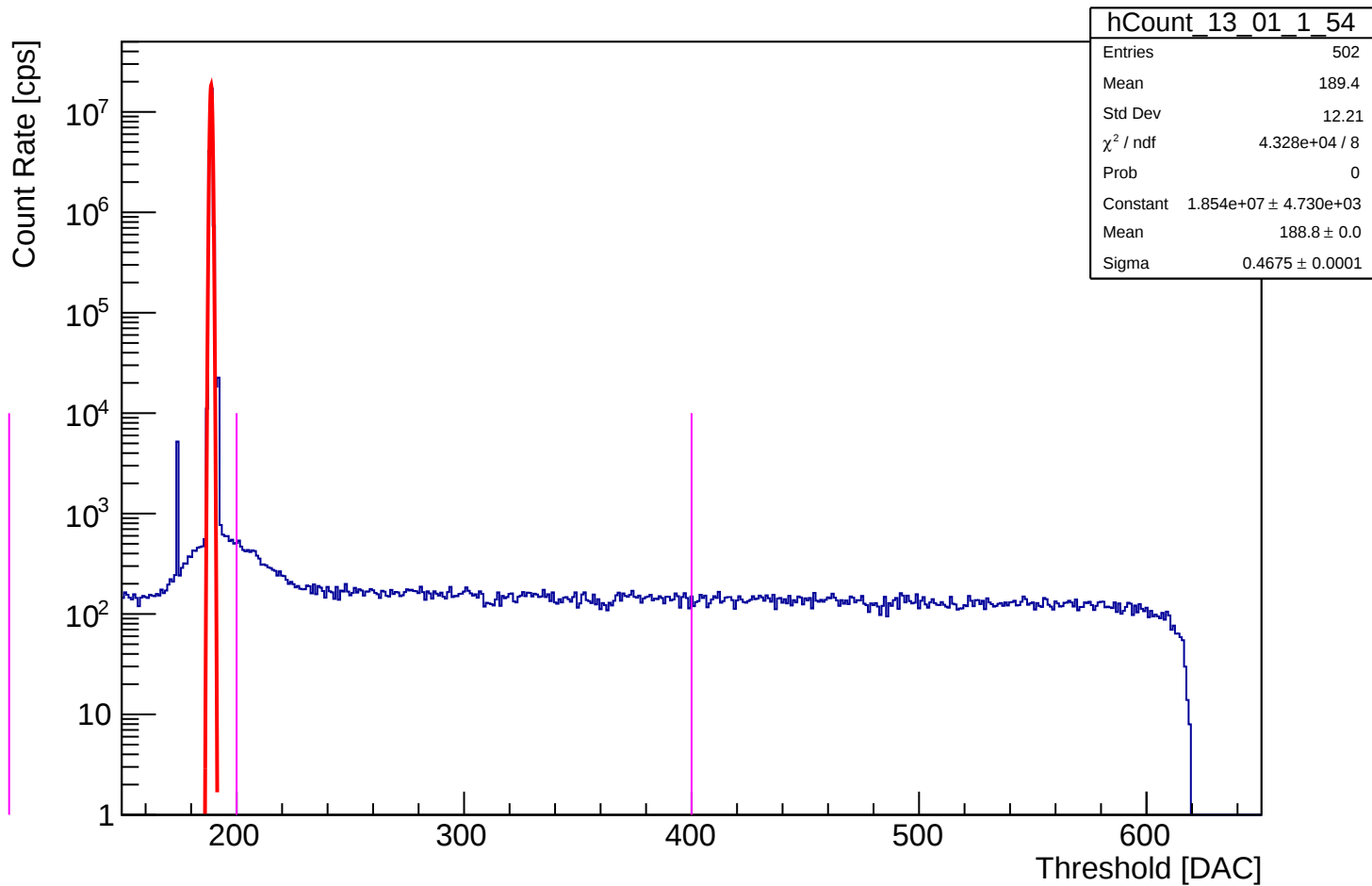




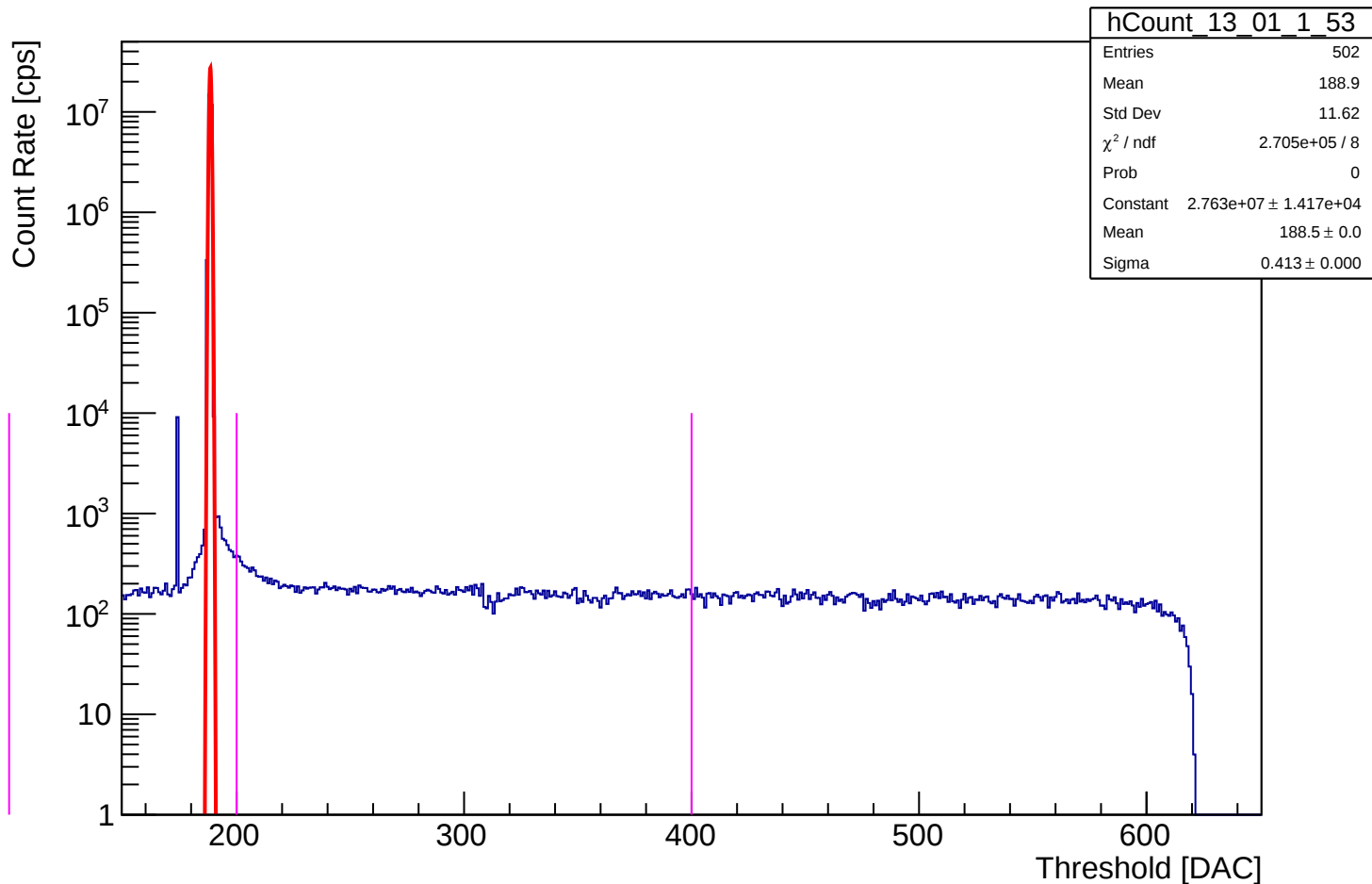
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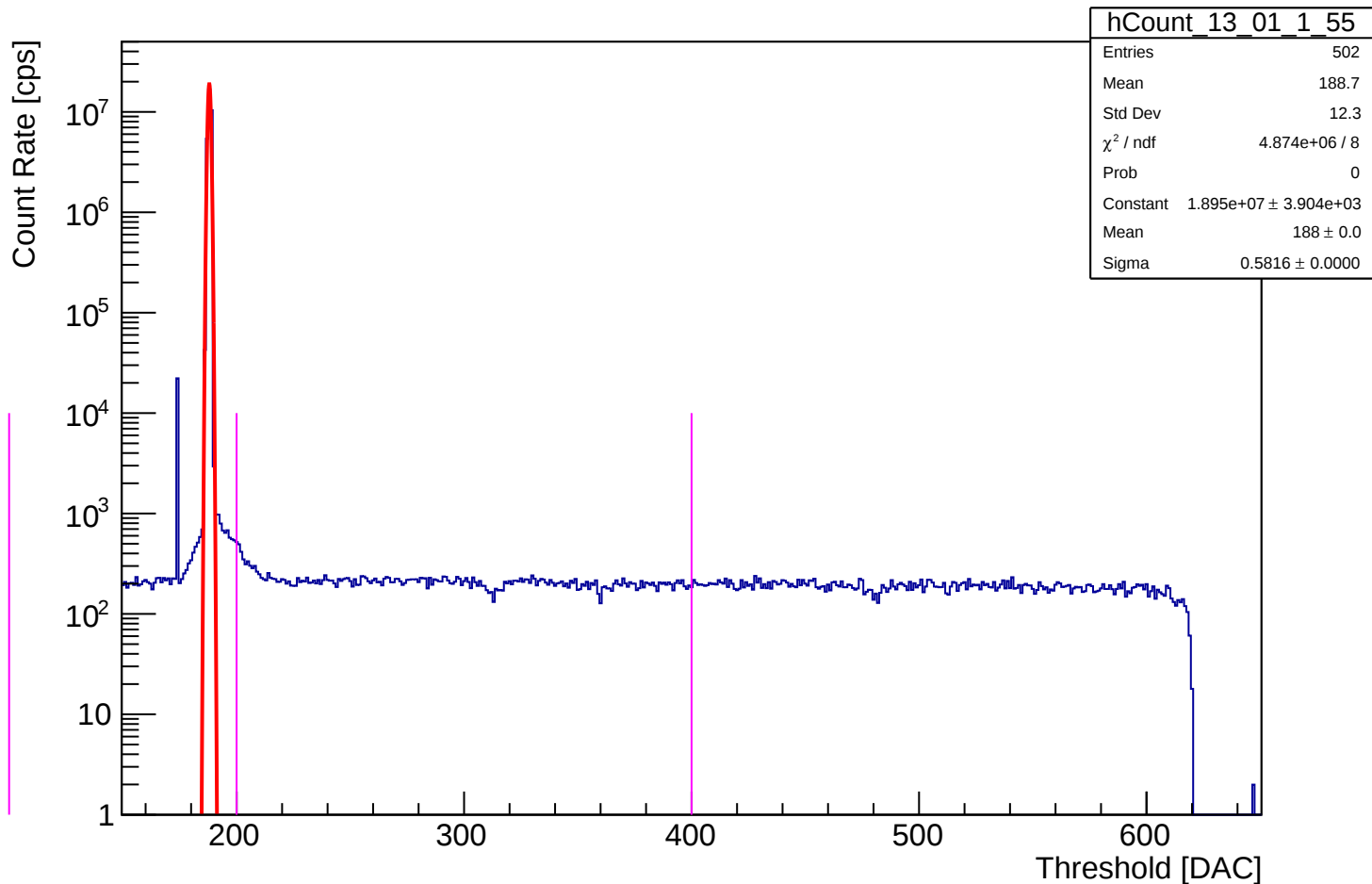
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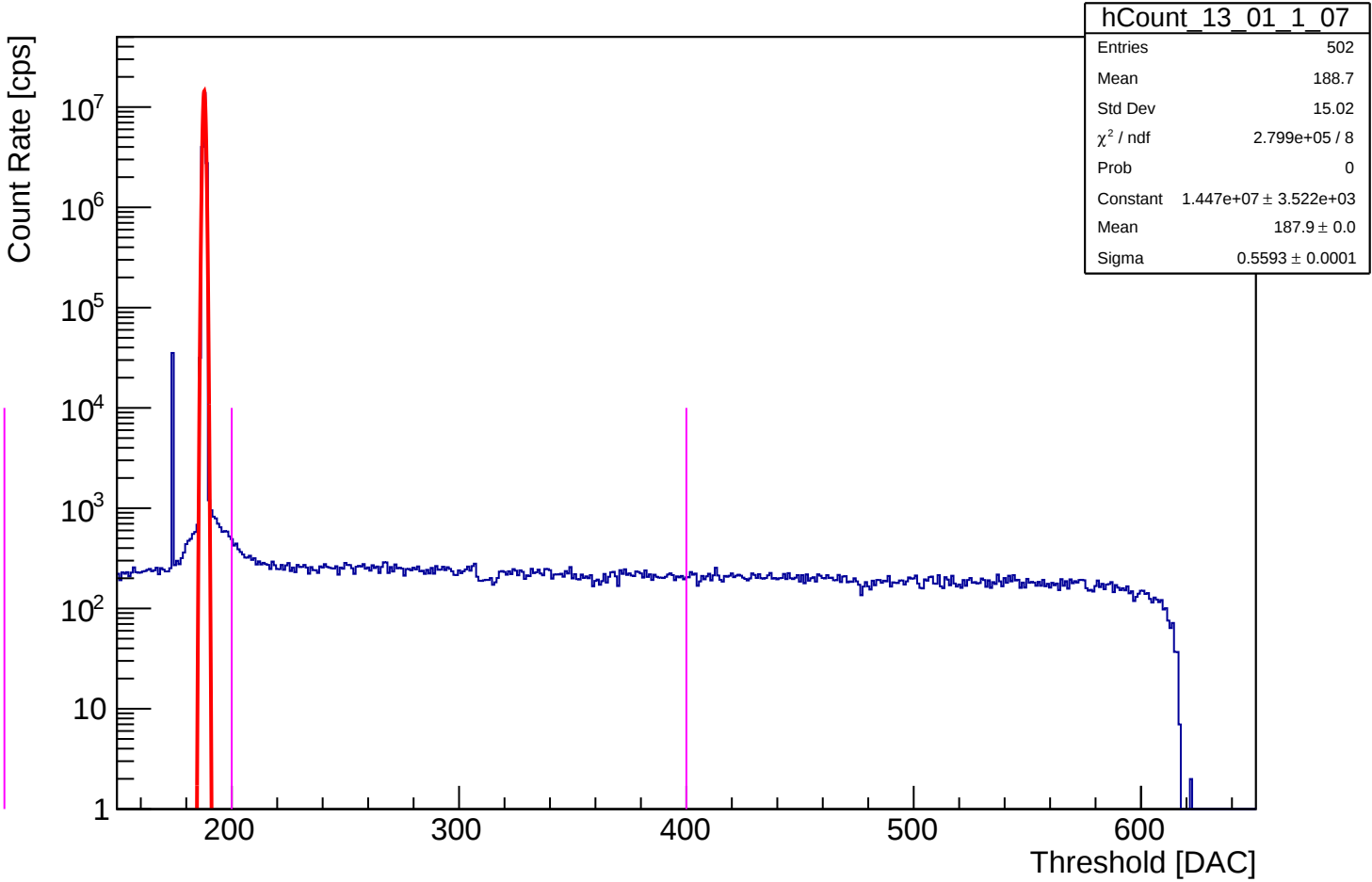


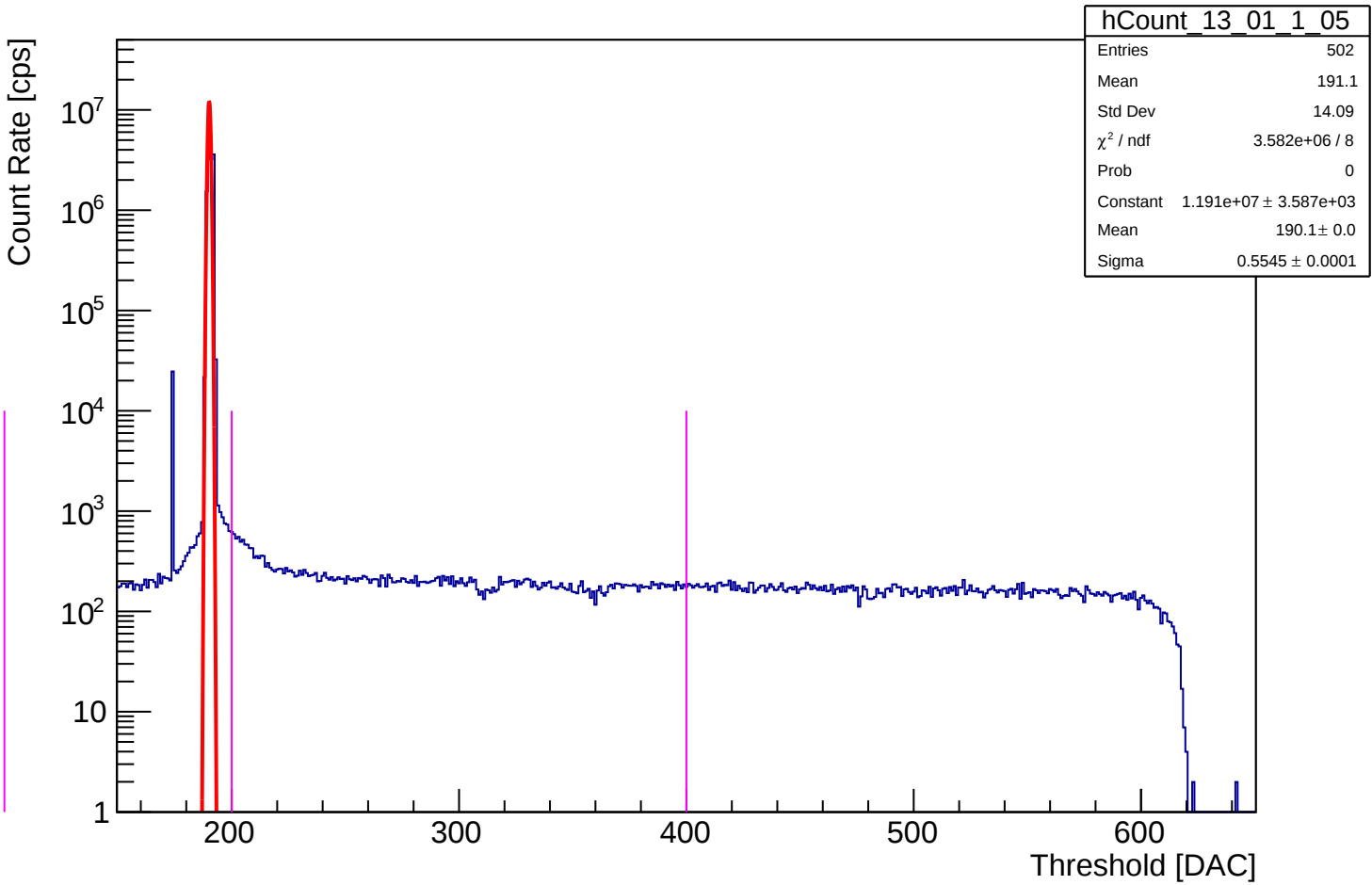
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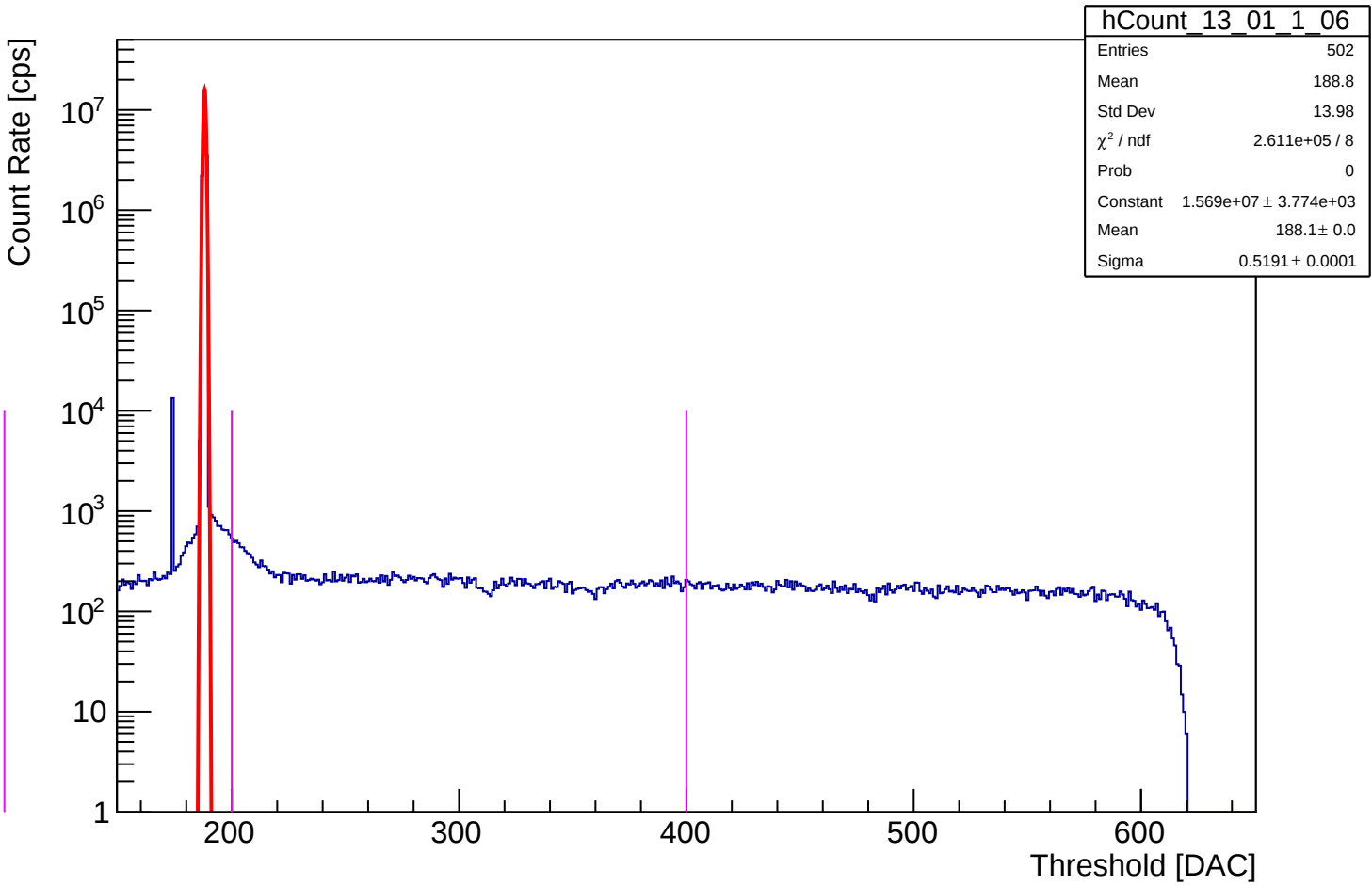


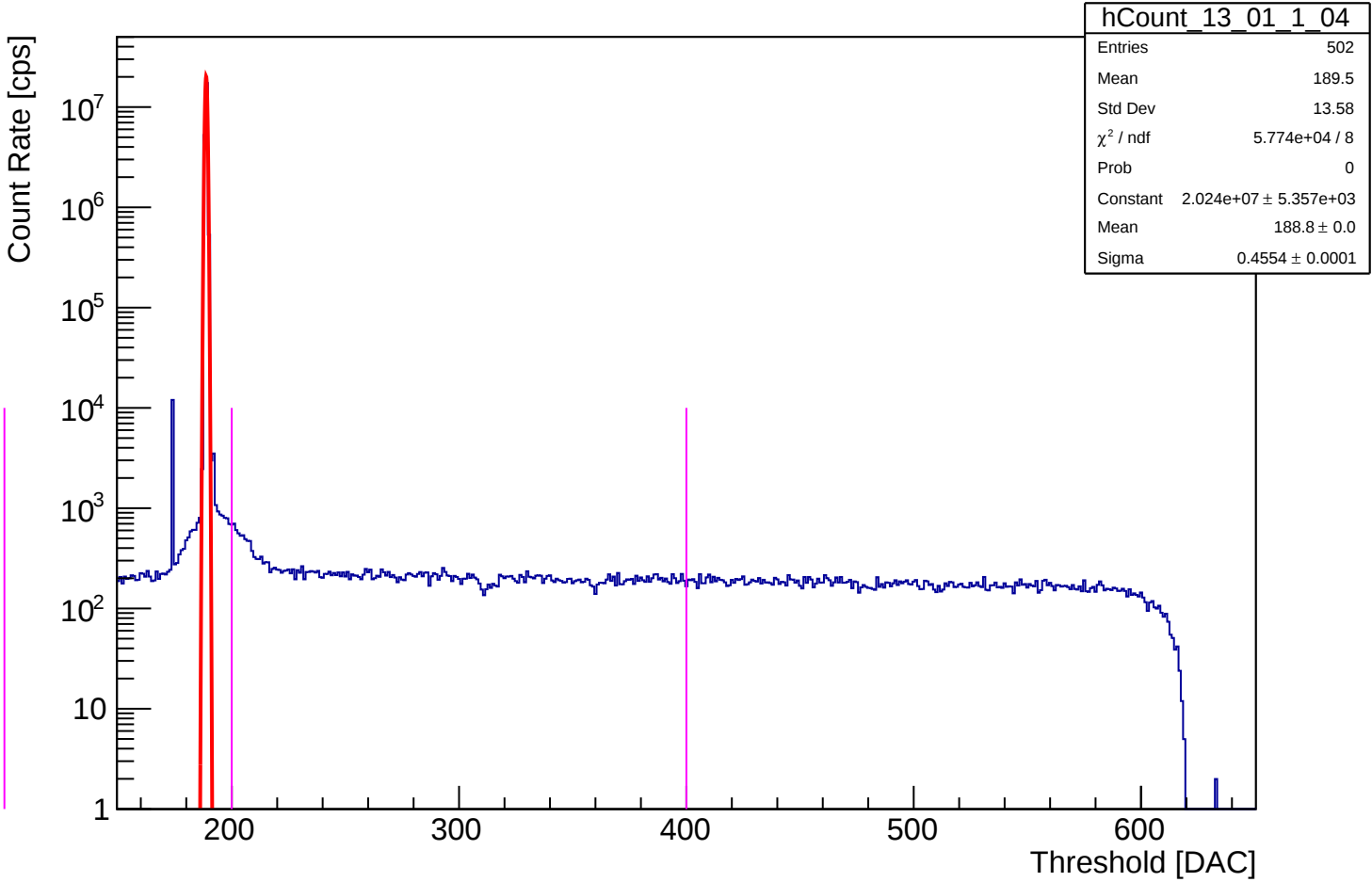
Row 1 Tile 1 Pmt 5 Pixel 48 Slot 13 Fiber 1 Asic 1 Channel 55



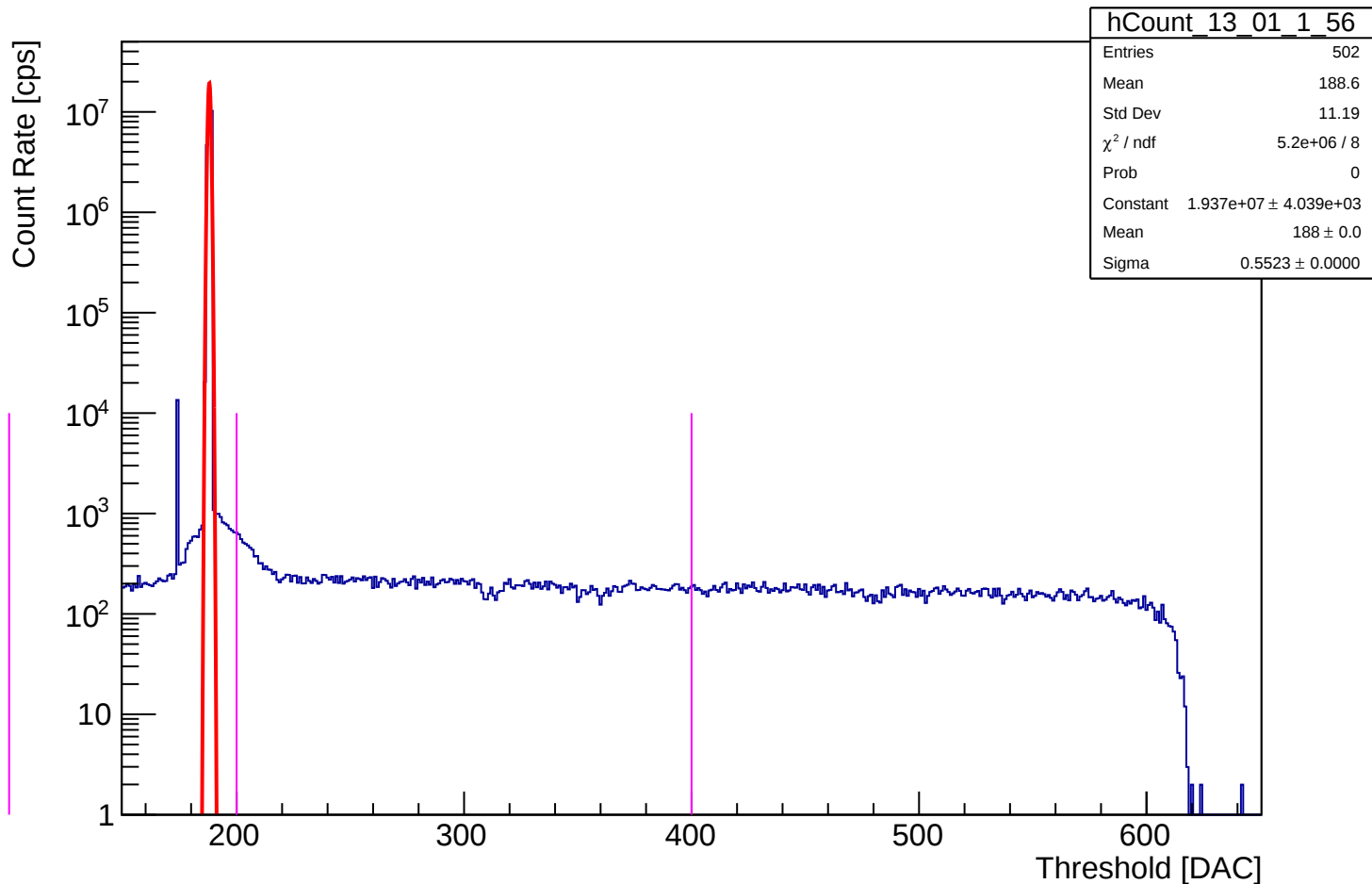




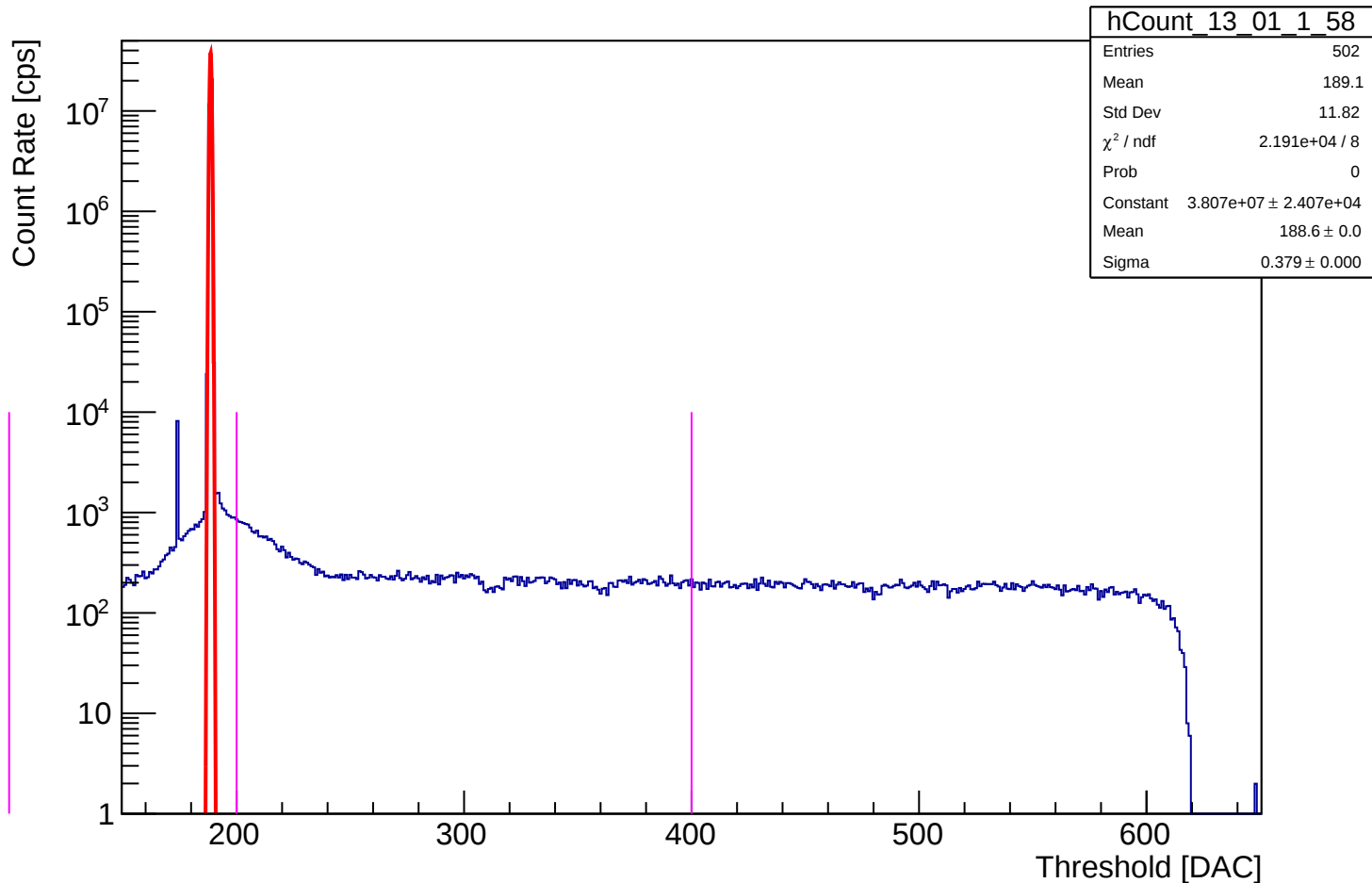




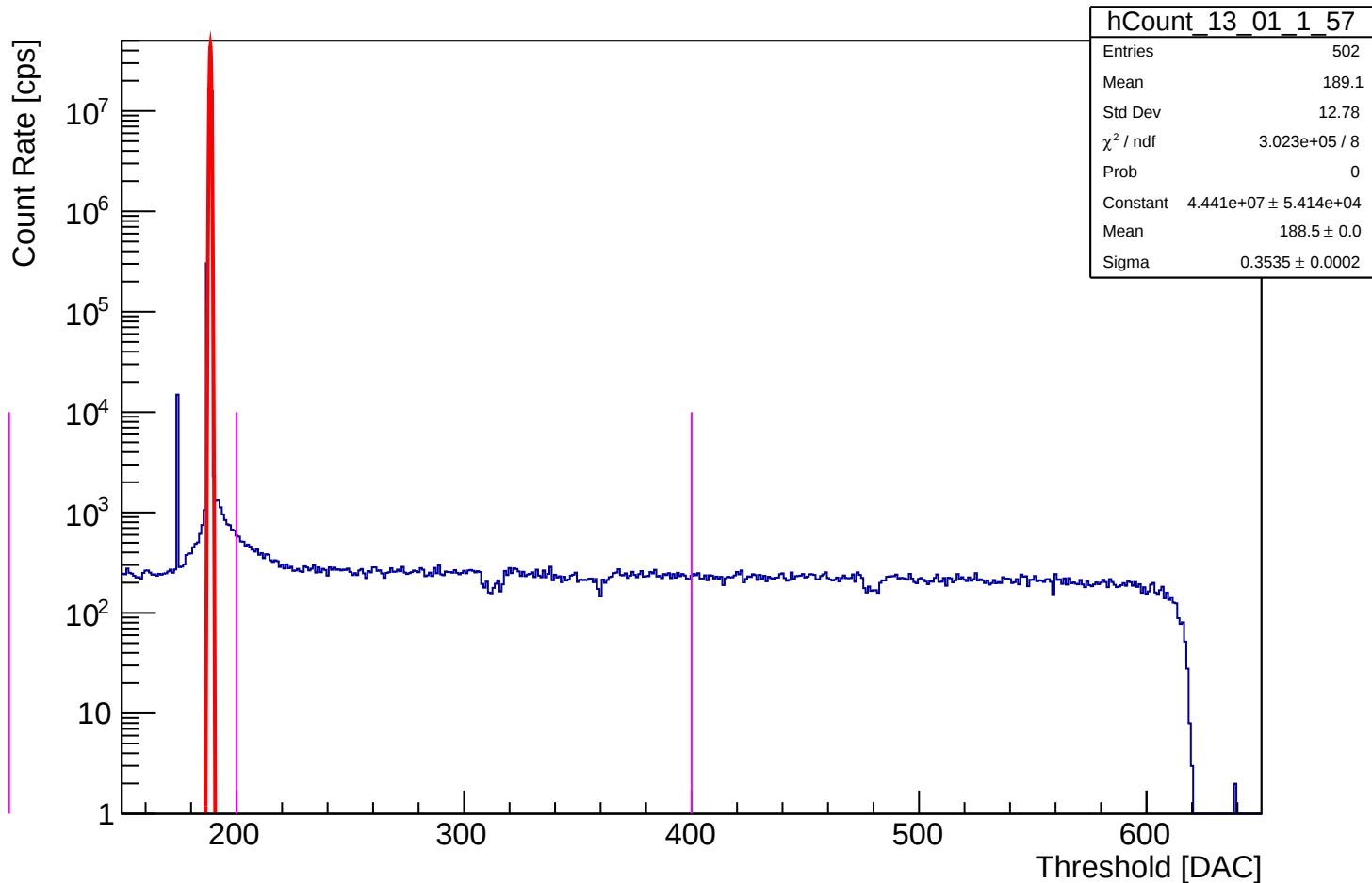
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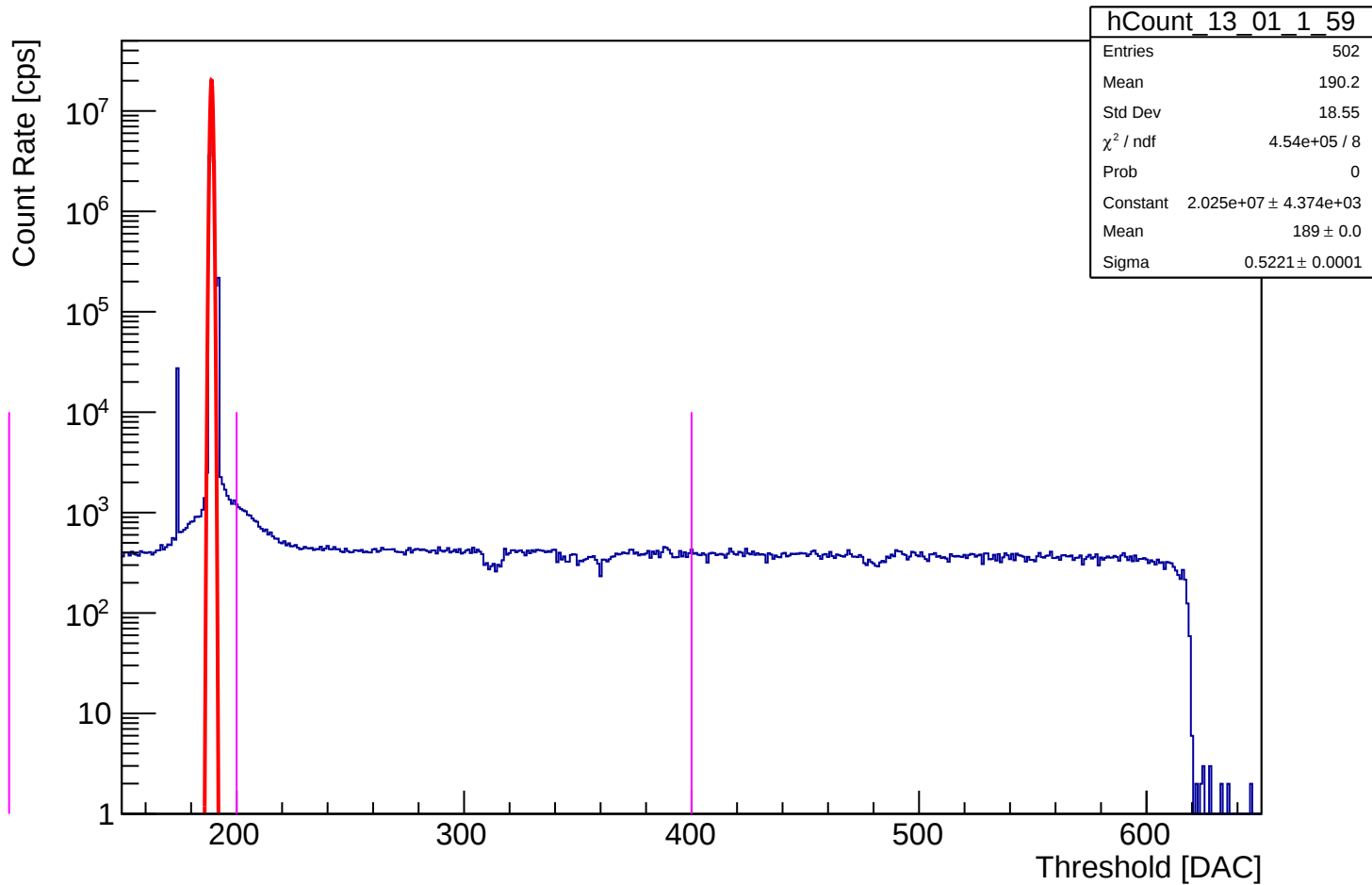
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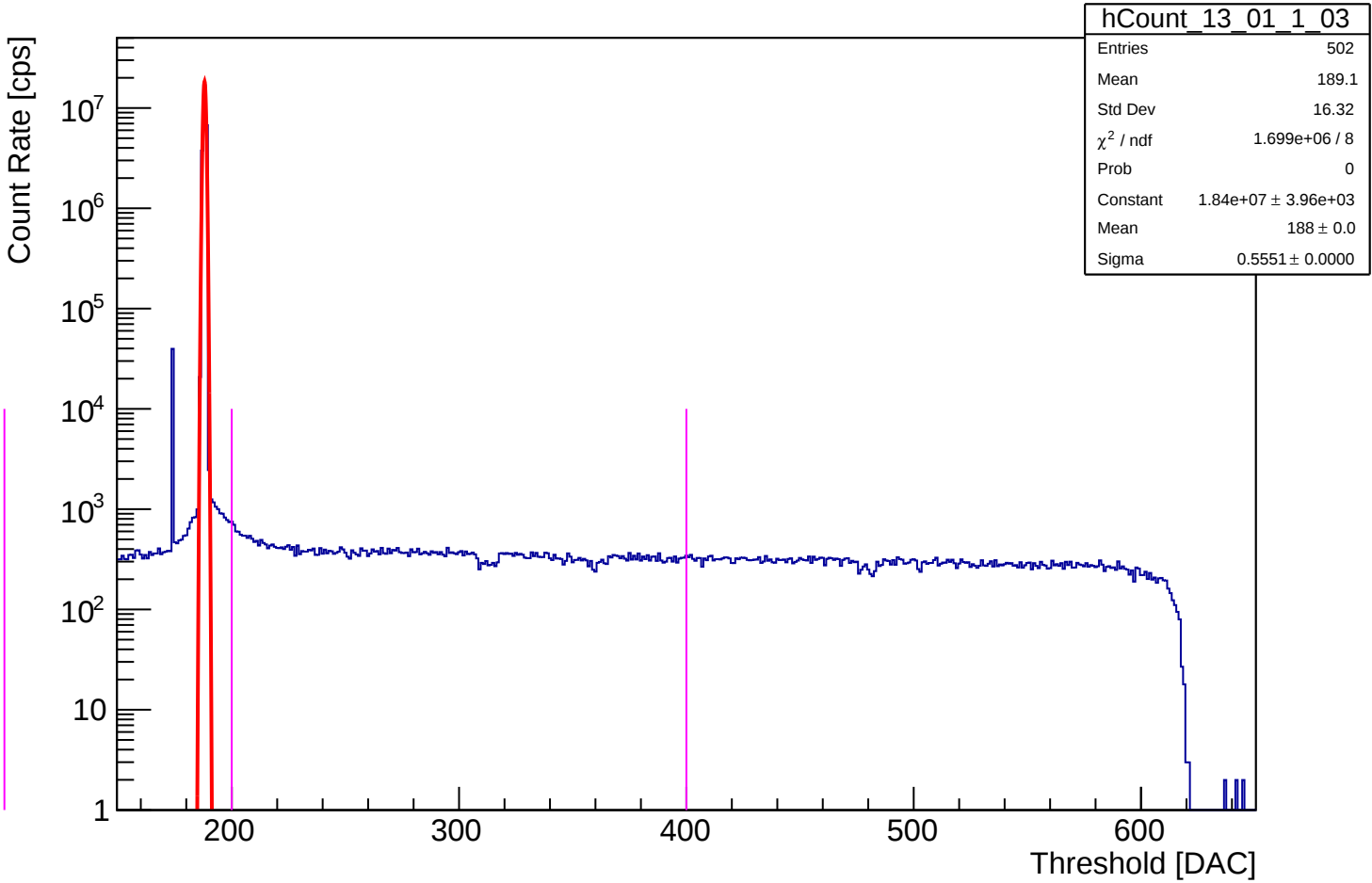


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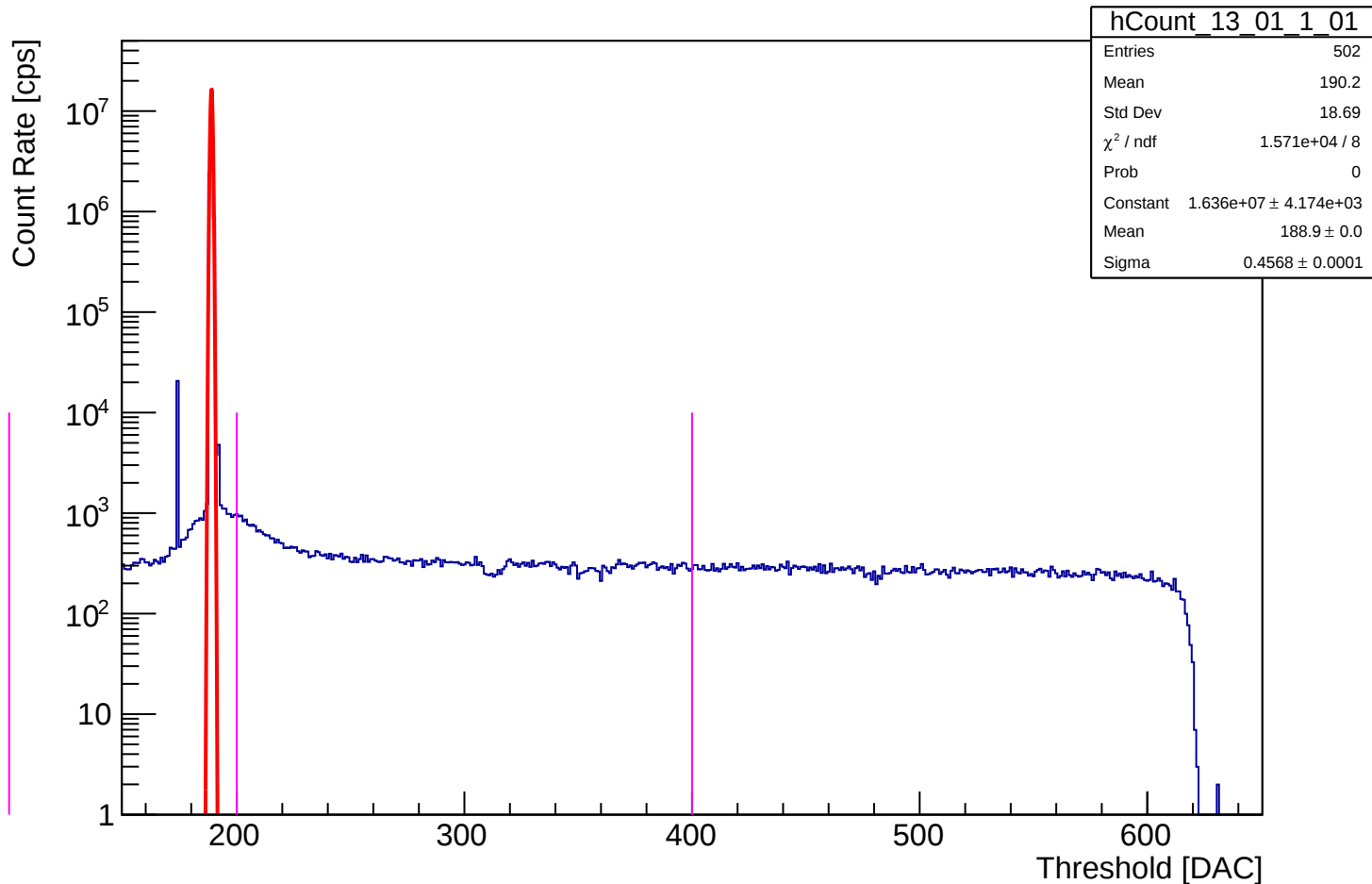


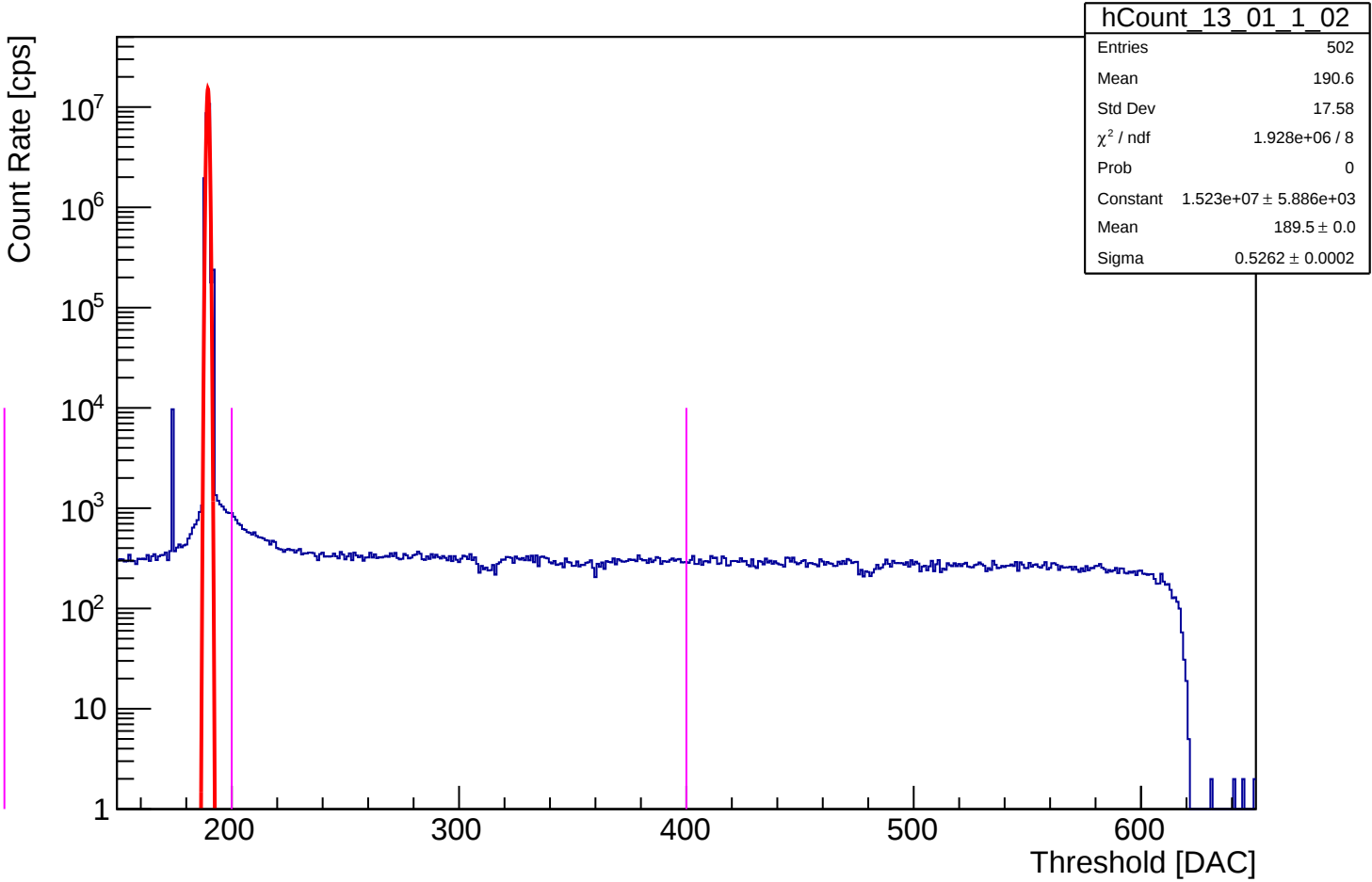
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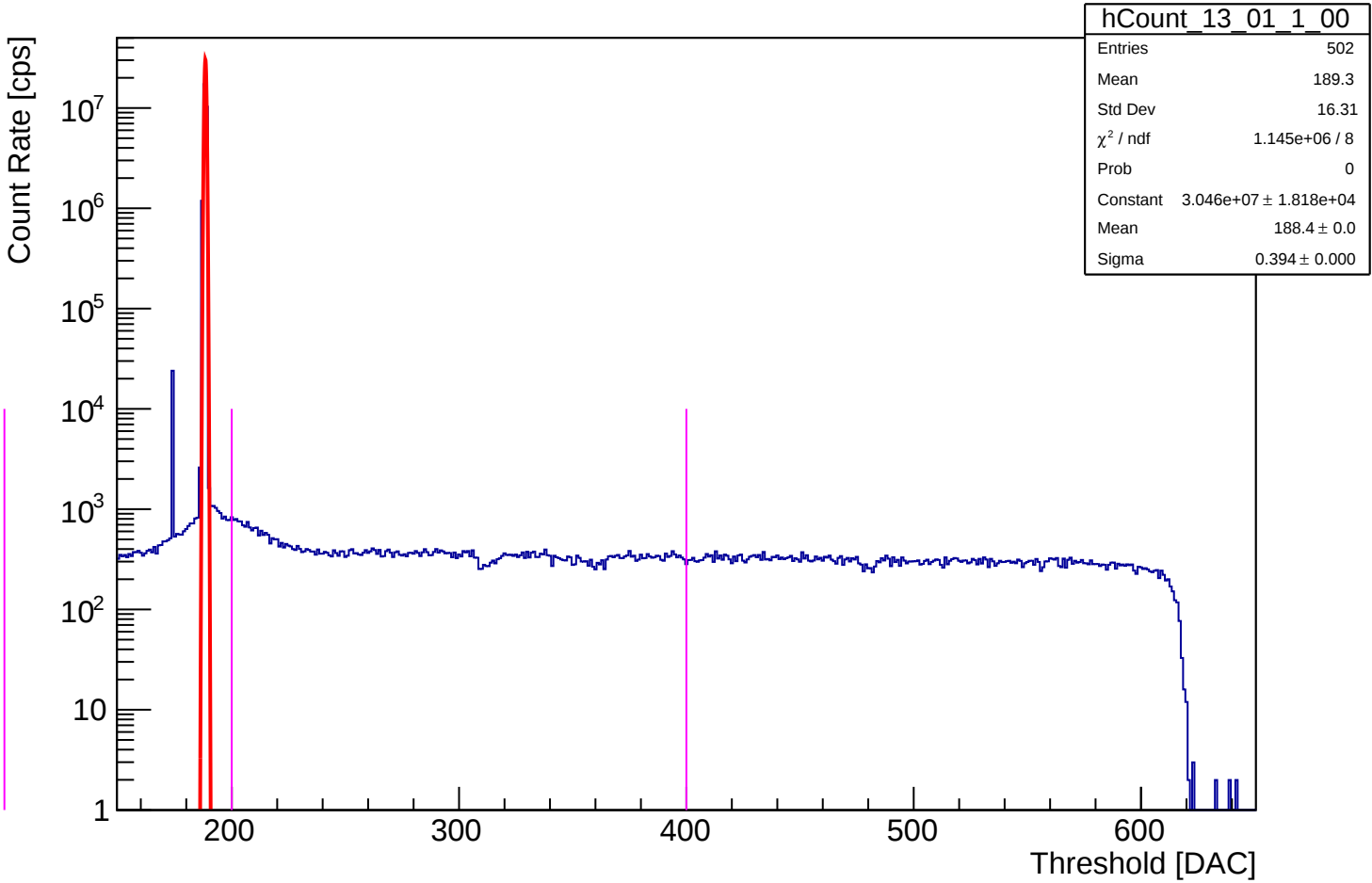




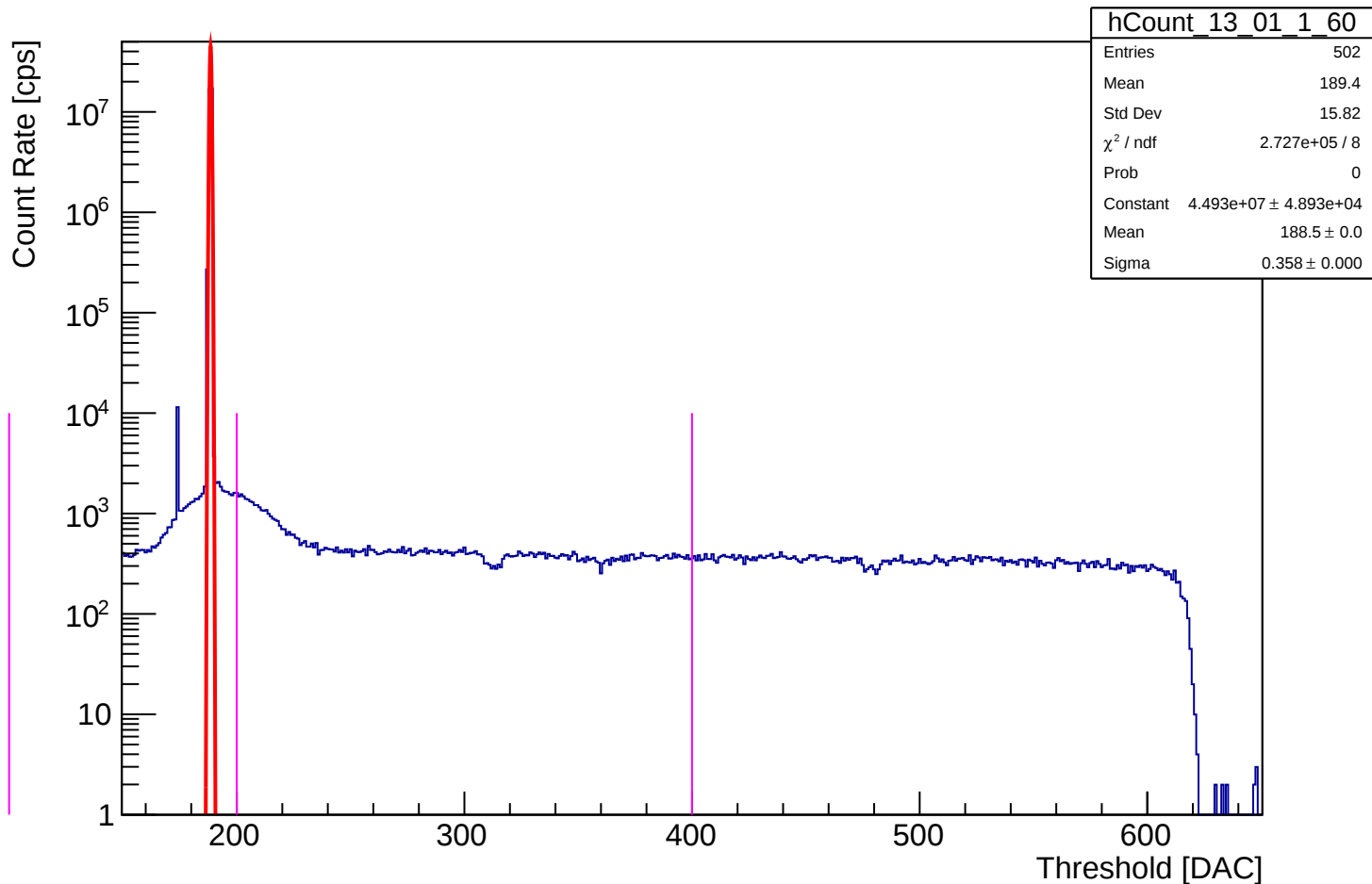
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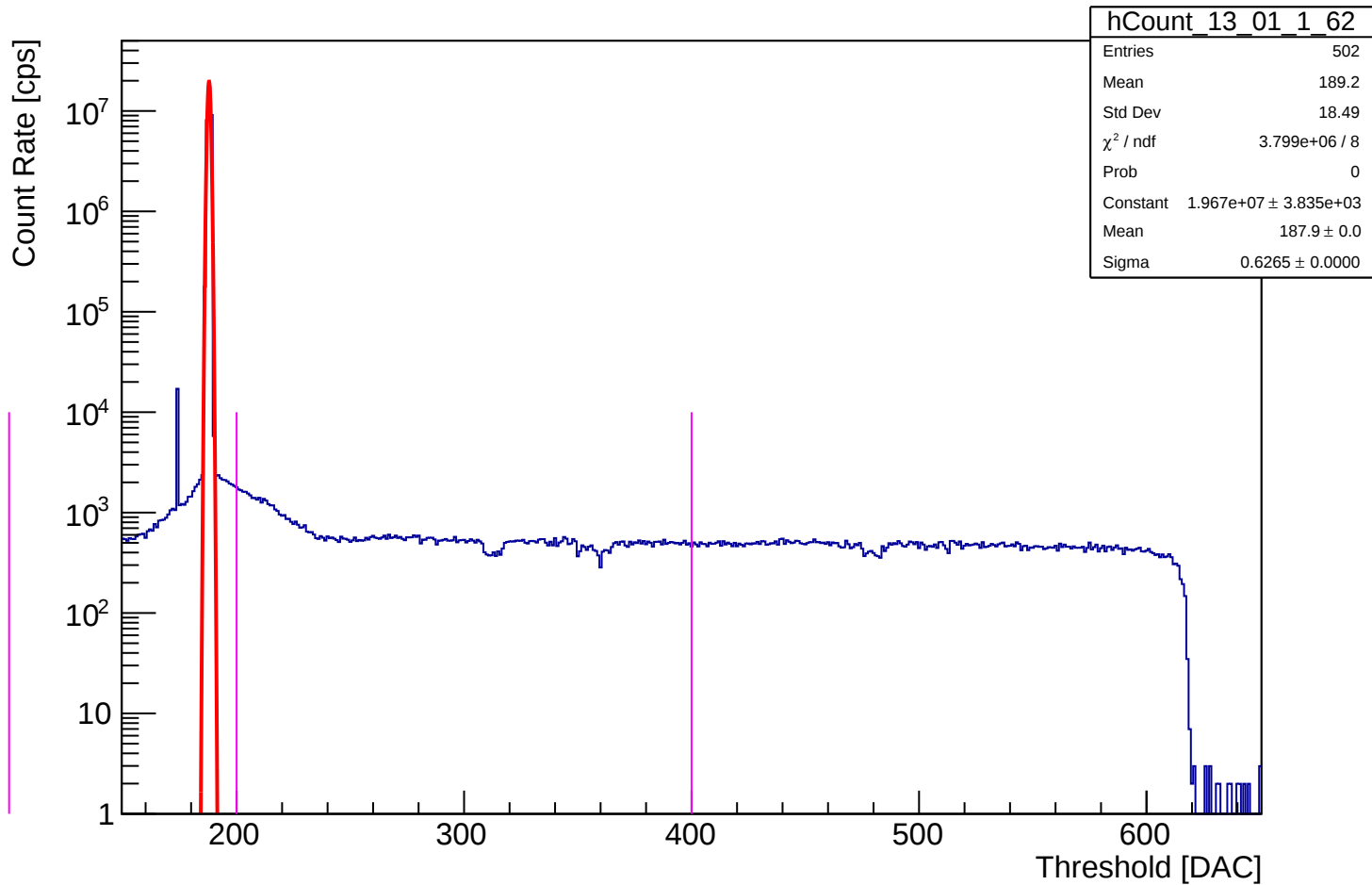




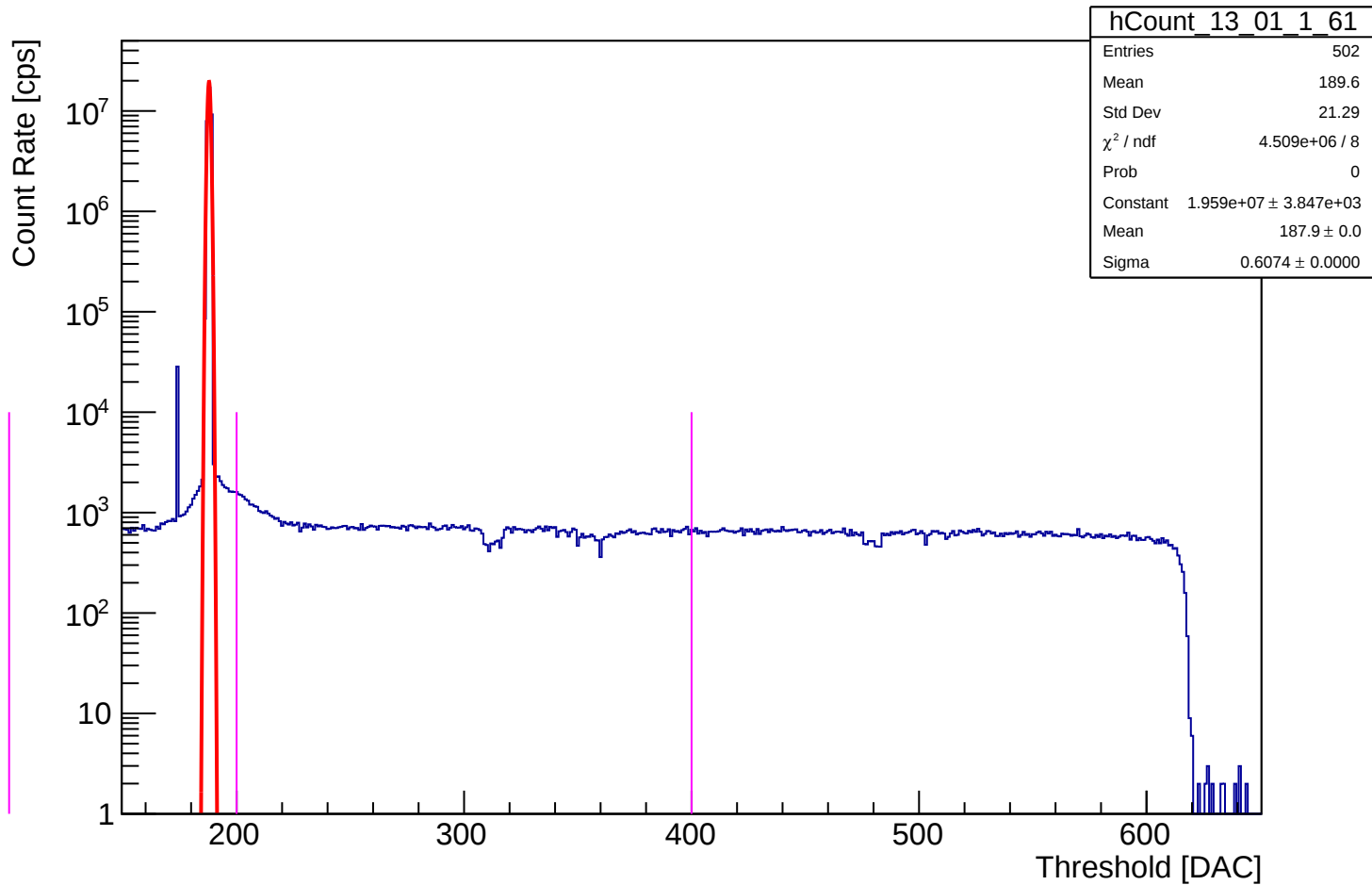
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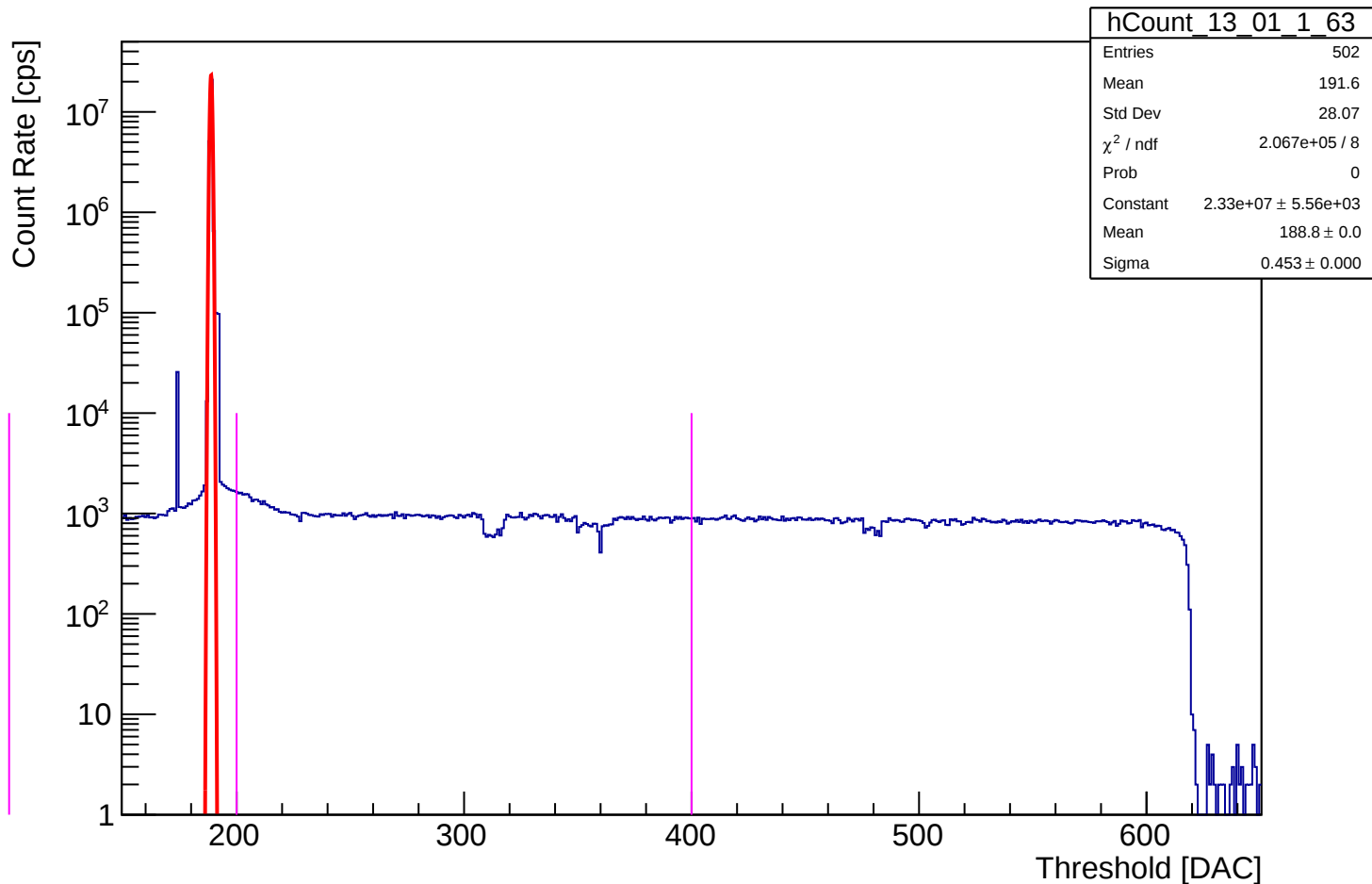
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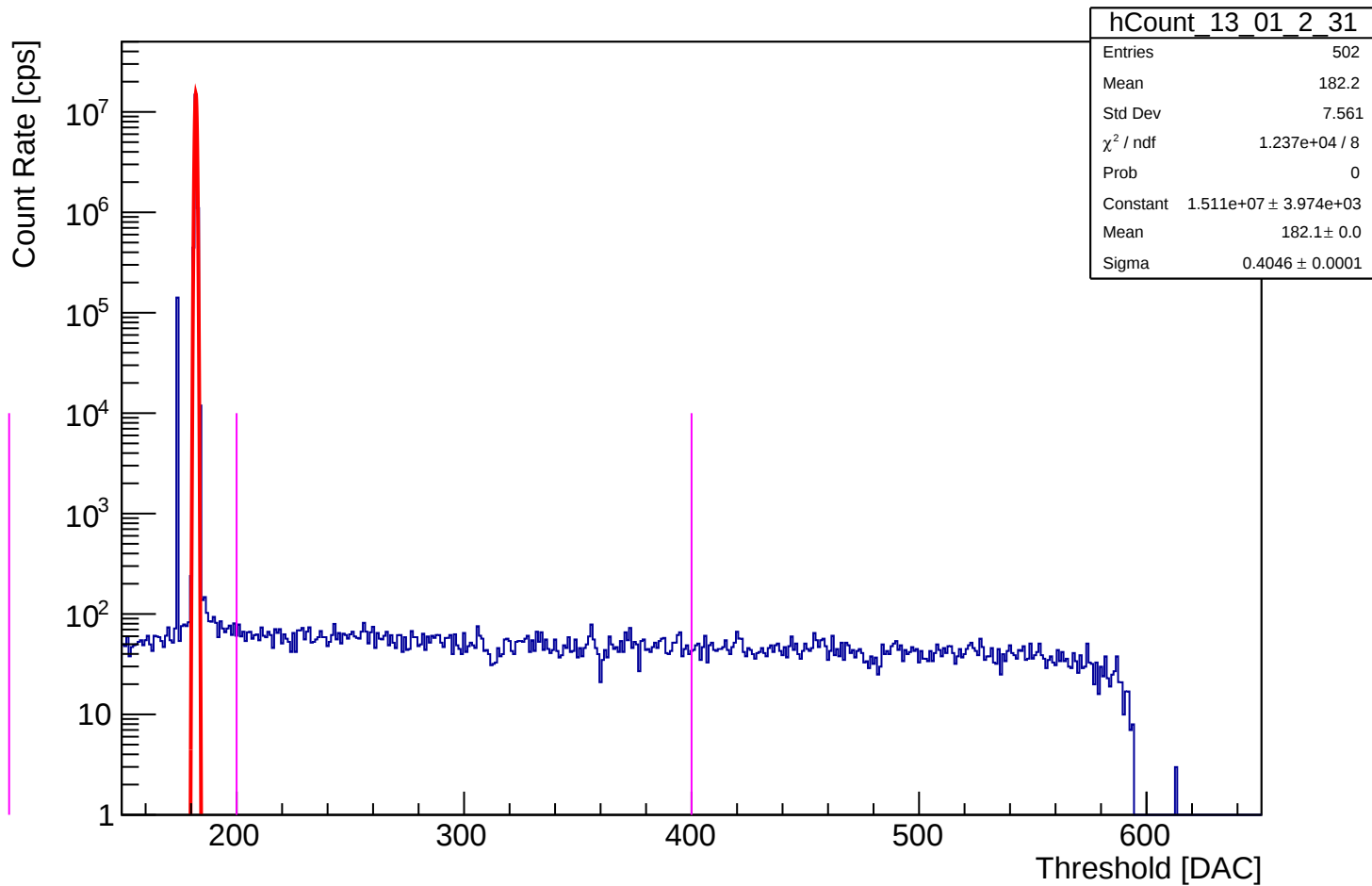
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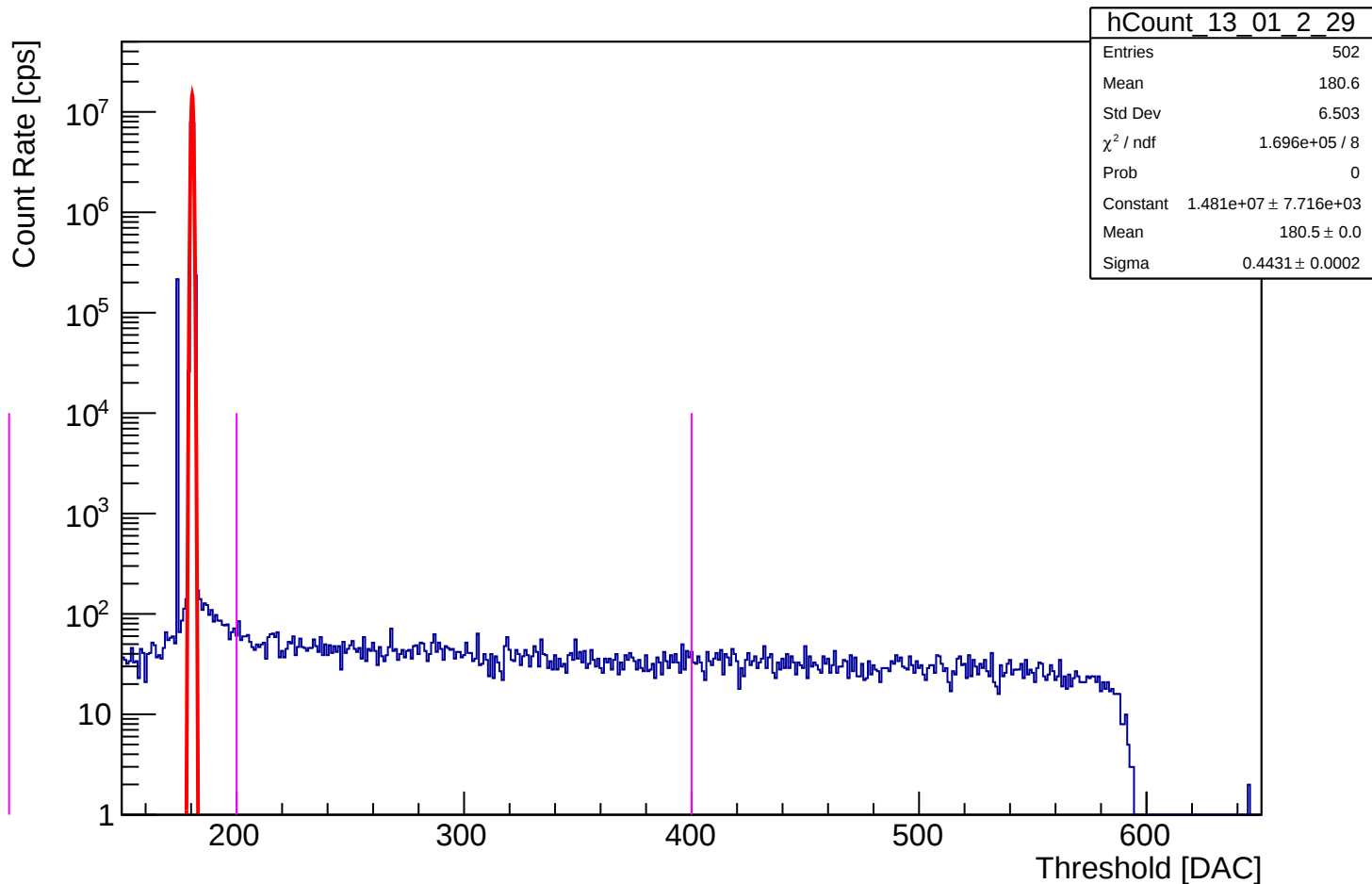
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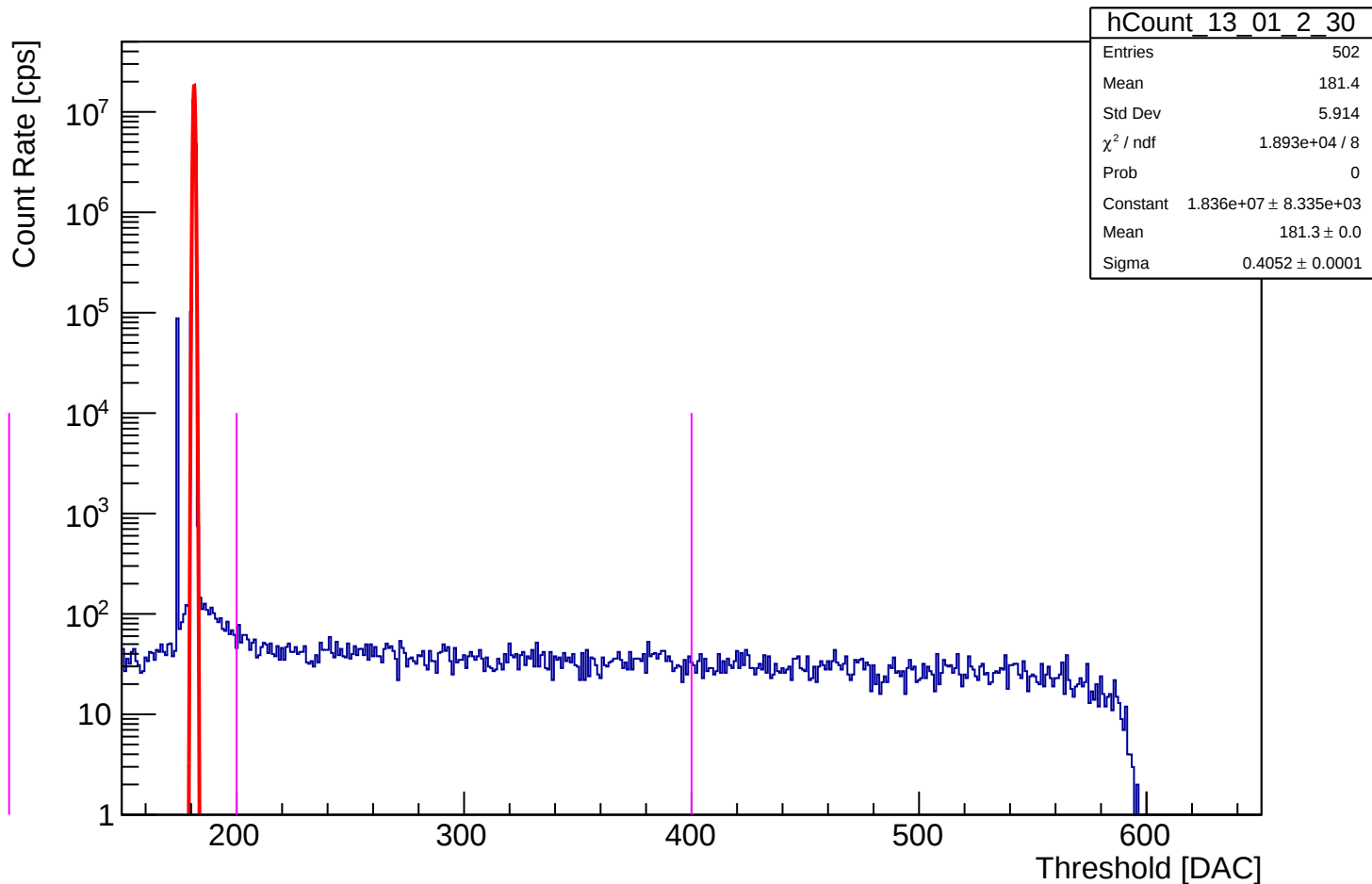
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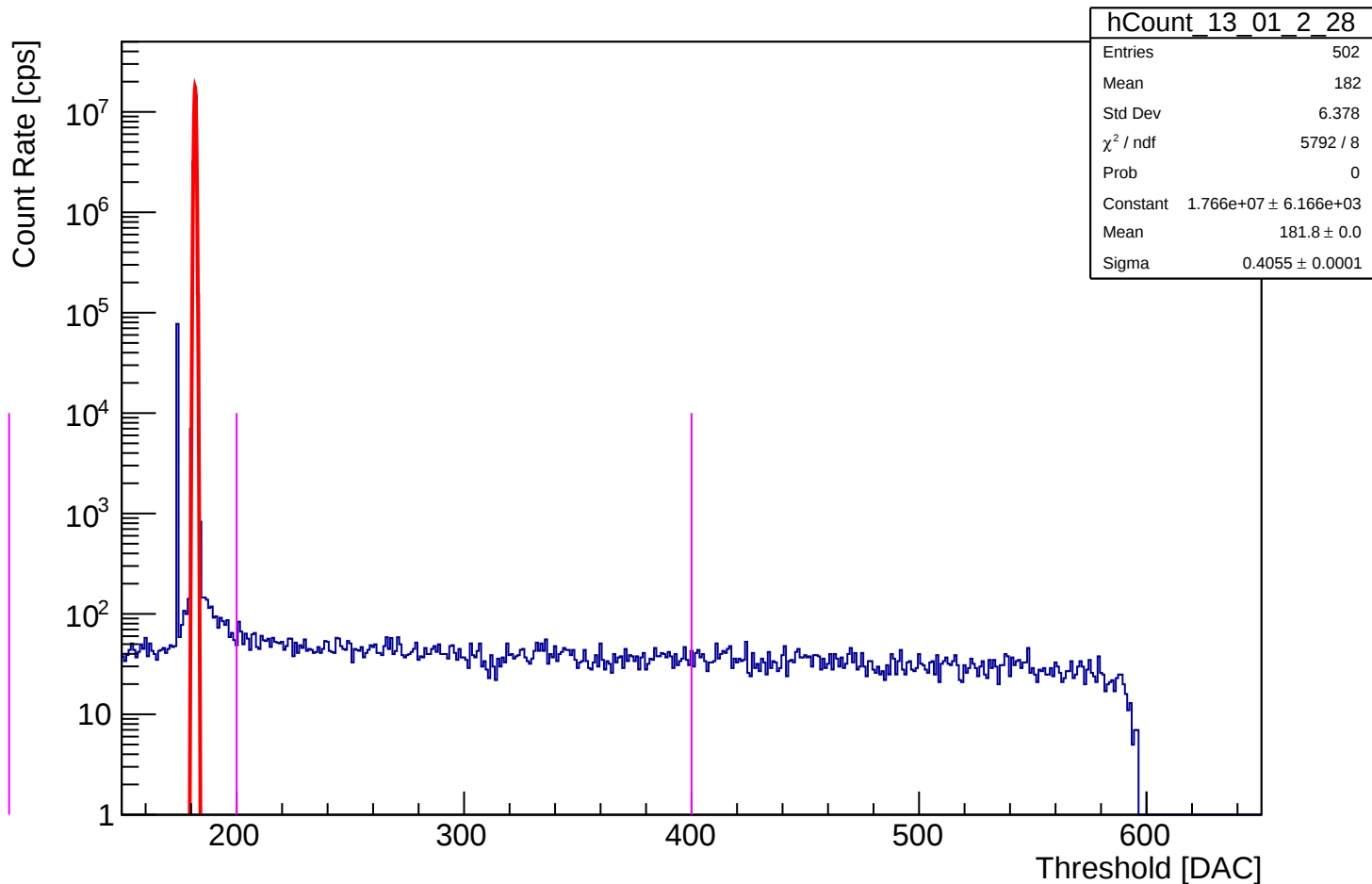
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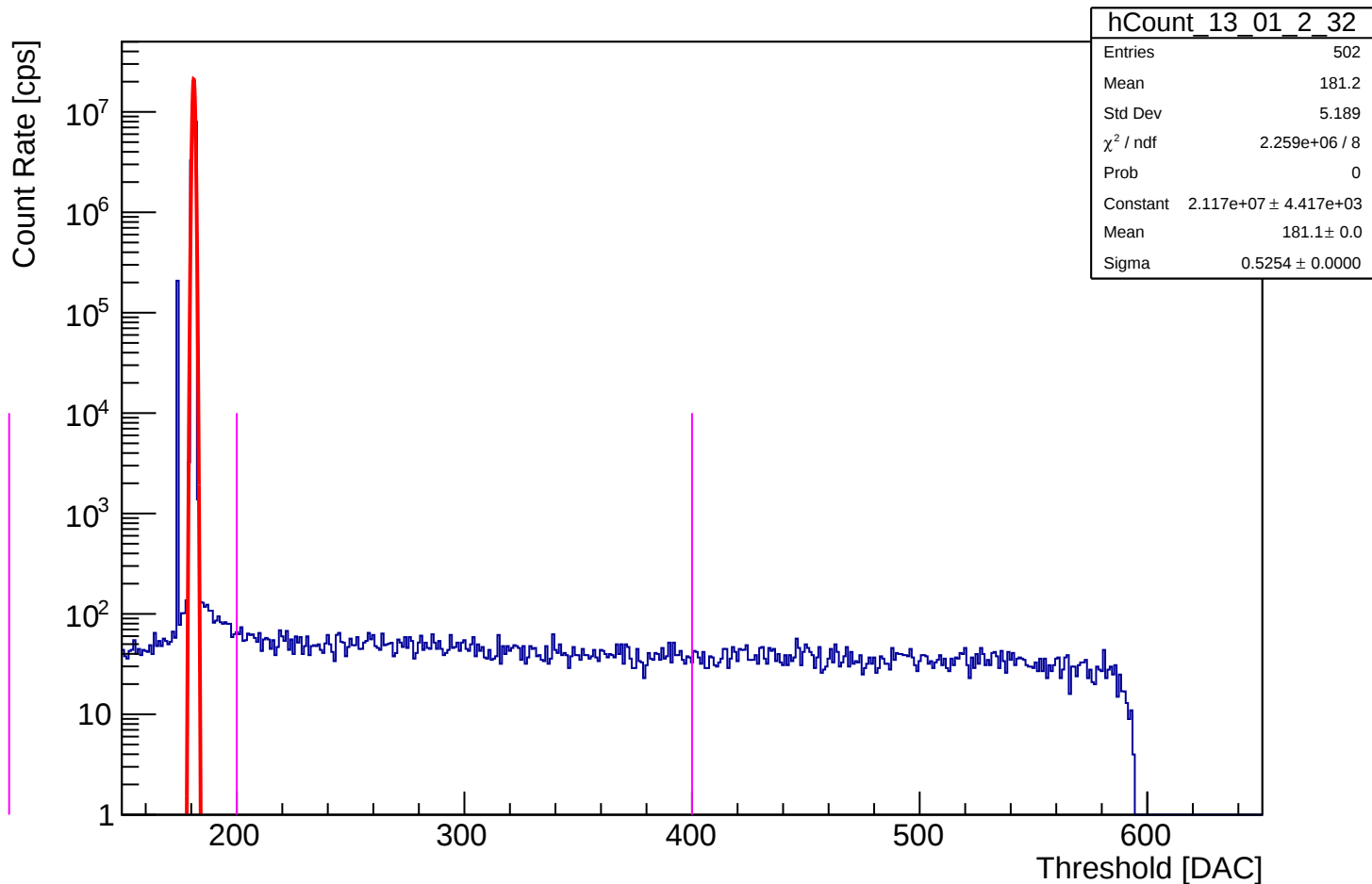
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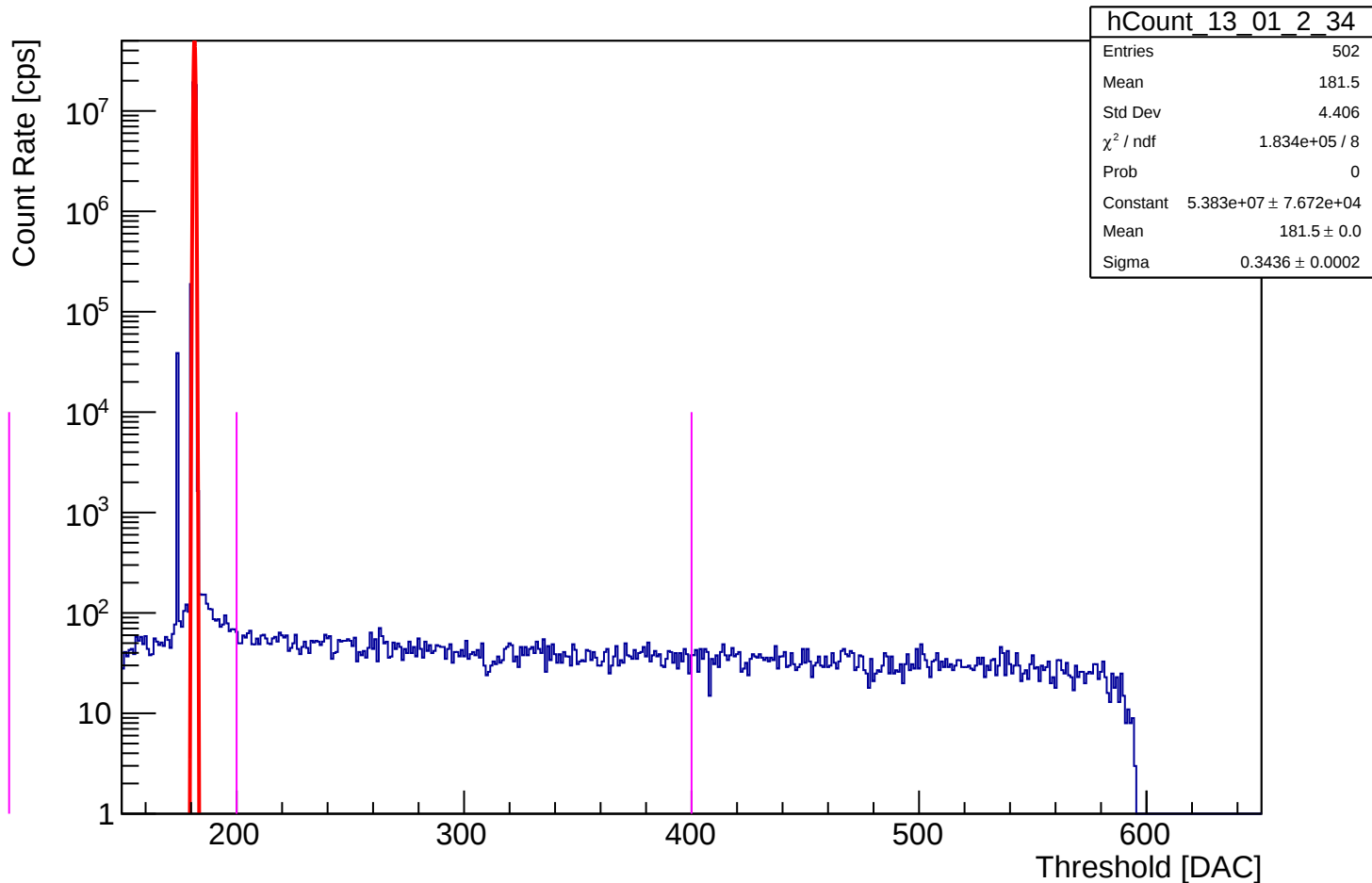
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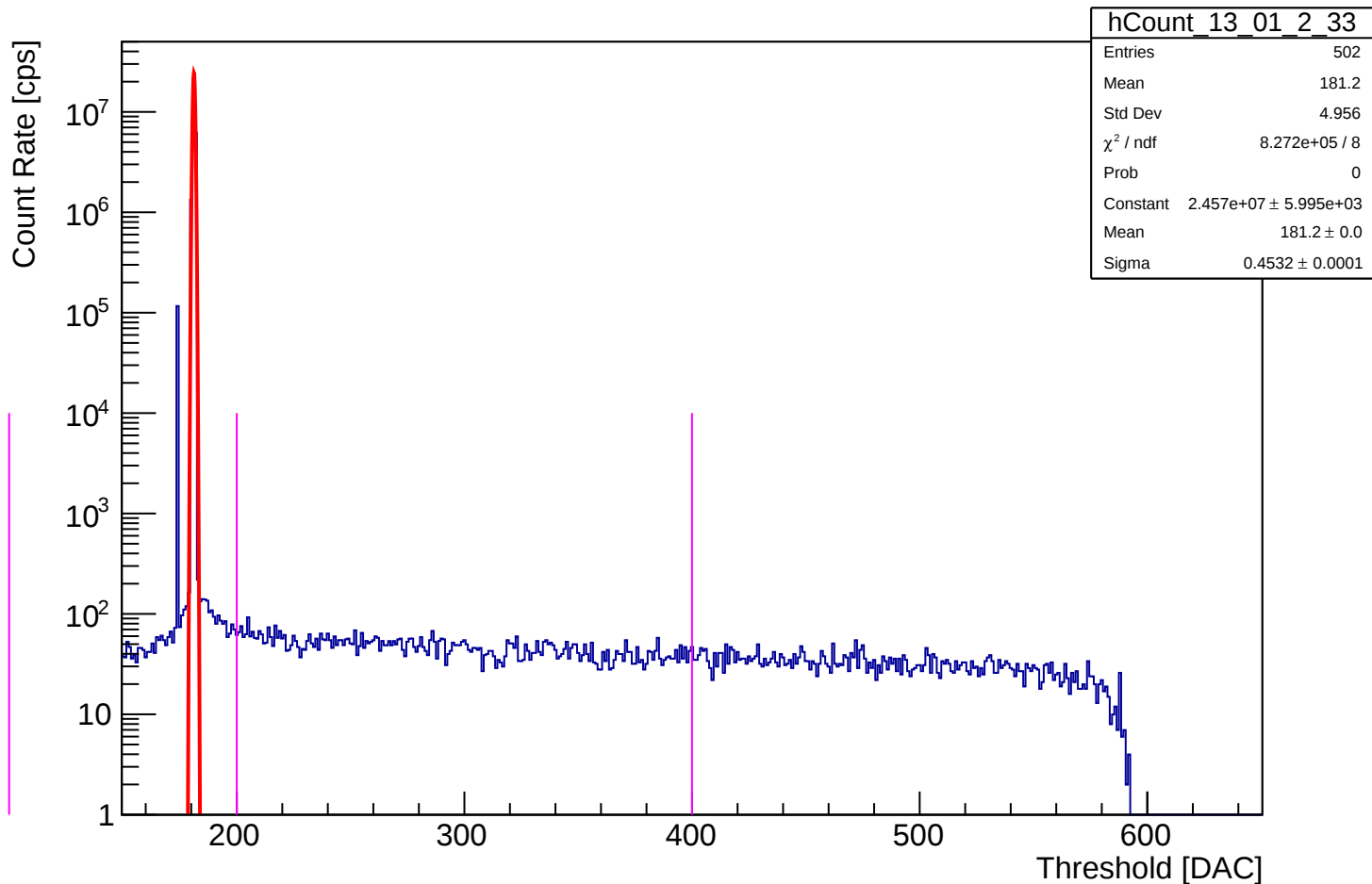
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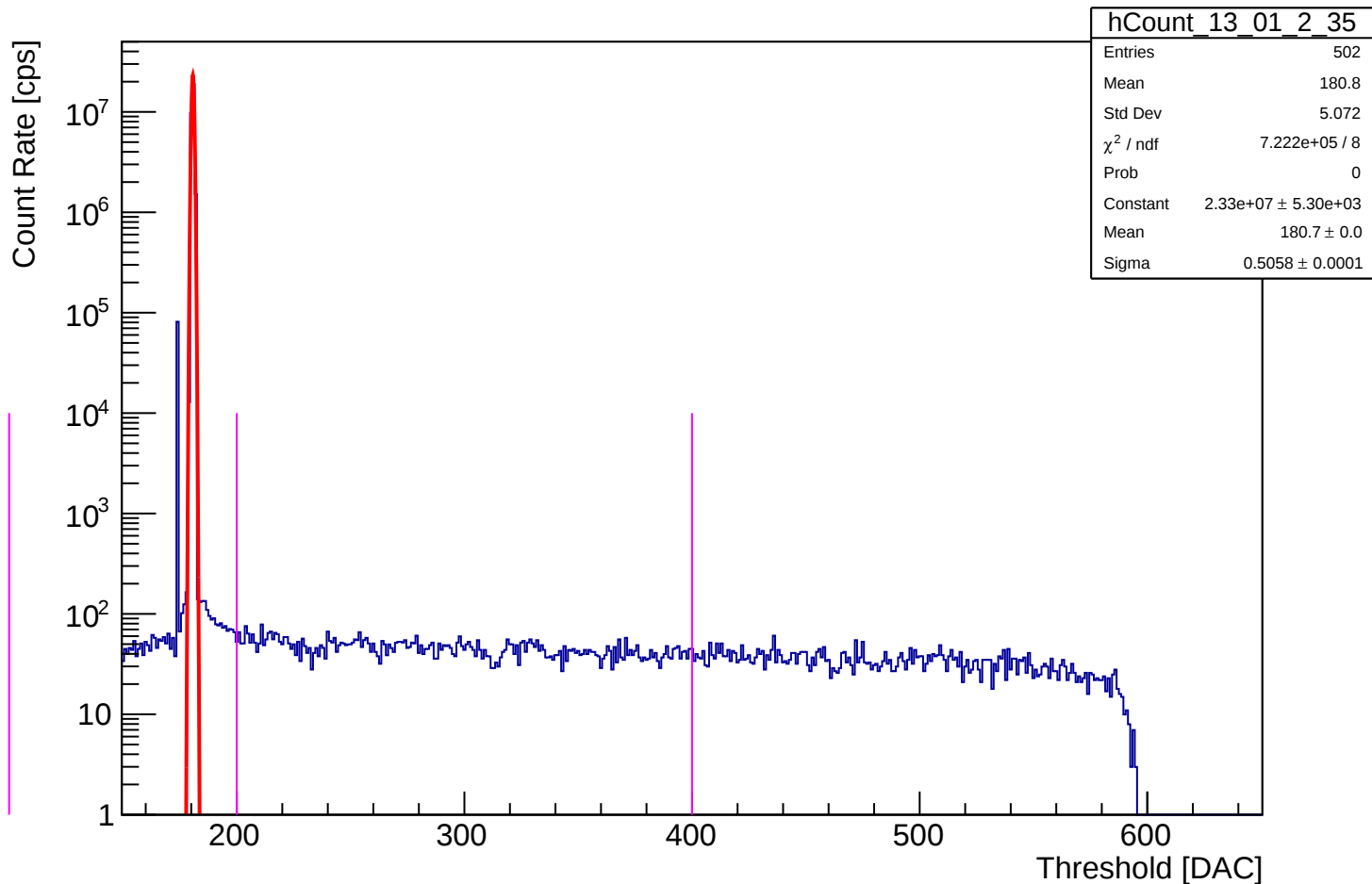
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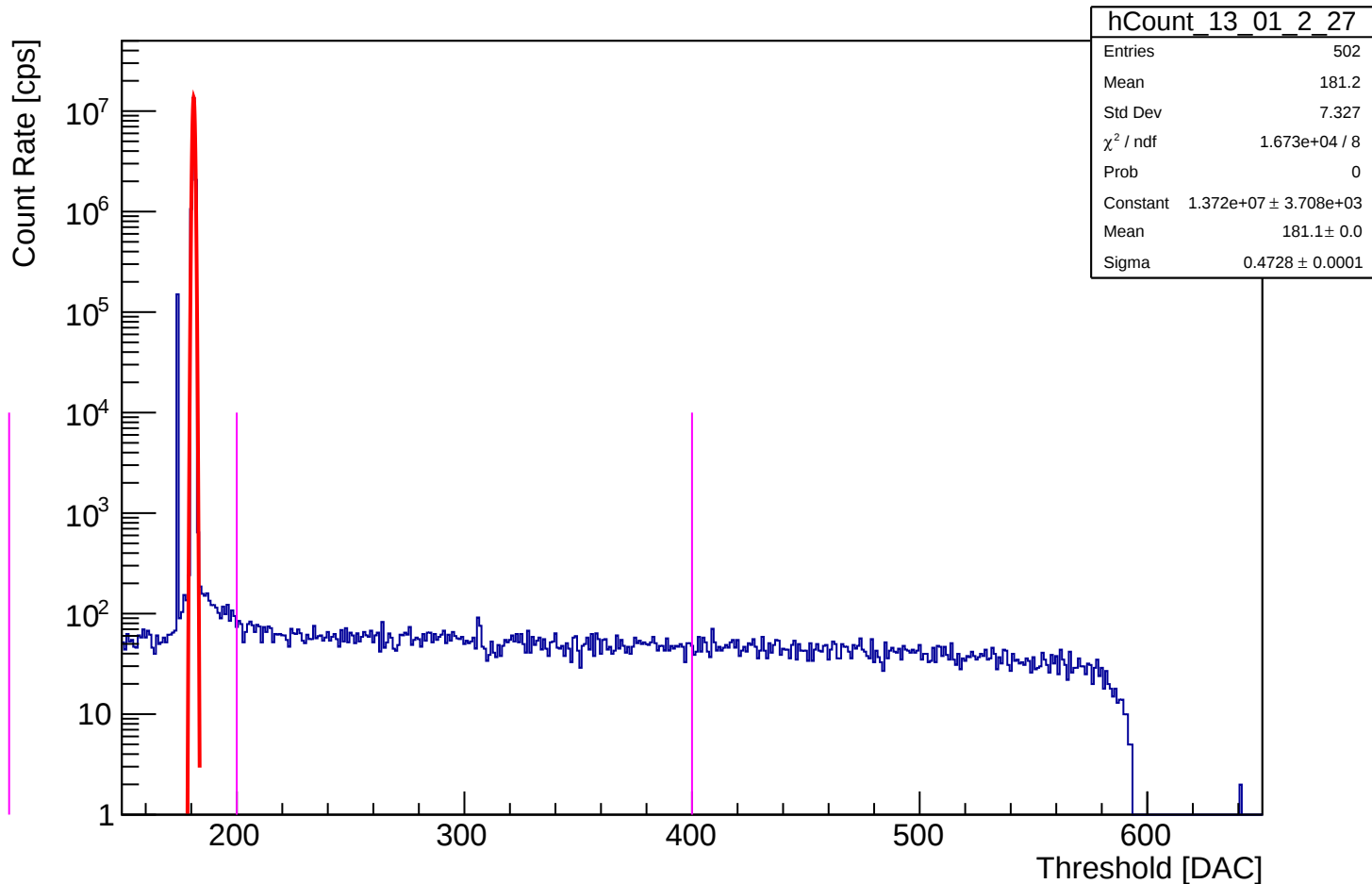
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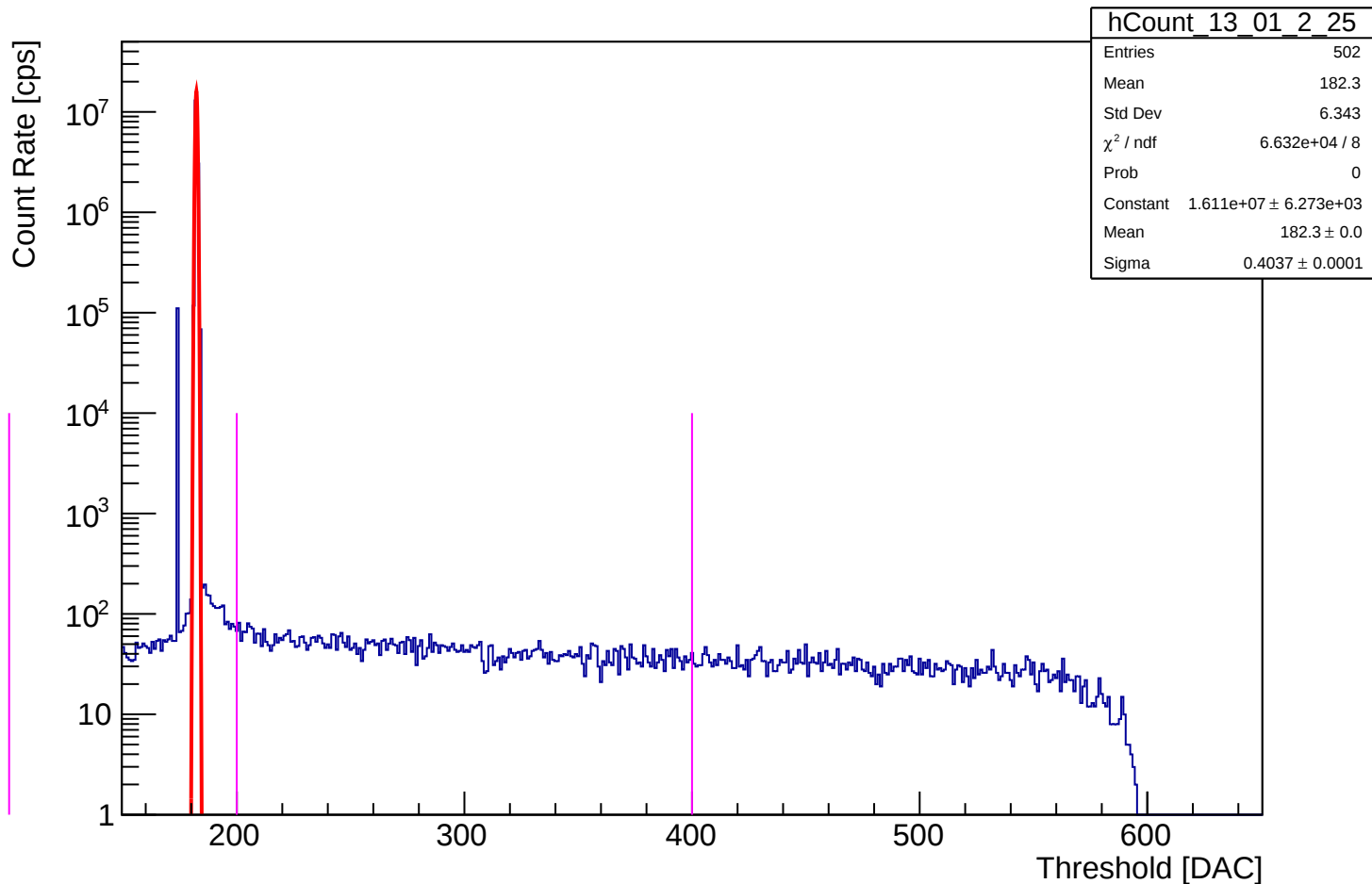
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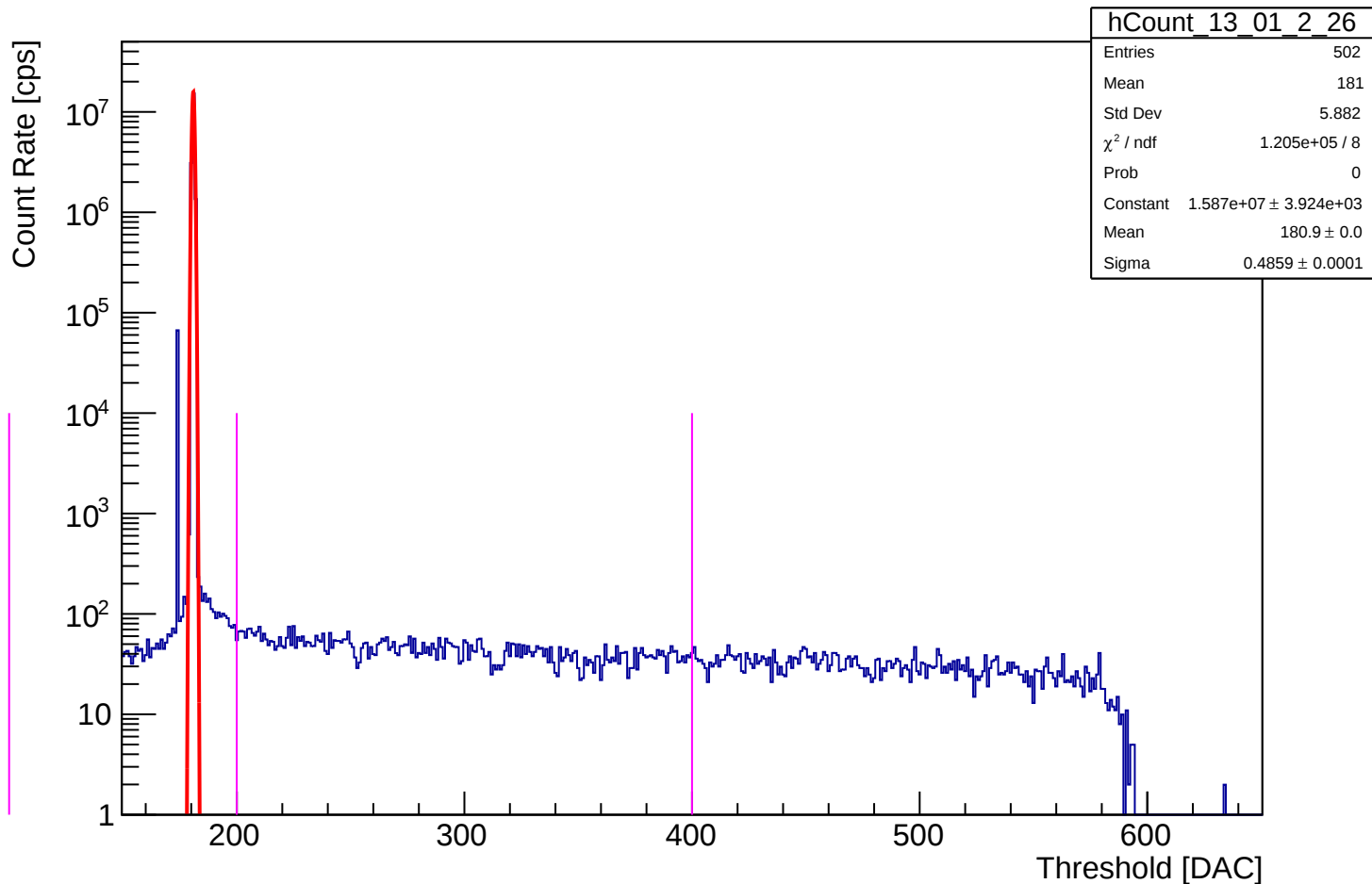
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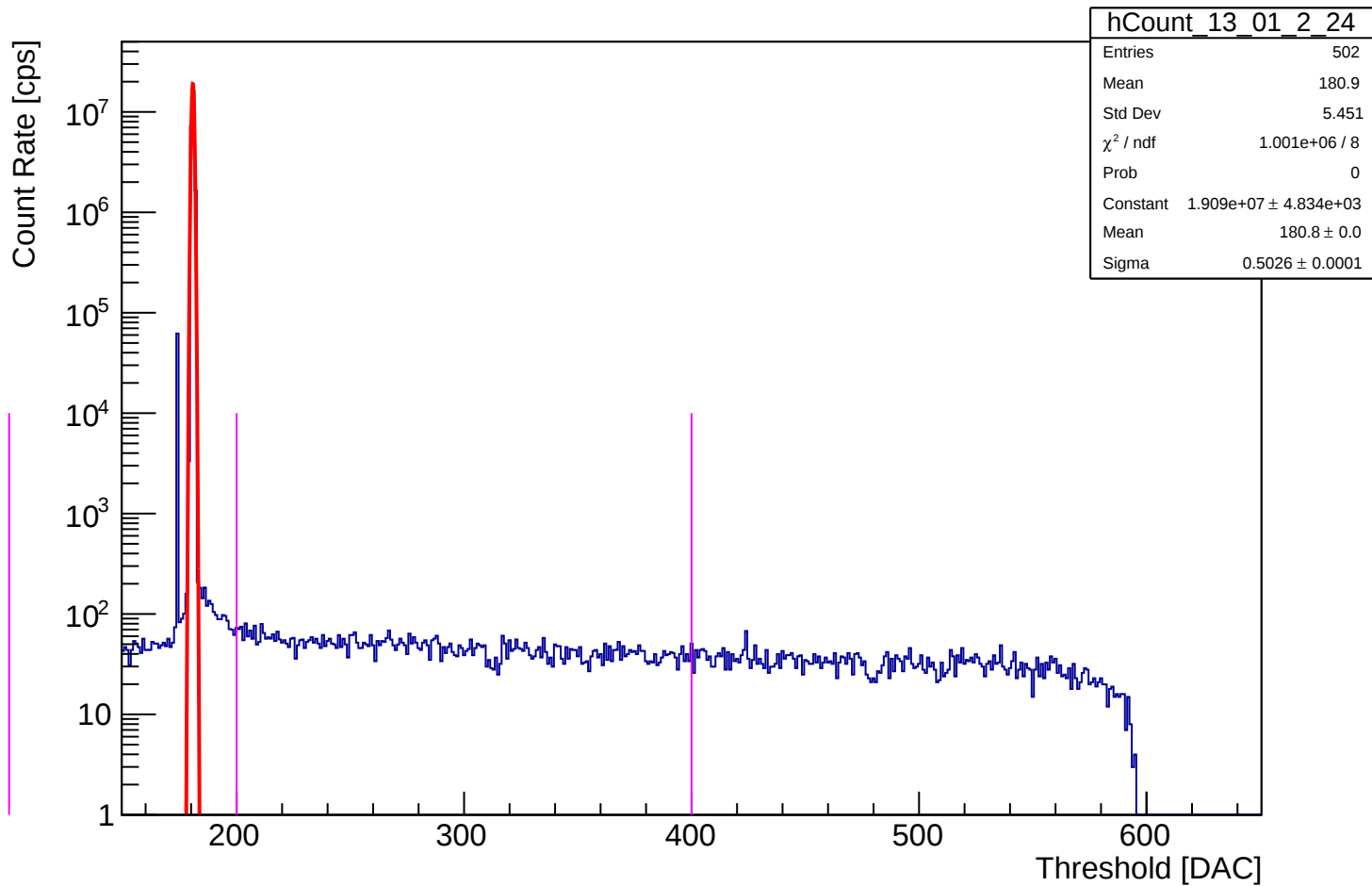
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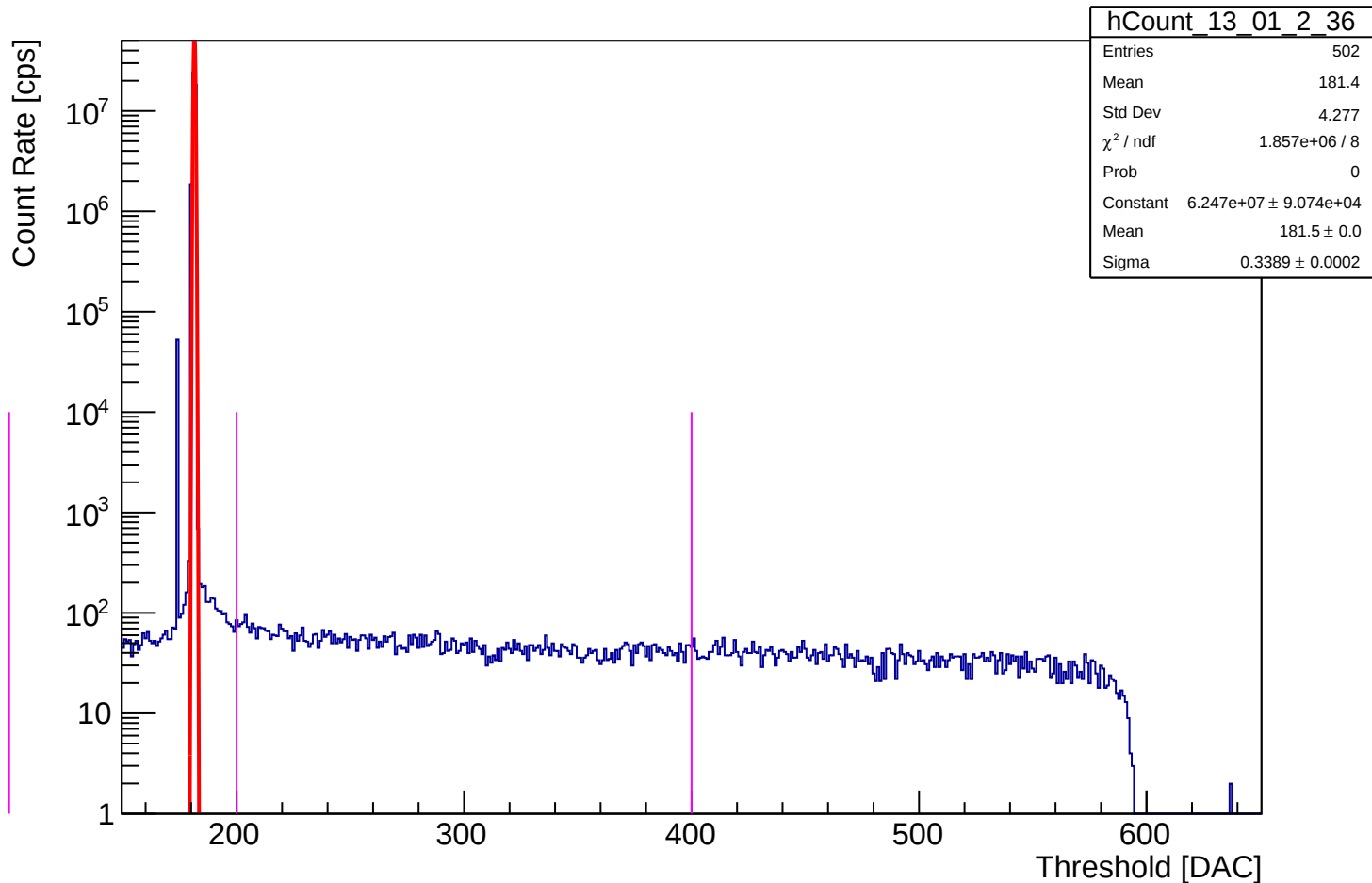
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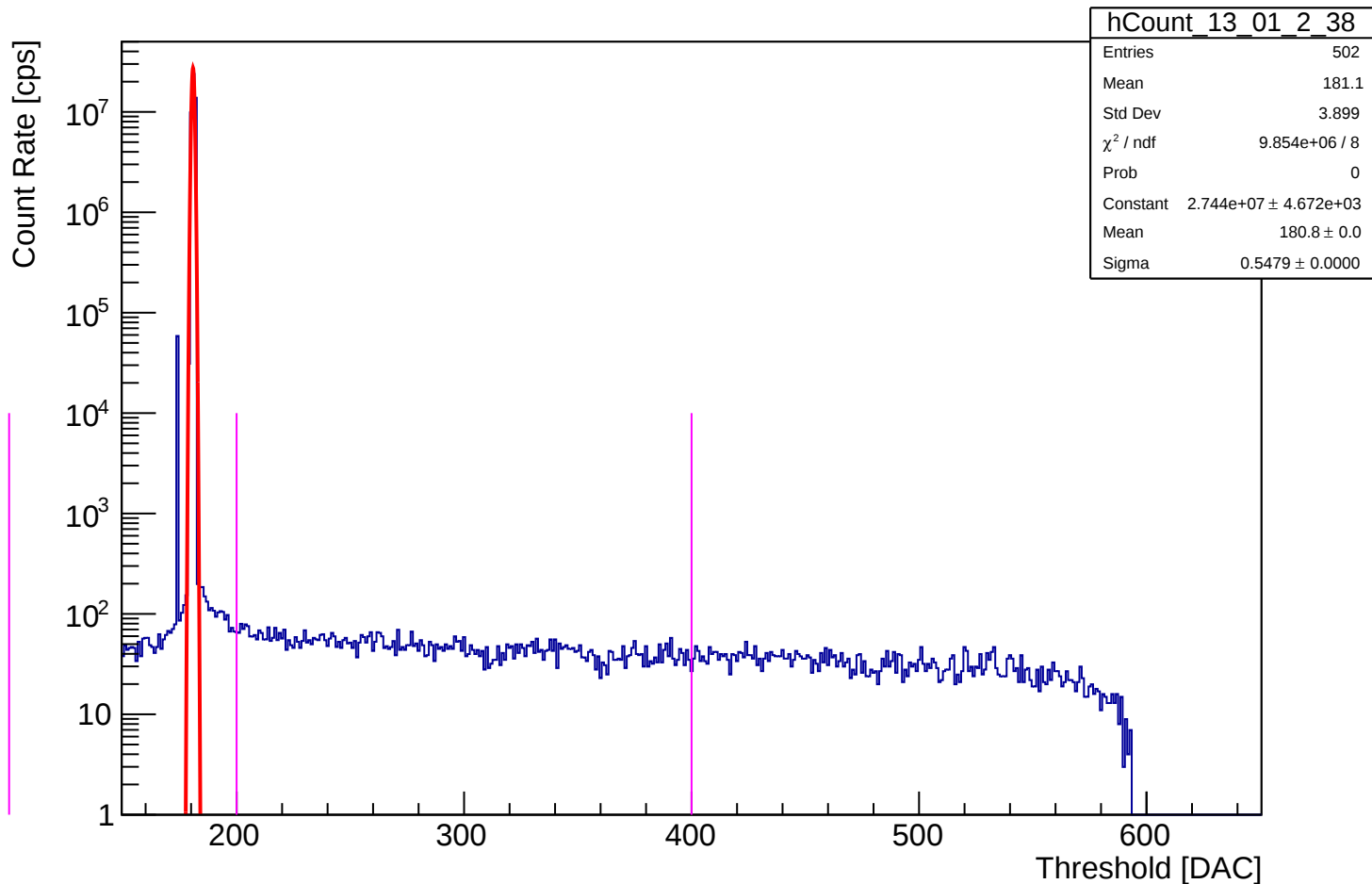
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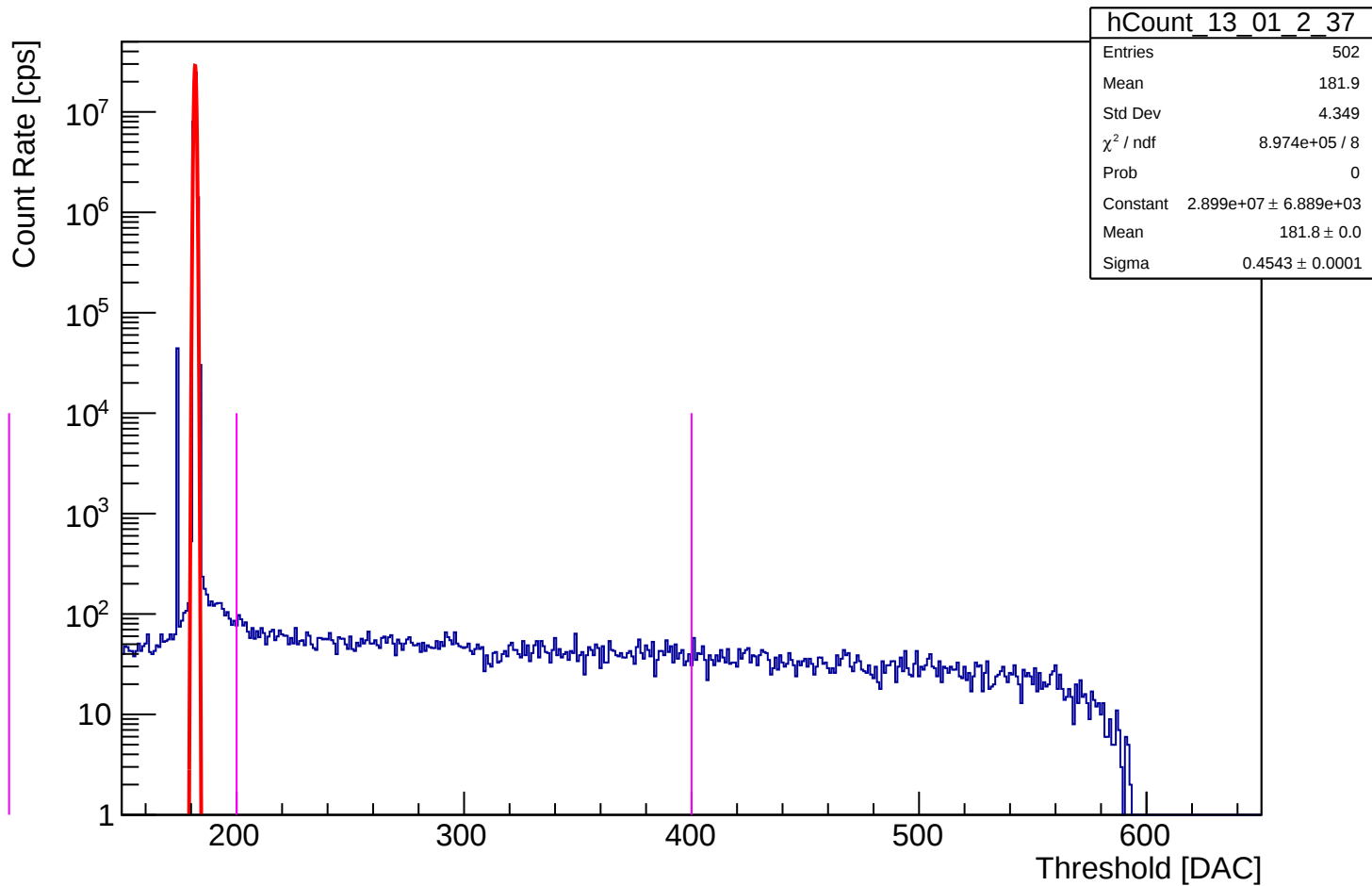
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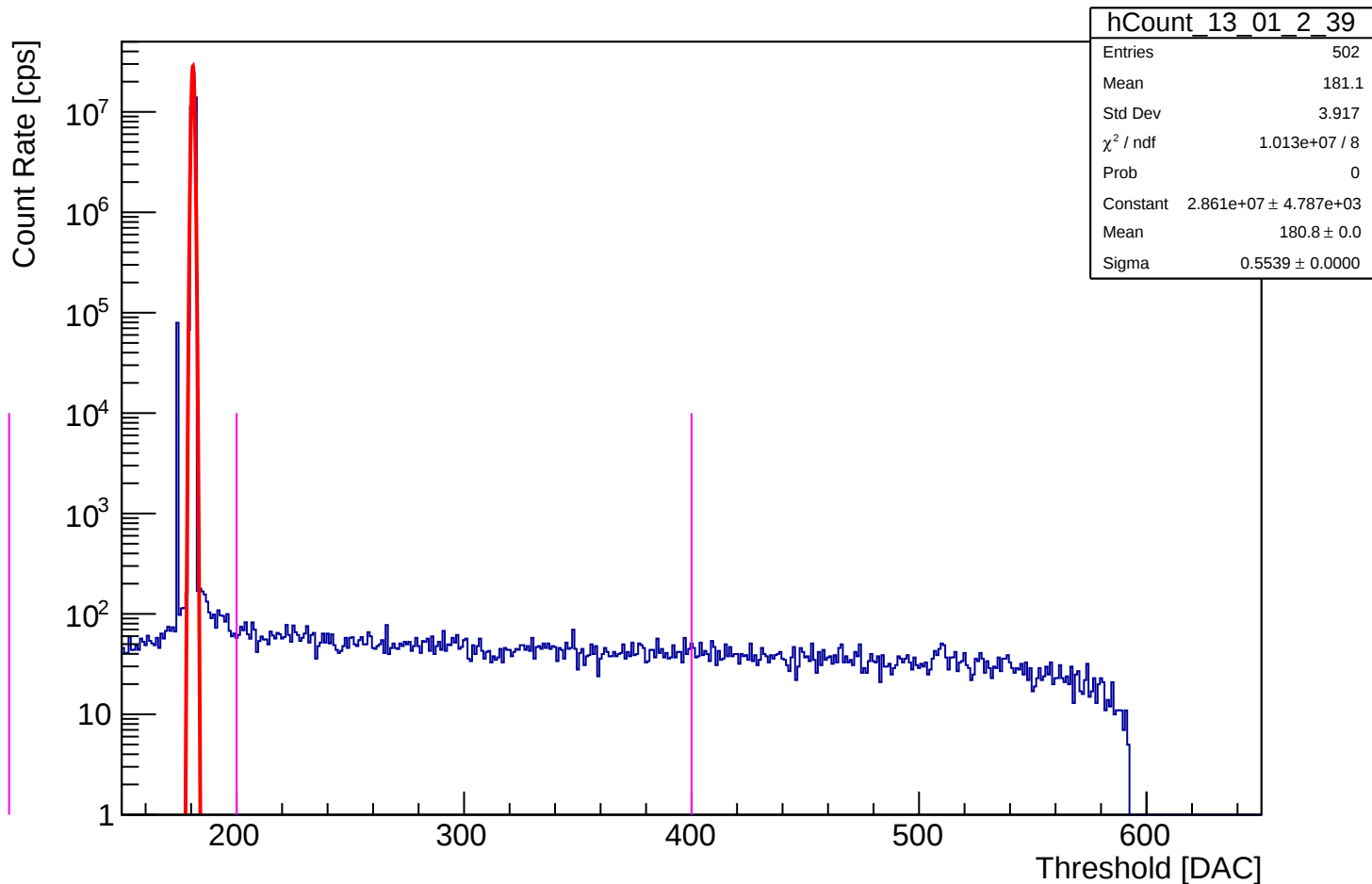
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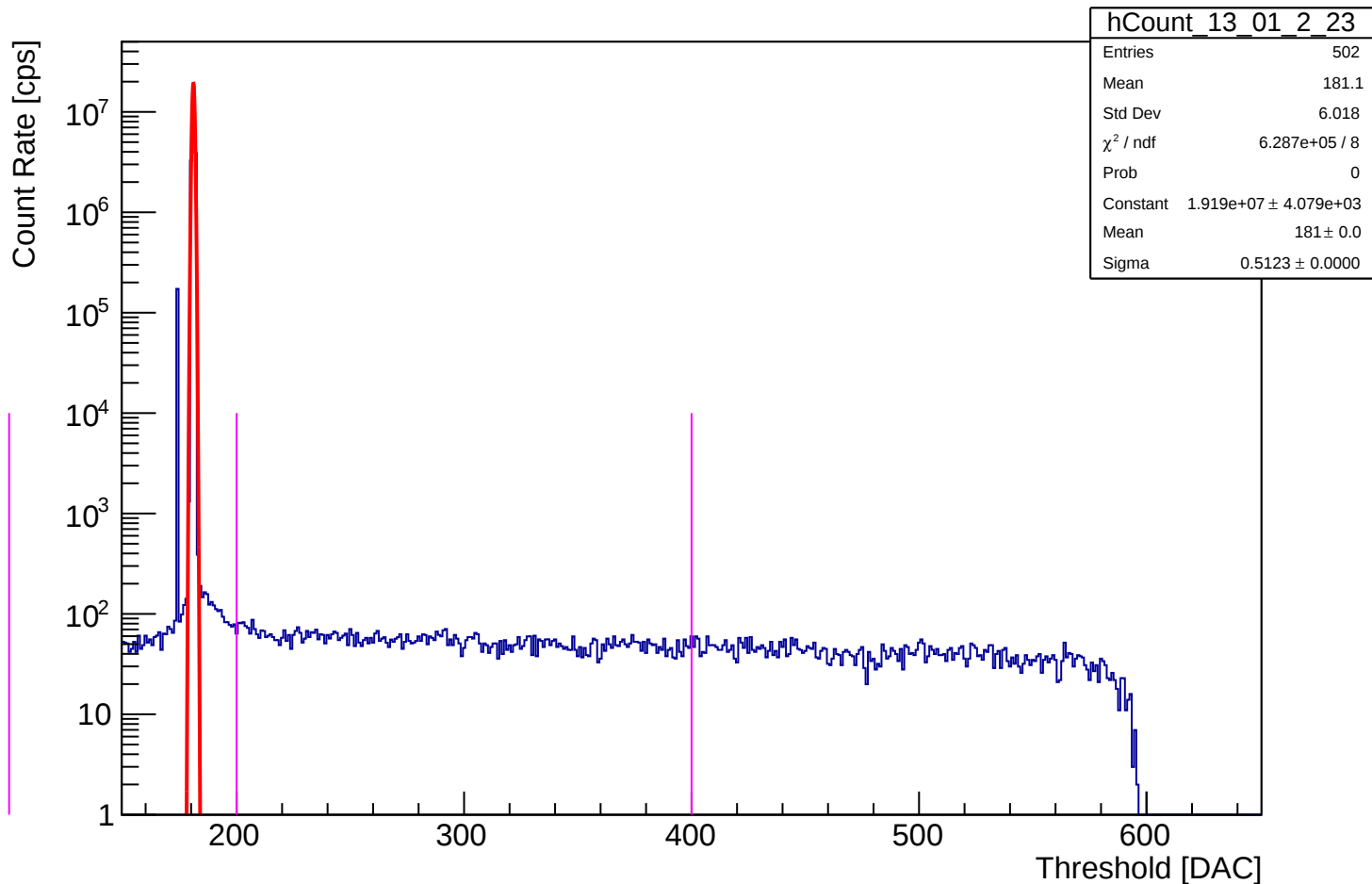
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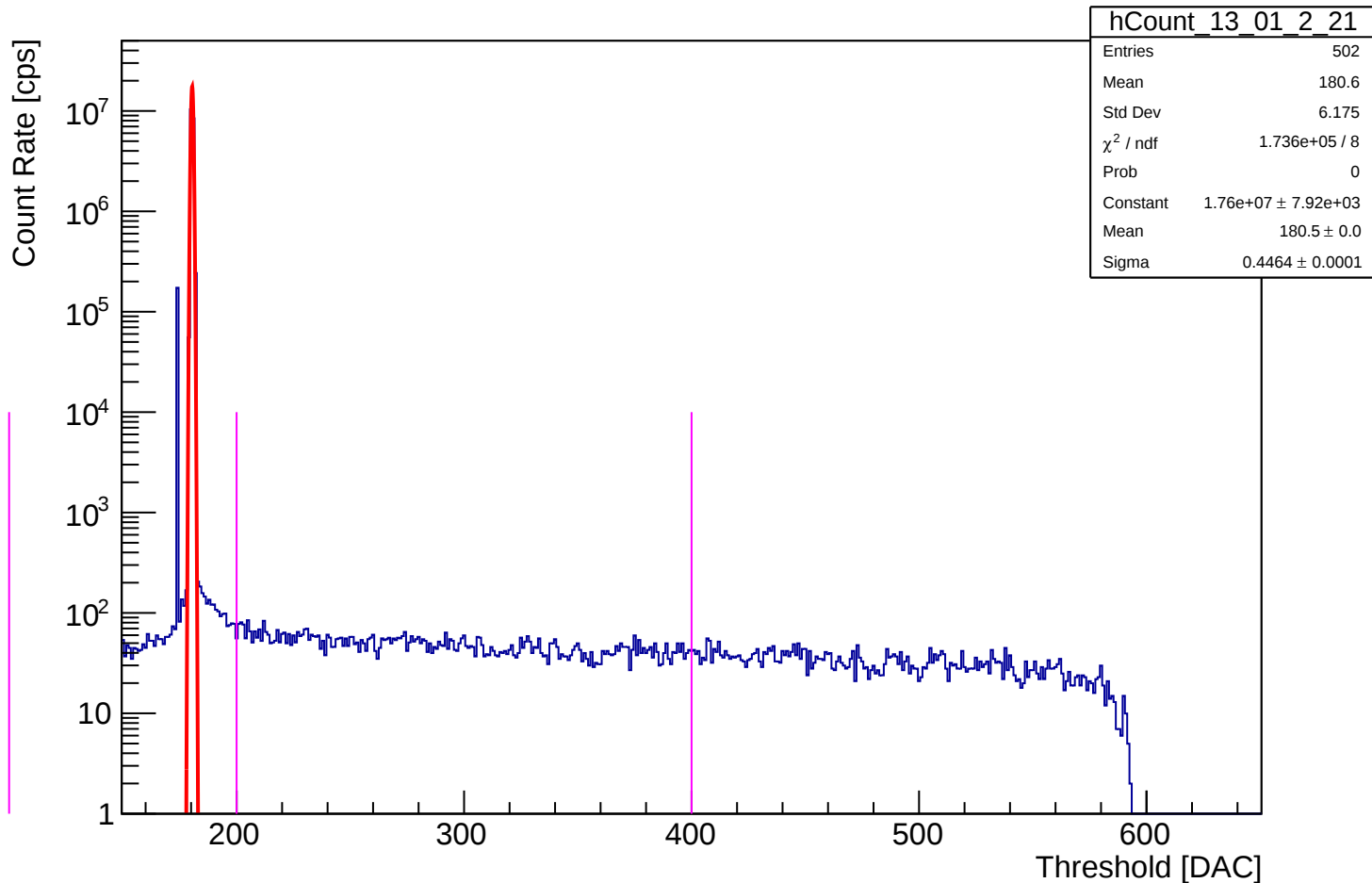
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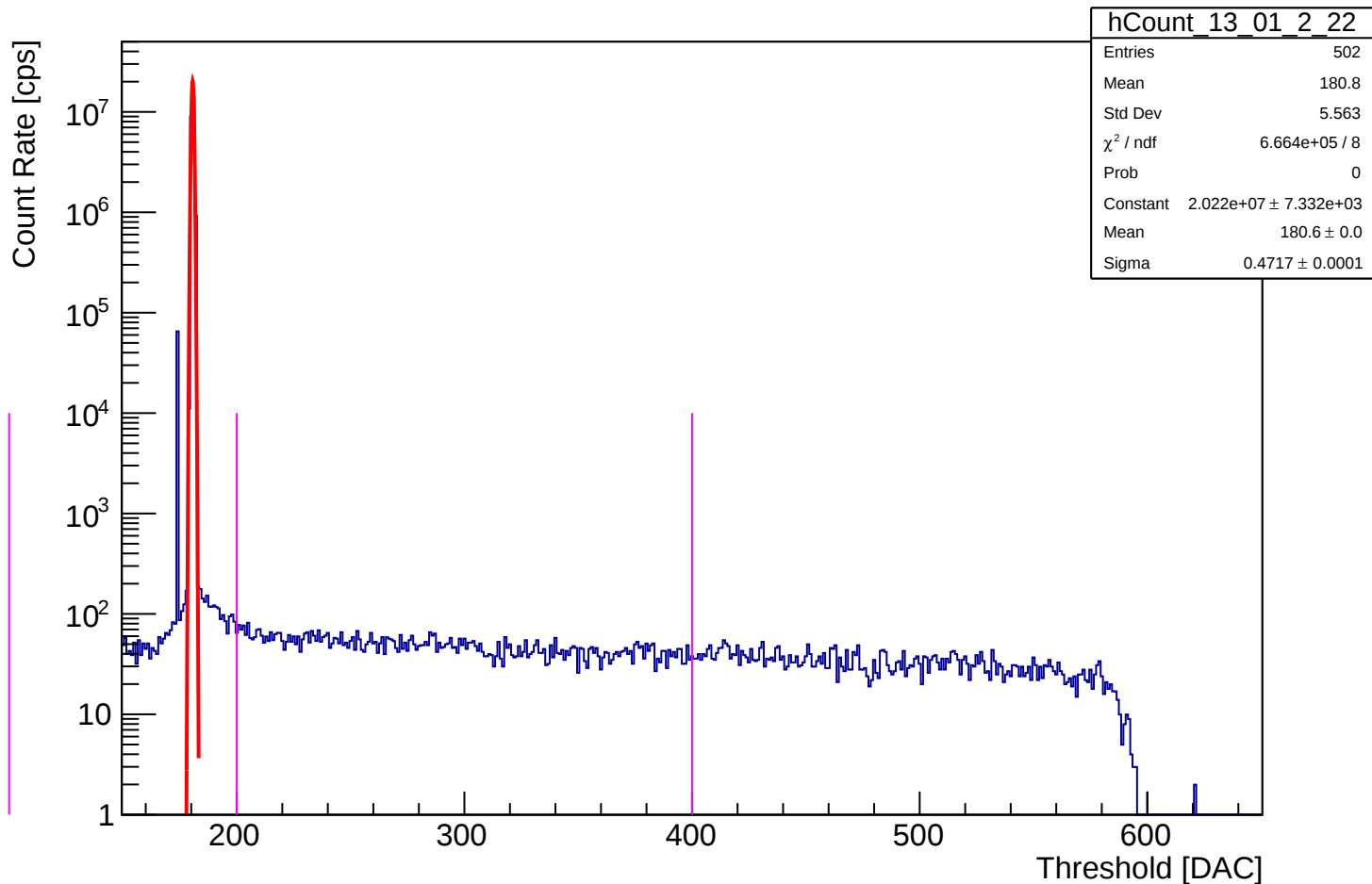
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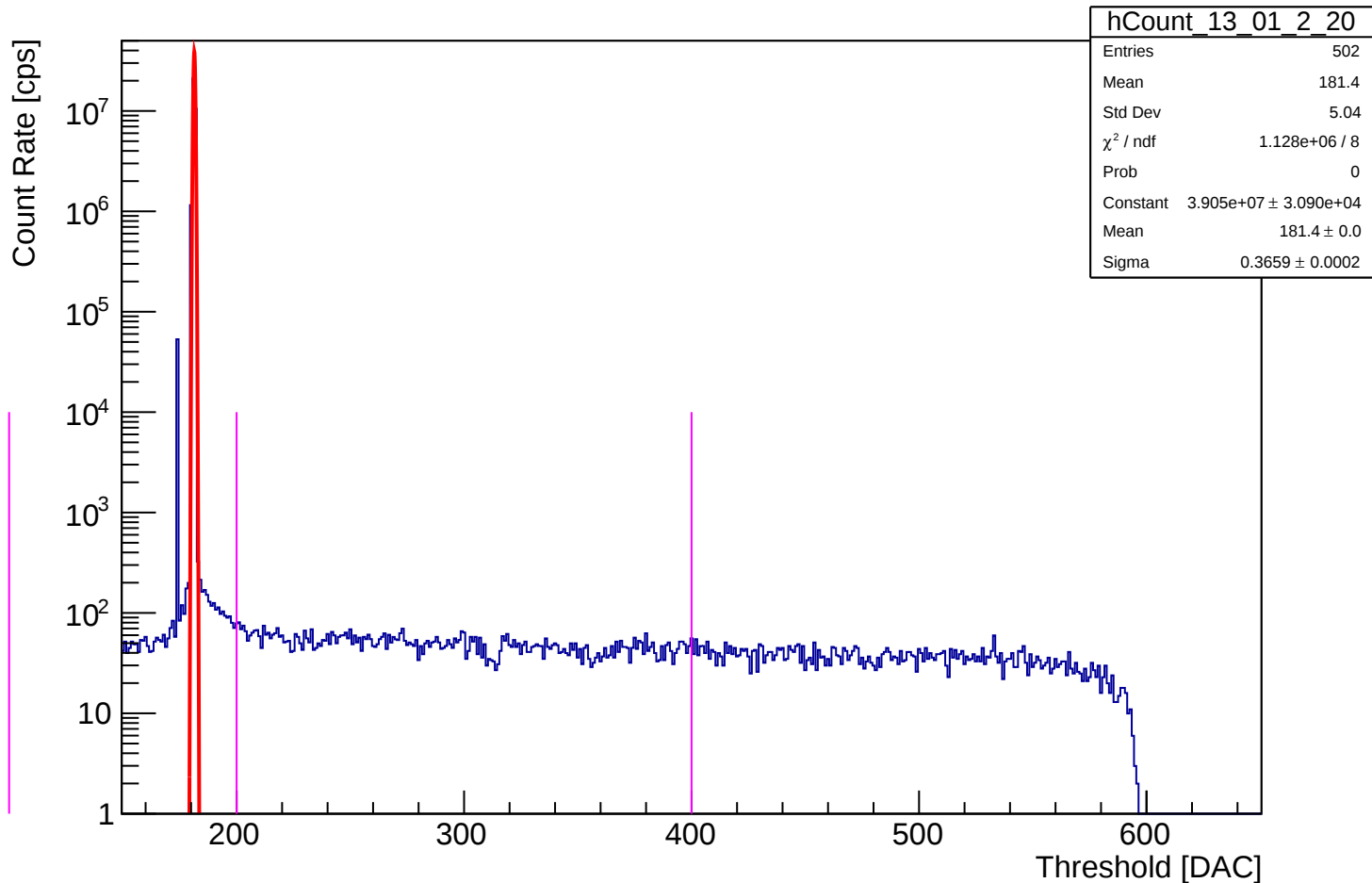
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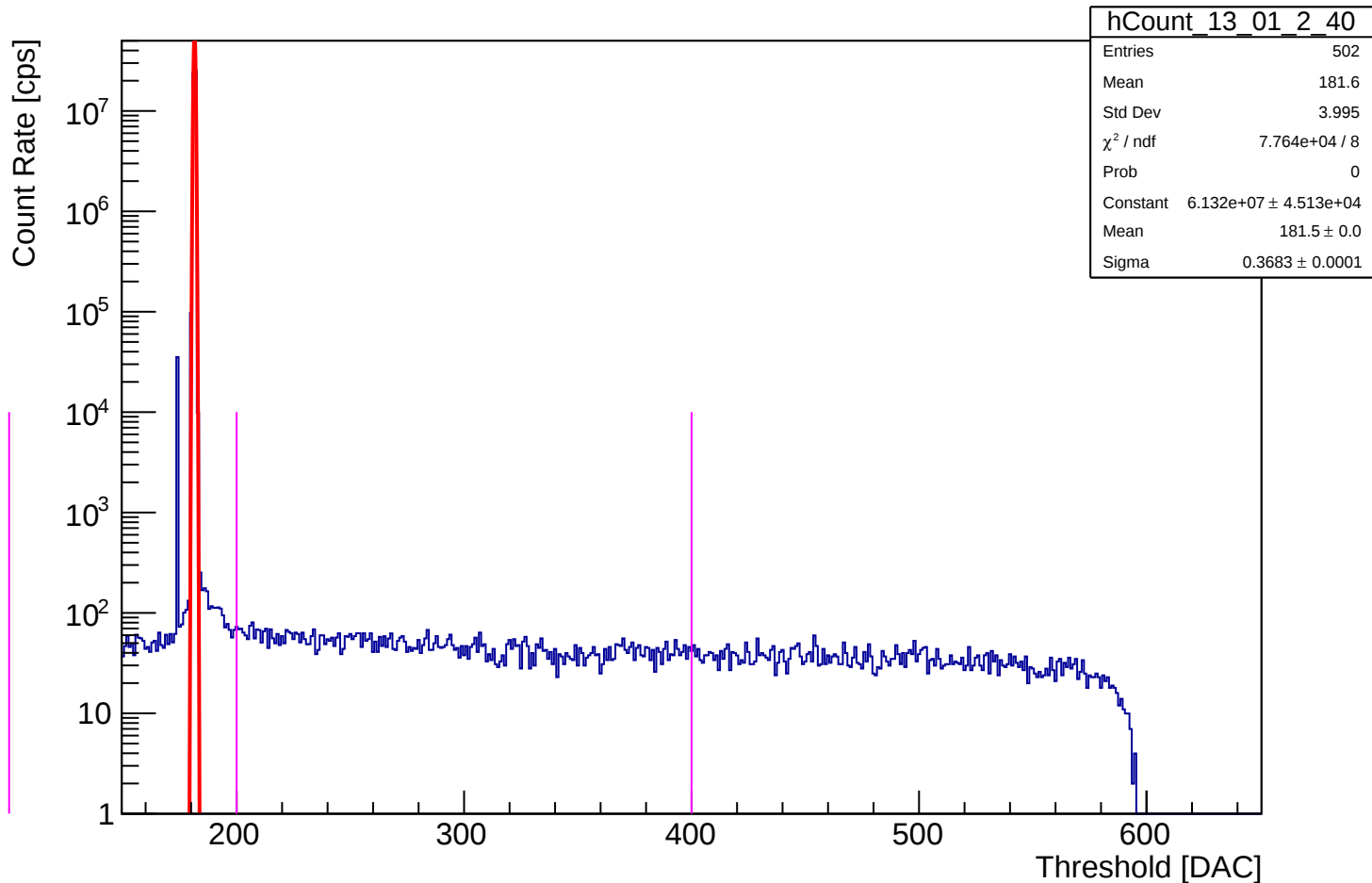
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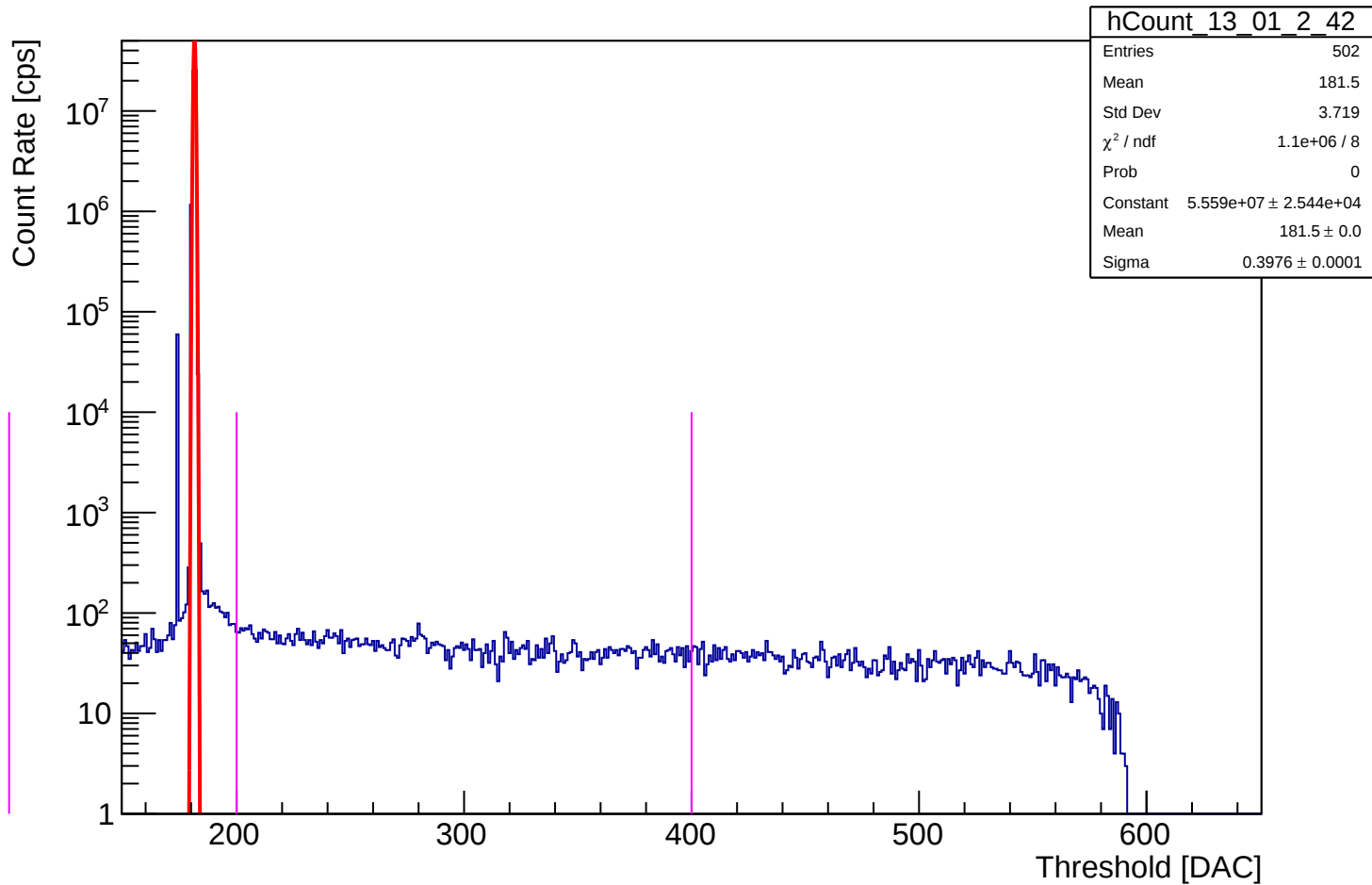
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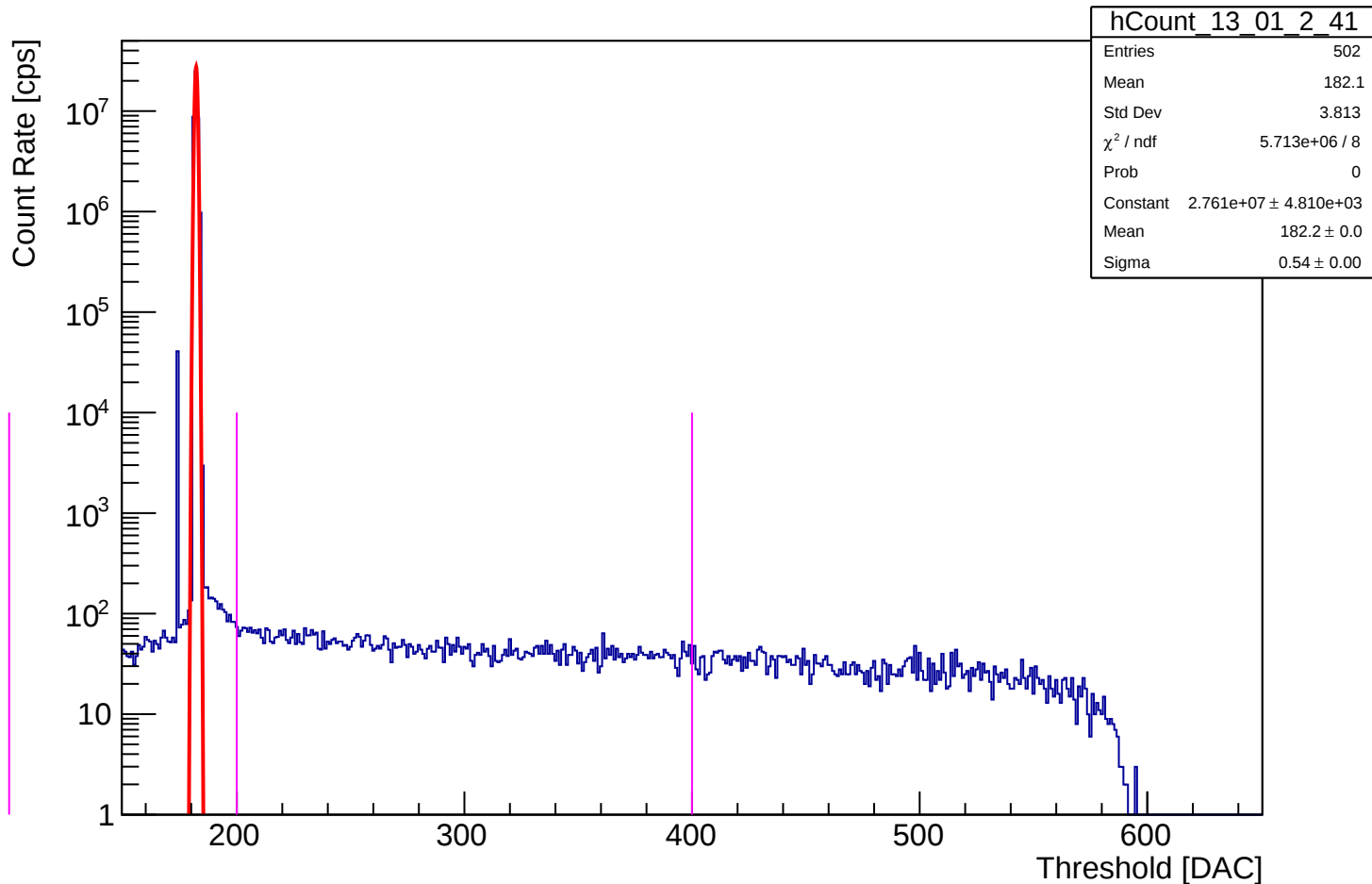
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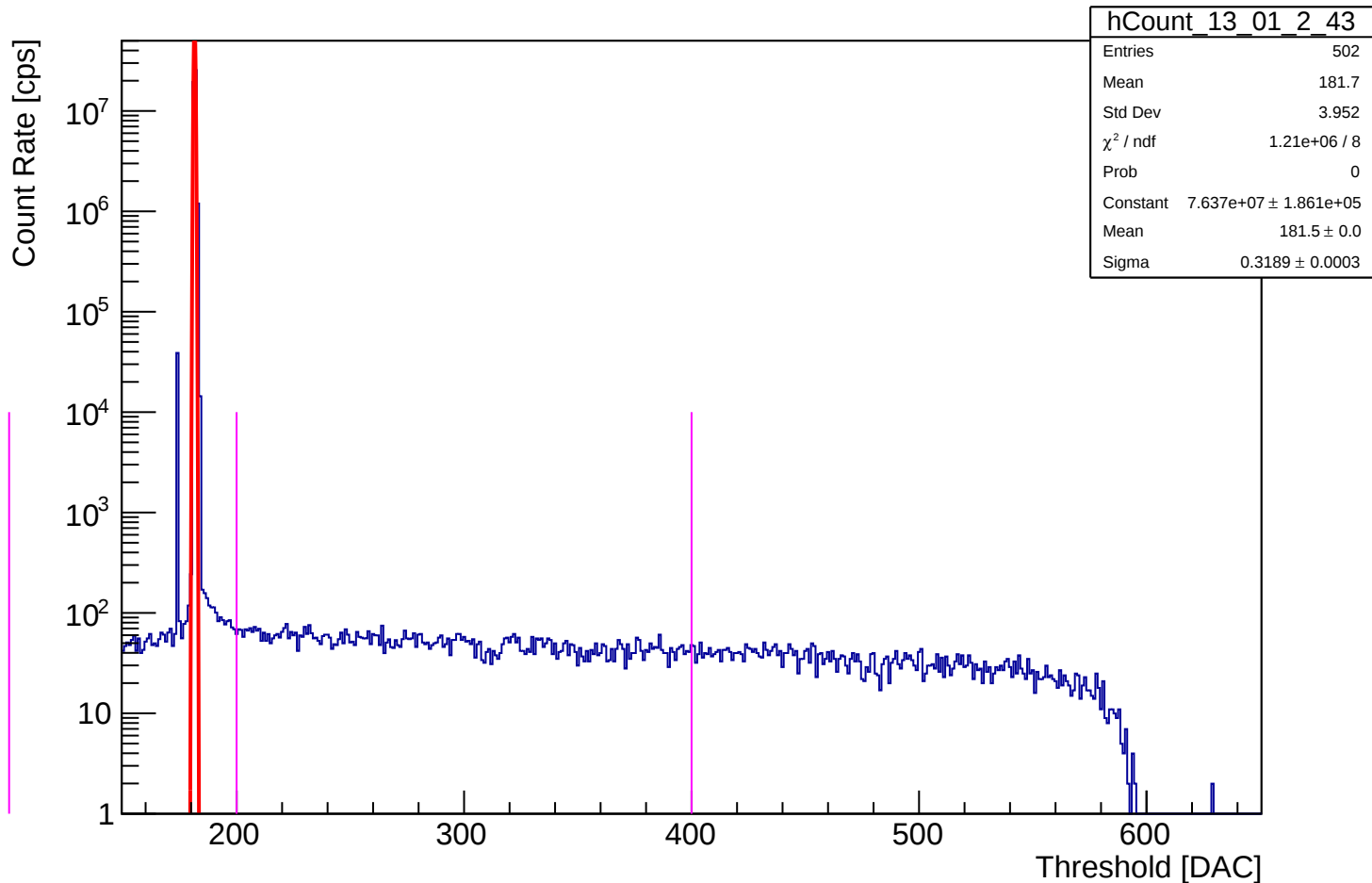
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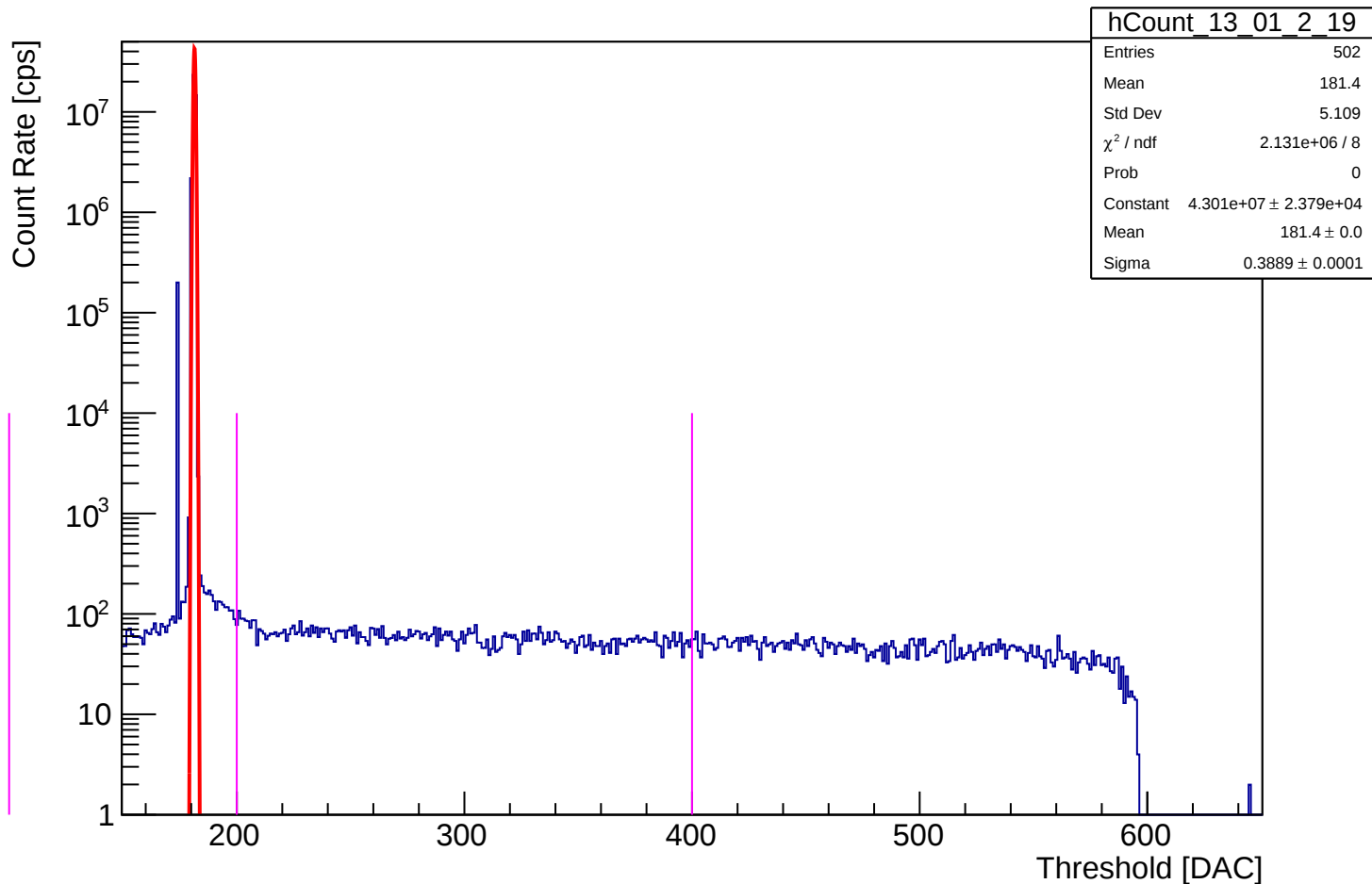
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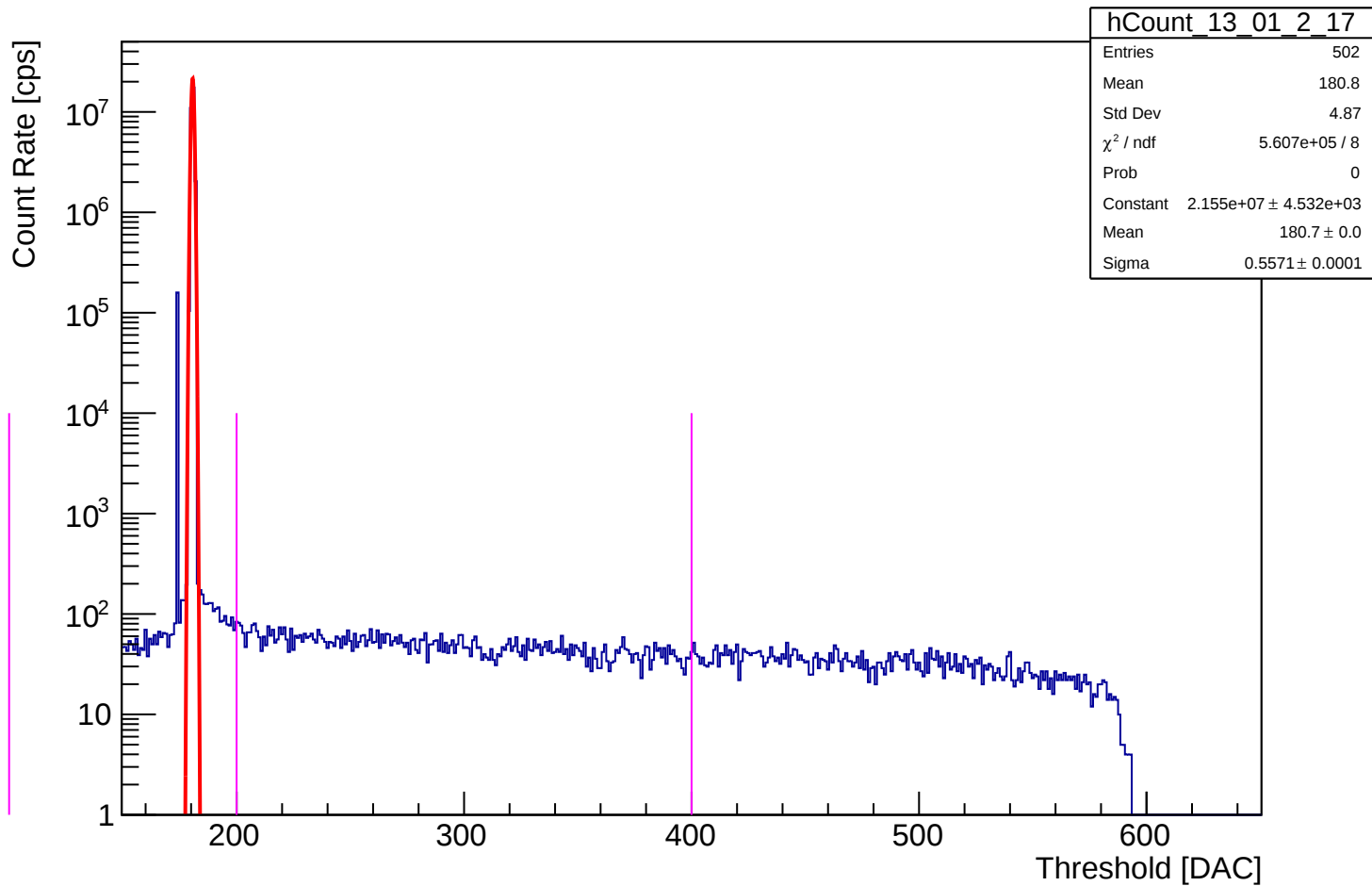
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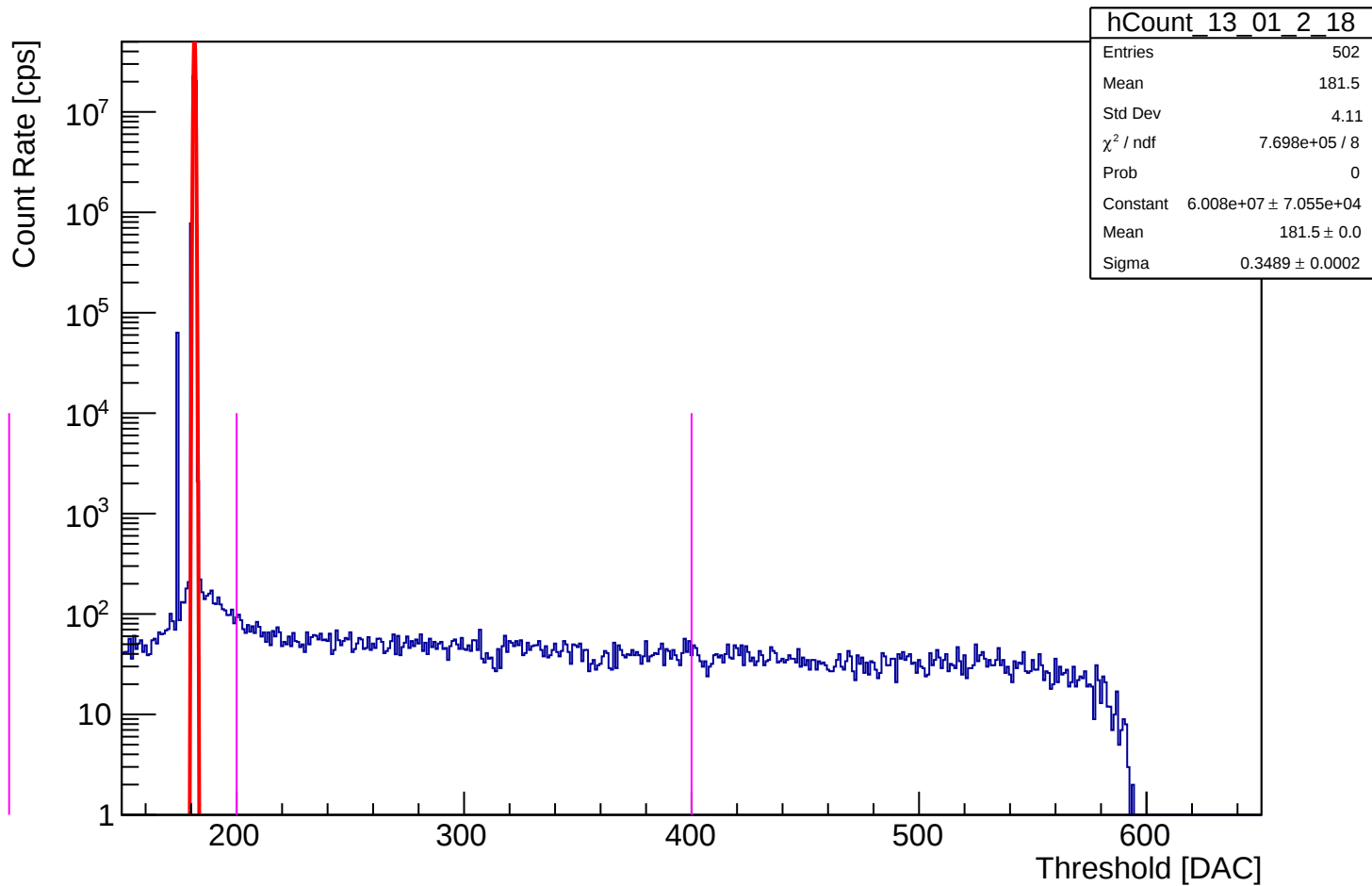
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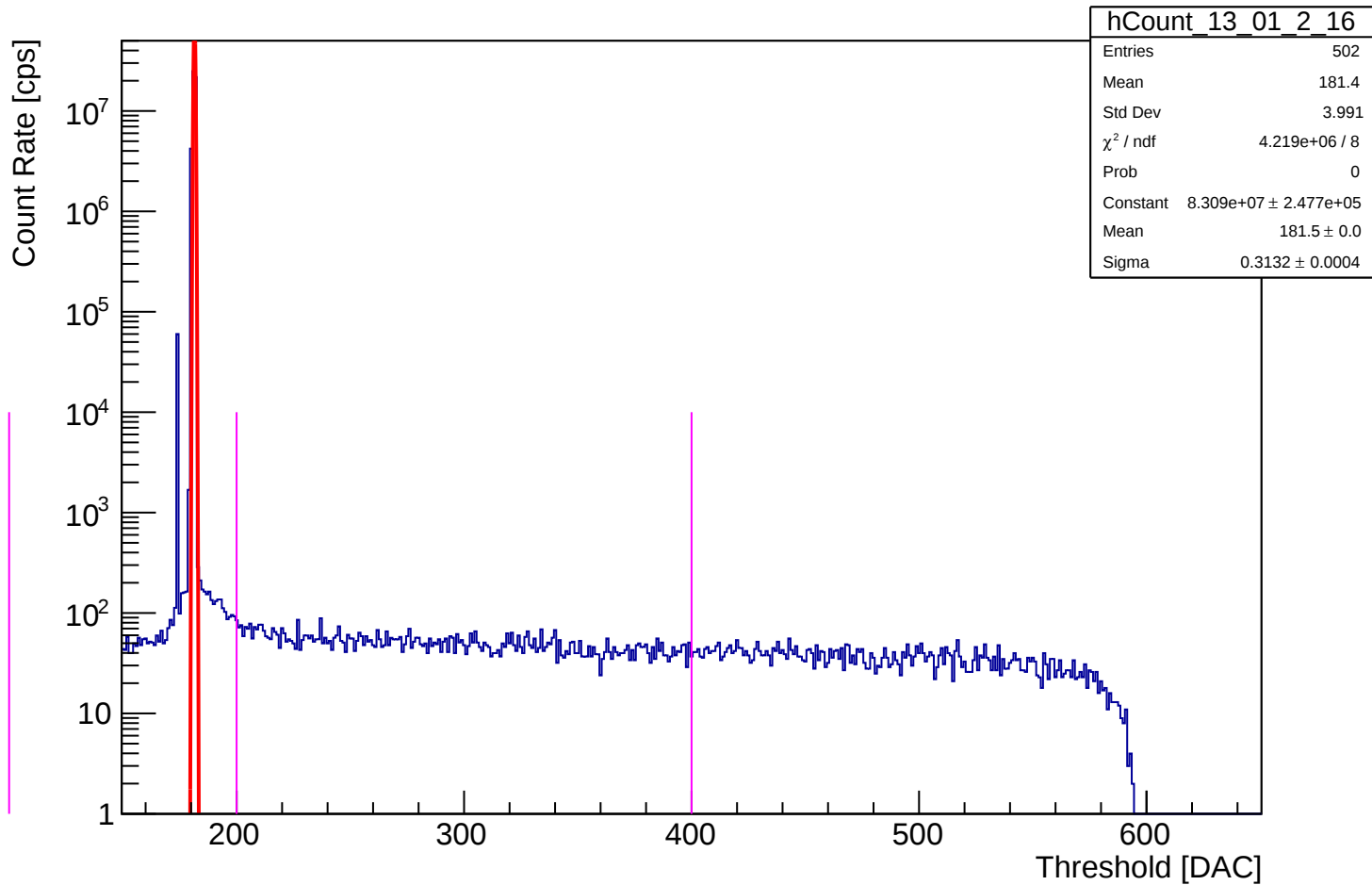
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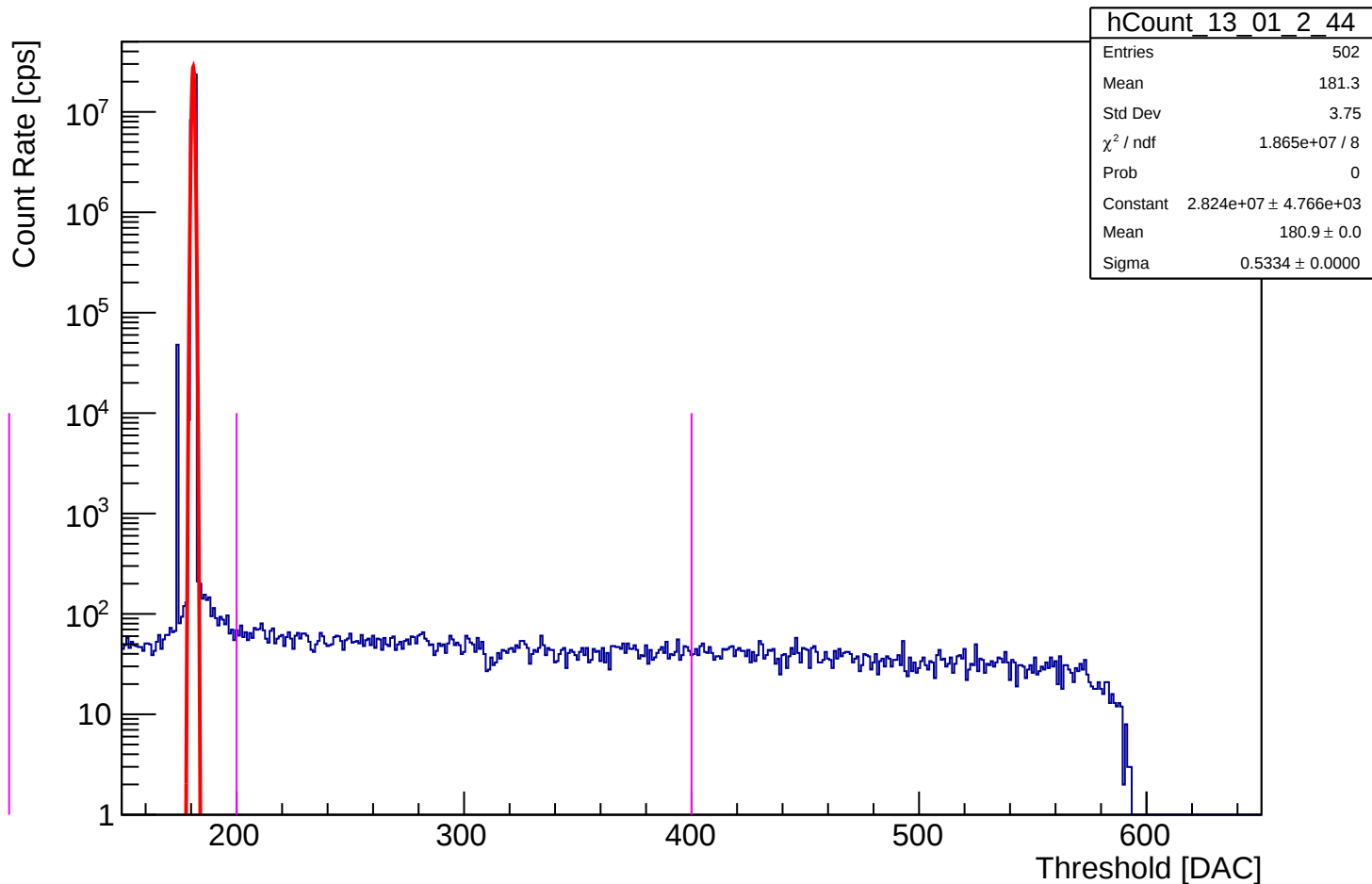
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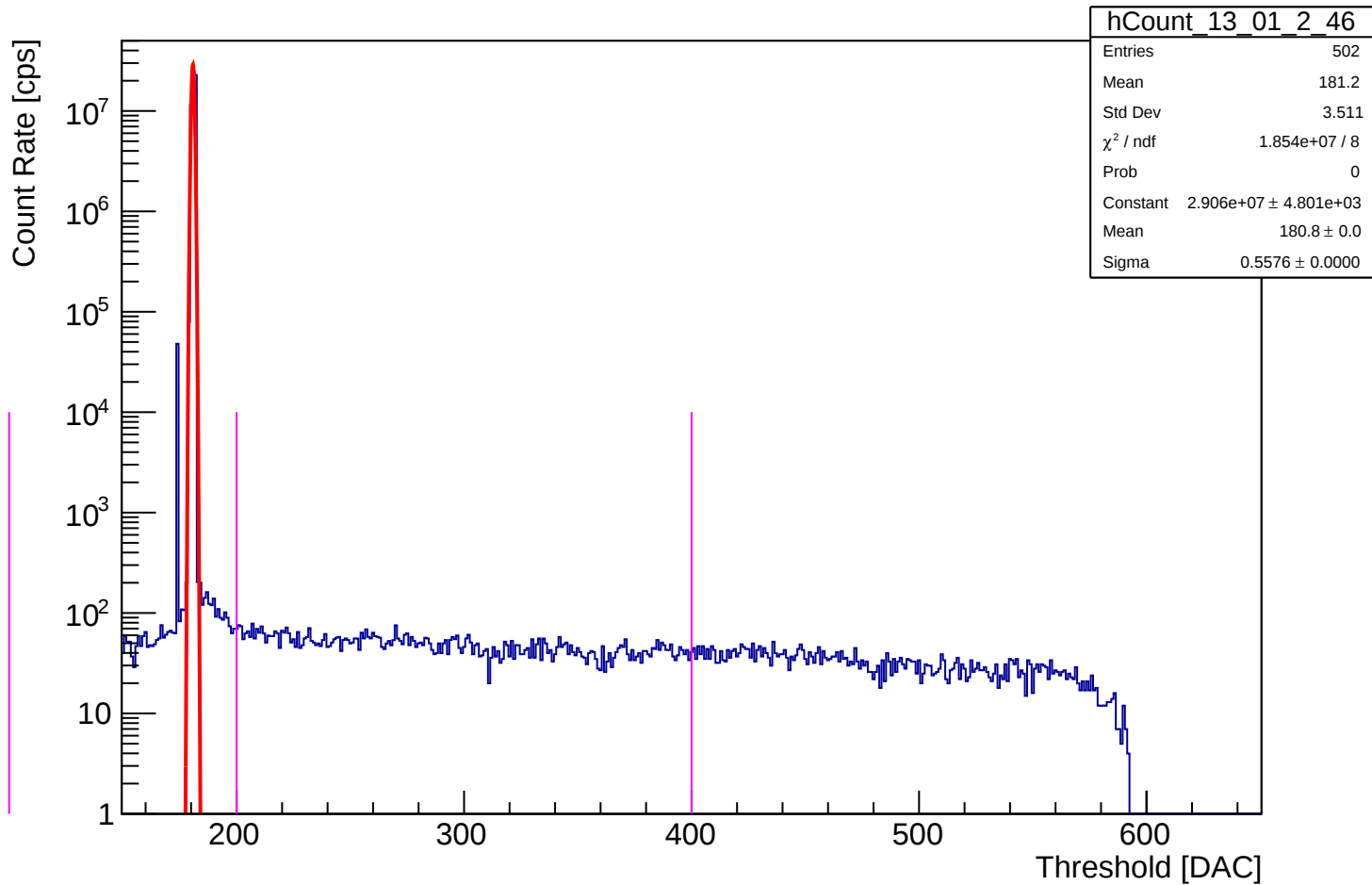
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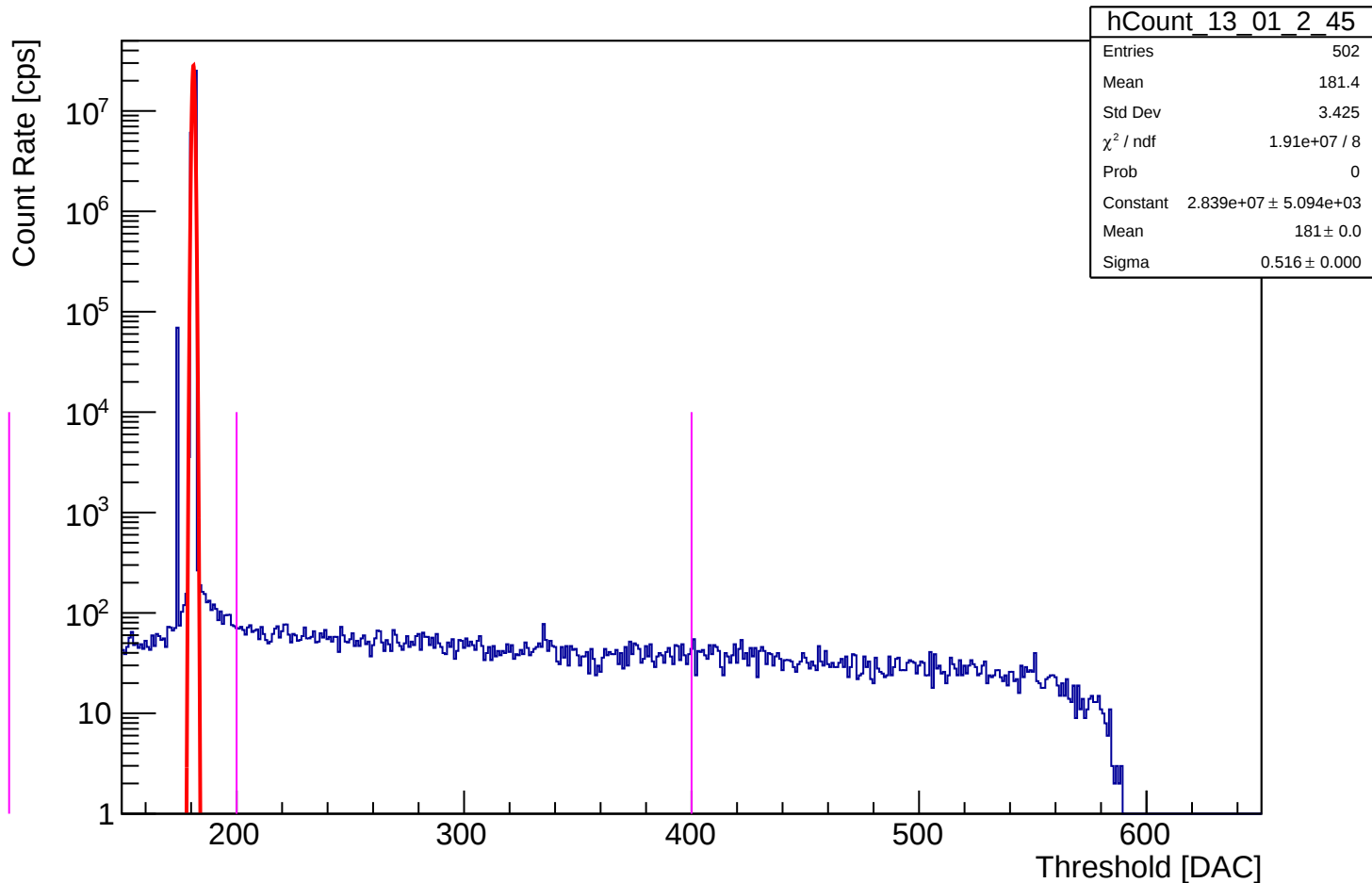
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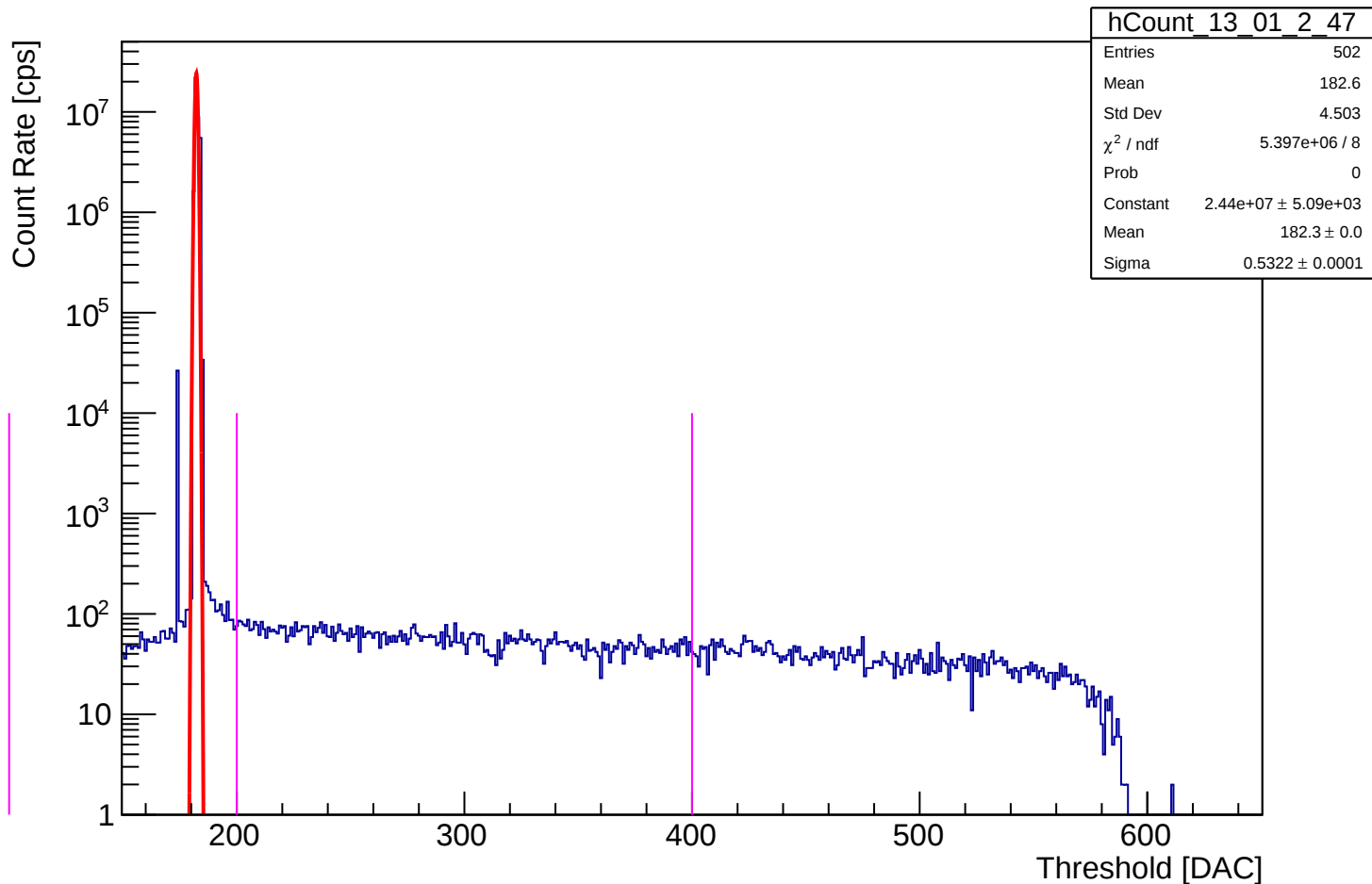
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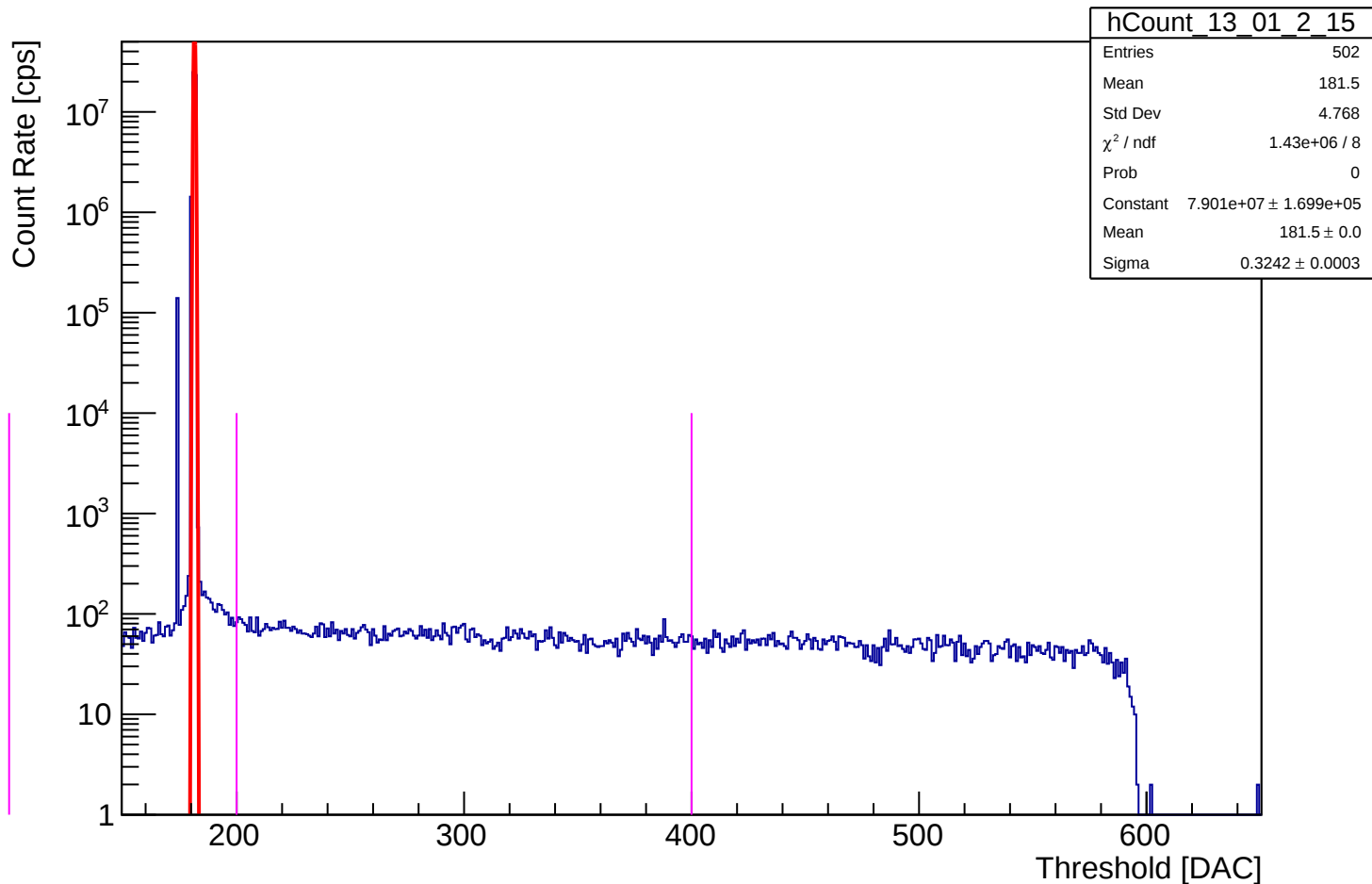
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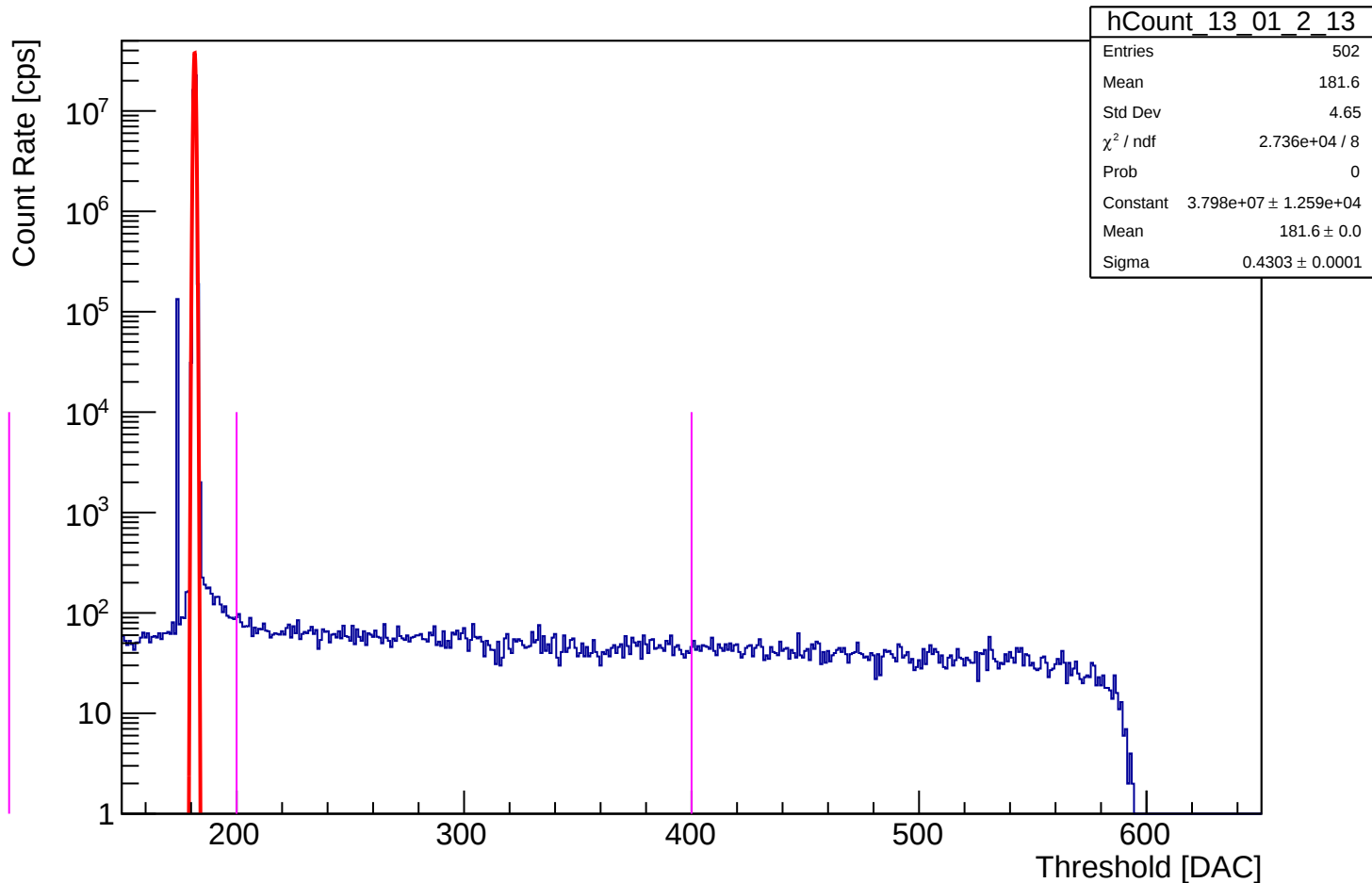
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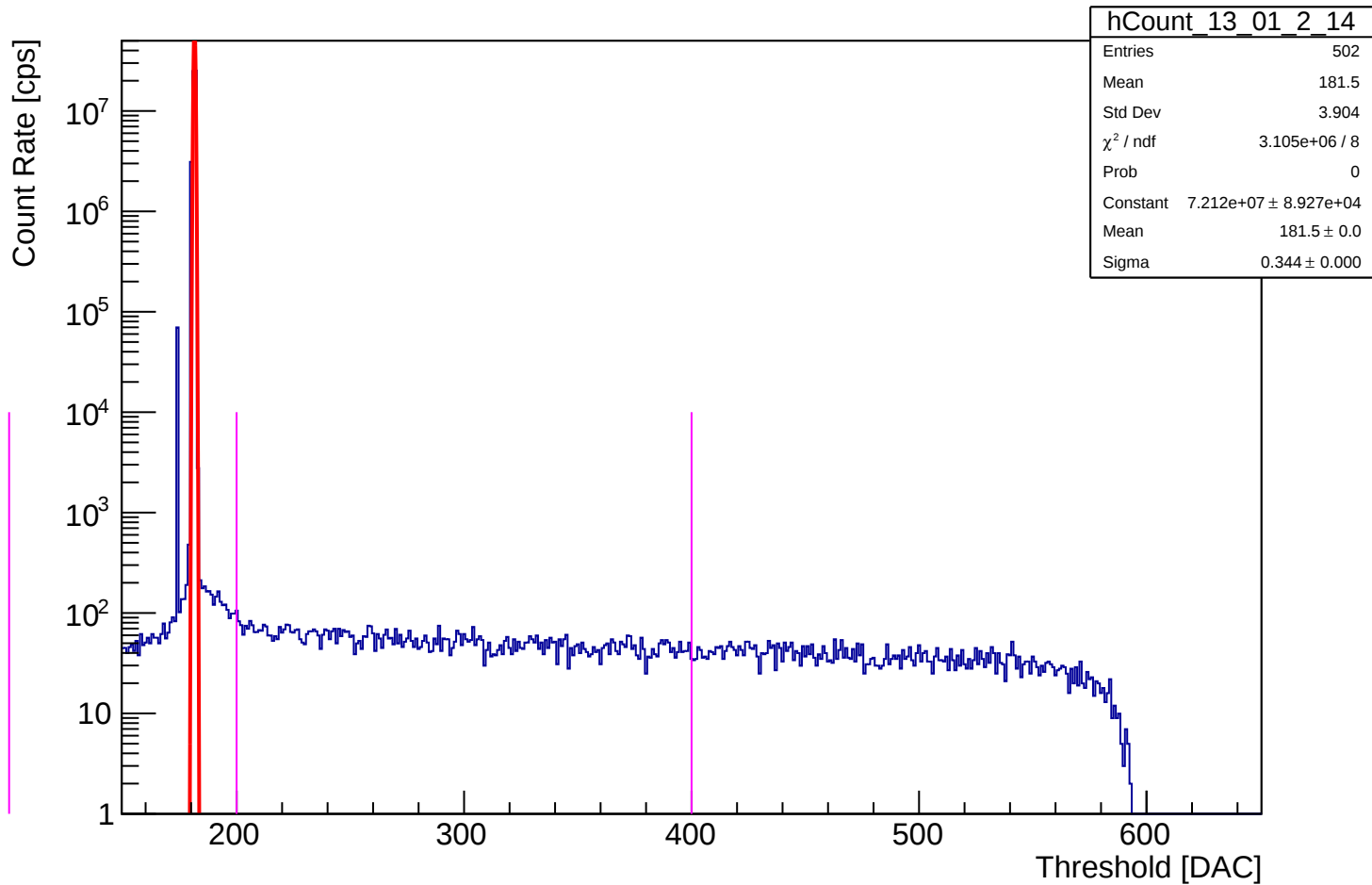
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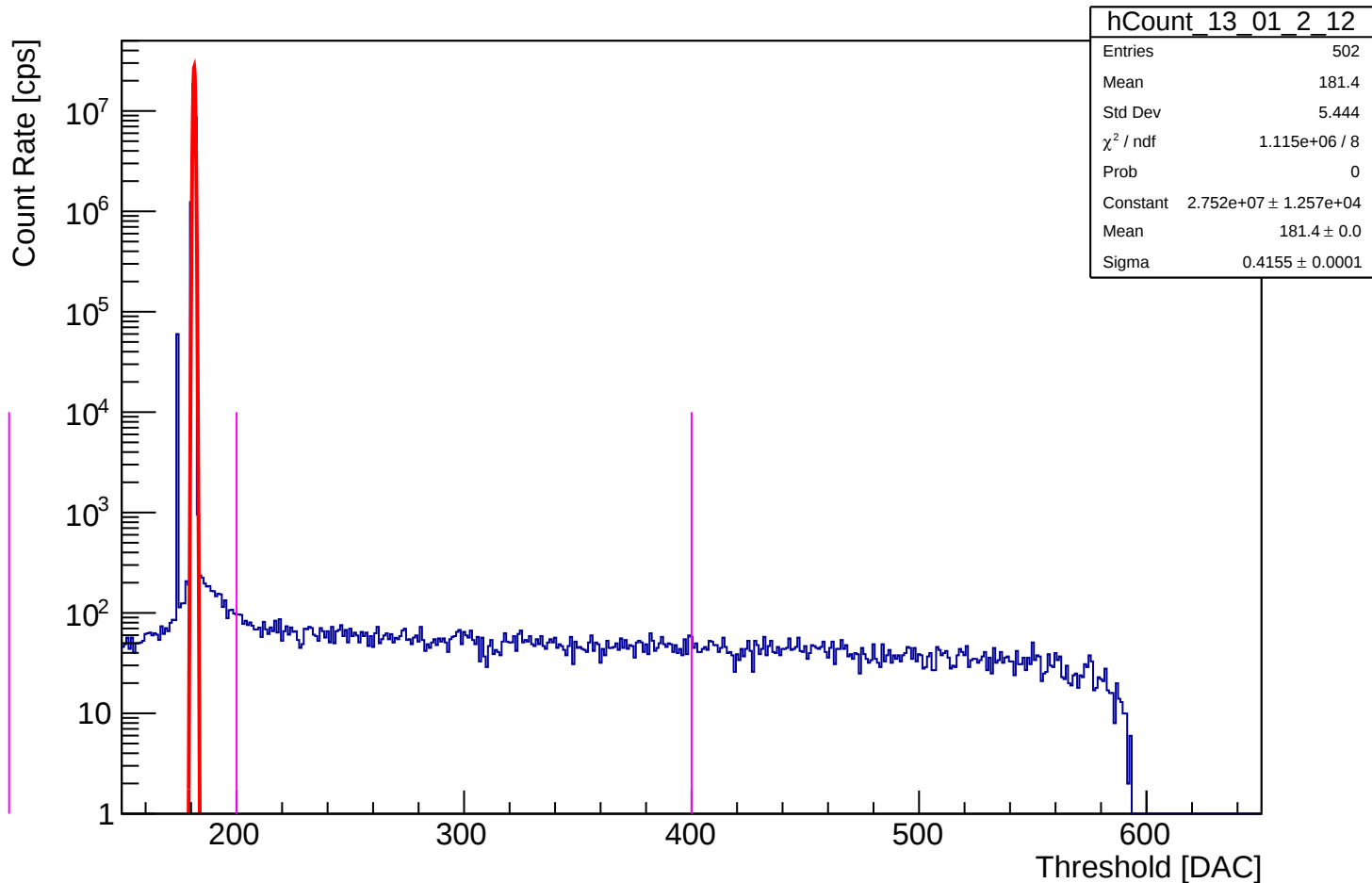
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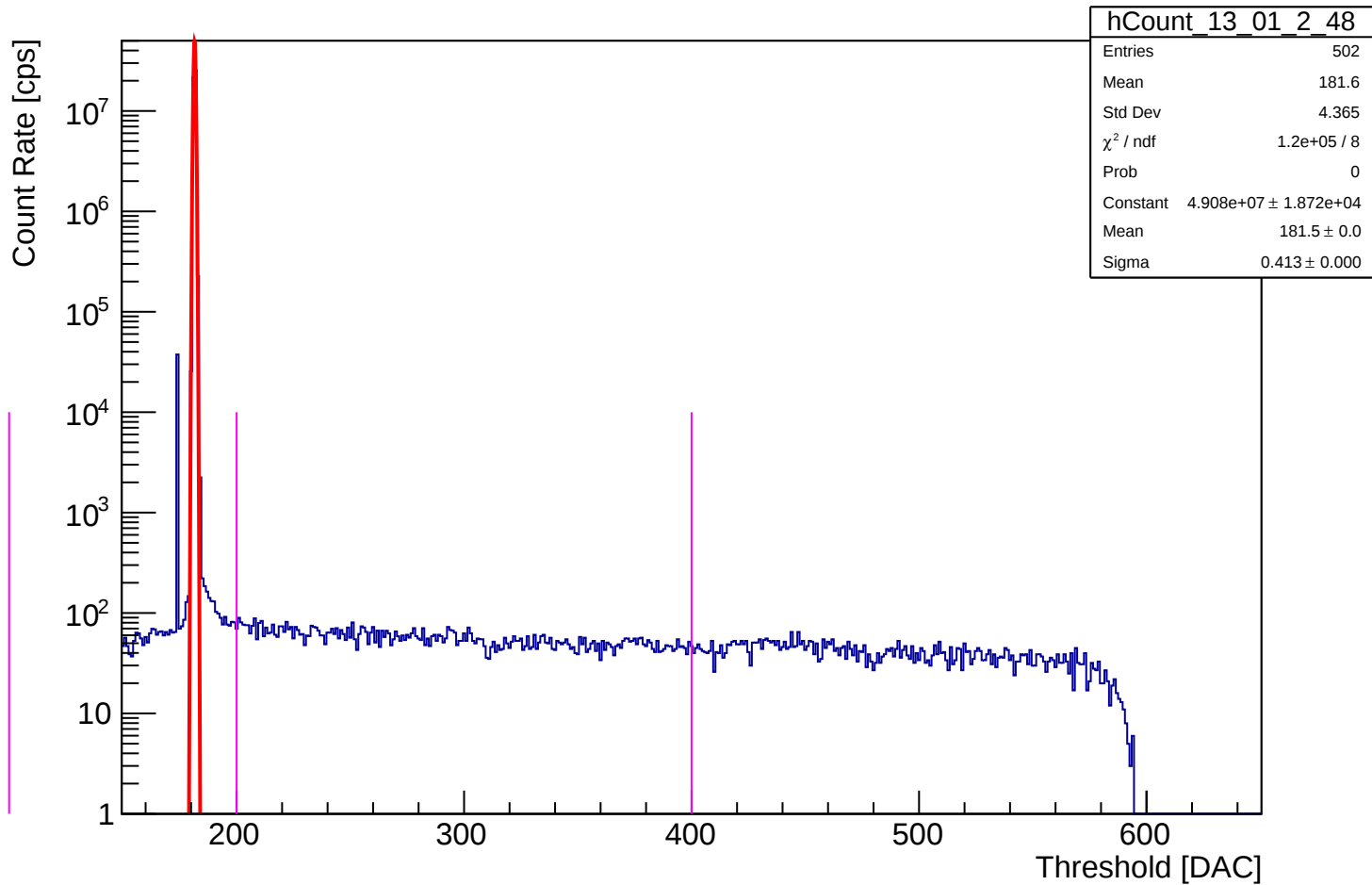
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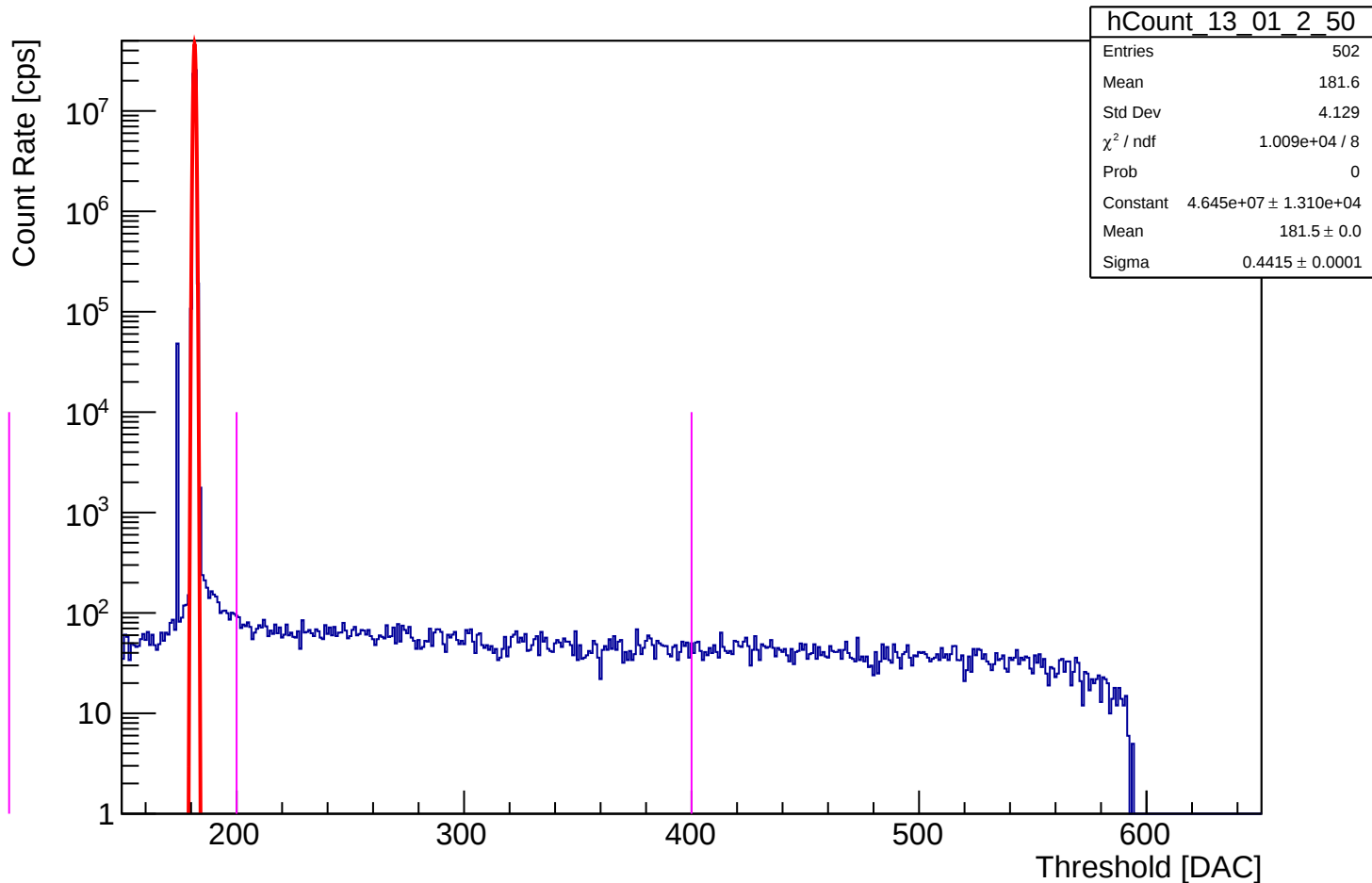
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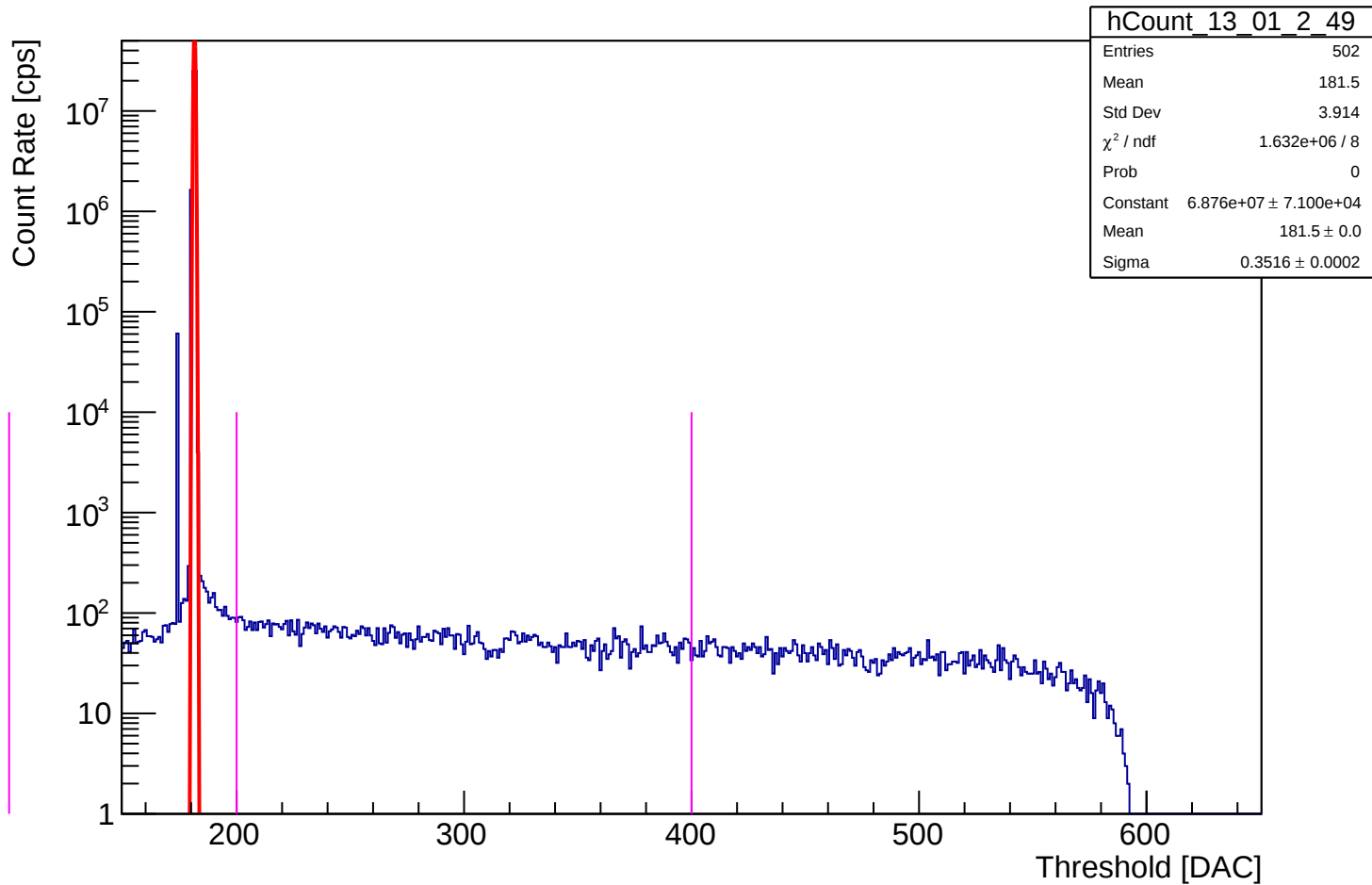
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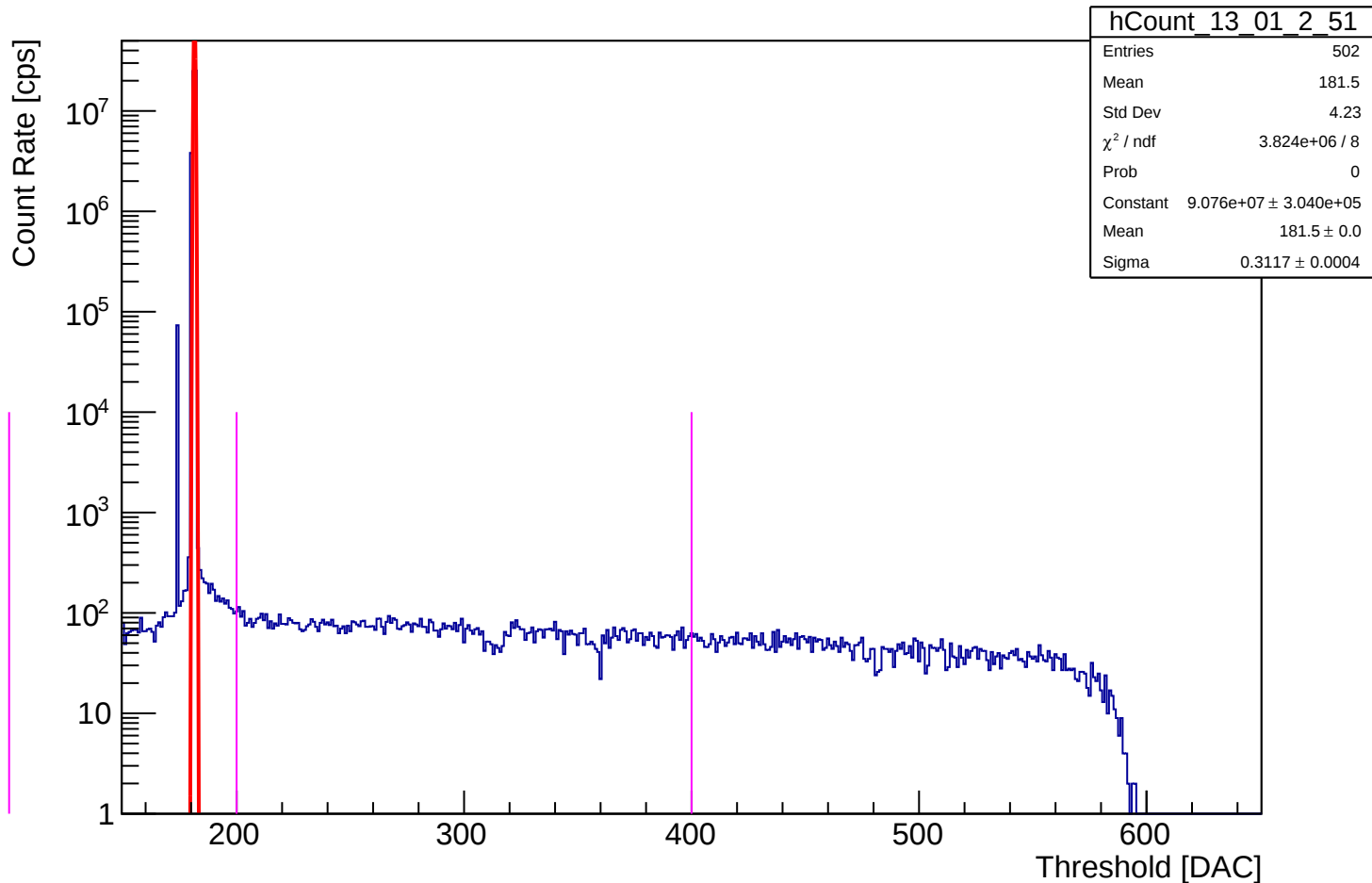
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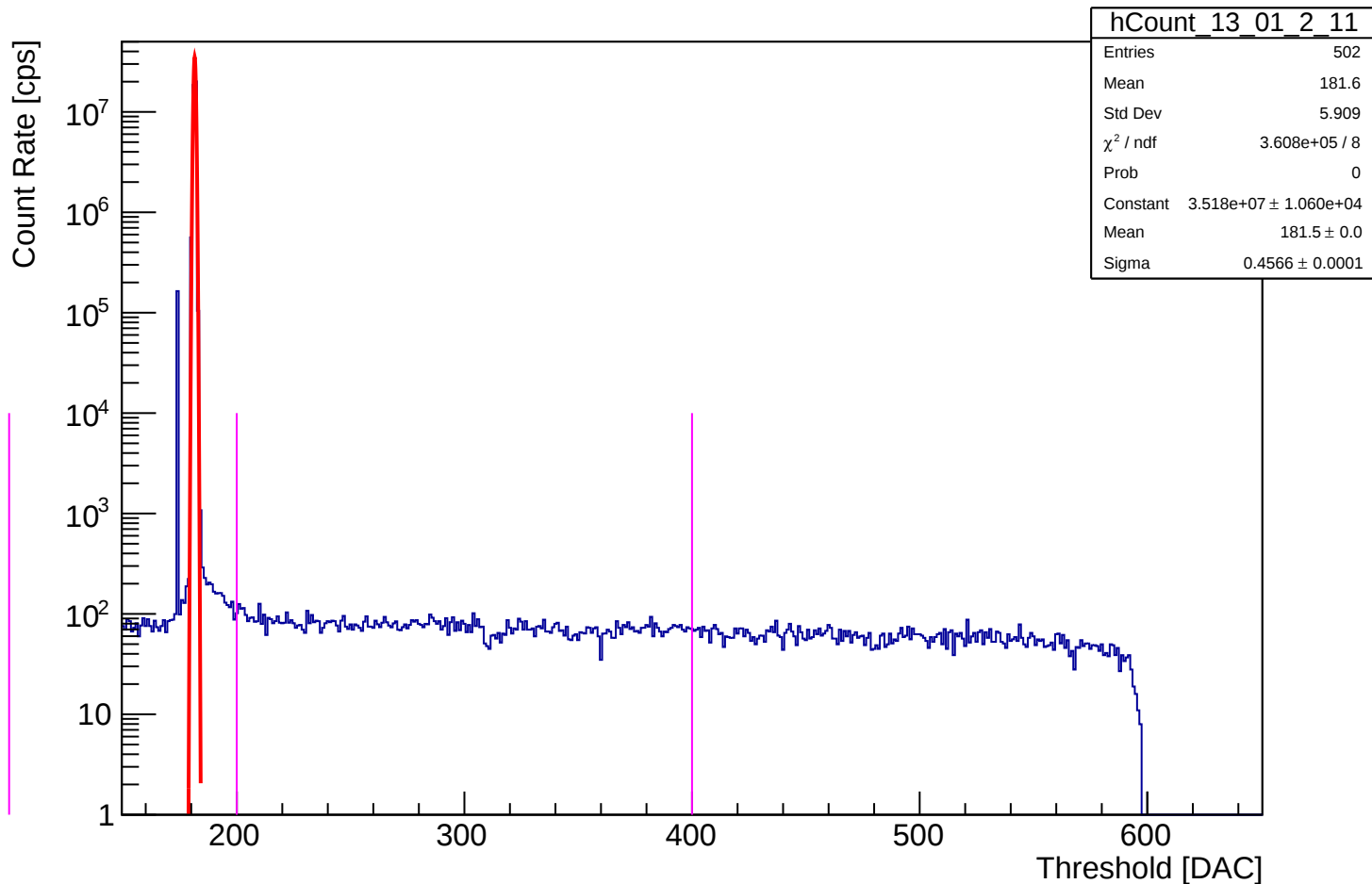
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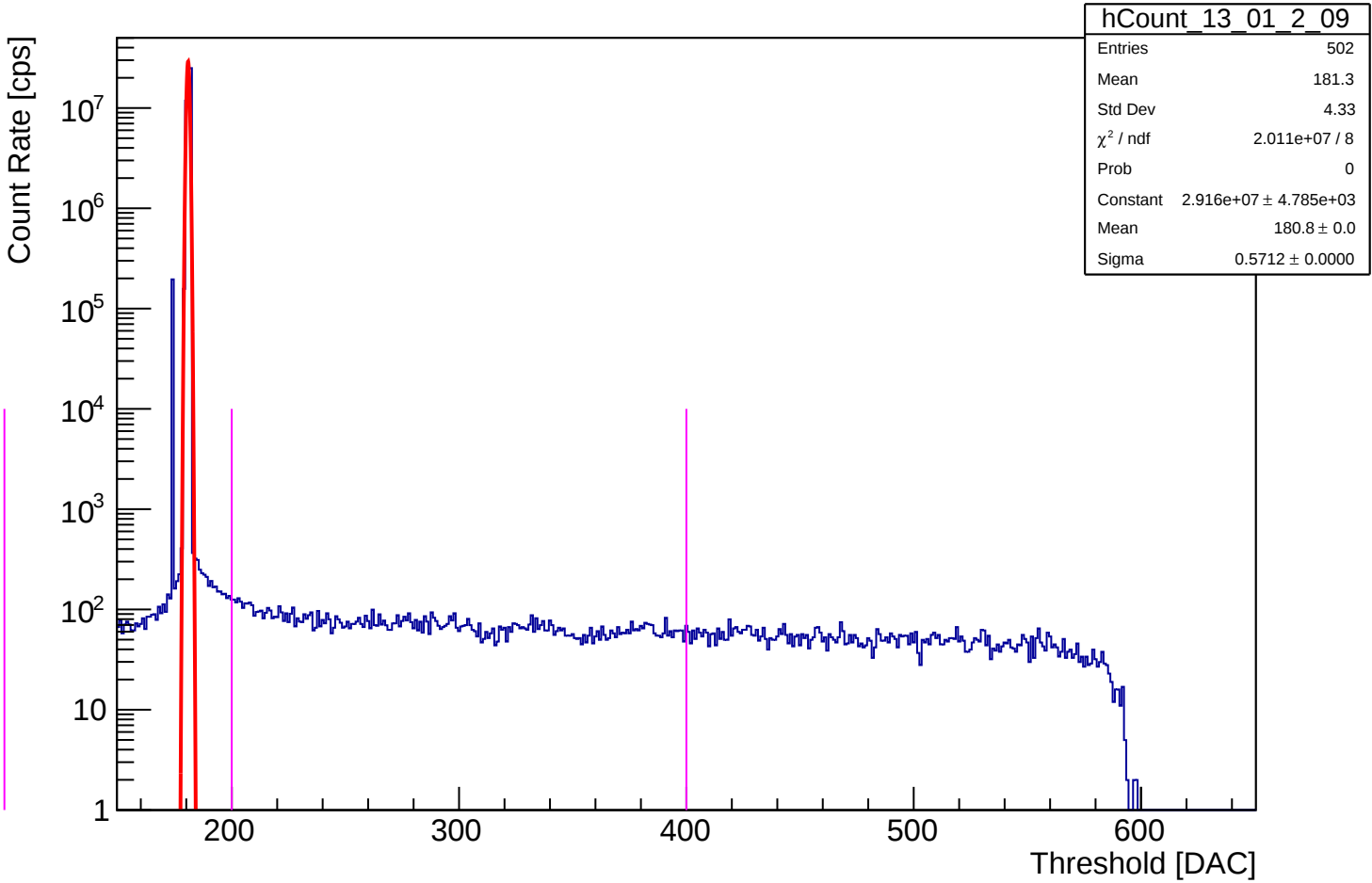


Row 1 Tile 1 Pmt 6 Pixel 40 Slot 13 Fiber 1 Asic 2 Channel 51

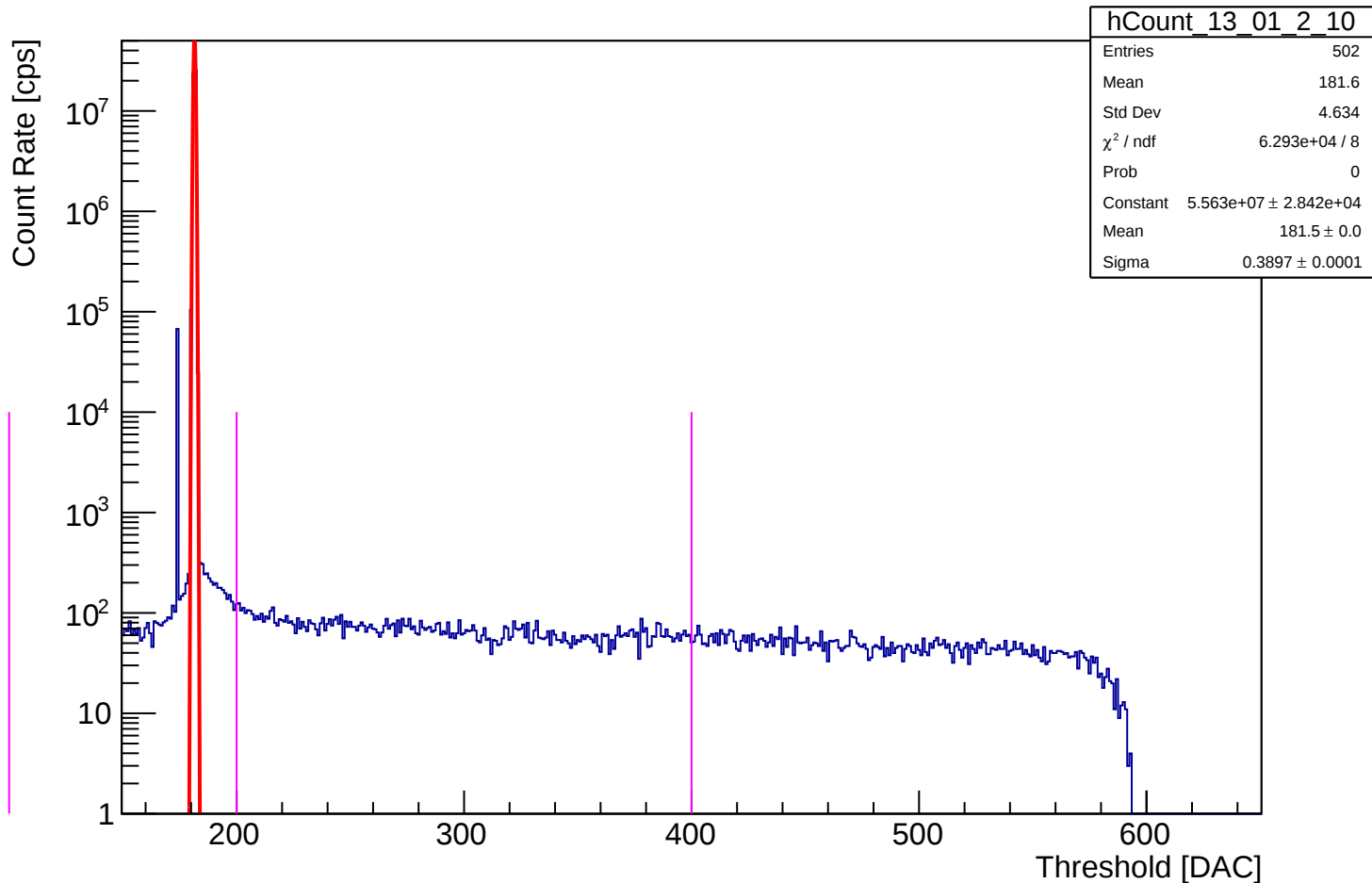


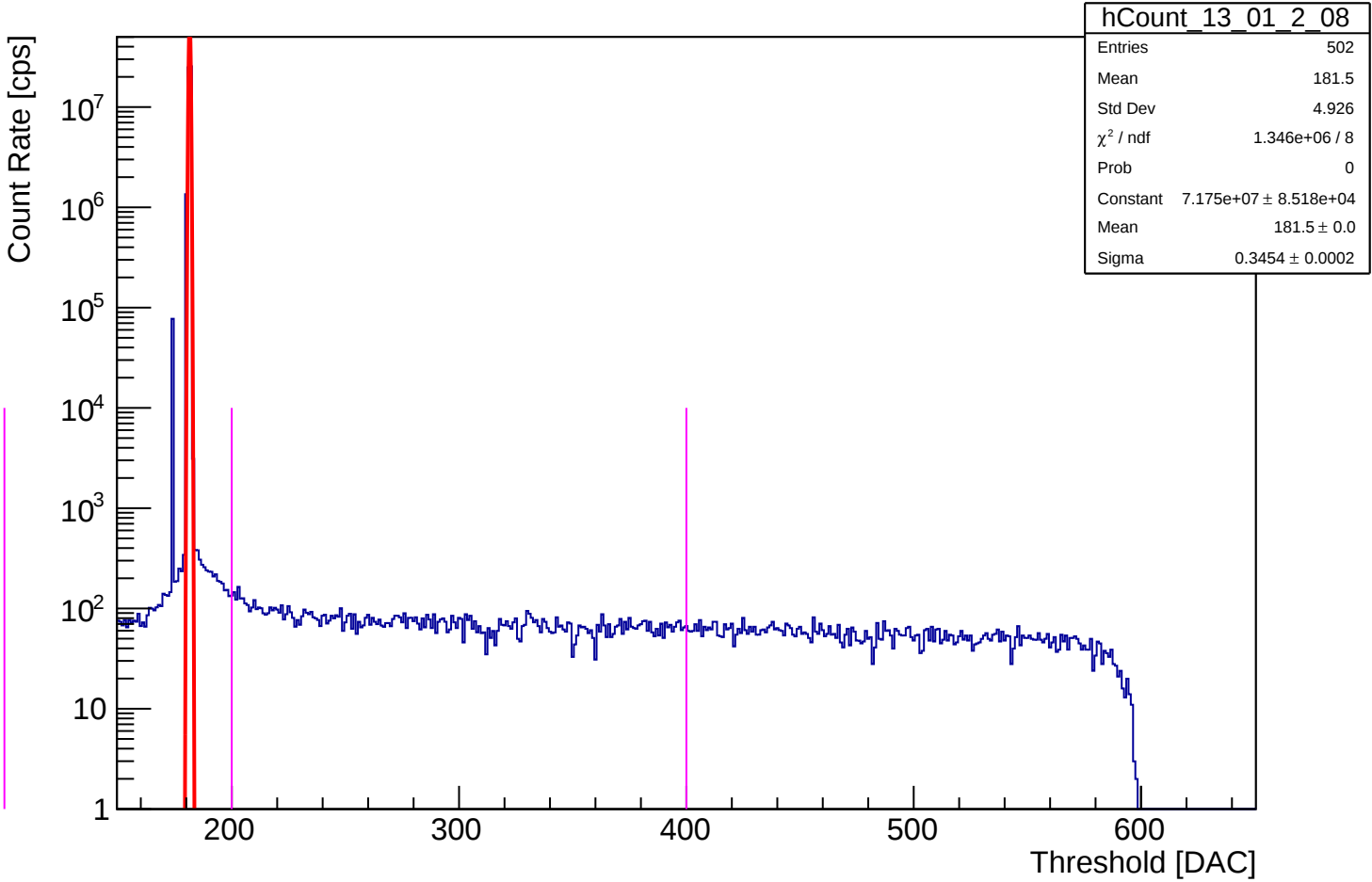
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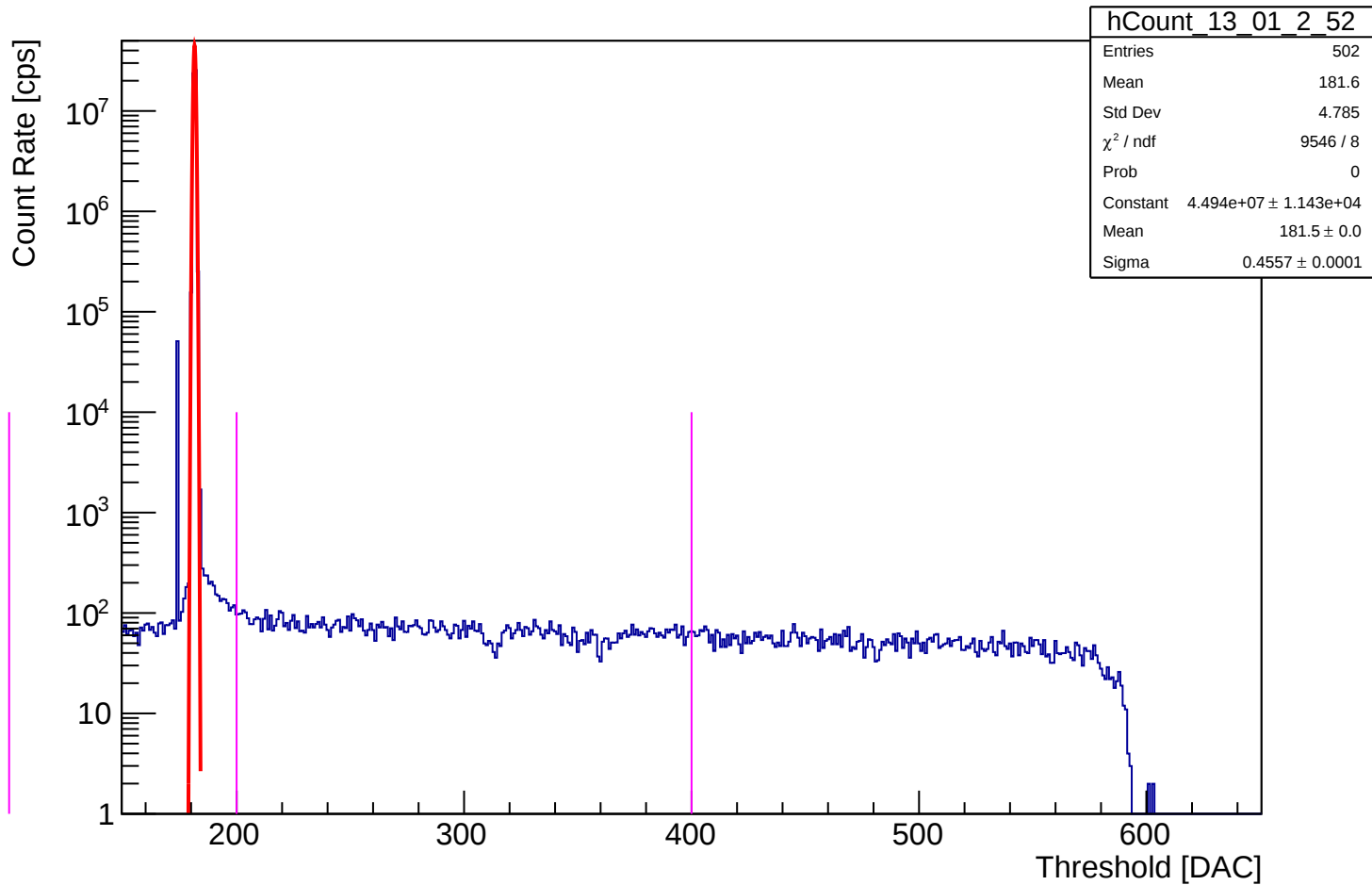


Row 1 Tile 1 Pmt 6 Pixel 43 Slot 13 Fiber 1 Asic 2 Channel 10

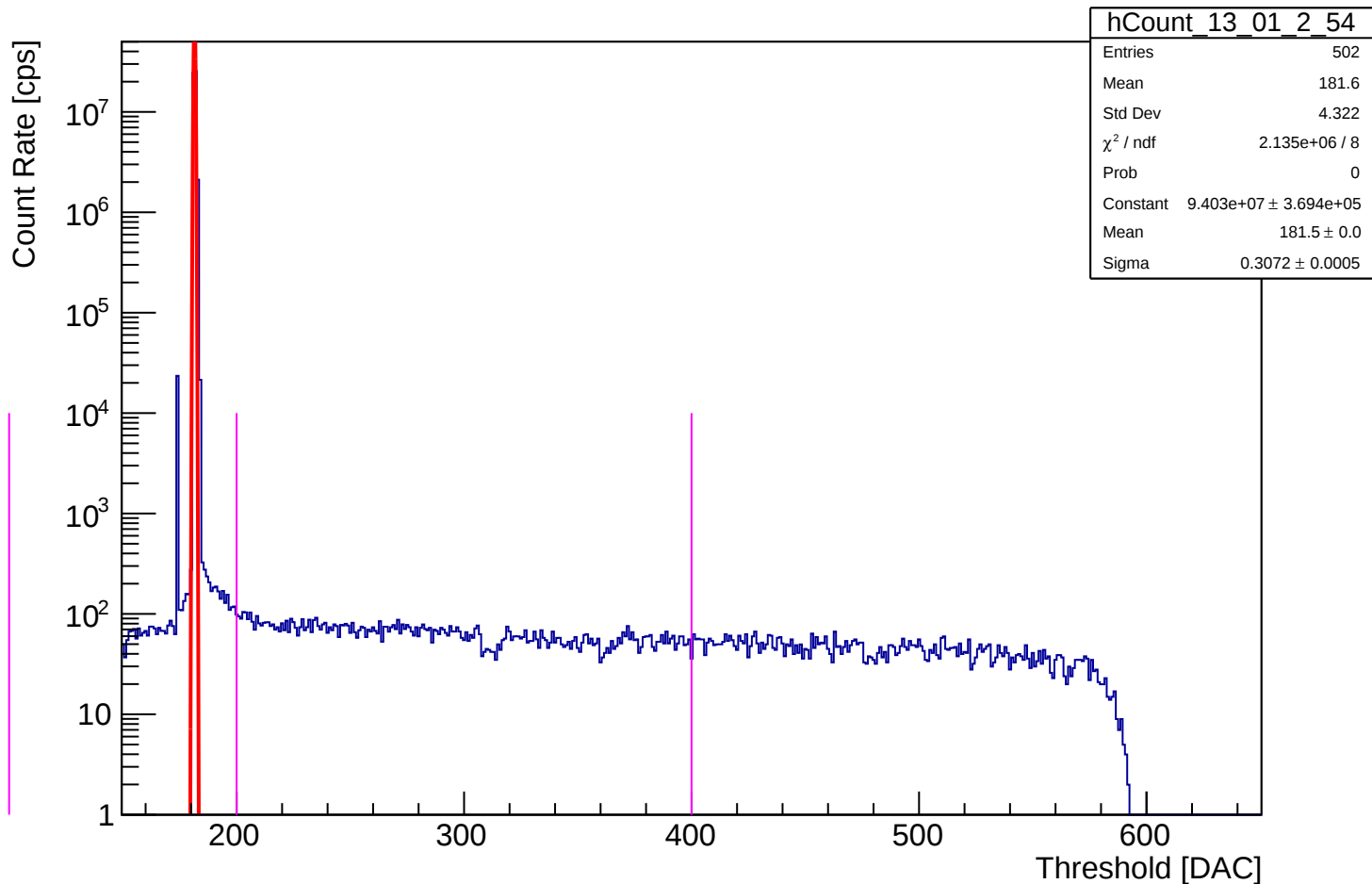




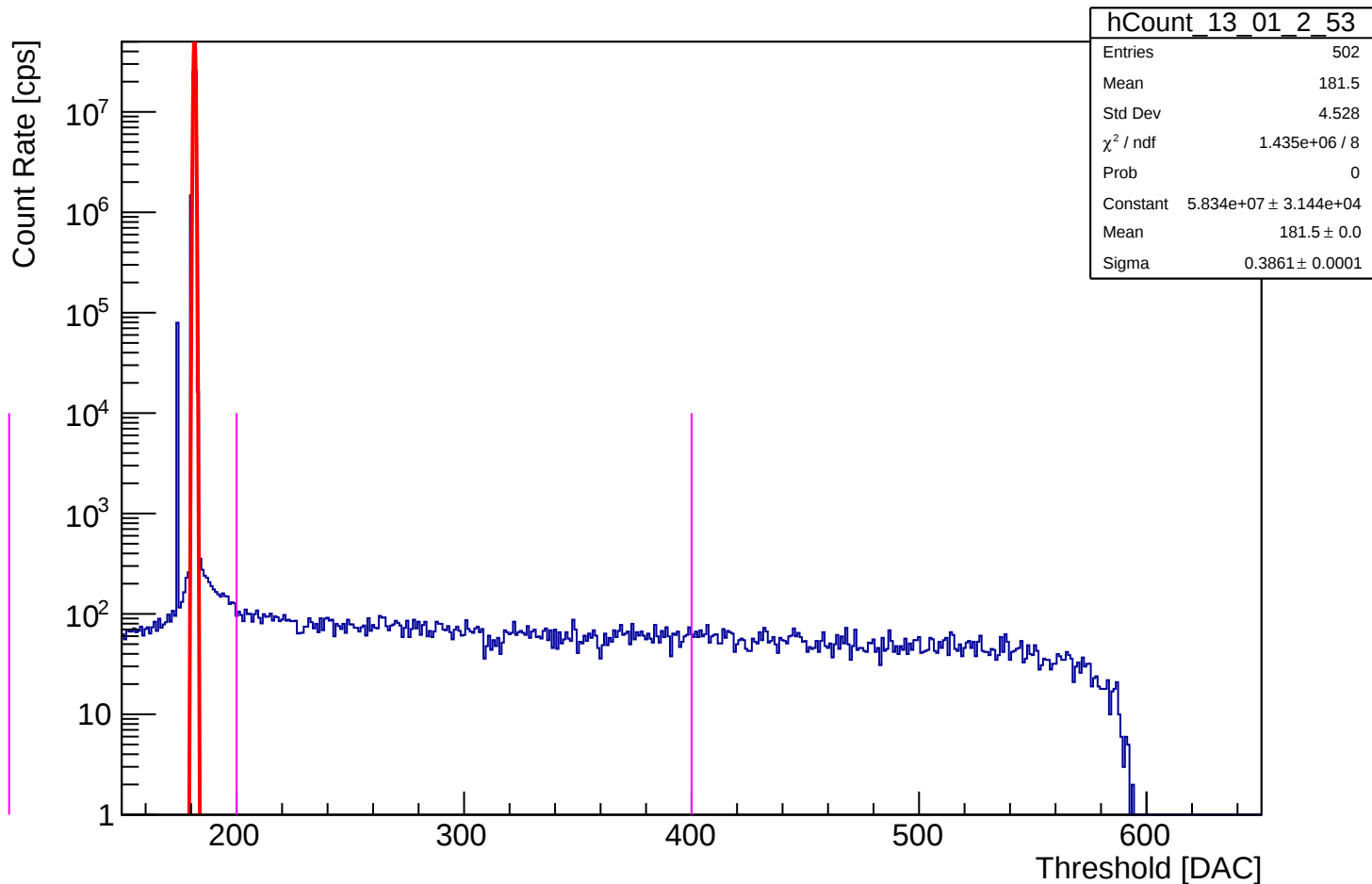
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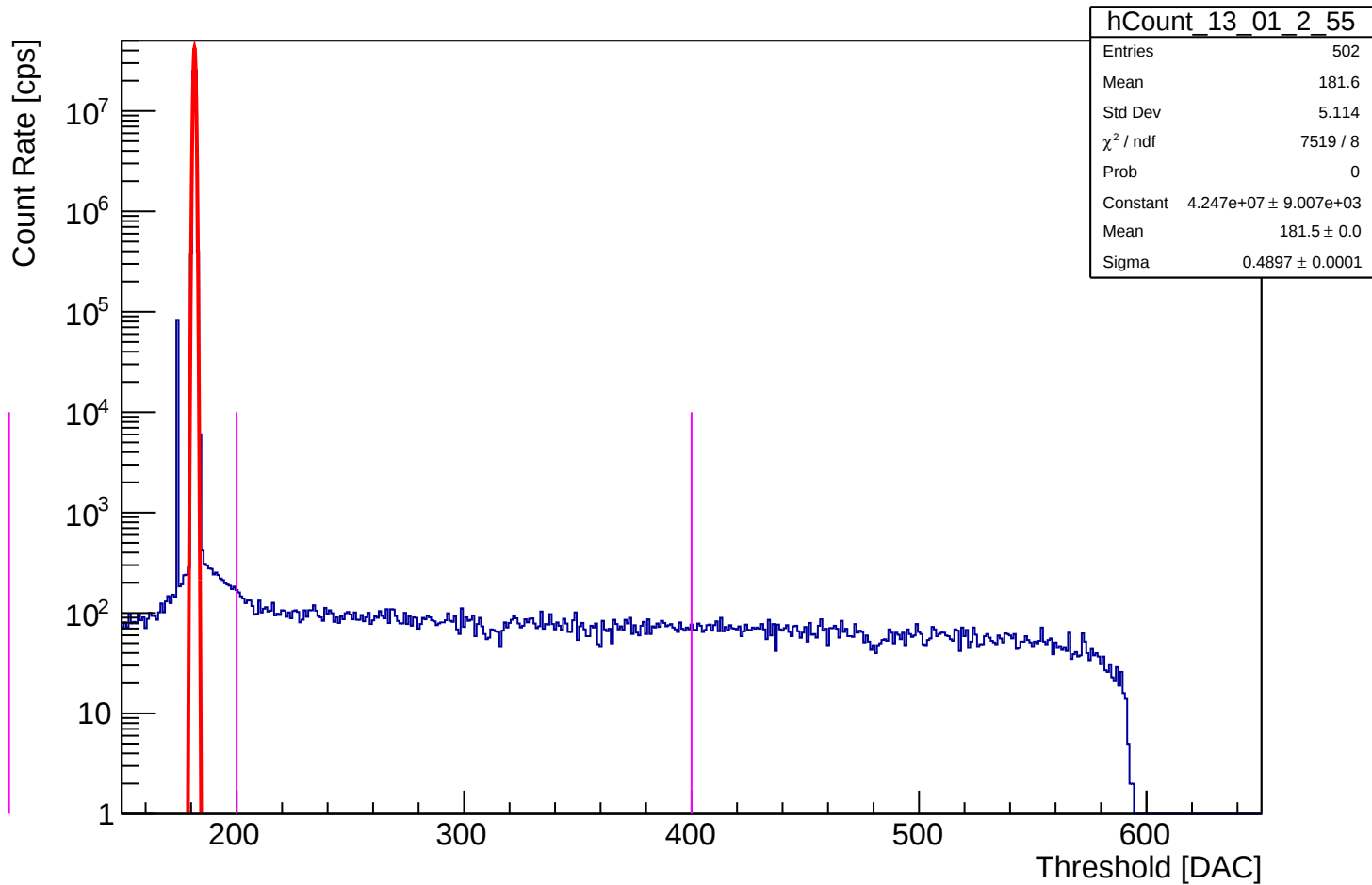
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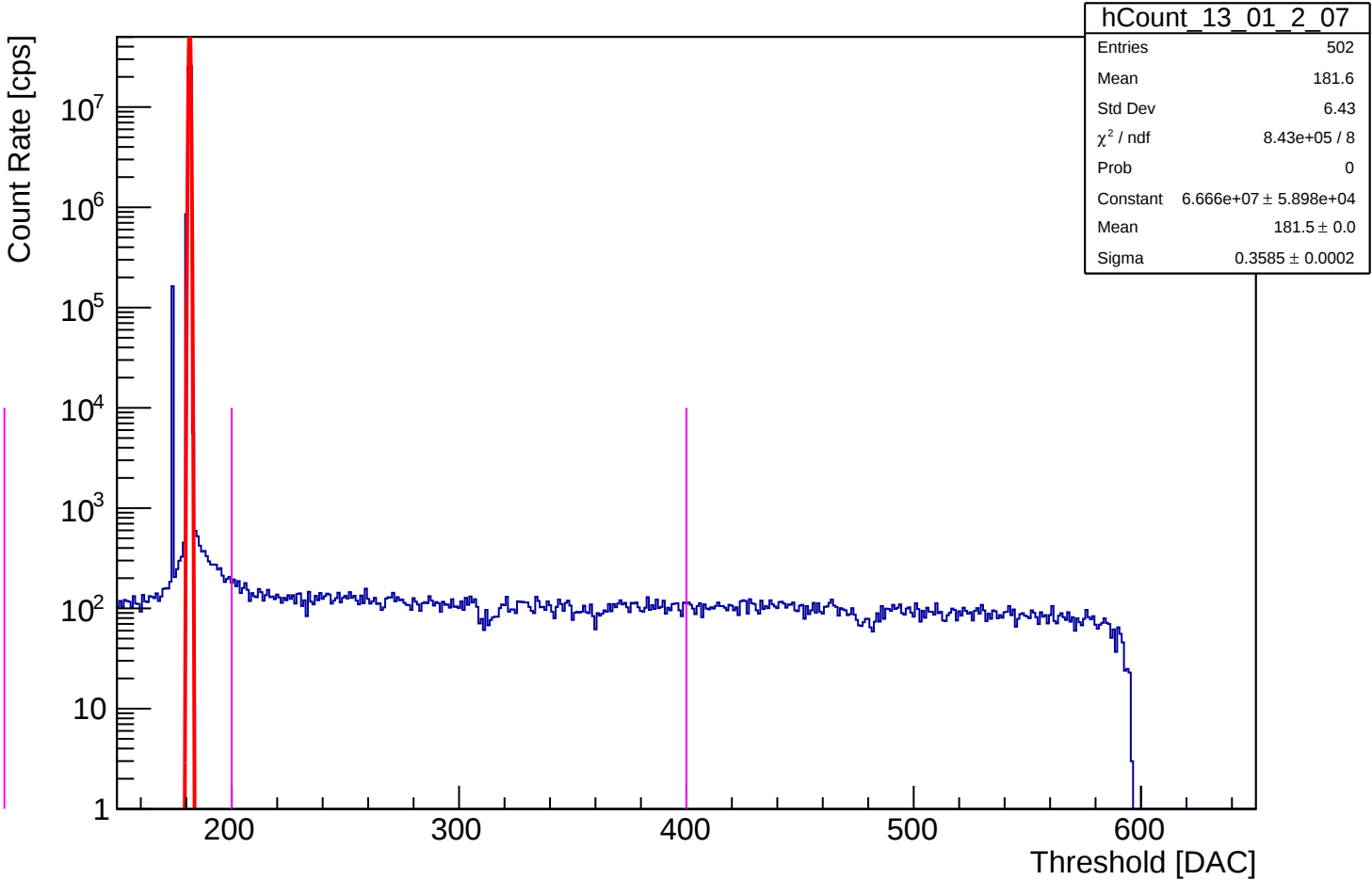


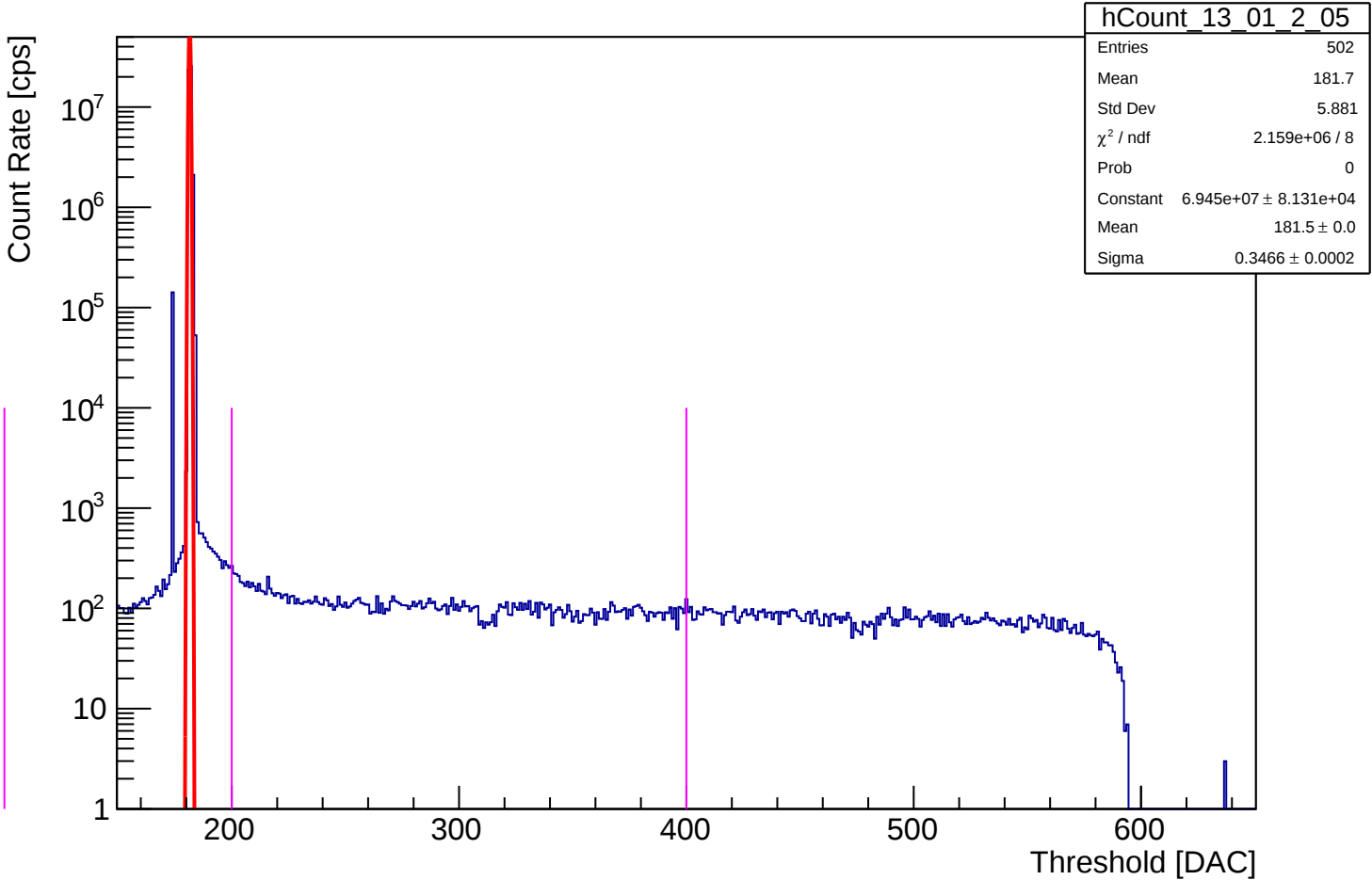
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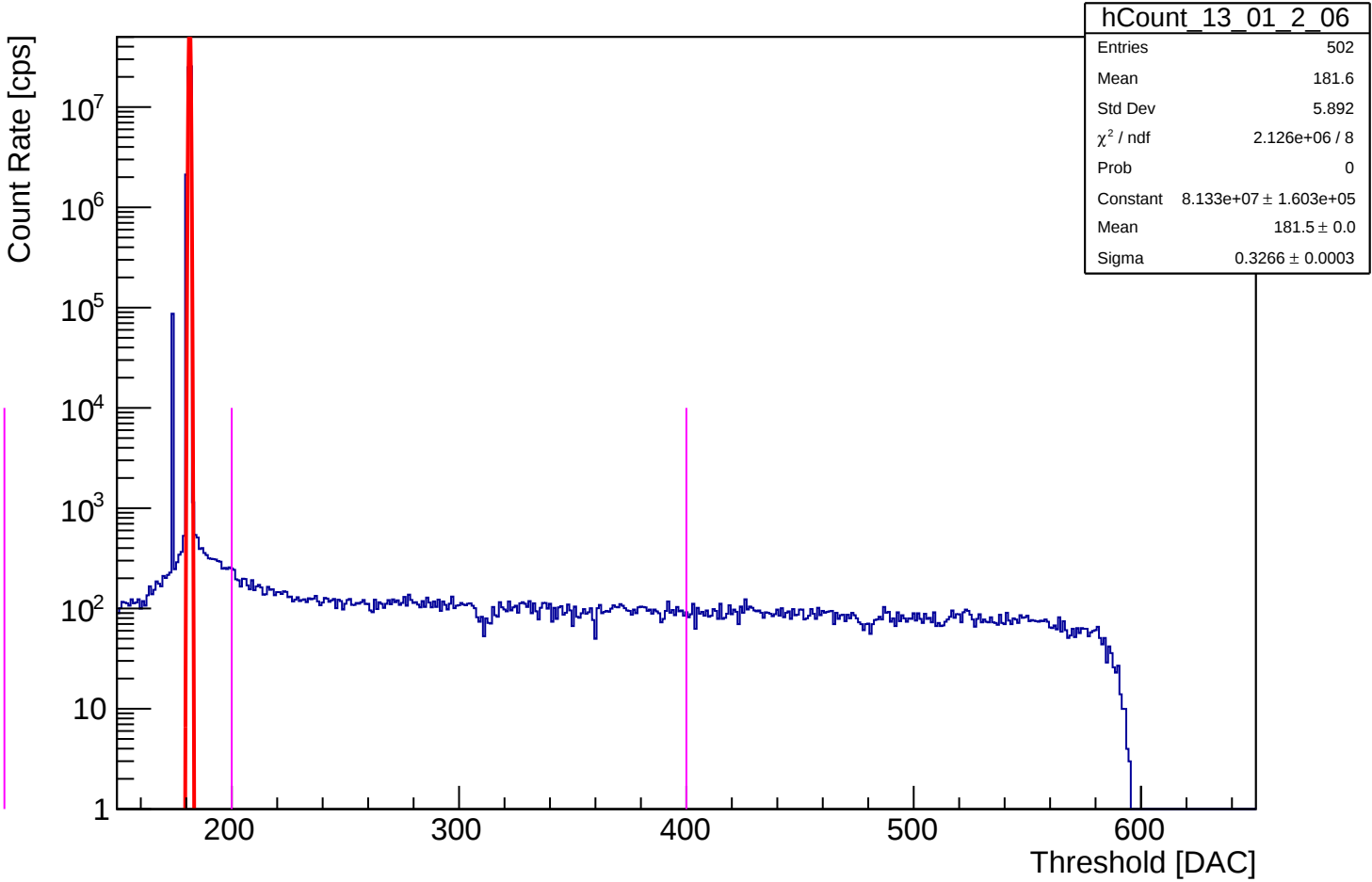


Row 1 Tile 1 Pmt 6 Pixel 48 Slot 13 Fiber 1 Asic 2 Channel 55

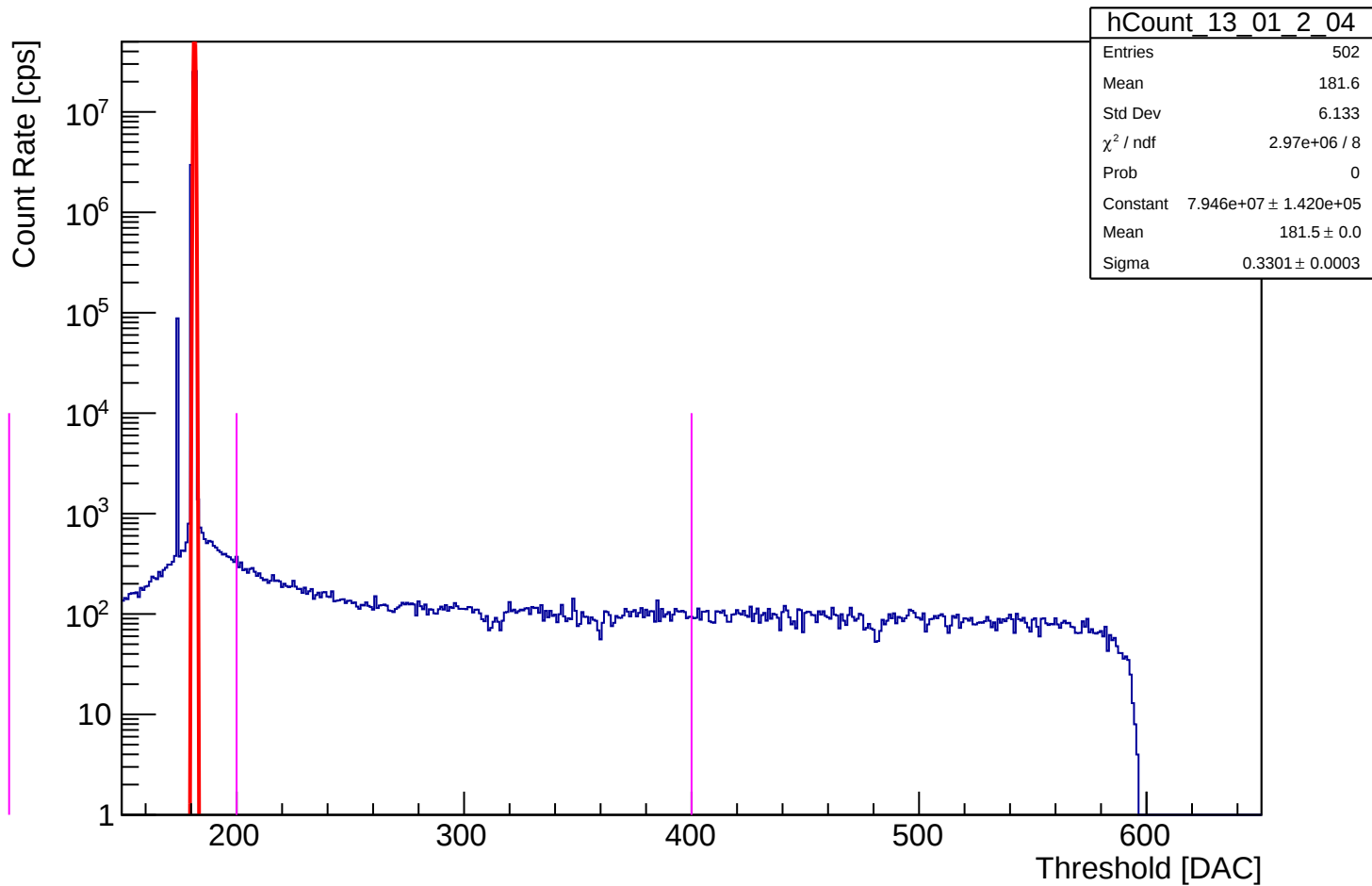




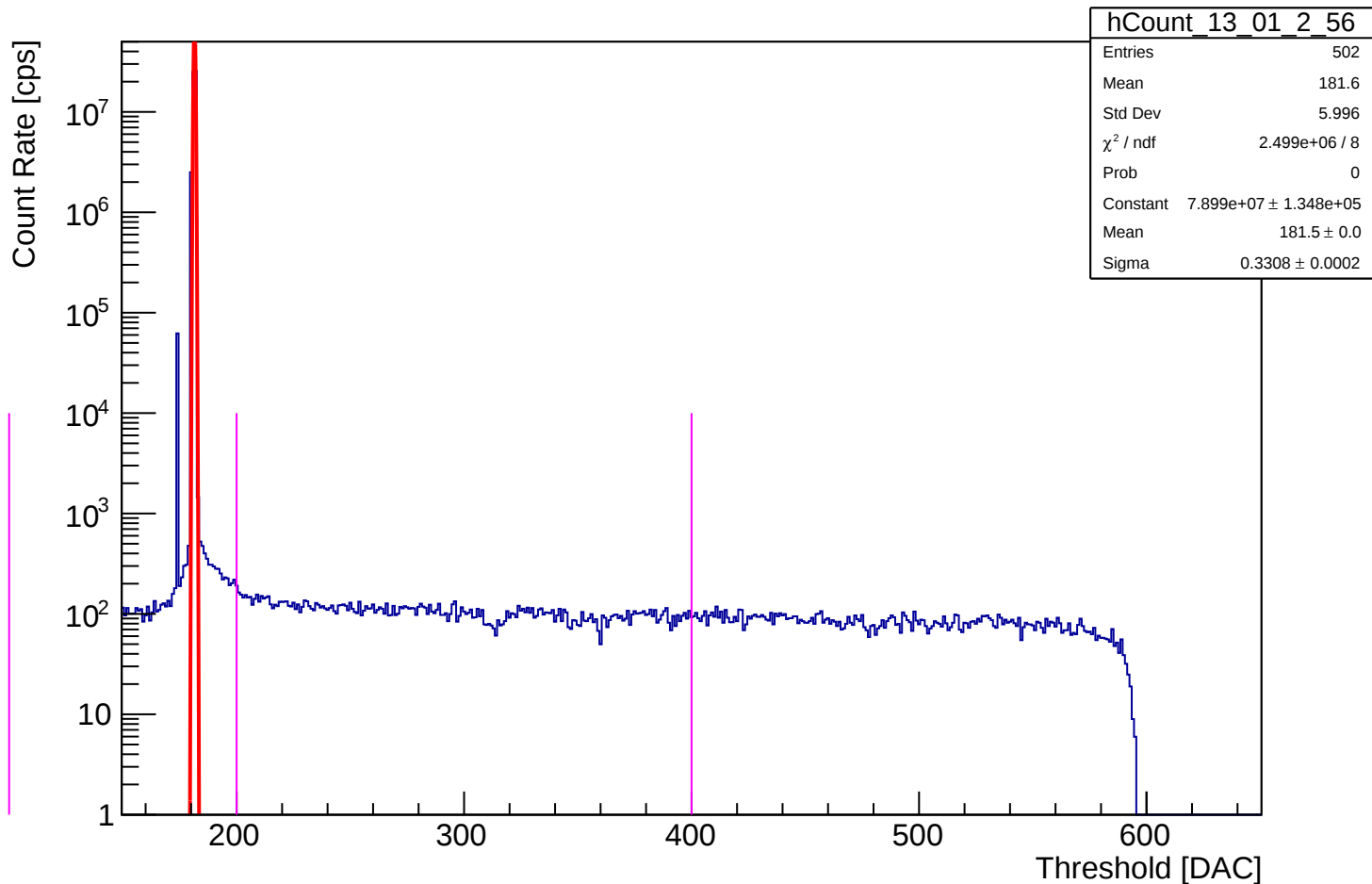




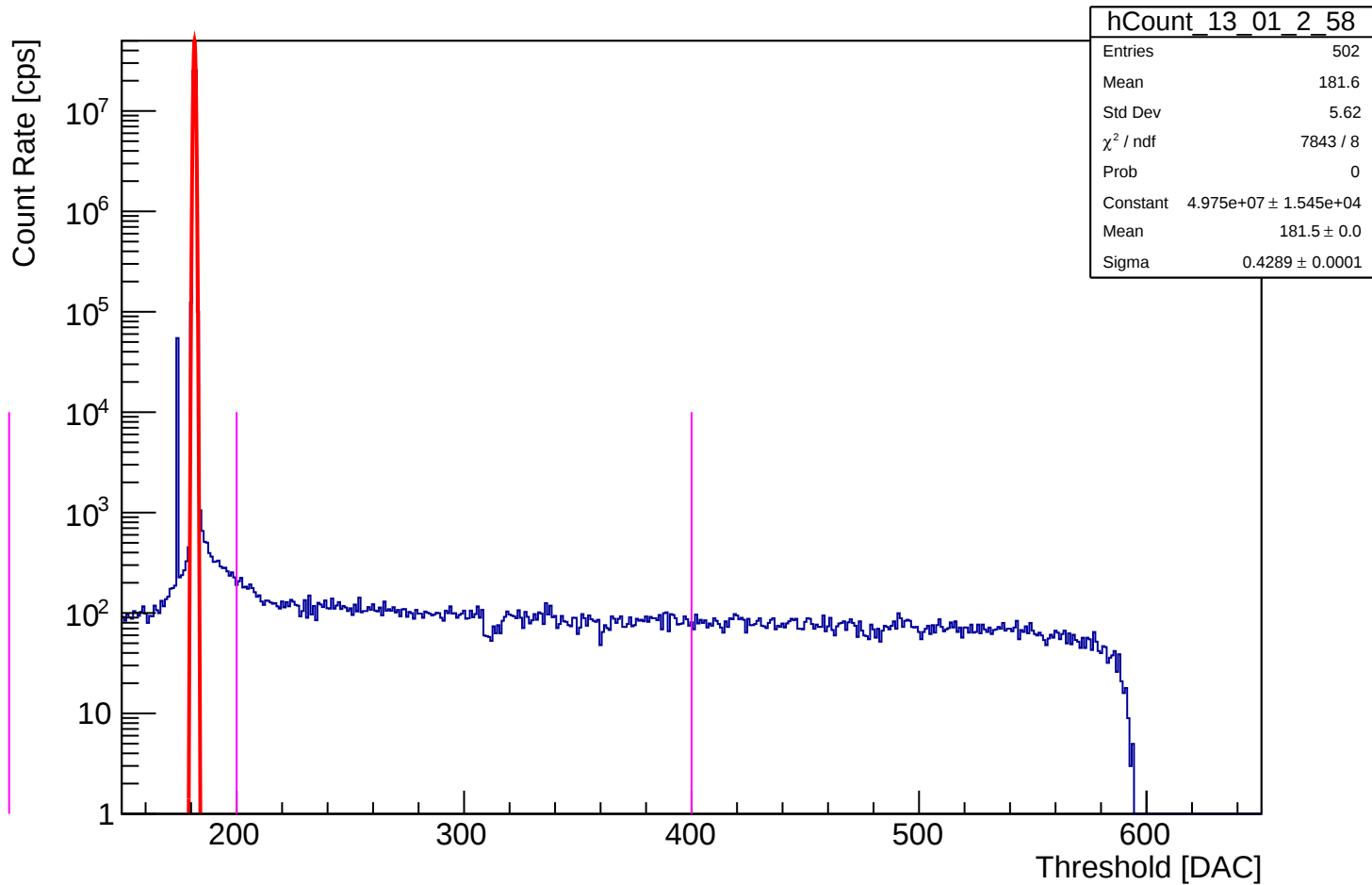
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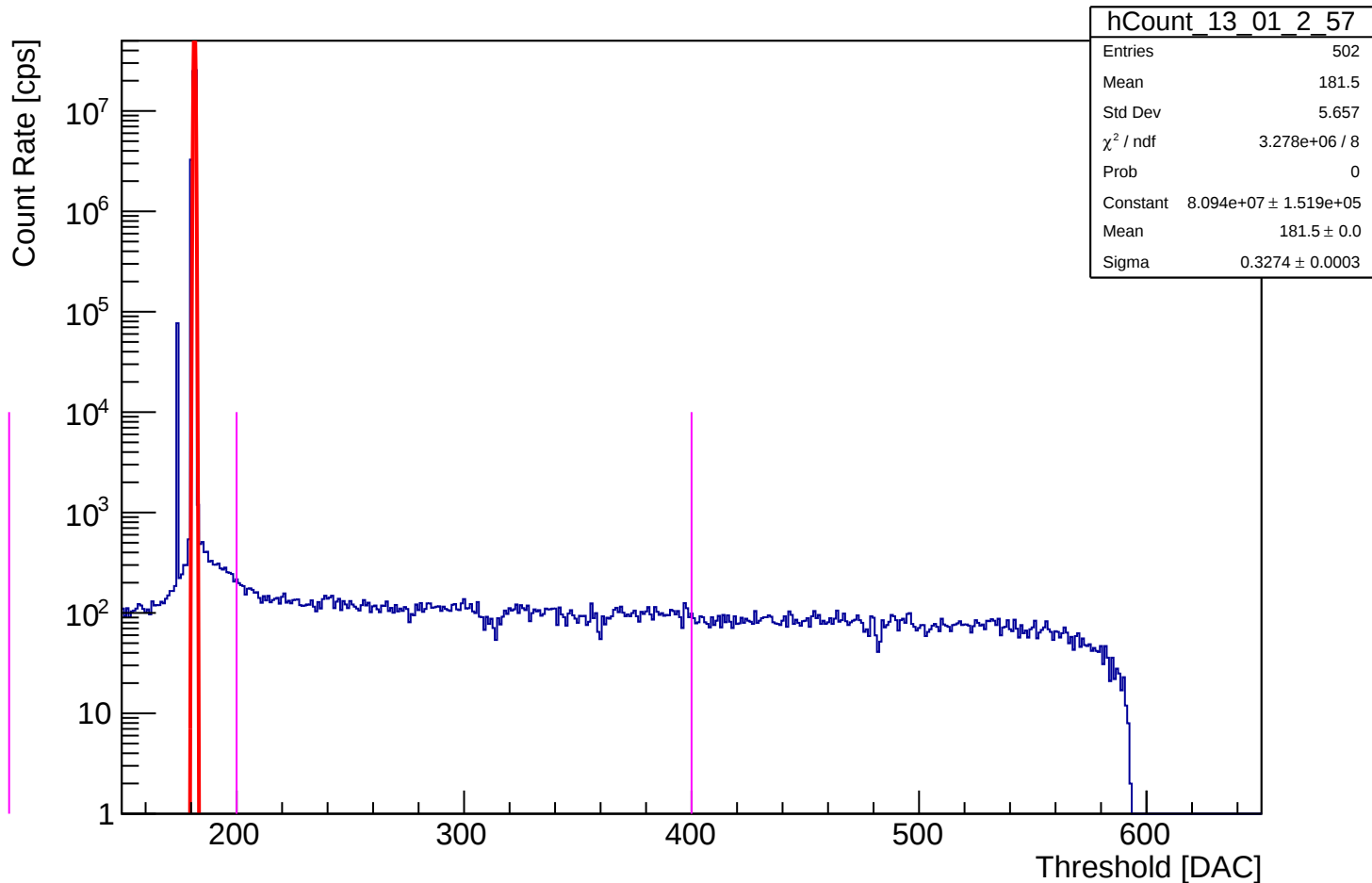
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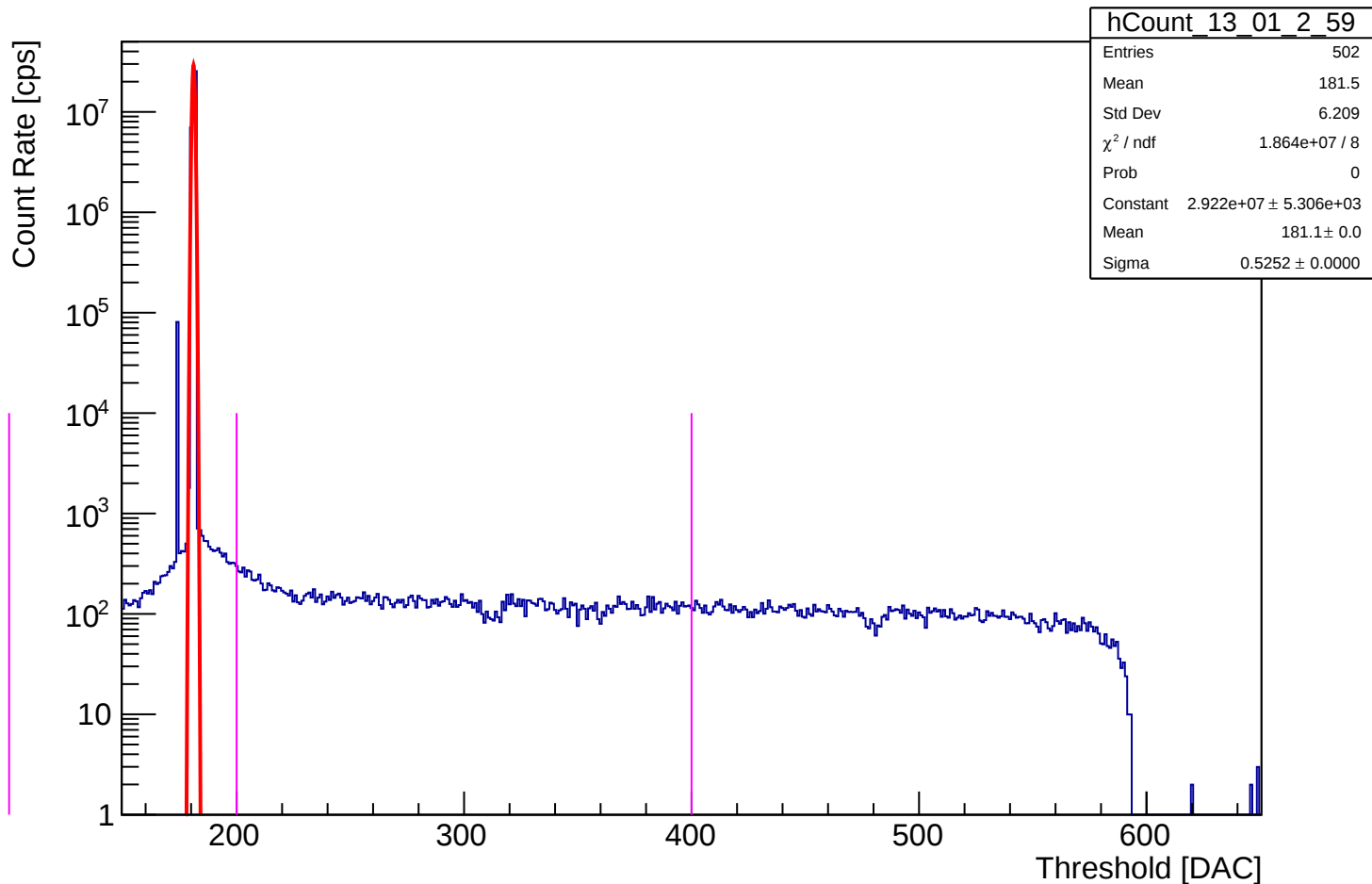
Row 1 Tile 1 Pmt 6 Pixel 54 Slot 13 Fiber 1 Asic 2 Channel 58

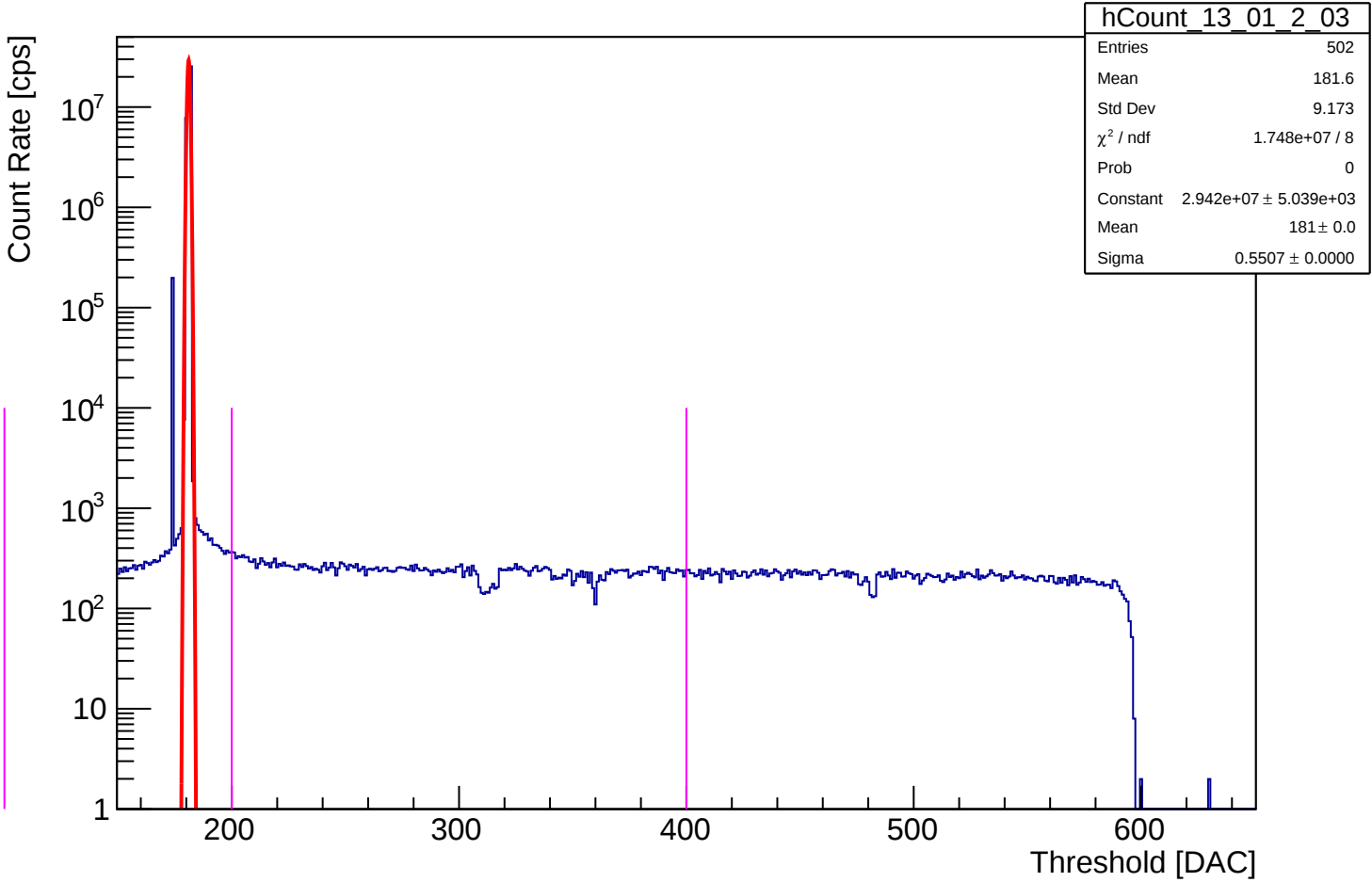


Row 1 Tile 1 Pmt 6 Pixel 55 Slot 13 Fiber 1 Asic 2 Channel 57

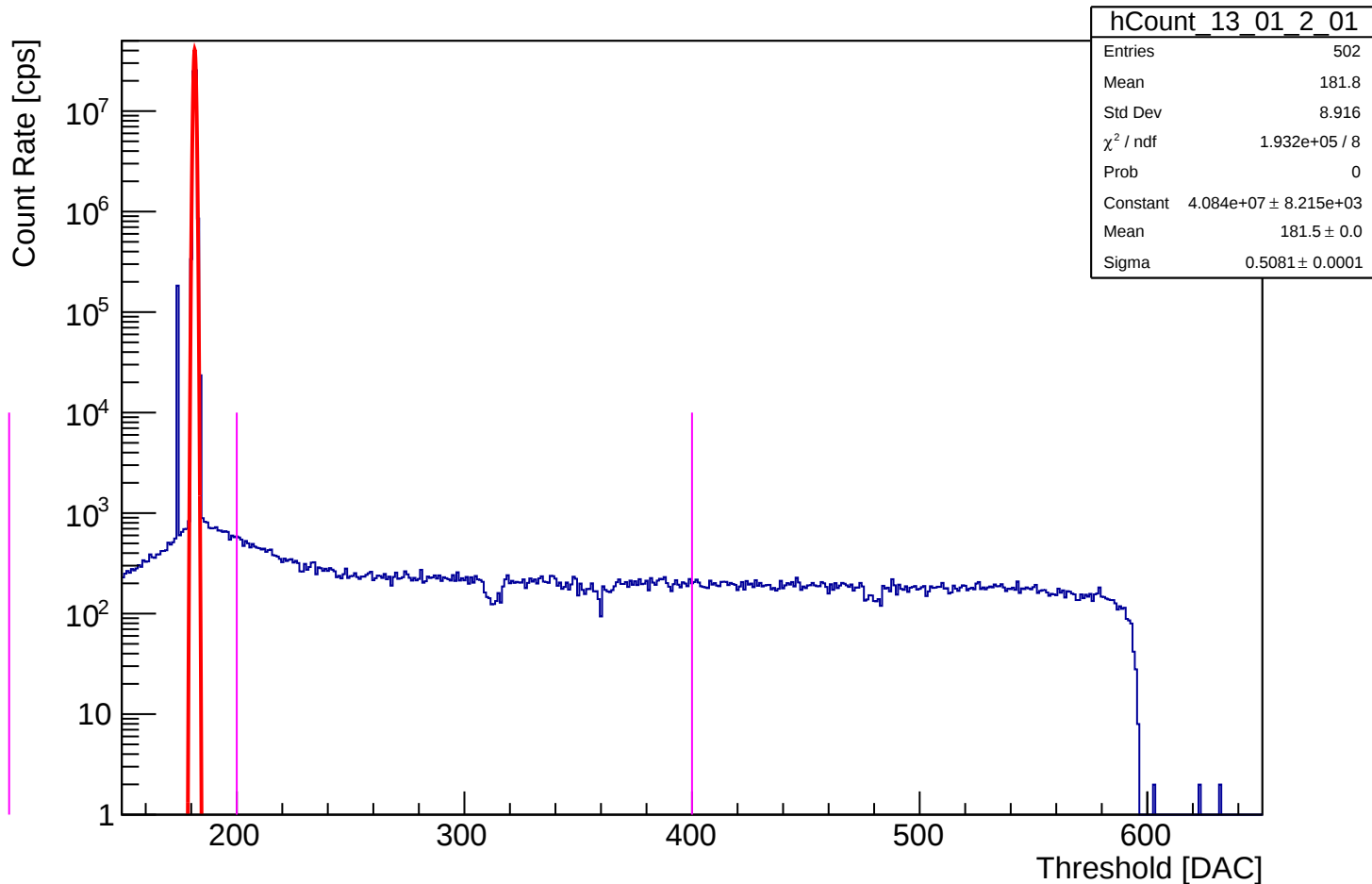


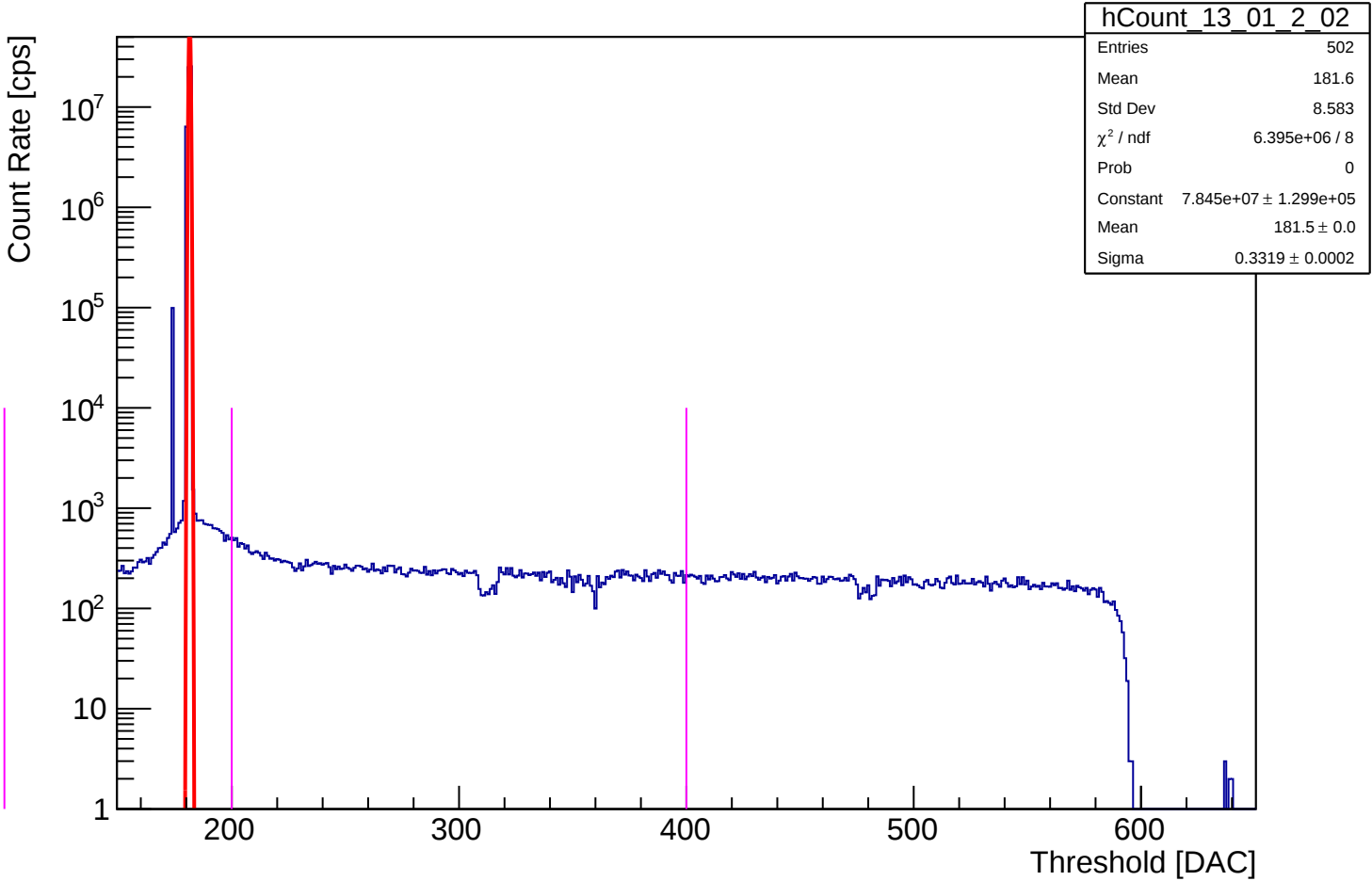
Row 1 Tile 1 Pmt 6 Pixel 56 Slot 13 Fiber 1 Asic 2 Channel 59

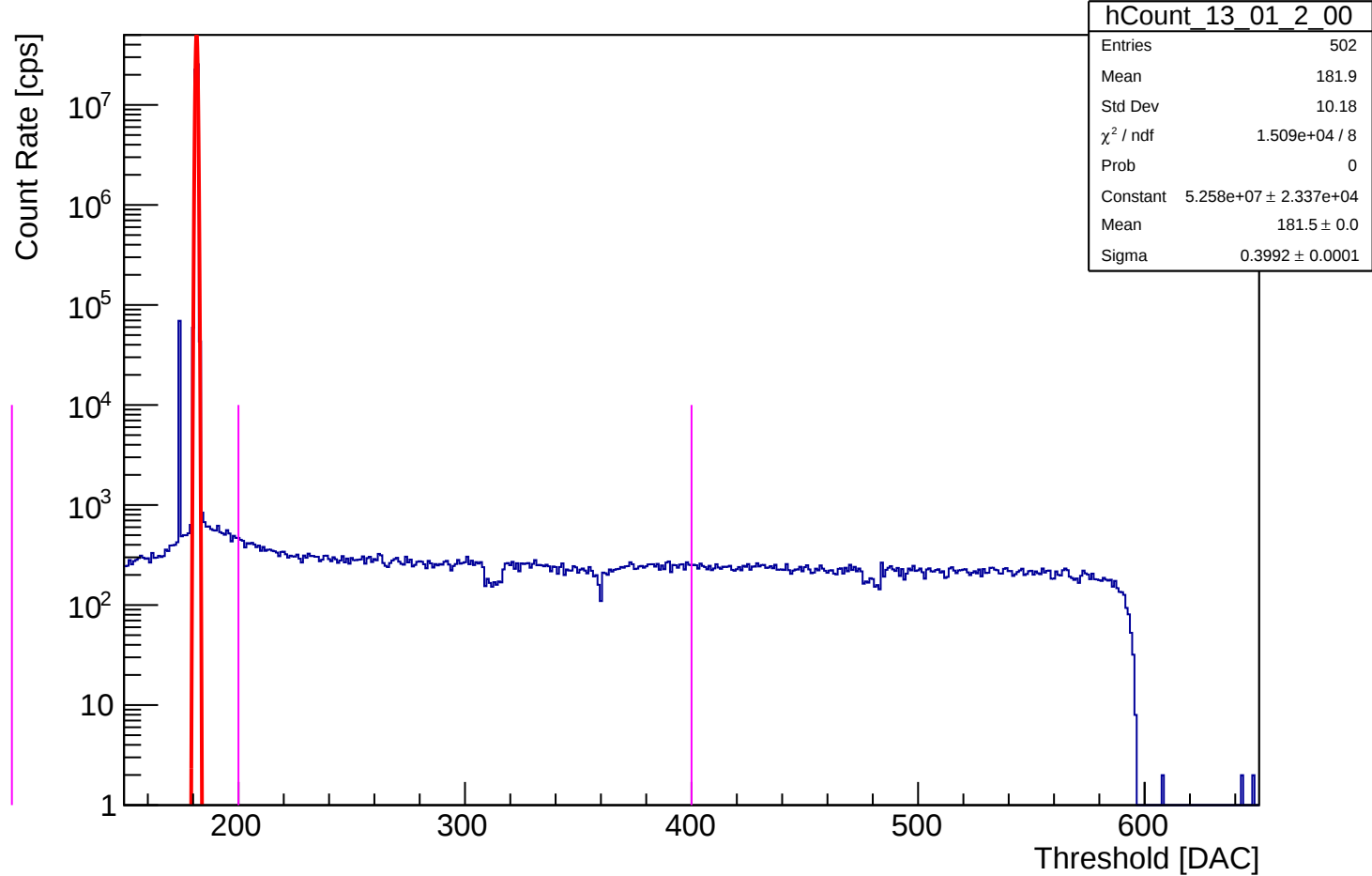




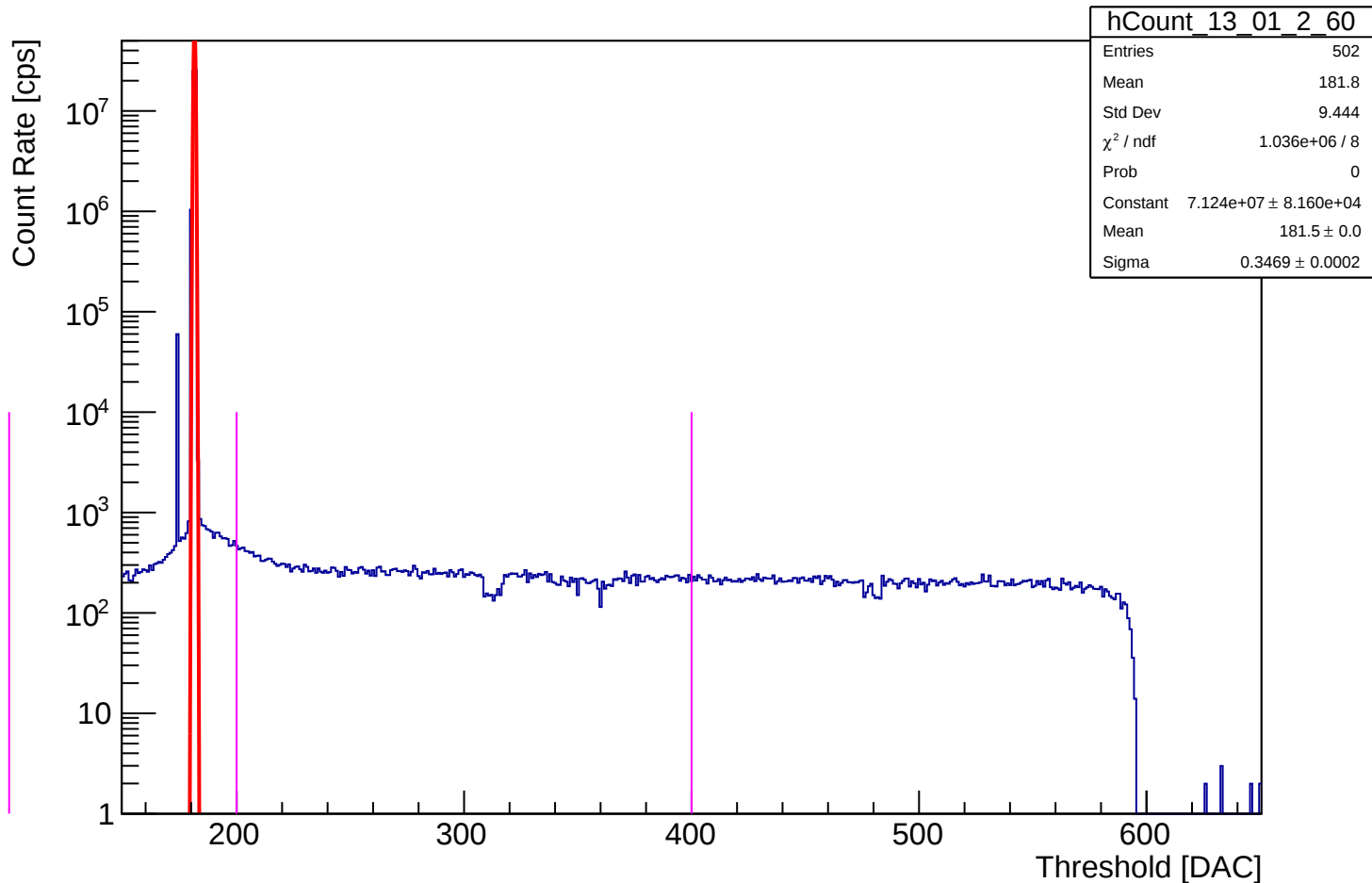
Row 1 Tile 1 Pmt 6 Pixel 58 Slot 13 Fiber 1 Asic 2 Channel 1



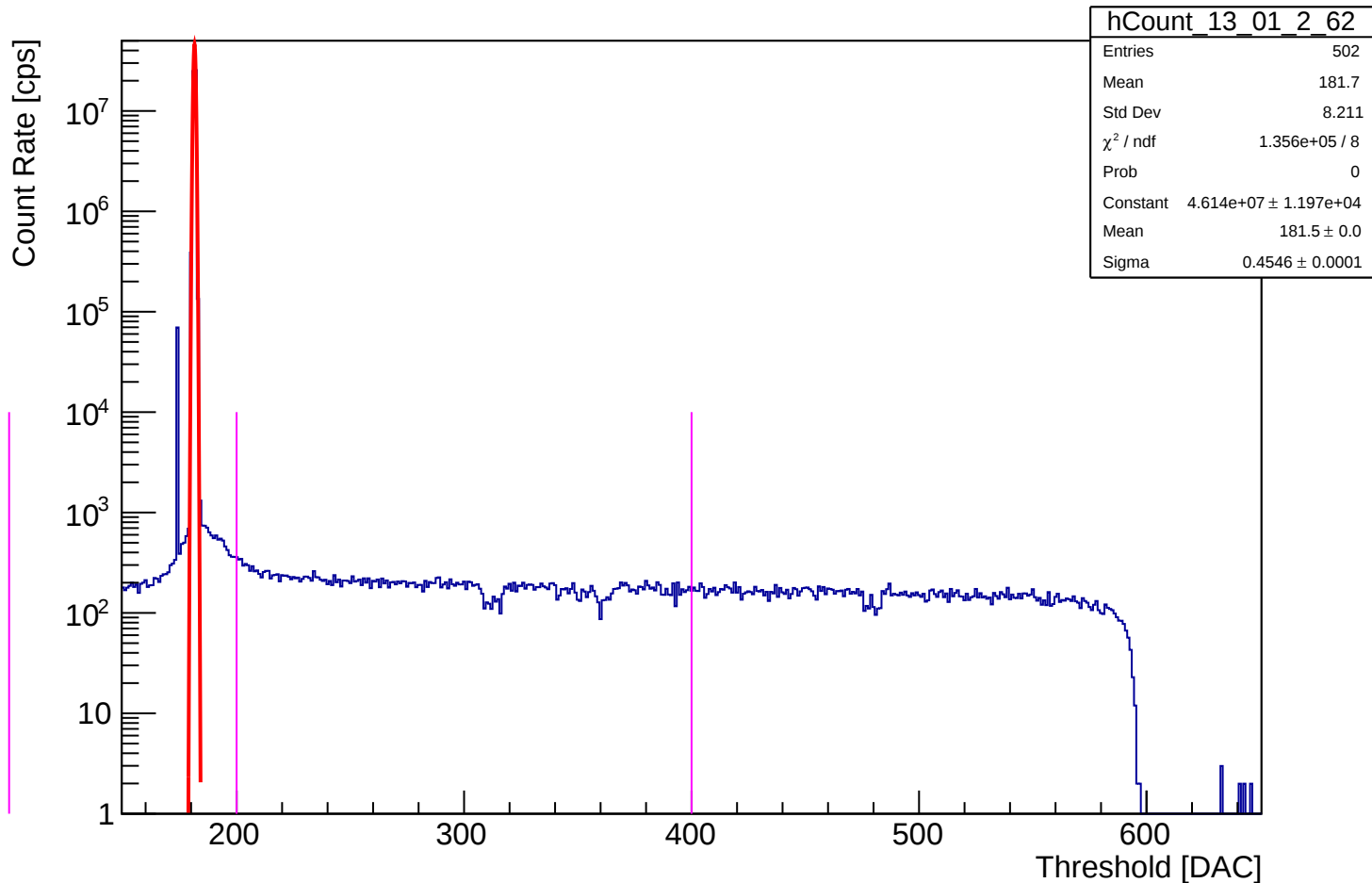




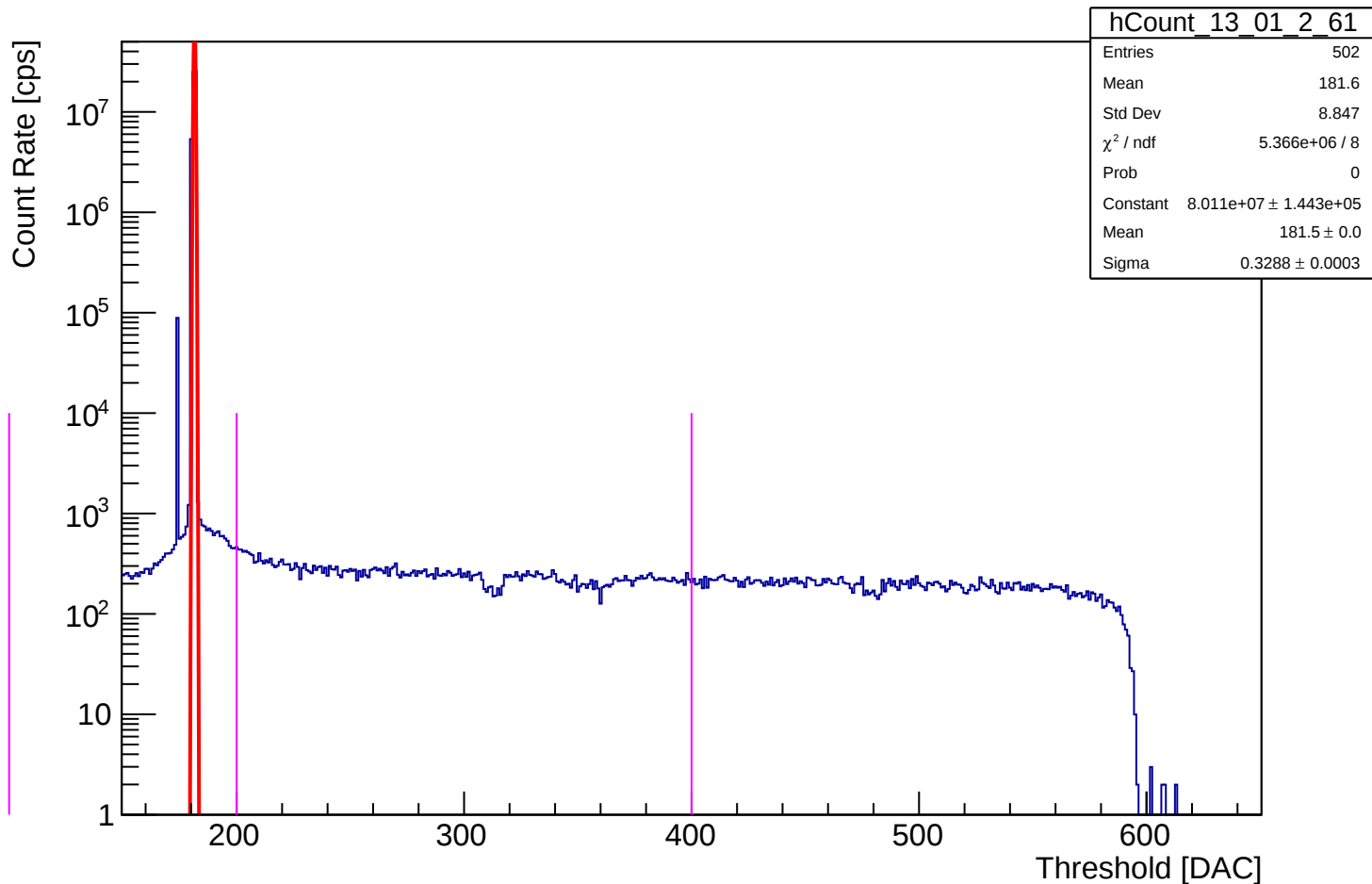
Row 1 Tile 1 Pmt 6 Pixel 61 Slot 13 Fiber 1 Asic 2 Channel 60



Row 1 Tile 1 Pmt 6 Pixel 62 Slot 13 Fiber 1 Asic 2 Channel 62



Row 1 Tile 1 Pmt 6 Pixel 63 Slot 13 Fiber 1 Asic 2 Channel 61



Row 1 Tile 1 Pmt 6 Pixel 64 Slot 13 Fiber 1 Asic 2 Channel 63

