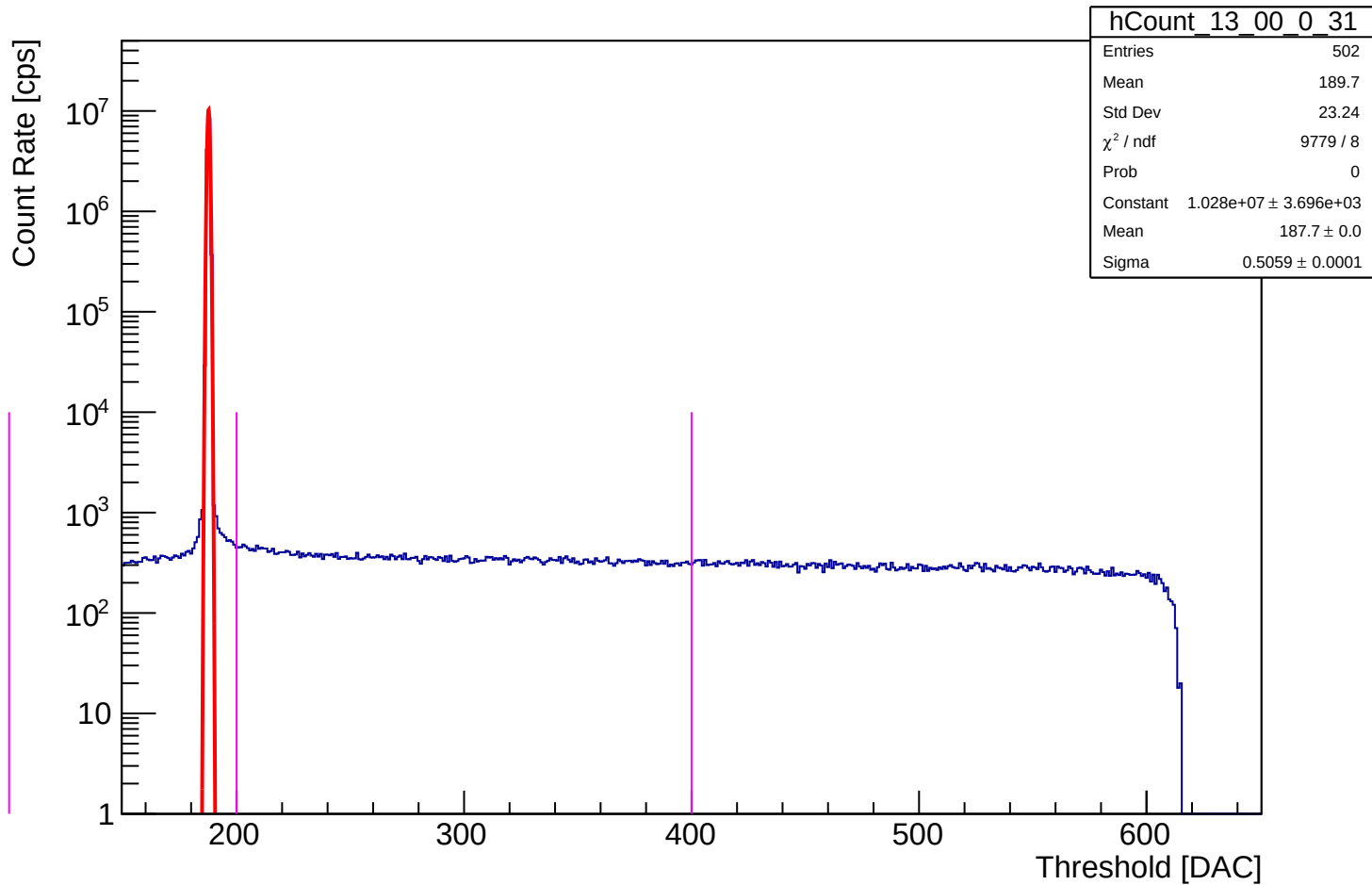
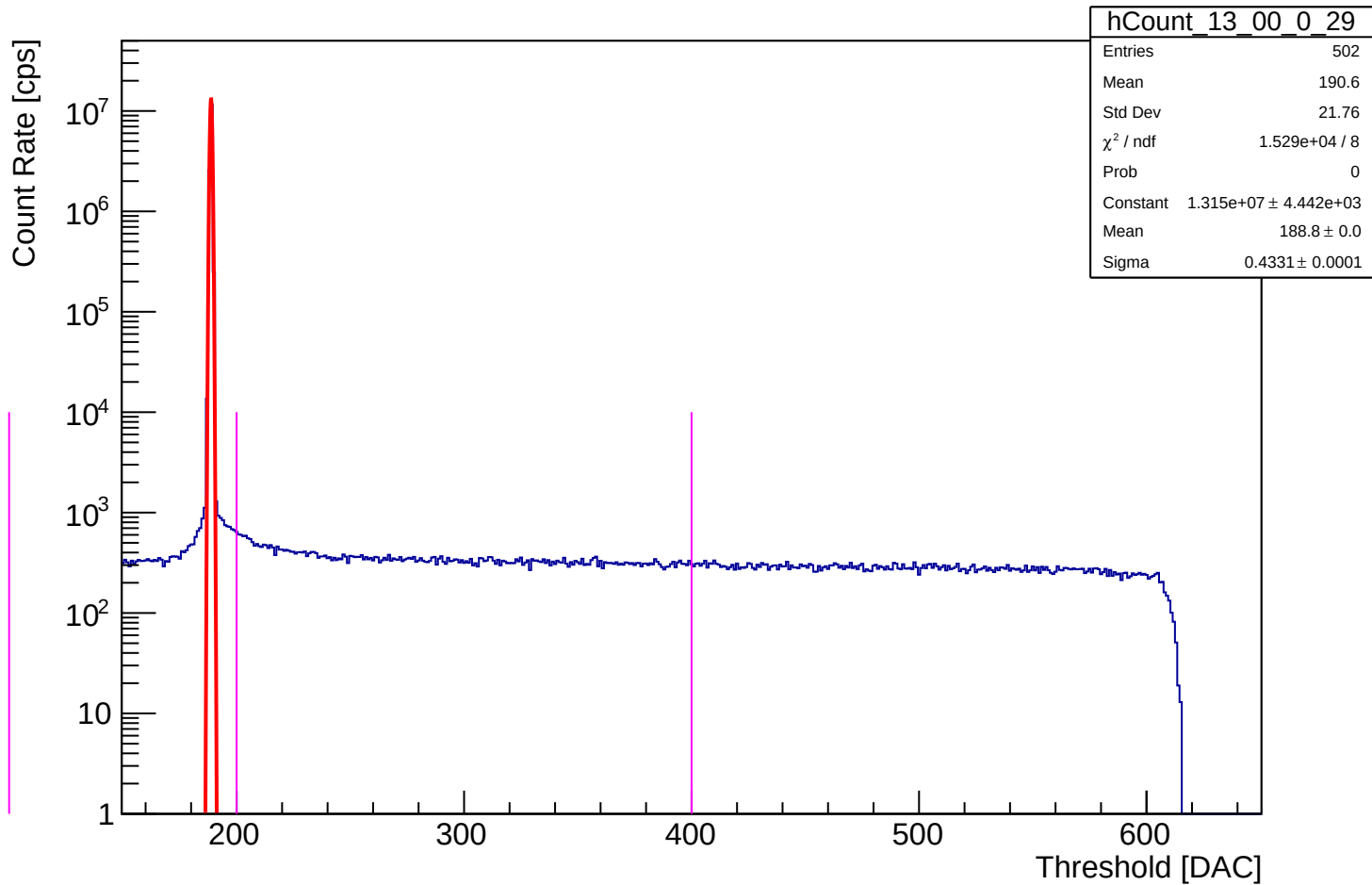


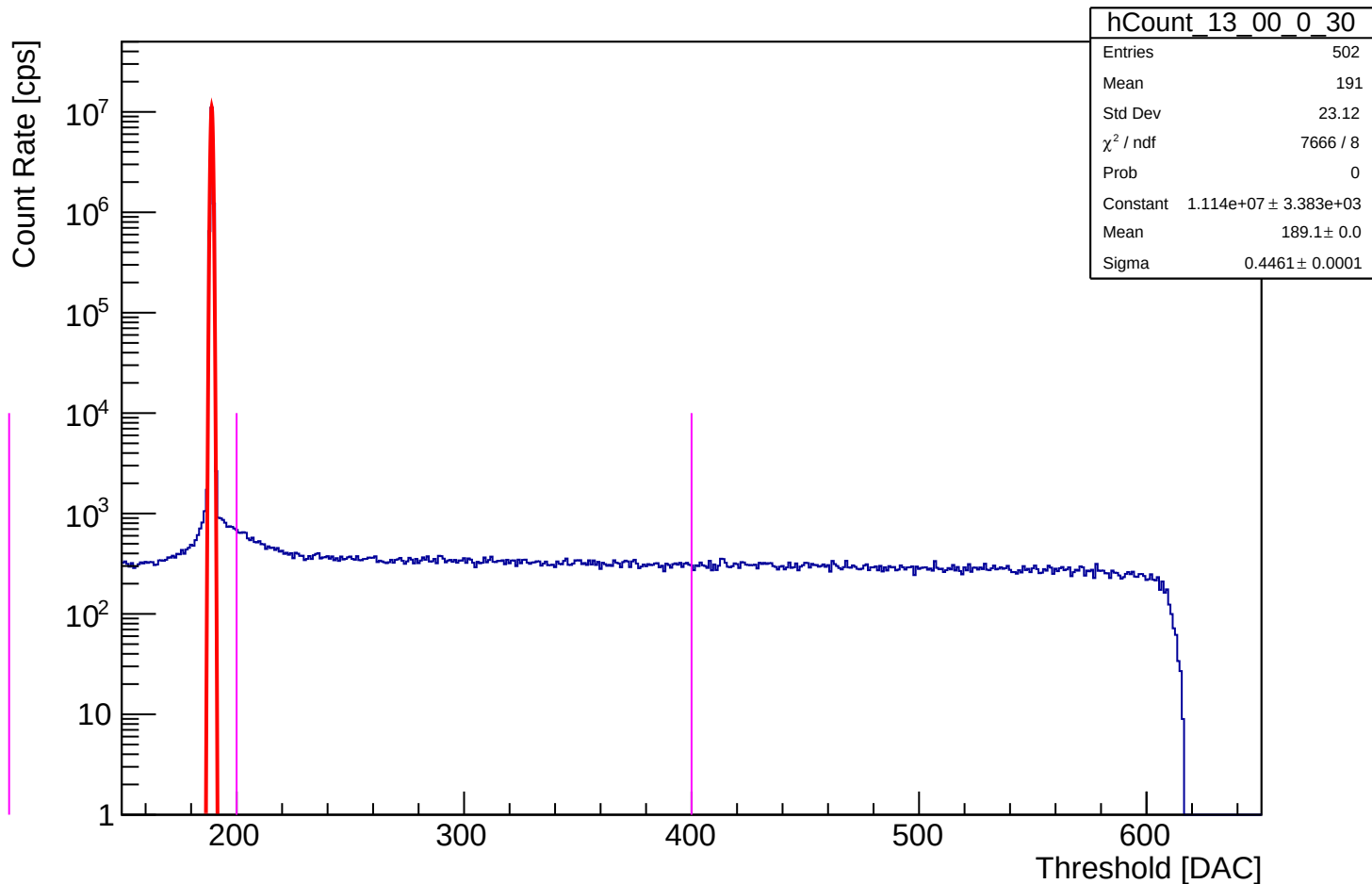
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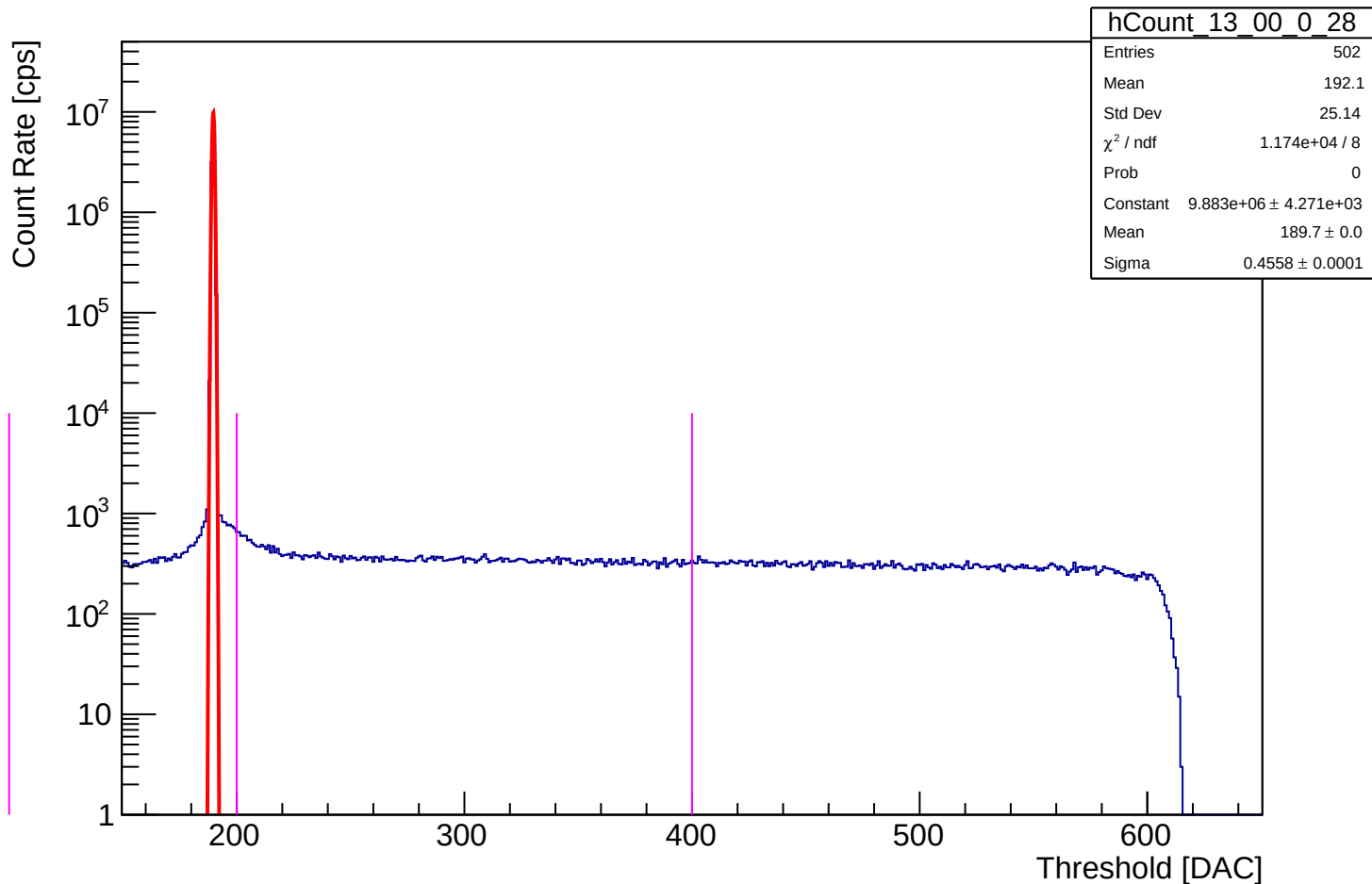
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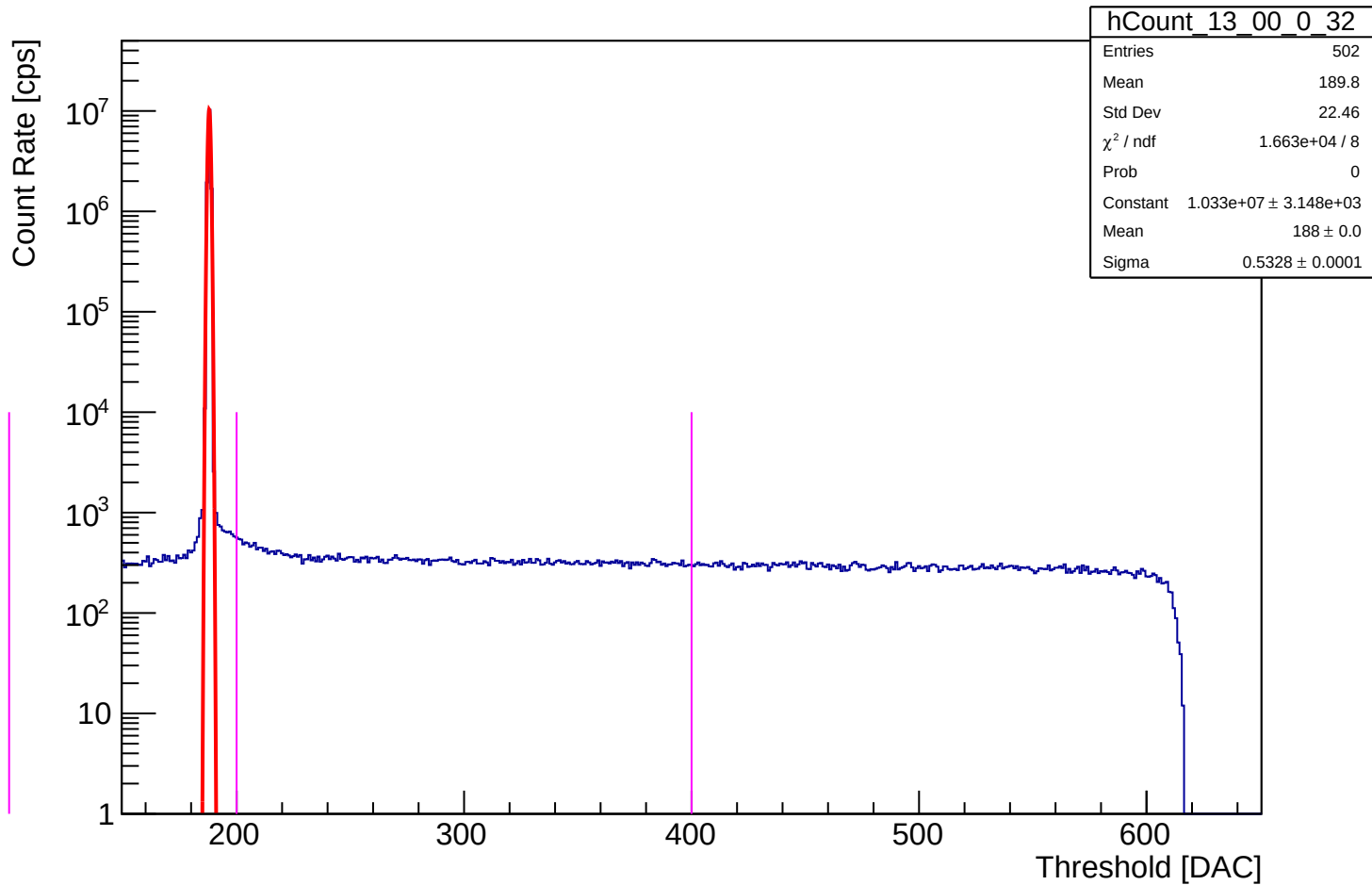
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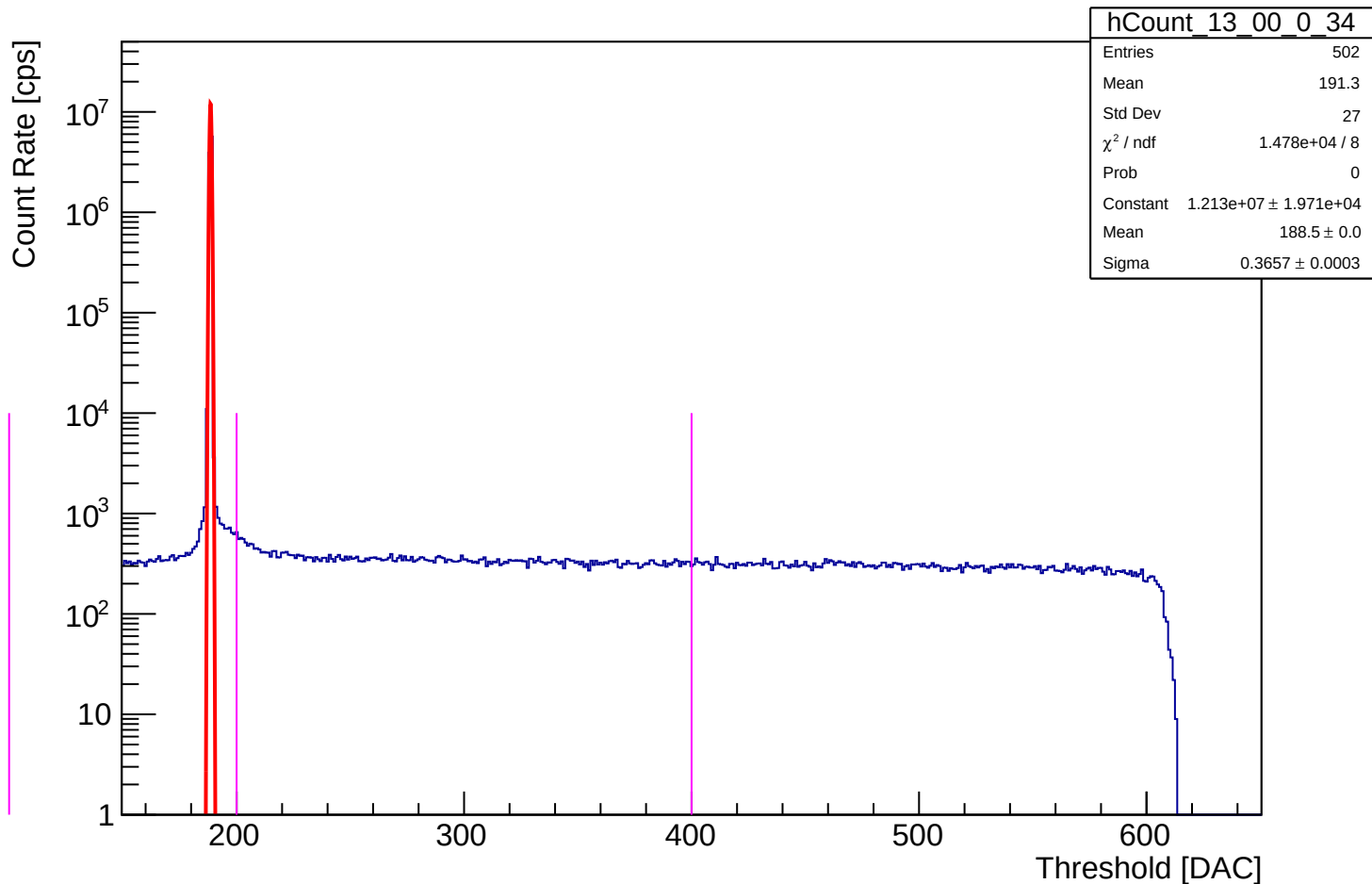
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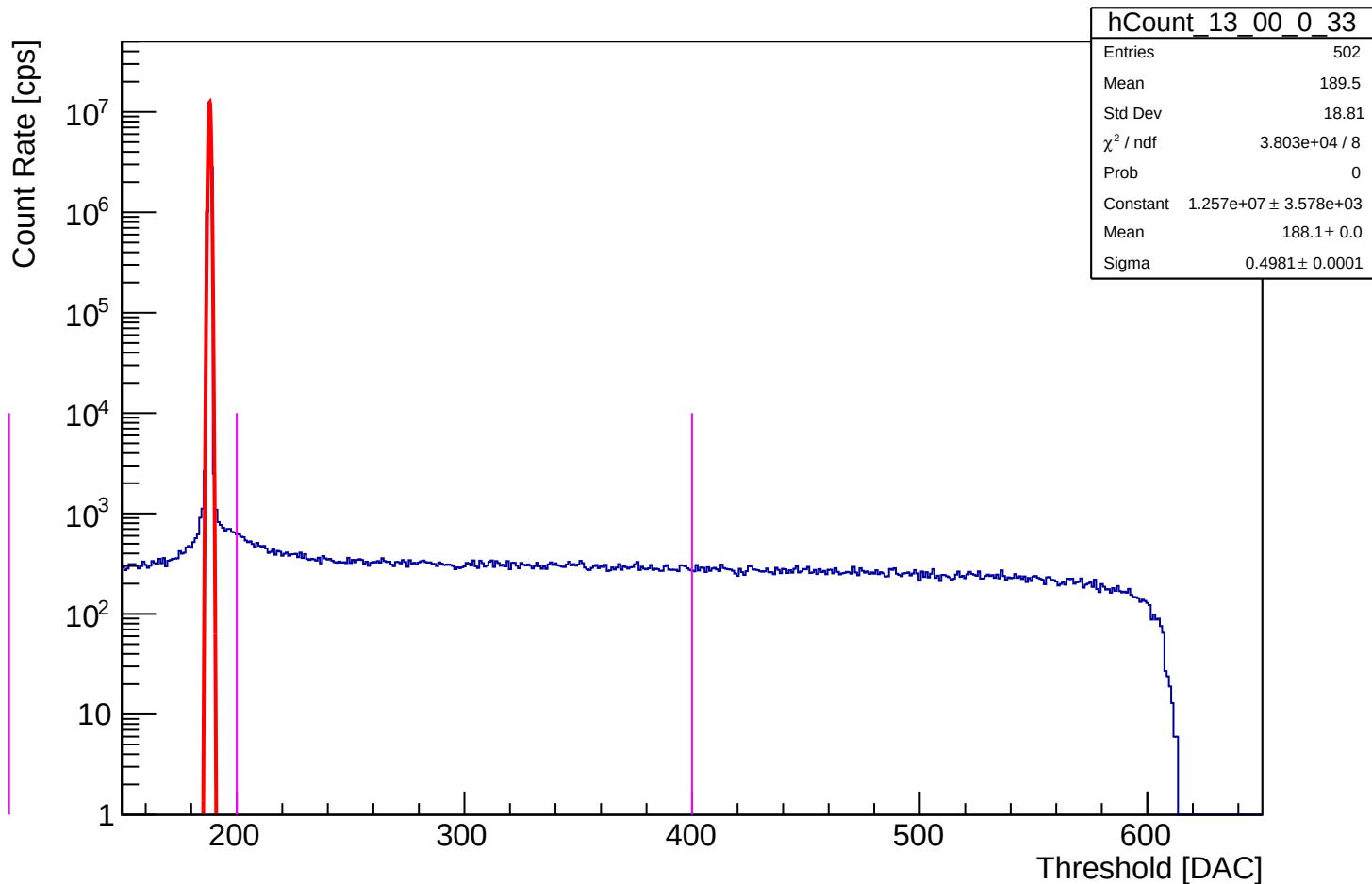
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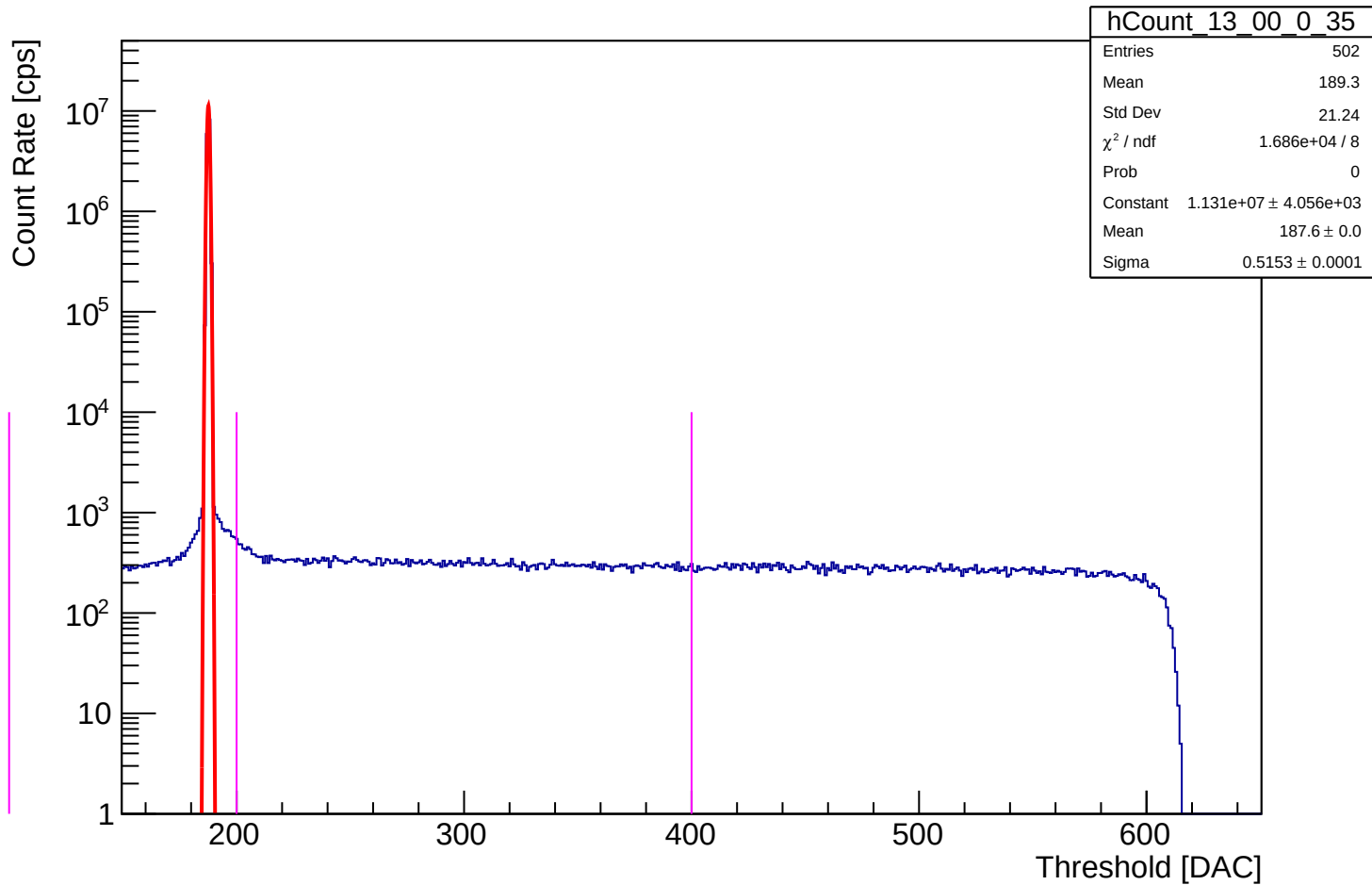
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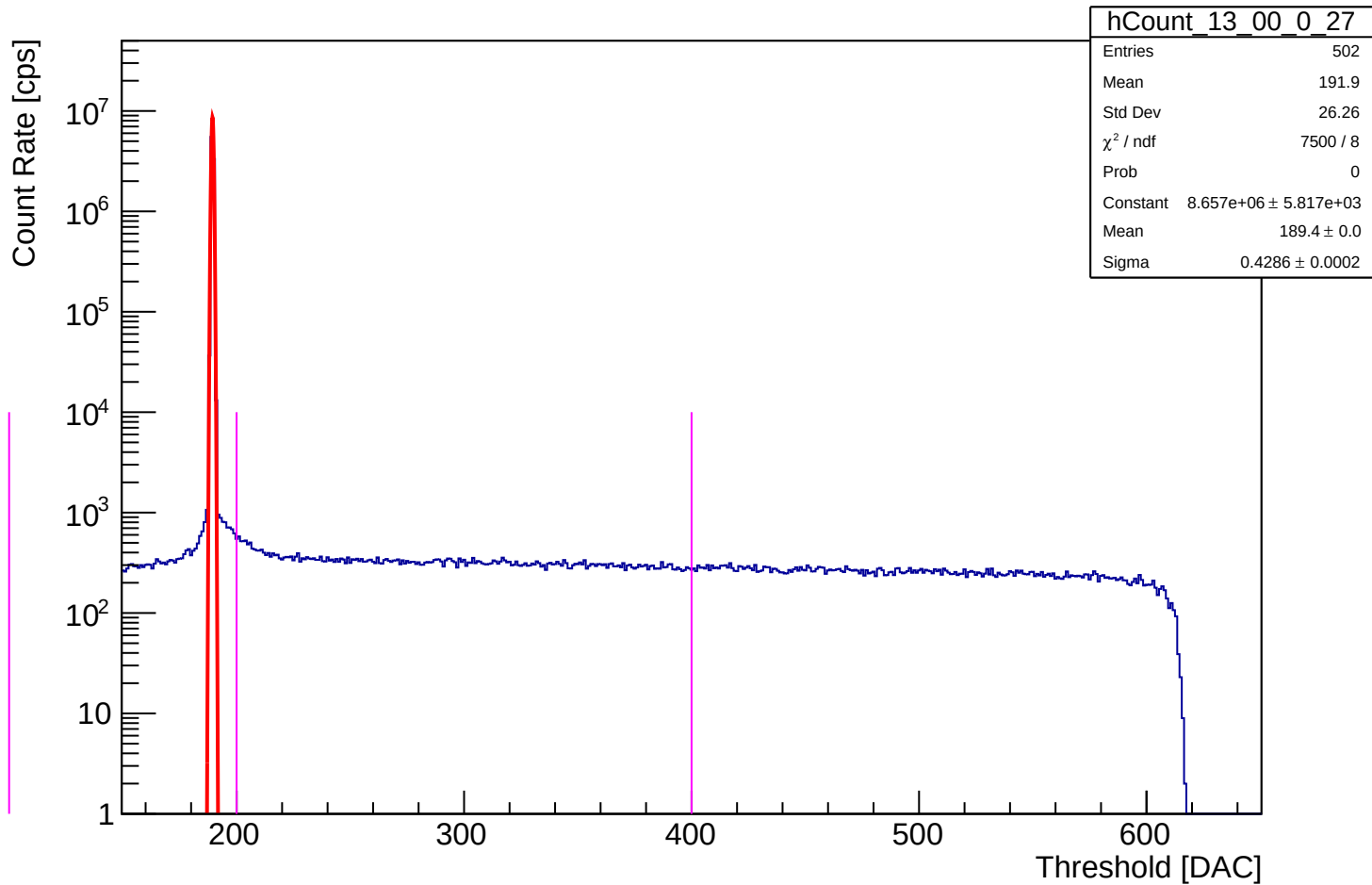
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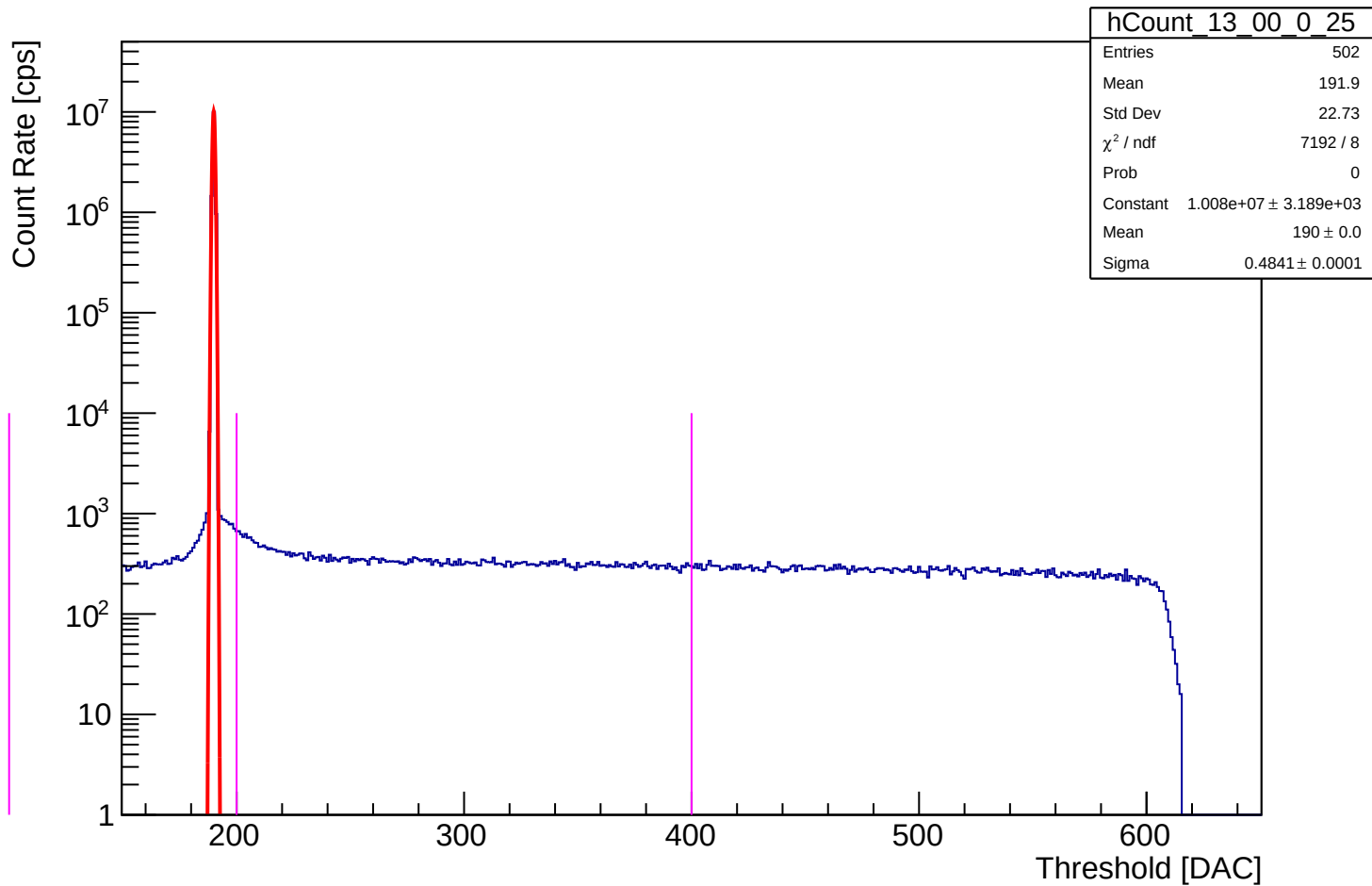
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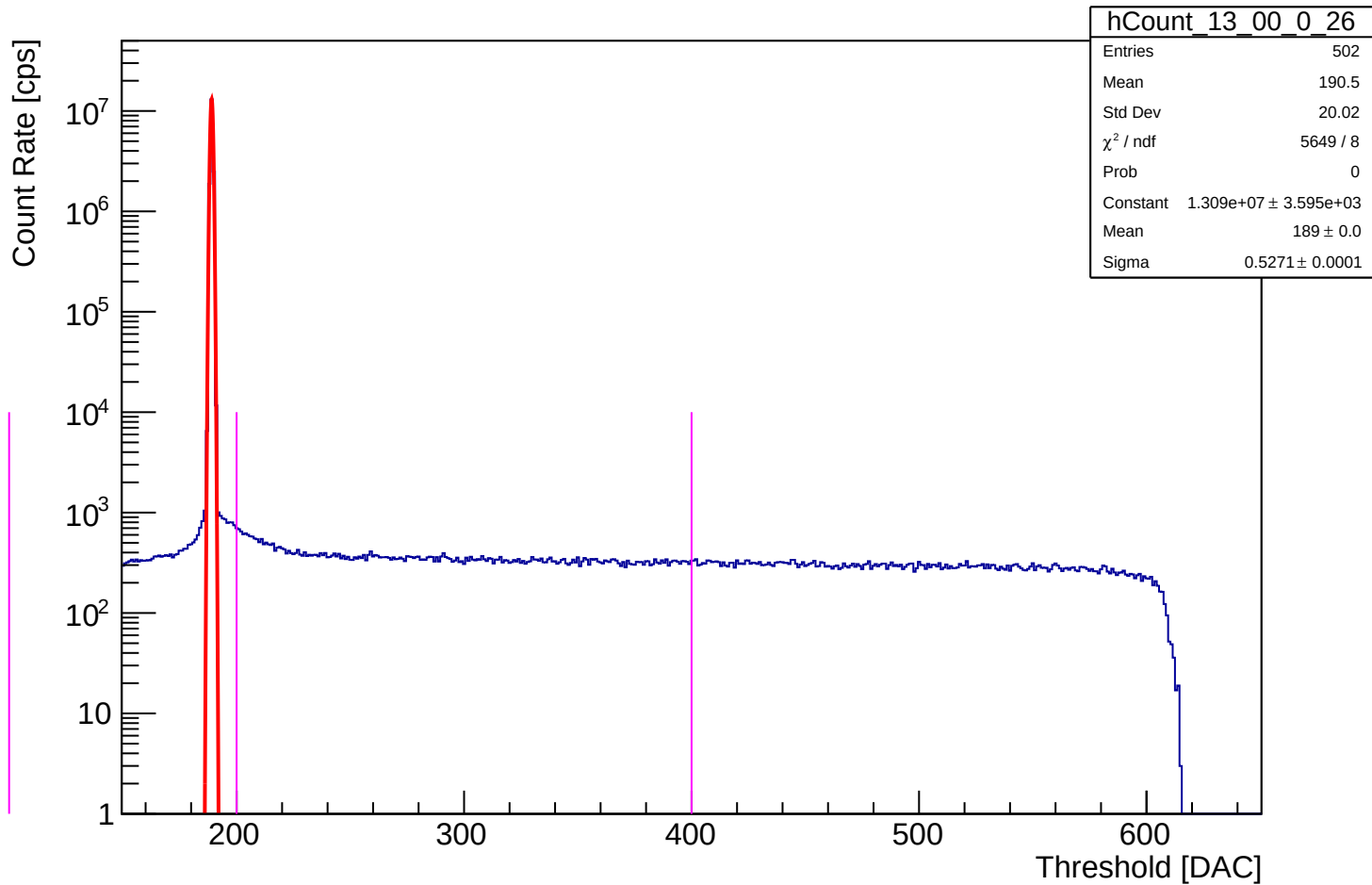
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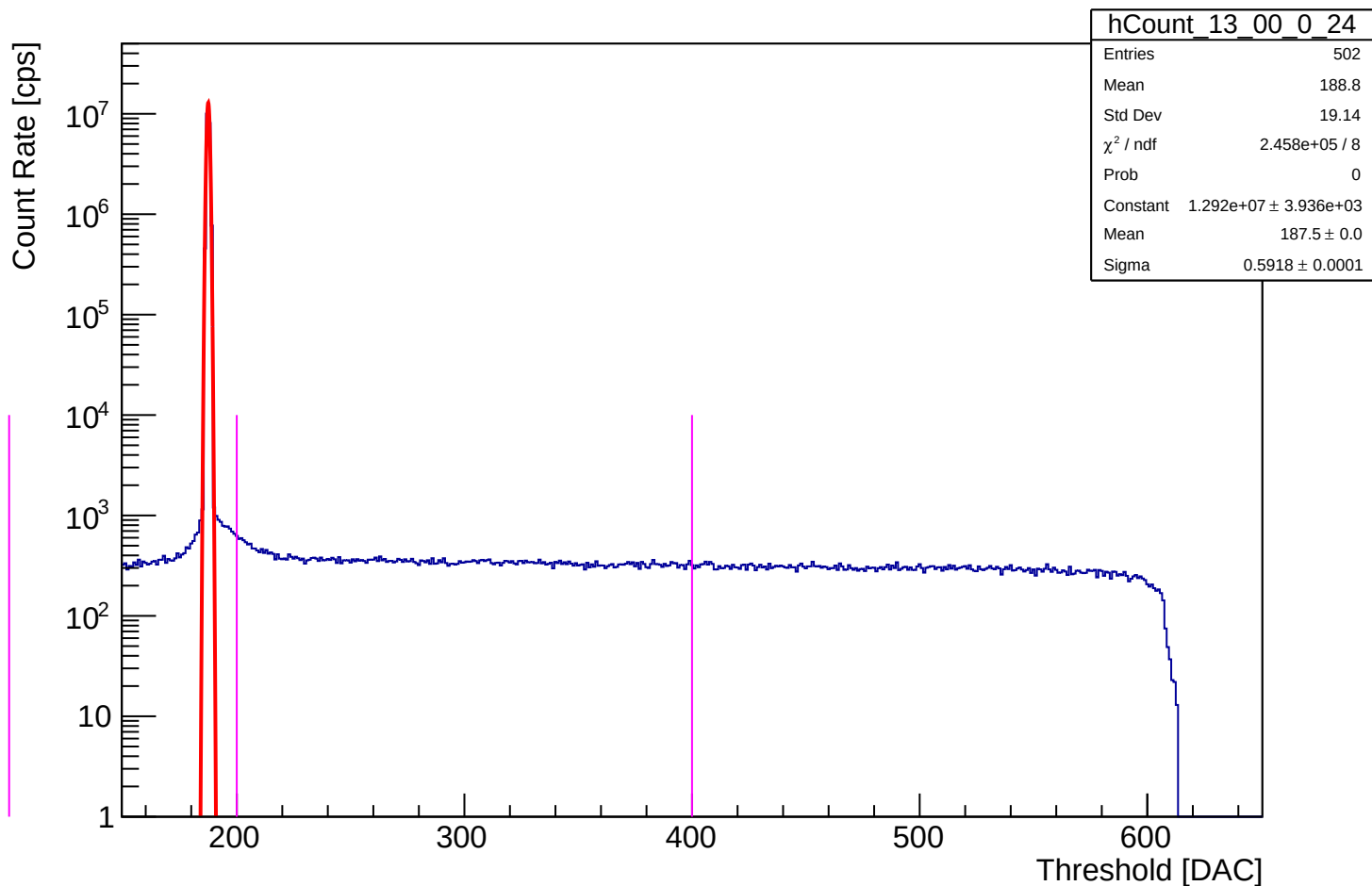
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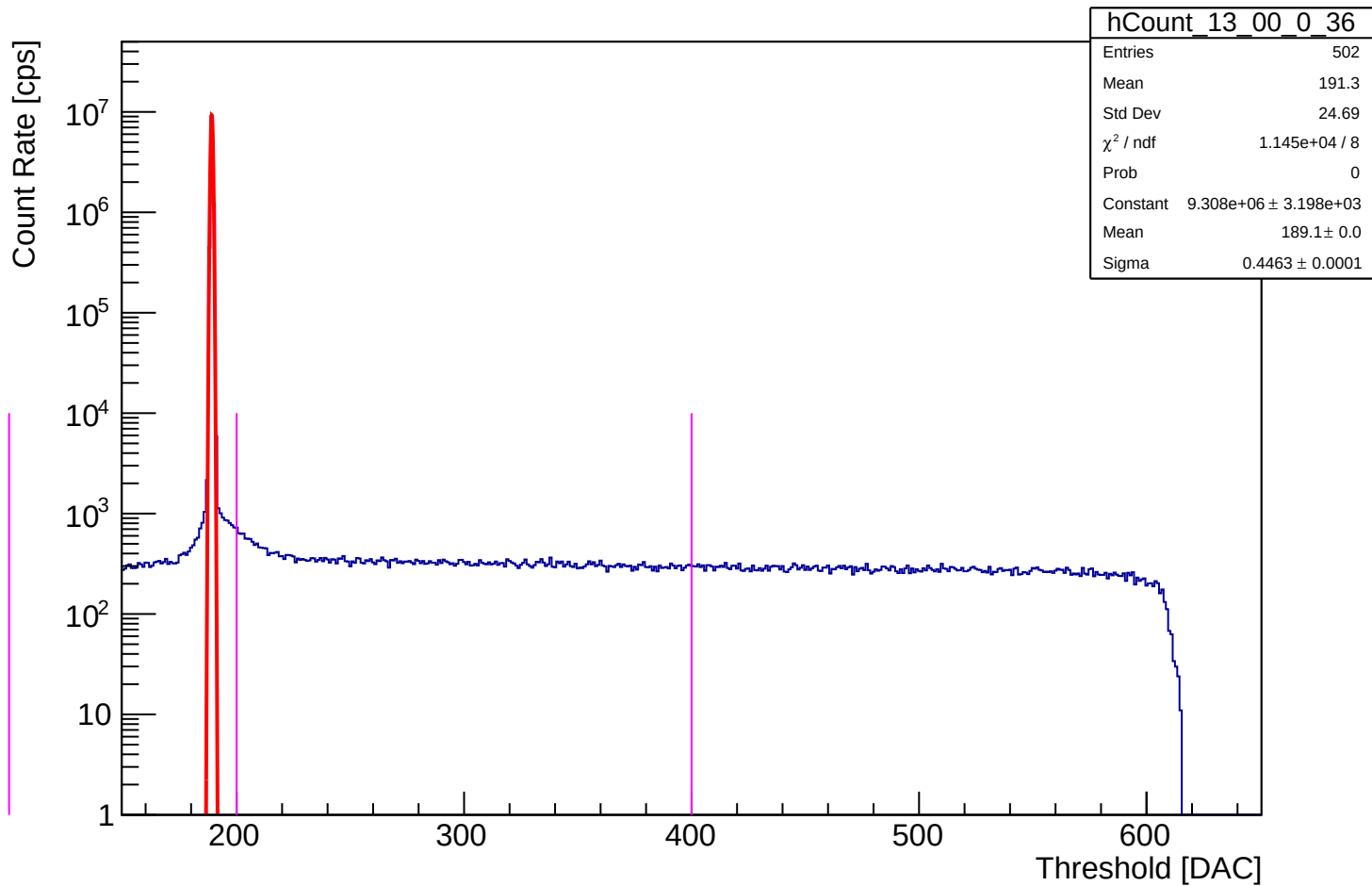
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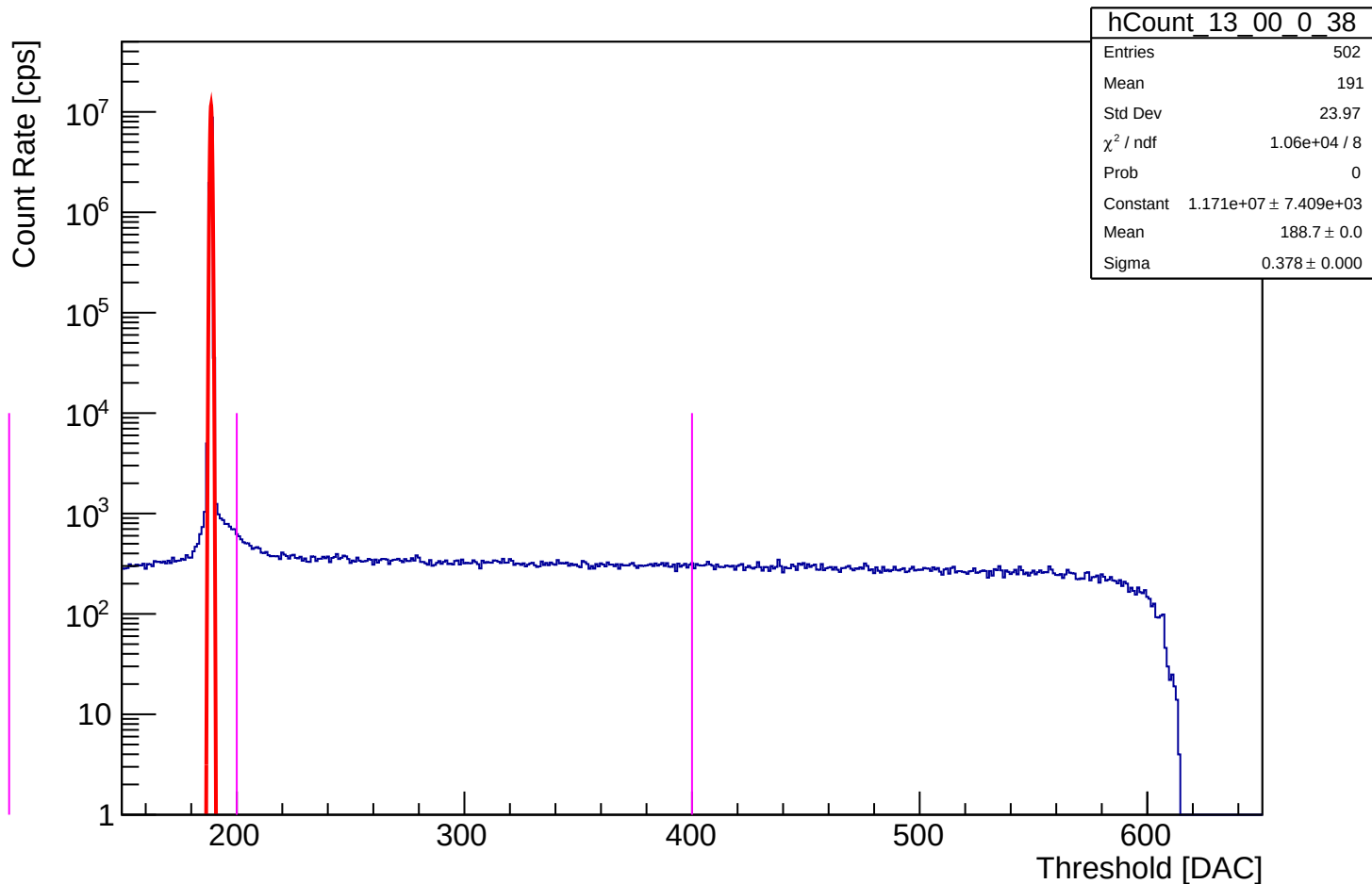
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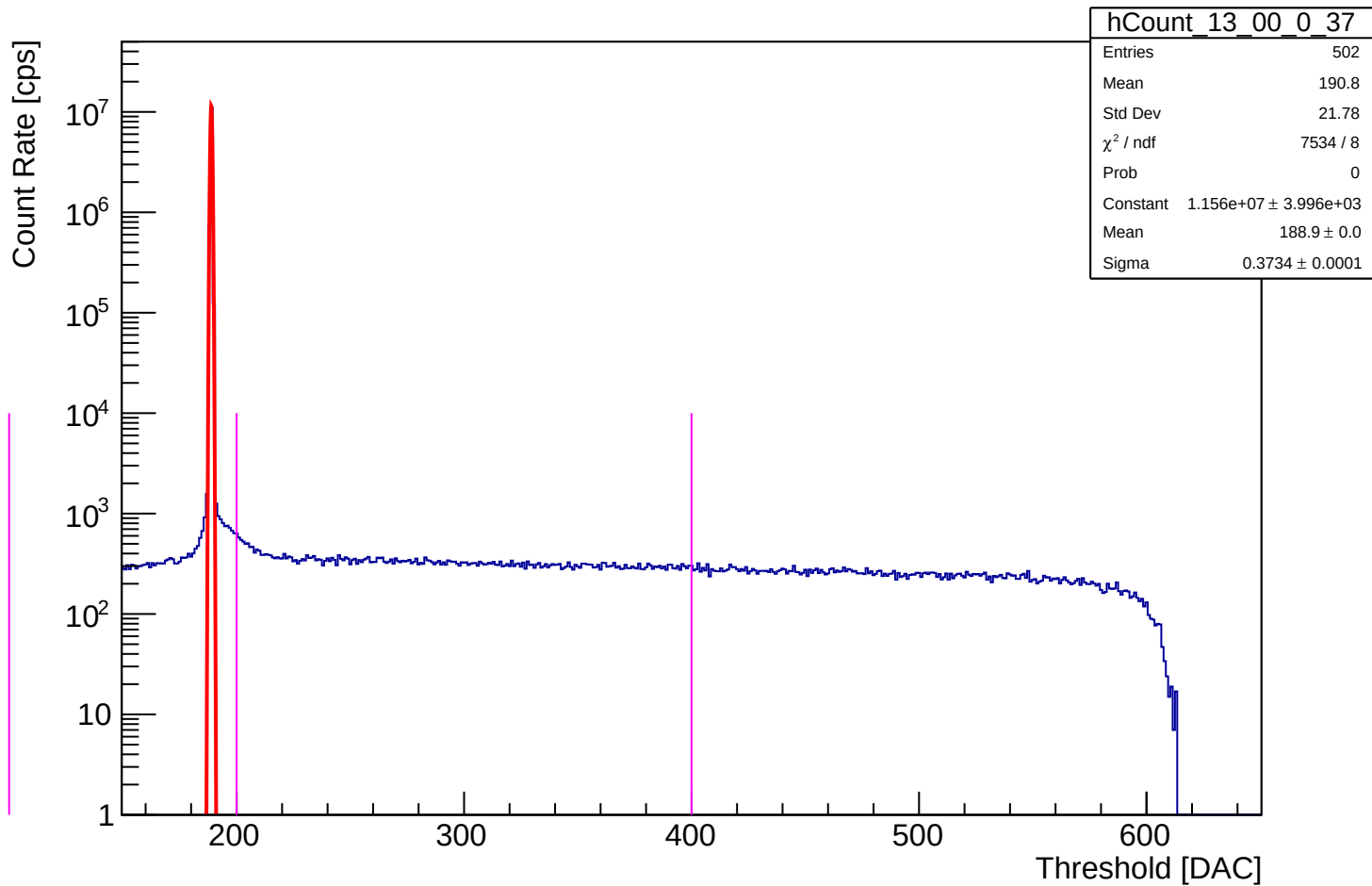
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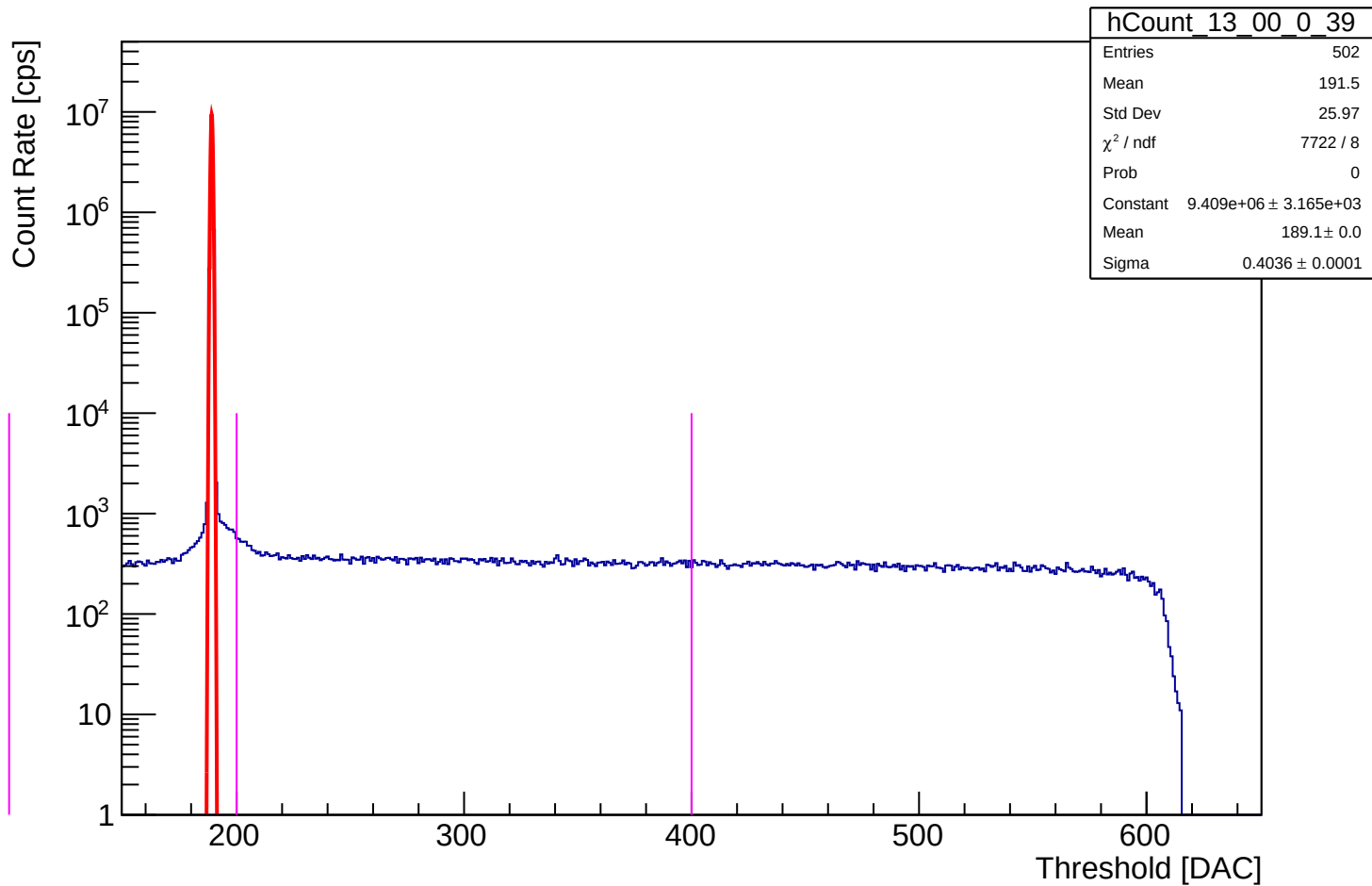
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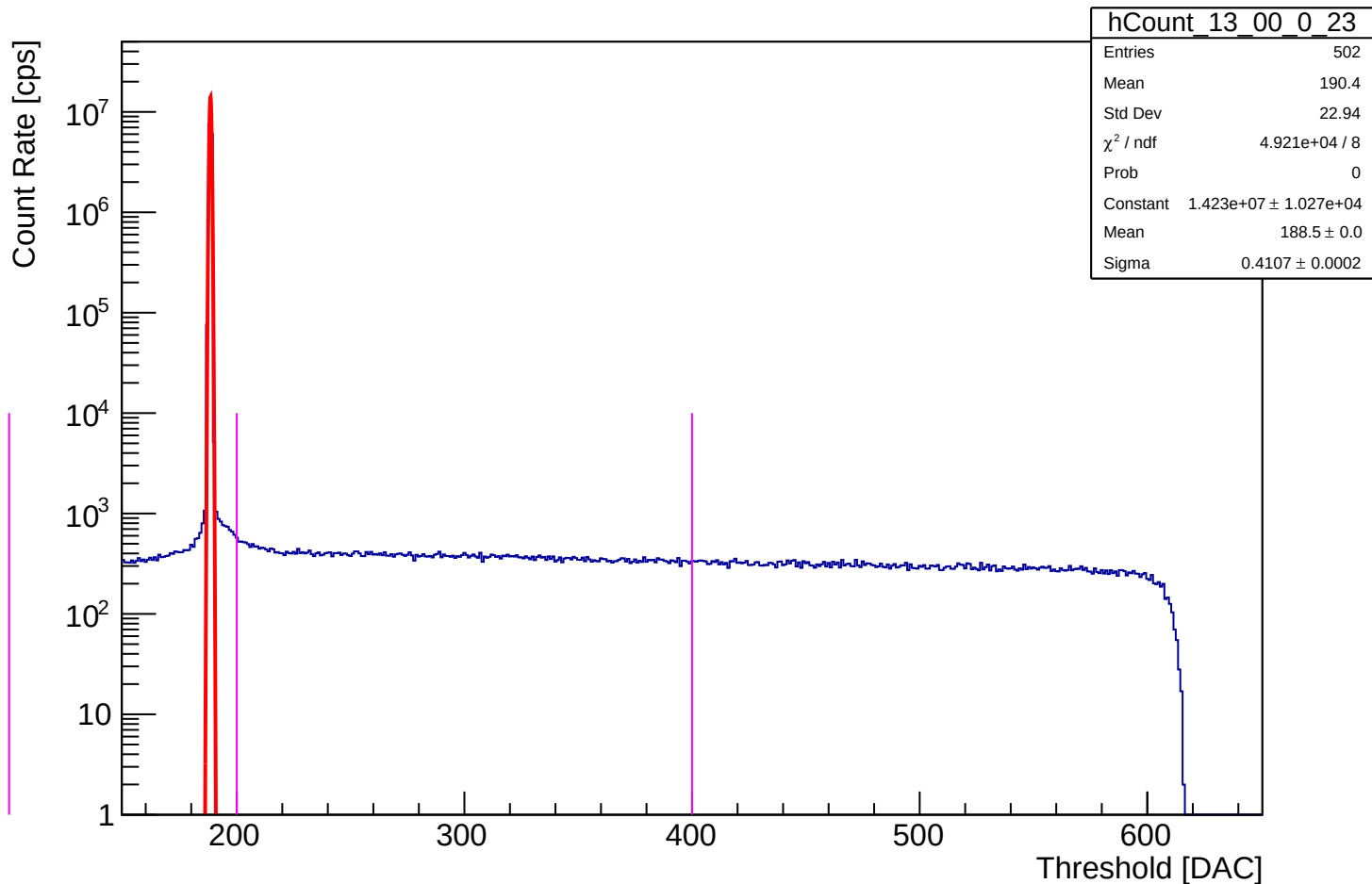
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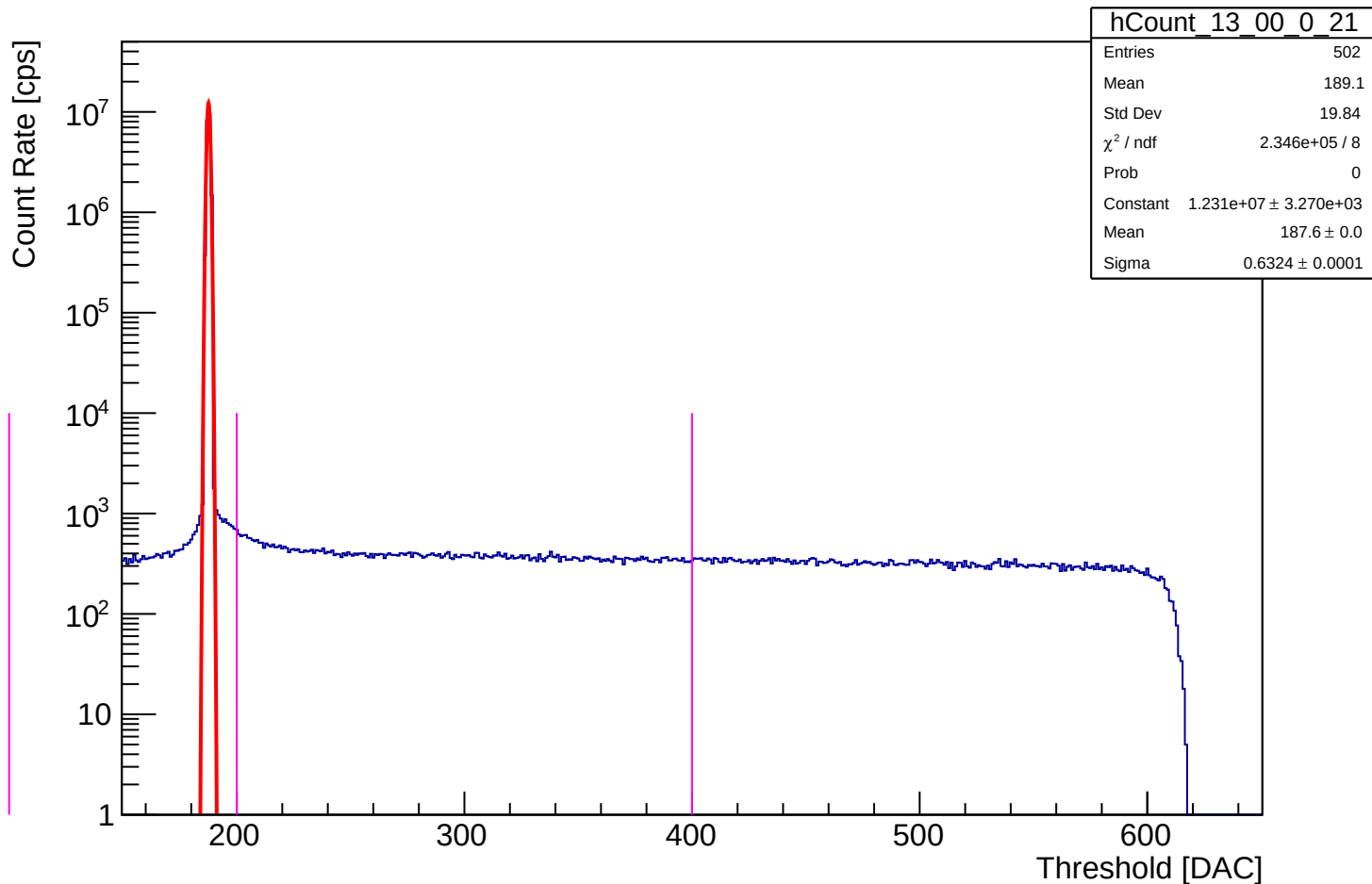
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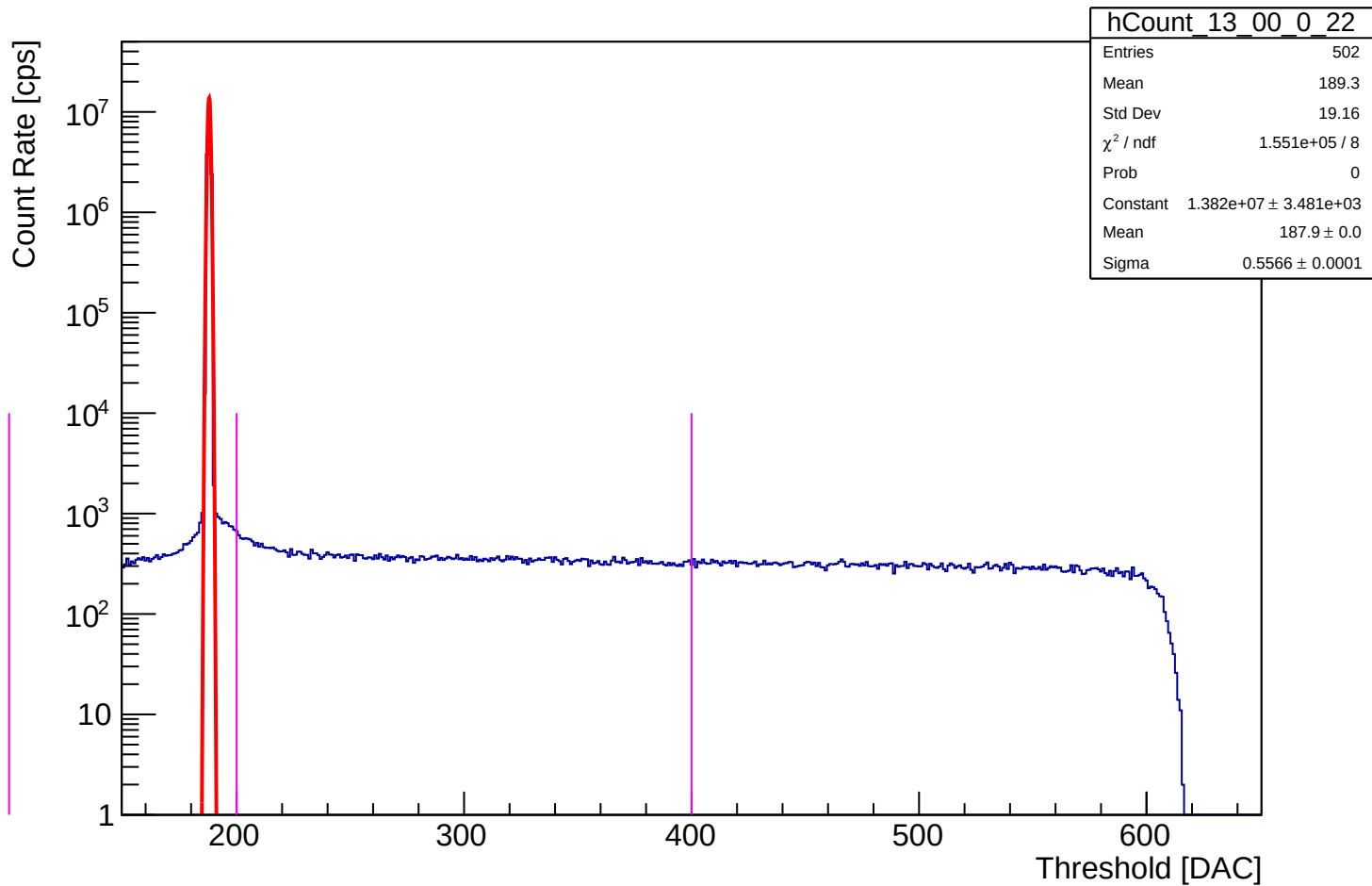
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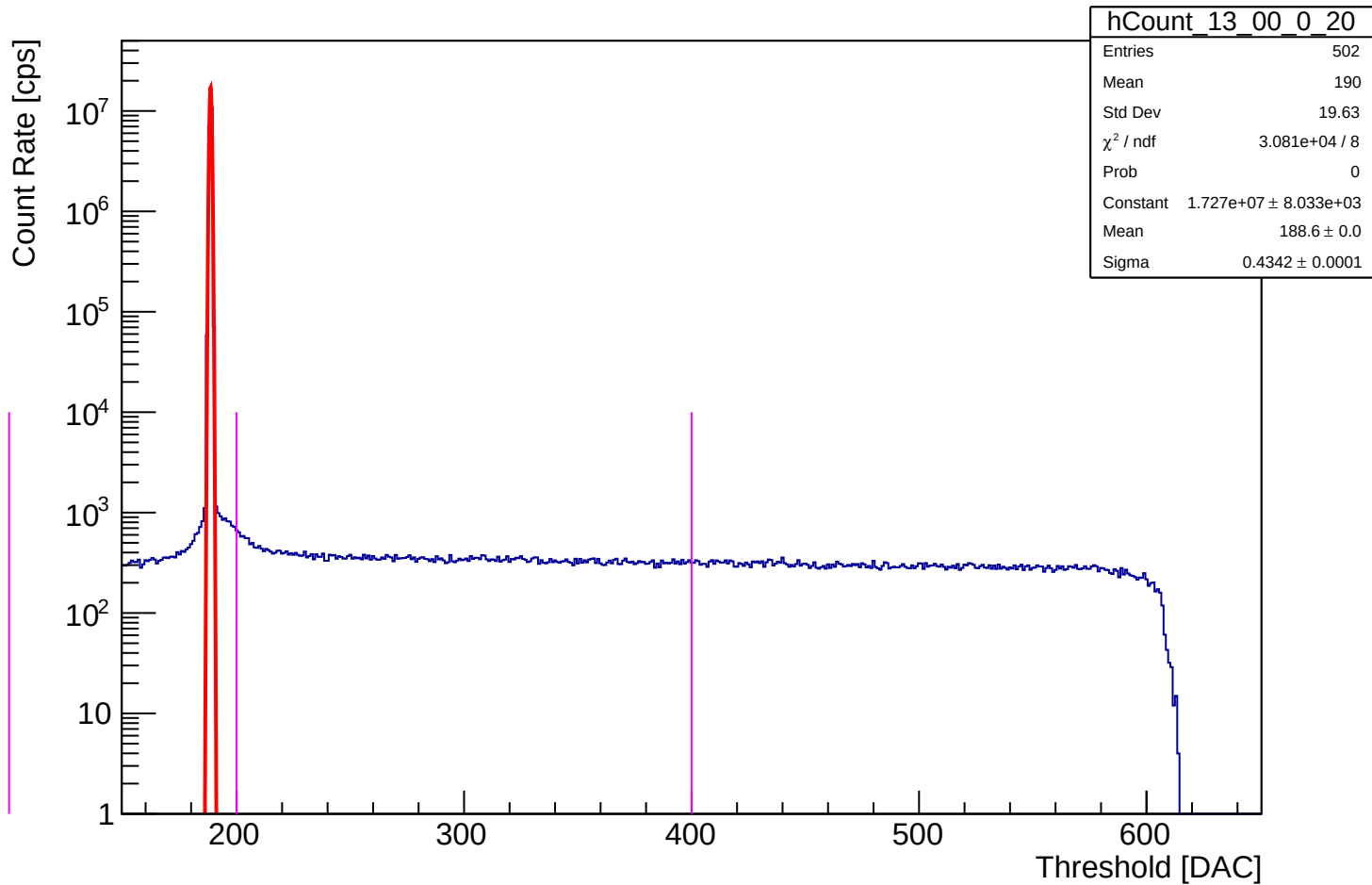
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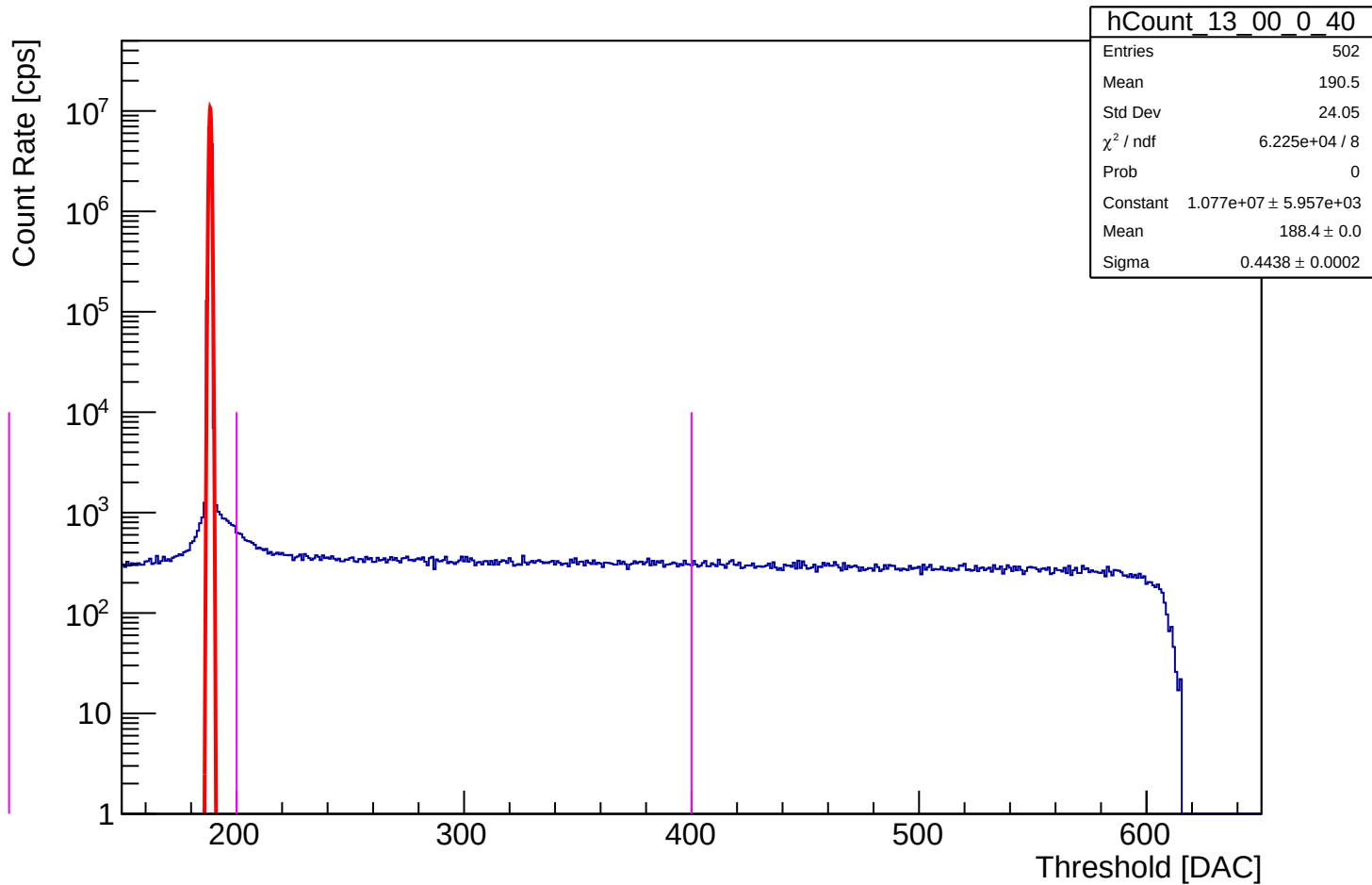
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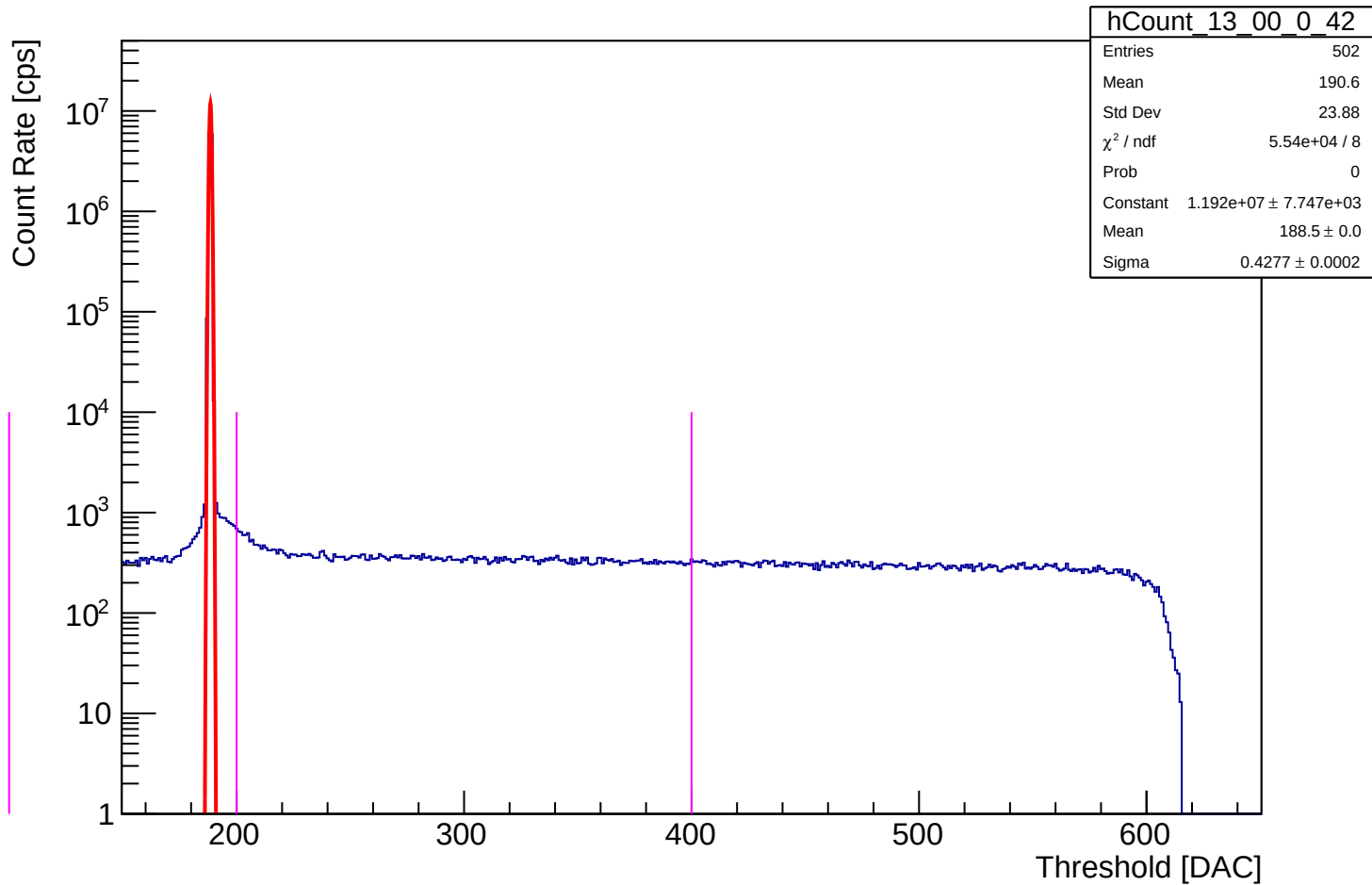
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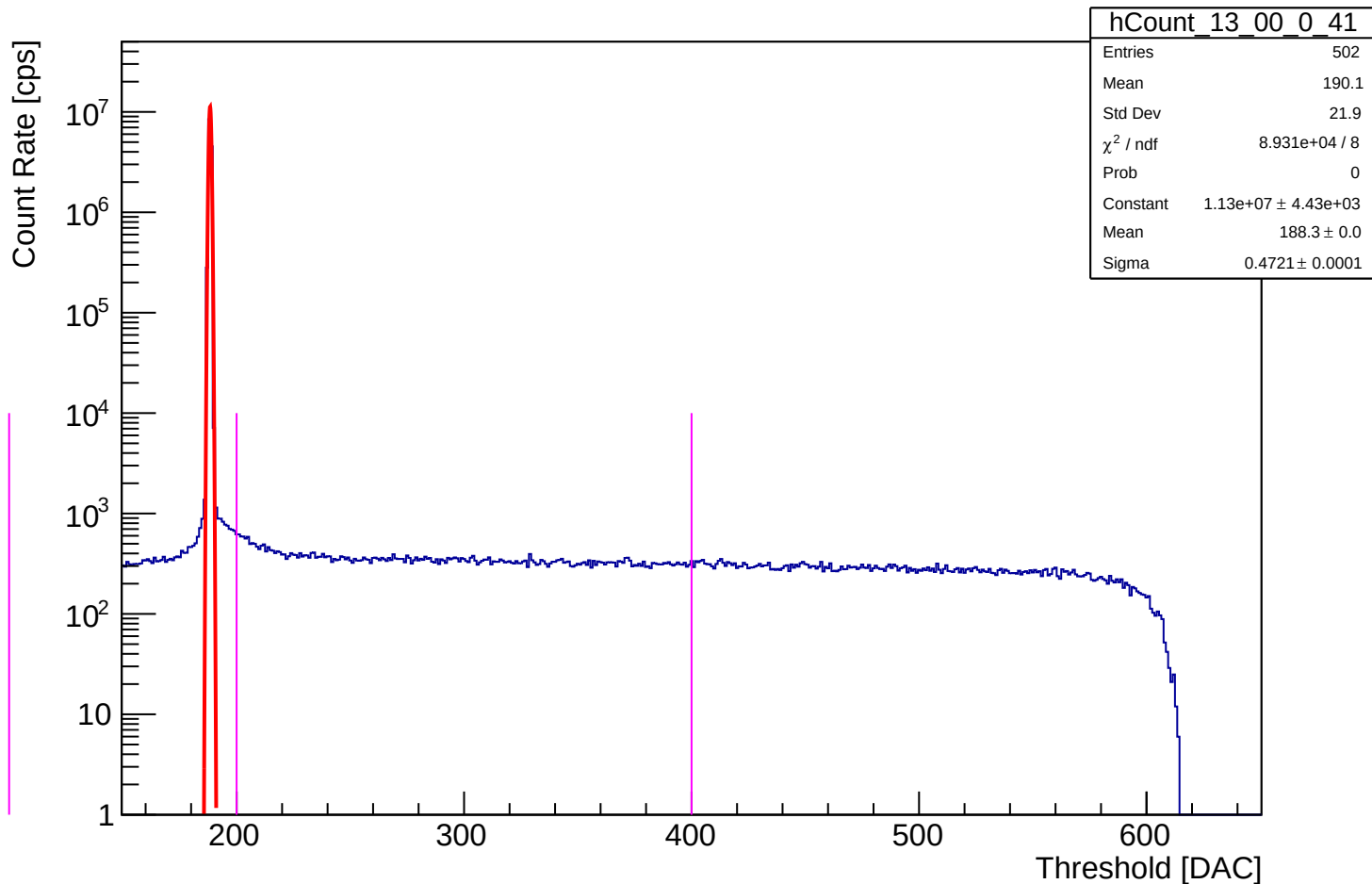
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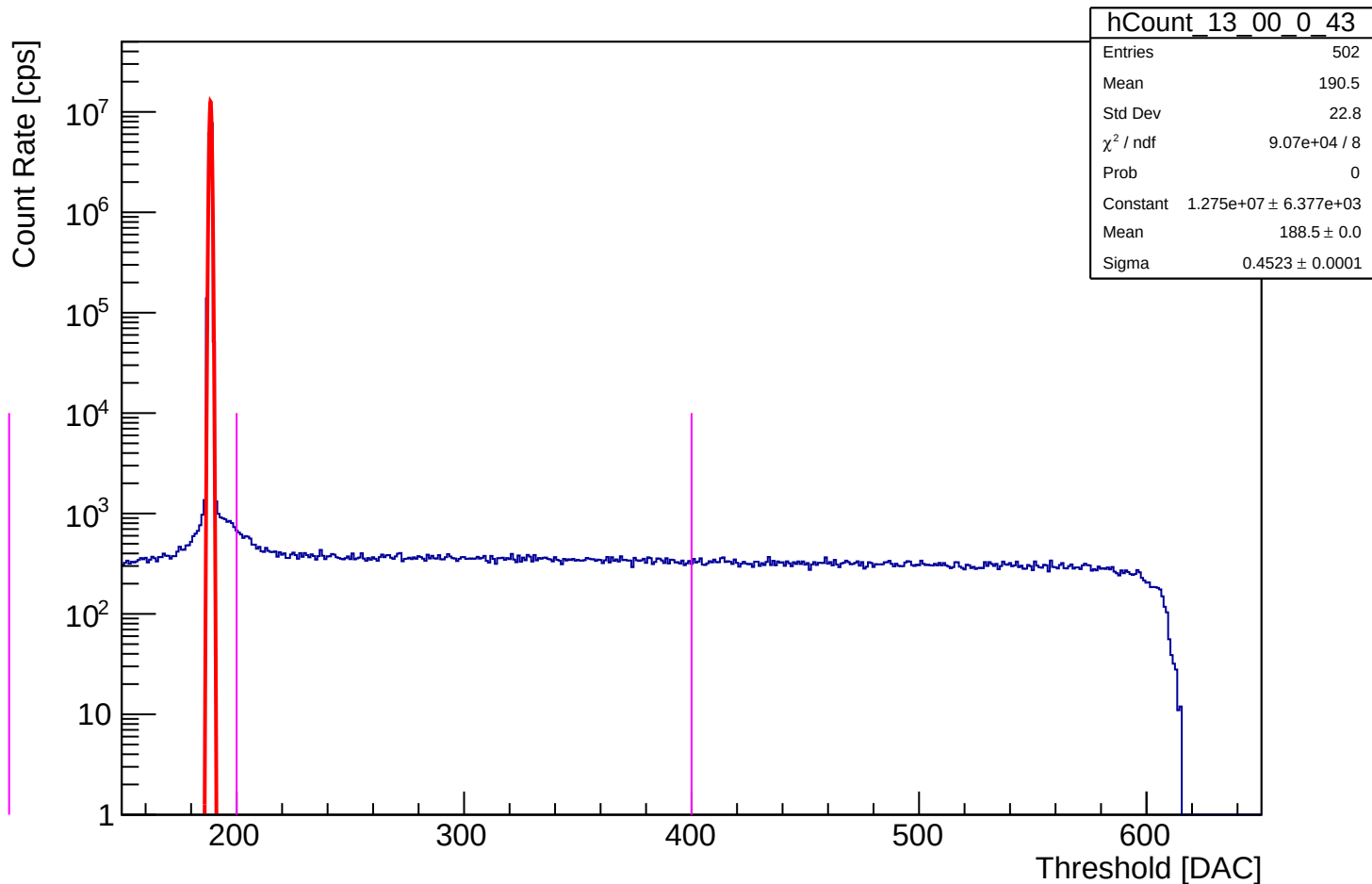
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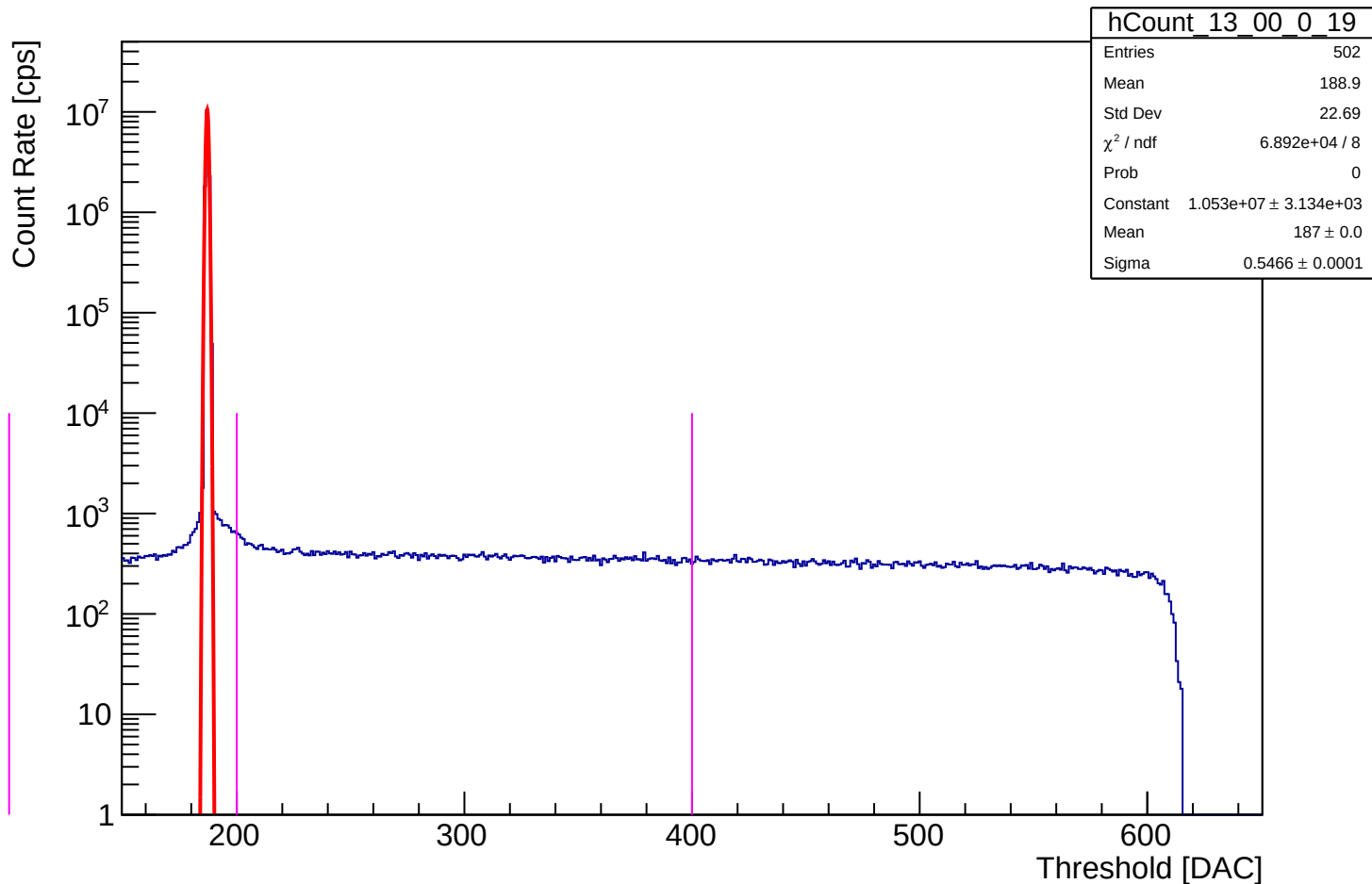
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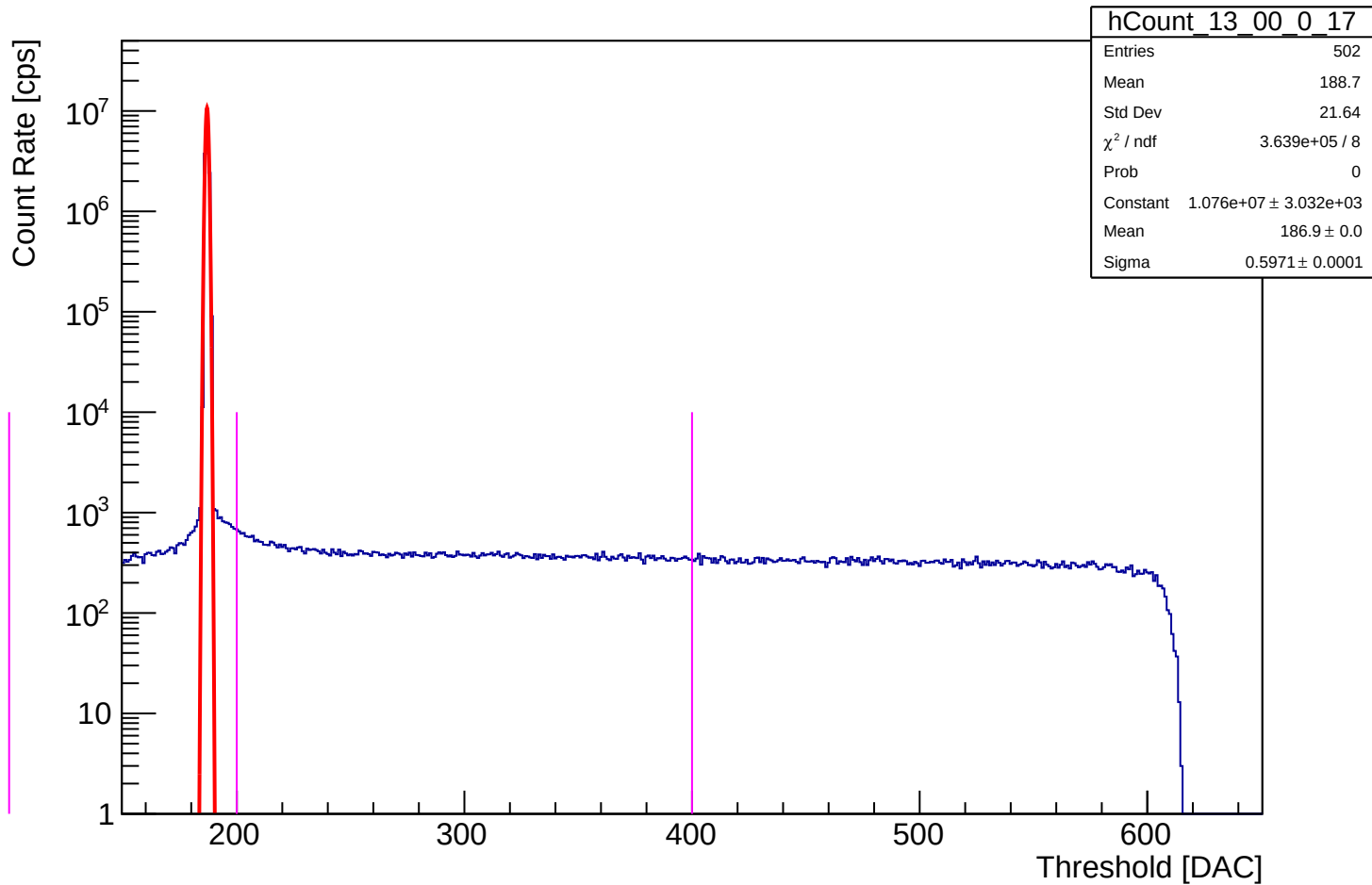
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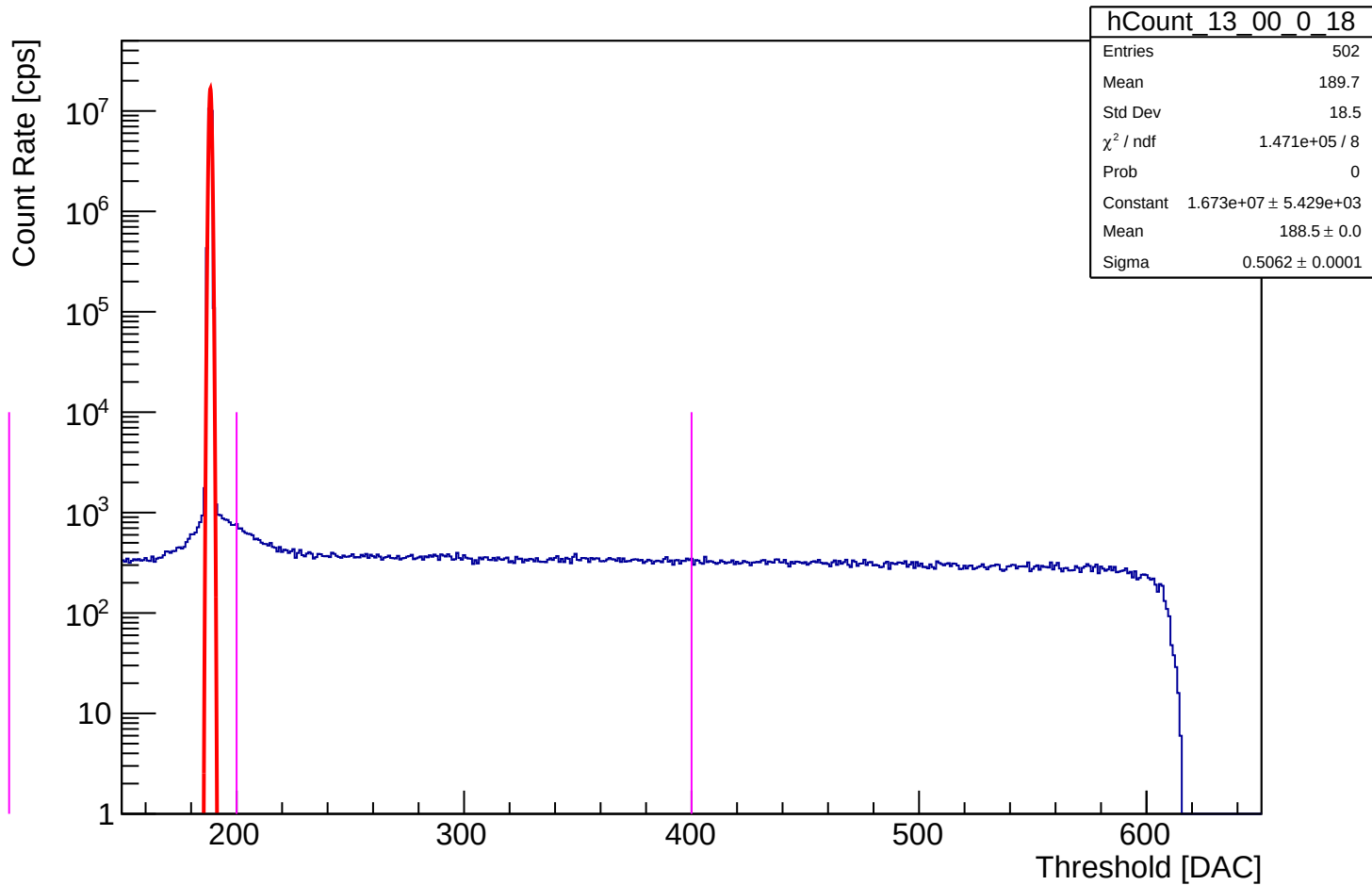
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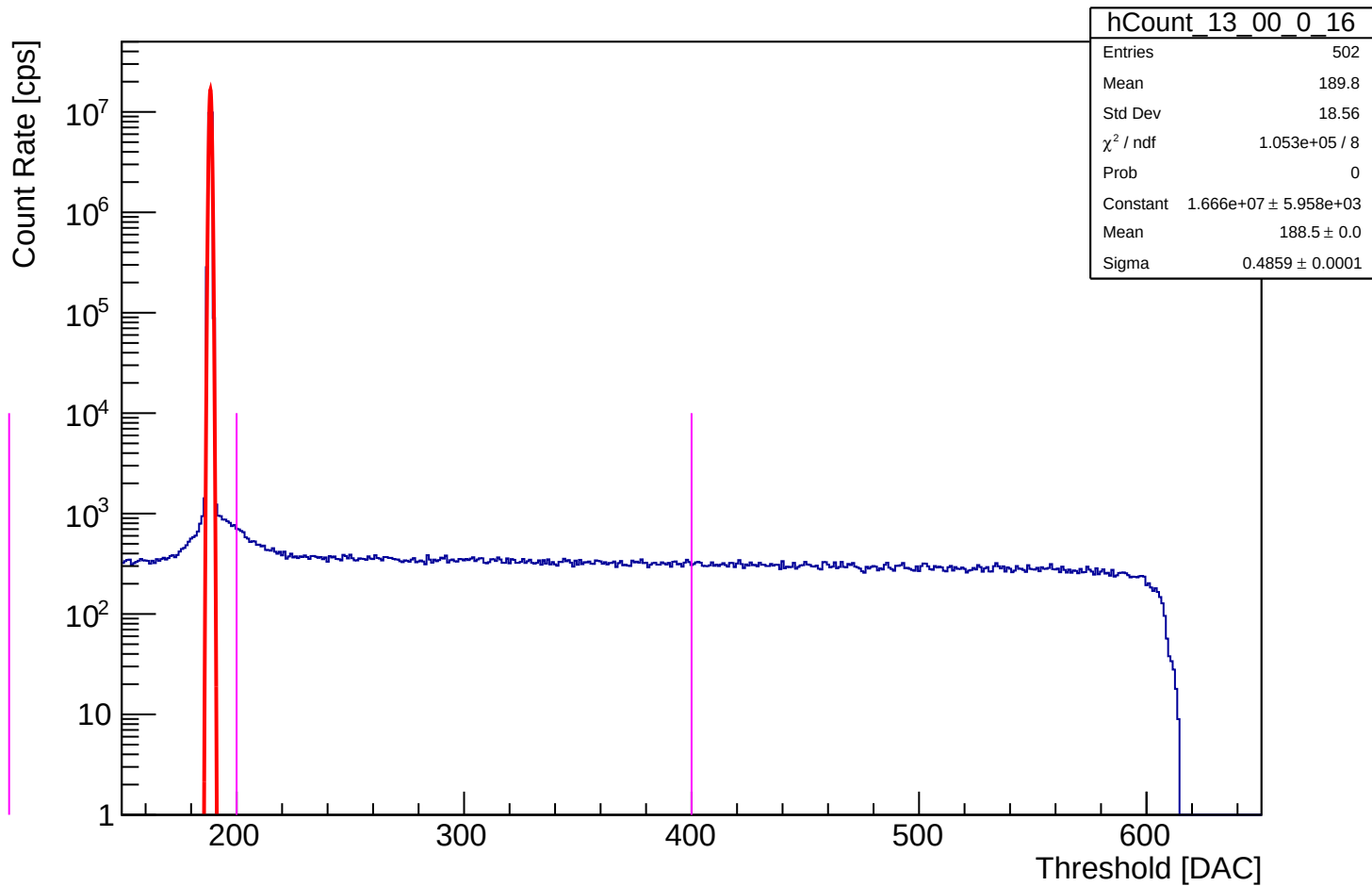
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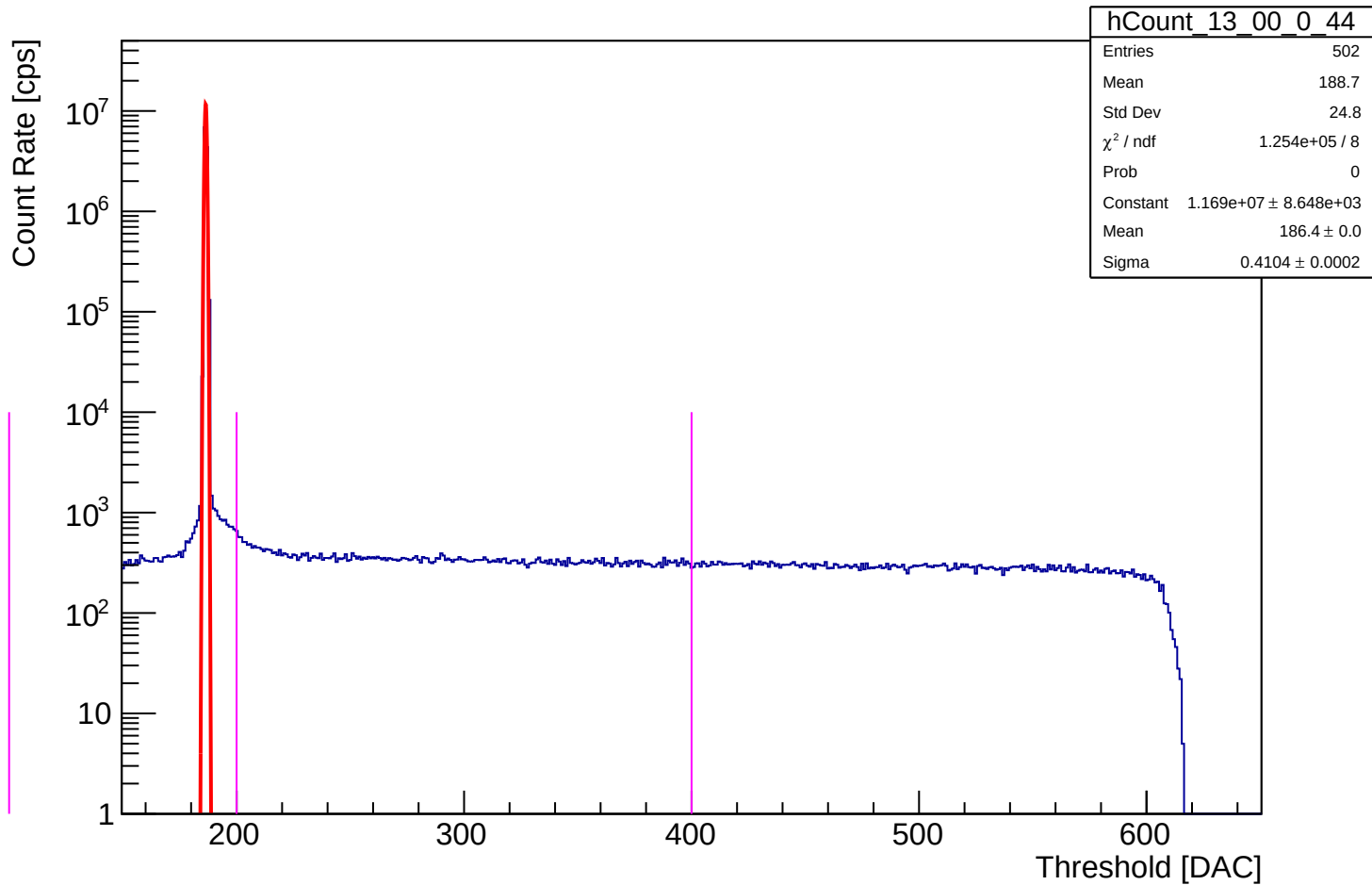
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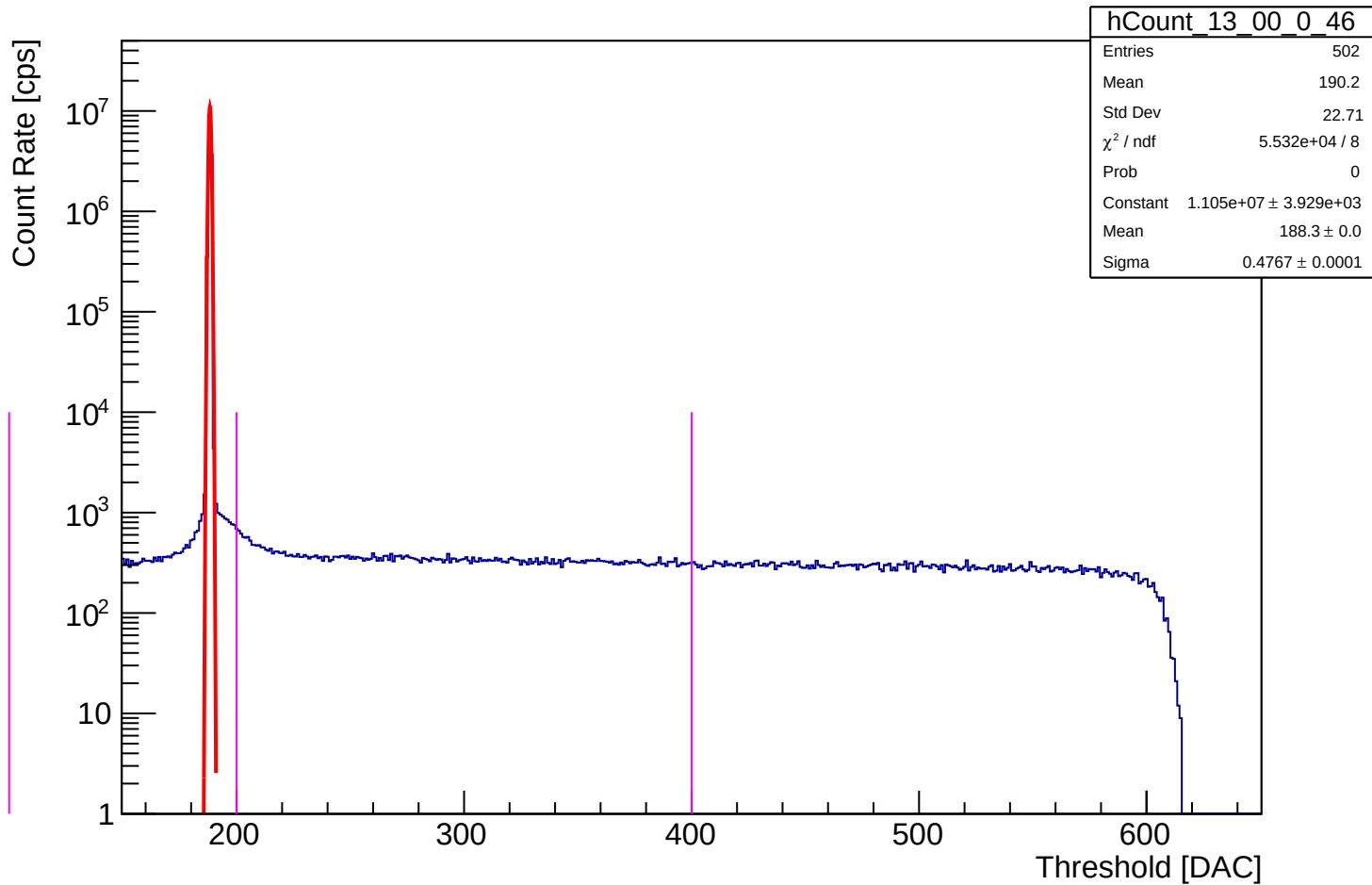
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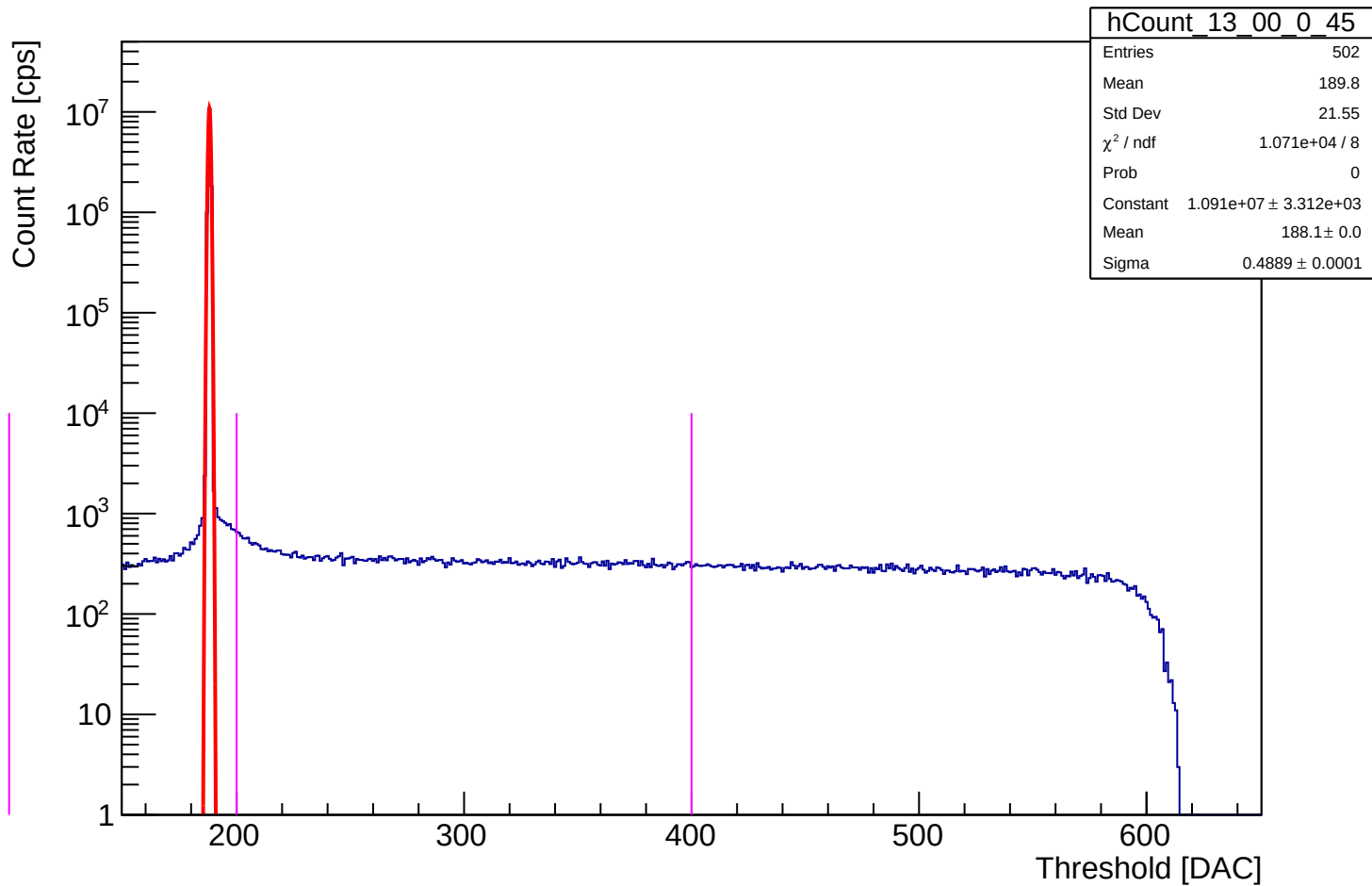
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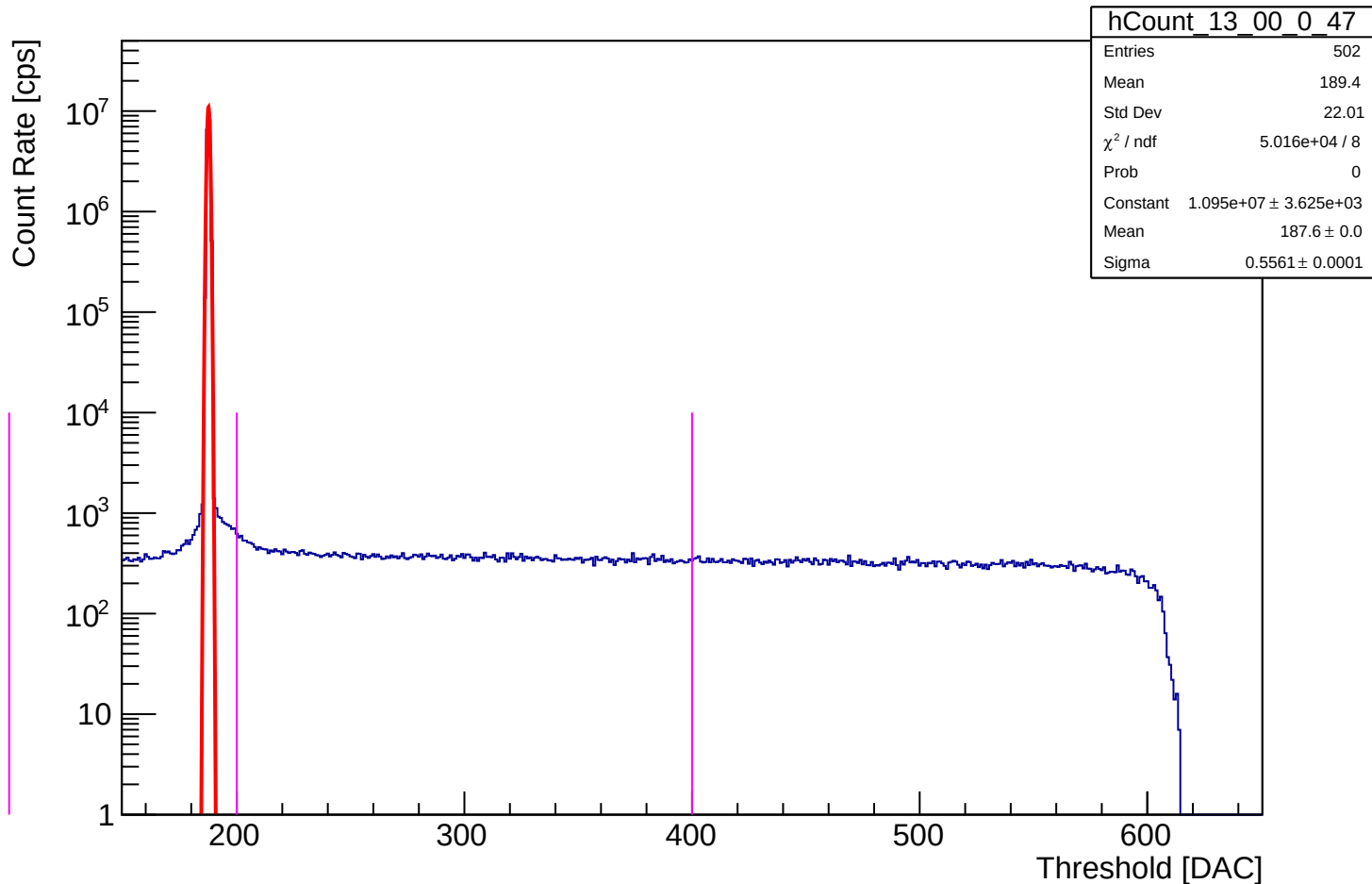
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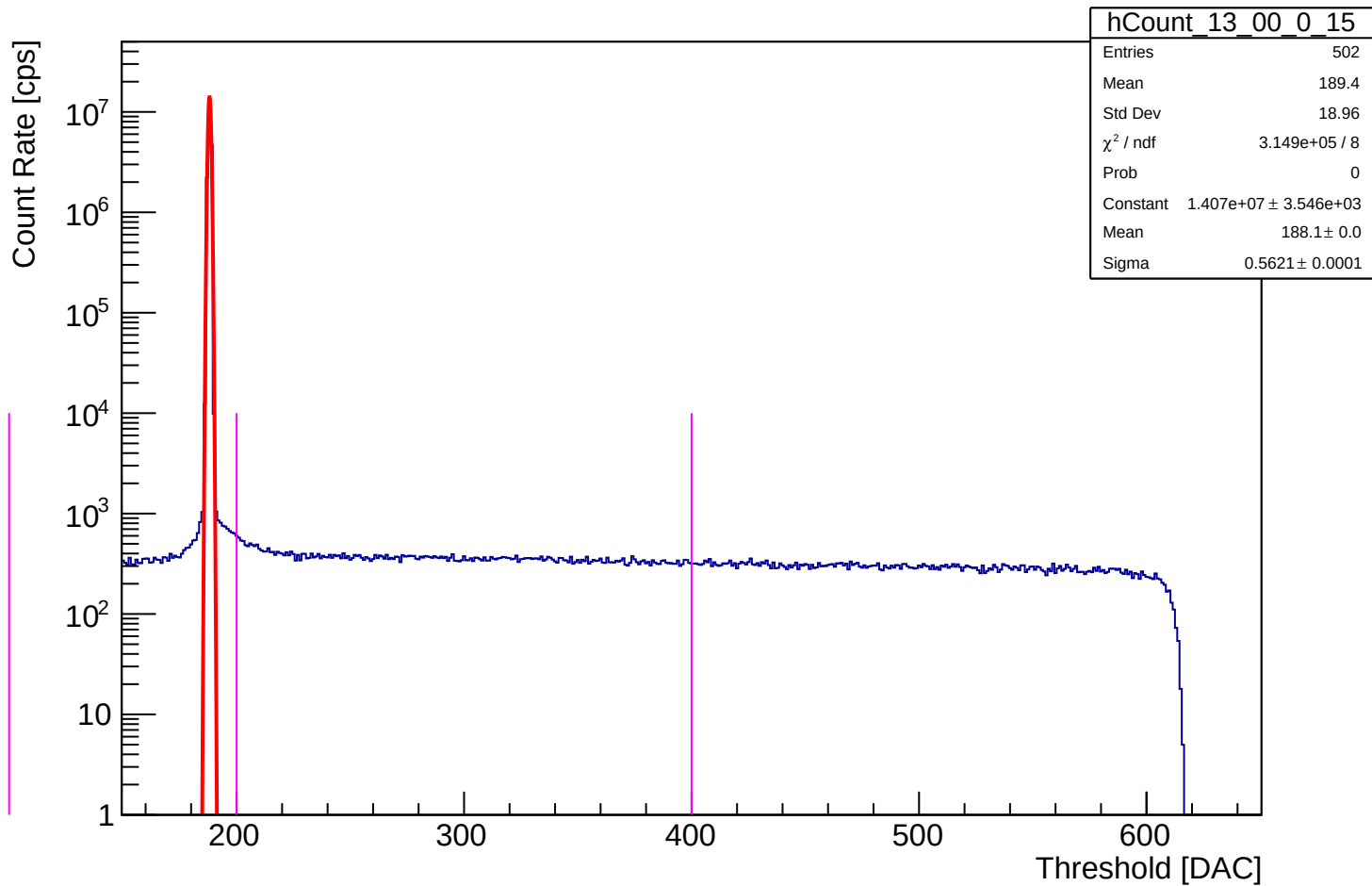
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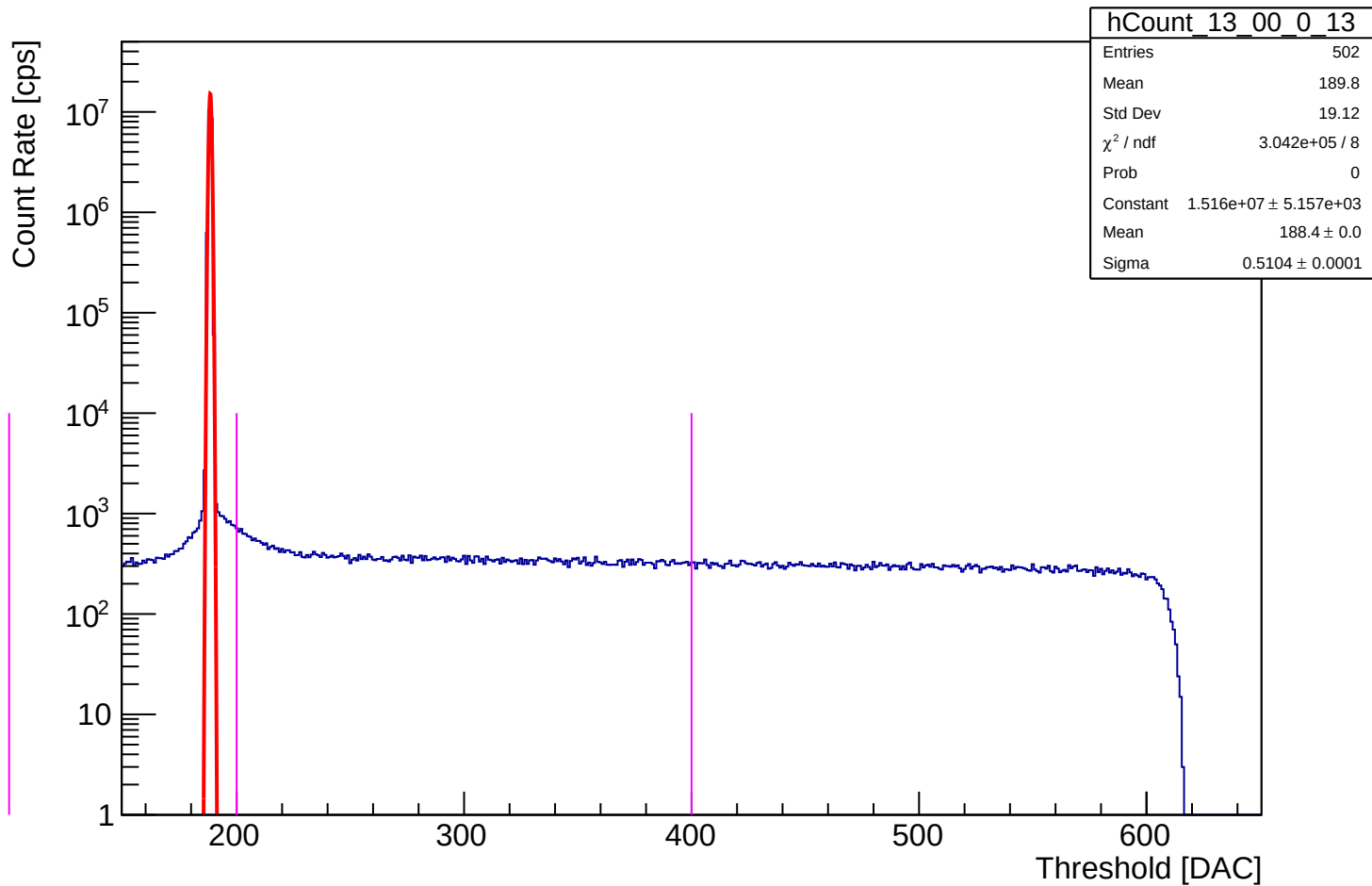
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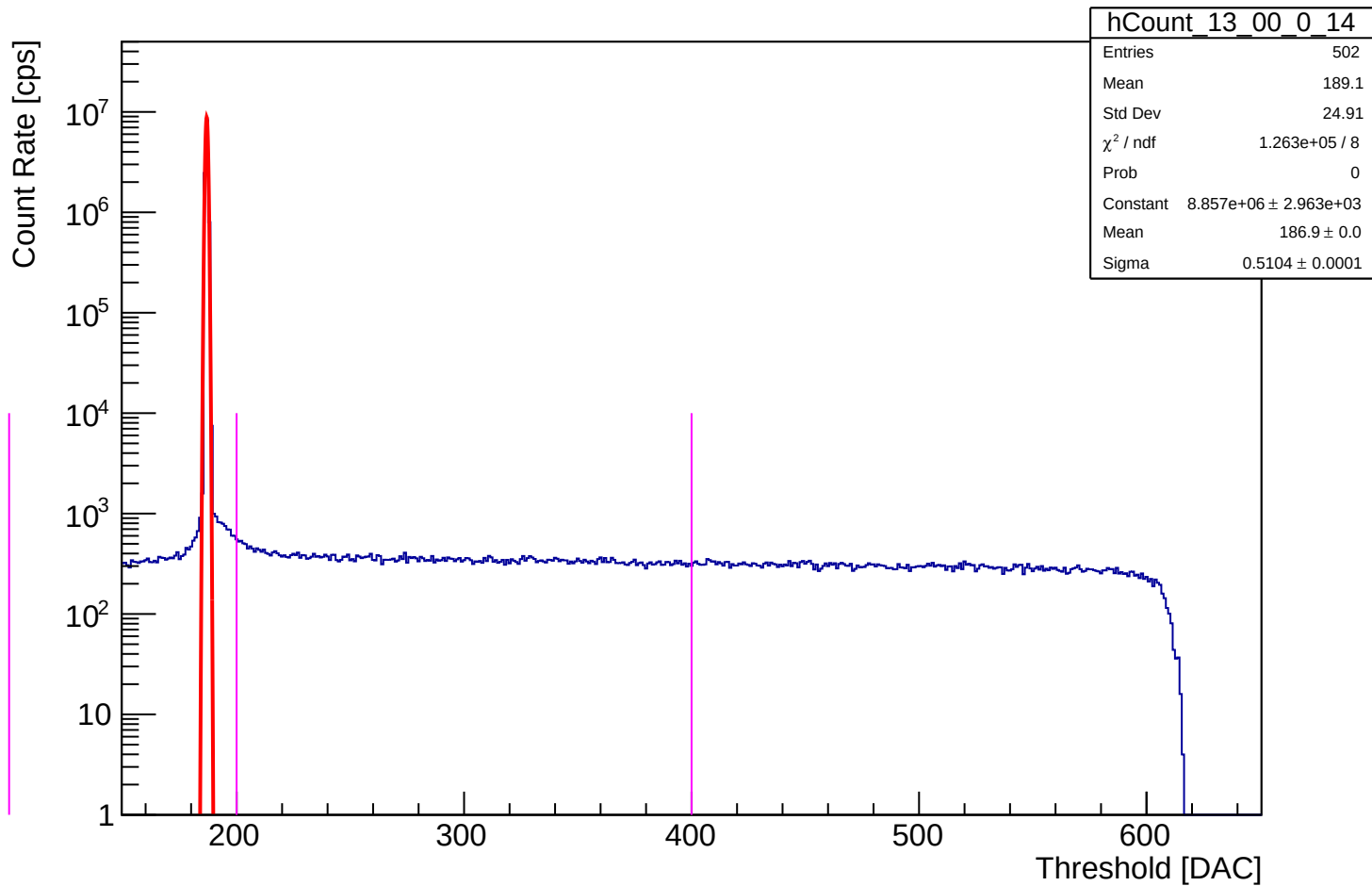
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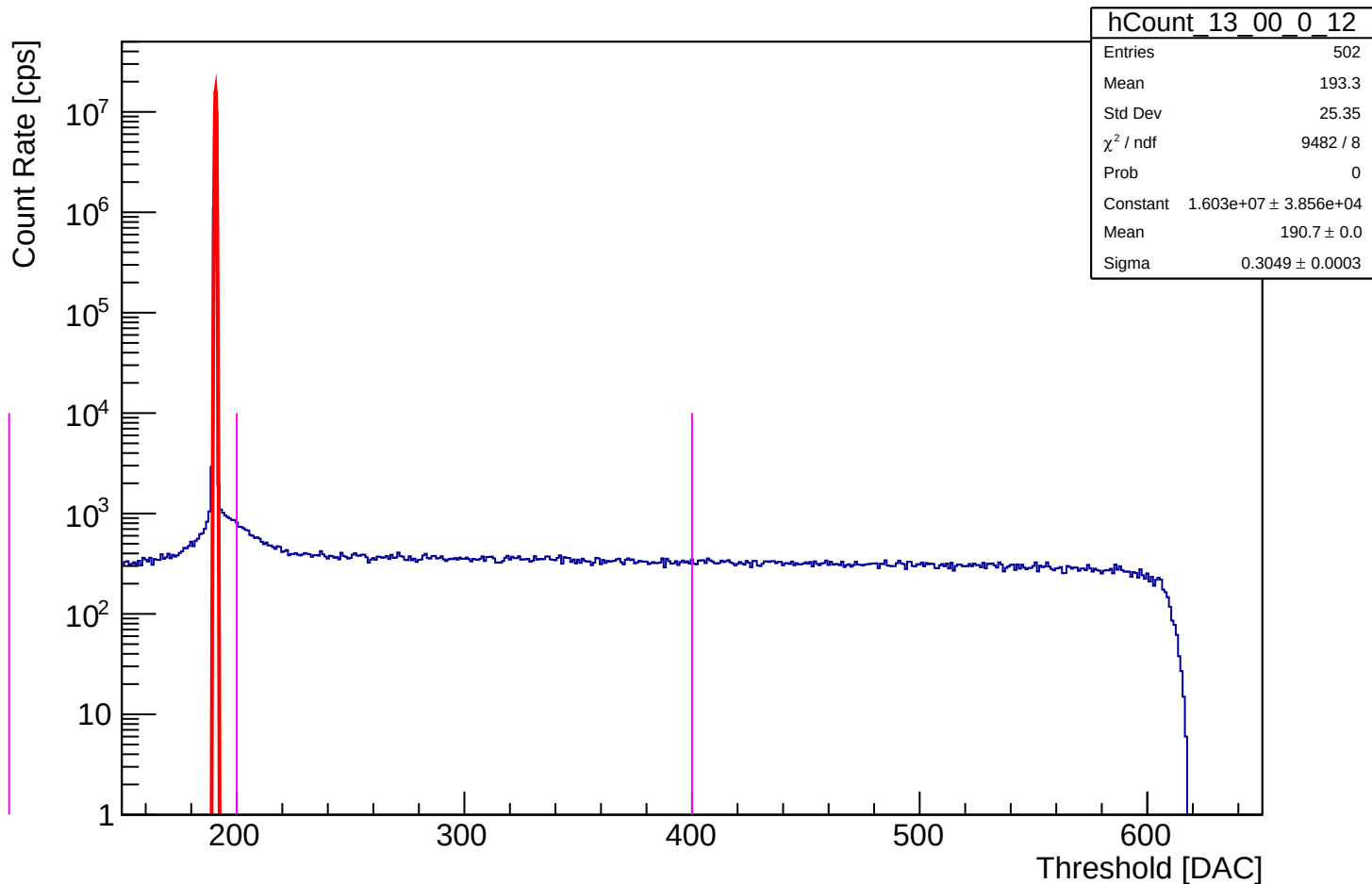
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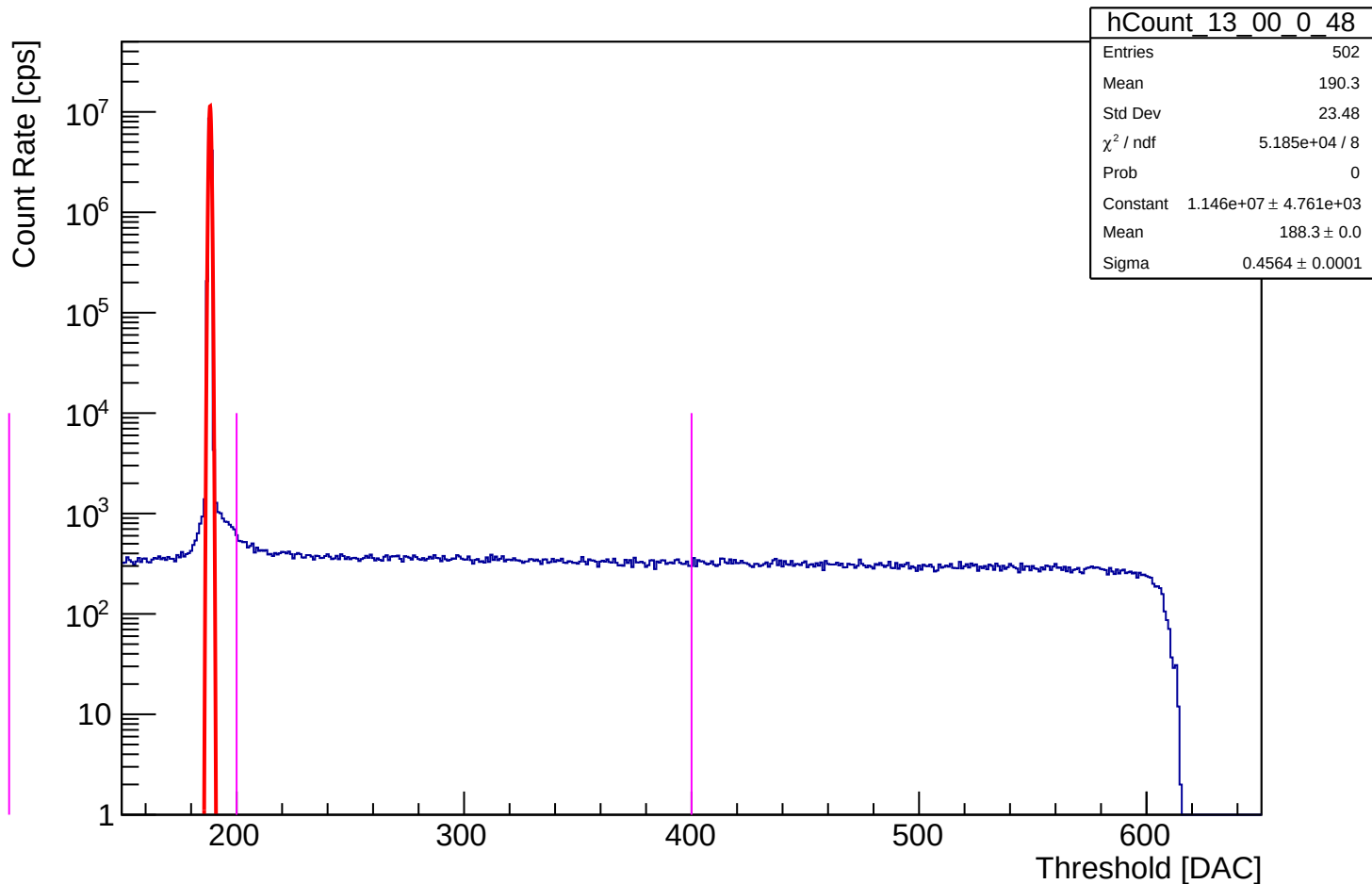
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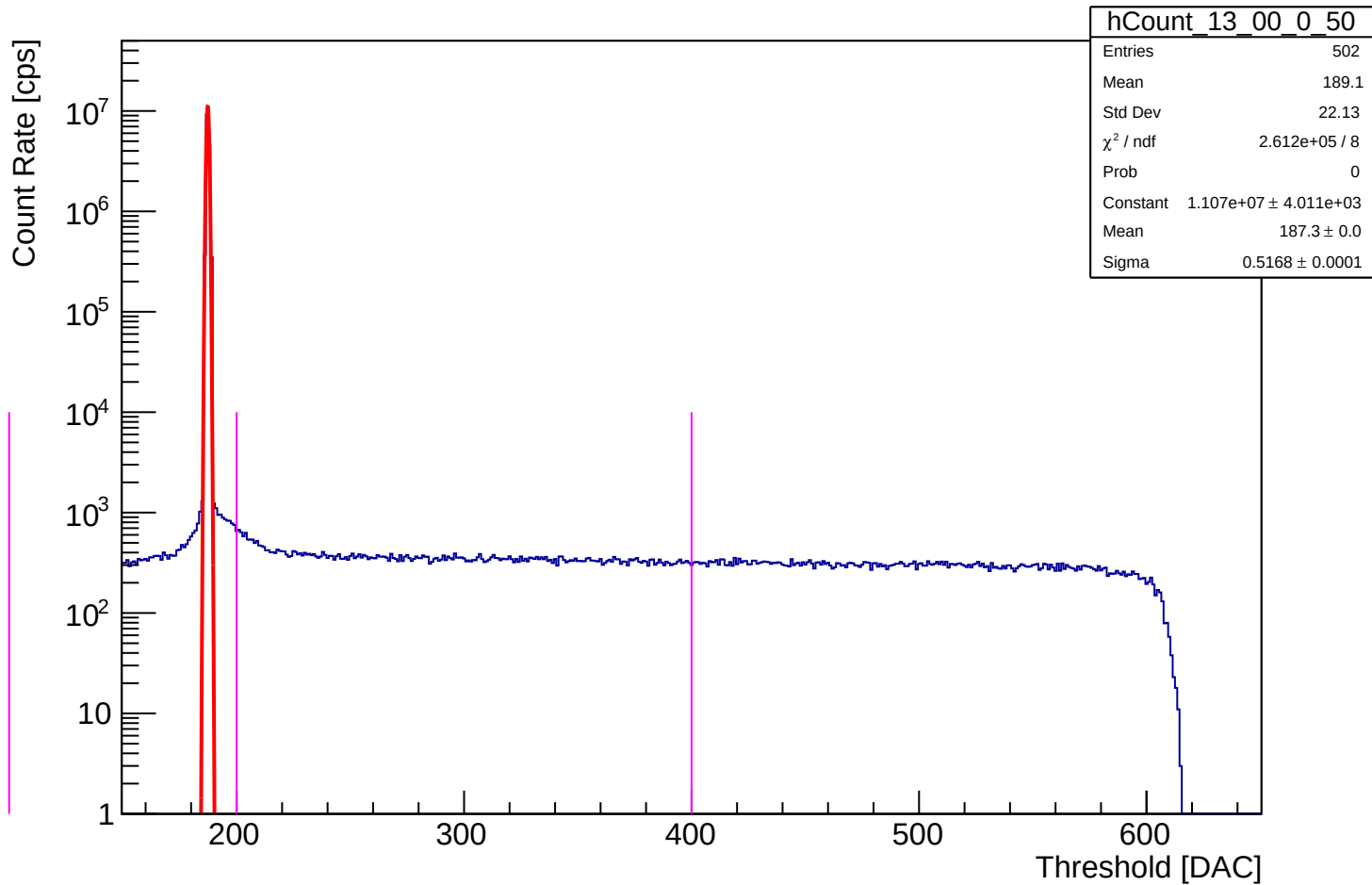
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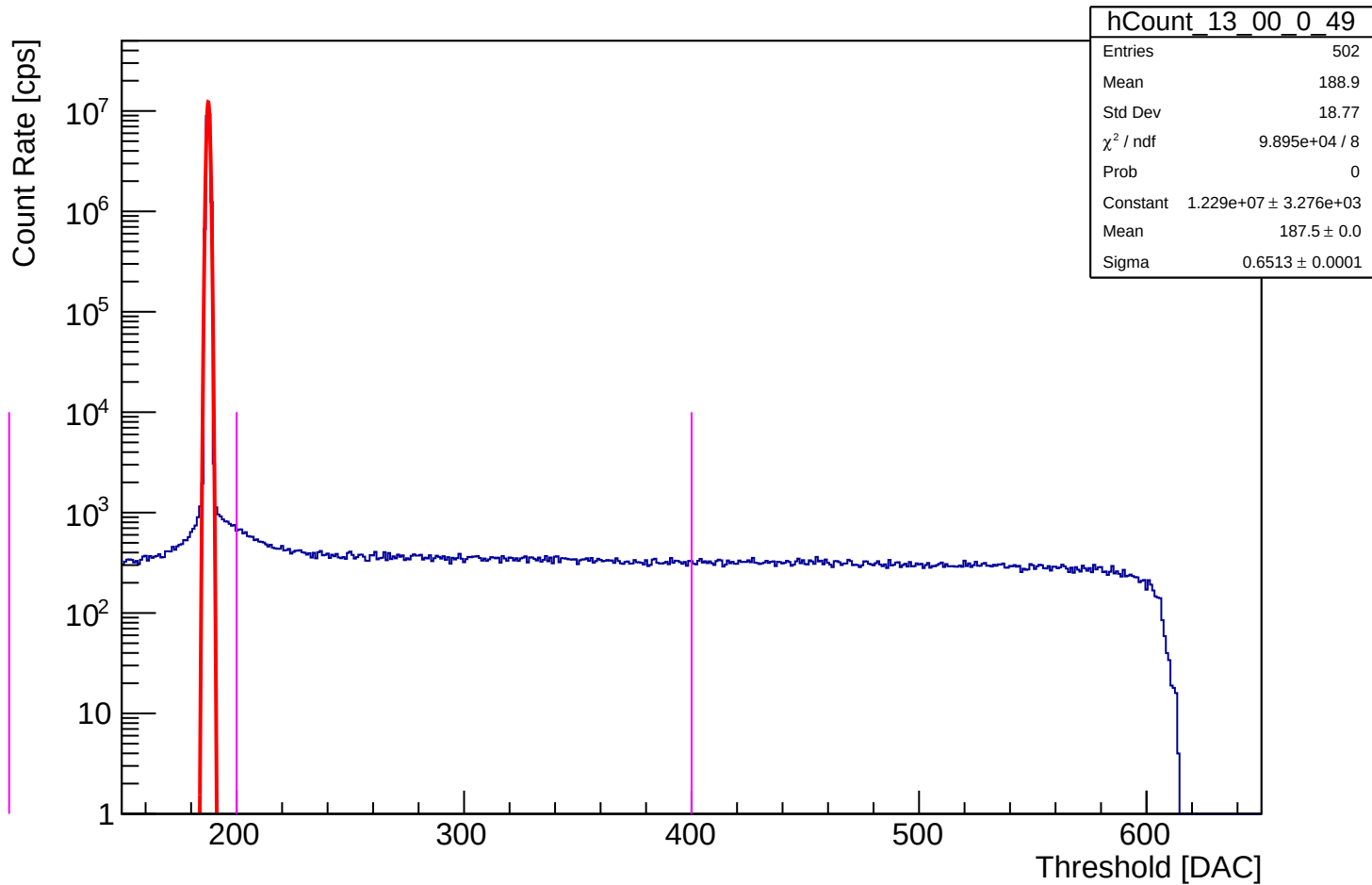
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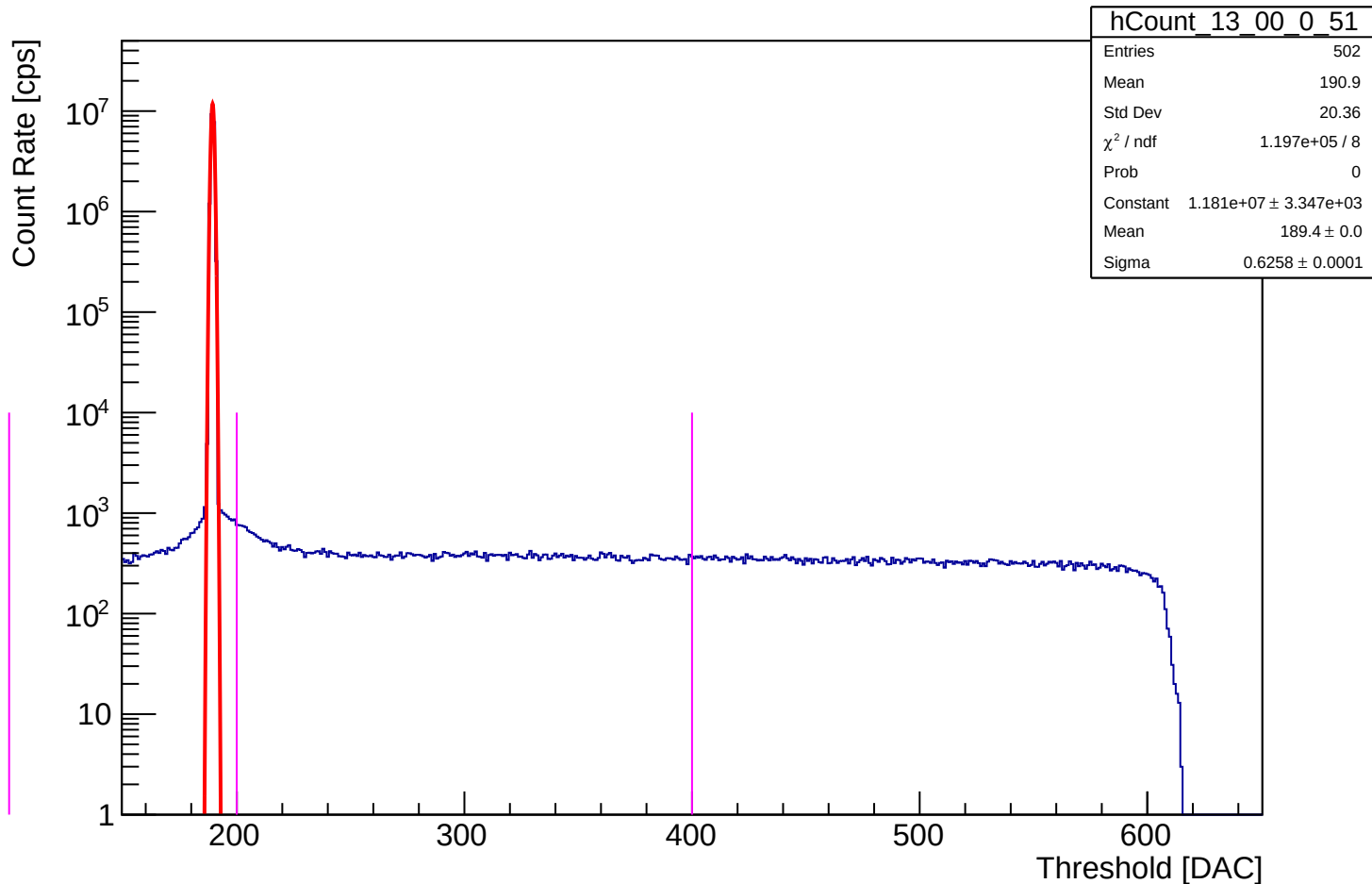
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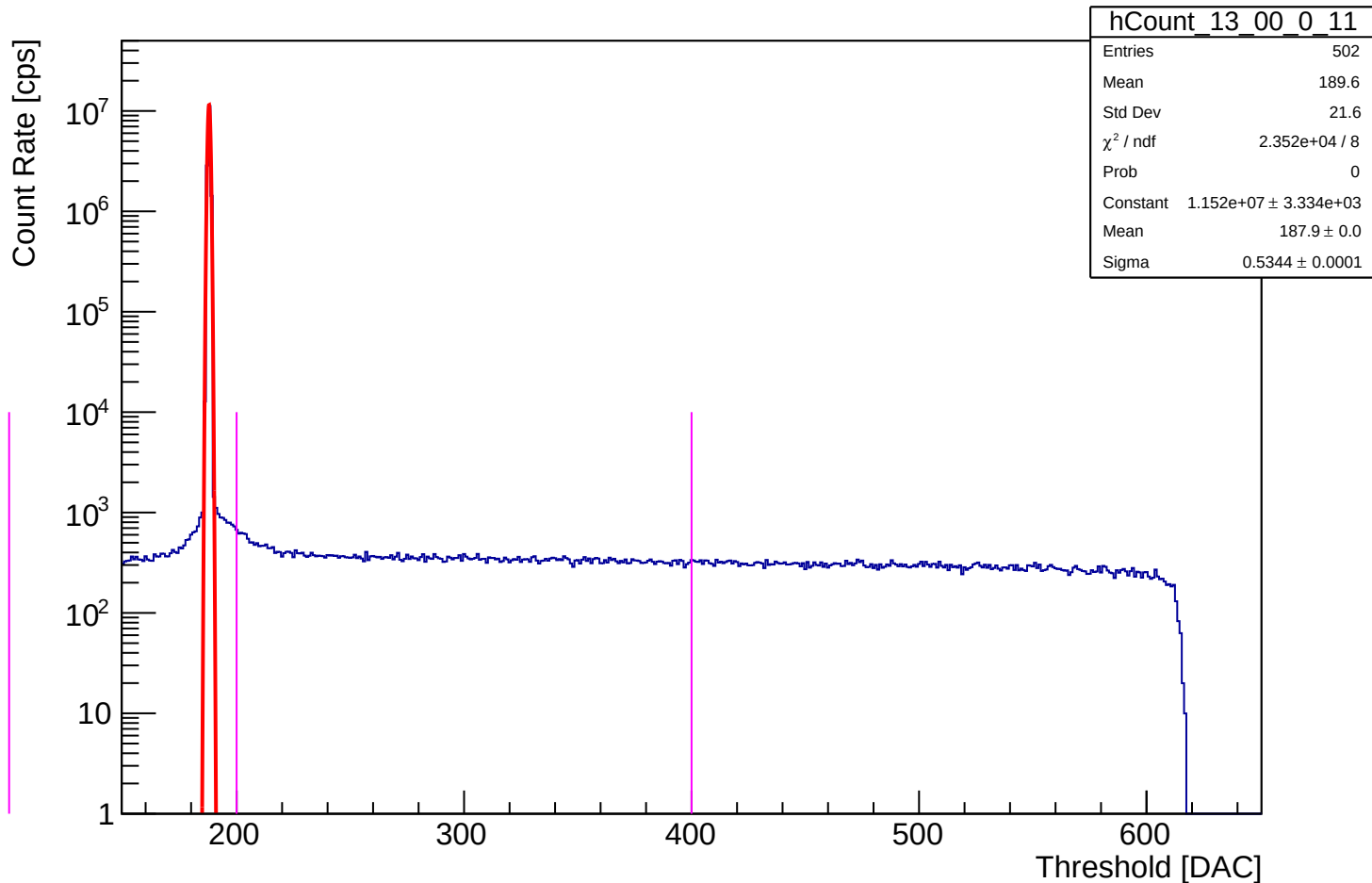
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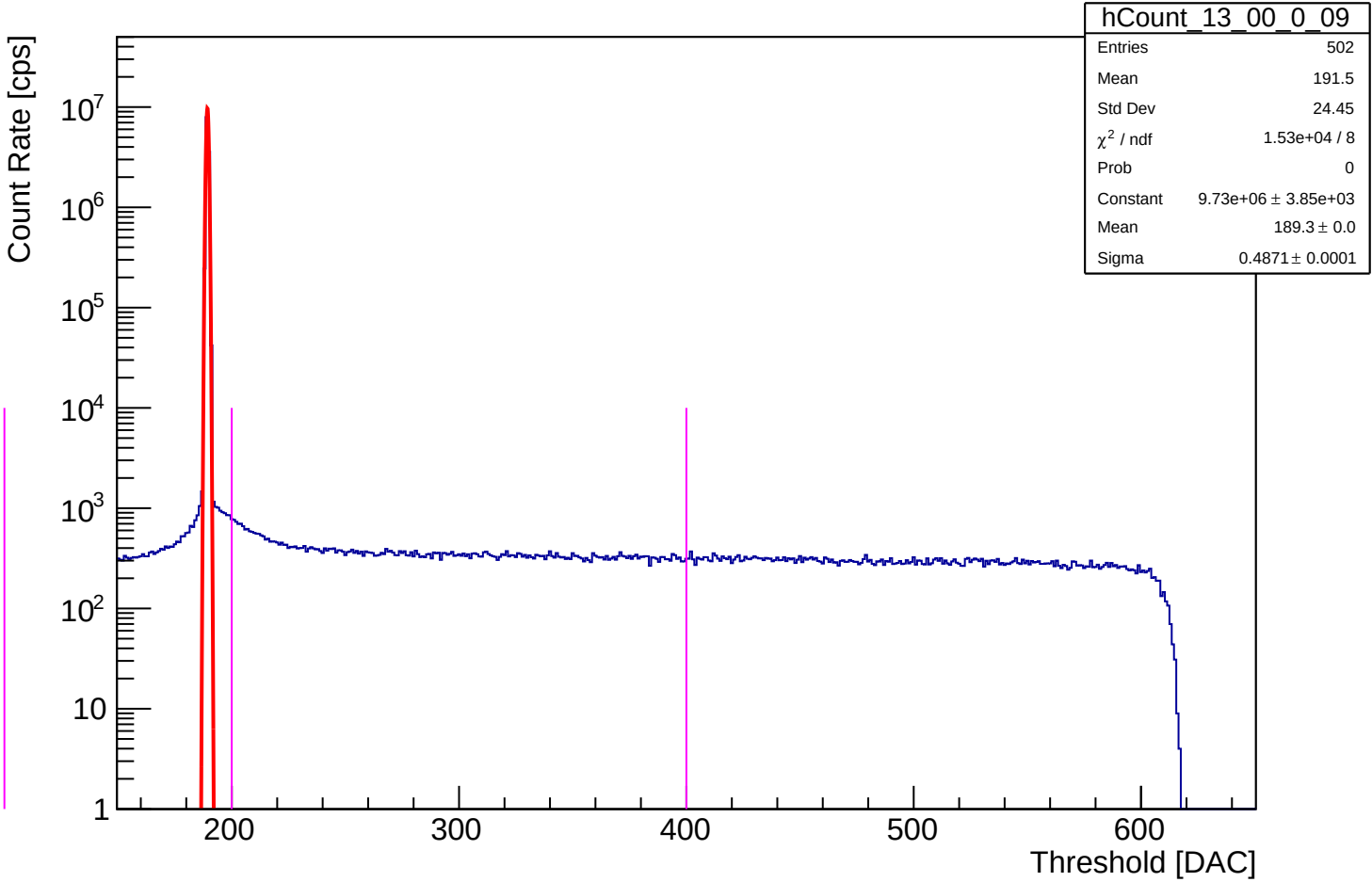


Row 1 Tile 1 Pmt 1 Pixel 40 Slot 13 Fiber 0 Asic 0 Channel 51

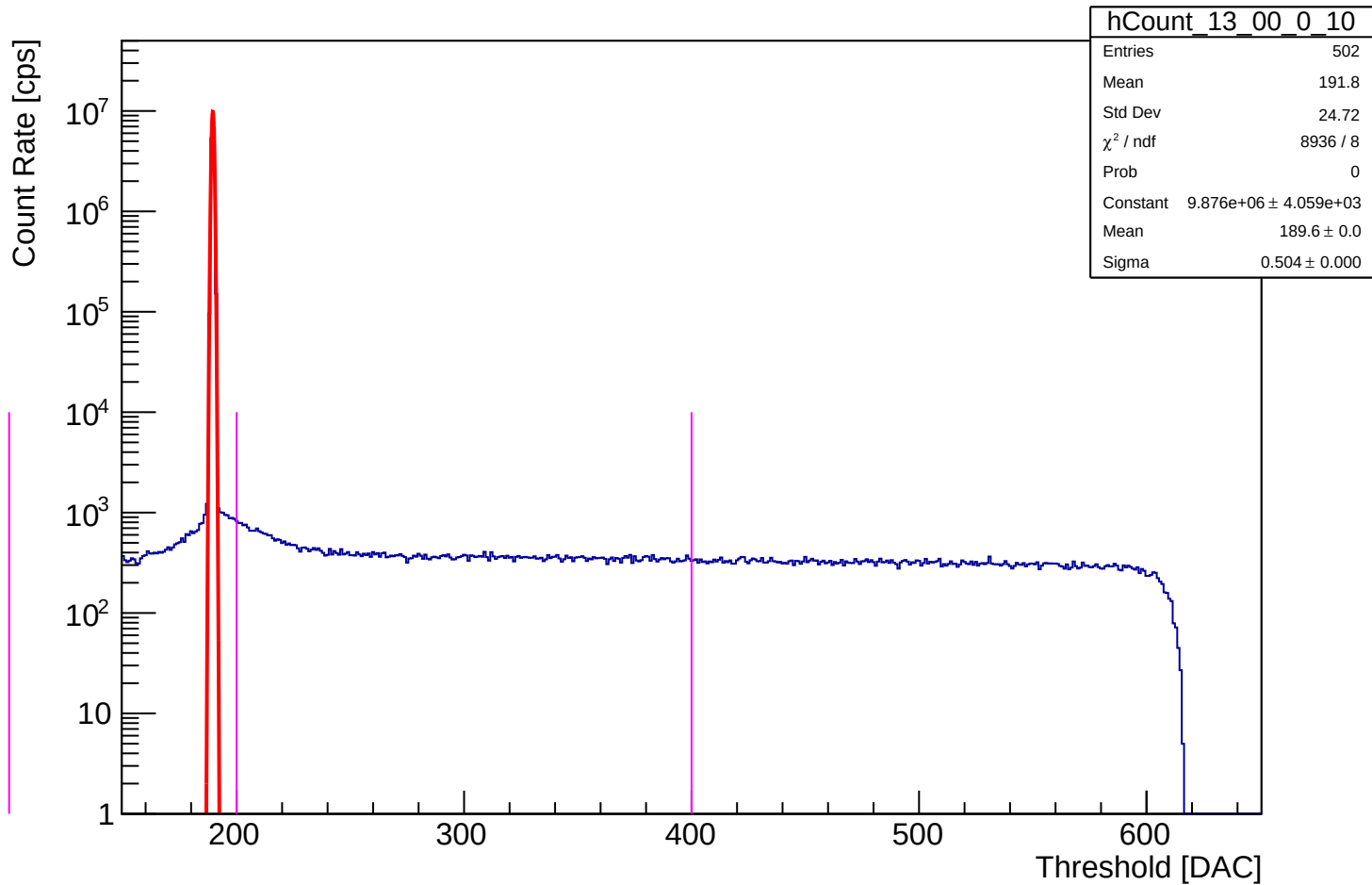


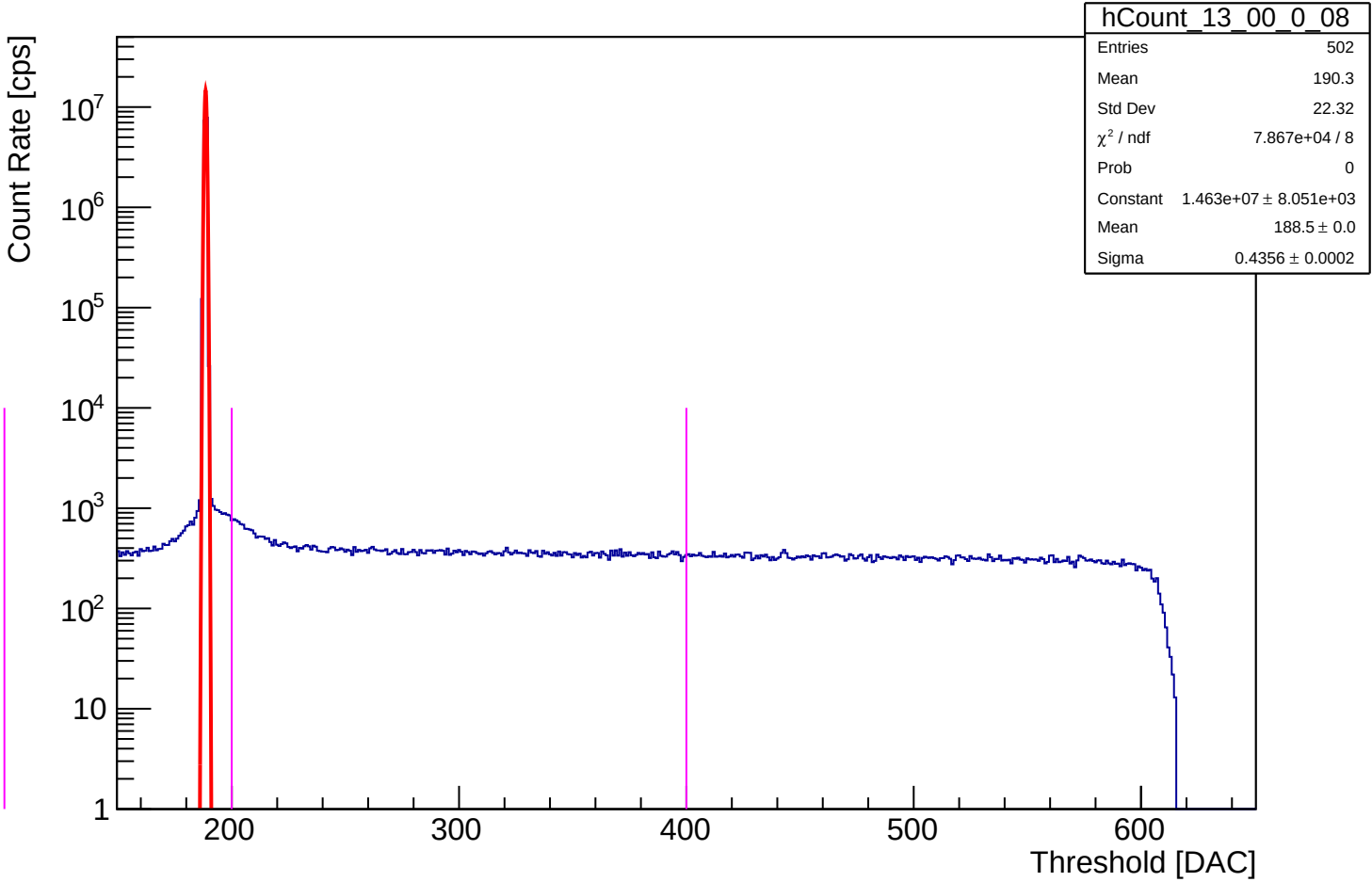
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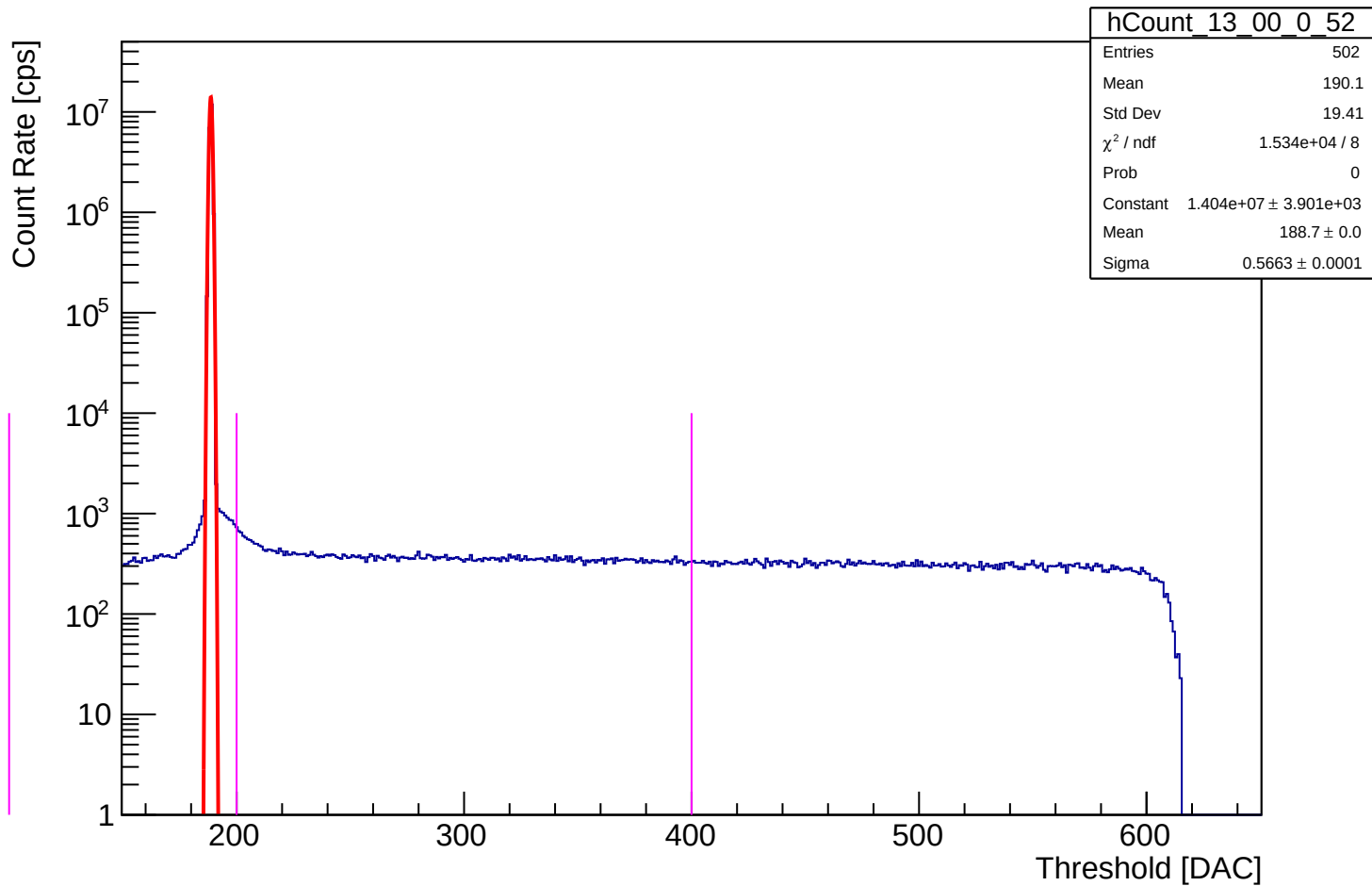


Row 1 Tile 1 Pmt 1 Pixel 43 Slot 13 Fiber 0 Asic 0 Channel 10

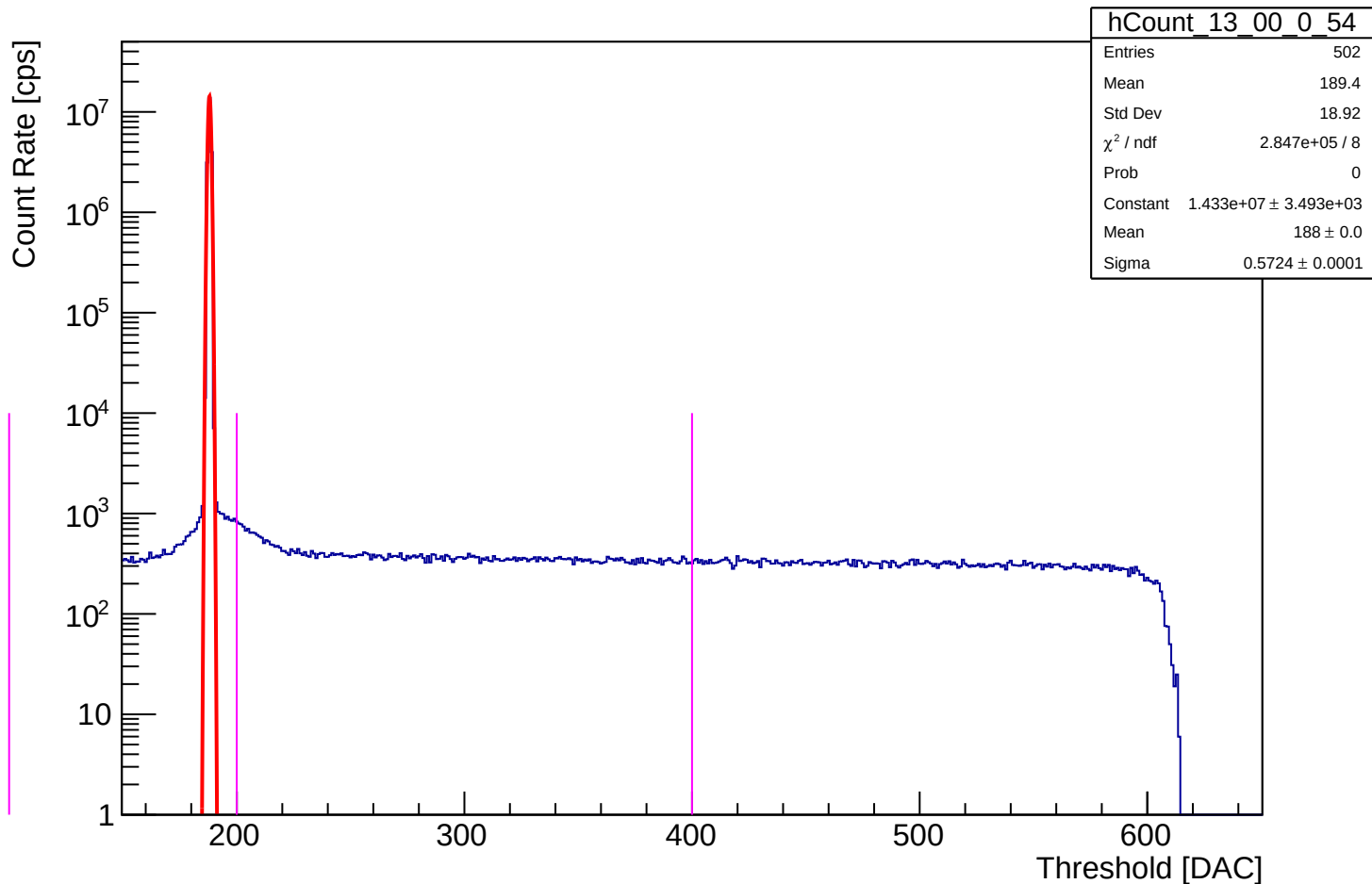




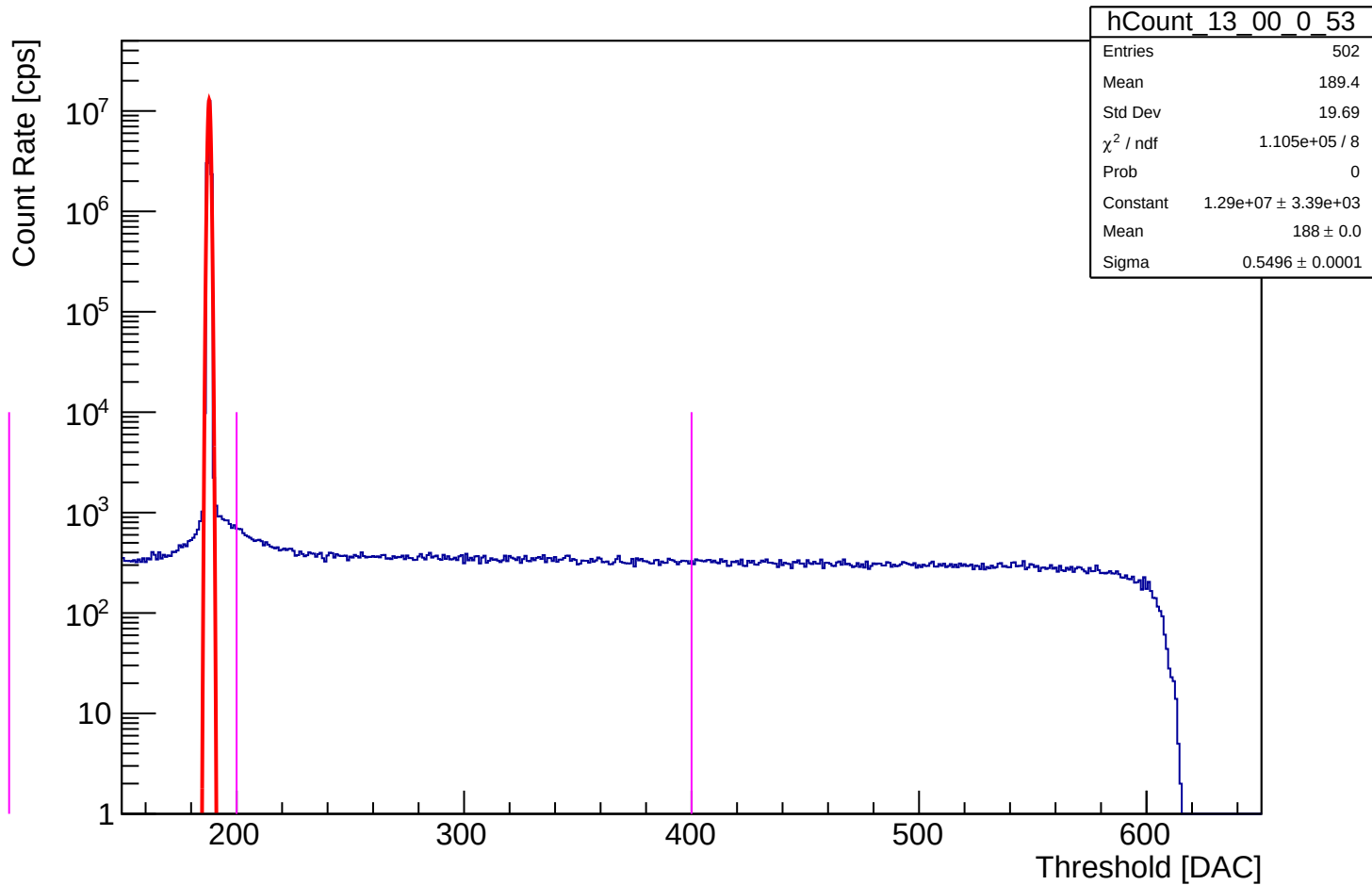
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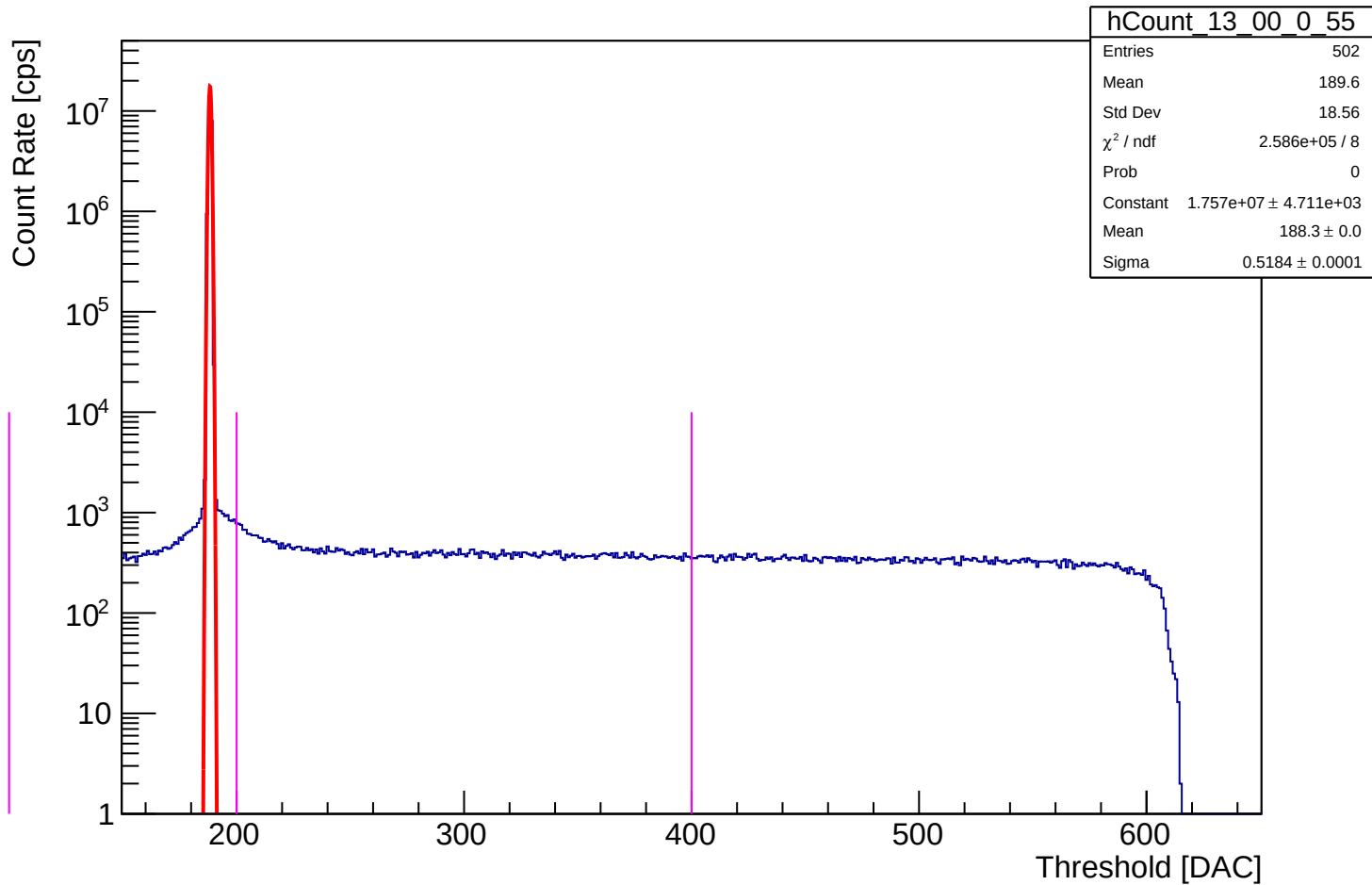
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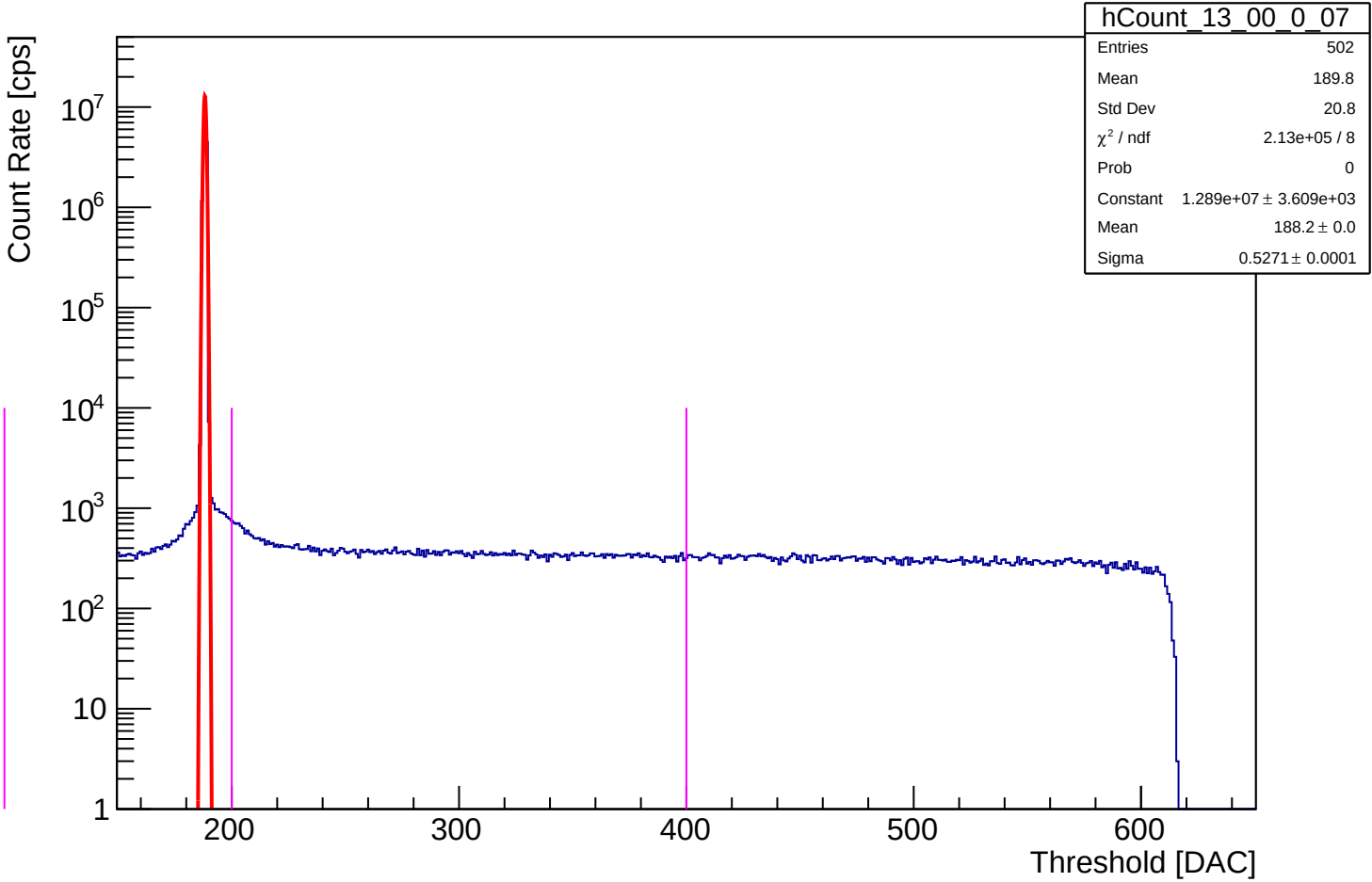


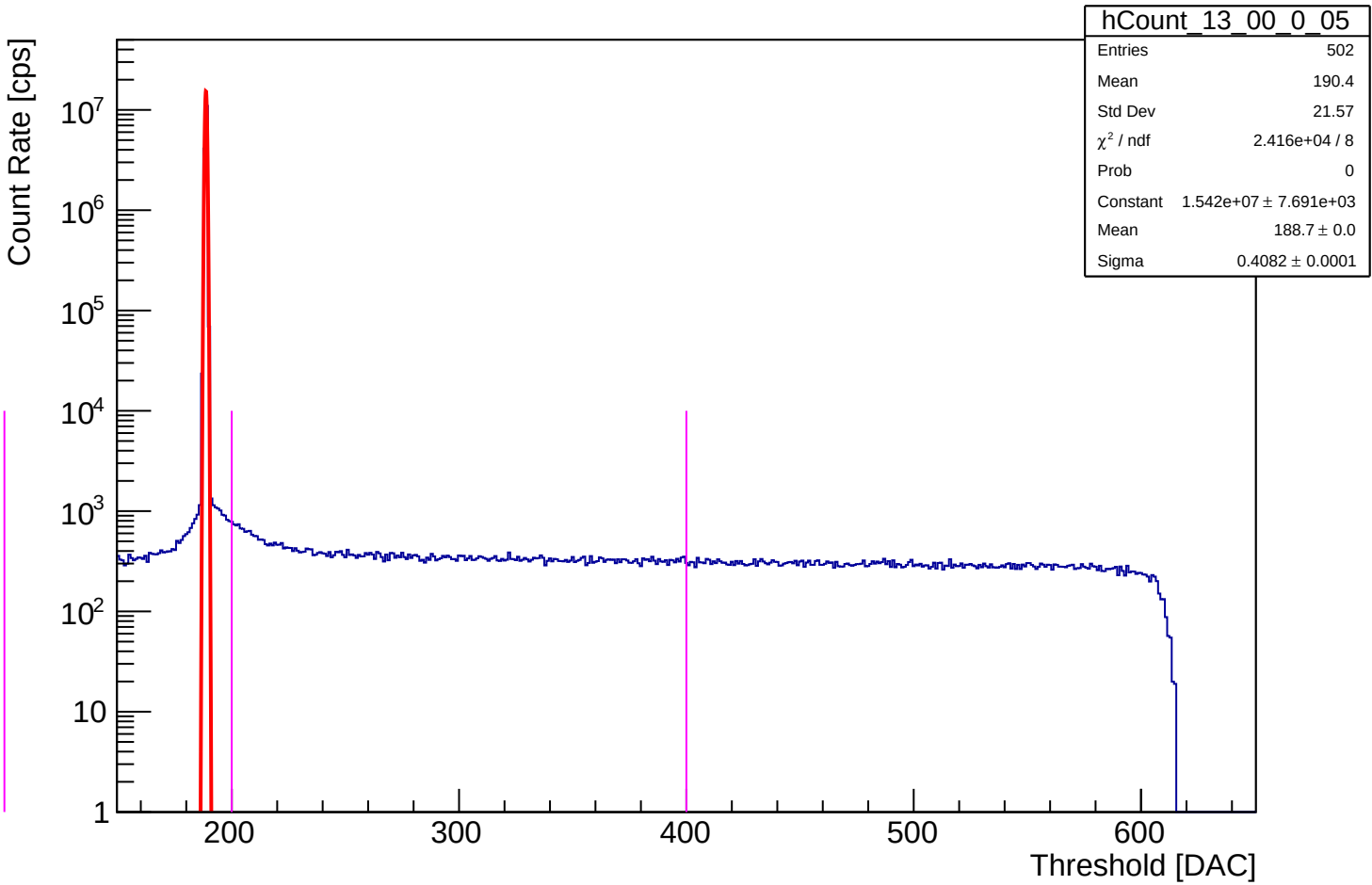
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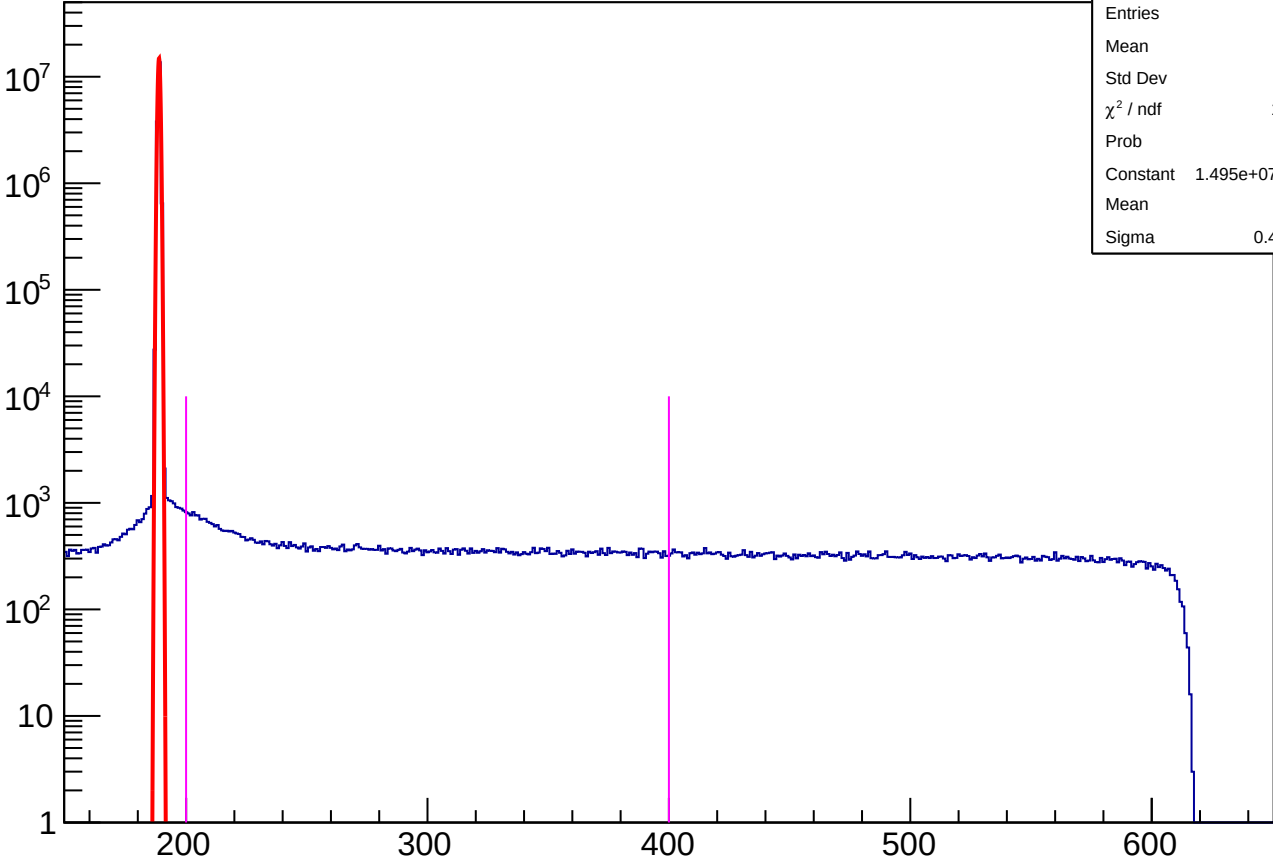
Row 1 Tile 1 Pmt 1 Pixel 48 Slot 13 Fiber 0 Asic 0 Channel 55







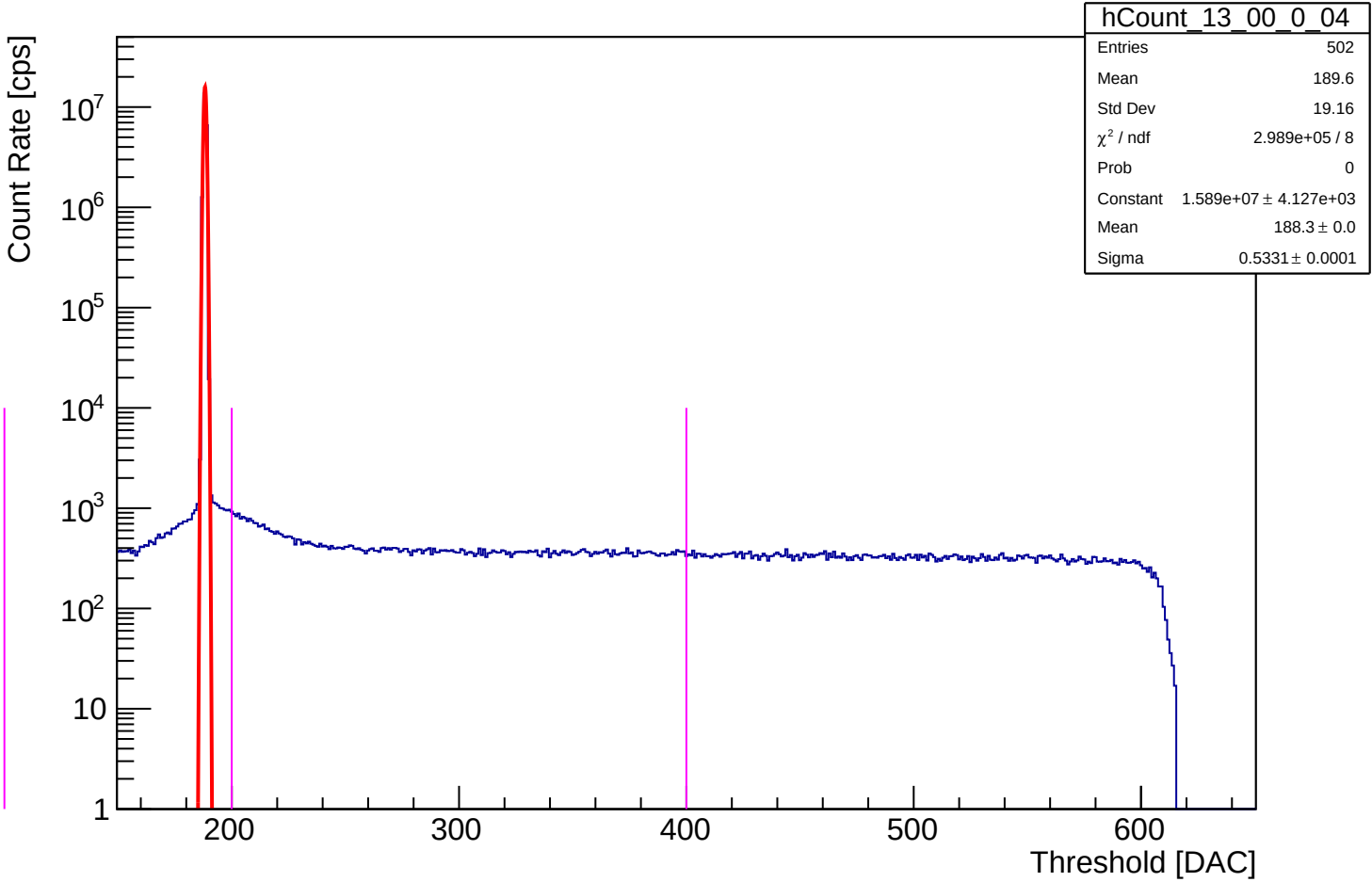
Count Rate [cps]



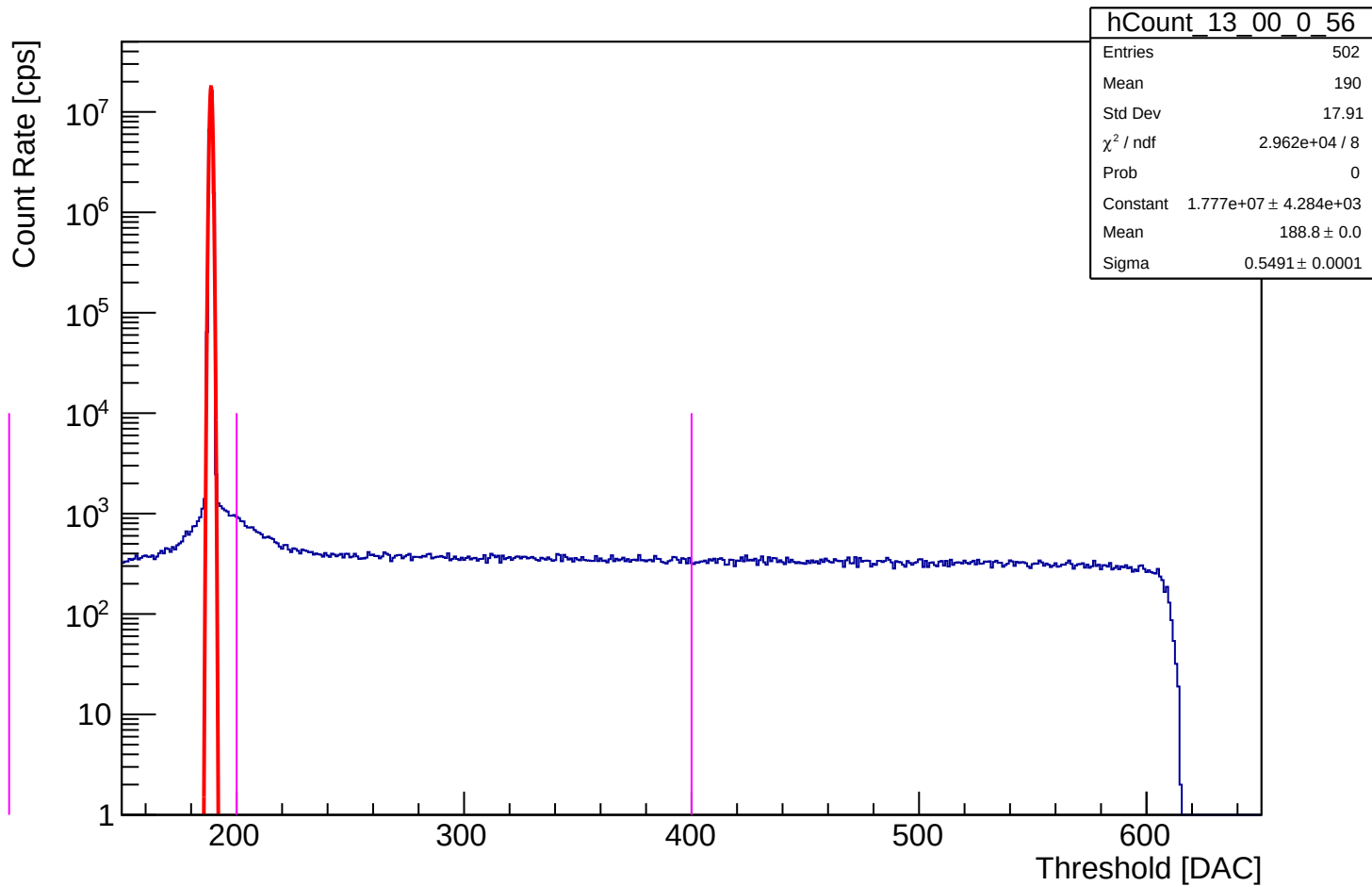
hCount 13 00 0 06

Entries	502
Mean	190.4
Std Dev	20.55
χ^2 / ndf	1.401e+04 / 8
Prob	0
Constant	1.495e+07 ± 4.261e+03
Mean	188.8 ± 0.0
Sigma	0.4816 ± 0.0001

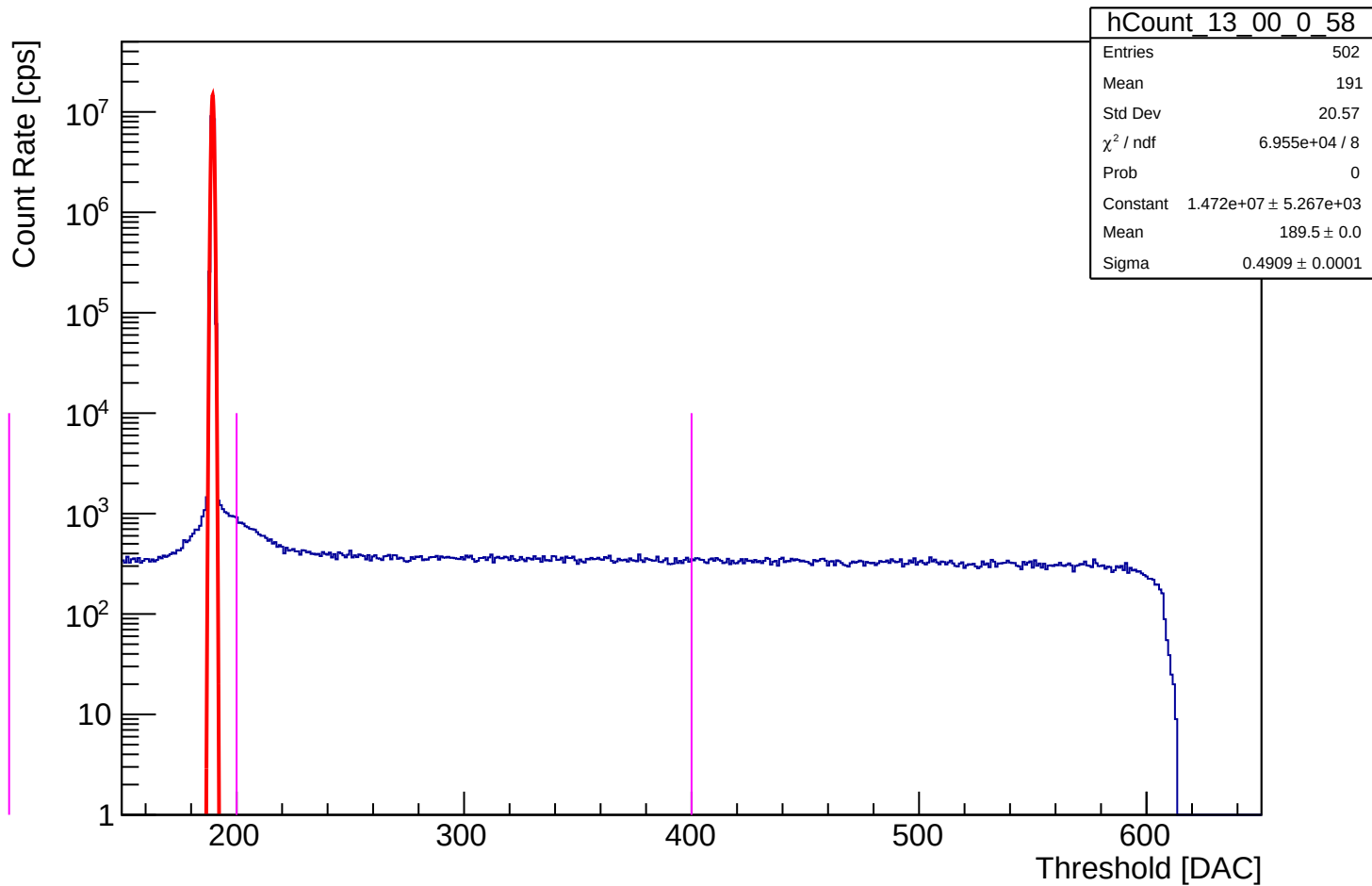
Threshold [DAC]



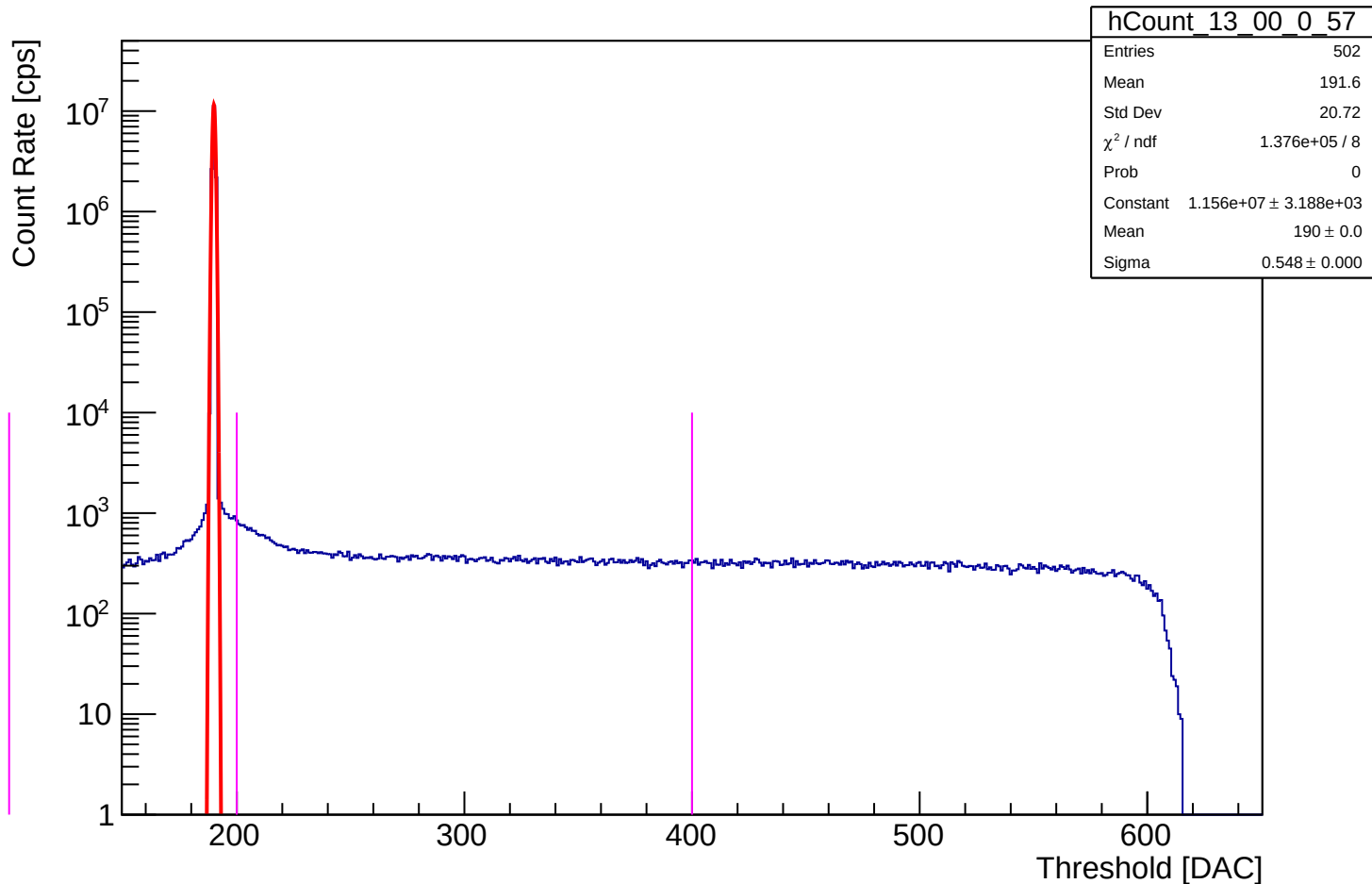
Row 1 Tile 1 Pmt 1 Pixel 53 Slot 13 Fiber 0 Asic 0 Channel 56



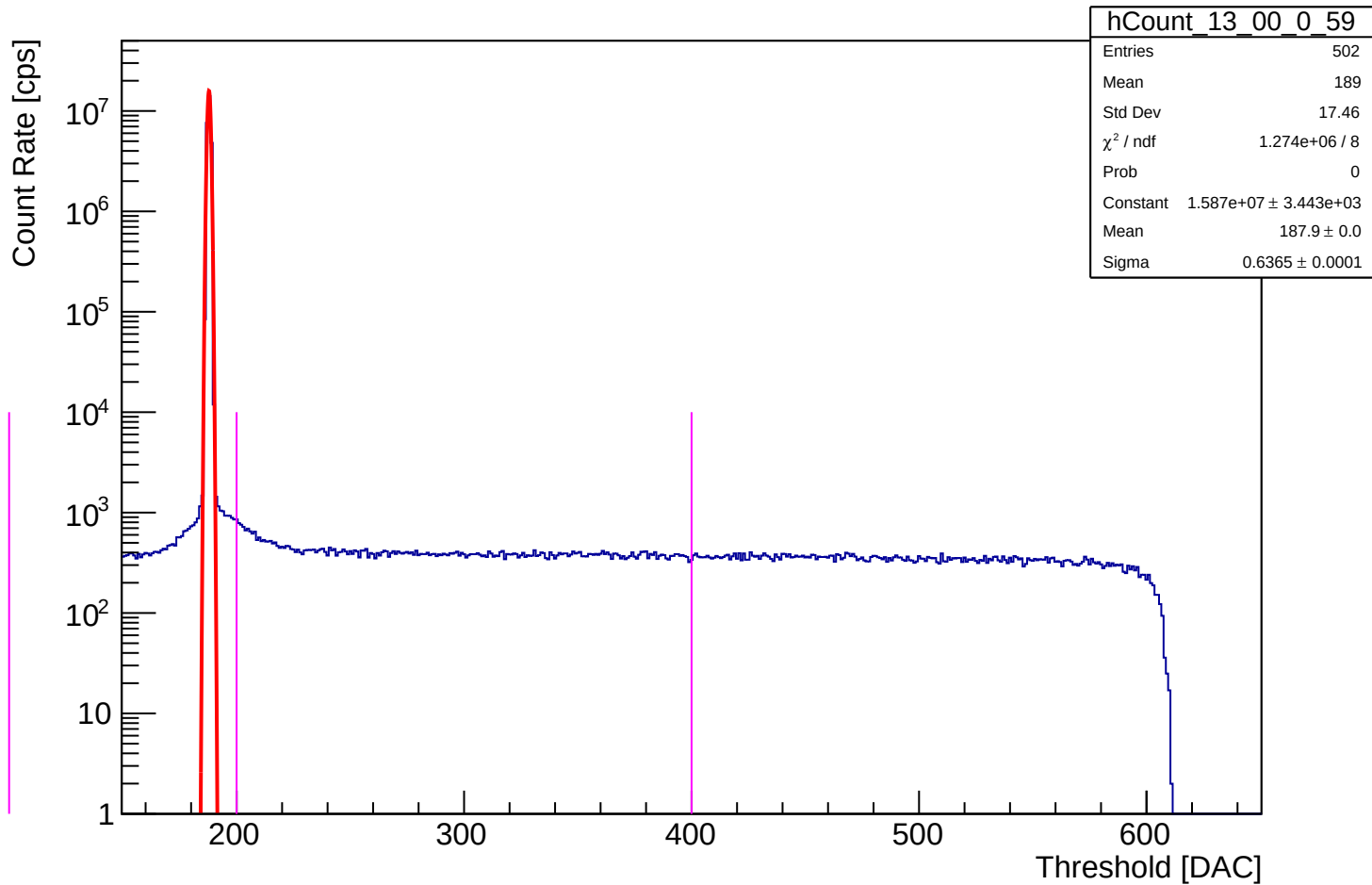
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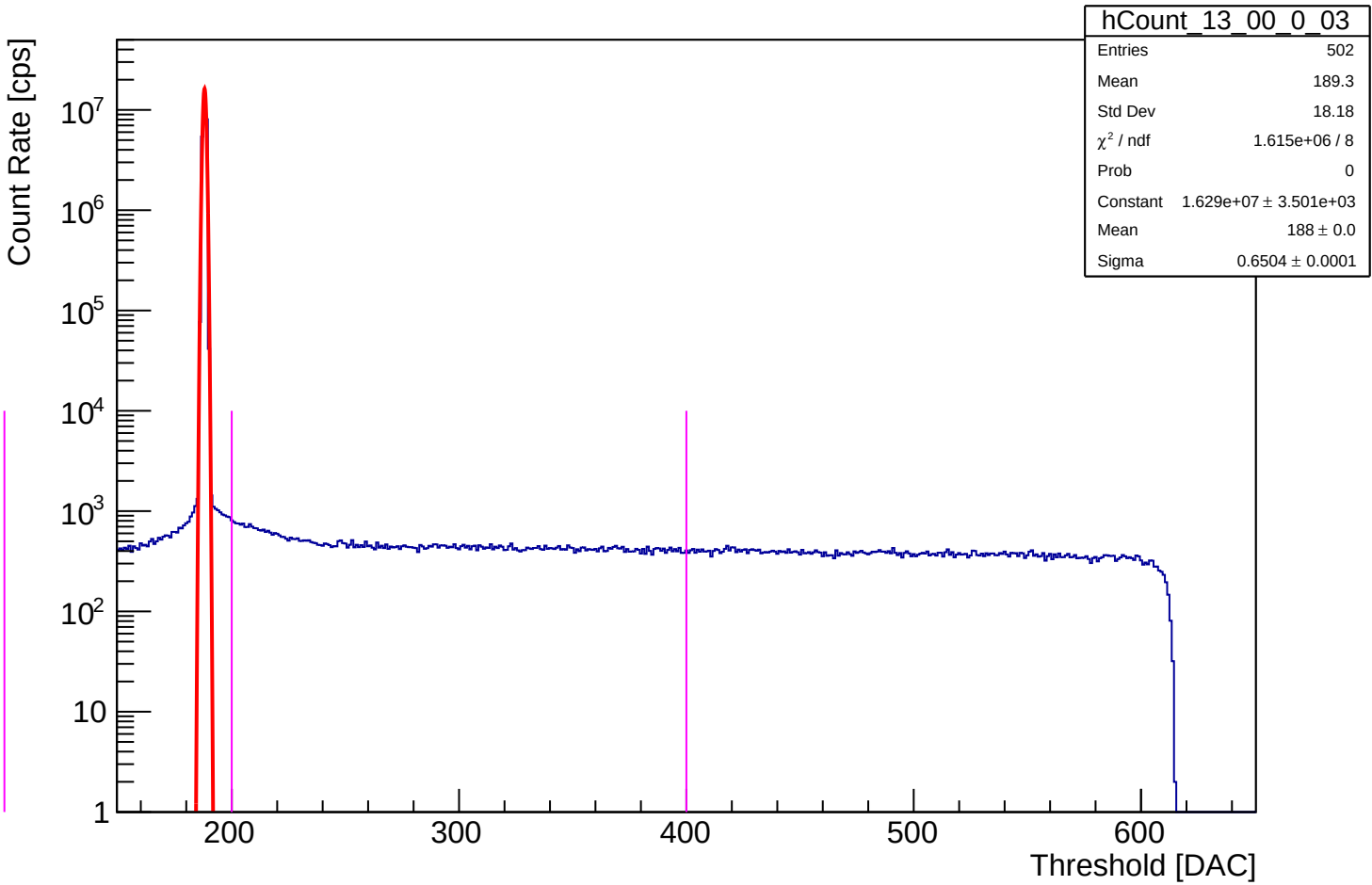


Row 1 Tile 1 Pmt 1 Pixel 55 Slot 13 Fiber 0 Asic 0 Channel 57

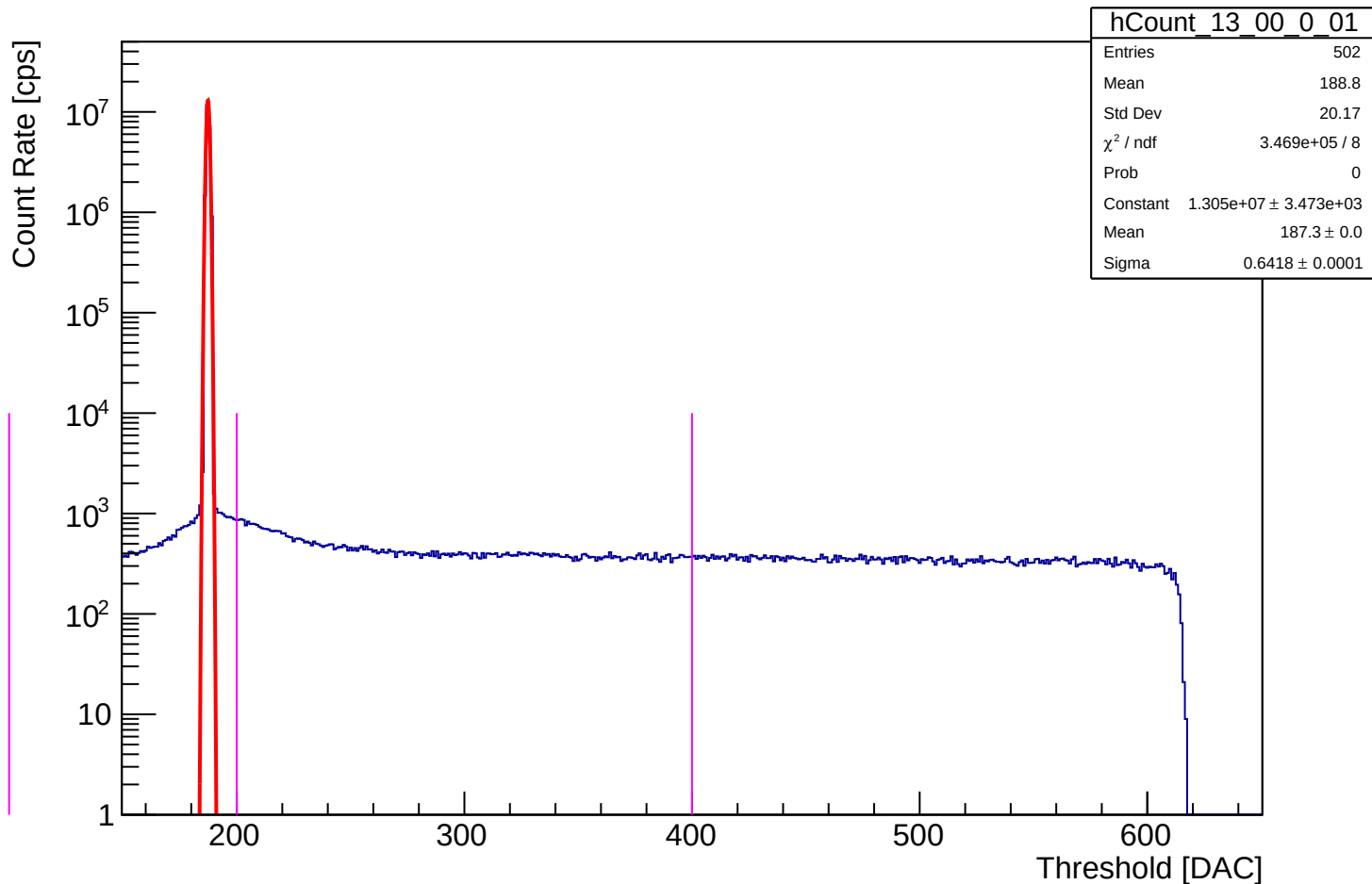


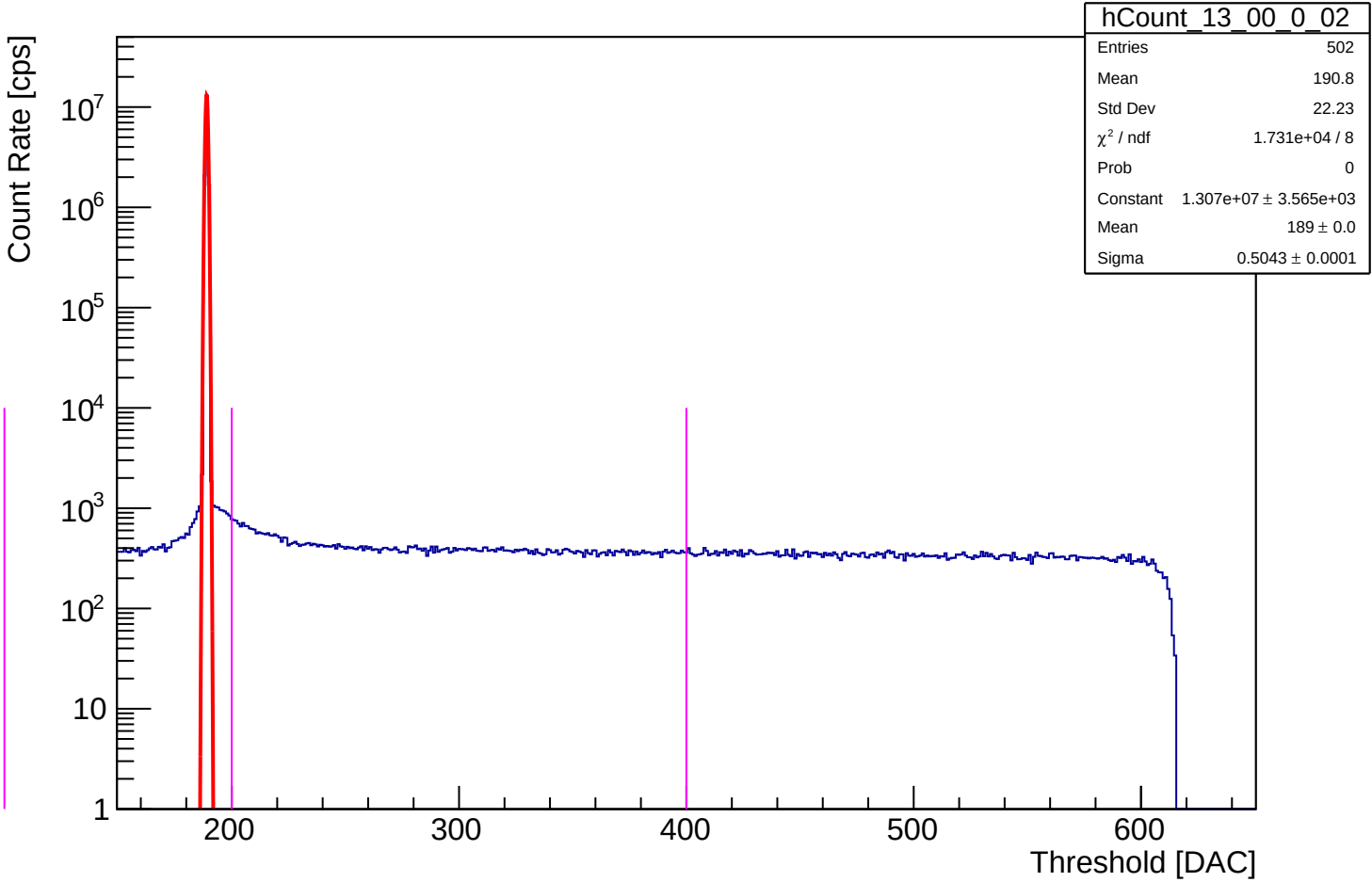
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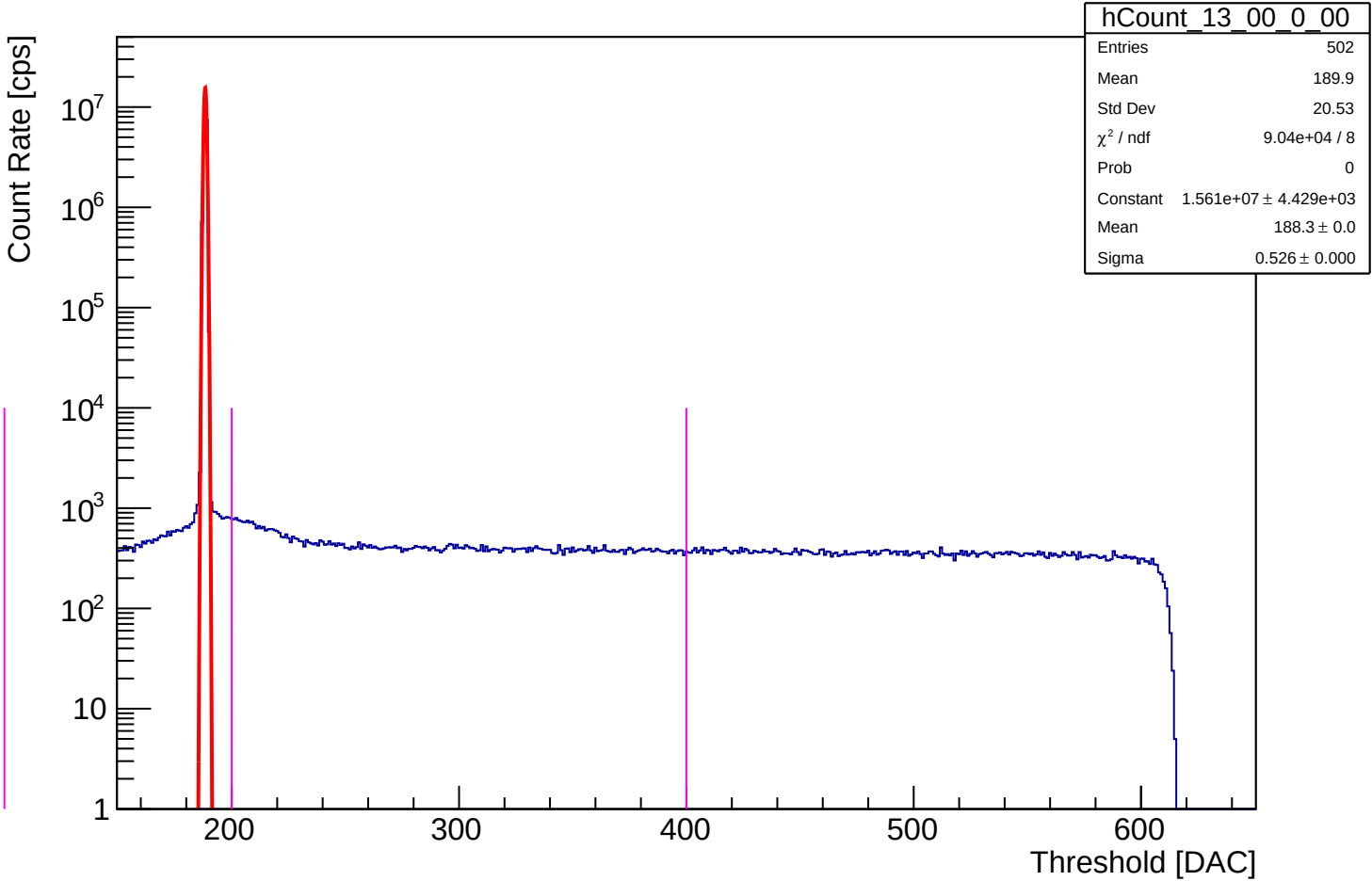




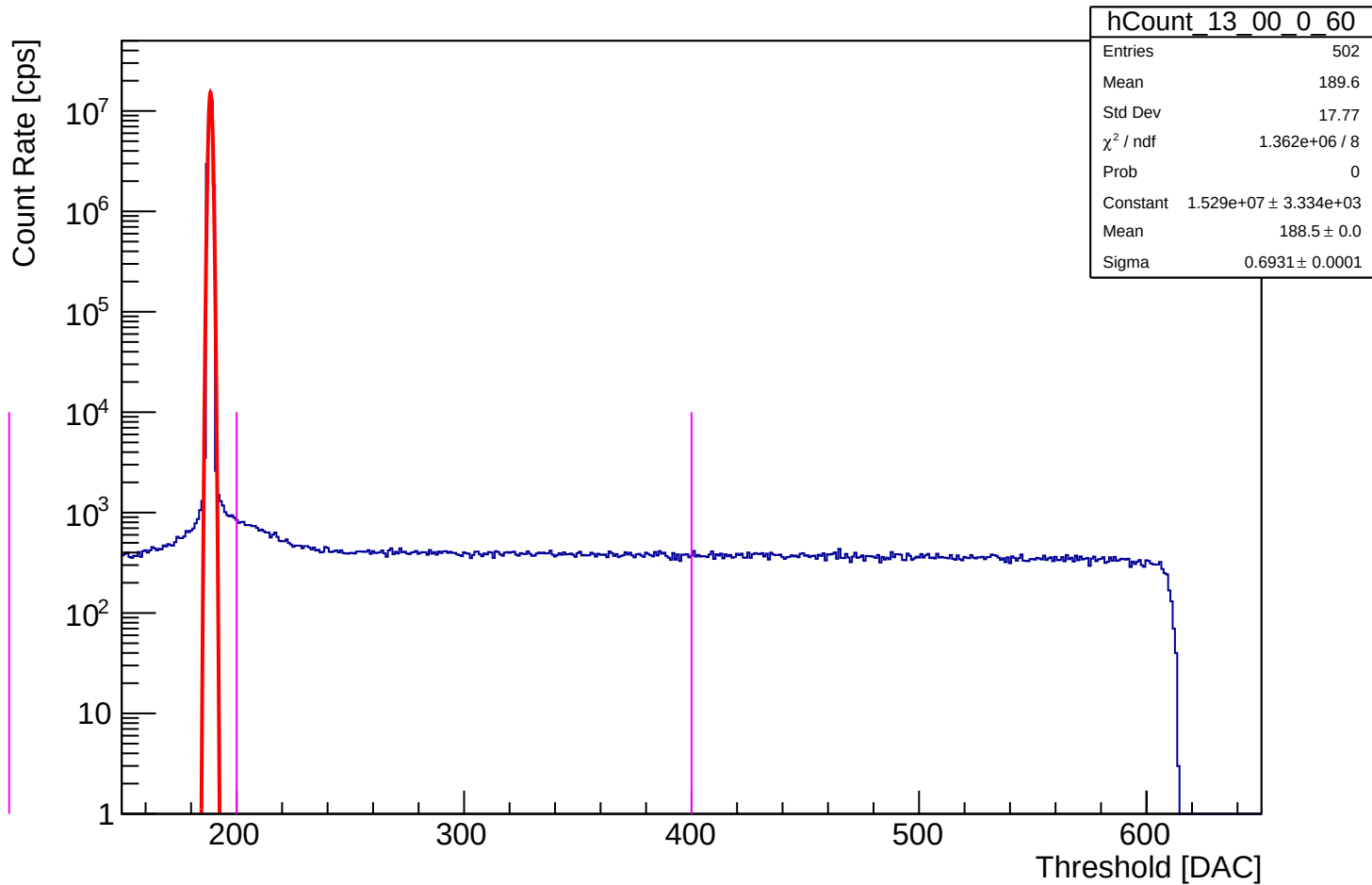
Row 1 Tile 1 Pmt 1 Pixel 58 Slot 13 Fiber 0 Asic 0 Channel 1



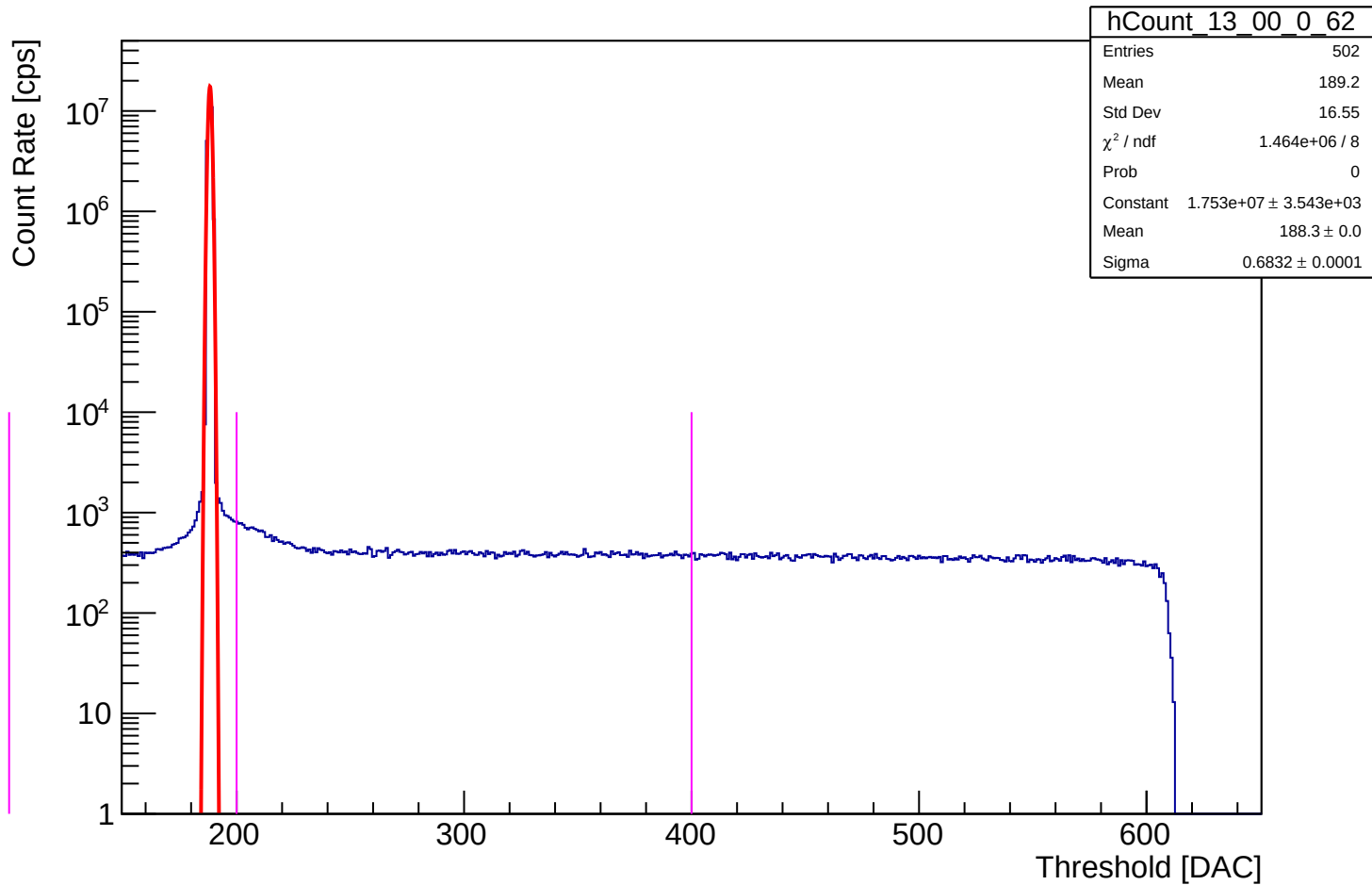




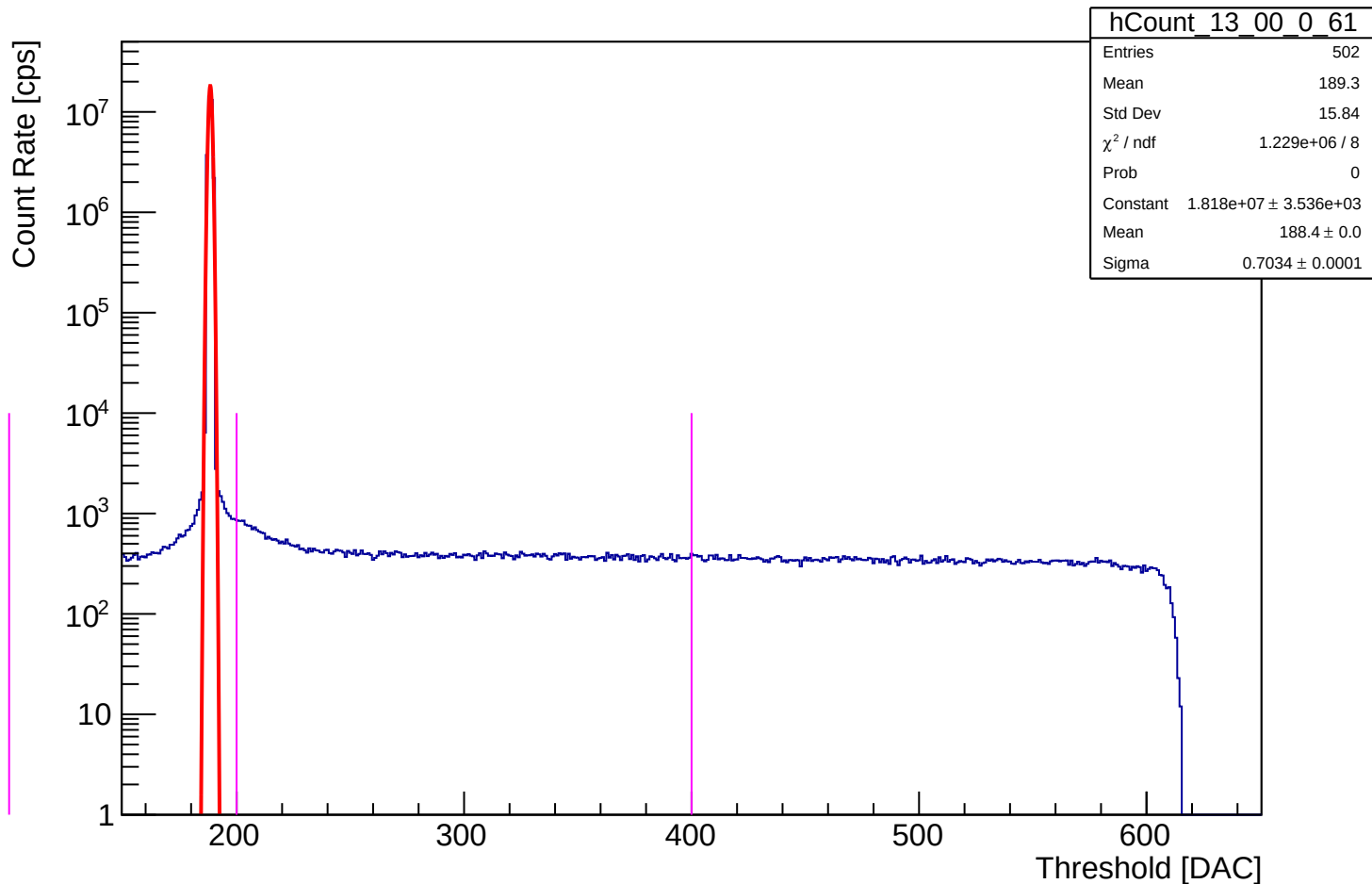
Row 1 Tile 1 Pmt 1 Pixel 61 Slot 13 Fiber 0 Asic 0 Channel 60



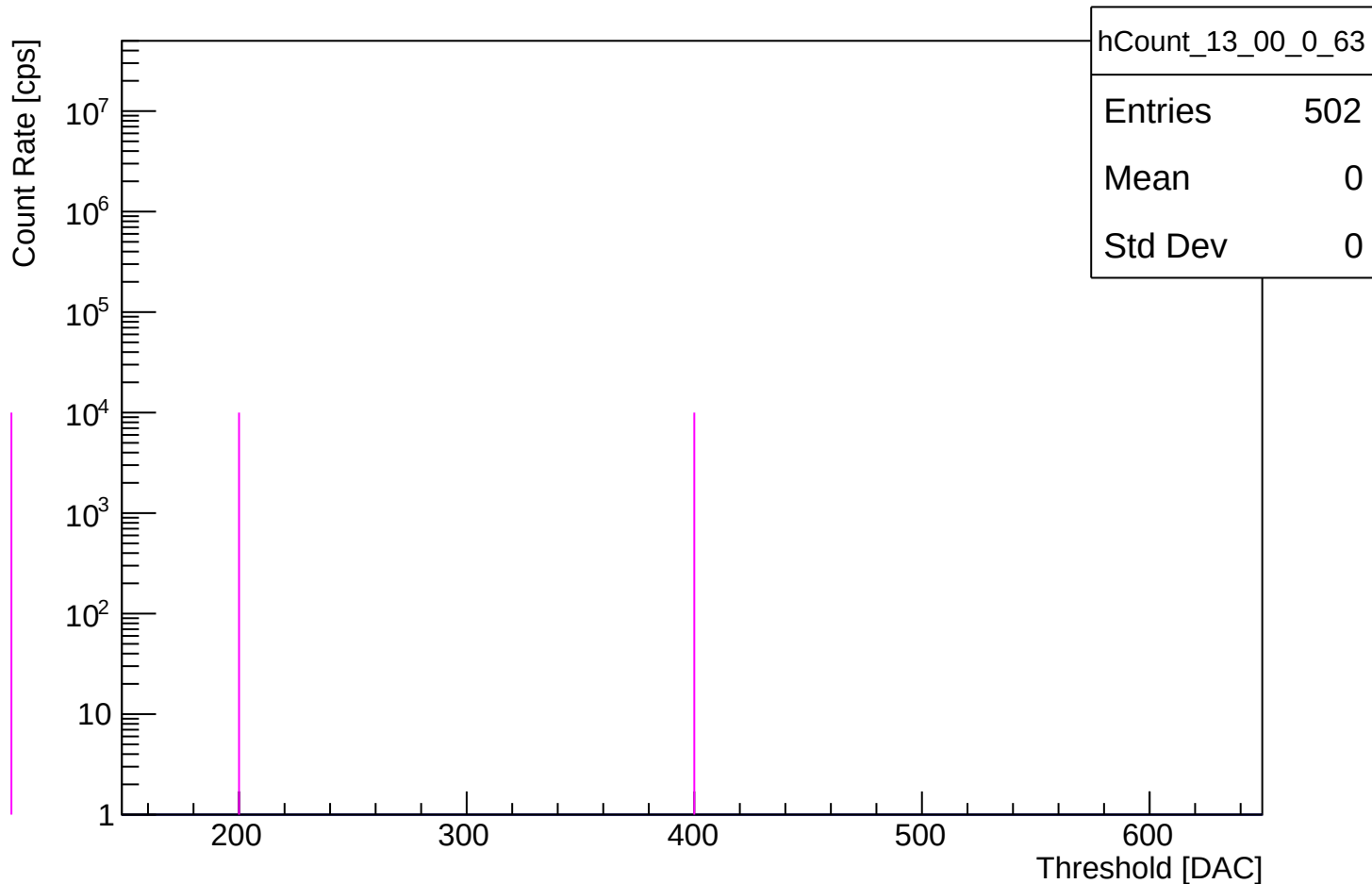
Row 1 Tile 1 Pmt 1 Pixel 62 Slot 13 Fiber 0 Asic 0 Channel 62



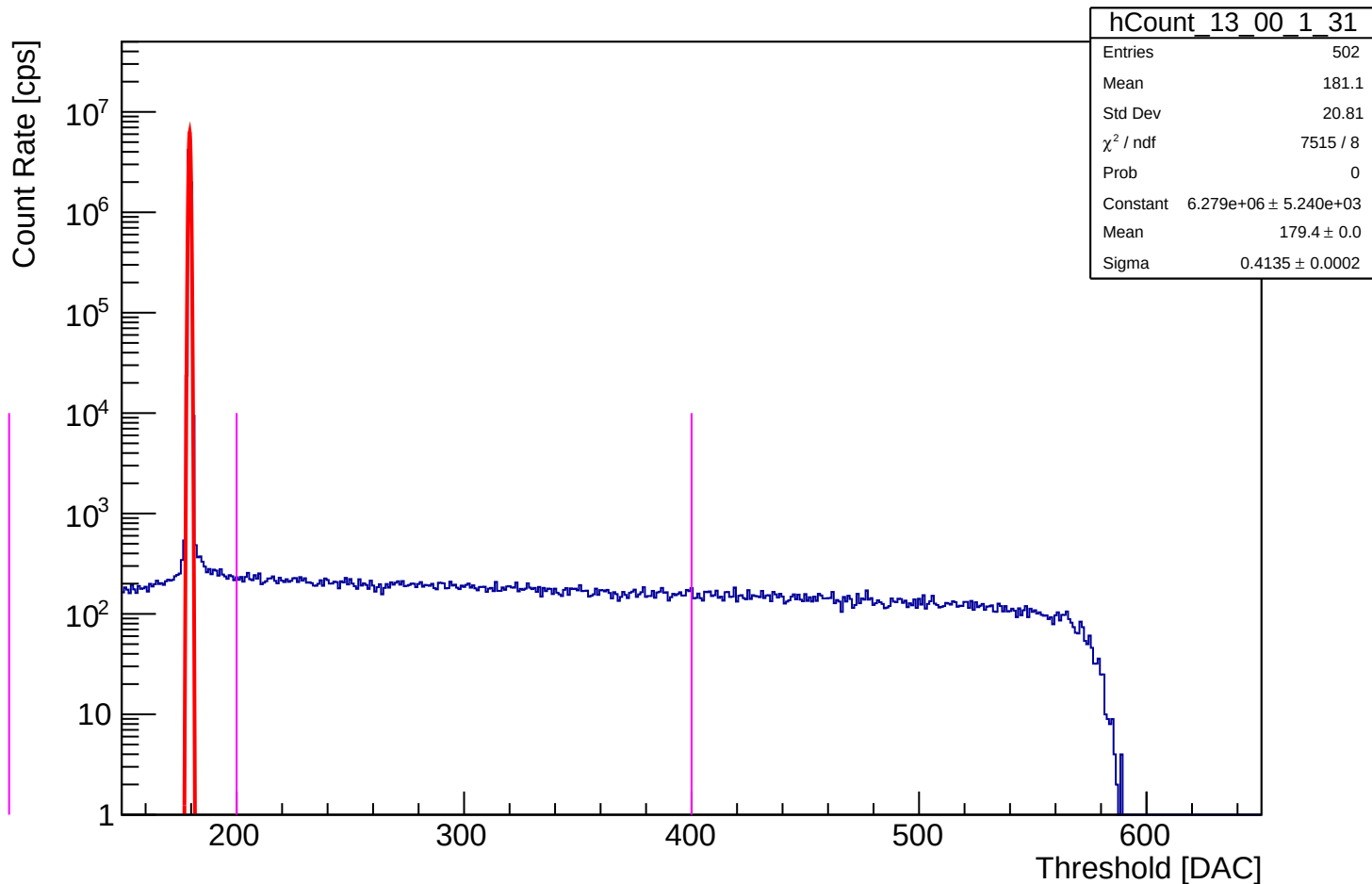
Row 1 Tile 1 Pmt 1 Pixel 63 Slot 13 Fiber 0 Asic 0 Channel 61



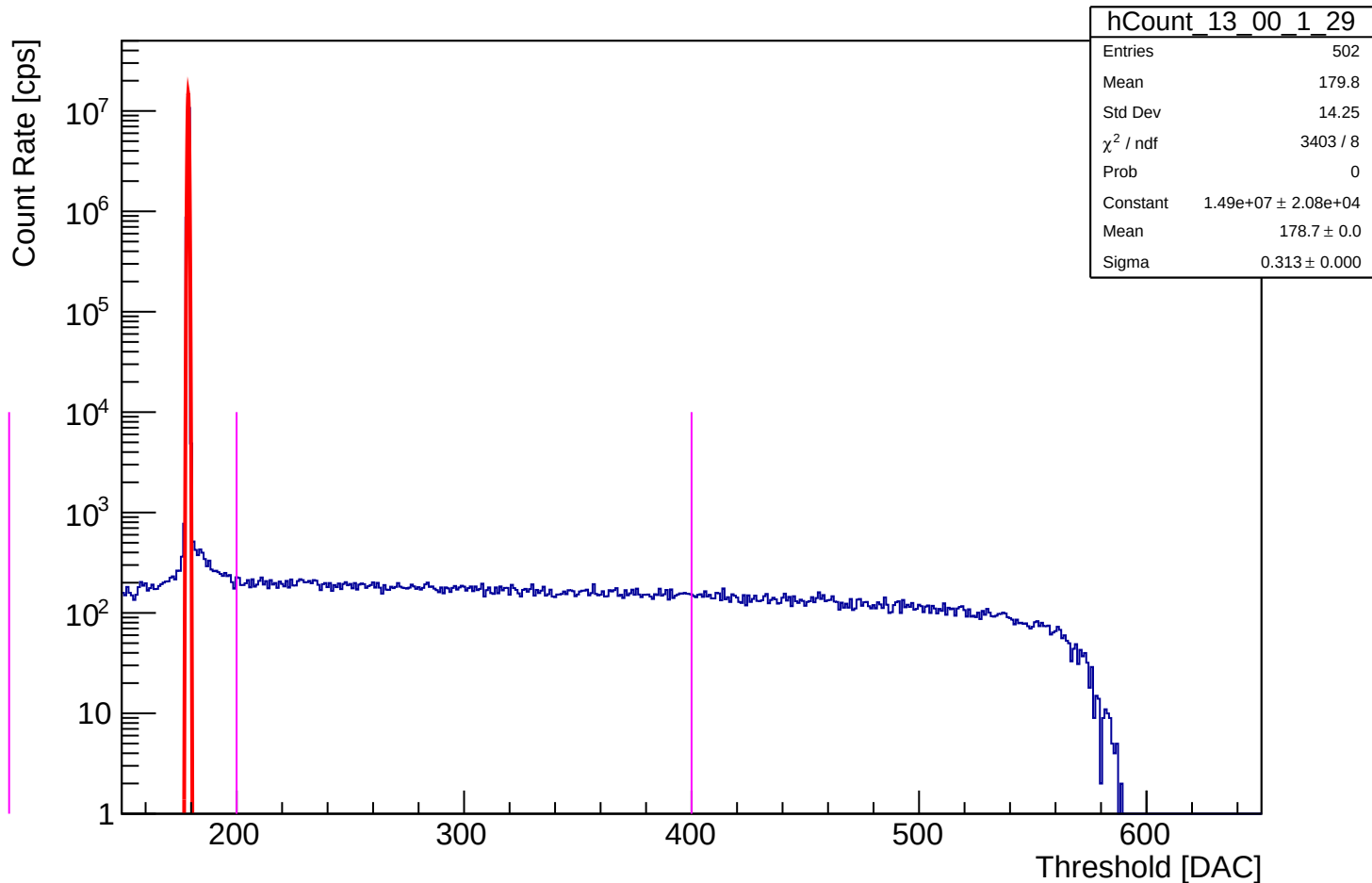
Row 1 Tile 1 Pmt 1 Pixel 64 Slot 13 Fiber 0 Asic 0 Channel 63



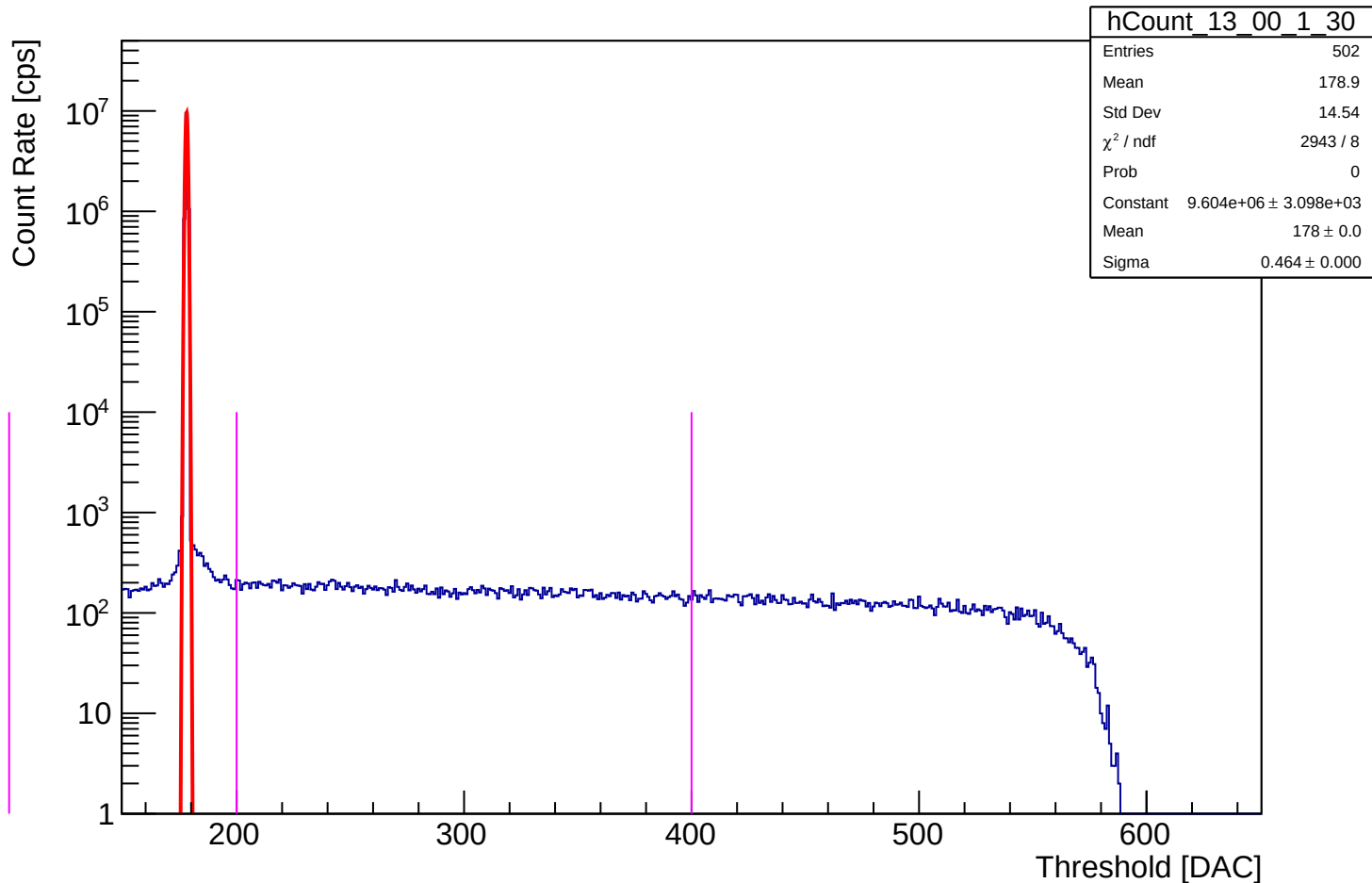
Row 1 Tile 1 Pmt 2 Pixel 1 Slot 13 Fiber 0 Asic 1 Channel 31



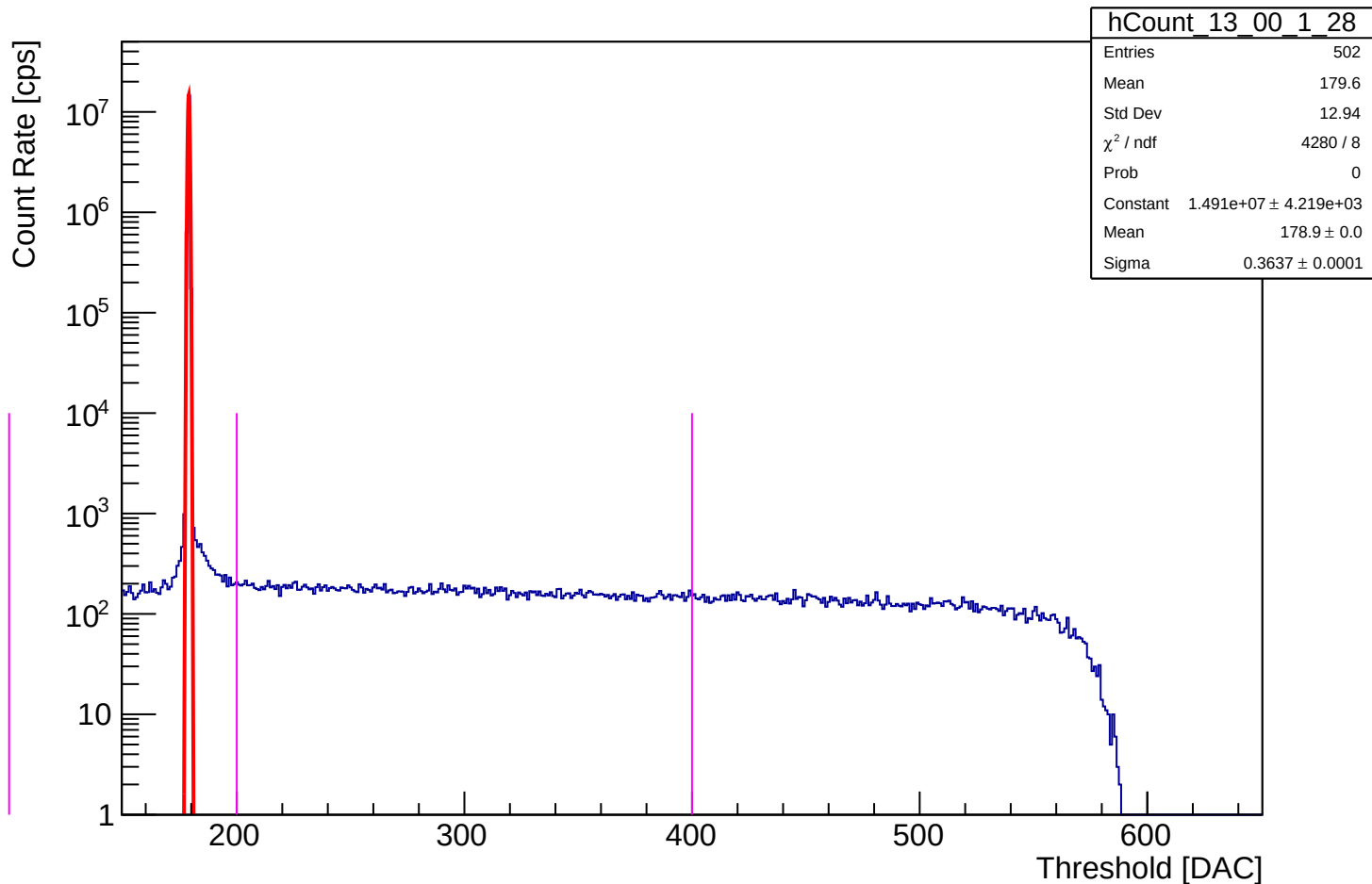
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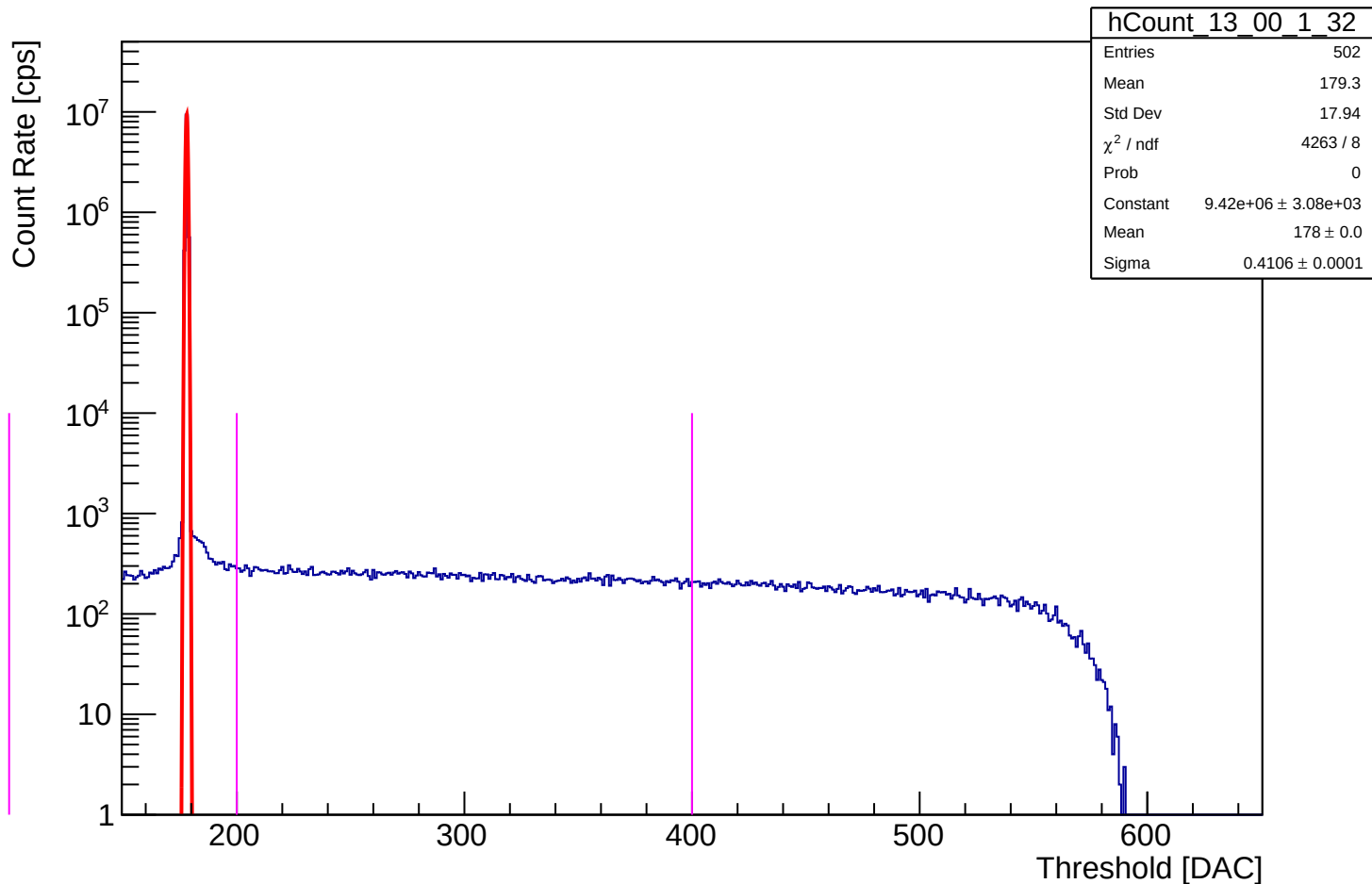
Row 1 Tile 1 Pmt 2 Pixel 3 Slot 13 Fiber 0 Asic 1 Channel 30



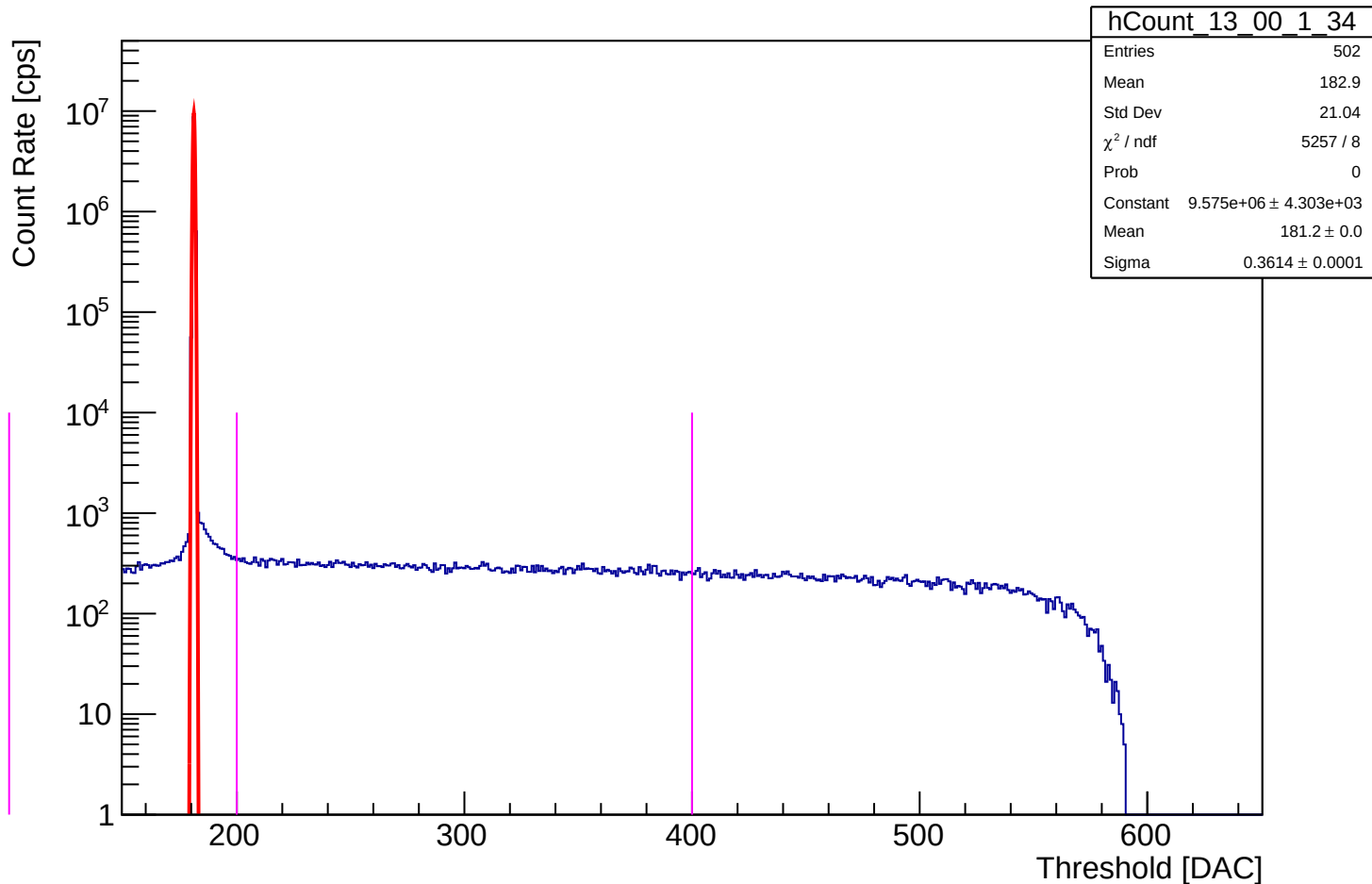
Row 1 Tile 1 Pmt 2 Pixel 4 Slot 13 Fiber 0 Asic 1 Channel 28



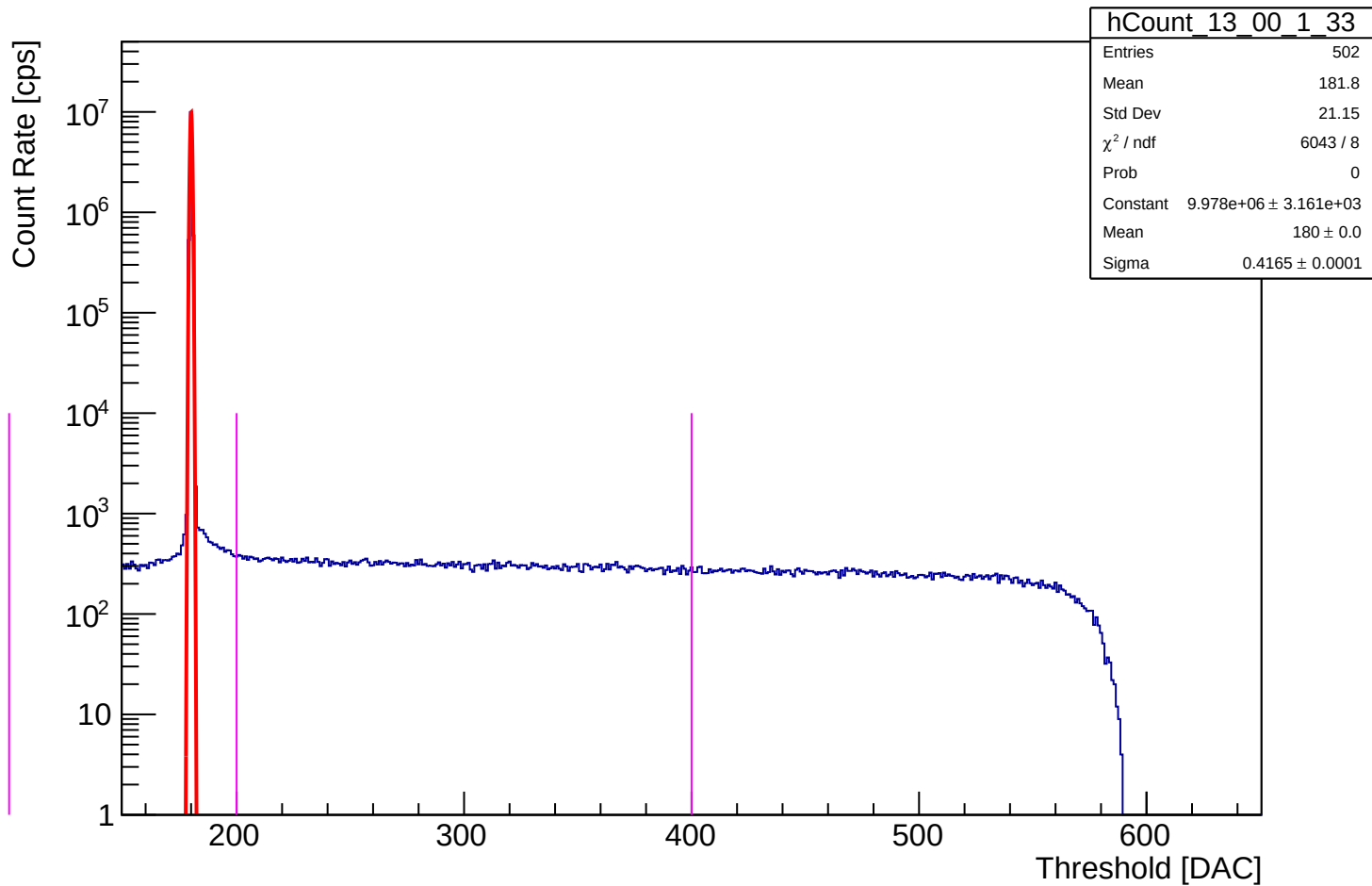
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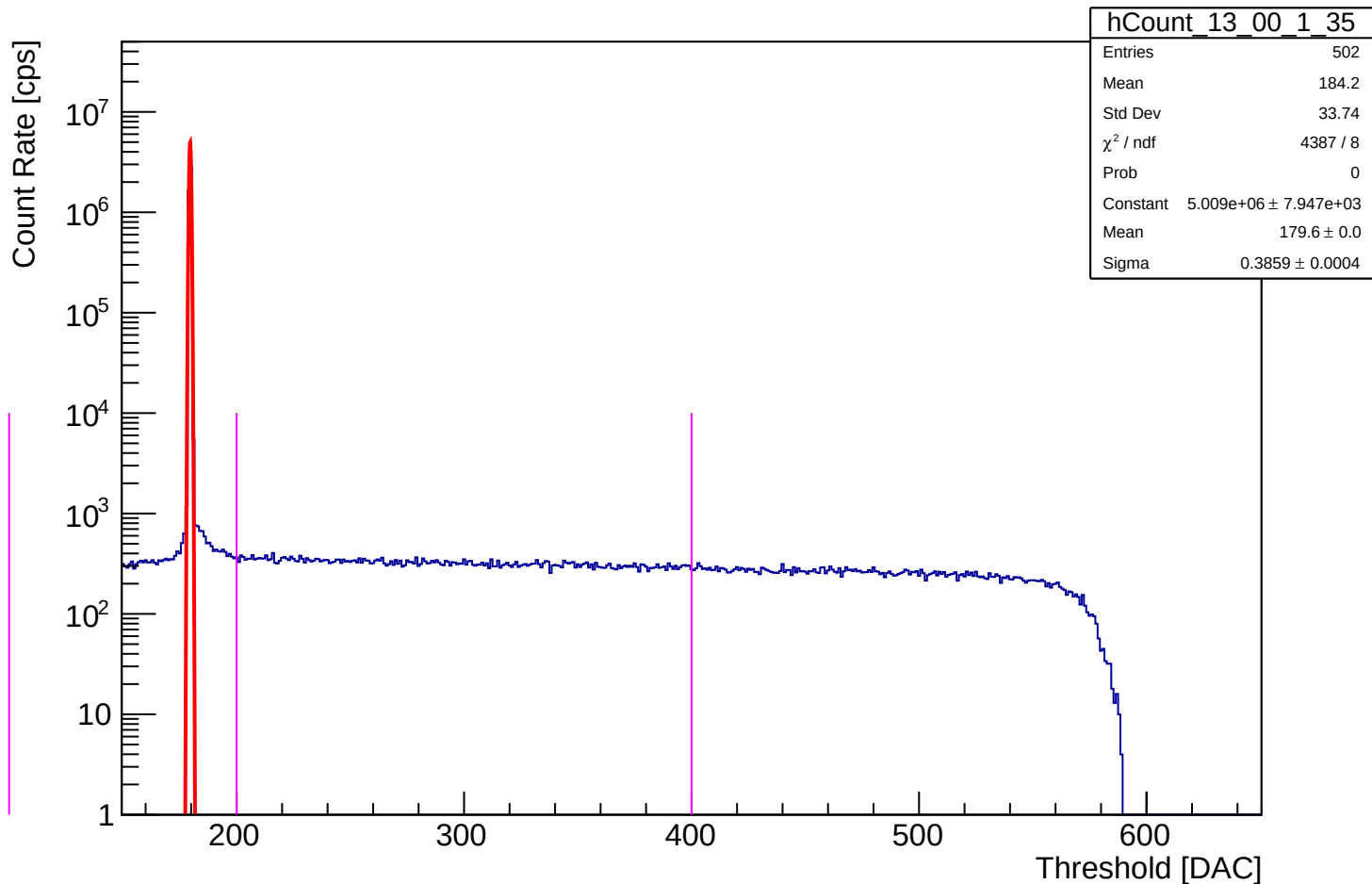
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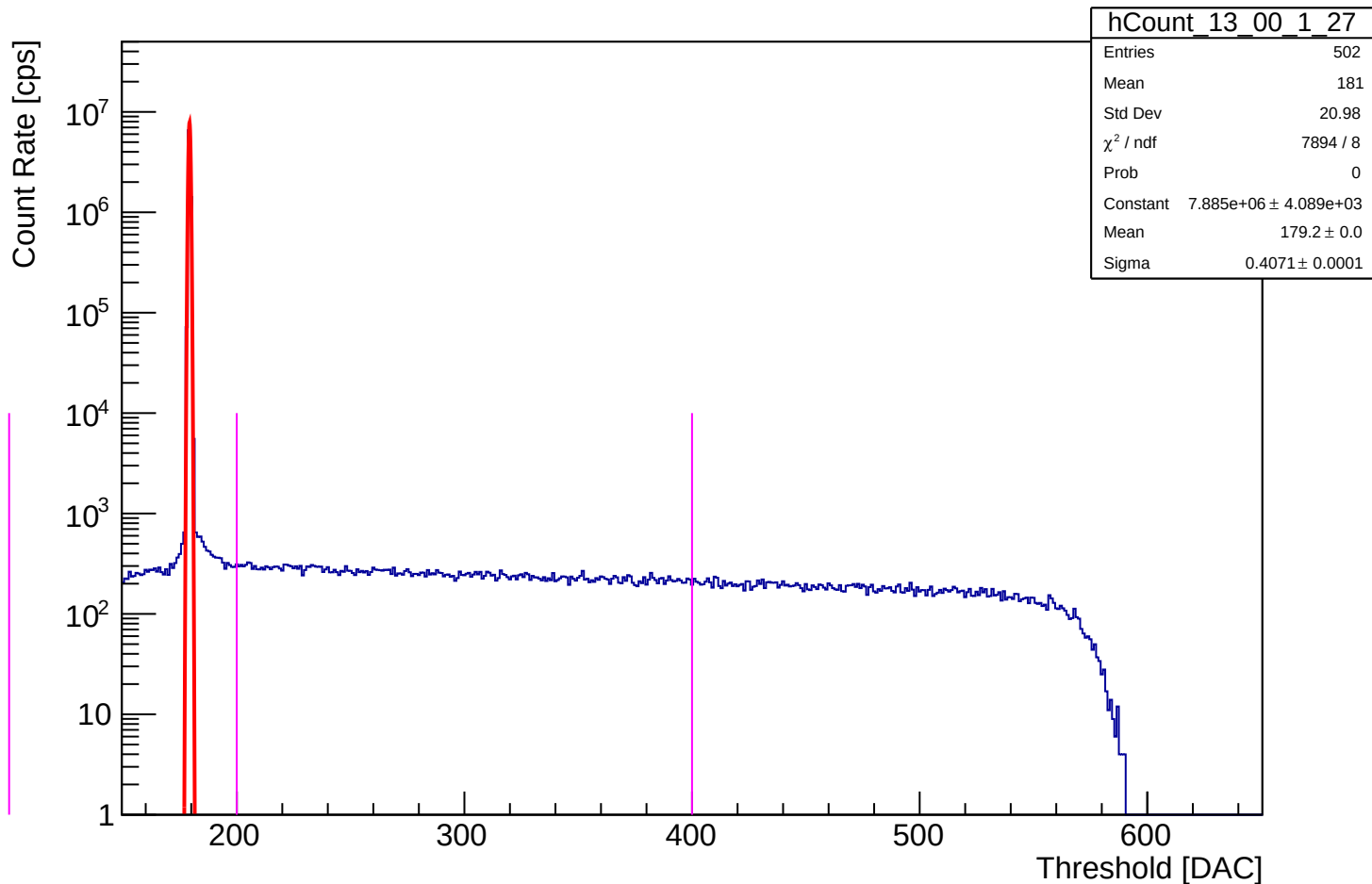
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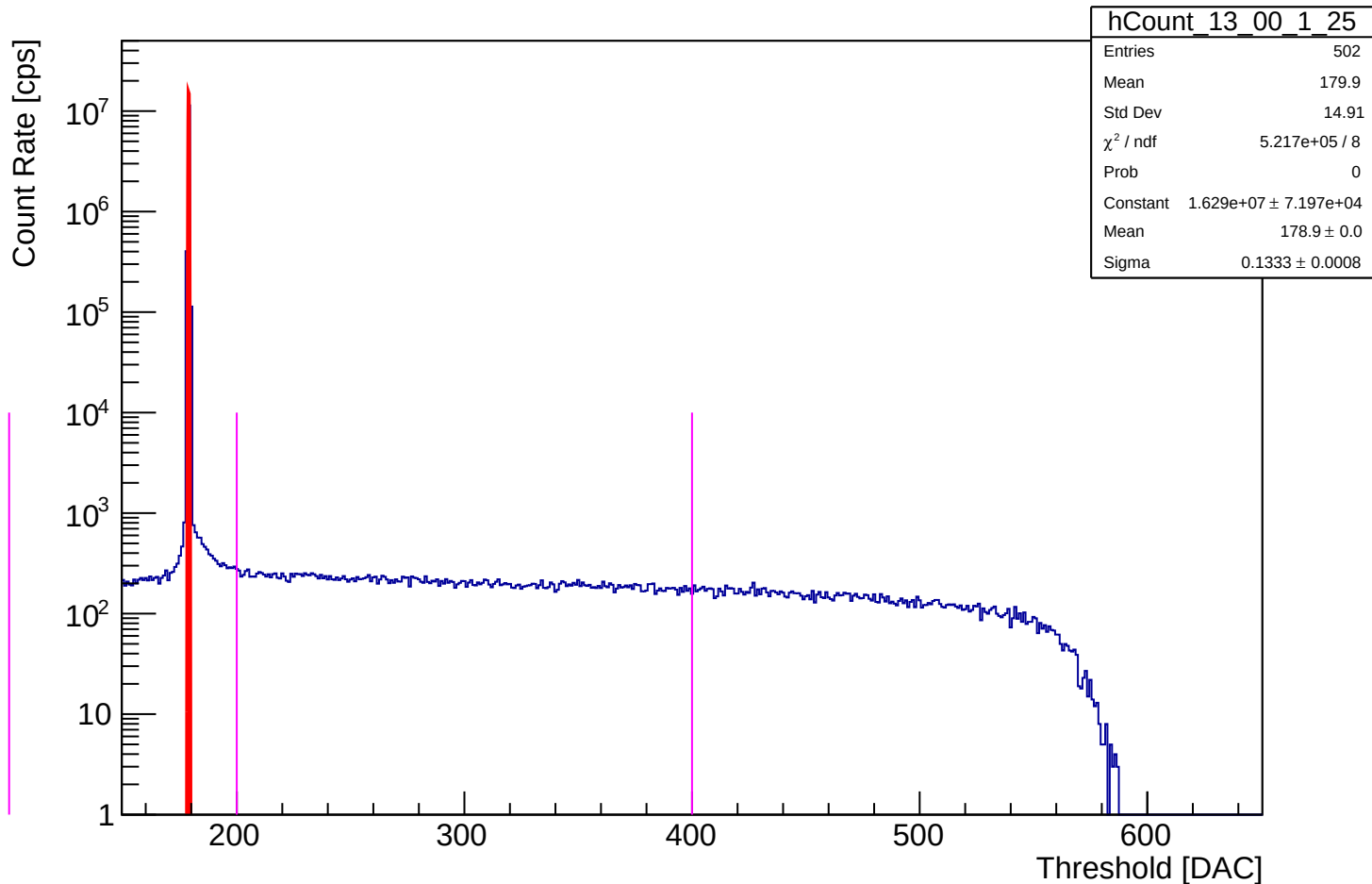
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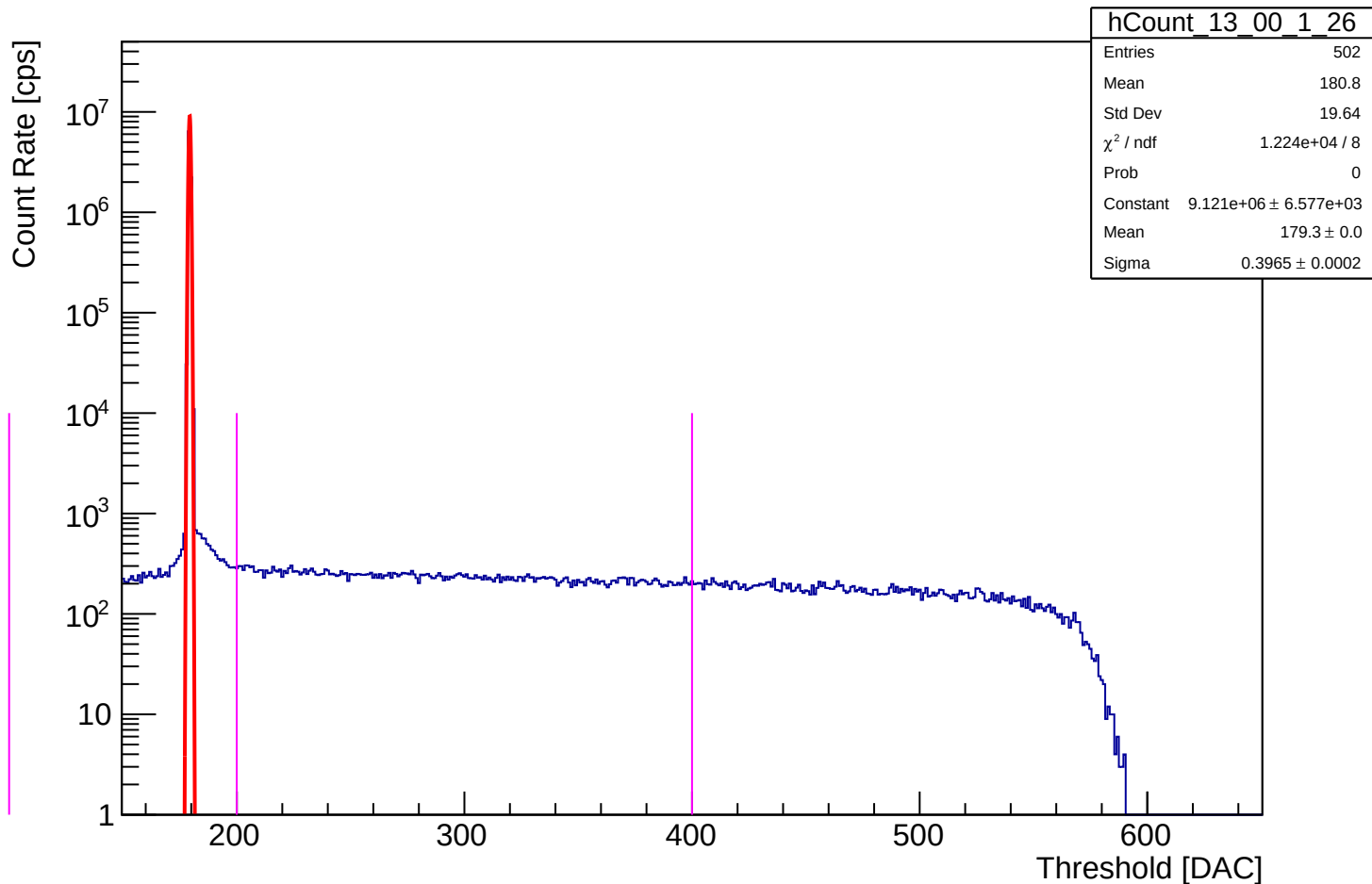
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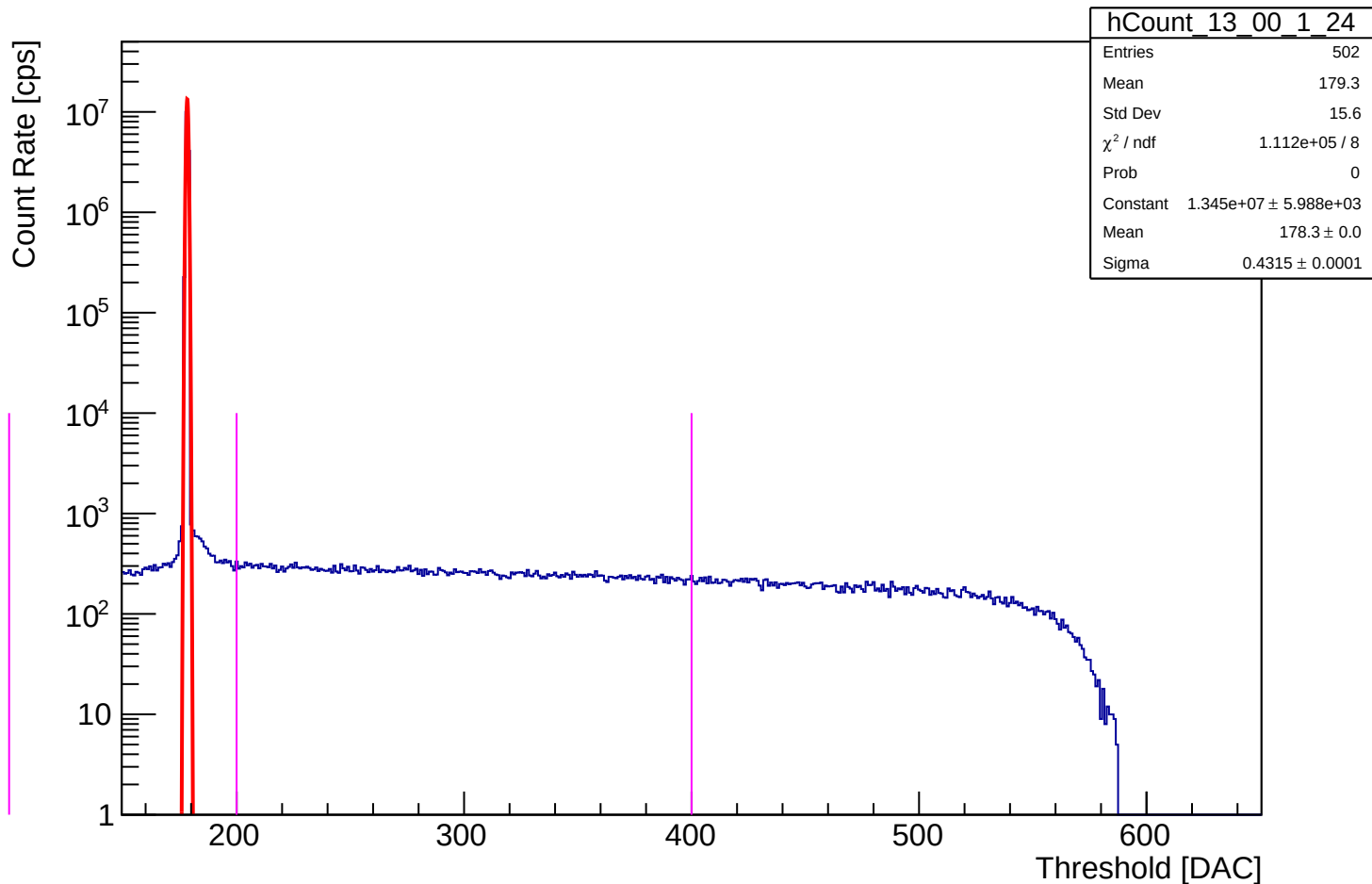
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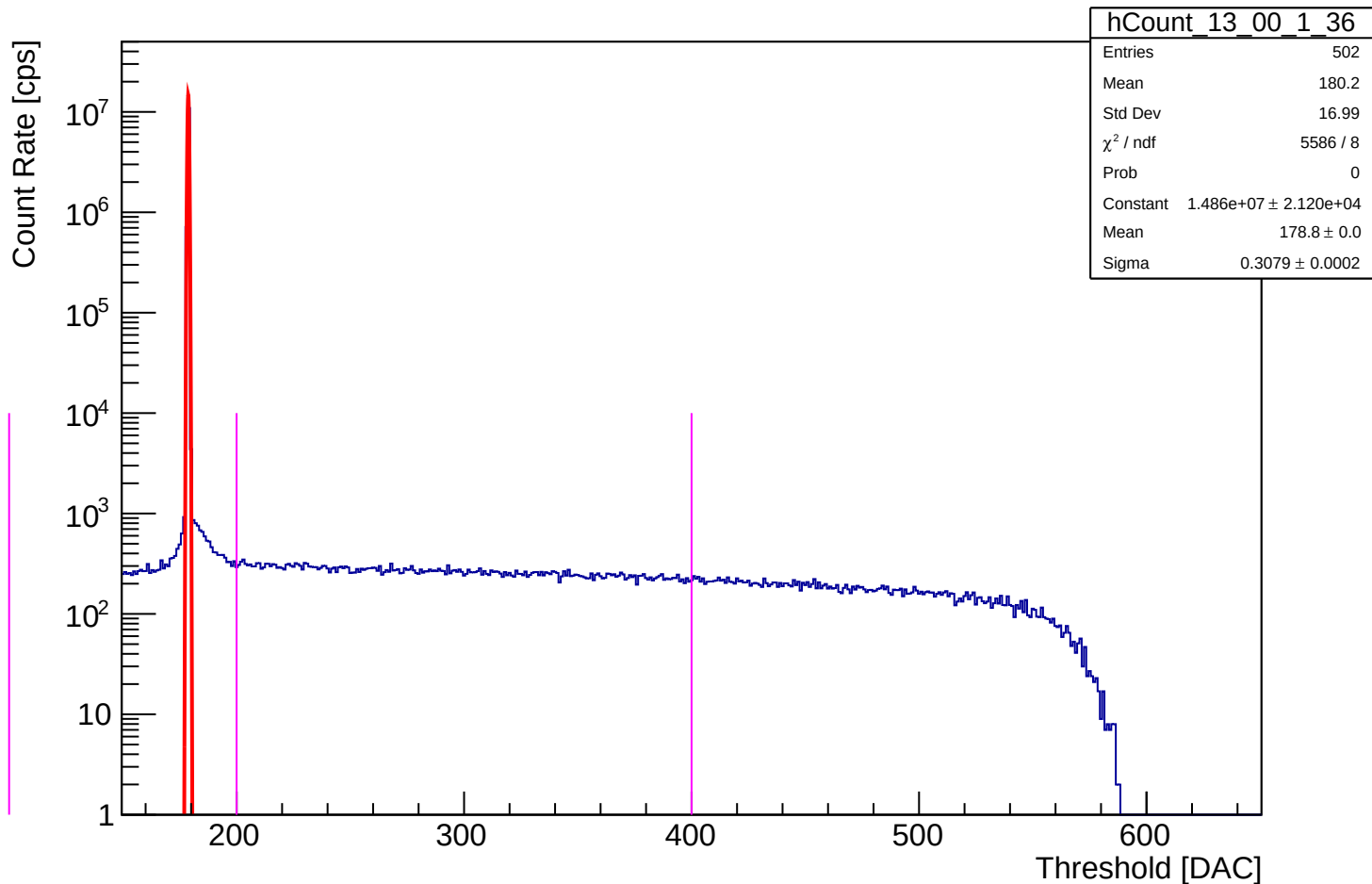
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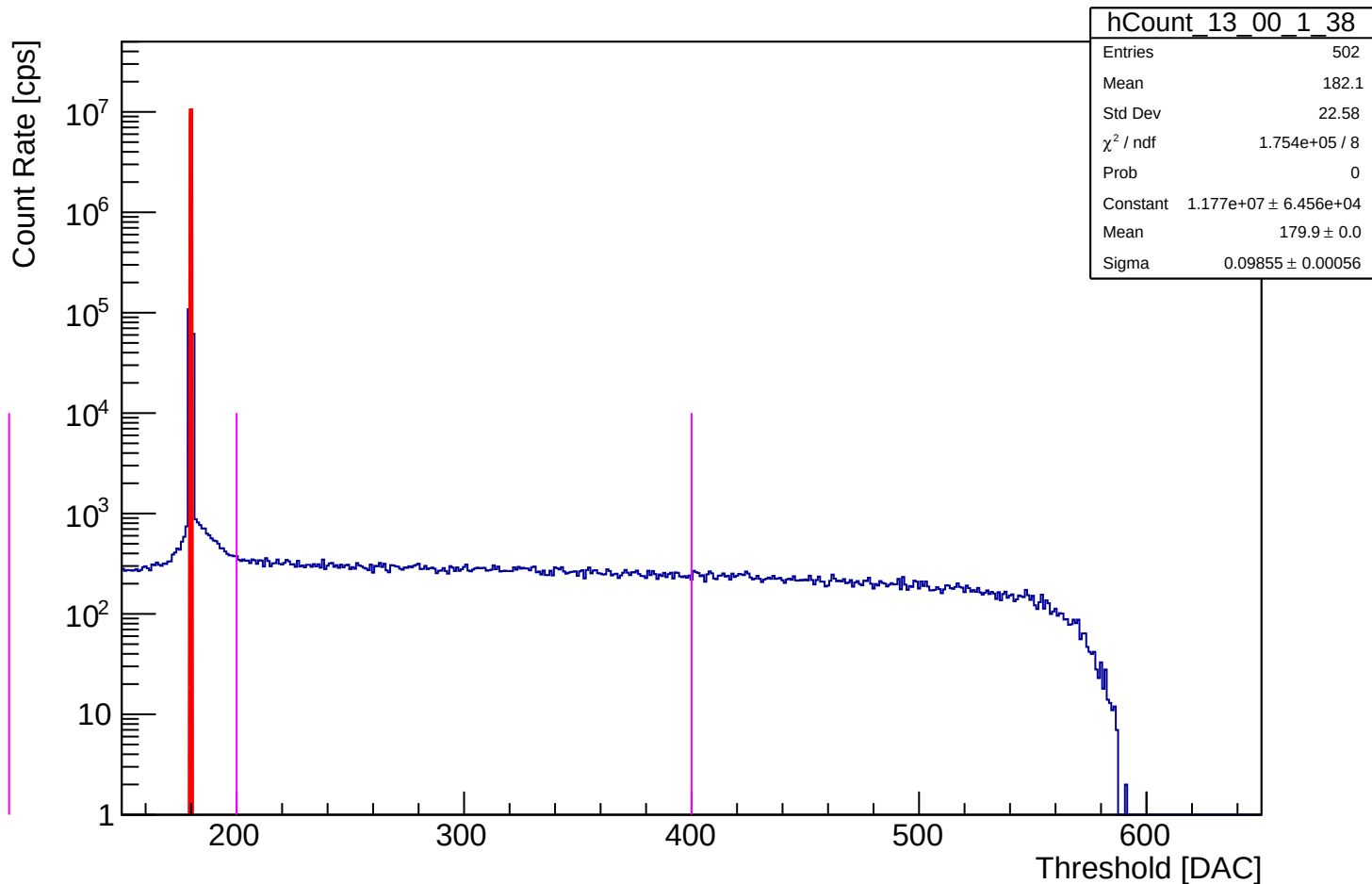
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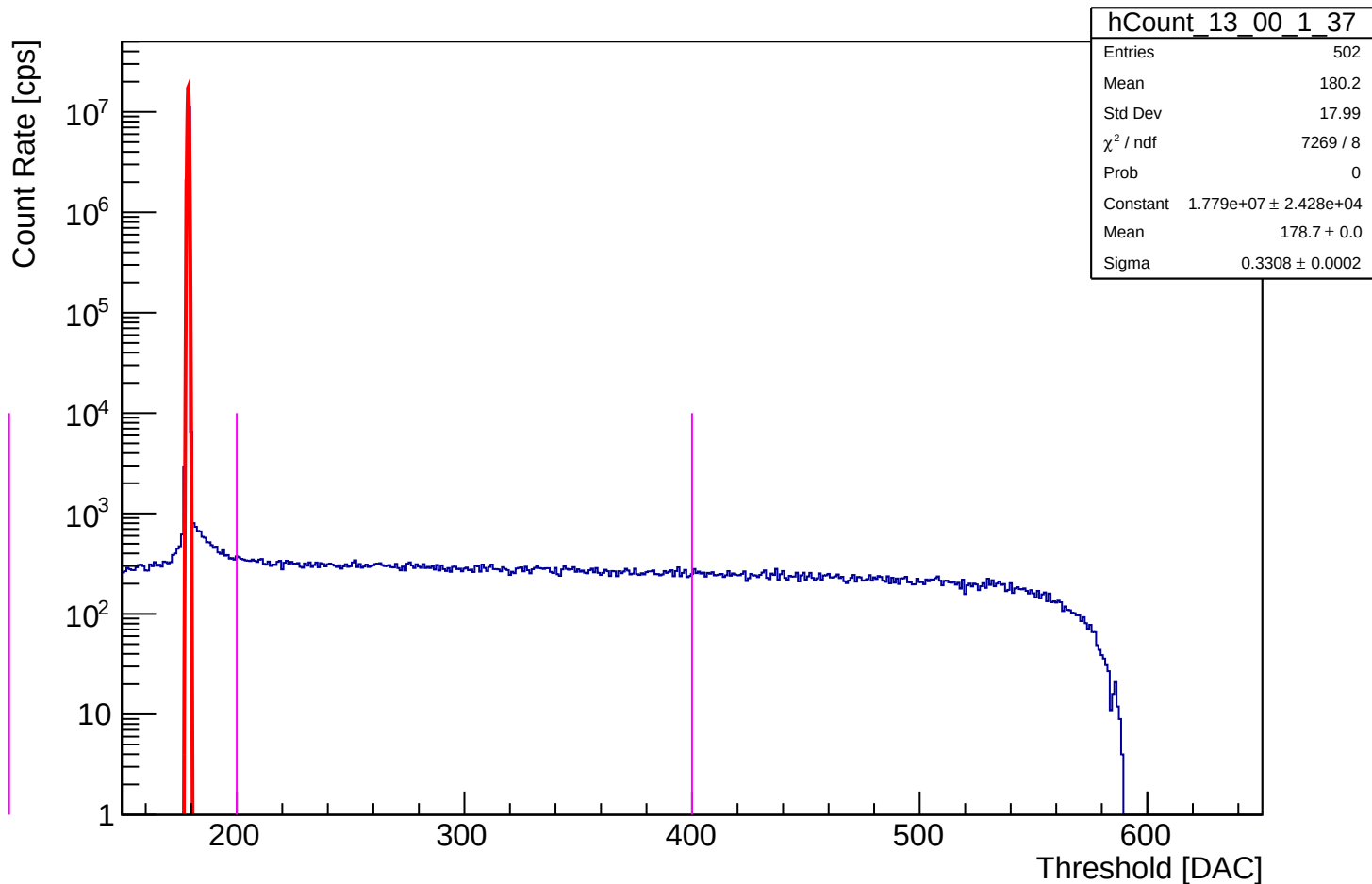
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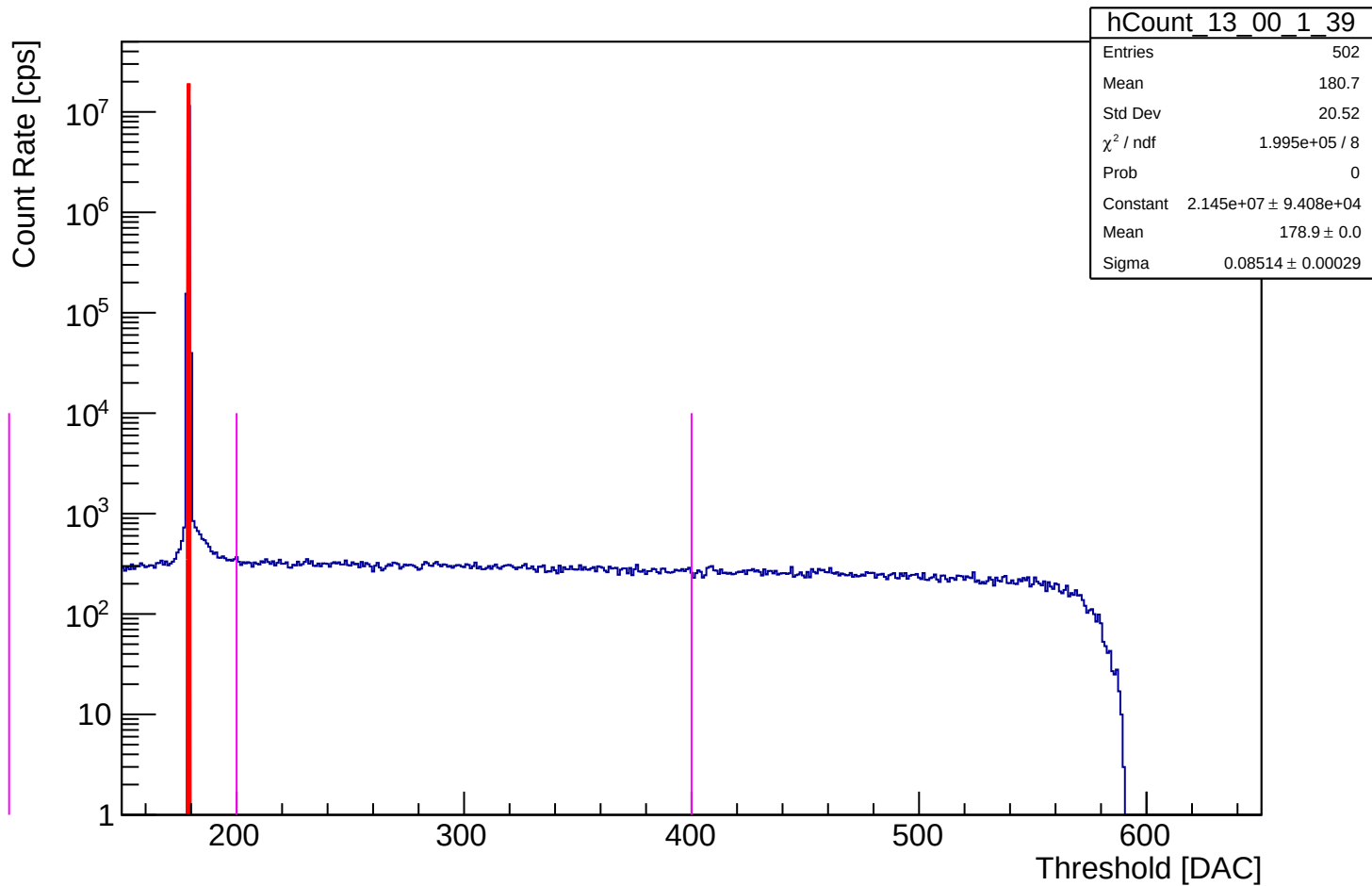
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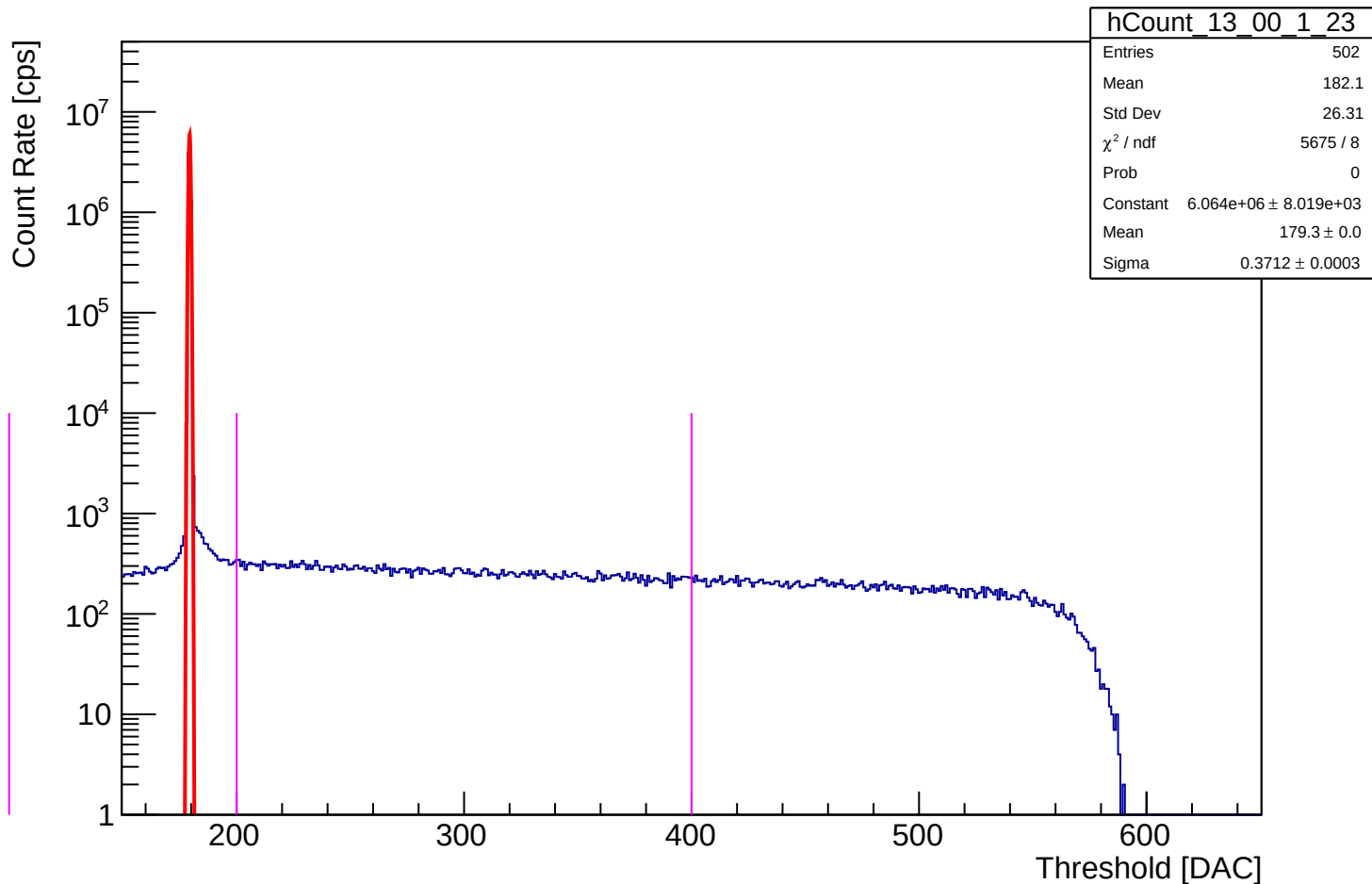
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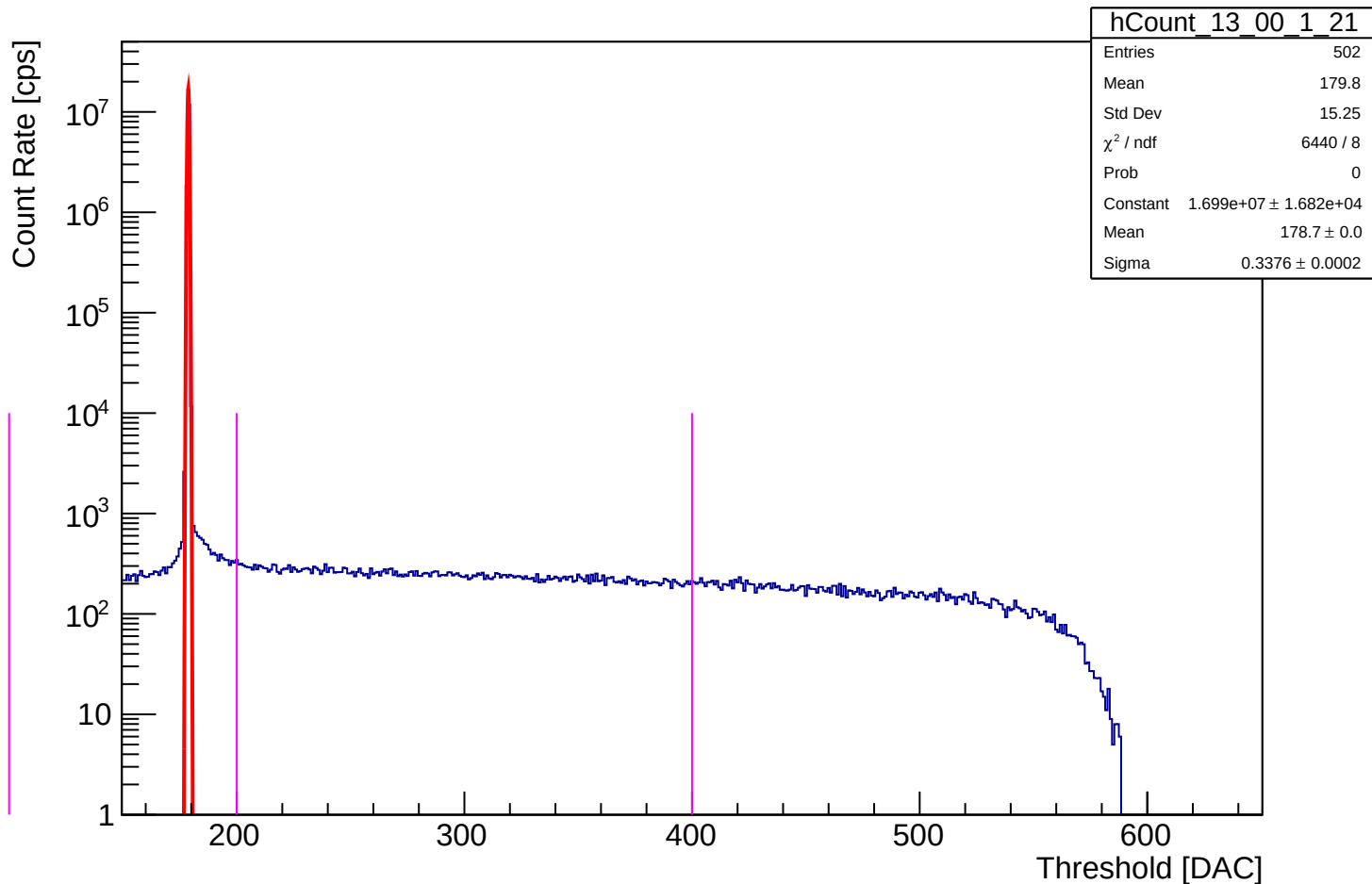
Row 1 Tile 1 Pmt 2 Pixel 16 Slot 13 Fiber 0 Asic 1 Channel 39



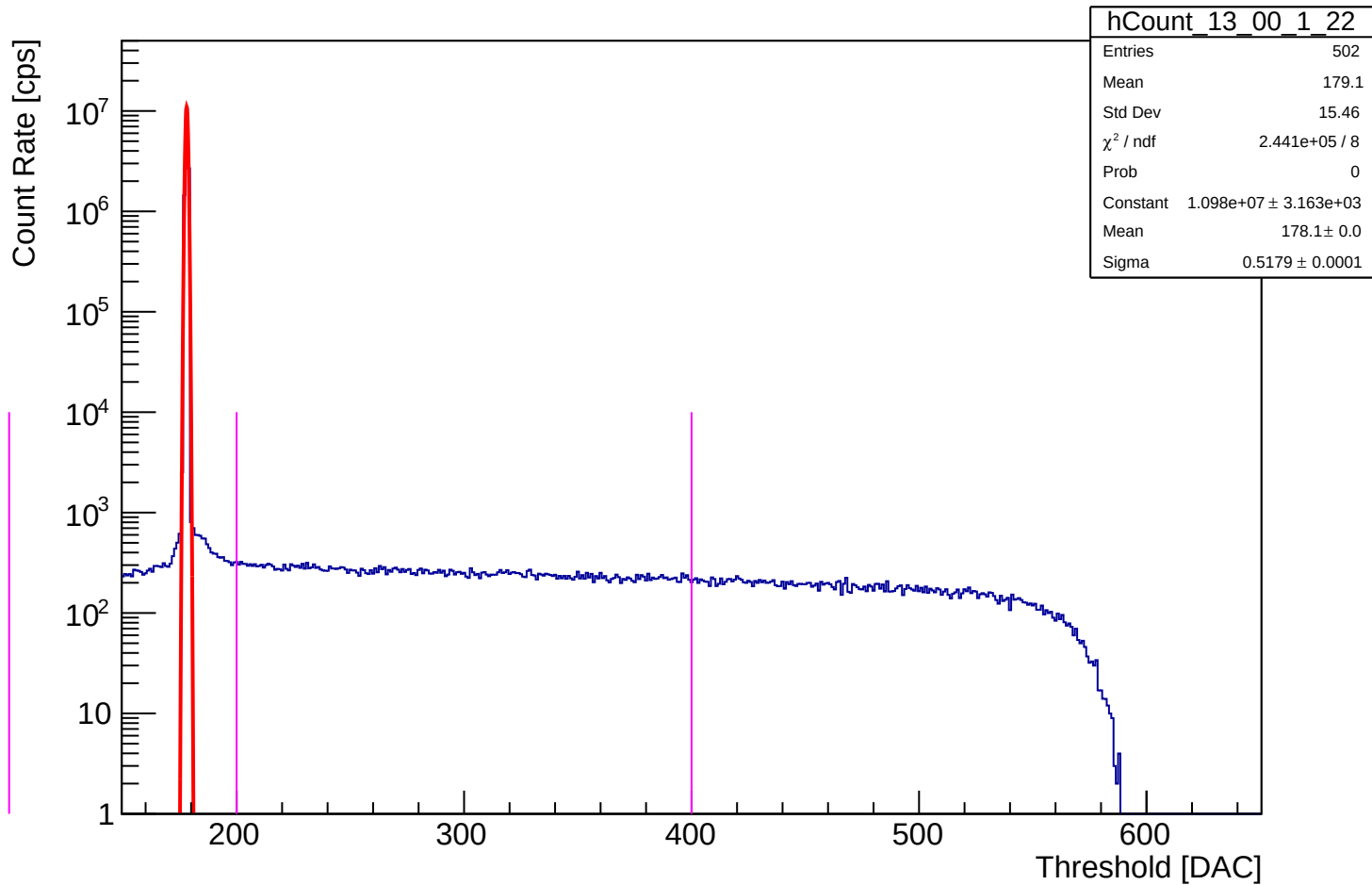
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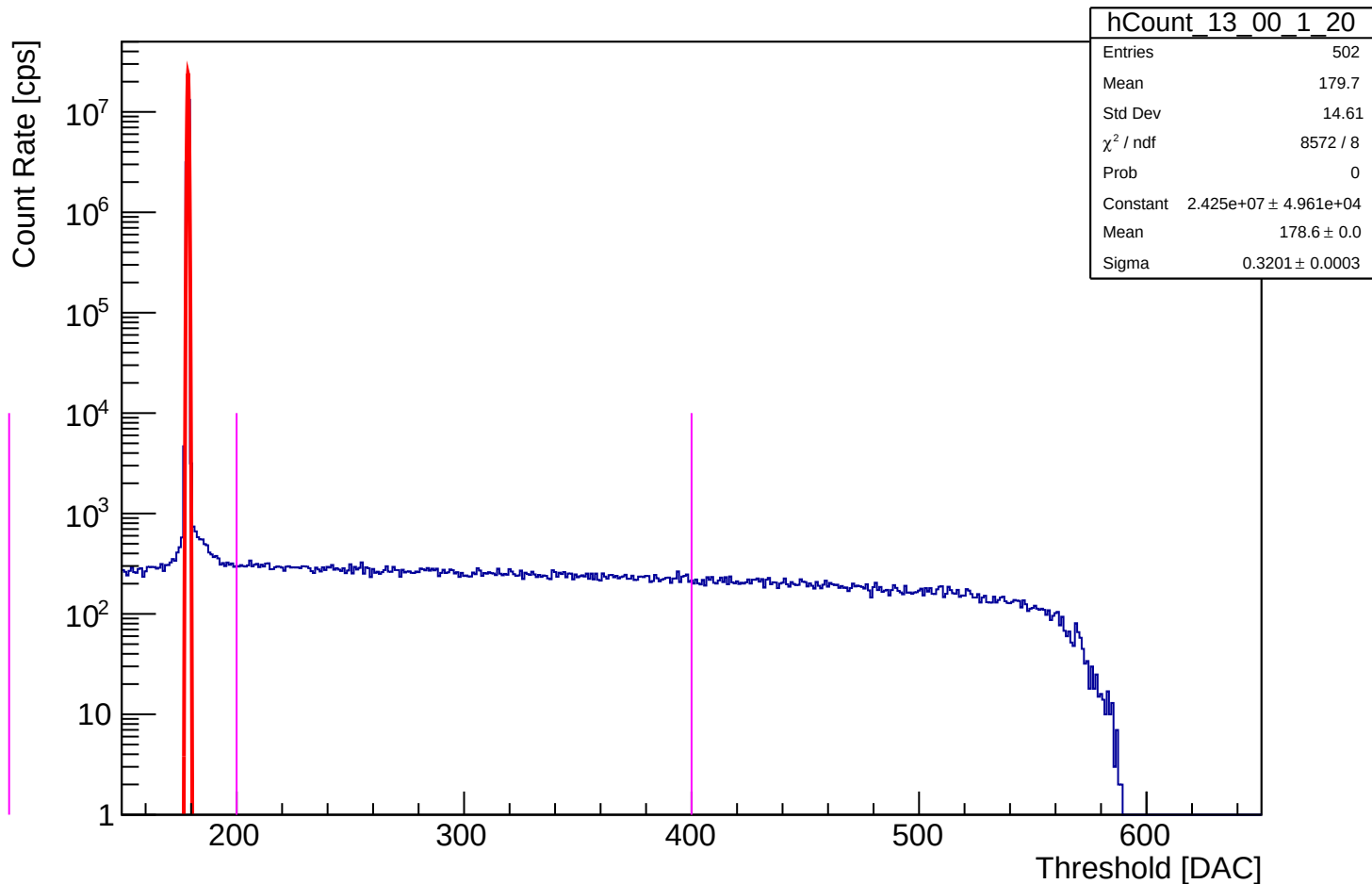
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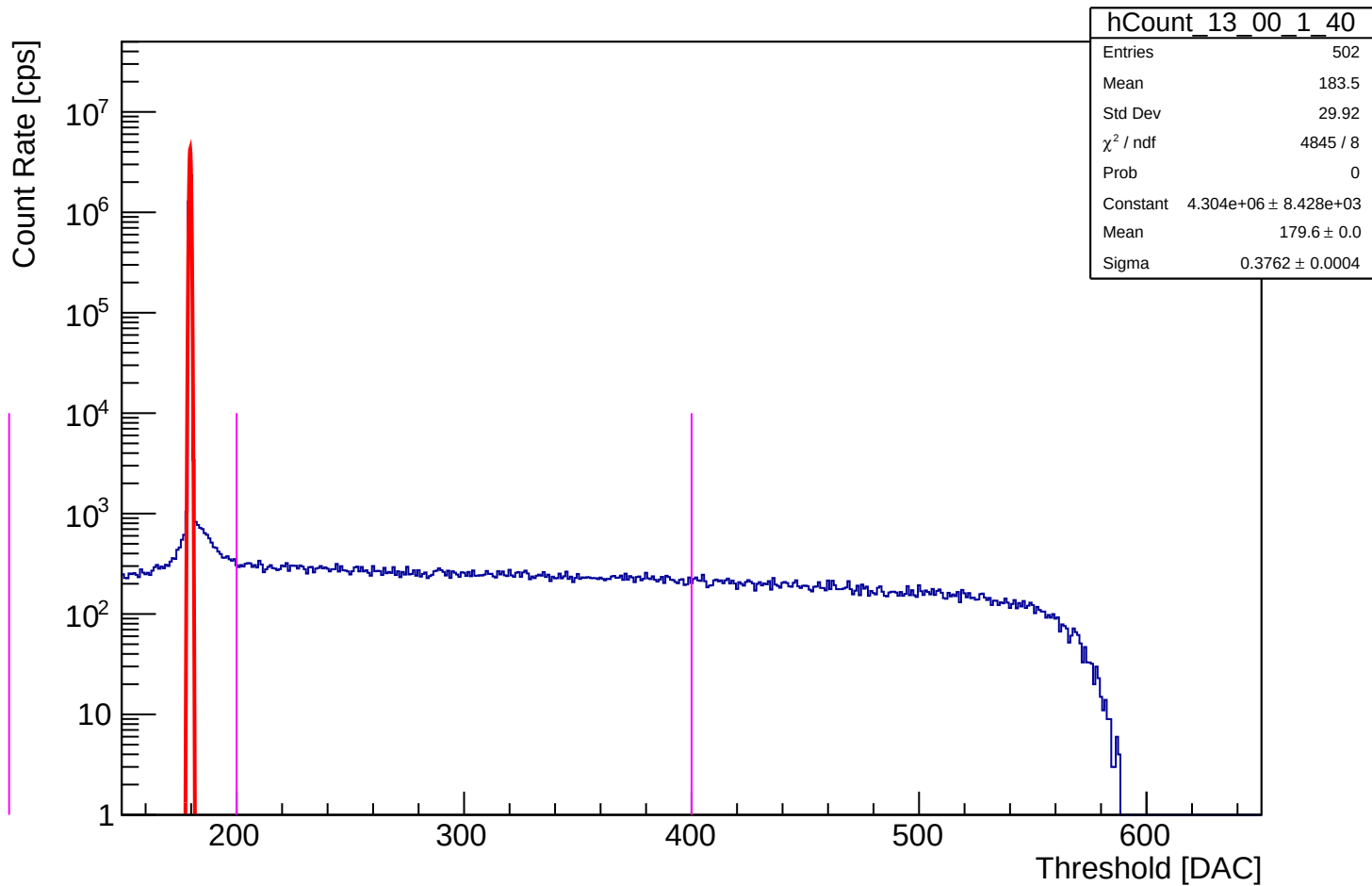
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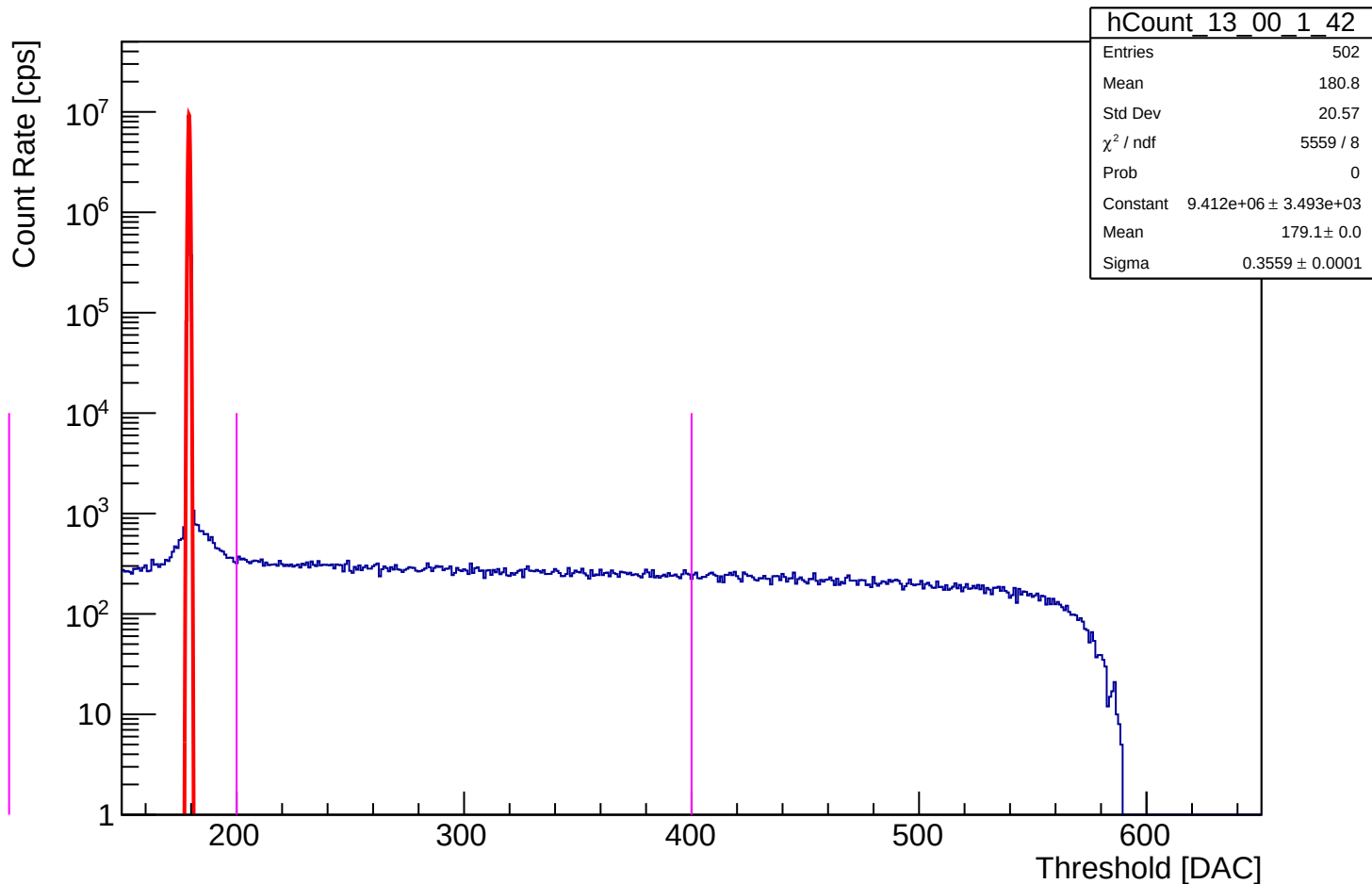
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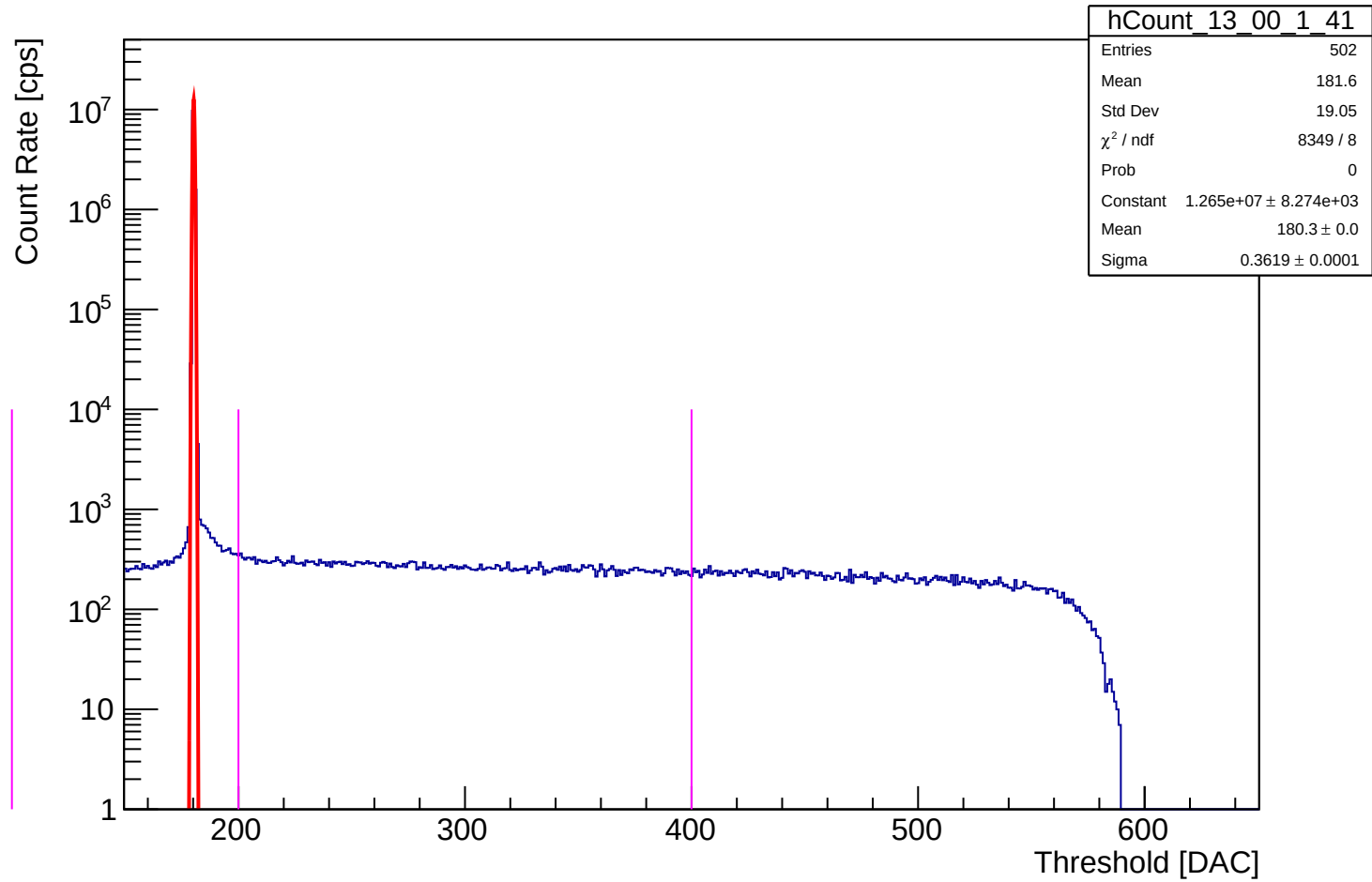


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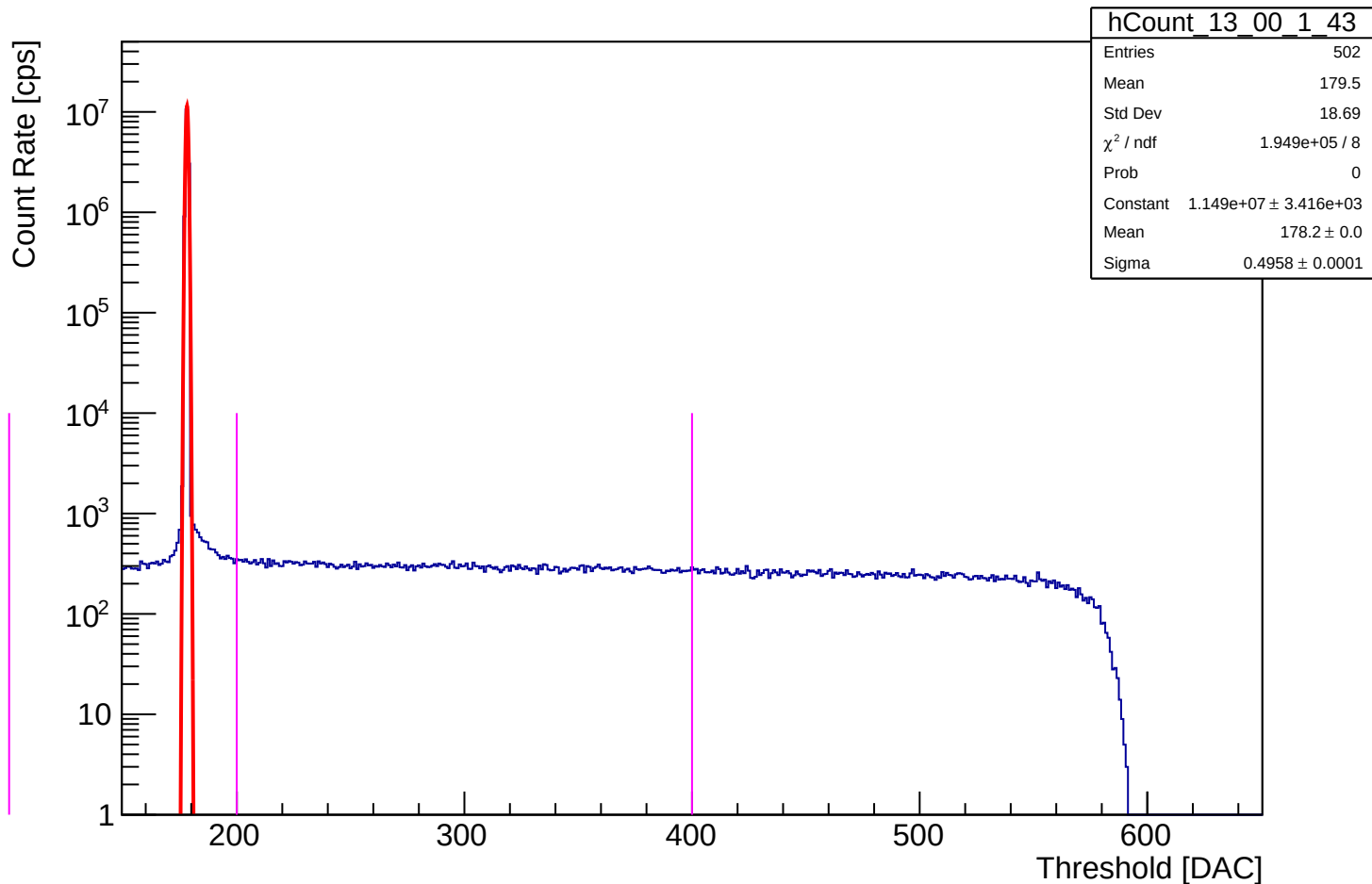


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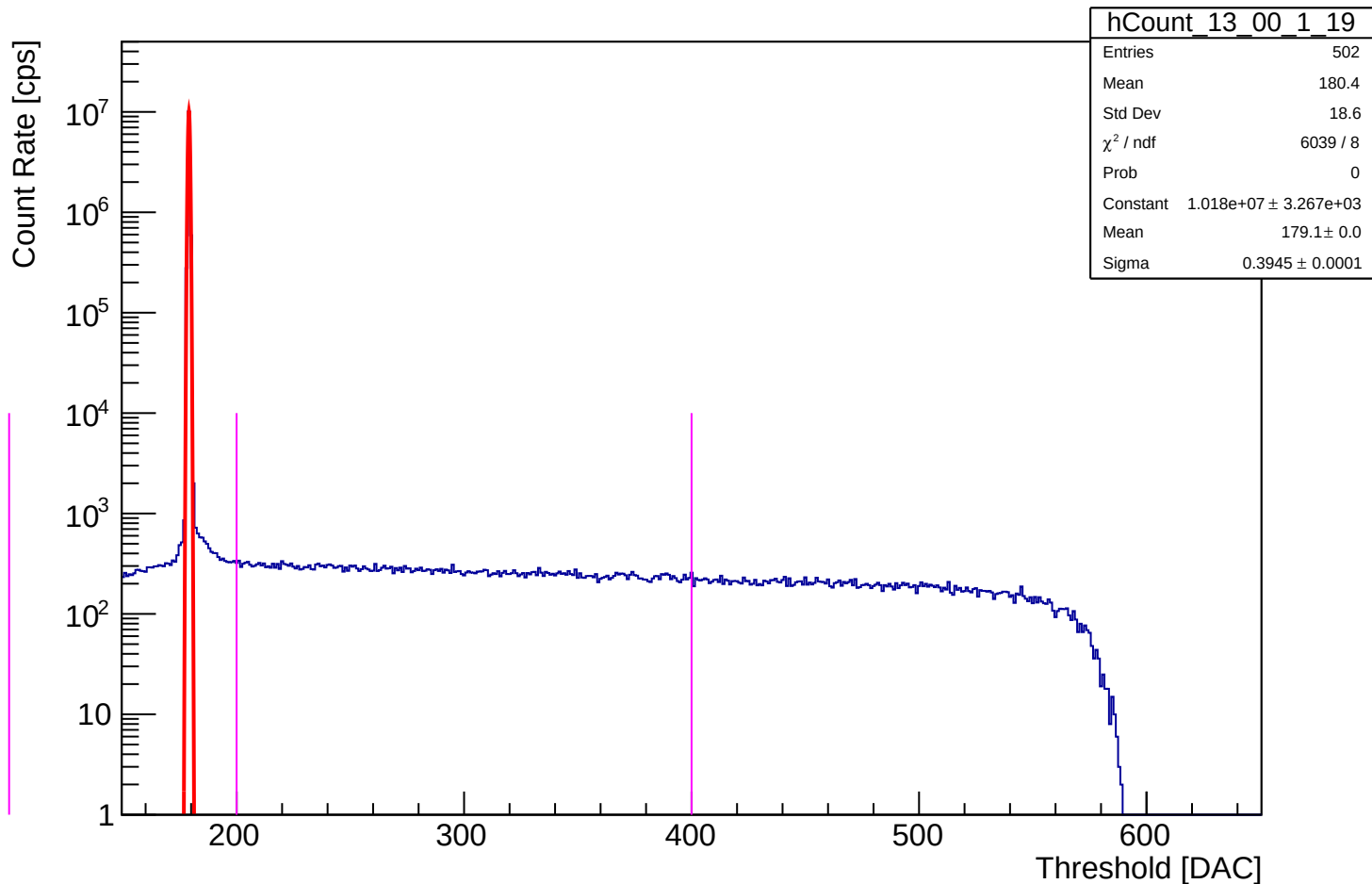




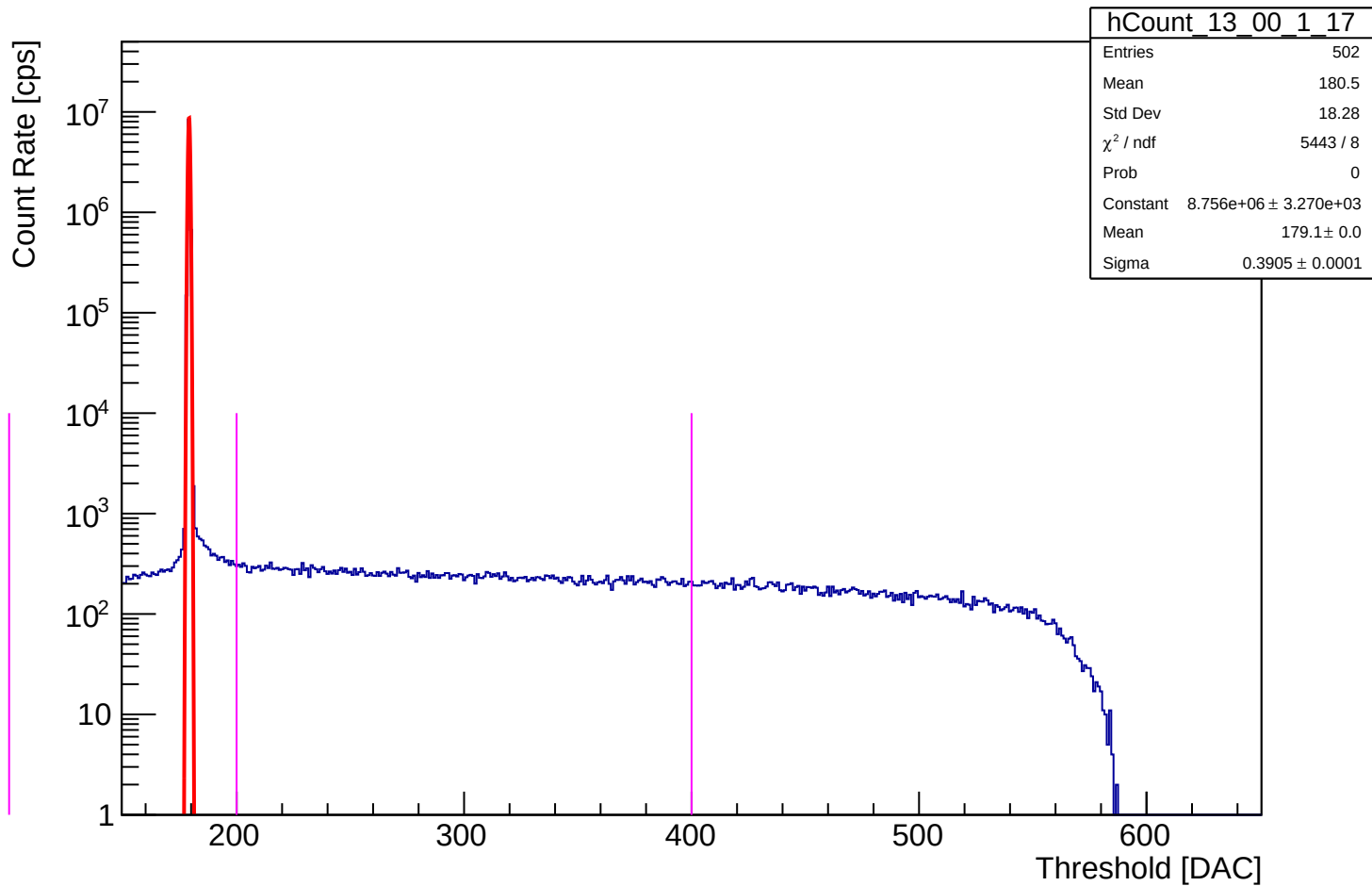
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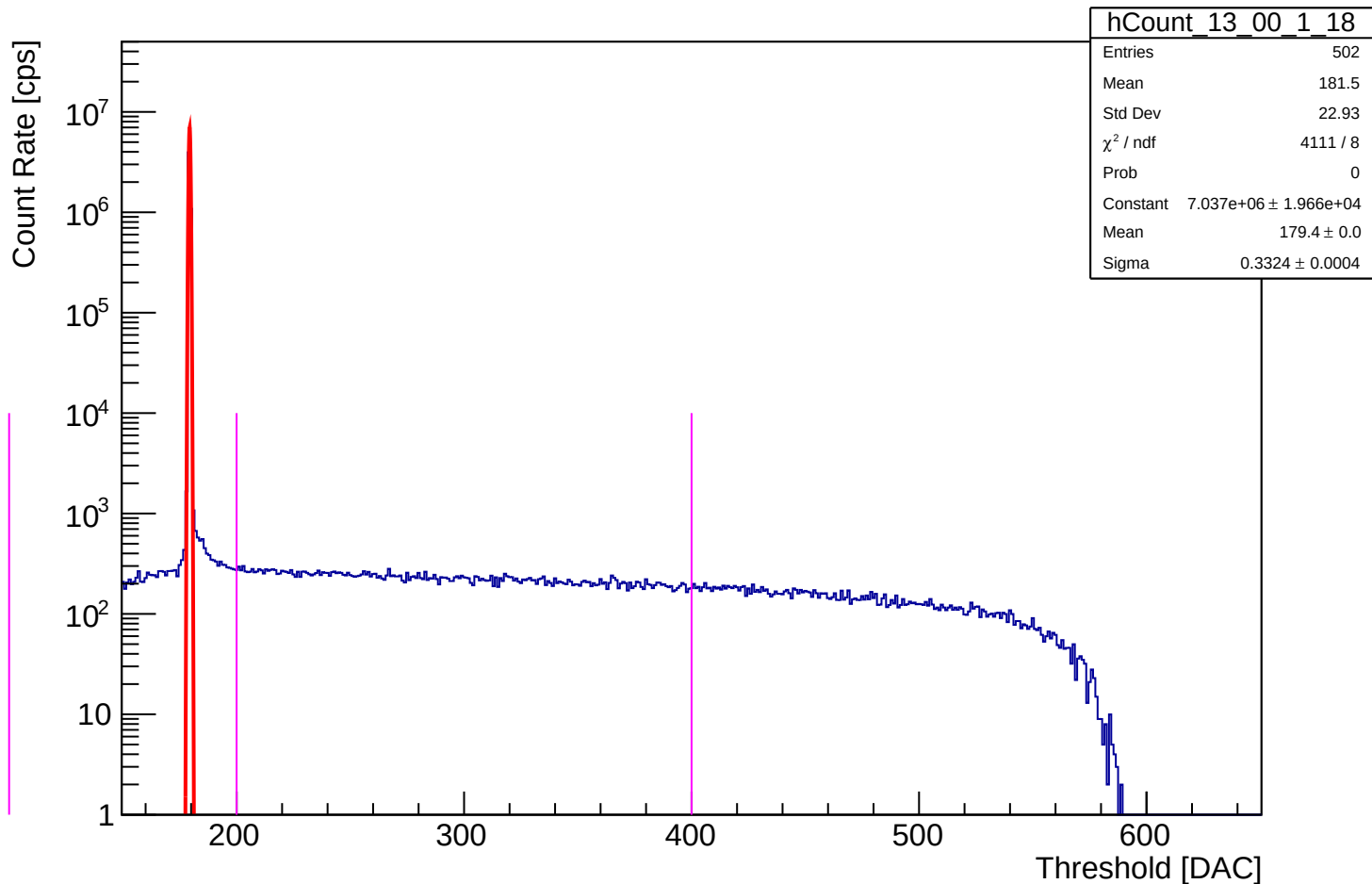
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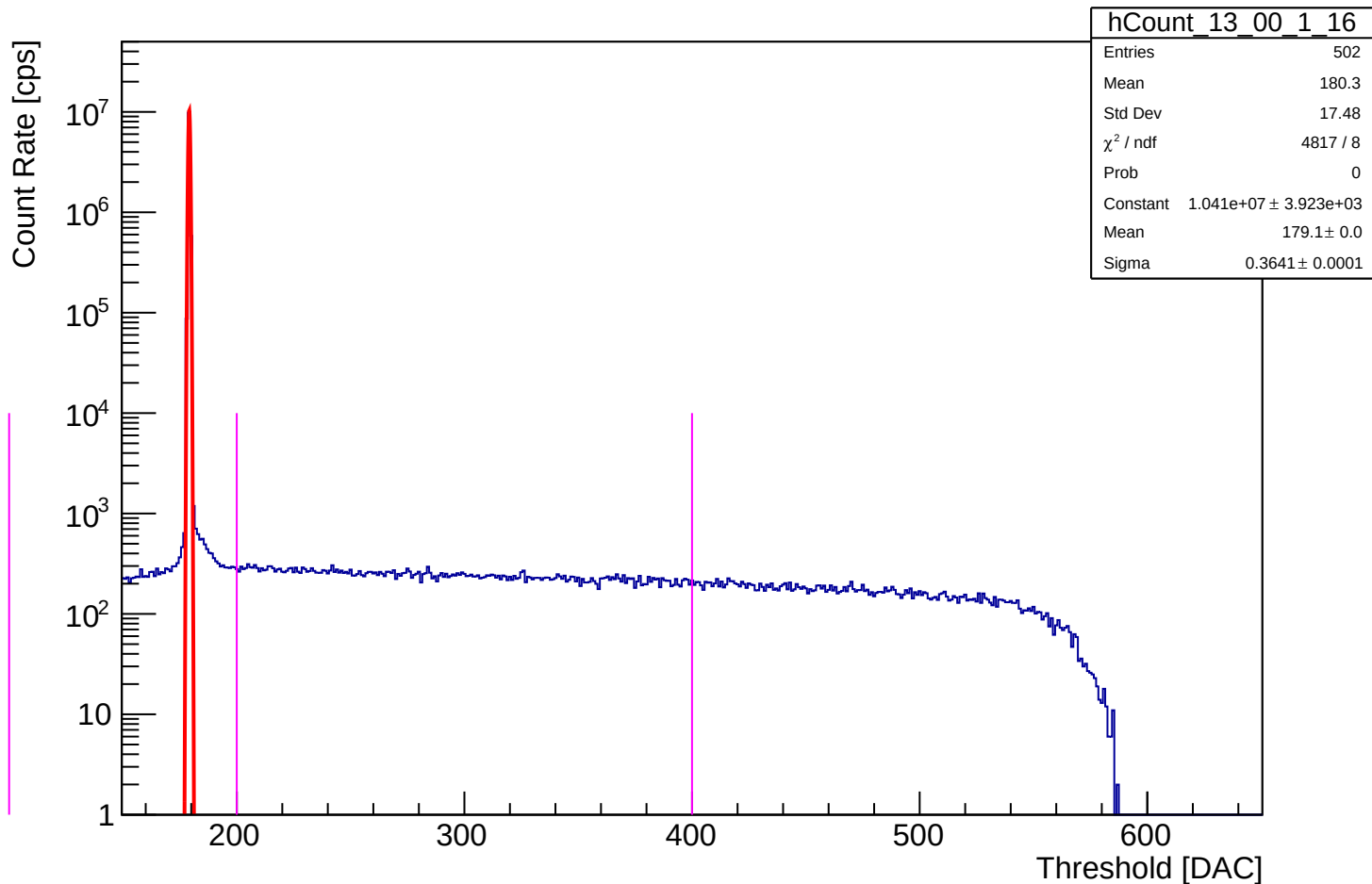
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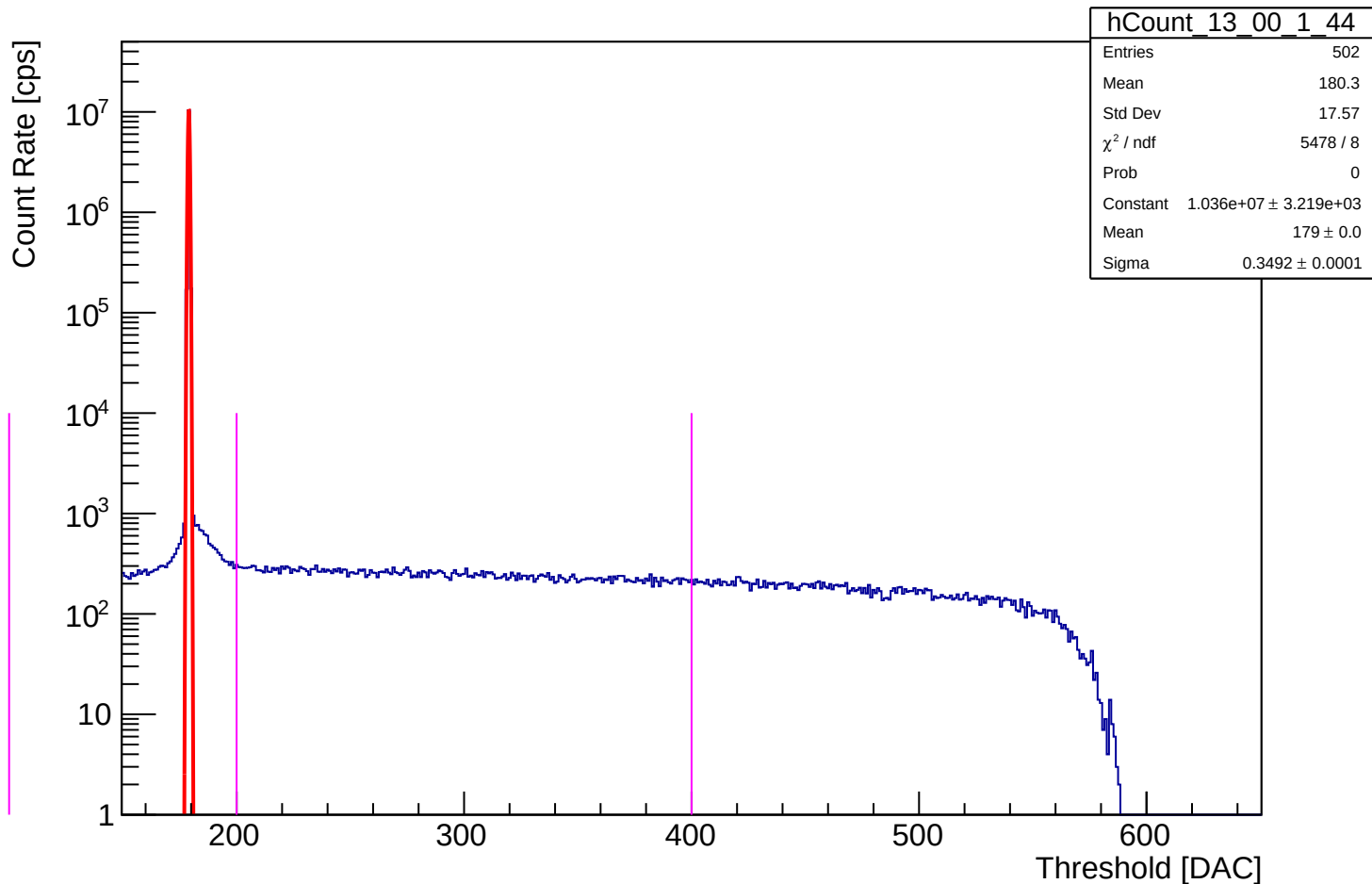
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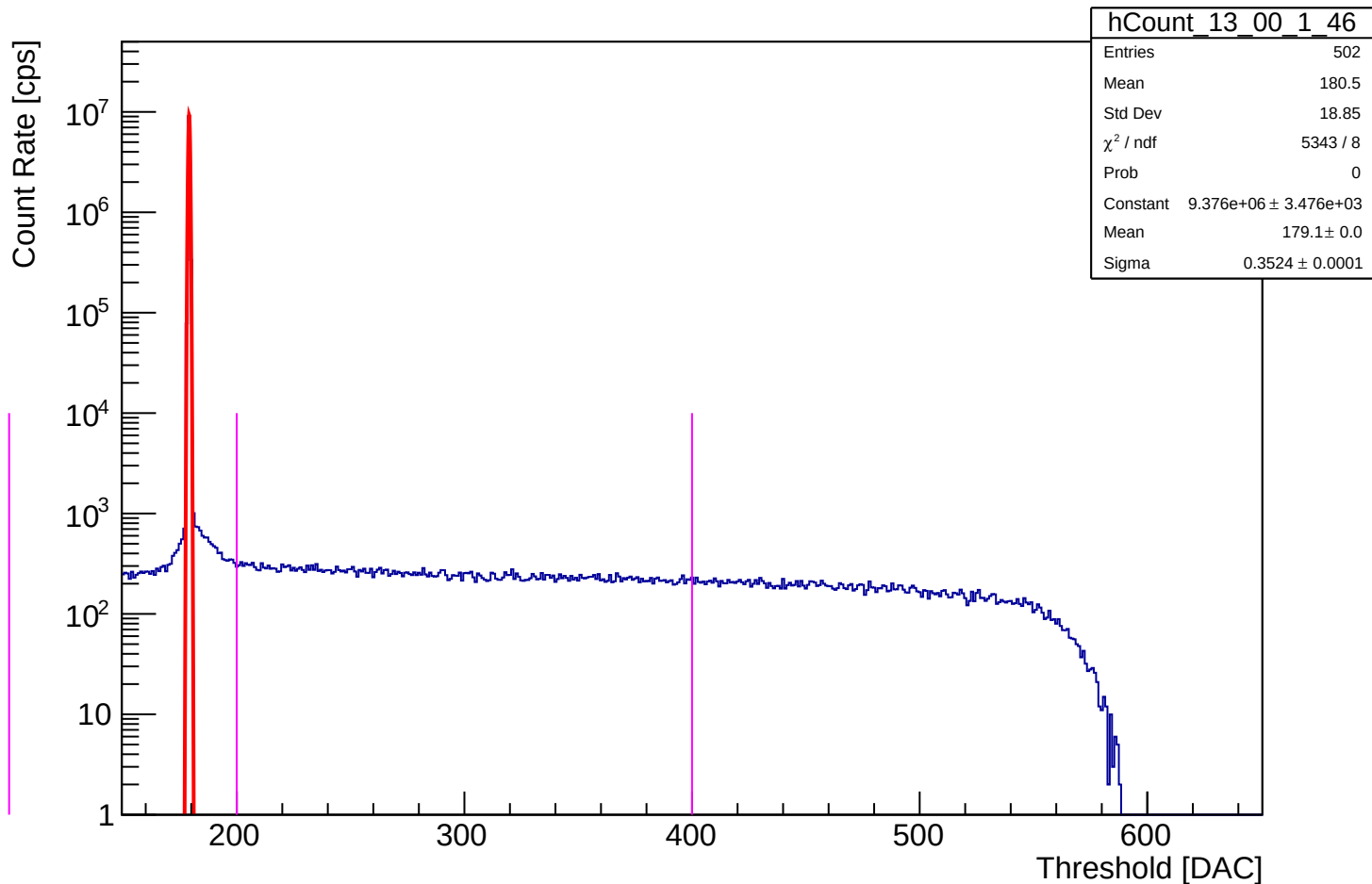
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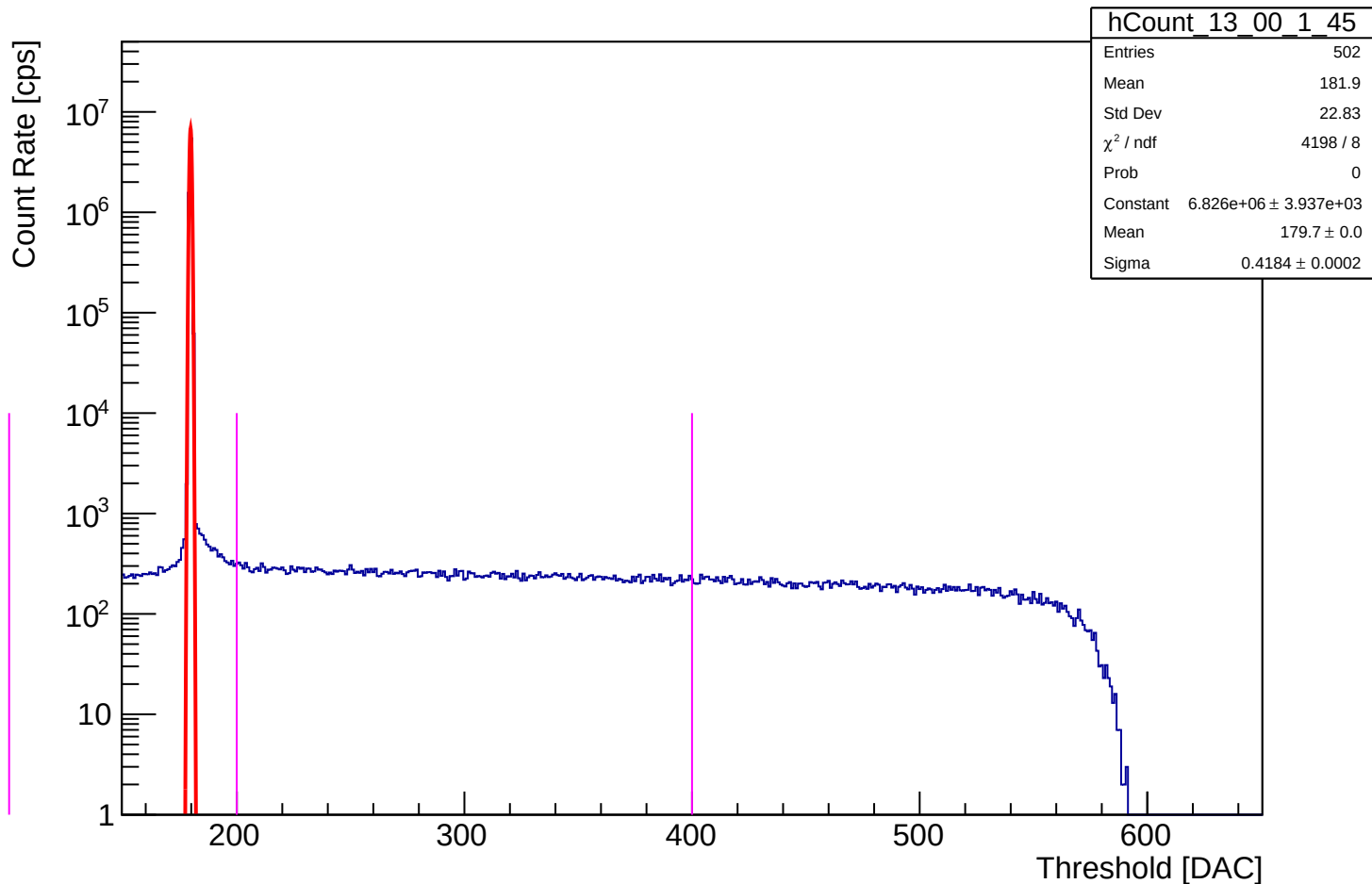
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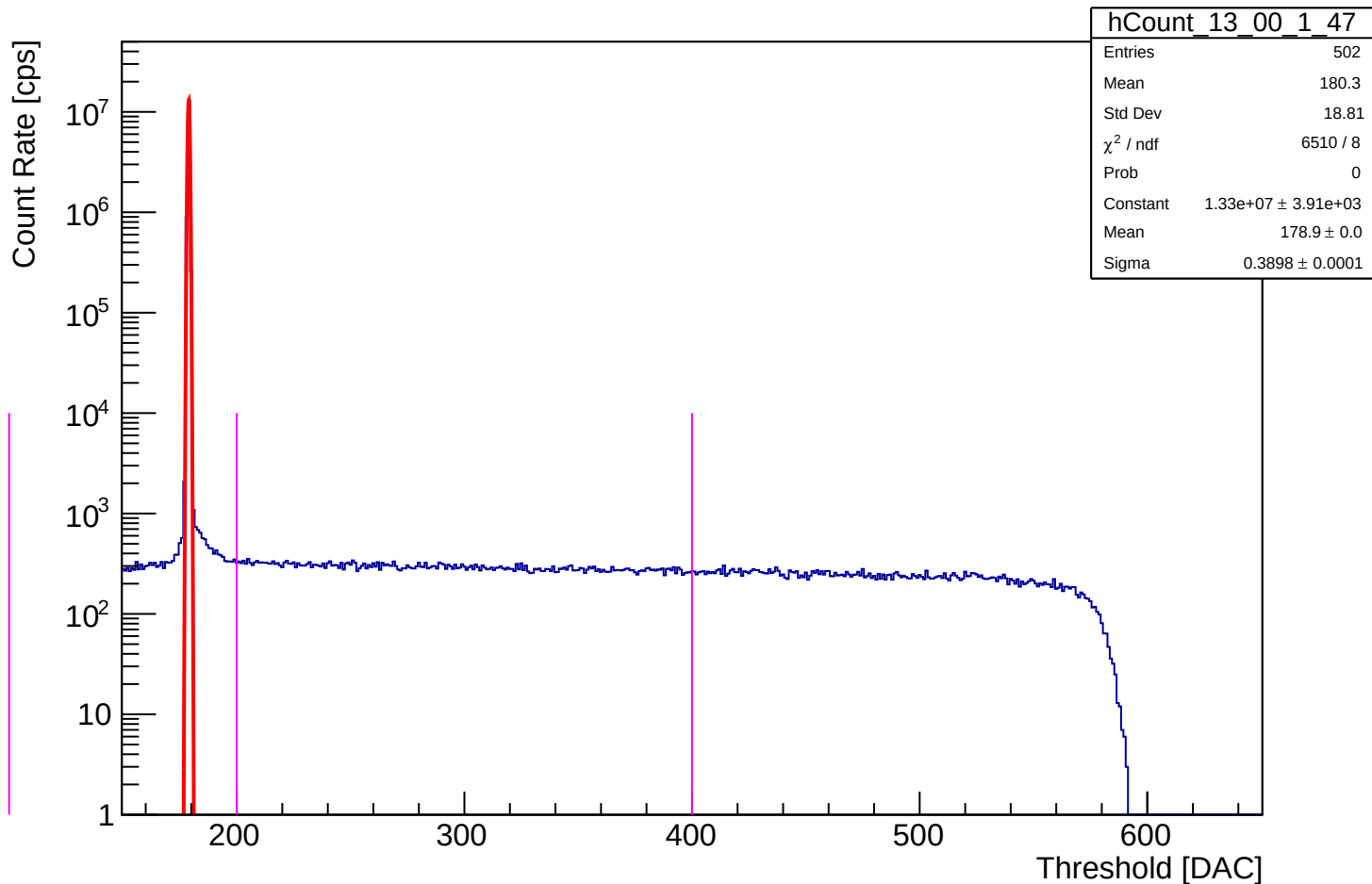
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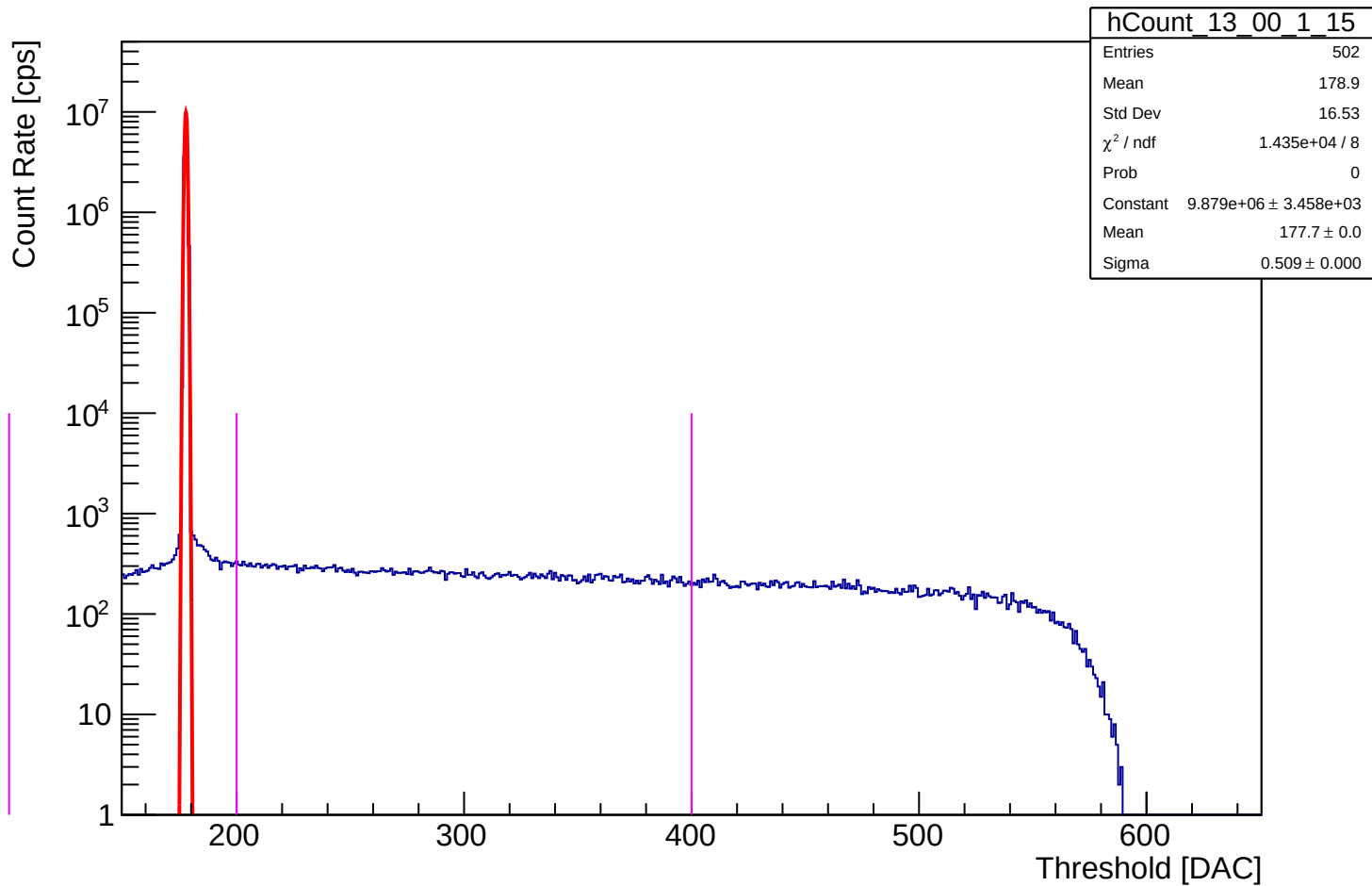
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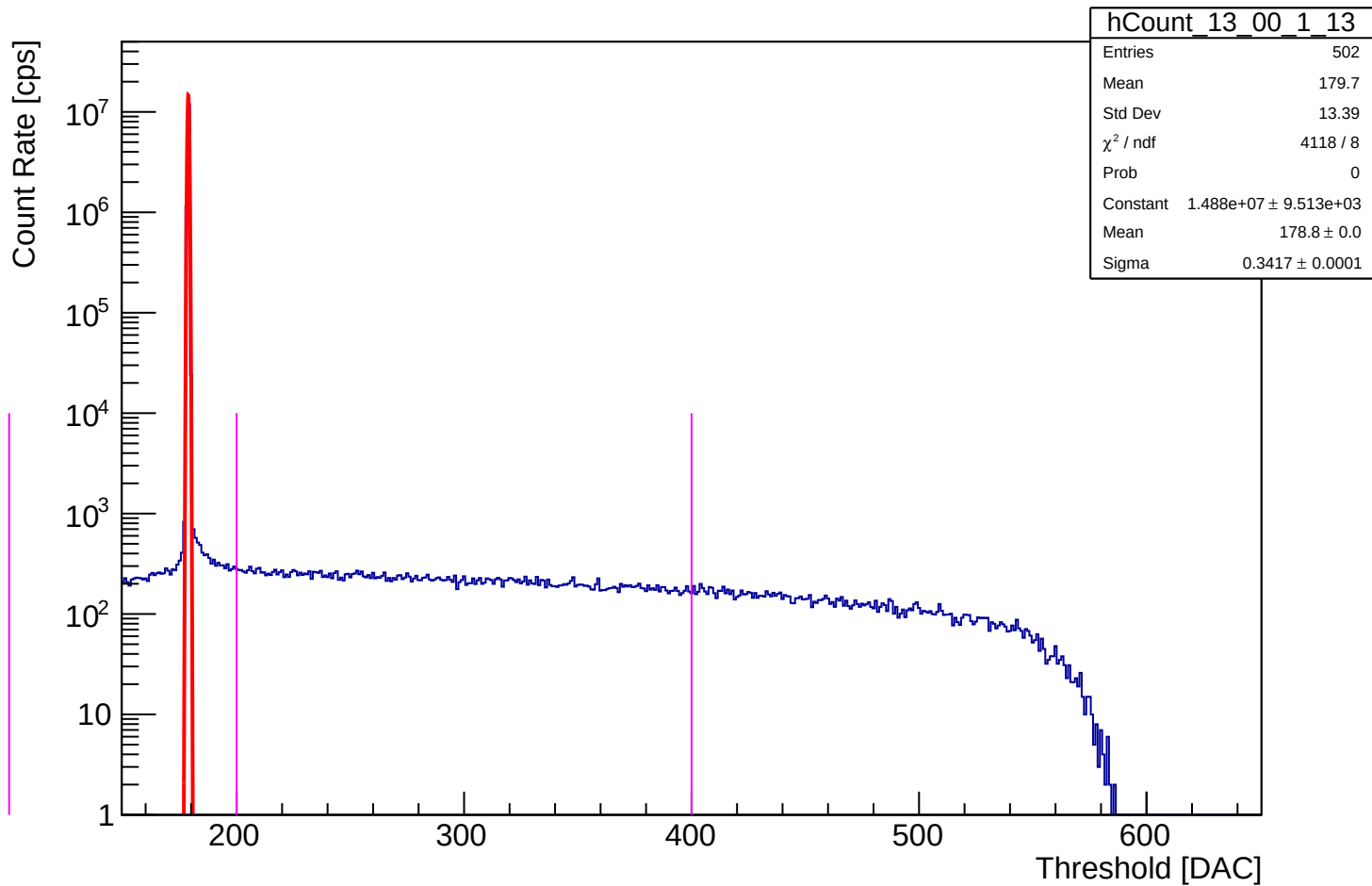
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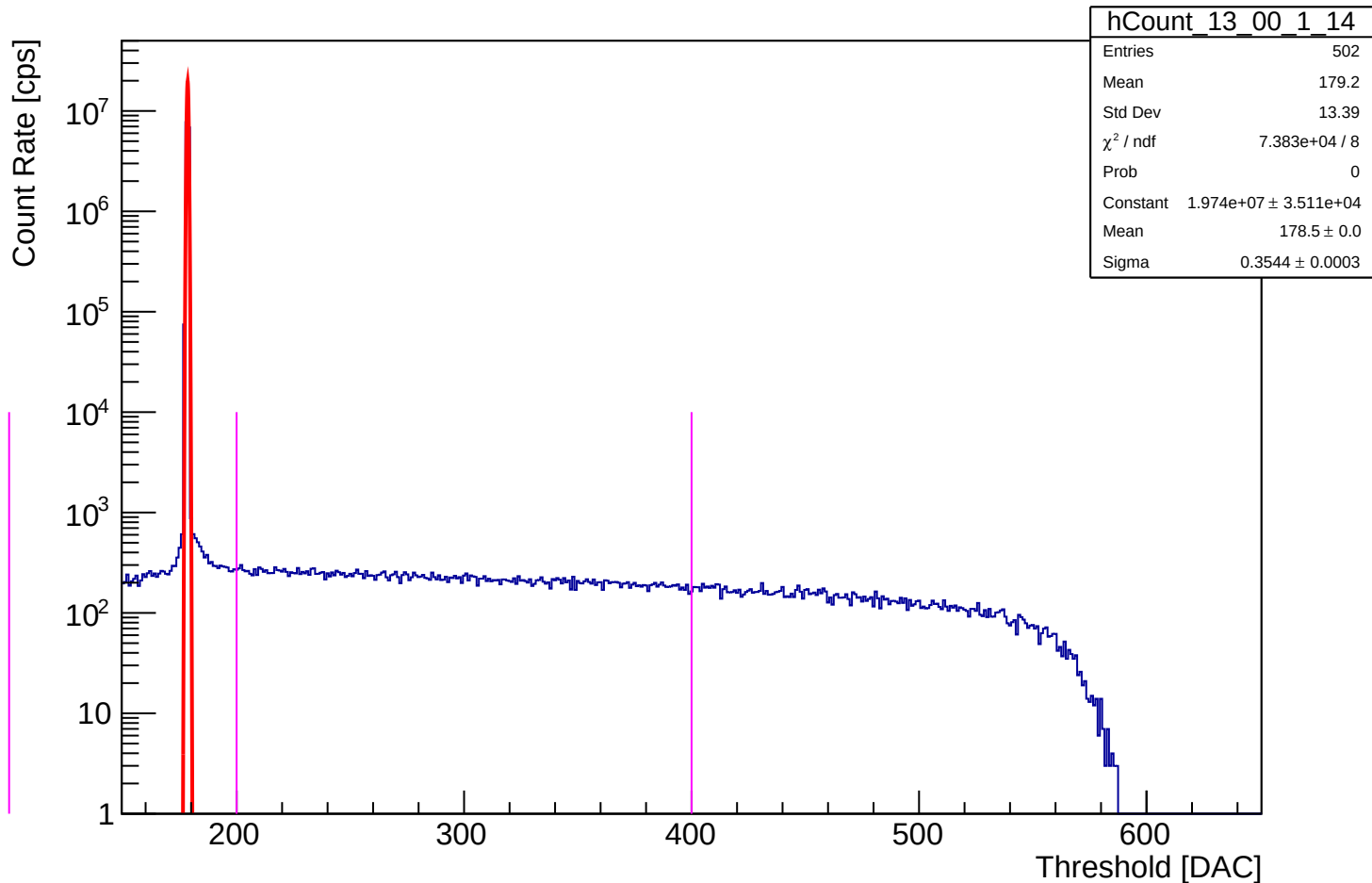
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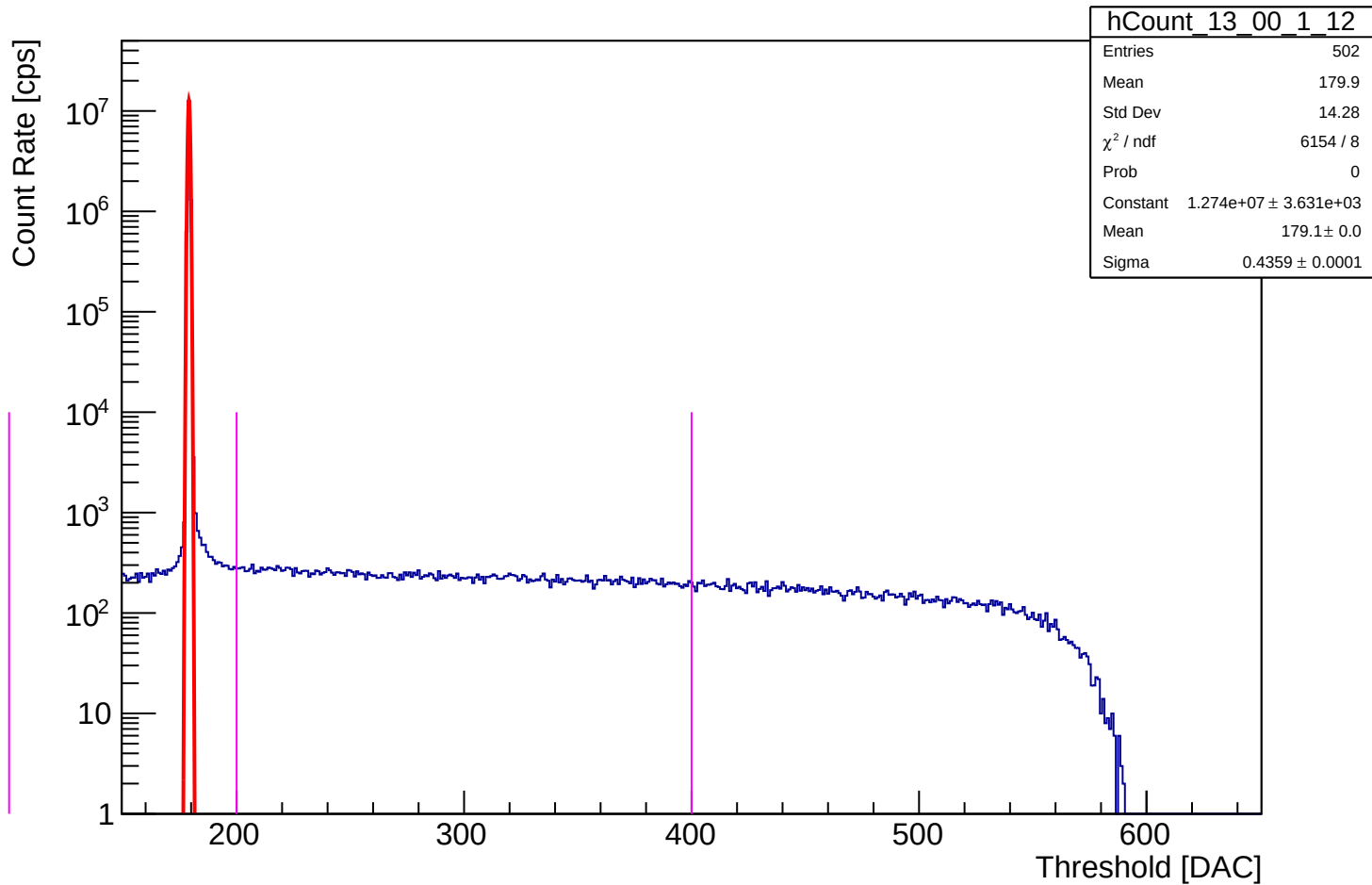
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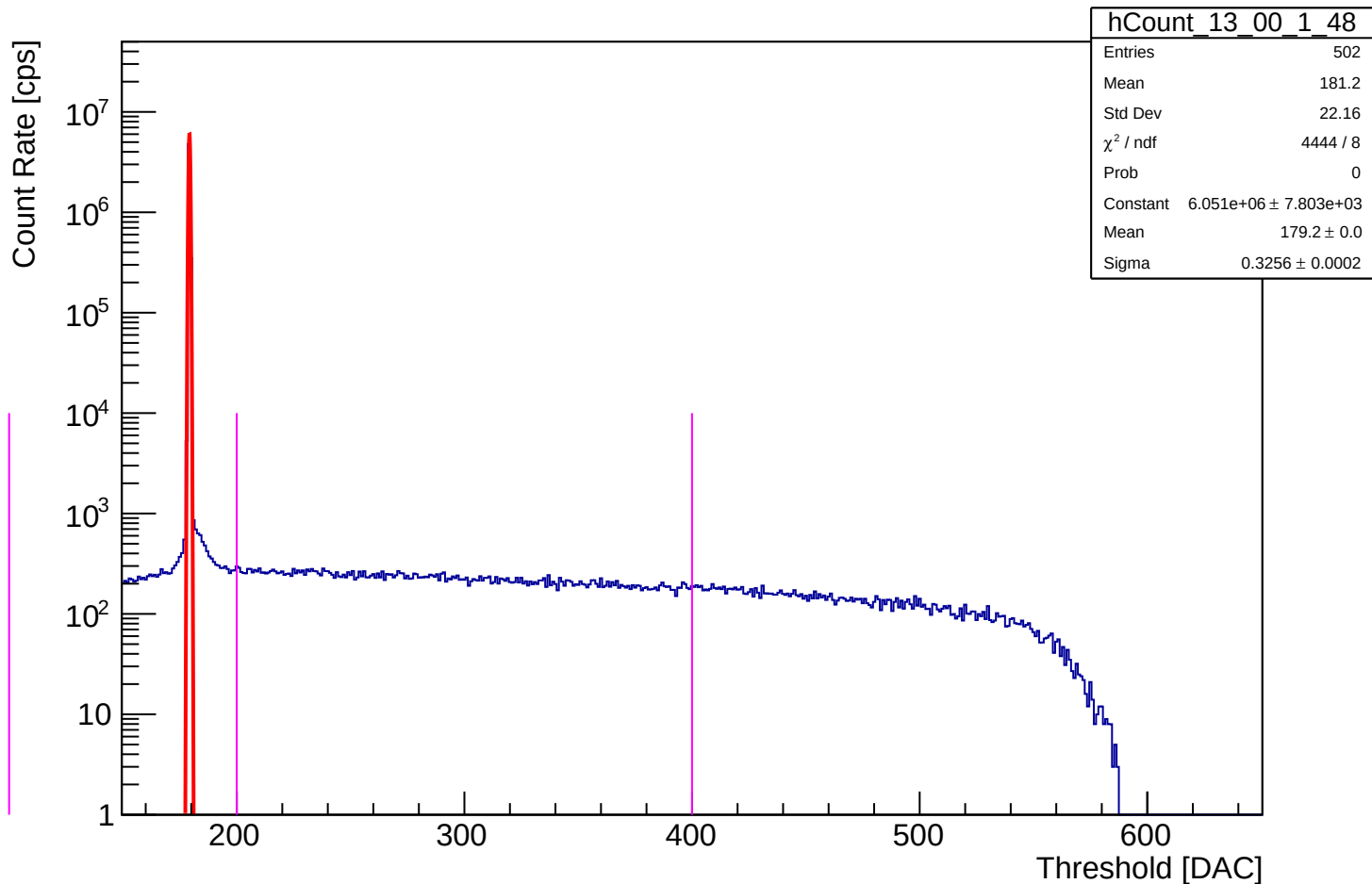
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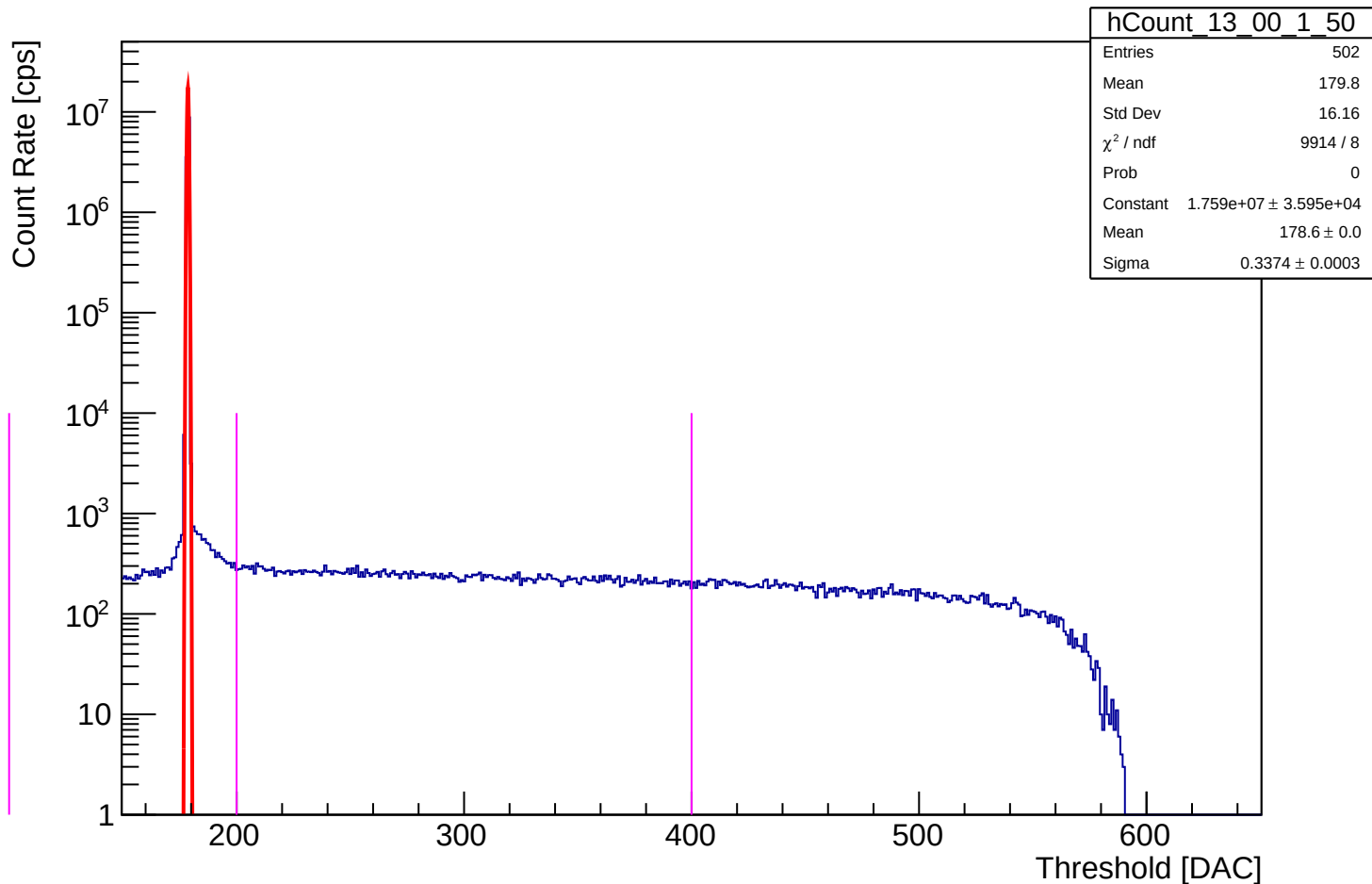
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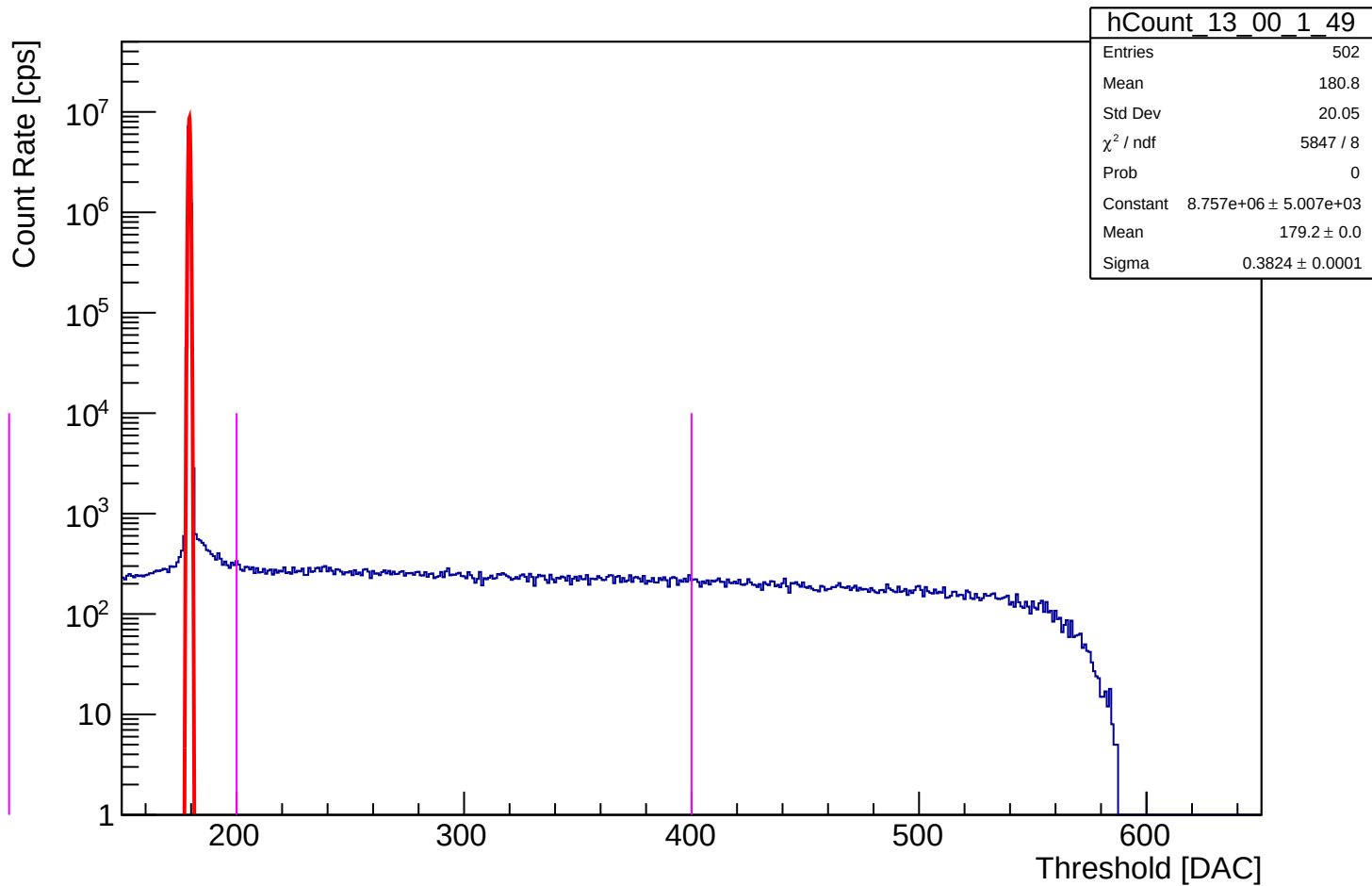
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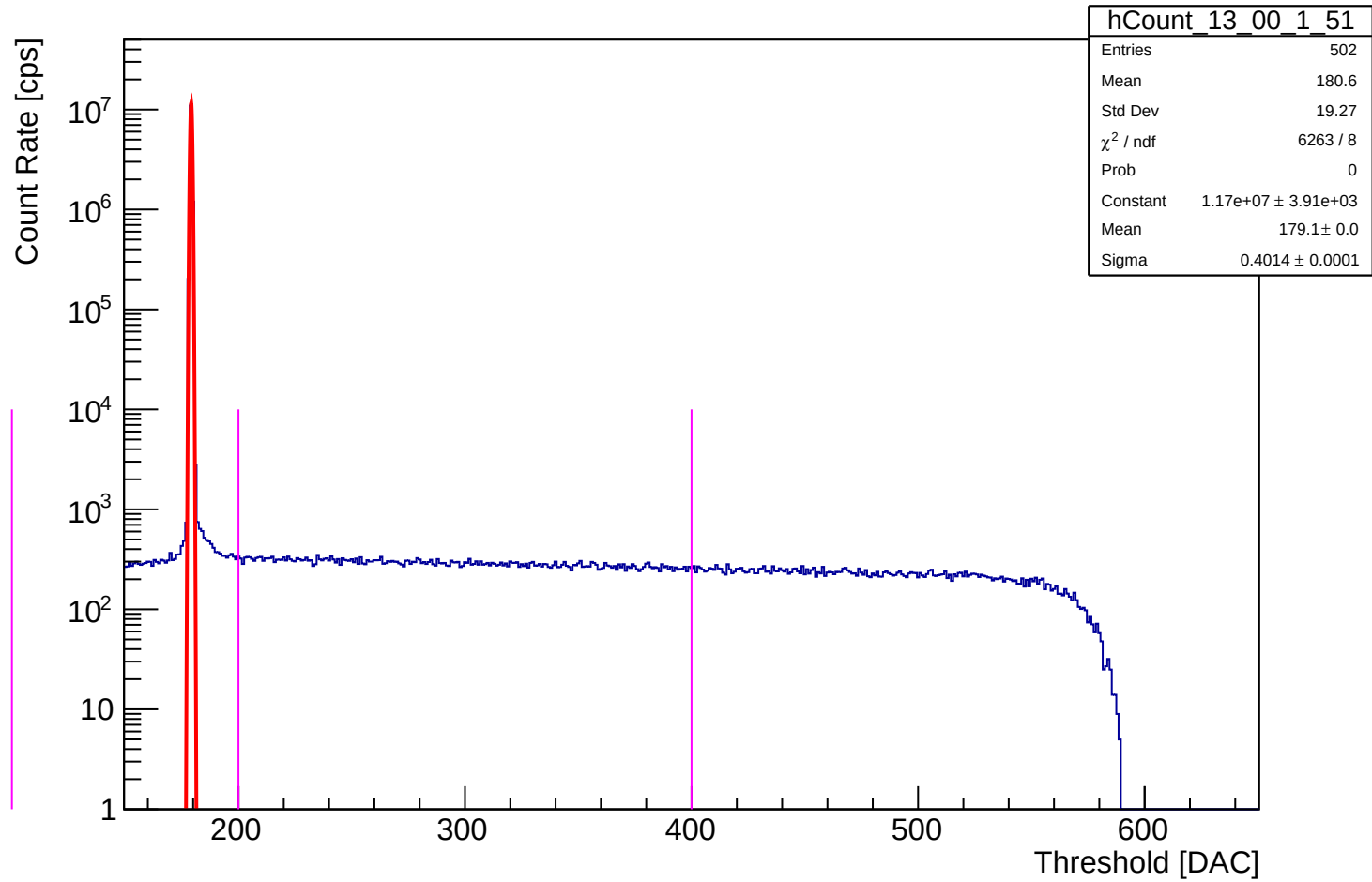


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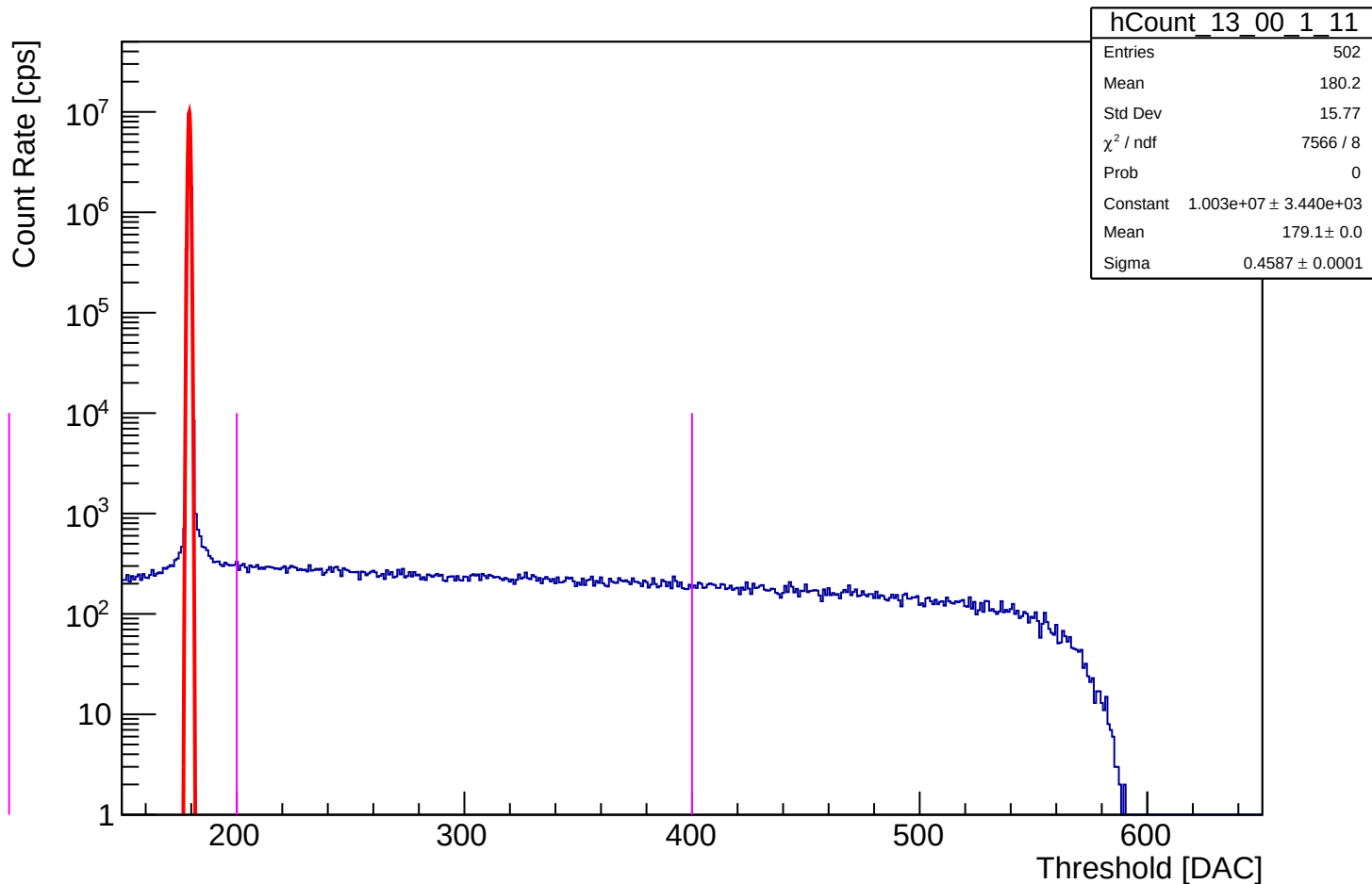


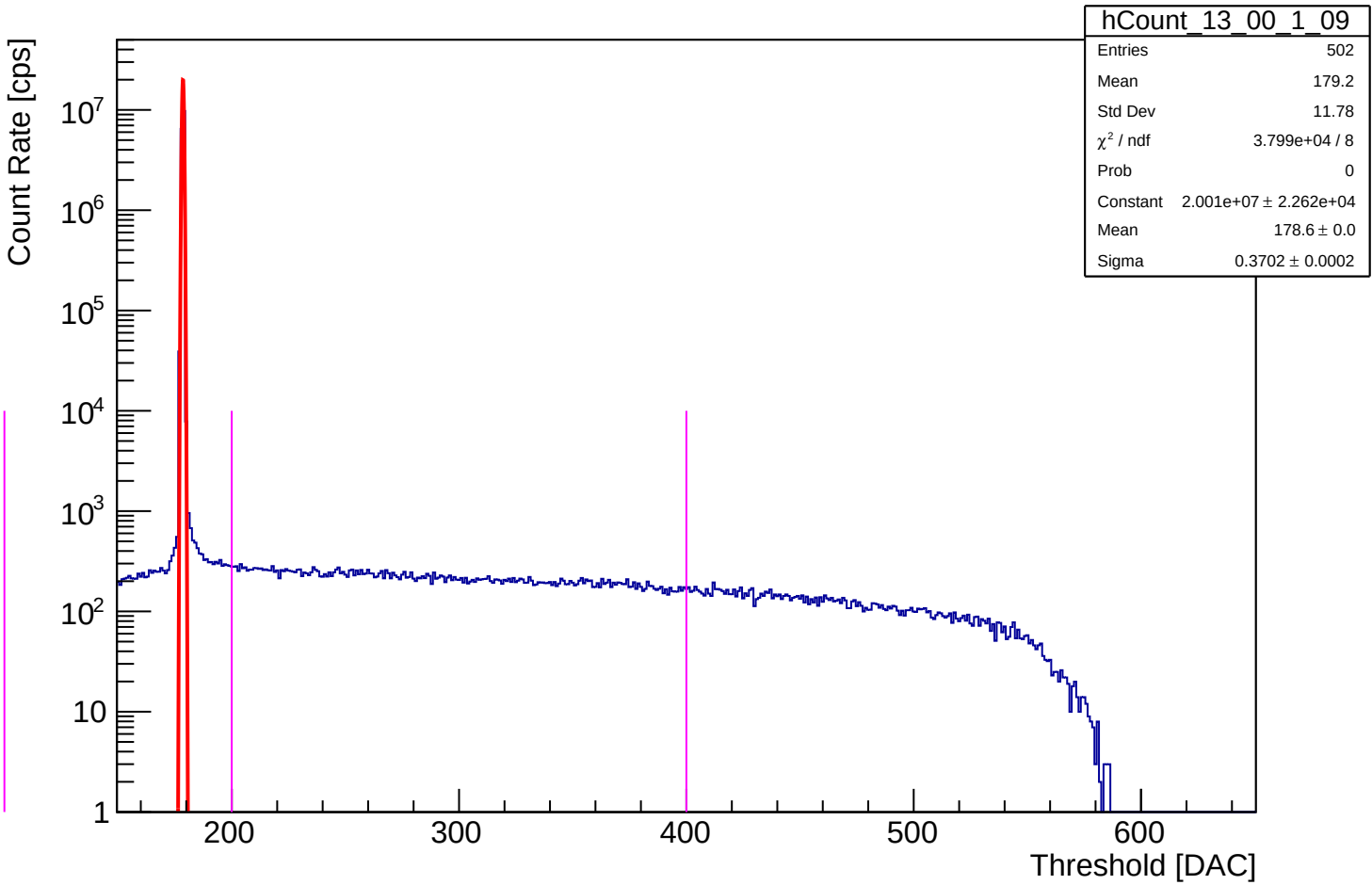
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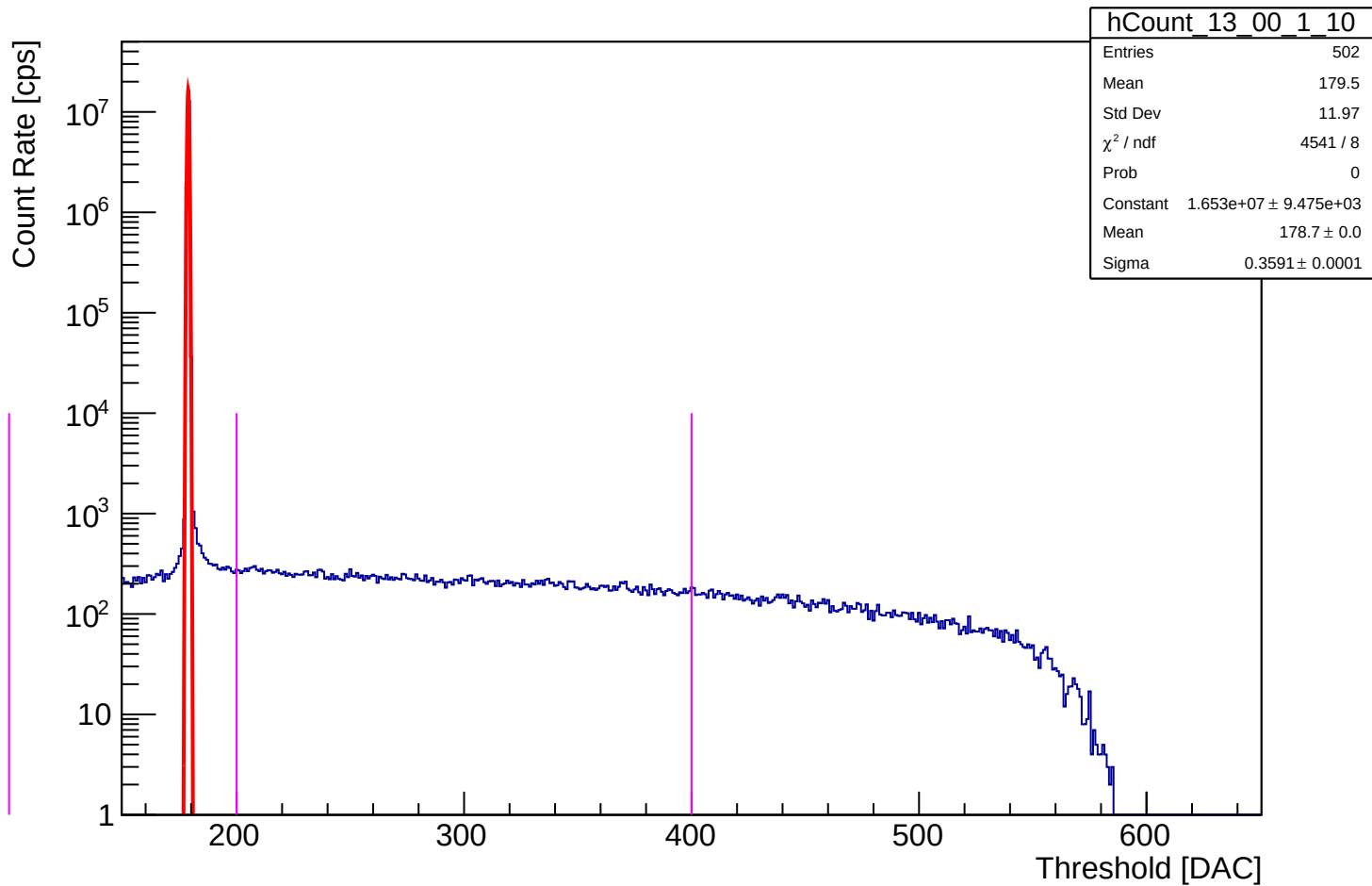


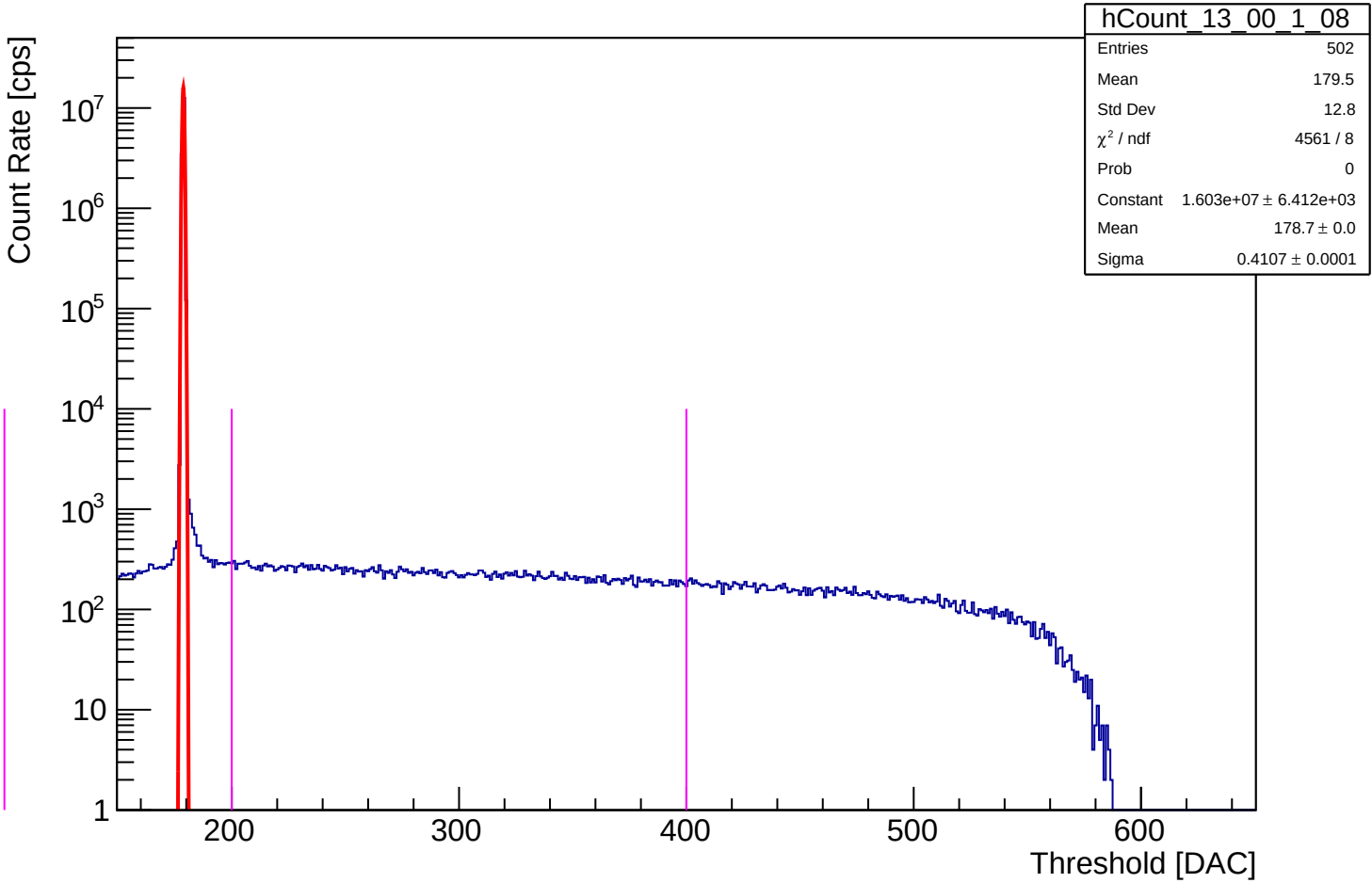
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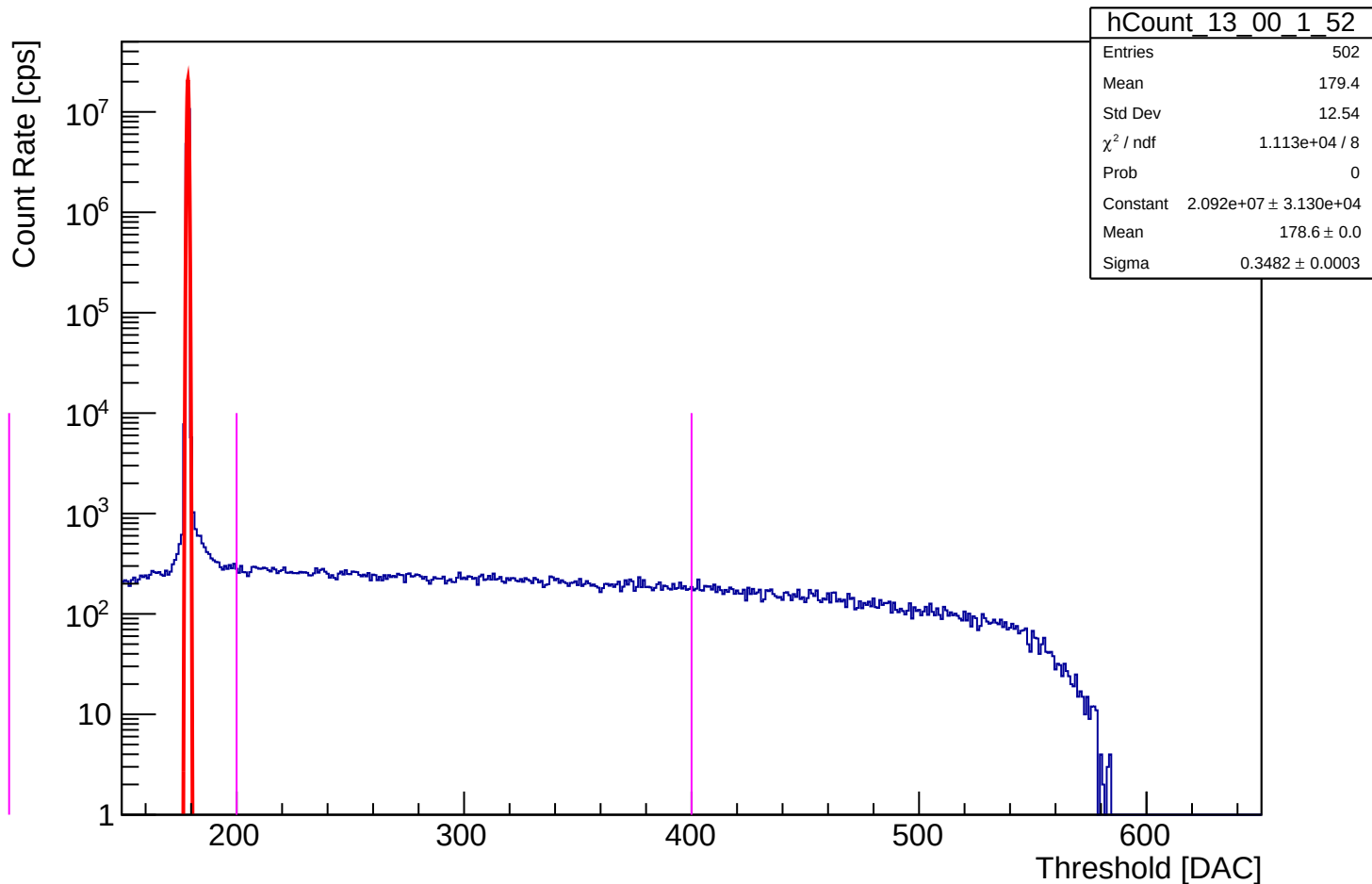


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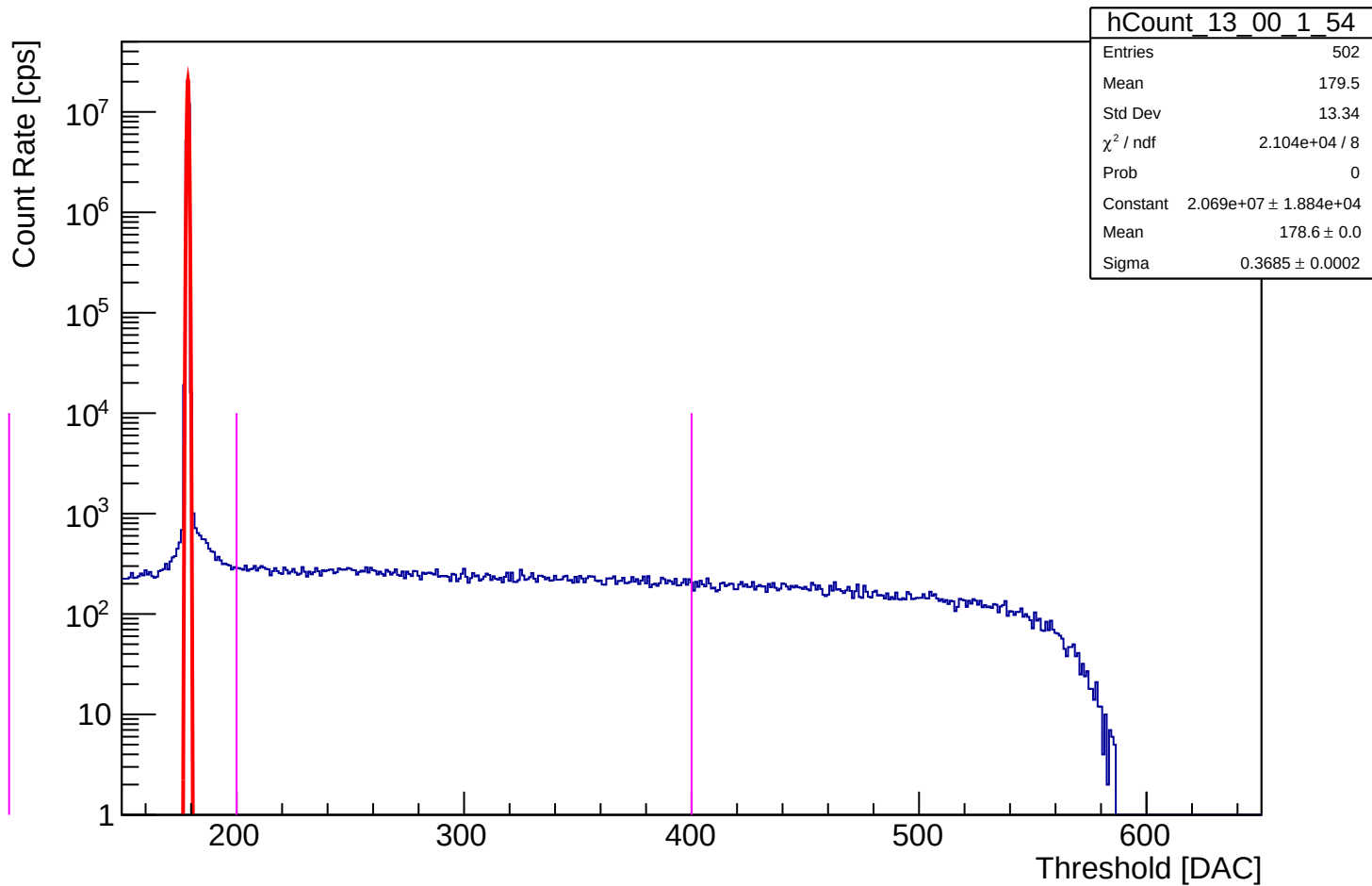




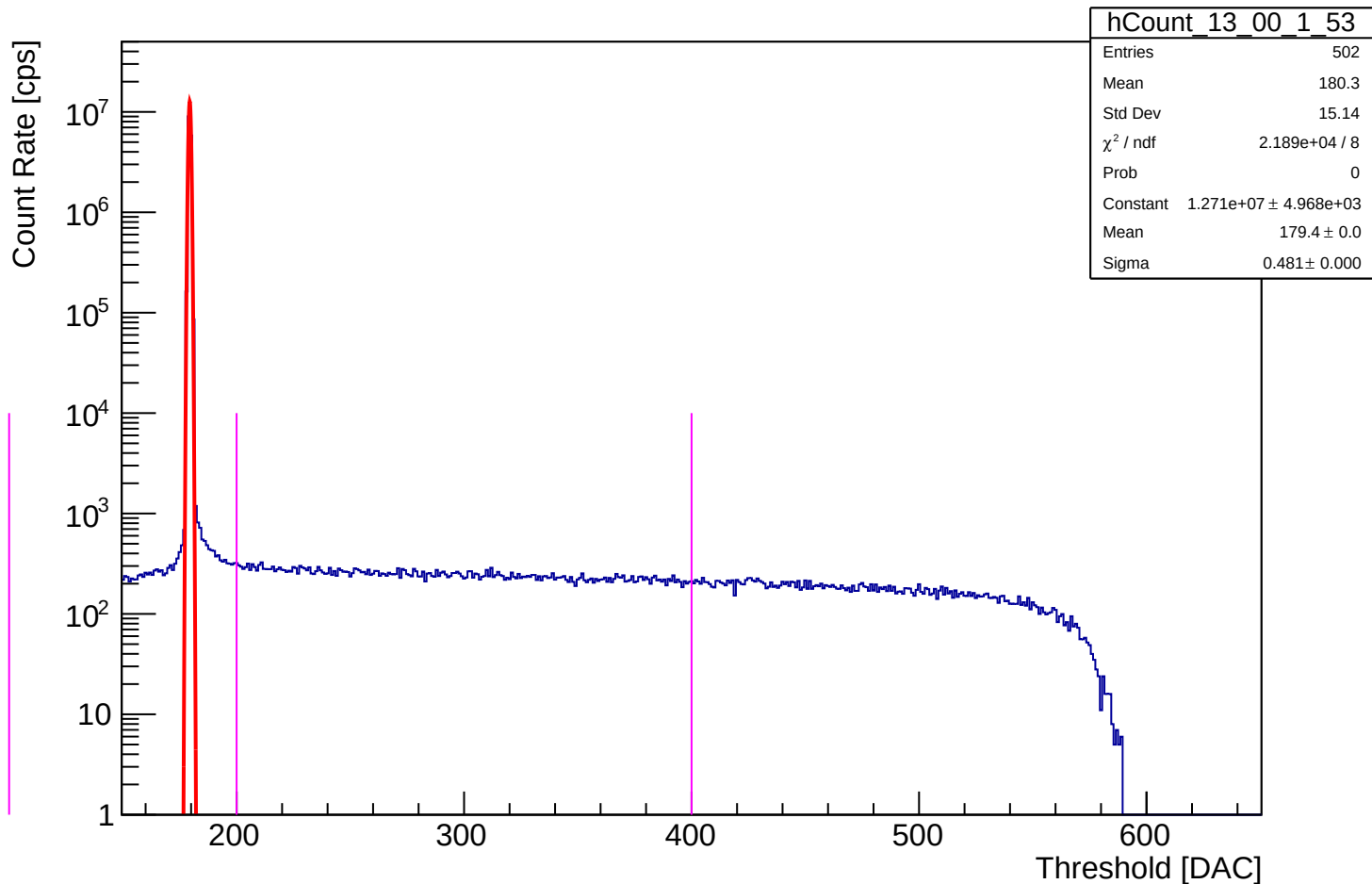
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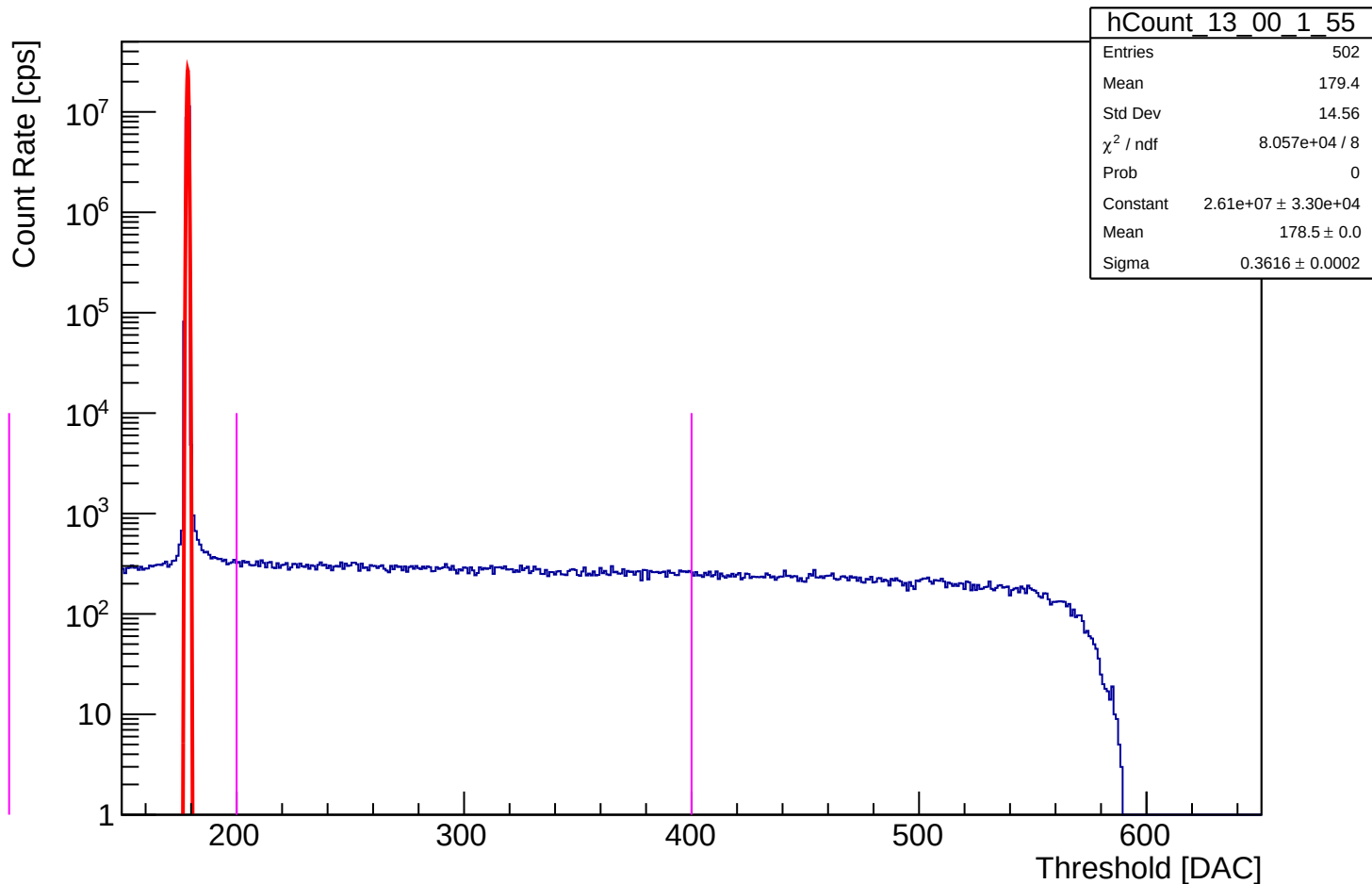
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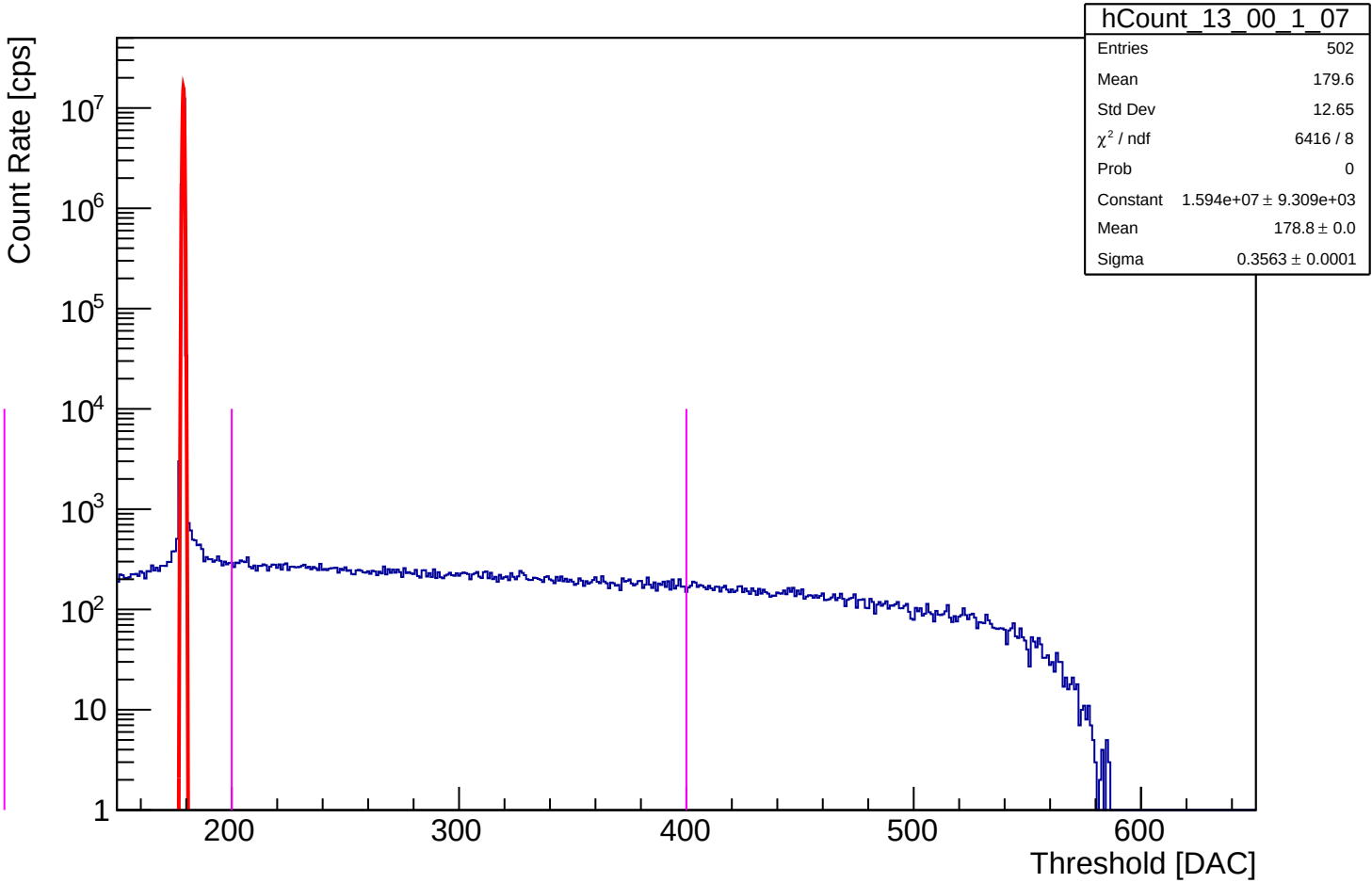


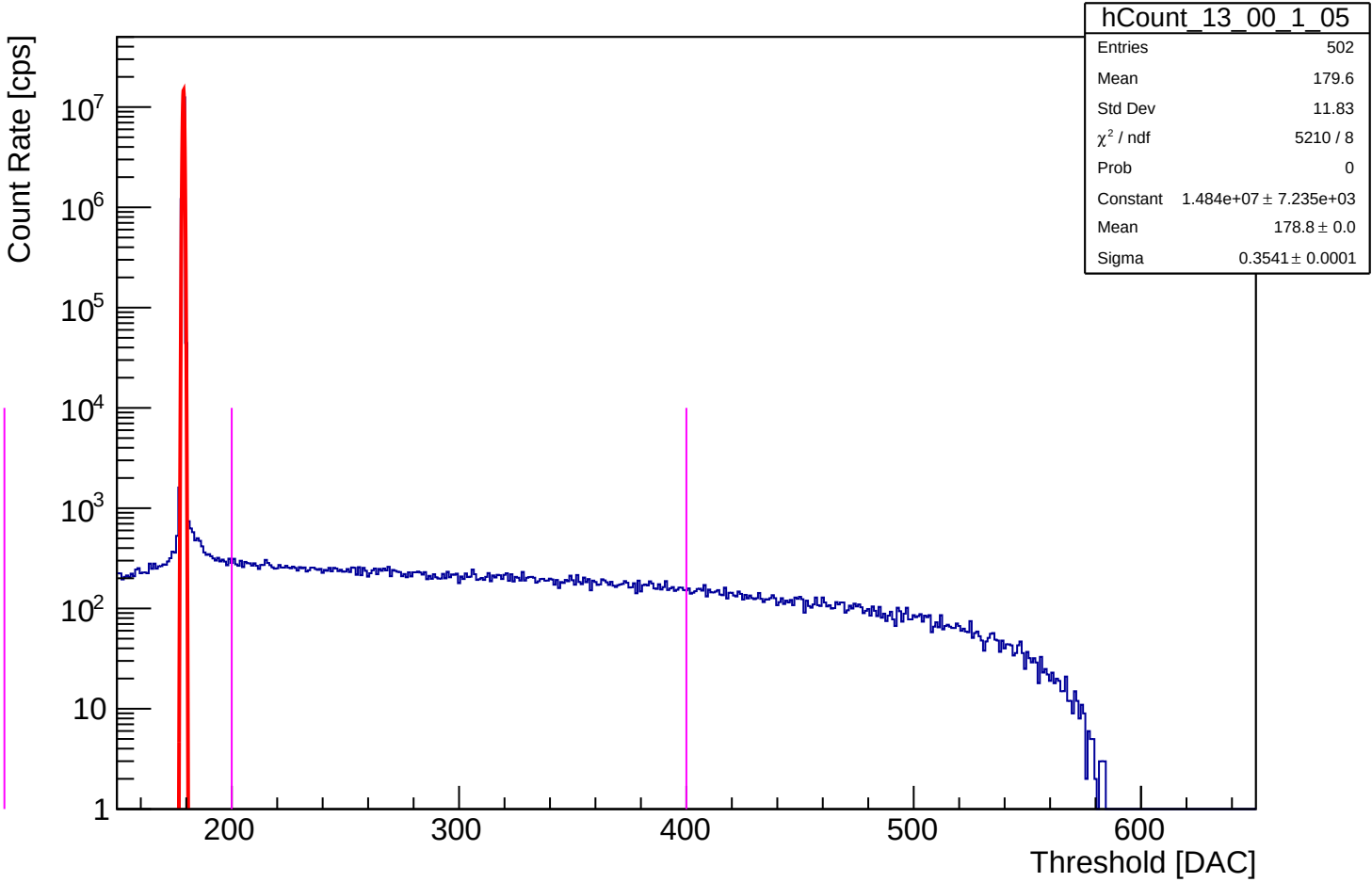
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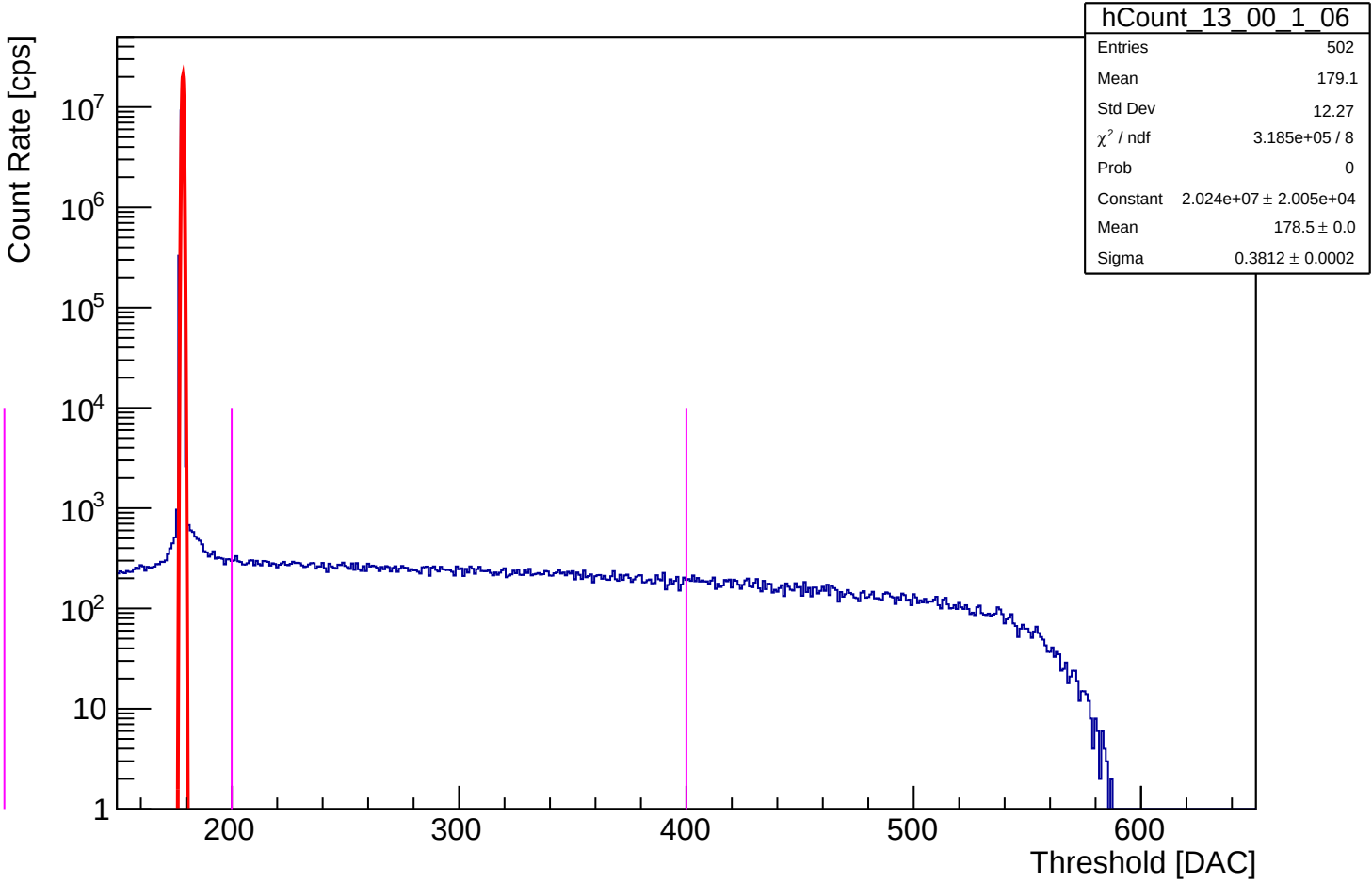


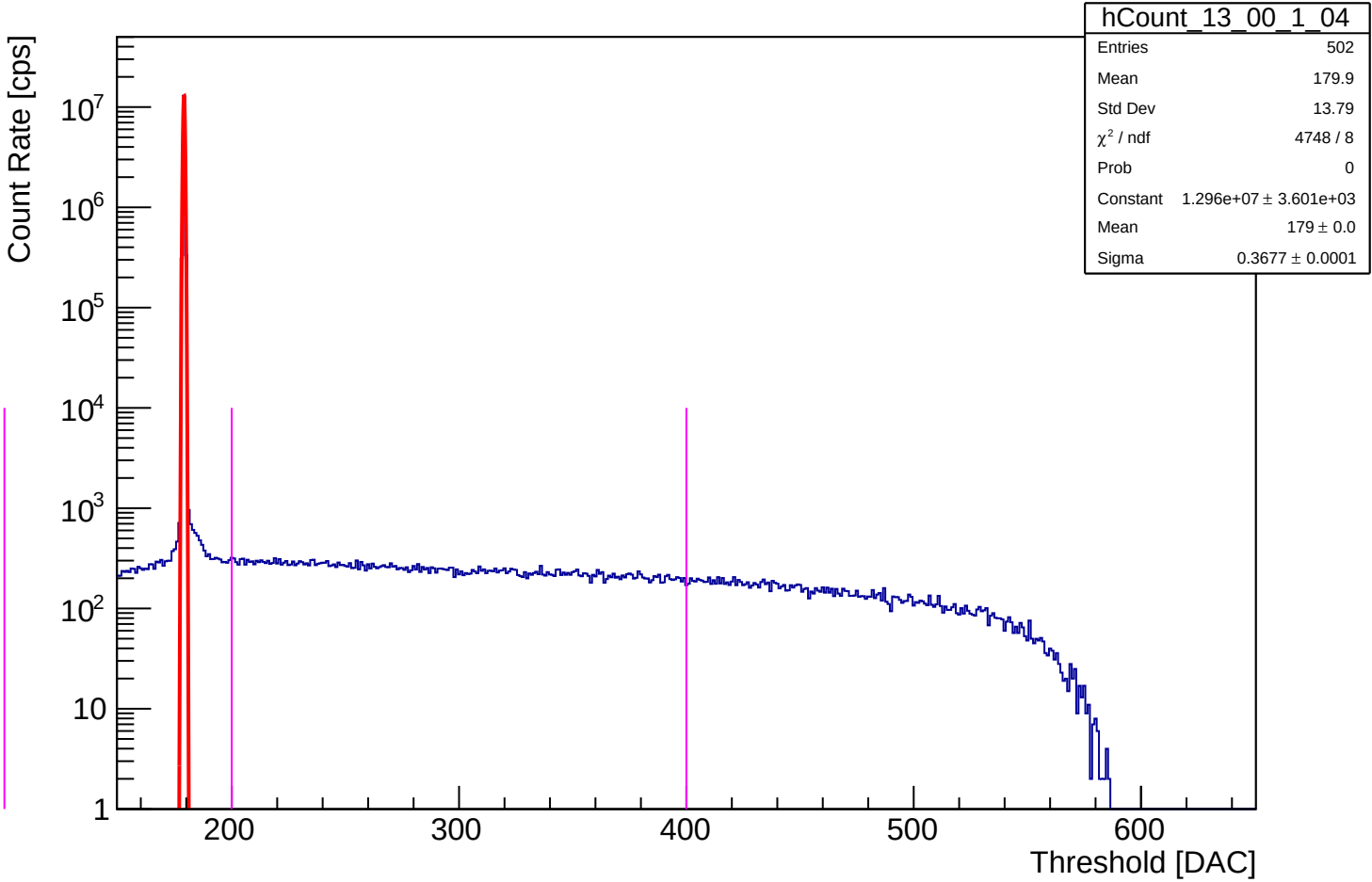
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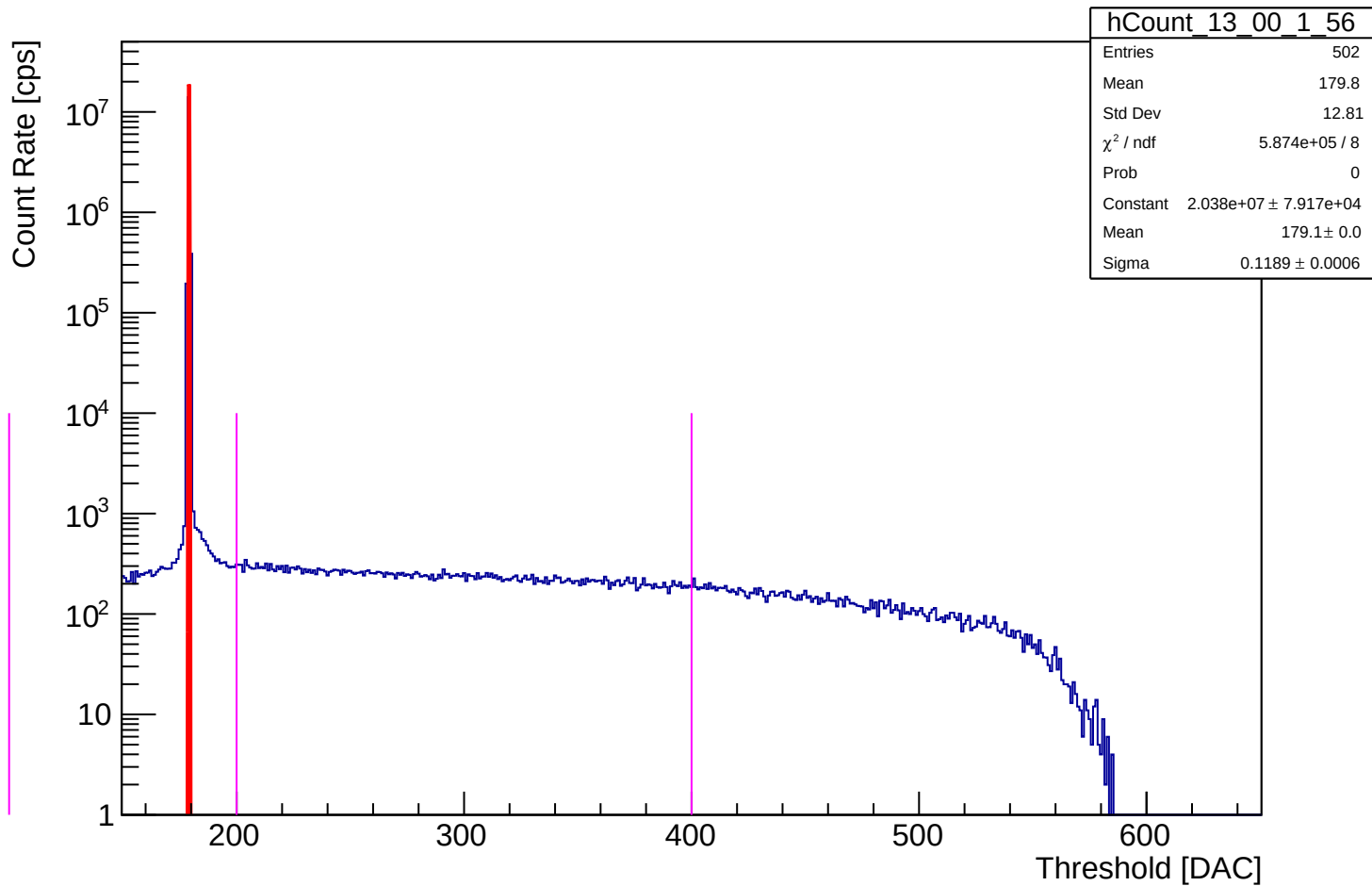




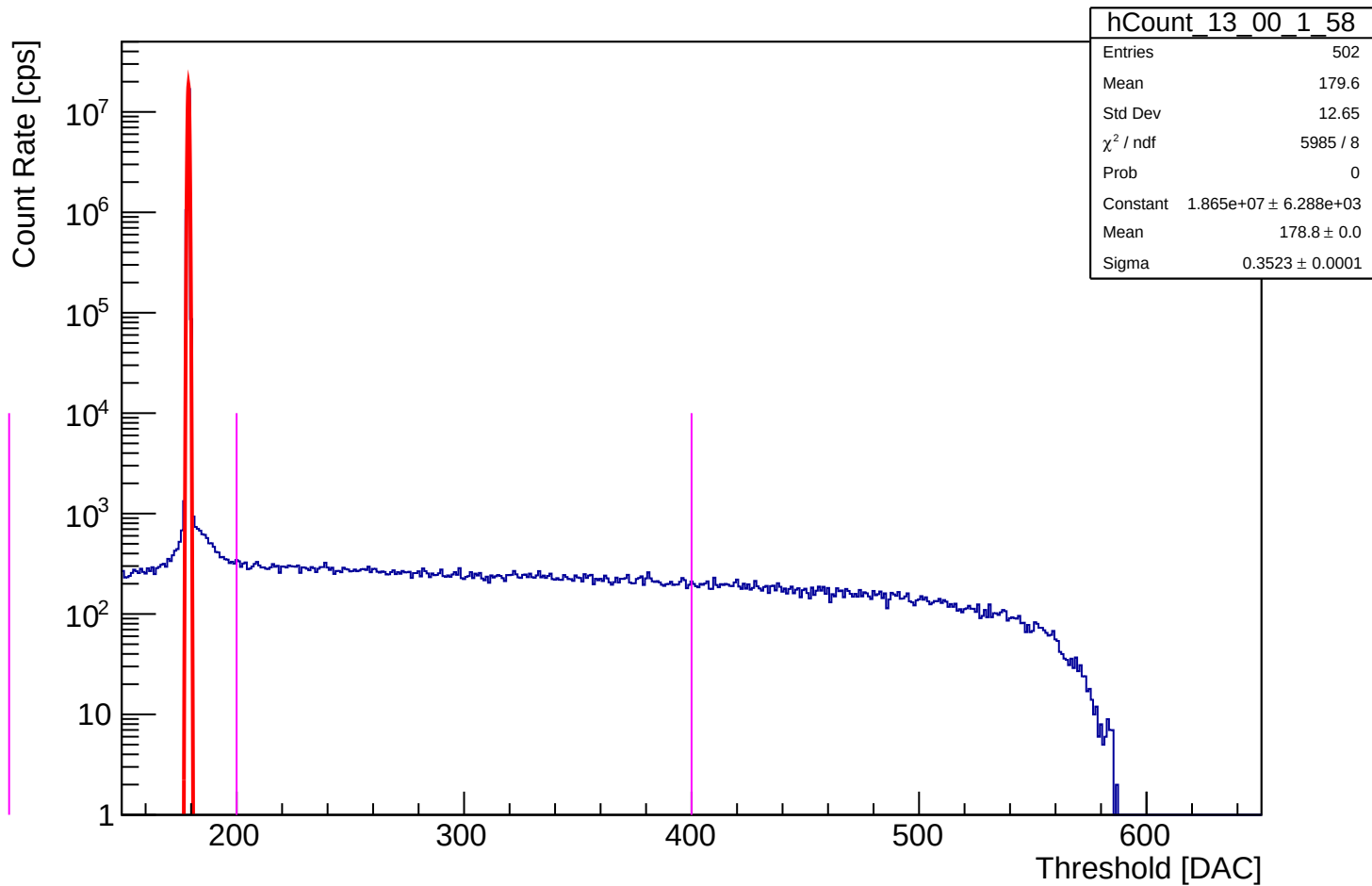




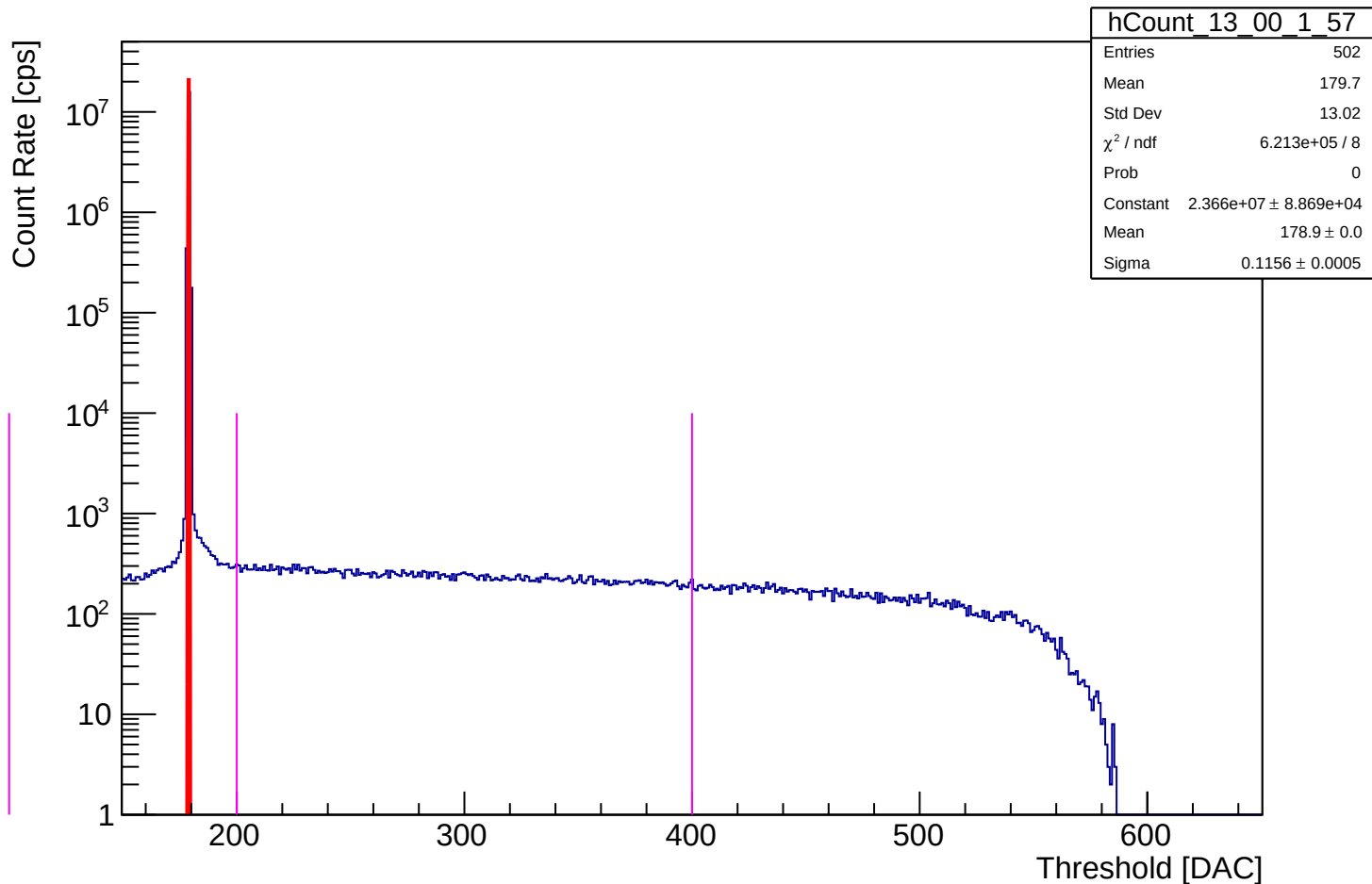
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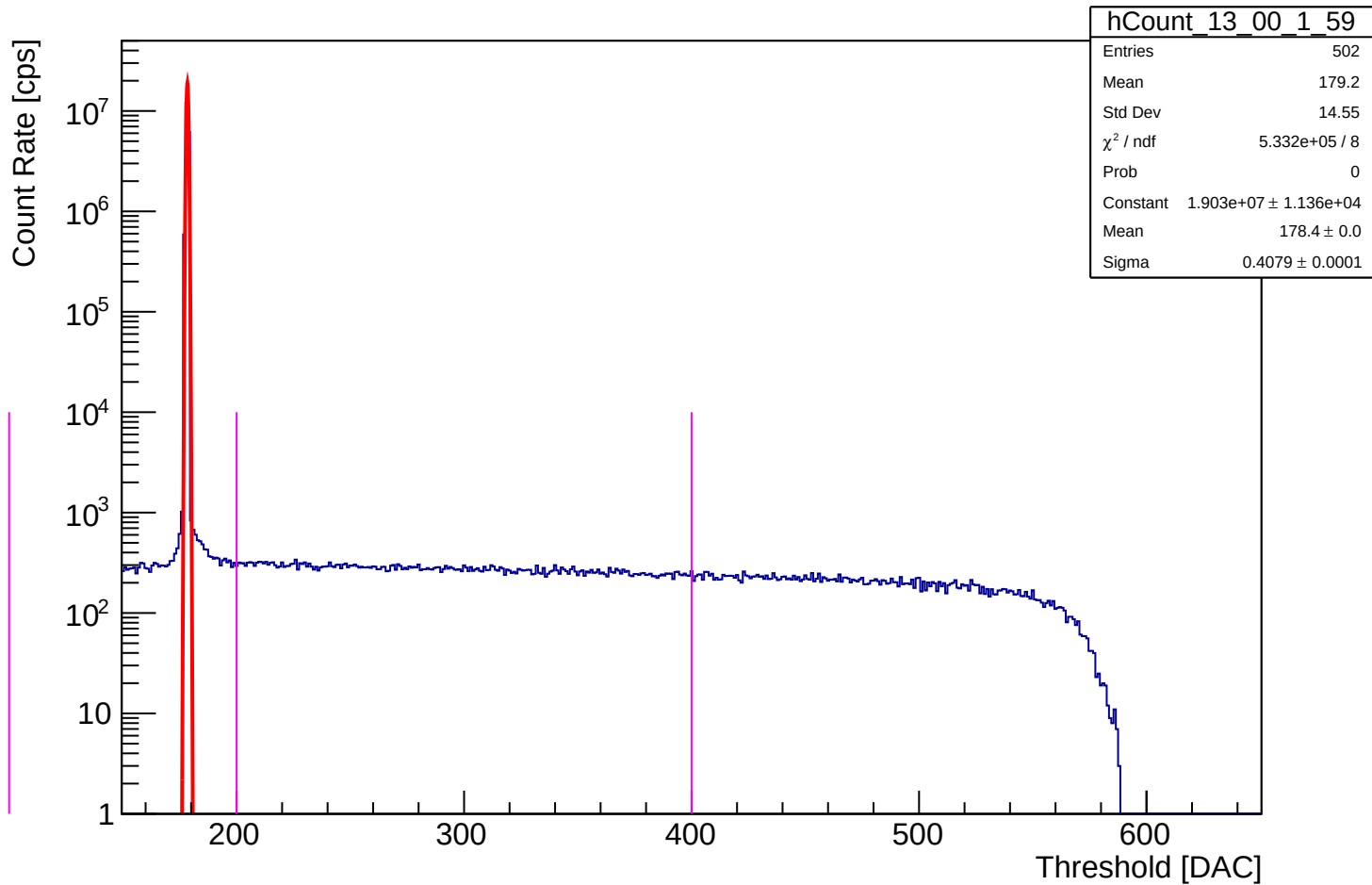
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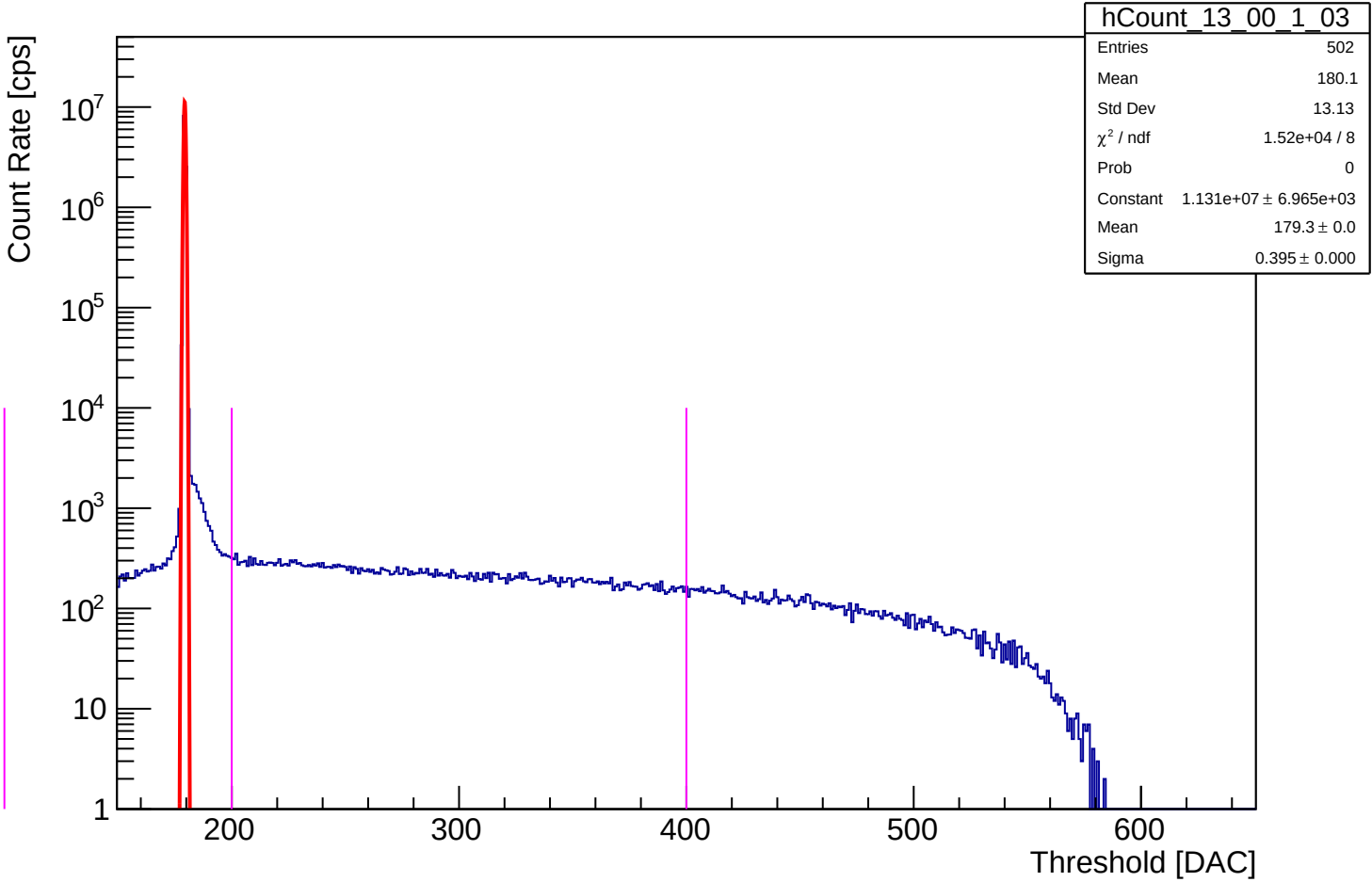


Row 1 Tile 1 Pmt 2 Pixel 55 Slot 13 Fiber 0 Asic 1 Channel 57

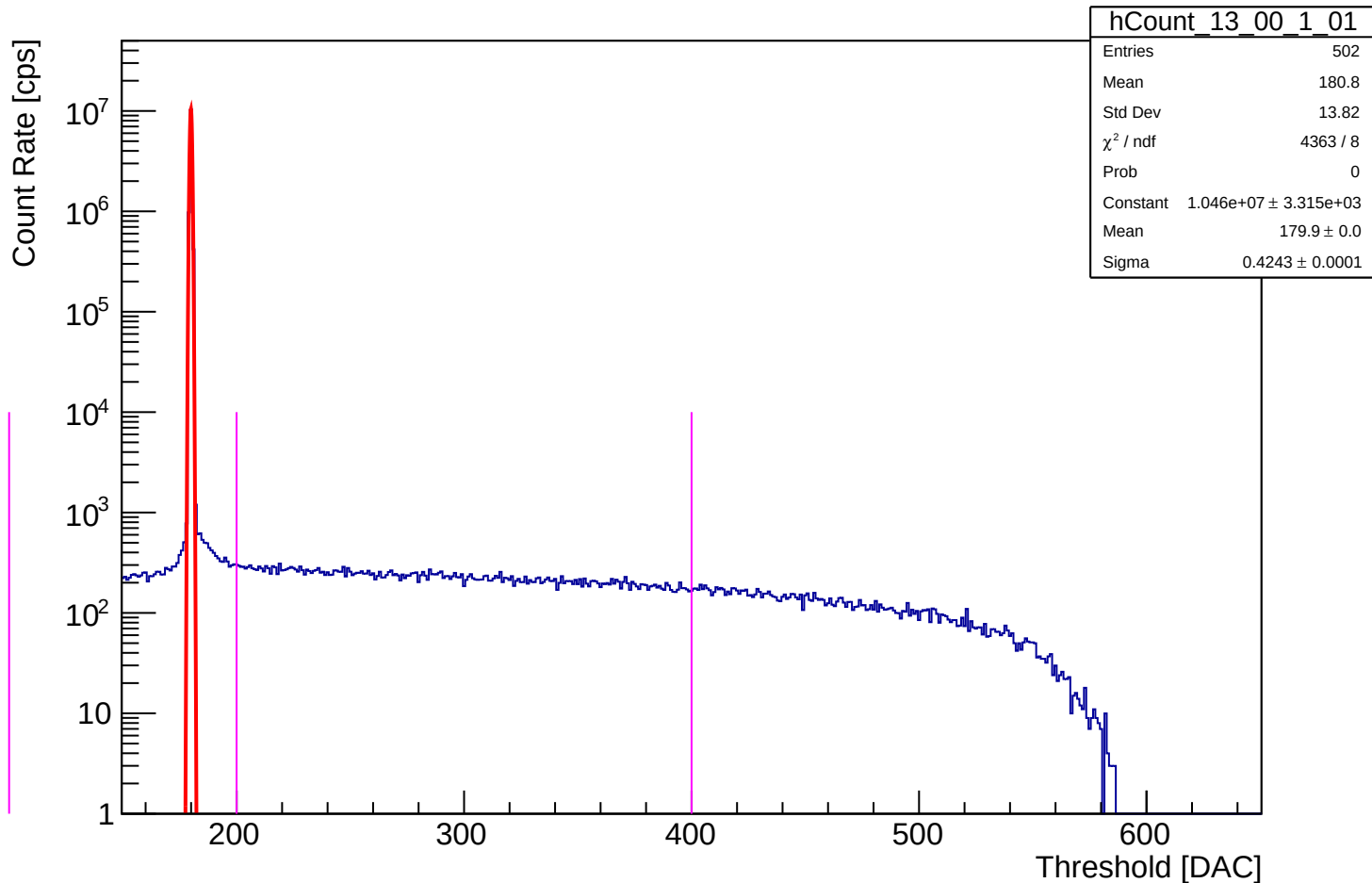


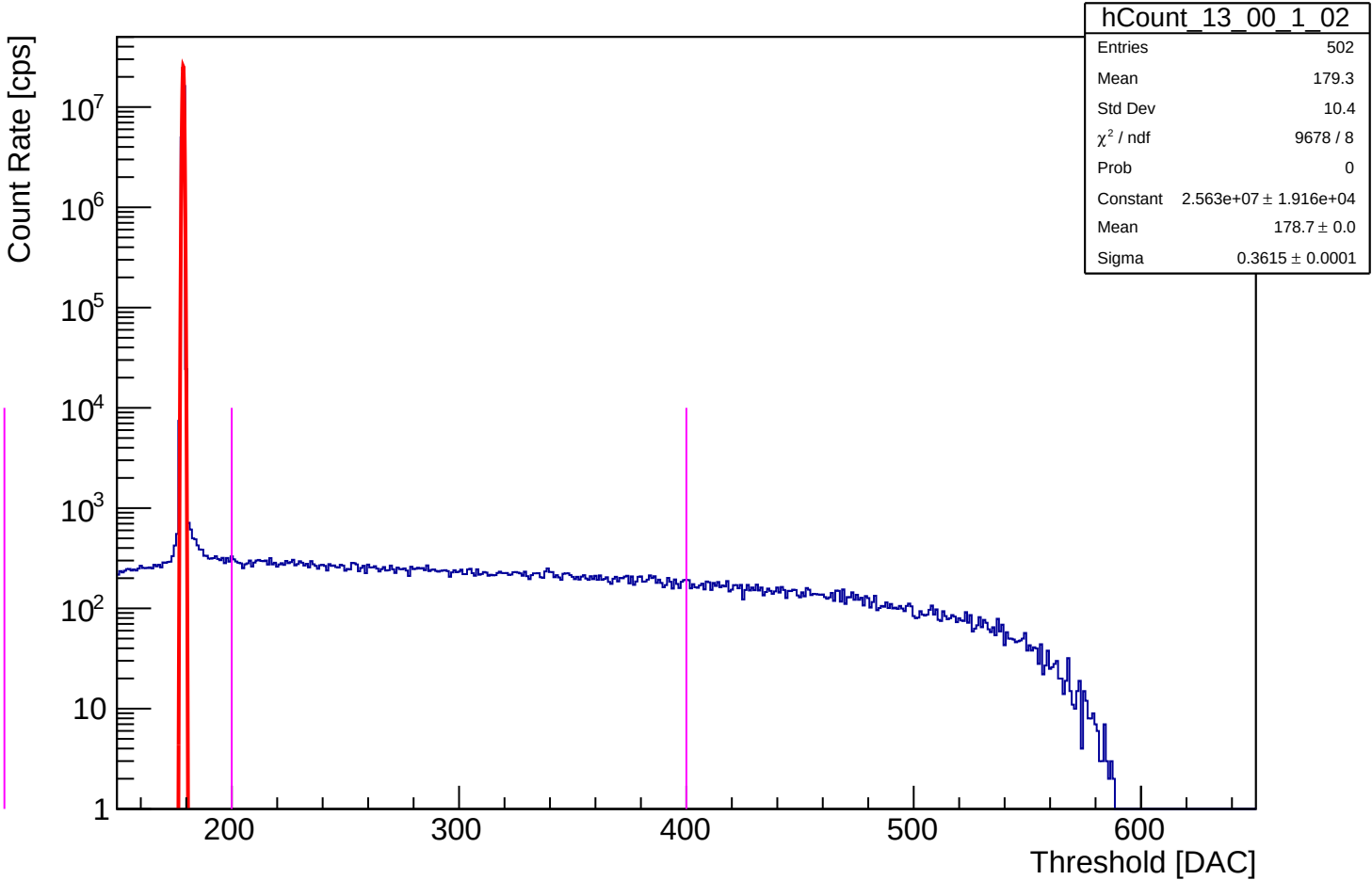
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Row 1 Tile 1 Pmt 2 Pixel 58 Slot 13 Fiber 0 Asic 1 Channel 1





Count Rate [cps]

10⁷
10⁶
10⁵
10⁴
10³
10²
10
1

200

300

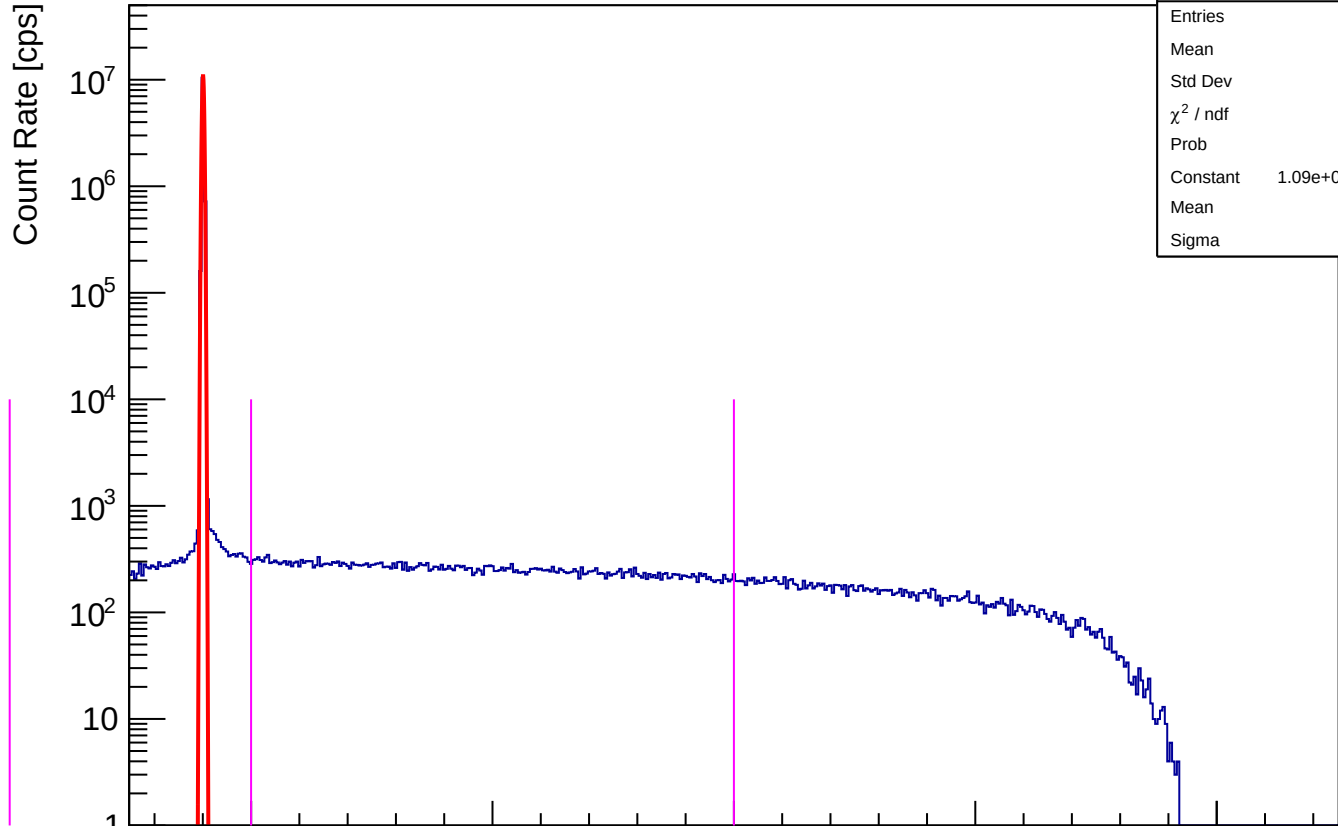
400

500

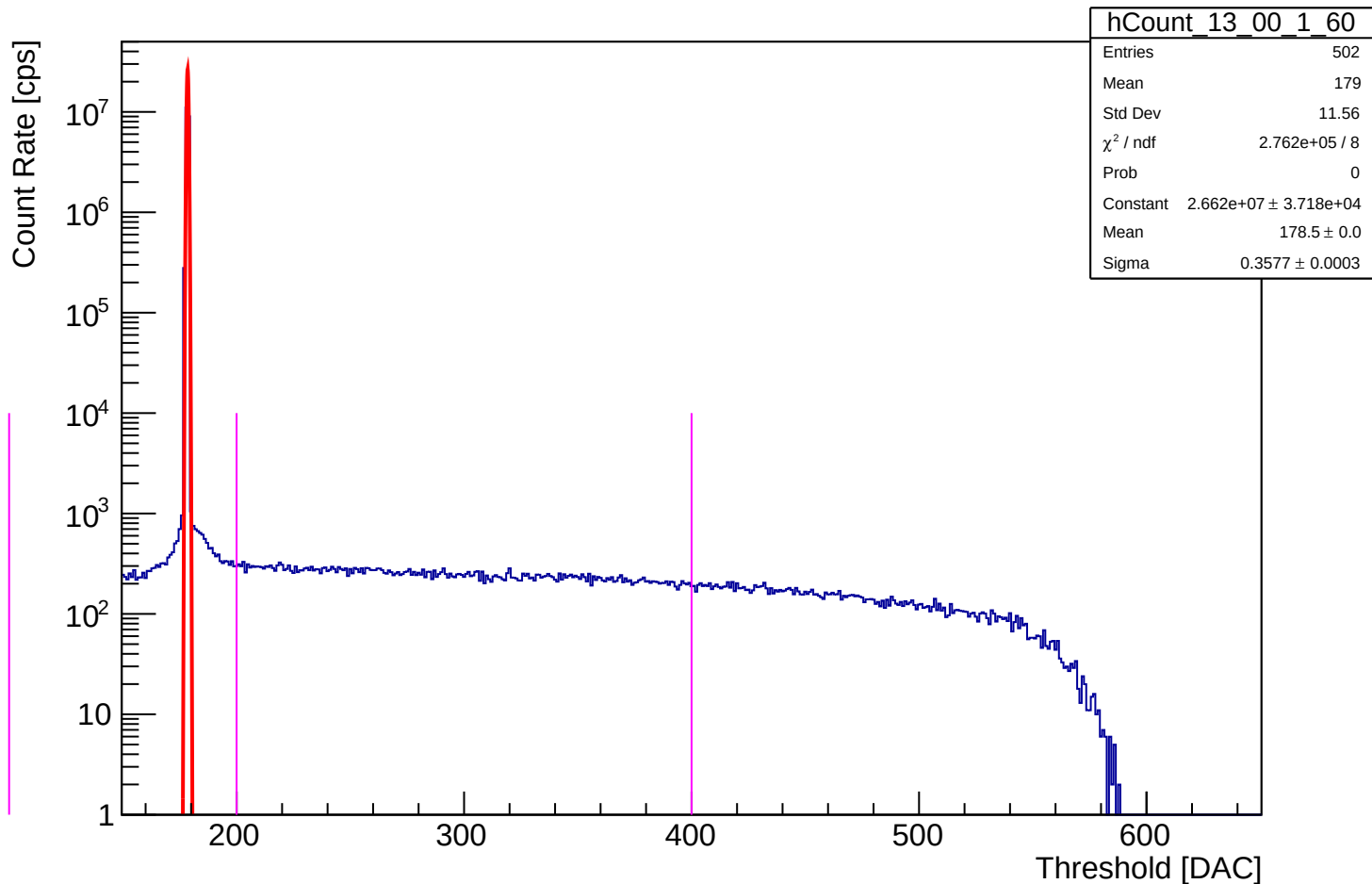
600

Threshold [DAC]

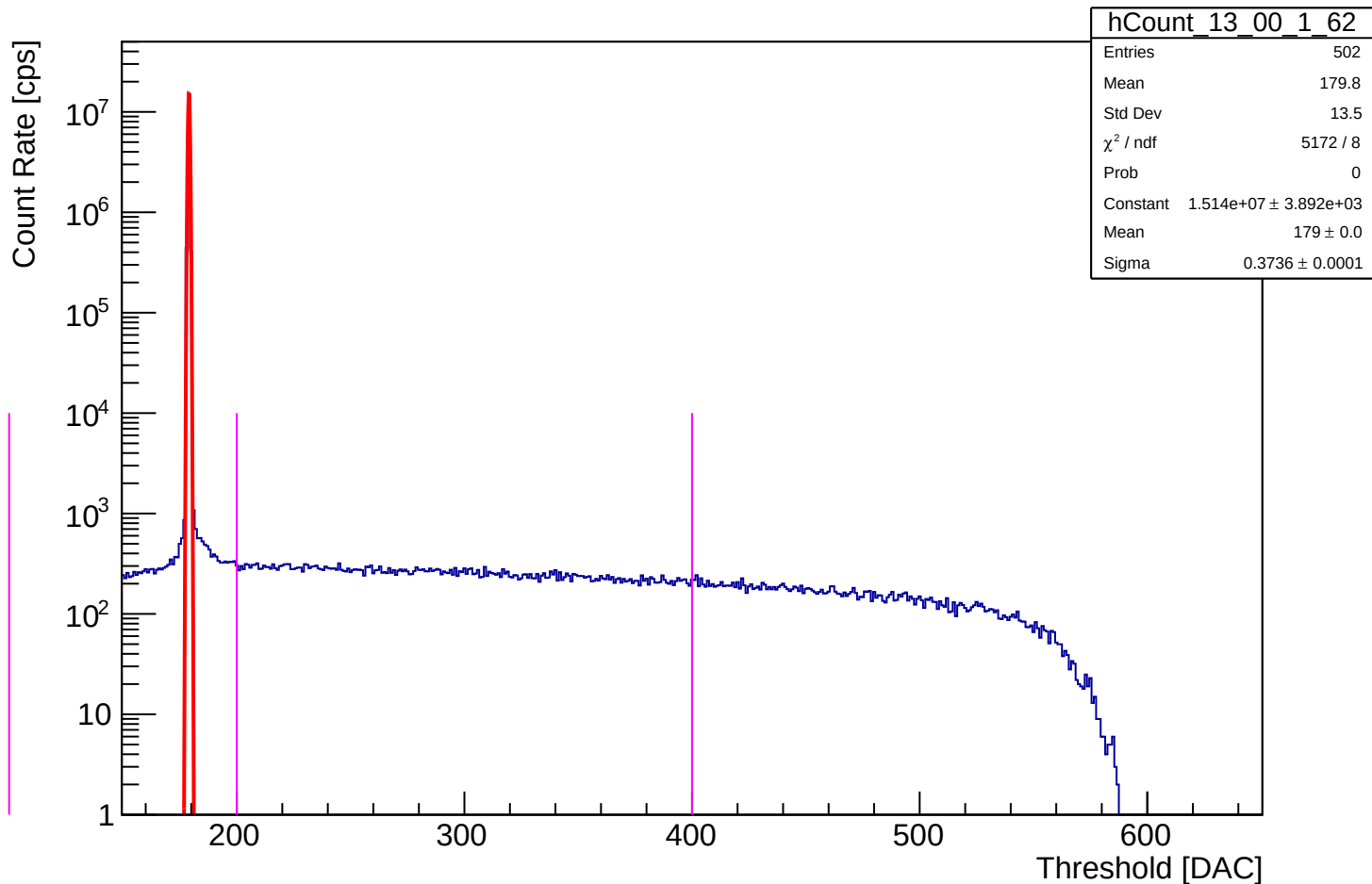
hCount_13_00_1_00	
Entries	502
Mean	181.1
Std Dev	15.48
χ^2 / ndf	4556 / 8
Prob	0
Constant	$1.09\text{e}+07 \pm 3.67\text{e}+03$
Mean	180.1 ± 0.0
Sigma	0.382 ± 0.000

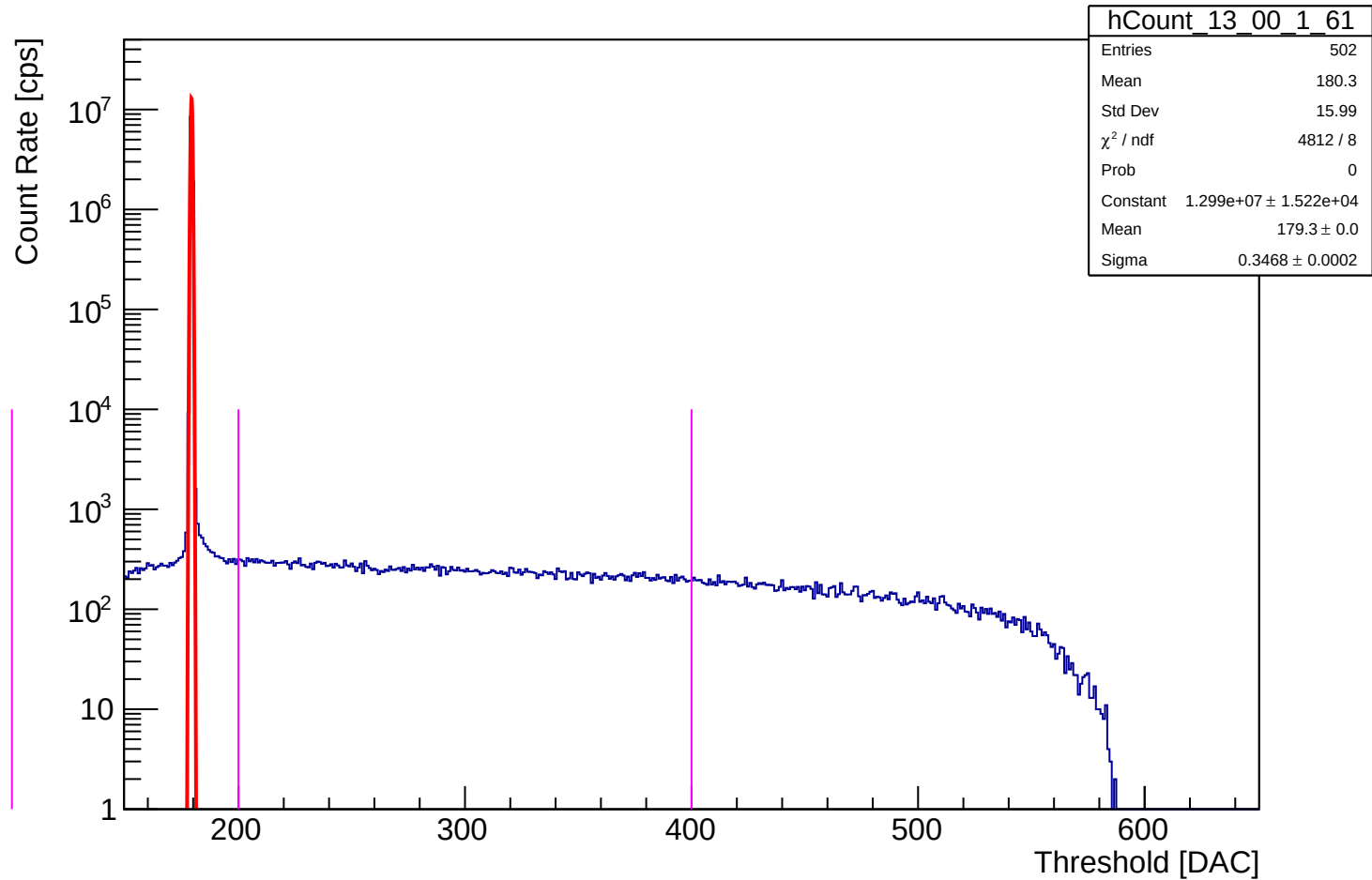


Row 1 Tile 1 Pmt 2 Pixel 61 Slot 13 Fiber 0 Asic 1 Channel 60

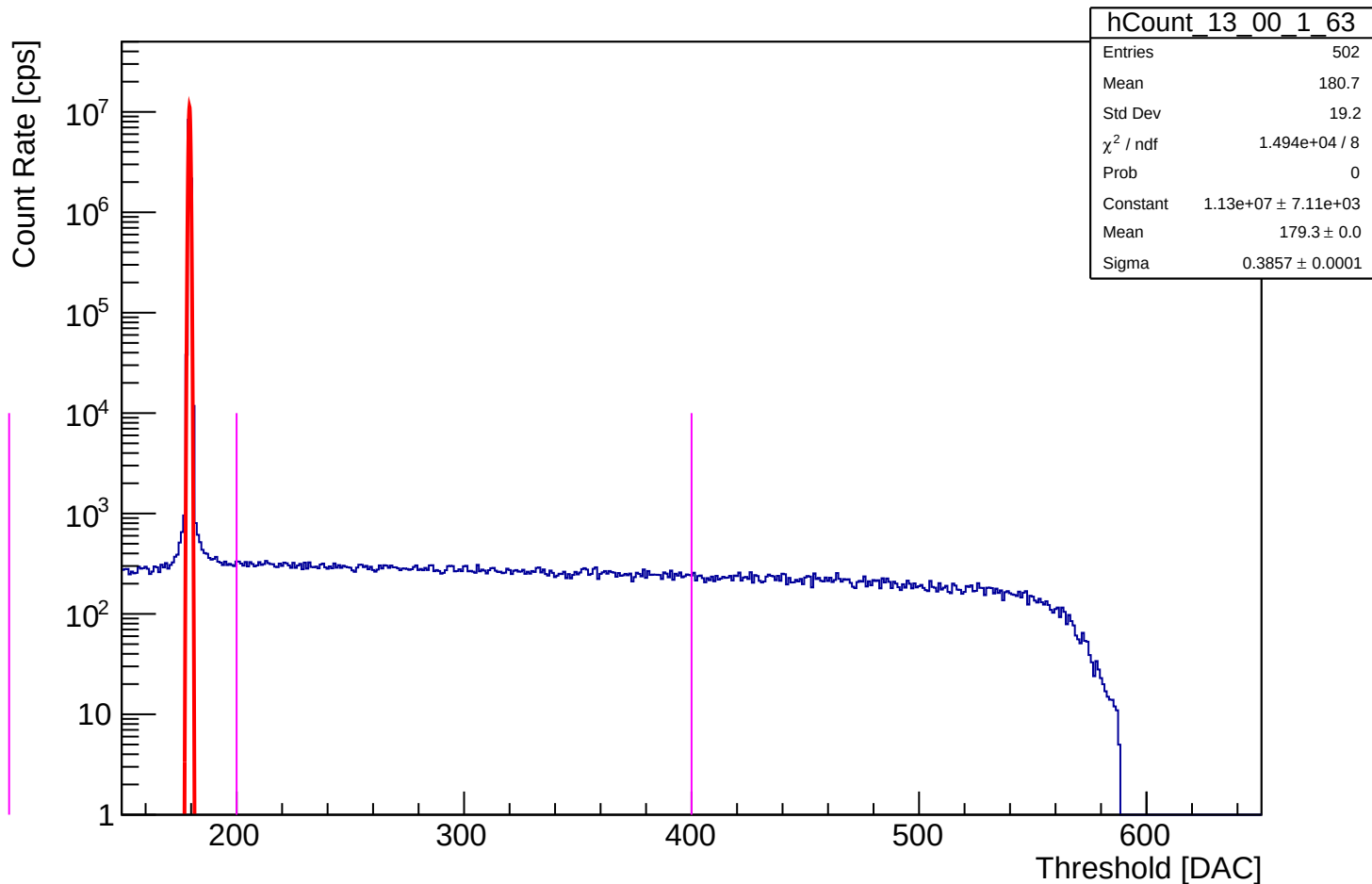


Row 1 Tile 1 Pmt 2 Pixel 62 Slot 13 Fiber 0 Asic 1 Channel 62

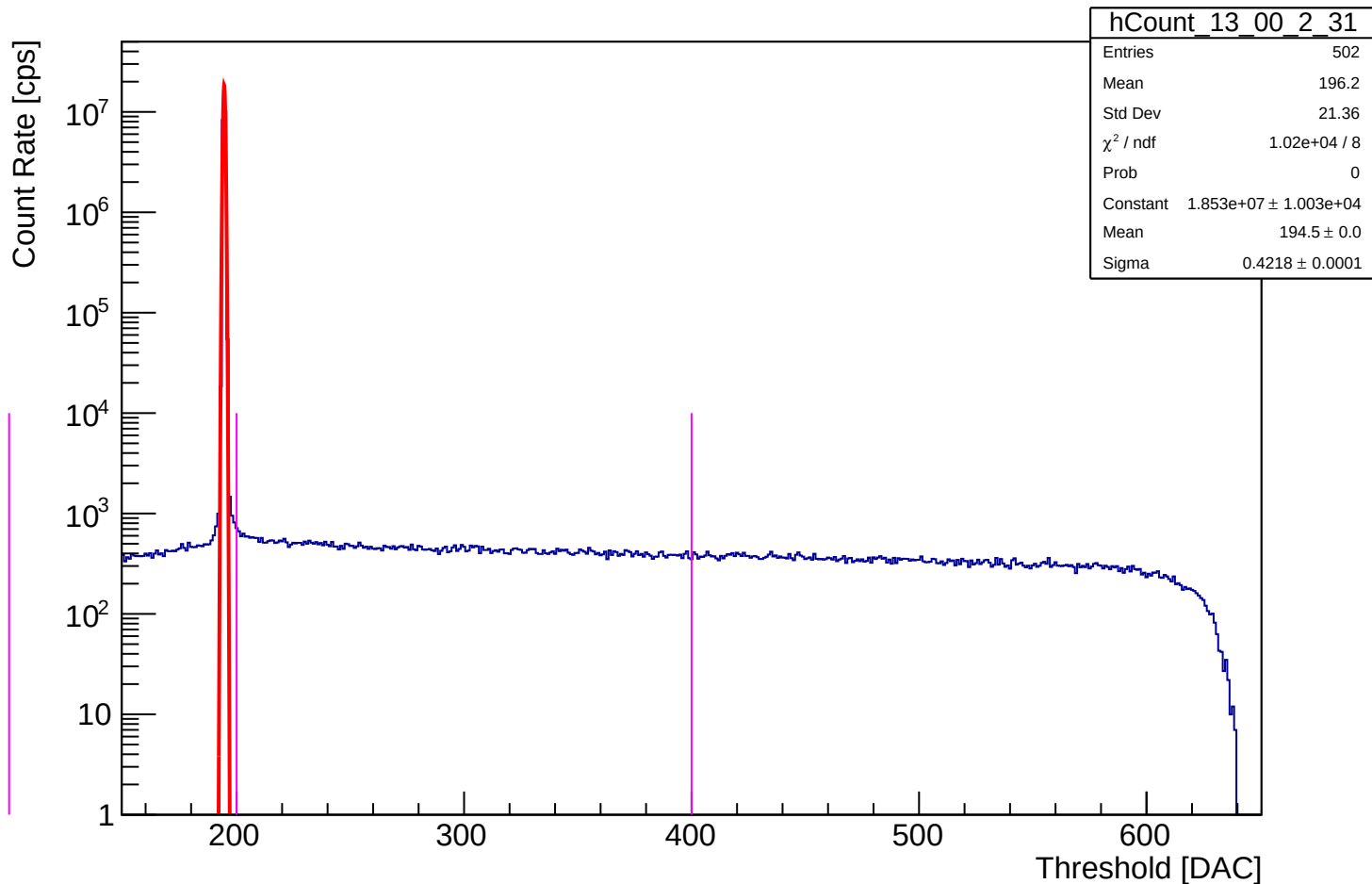




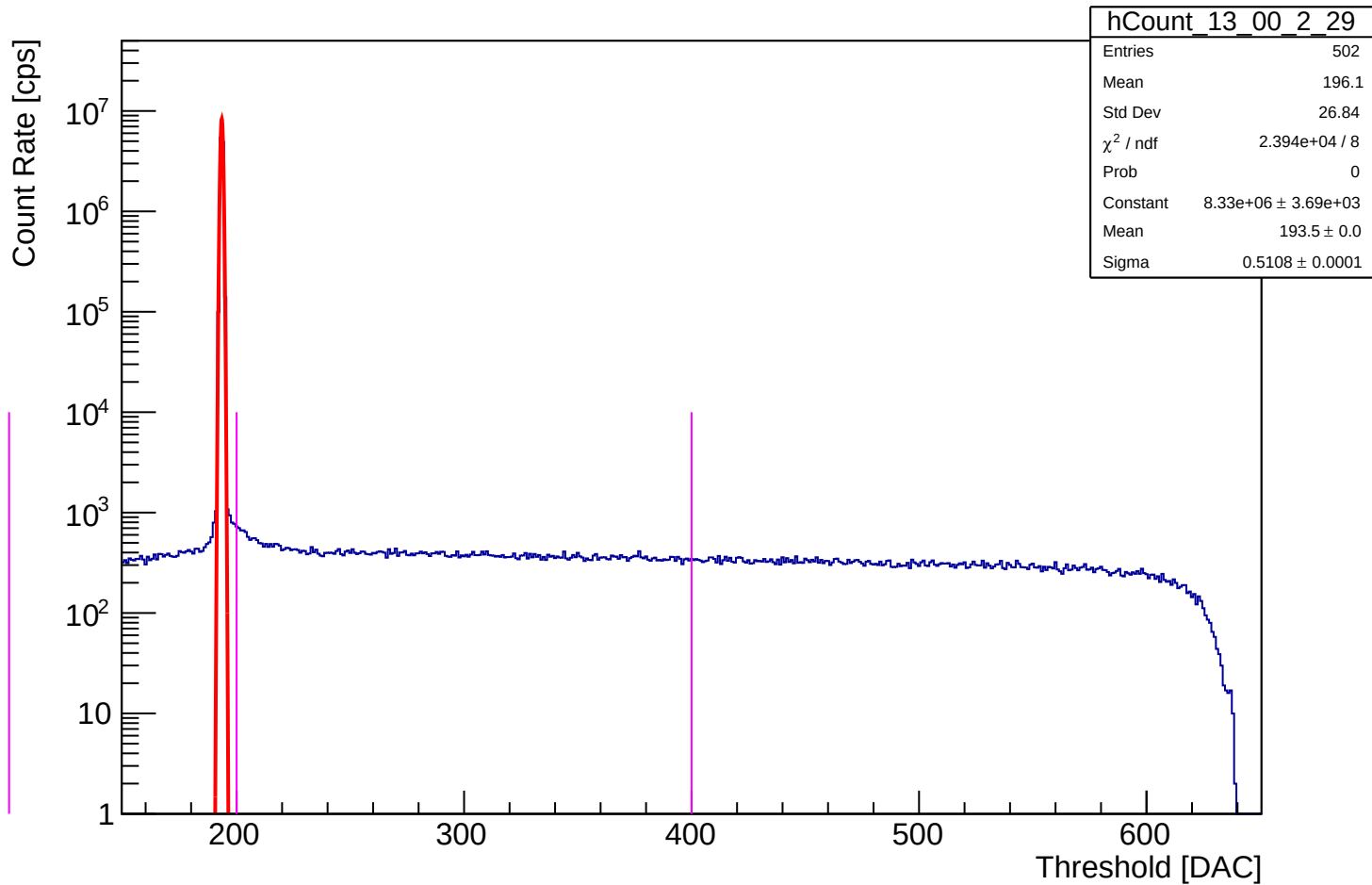
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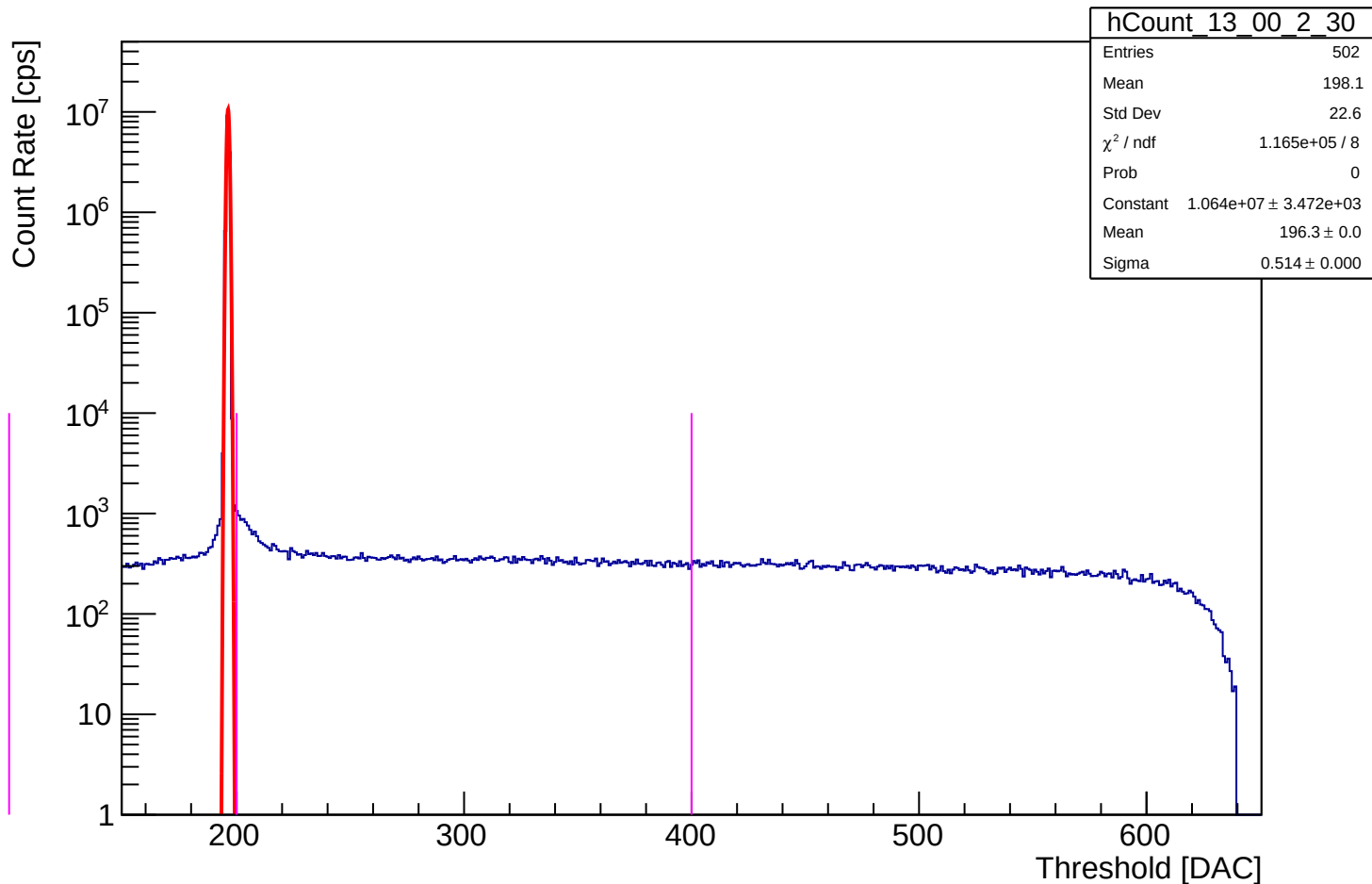
Row 1 Tile 1 Pmt 3 Pixel 1 Slot 13 Fiber 0 Asic 2 Channel 31



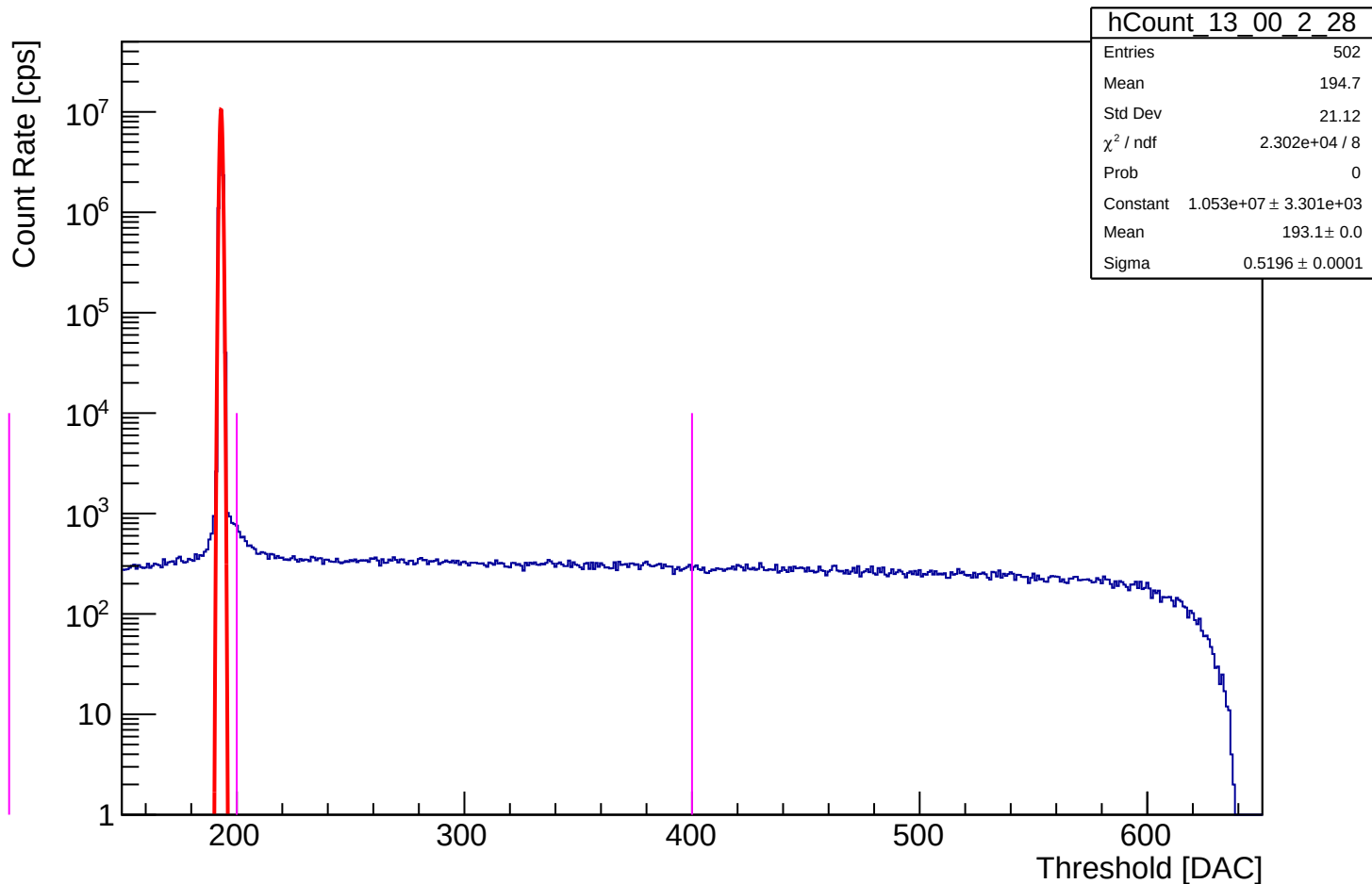
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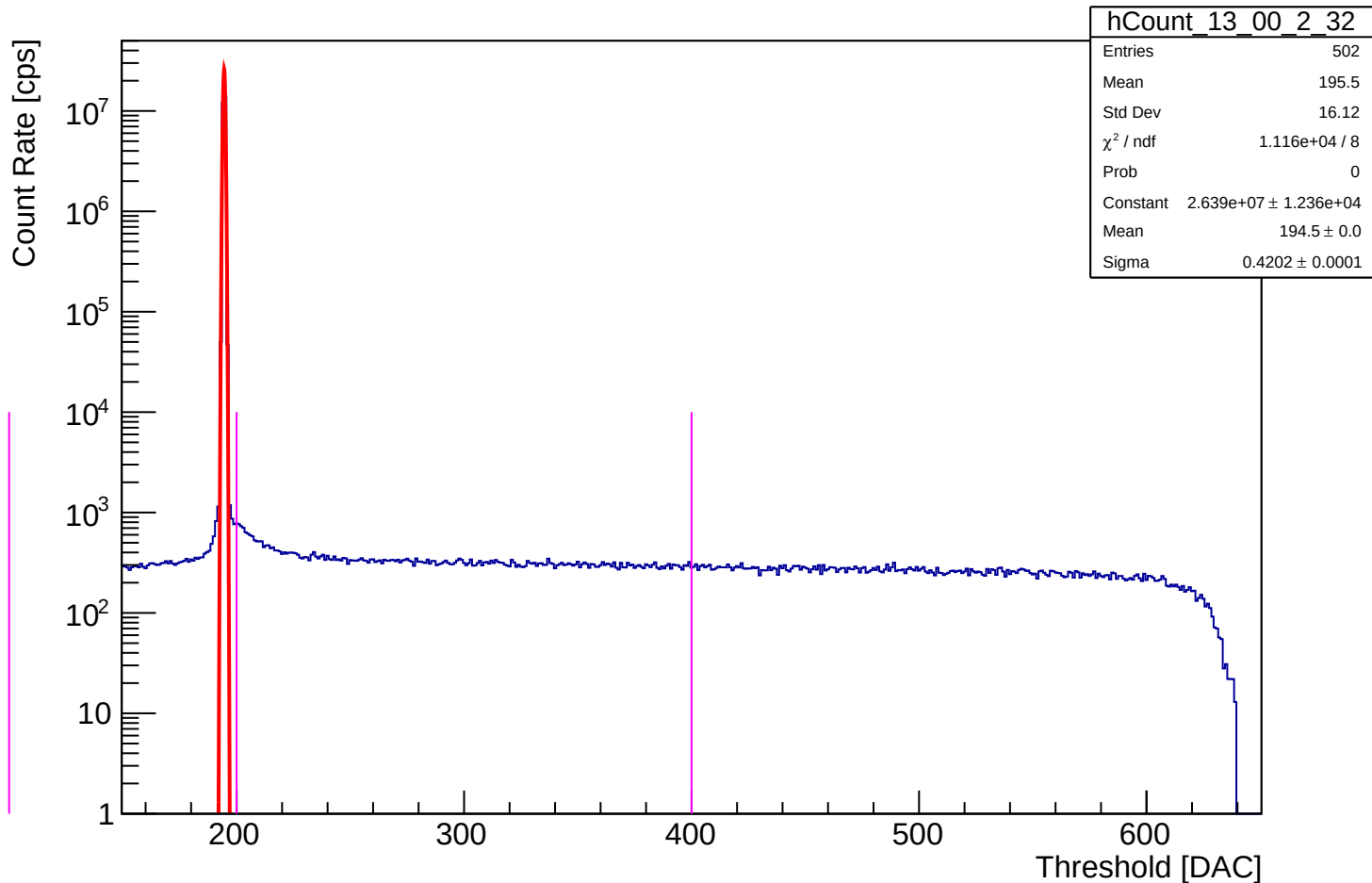
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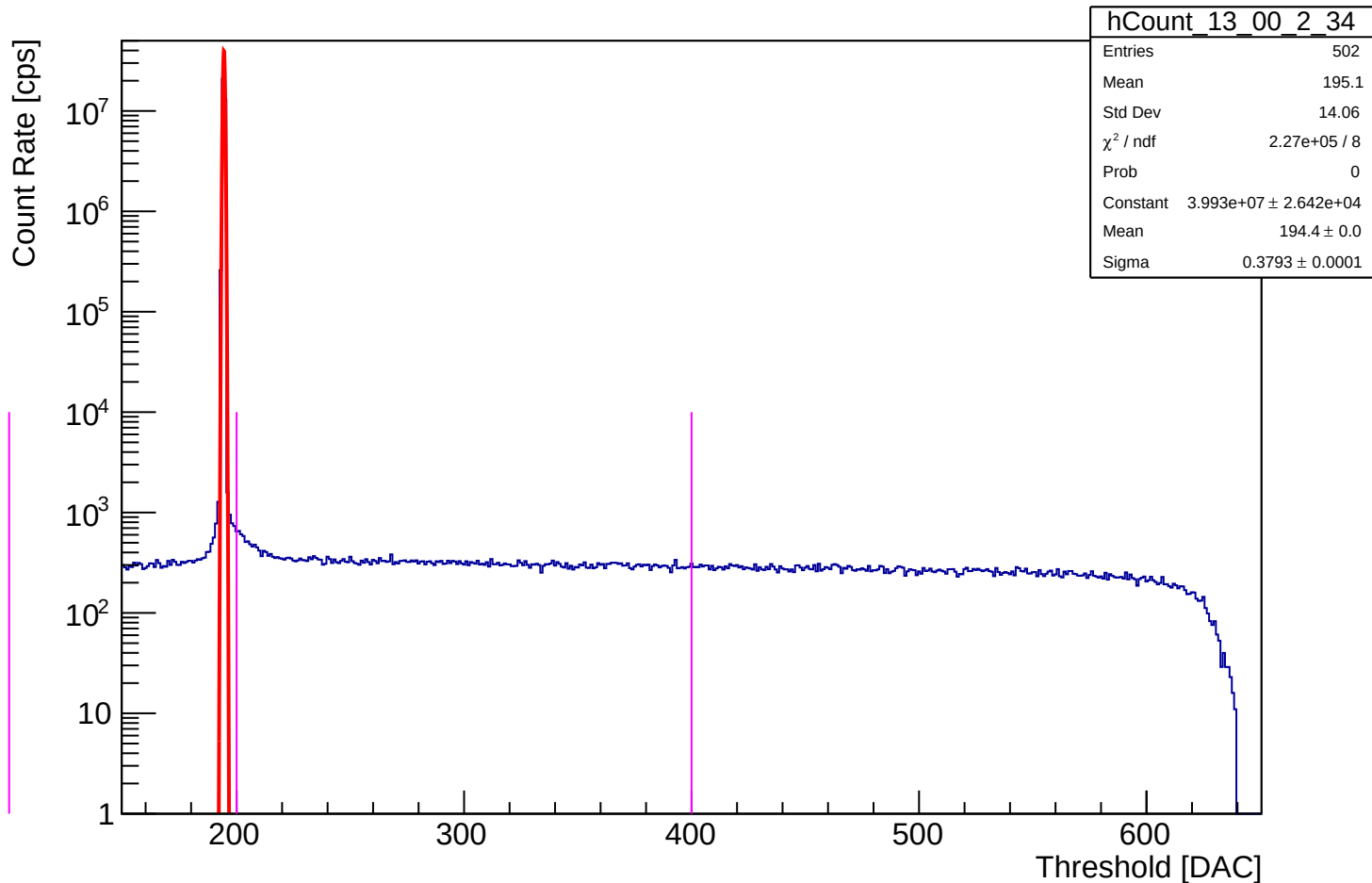
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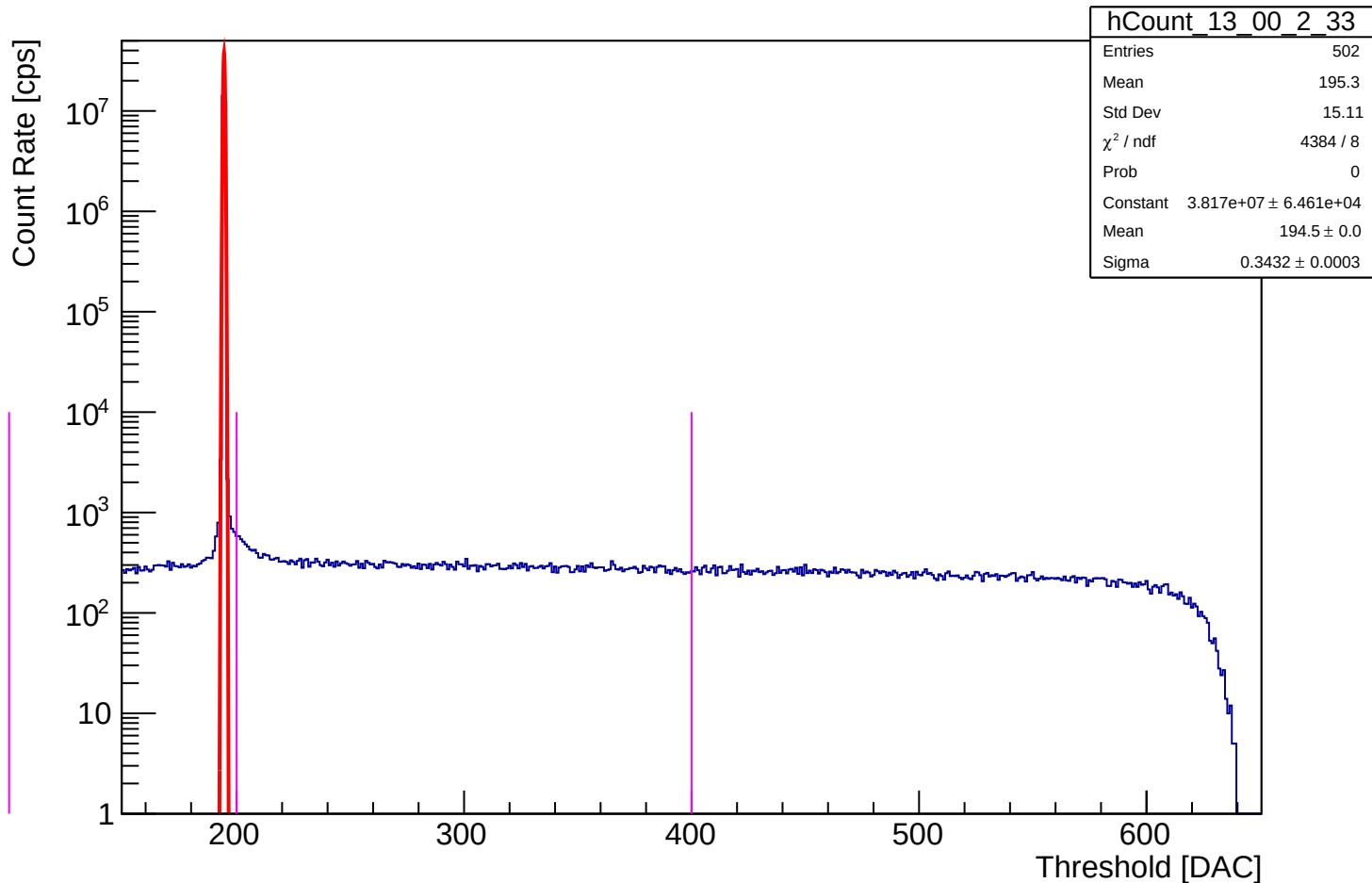
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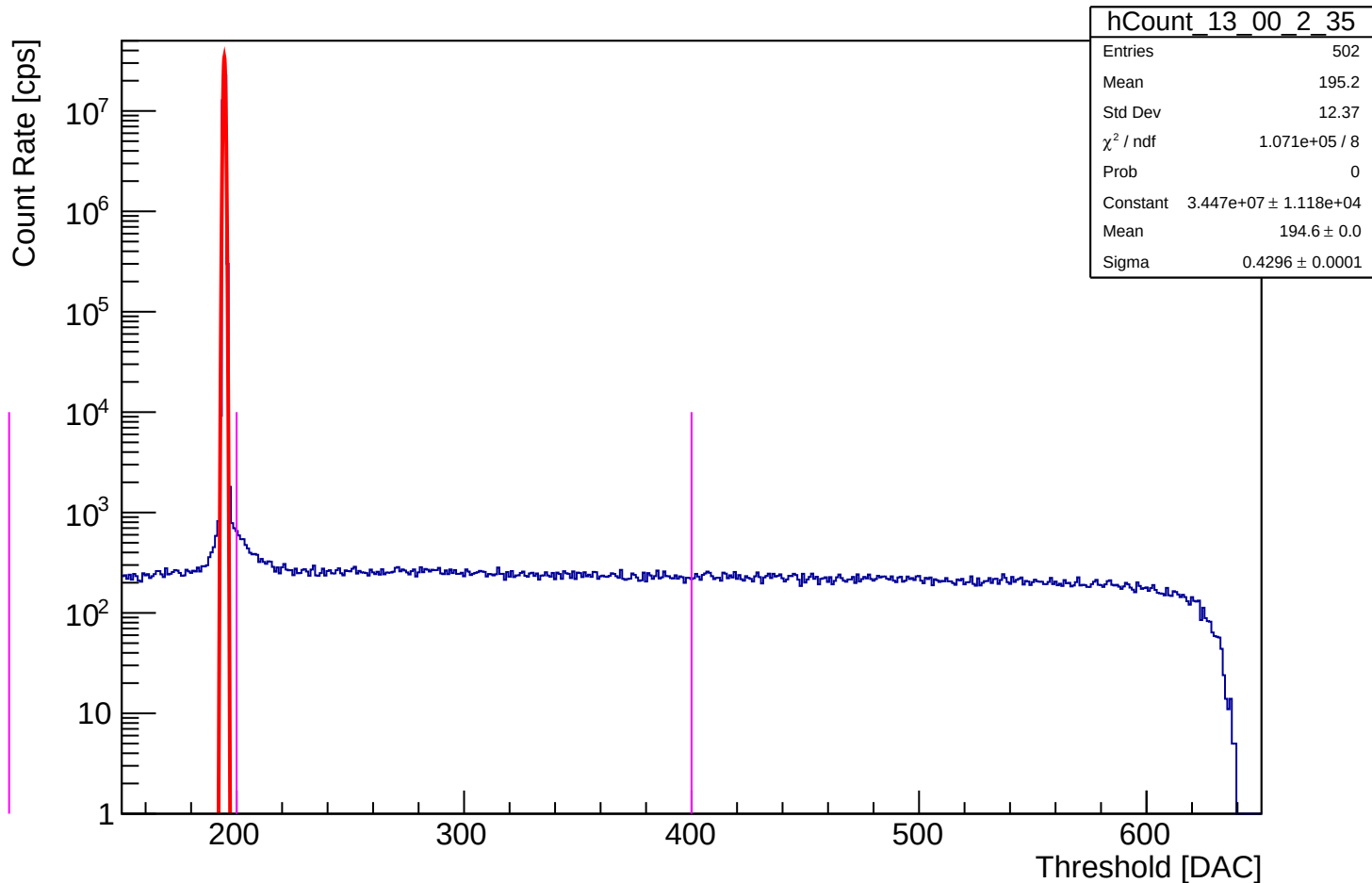
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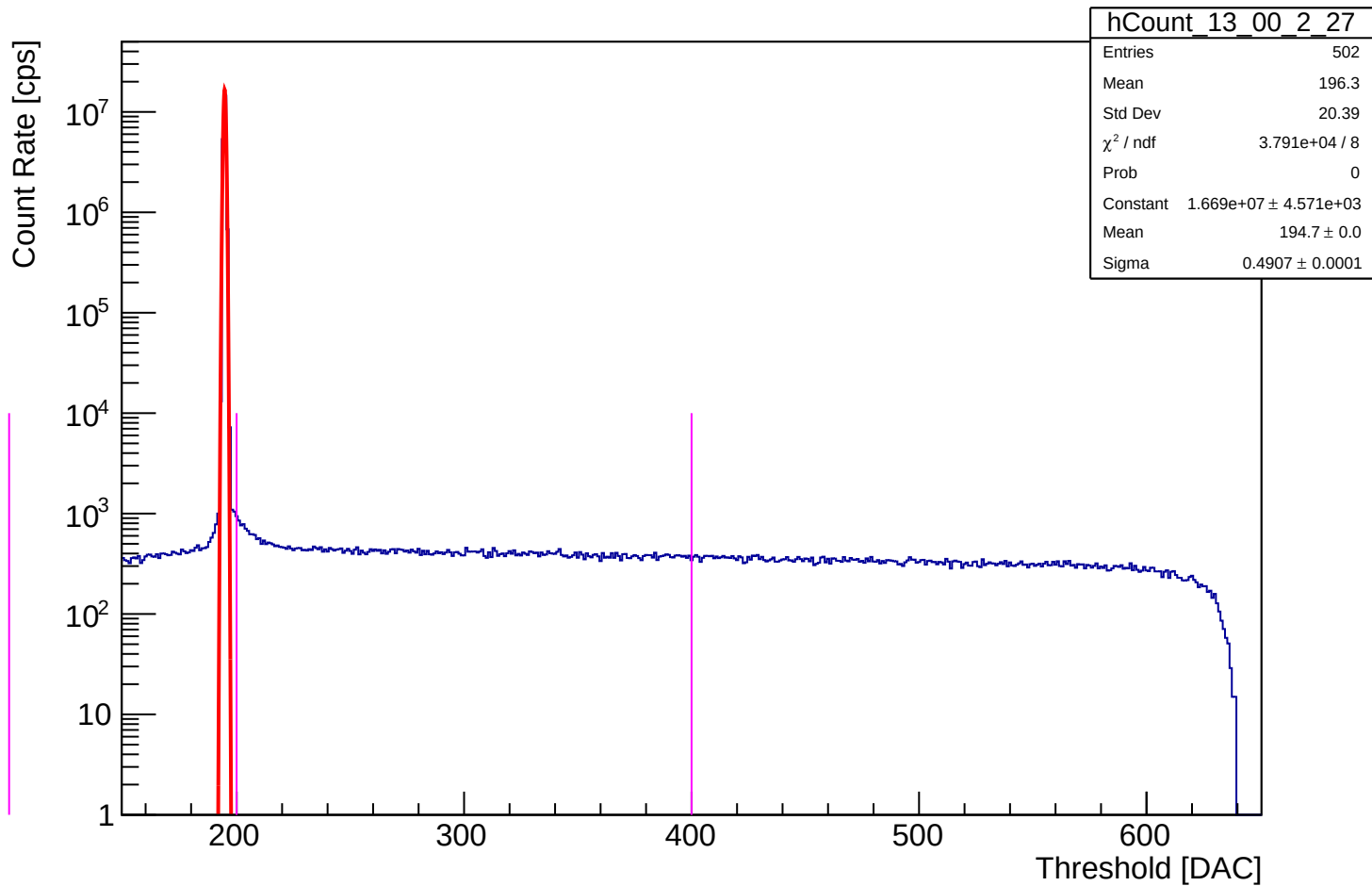
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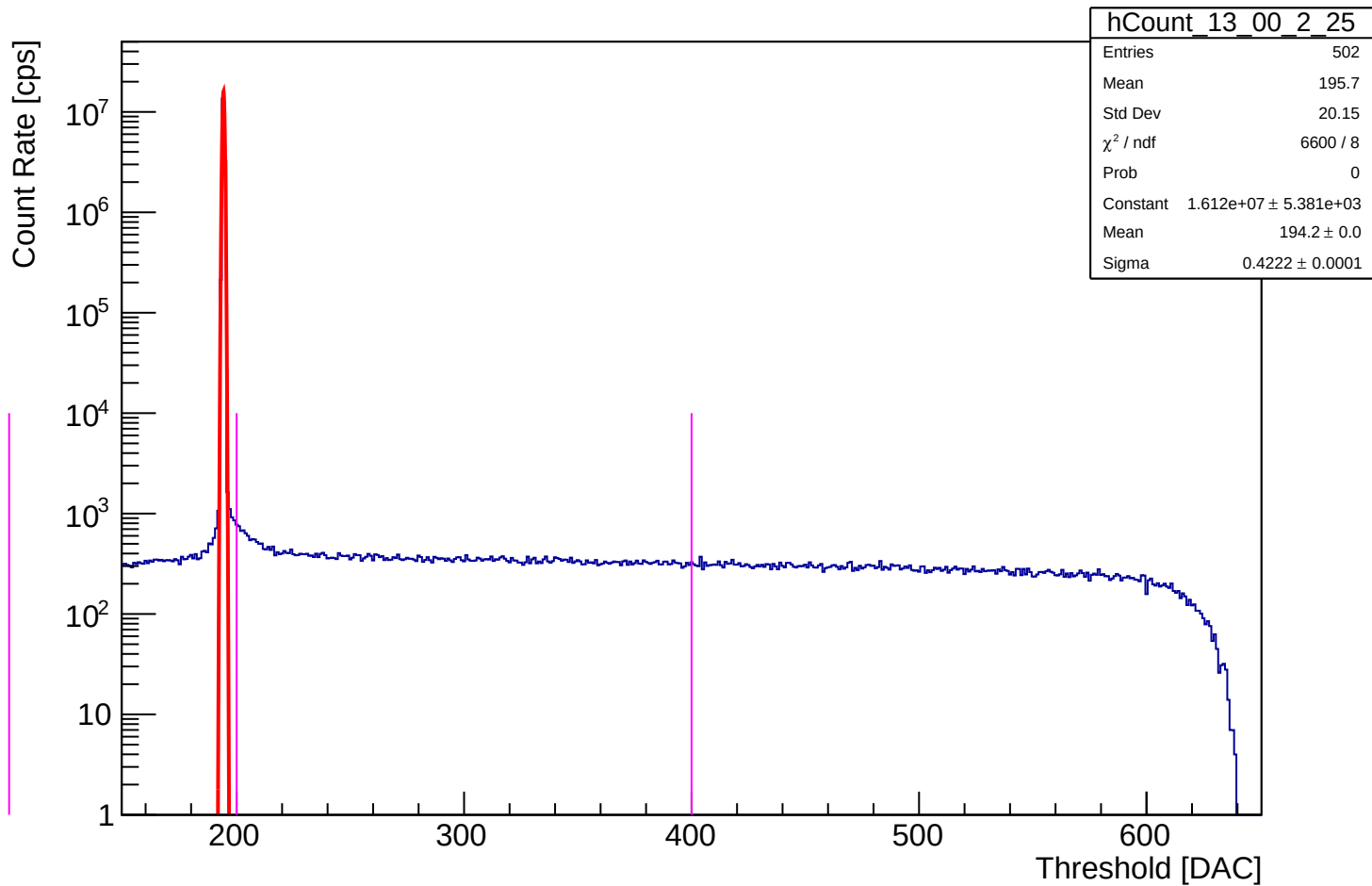
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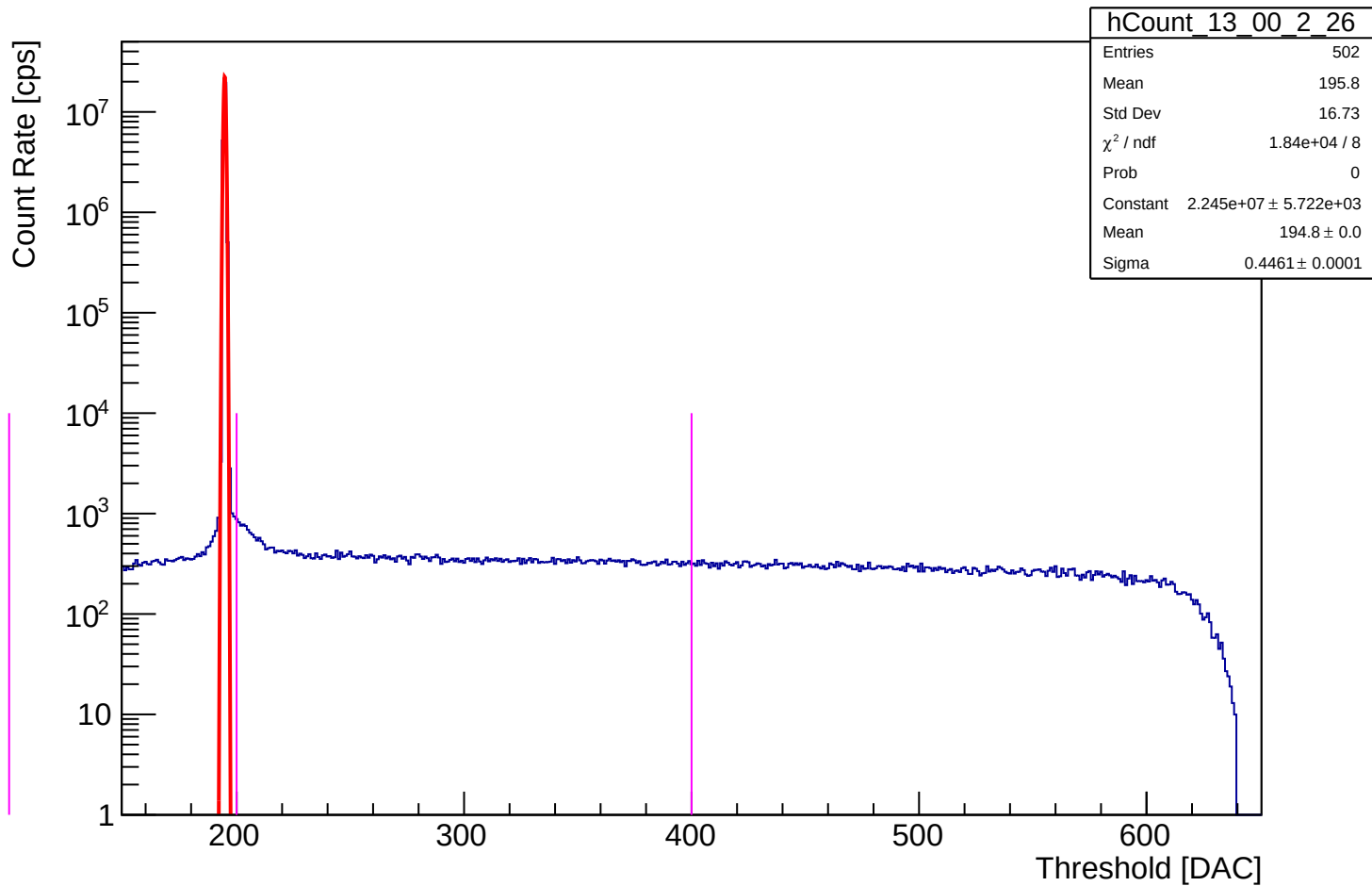
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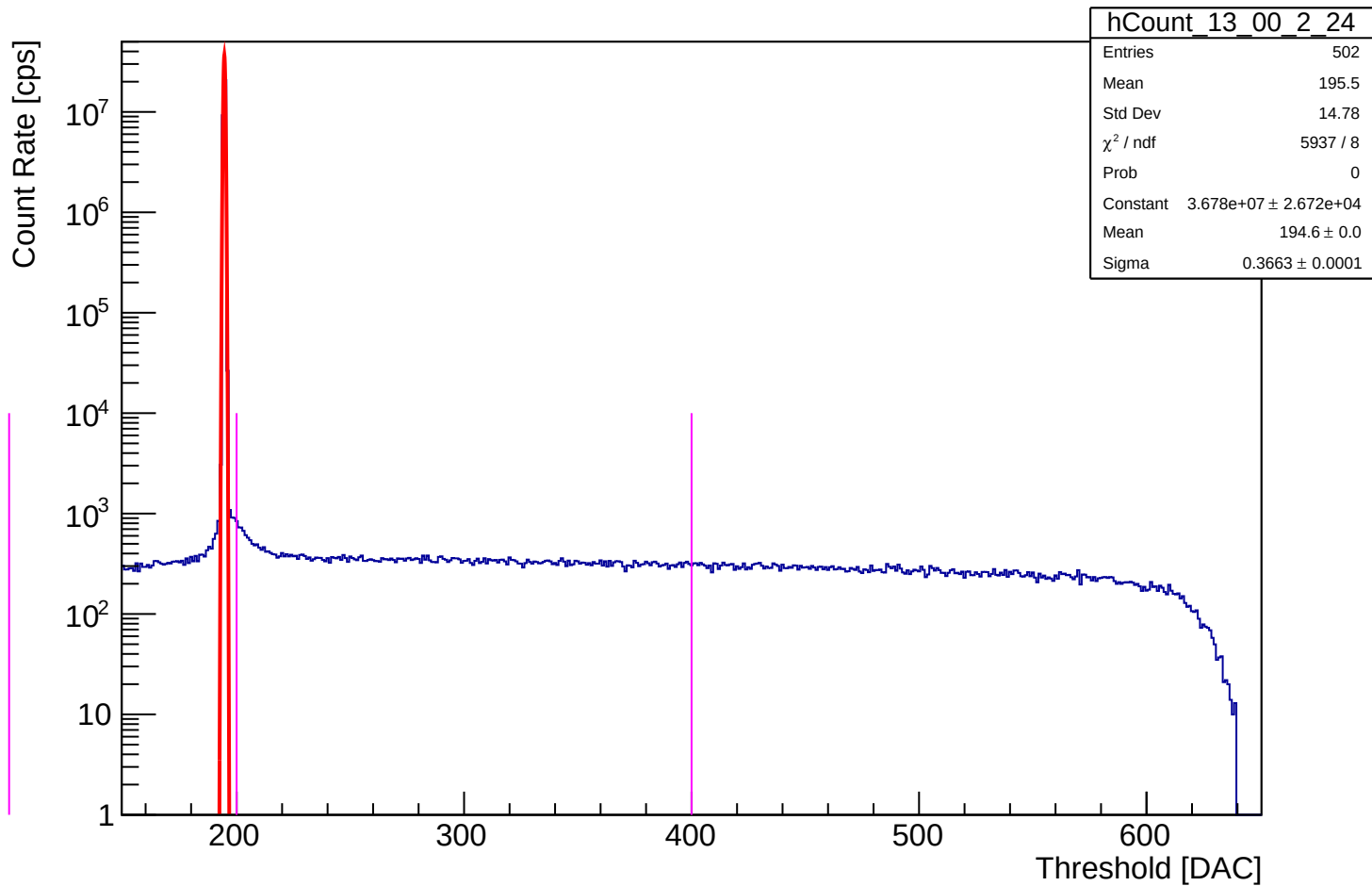
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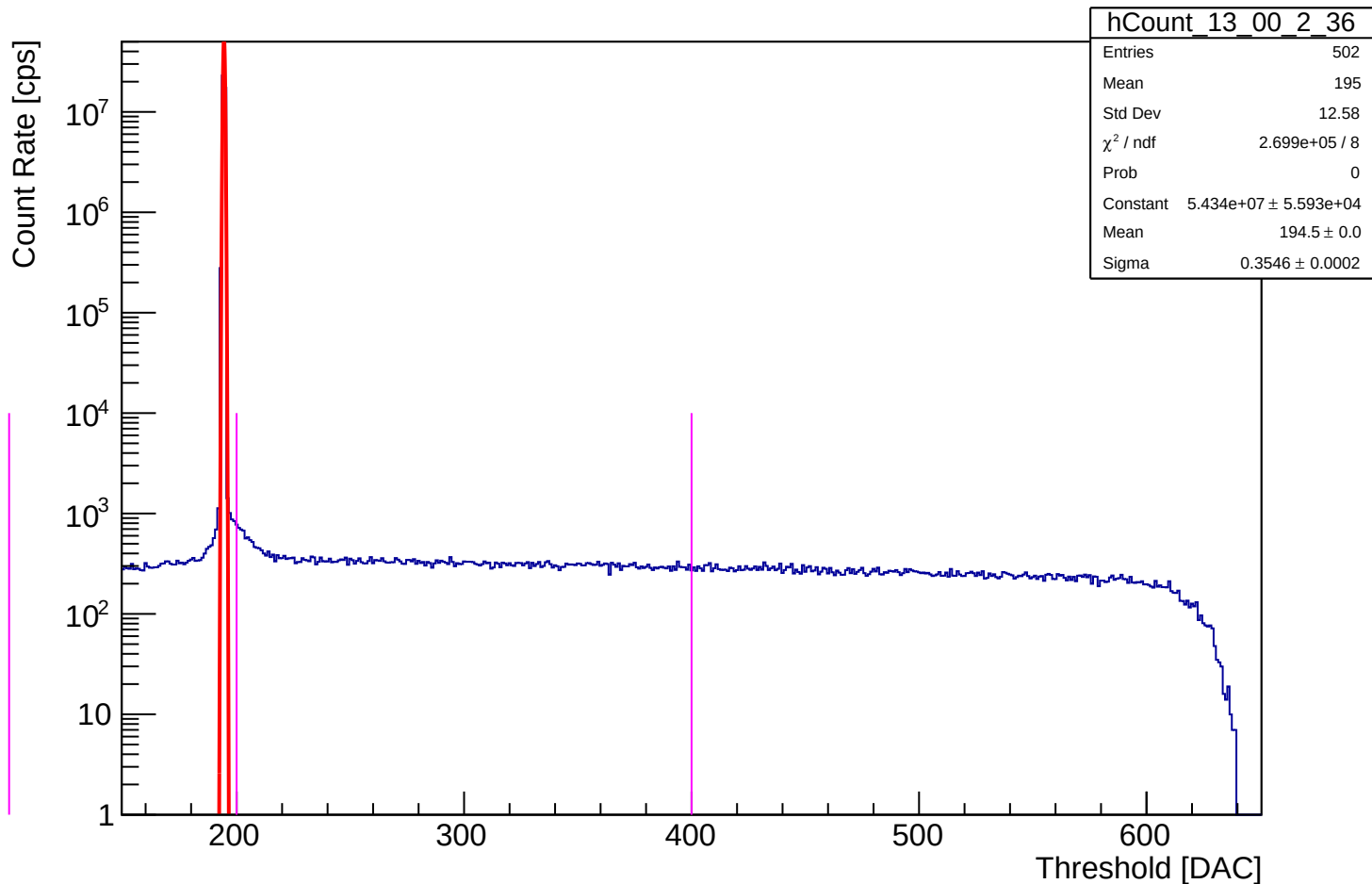
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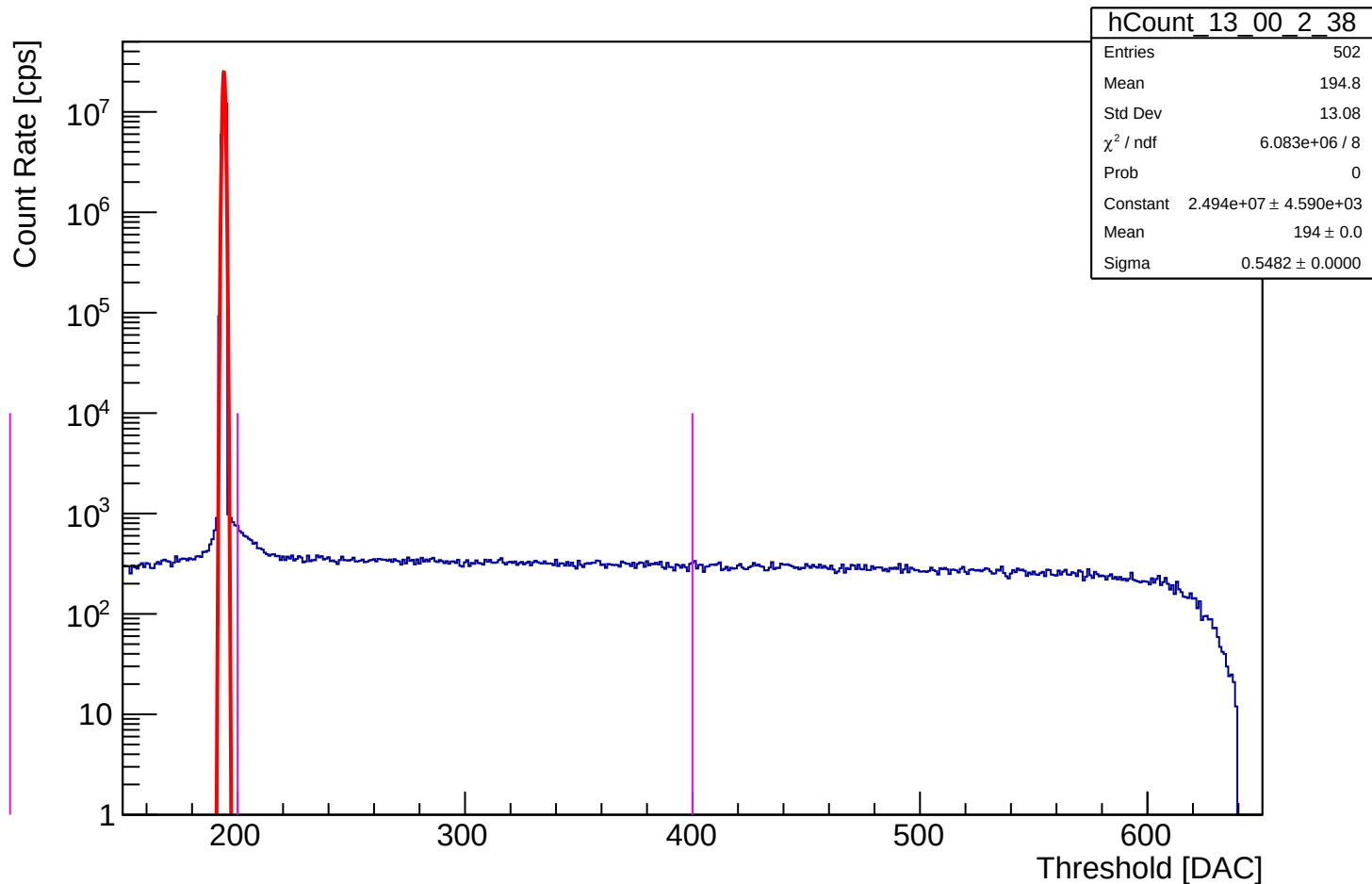
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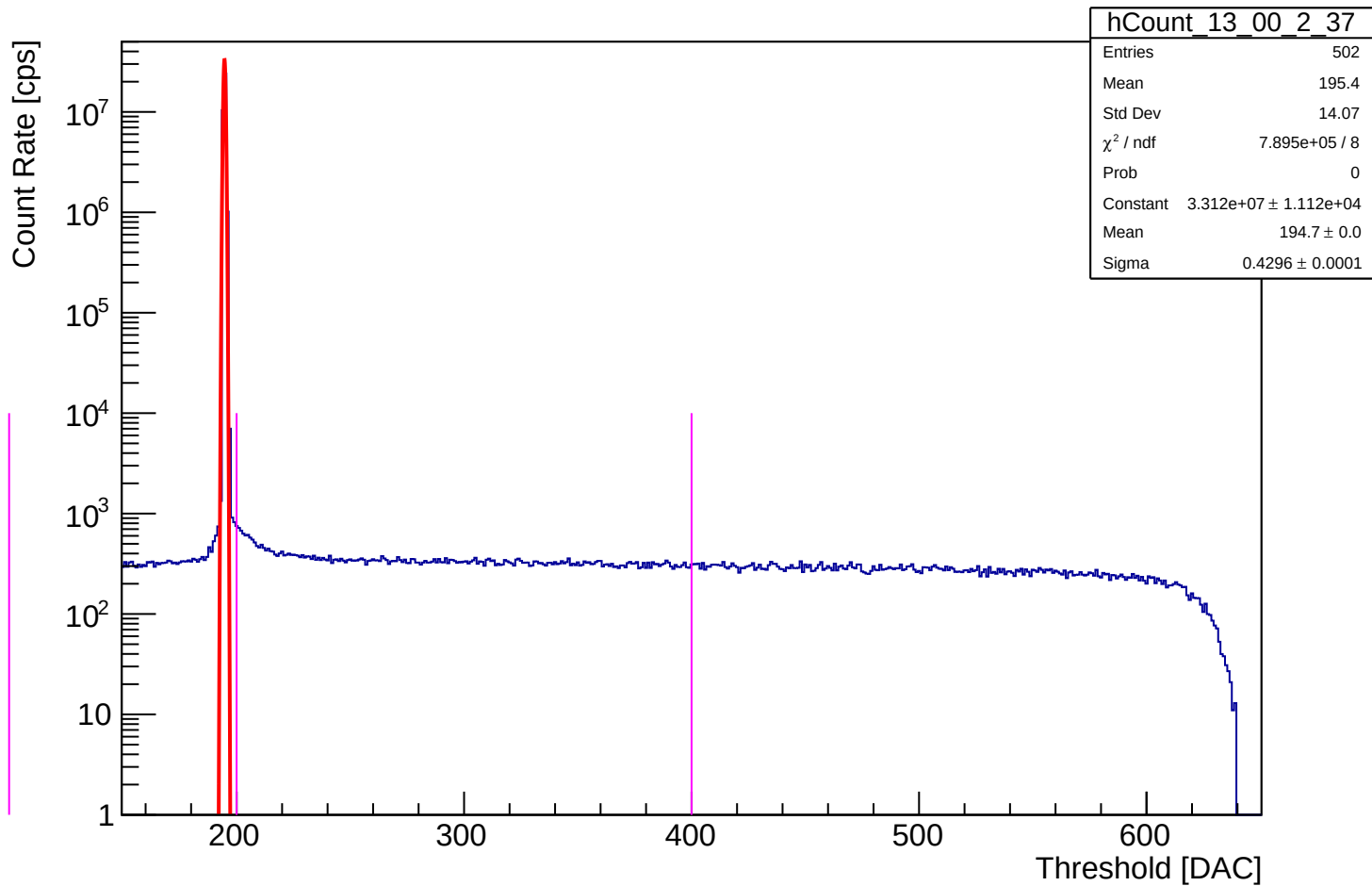
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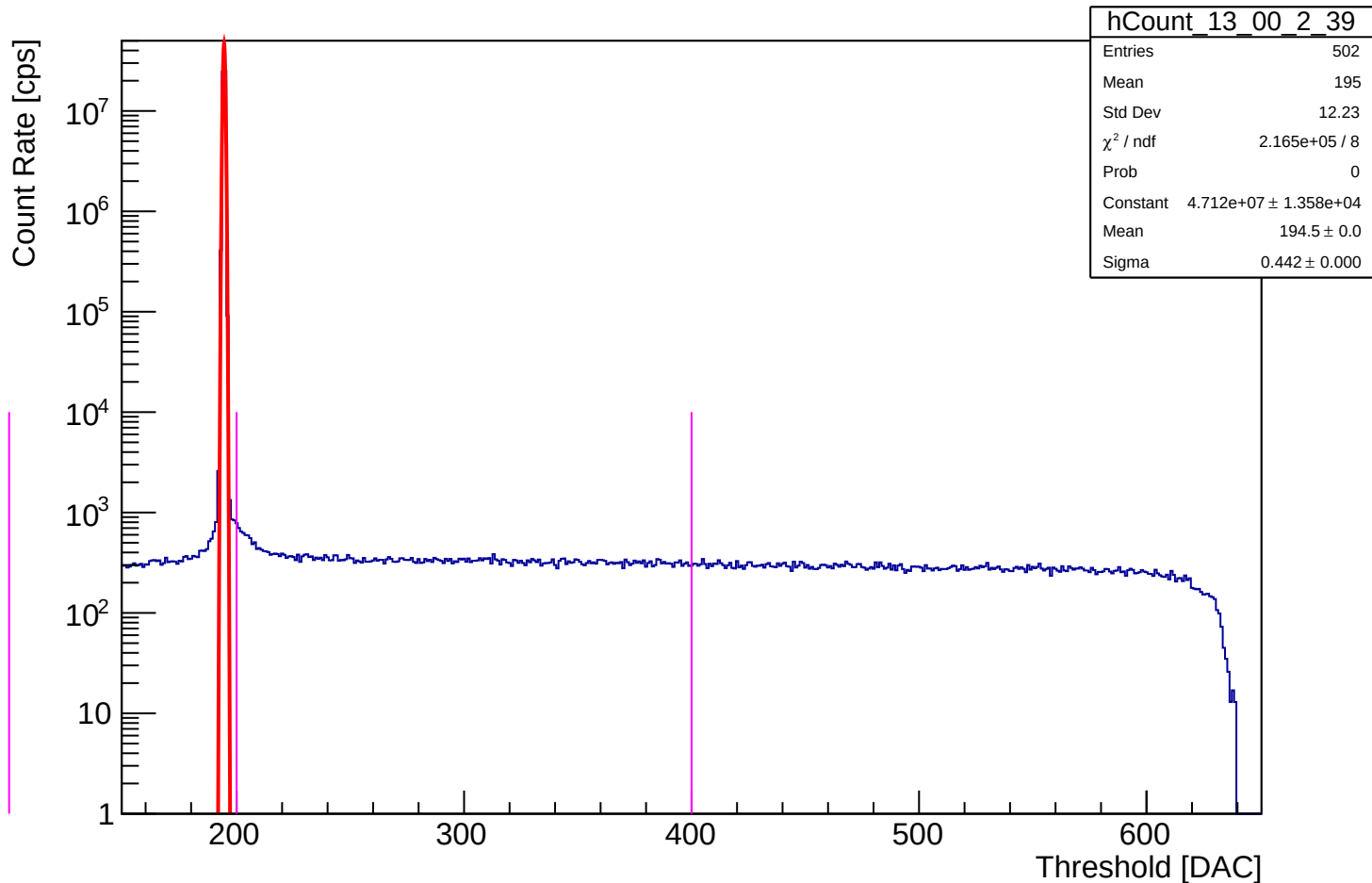
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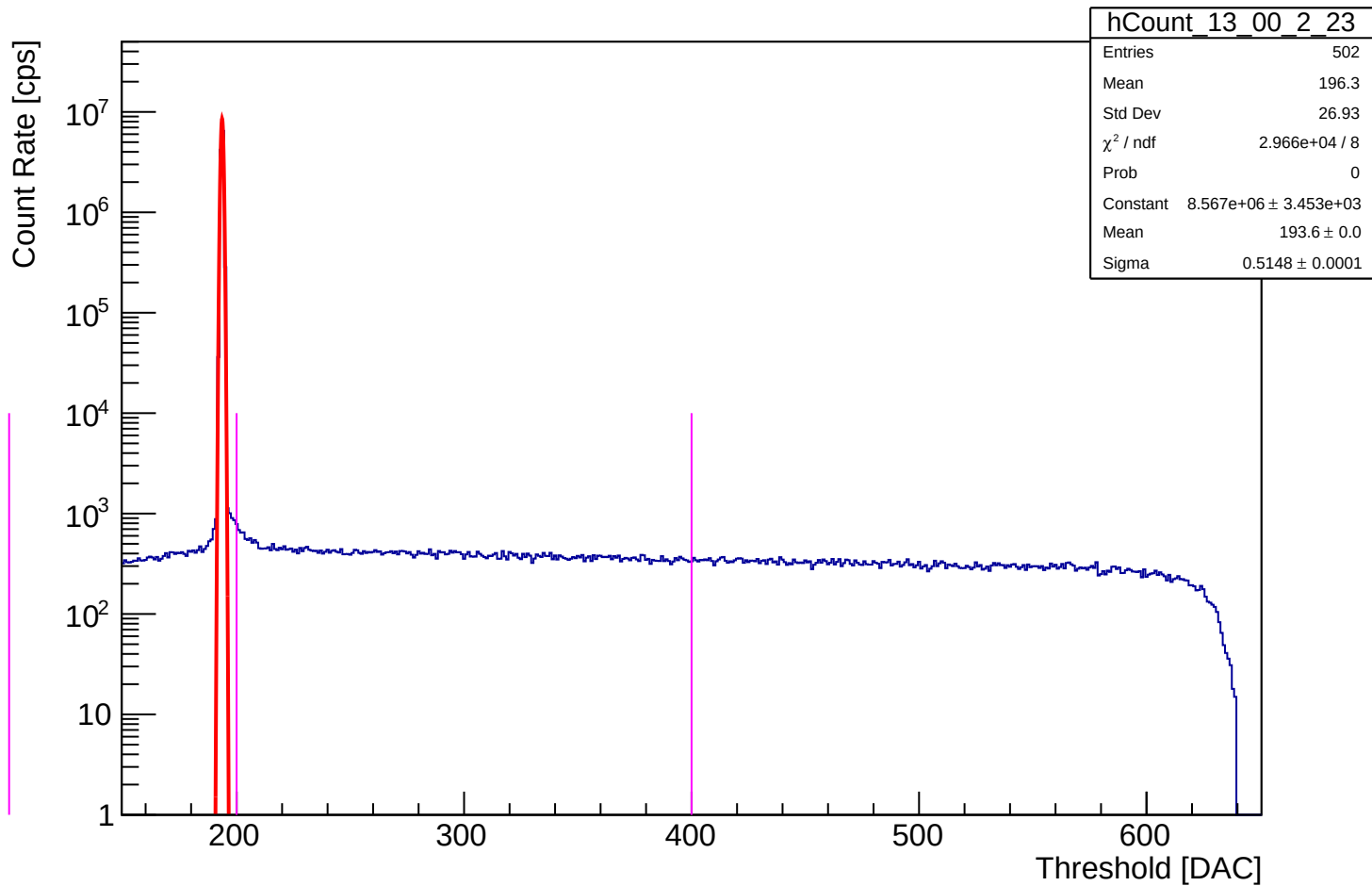
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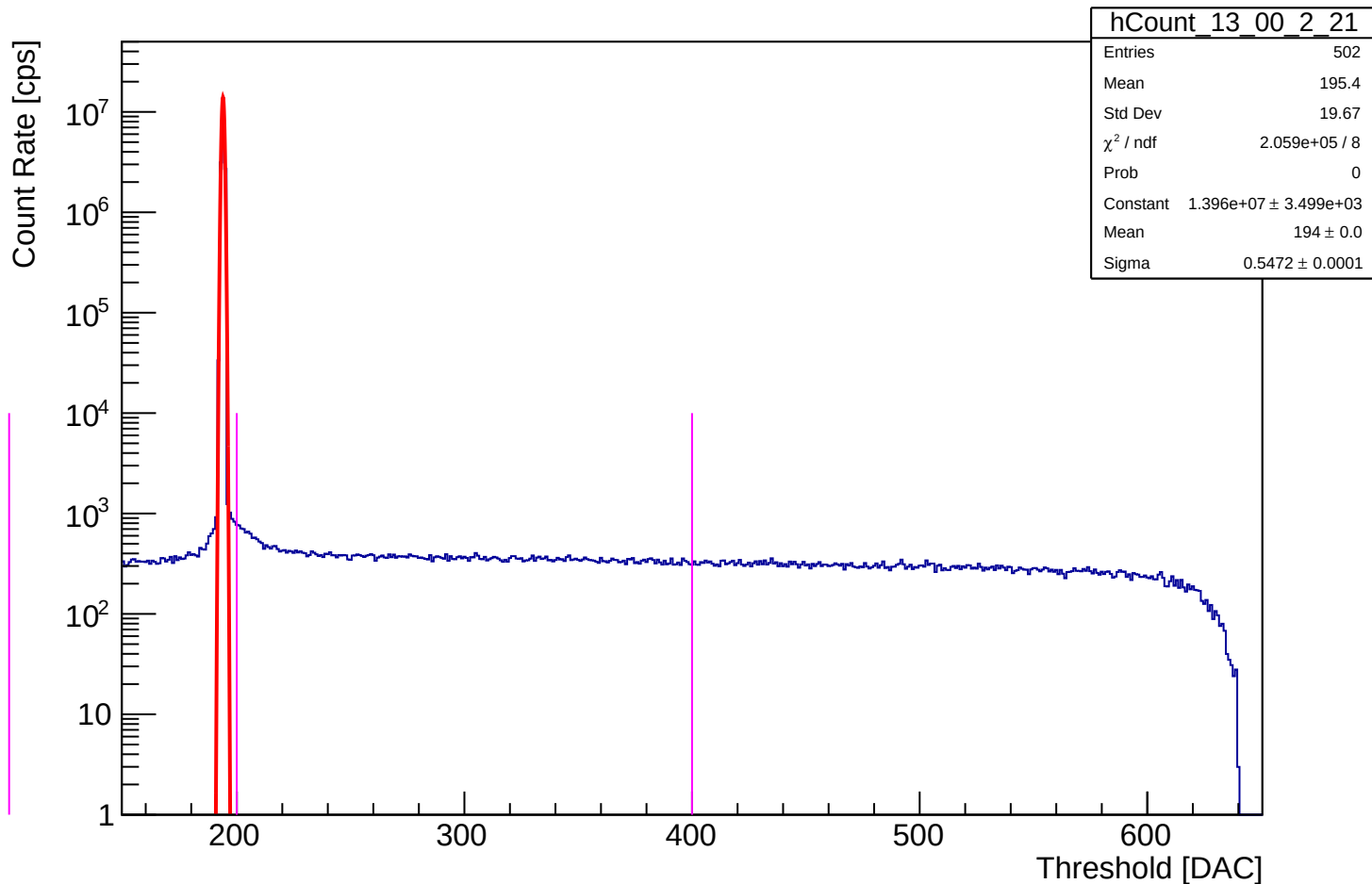
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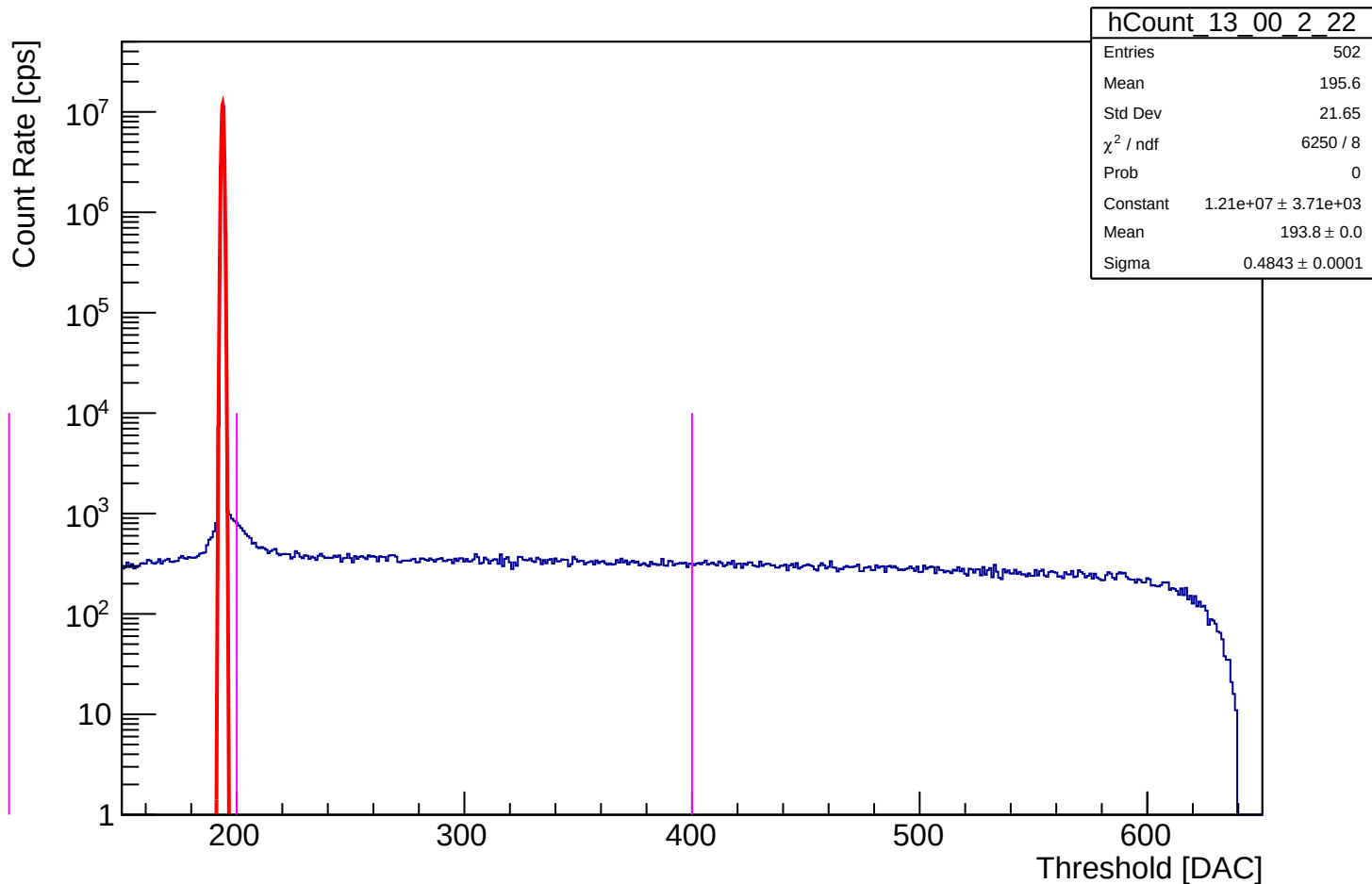
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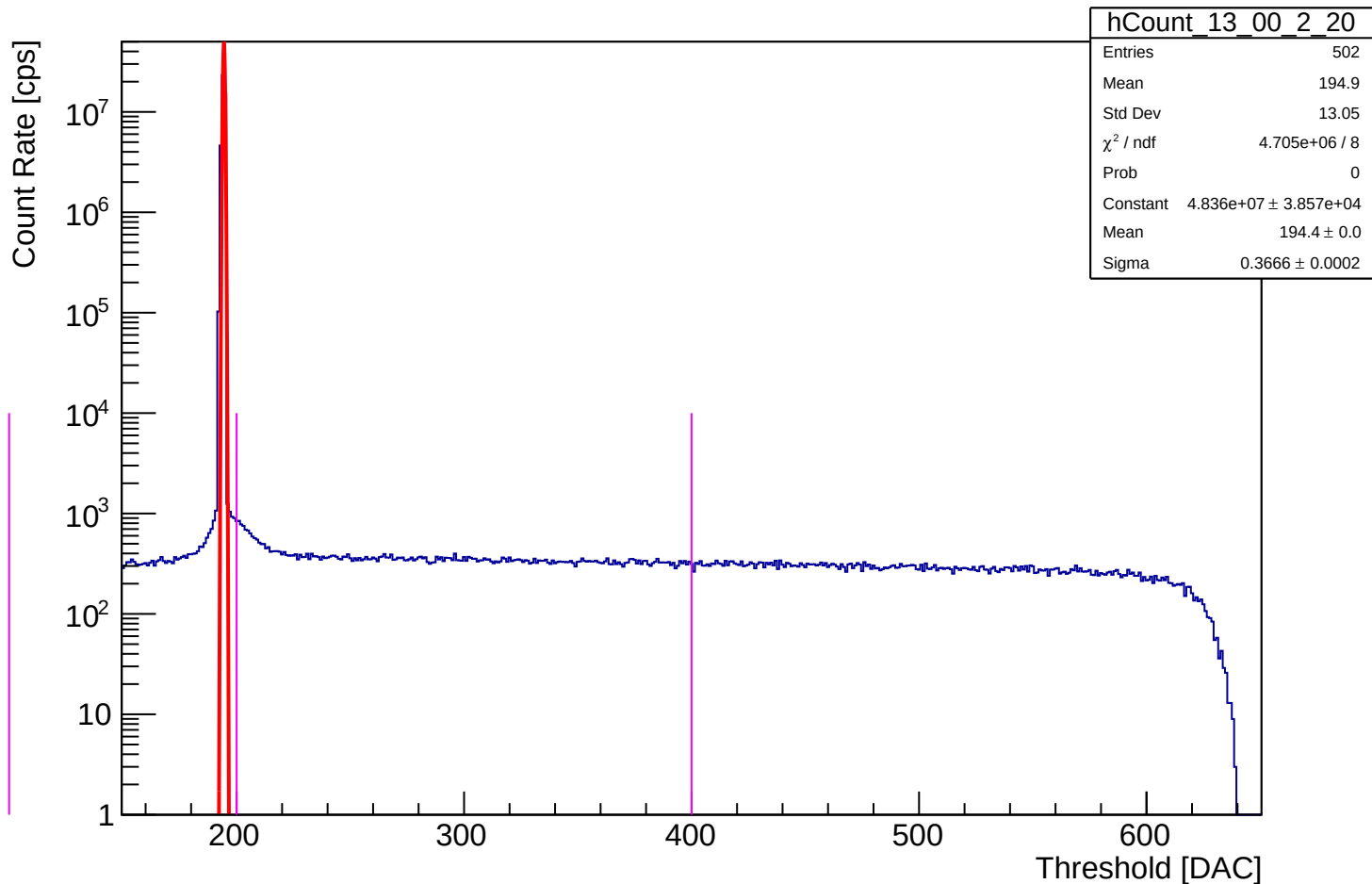
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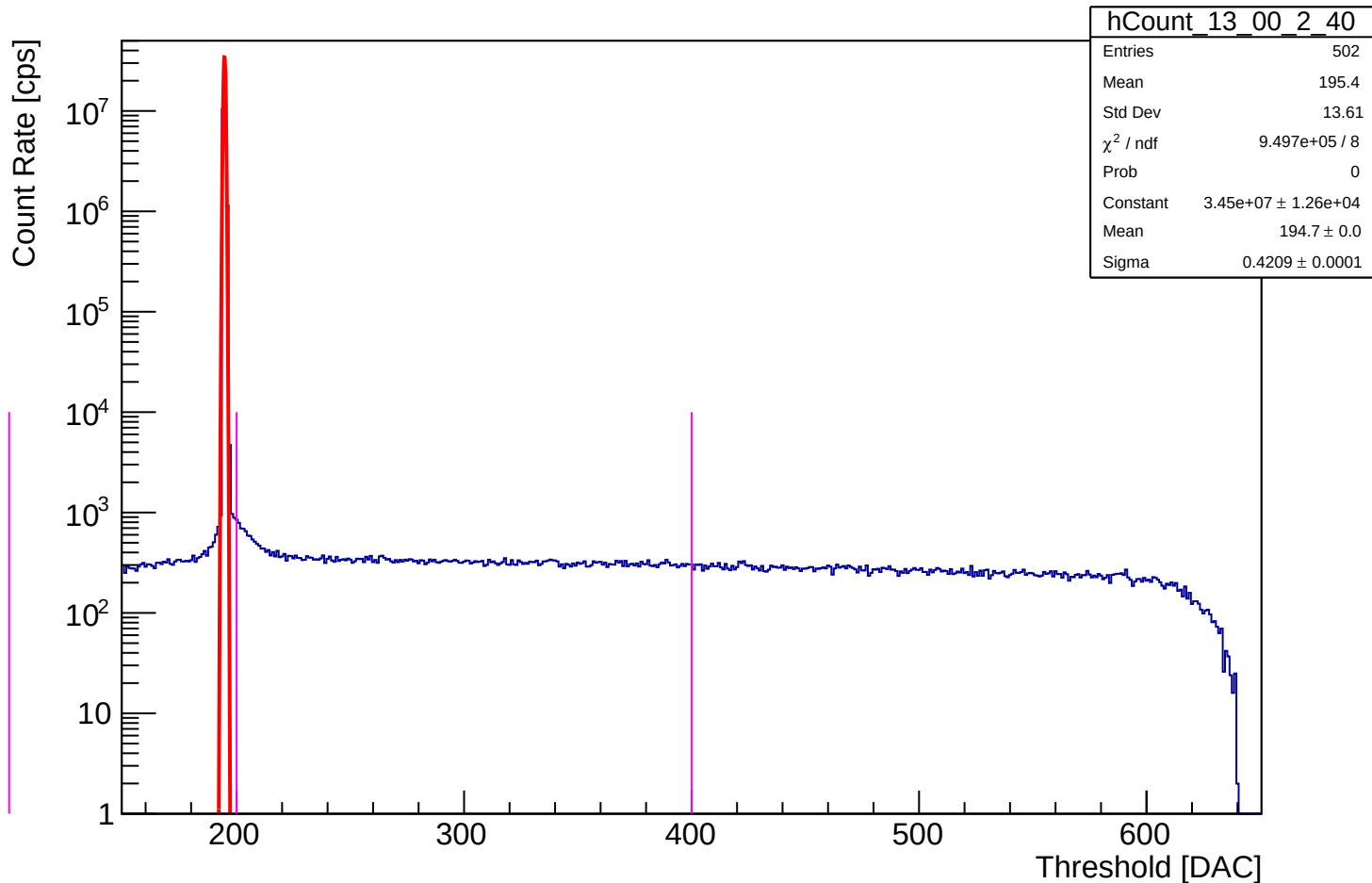
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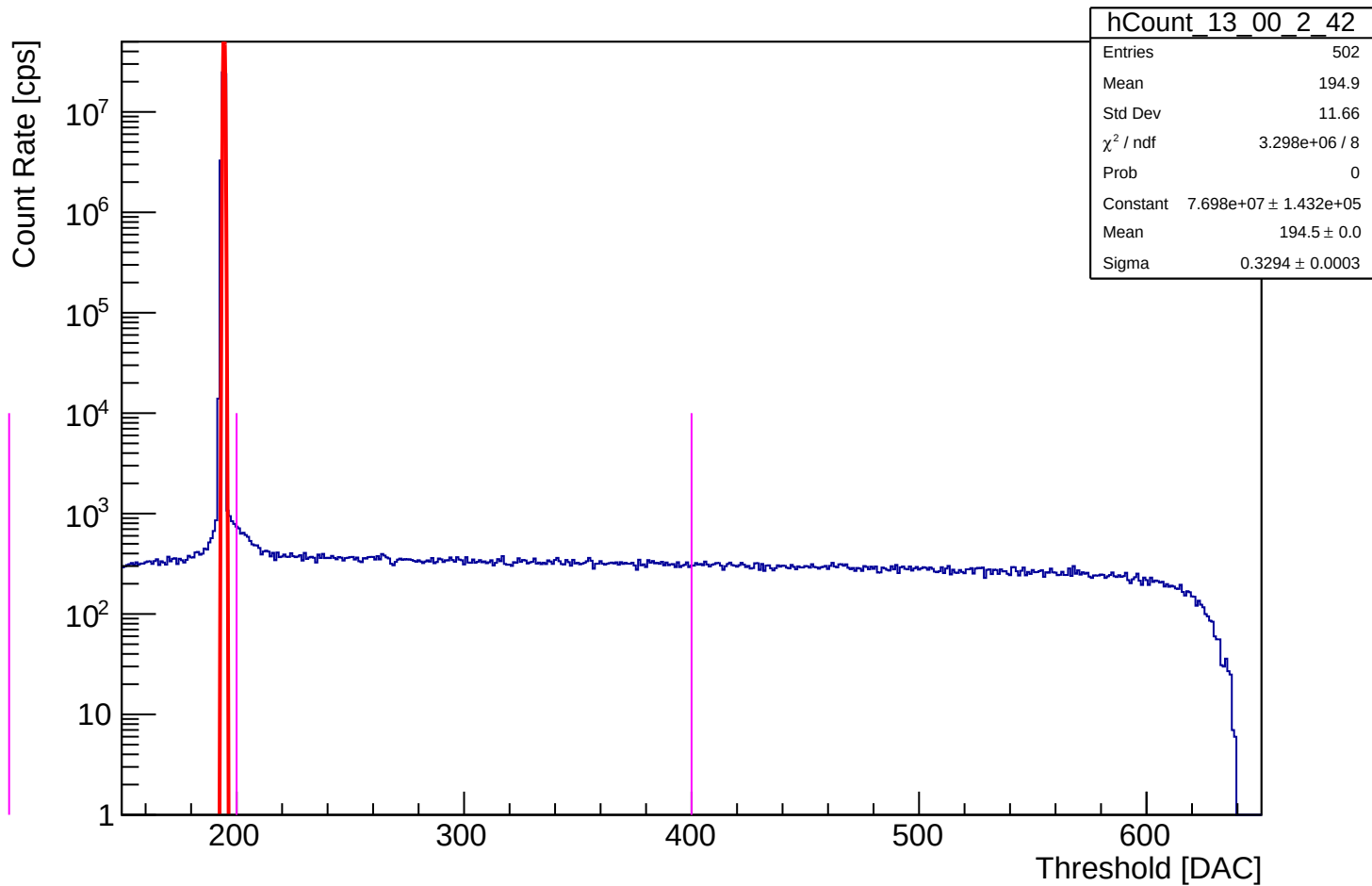
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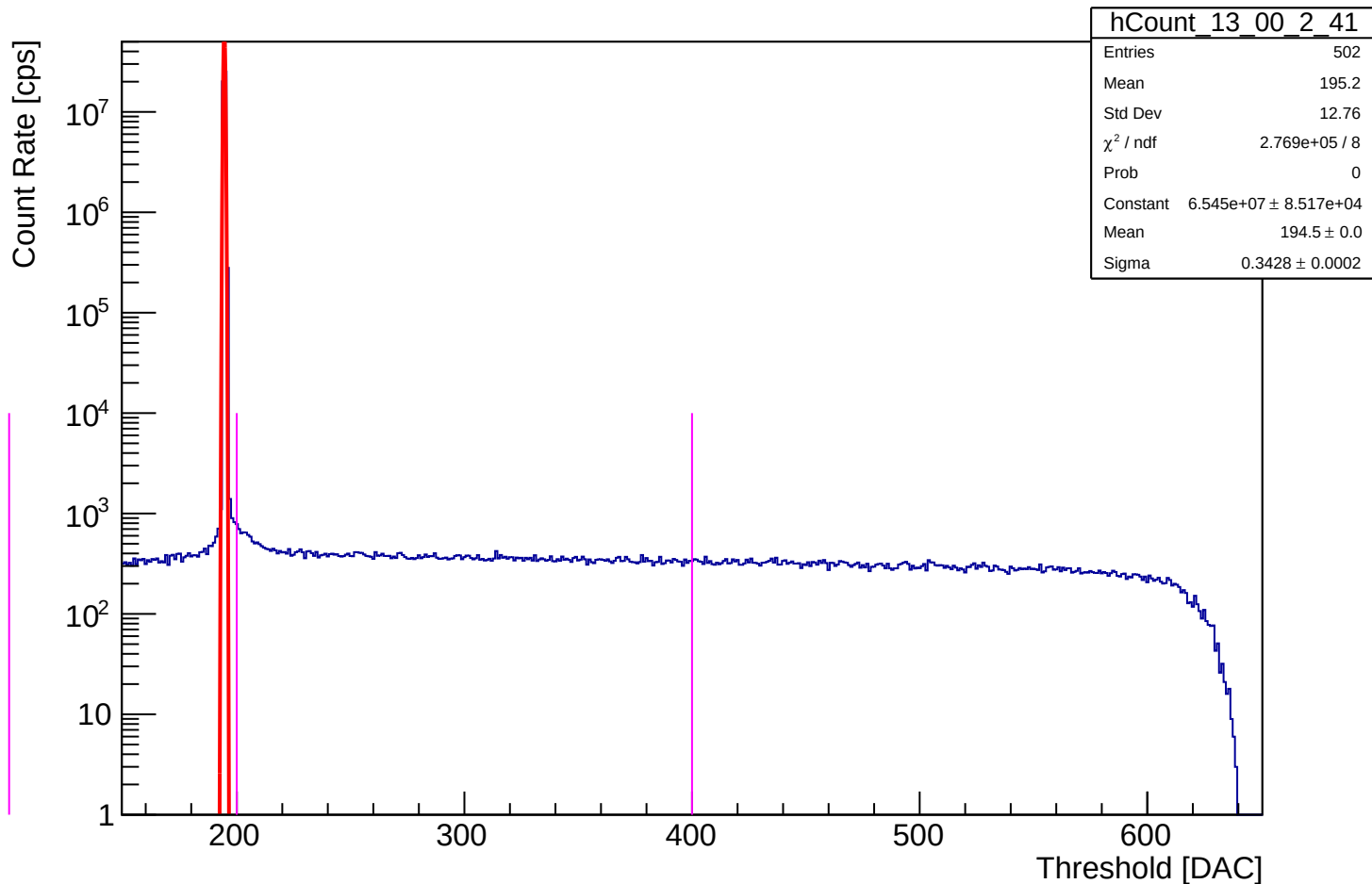
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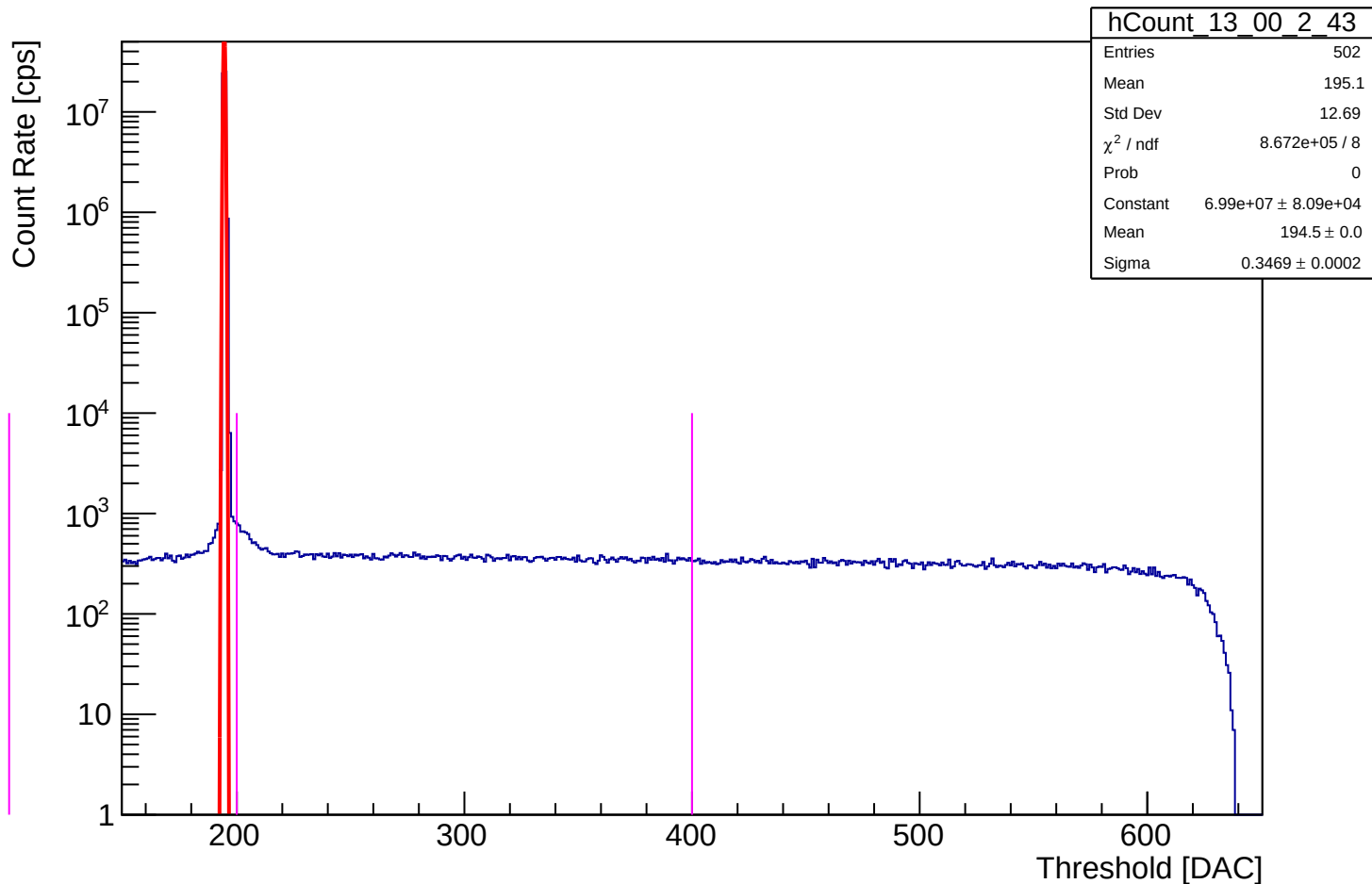
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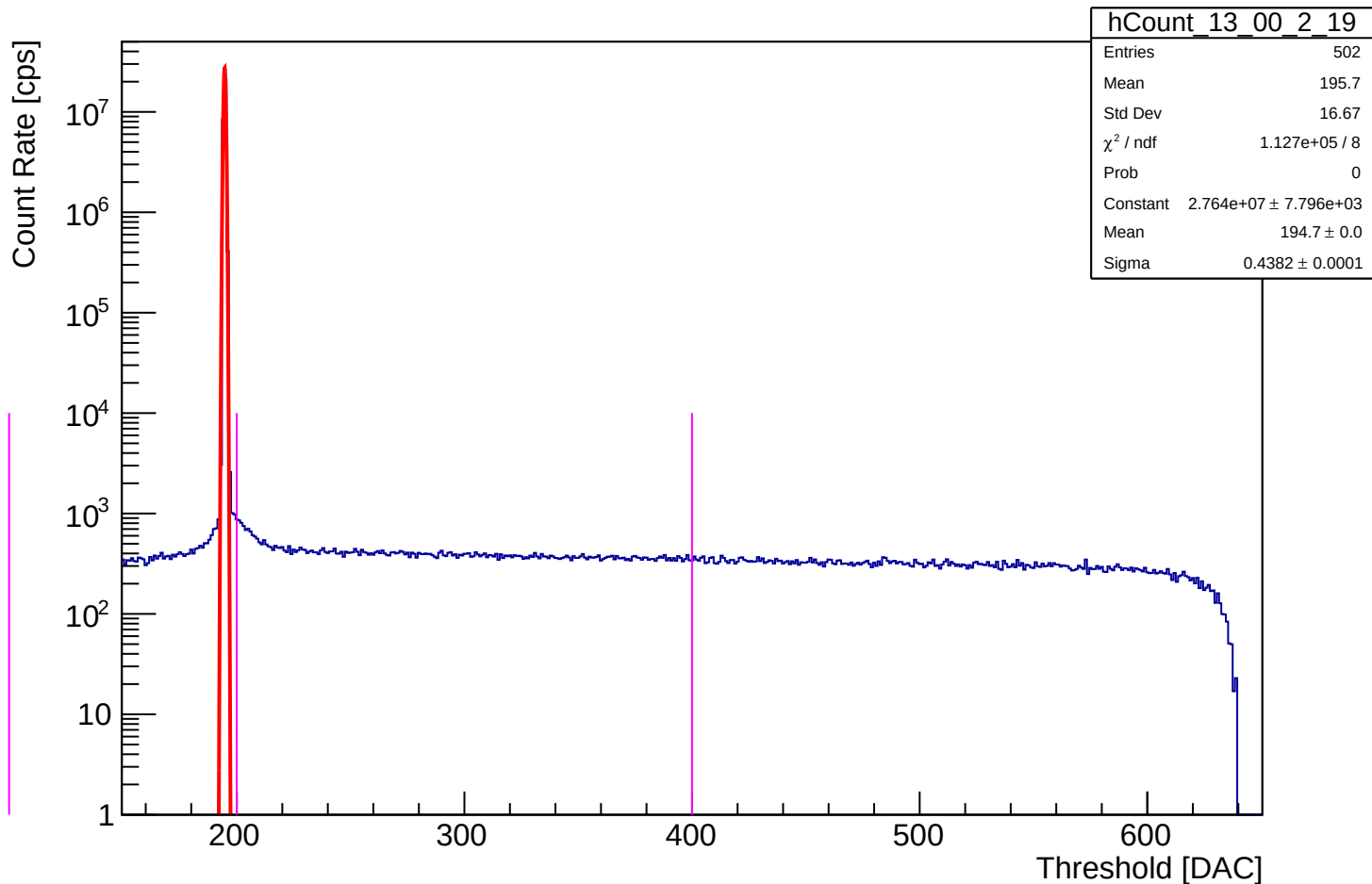
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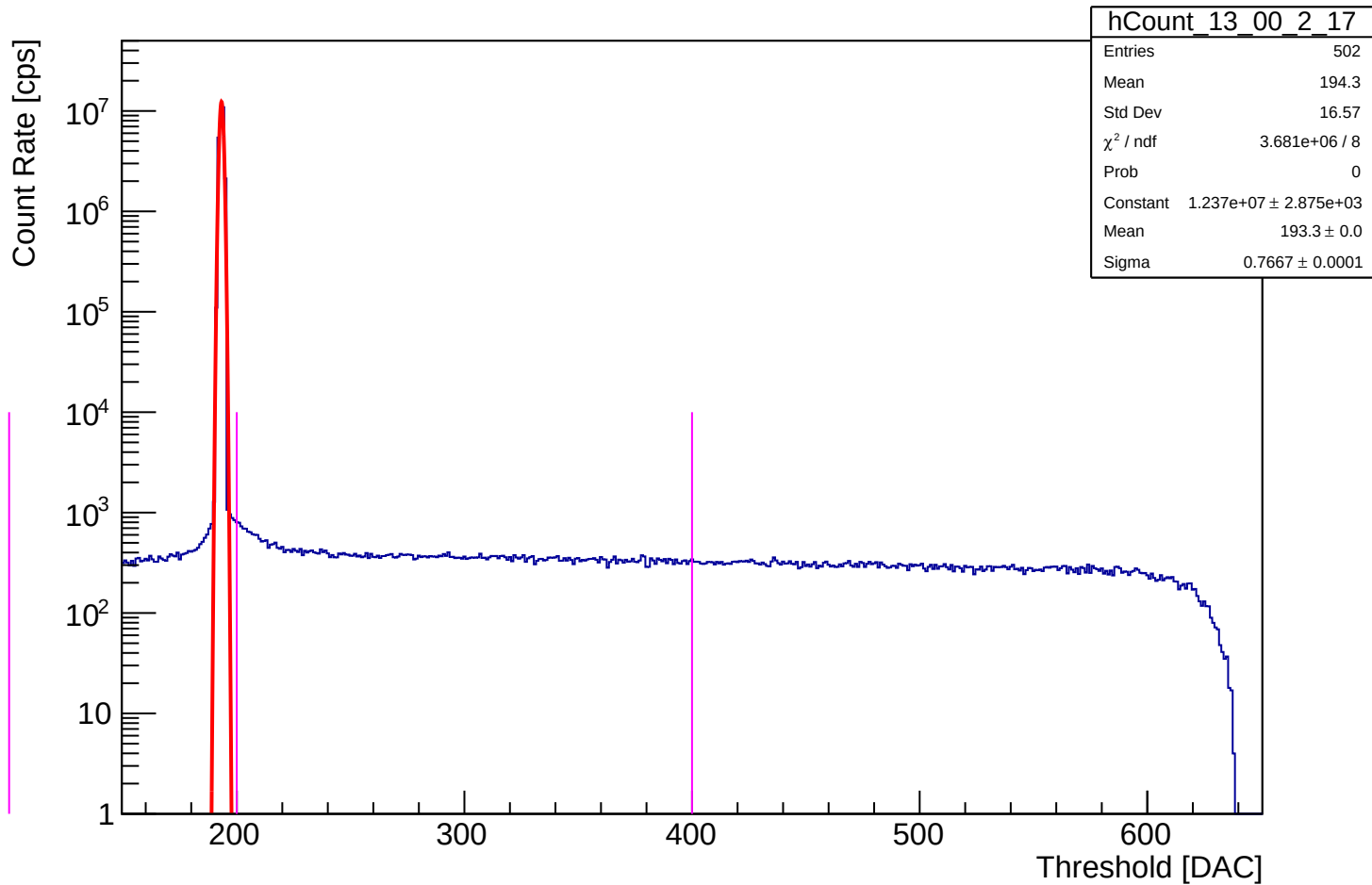
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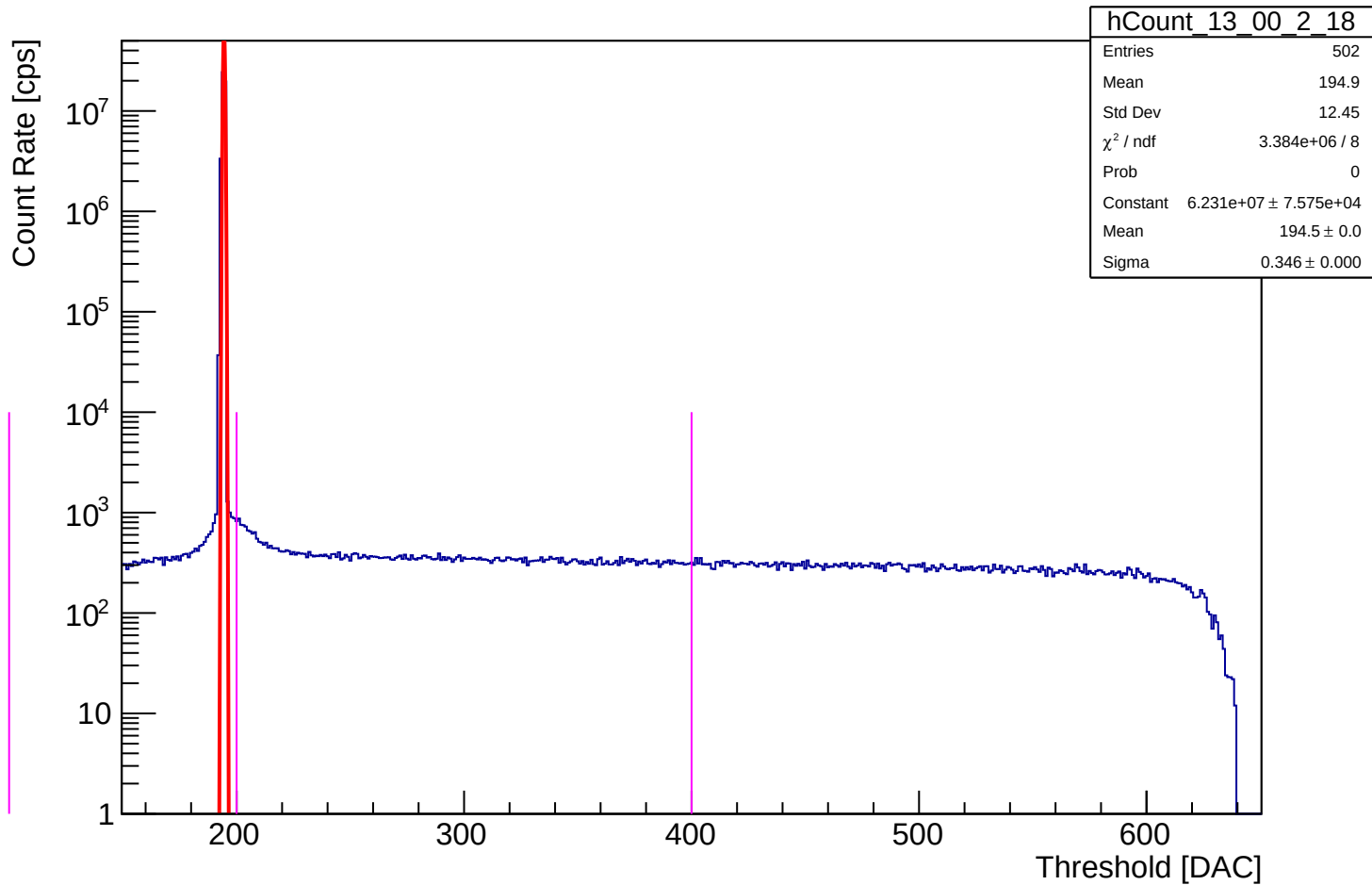
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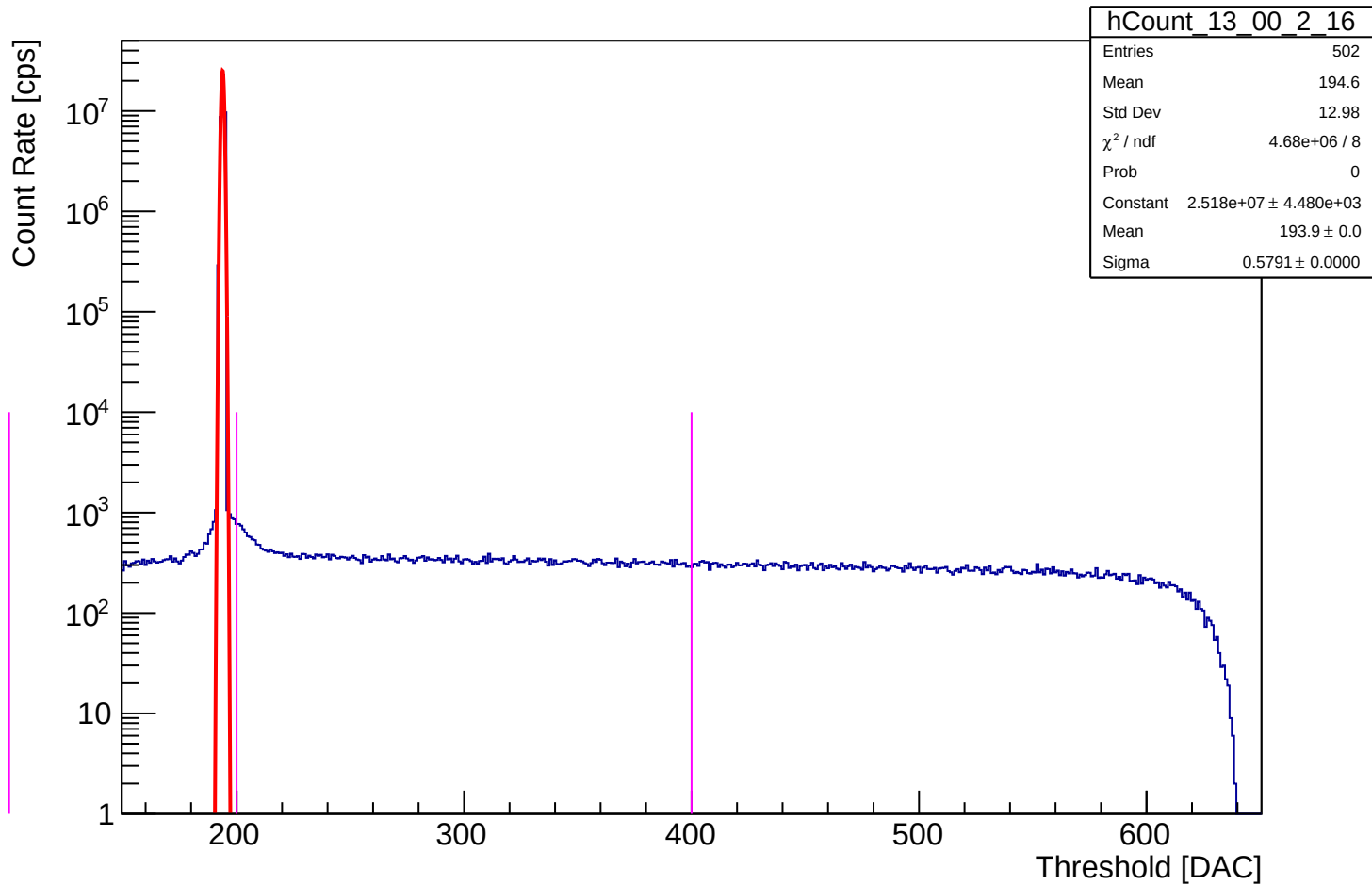
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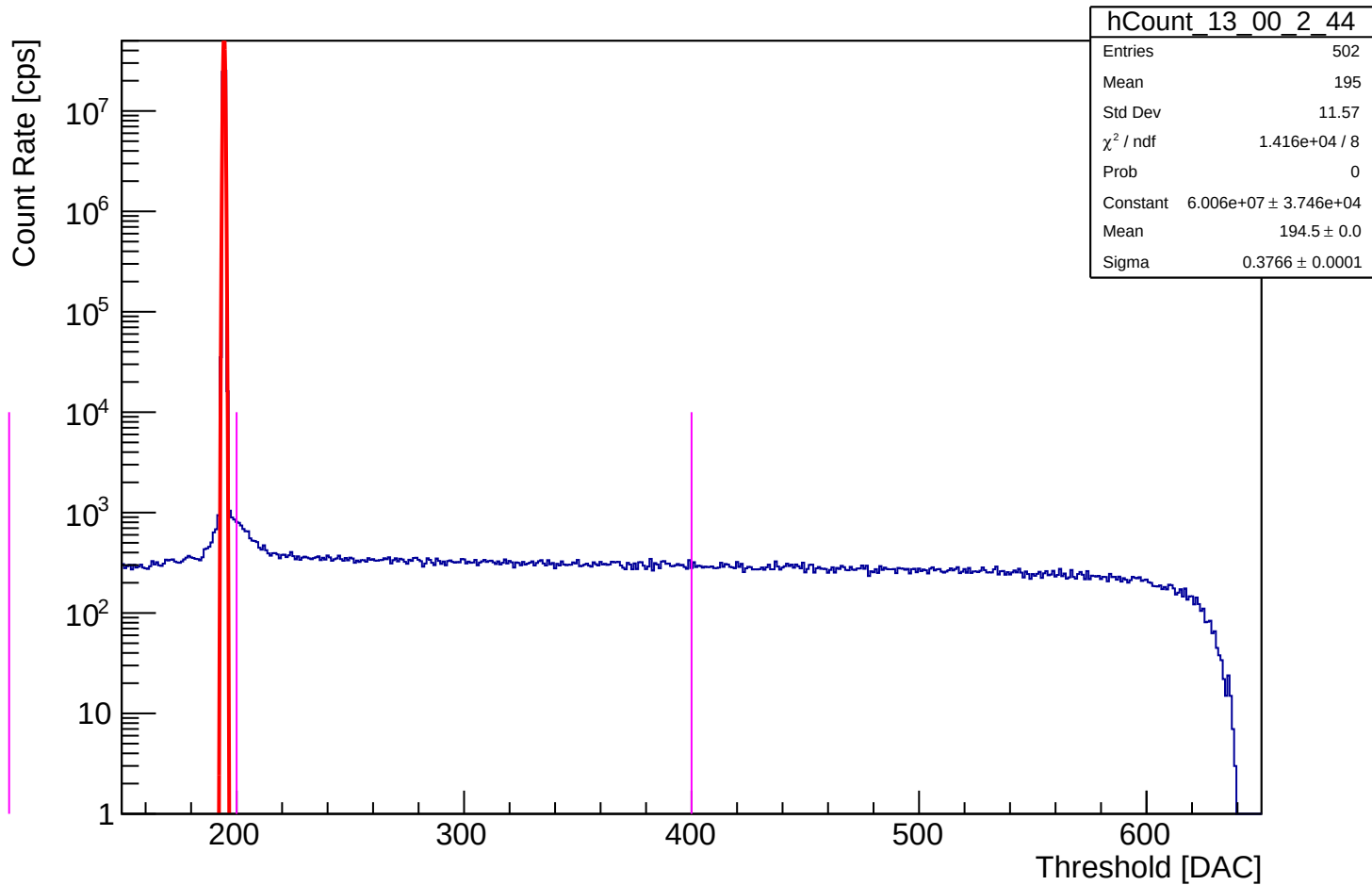
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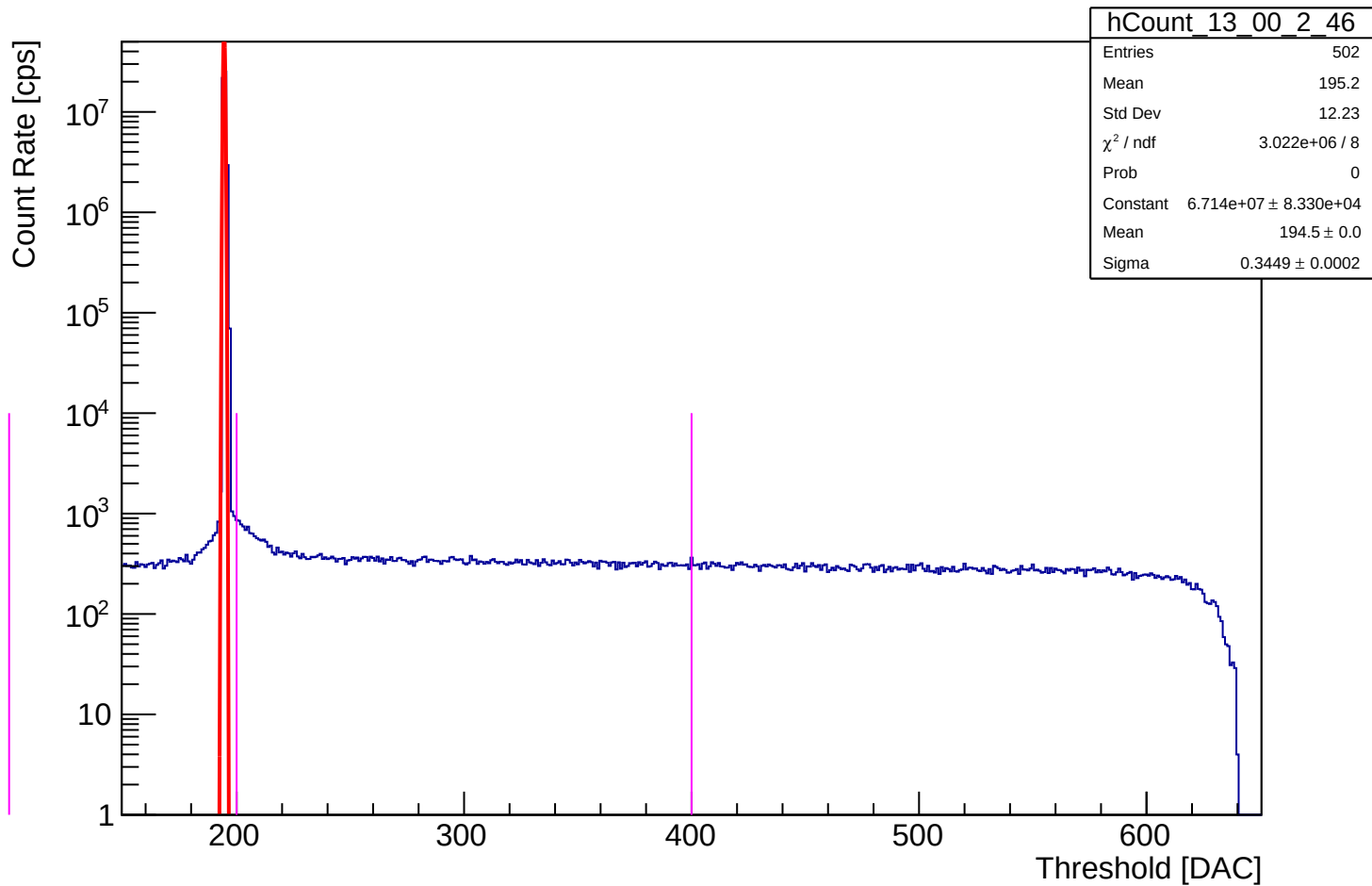
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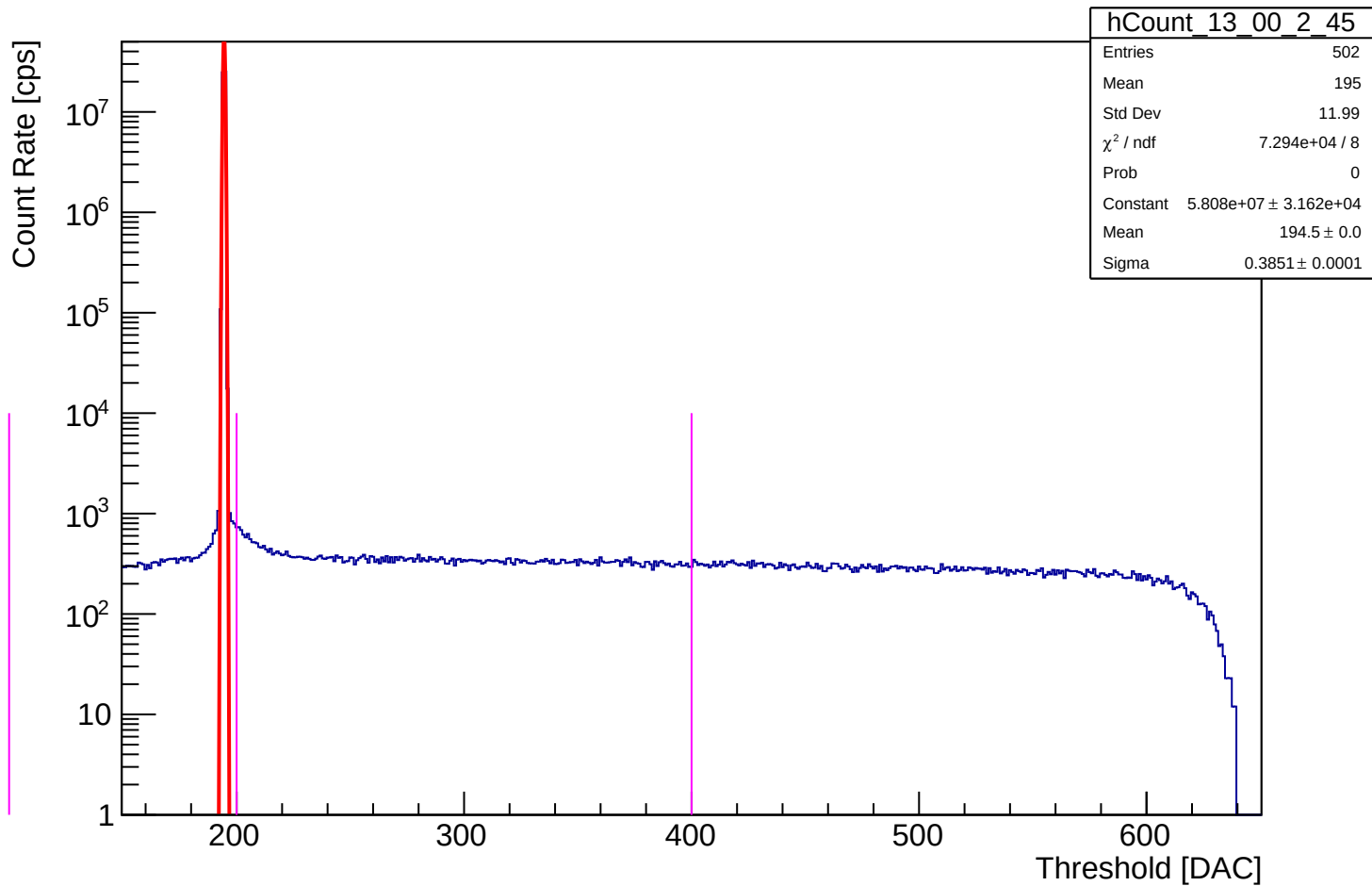
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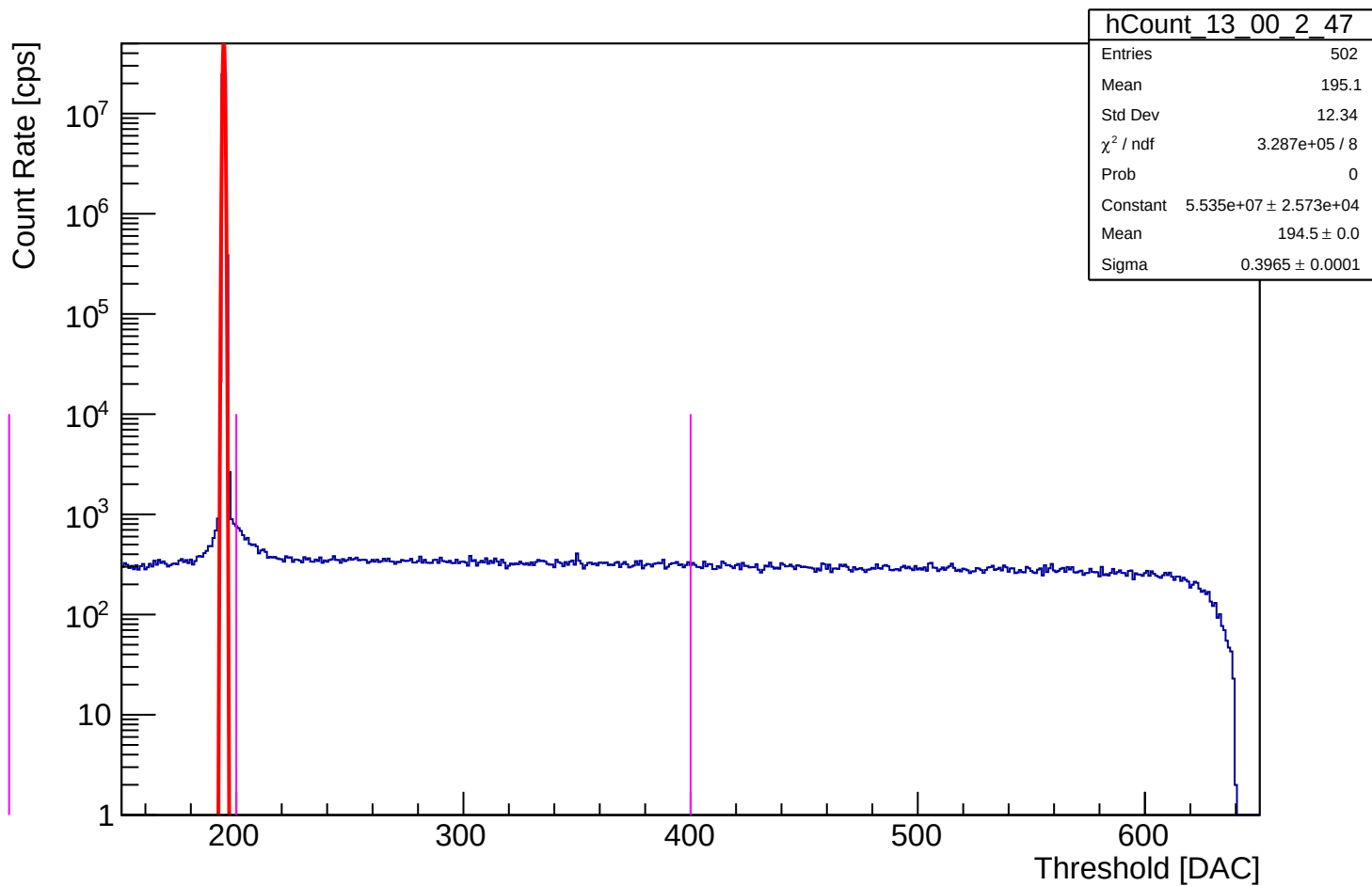
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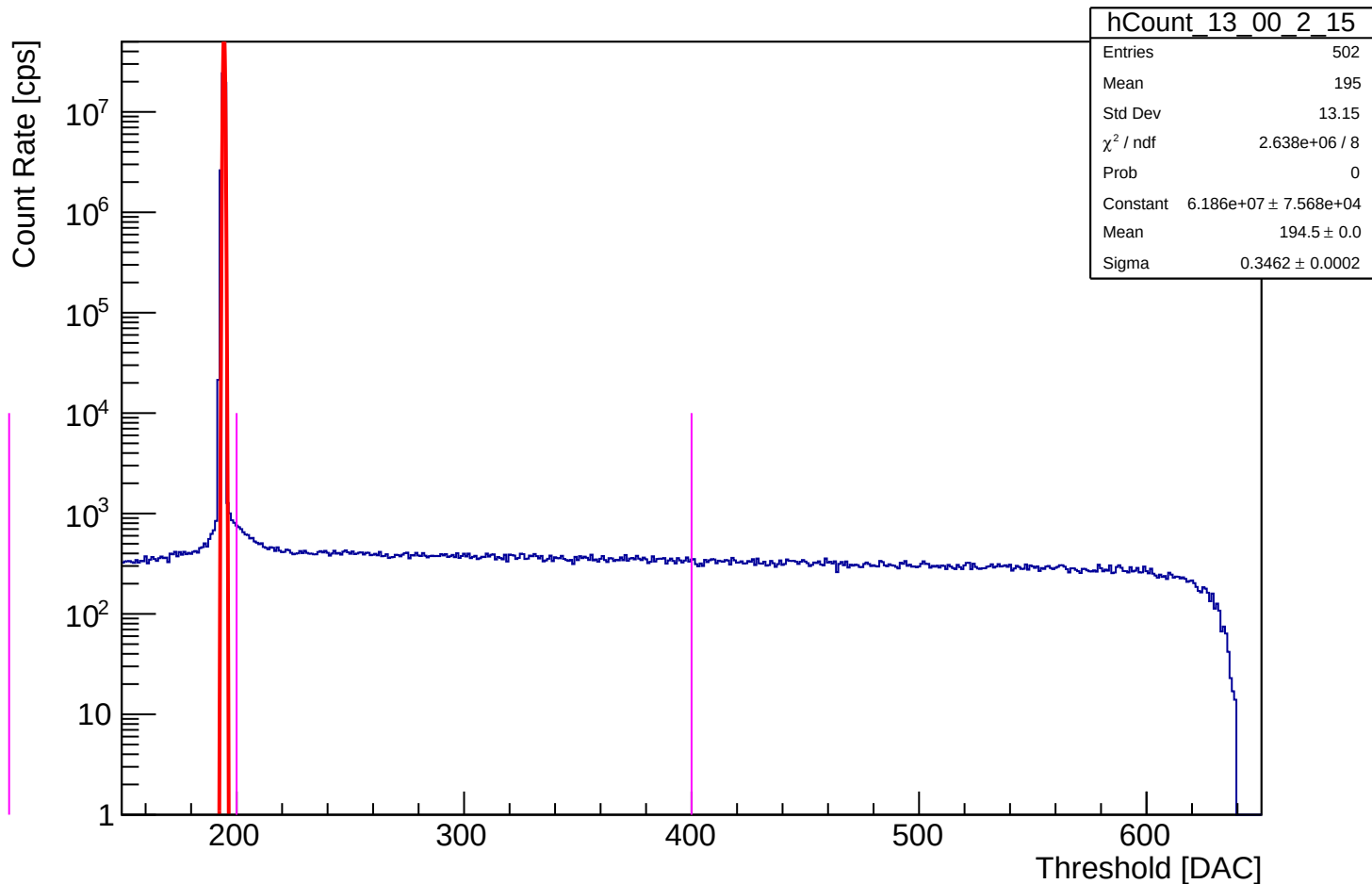
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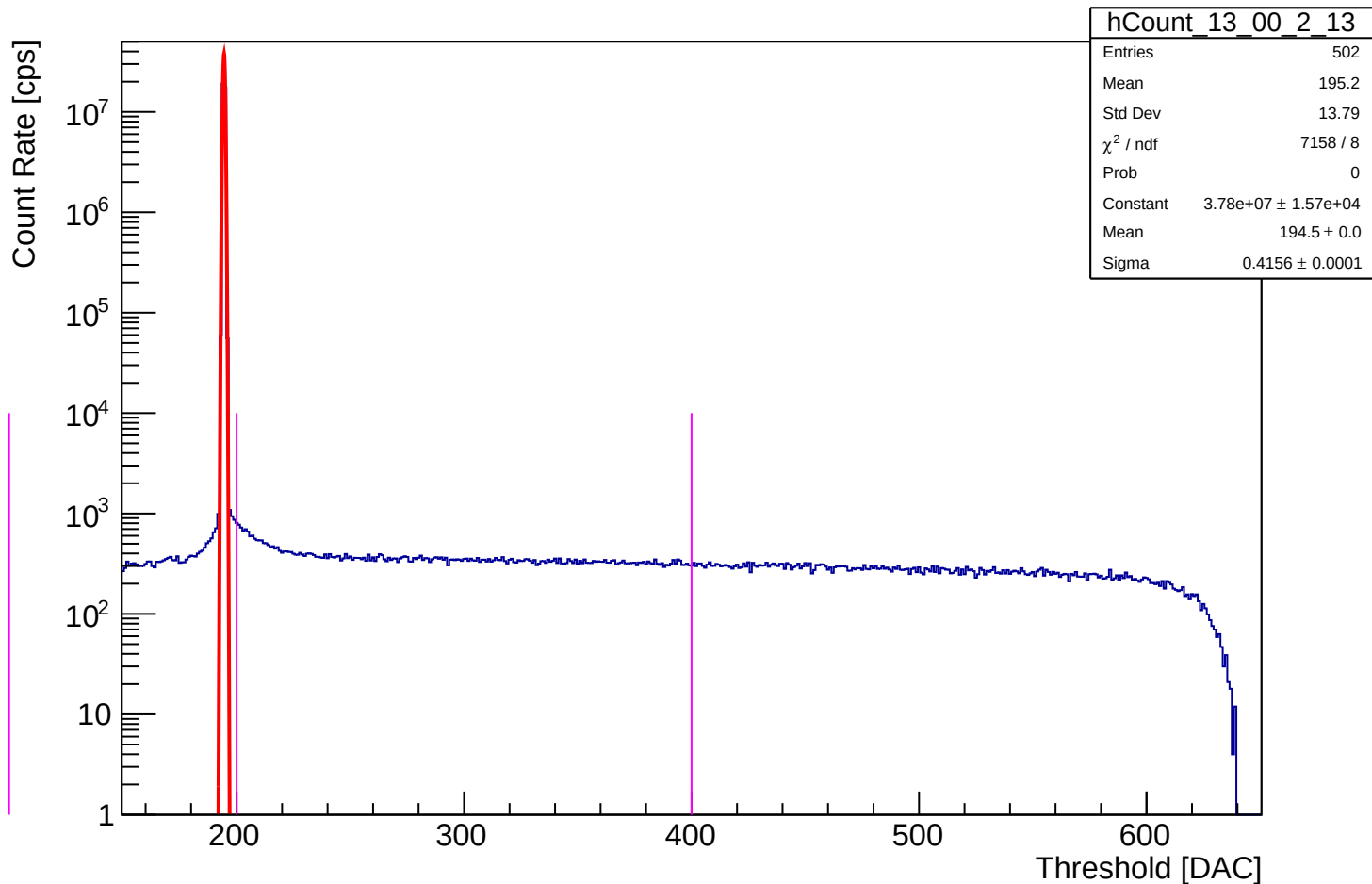
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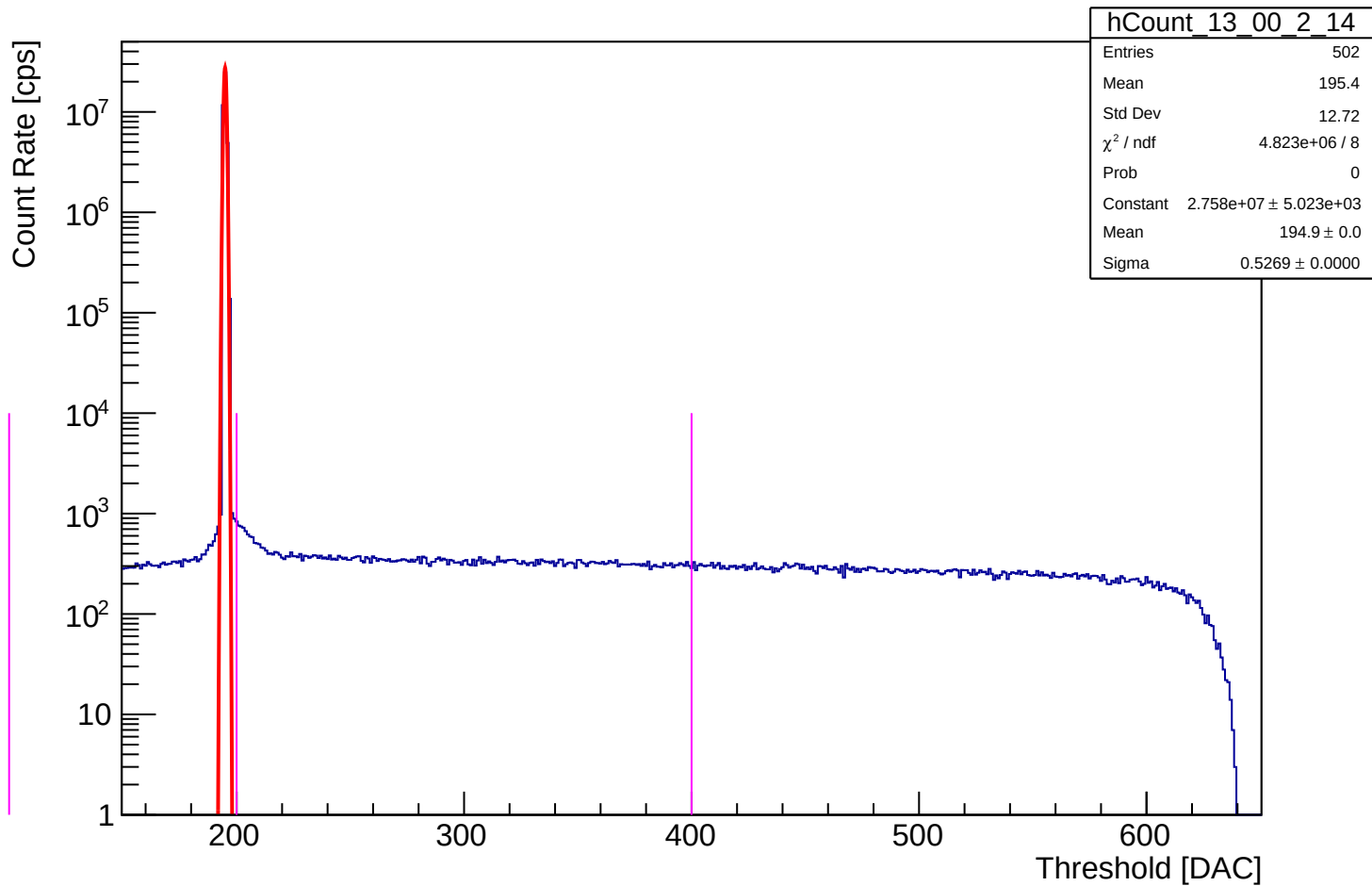
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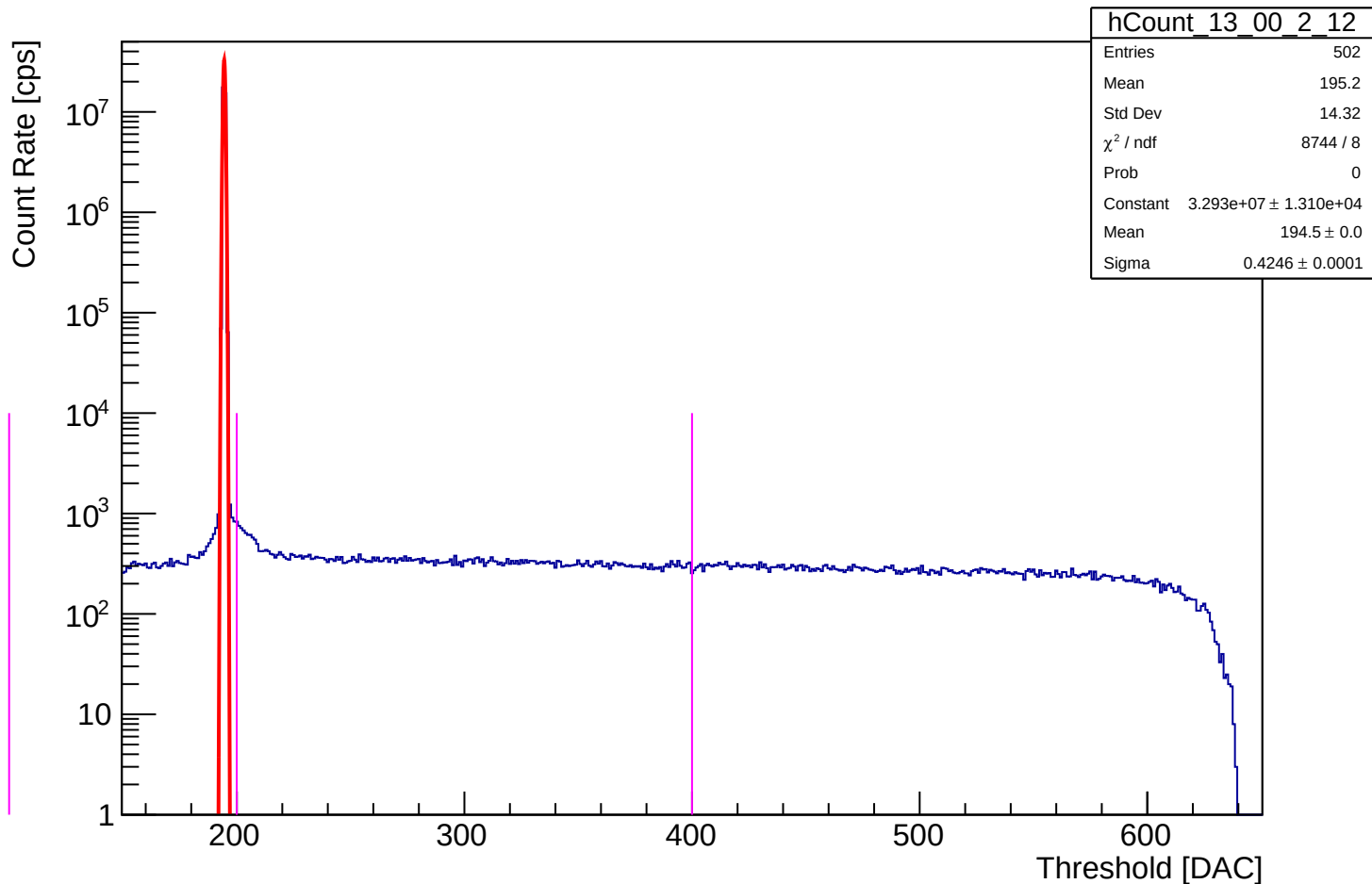
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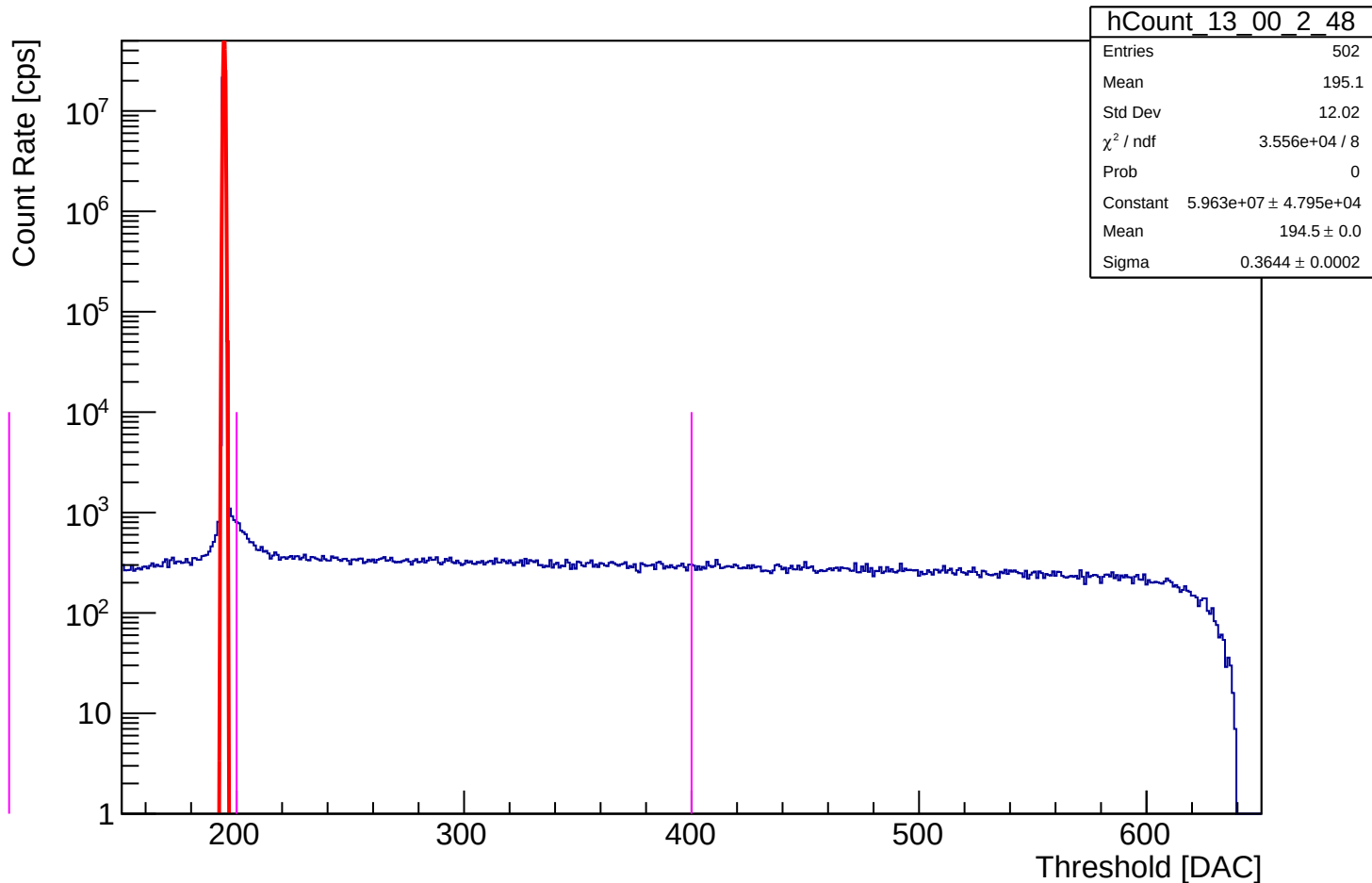
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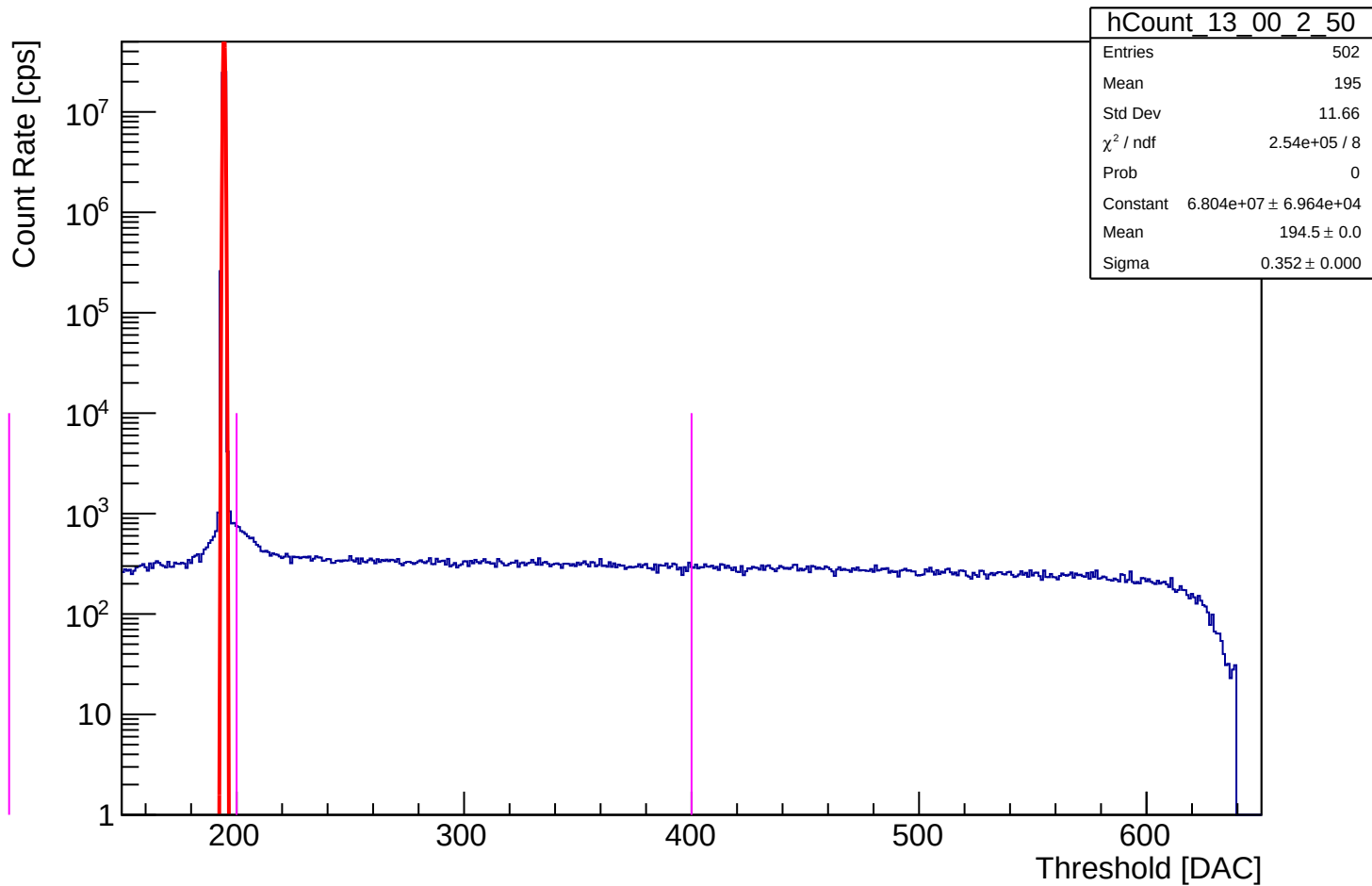
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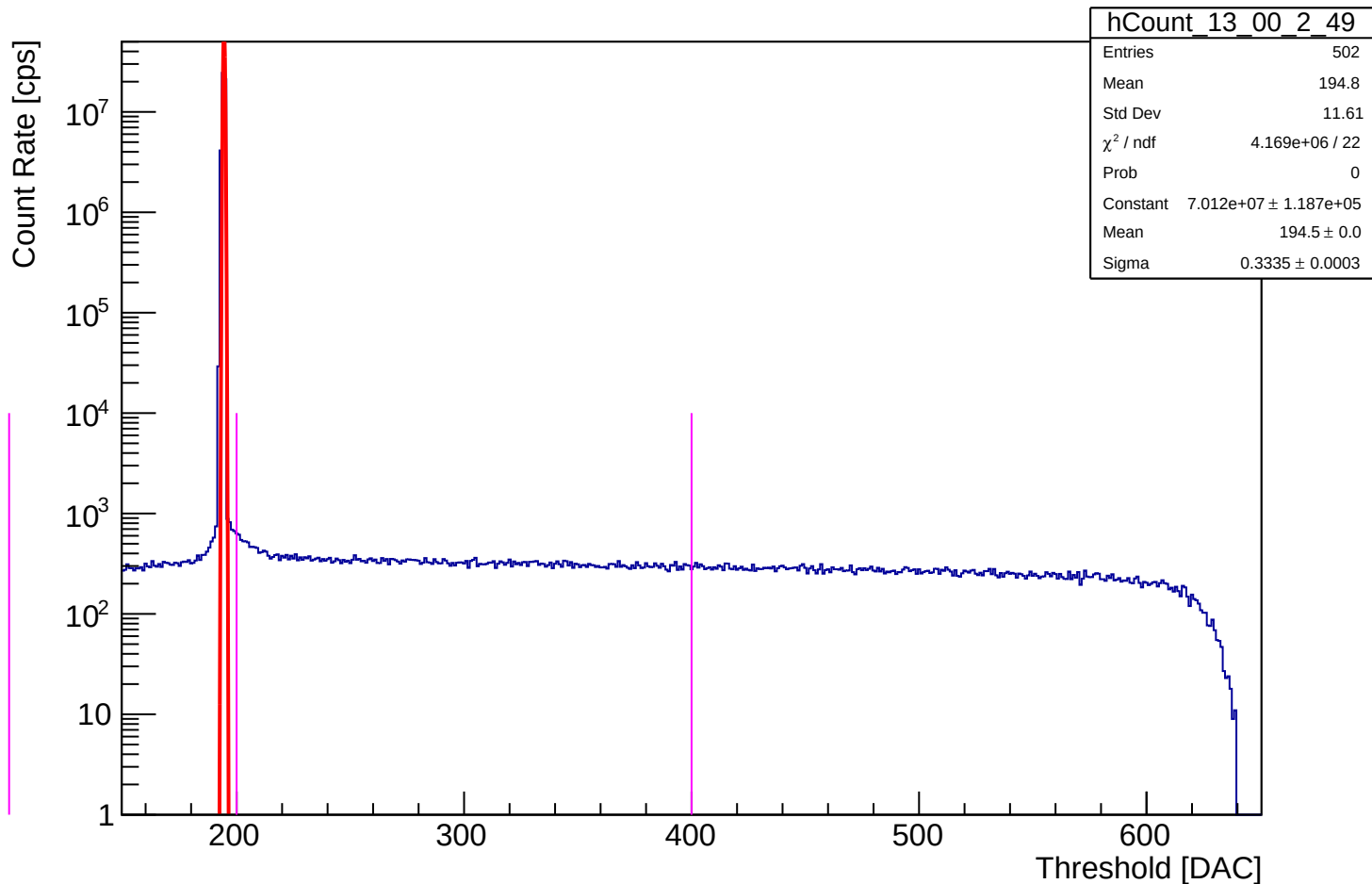
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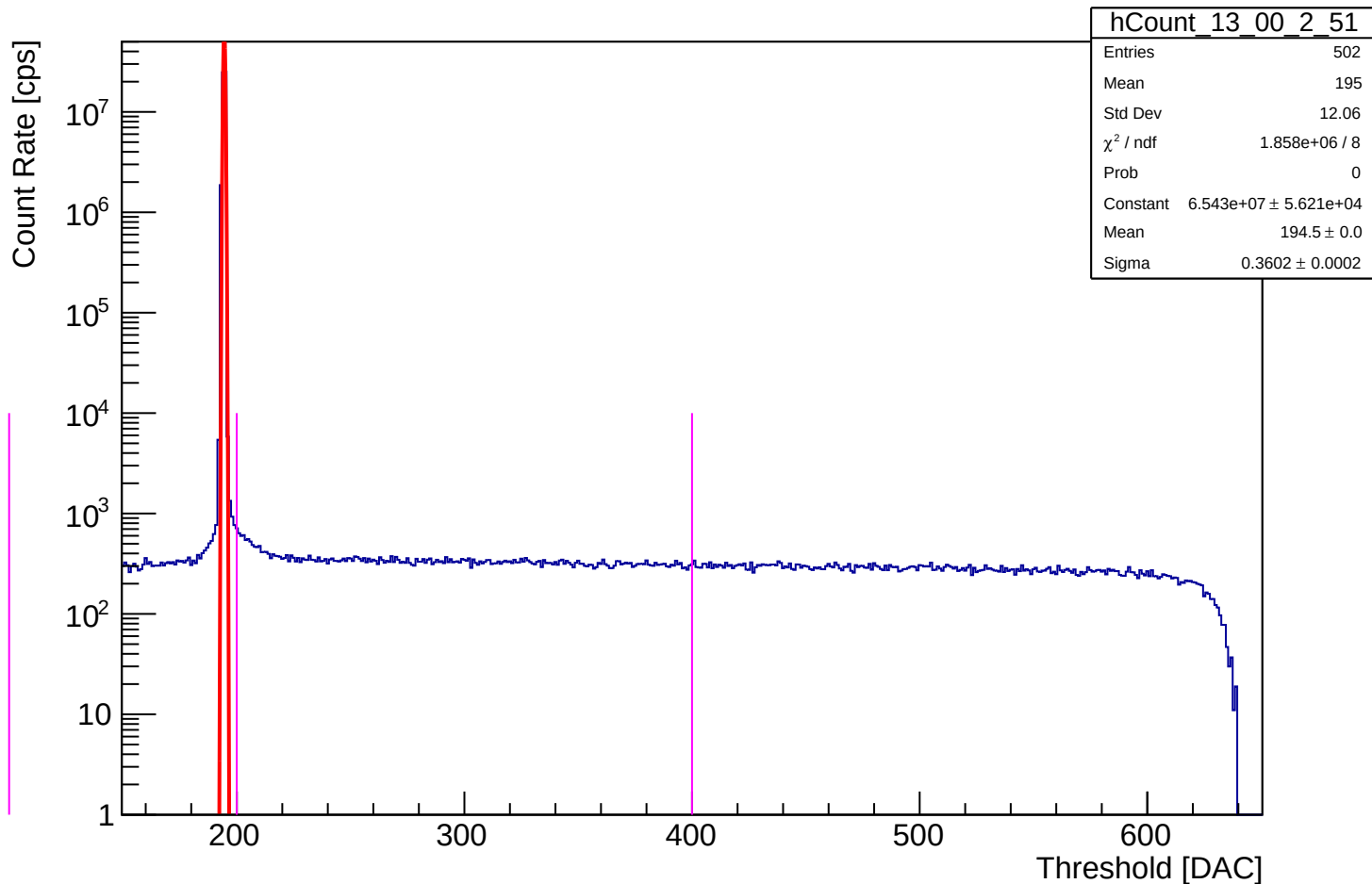
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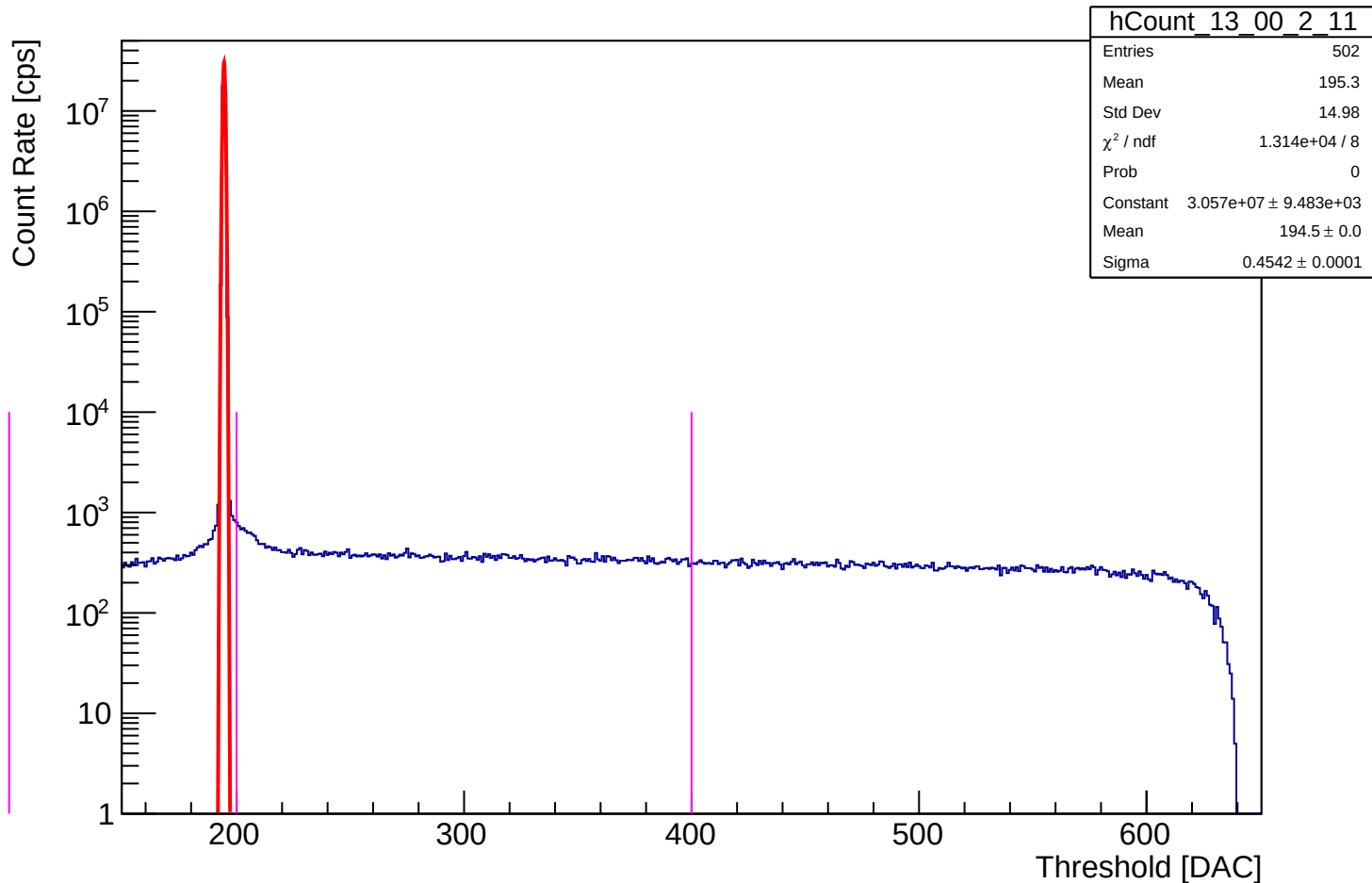
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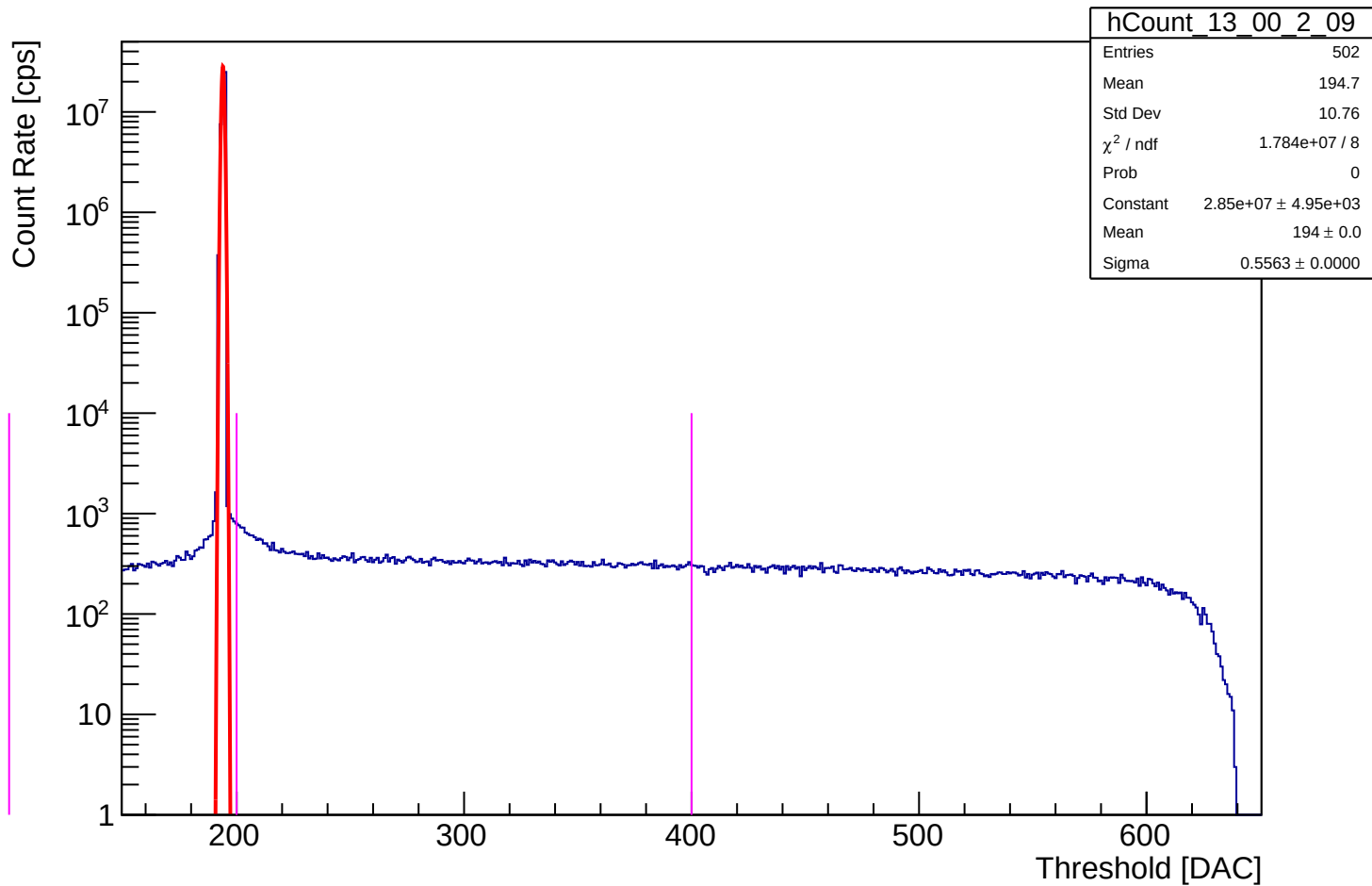
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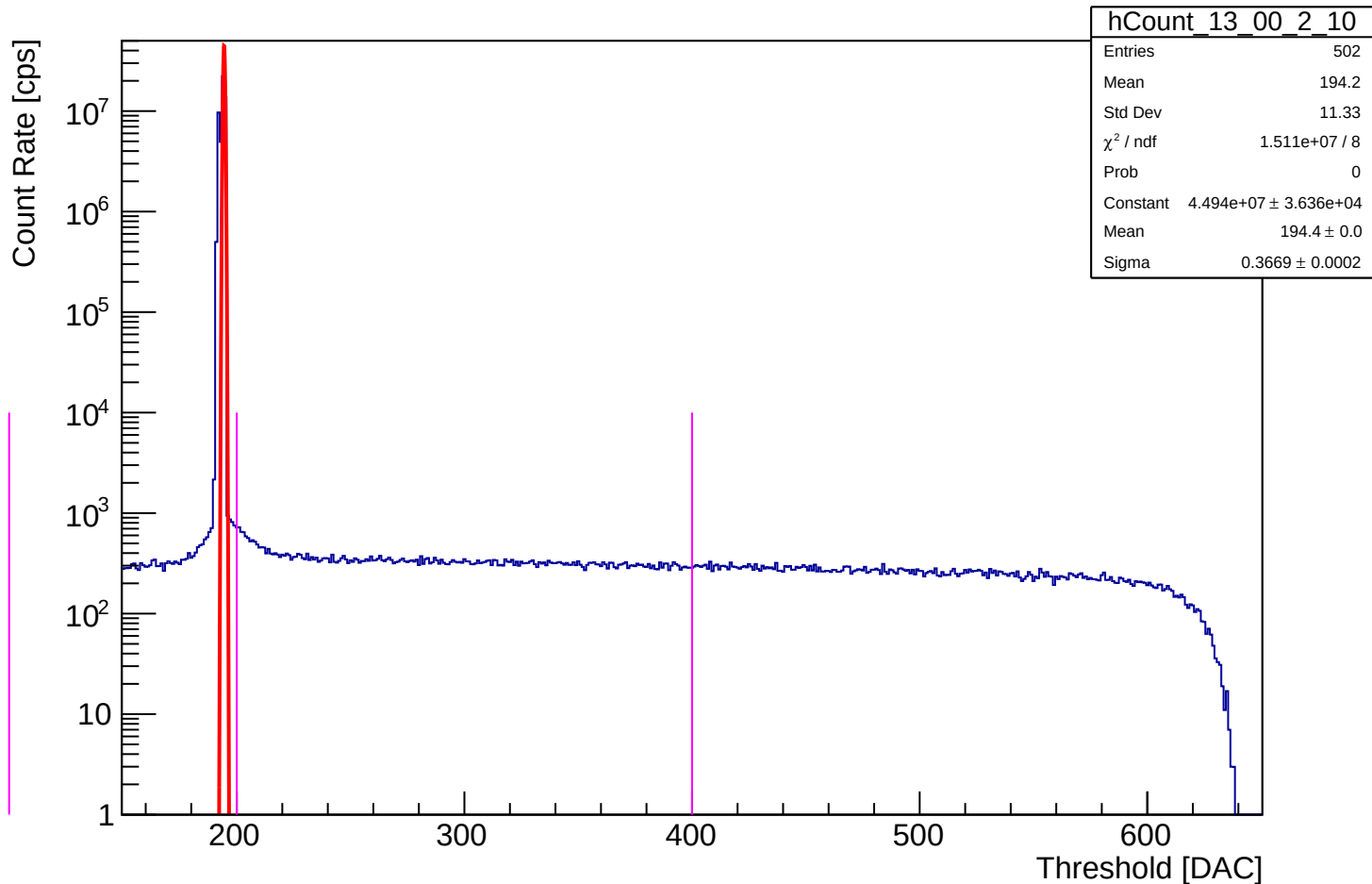
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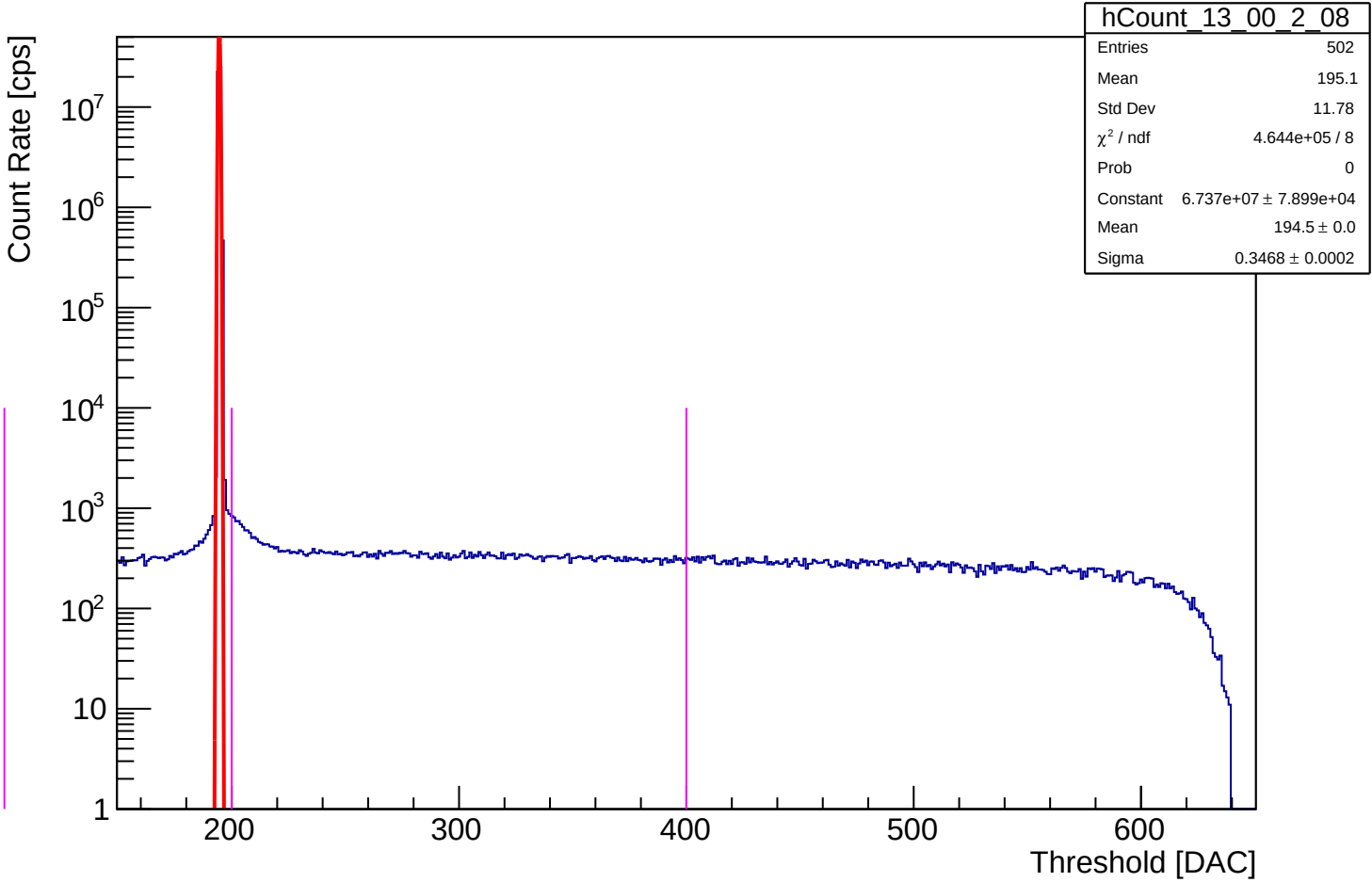


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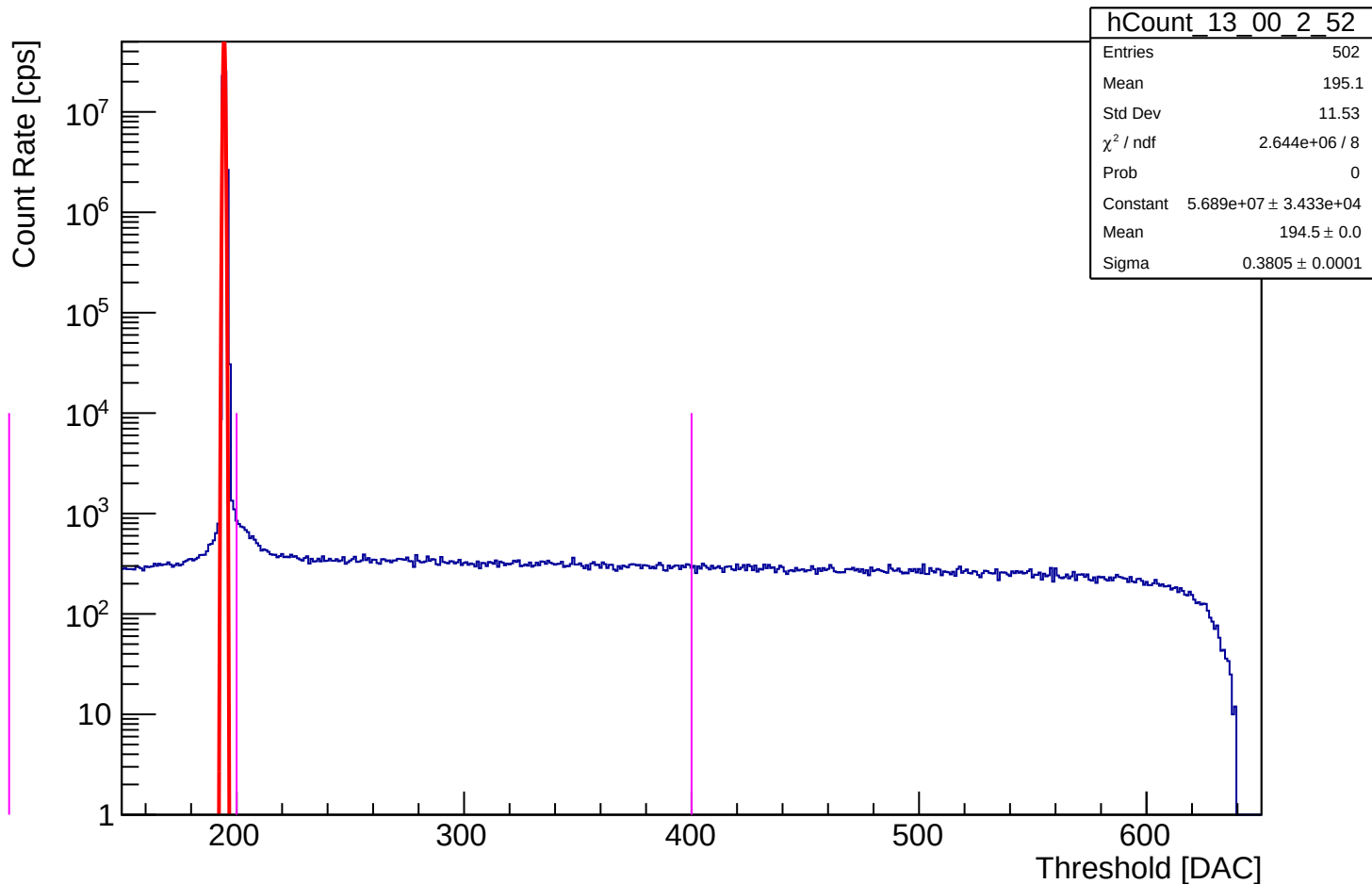


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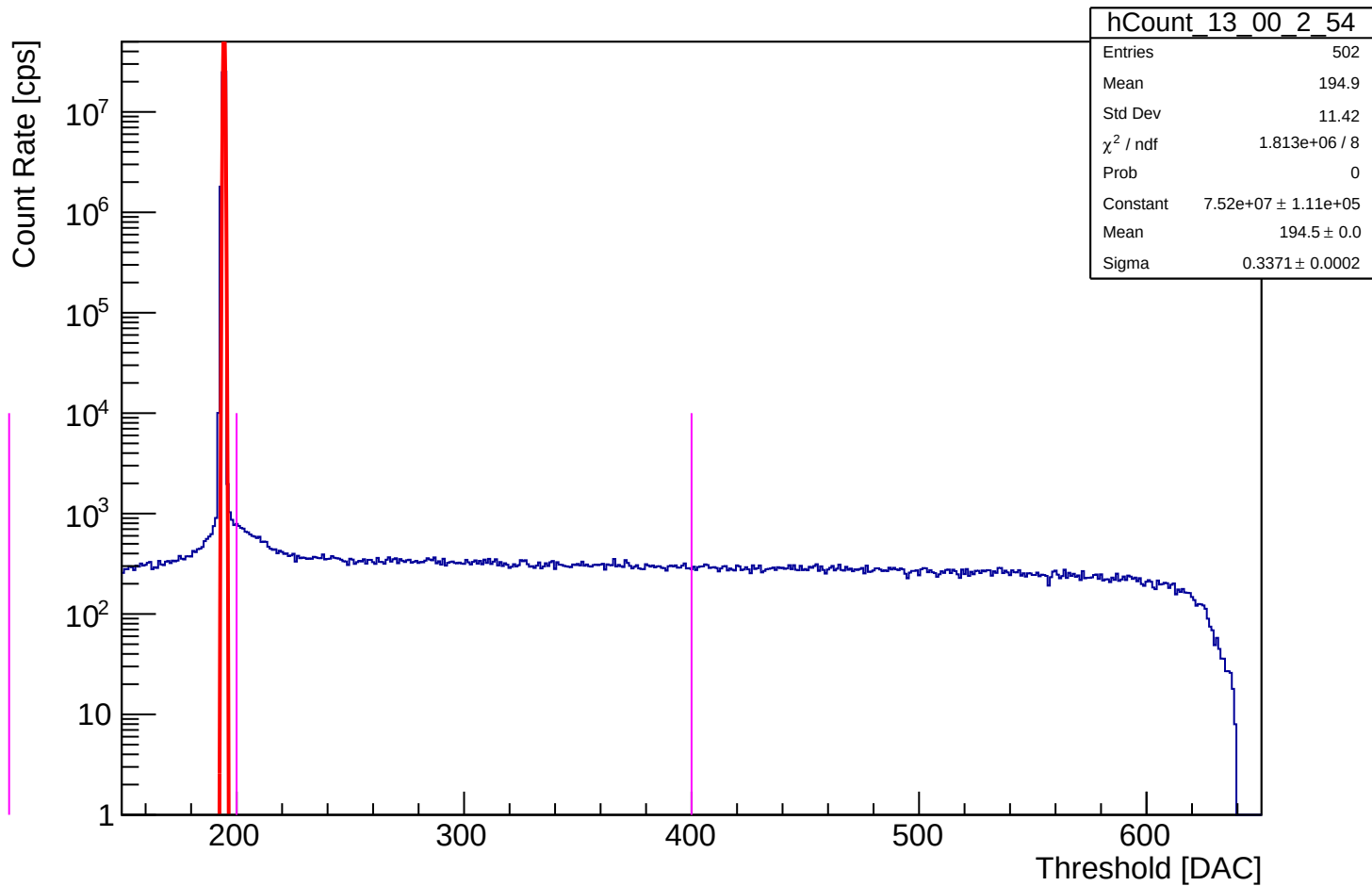




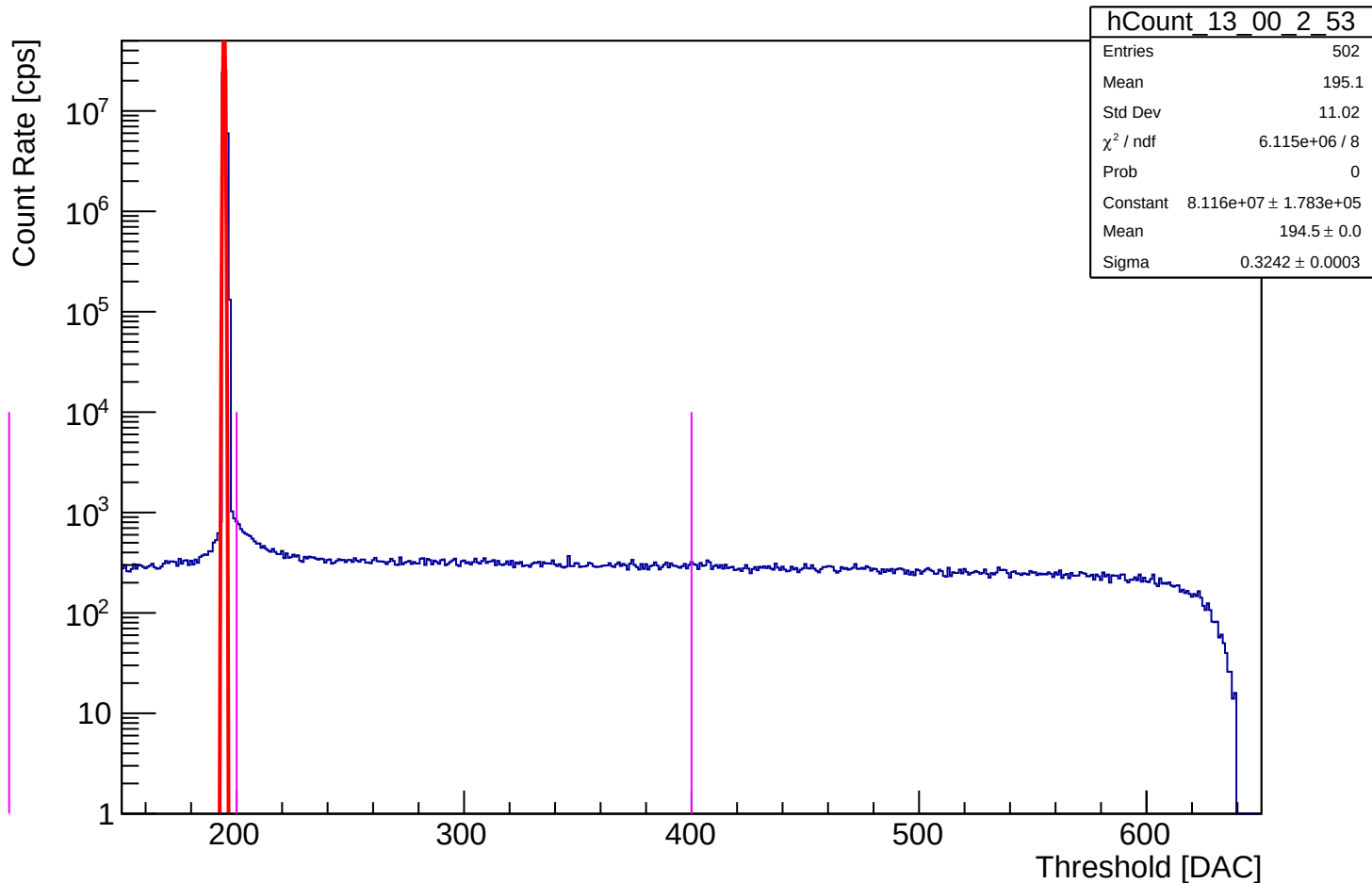
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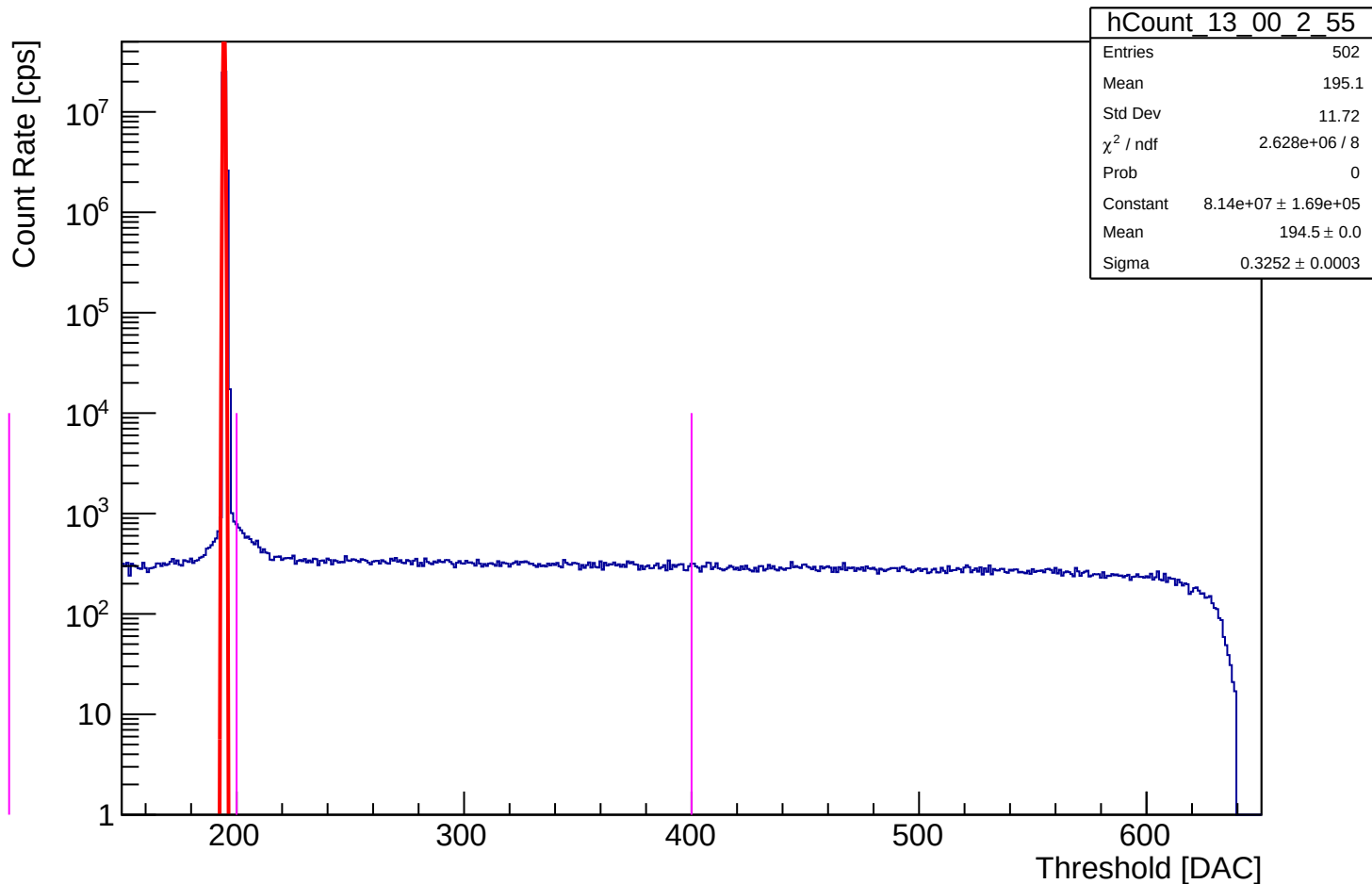
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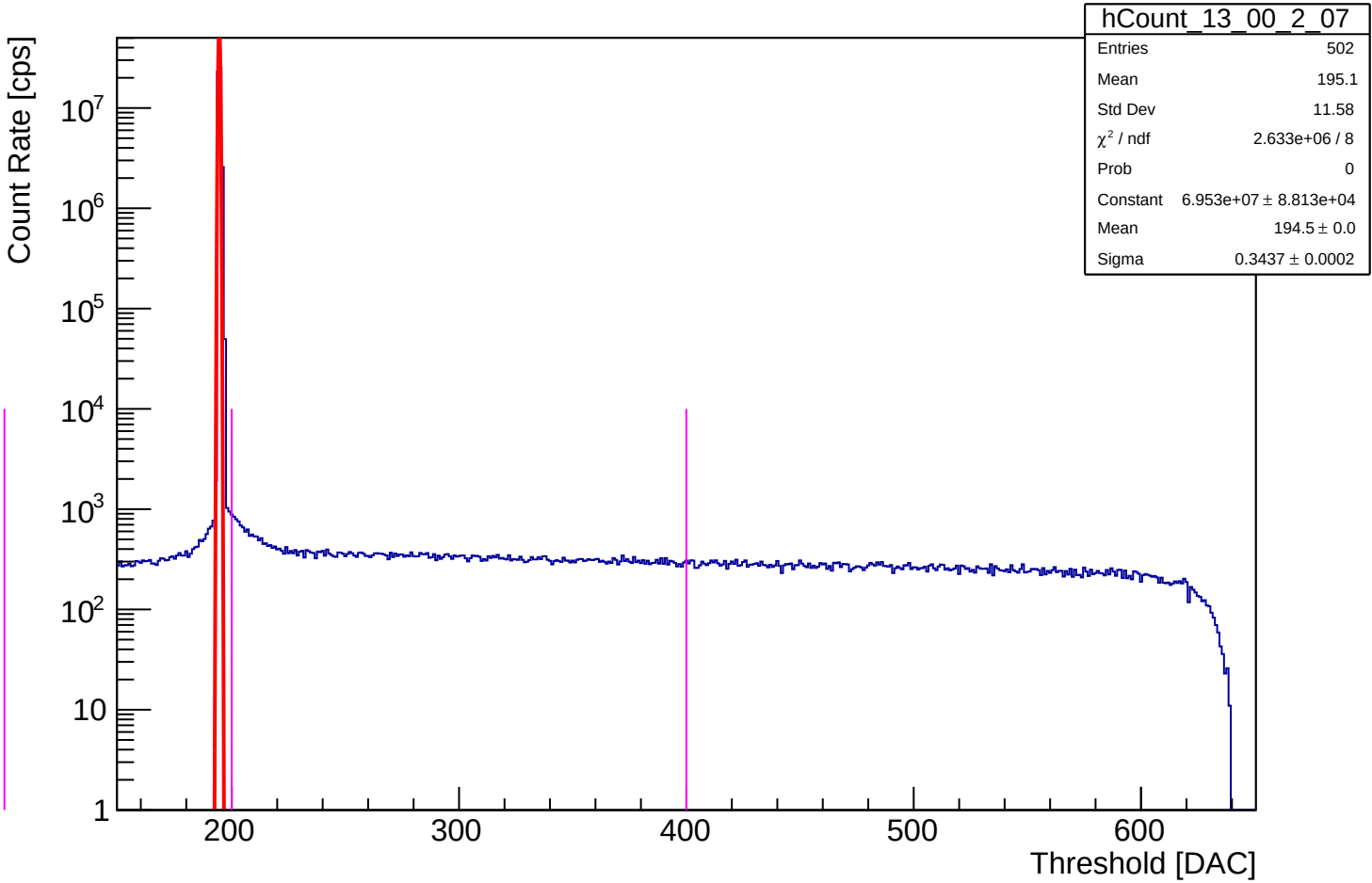


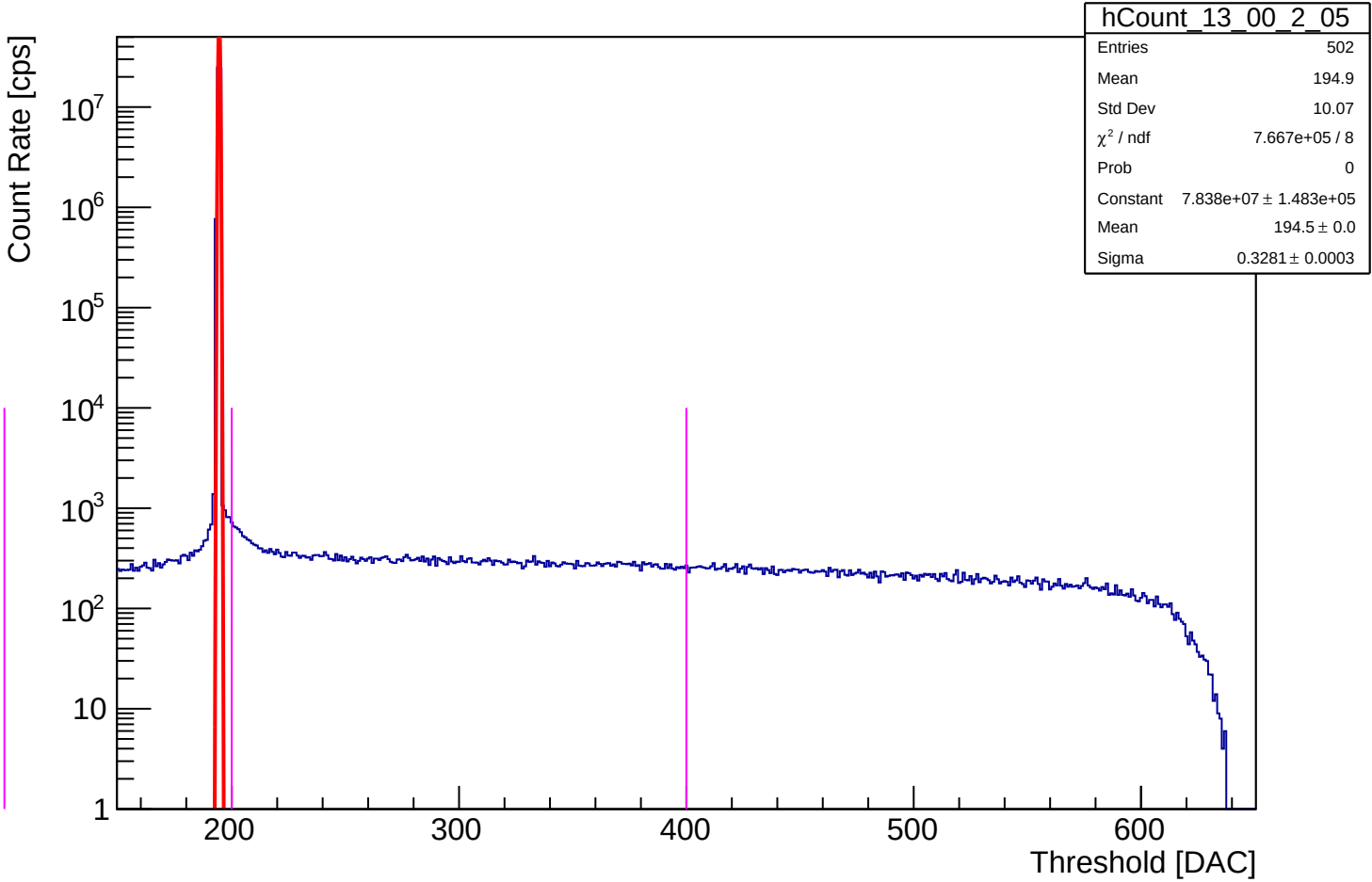
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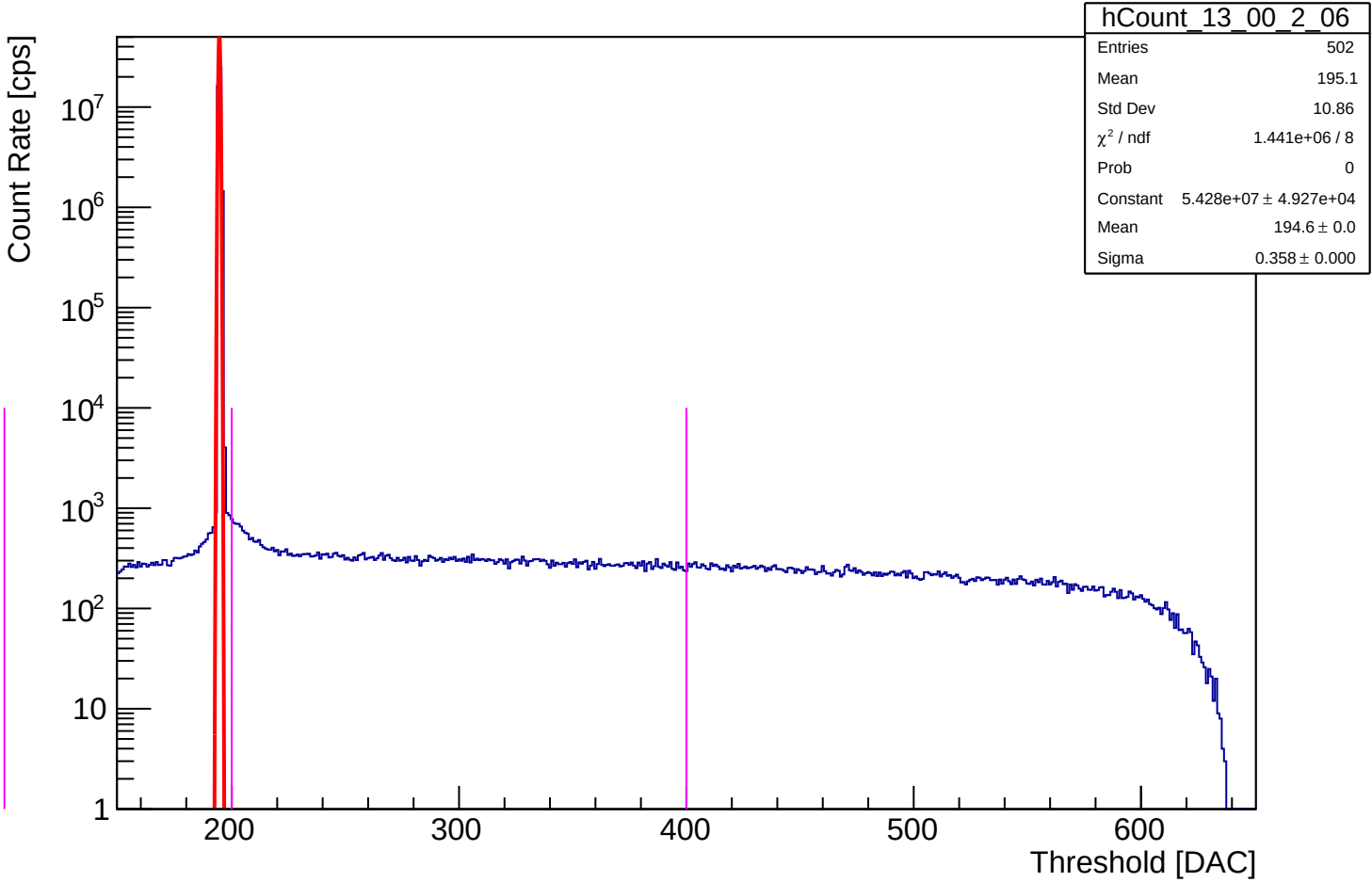


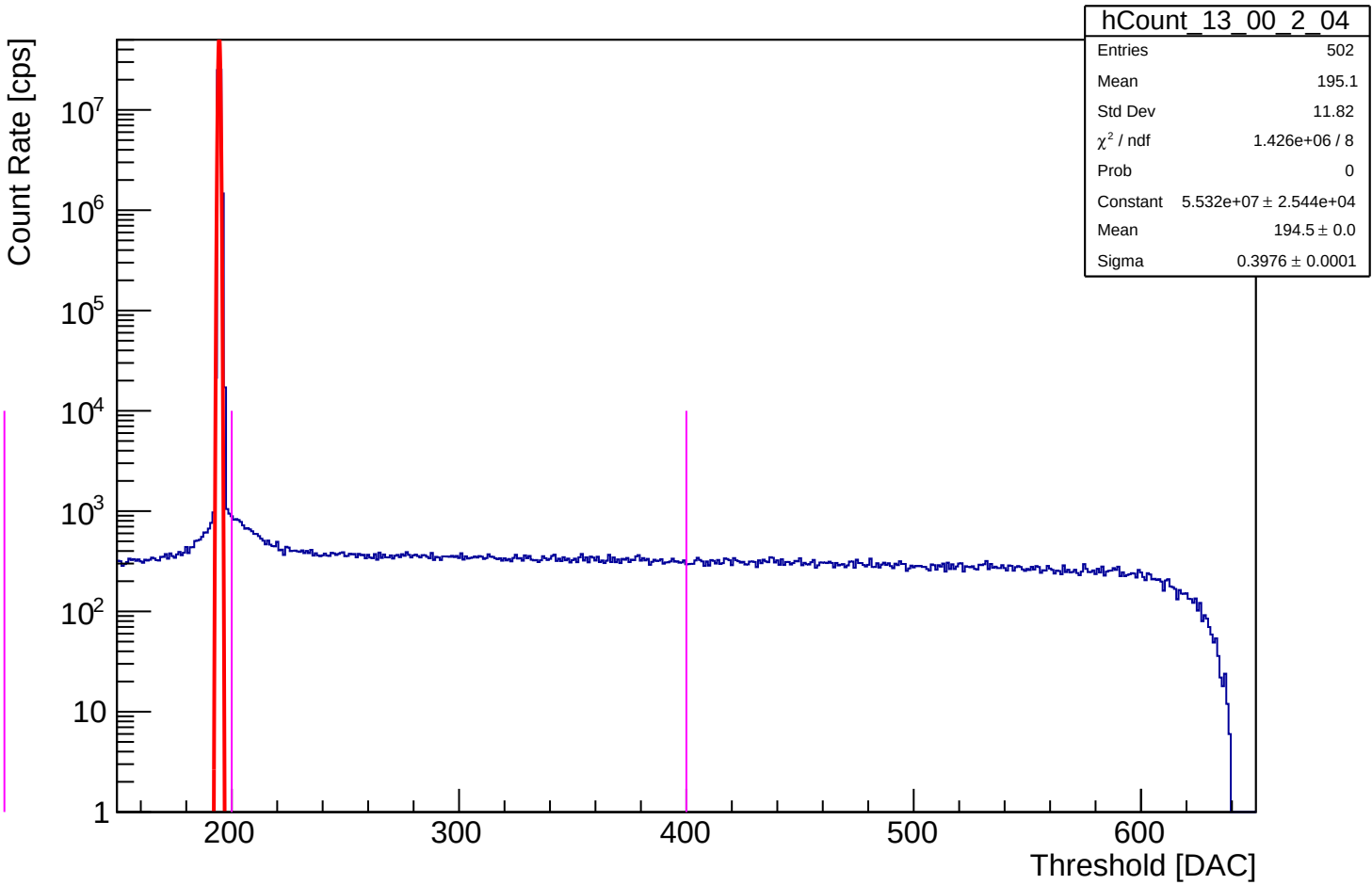
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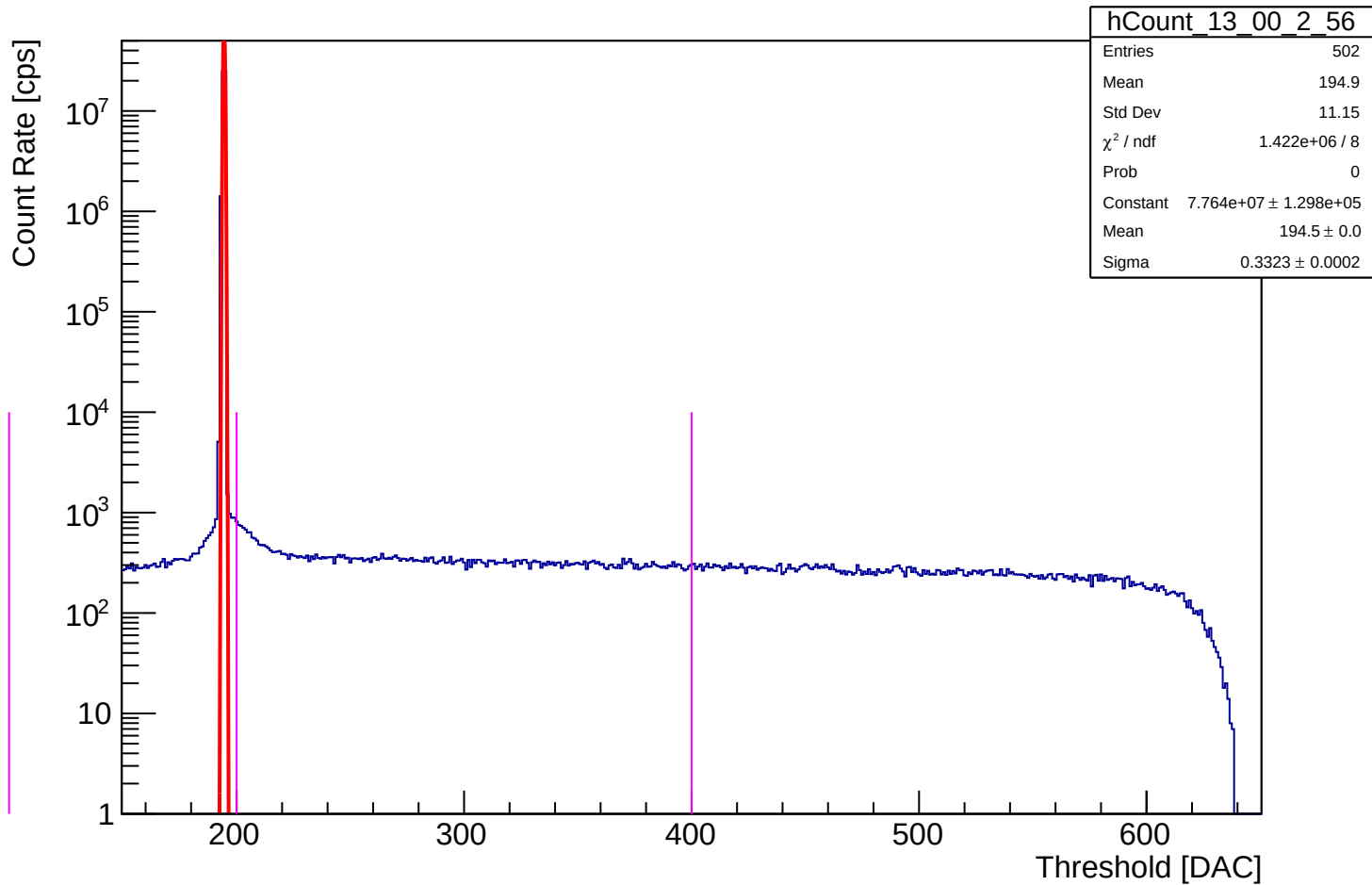




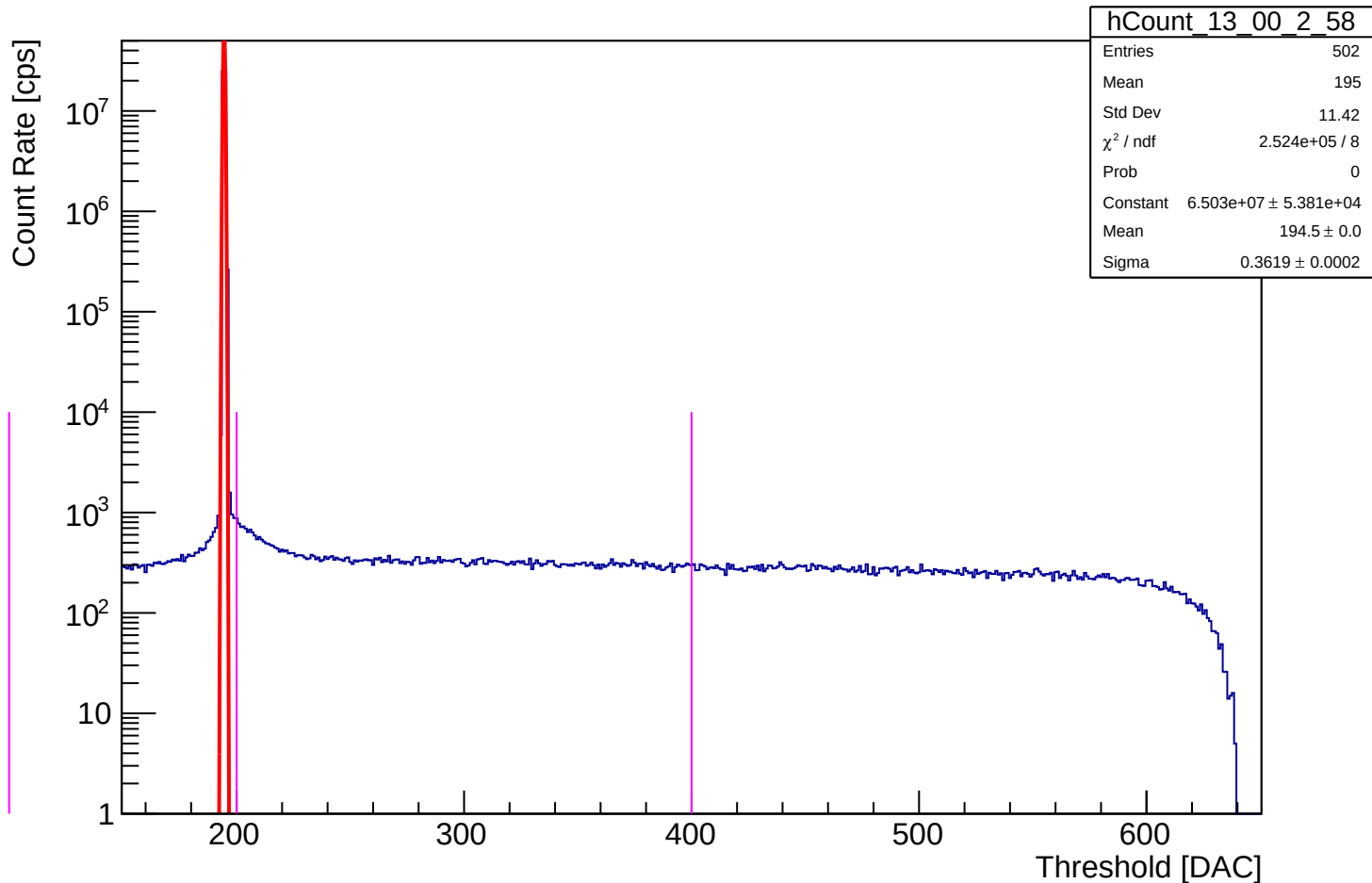




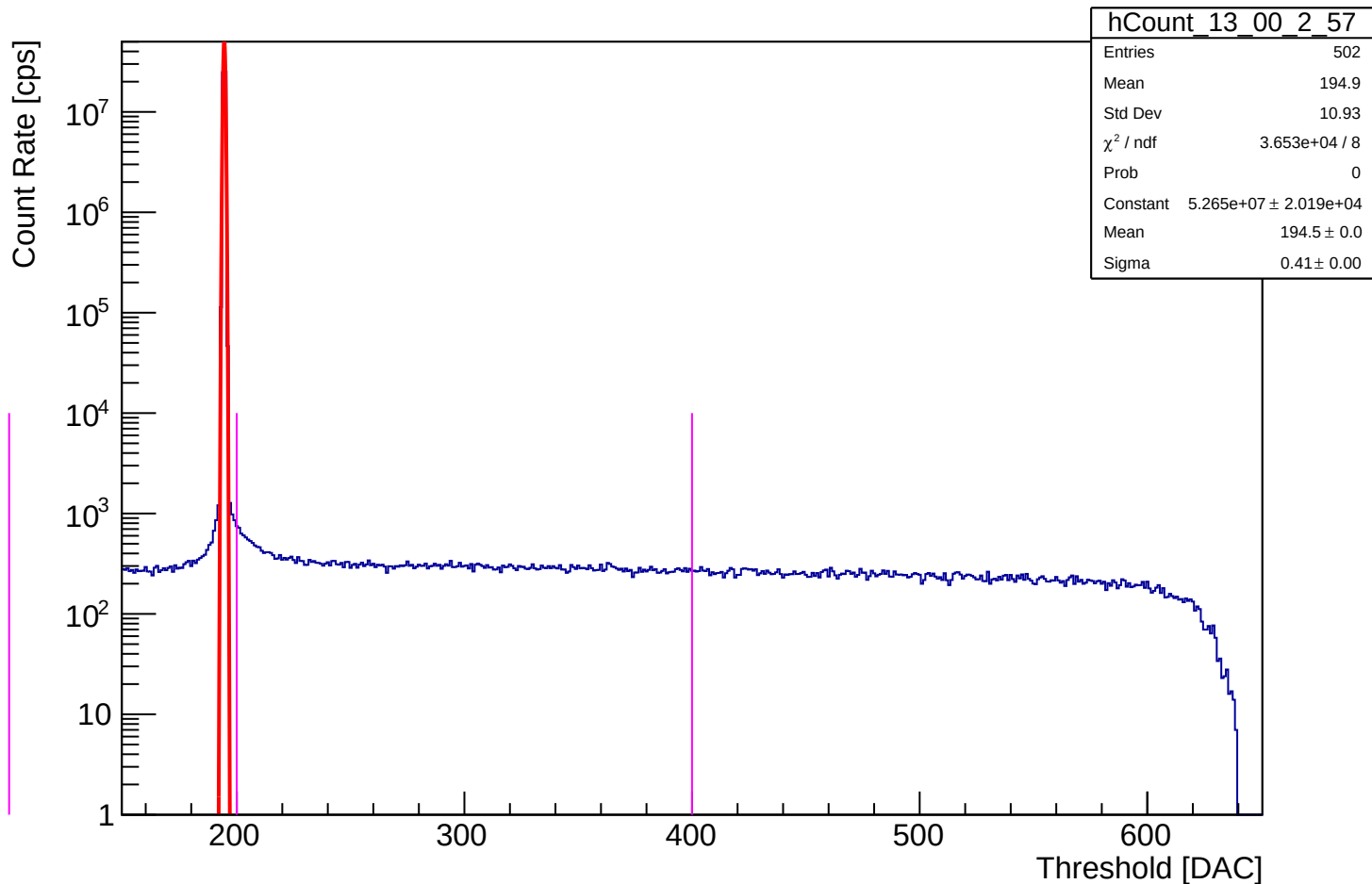
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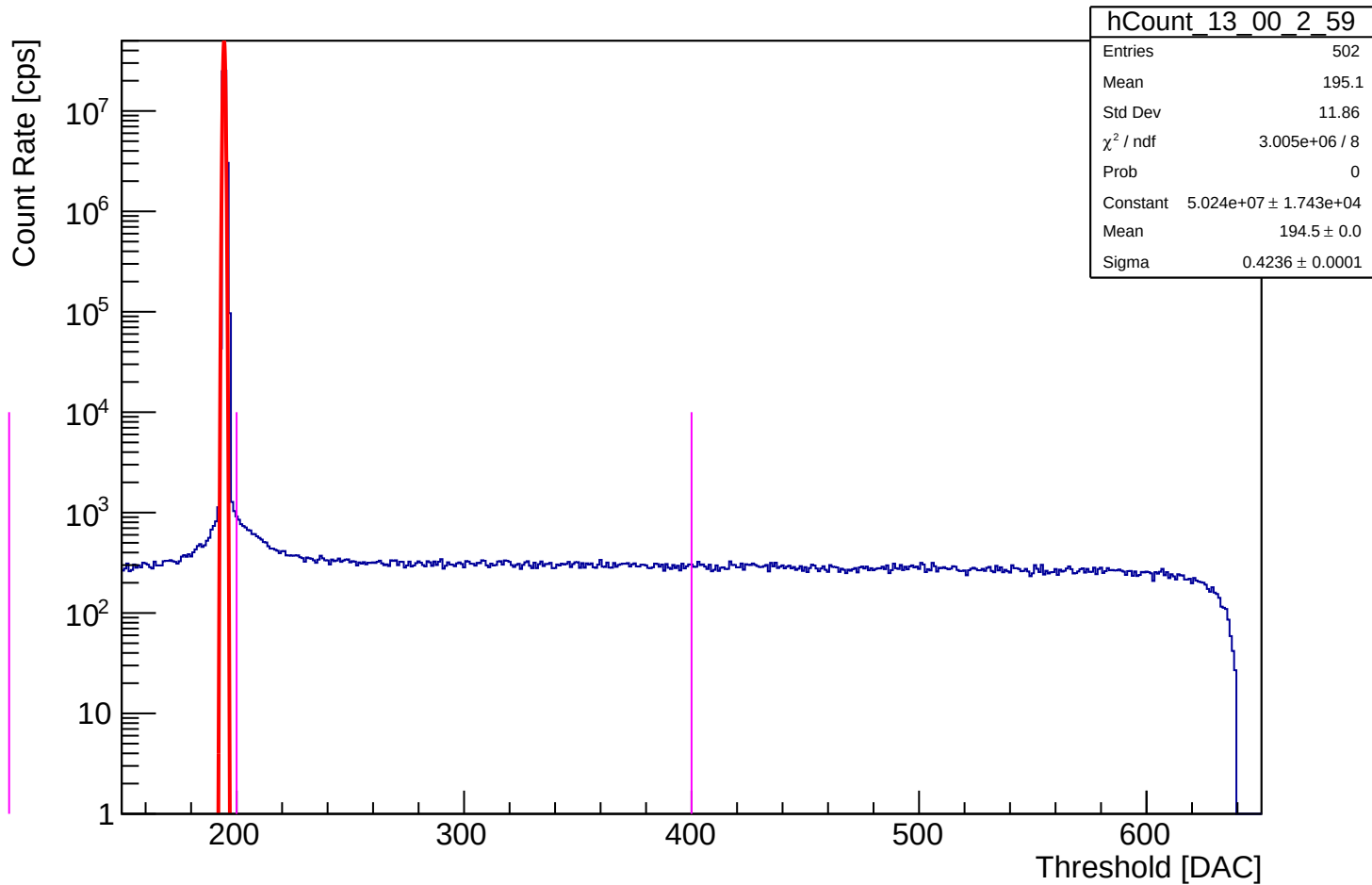
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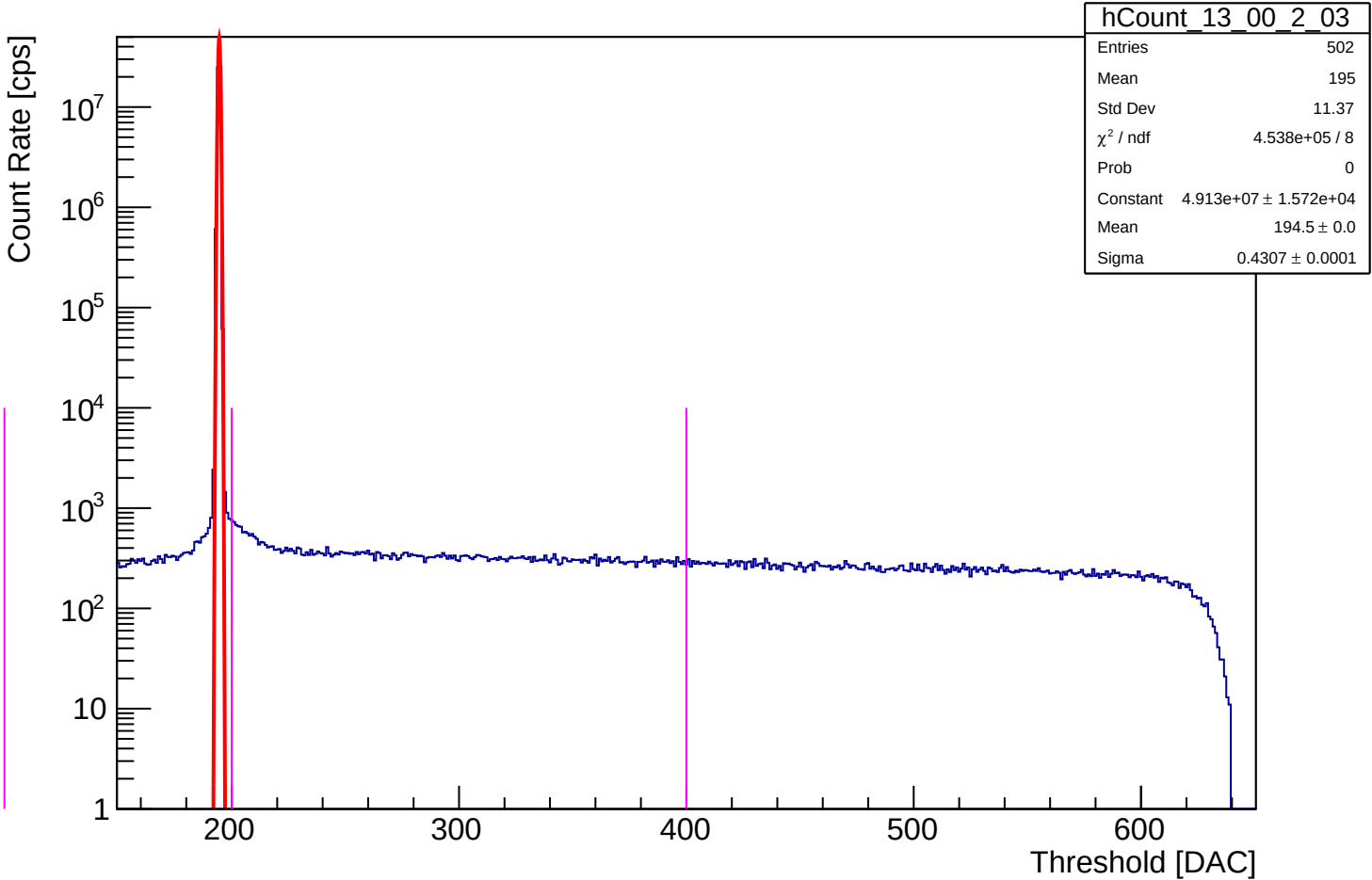


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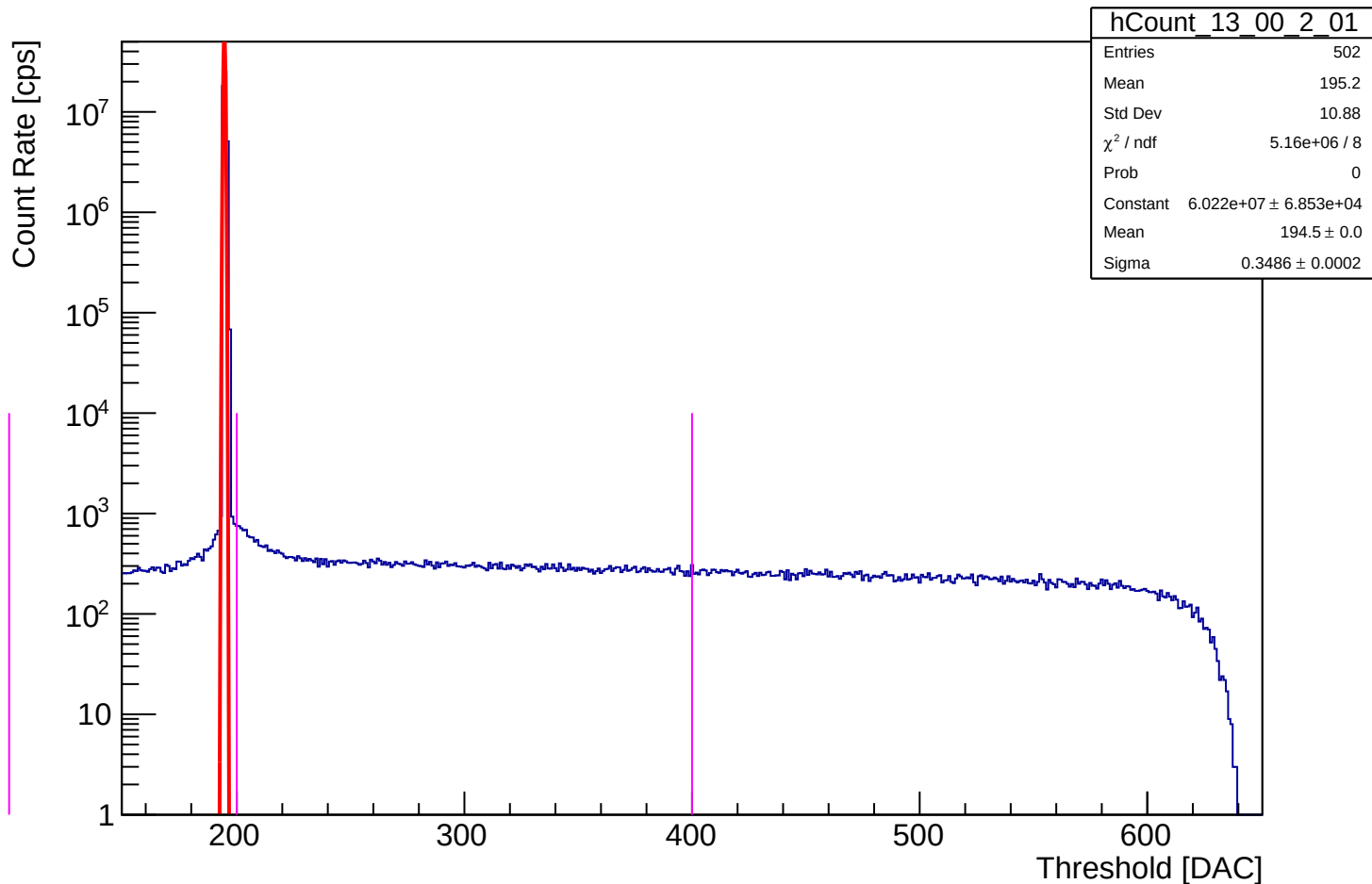


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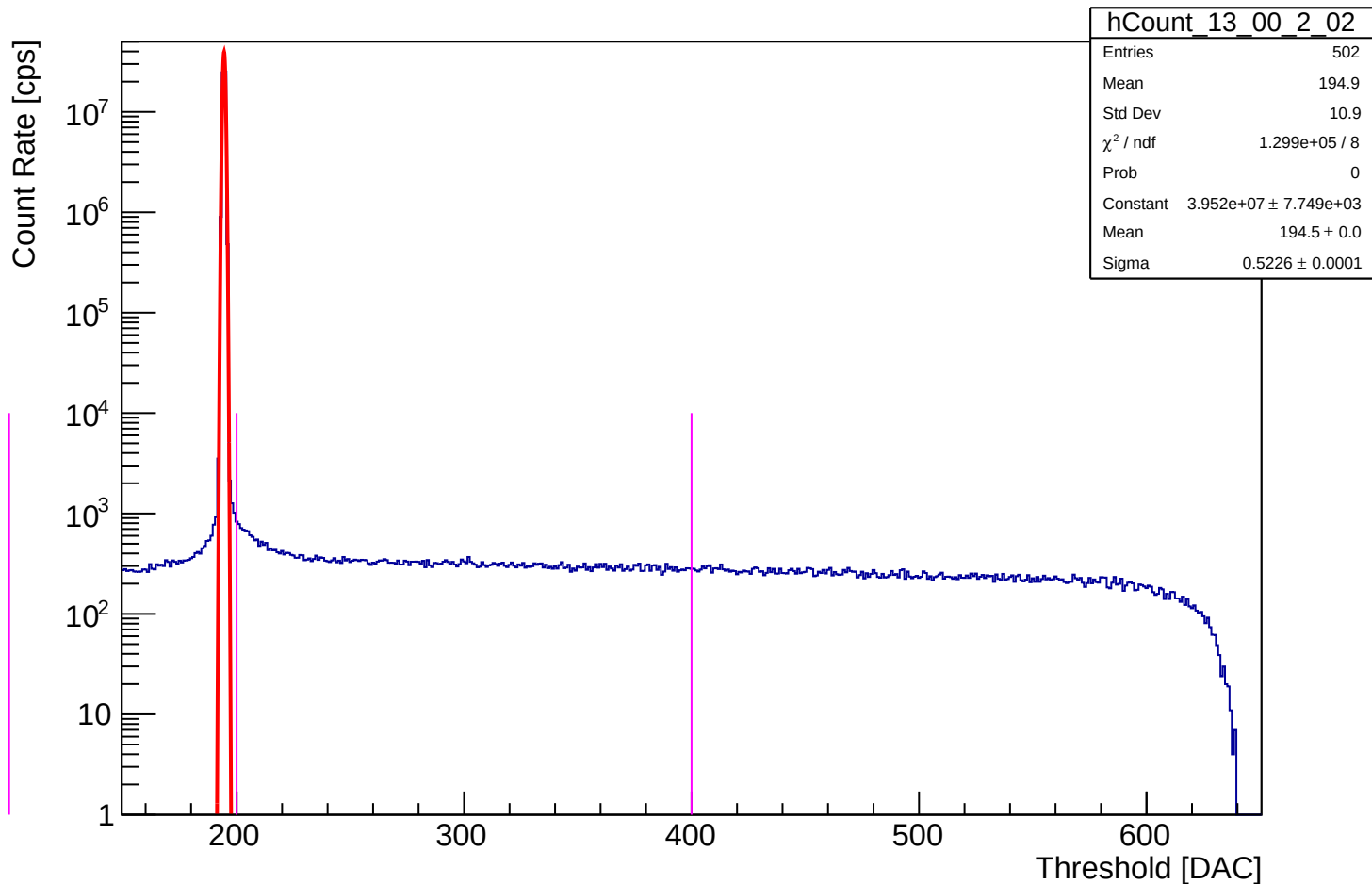


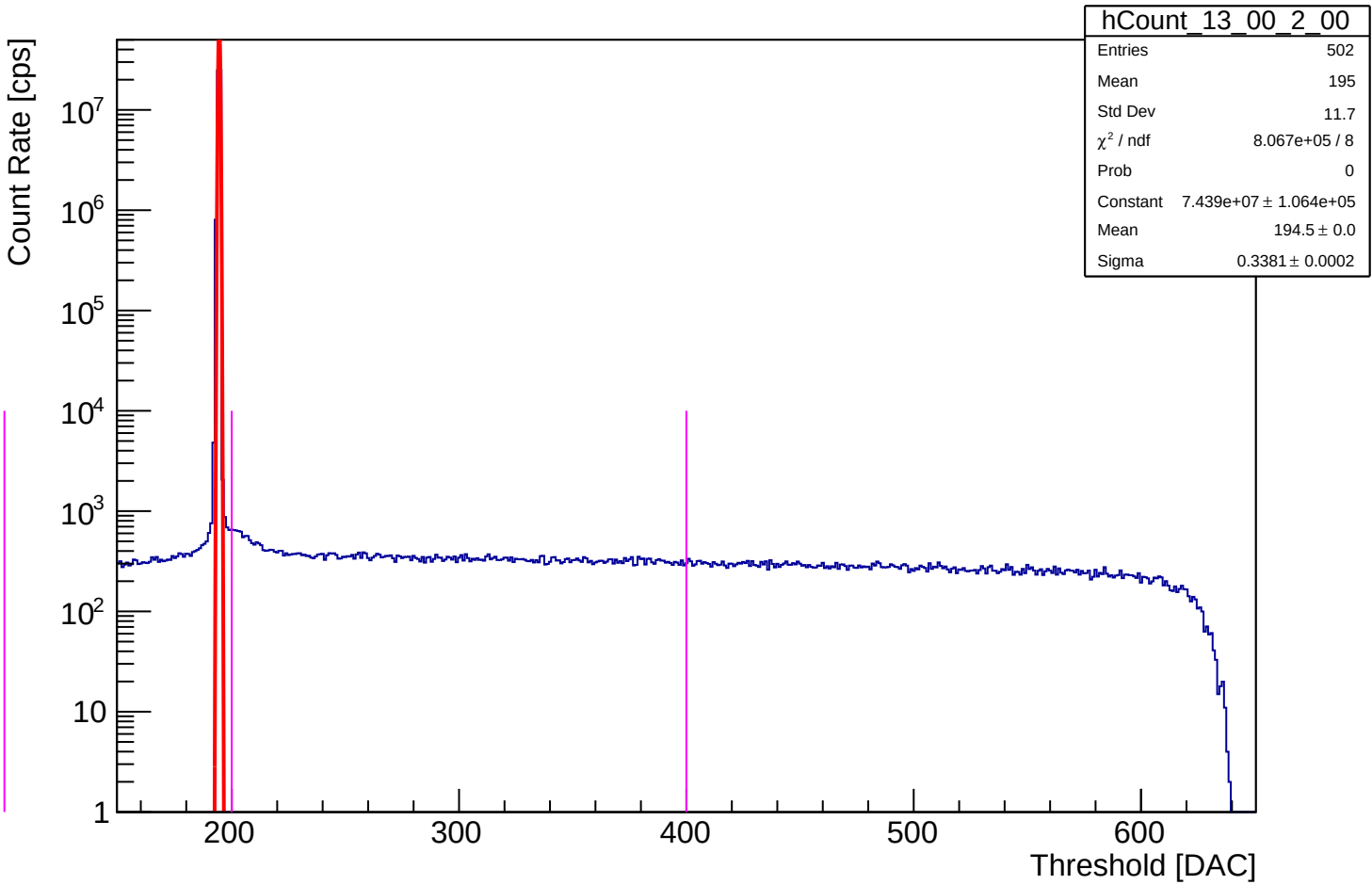


Row 1 Tile 1 Pmt 3 Pixel 58 Slot 13 Fiber 0 Asic 2 Channel 1

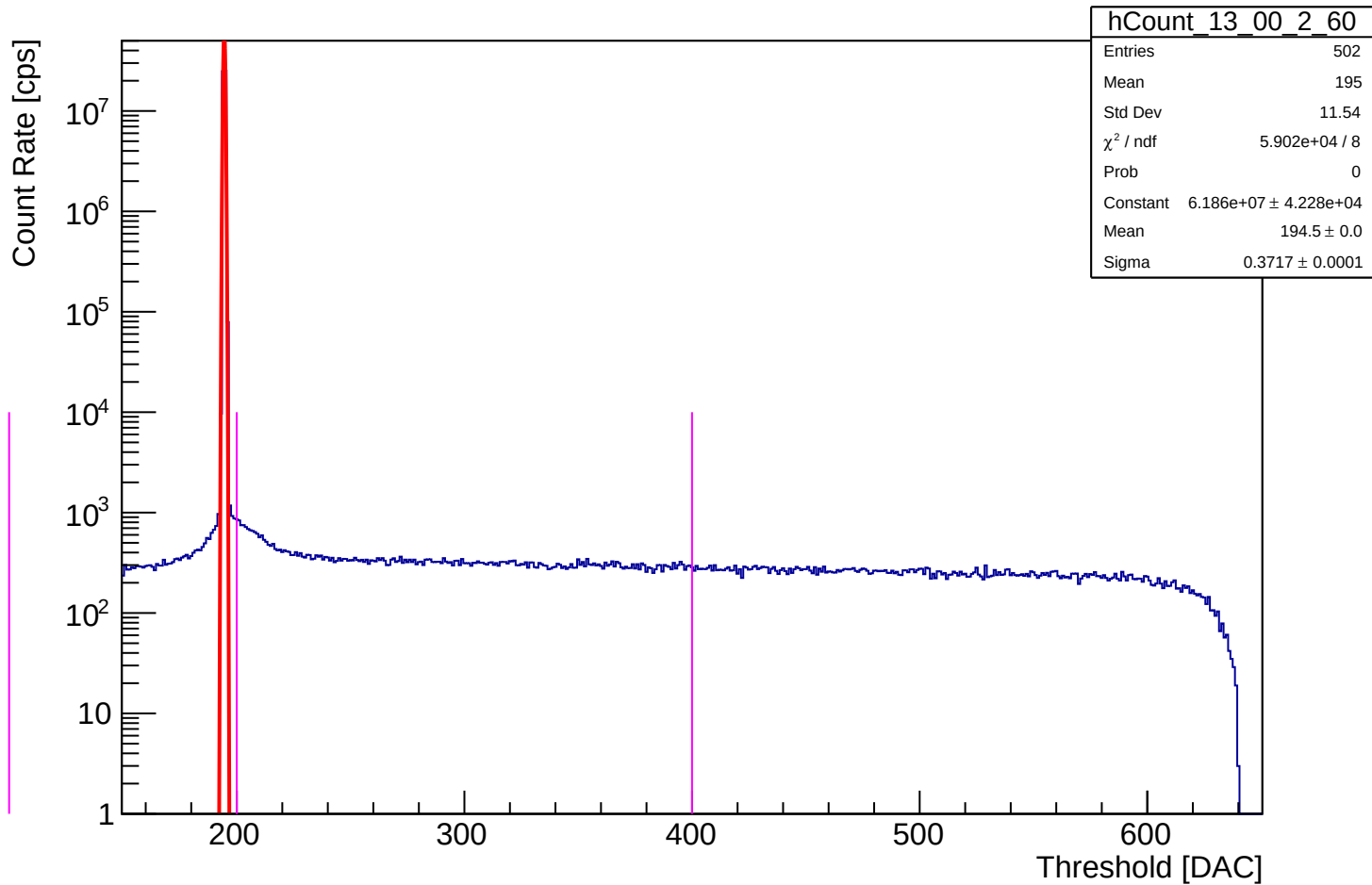


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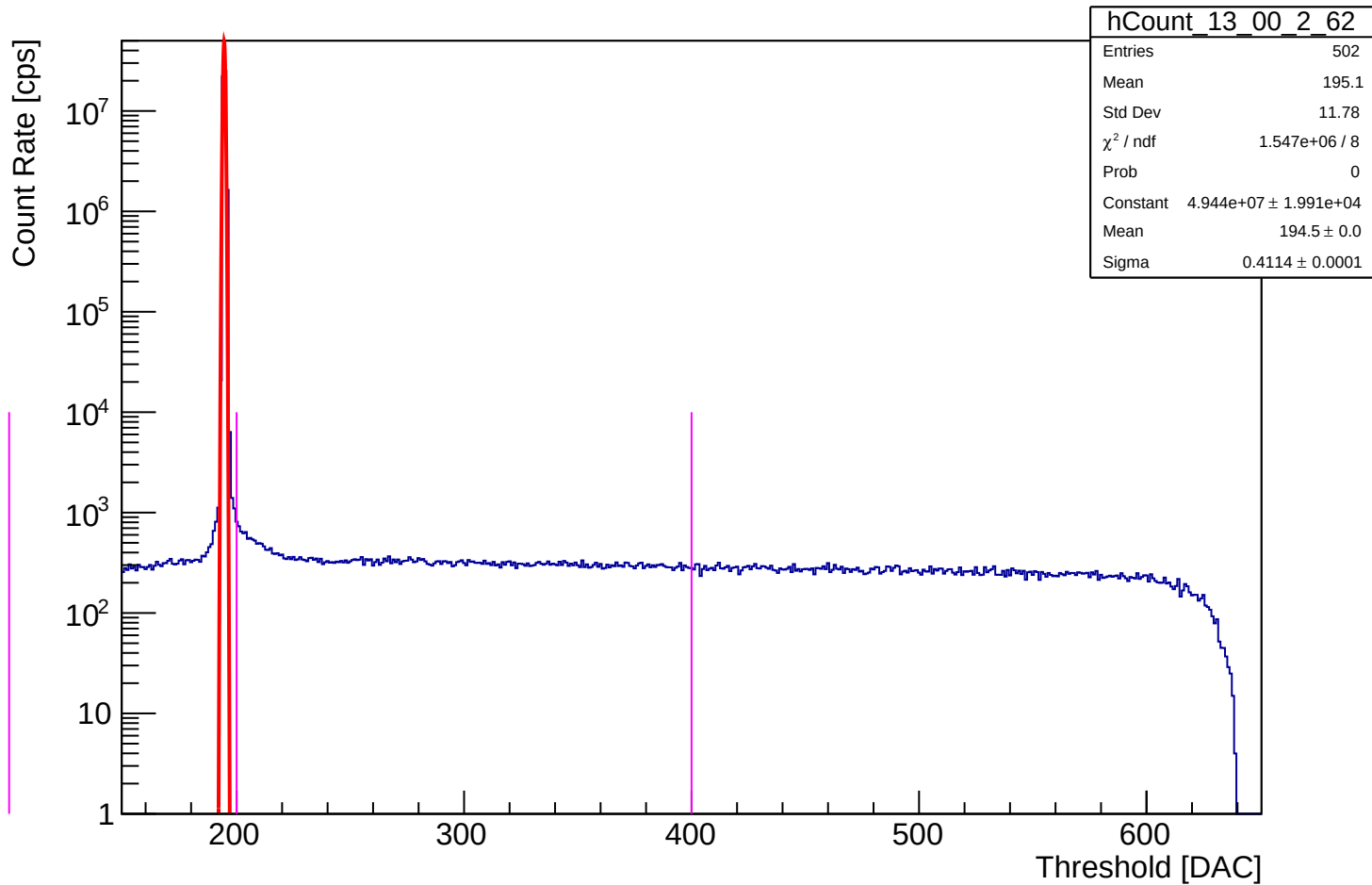




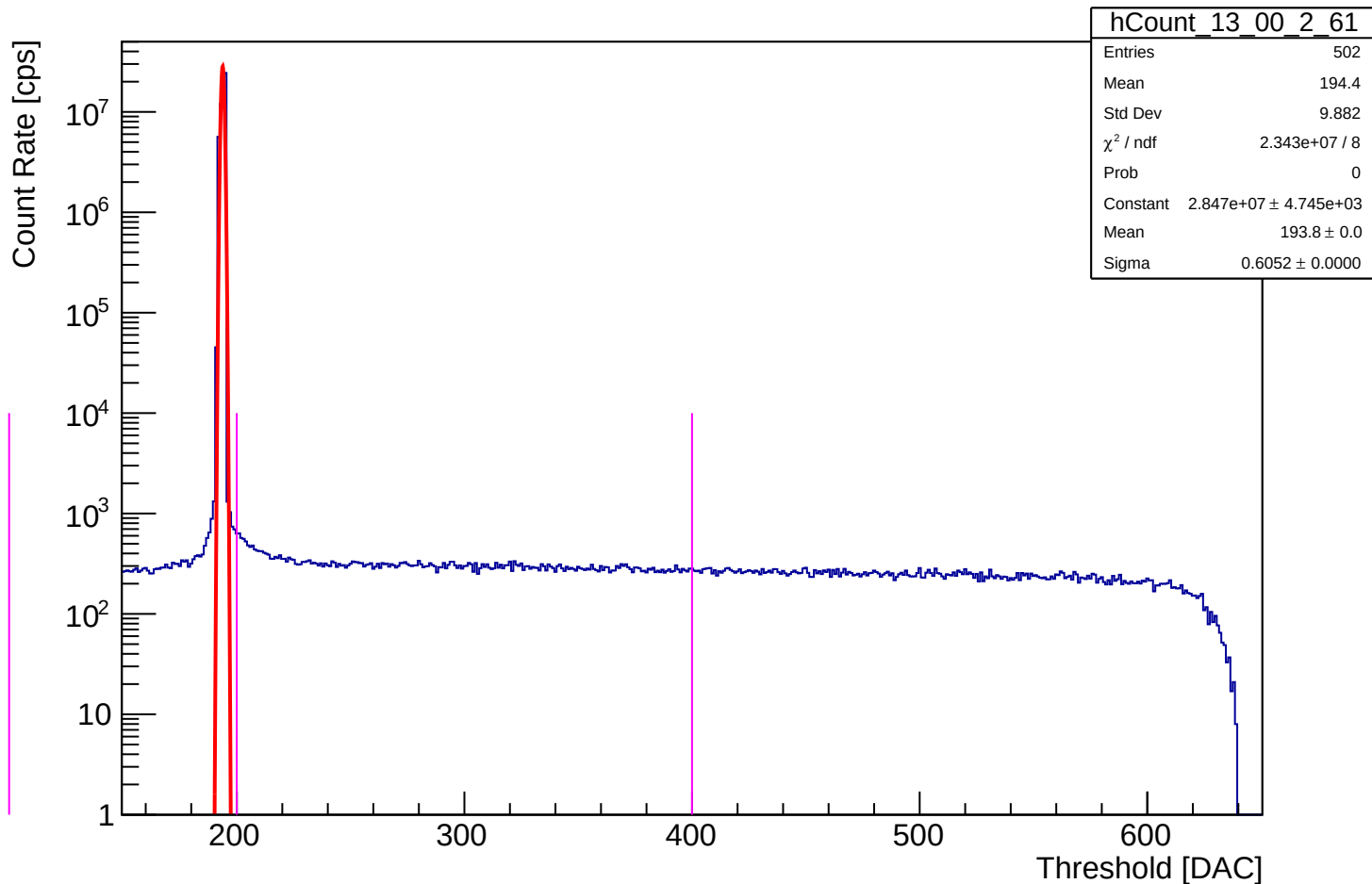
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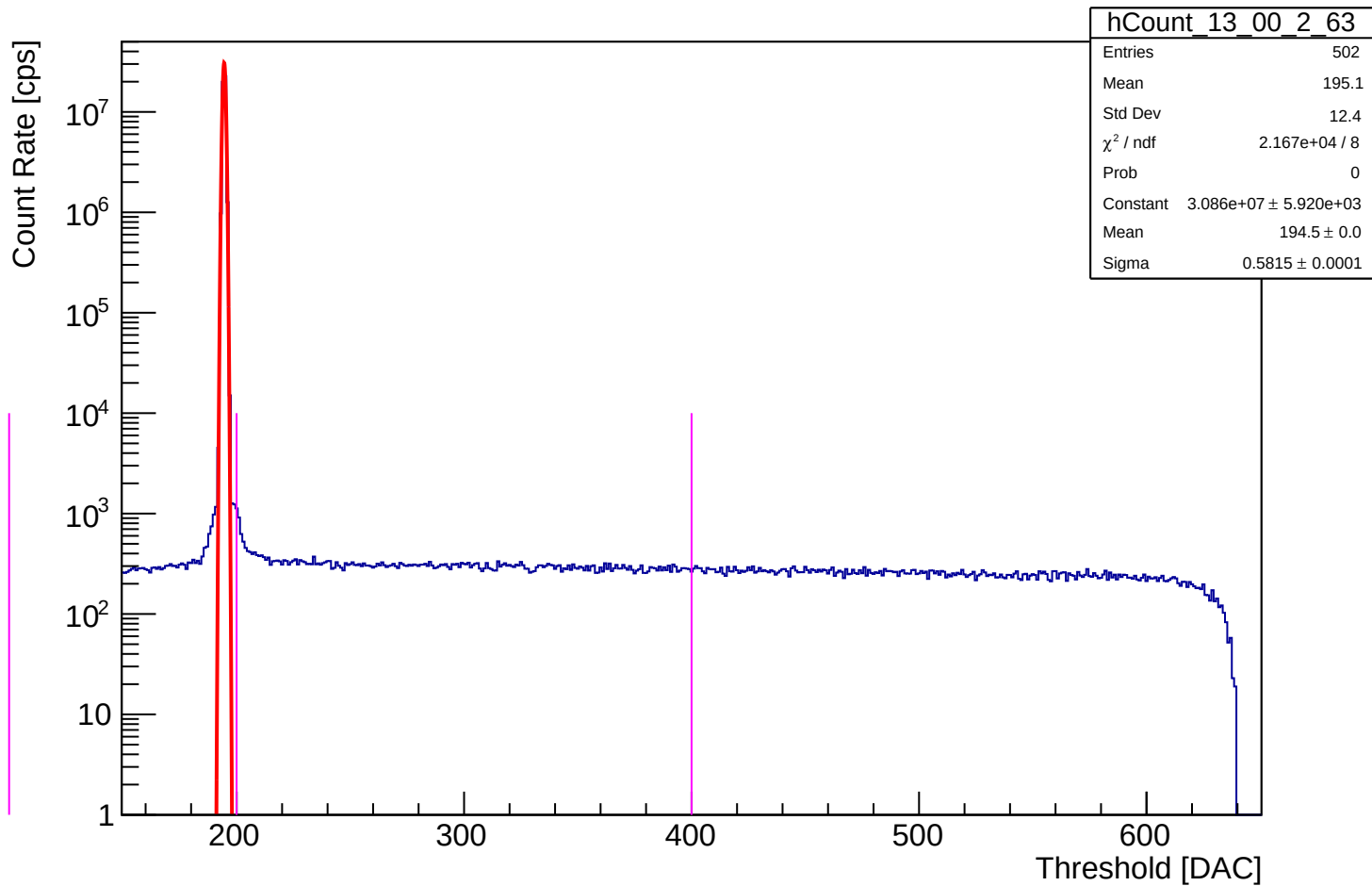
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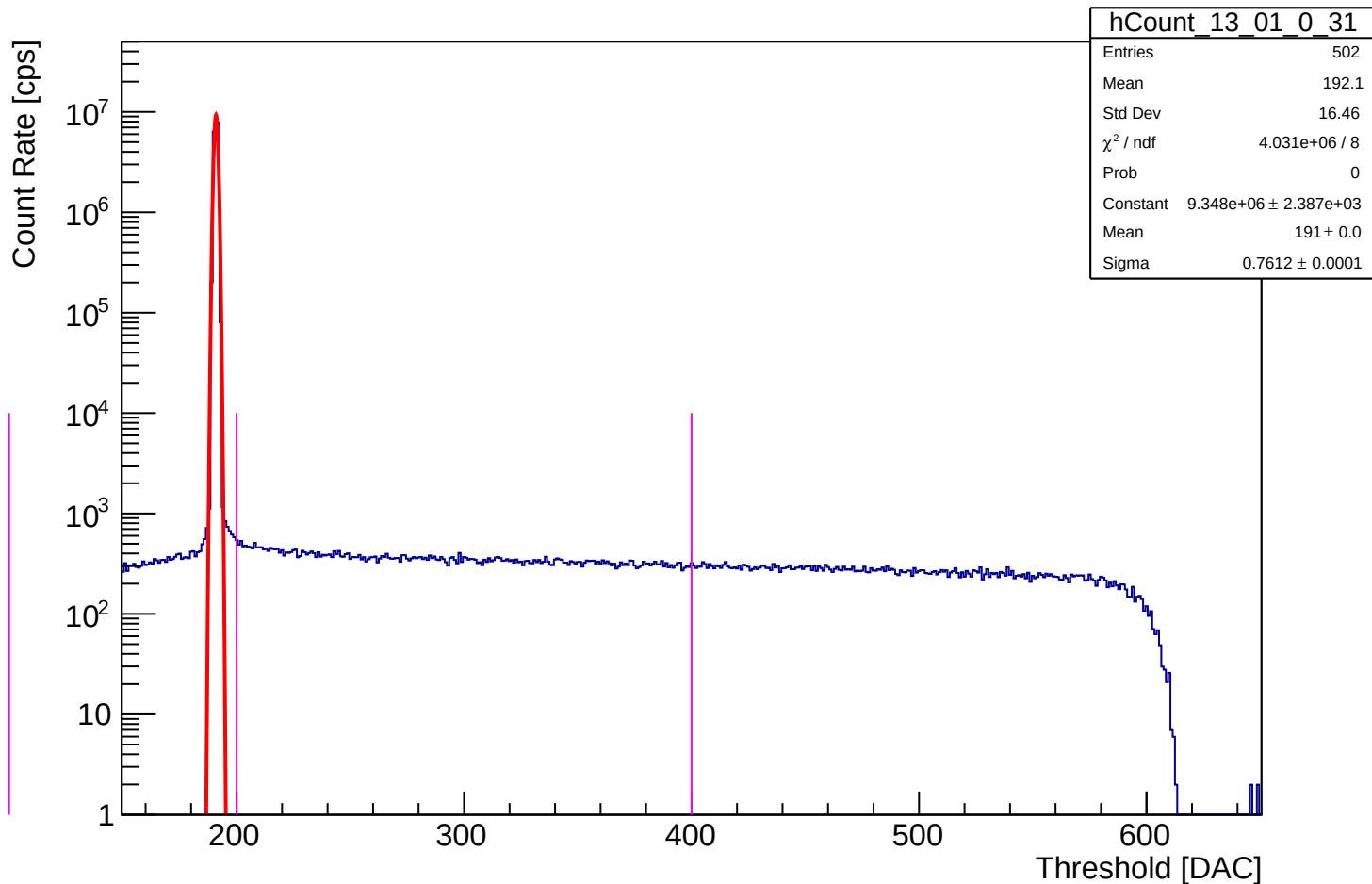
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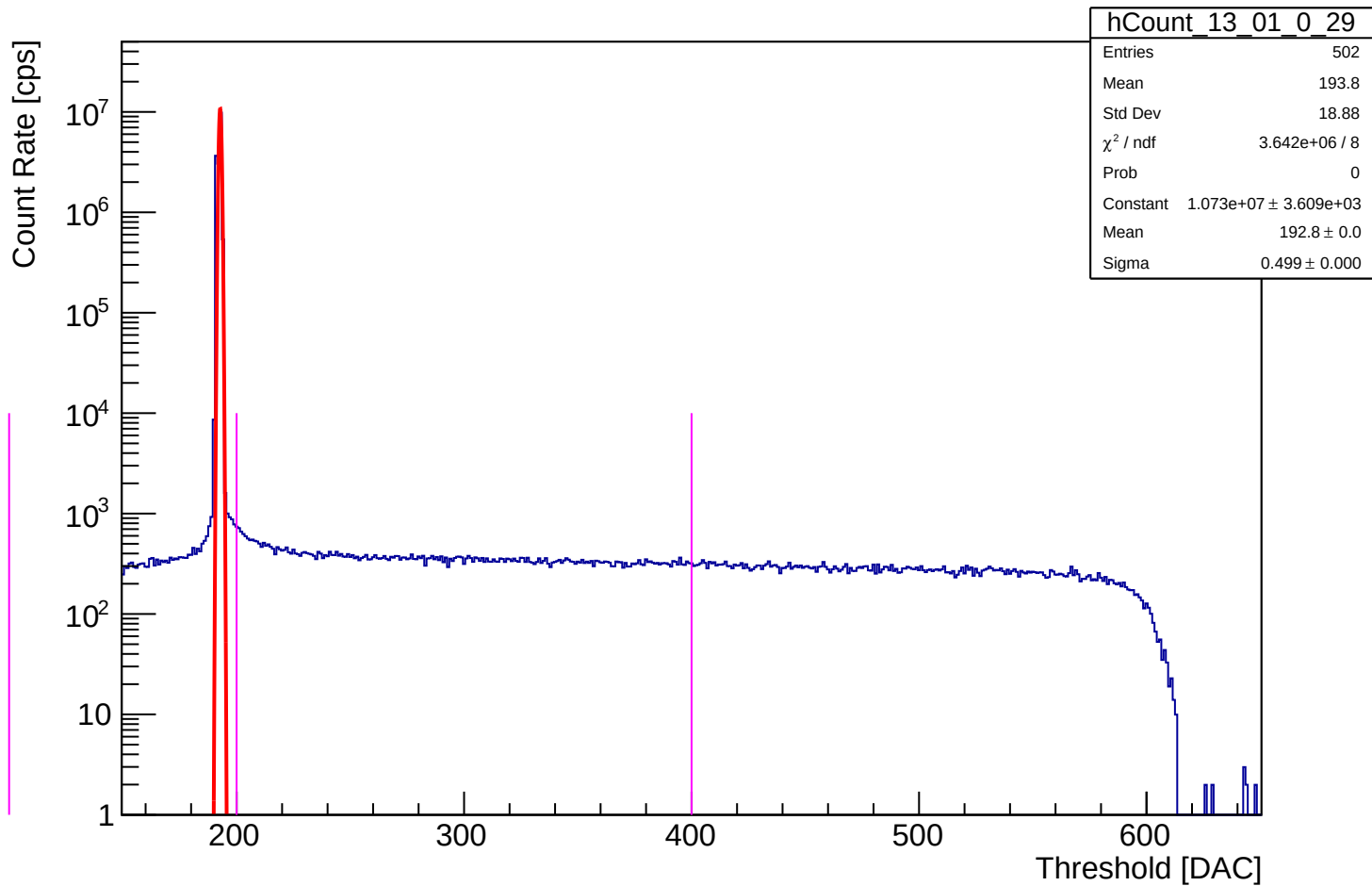
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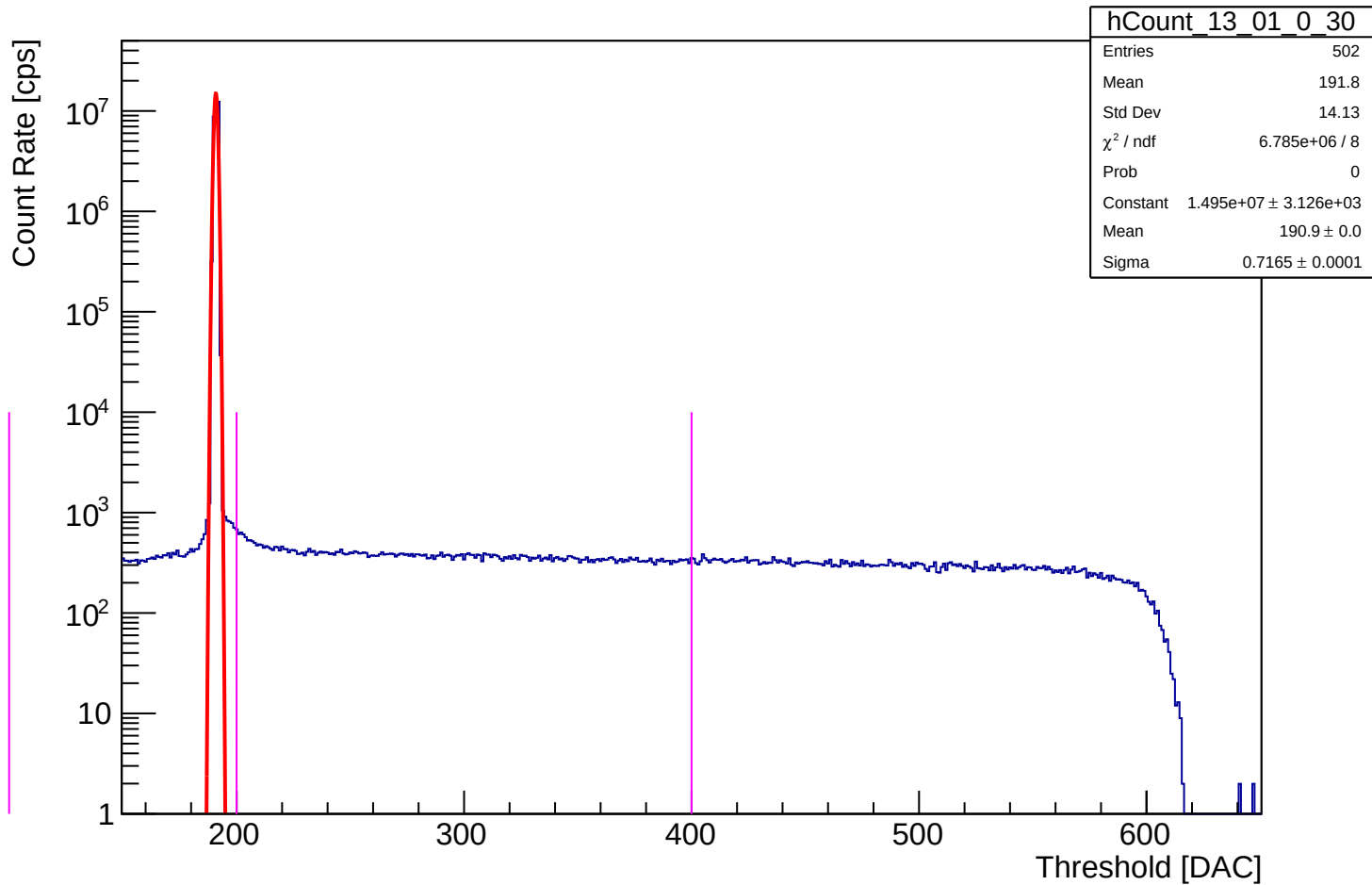
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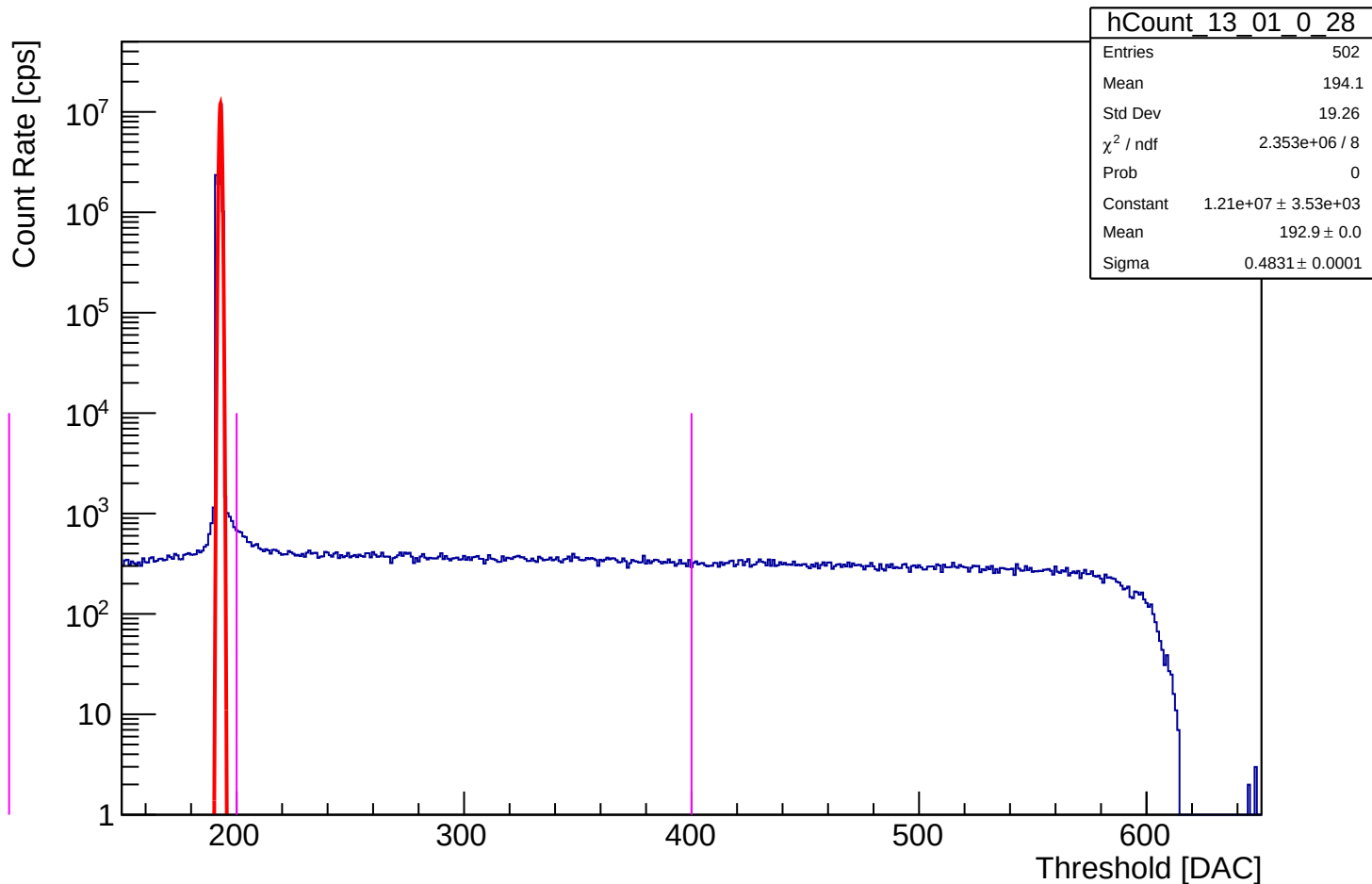
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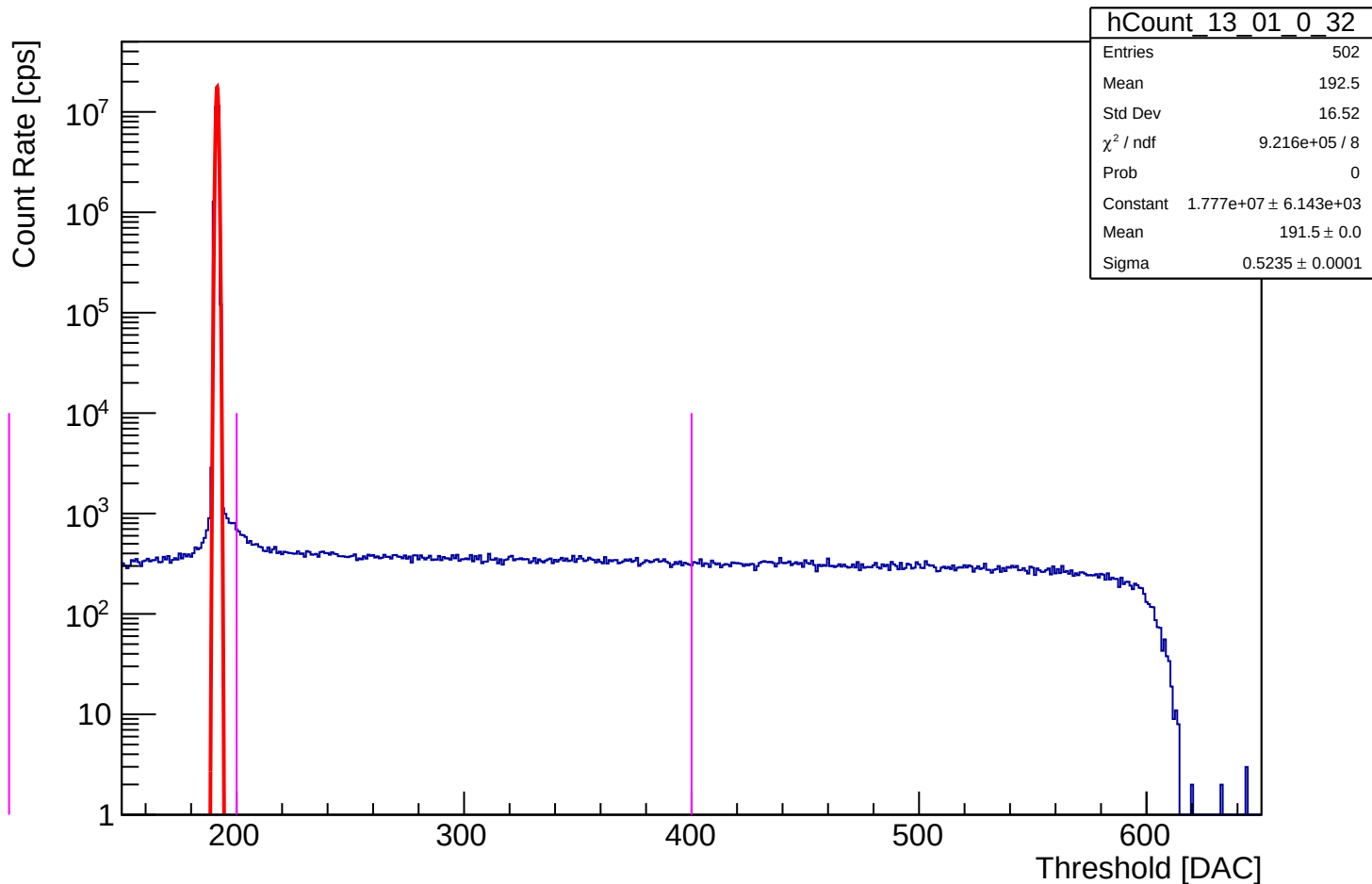
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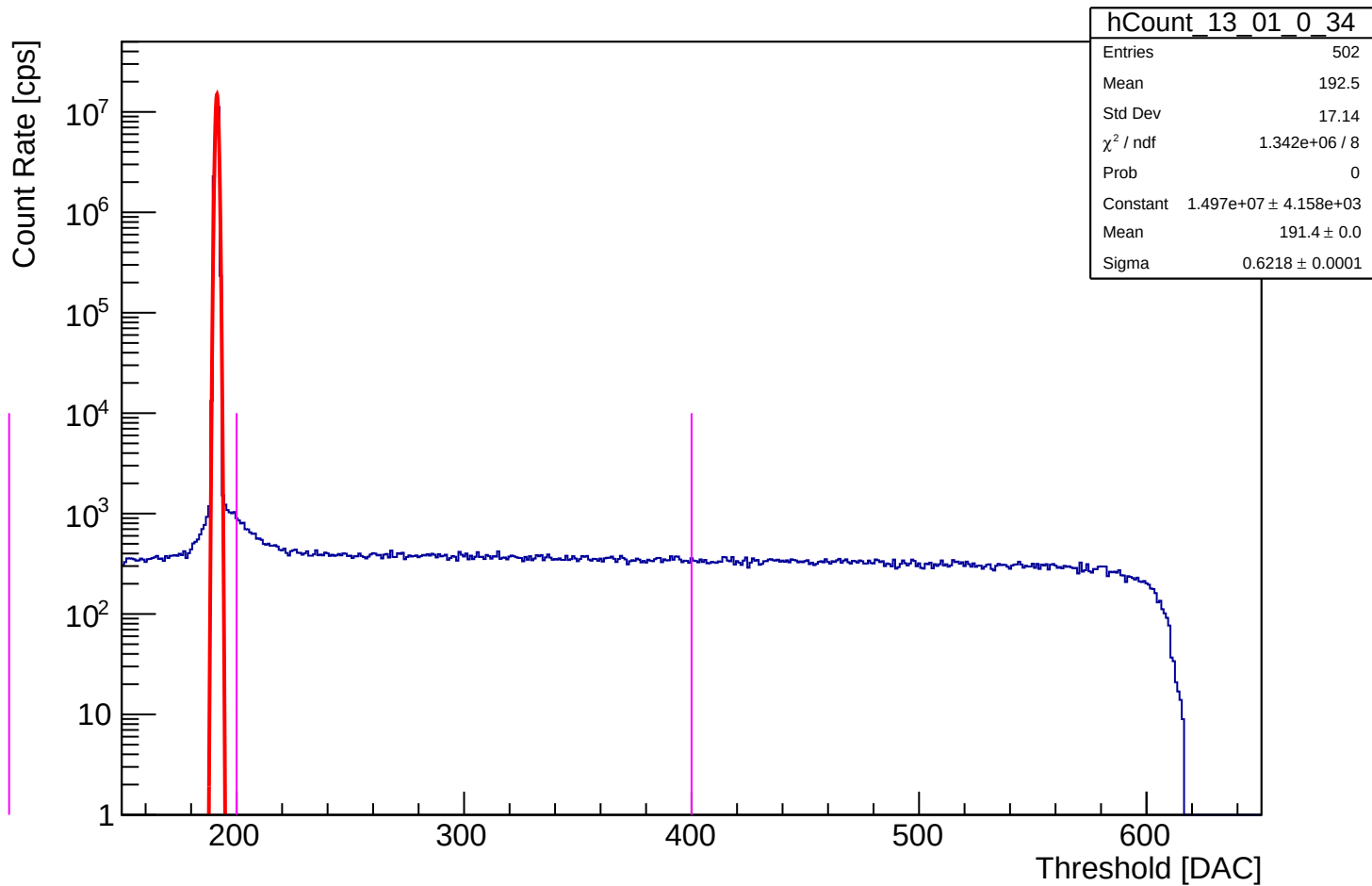
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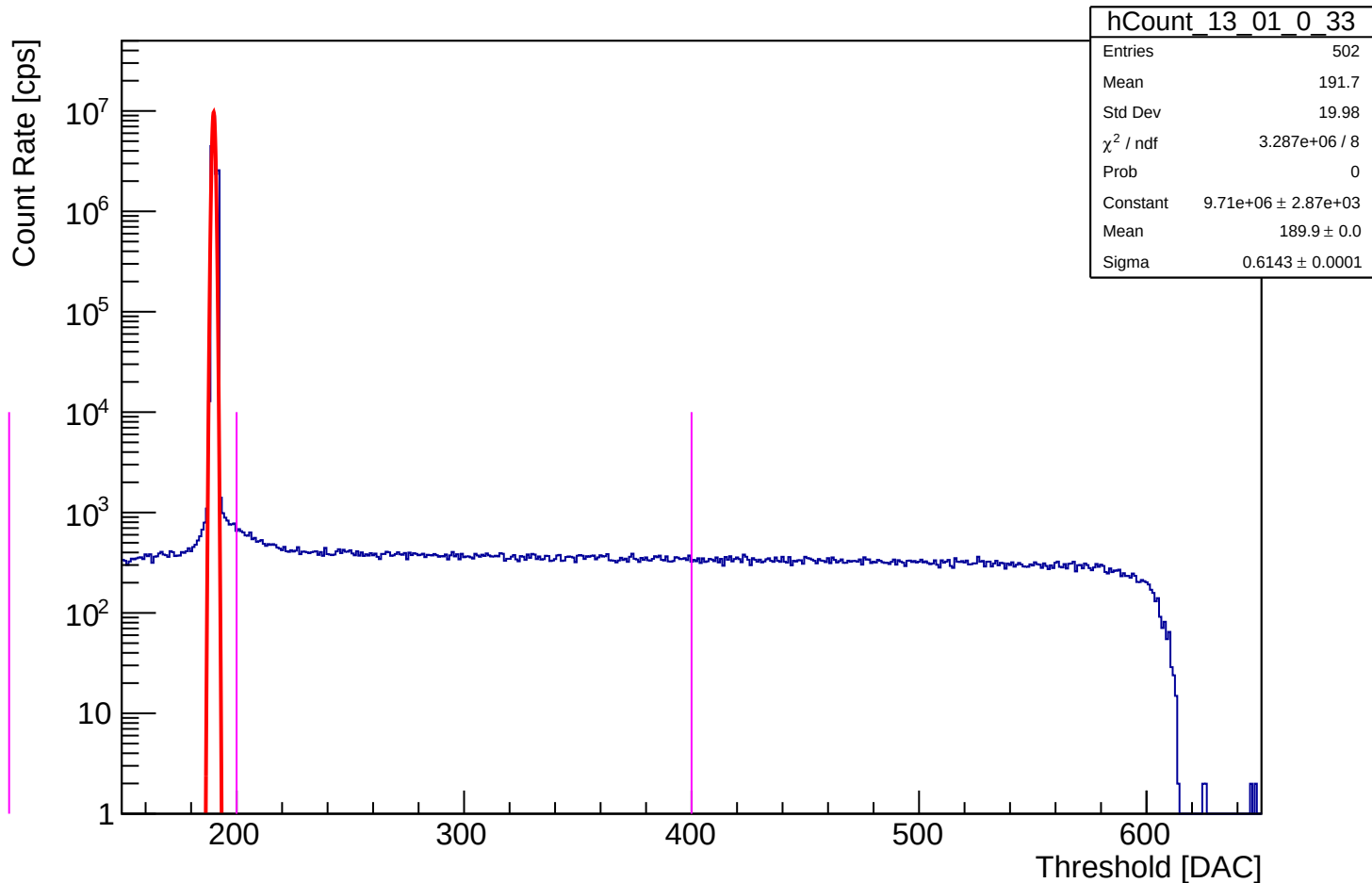
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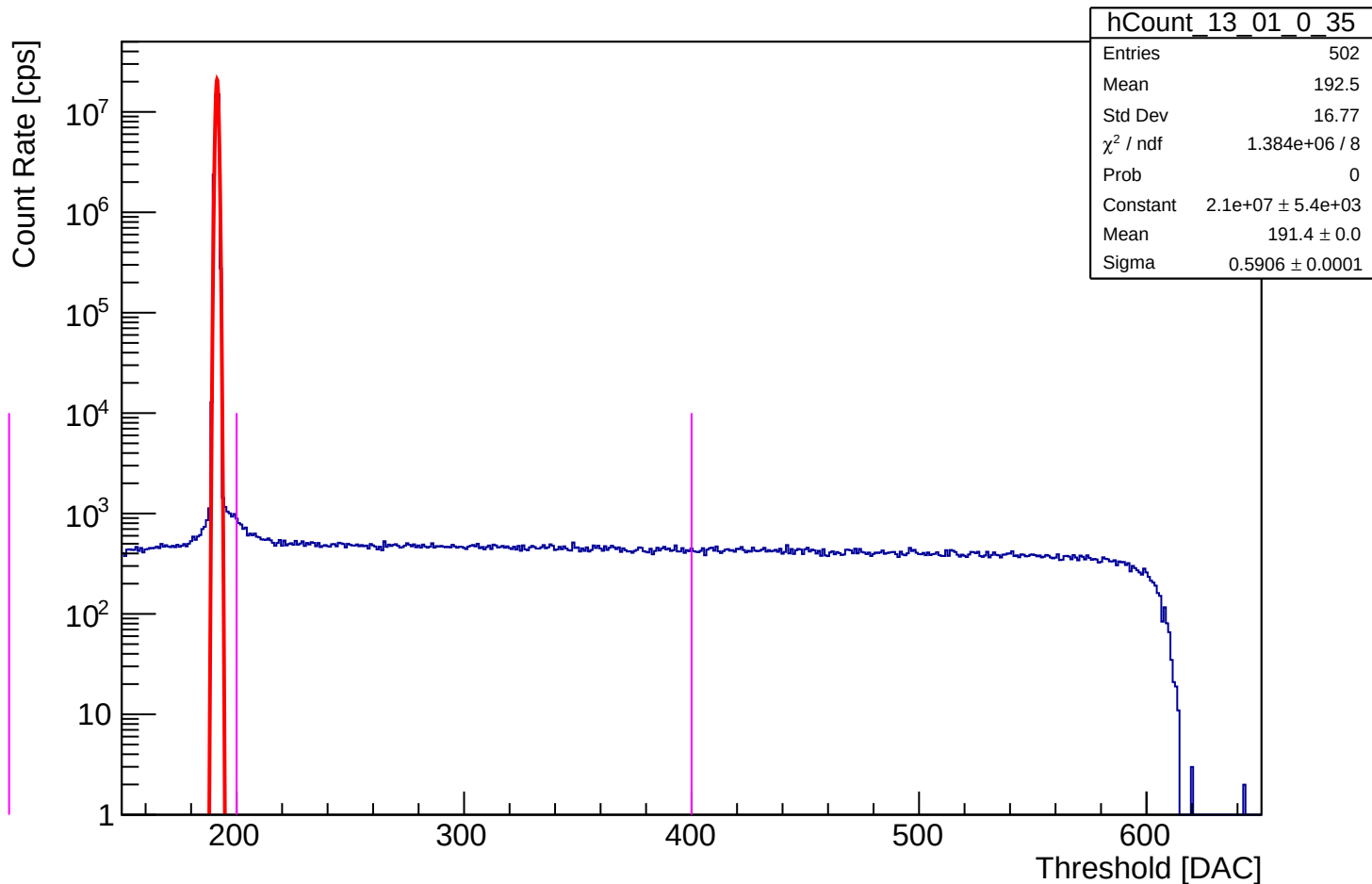
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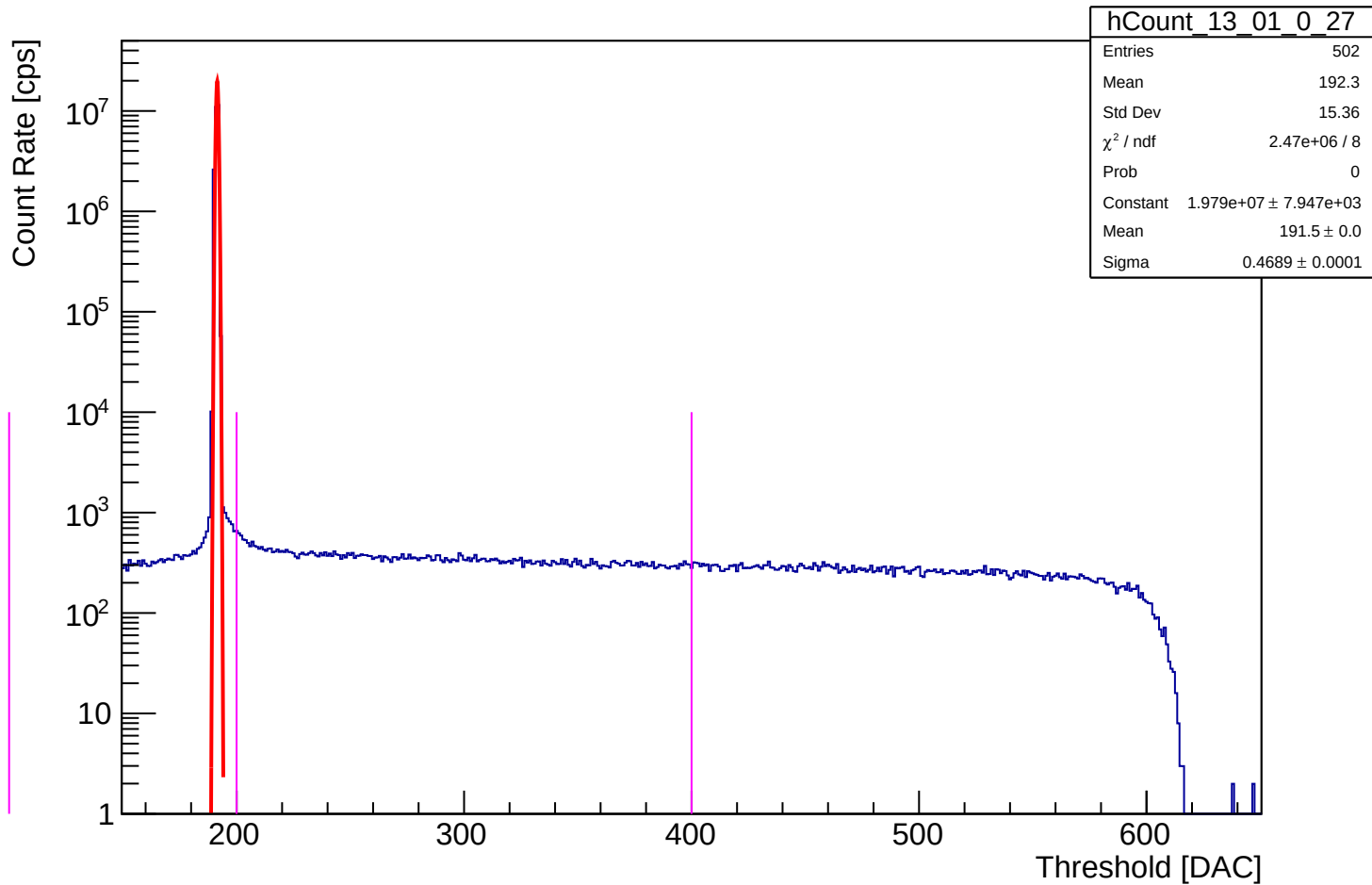
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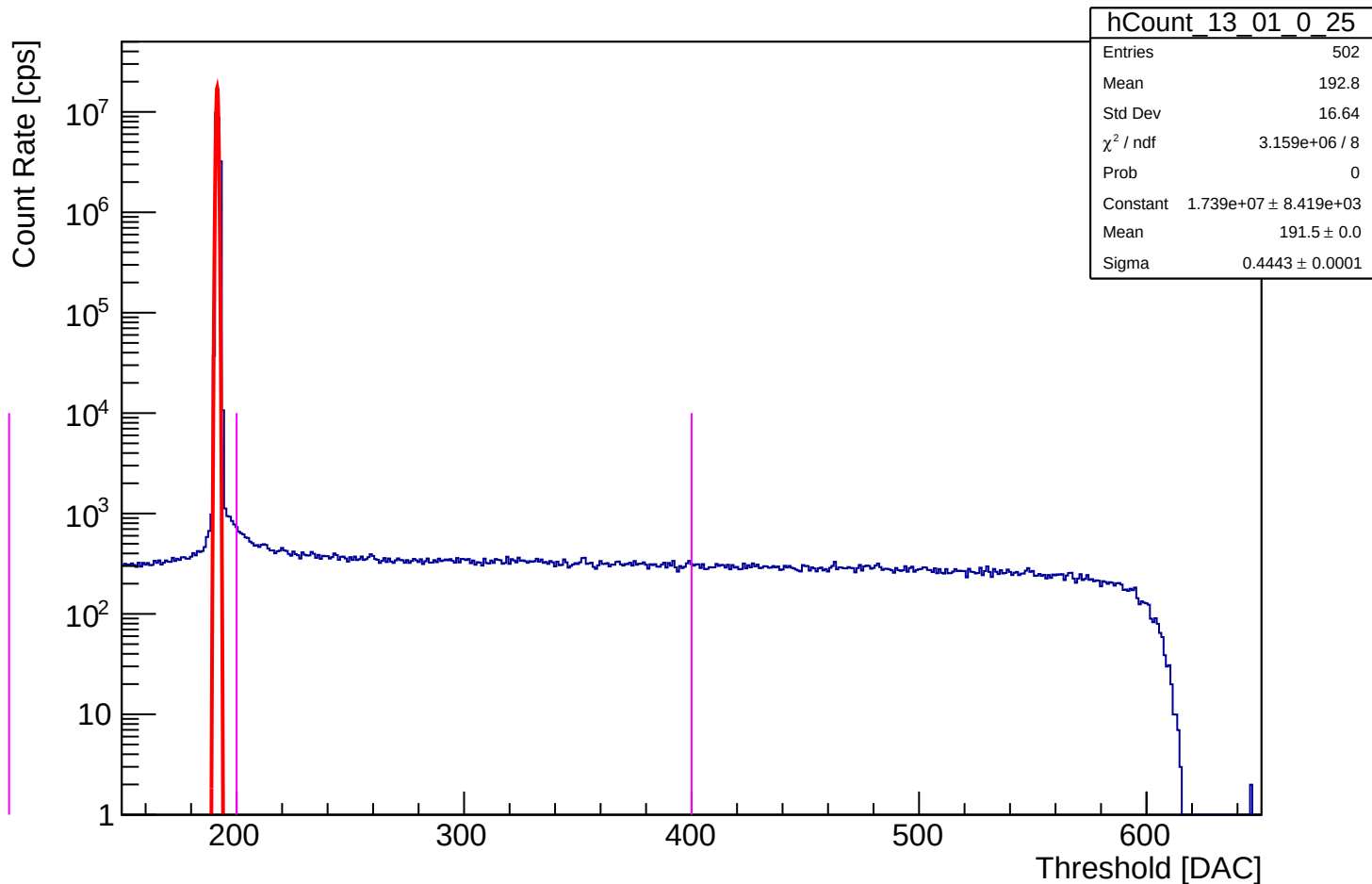
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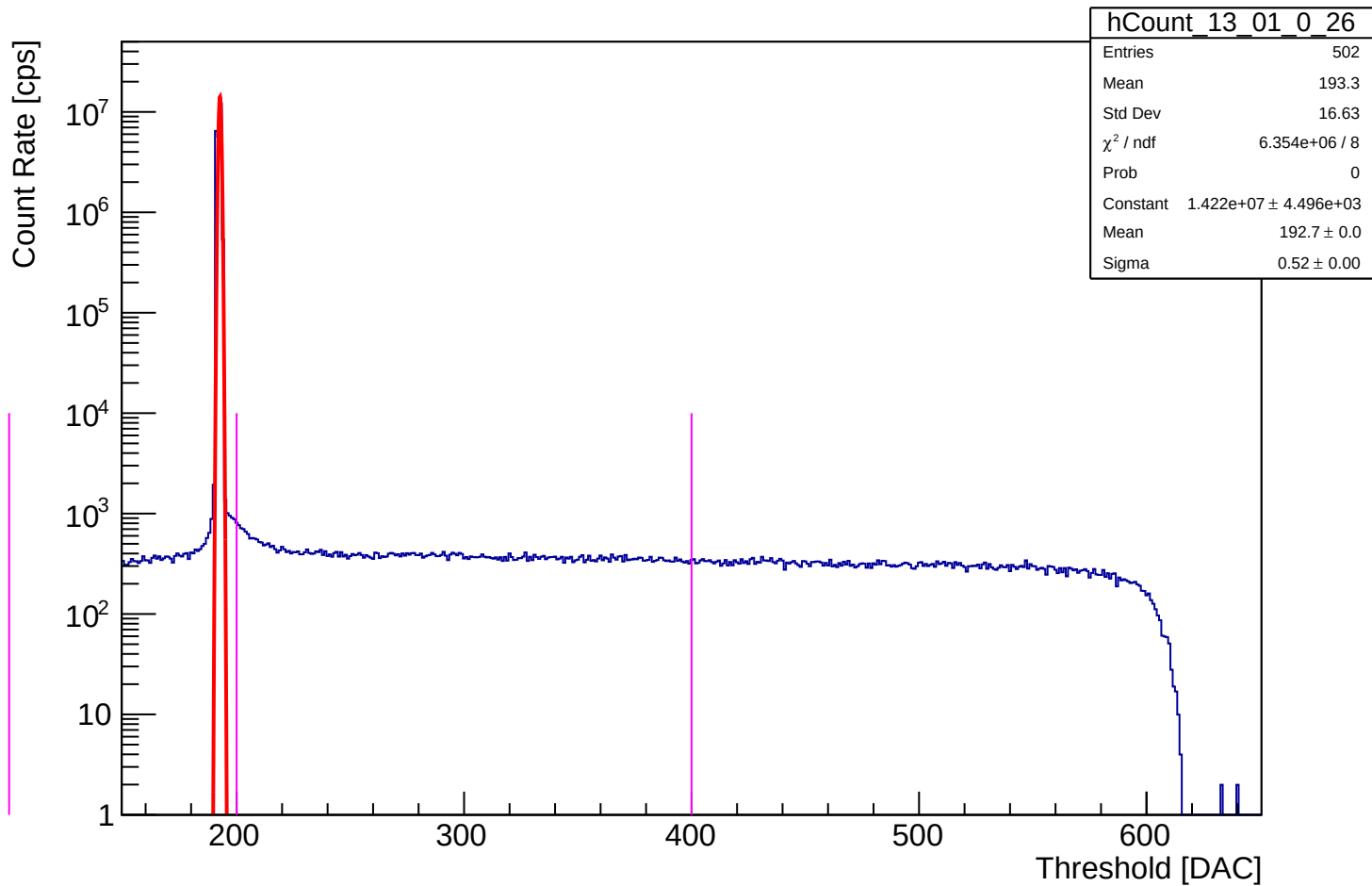
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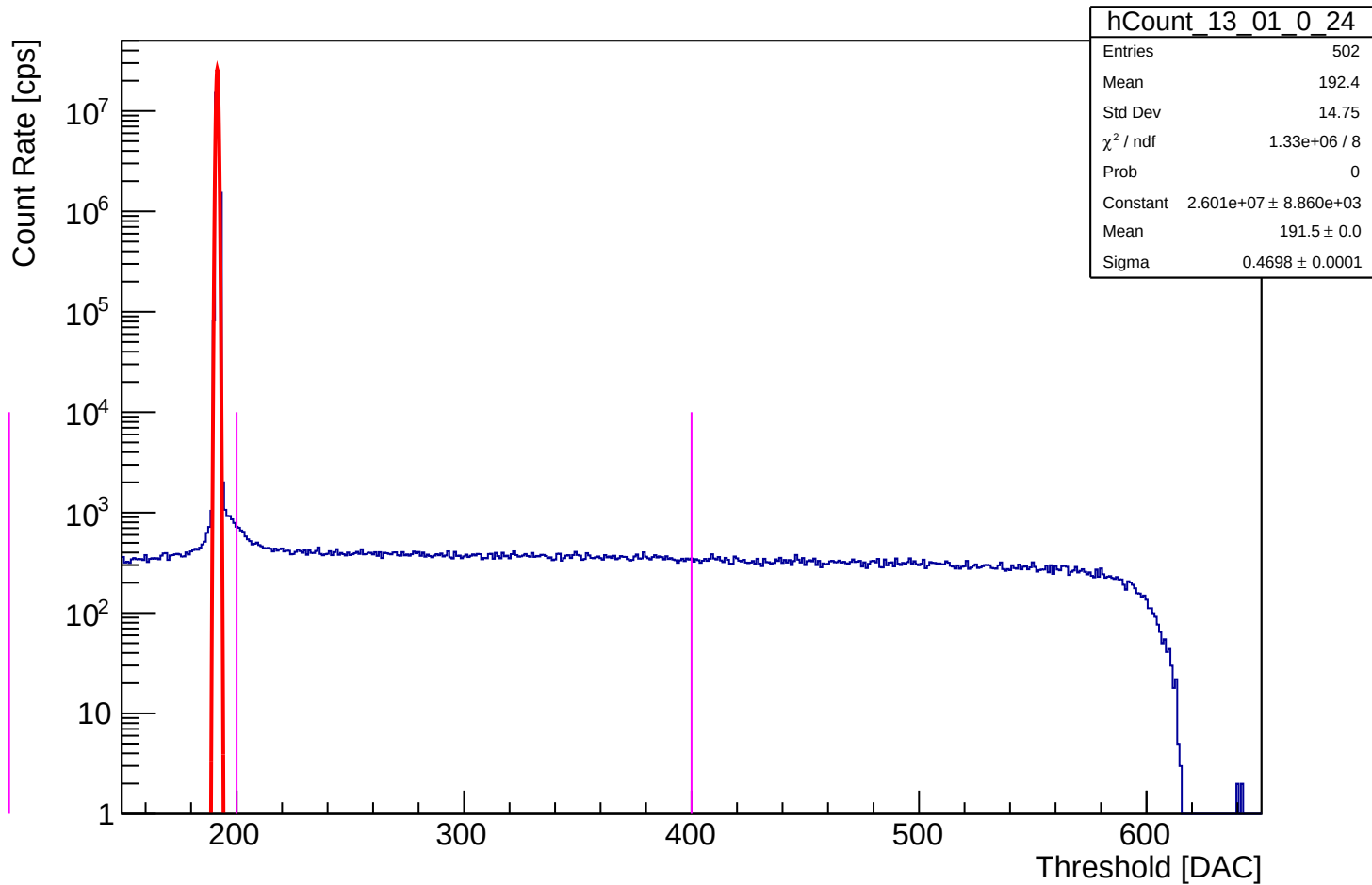
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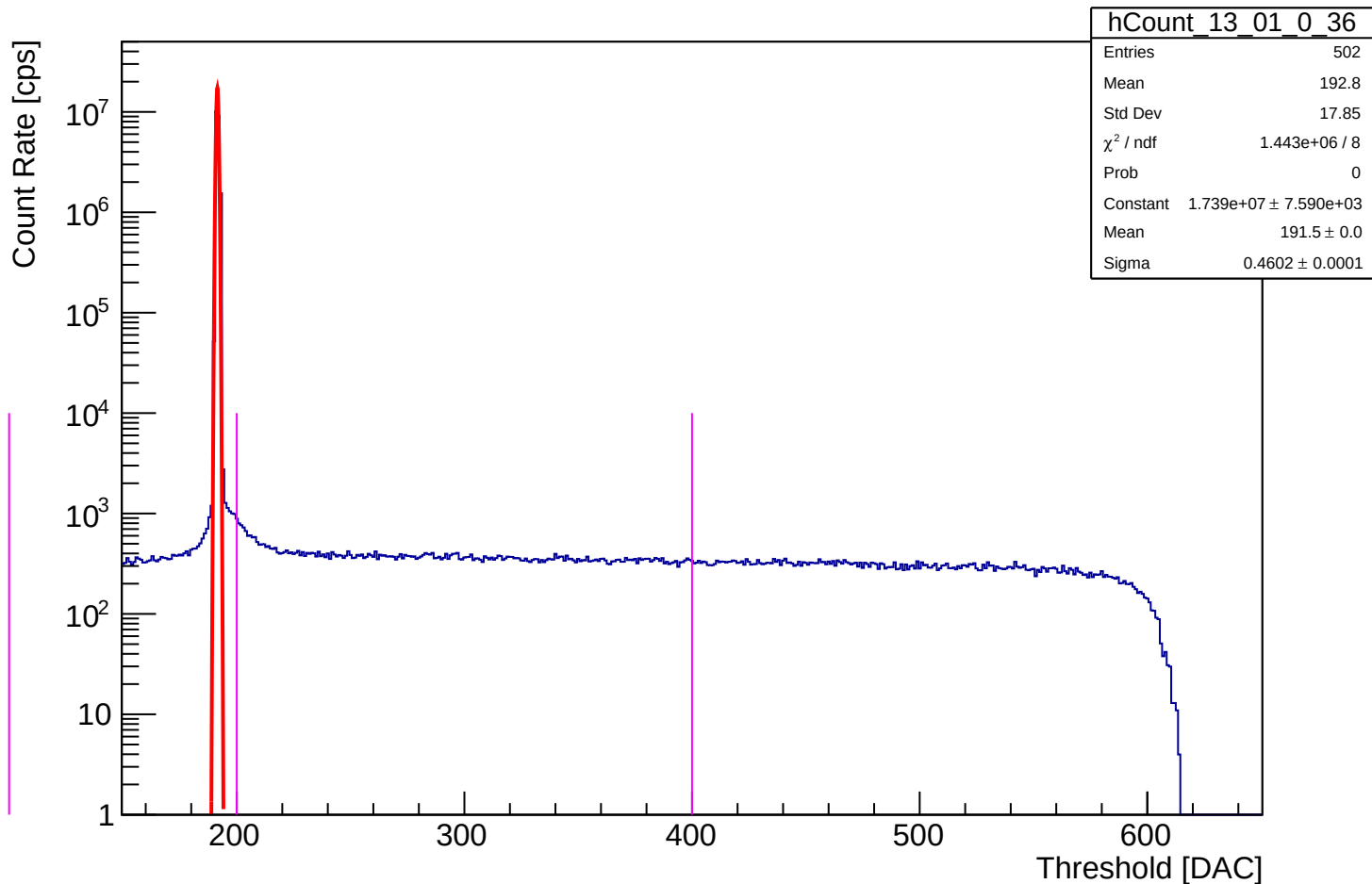
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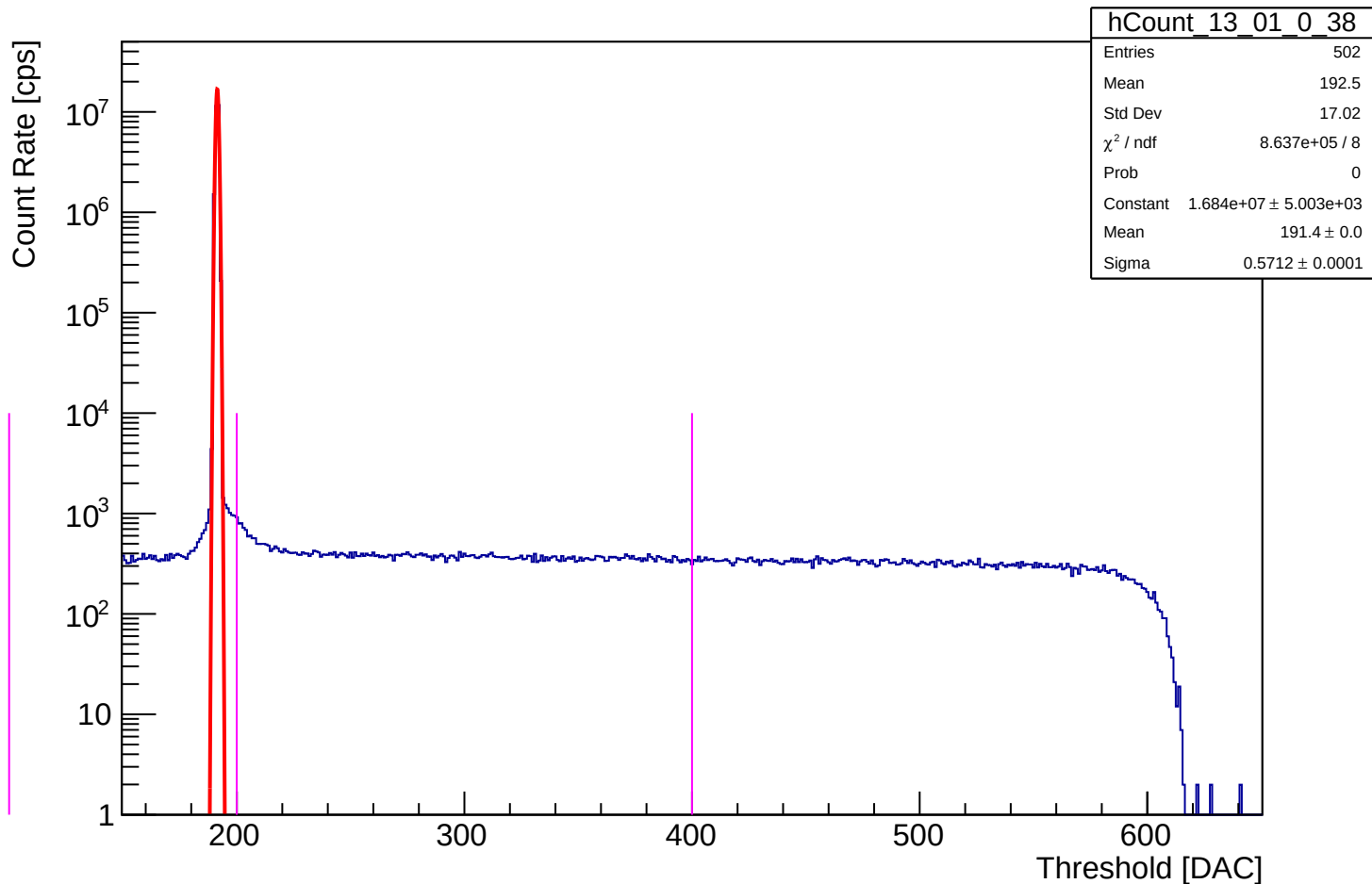
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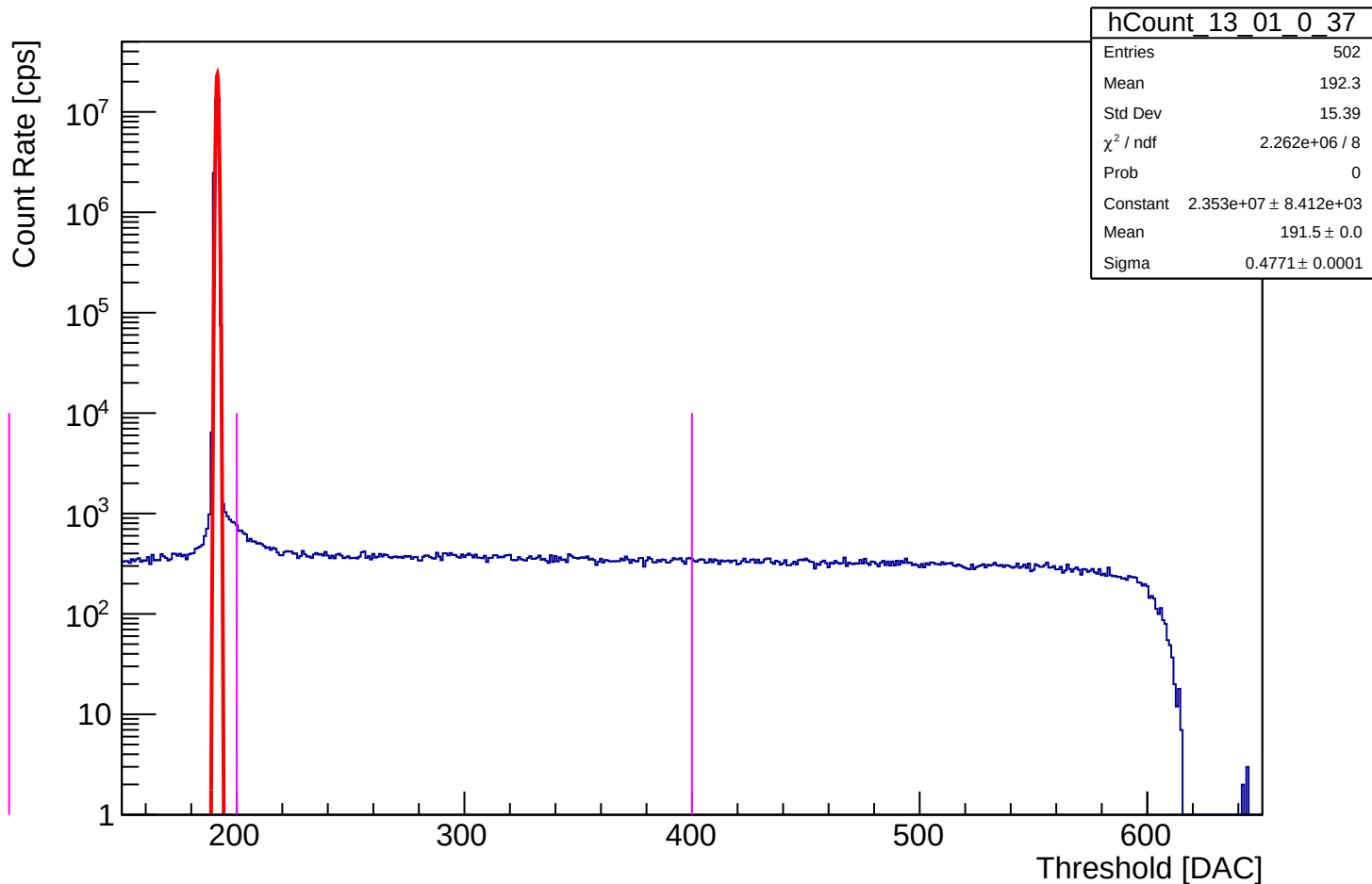
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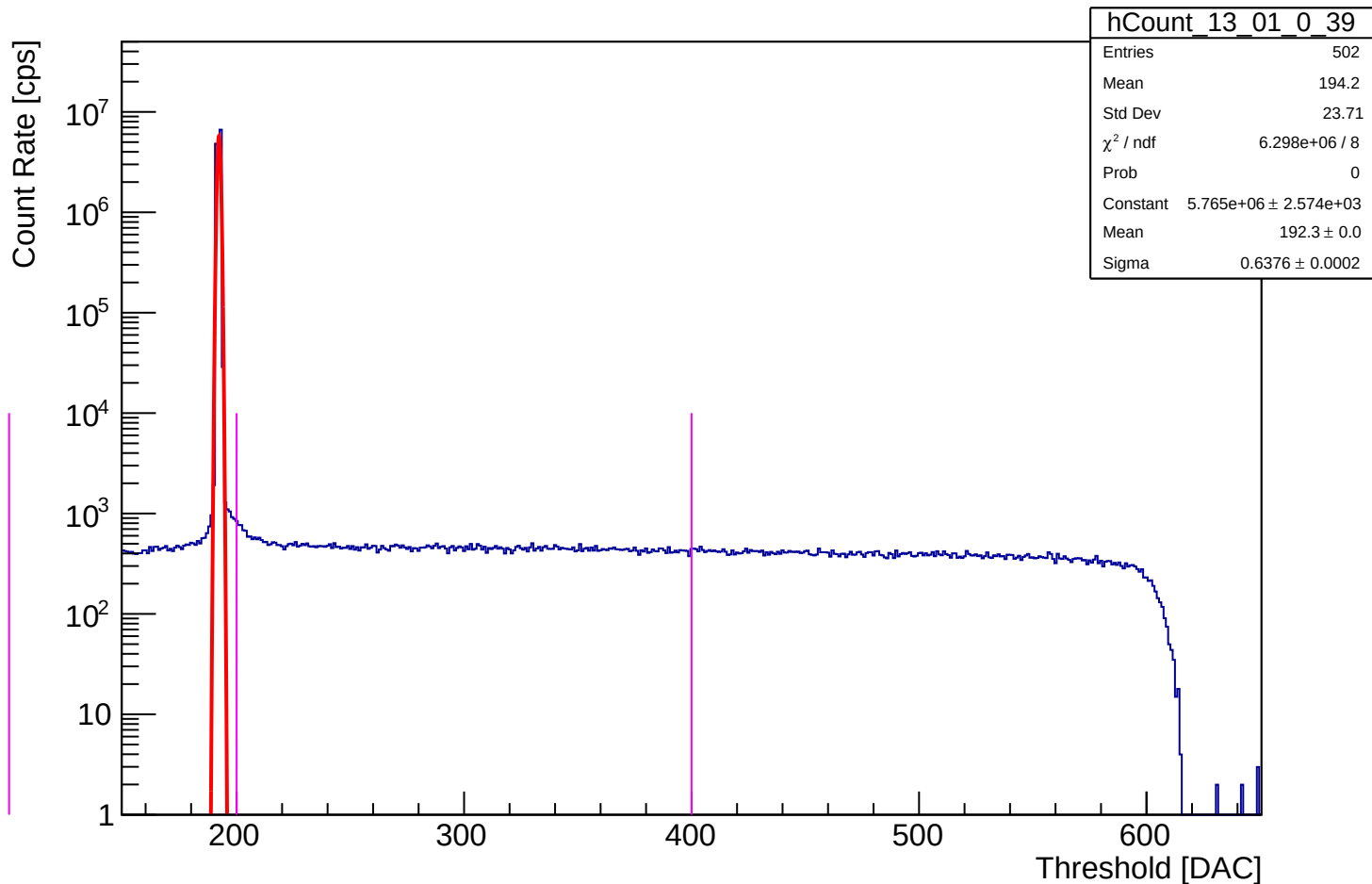
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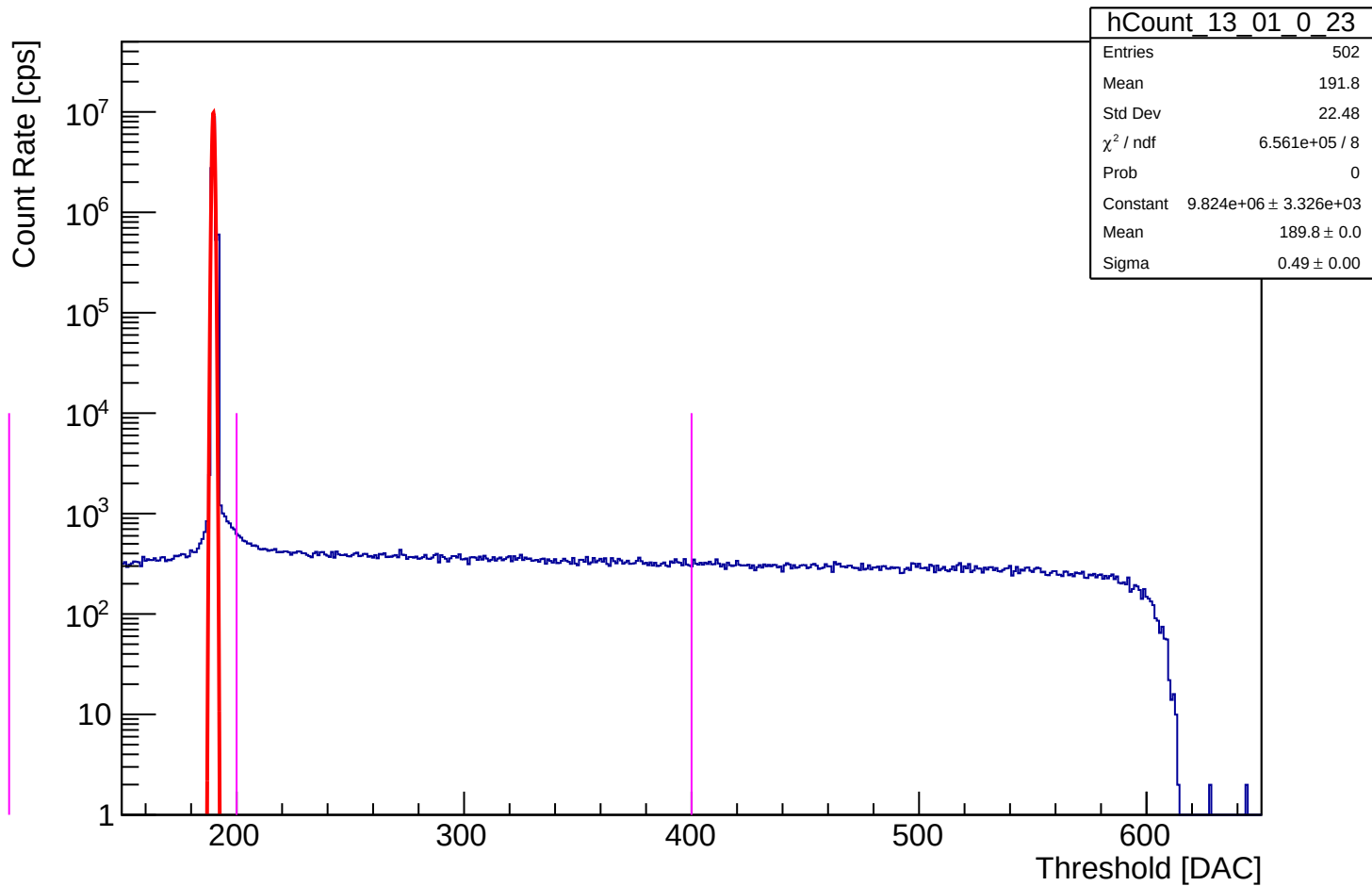
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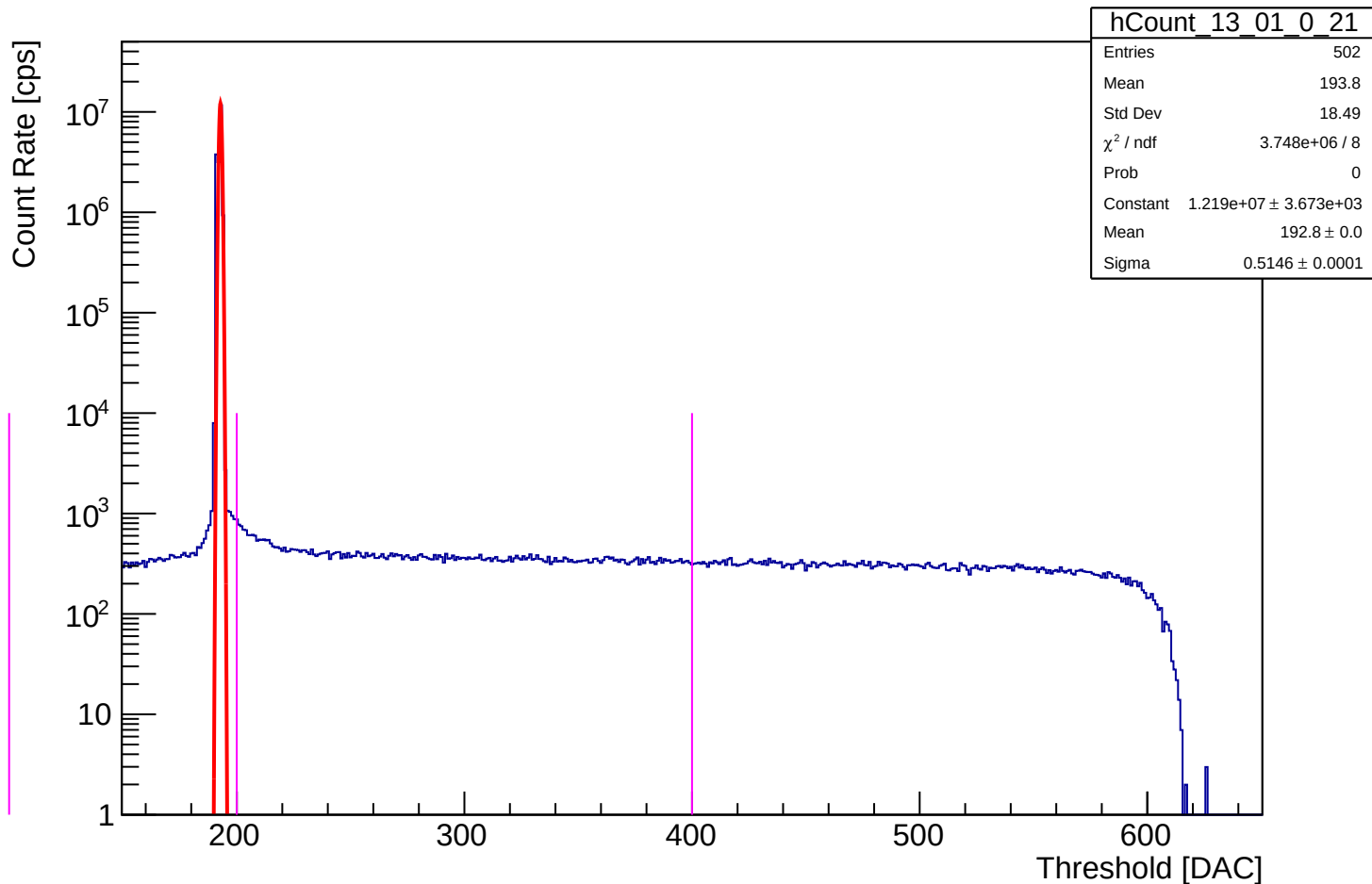
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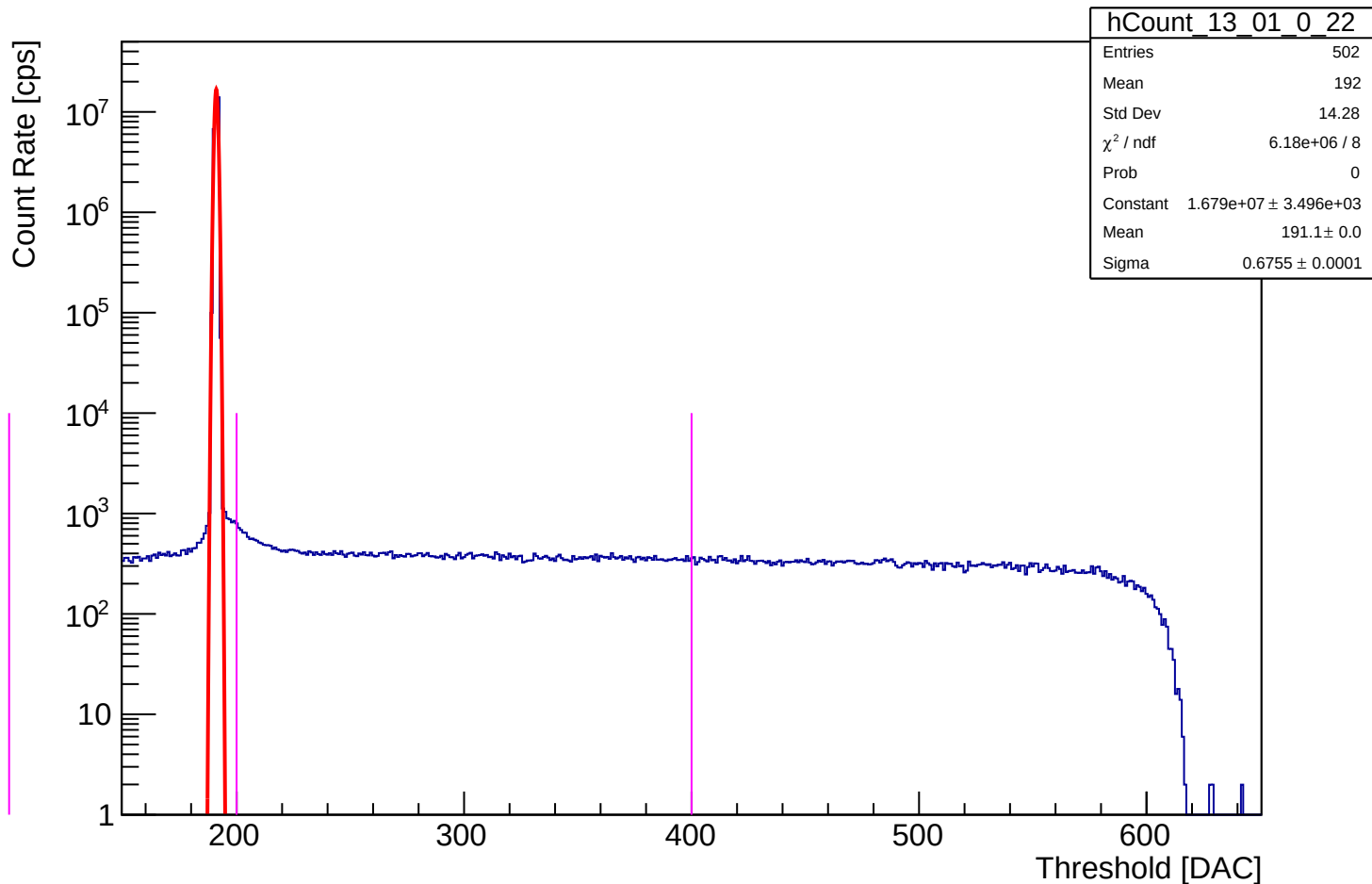
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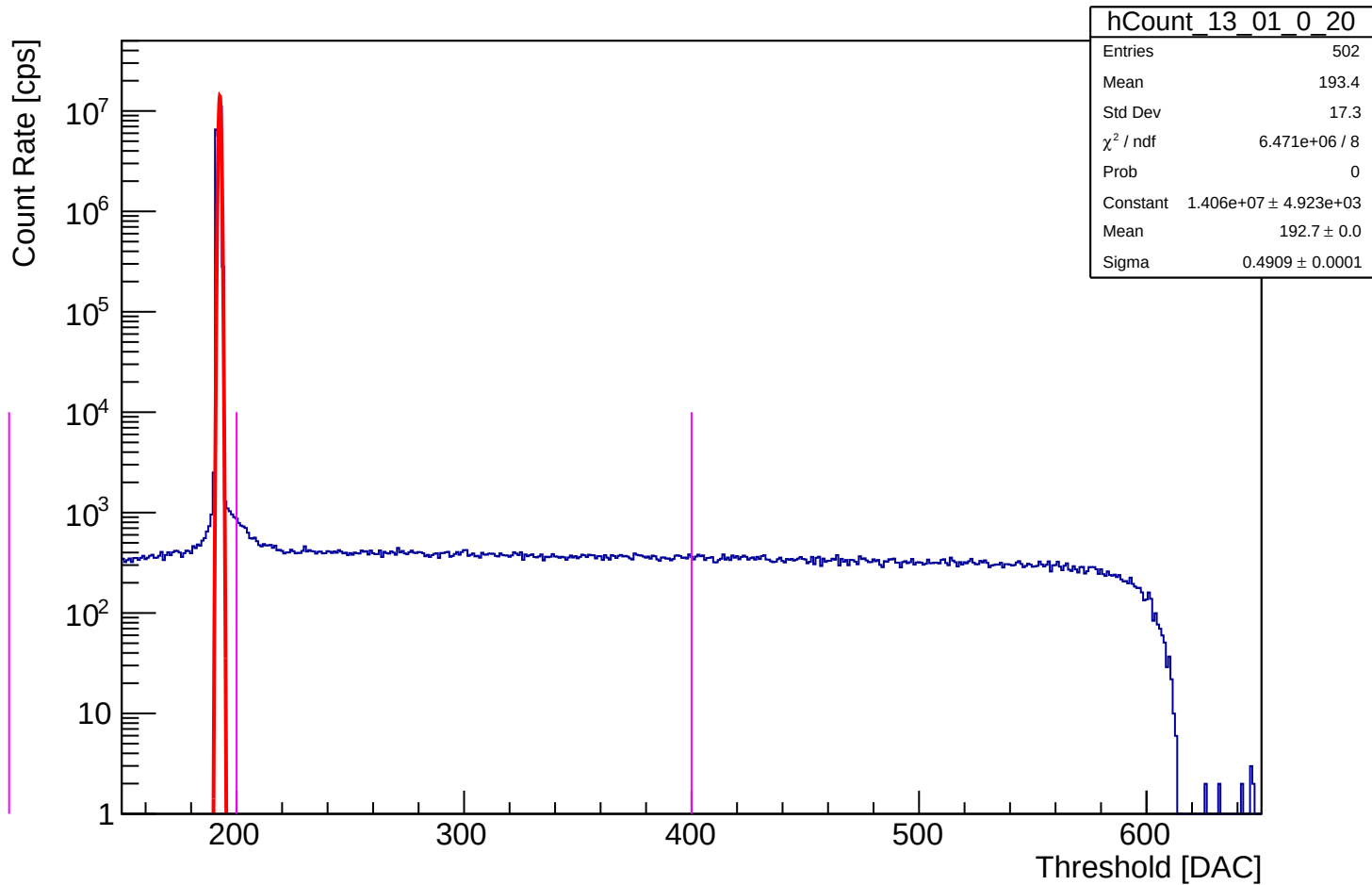
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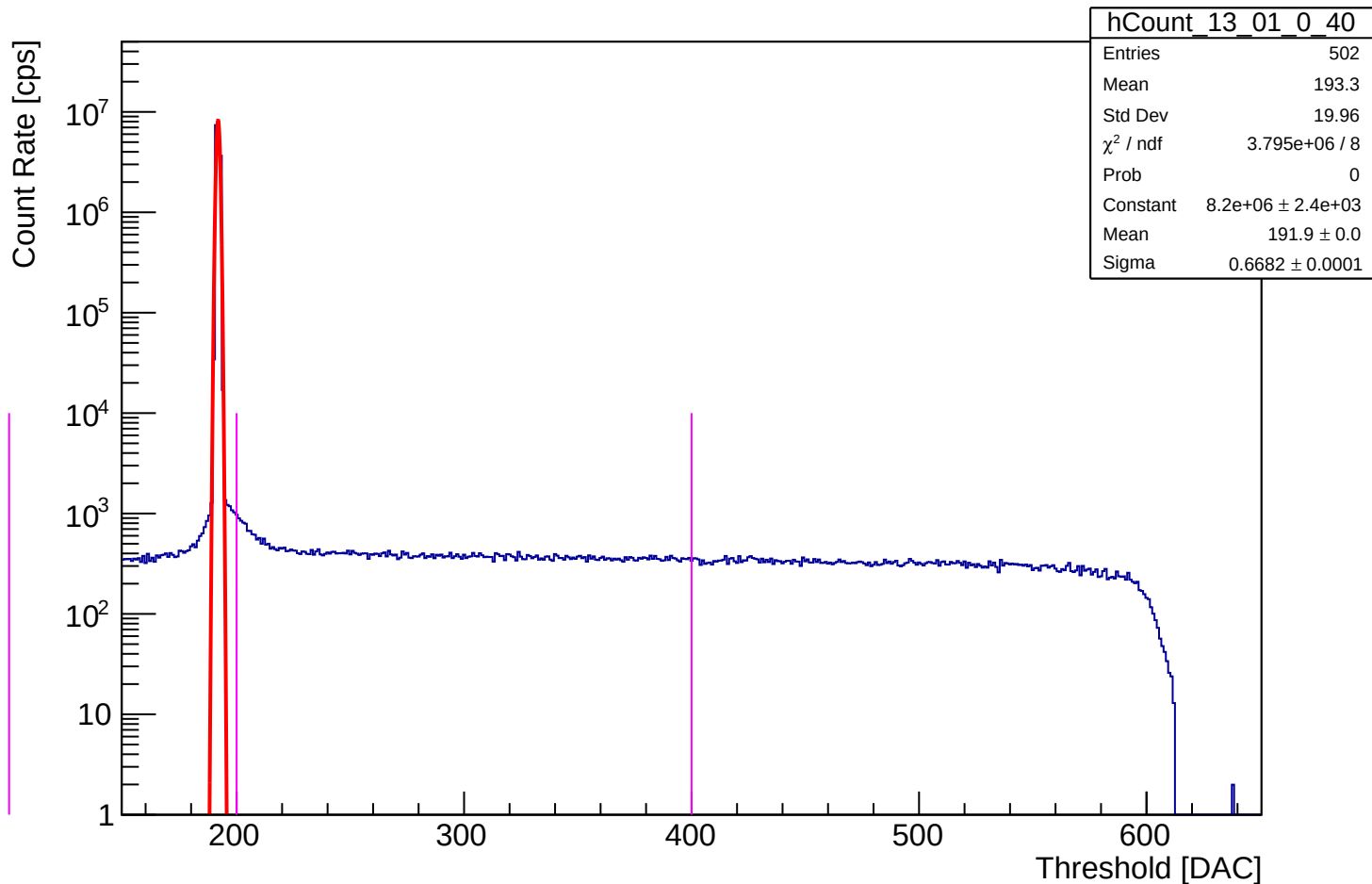
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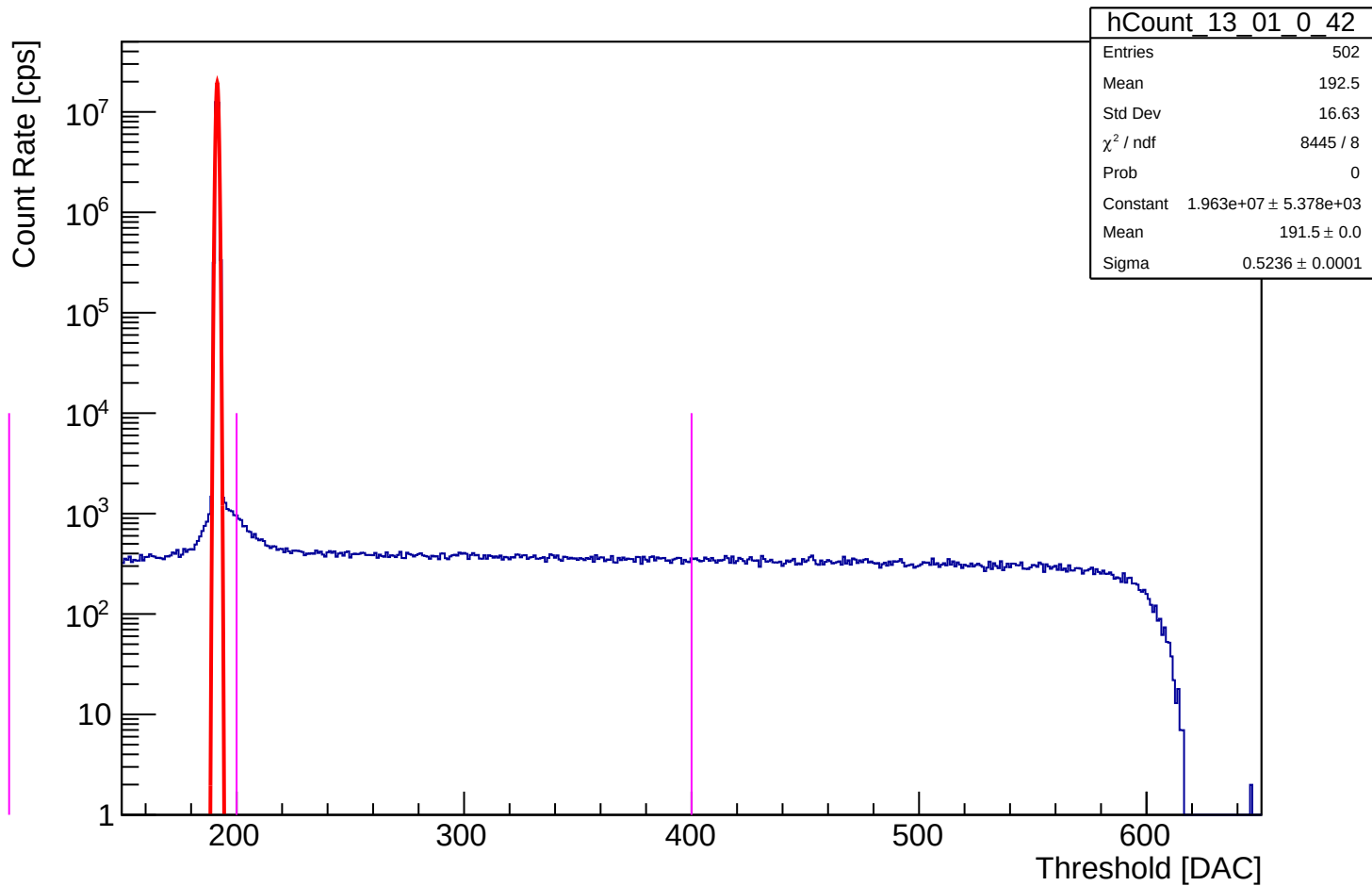
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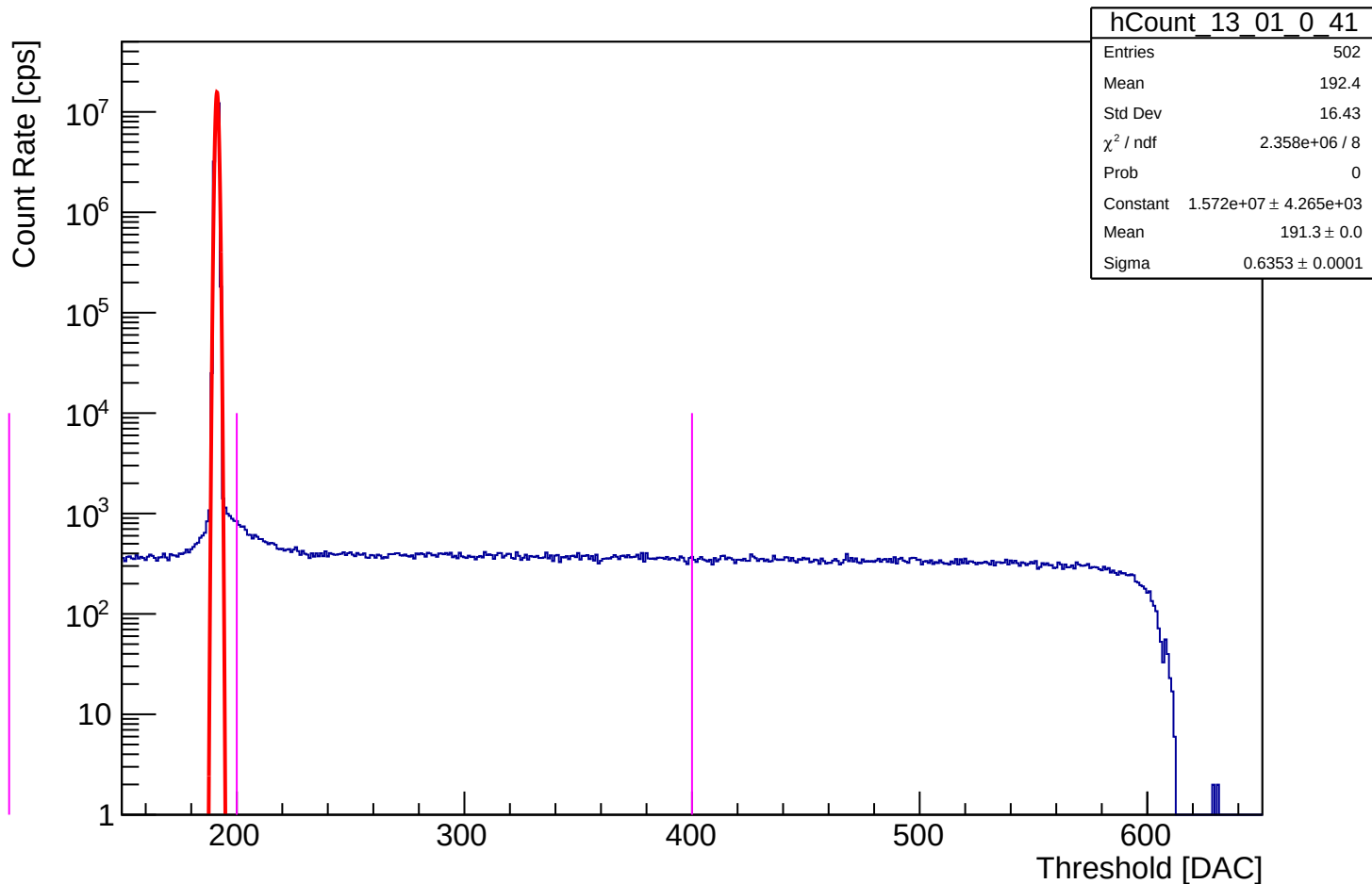
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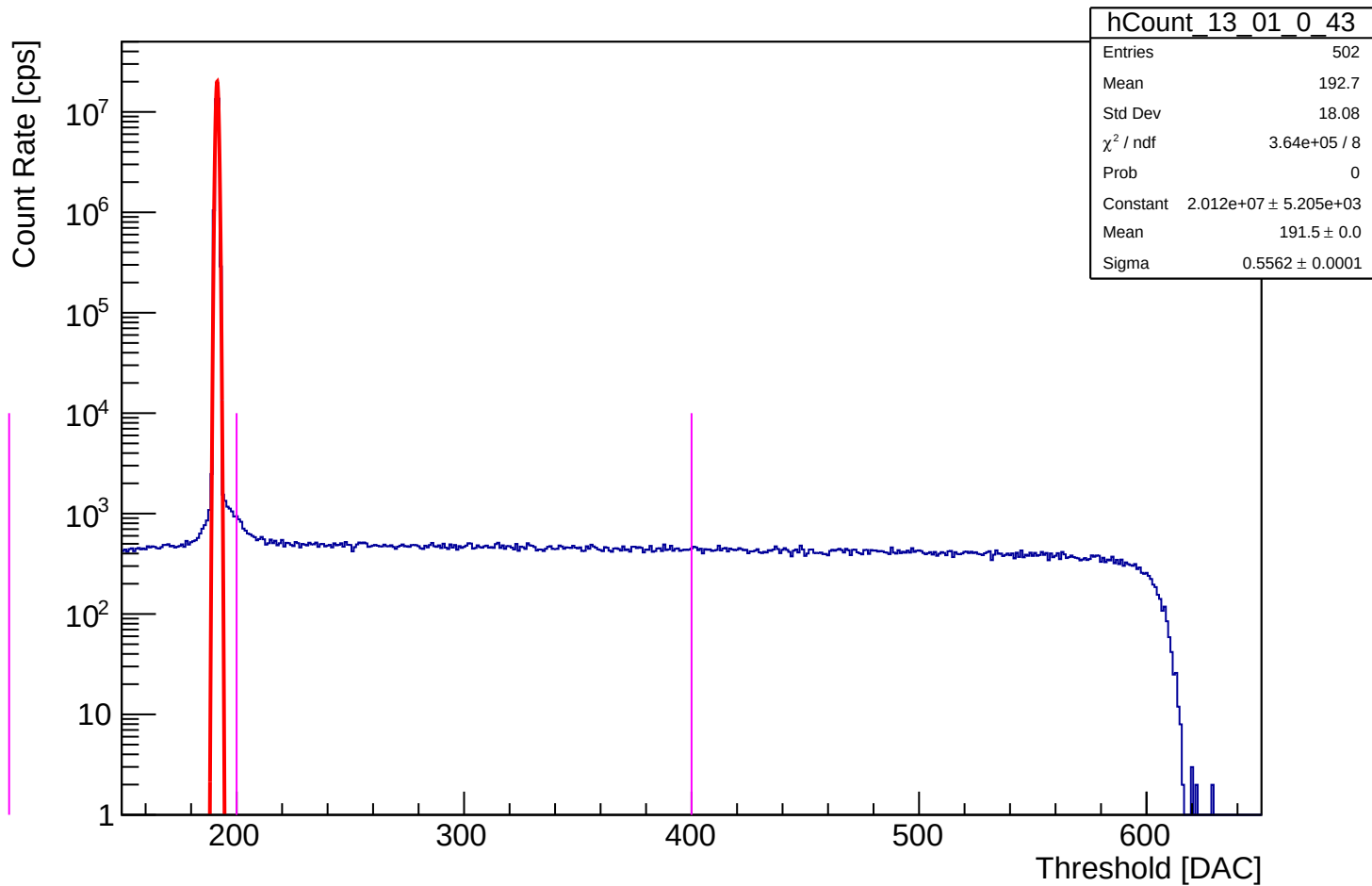
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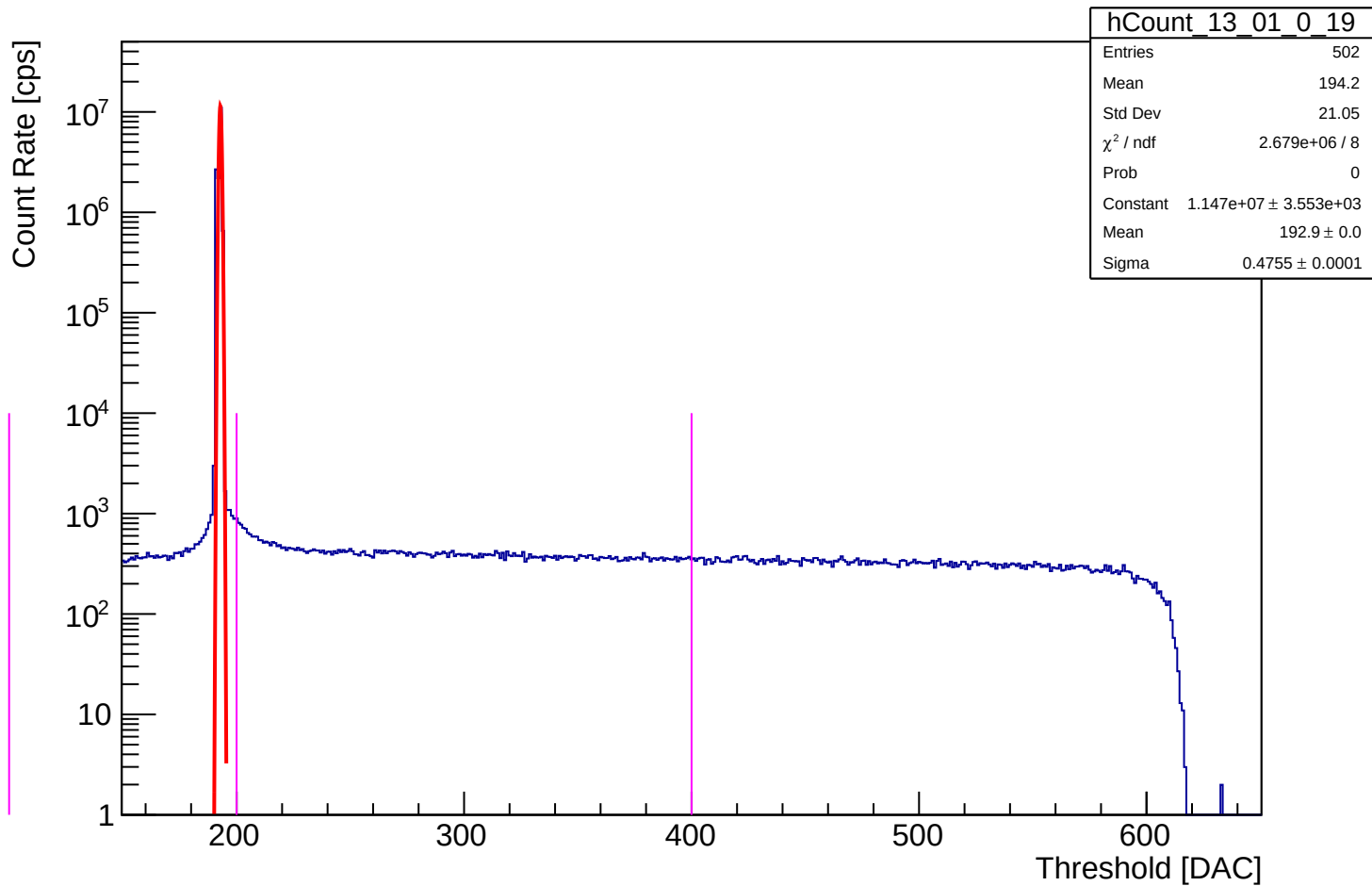
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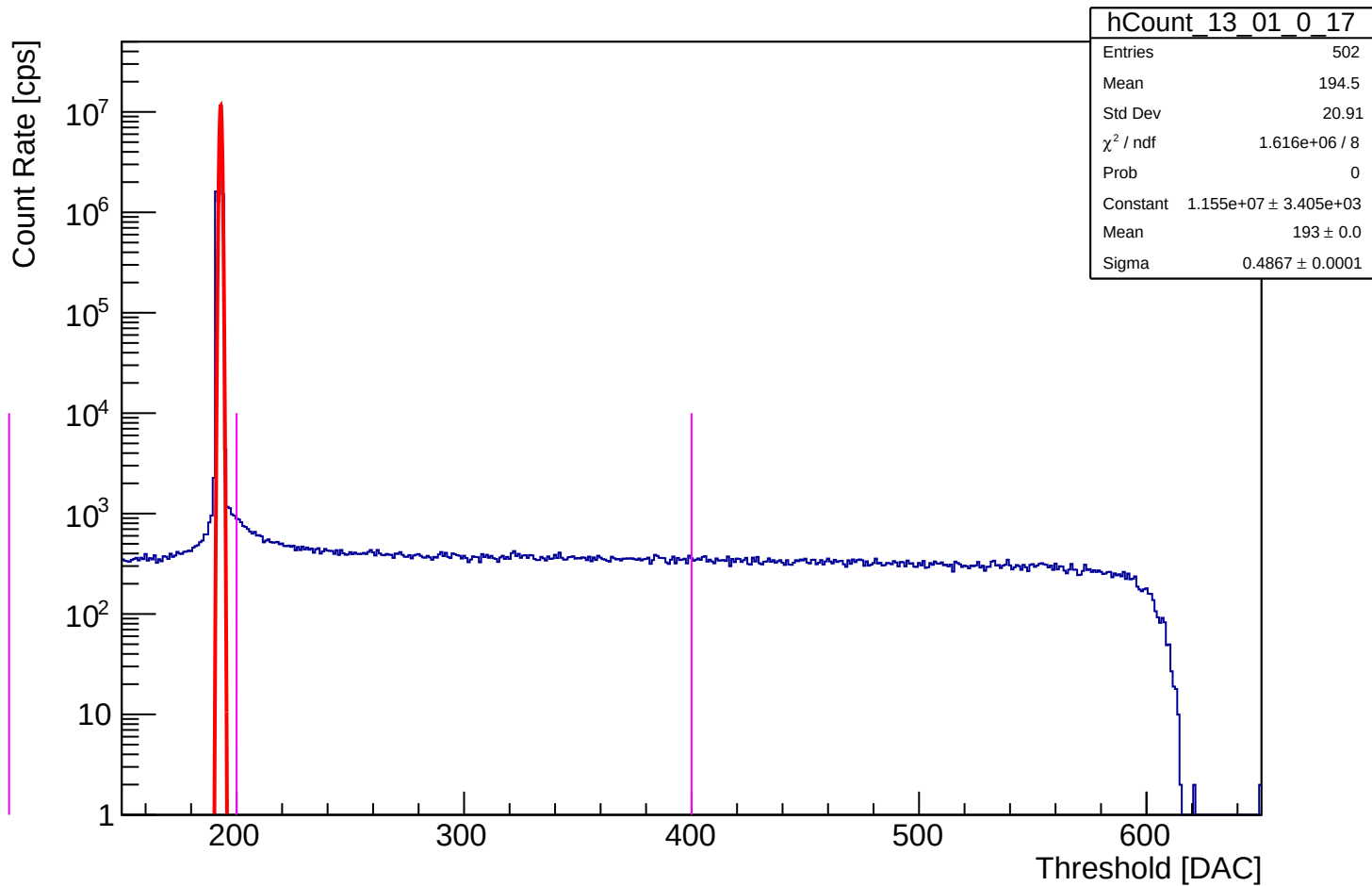
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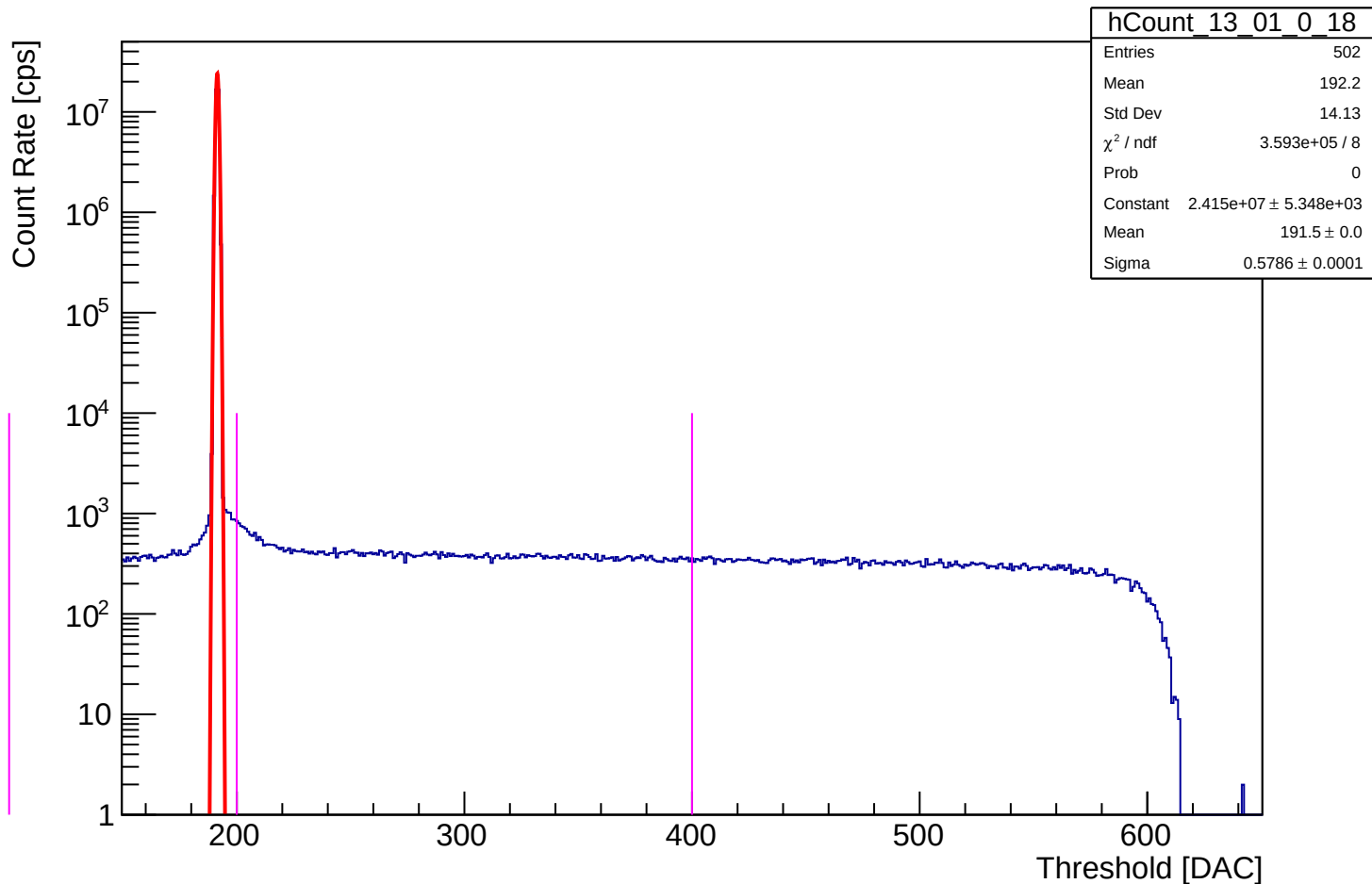
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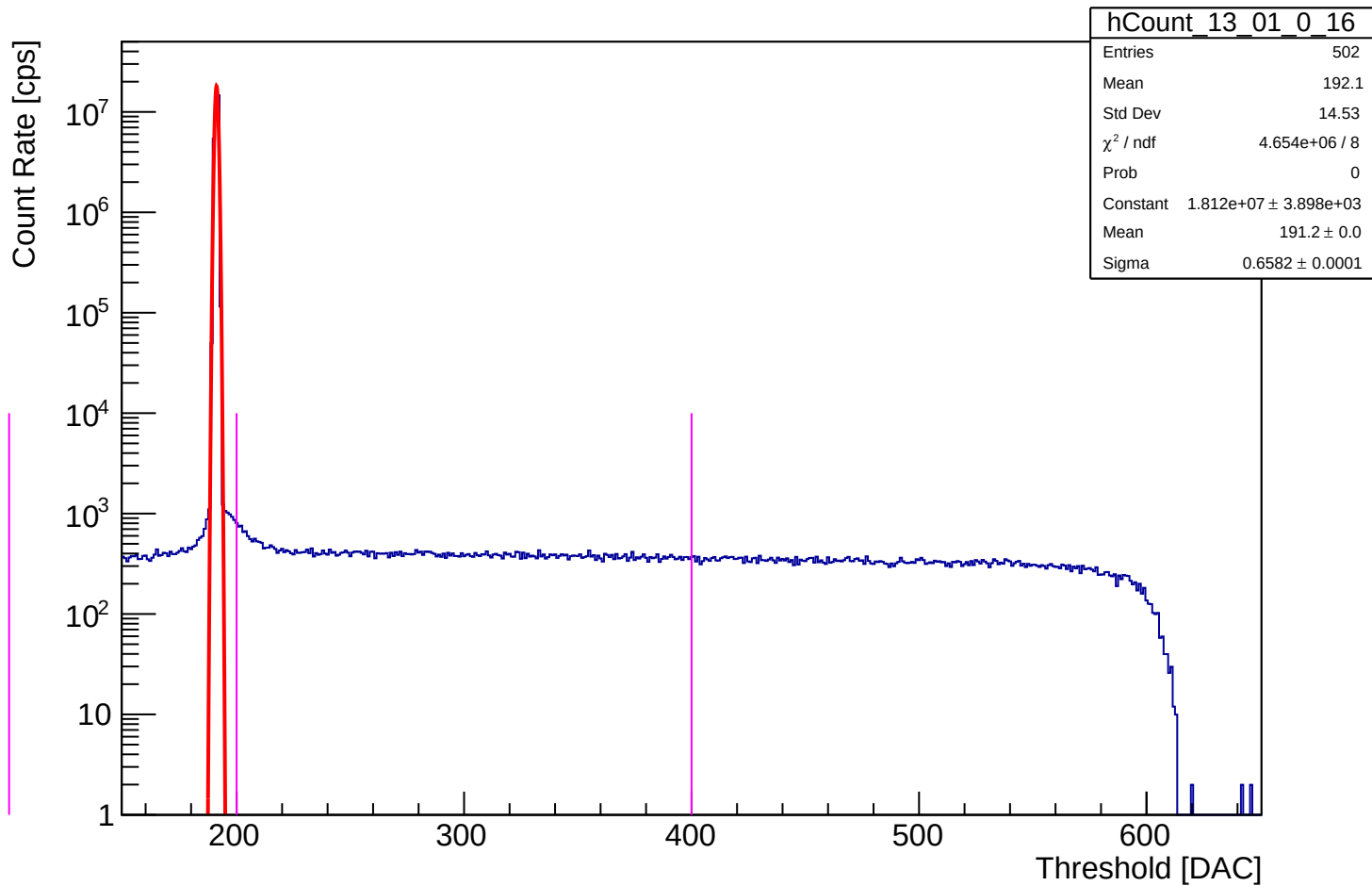
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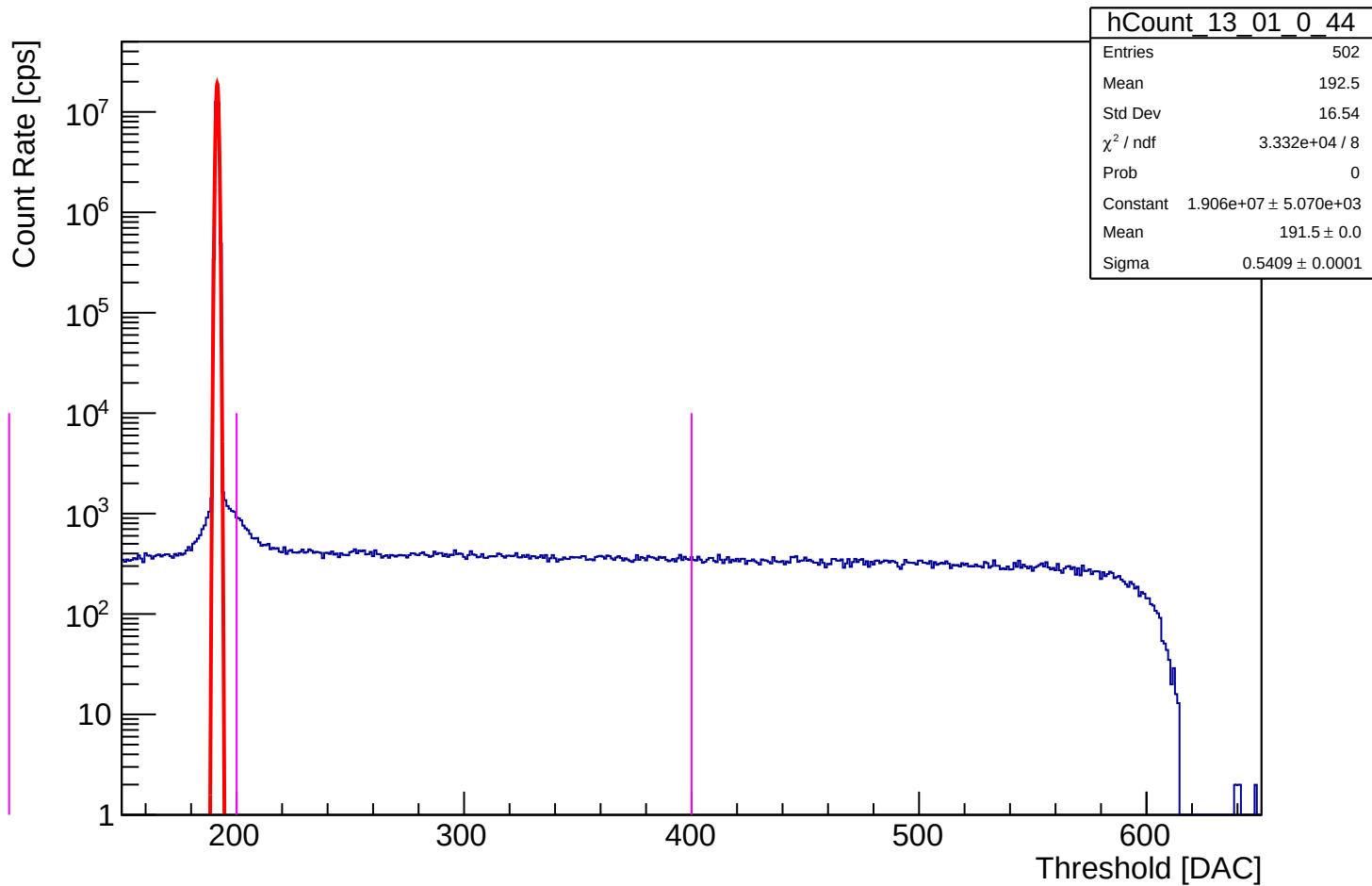
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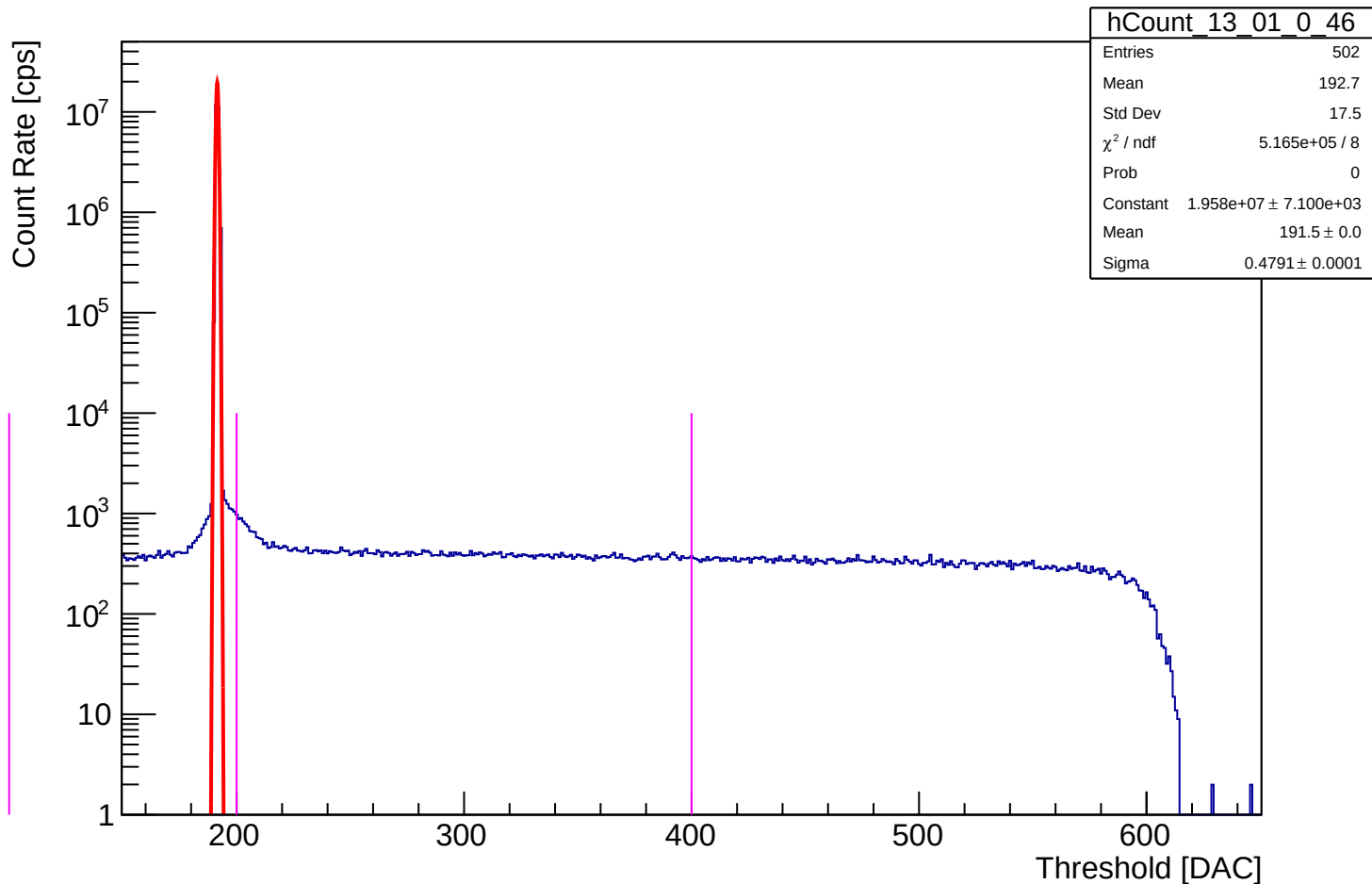
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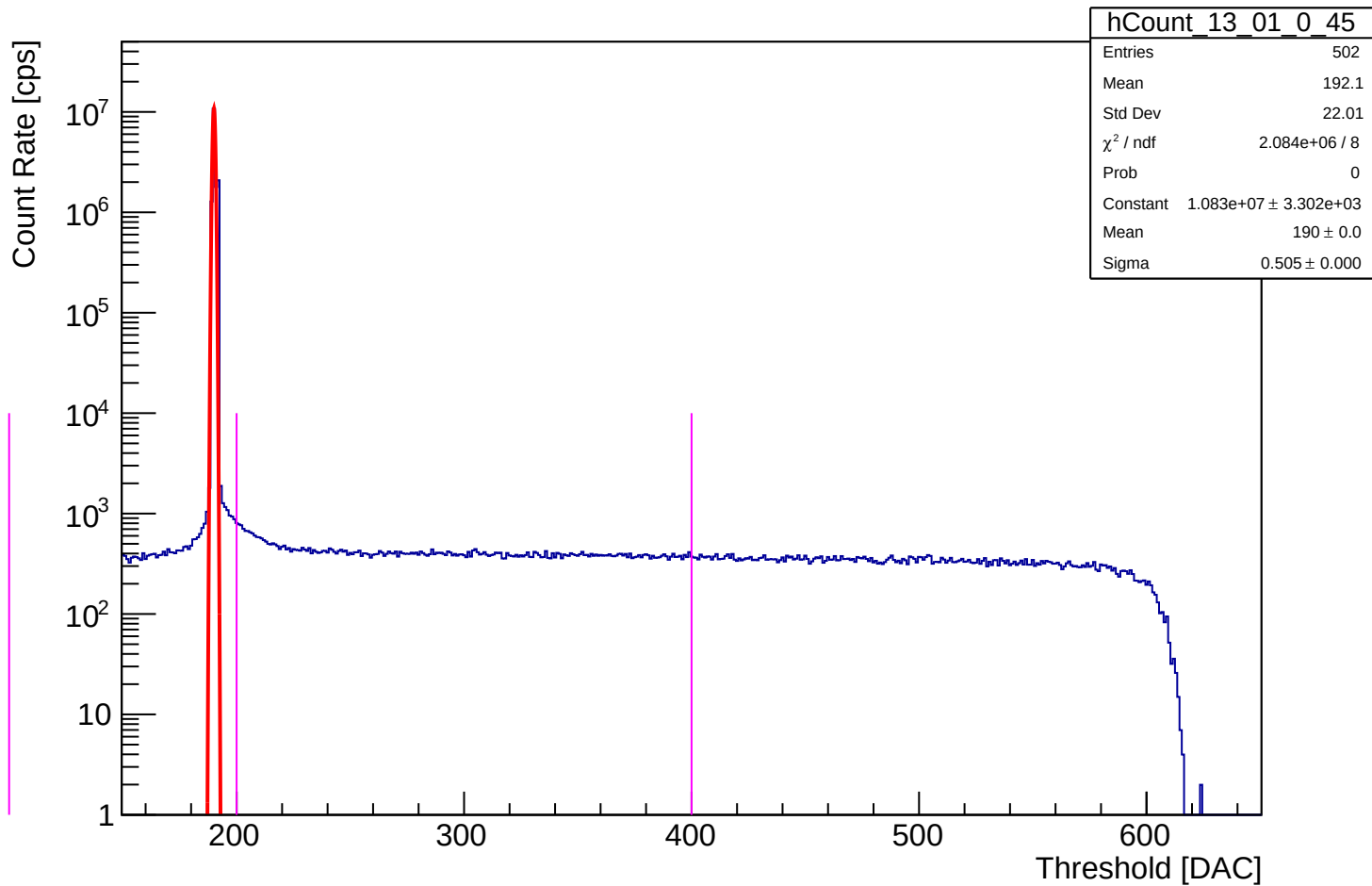
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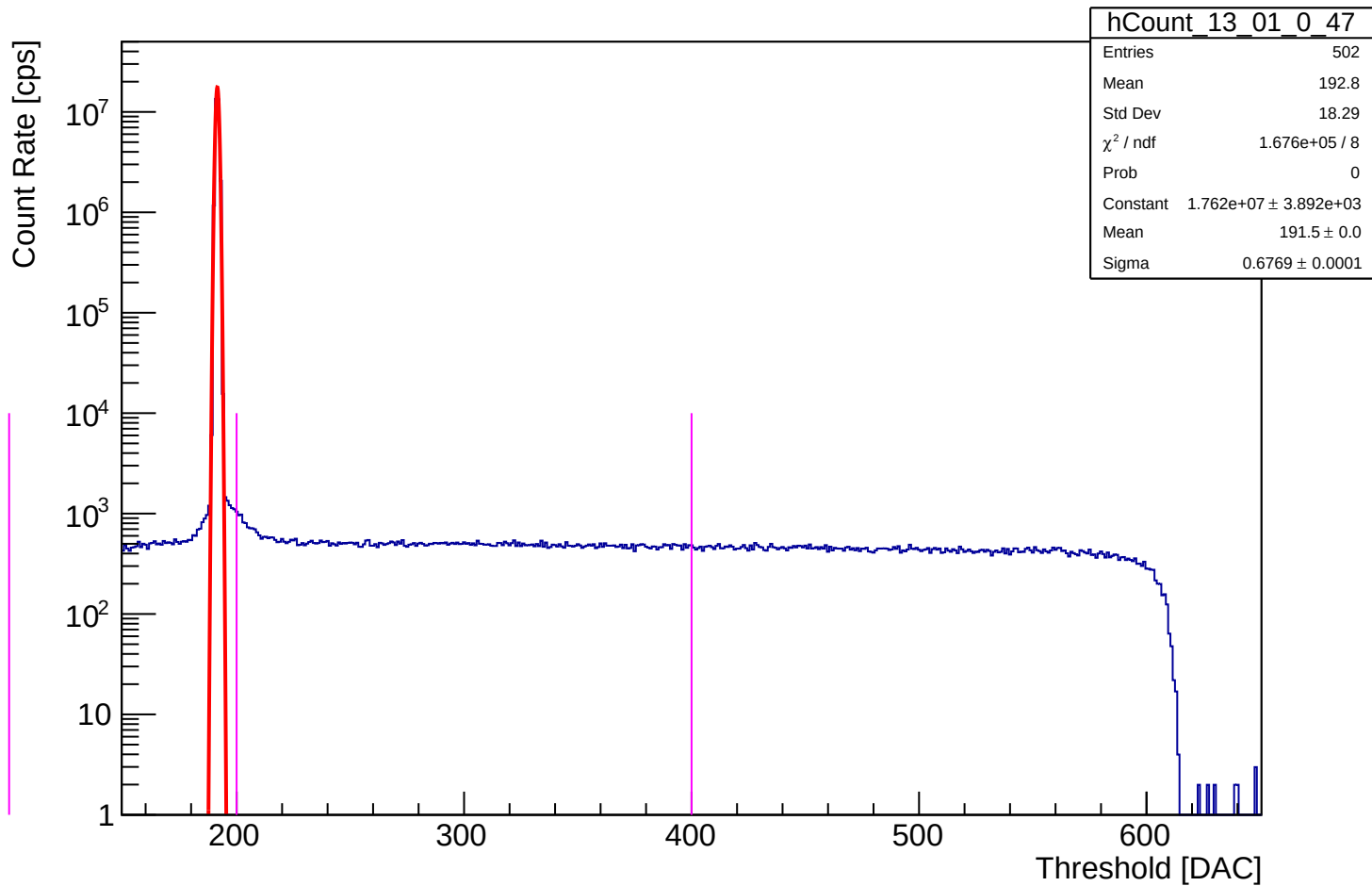
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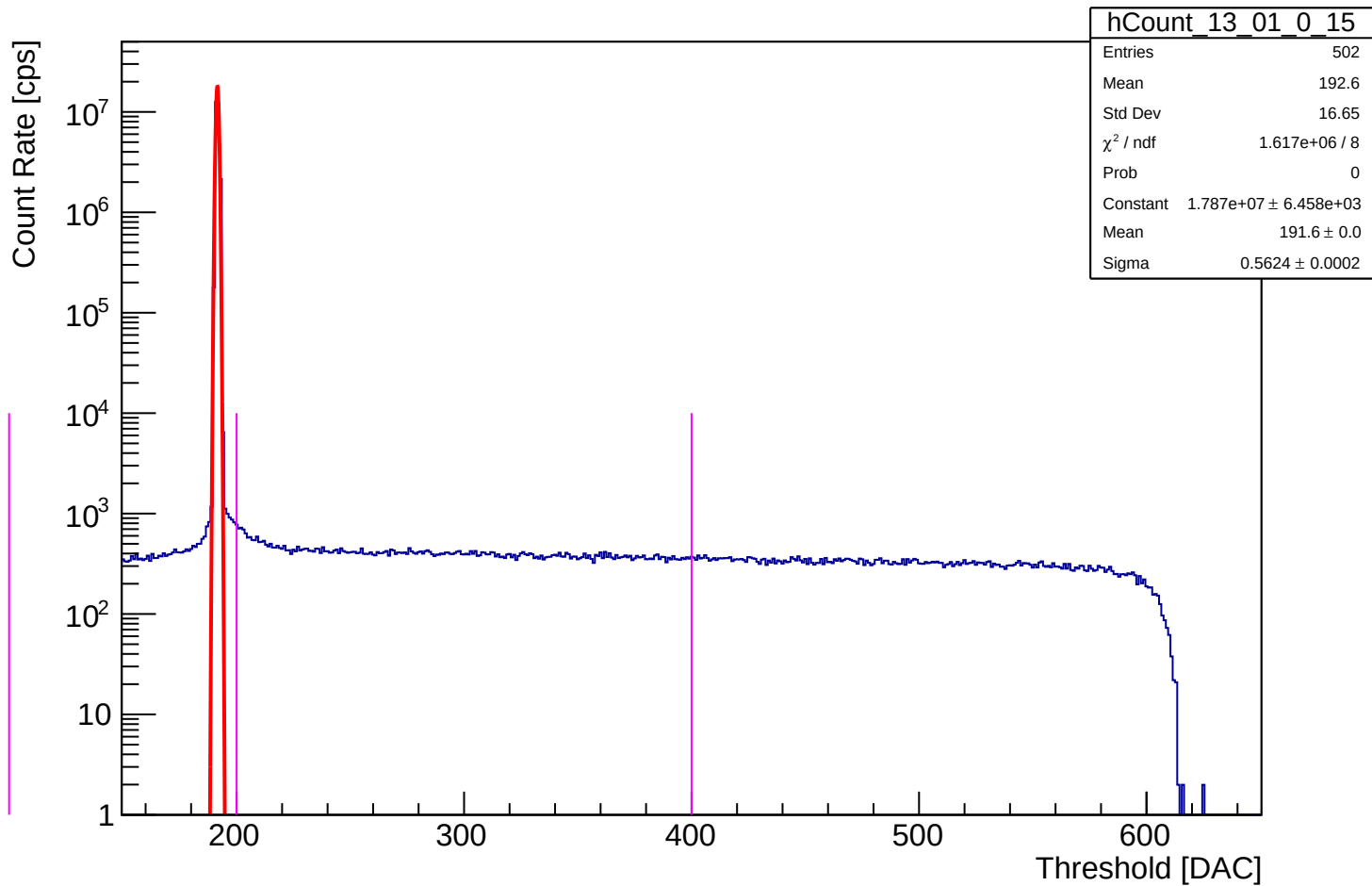
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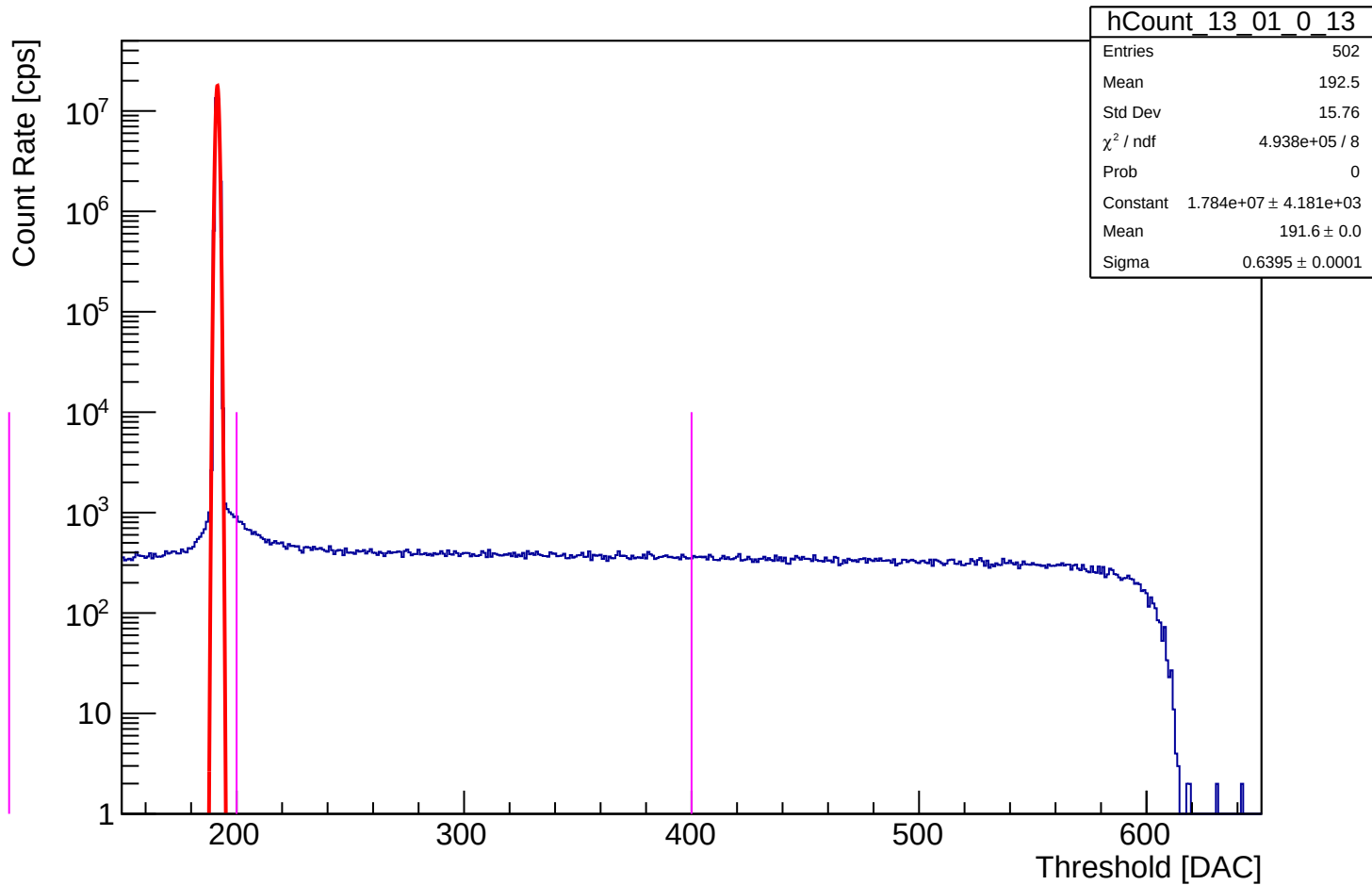
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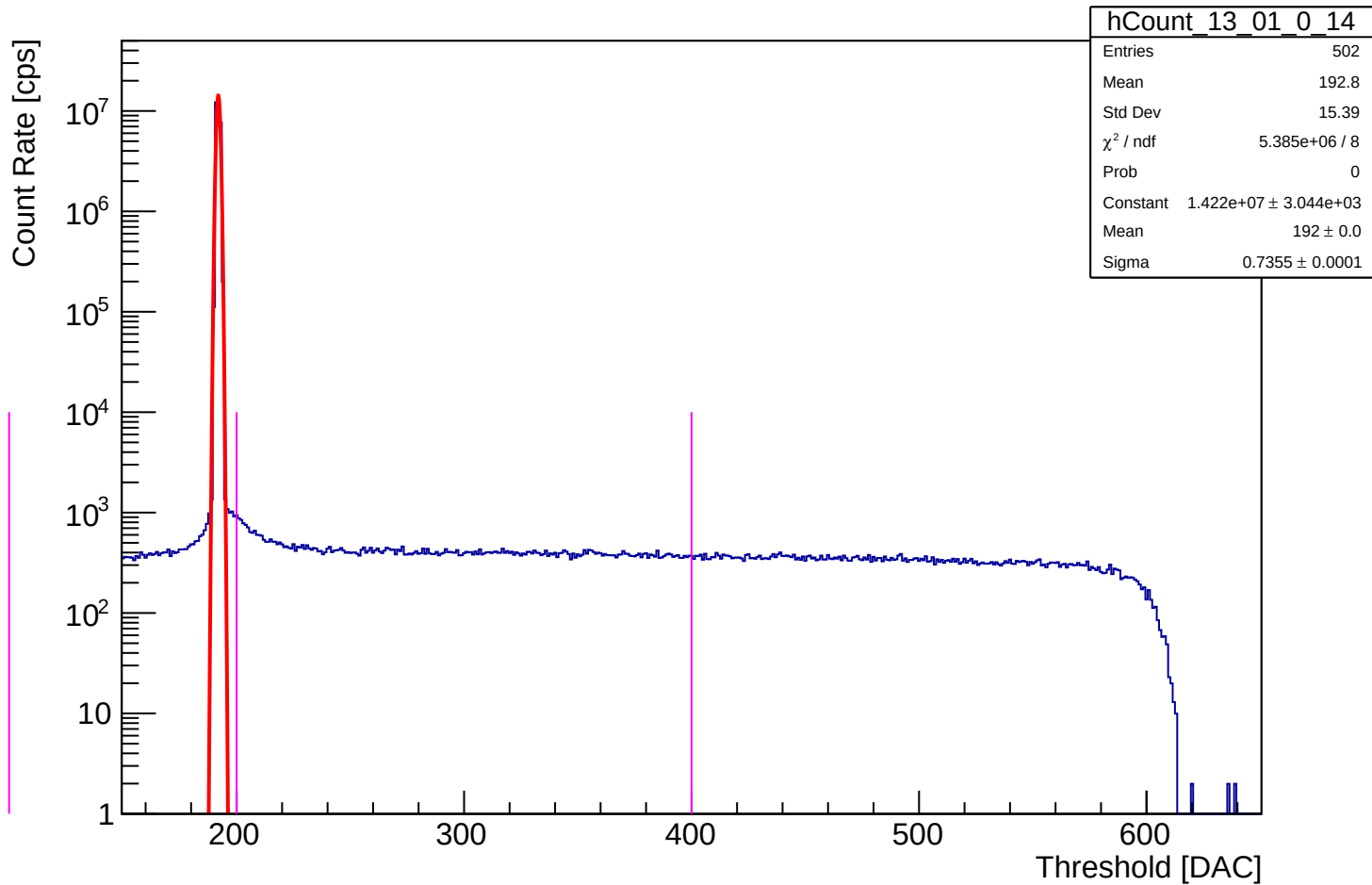
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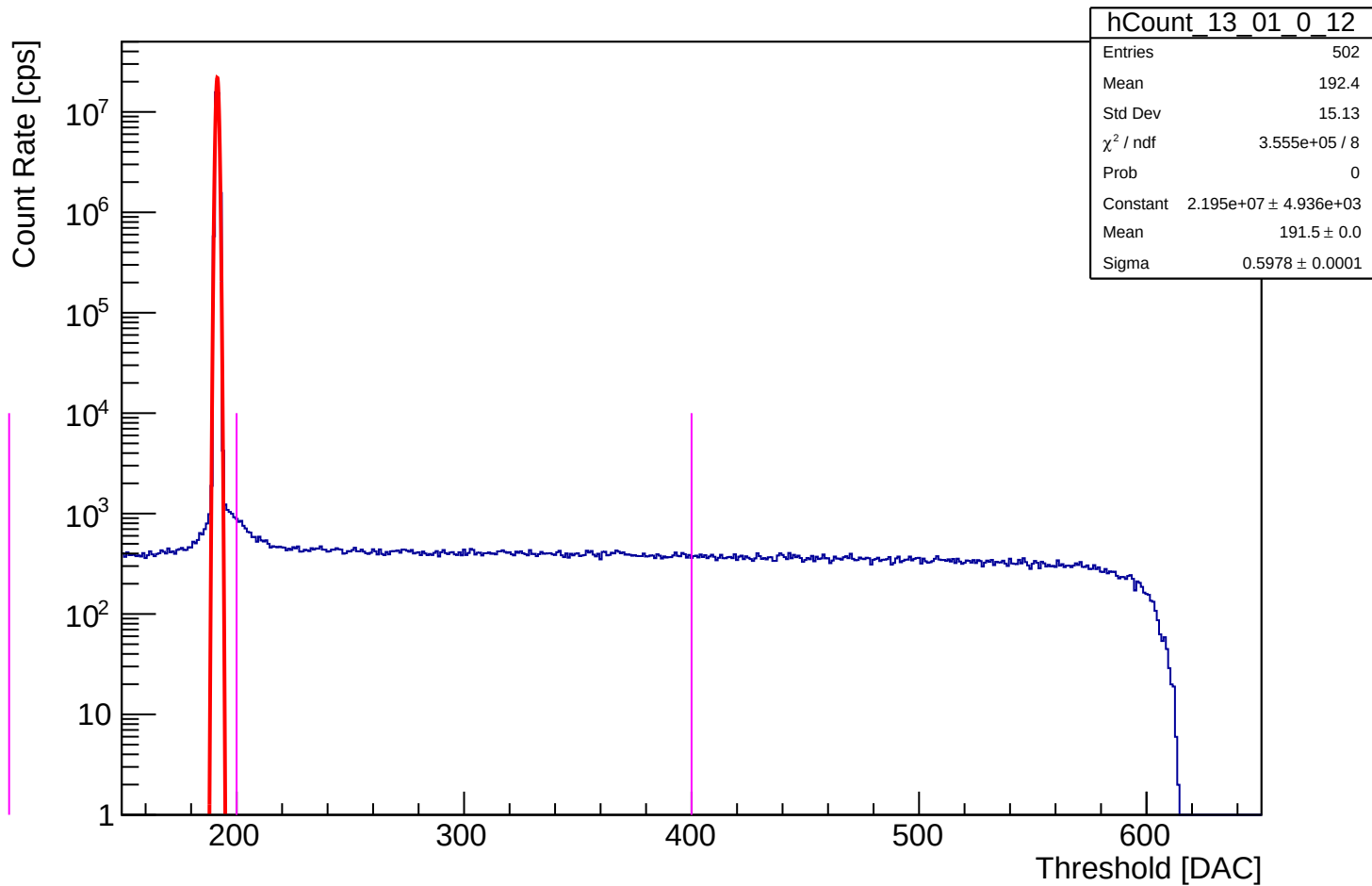
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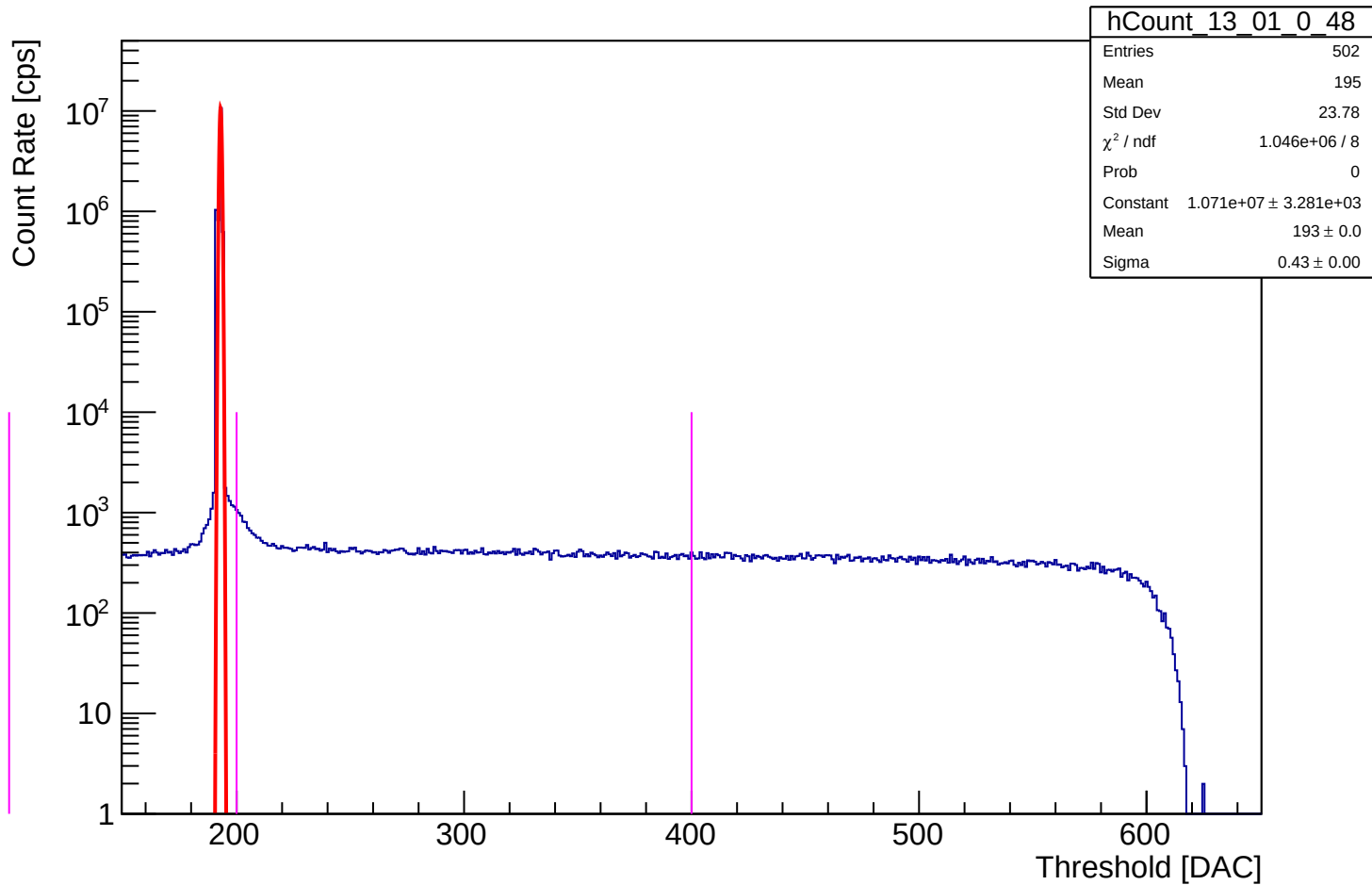
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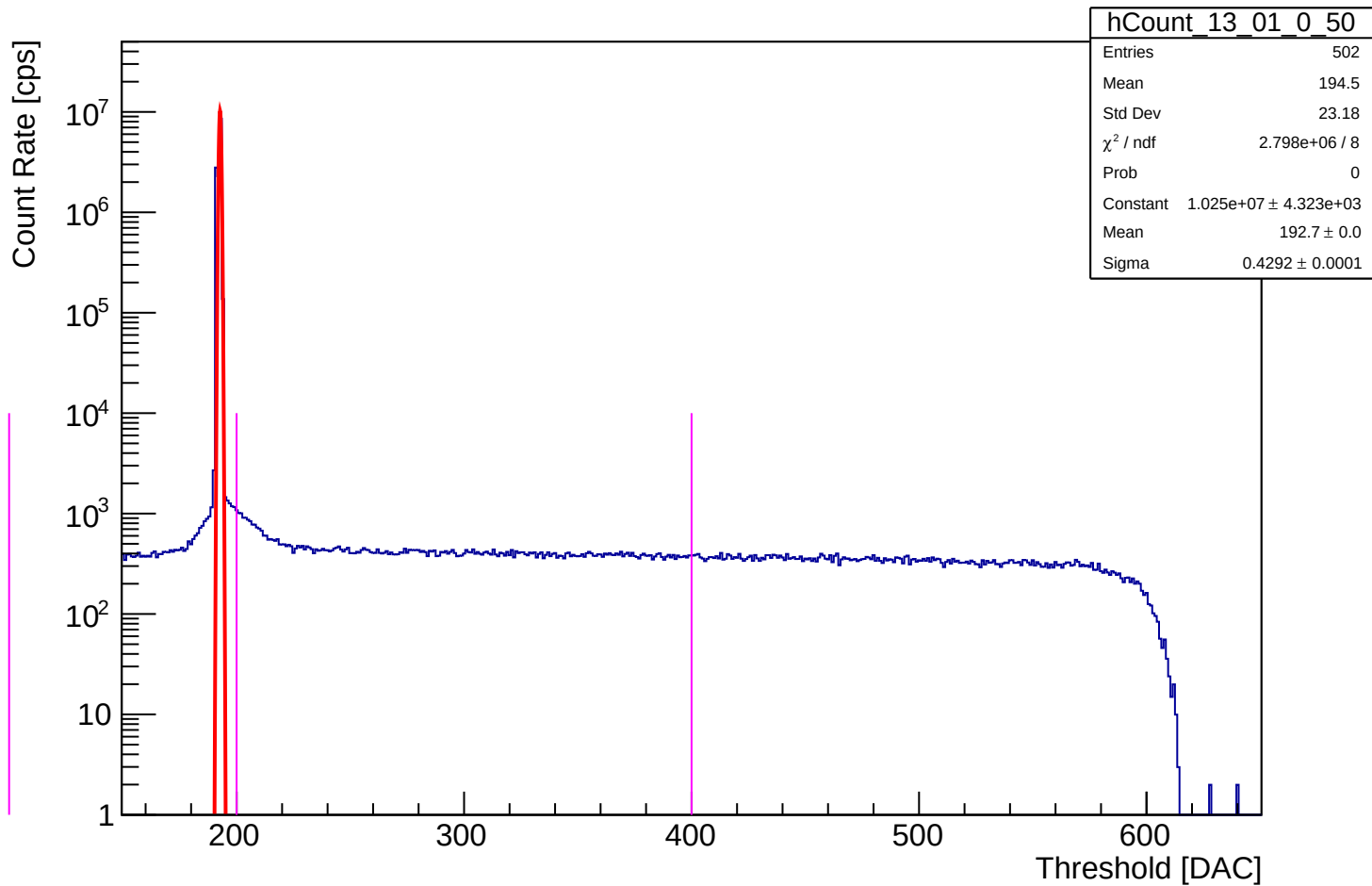
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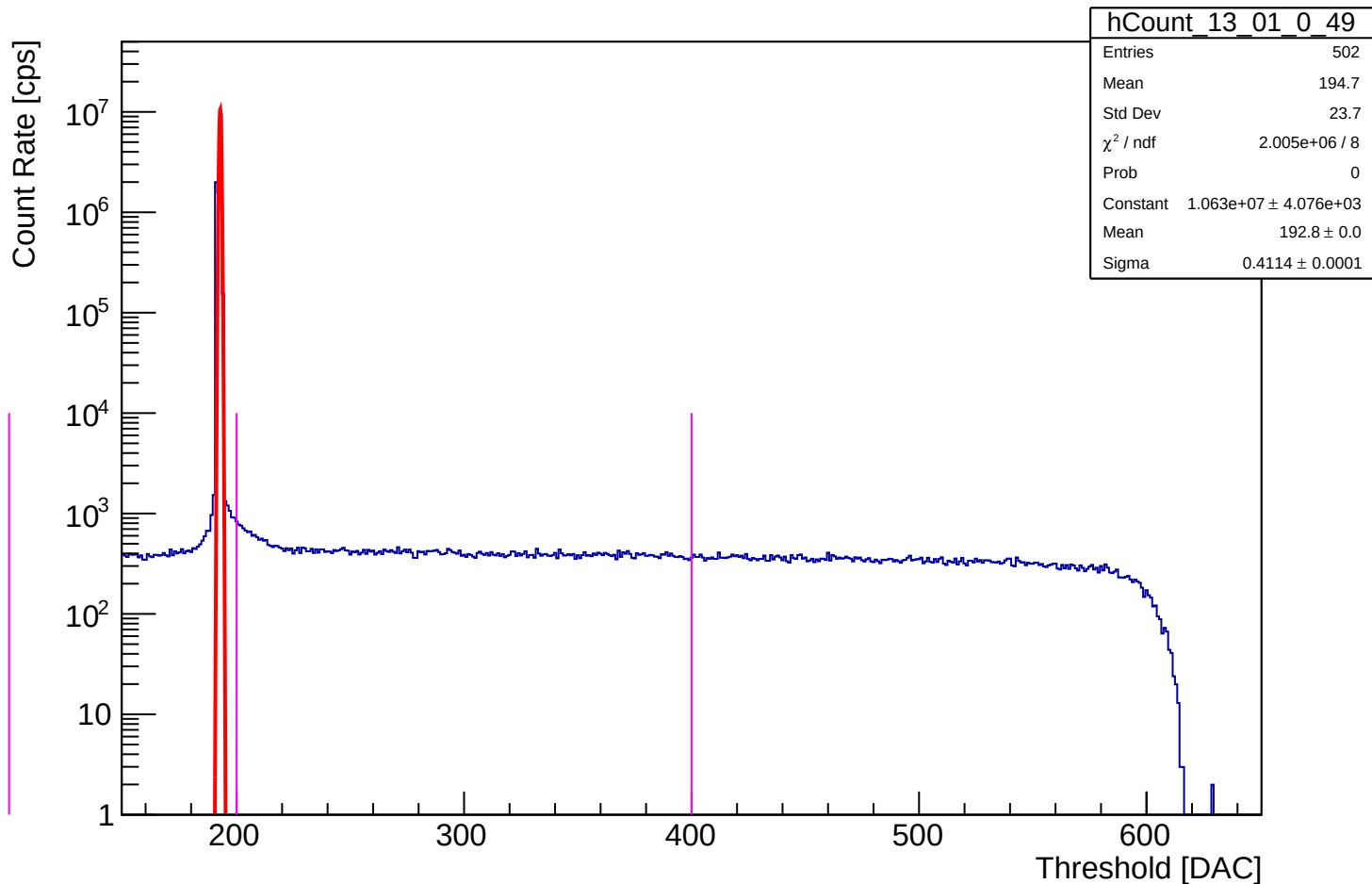
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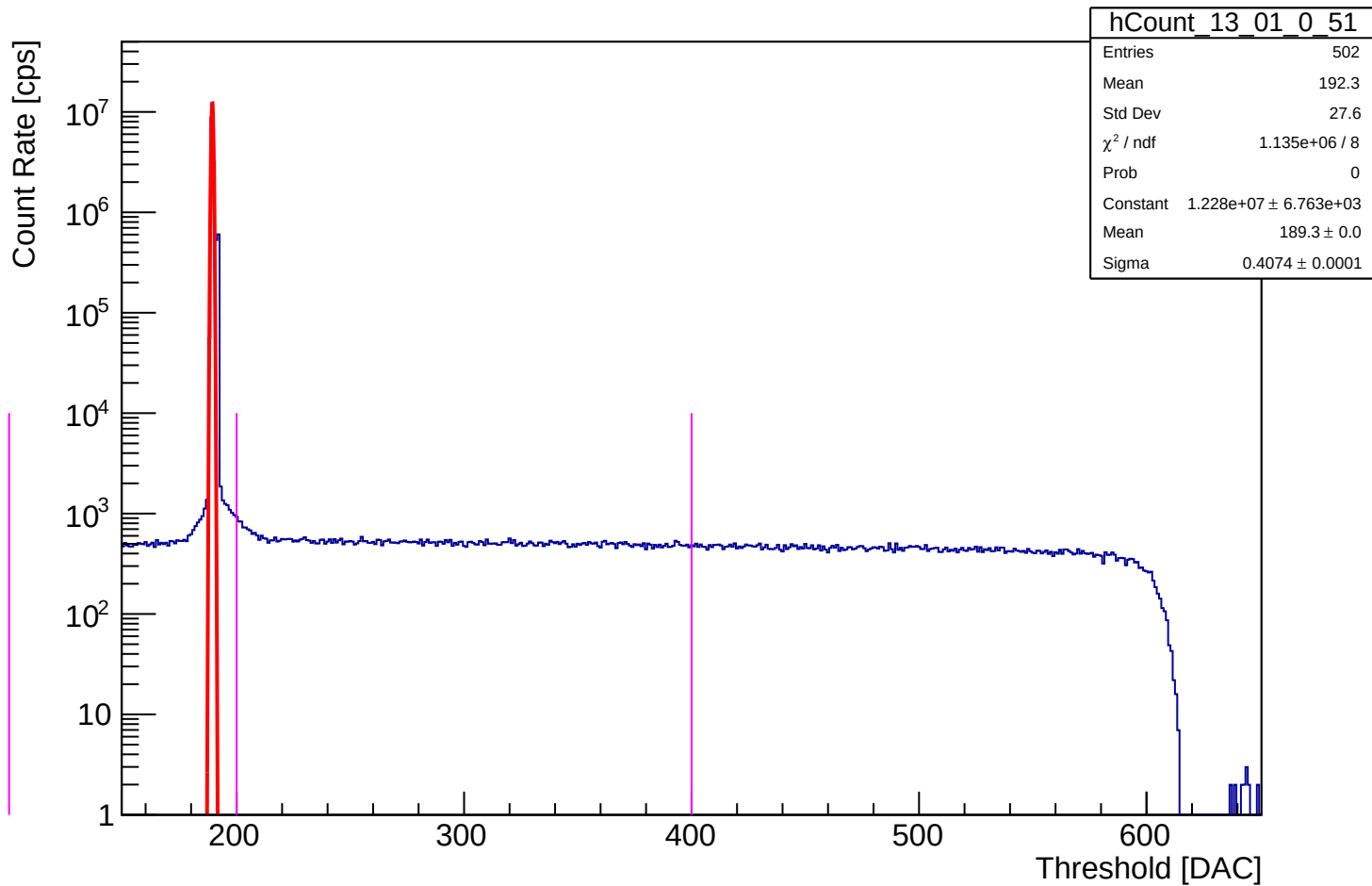
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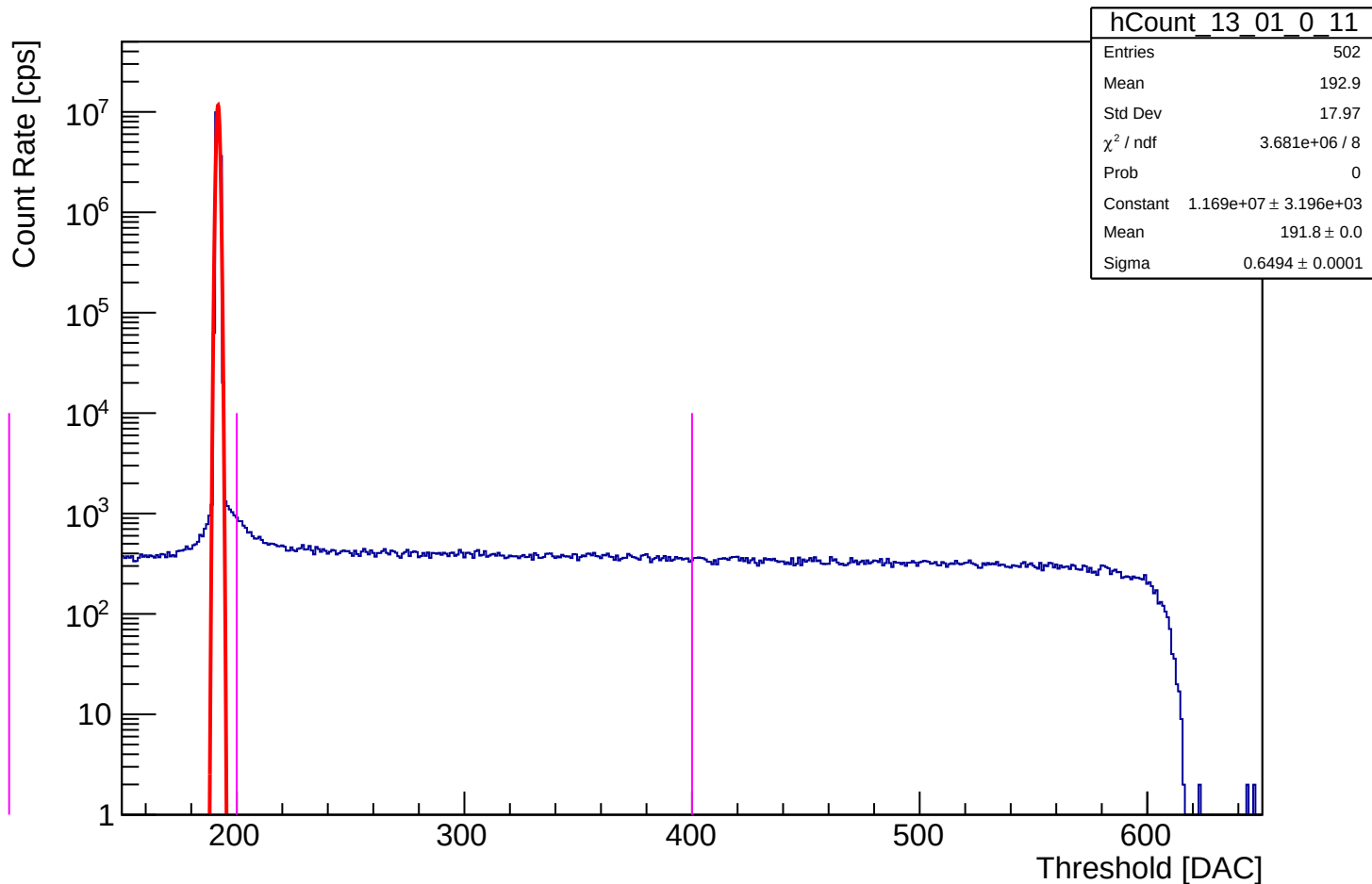
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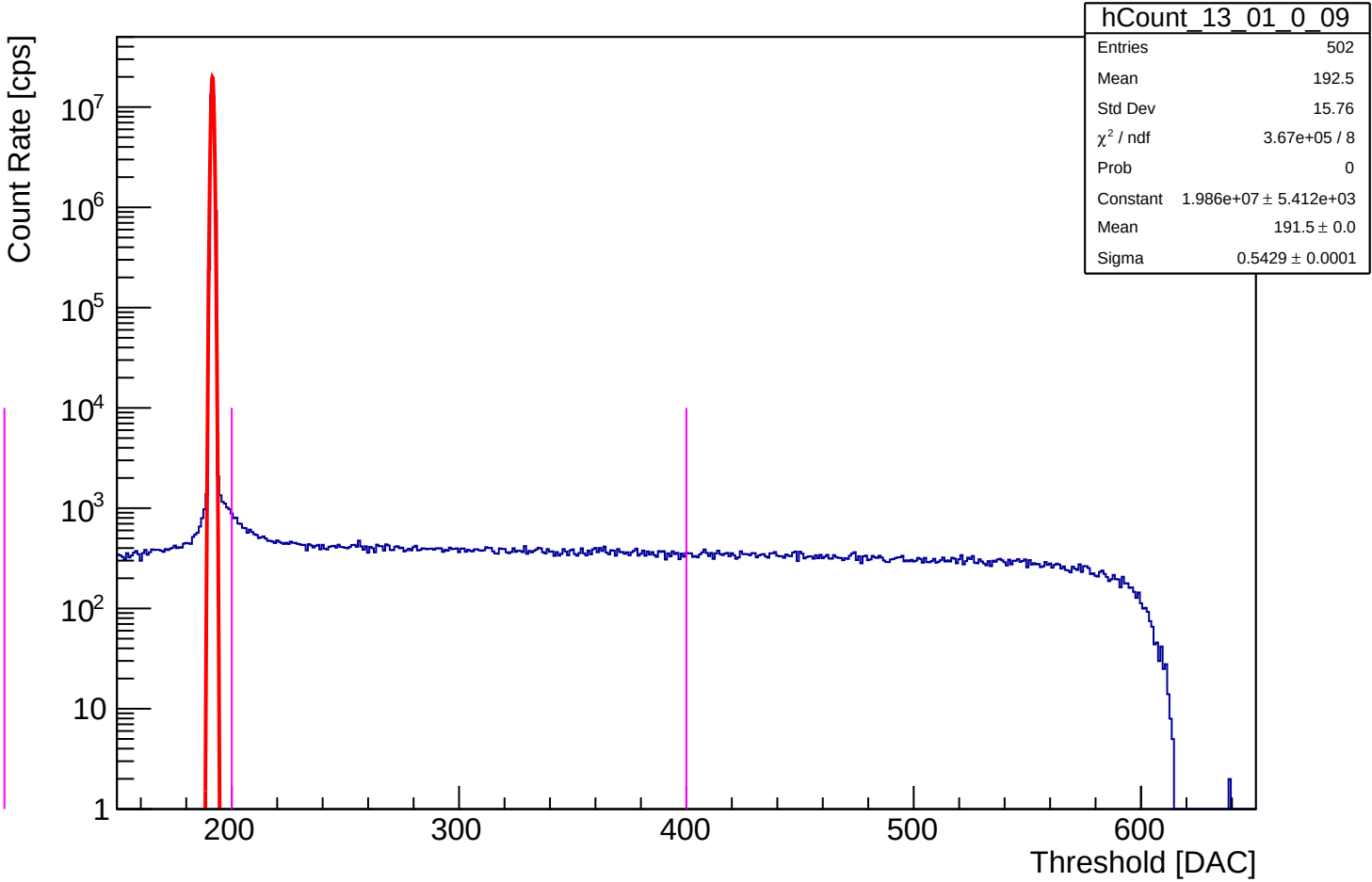


Row 1 Tile 1 Pmt 4 Pixel 40 Slot 13 Fiber 1 Asic 0 Channel 51

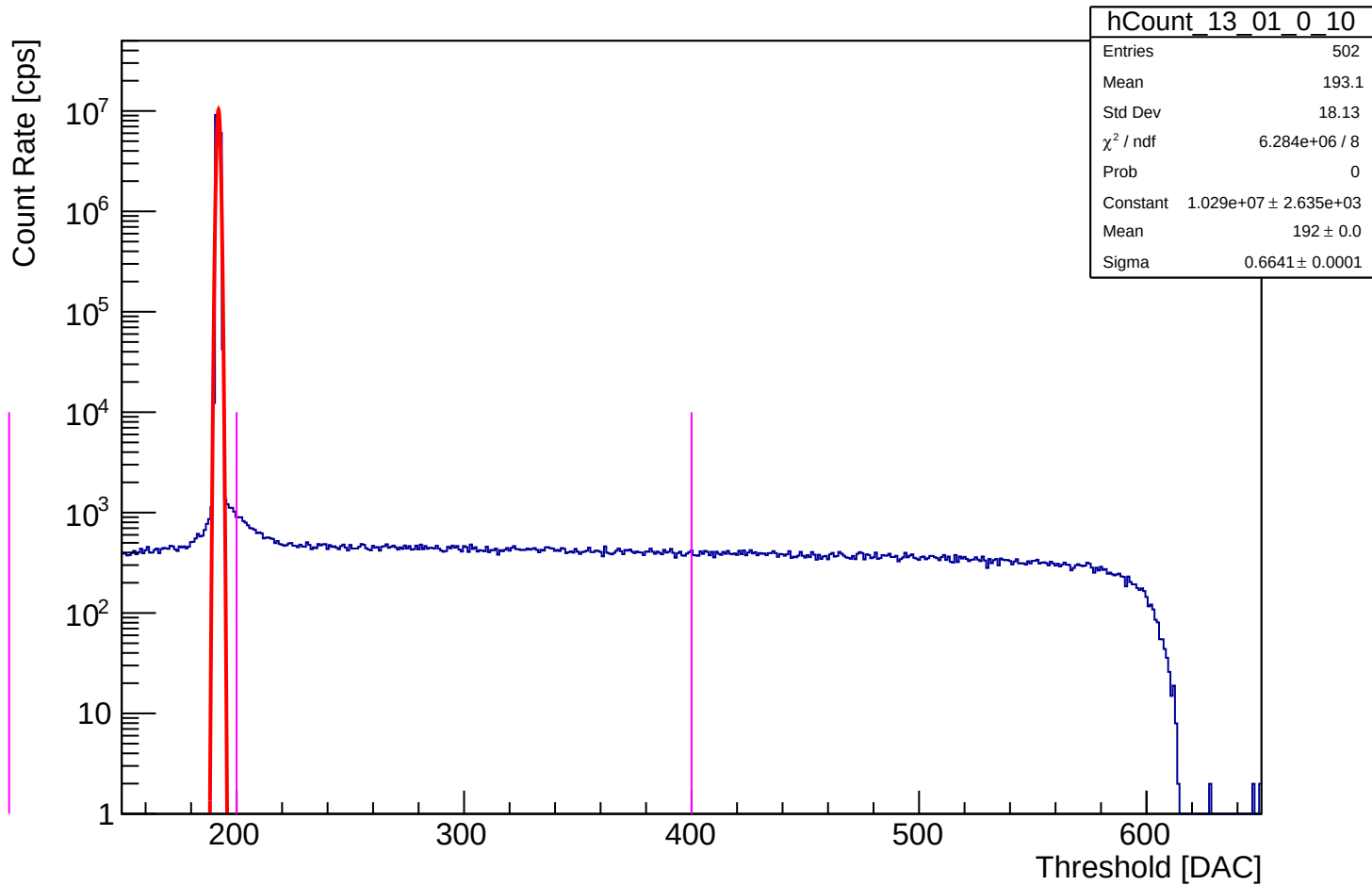


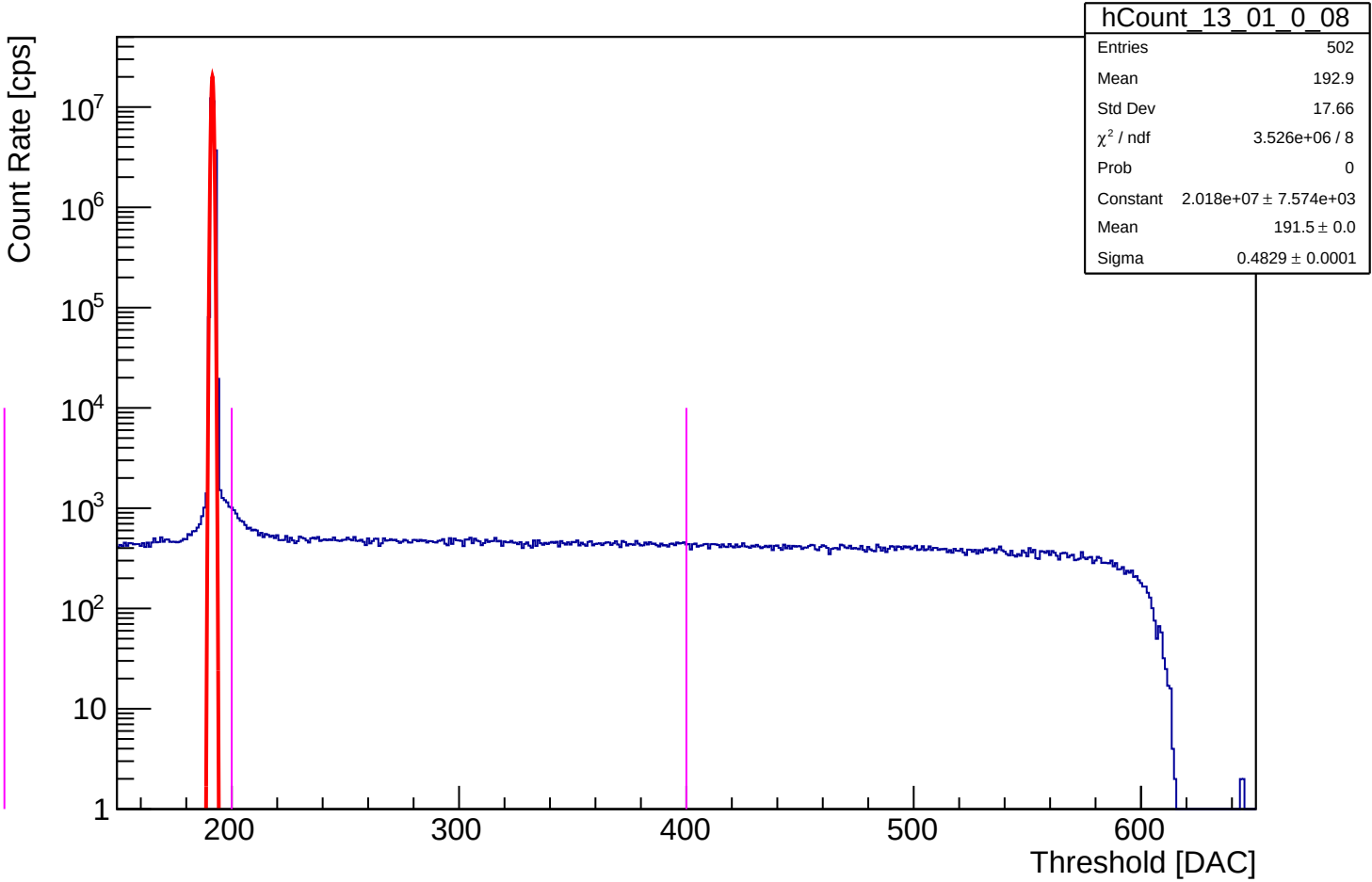
Row 1 Tile 1 Pmt 4 Pixel 41 Slot 13 Fiber 1 Asic 0 Channel 11



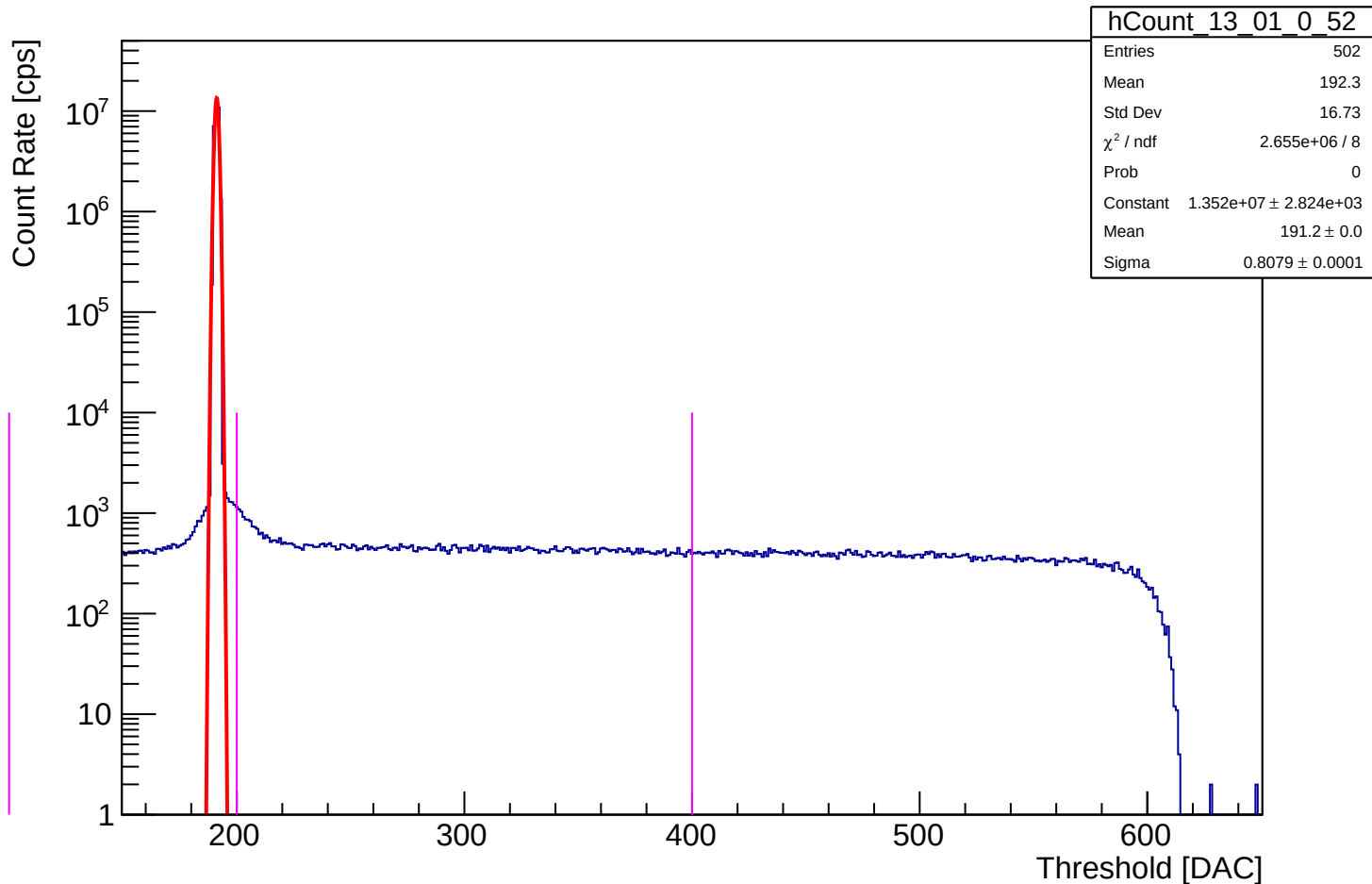


Row 1 Tile 1 Pmt 4 Pixel 43 Slot 13 Fiber 1 Asic 0 Channel 10

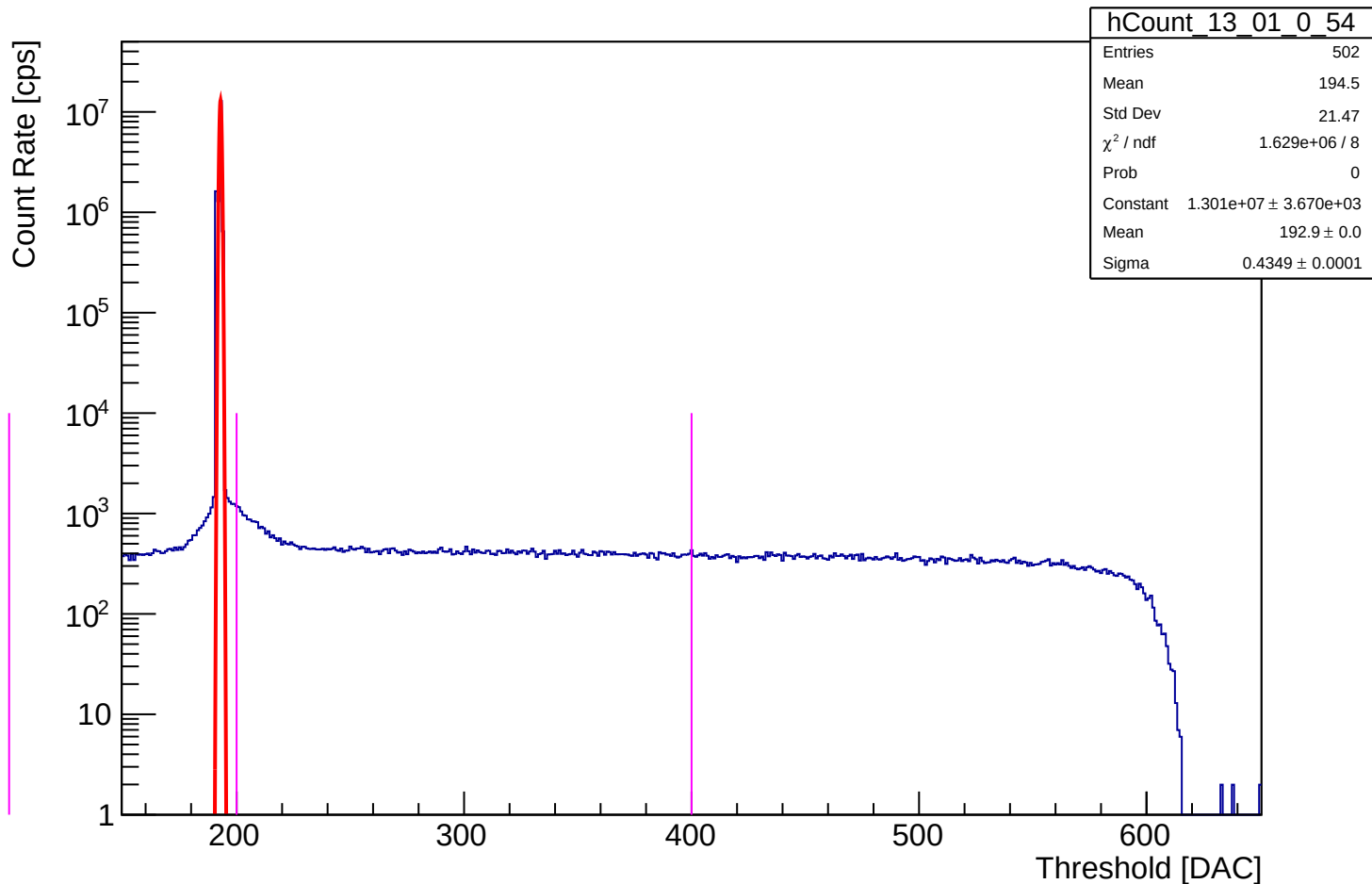




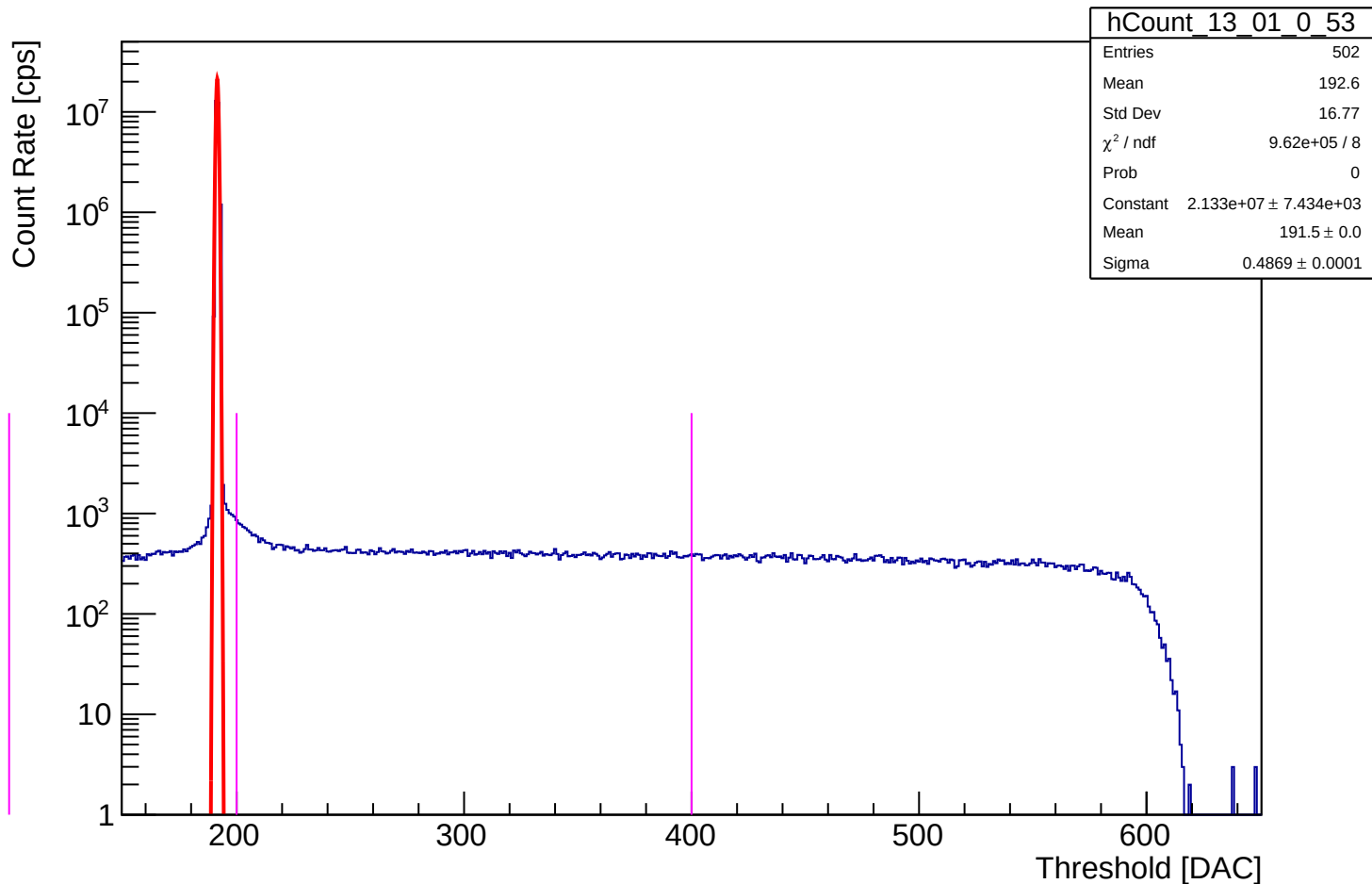
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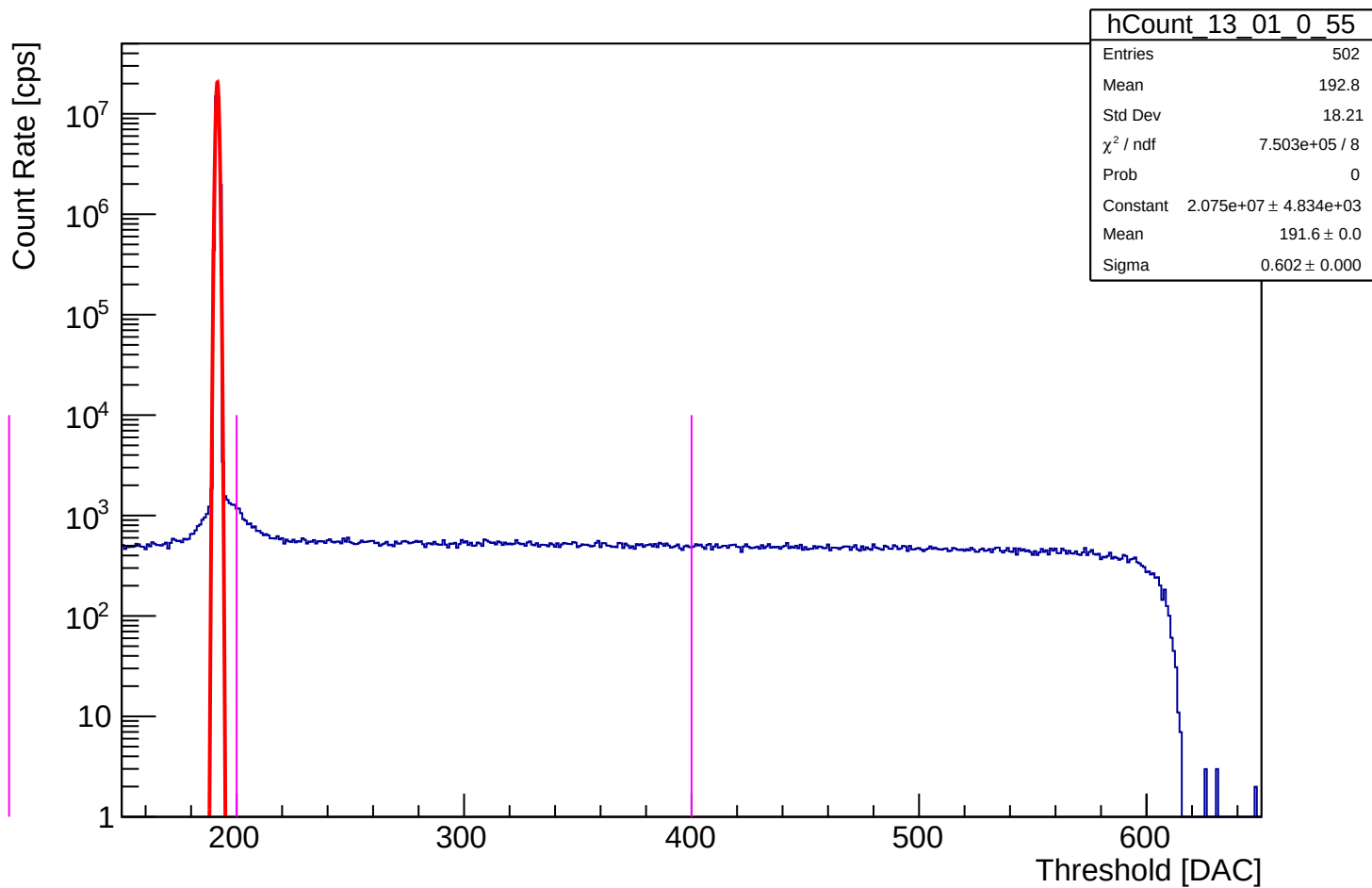
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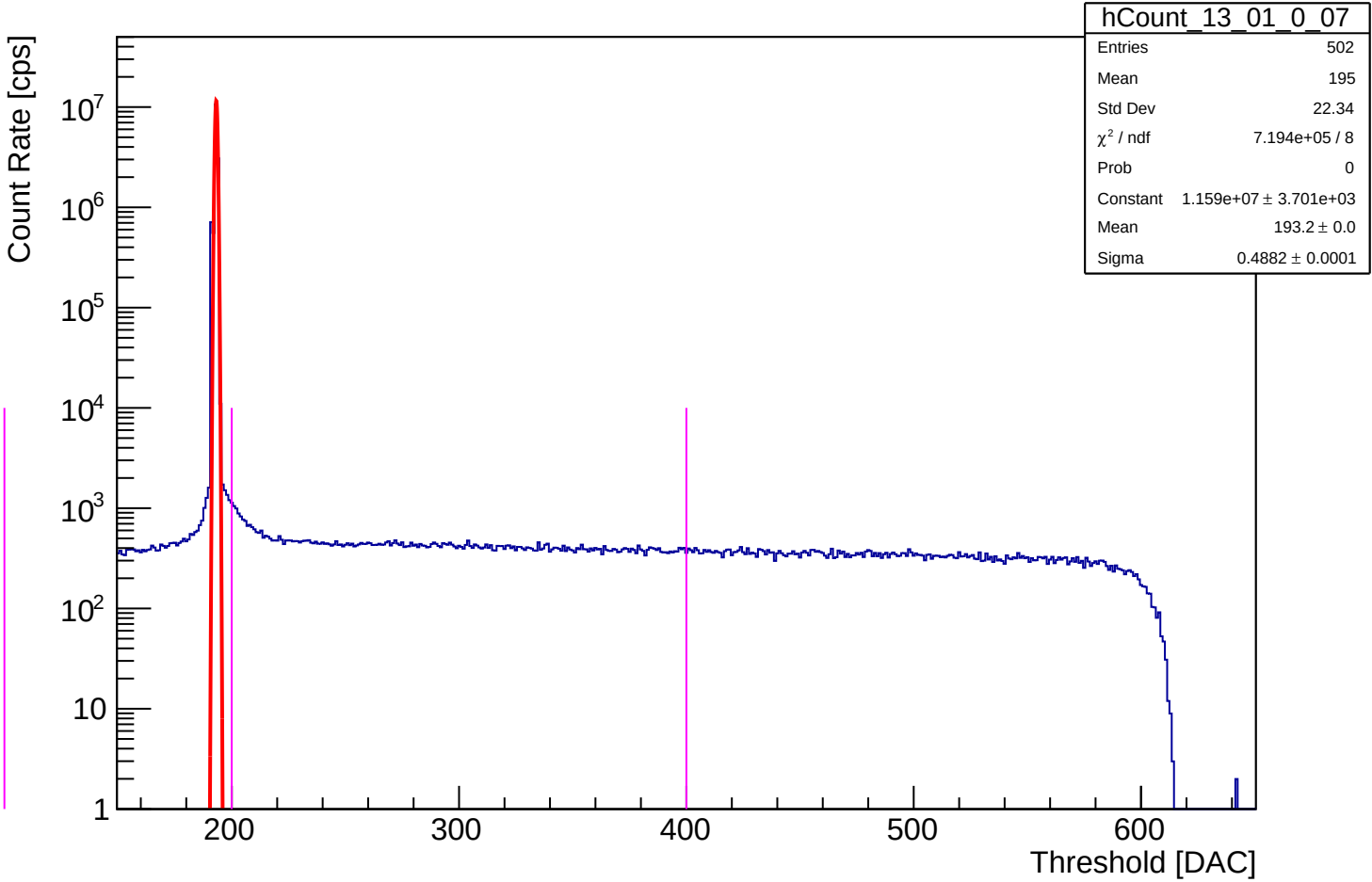


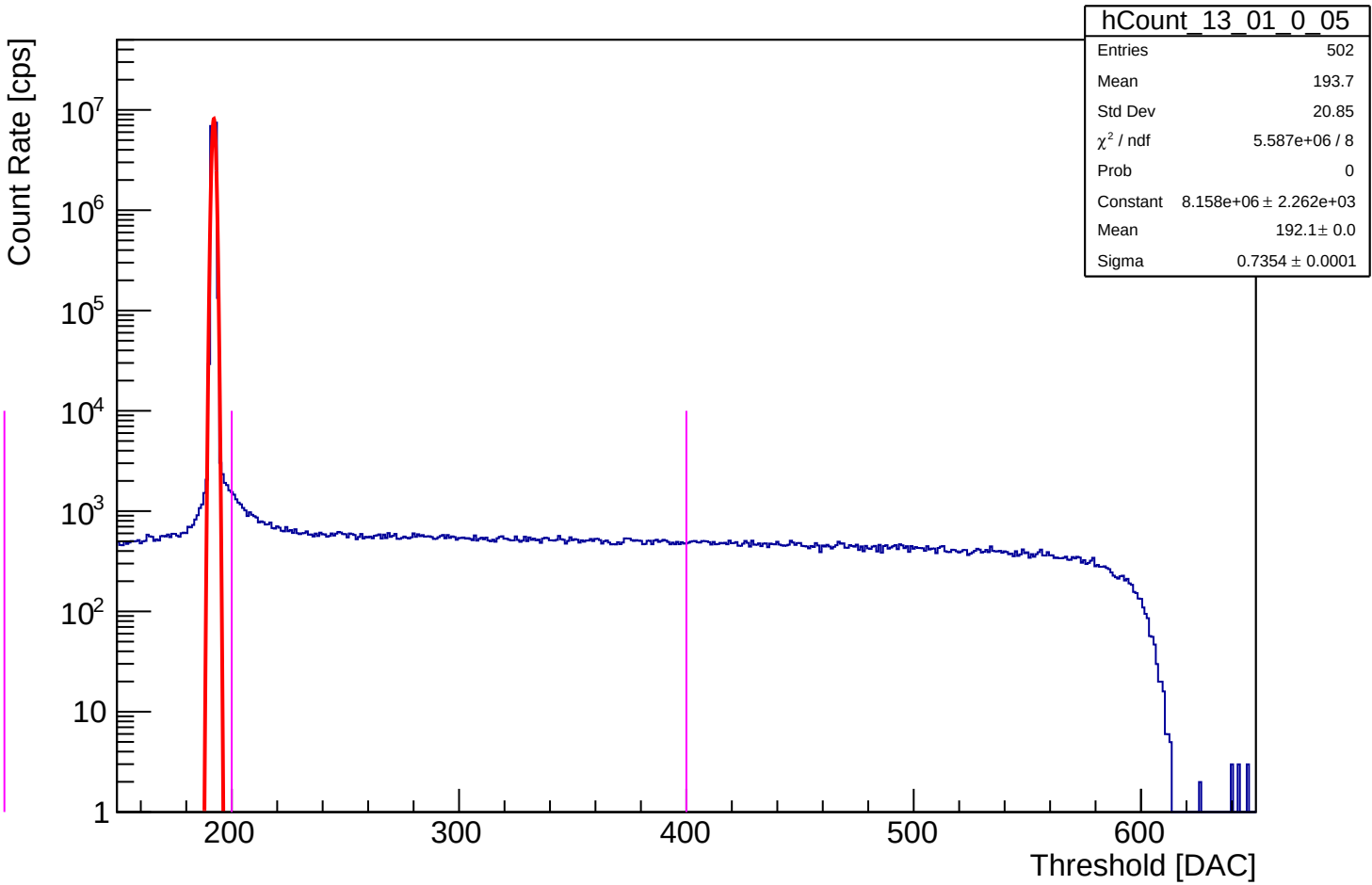
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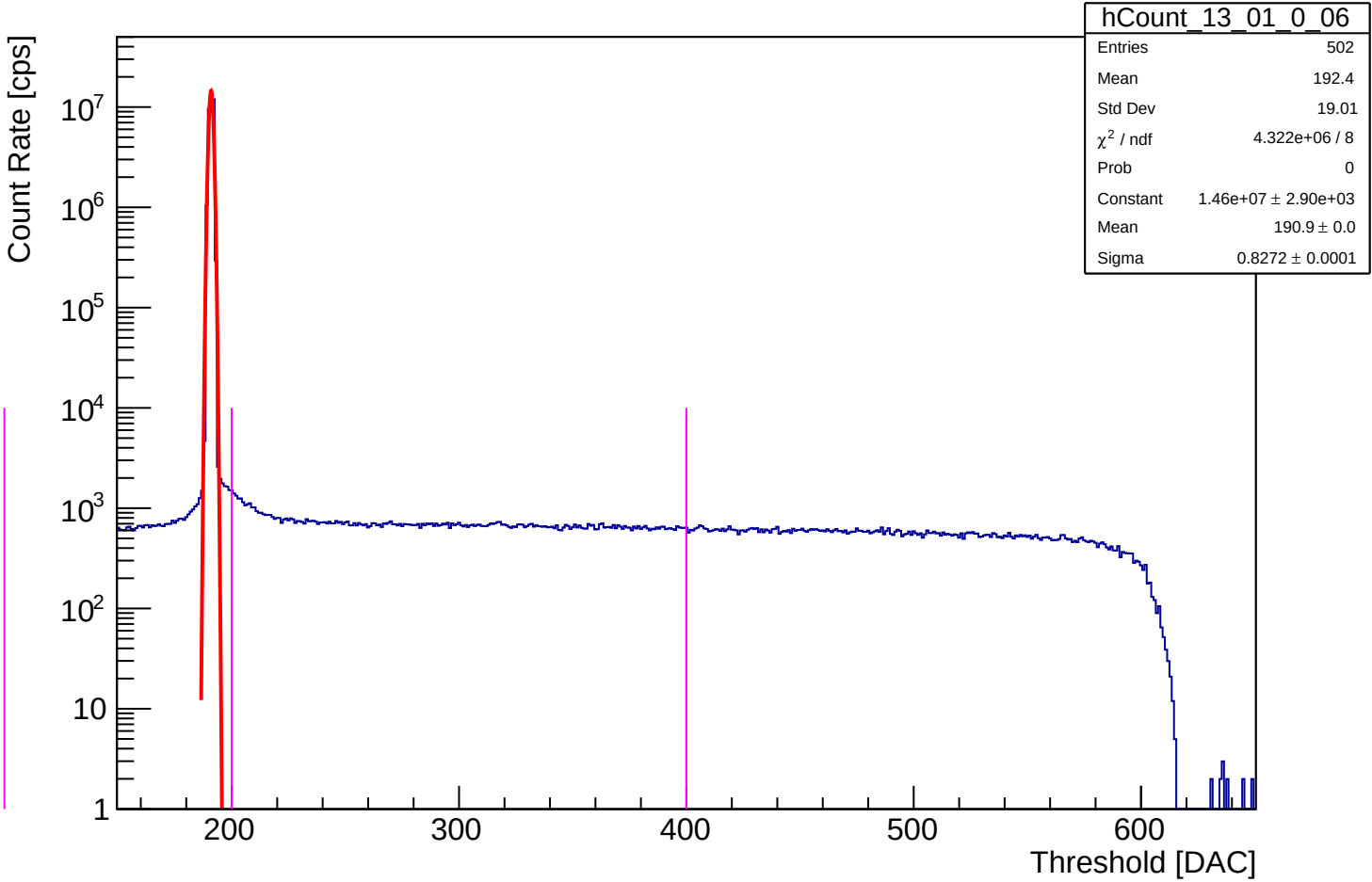


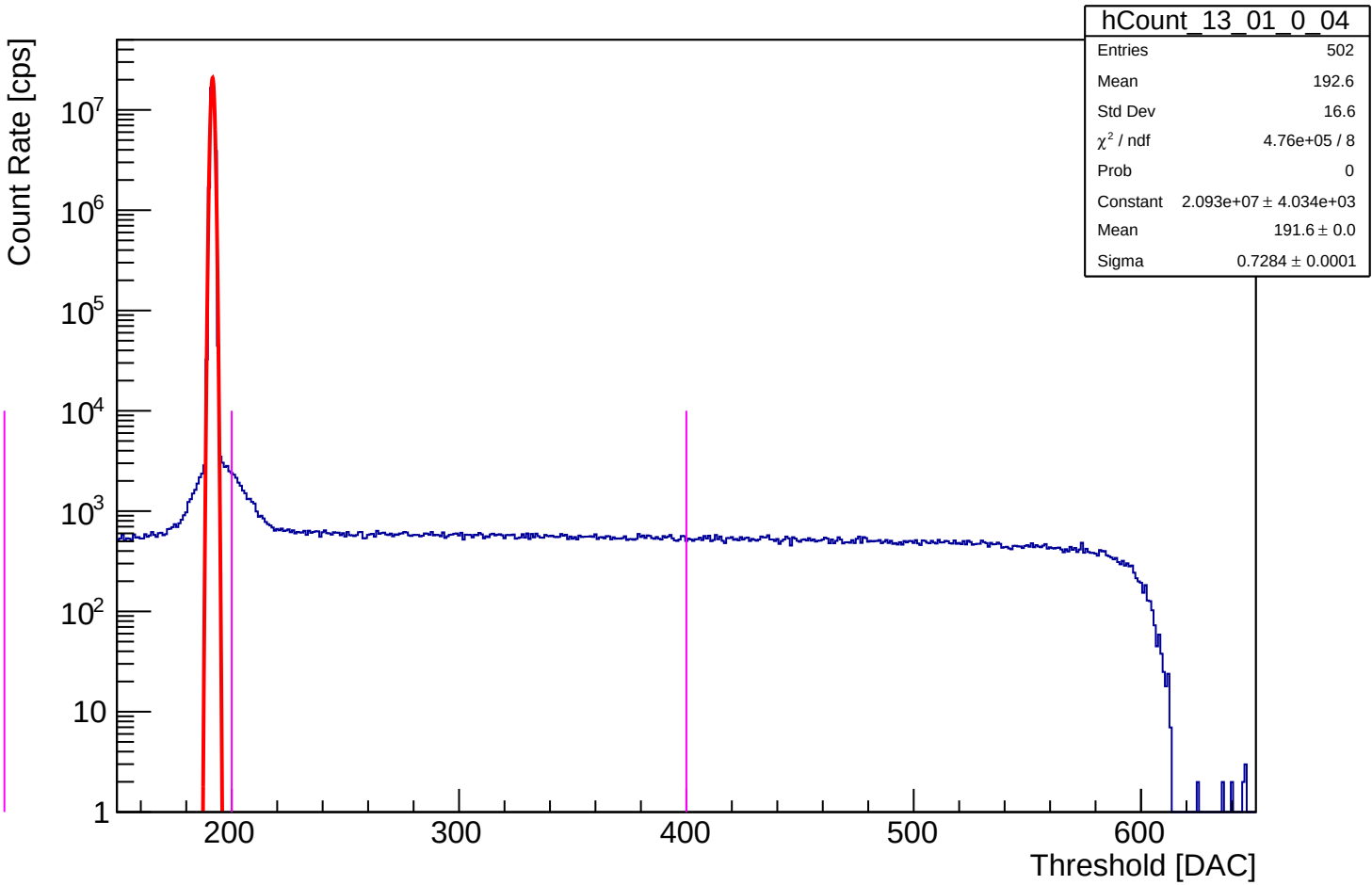
Row 1 Tile 1 Pmt 4 Pixel 48 Slot 13 Fiber 1 Asic 0 Channel 55



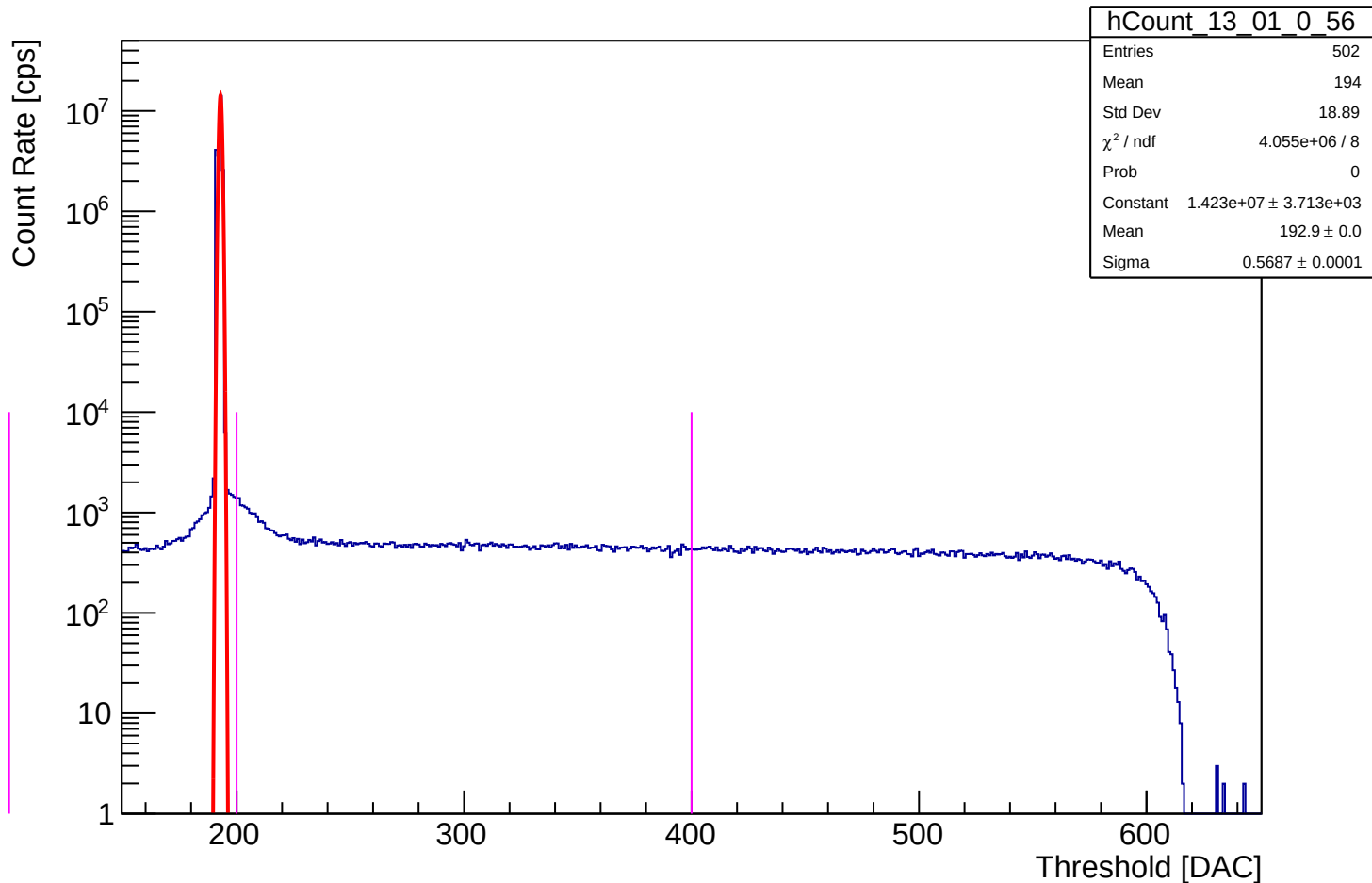




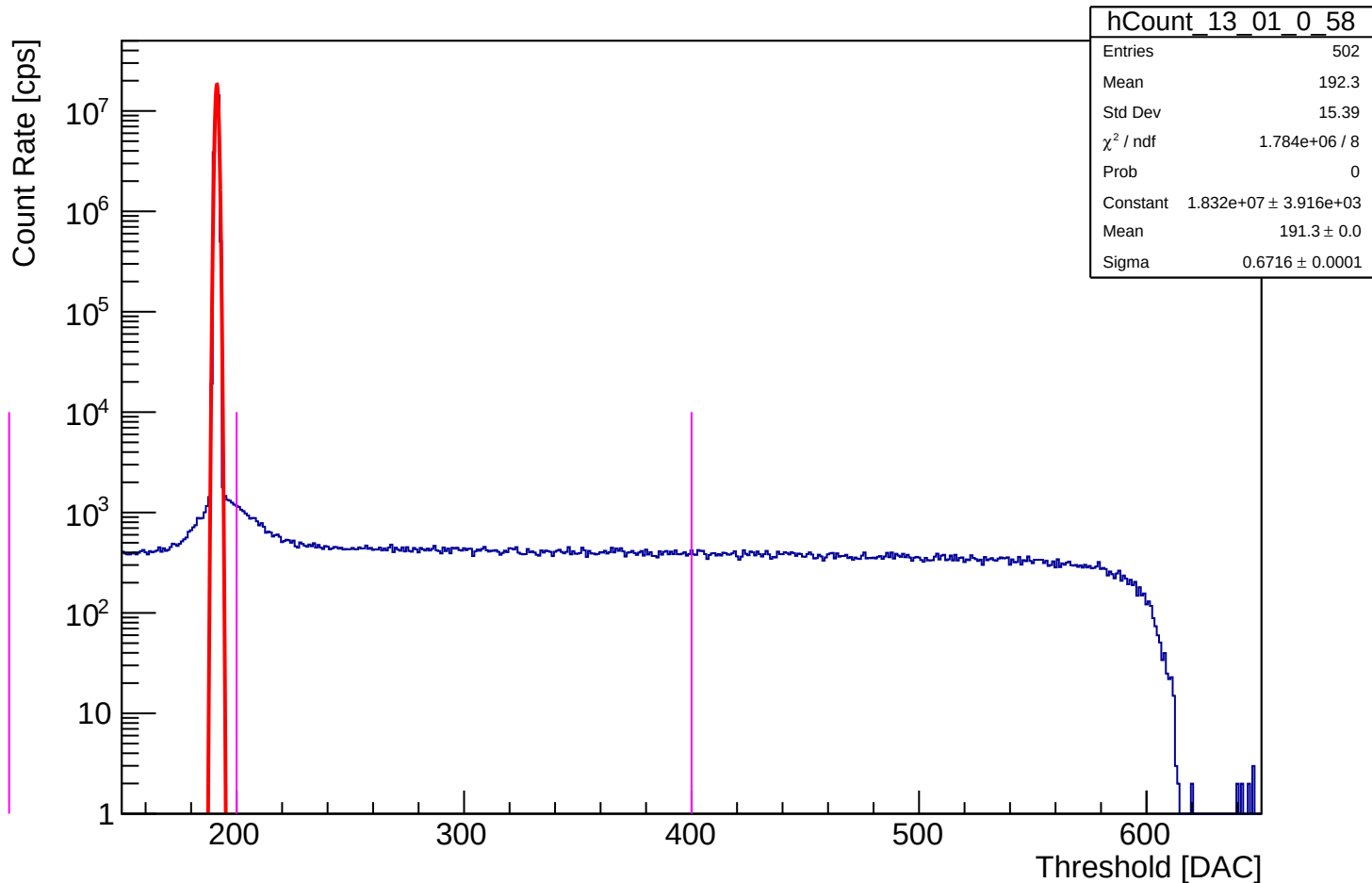




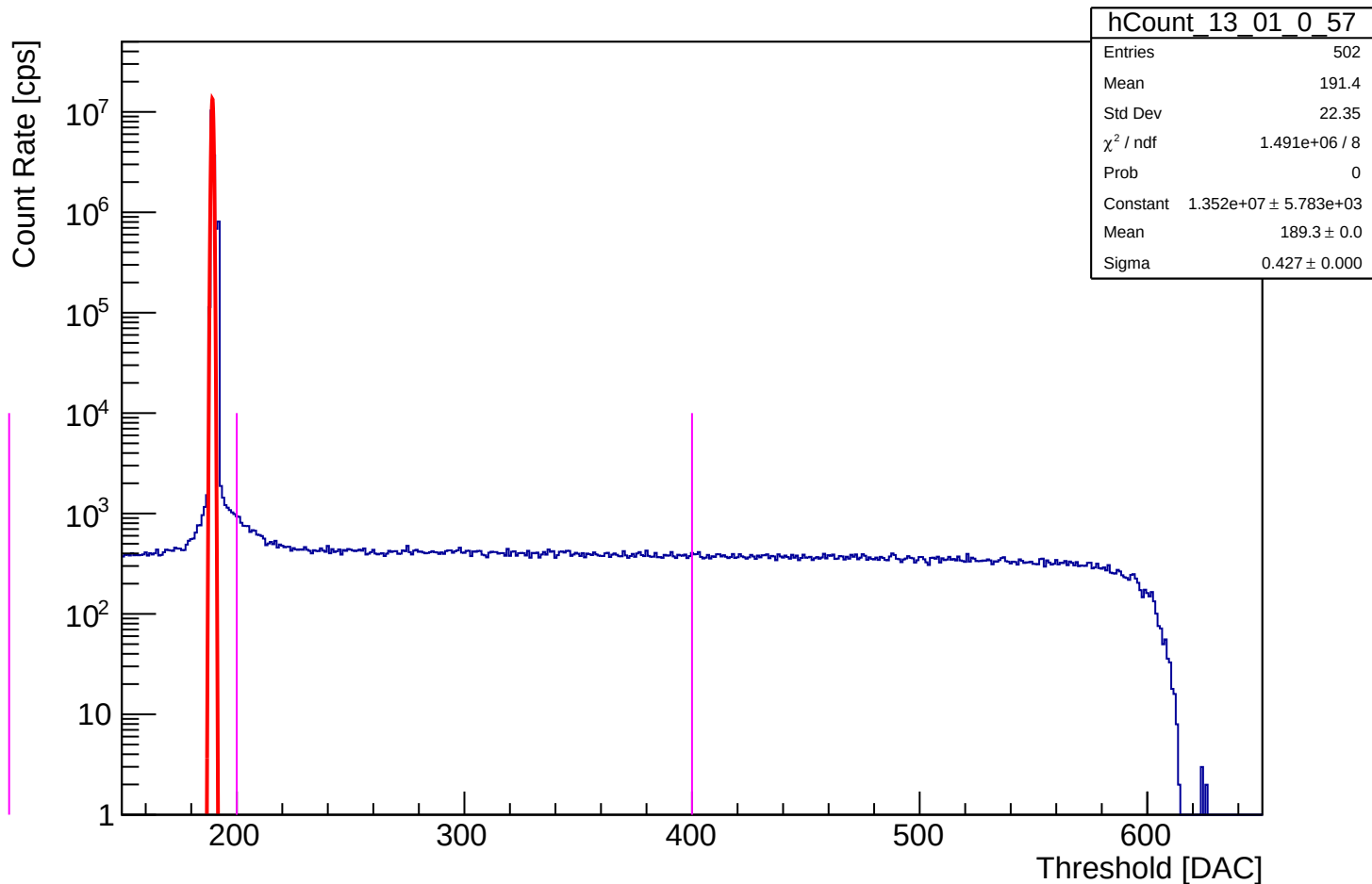
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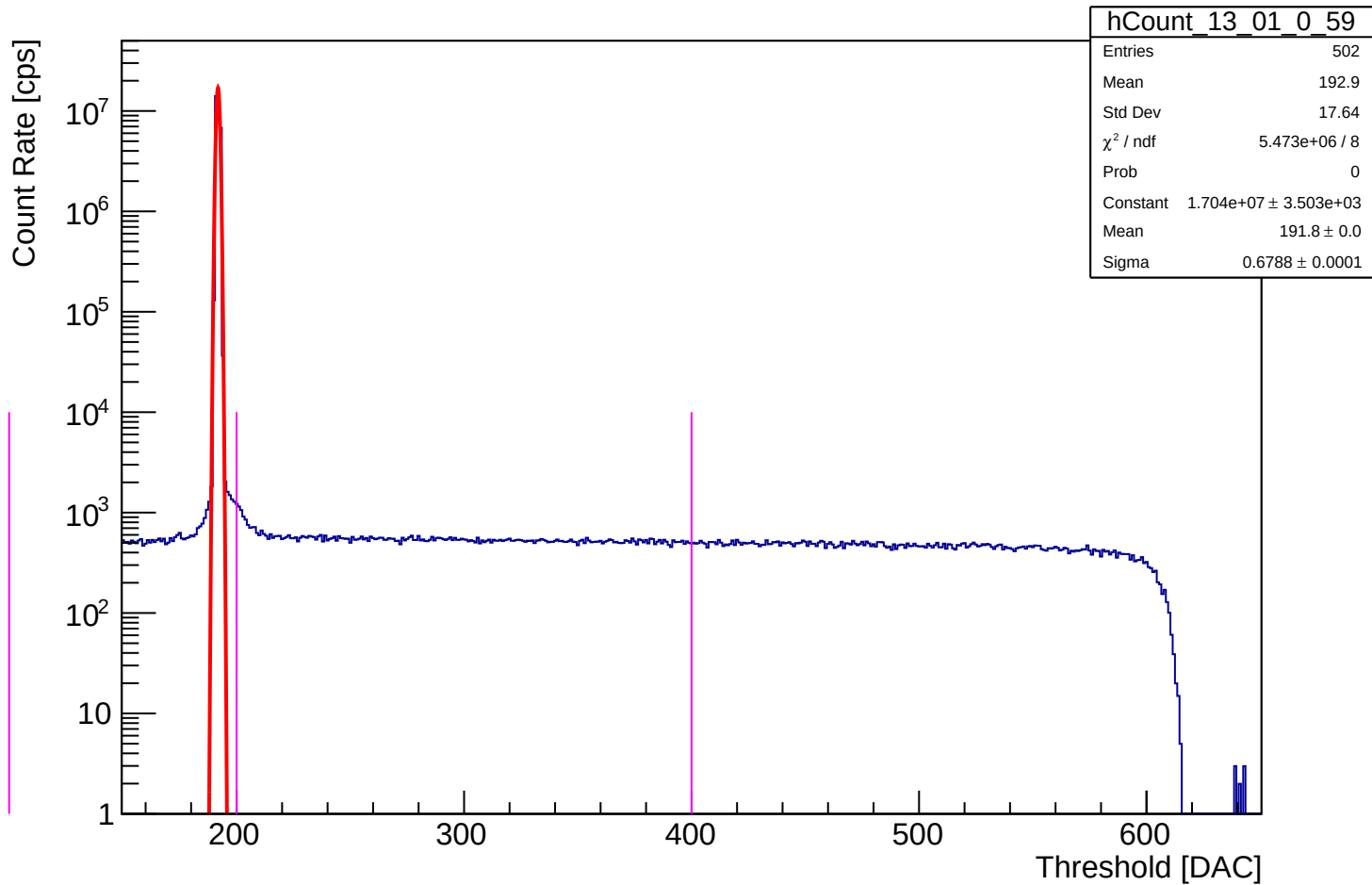
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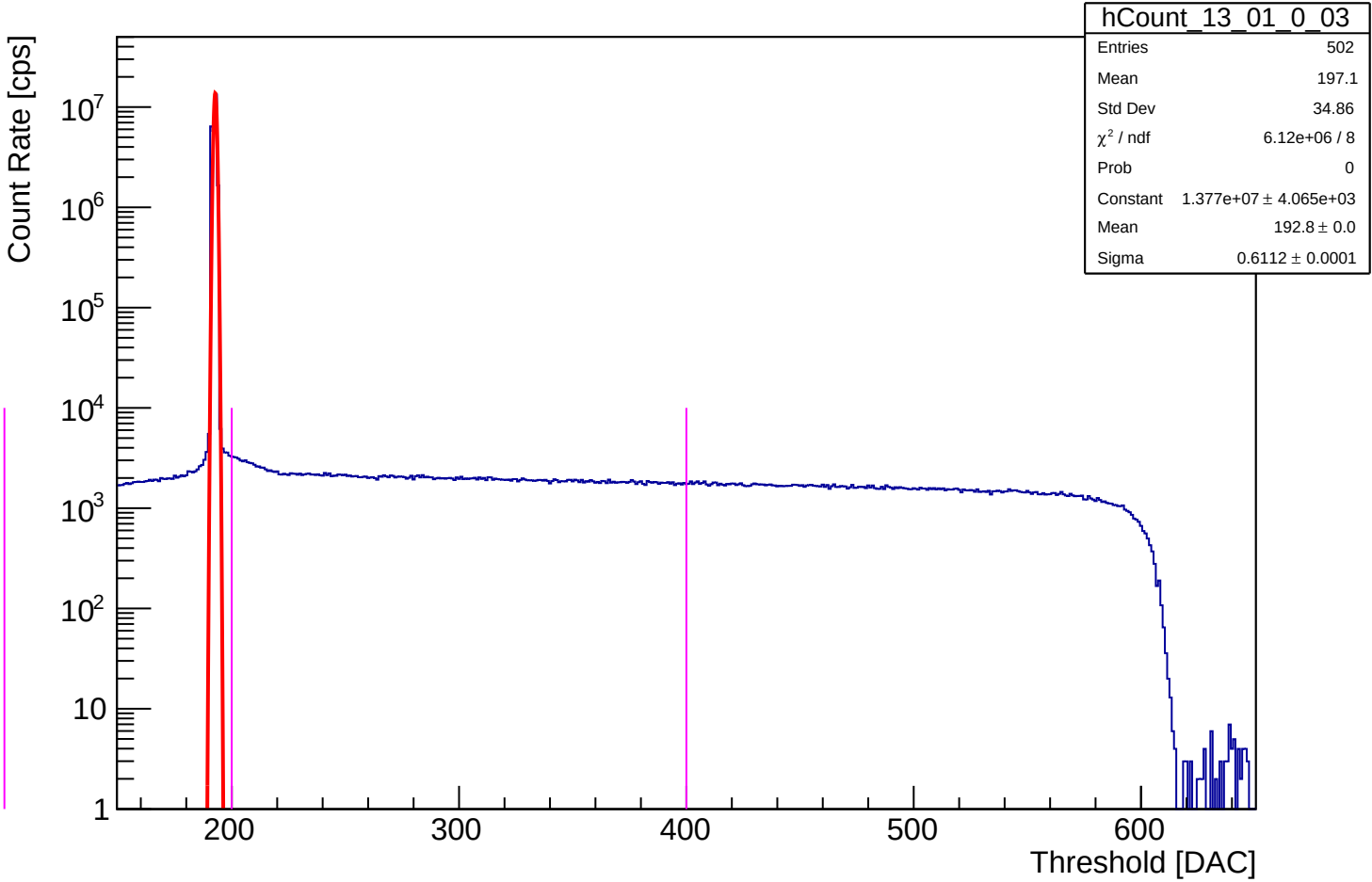


Row 1 Tile 1 Pmt 4 Pixel 55 Slot 13 Fiber 1 Asic 0 Channel 57

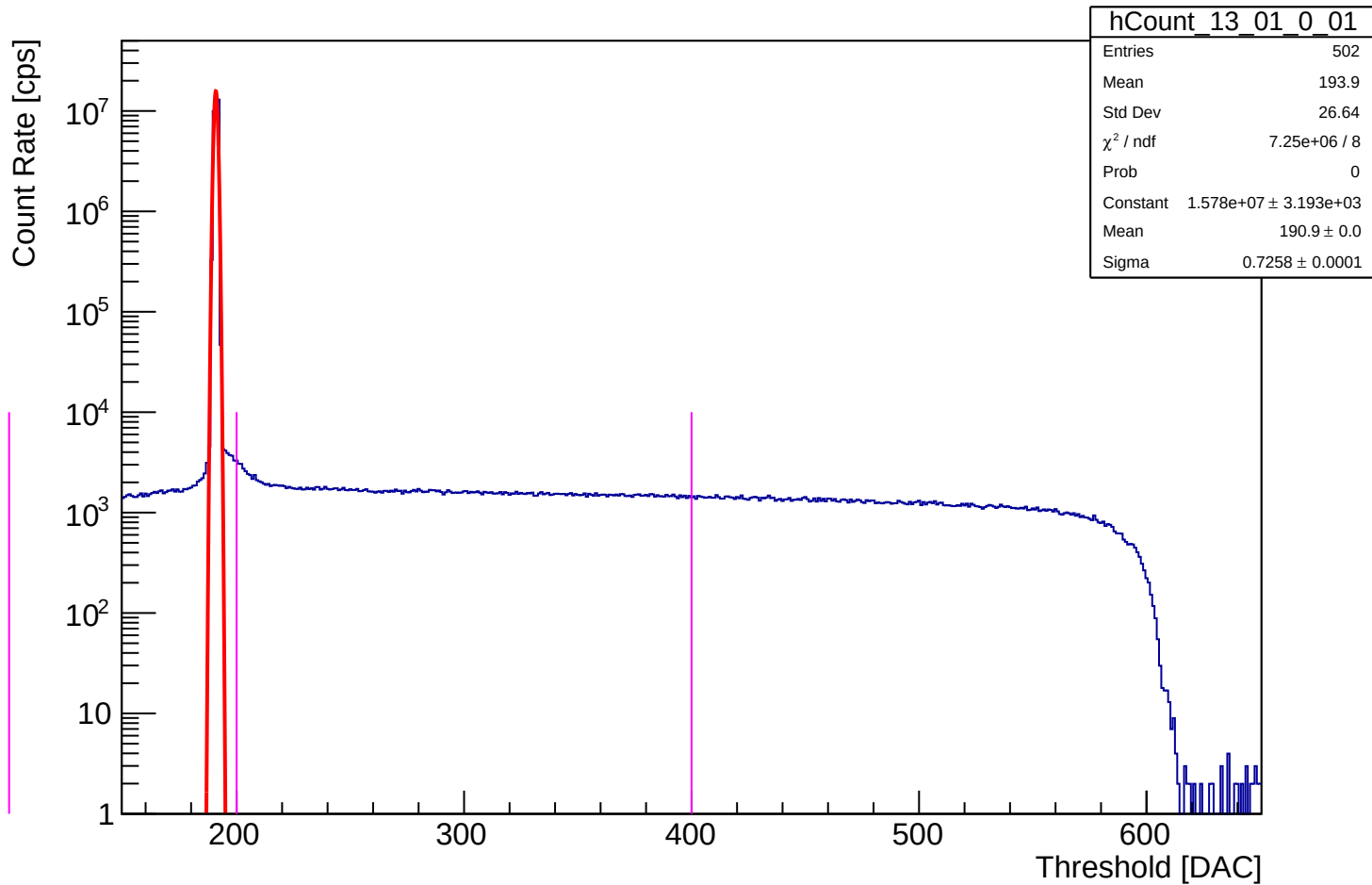


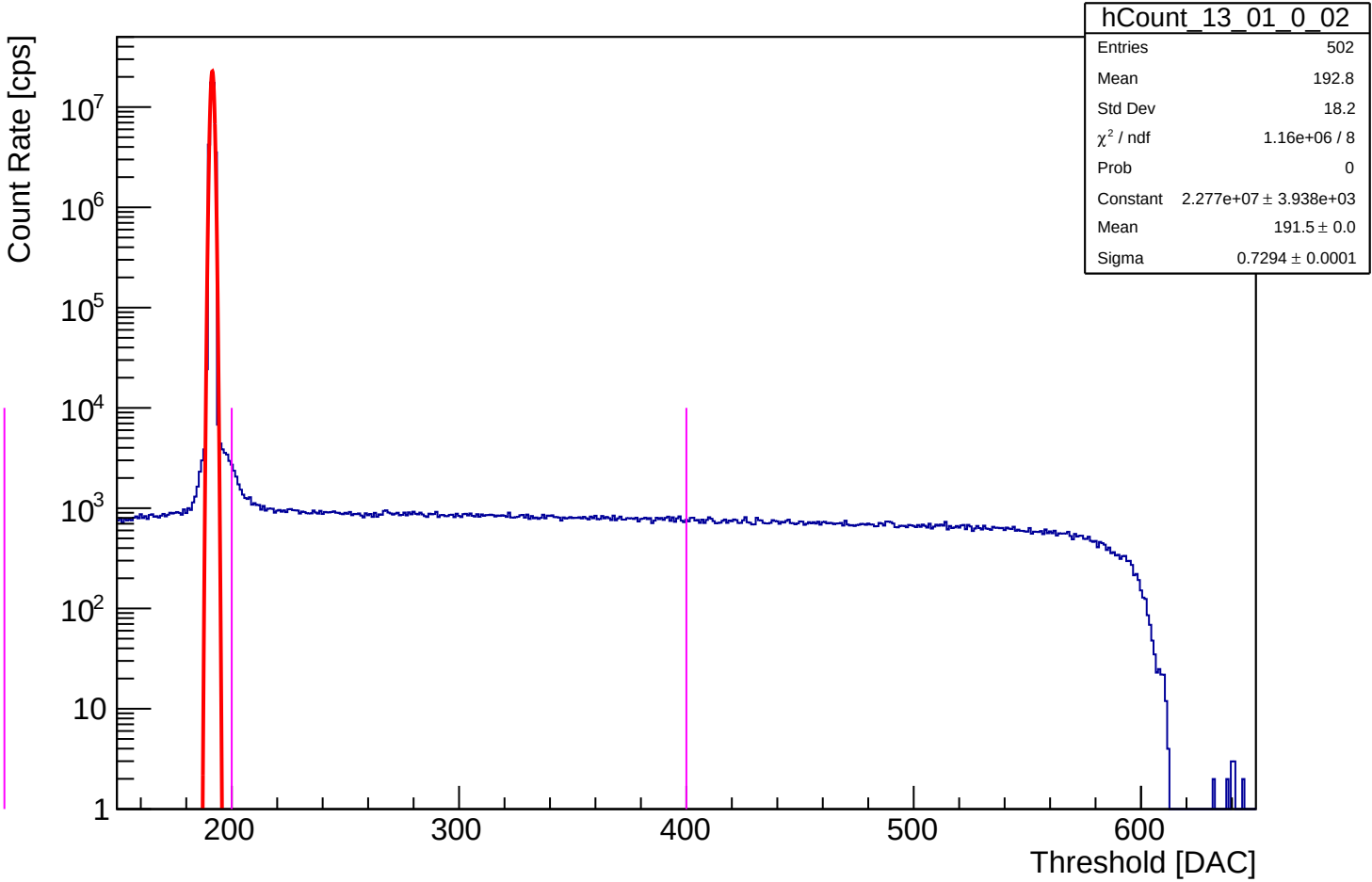
Row 1 Tile 1 Pmt 4 Pixel 56 Slot 13 Fiber 1 Asic 0 Channel 59

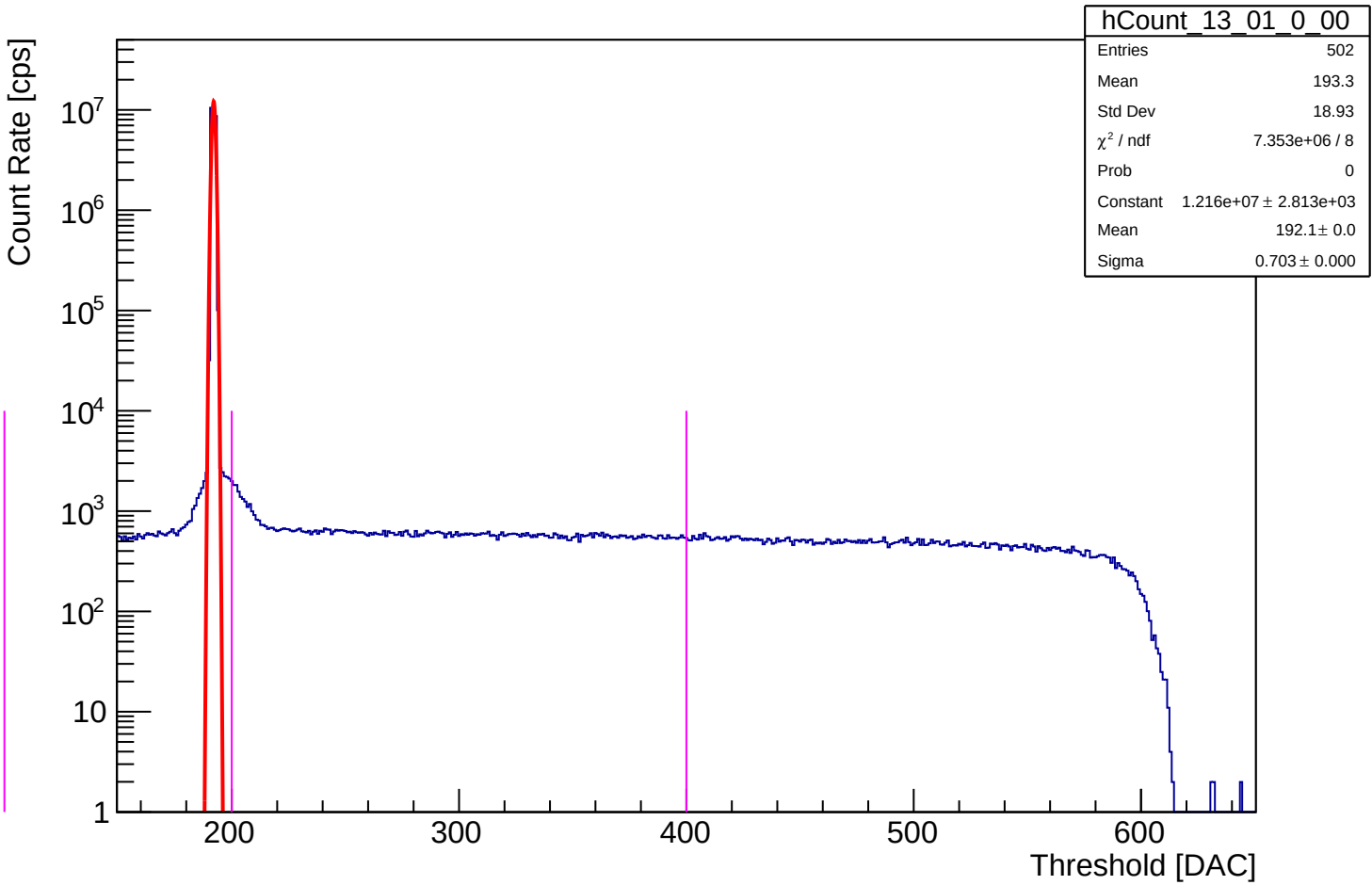




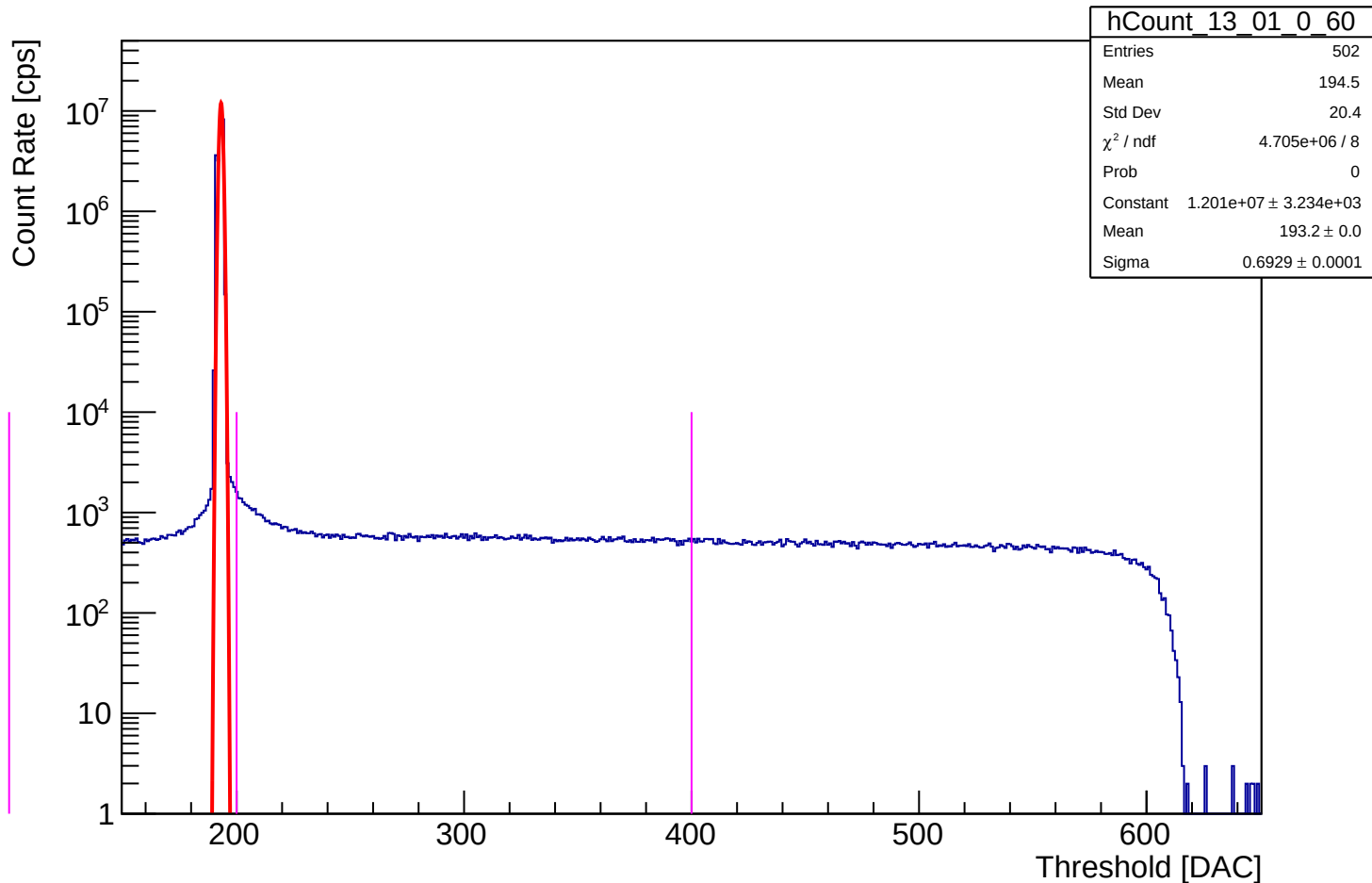
Row 1 Tile 1 Pmt 4 Pixel 58 Slot 13 Fiber 1 Asic 0 Channel 1



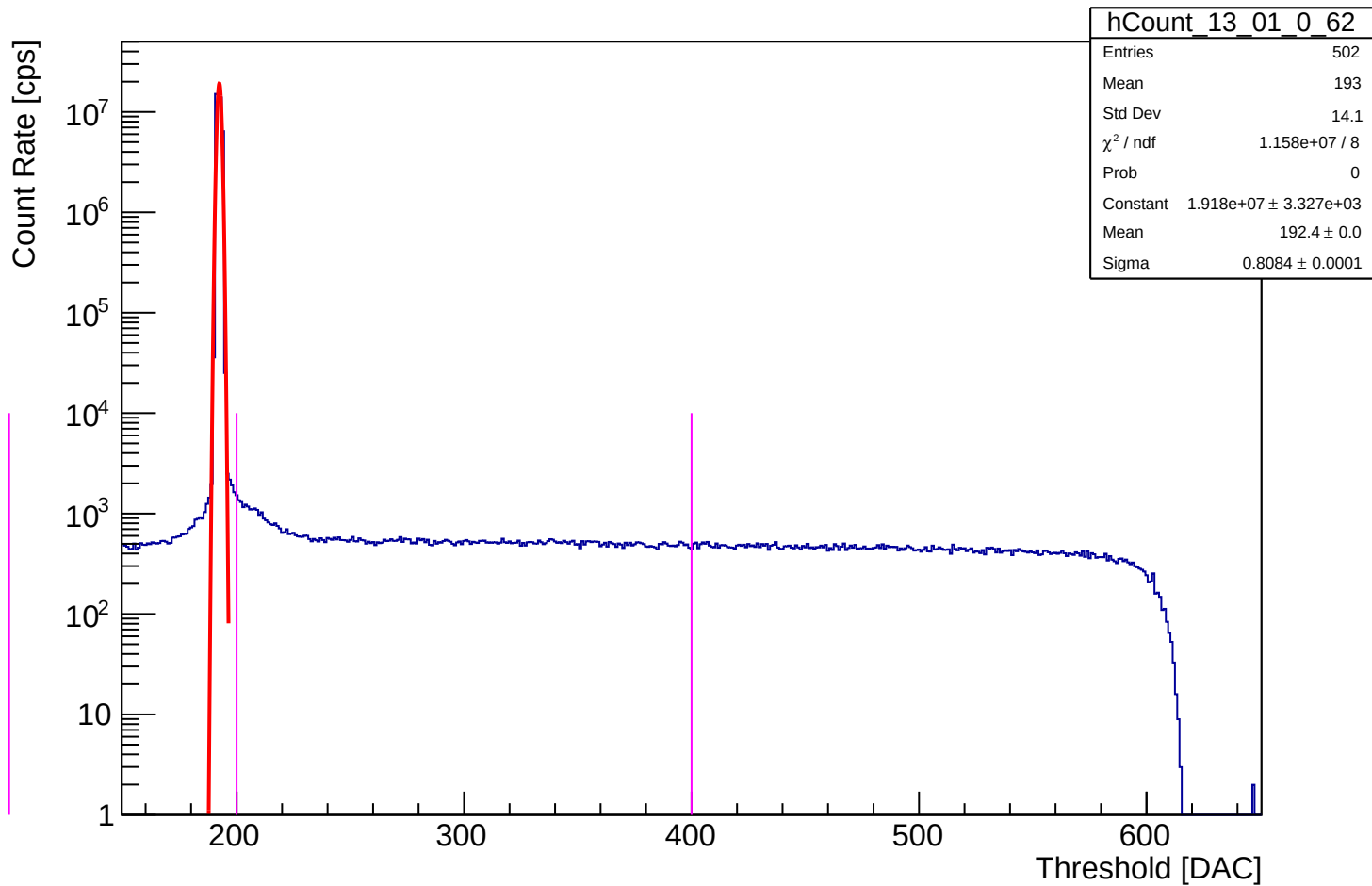




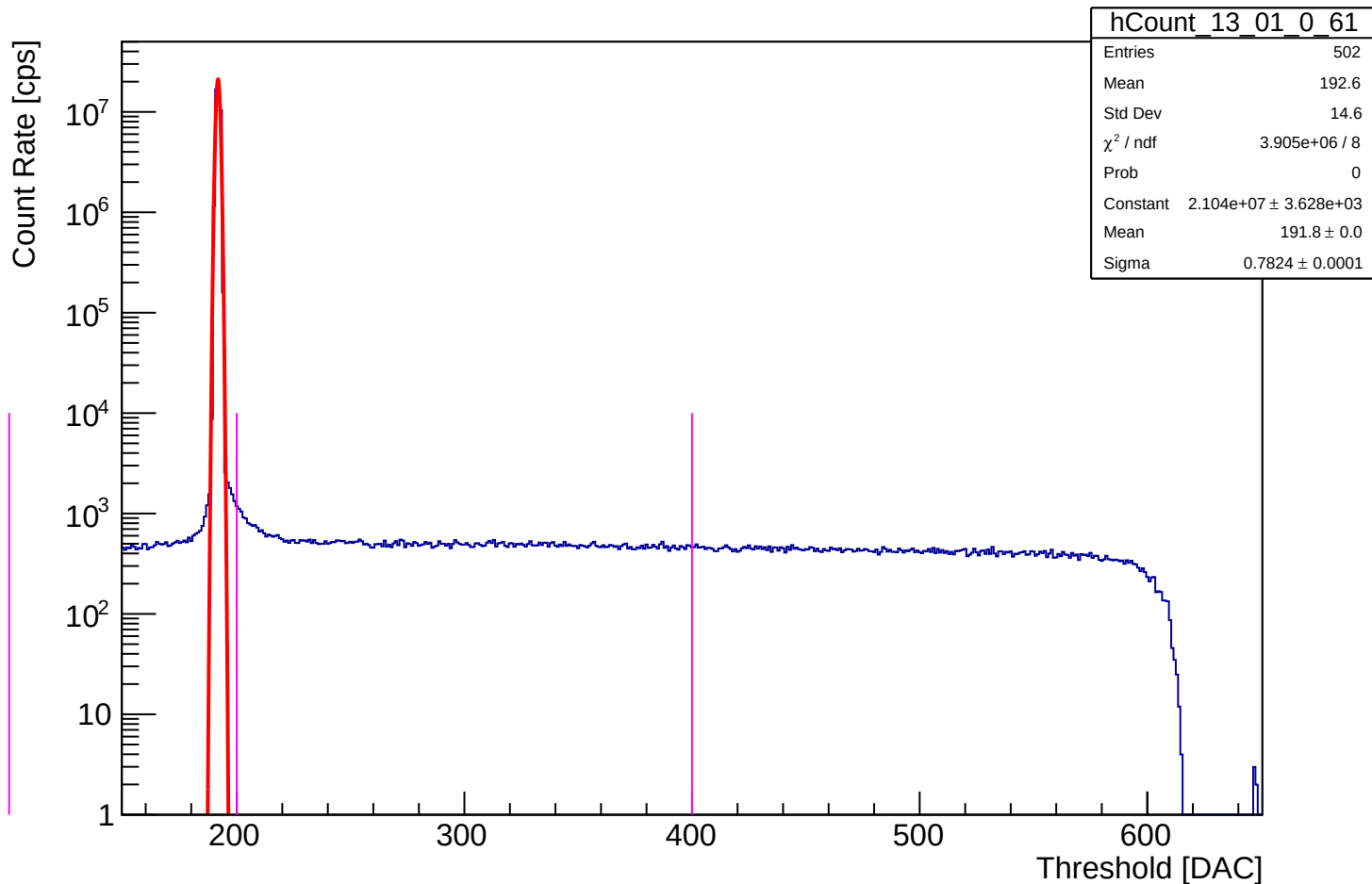
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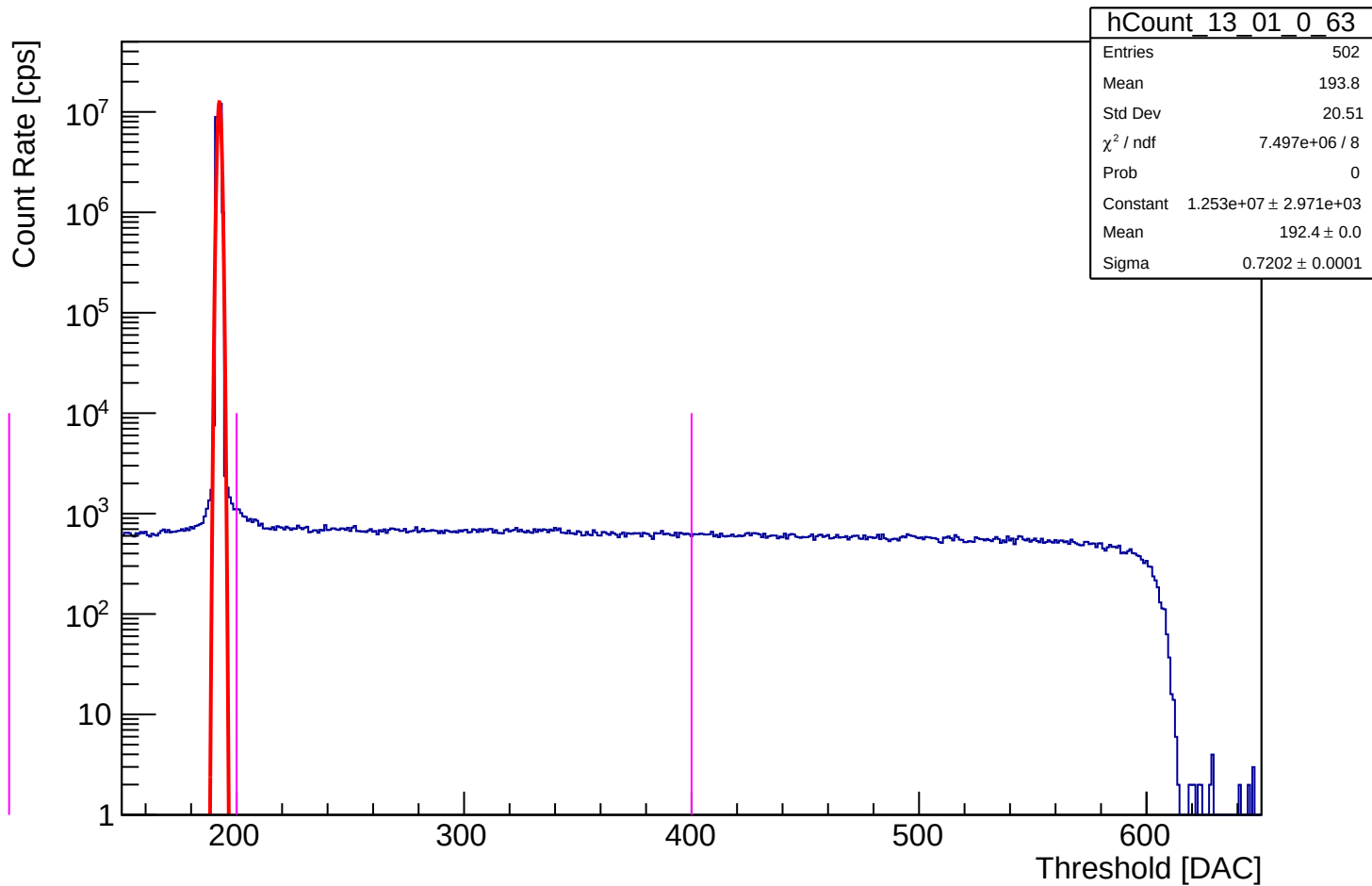
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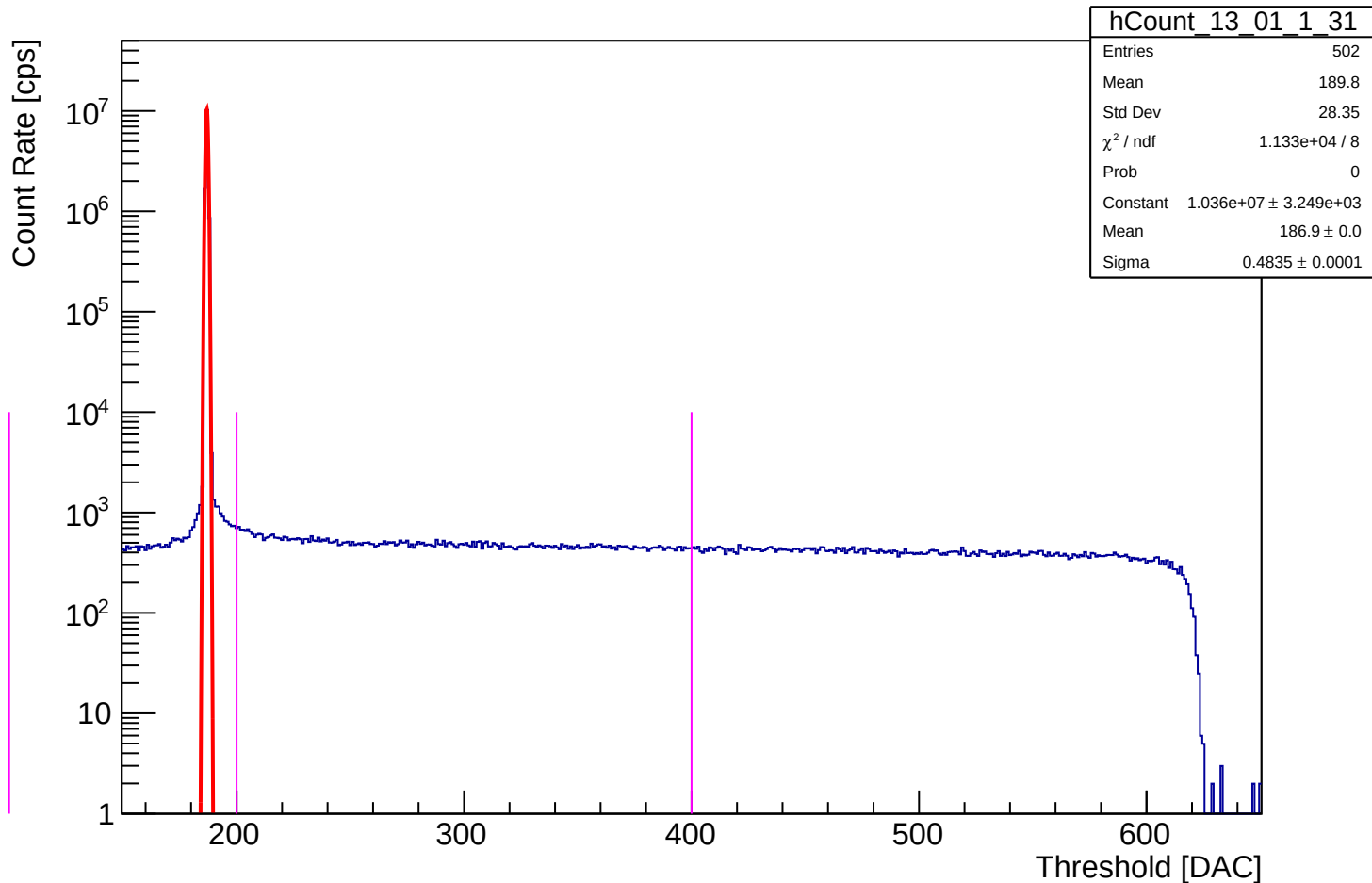
Row 1 Tile 1 Pmt 4 Pixel 63 Slot 13 Fiber 1 Asic 0 Channel 61



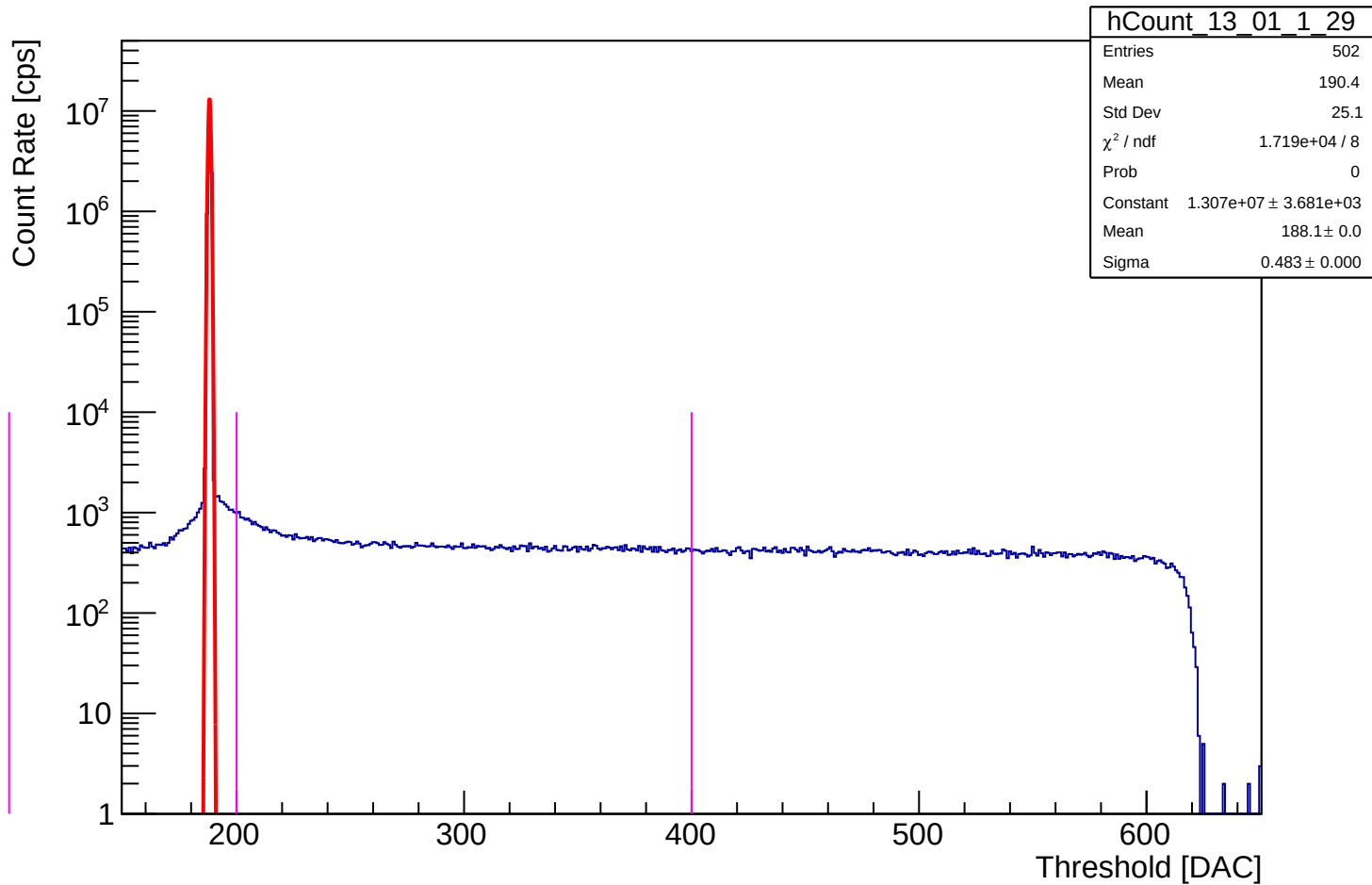
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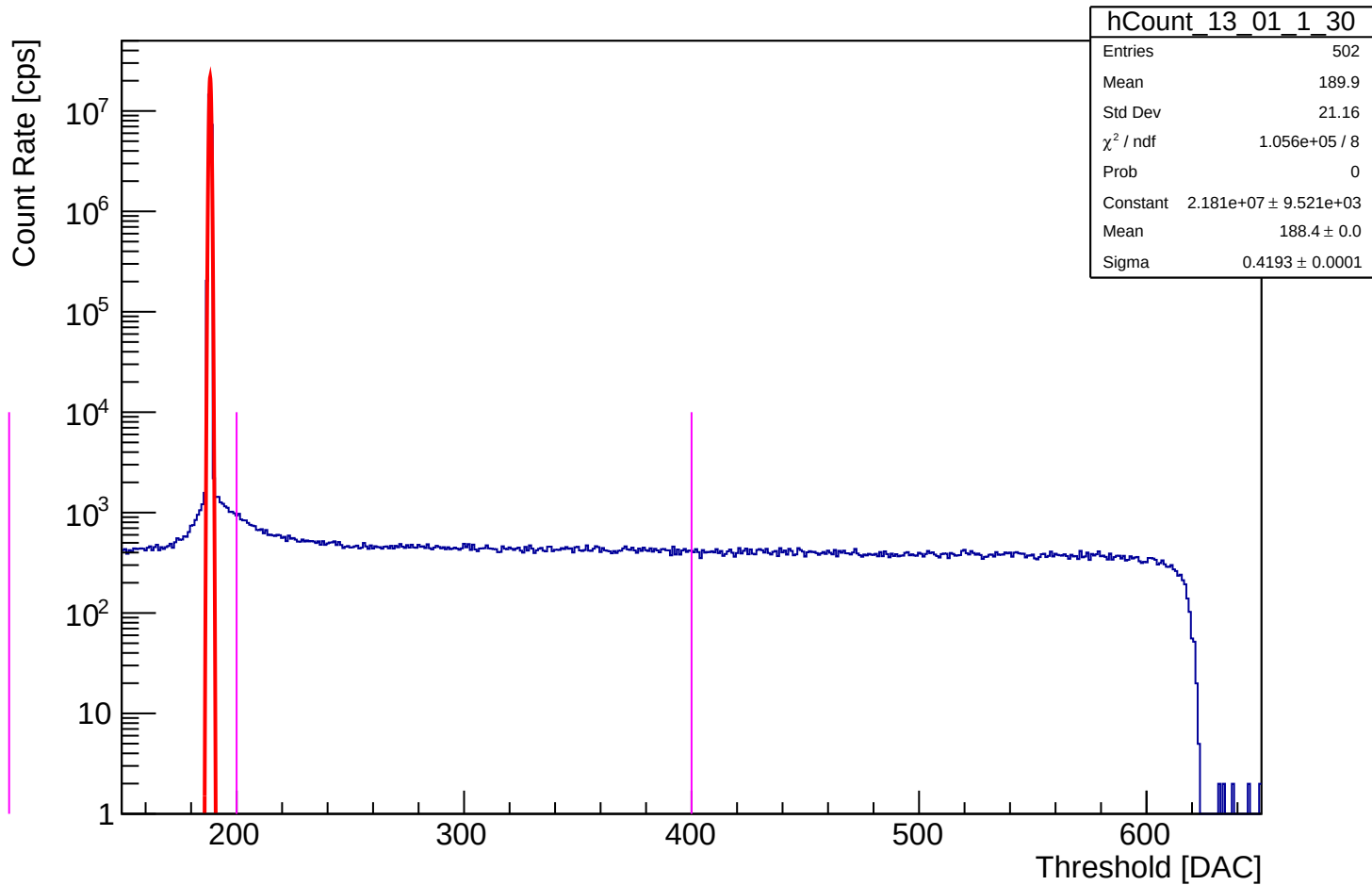
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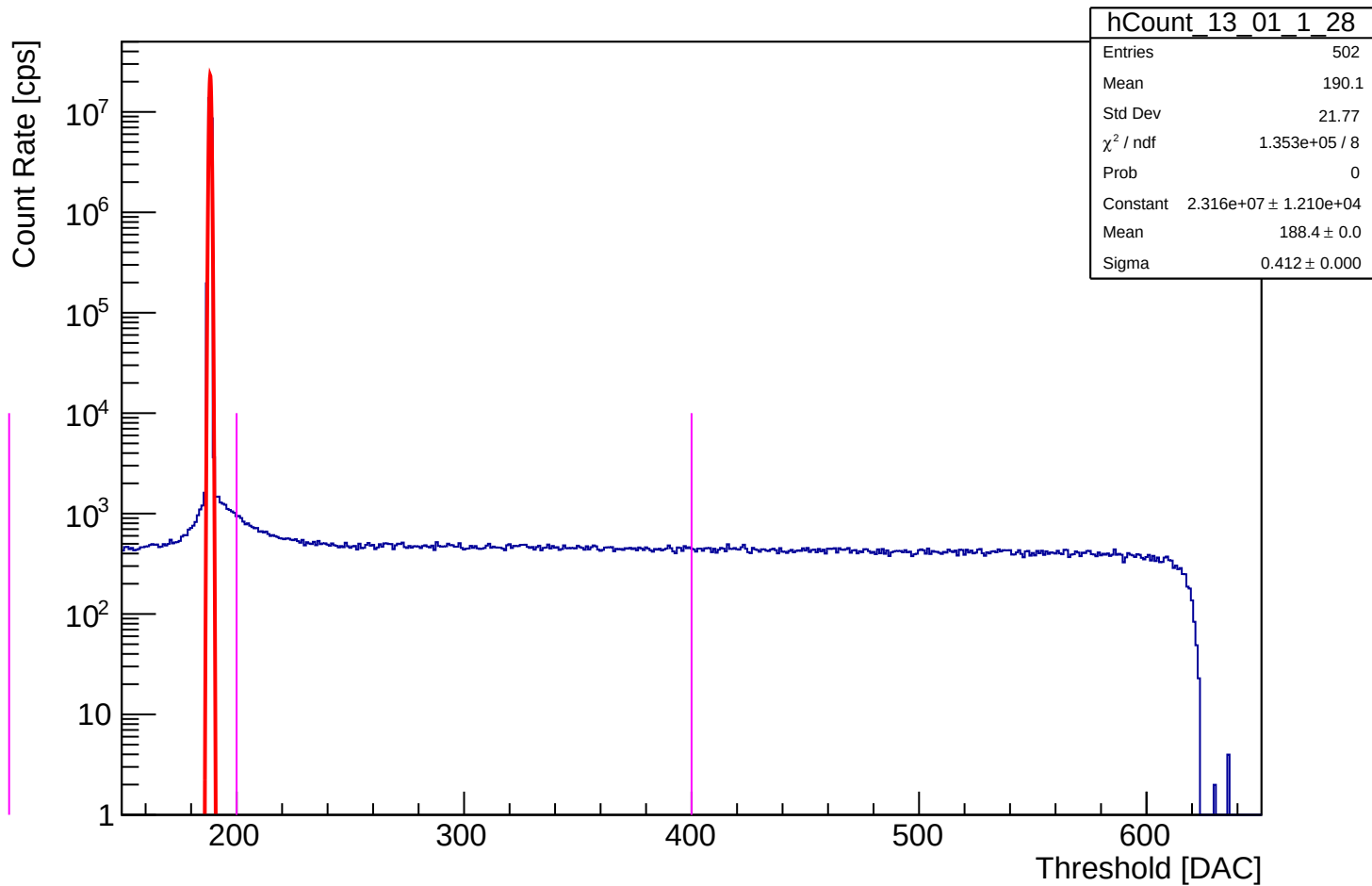
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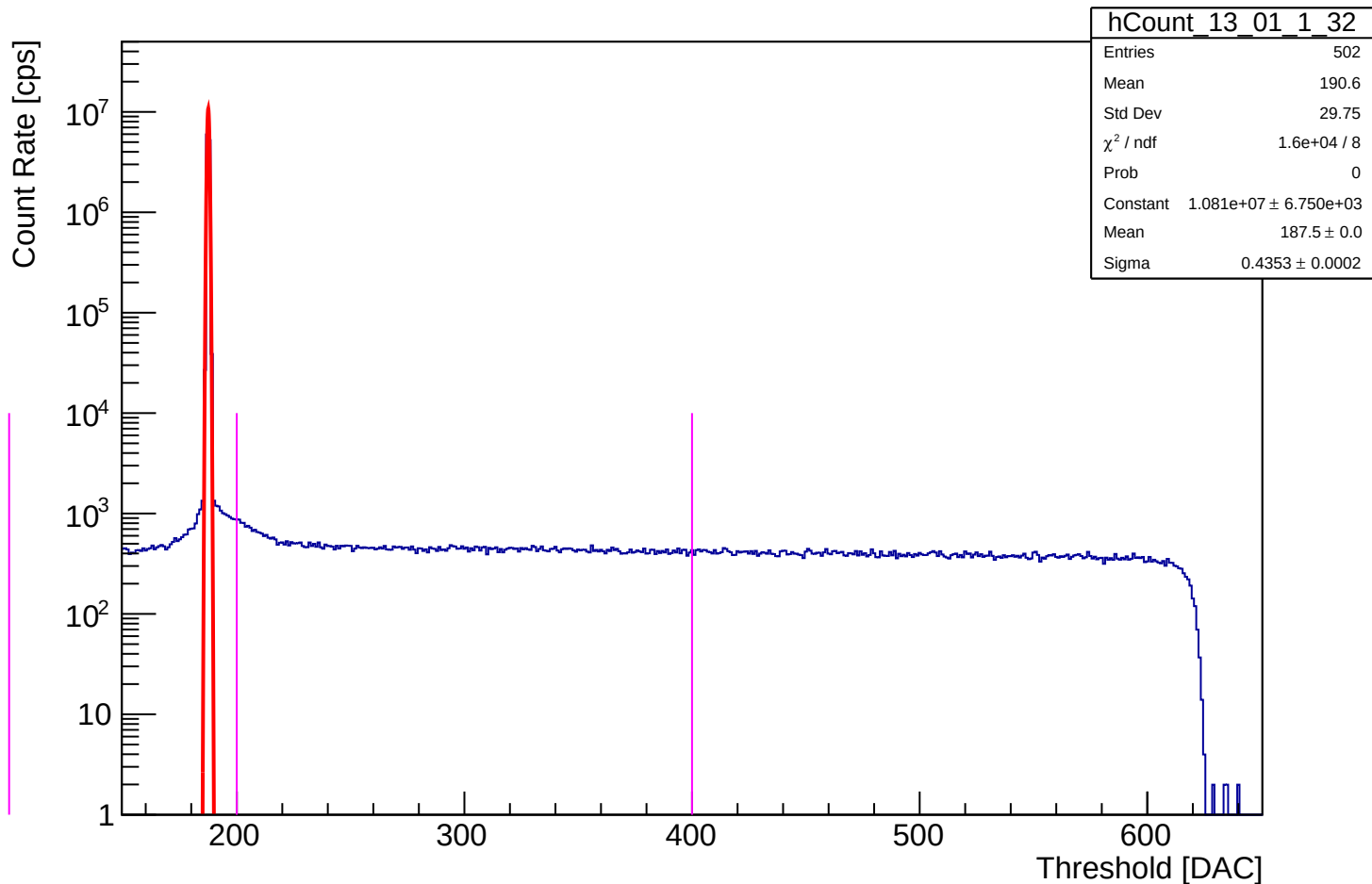
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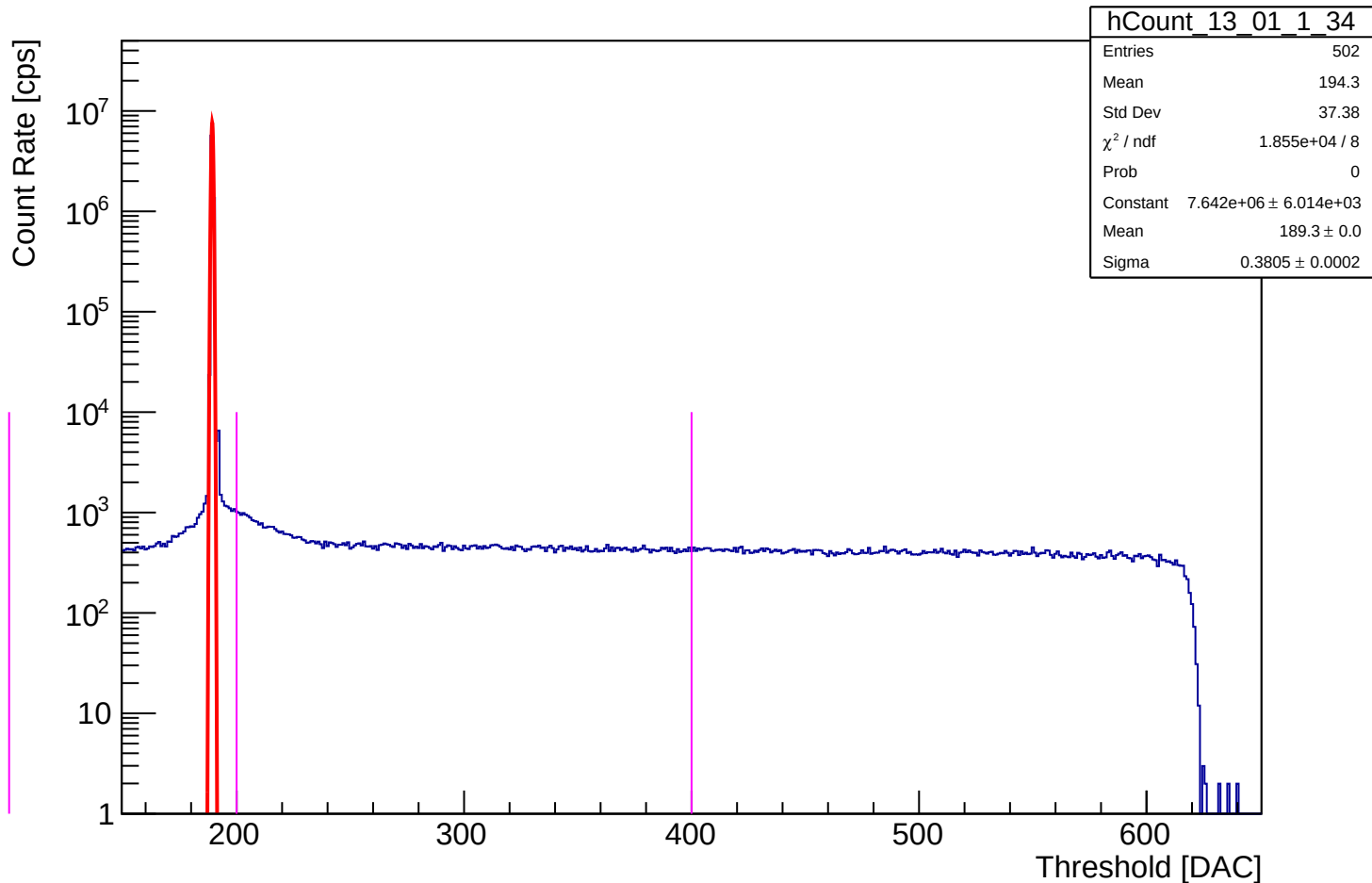
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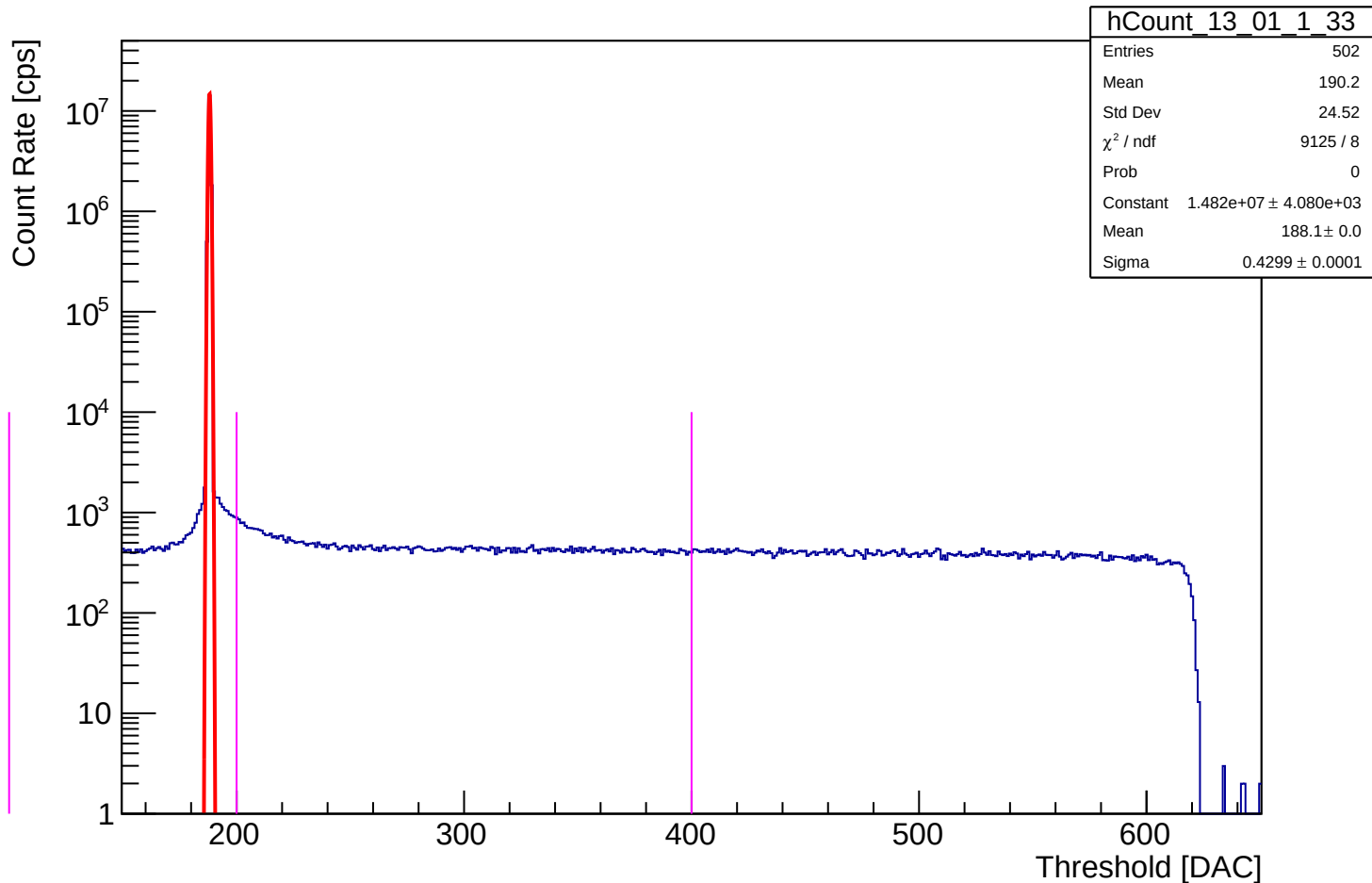
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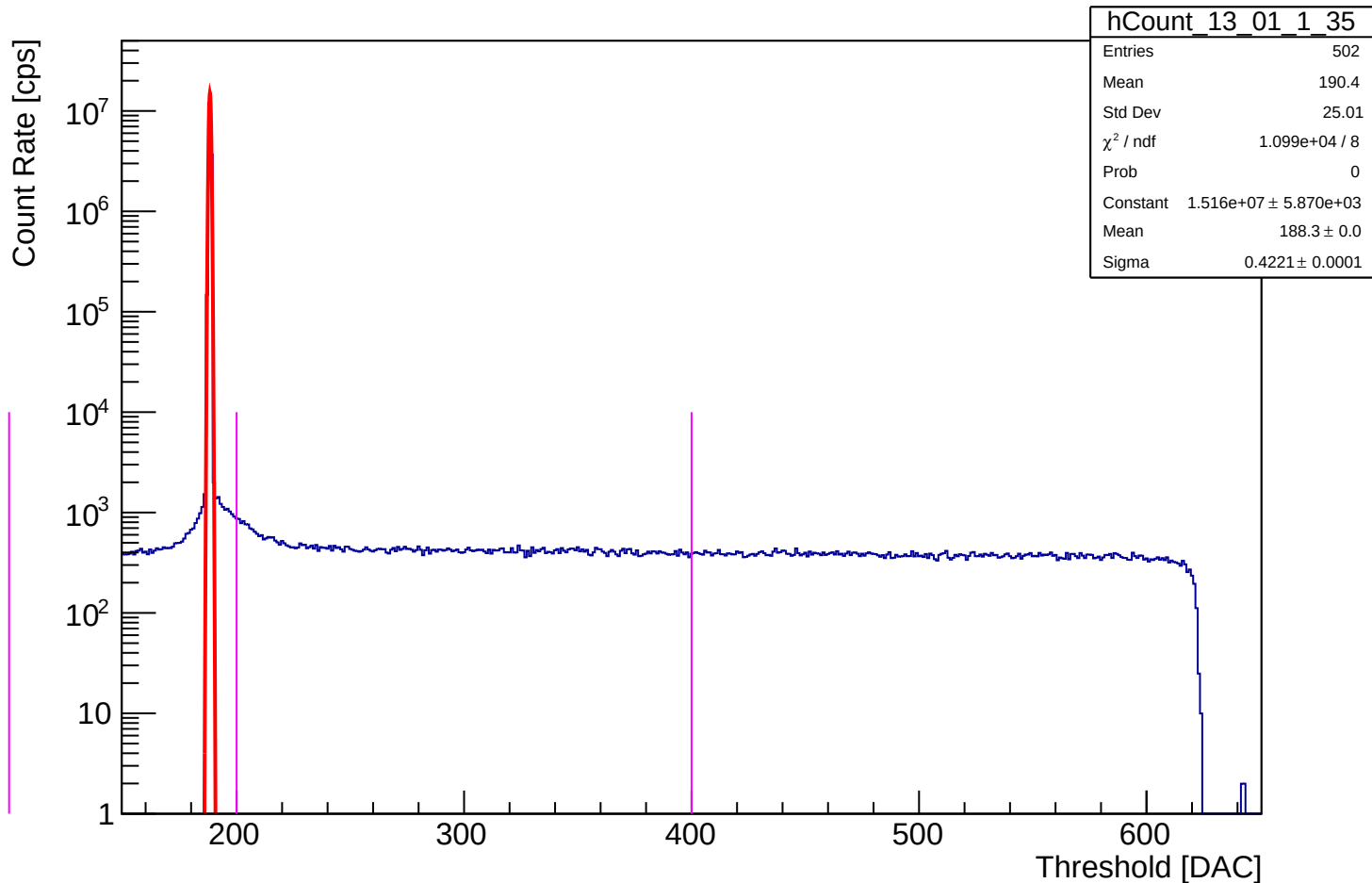
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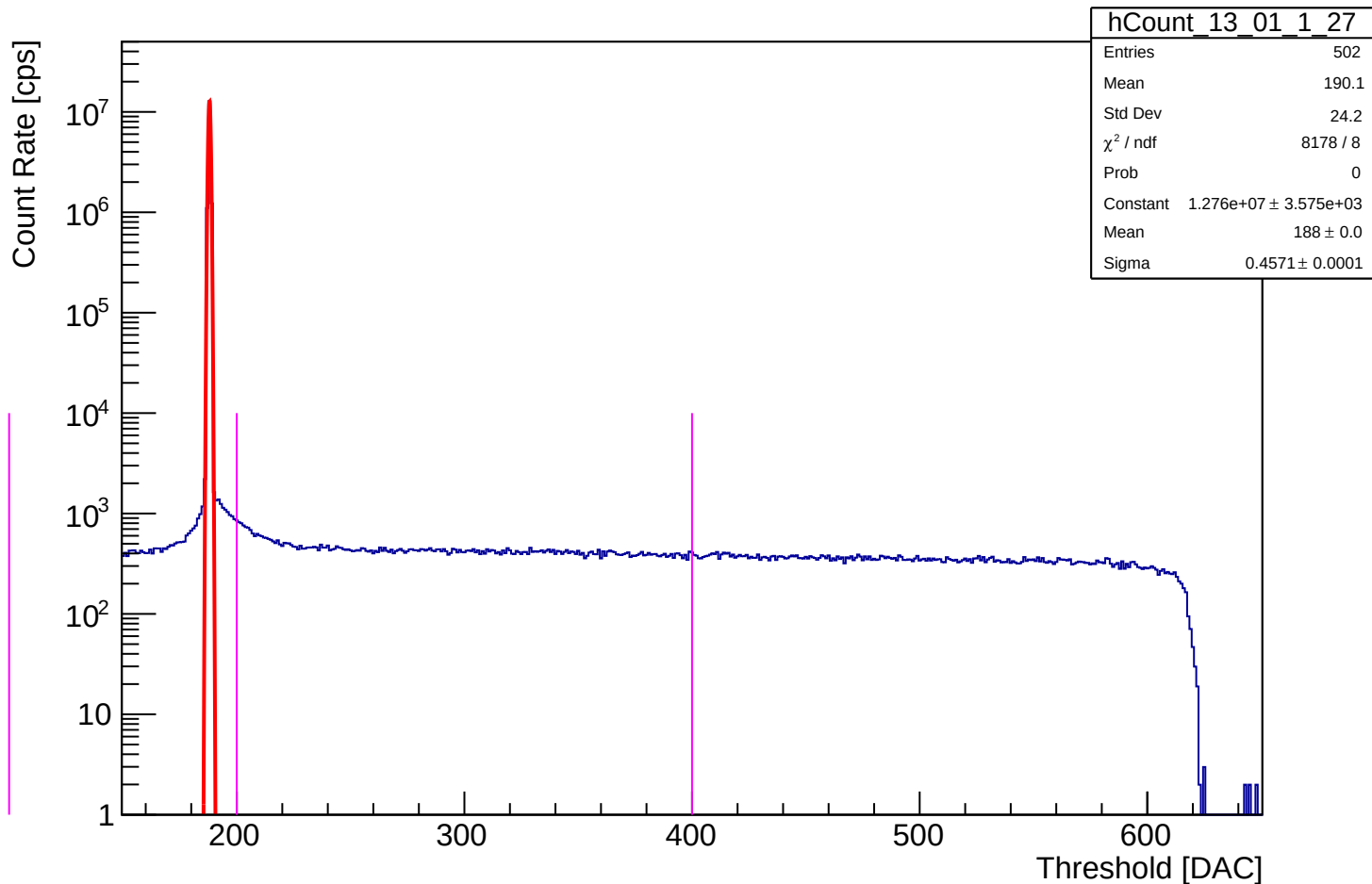
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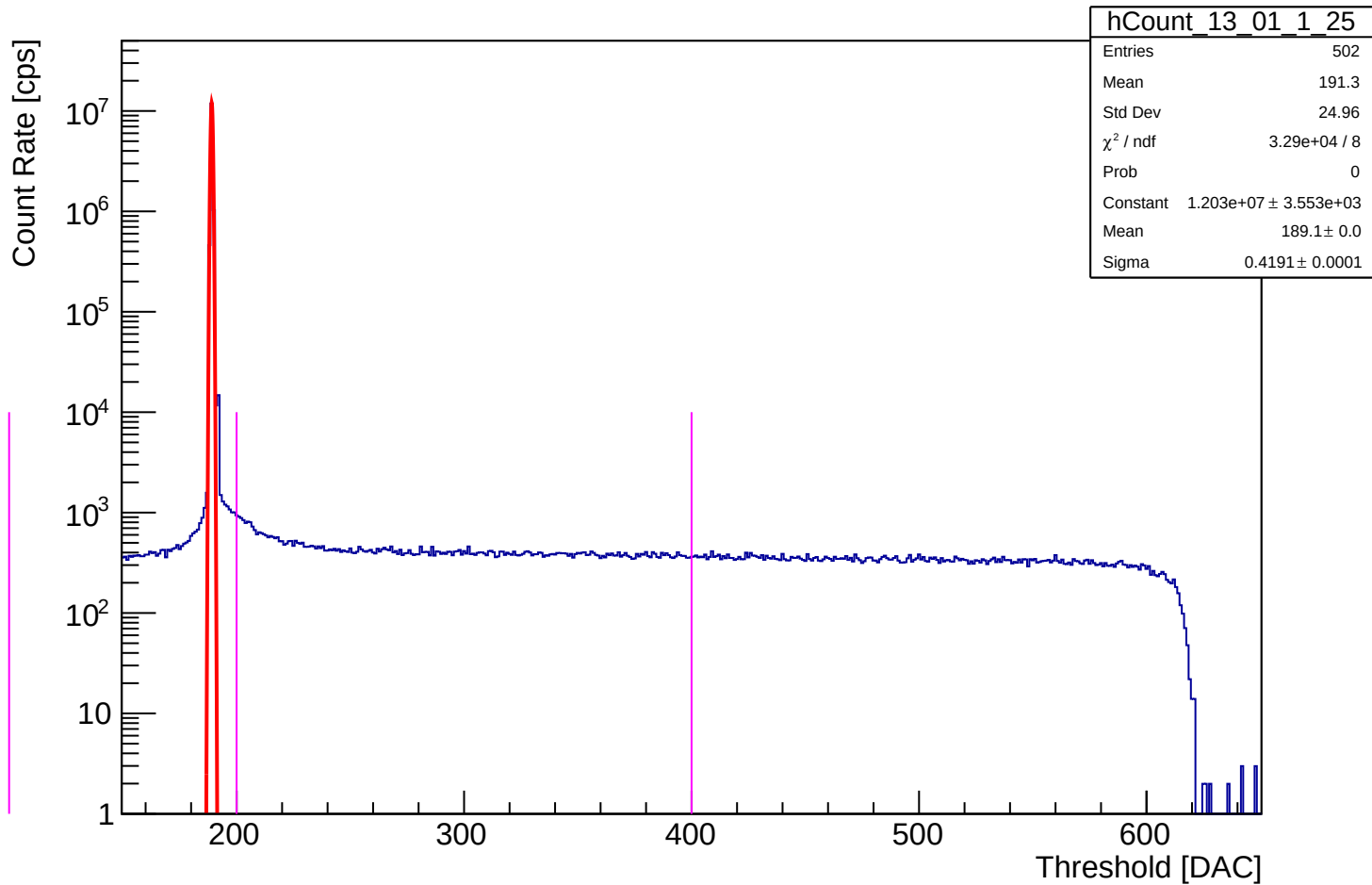
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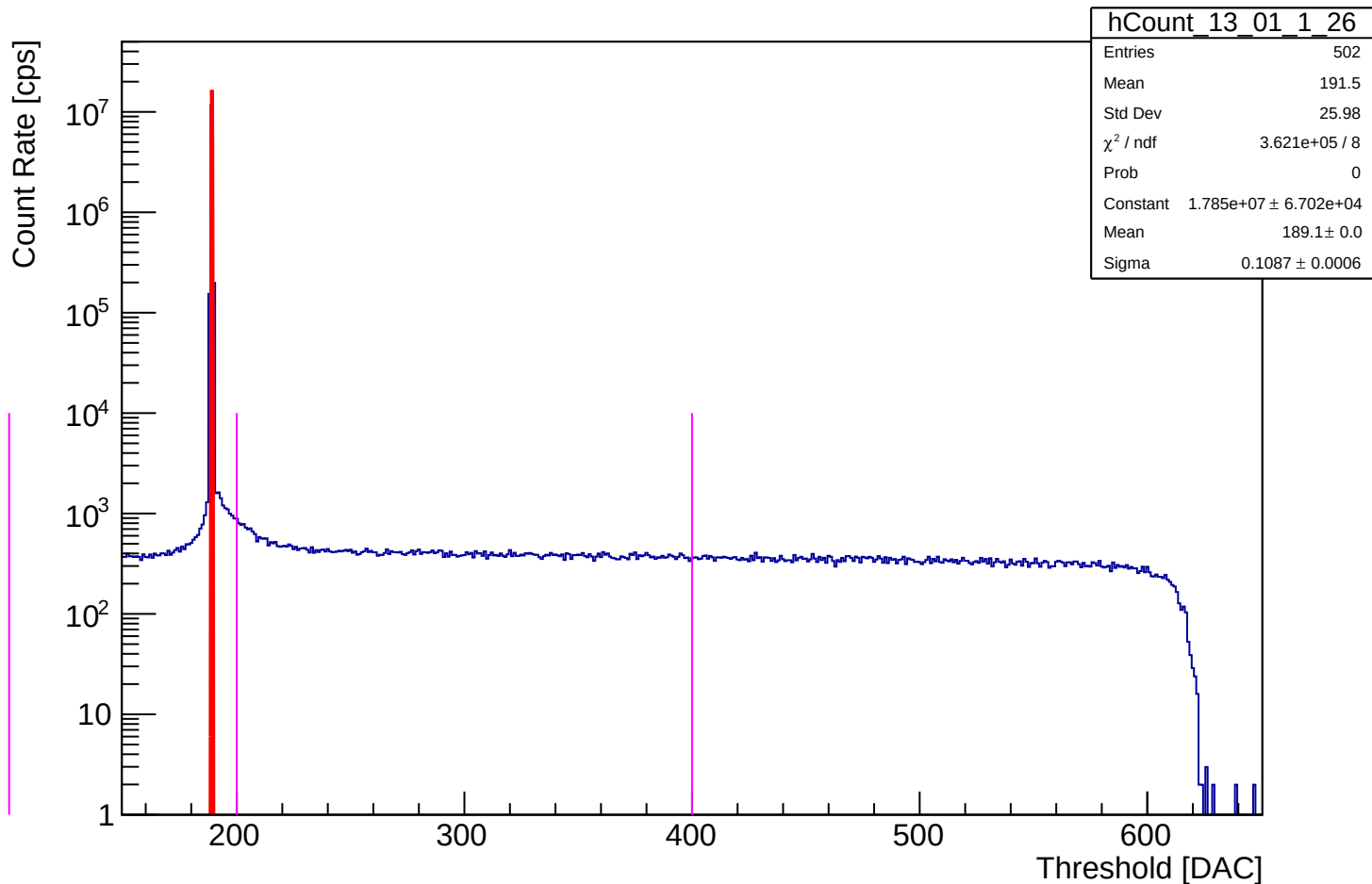
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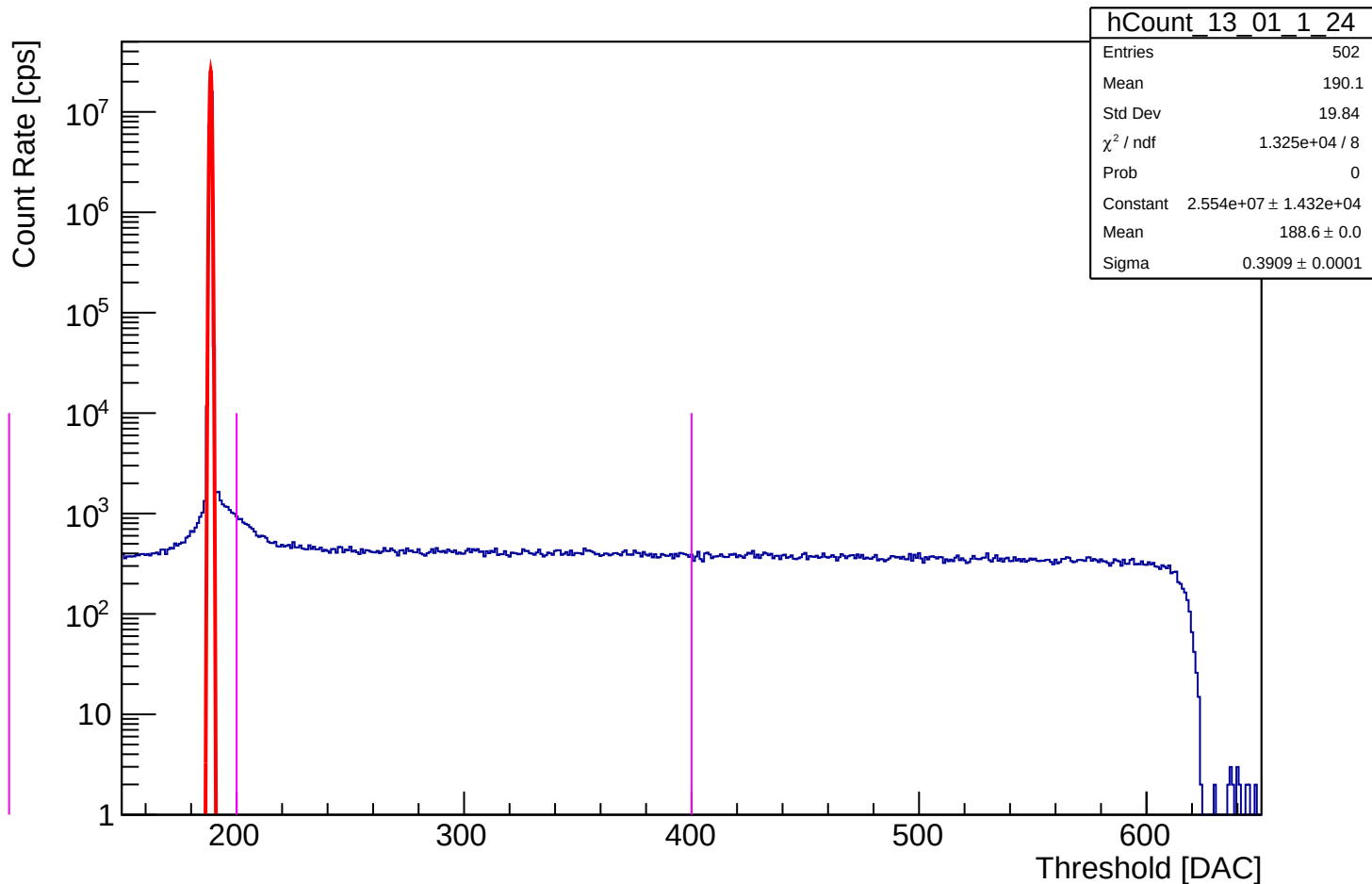
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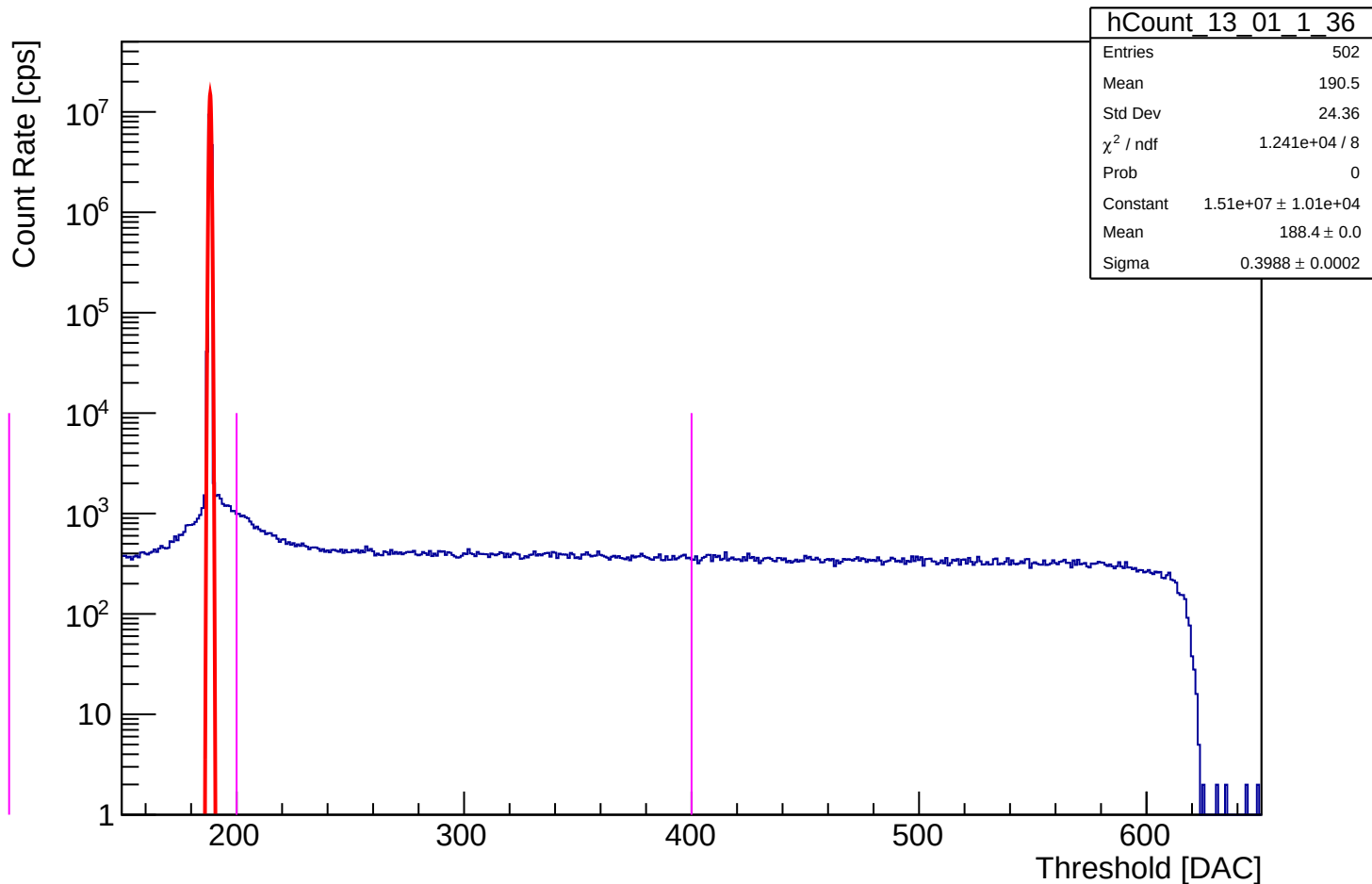
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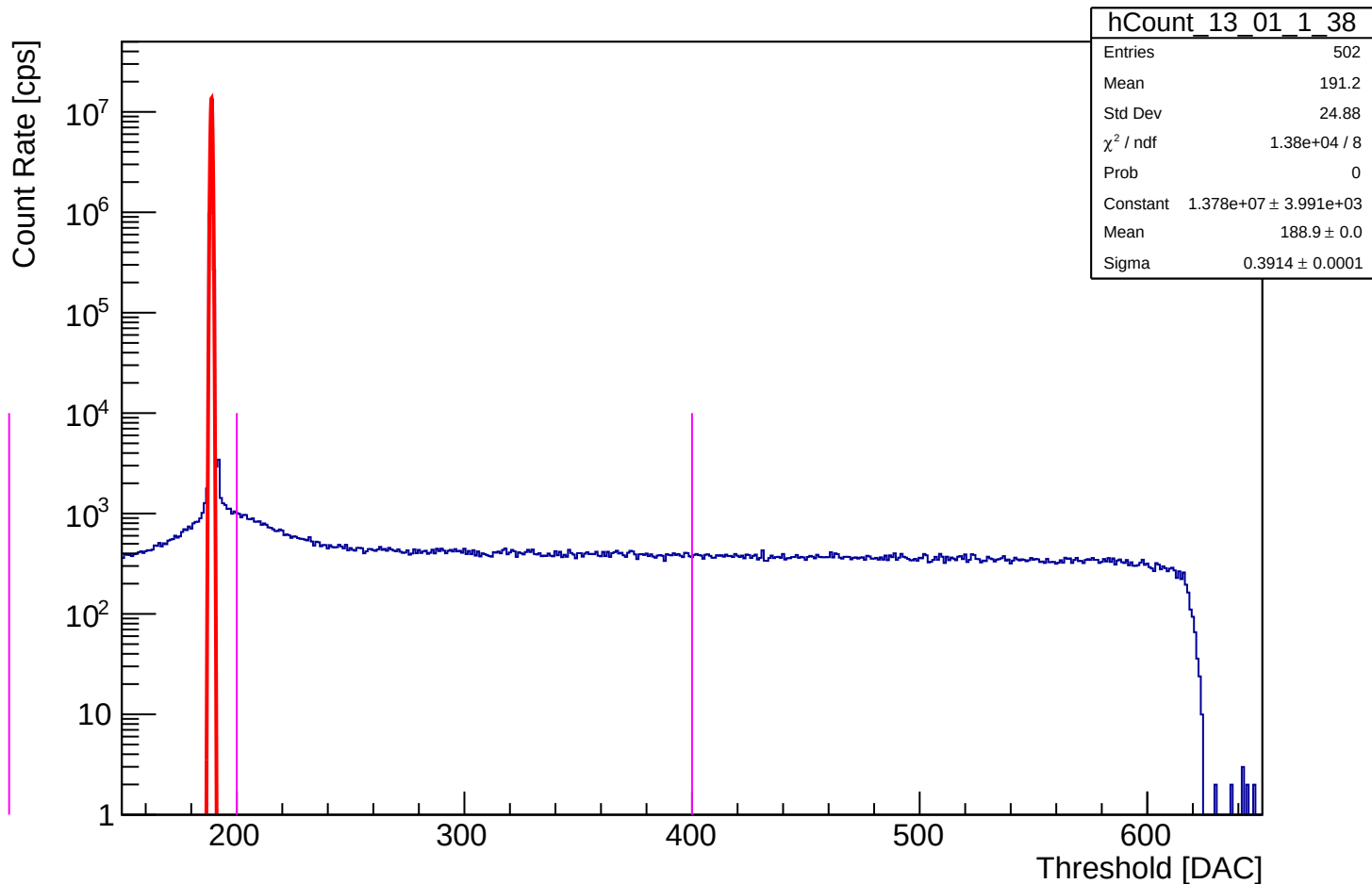
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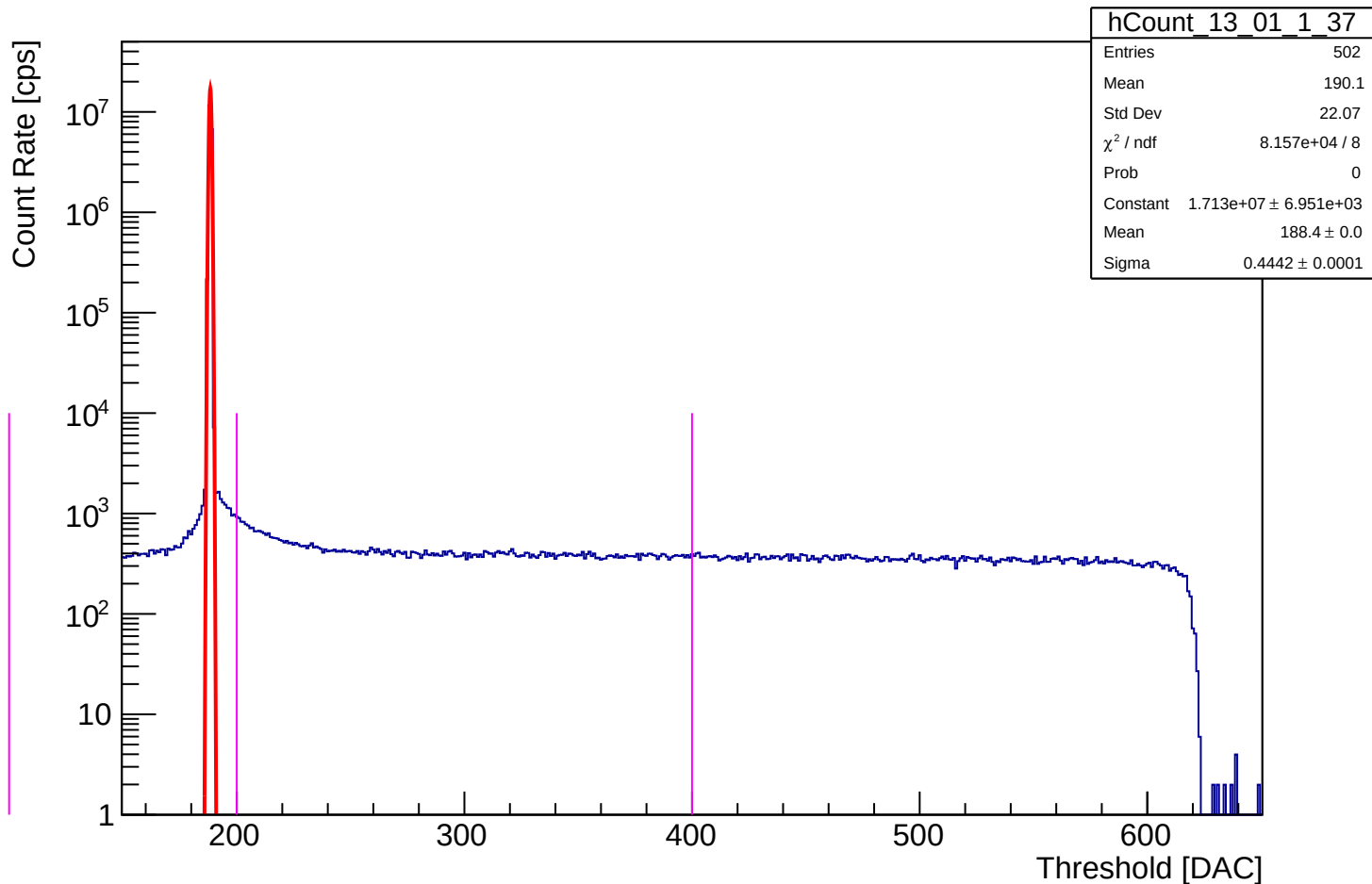
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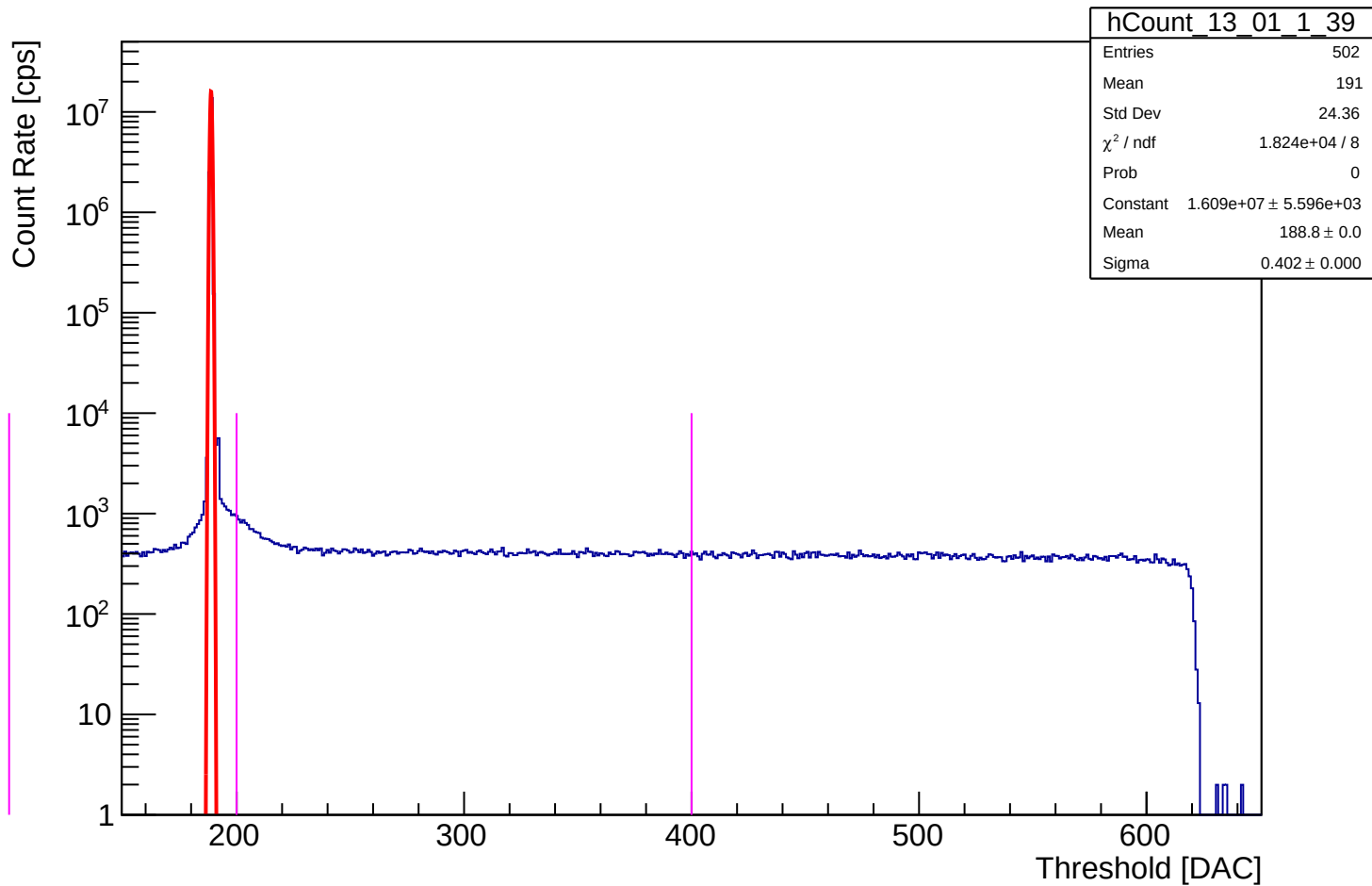
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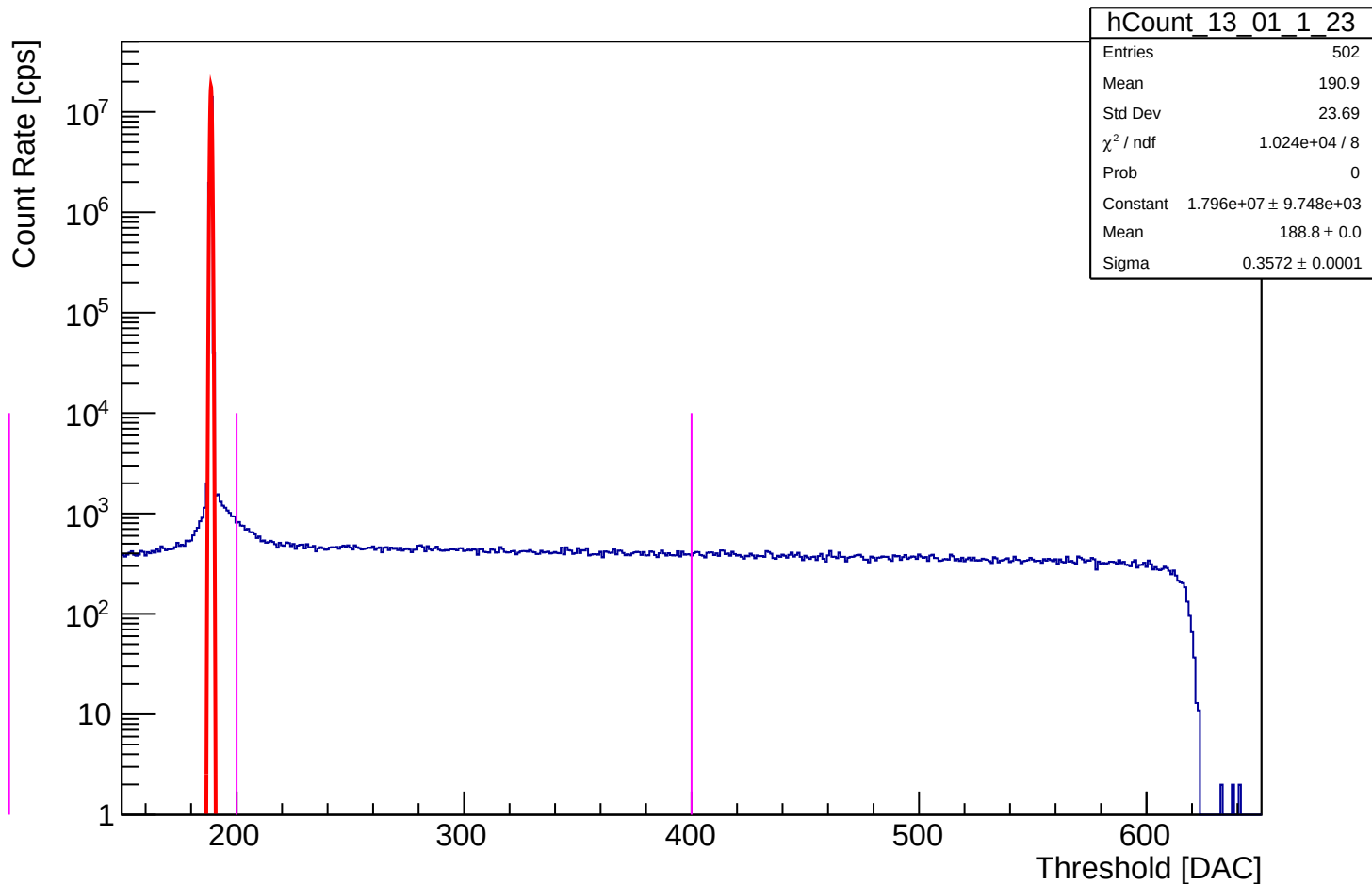
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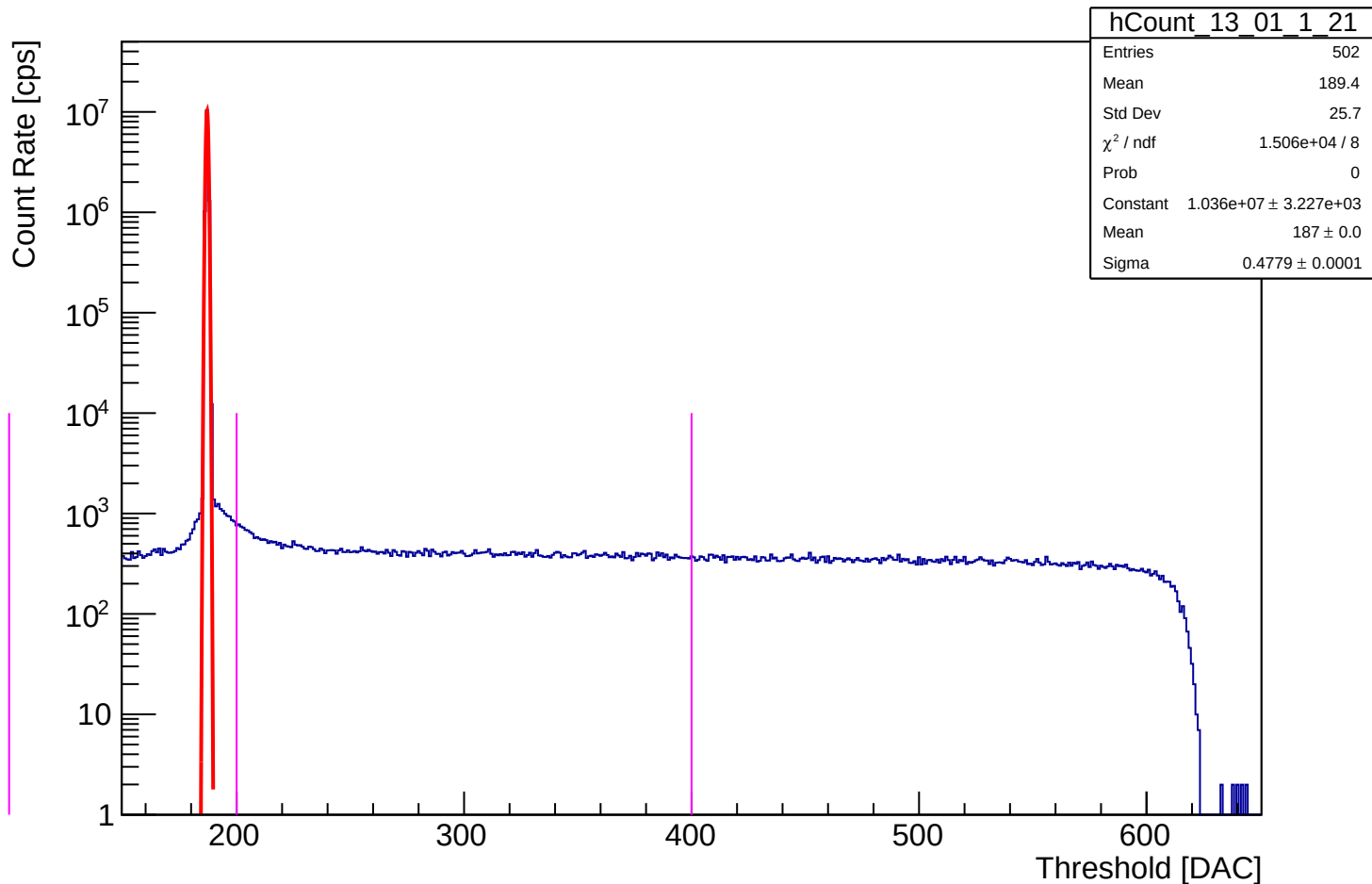
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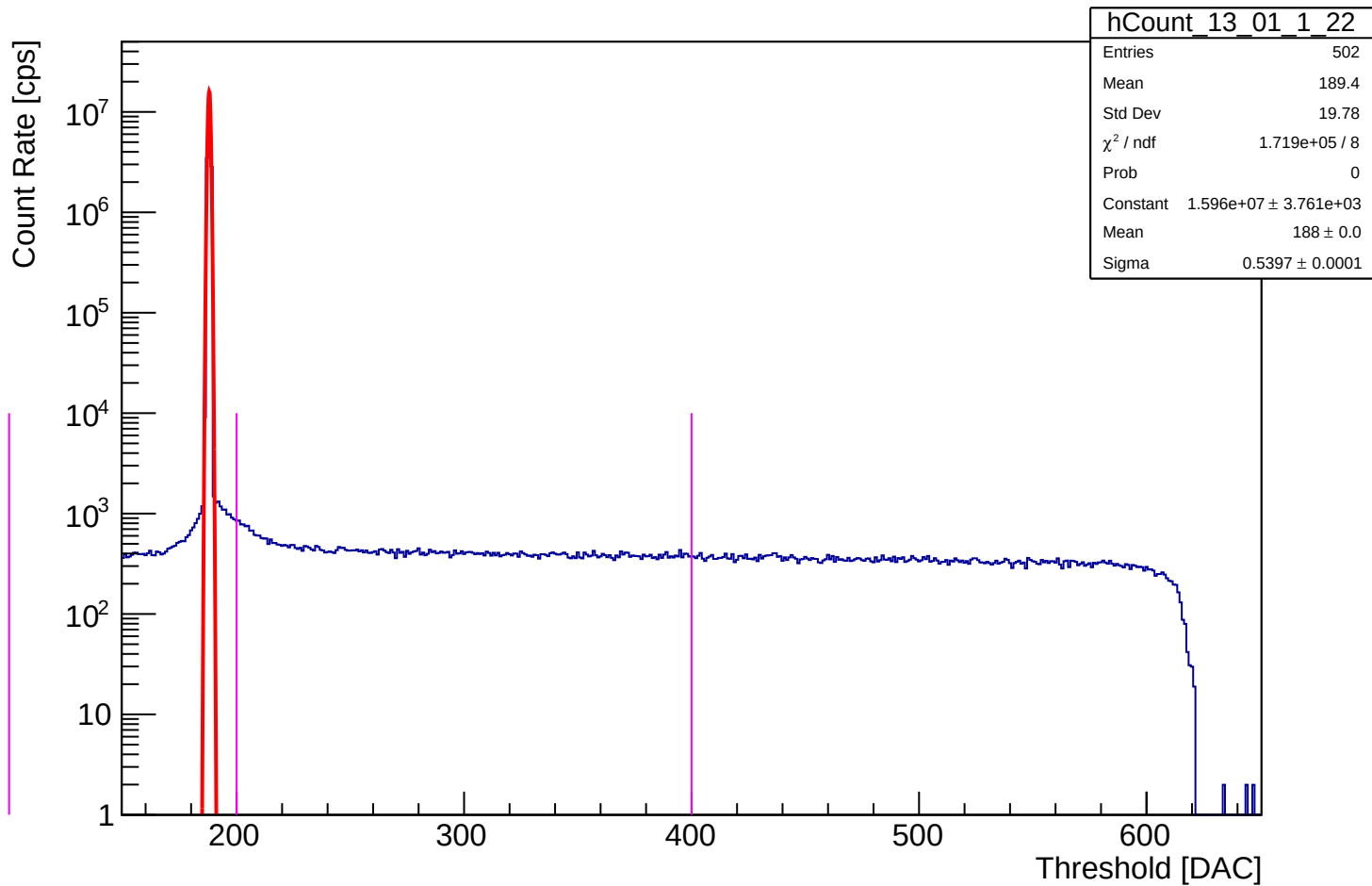
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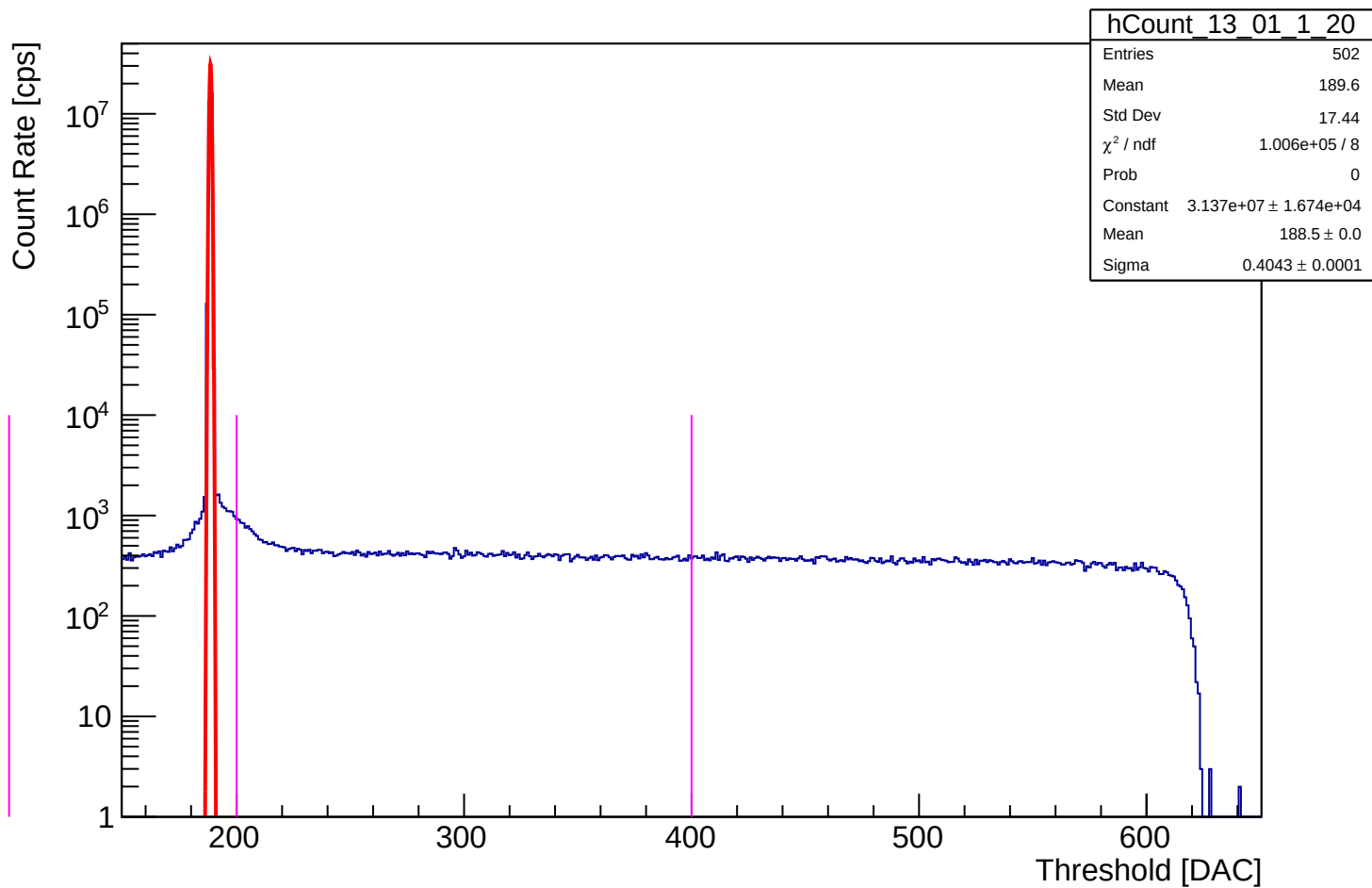
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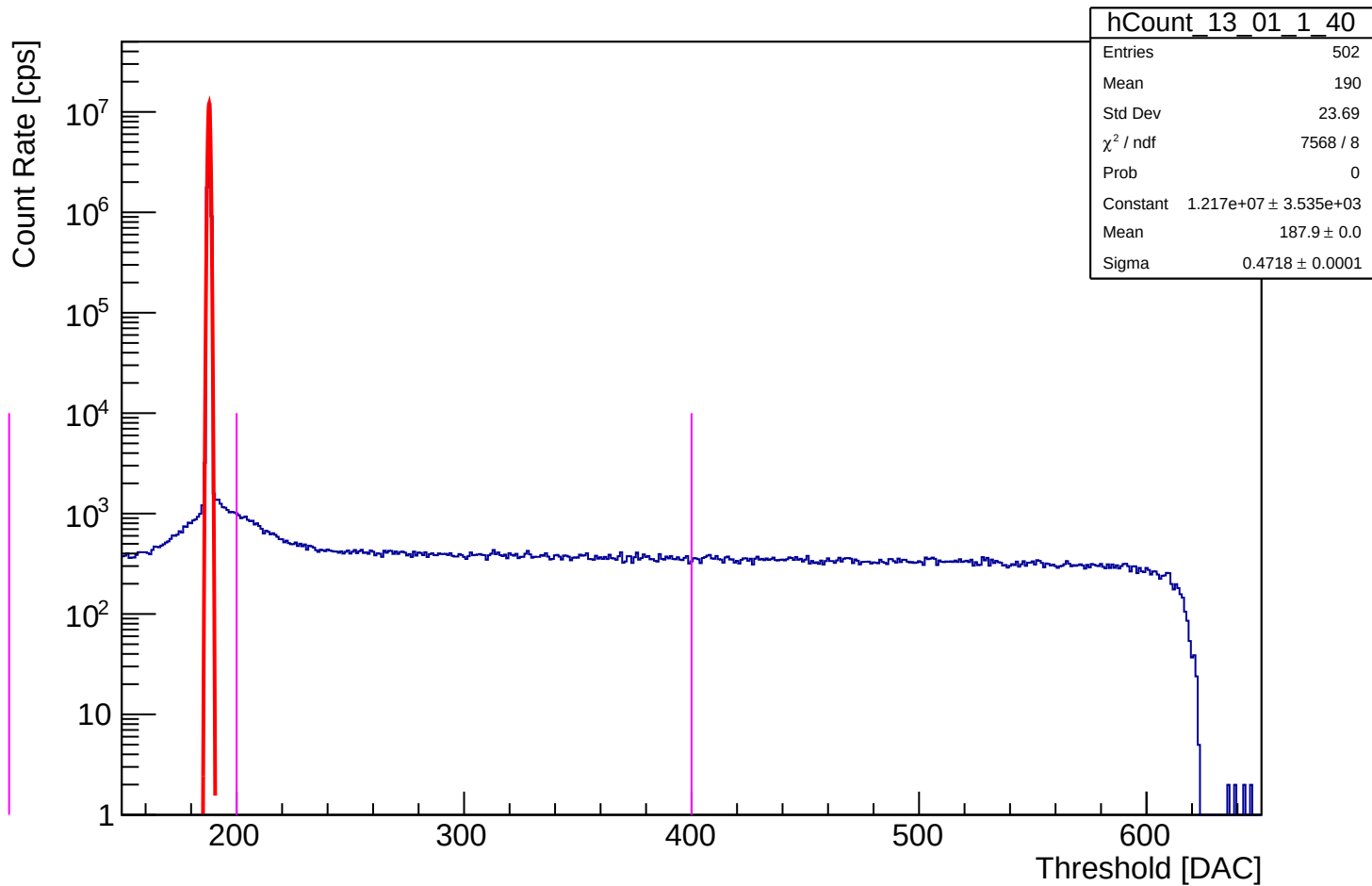
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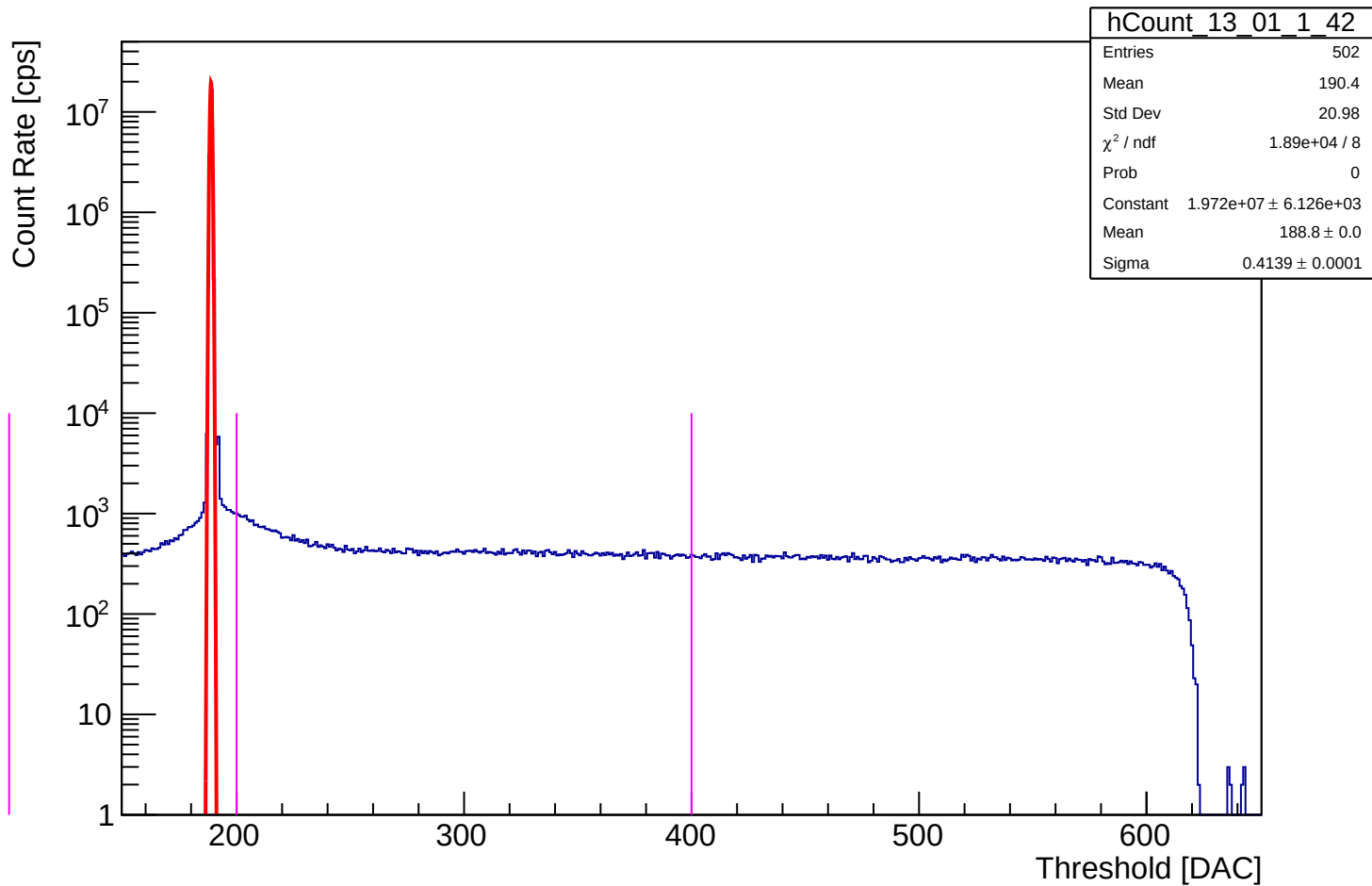
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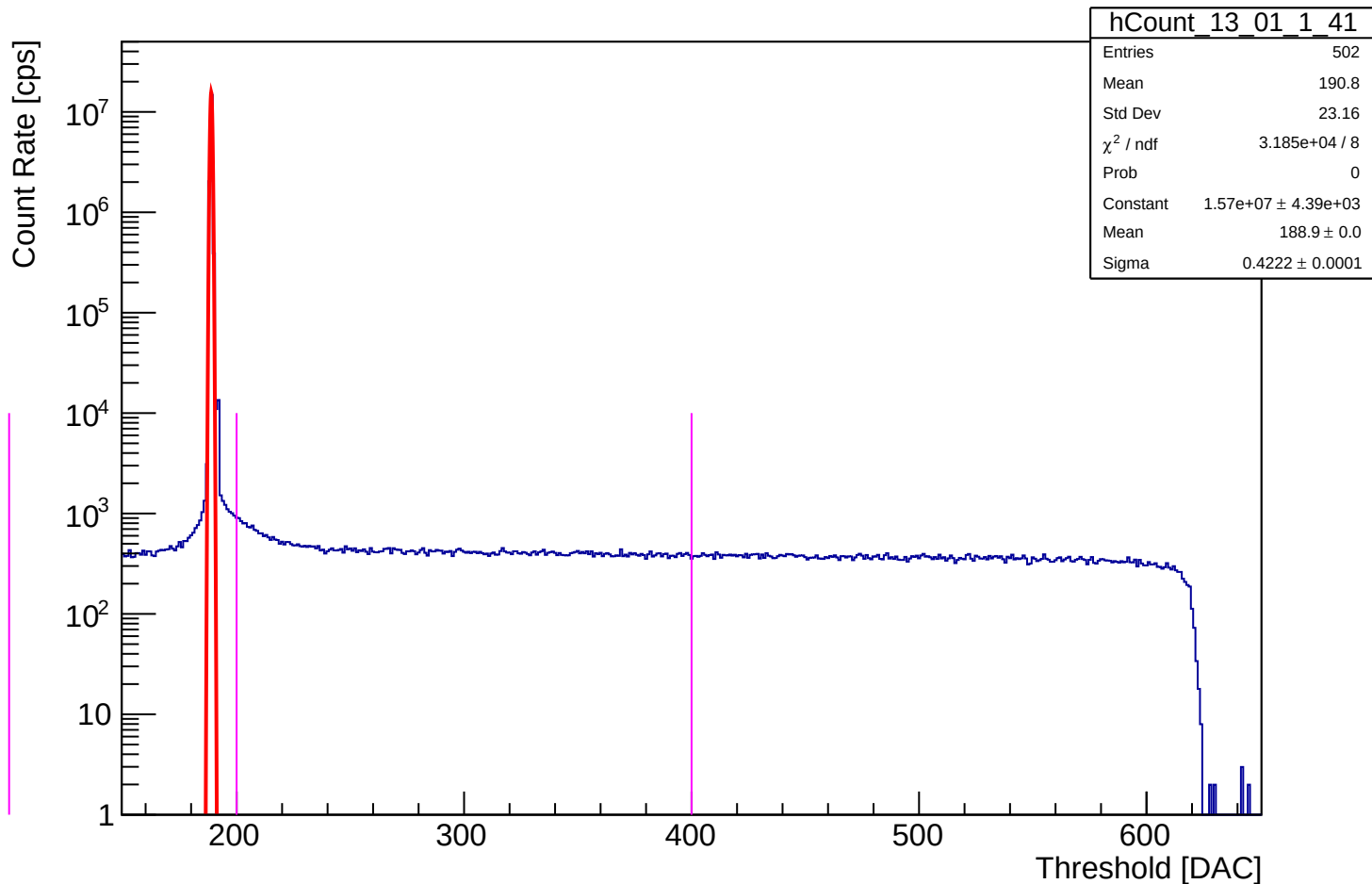
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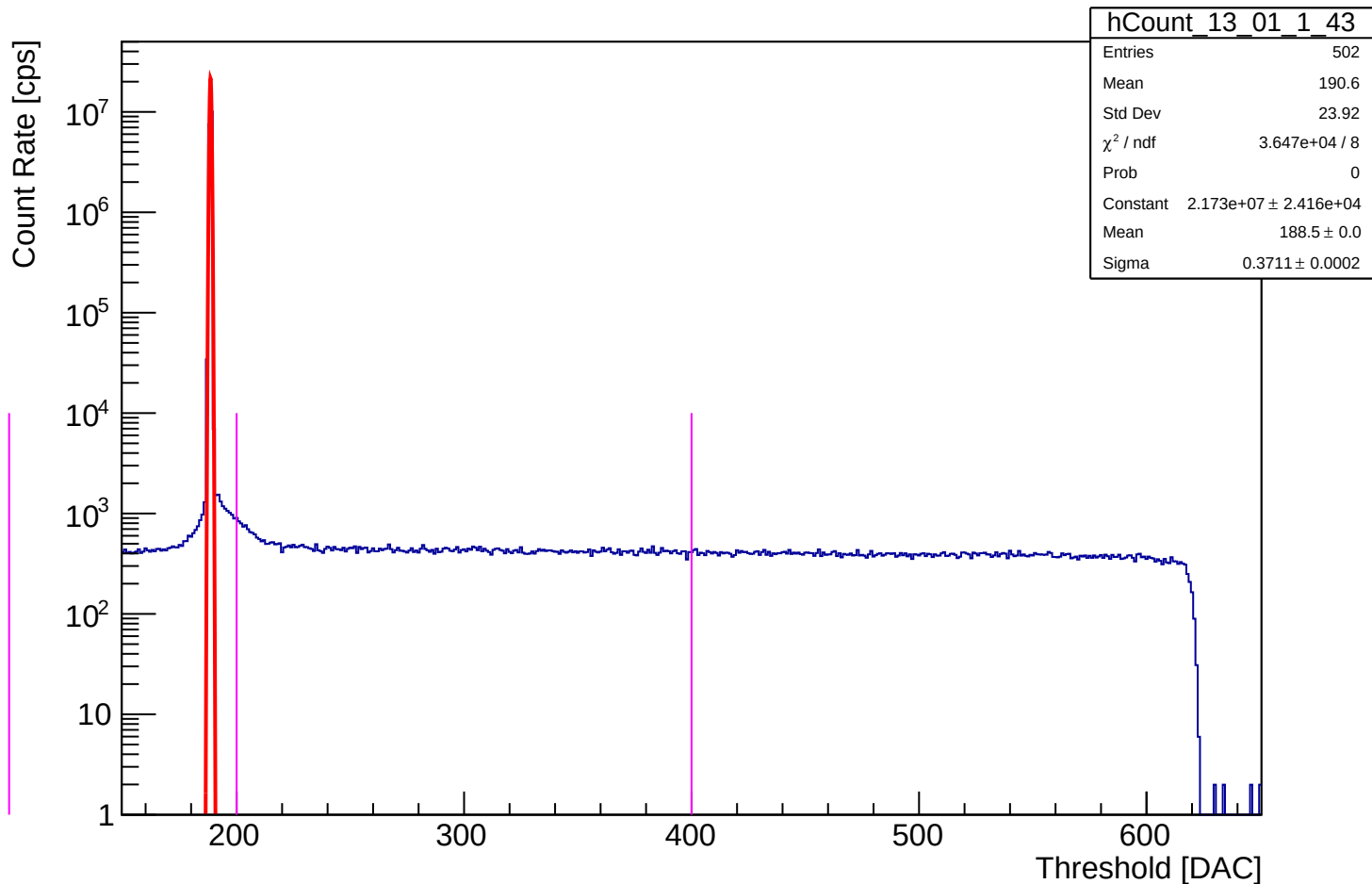
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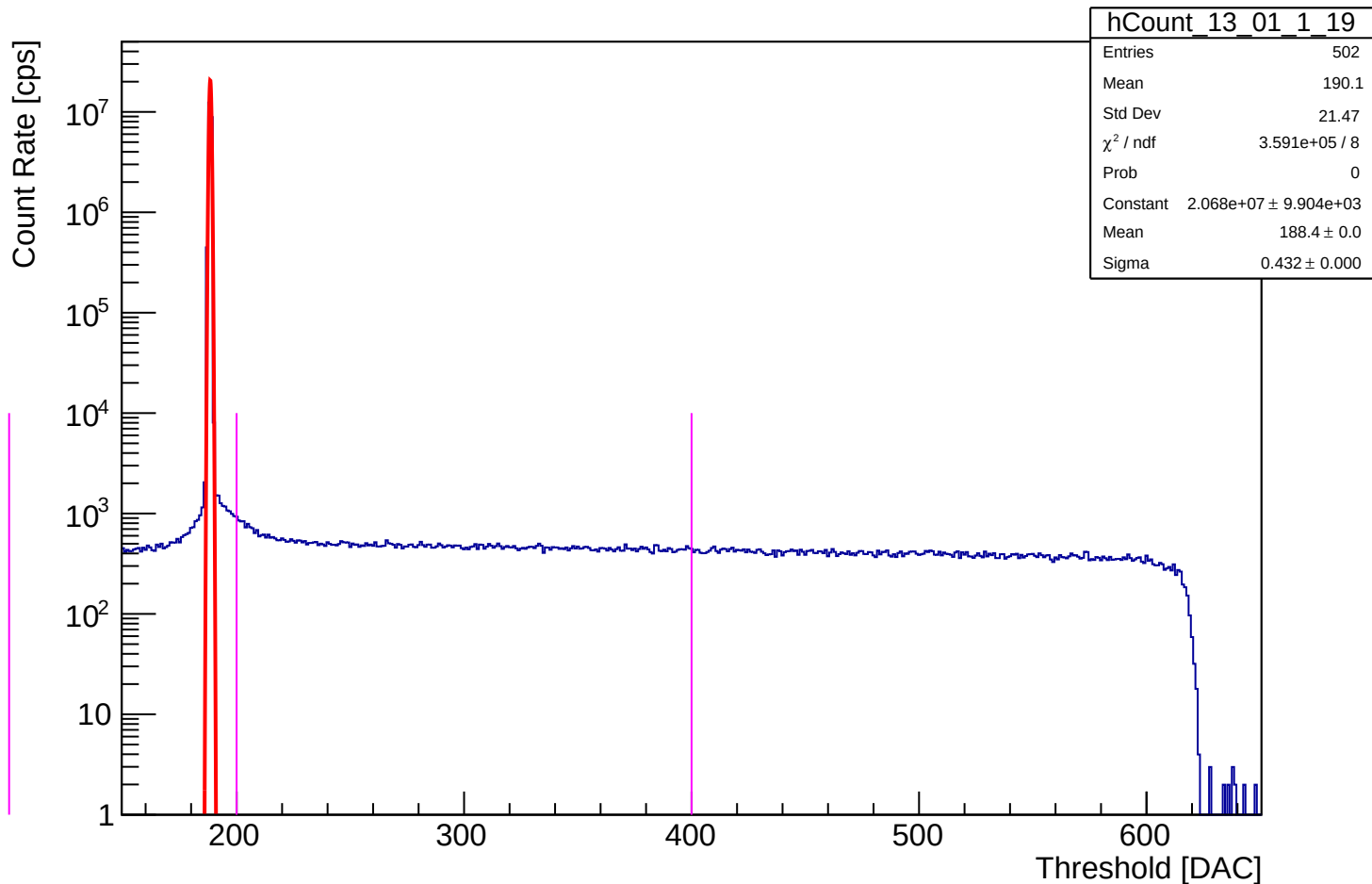
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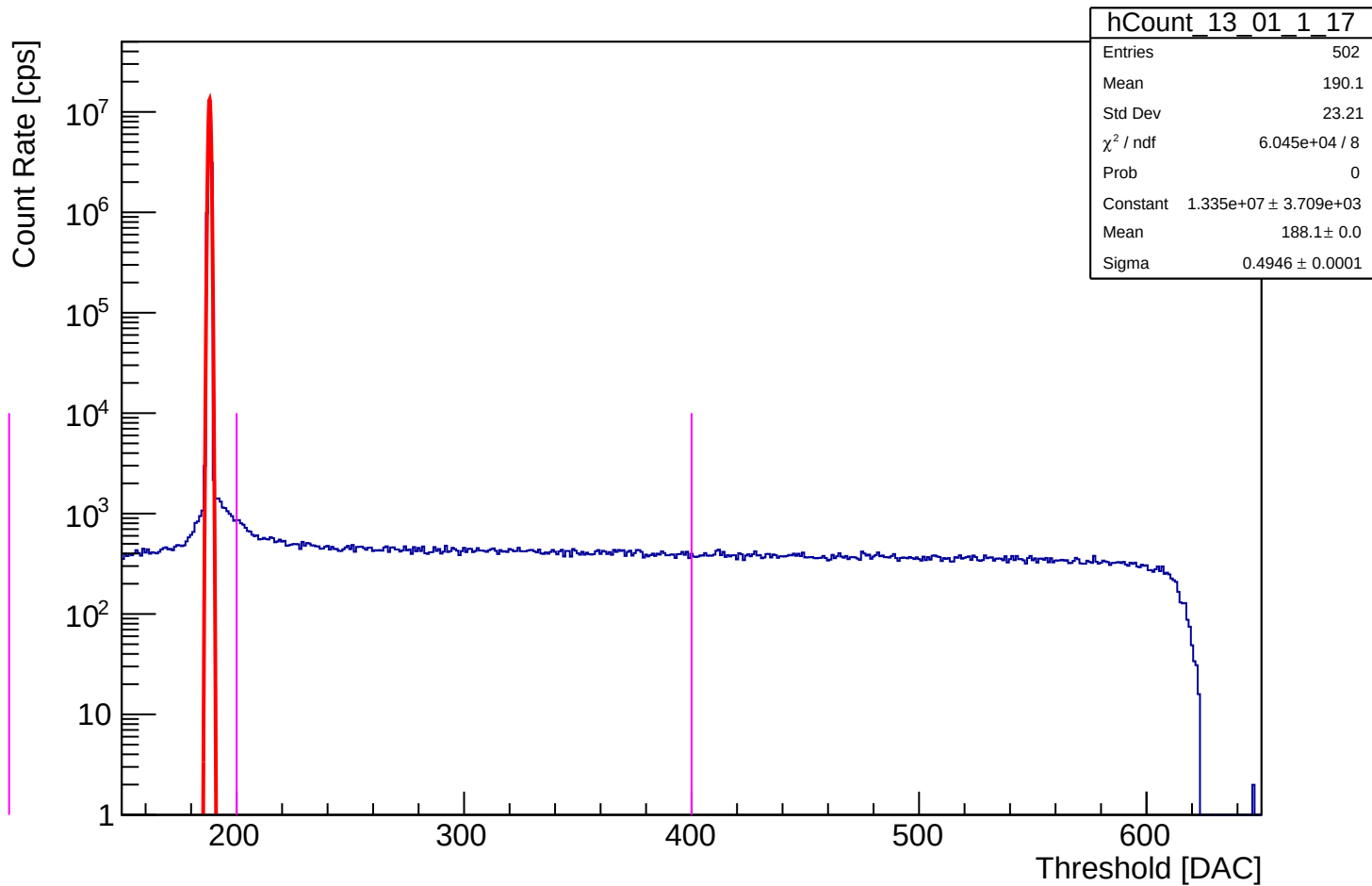
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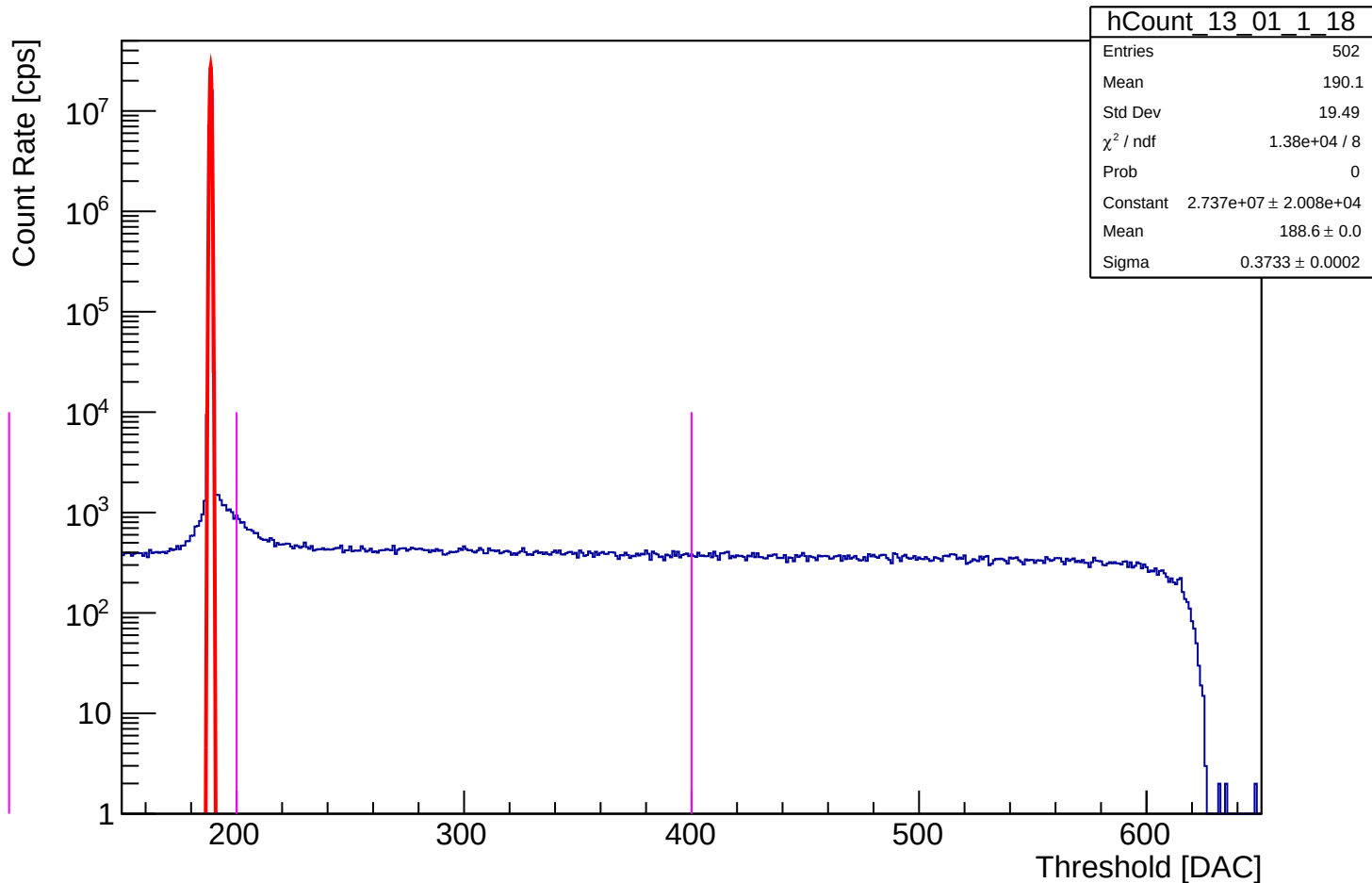
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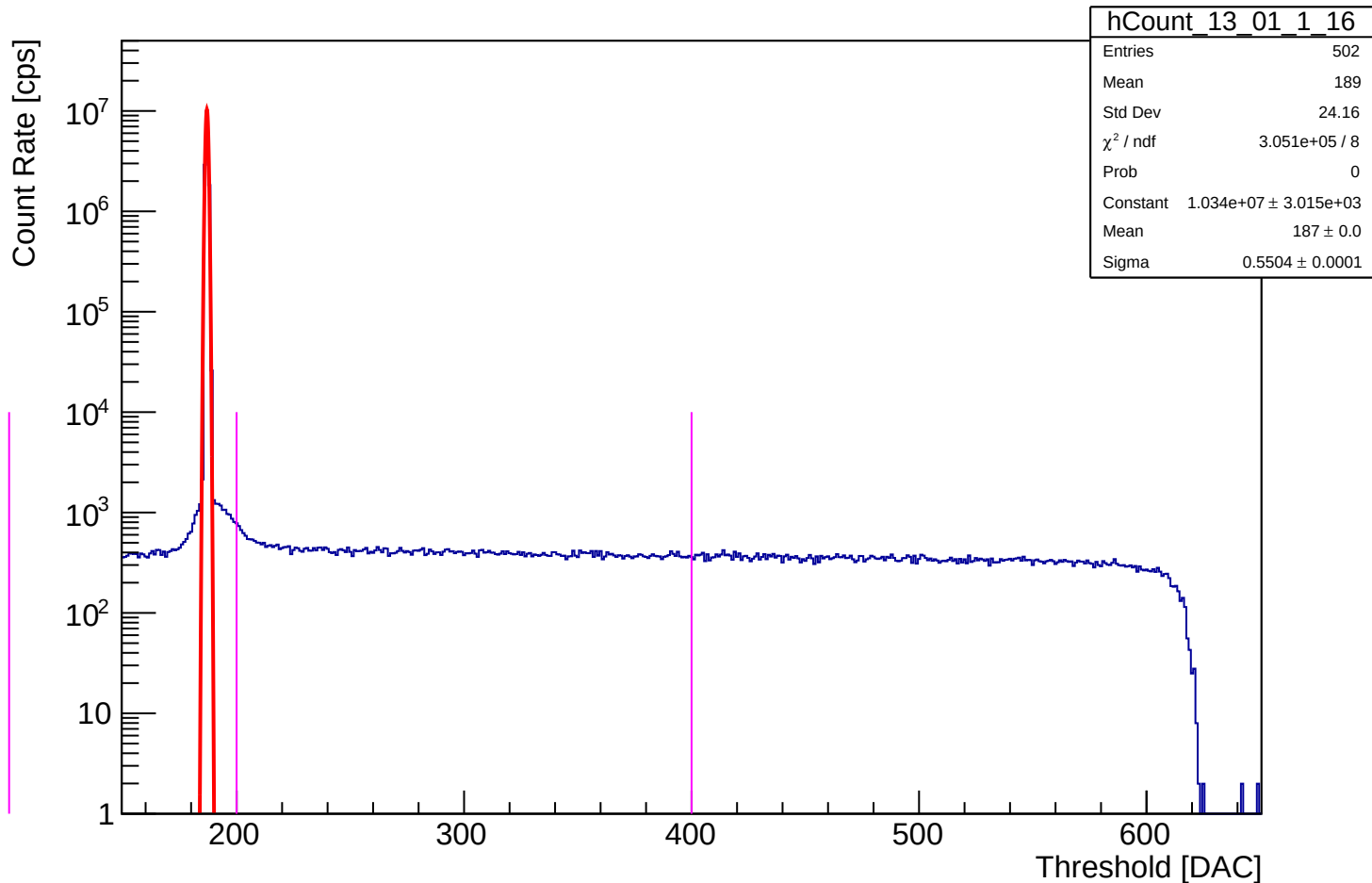
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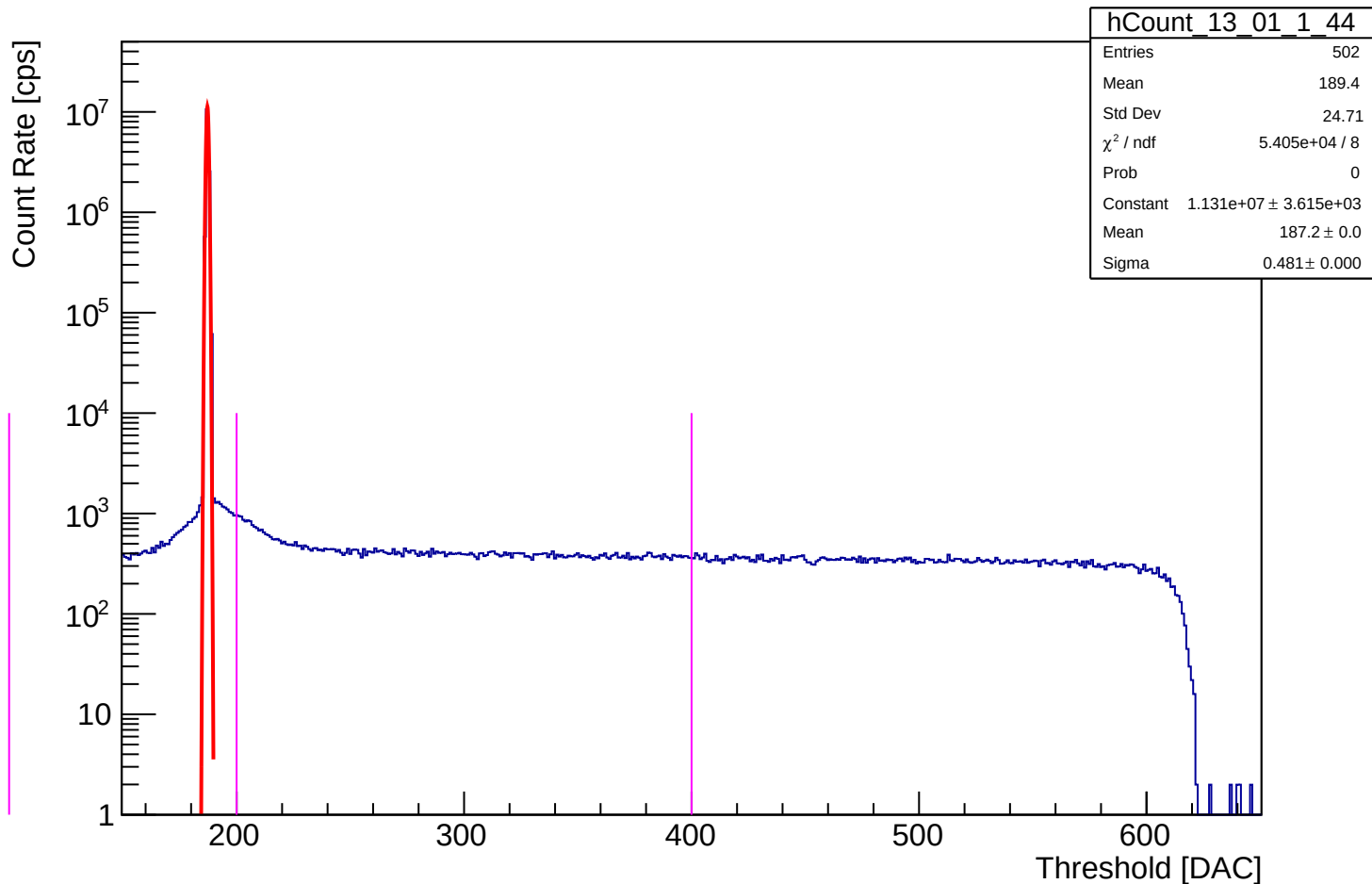


Row 1 Tile 1 Pmt 5 Pixel 27 Slot 13 Fiber 1 Asic 1 Channel 18

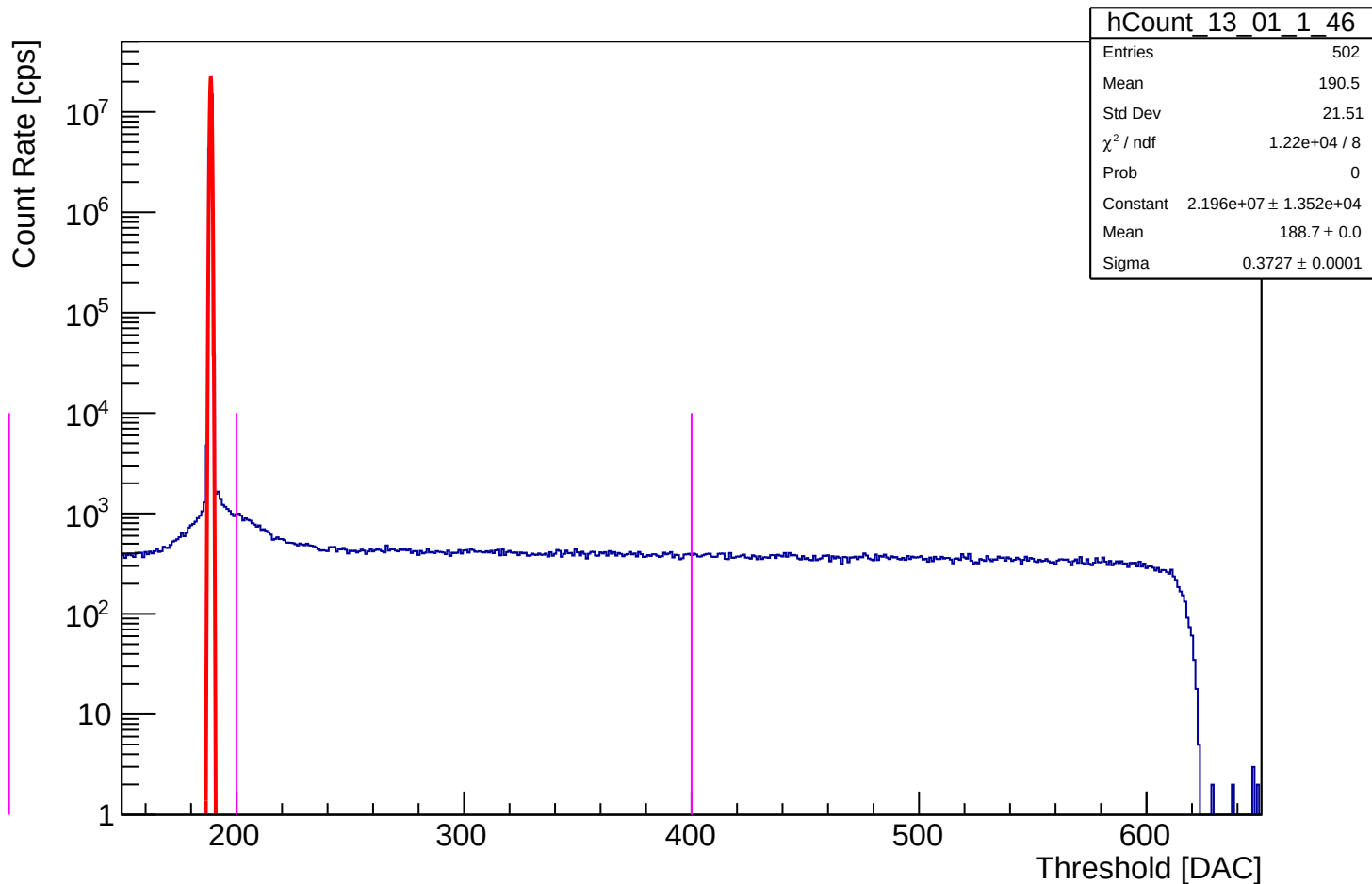


Row 1 Tile 1 Pmt 5 Pixel 28 Slot 13 Fiber 1 Asic 1 Channel 16

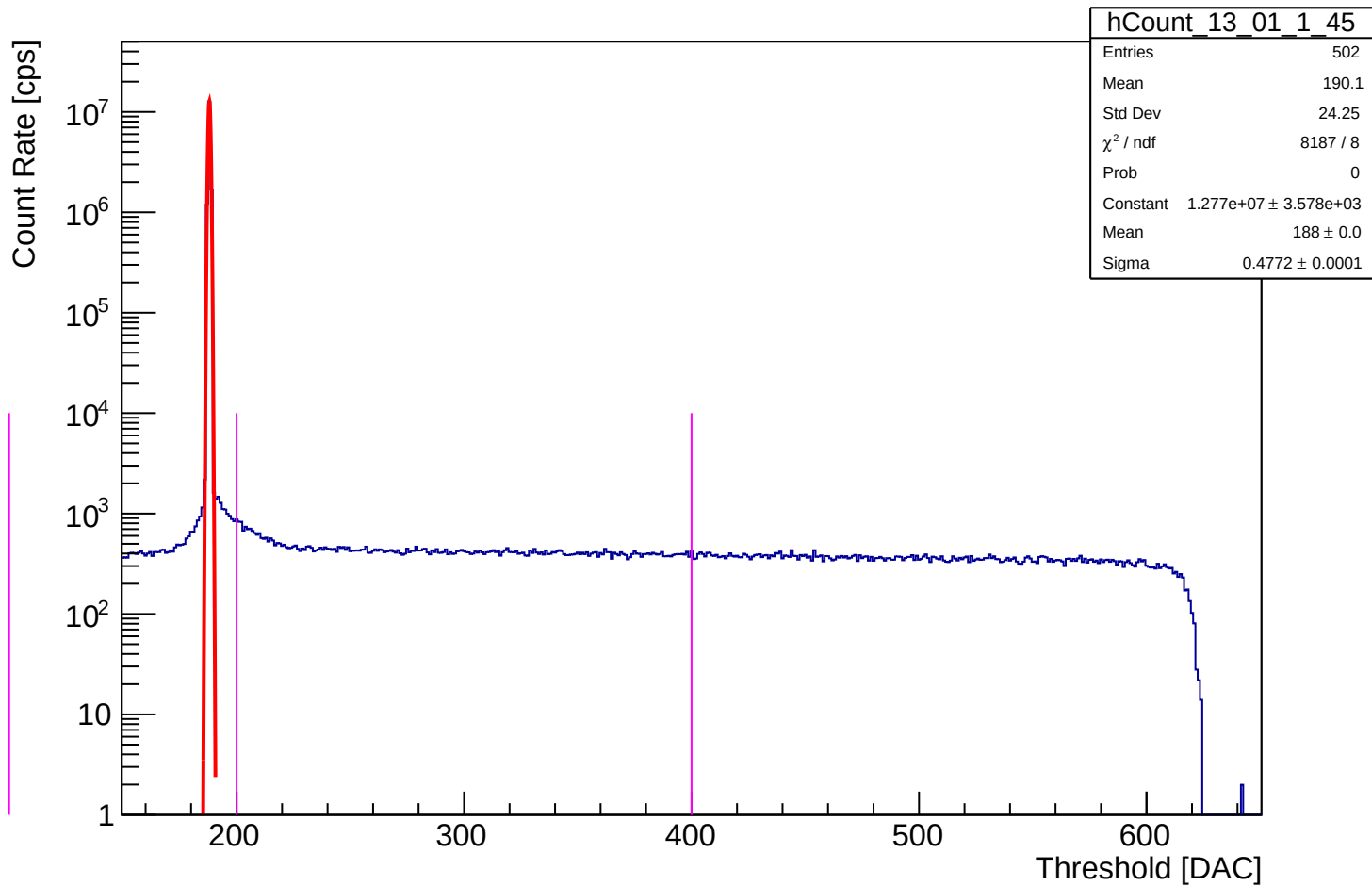




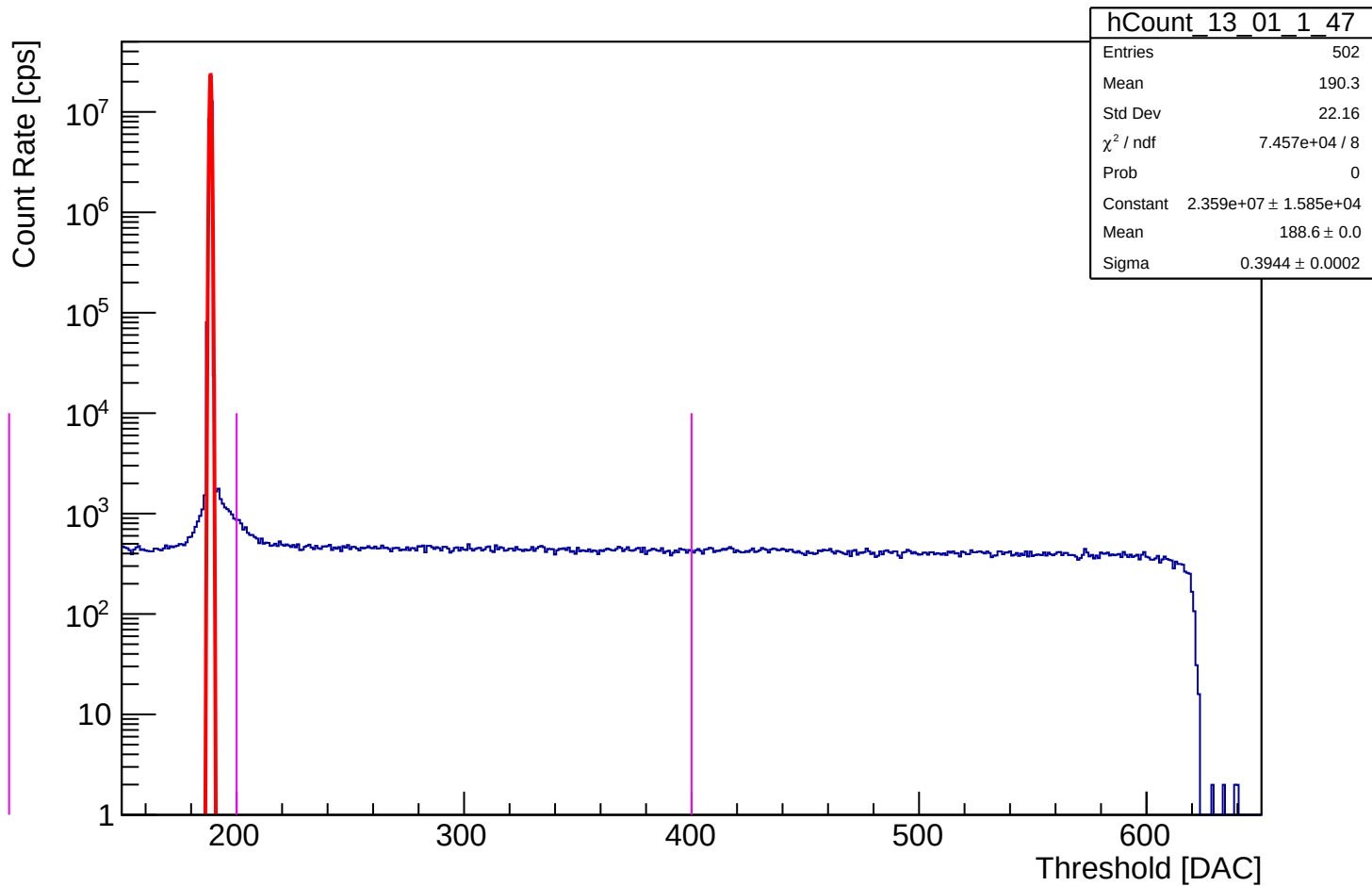
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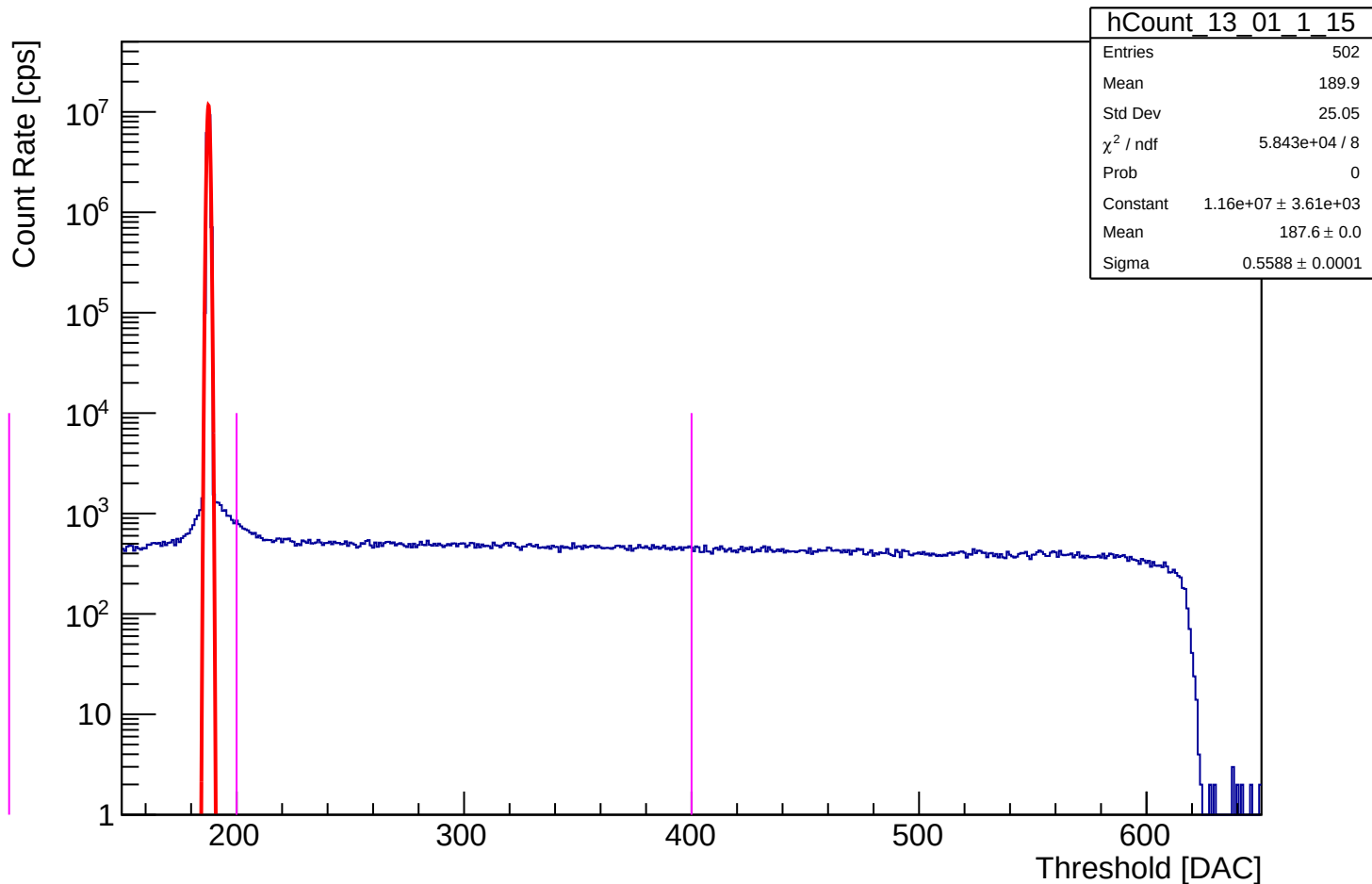
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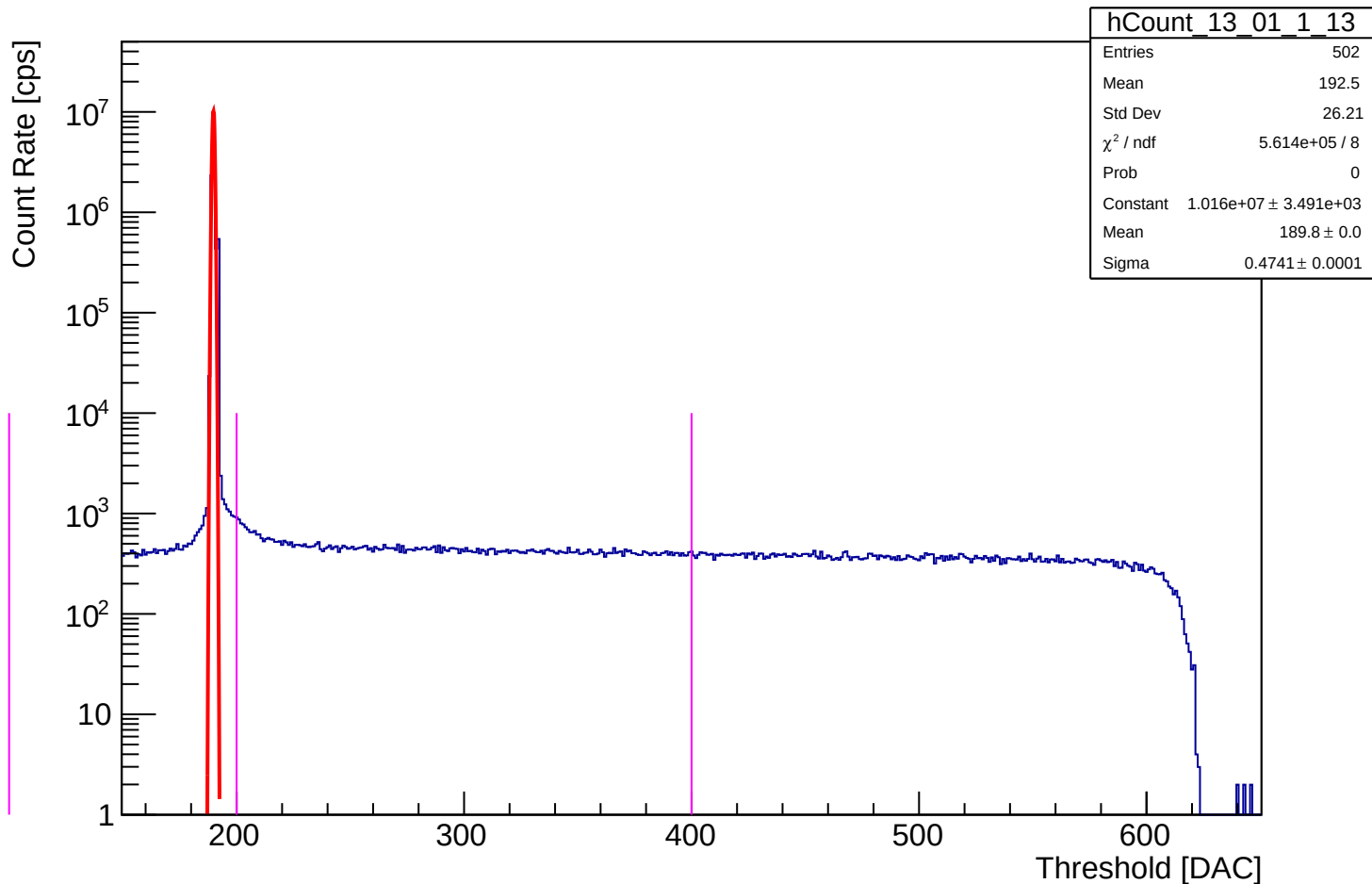
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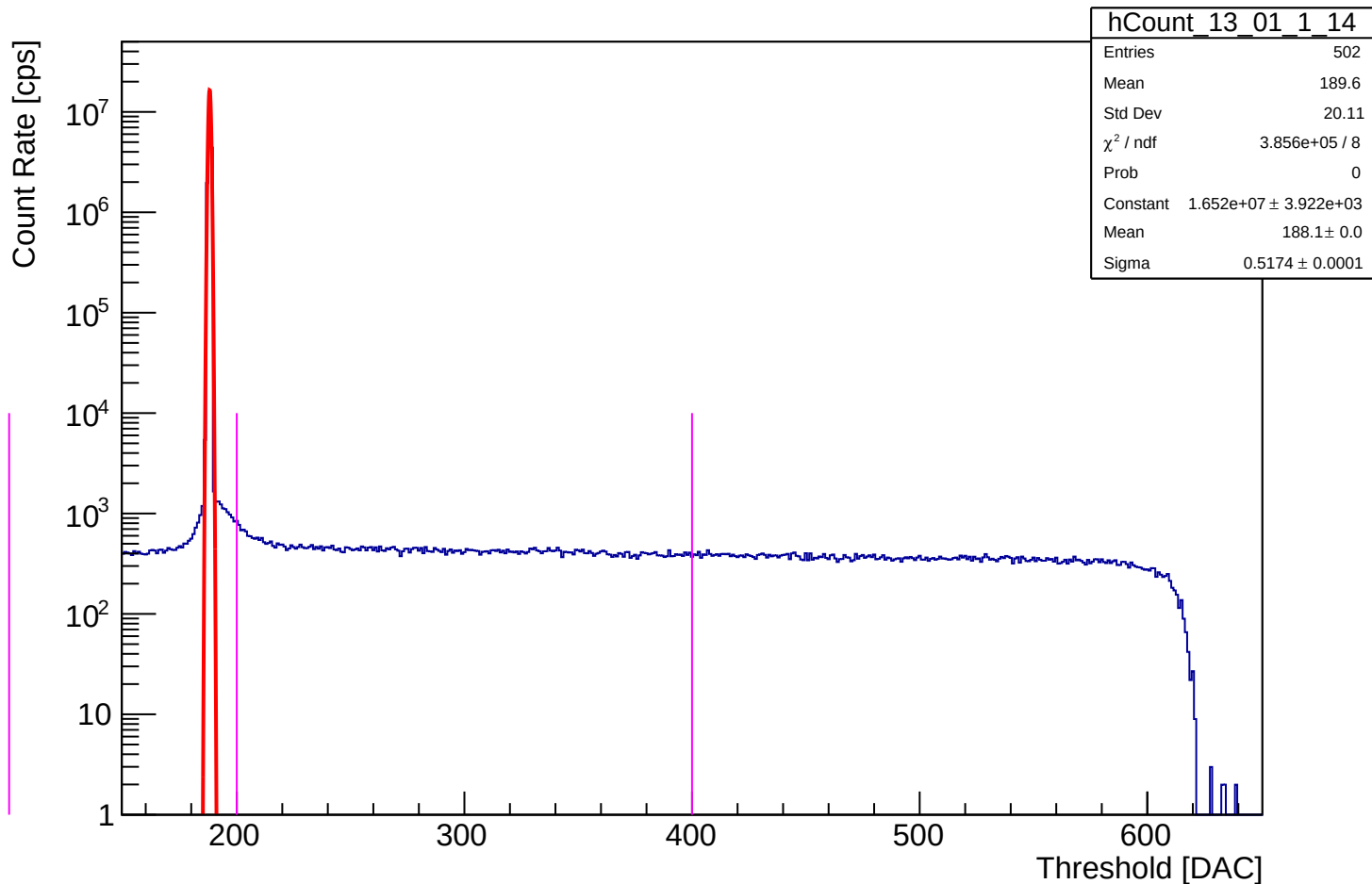
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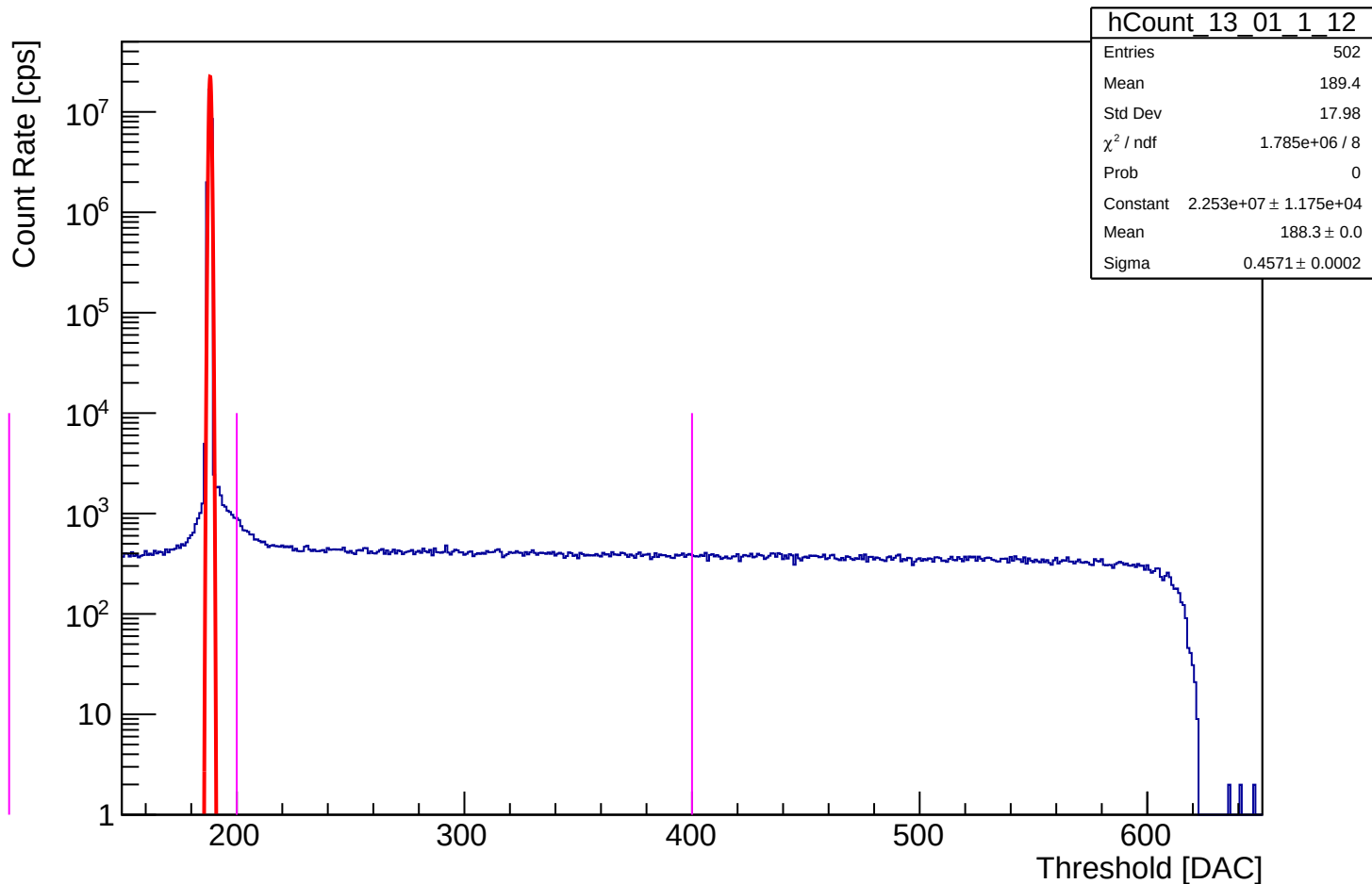
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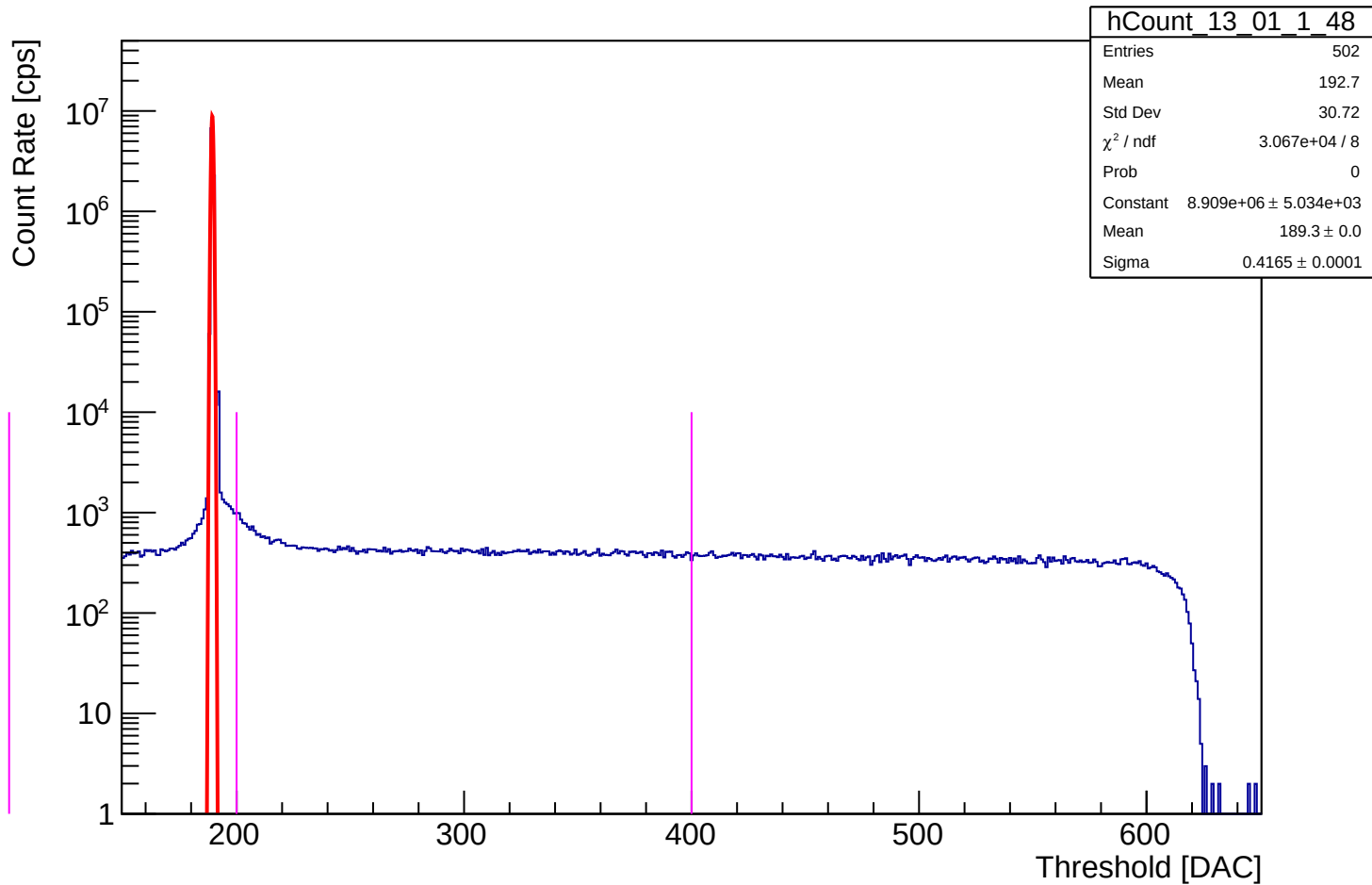
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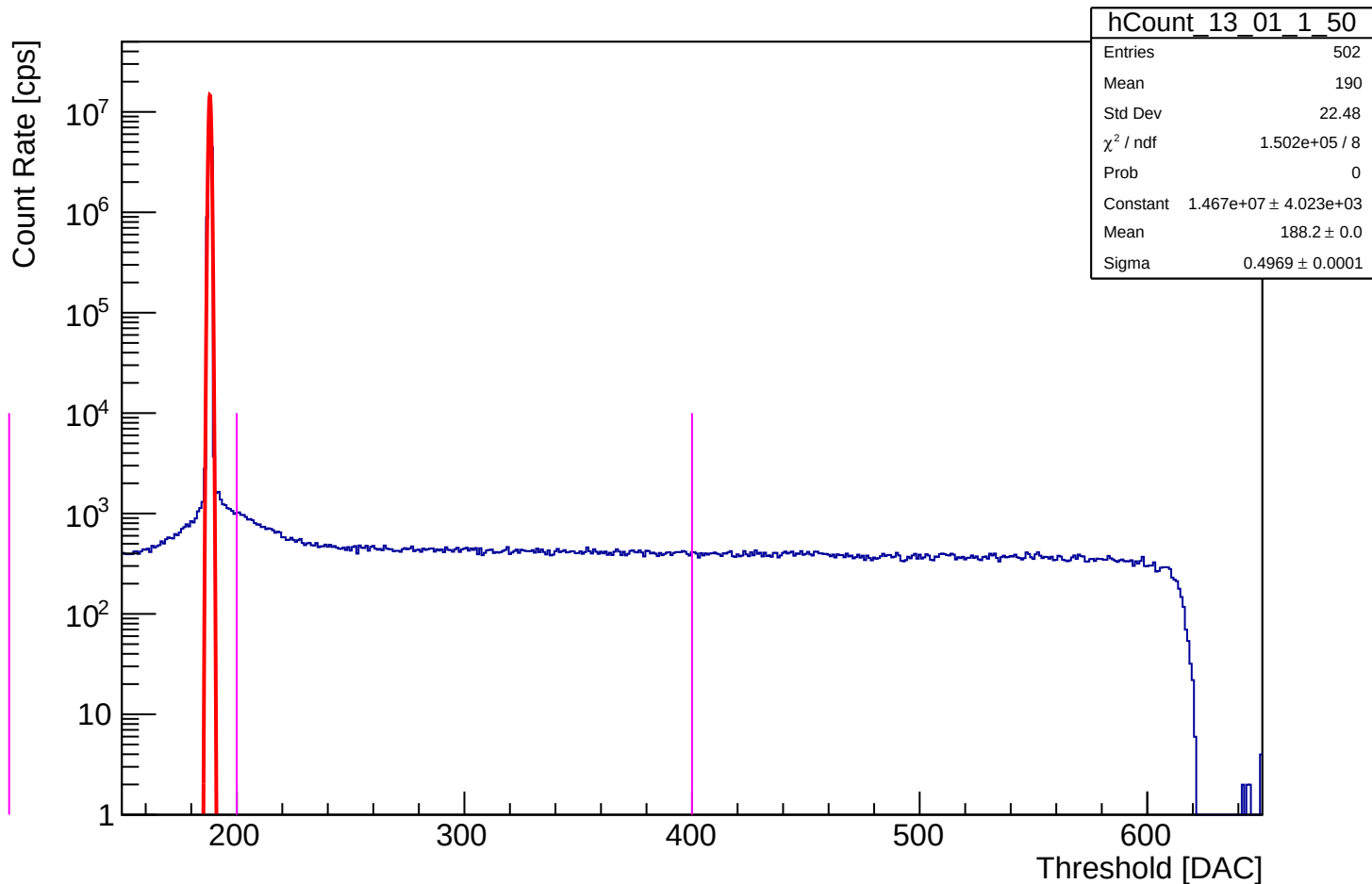
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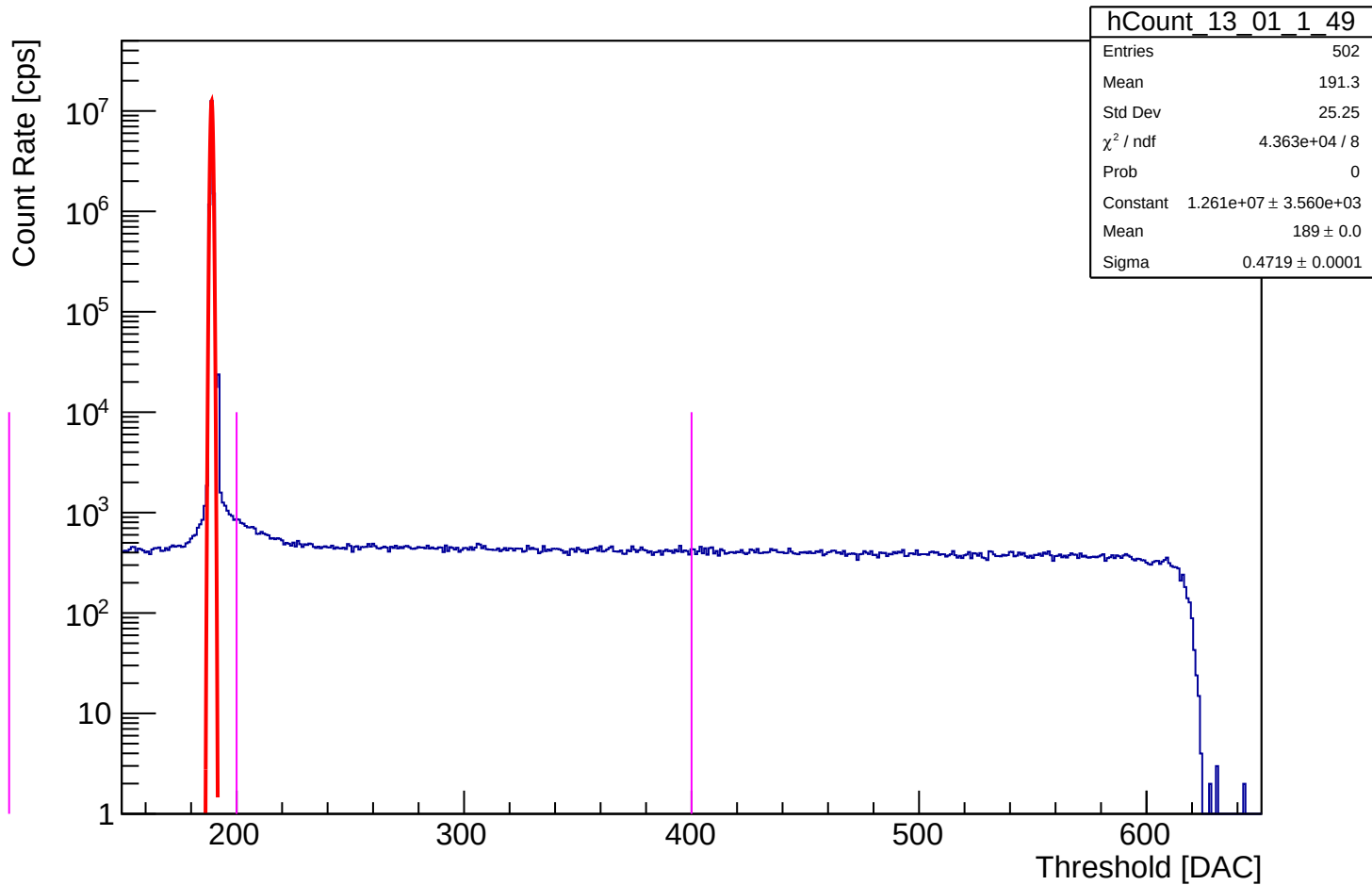
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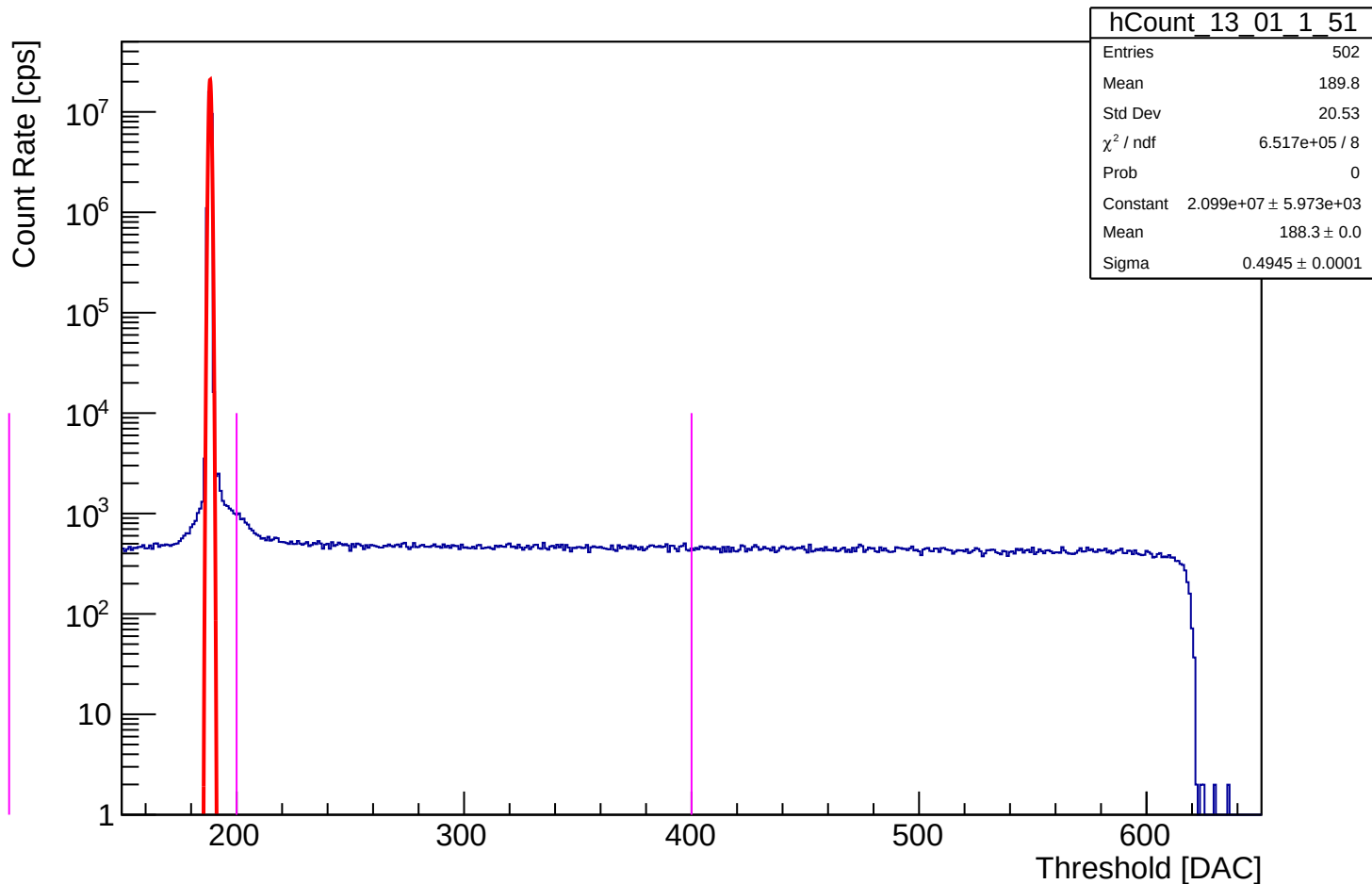
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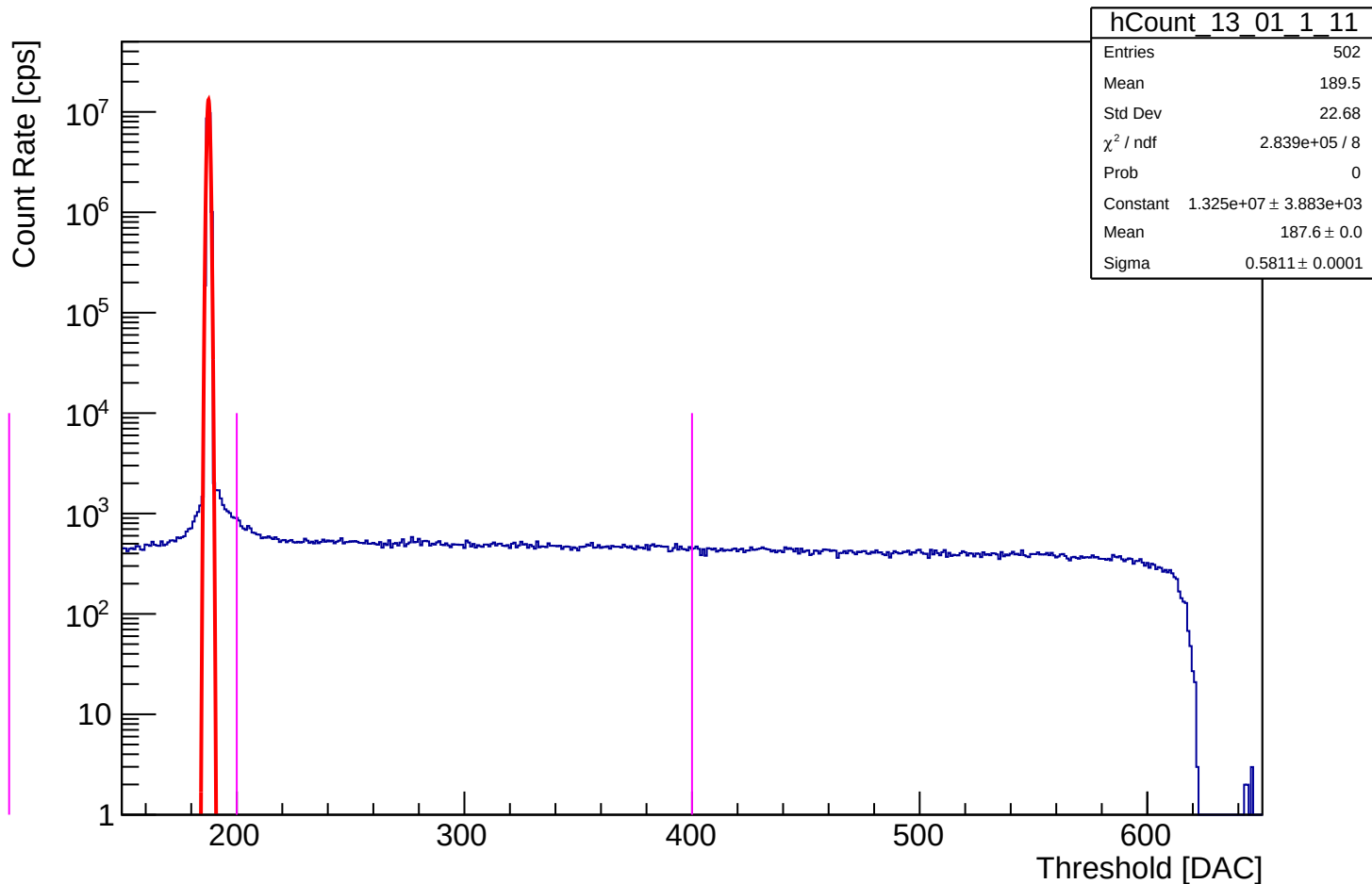
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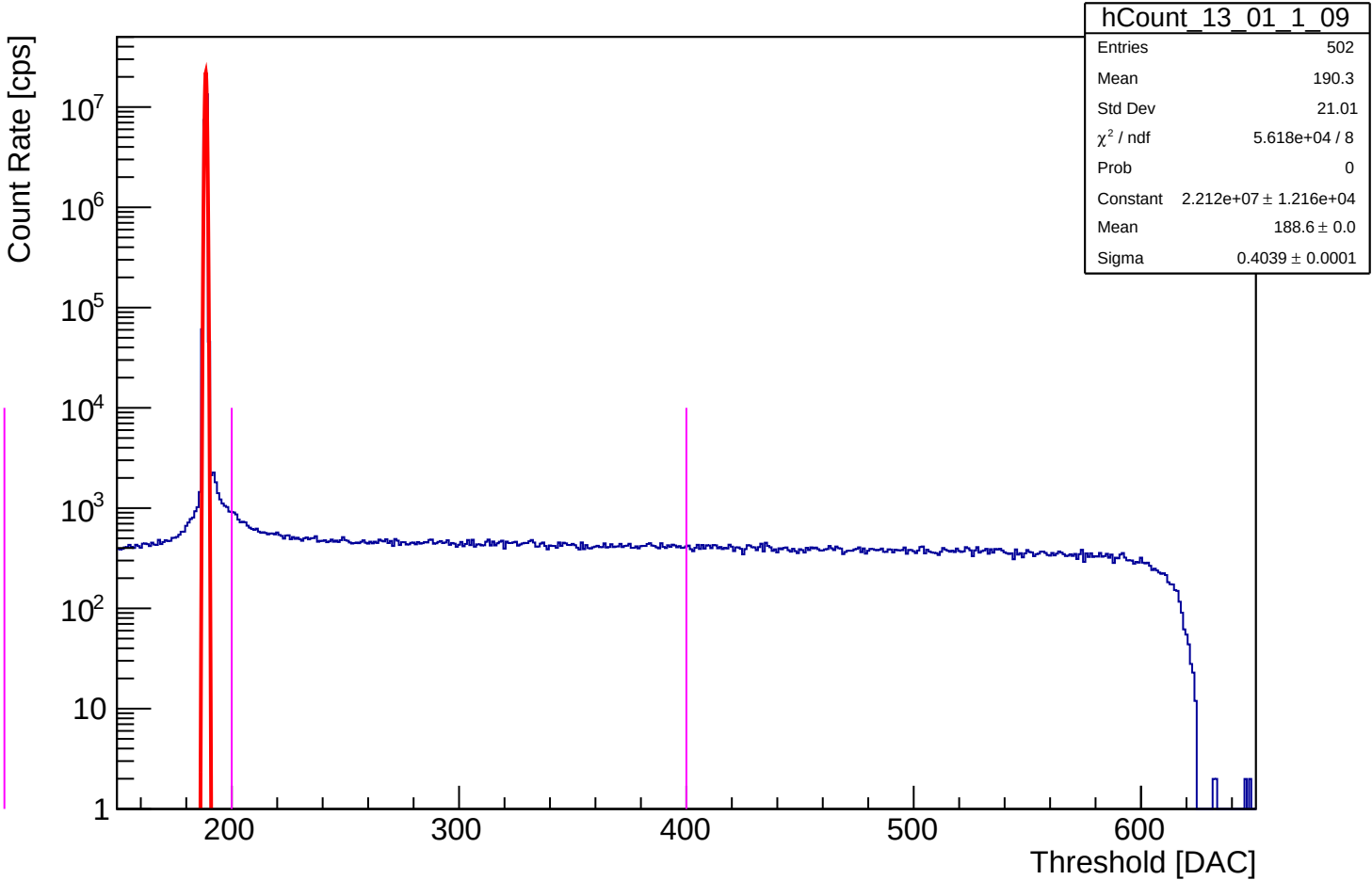


Row 1 Tile 1 Pmt 5 Pixel 40 Slot 13 Fiber 1 Asic 1 Channel 51

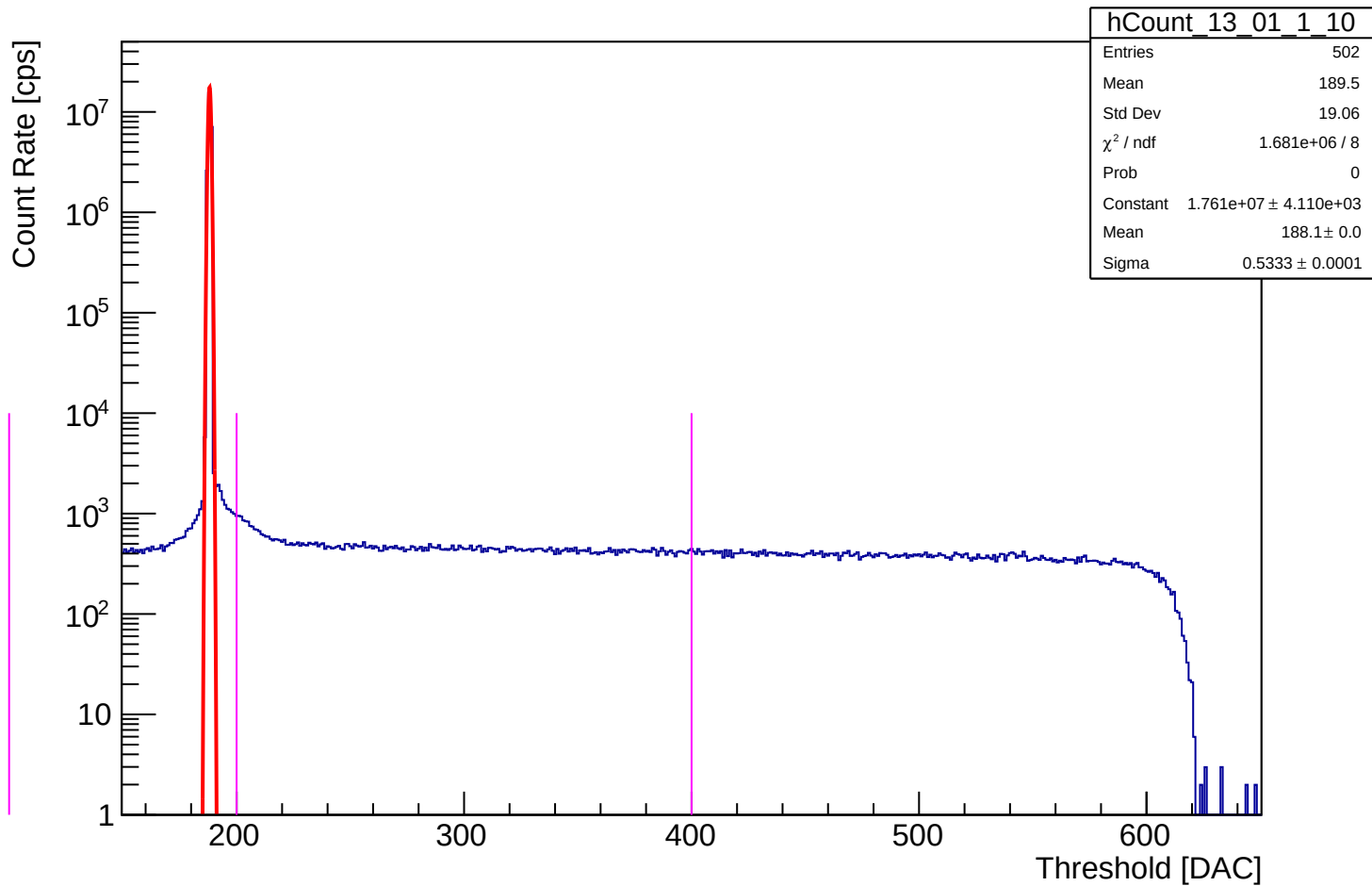


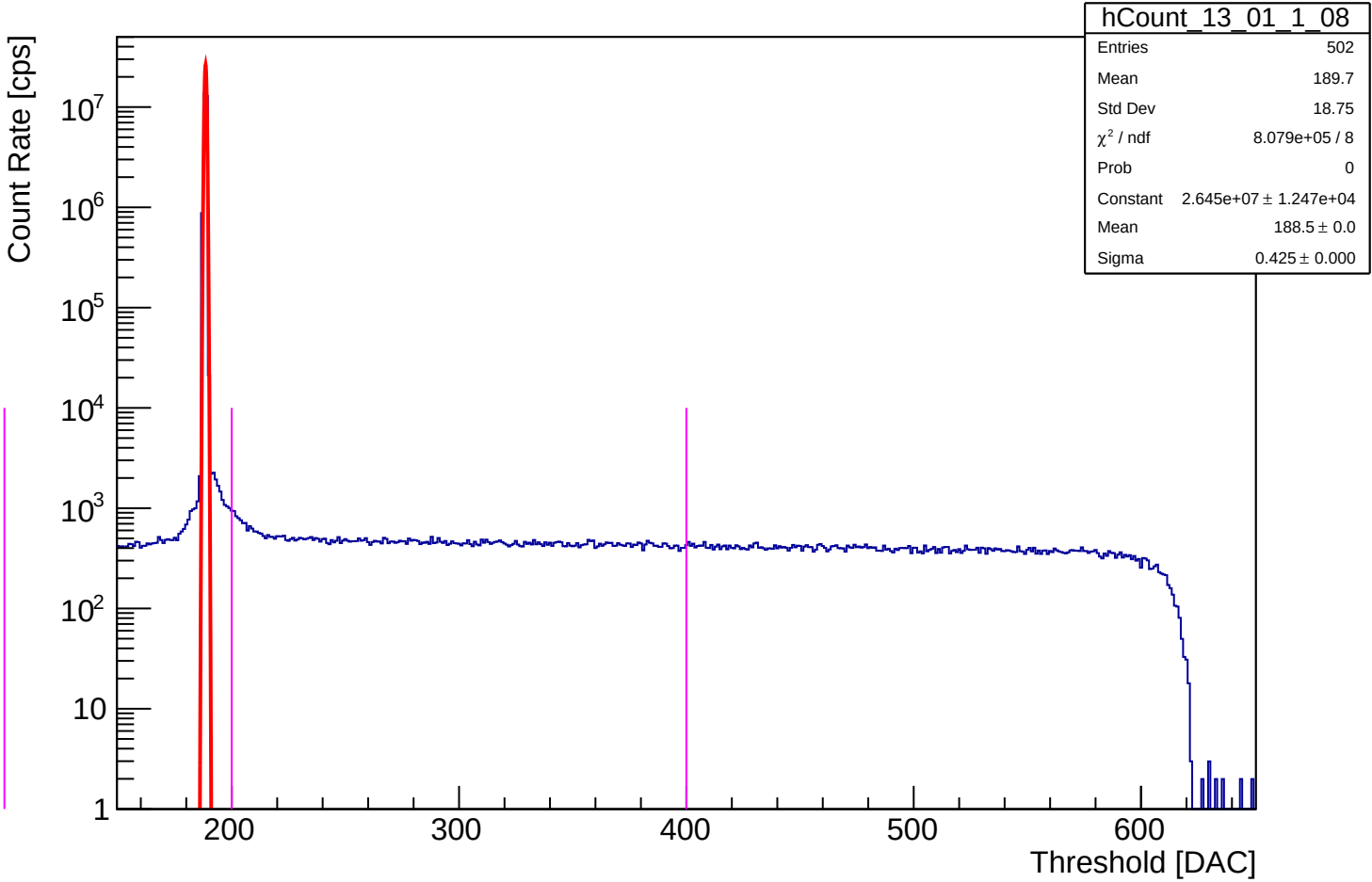
Row 1 Tile 1 Pmt 5 Pixel 41 Slot 13 Fiber 1 Asic 1 Channel 11



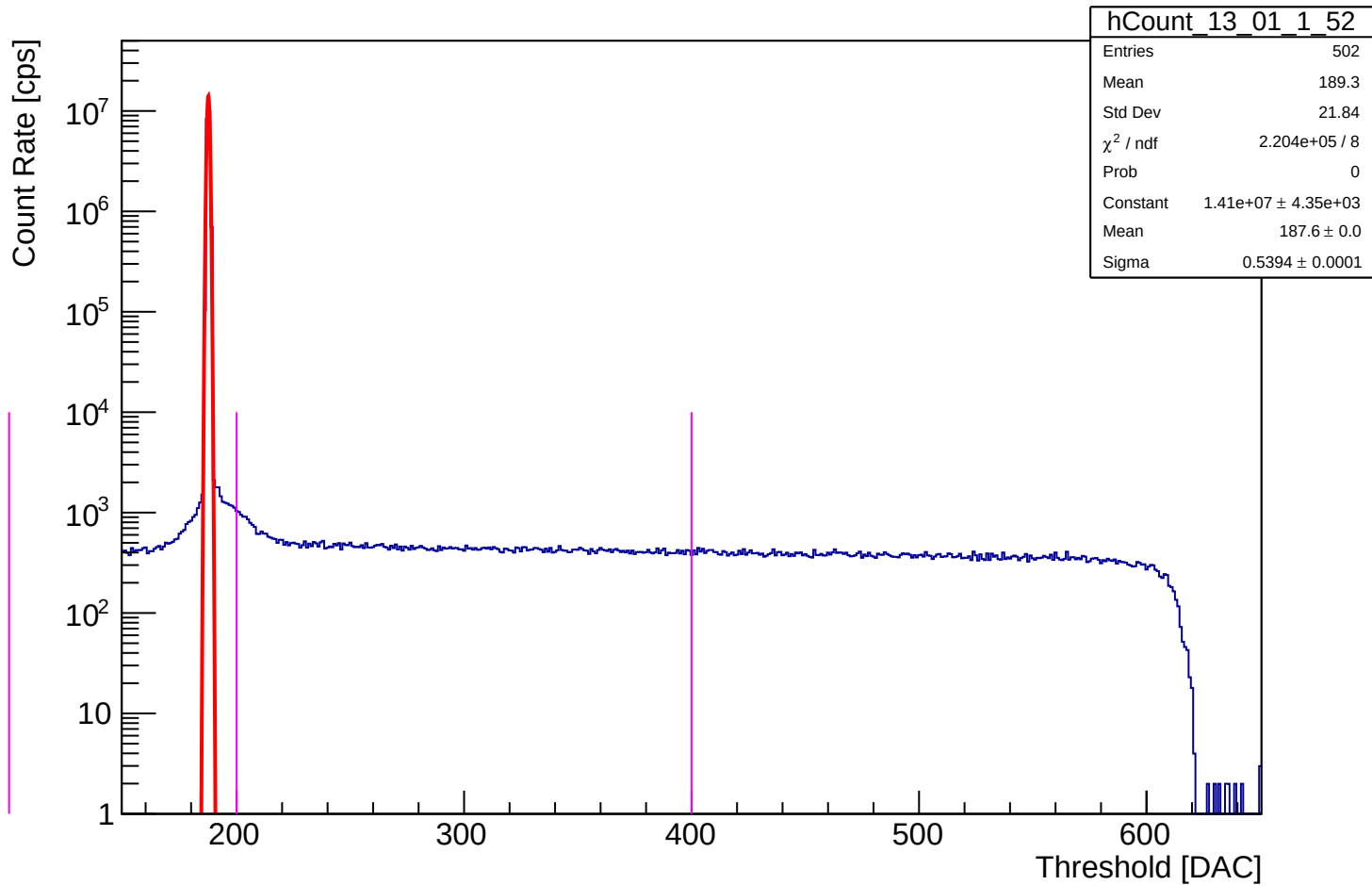


Row 1 Tile 1 Pmt 5 Pixel 43 Slot 13 Fiber 1 Asic 1 Channel 10

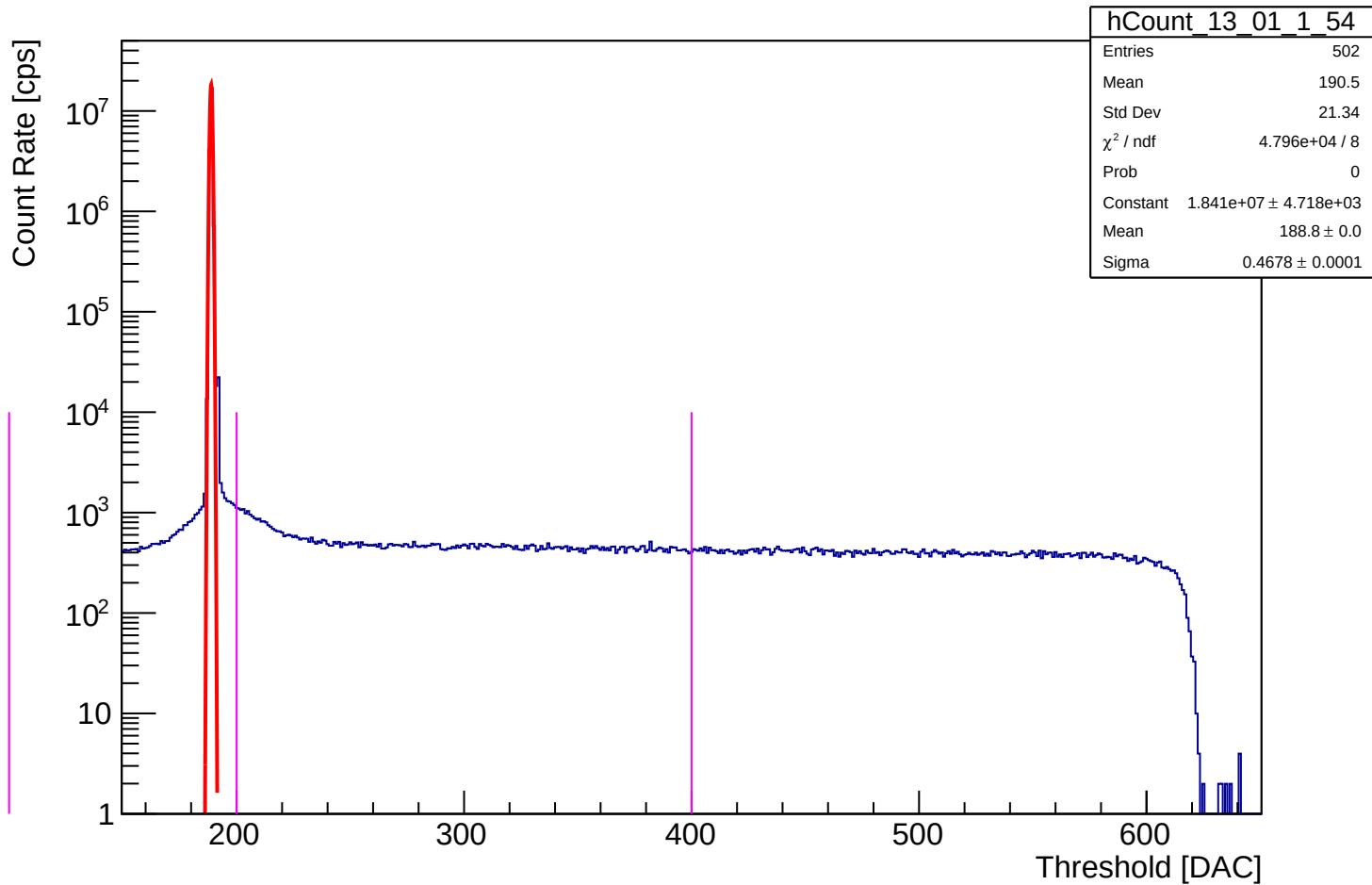




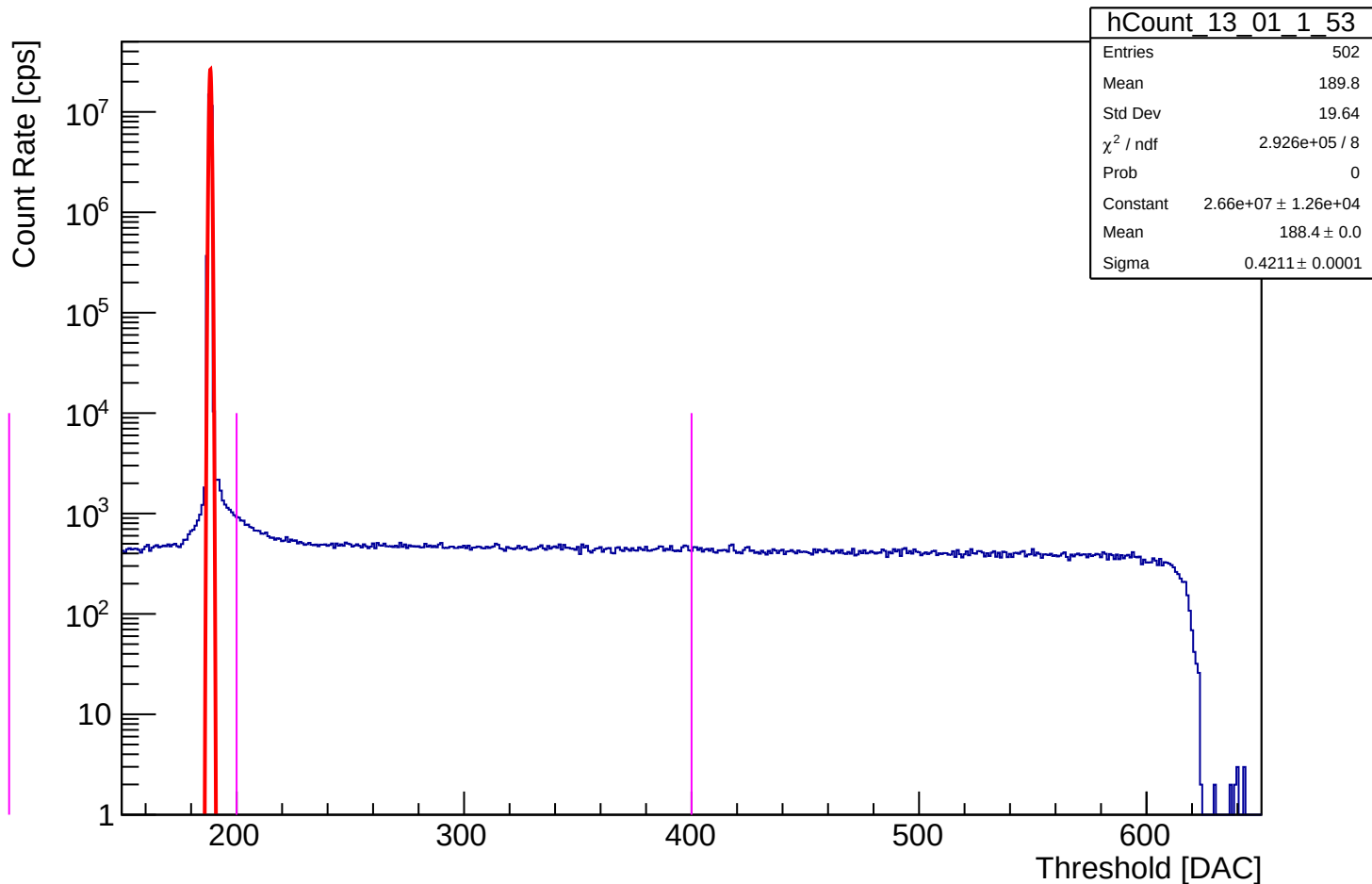
Row 1 Tile 1 Pmt 5 Pixel 45 Slot 13 Fiber 1 Asic 1 Channel 52



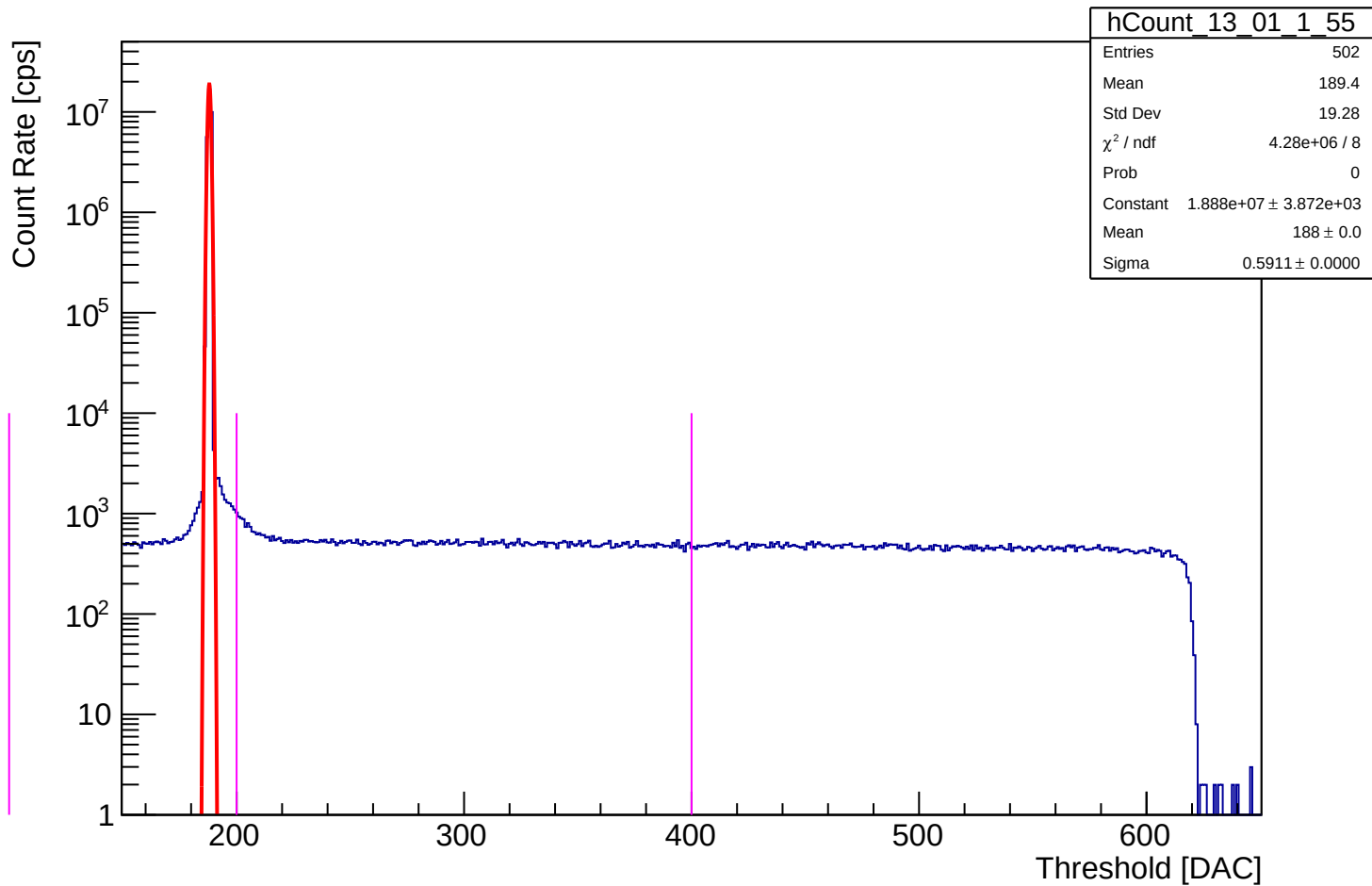
Row 1 Tile 1 Pmt 5 Pixel 46 Slot 13 Fiber 1 Asic 1 Channel 54

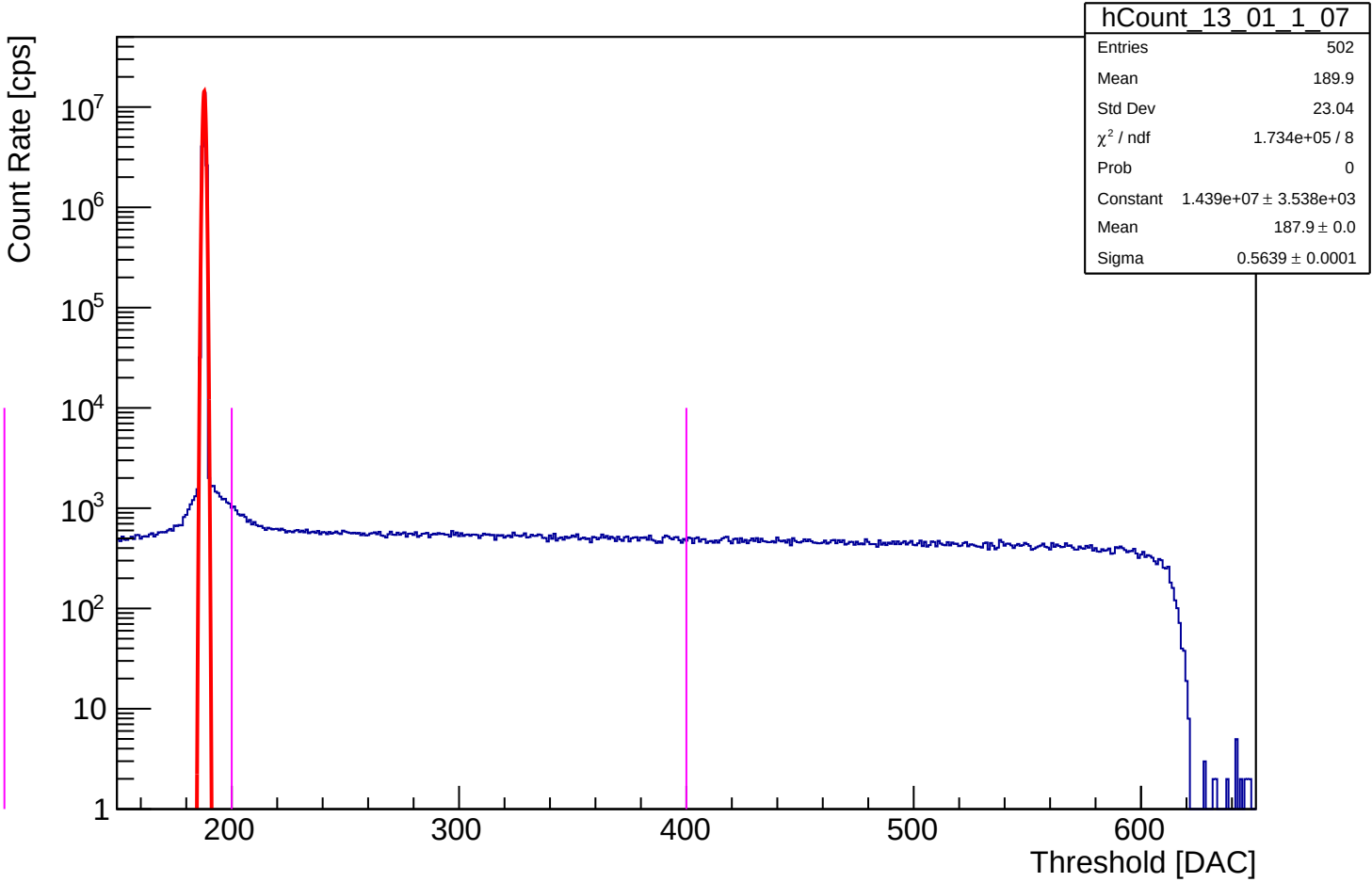


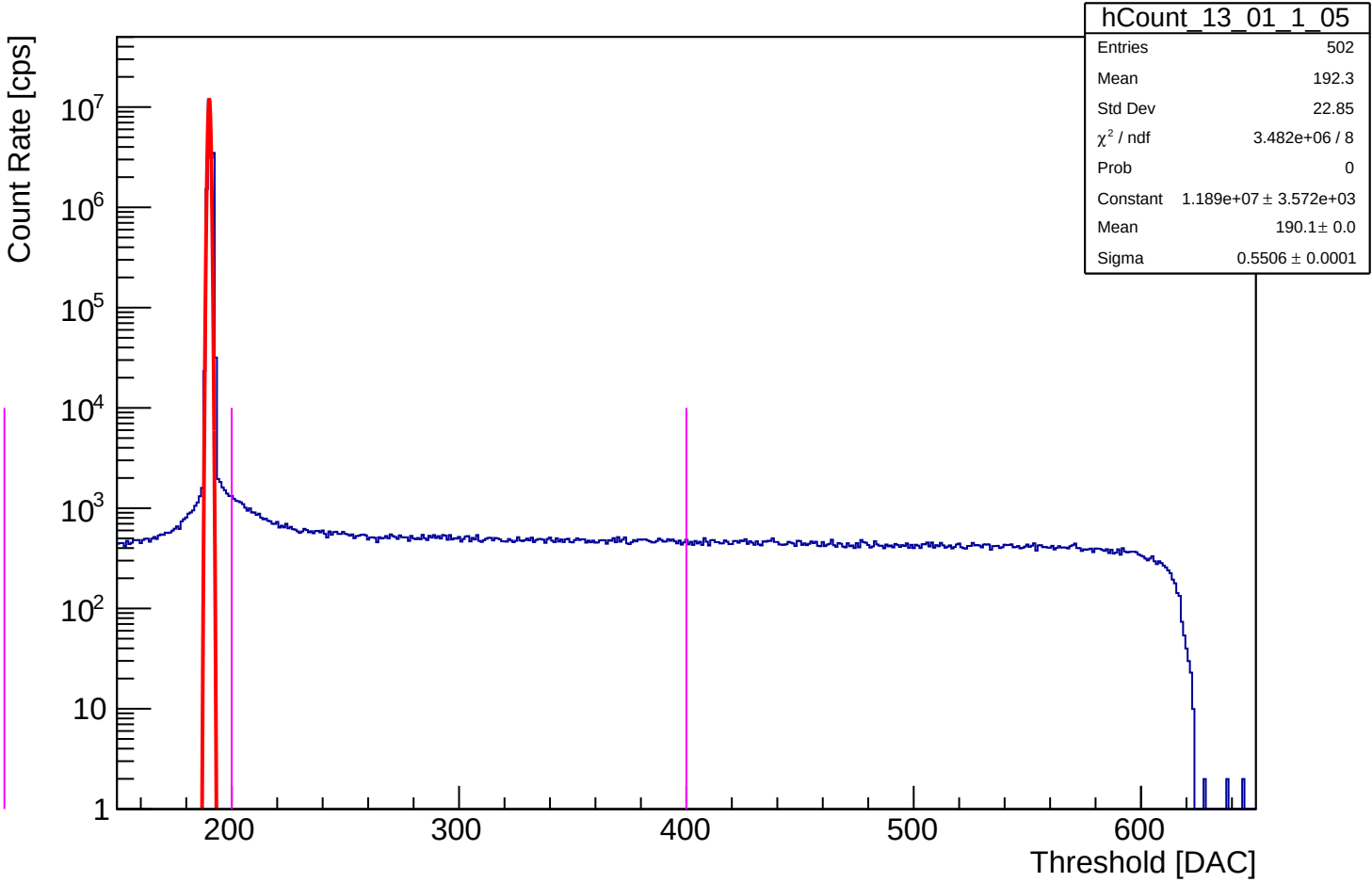
Row 1 Tile 1 Pmt 5 Pixel 47 Slot 13 Fiber 1 Asic 1 Channel 53

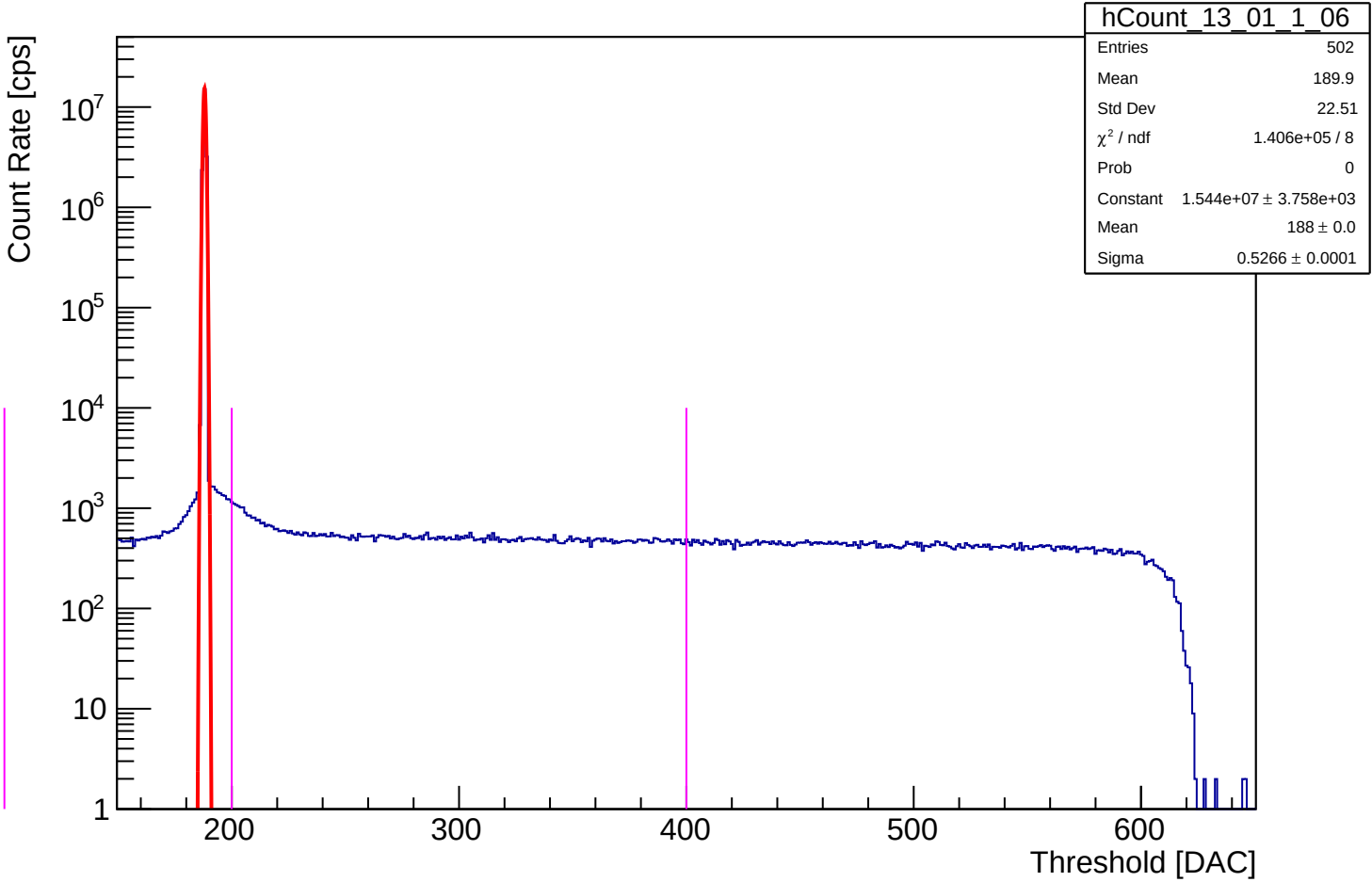


Row 1 Tile 1 Pmt 5 Pixel 48 Slot 13 Fiber 1 Asic 1 Channel 55





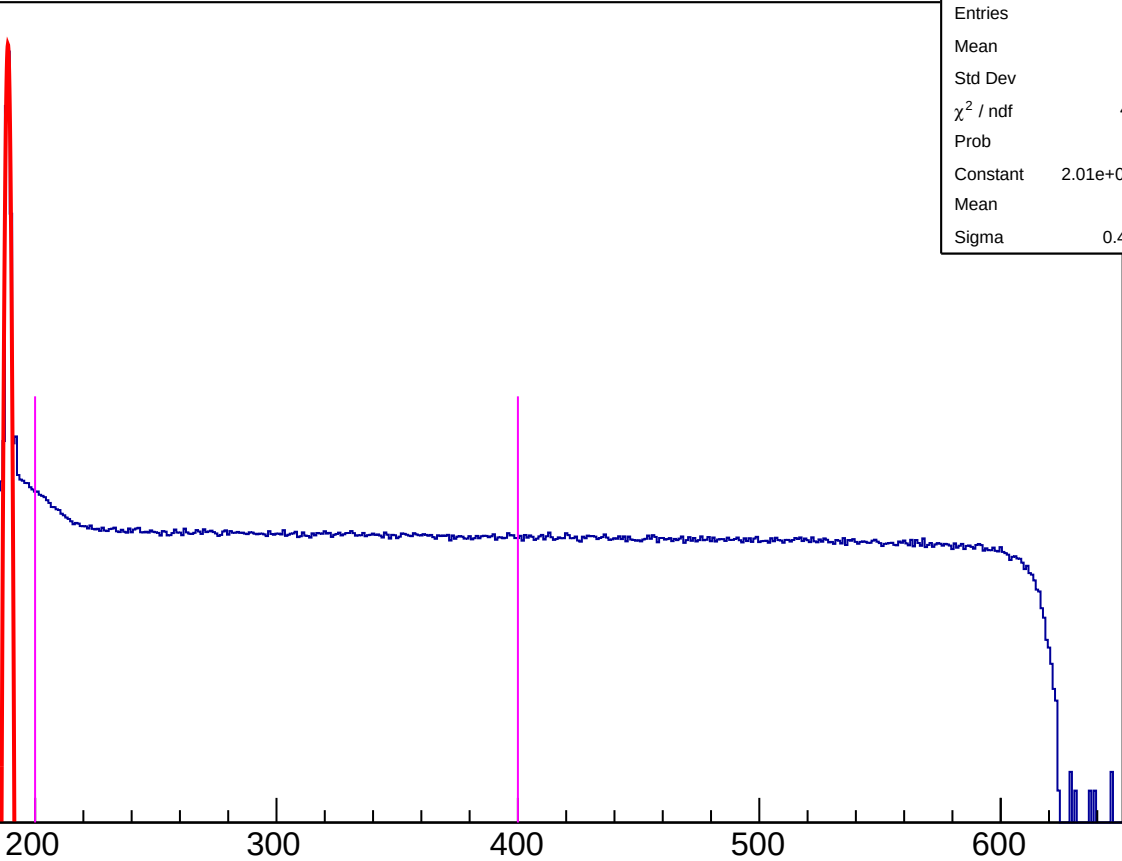




Count Rate [cps]

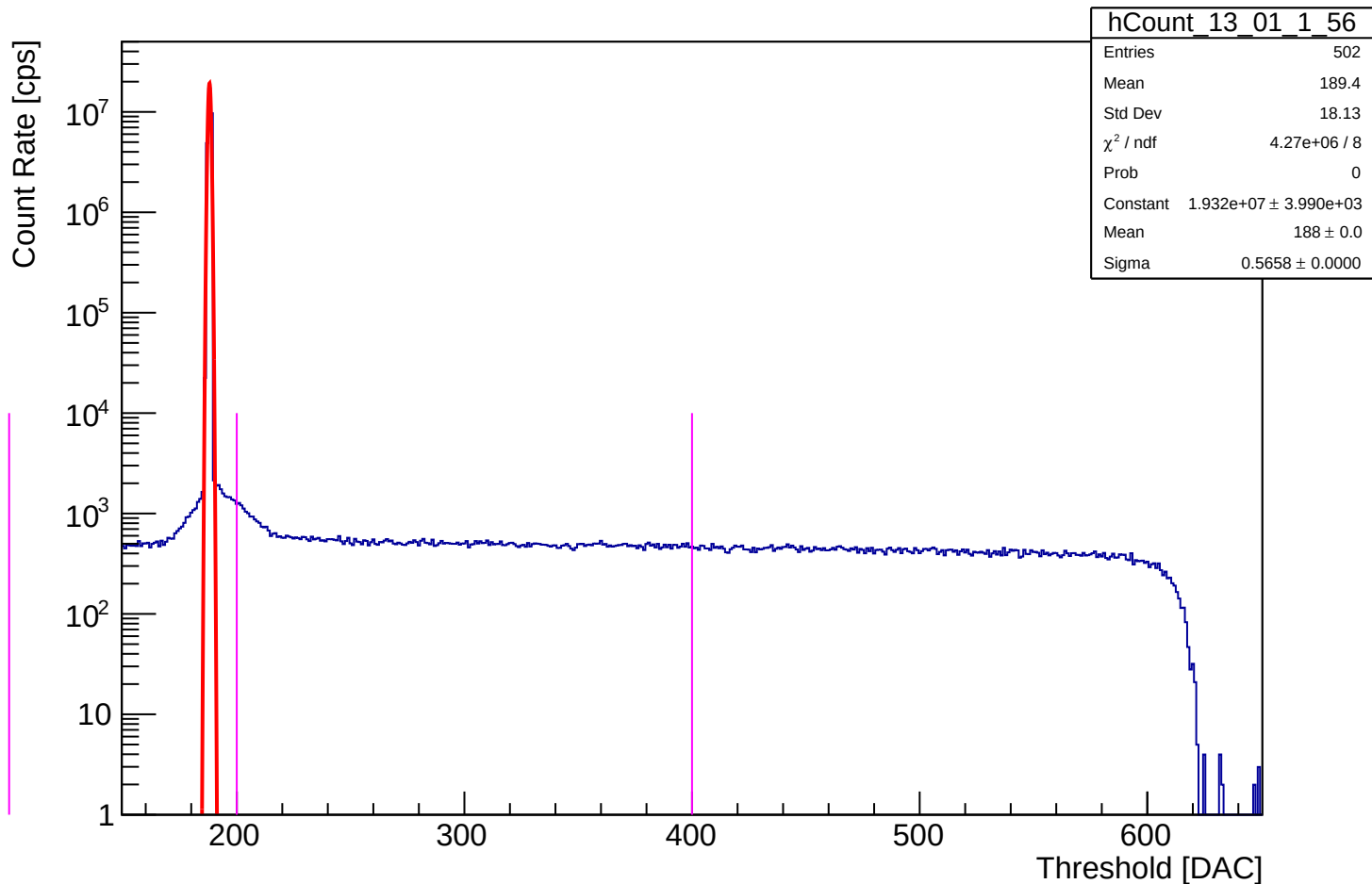
10^7
 10^6
 10^5
 10^4
 10^3
 10^2
 10
 1

hCount_13_01_1_04	
Entries	502
Mean	190.5
Std Dev	21.73
χ^2 / ndf	4.312e+04 / 8
Prob	0
Constant	$2.01\text{e}+07 \pm 5.36\text{e}+03$
Mean	188.8 ± 0.0
Sigma	0.4574 ± 0.0001

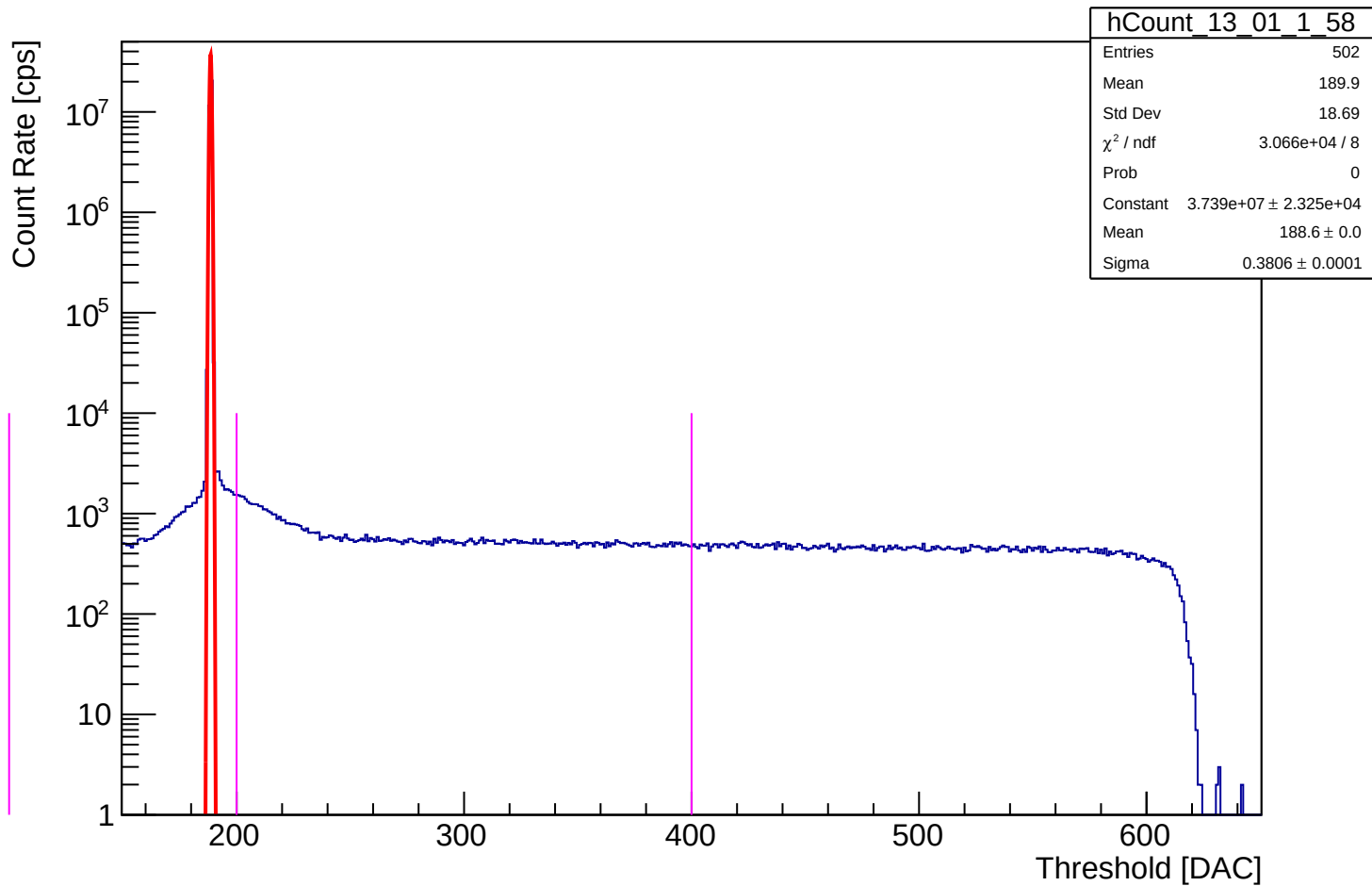


Threshold [DAC]

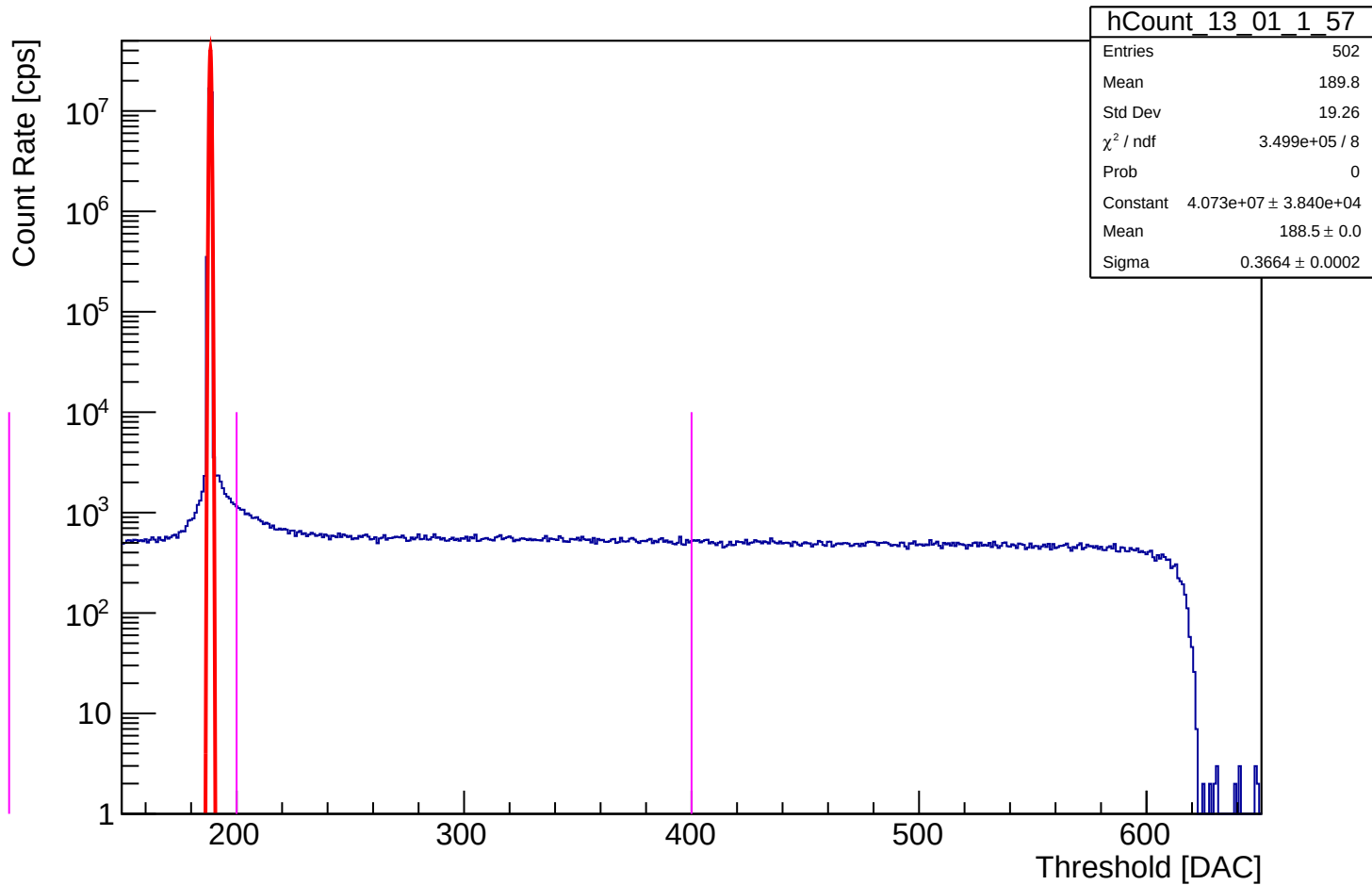
Row 1 Tile 1 Pmt 5 Pixel 53 Slot 13 Fiber 1 Asic 1 Channel 56

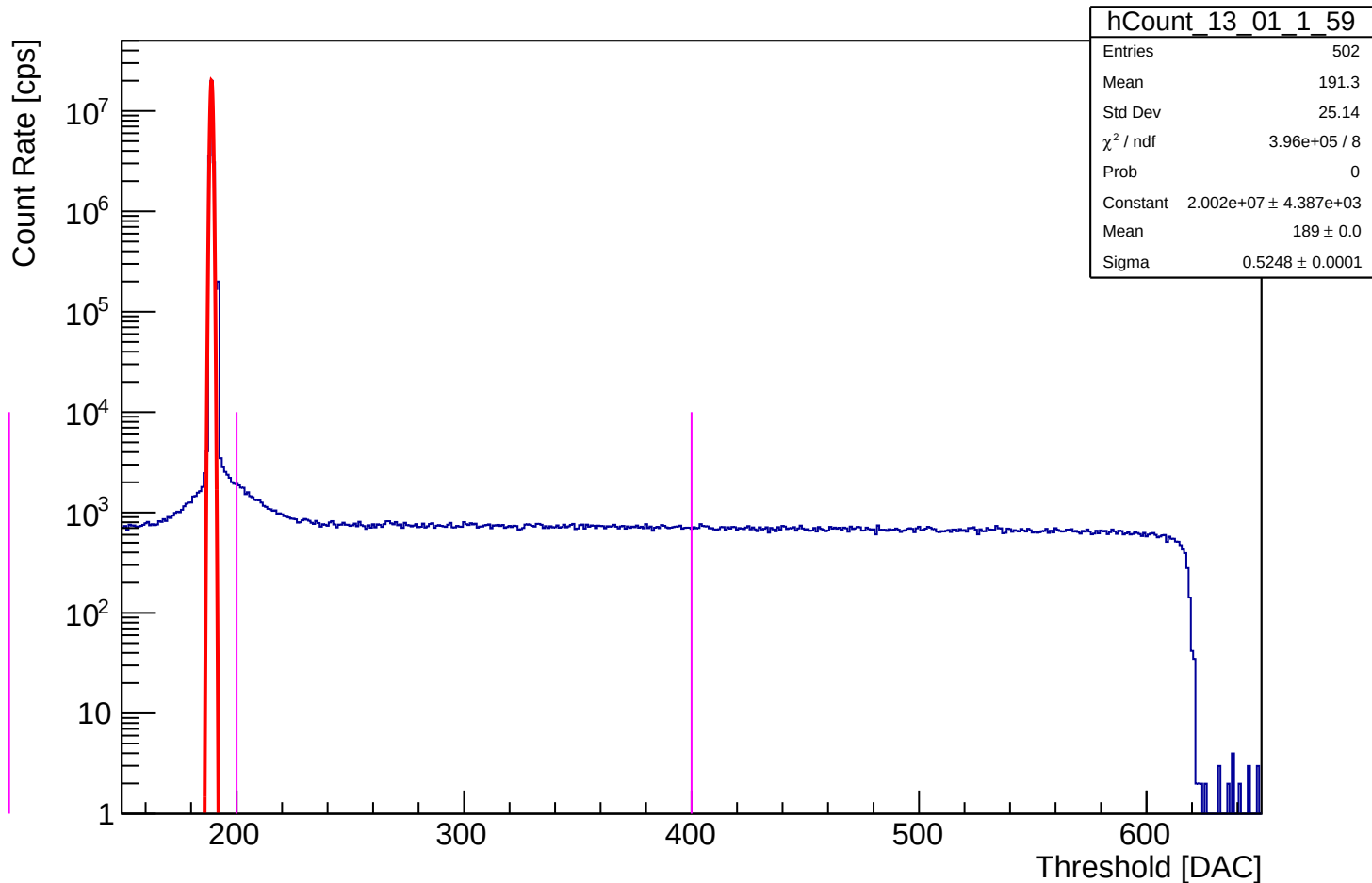


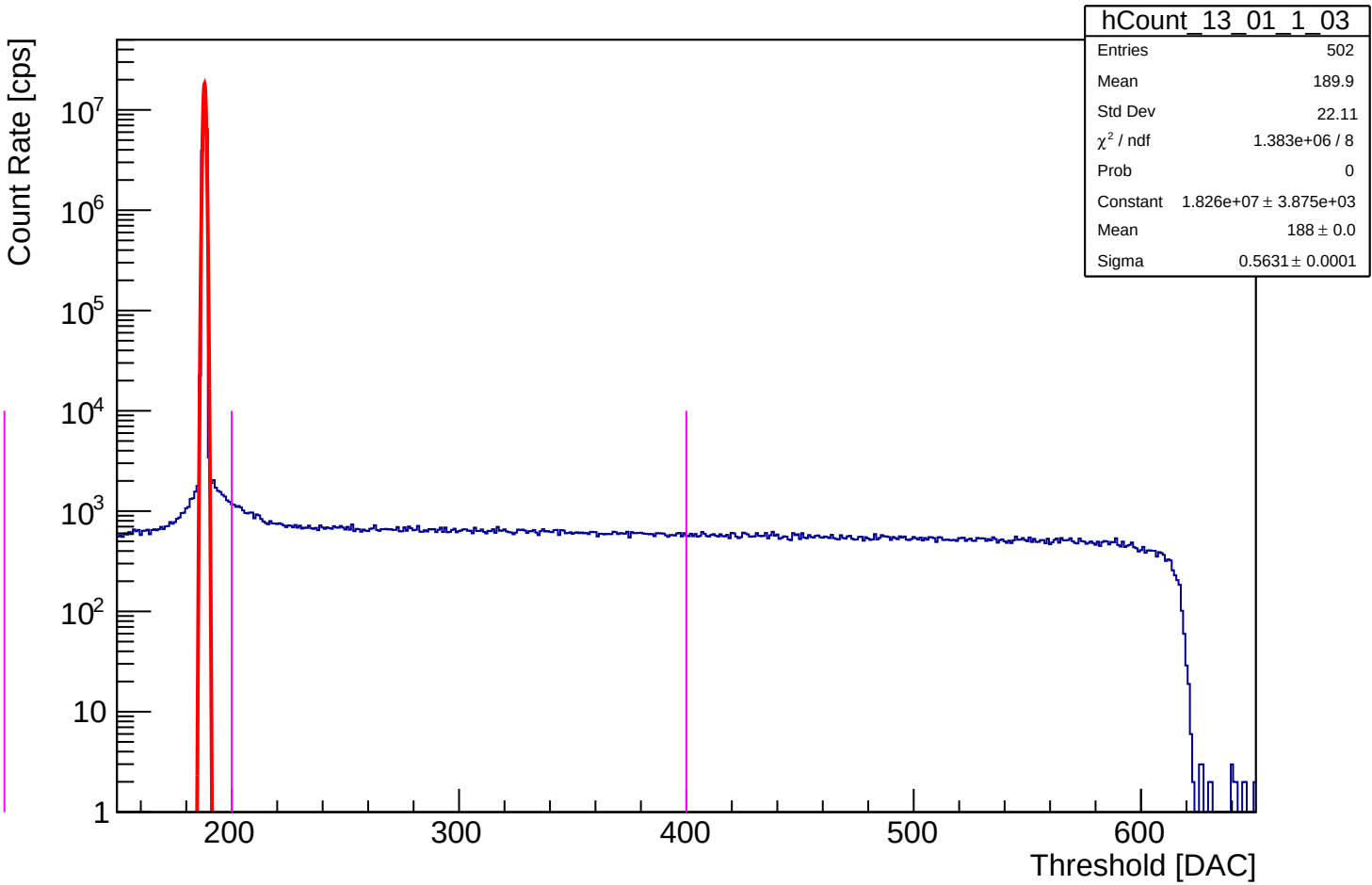
Row 1 Tile 1 Pmt 5 Pixel 54 Slot 13 Fiber 1 Asic 1 Channel 58



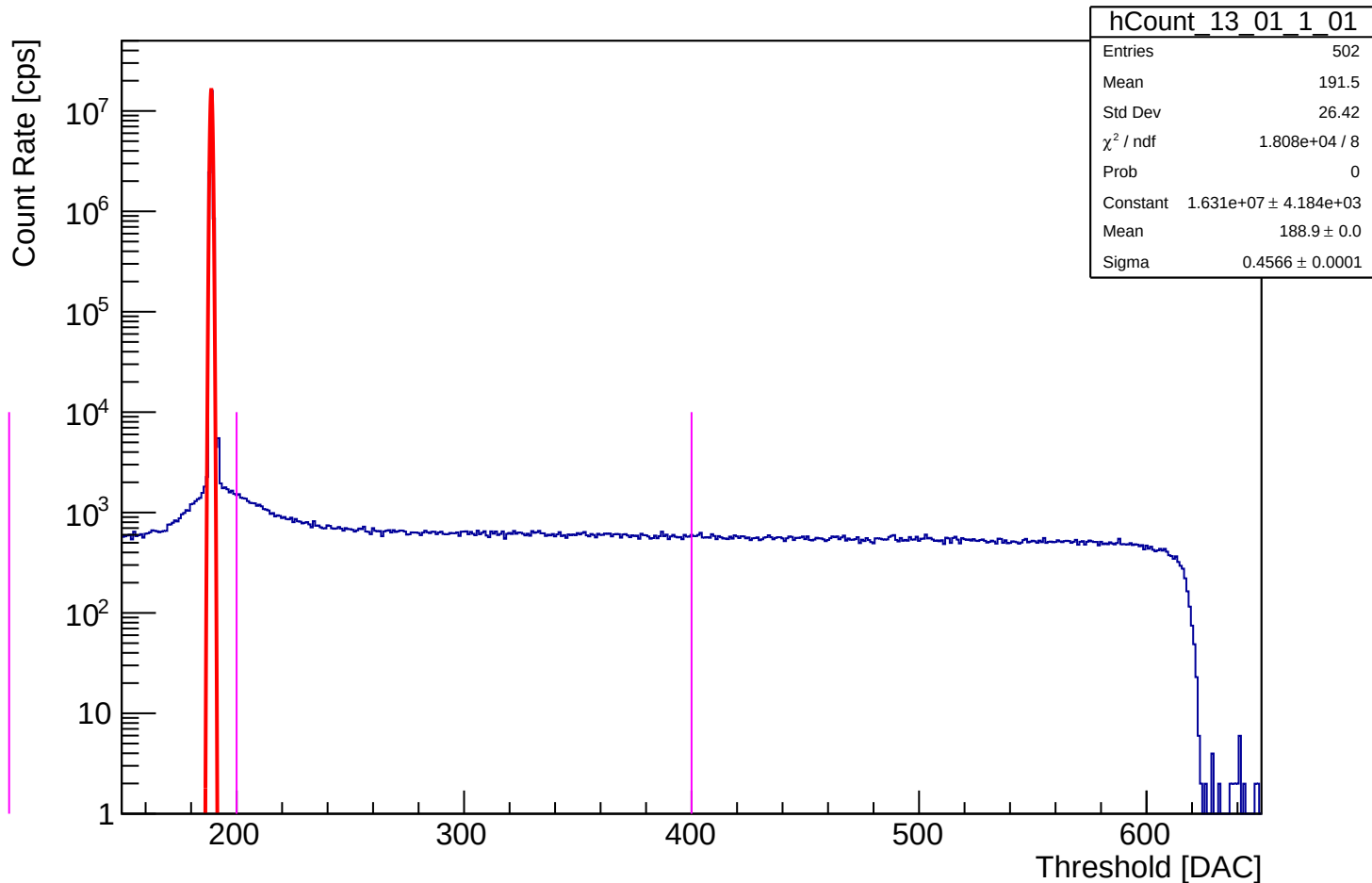
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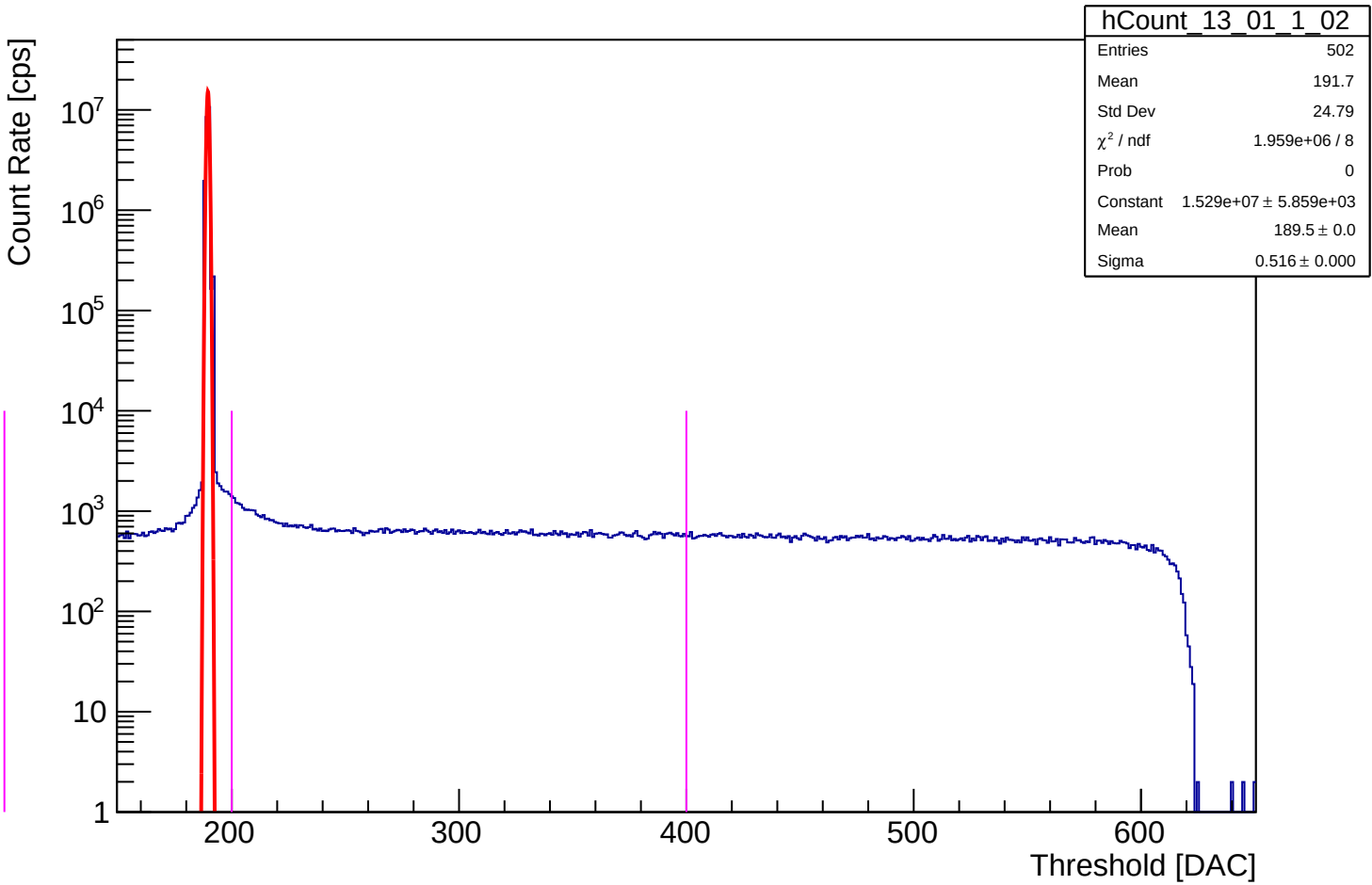


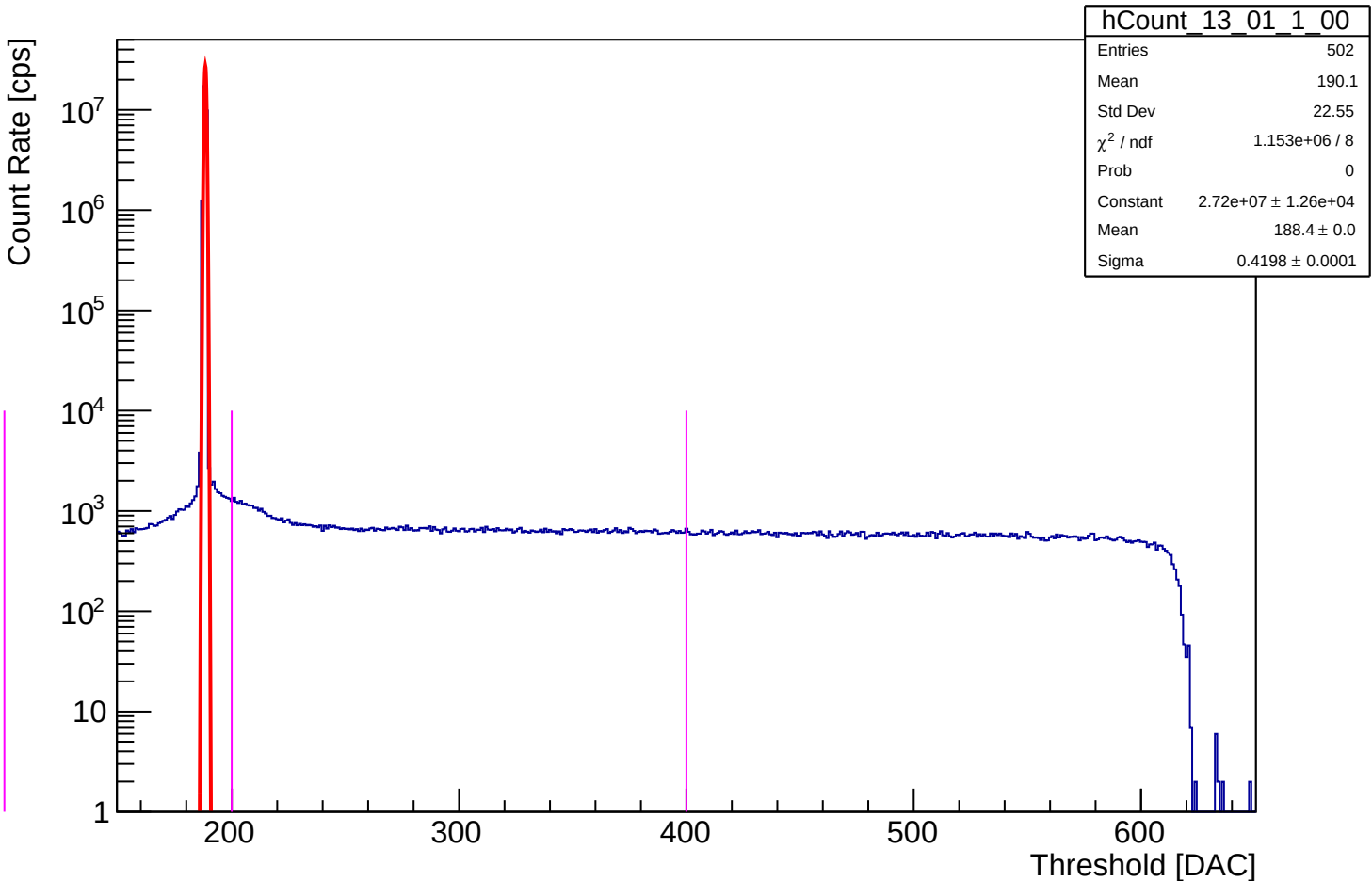




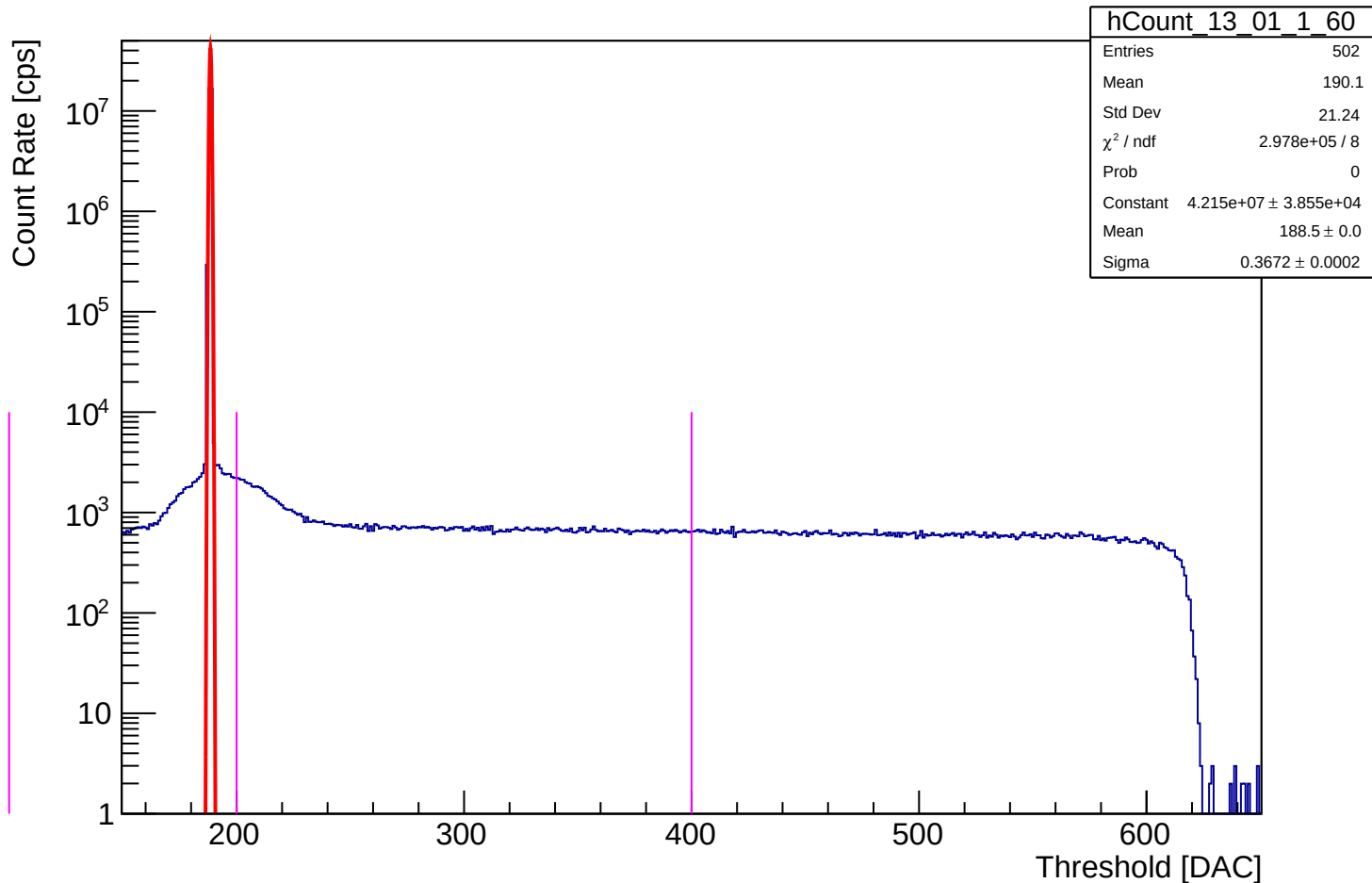
Row 1 Tile 1 Pmt 5 Pixel 58 Slot 13 Fiber 1 Asic 1 Channel 1



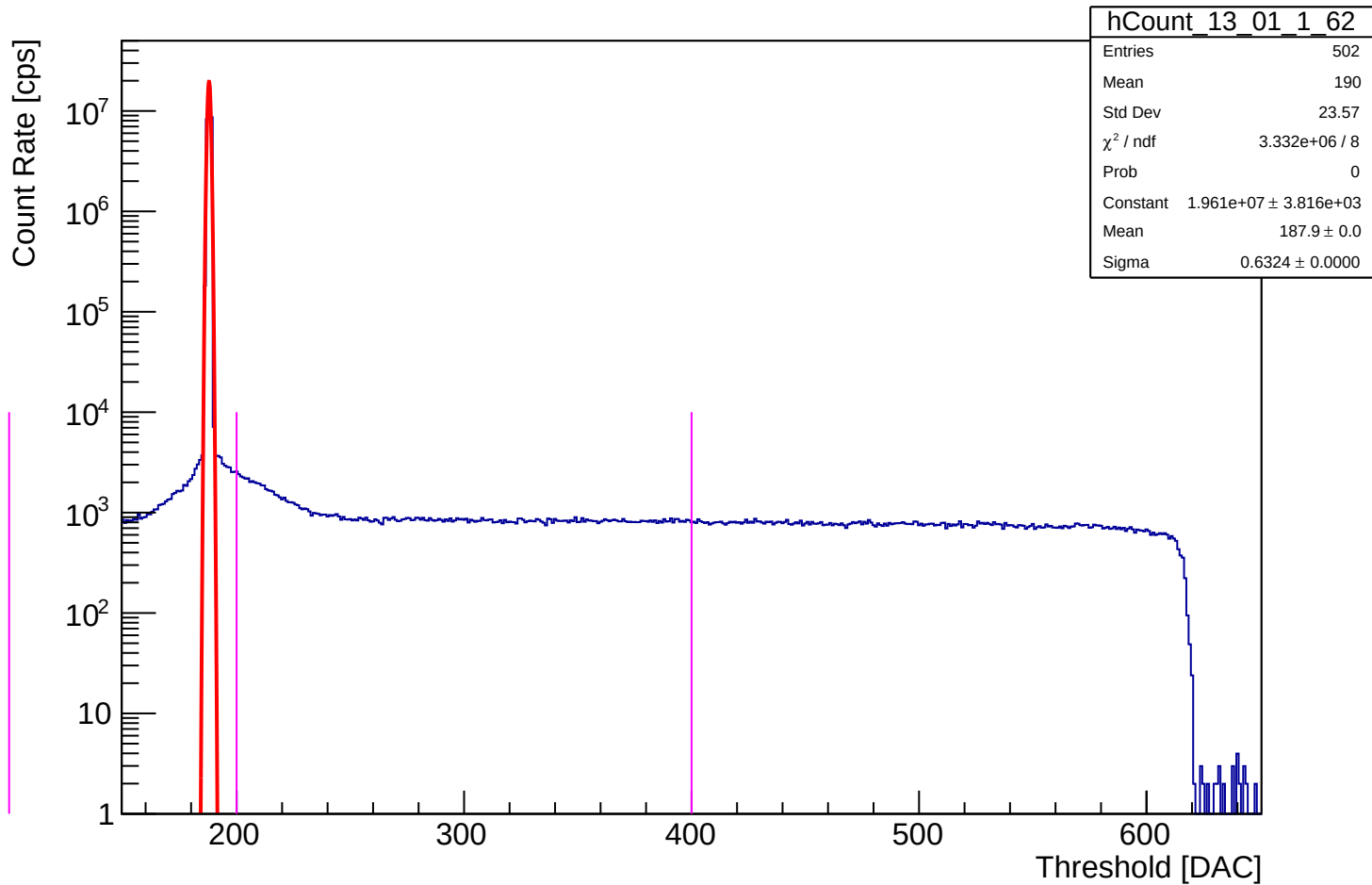


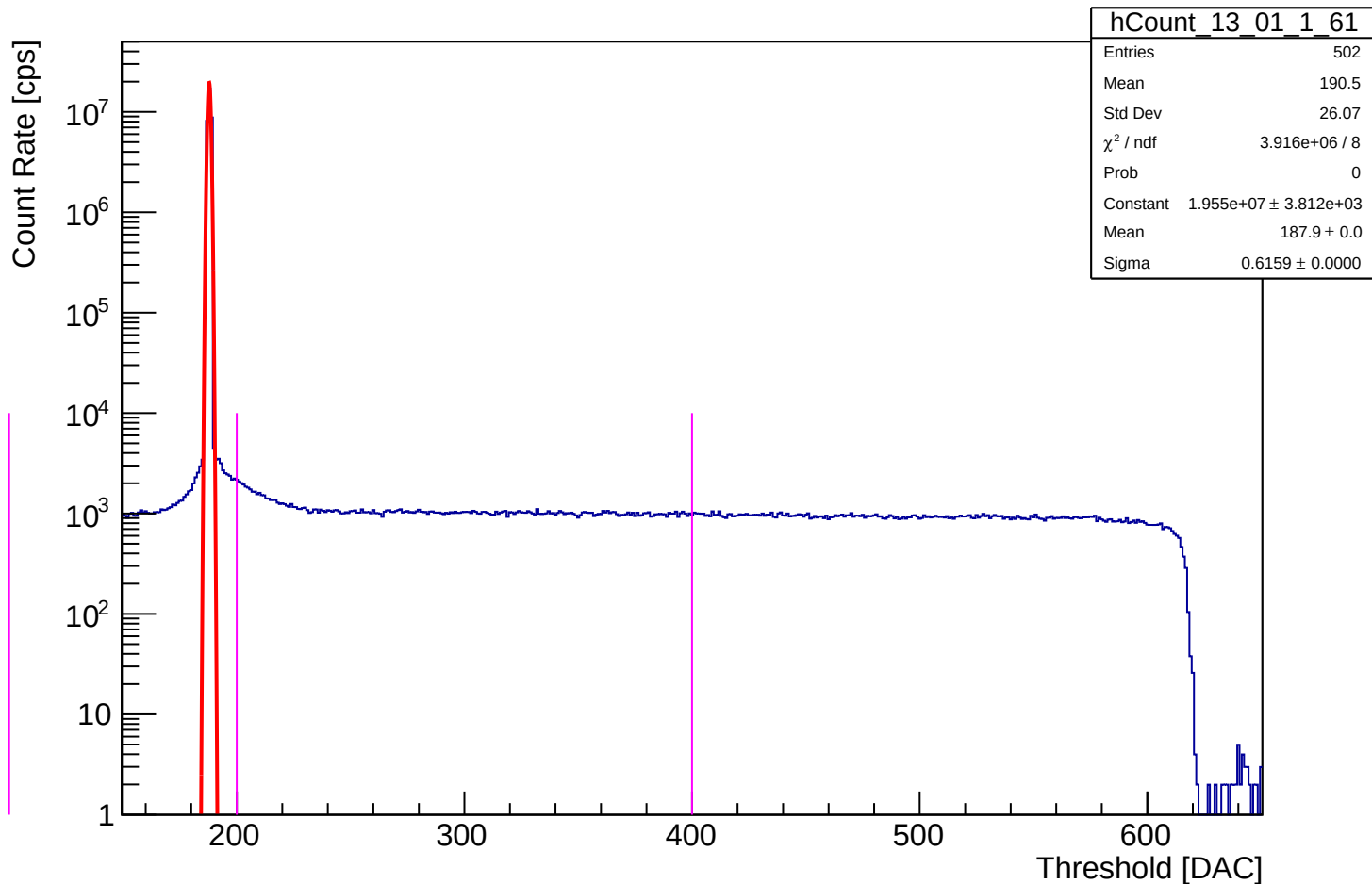


Row 1 Tile 1 Pmt 5 Pixel 61 Slot 13 Fiber 1 Asic 1 Channel 60

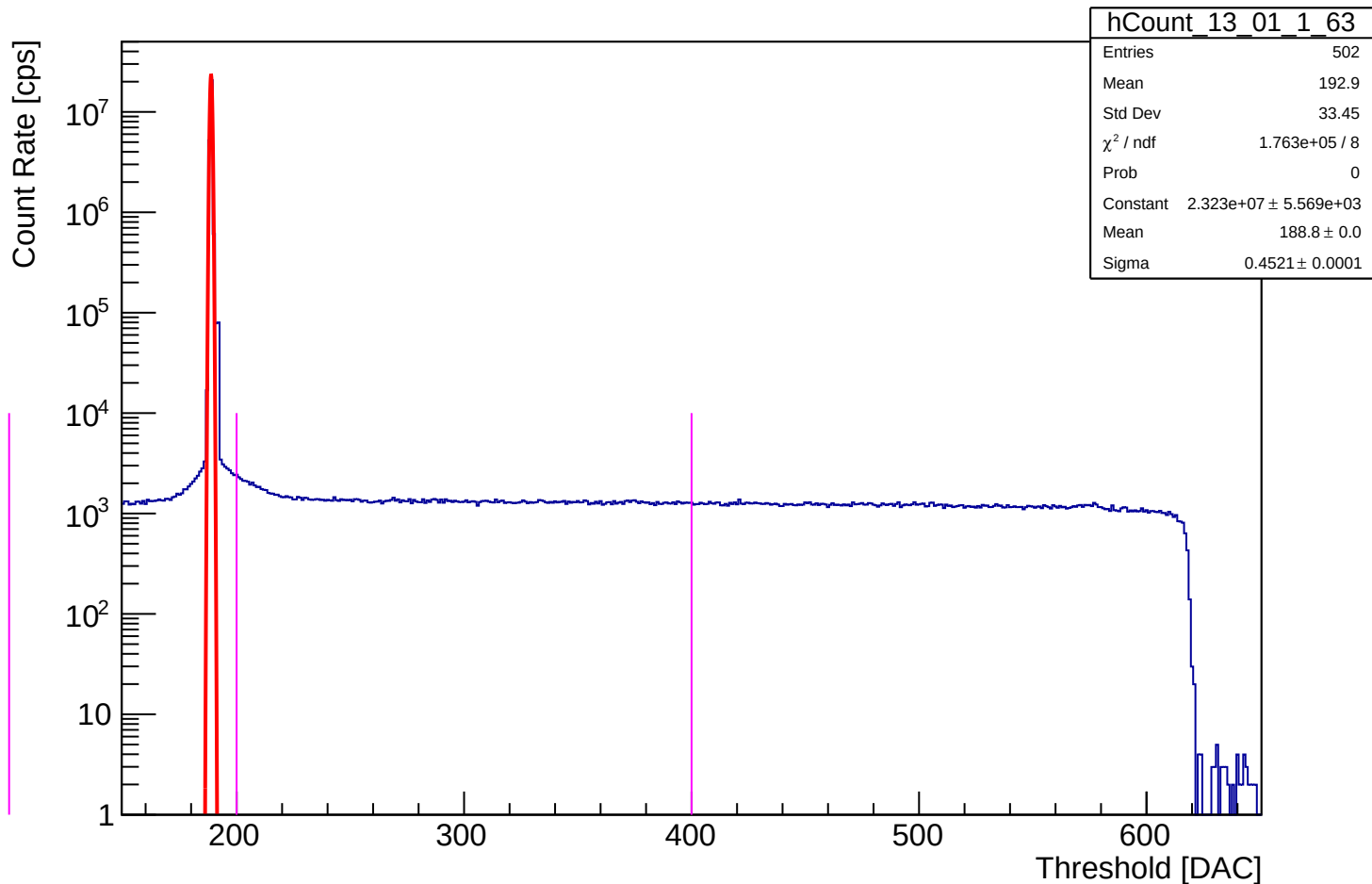


Row 1 Tile 1 Pmt 5 Pixel 62 Slot 13 Fiber 1 Asic 1 Channel 62

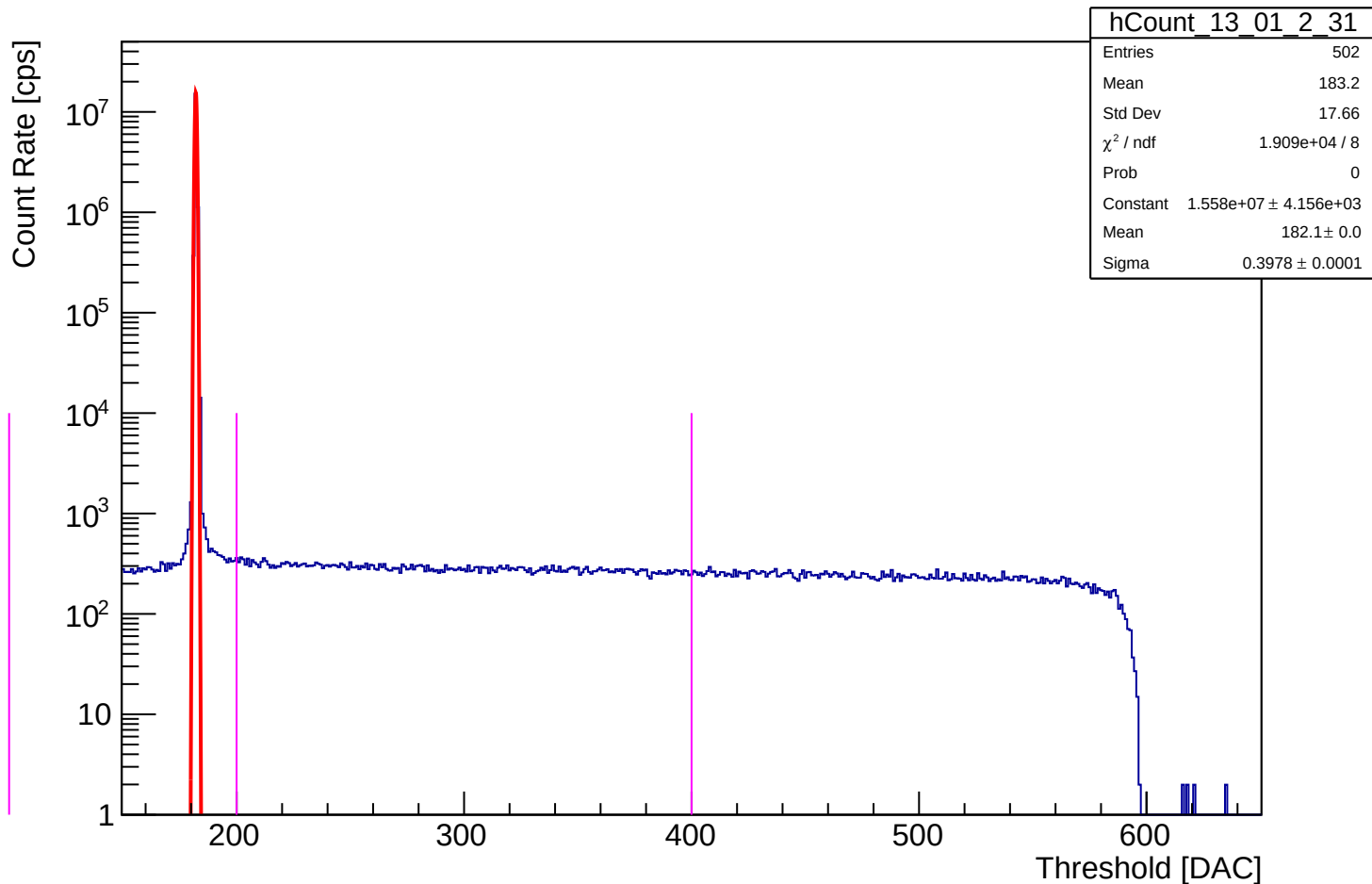




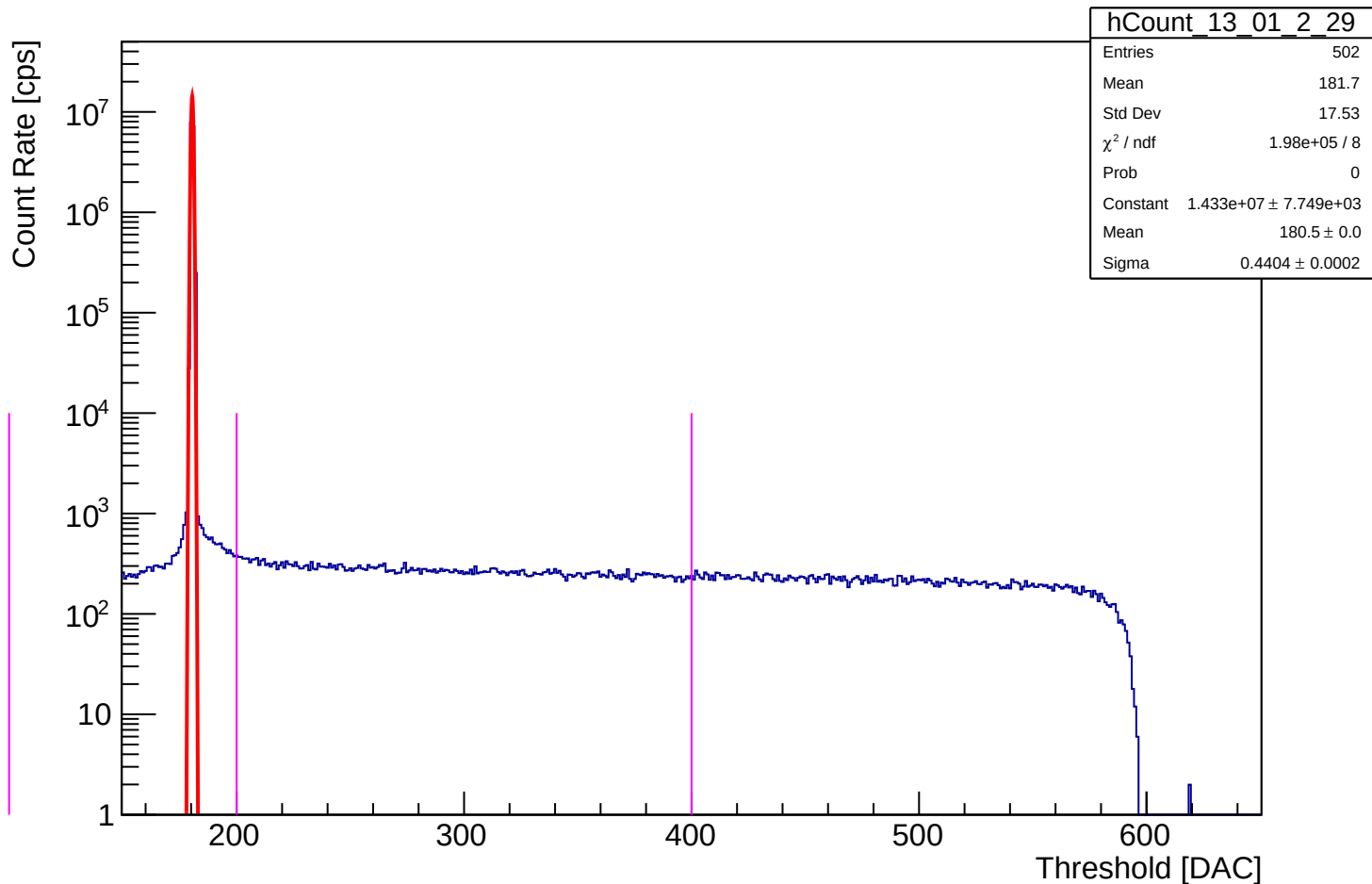
Row 1 Tile 1 Pmt 5 Pixel 64 Slot 13 Fiber 1 Asic 1 Channel 63



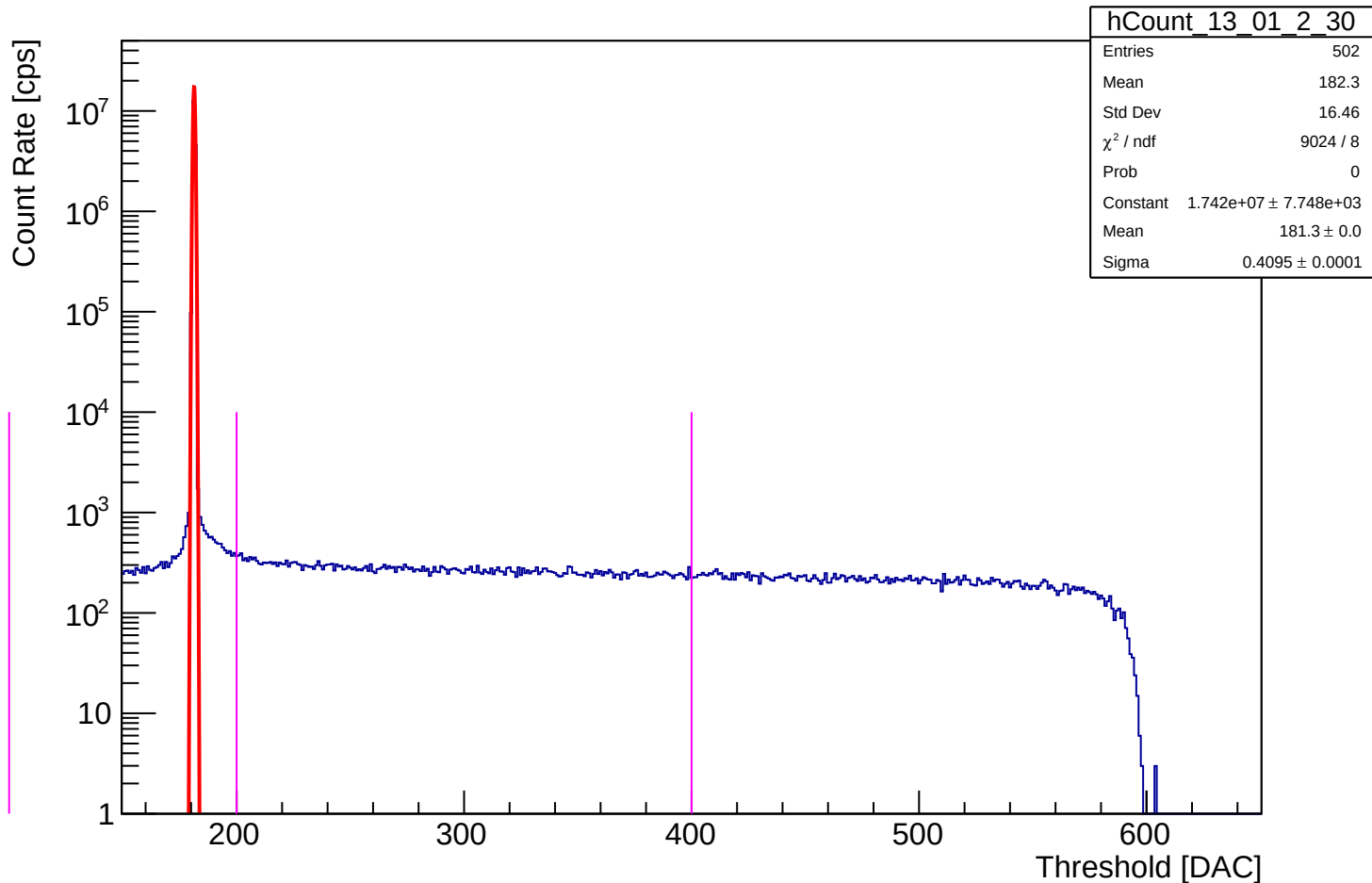
Row 1 Tile 1 Pmt 6 Pixel 1 Slot 13 Fiber 1 Asic 2 Channel 31



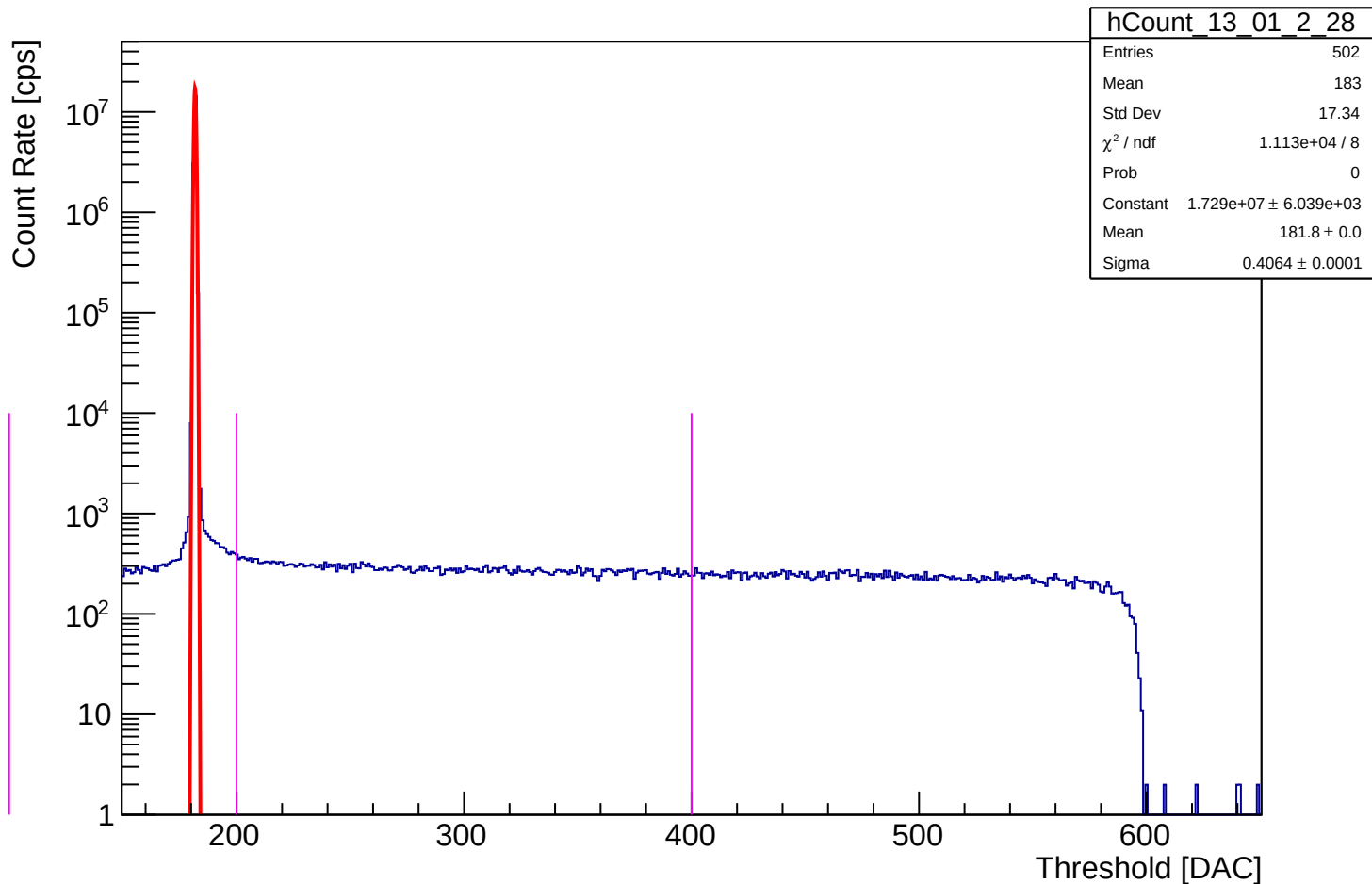
Row 1 Tile 1 Pmt 6 Pixel 2 Slot 13 Fiber 1 Asic 2 Channel 29



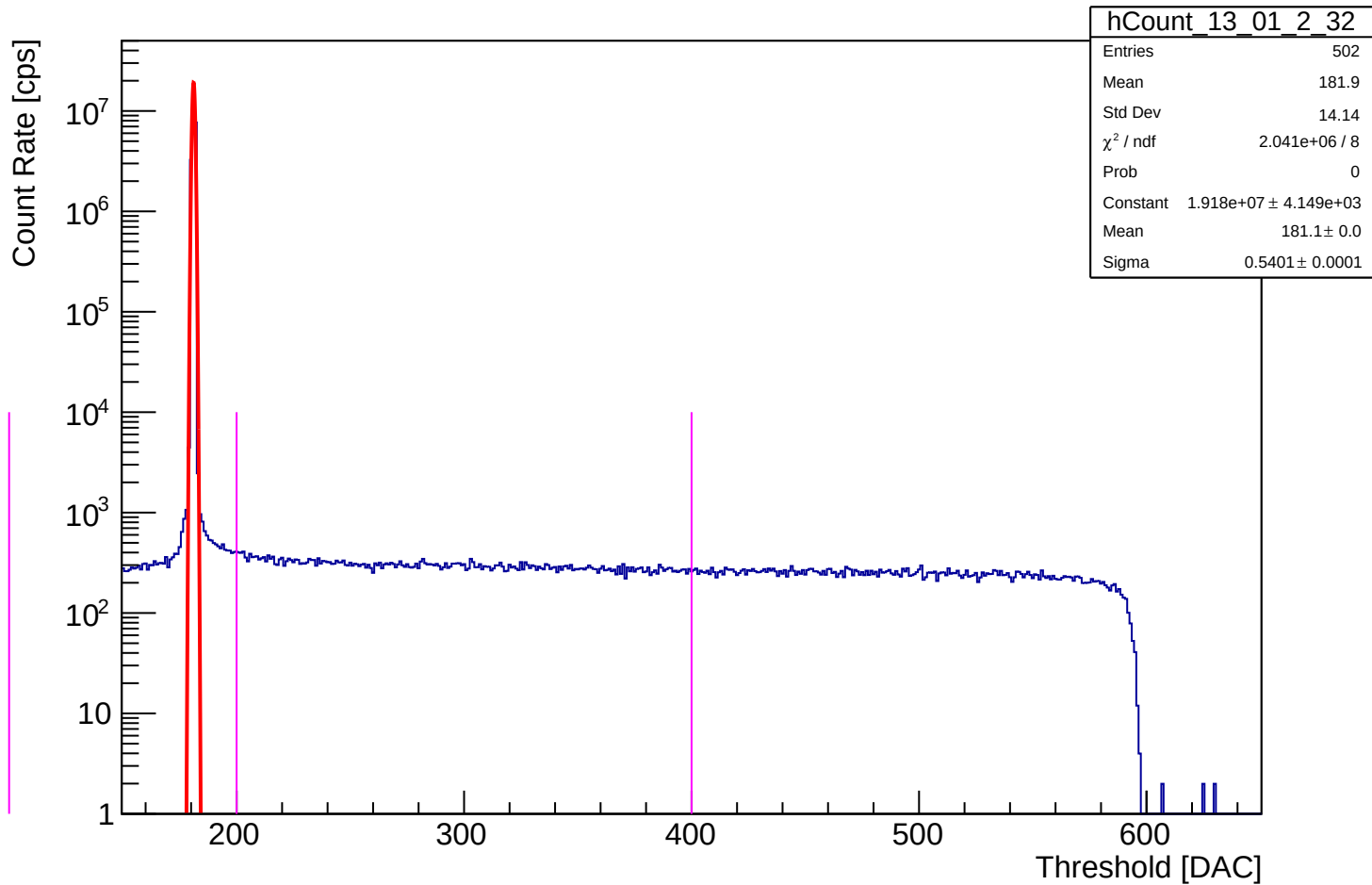
Row 1 Tile 1 Pmt 6 Pixel 3 Slot 13 Fiber 1 Asic 2 Channel 30



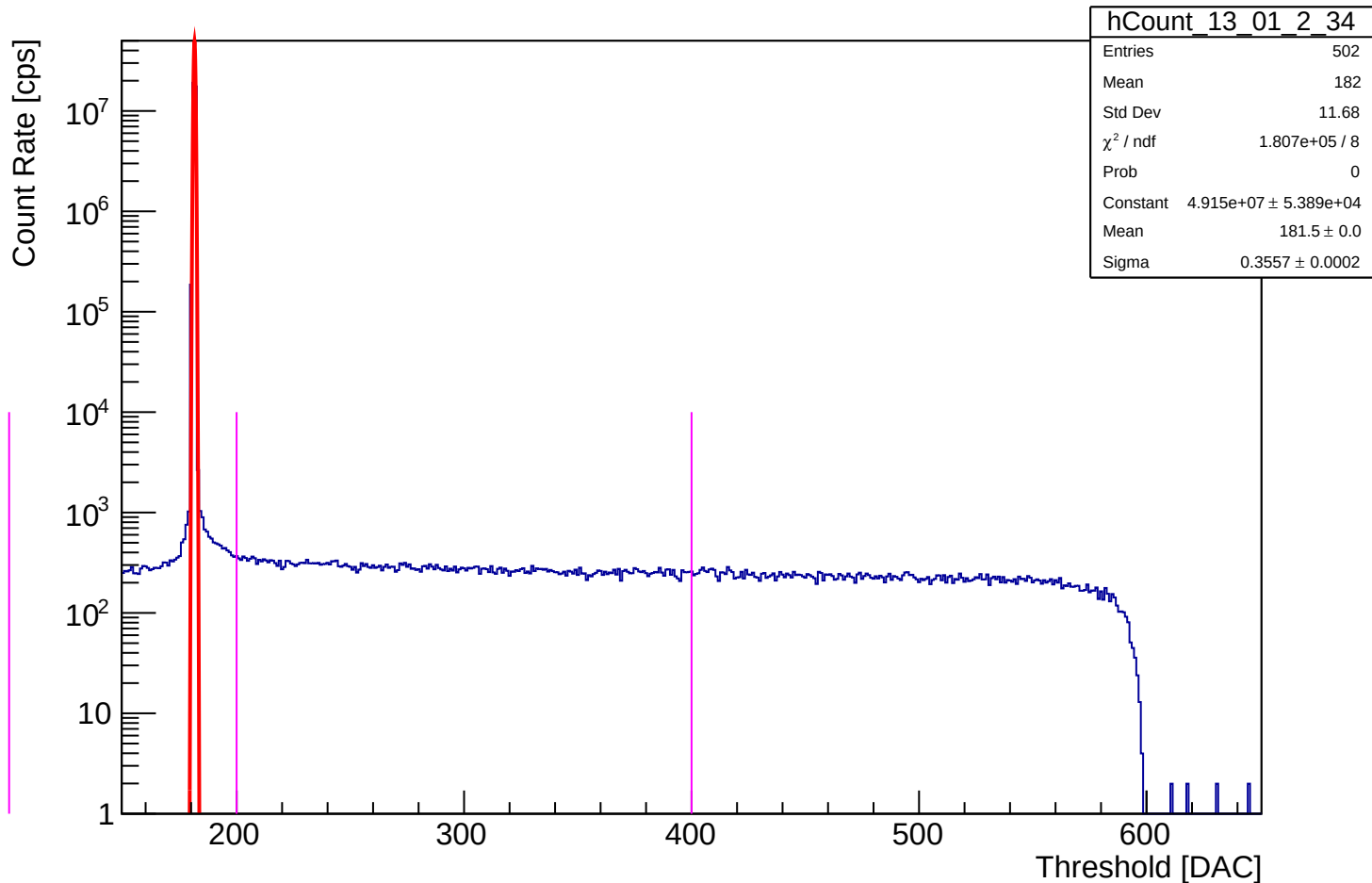
Row 1 Tile 1 Pmt 6 Pixel 4 Slot 13 Fiber 1 Asic 2 Channel 28



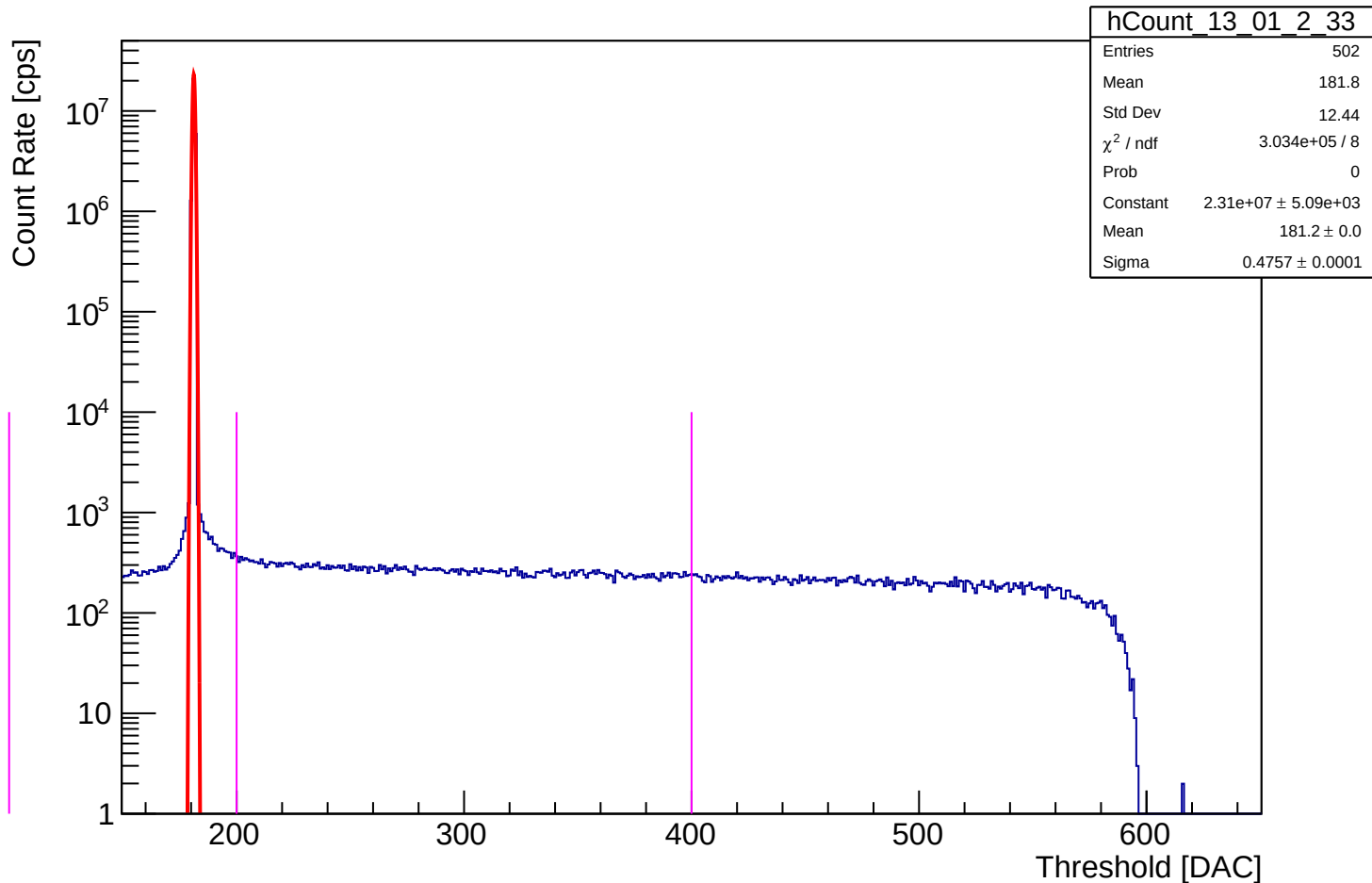
Row 1 Tile 1 Pmt 6 Pixel 5 Slot 13 Fiber 1 Asic 2 Channel 32

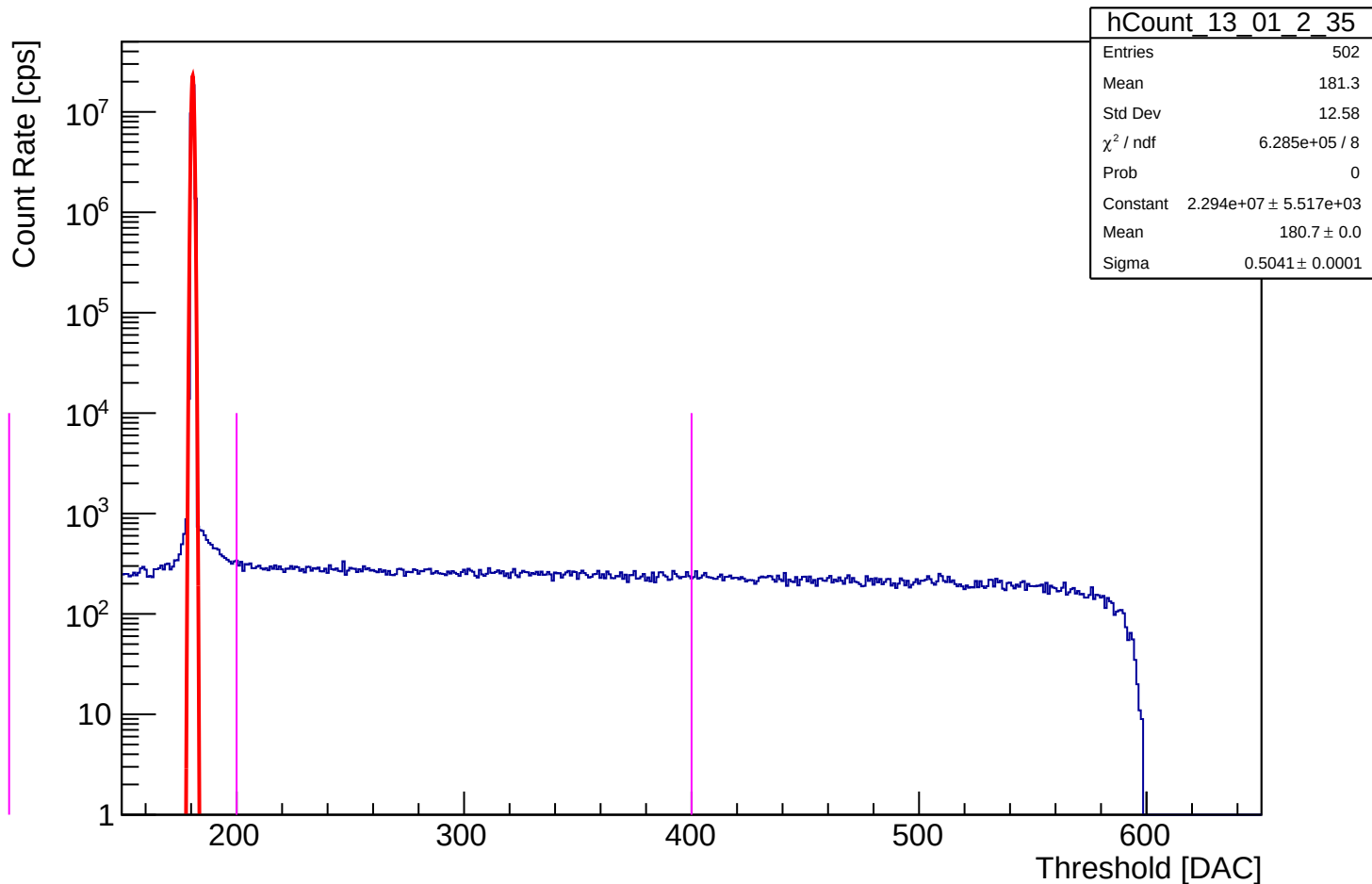


Row 1 Tile 1 Pmt 6 Pixel 6 Slot 13 Fiber 1 Asic 2 Channel 34

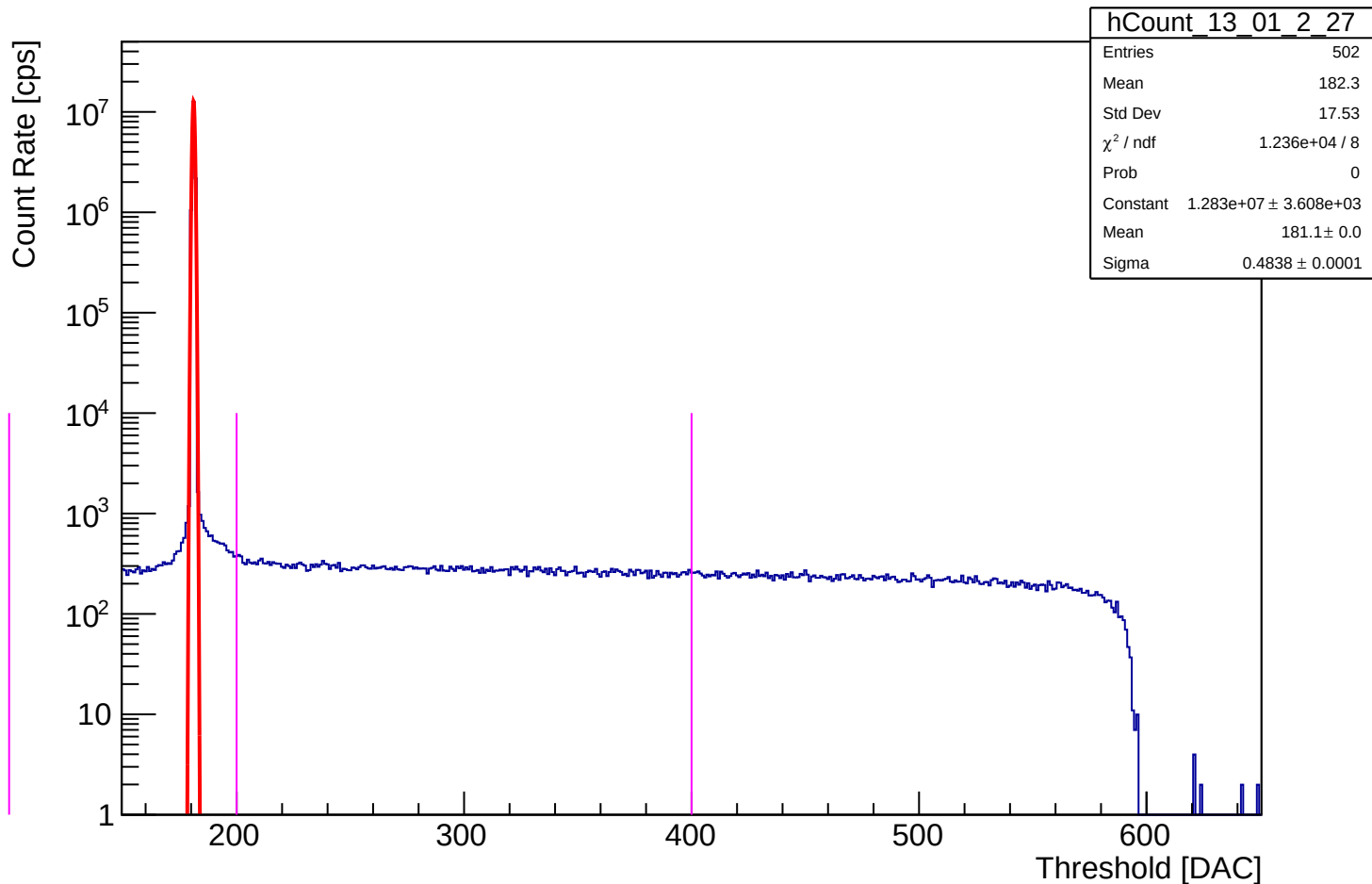


Row 1 Tile 1 Pmt 6 Pixel 7 Slot 13 Fiber 1 Asic 2 Channel 33

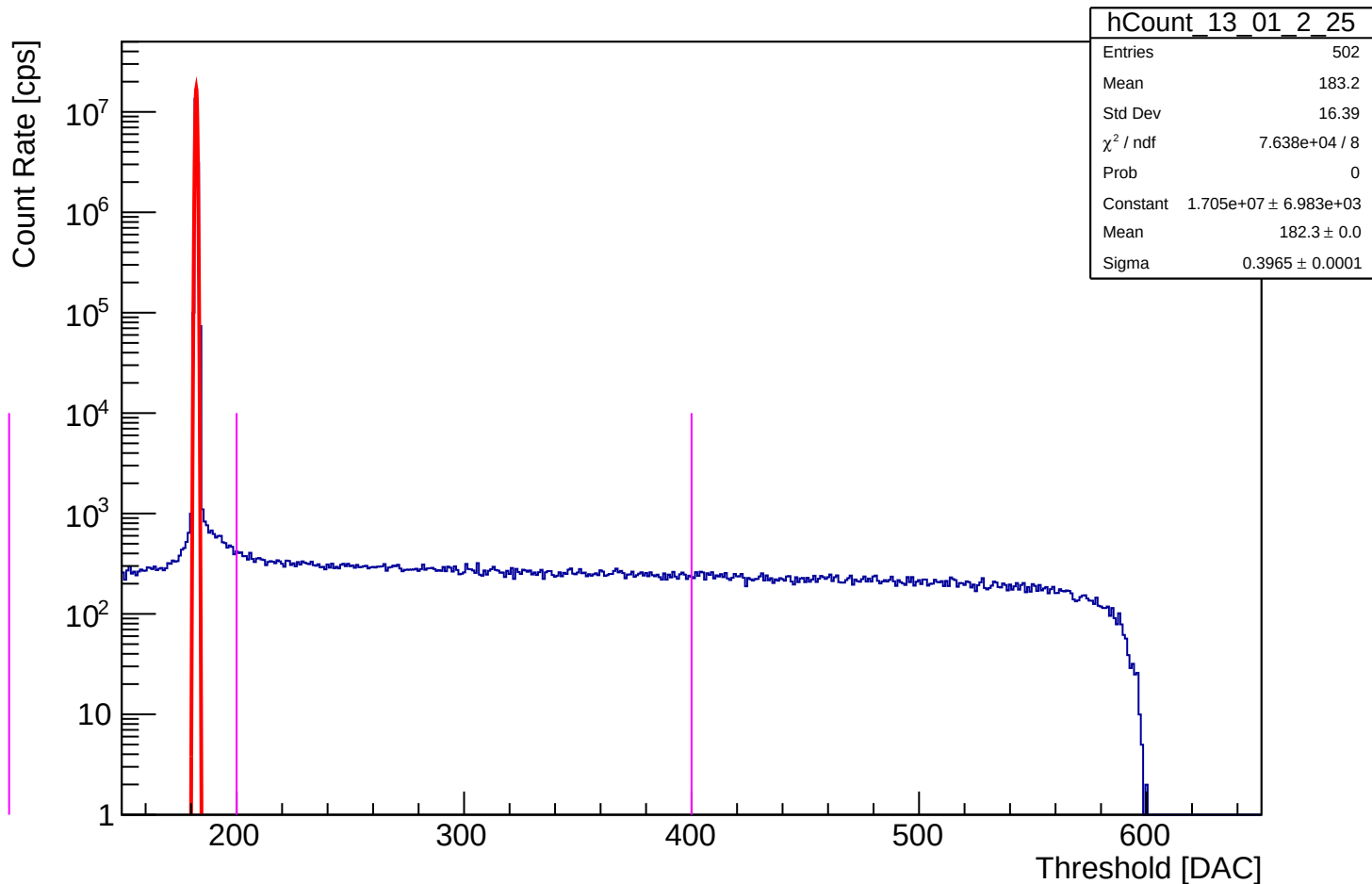




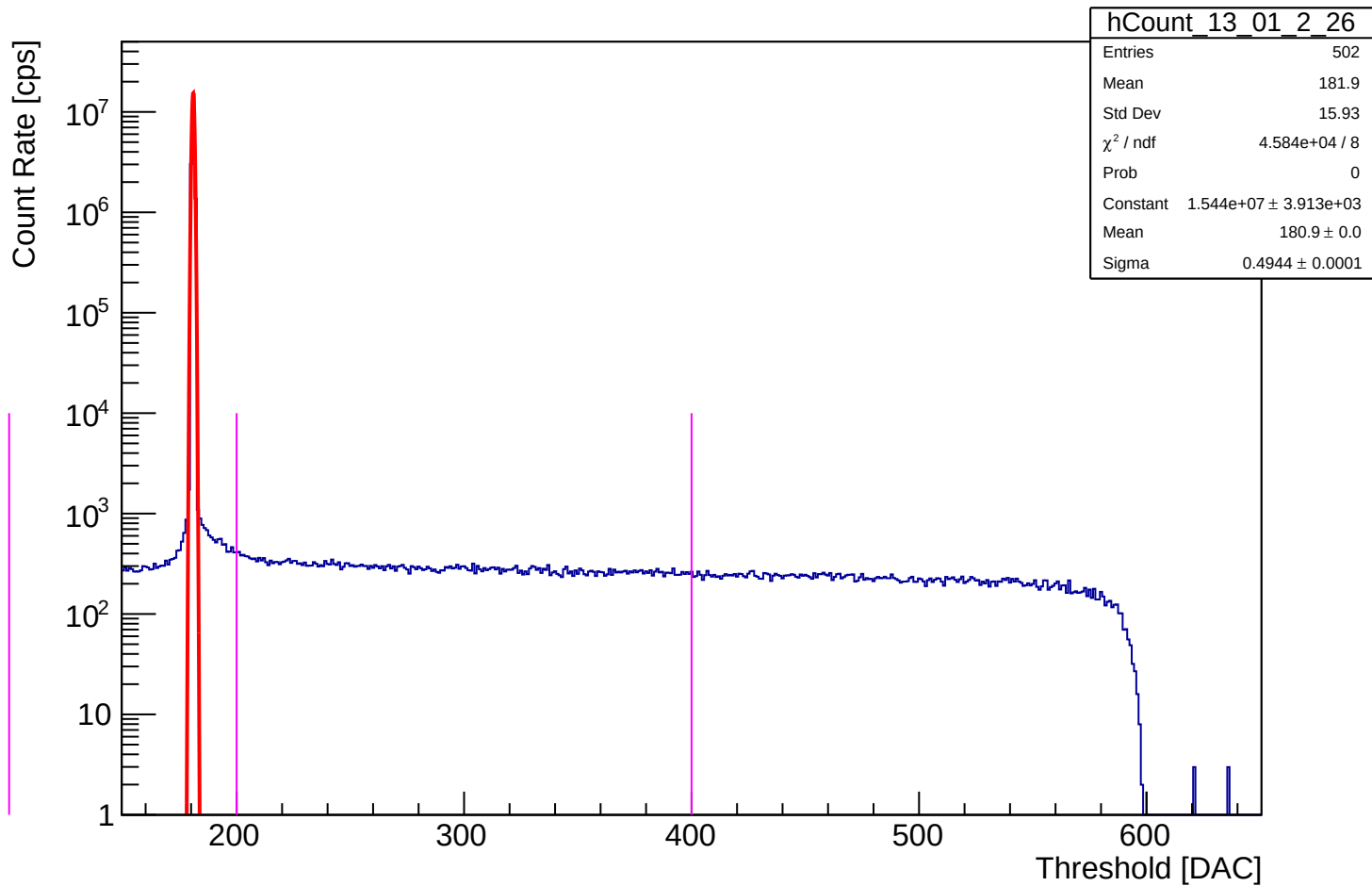
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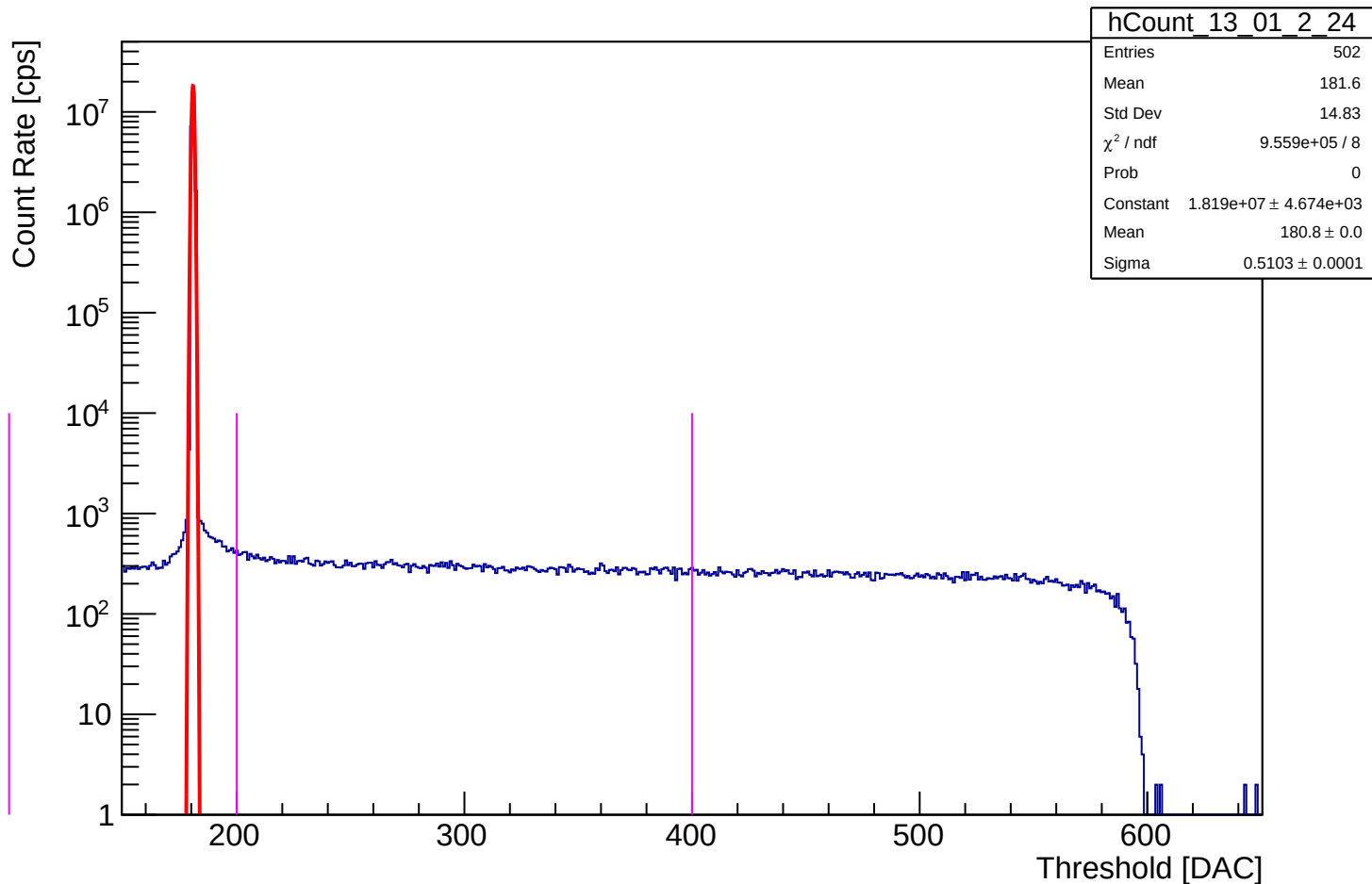
Row 1 Tile 1 Pmt 6 Pixel 10 Slot 13 Fiber 1 Asic 2 Channel 25



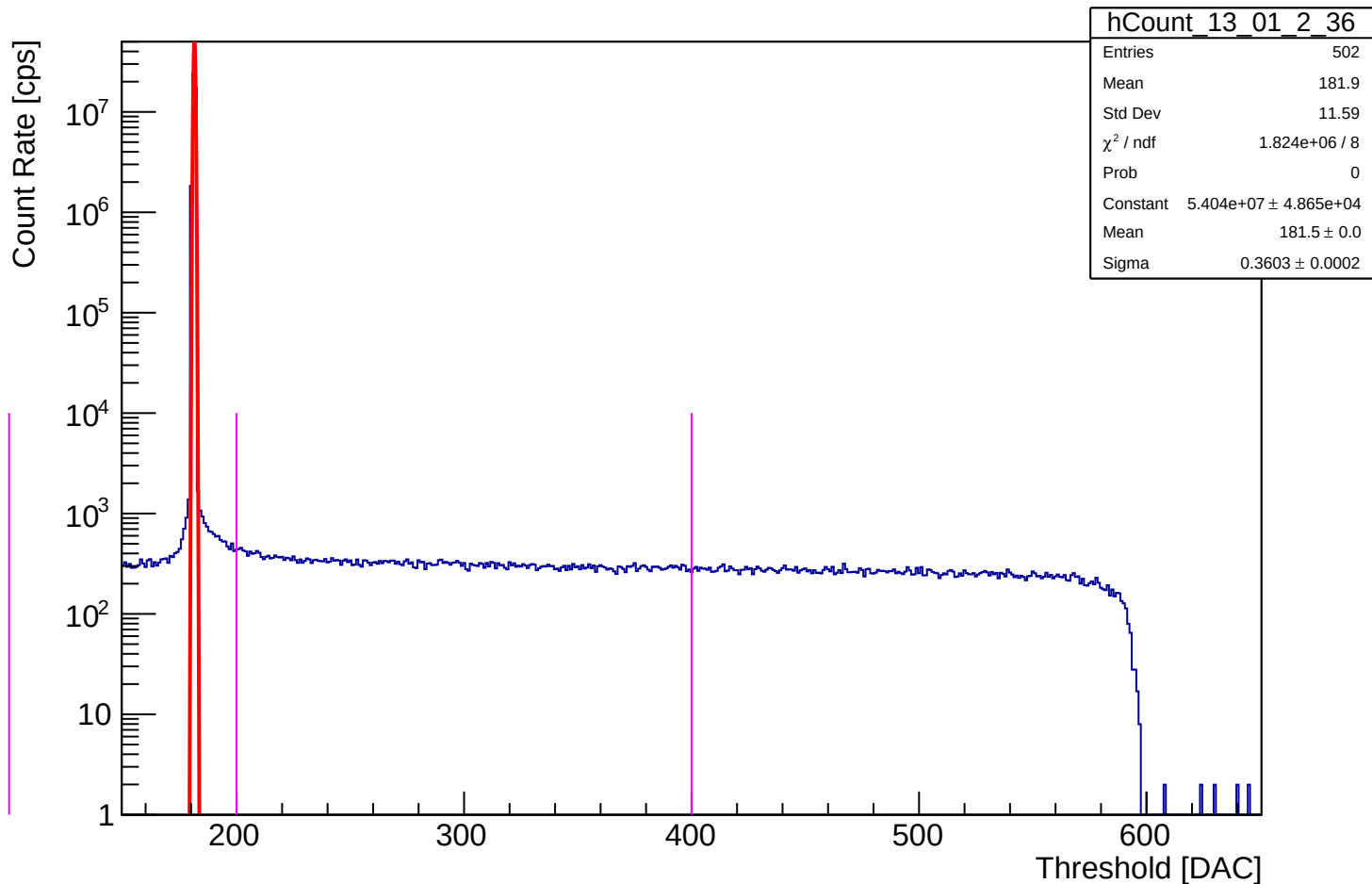
Row 1 Tile 1 Pmt 6 Pixel 11 Slot 13 Fiber 1 Asic 2 Channel 26



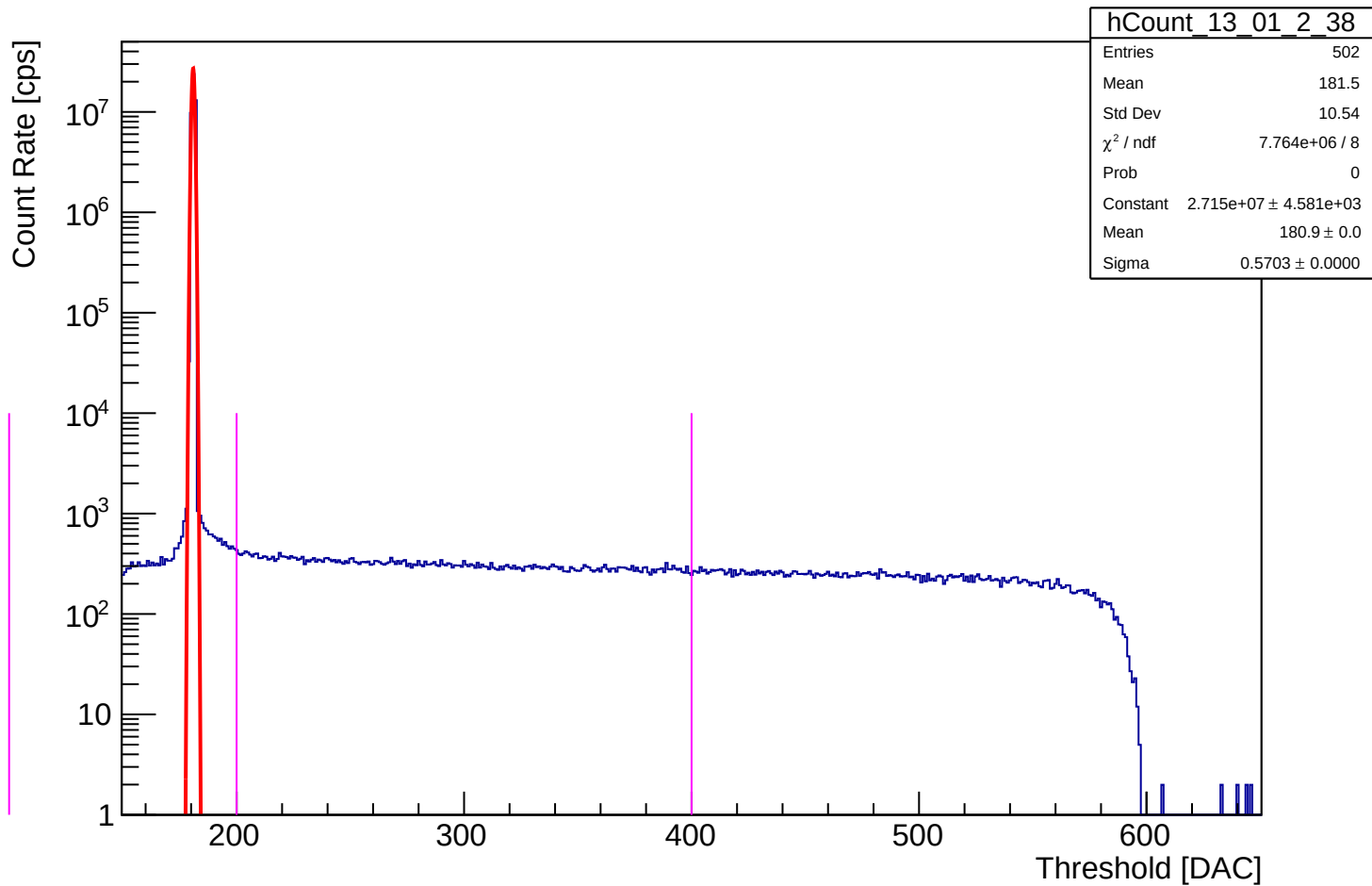
Row 1 Tile 1 Pmt 6 Pixel 12 Slot 13 Fiber 1 Asic 2 Channel 24



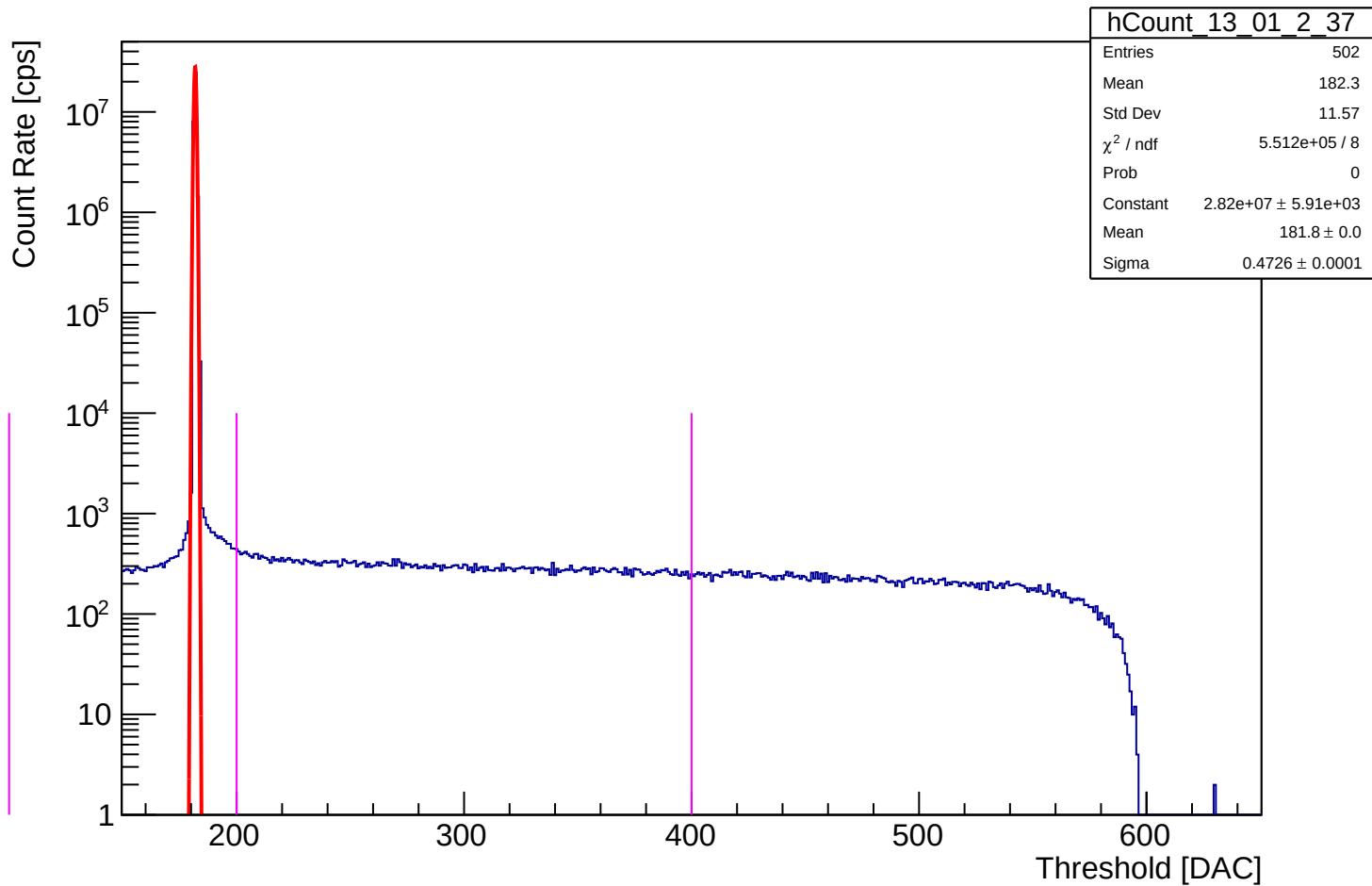
Row 1 Tile 1 Pmt 6 Pixel 13 Slot 13 Fiber 1 Asic 2 Channel 36



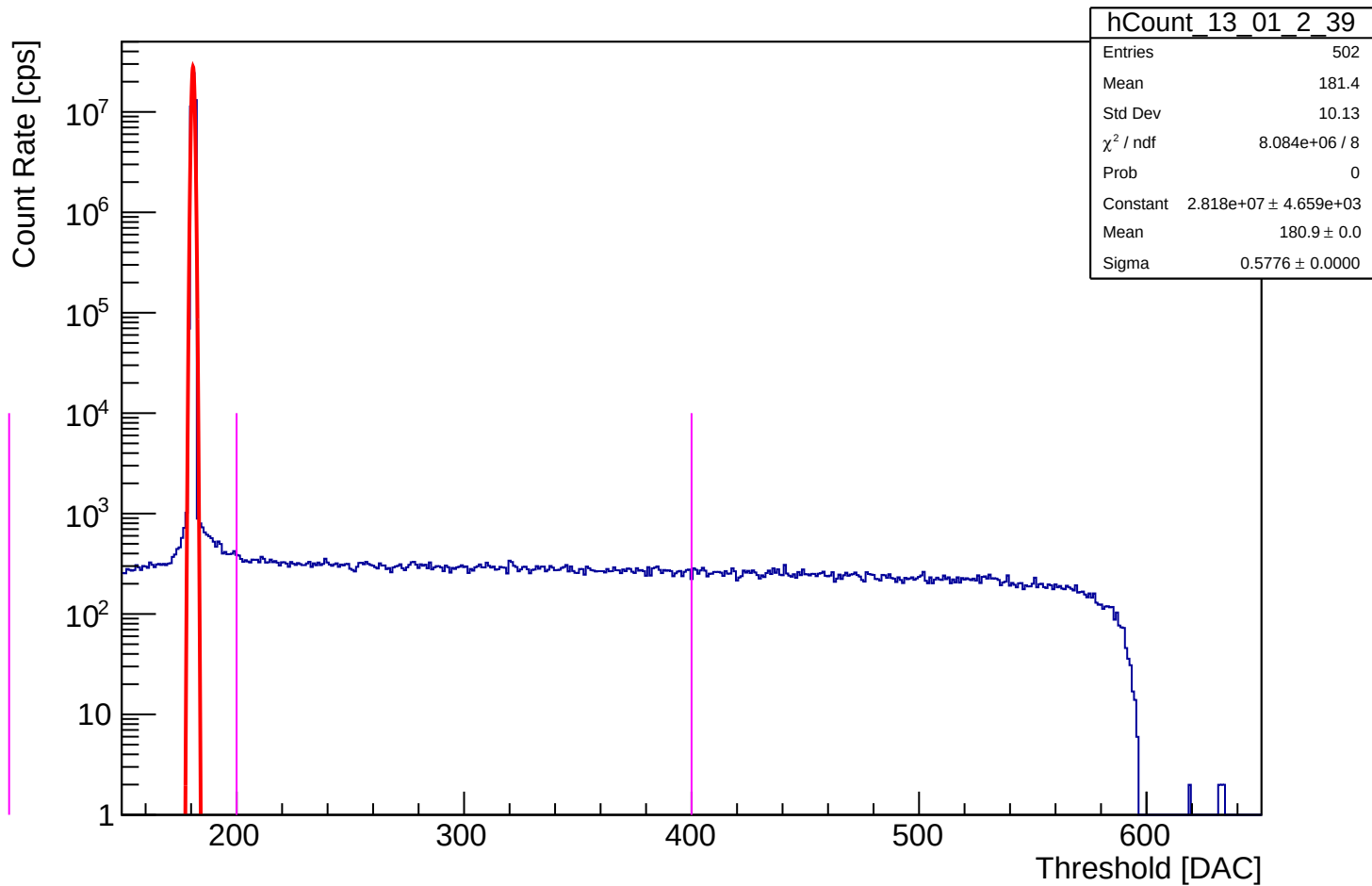
Row 1 Tile 1 Pmt 6 Pixel 14 Slot 13 Fiber 1 Asic 2 Channel 38



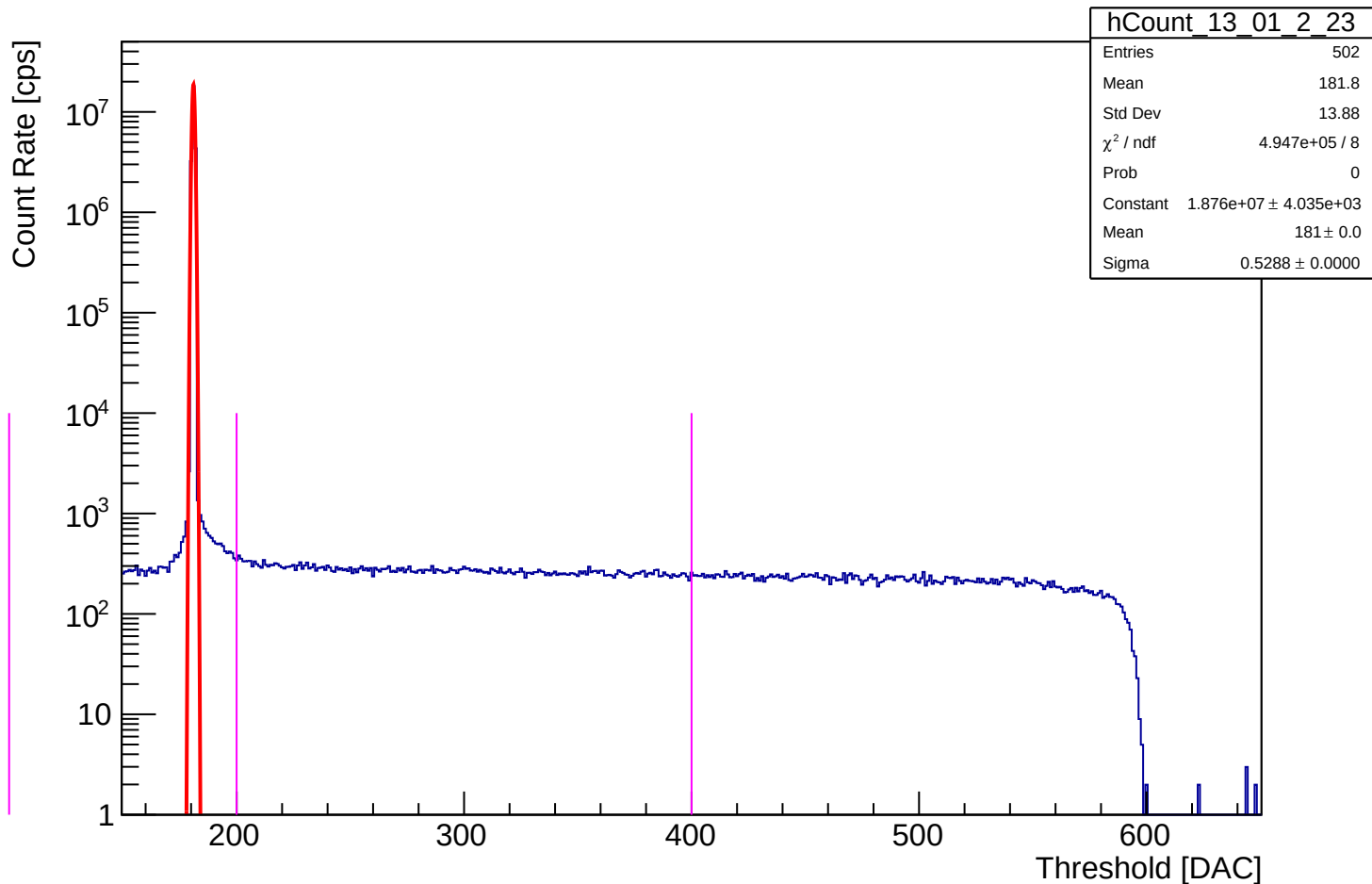
Row 1 Tile 1 Pmt 6 Pixel 15 Slot 13 Fiber 1 Asic 2 Channel 37



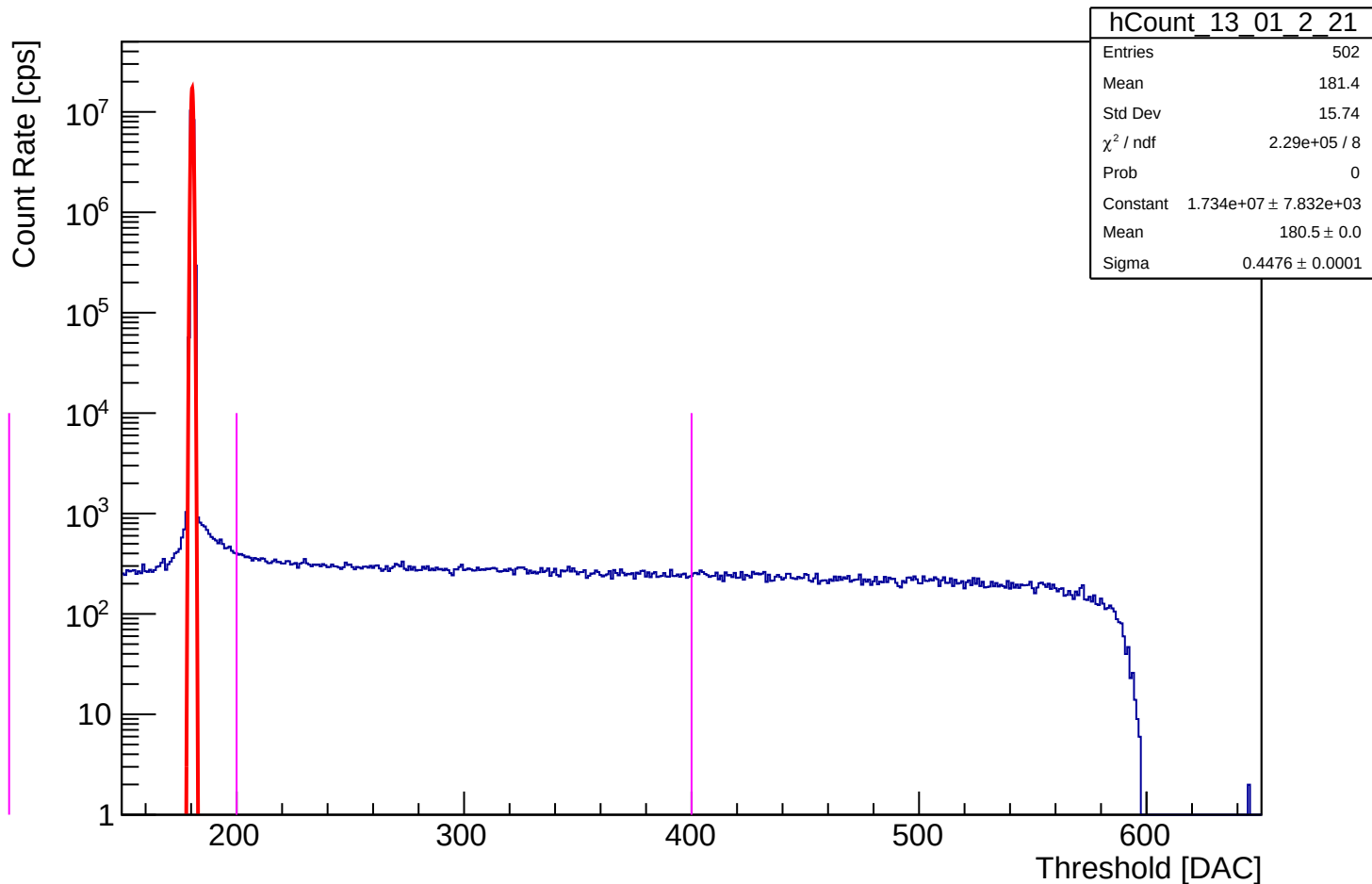
Row 1 Tile 1 Pmt 6 Pixel 16 Slot 13 Fiber 1 Asic 2 Channel 39



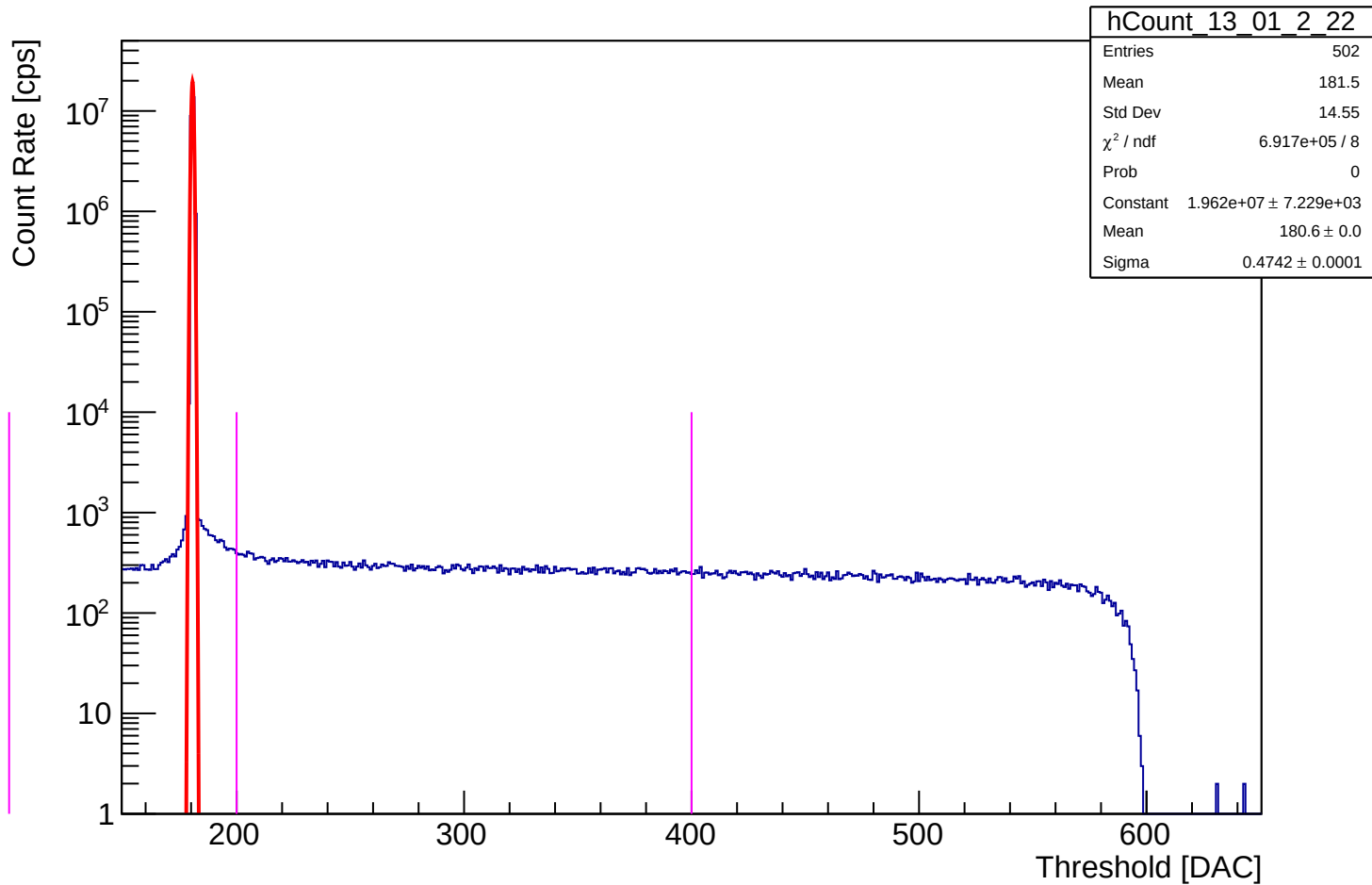
Row 1 Tile 1 Pmt 6 Pixel 17 Slot 13 Fiber 1 Asic 2 Channel 23



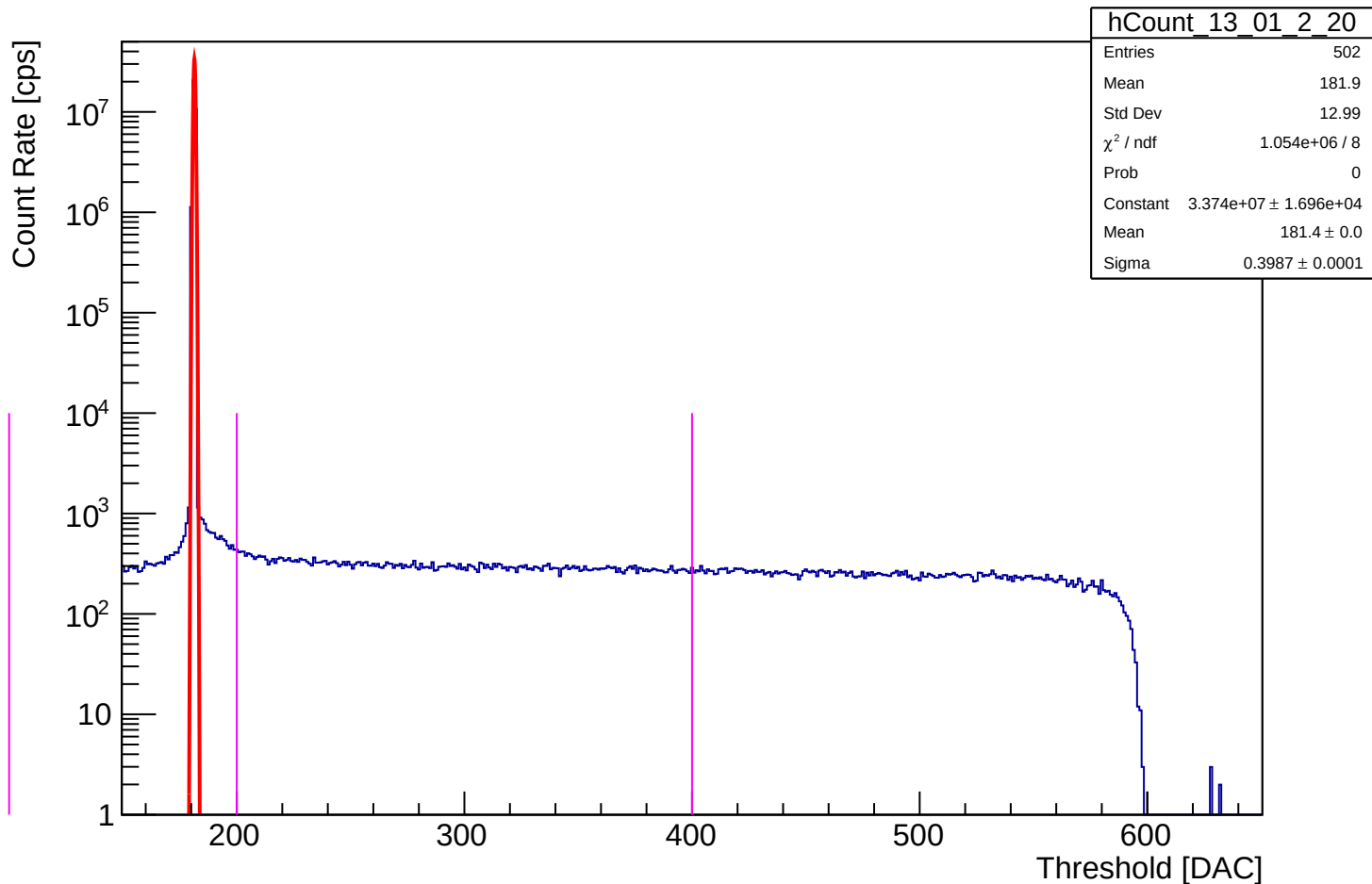
Row 1 Tile 1 Pmt 6 Pixel 18 Slot 13 Fiber 1 Asic 2 Channel 21



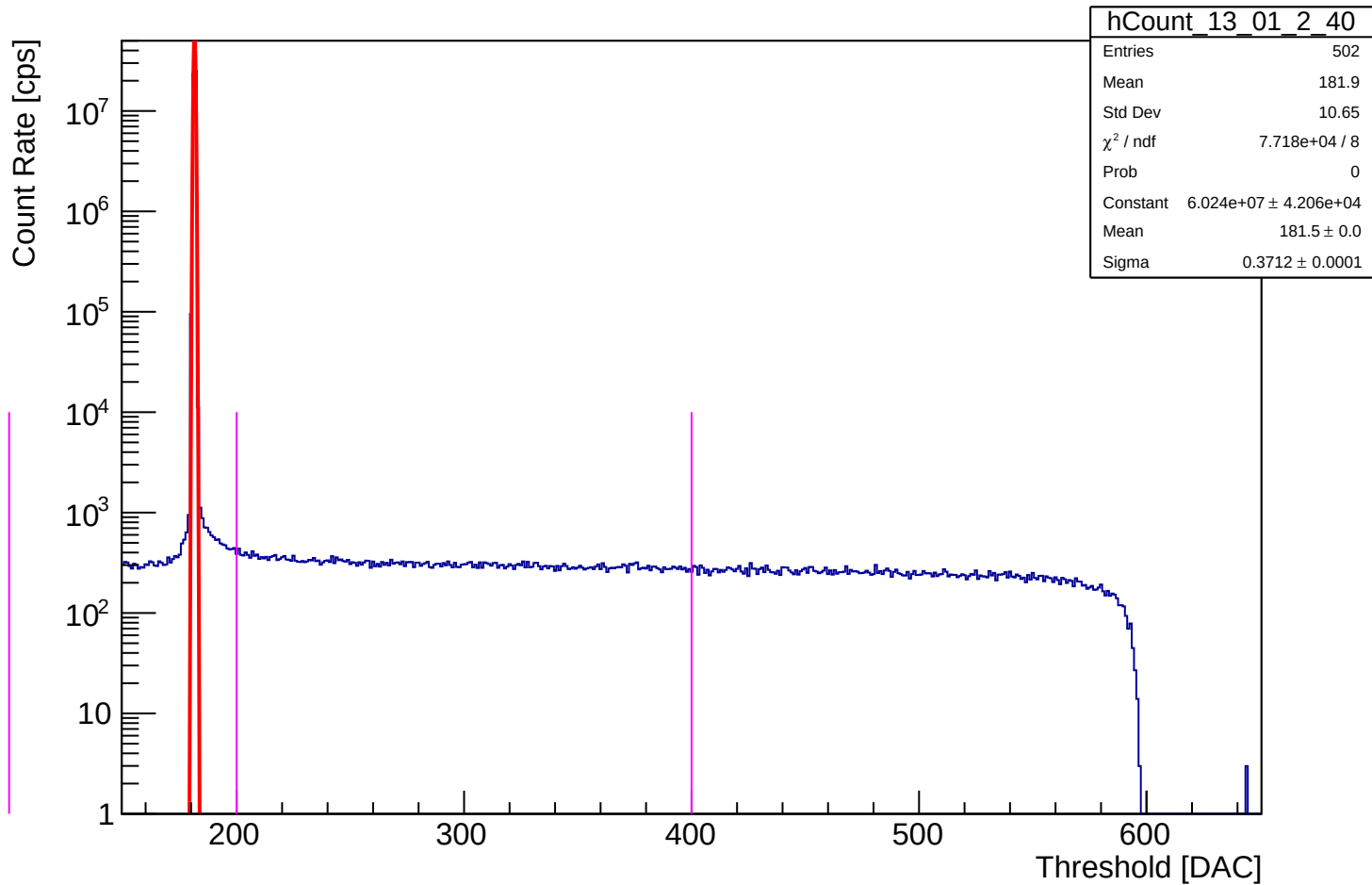
Row 1 Tile 1 Pmt 6 Pixel 19 Slot 13 Fiber 1 Asic 2 Channel 22



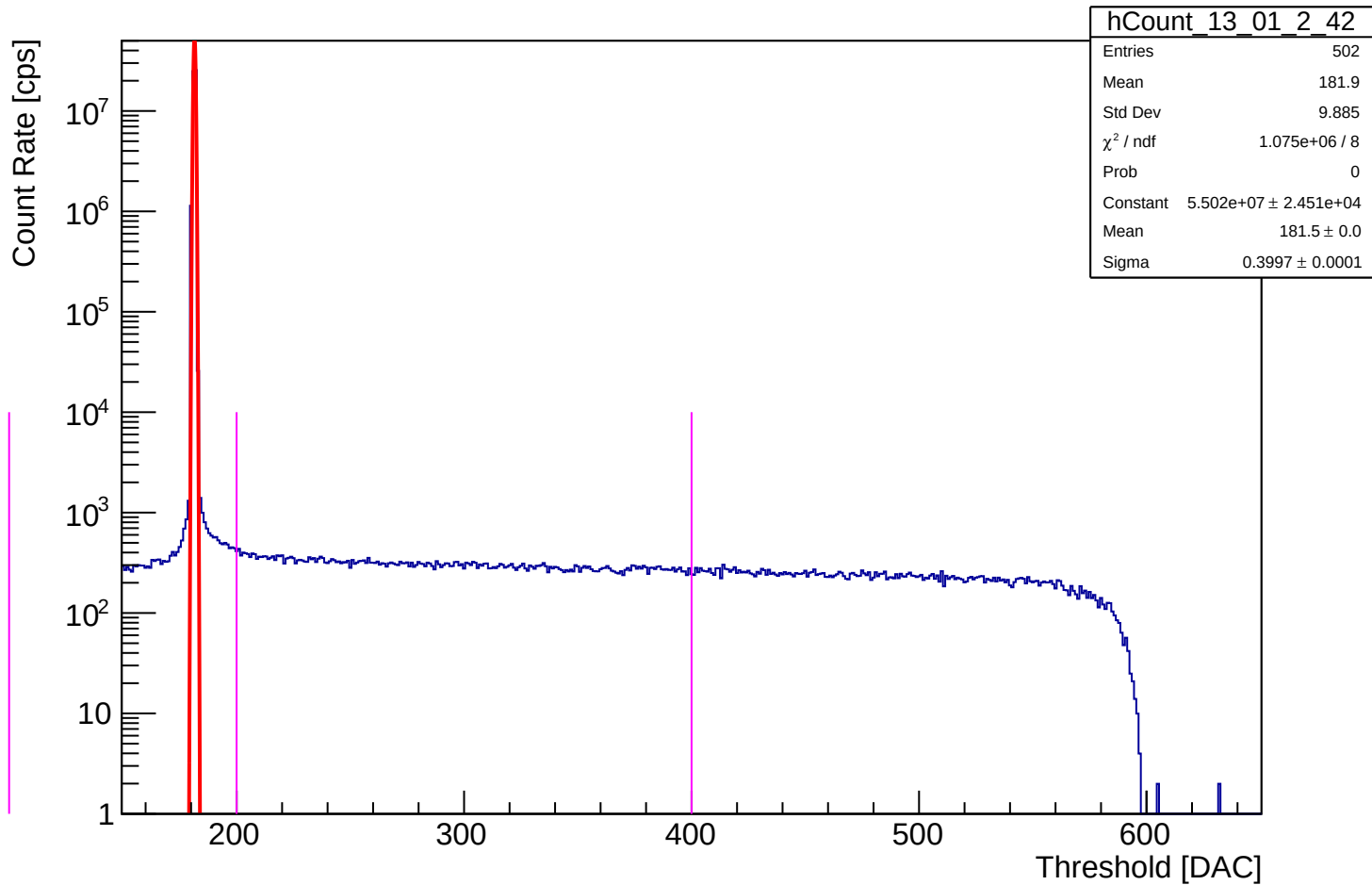
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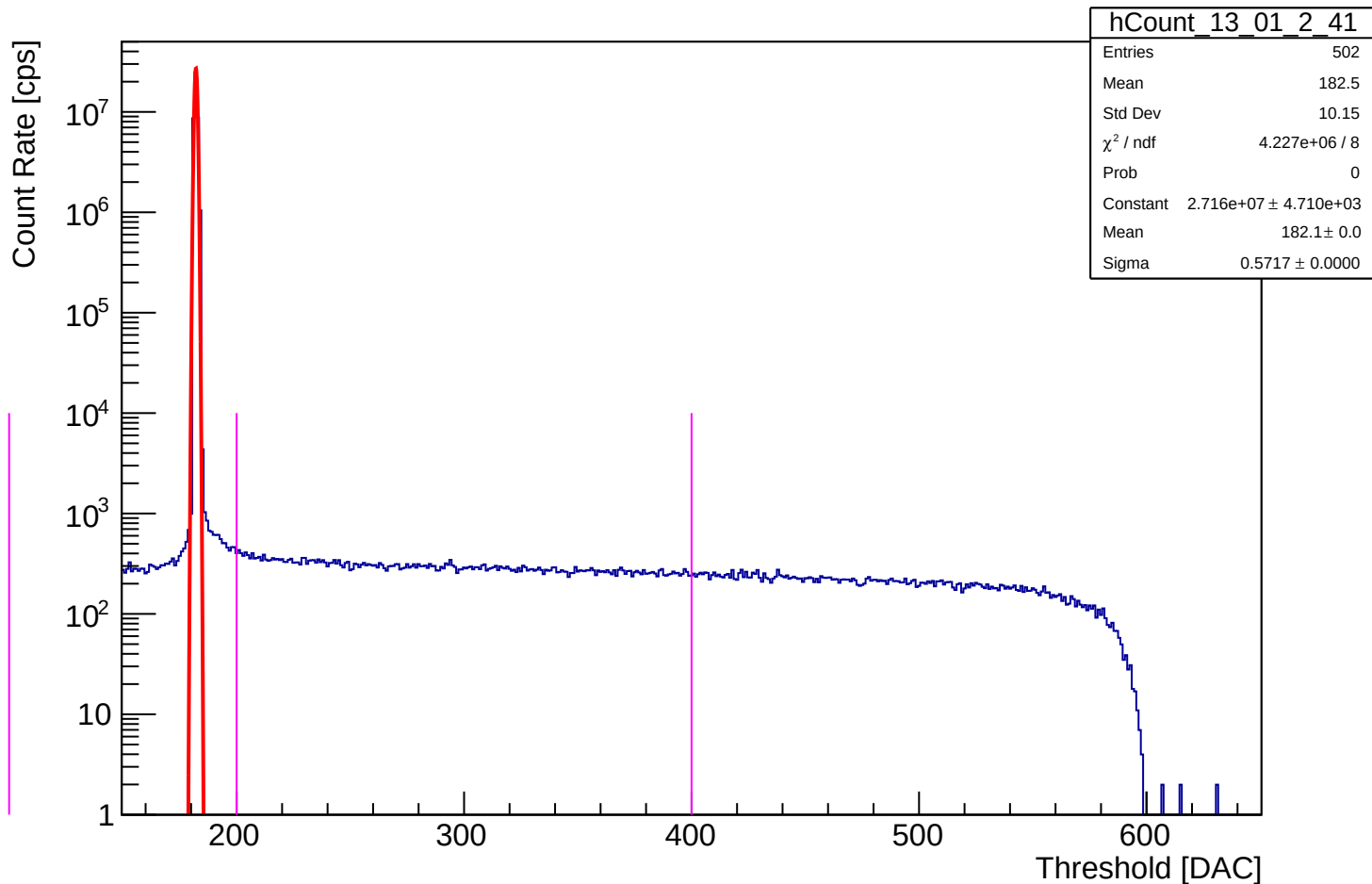
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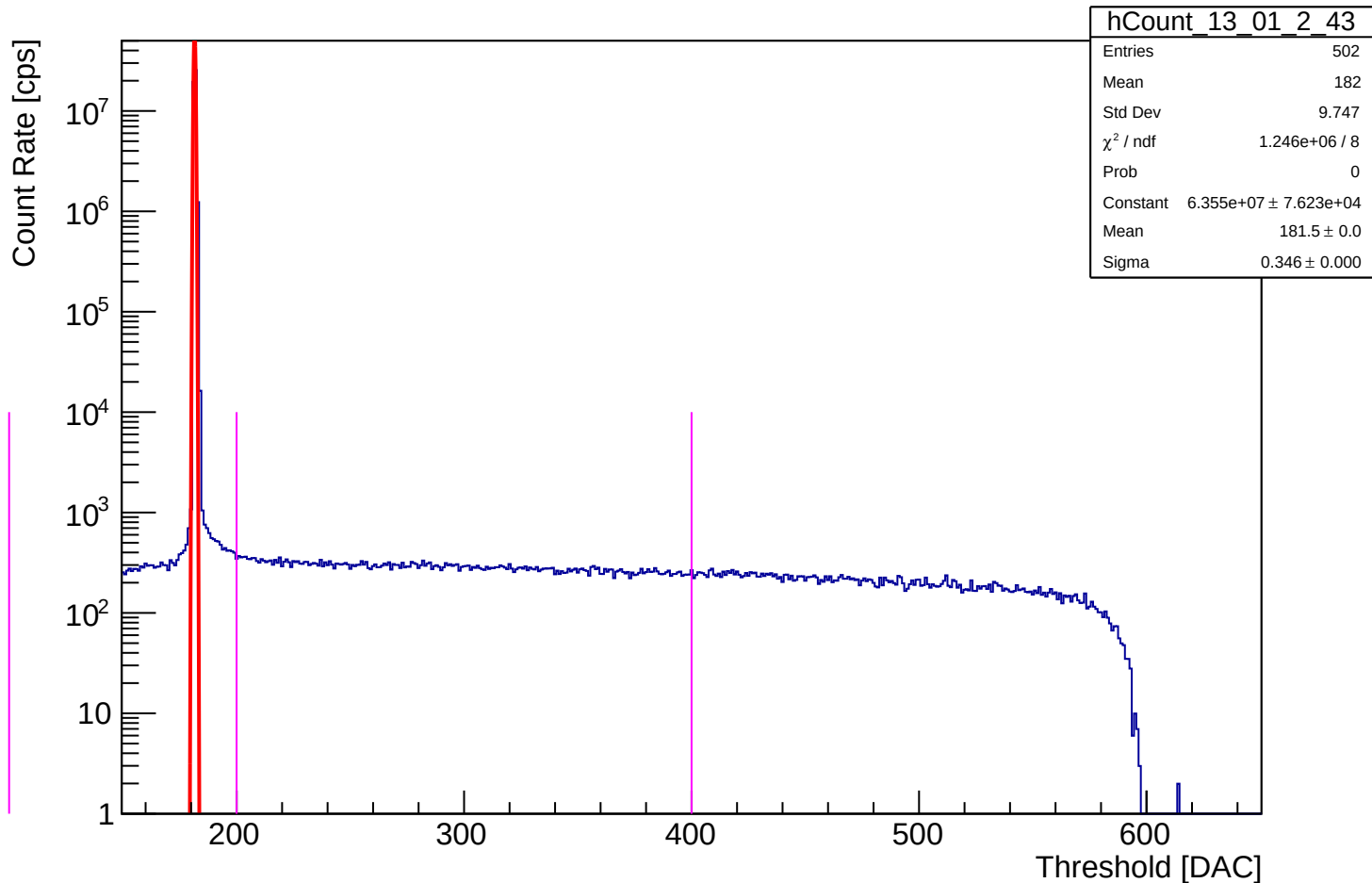
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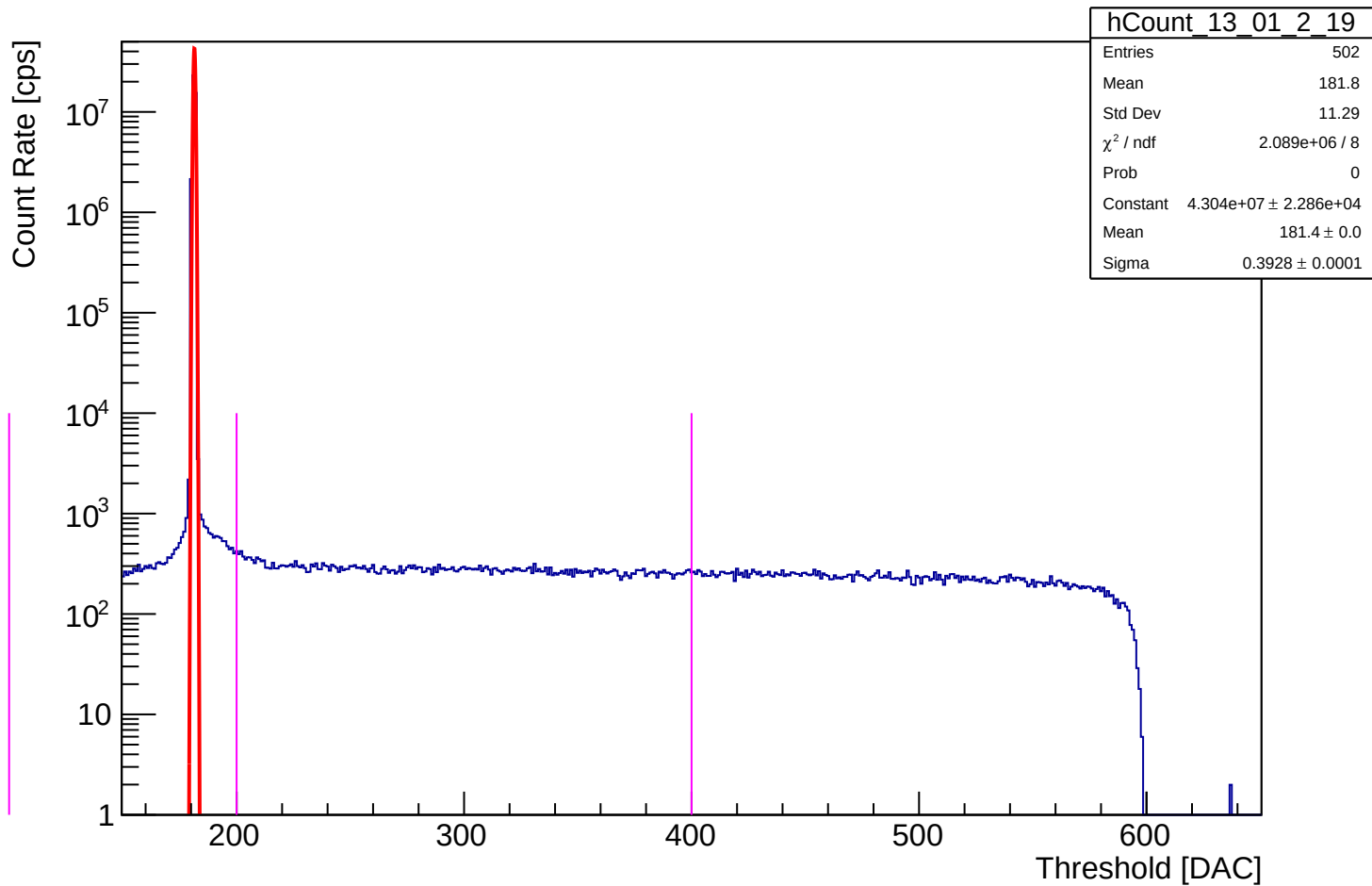
Row 1 Tile 1 Pmt 6 Pixel 23 Slot 13 Fiber 1 Asic 2 Channel 41



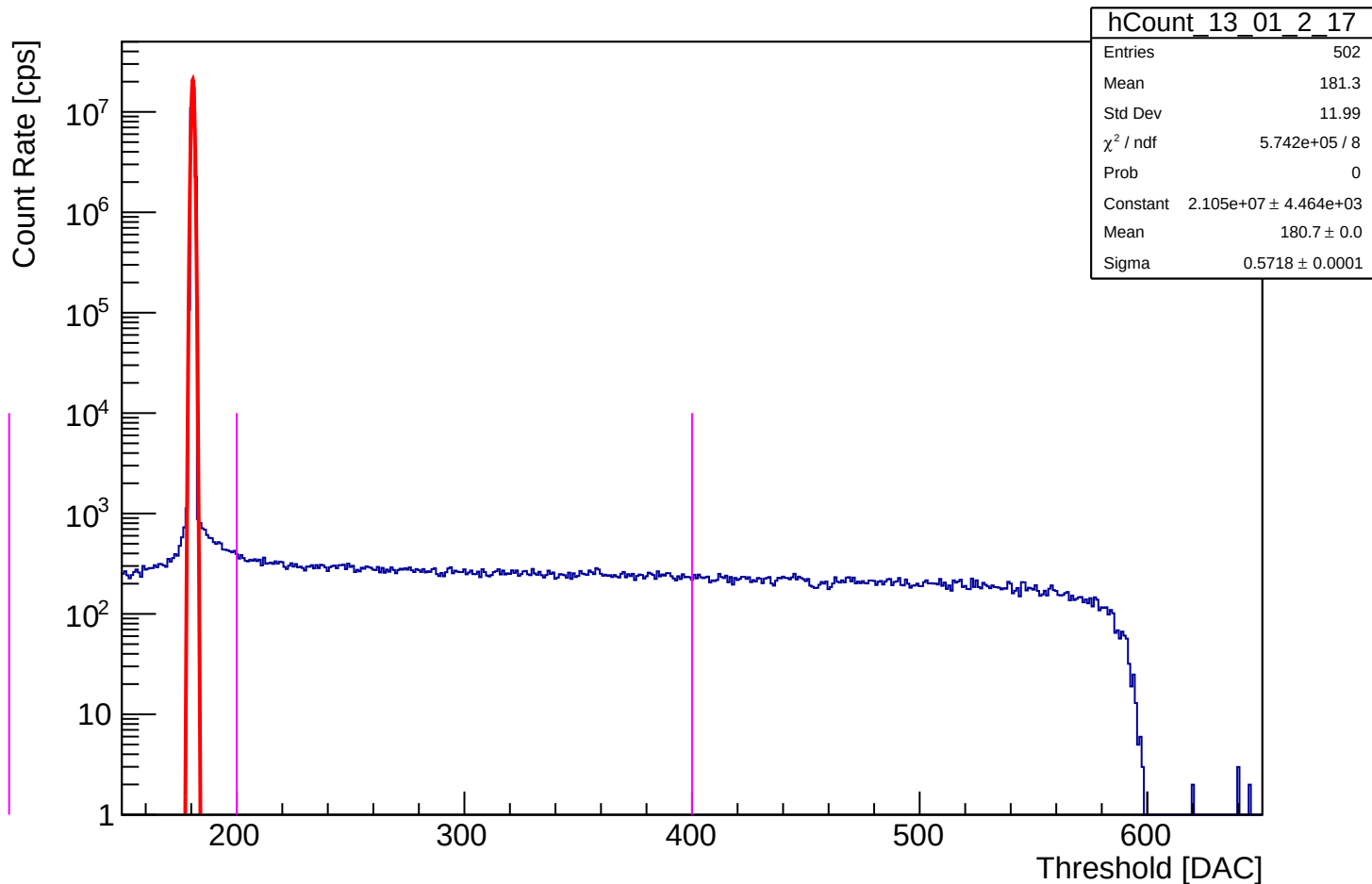
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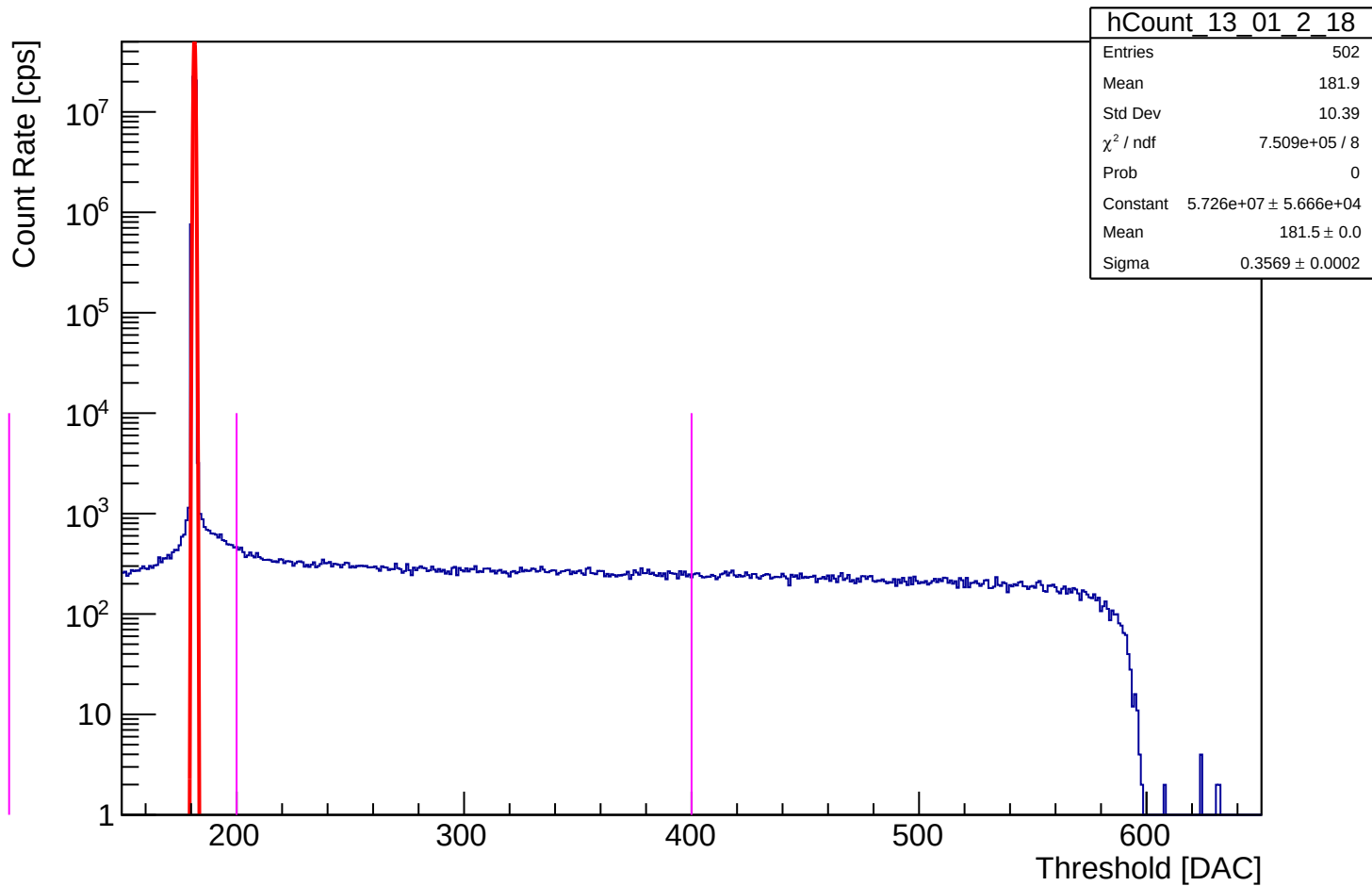
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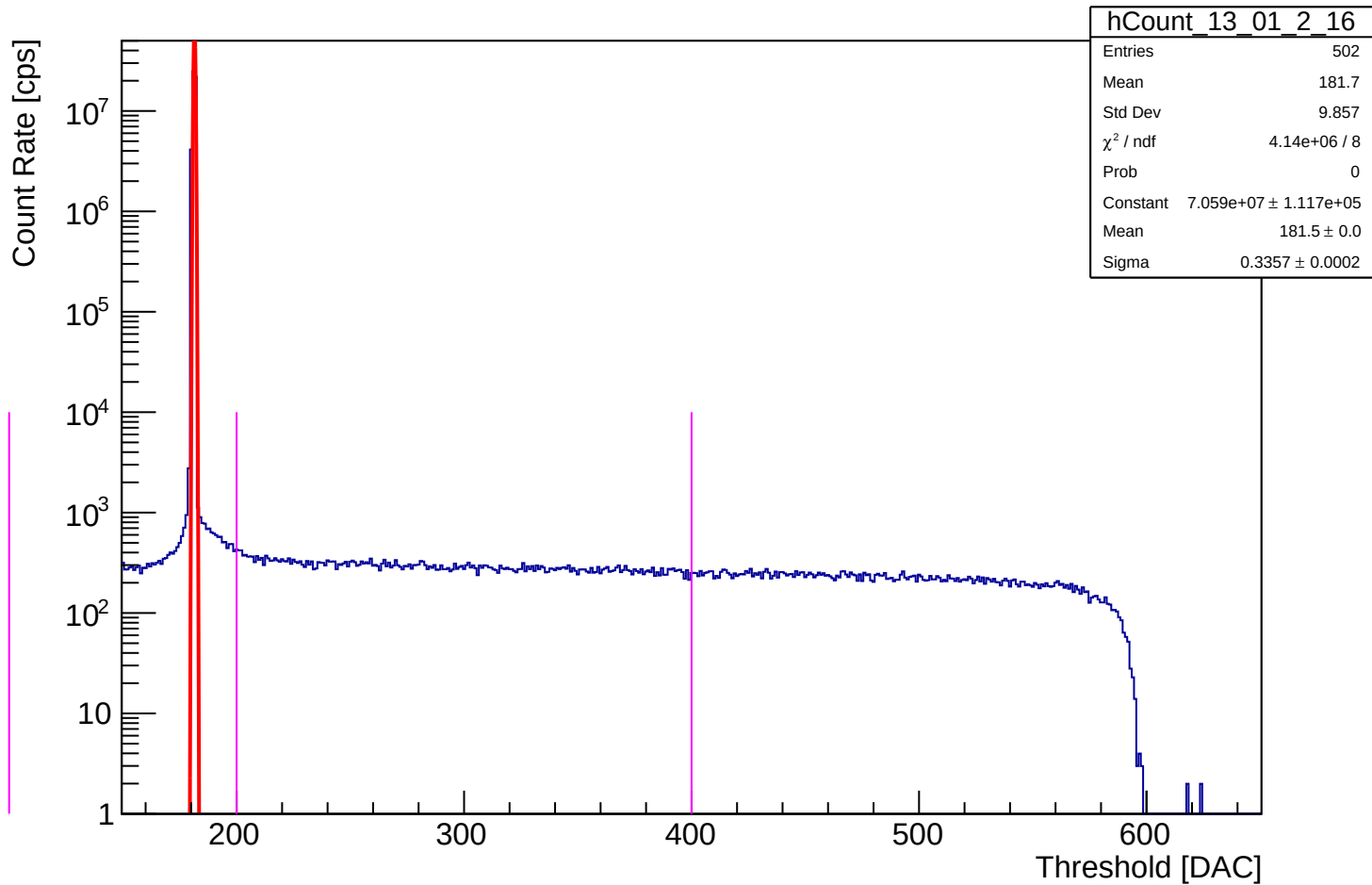
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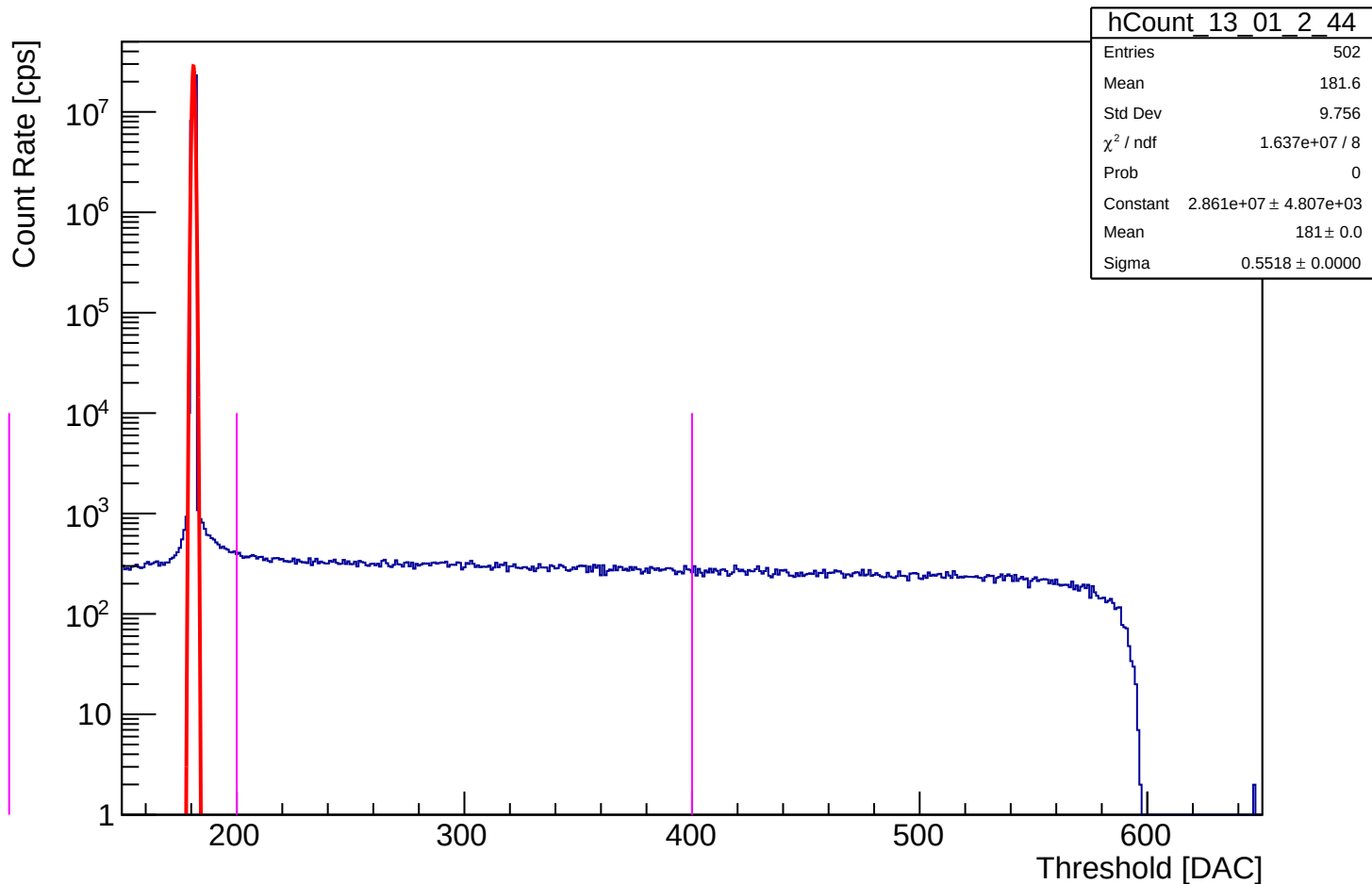


Row 1 Tile 1 Pmt 6 Pixel 27 Slot 13 Fiber 1 Asic 2 Channel 18

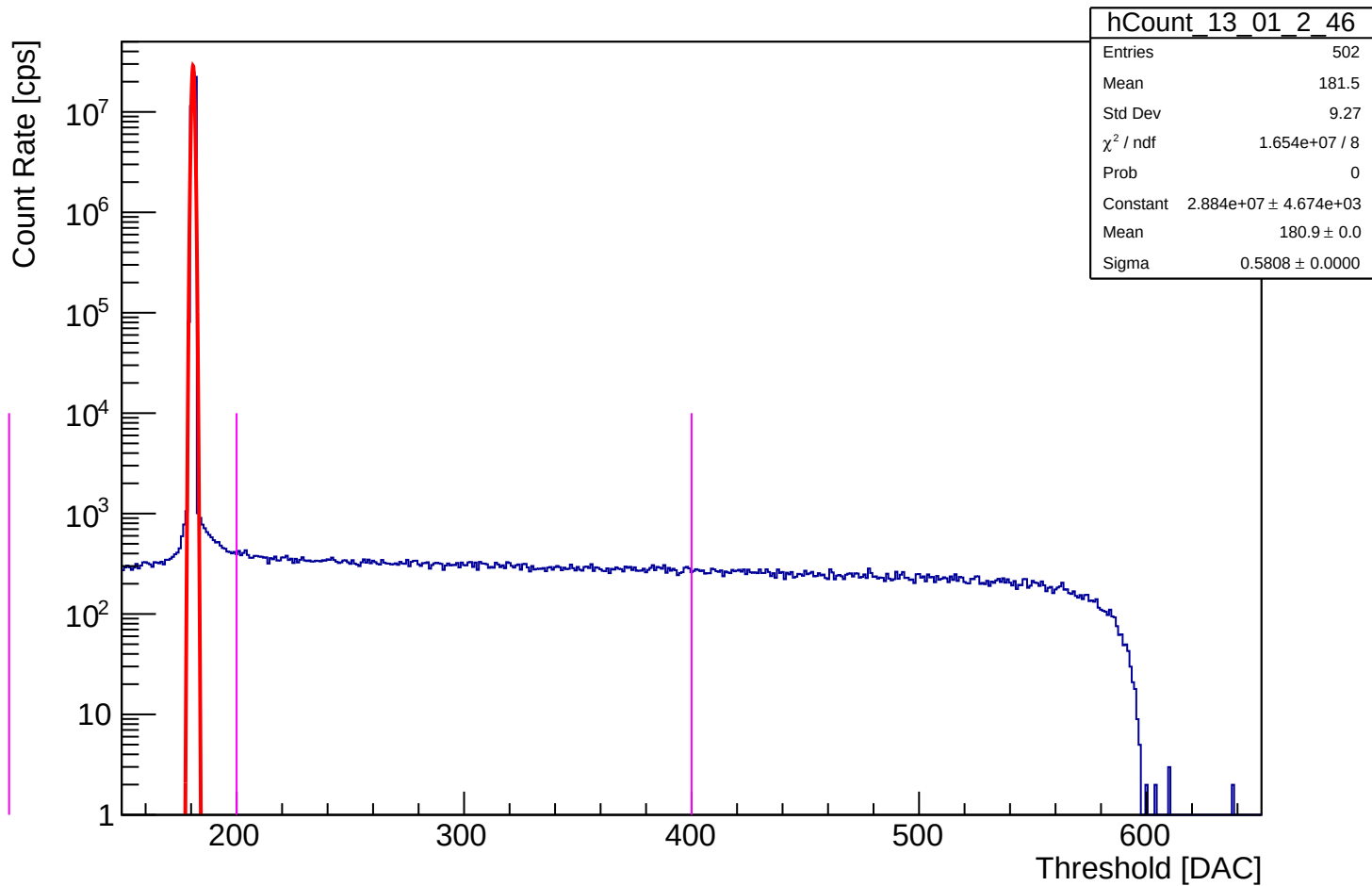


Row 1 Tile 1 Pmt 6 Pixel 28 Slot 13 Fiber 1 Asic 2 Channel 16

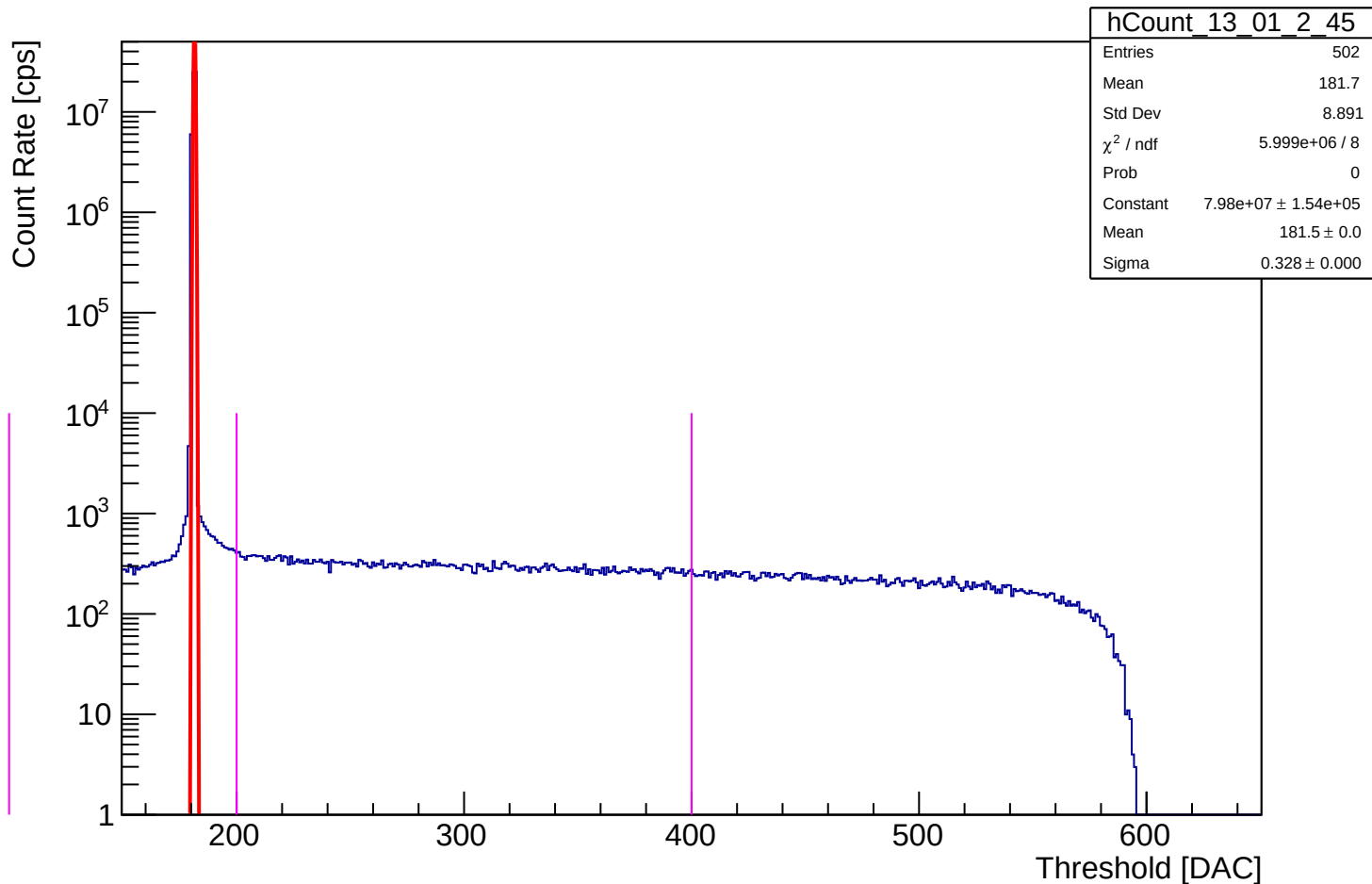




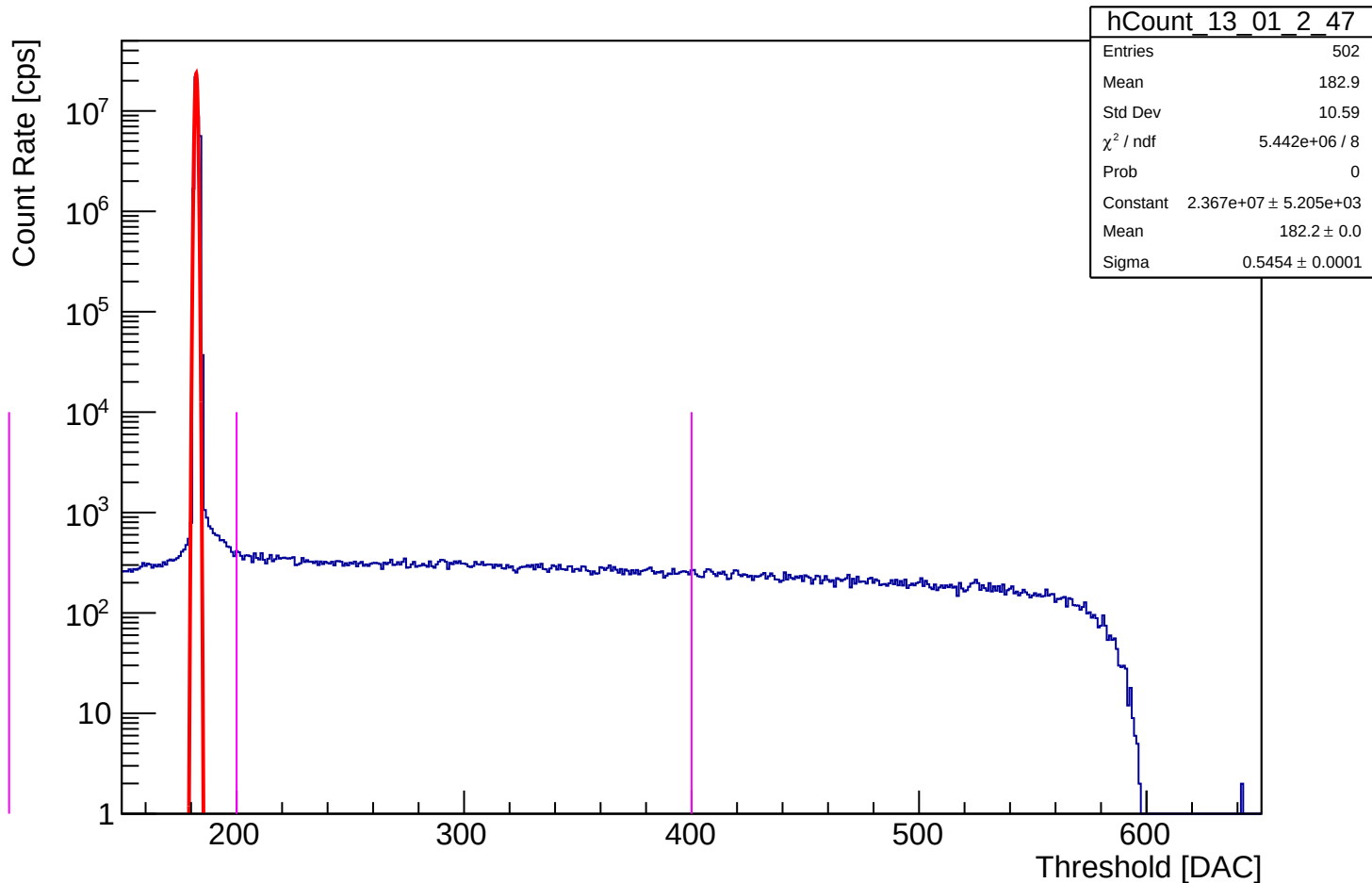
Row 1 Tile 1 Pmt 6 Pixel 30 Slot 13 Fiber 1 Asic 2 Channel 46



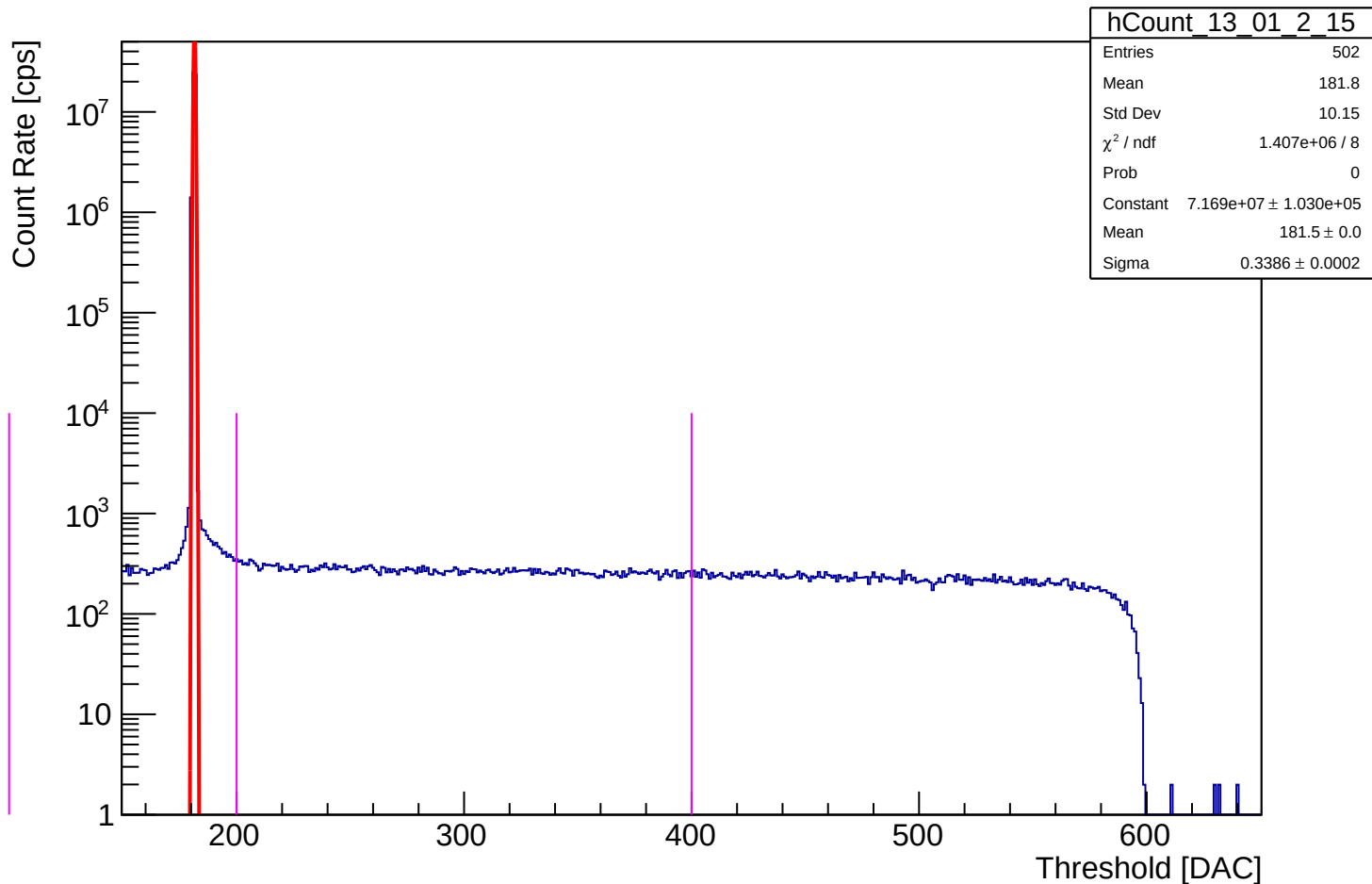
Row 1 Tile 1 Pmt 6 Pixel 31 Slot 13 Fiber 1 Asic 2 Channel 45



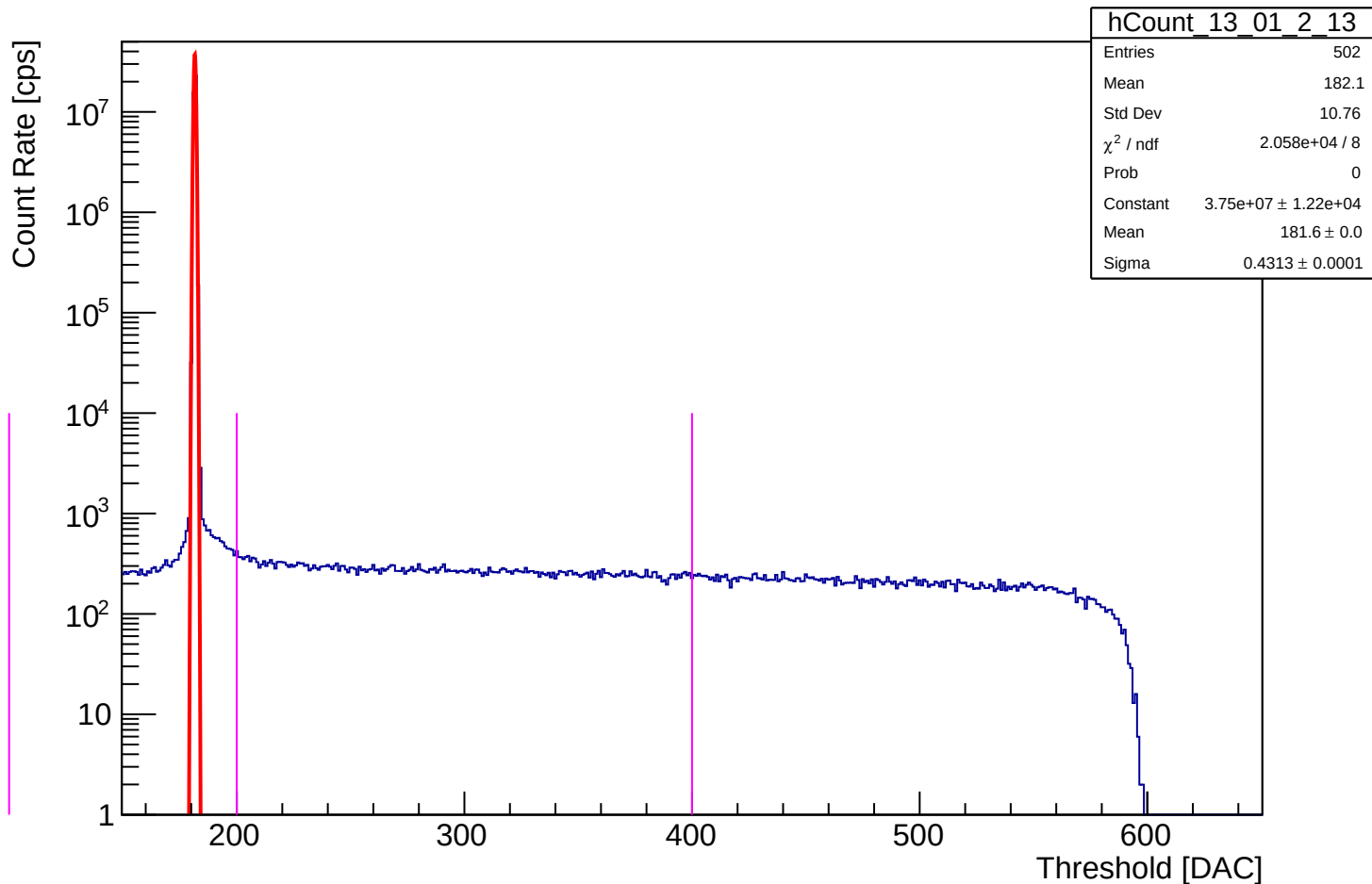
Row 1 Tile 1 Pmt 6 Pixel 32 Slot 13 Fiber 1 Asic 2 Channel 47



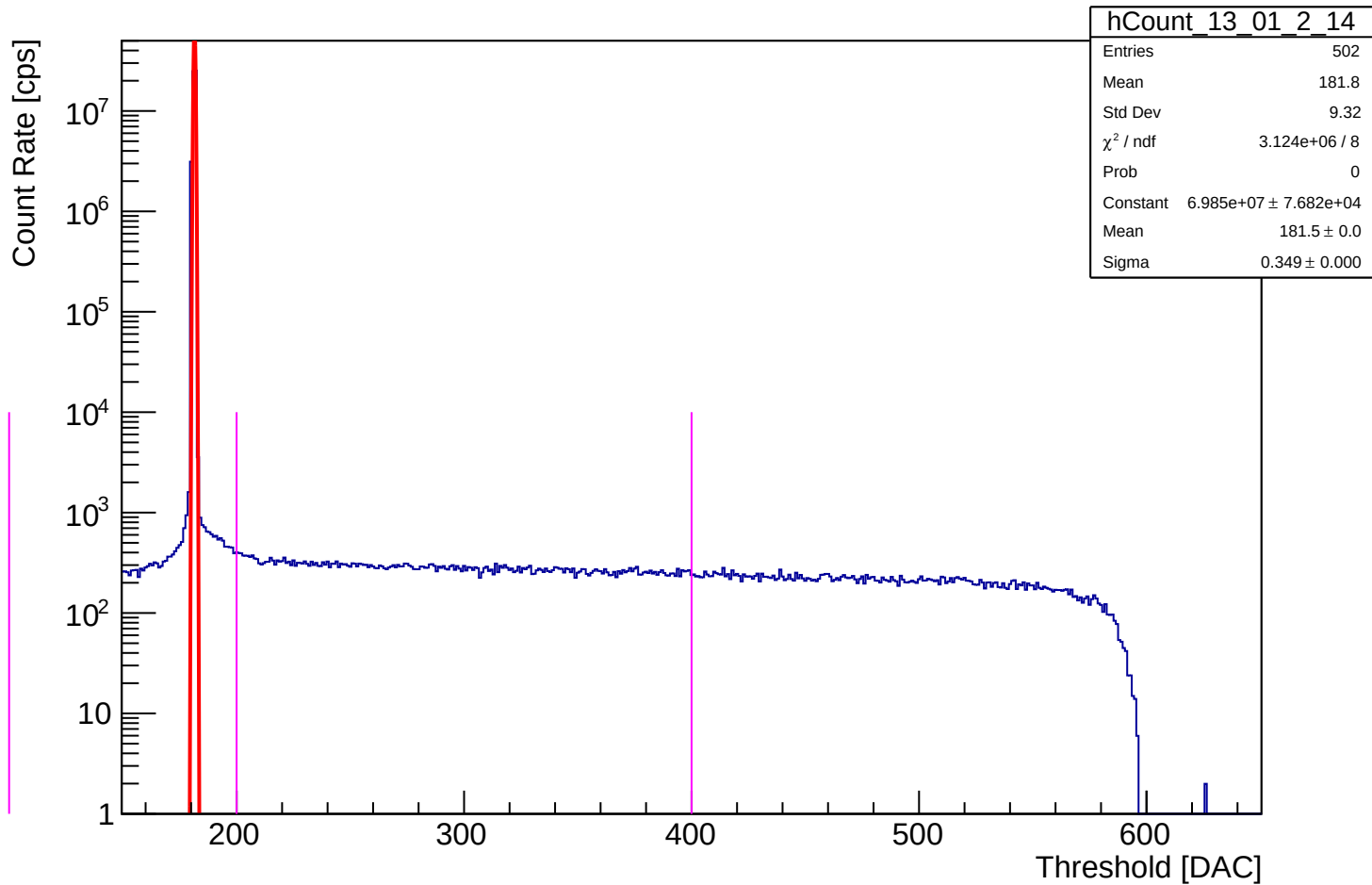
Row 1 Tile 1 Pmt 6 Pixel 33 Slot 13 Fiber 1 Asic 2 Channel 15



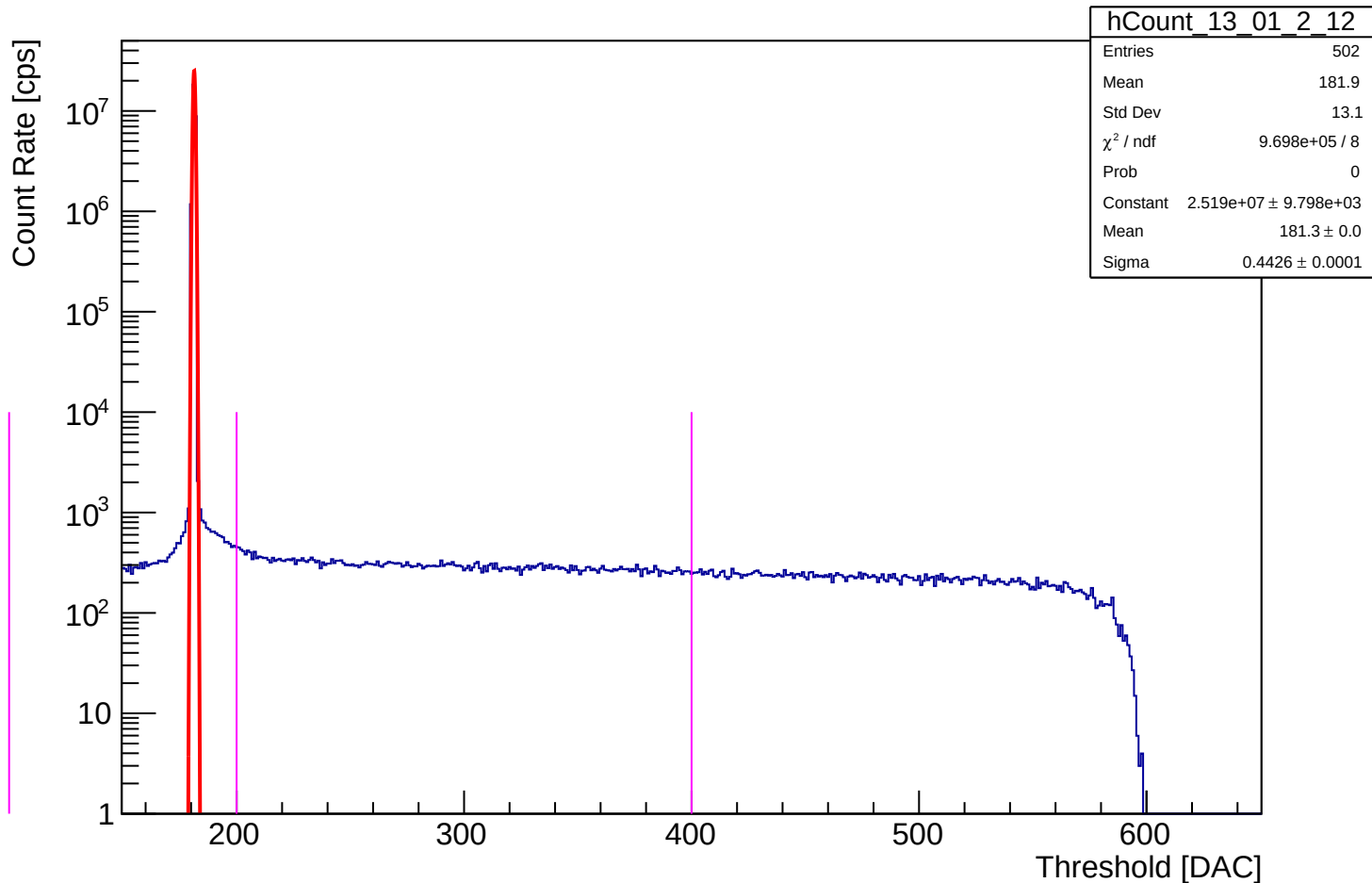
Row 1 Tile 1 Pmt 6 Pixel 34 Slot 13 Fiber 1 Asic 2 Channel 13



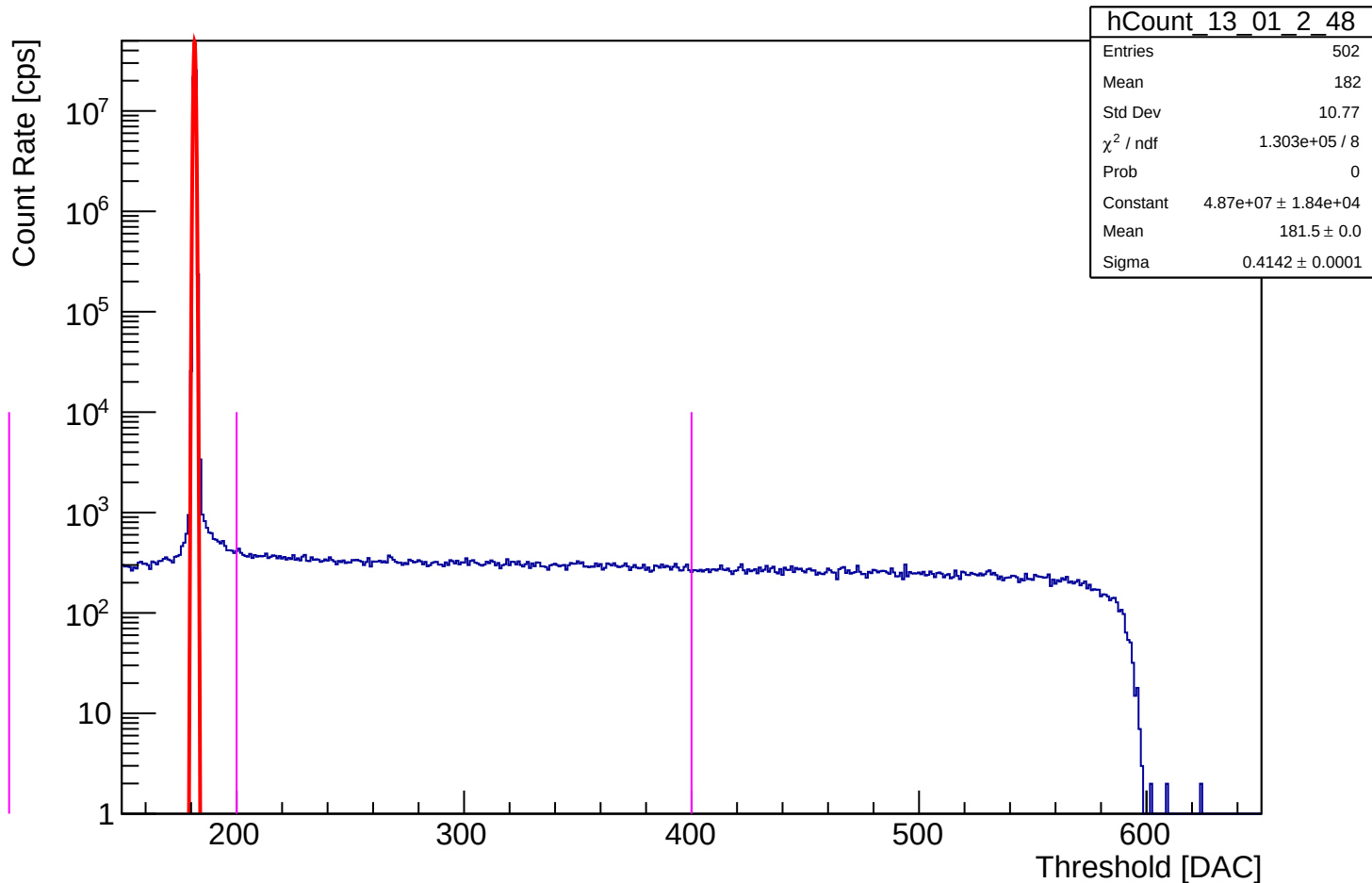
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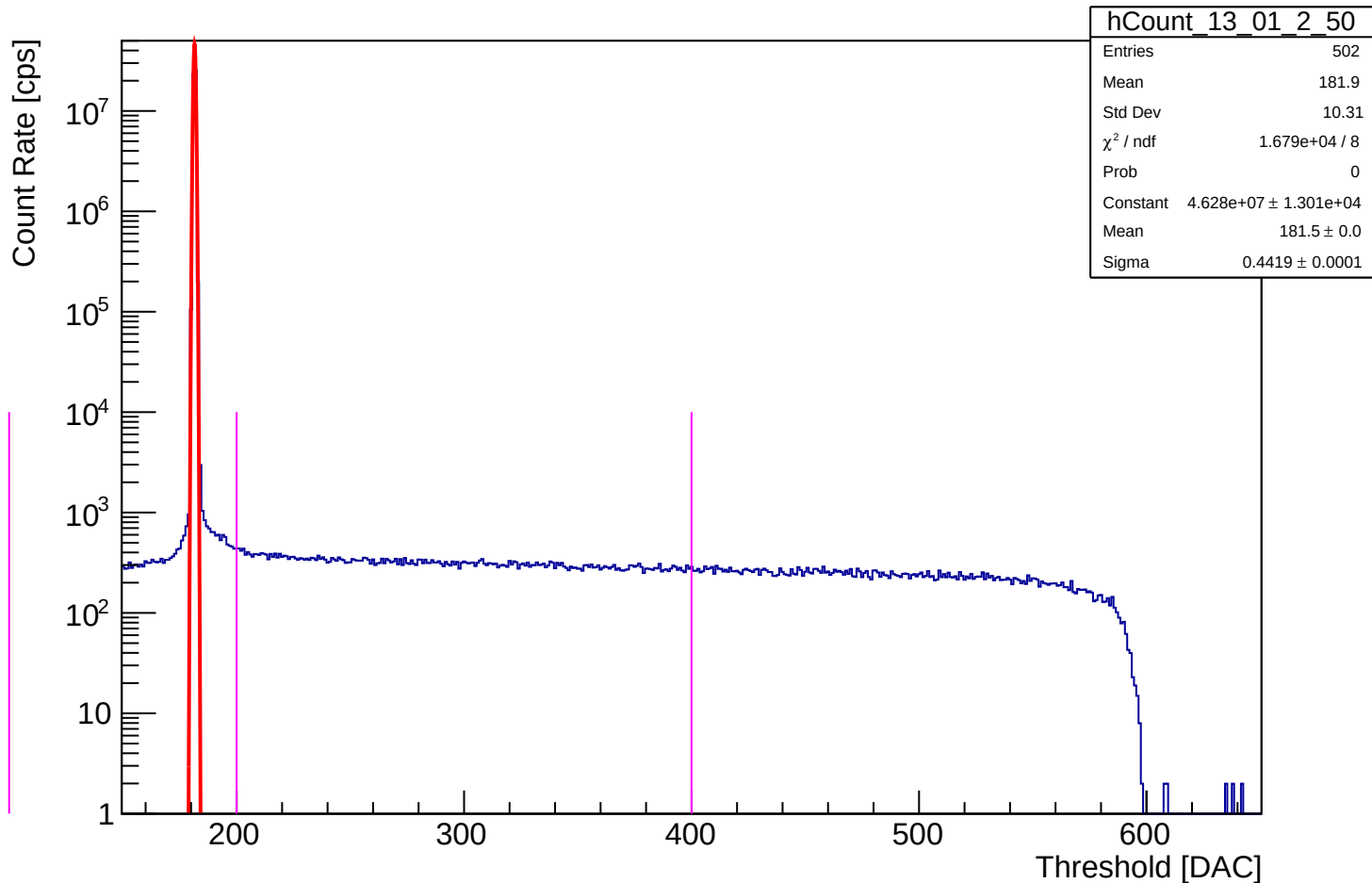
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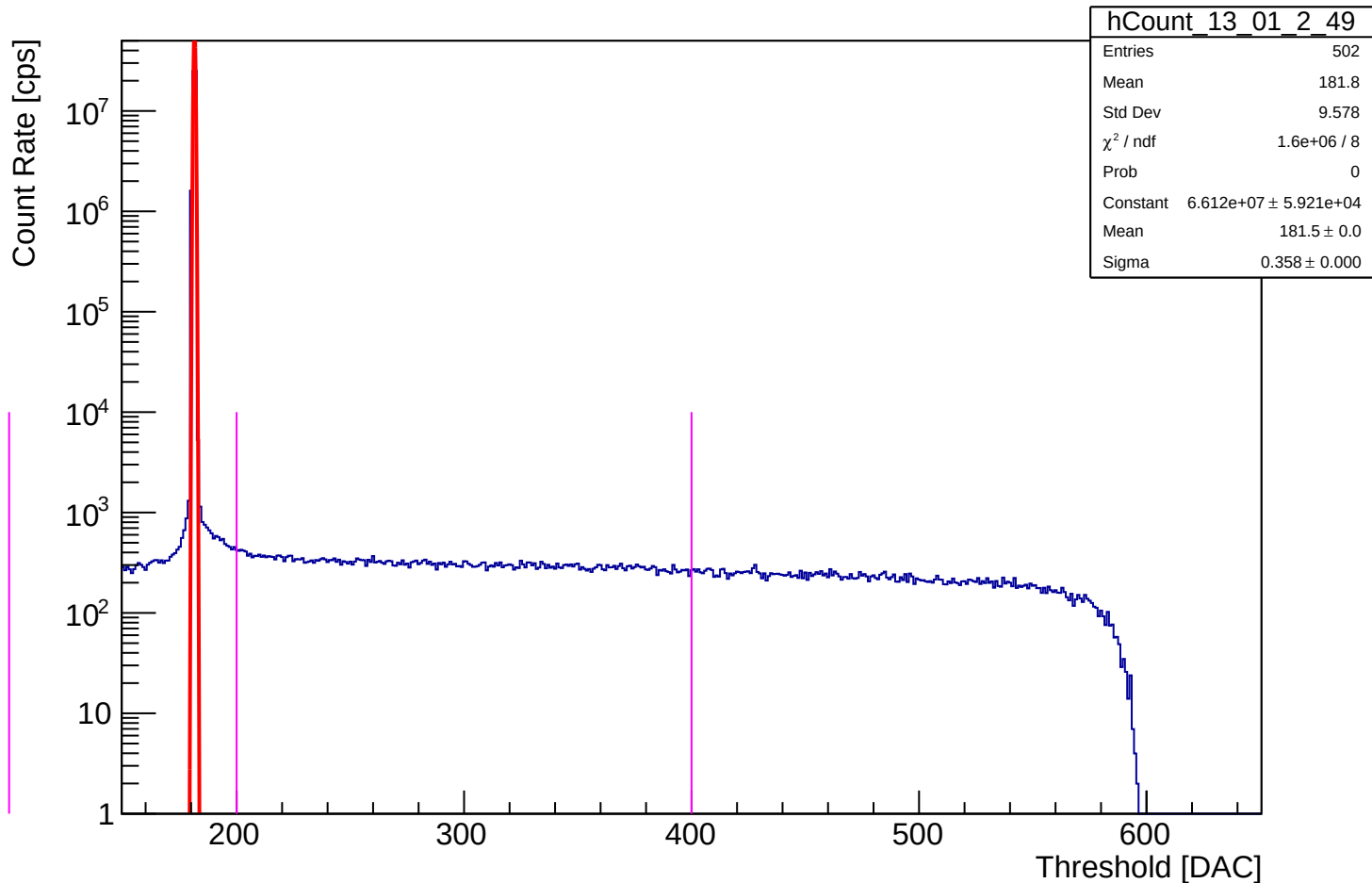
Row 1 Tile 1 Pmt 6 Pixel 37 Slot 13 Fiber 1 Asic 2 Channel 48



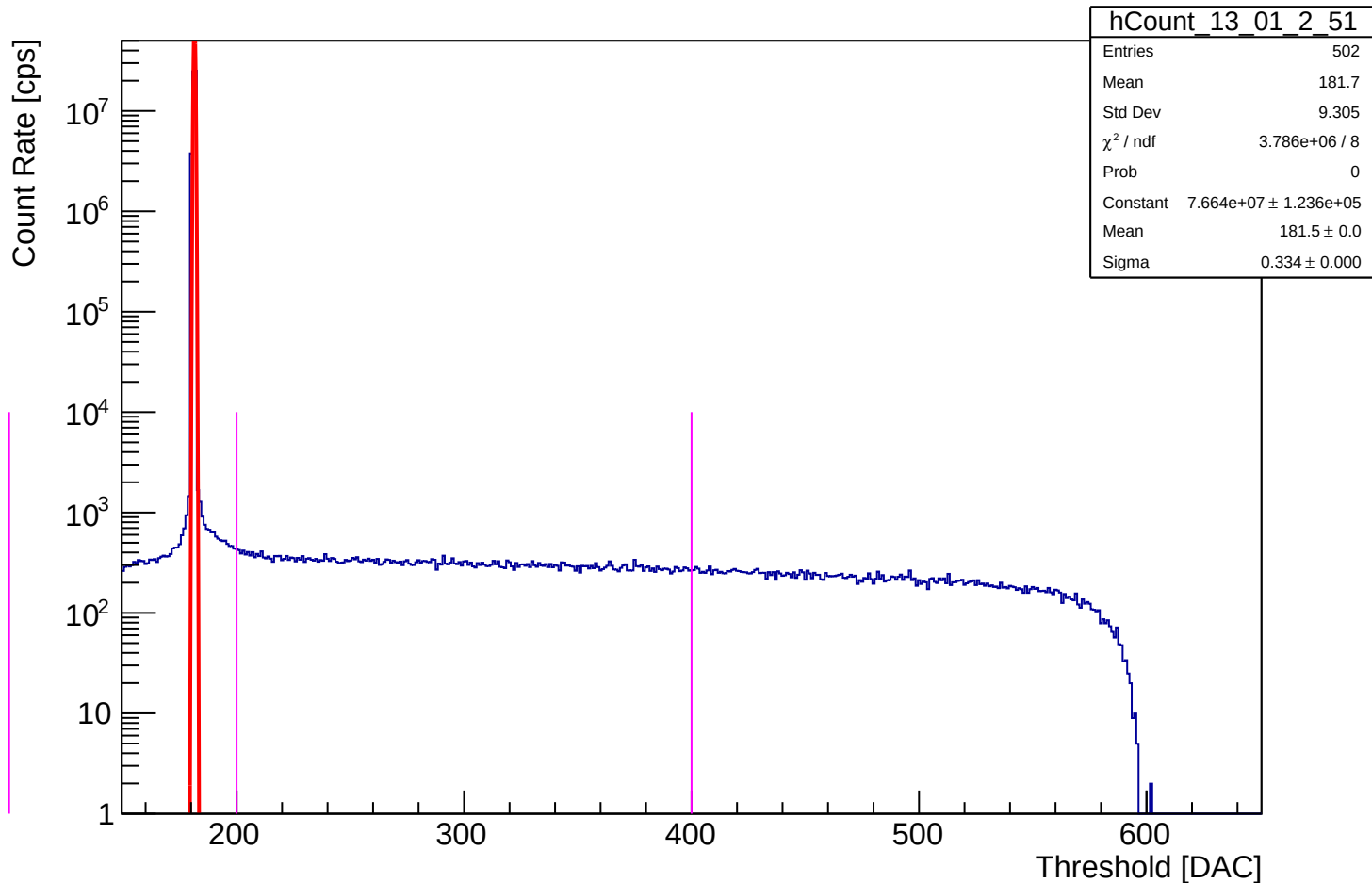
Row 1 Tile 1 Pmt 6 Pixel 38 Slot 13 Fiber 1 Asic 2 Channel 50



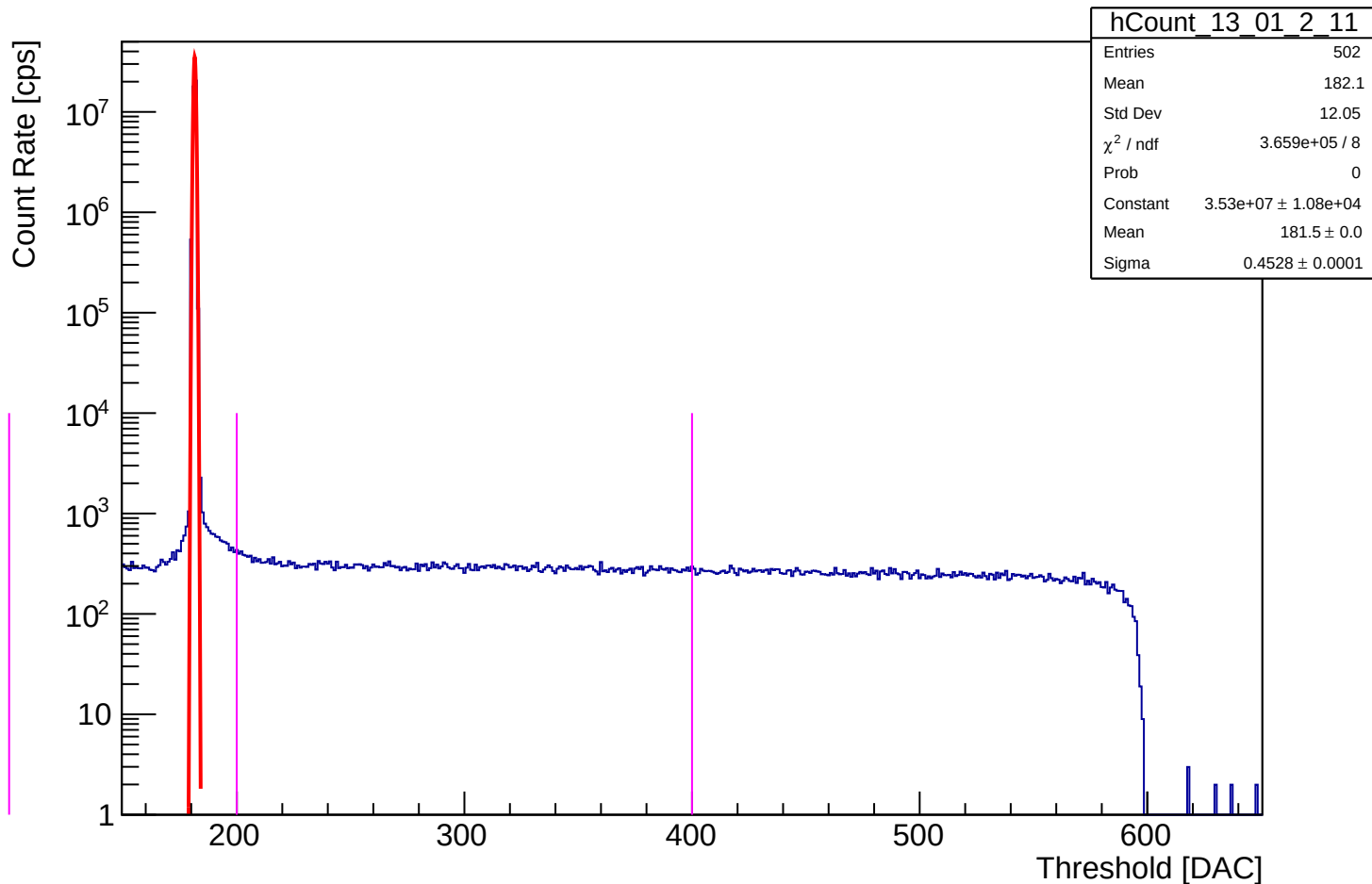
Row 1 Tile 1 Pmt 6 Pixel 39 Slot 13 Fiber 1 Asic 2 Channel 49

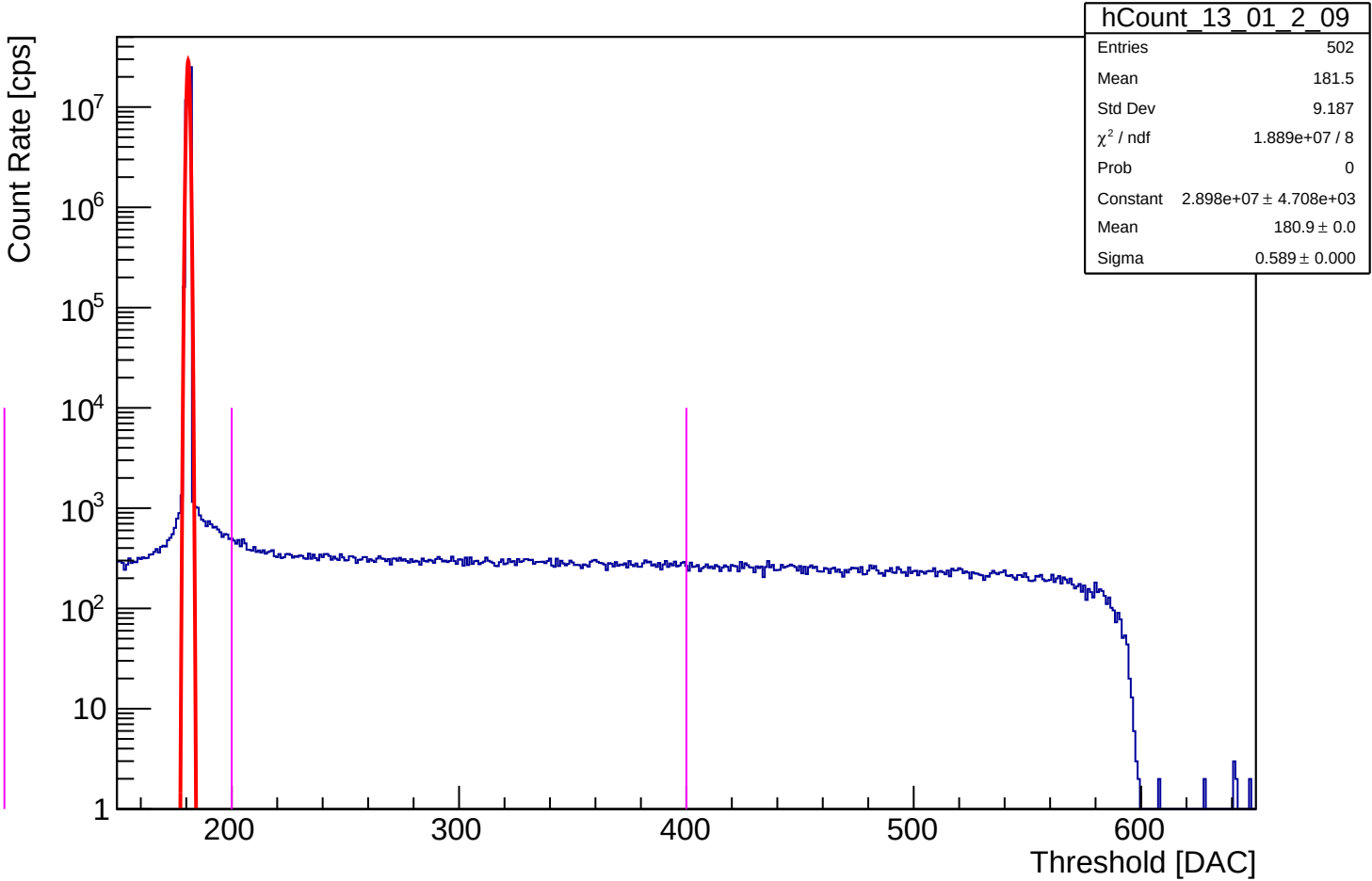


Row 1 Tile 1 Pmt 6 Pixel 40 Slot 13 Fiber 1 Asic 2 Channel 51

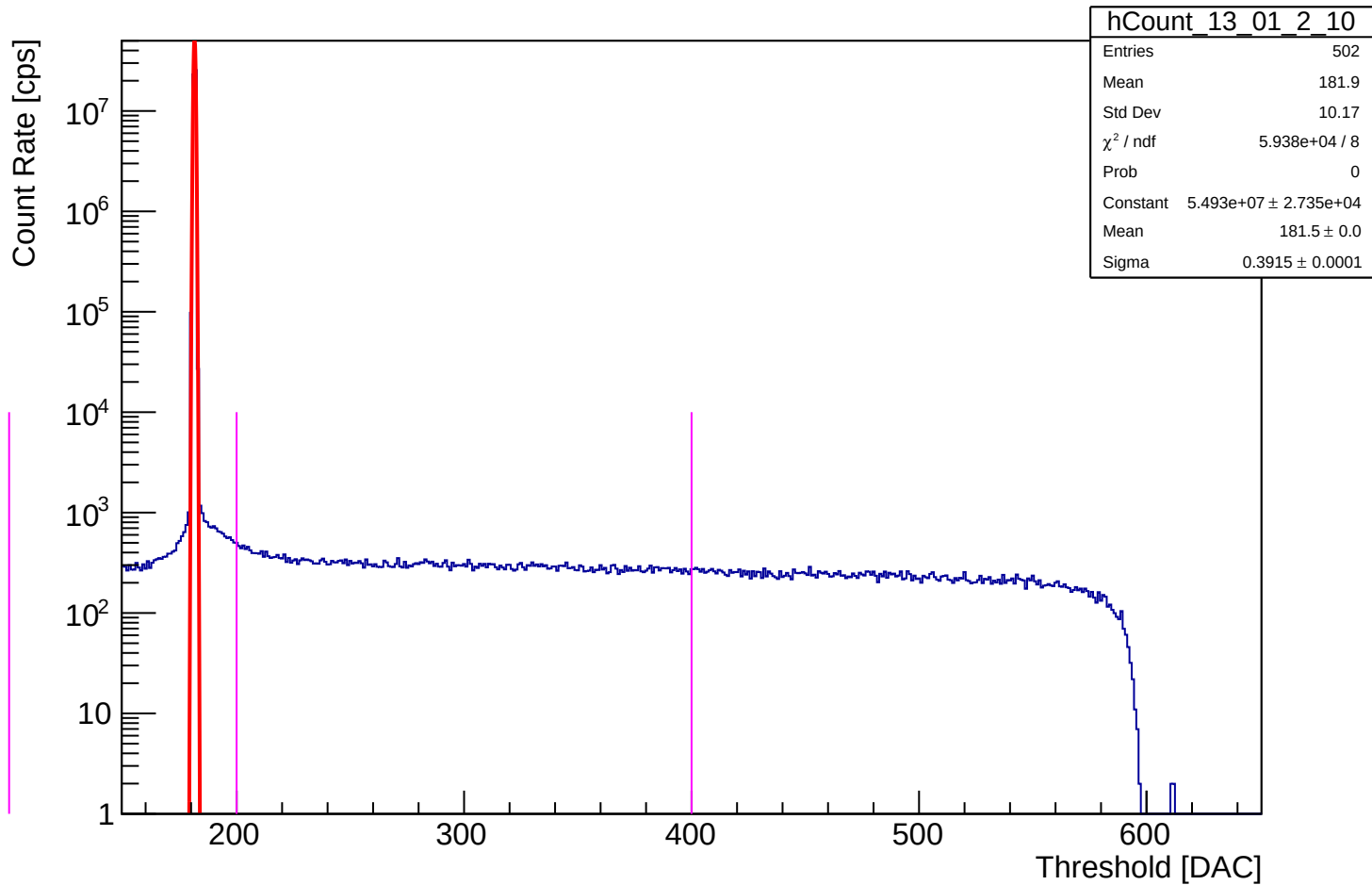


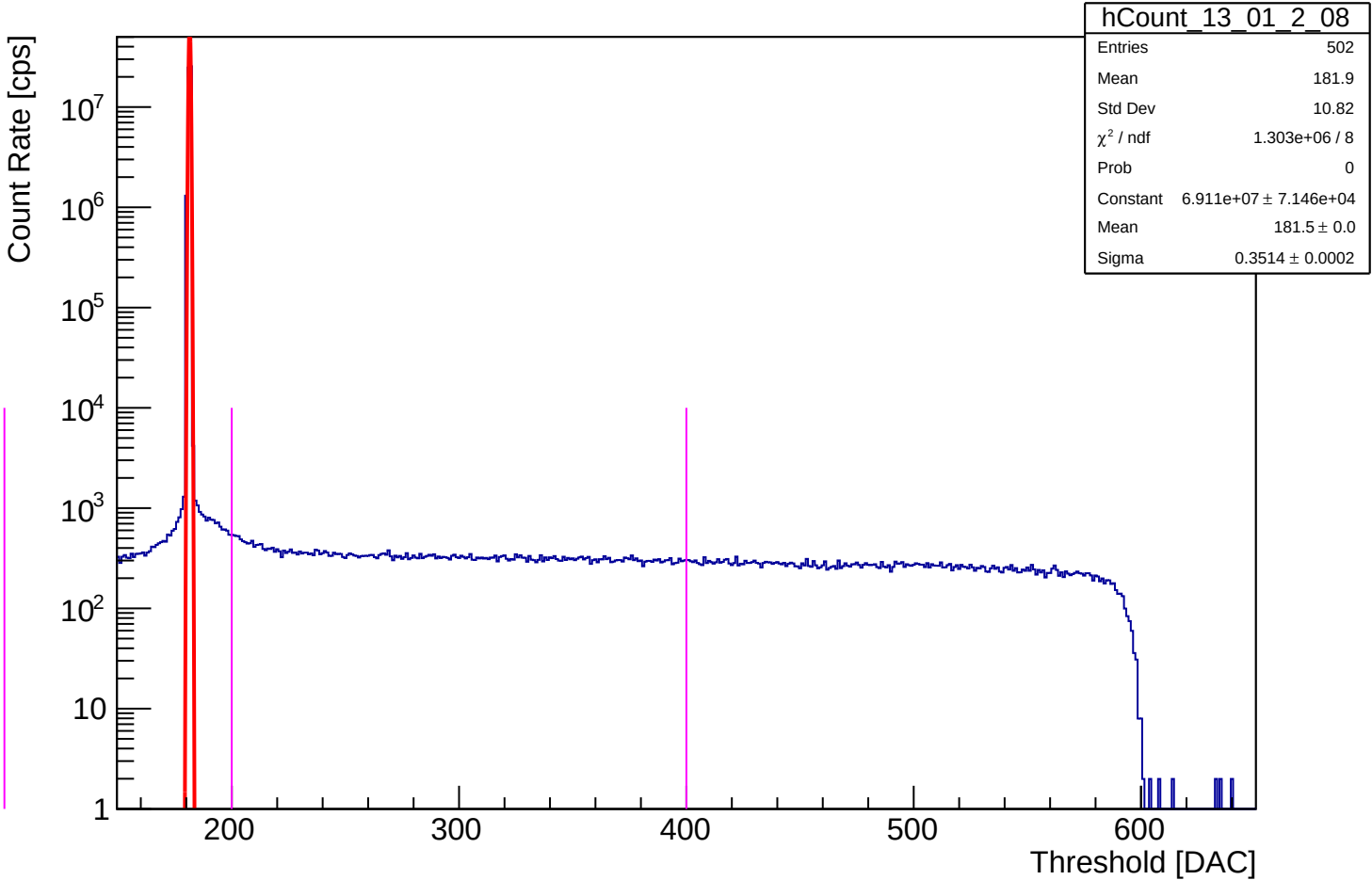
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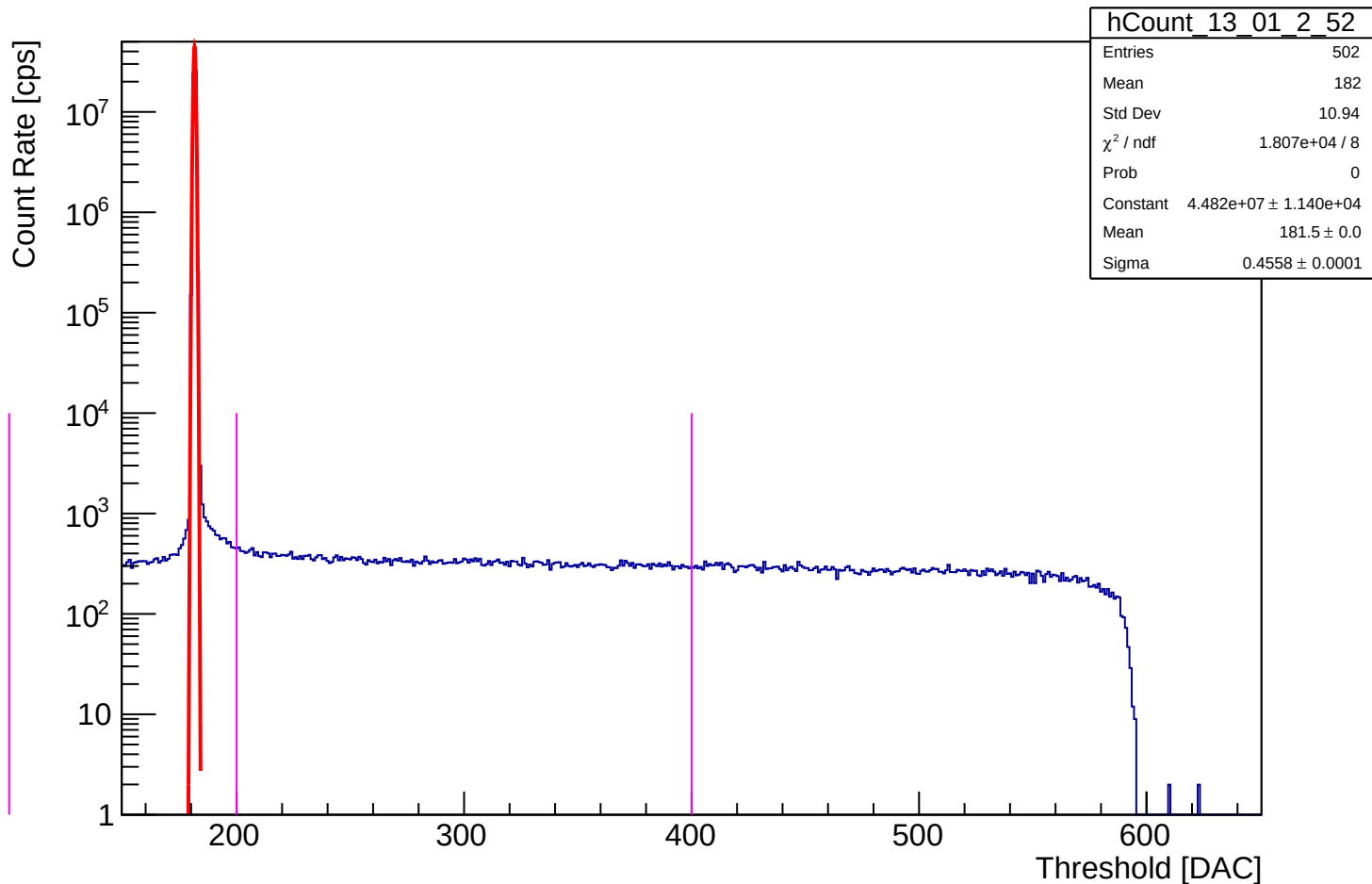


Row 1 Tile 1 Pmt 6 Pixel 43 Slot 13 Fiber 1 Asic 2 Channel 10

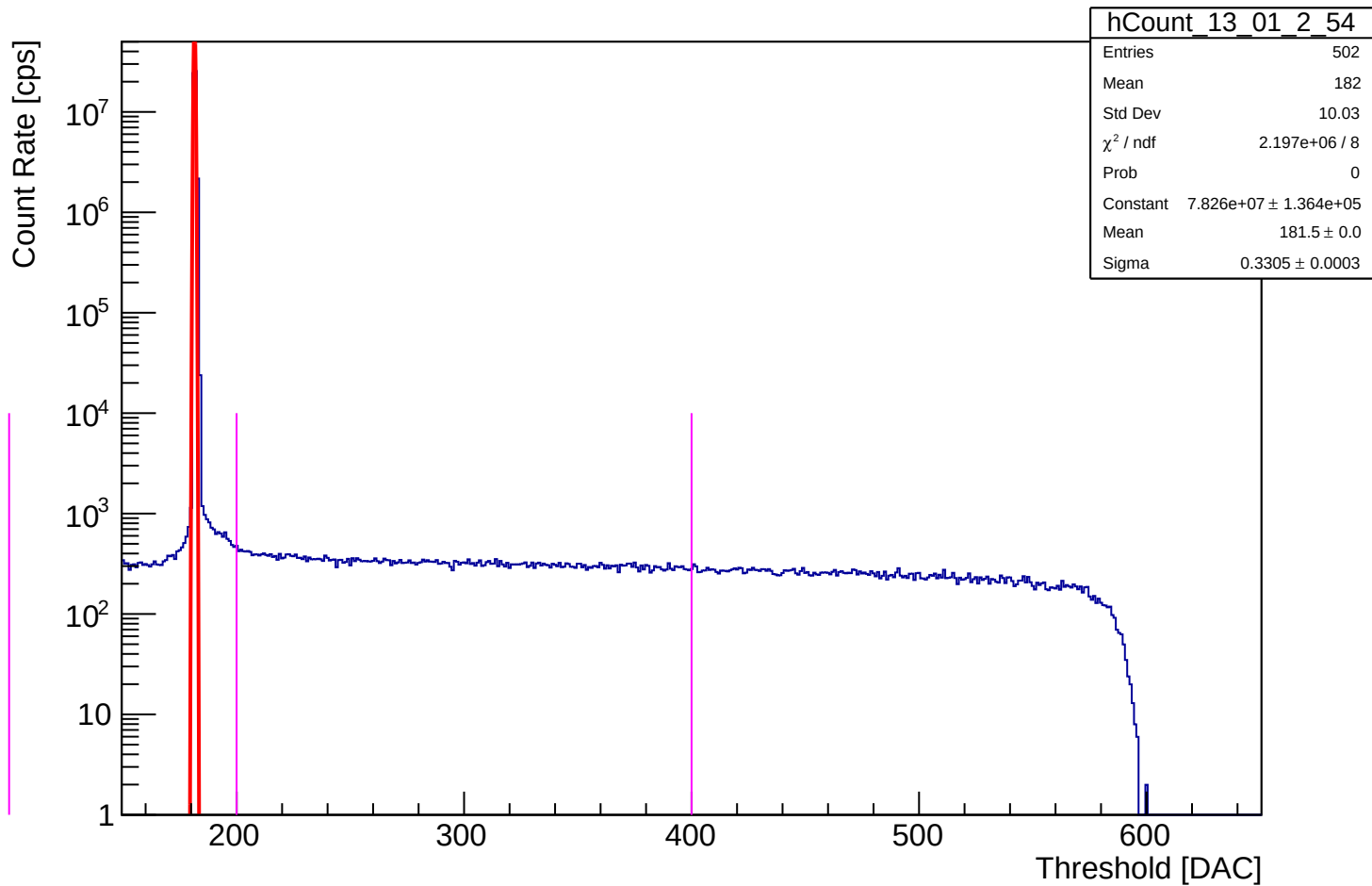




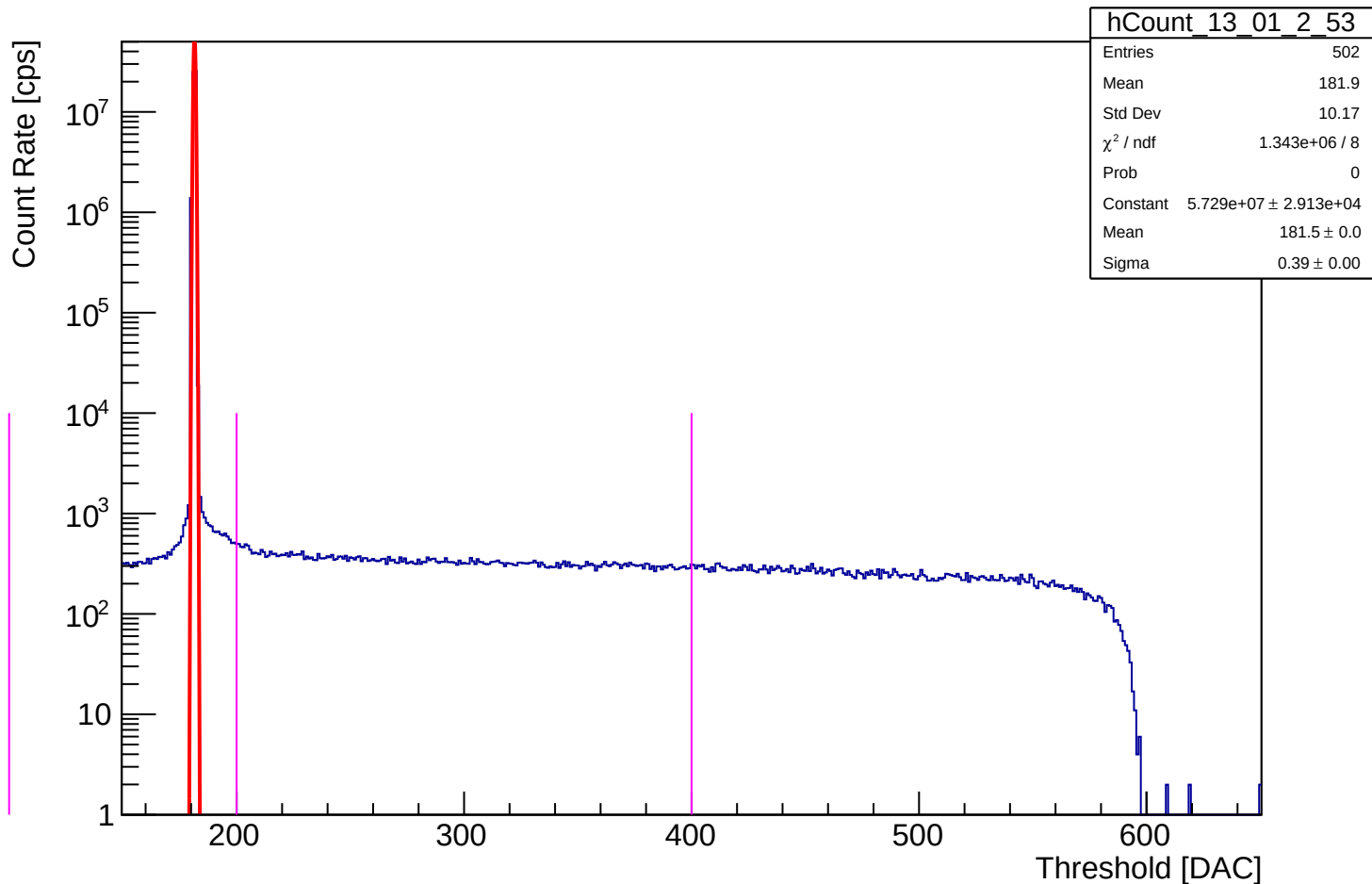
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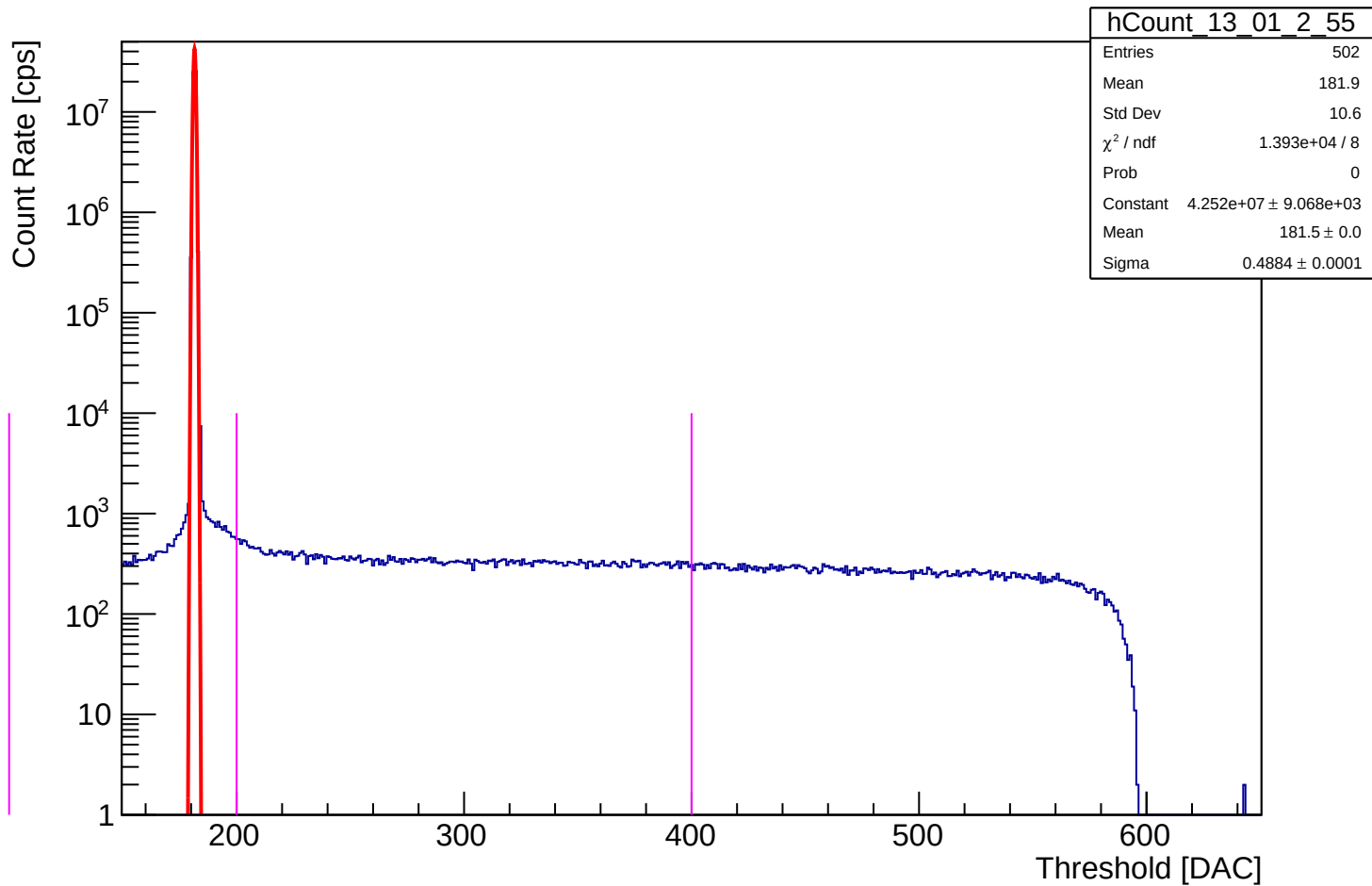
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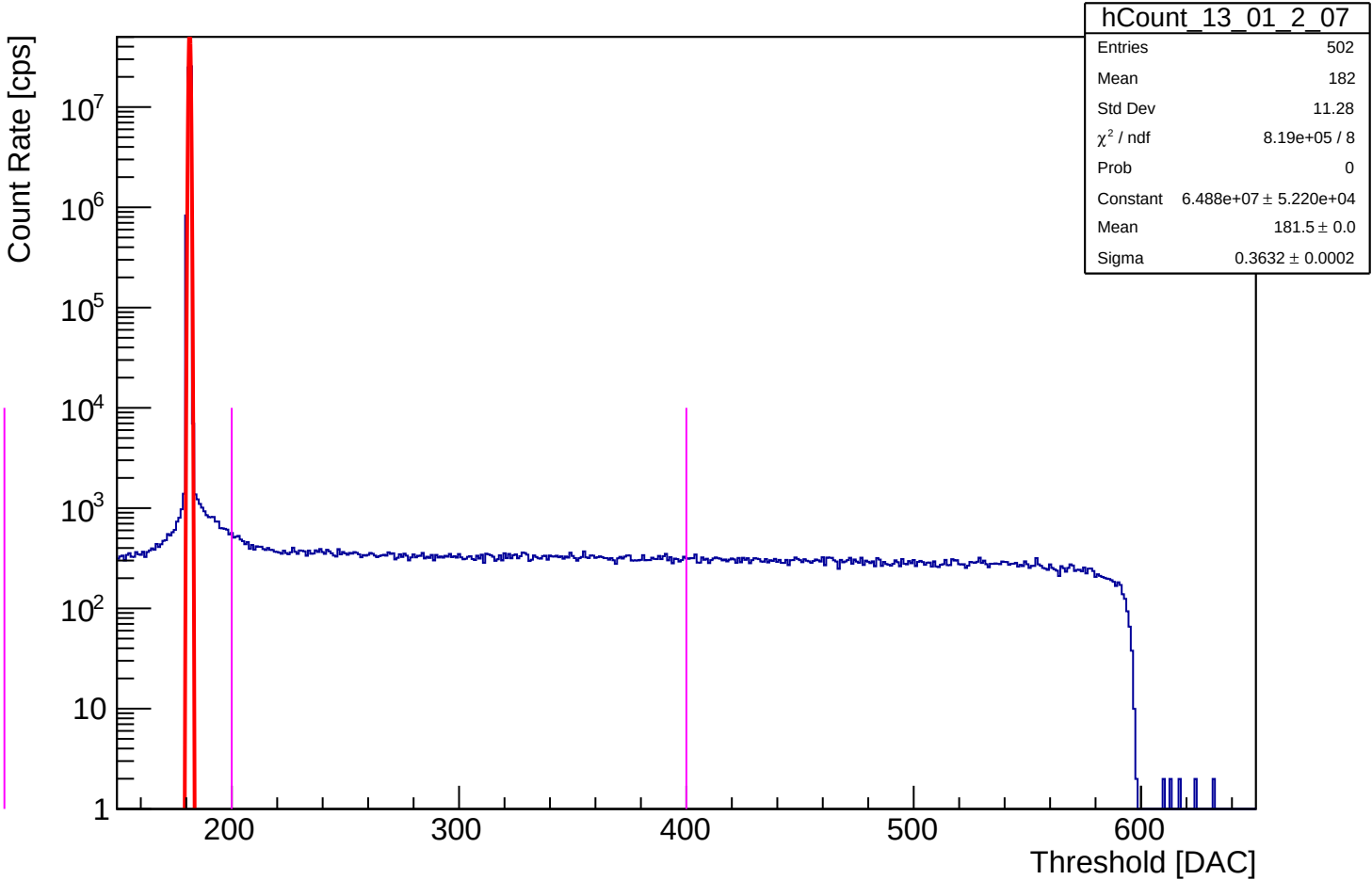


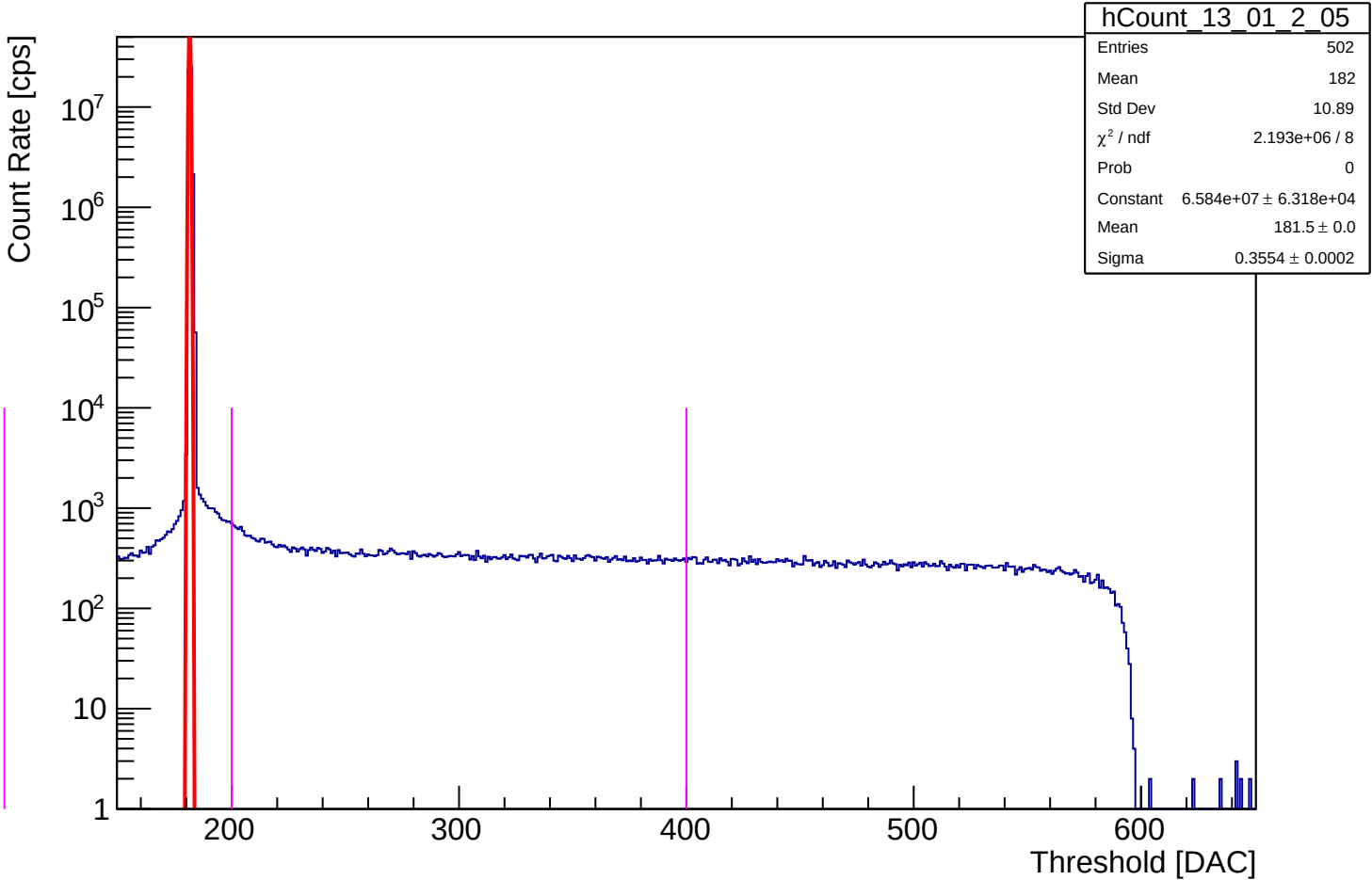
Row 1 Tile 1 Pmt 6 Pixel 47 Slot 13 Fiber 1 Asic 2 Channel 53

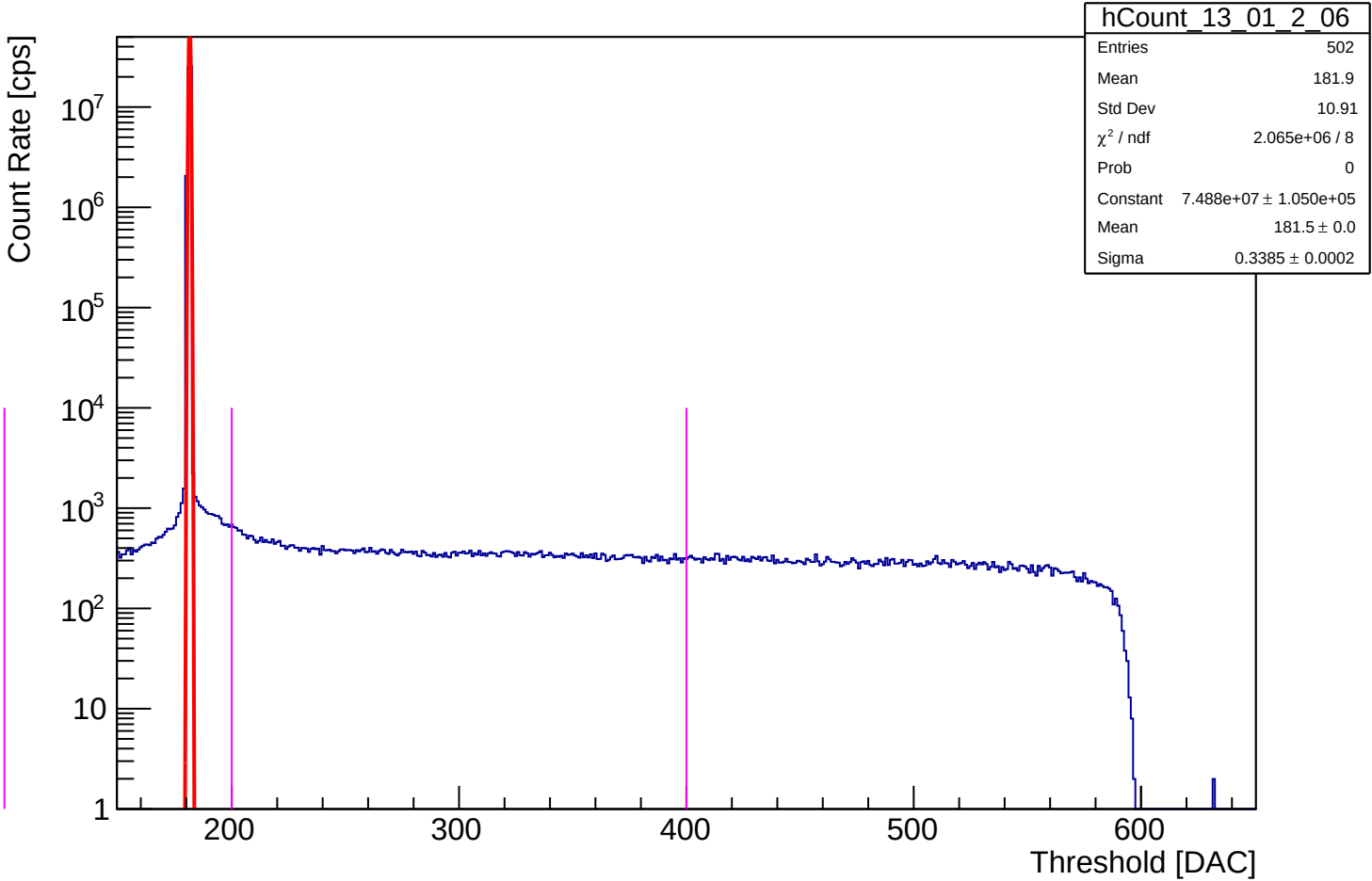


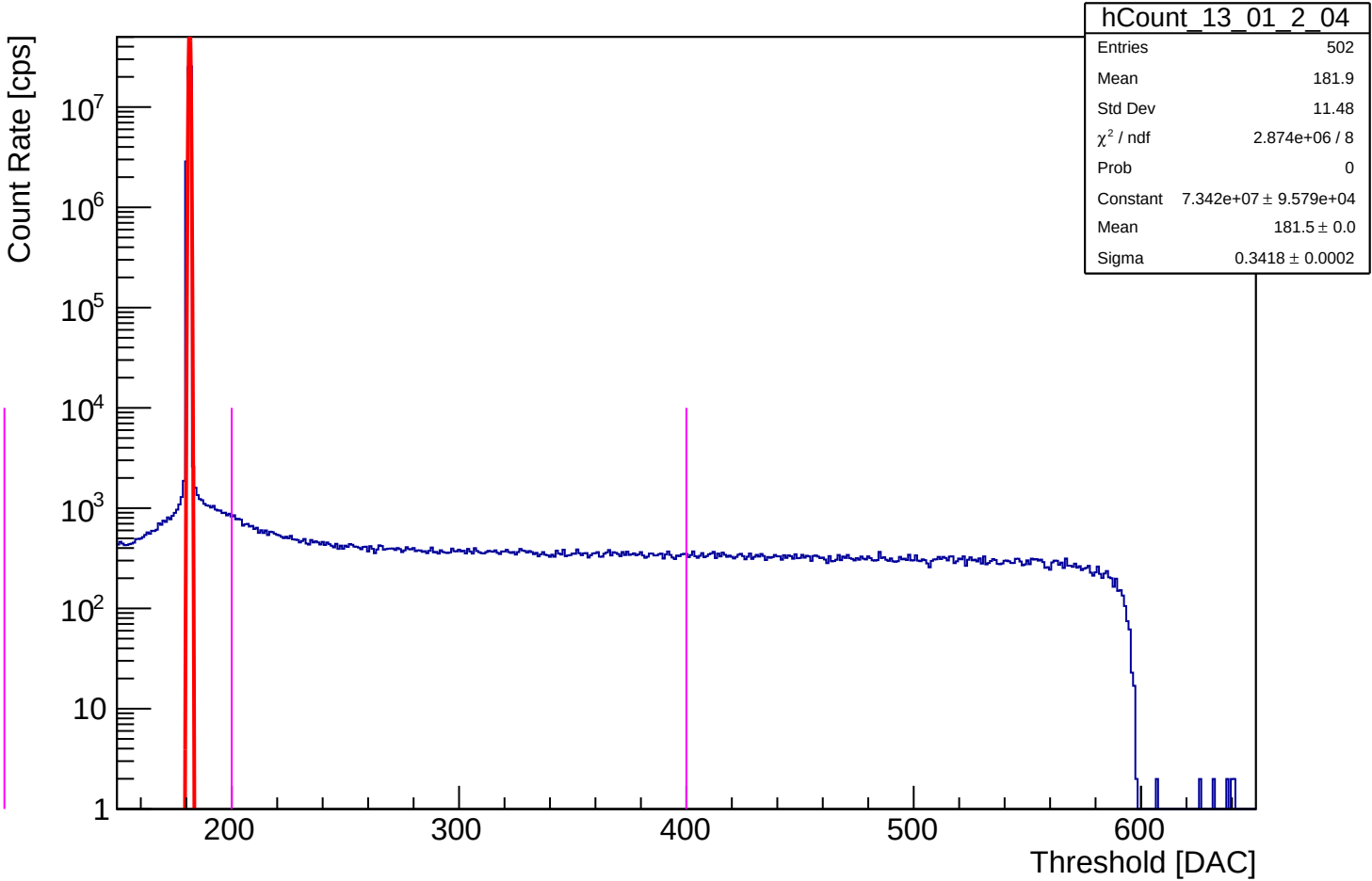
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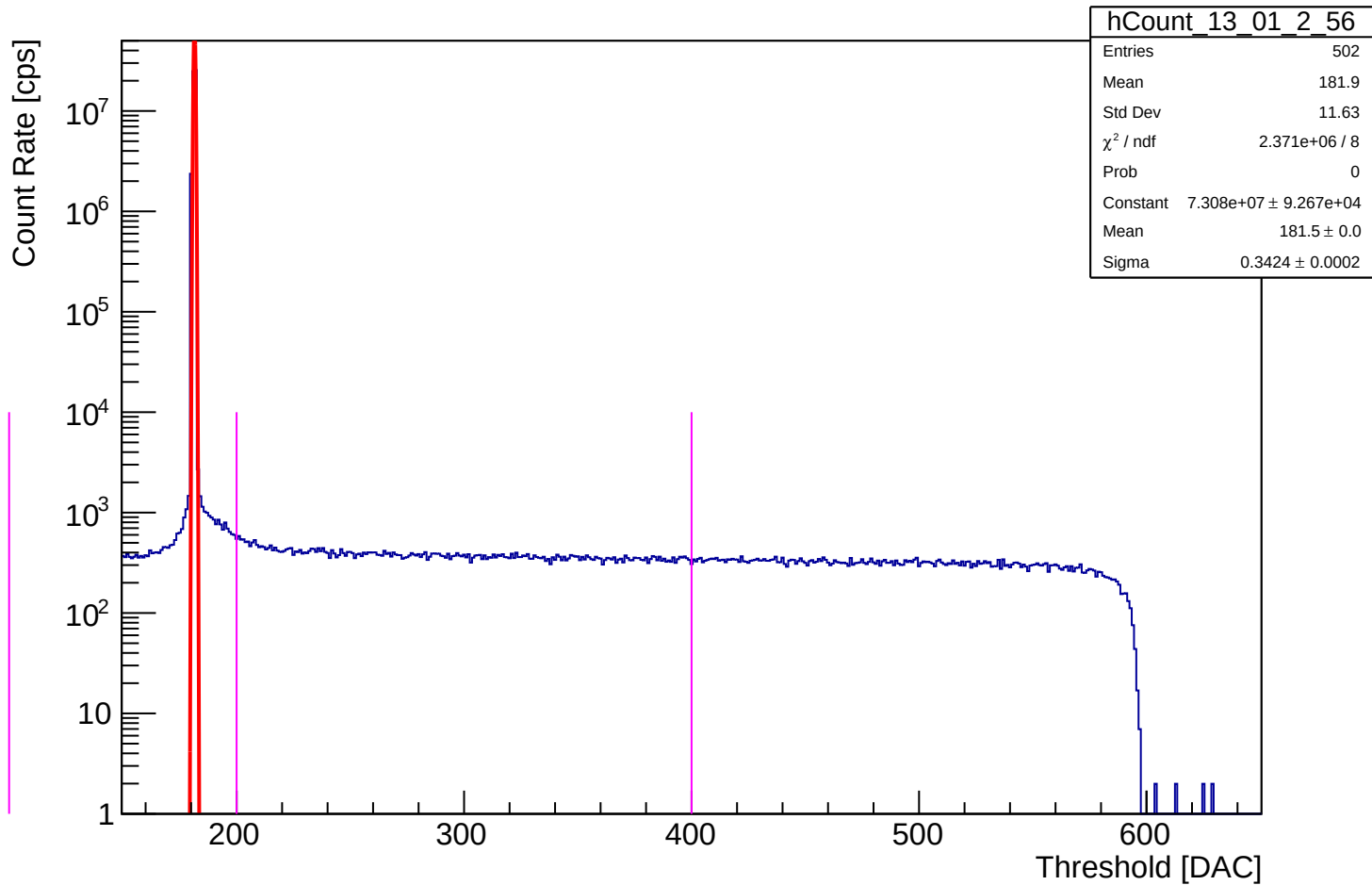




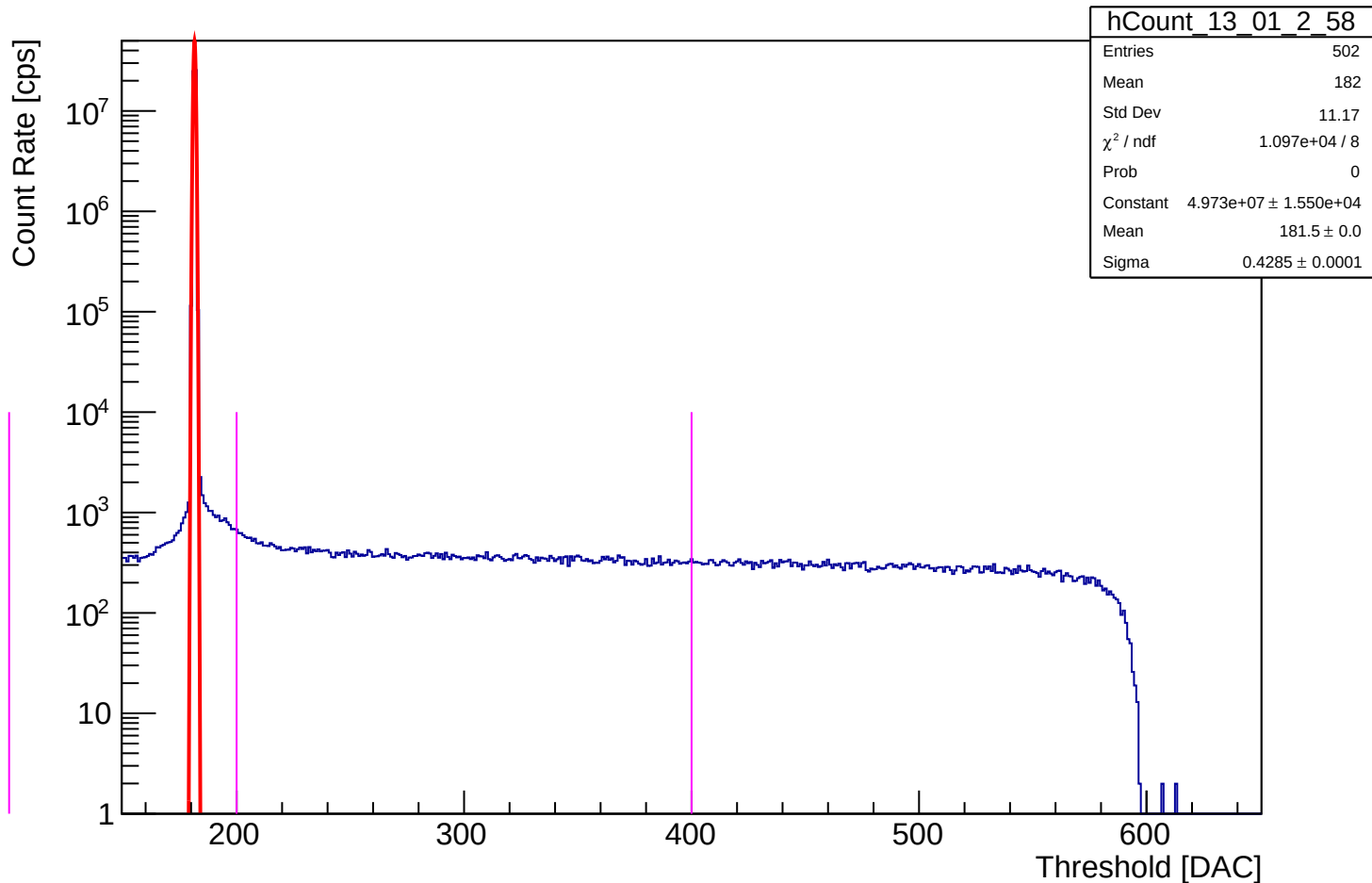




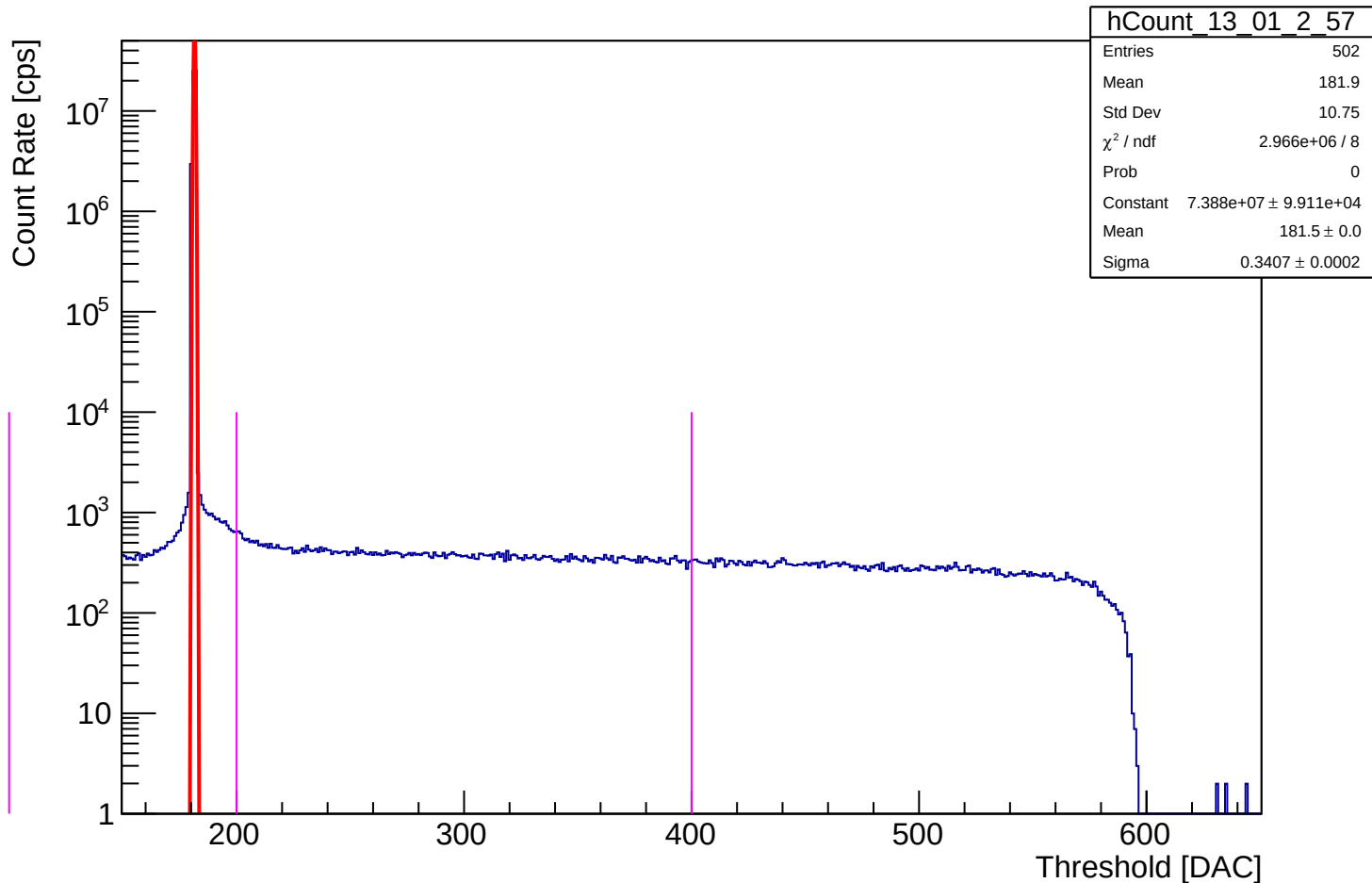
Row 1 Tile 1 Pmt 6 Pixel 53 Slot 13 Fiber 1 Asic 2 Channel 56

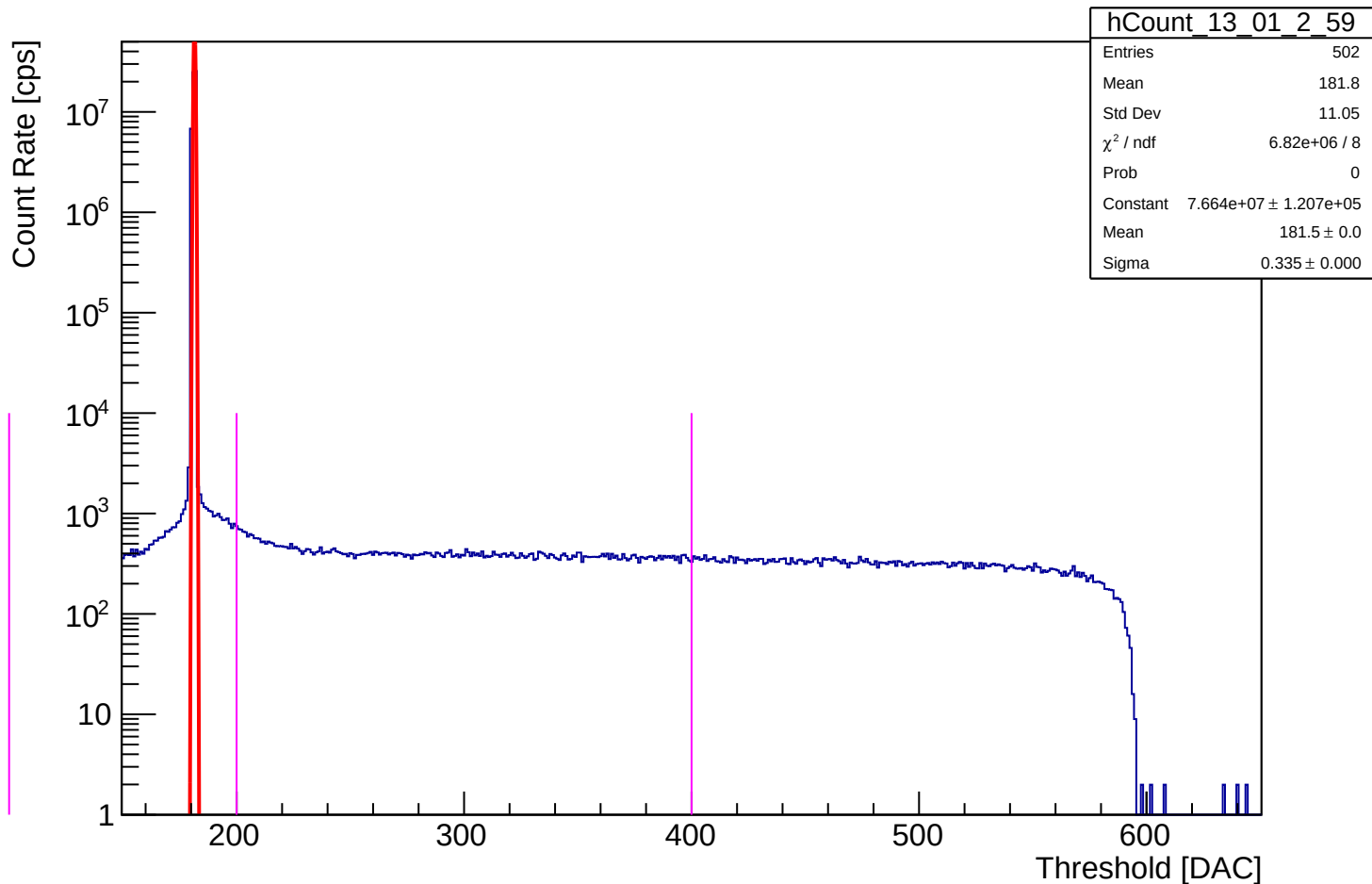


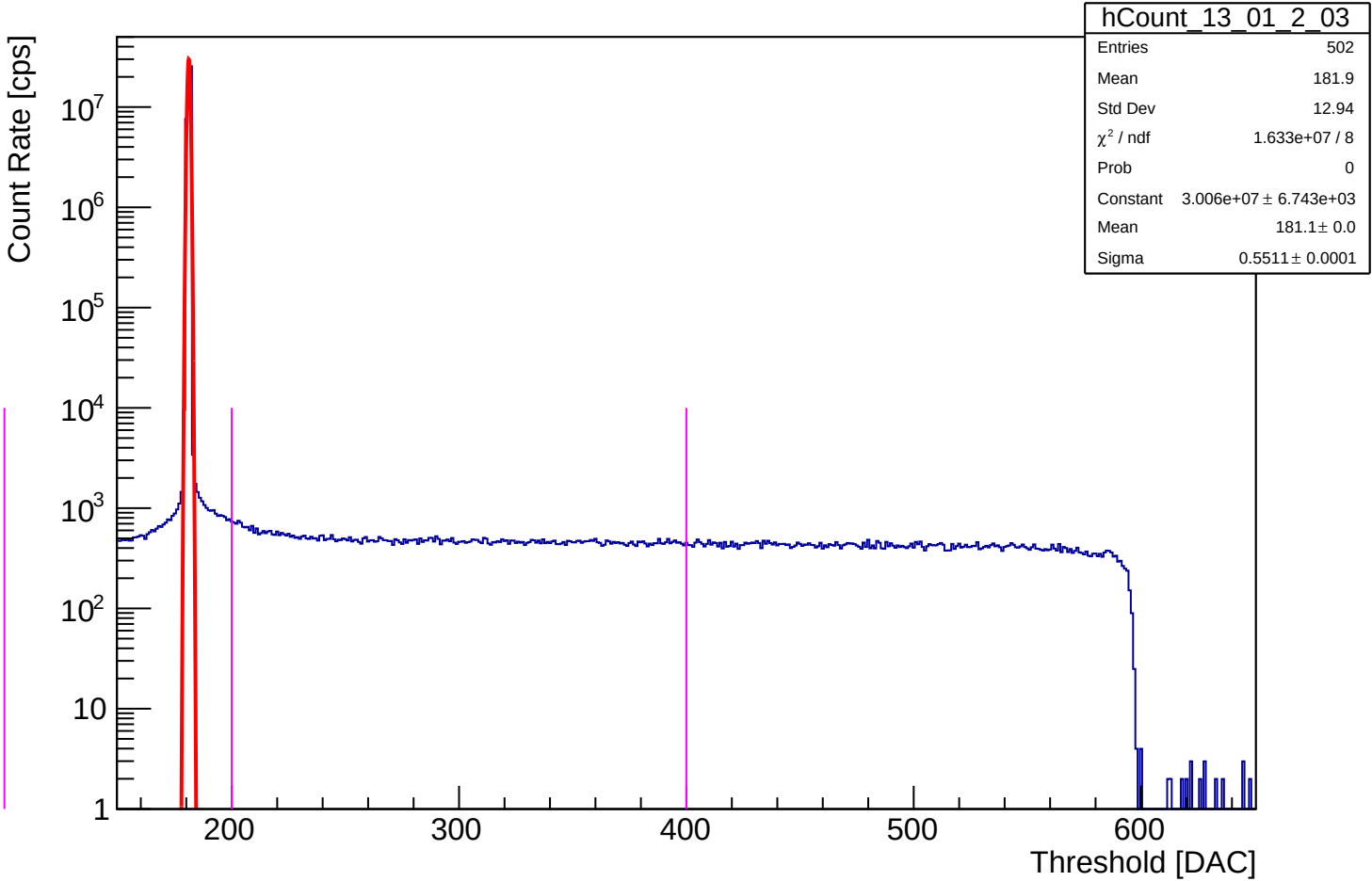
Row 1 Tile 1 Pmt 6 Pixel 54 Slot 13 Fiber 1 Asic 2 Channel 58



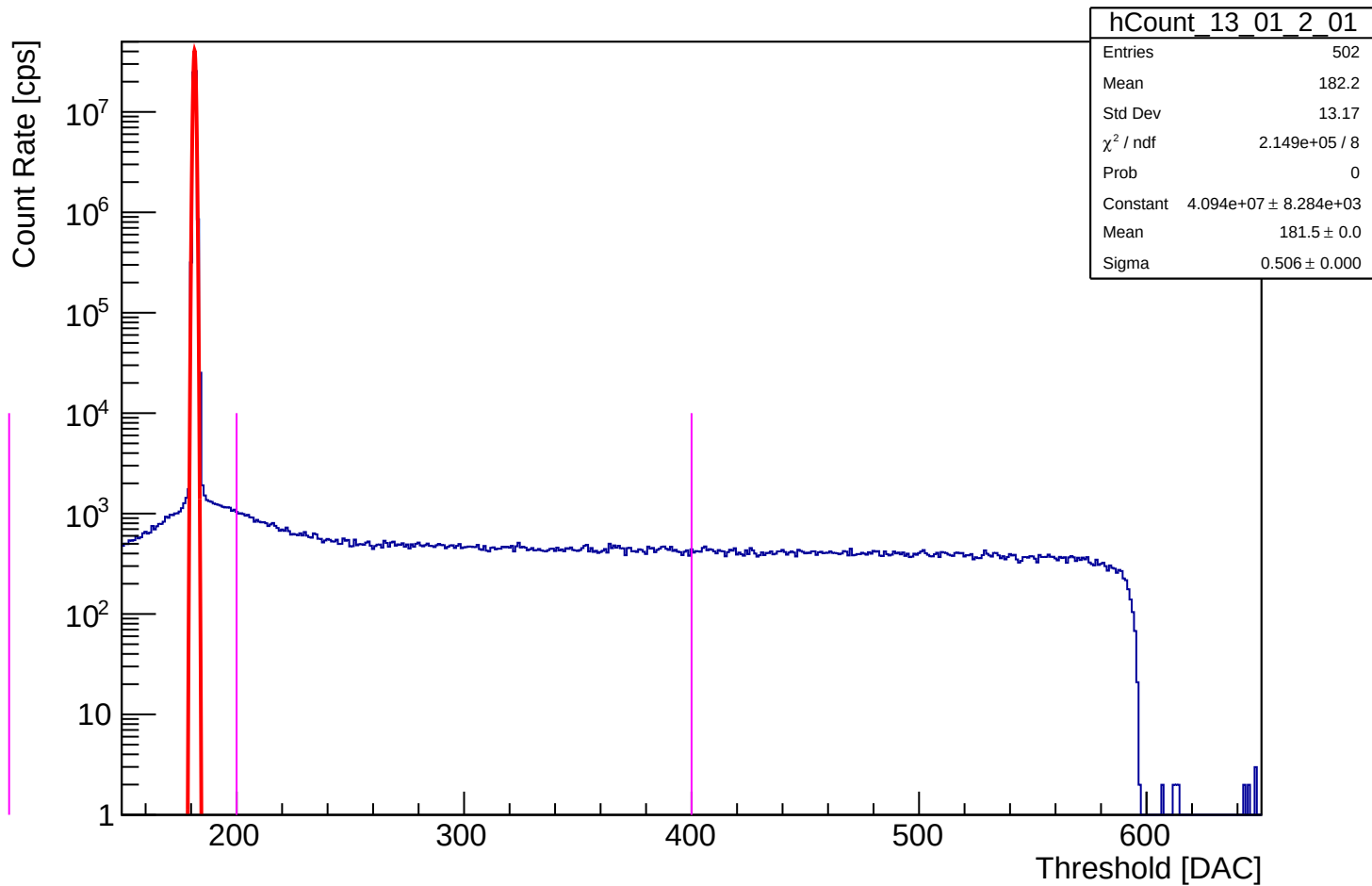
Row 1 Tile 1 Pmt 6 Pixel 55 Slot 13 Fiber 1 Asic 2 Channel 57

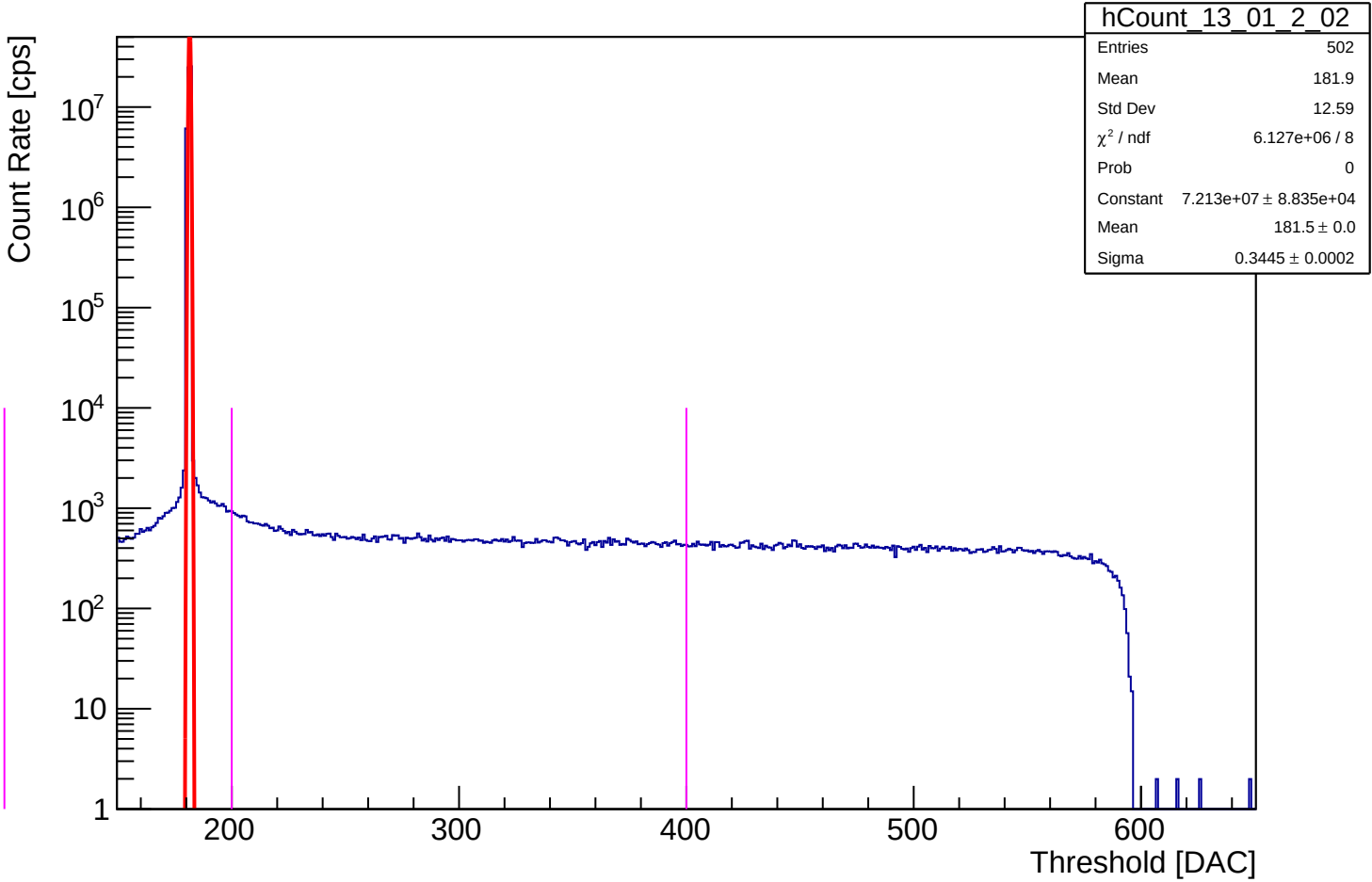


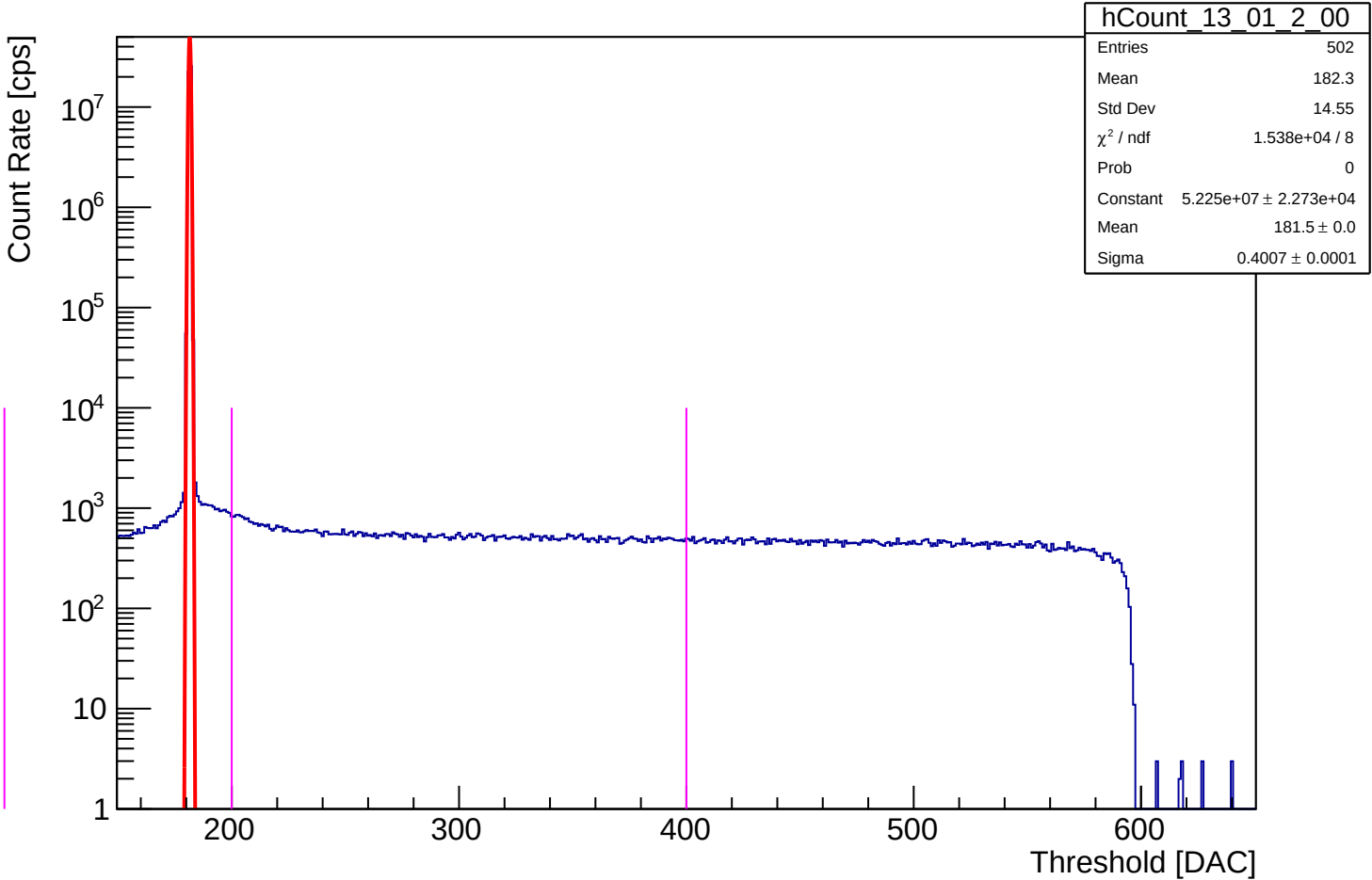




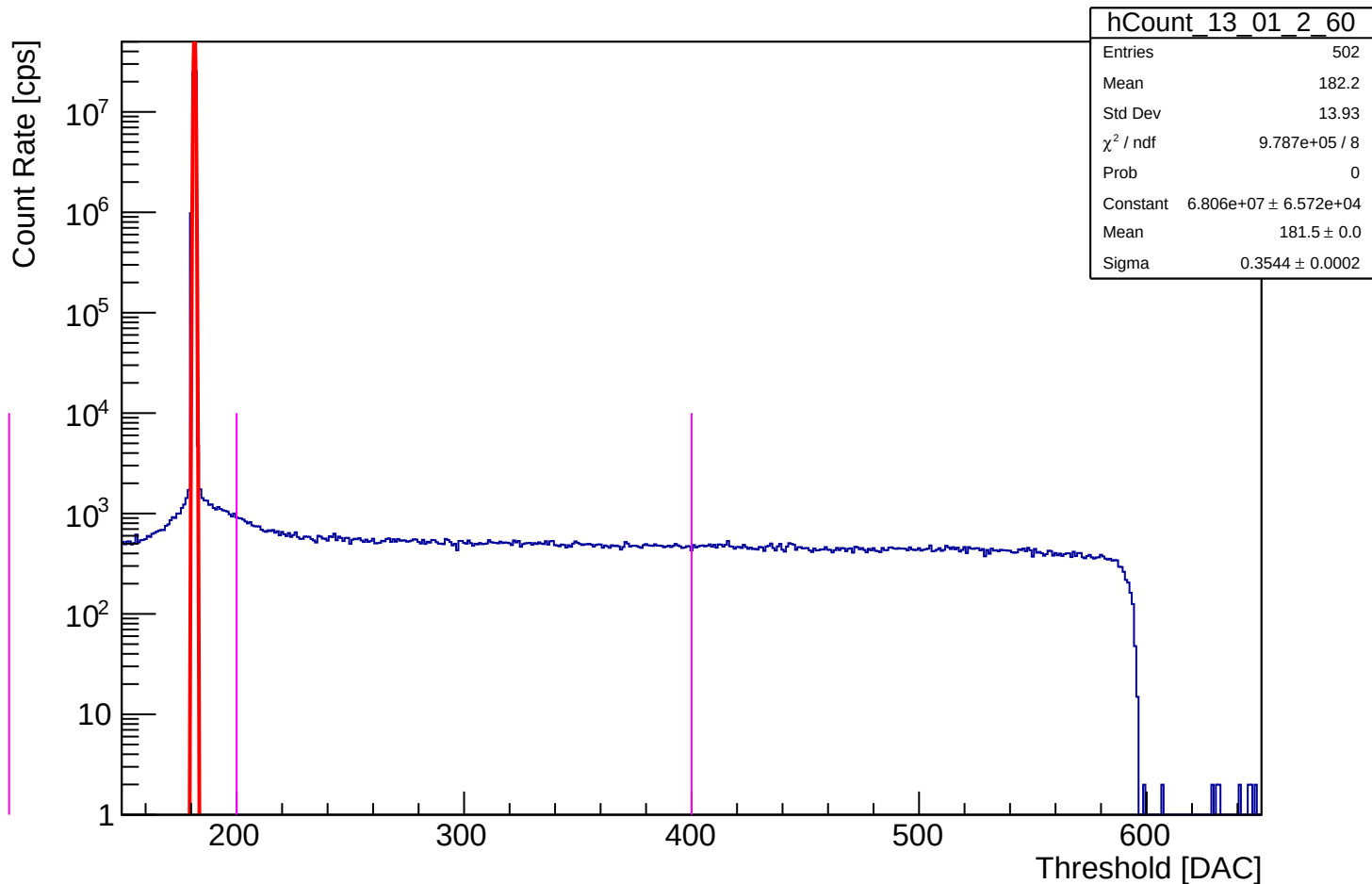
Row 1 Tile 1 Pmt 6 Pixel 58 Slot 13 Fiber 1 Asic 2 Channel 1



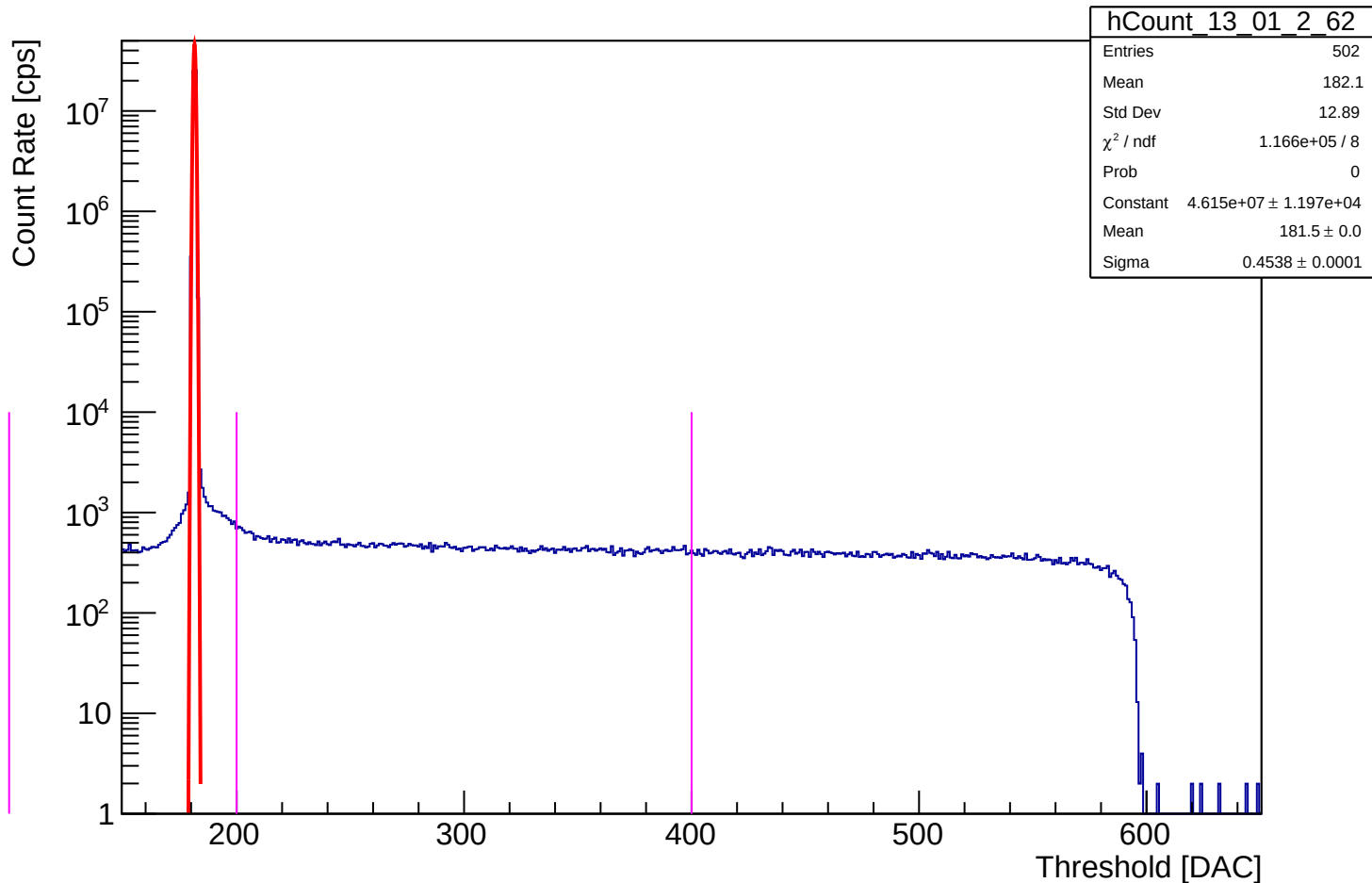




Row 1 Tile 1 Pmt 6 Pixel 61 Slot 13 Fiber 1 Asic 2 Channel 60



Row 1 Tile 1 Pmt 6 Pixel 62 Slot 13 Fiber 1 Asic 2 Channel 62



Row 1 Tile 1 Pmt 6 Pixel 63 Slot 13 Fiber 1 Asic 2 Channel 61

