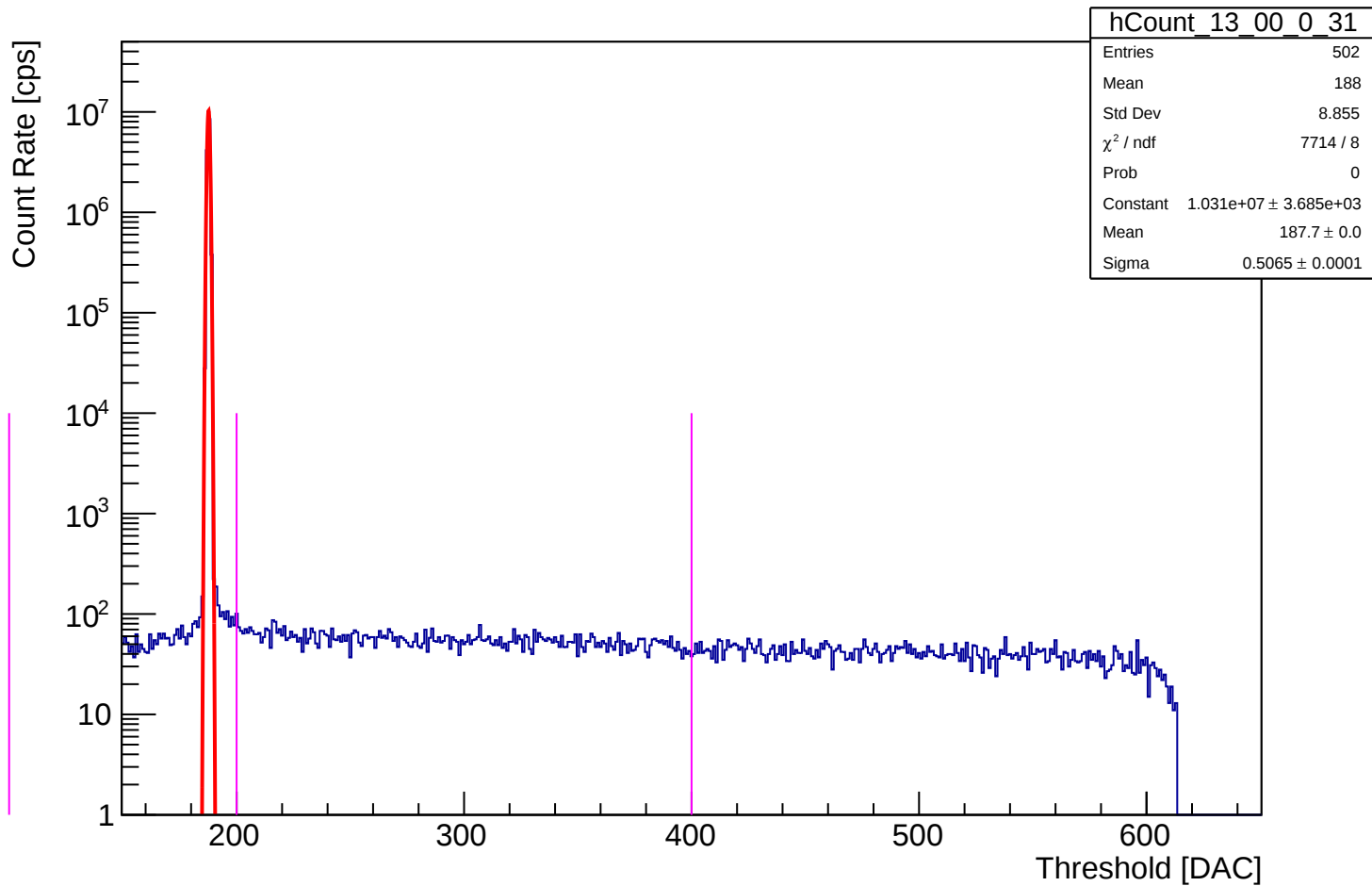
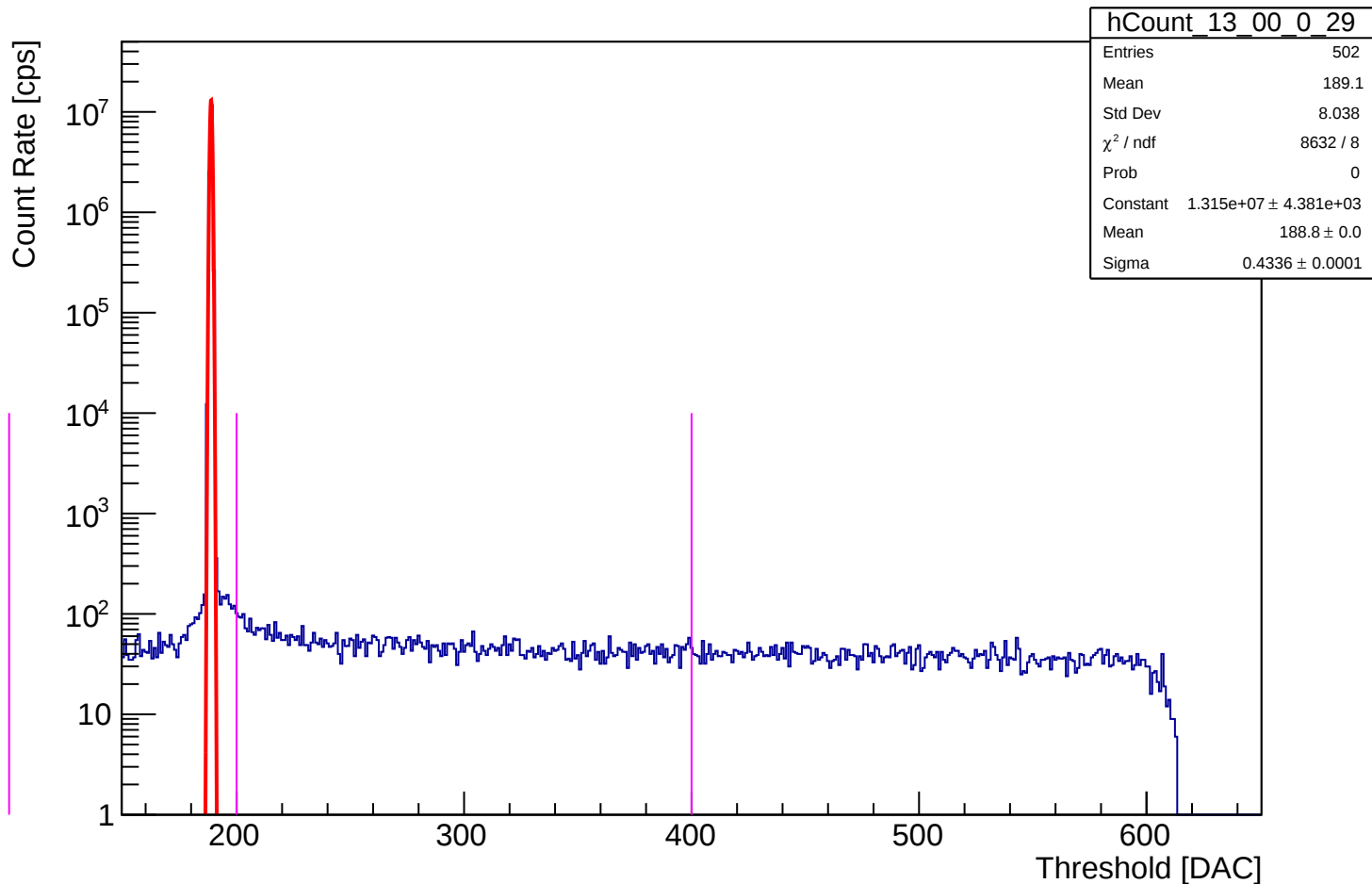


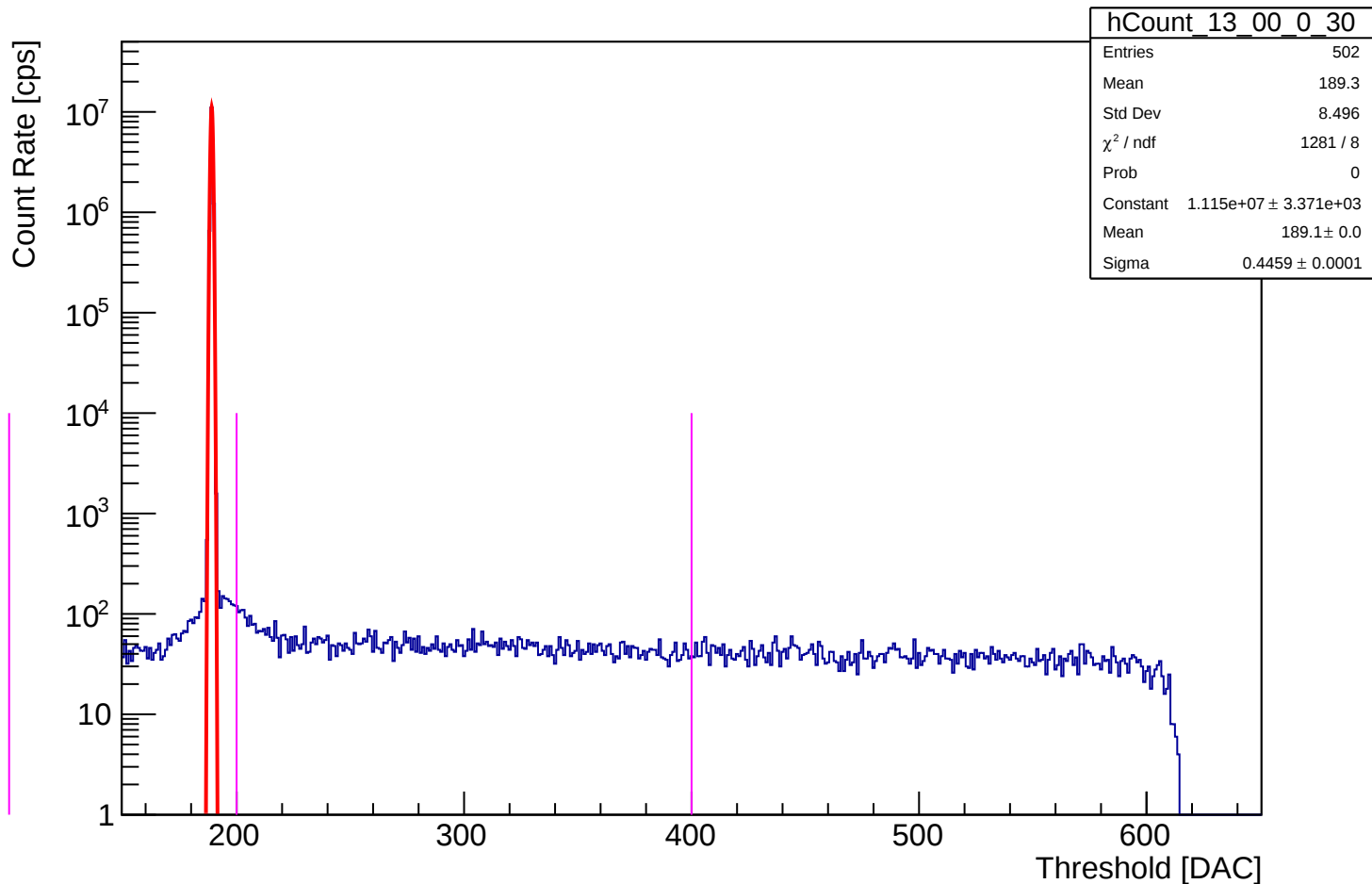
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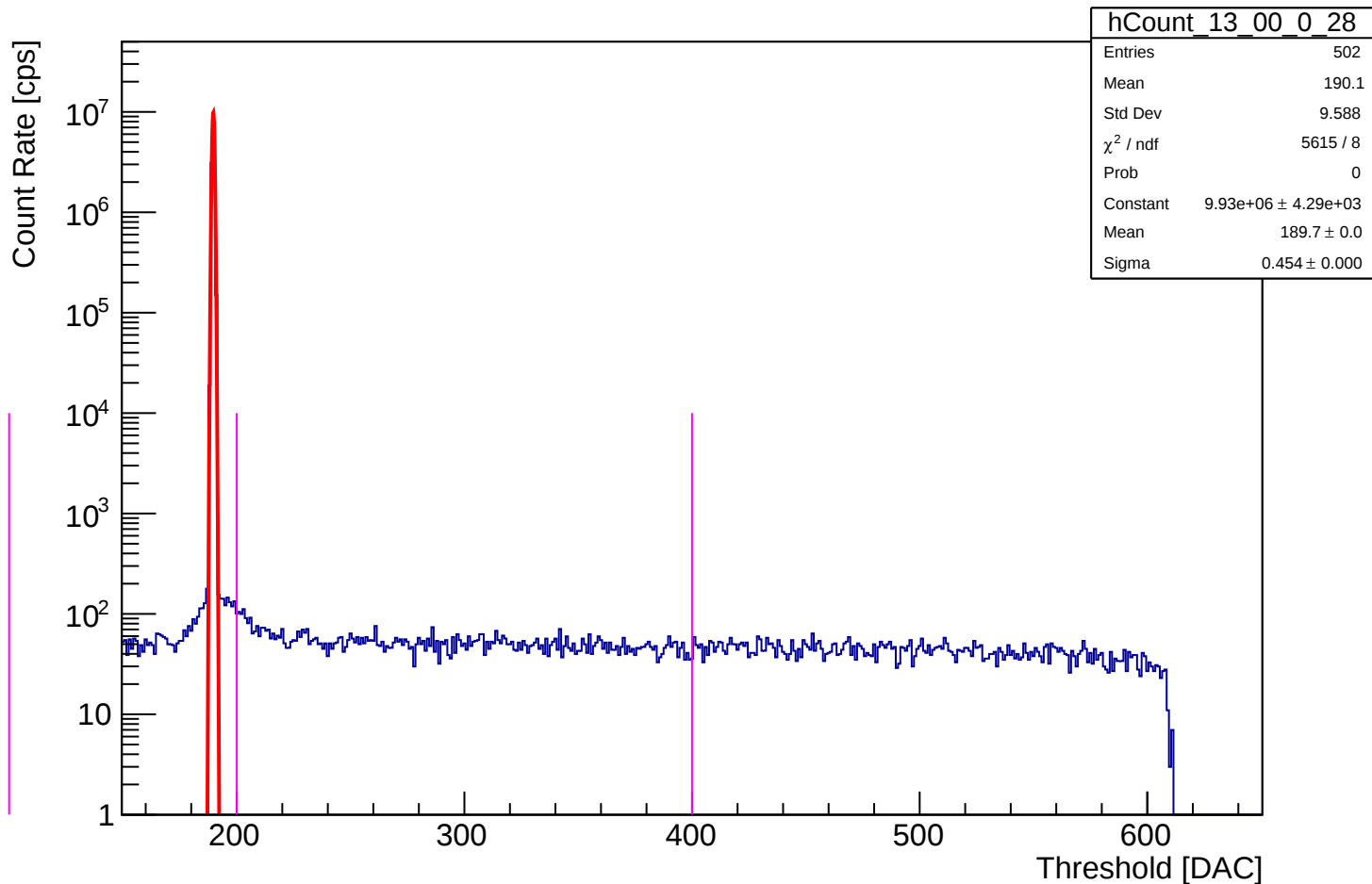
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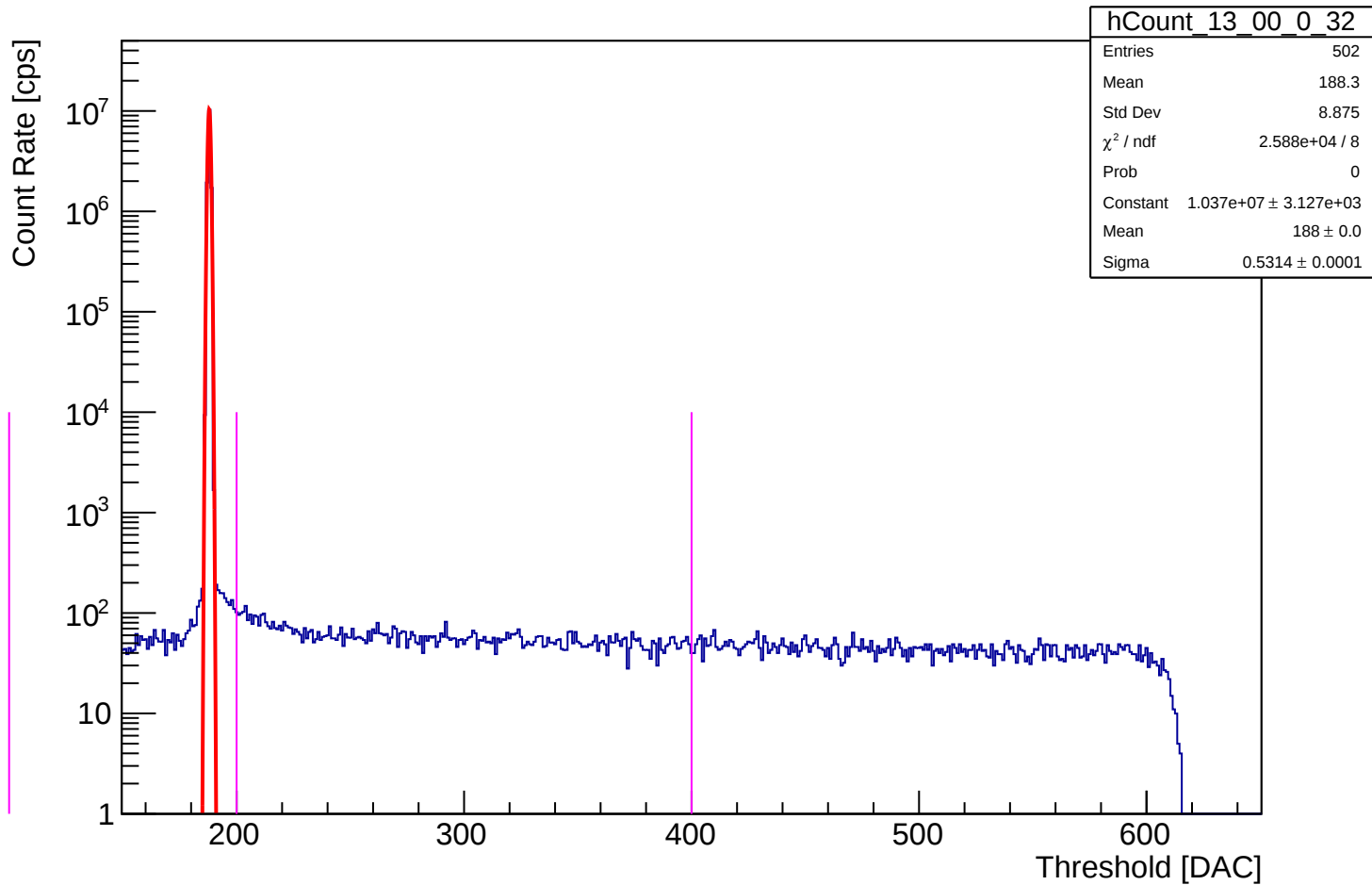
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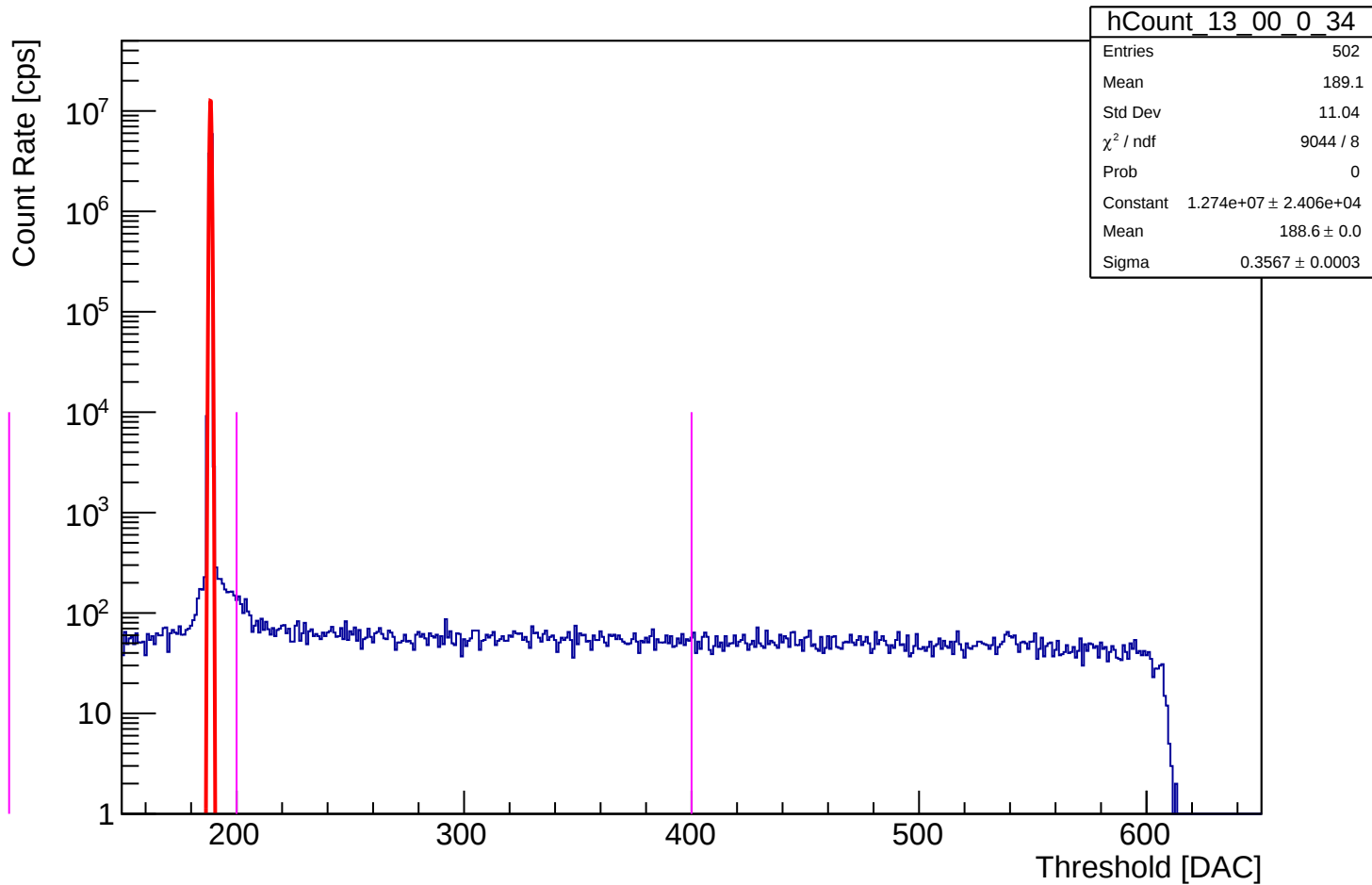
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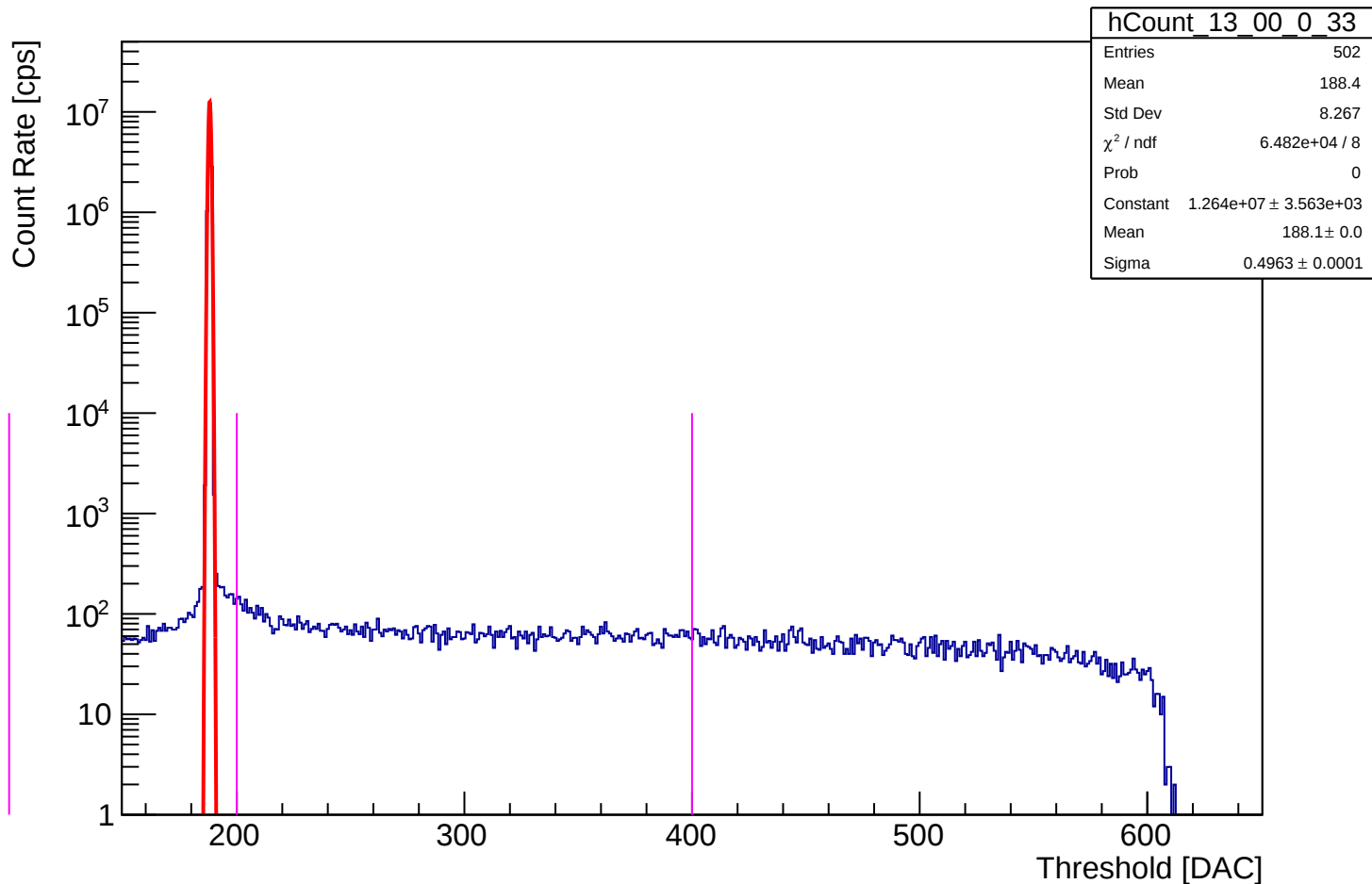
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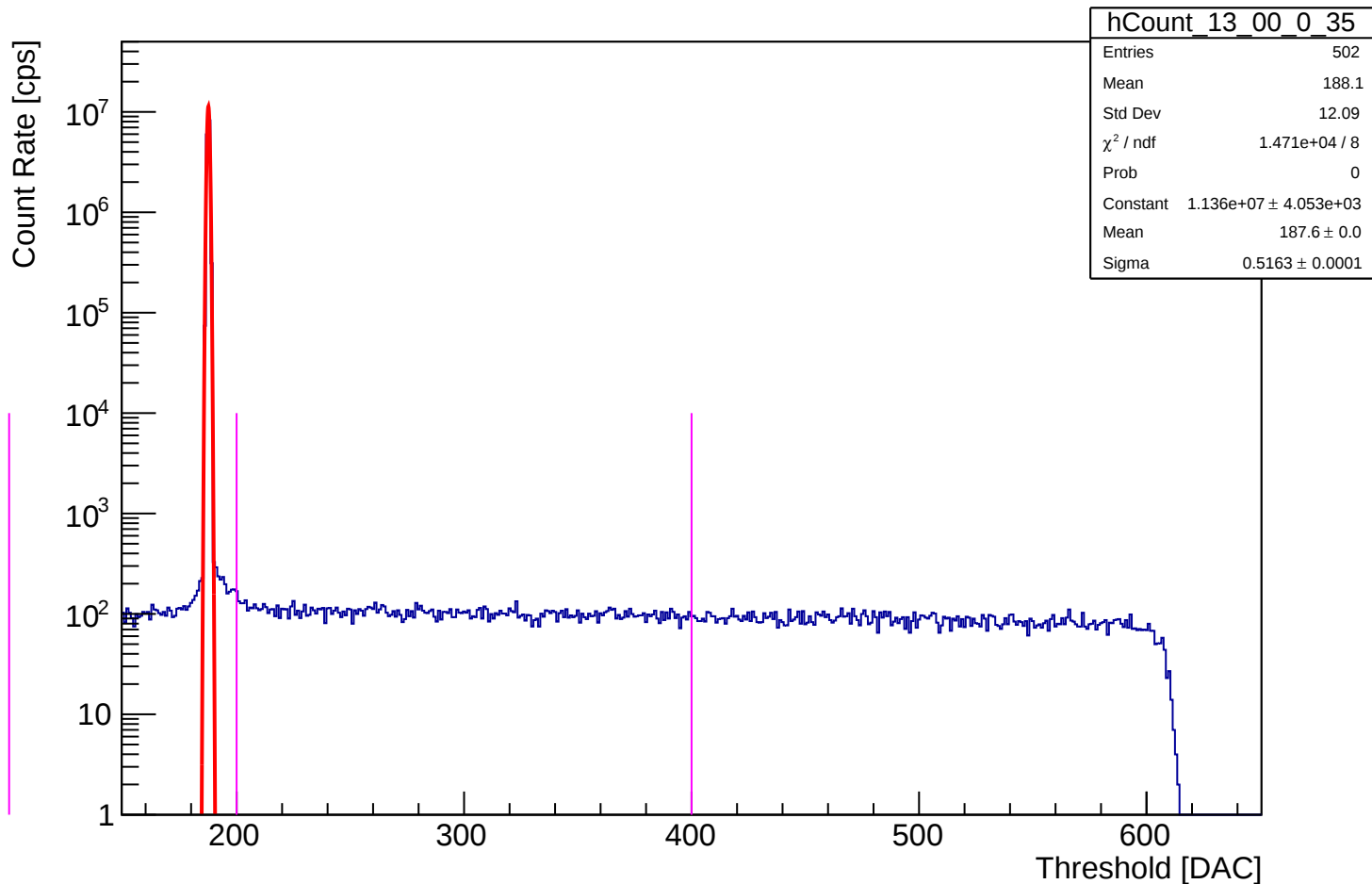
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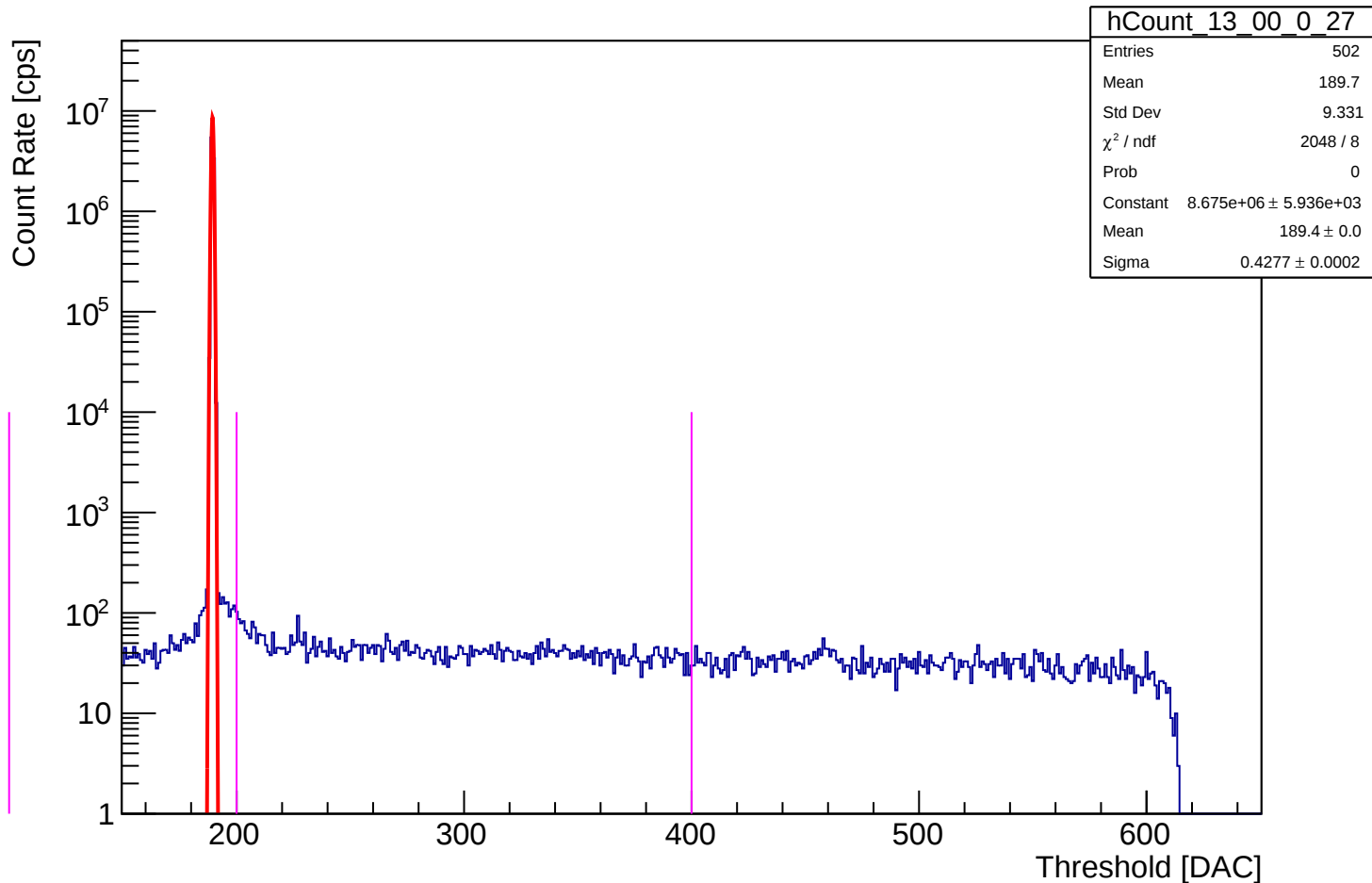
Row 1 Tile 1 Pmt 1 Pixel 7 Slot 13 Fiber 0 Asic 0 Channel 33



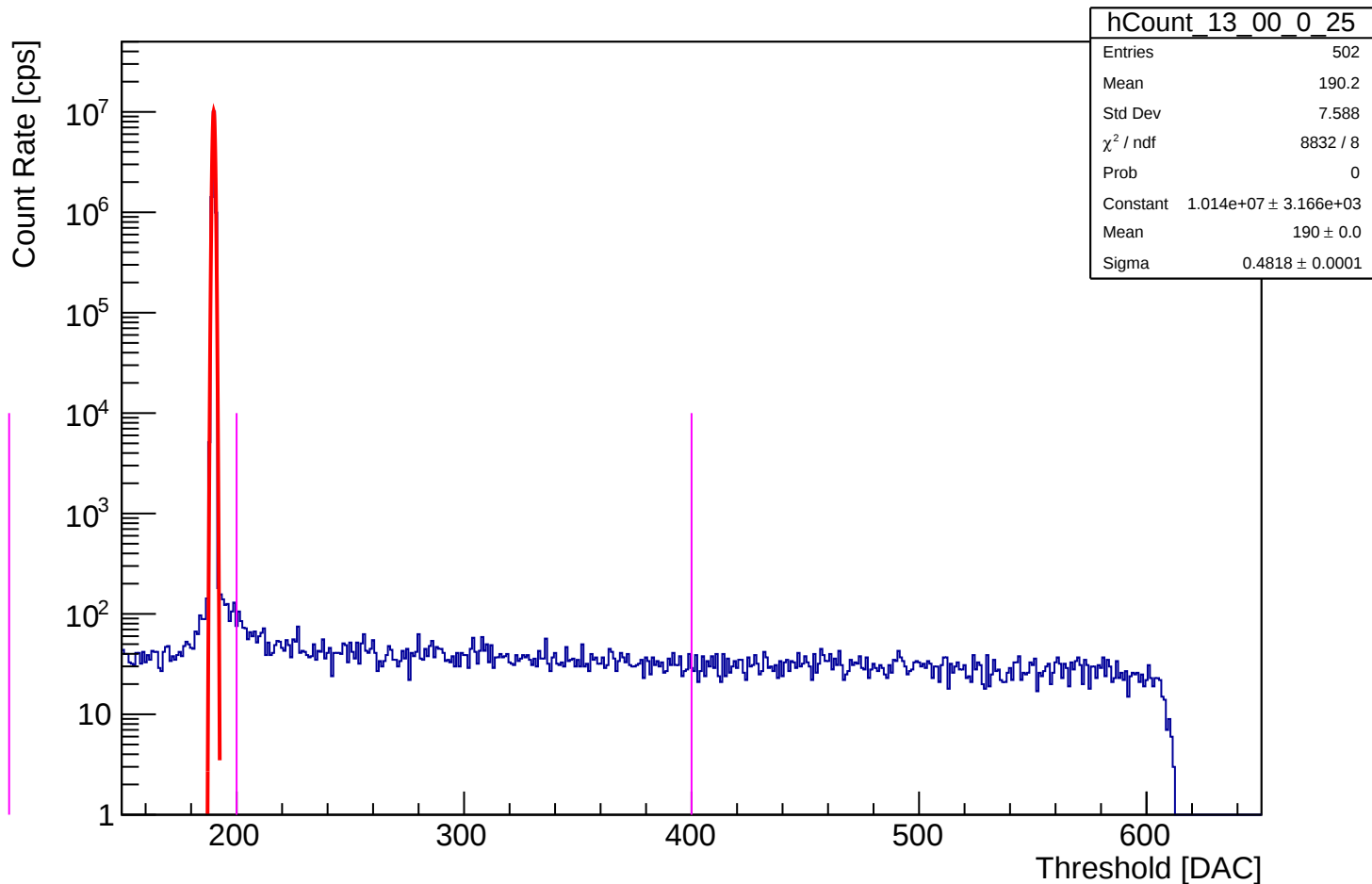
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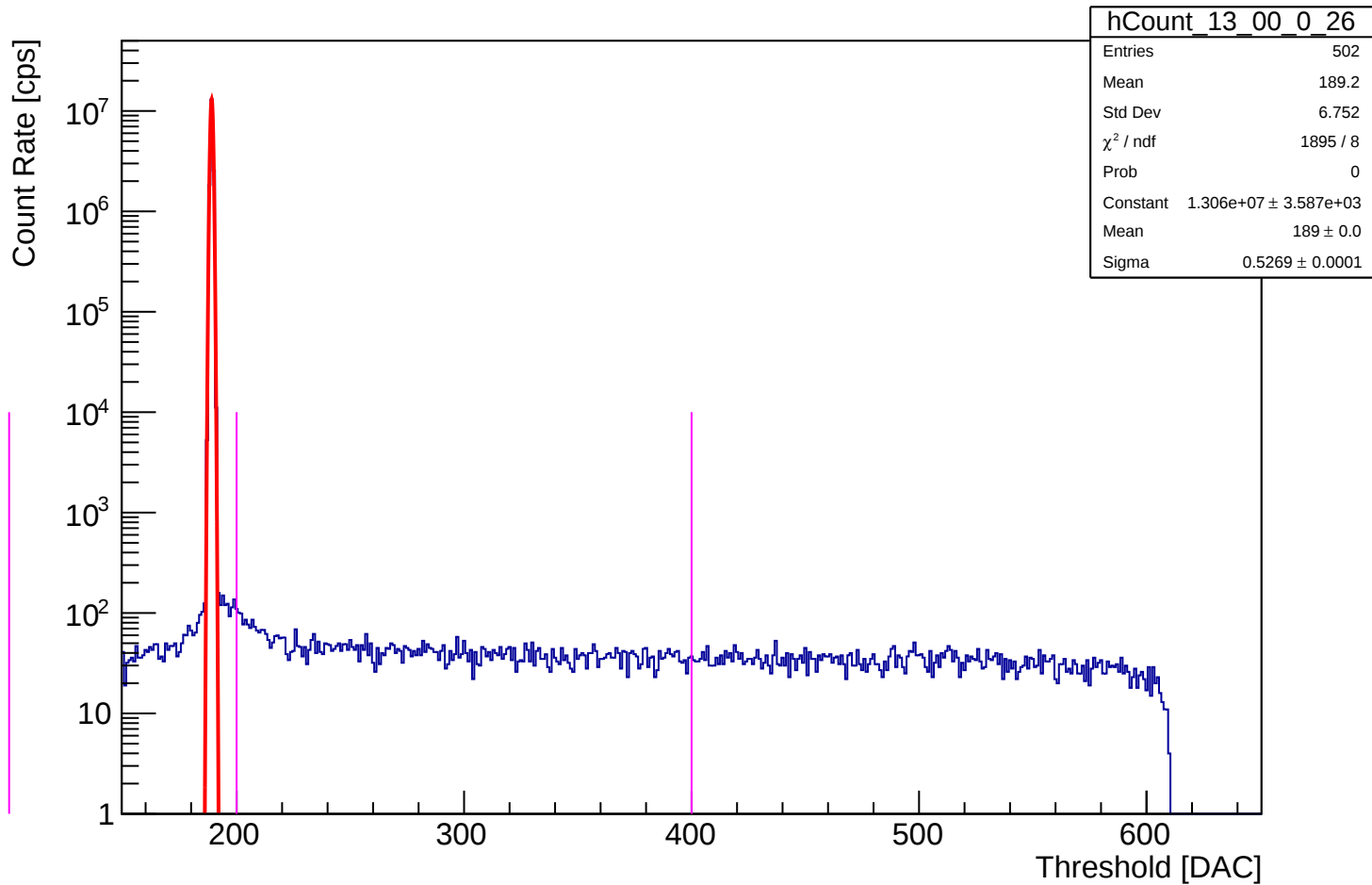
Row 1 Tile 1 Pmt 1 Pixel 9 Slot 13 Fiber 0 Asic 0 Channel 27



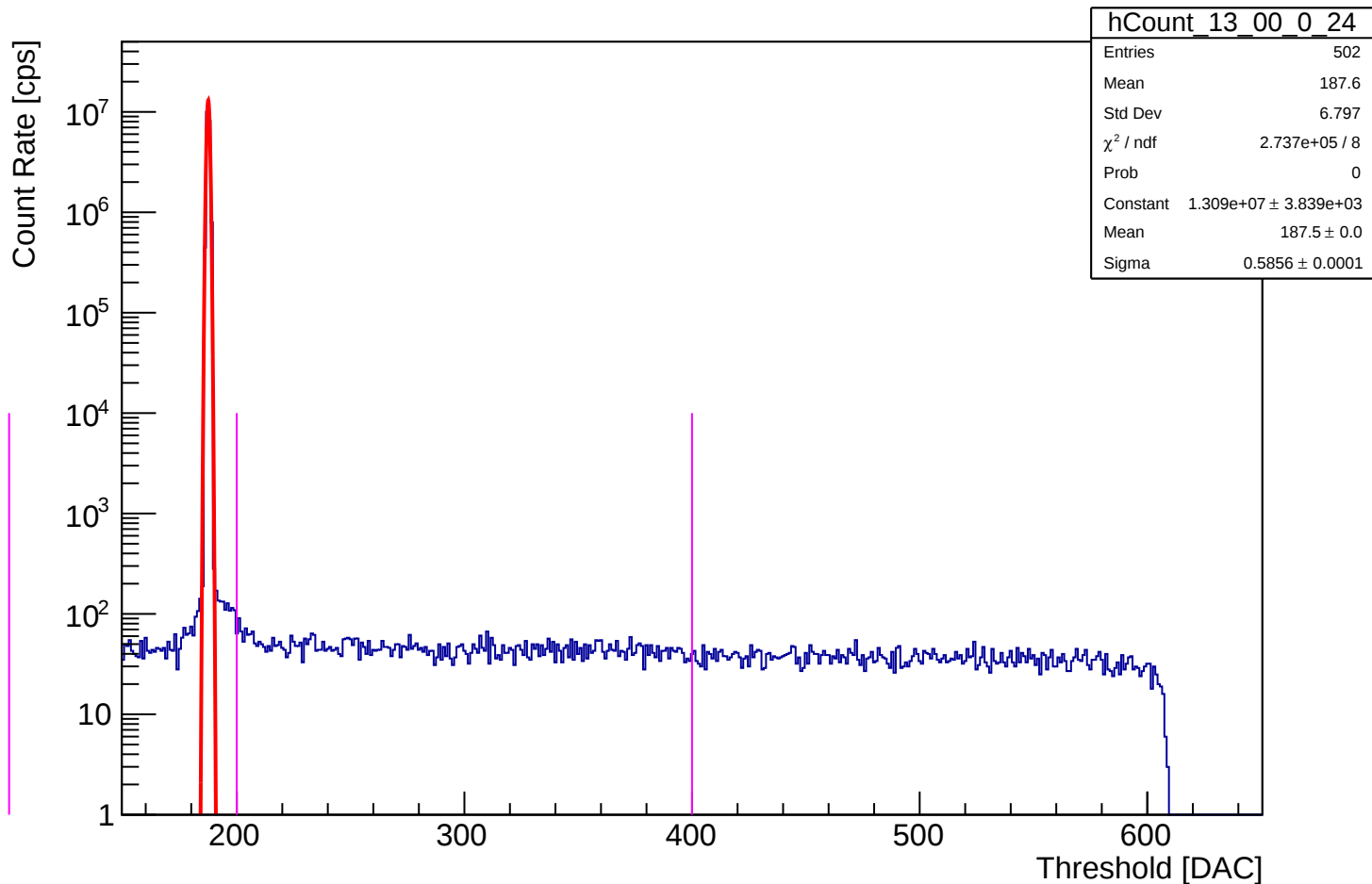
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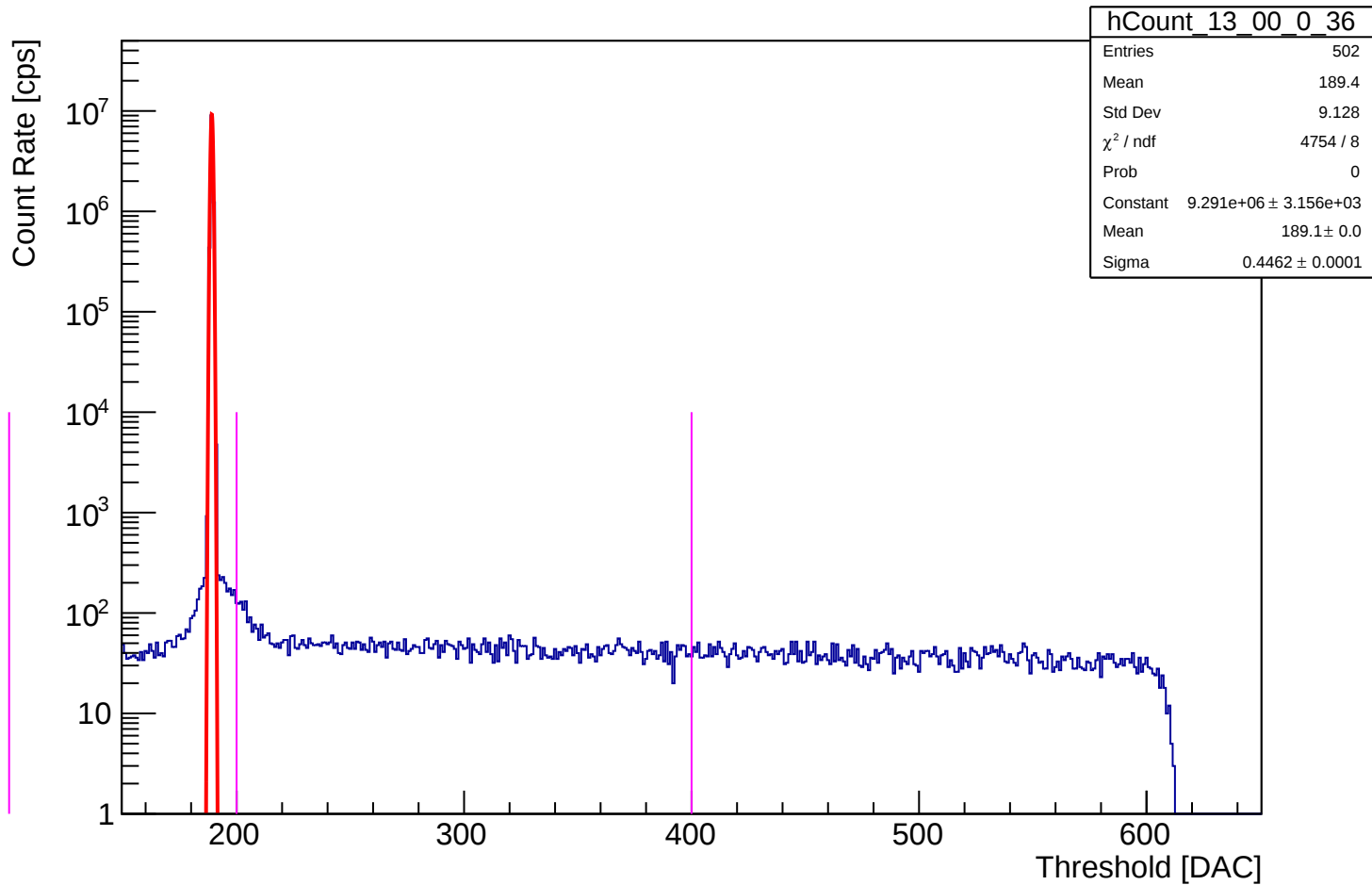
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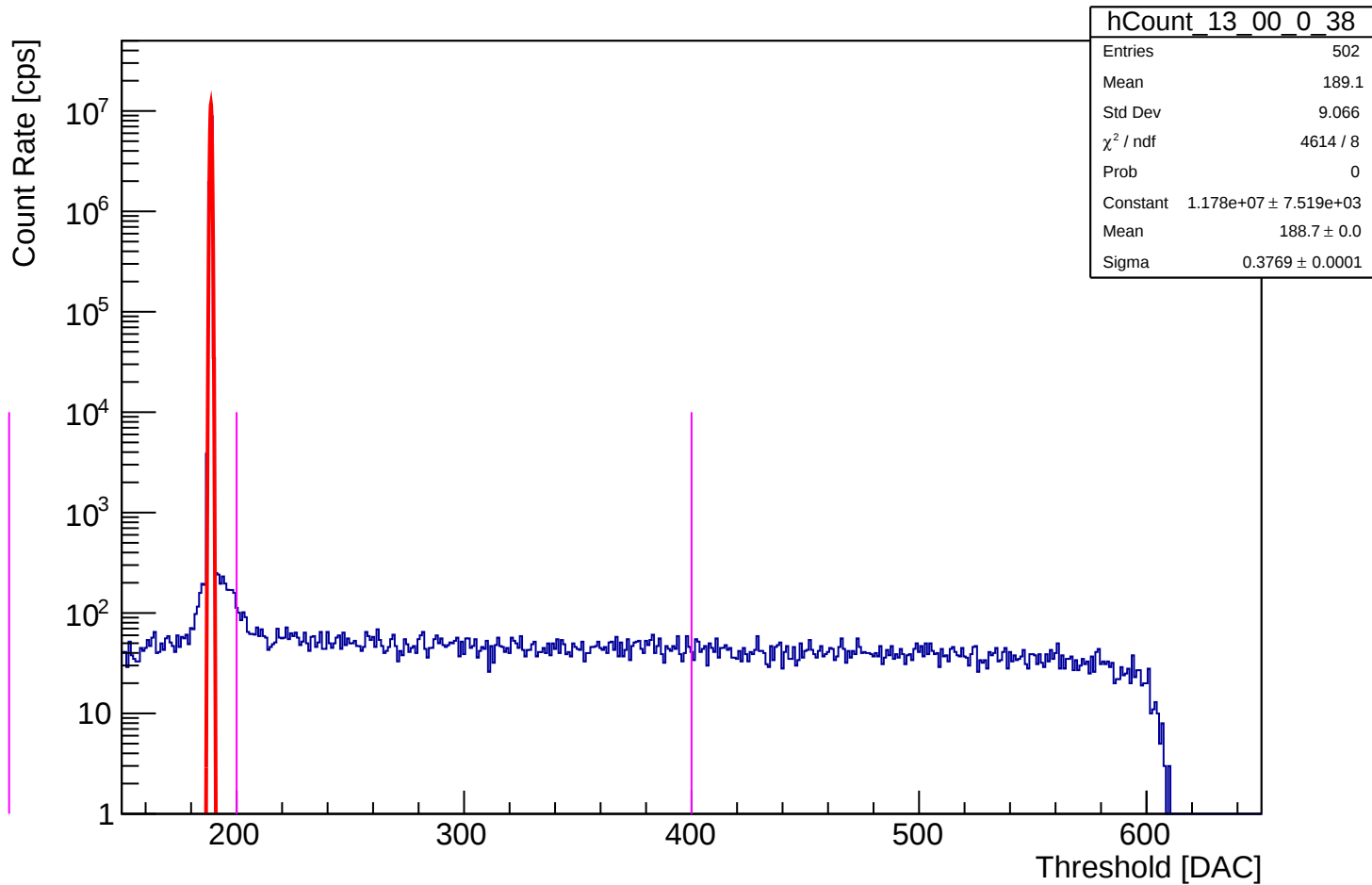
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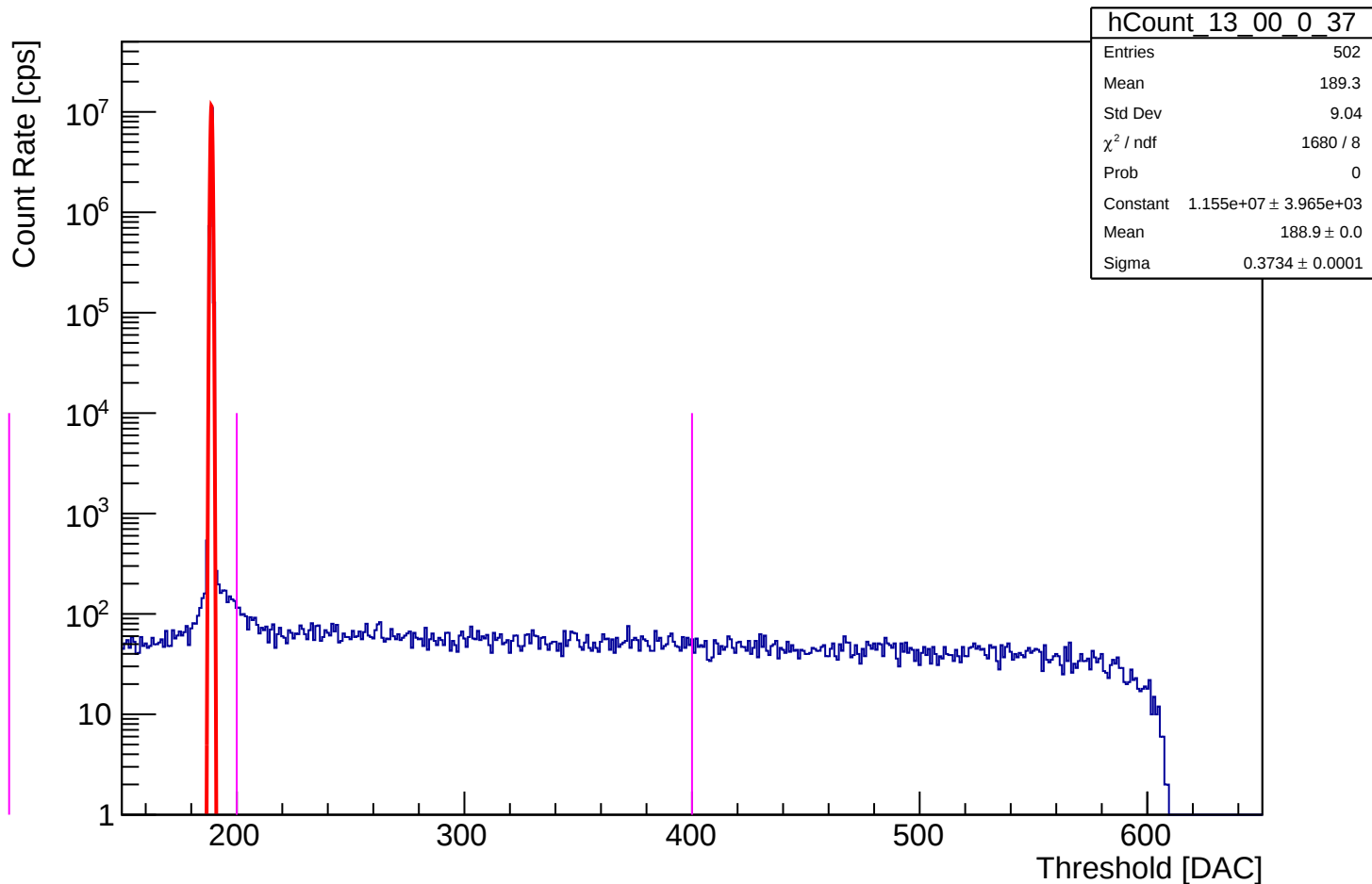
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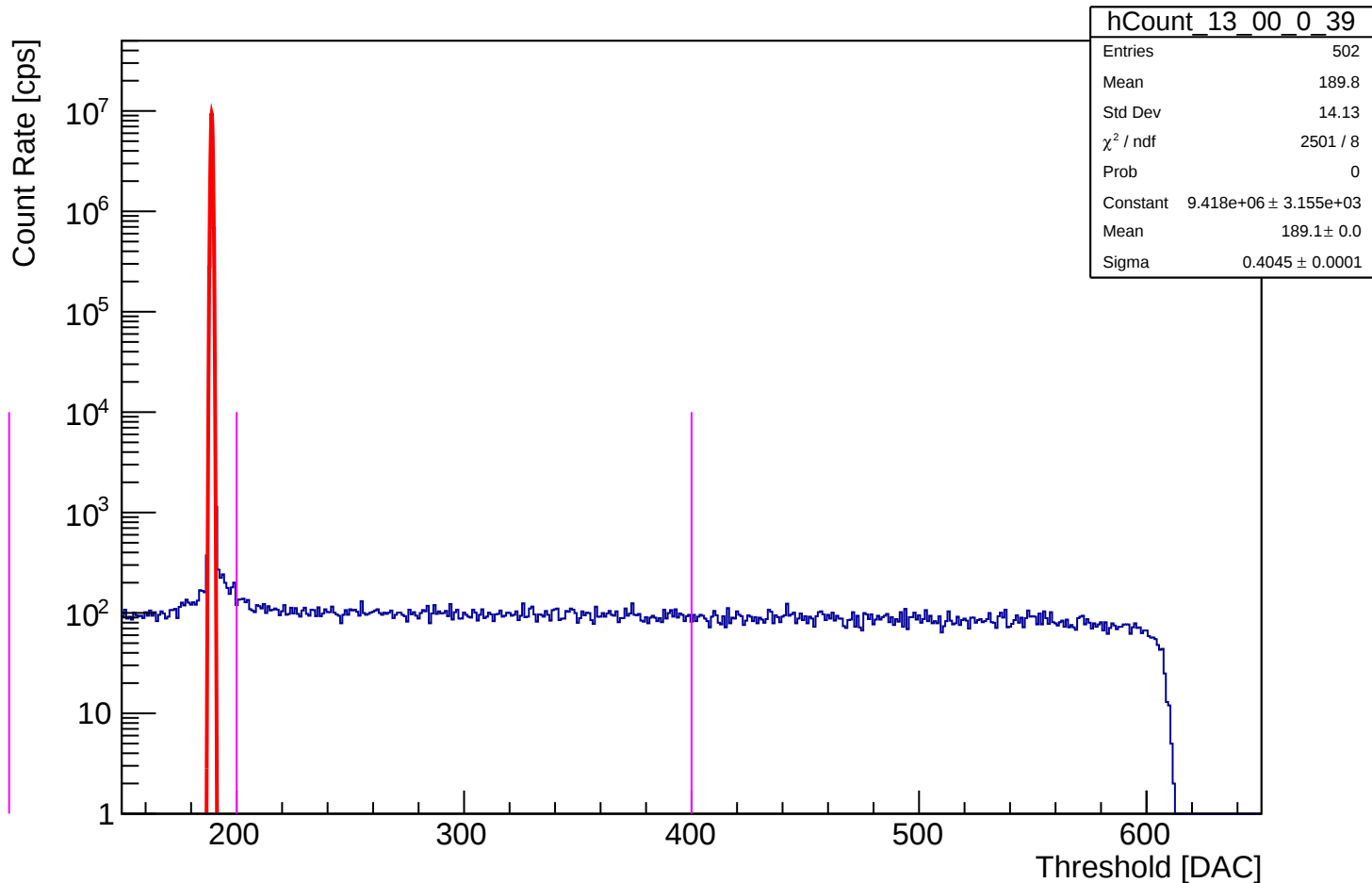
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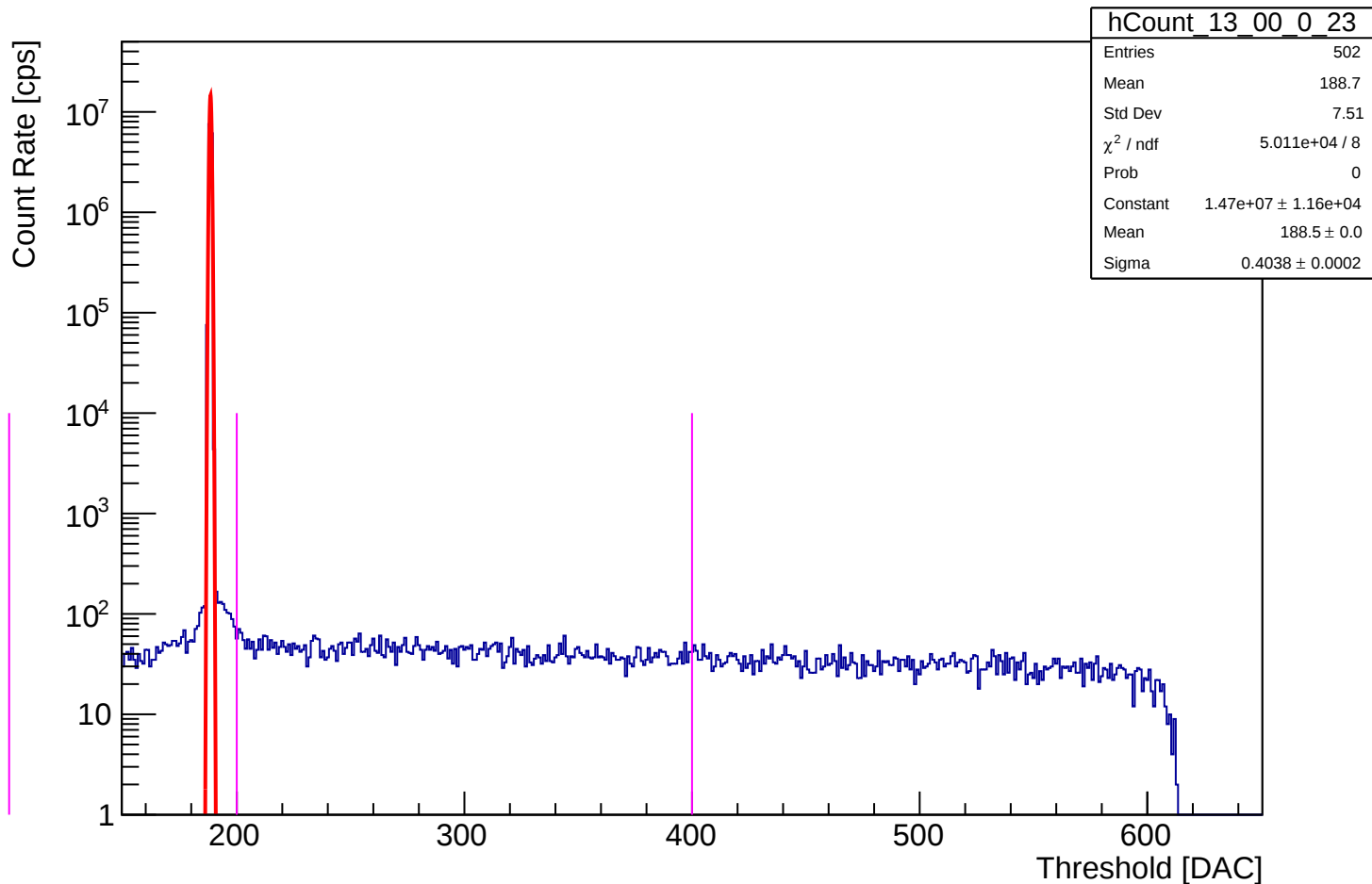
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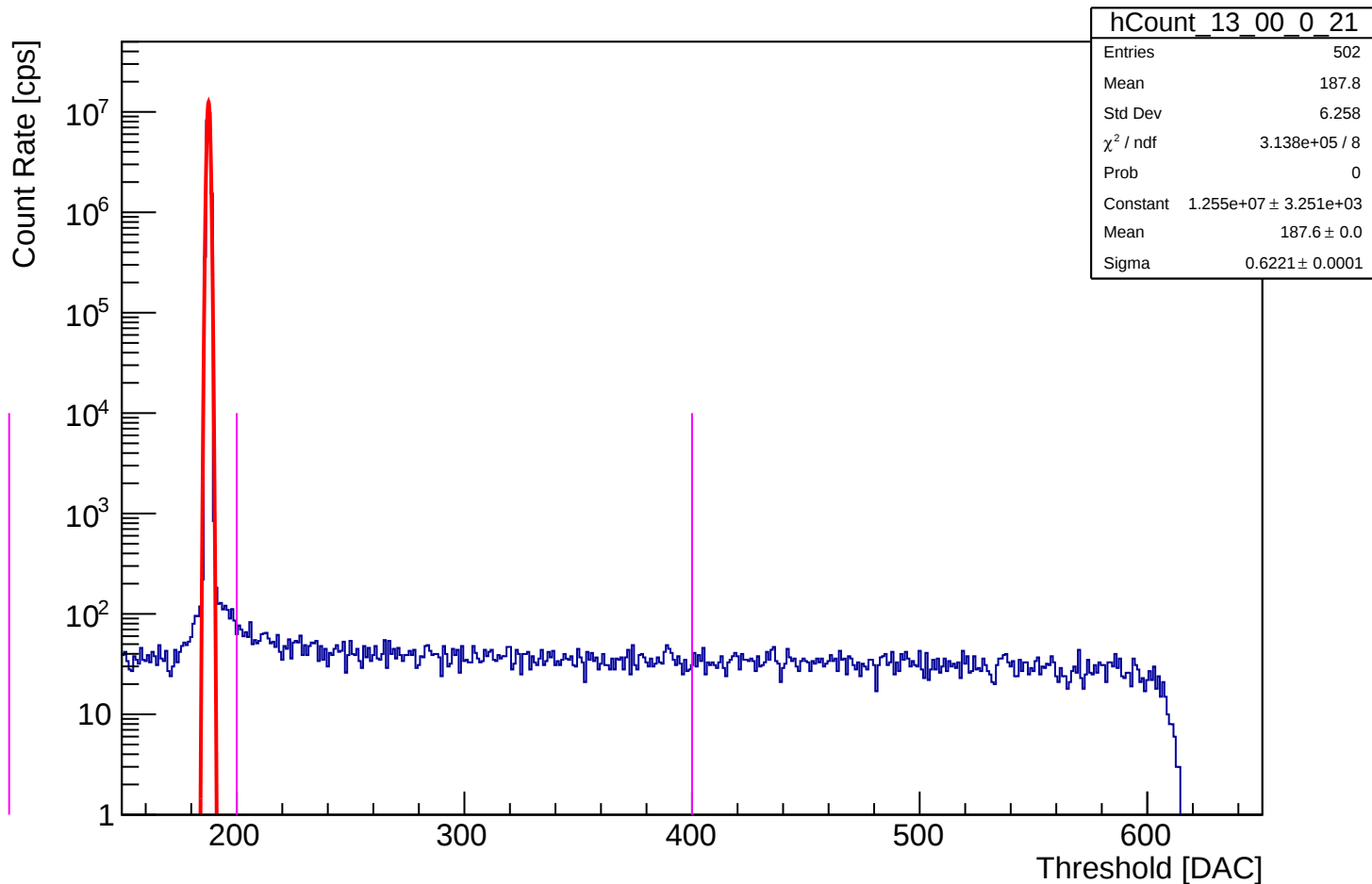
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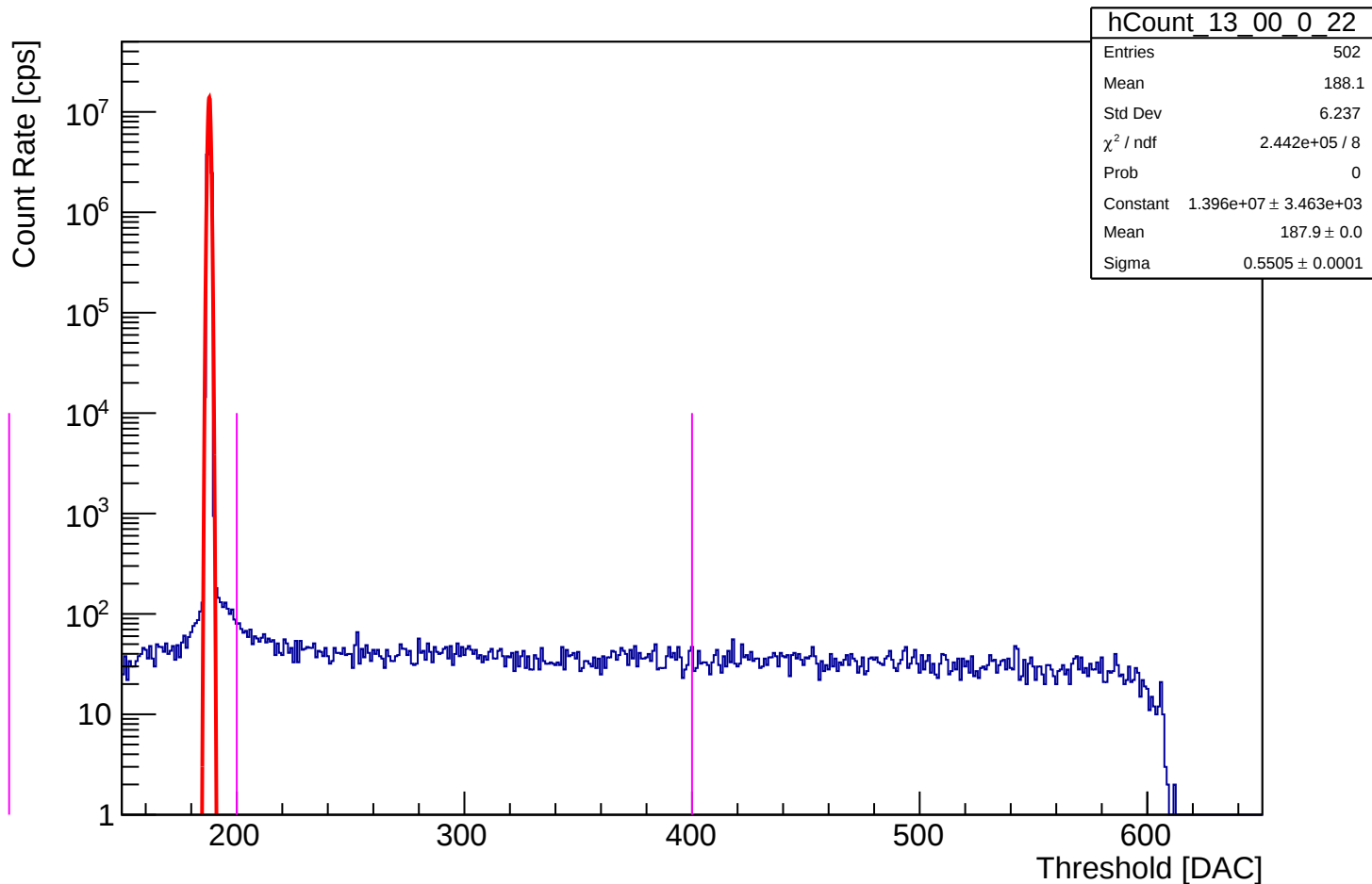
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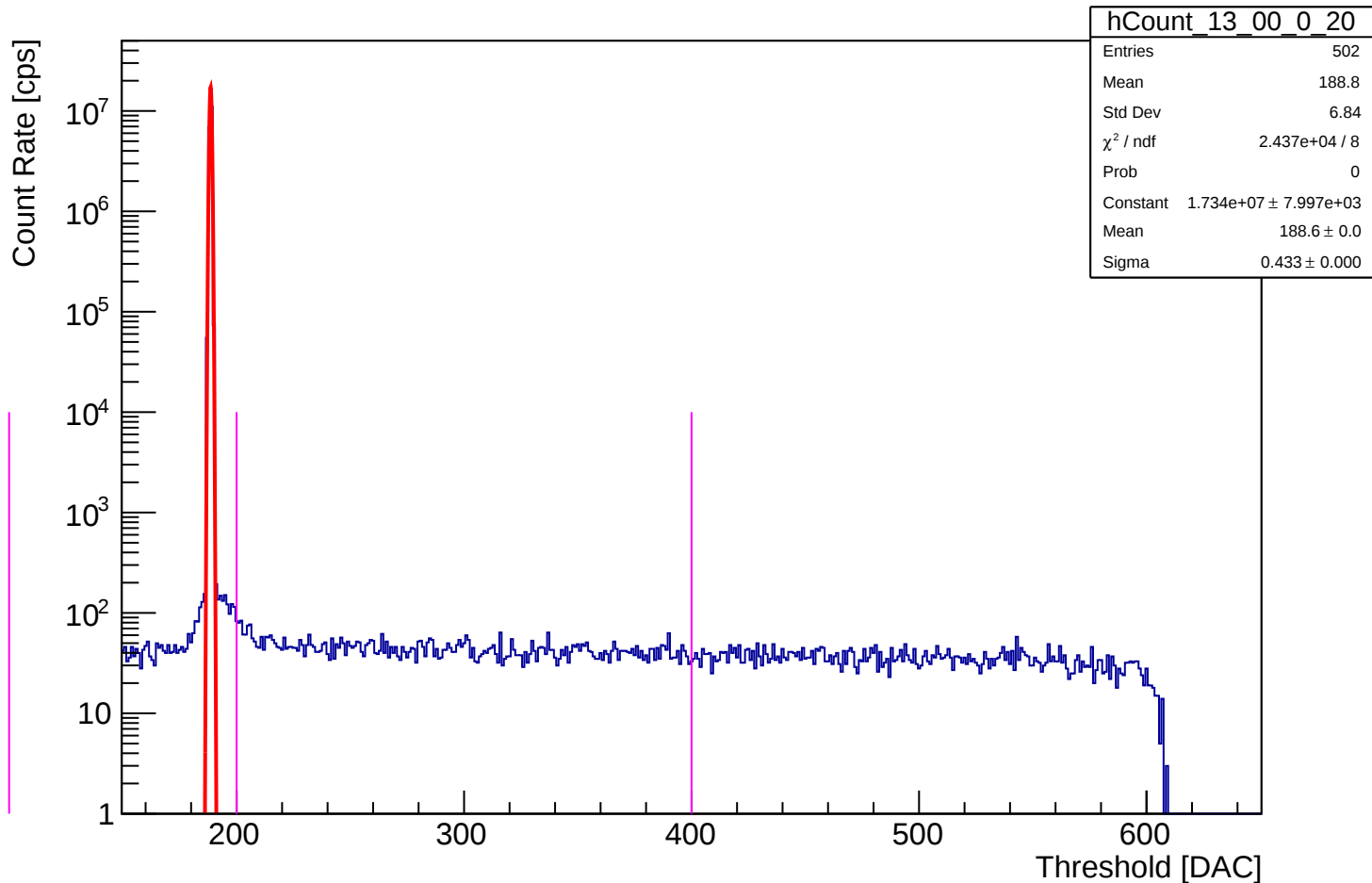
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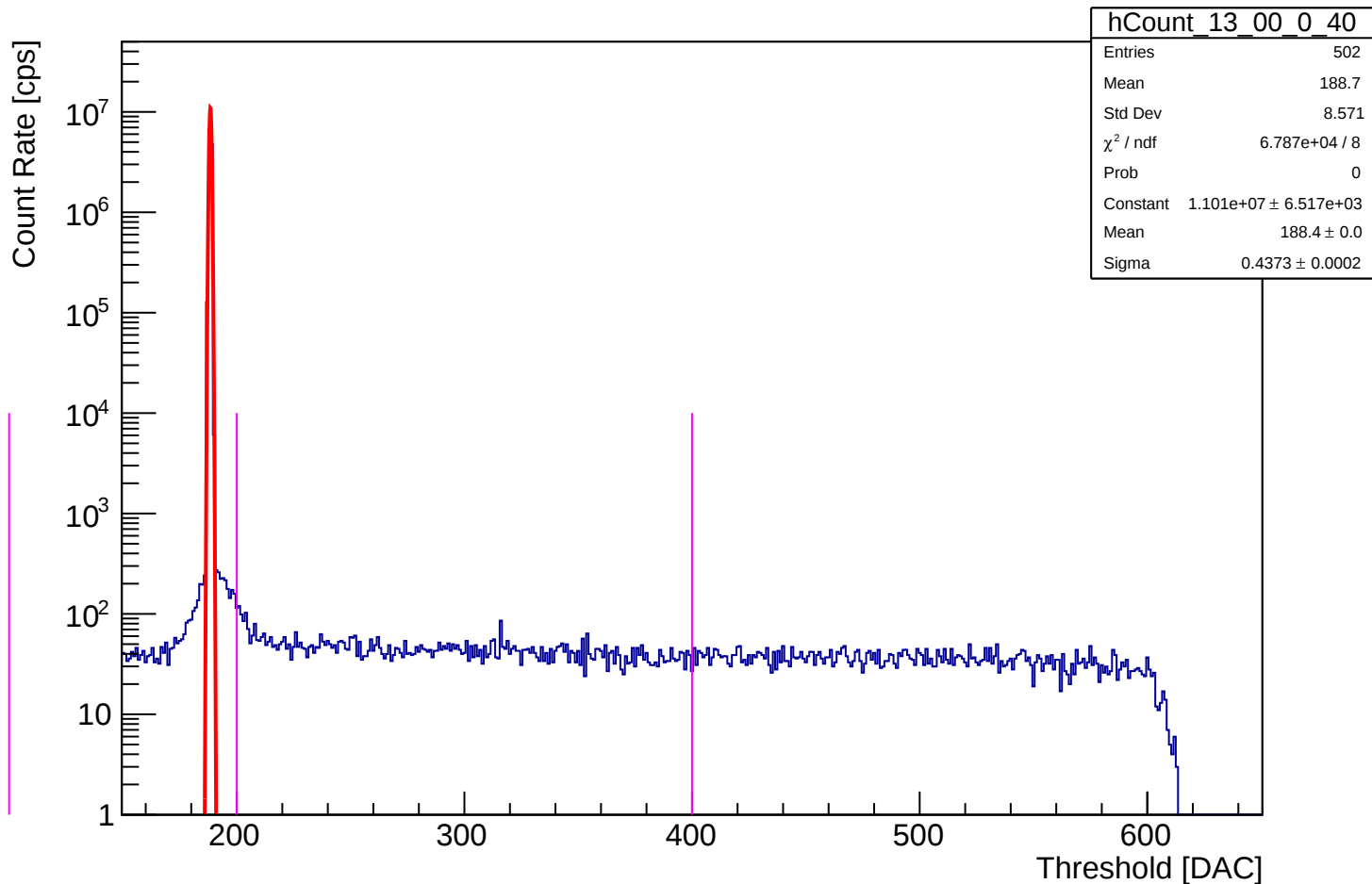
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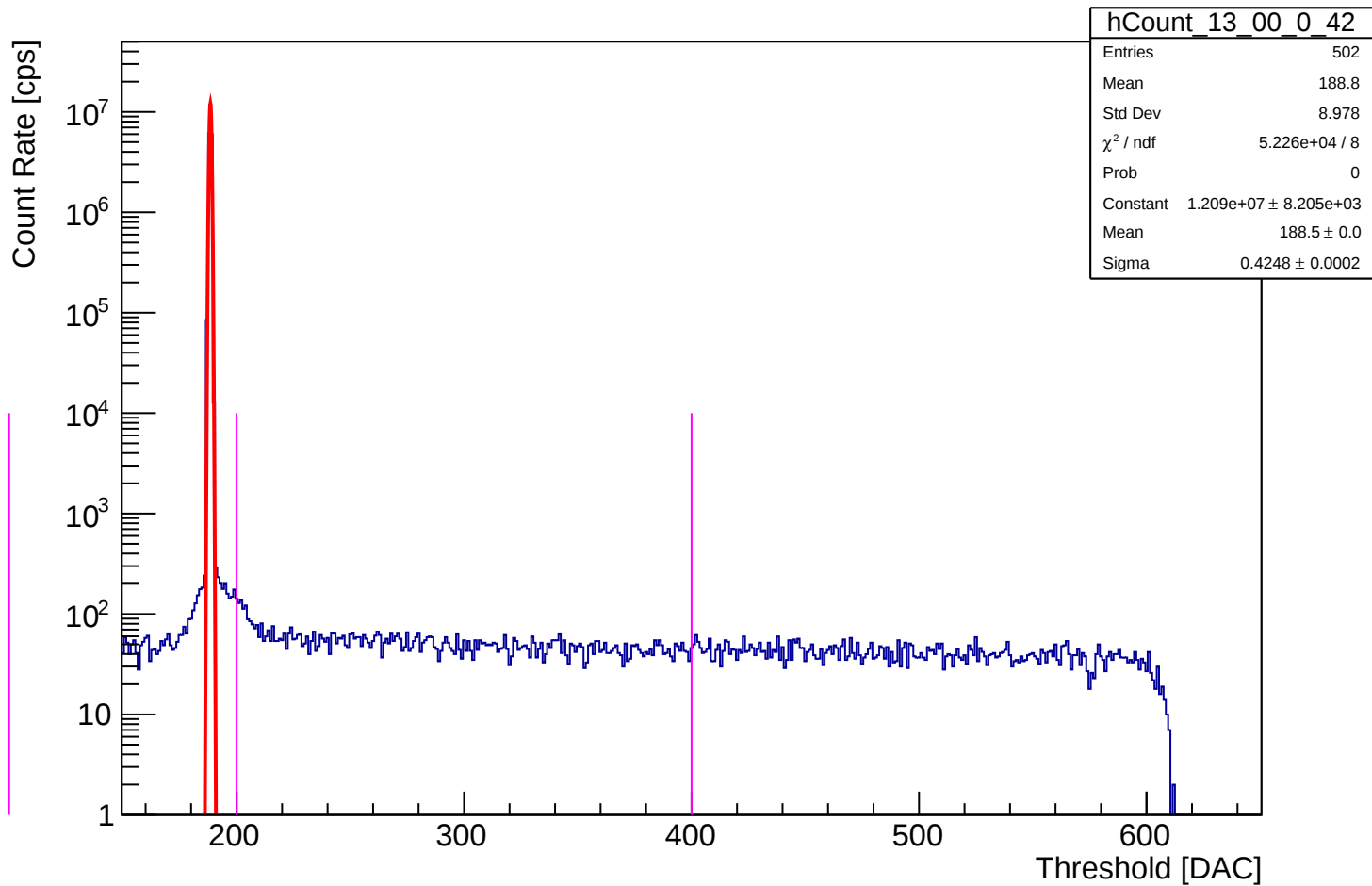
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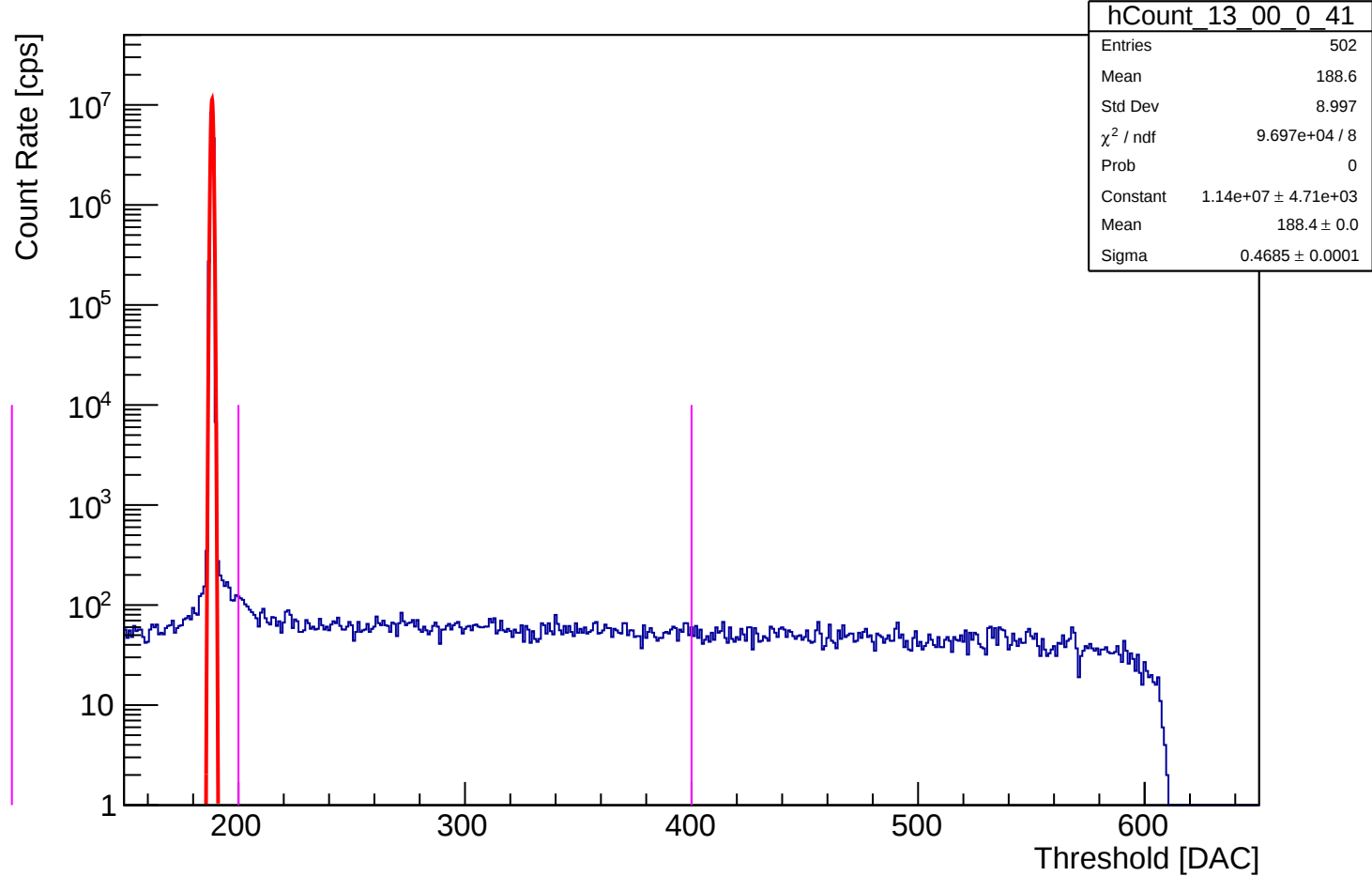


Row 1 Tile 1 Pmt 1 Pixel 21 Slot 13 Fiber 0 Asic 0 Channel 40

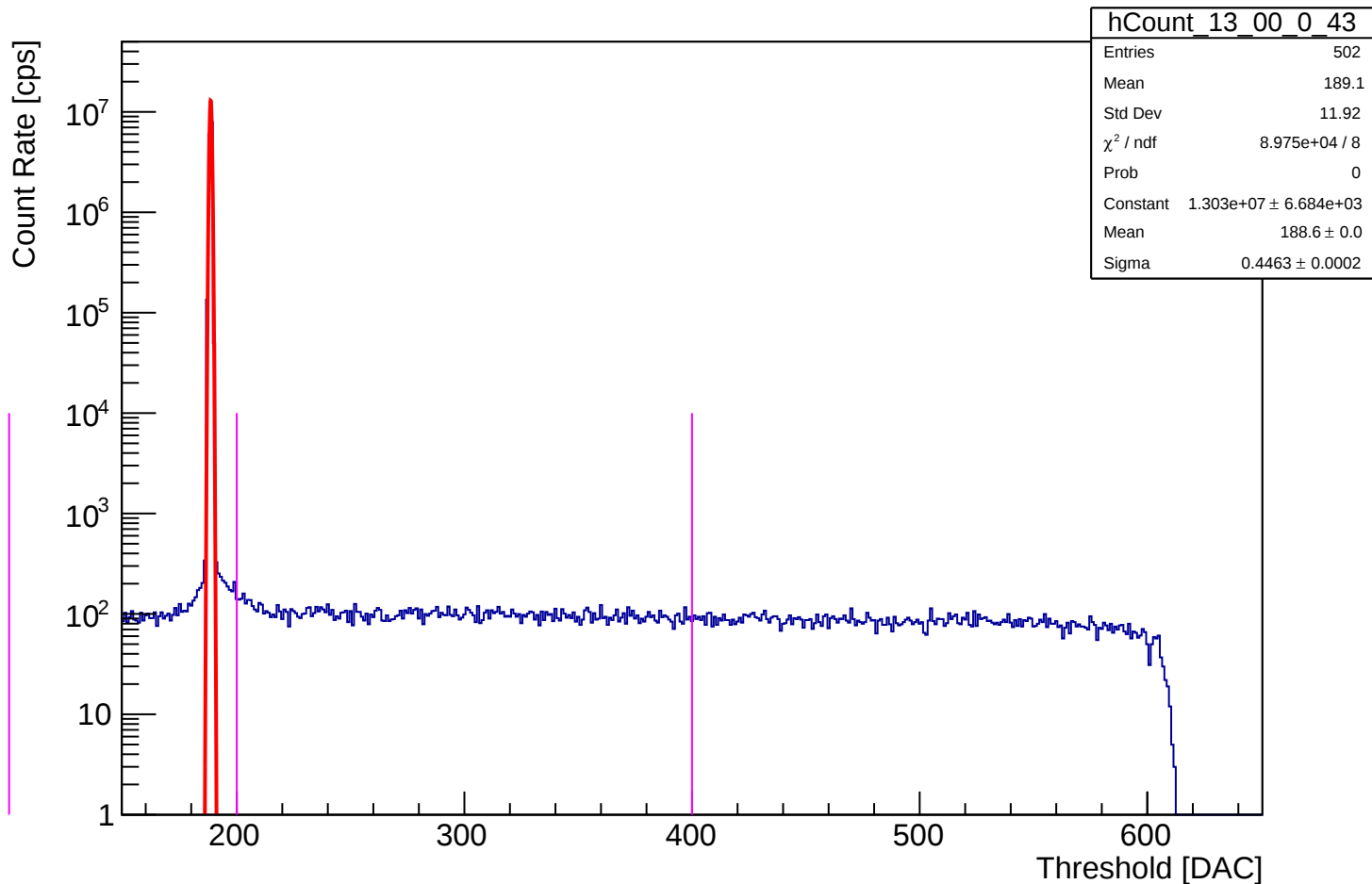


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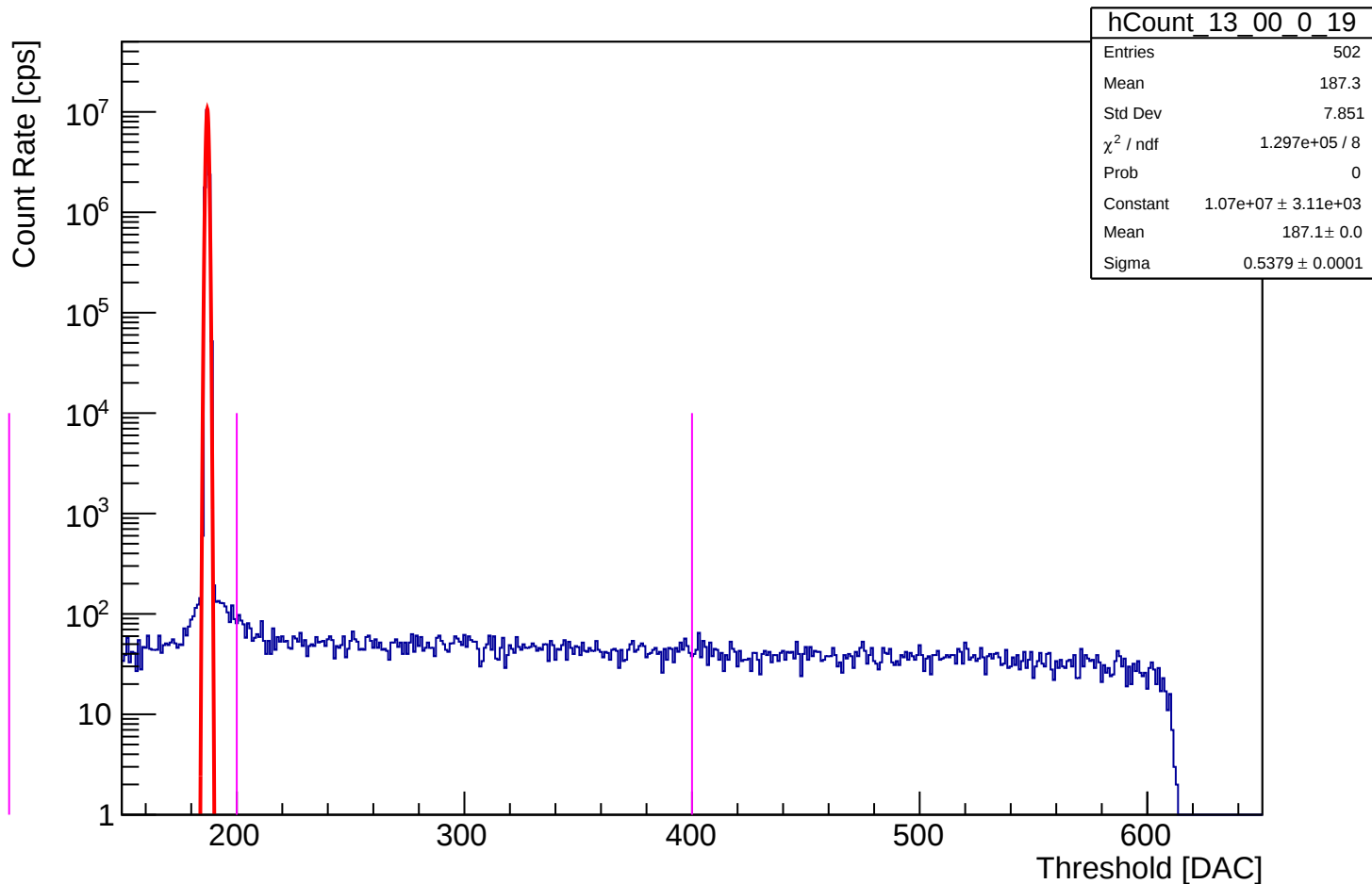




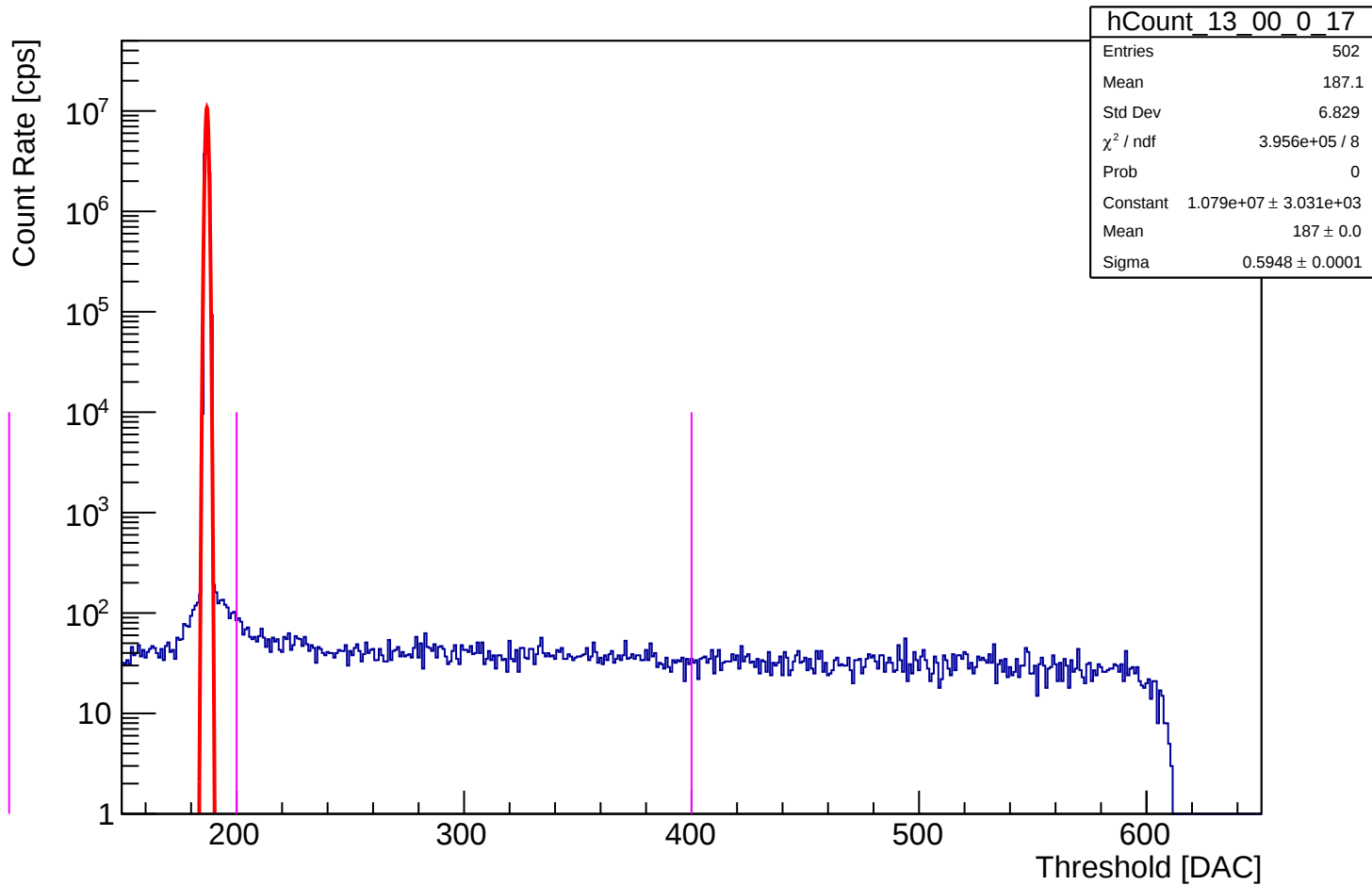
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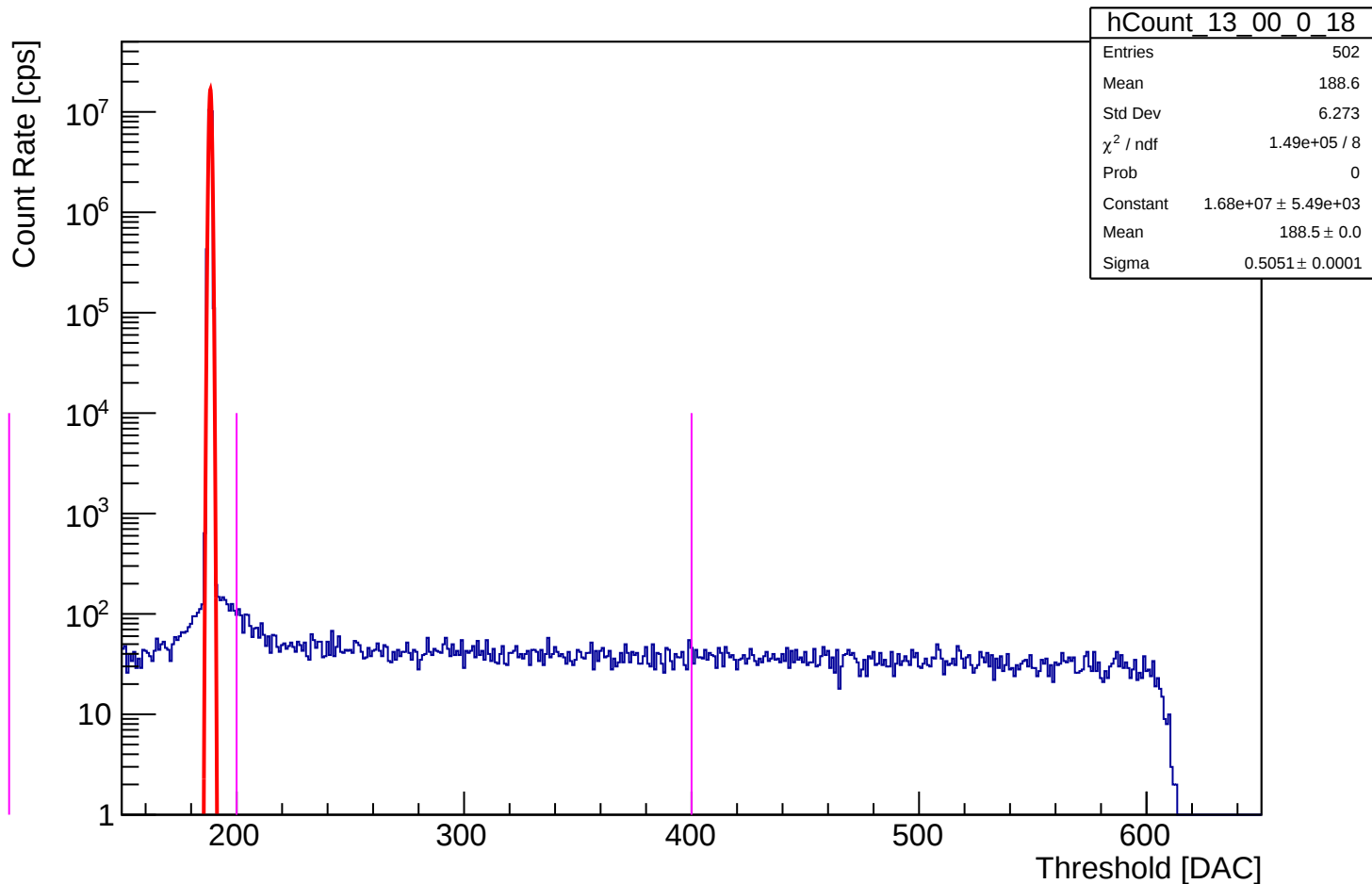
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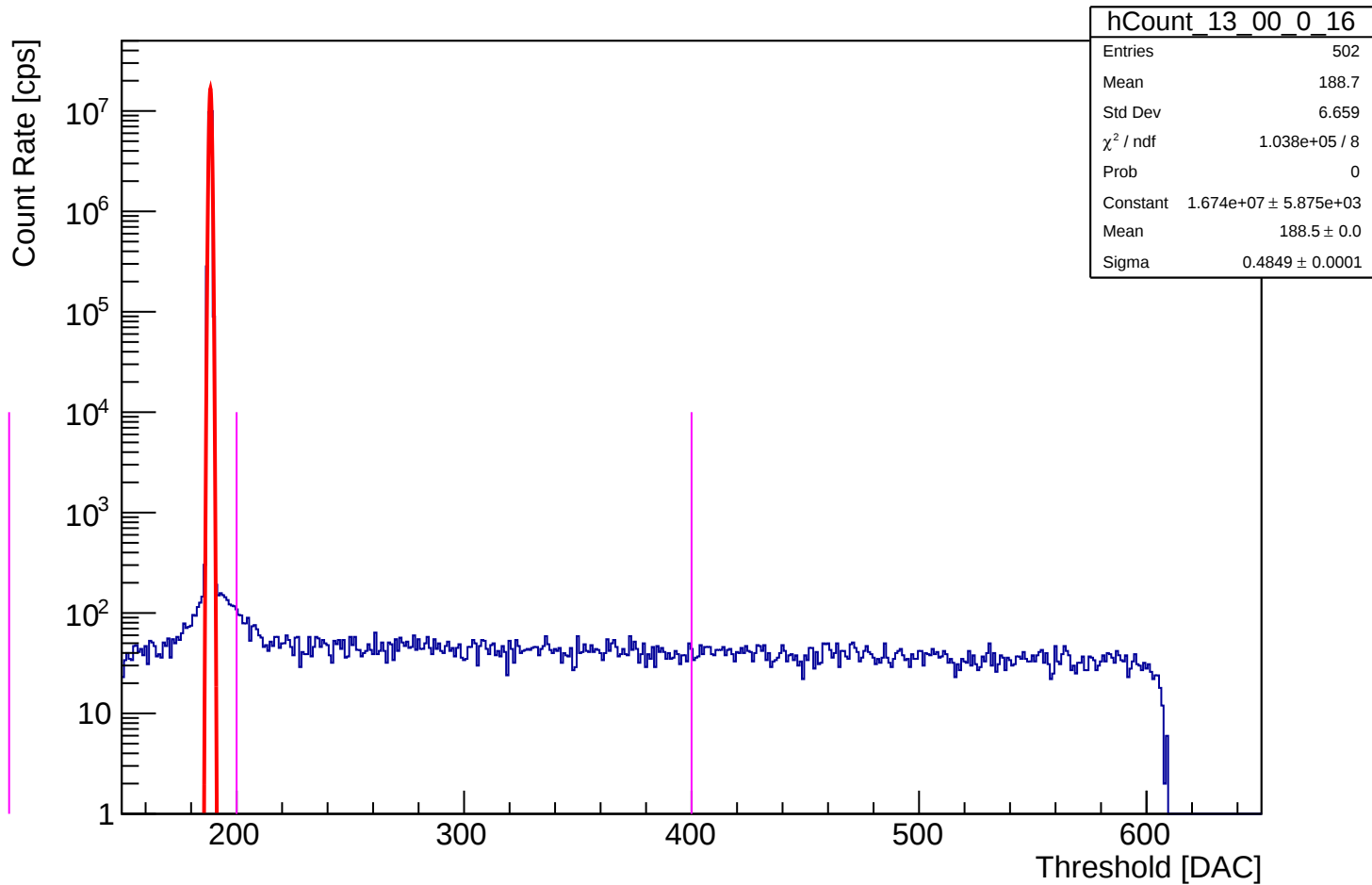
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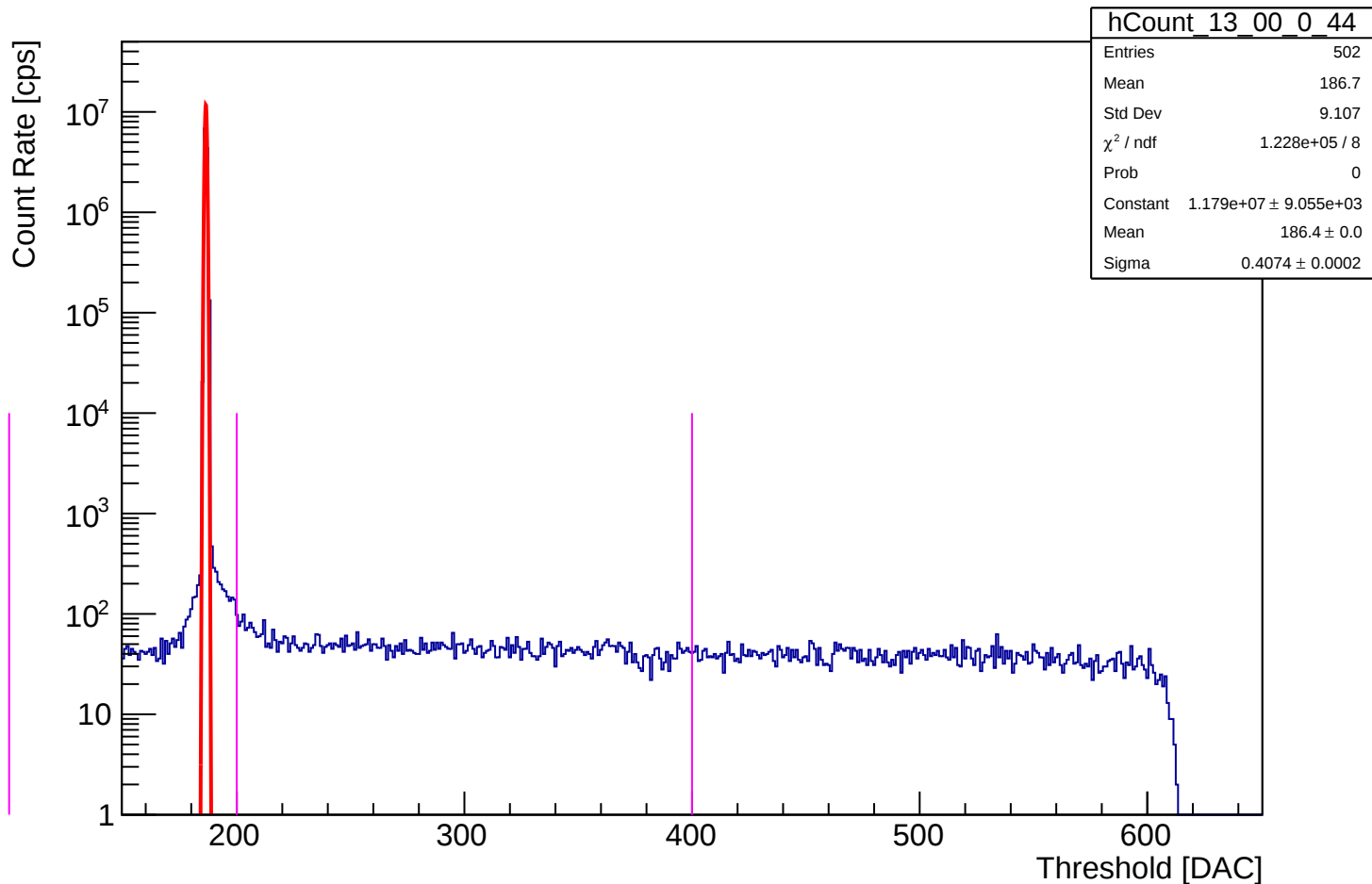
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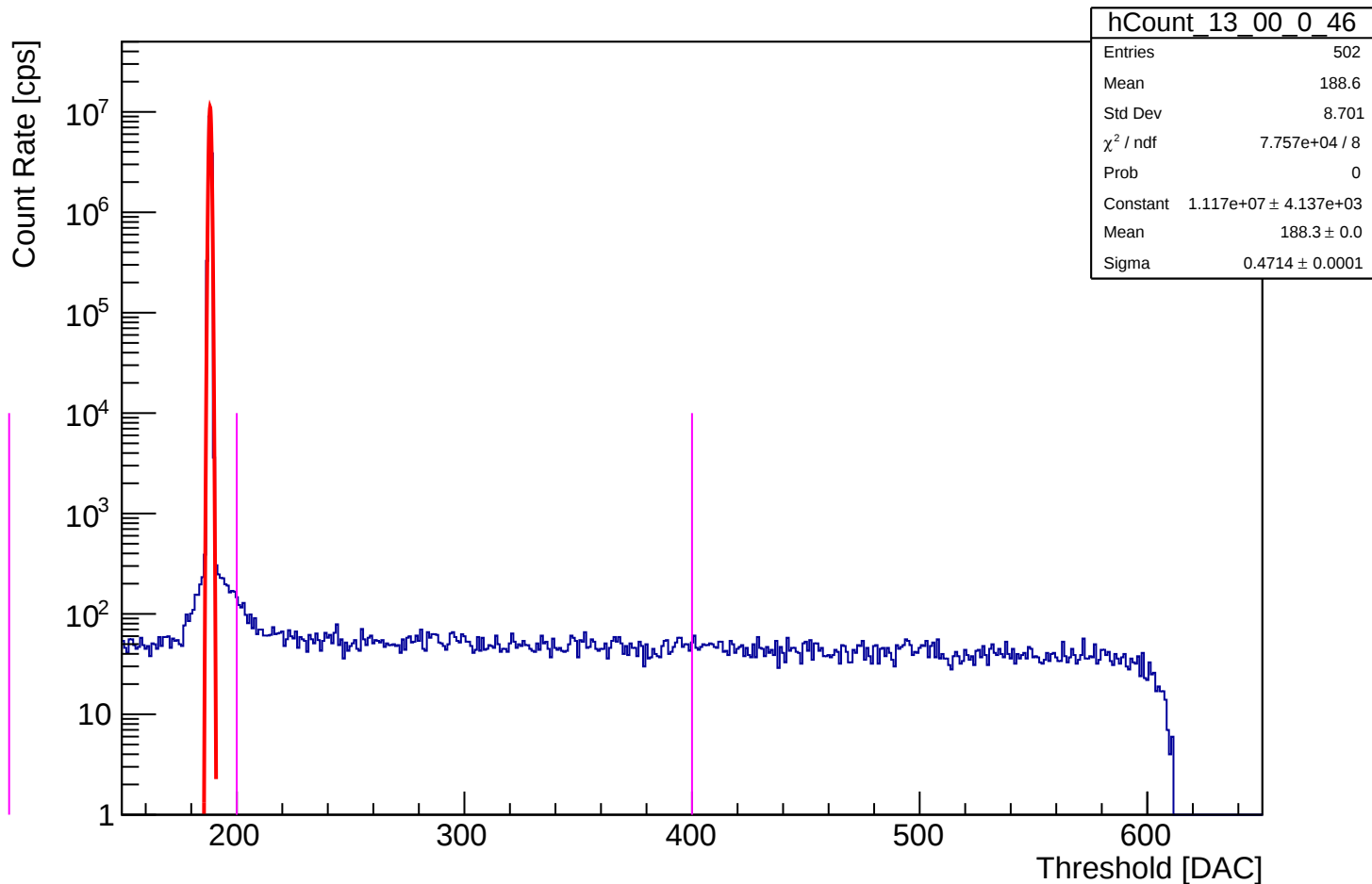
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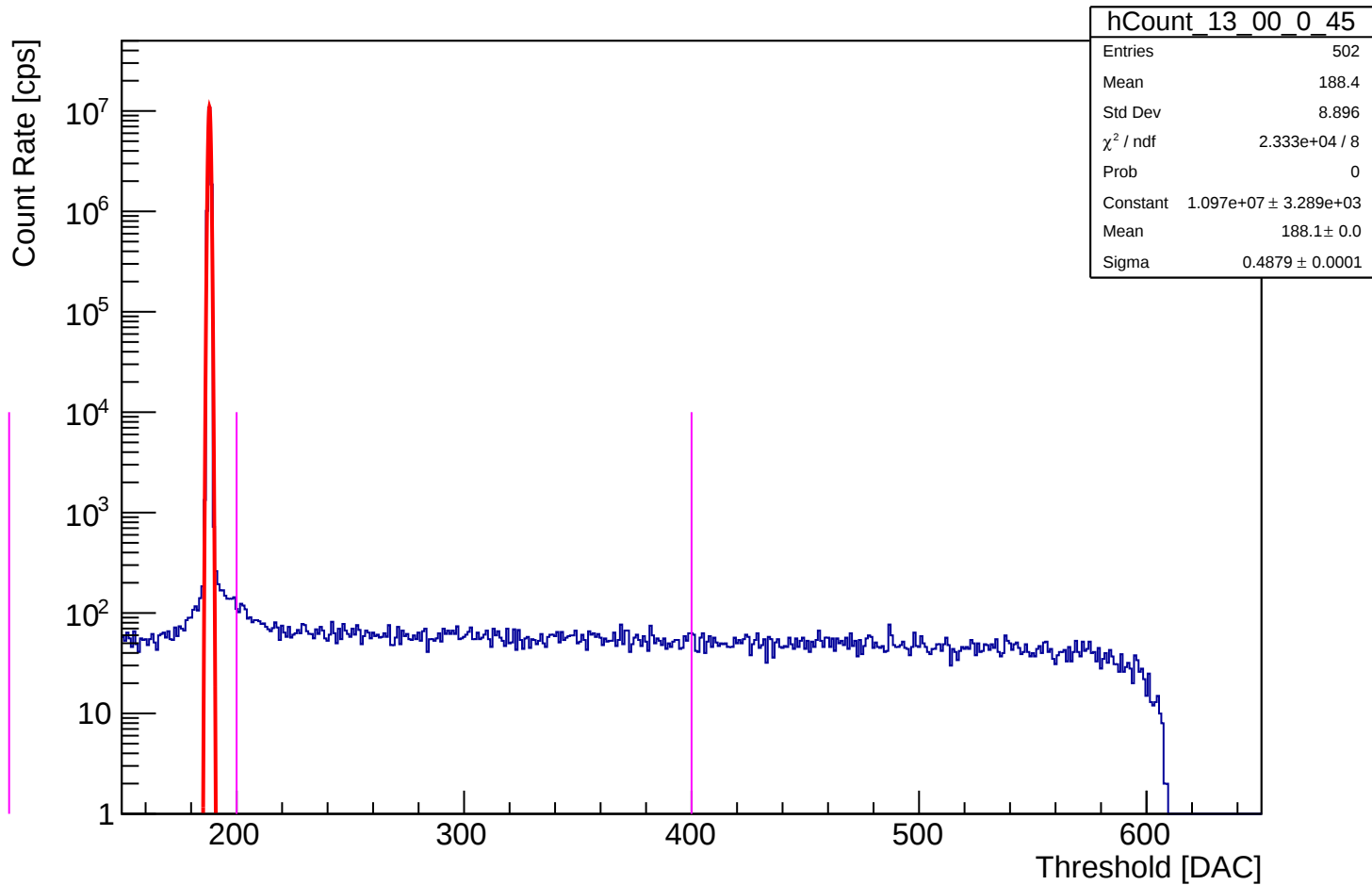
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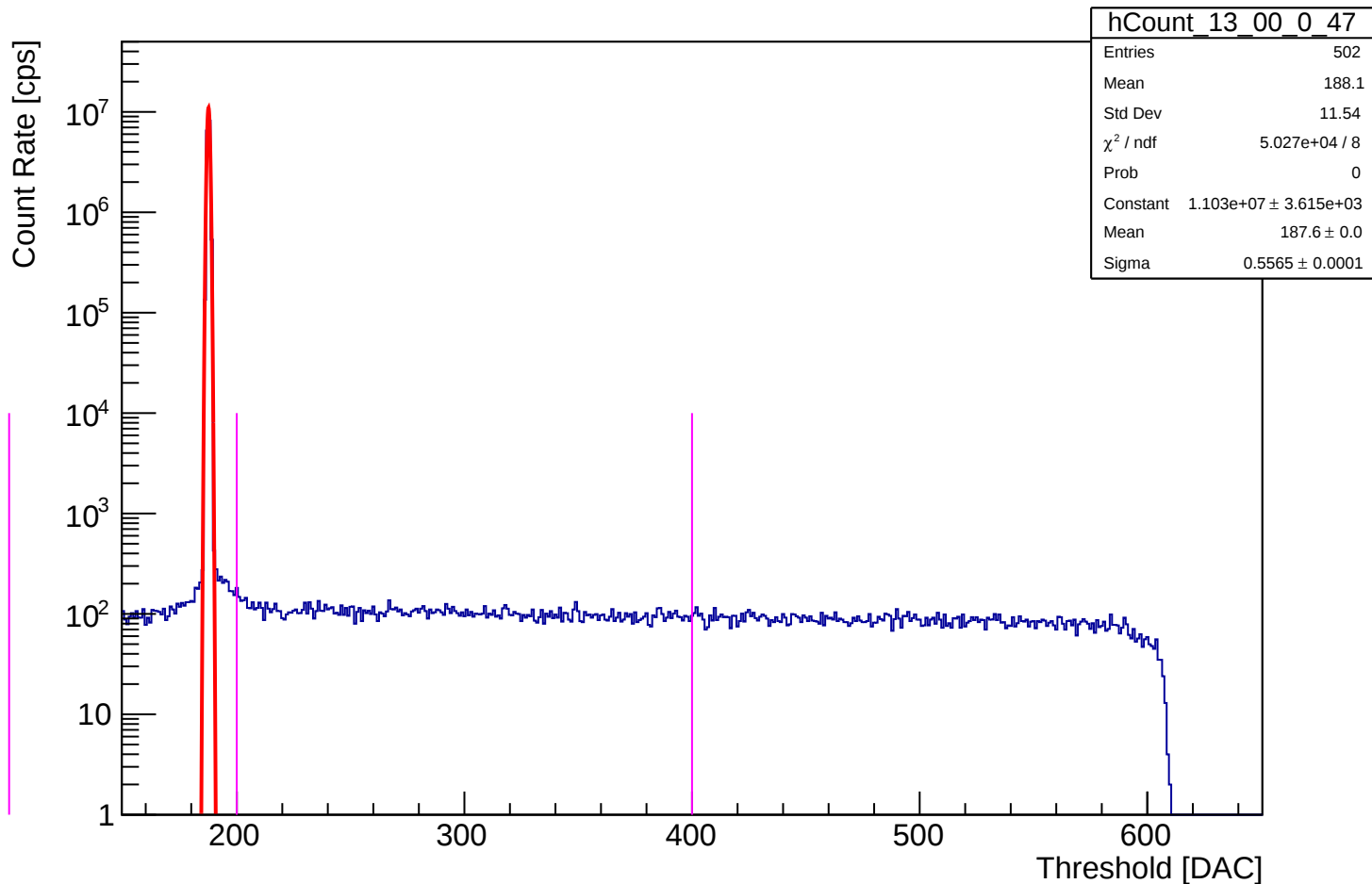
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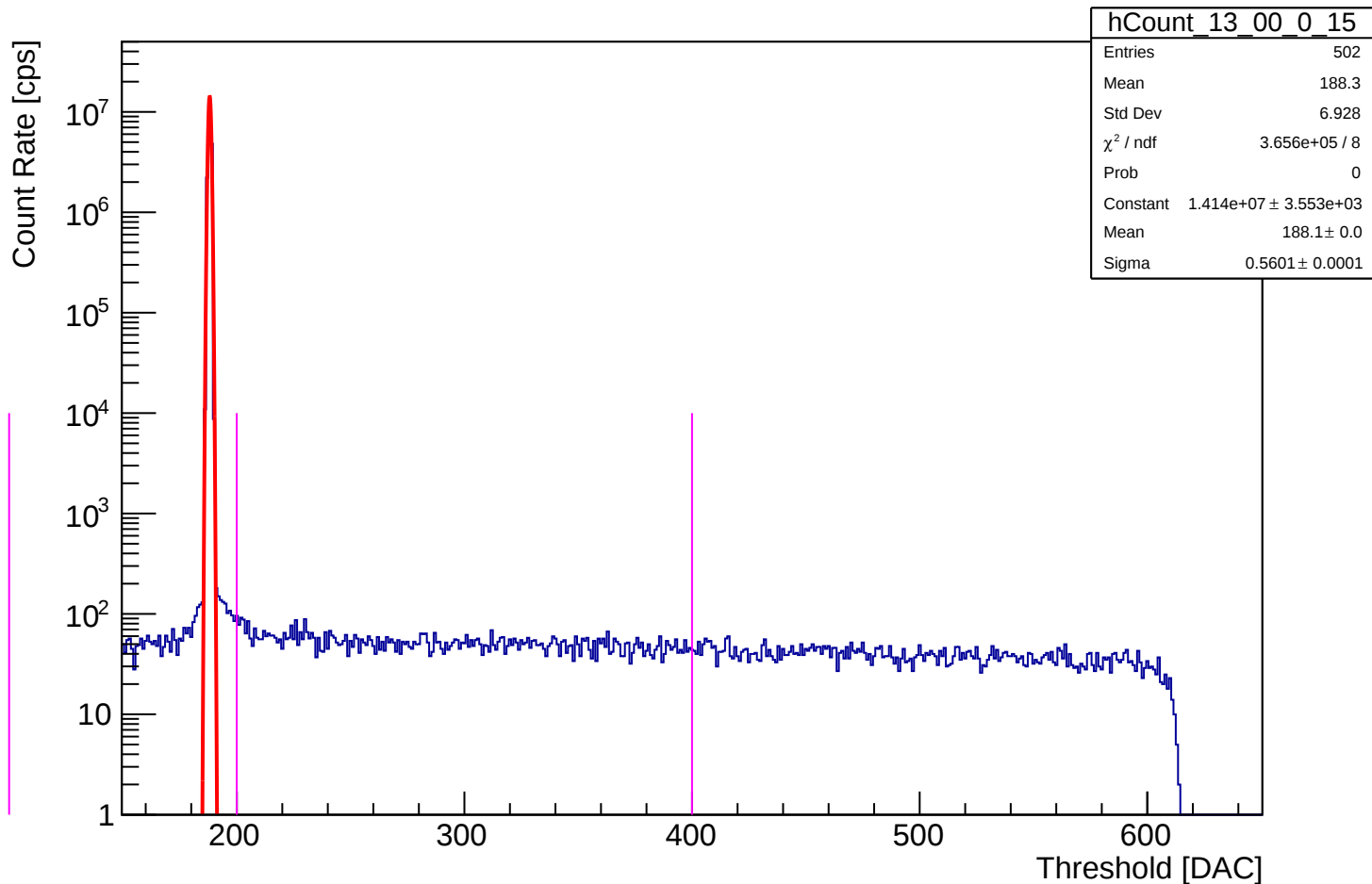
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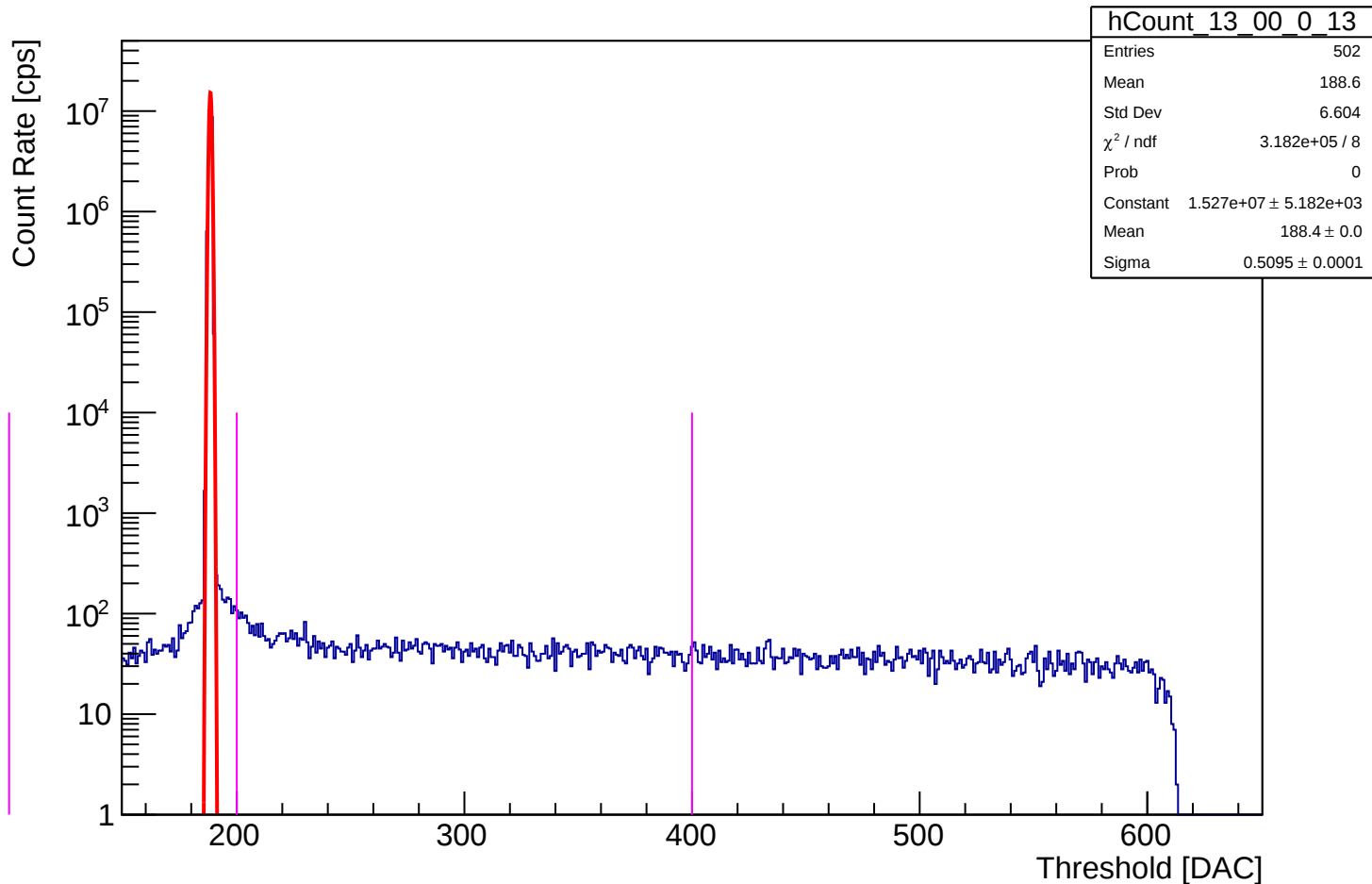
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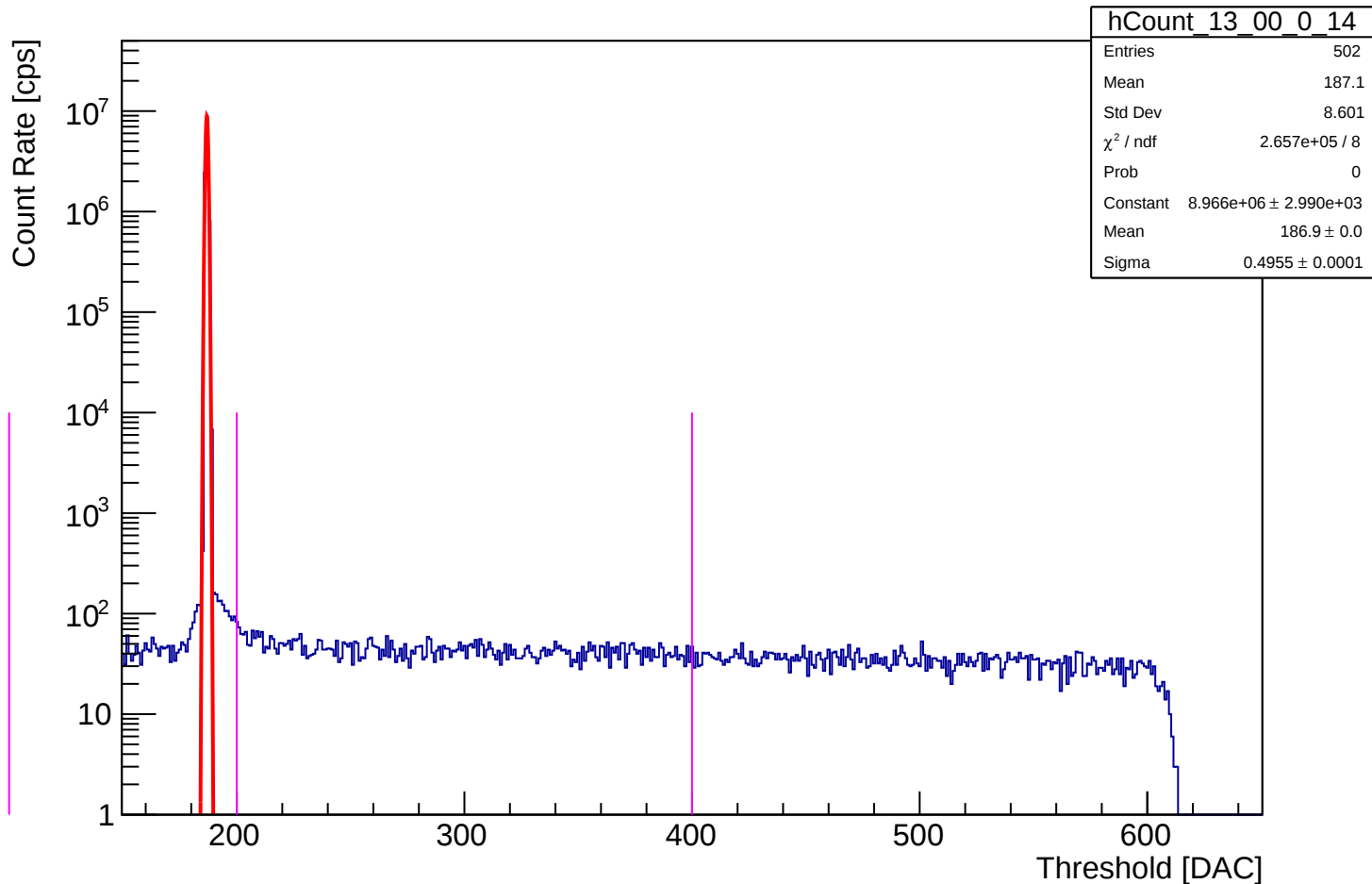
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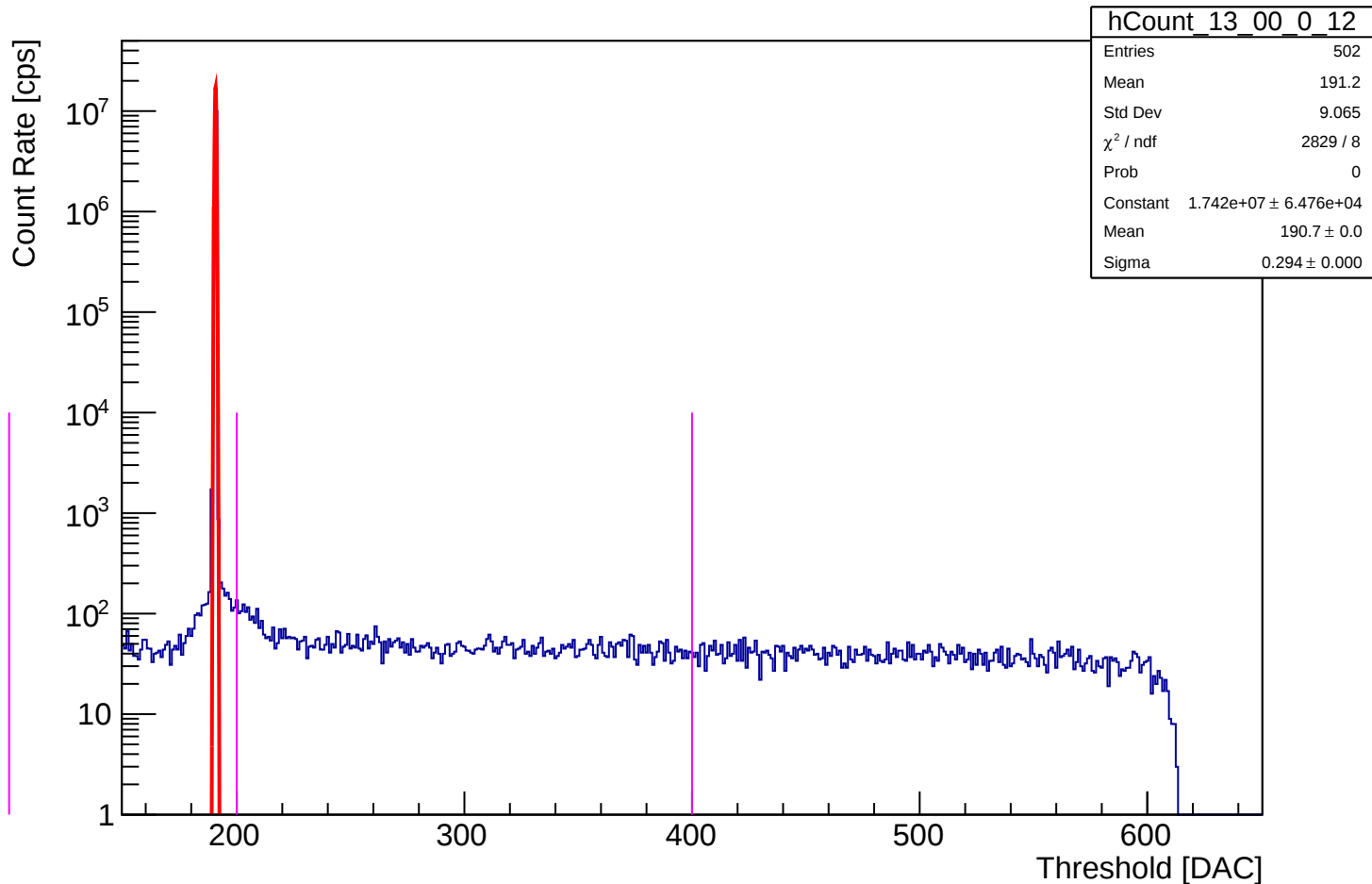
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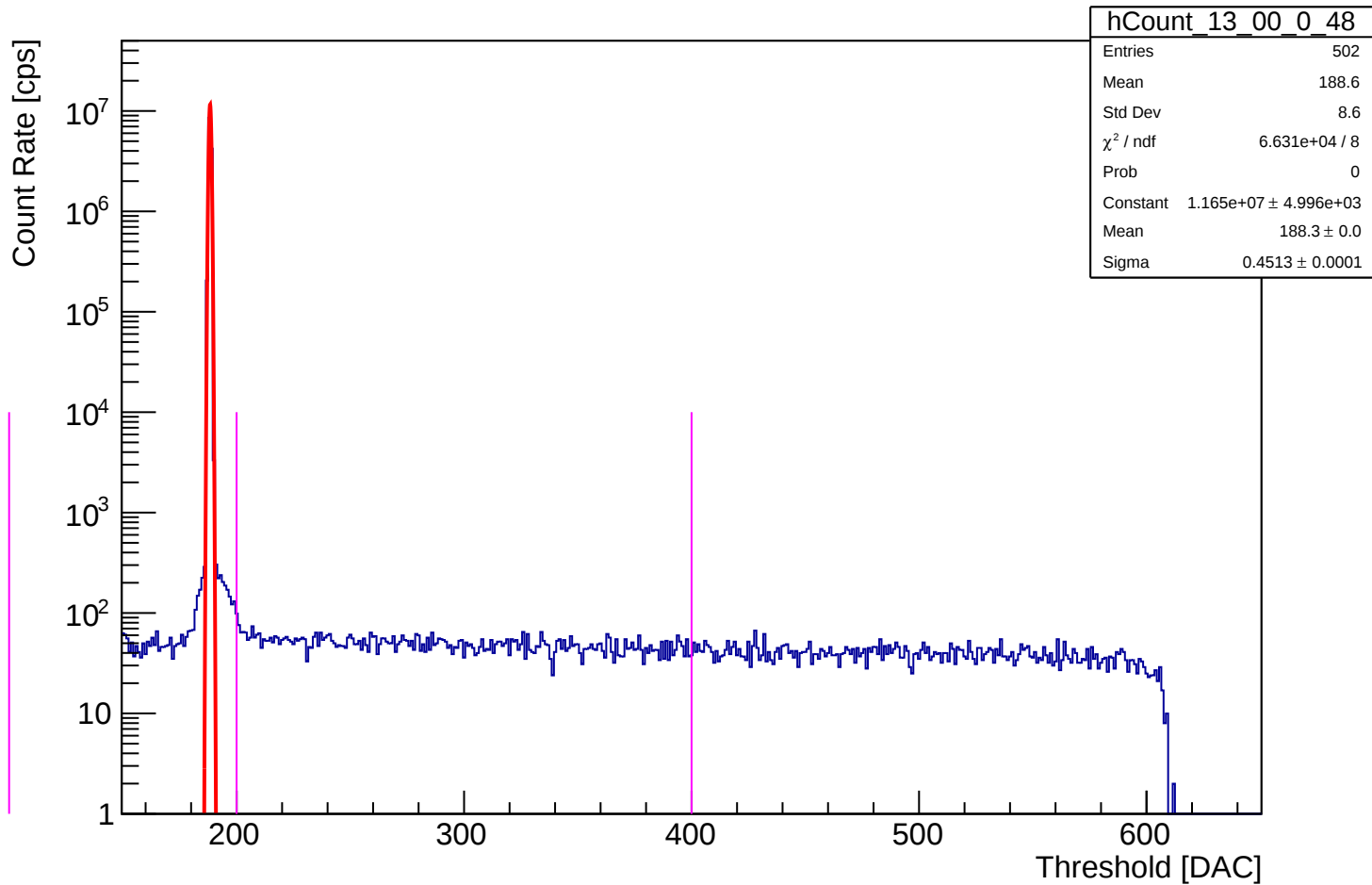
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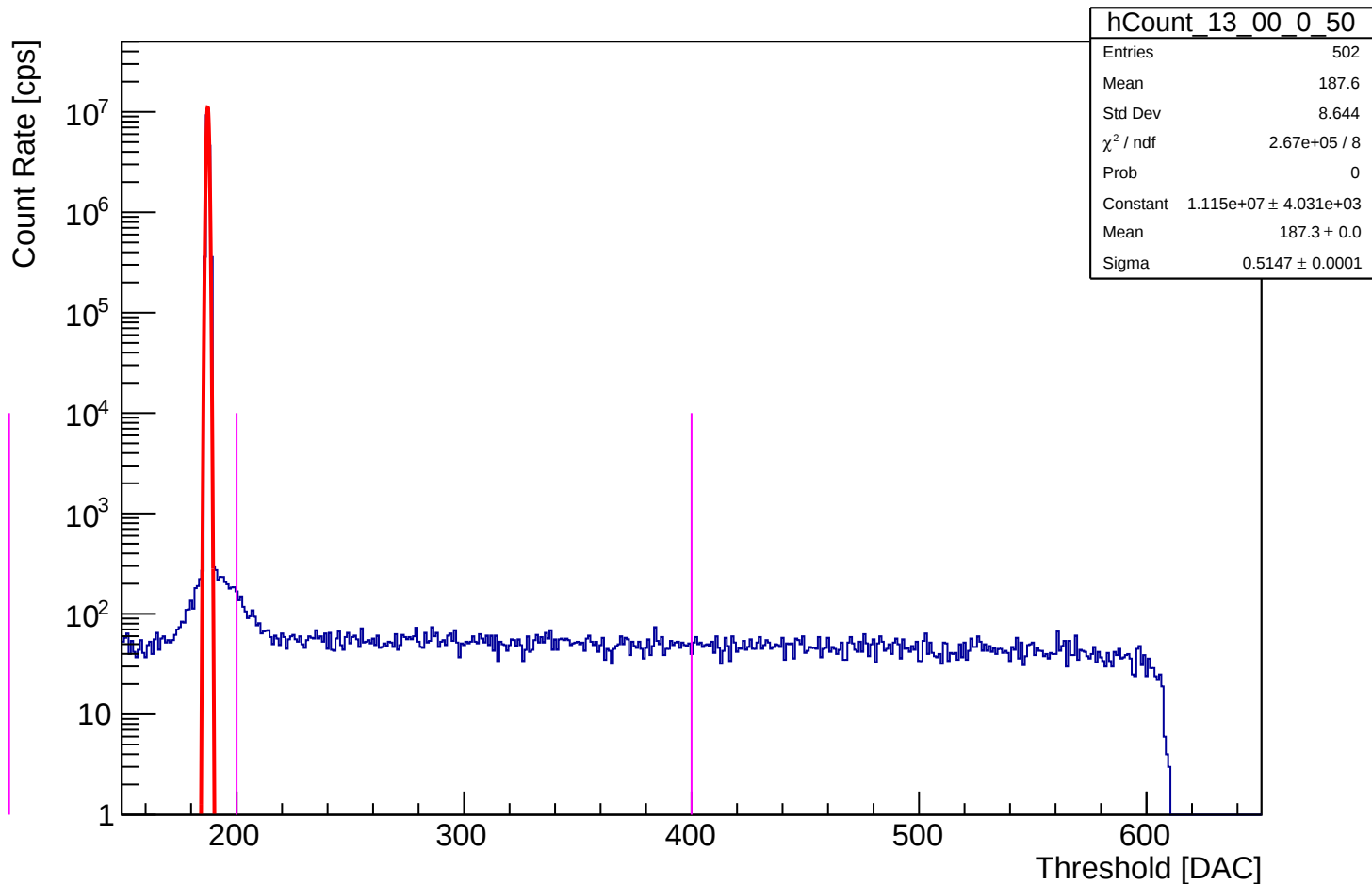
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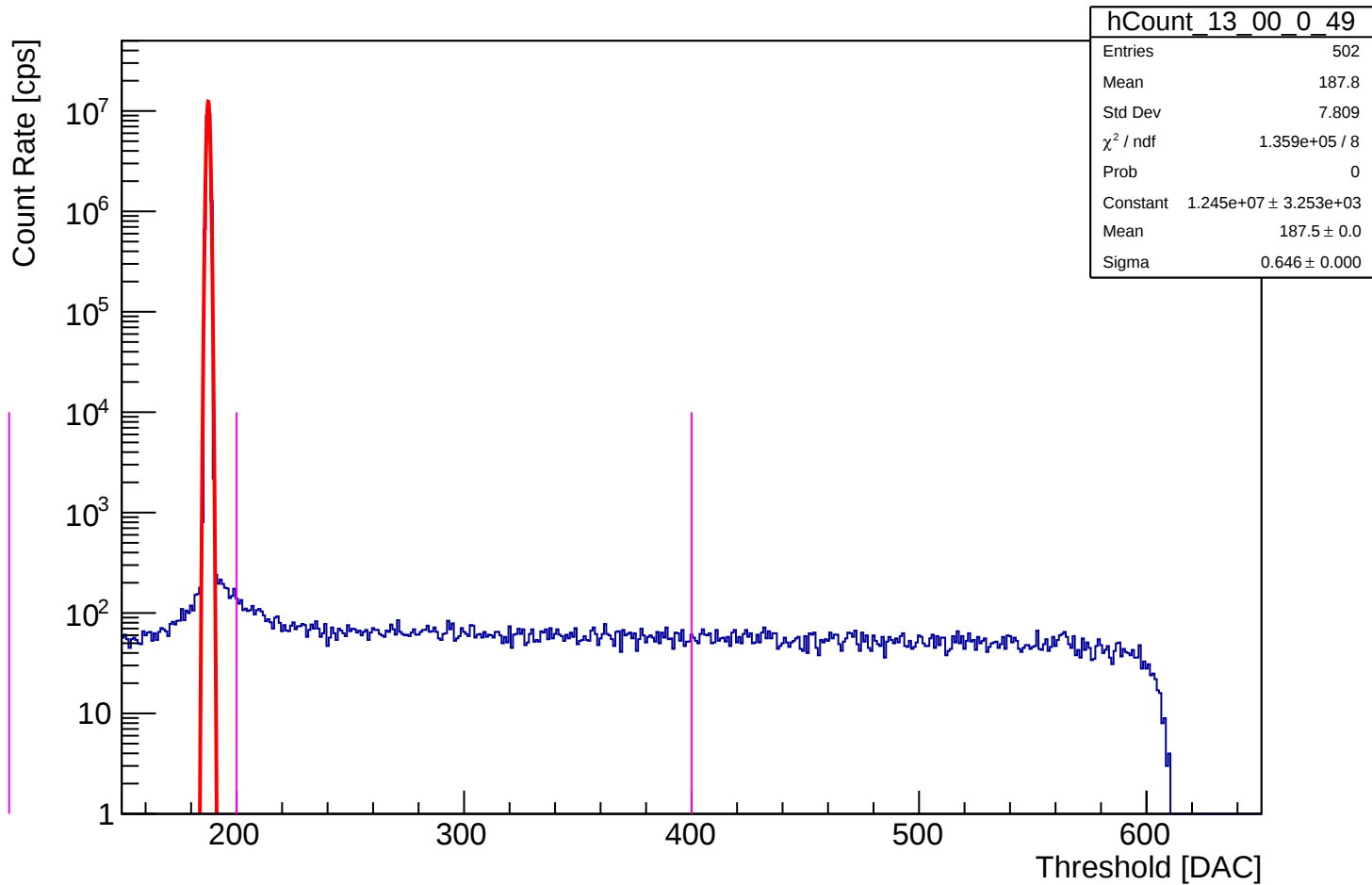
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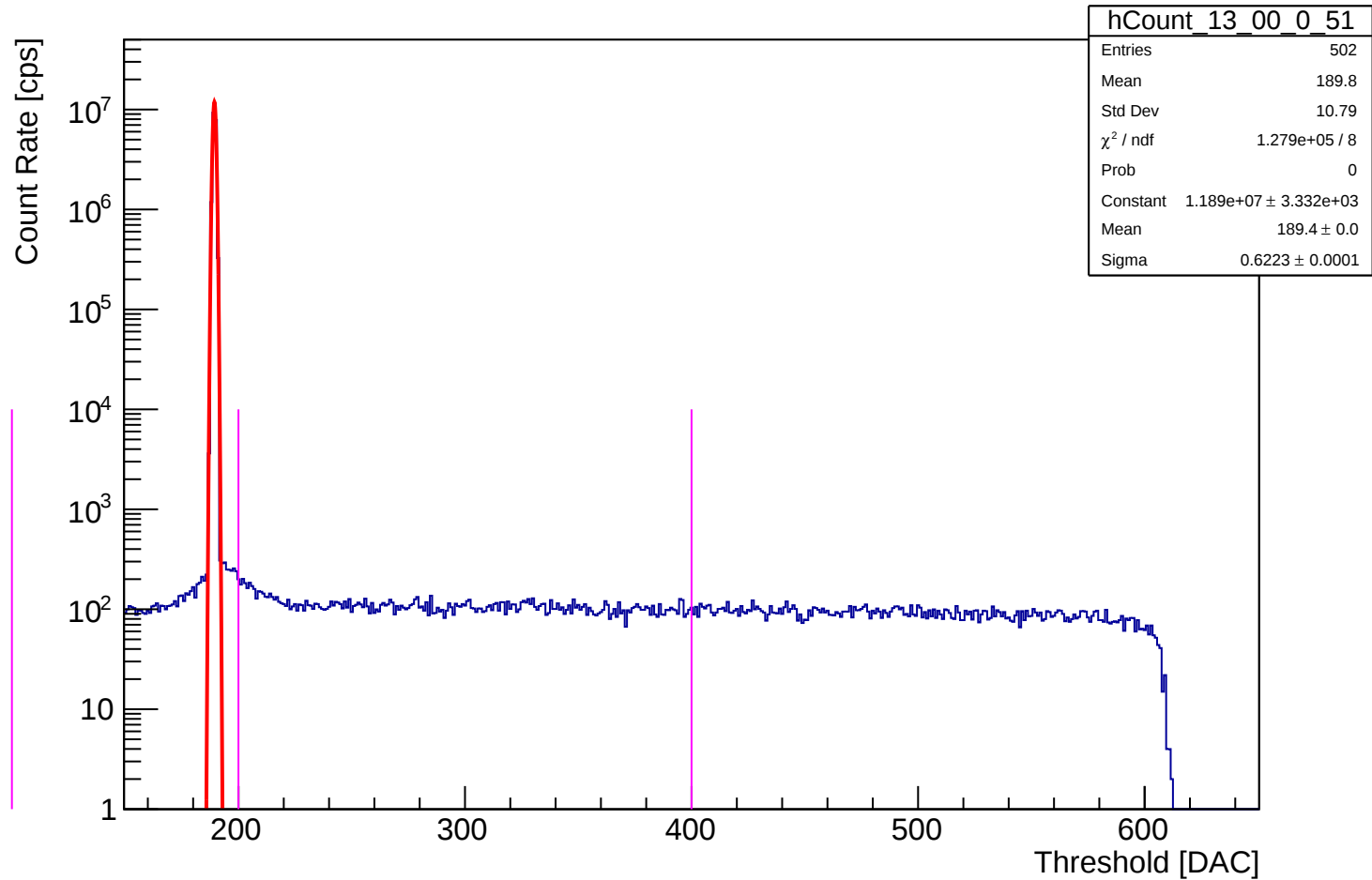


Row 1 Tile 1 Pmt 1 Pixel 38 Slot 13 Fiber 0 Asic 0 Channel 50

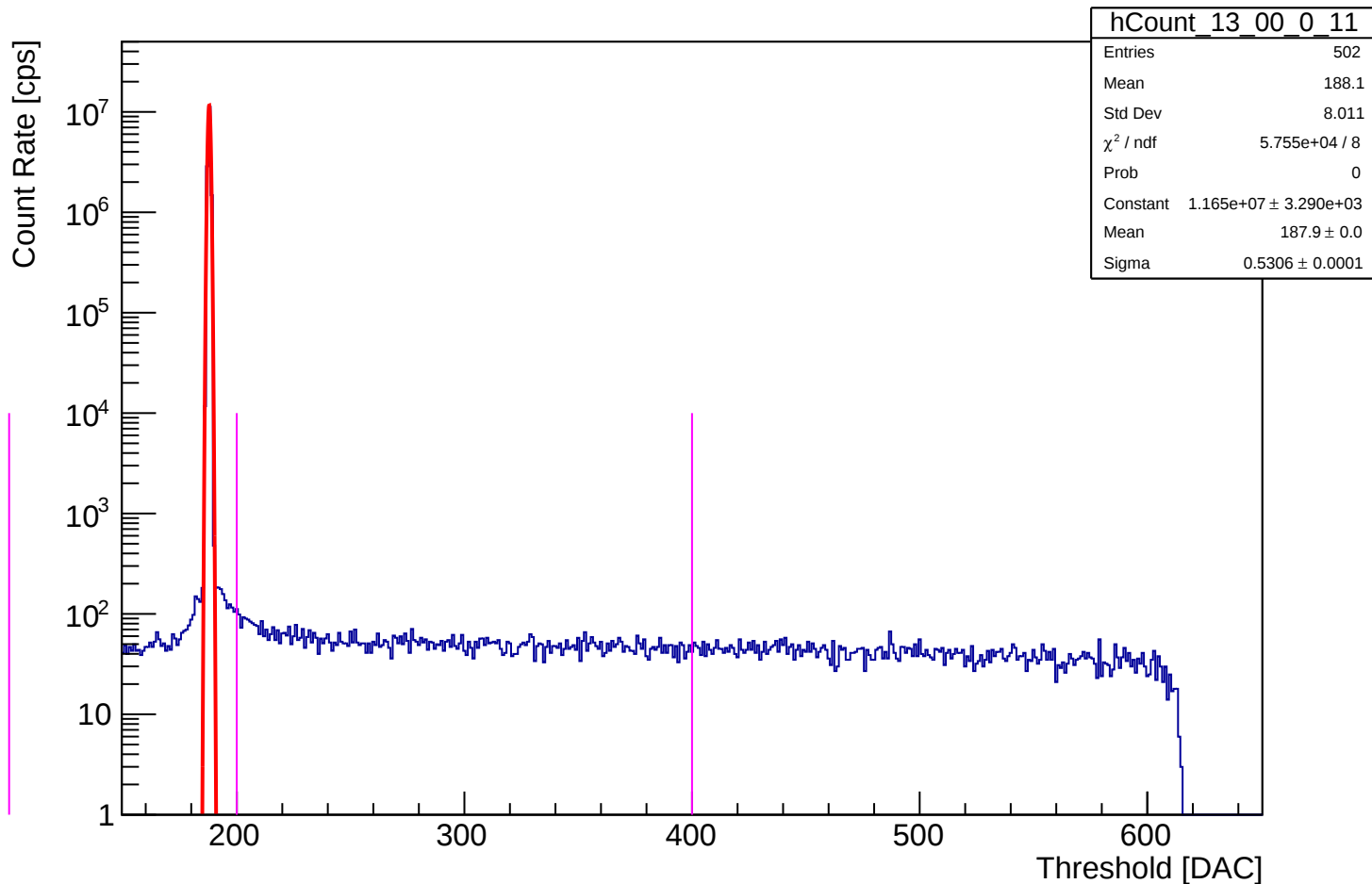


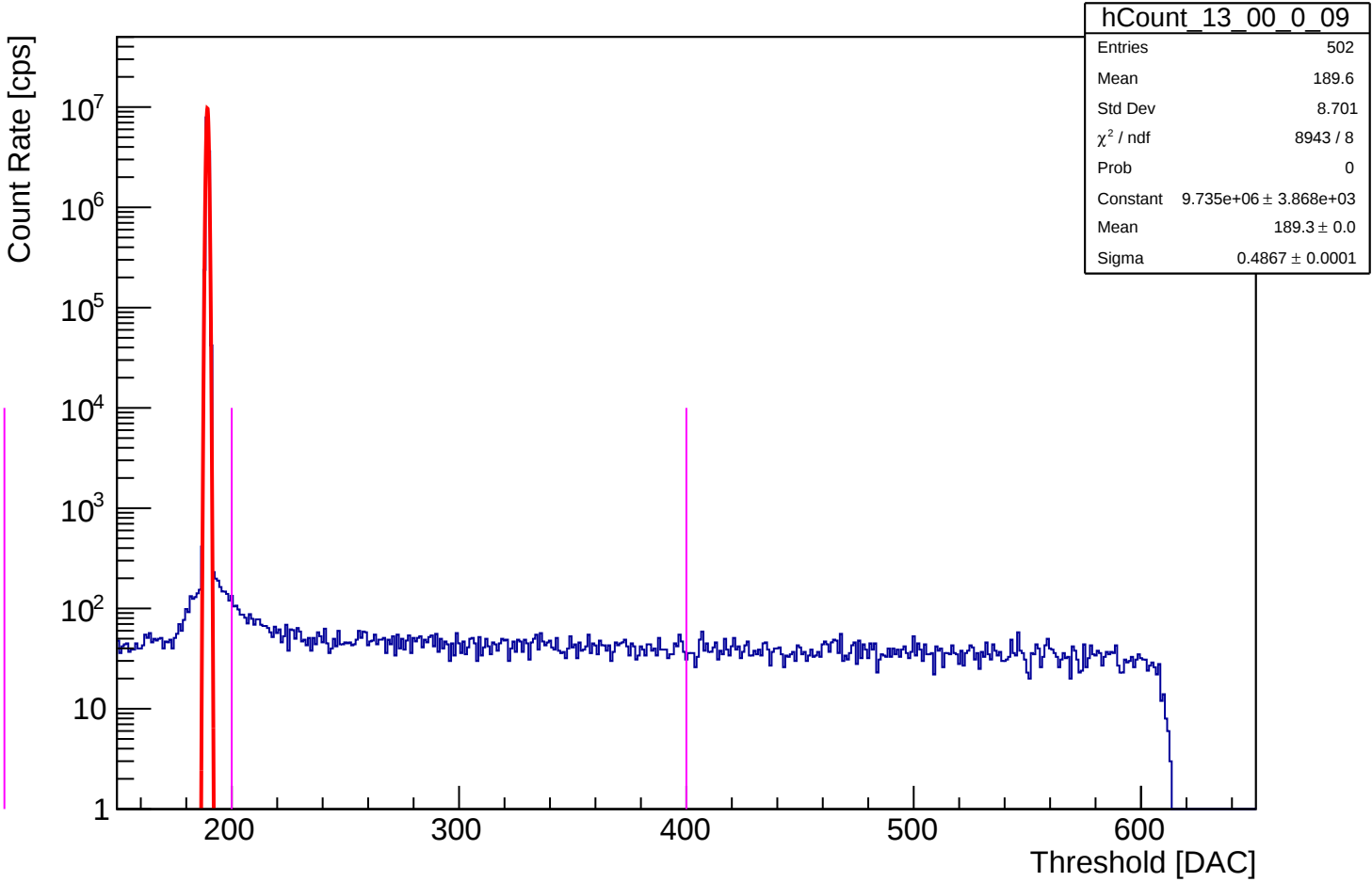
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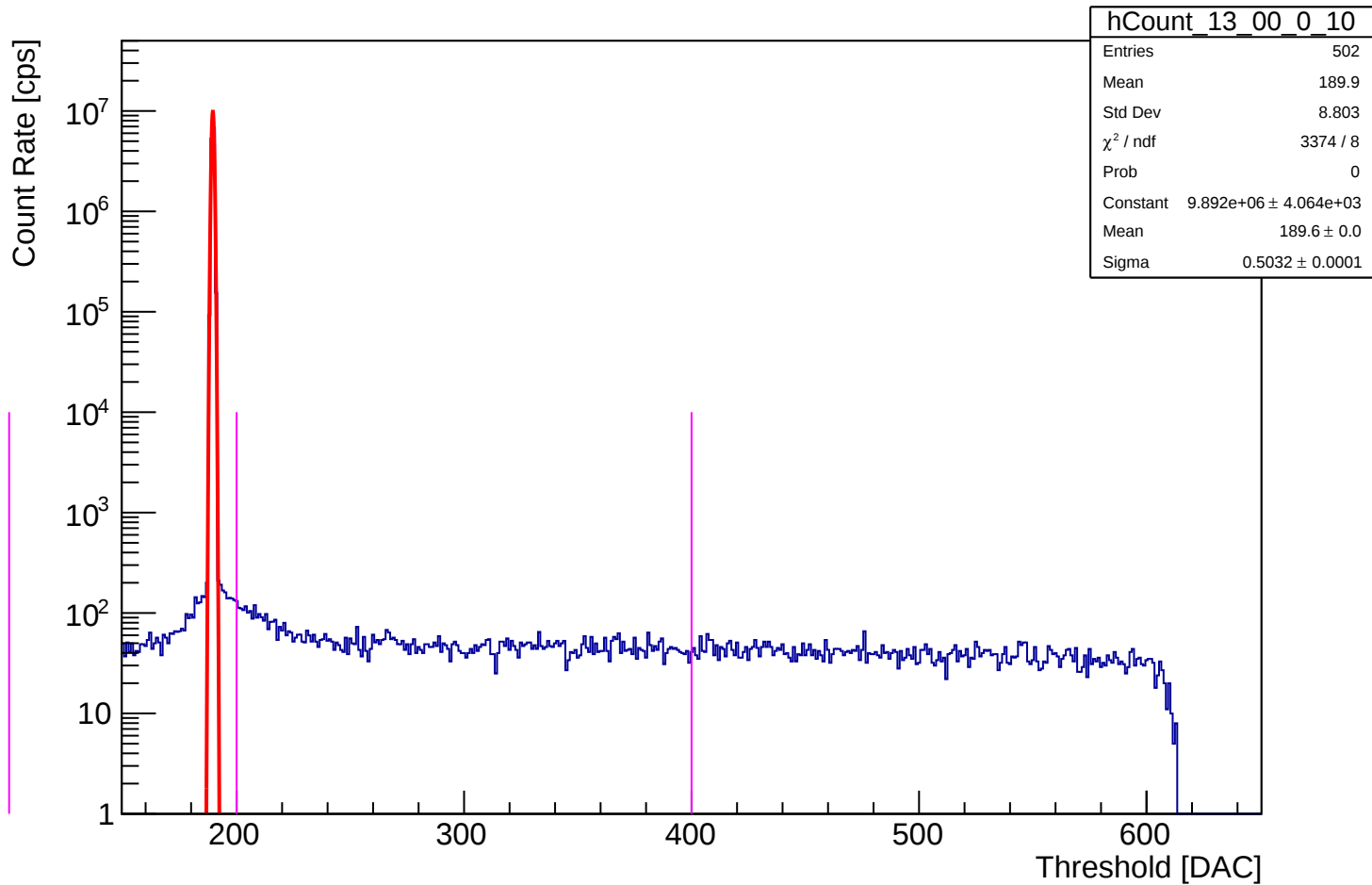


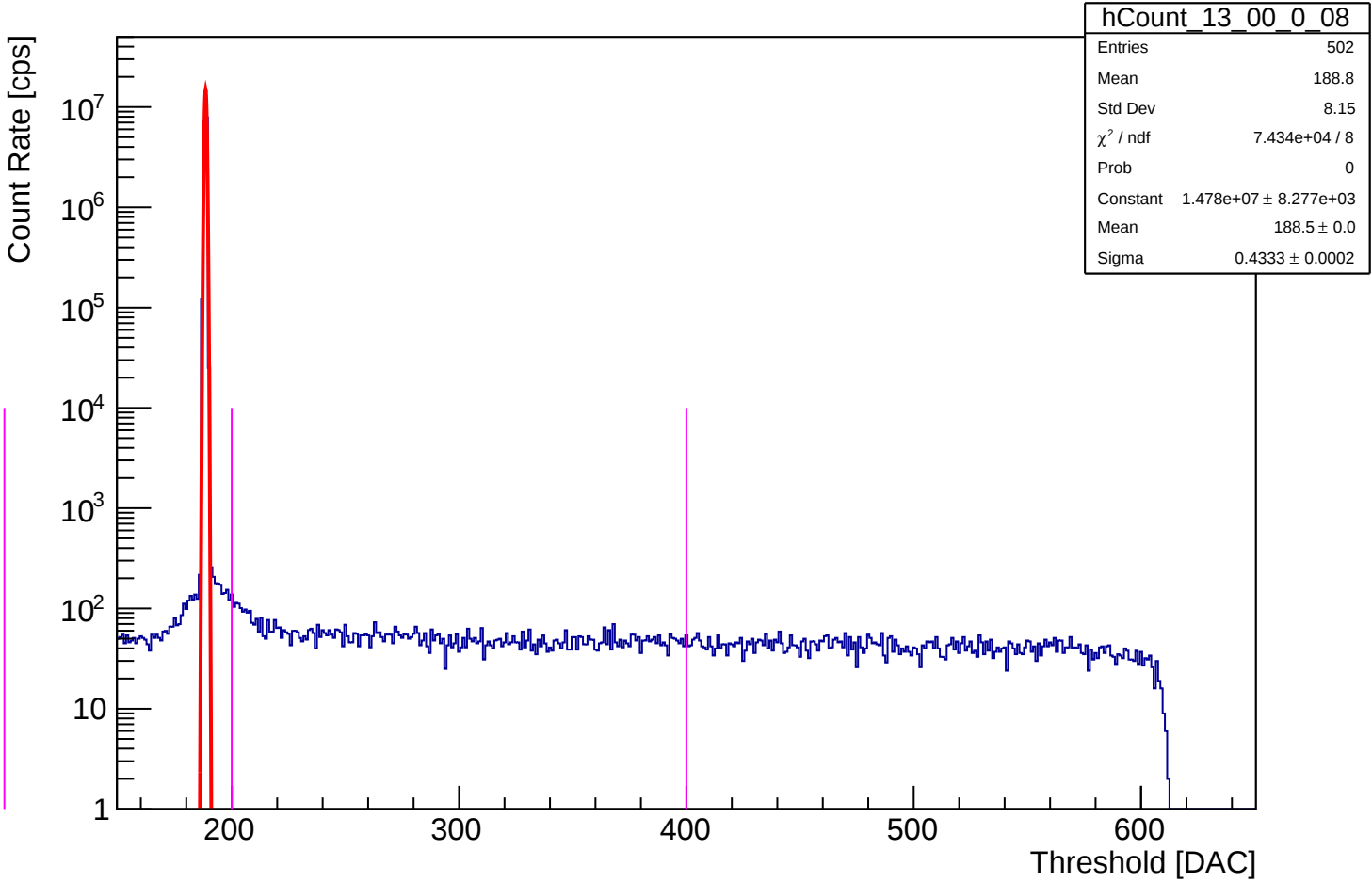
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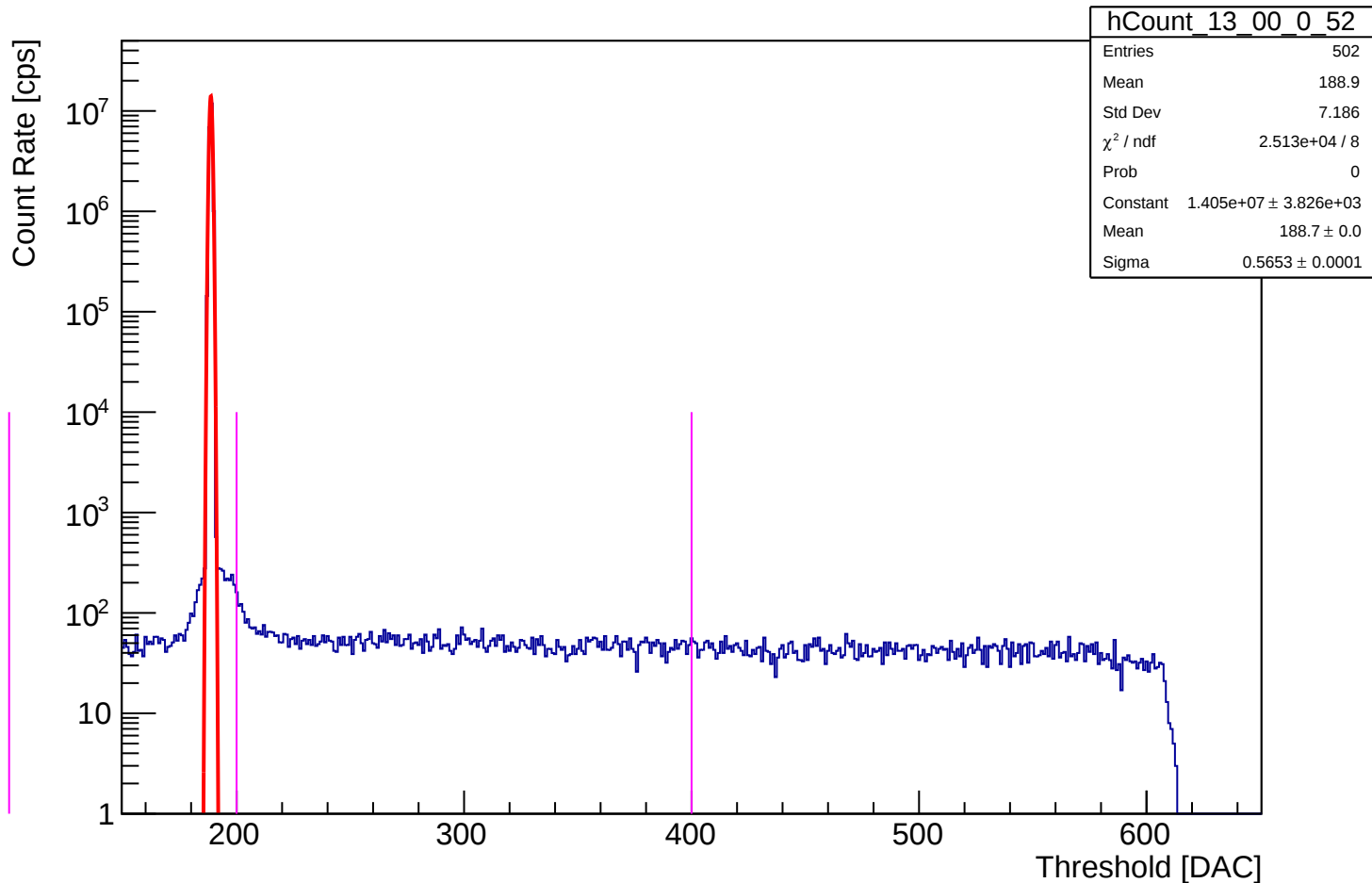


Row 1 Tile 1 Pmt 1 Pixel 43 Slot 13 Fiber 0 Asic 0 Channel 10

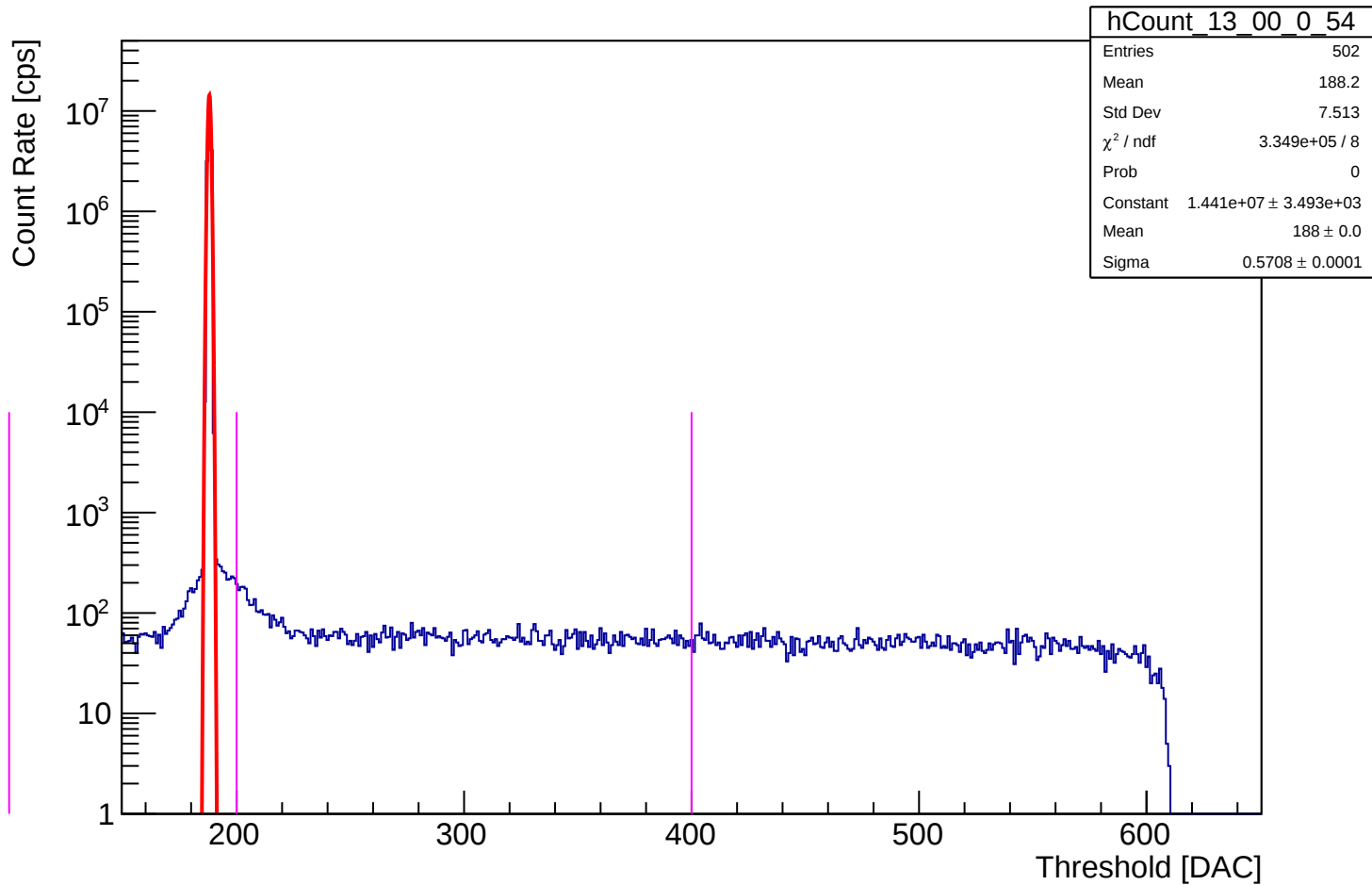




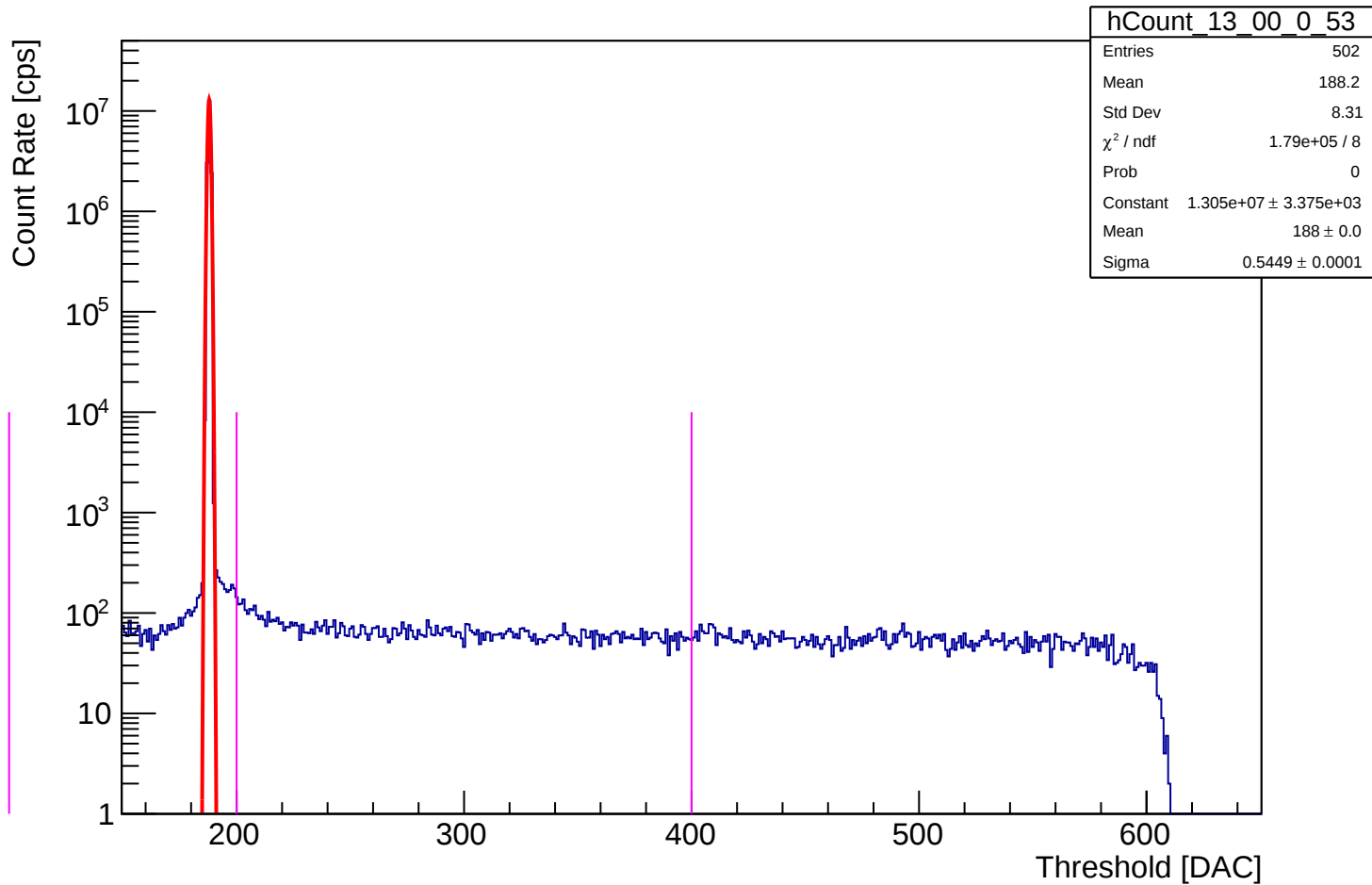
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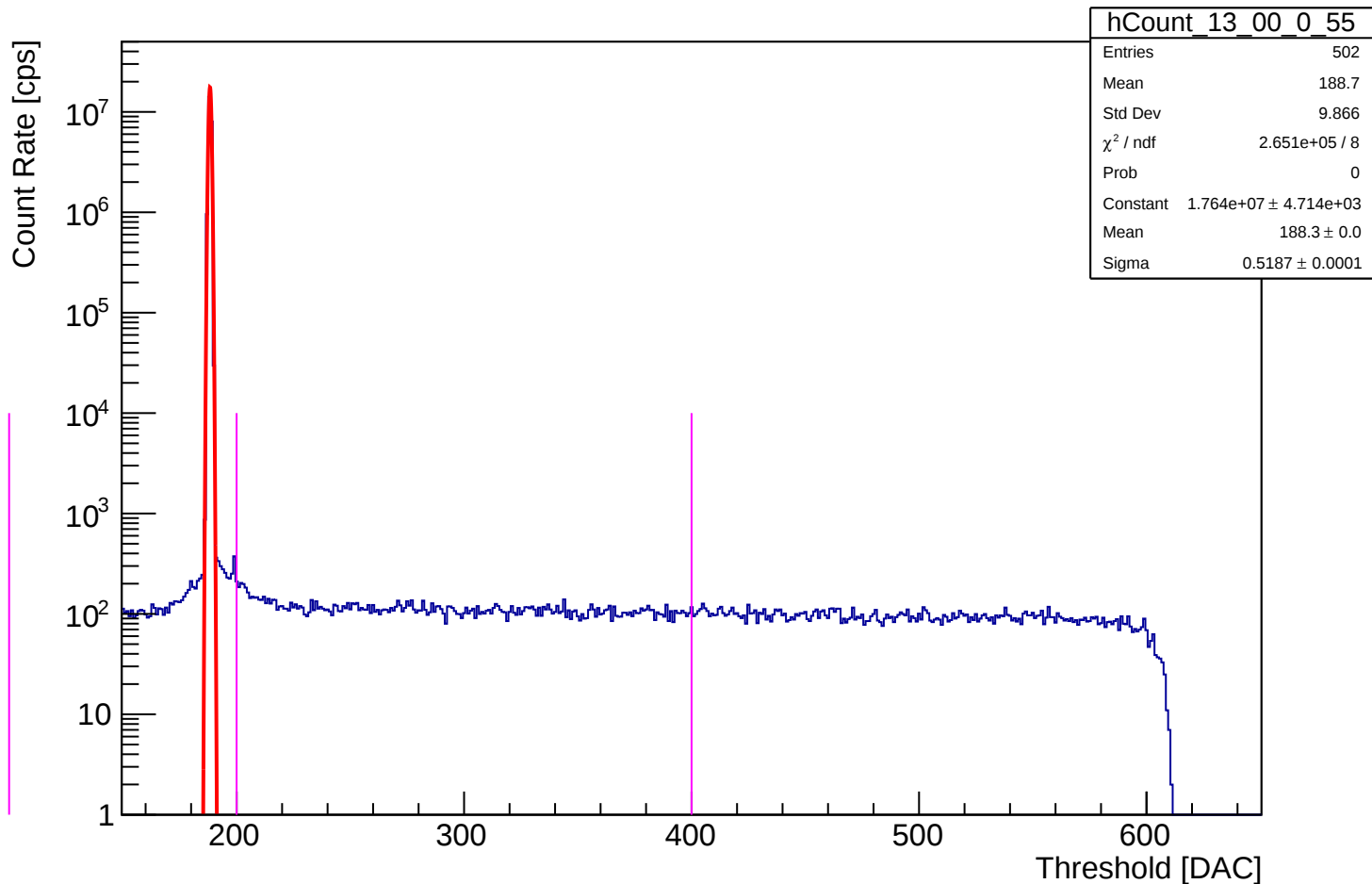
Row 1 Tile 1 Pmt 1 Pixel 46 Slot 13 Fiber 0 Asic 0 Channel 54

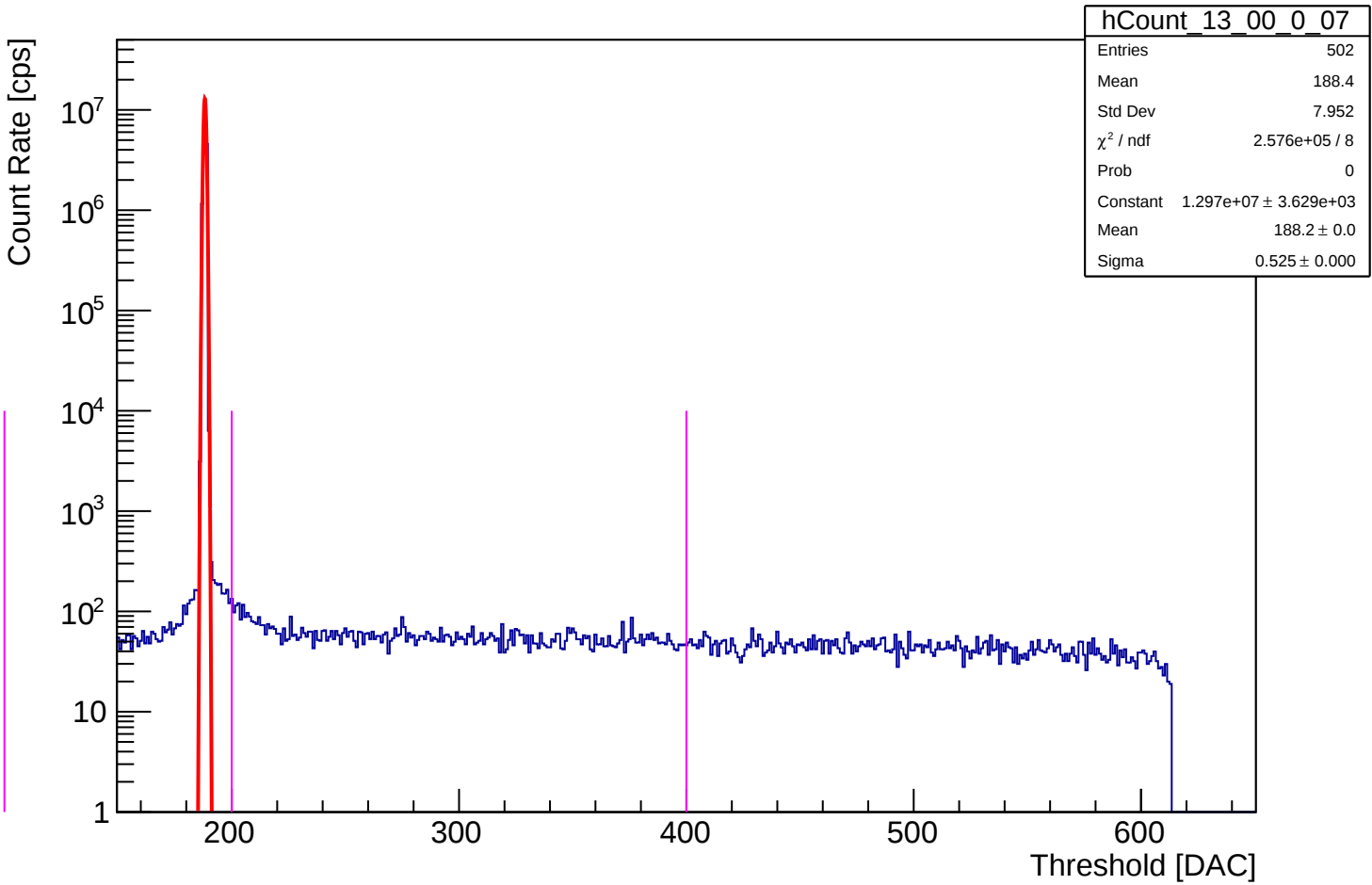


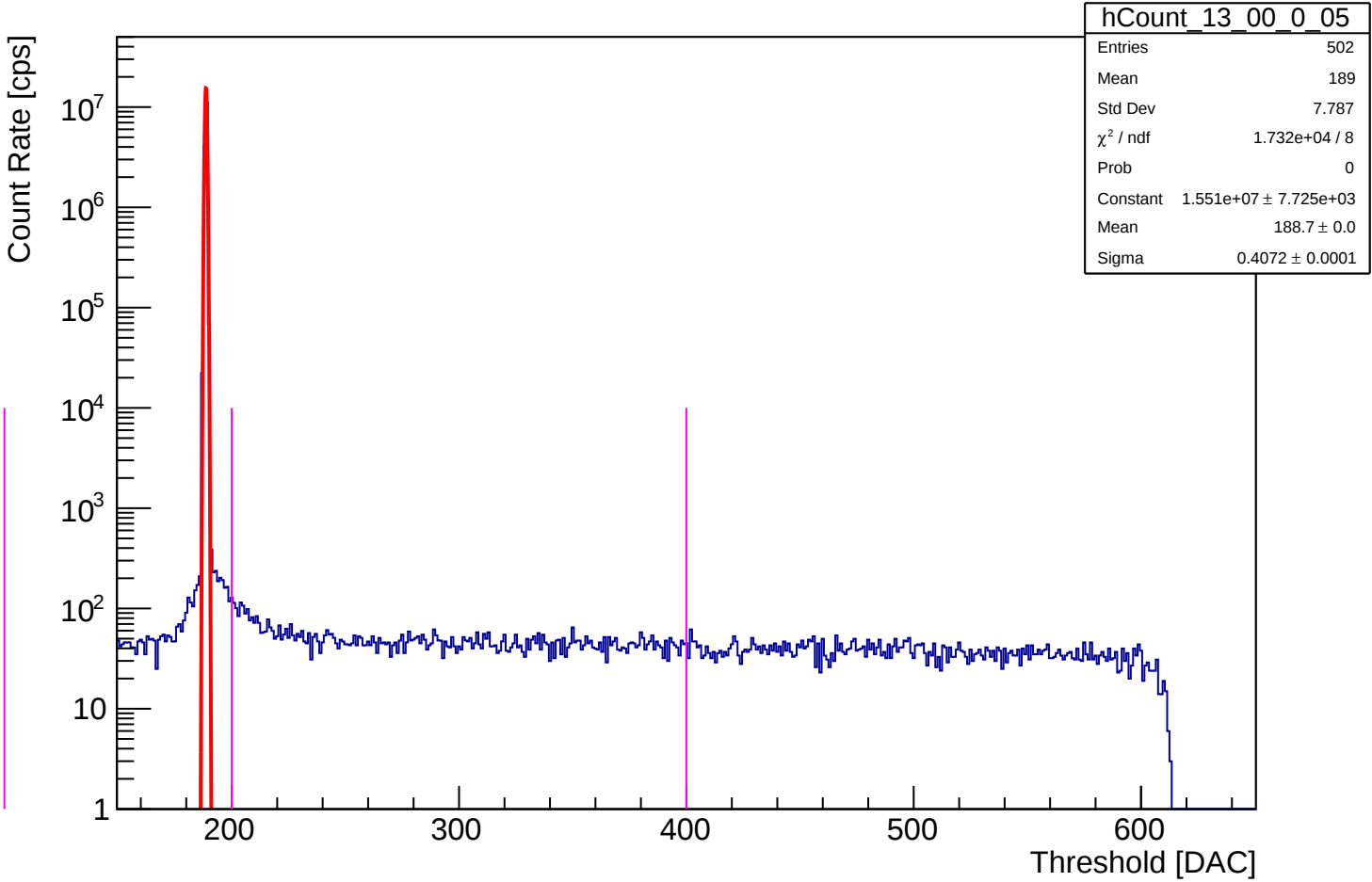
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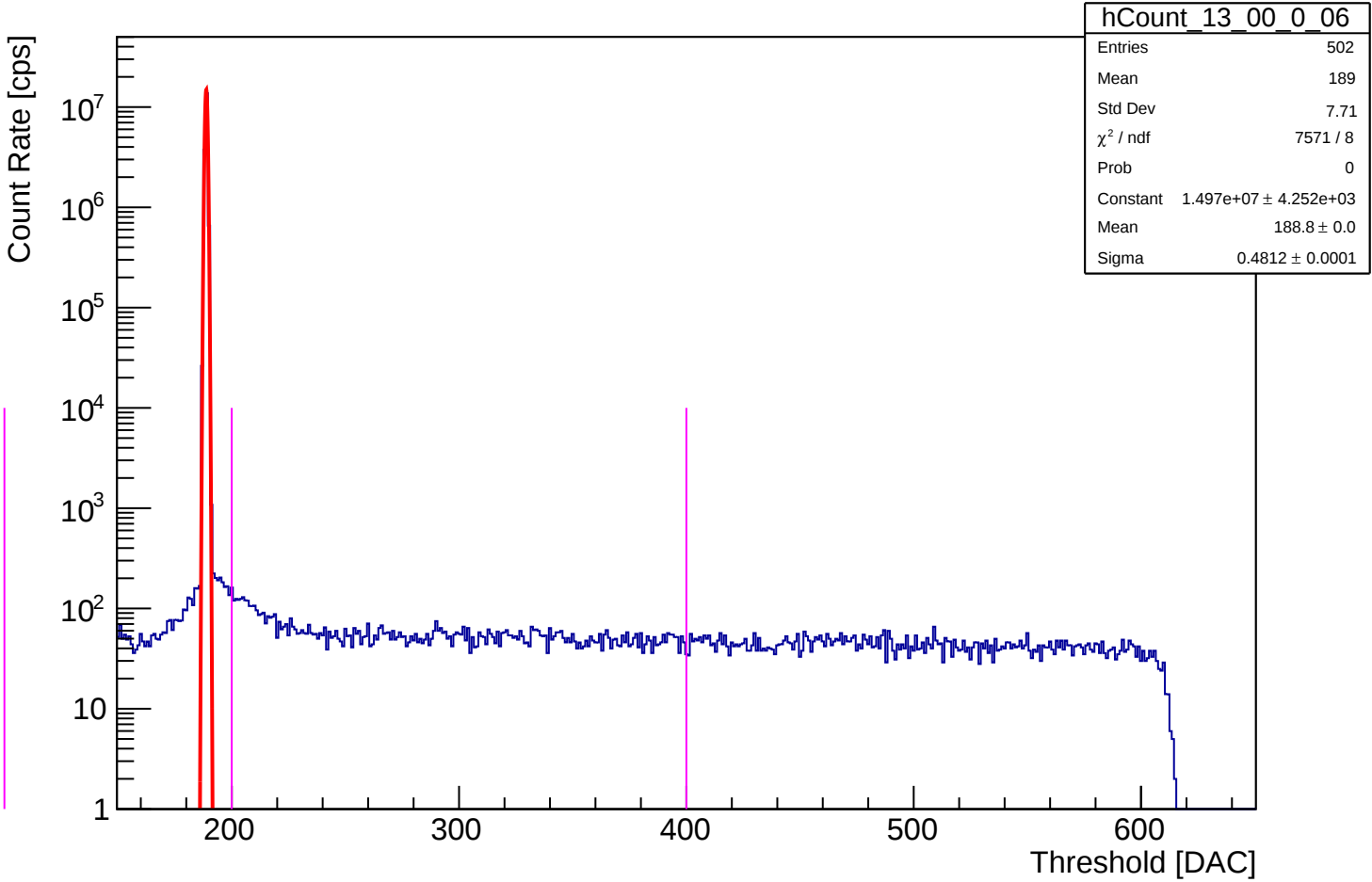


Row 1 Tile 1 Pmt 1 Pixel 48 Slot 13 Fiber 0 Asic 0 Channel 55



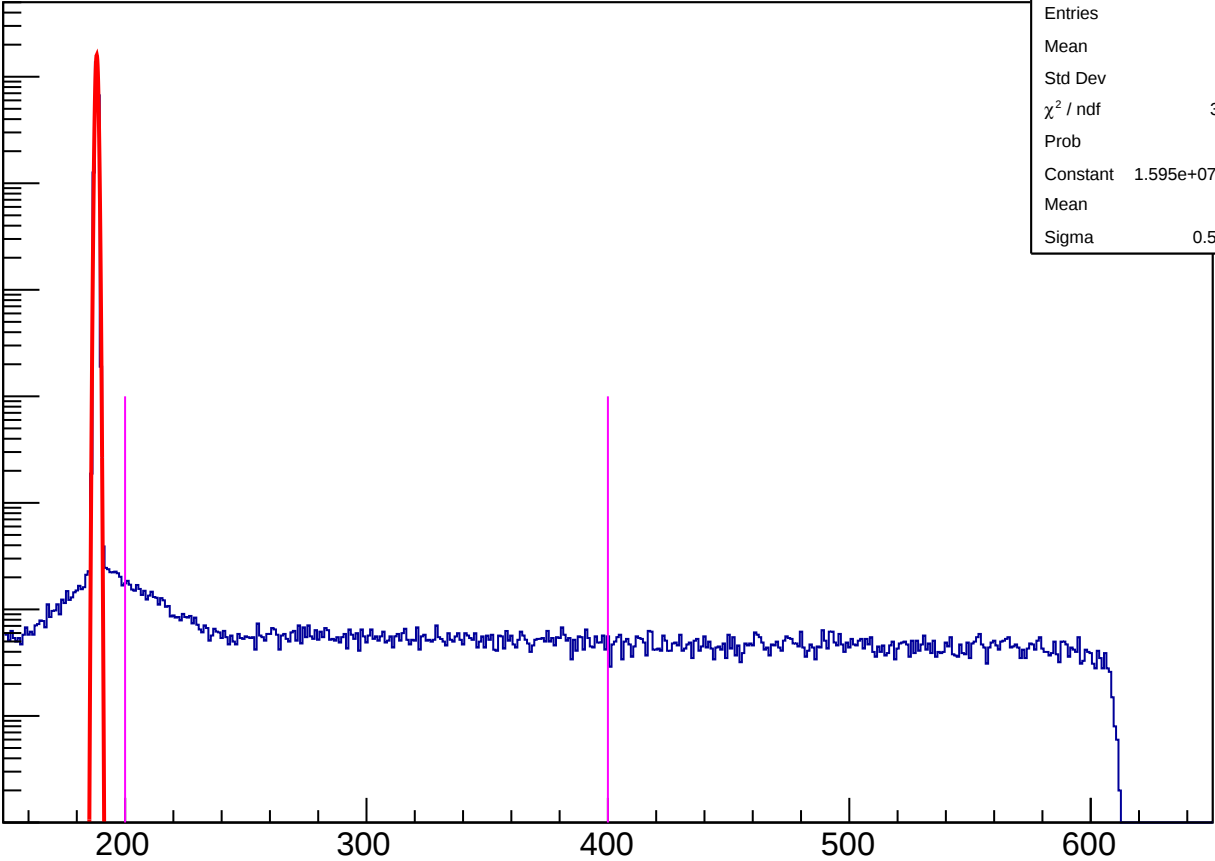






Count Rate [cps]

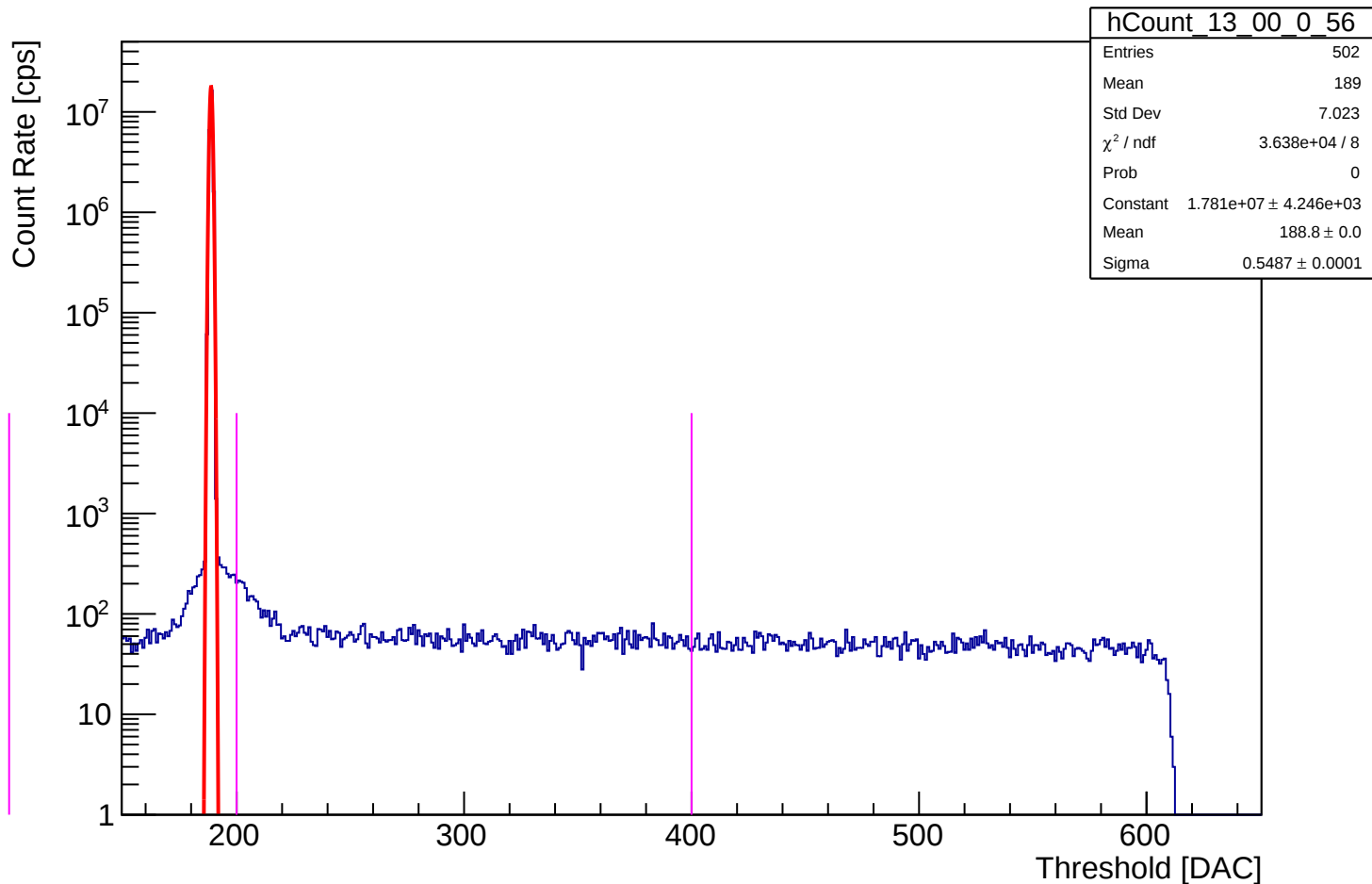
$10^7$   
 $10^6$   
 $10^5$   
 $10^4$   
 $10^3$   
 $10^2$   
 $10$   
 $1$



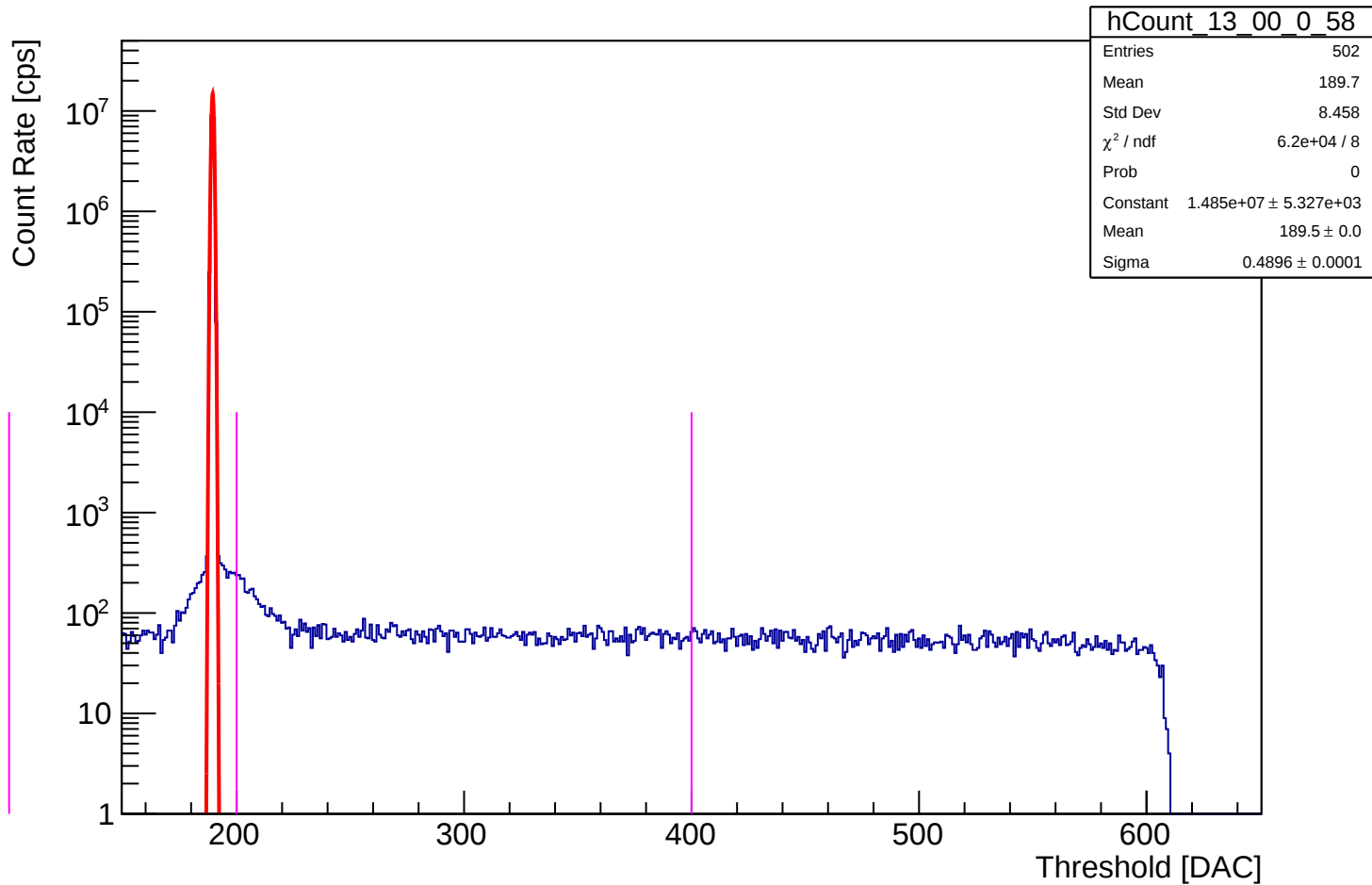
Threshold [DAC]

| hCount_13_00_0_04 |                           |
|-------------------|---------------------------|
| Entries           | 502                       |
| Mean              | 188.4                     |
| Std Dev           | 7.255                     |
| $\chi^2$ / ndf    | 3.184e+05 / 8             |
| Prob              | 0                         |
| Constant          | $1.595e+07 \pm 4.129e+03$ |
| Mean              | $188.3 \pm 0.0$           |
| Sigma             | $0.5322 \pm 0.0001$       |

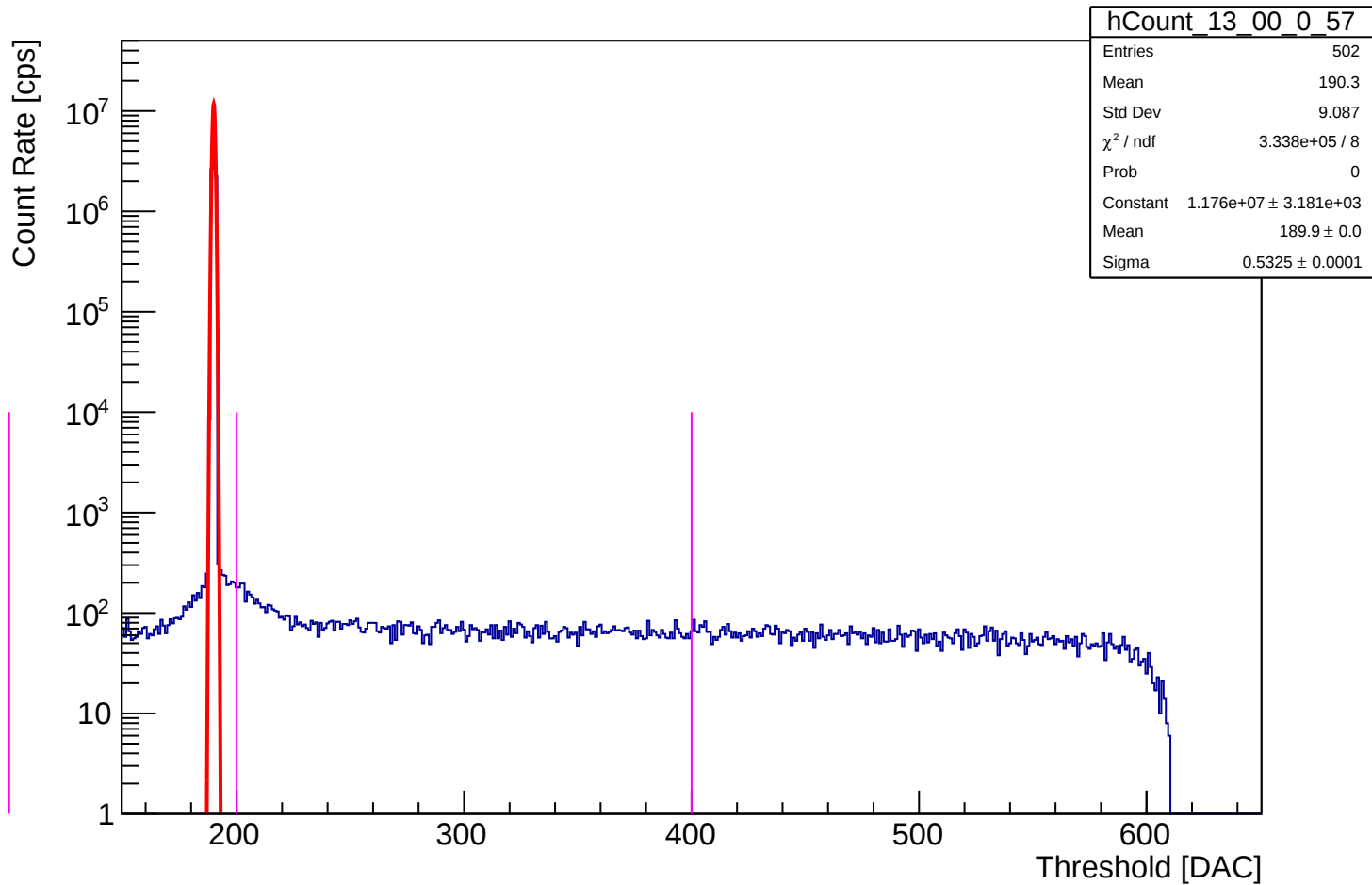
Row 1 Tile 1 Pmt 1 Pixel 53 Slot 13 Fiber 0 Asic 0 Channel 56



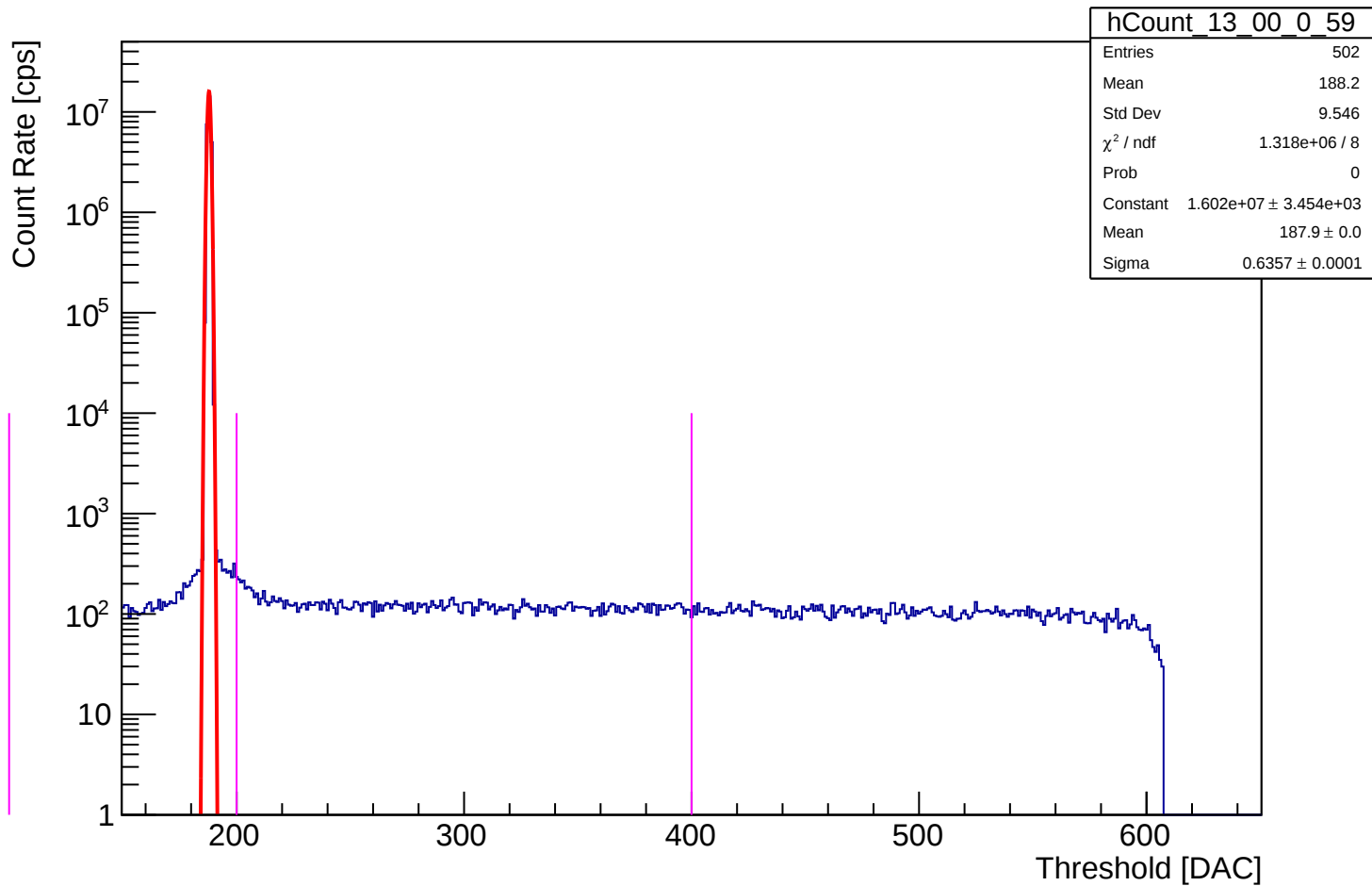
Row 1 Tile 1 Pmt 1 Pixel 54 Slot 13 Fiber 0 Asic 0 Channel 58

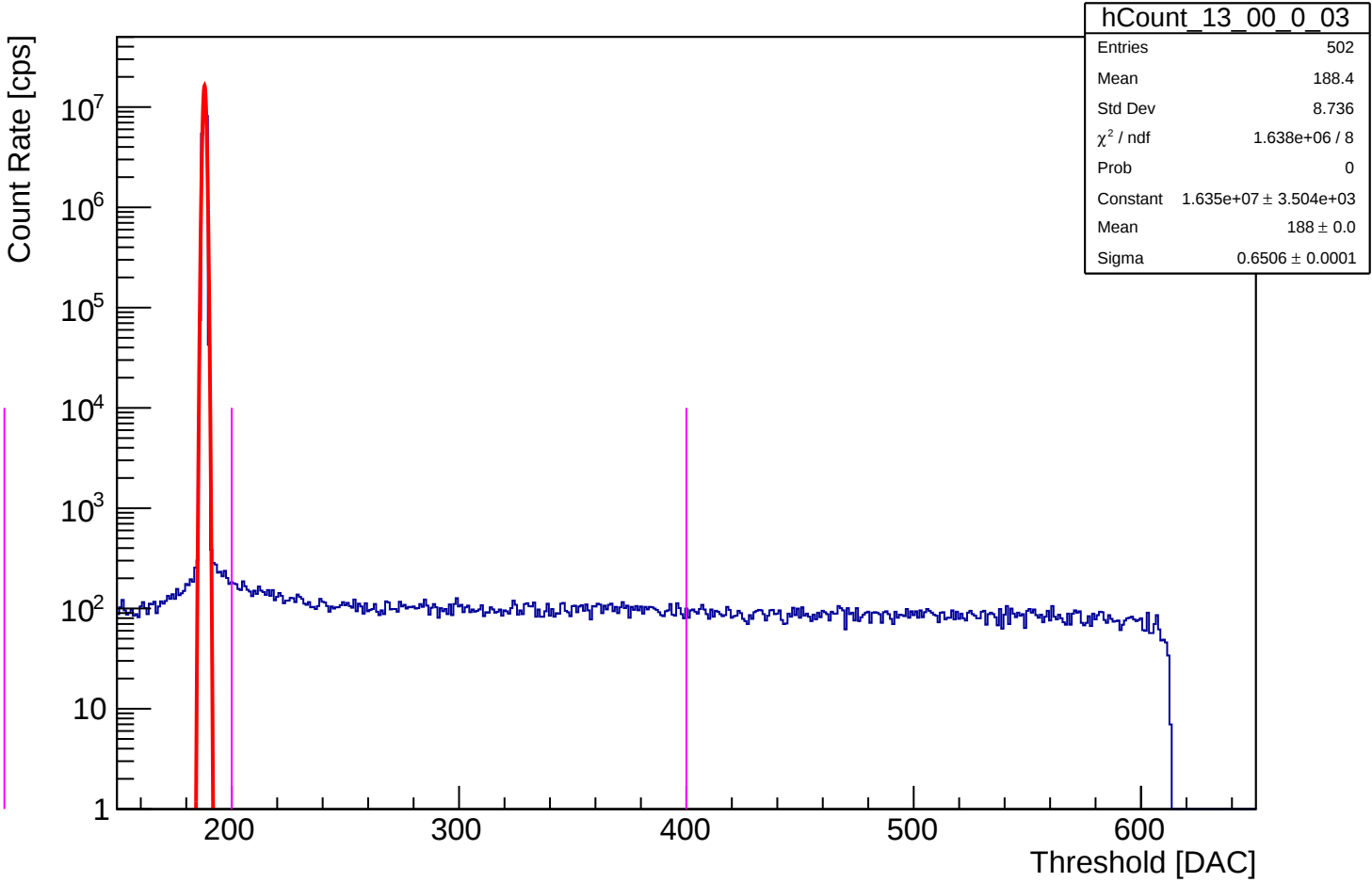


Row 1 Tile 1 Pmt 1 Pixel 55 Slot 13 Fiber 0 Asic 0 Channel 57

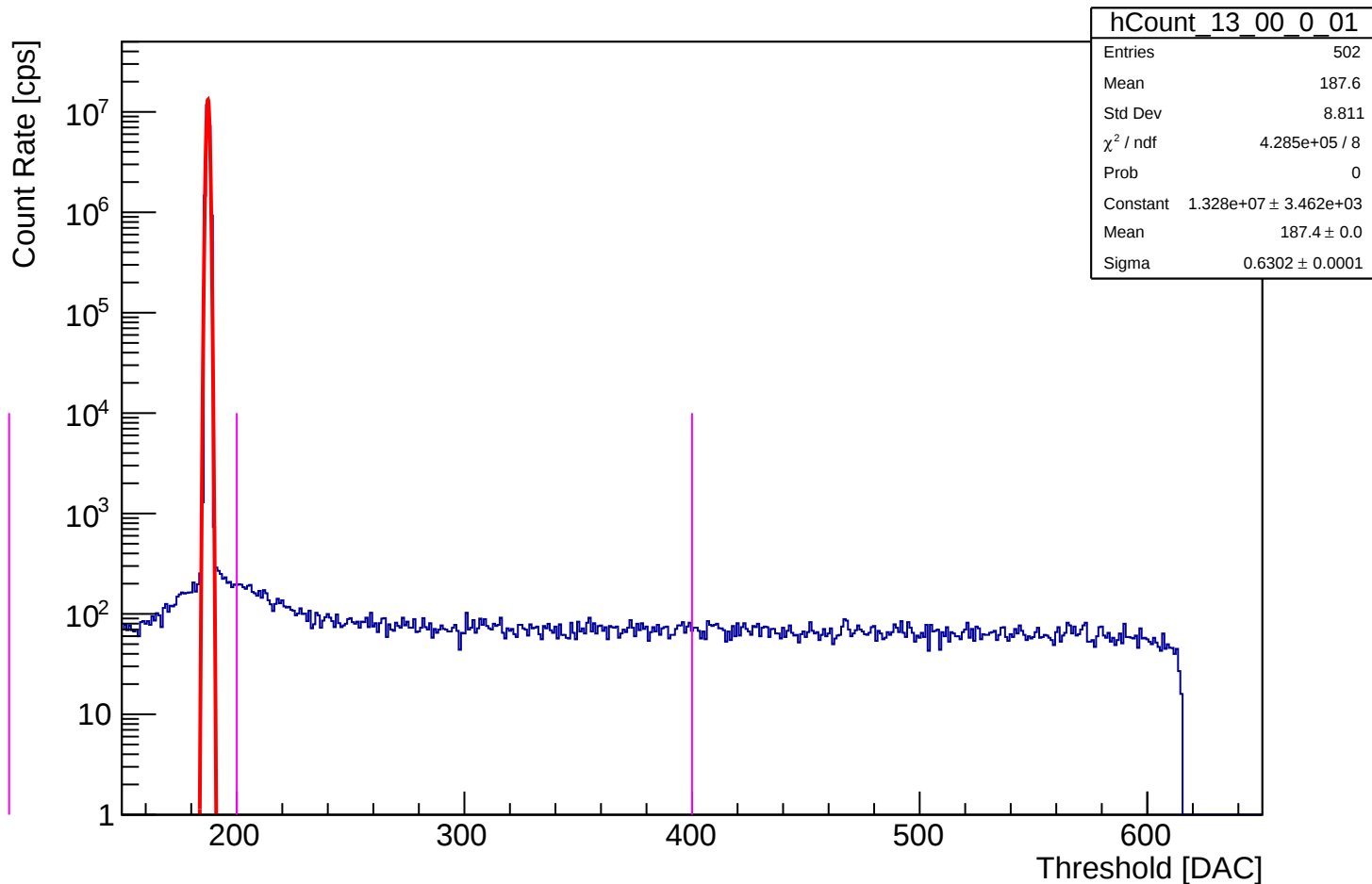


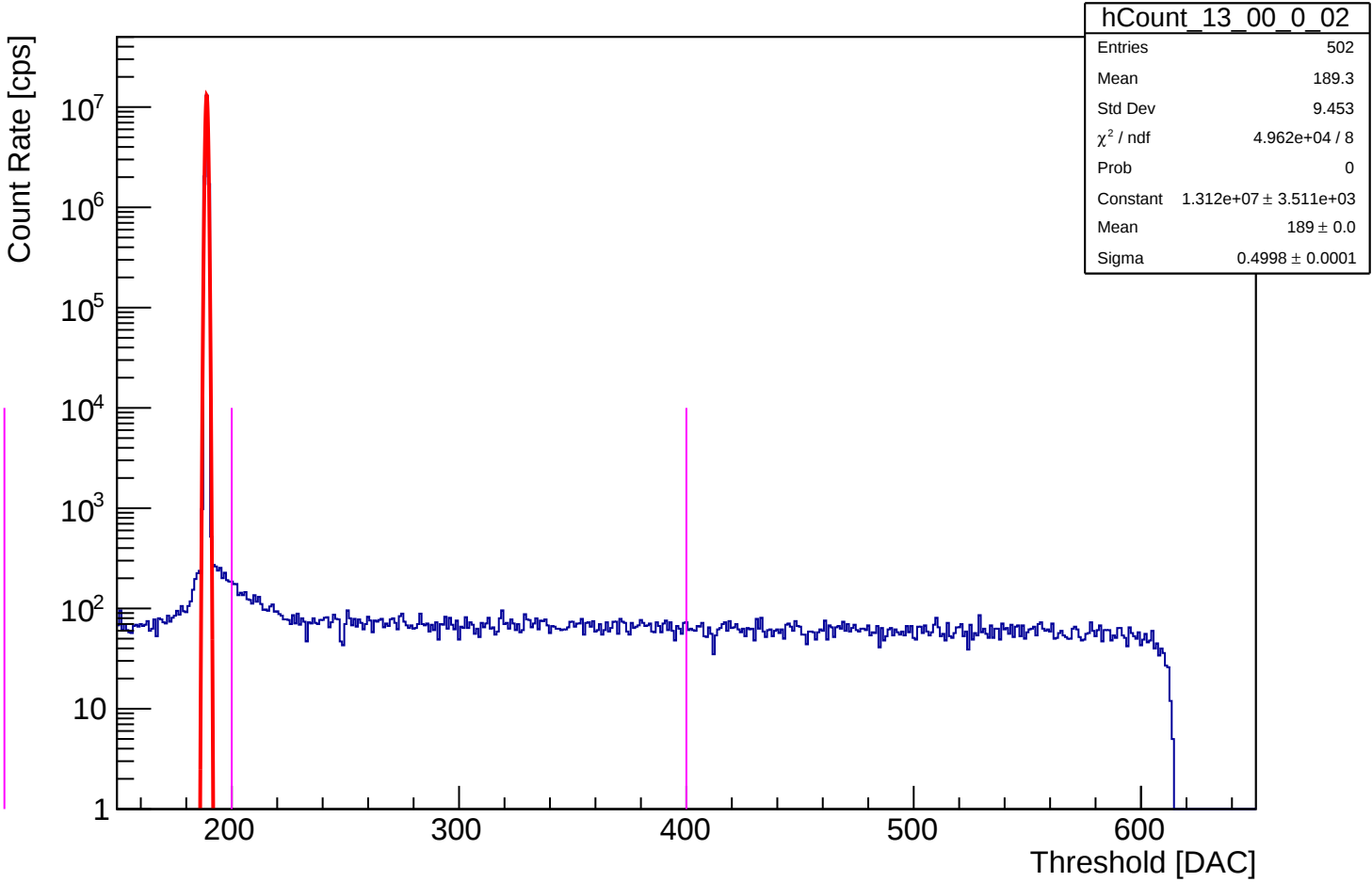
Row 1 Tile 1 Pmt 1 Pixel 56 Slot 13 Fiber 0 Asic 0 Channel 59

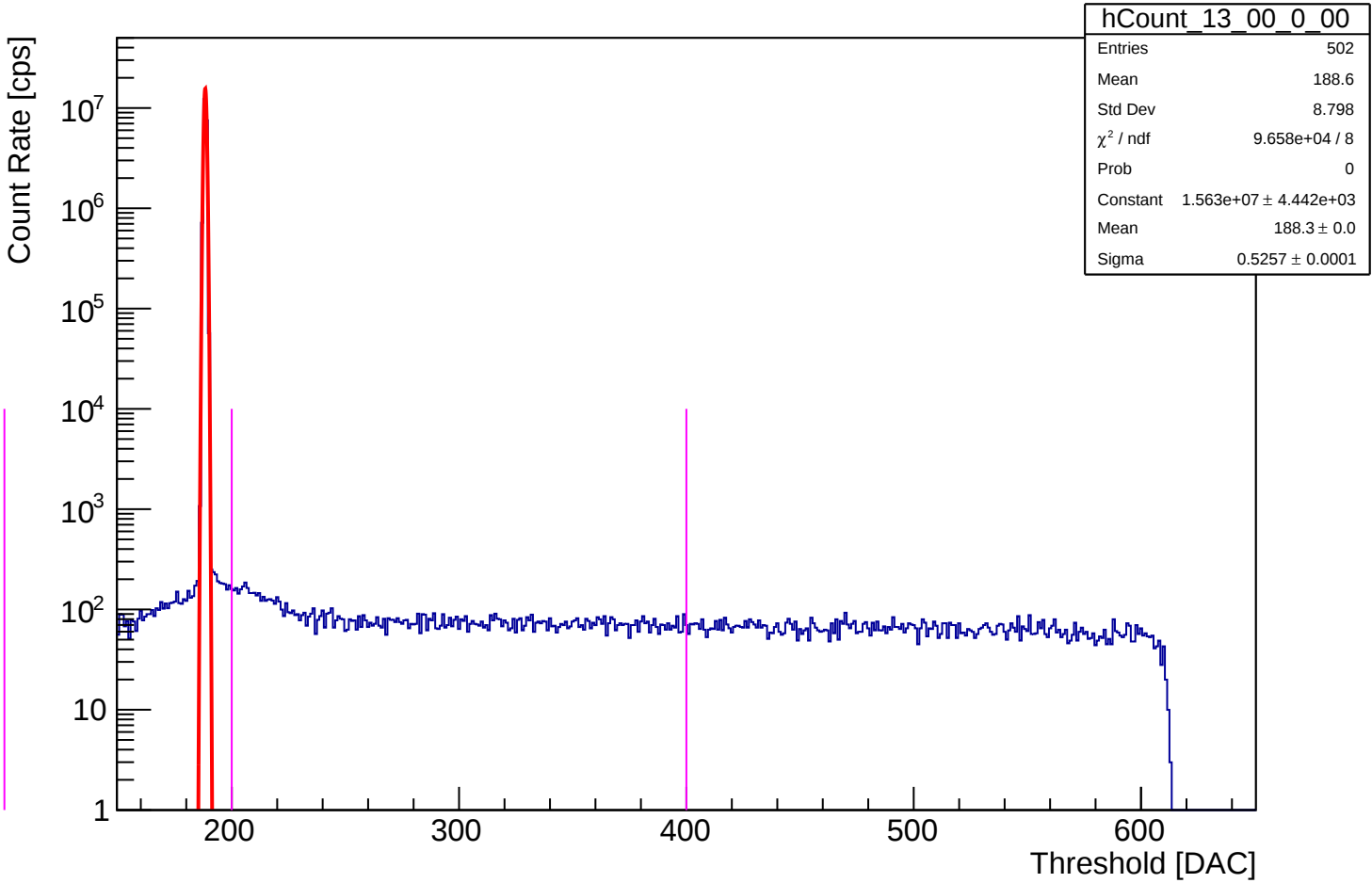




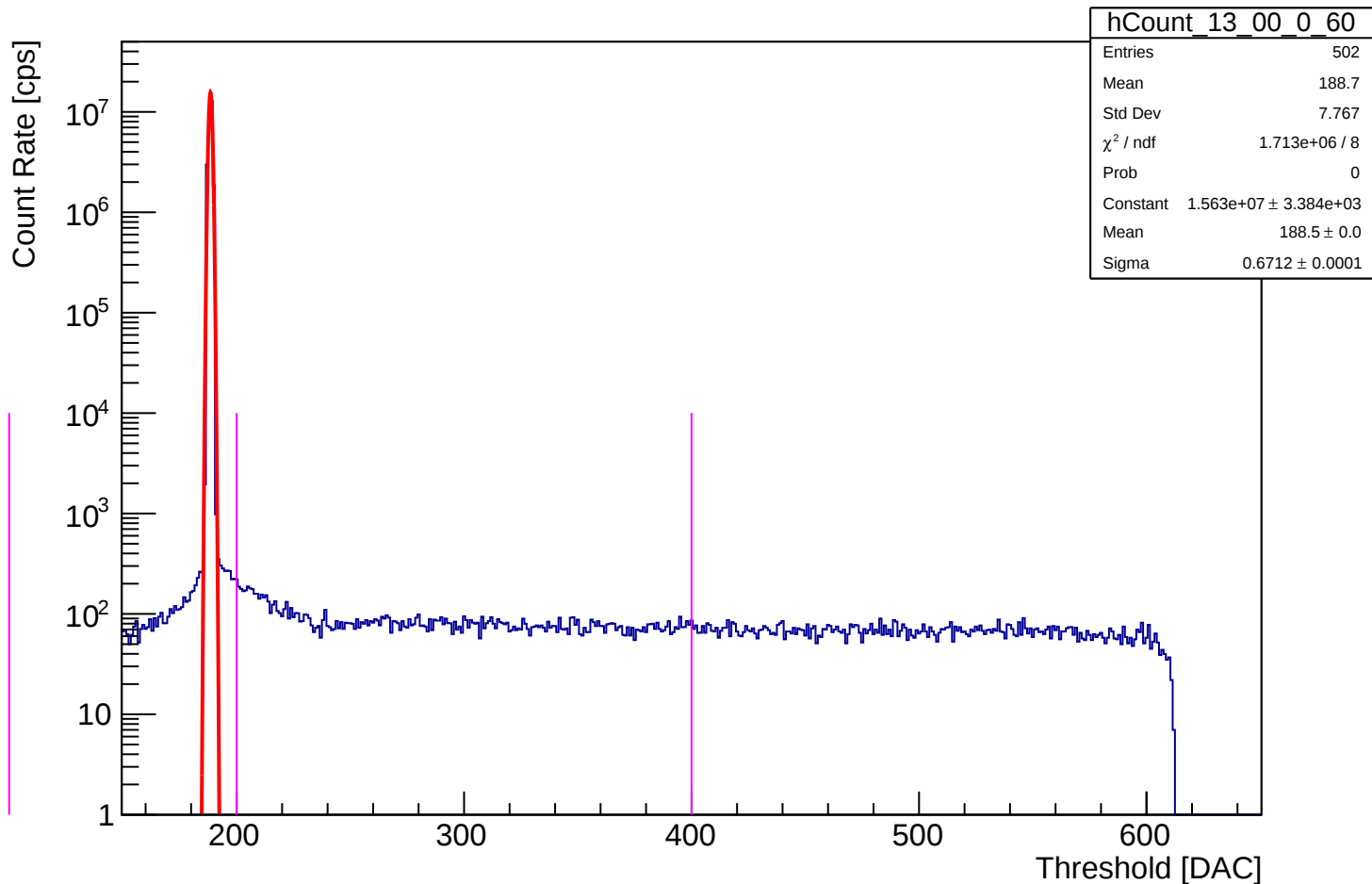
Row 1 Tile 1 Pmt 1 Pixel 58 Slot 13 Fiber 0 Asic 0 Channel 1



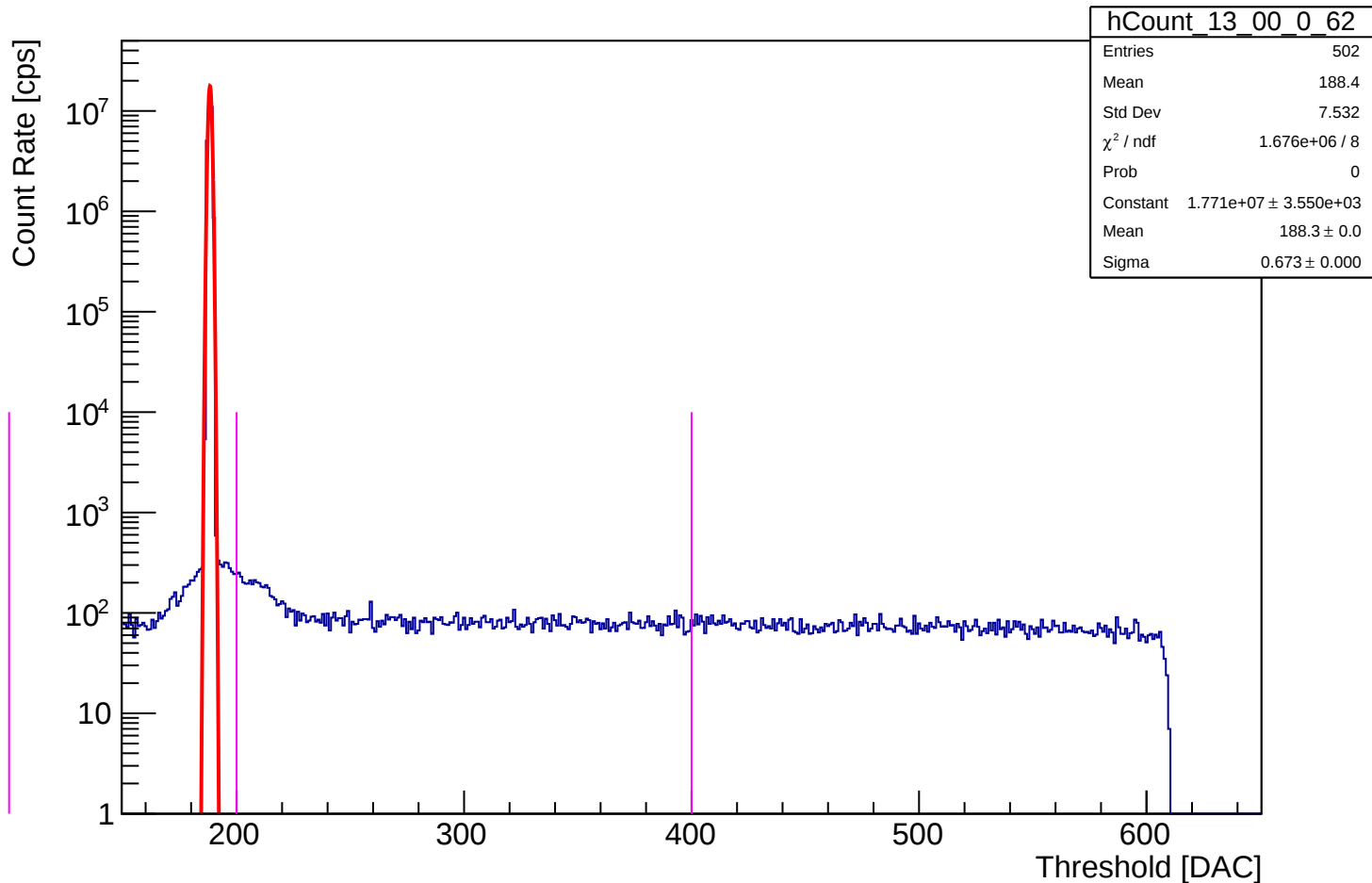




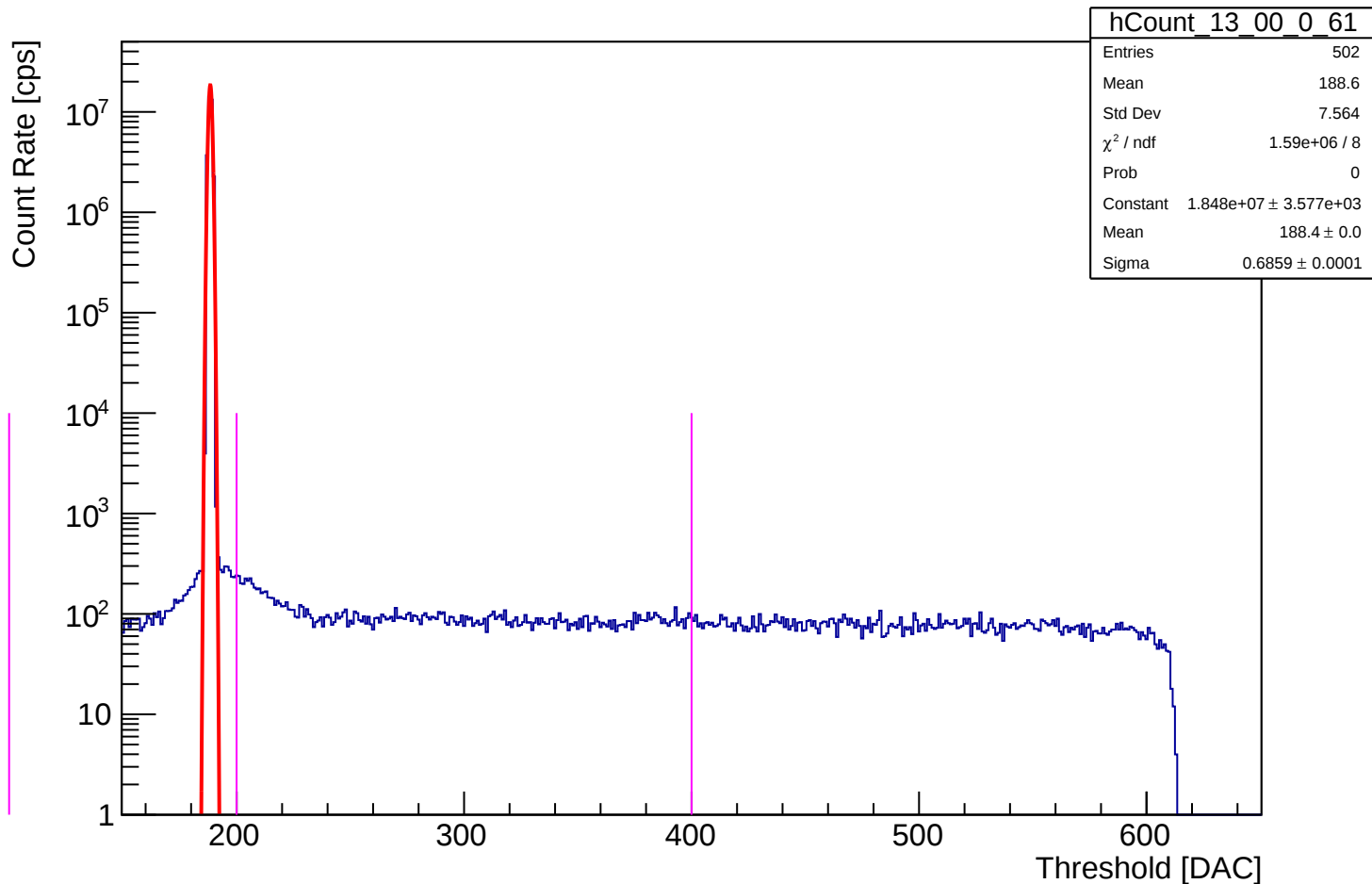
Row 1 Tile 1 Pmt 1 Pixel 61 Slot 13 Fiber 0 Asic 0 Channel 60



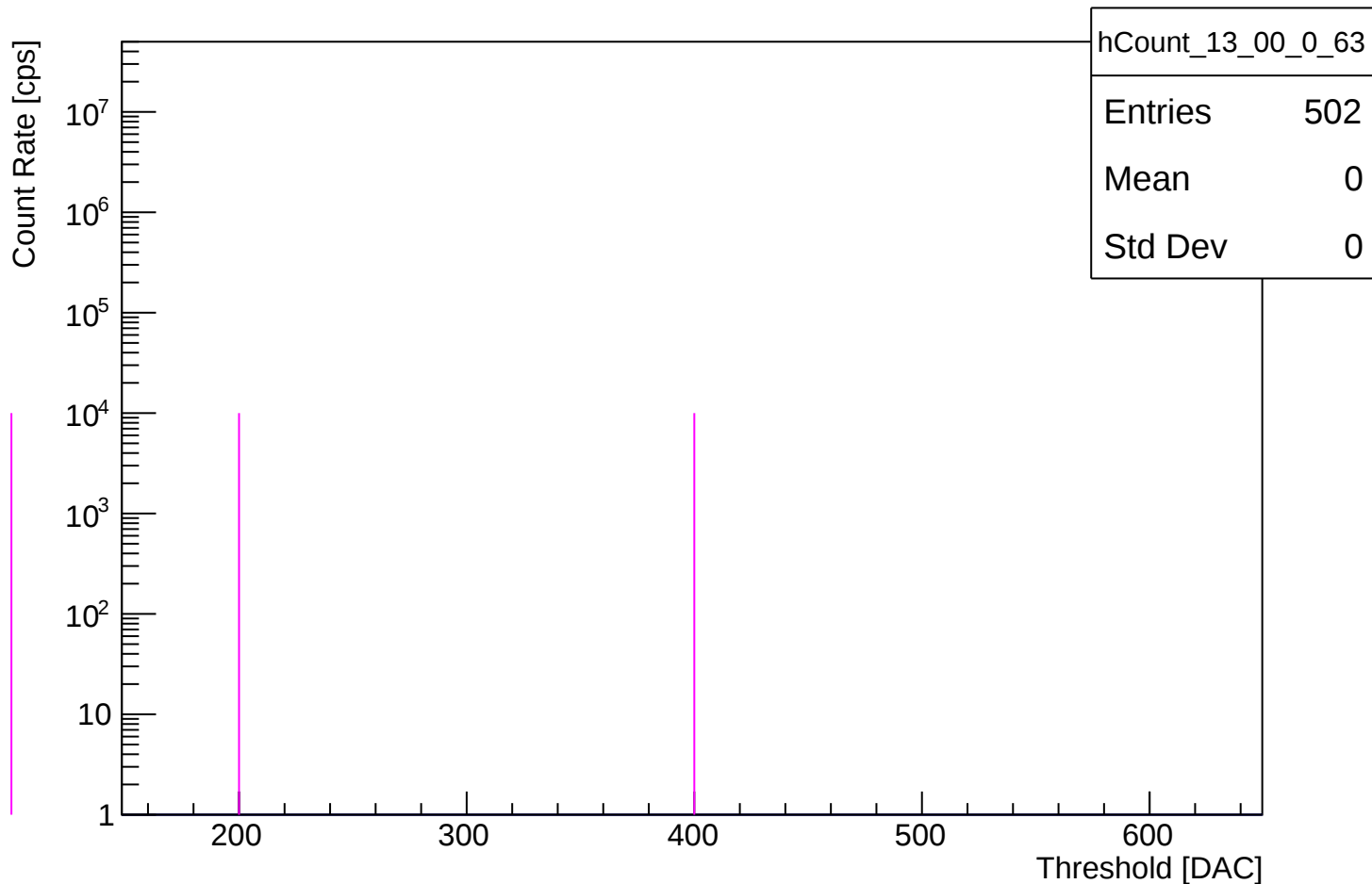
Row 1 Tile 1 Pmt 1 Pixel 62 Slot 13 Fiber 0 Asic 0 Channel 62



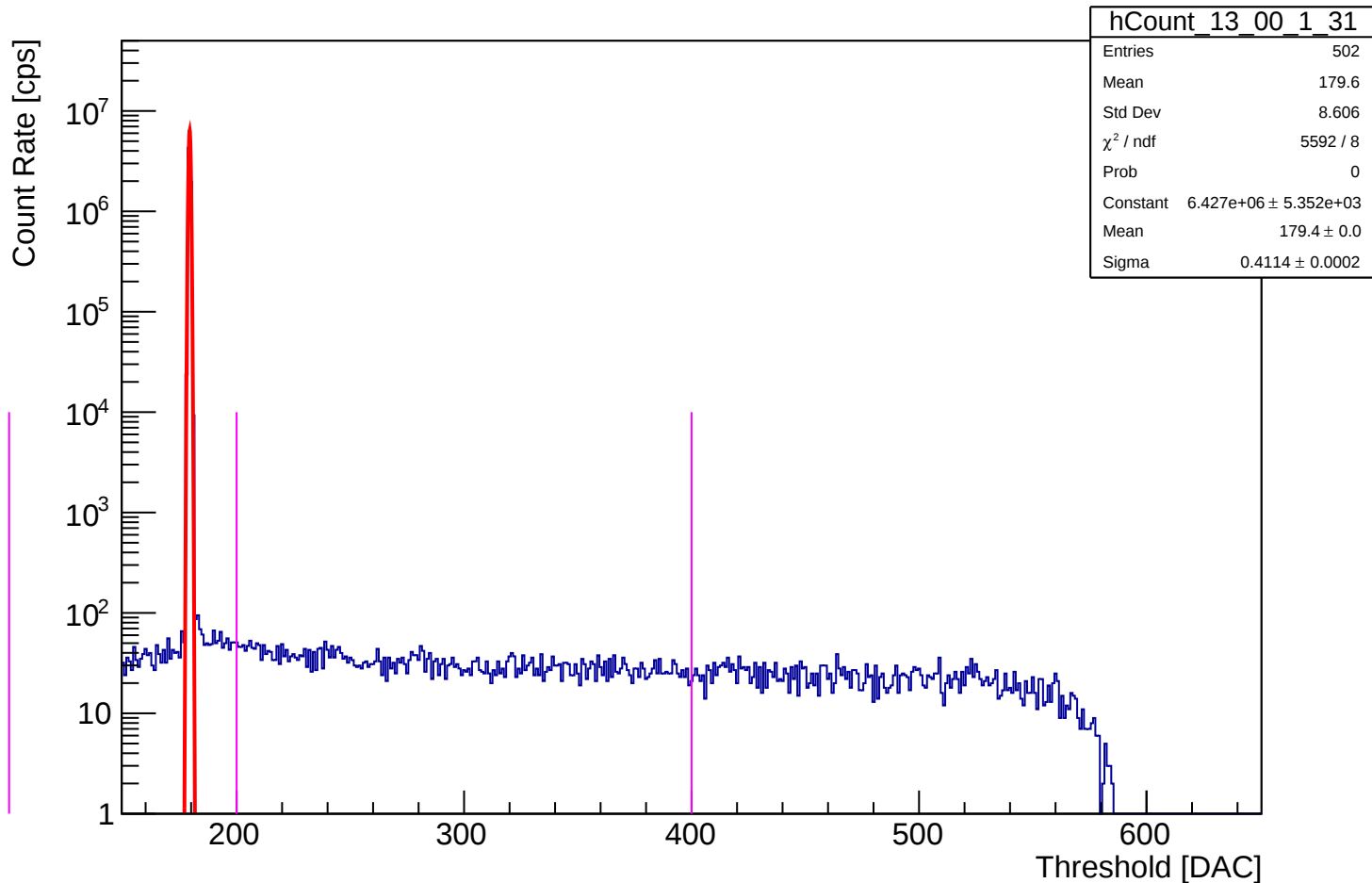
Row 1 Tile 1 Pmt 1 Pixel 63 Slot 13 Fiber 0 Asic 0 Channel 61



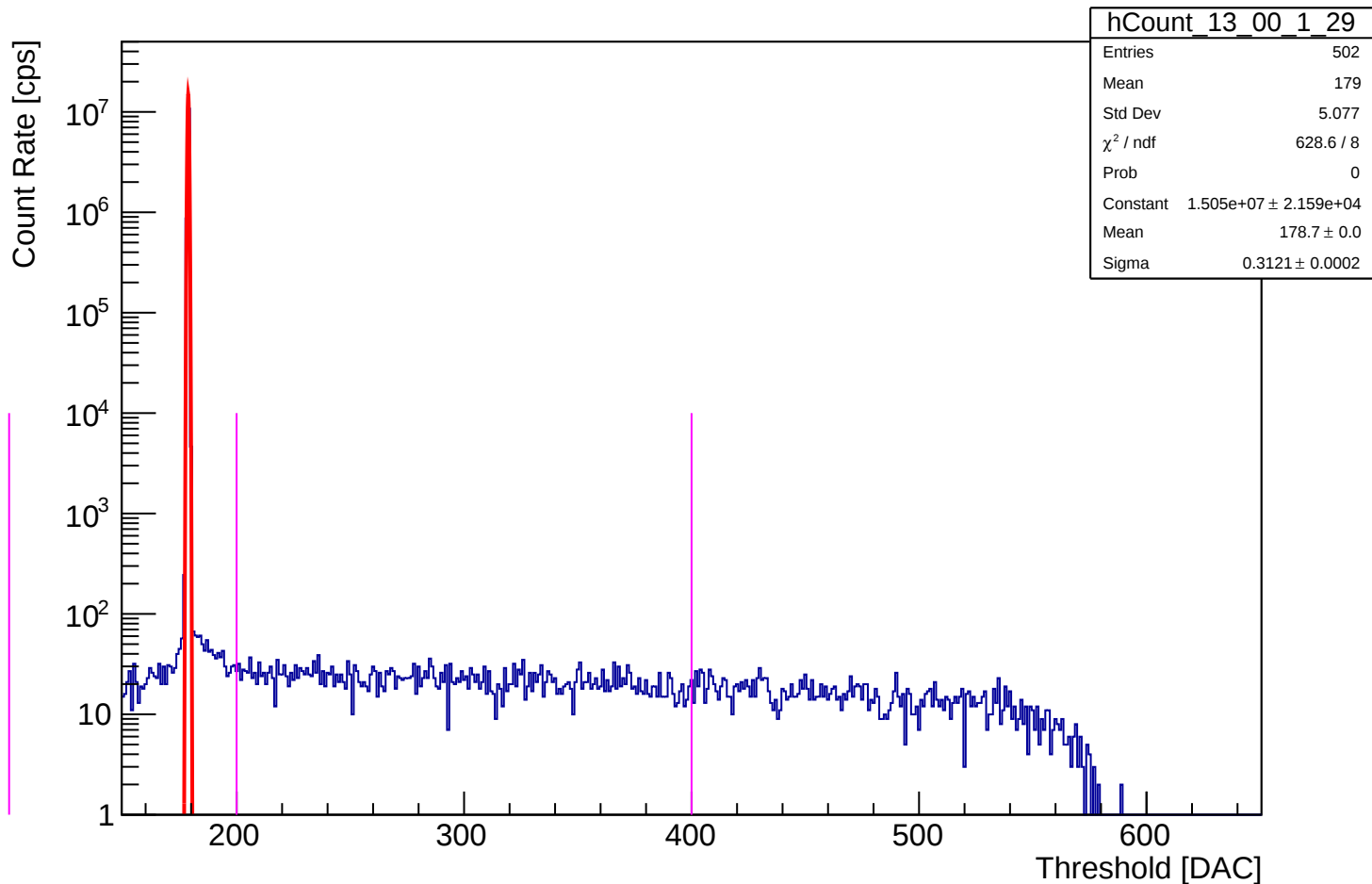
Row 1 Tile 1 Pmt 1 Pixel 64 Slot 13 Fiber 0 Asic 0 Channel 63



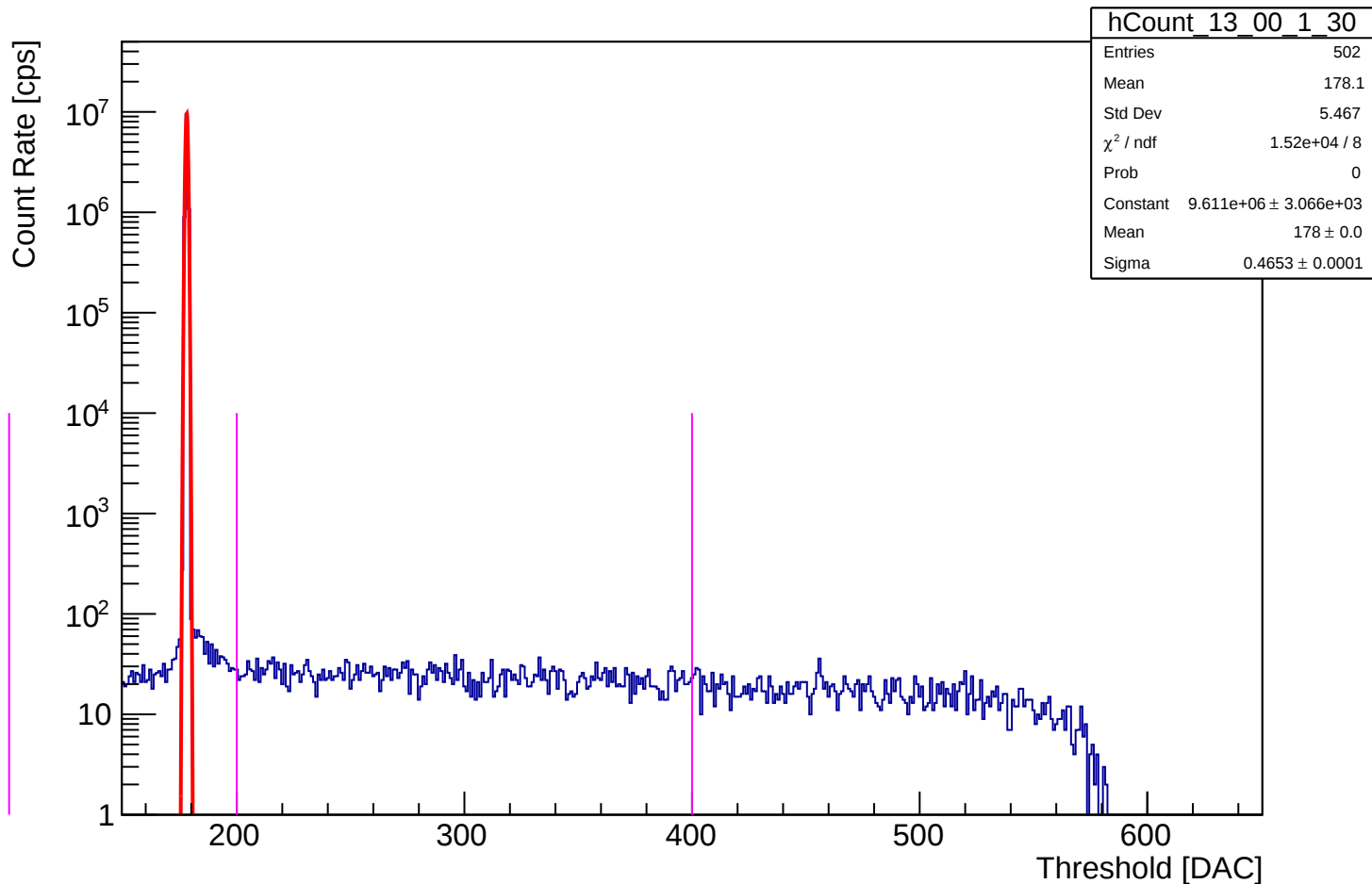
Row 1 Tile 1 Pmt 2 Pixel 1 Slot 13 Fiber 0 Asic 1 Channel 31



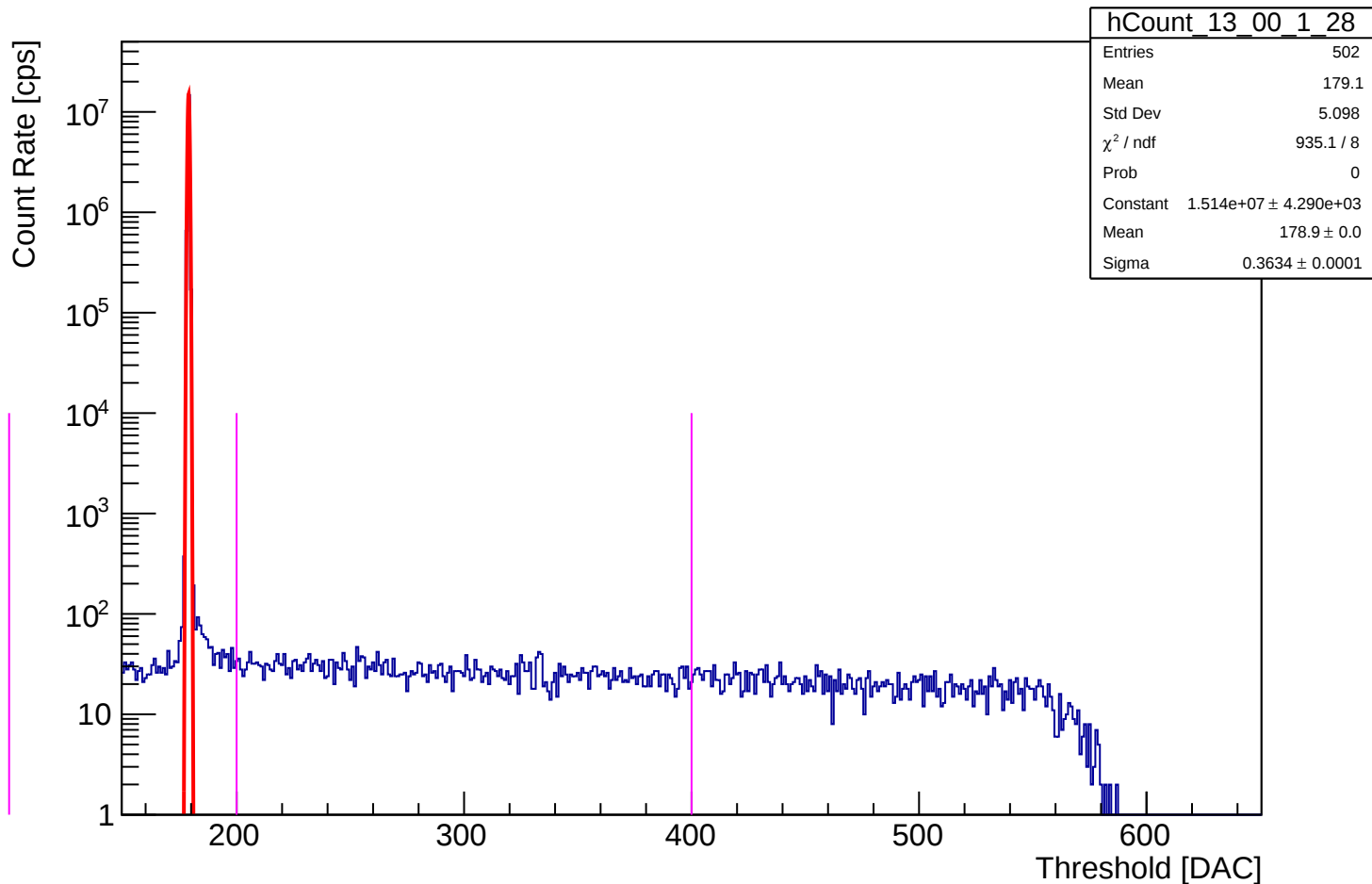
Row 1 Tile 1 Pmt 2 Pixel 2 Slot 13 Fiber 0 Asic 1 Channel 29



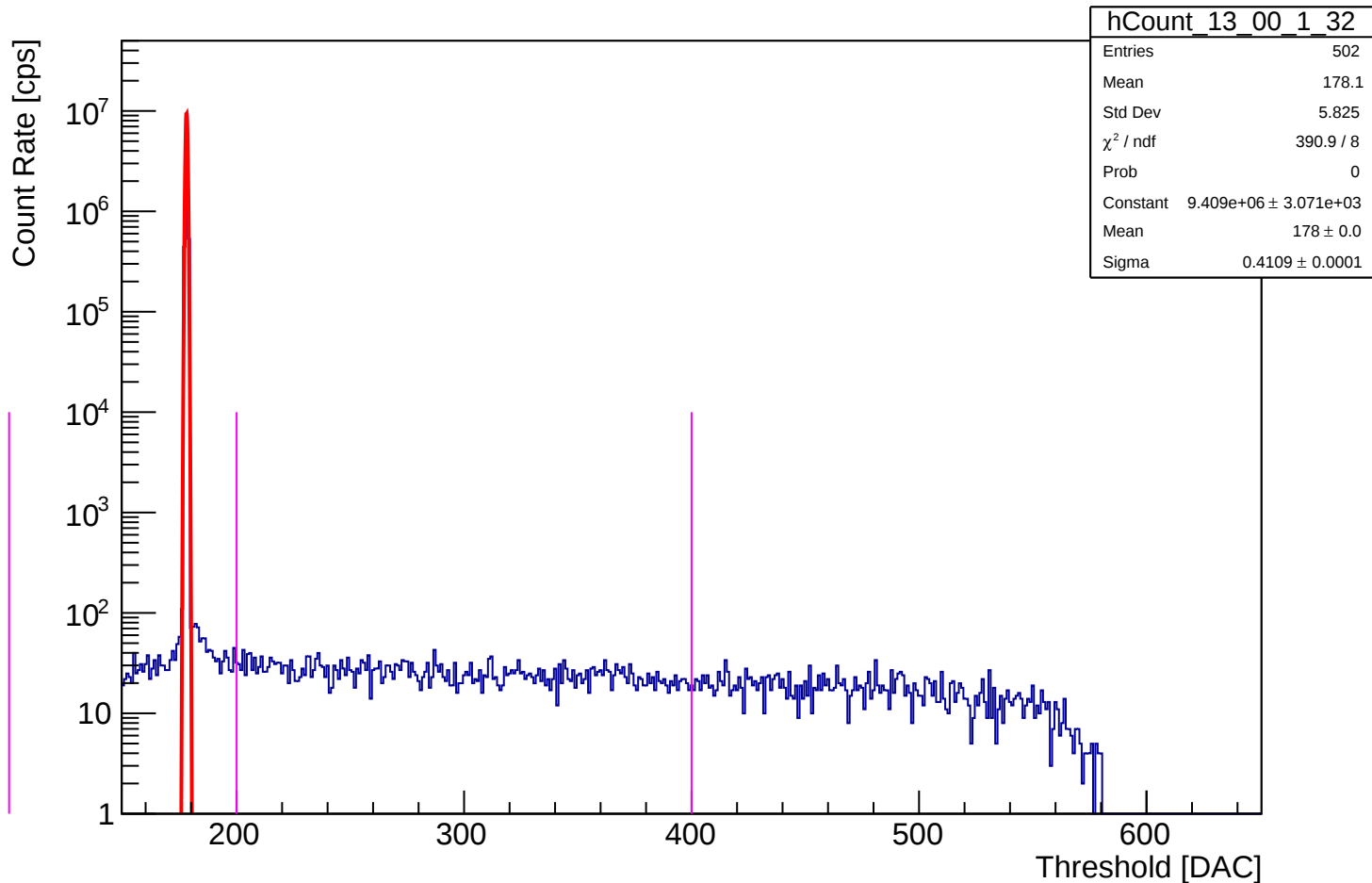
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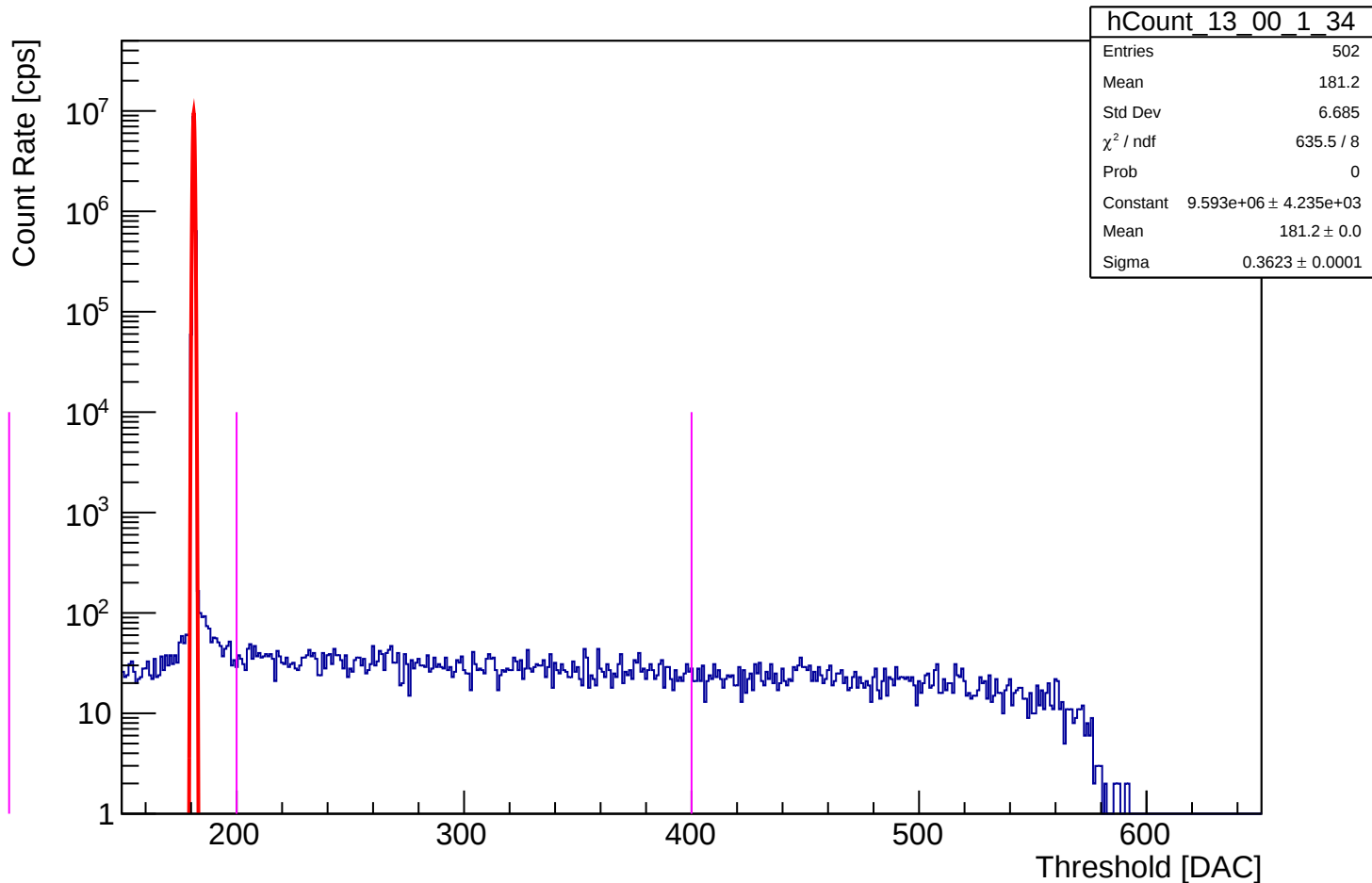
Row 1 Tile 1 Pmt 2 Pixel 4 Slot 13 Fiber 0 Asic 1 Channel 28



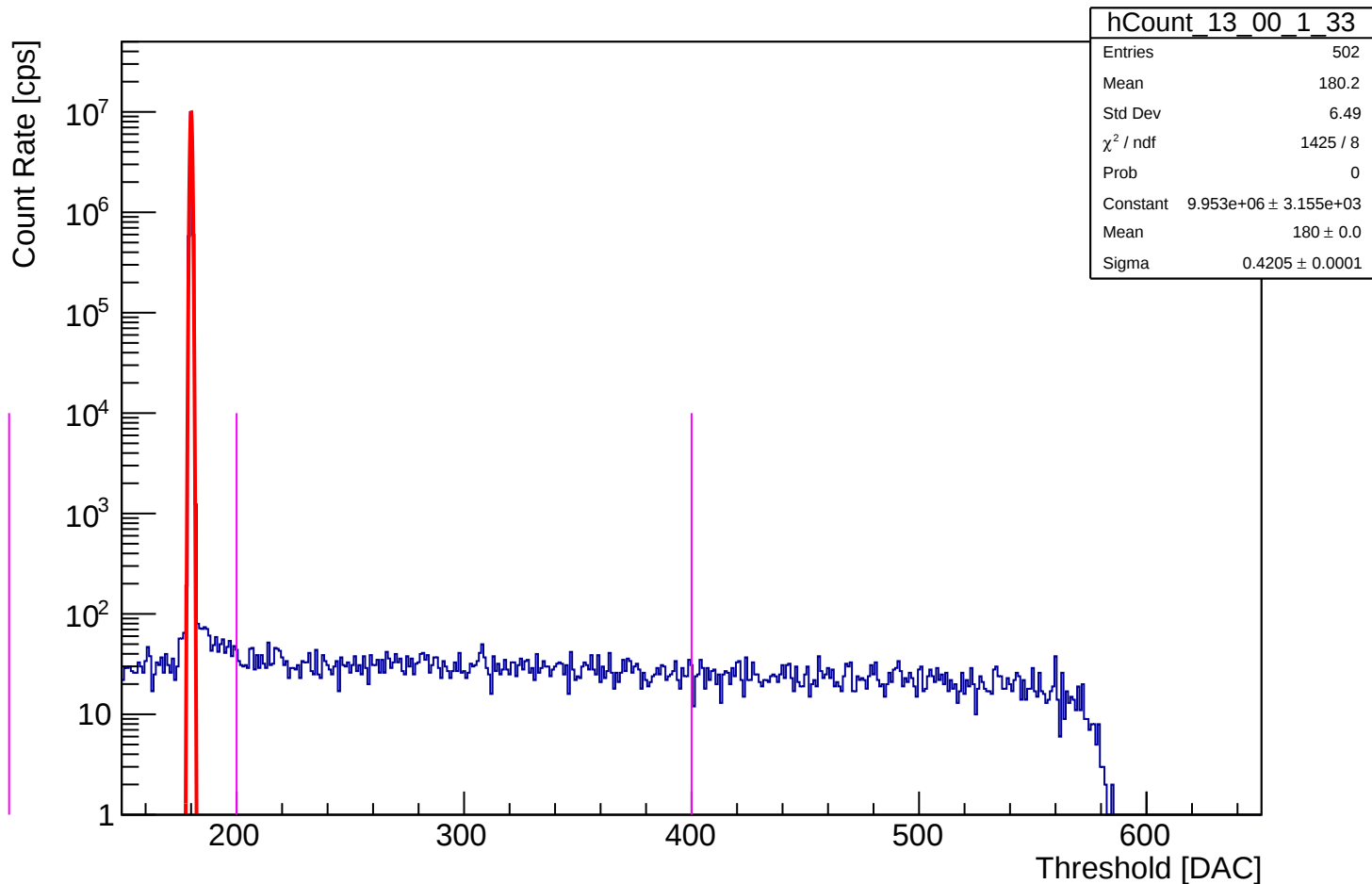
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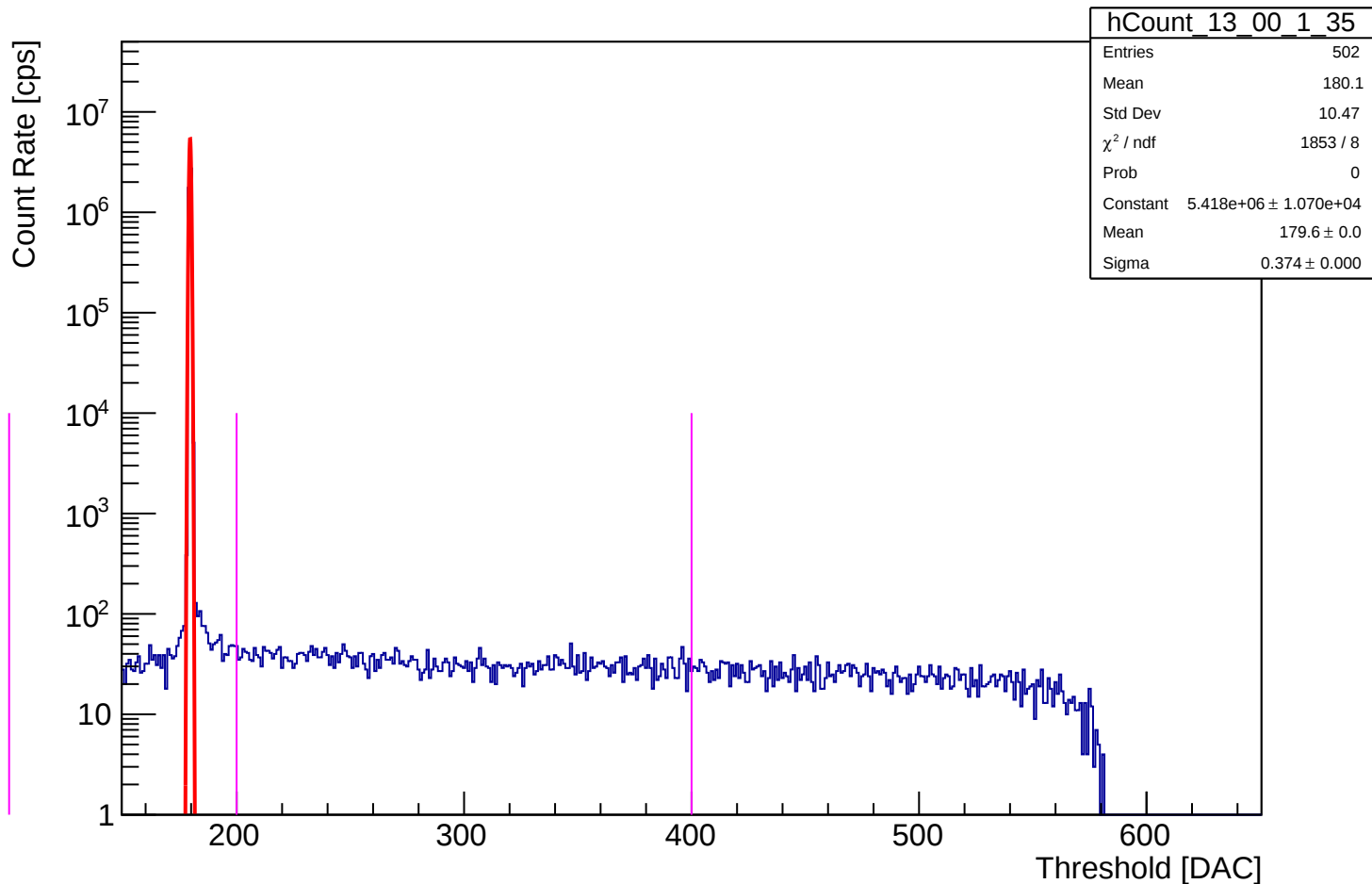
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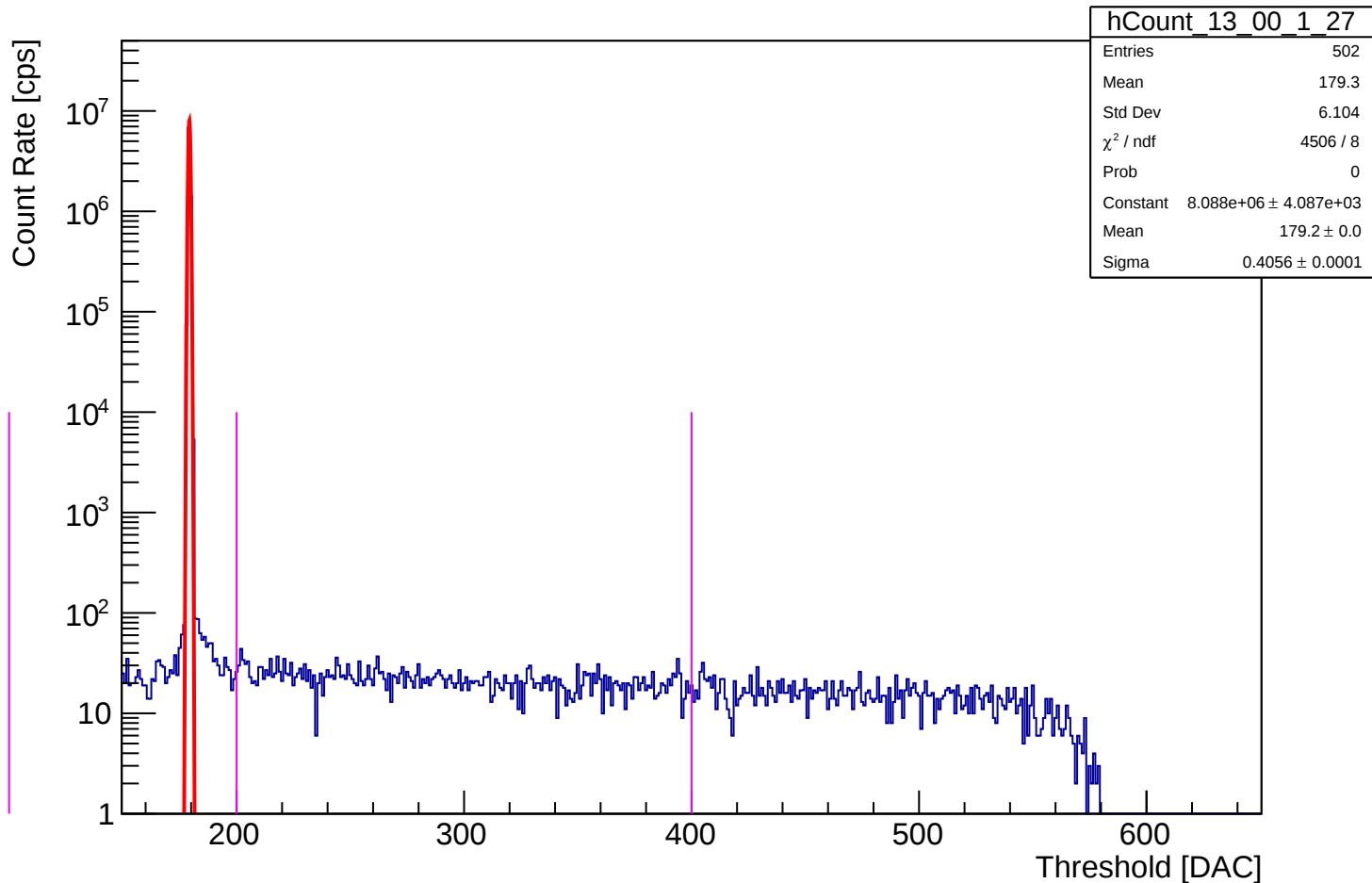
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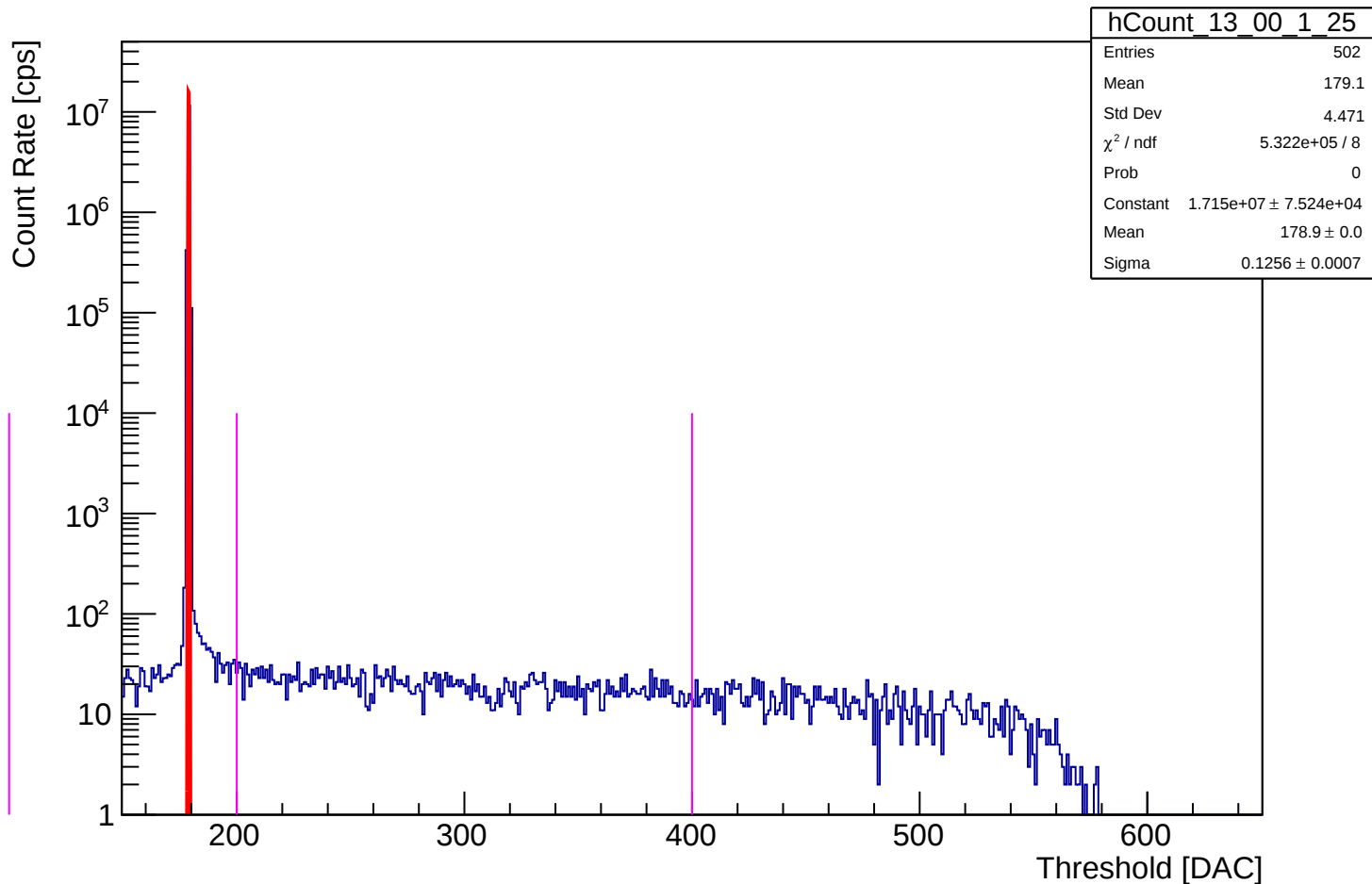
Row 1 Tile 1 Pmt 2 Pixel 8 Slot 13 Fiber 0 Asic 1 Channel 35



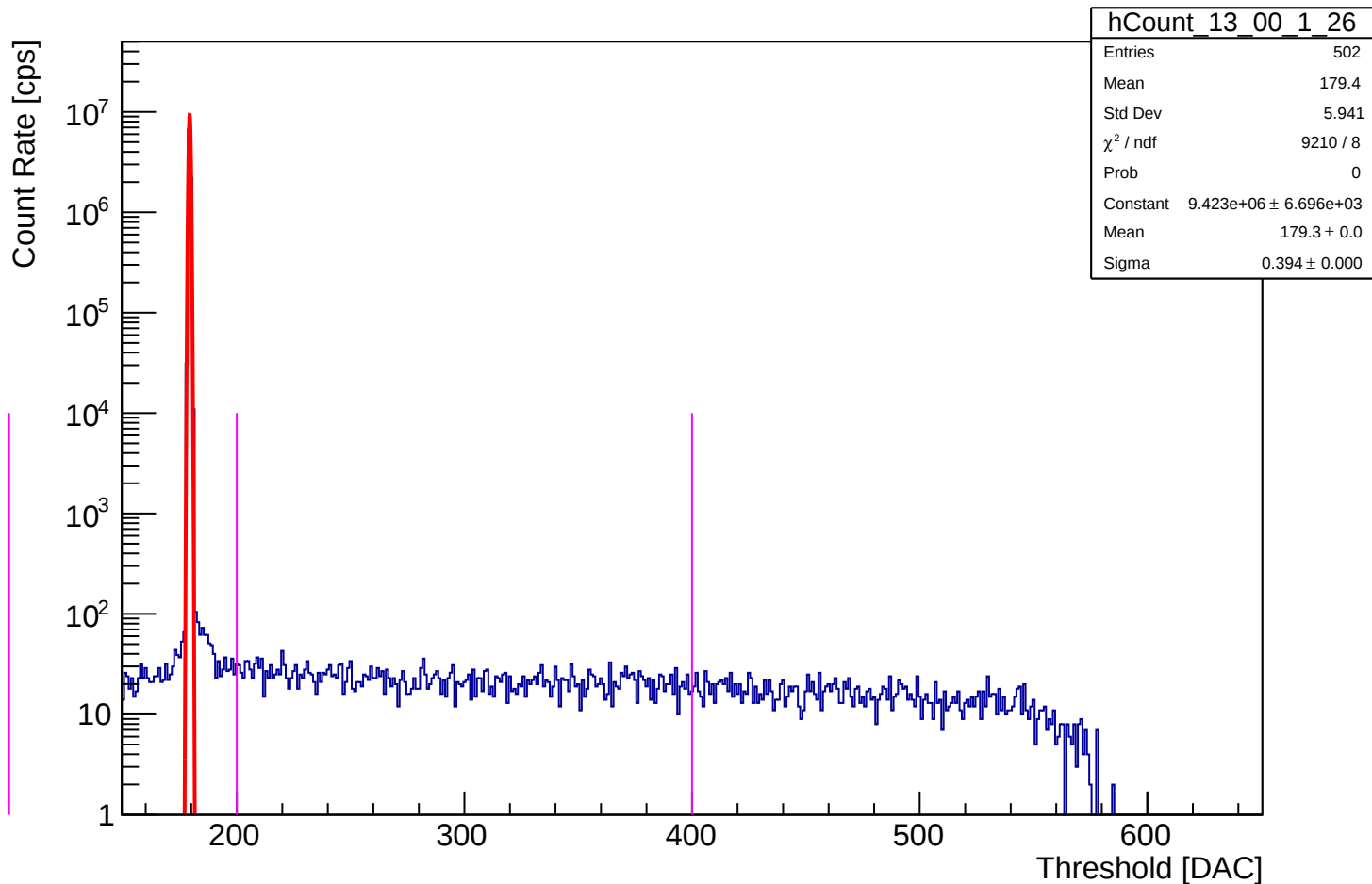
Row 1 Tile 1 Pmt 2 Pixel 9 Slot 13 Fiber 0 Asic 1 Channel 27



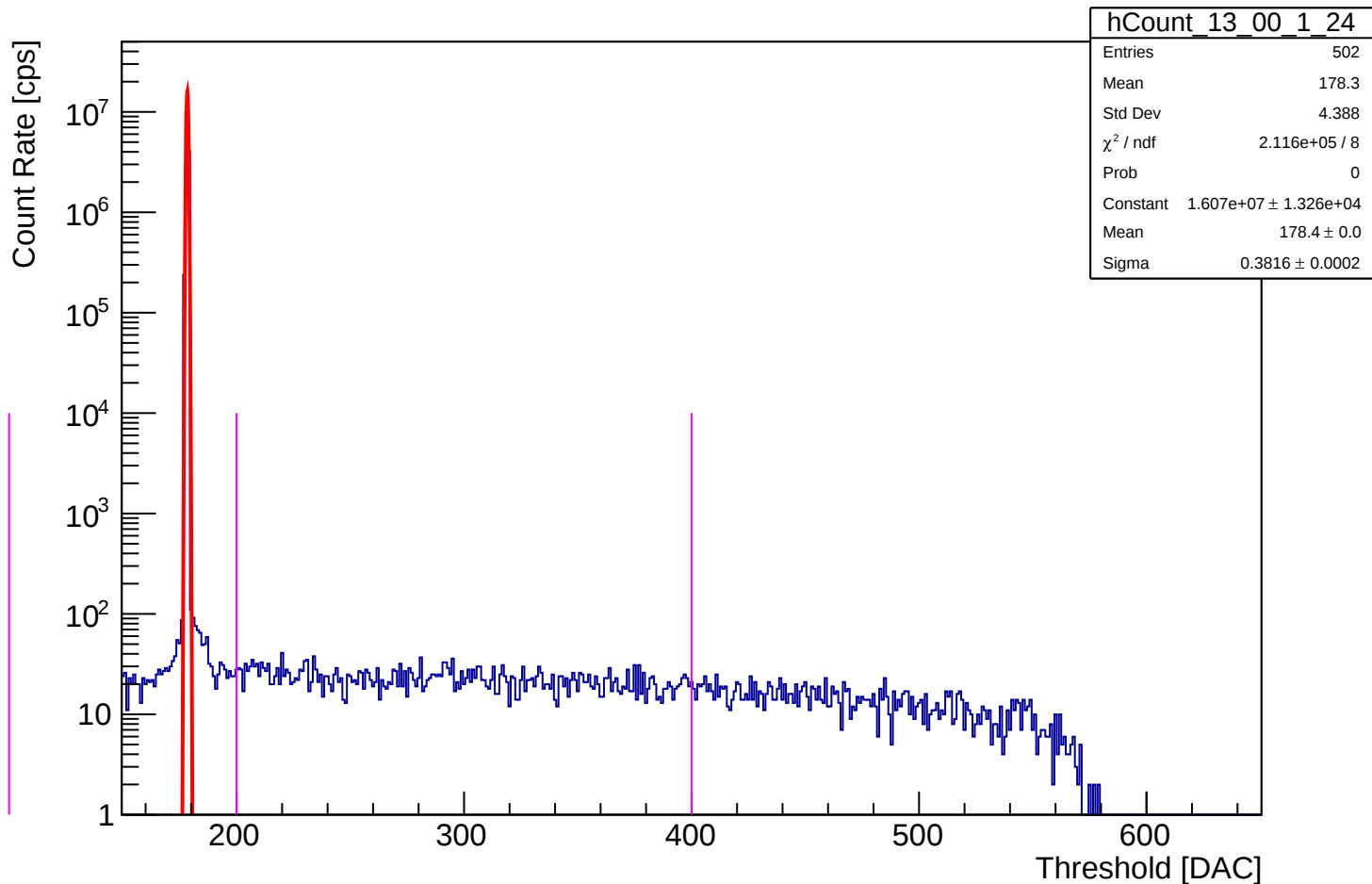
Row 1 Tile 1 Pmt 2 Pixel 10 Slot 13 Fiber 0 Asic 1 Channel 25



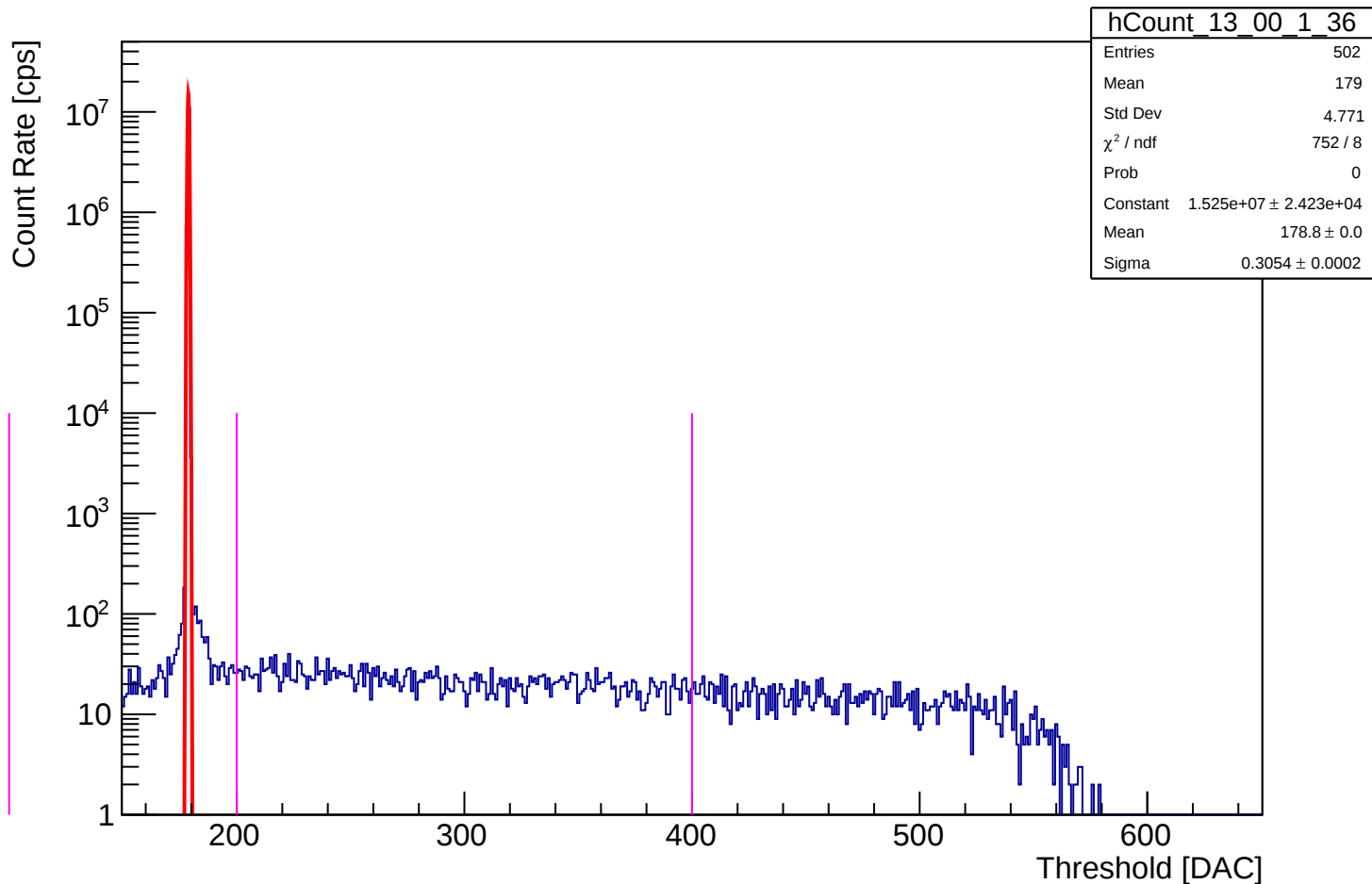
Row 1 Tile 1 Pmt 2 Pixel 11 Slot 13 Fiber 0 Asic 1 Channel 26



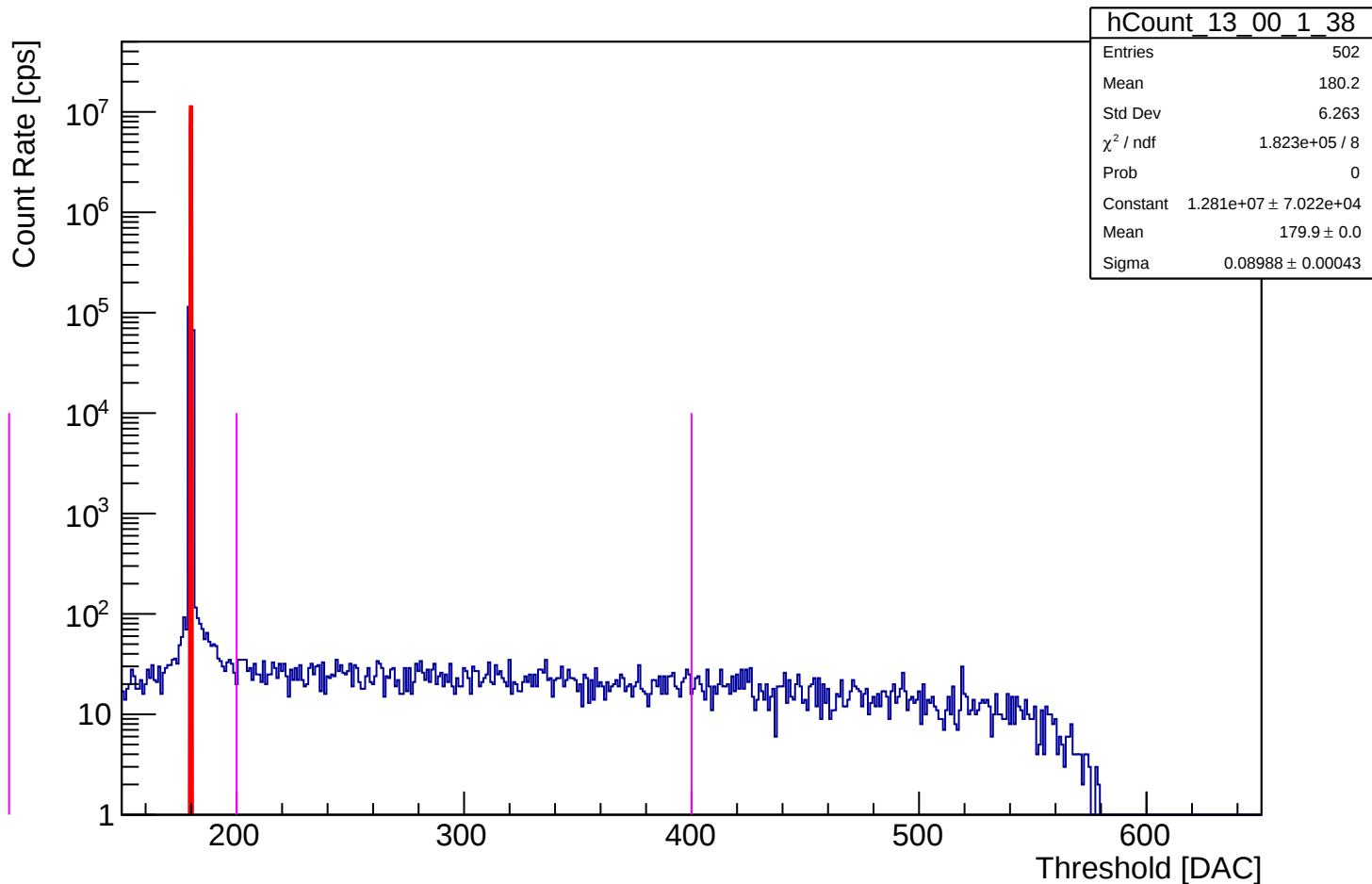
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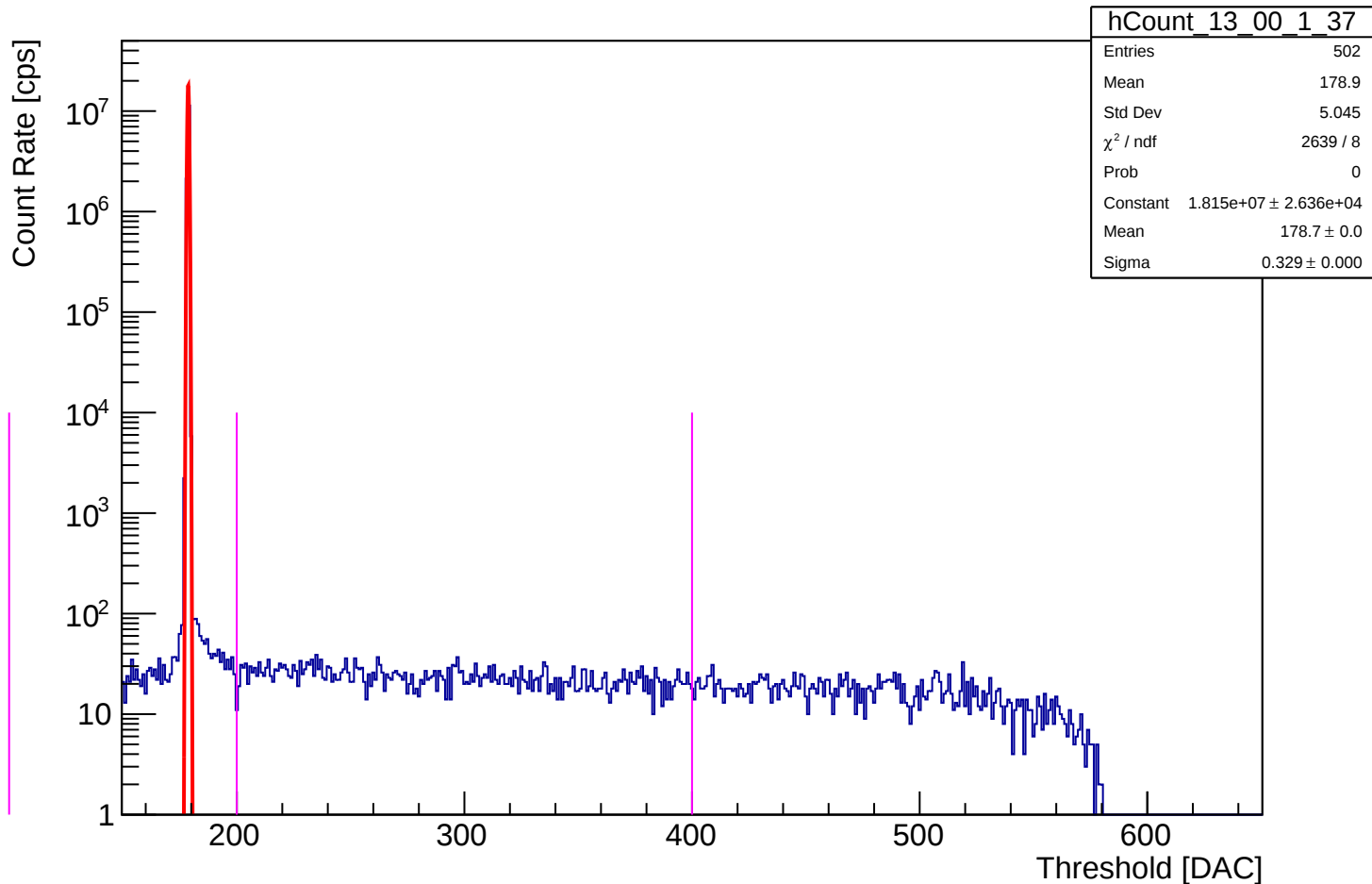
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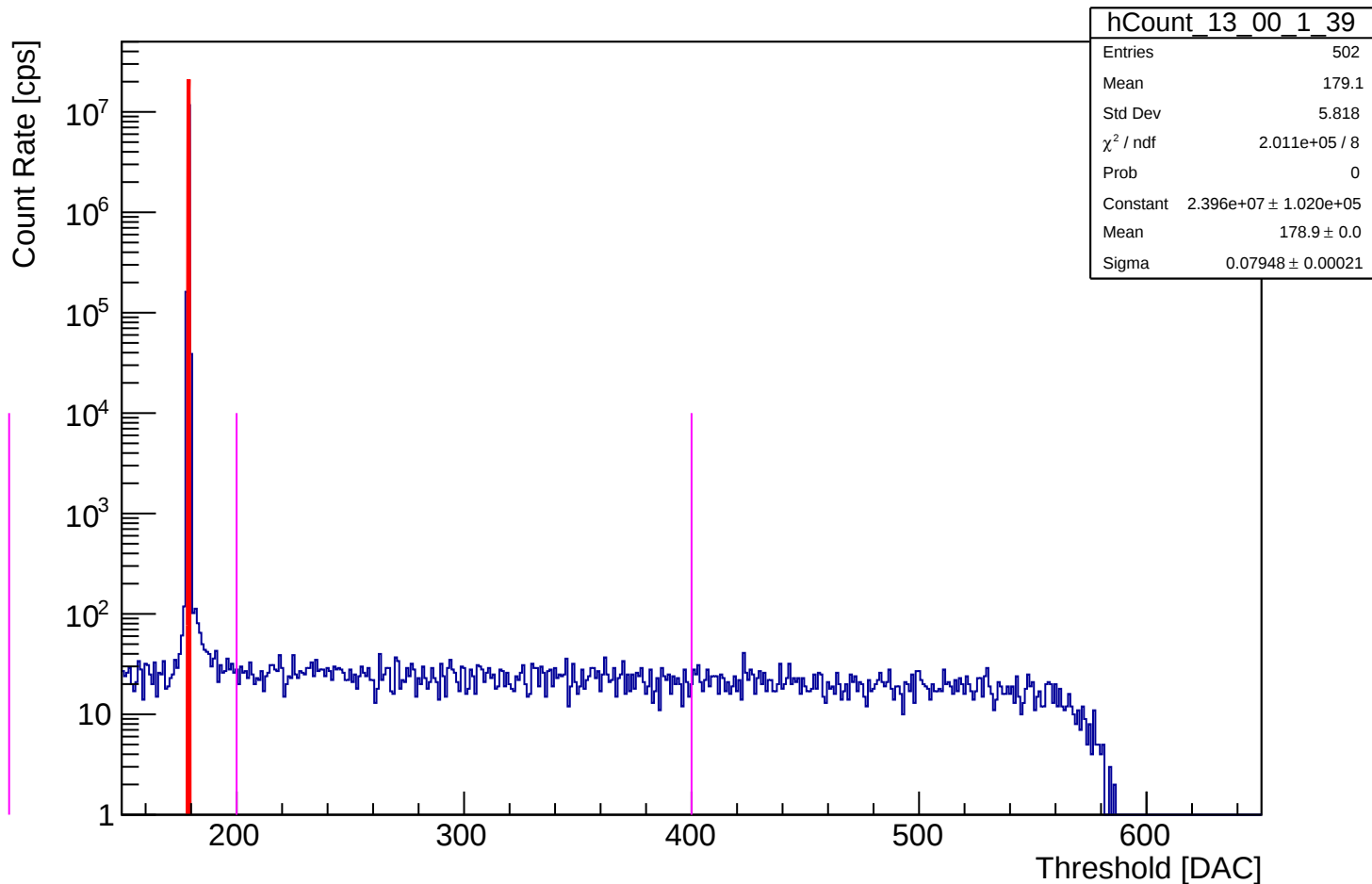
Row 1 Tile 1 Pmt 2 Pixel 14 Slot 13 Fiber 0 Asic 1 Channel 38



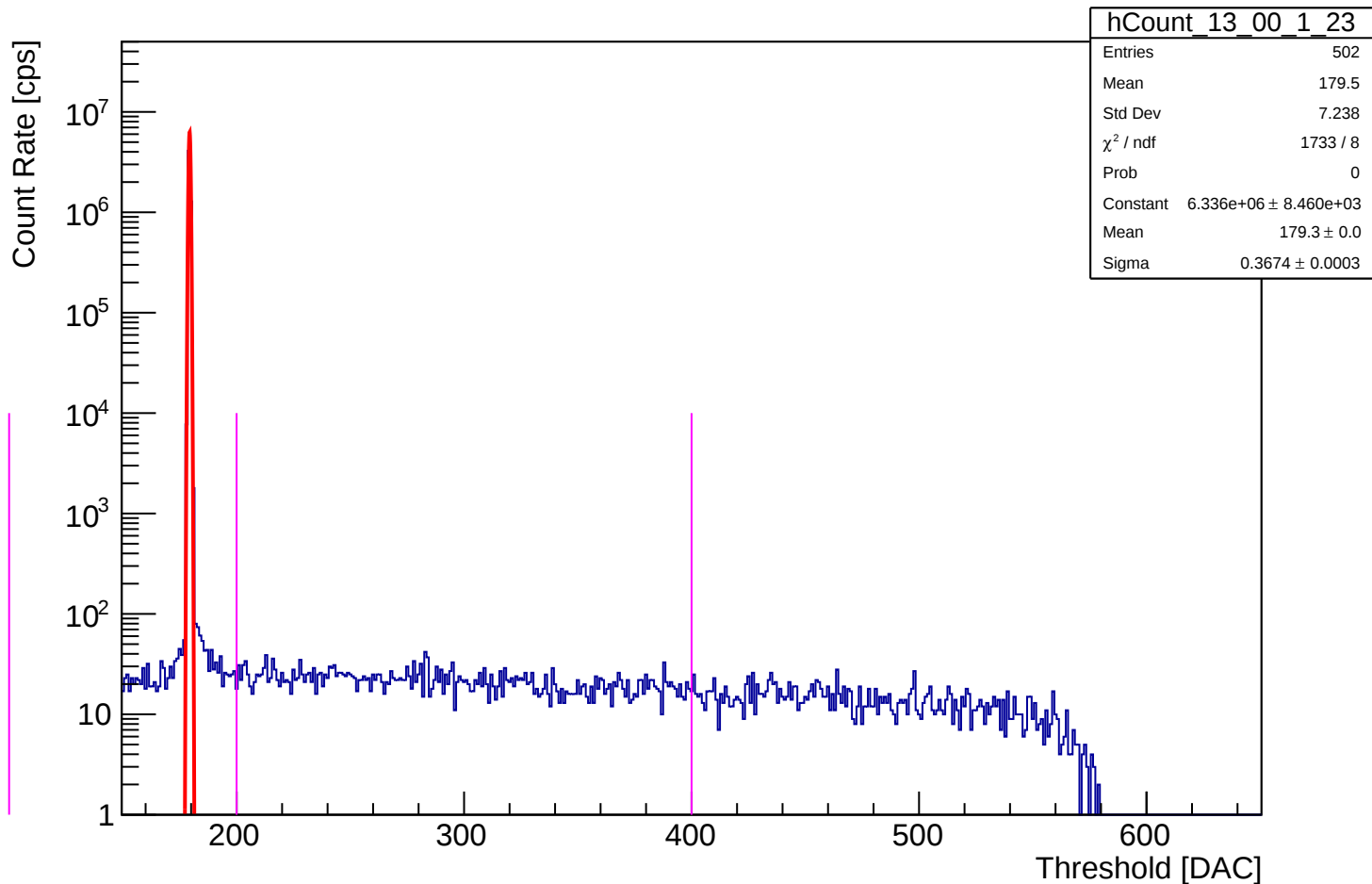
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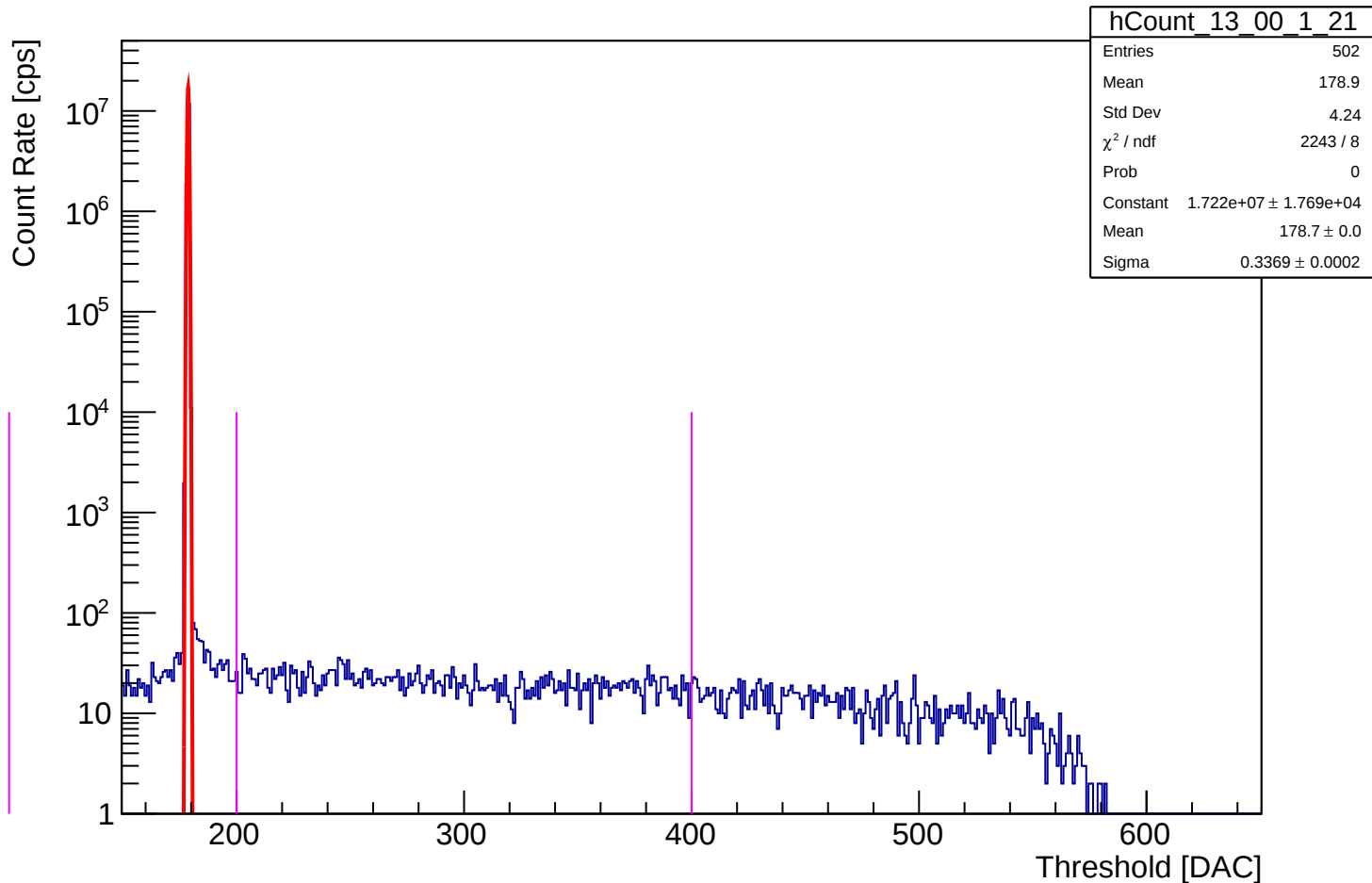
Row 1 Tile 1 Pmt 2 Pixel 16 Slot 13 Fiber 0 Asic 1 Channel 39



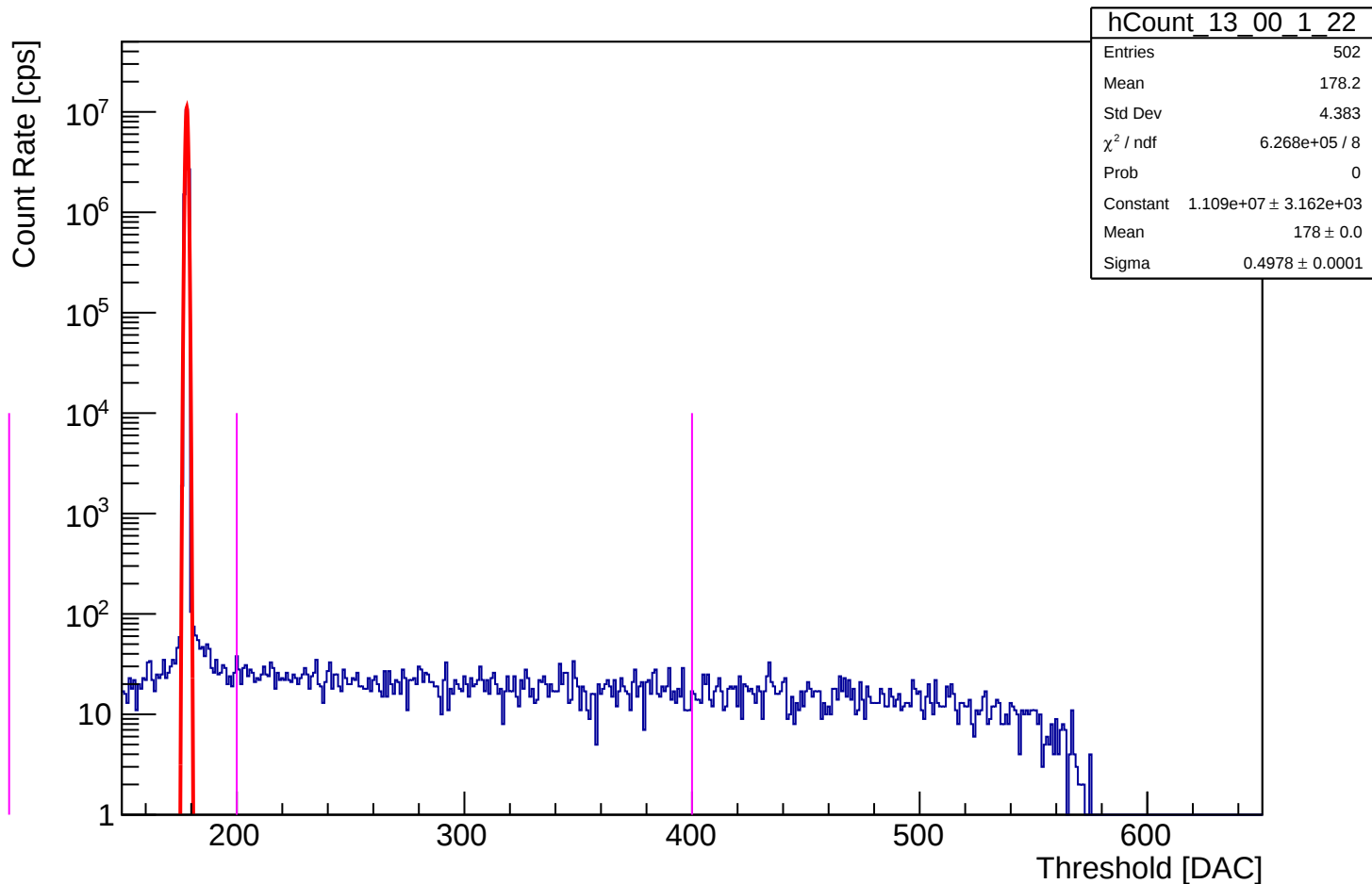
Row 1 Tile 1 Pmt 2 Pixel 17 Slot 13 Fiber 0 Asic 1 Channel 23



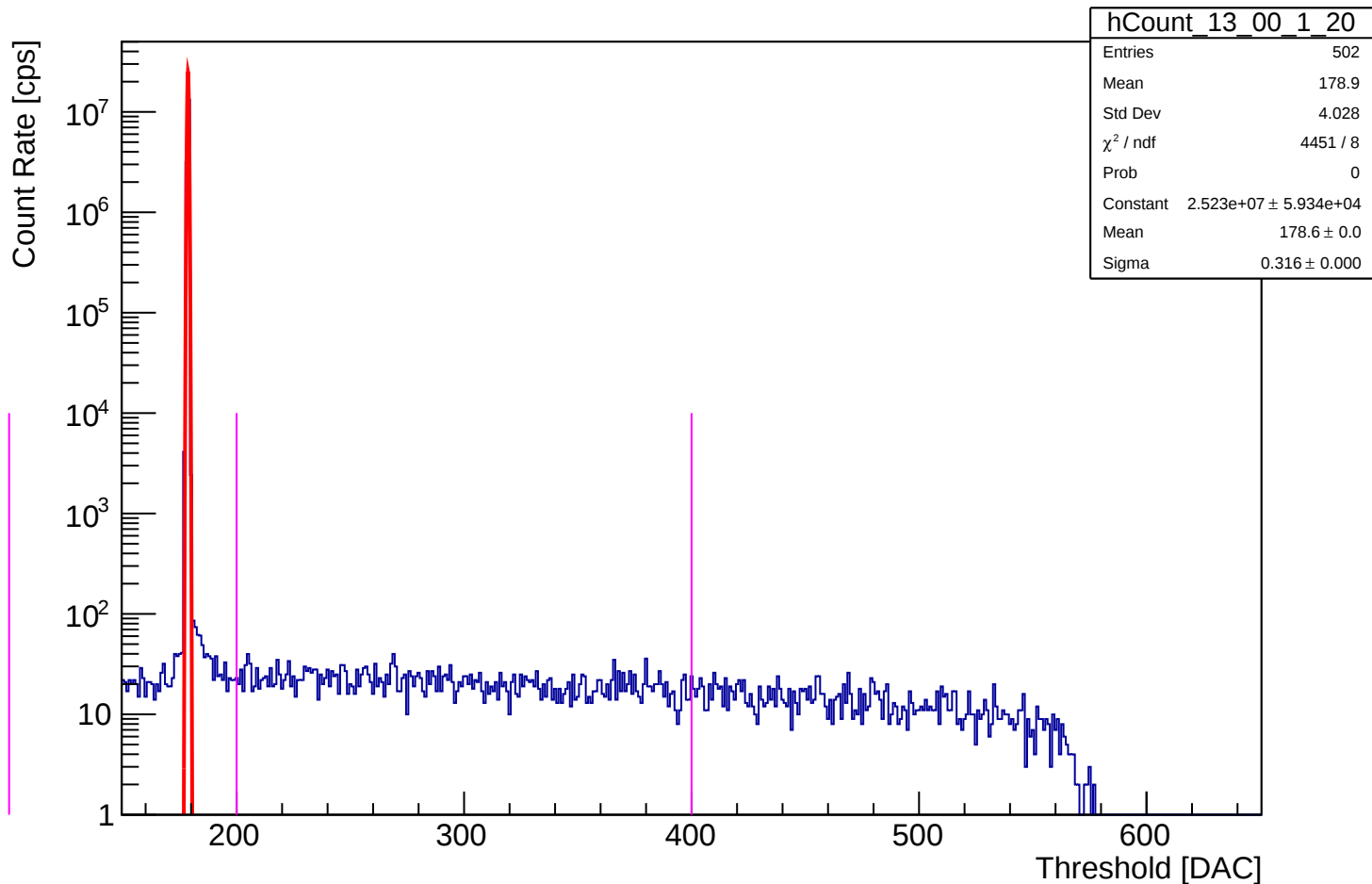
Row 1 Tile 1 Pmt 2 Pixel 18 Slot 13 Fiber 0 Asic 1 Channel 21



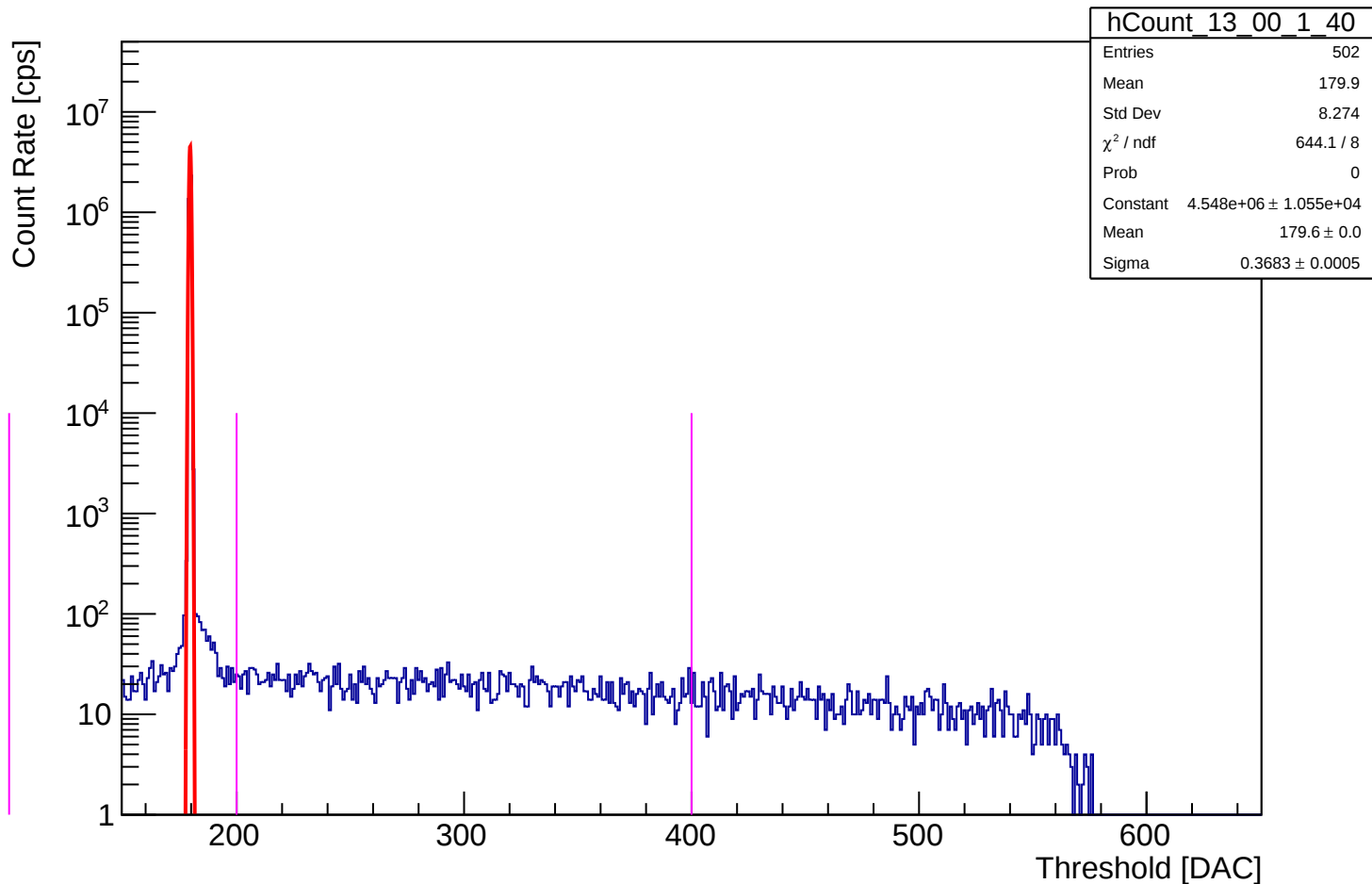
Row 1 Tile 1 Pmt 2 Pixel 19 Slot 13 Fiber 0 Asic 1 Channel 22



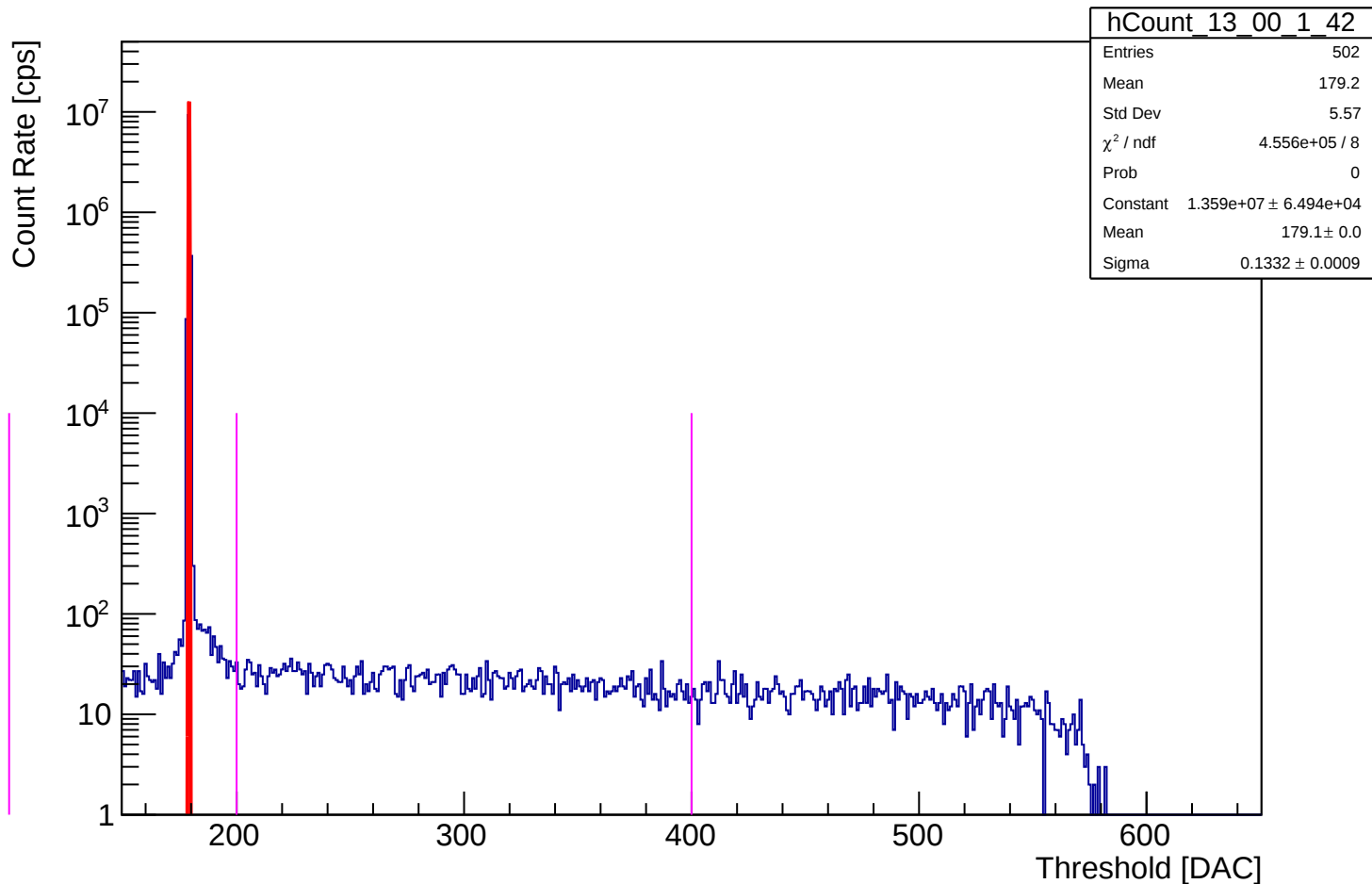
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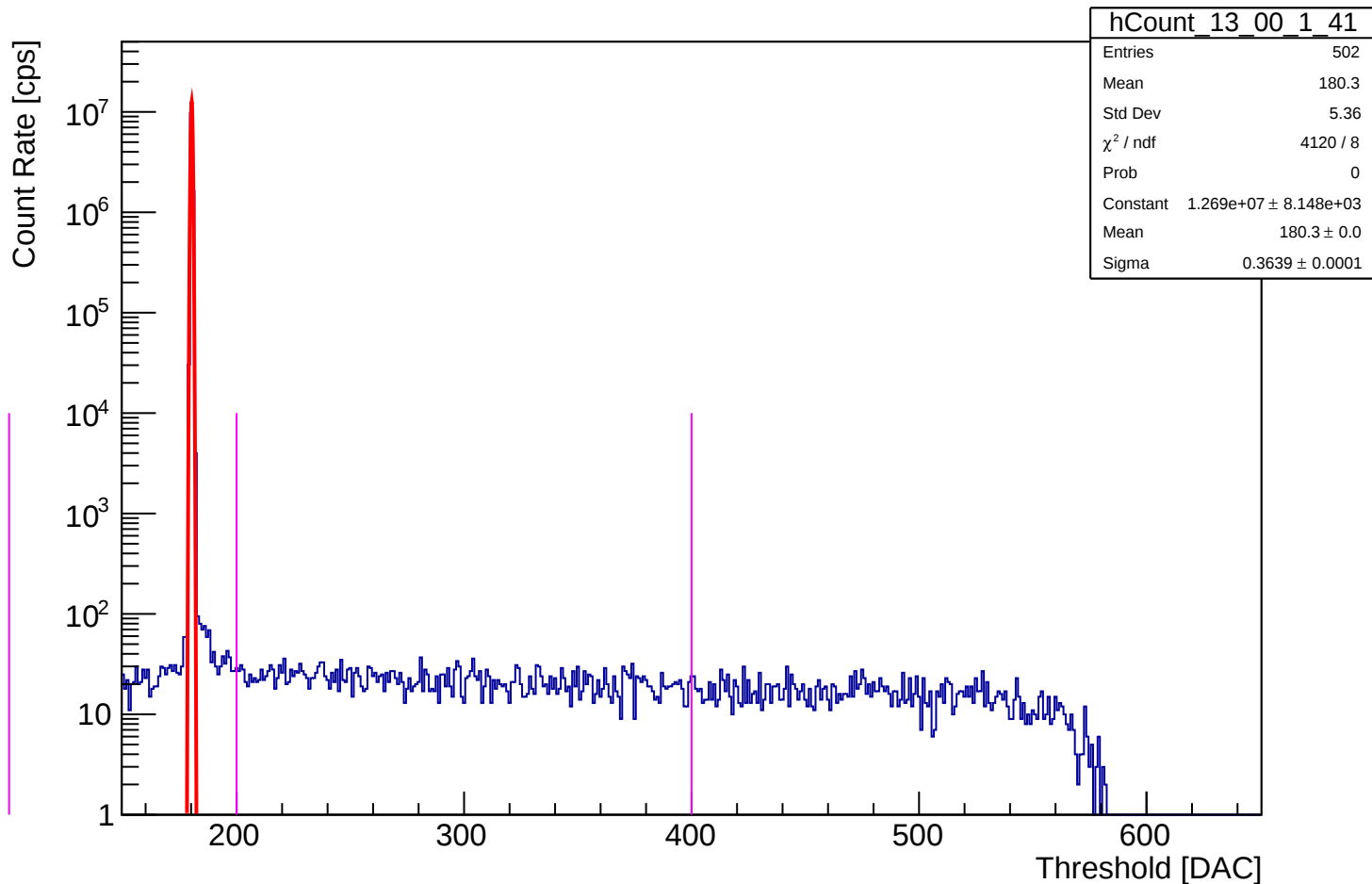
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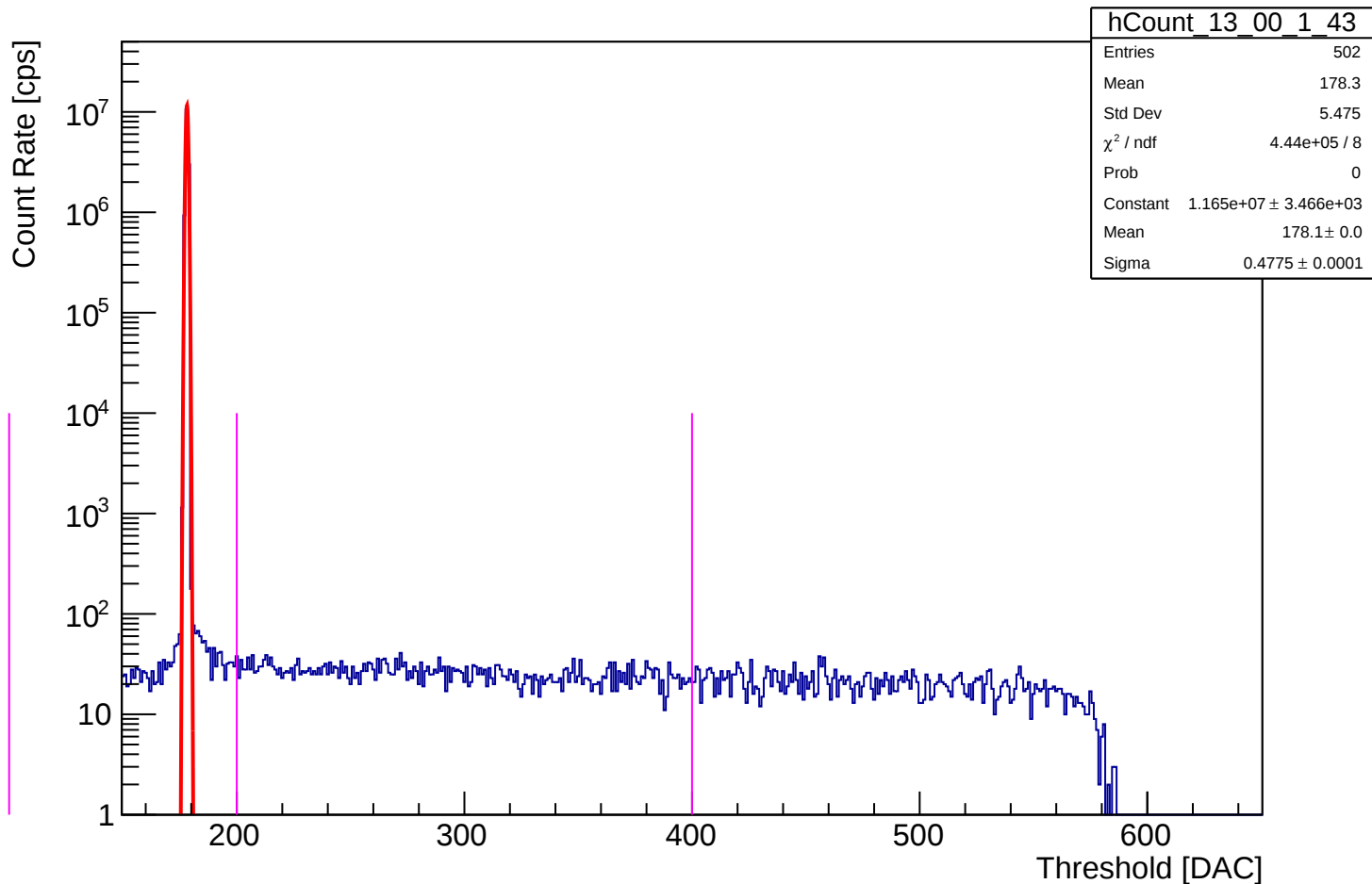
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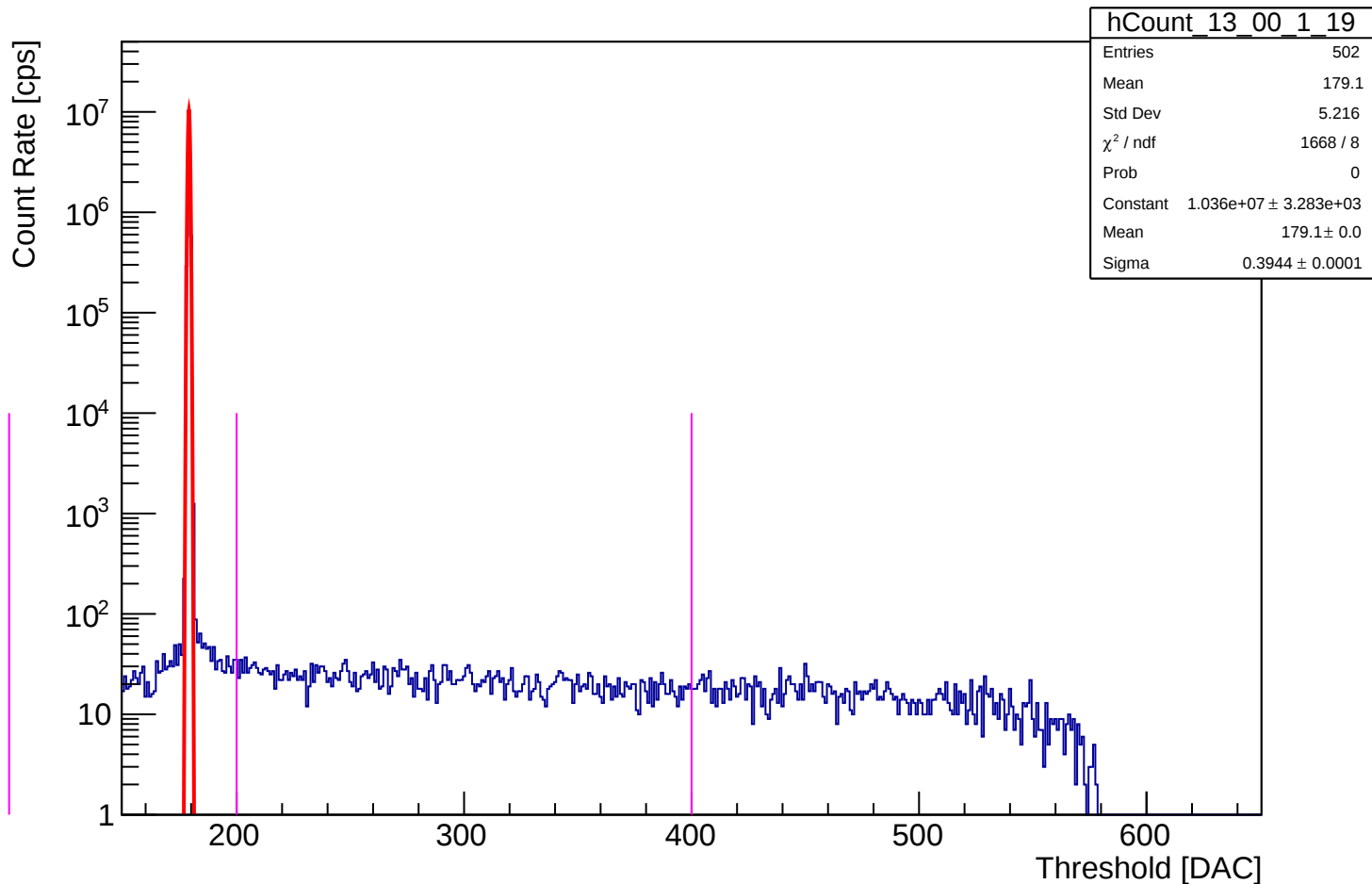
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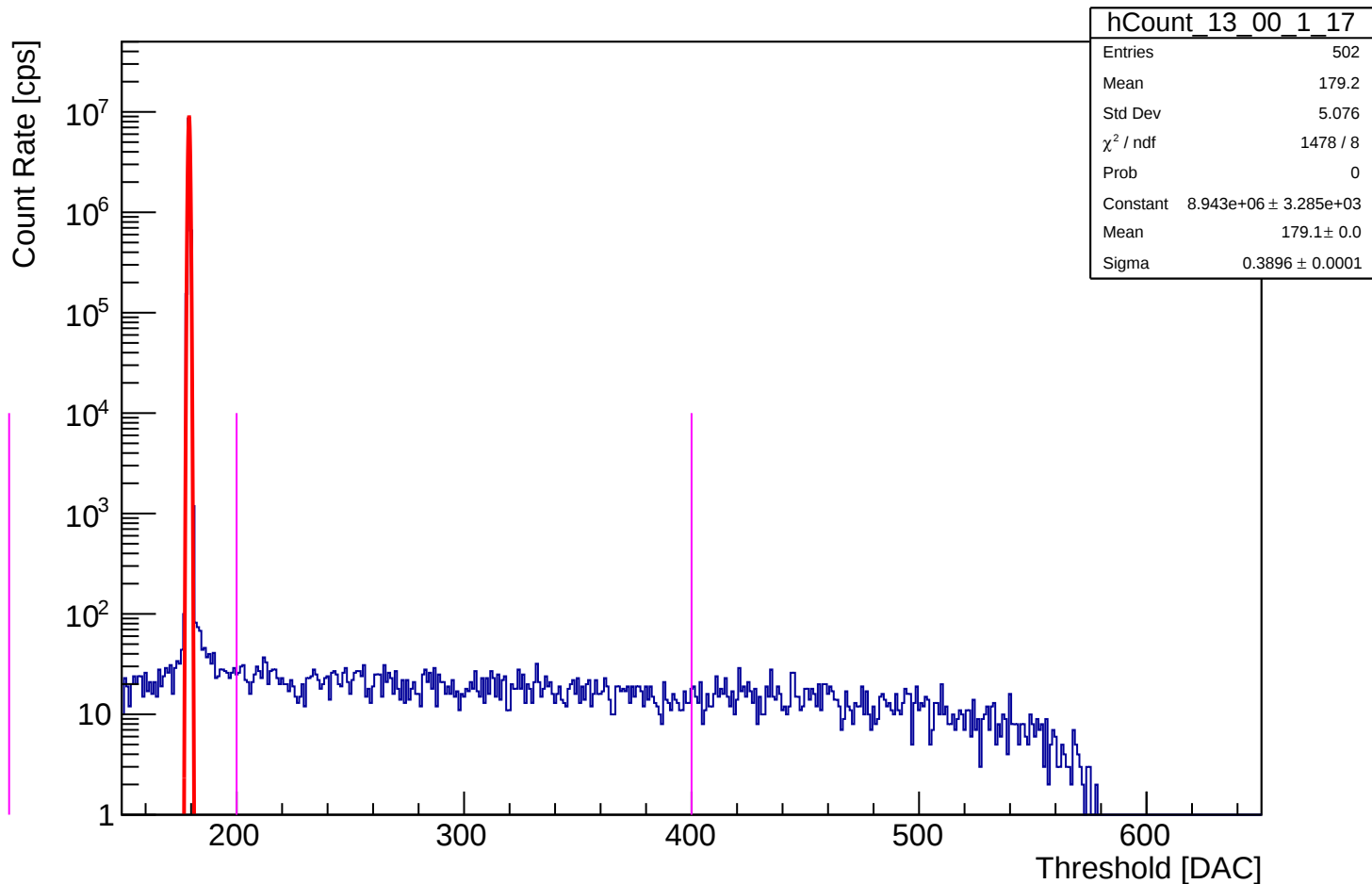
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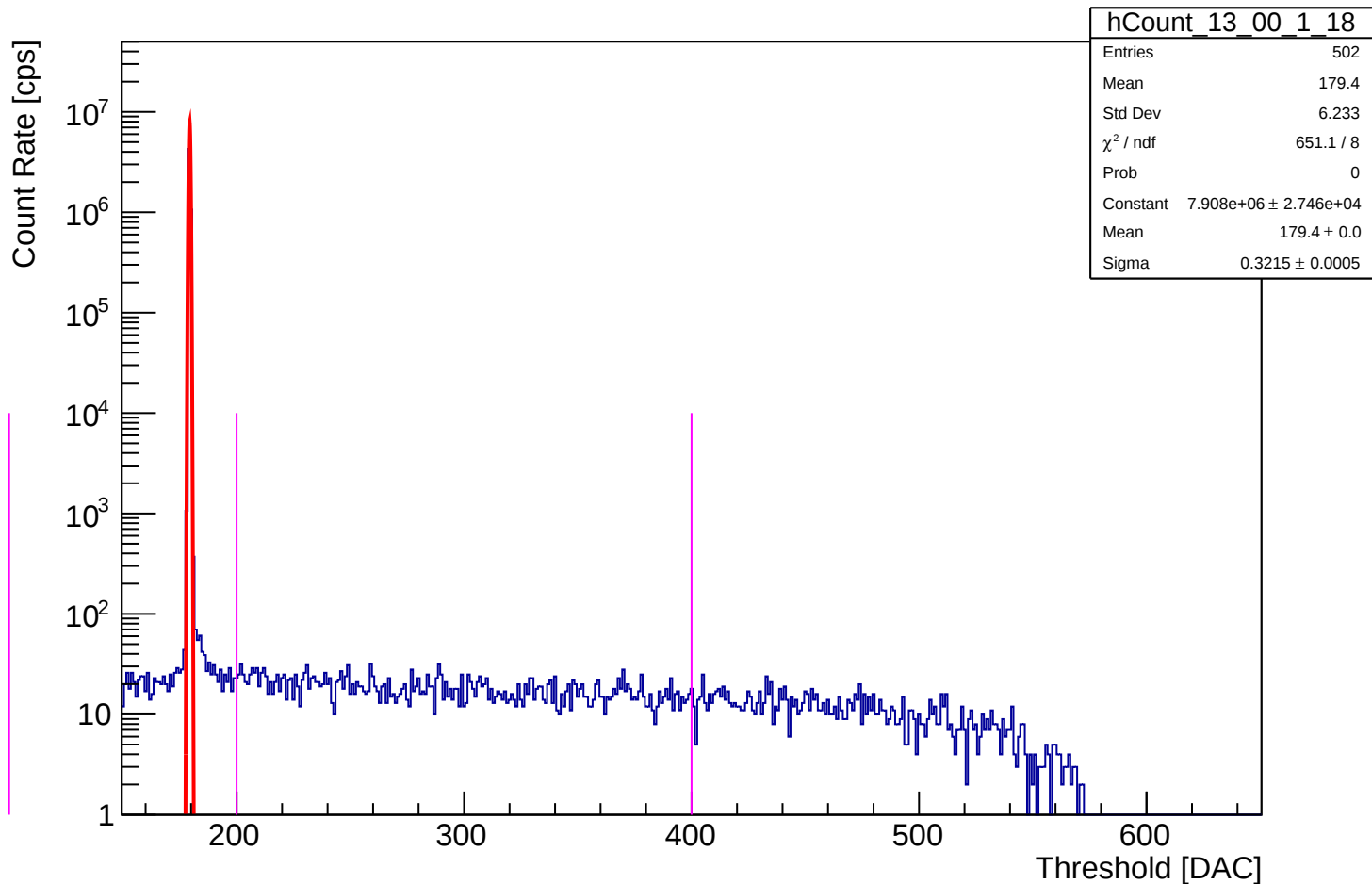
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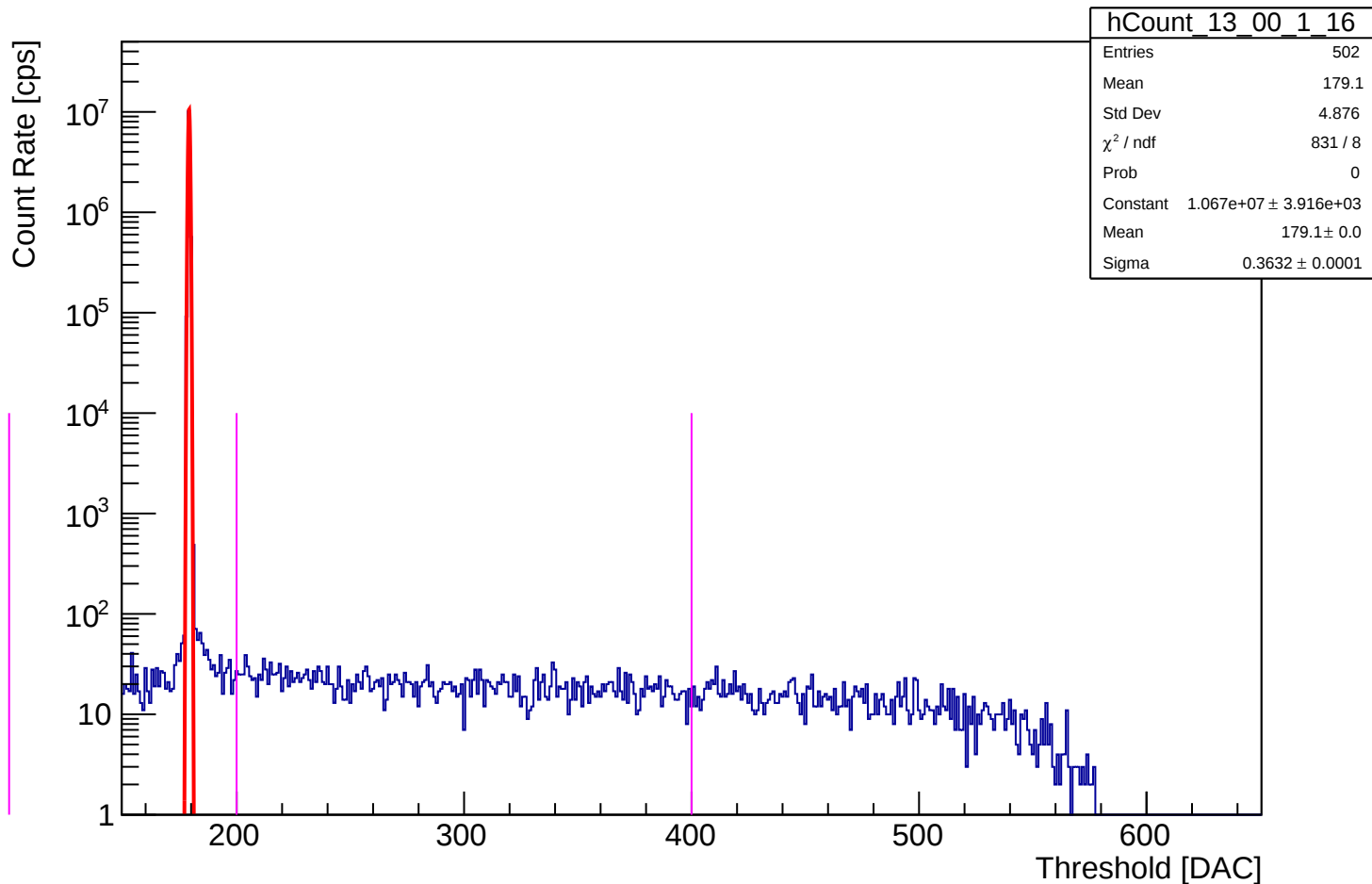
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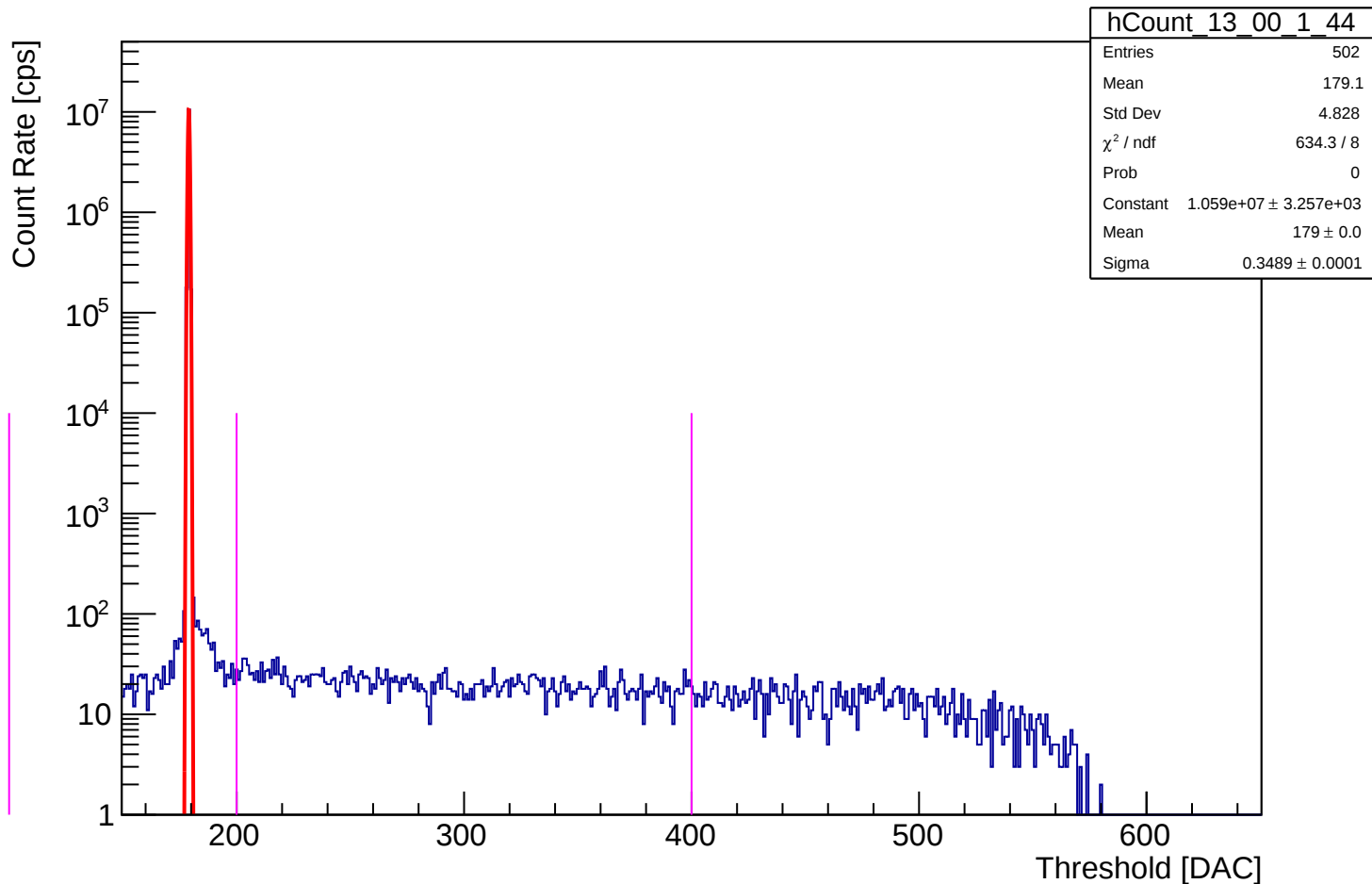
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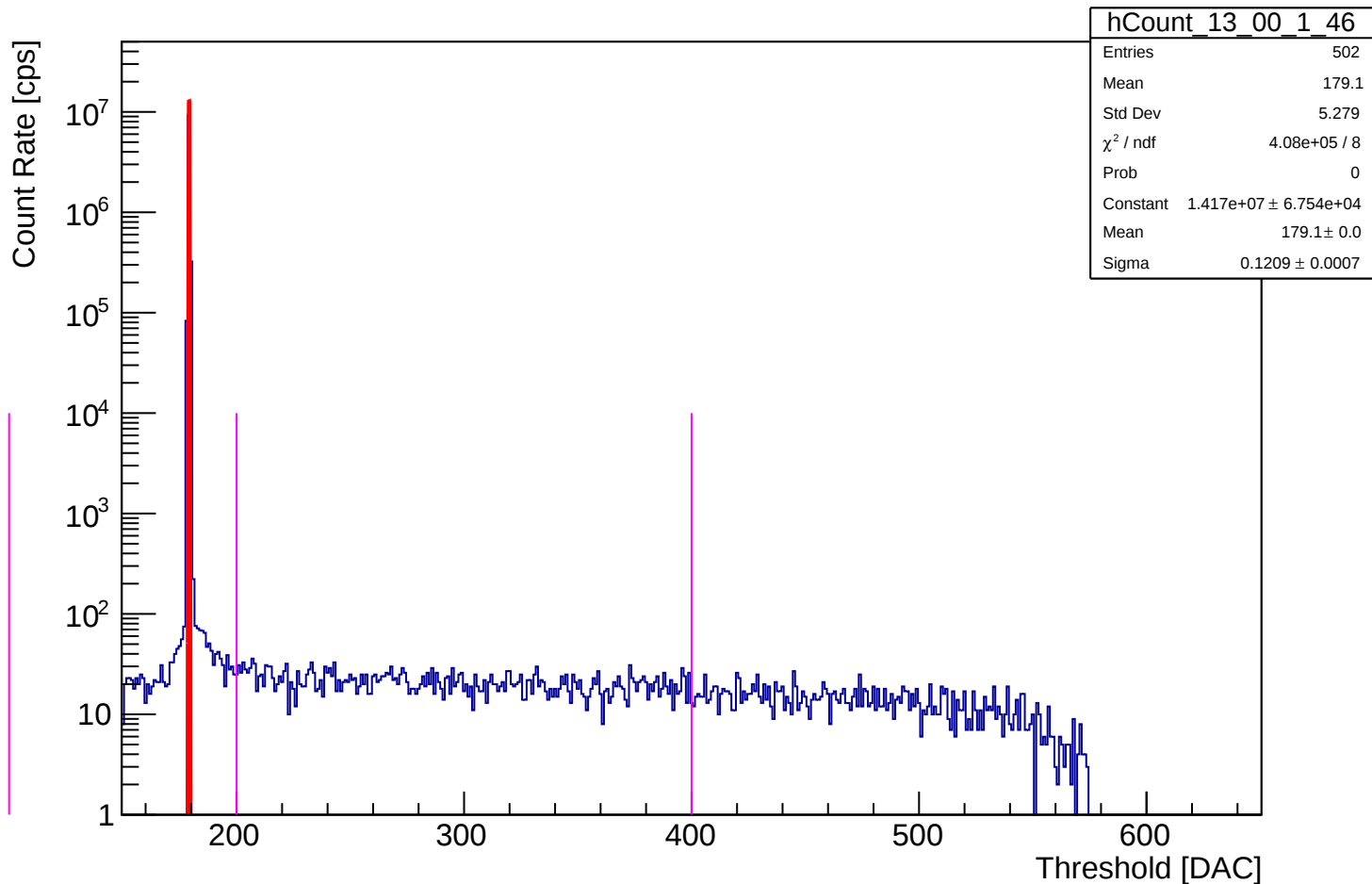
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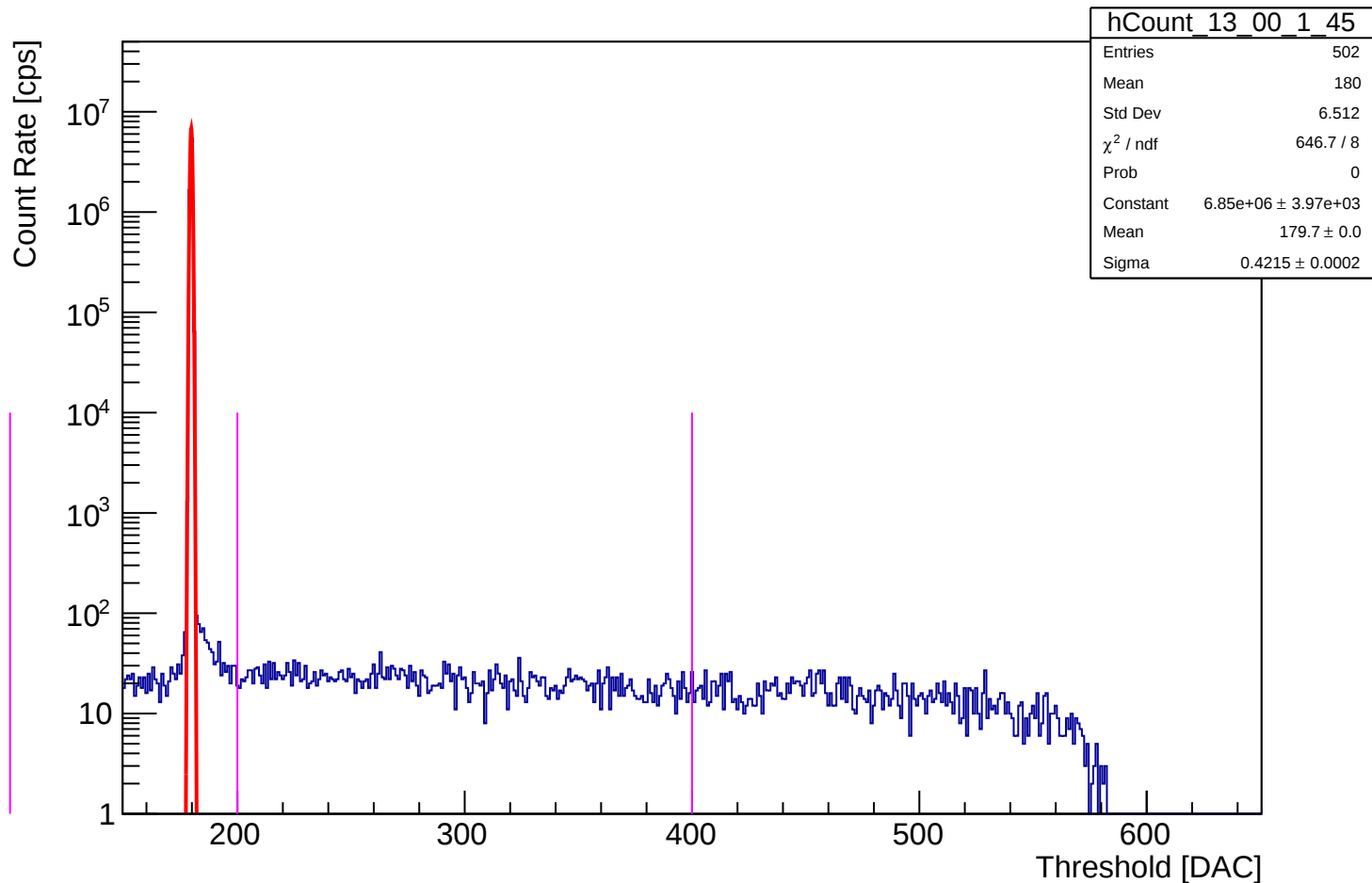
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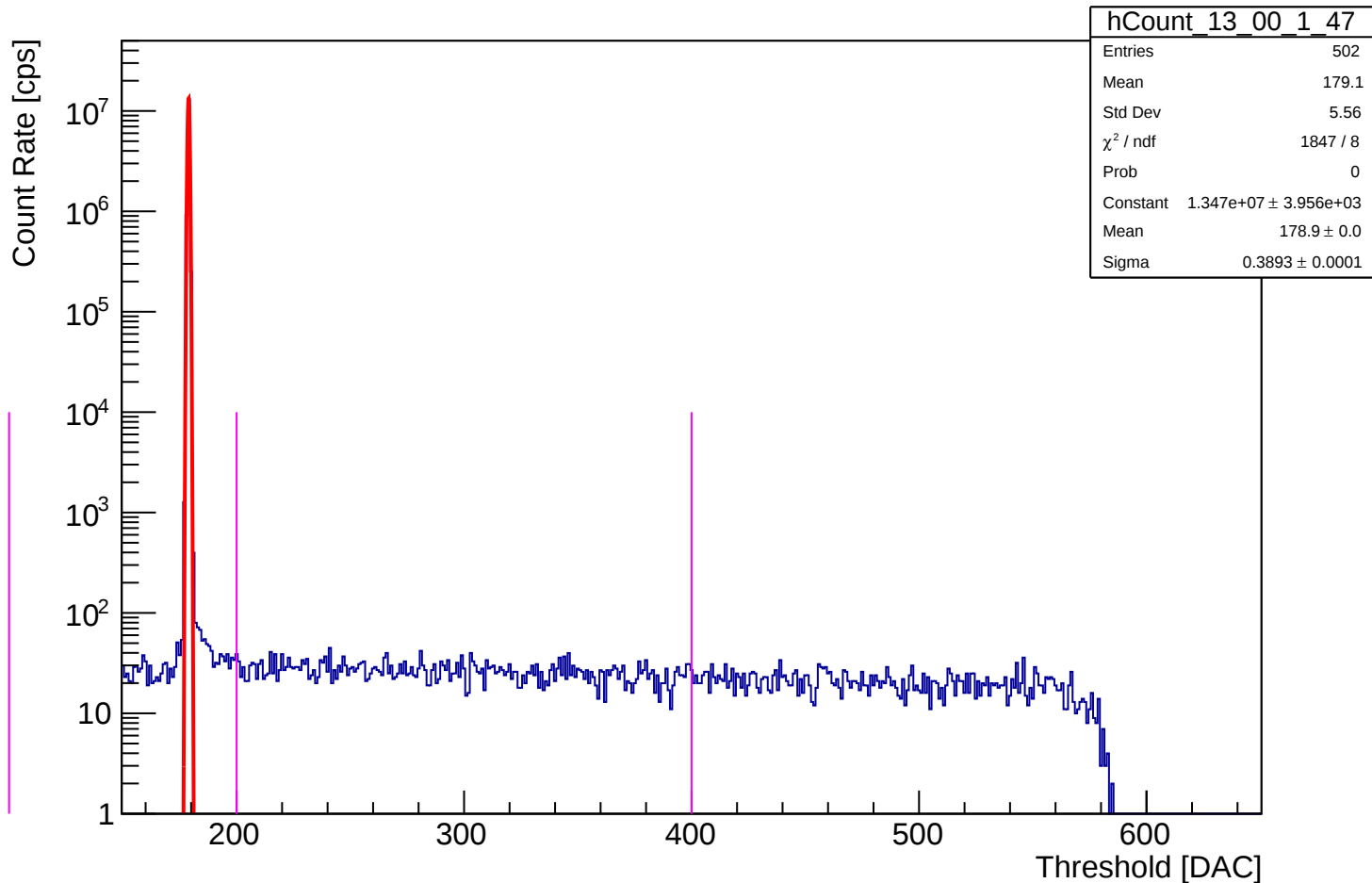
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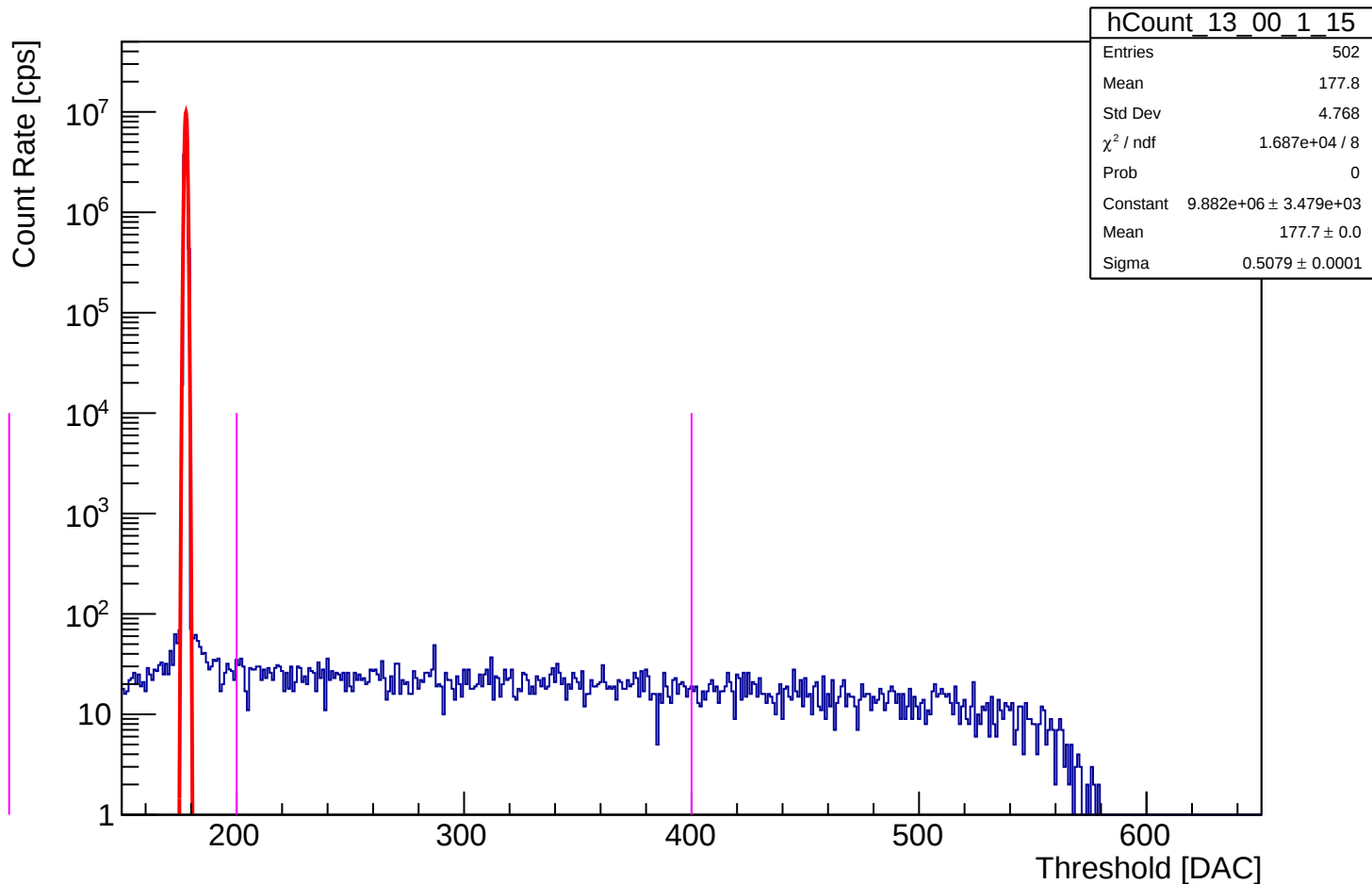
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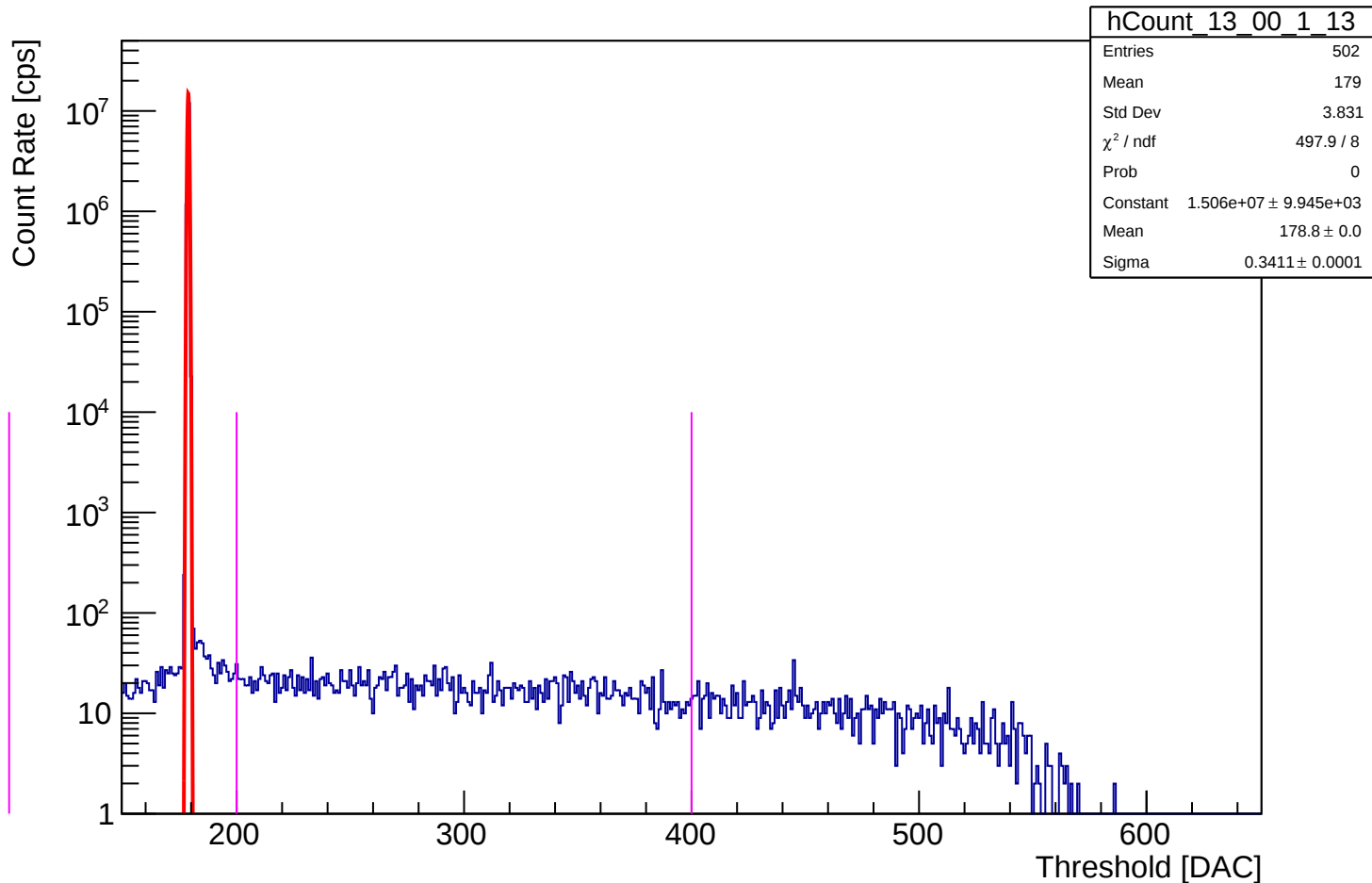
Row 1 Tile 1 Pmt 2 Pixel 32 Slot 13 Fiber 0 Asic 1 Channel 47



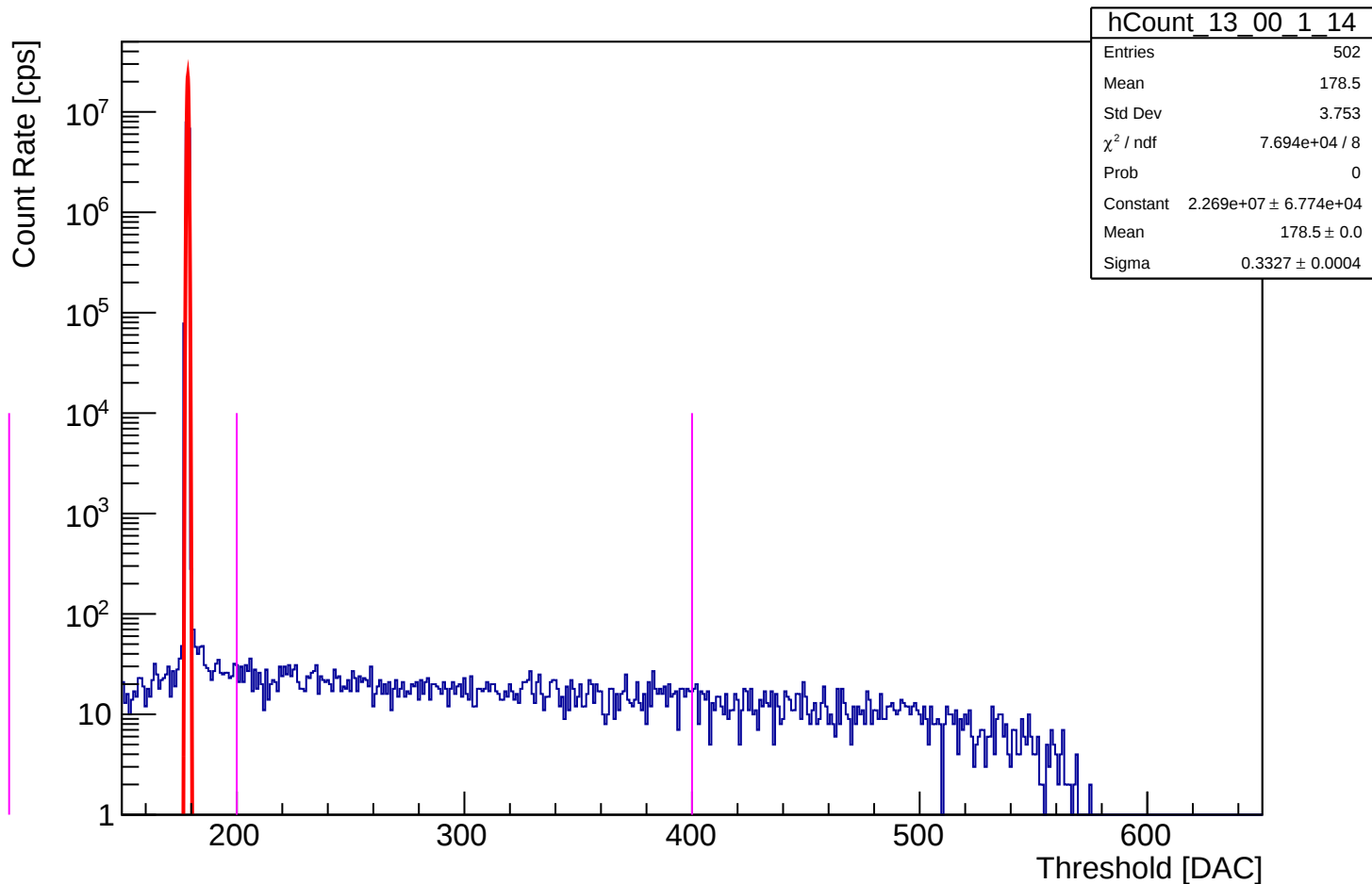
Row 1 Tile 1 Pmt 2 Pixel 33 Slot 13 Fiber 0 Asic 1 Channel 15



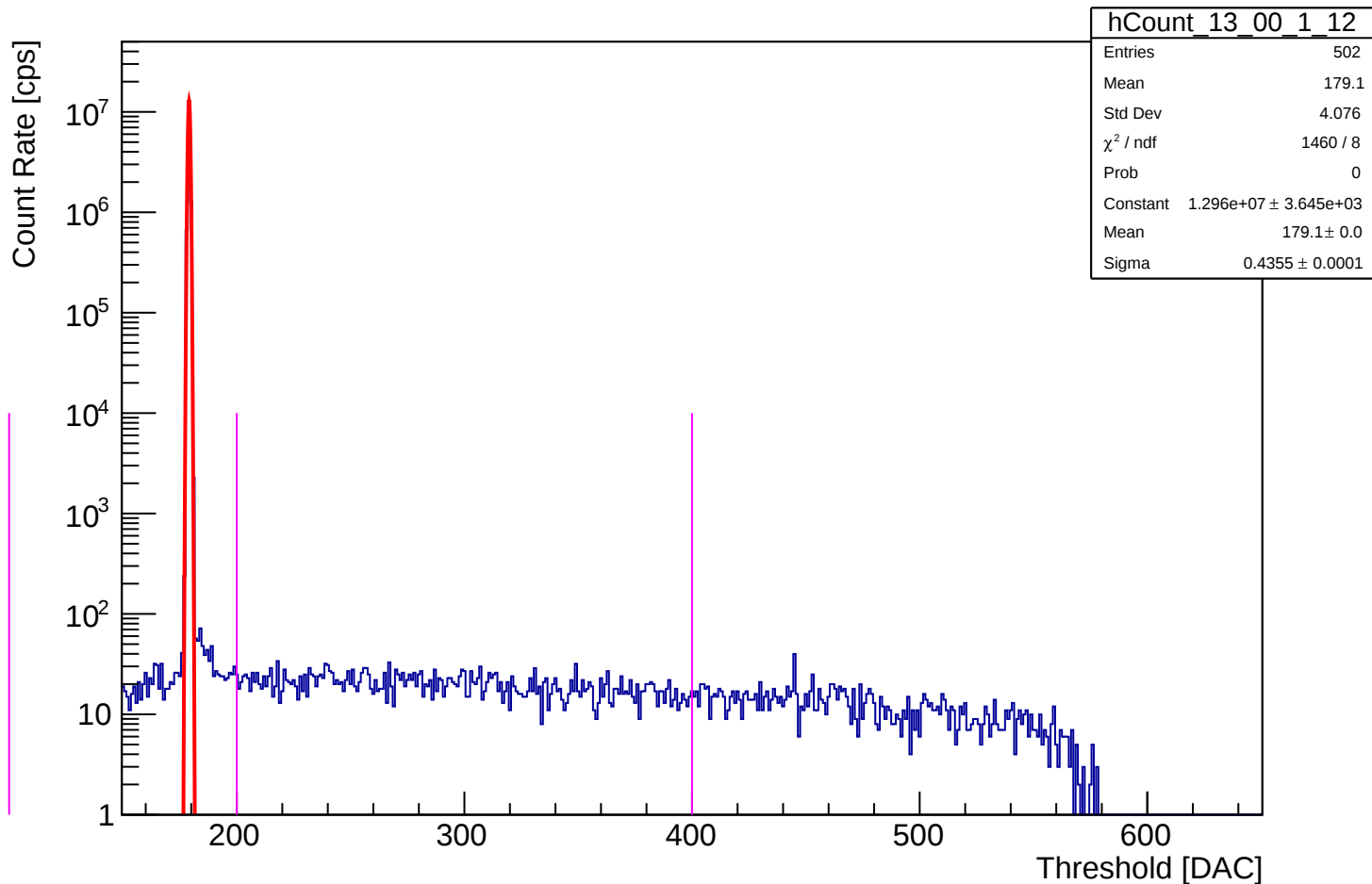
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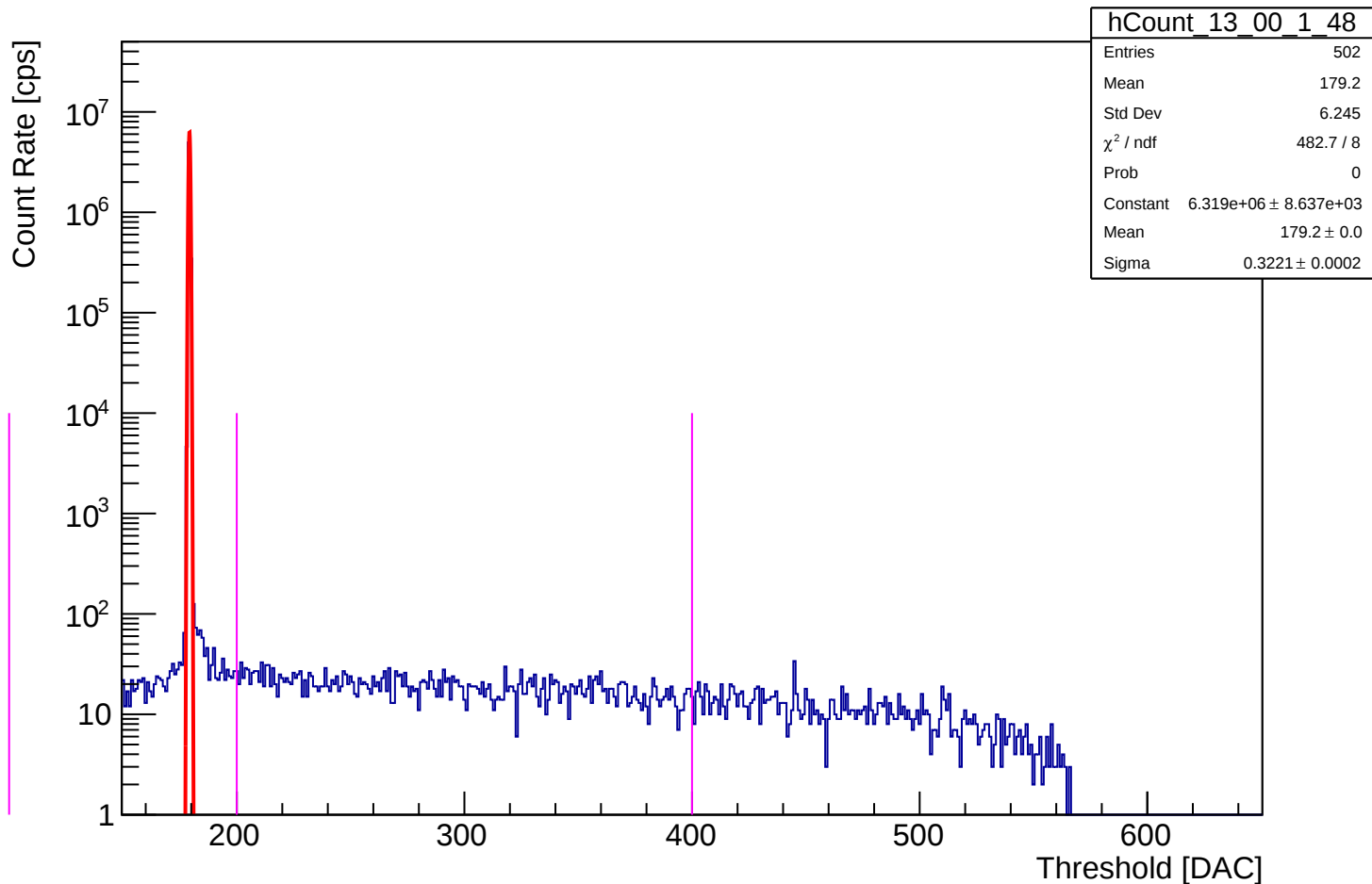
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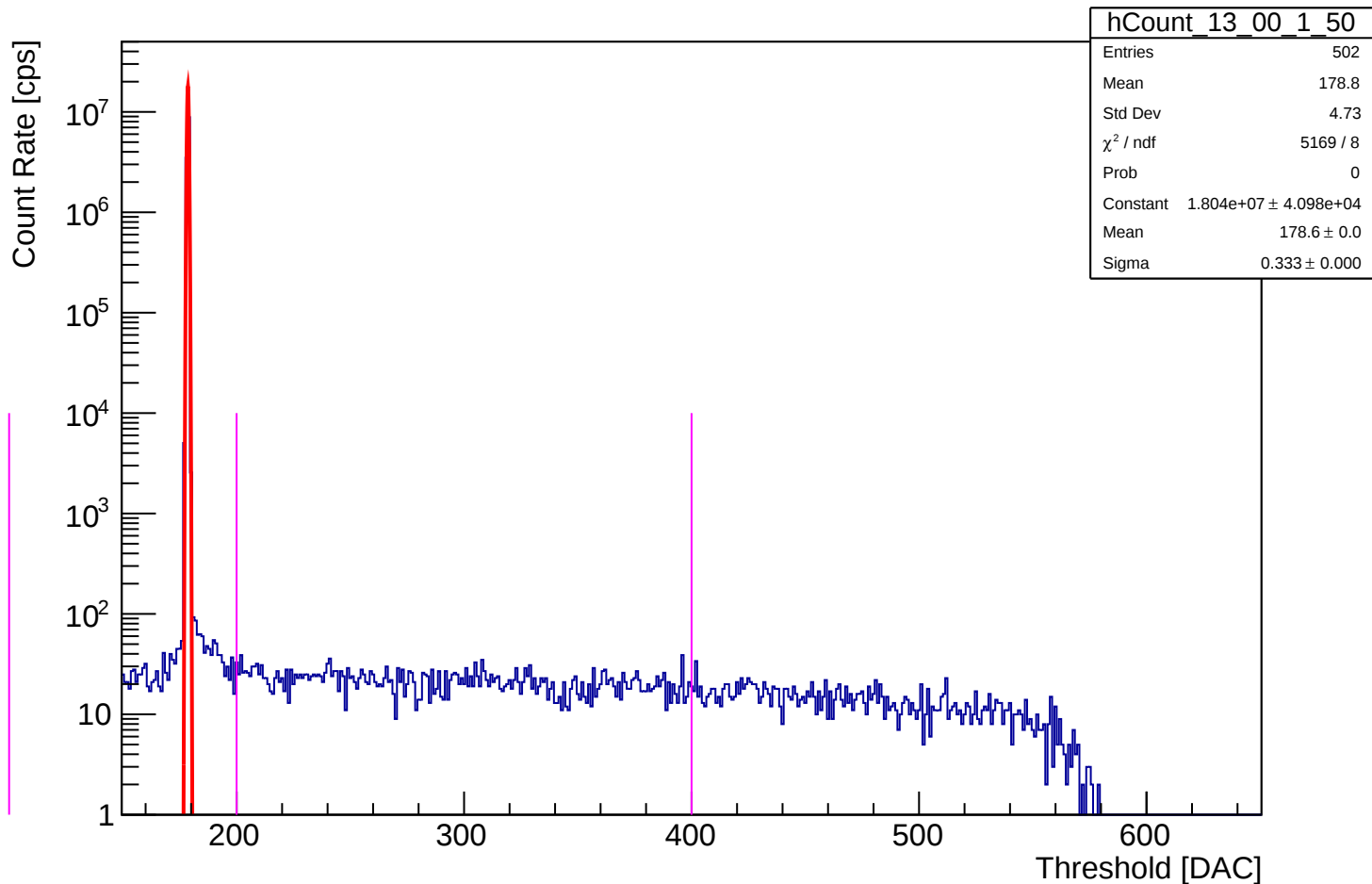
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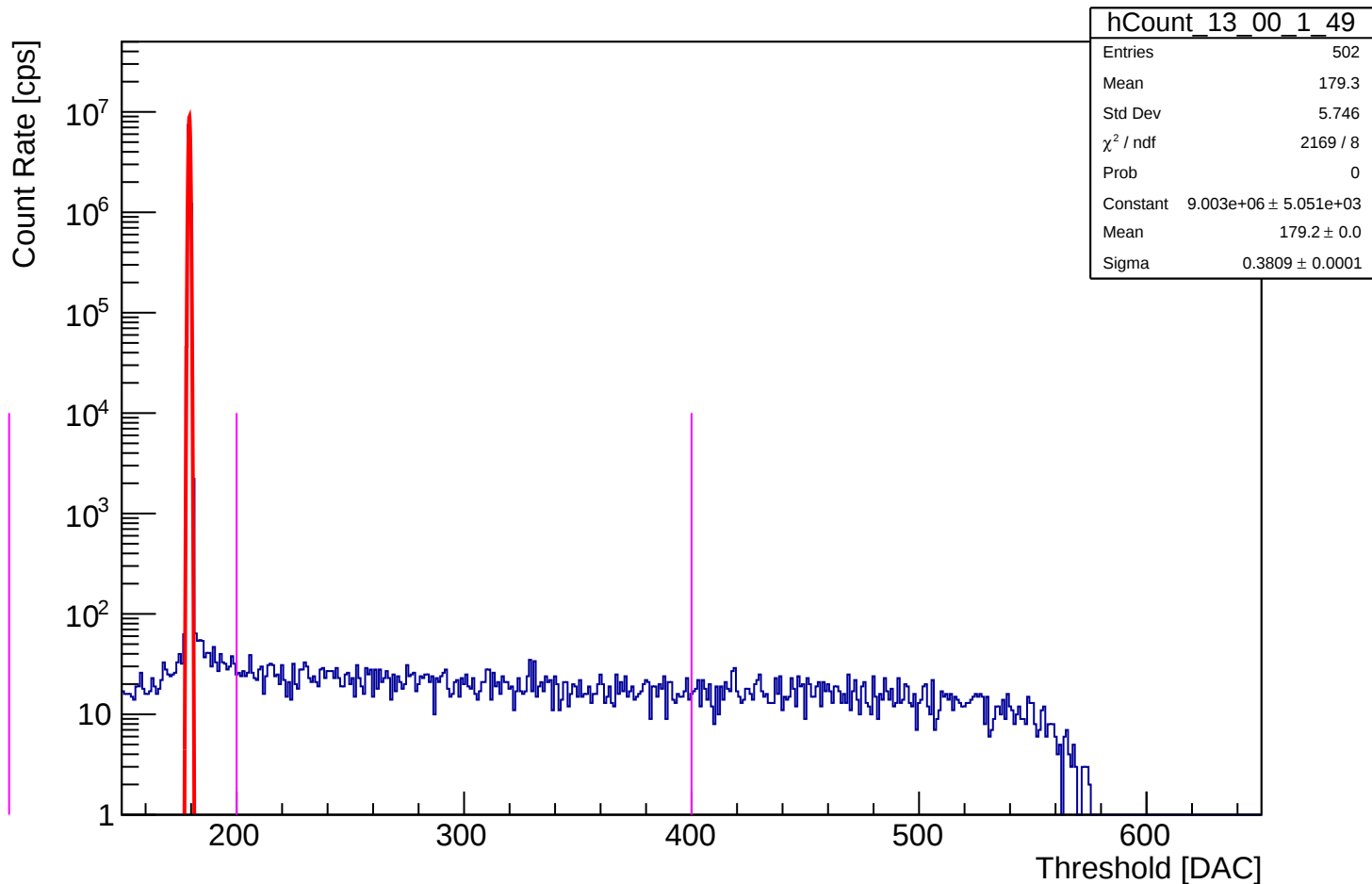
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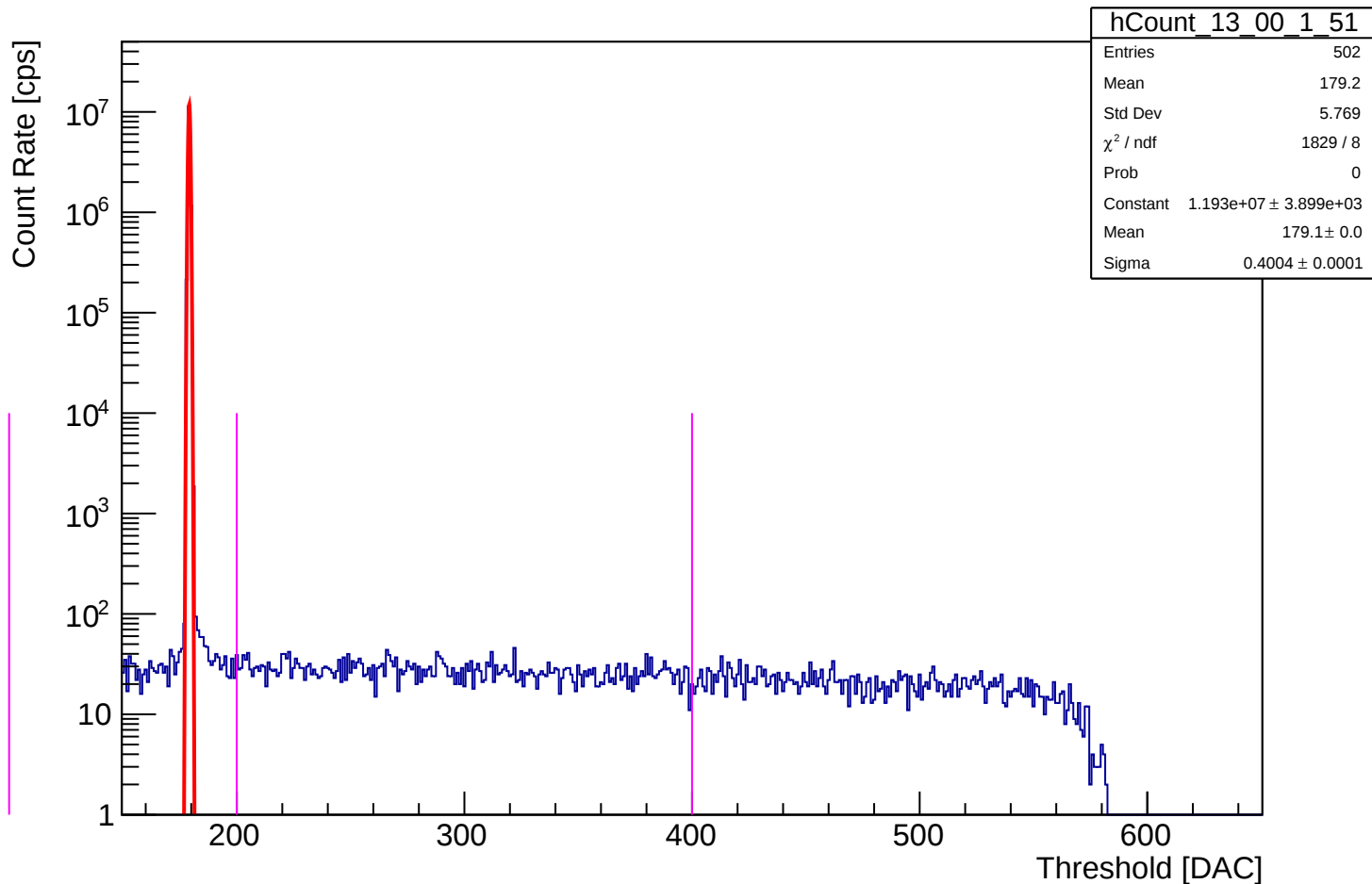
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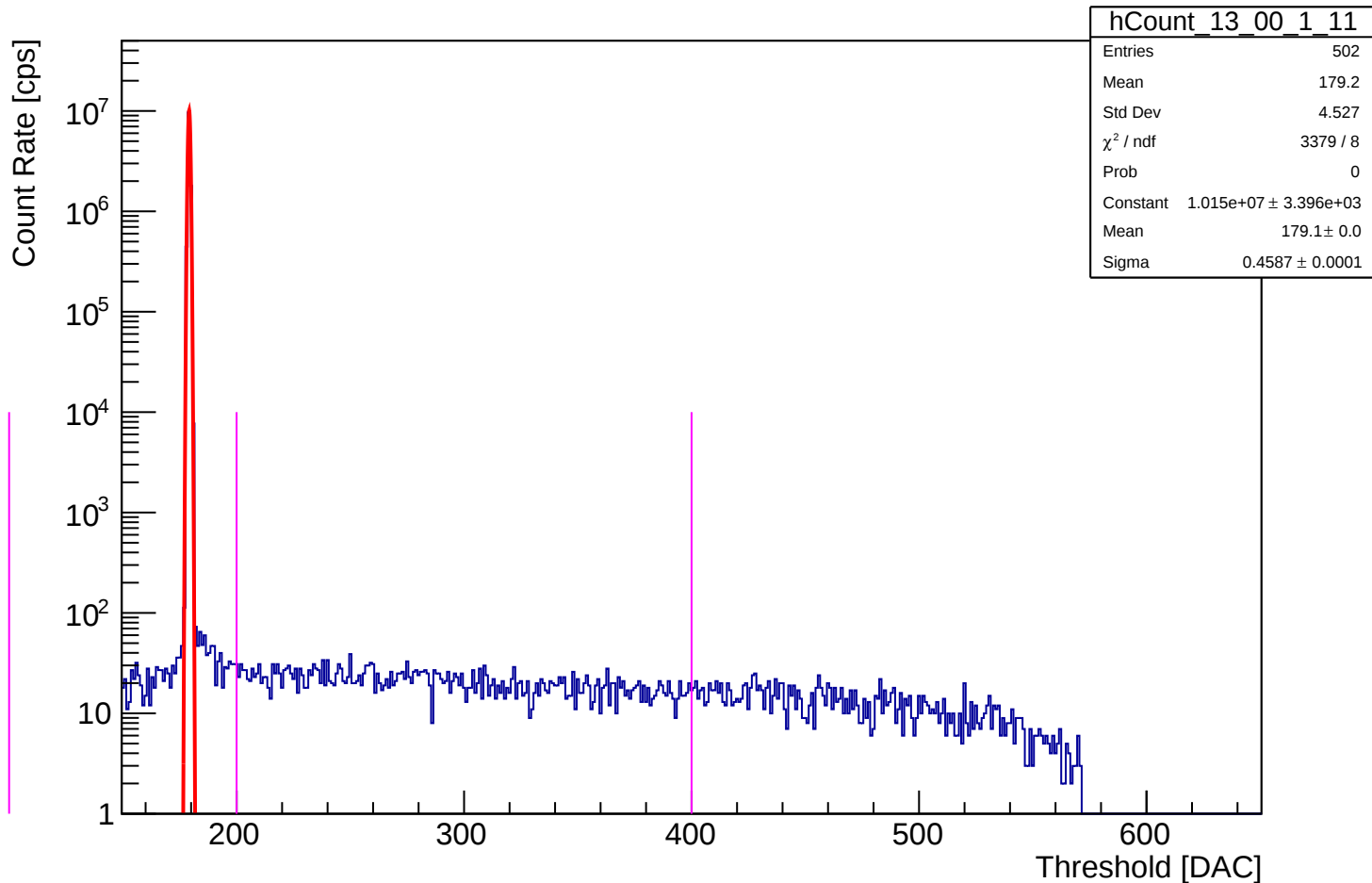
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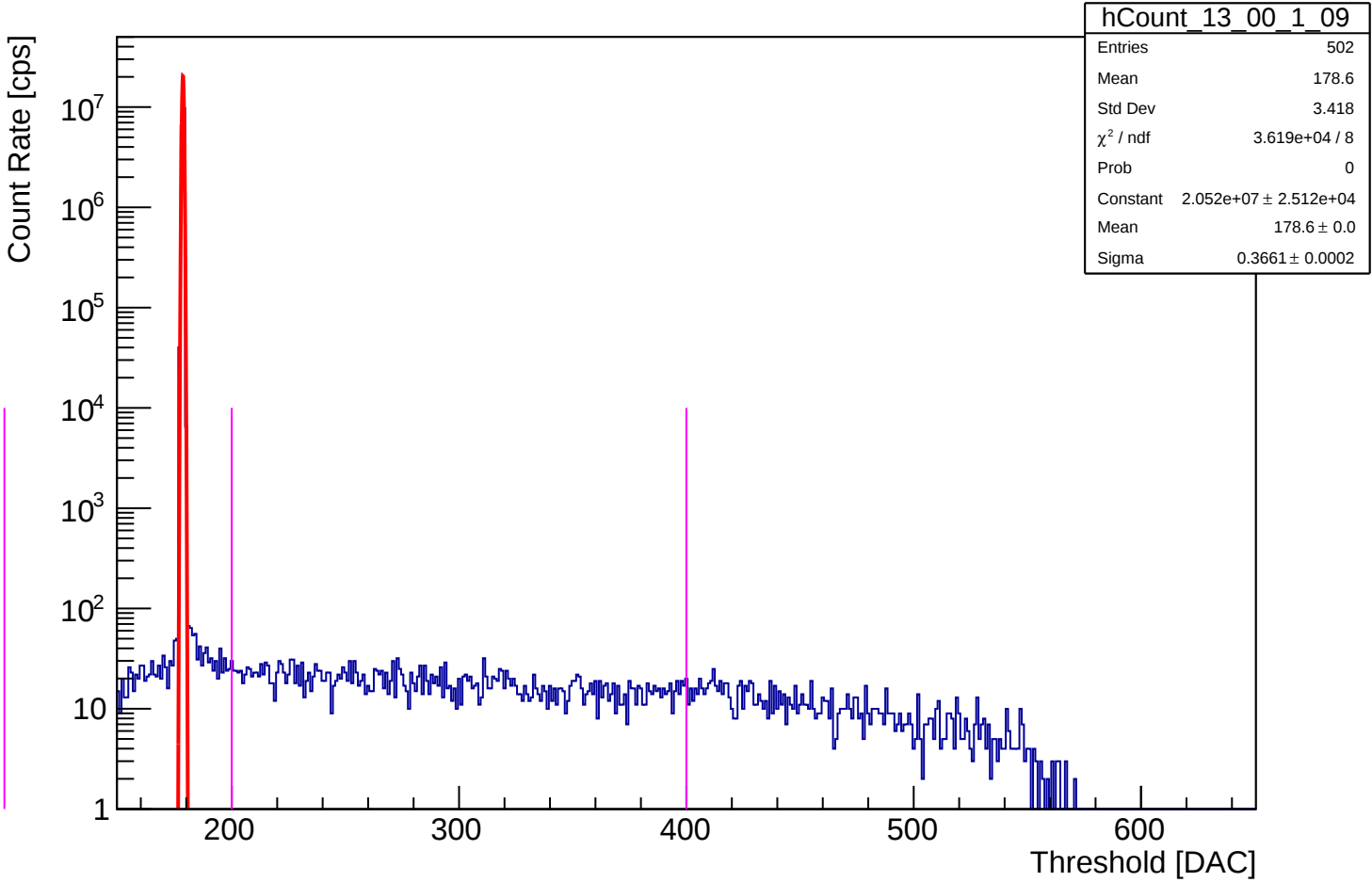


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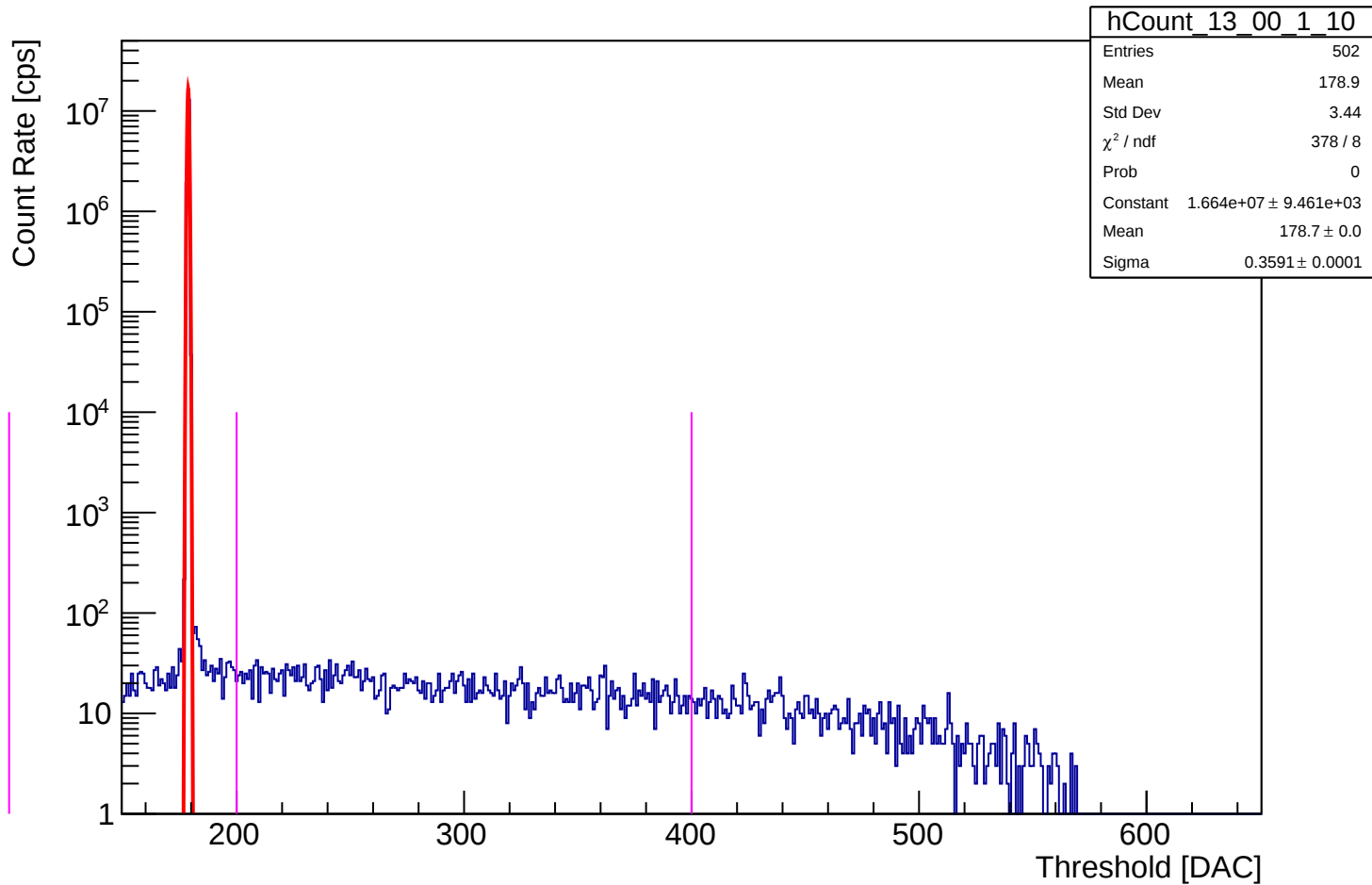


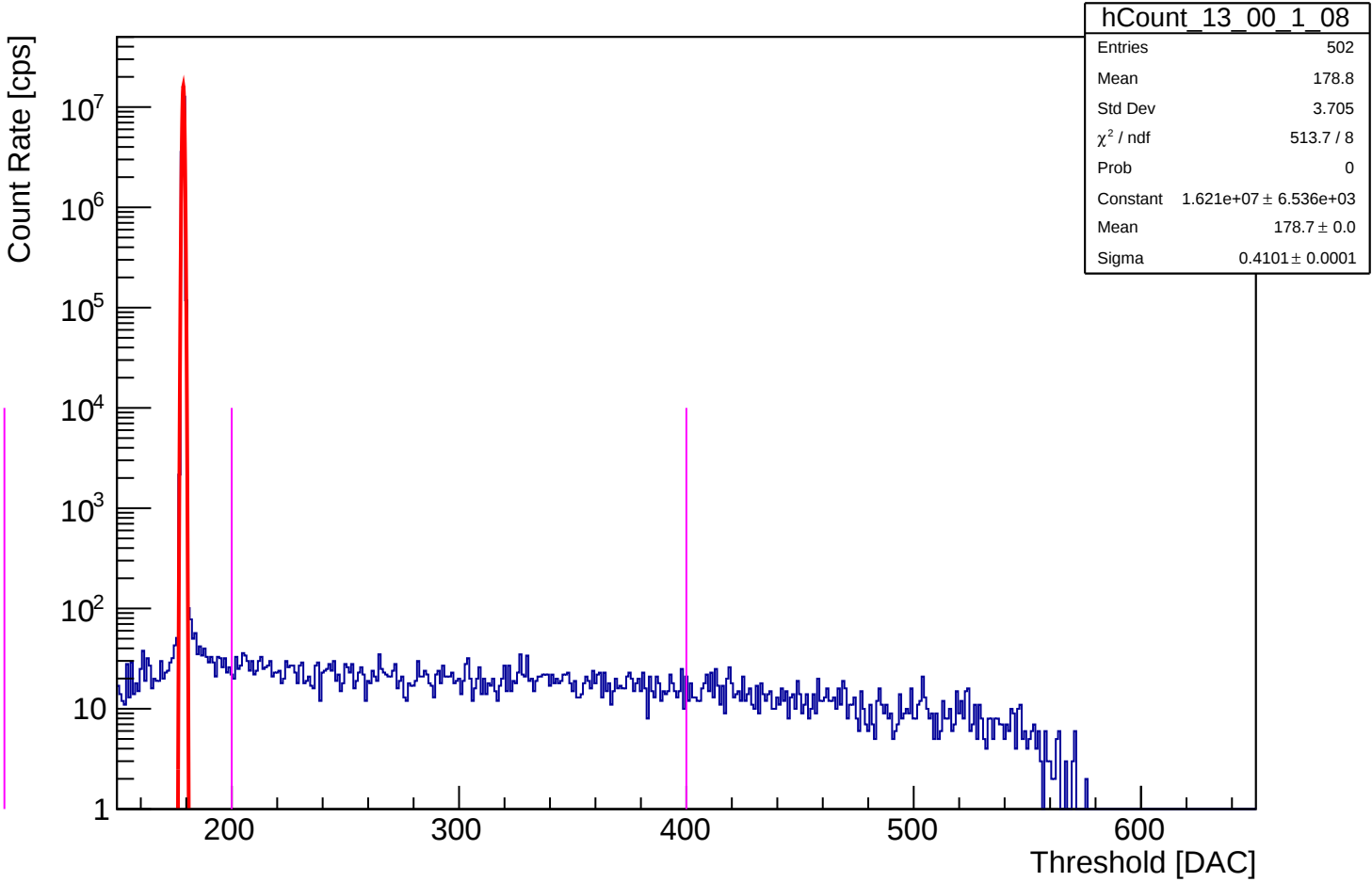
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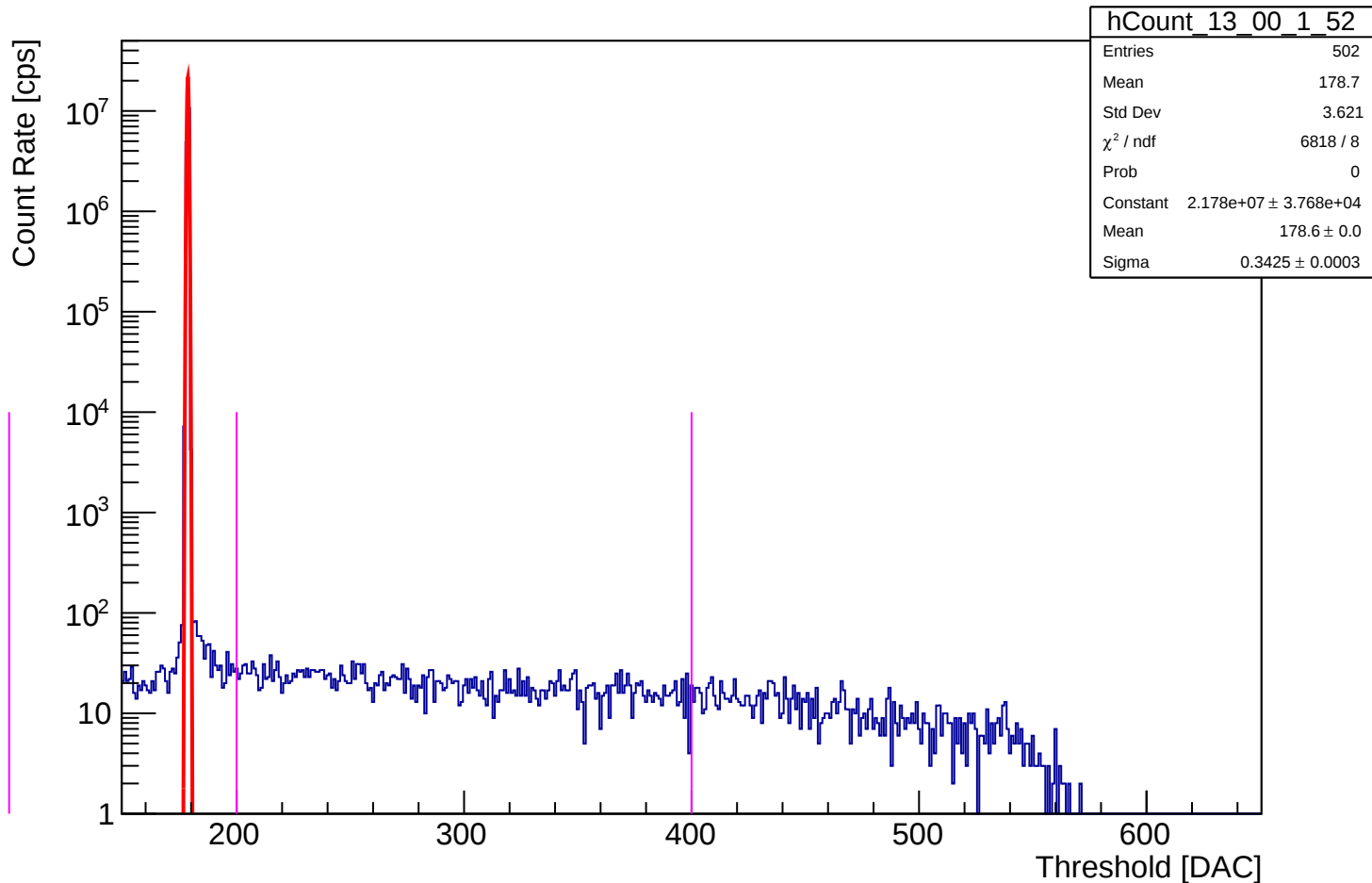


Row 1 Tile 1 Pmt 2 Pixel 43 Slot 13 Fiber 0 Asic 1 Channel 10

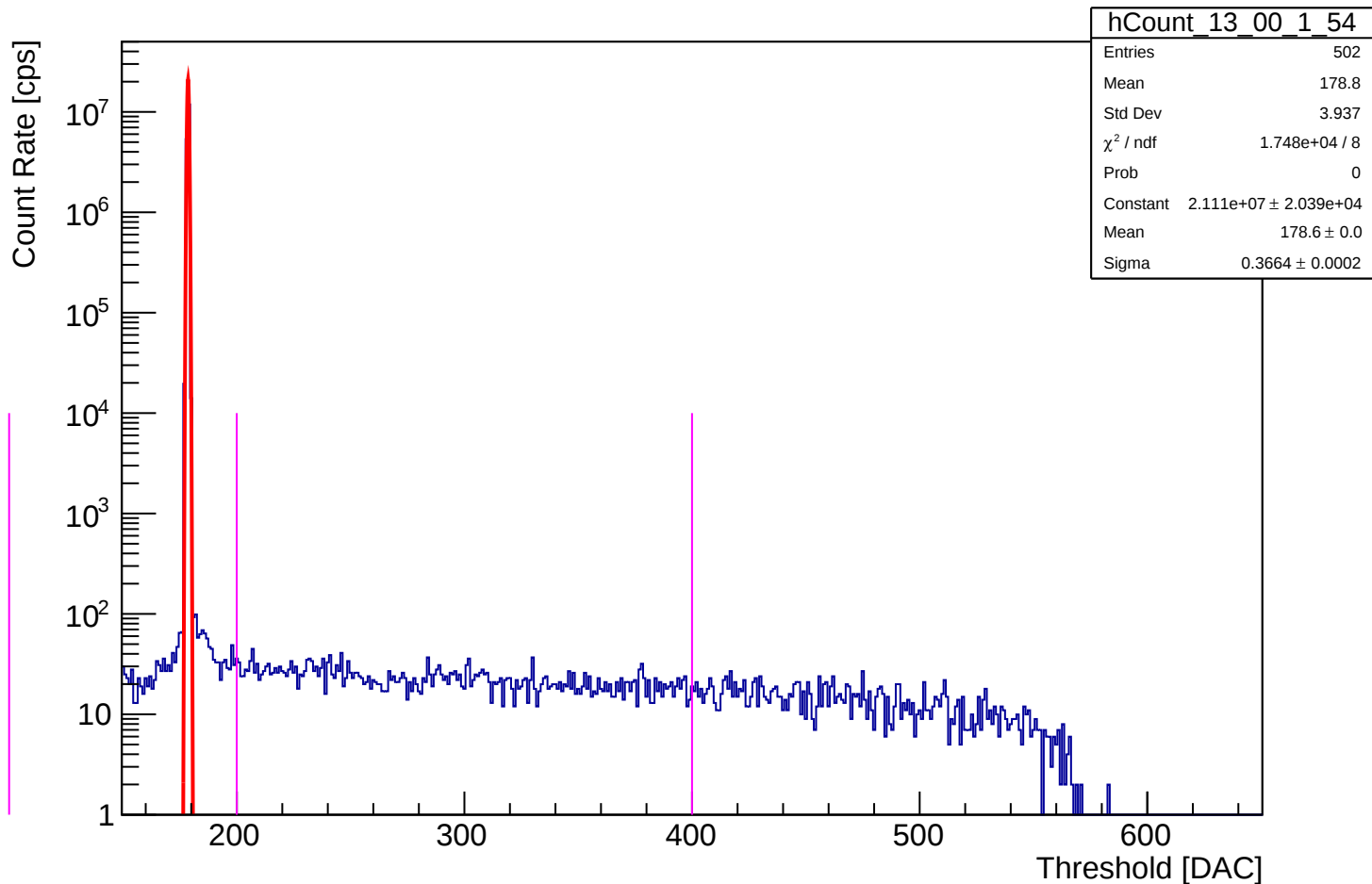




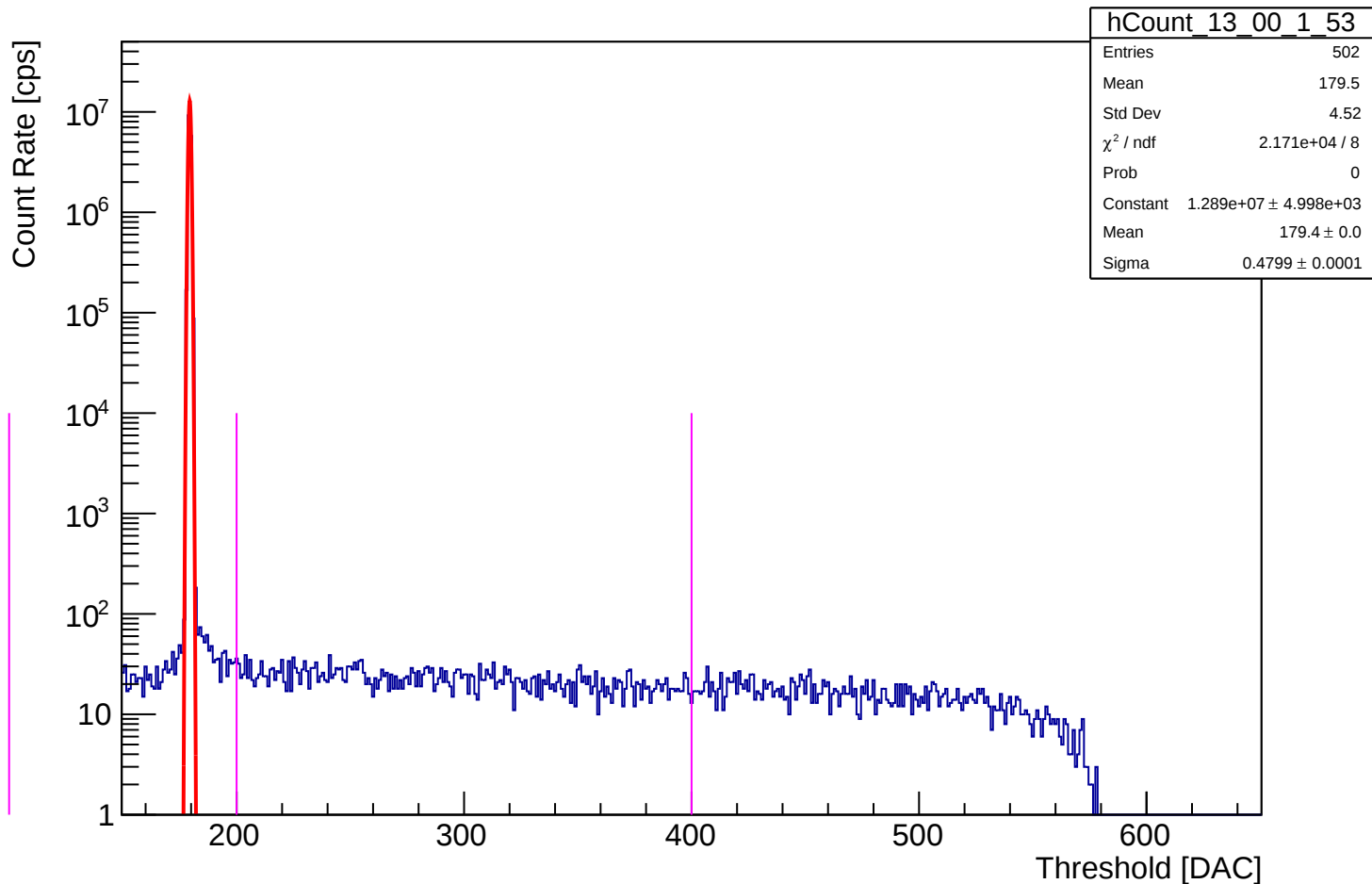
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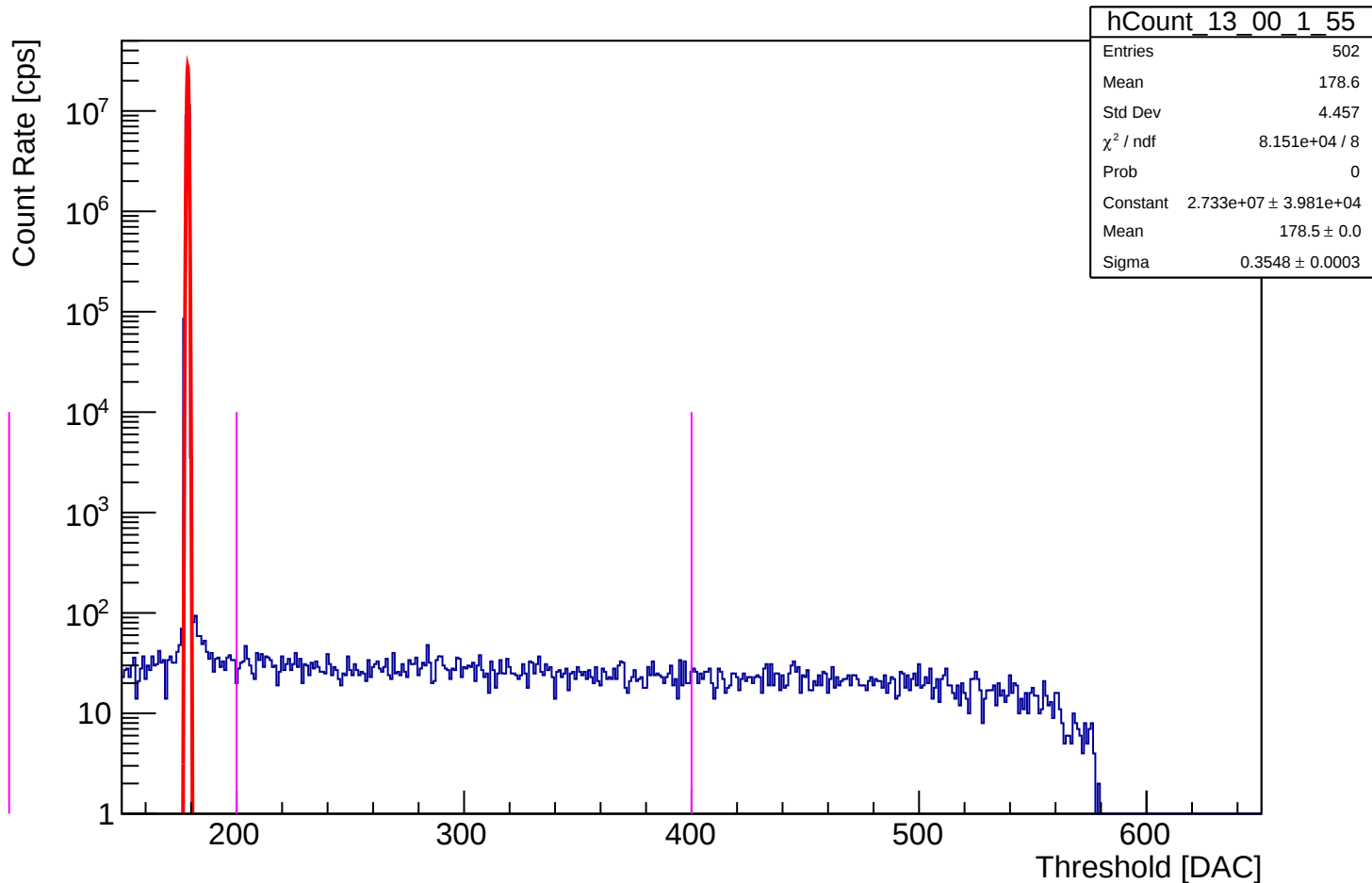
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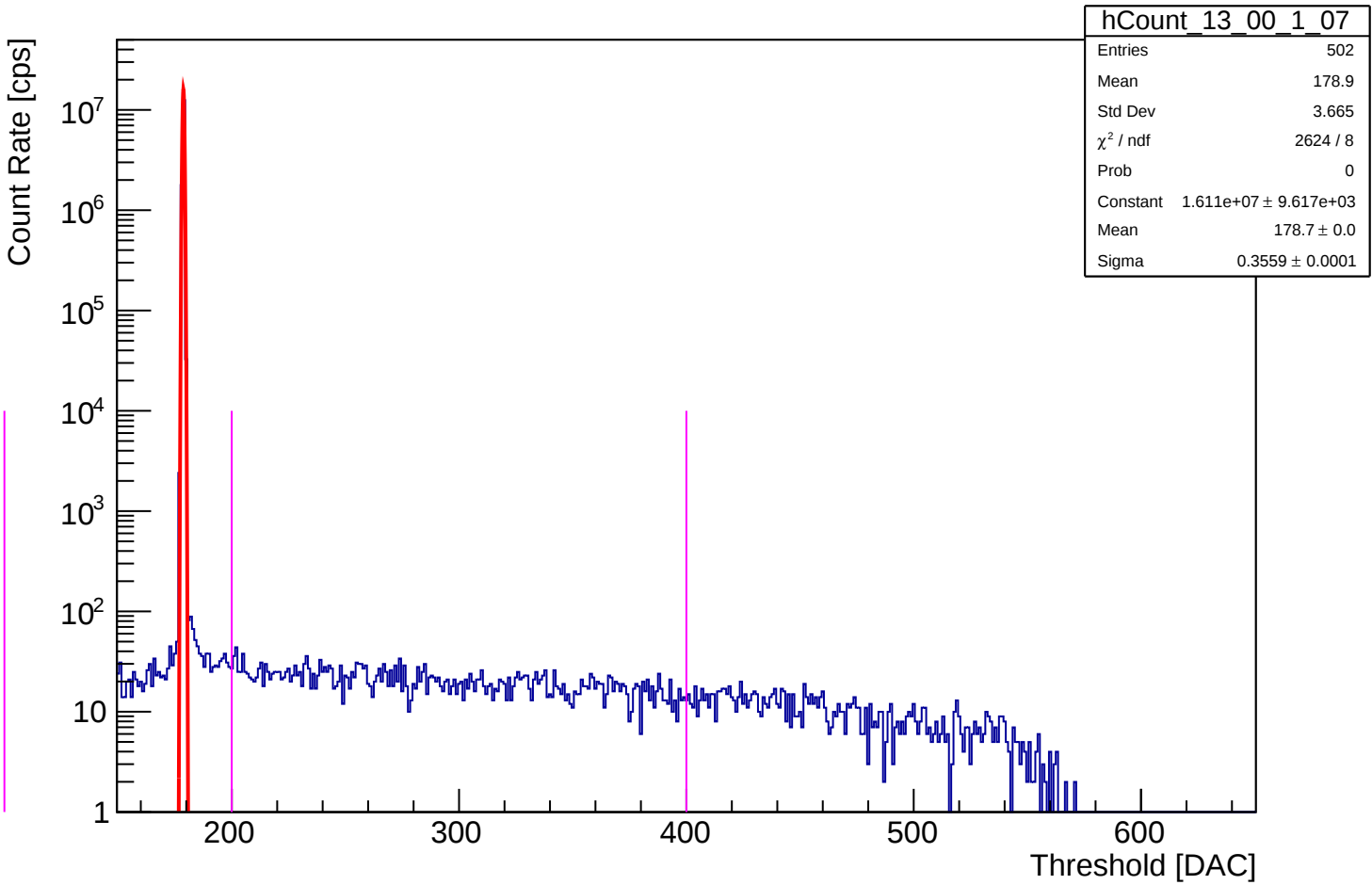


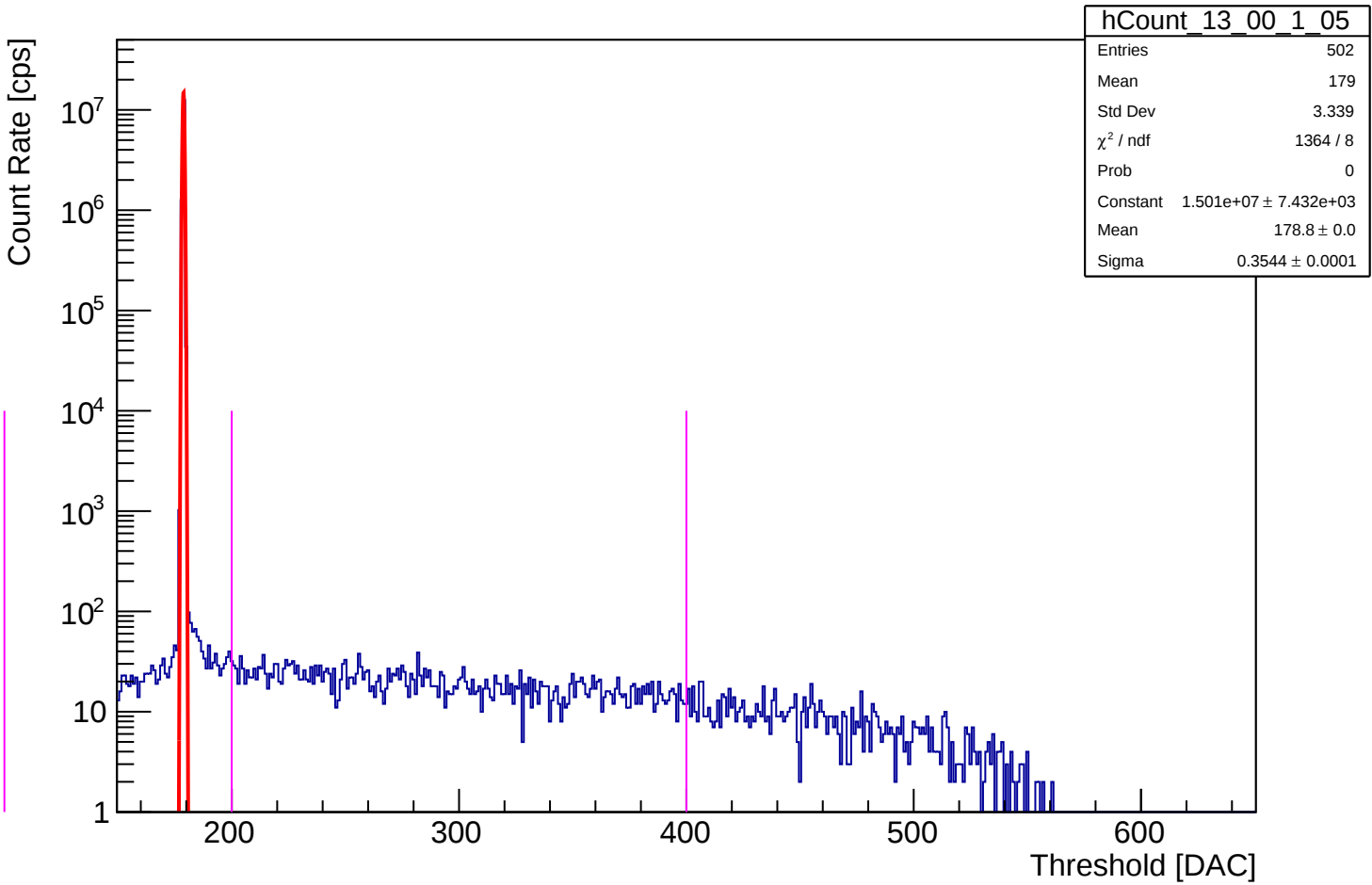
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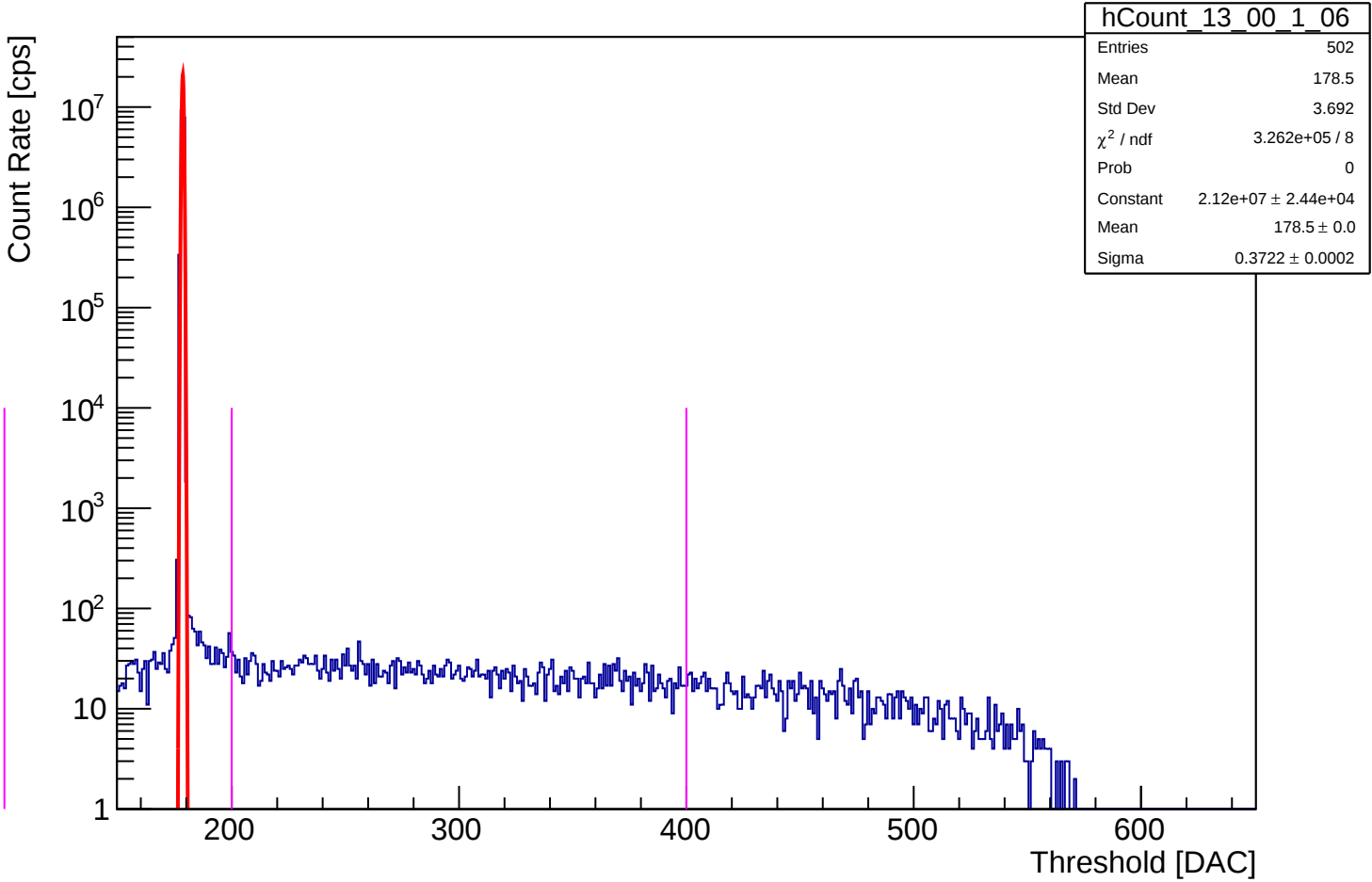


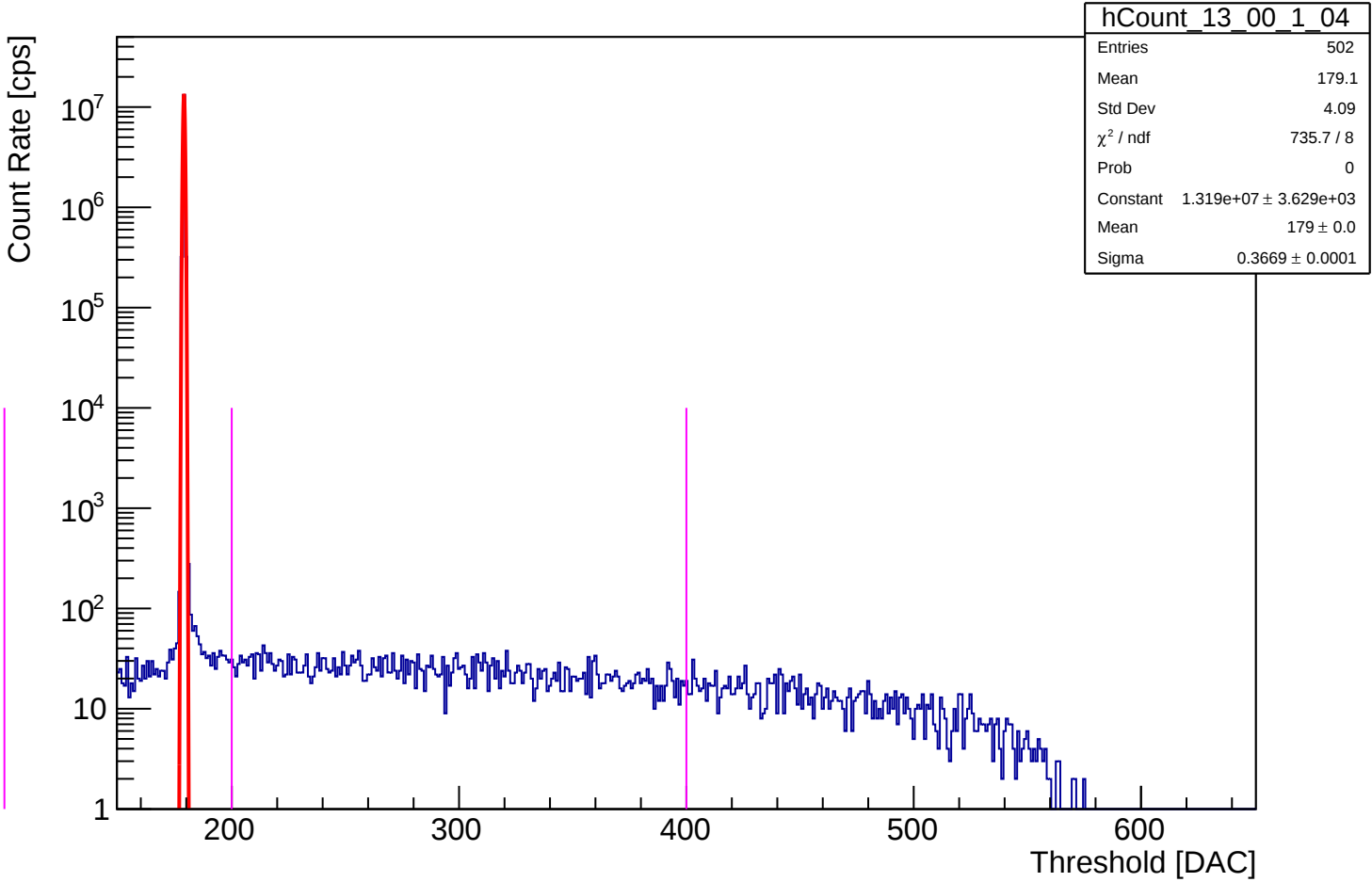
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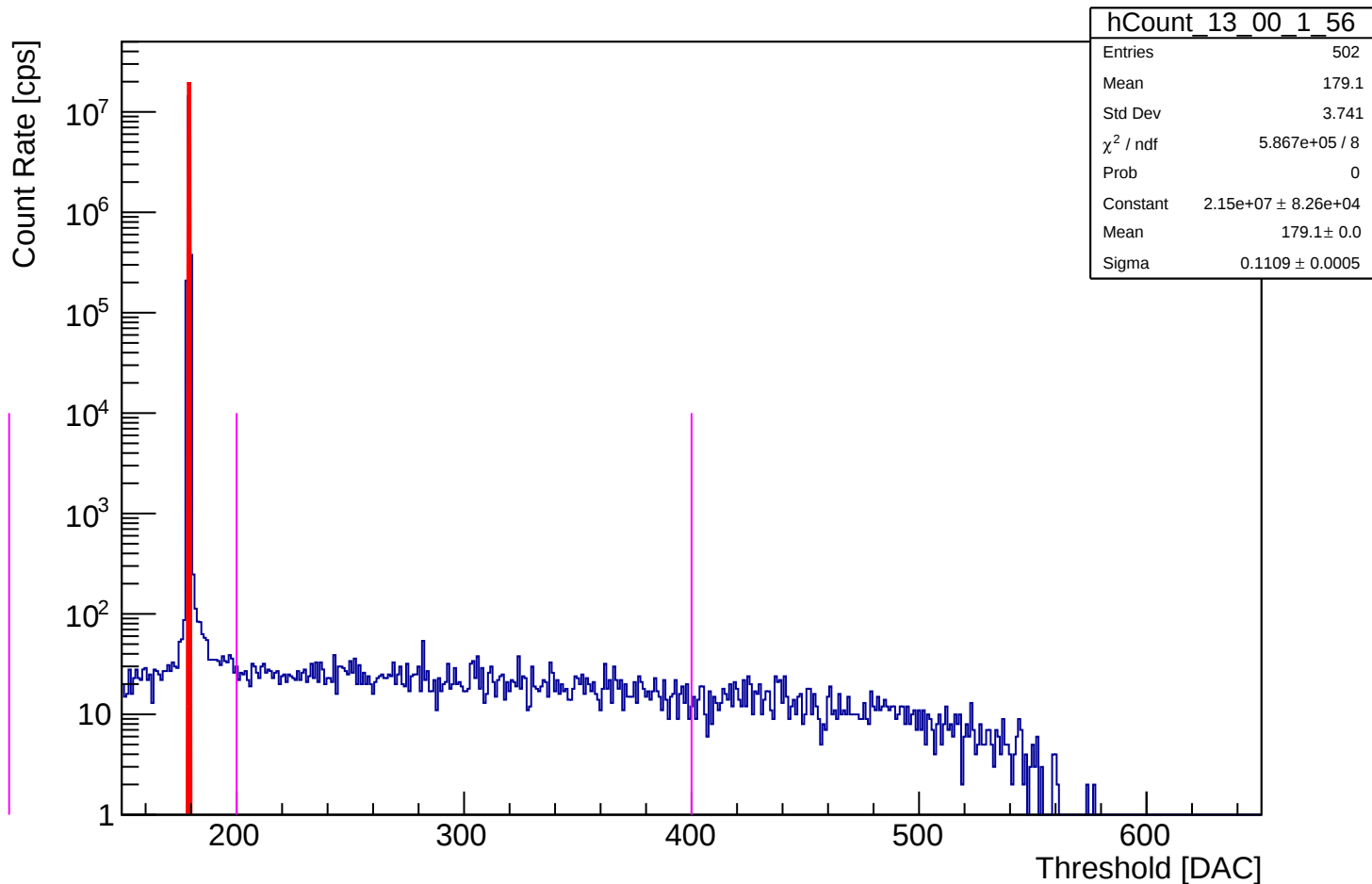




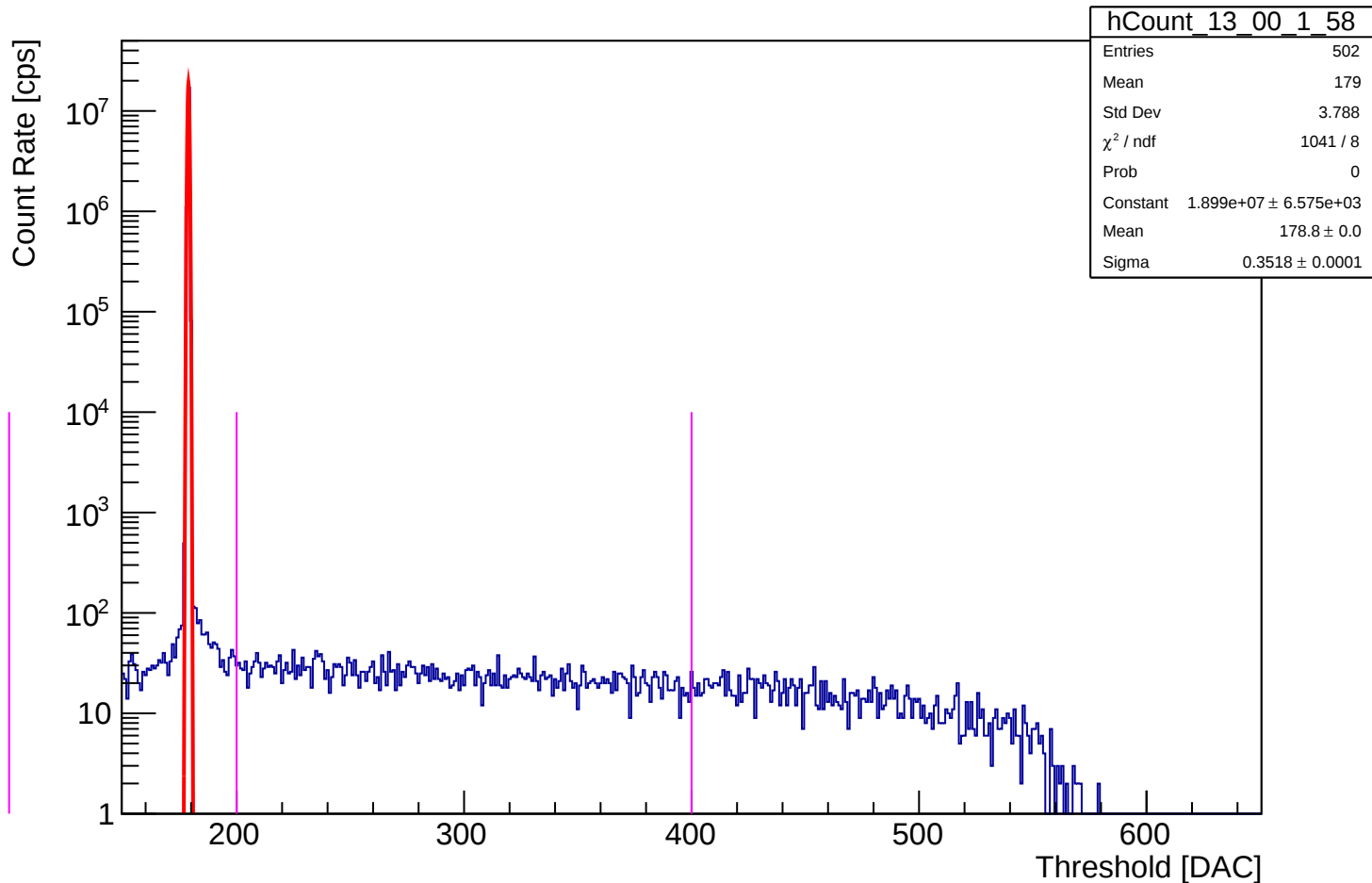




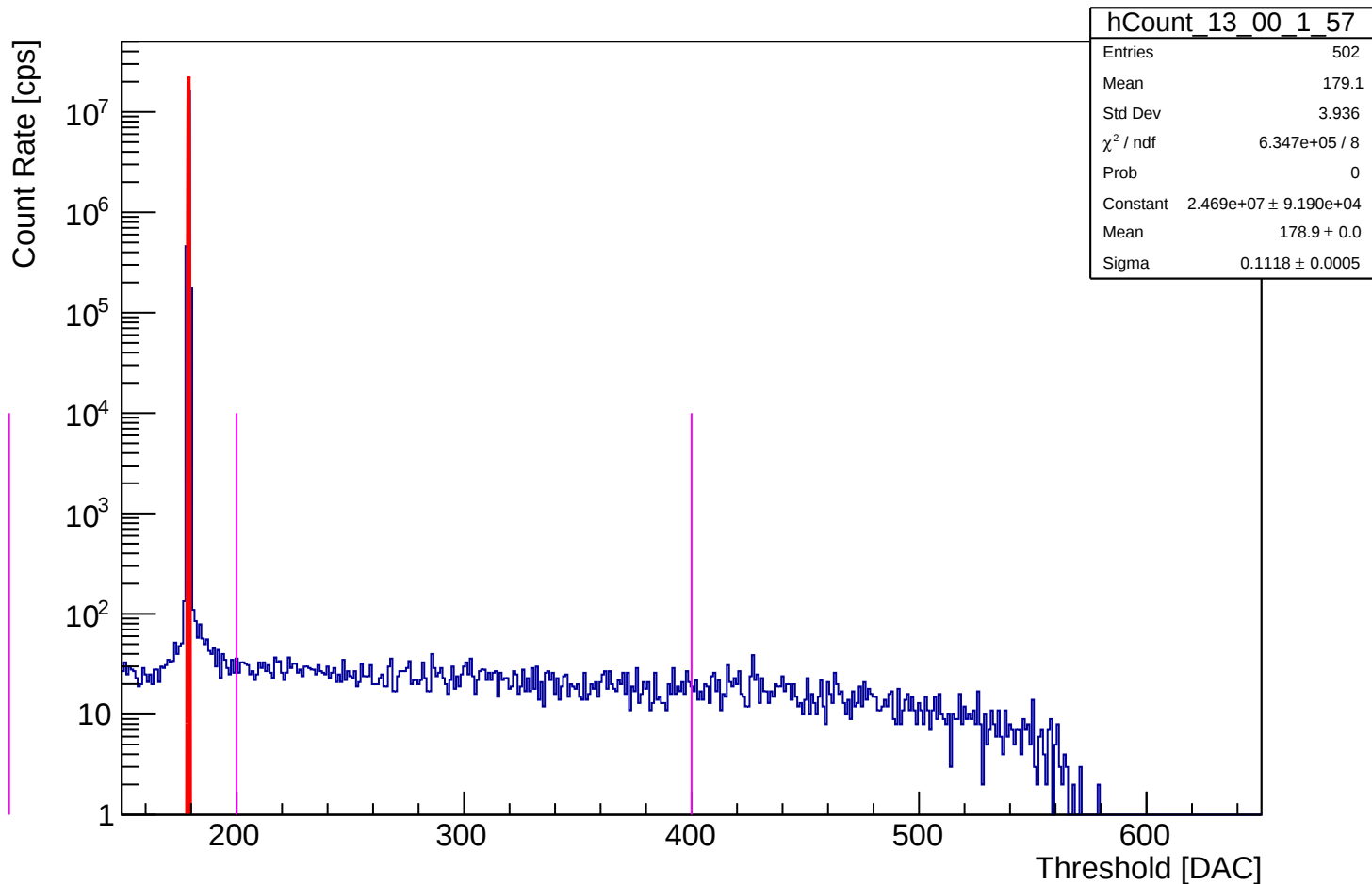
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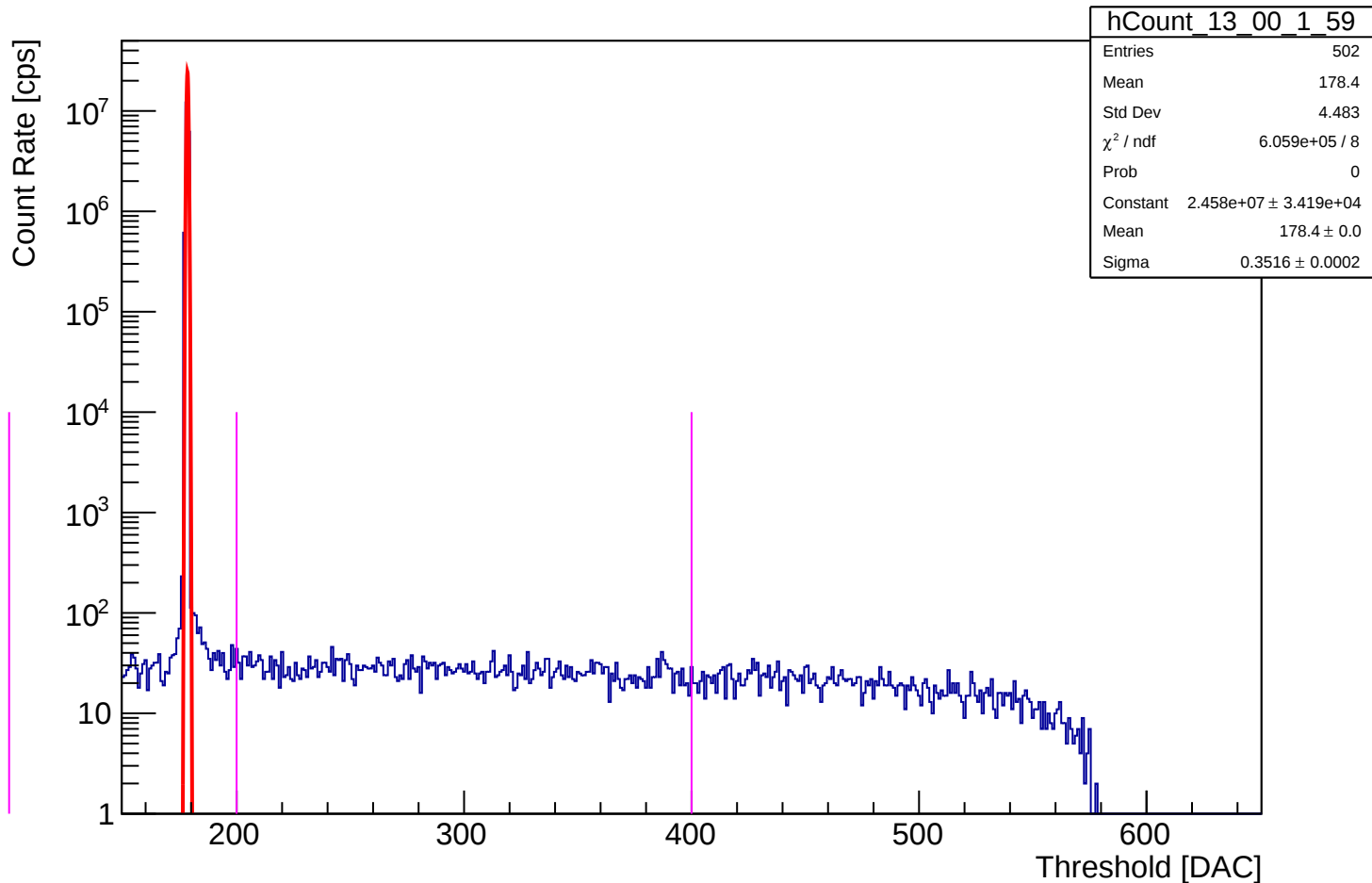
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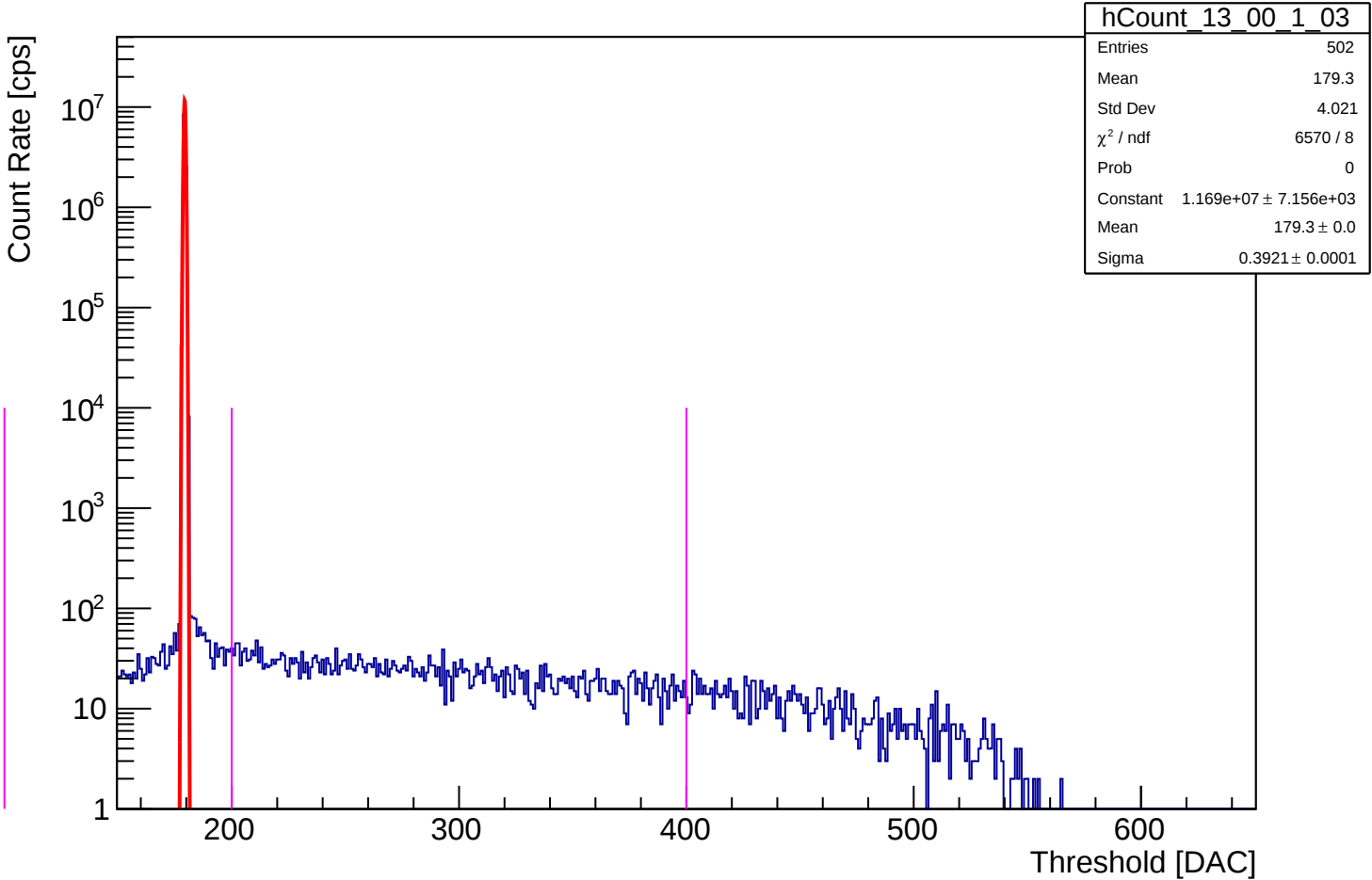


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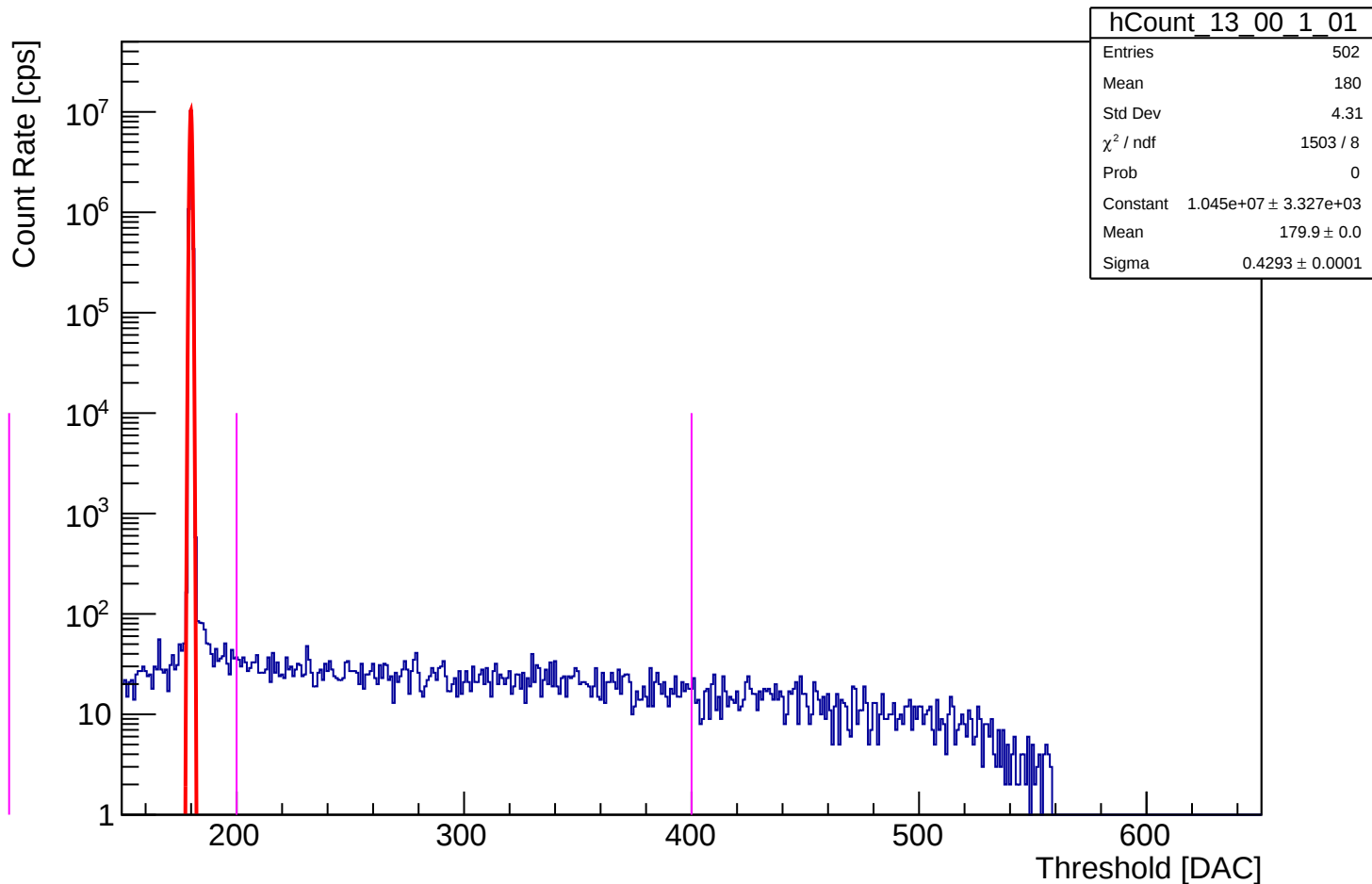


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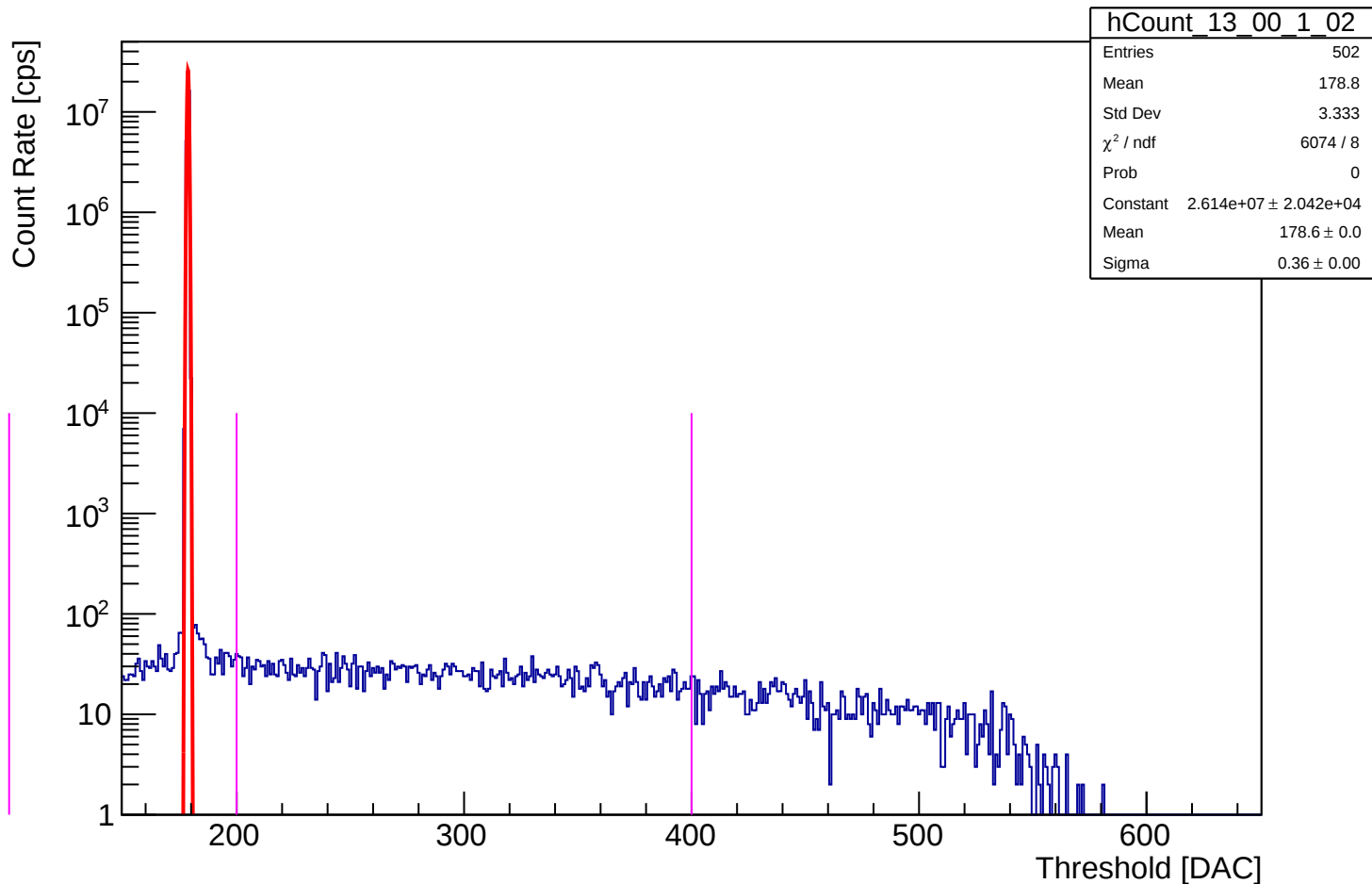




Row 1 Tile 1 Pmt 2 Pixel 58 Slot 13 Fiber 0 Asic 1 Channel 1



Row 1 Tile 1 Pmt 2 Pixel 59 Slot 13 Fiber 0 Asic 1 Channel 2



Count Rate [cps]

10<sup>7</sup>  
10<sup>6</sup>  
10<sup>5</sup>  
10<sup>4</sup>  
10<sup>3</sup>  
10<sup>2</sup>  
10  
1

200

300

400

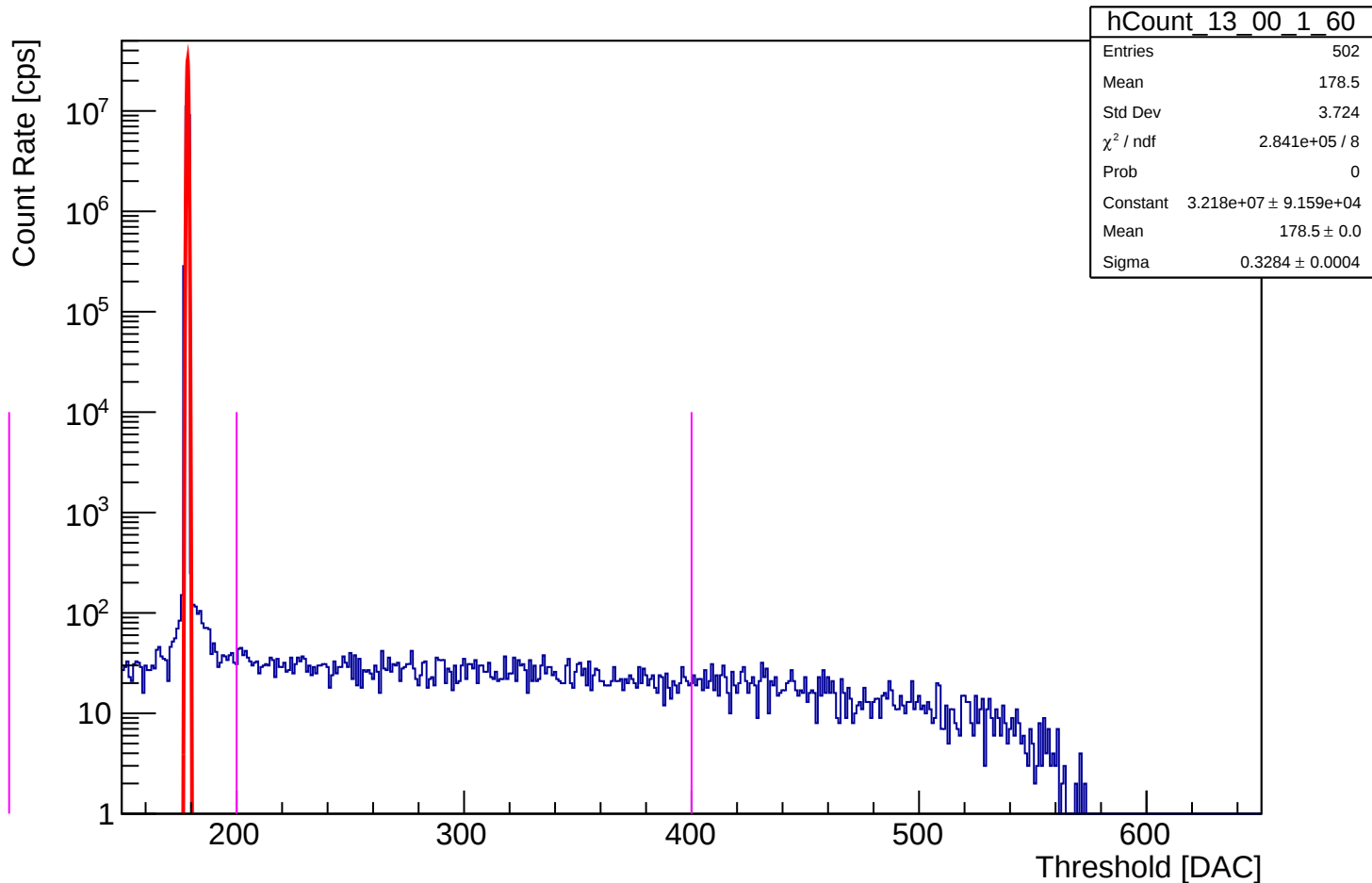
500

600

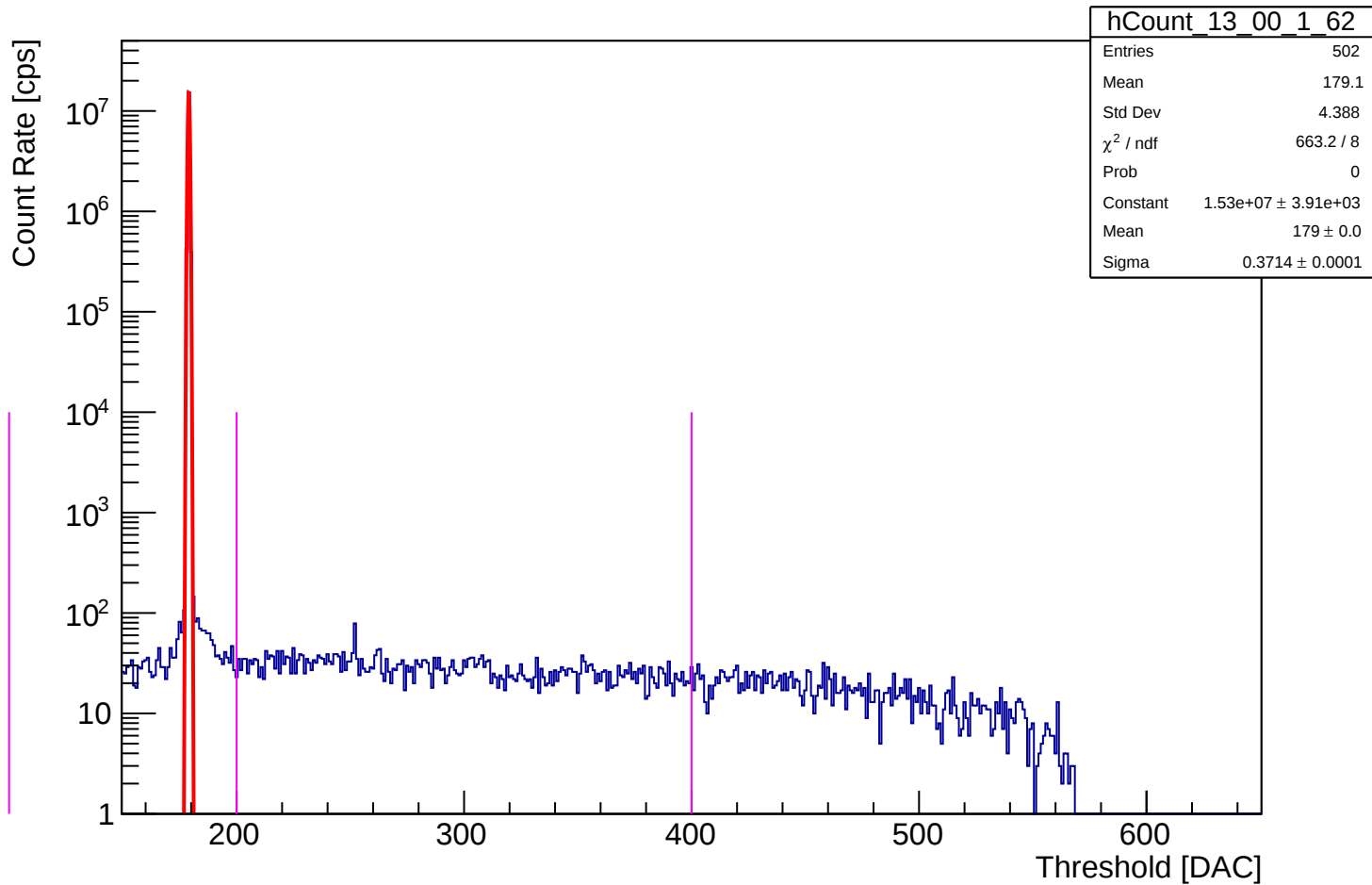
Threshold [DAC]

| hCount_13_00_1_00 |                           |
|-------------------|---------------------------|
| Entries           | 502                       |
| Mean              | 180.2                     |
| Std Dev           | 4.973                     |
| $\chi^2$ / ndf    | 857.7 / 8                 |
| Prob              | 0                         |
| Constant          | 1.087e+07 $\pm$ 3.618e+03 |
| Mean              | 180.1 $\pm$ 0.0           |
| Sigma             | 0.3854 $\pm$ 0.0001       |

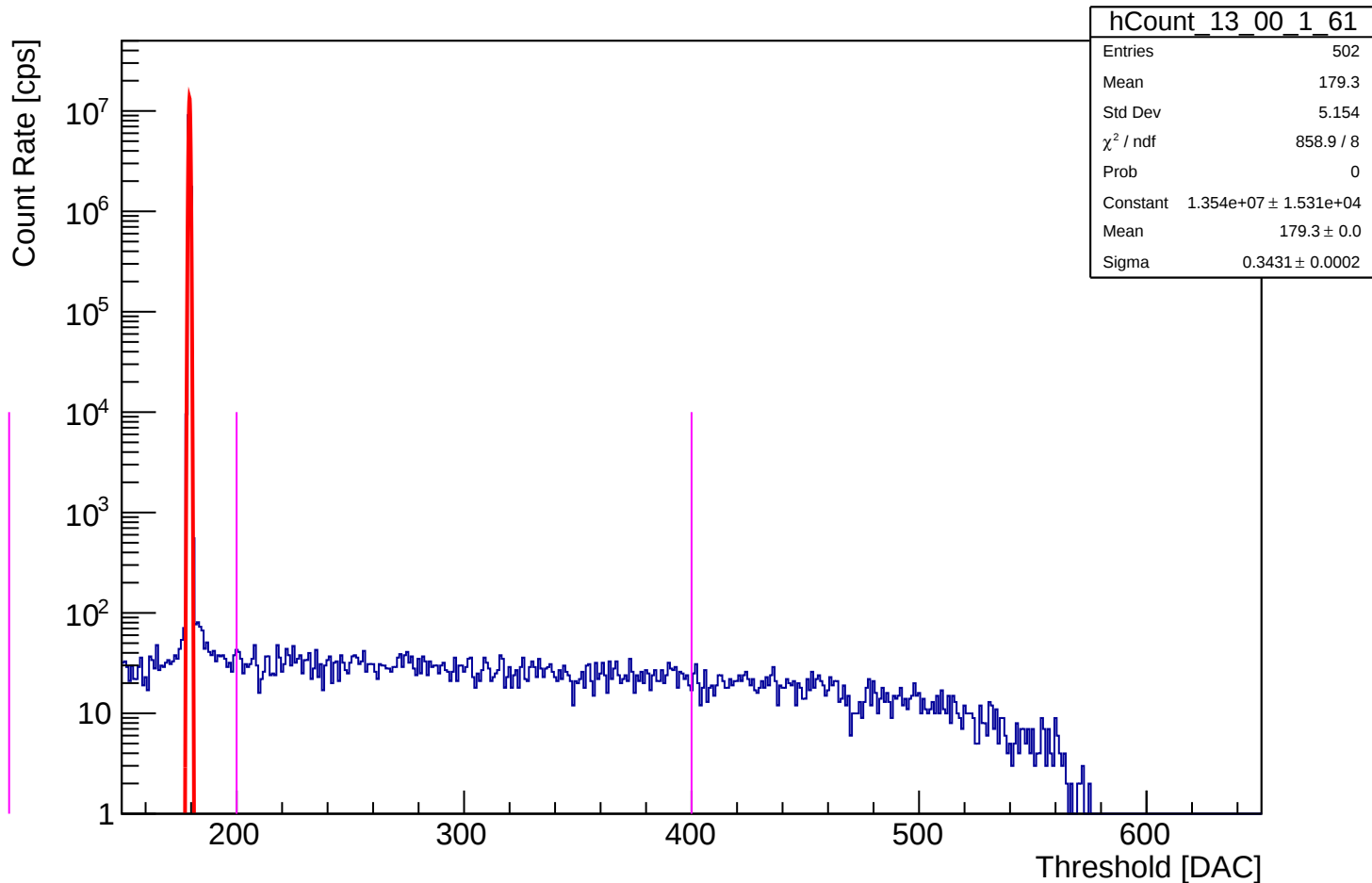
Row 1 Tile 1 Pmt 2 Pixel 61 Slot 13 Fiber 0 Asic 1 Channel 60



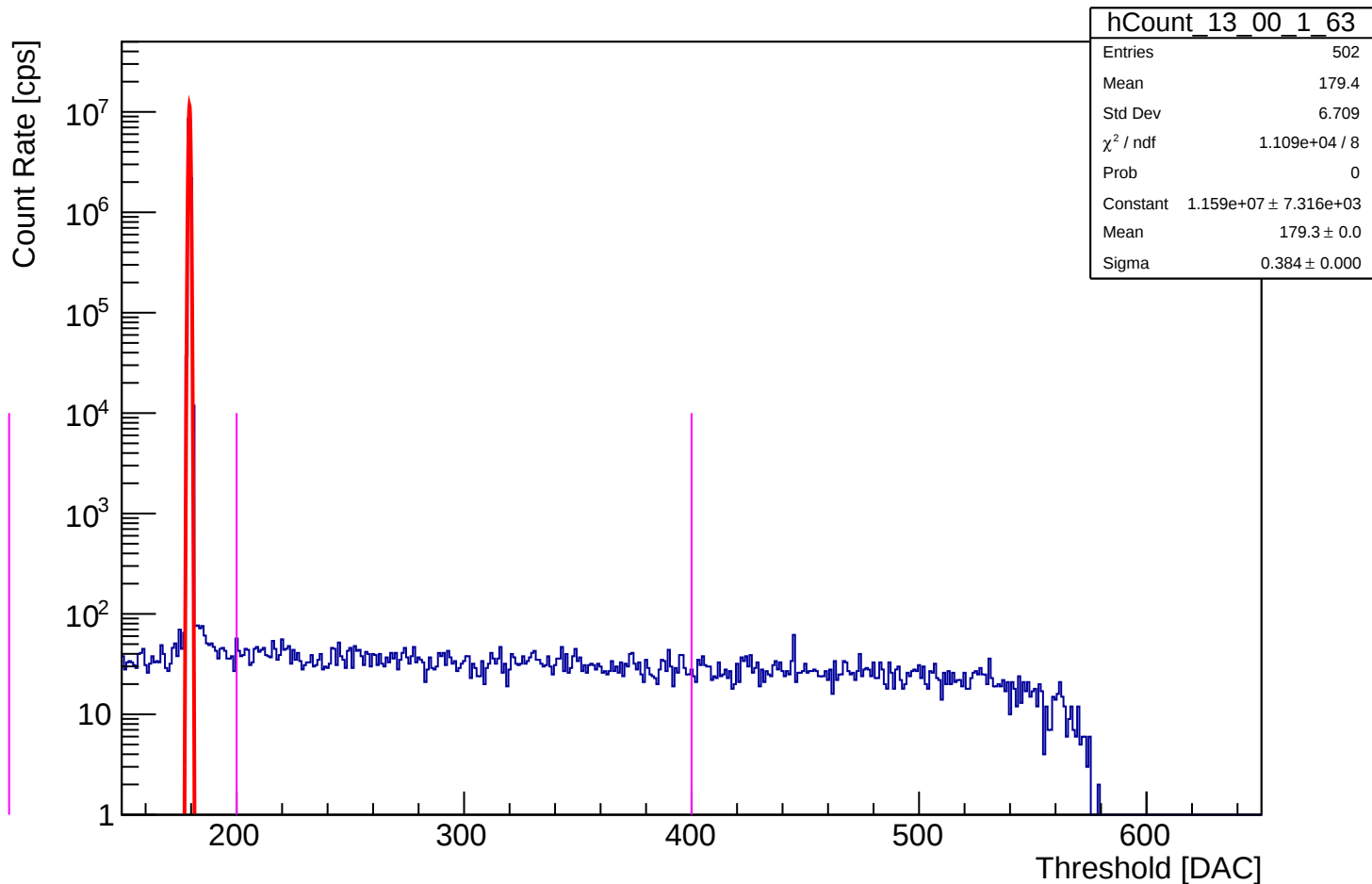
Row 1 Tile 1 Pmt 2 Pixel 62 Slot 13 Fiber 0 Asic 1 Channel 62



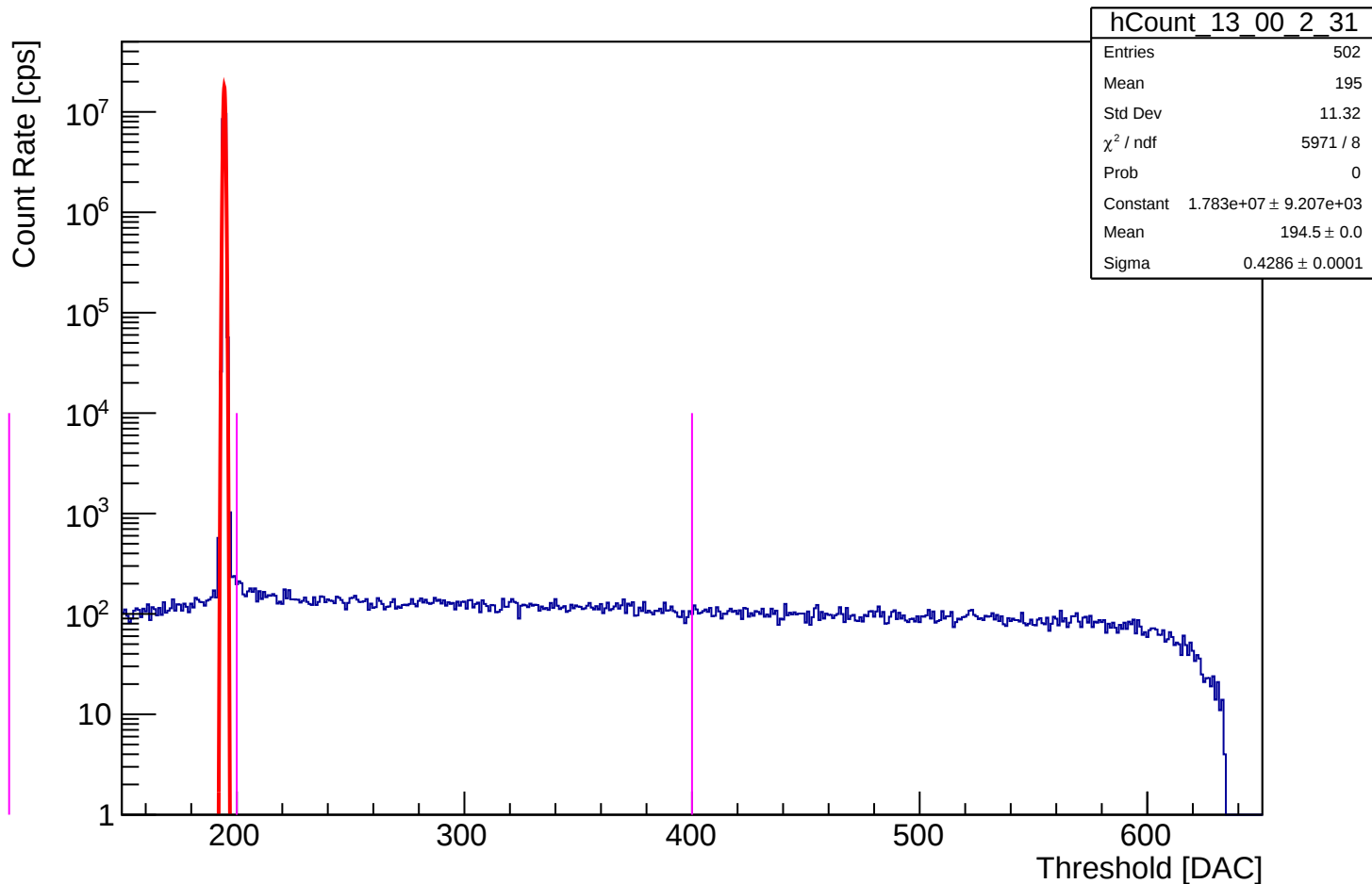
Row 1 Tile 1 Pmt 2 Pixel 63 Slot 13 Fiber 0 Asic 1 Channel 61



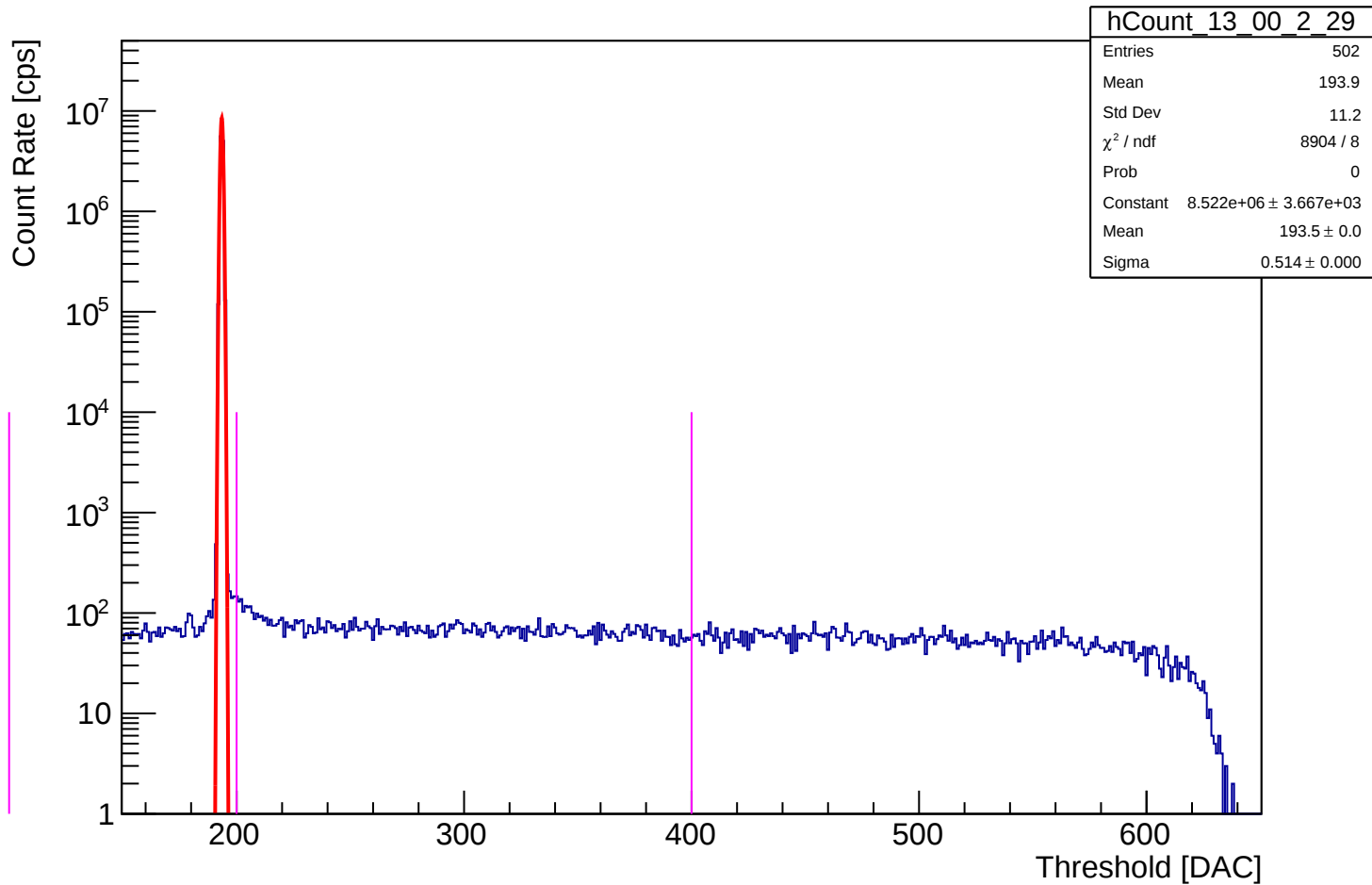
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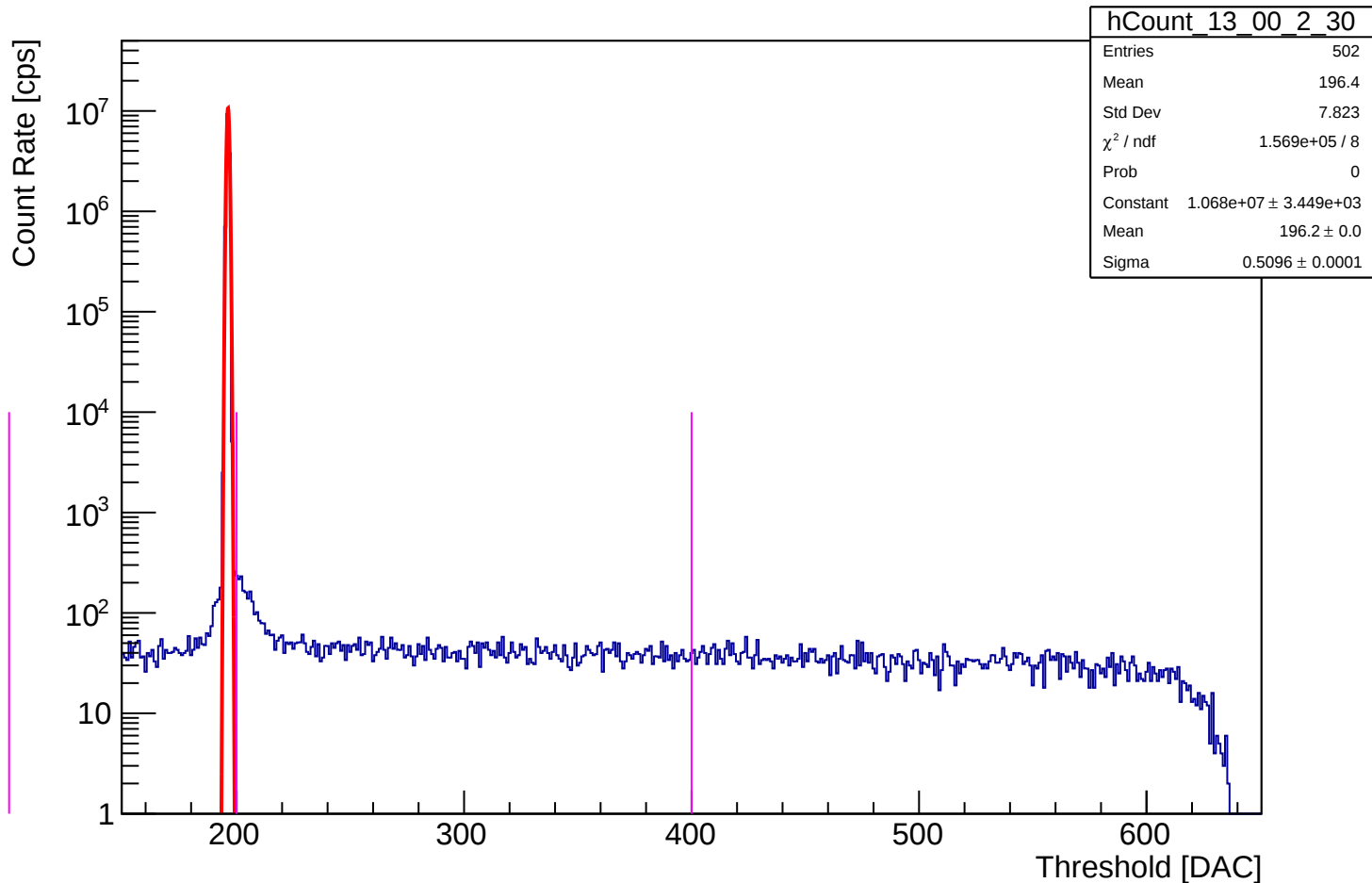
Row 1 Tile 1 Pmt 3 Pixel 1 Slot 13 Fiber 0 Asic 2 Channel 31



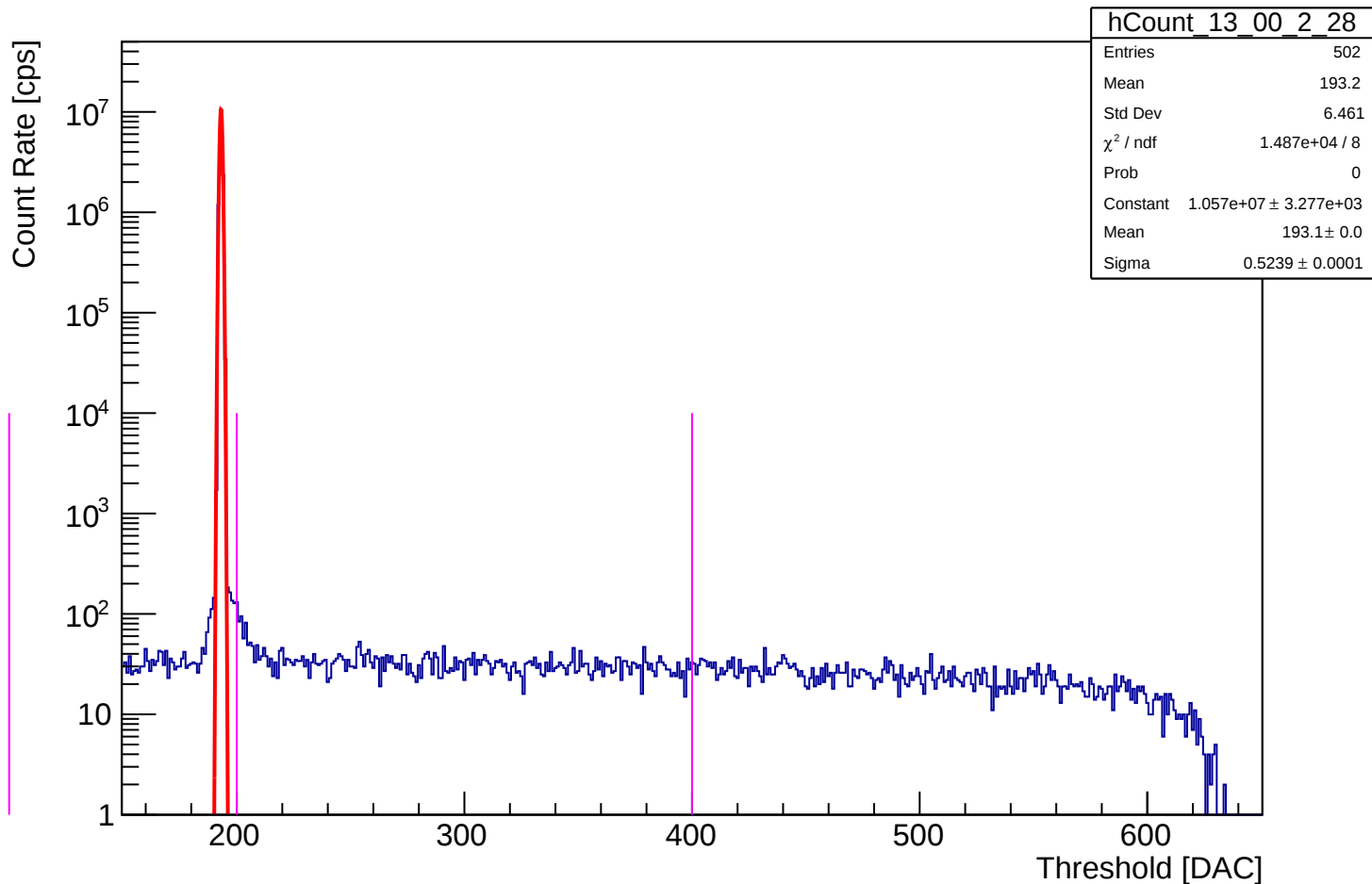
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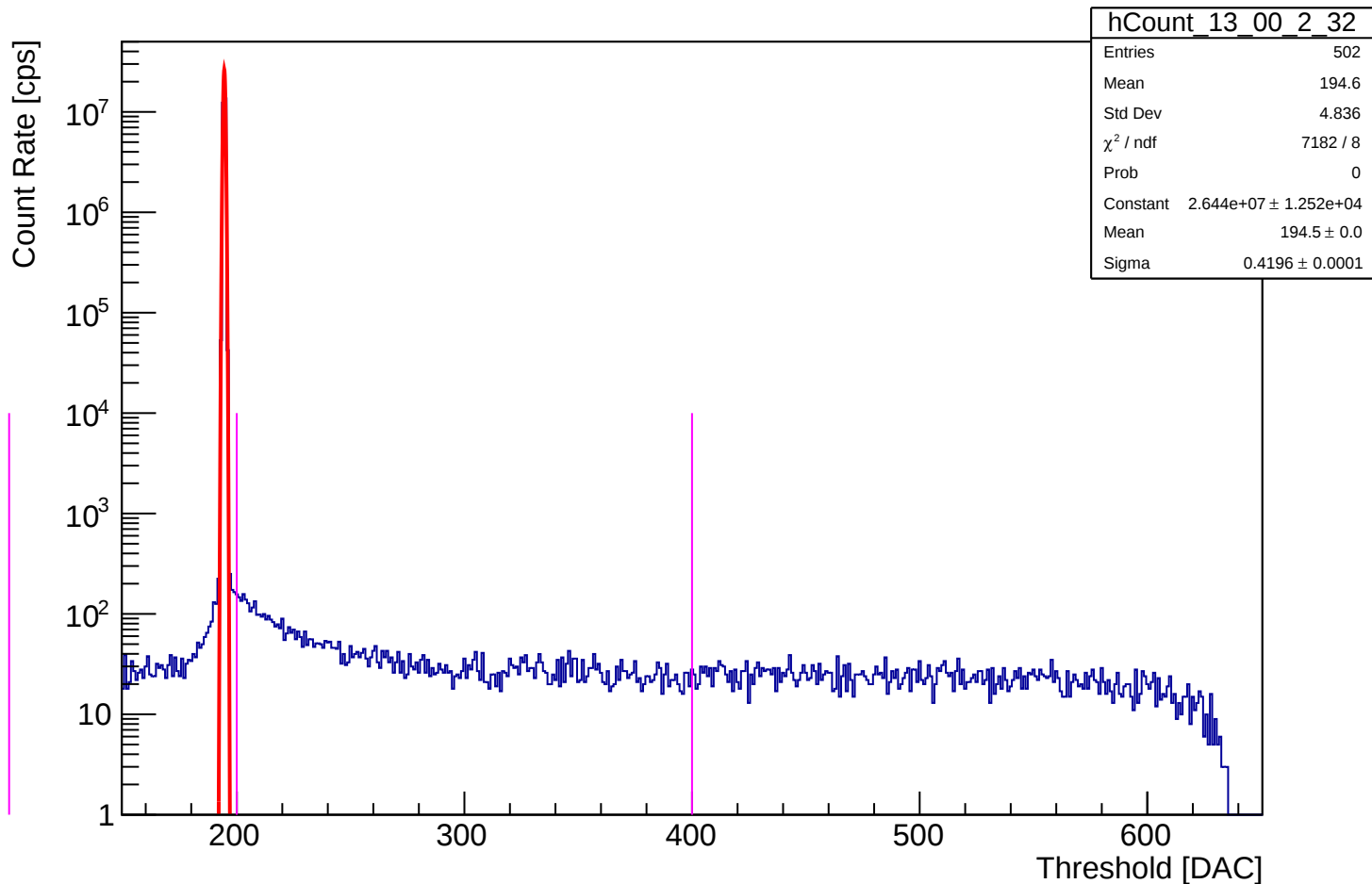
Row 1 Tile 1 Pmt 3 Pixel 3 Slot 13 Fiber 0 Asic 2 Channel 30



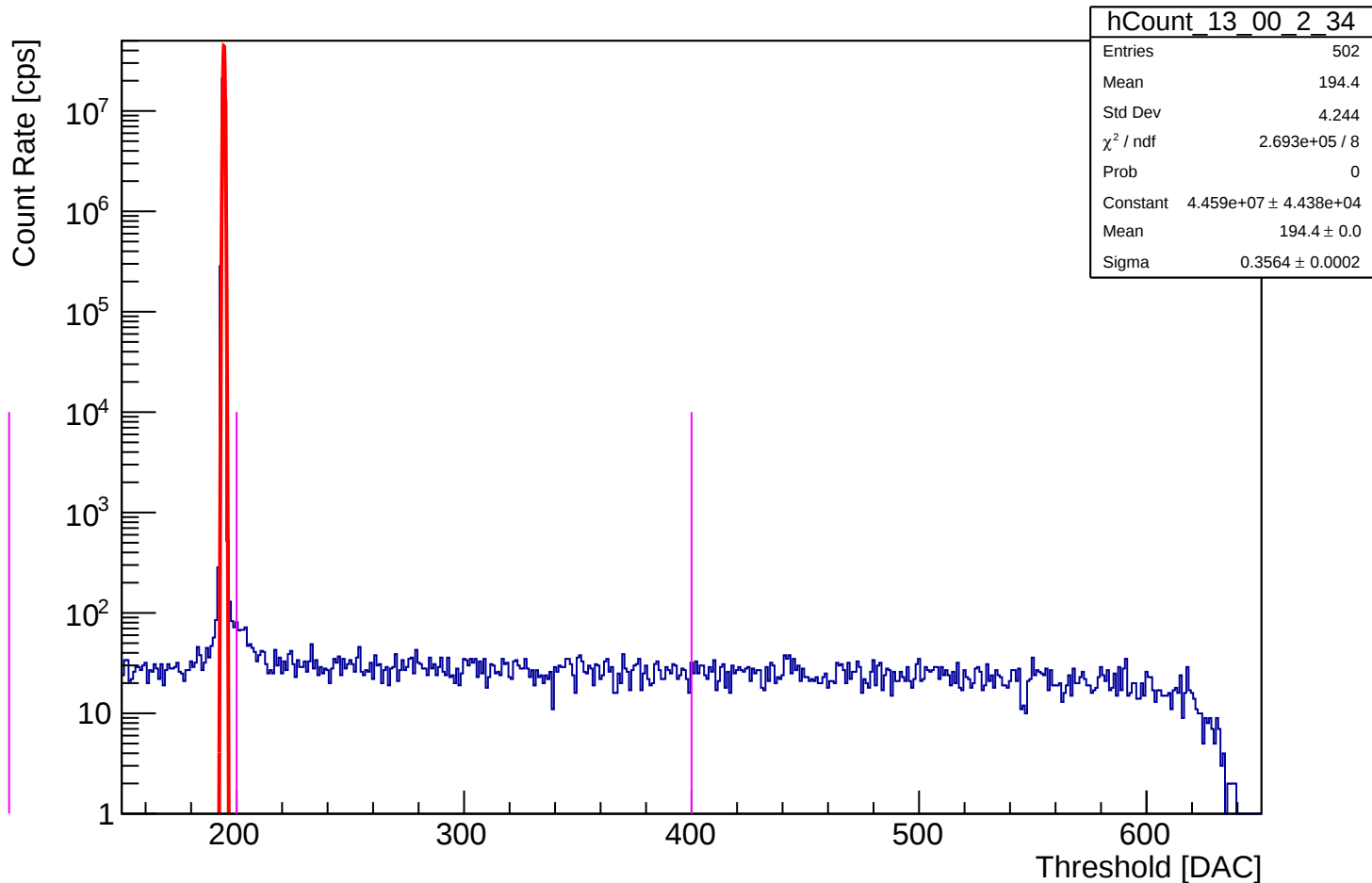
Row 1 Tile 1 Pmt 3 Pixel 4 Slot 13 Fiber 0 Asic 2 Channel 28



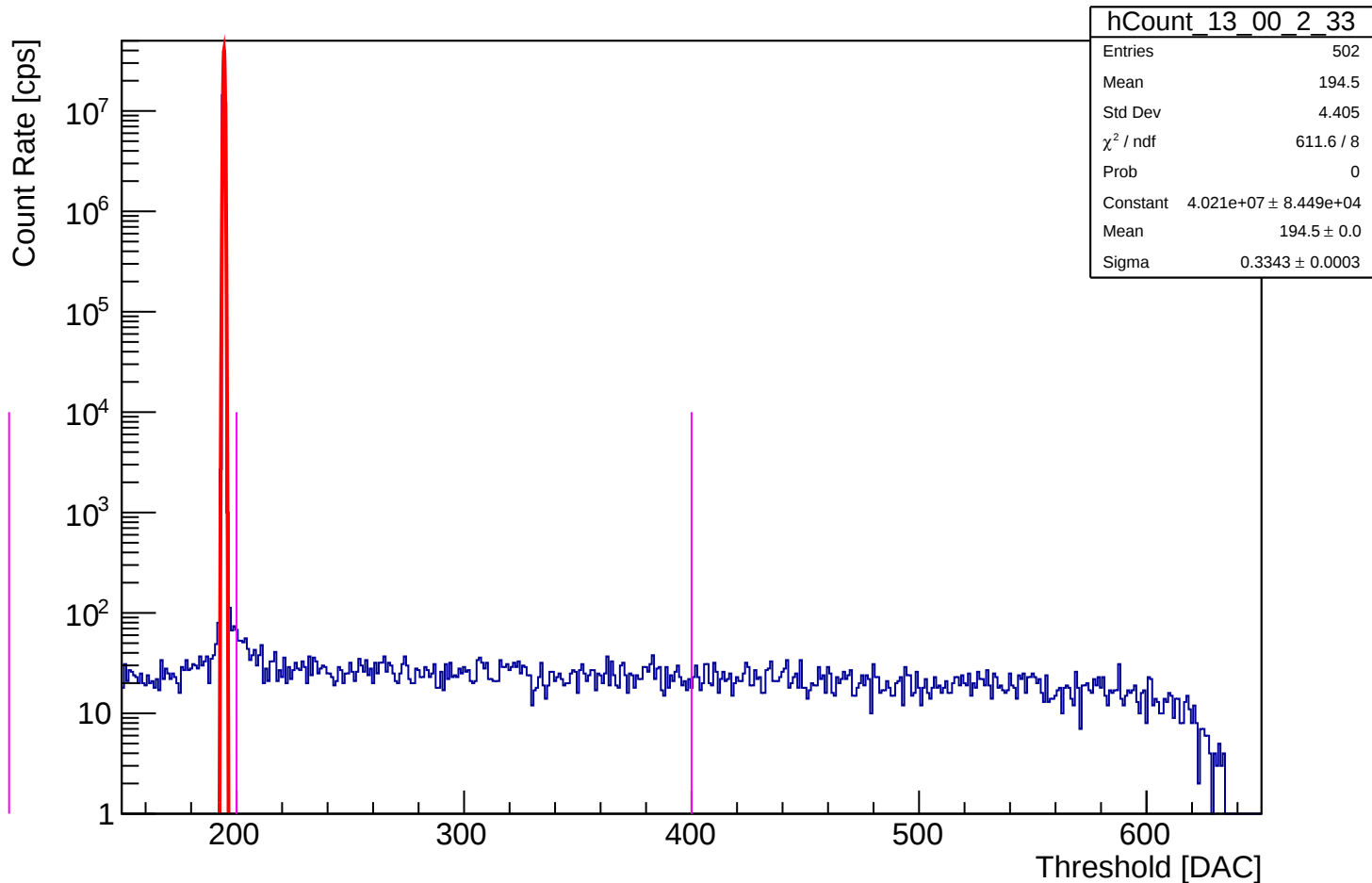
Row 1 Tile 1 Pmt 3 Pixel 5 Slot 13 Fiber 0 Asic 2 Channel 32



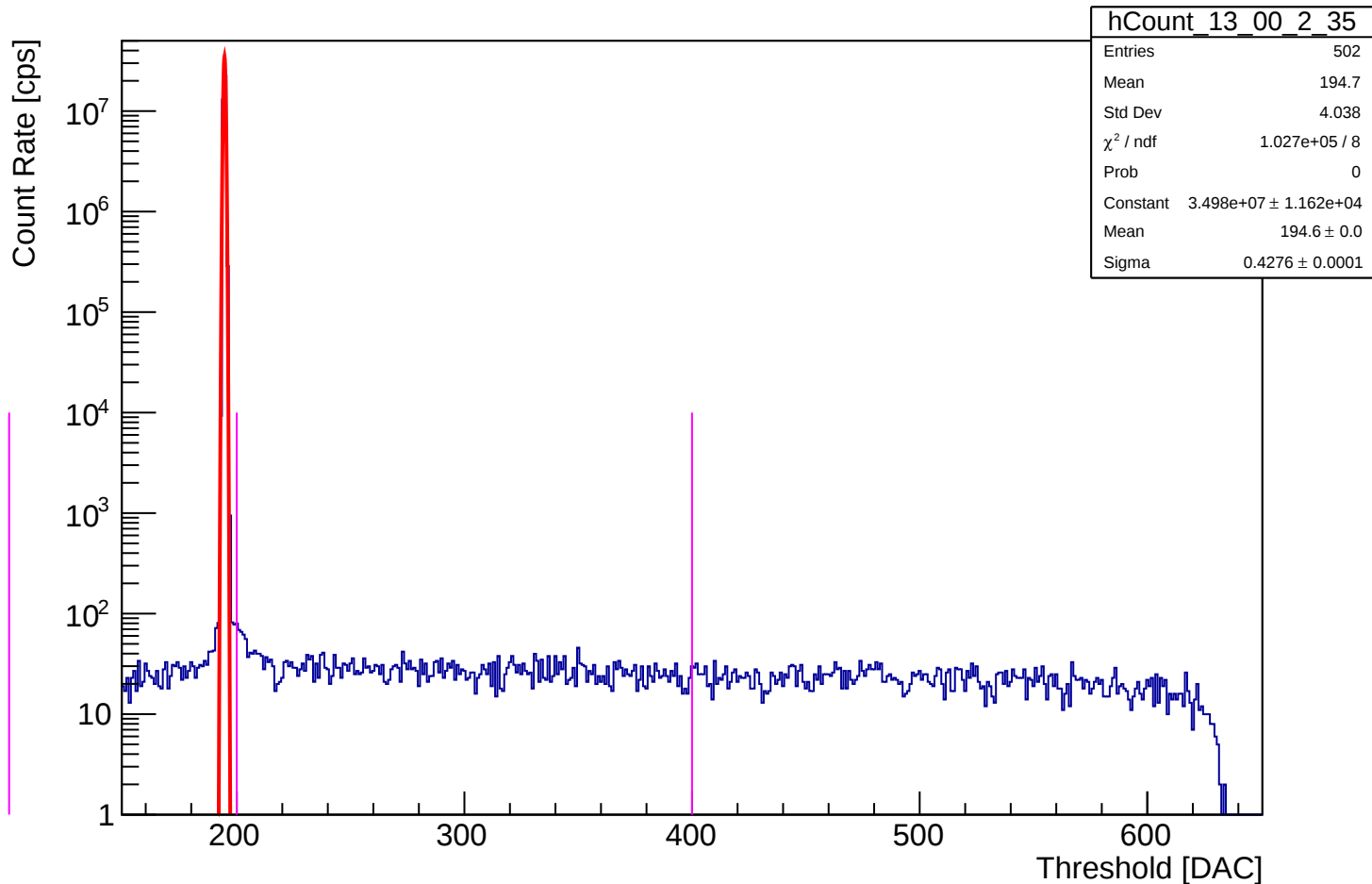
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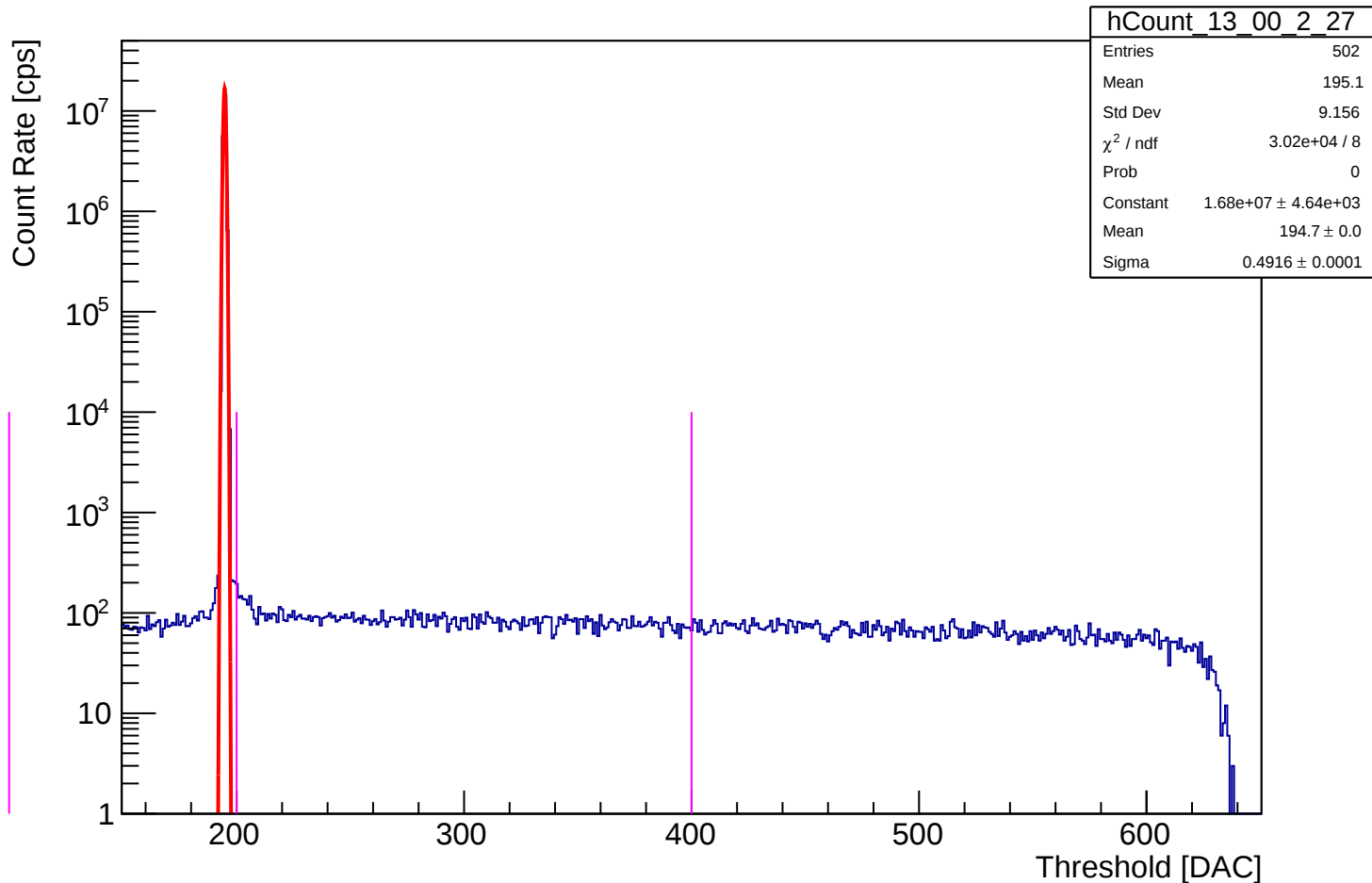
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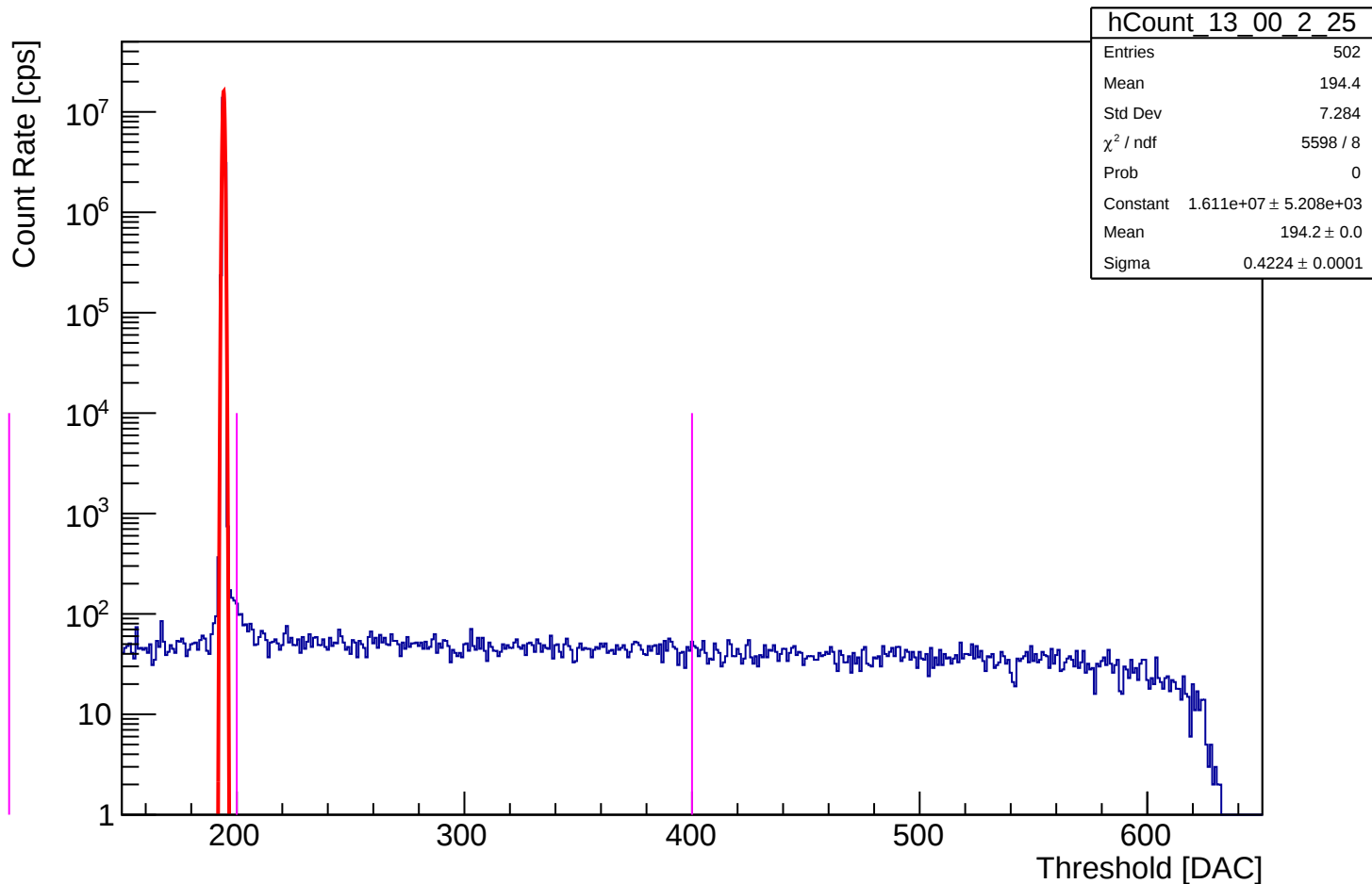
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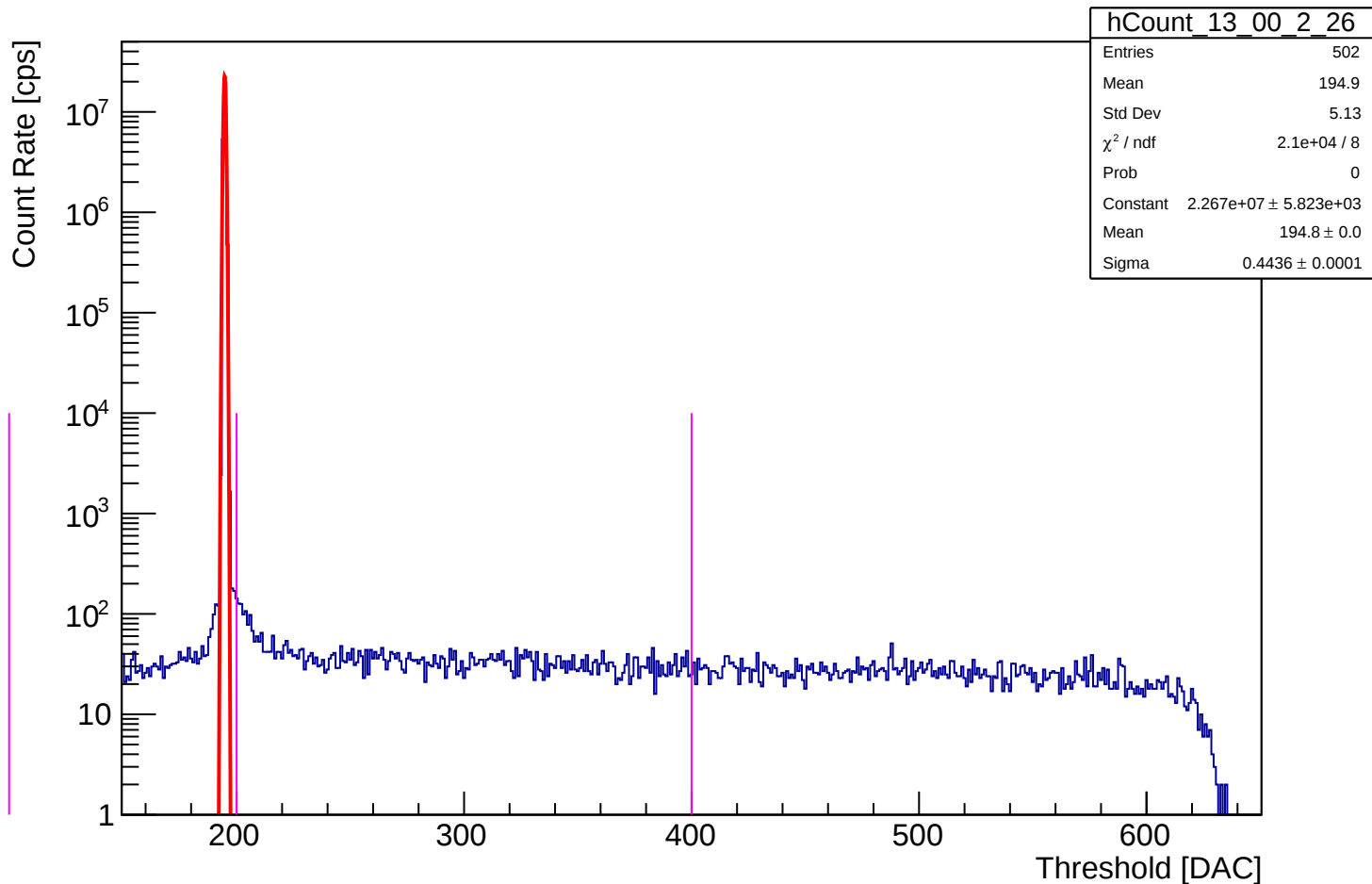
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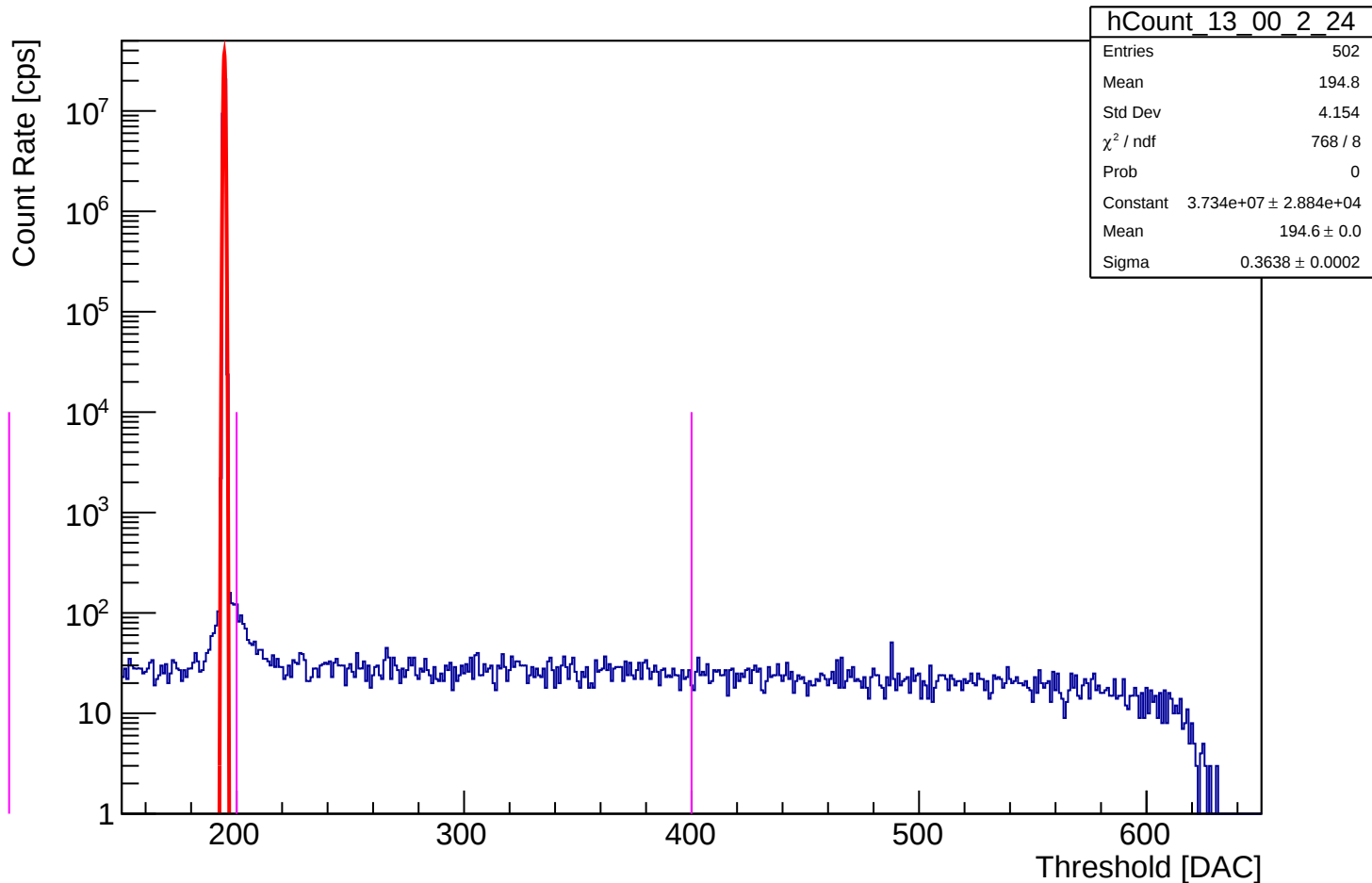
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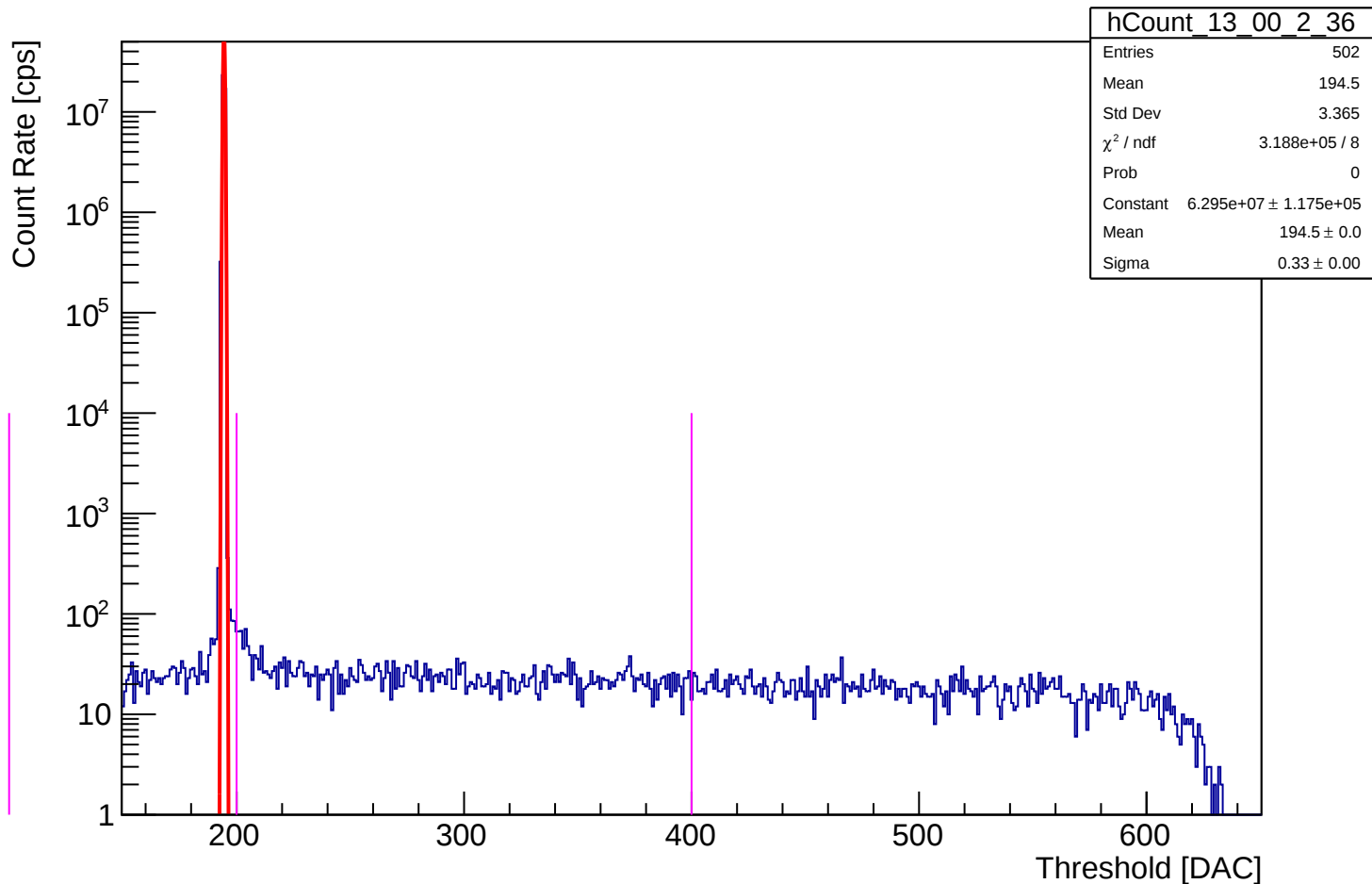
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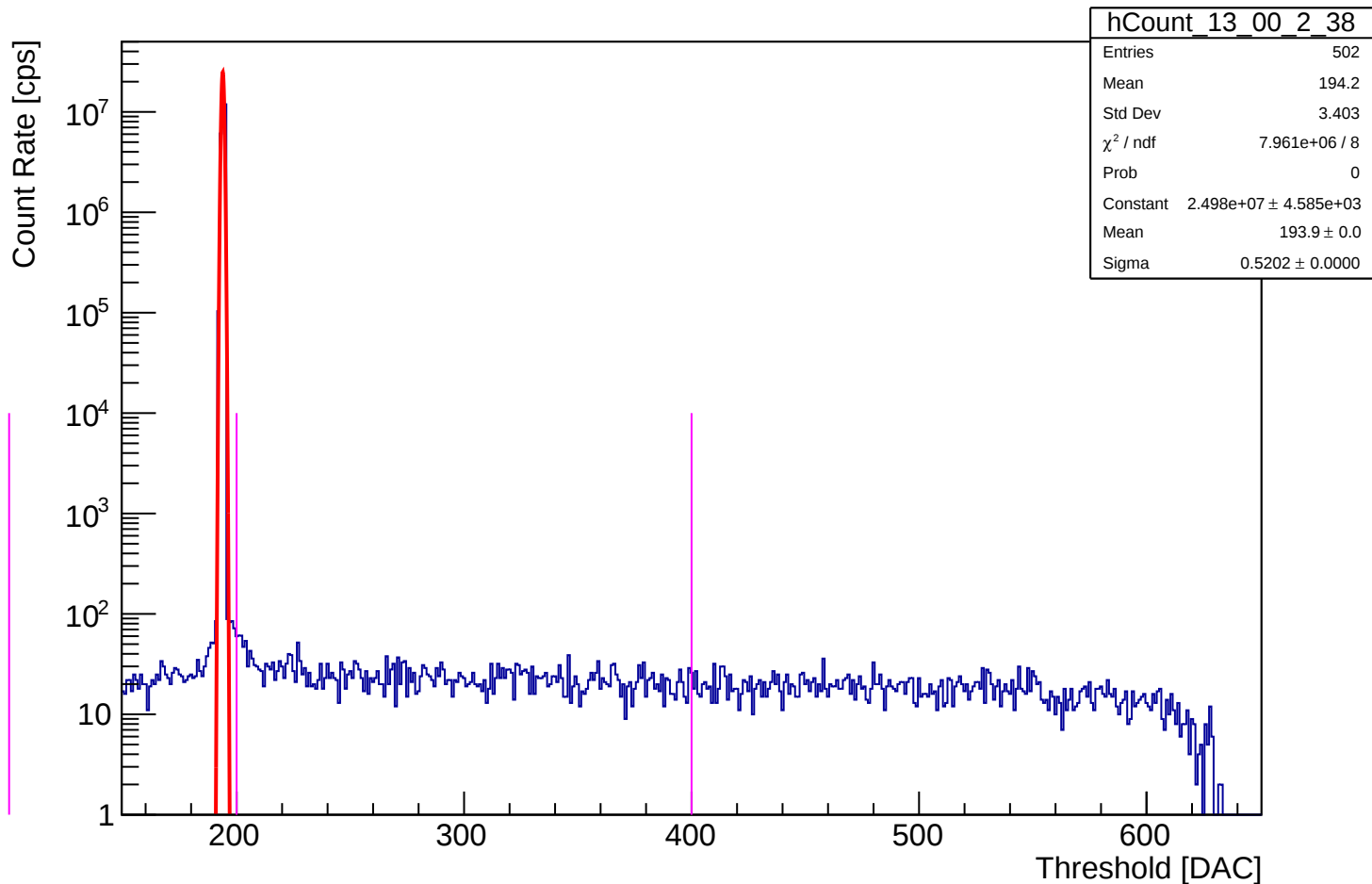
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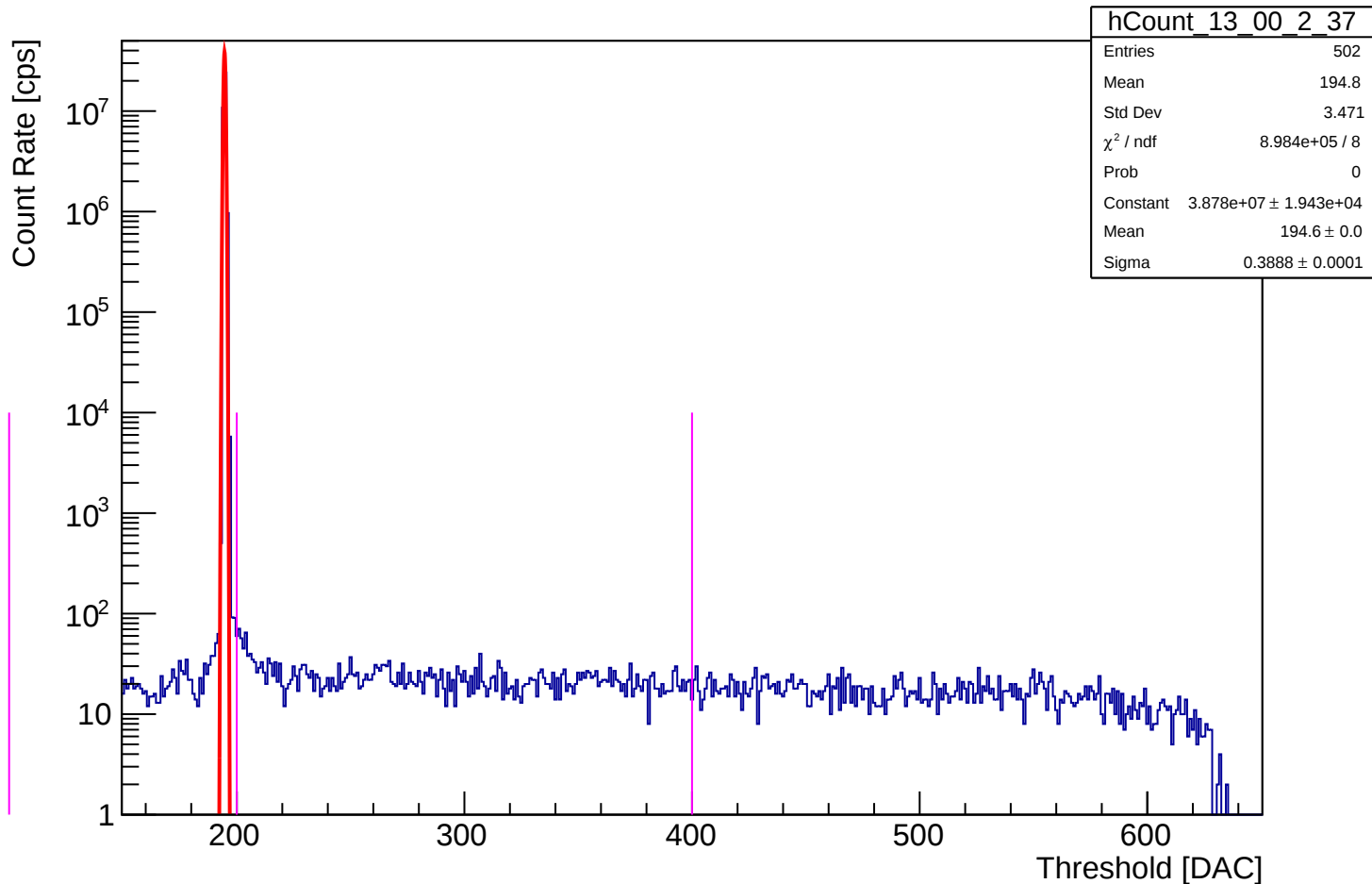
Row 1 Tile 1 Pmt 3 Pixel 13 Slot 13 Fiber 0 Asic 2 Channel 36



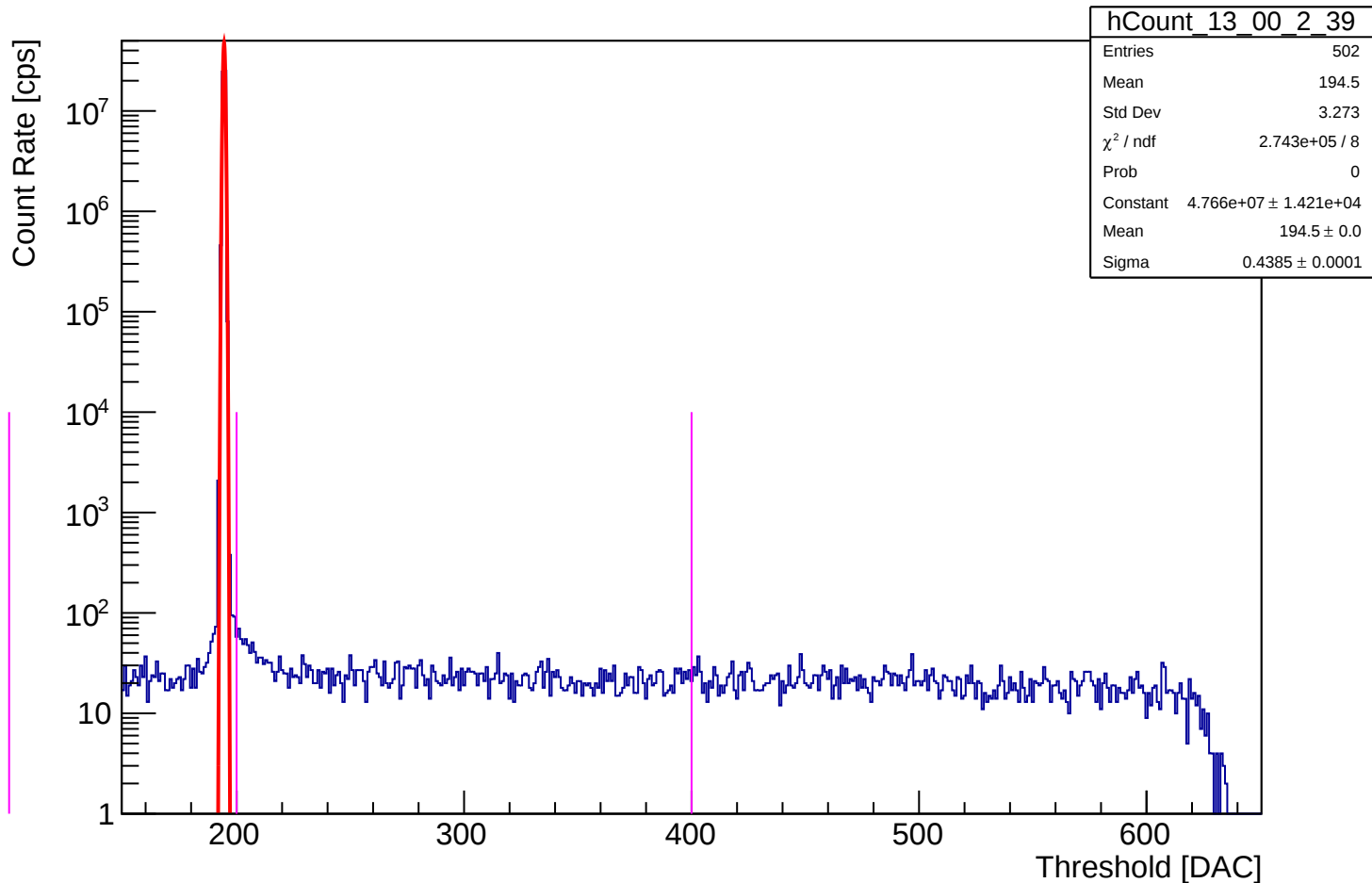
Row 1 Tile 1 Pmt 3 Pixel 14 Slot 13 Fiber 0 Asic 2 Channel 38



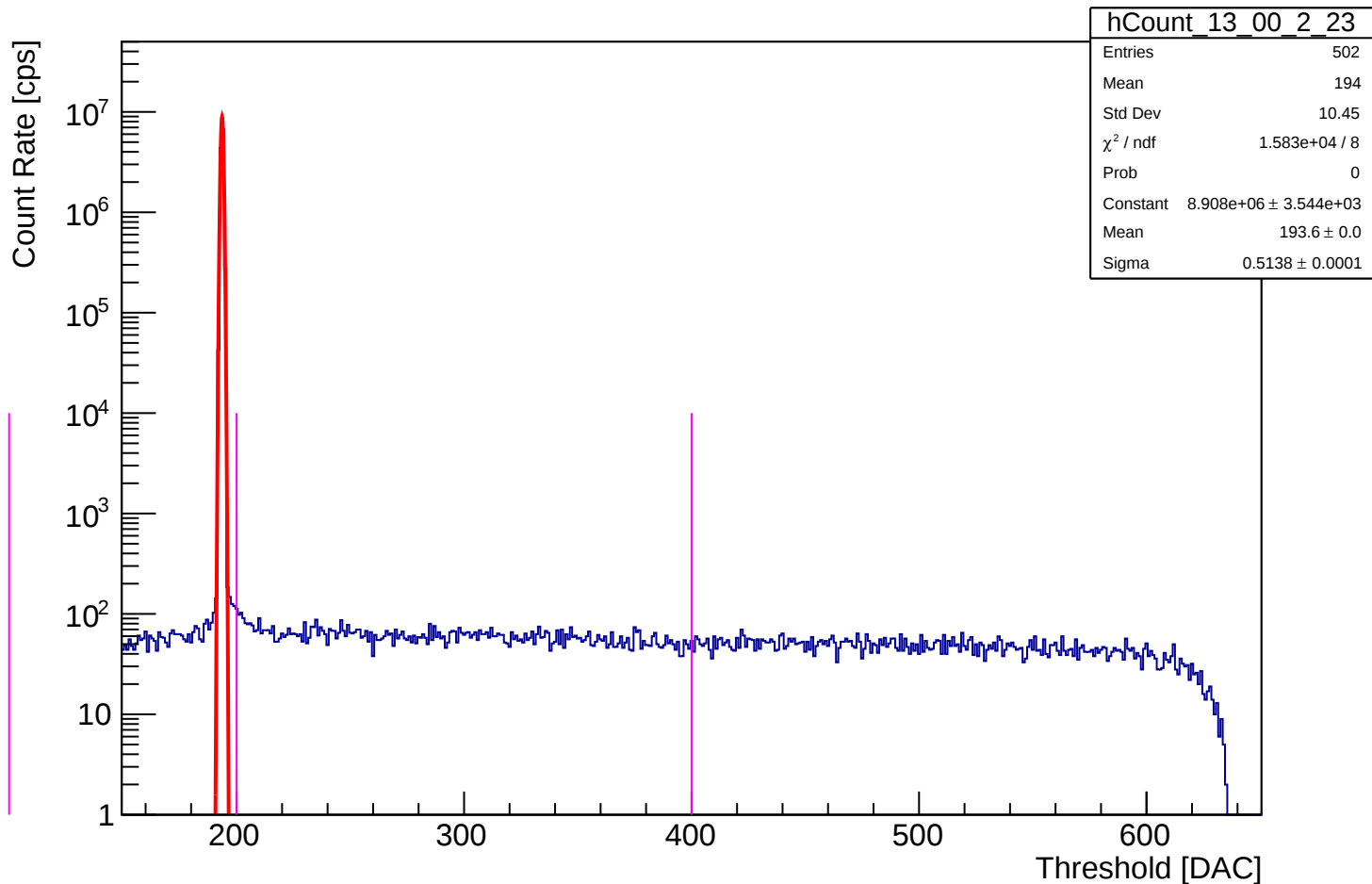
Row 1 Tile 1 Pmt 3 Pixel 15 Slot 13 Fiber 0 Asic 2 Channel 37



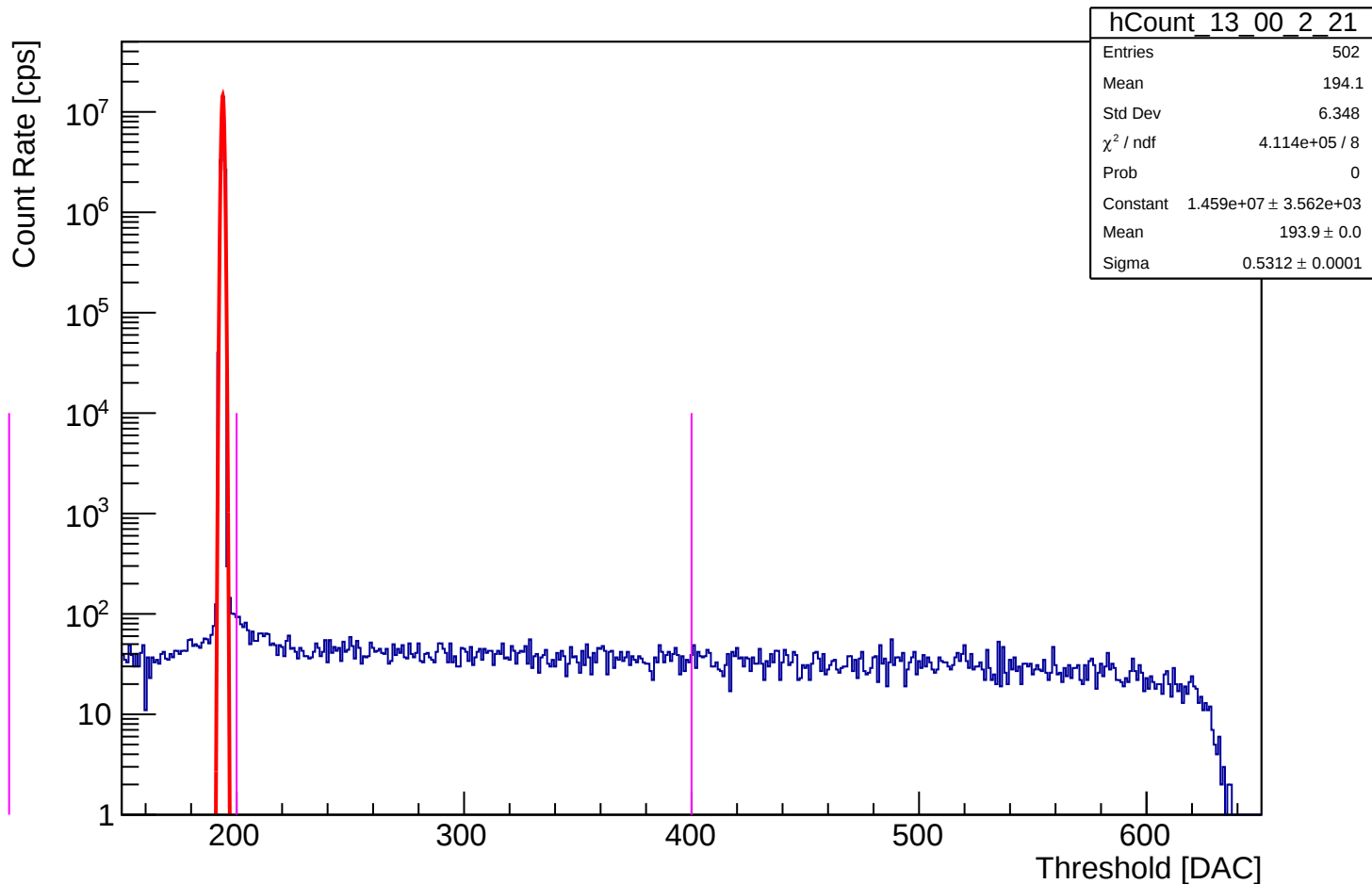
Row 1 Tile 1 Pmt 3 Pixel 16 Slot 13 Fiber 0 Asic 2 Channel 39



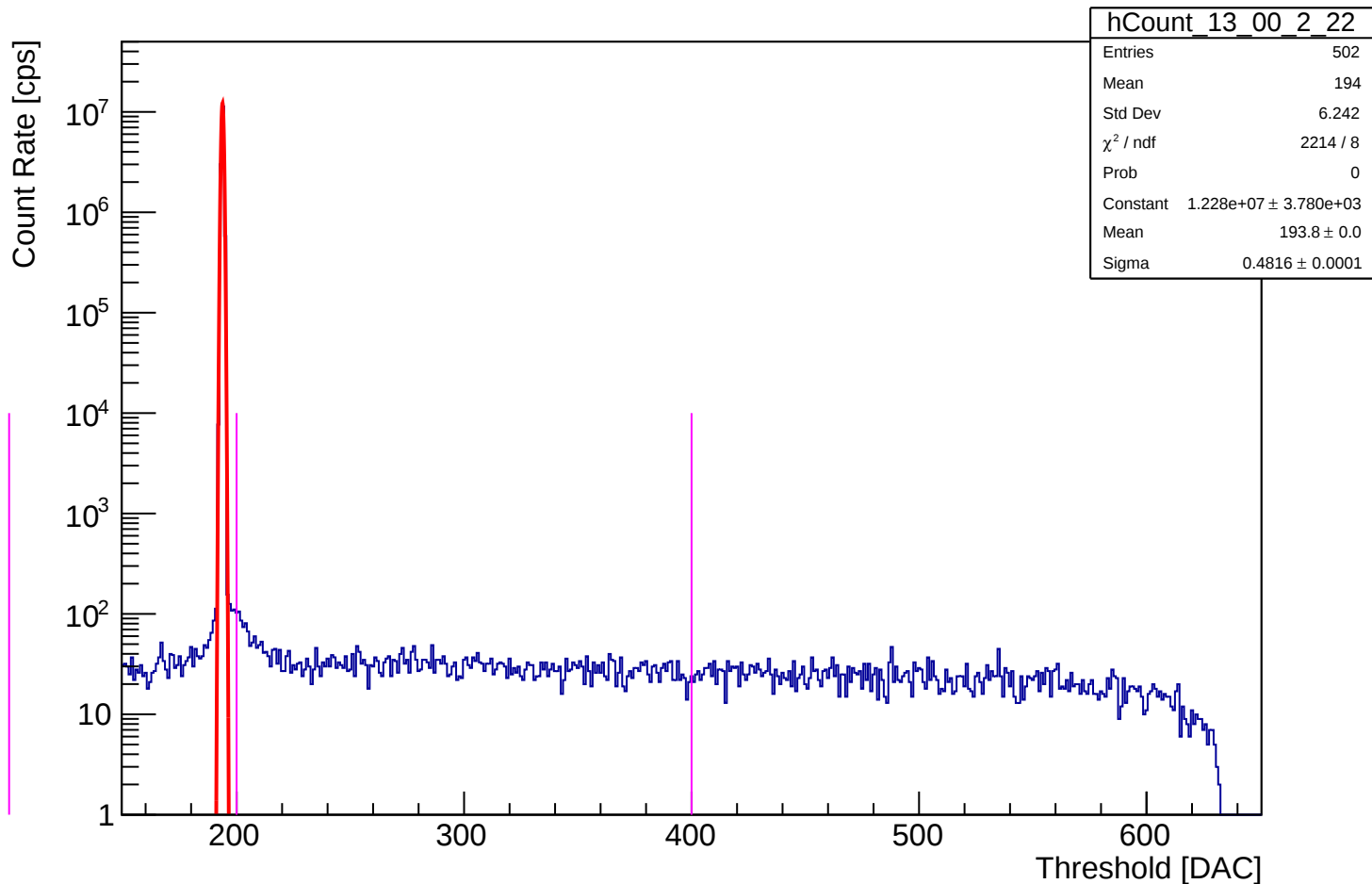
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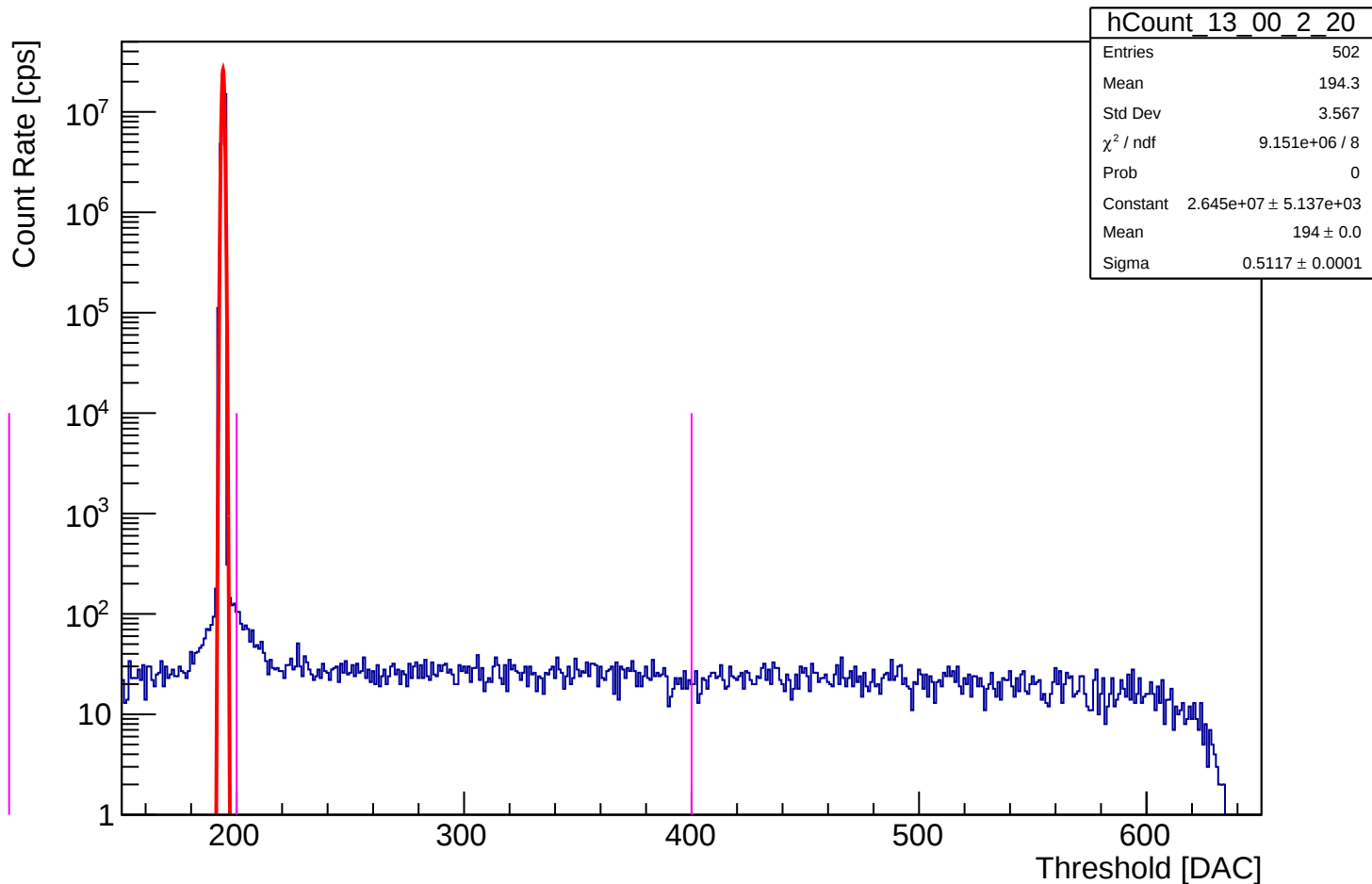
Row 1 Tile 1 Pmt 3 Pixel 18 Slot 13 Fiber 0 Asic 2 Channel 21



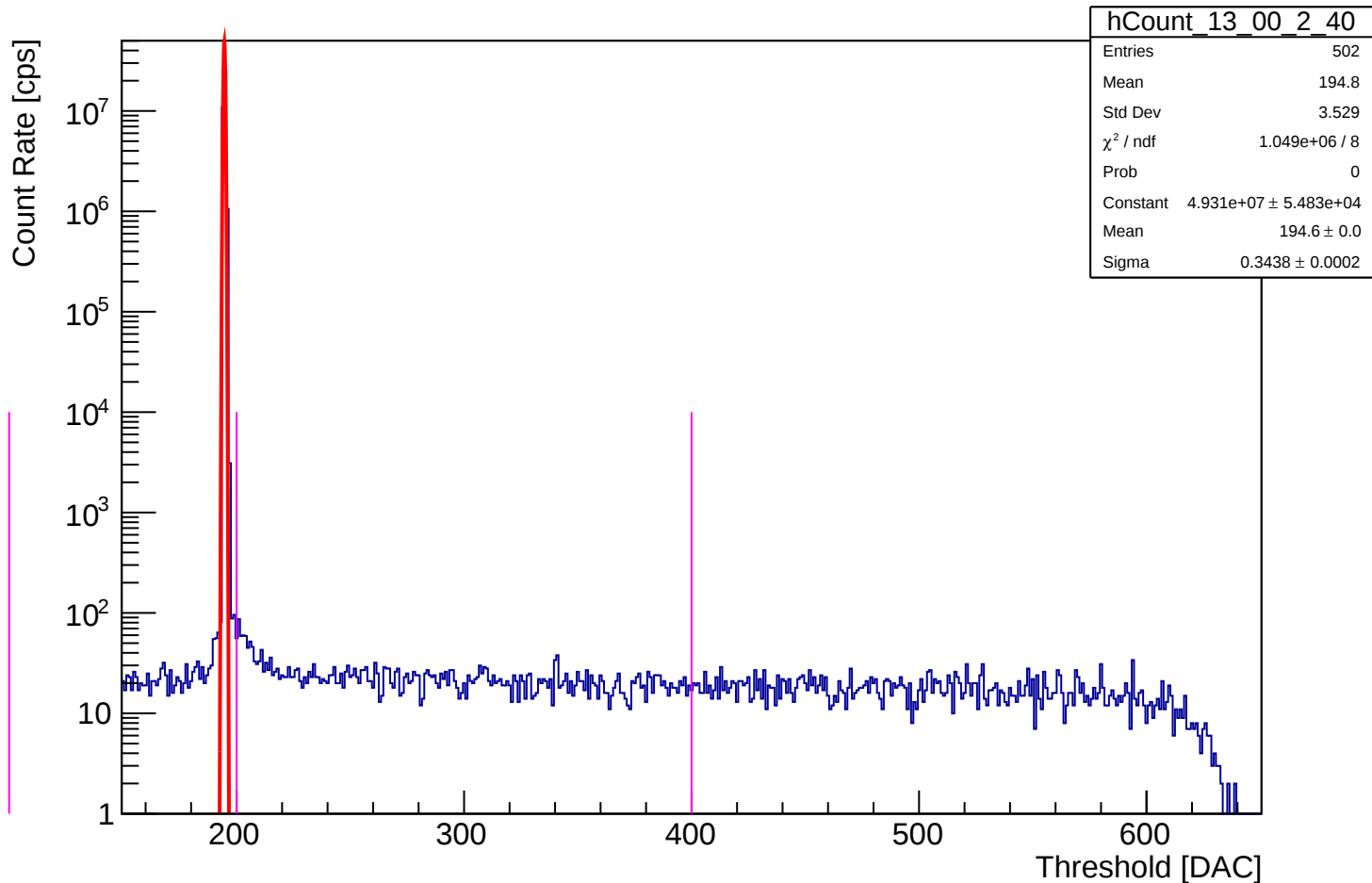
Row 1 Tile 1 Pmt 3 Pixel 19 Slot 13 Fiber 0 Asic 2 Channel 22



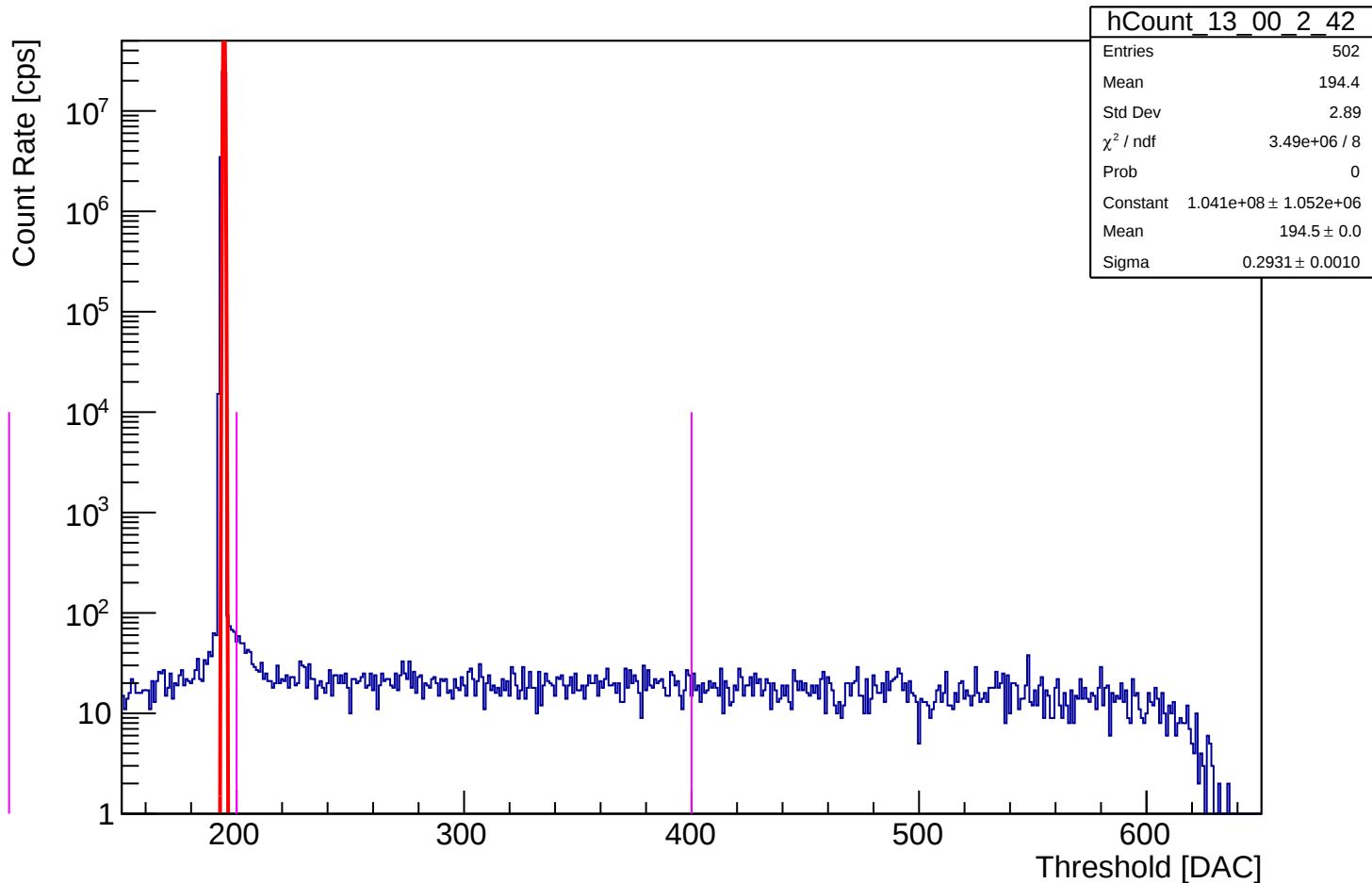
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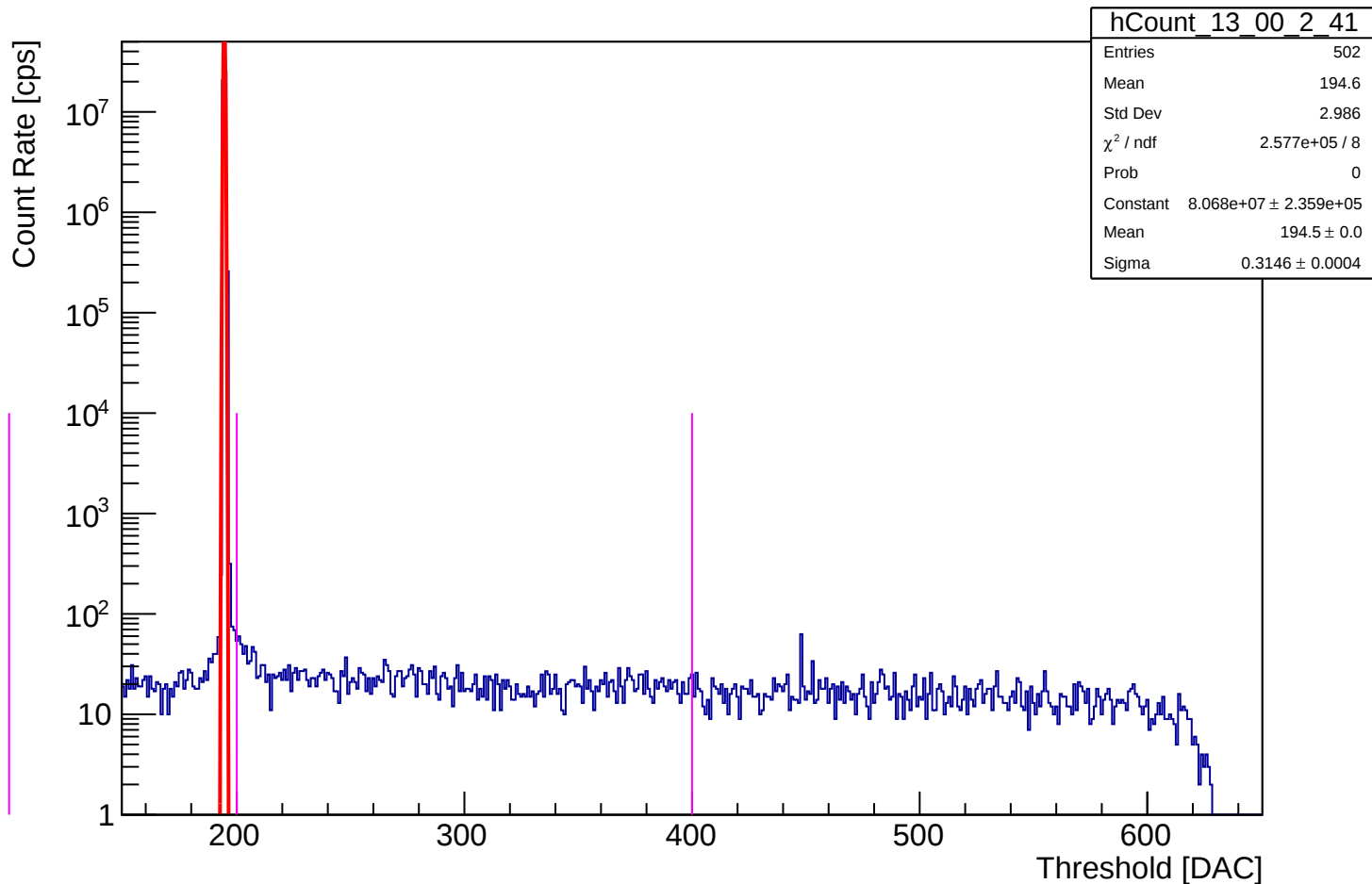
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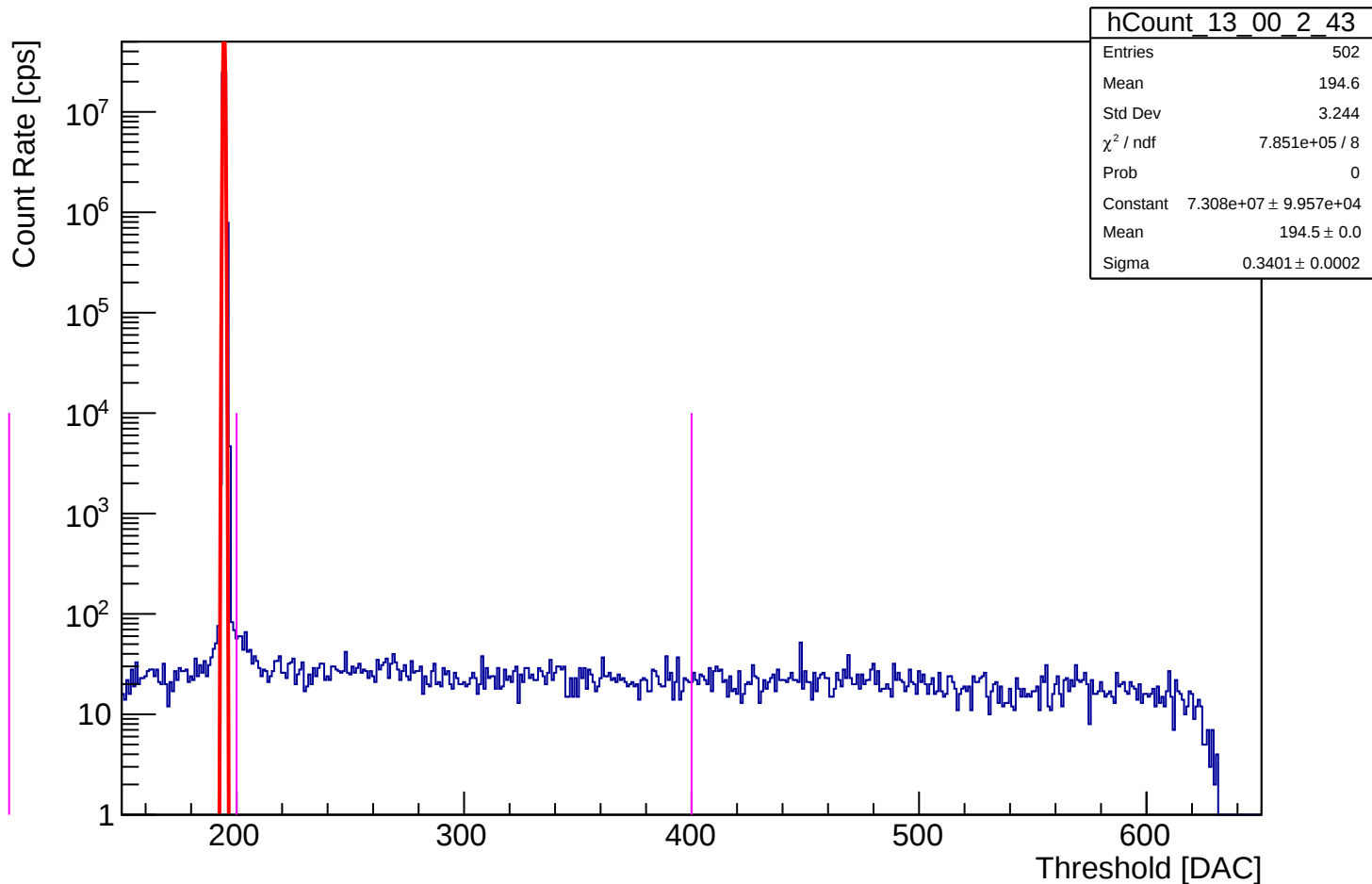
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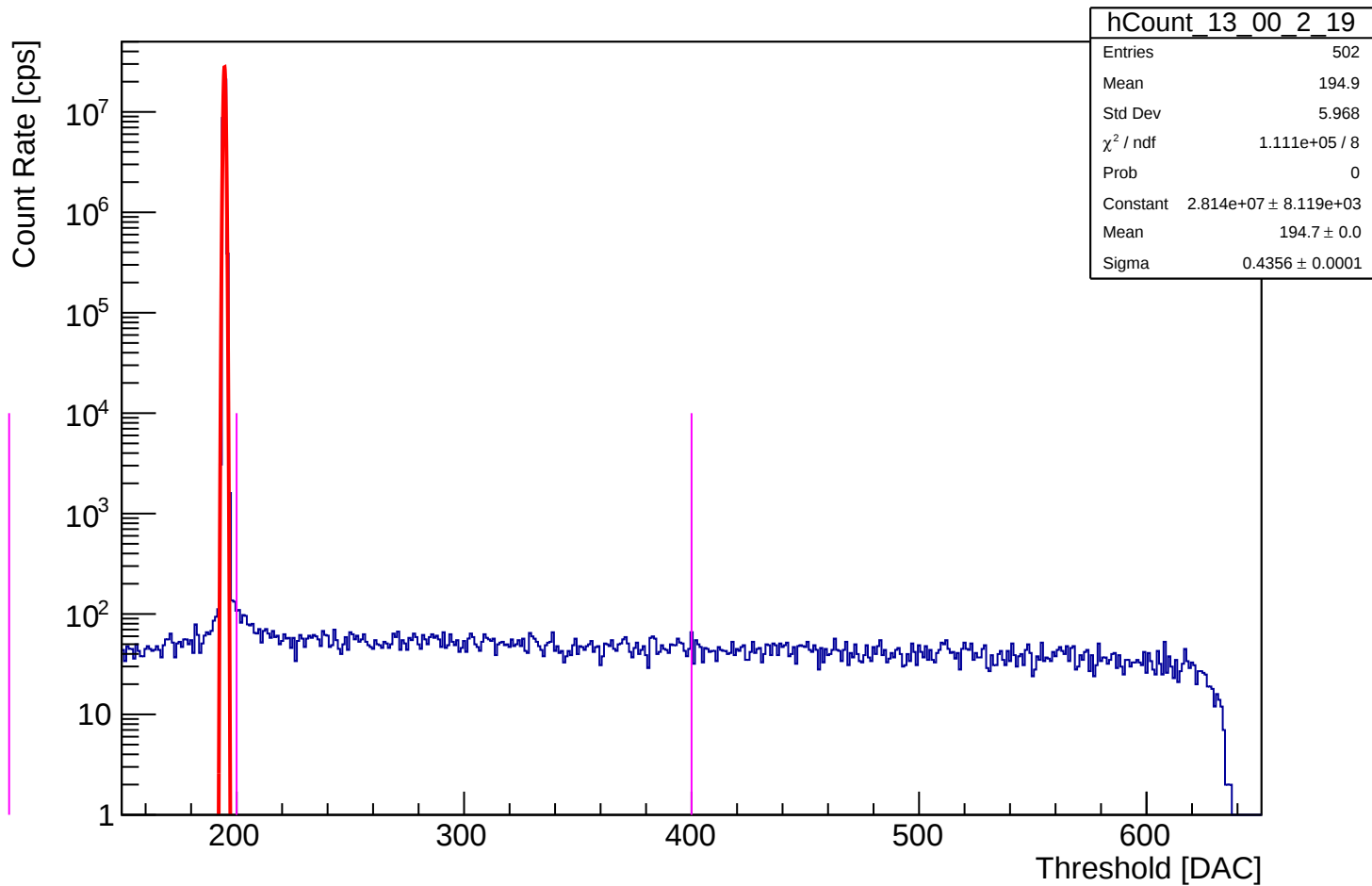
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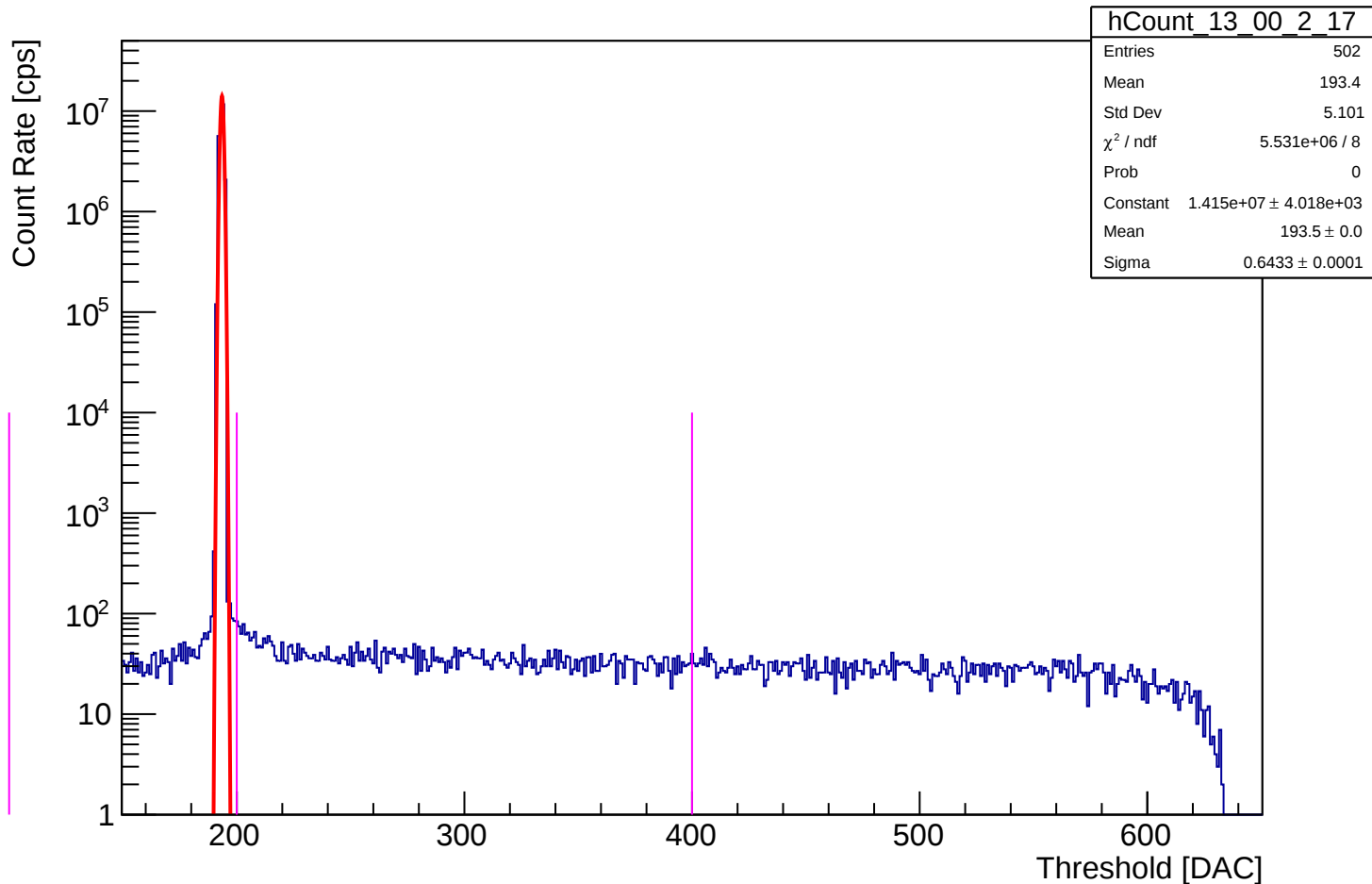
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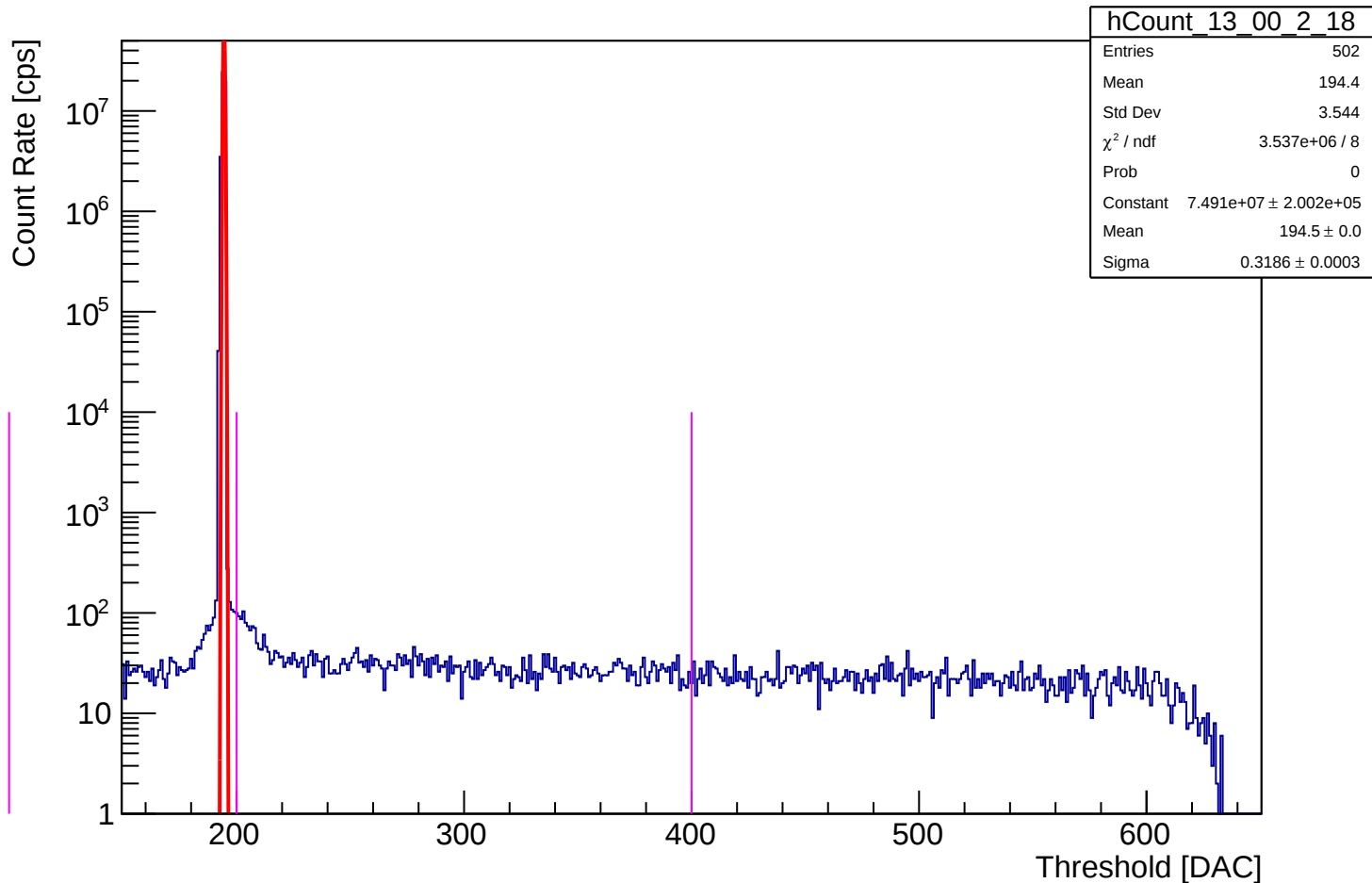
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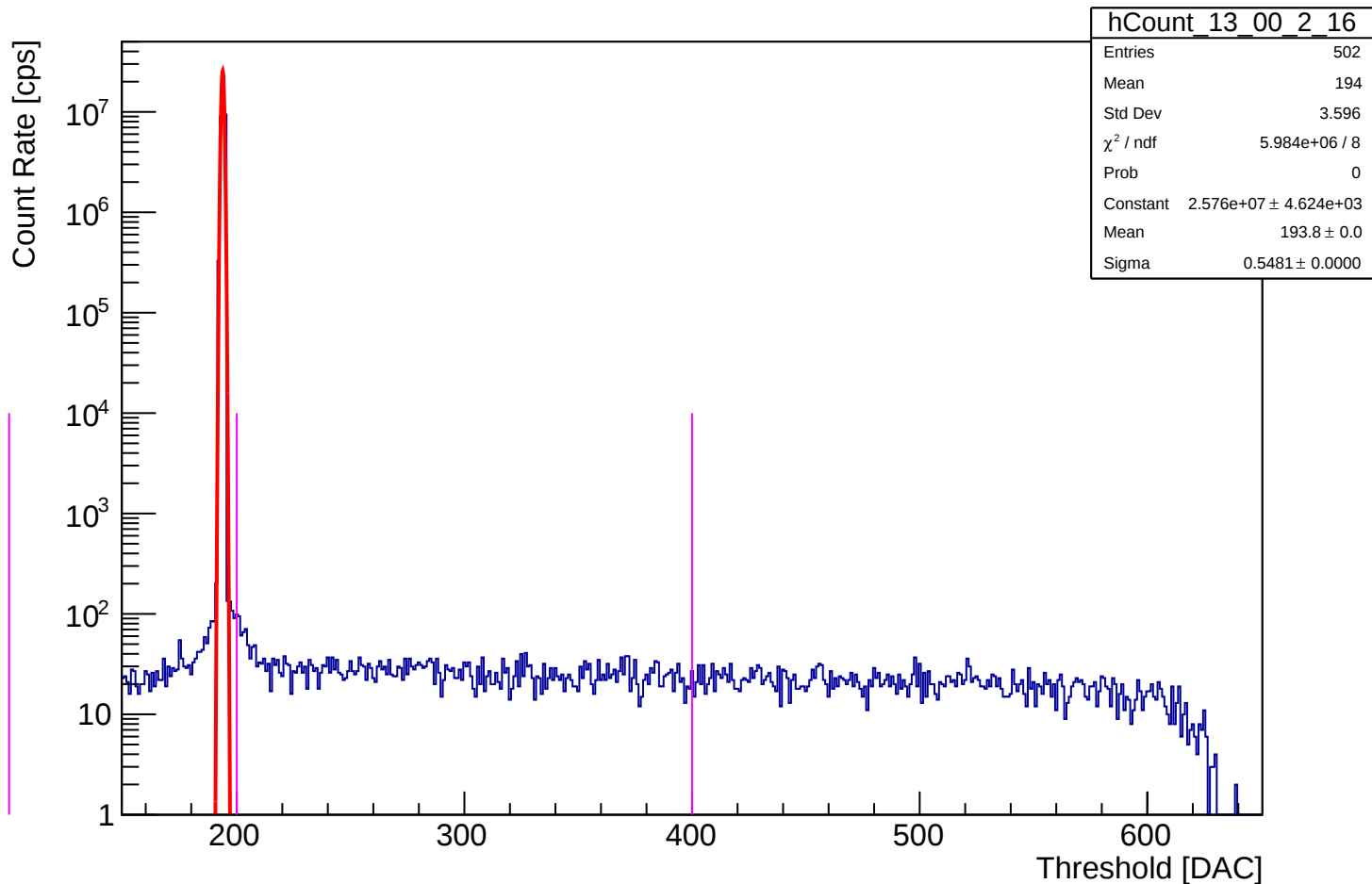
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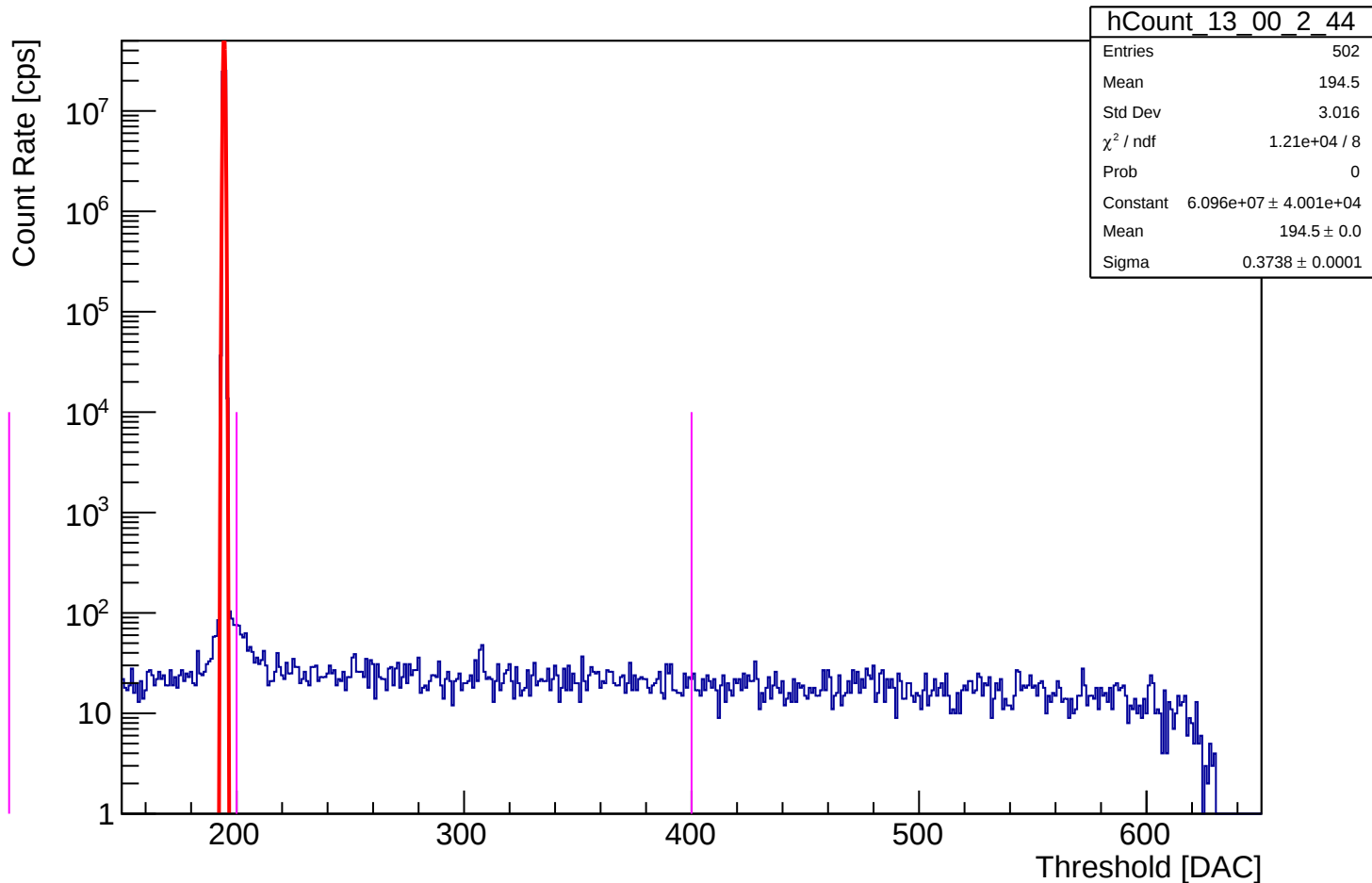
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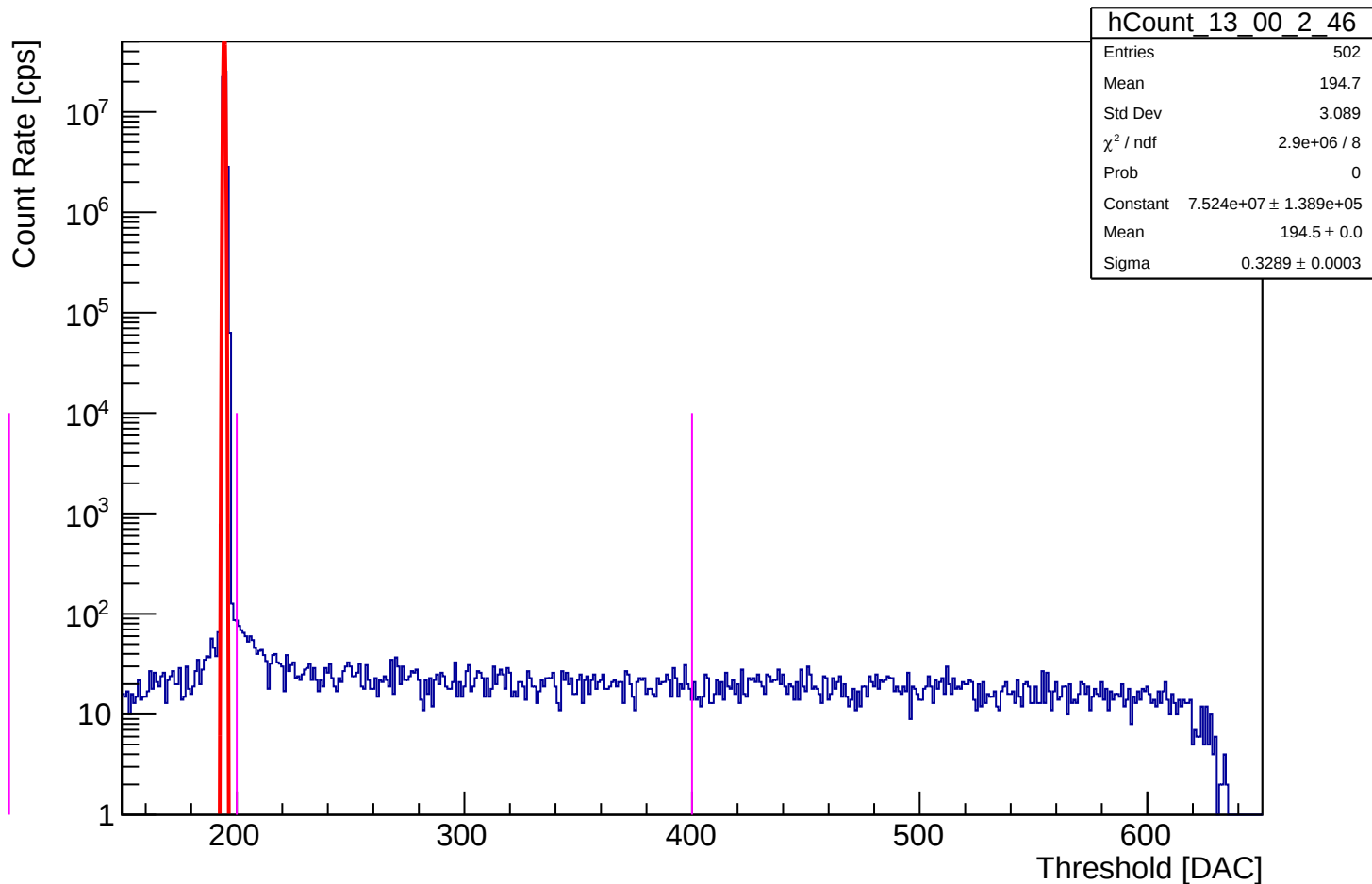
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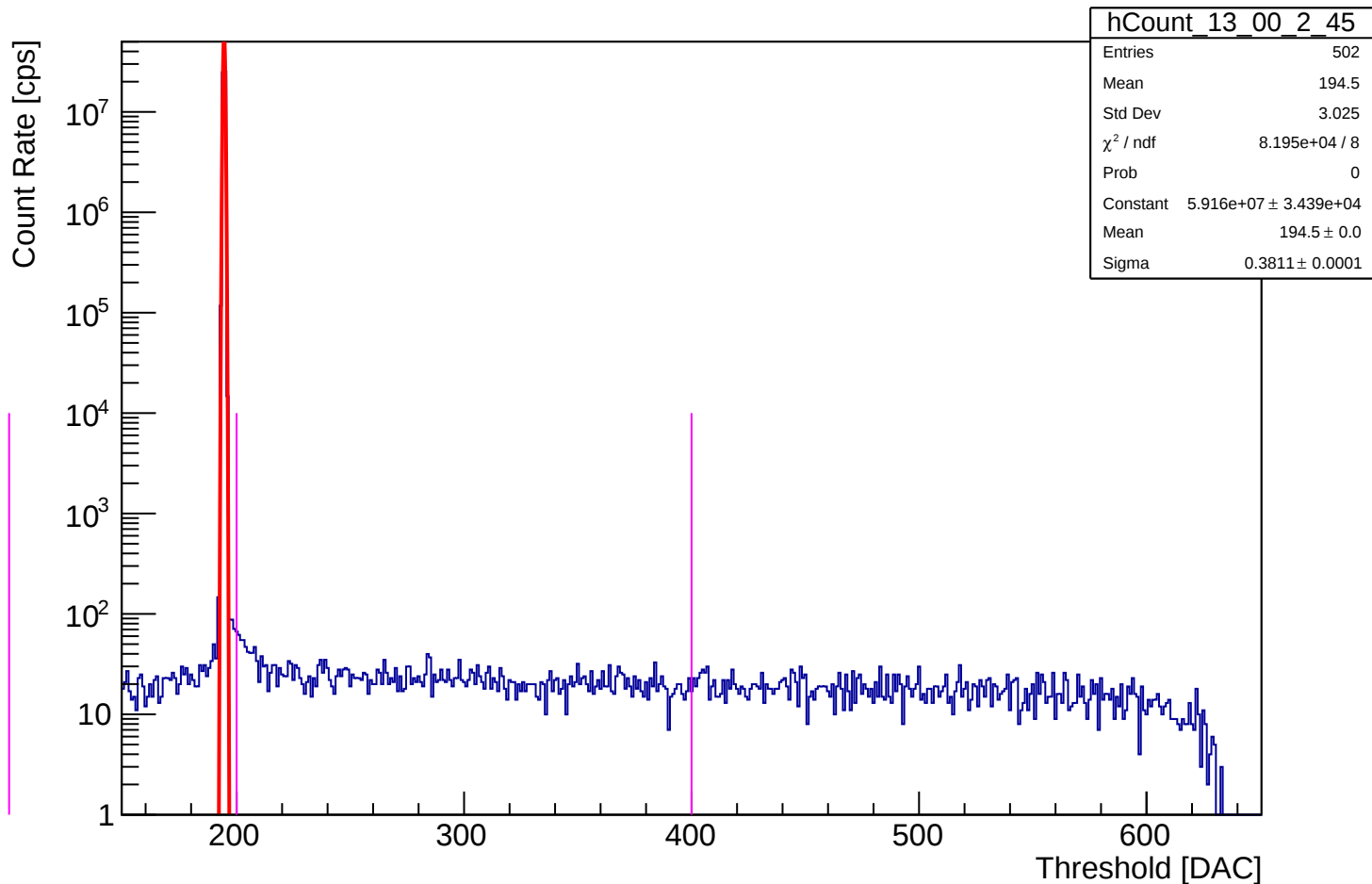
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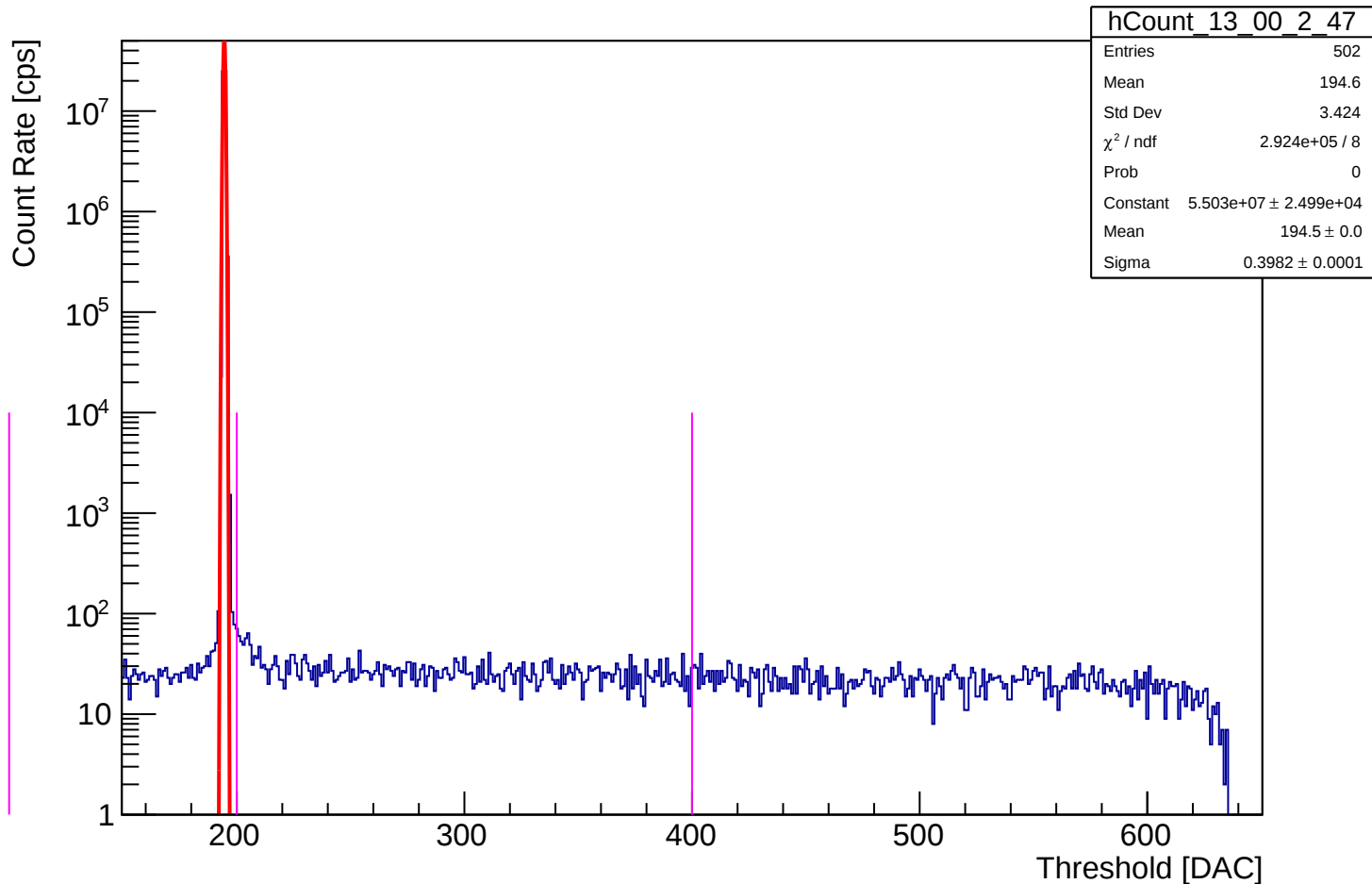
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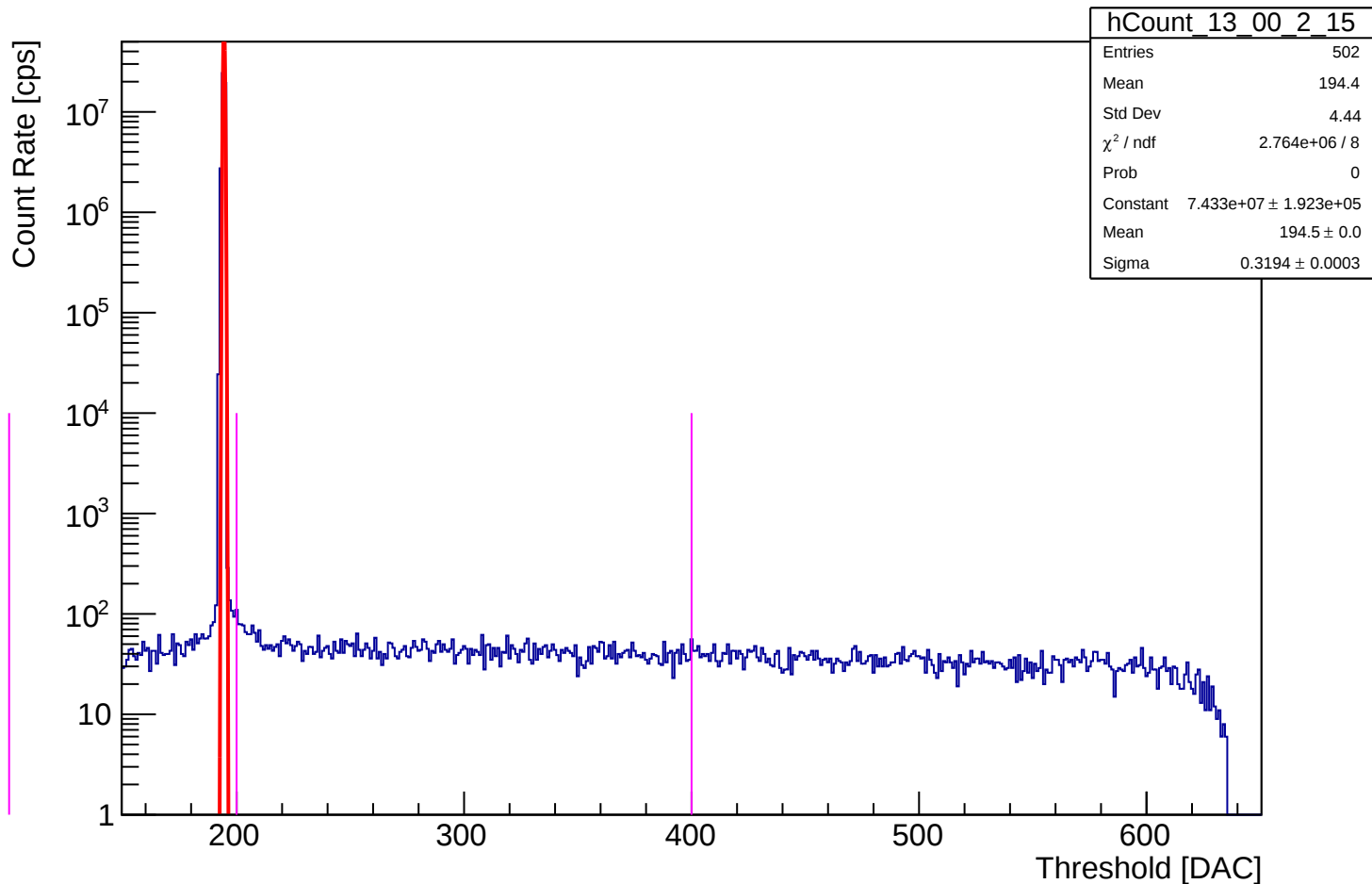
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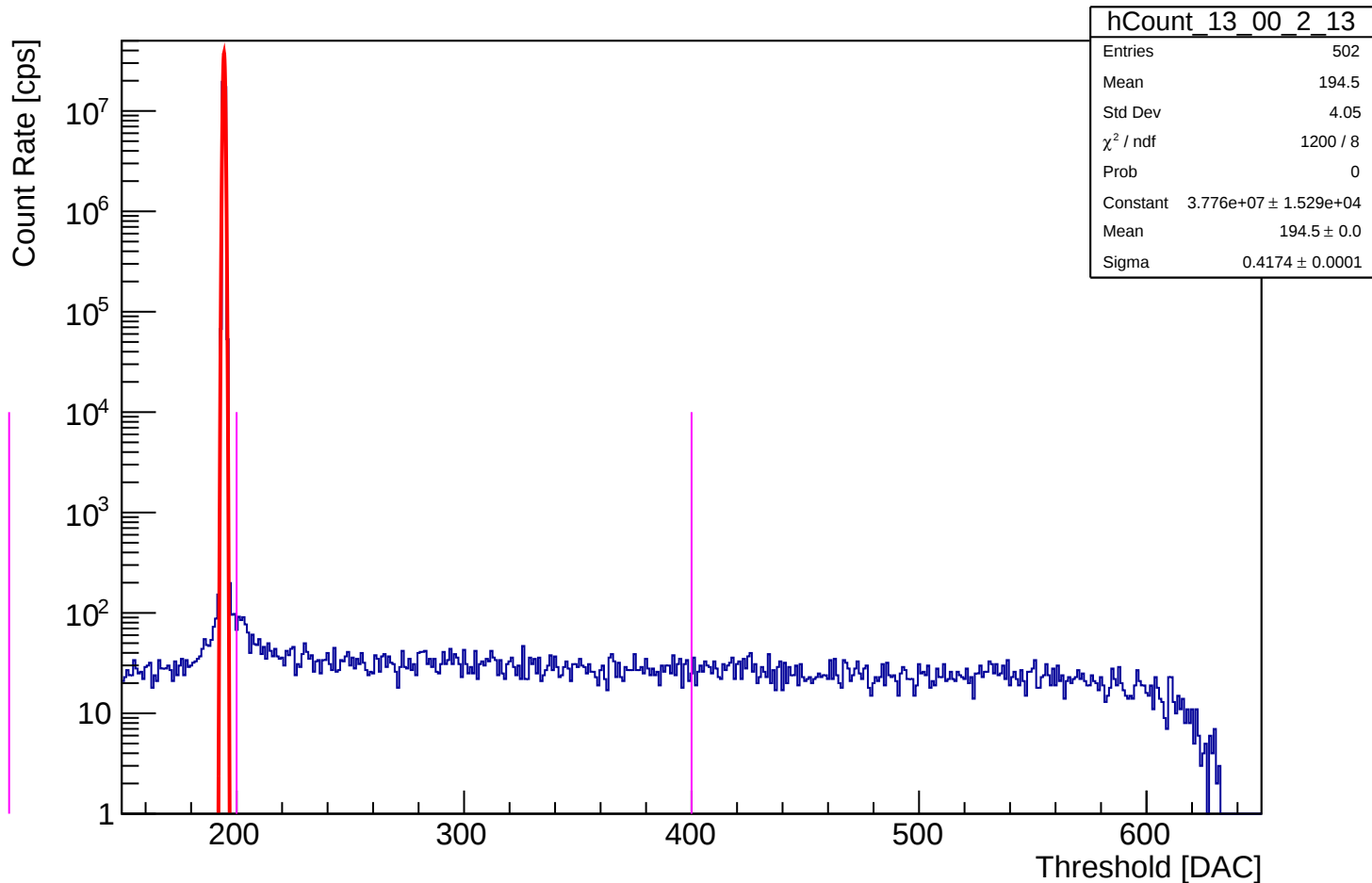
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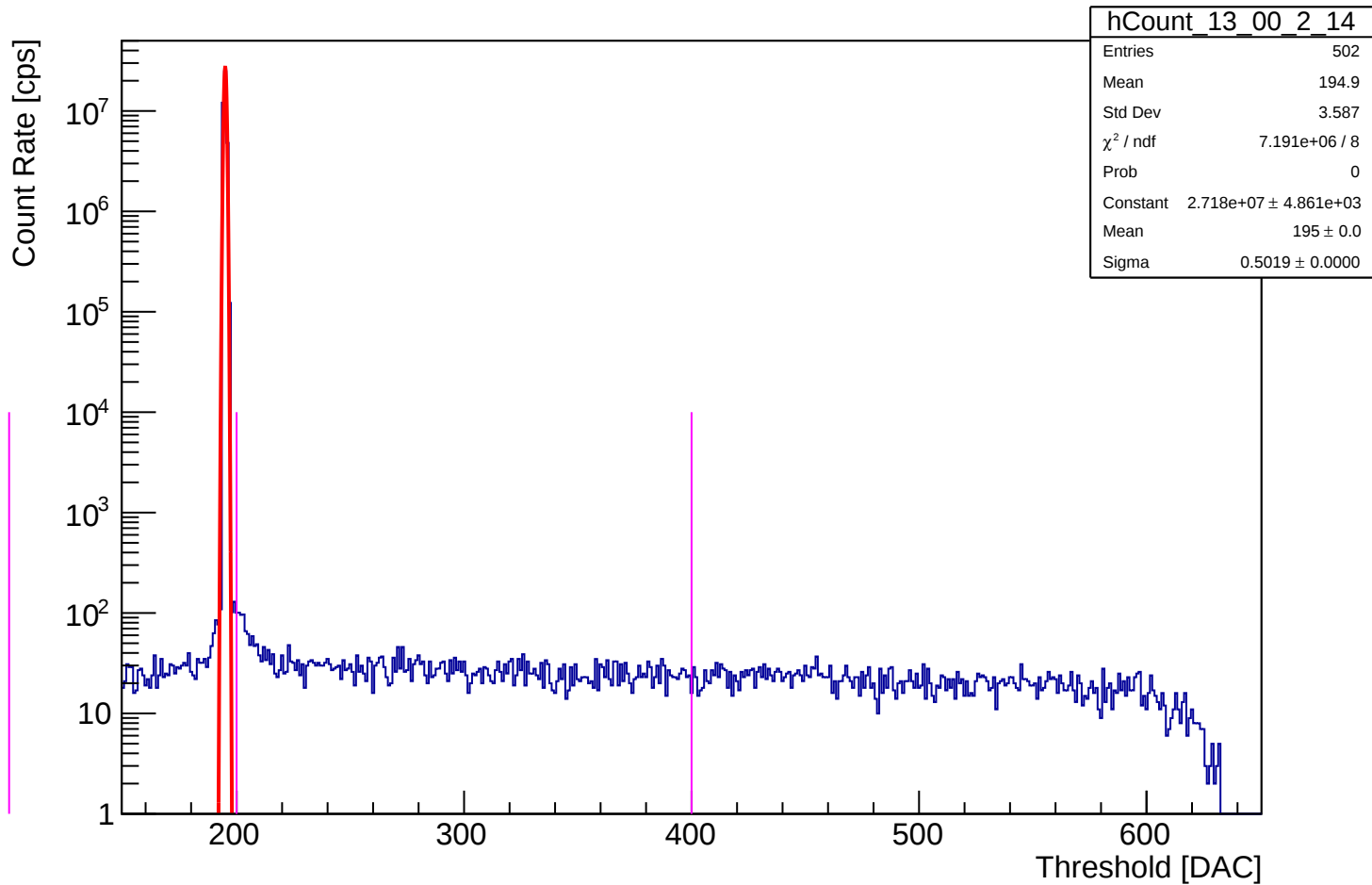
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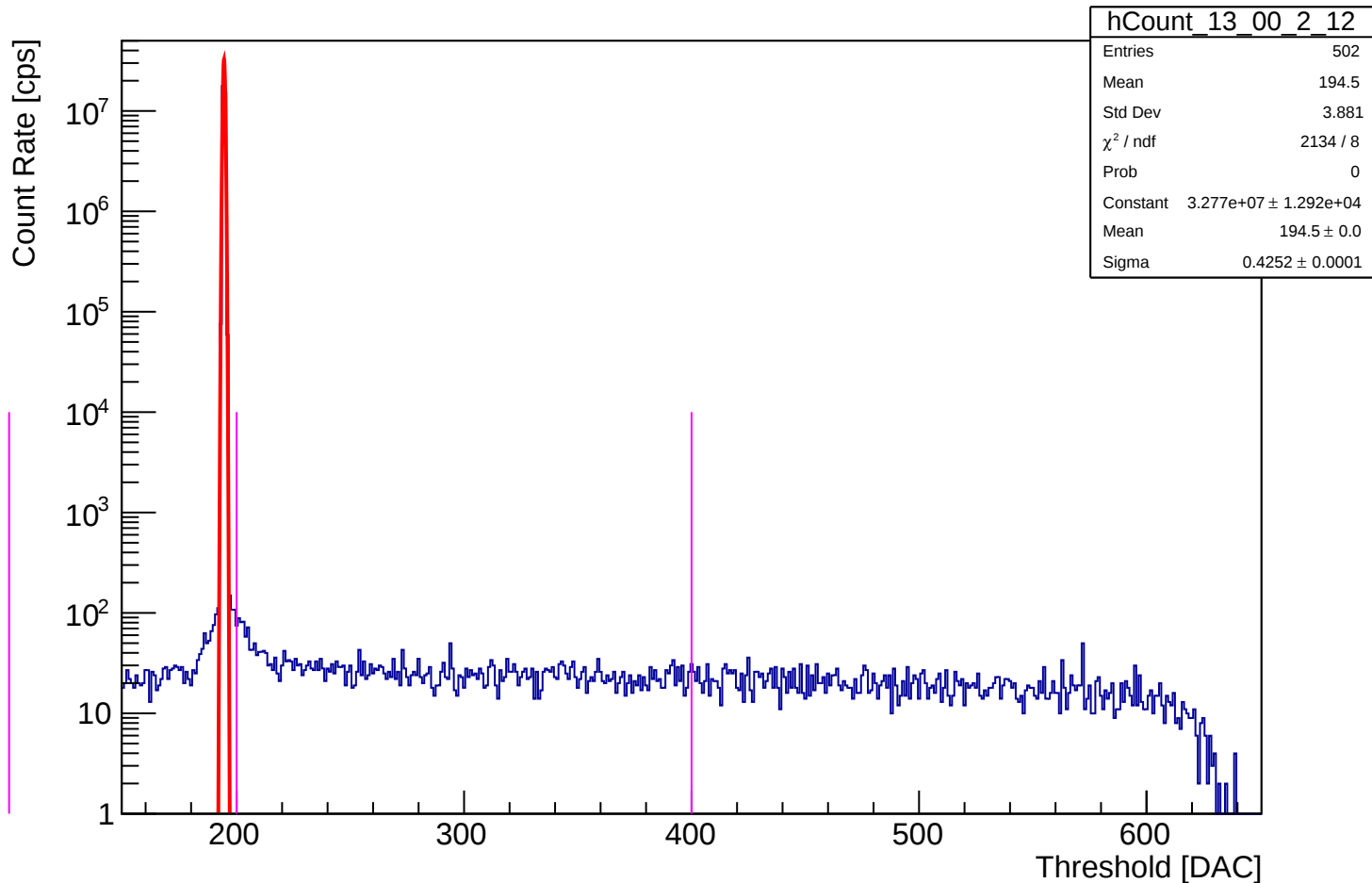
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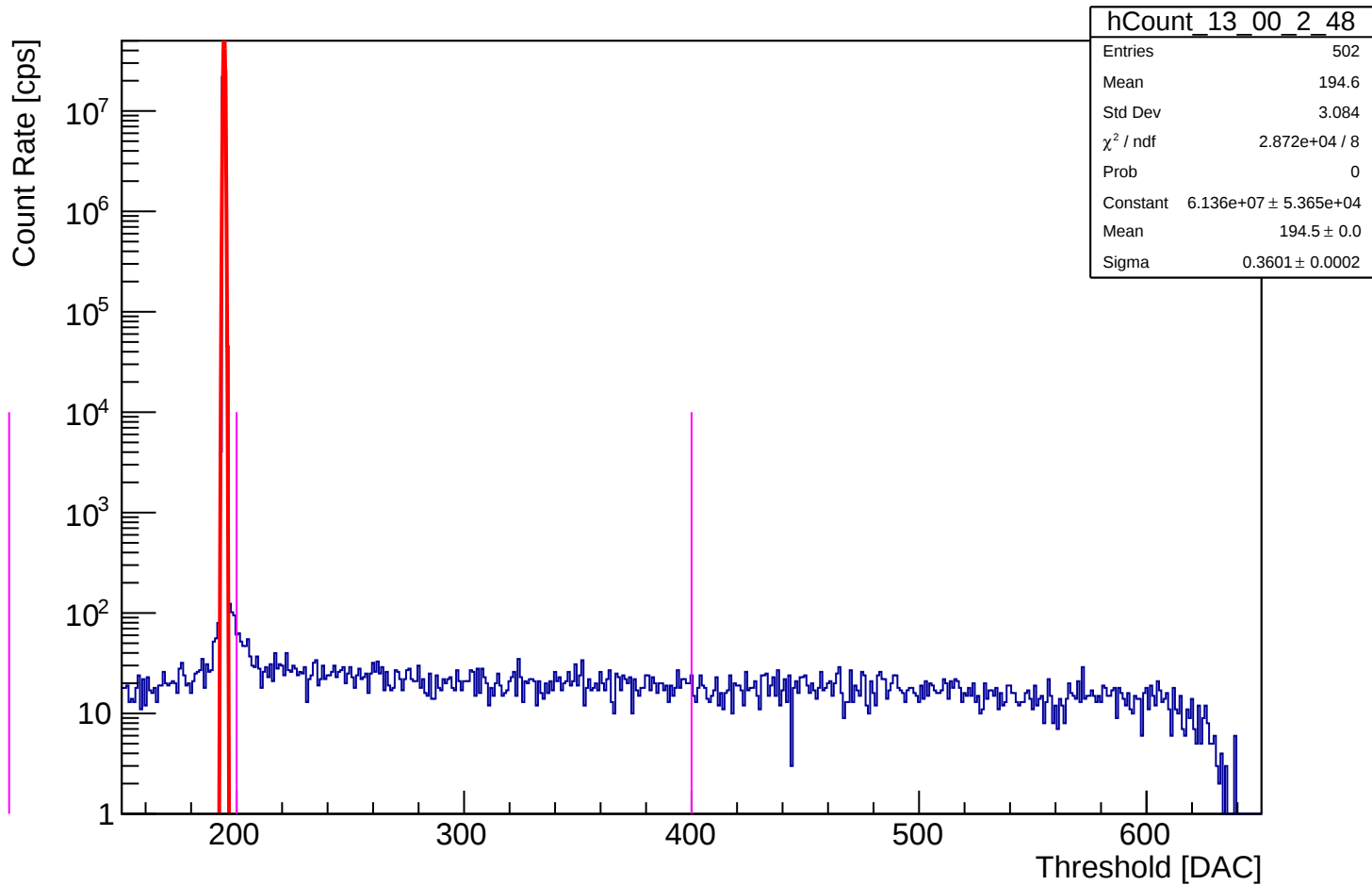
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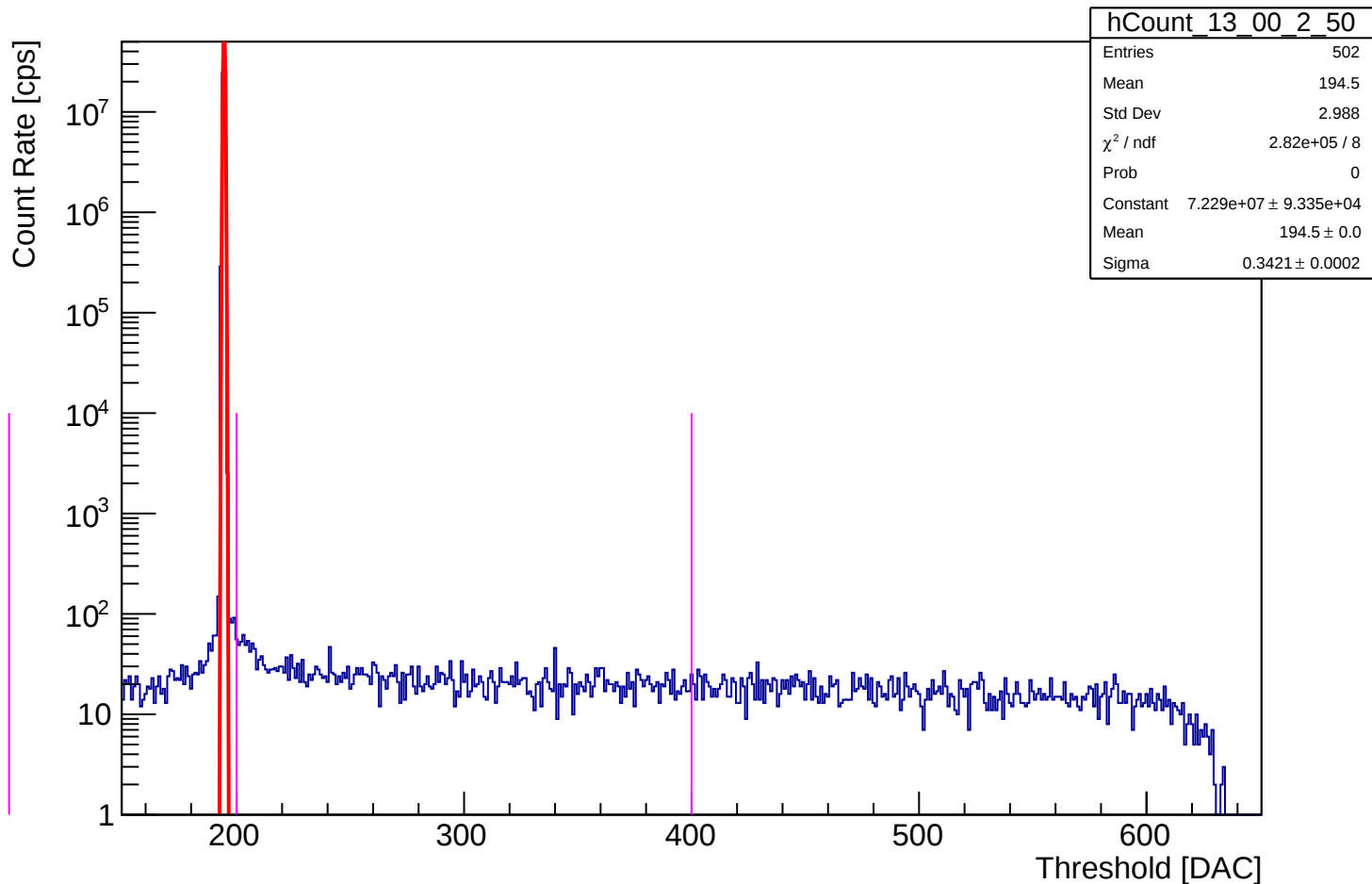
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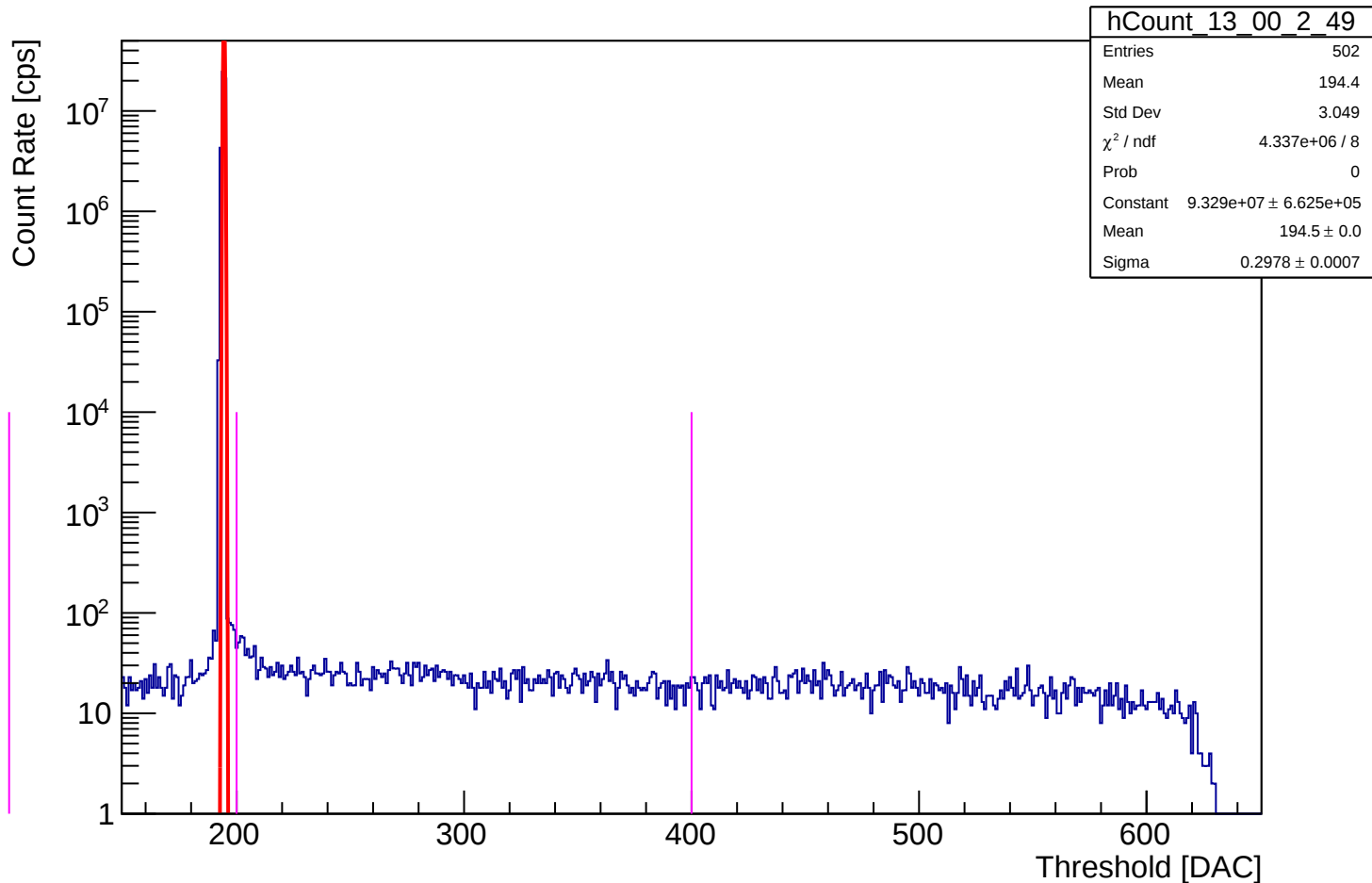
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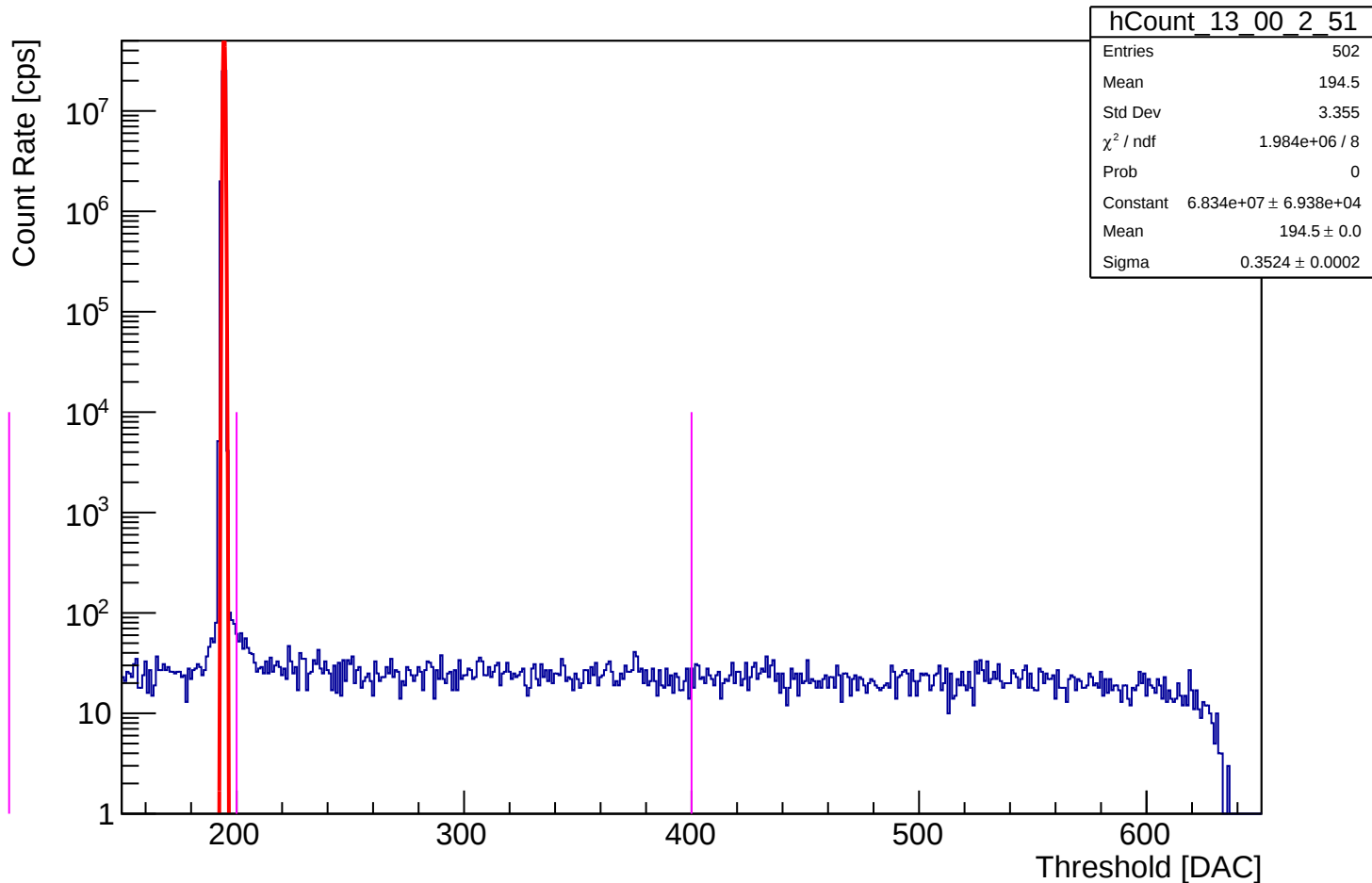
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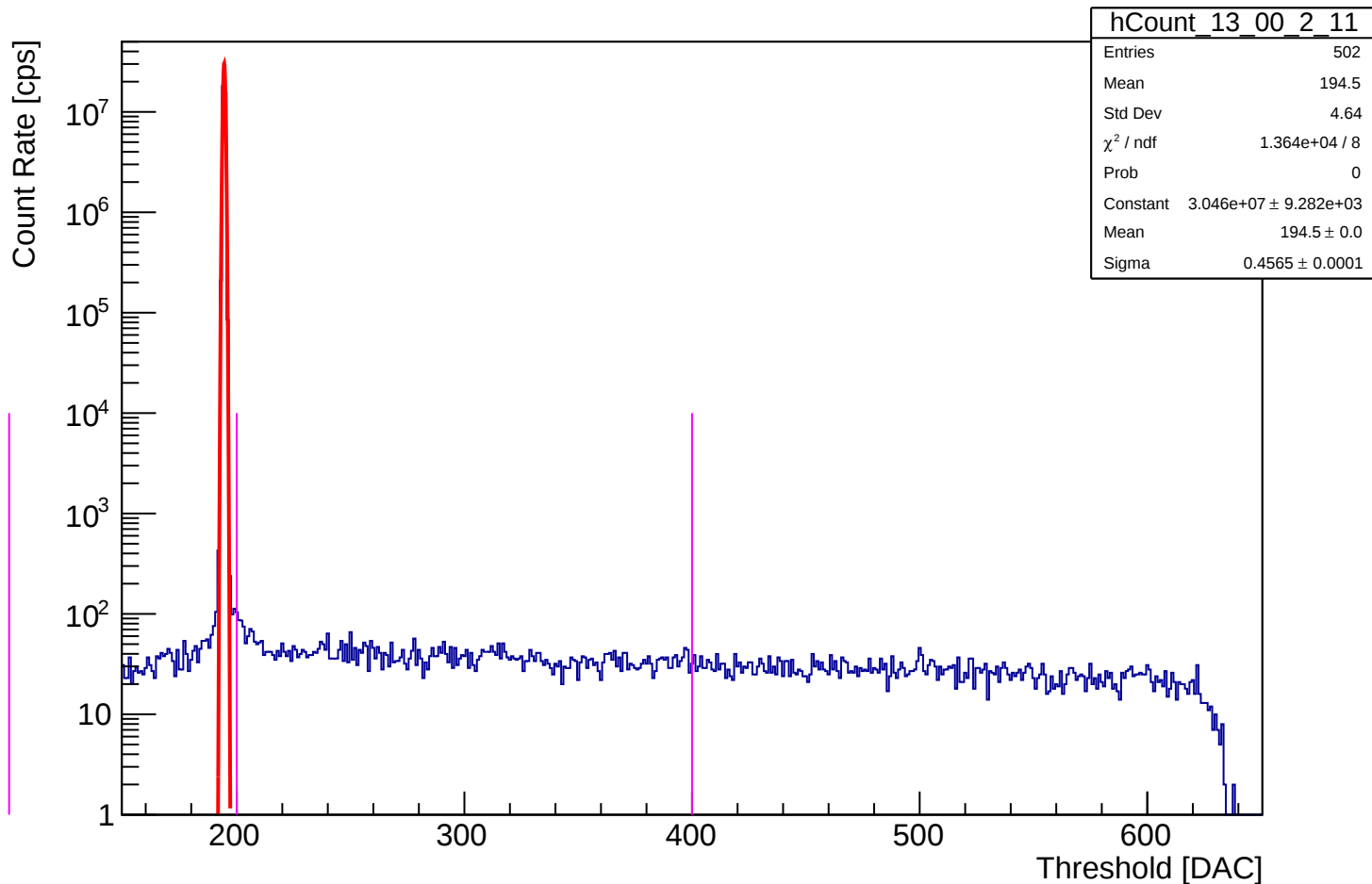
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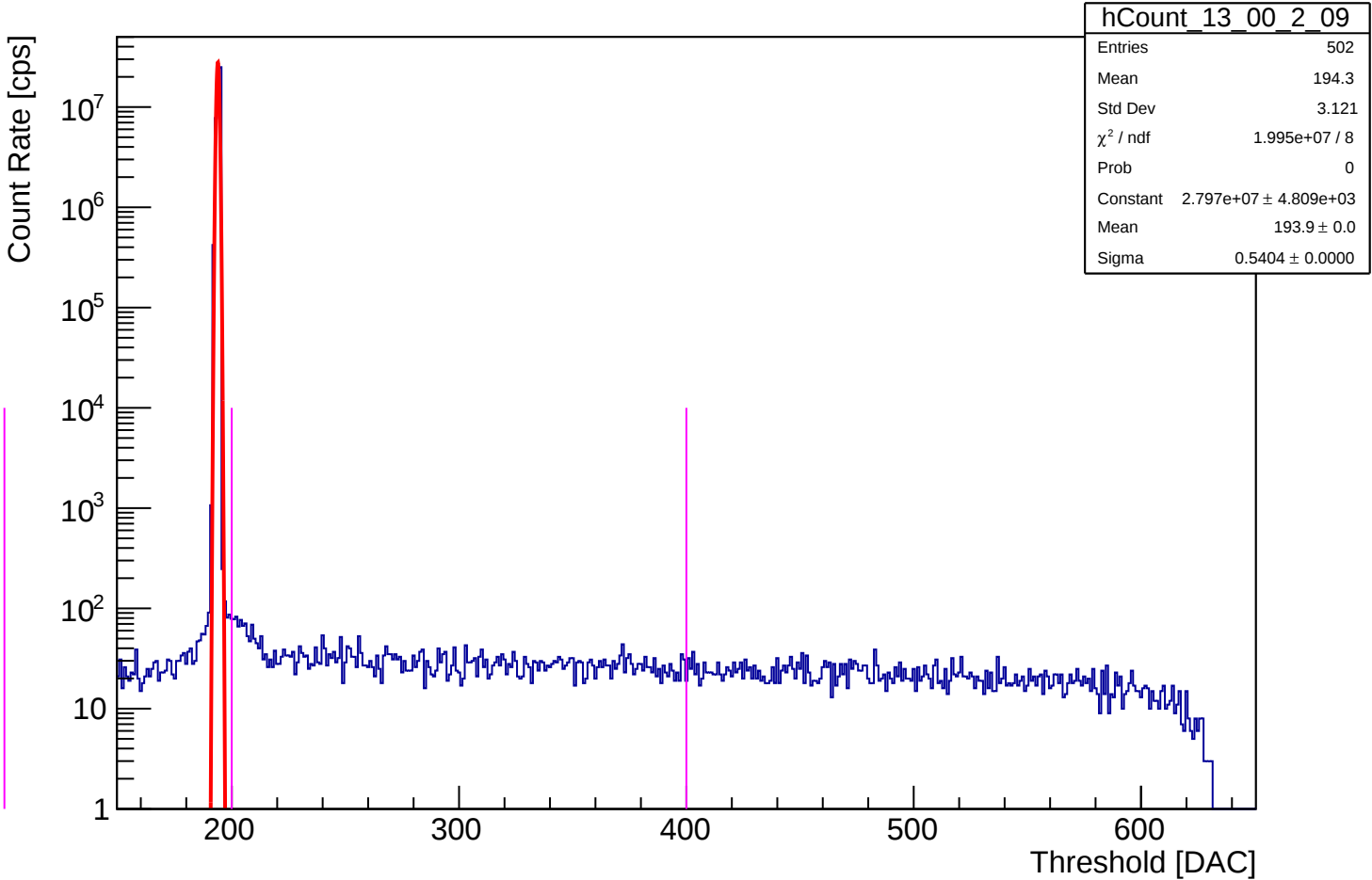


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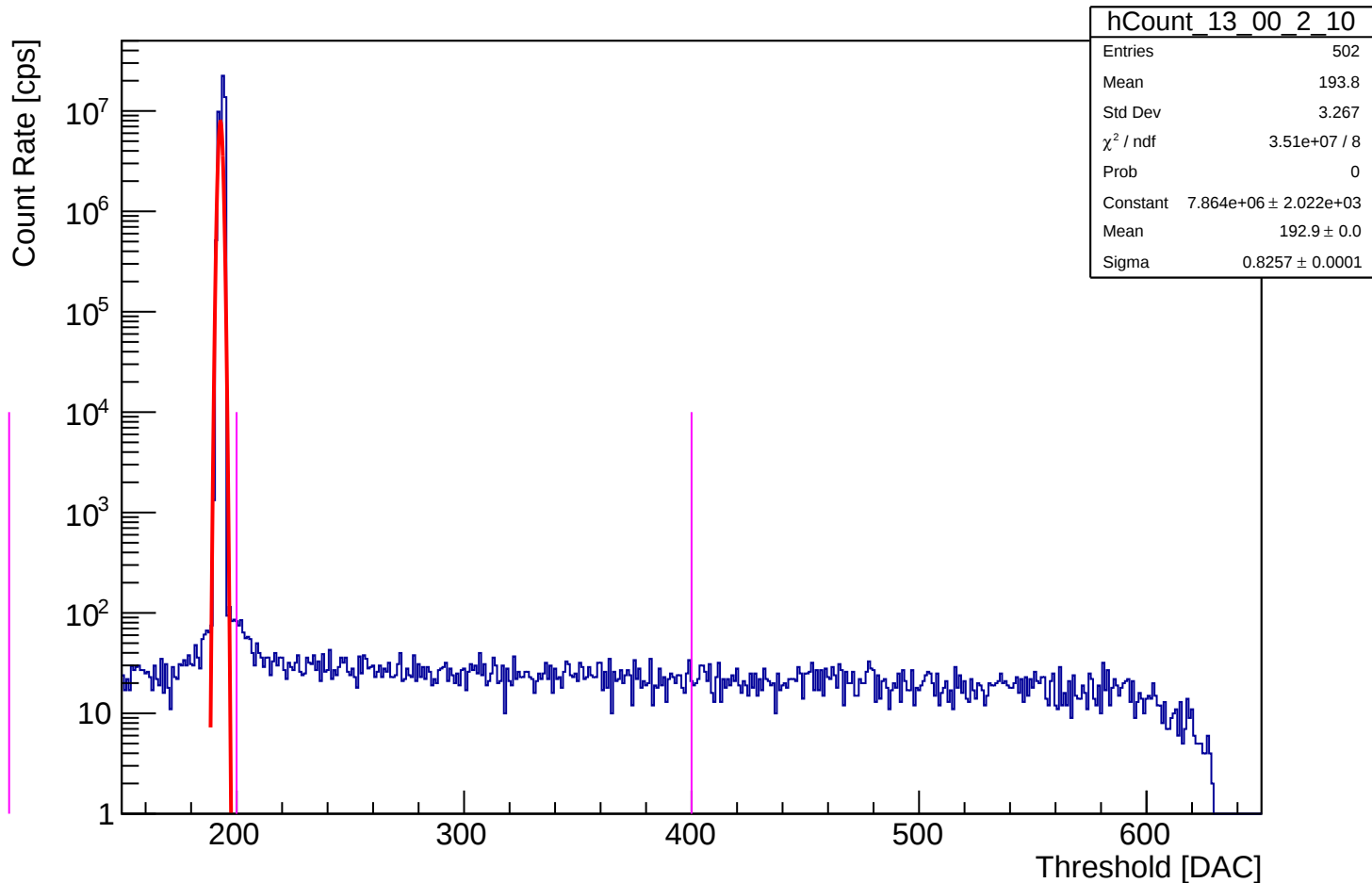


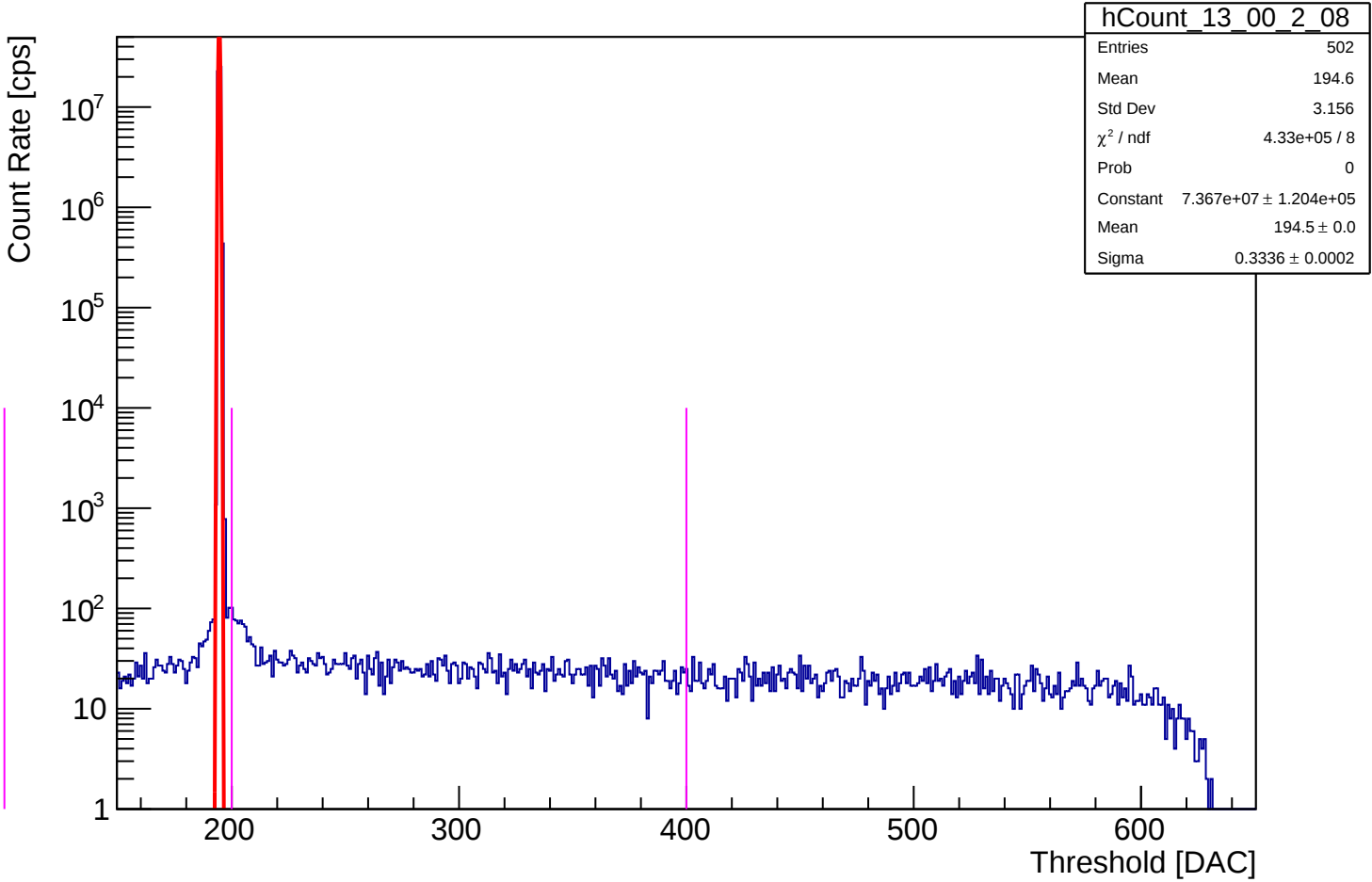
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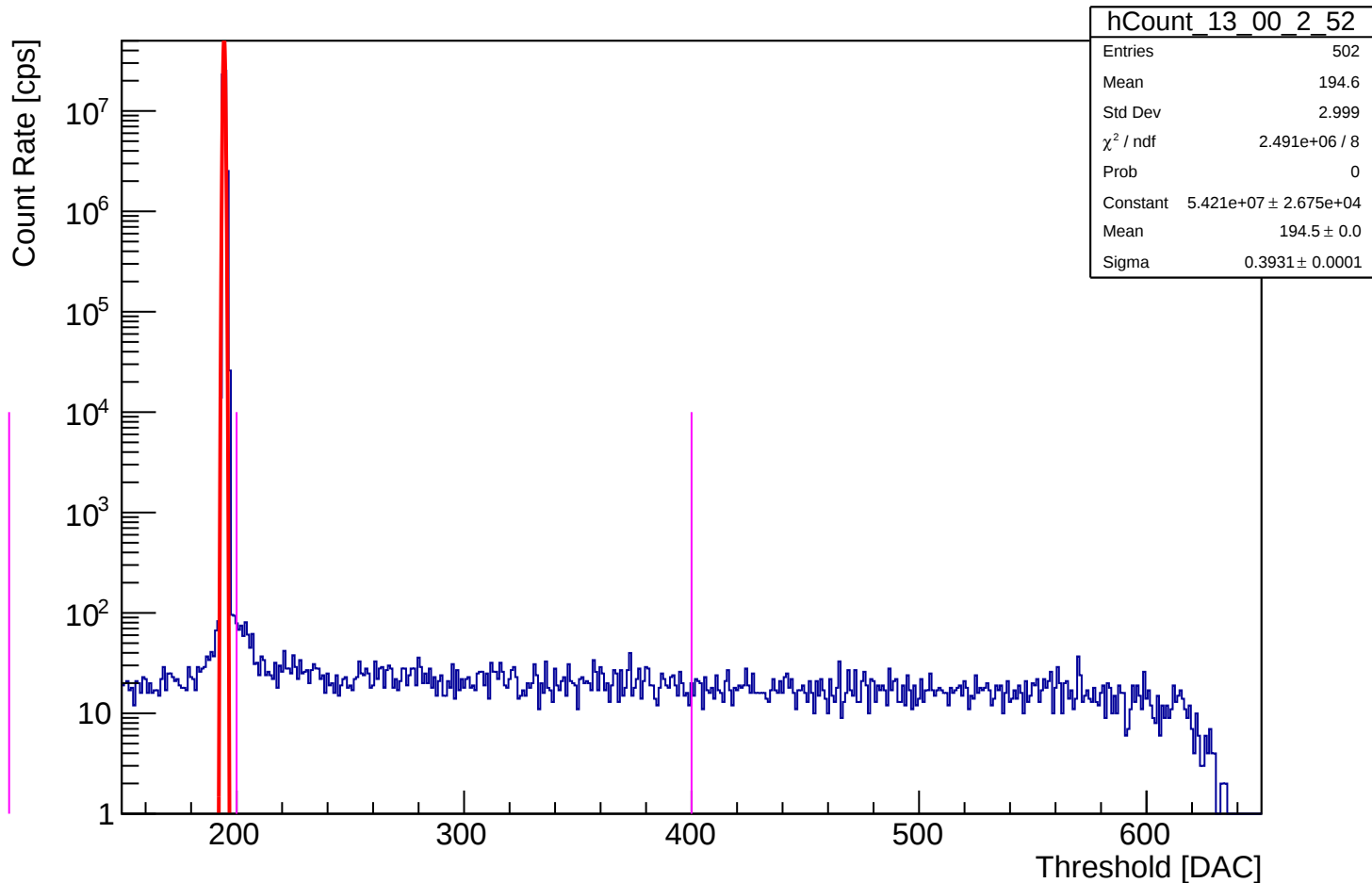


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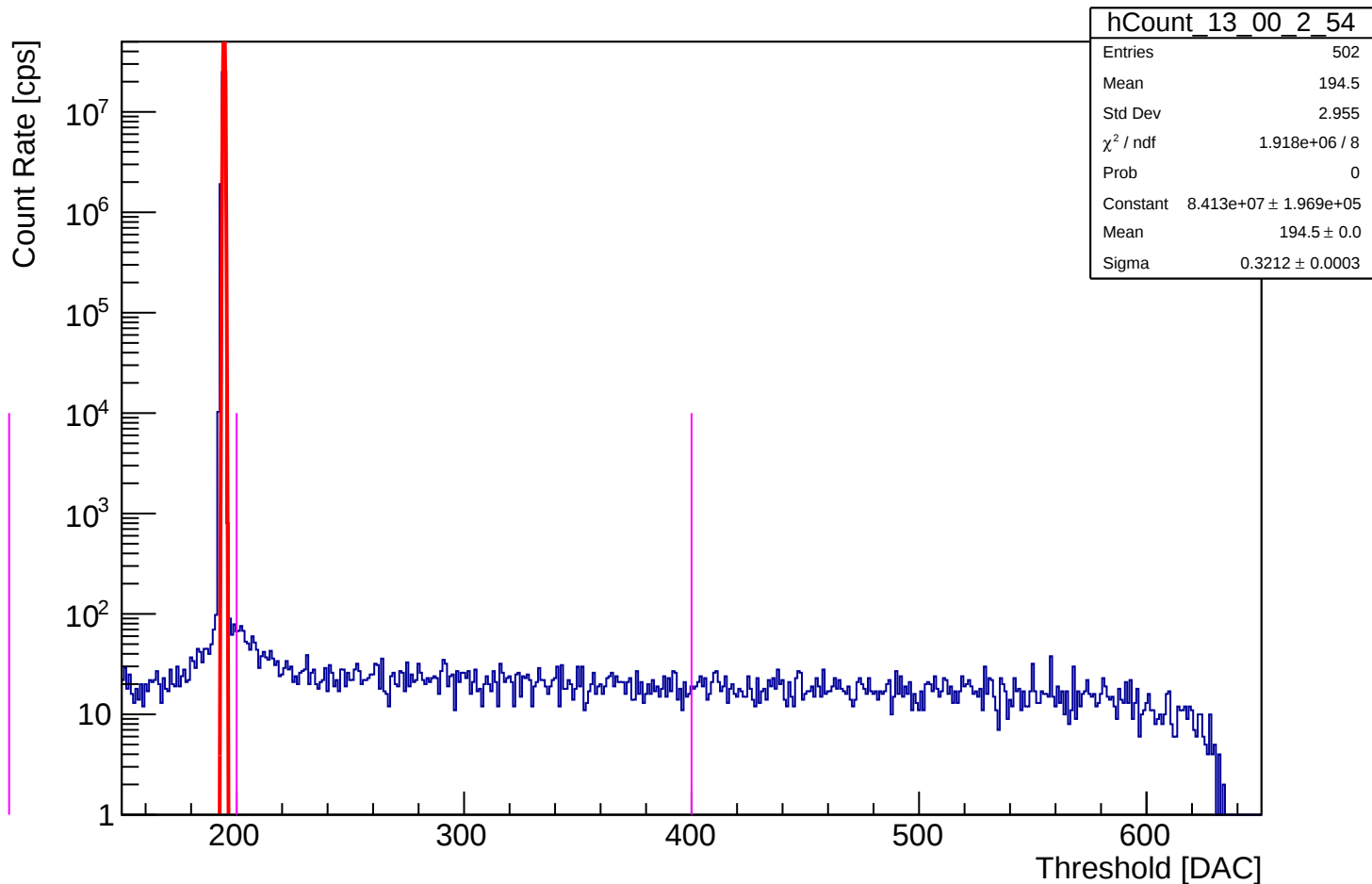




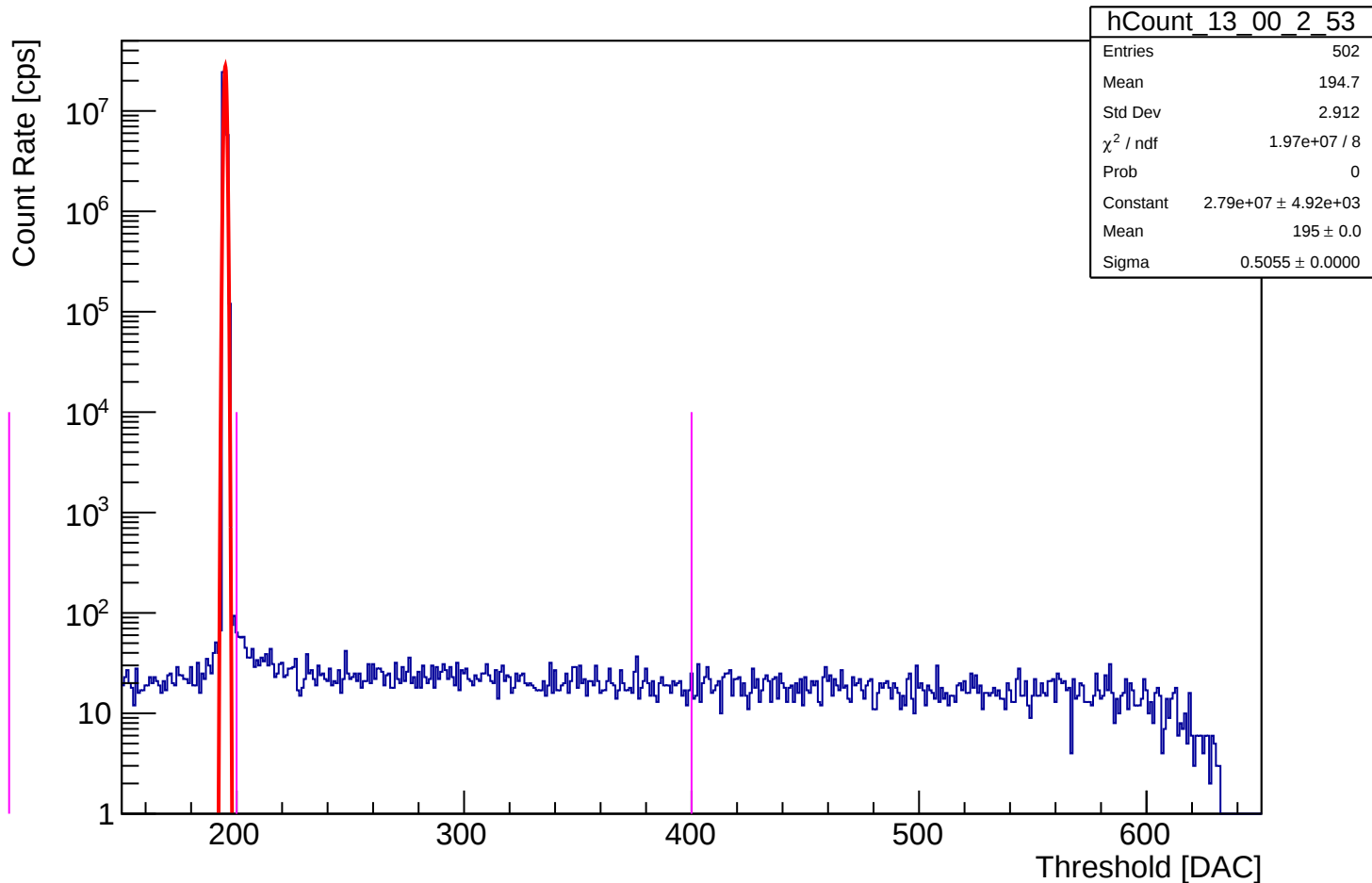
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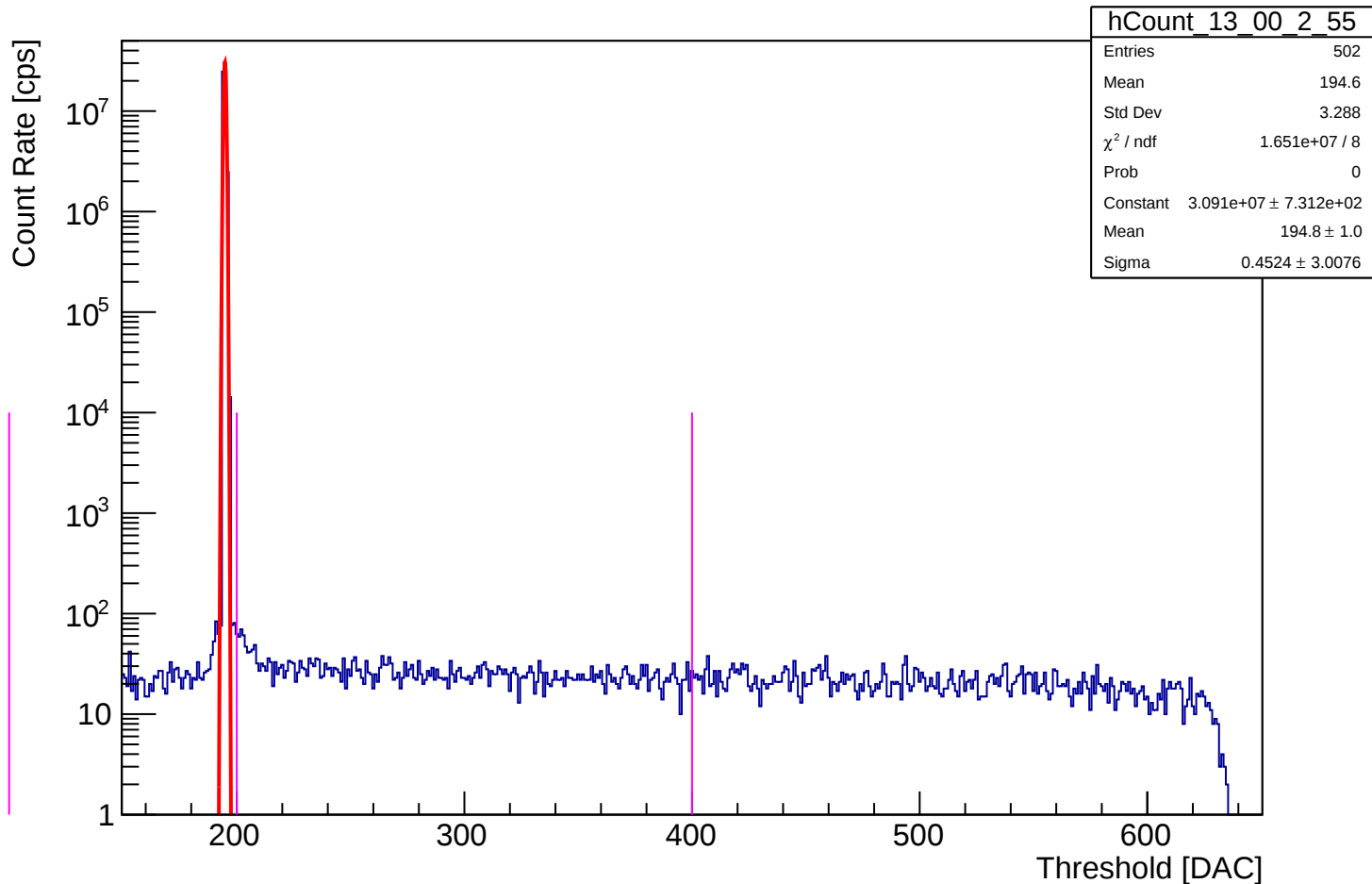
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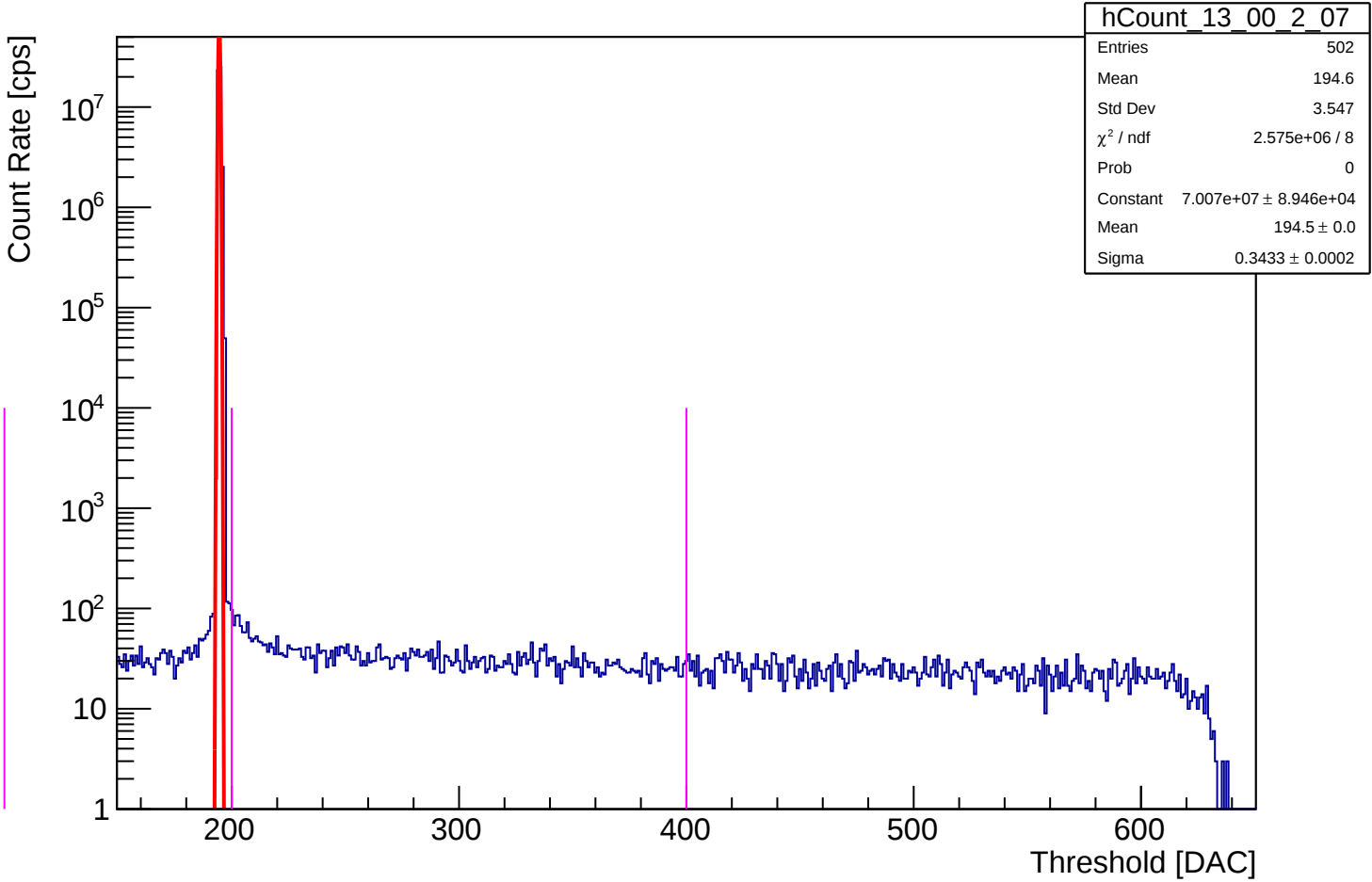


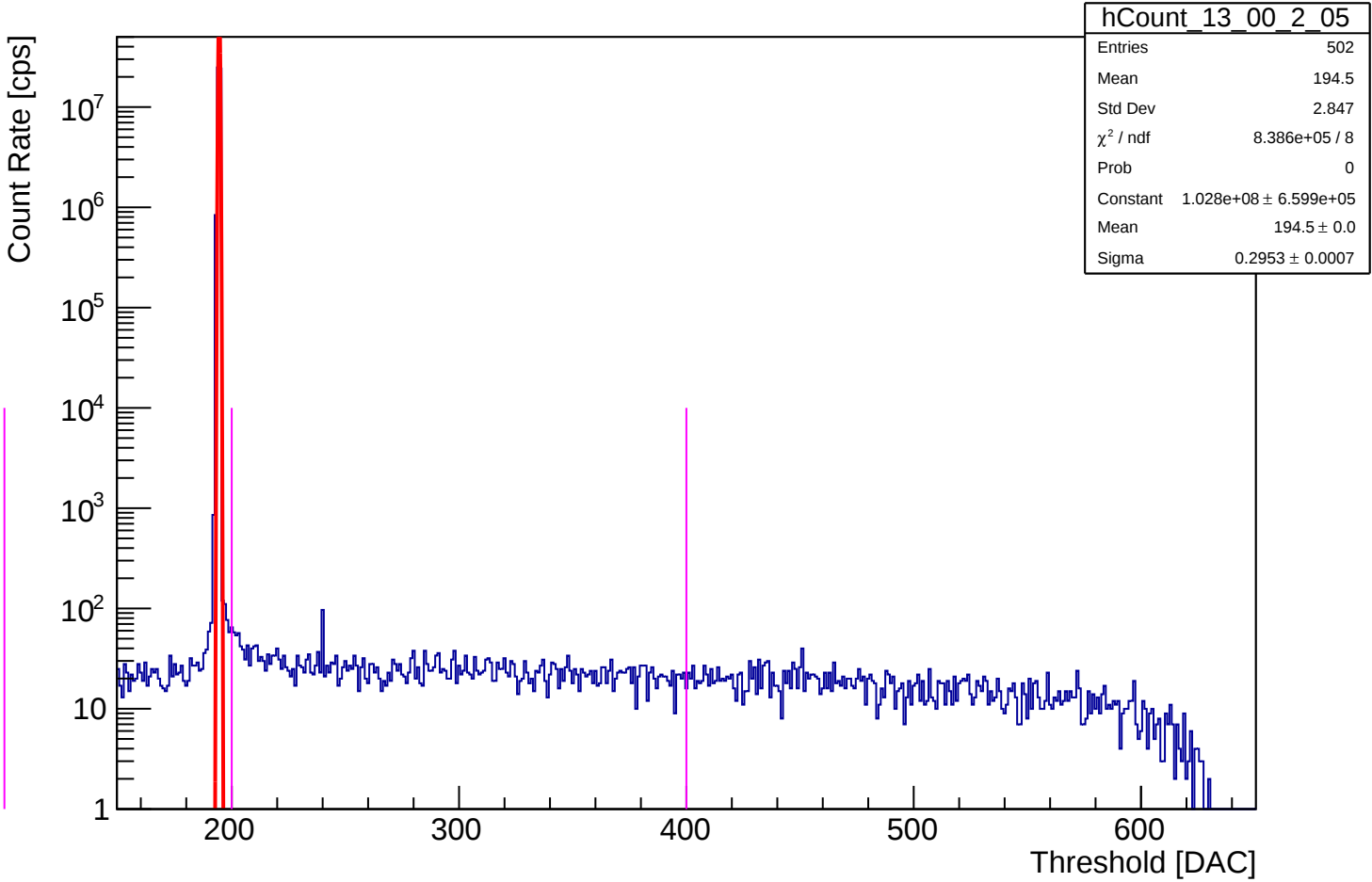
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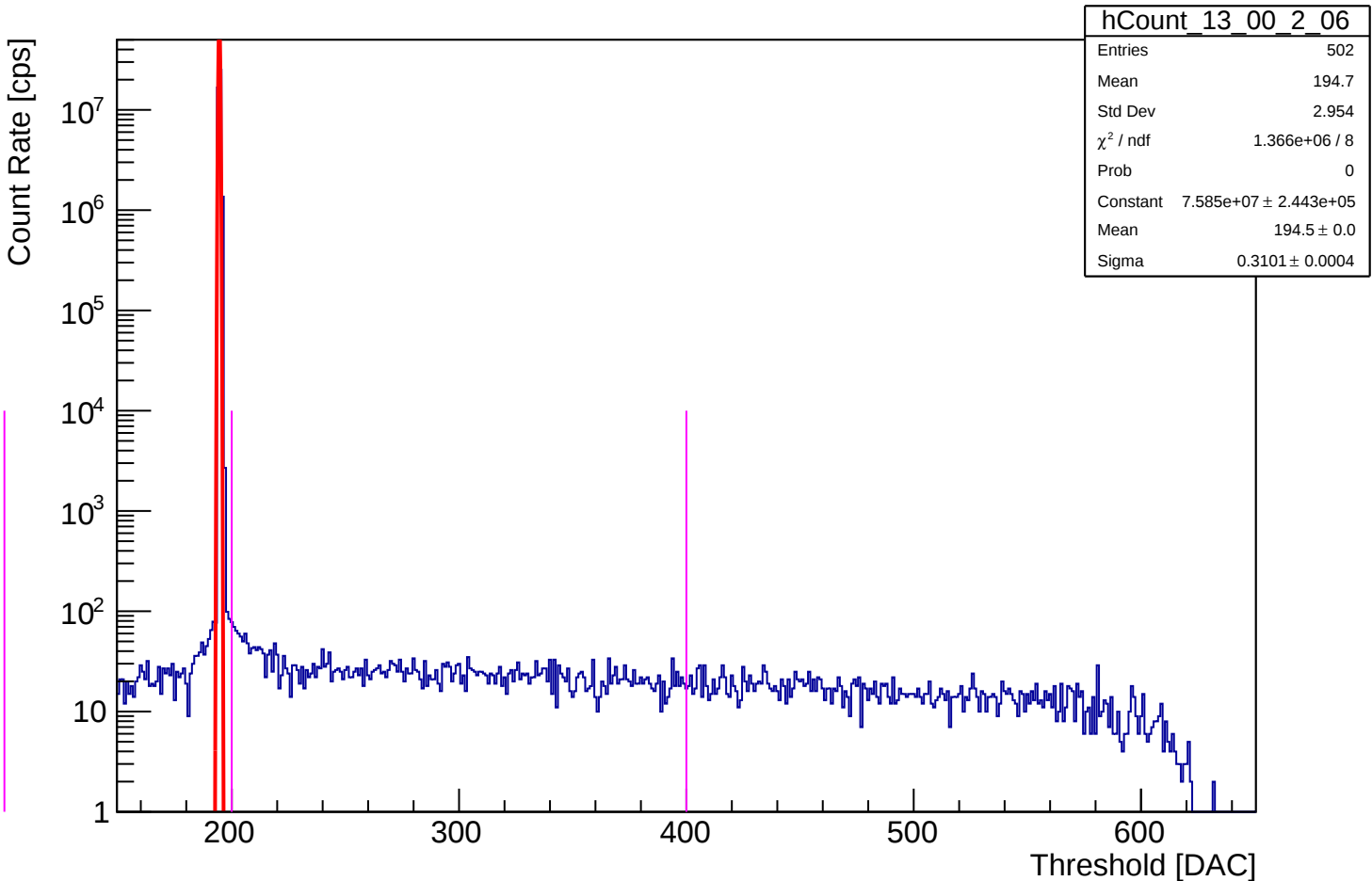


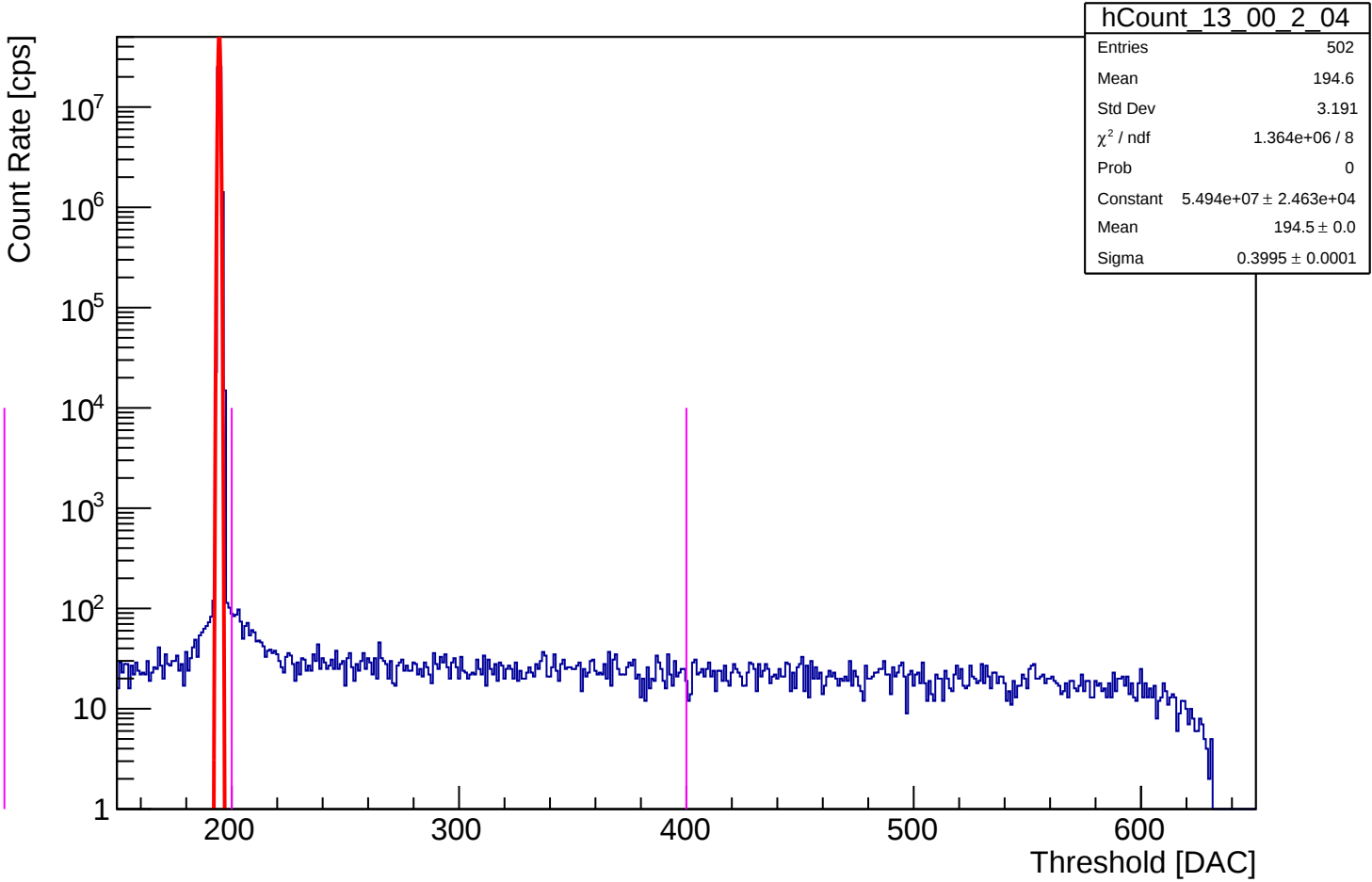
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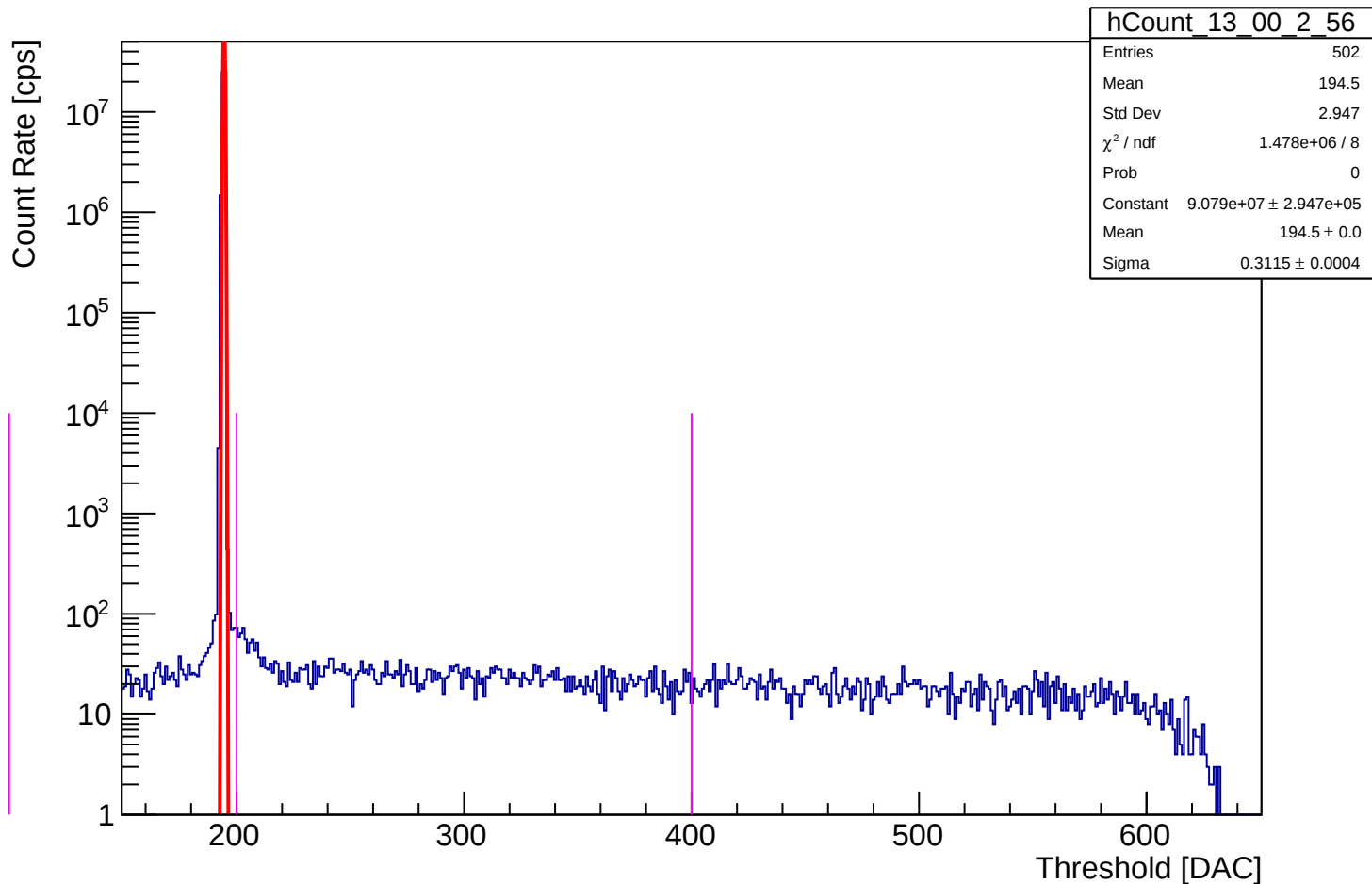




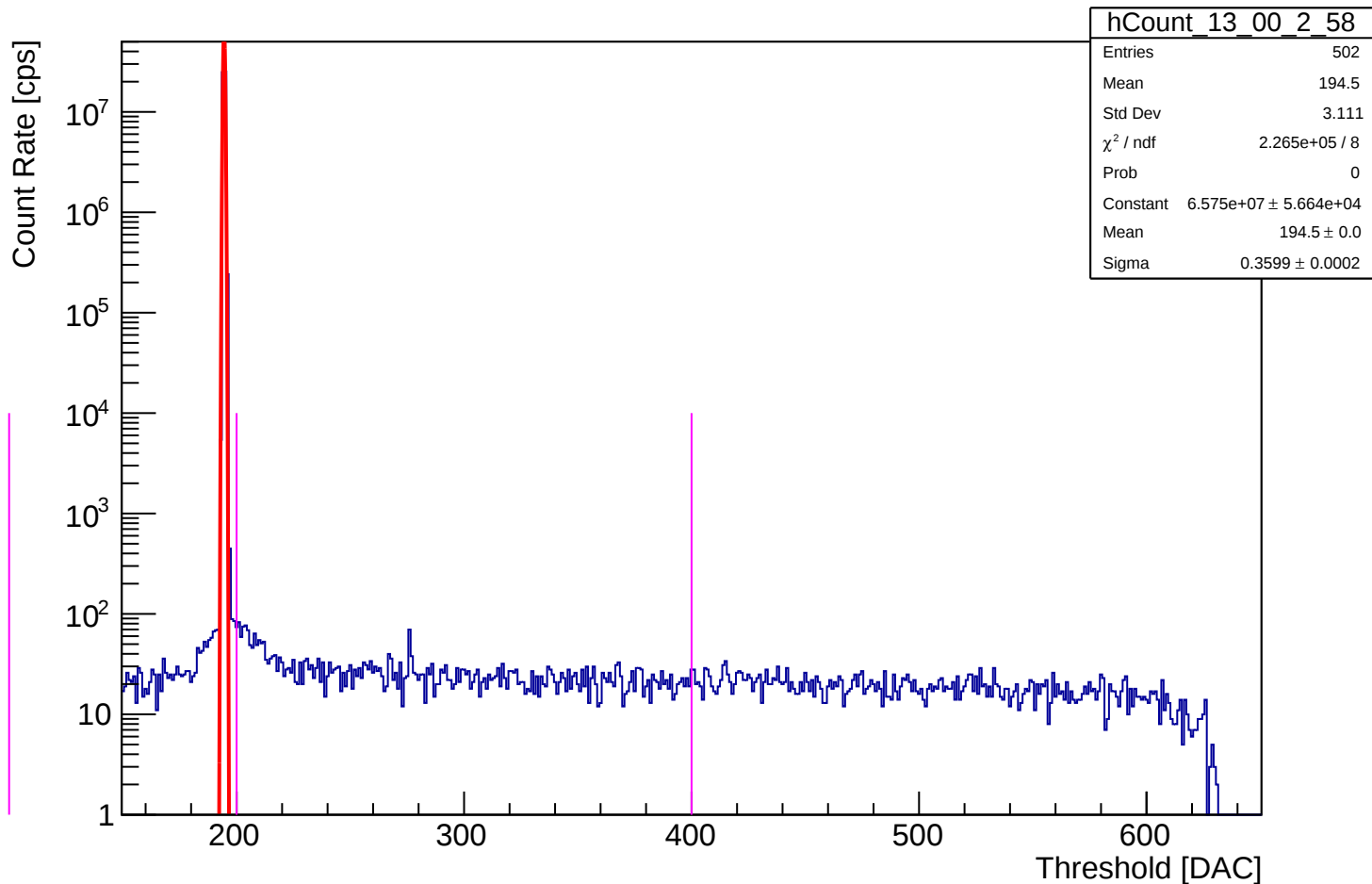




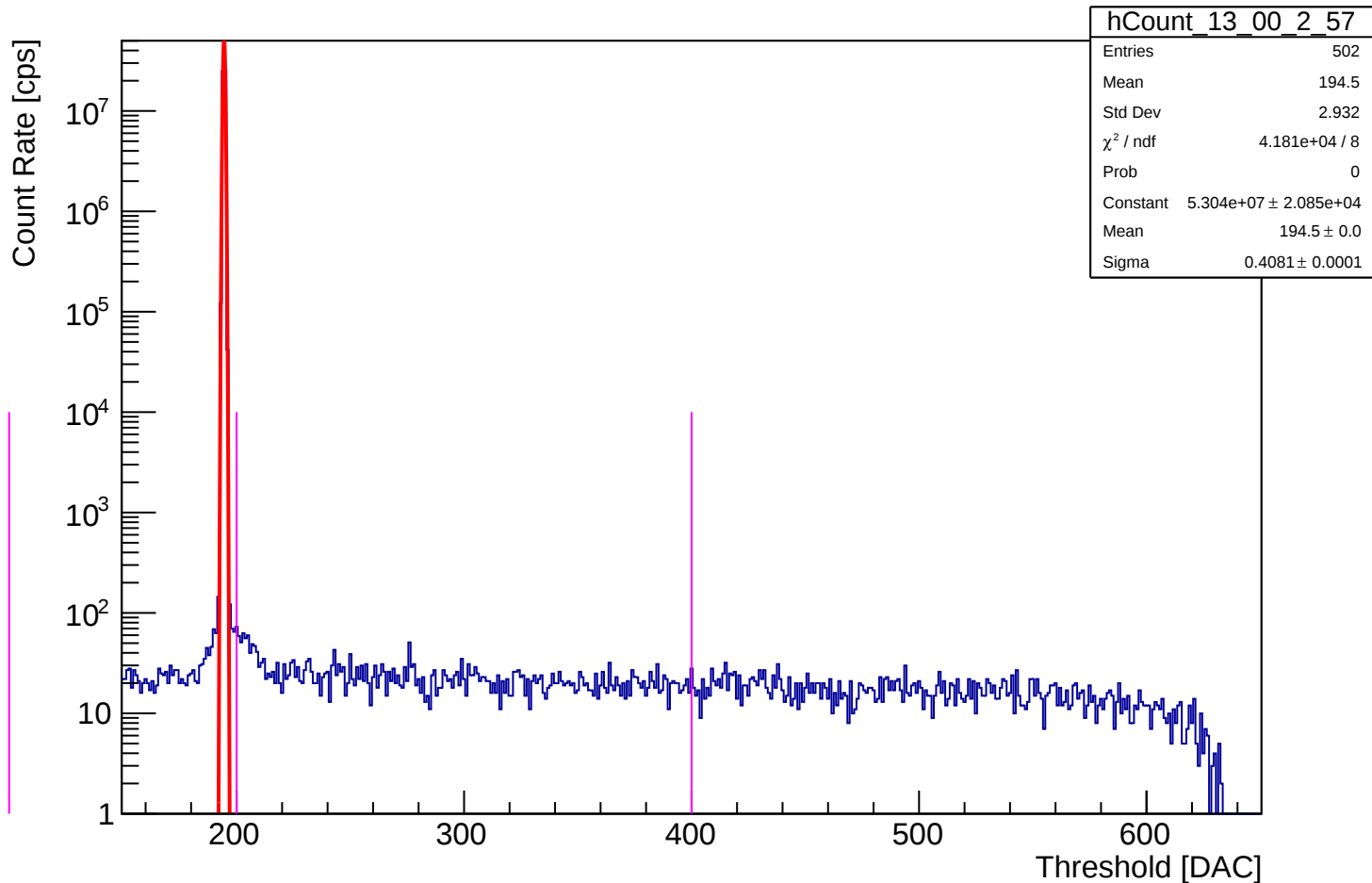
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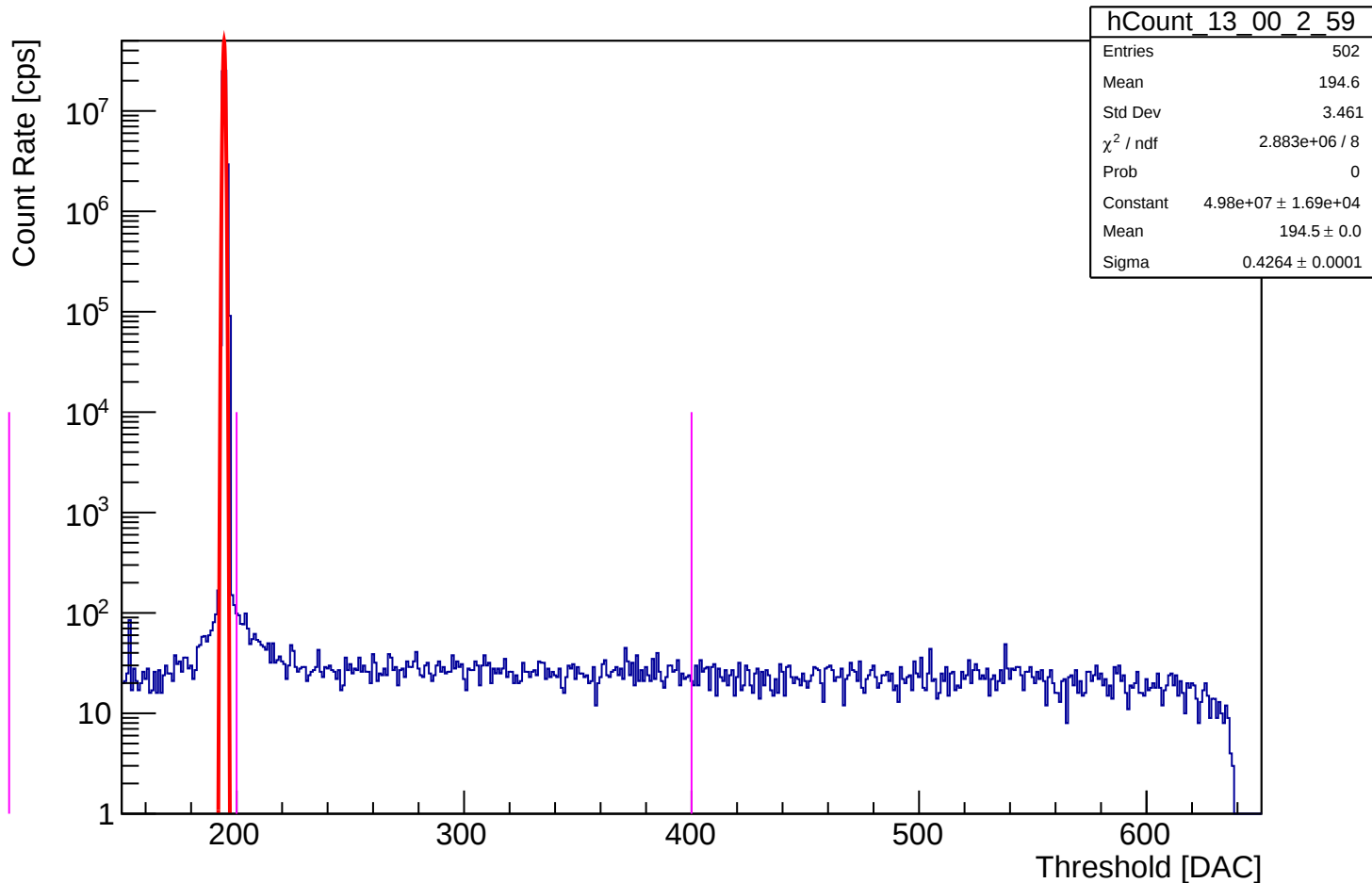
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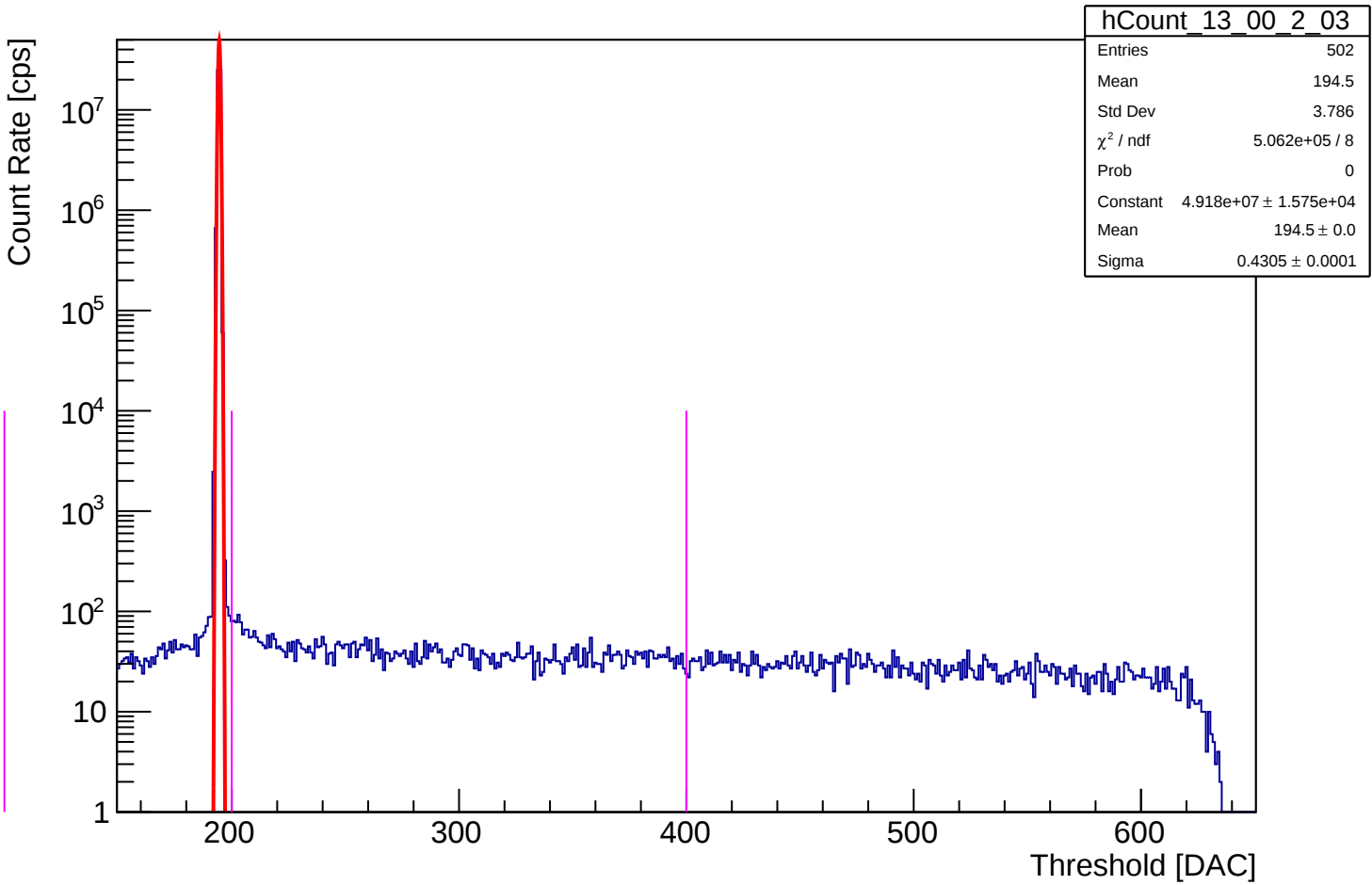


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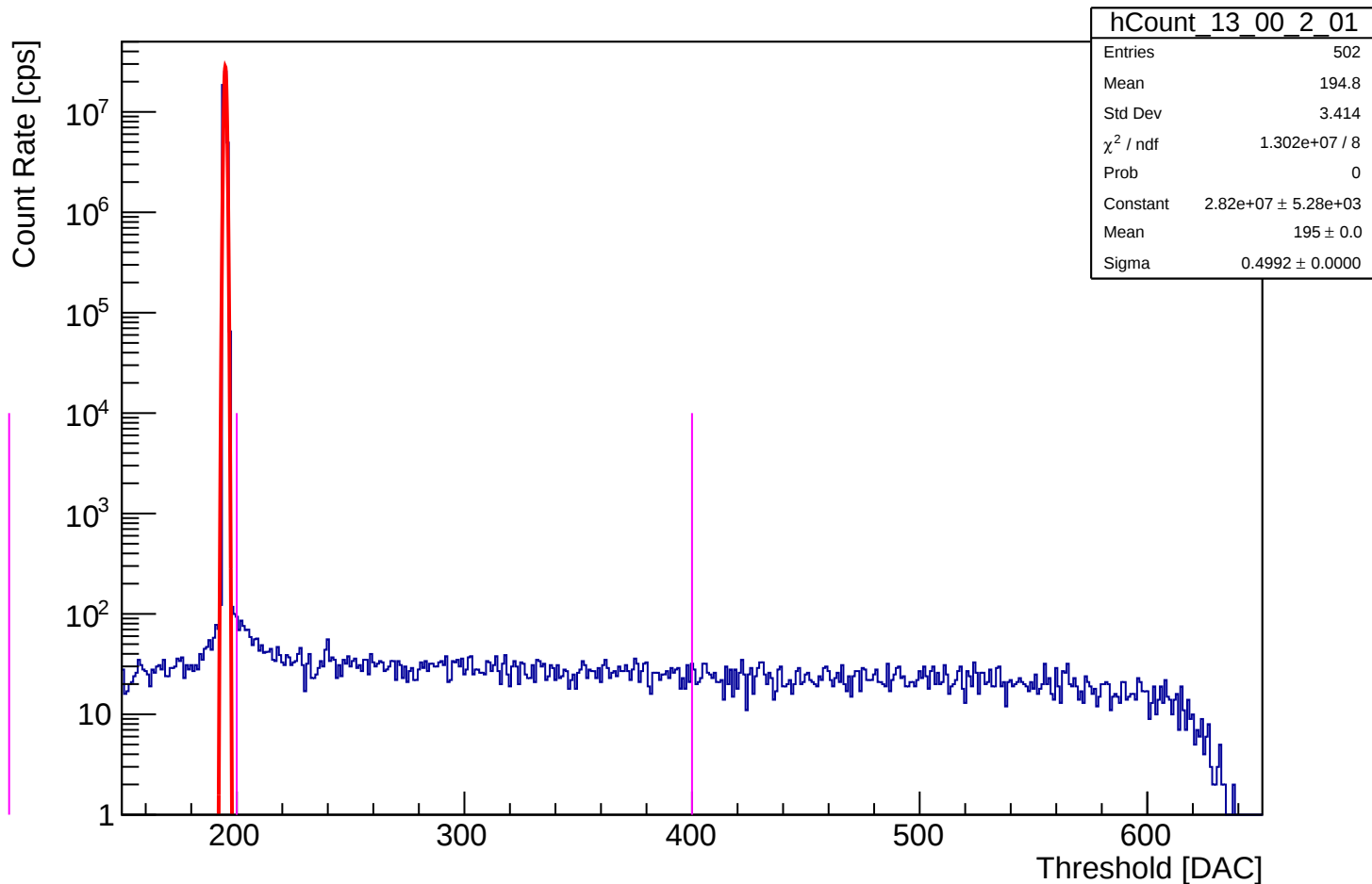


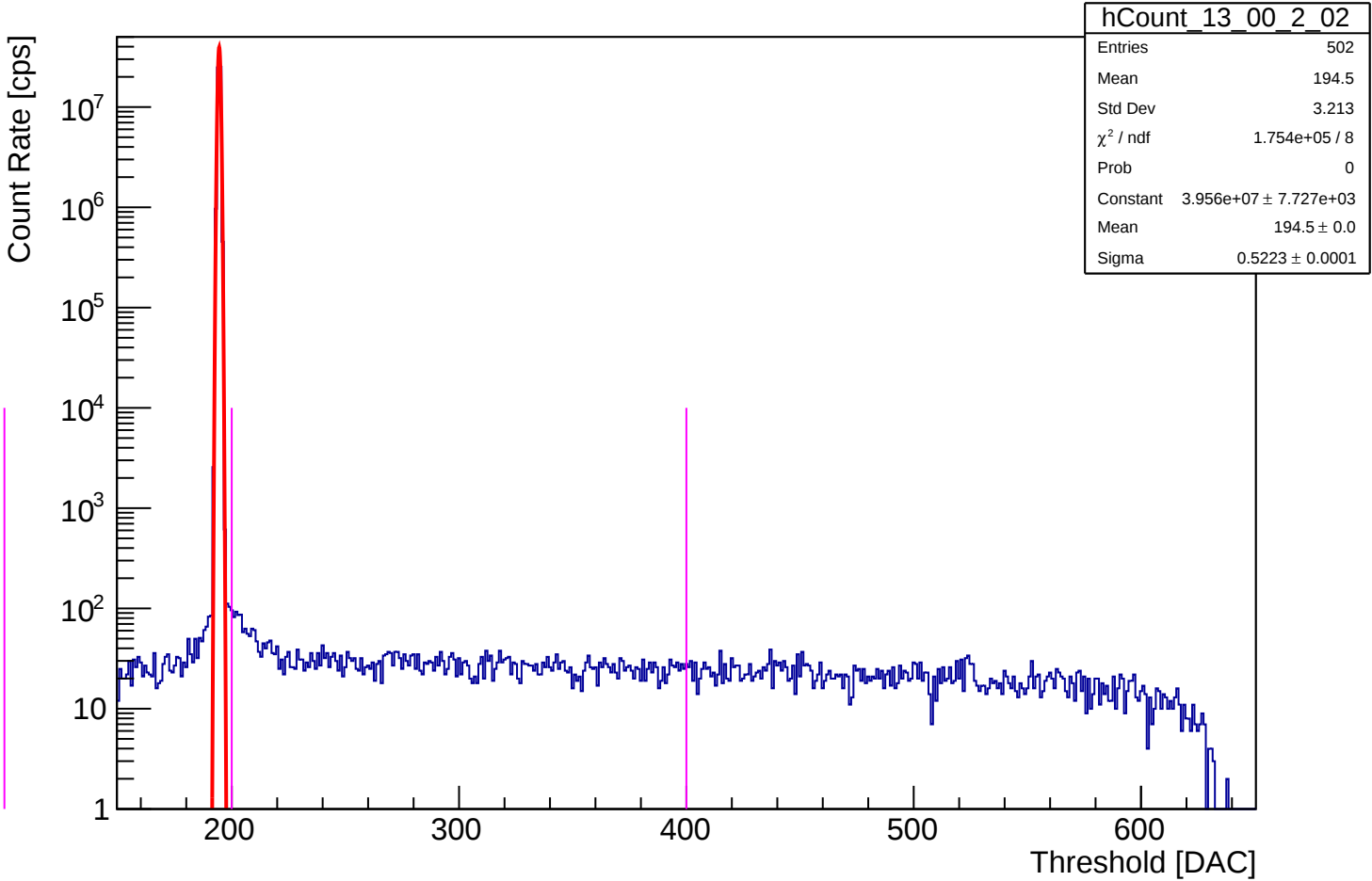
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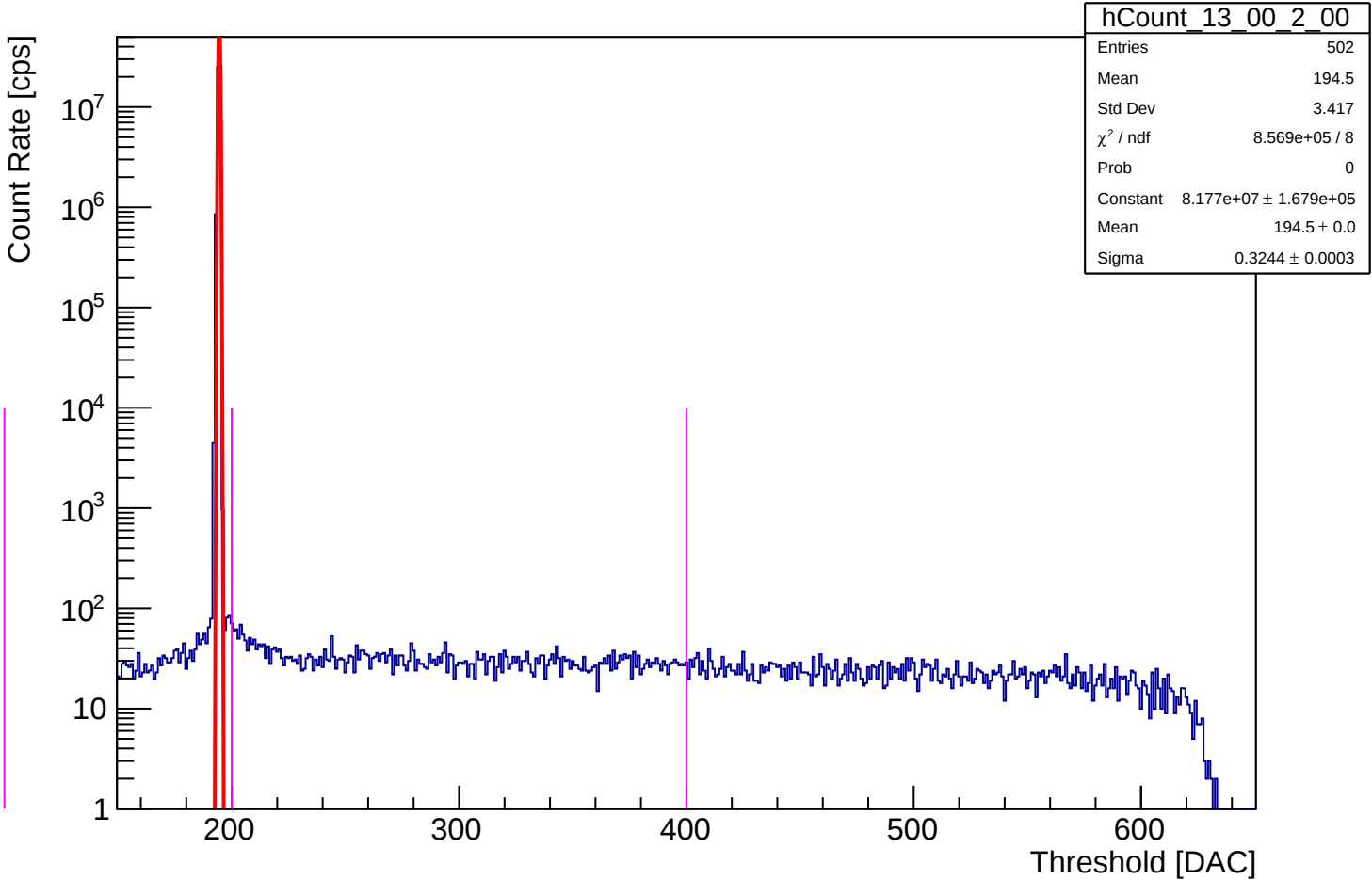




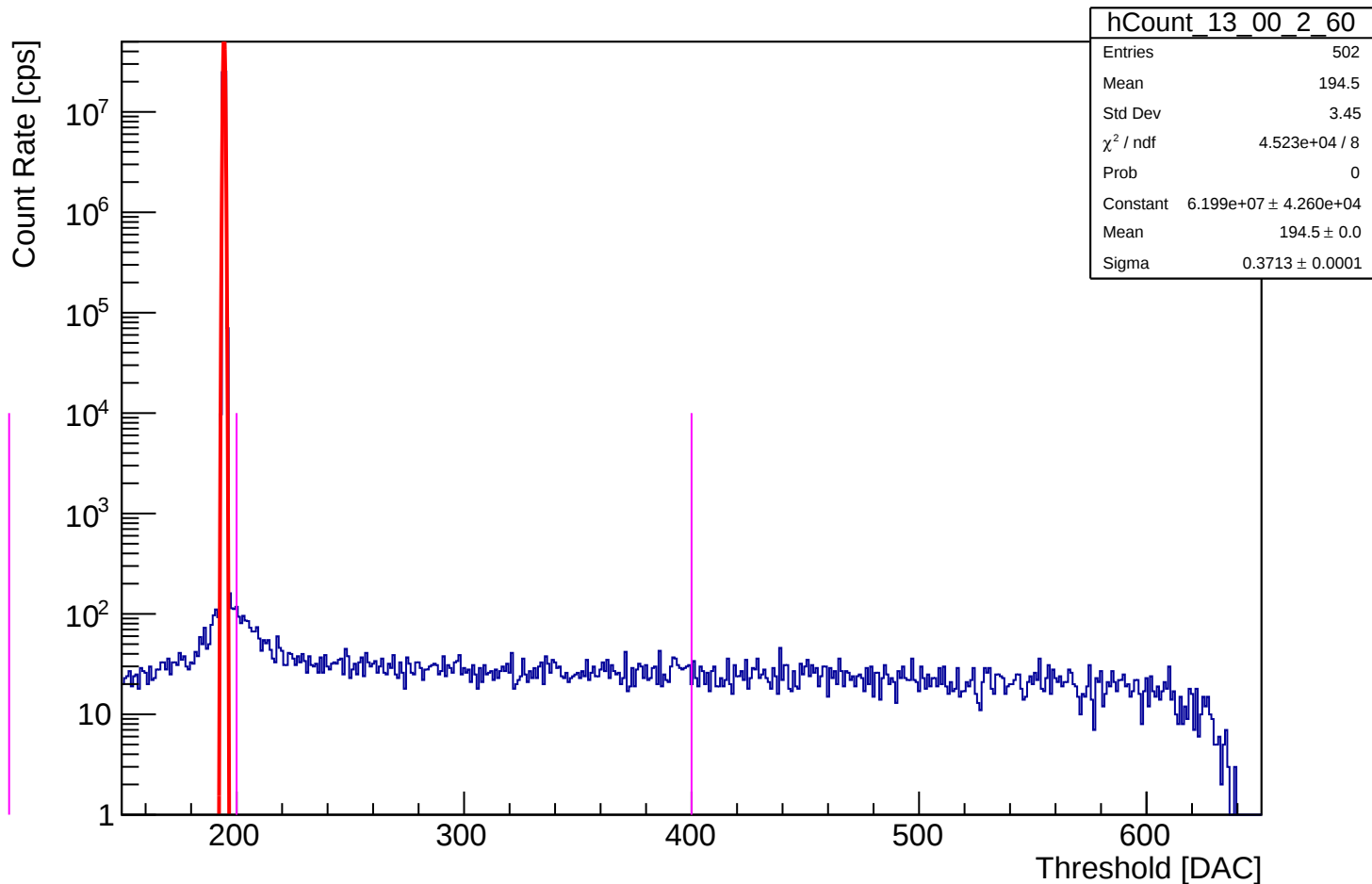
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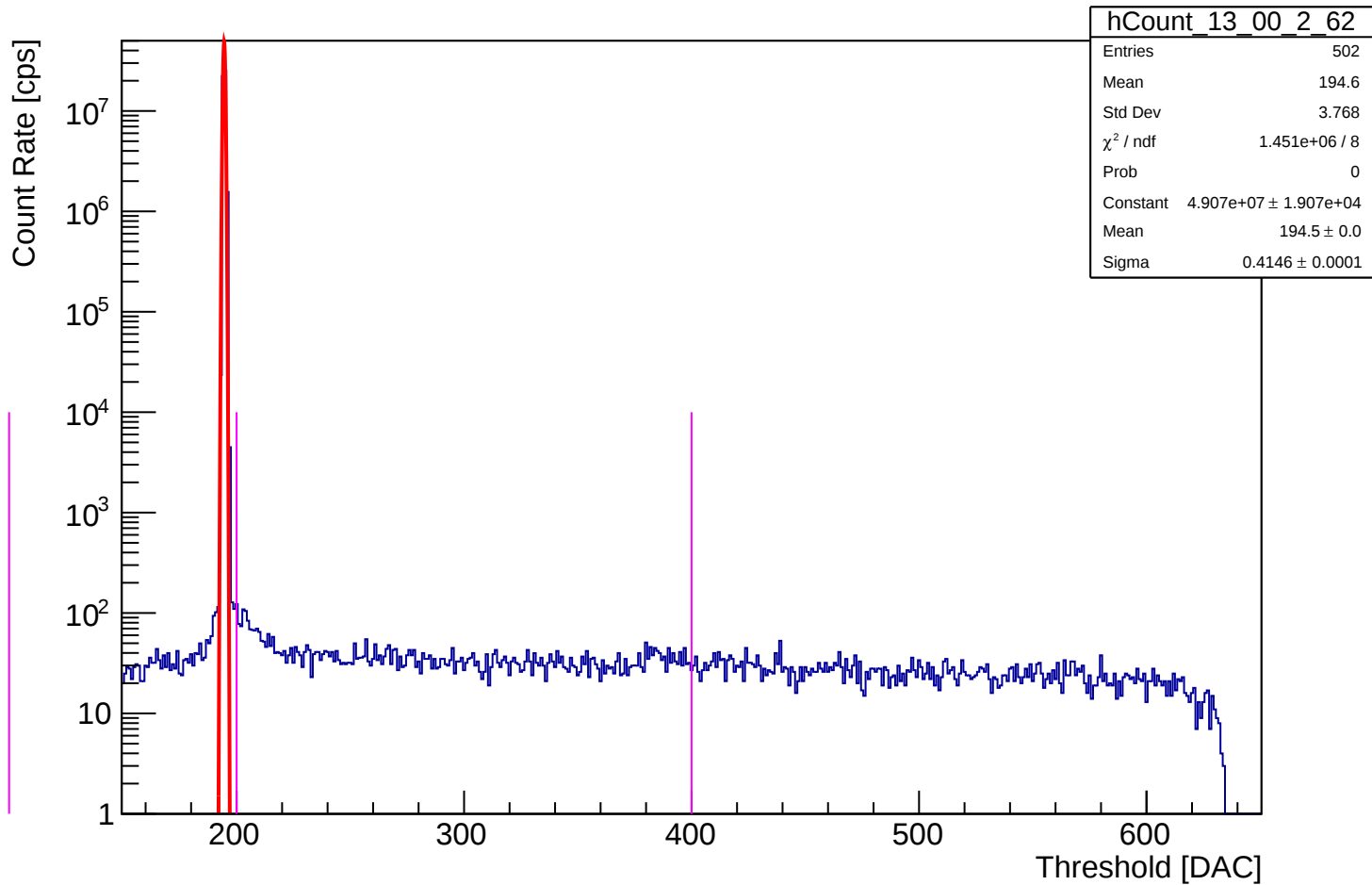




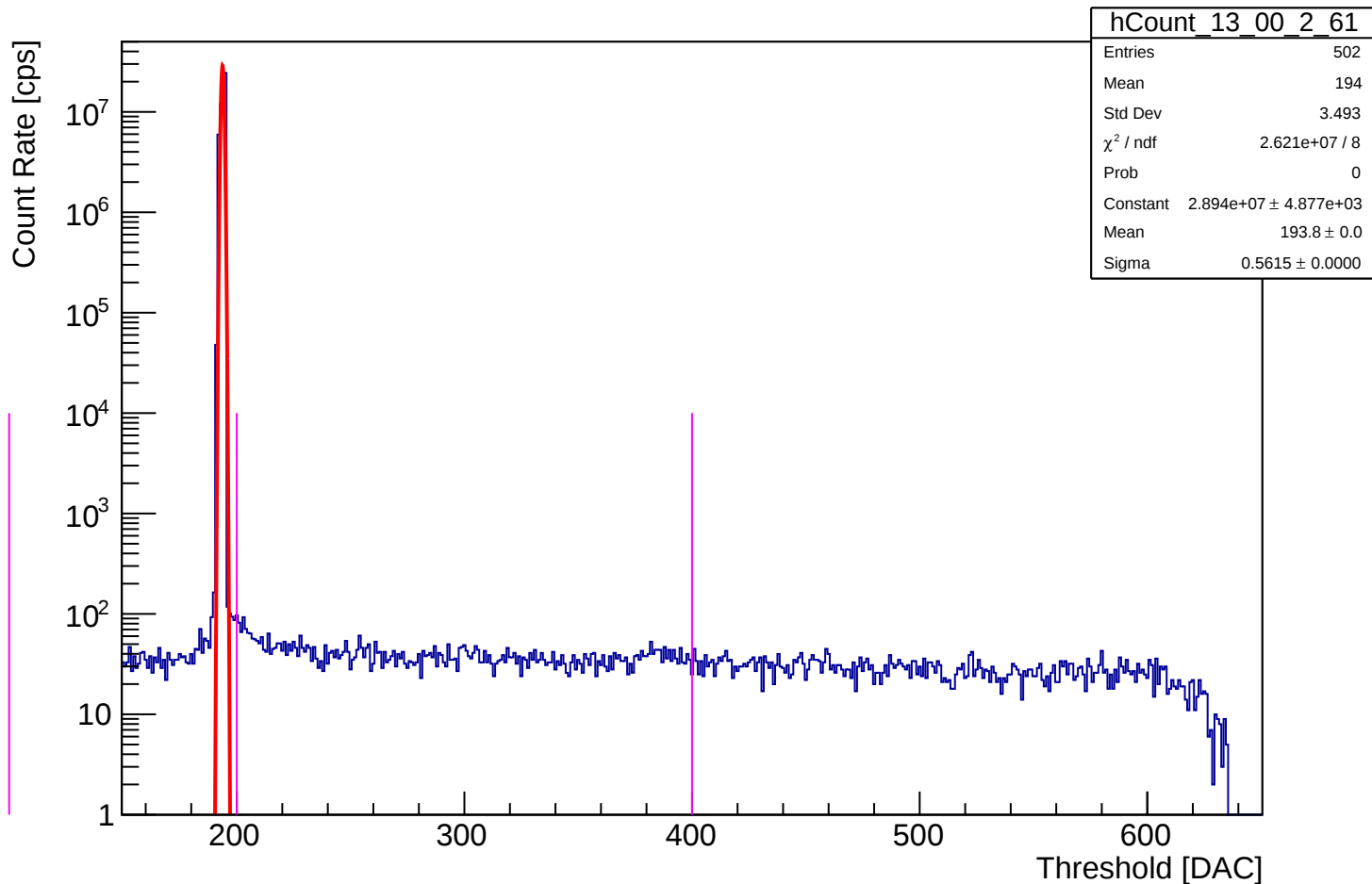
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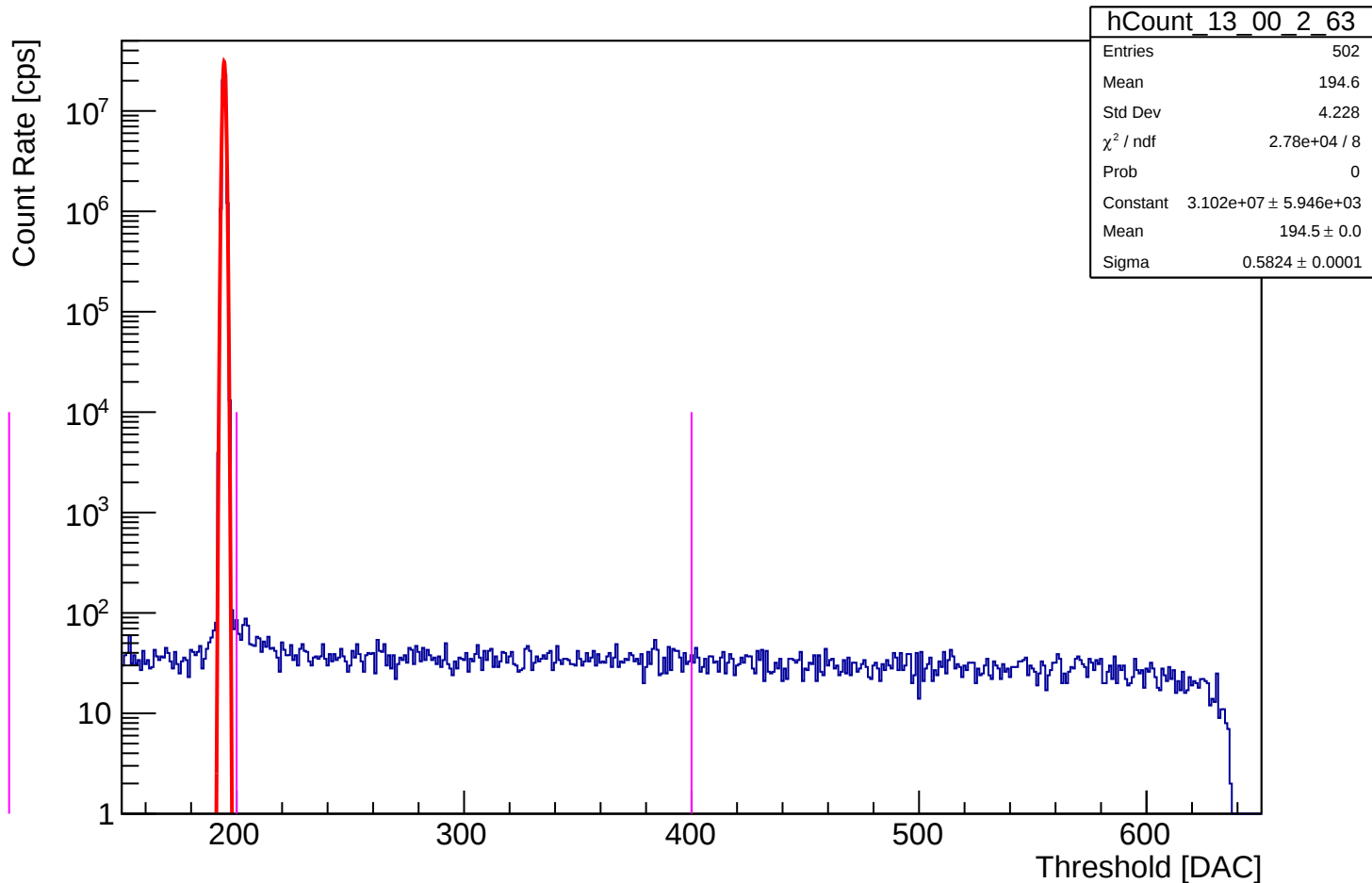
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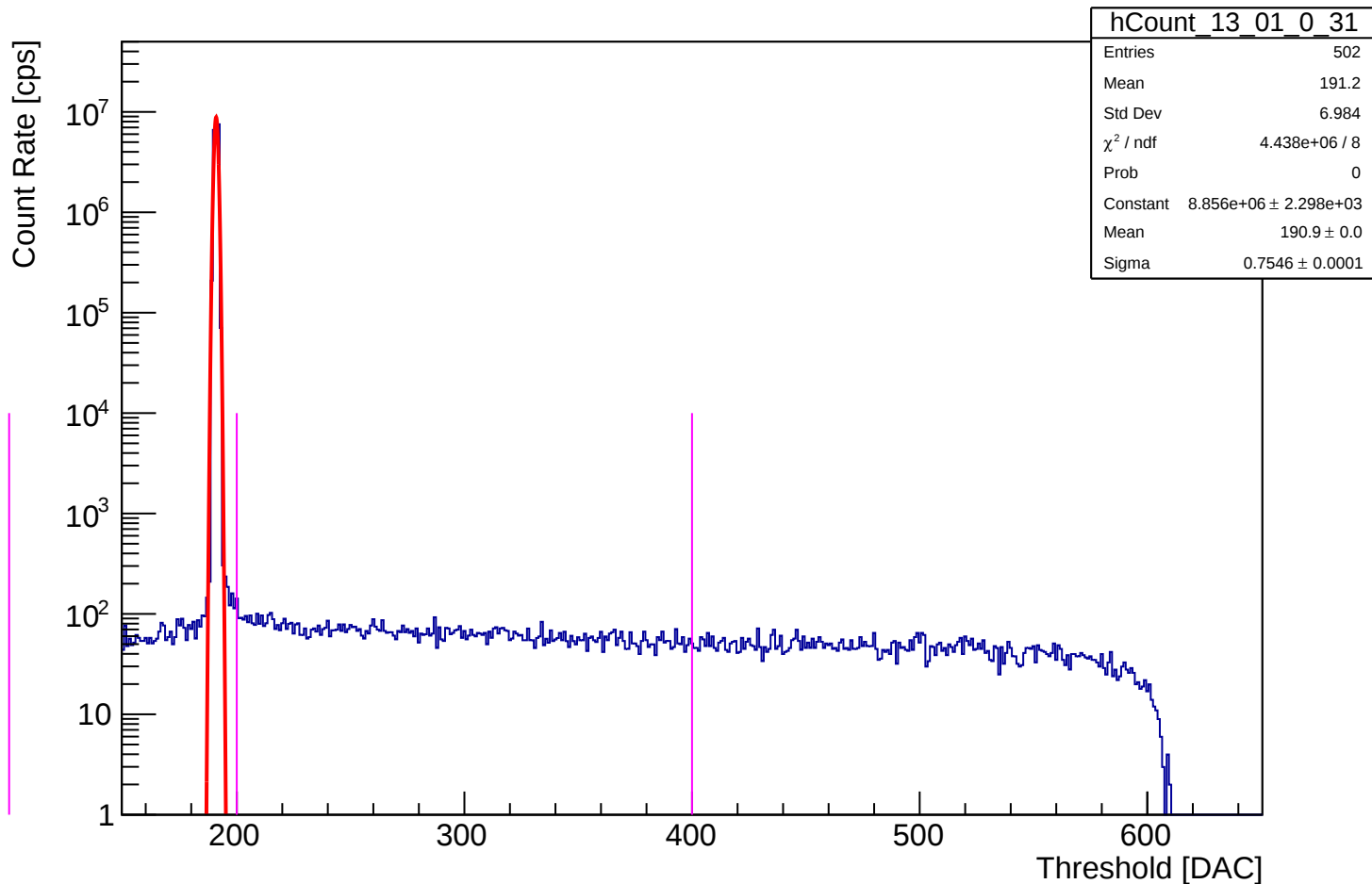
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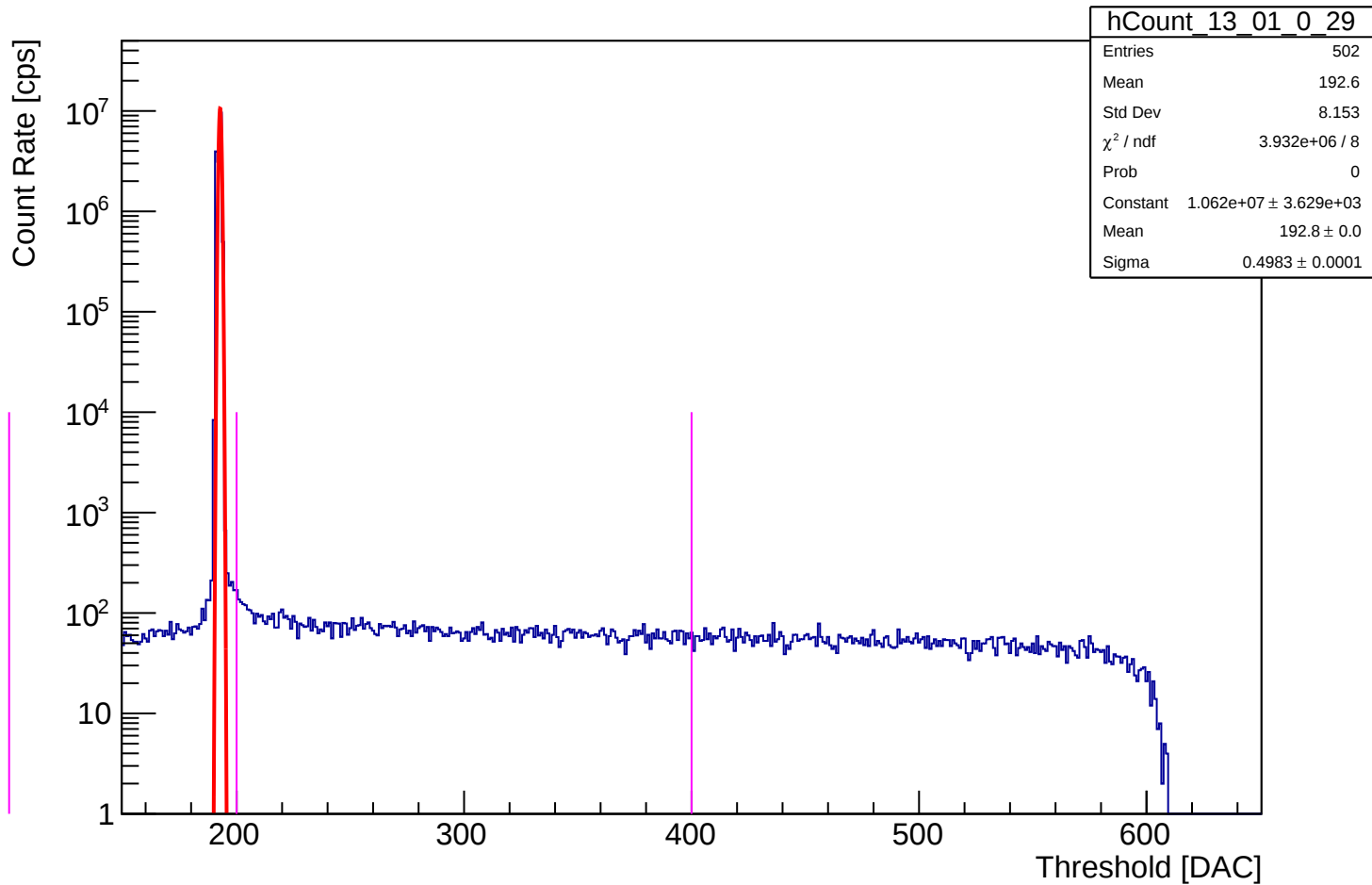
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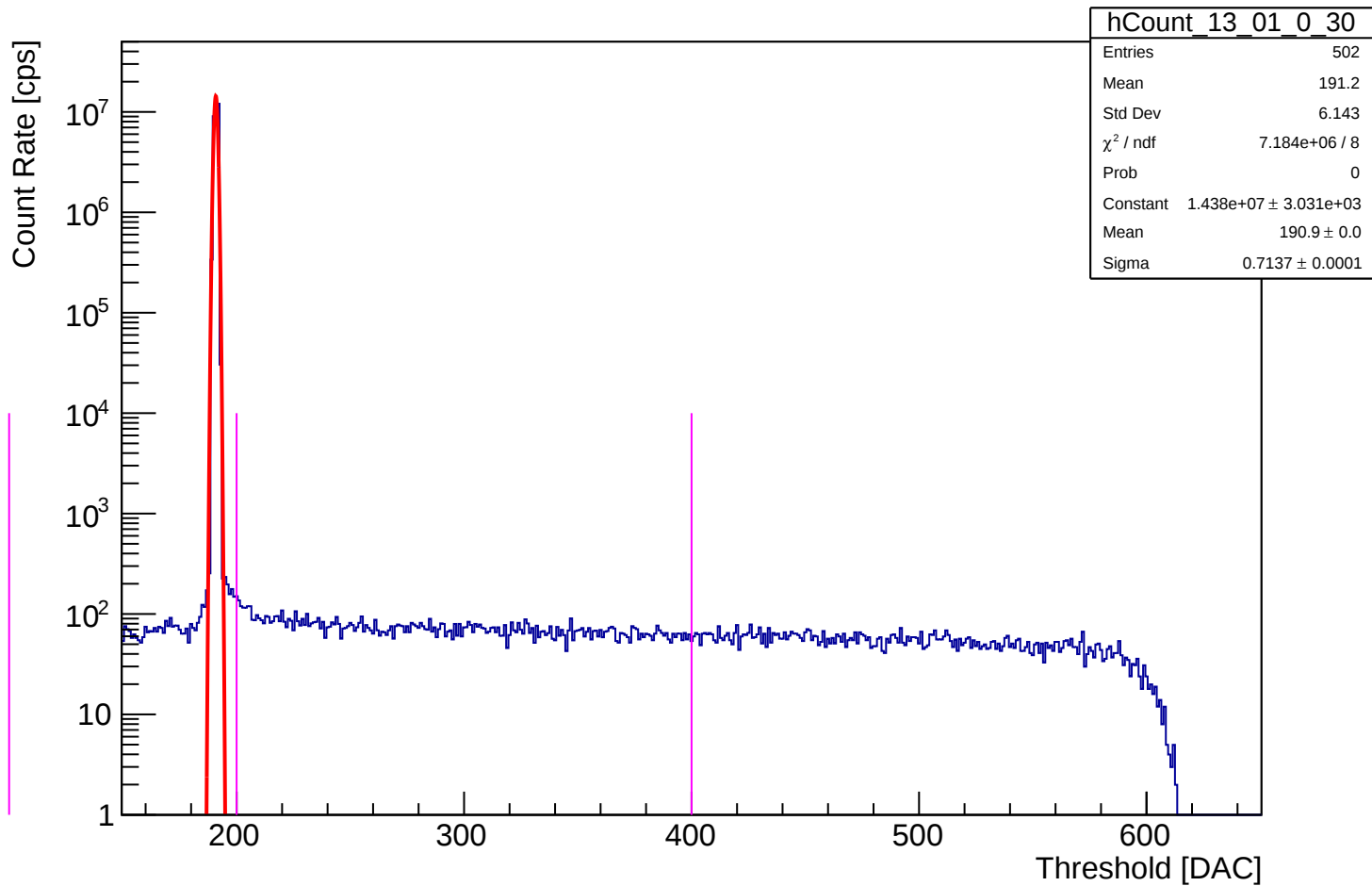
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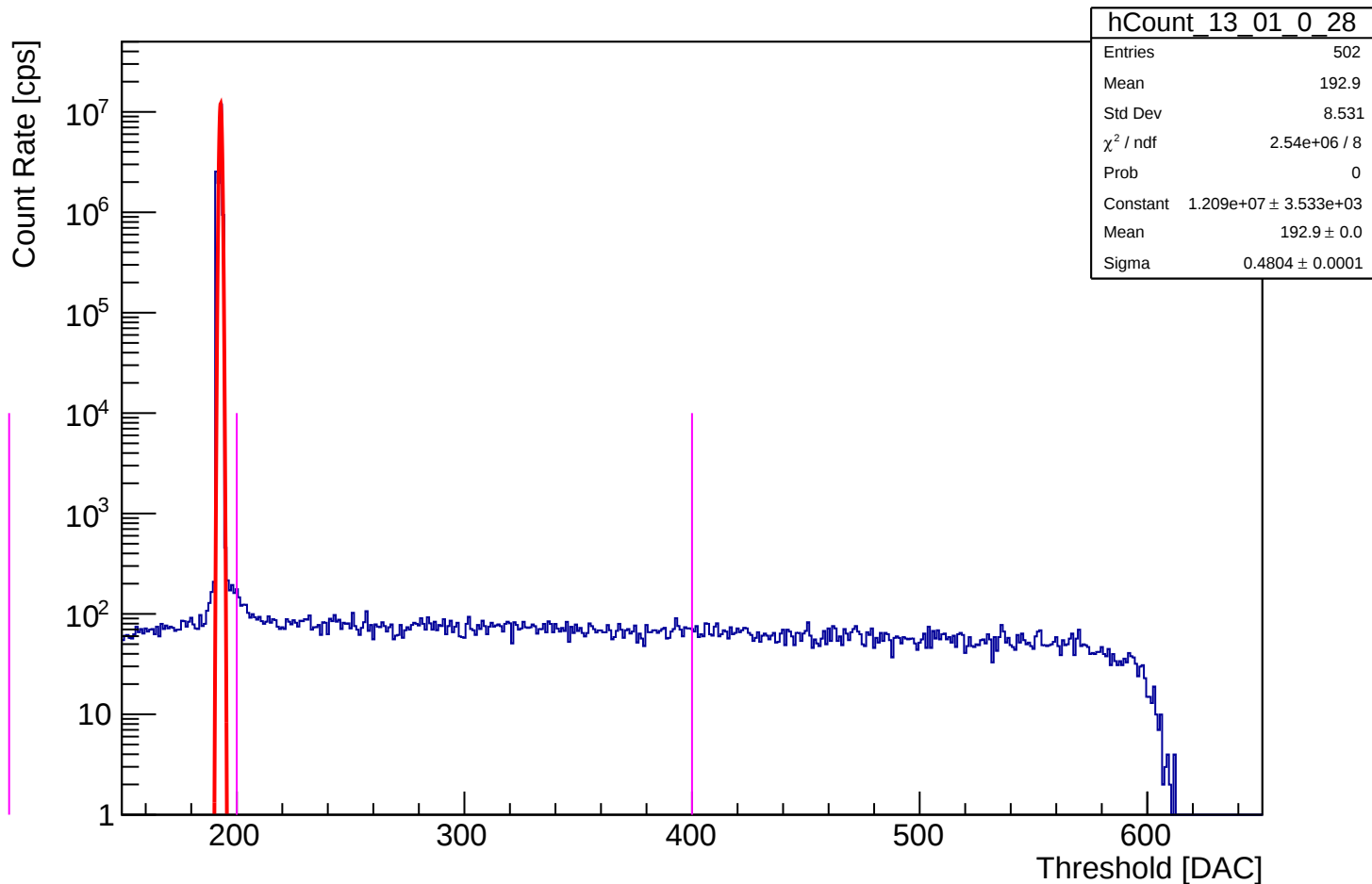
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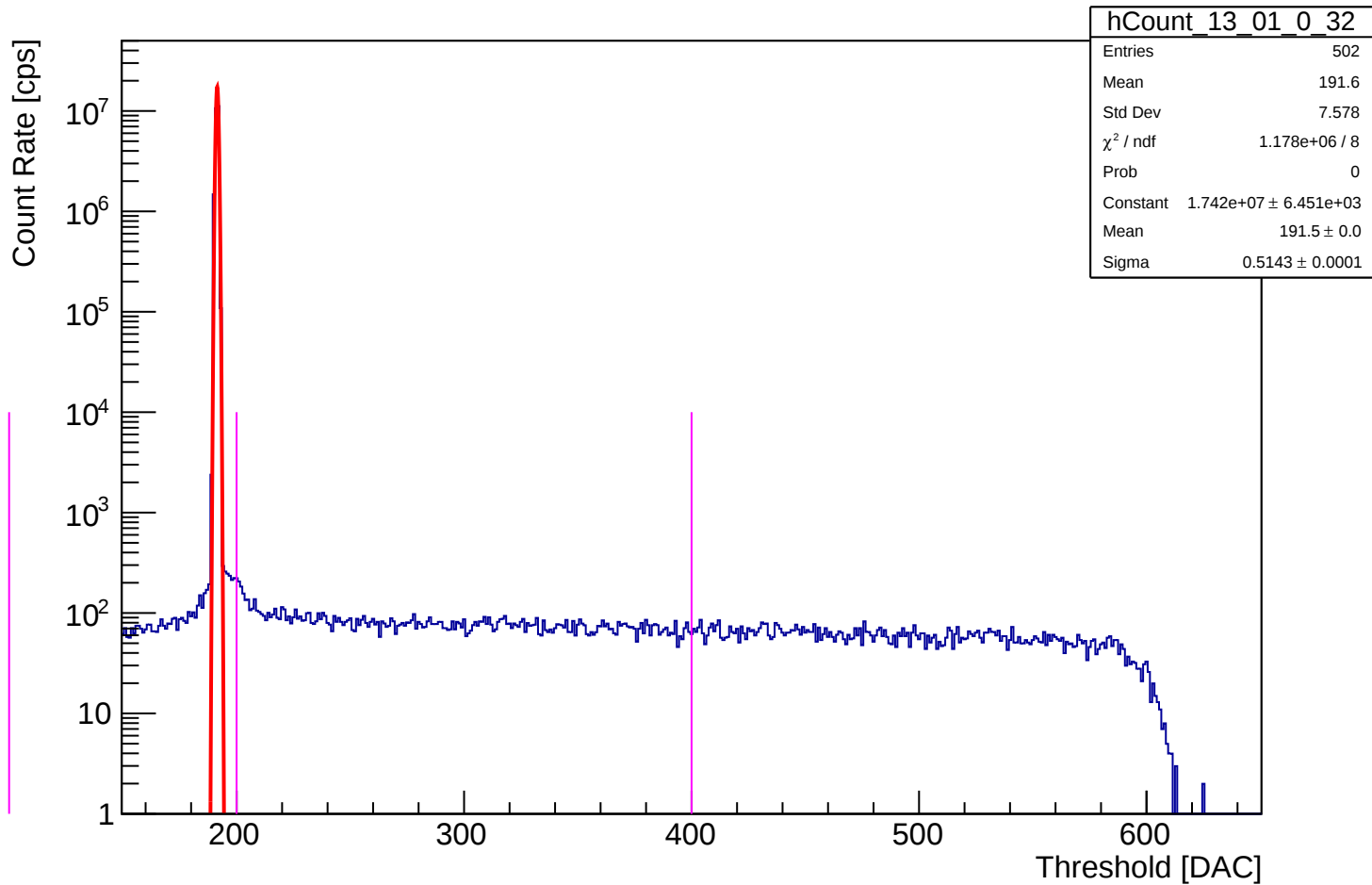
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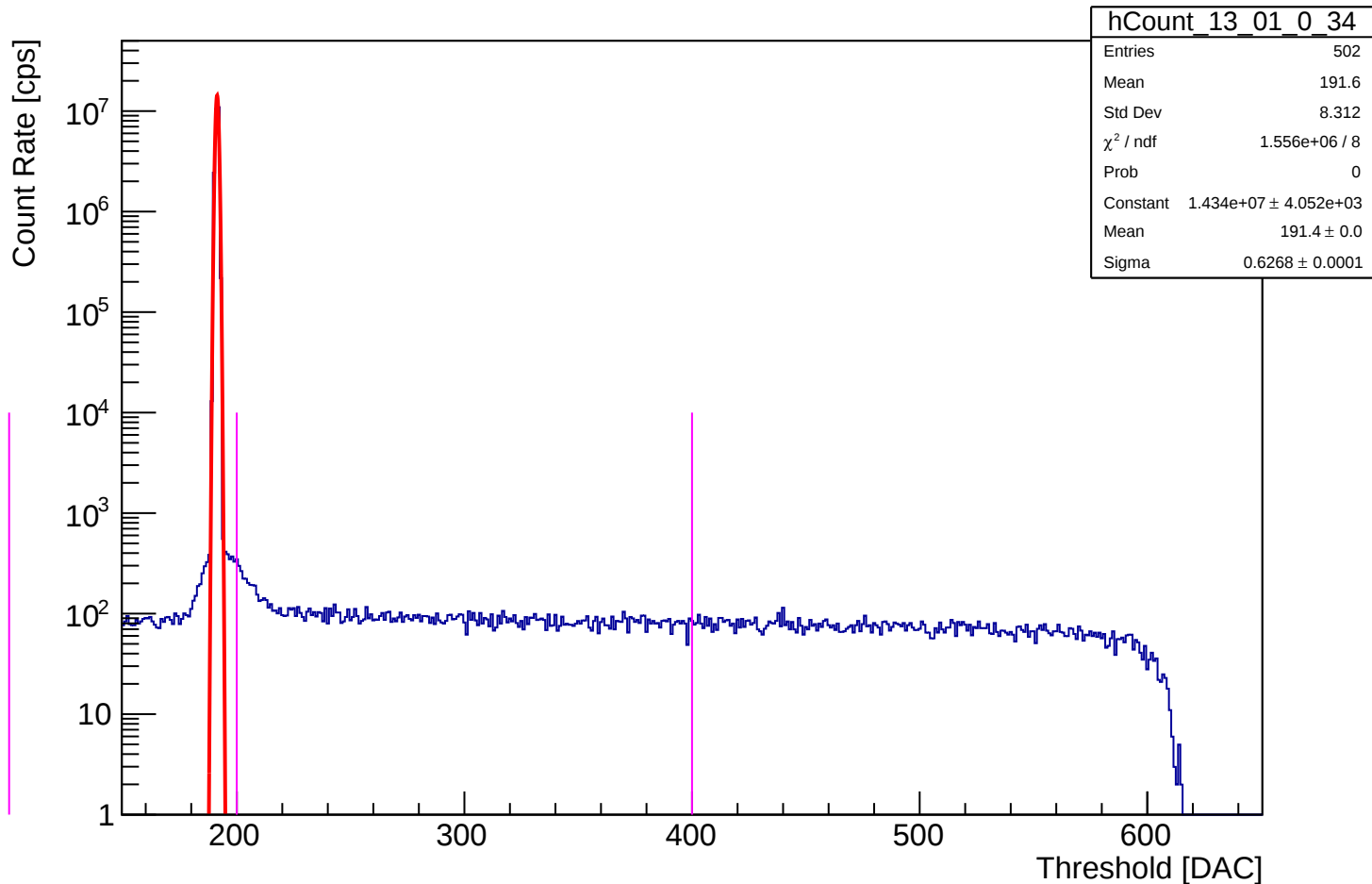
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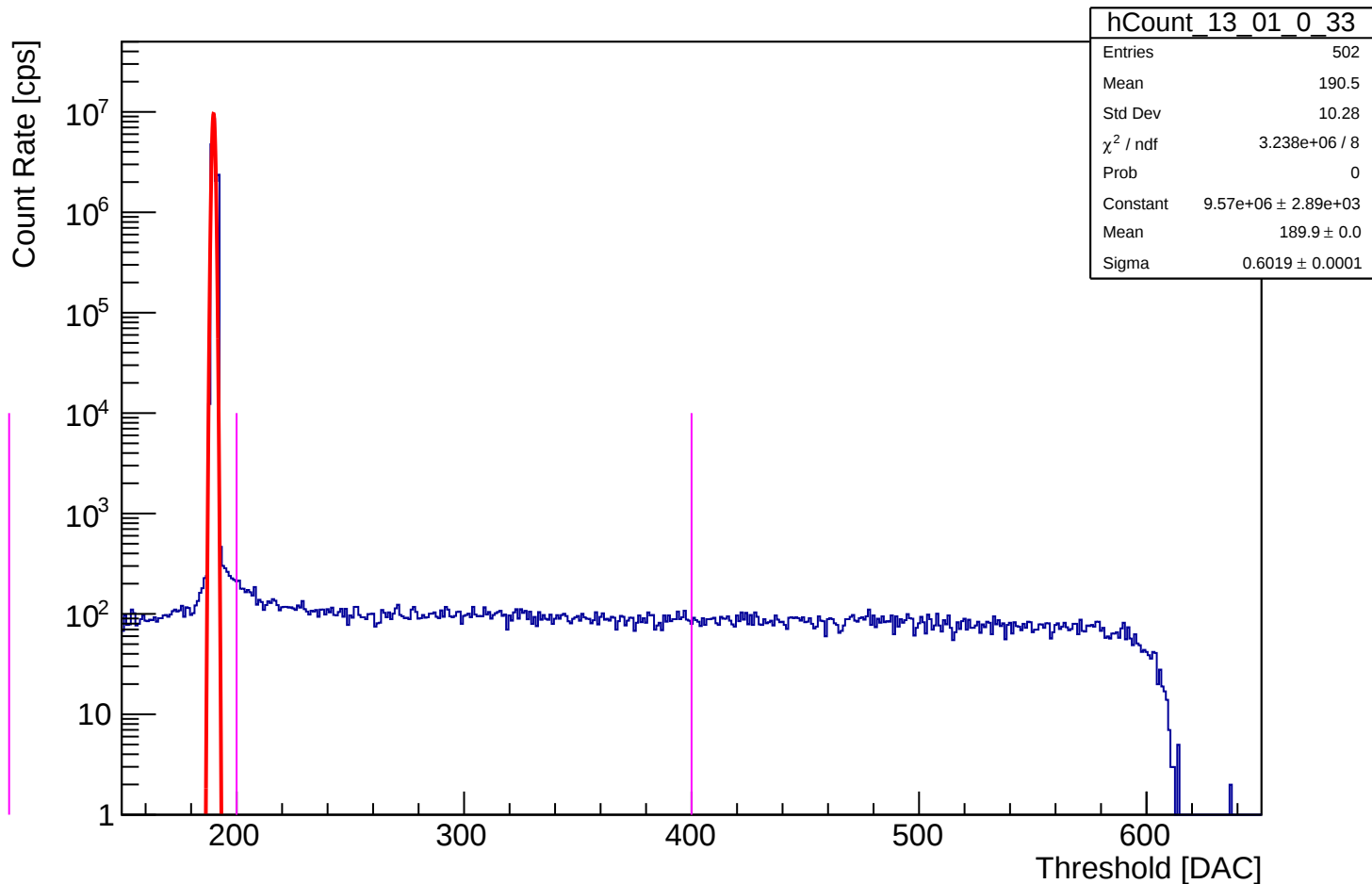
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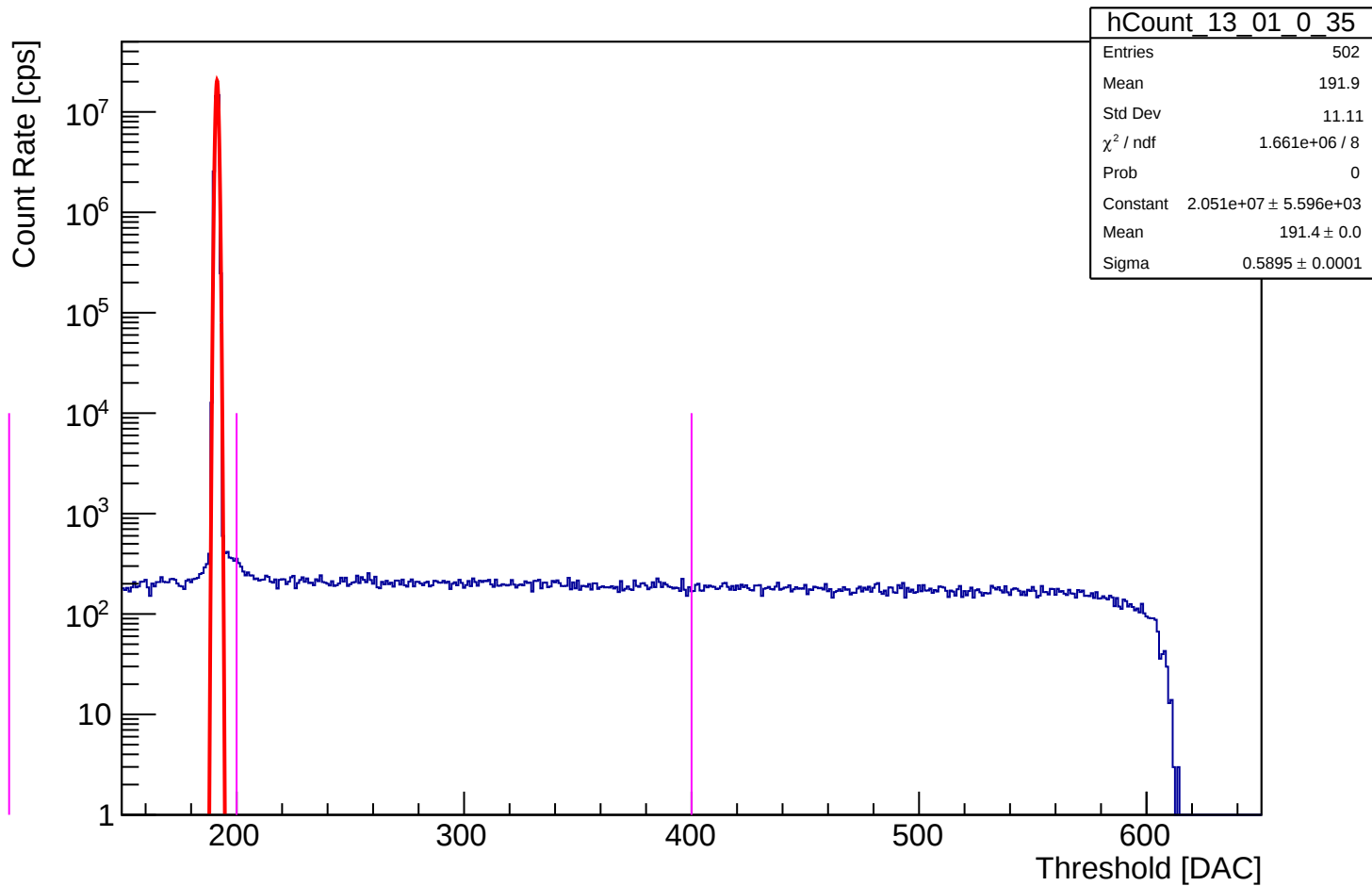
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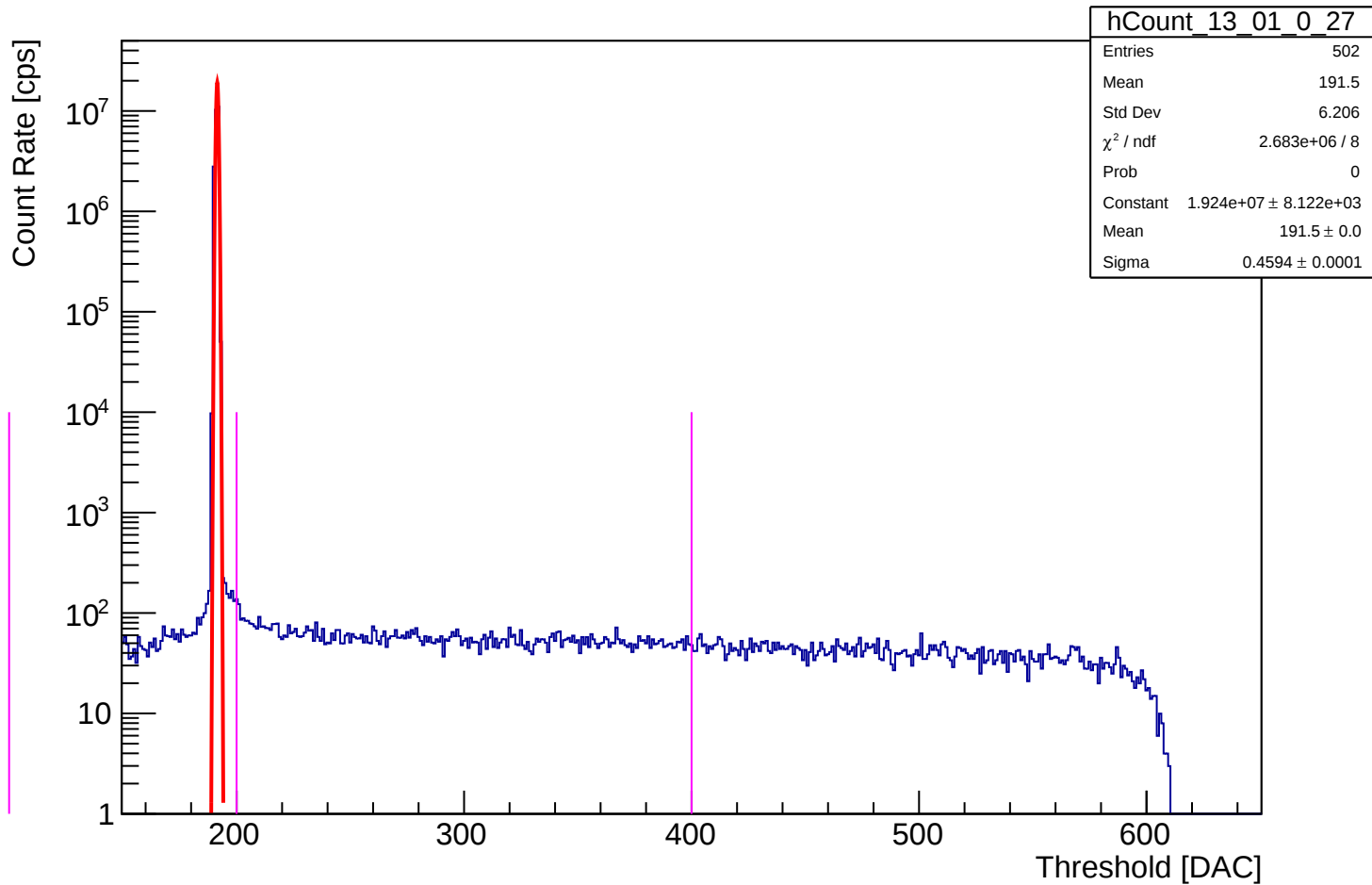
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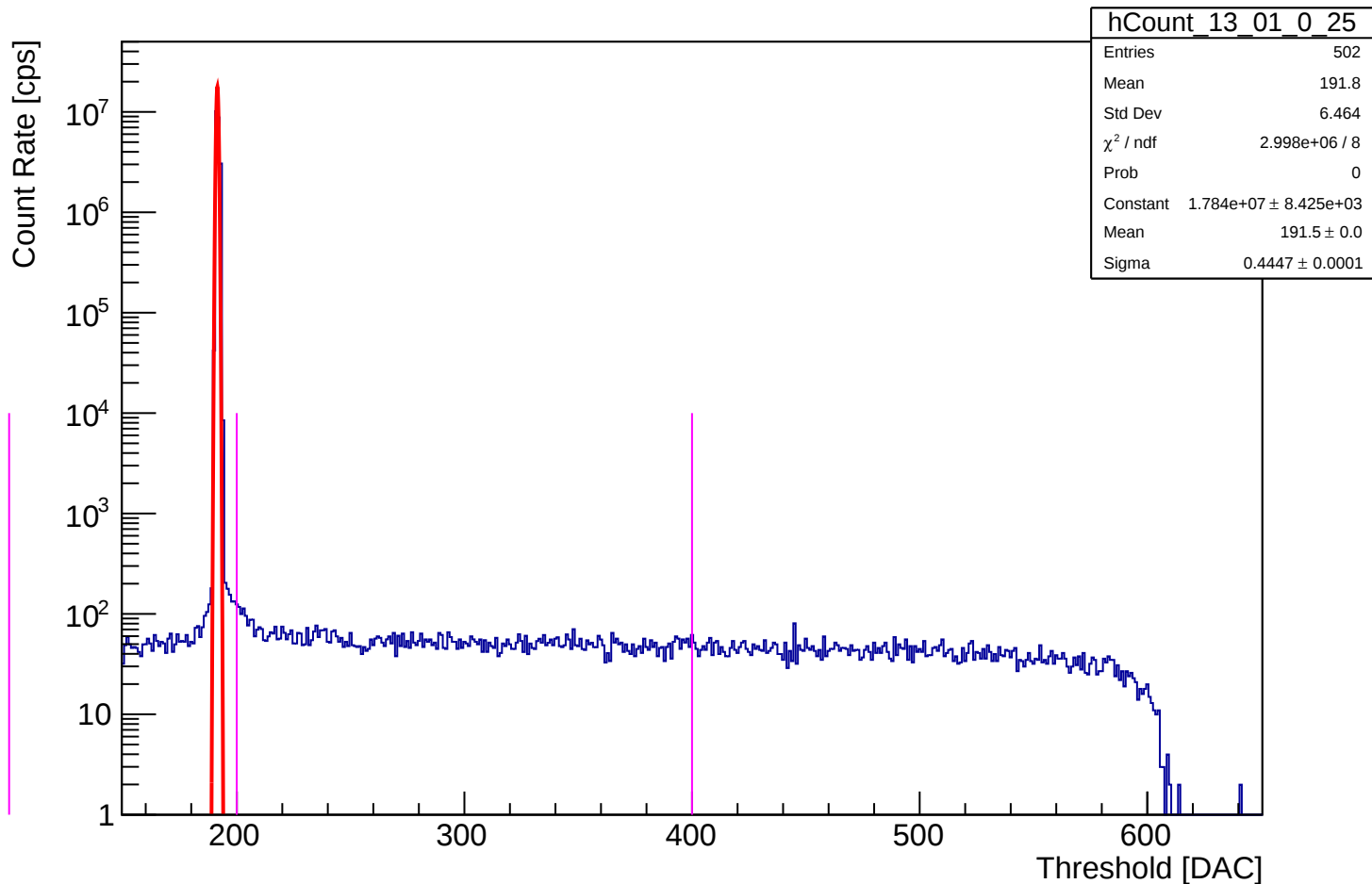
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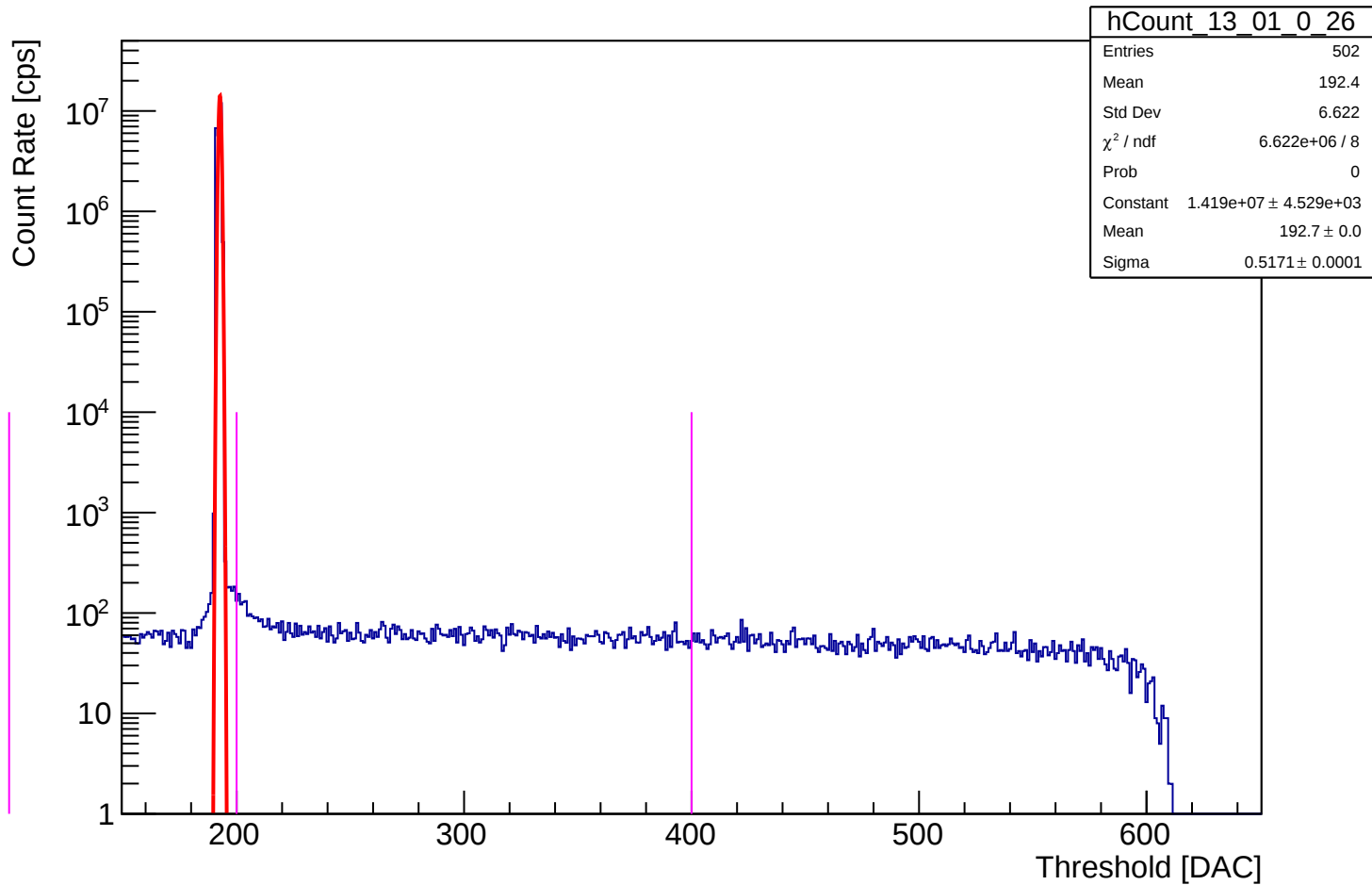
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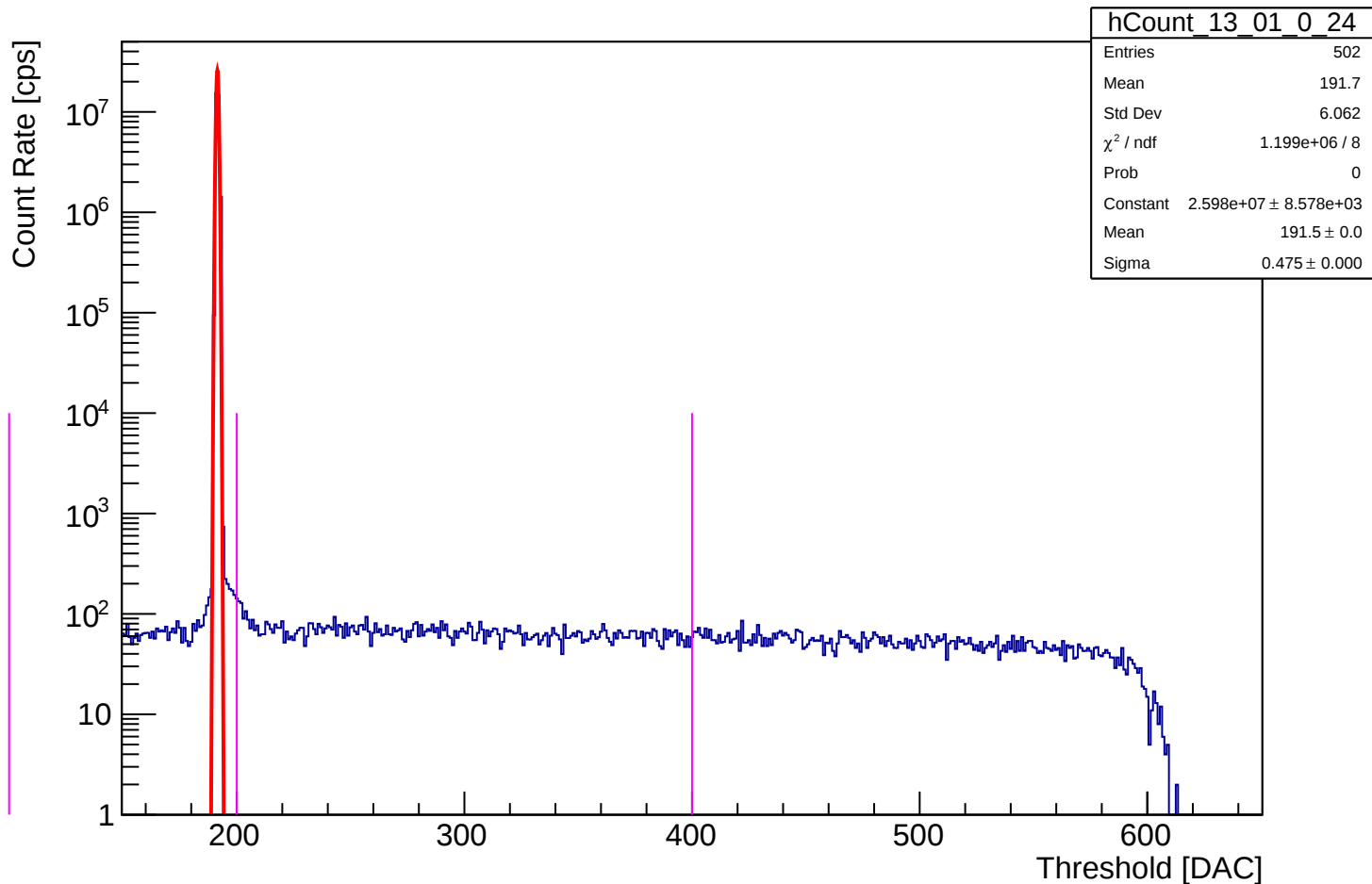
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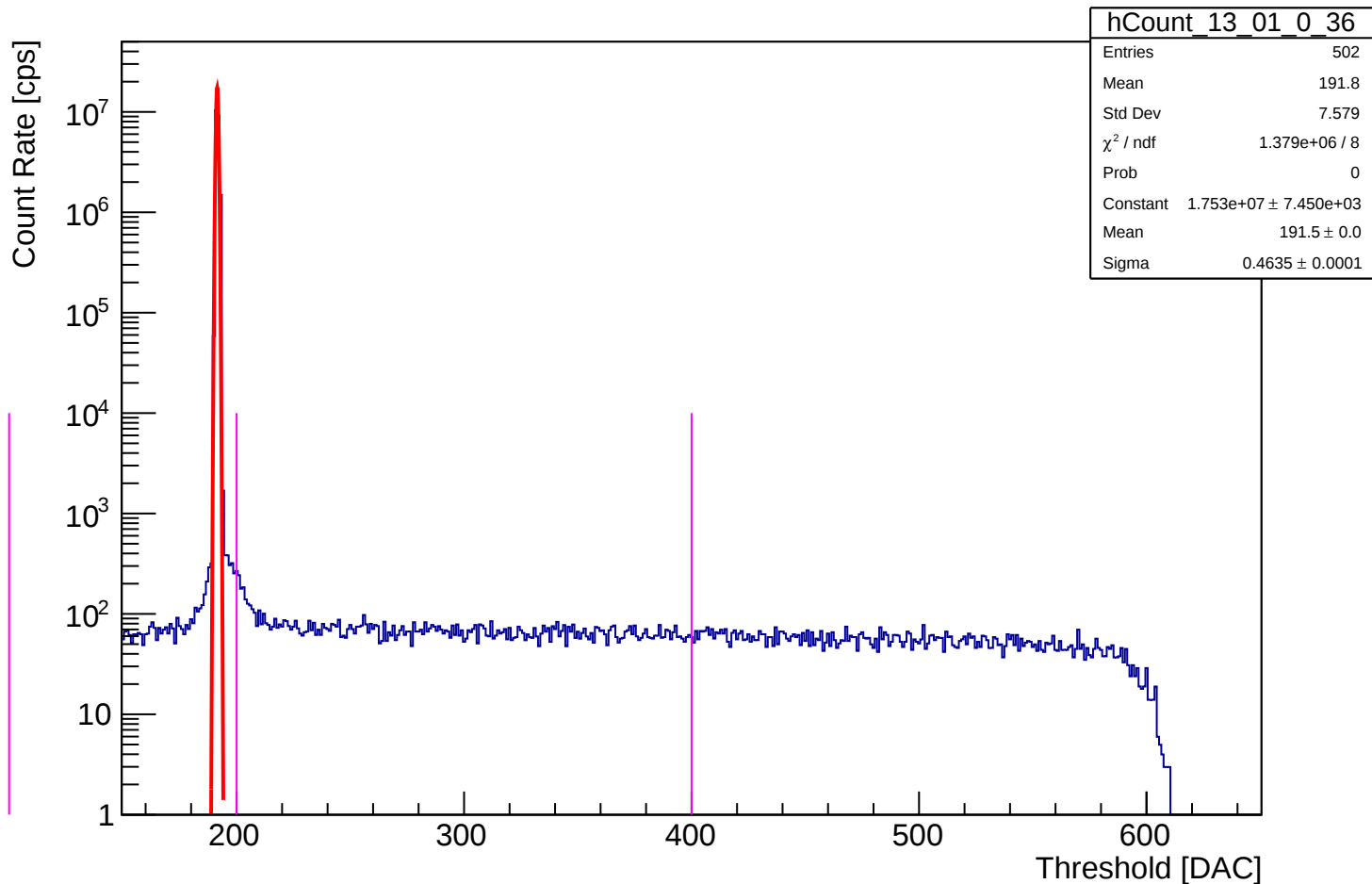
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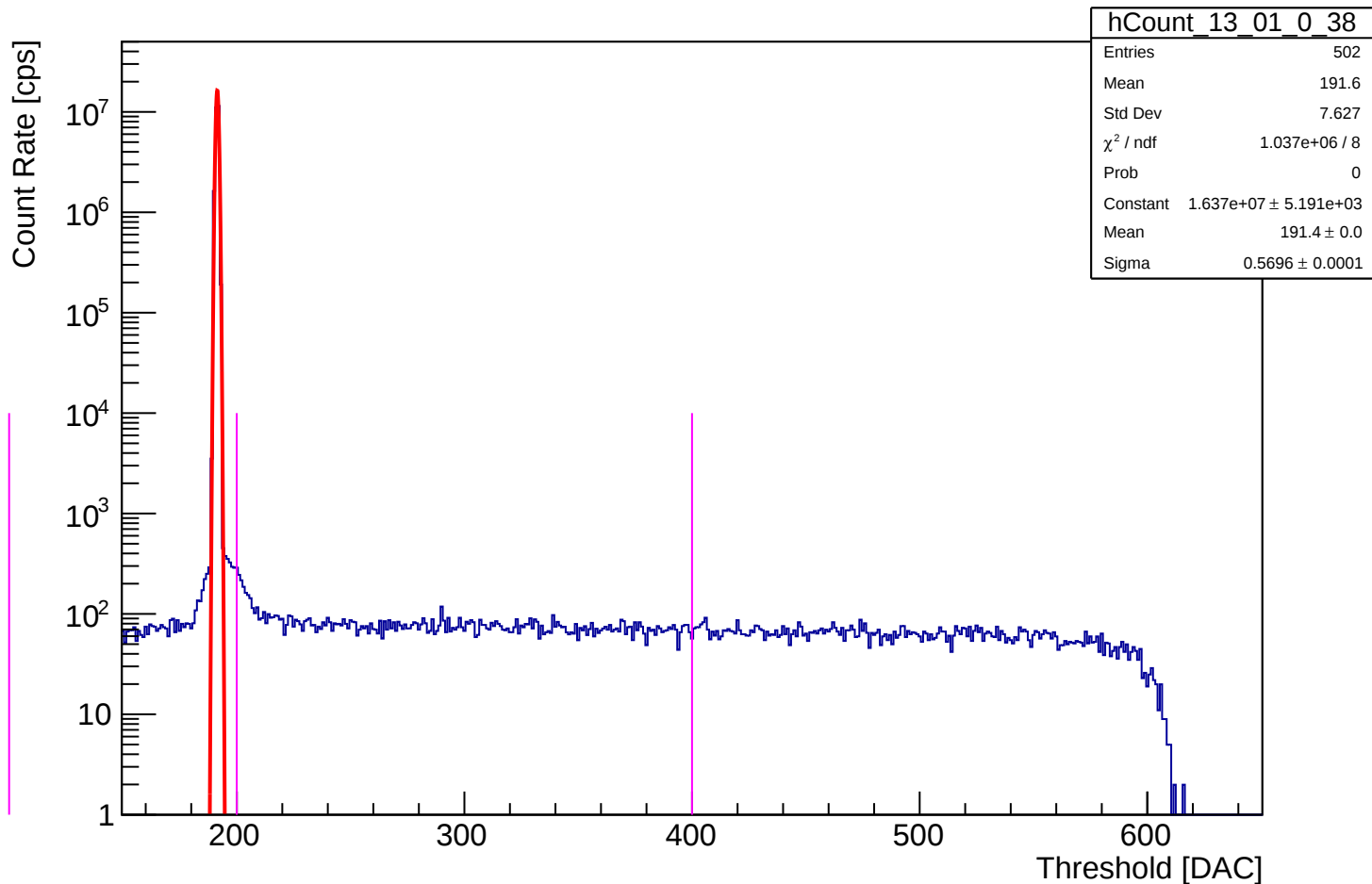
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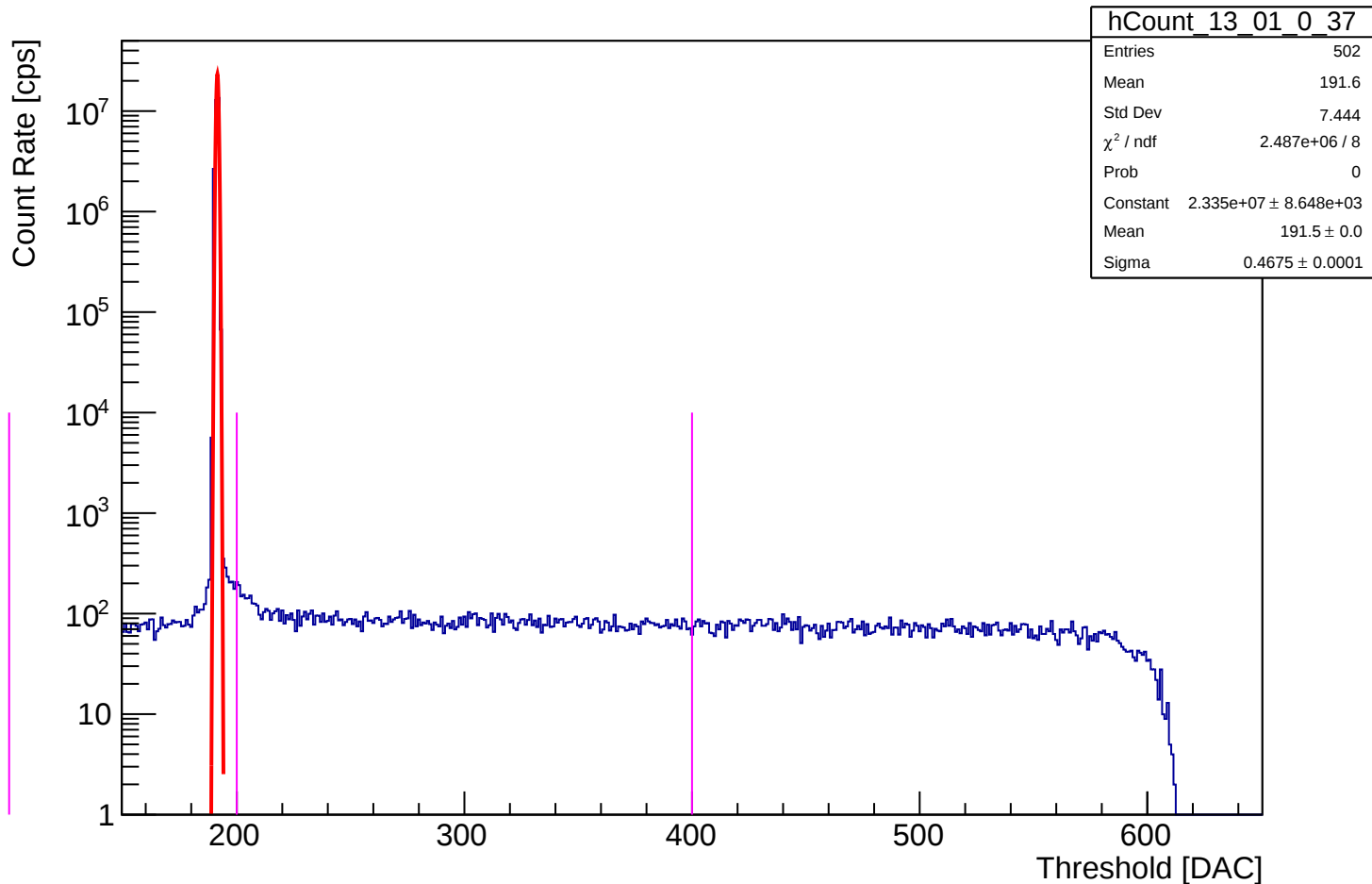
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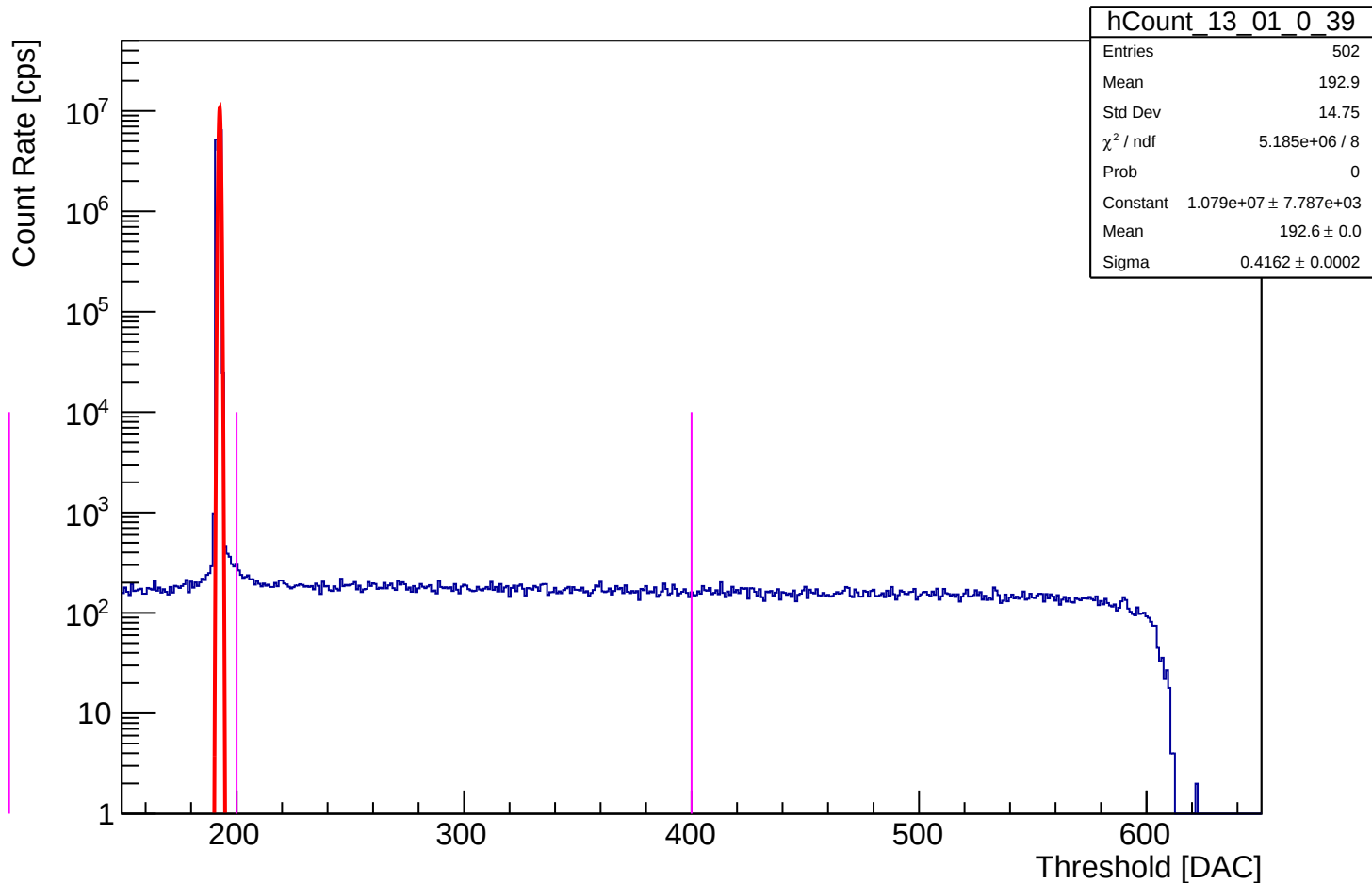
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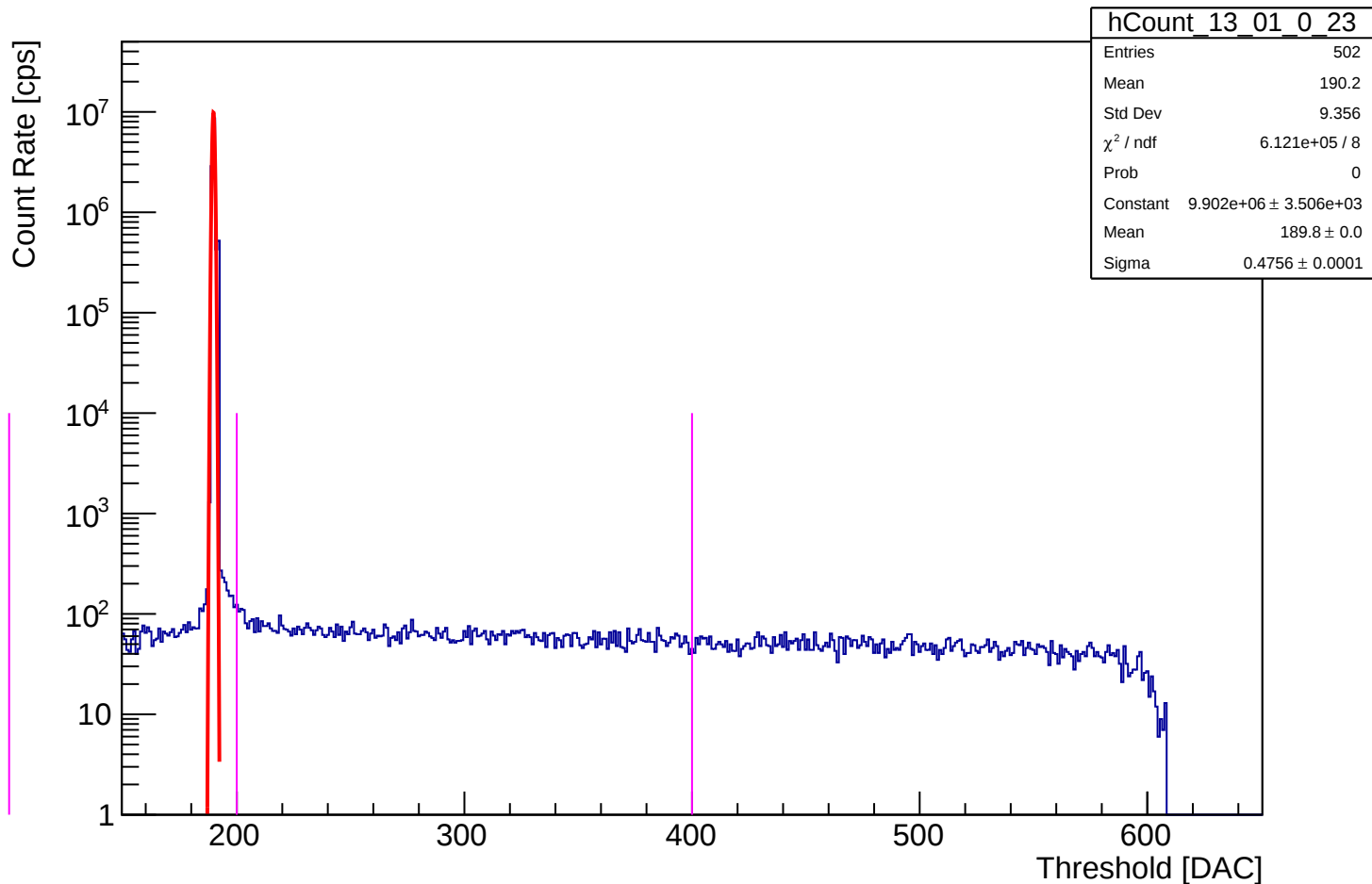
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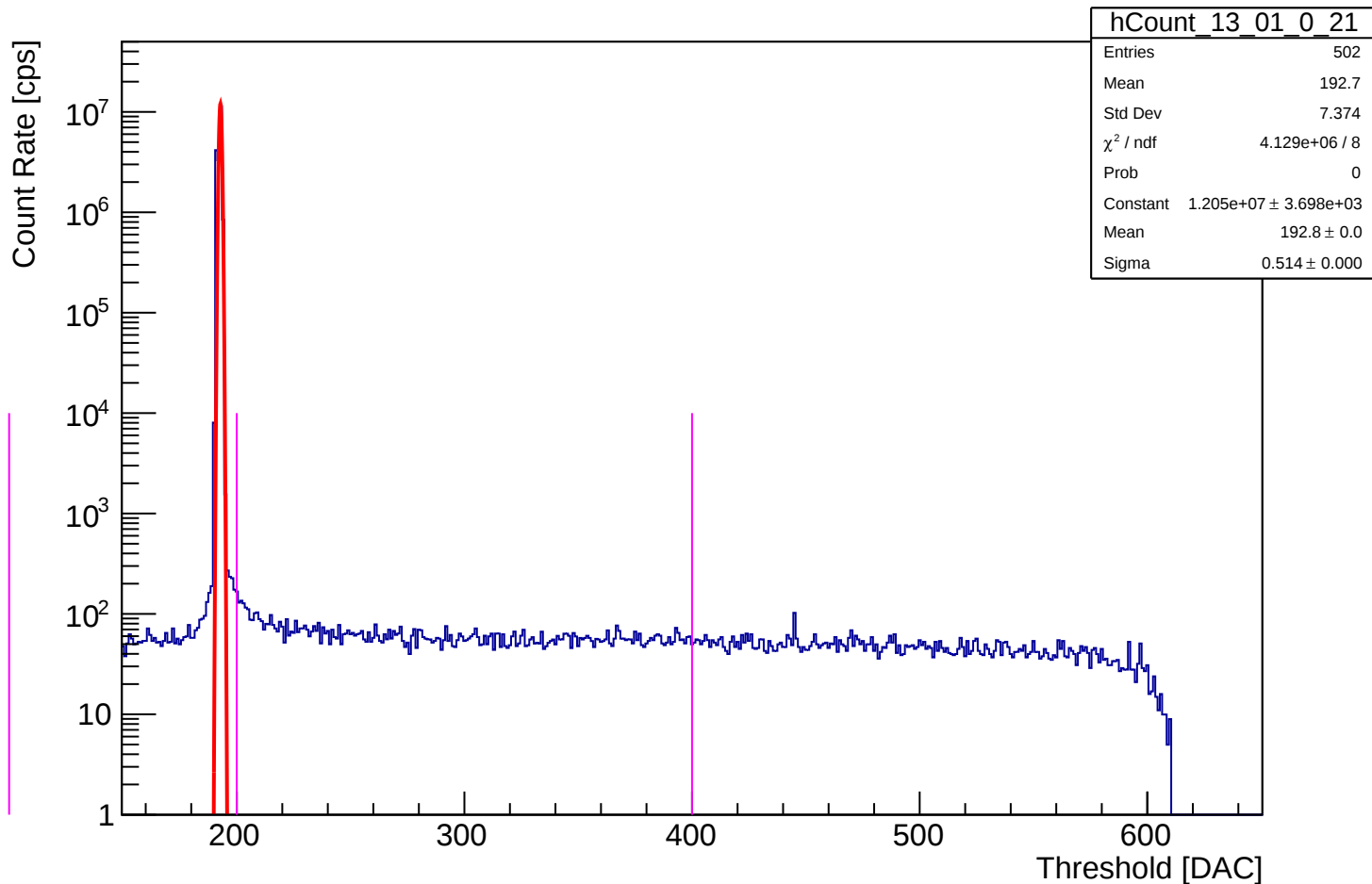
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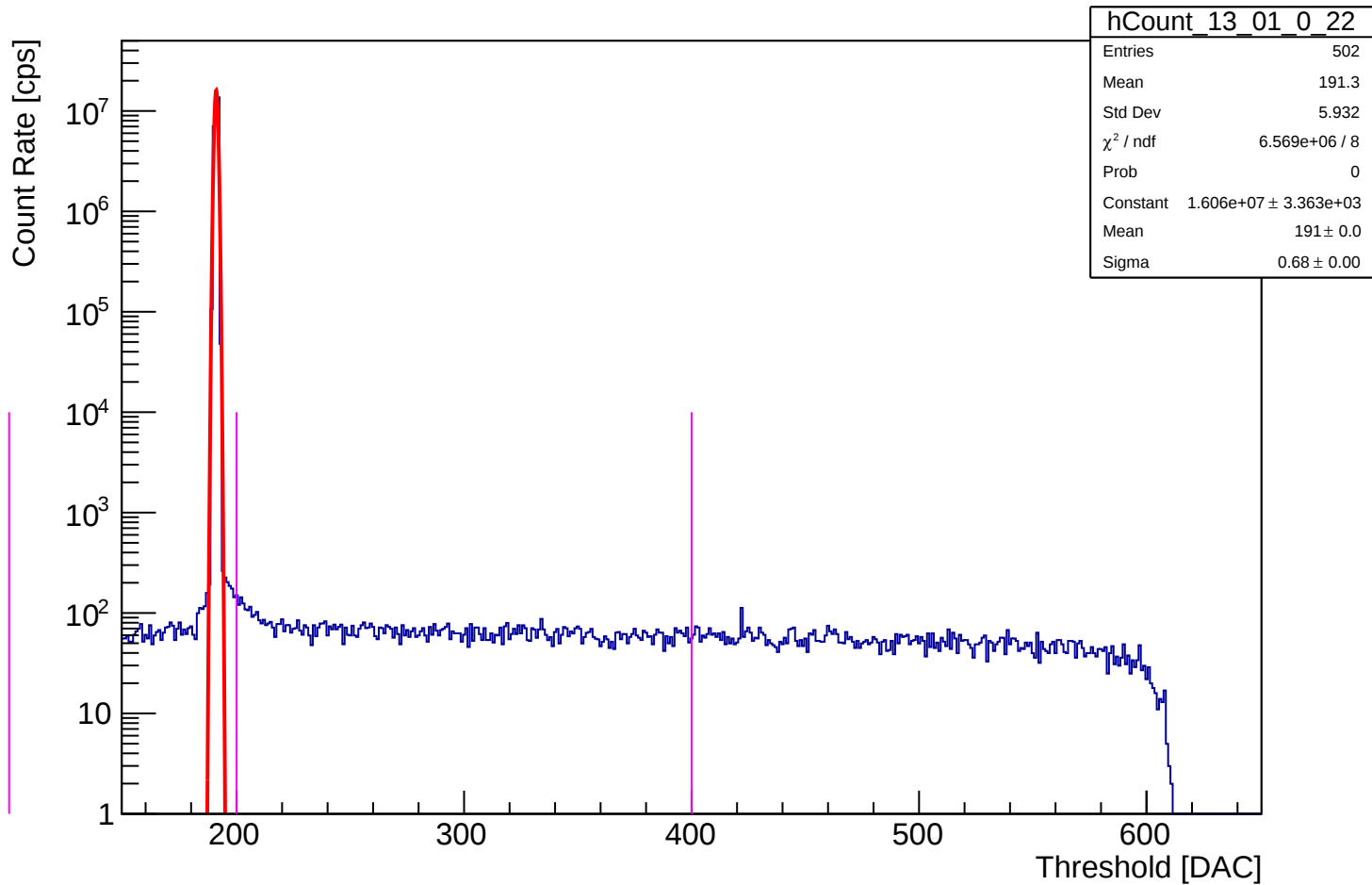
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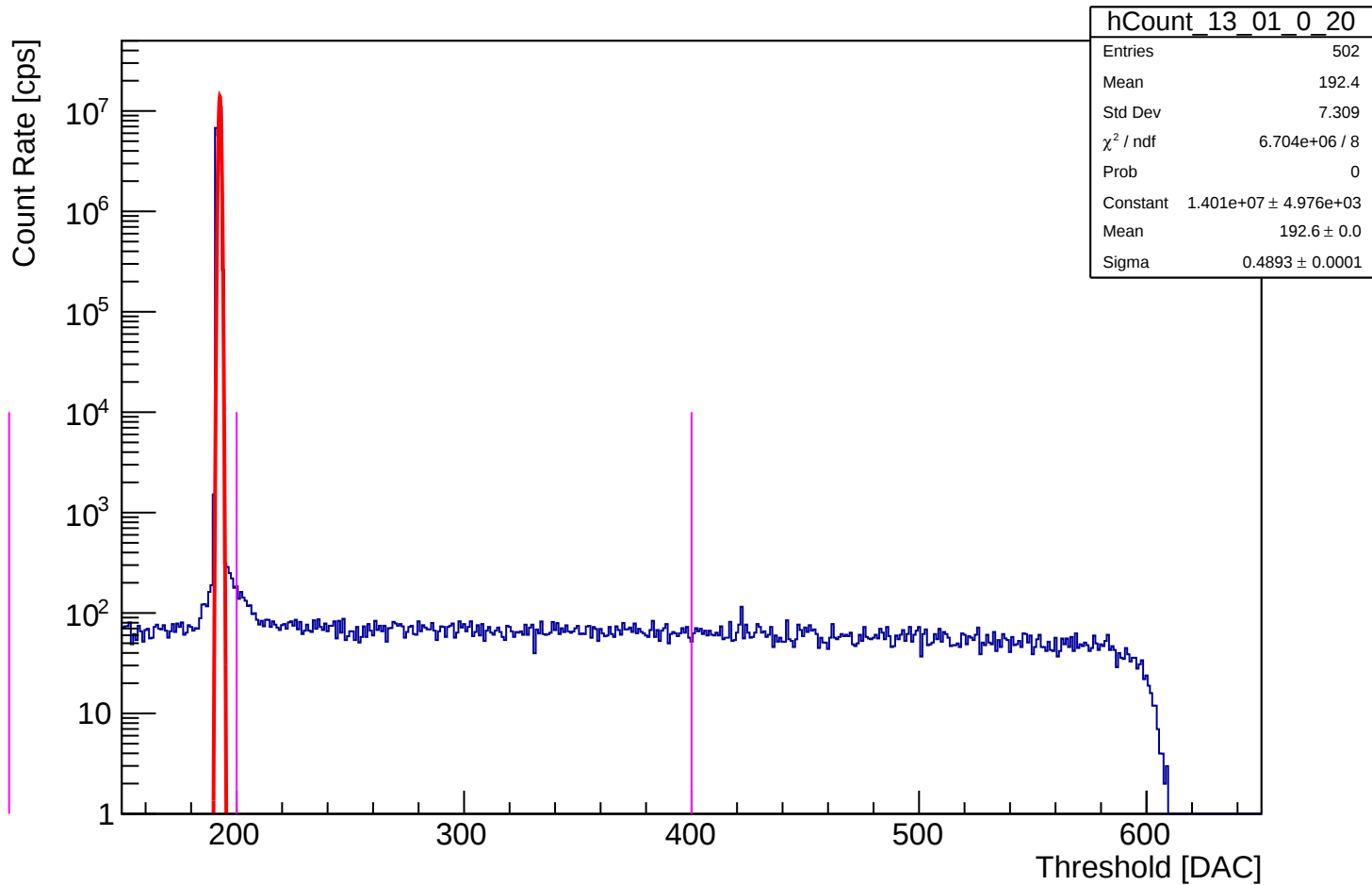
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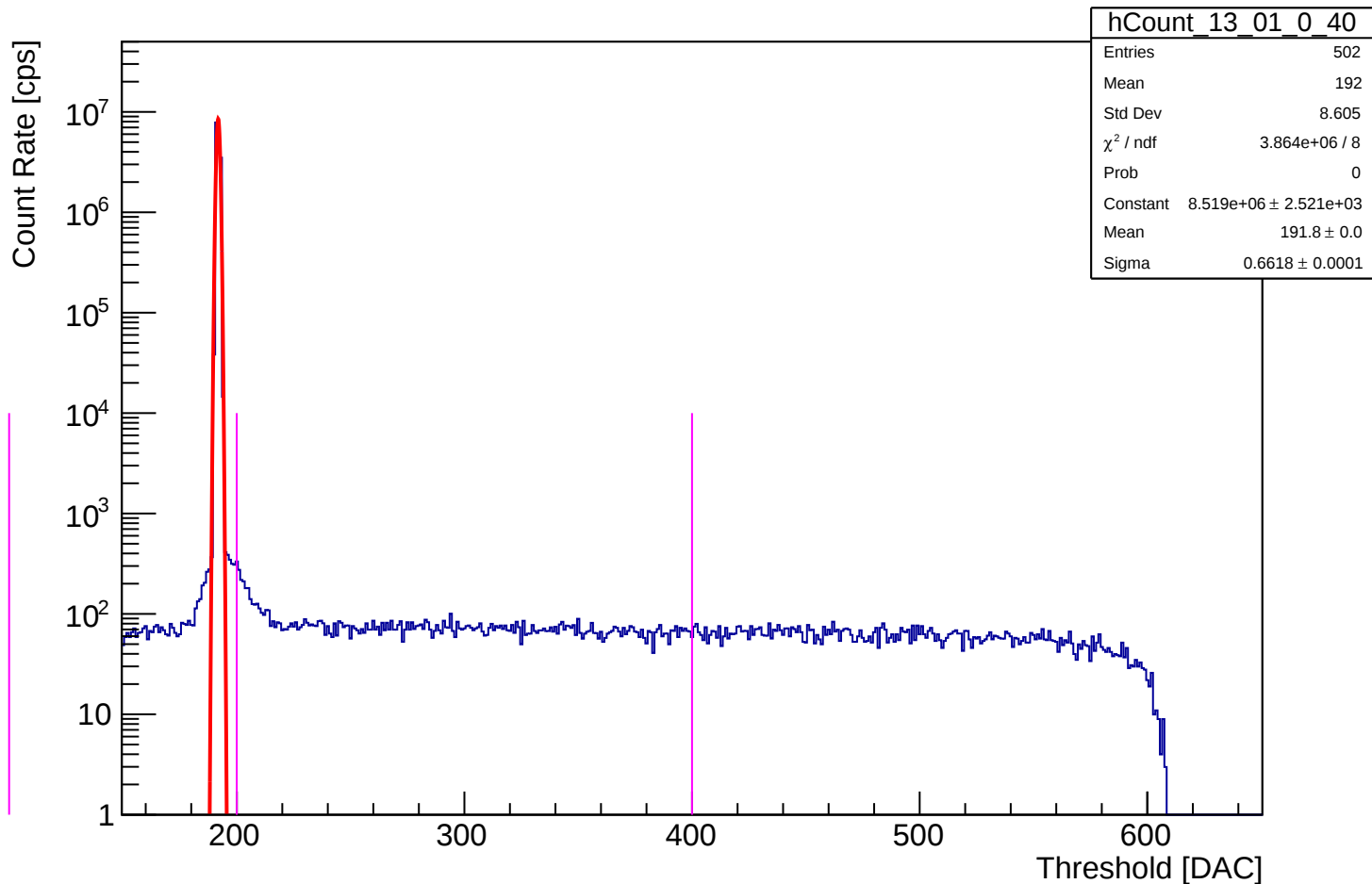
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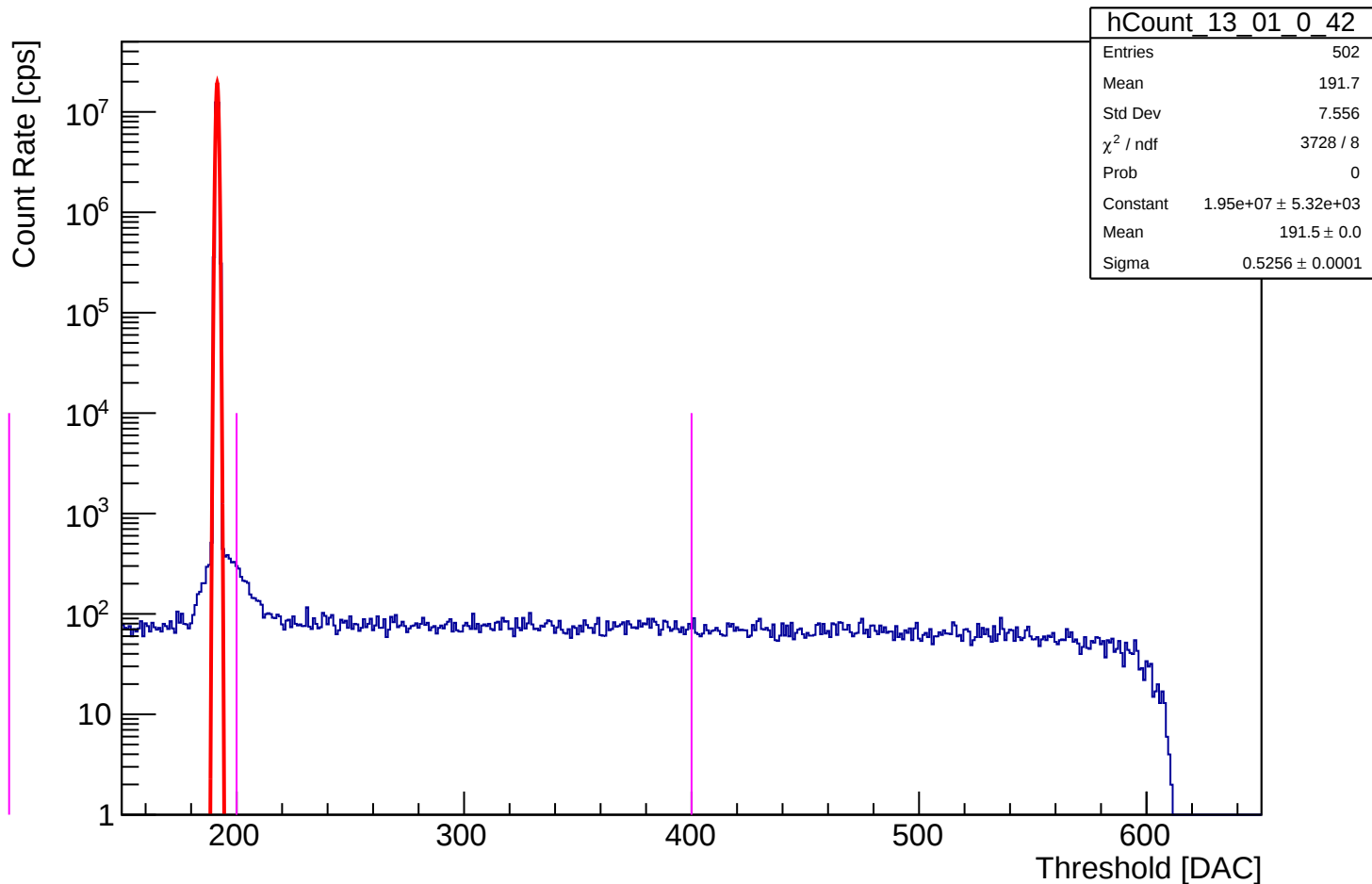
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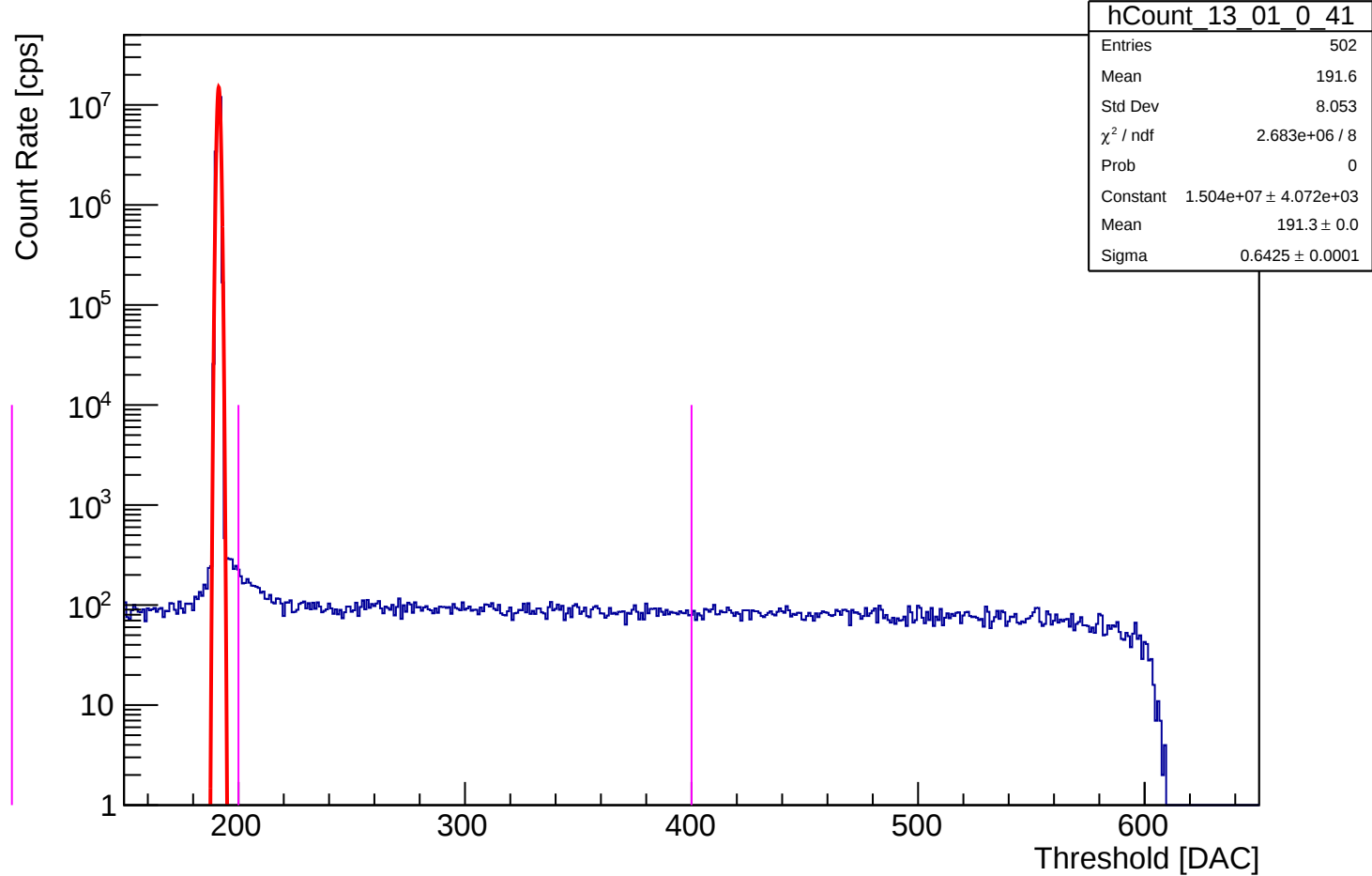


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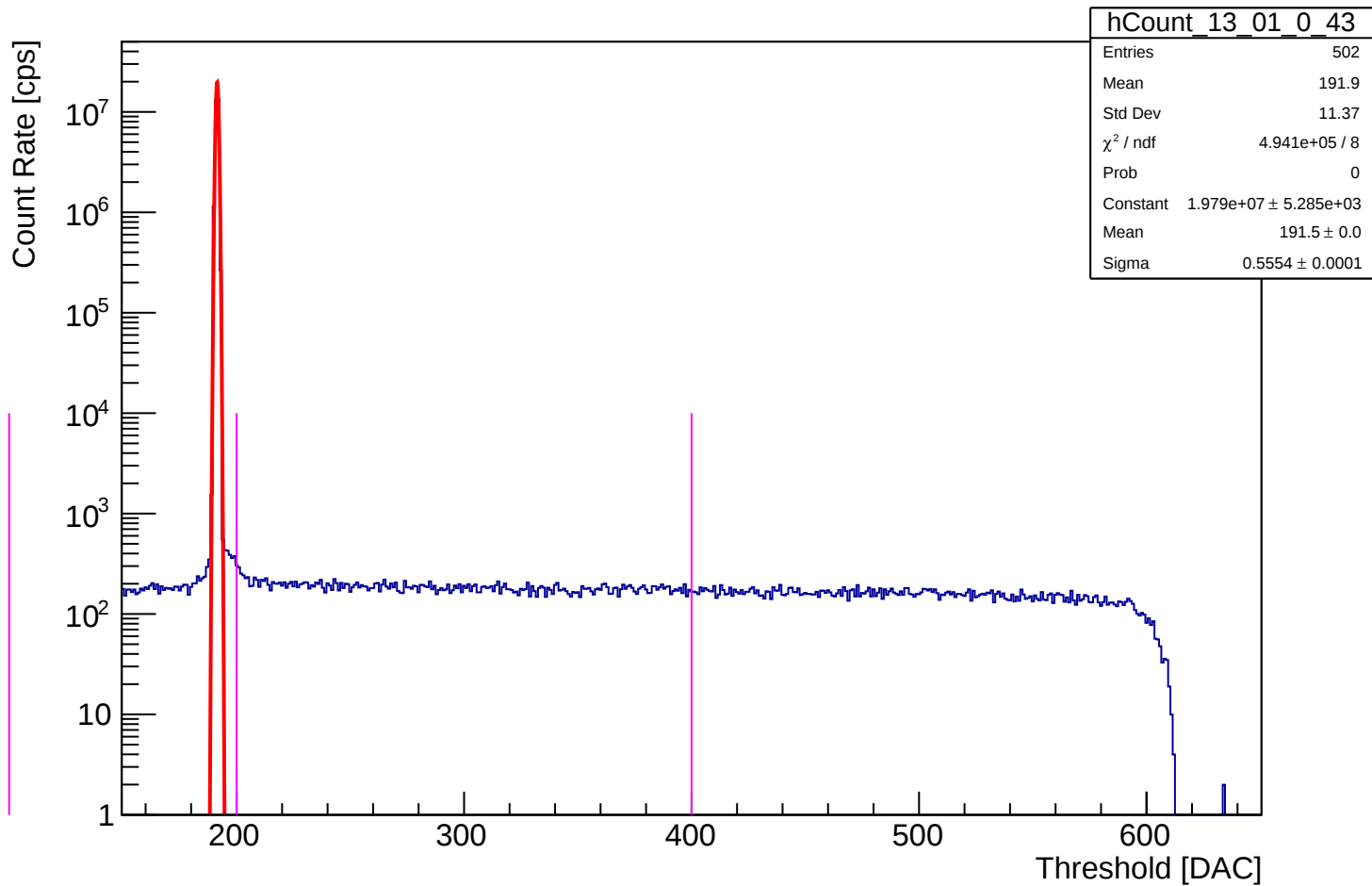


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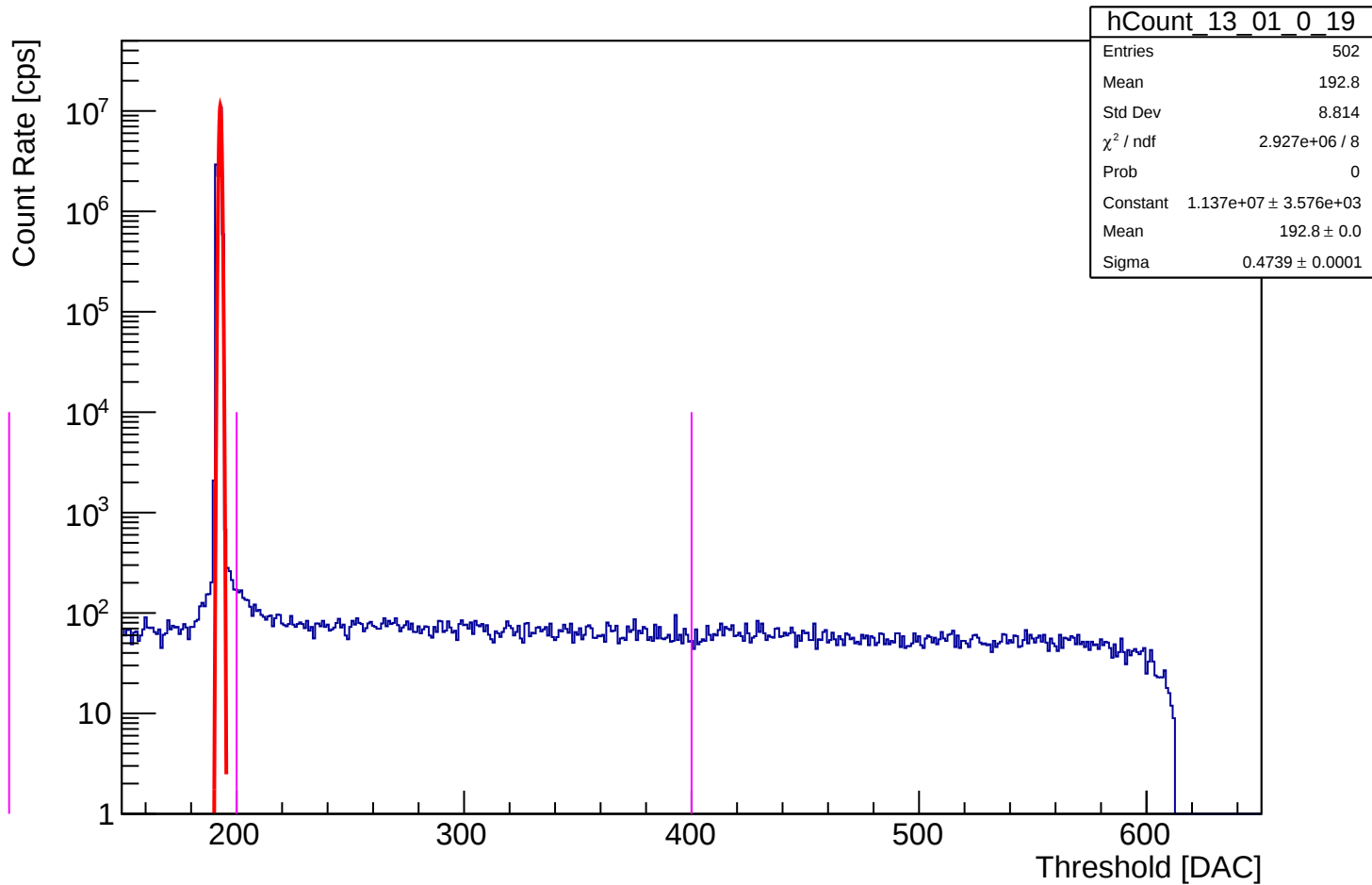




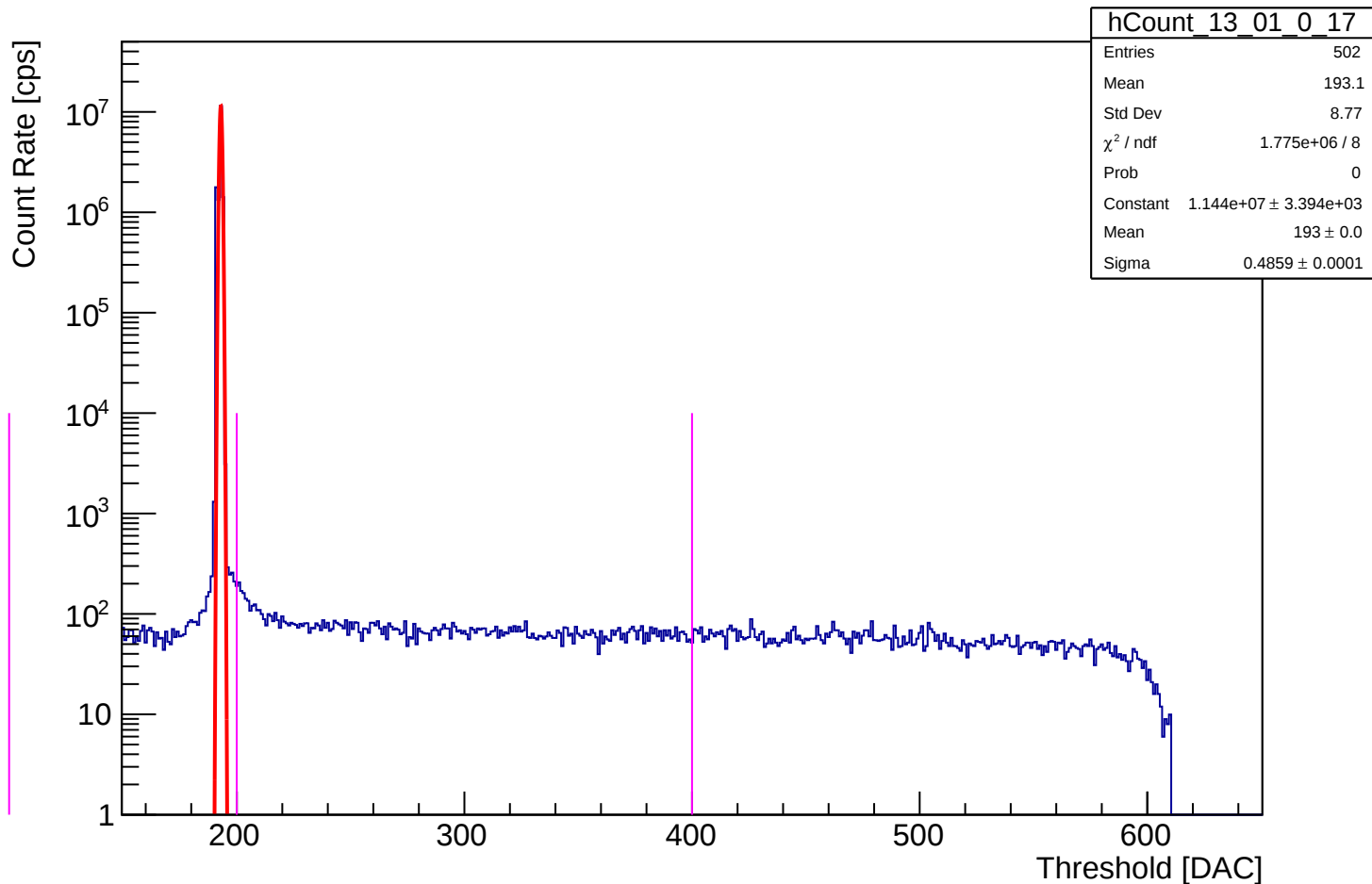
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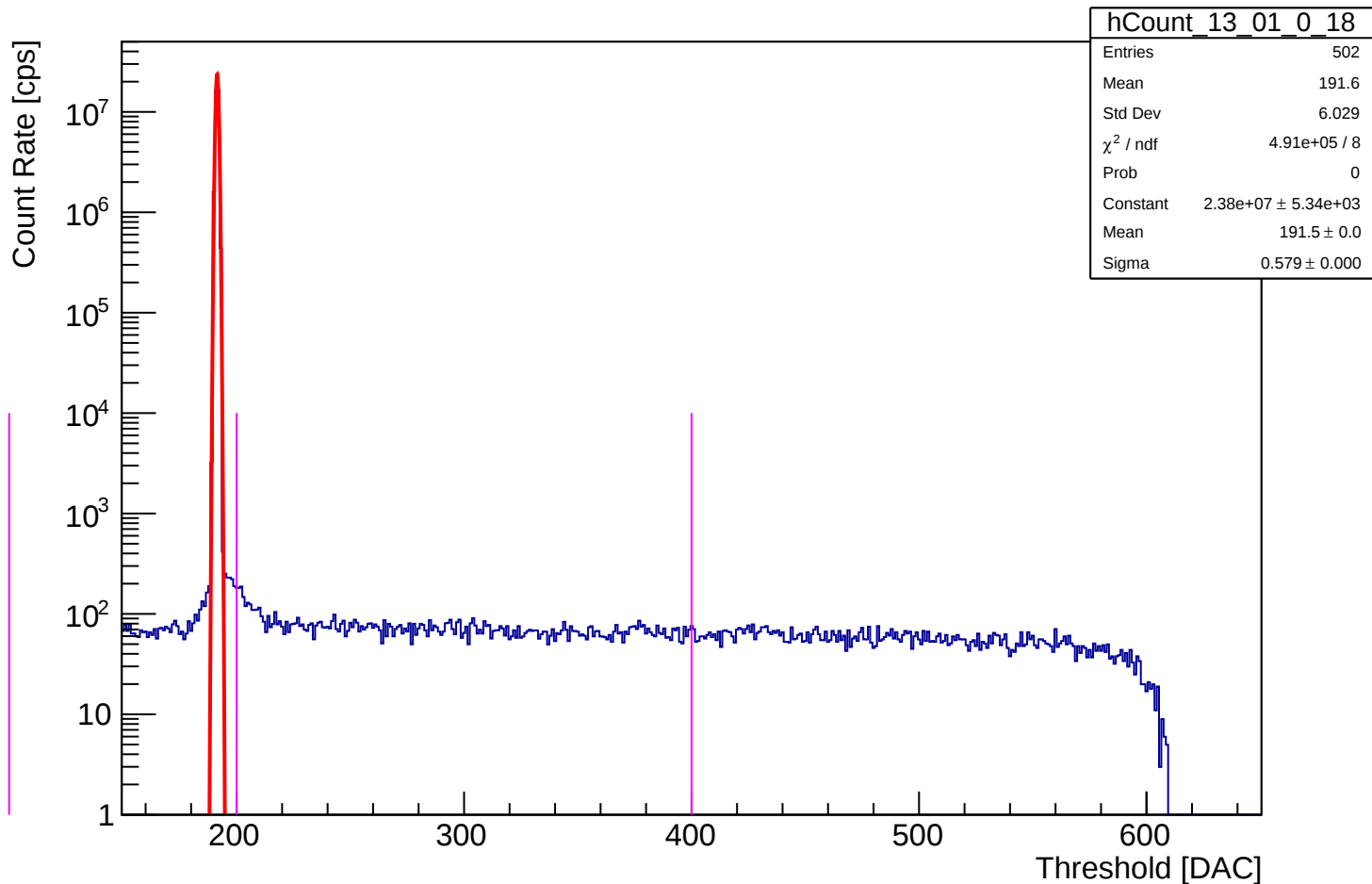
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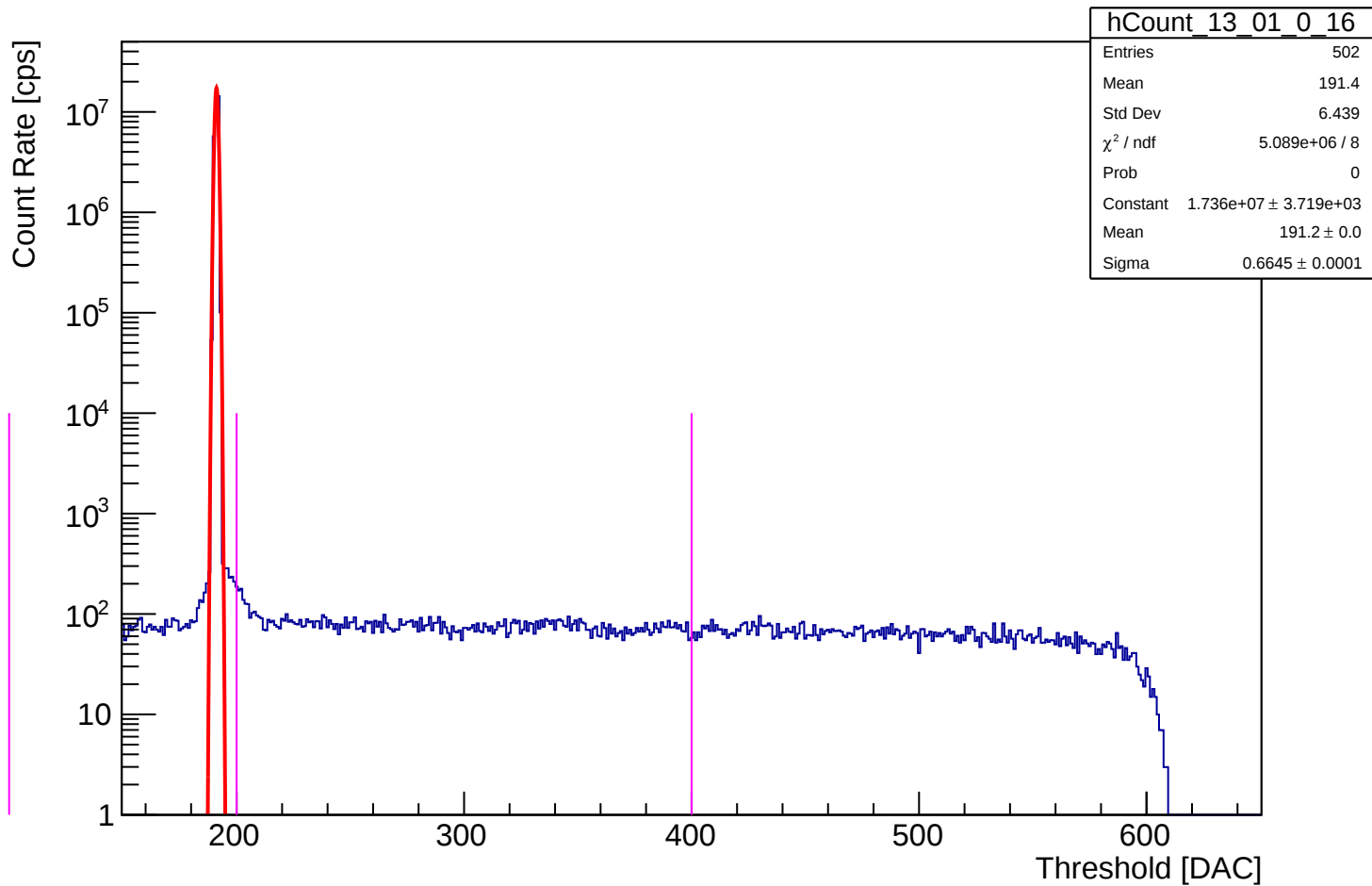
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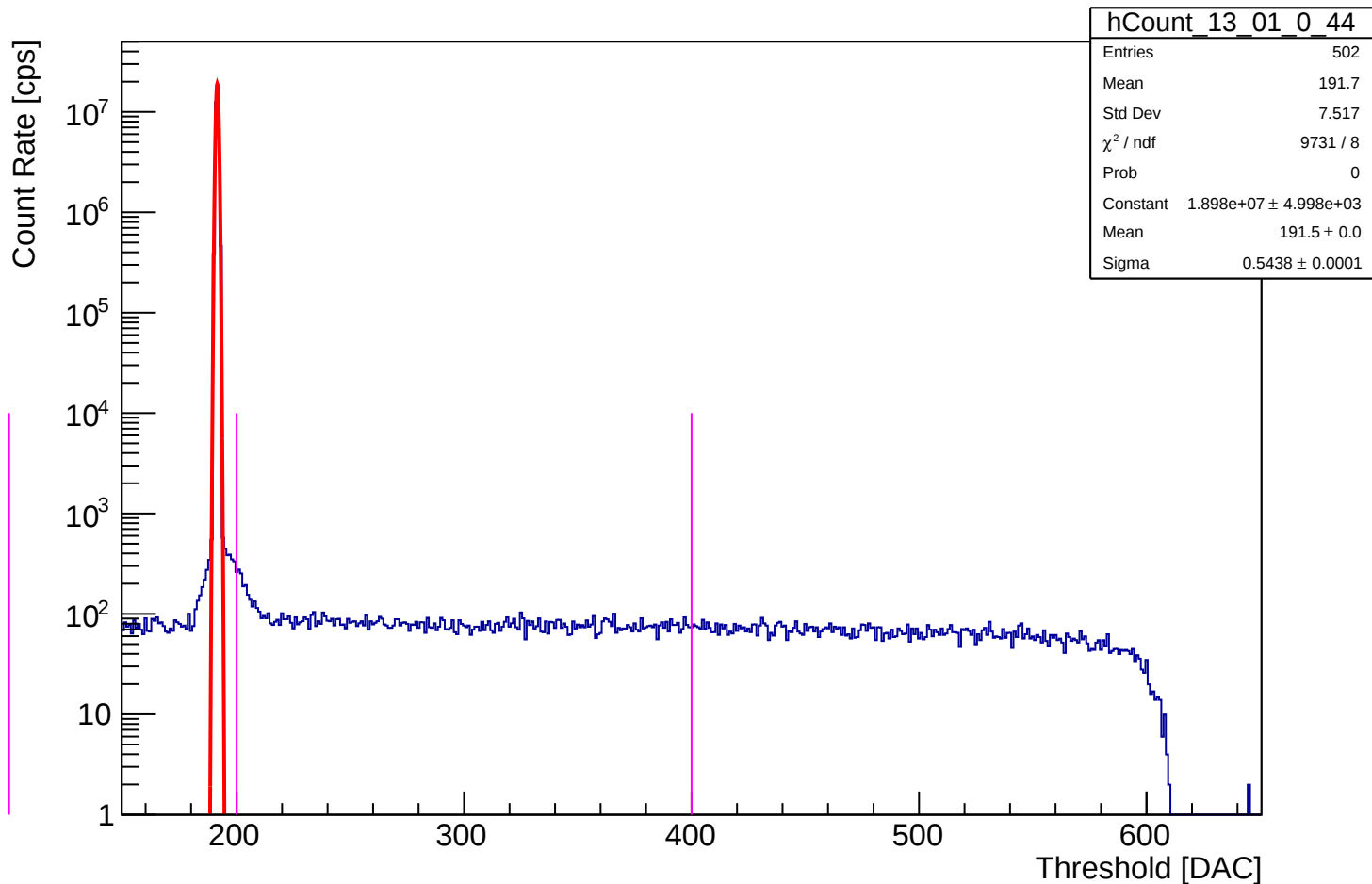
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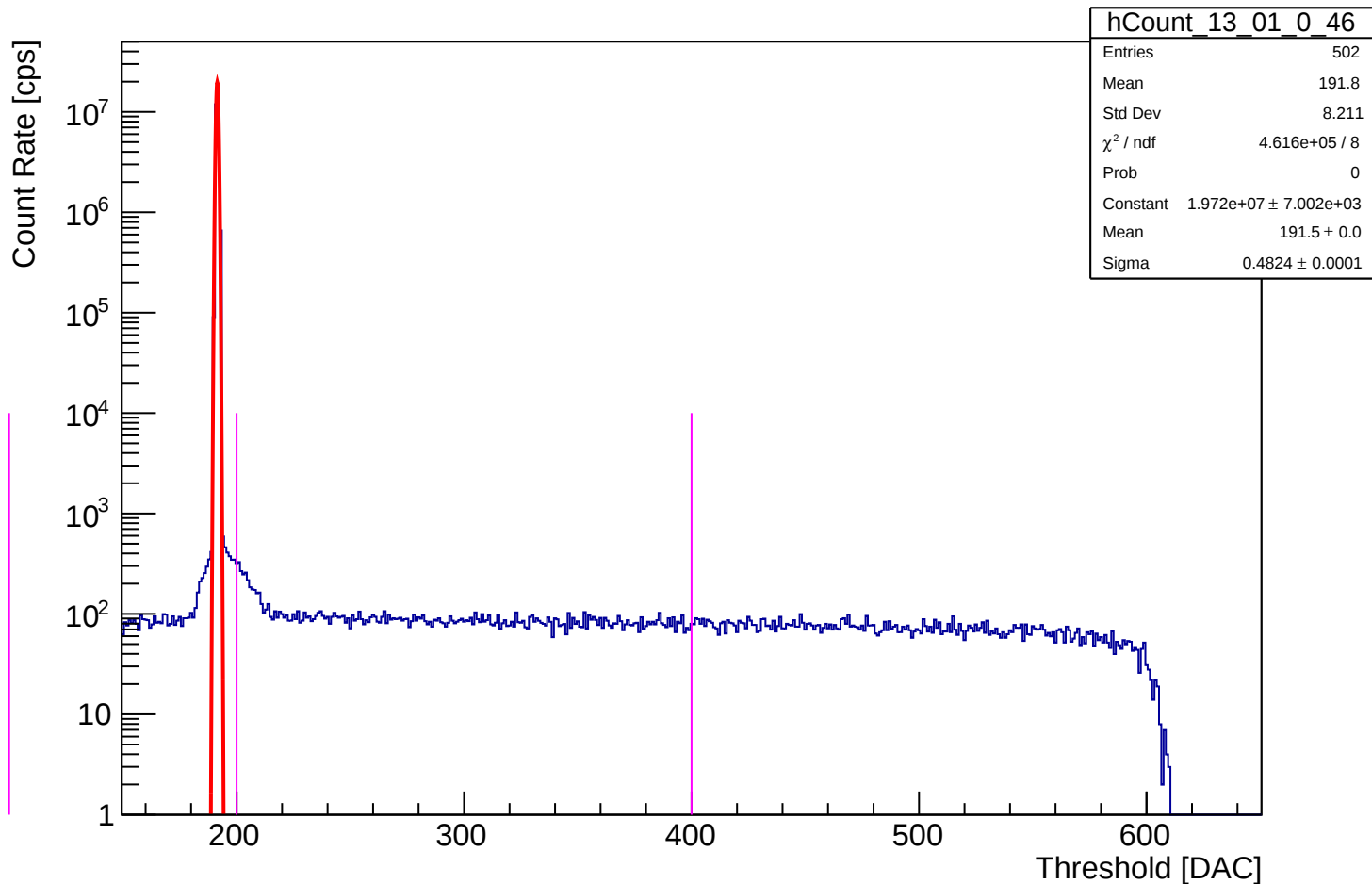
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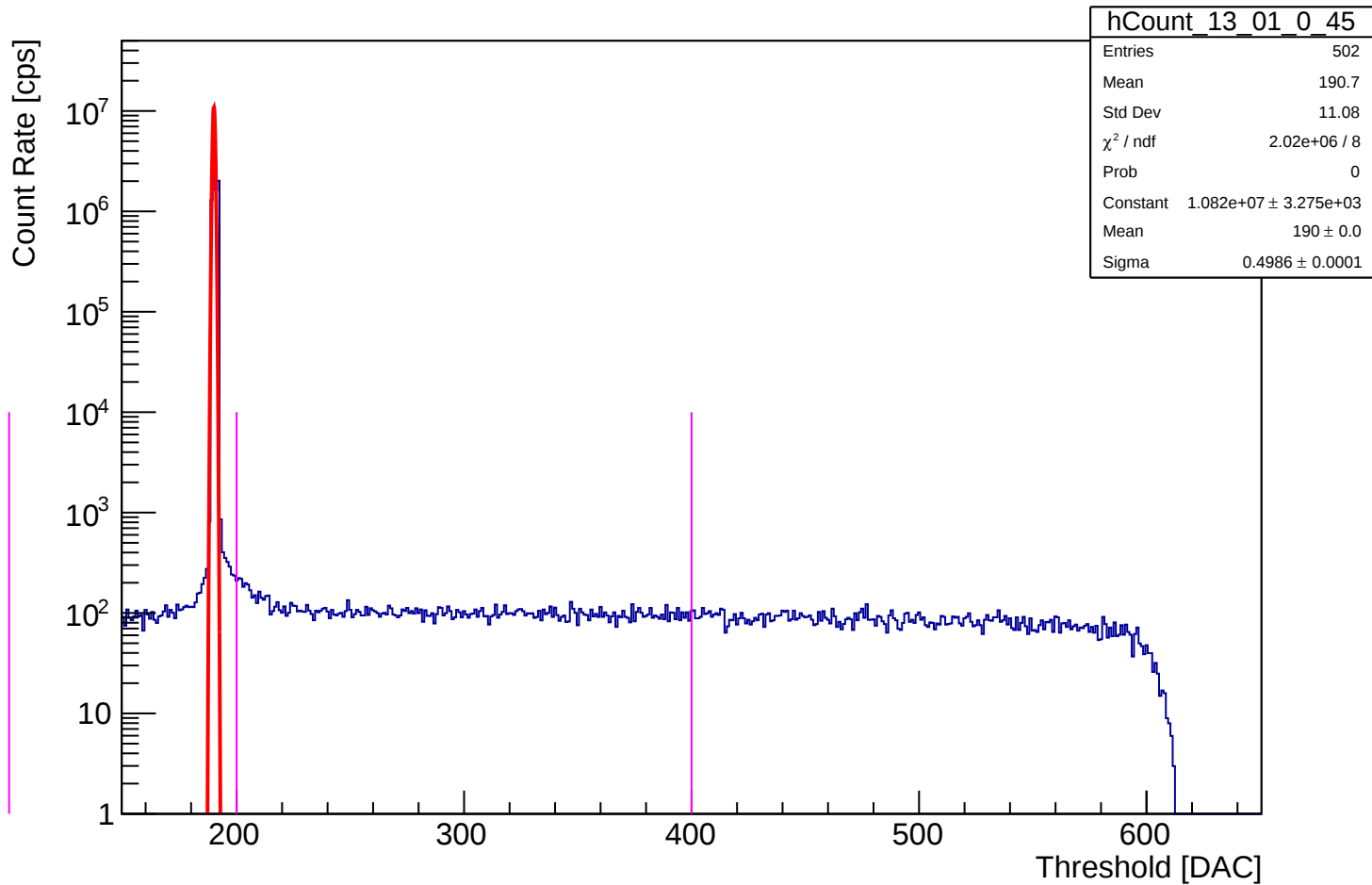
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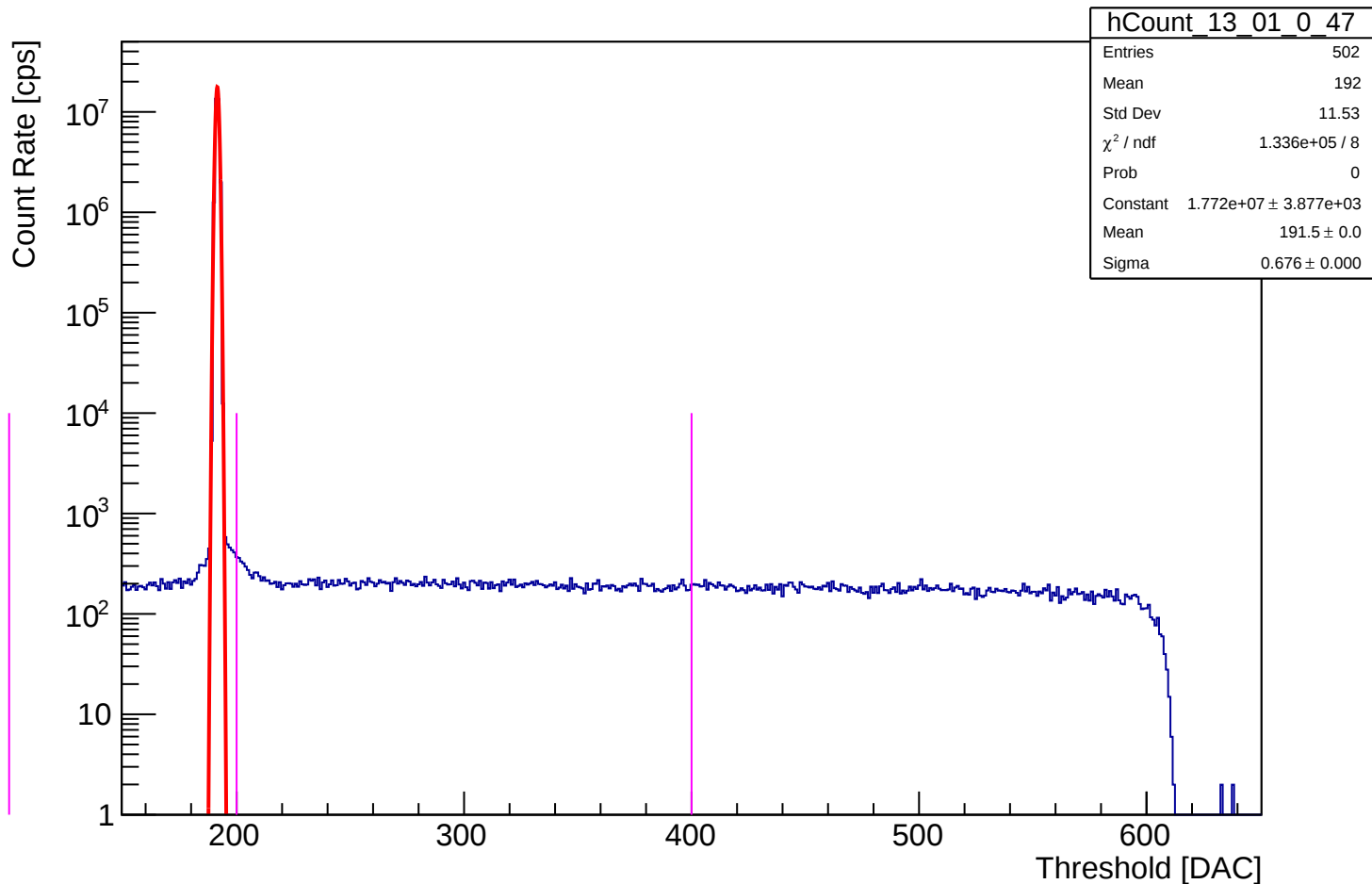
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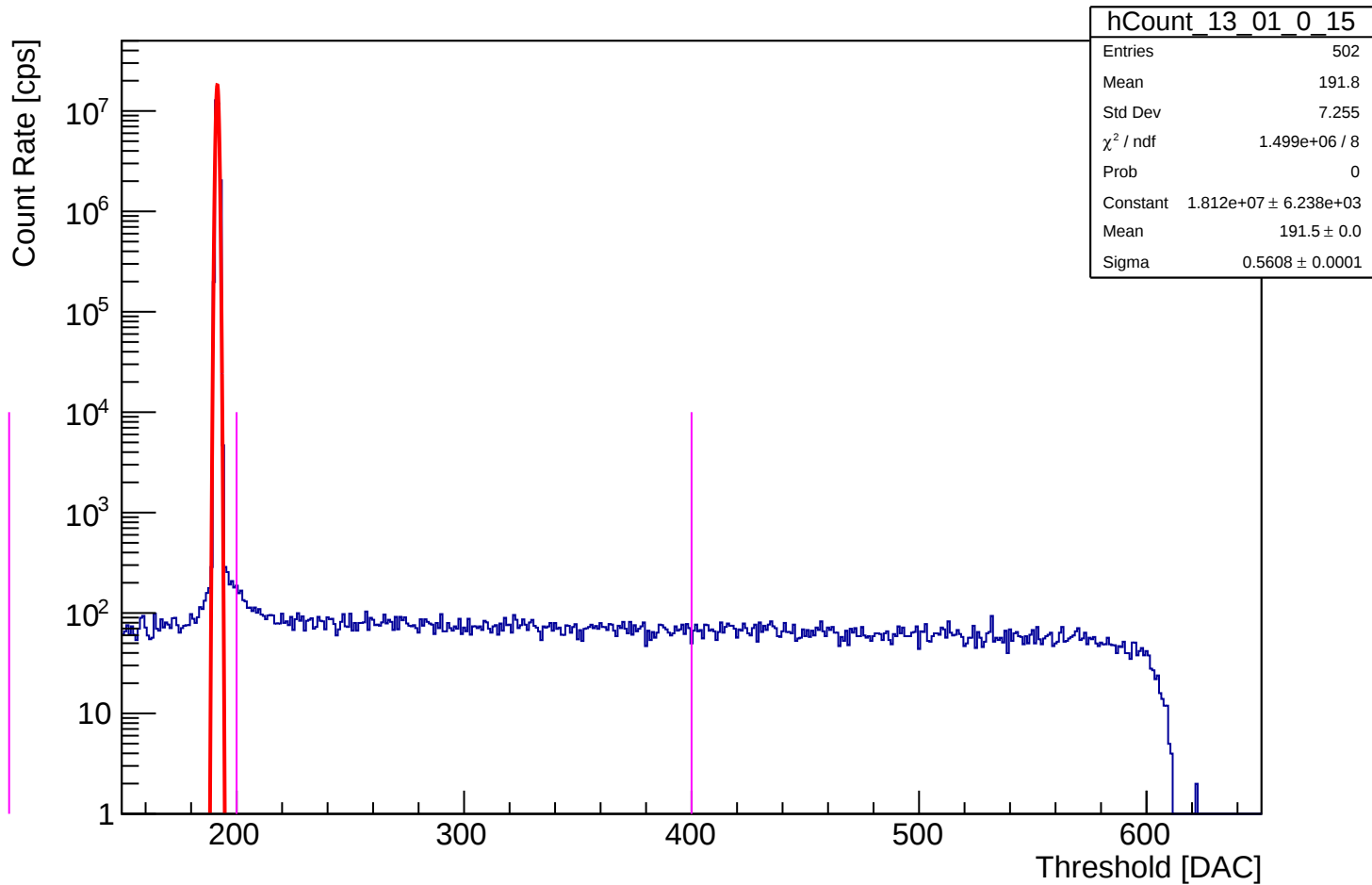
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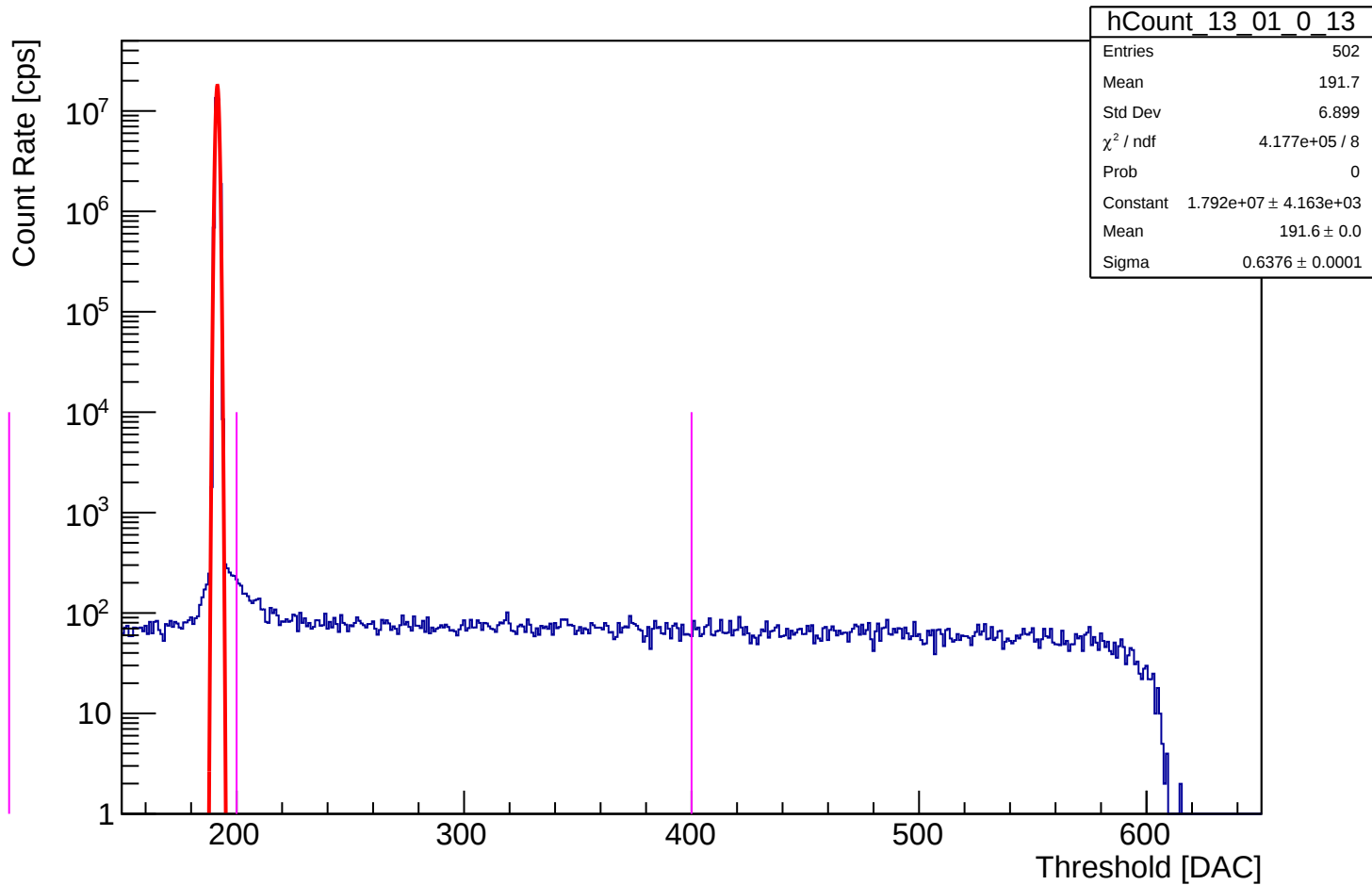
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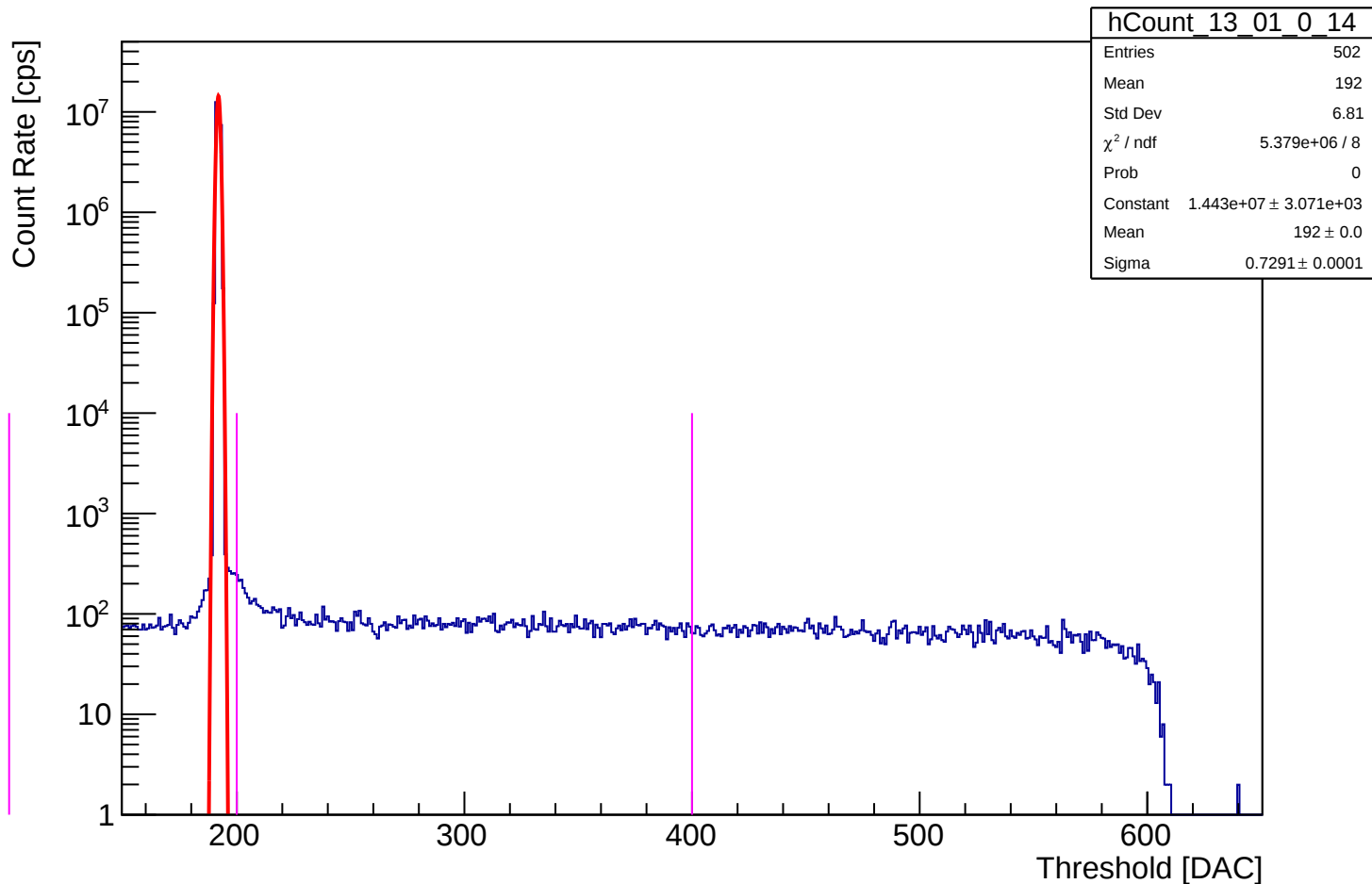
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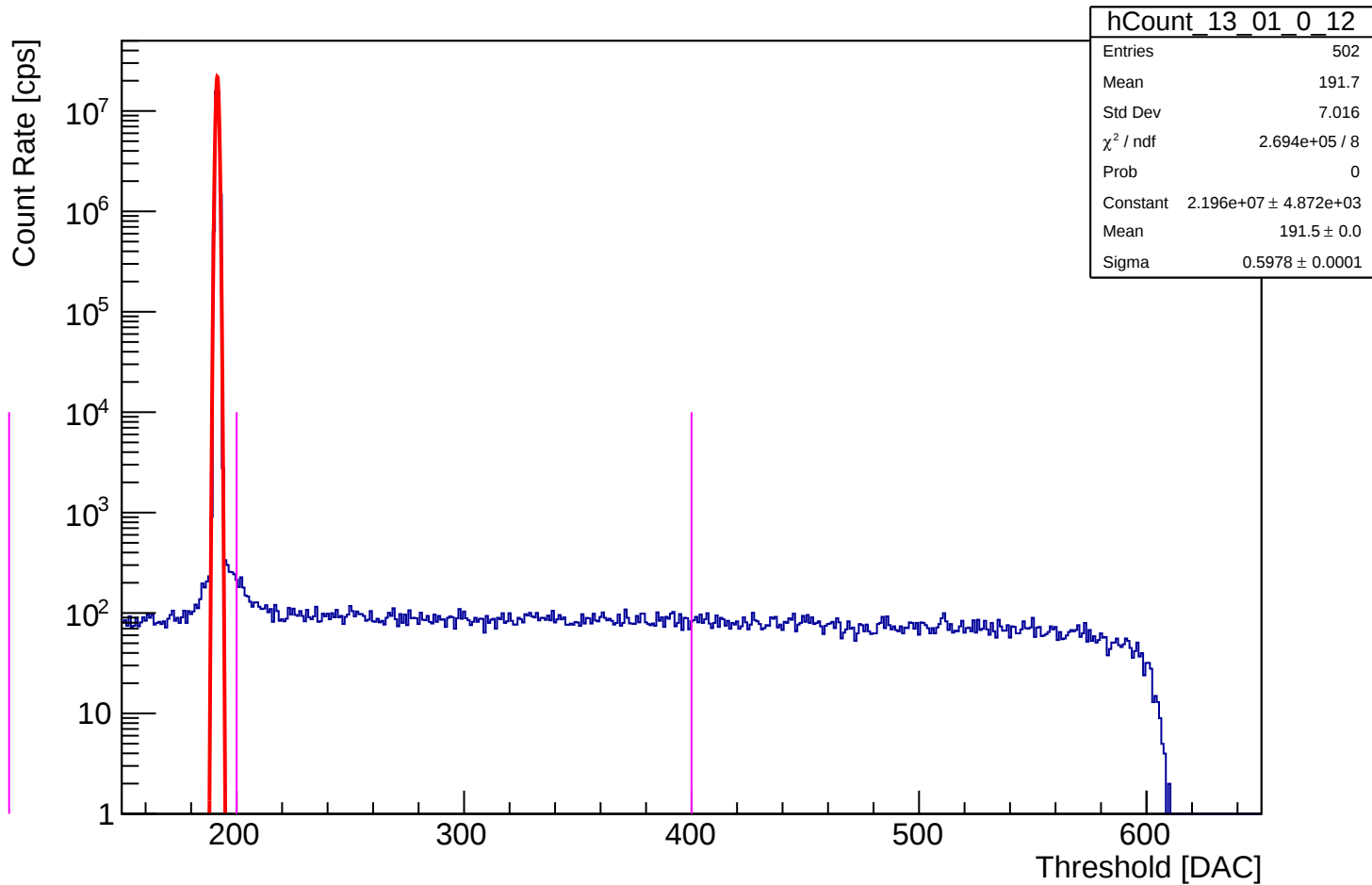
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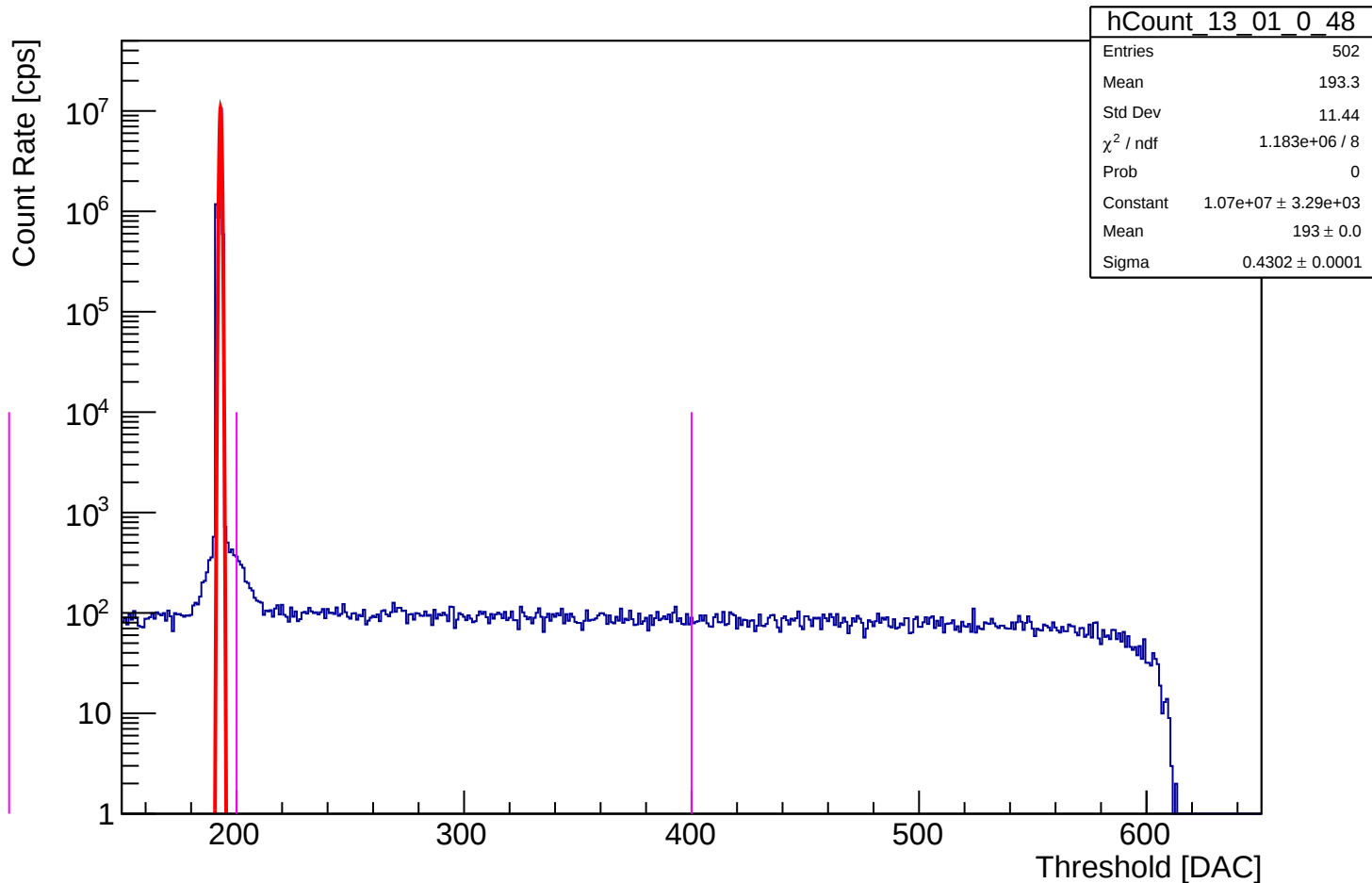
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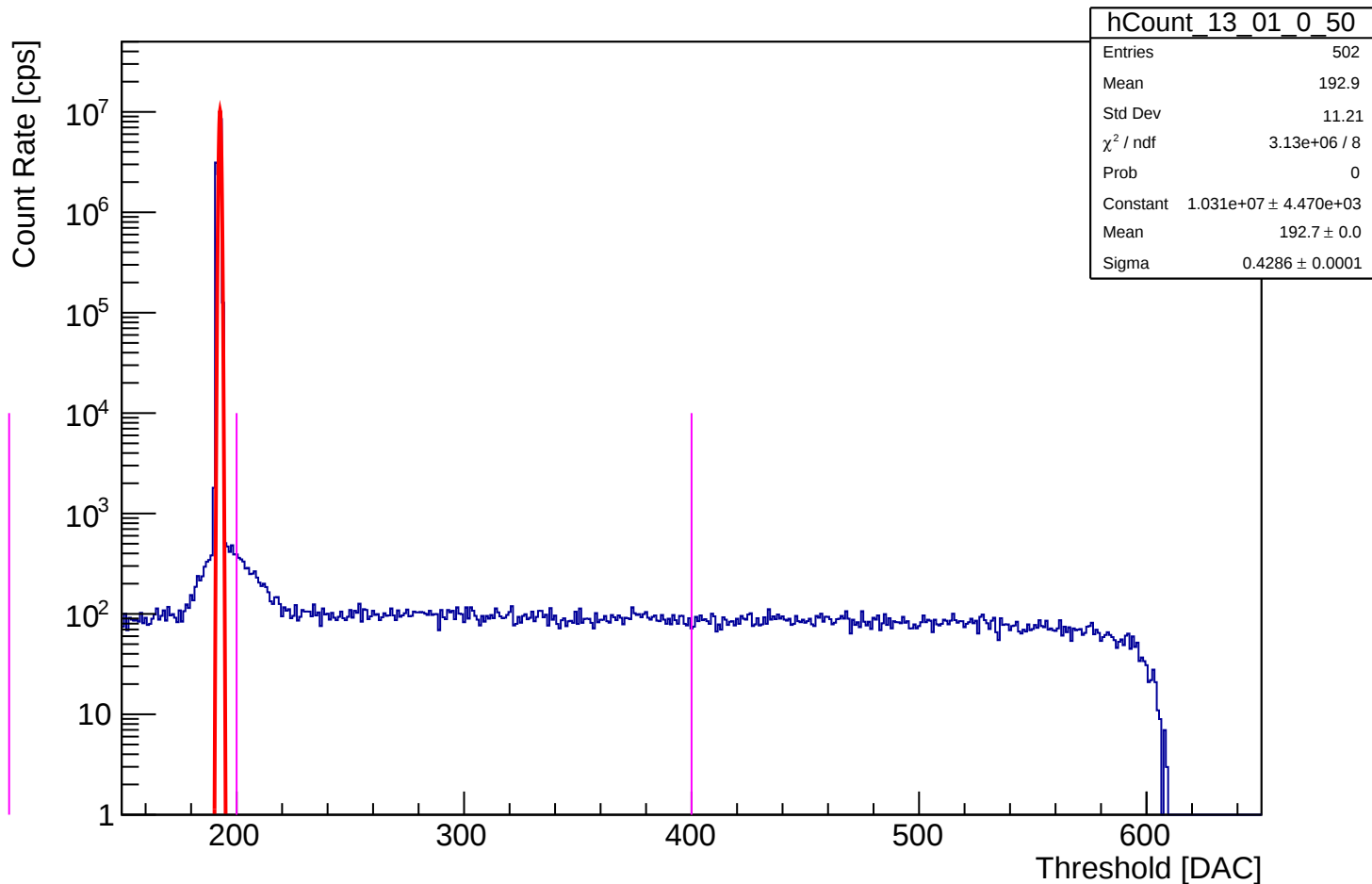
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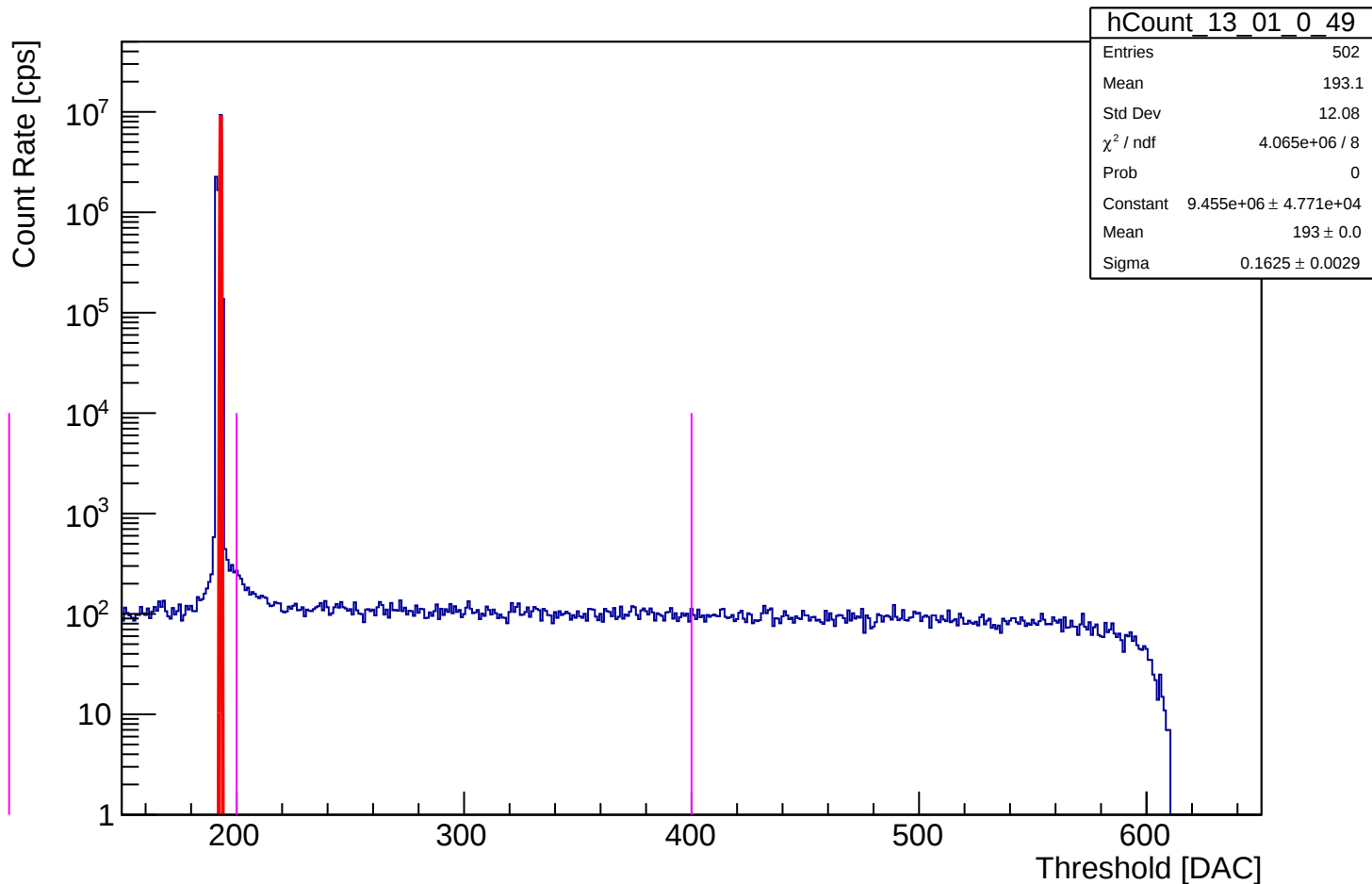
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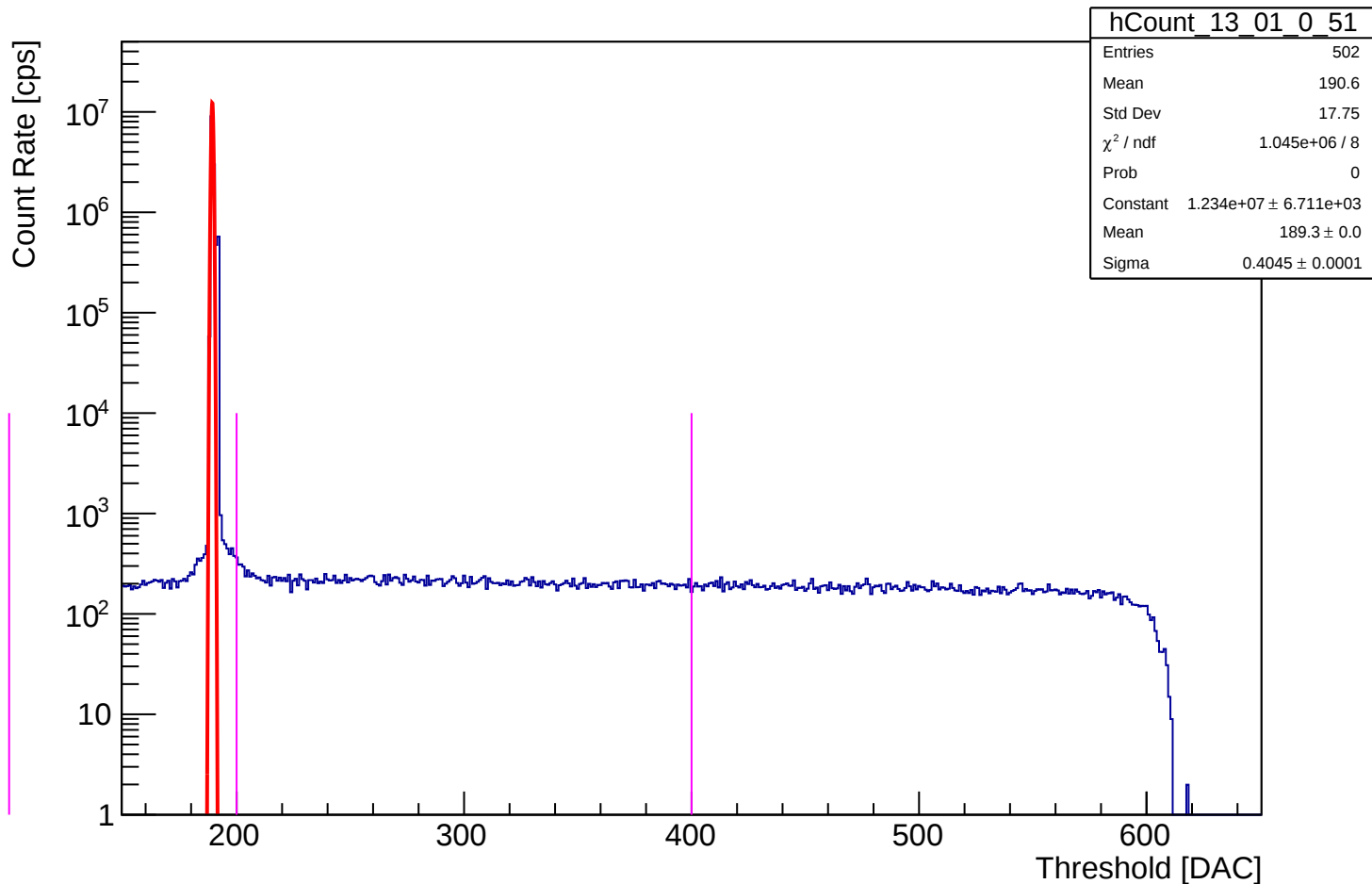
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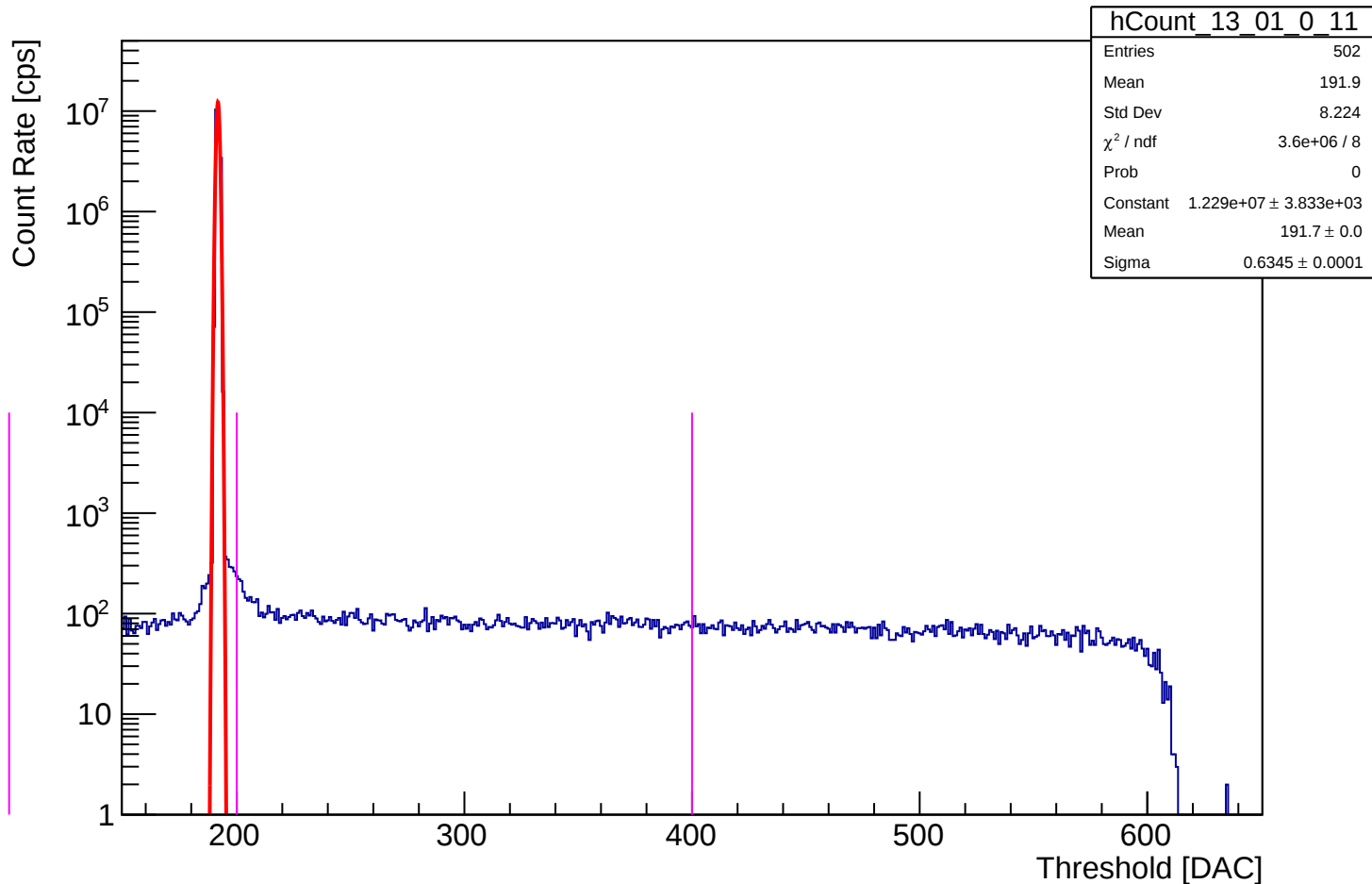
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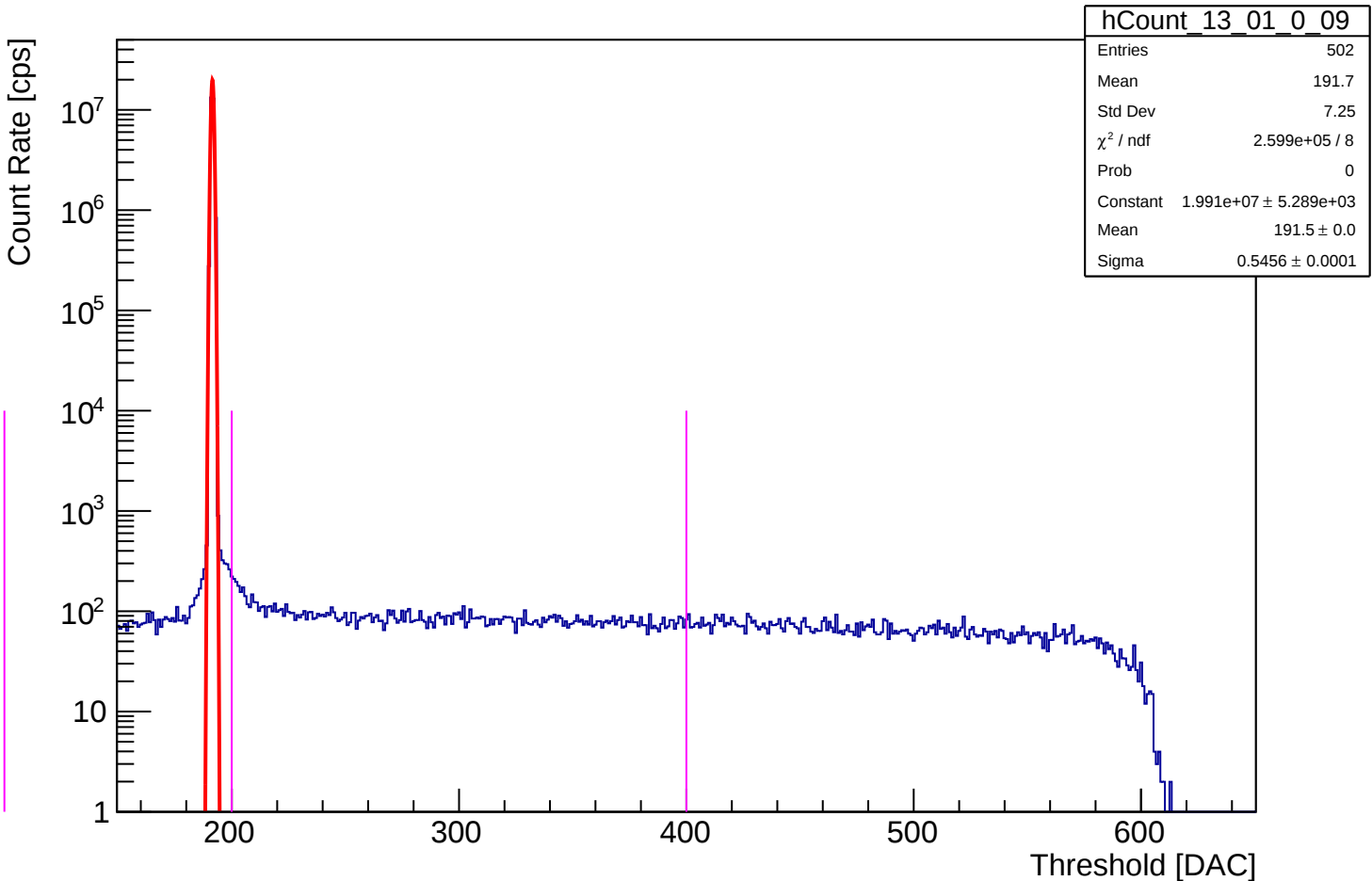


Row 1 Tile 1 Pmt 4 Pixel 40 Slot 13 Fiber 1 Asic 0 Channel 51

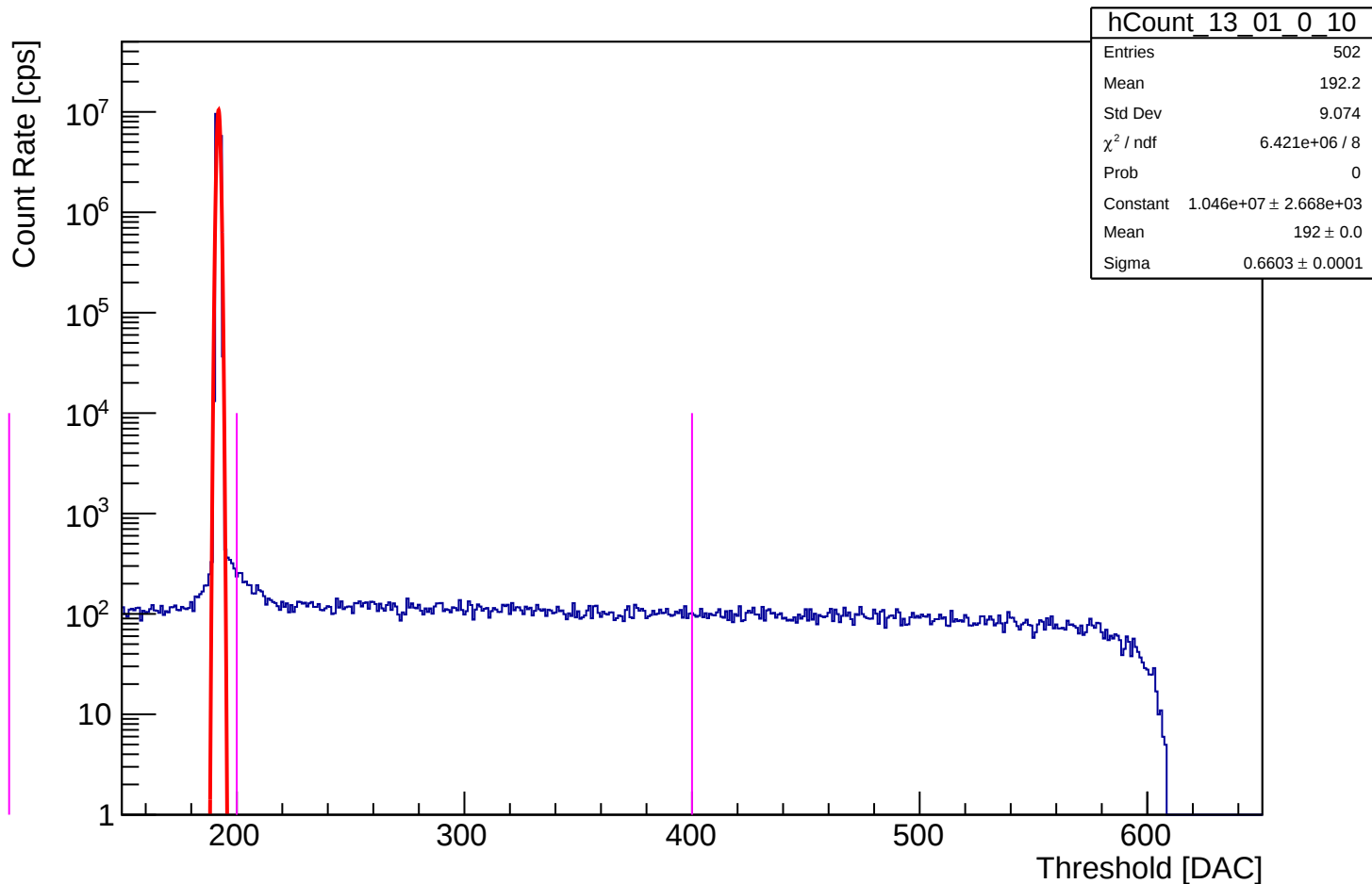


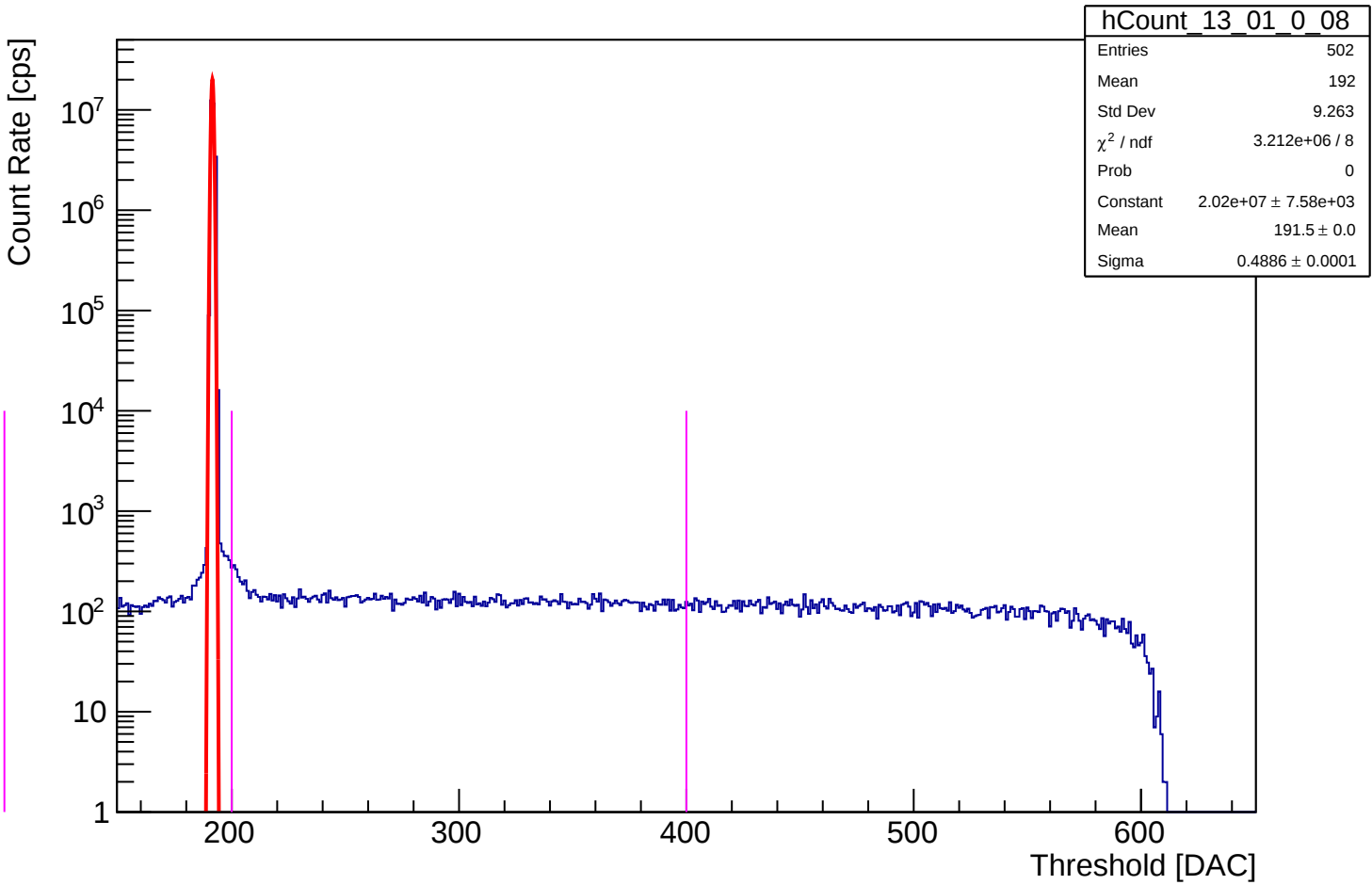
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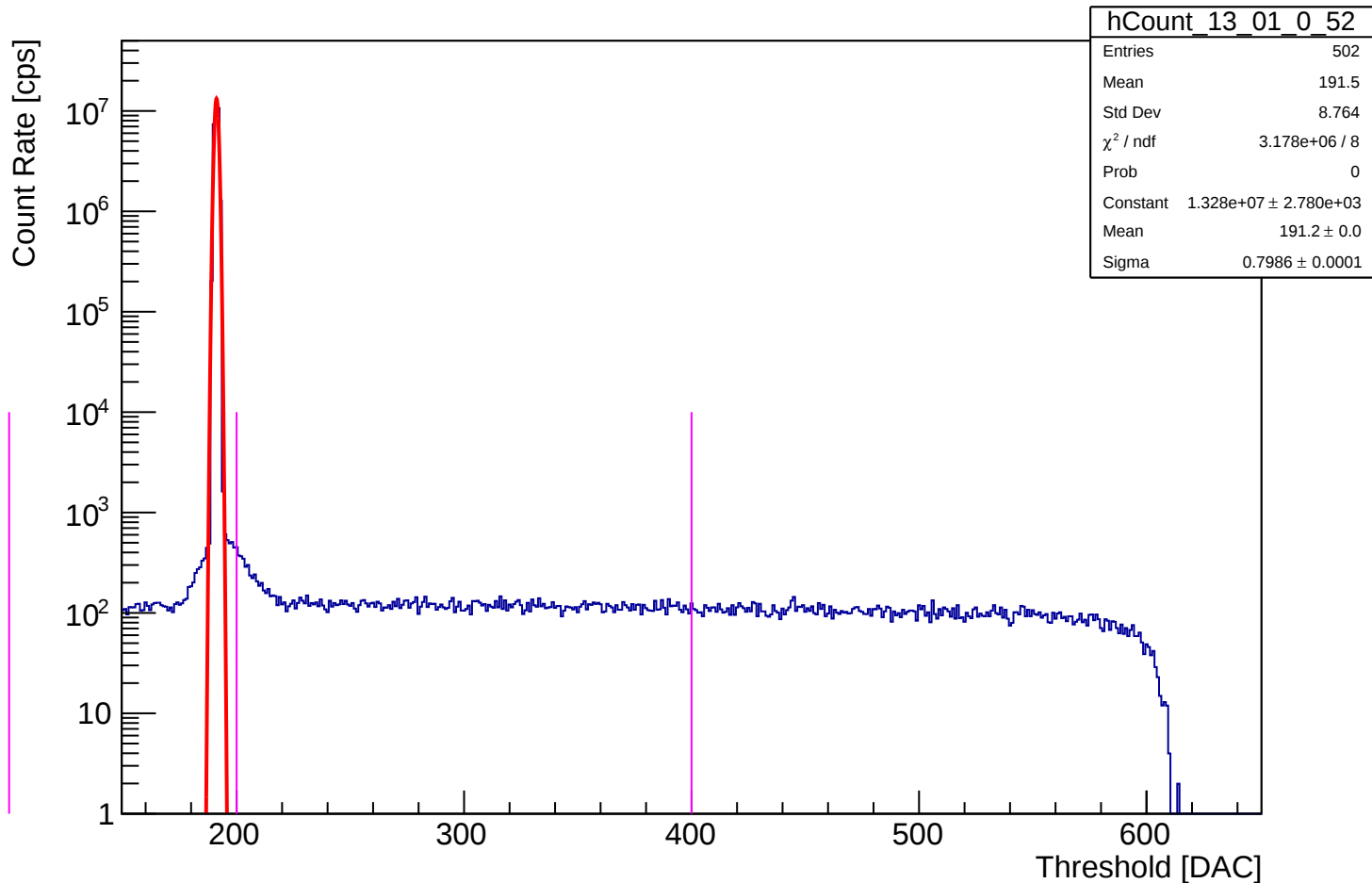


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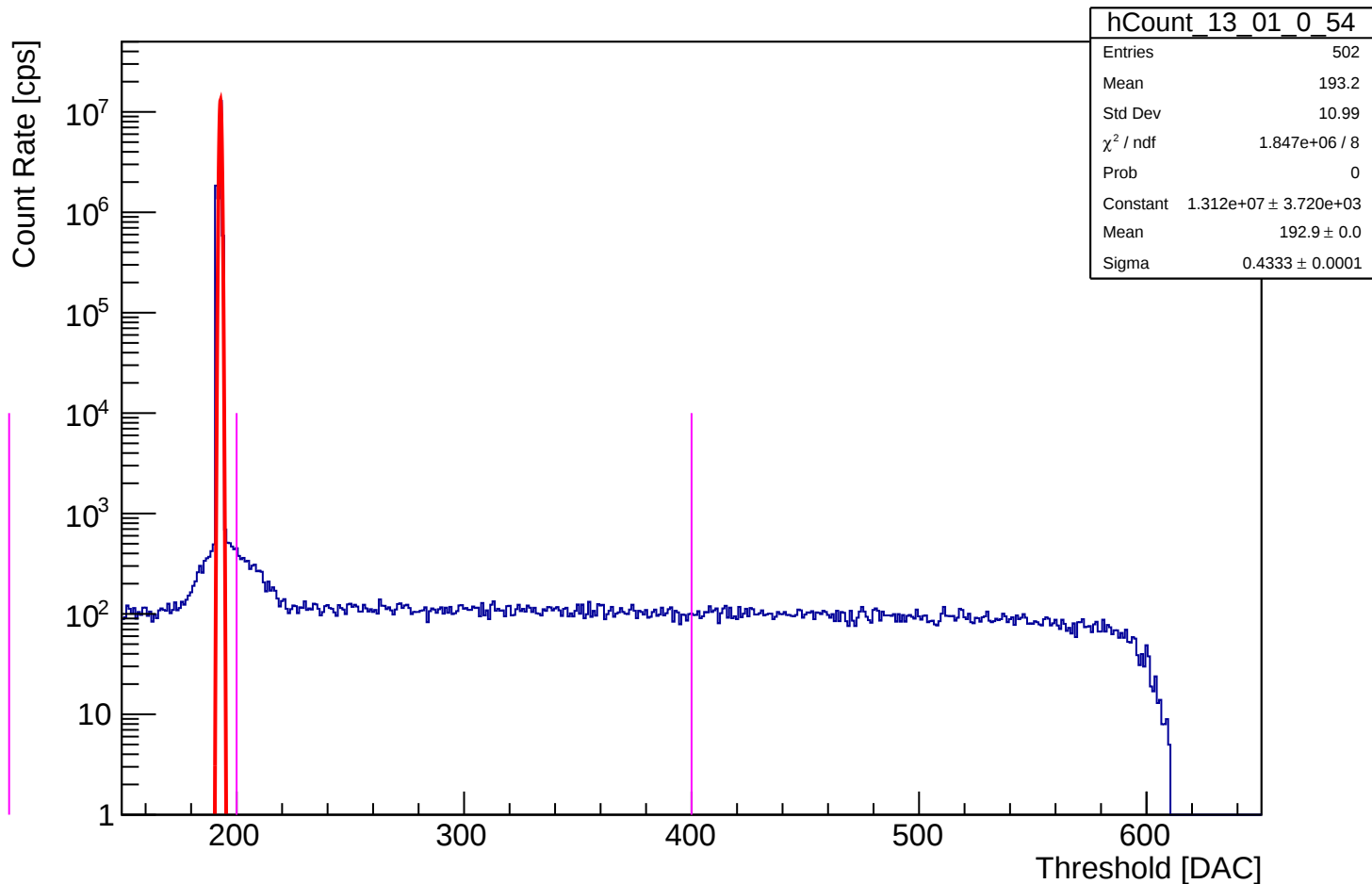




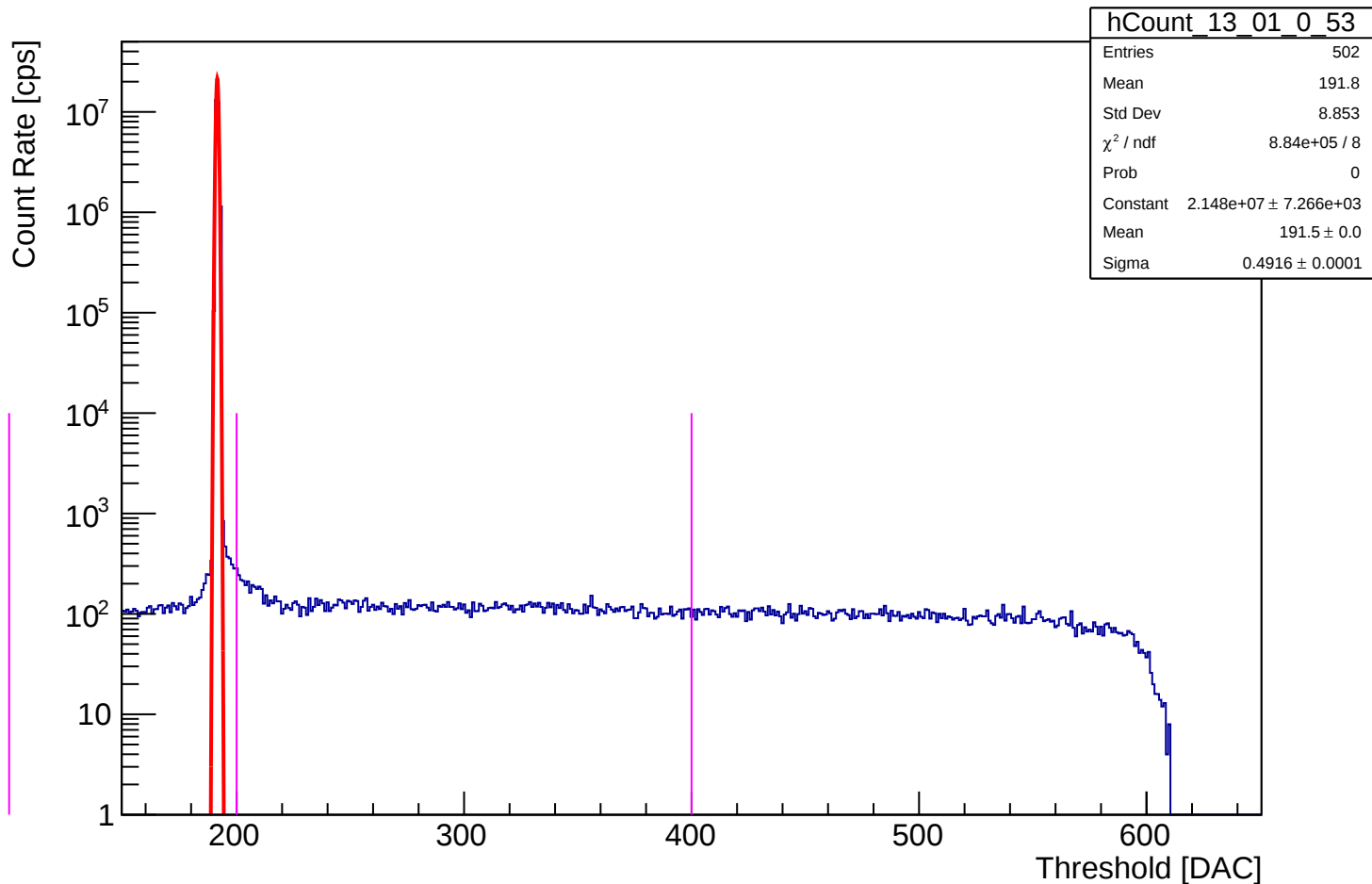
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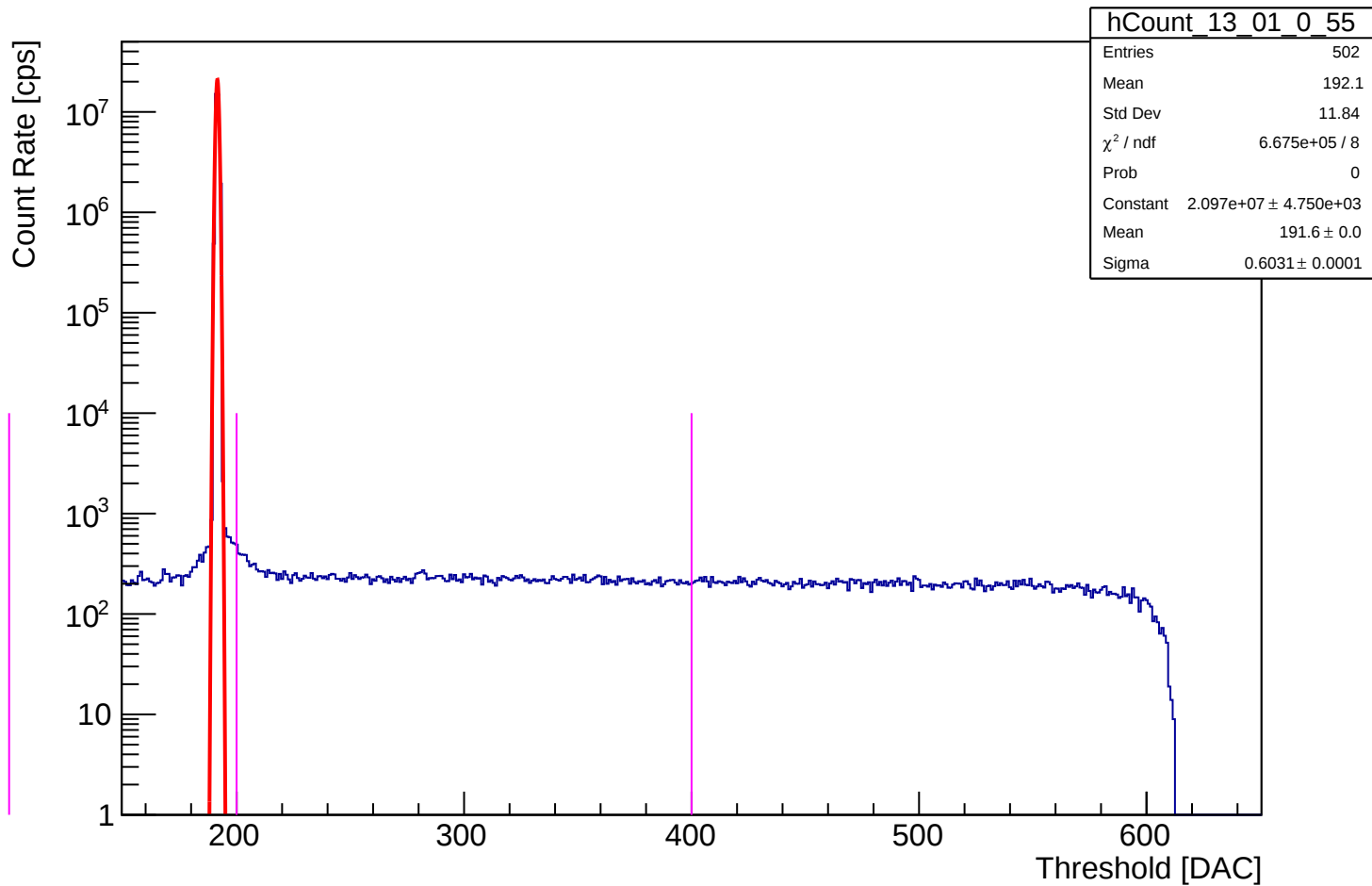
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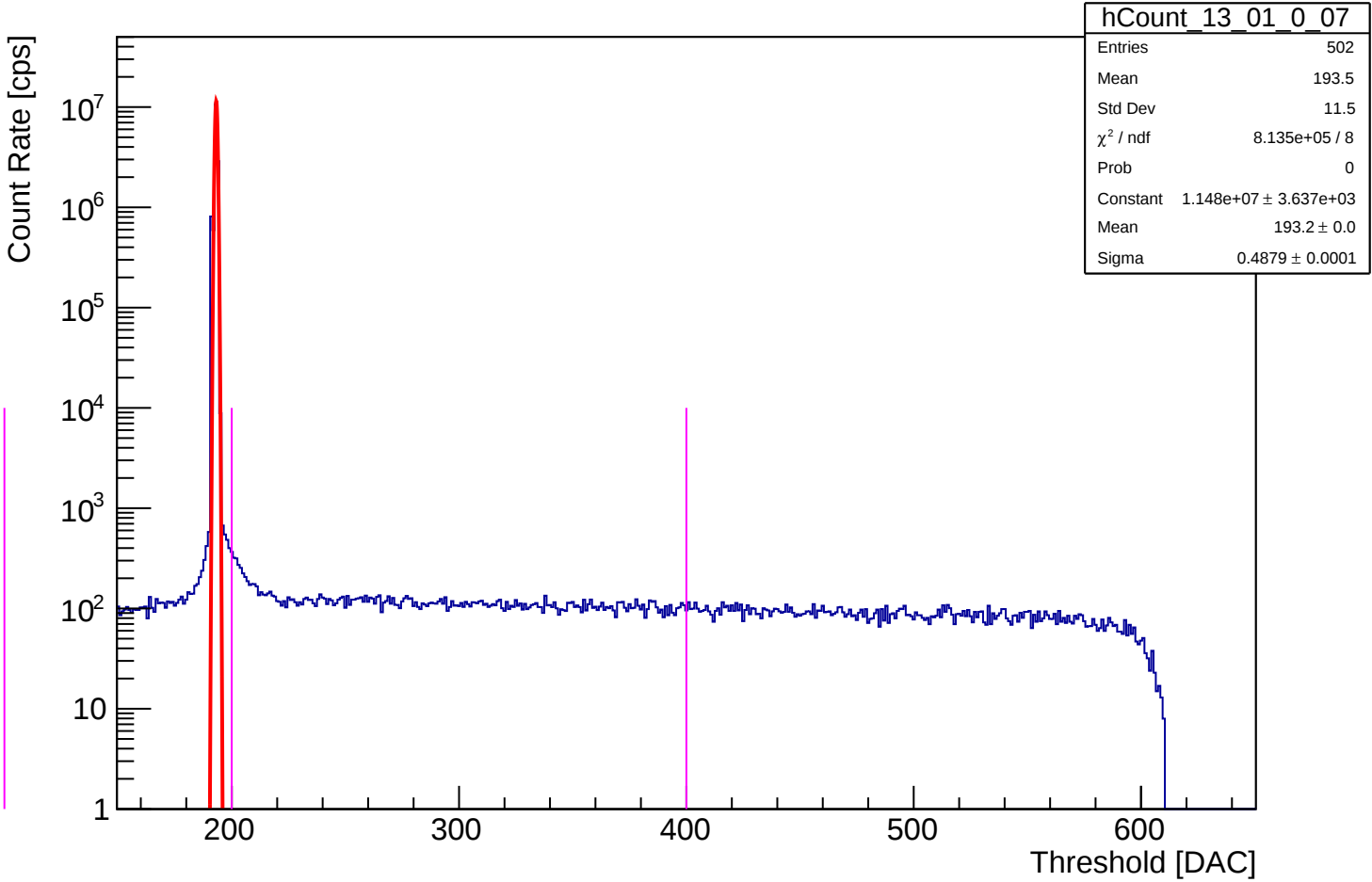


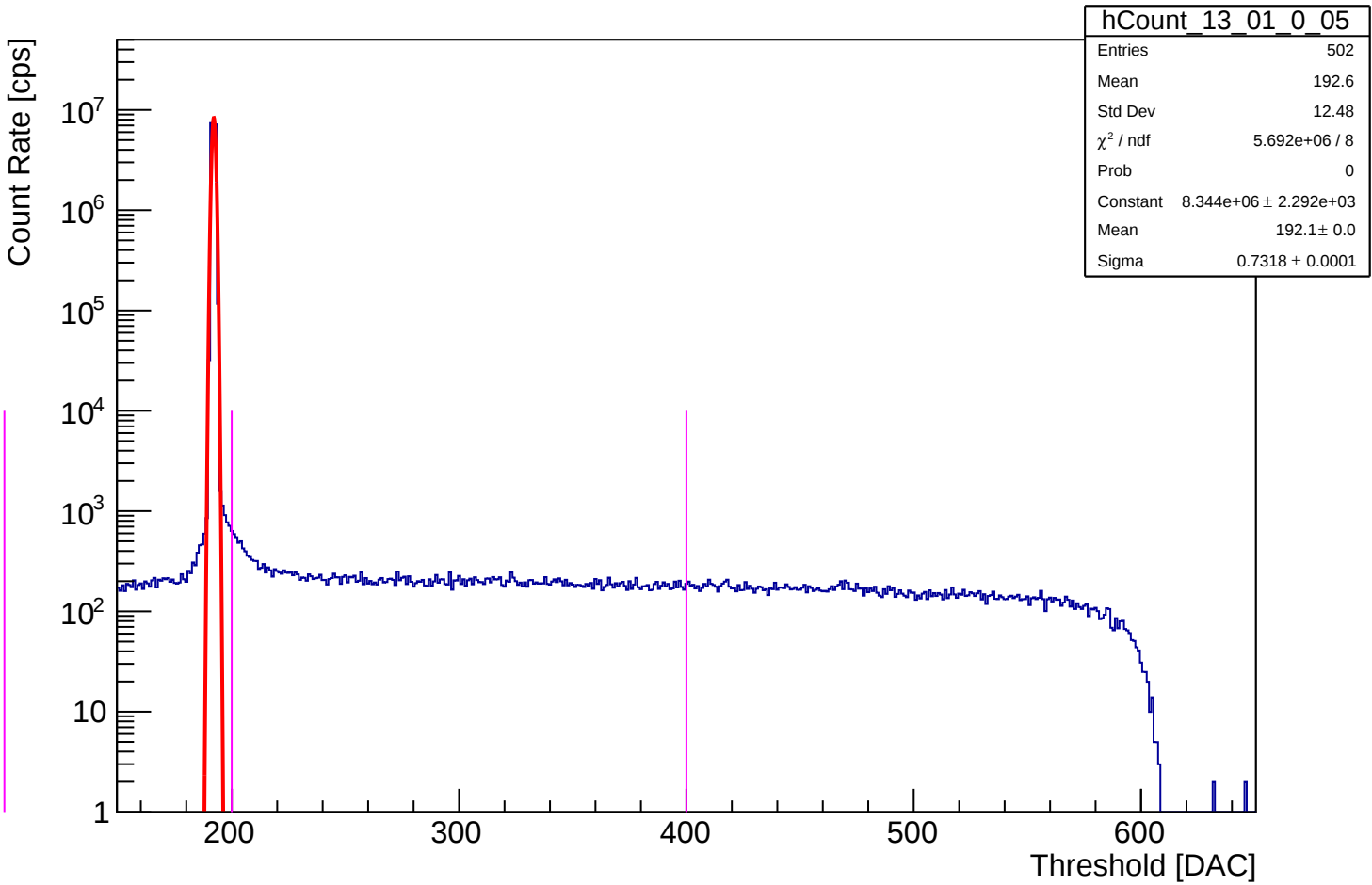
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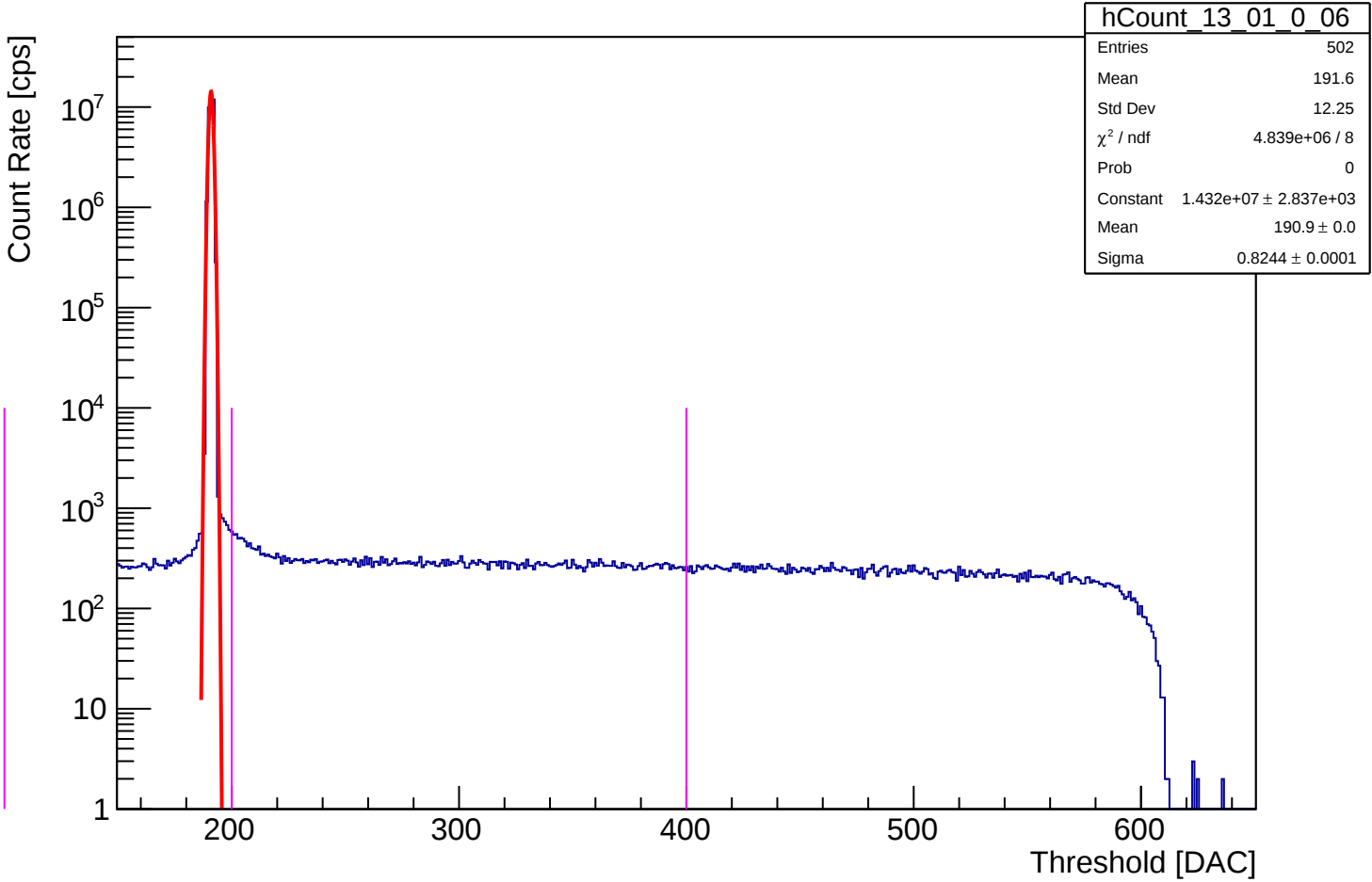


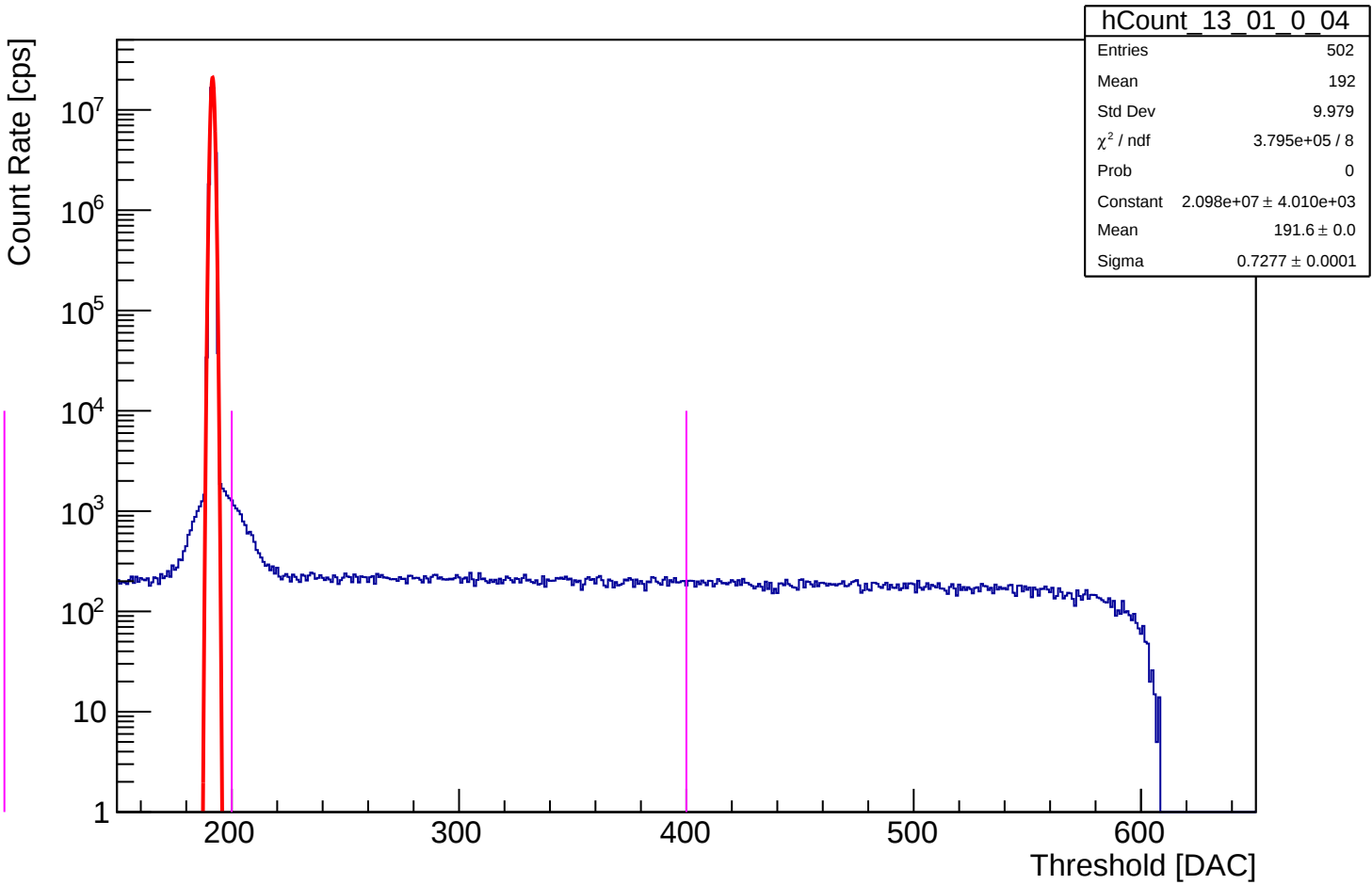
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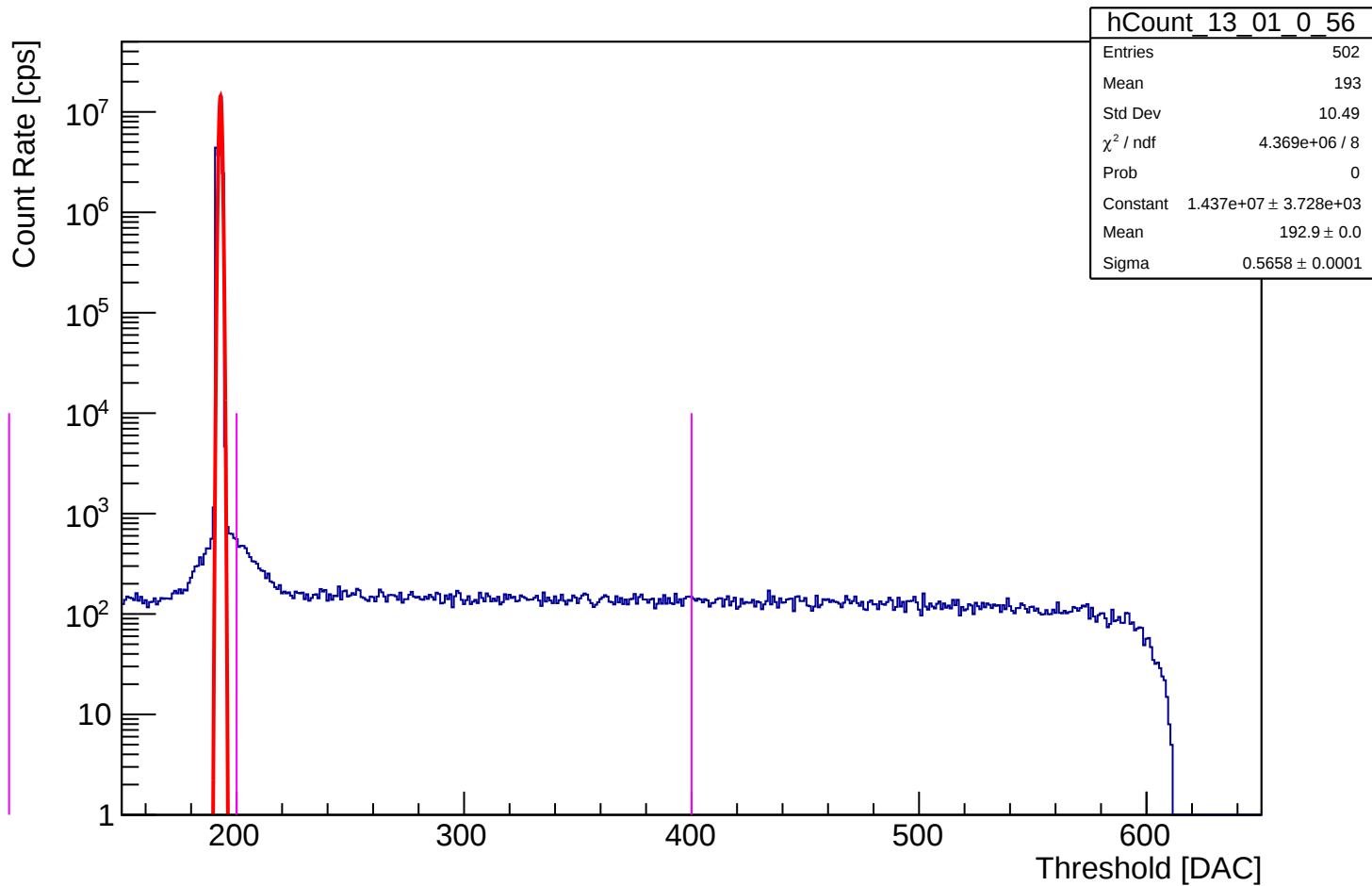




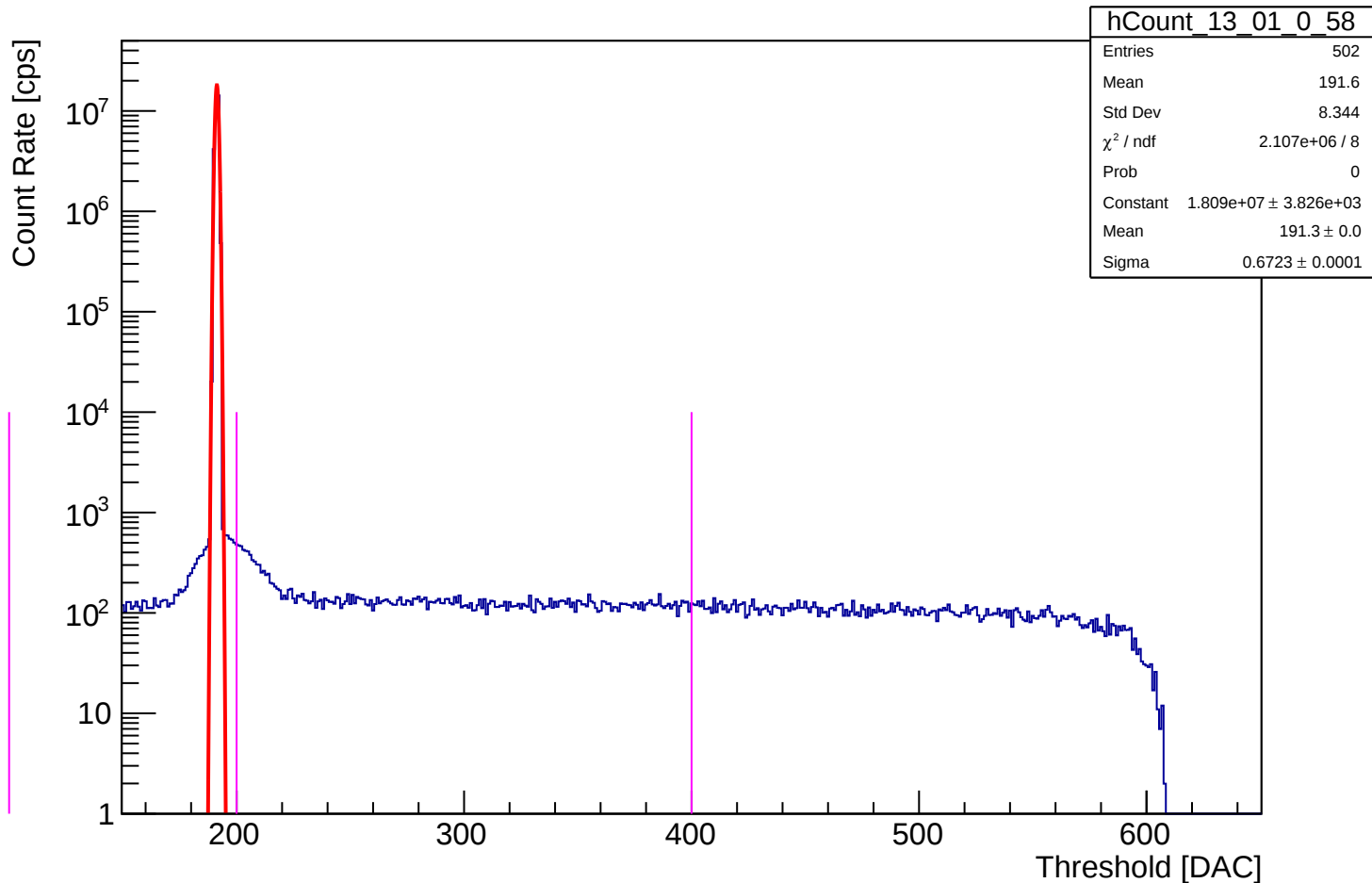




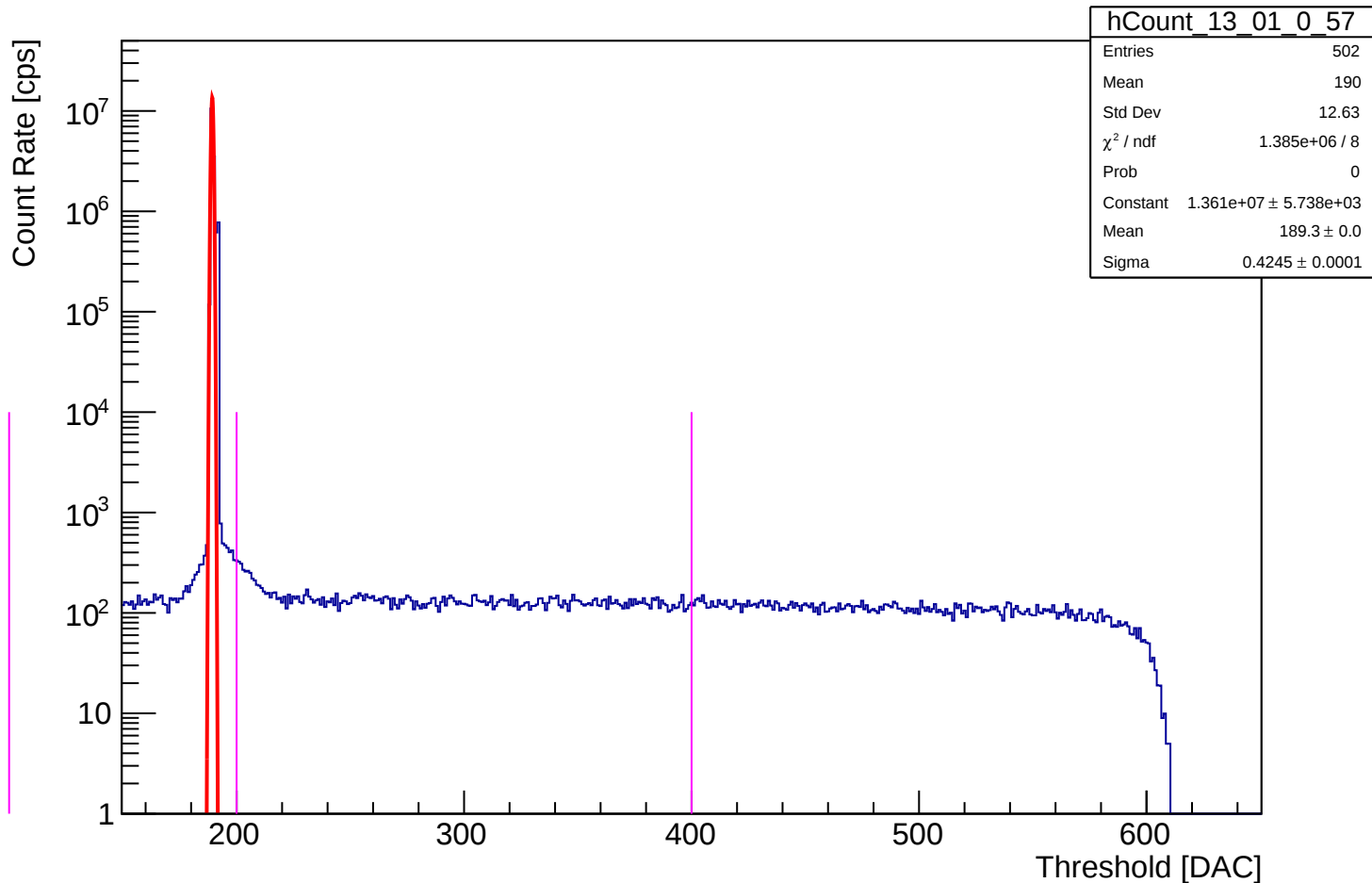
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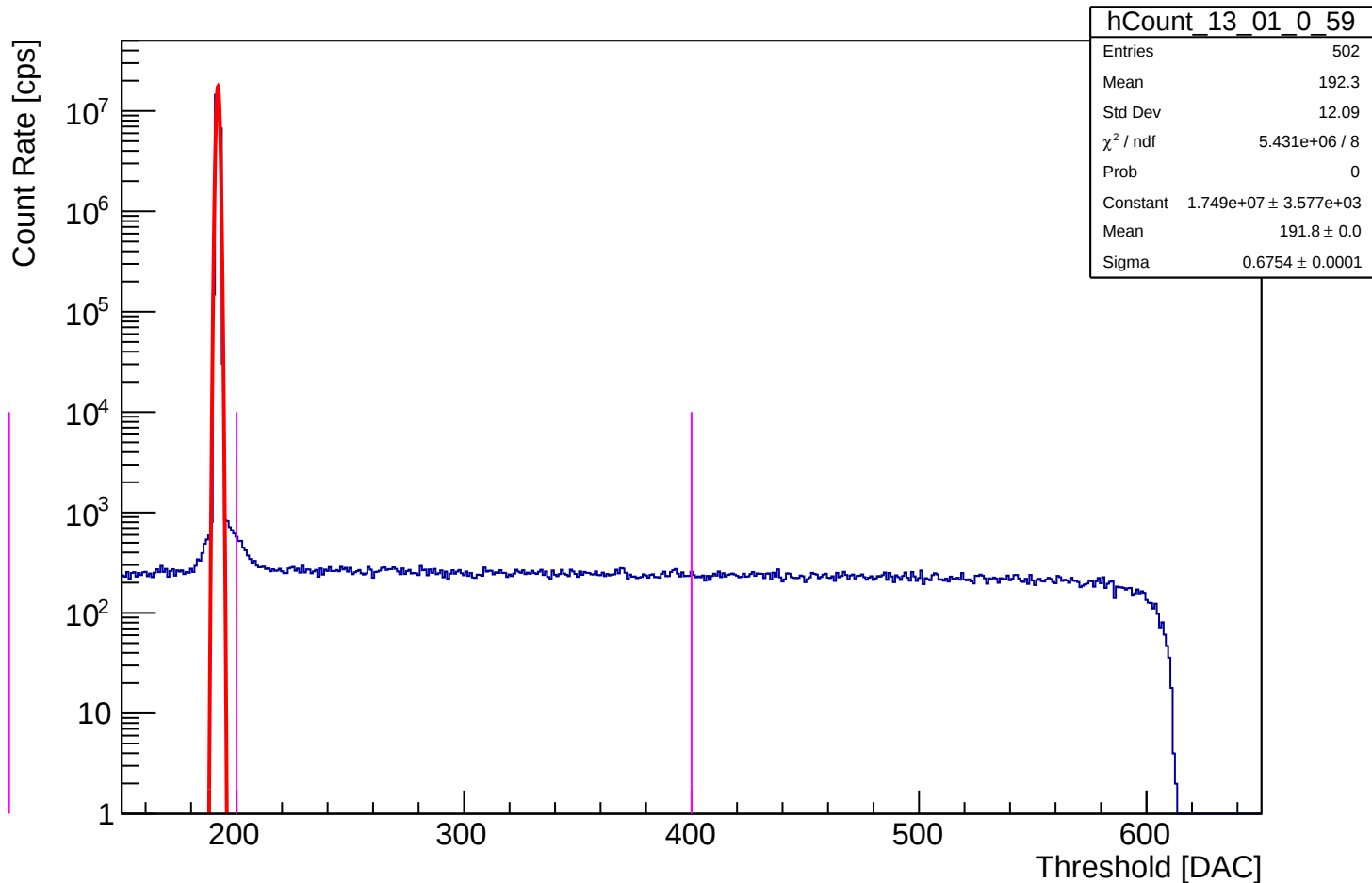
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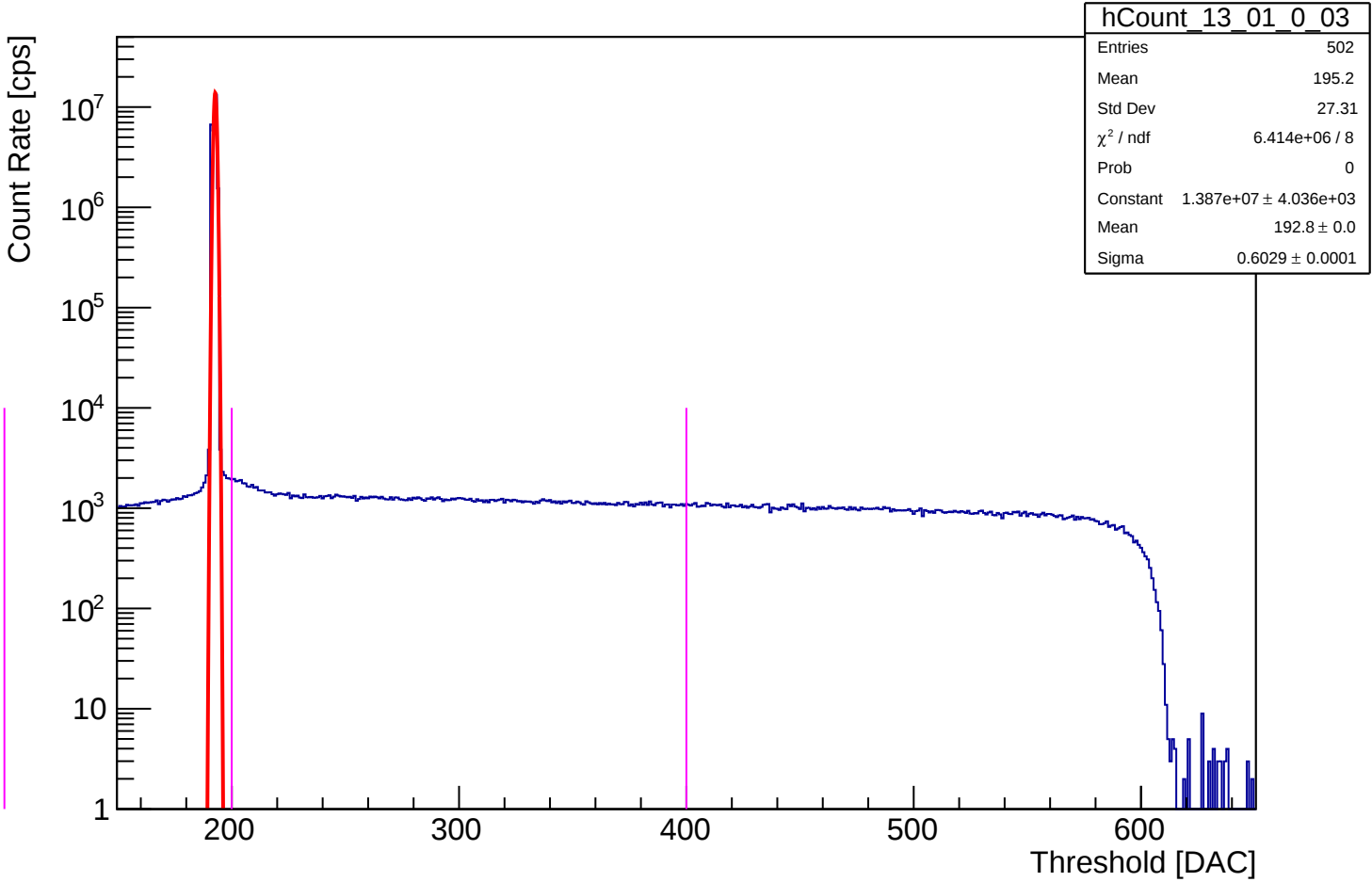


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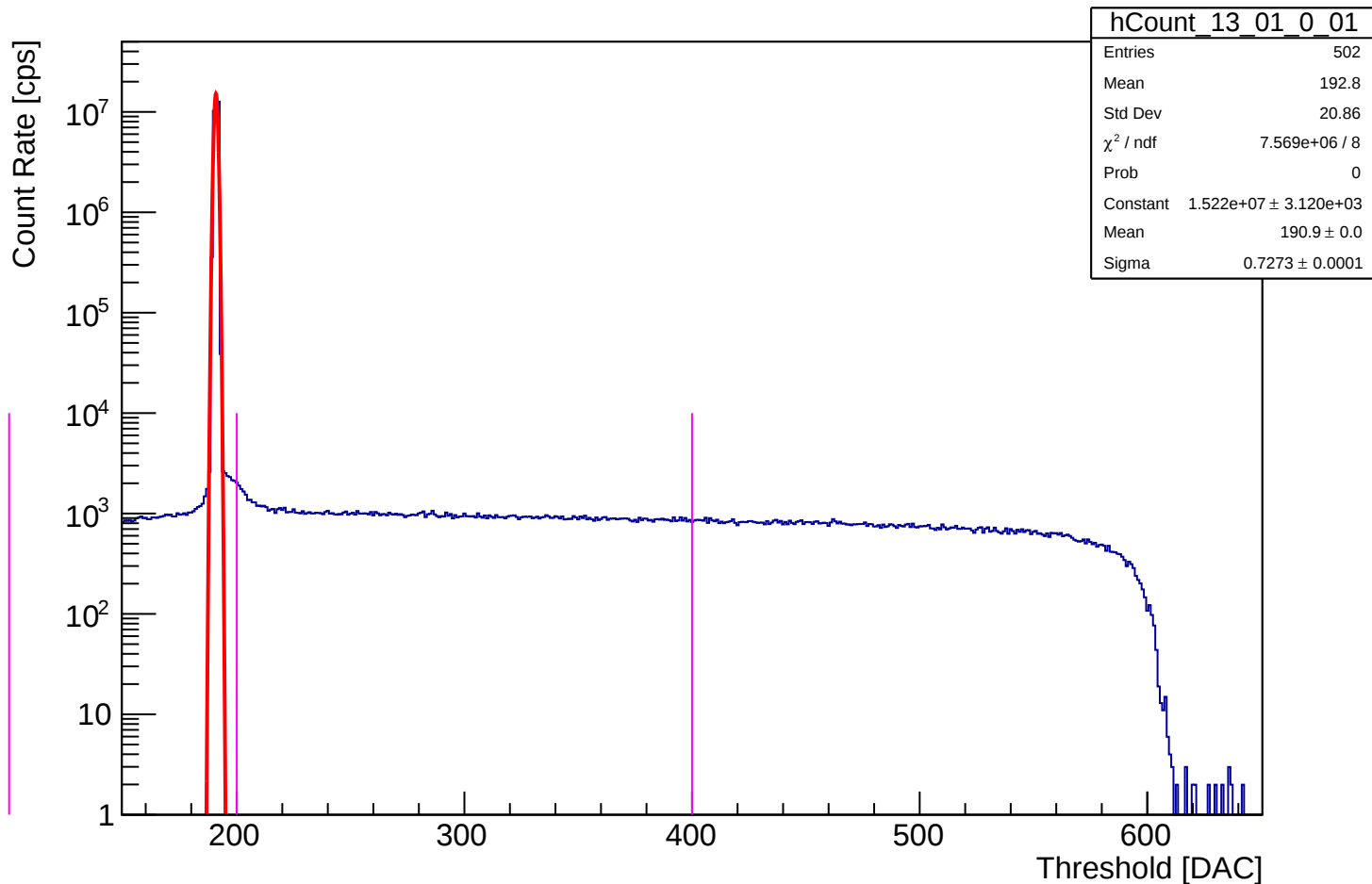


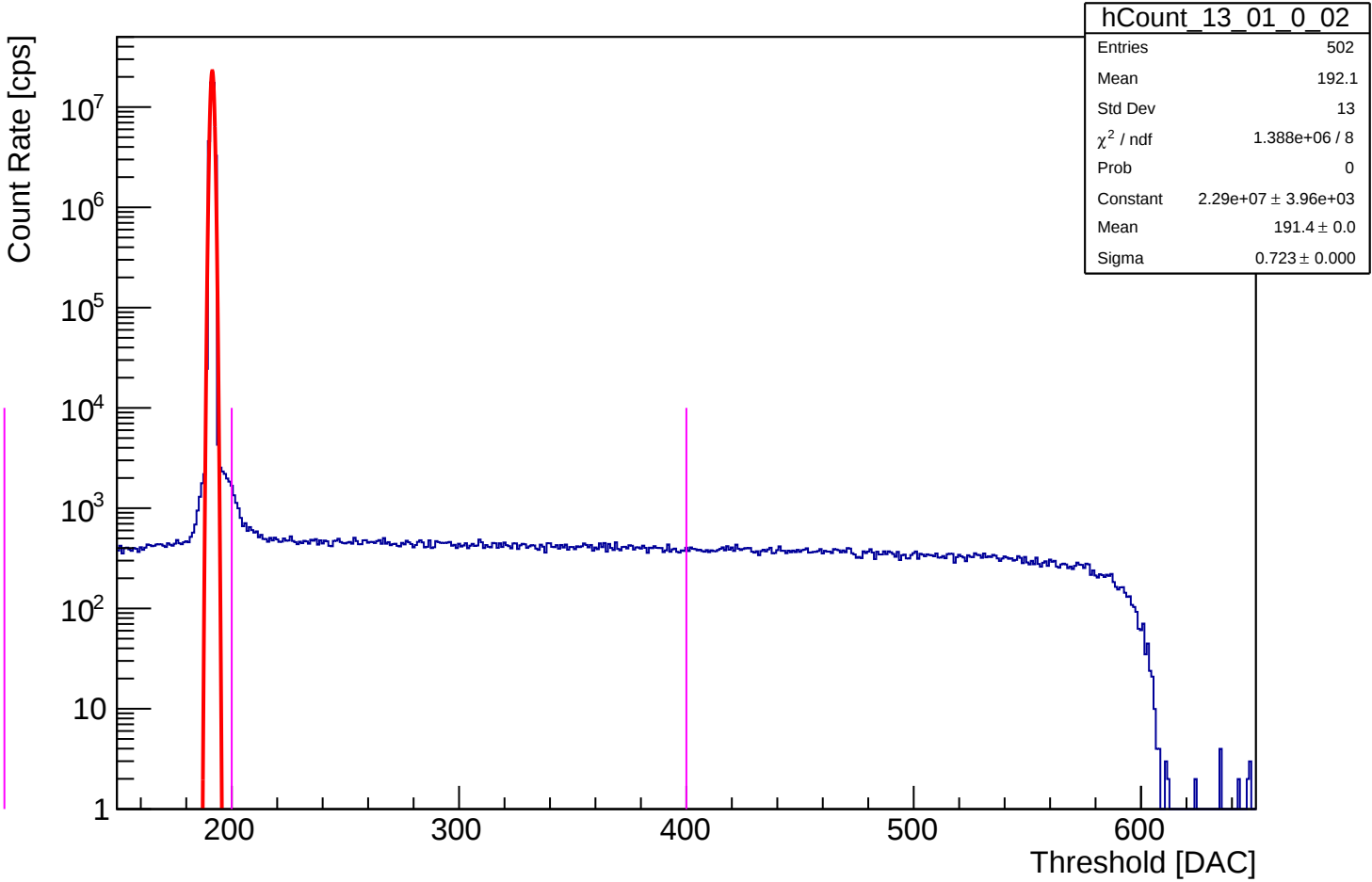
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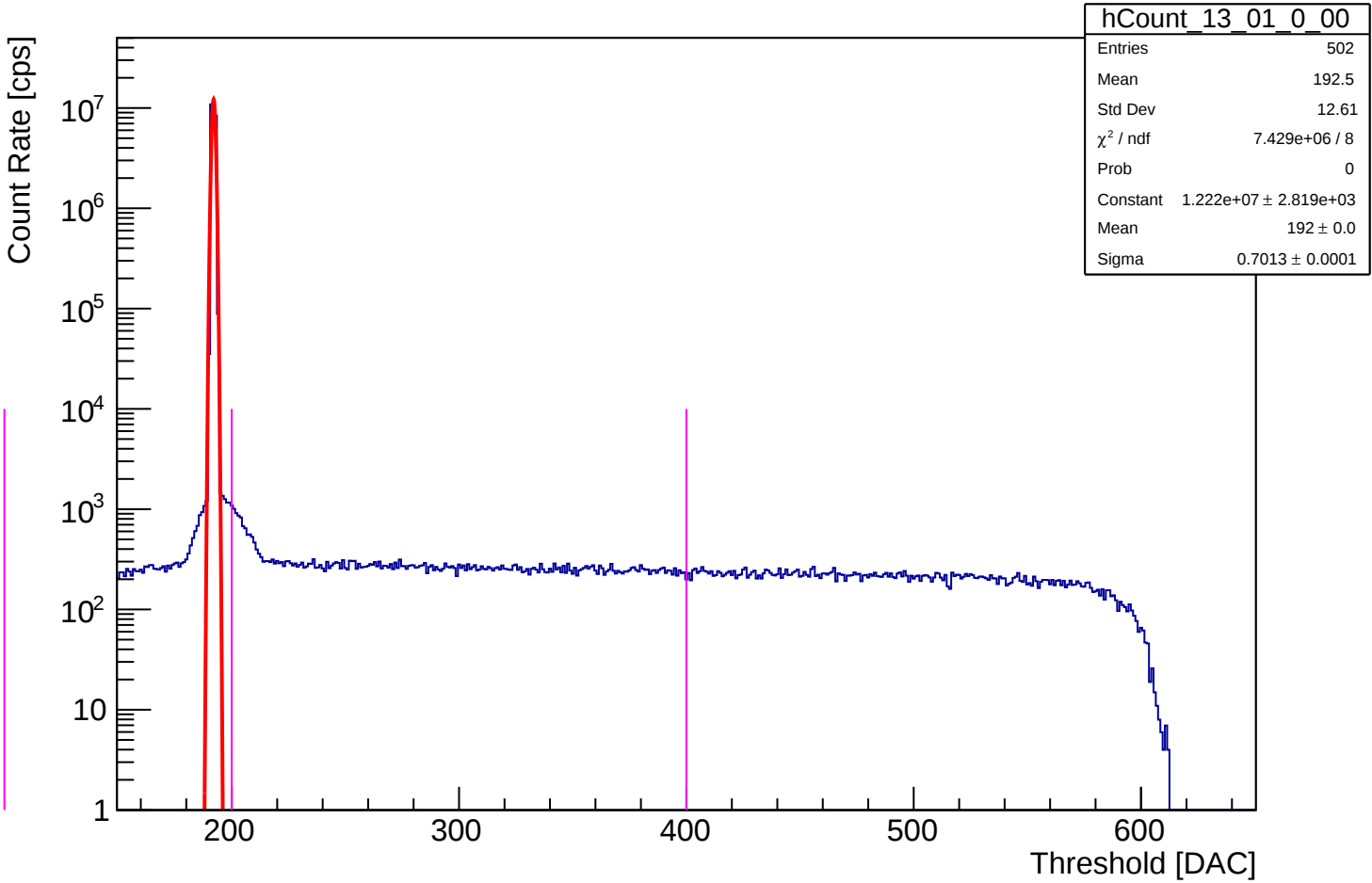




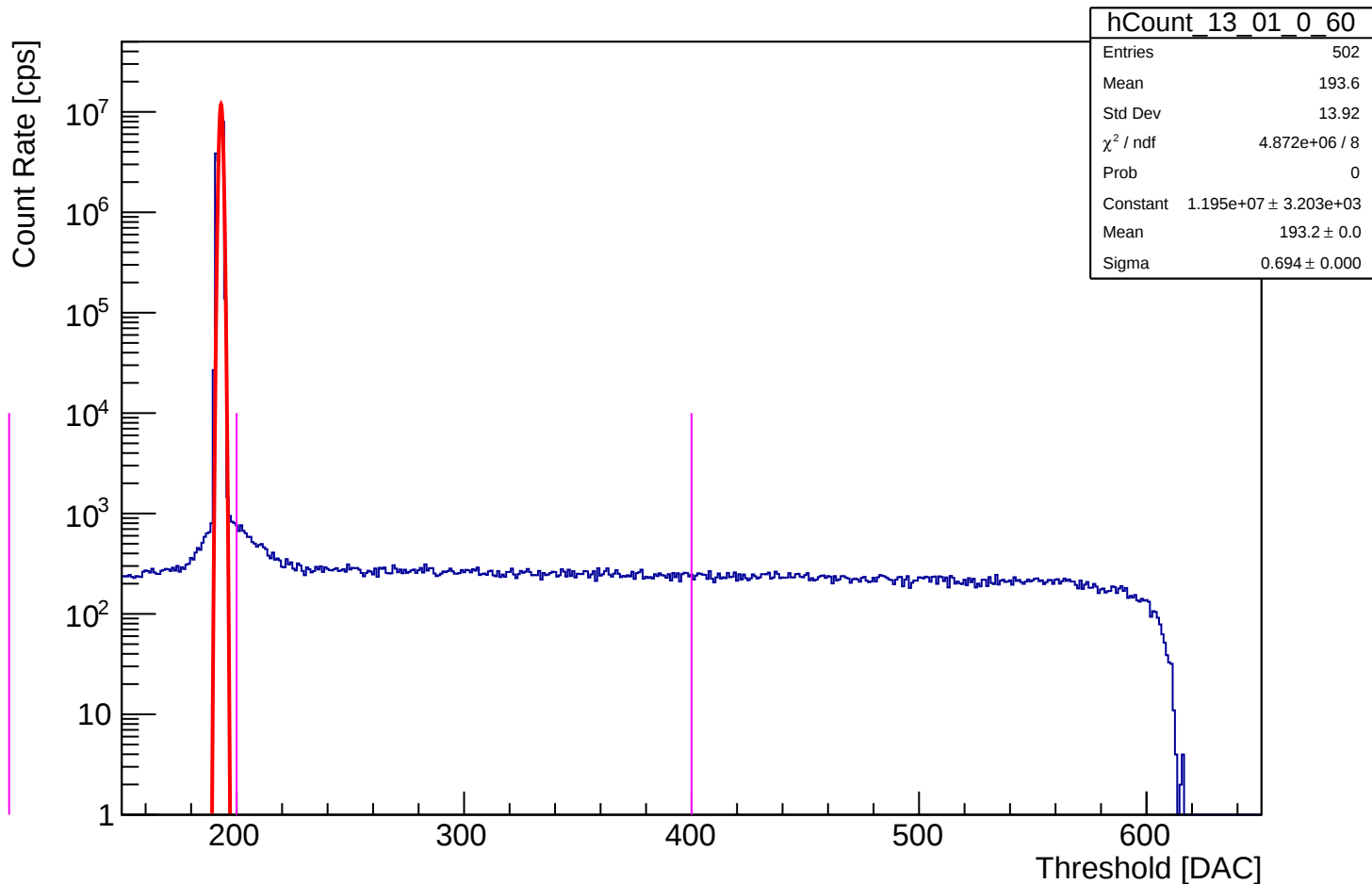
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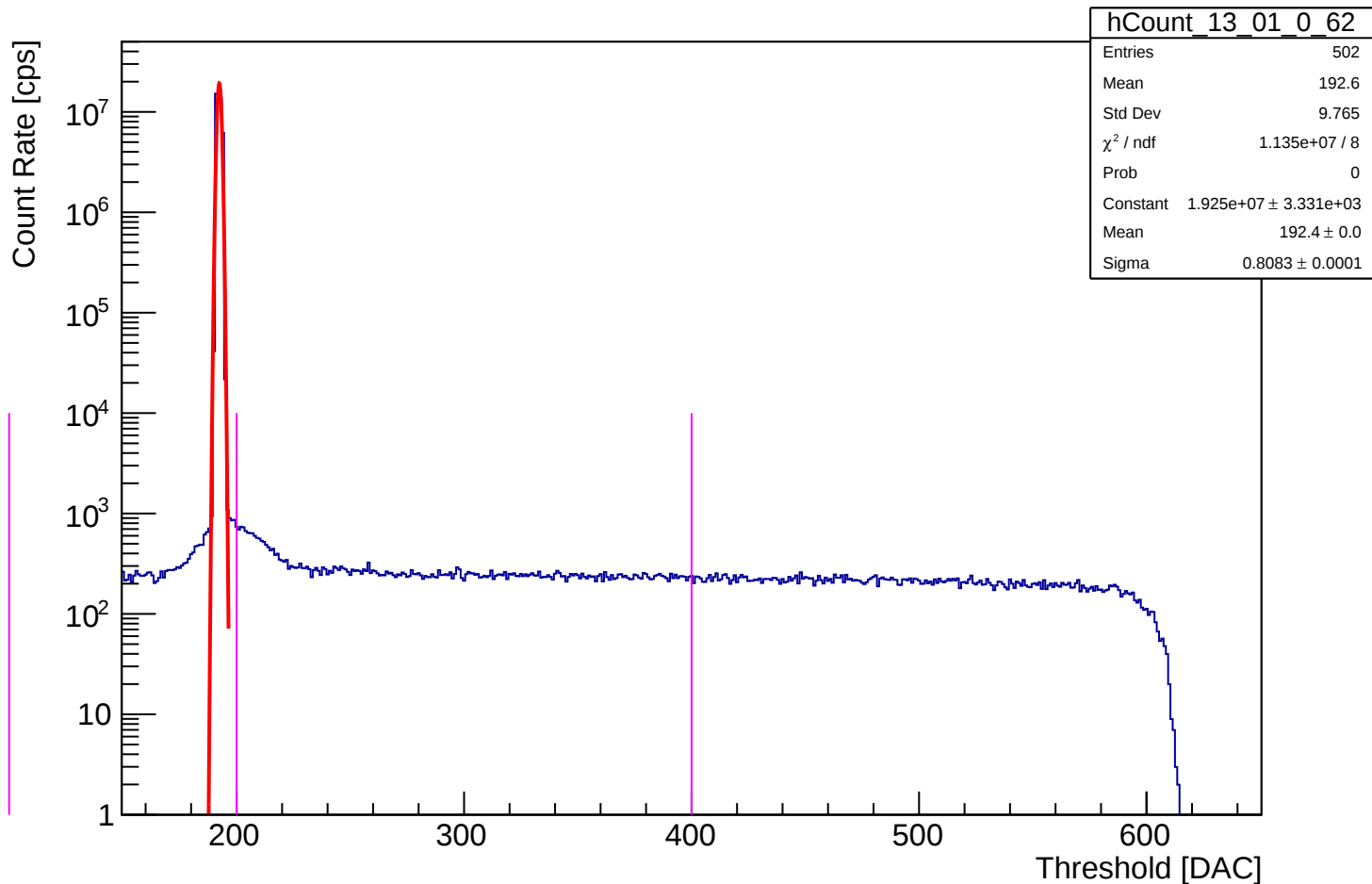




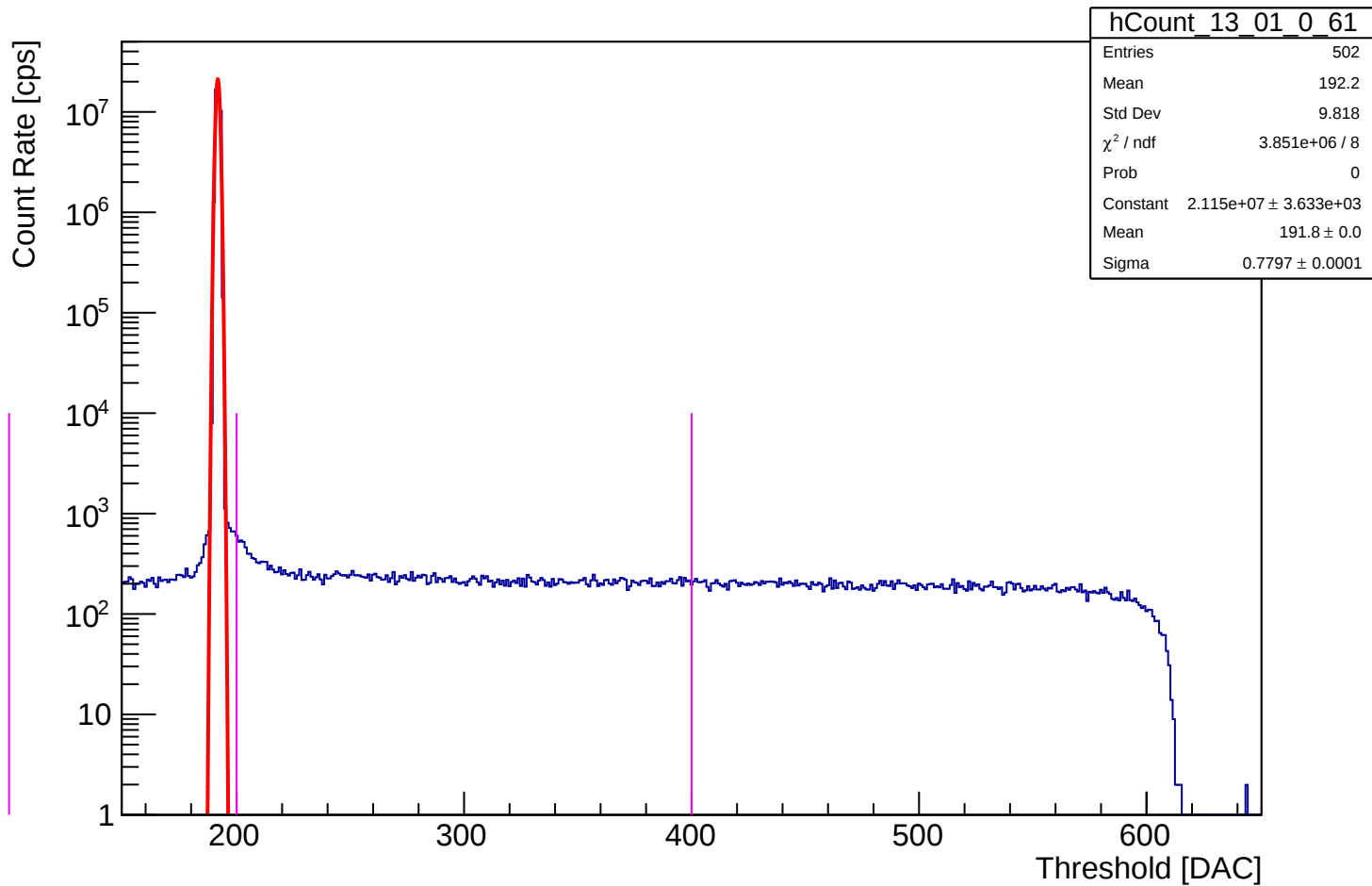
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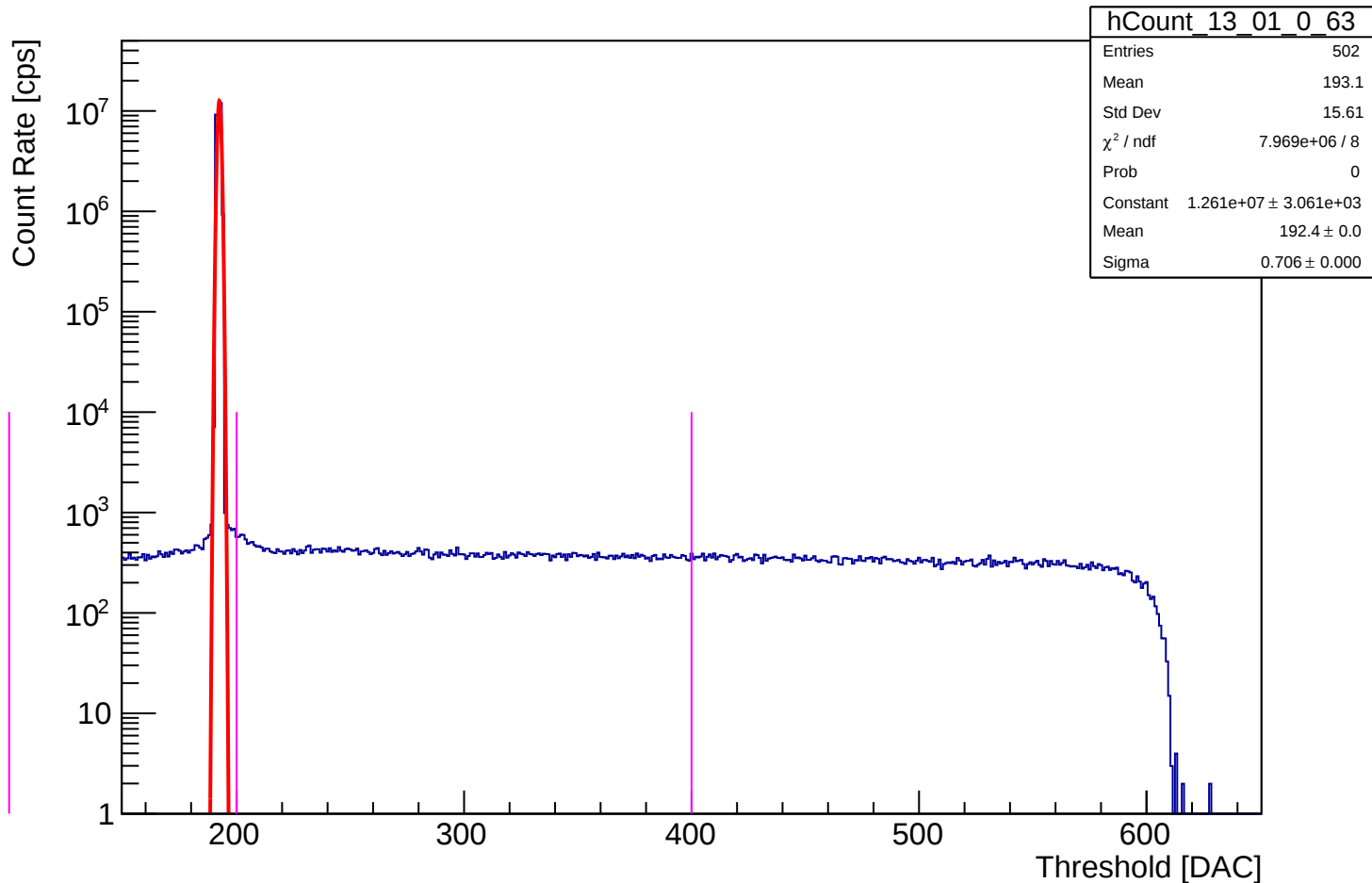
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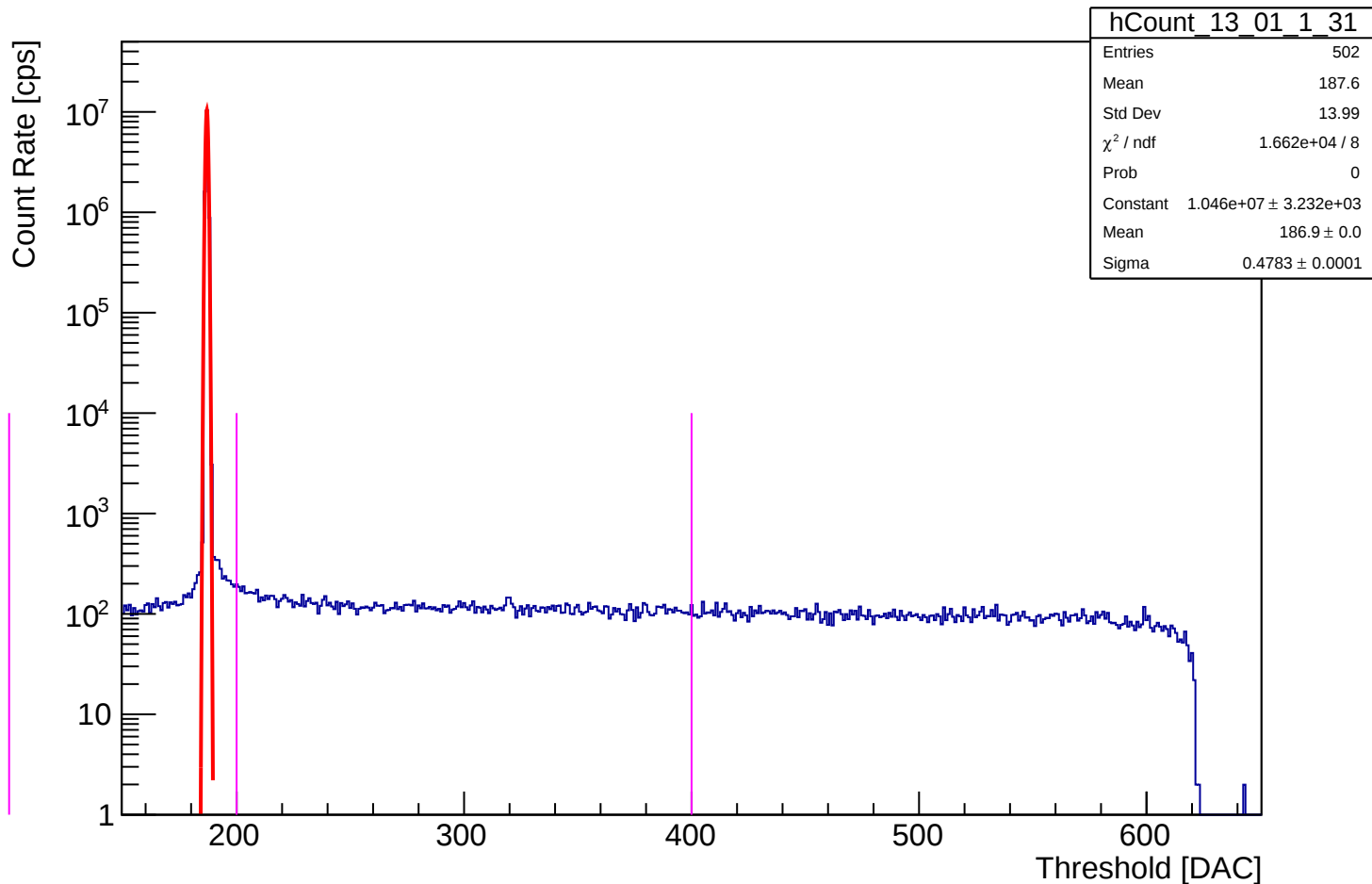
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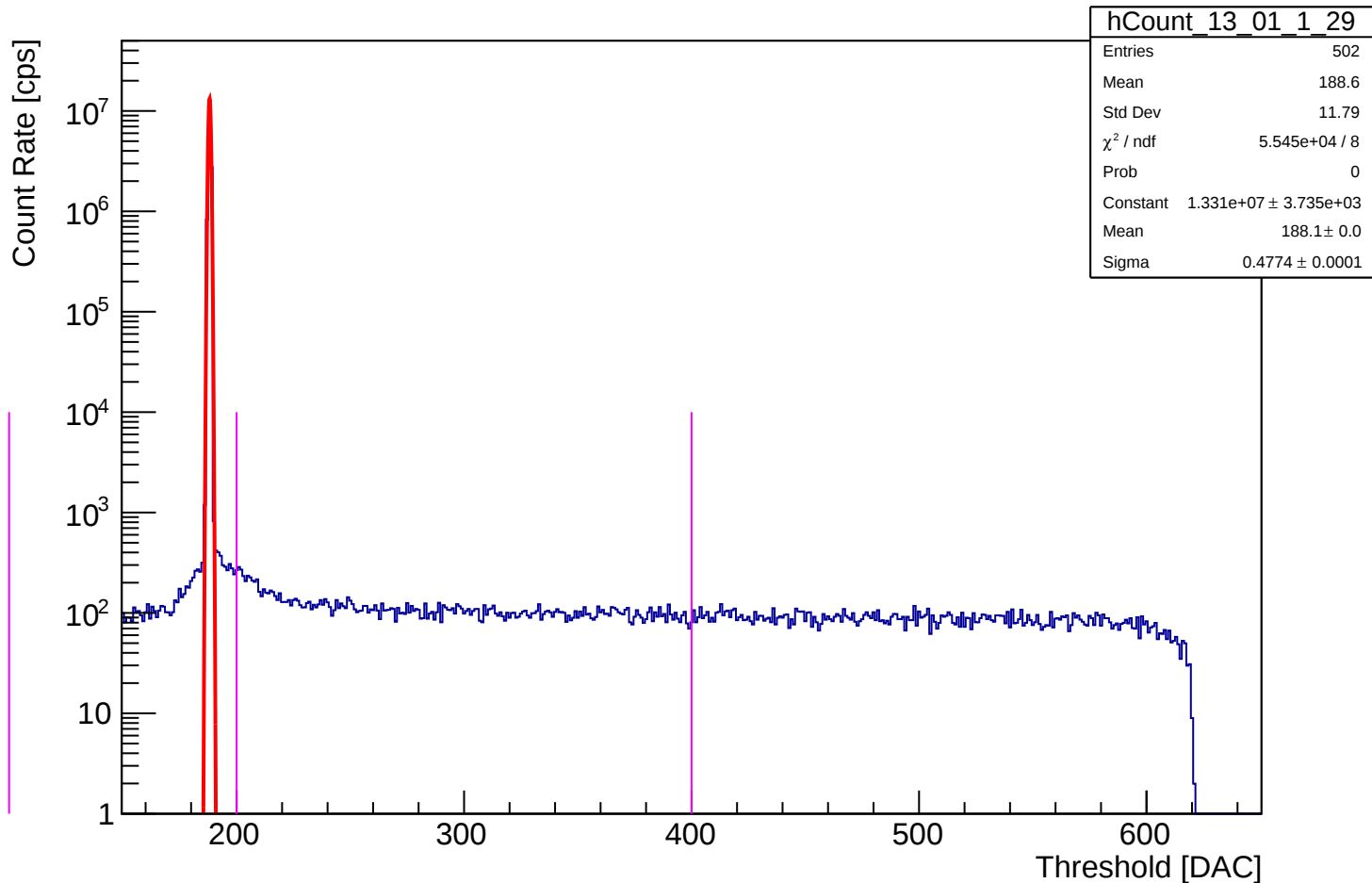
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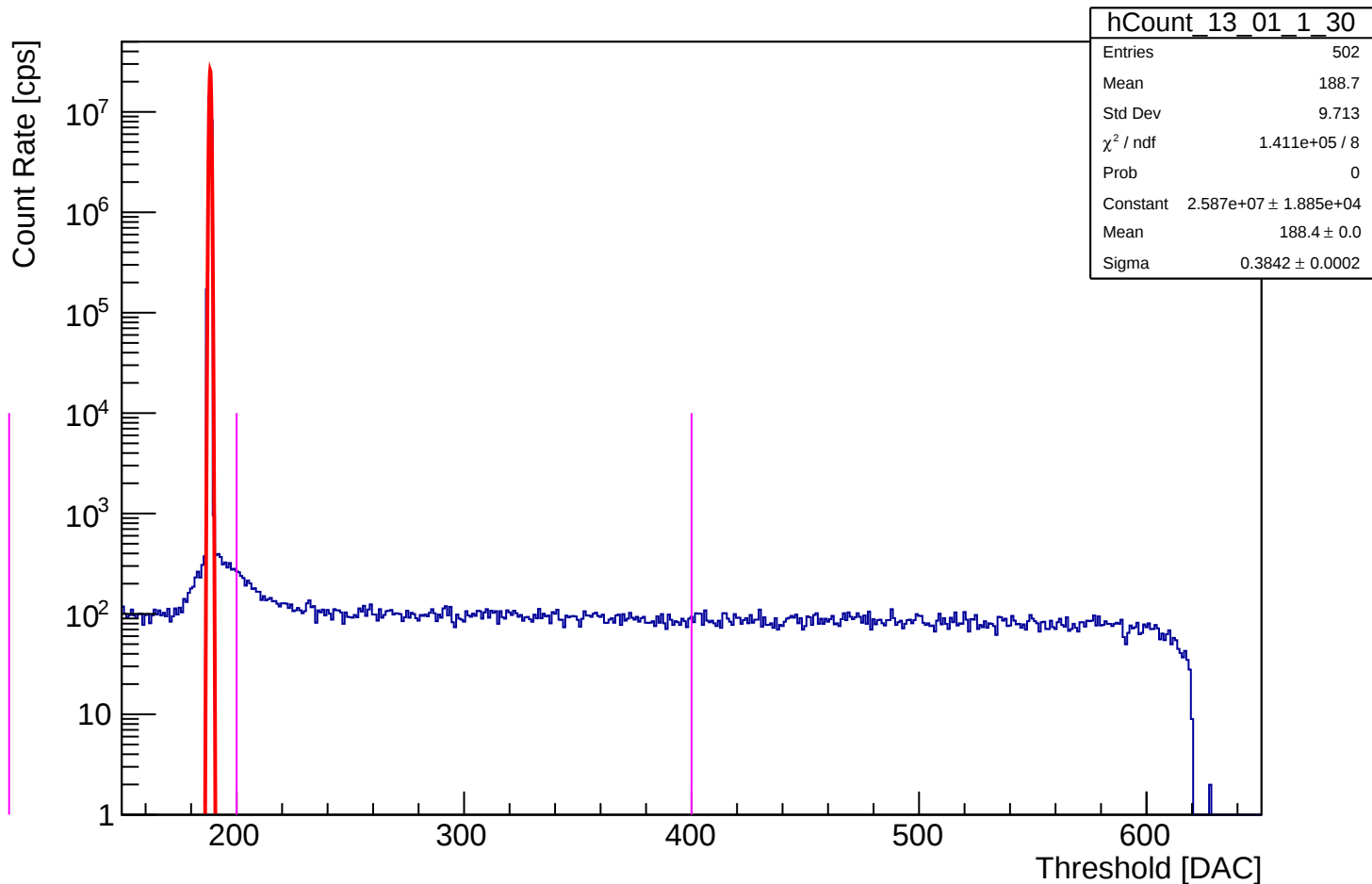
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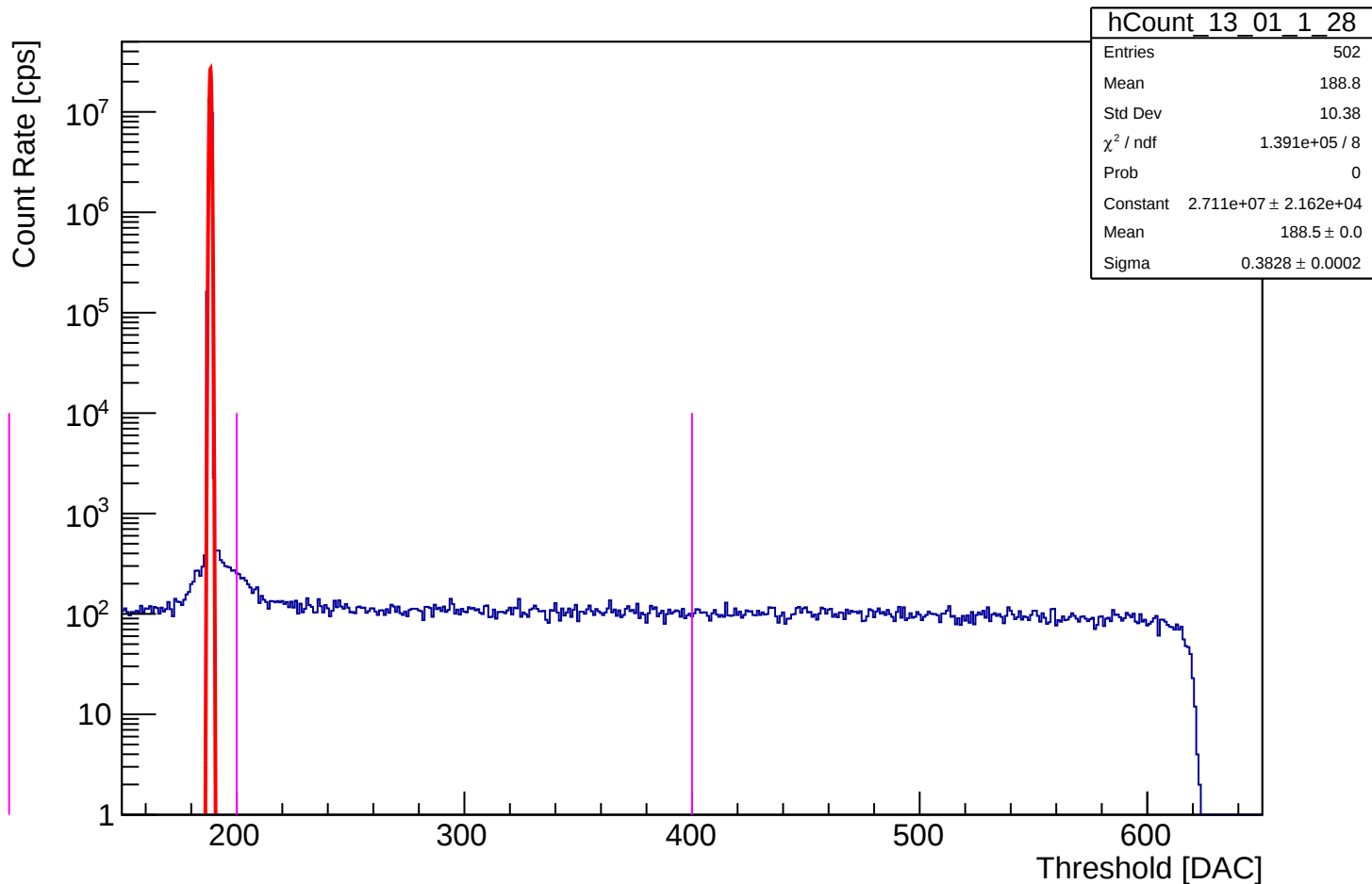
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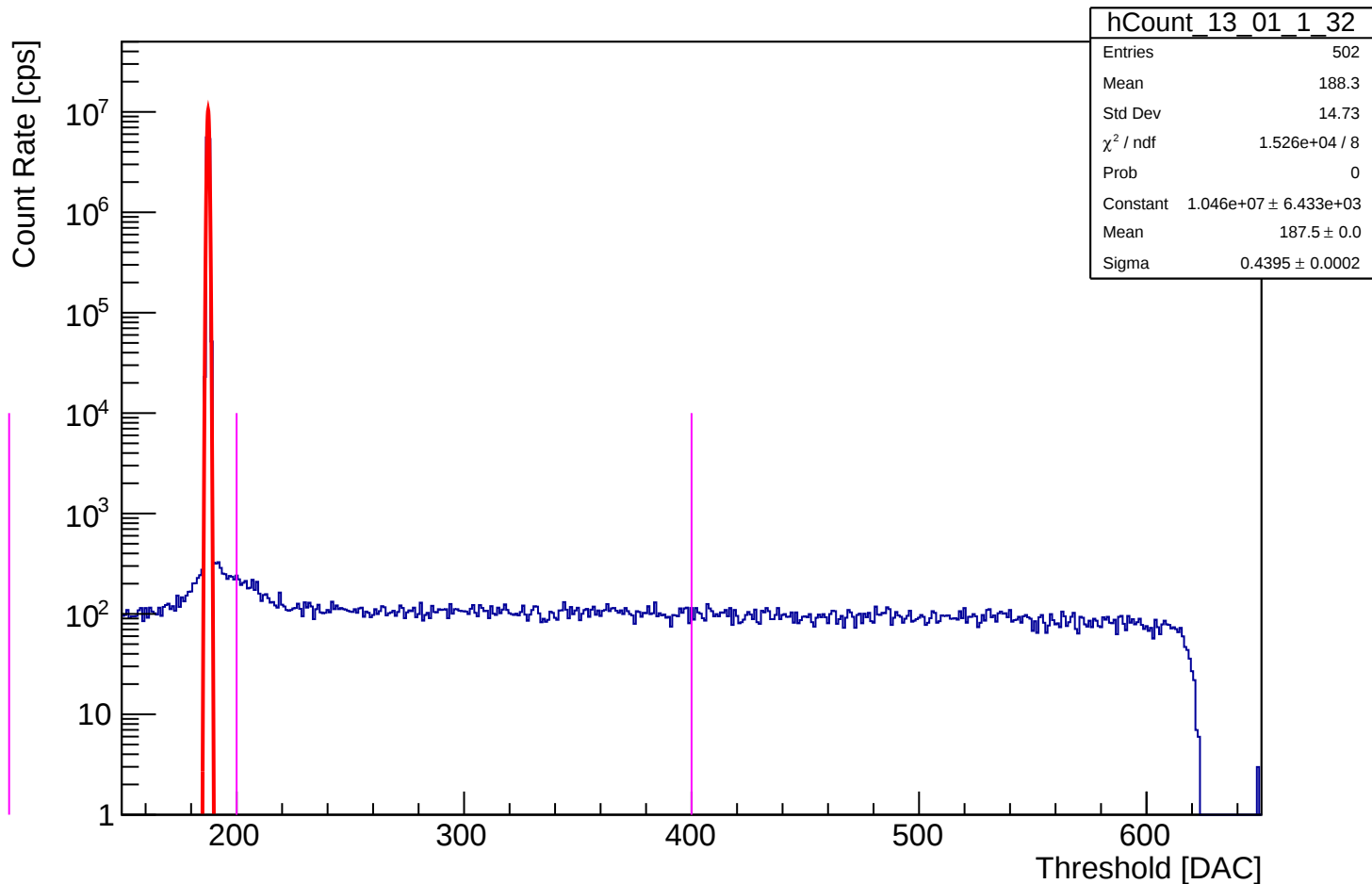
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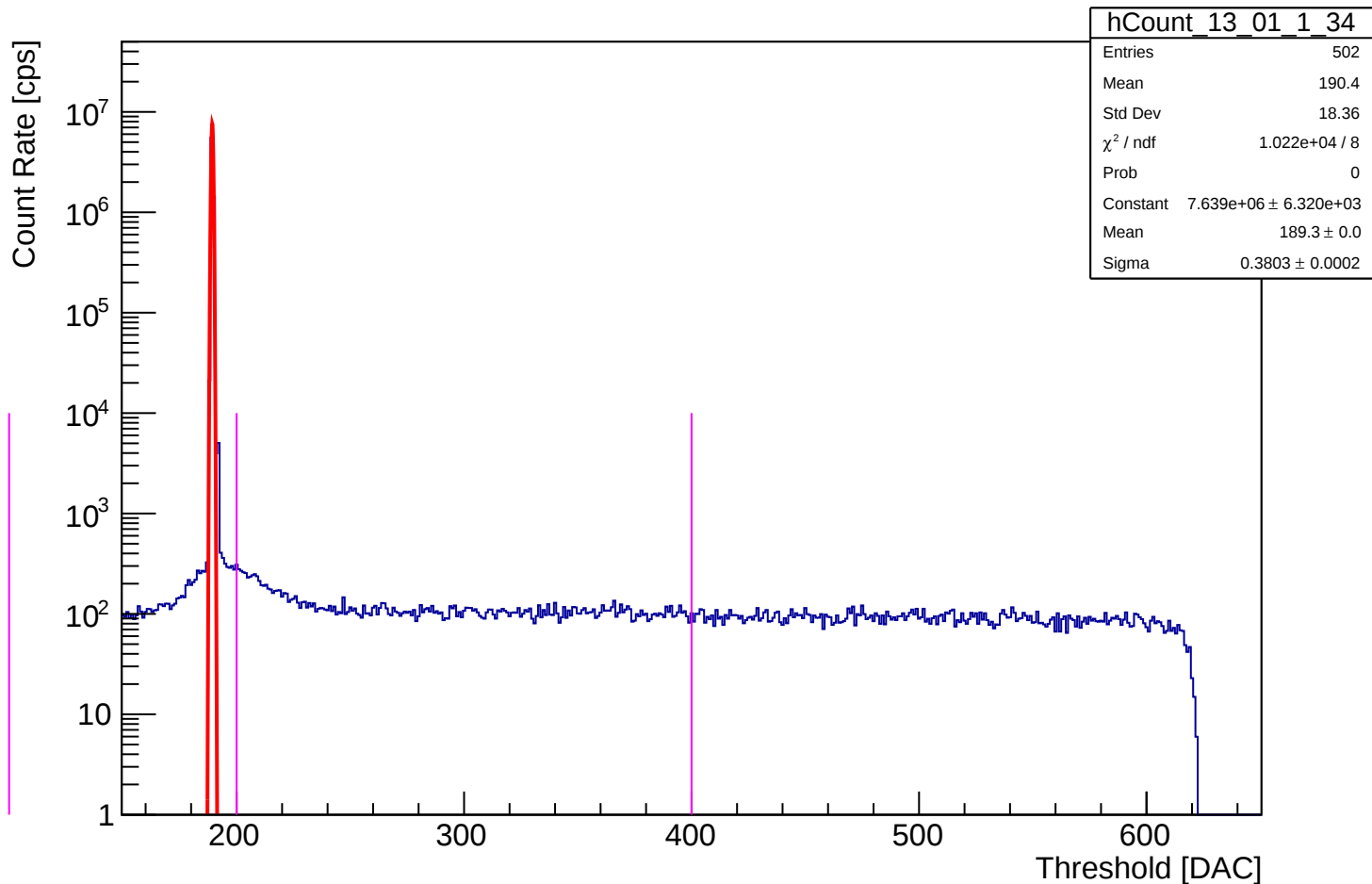
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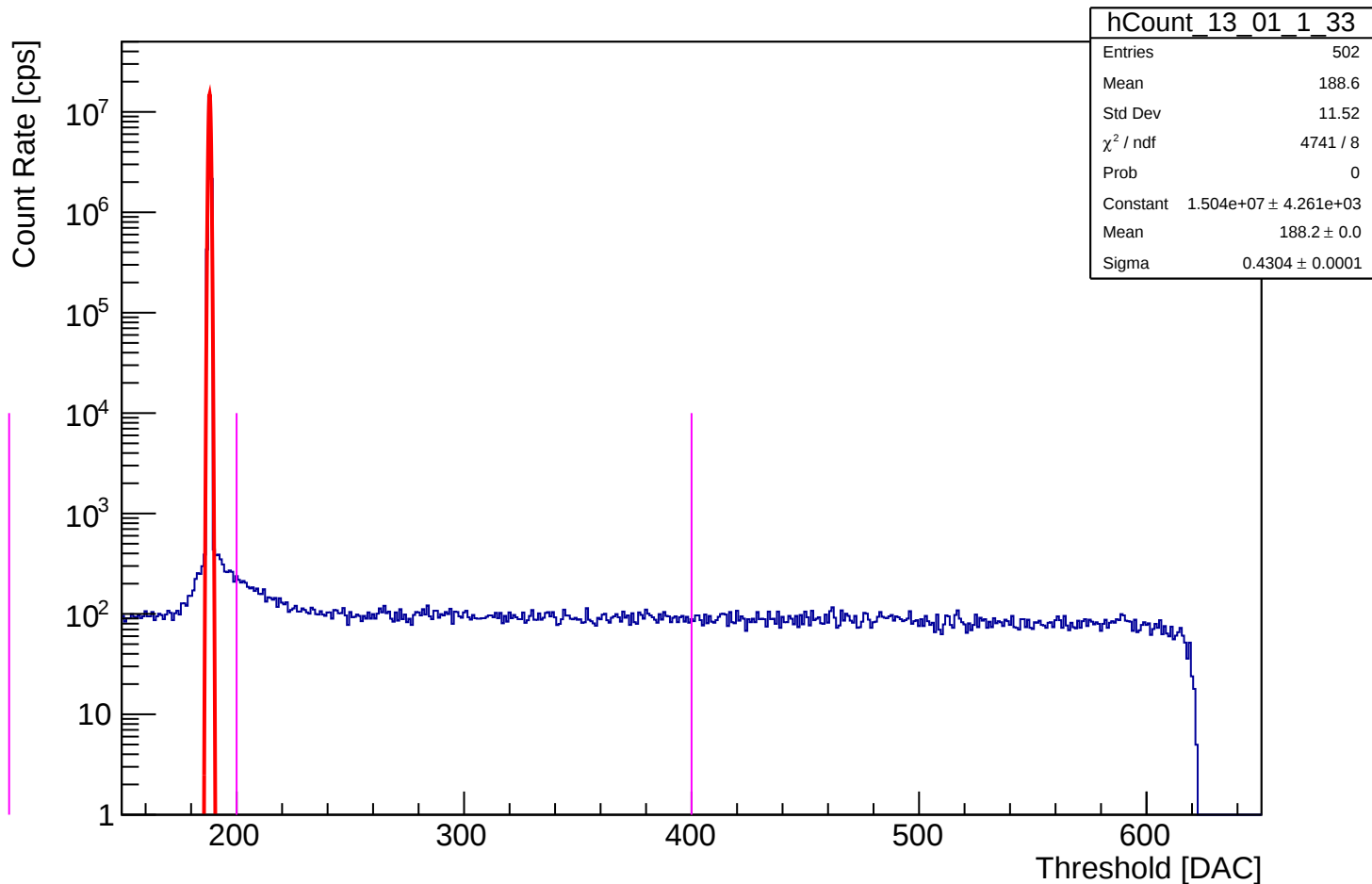
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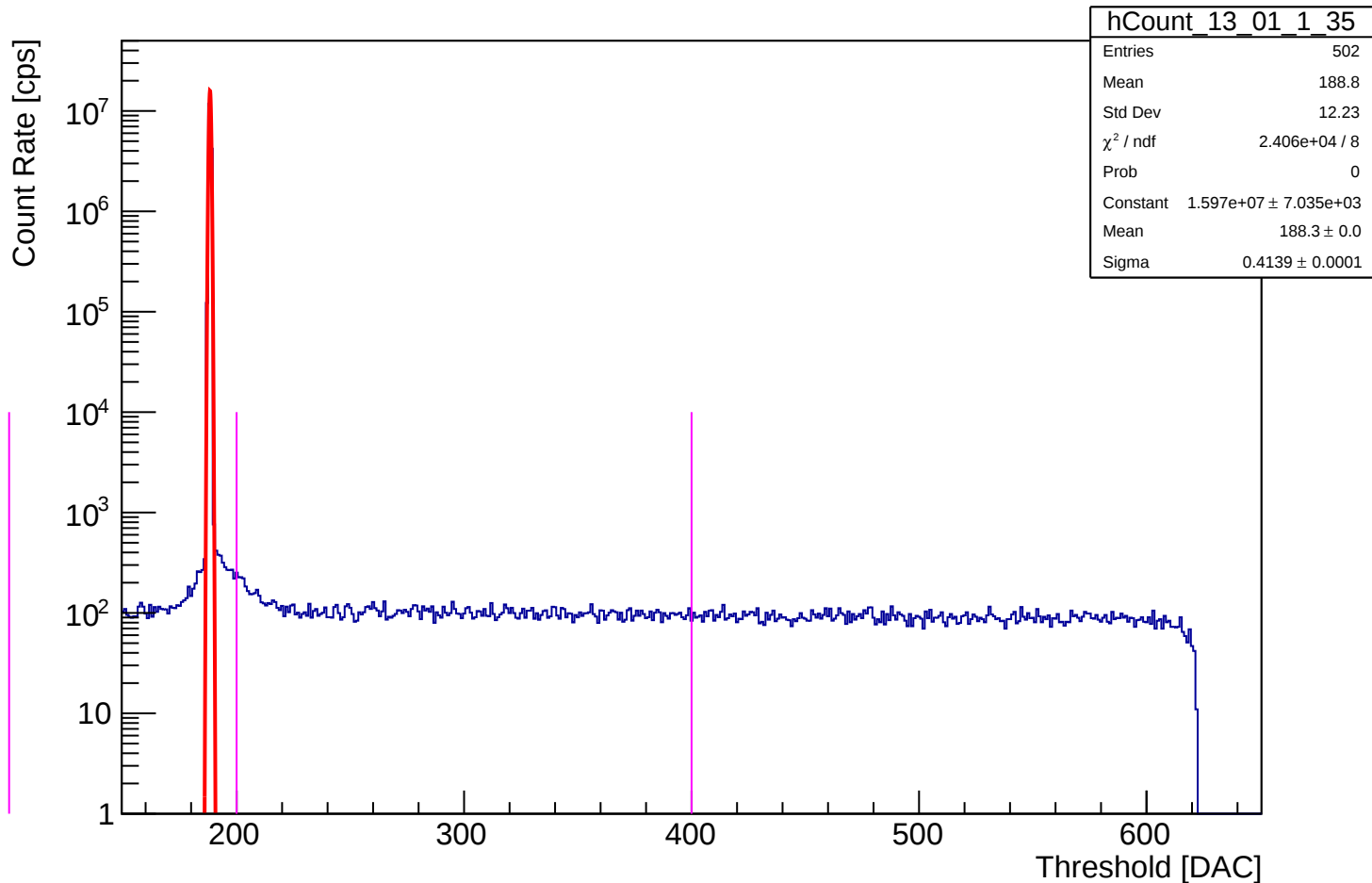
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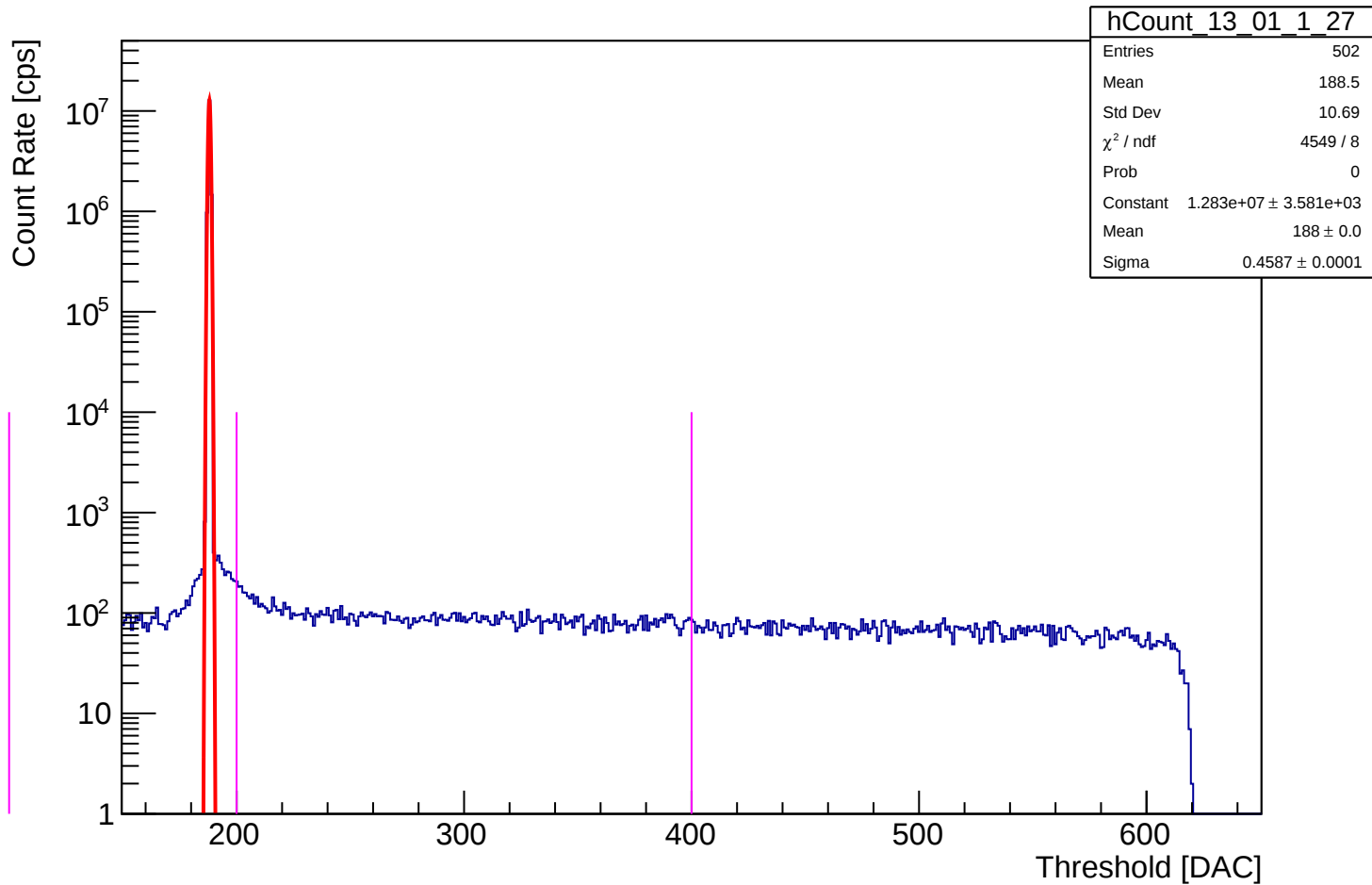
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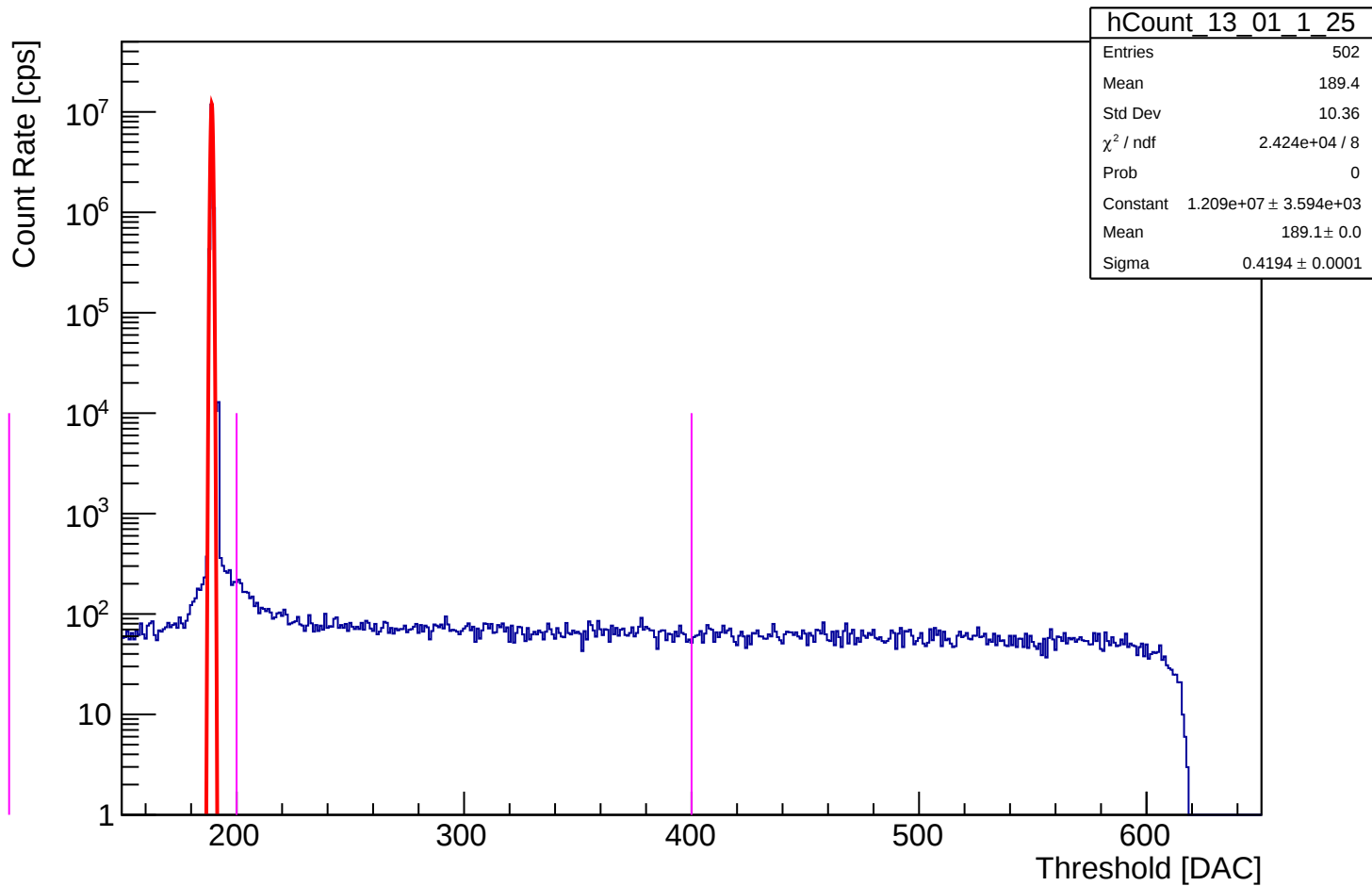
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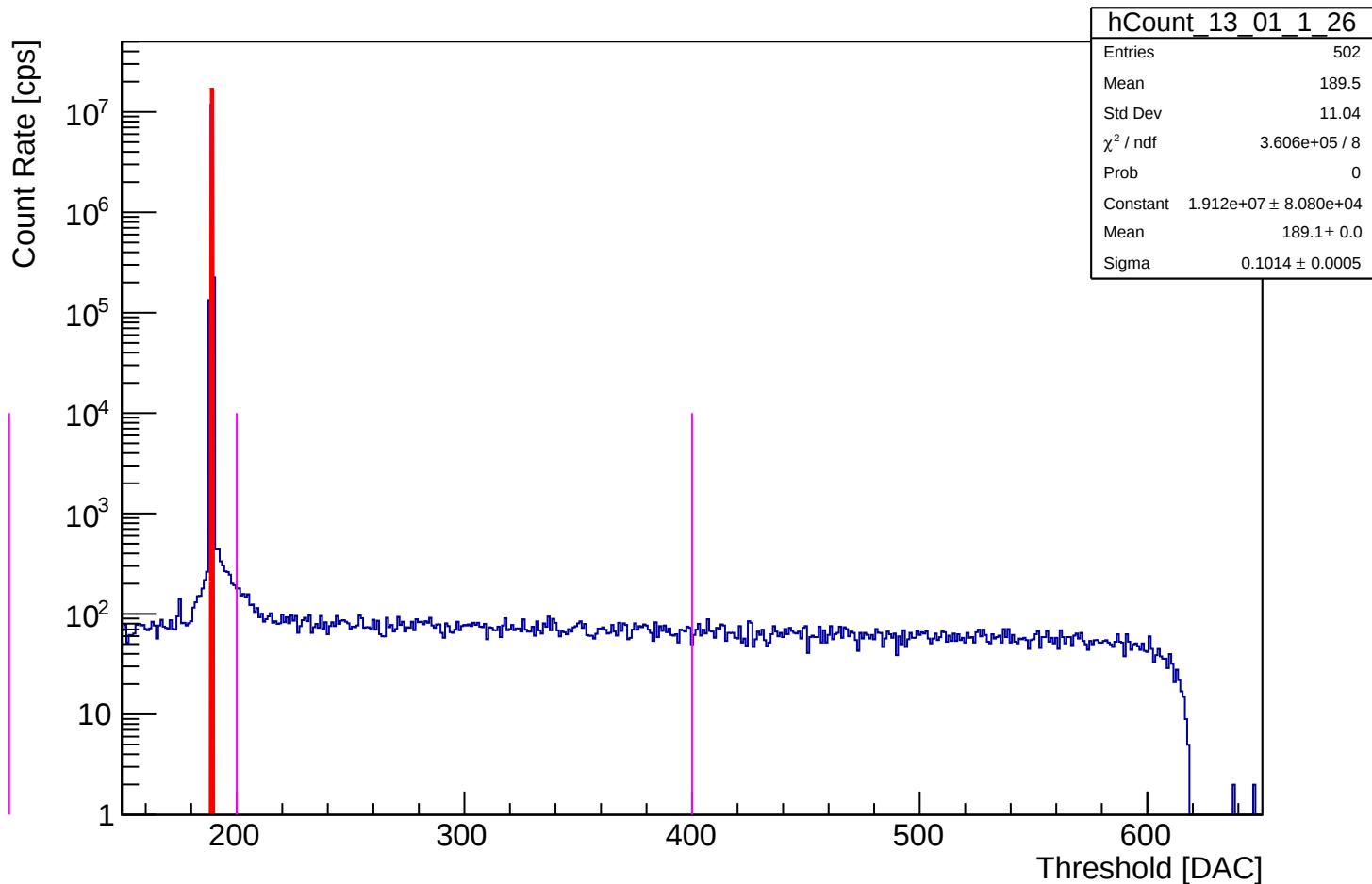
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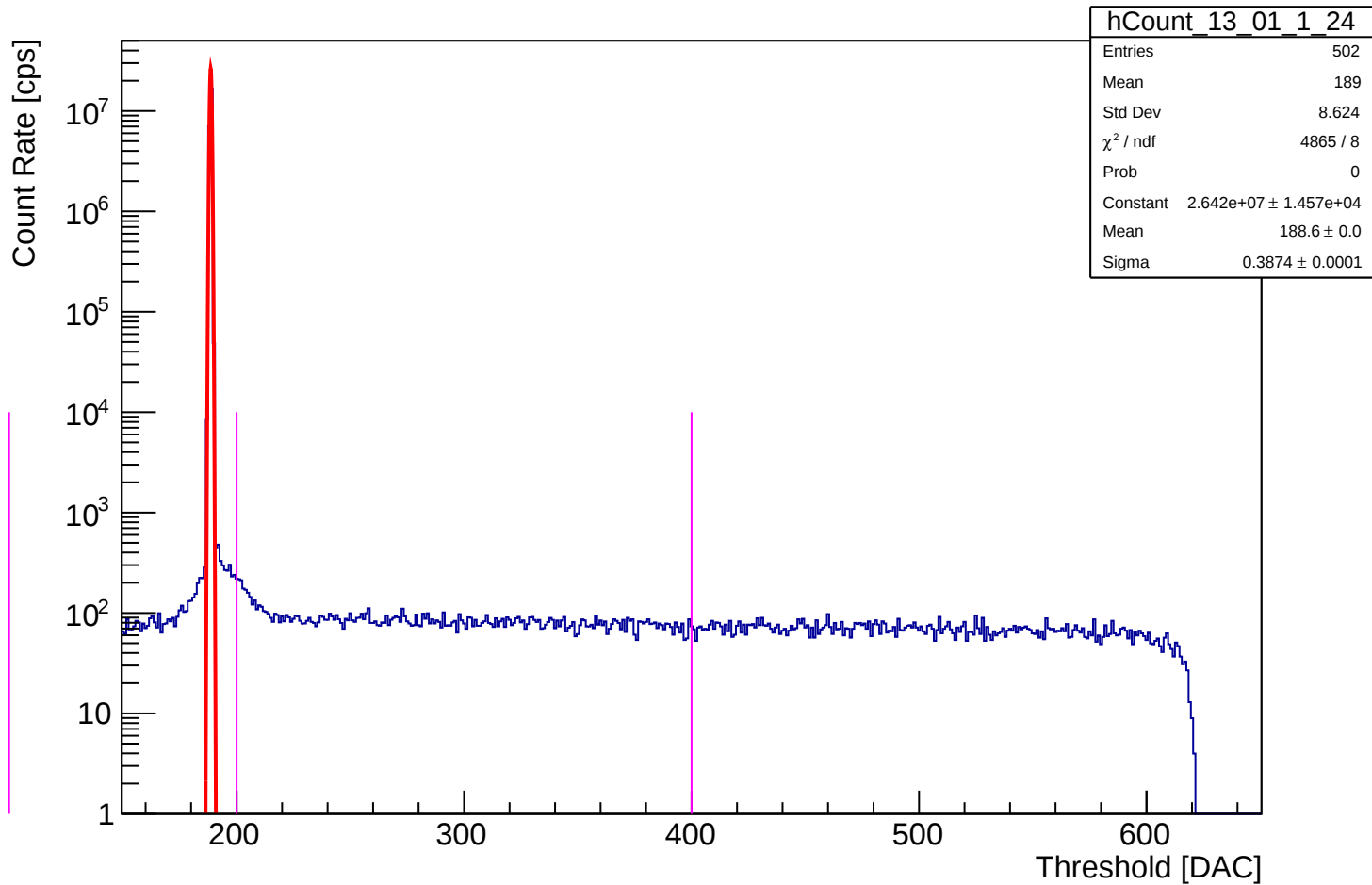
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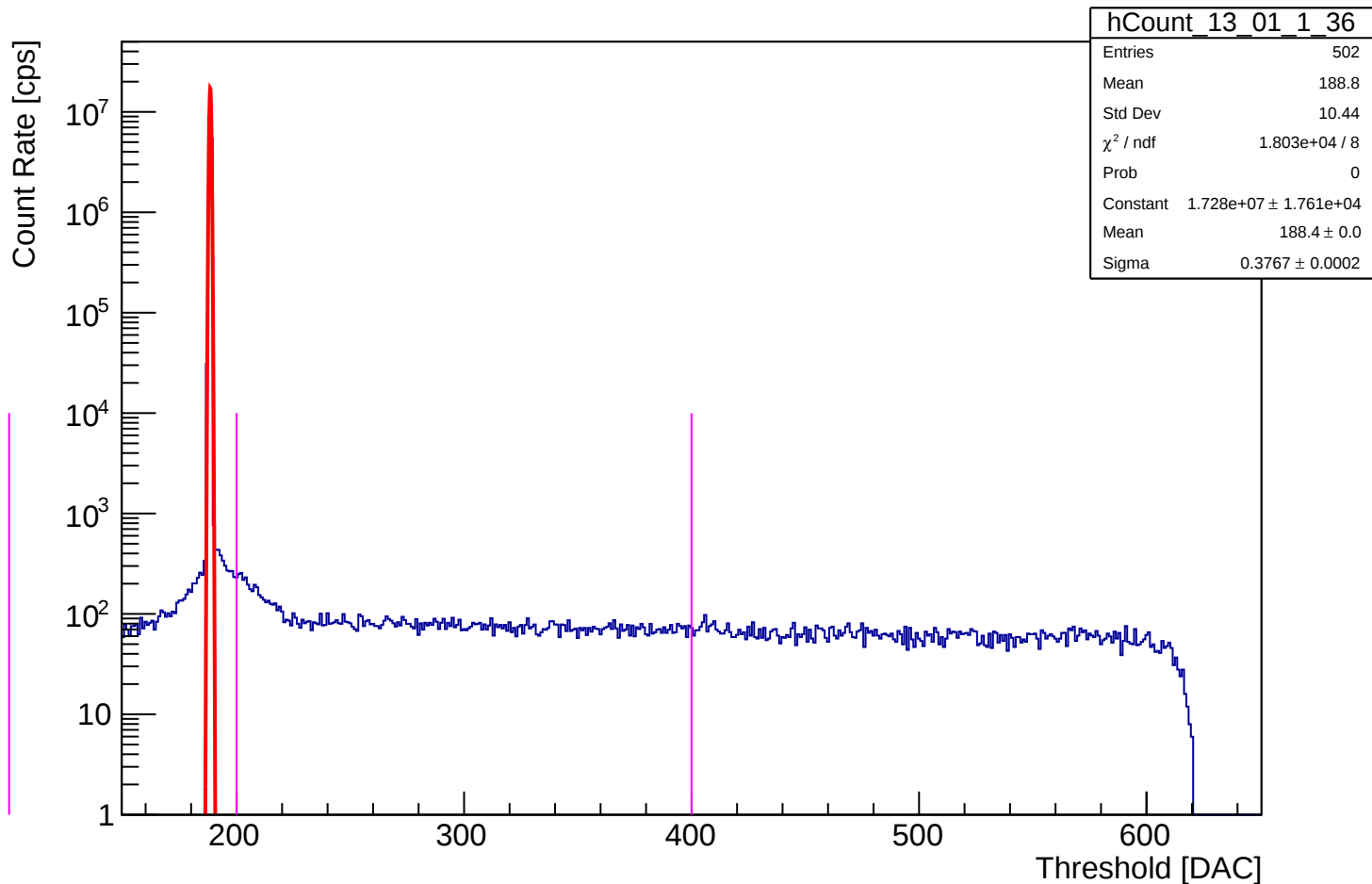
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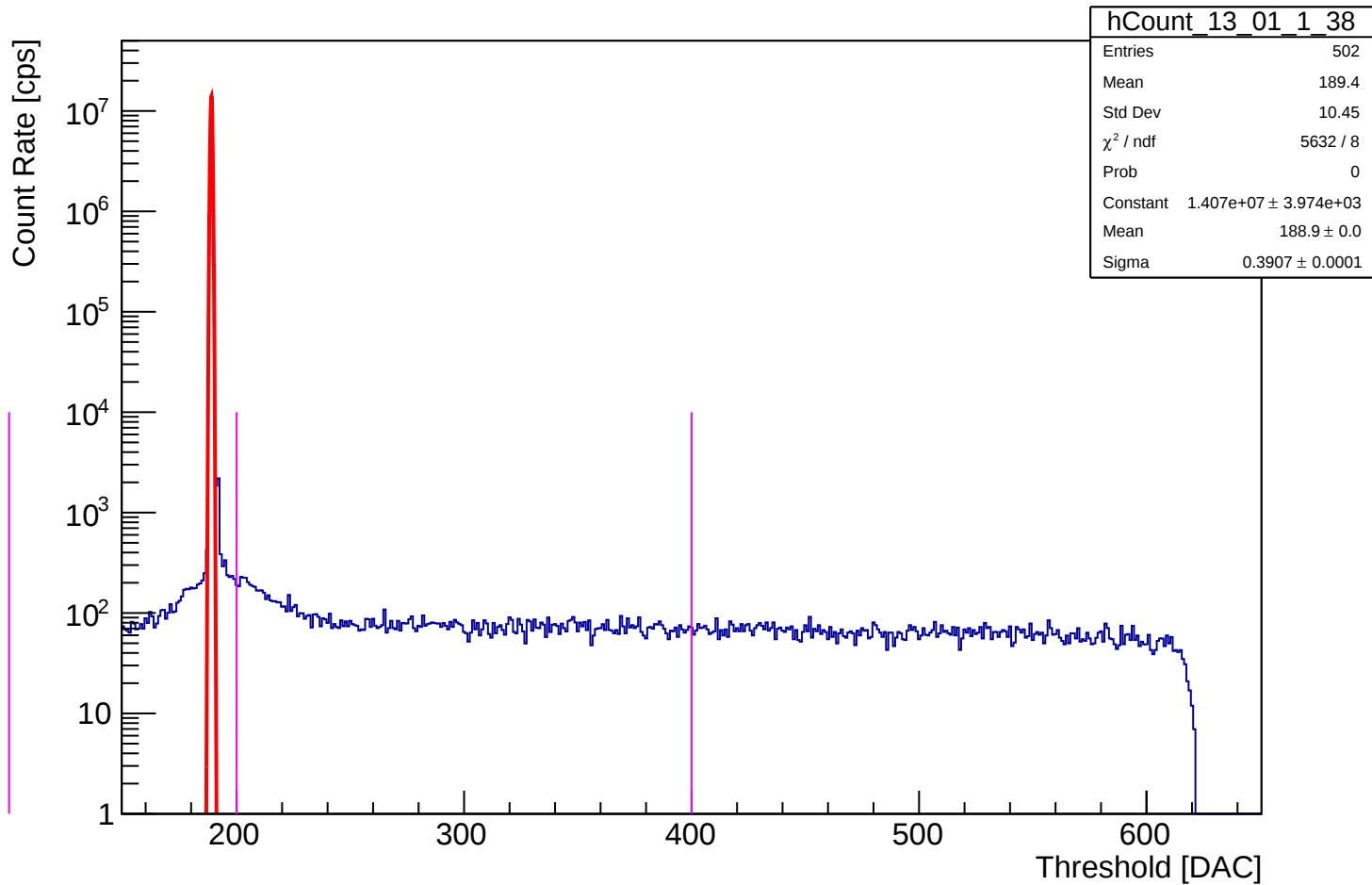
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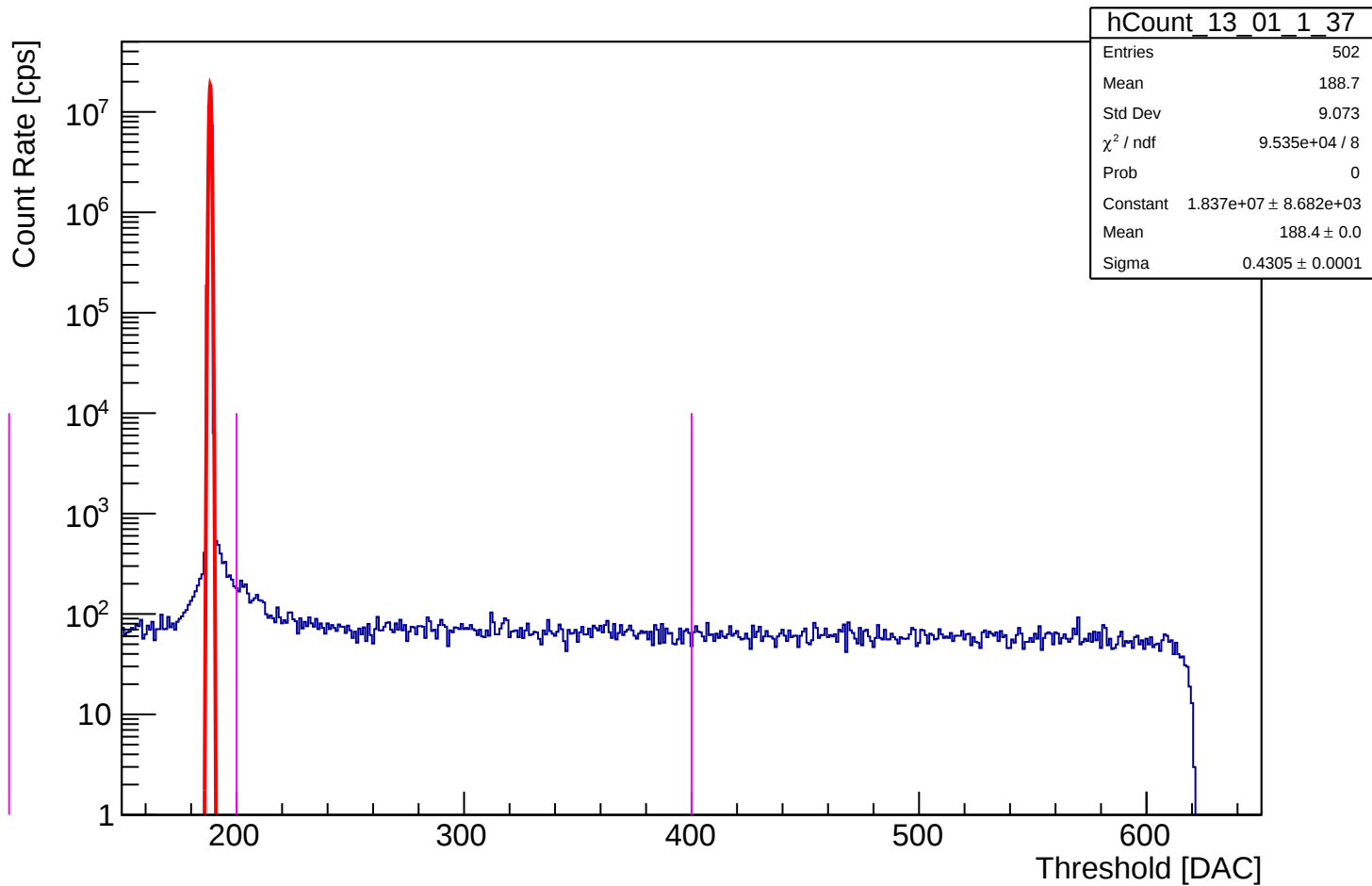
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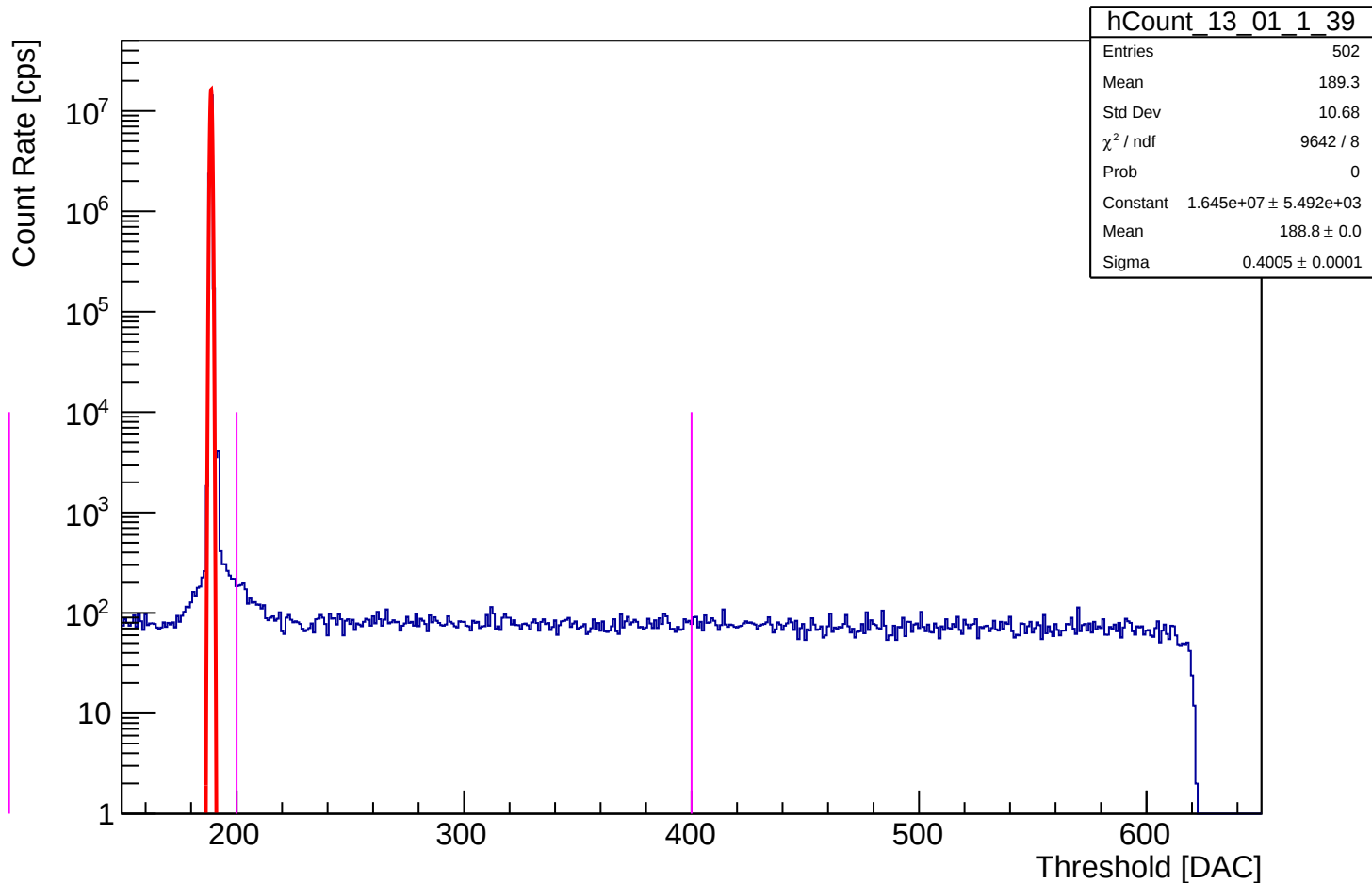
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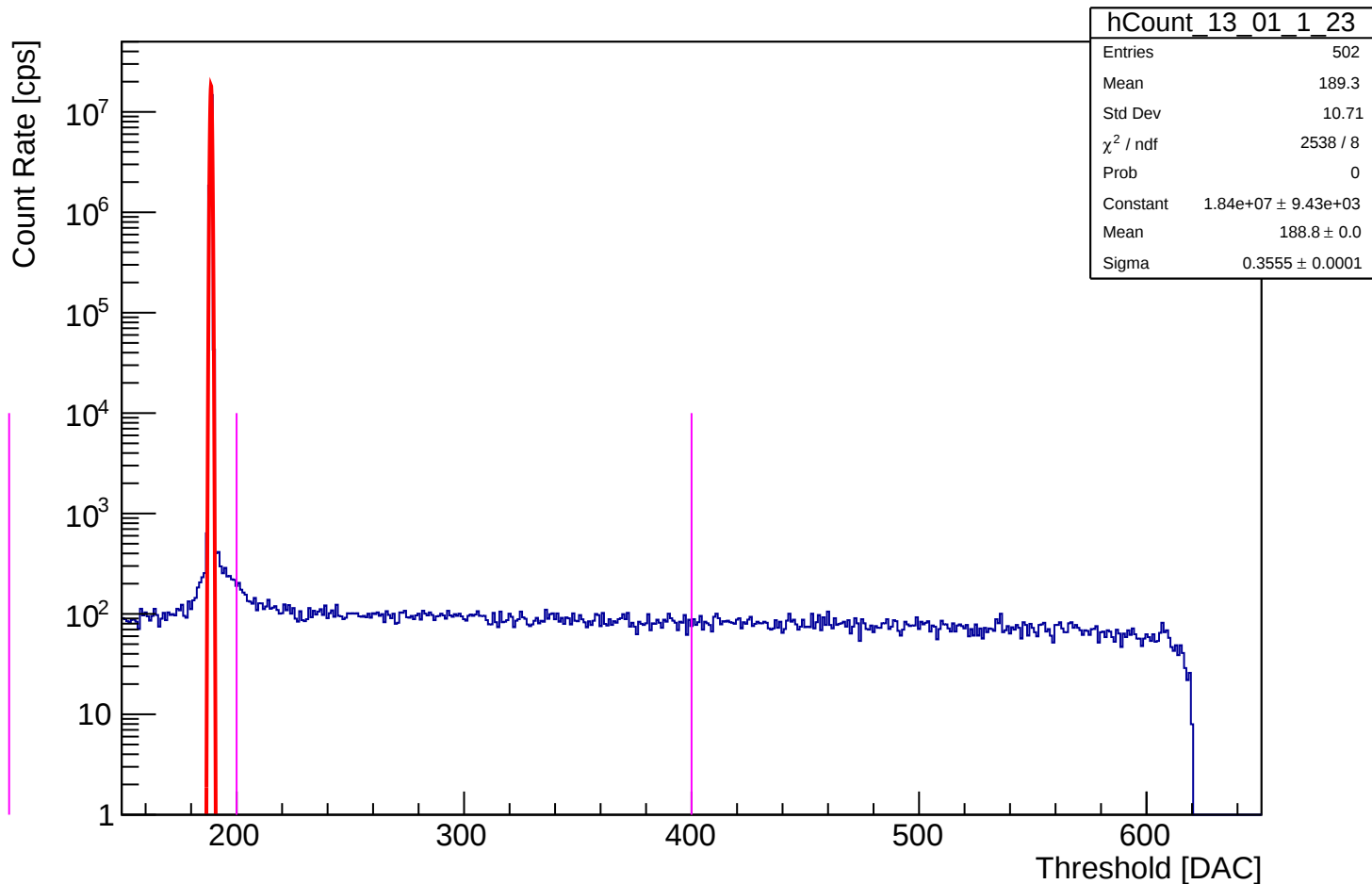
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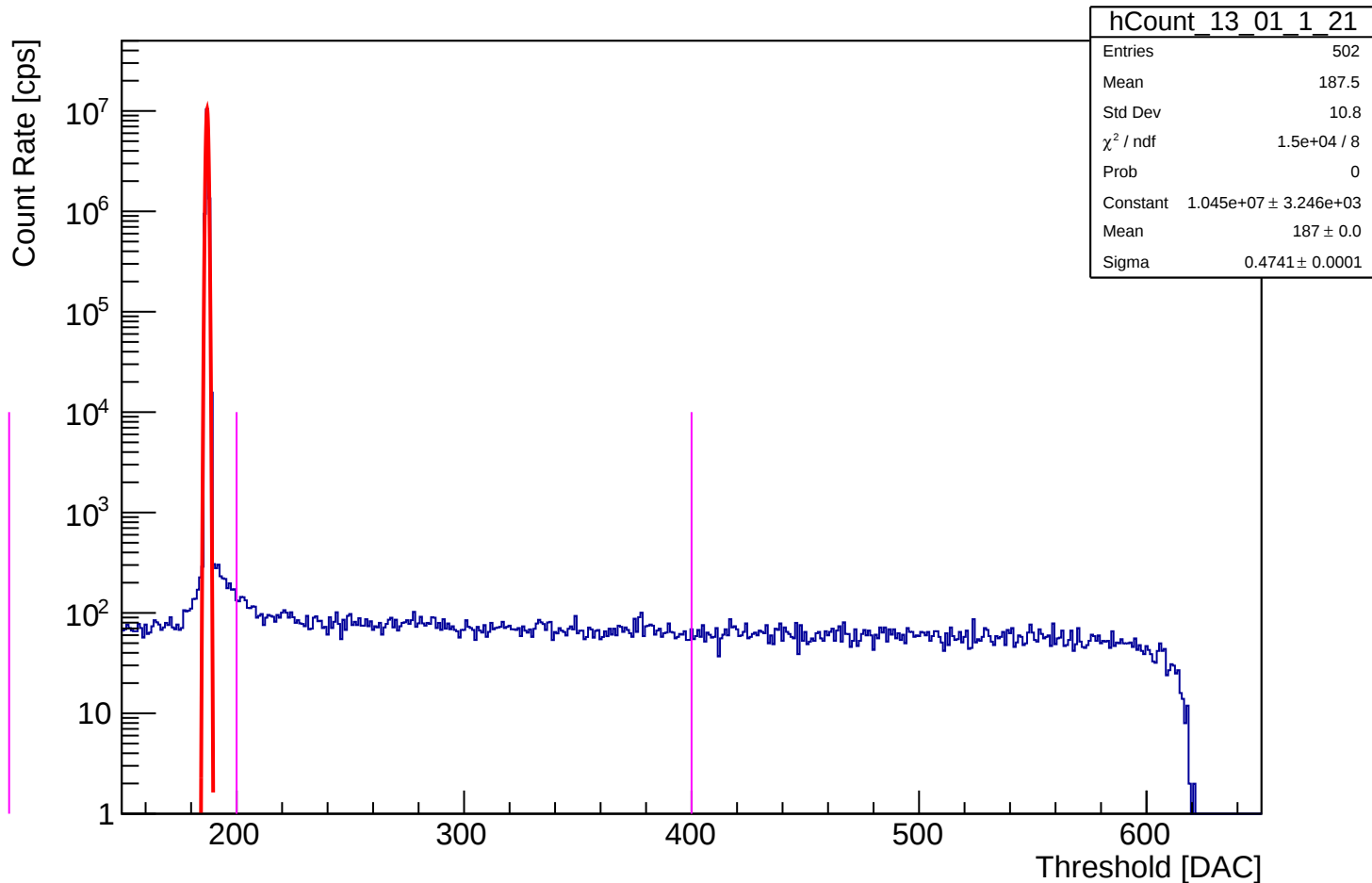
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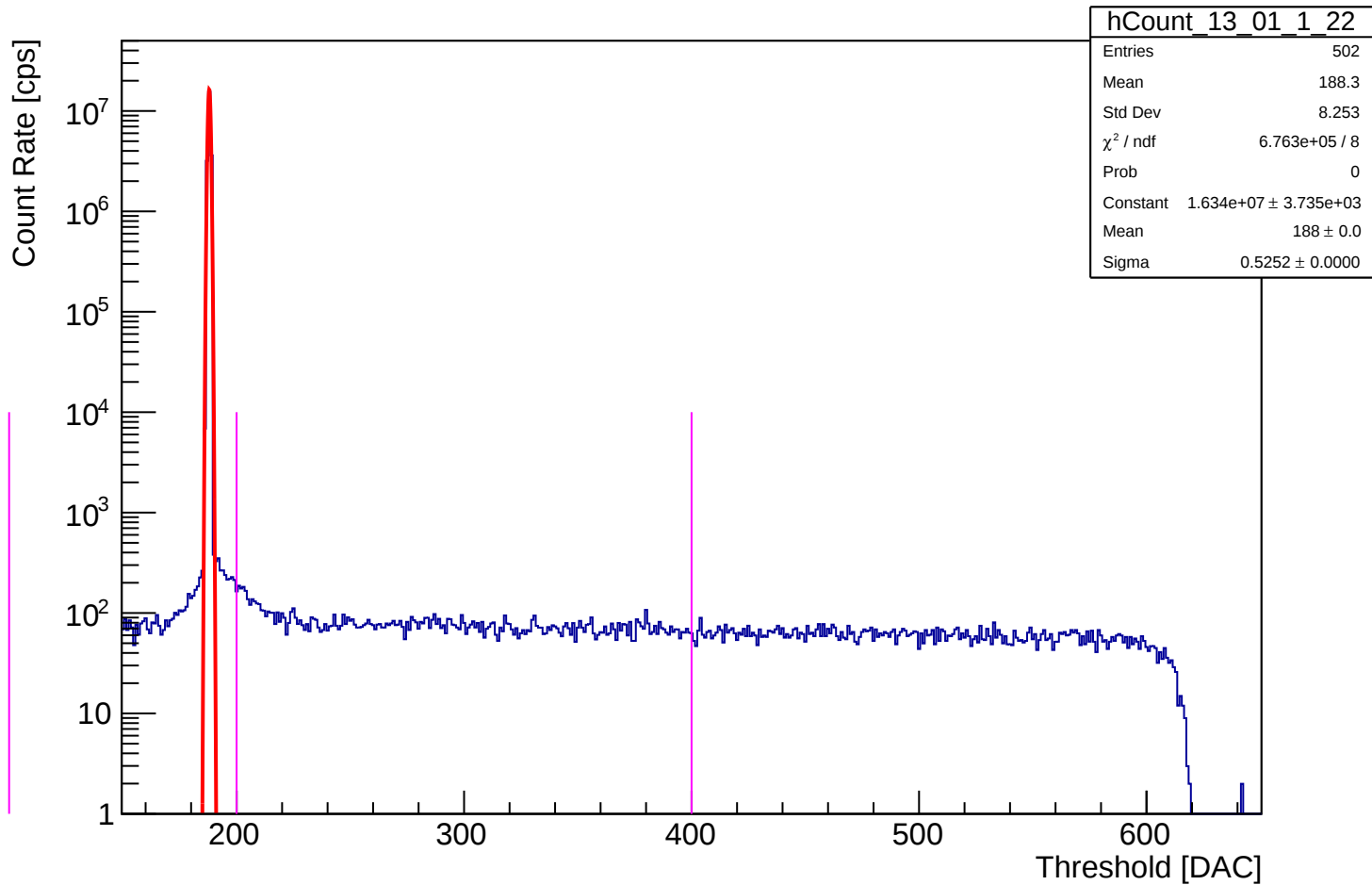
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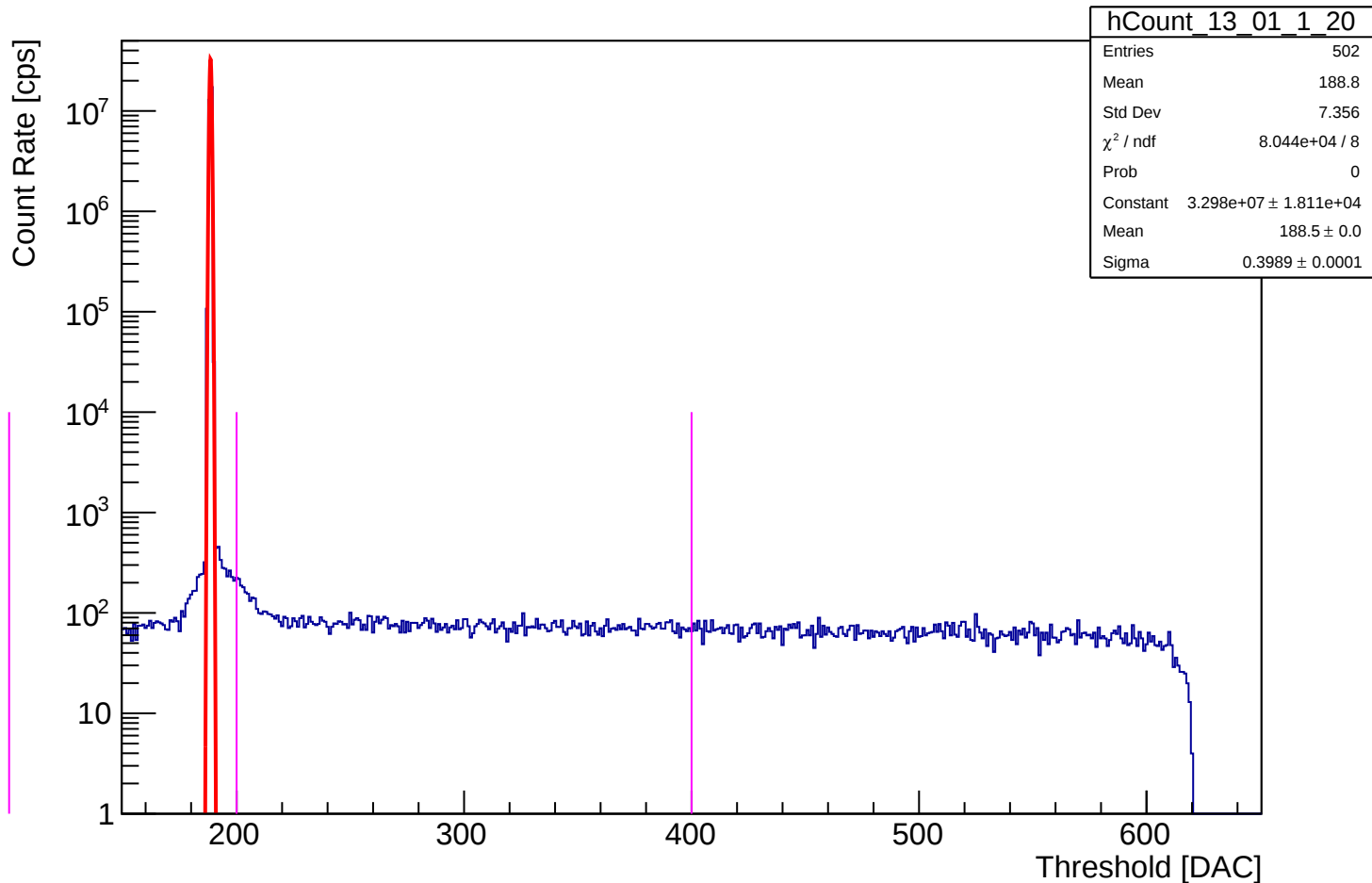
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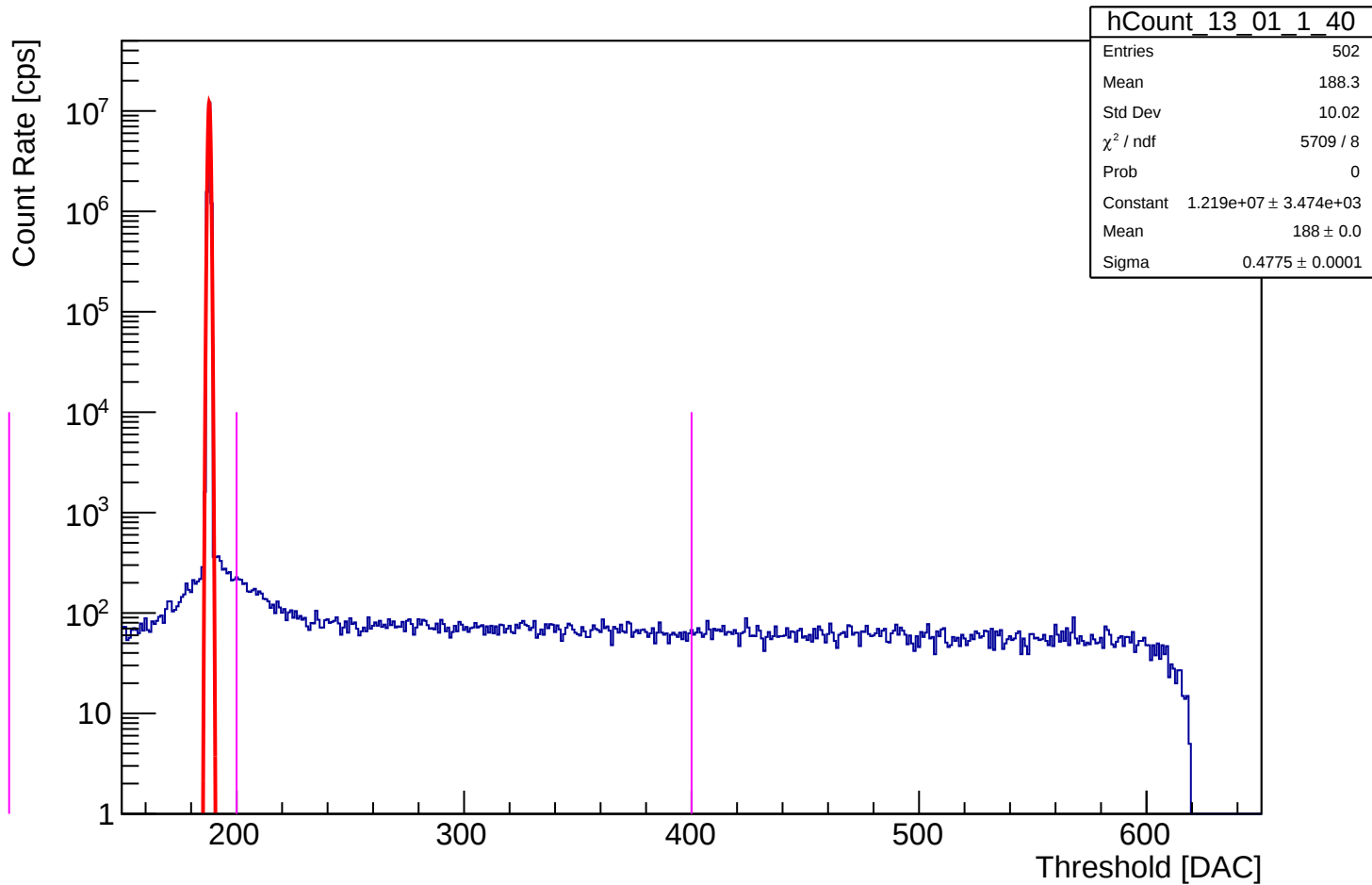
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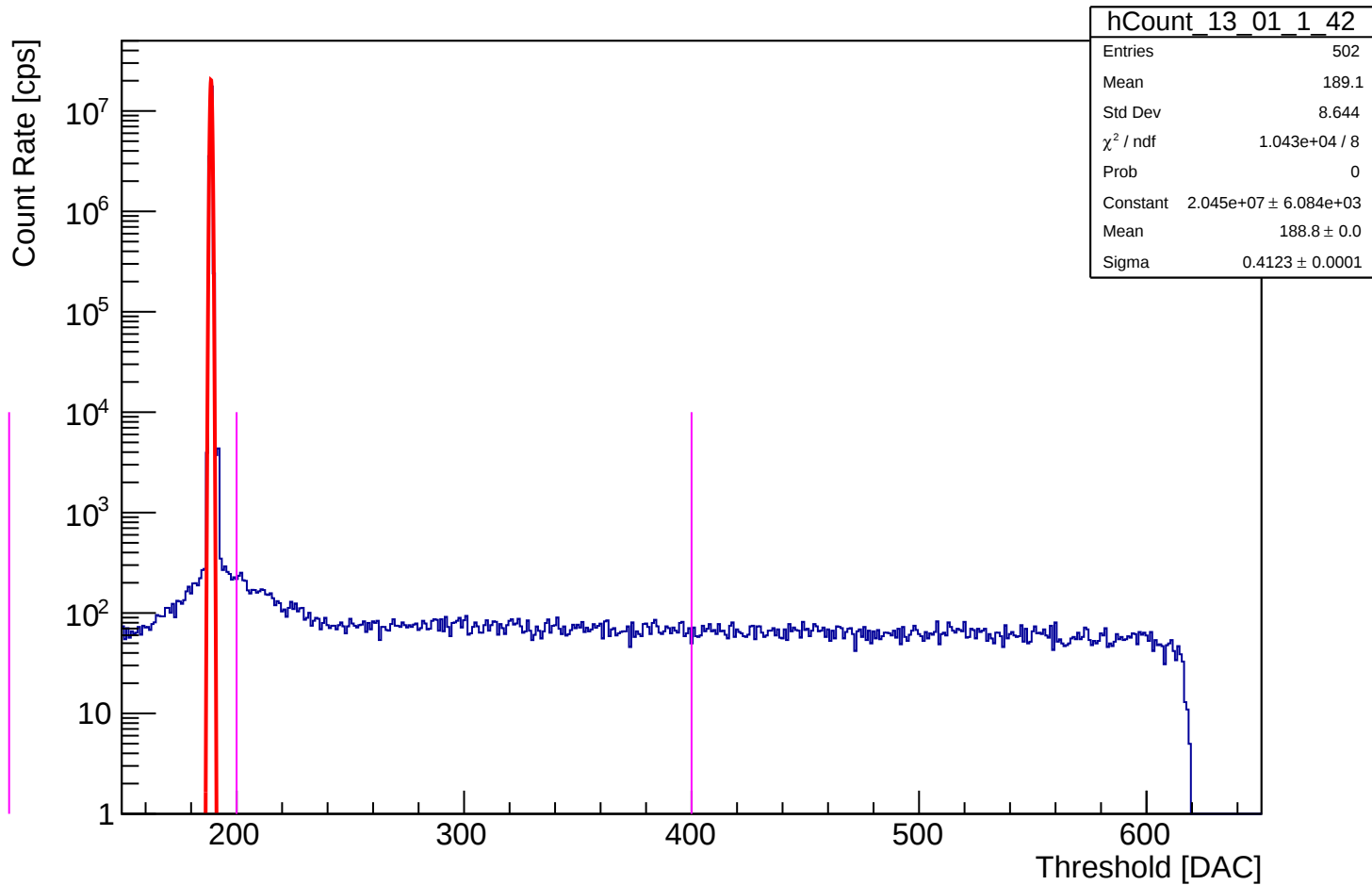
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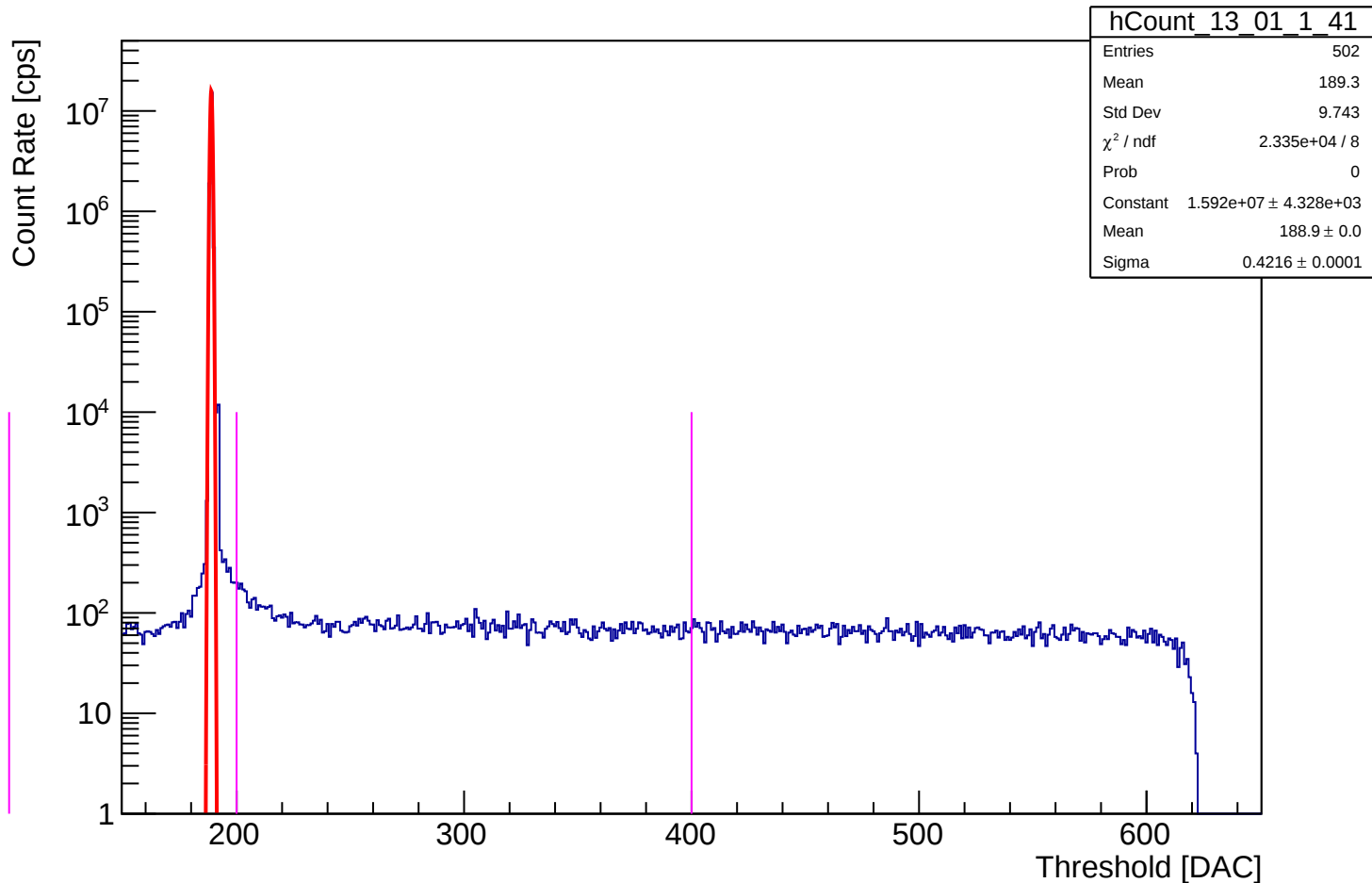
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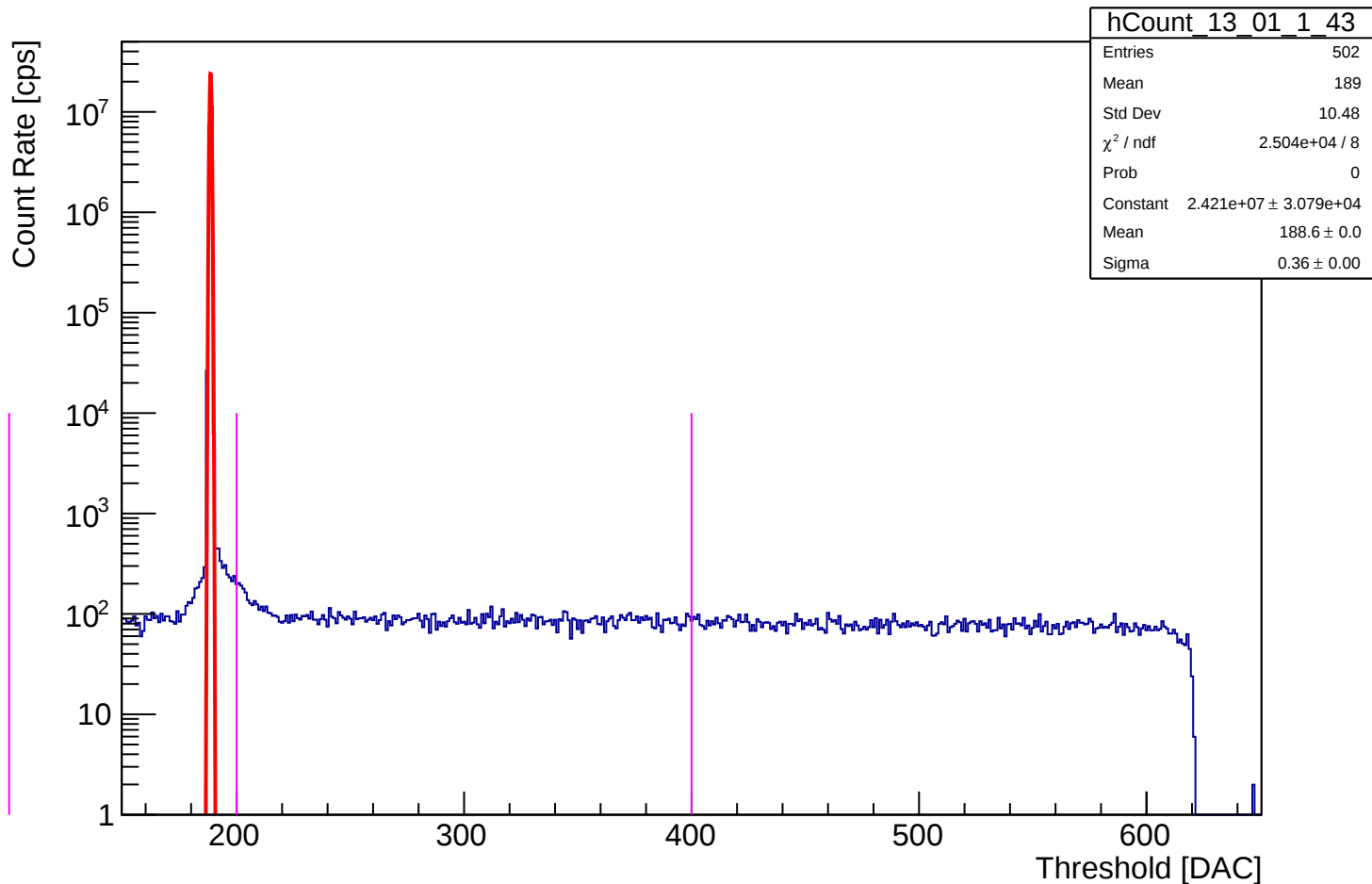
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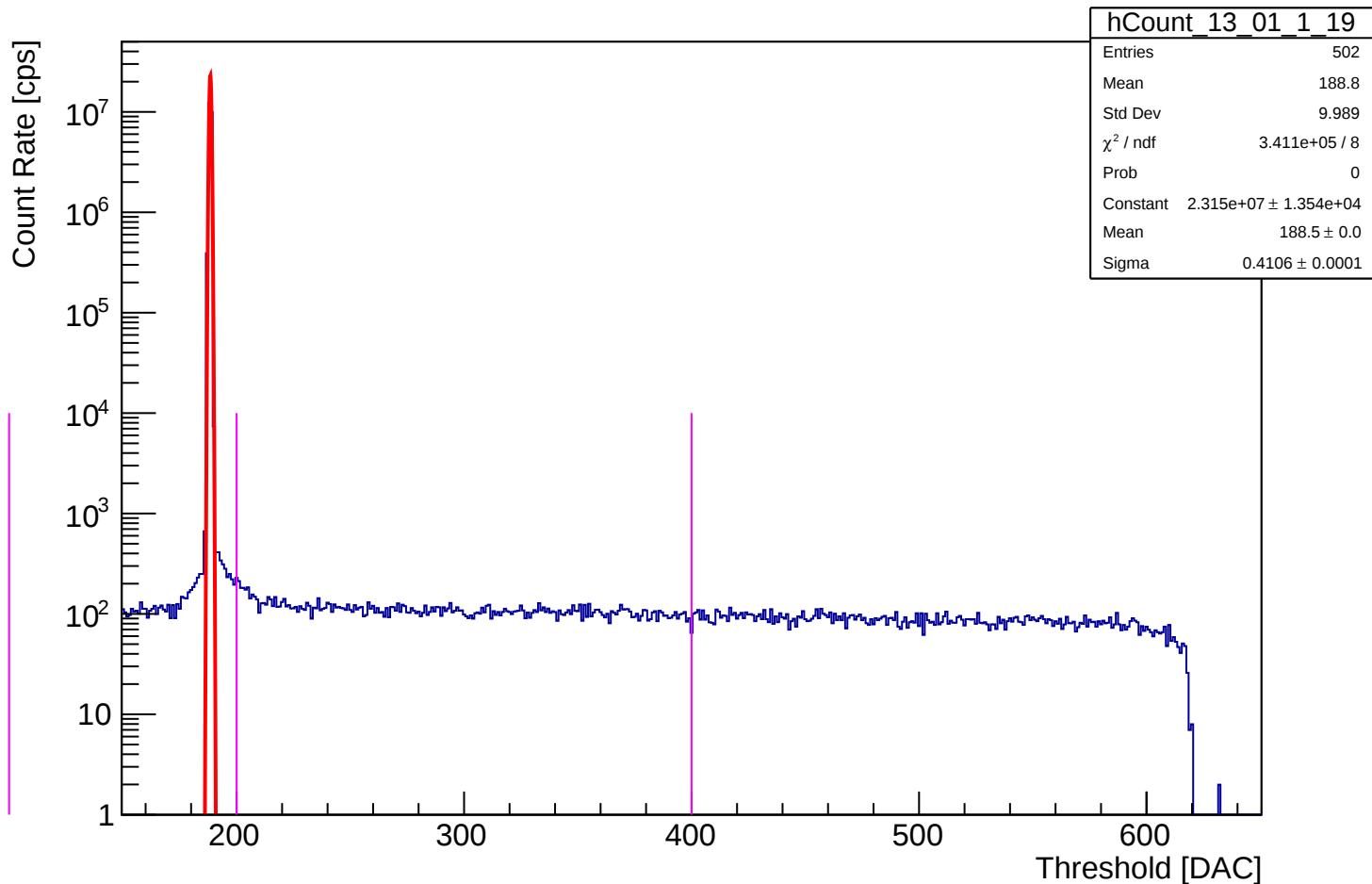
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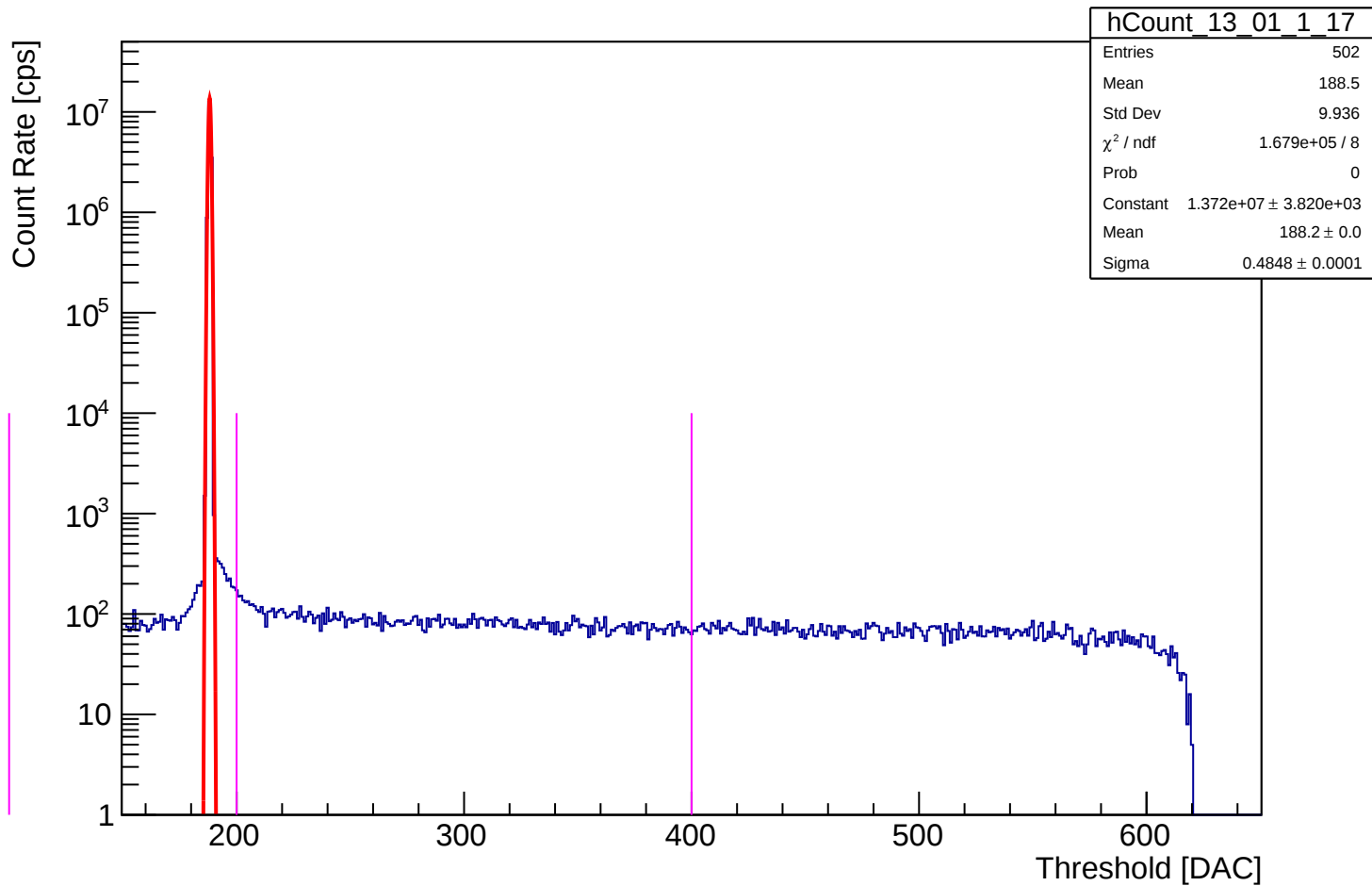
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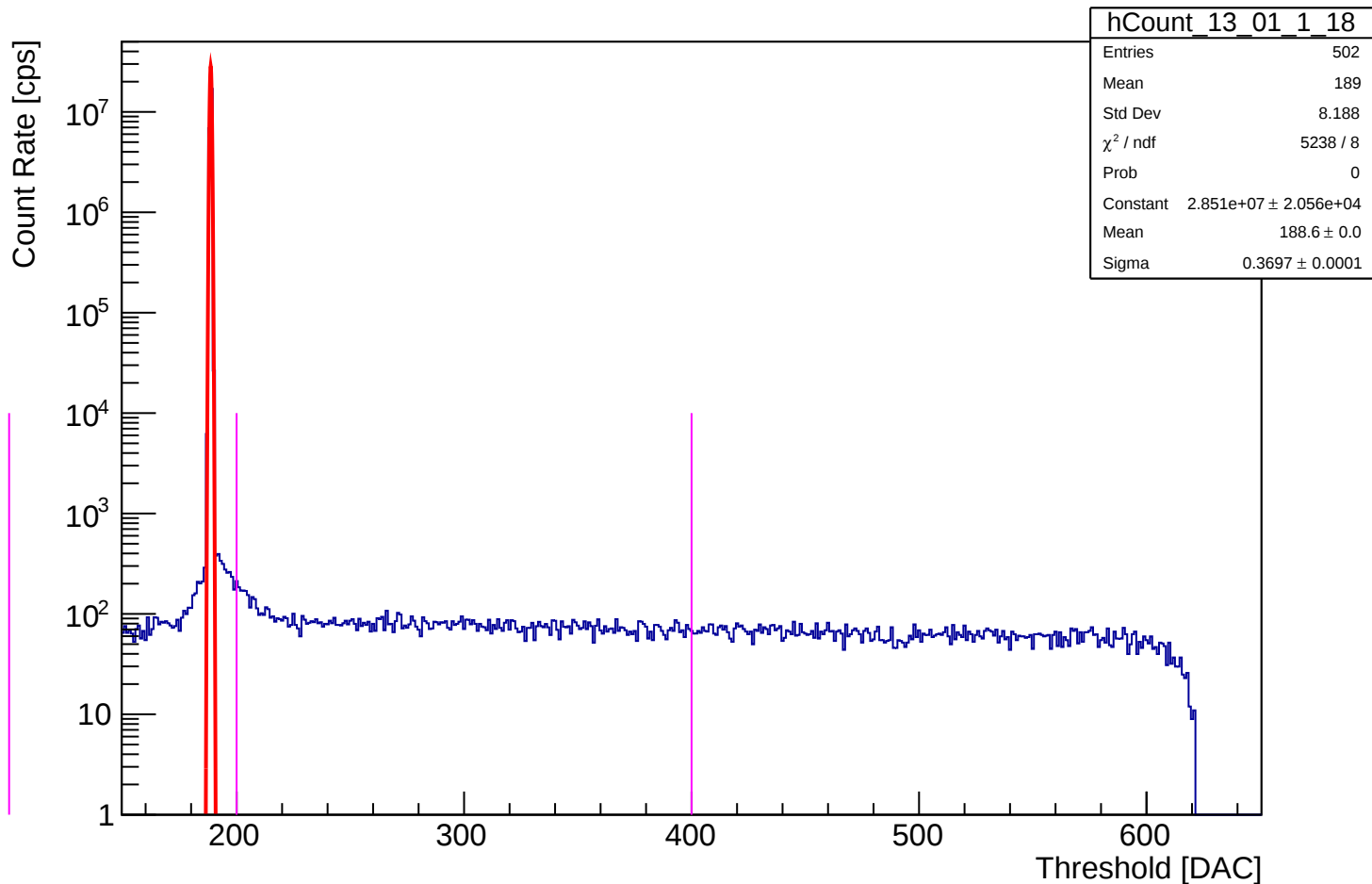
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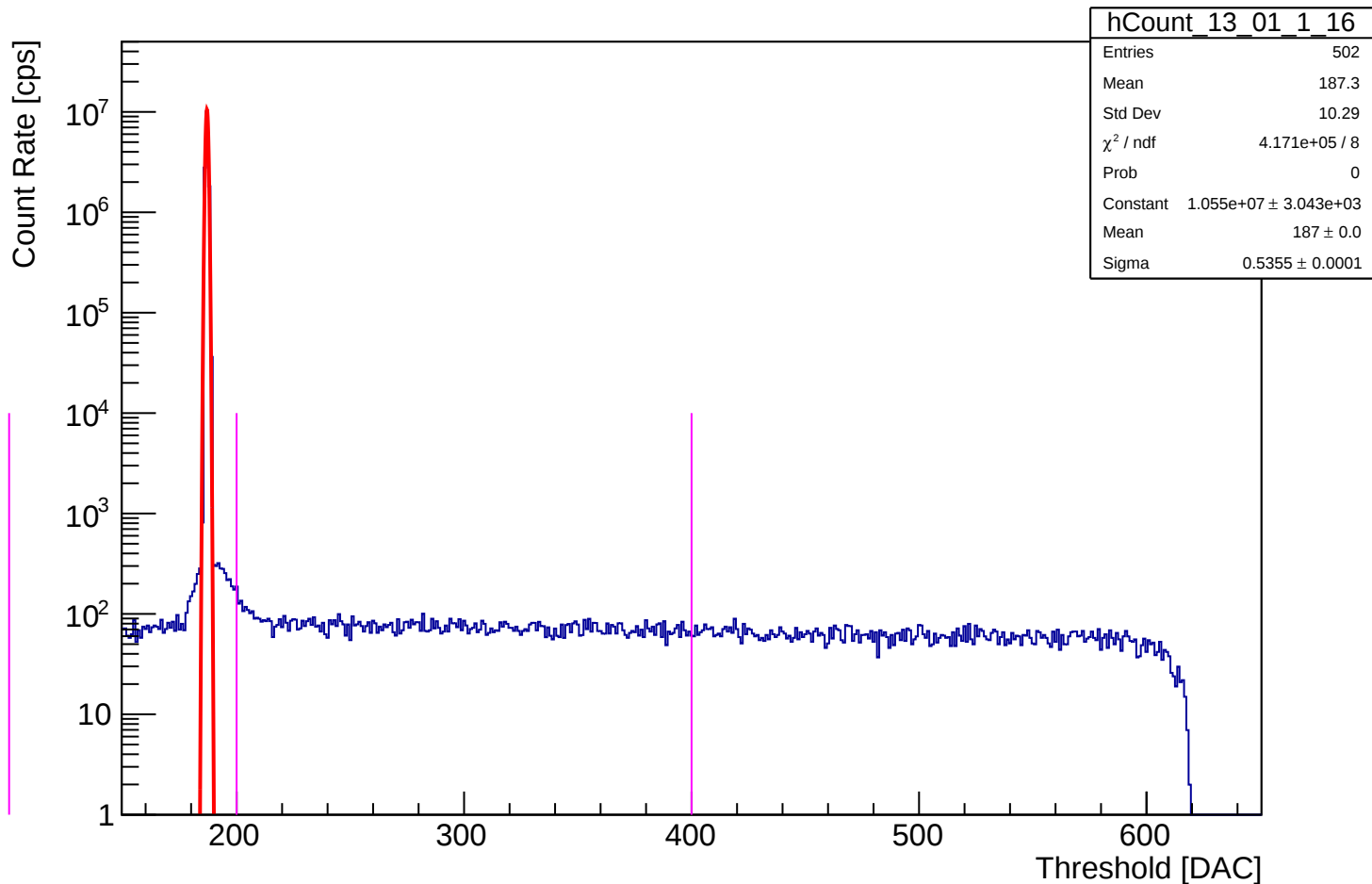
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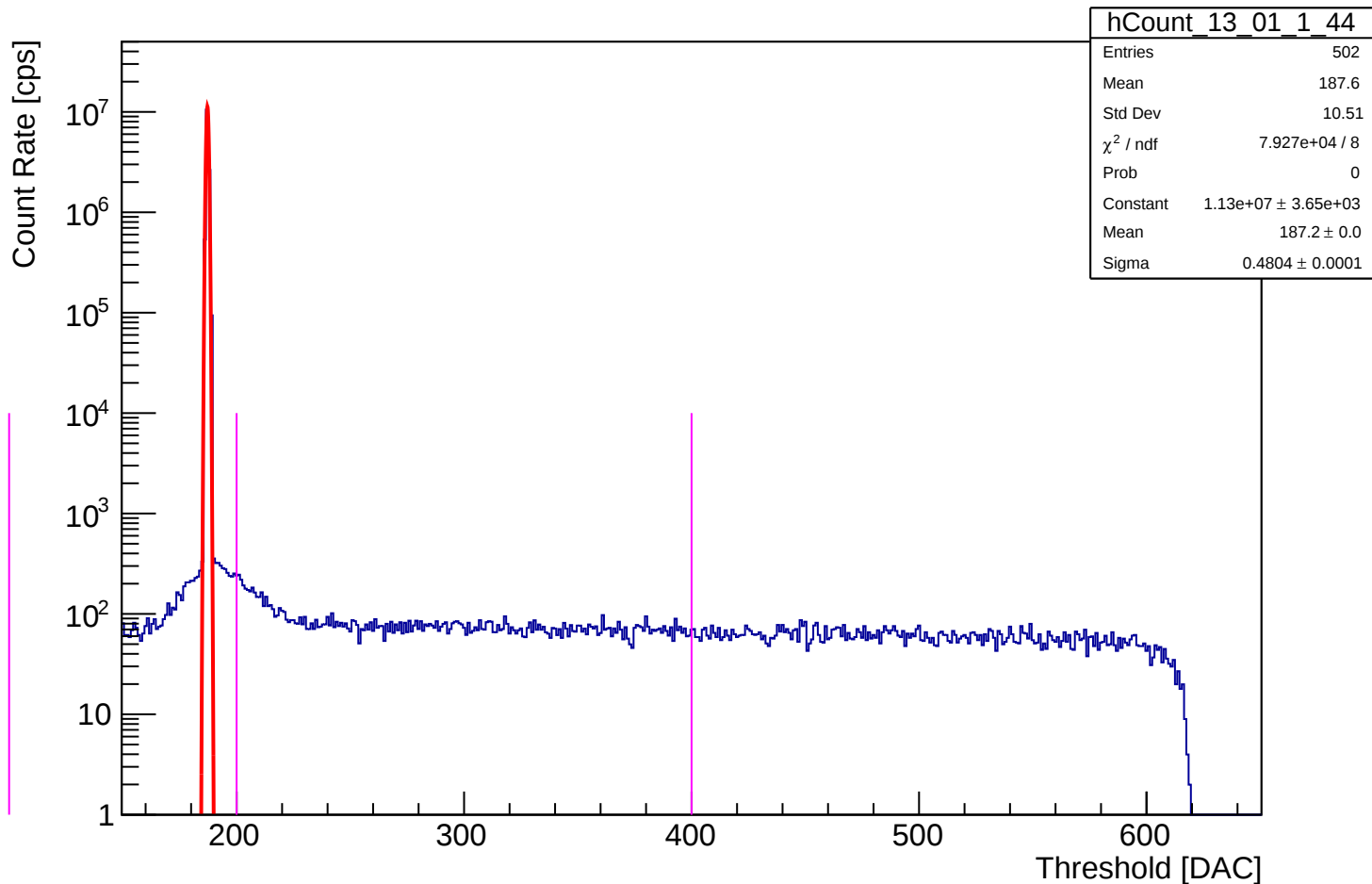
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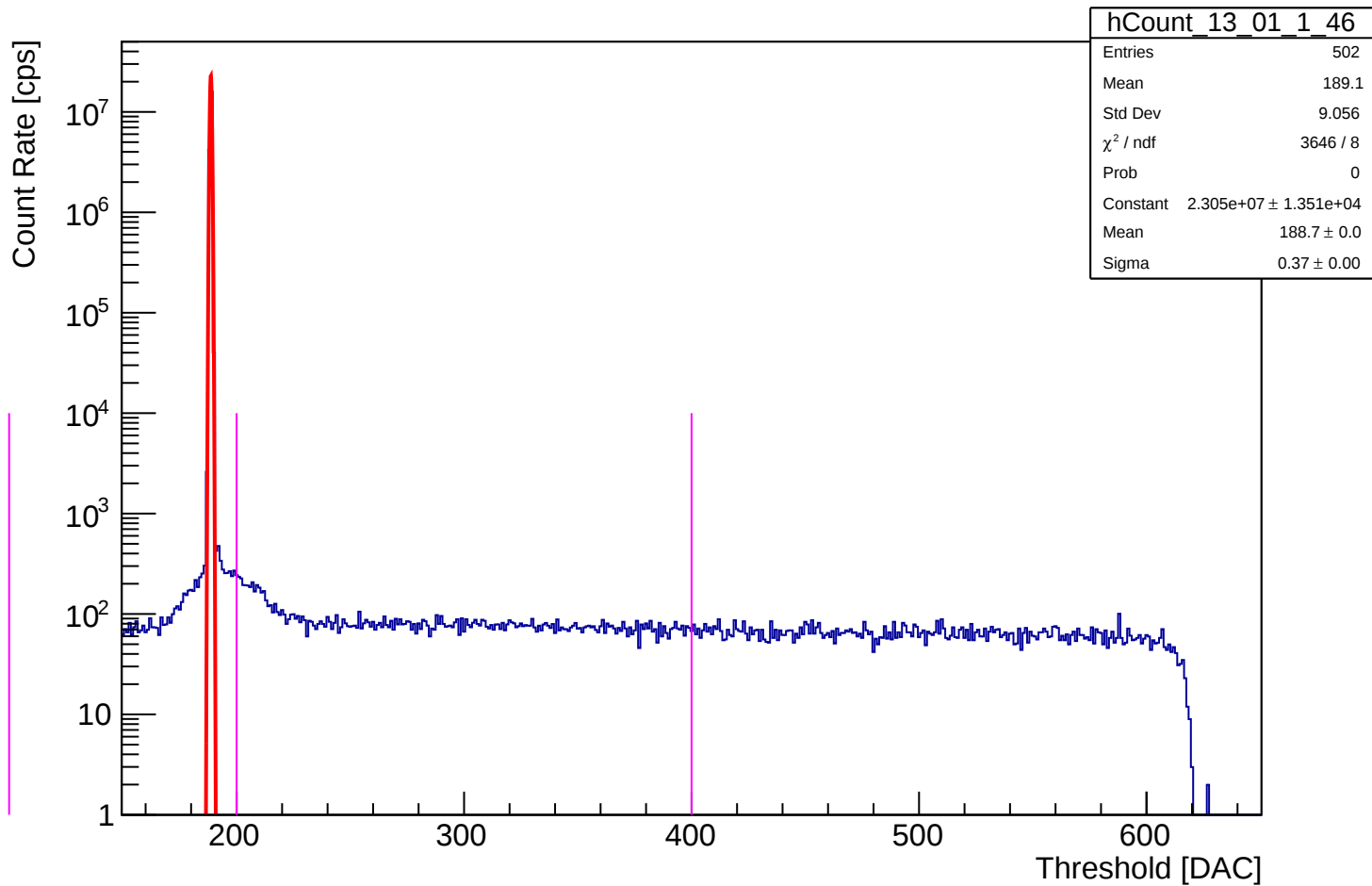
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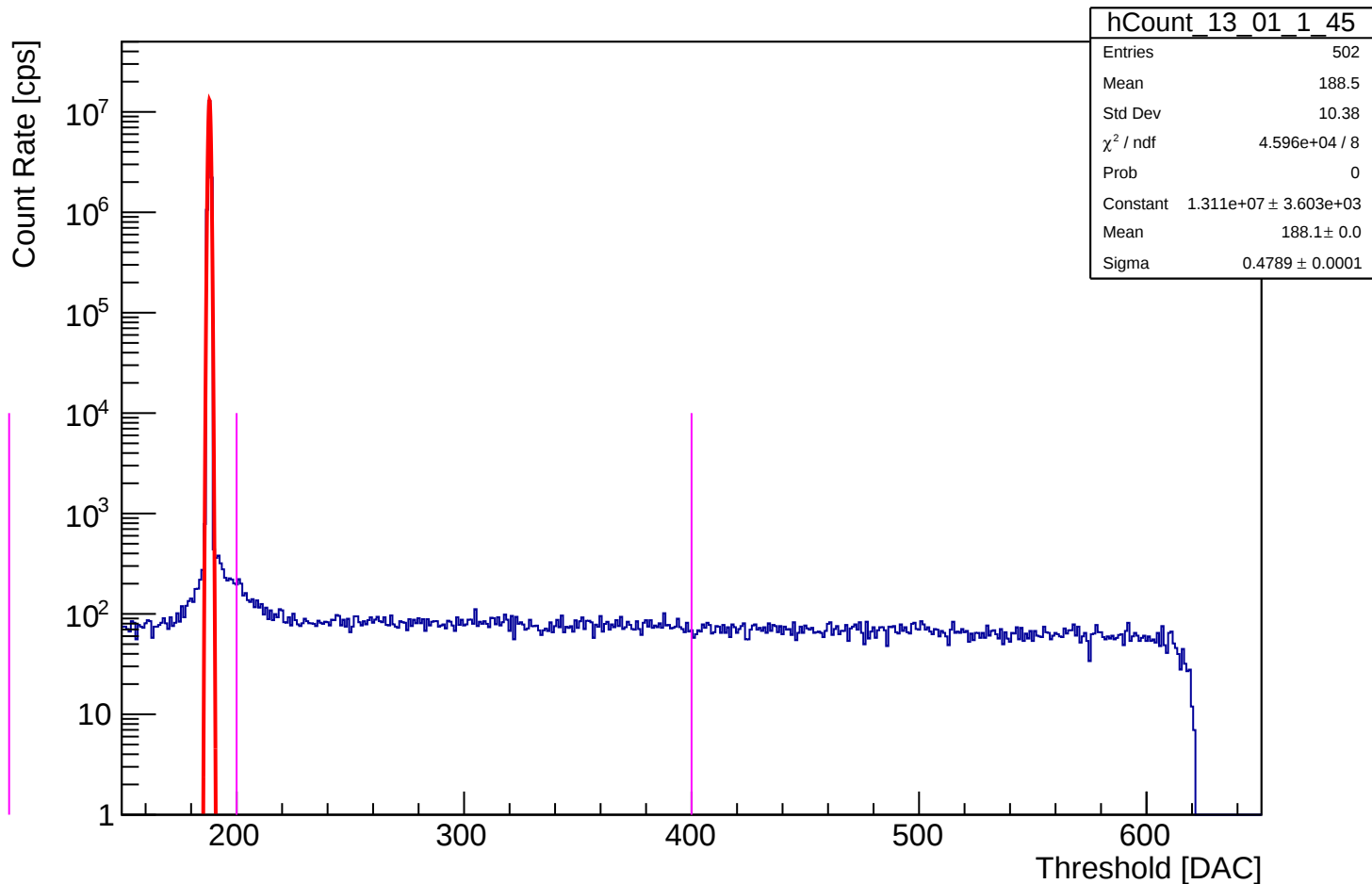
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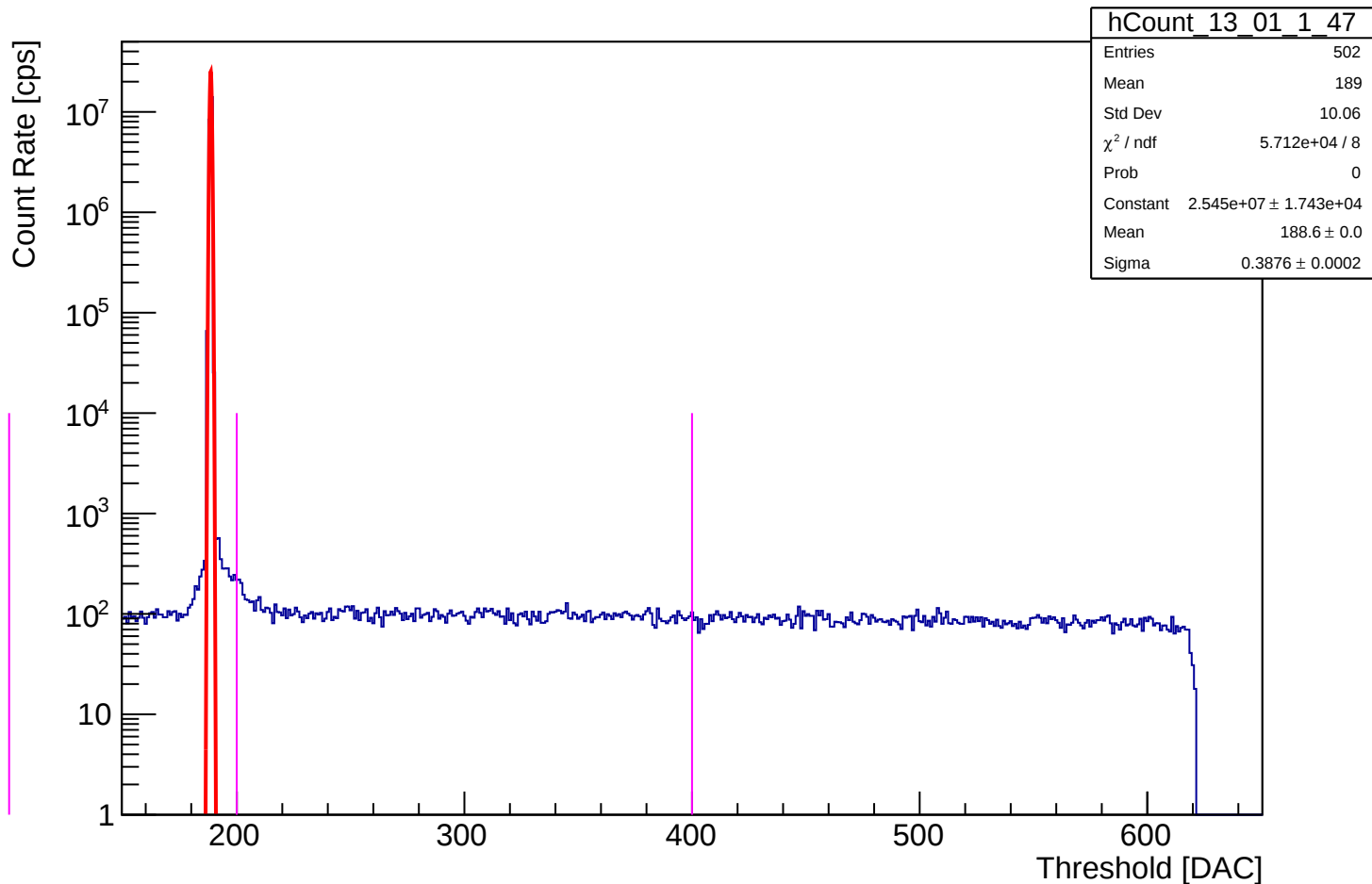
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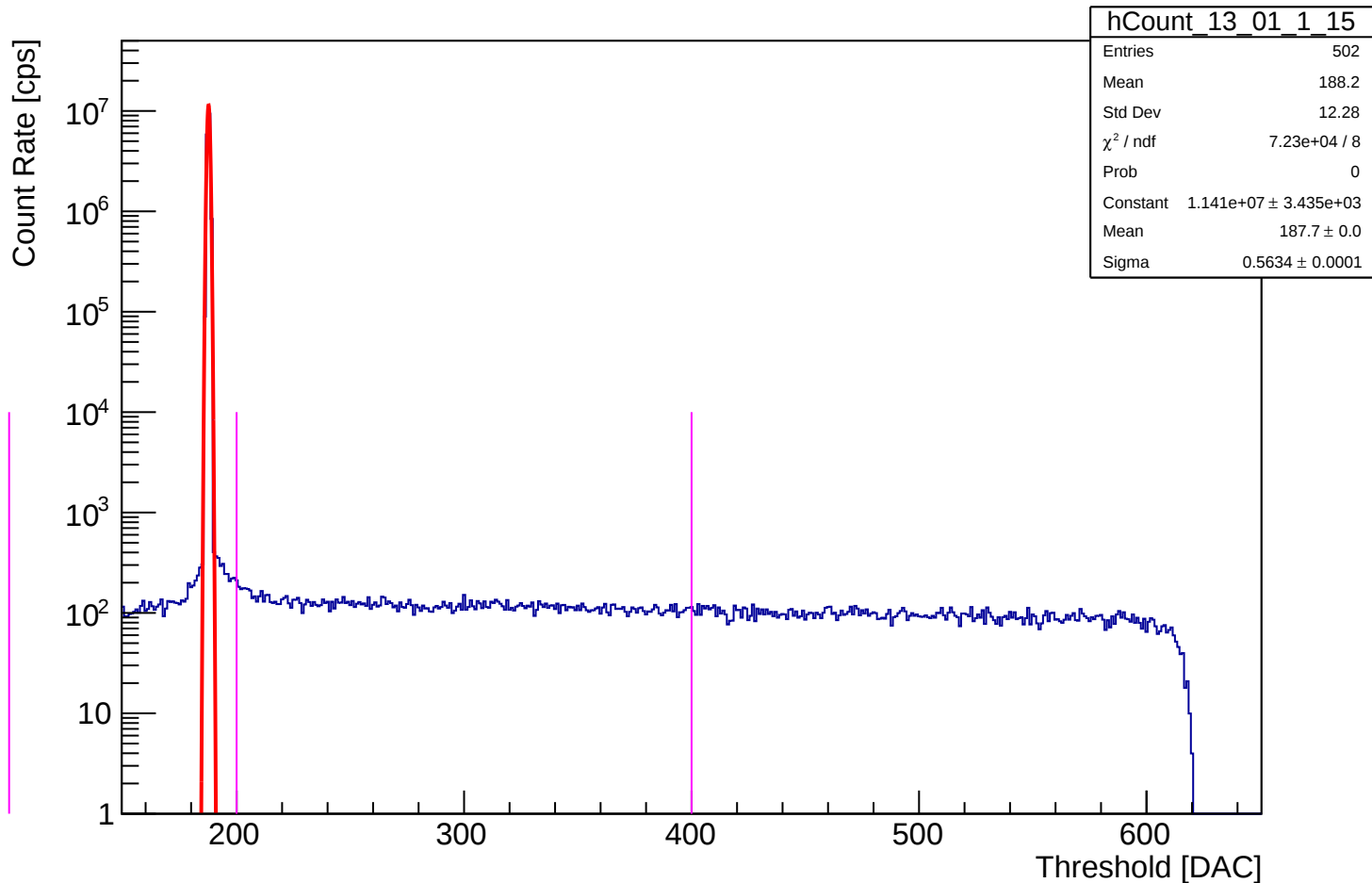
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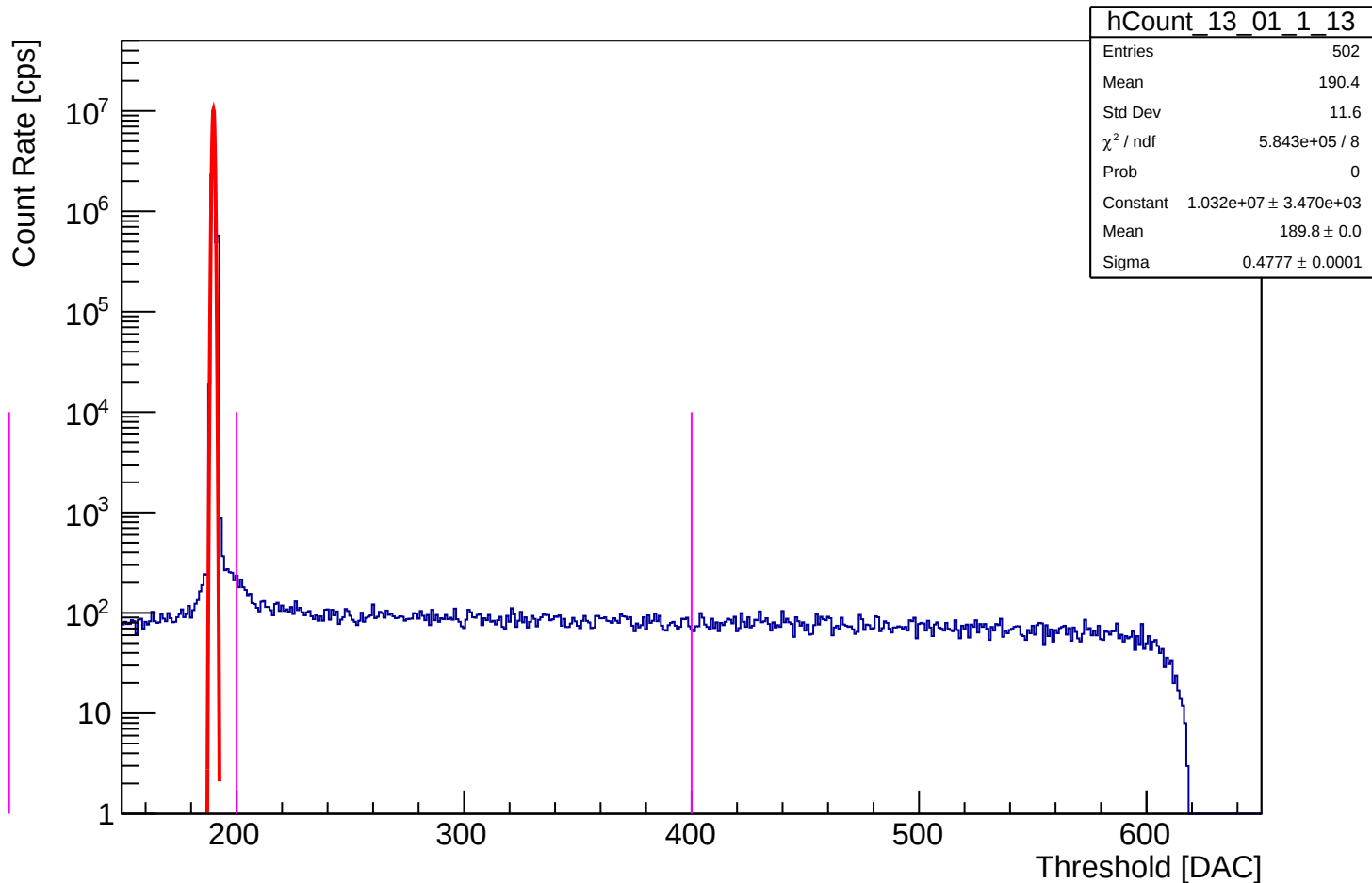
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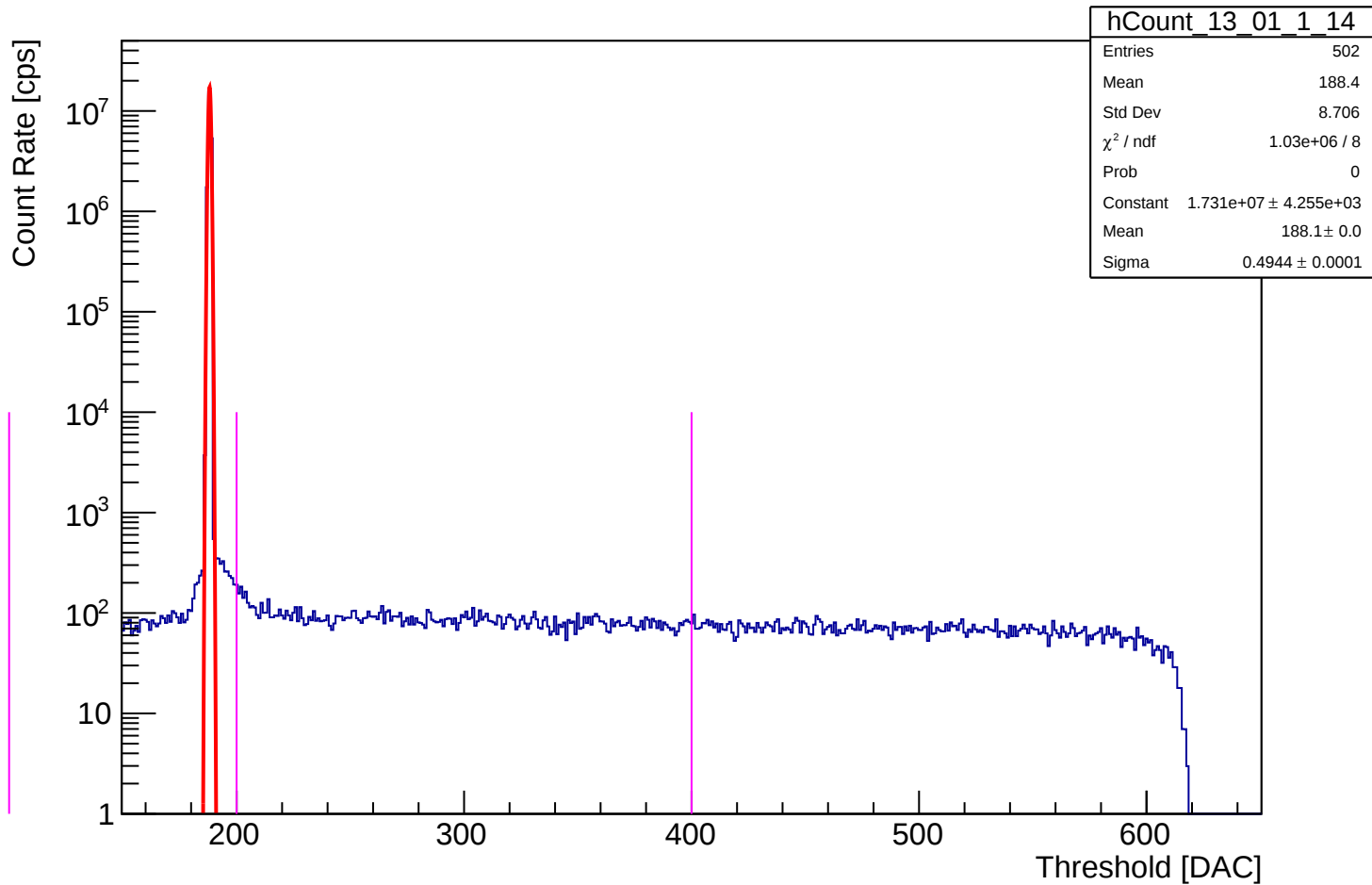
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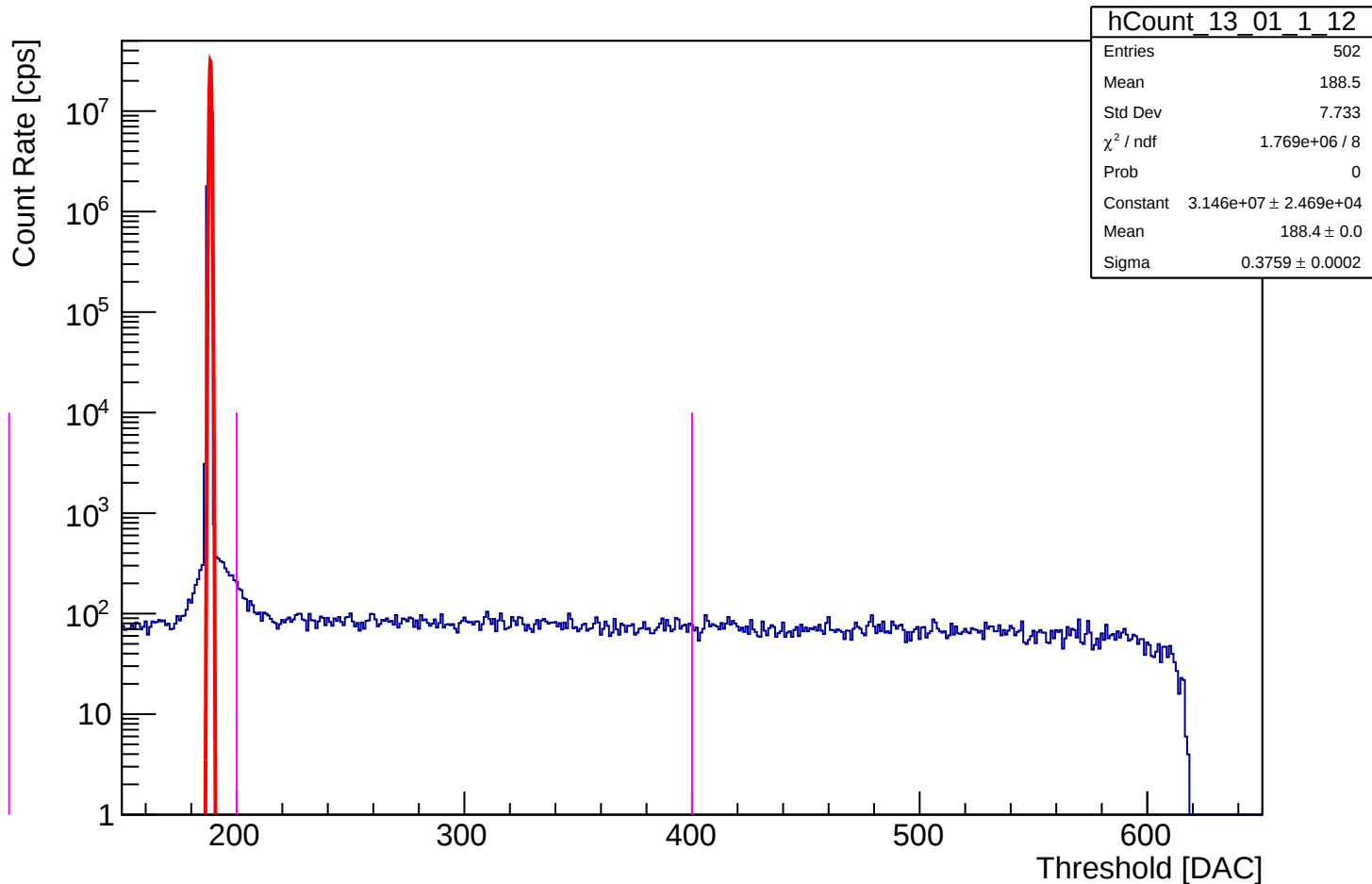
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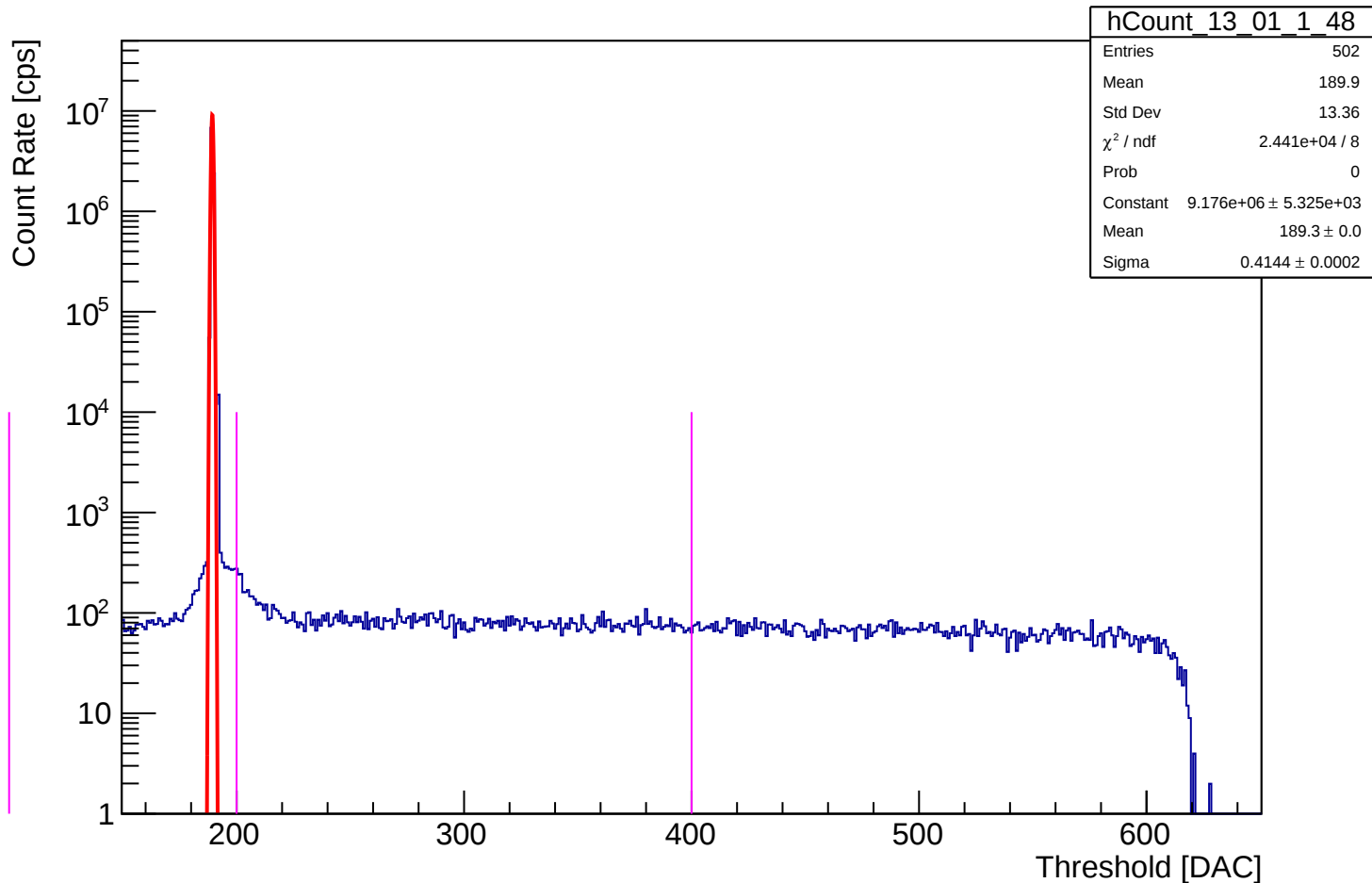
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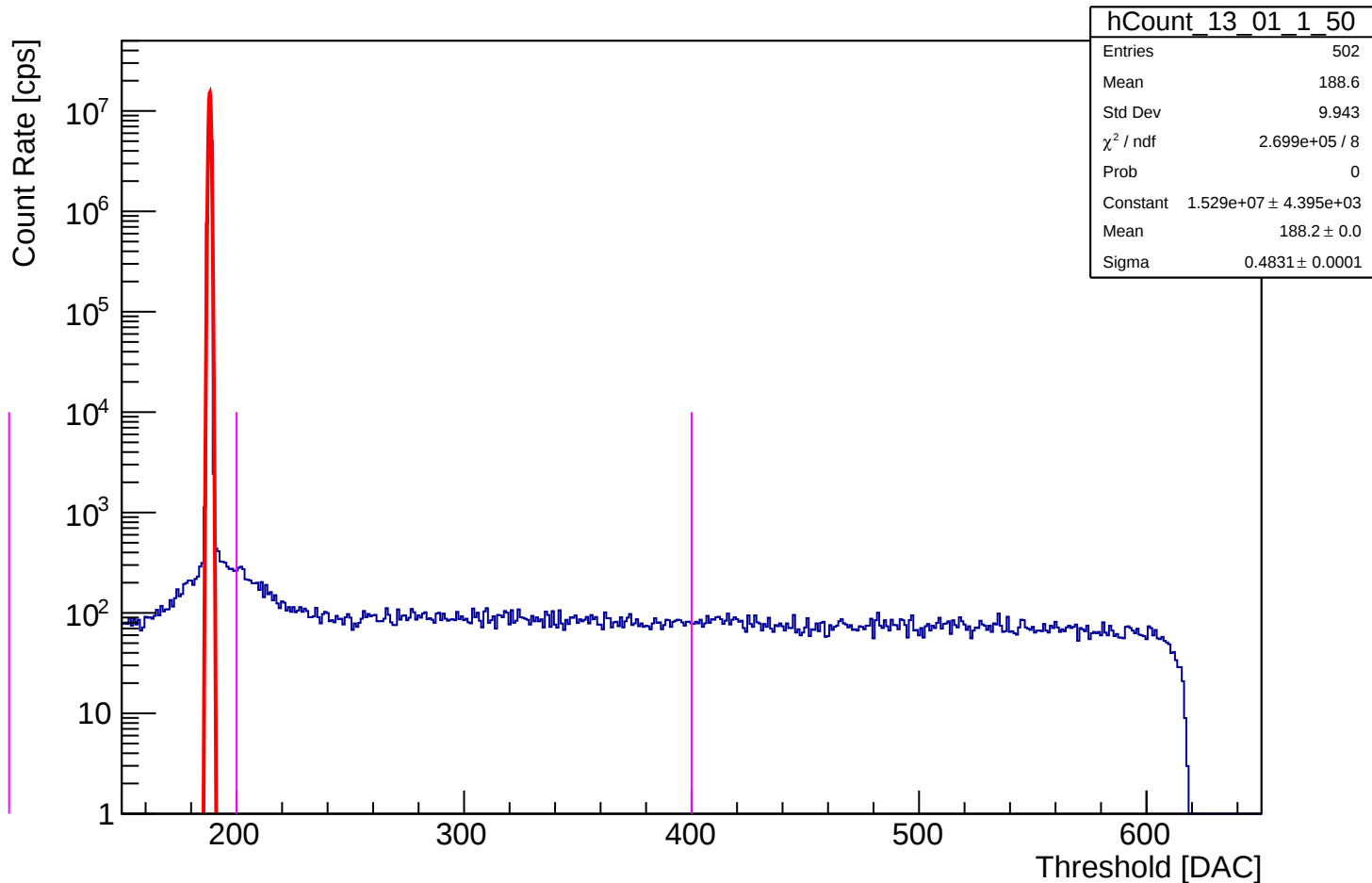
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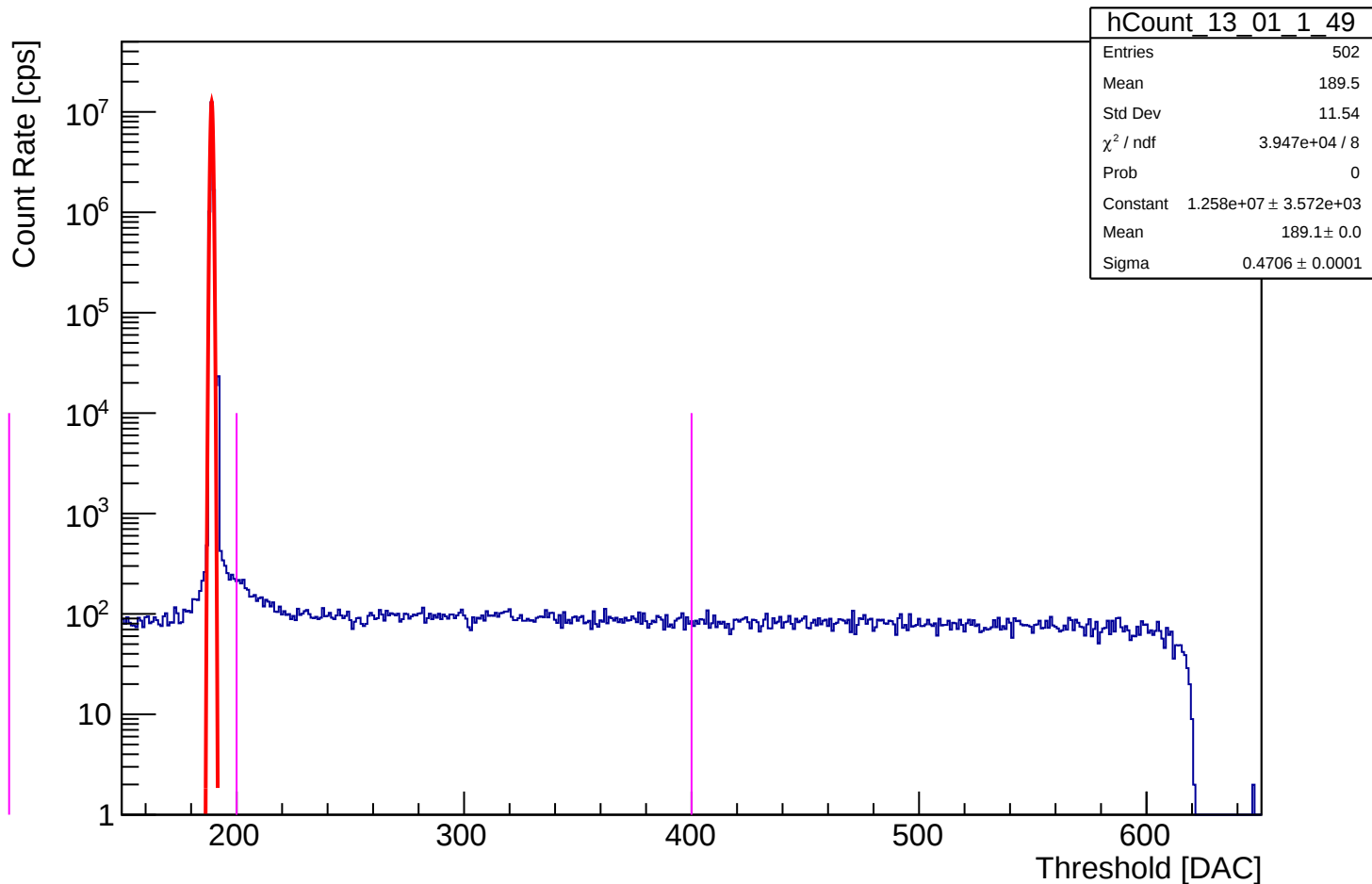
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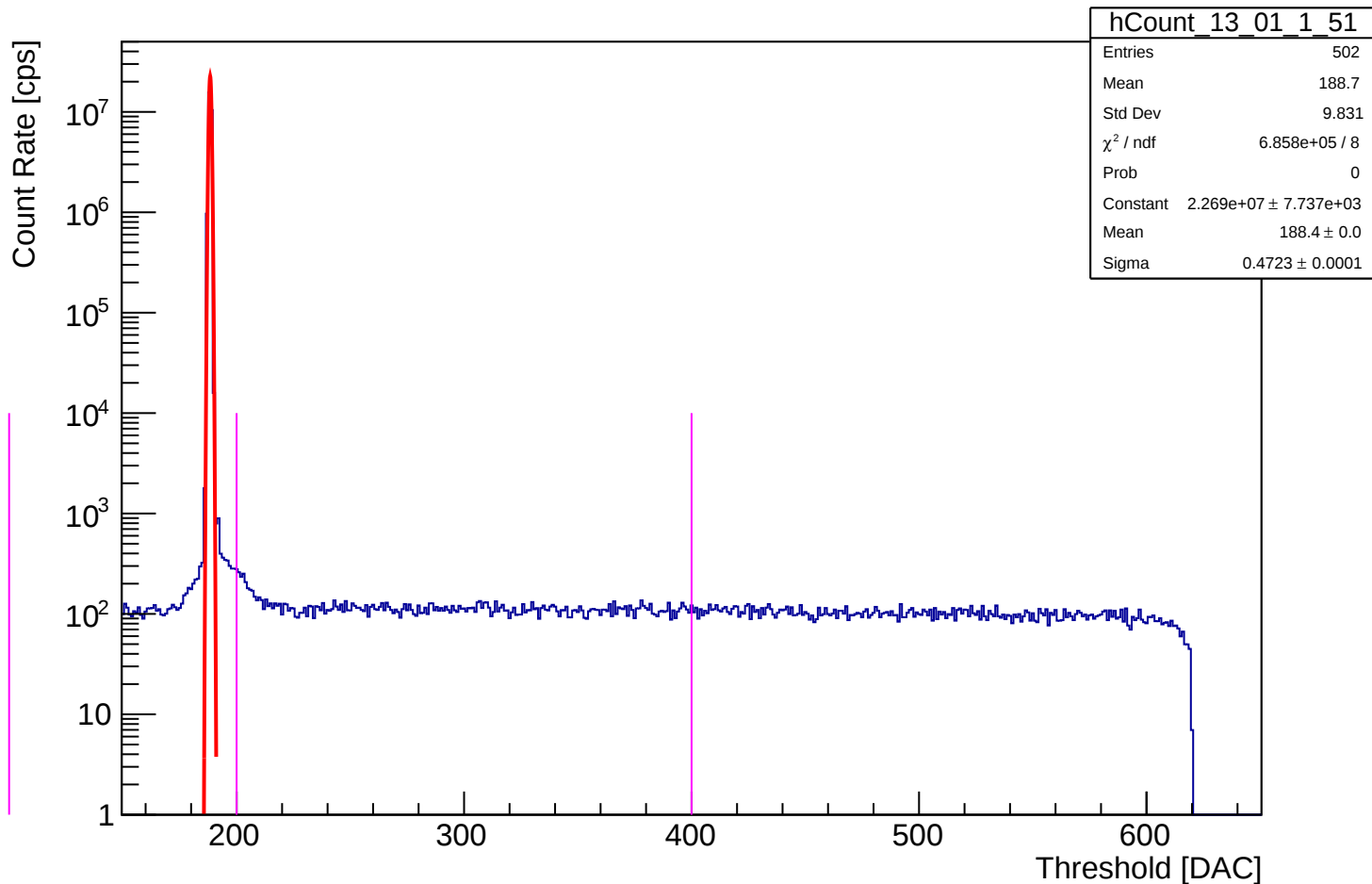
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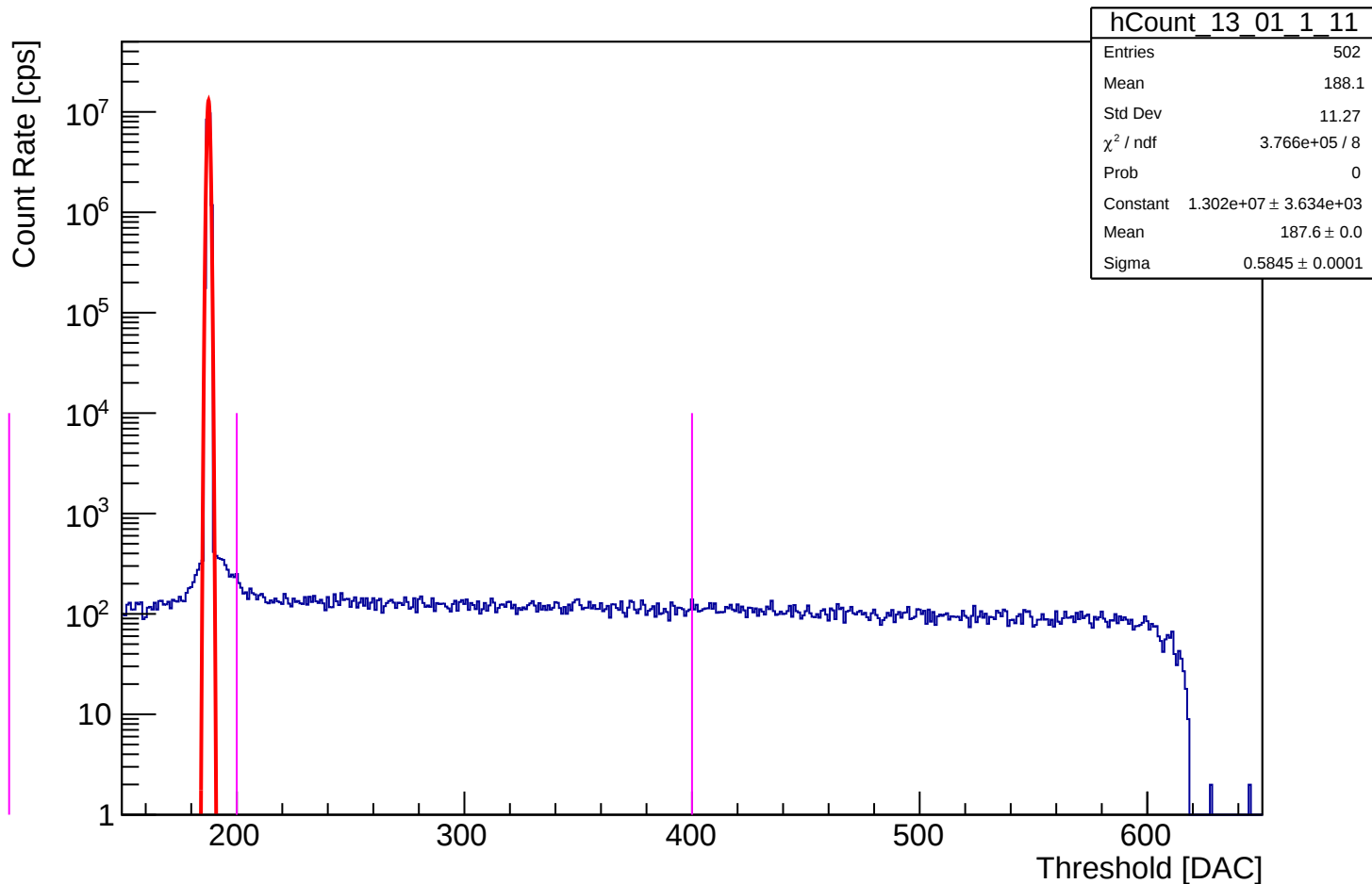
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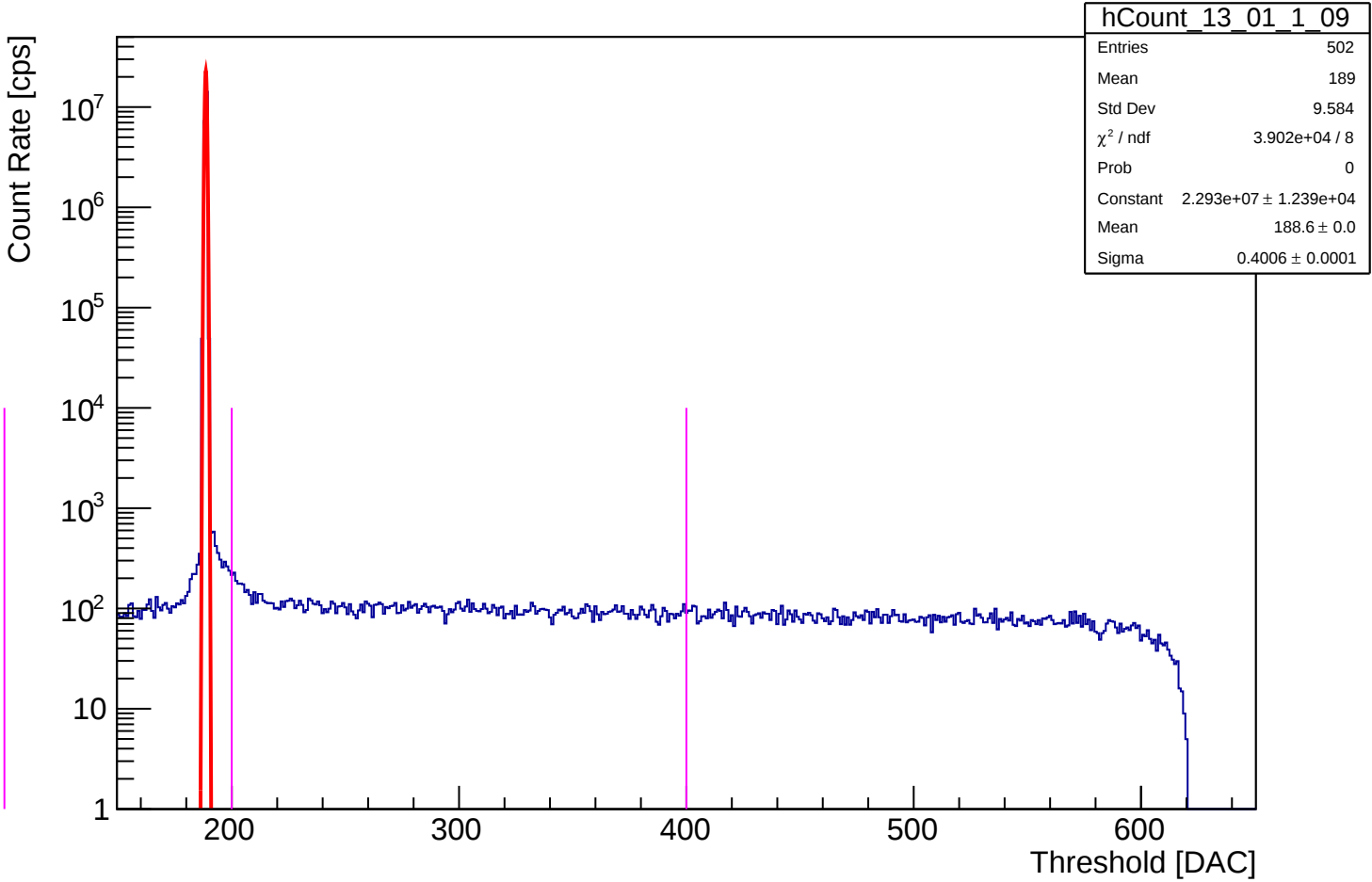


Row 1 Tile 1 Pmt 5 Pixel 40 Slot 13 Fiber 1 Asic 1 Channel 51

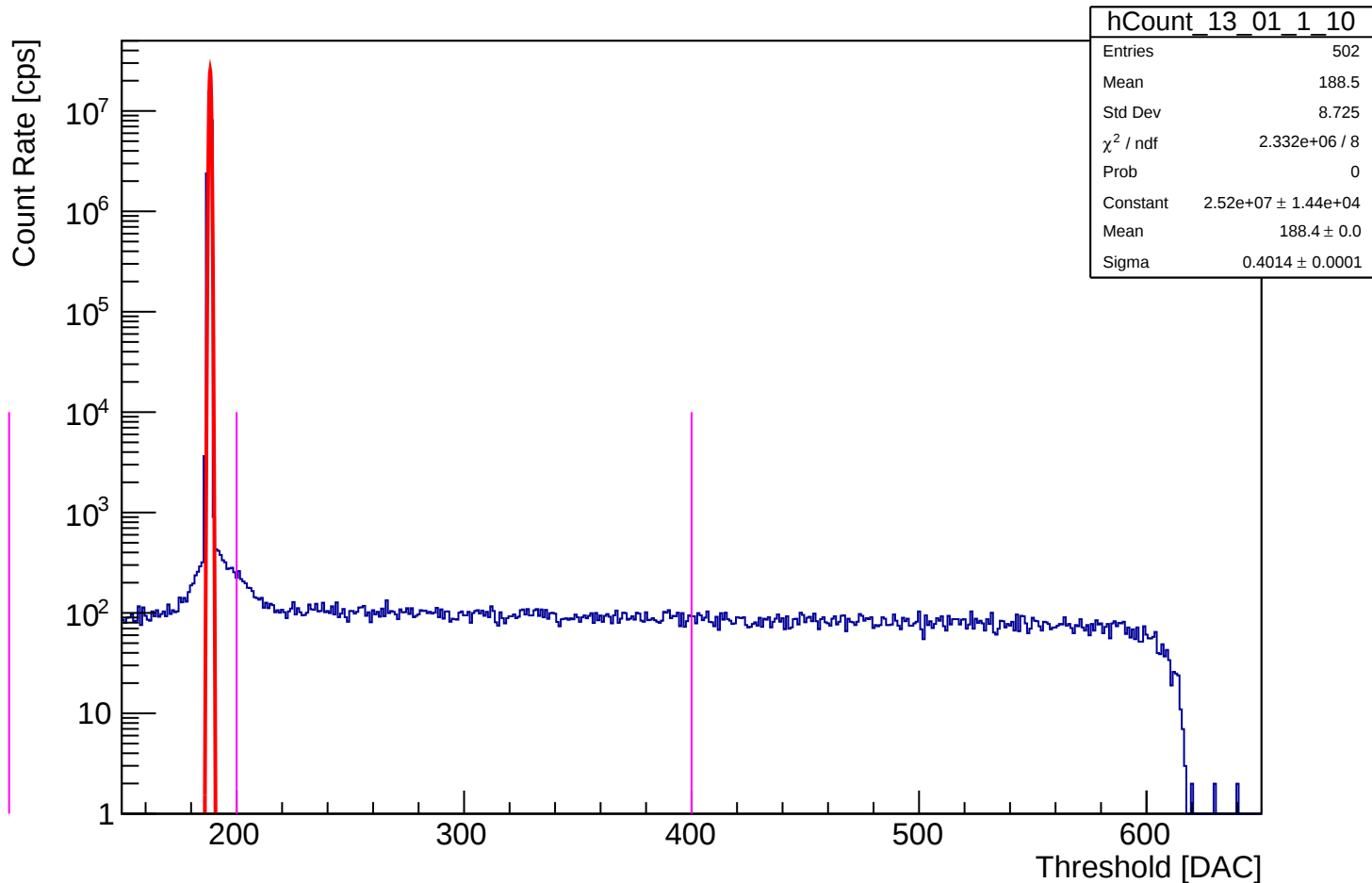


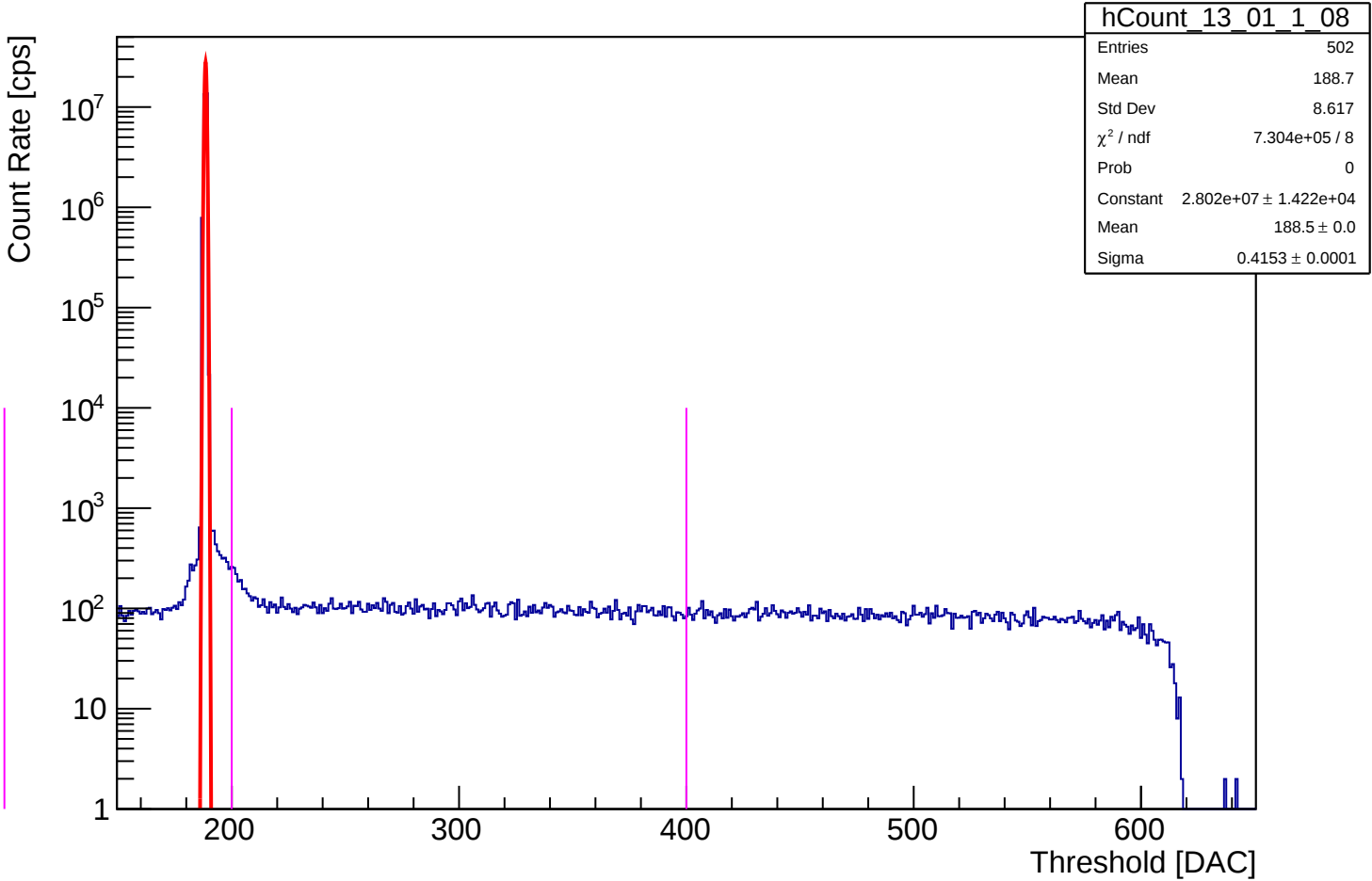
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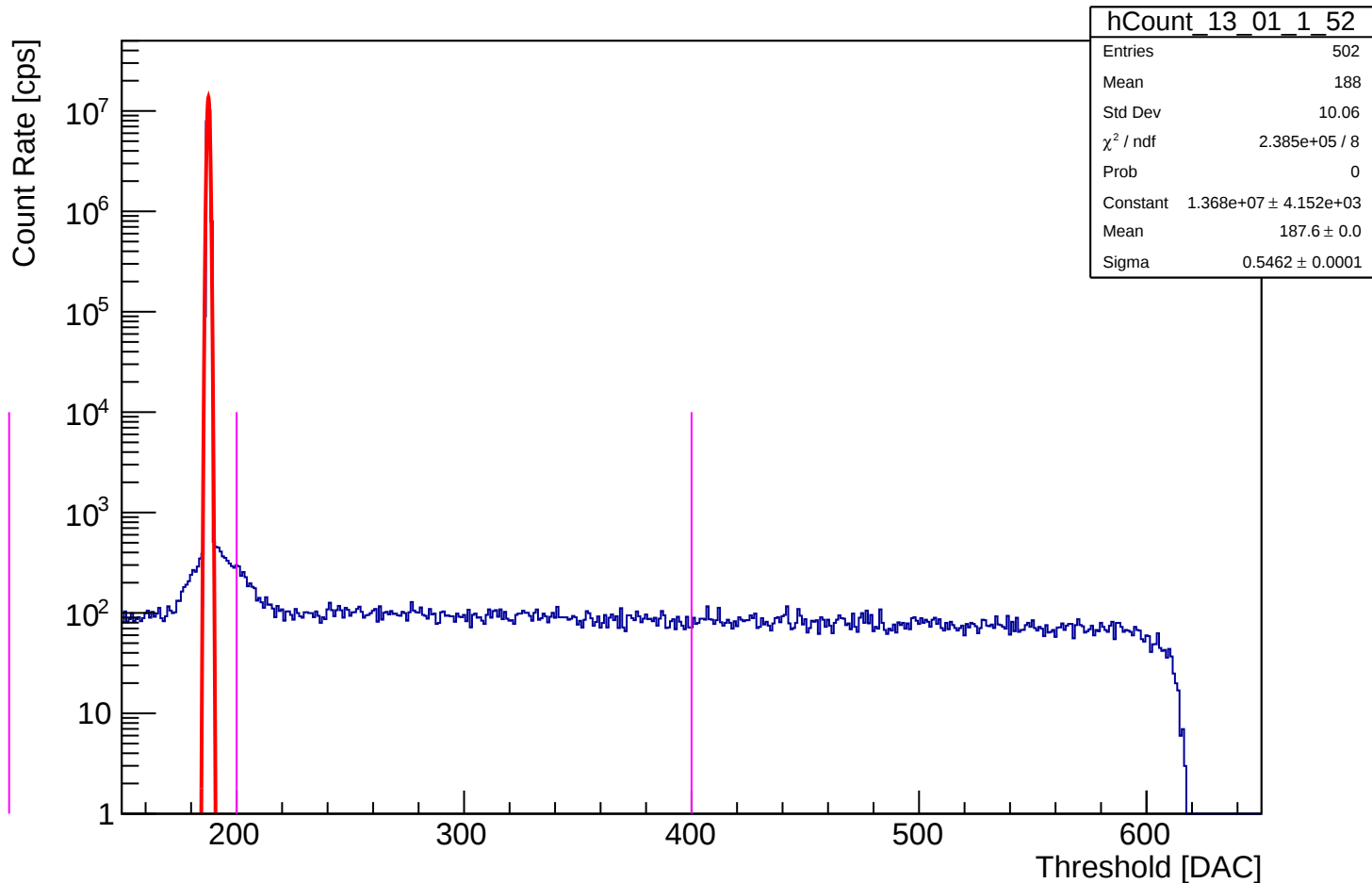


Row 1 Tile 1 Pmt 5 Pixel 43 Slot 13 Fiber 1 Asic 1 Channel 10

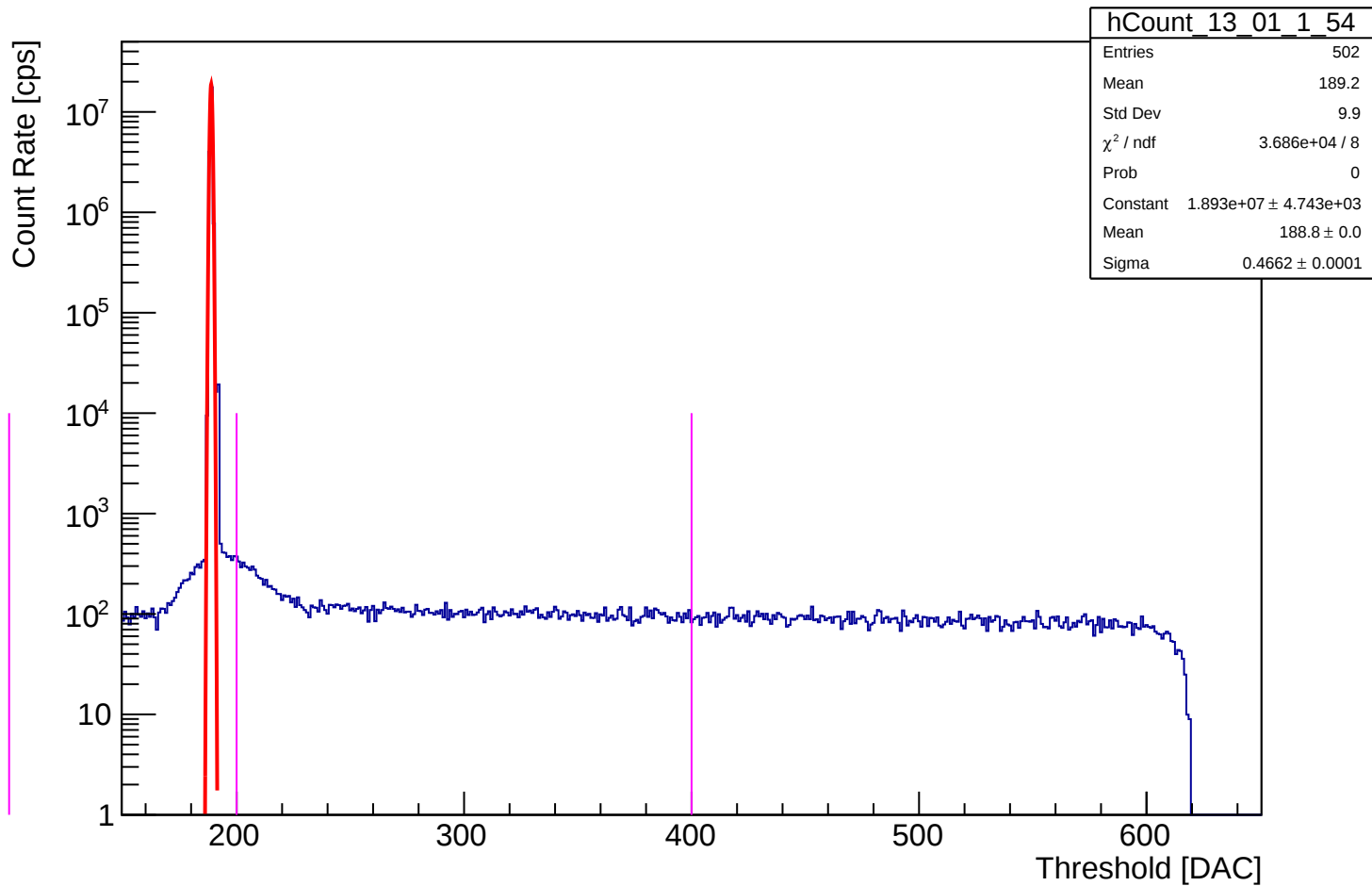




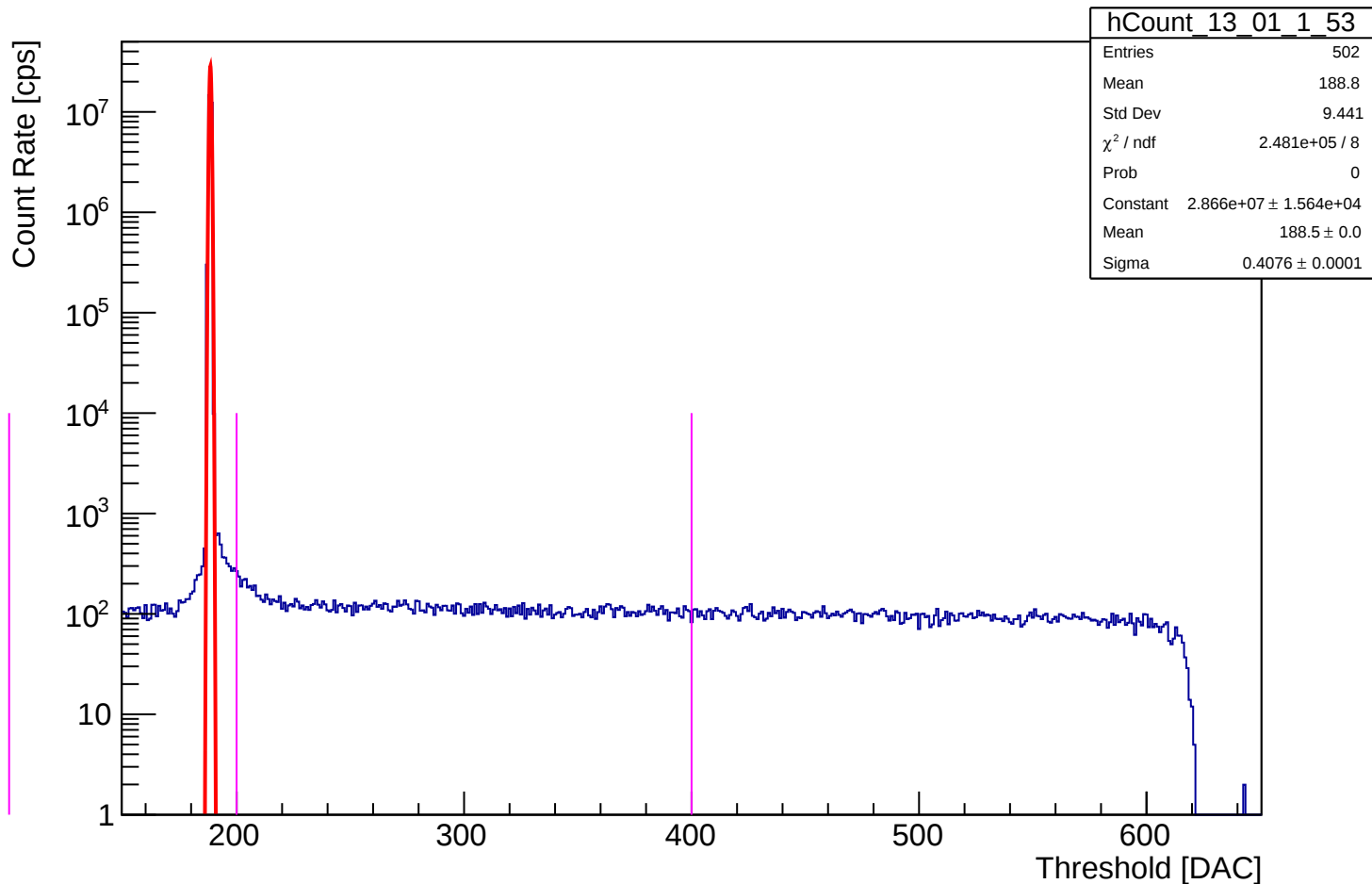
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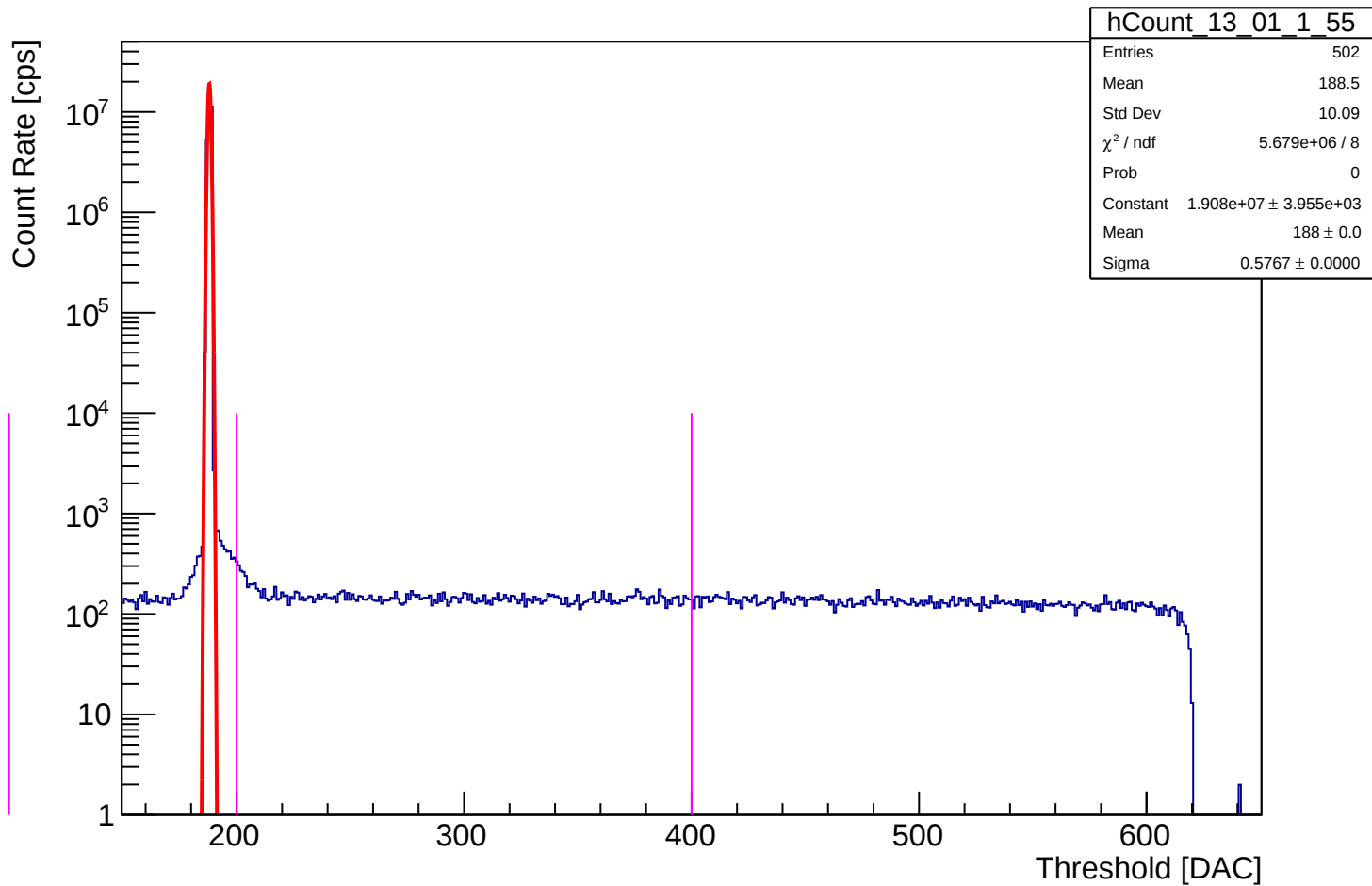
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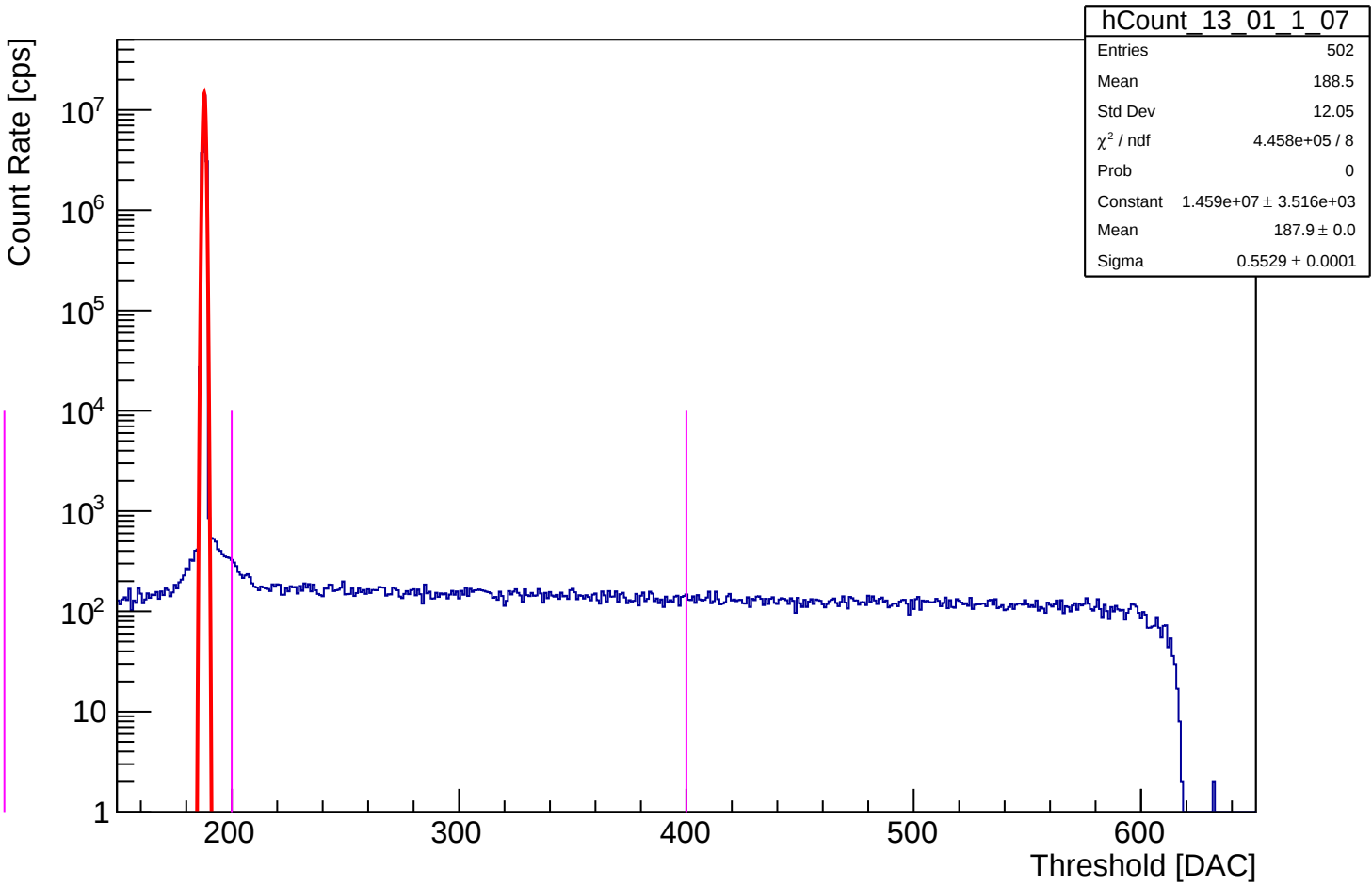


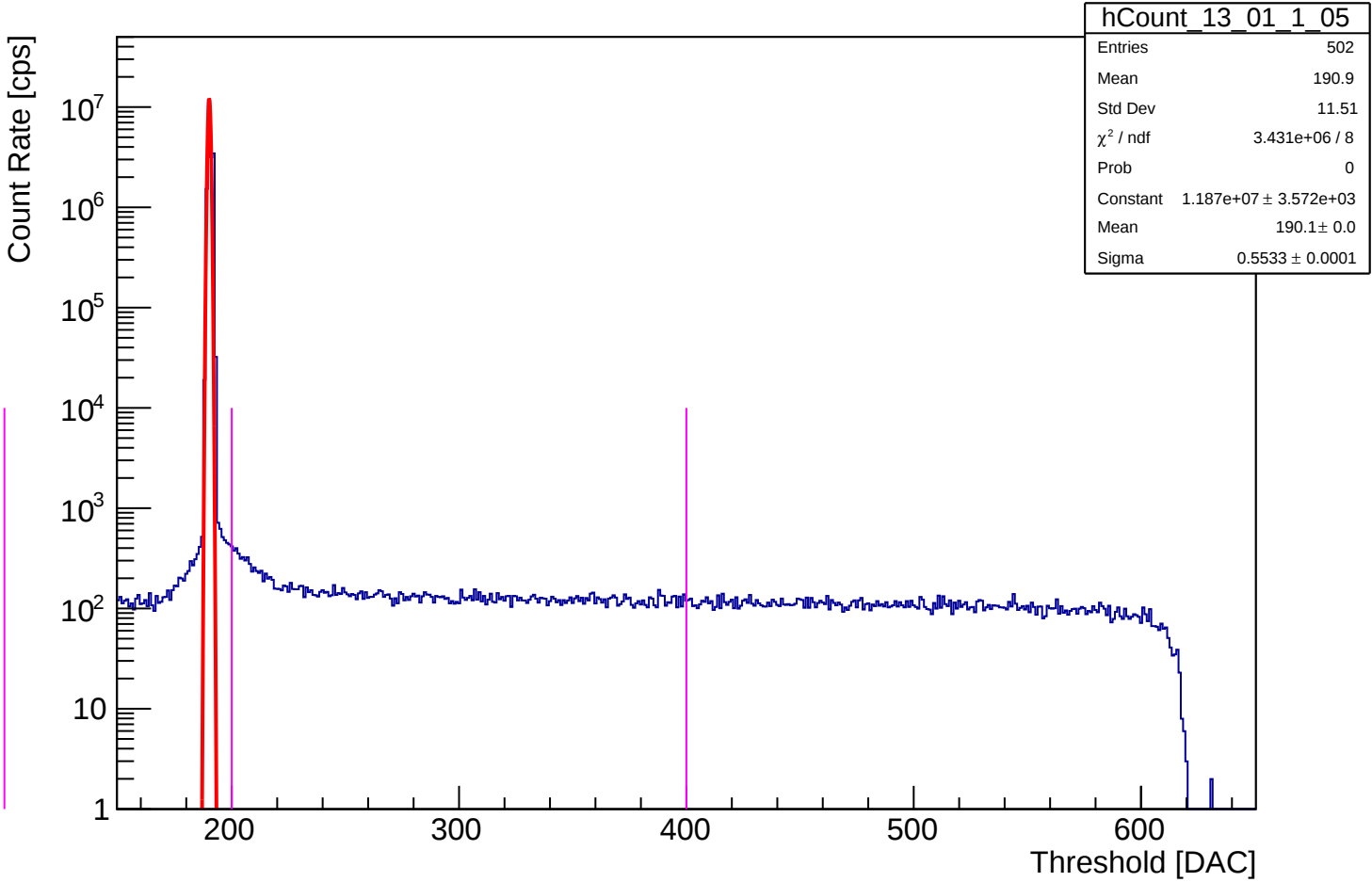
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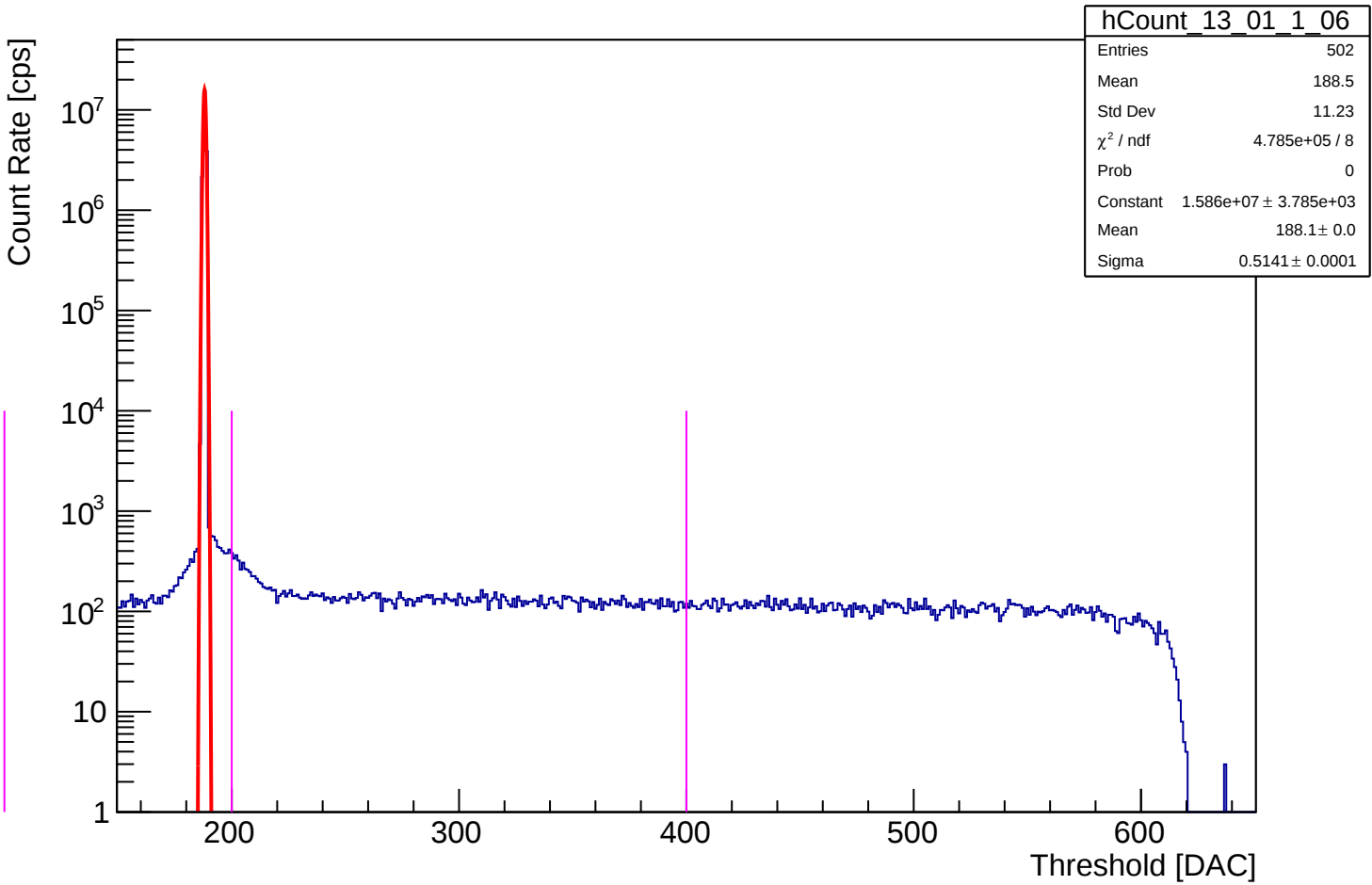


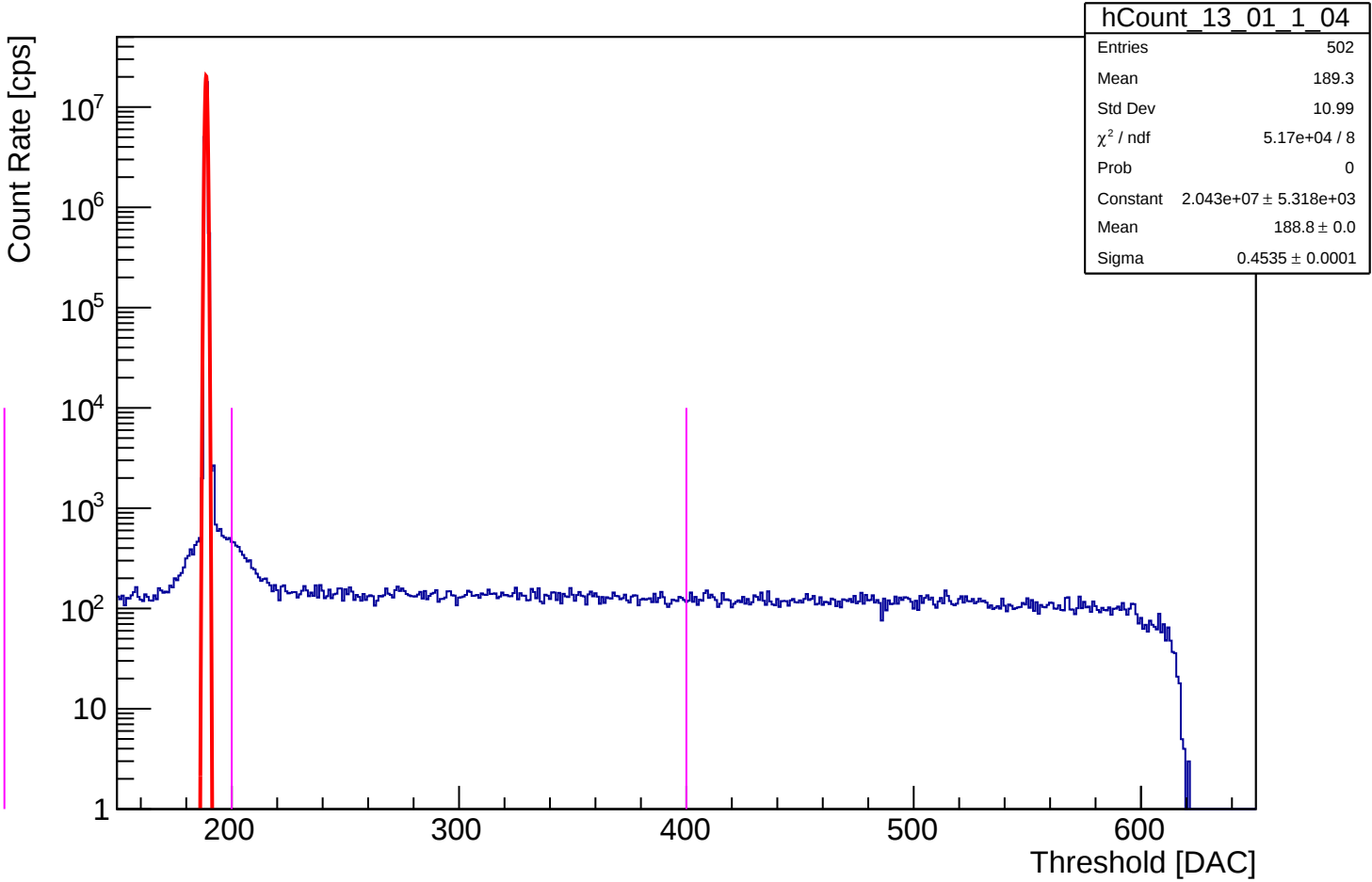
Row 1 Tile 1 Pmt 5 Pixel 48 Slot 13 Fiber 1 Asic 1 Channel 55



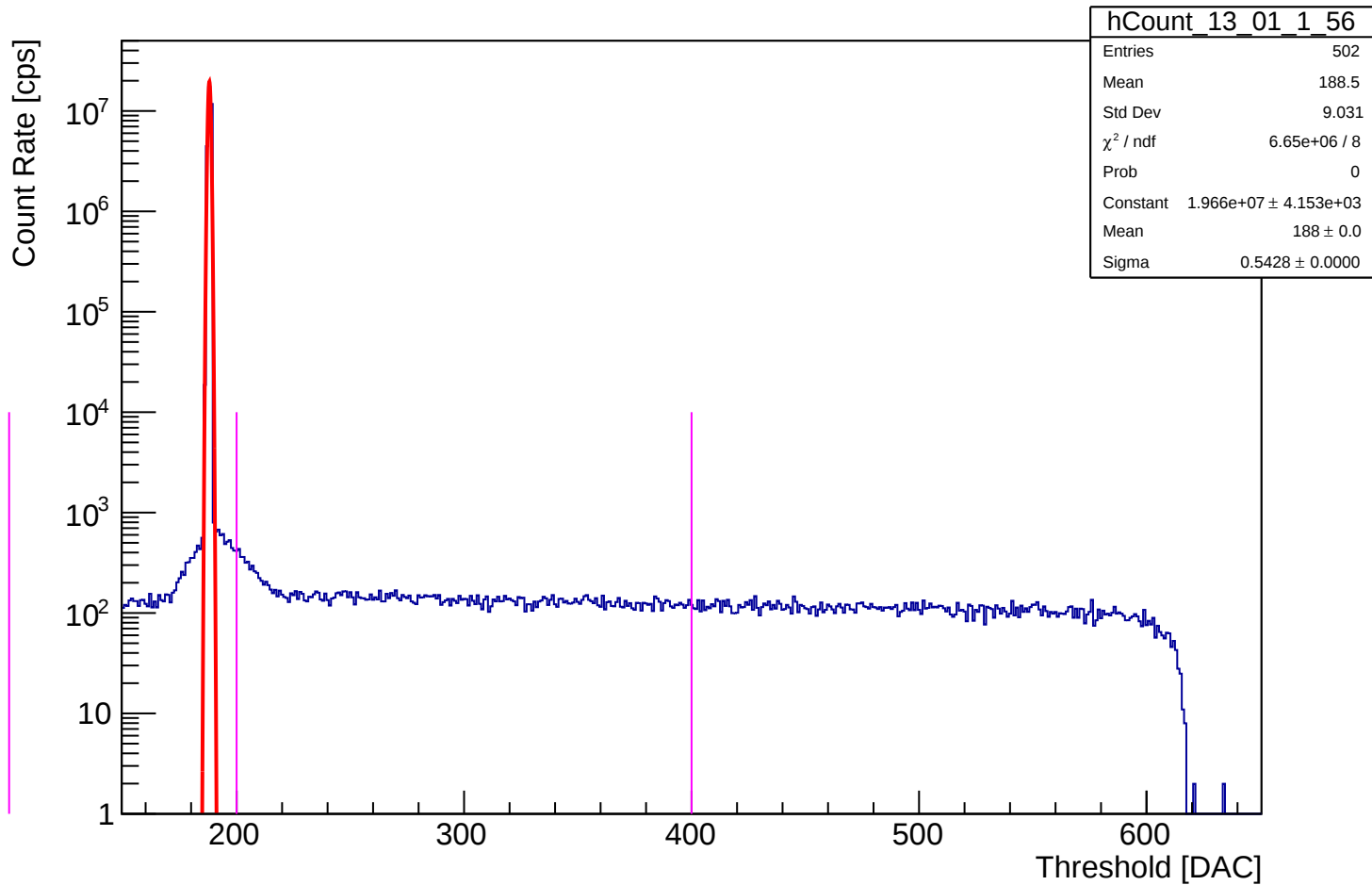




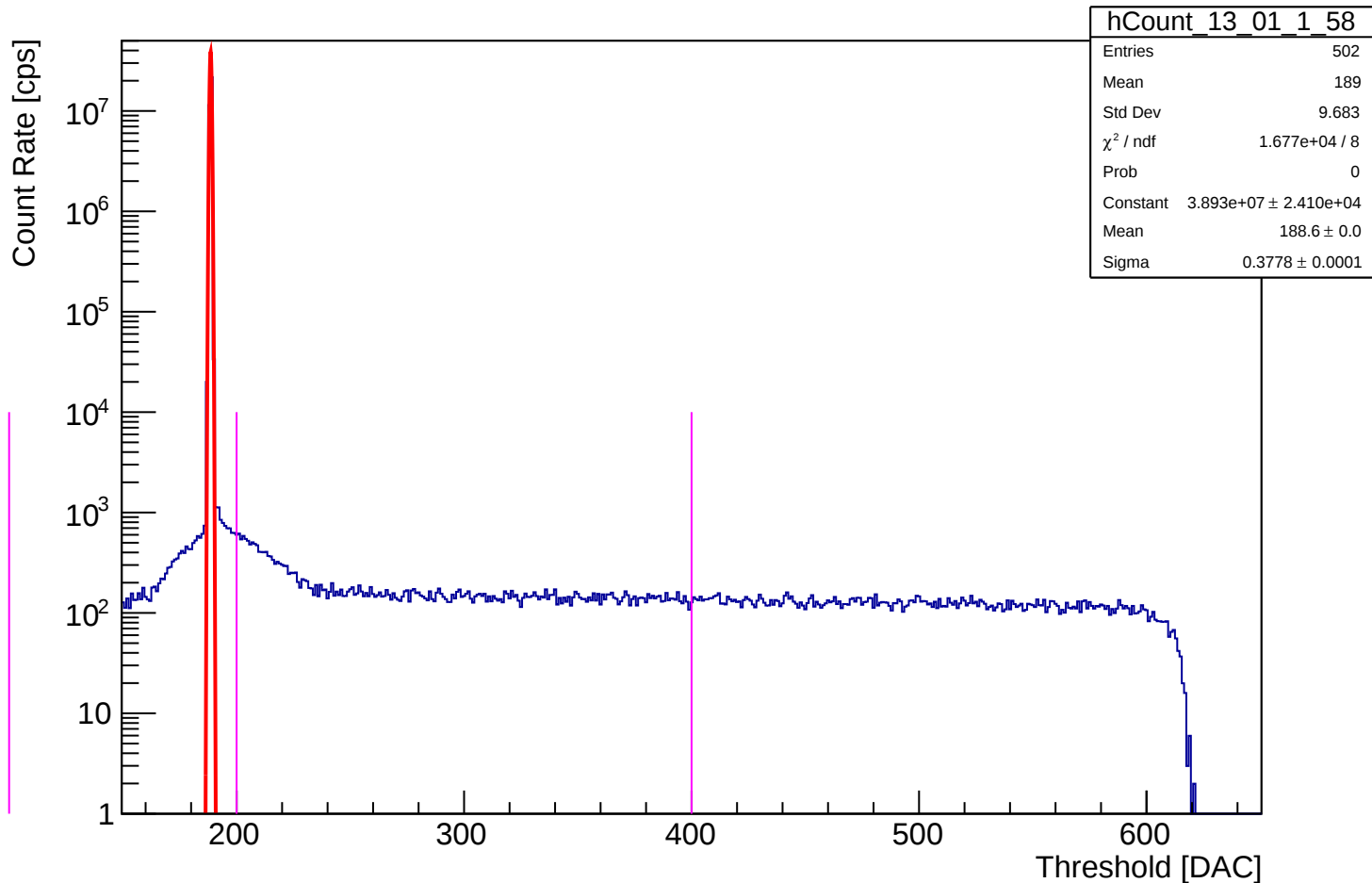




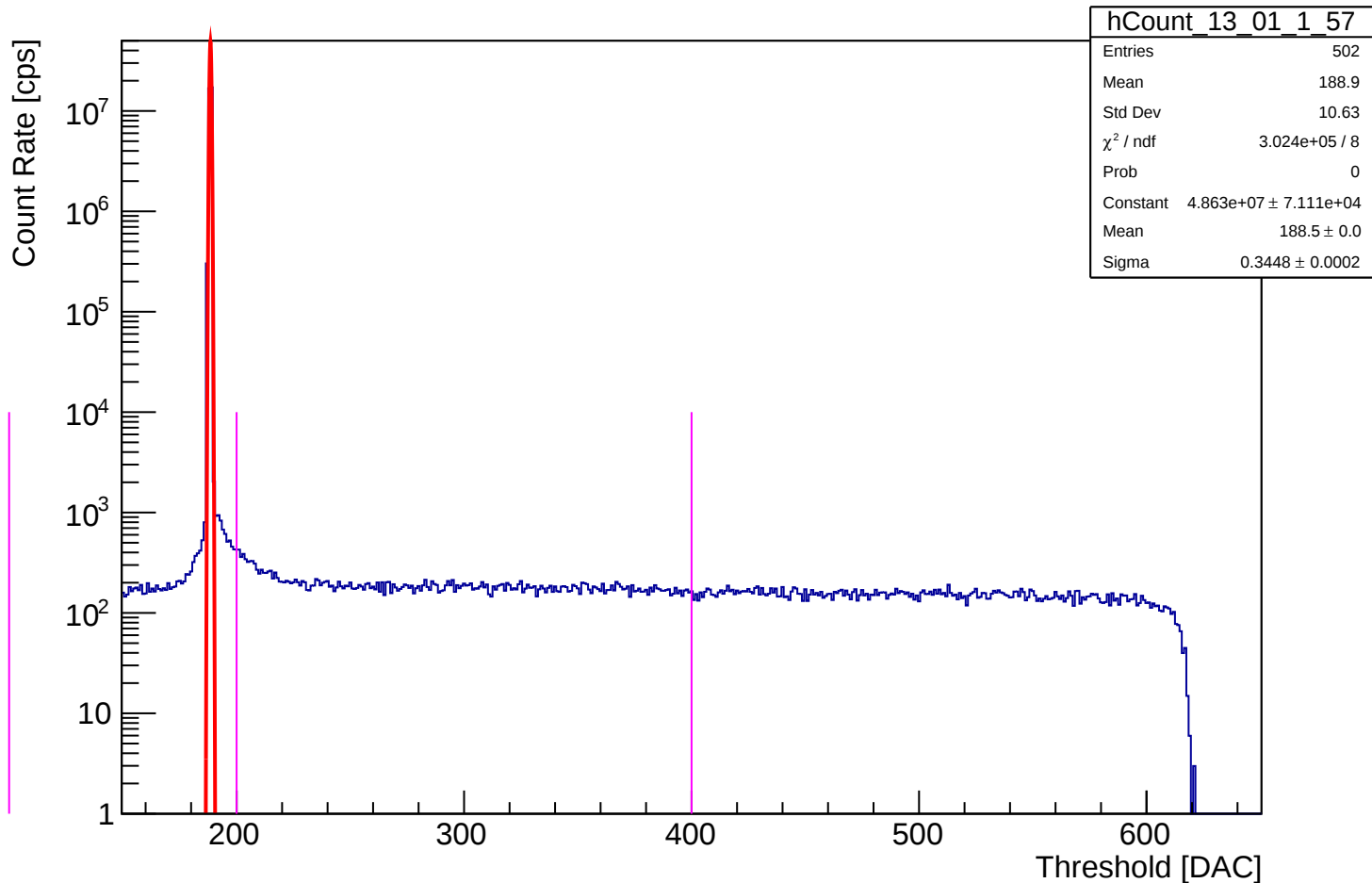
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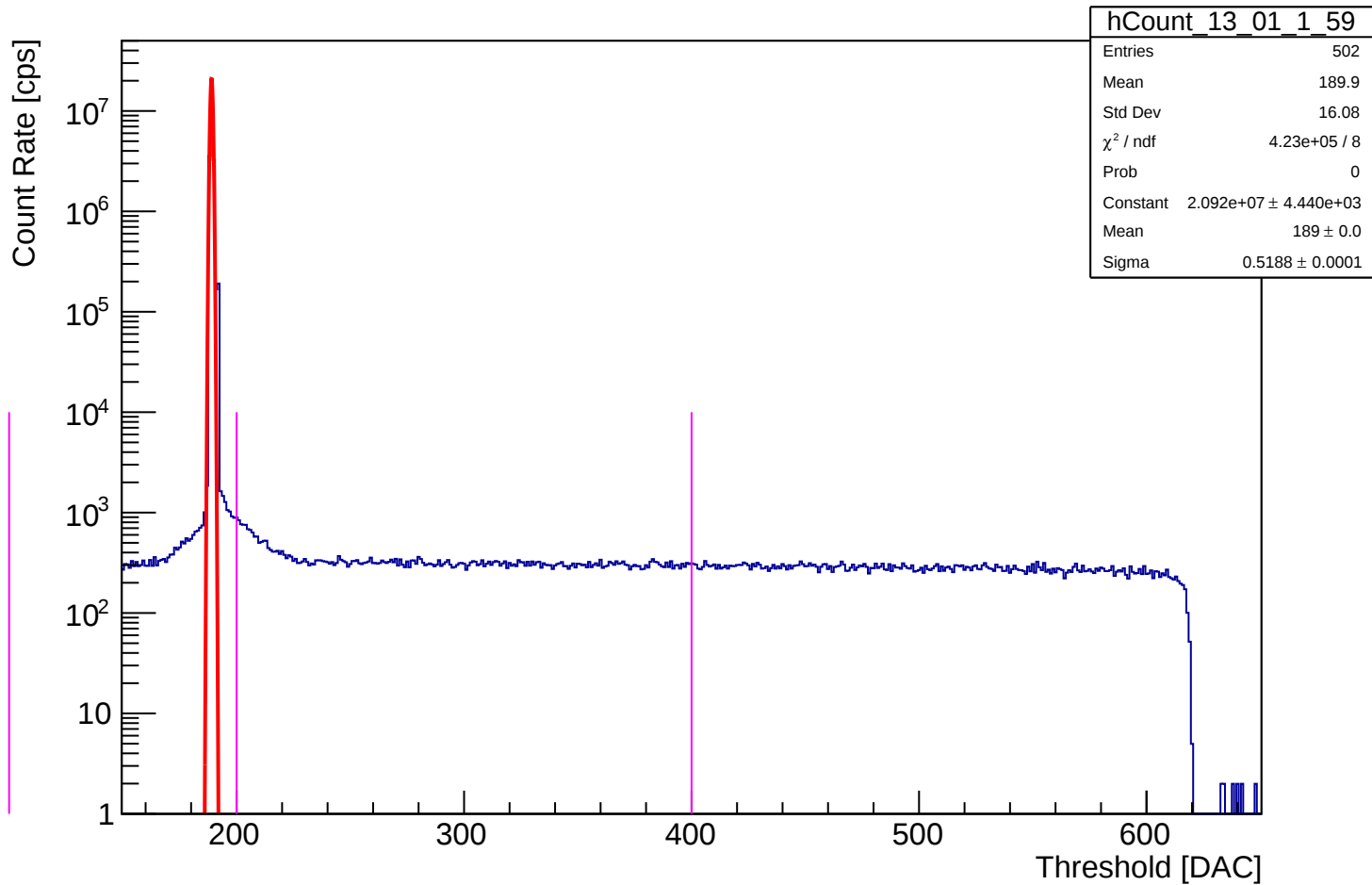
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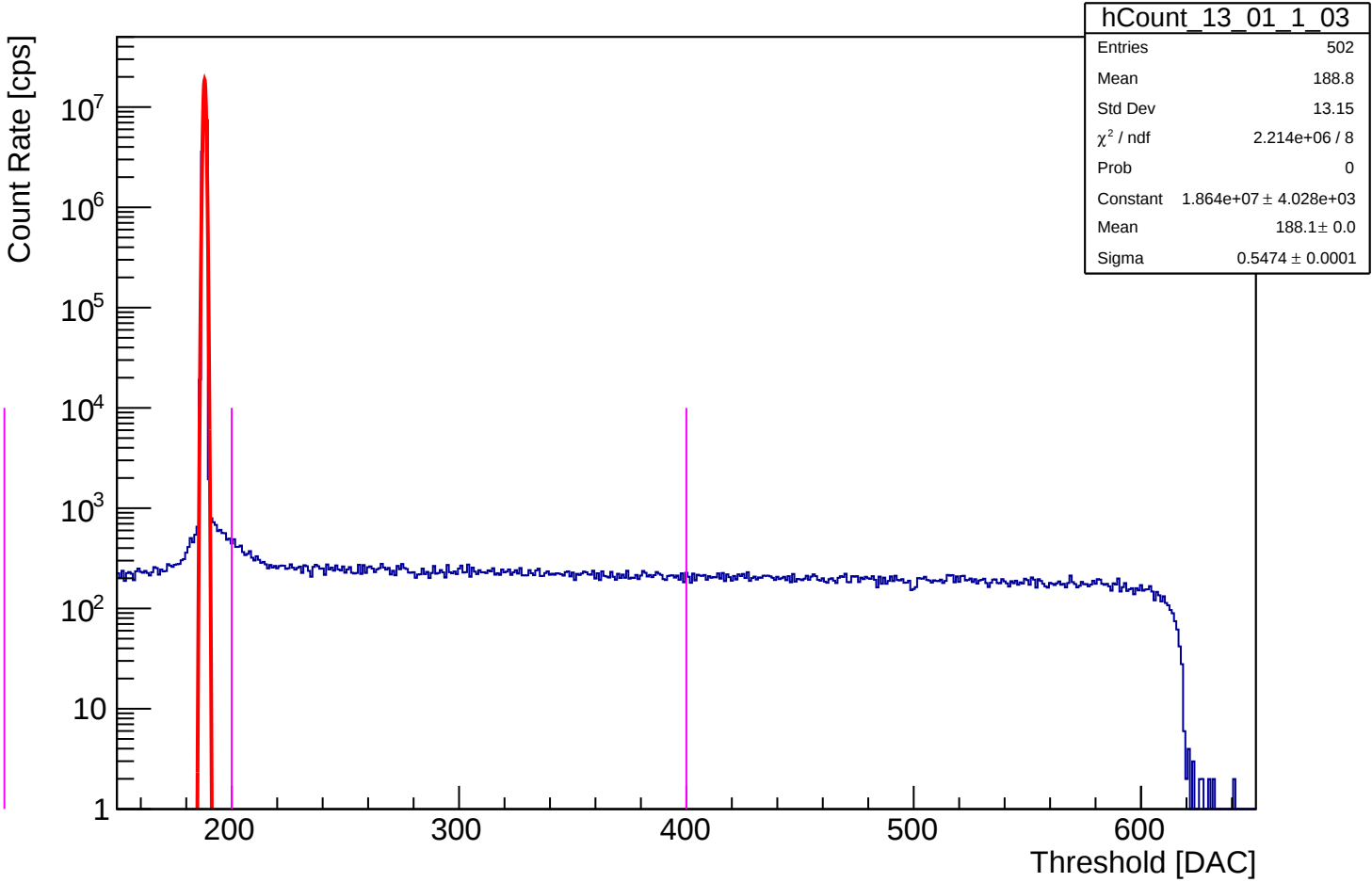


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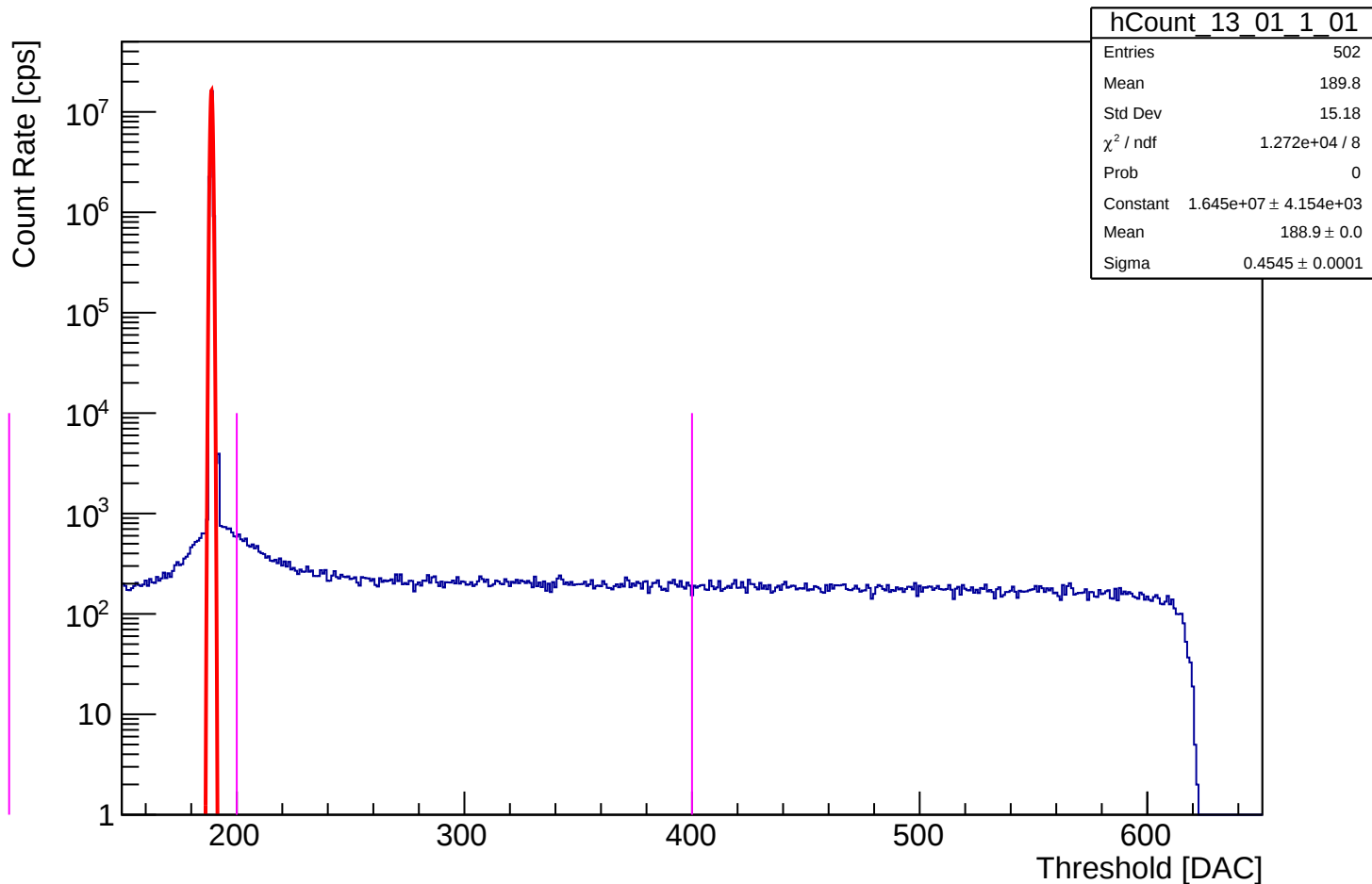


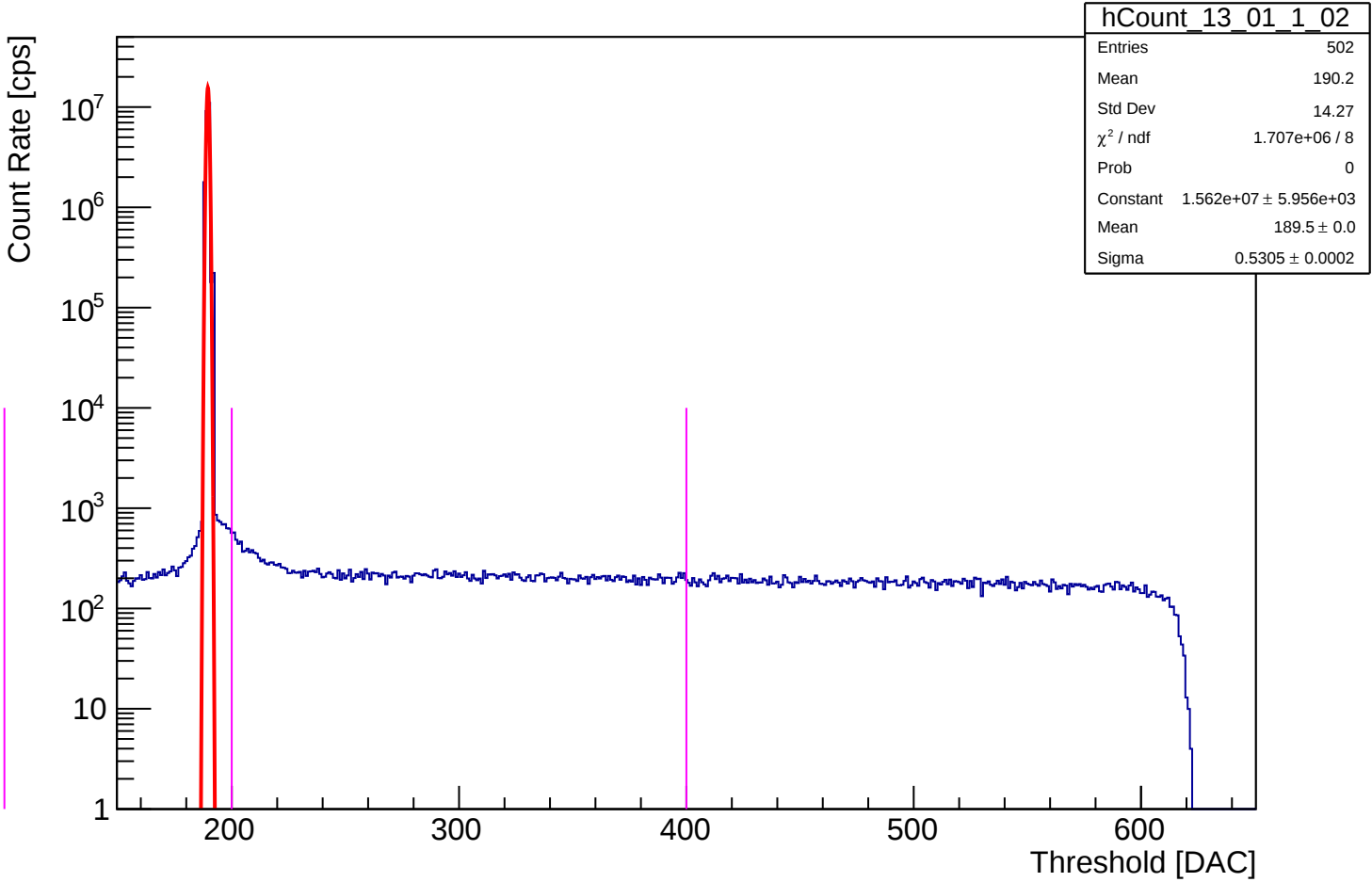
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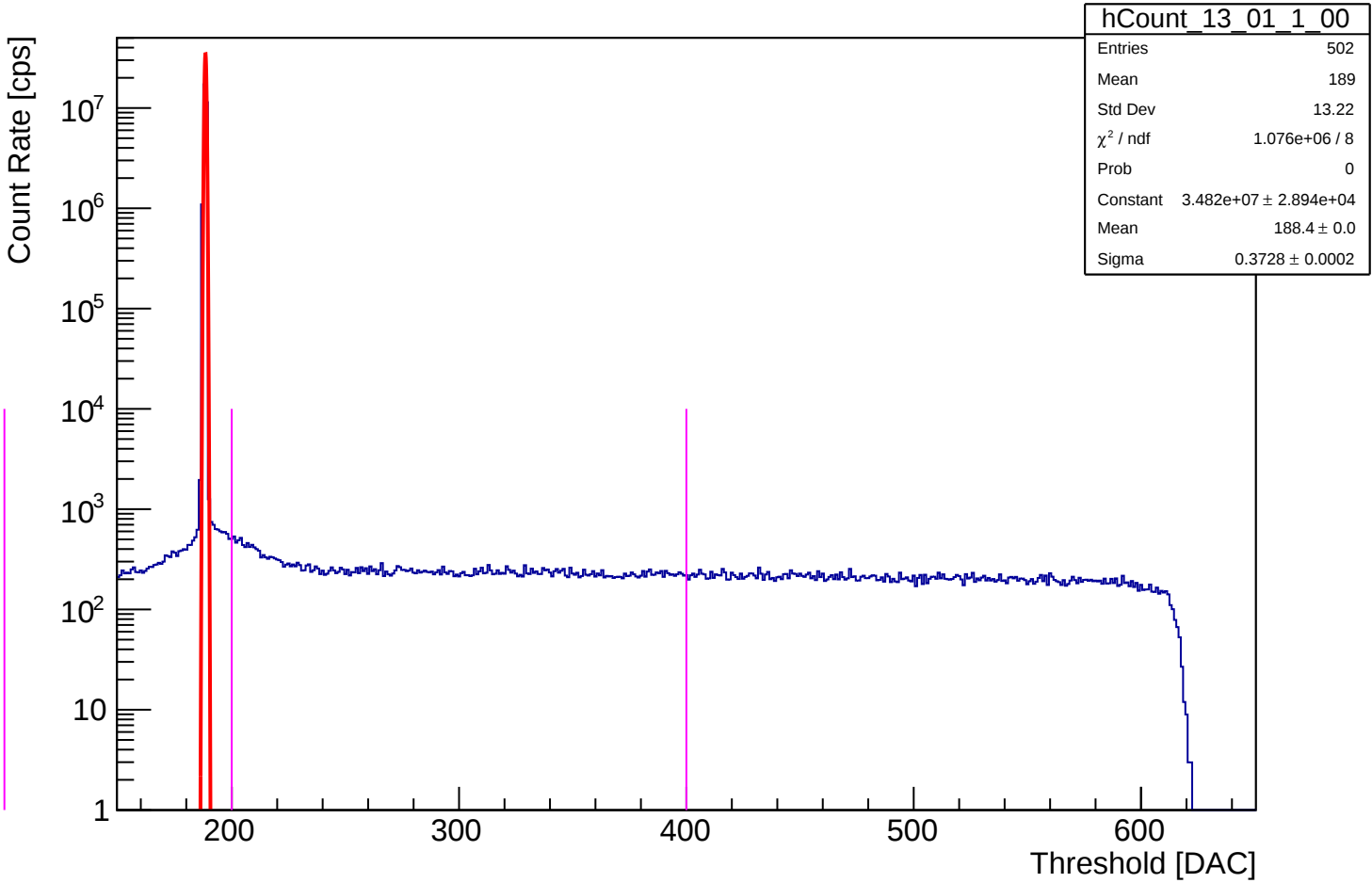




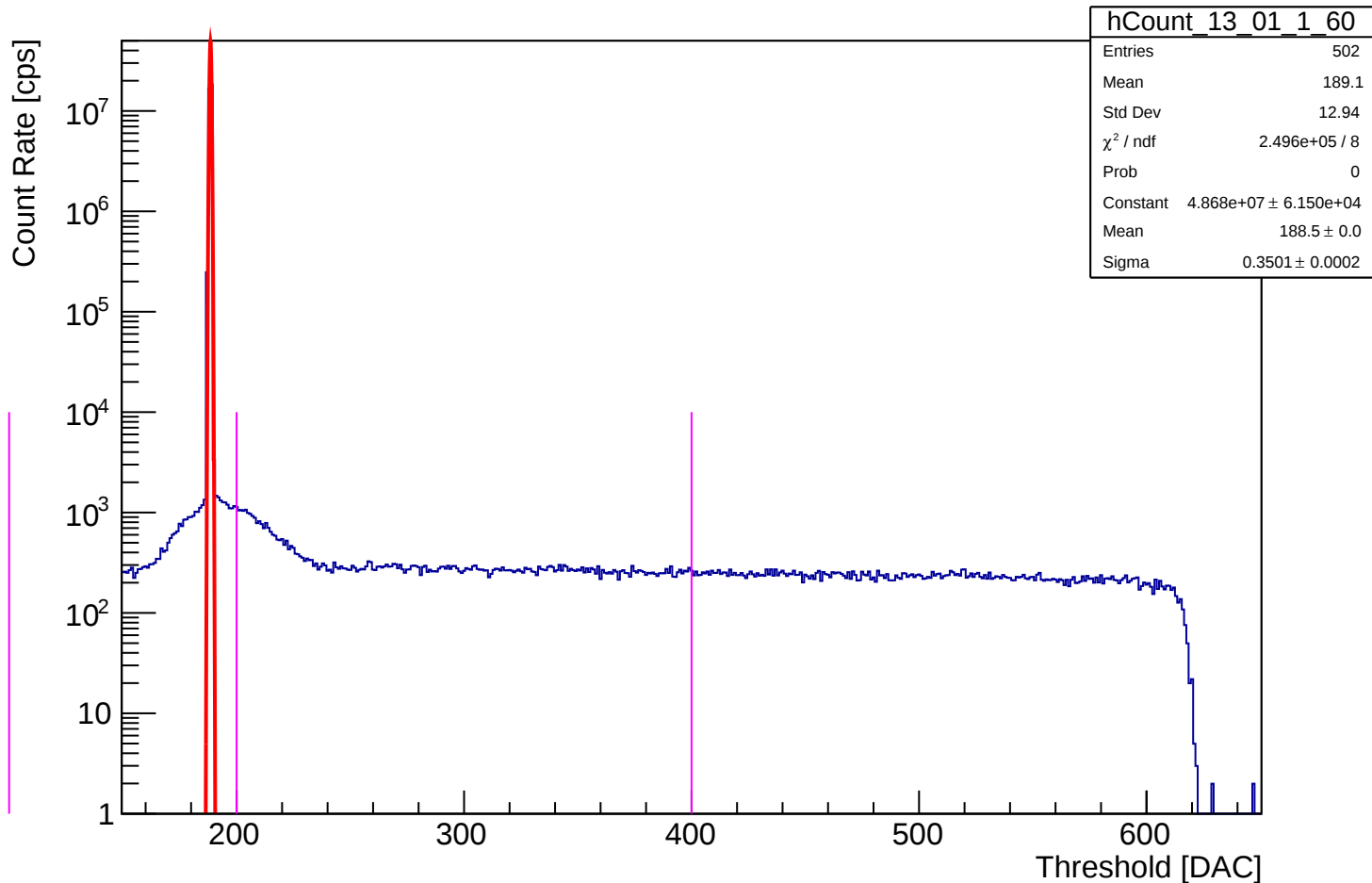
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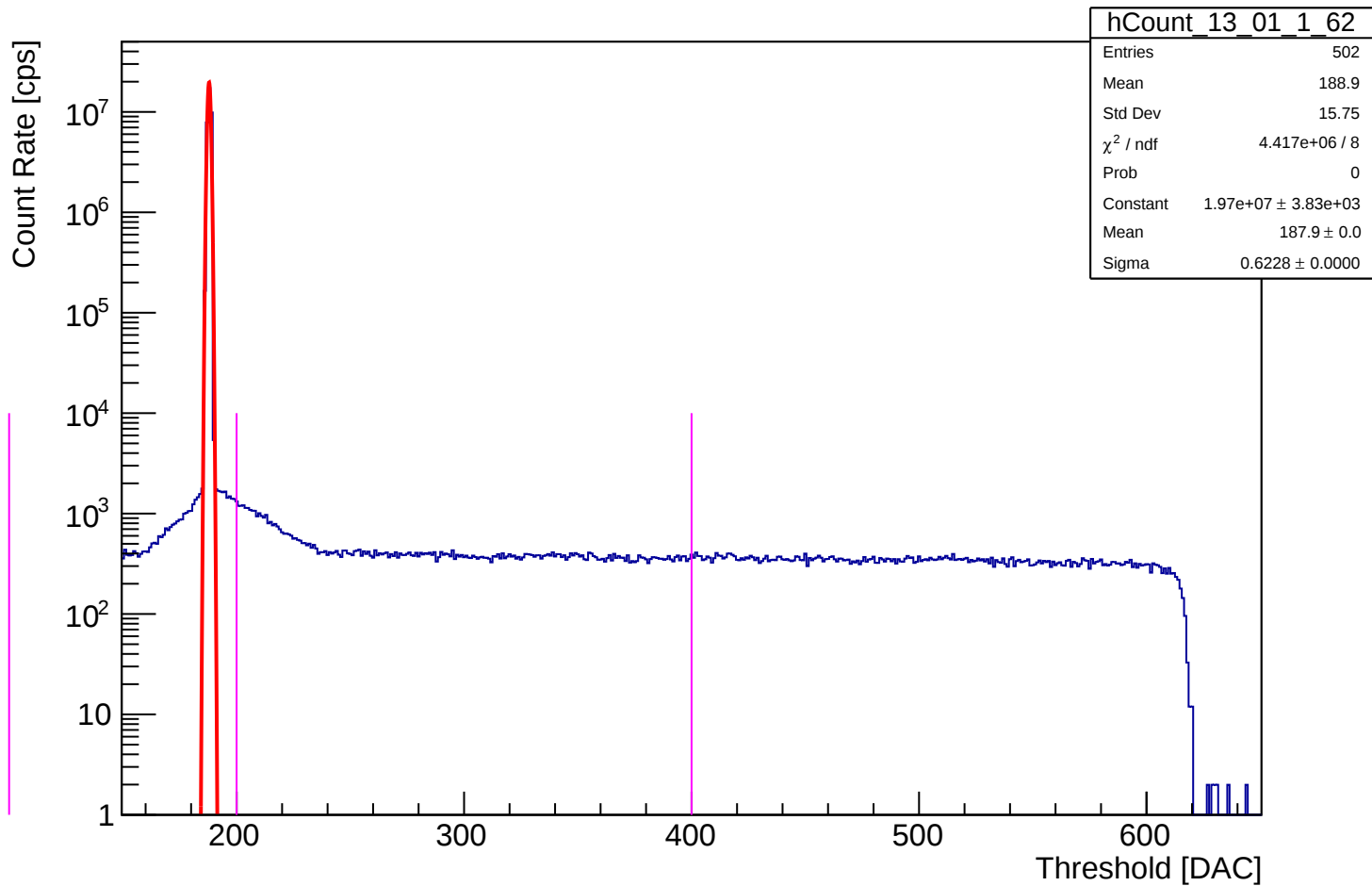




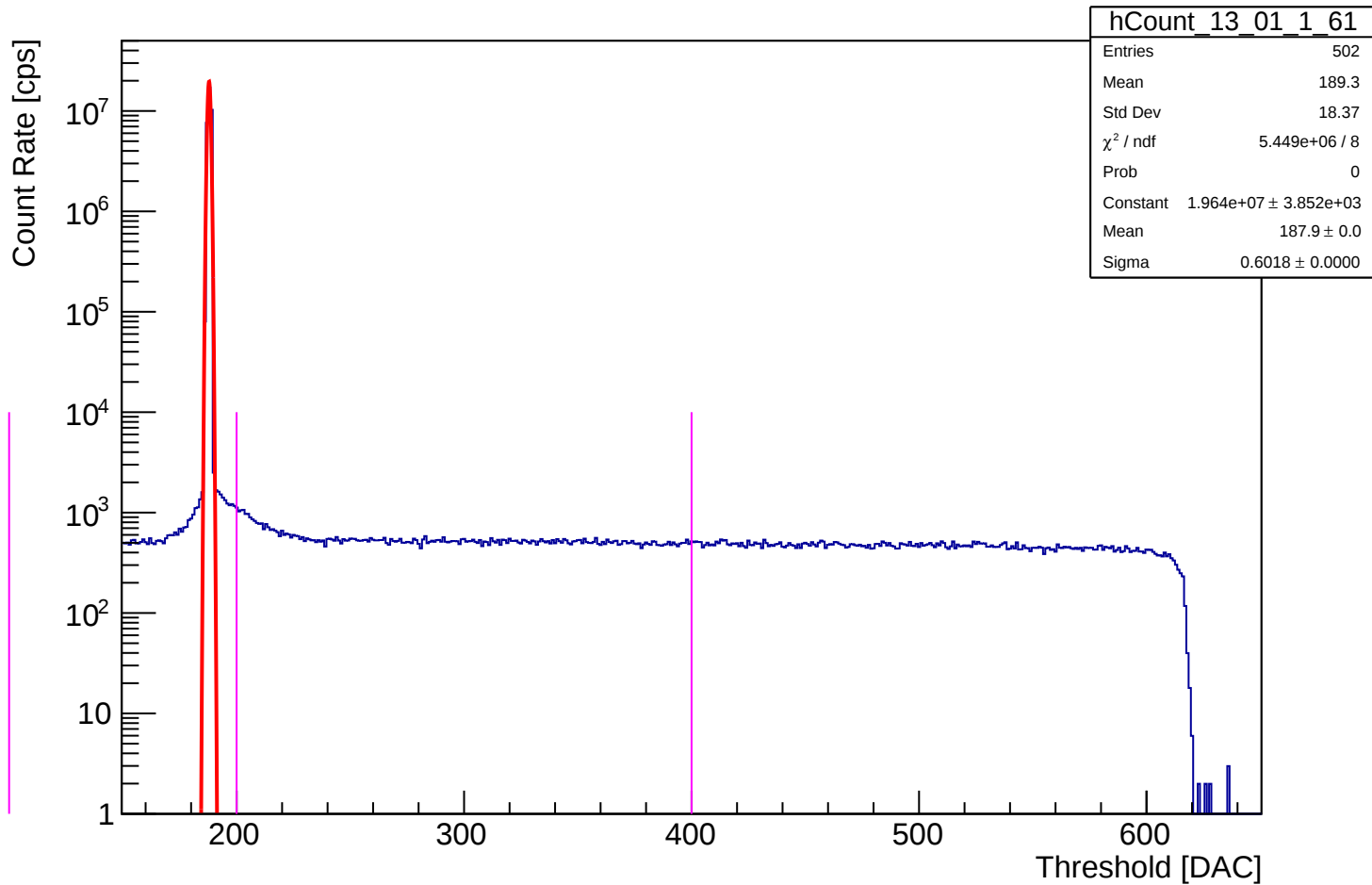
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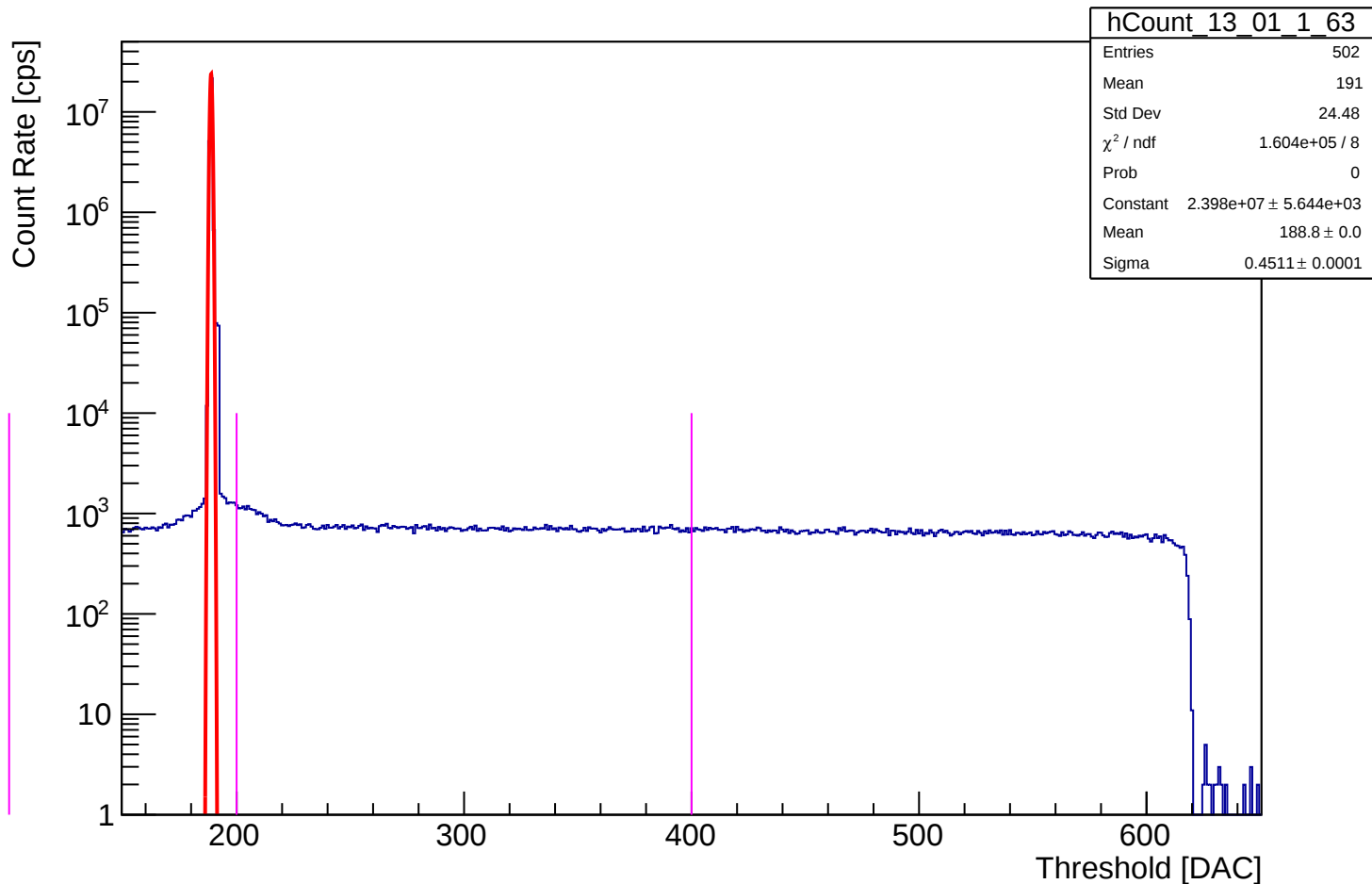
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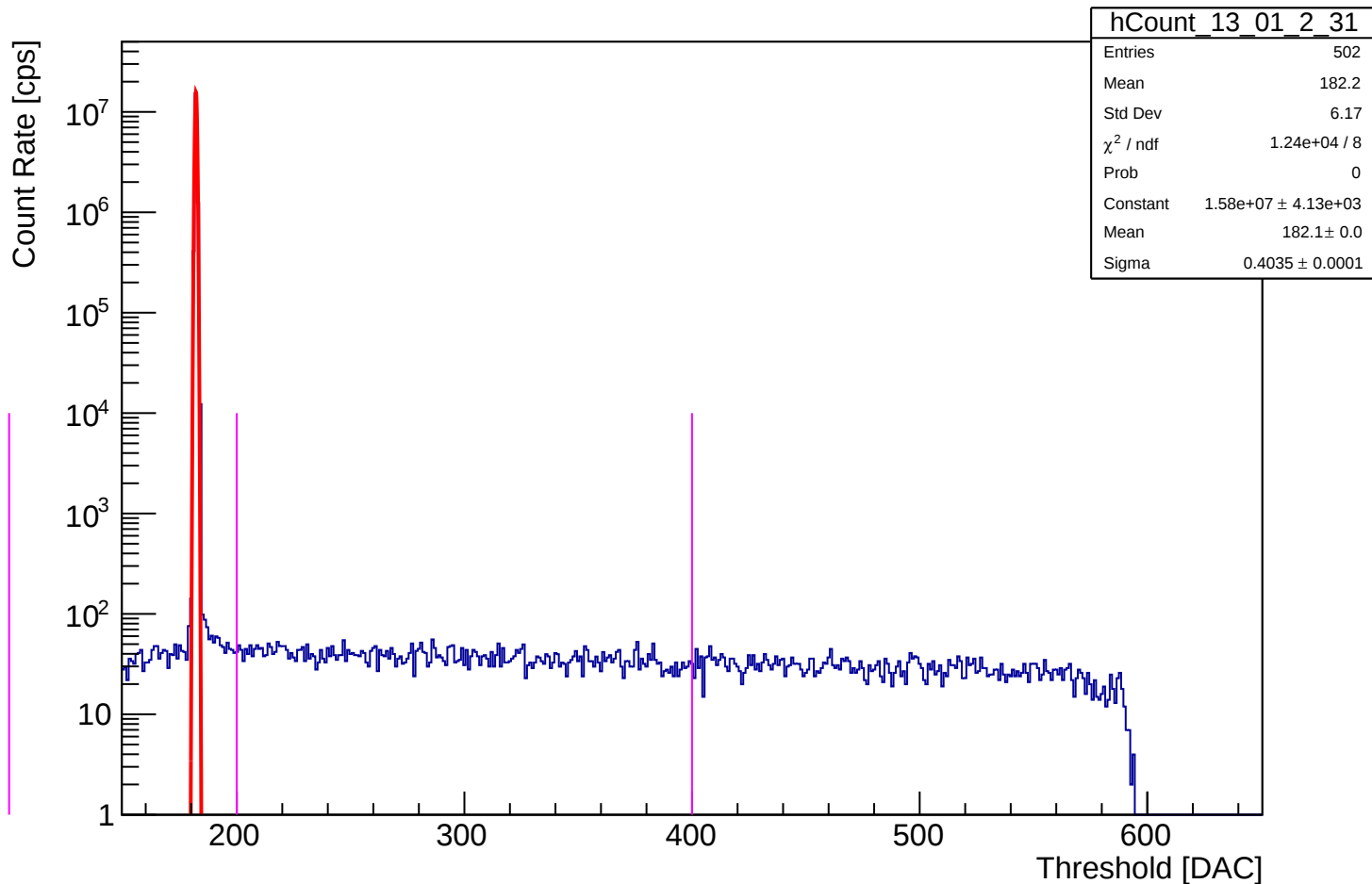
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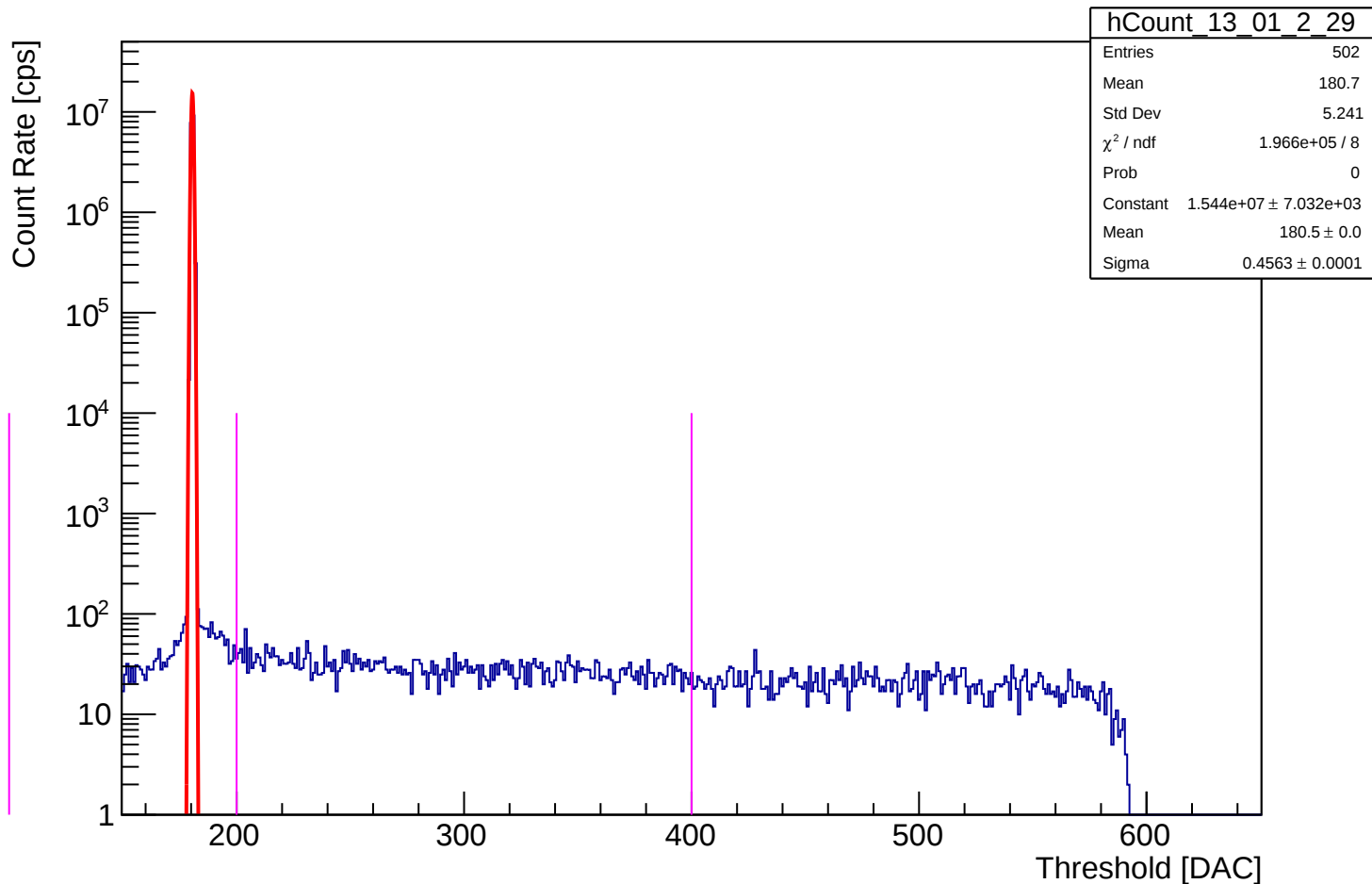
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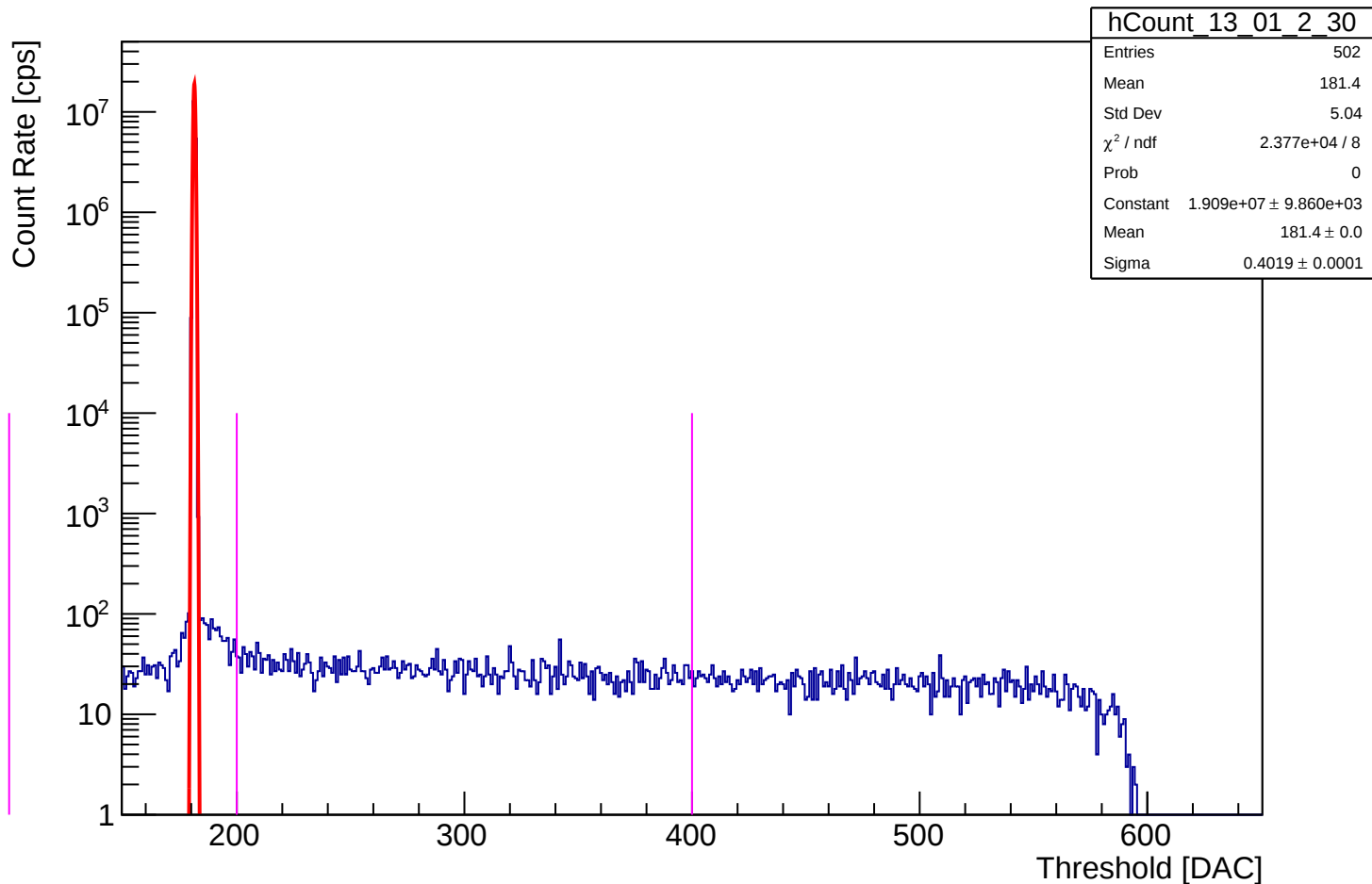
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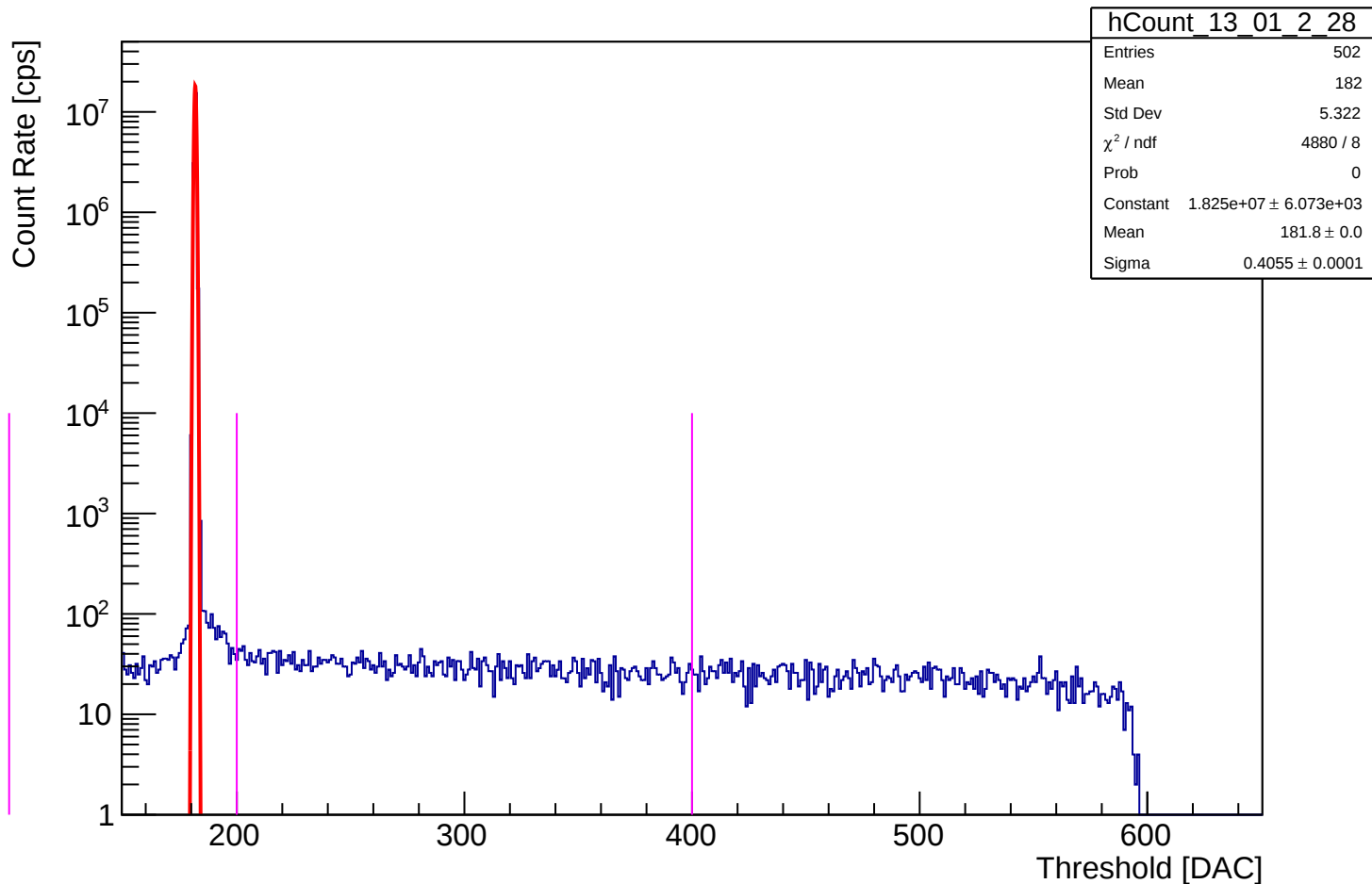
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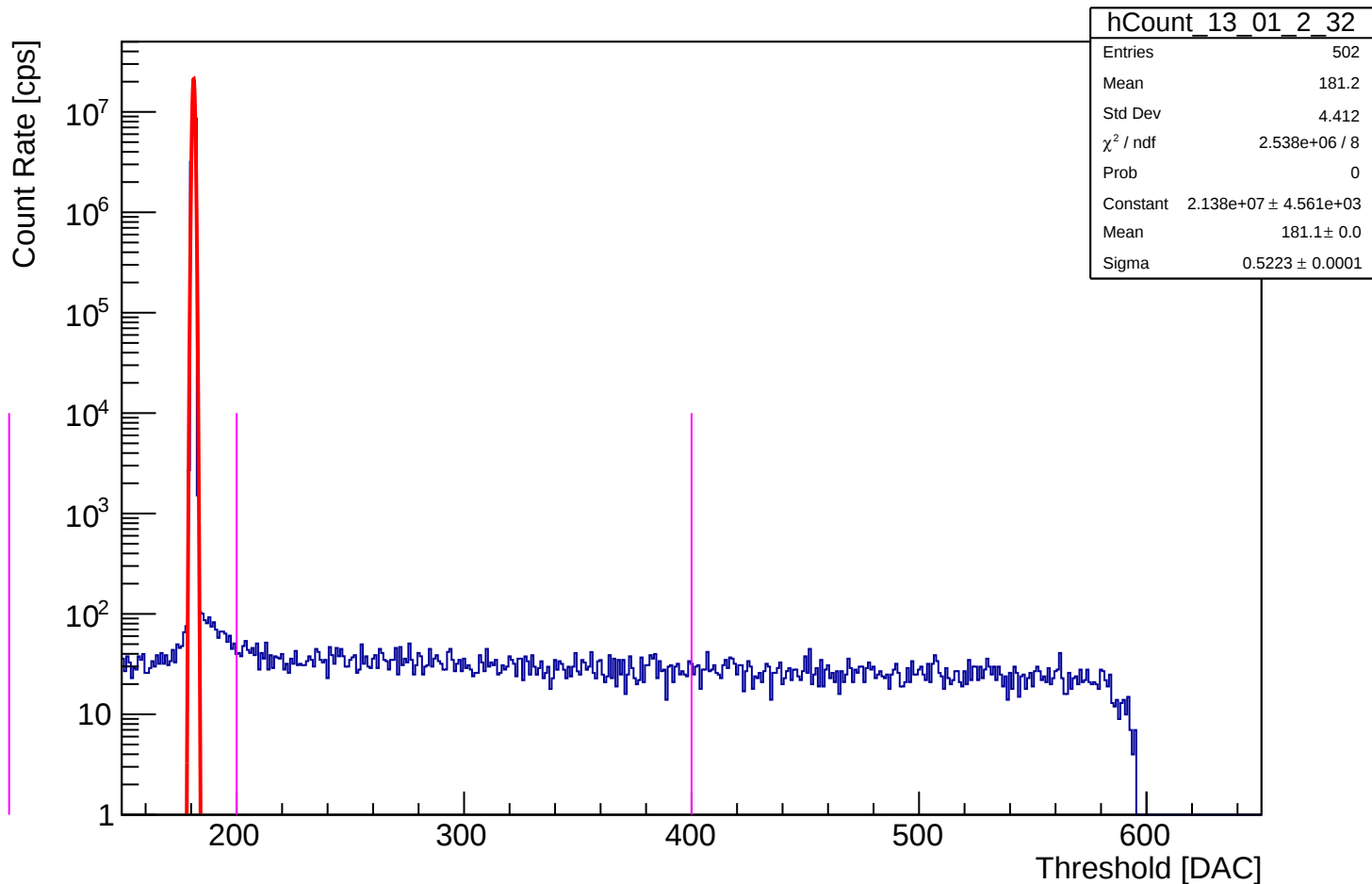
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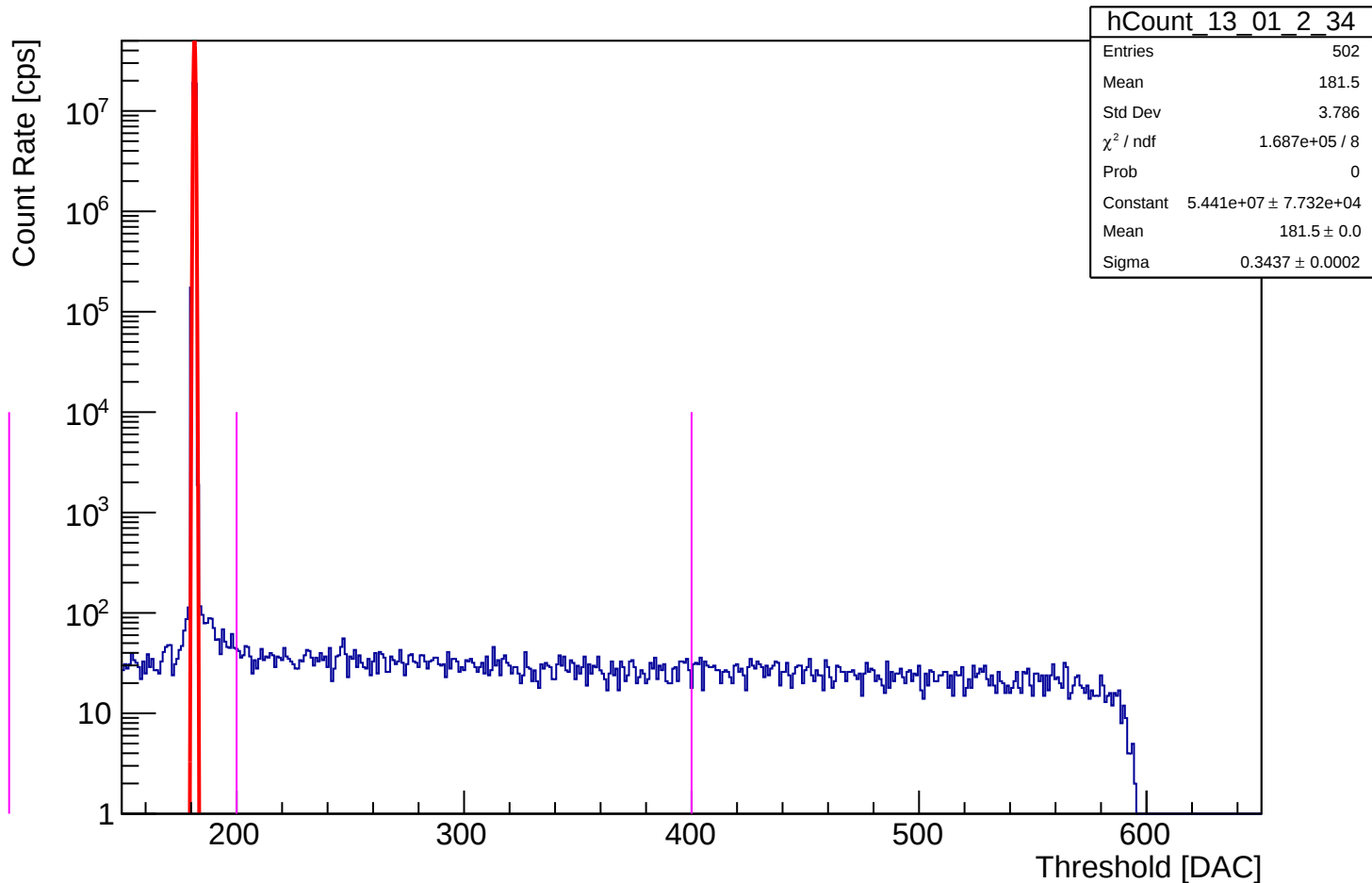
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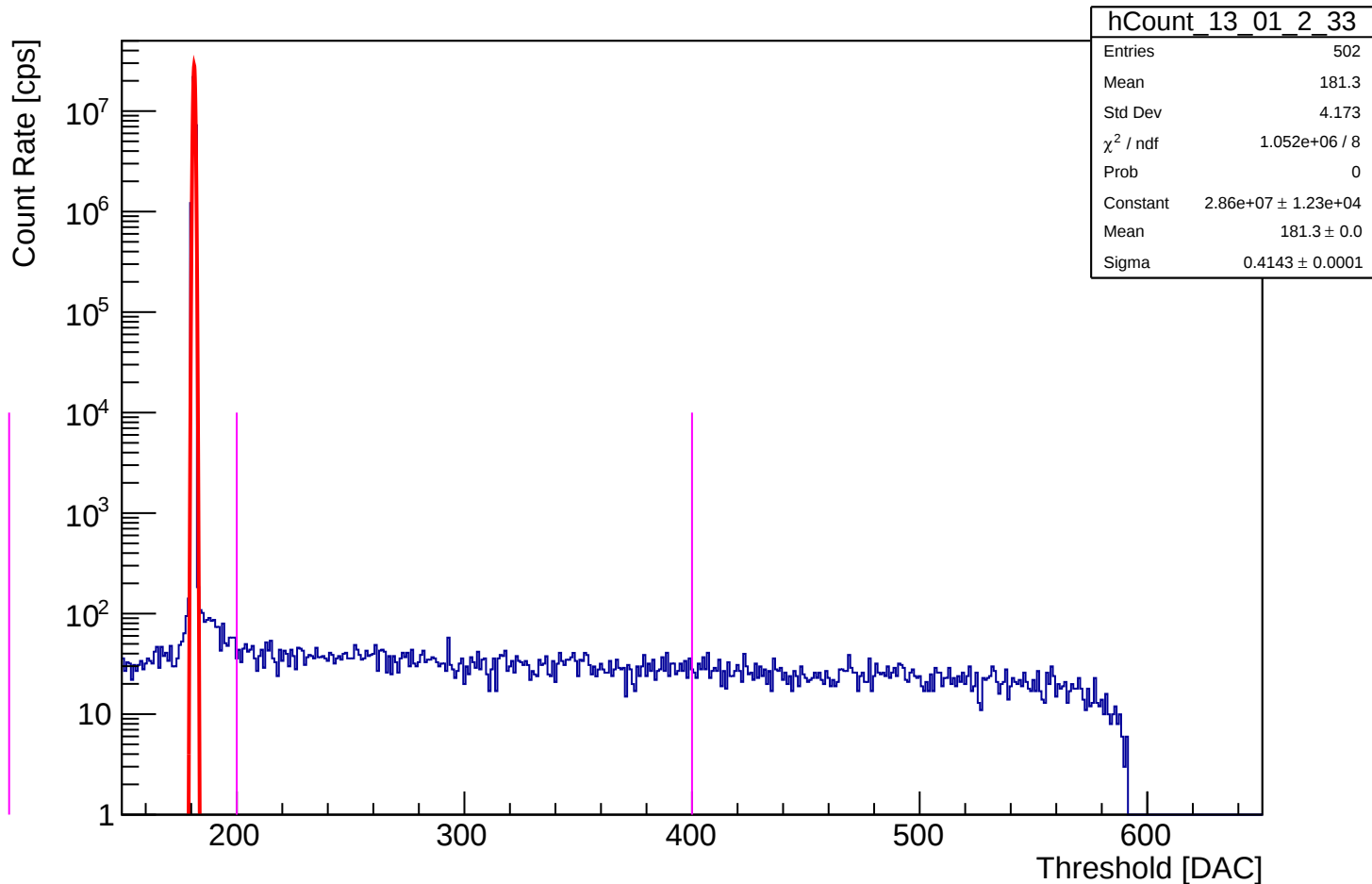
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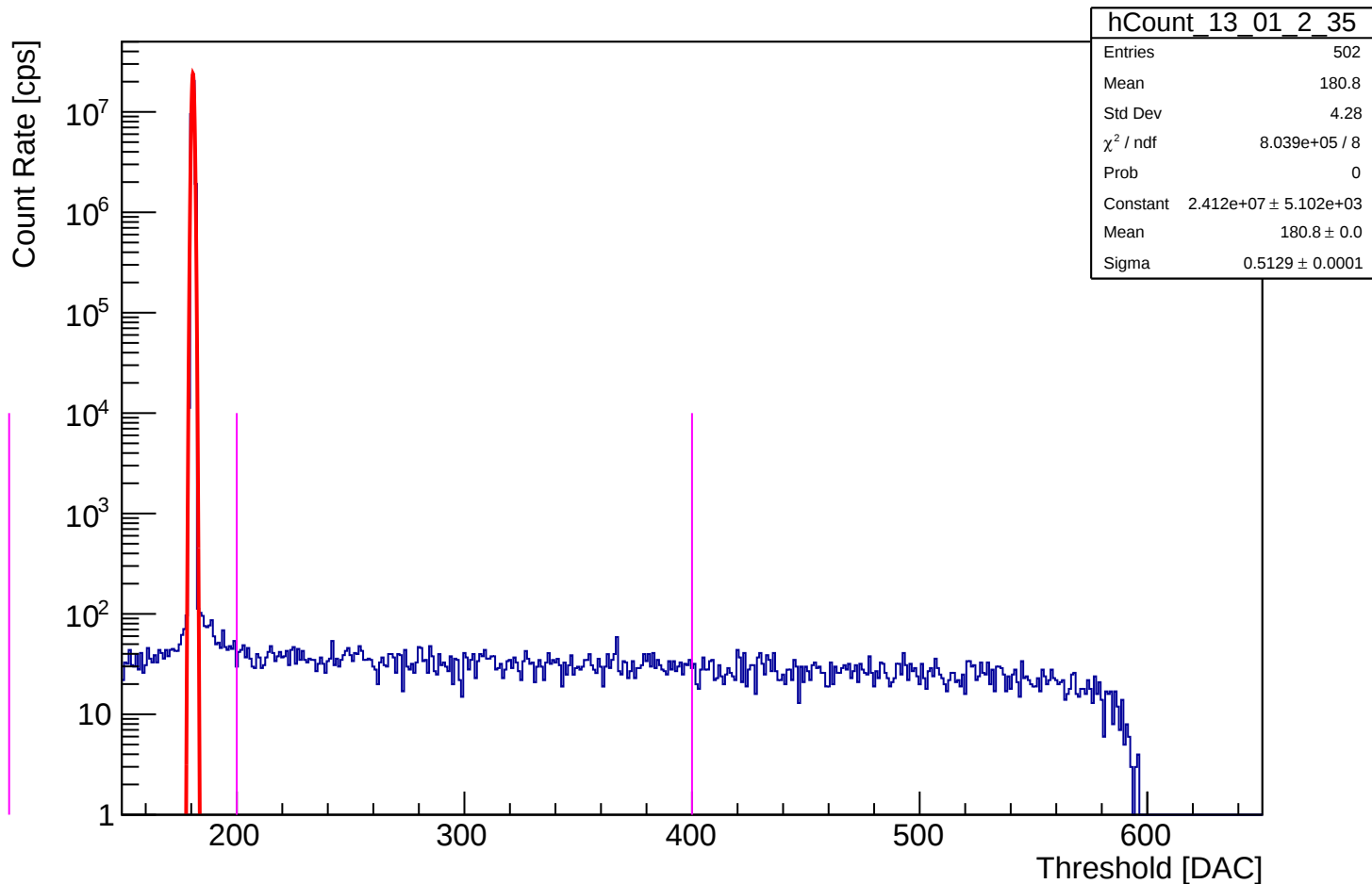
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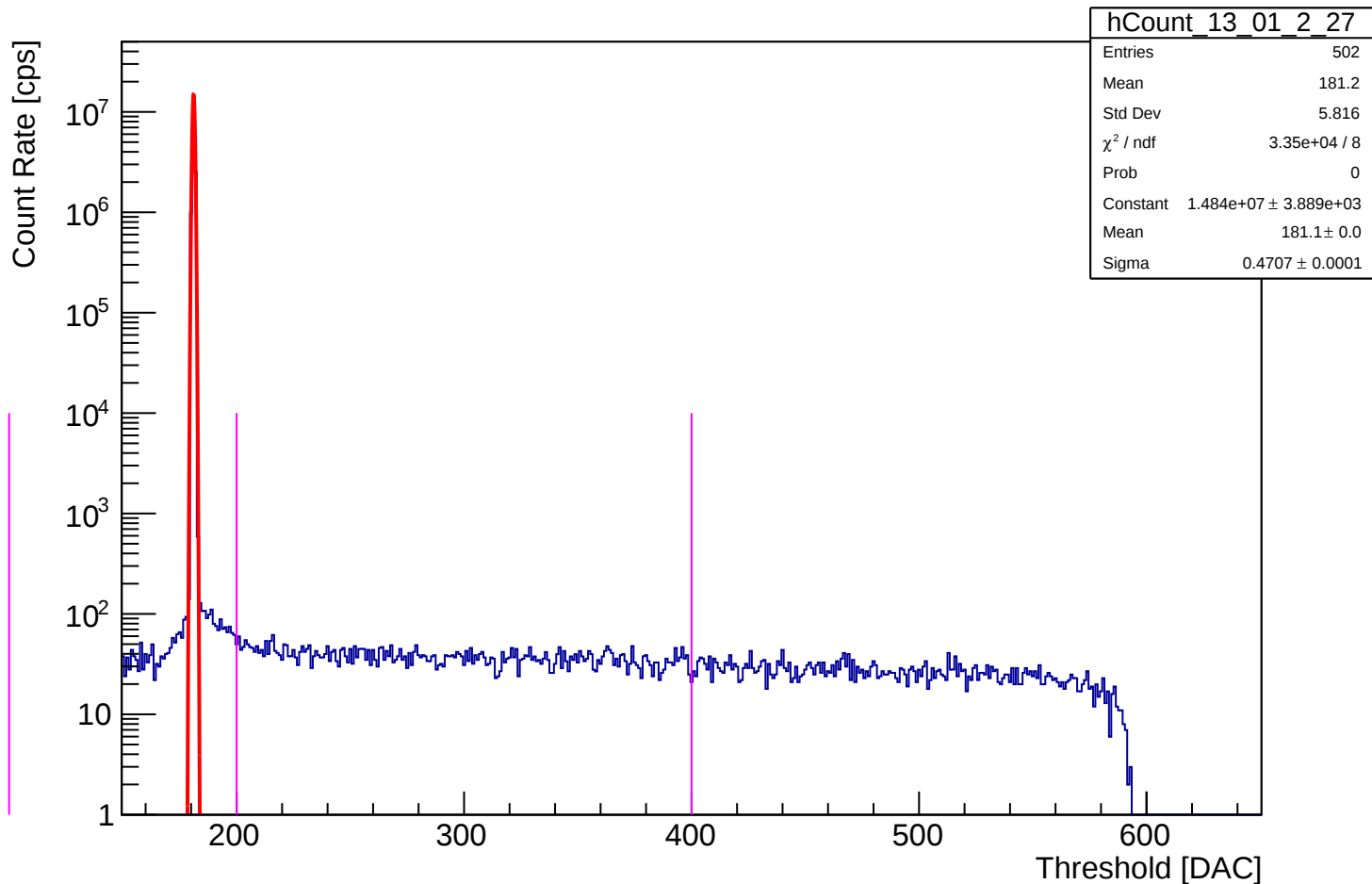
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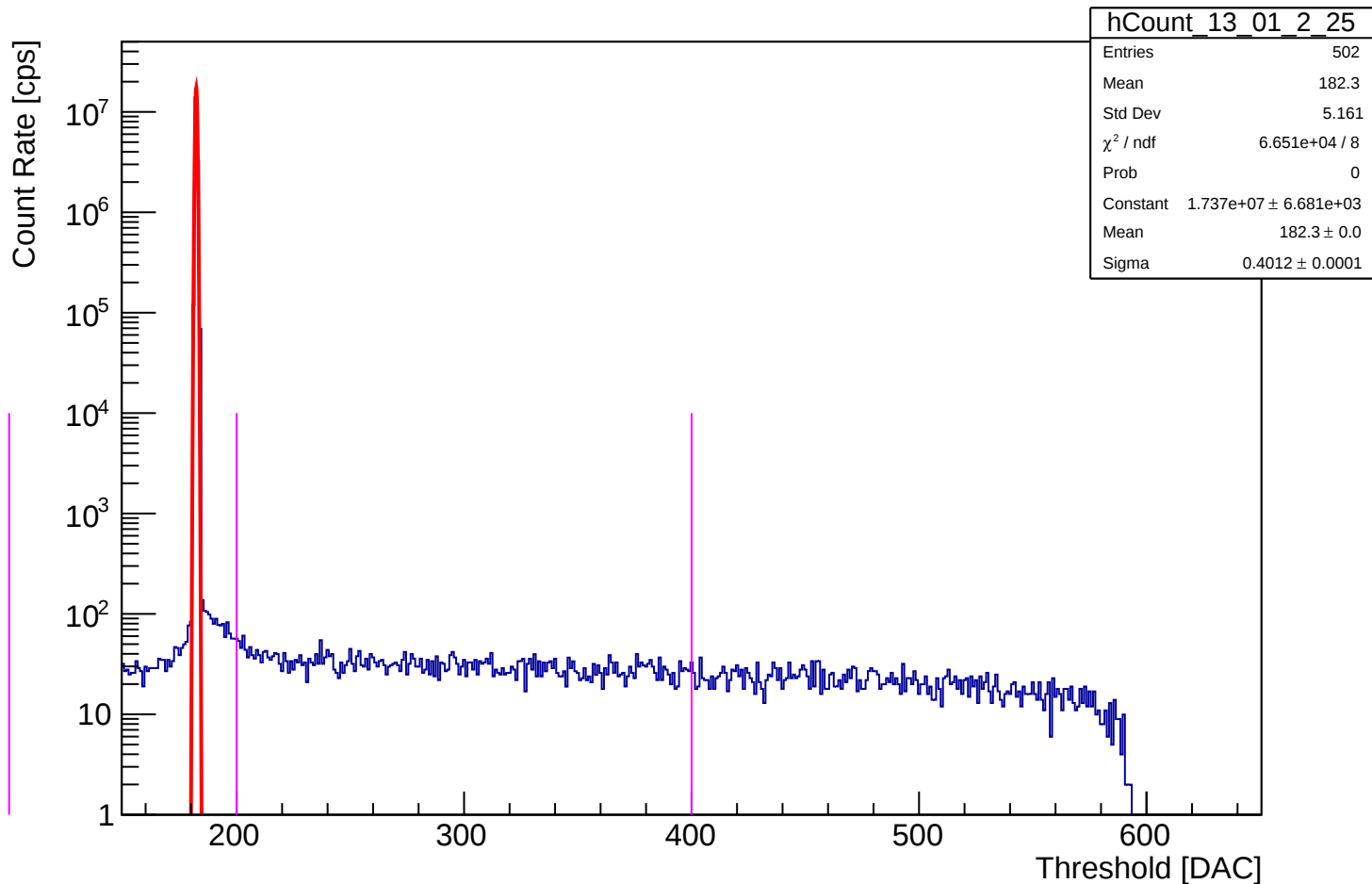
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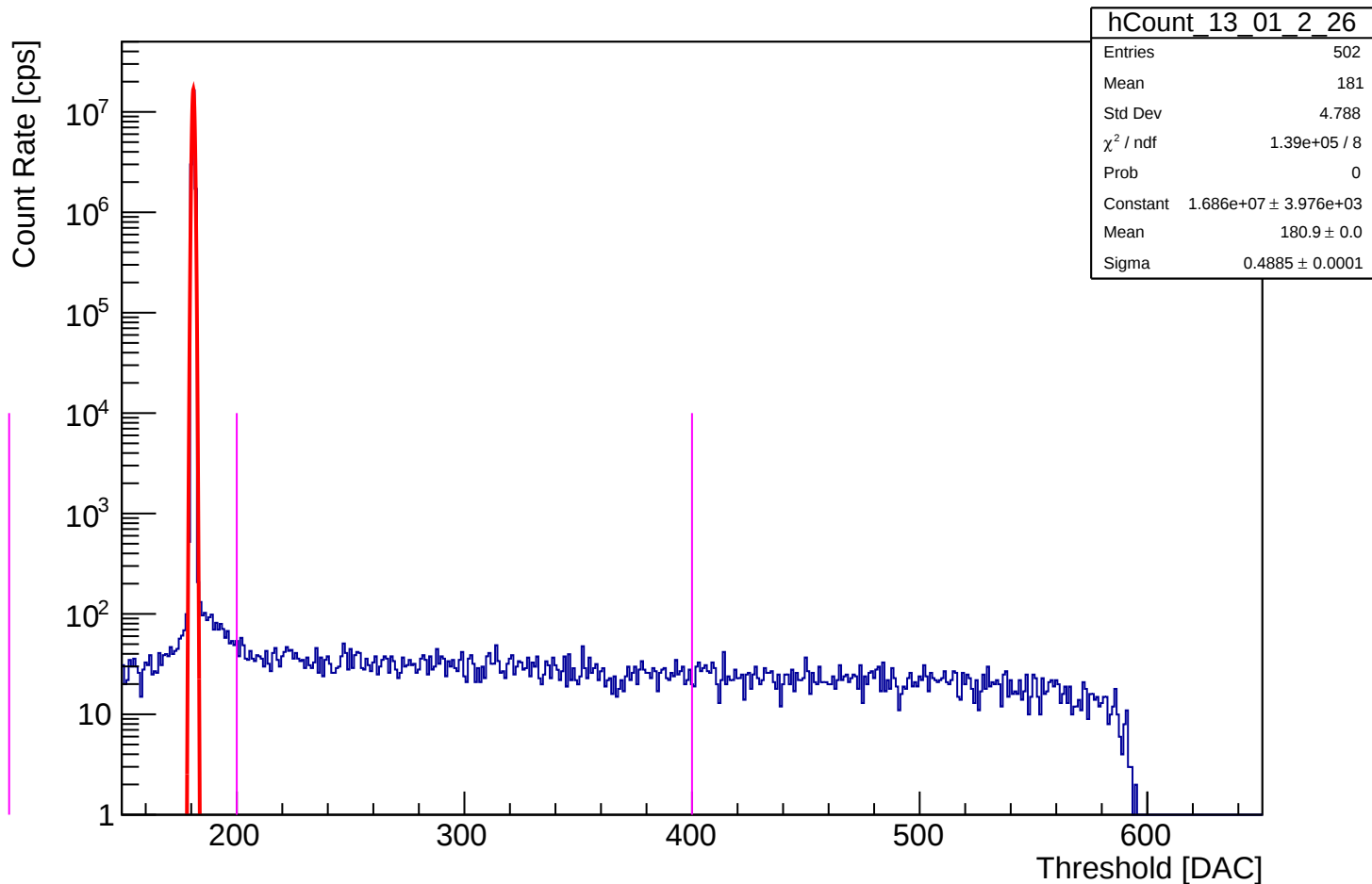
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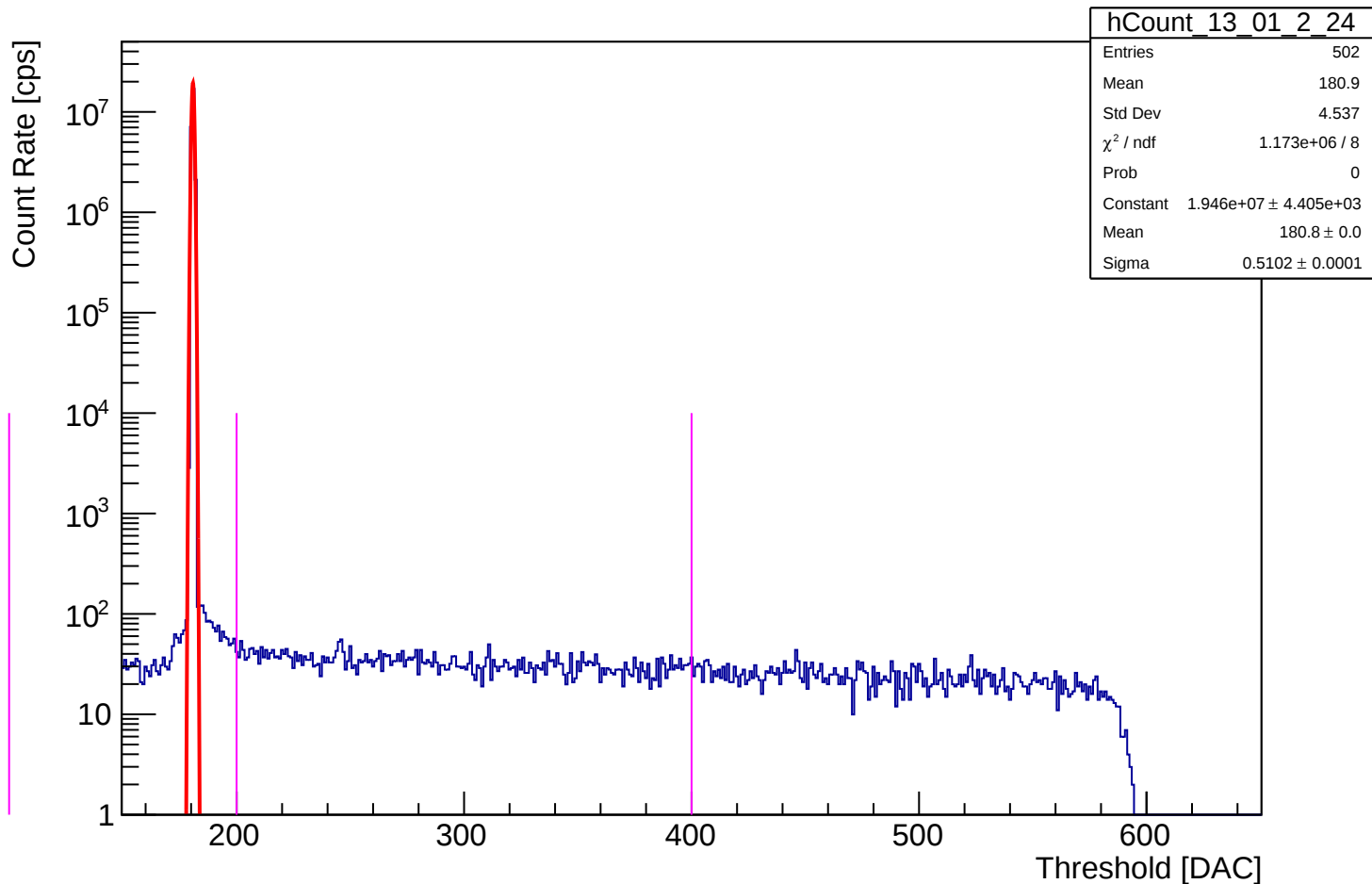
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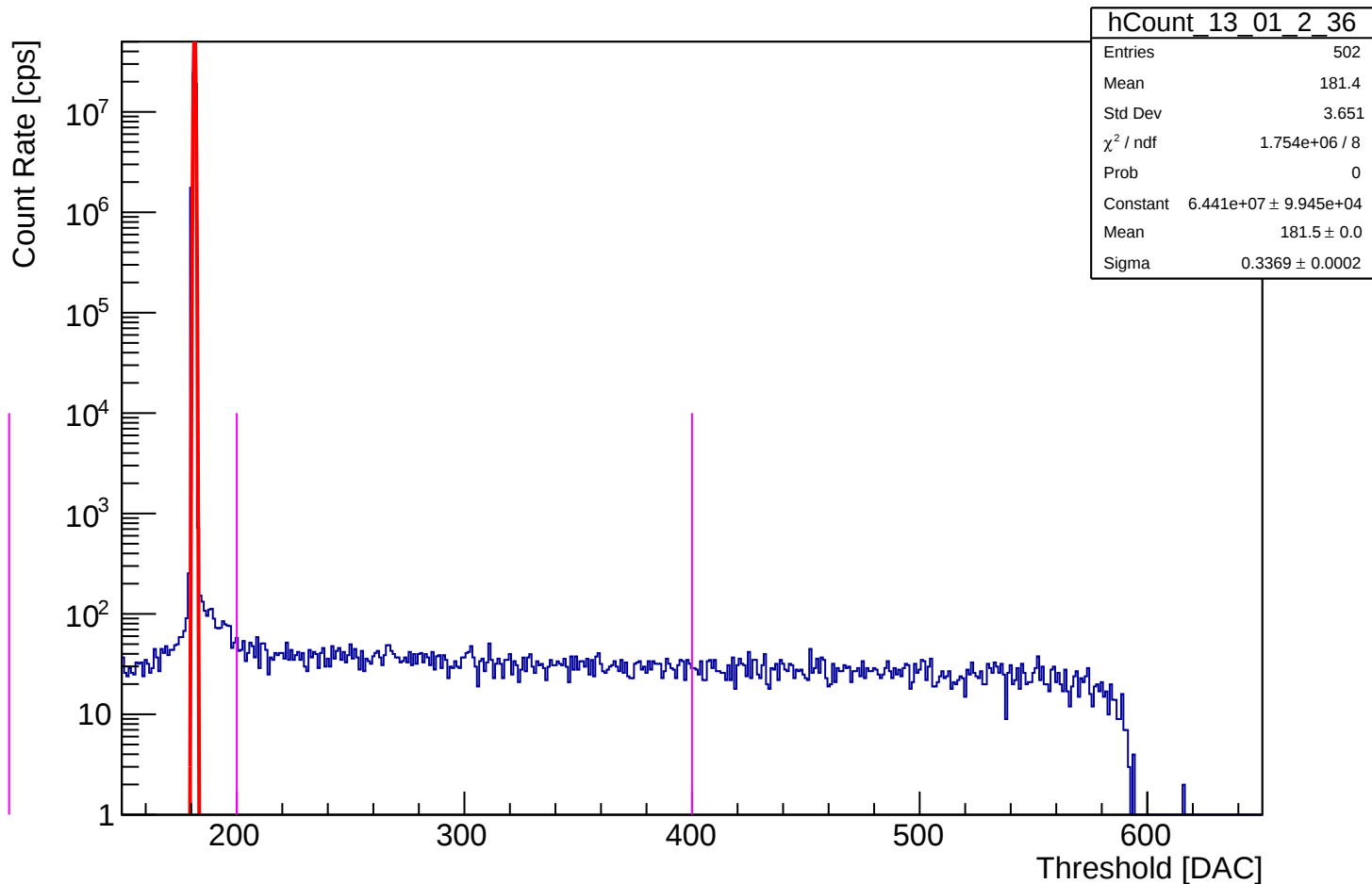
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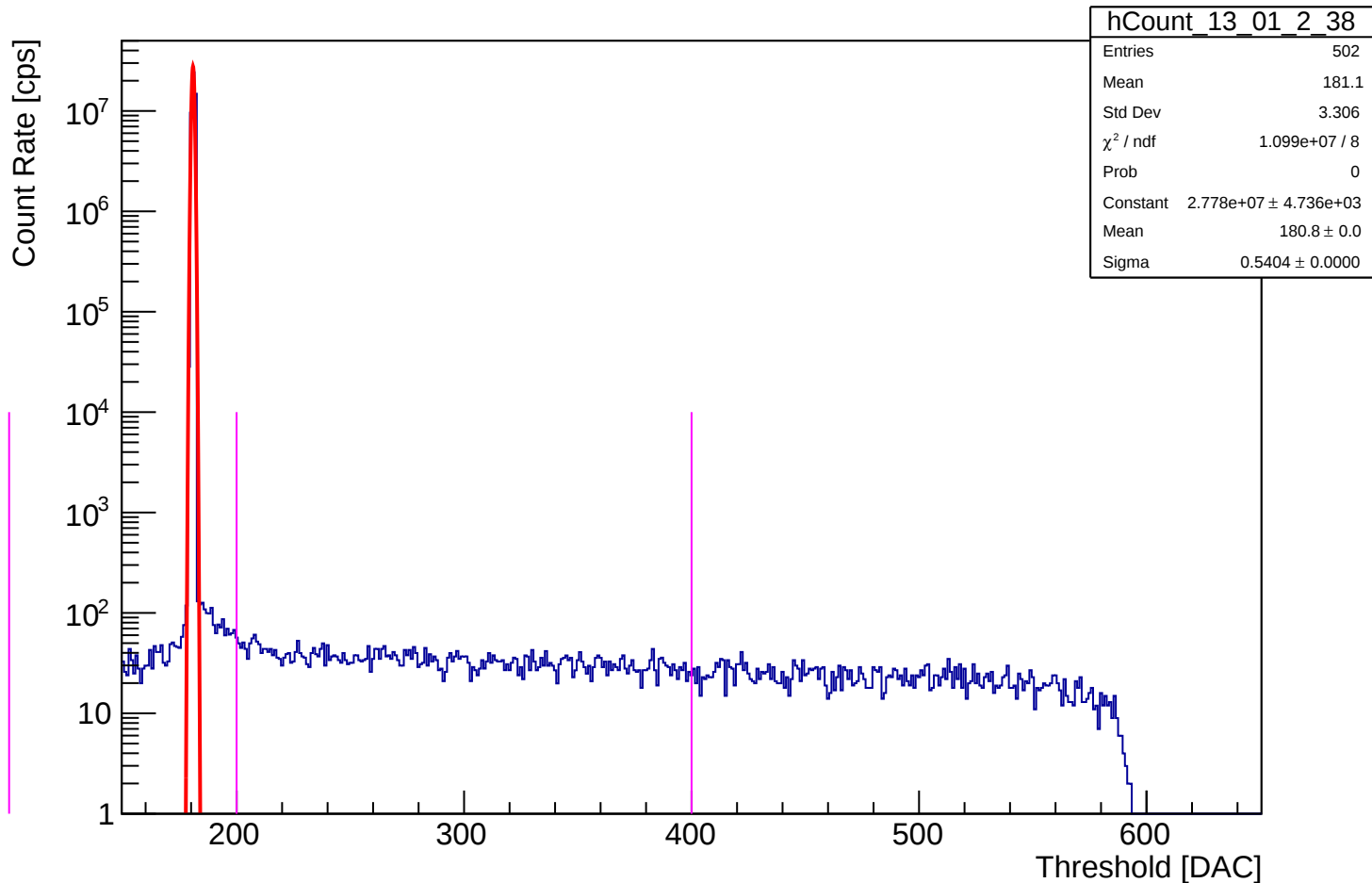
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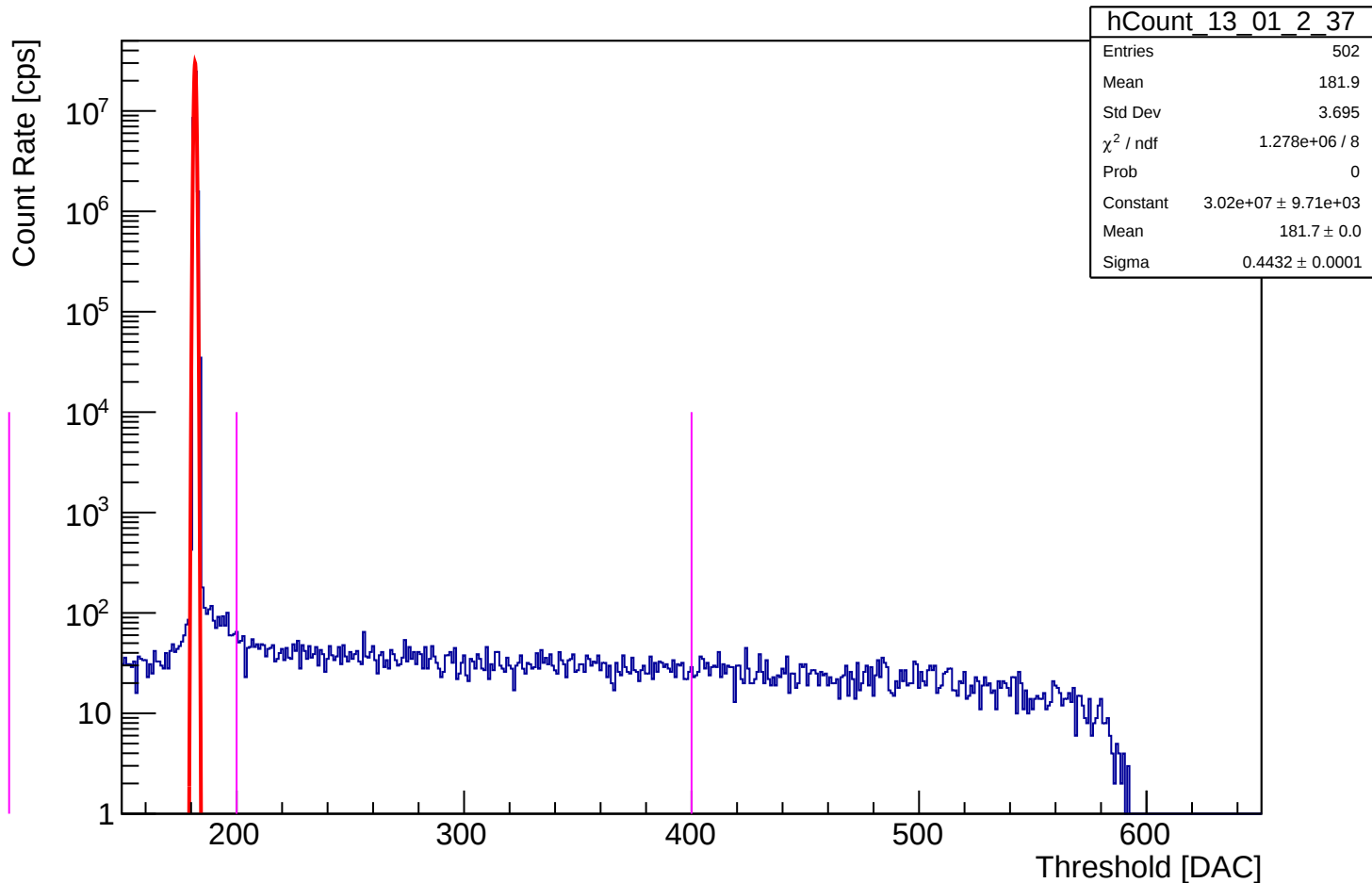
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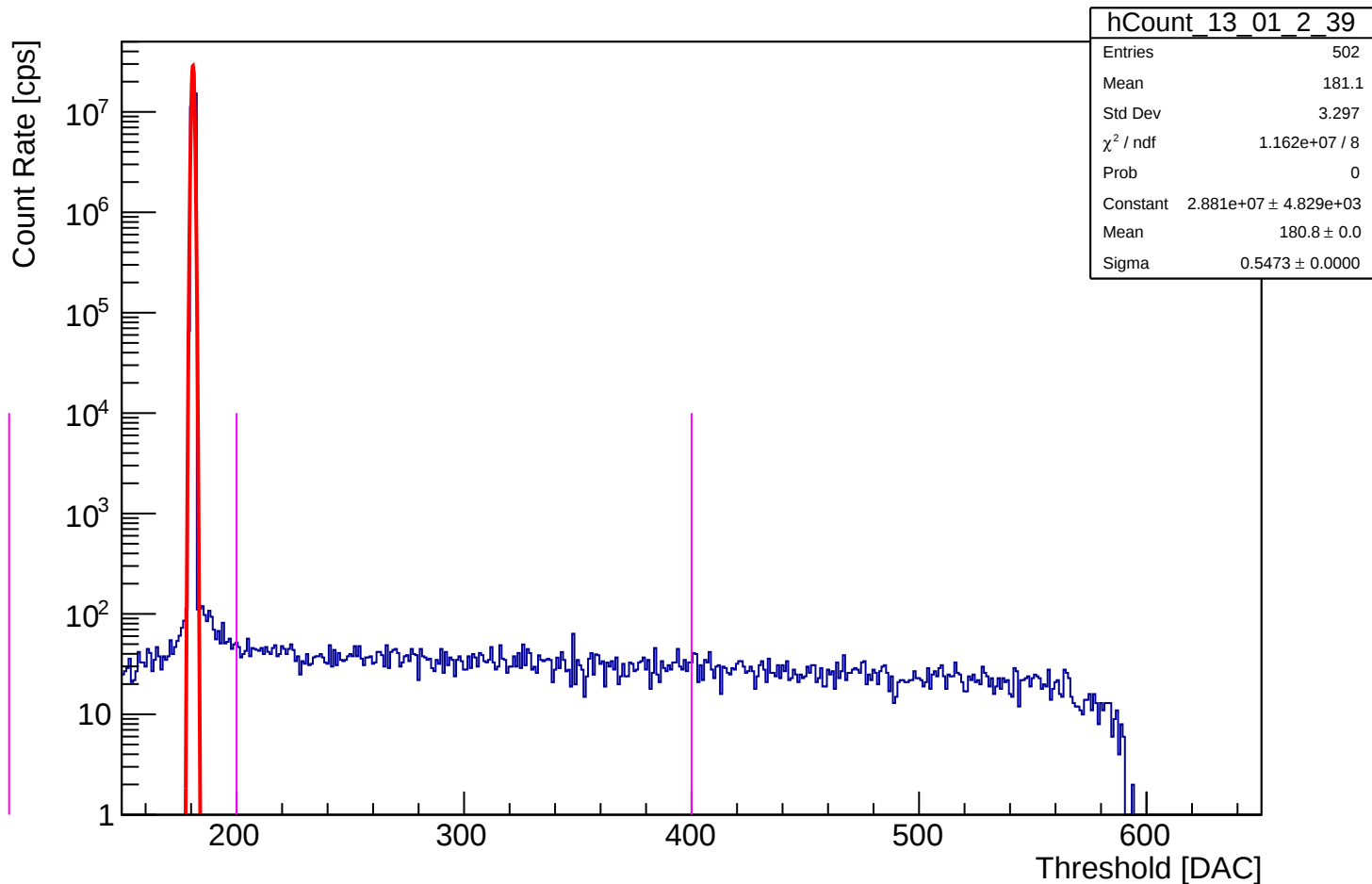
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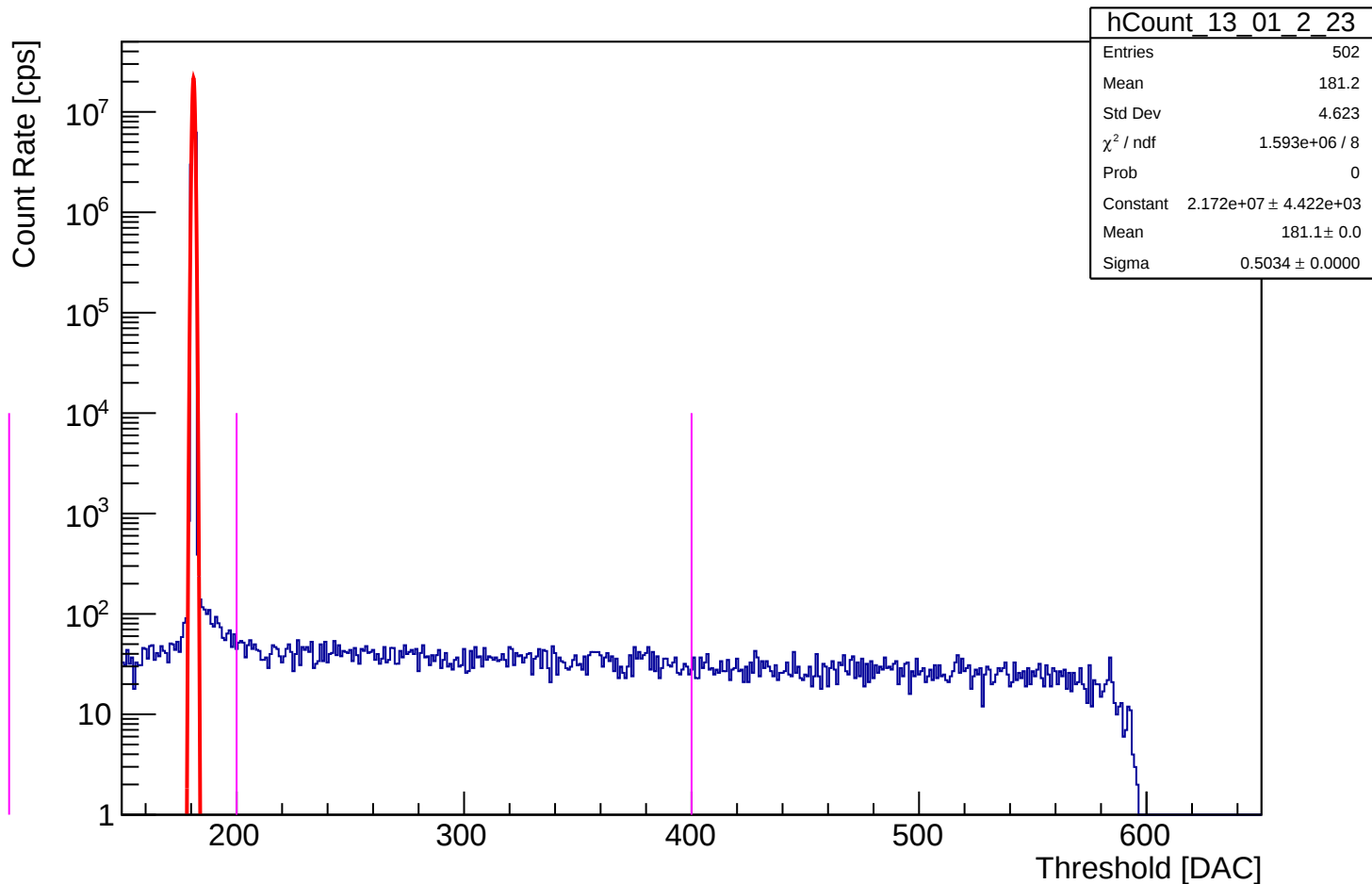
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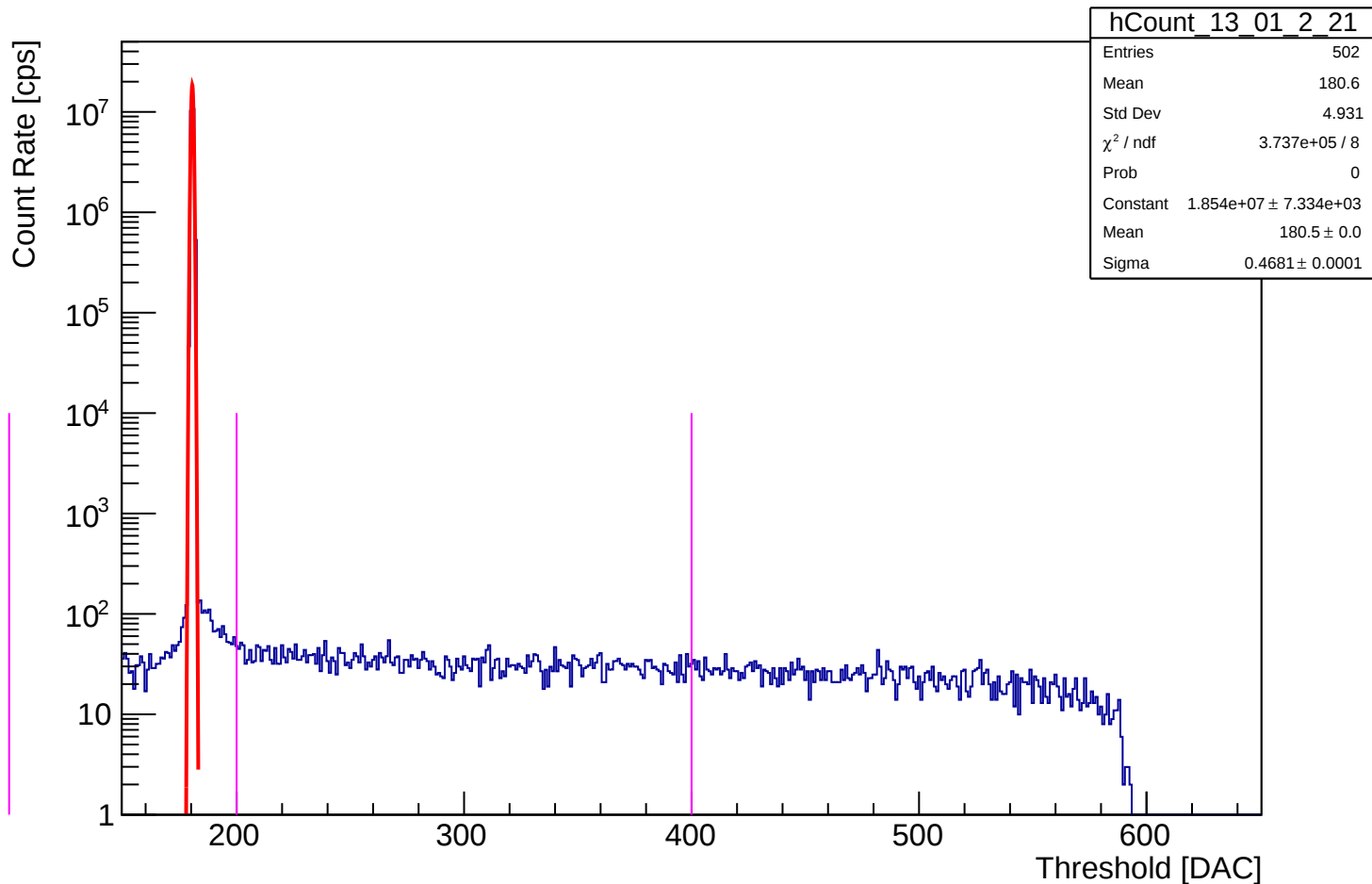
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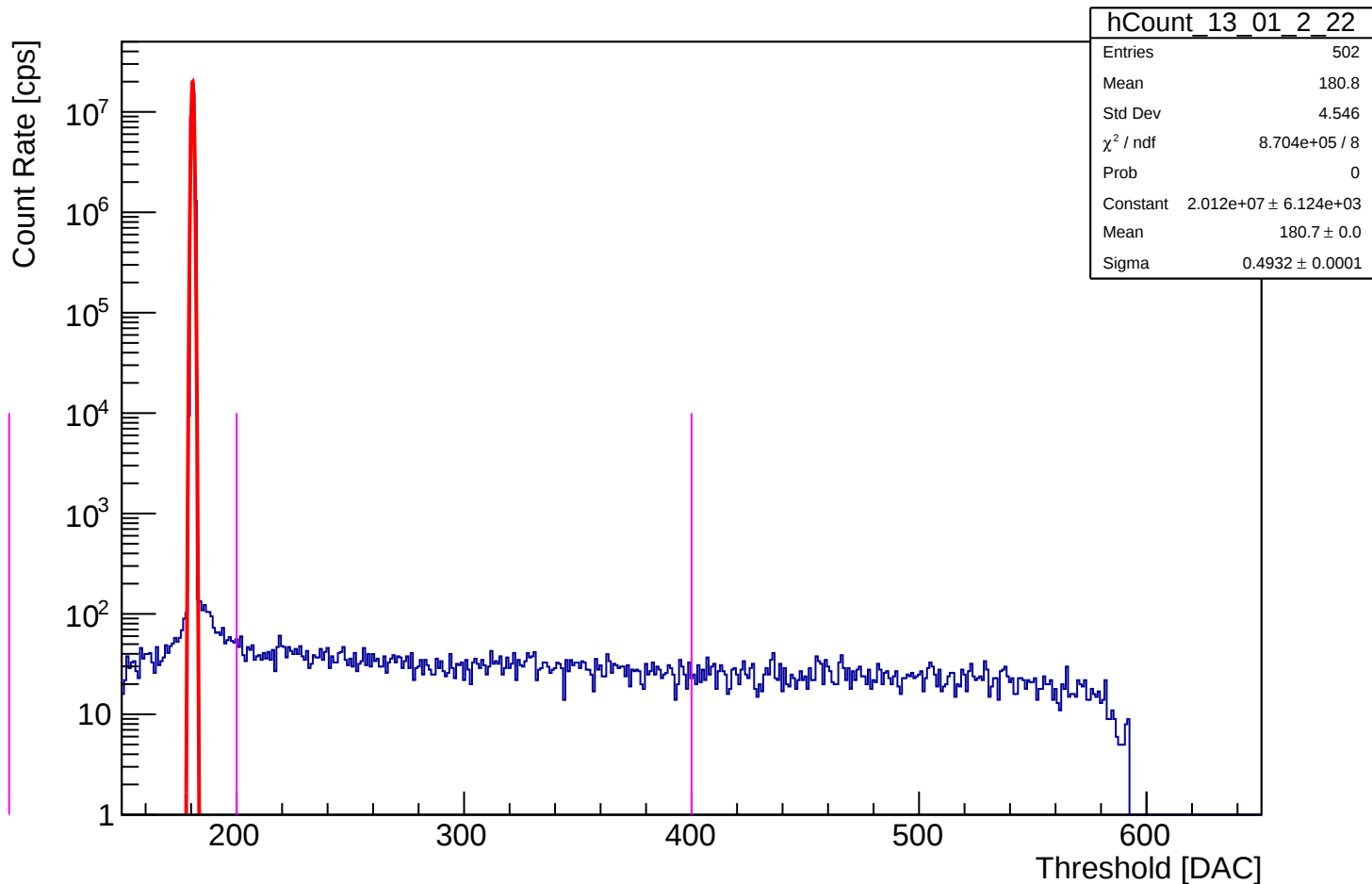
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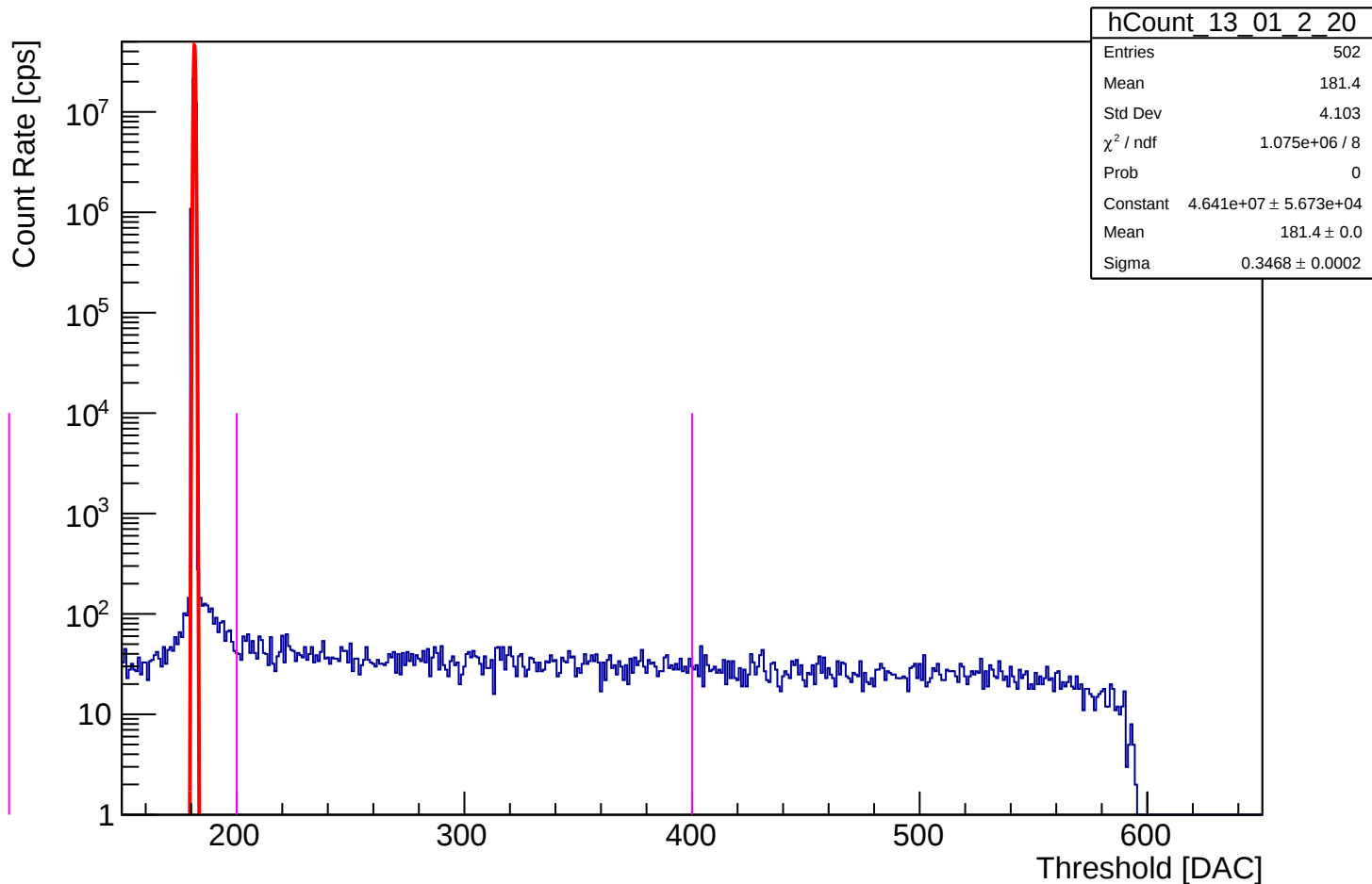
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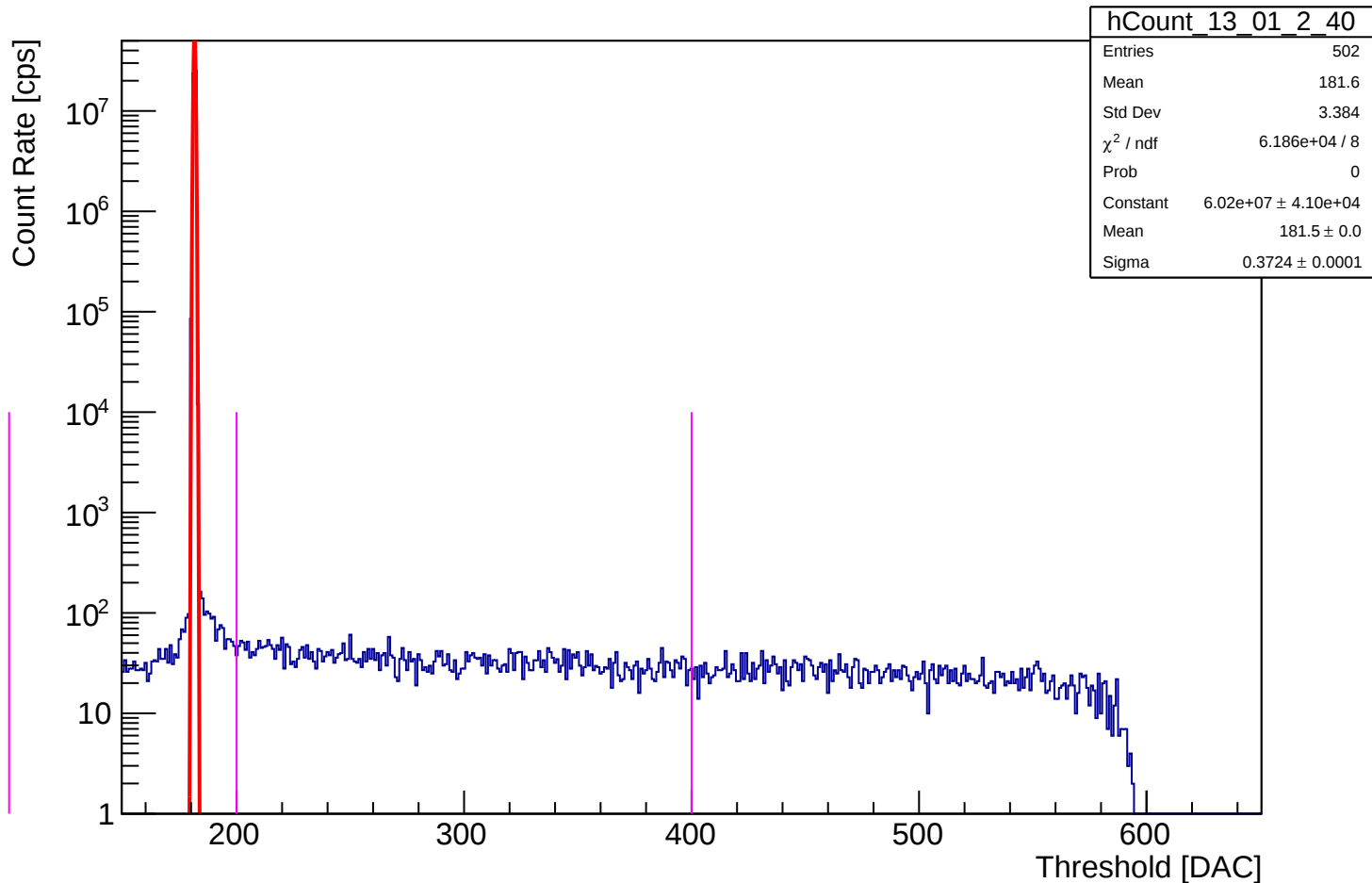
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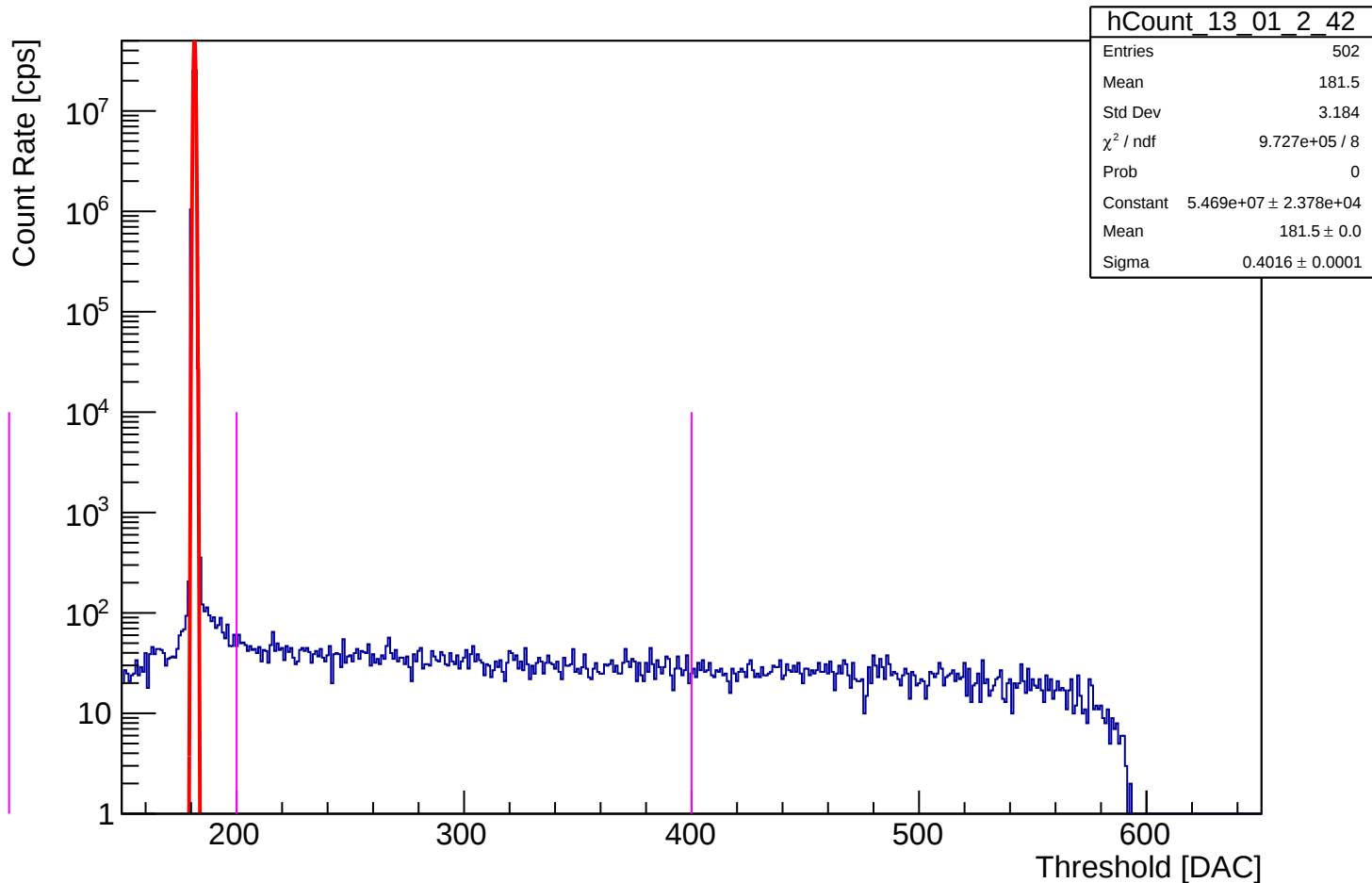
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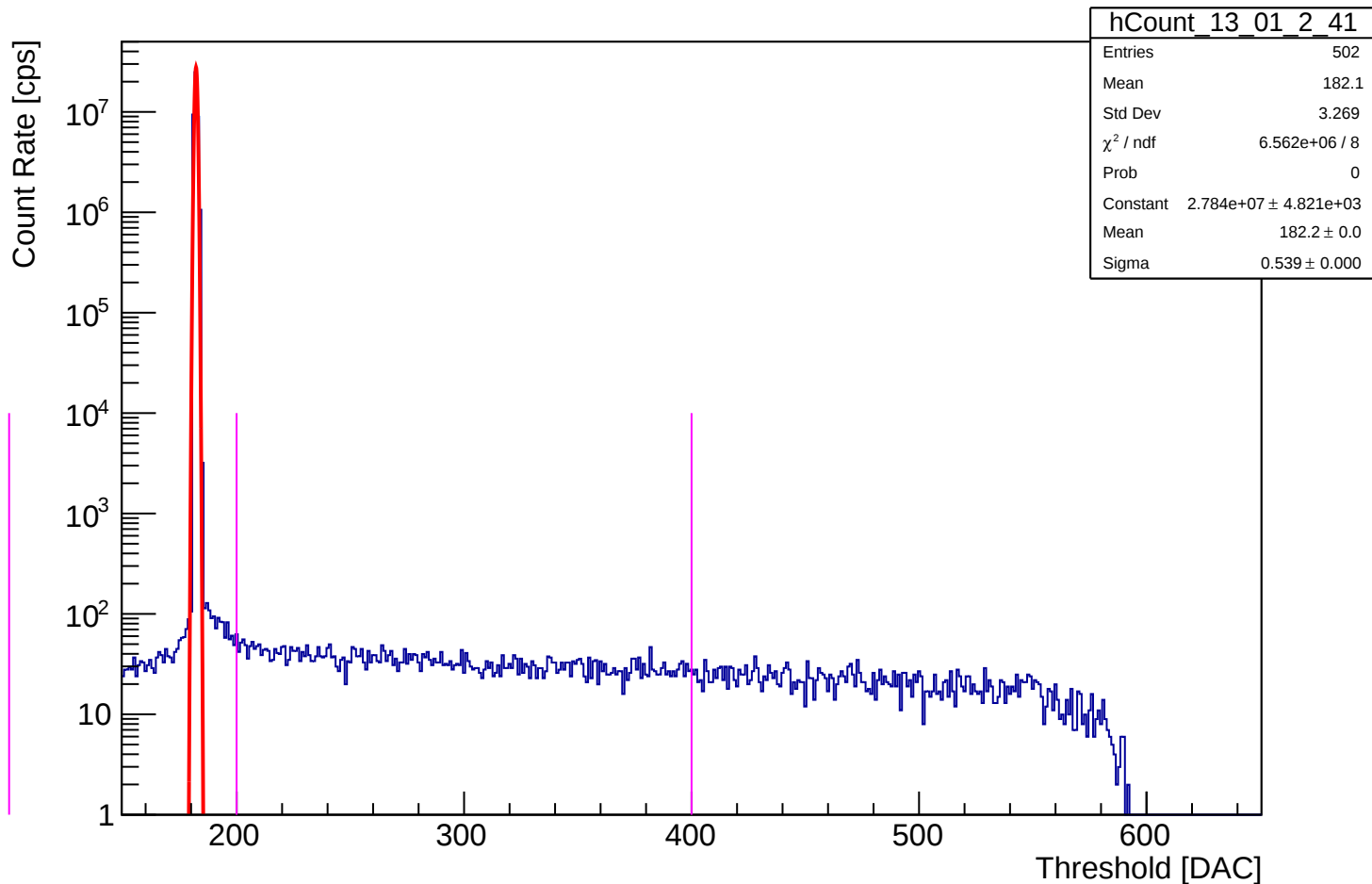
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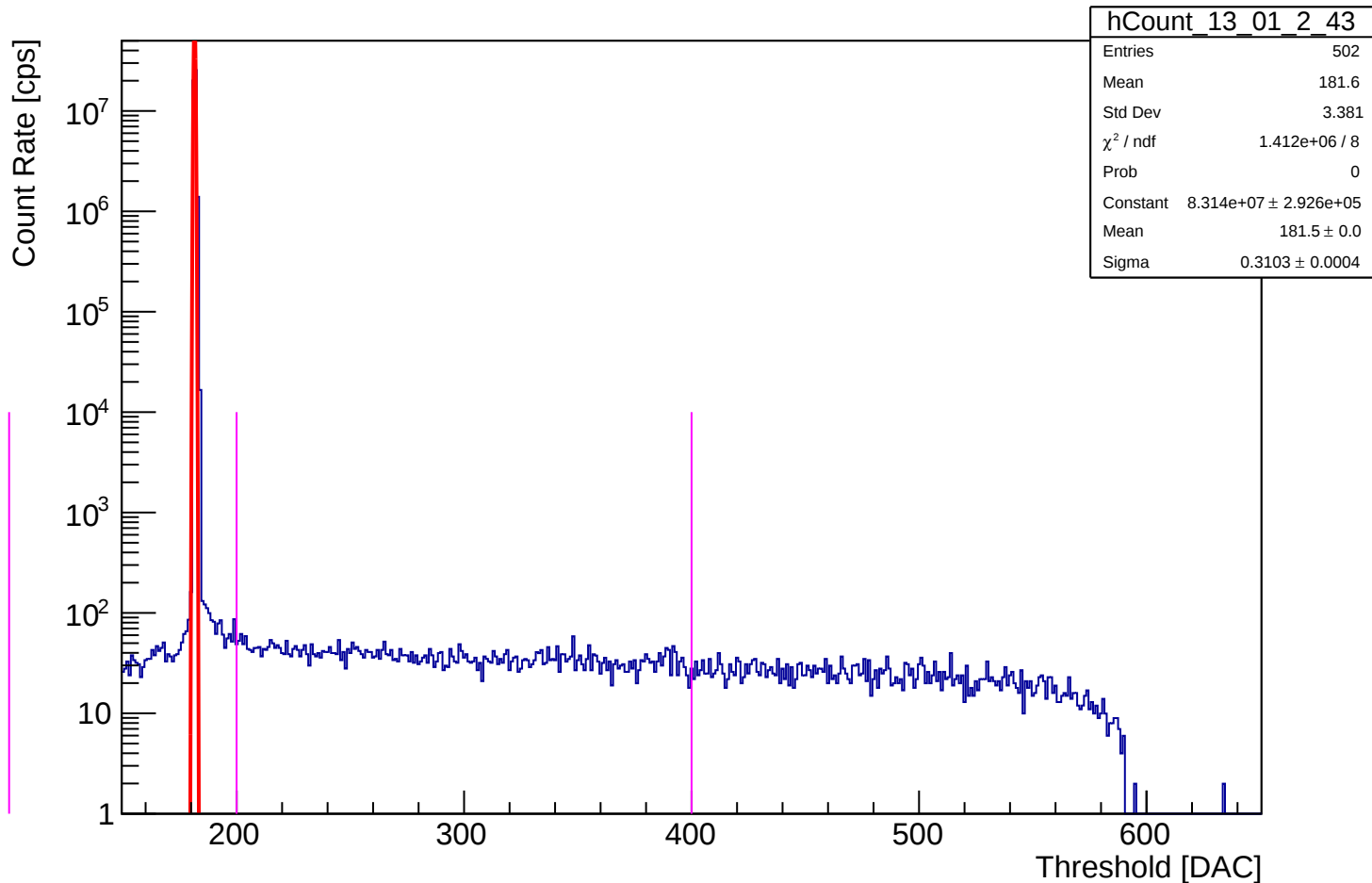
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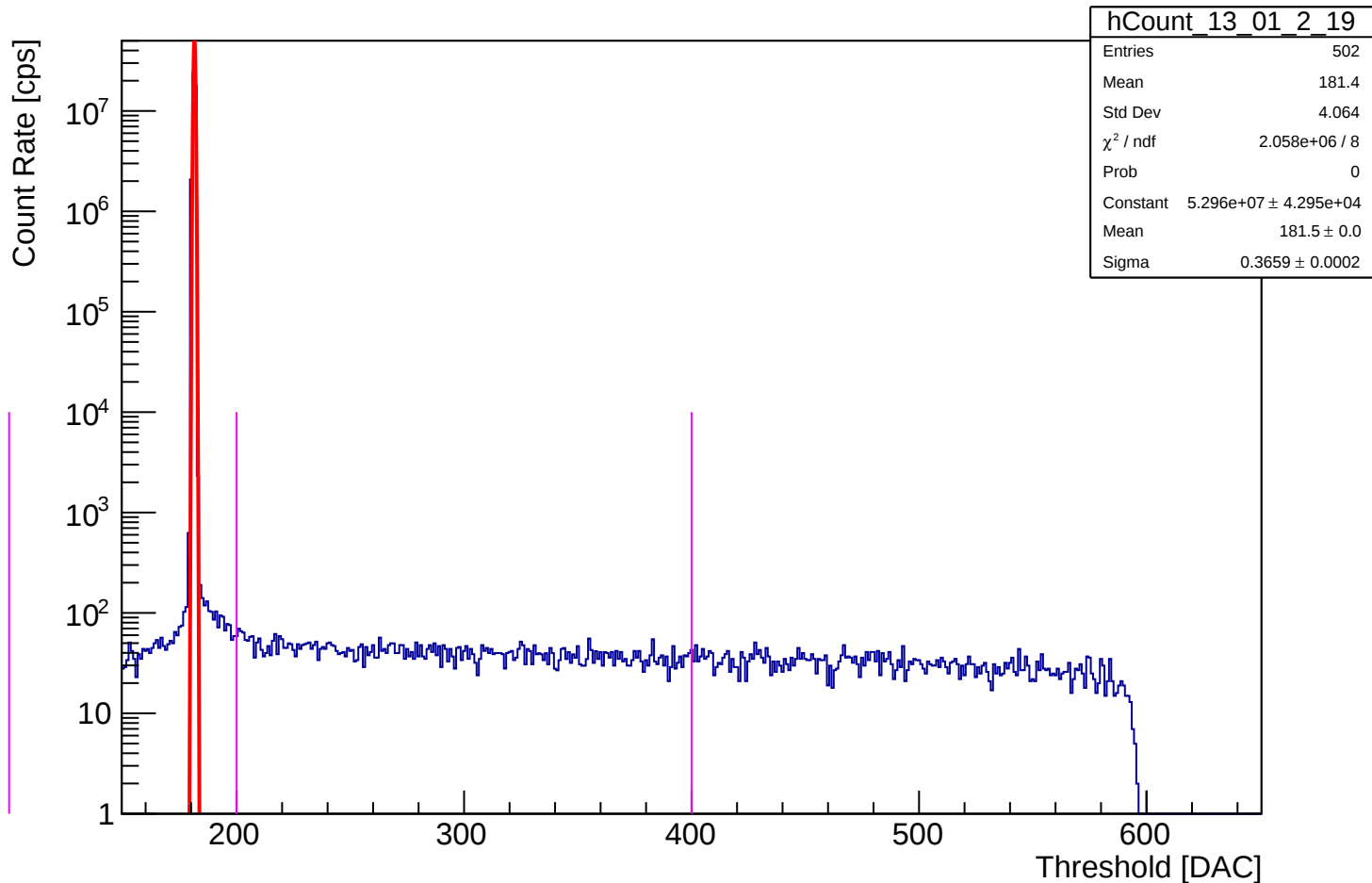
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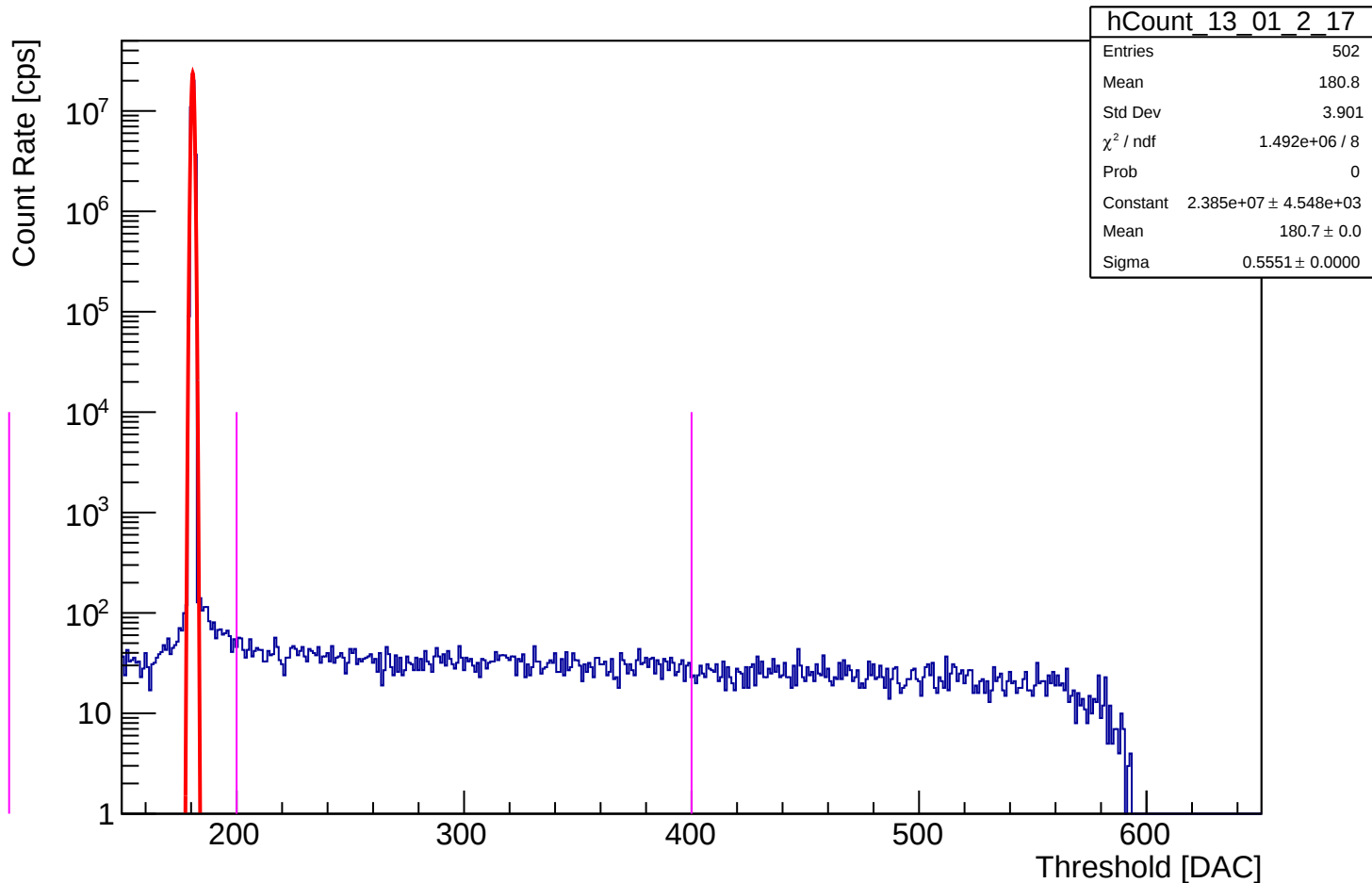
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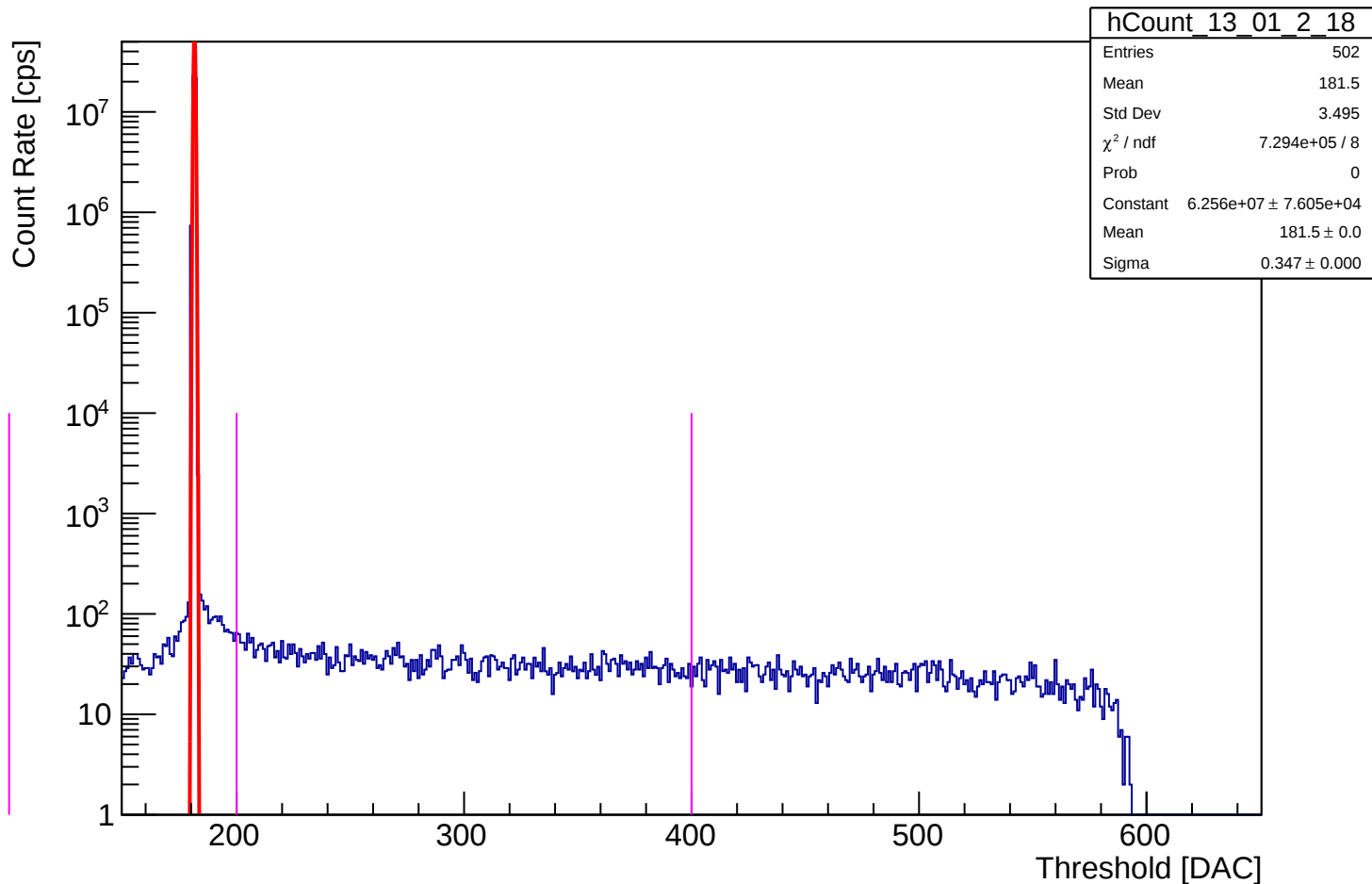
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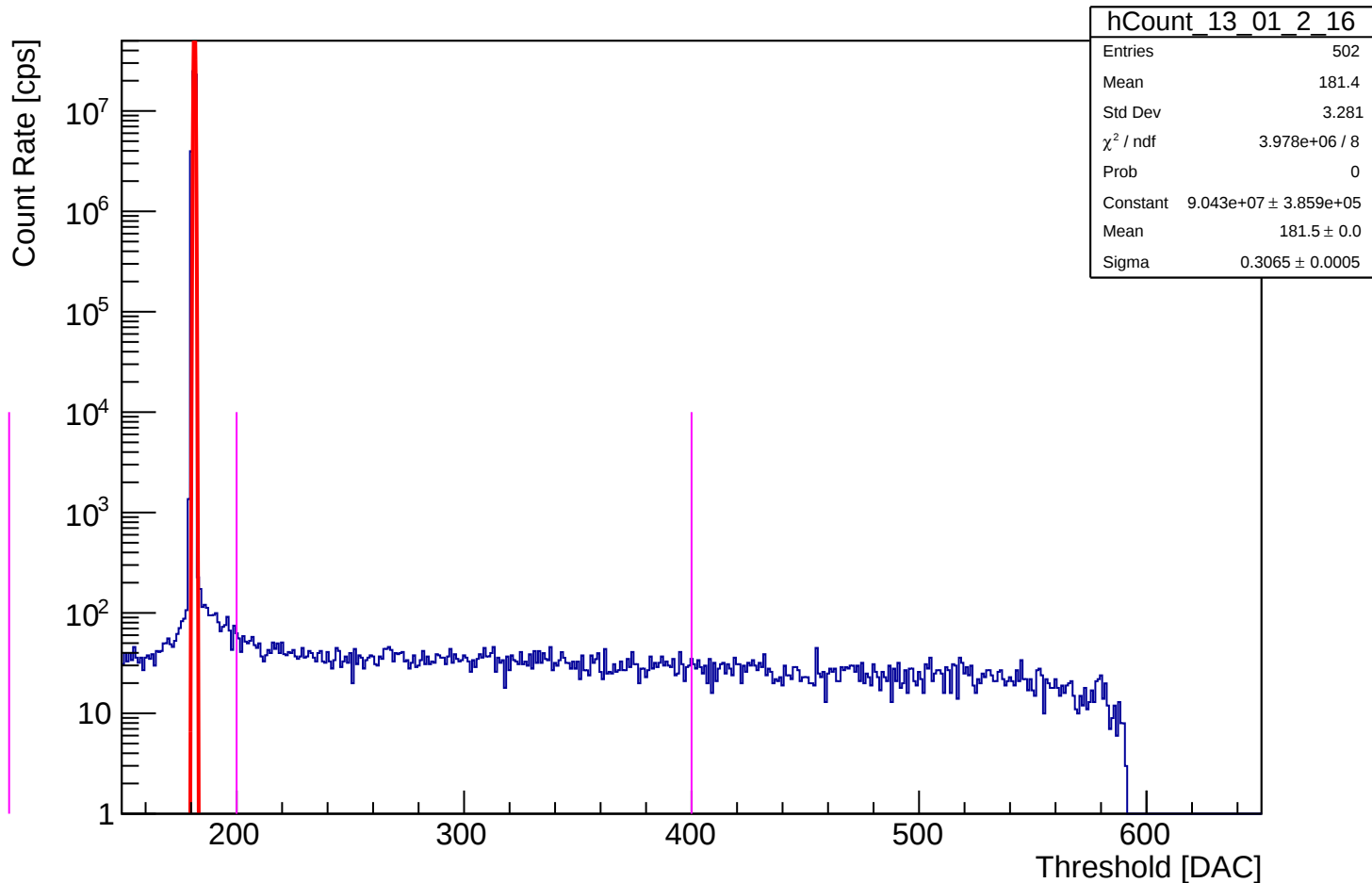
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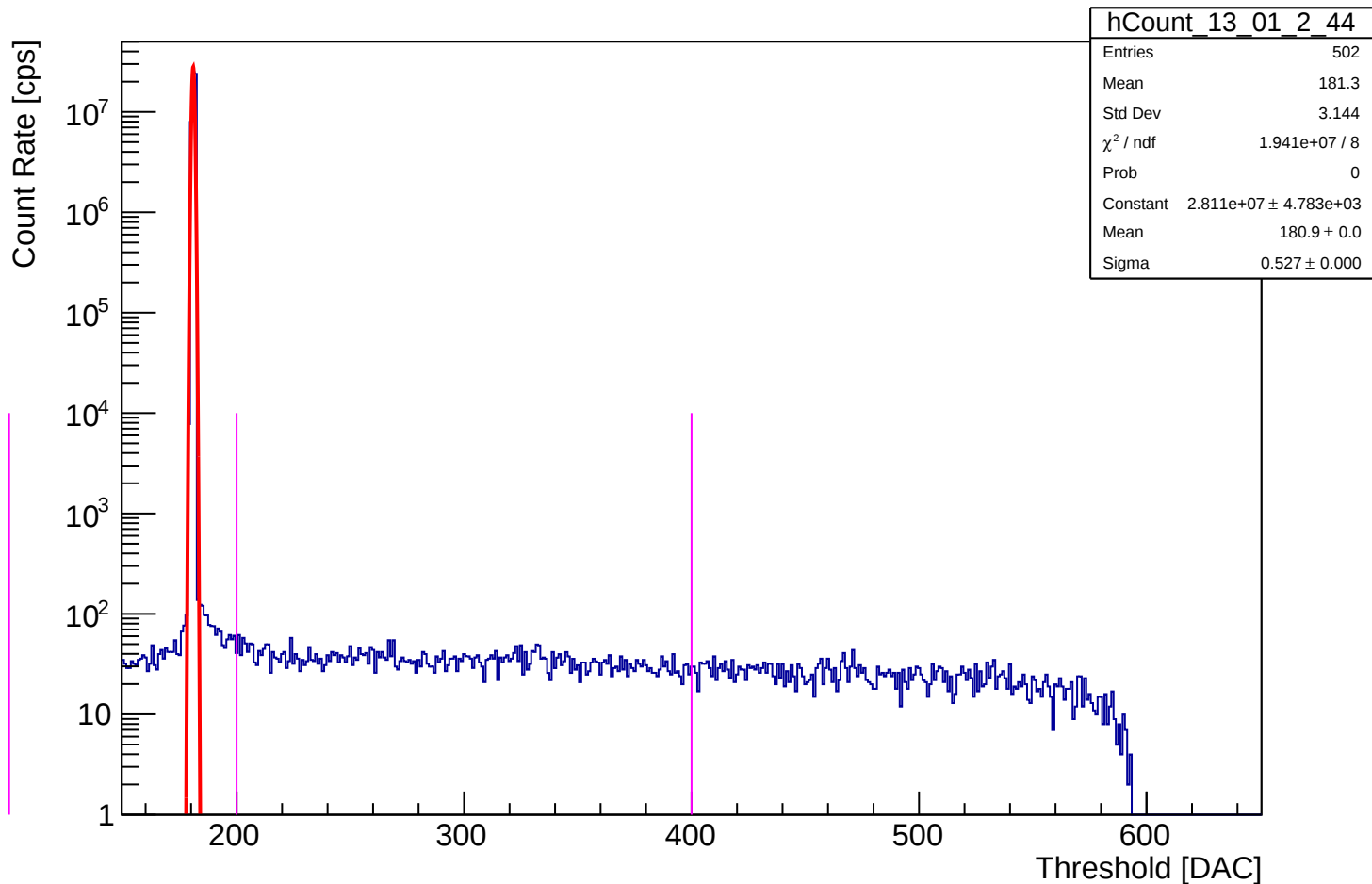
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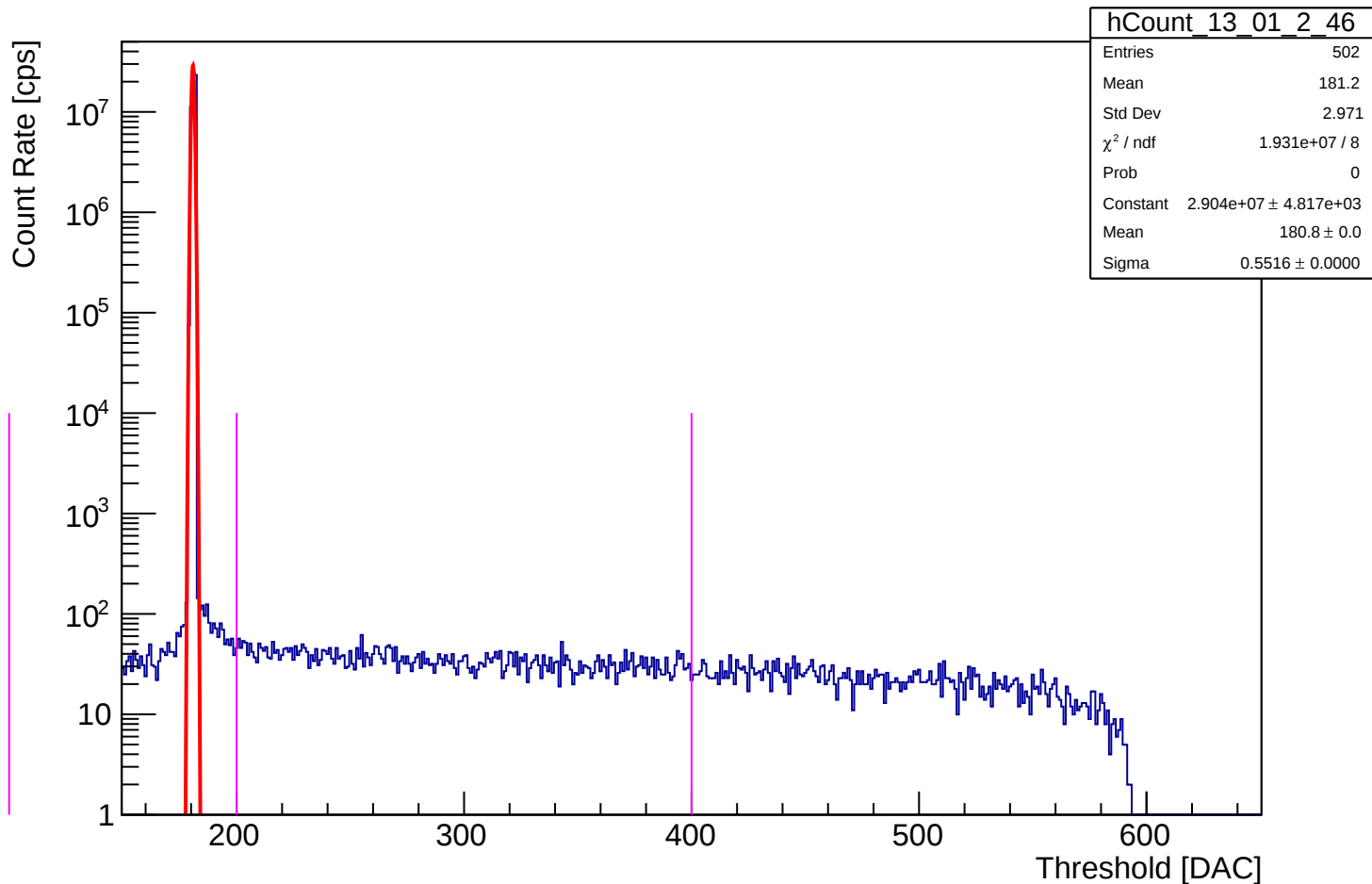
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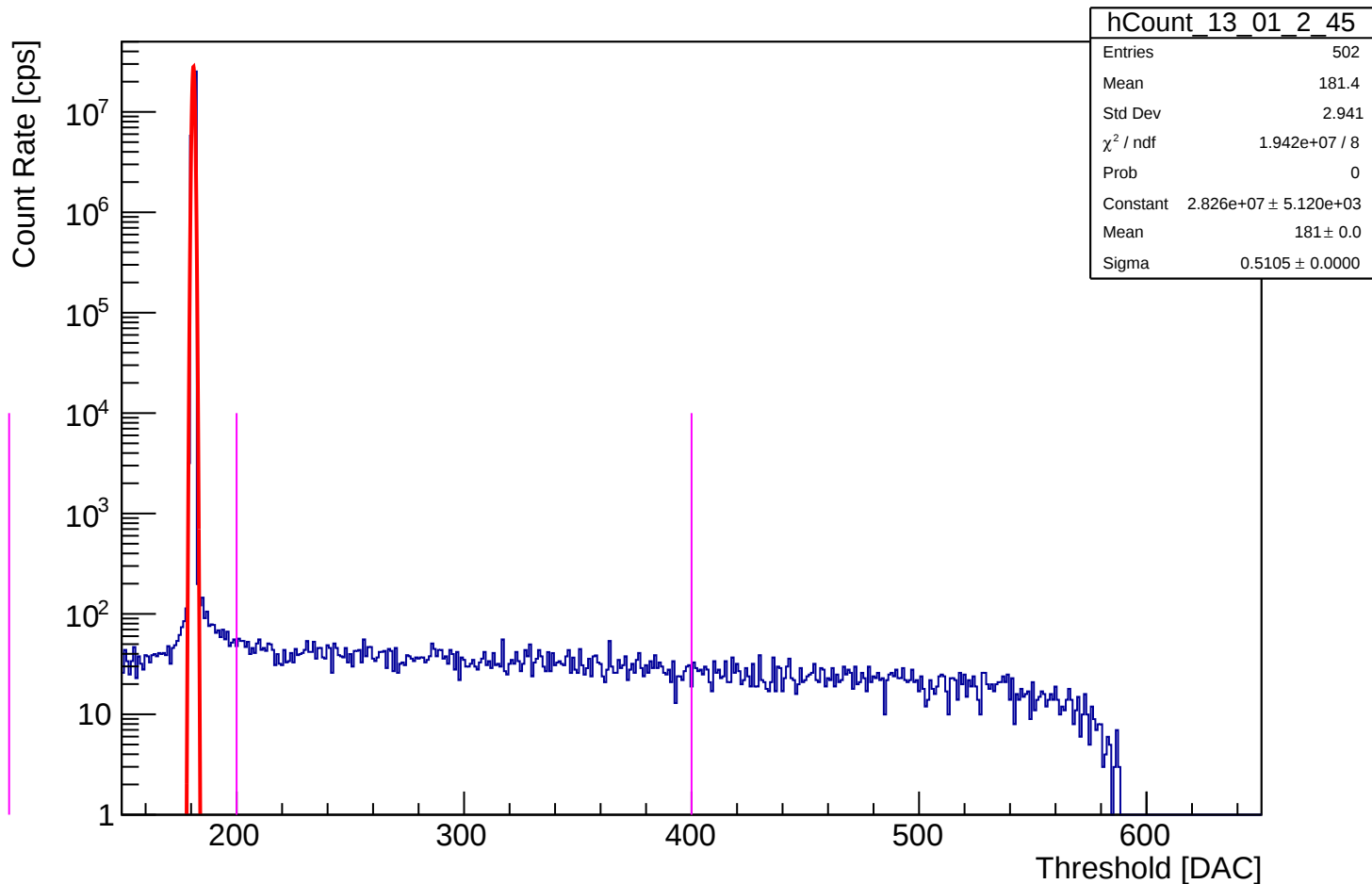
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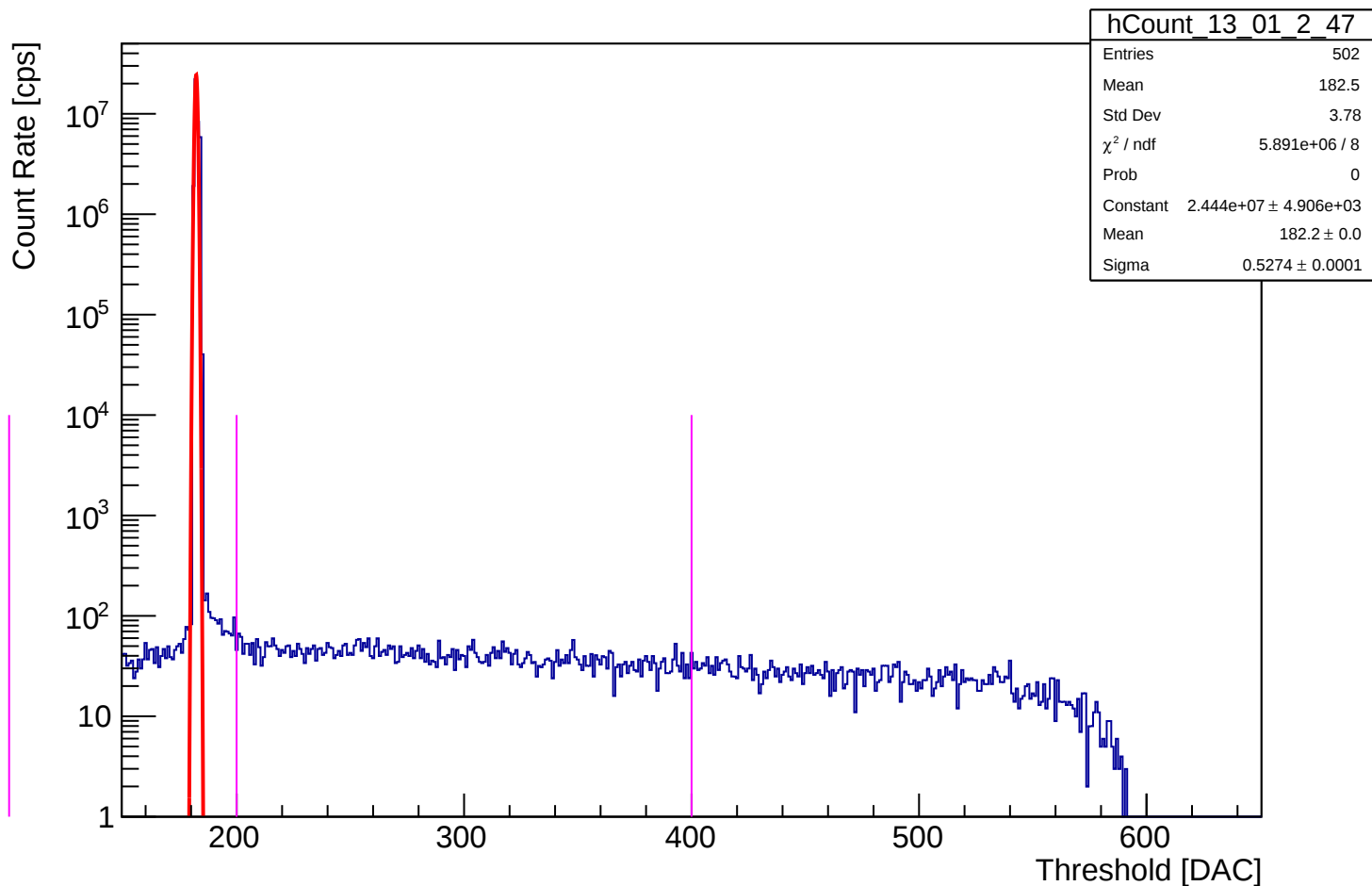
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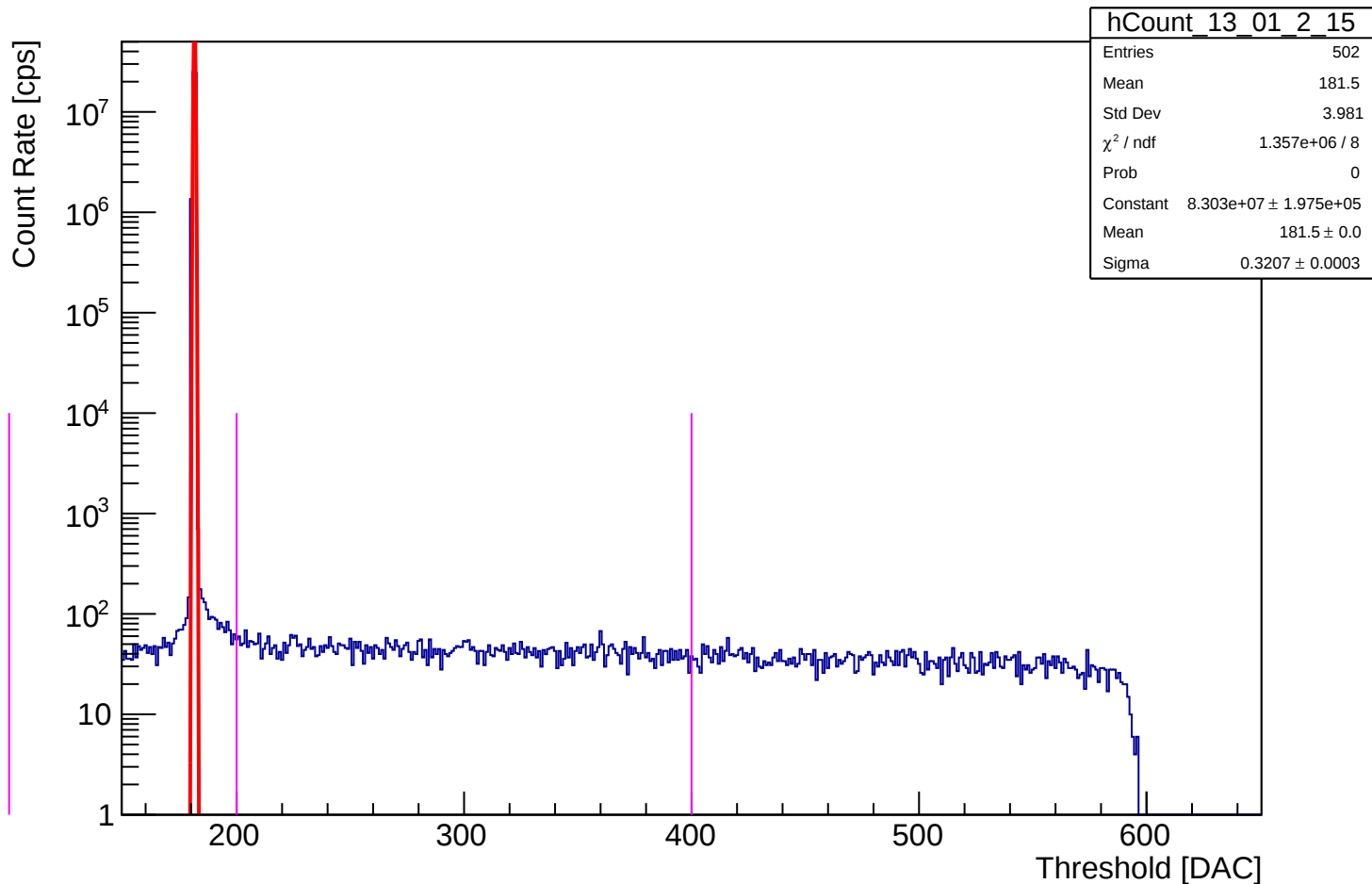
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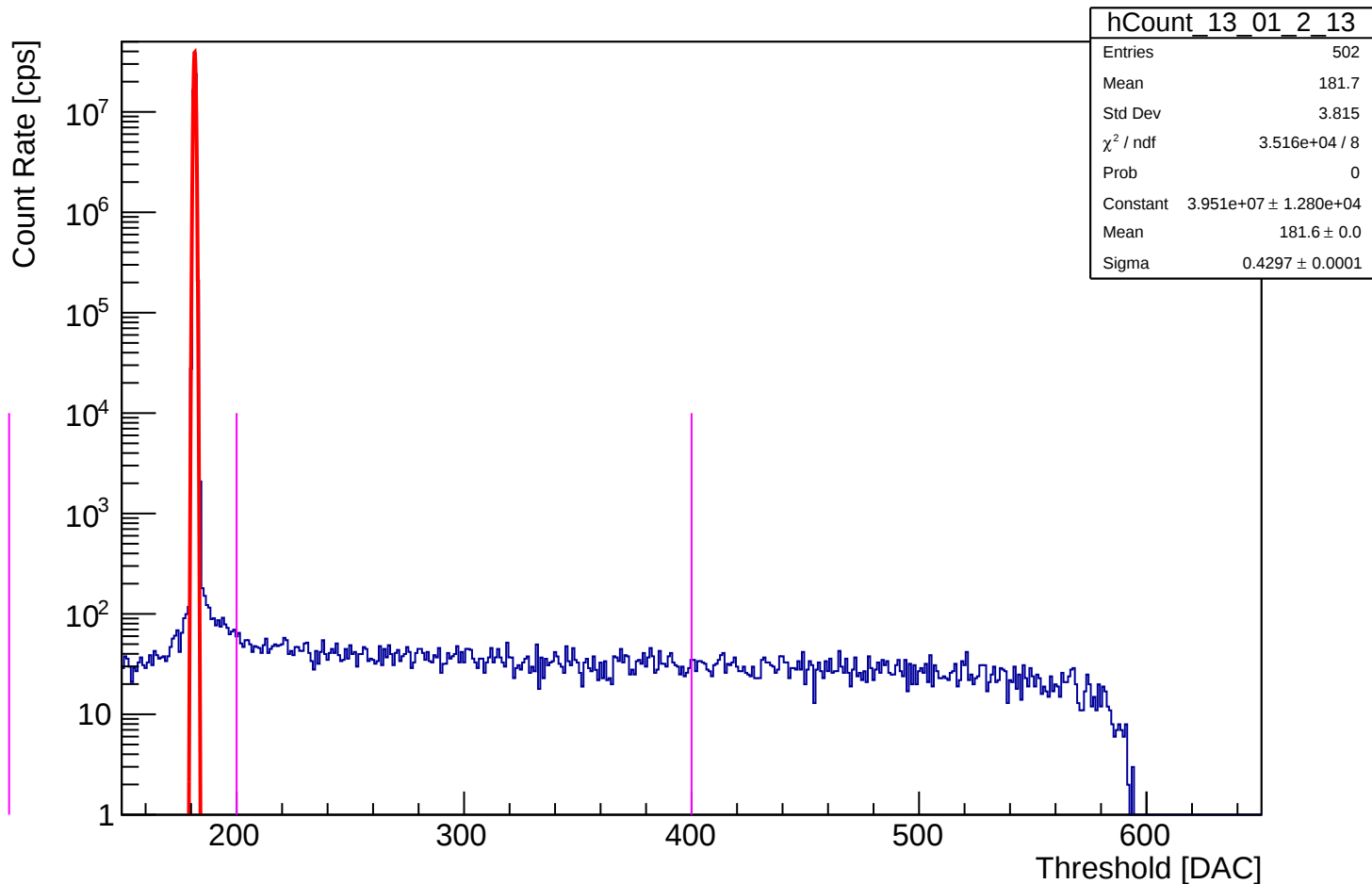
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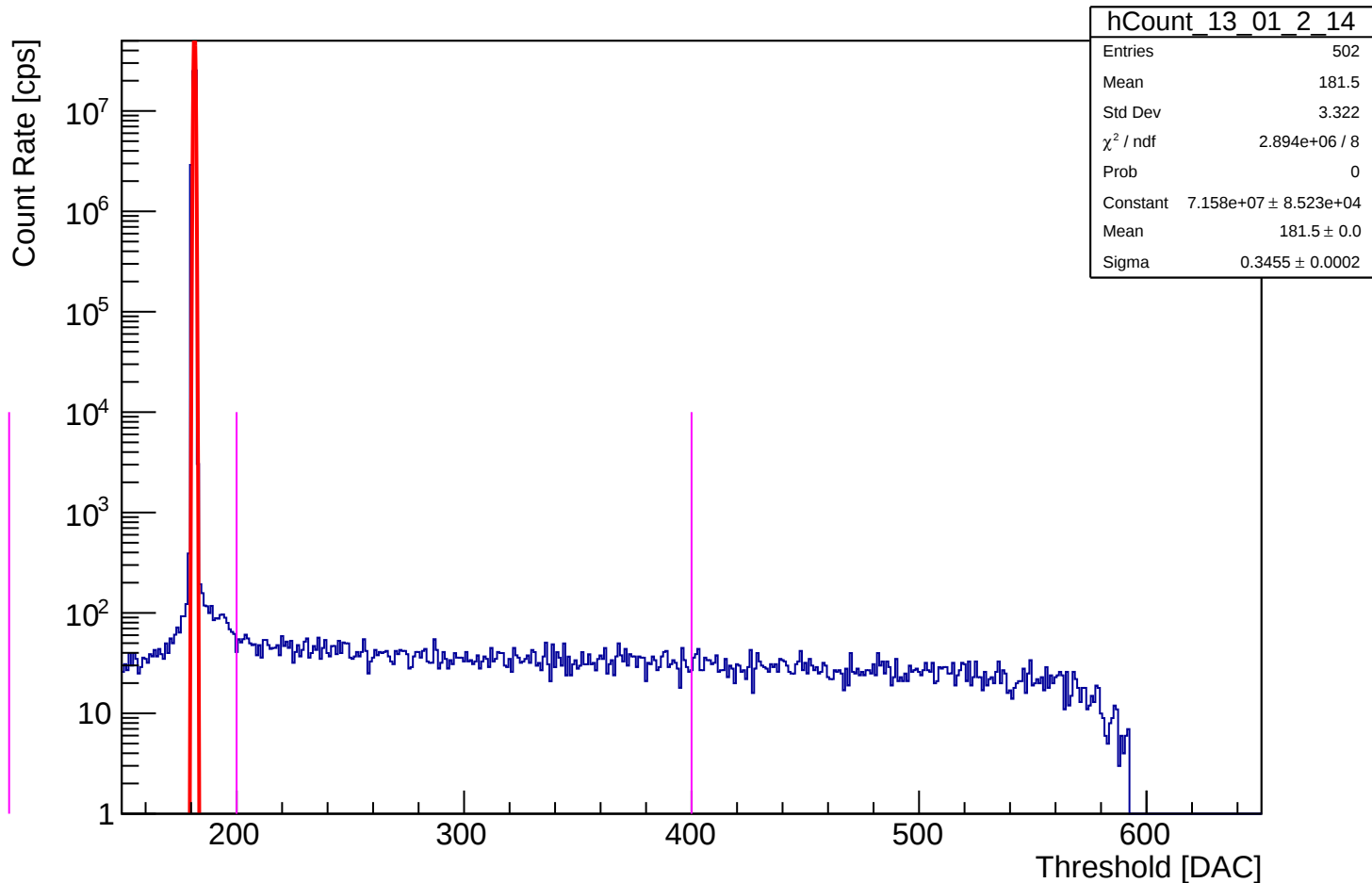
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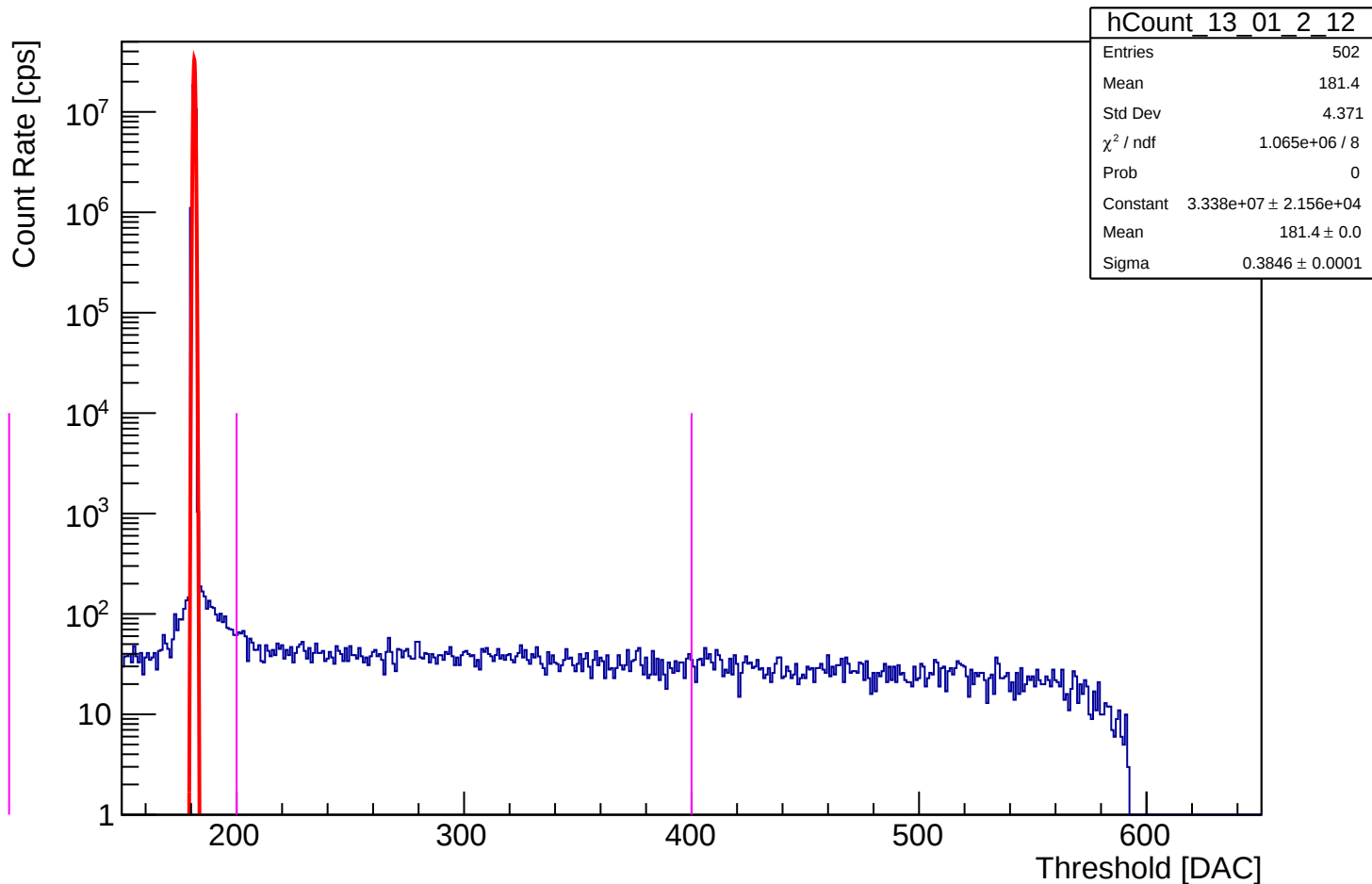
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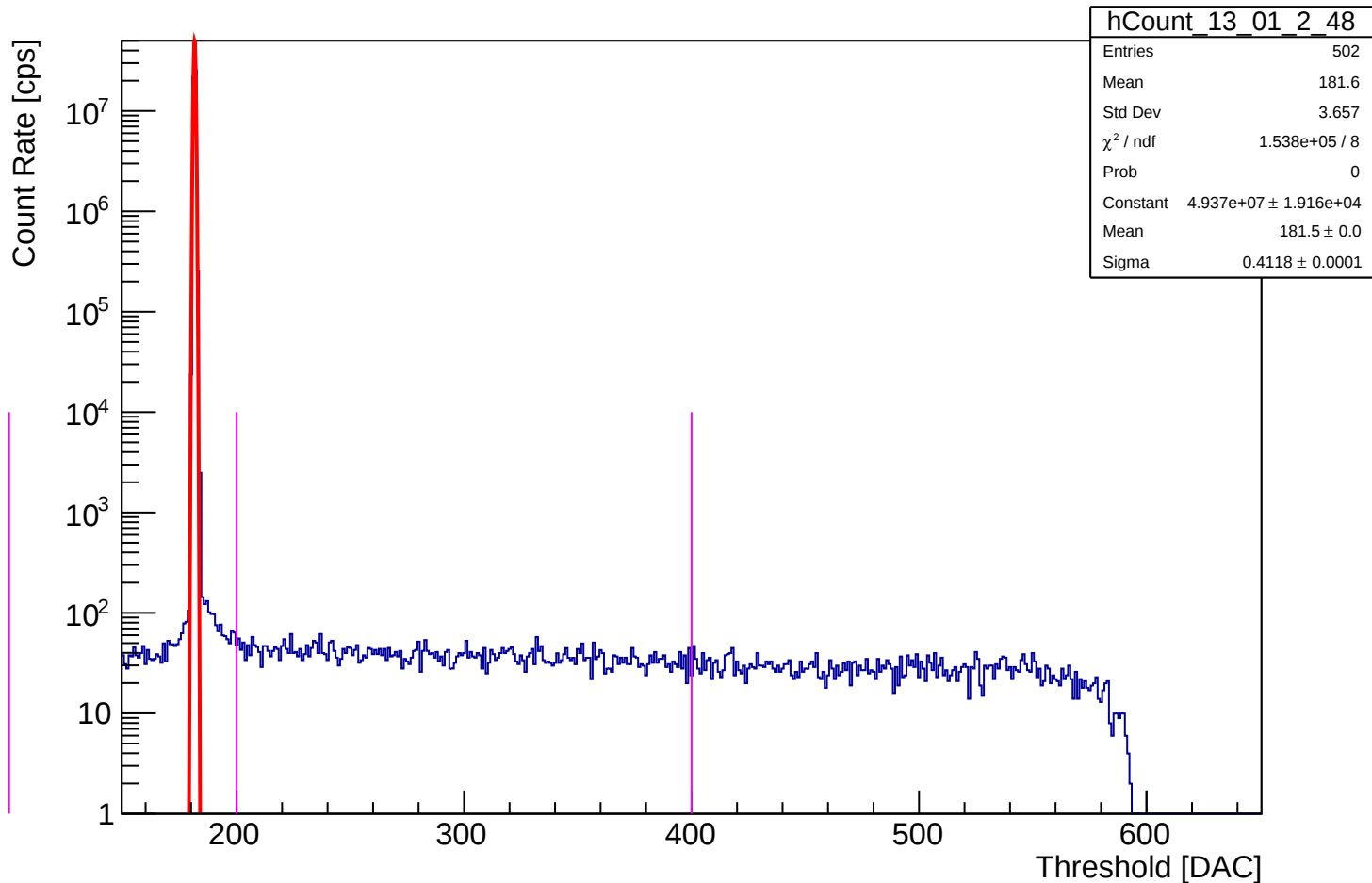
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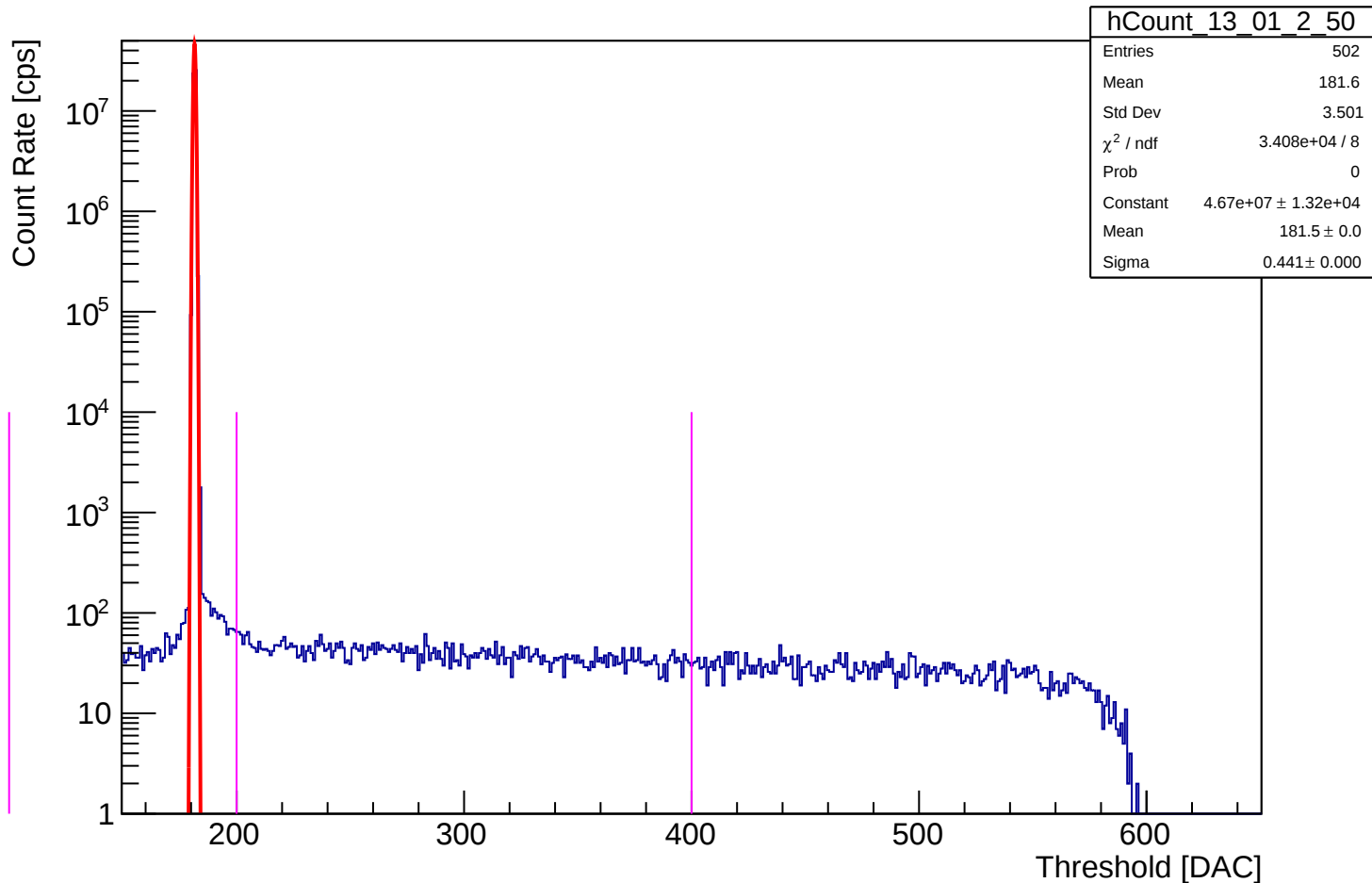
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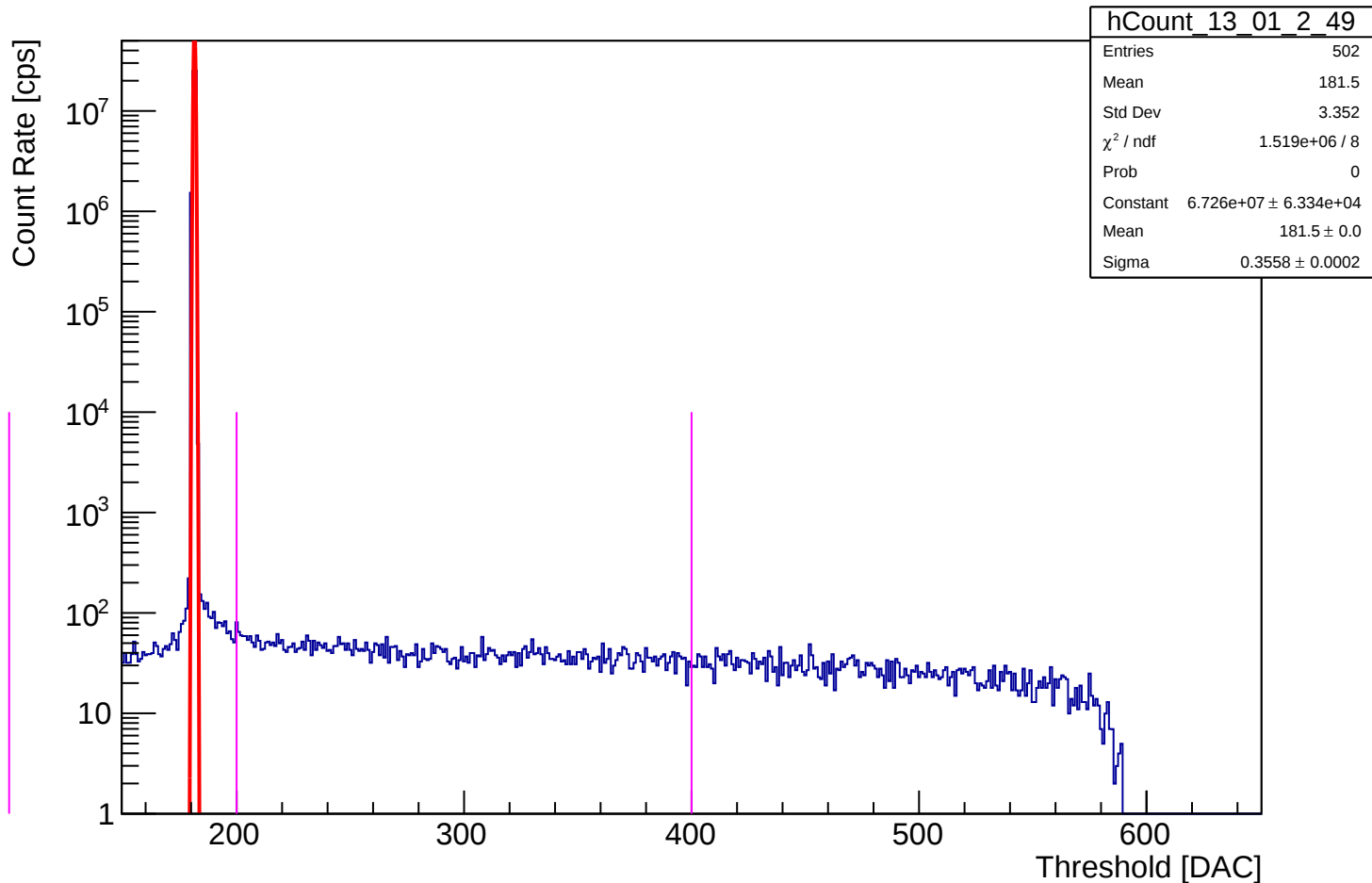
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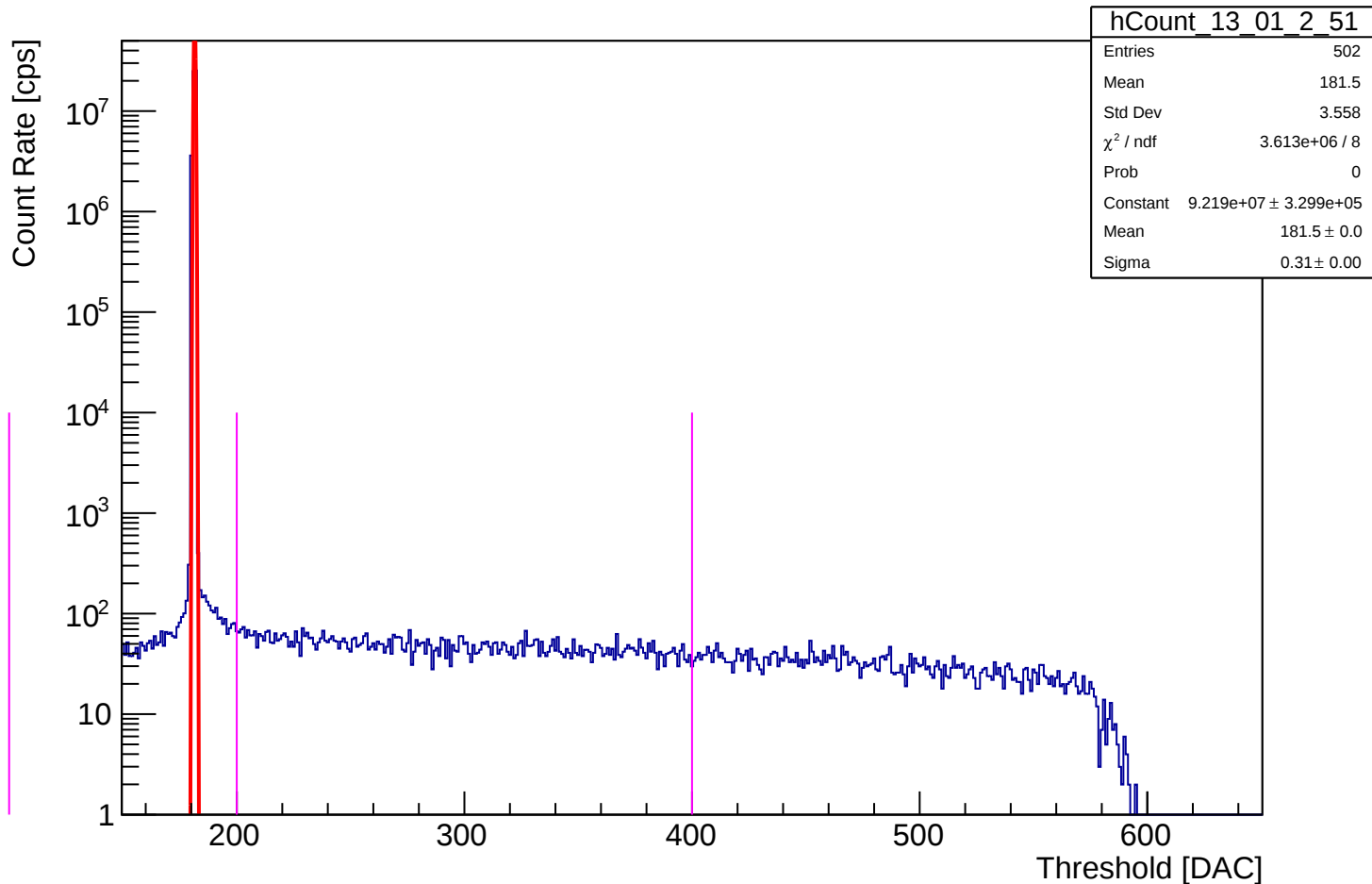
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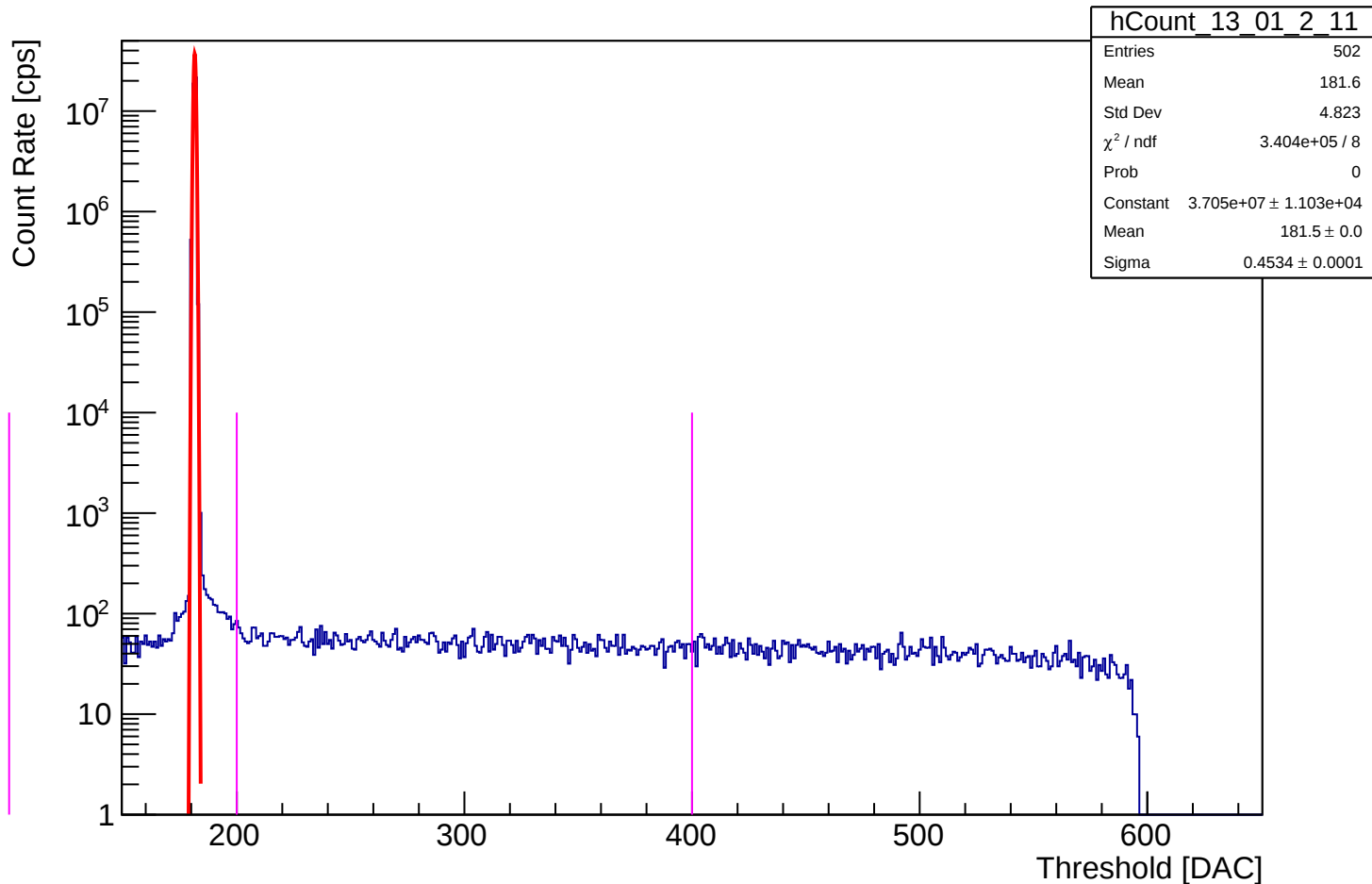
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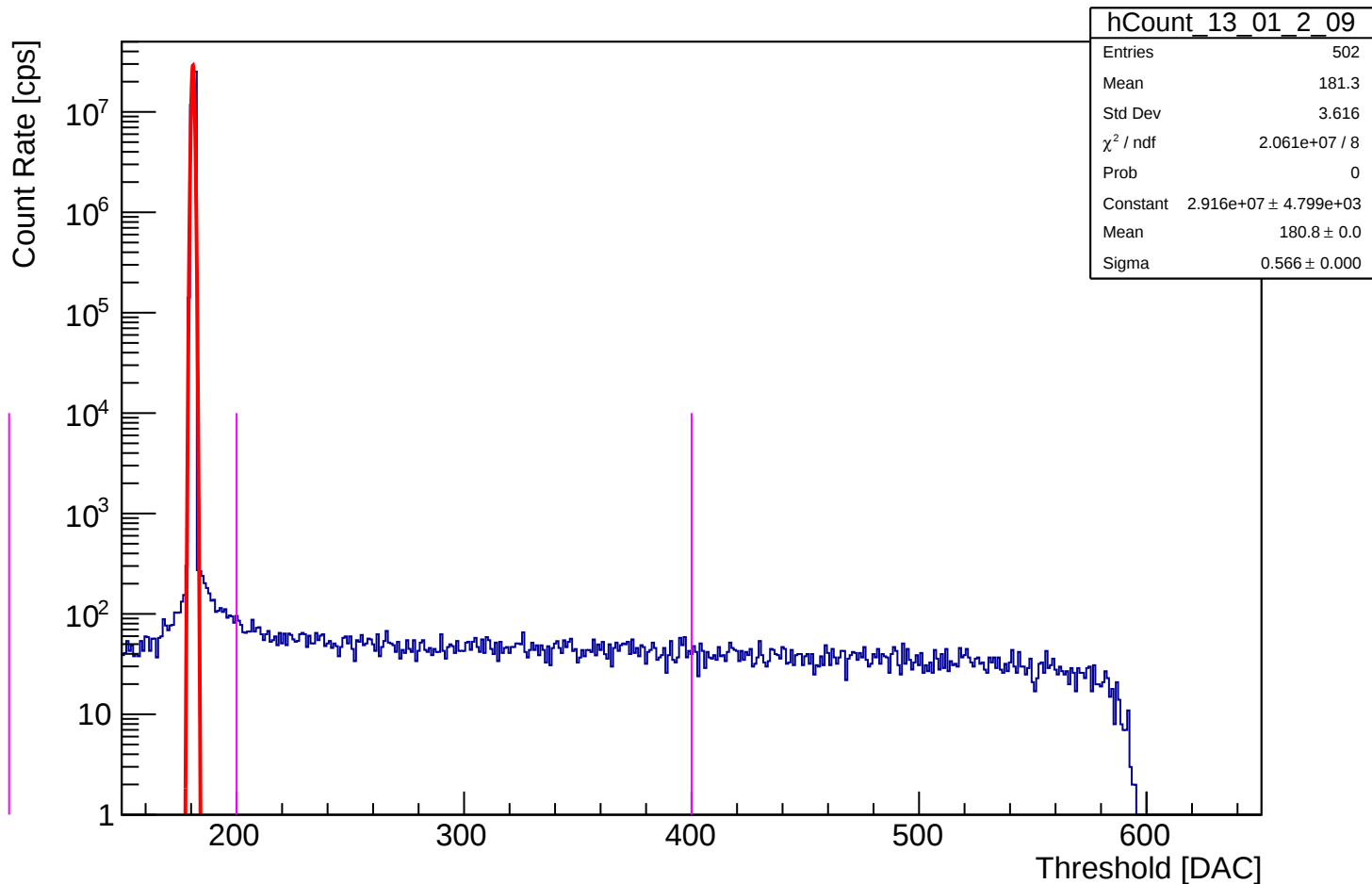
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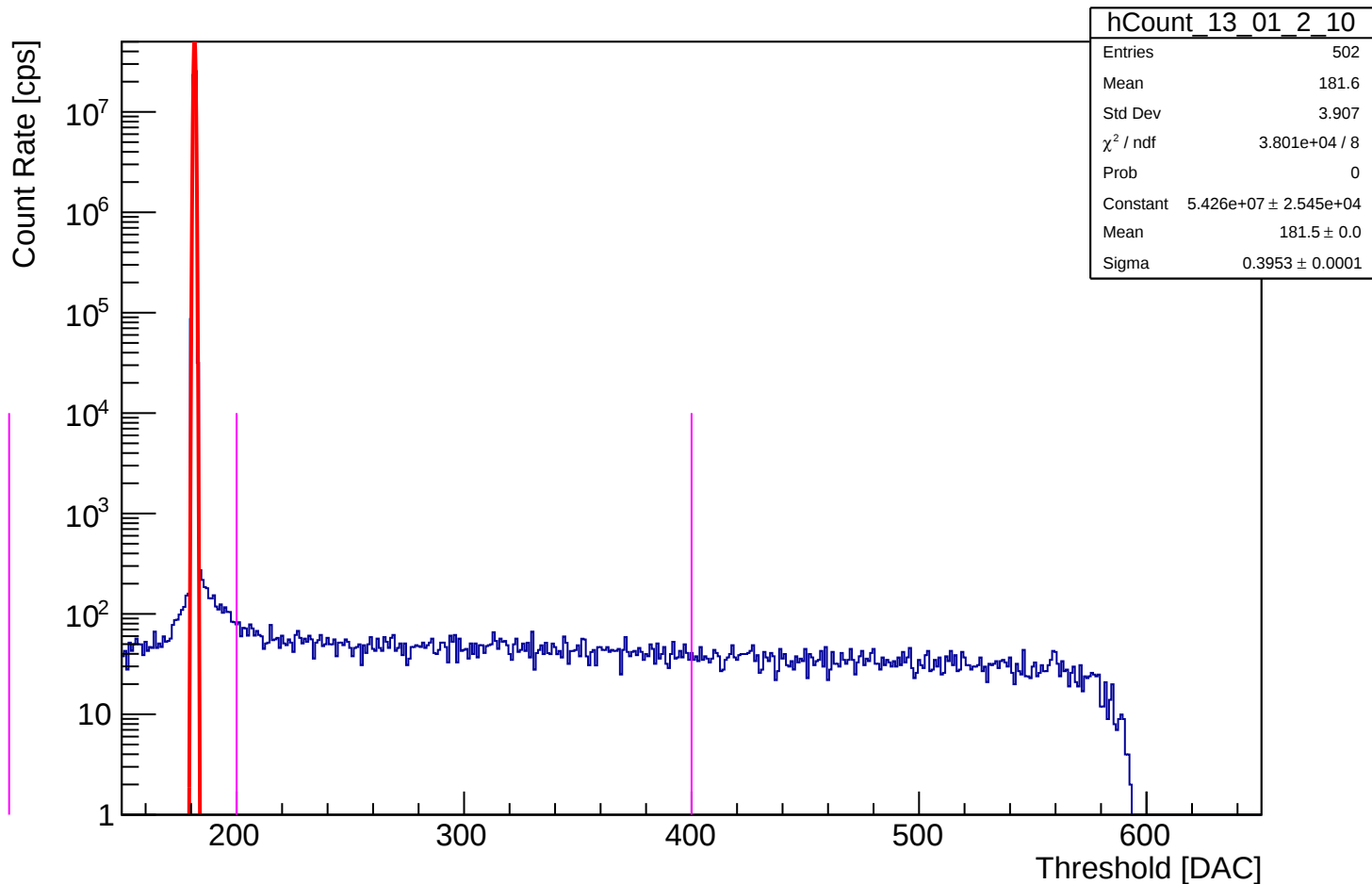
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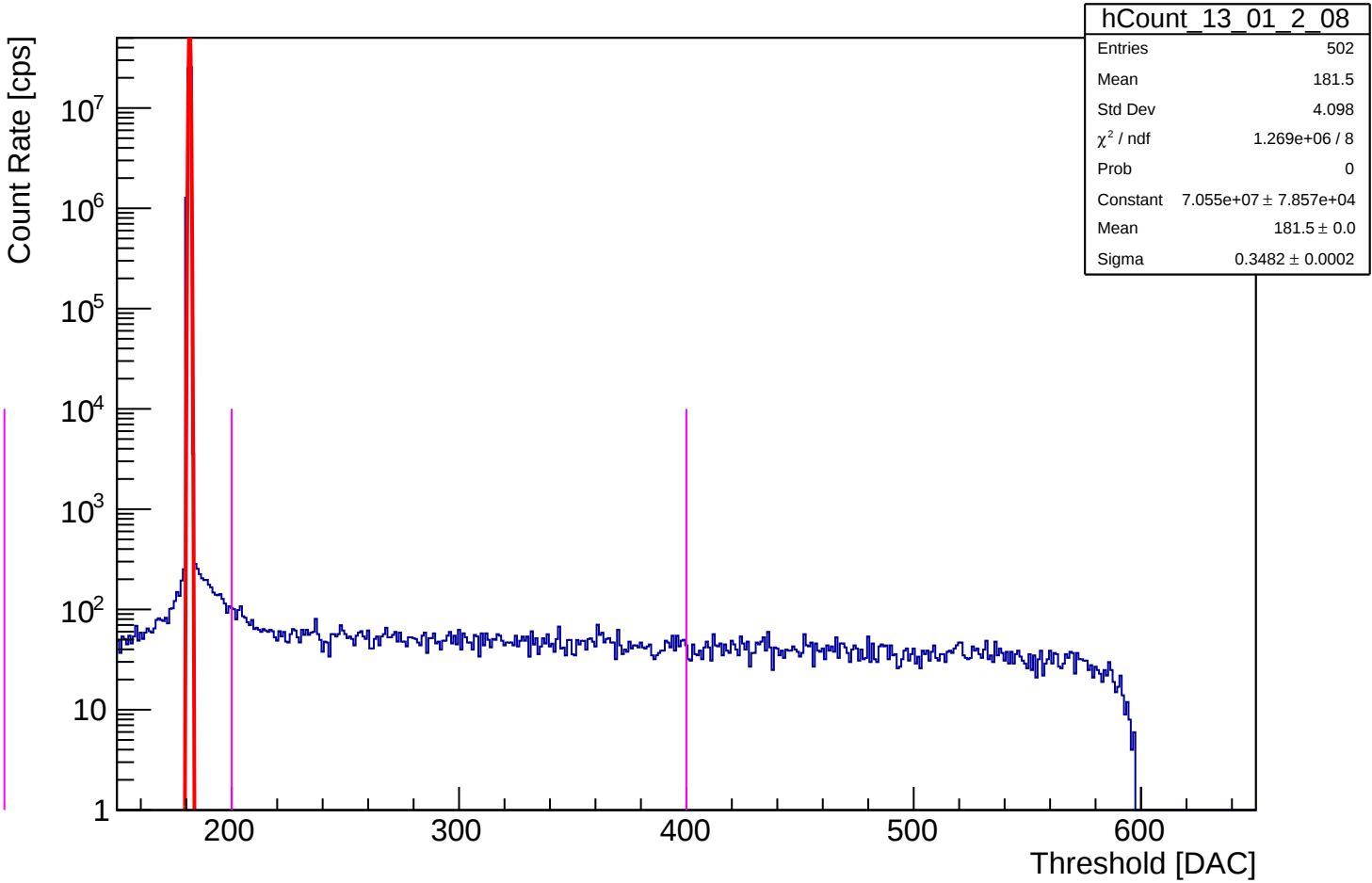


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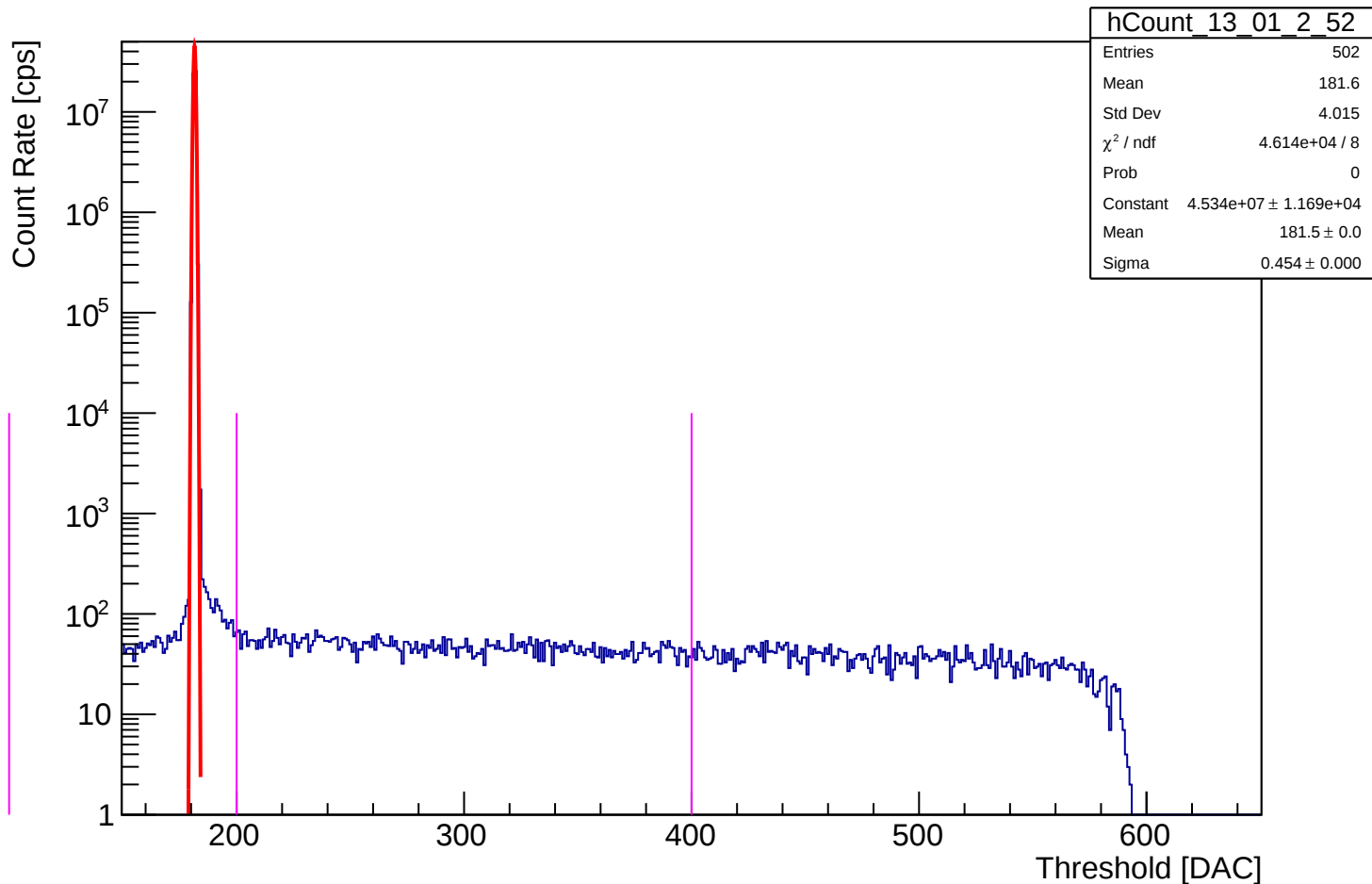


Row 1 Tile 1 Pmt 6 Pixel 43 Slot 13 Fiber 1 Asic 2 Channel 10

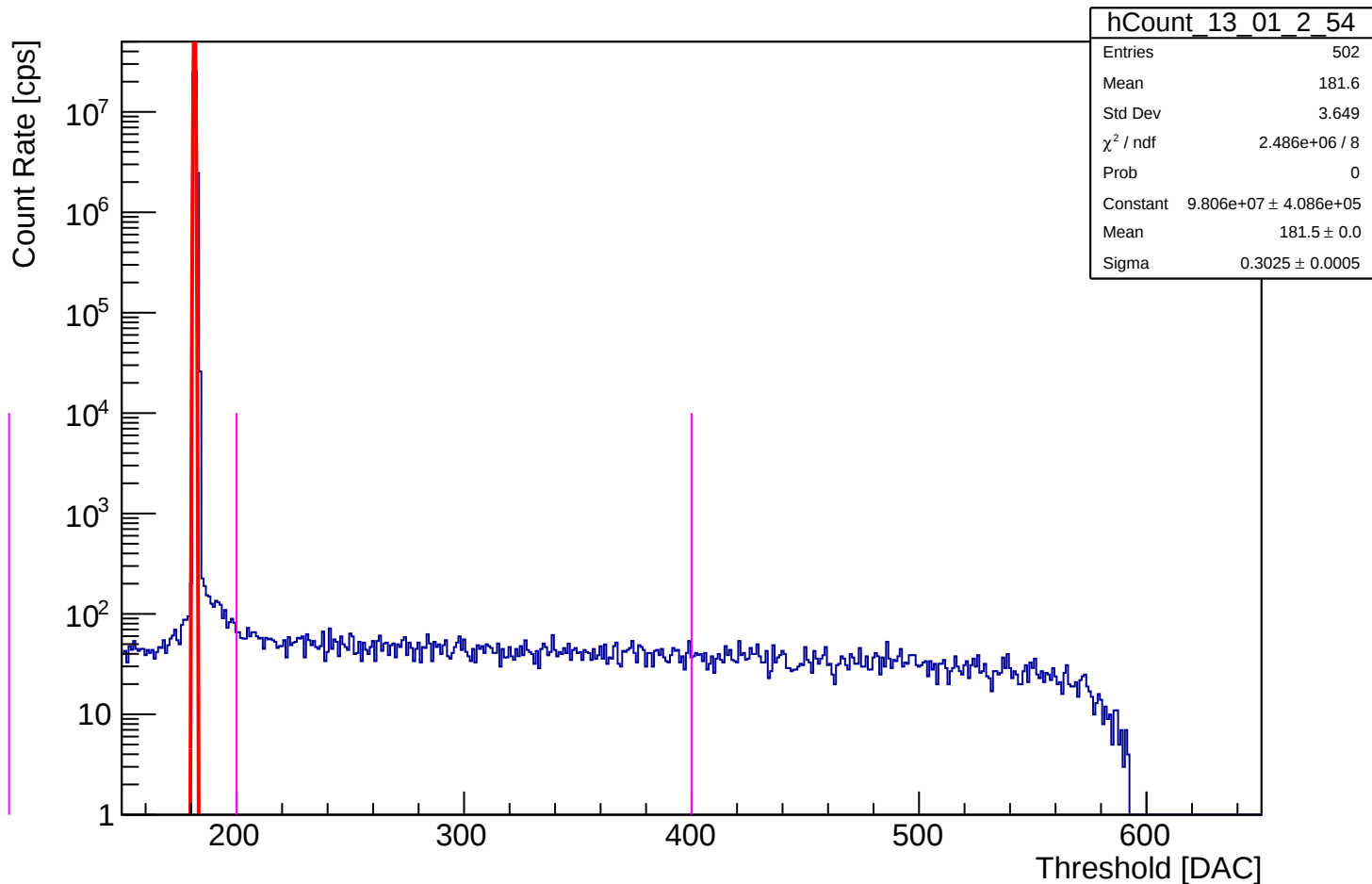




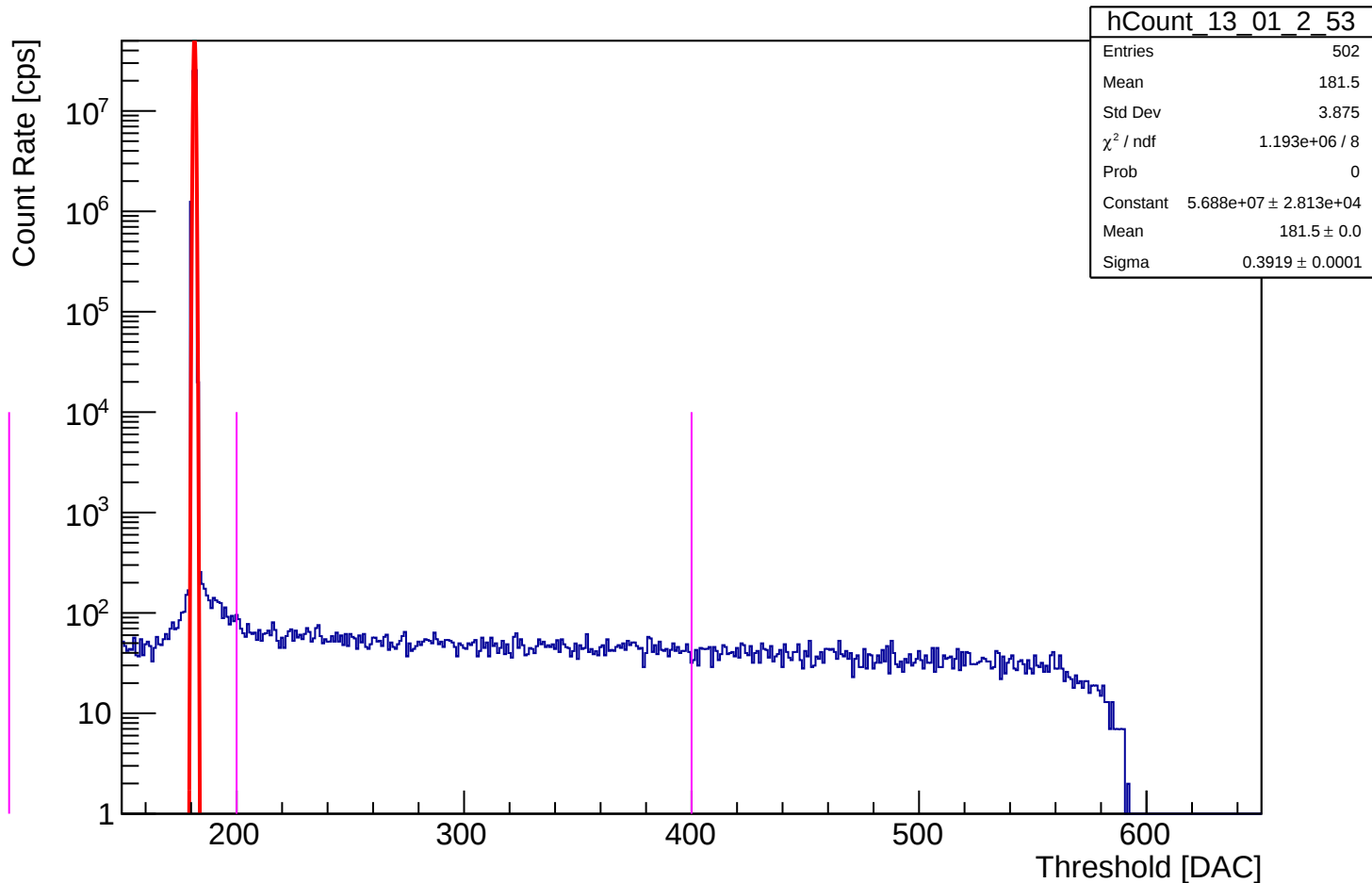
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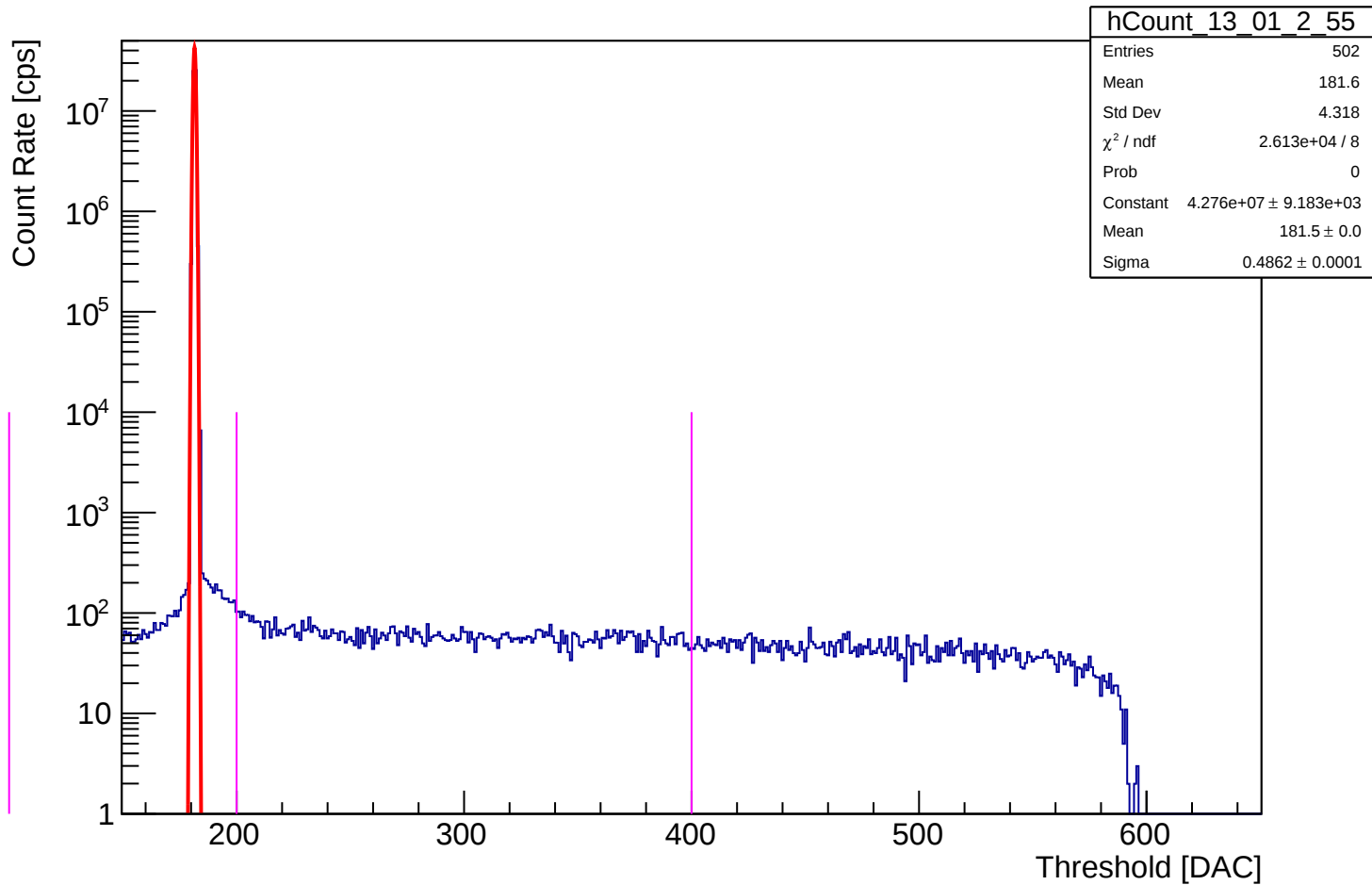
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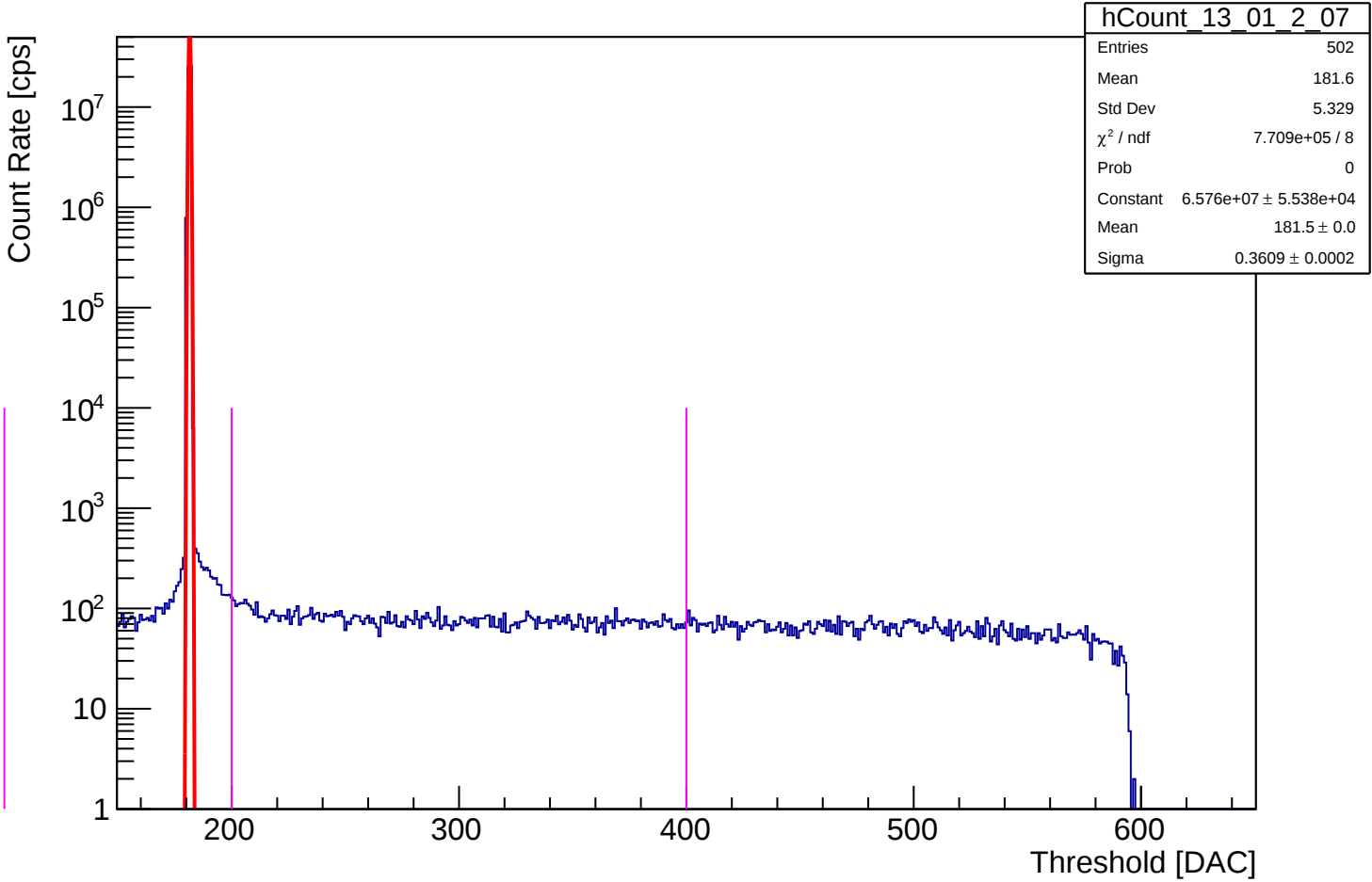


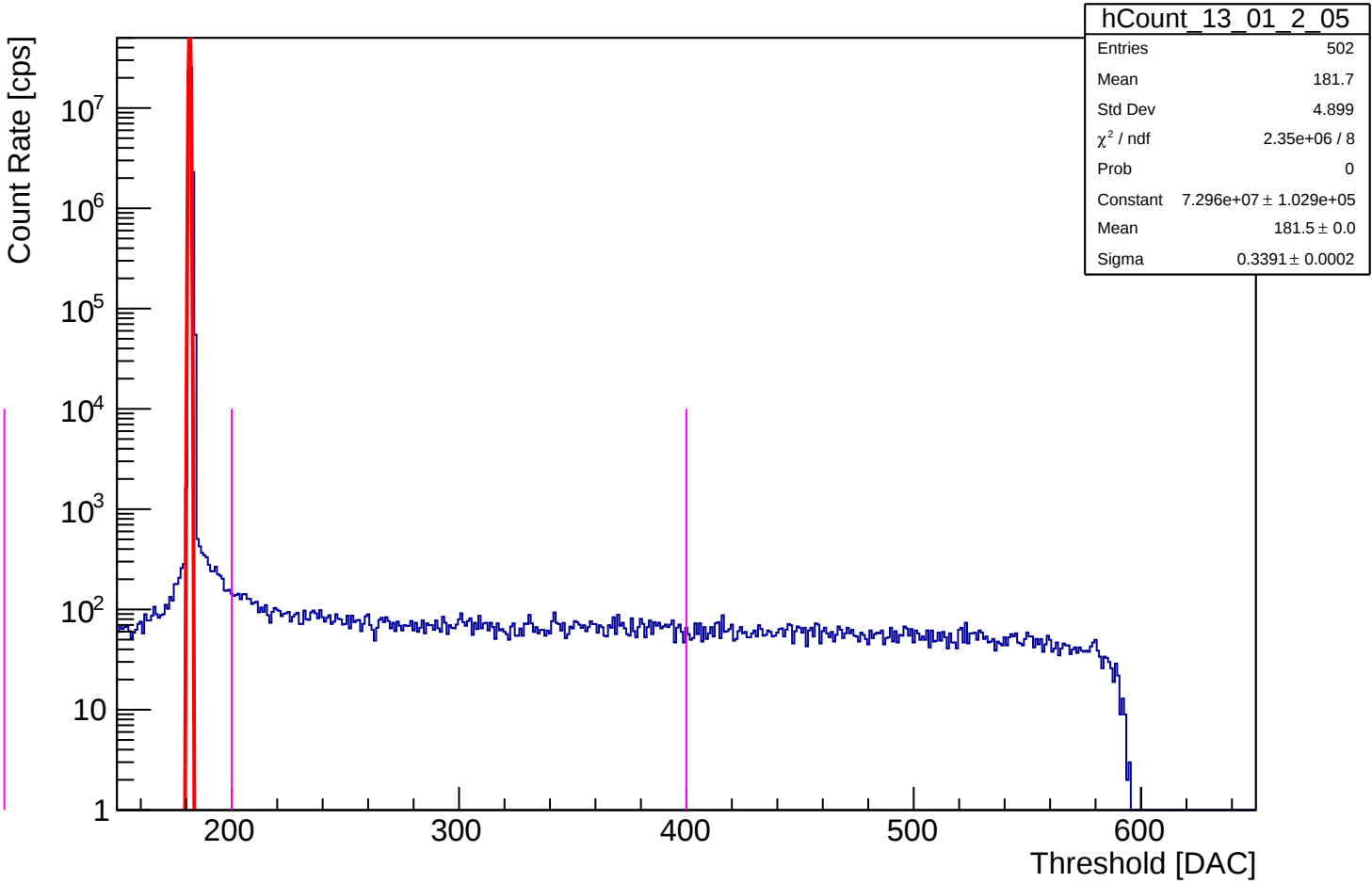
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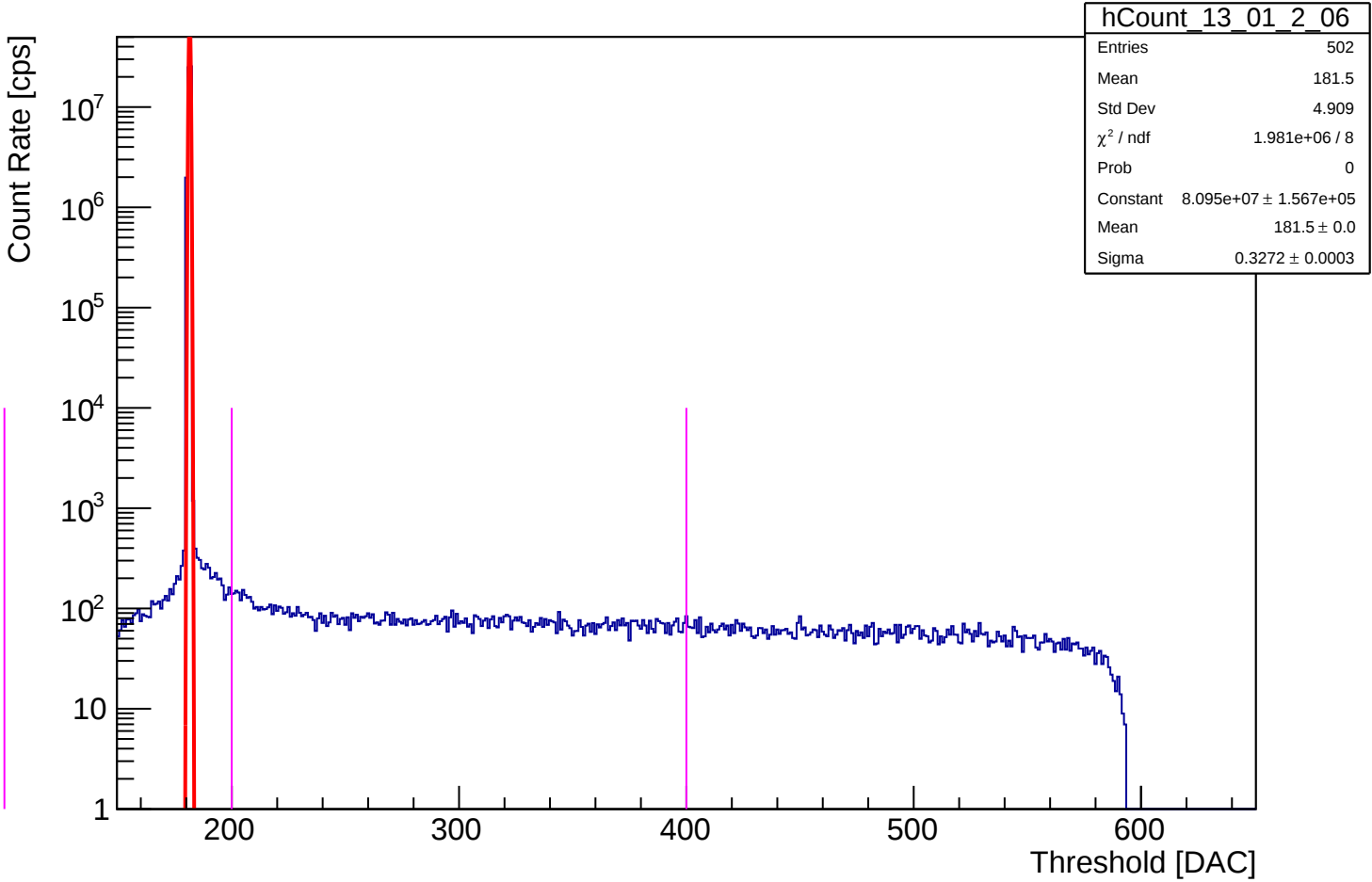


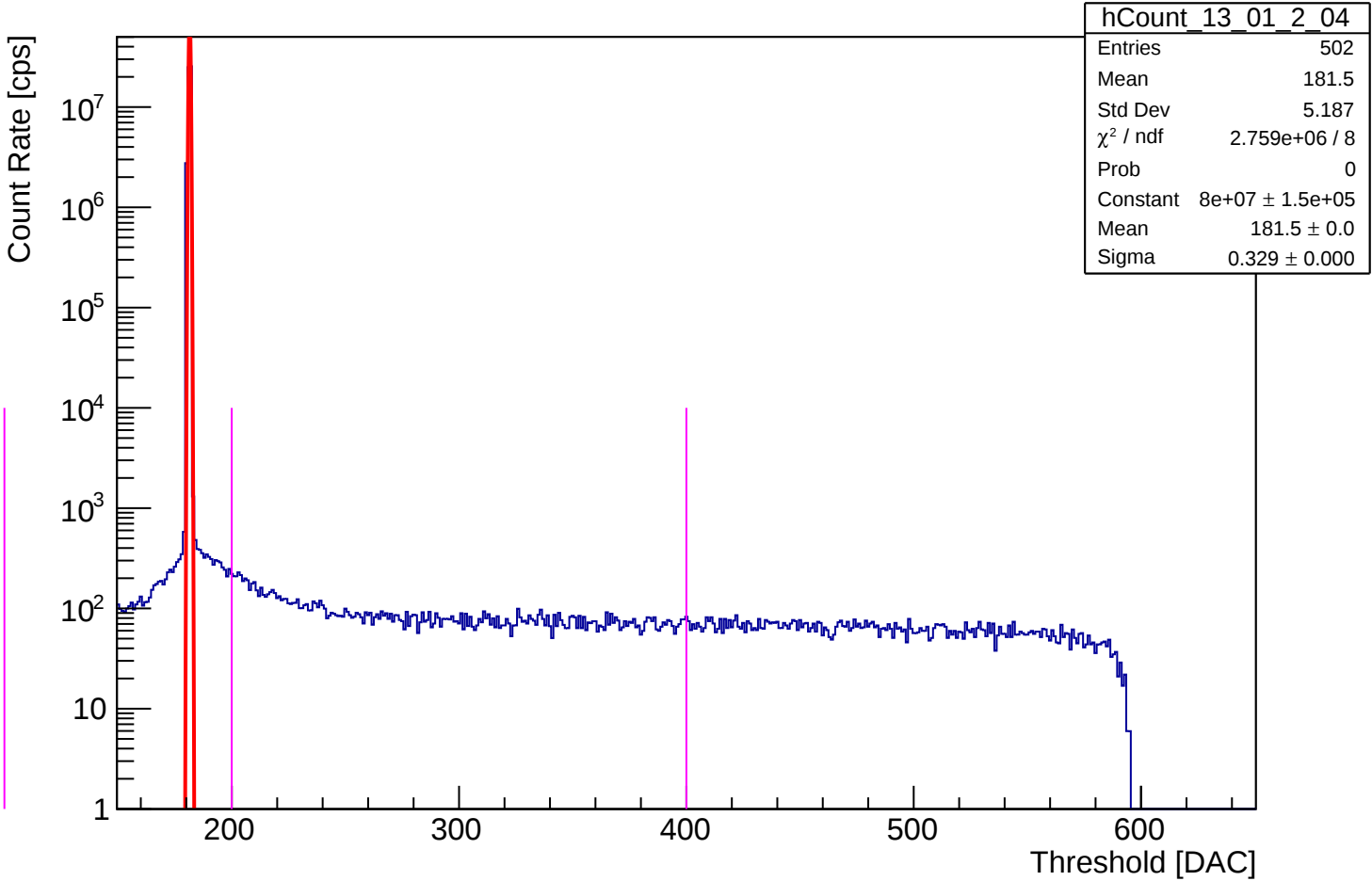
Row 1 Tile 1 Pmt 6 Pixel 48 Slot 13 Fiber 1 Asic 2 Channel 55



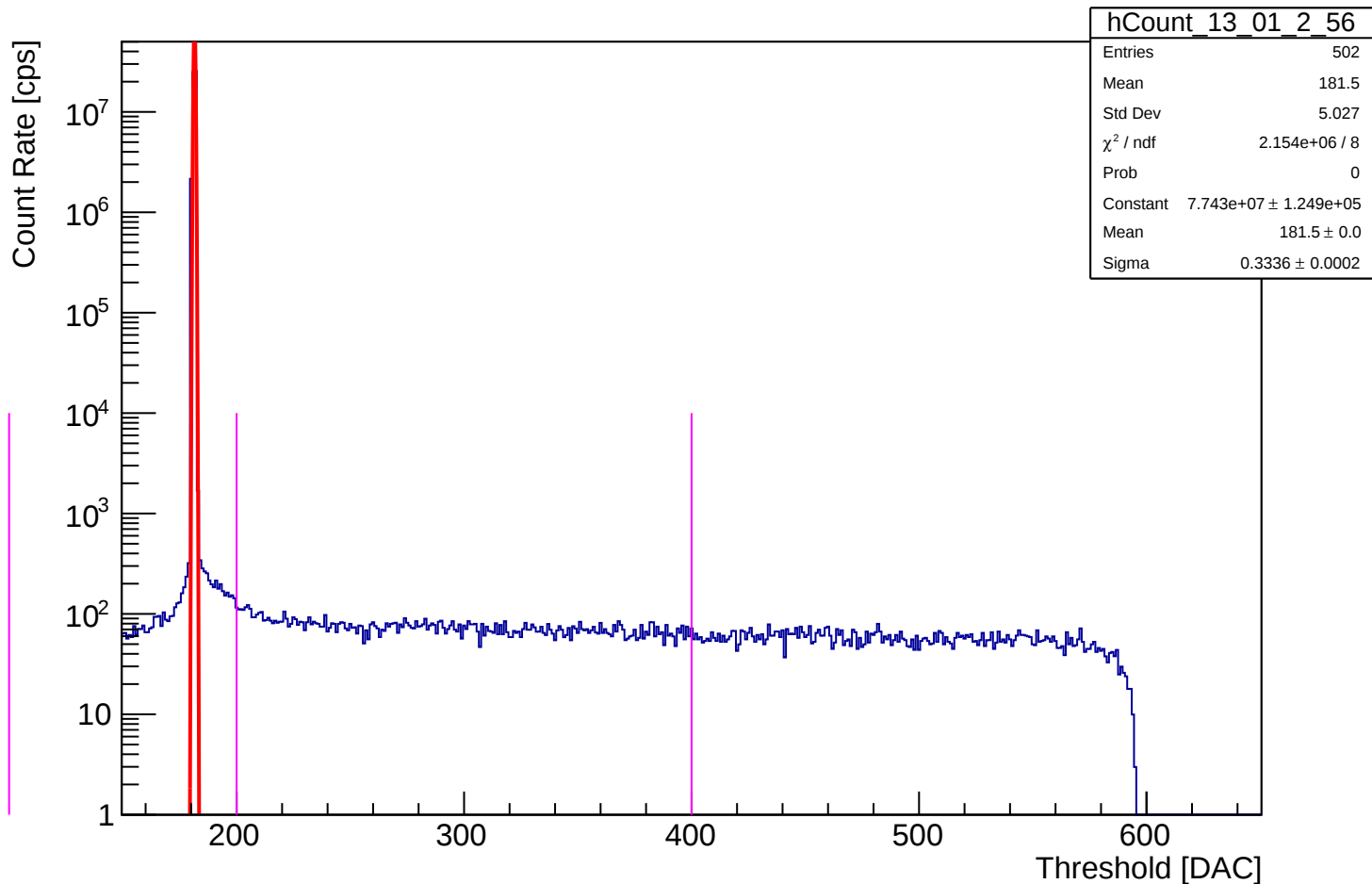




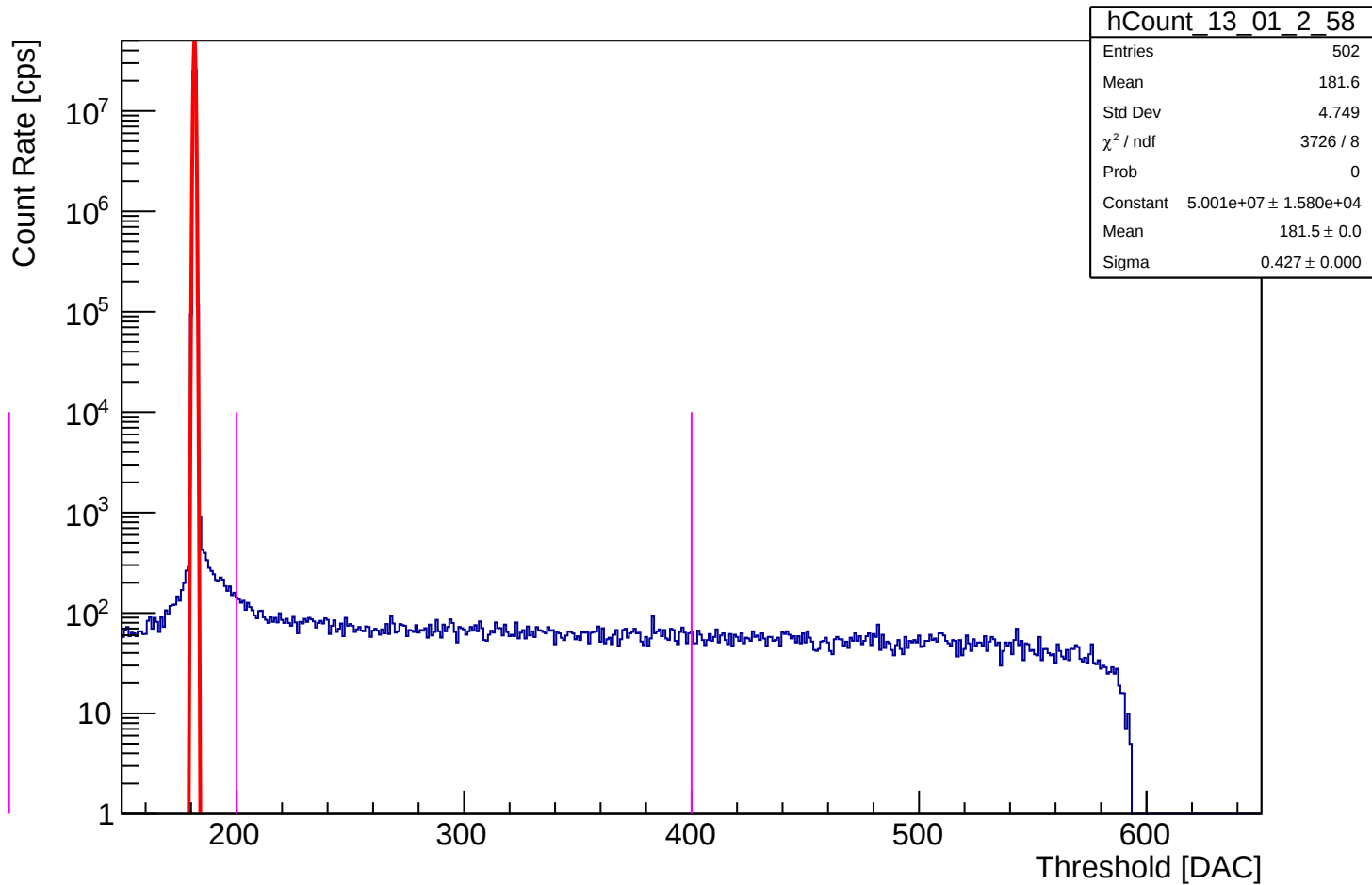




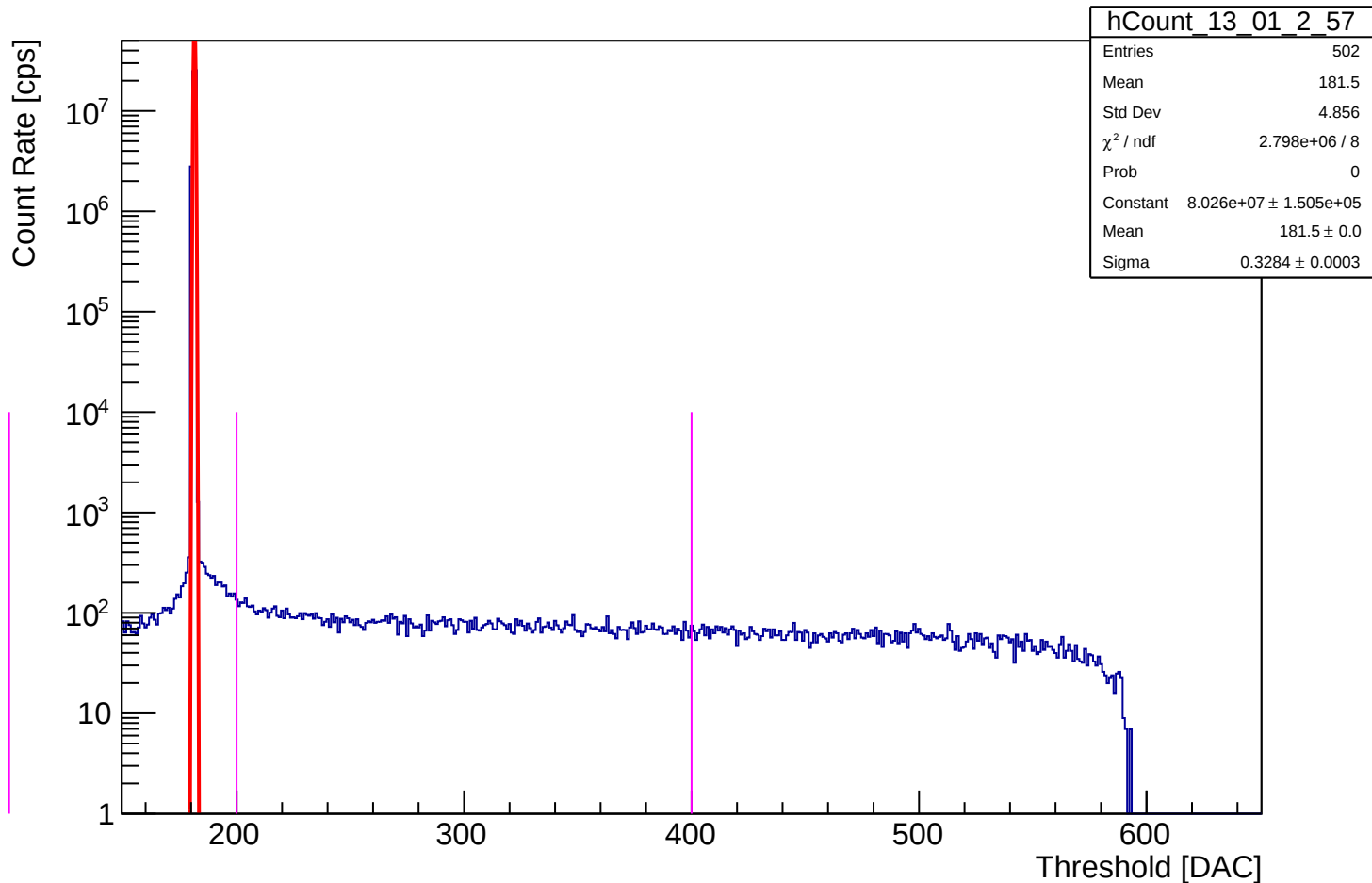
Row 1 Tile 1 Pmt 6 Pixel 53 Slot 13 Fiber 1 Asic 2 Channel 56



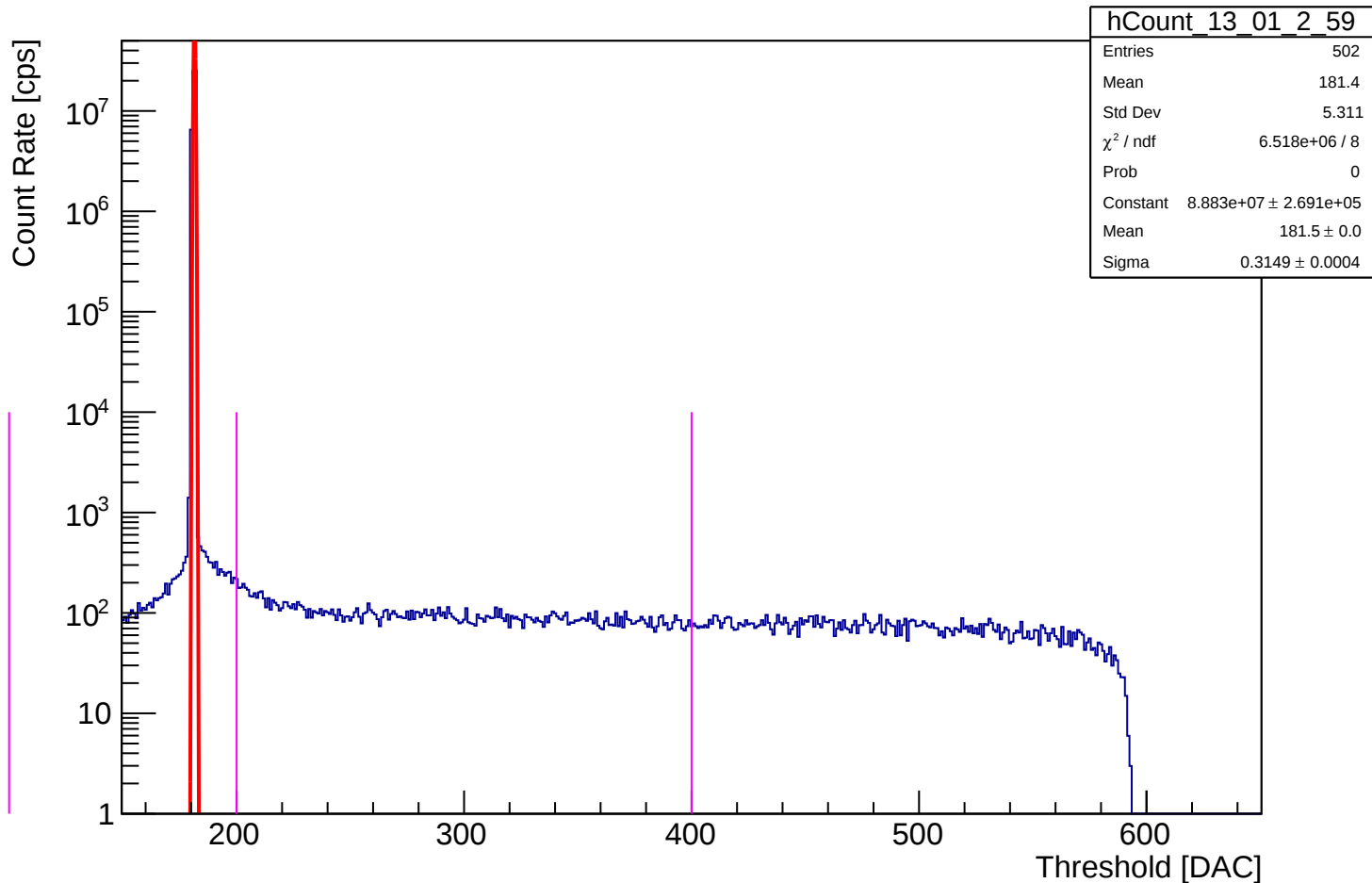
Row 1 Tile 1 Pmt 6 Pixel 54 Slot 13 Fiber 1 Asic 2 Channel 58

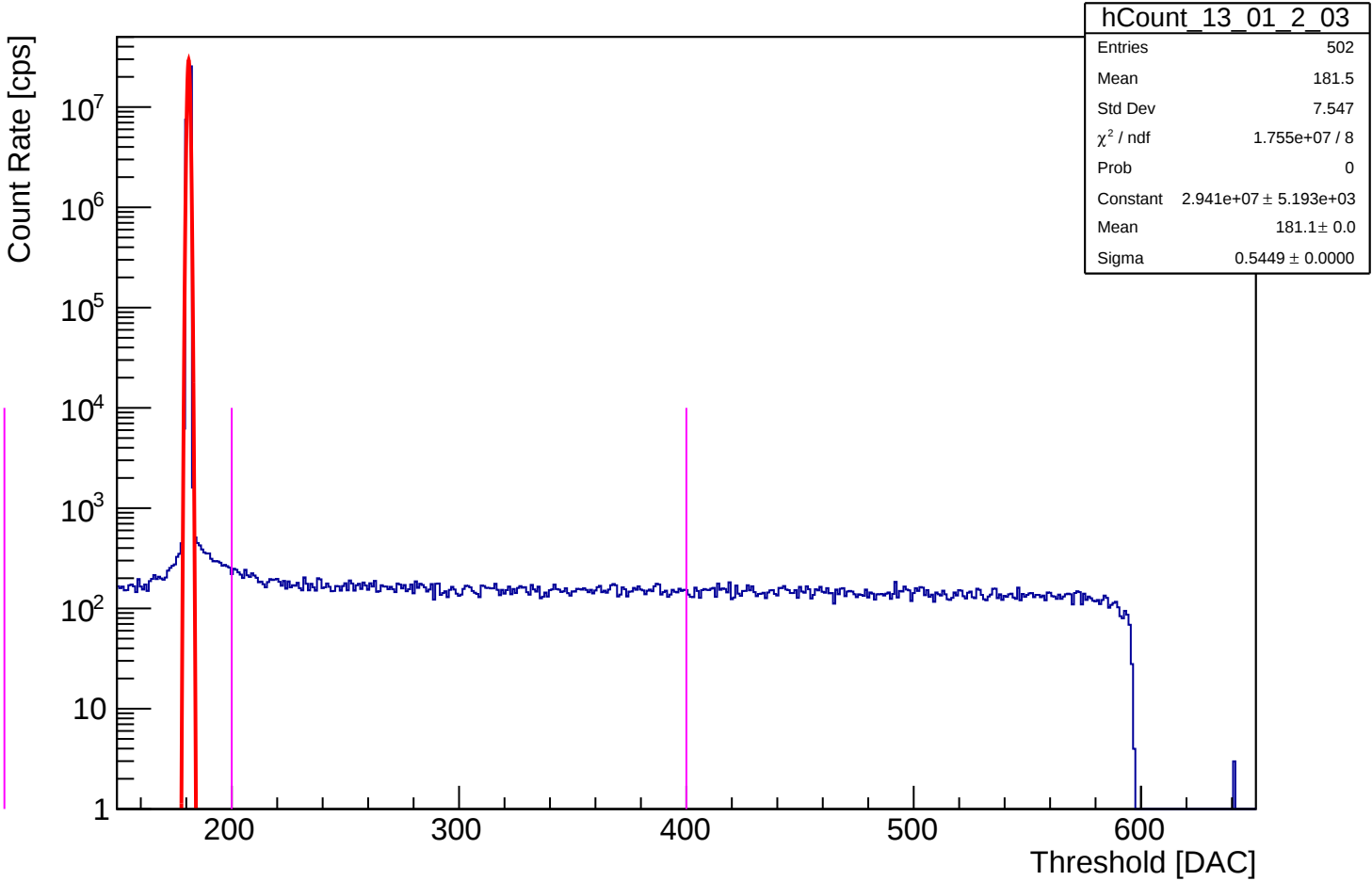


Row 1 Tile 1 Pmt 6 Pixel 55 Slot 13 Fiber 1 Asic 2 Channel 57

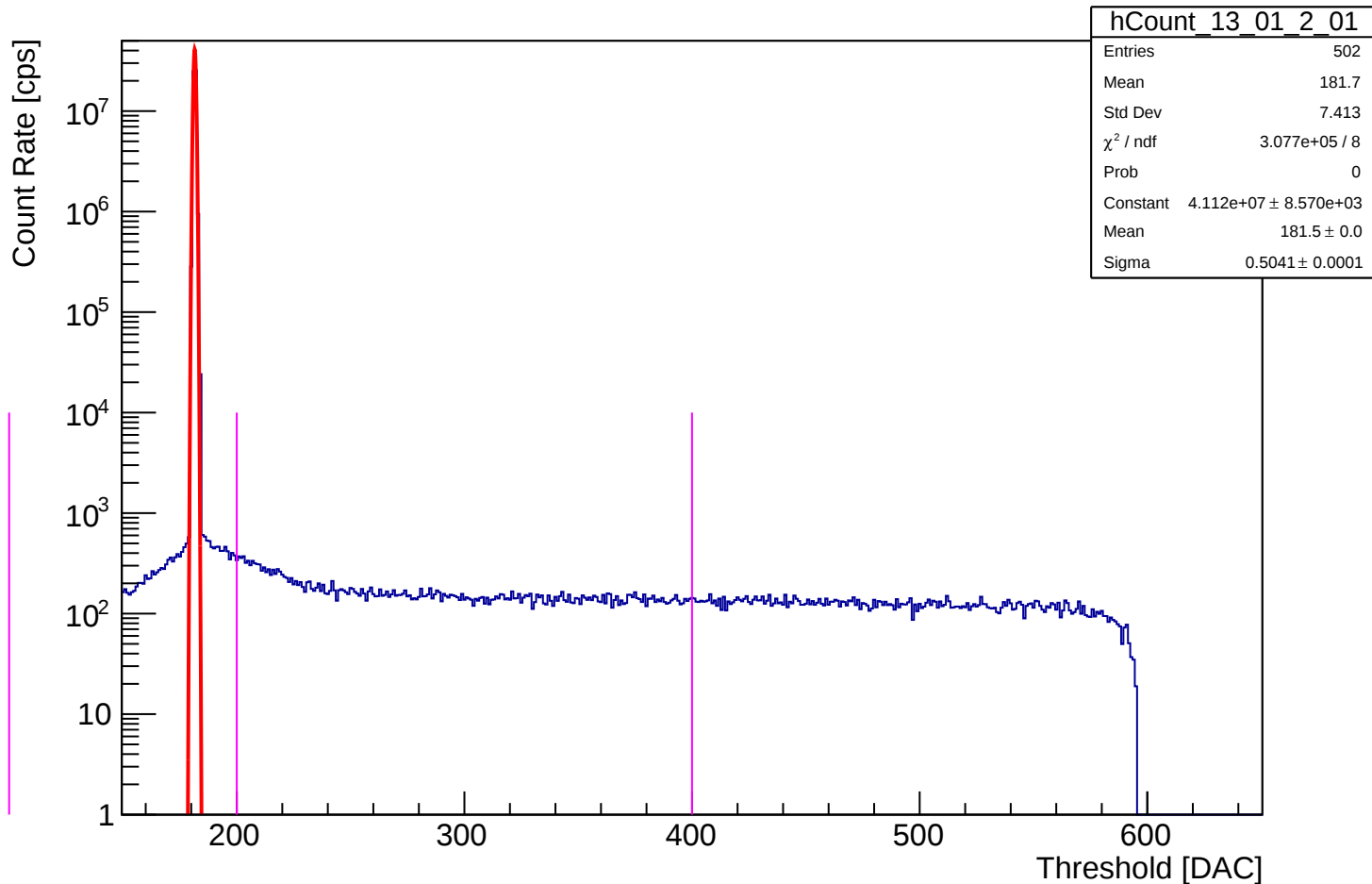


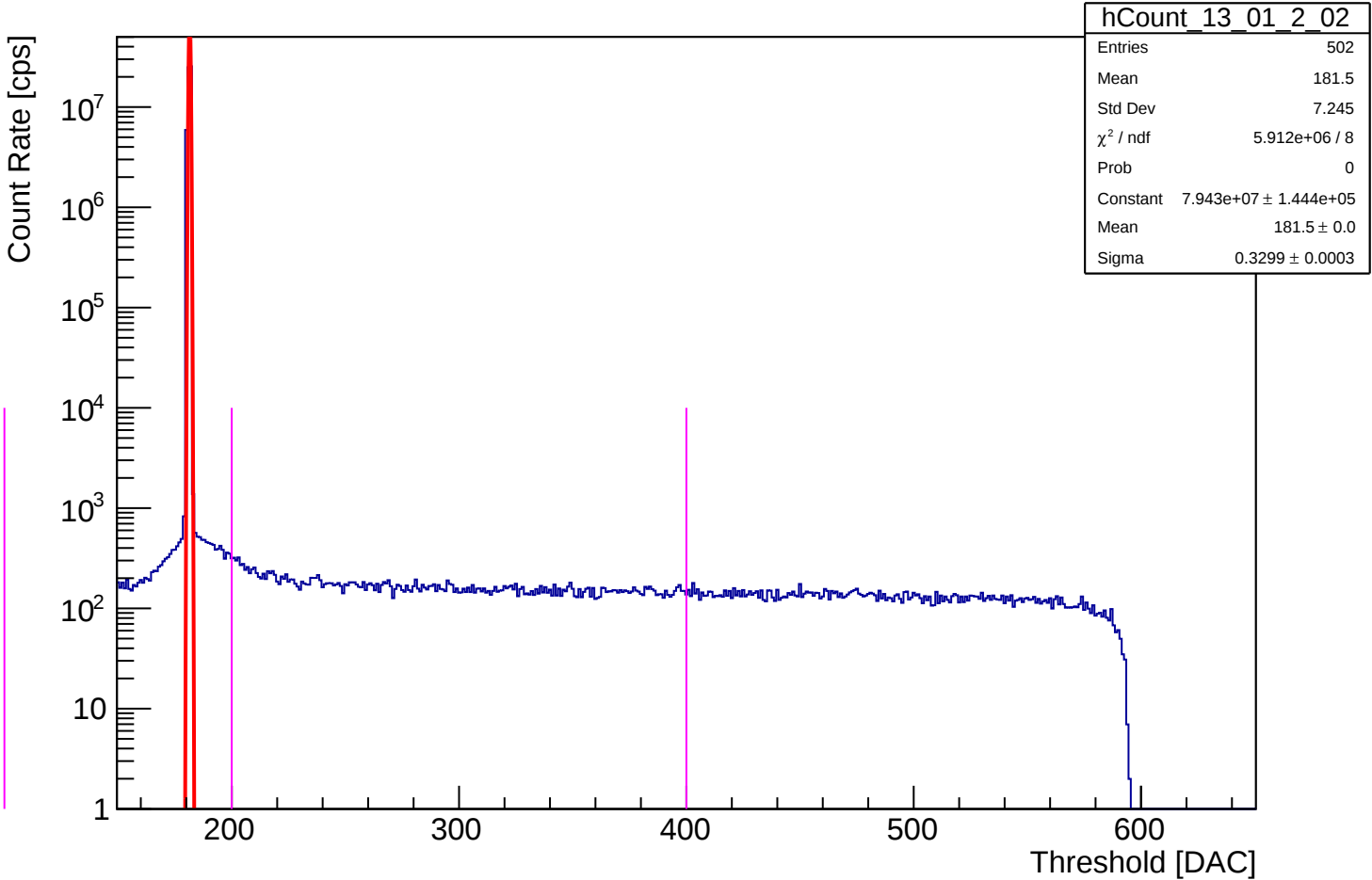
Row 1 Tile 1 Pmt 6 Pixel 56 Slot 13 Fiber 1 Asic 2 Channel 59

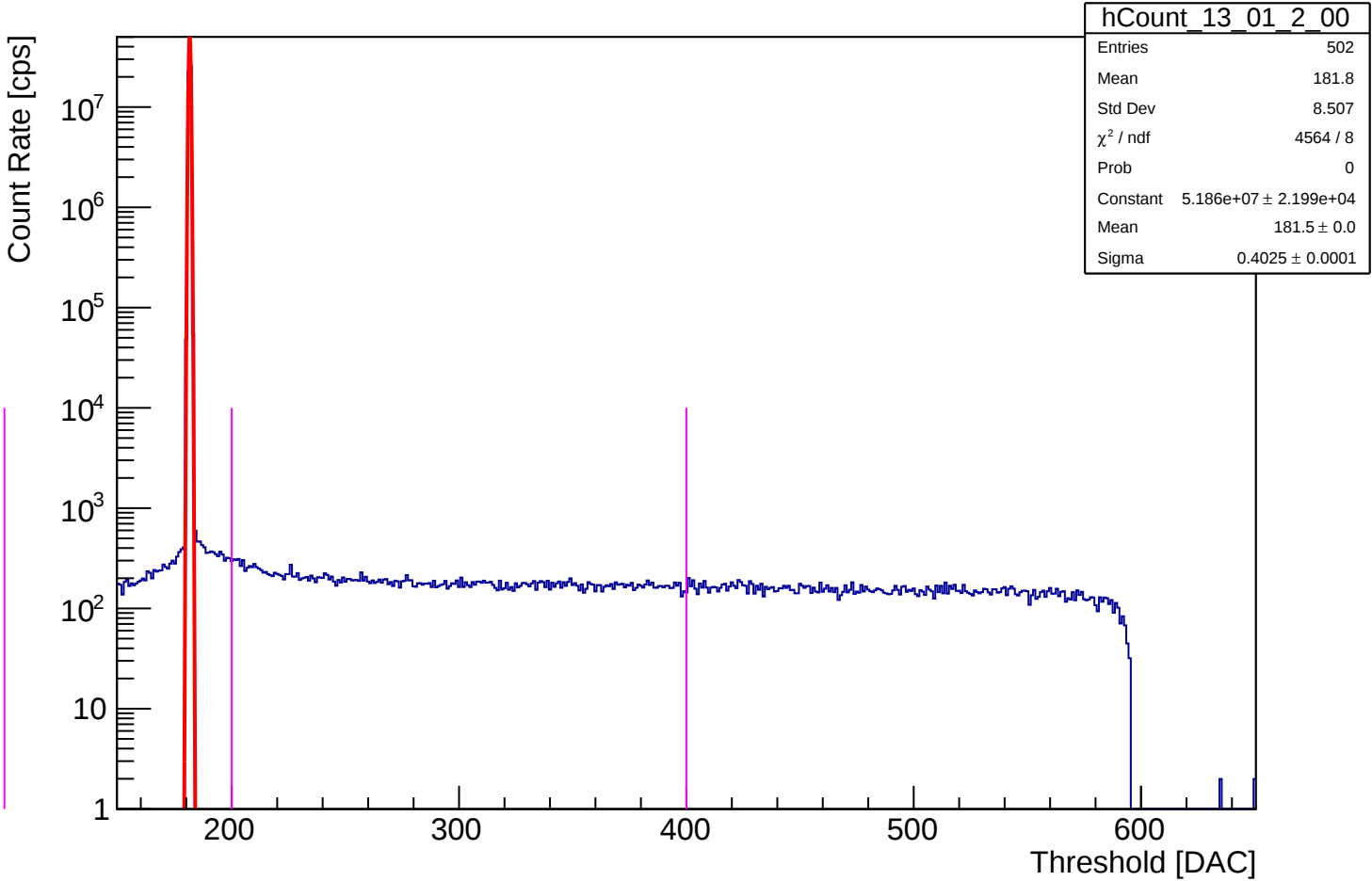




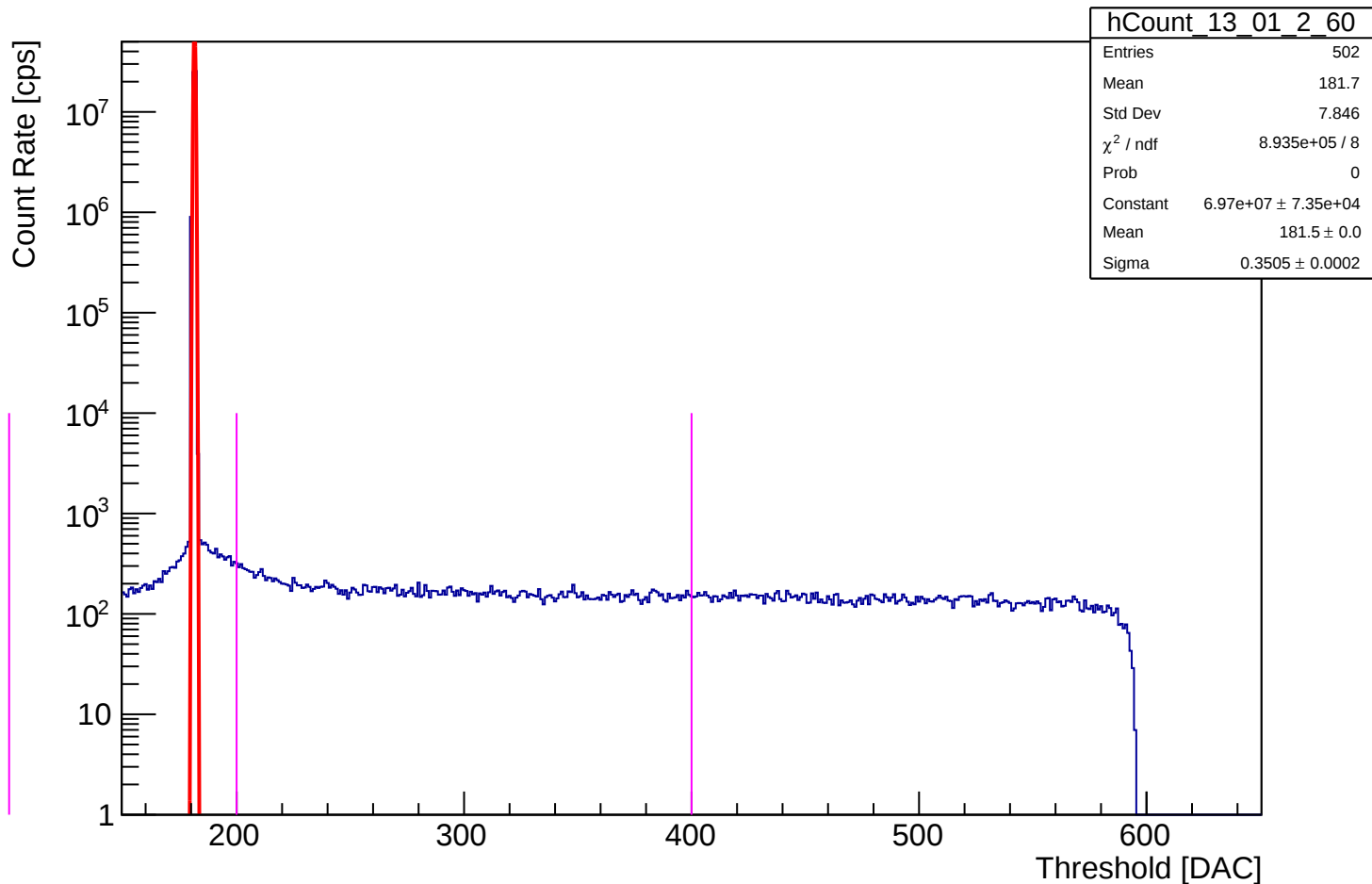
Row 1 Tile 1 Pmt 6 Pixel 58 Slot 13 Fiber 1 Asic 2 Channel 1



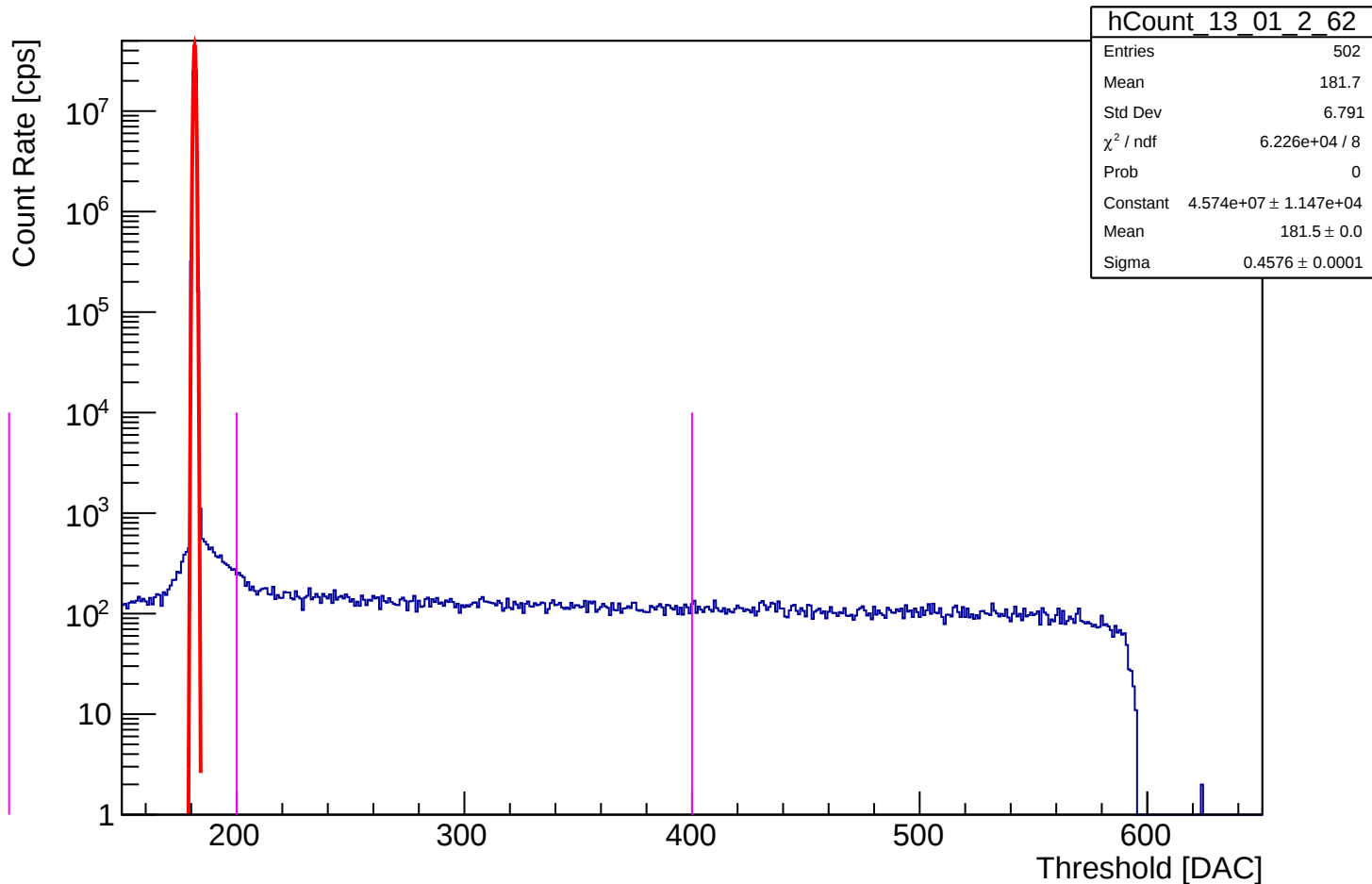




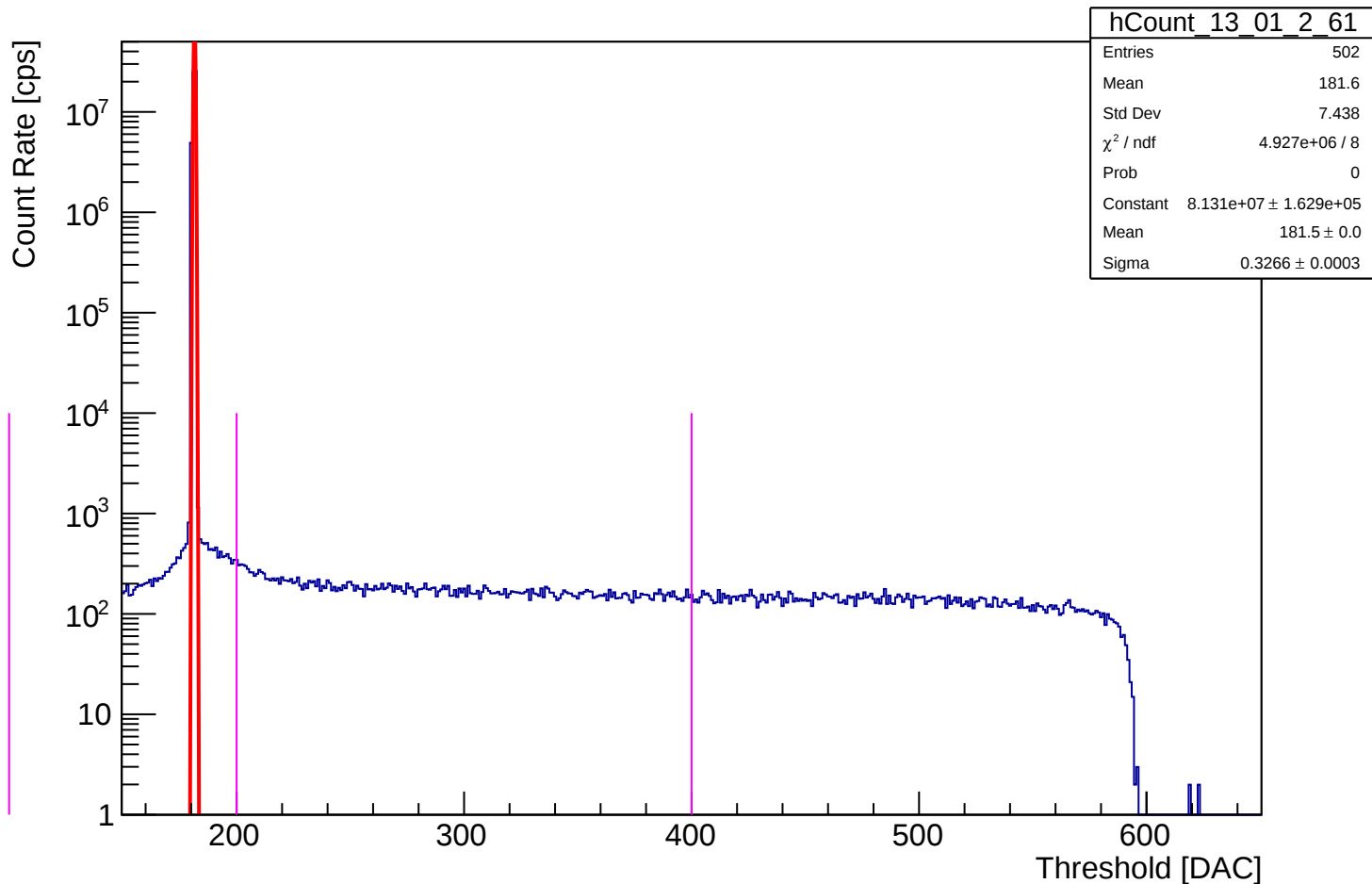
Row 1 Tile 1 Pmt 6 Pixel 61 Slot 13 Fiber 1 Asic 2 Channel 60



Row 1 Tile 1 Pmt 6 Pixel 62 Slot 13 Fiber 1 Asic 2 Channel 62



Row 1 Tile 1 Pmt 6 Pixel 63 Slot 13 Fiber 1 Asic 2 Channel 61



Row 1 Tile 1 Pmt 6 Pixel 64 Slot 13 Fiber 1 Asic 2 Channel 63

