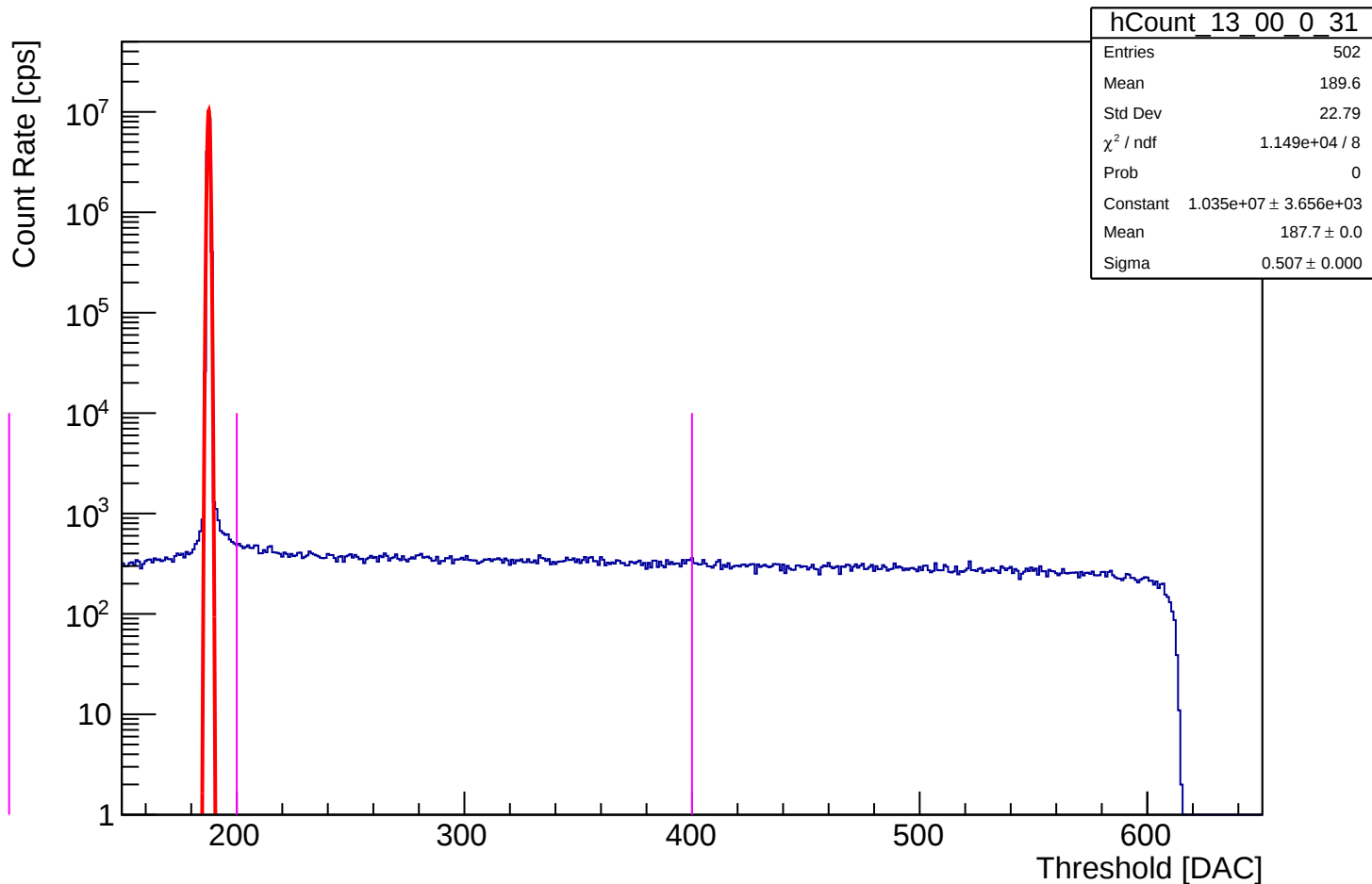
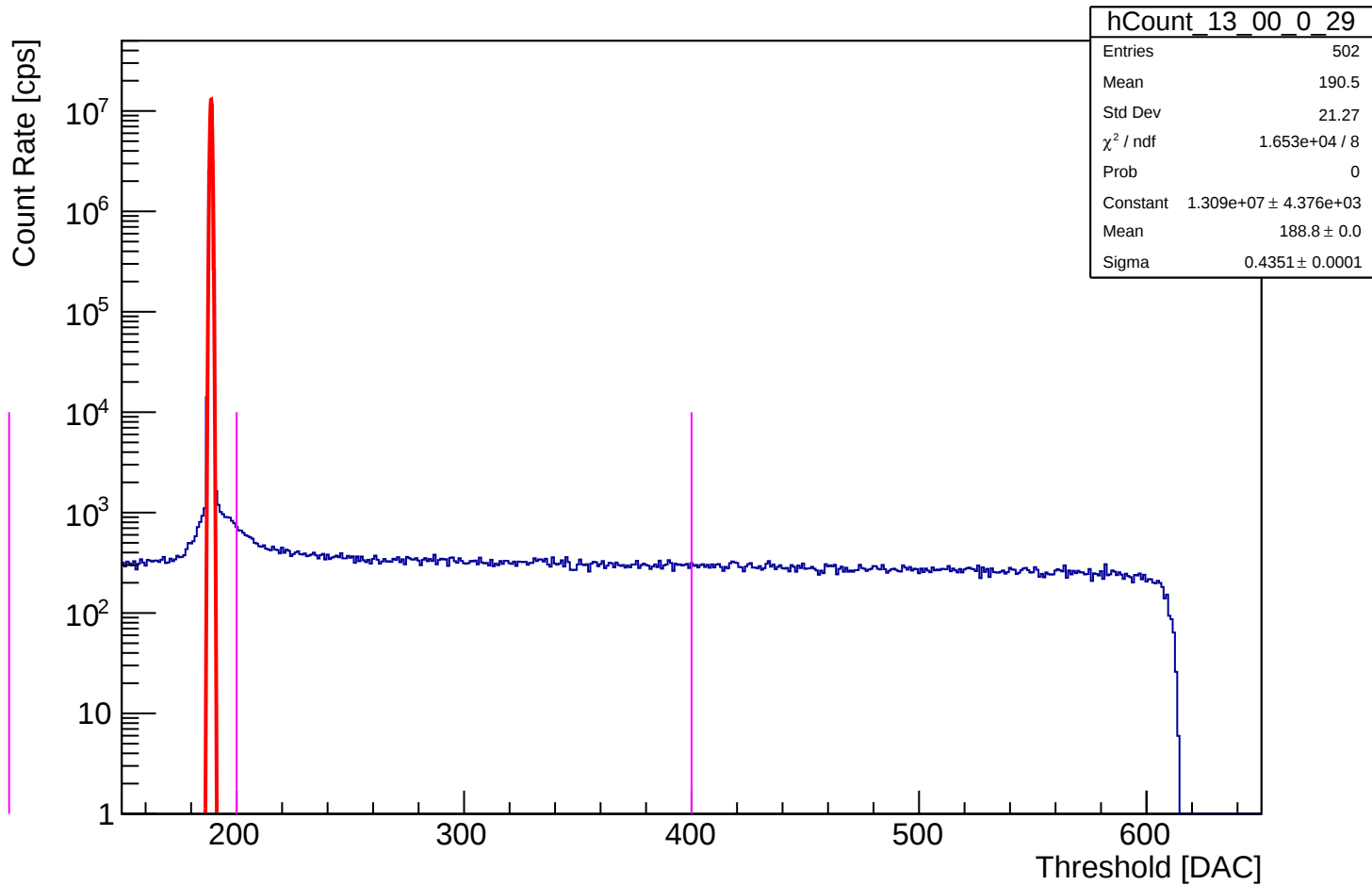


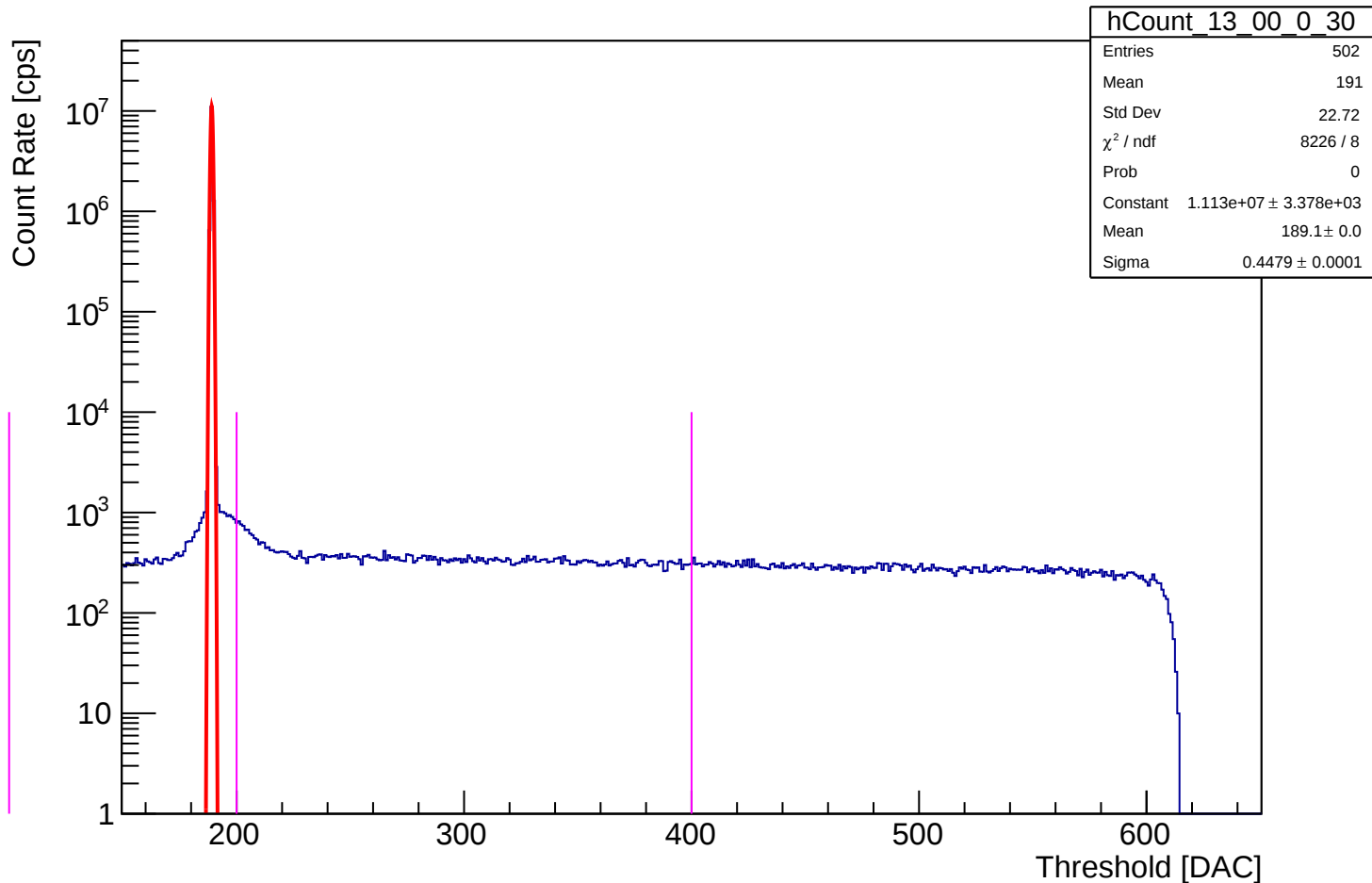
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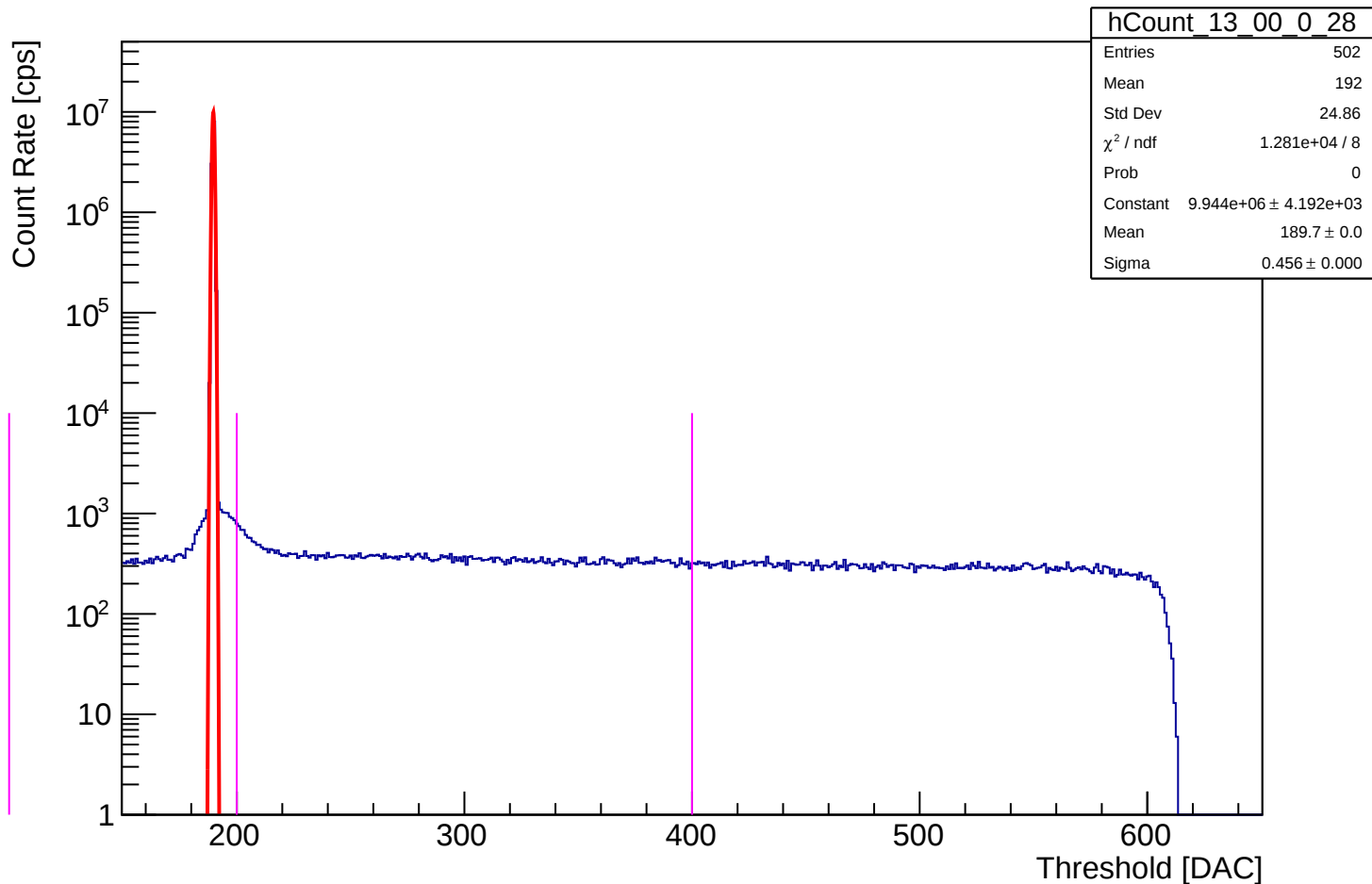
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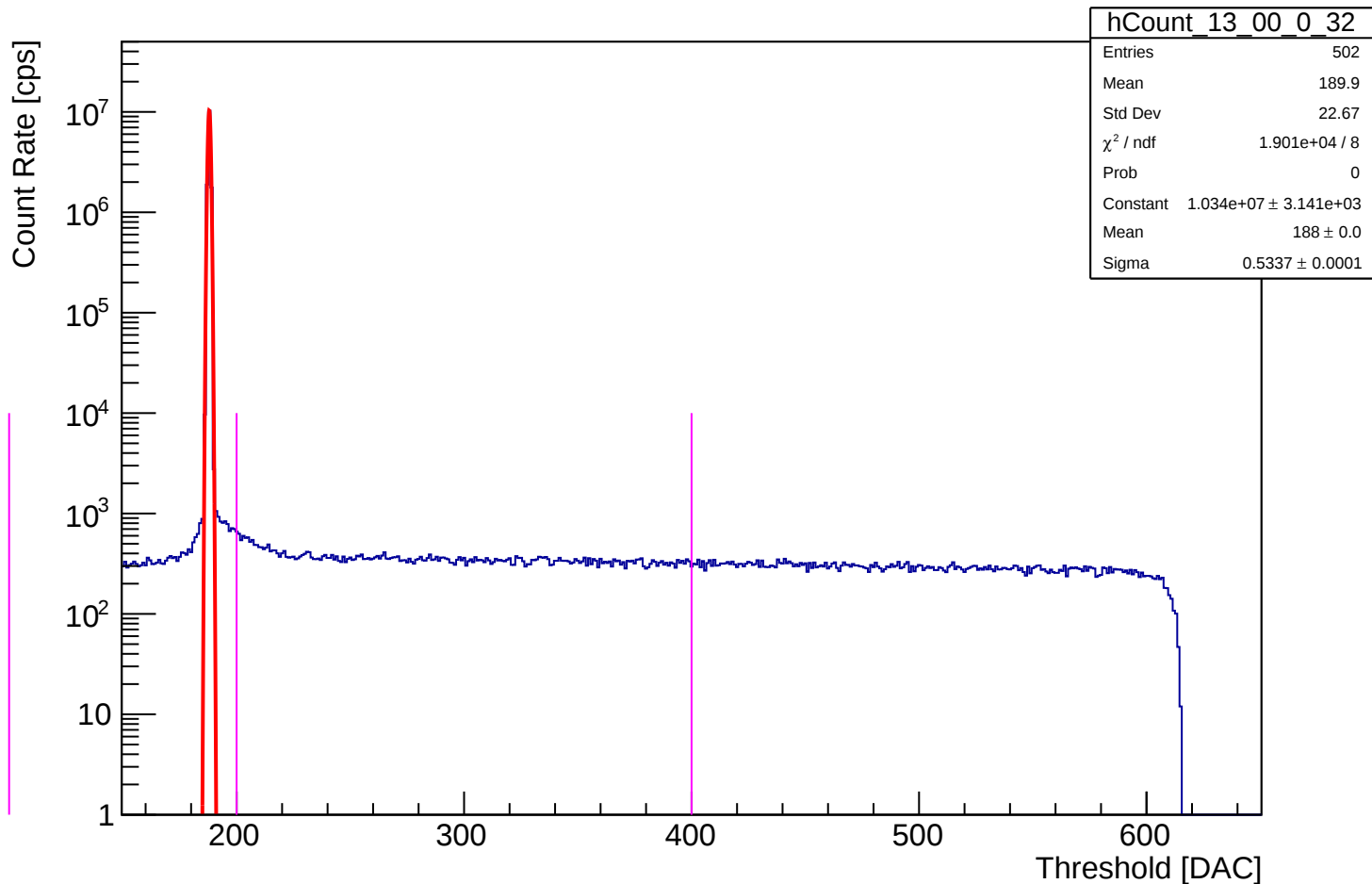
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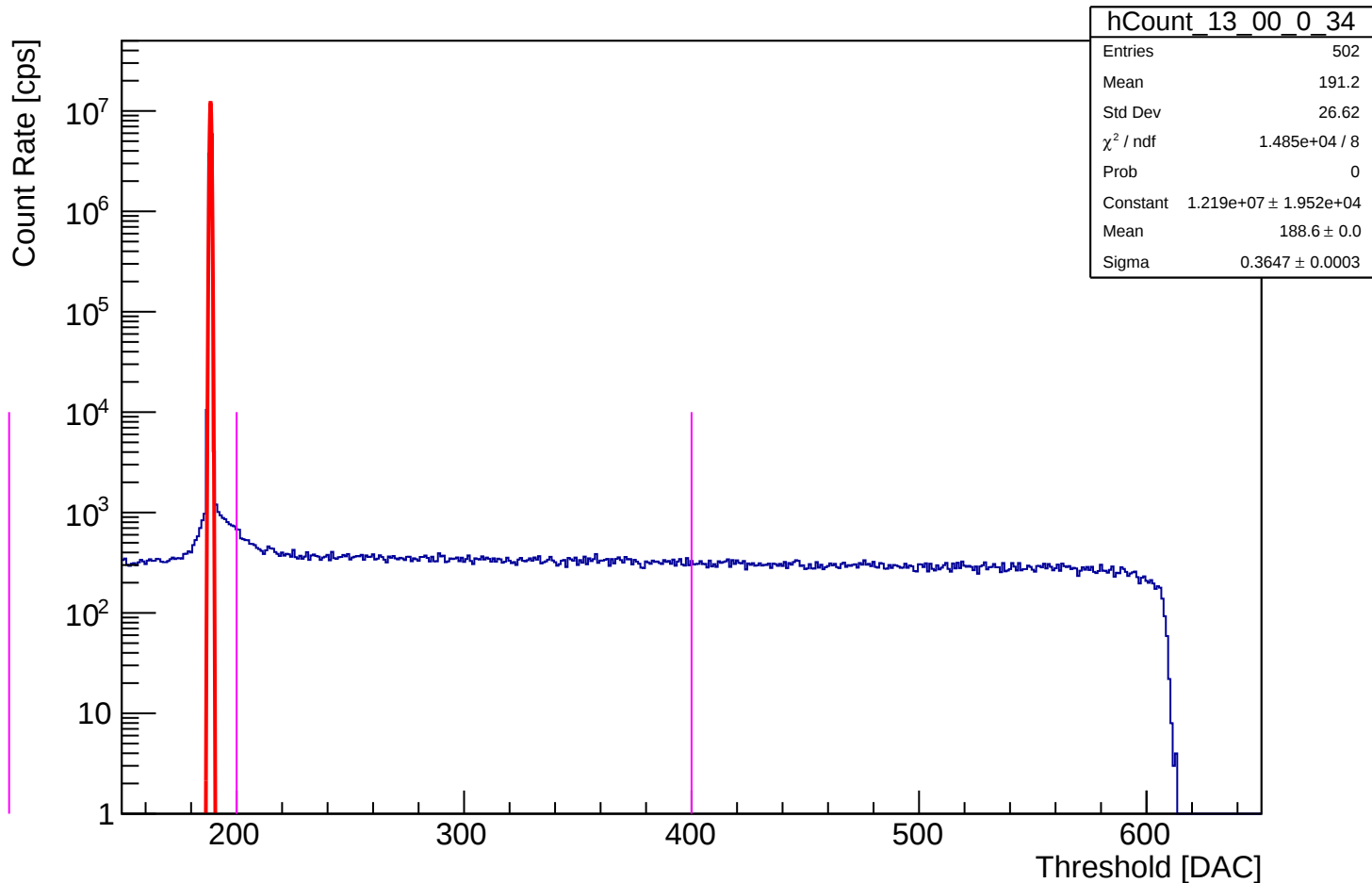
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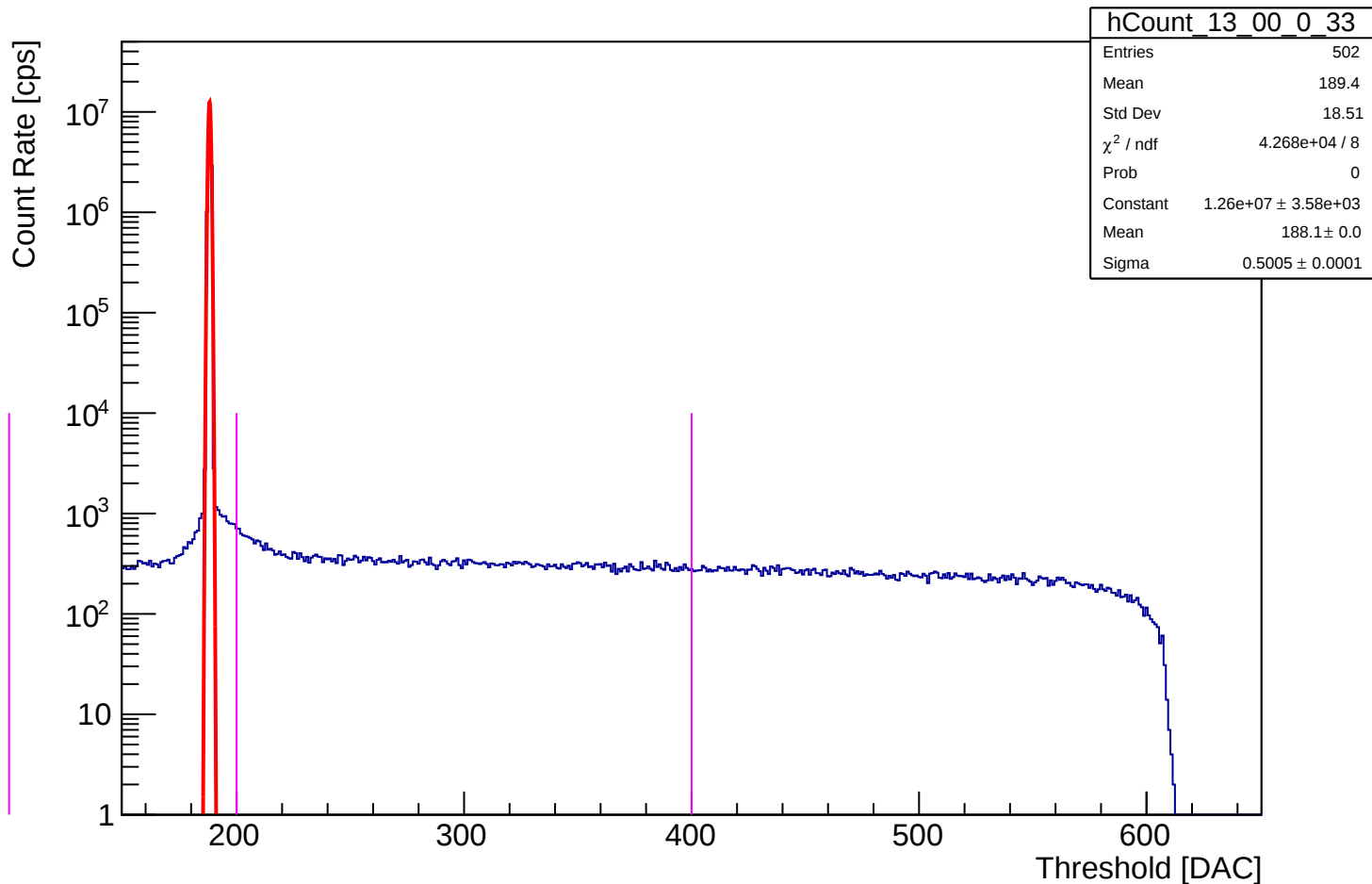
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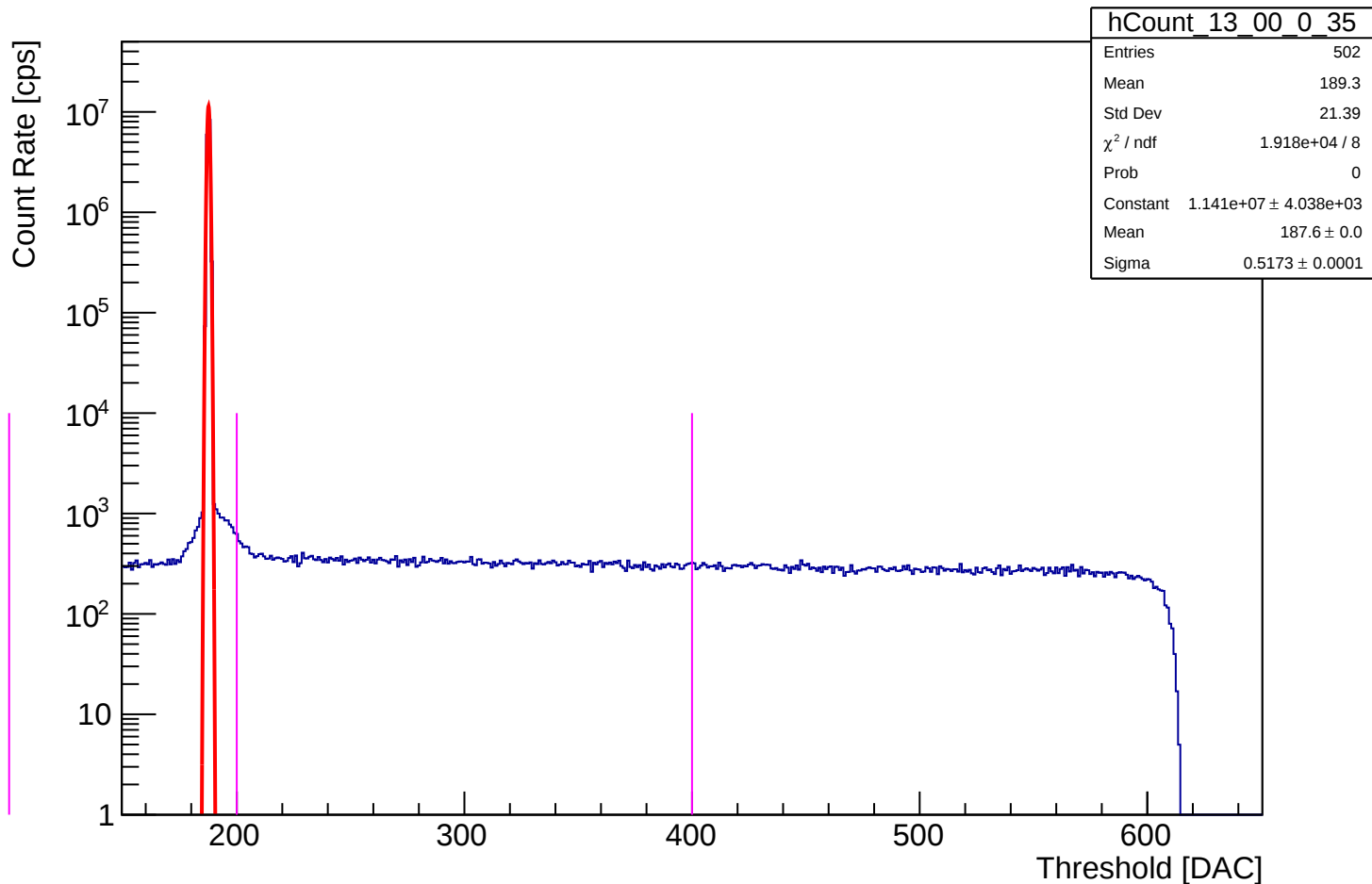
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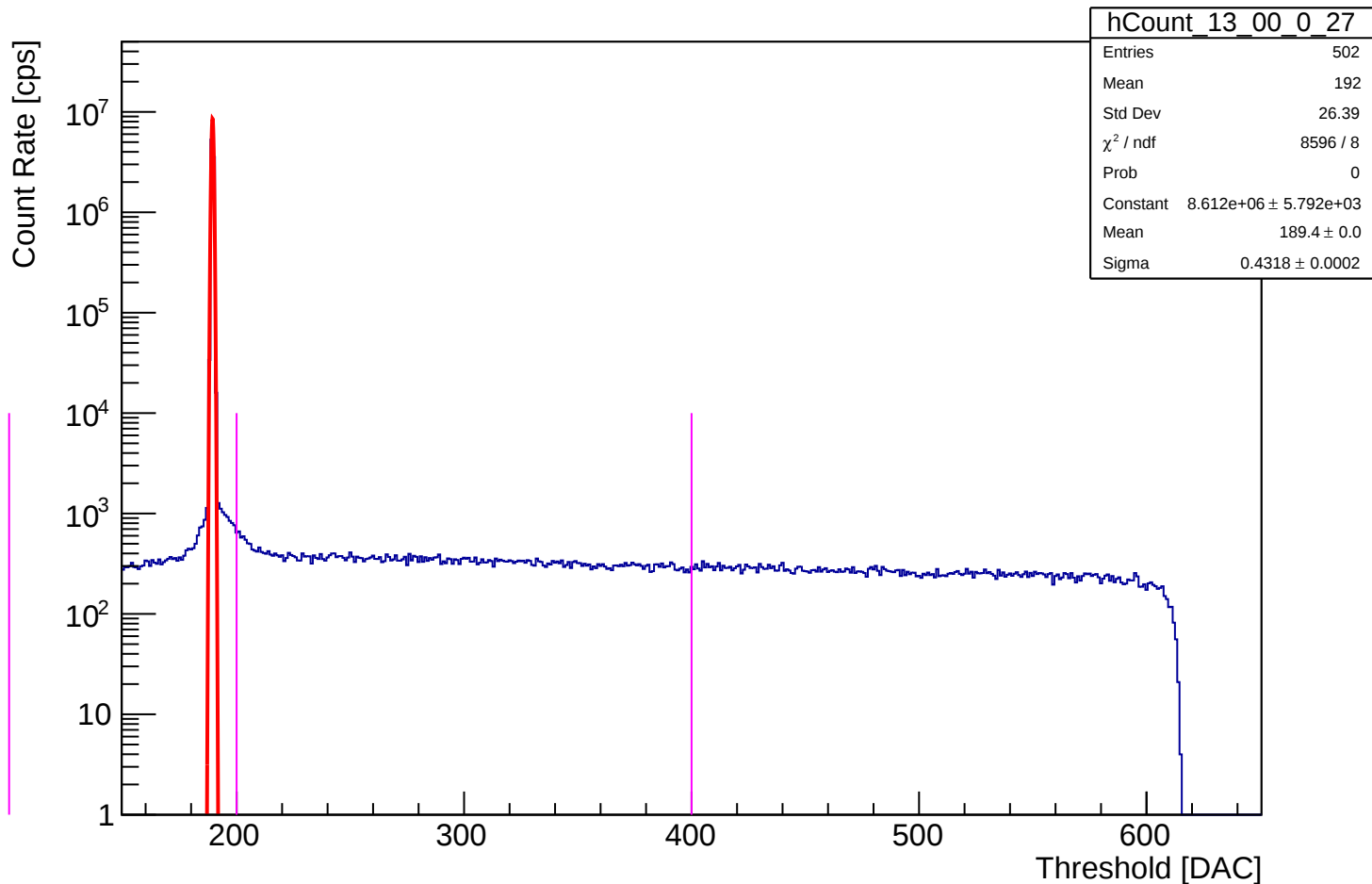
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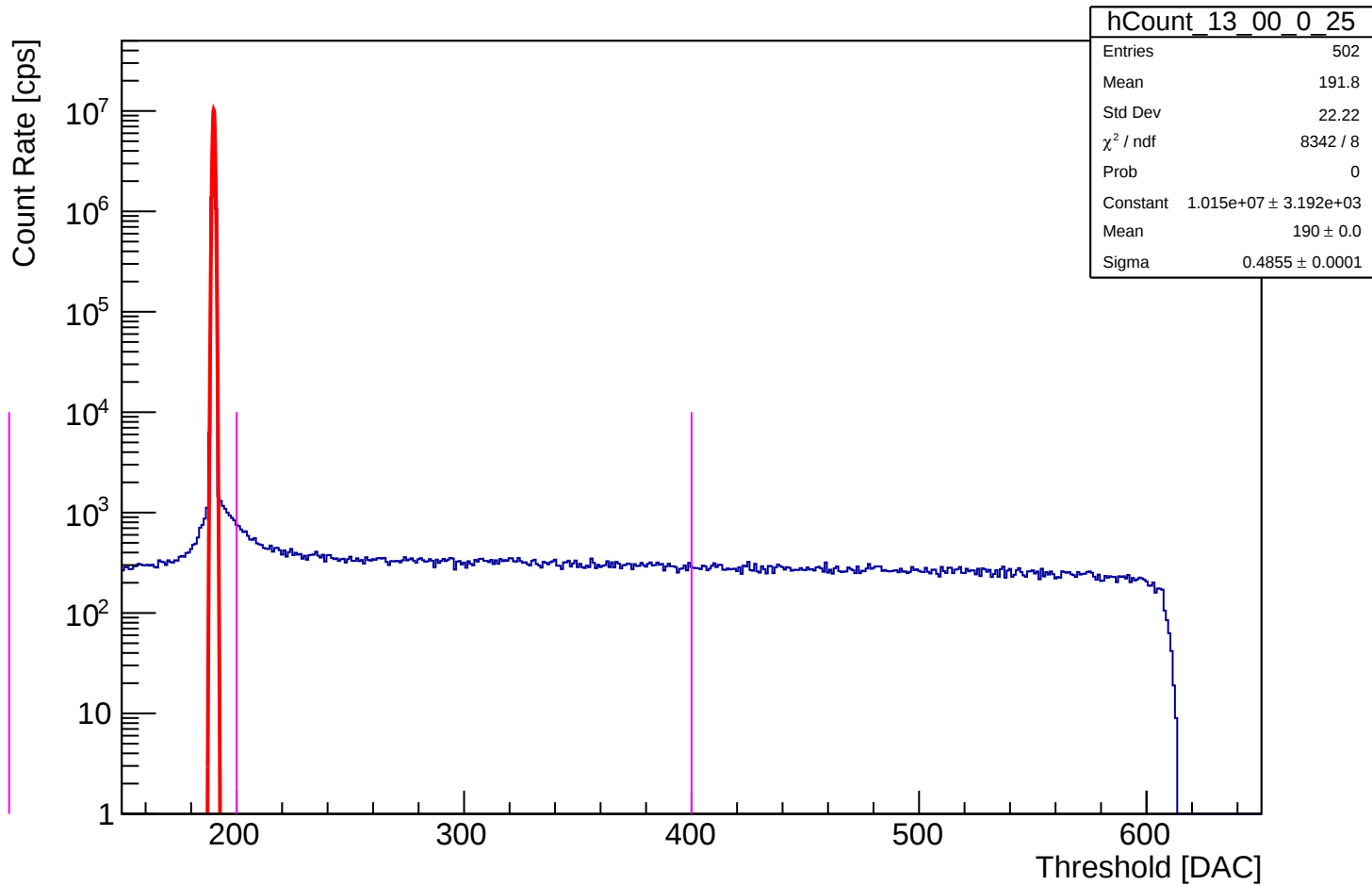
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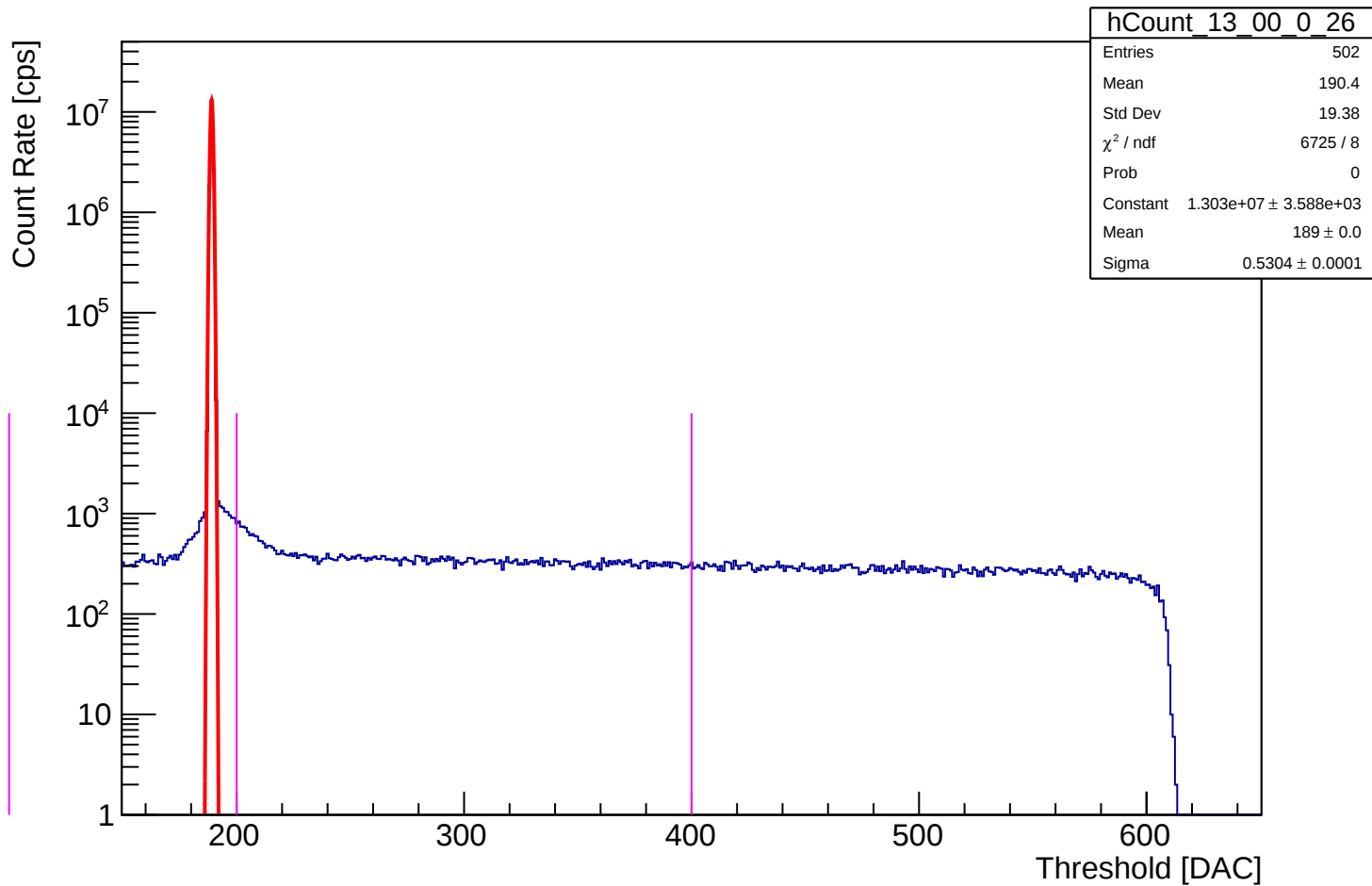
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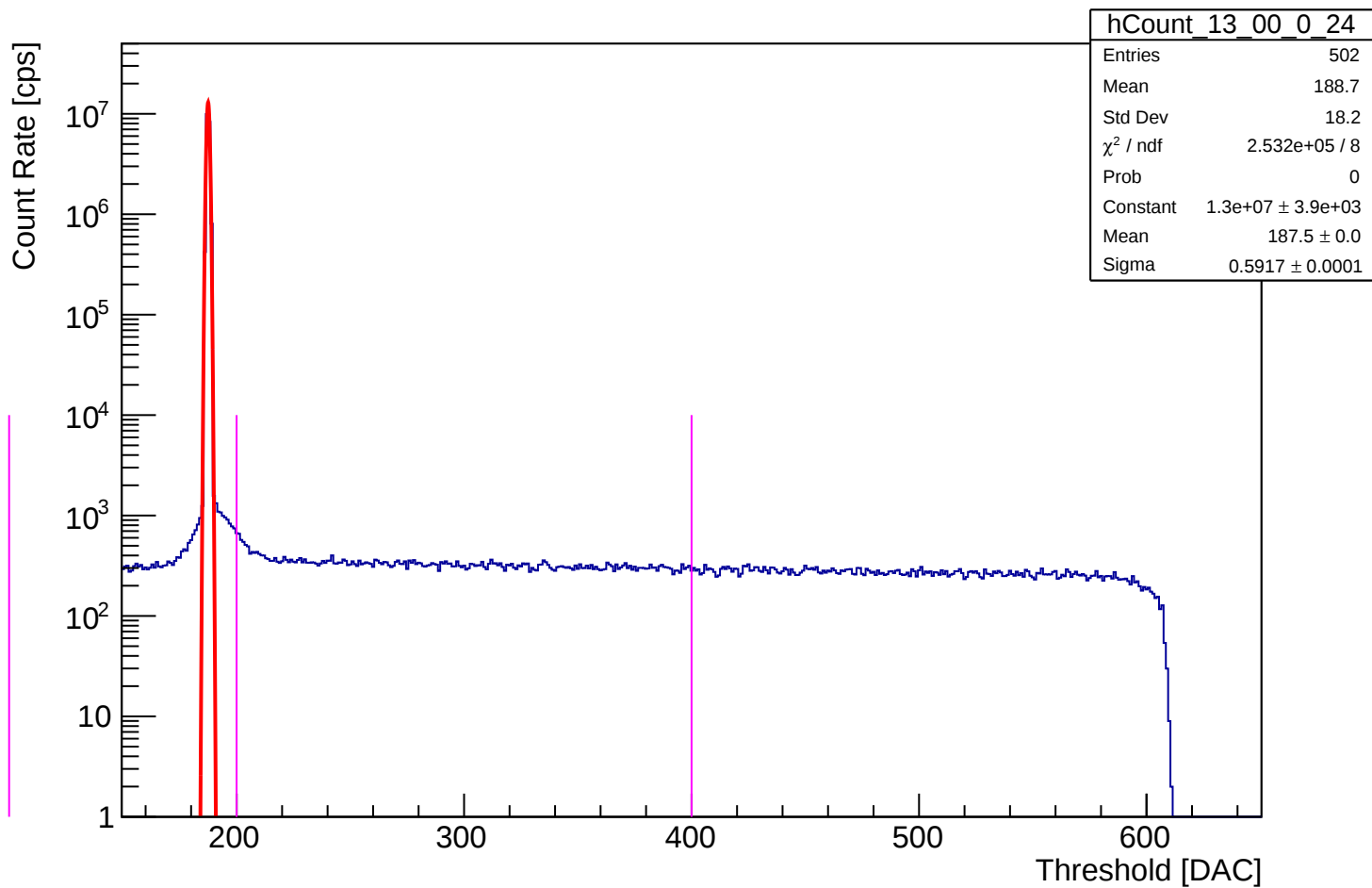
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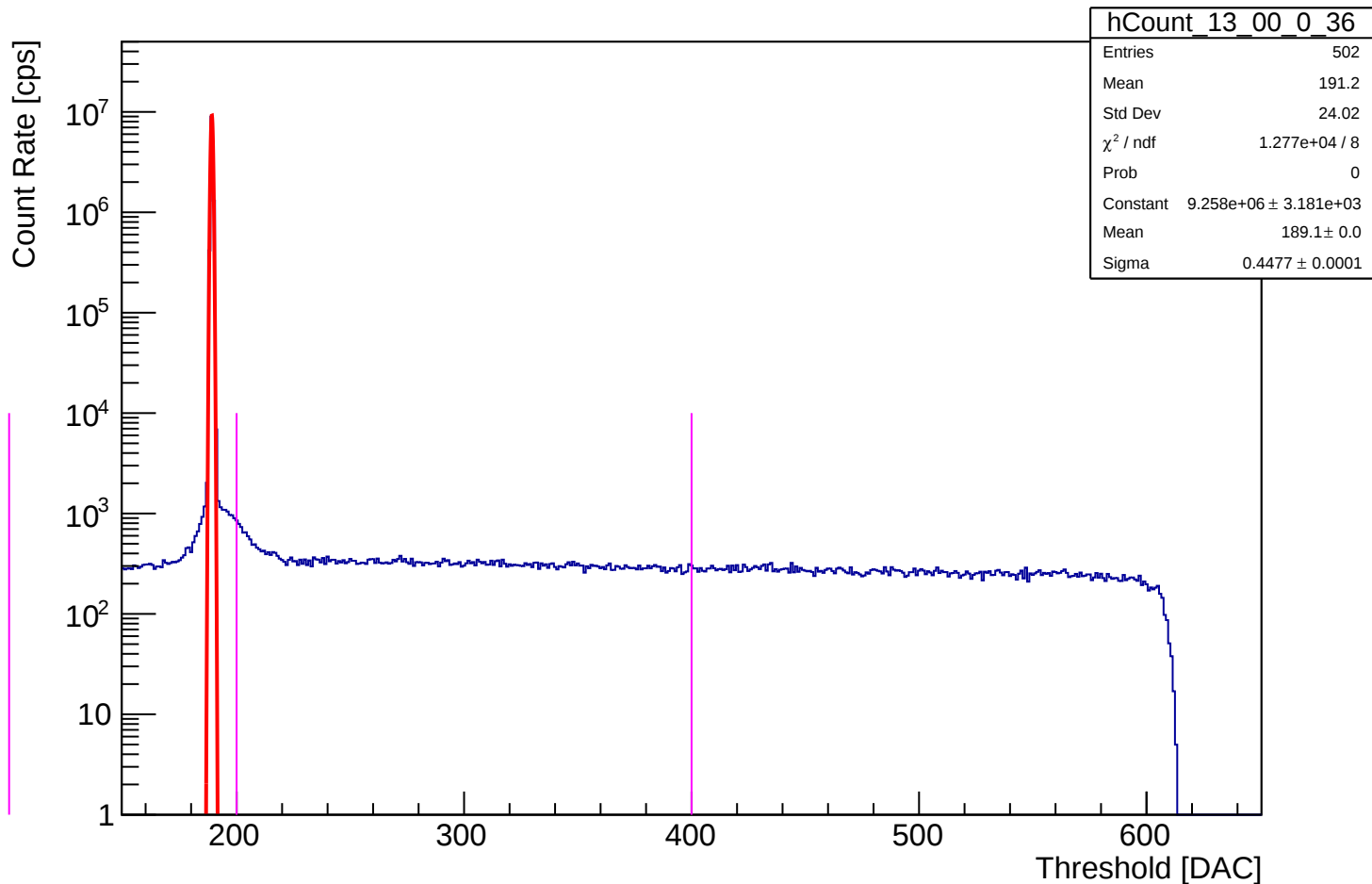
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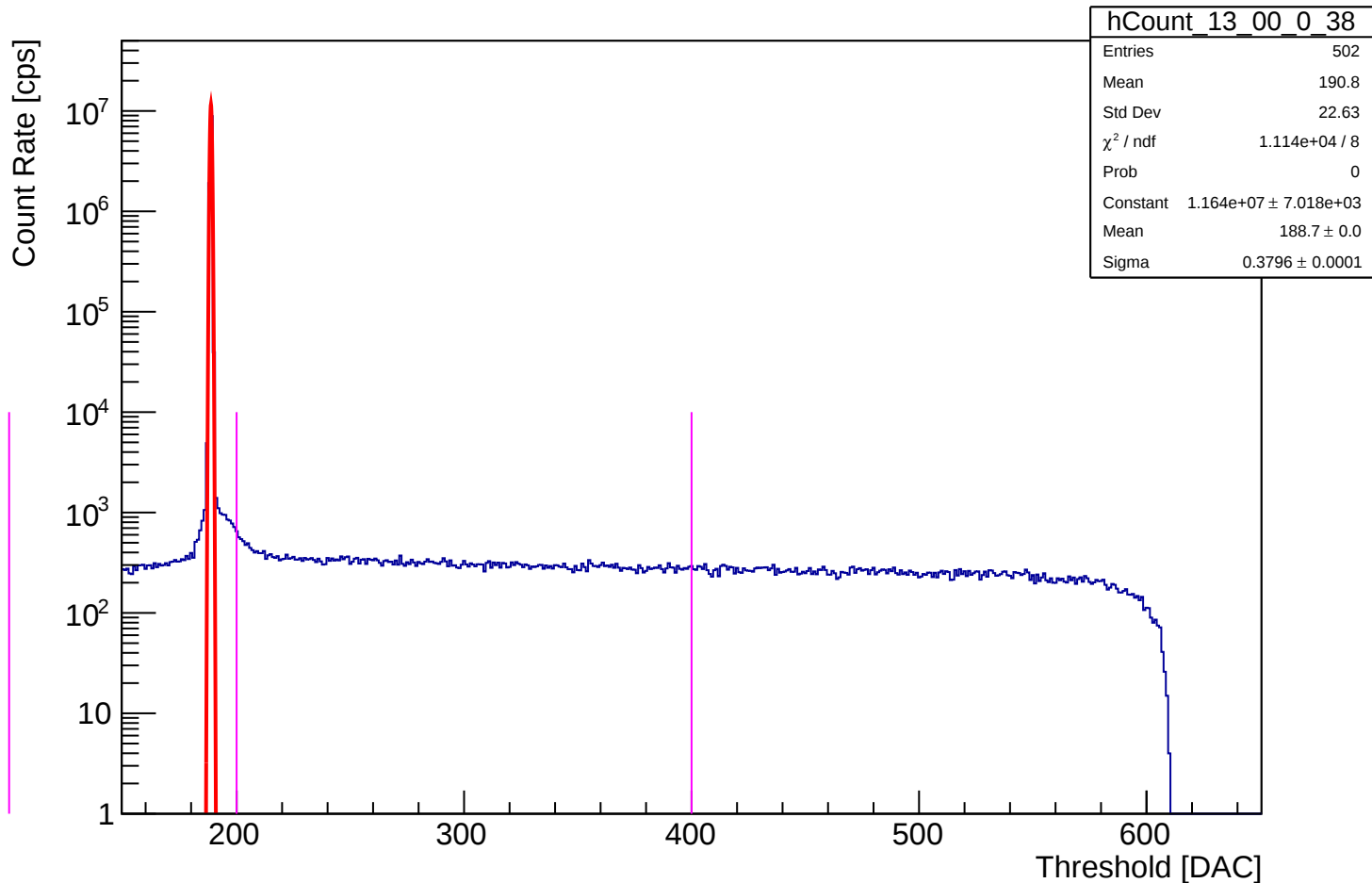
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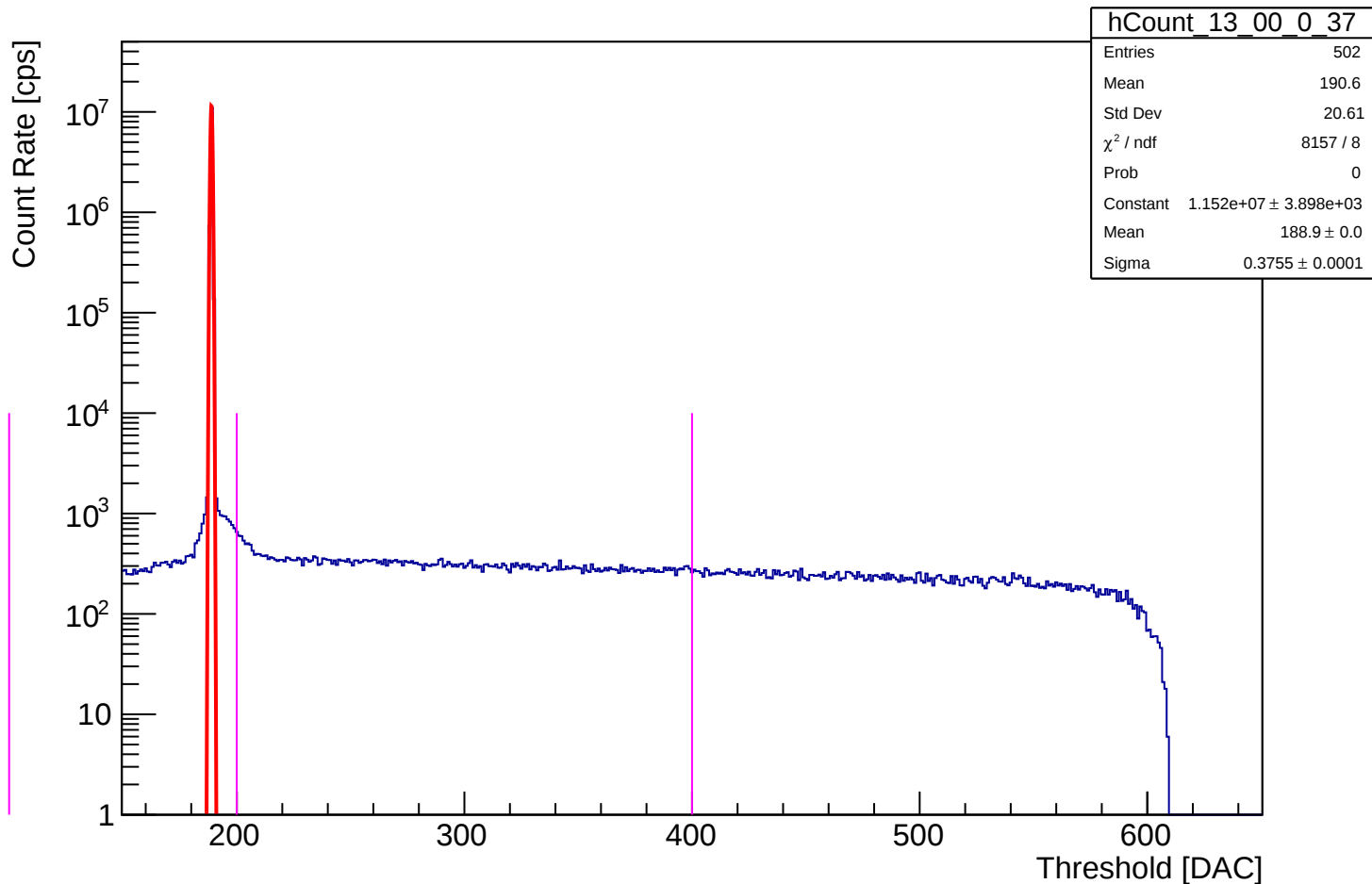
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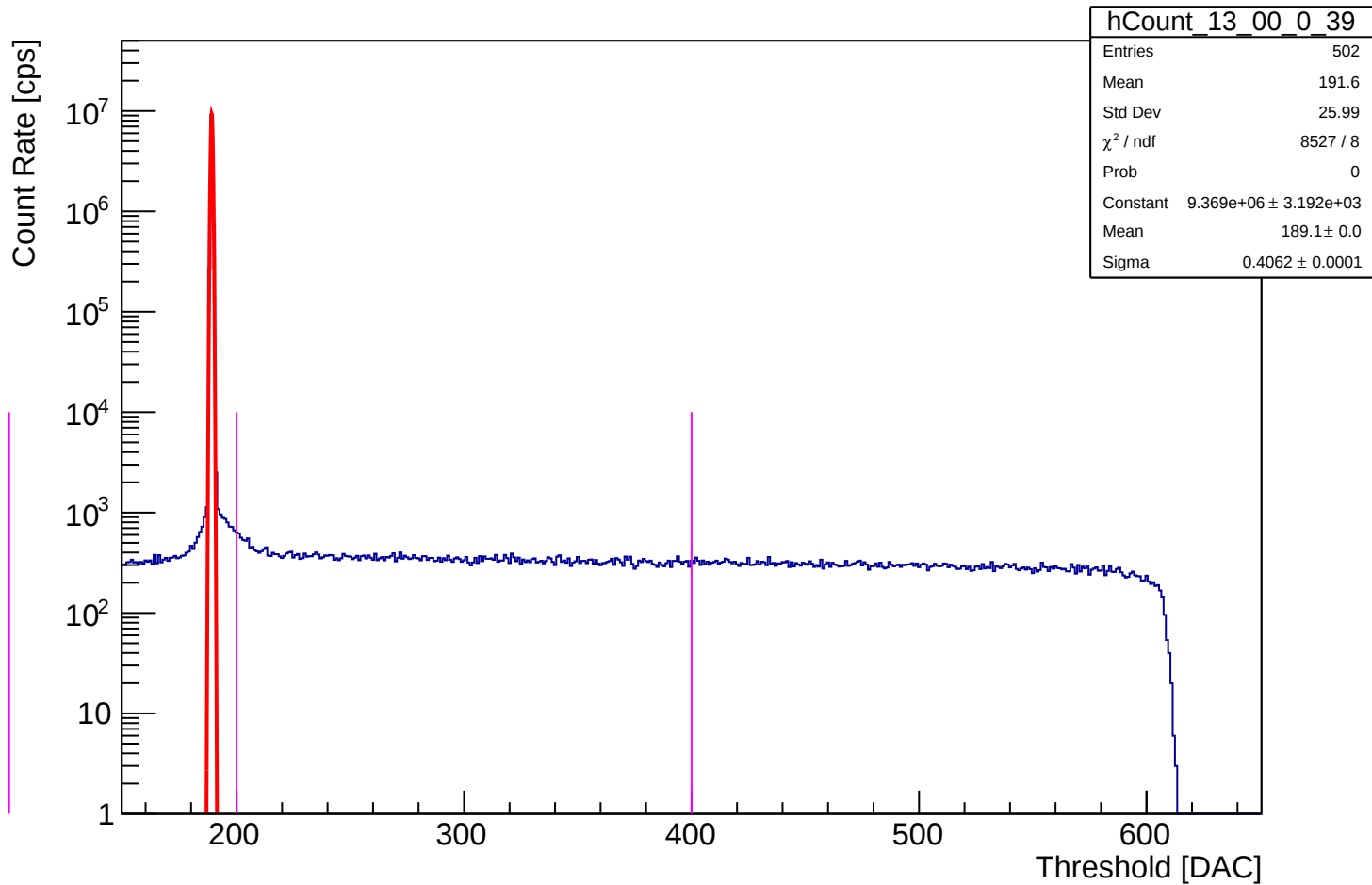
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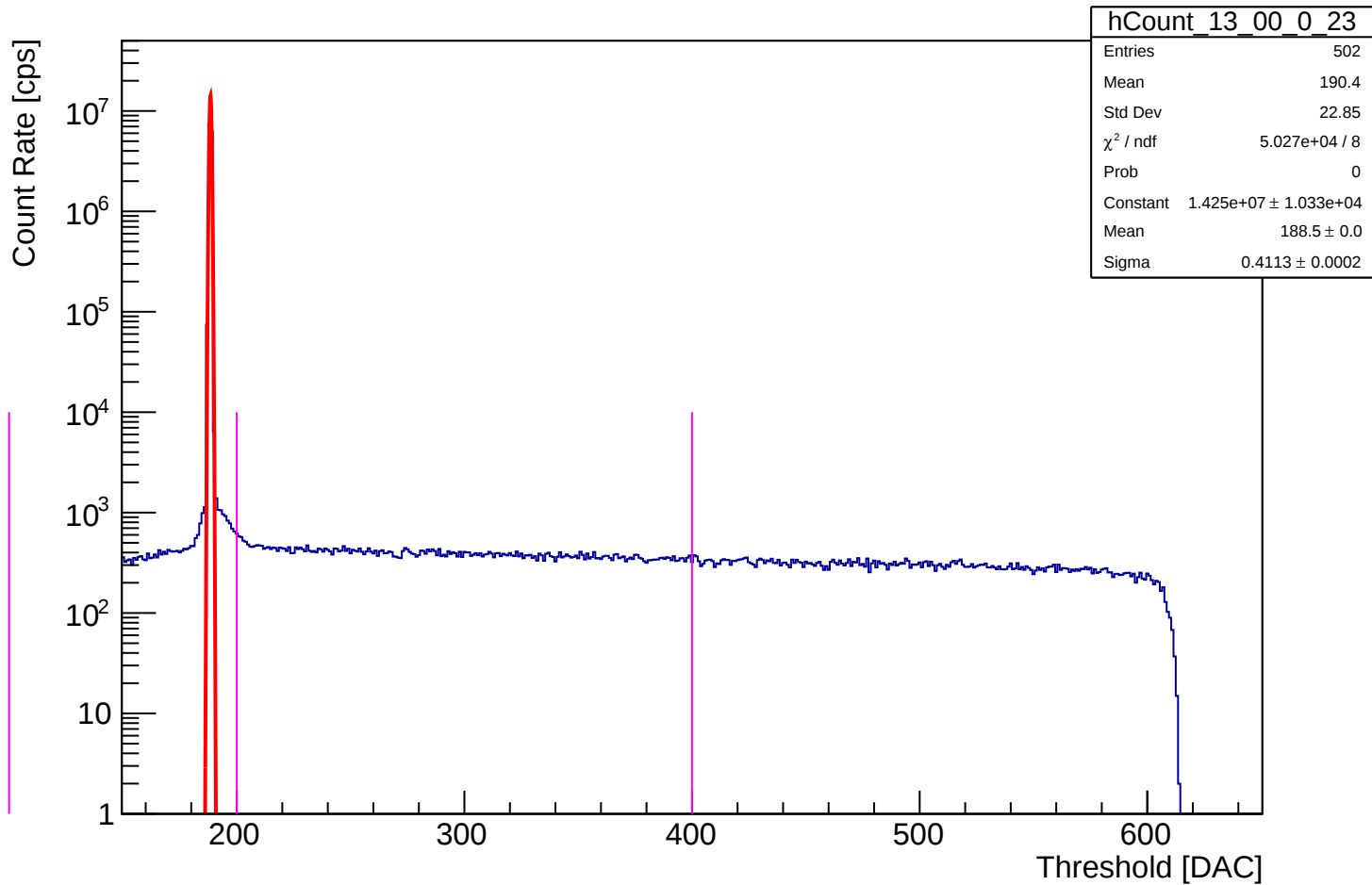
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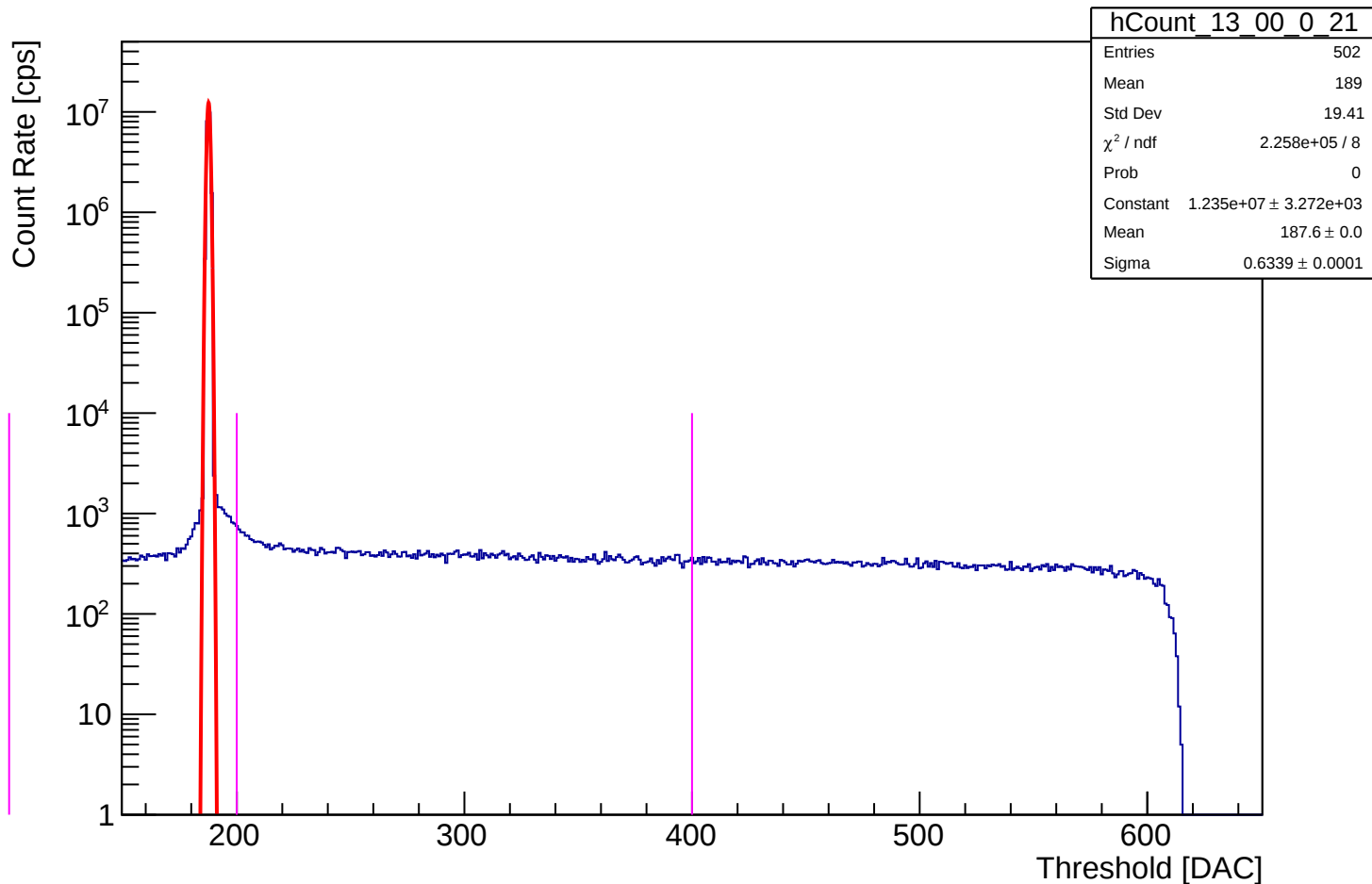
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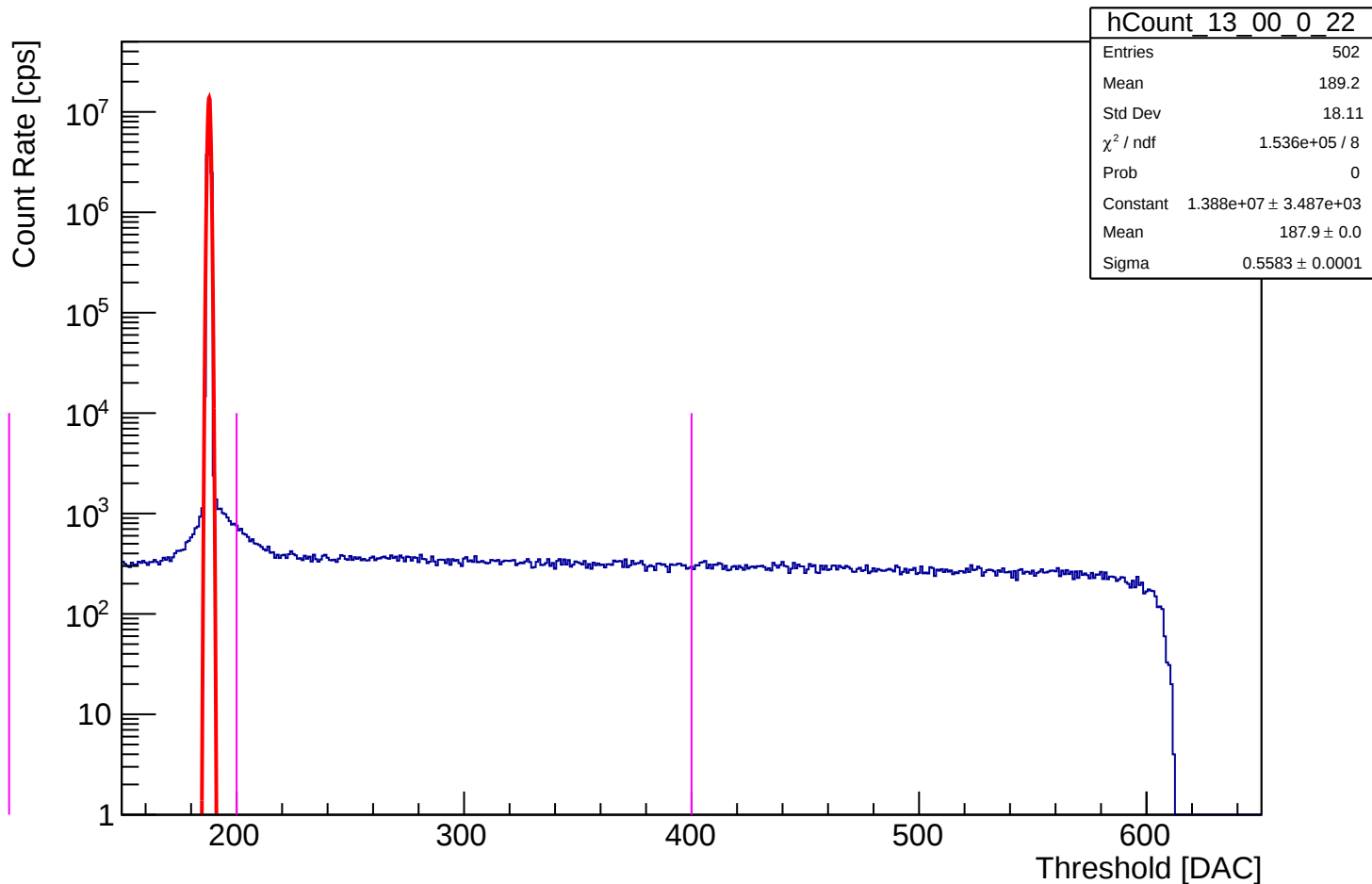
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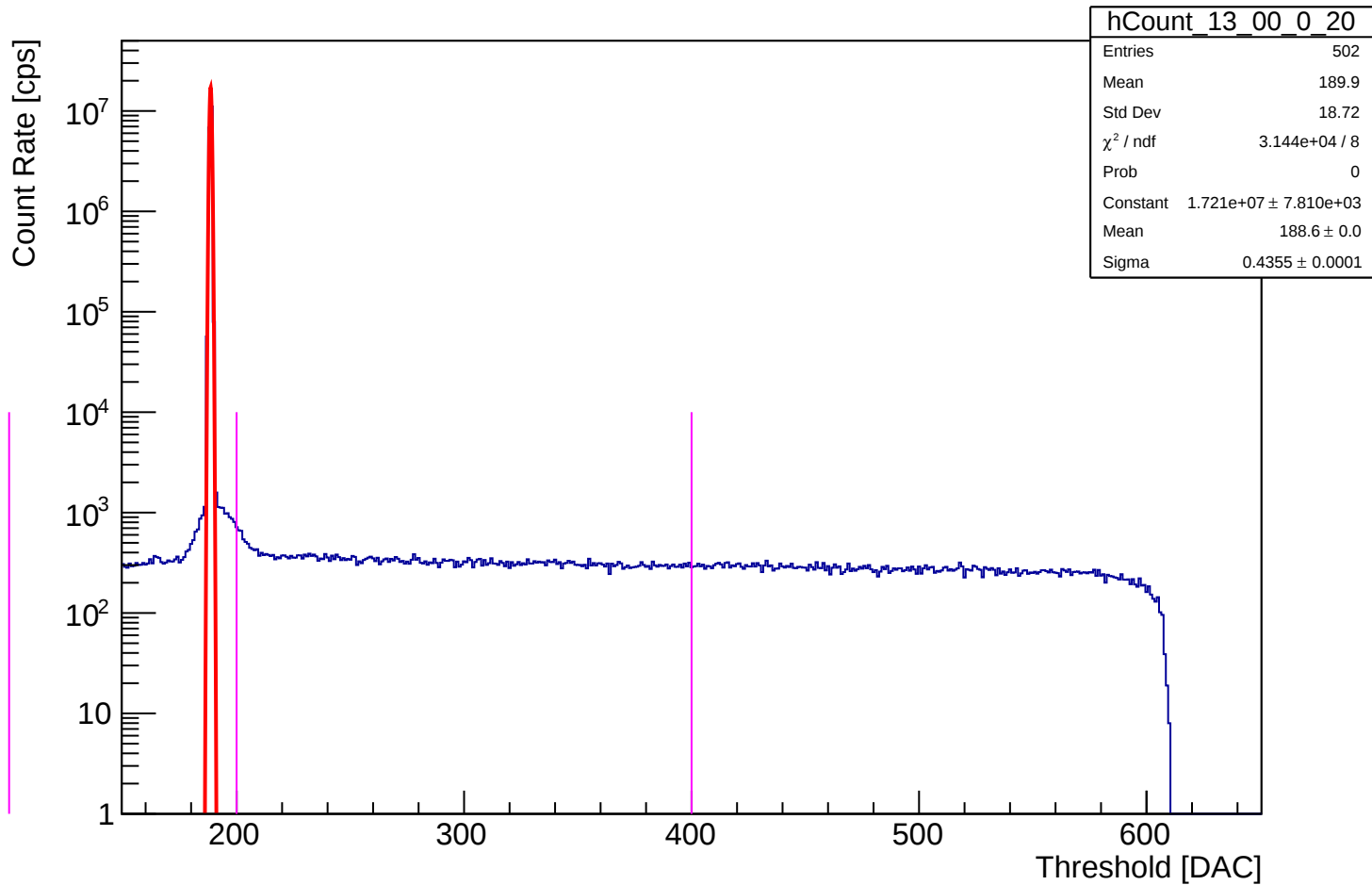
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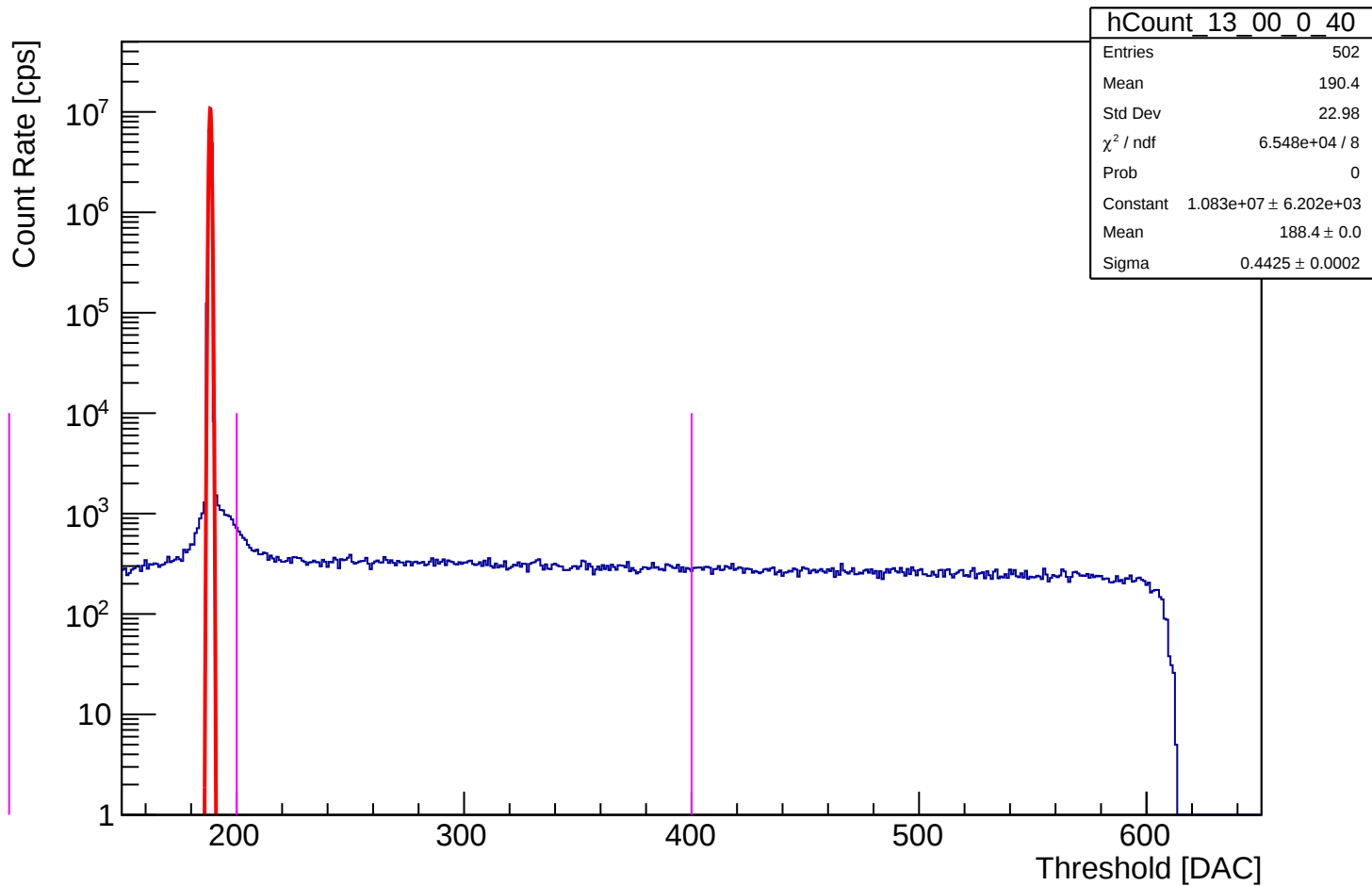
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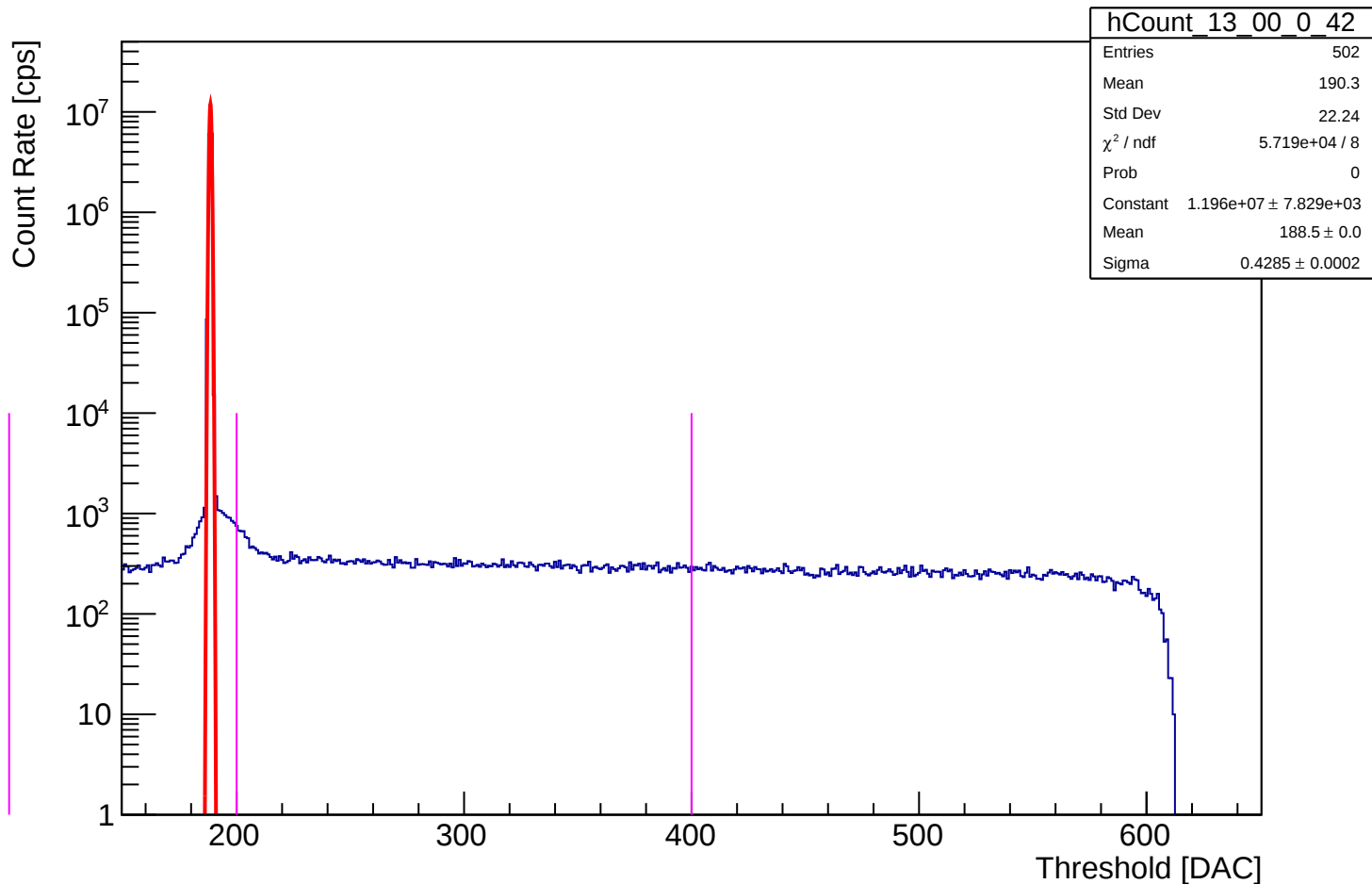
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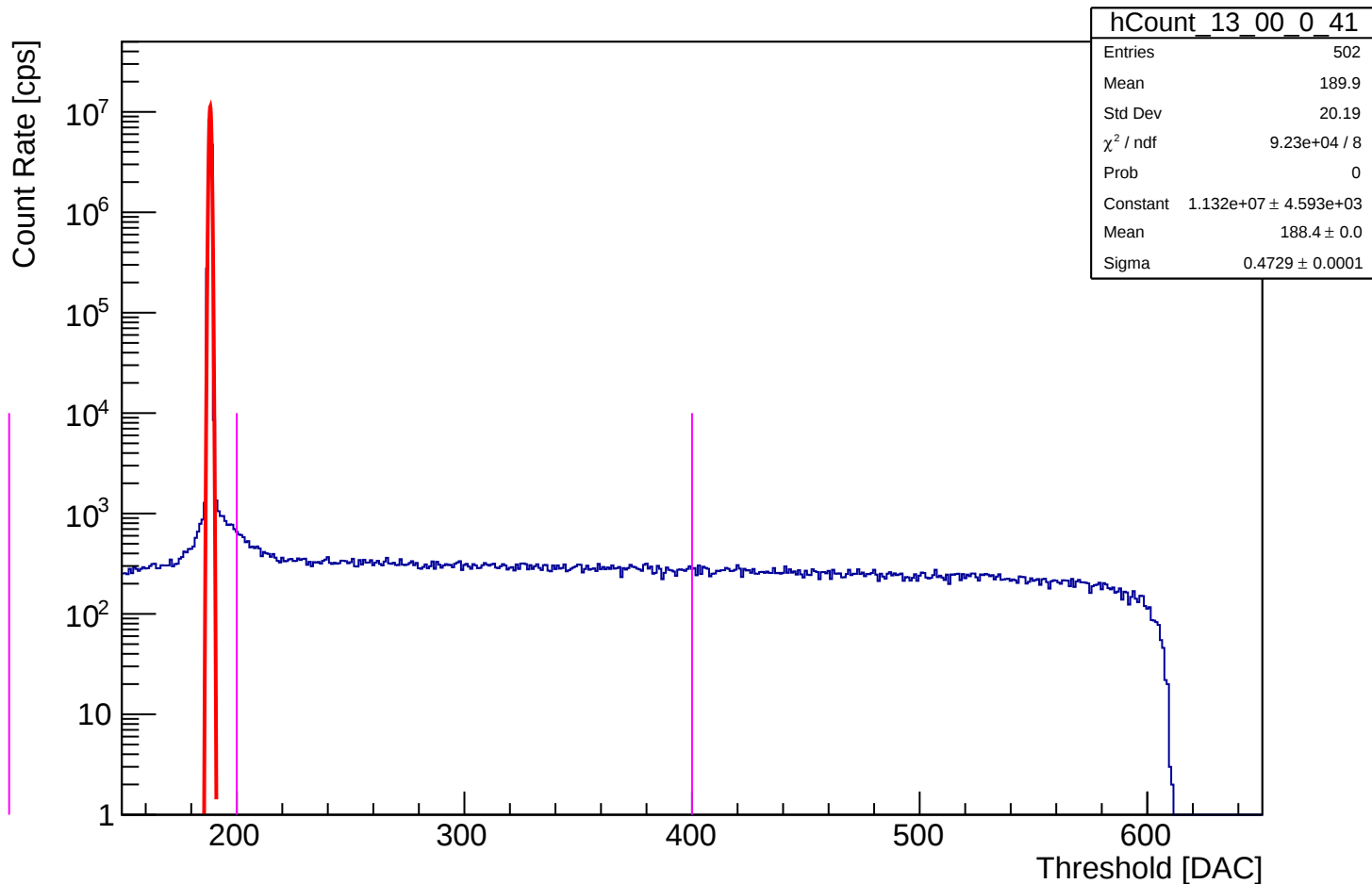
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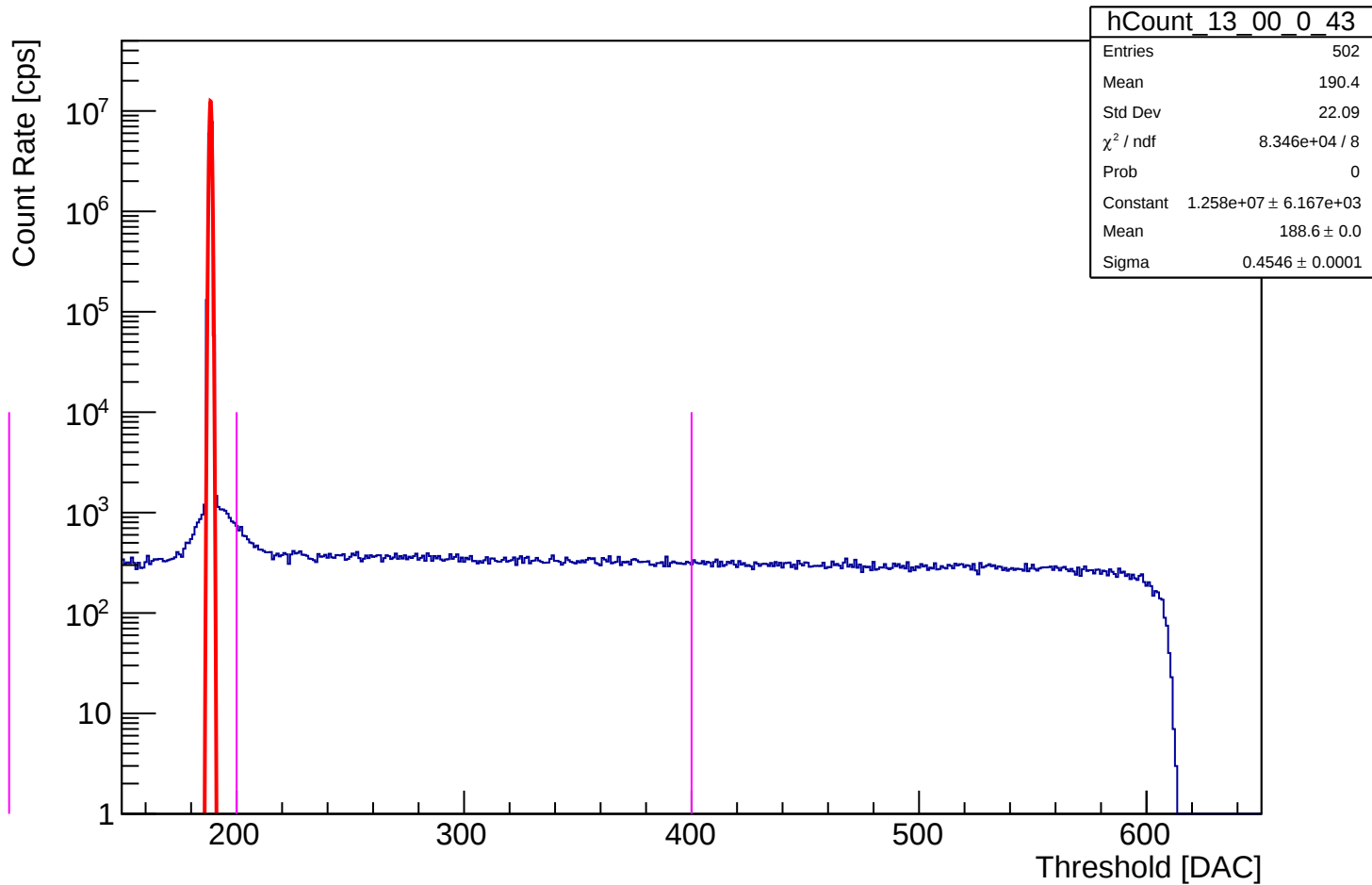
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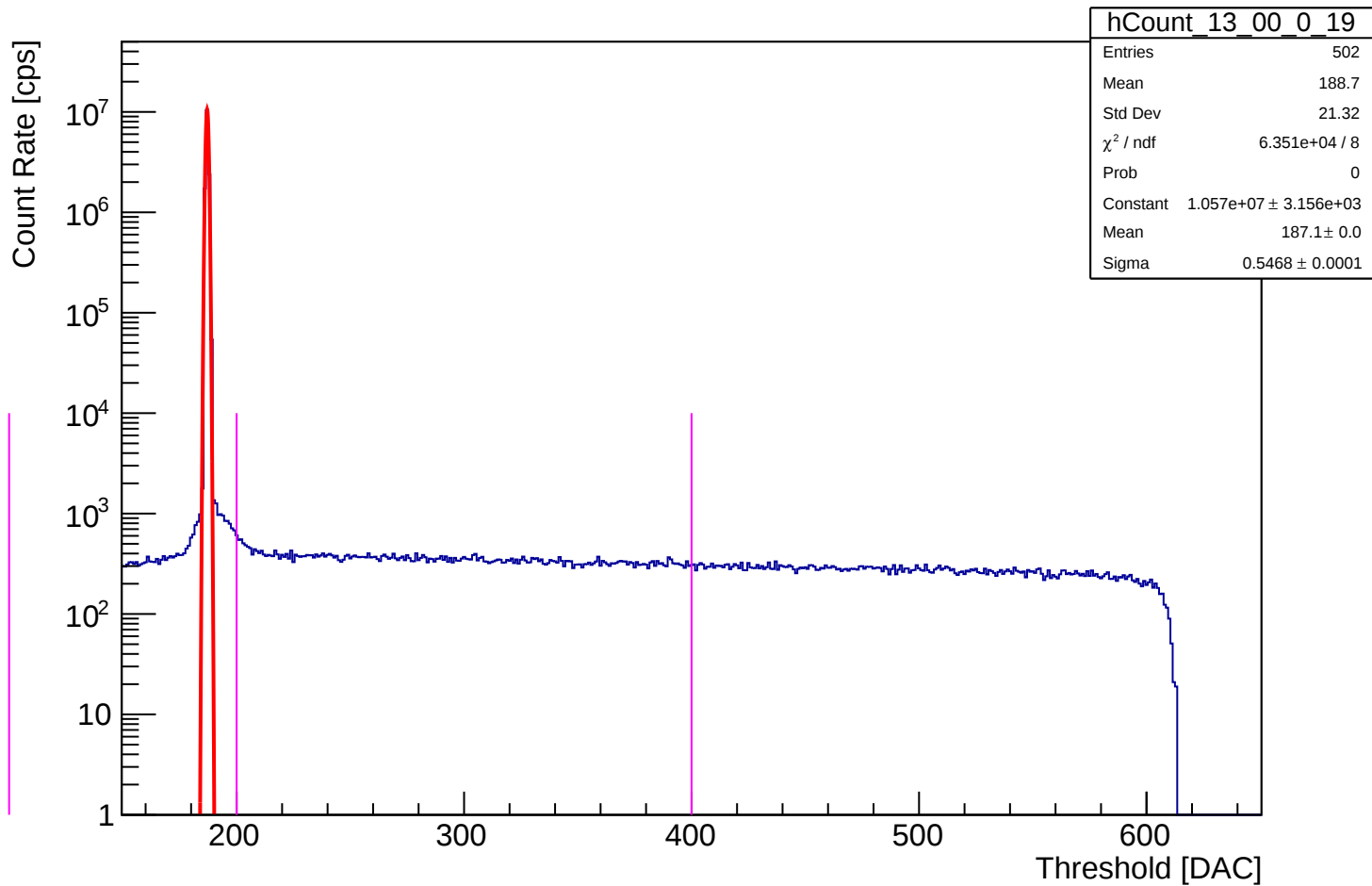
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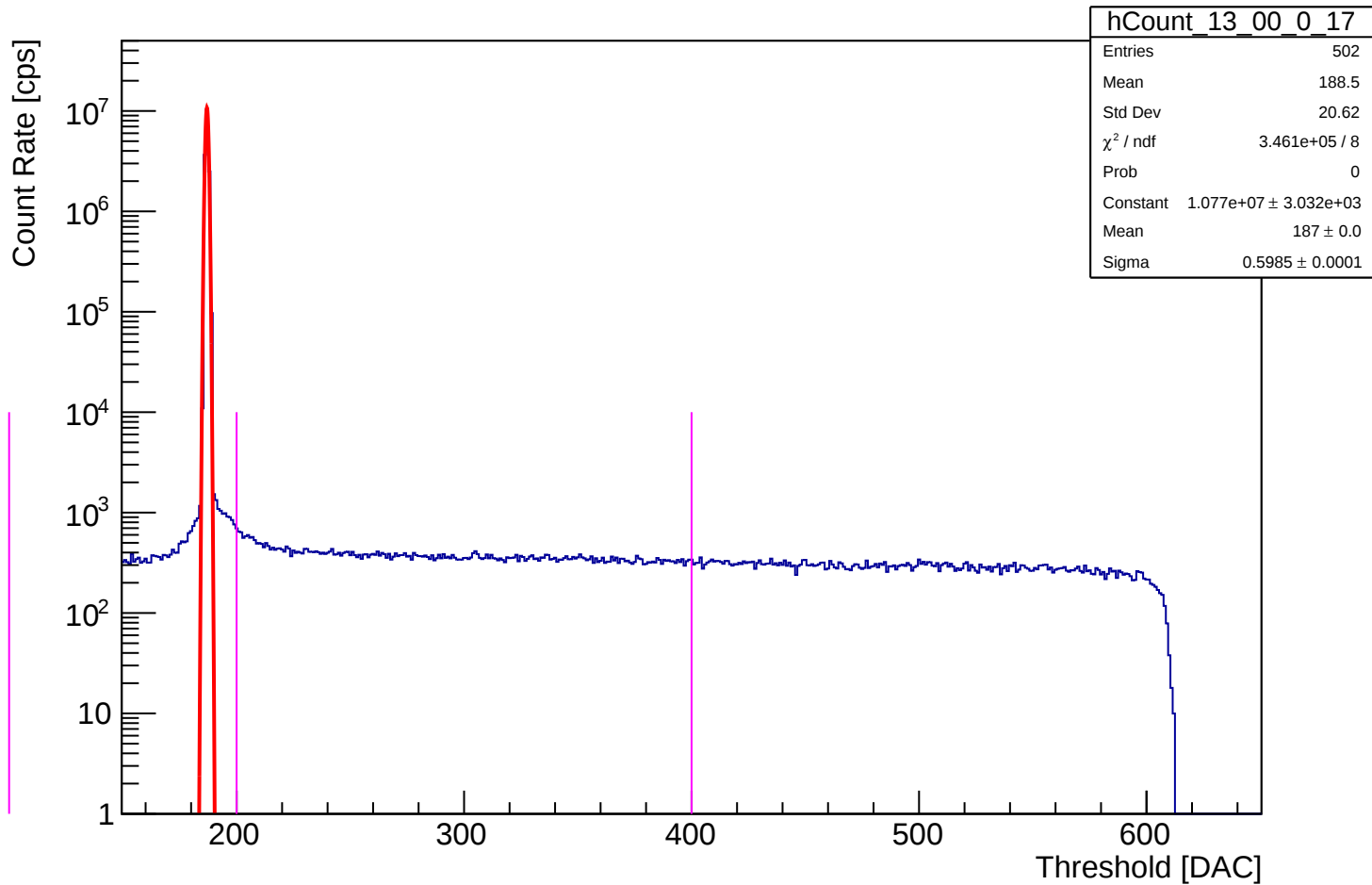
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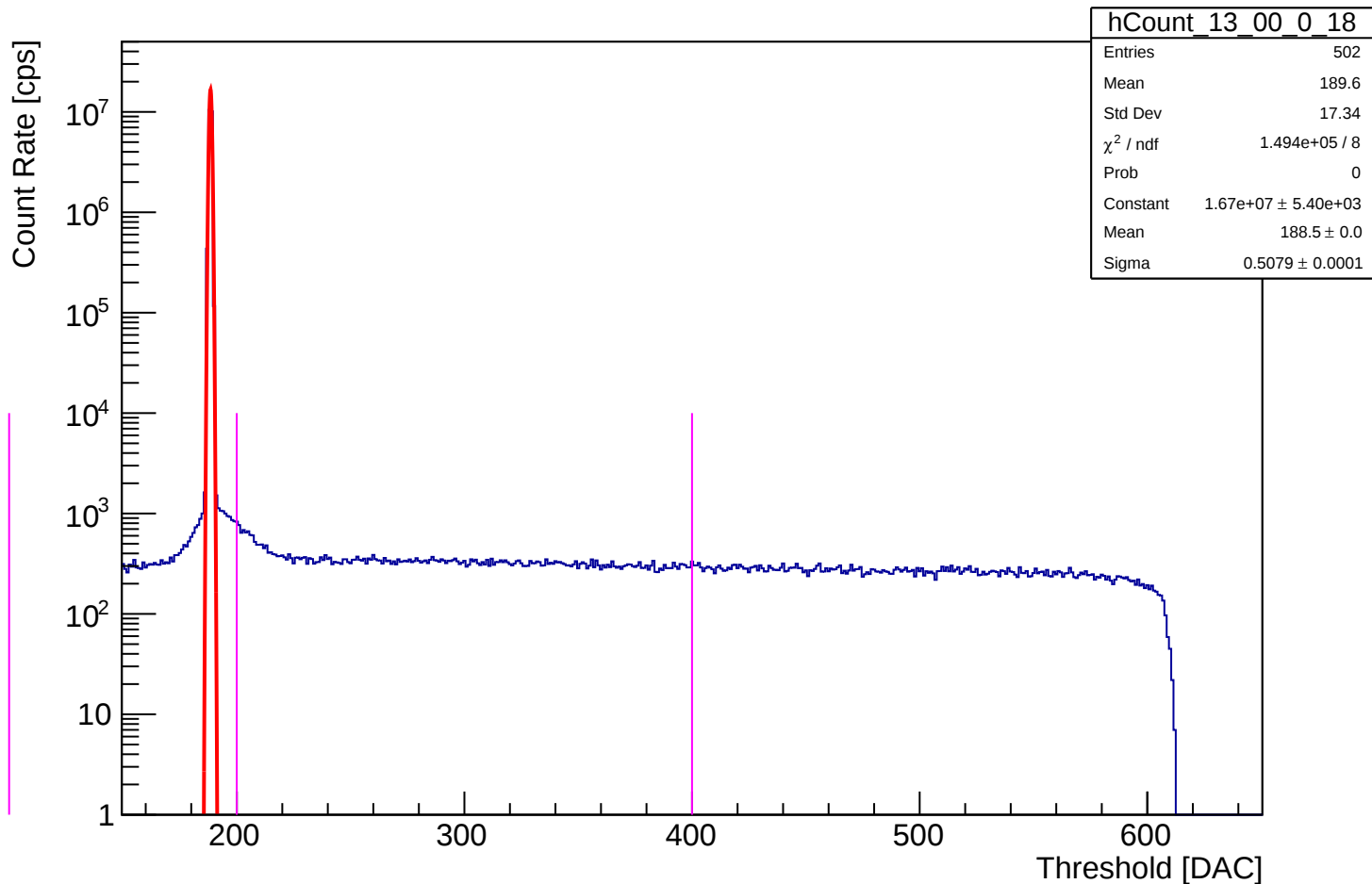
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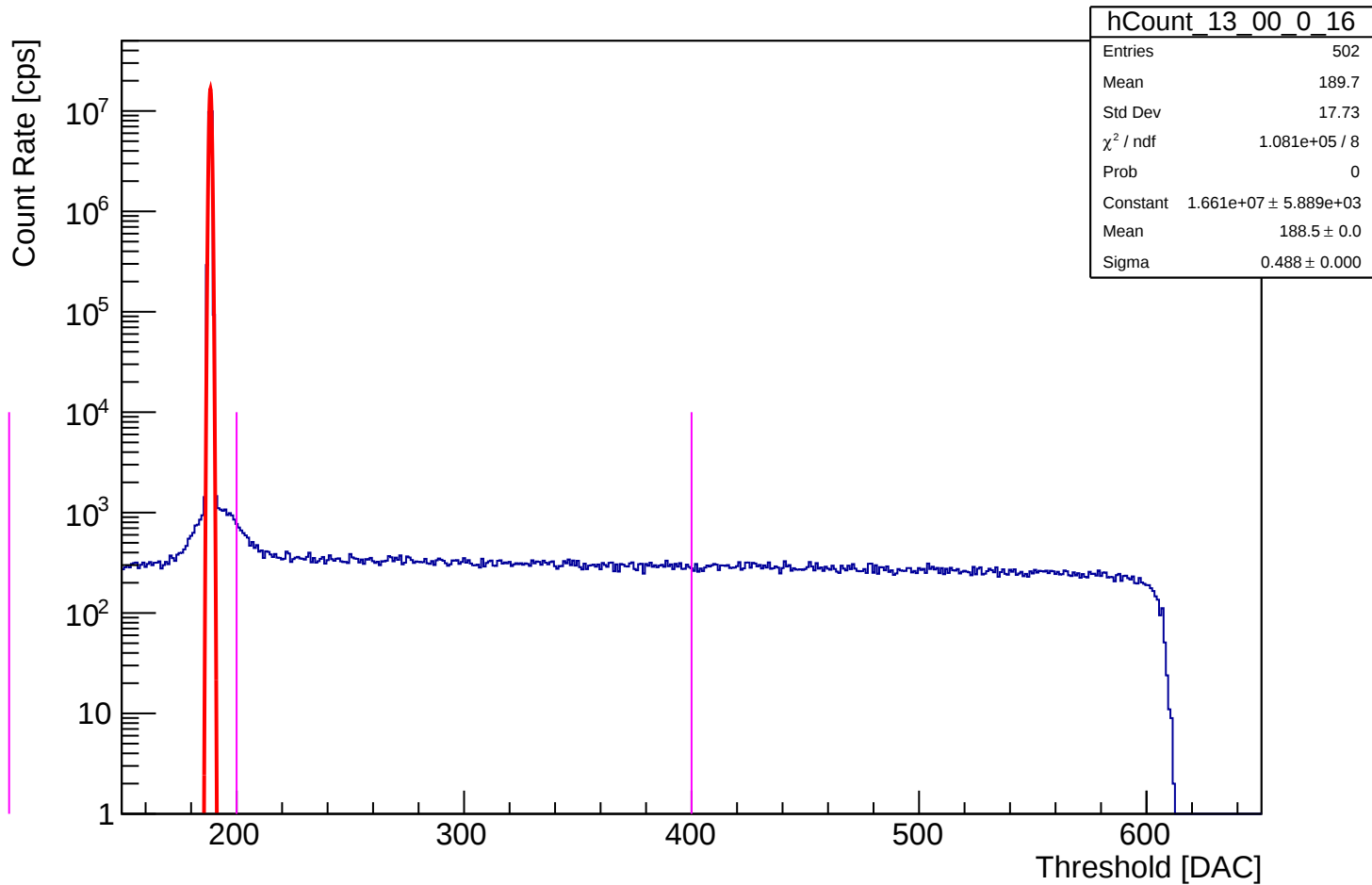
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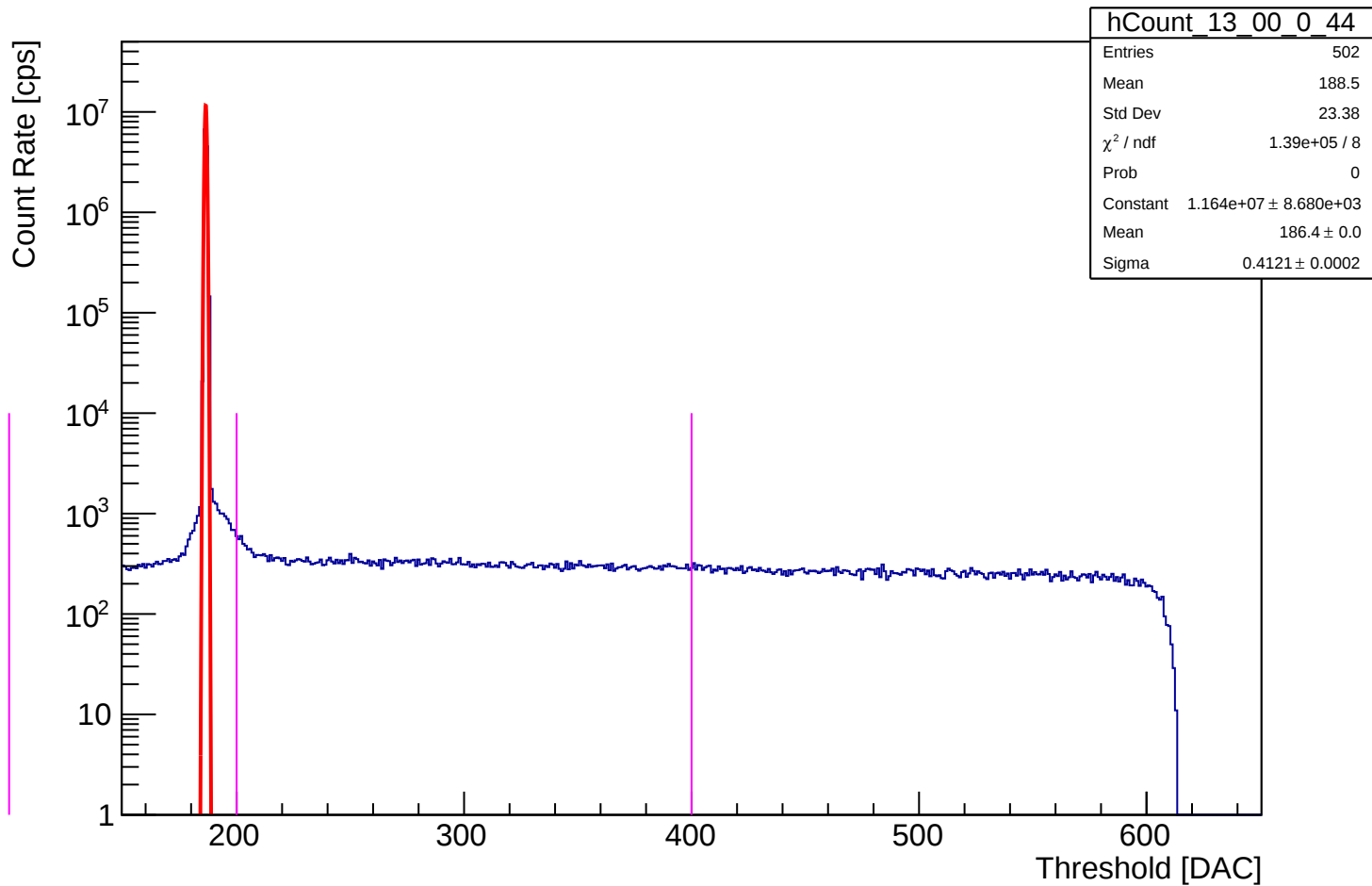
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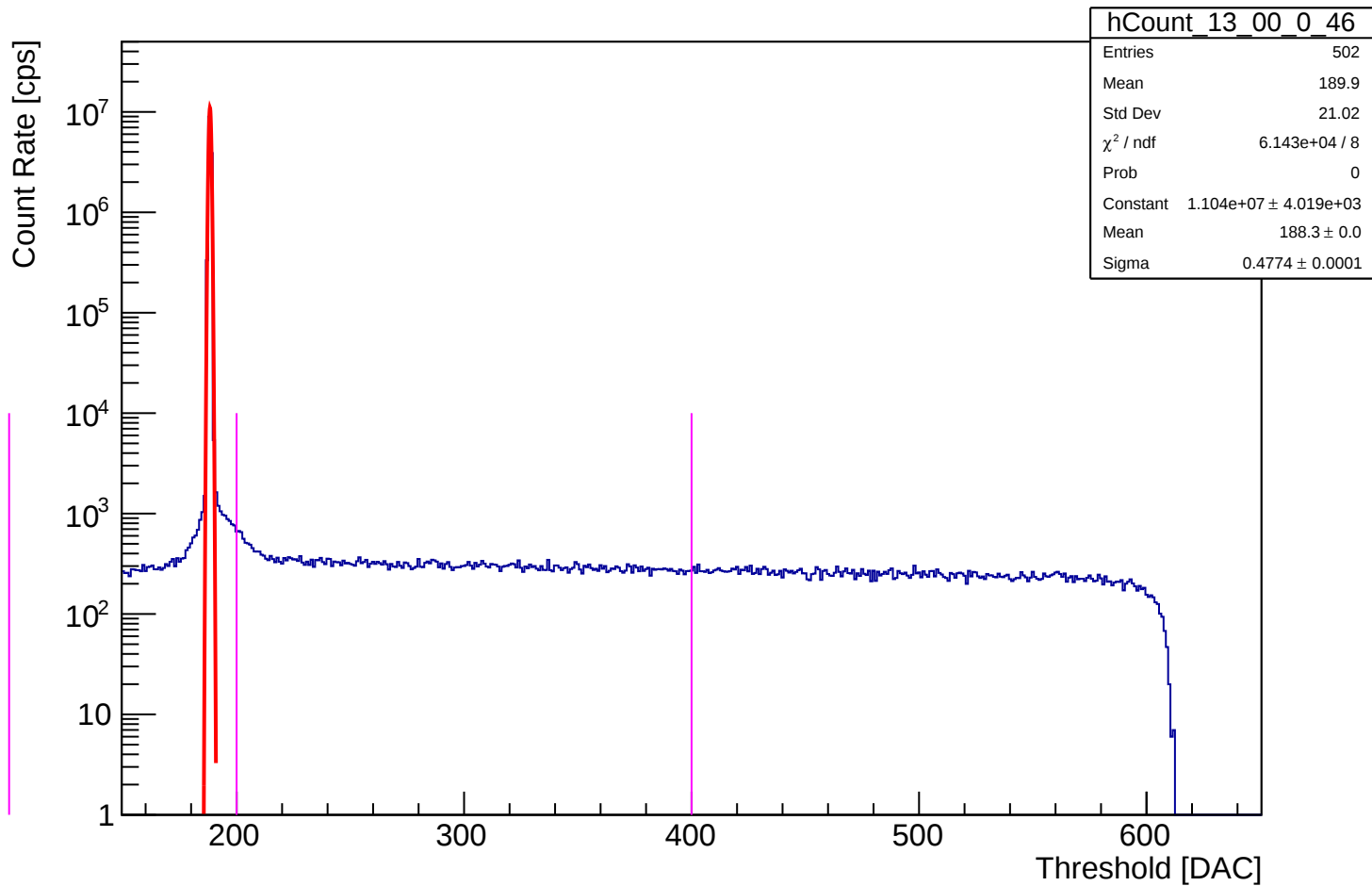
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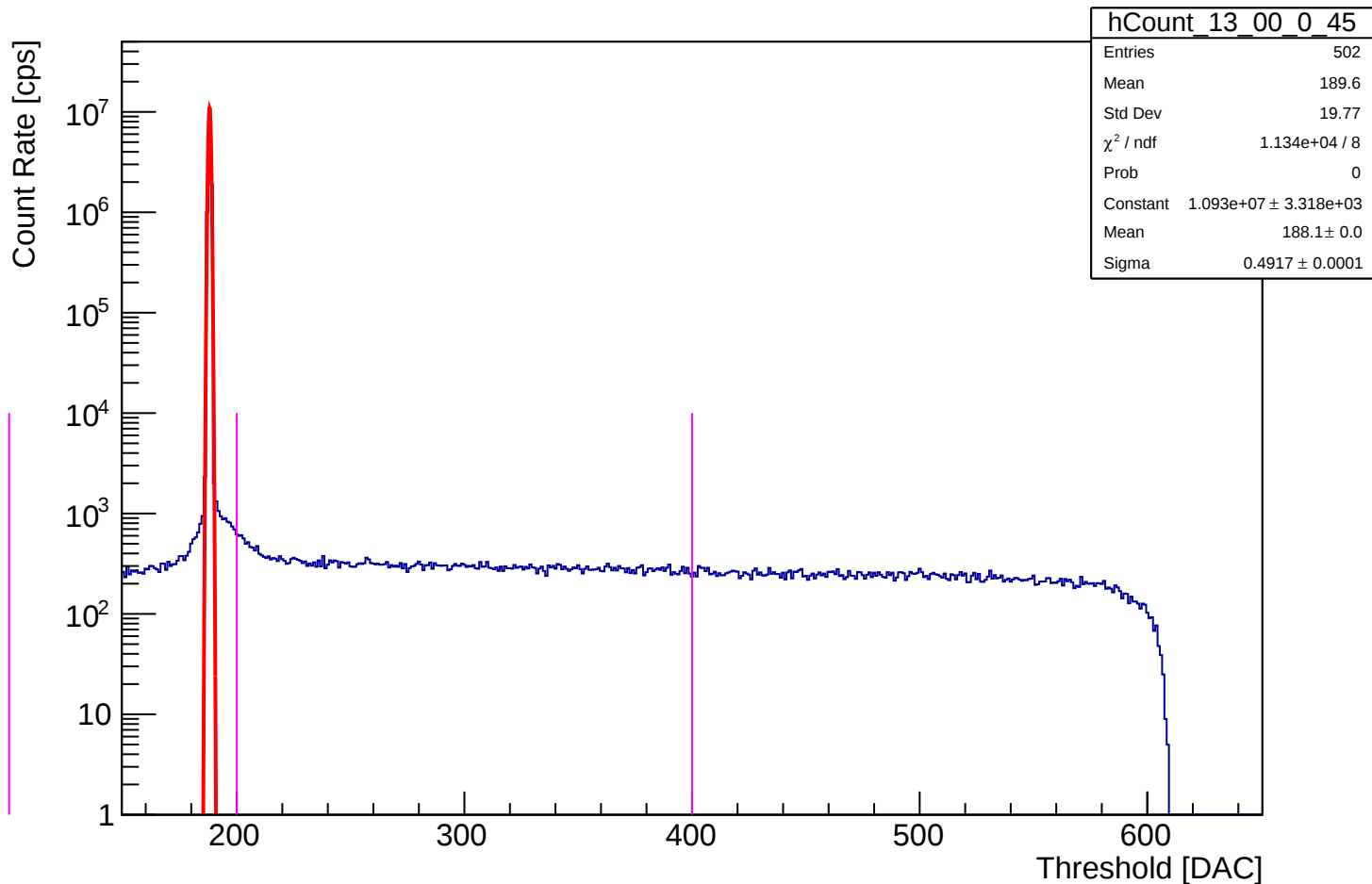
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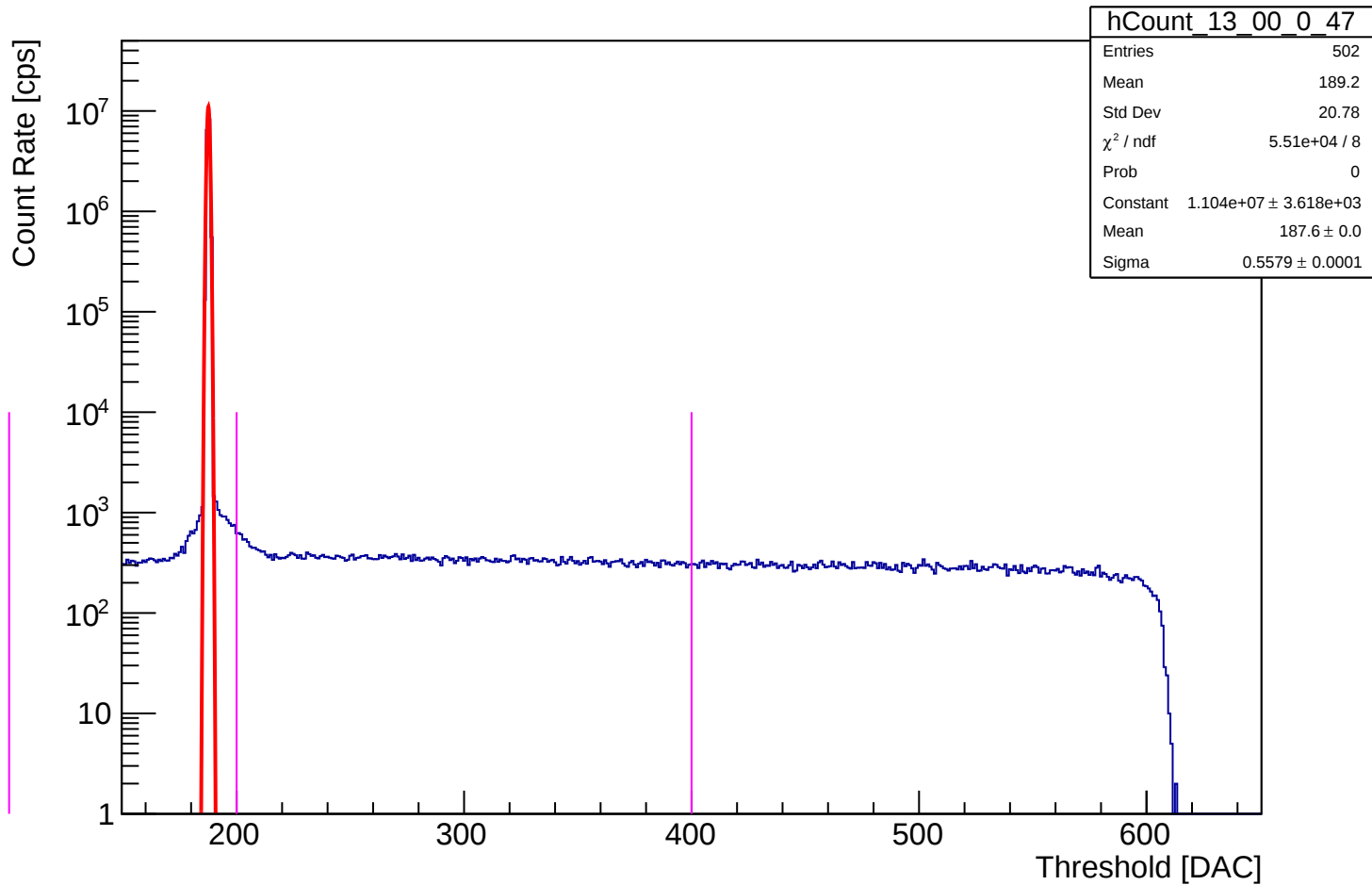
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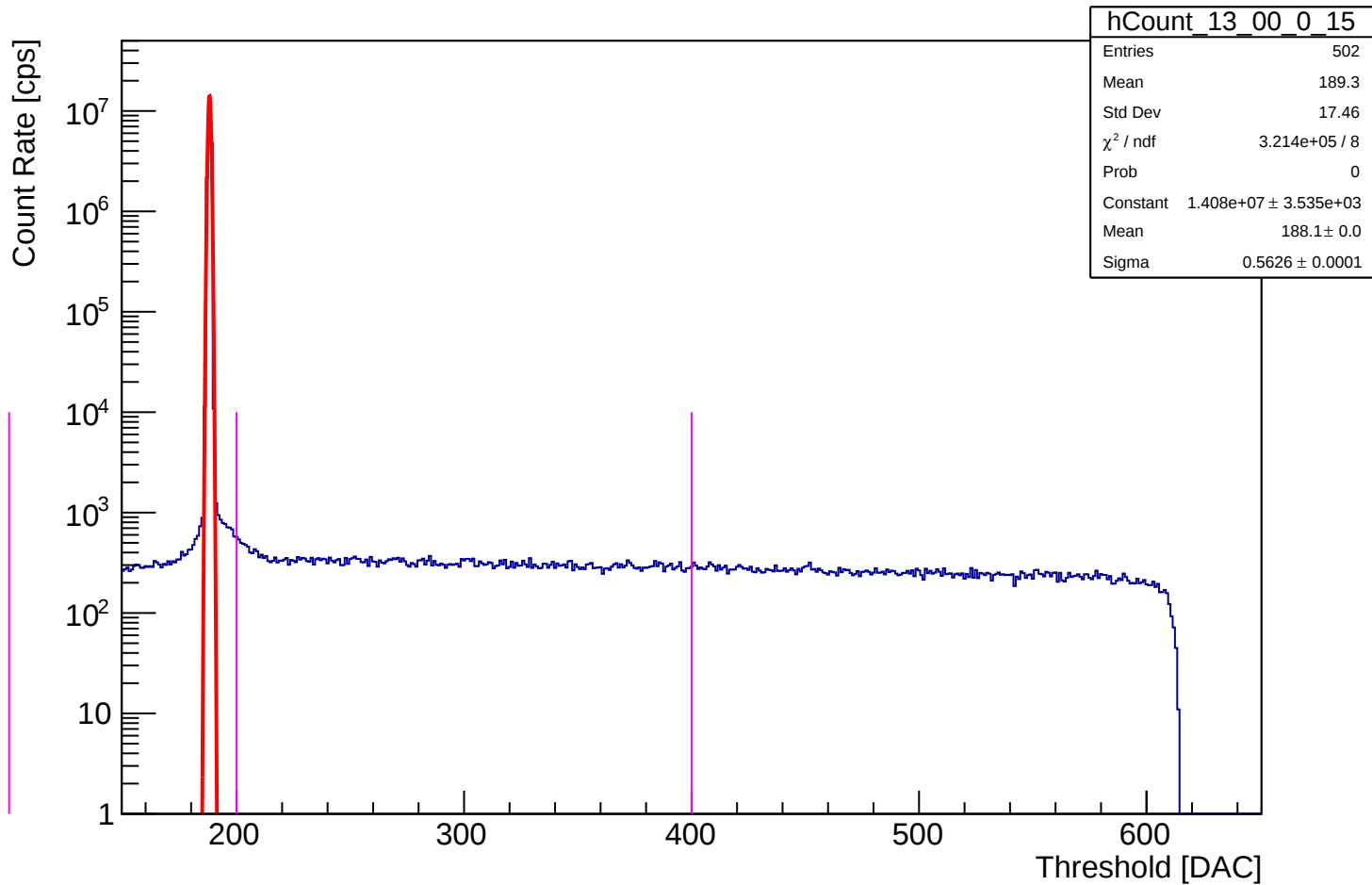
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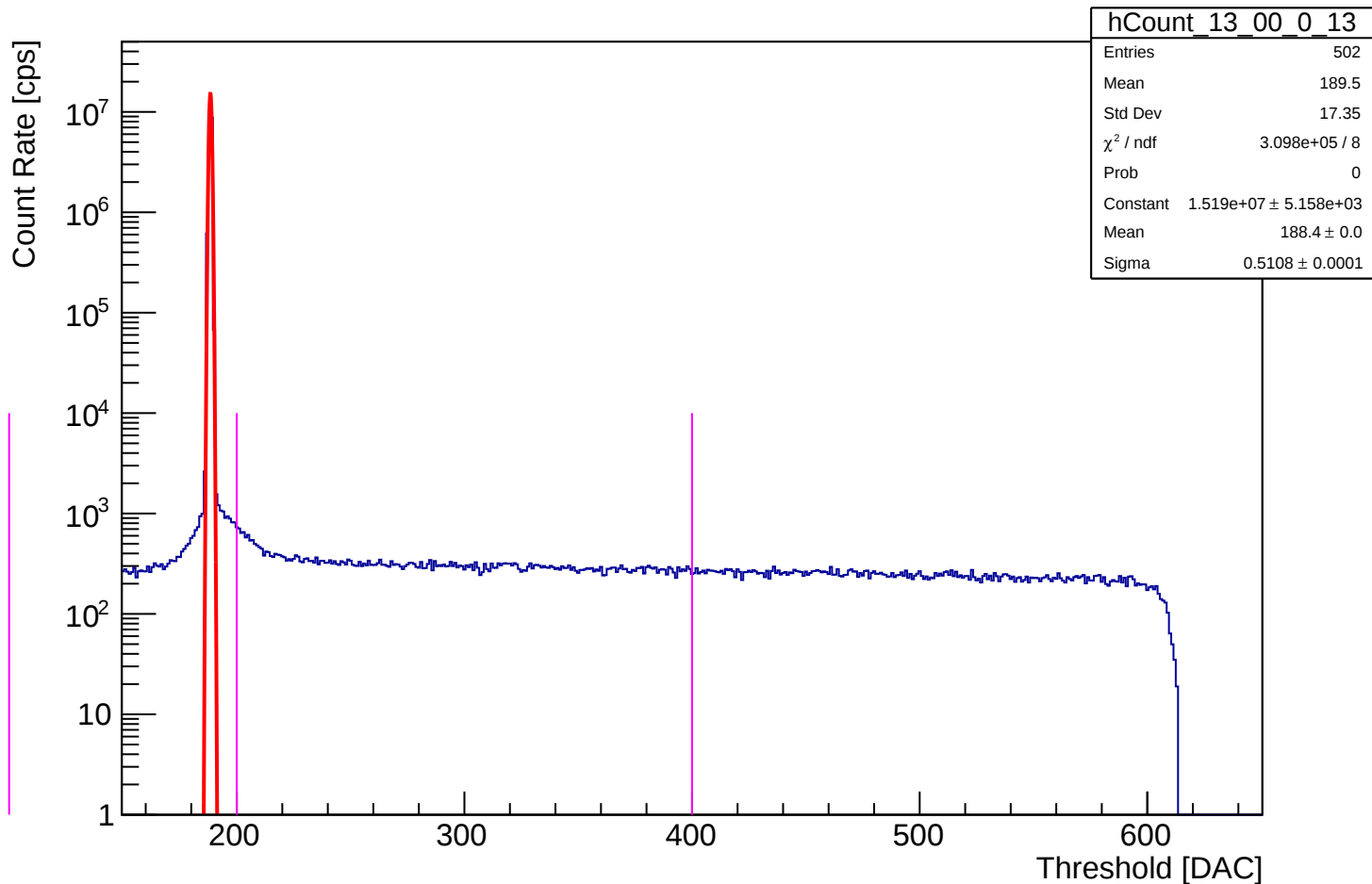
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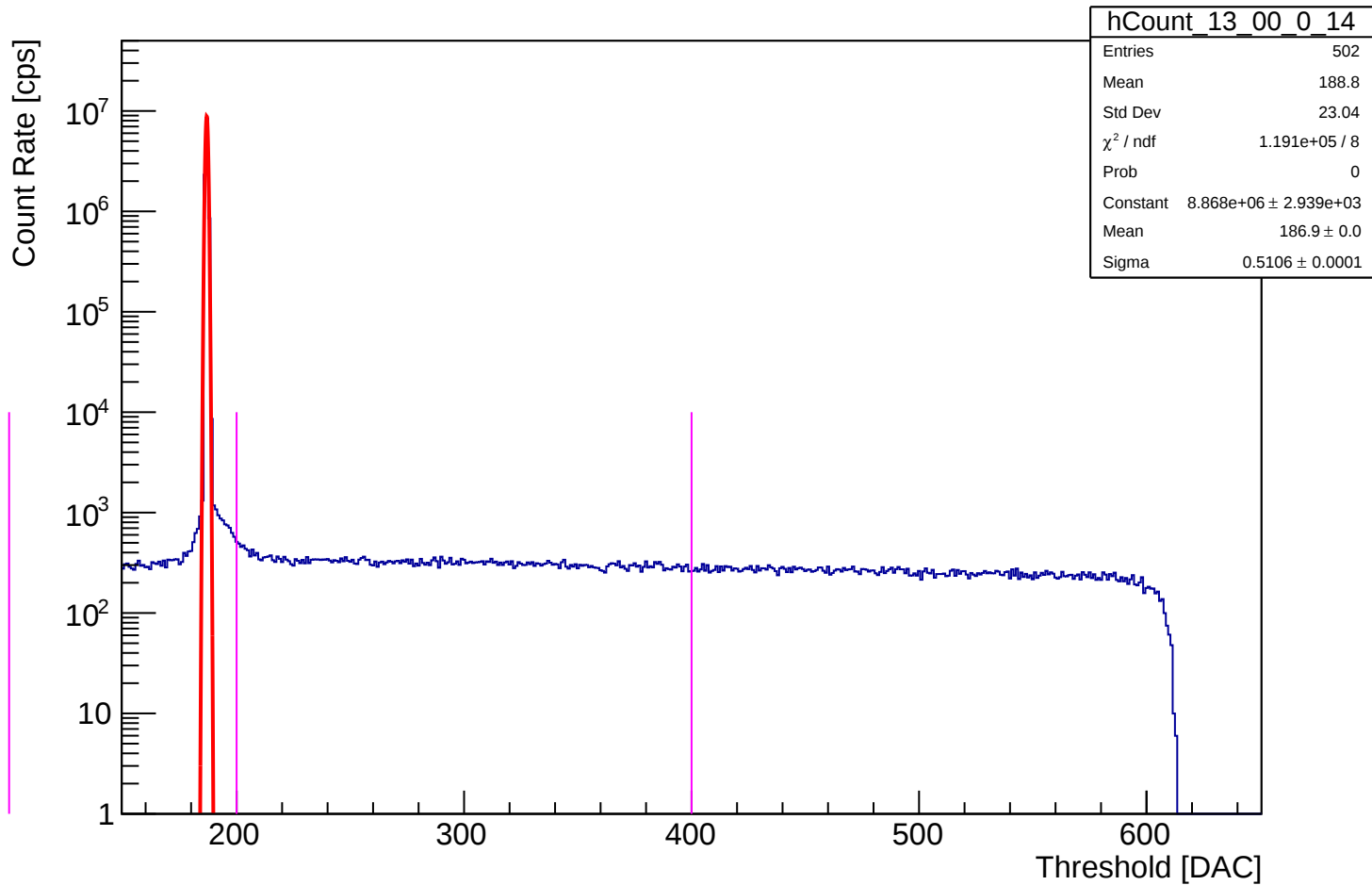
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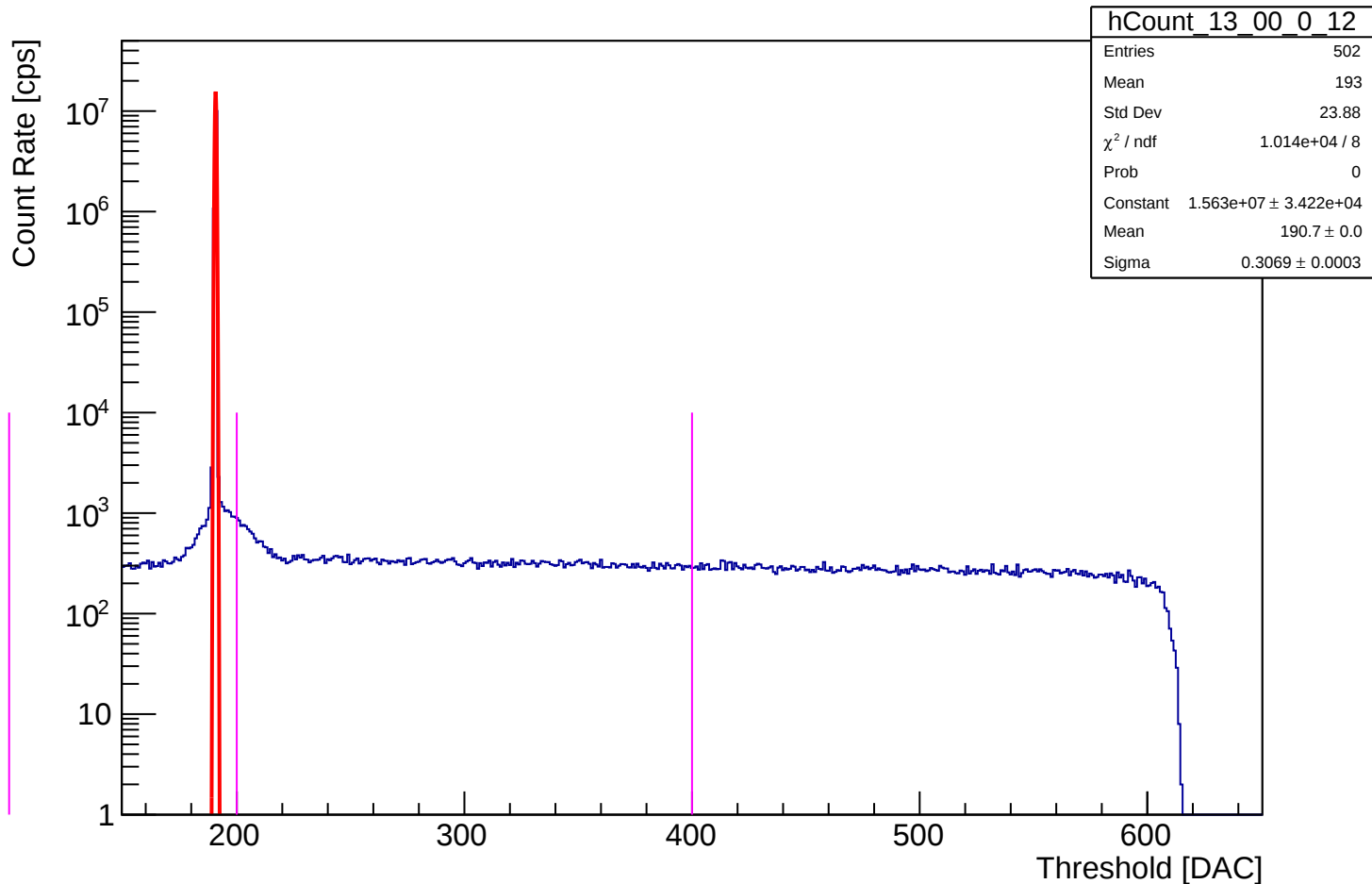
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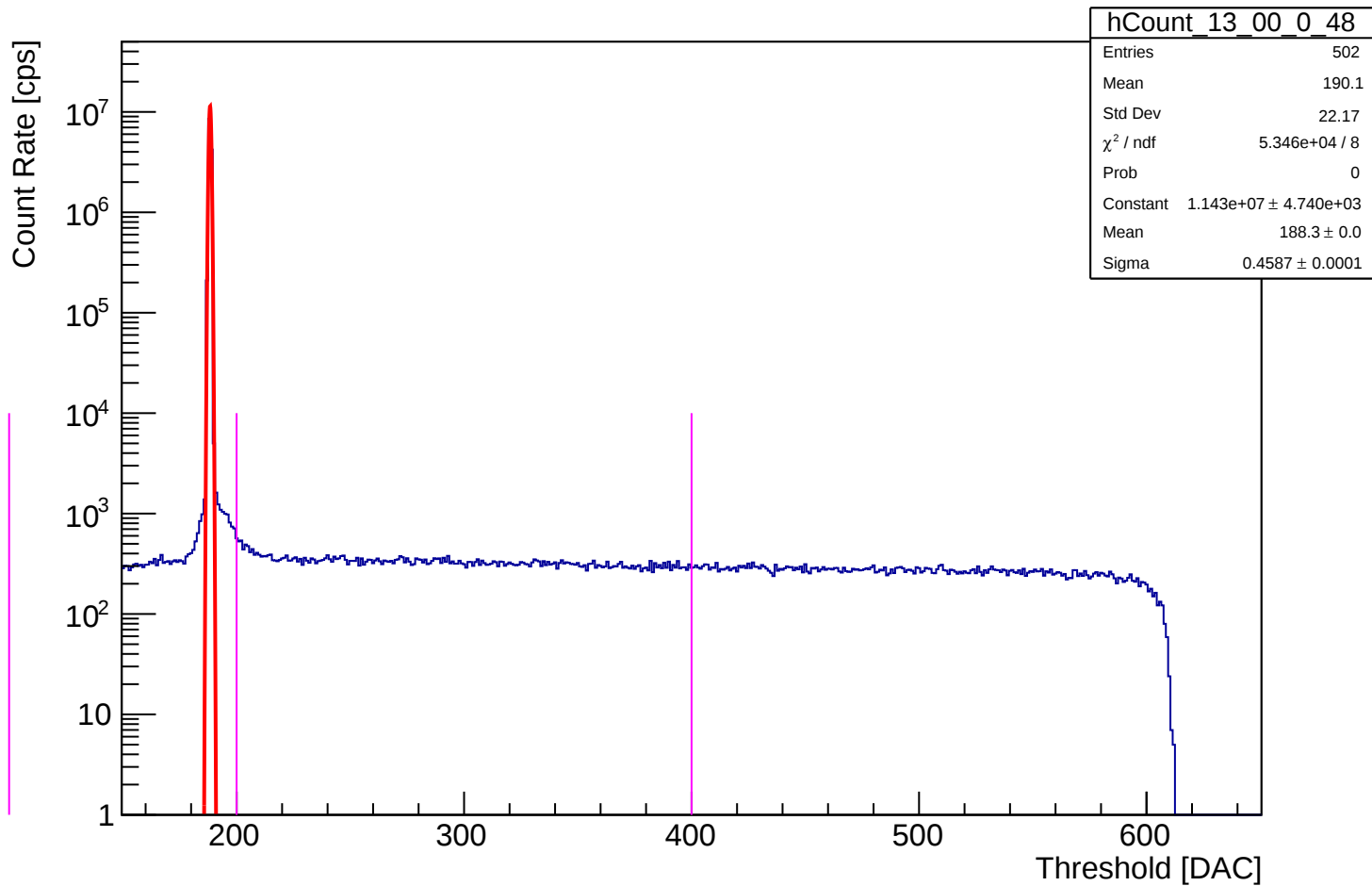
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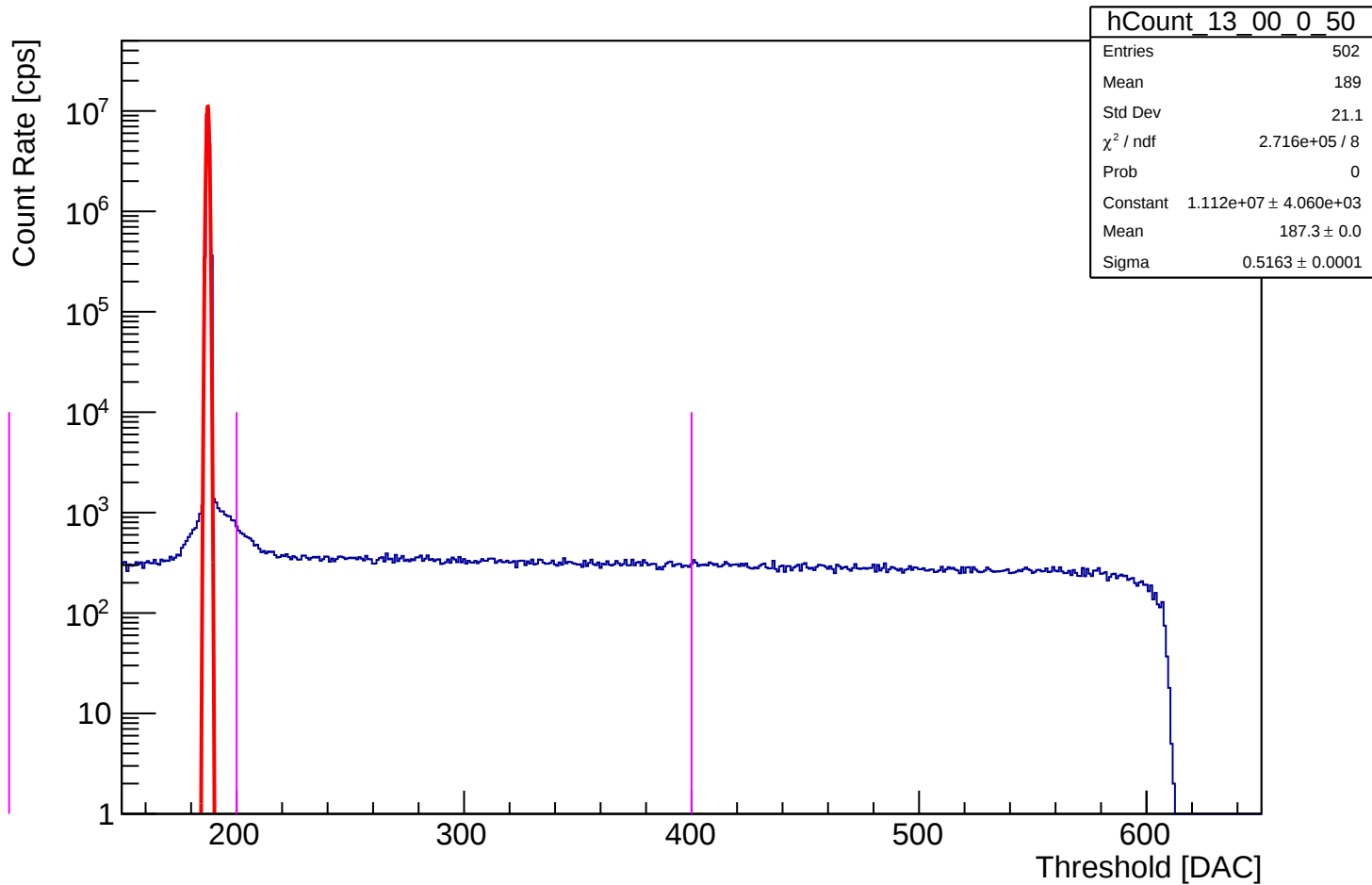
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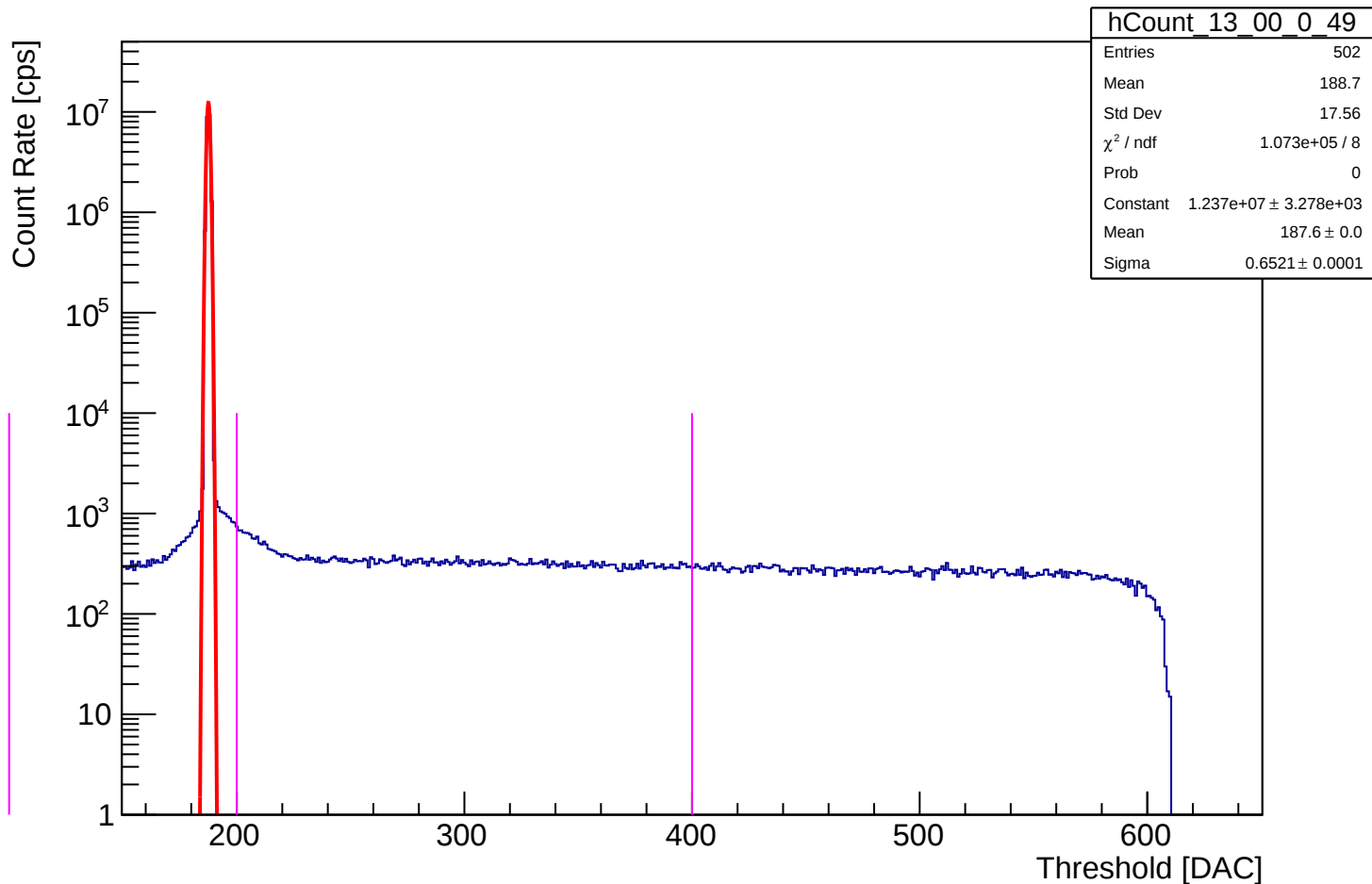
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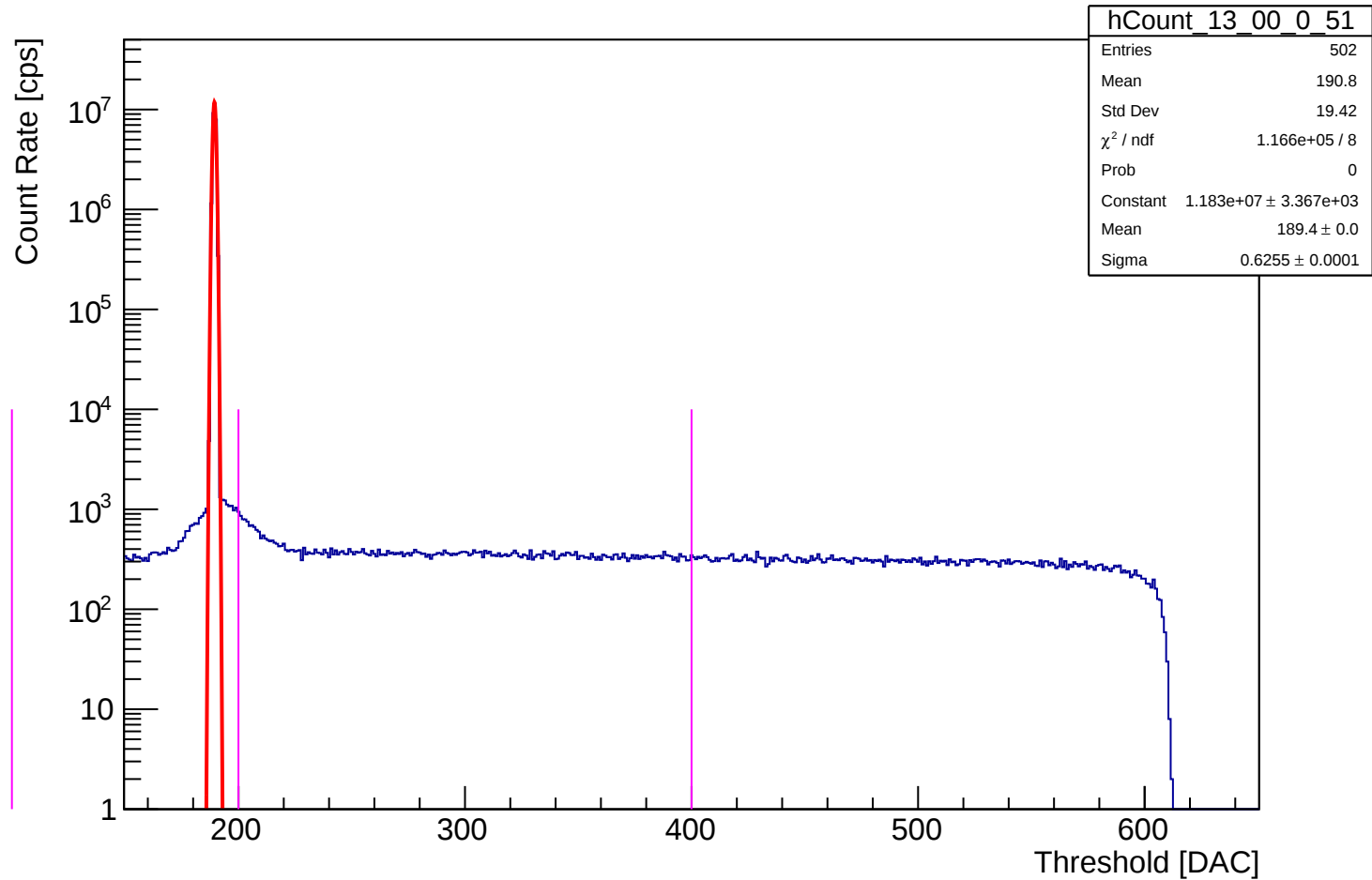


Row 1 Tile 1 Pmt 1 Pixel 38 Slot 13 Fiber 0 Asic 0 Channel 50

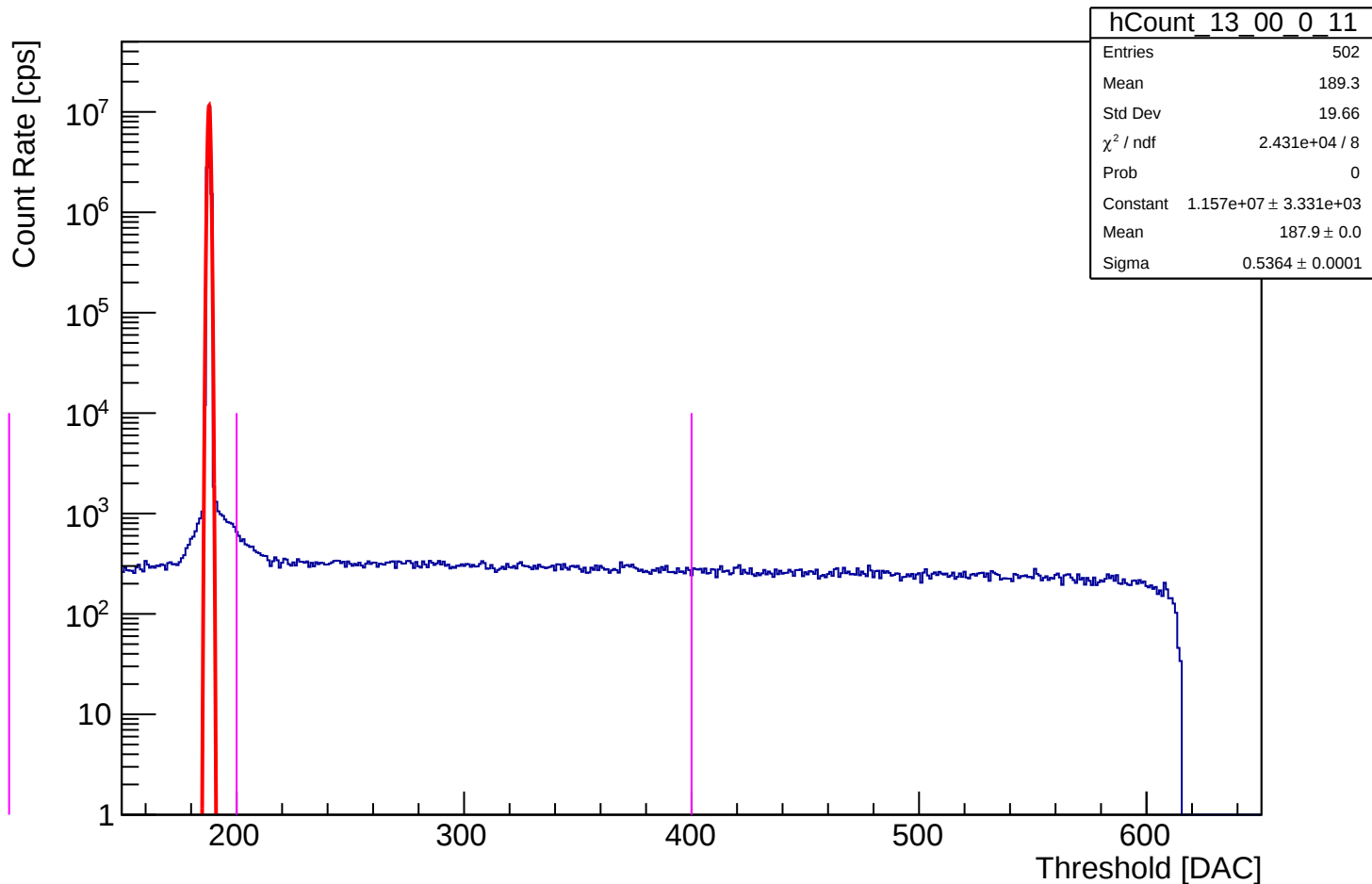


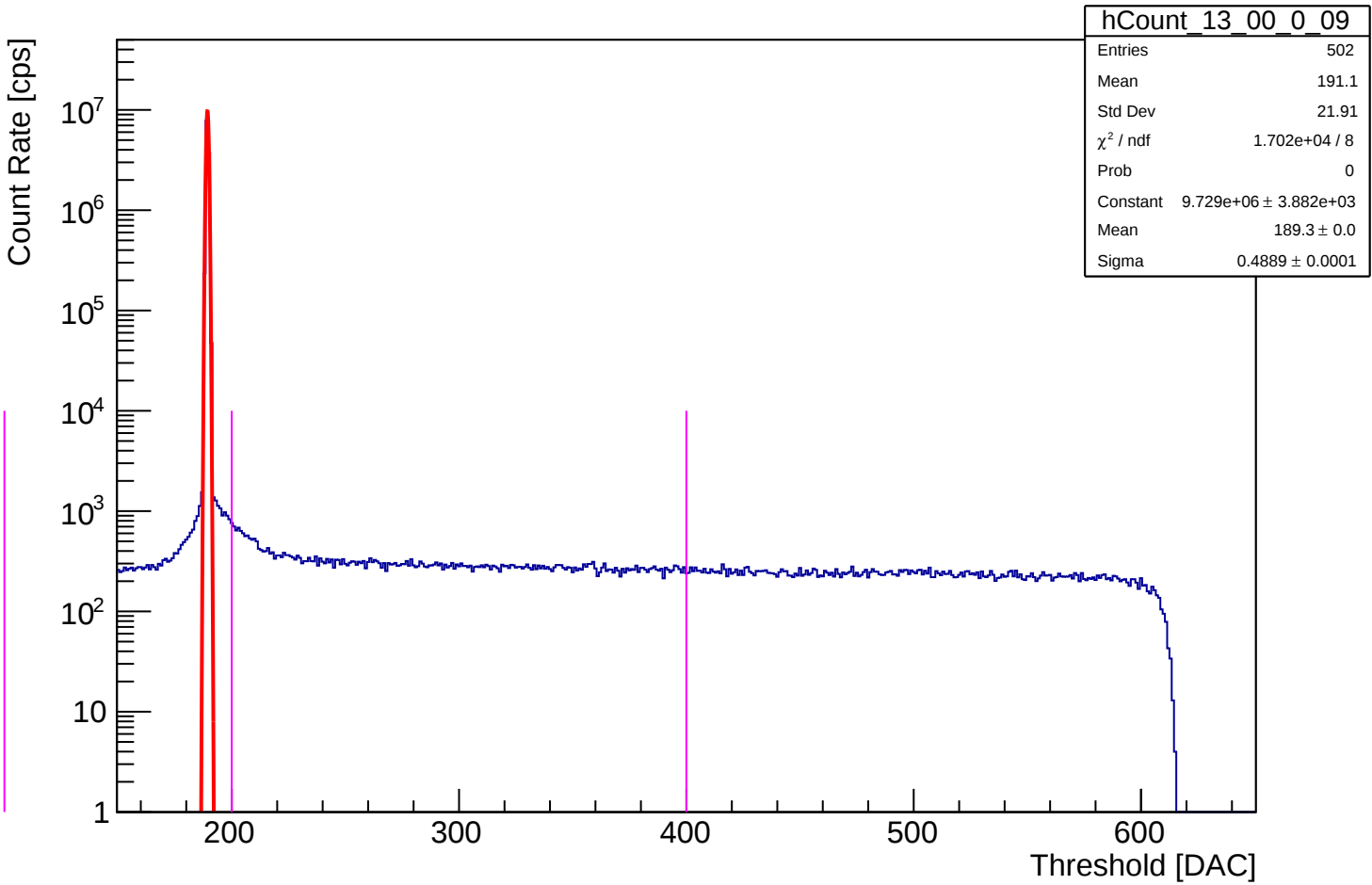
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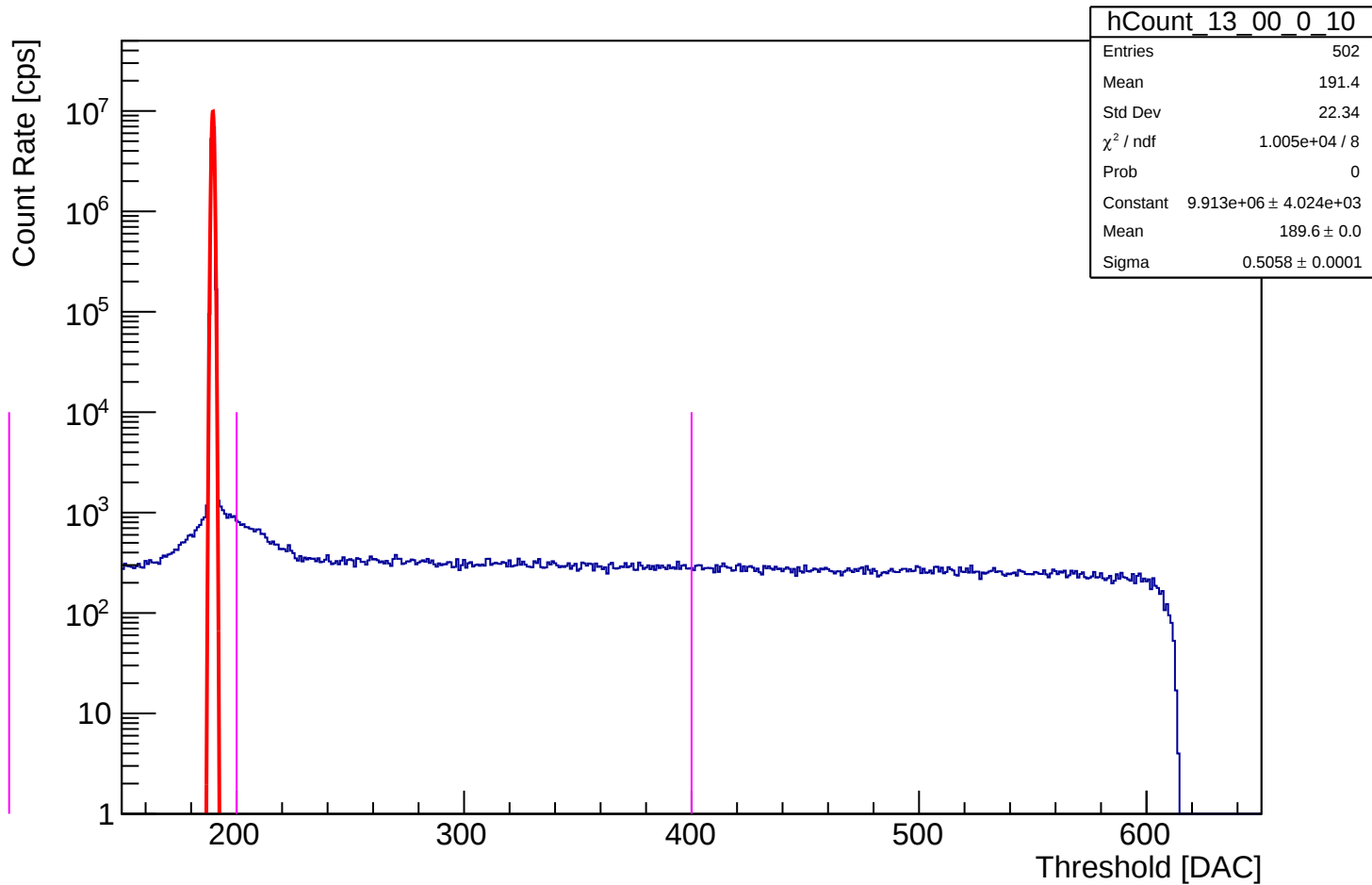


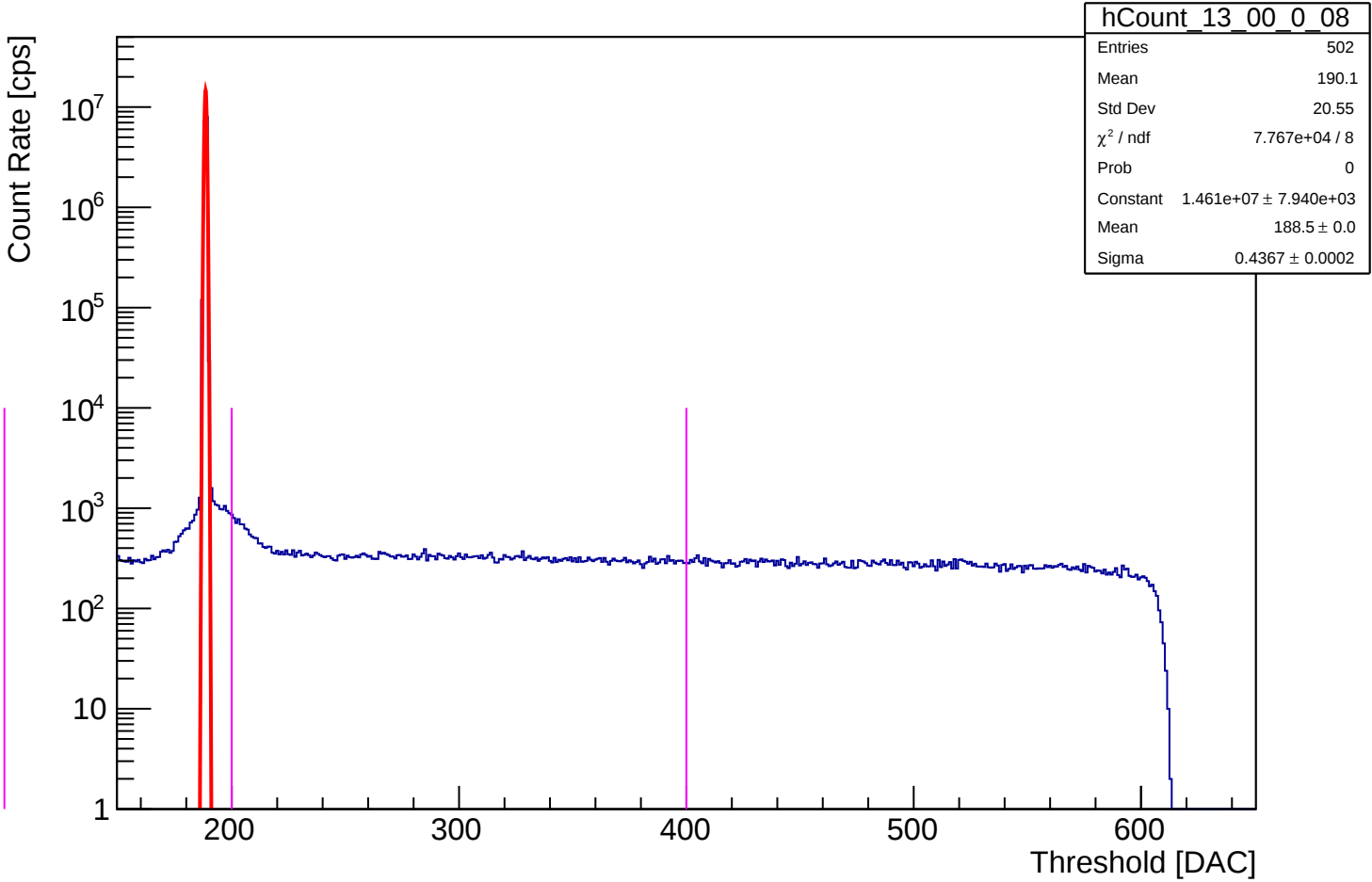
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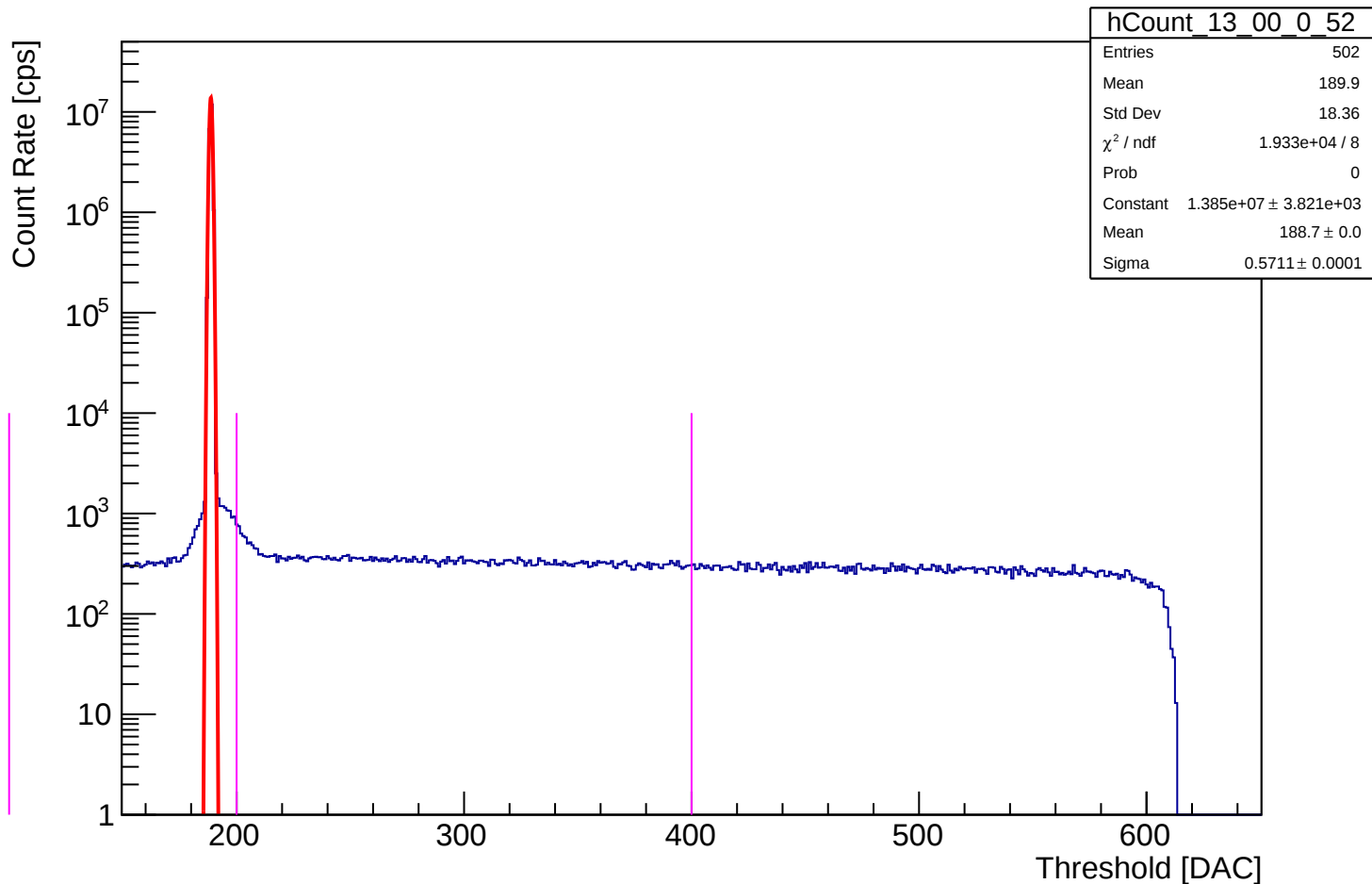


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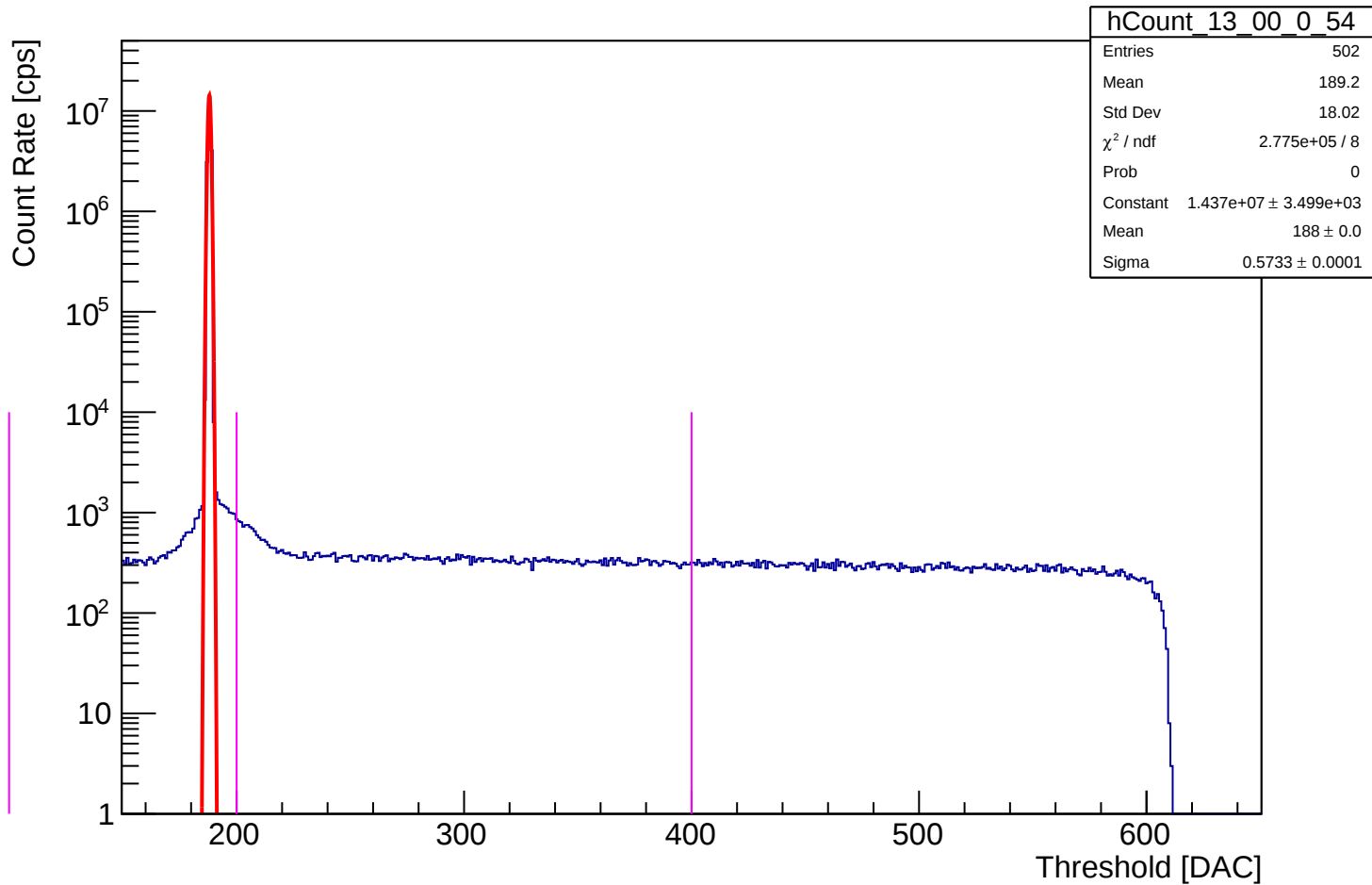




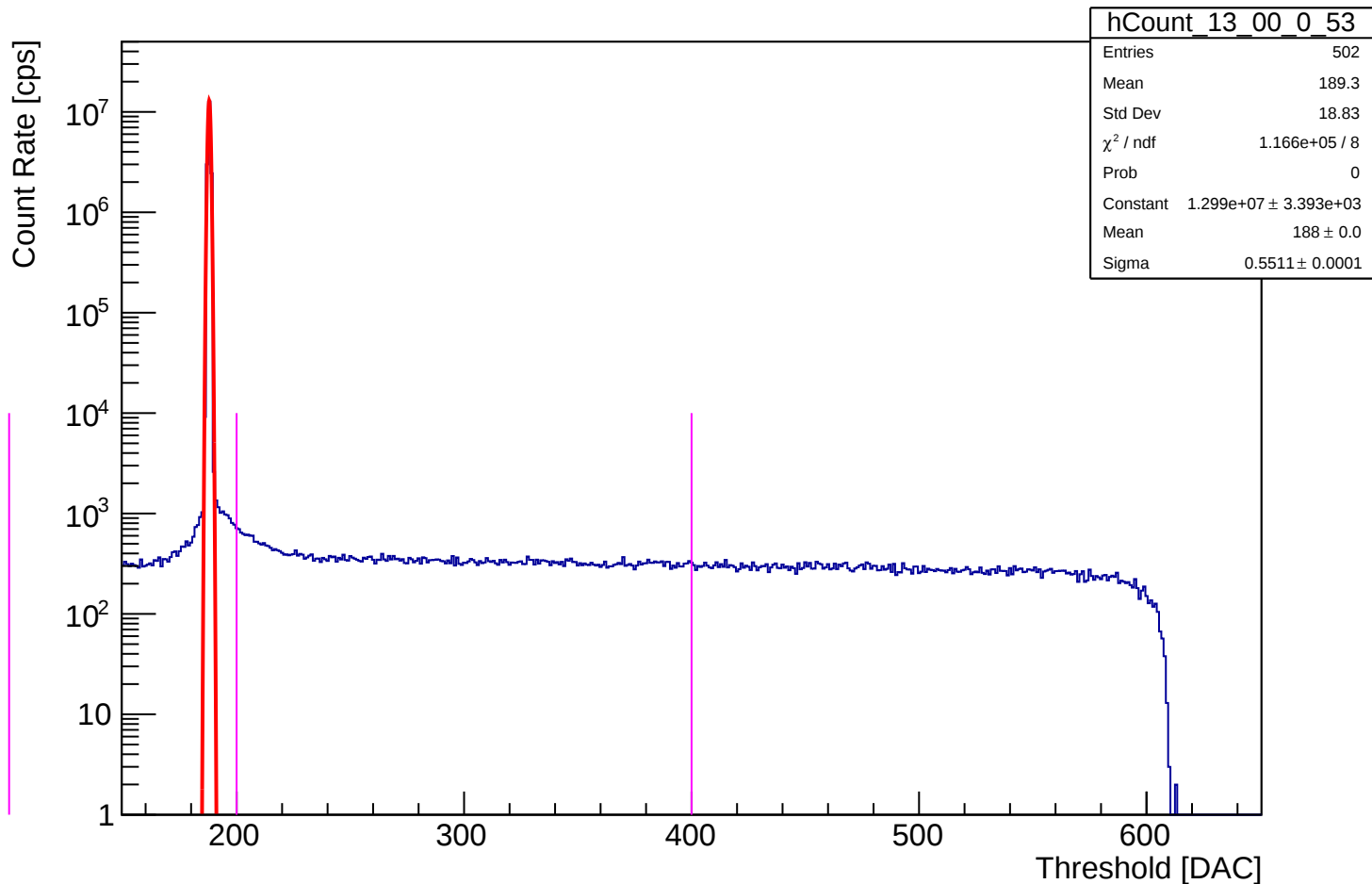
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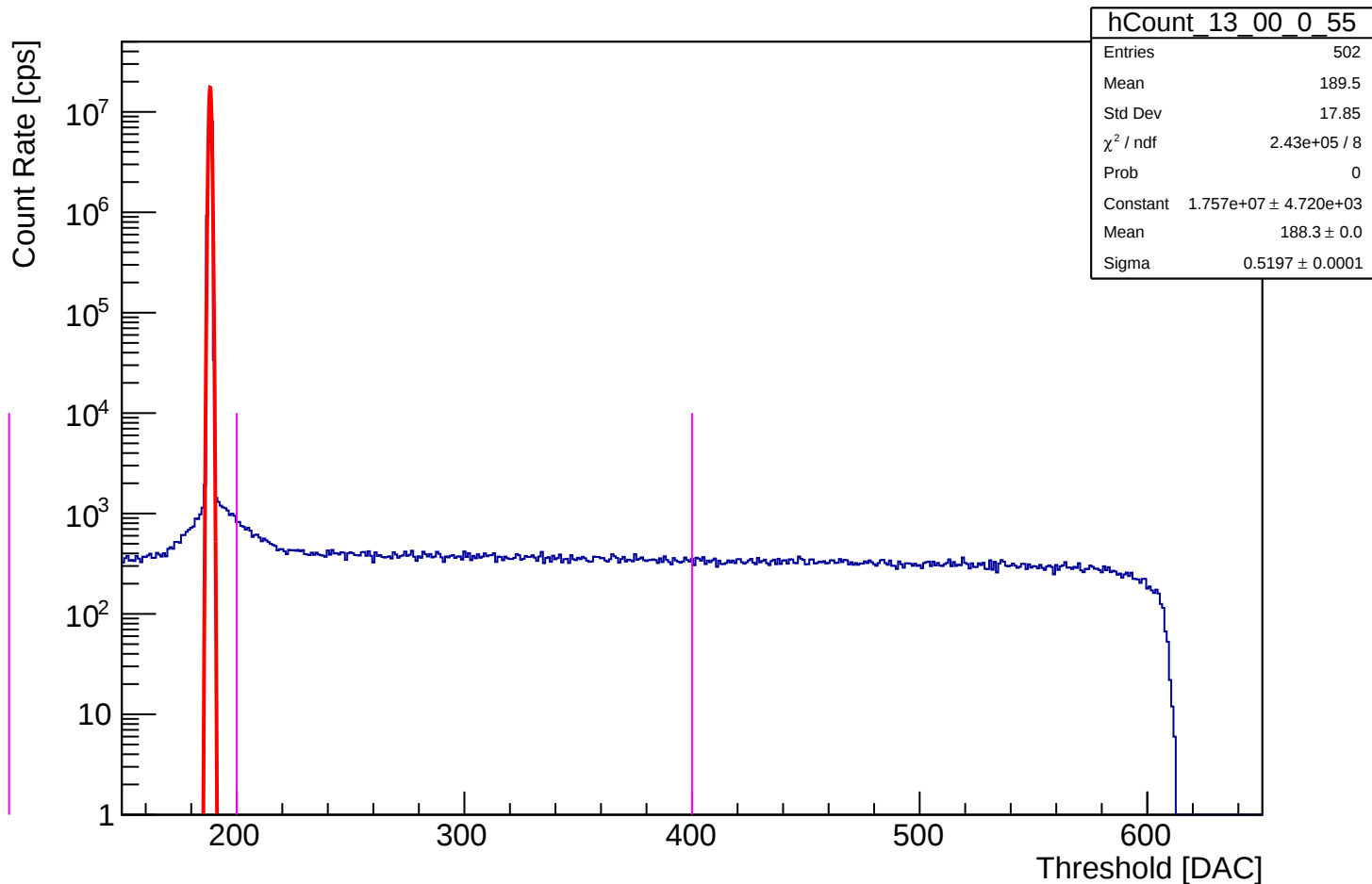
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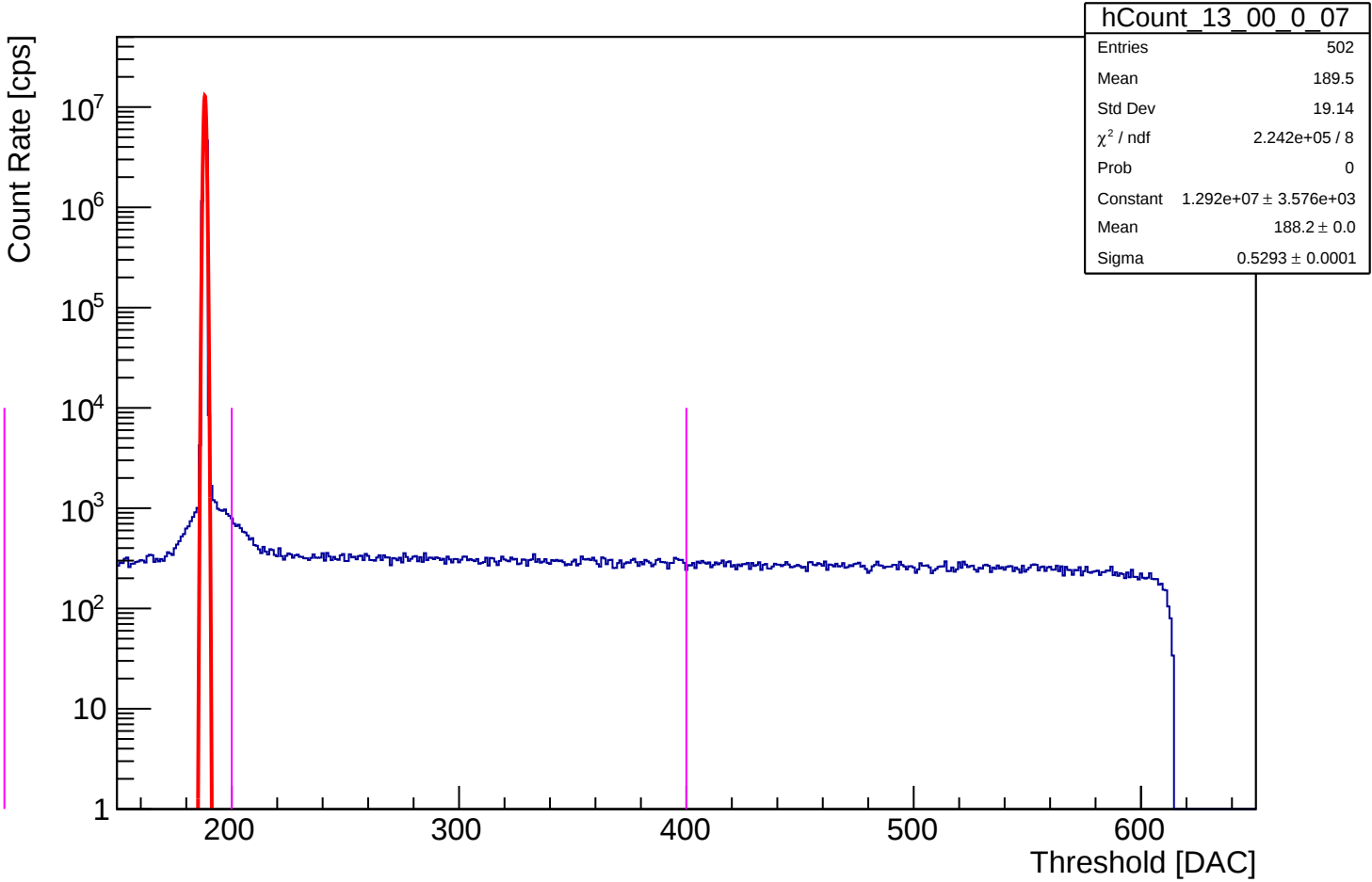


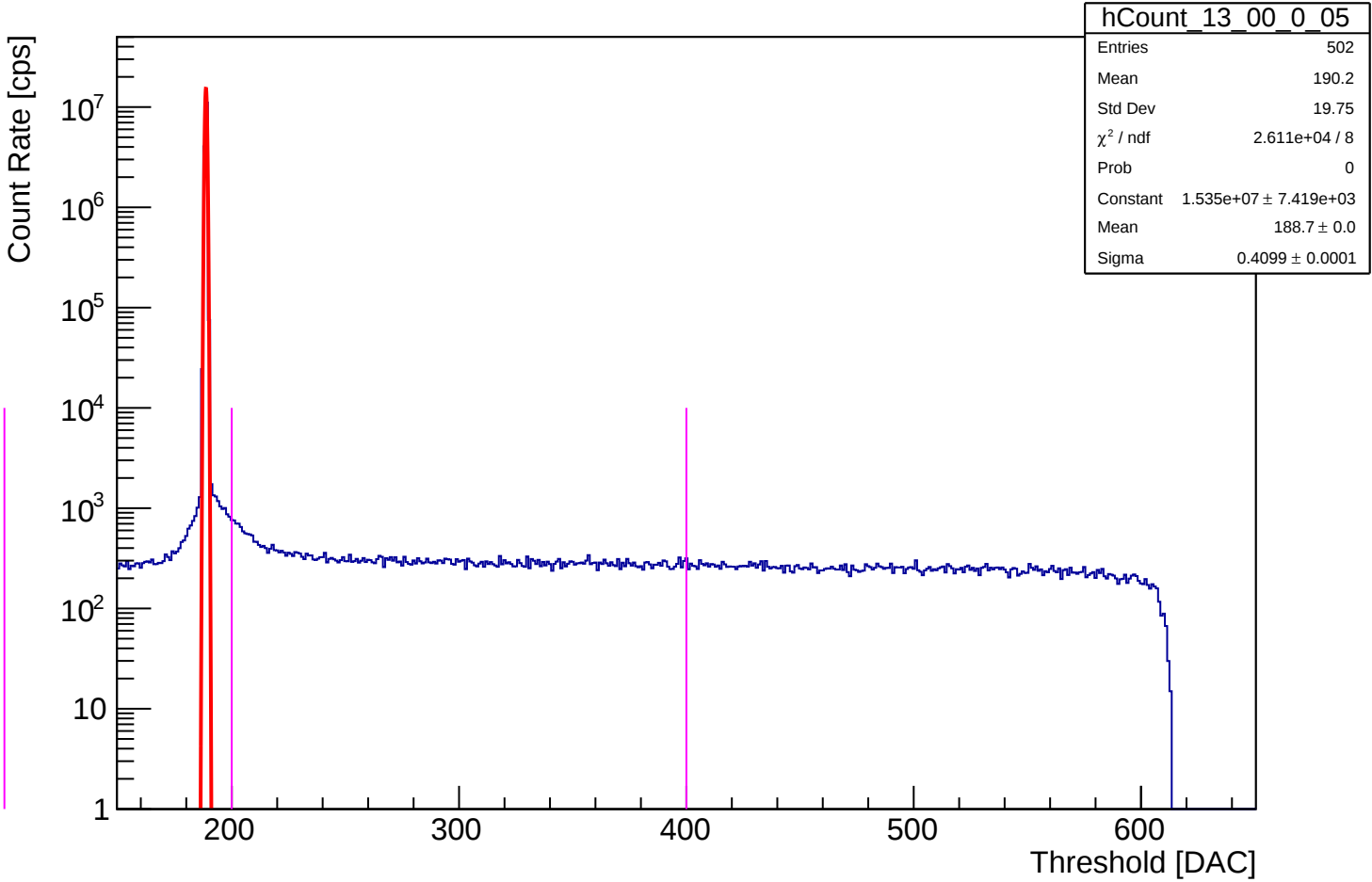
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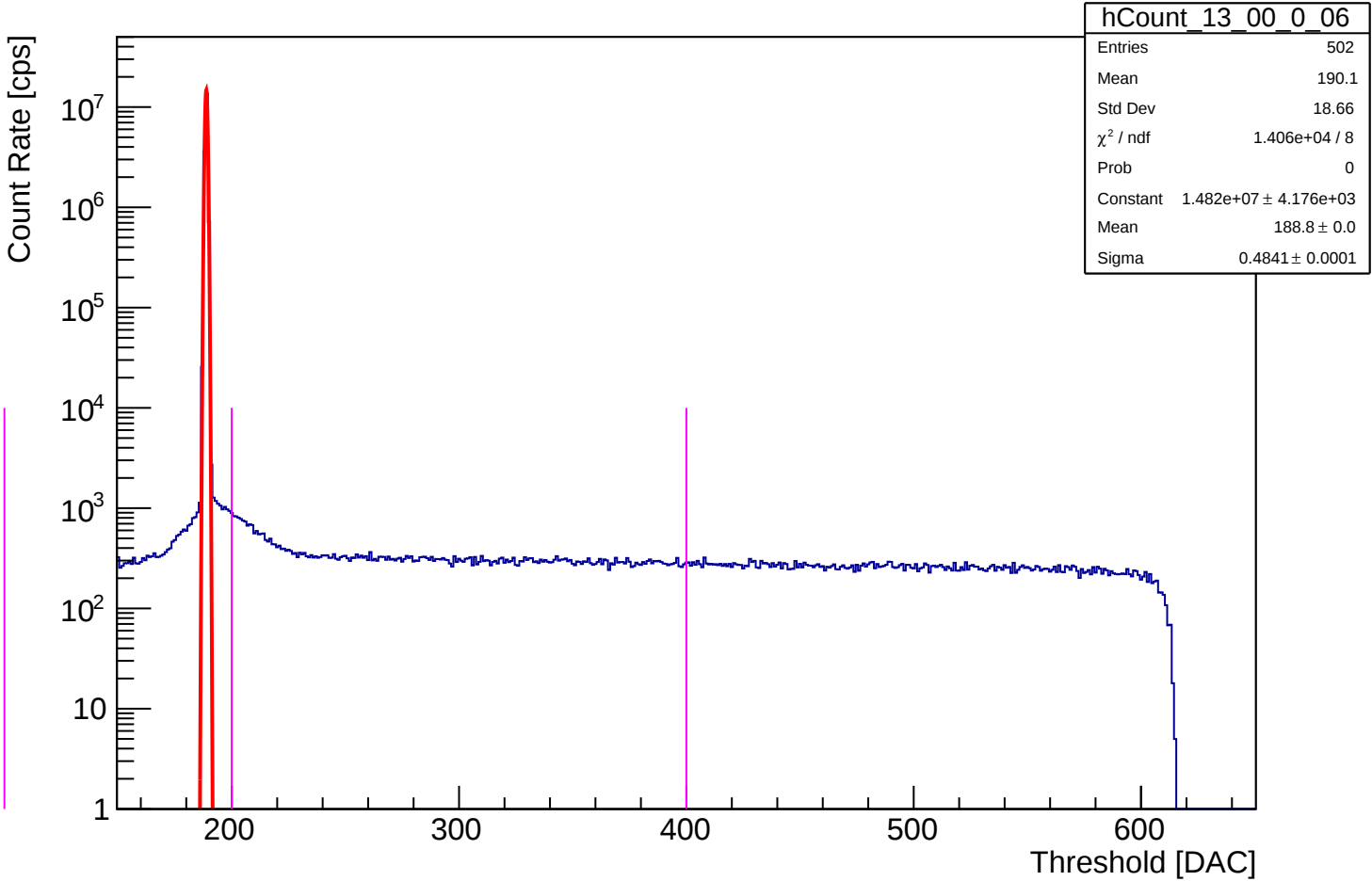


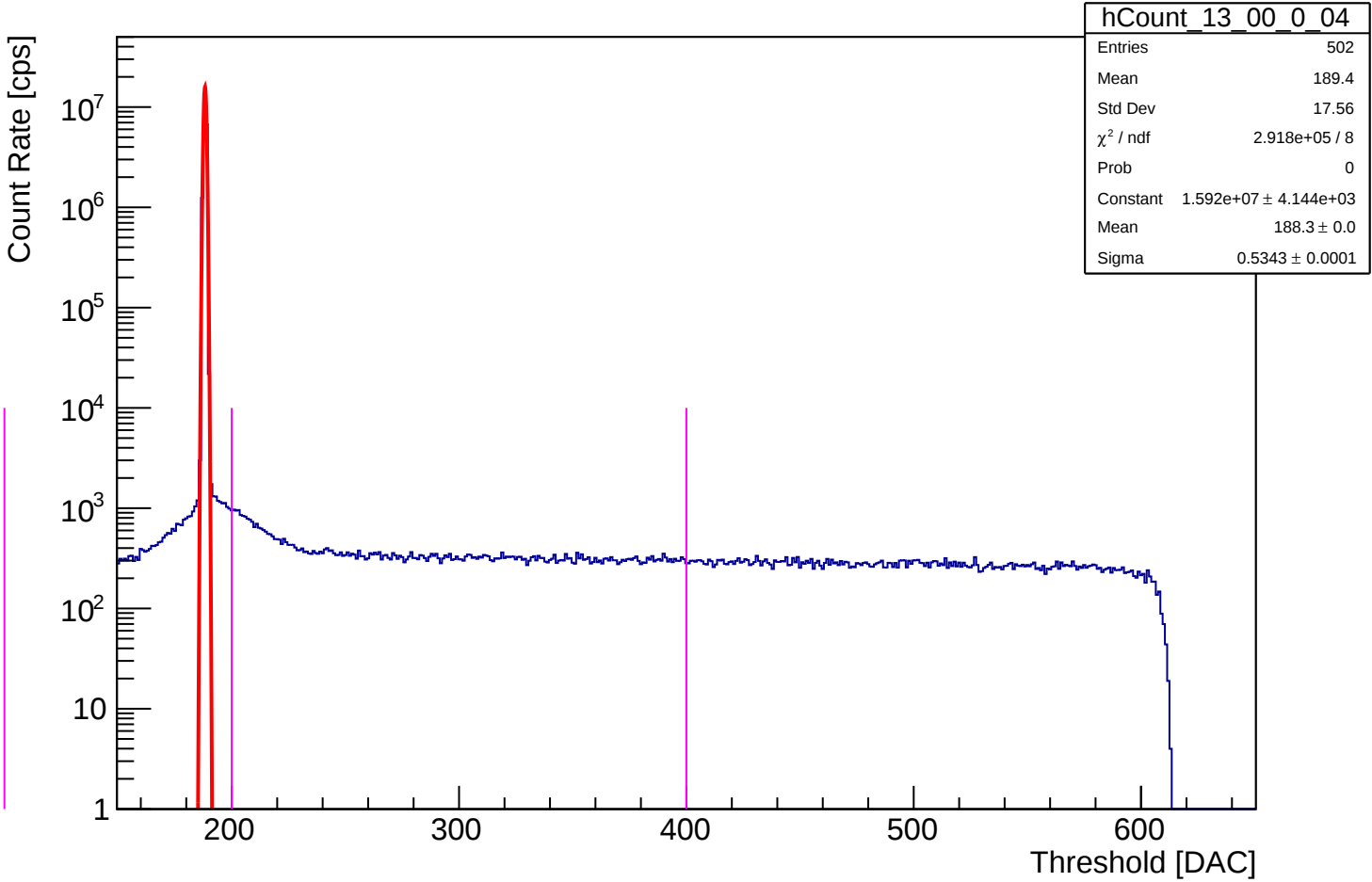
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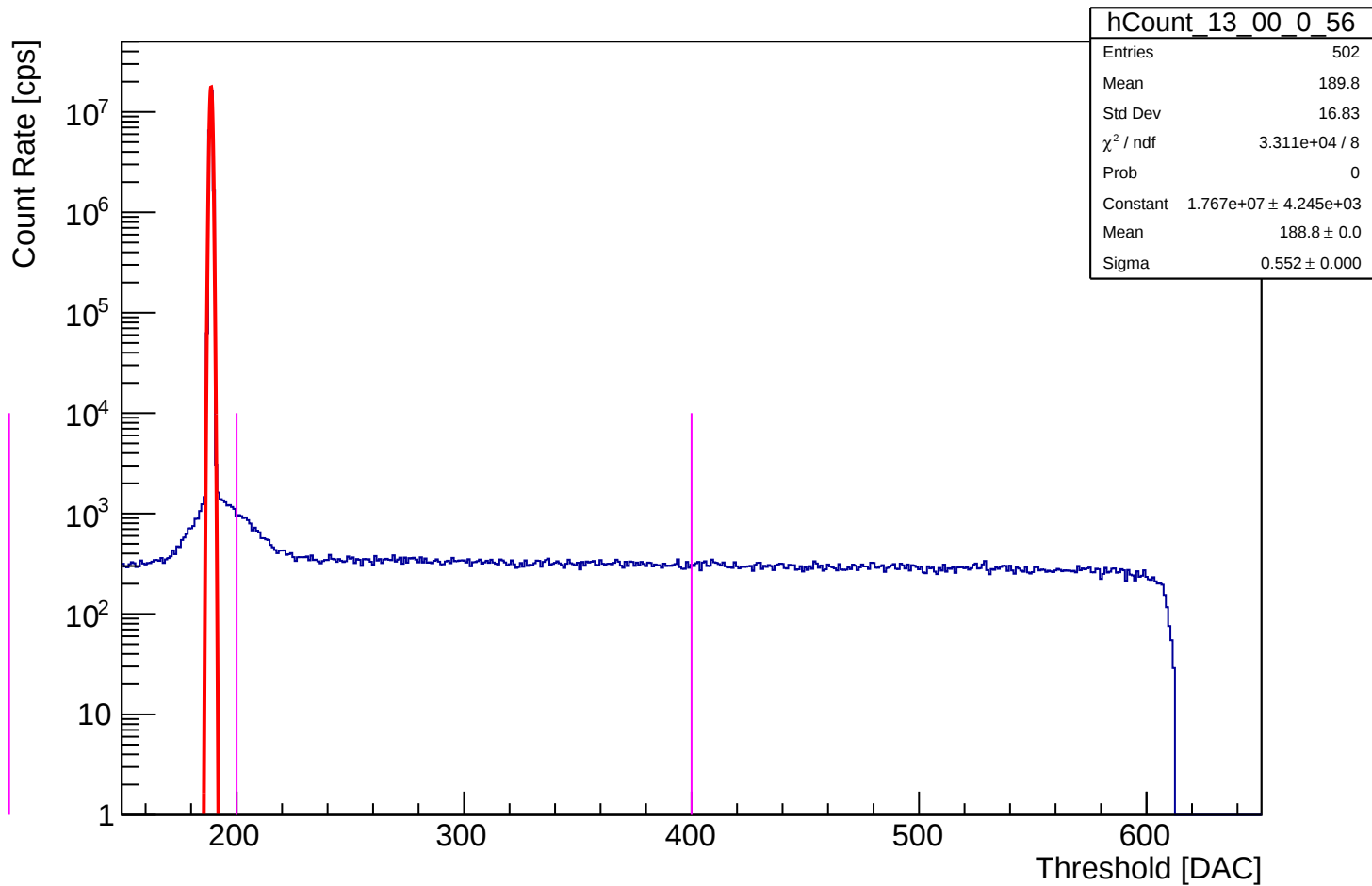




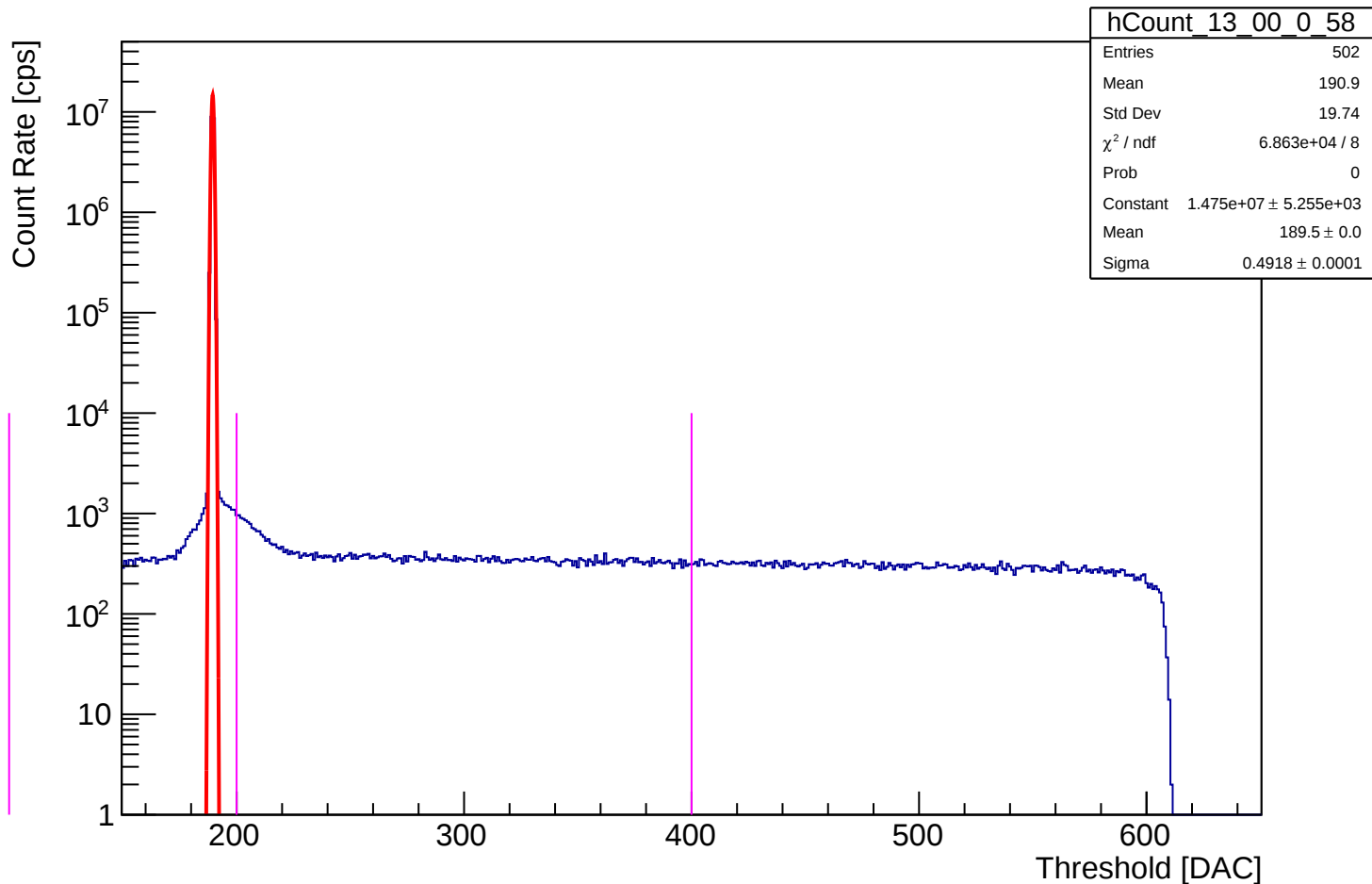




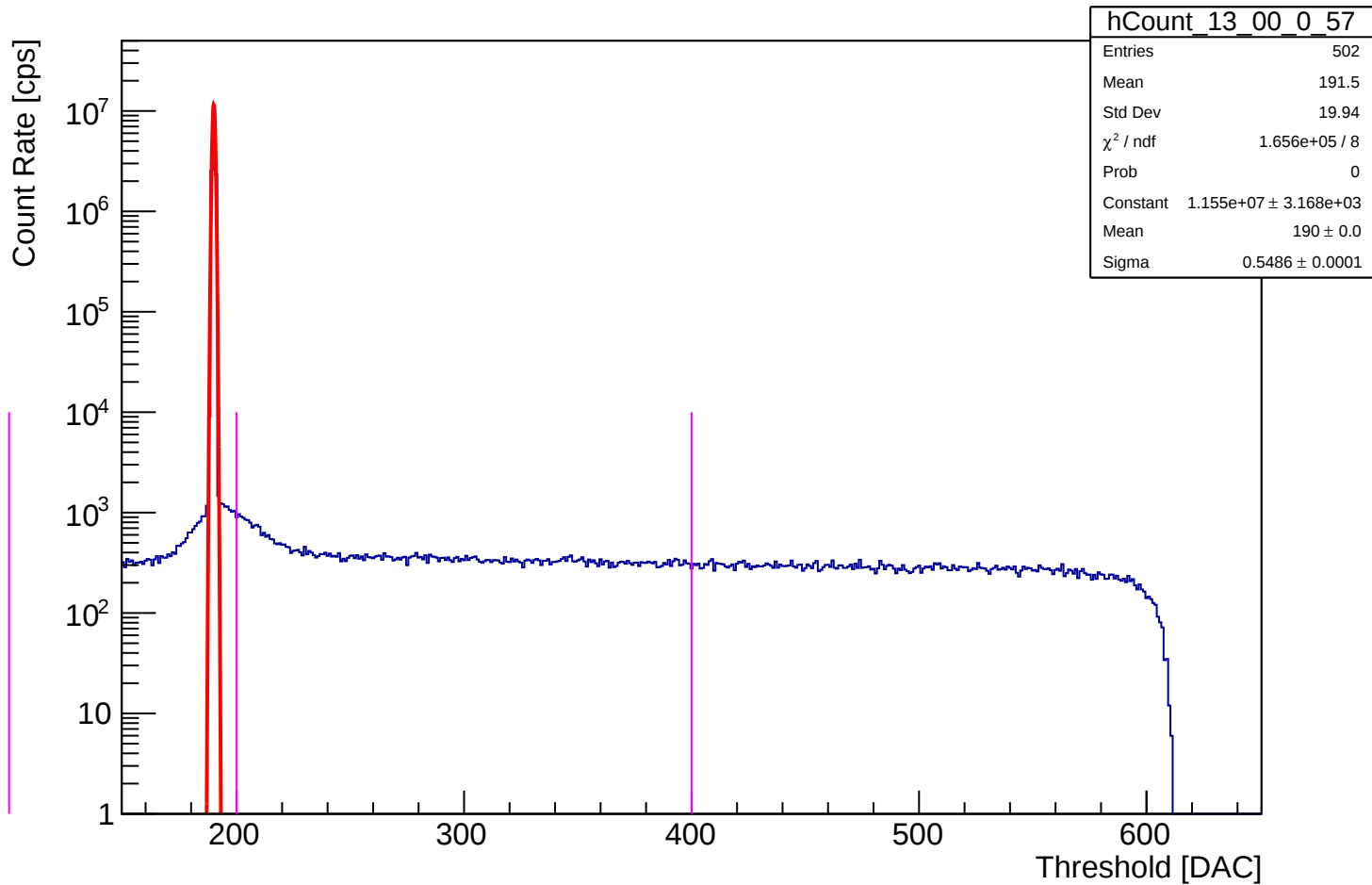
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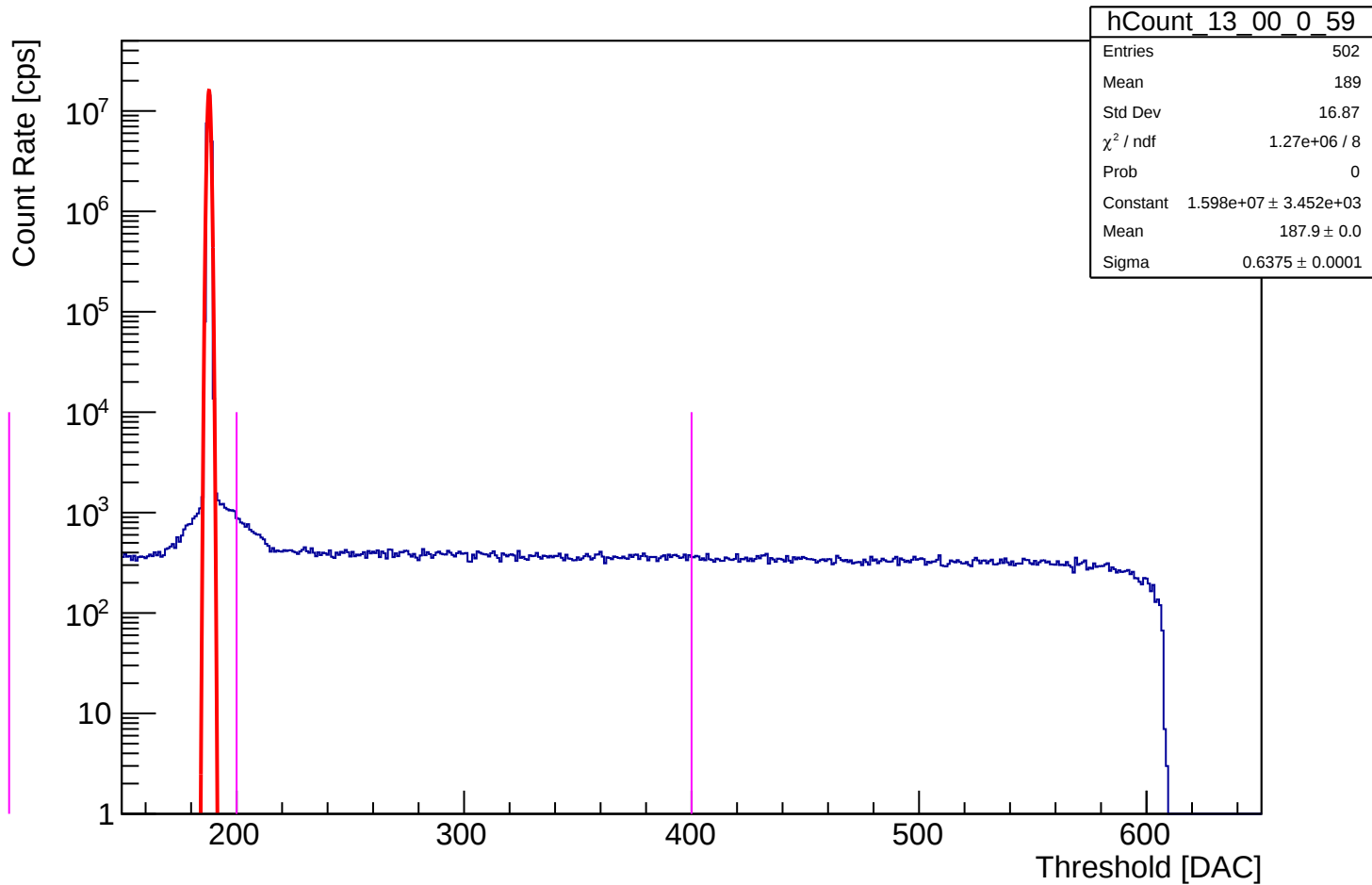
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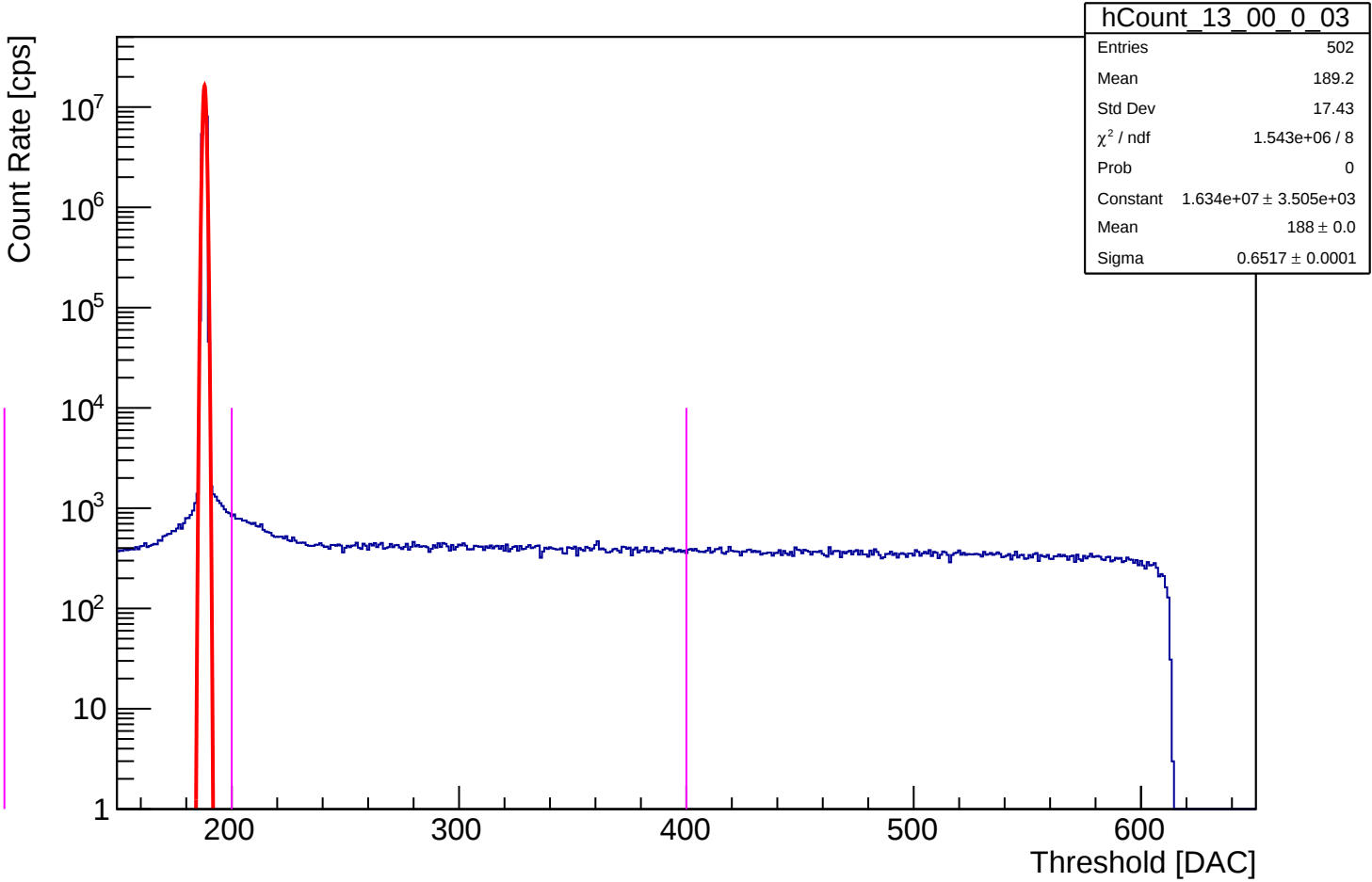


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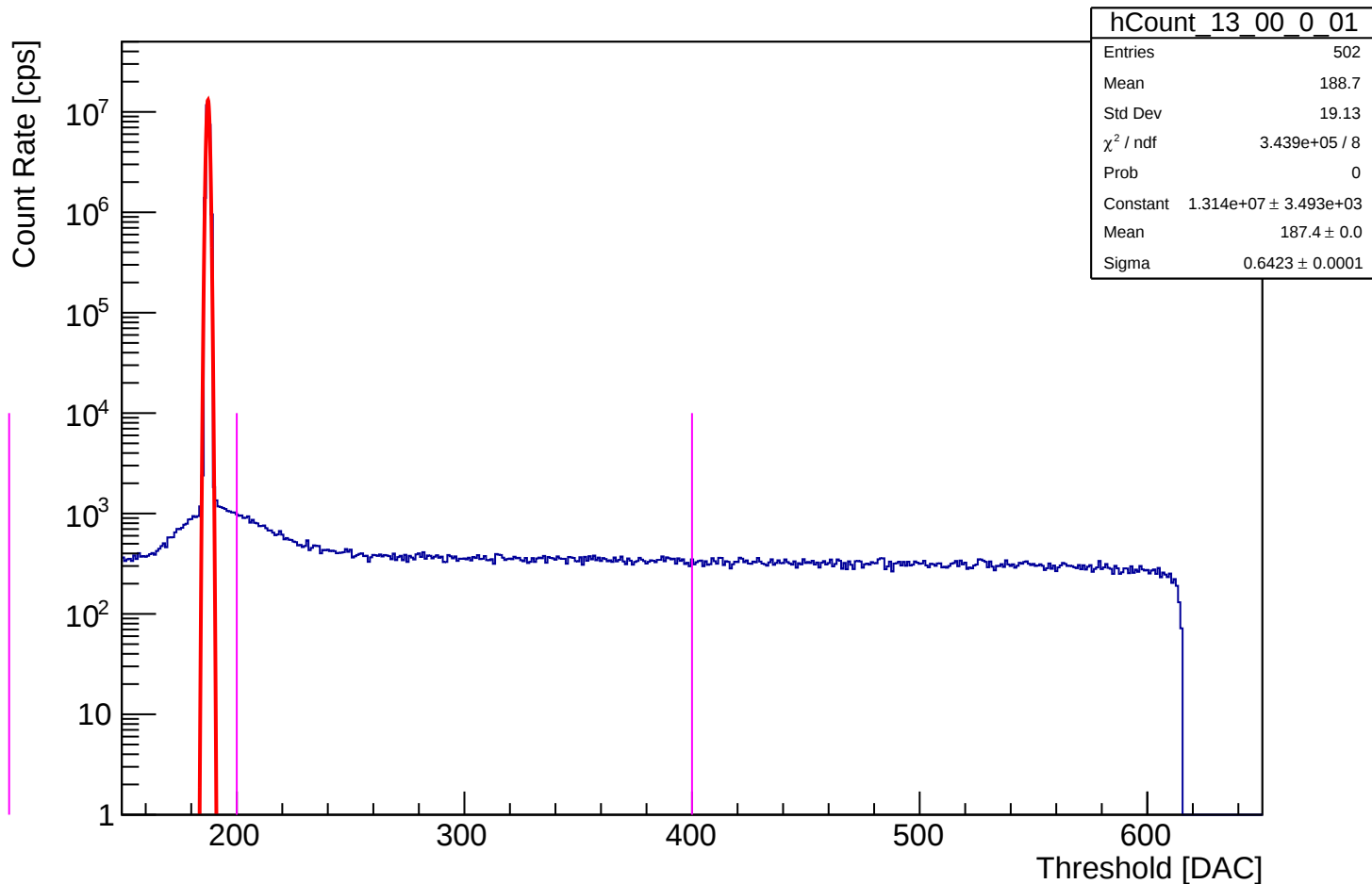


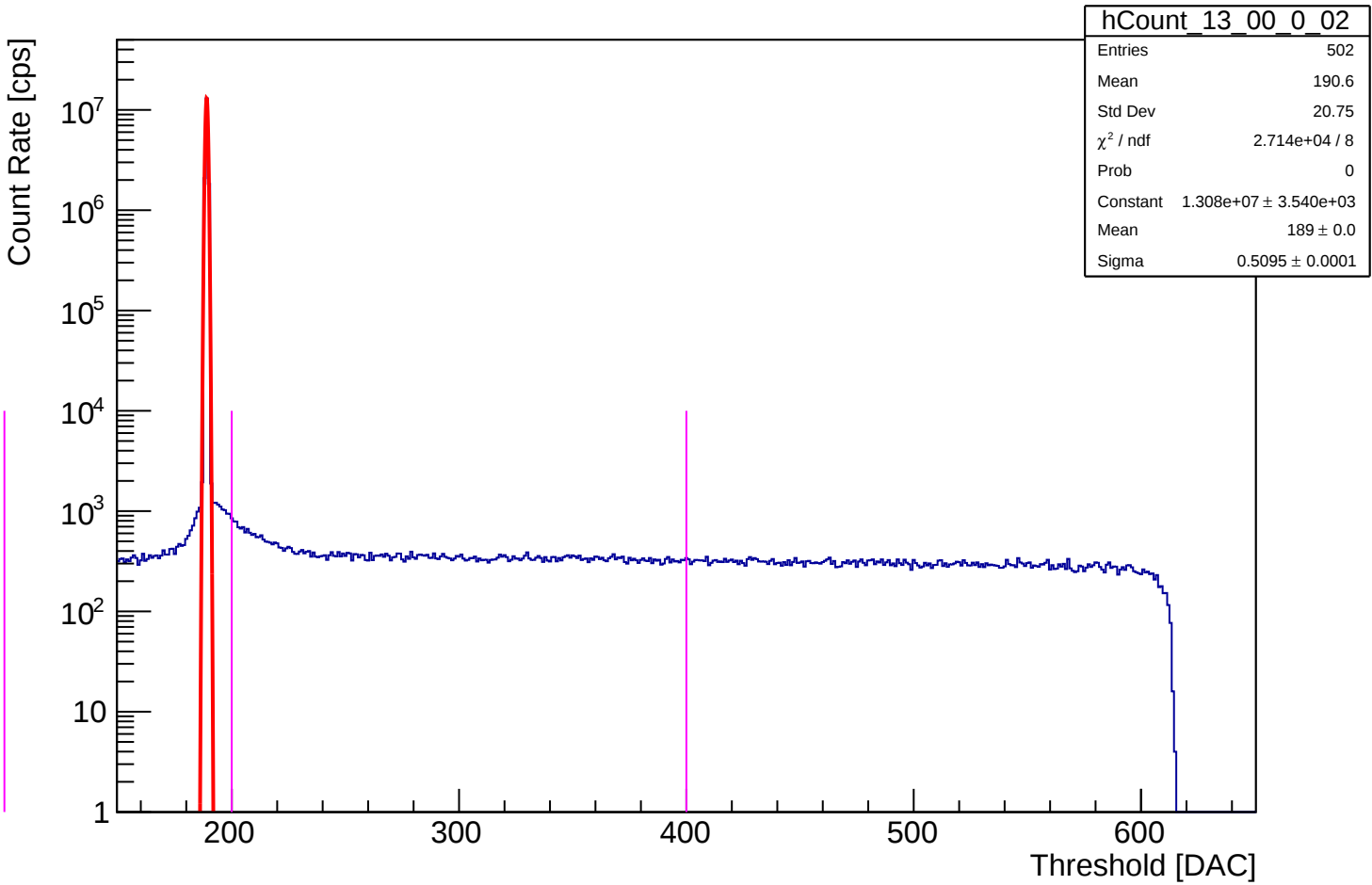
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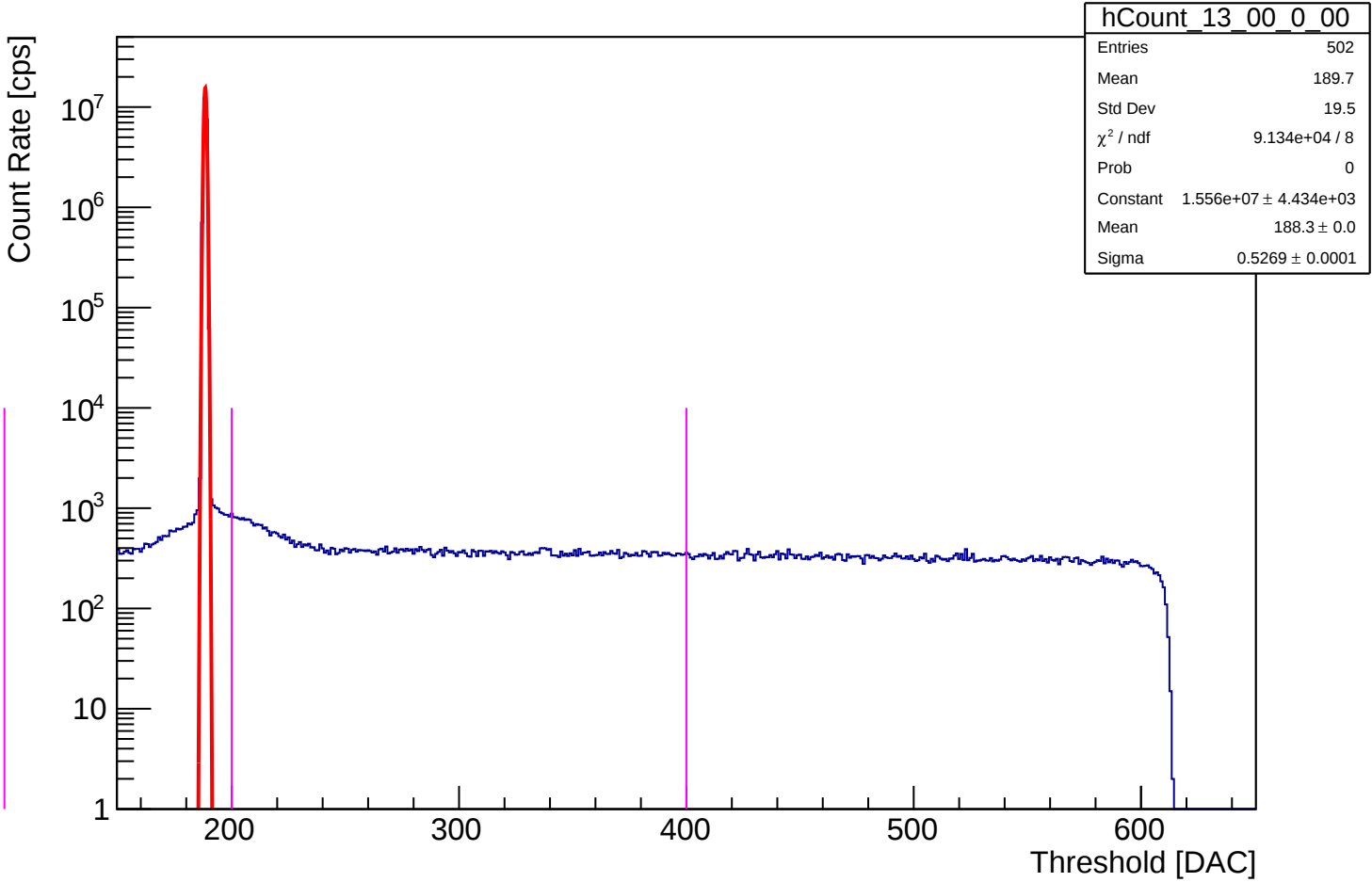




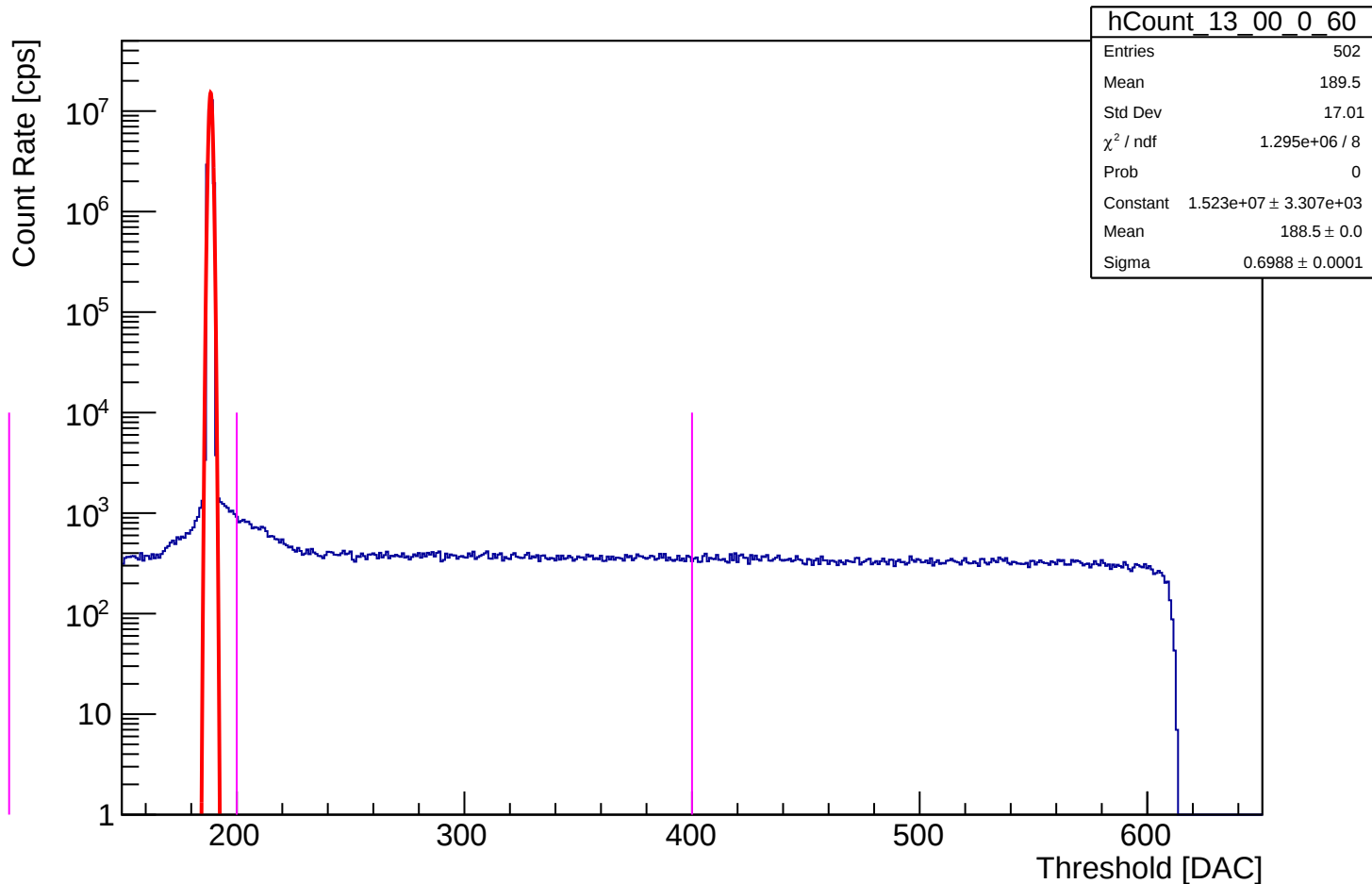
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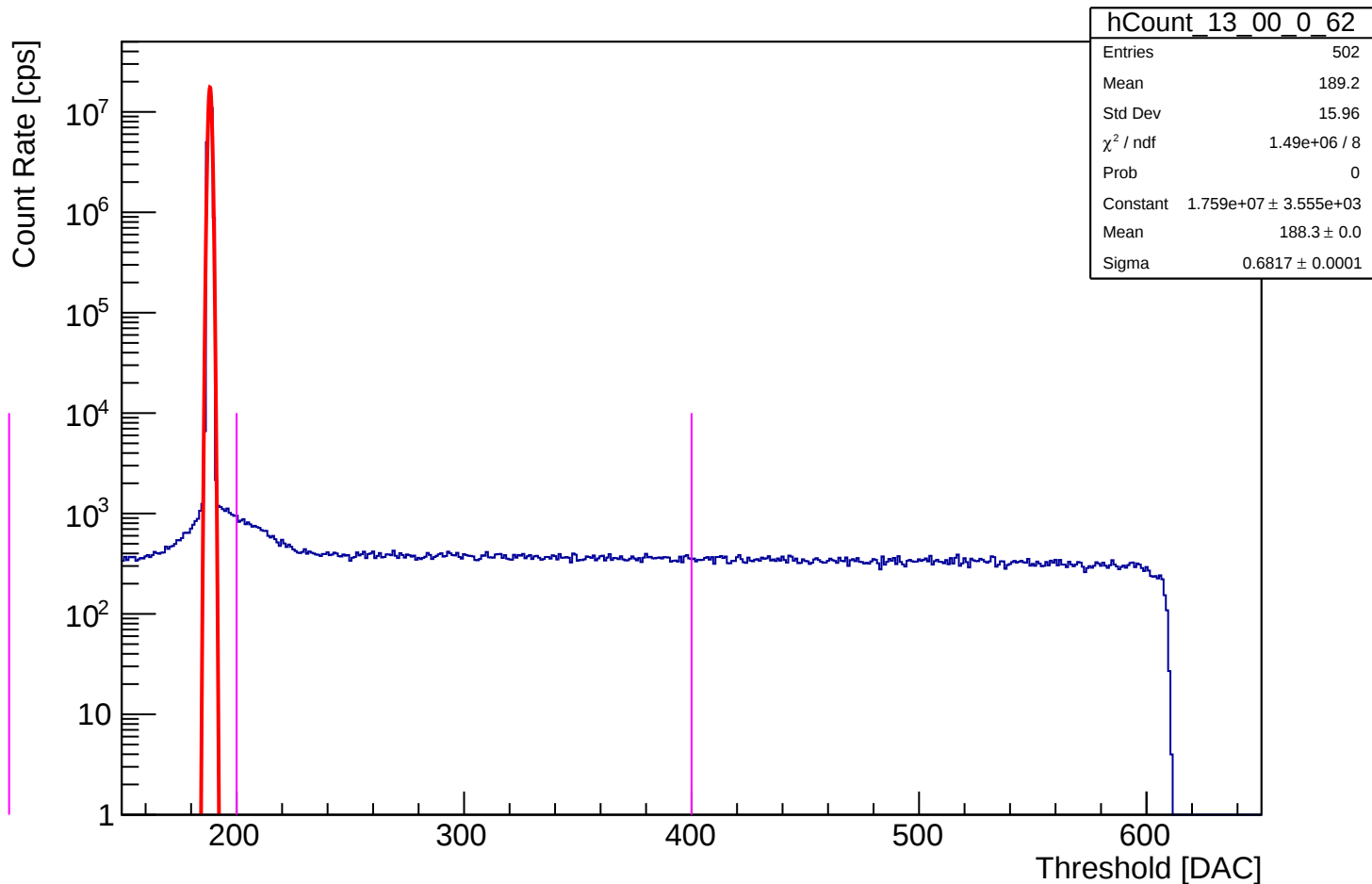




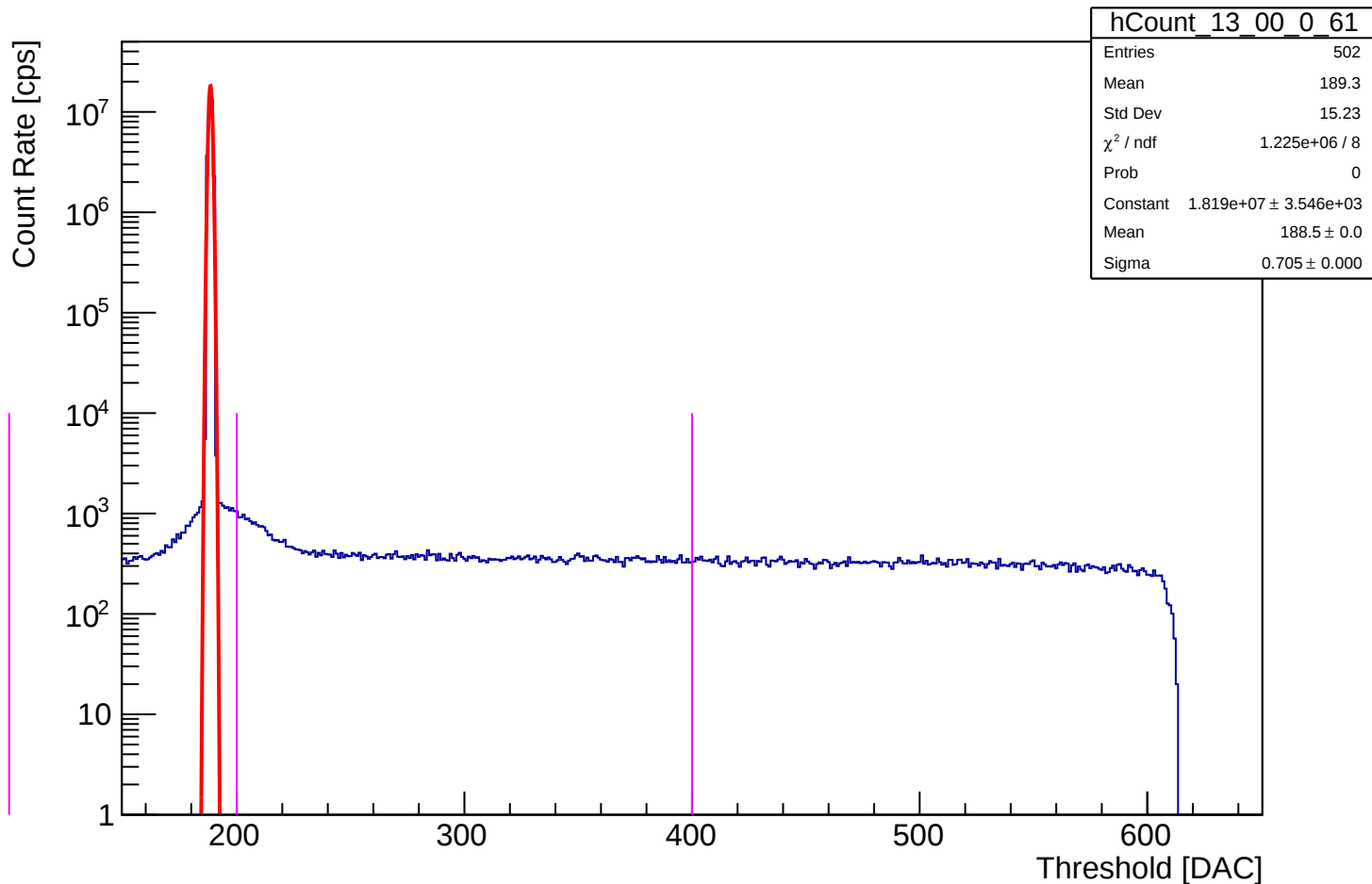
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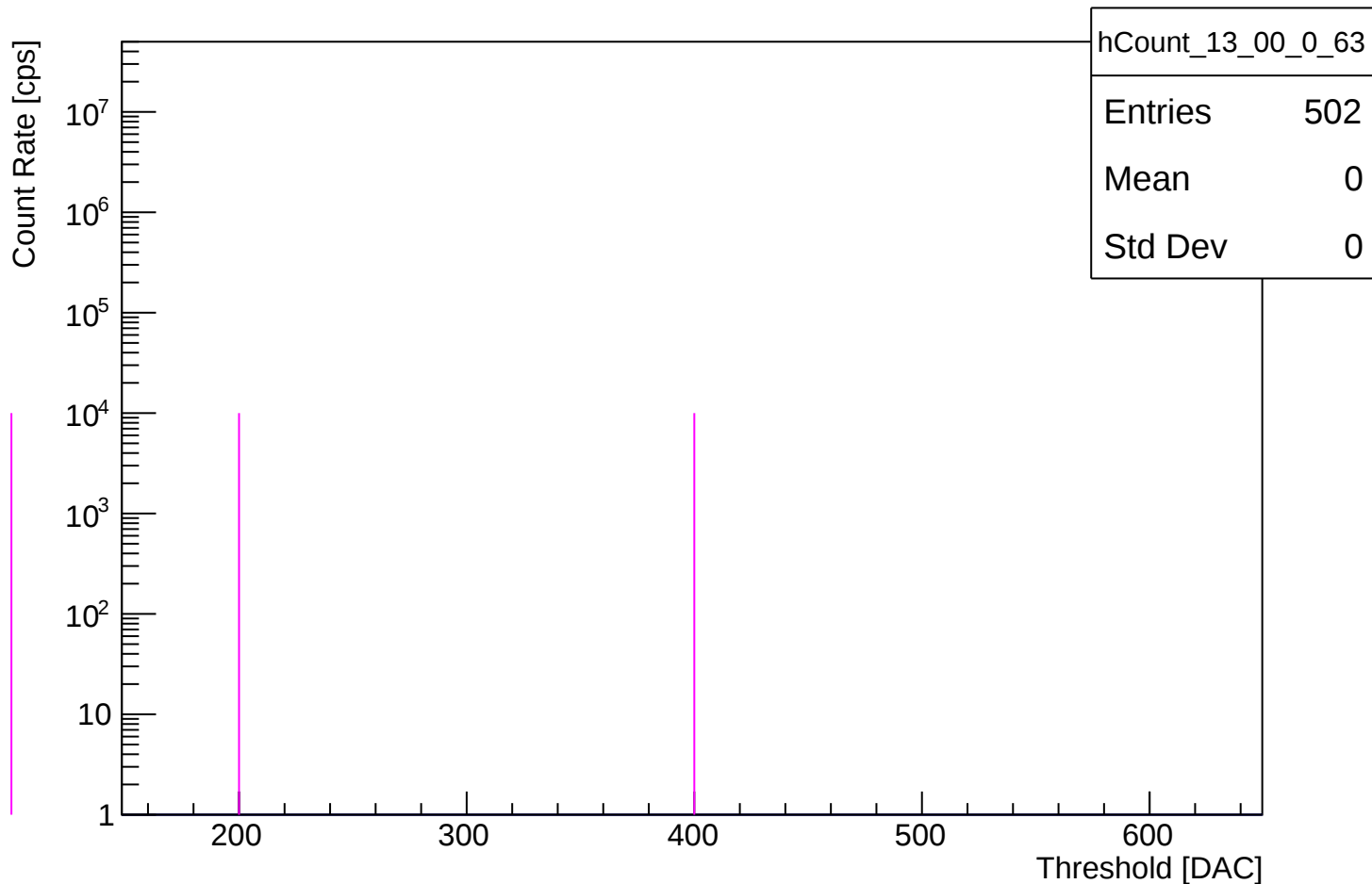
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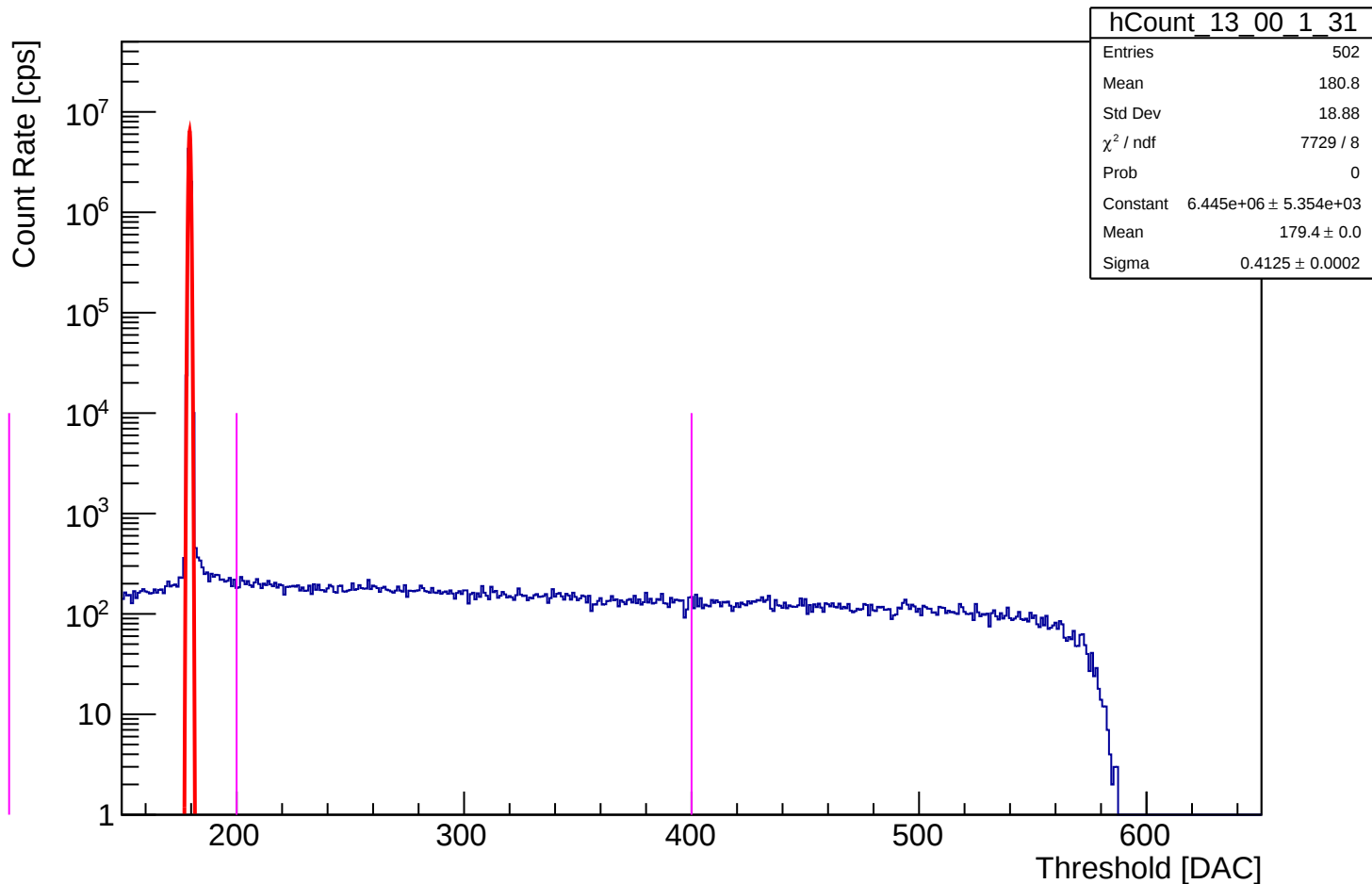
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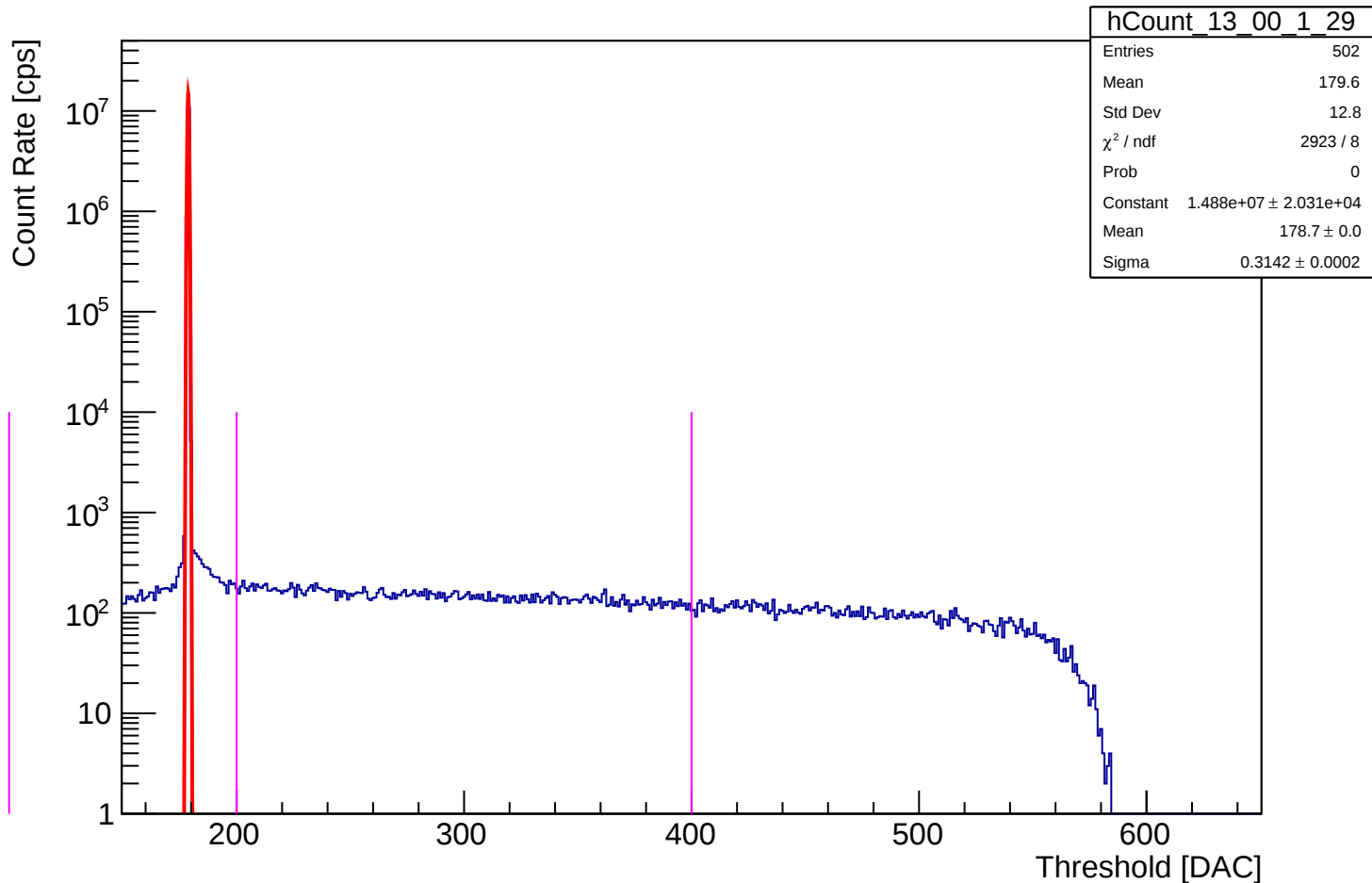
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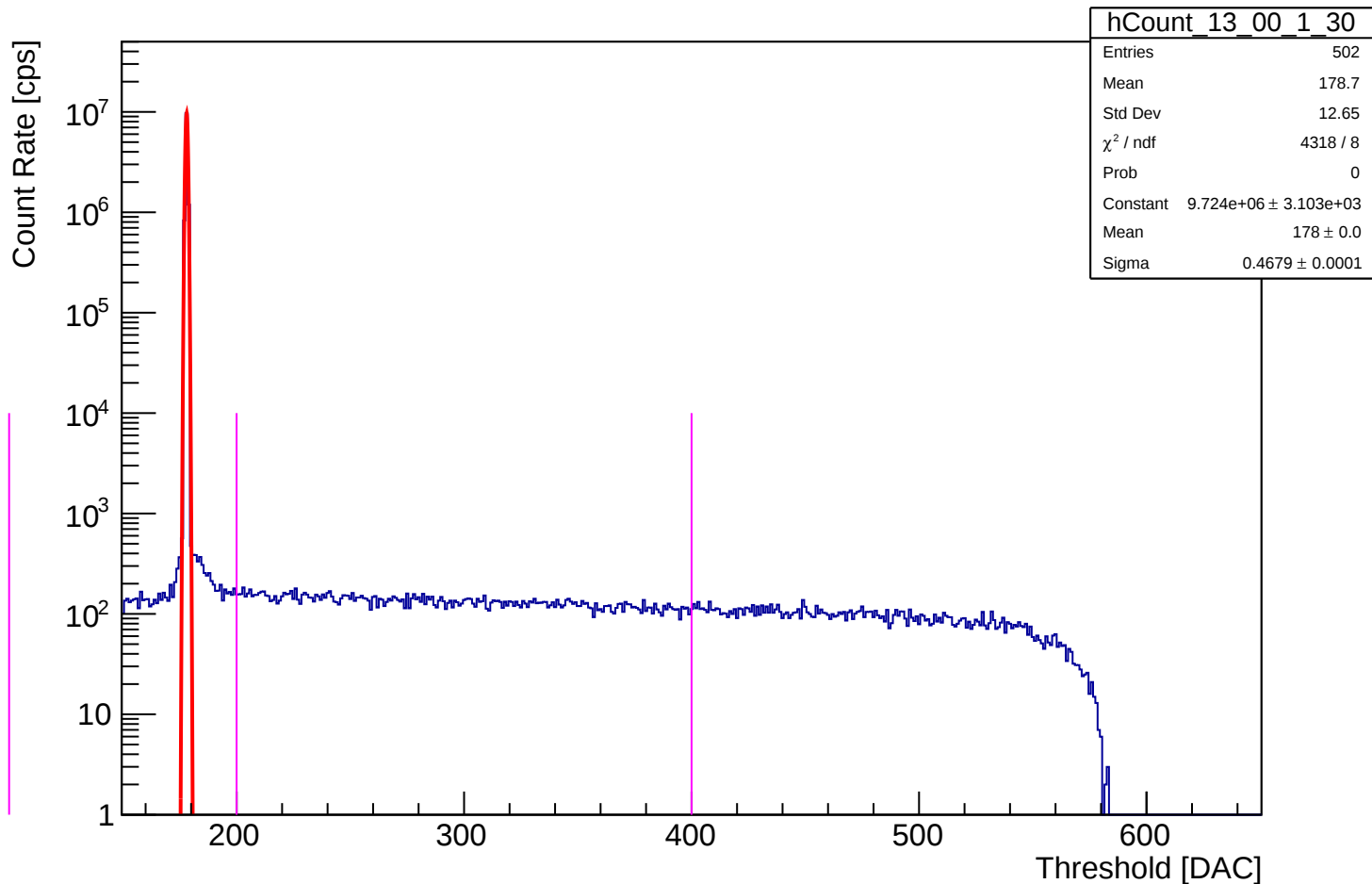
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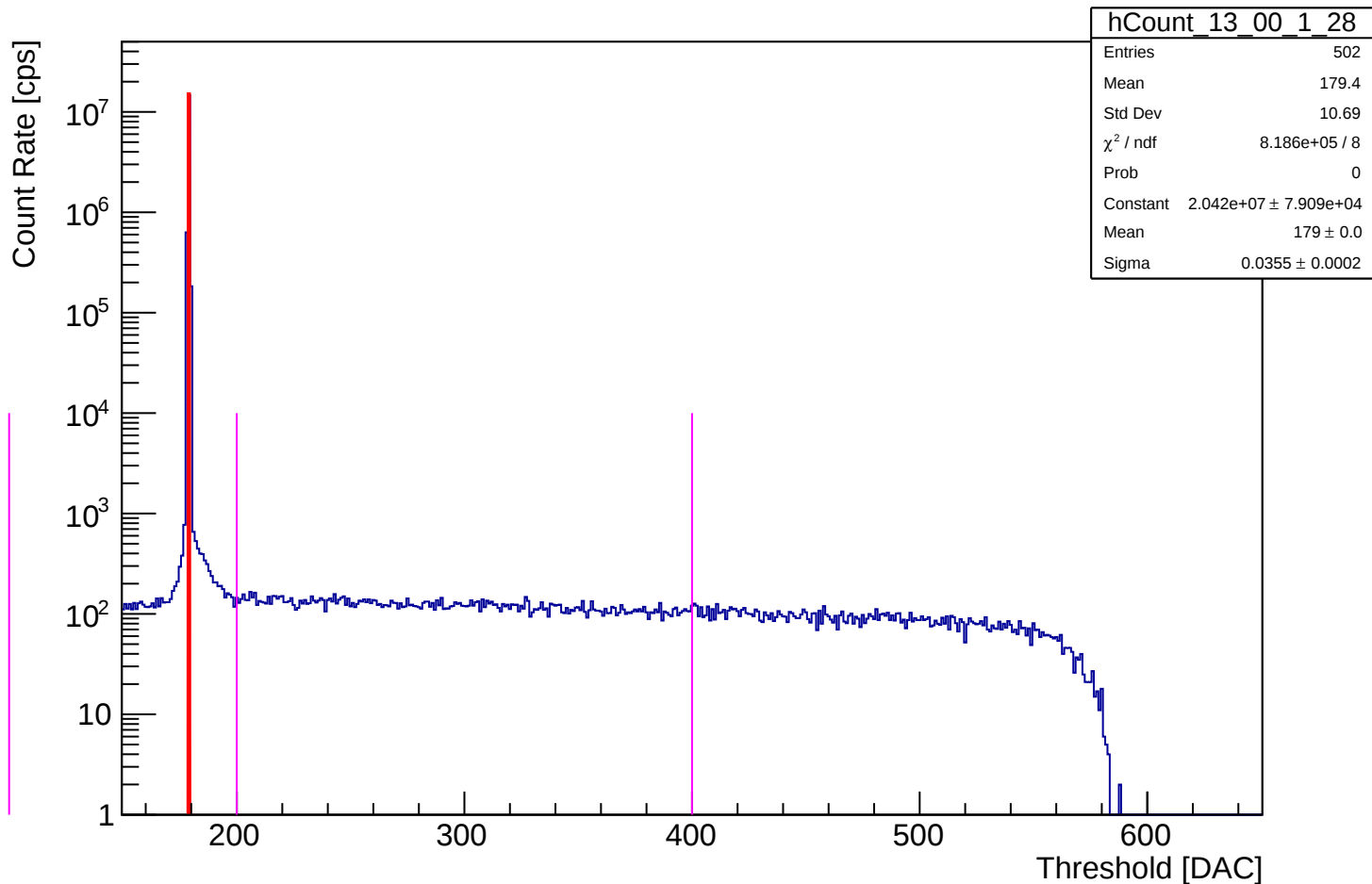
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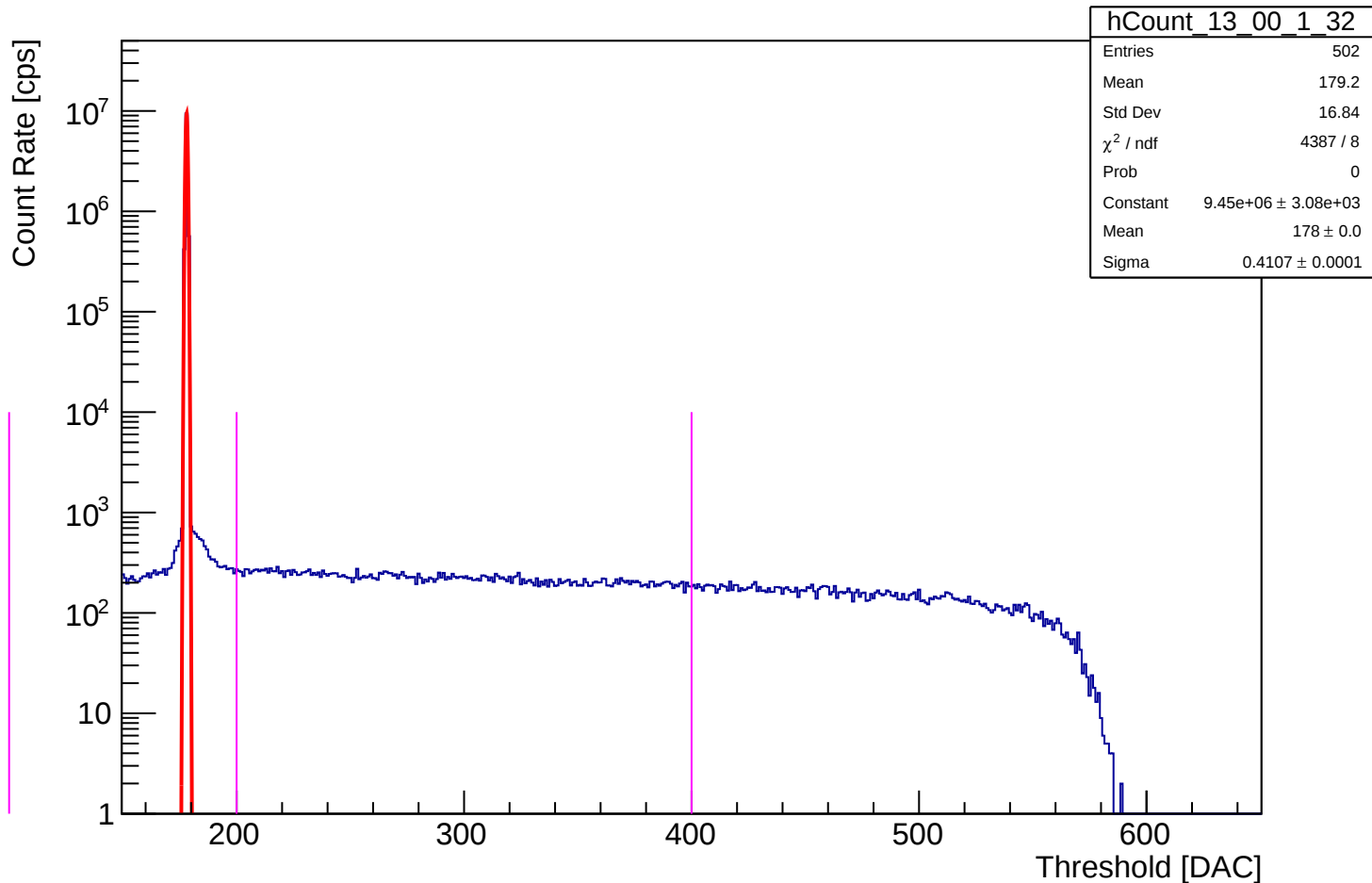
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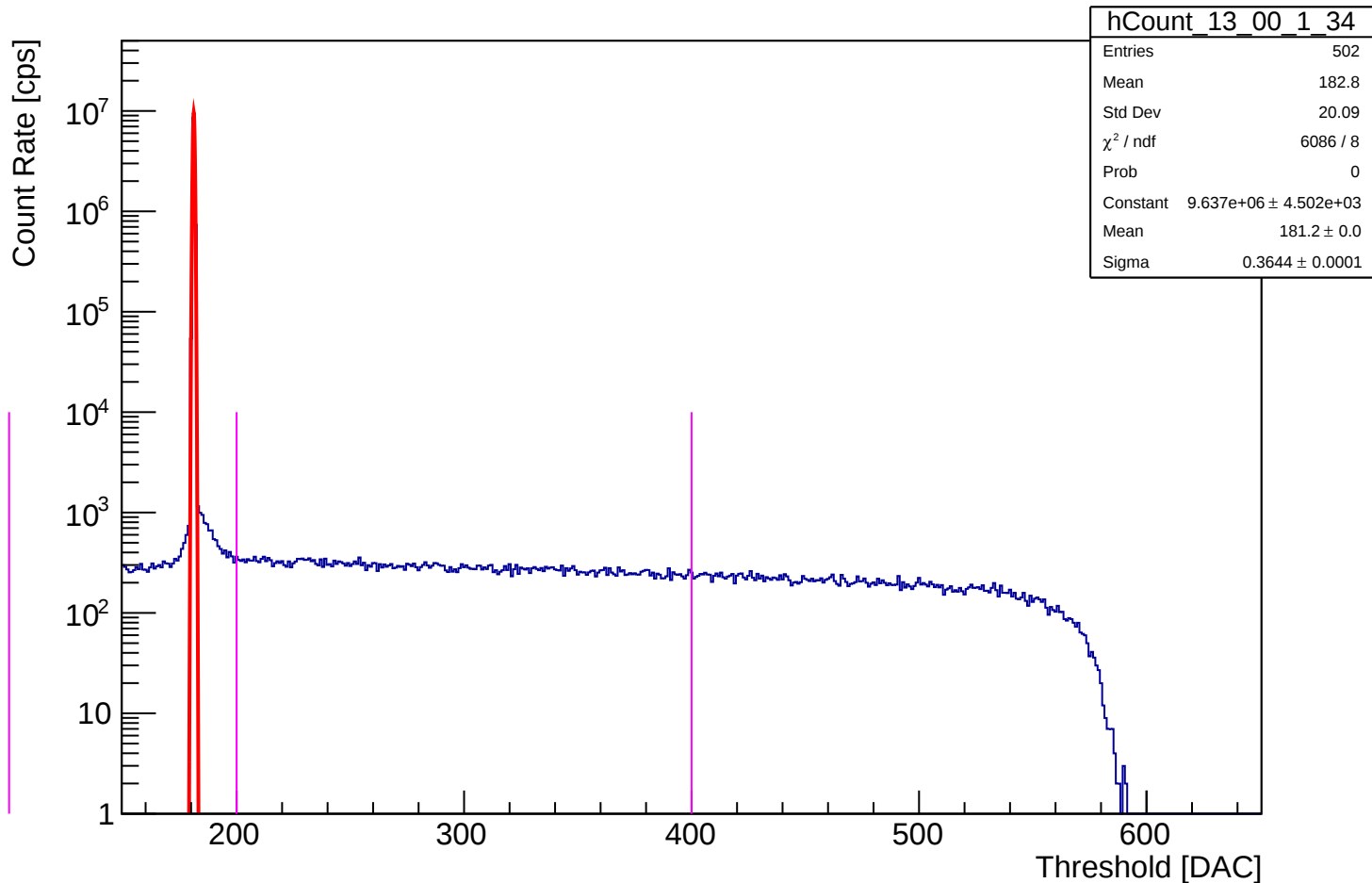
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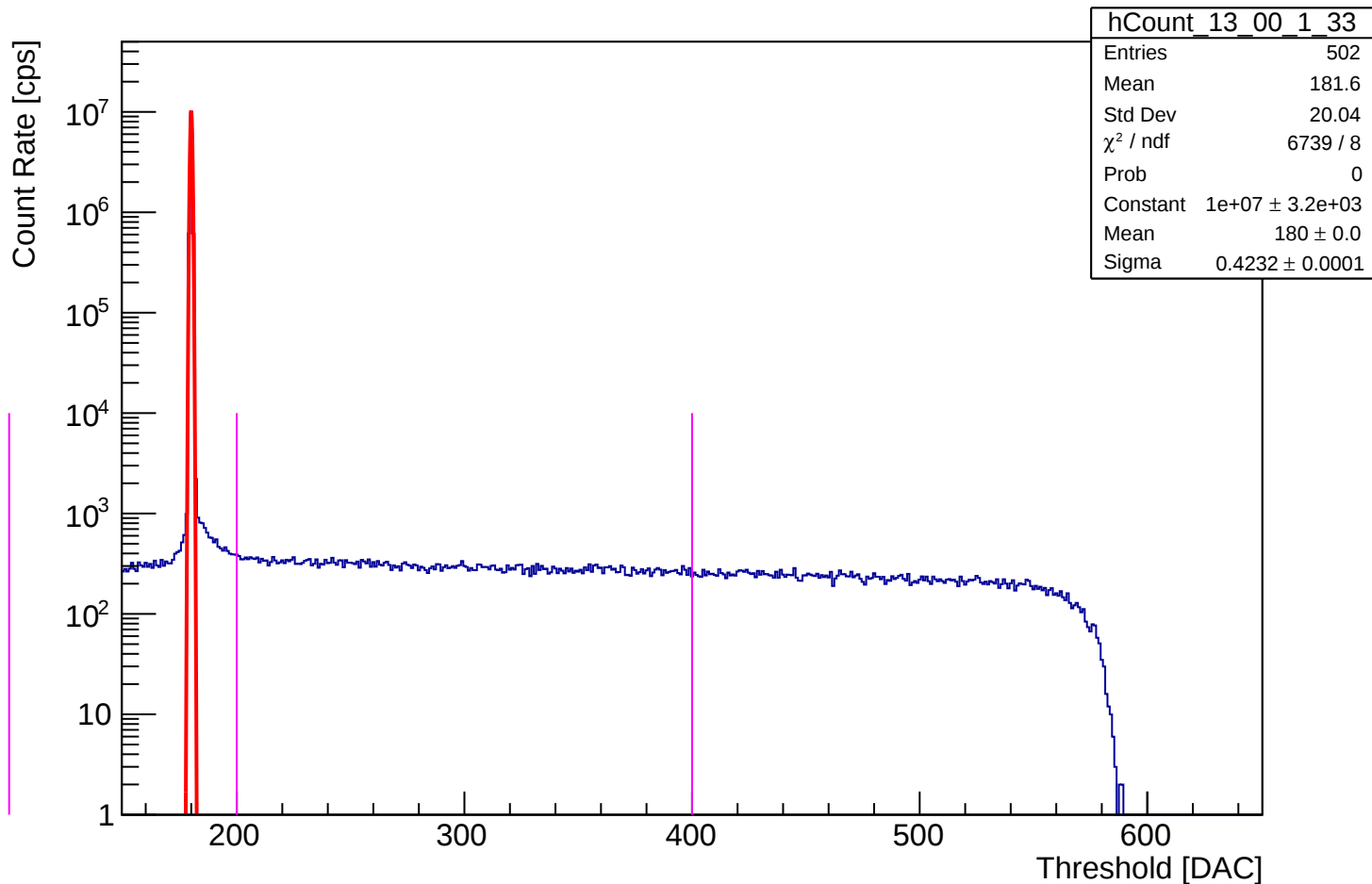
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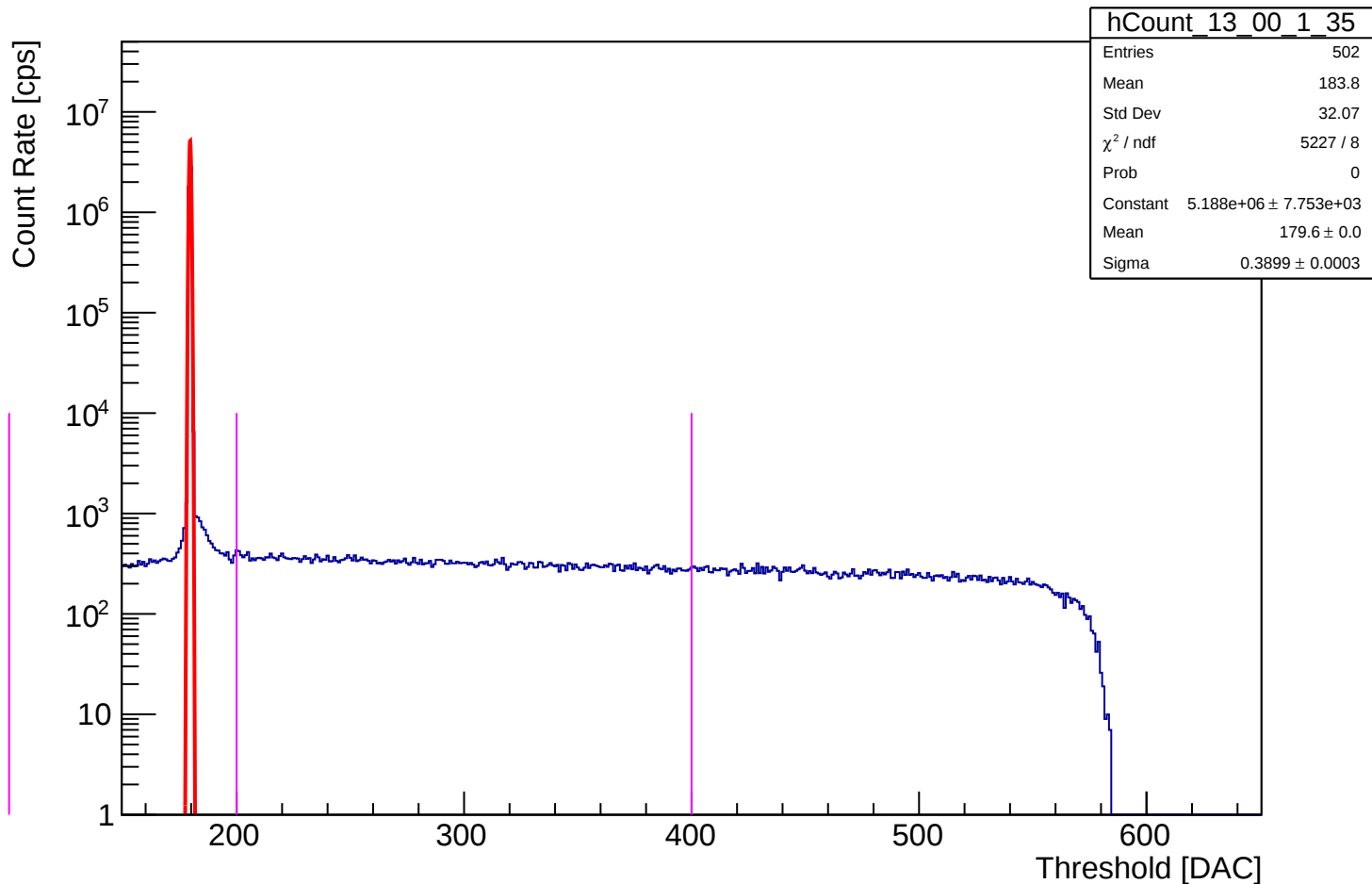
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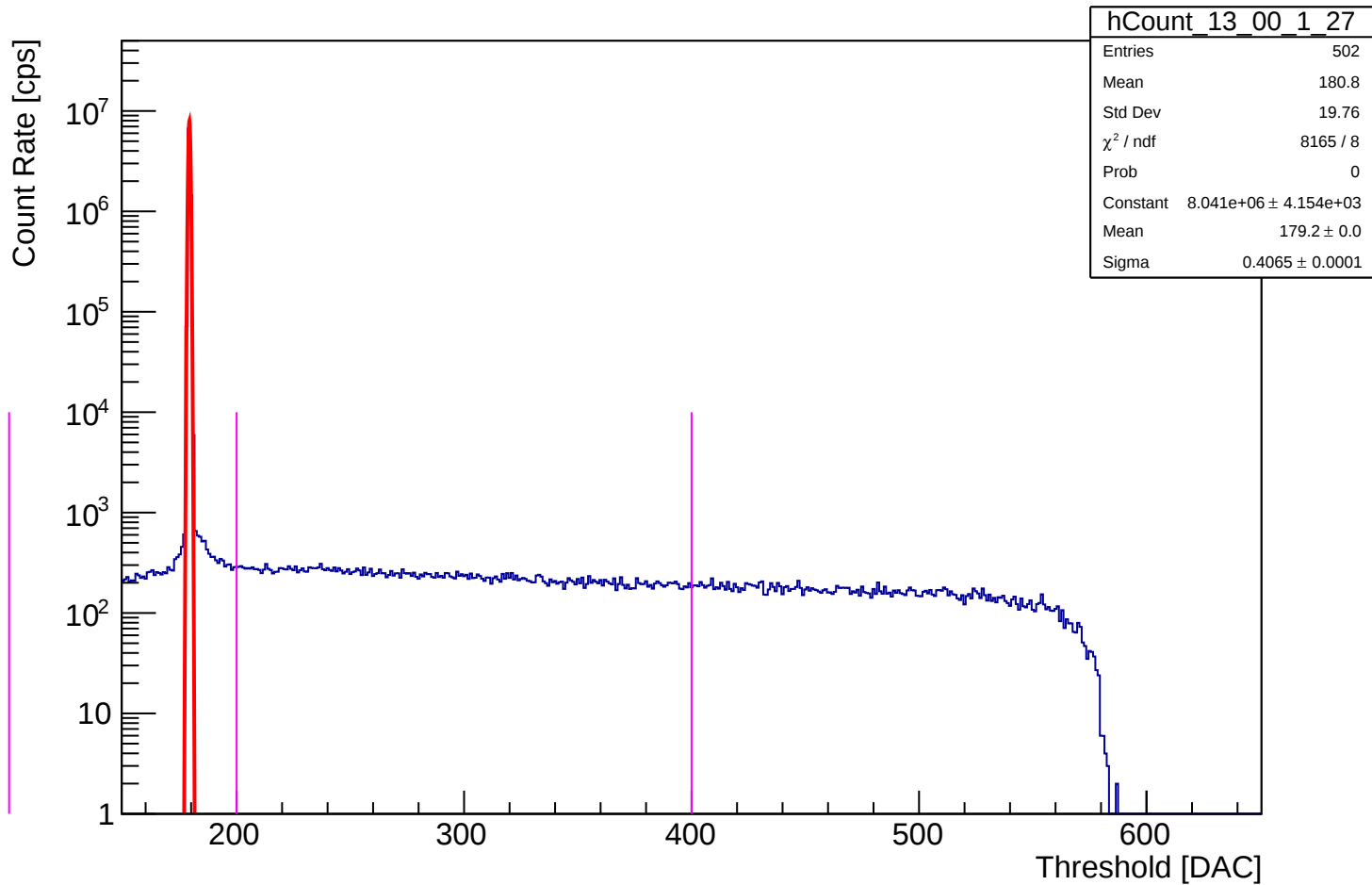
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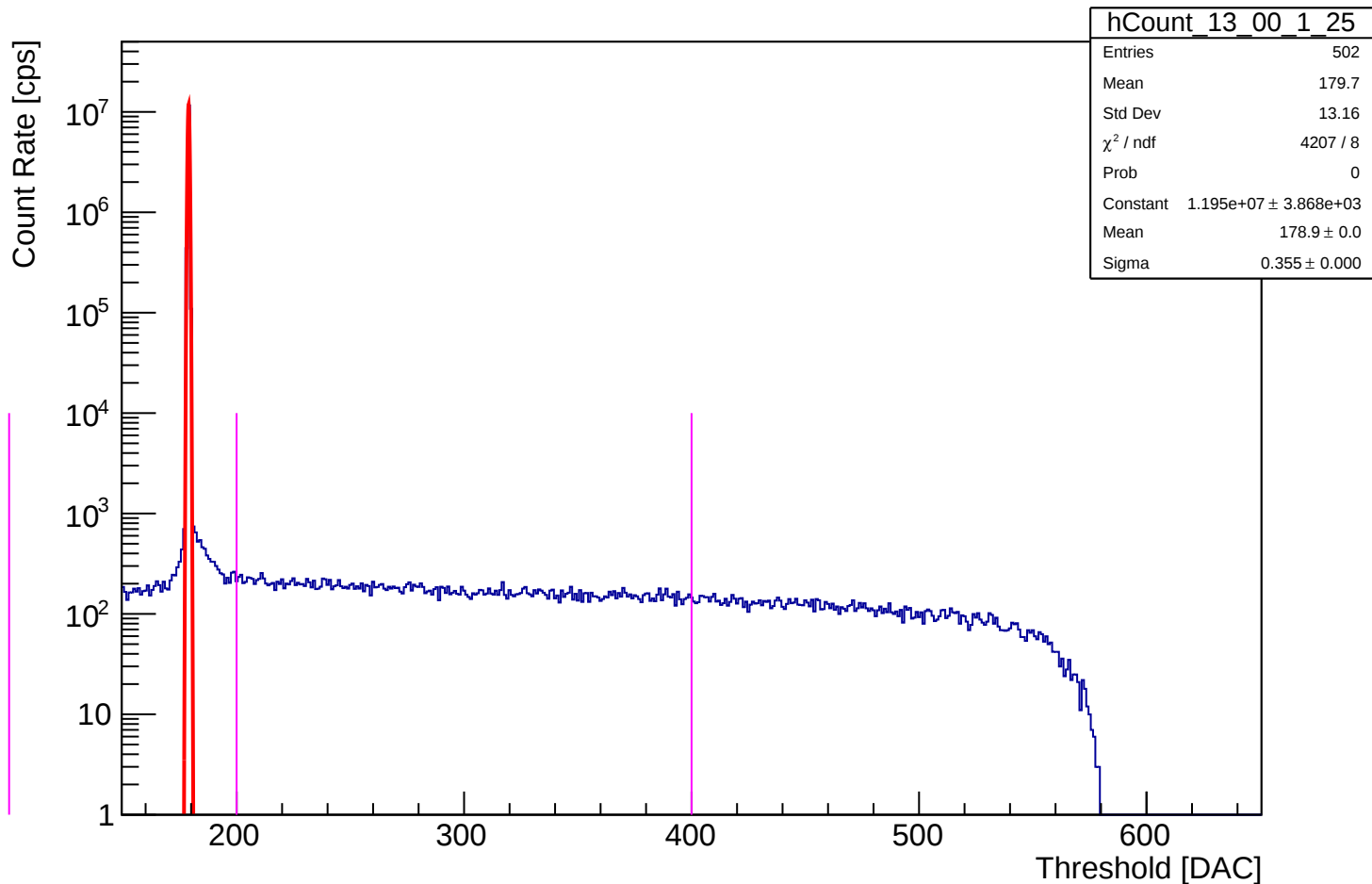
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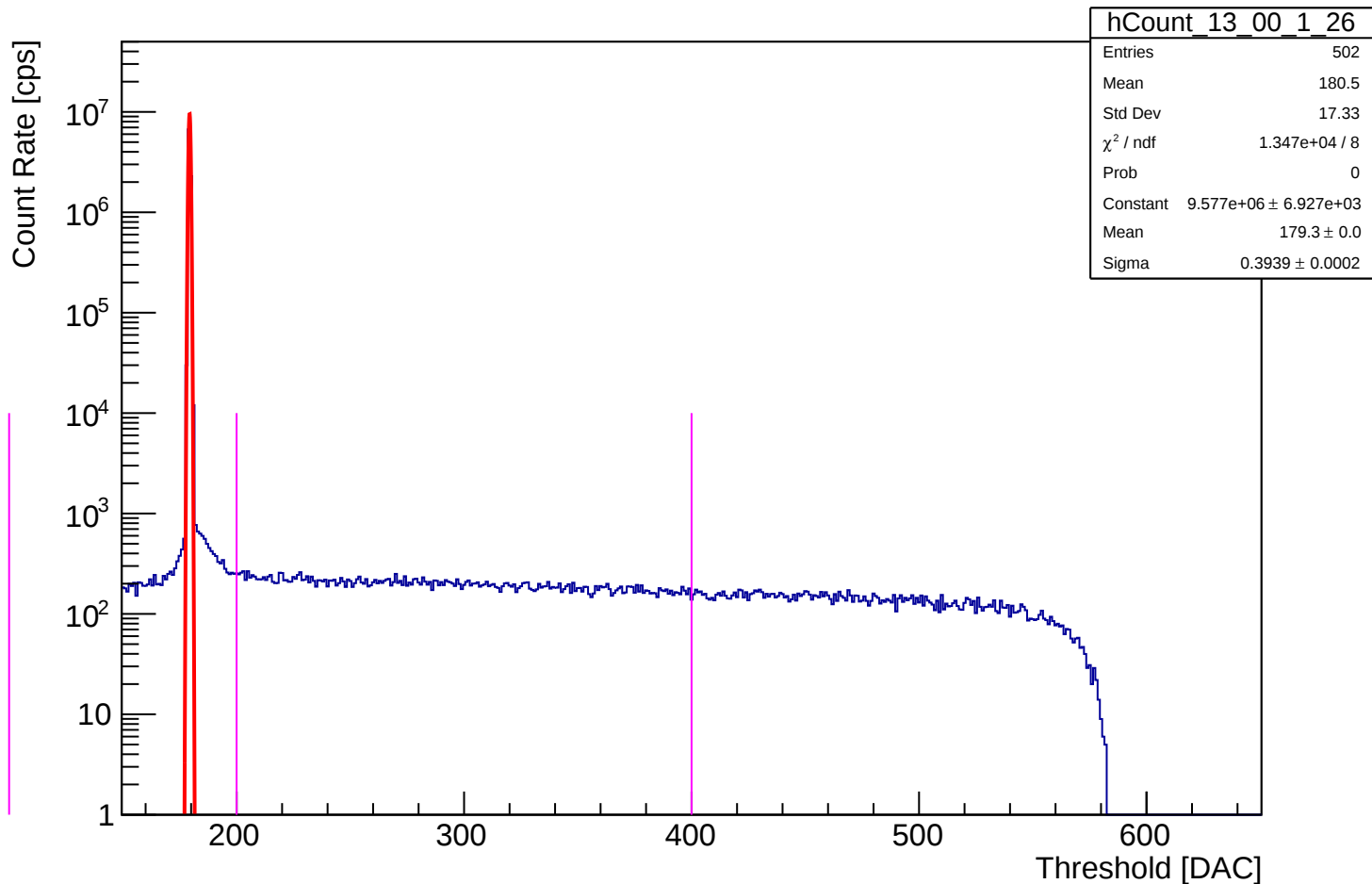
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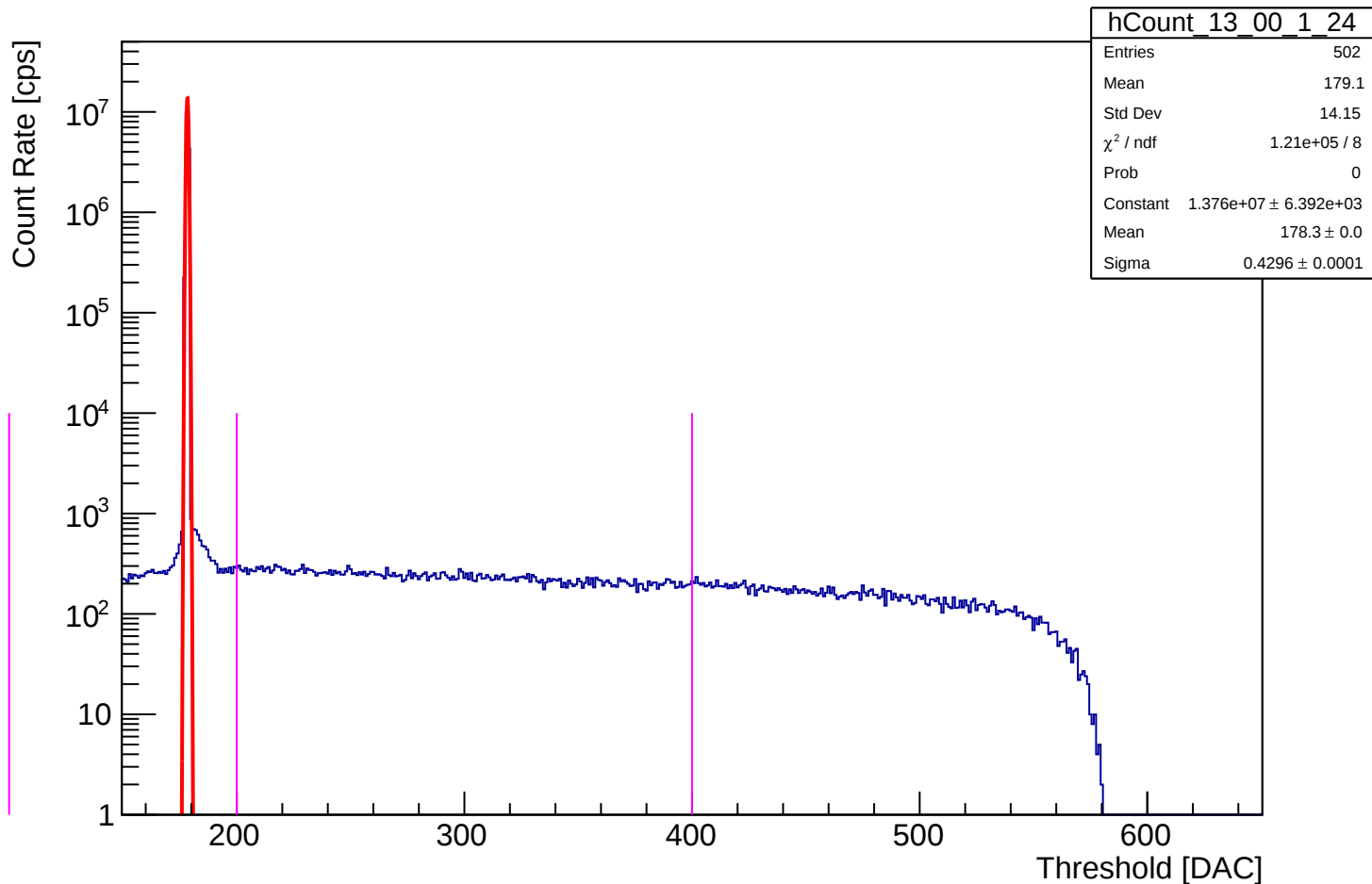
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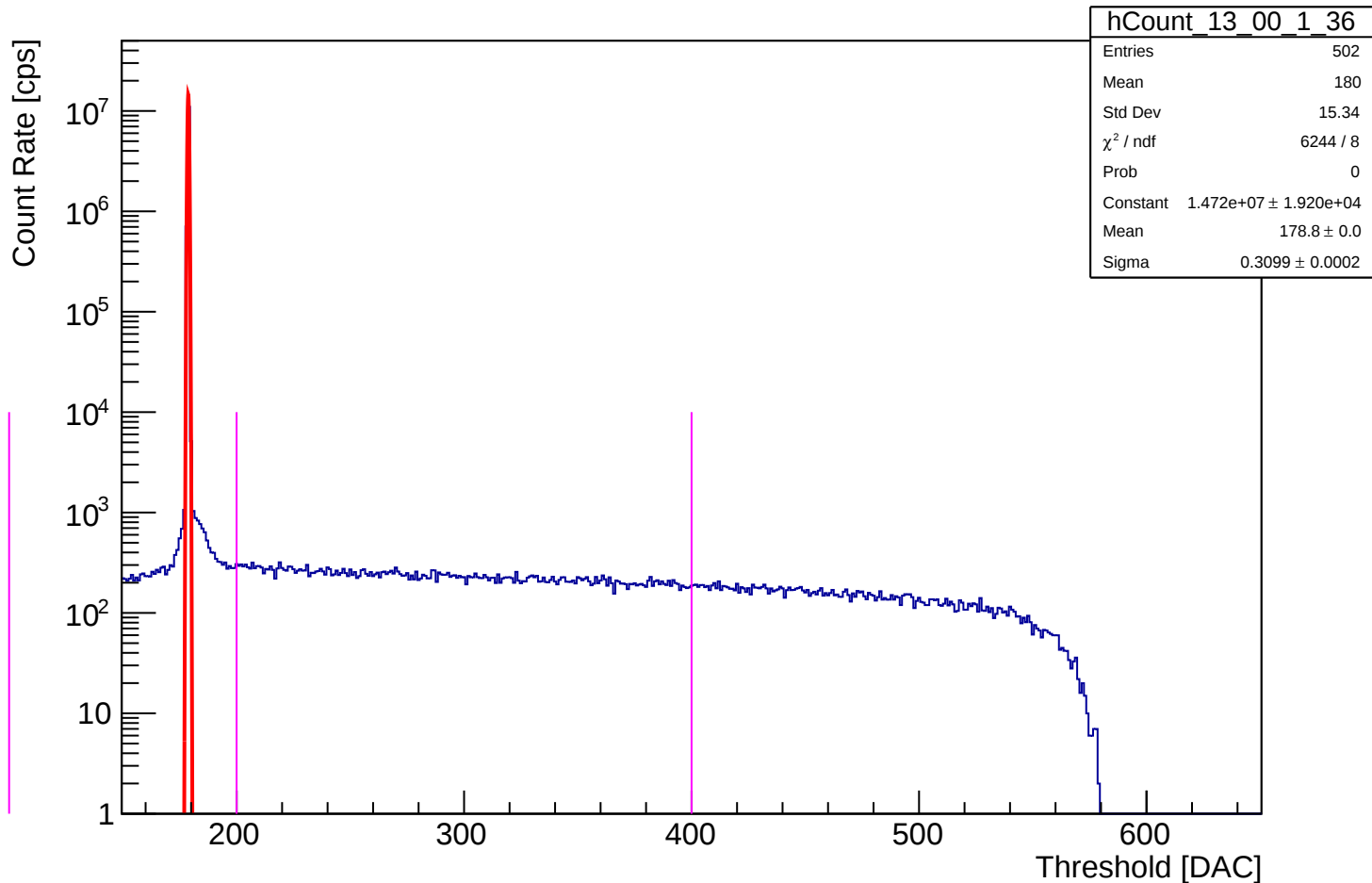
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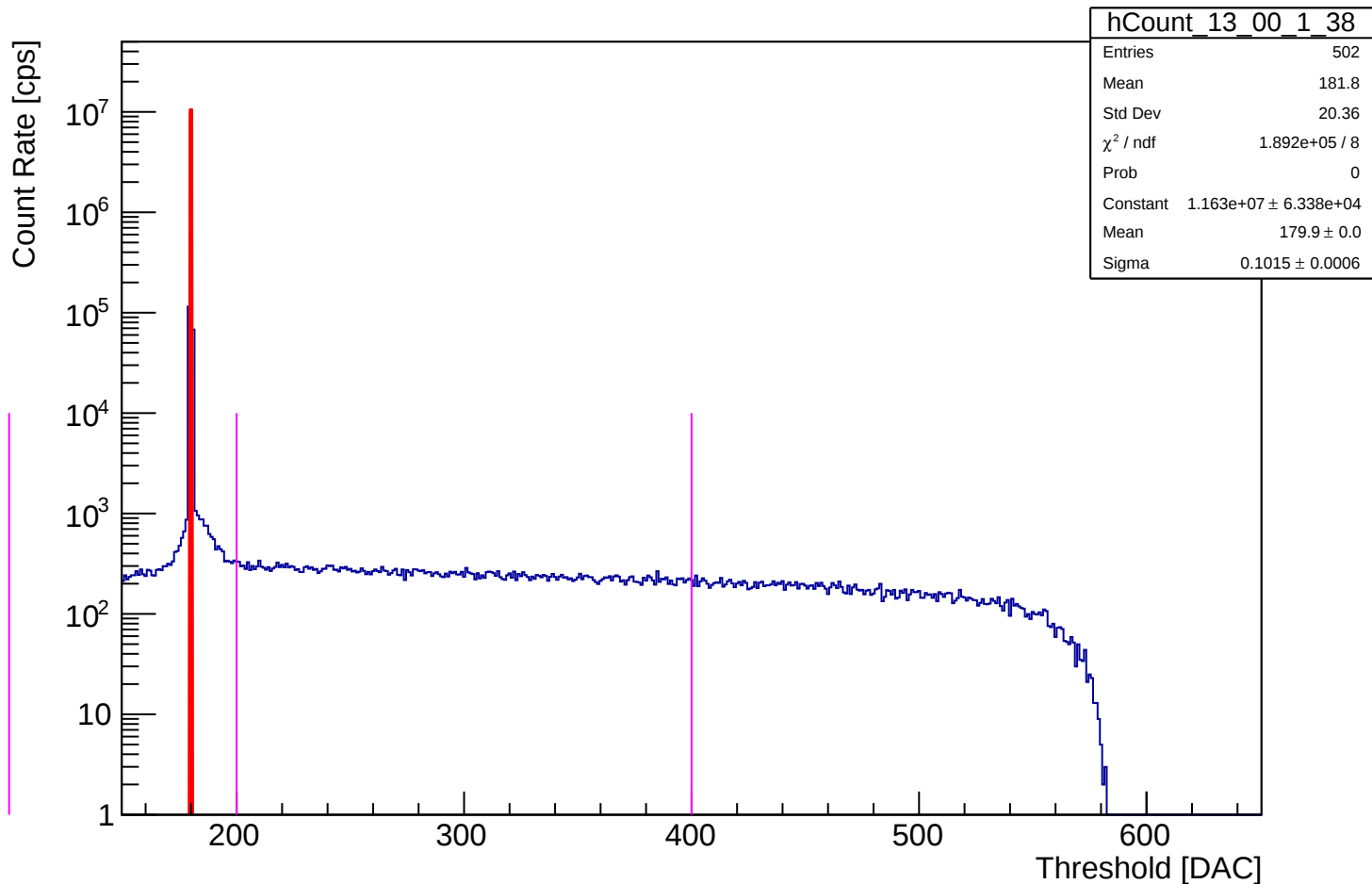
Row 1 Tile 1 Pmt 2 Pixel 12 Slot 13 Fiber 0 Asic 1 Channel 24



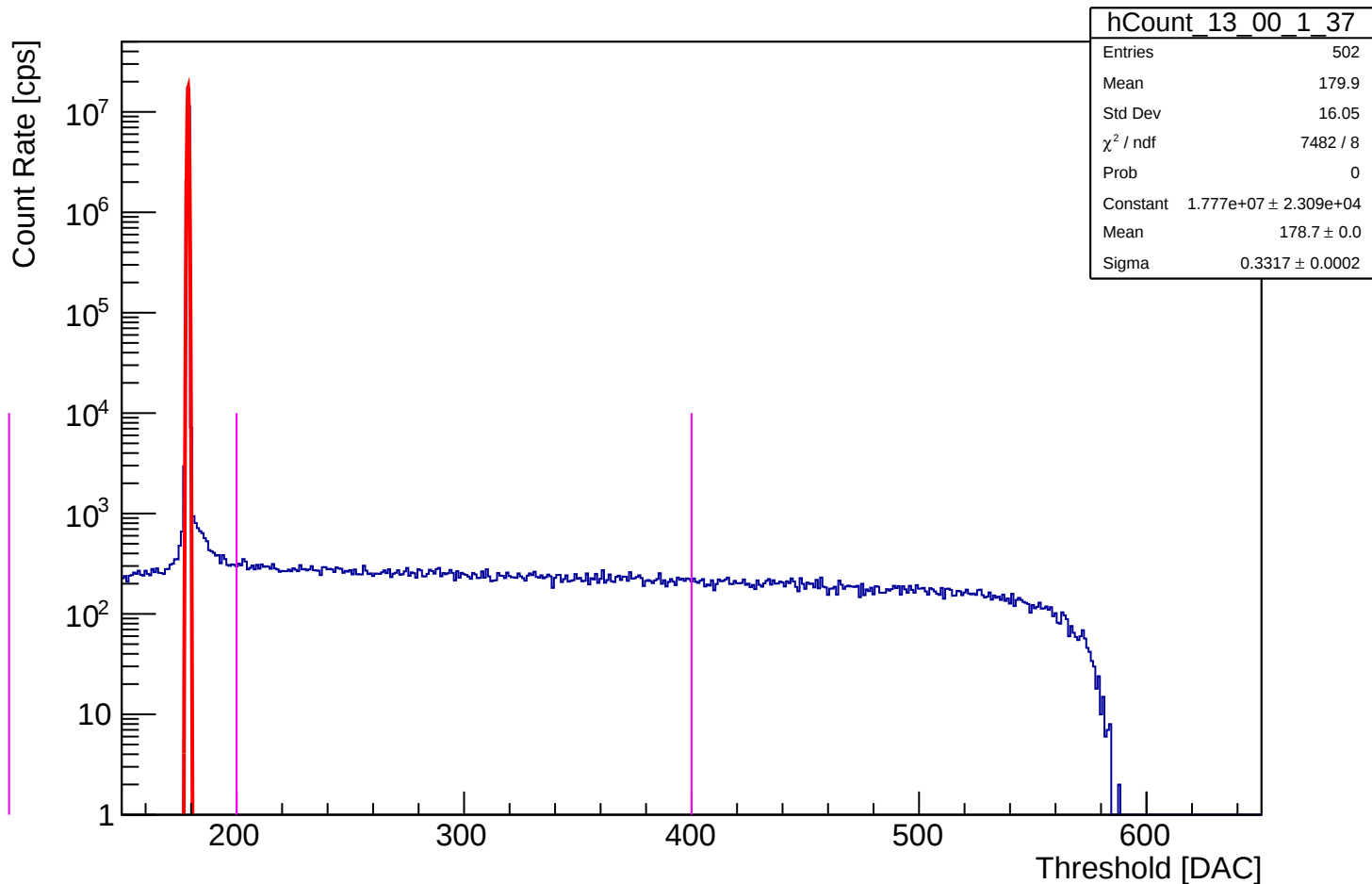
Row 1 Tile 1 Pmt 2 Pixel 13 Slot 13 Fiber 0 Asic 1 Channel 36



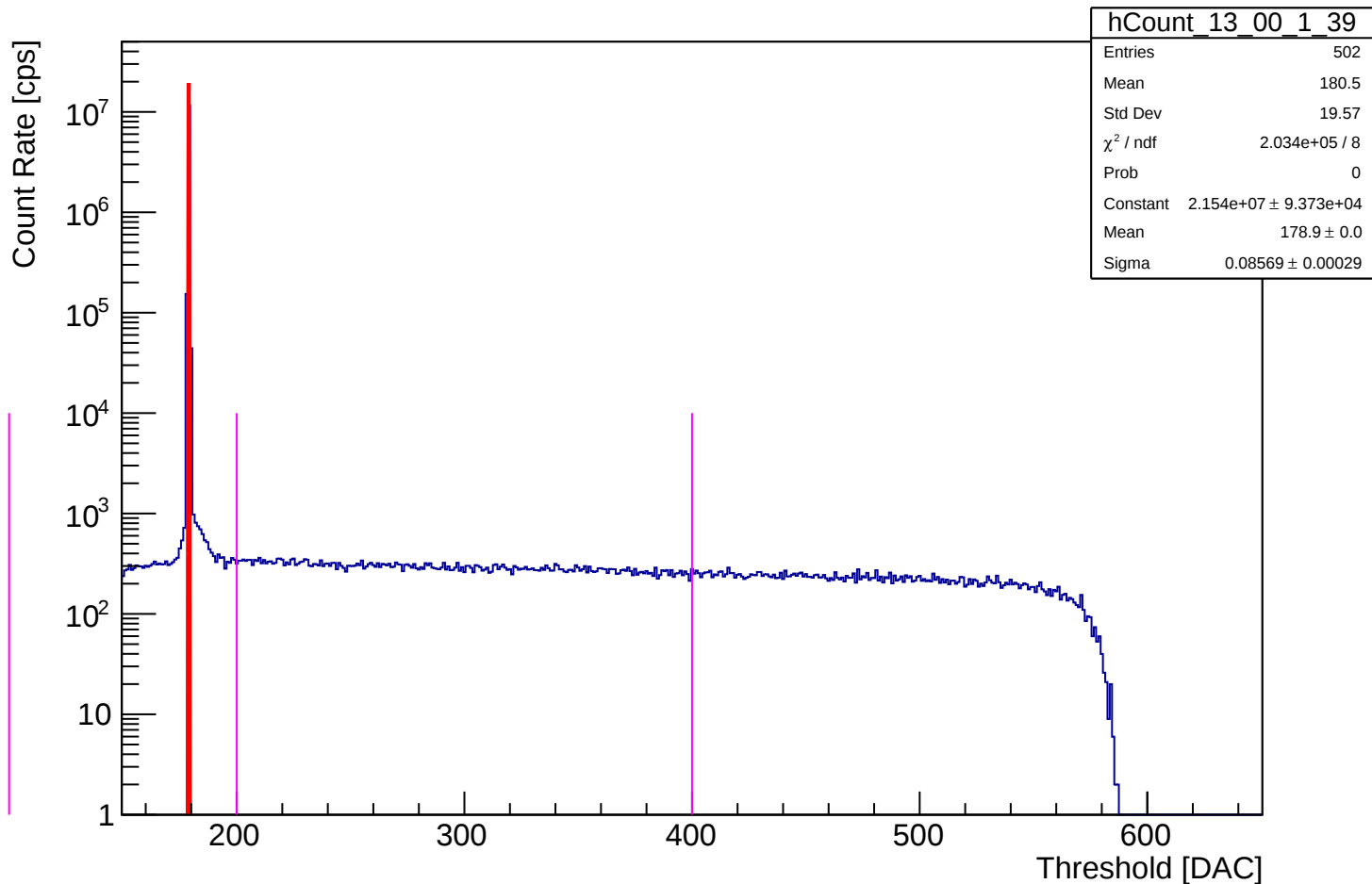
Row 1 Tile 1 Pmt 2 Pixel 14 Slot 13 Fiber 0 Asic 1 Channel 38



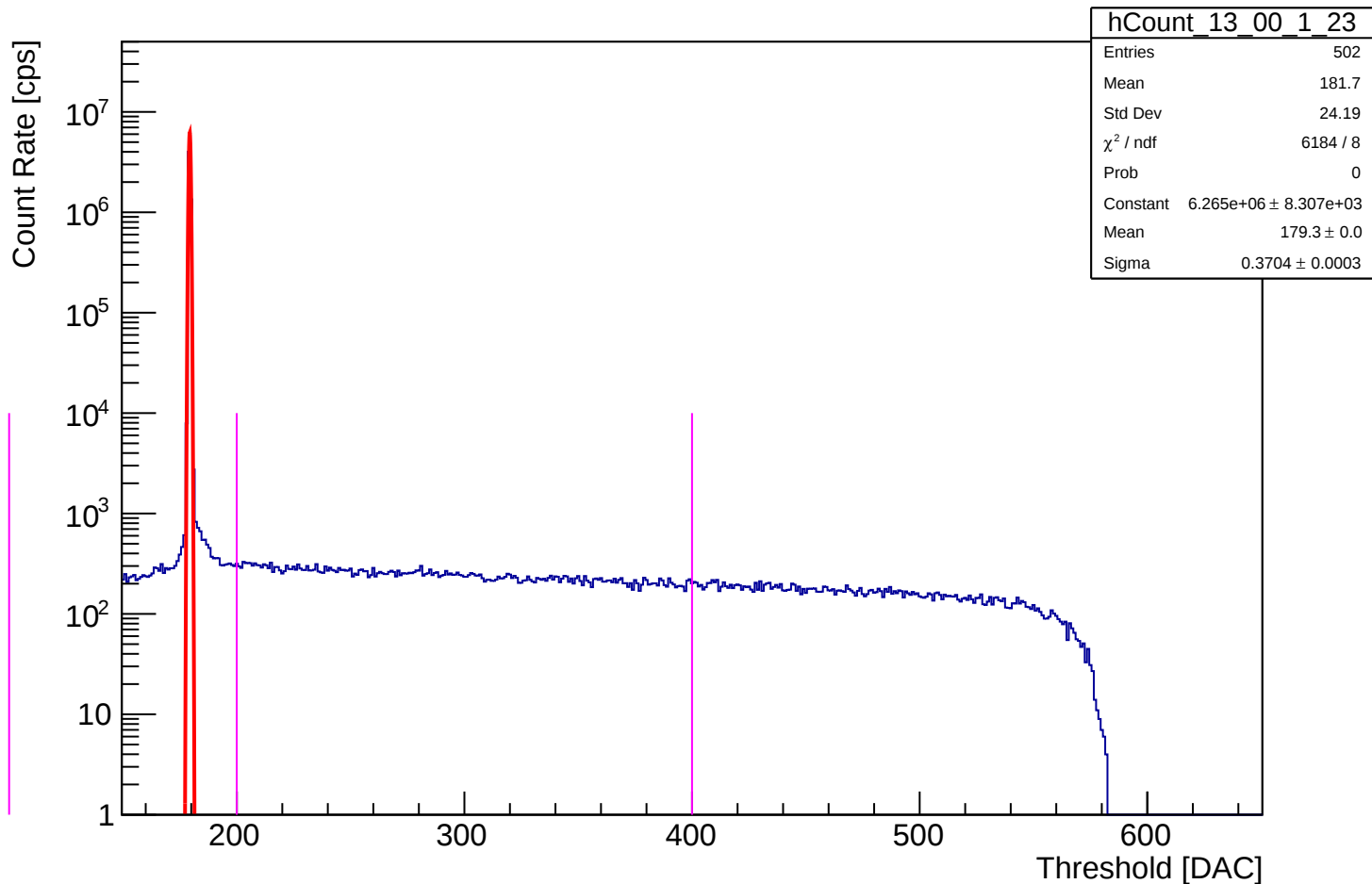
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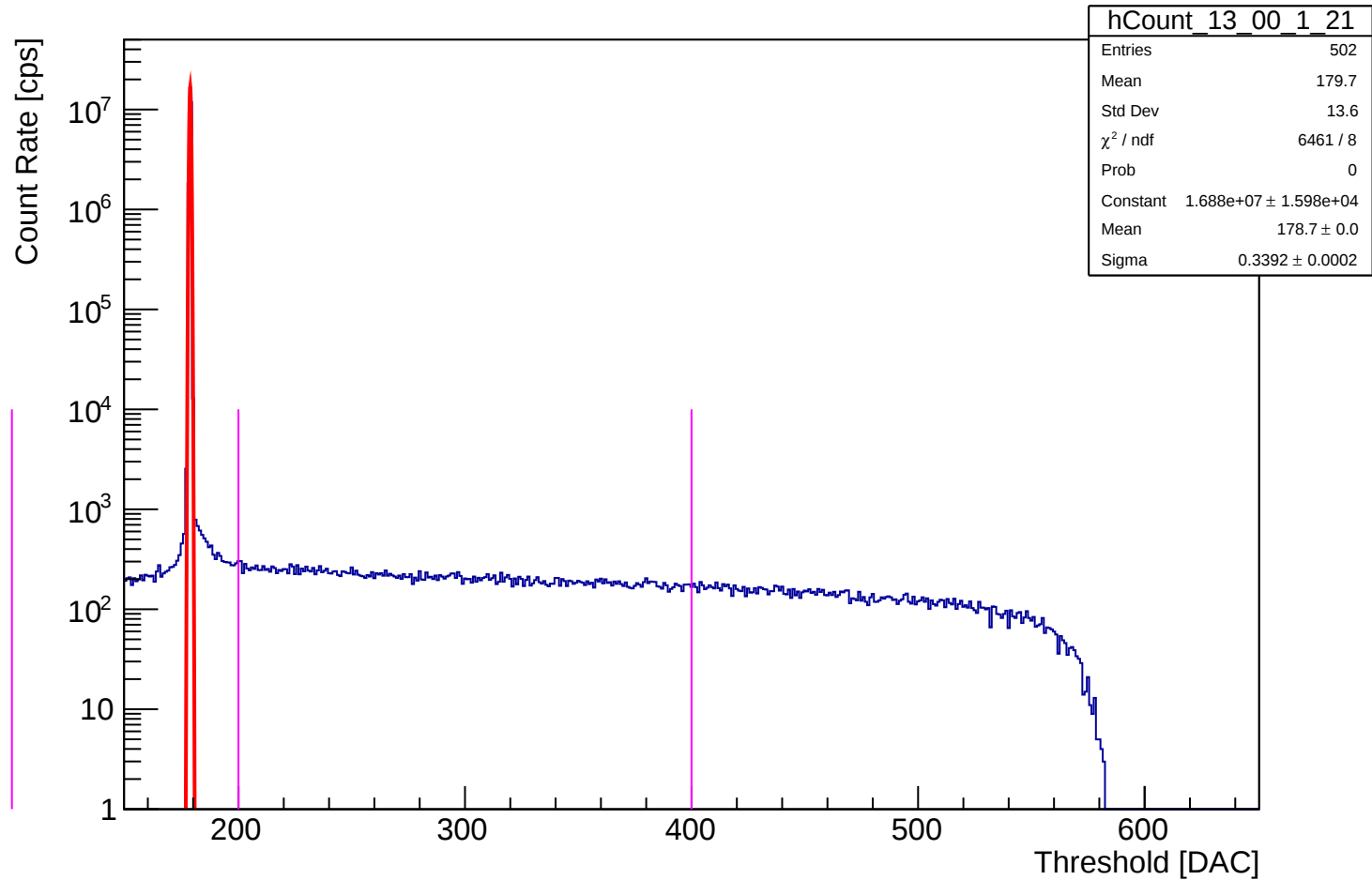


Row 1 Tile 1 Pmt 2 Pixel 16 Slot 13 Fiber 0 Asic 1 Channel 39

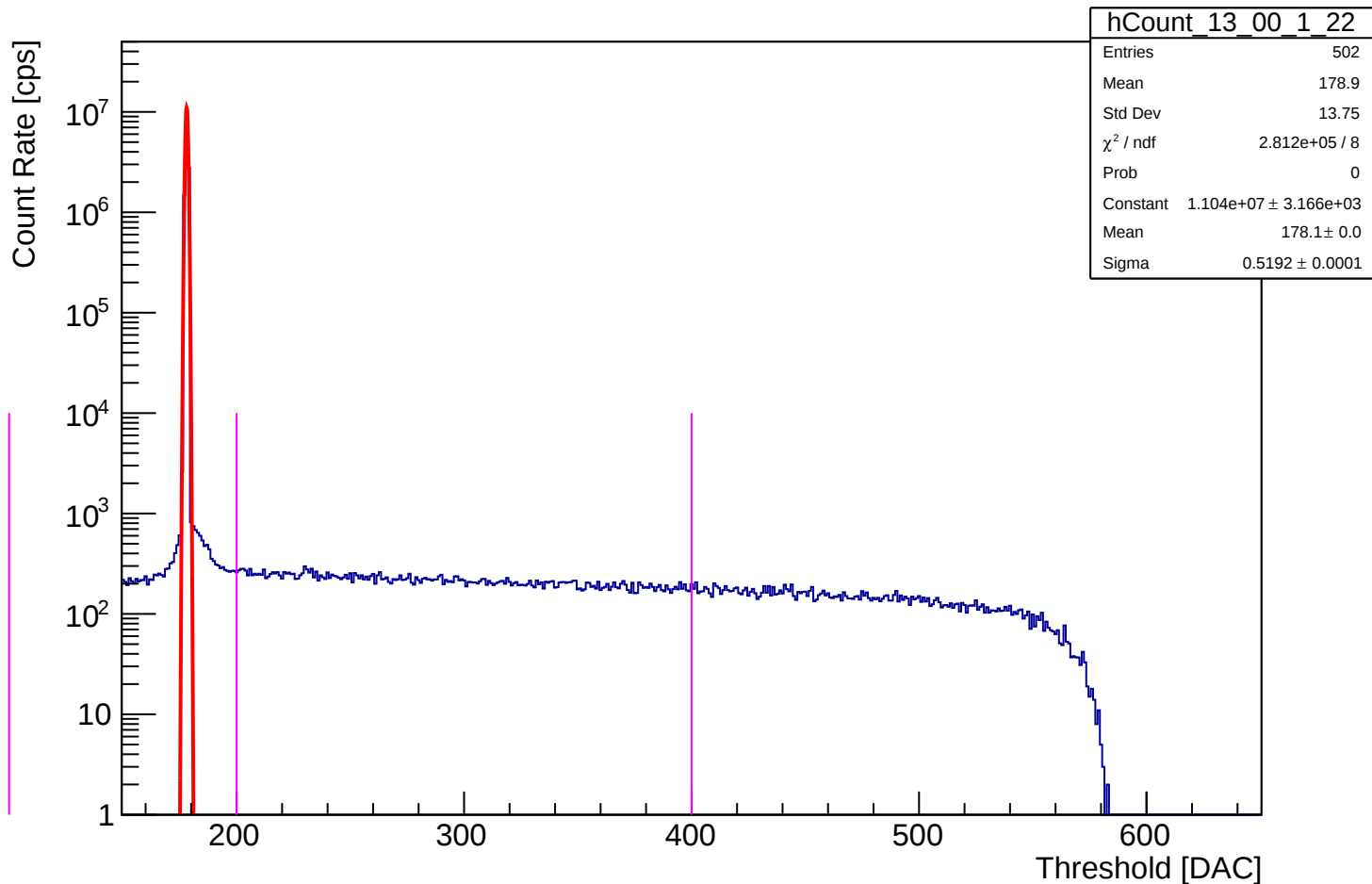


Row 1 Tile 1 Pmt 2 Pixel 17 Slot 13 Fiber 0 Asic 1 Channel 23

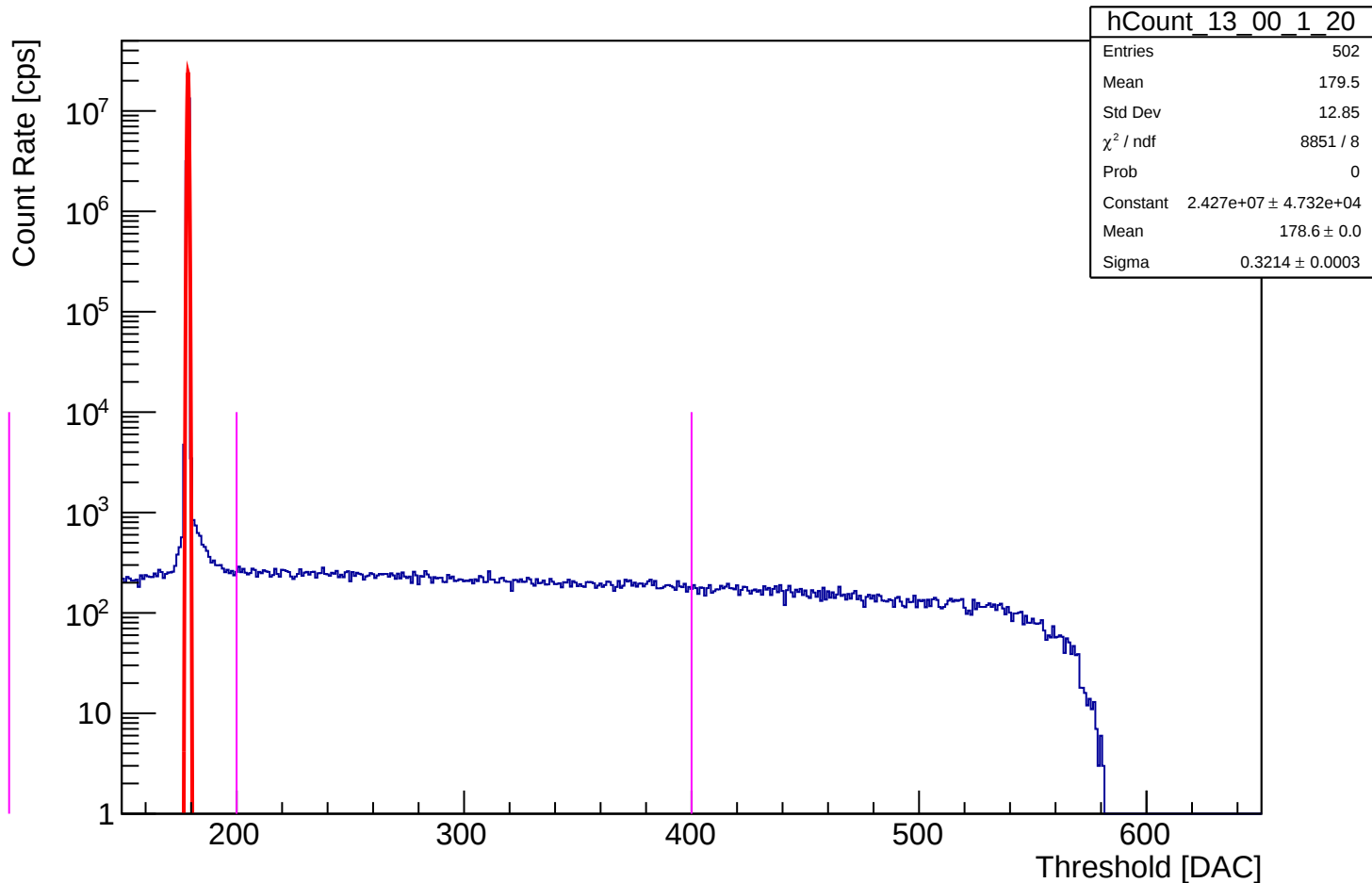




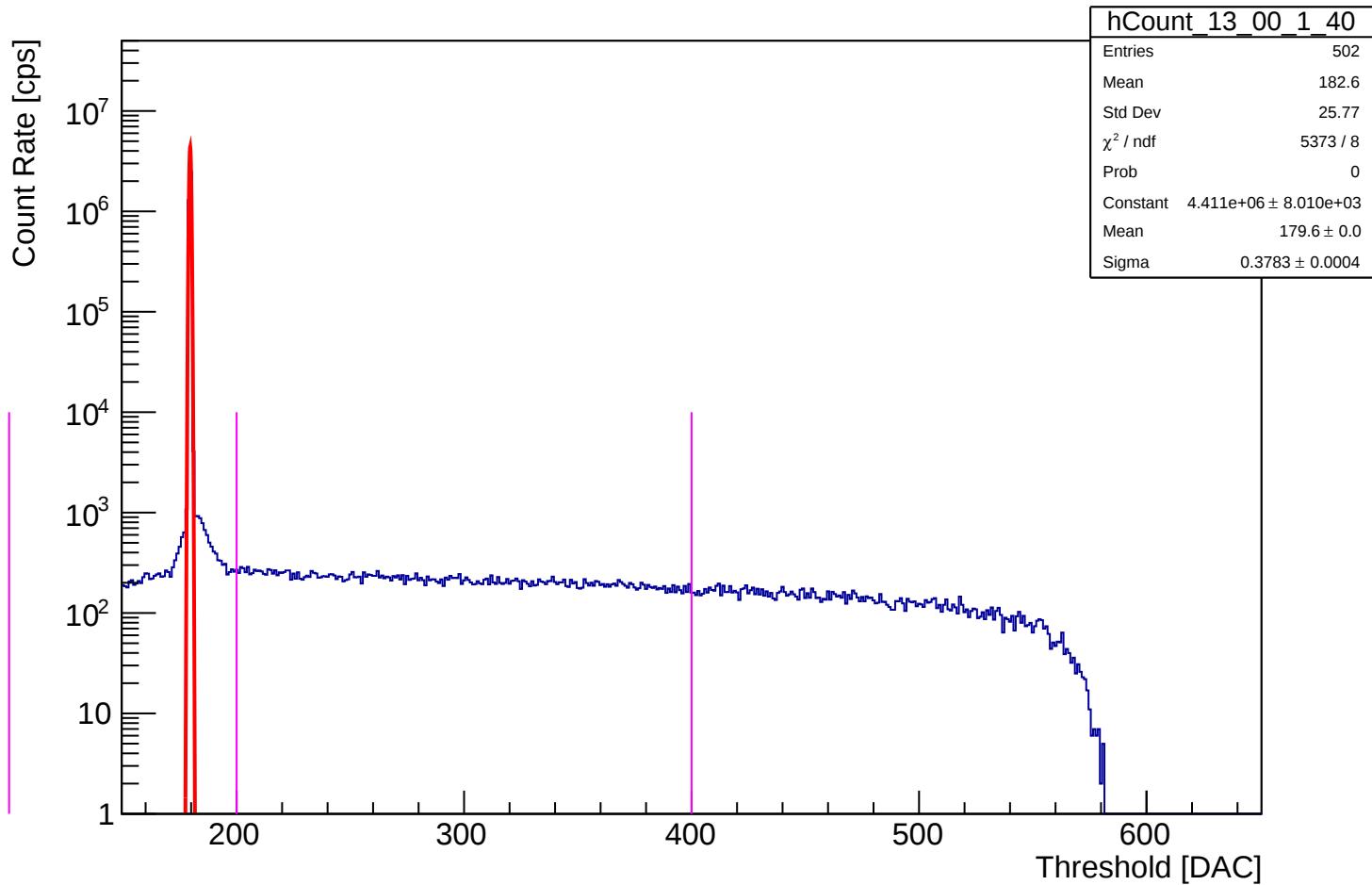
Row 1 Tile 1 Pmt 2 Pixel 19 Slot 13 Fiber 0 Asic 1 Channel 22



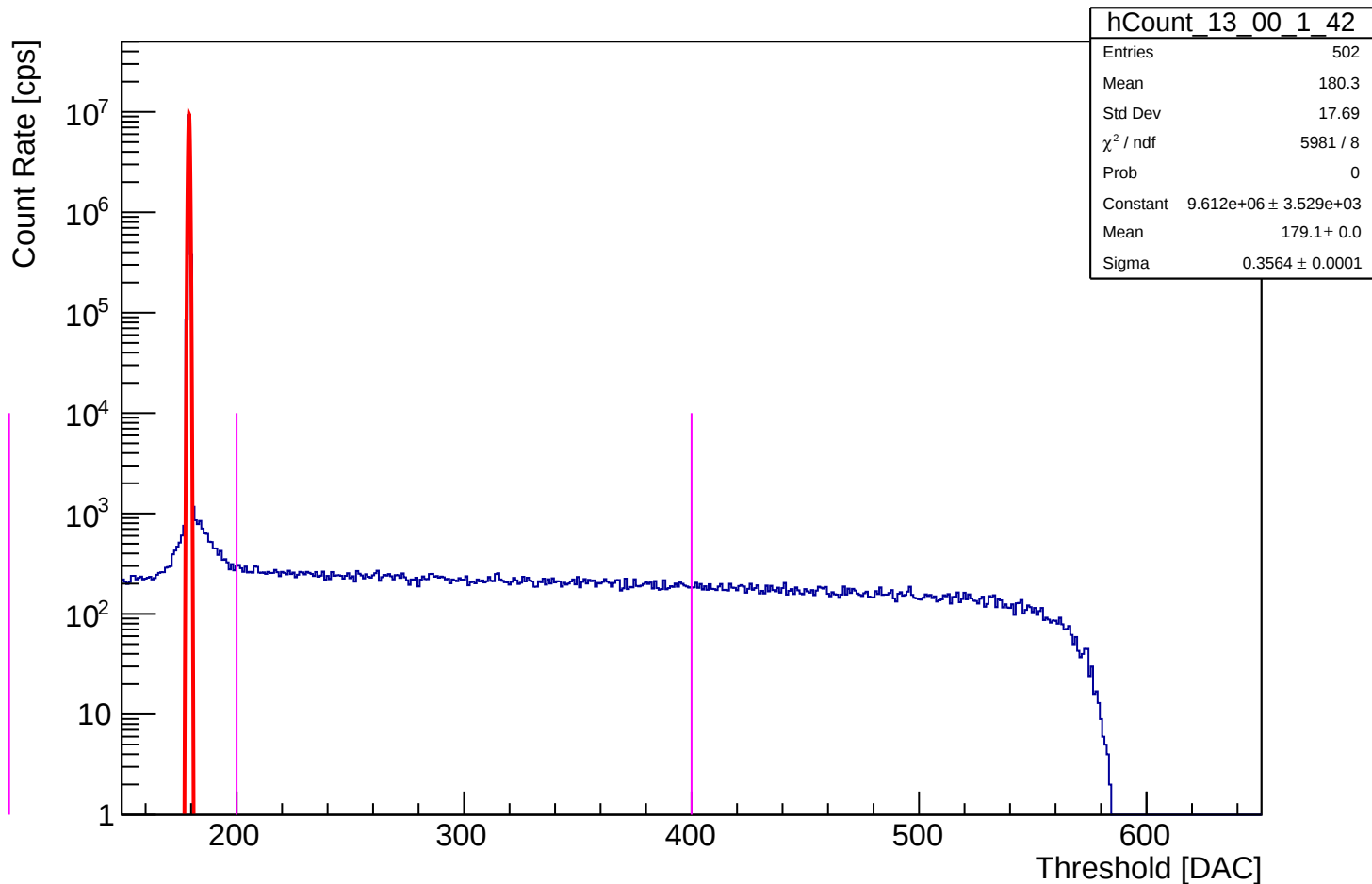
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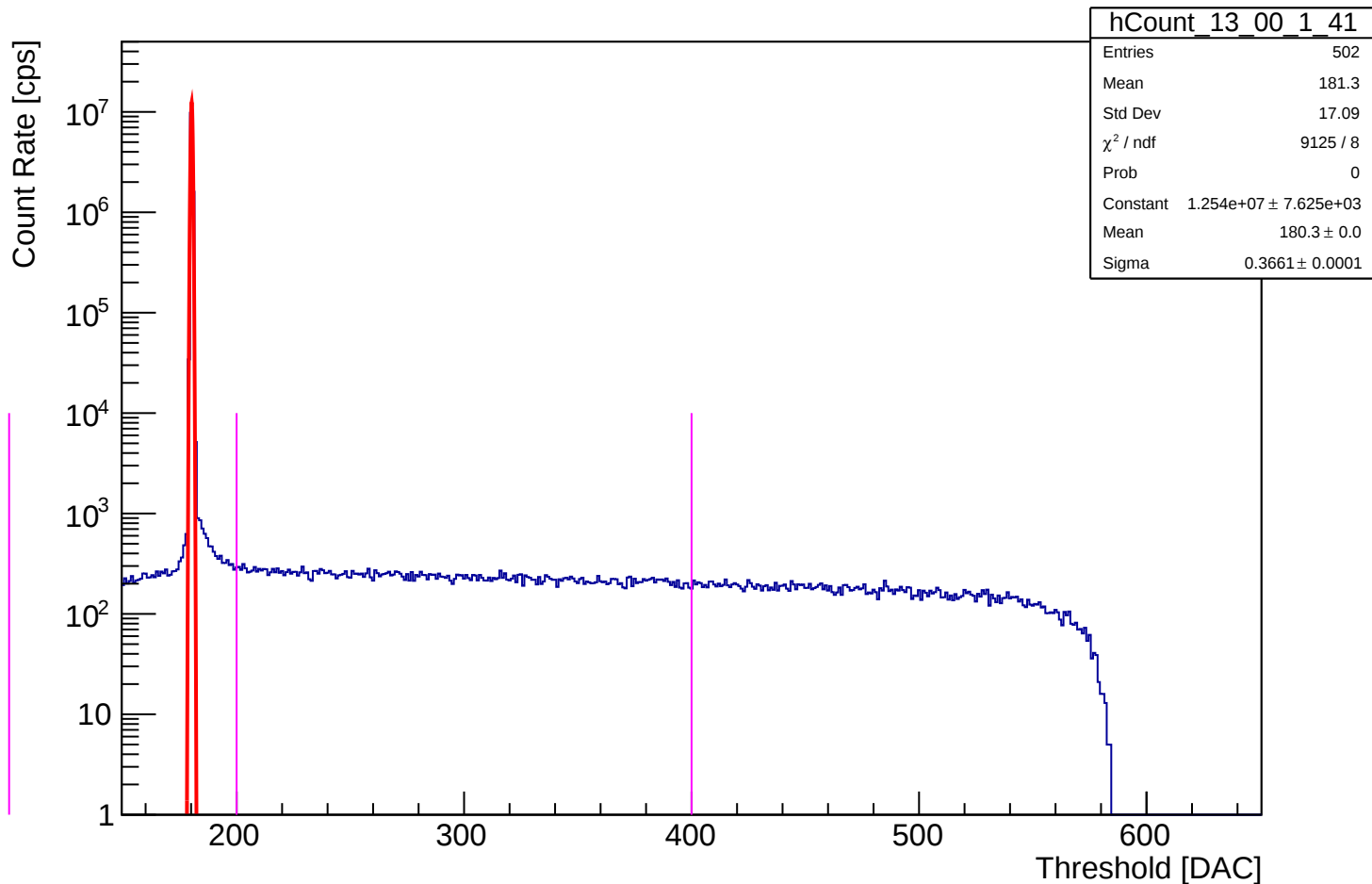
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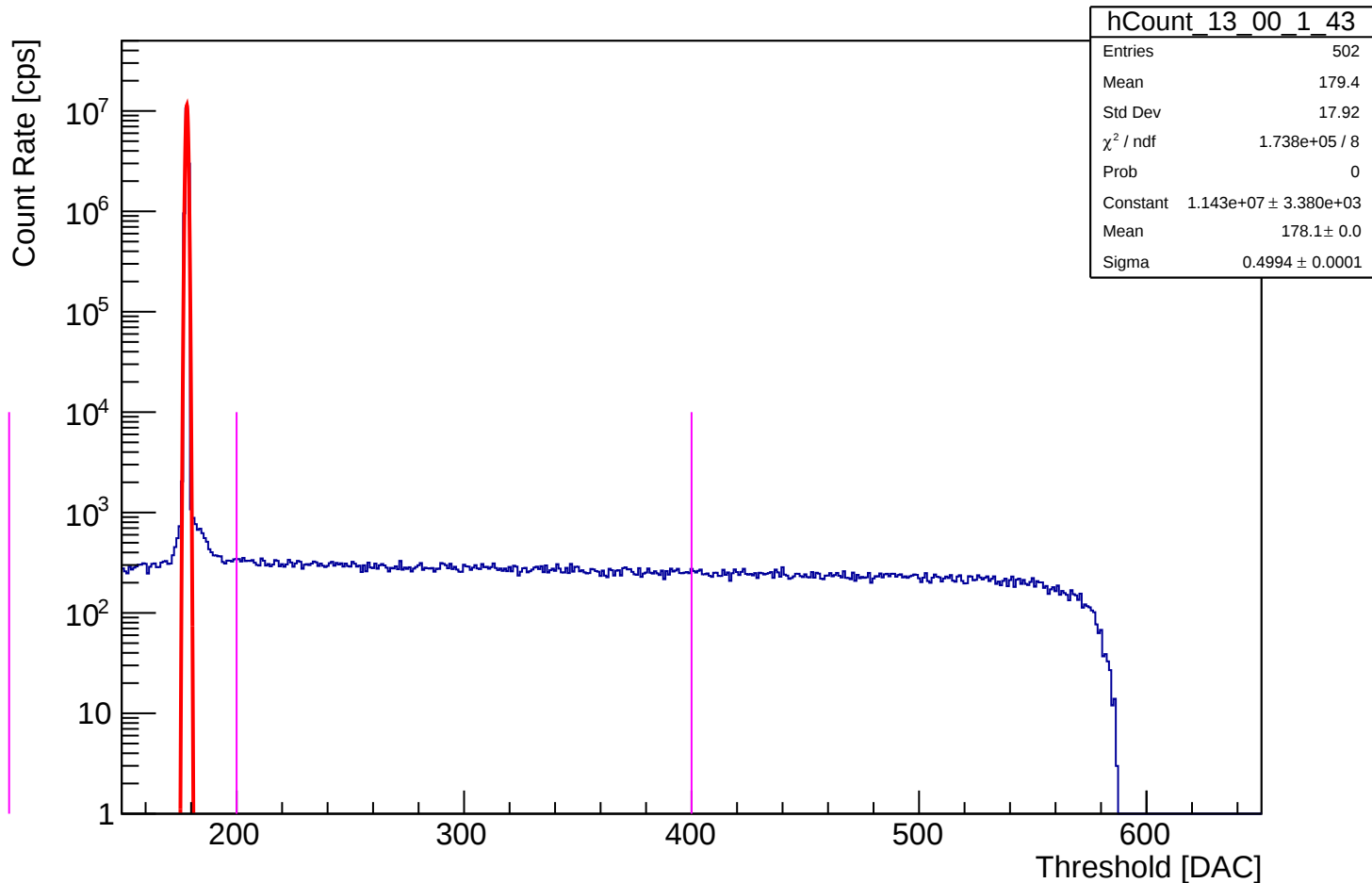
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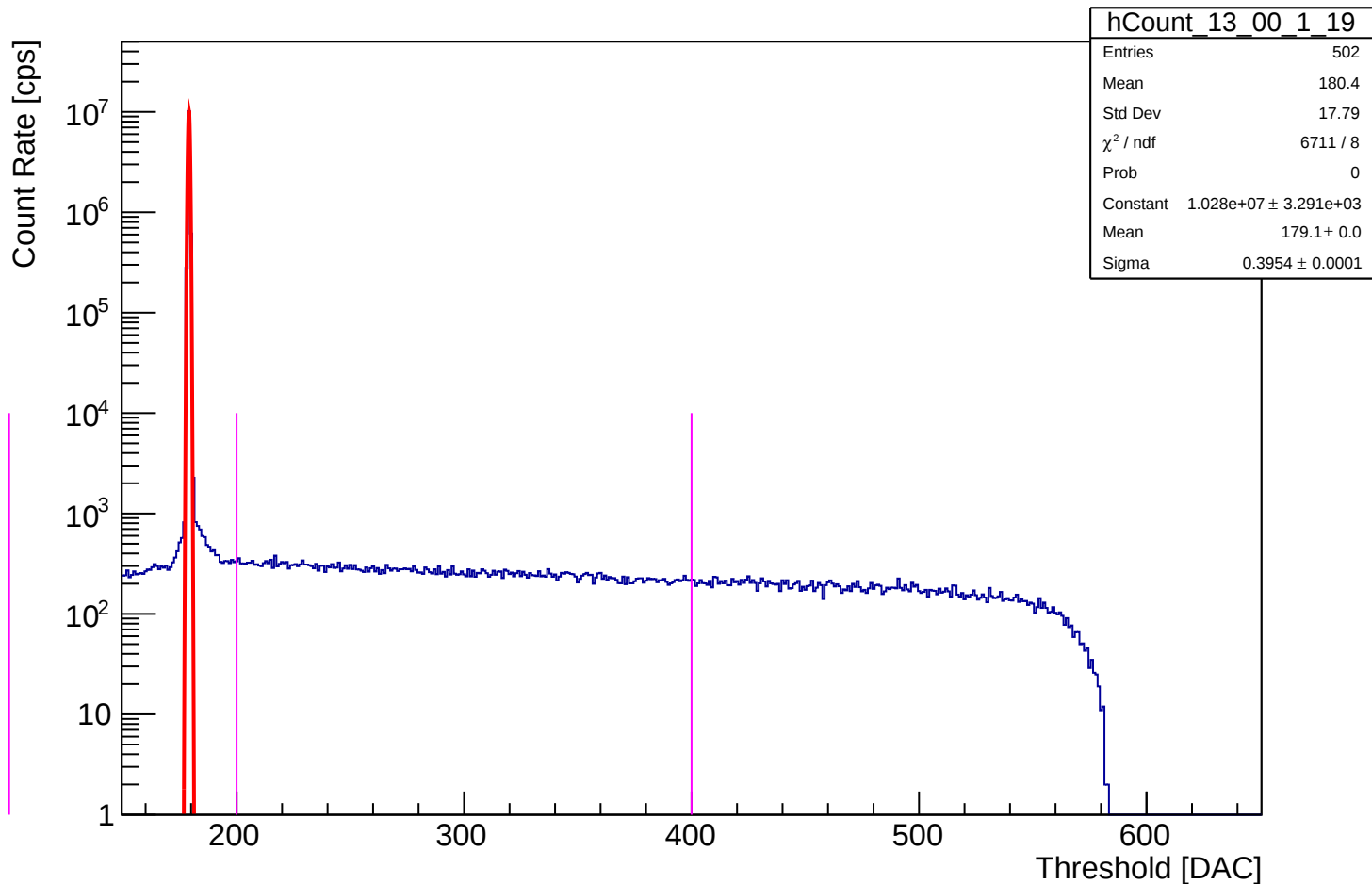
Row 1 Tile 1 Pmt 2 Pixel 23 Slot 13 Fiber 0 Asic 1 Channel 41



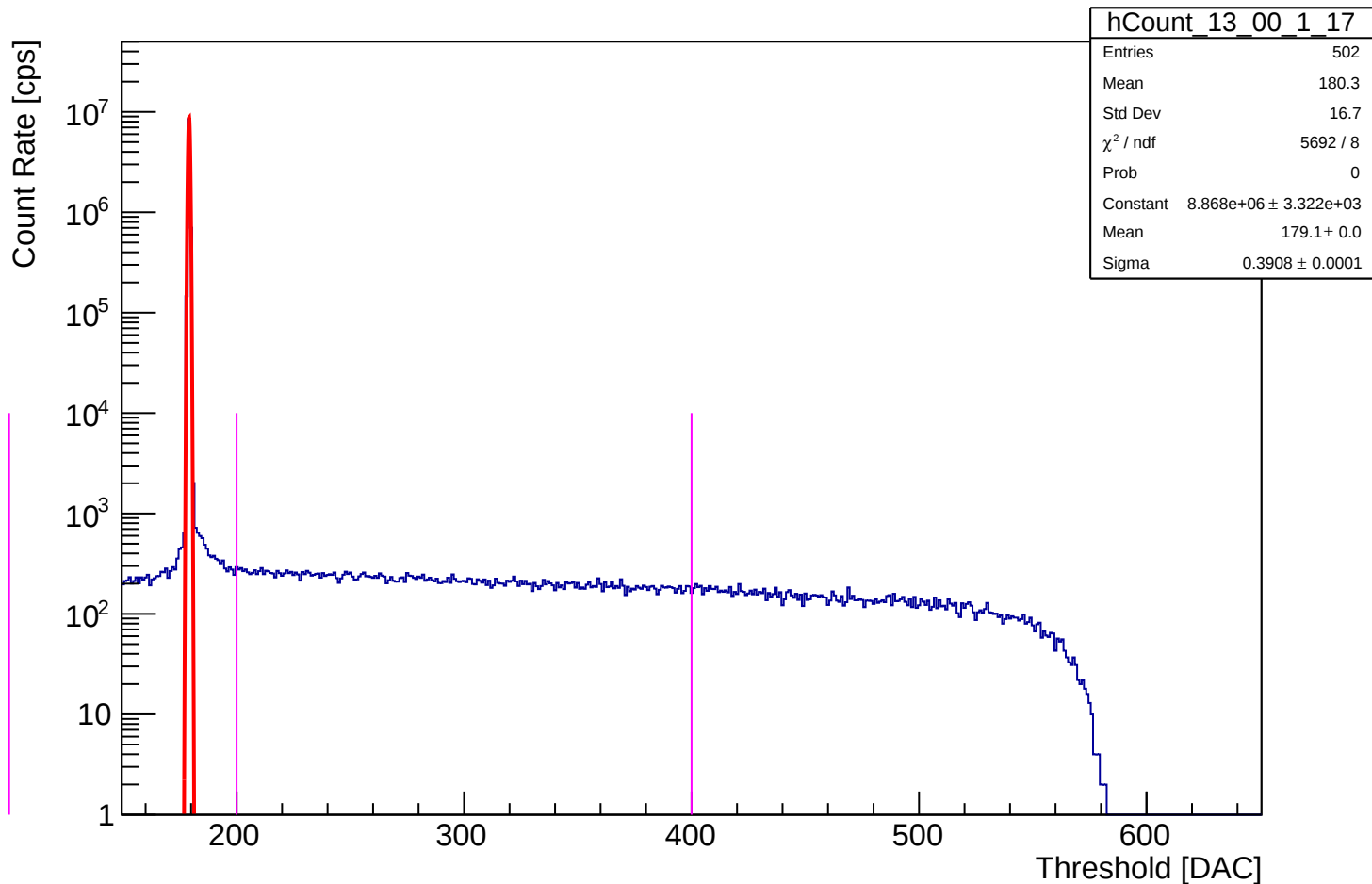
Row 1 Tile 1 Pmt 2 Pixel 24 Slot 13 Fiber 0 Asic 1 Channel 43



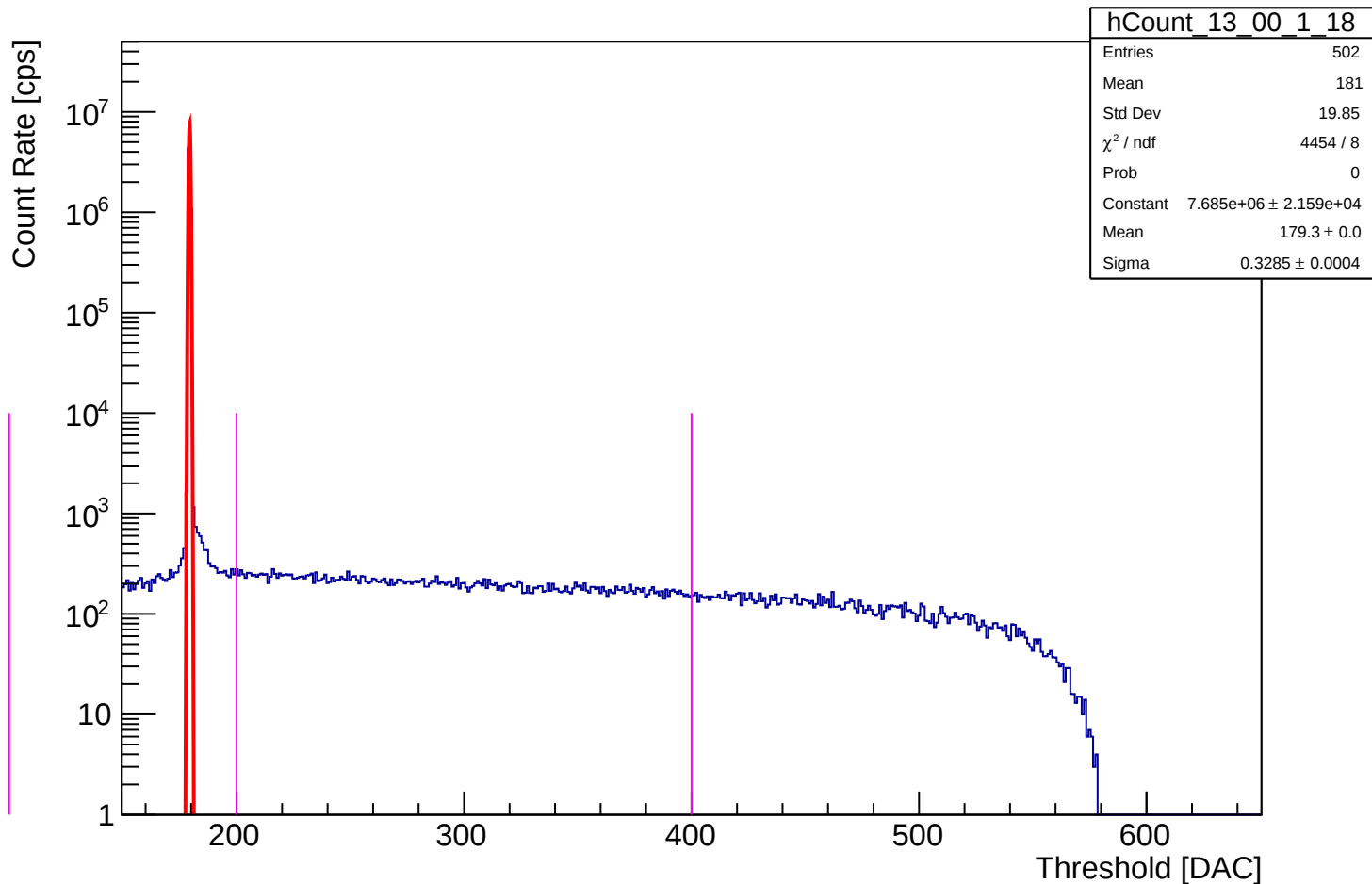
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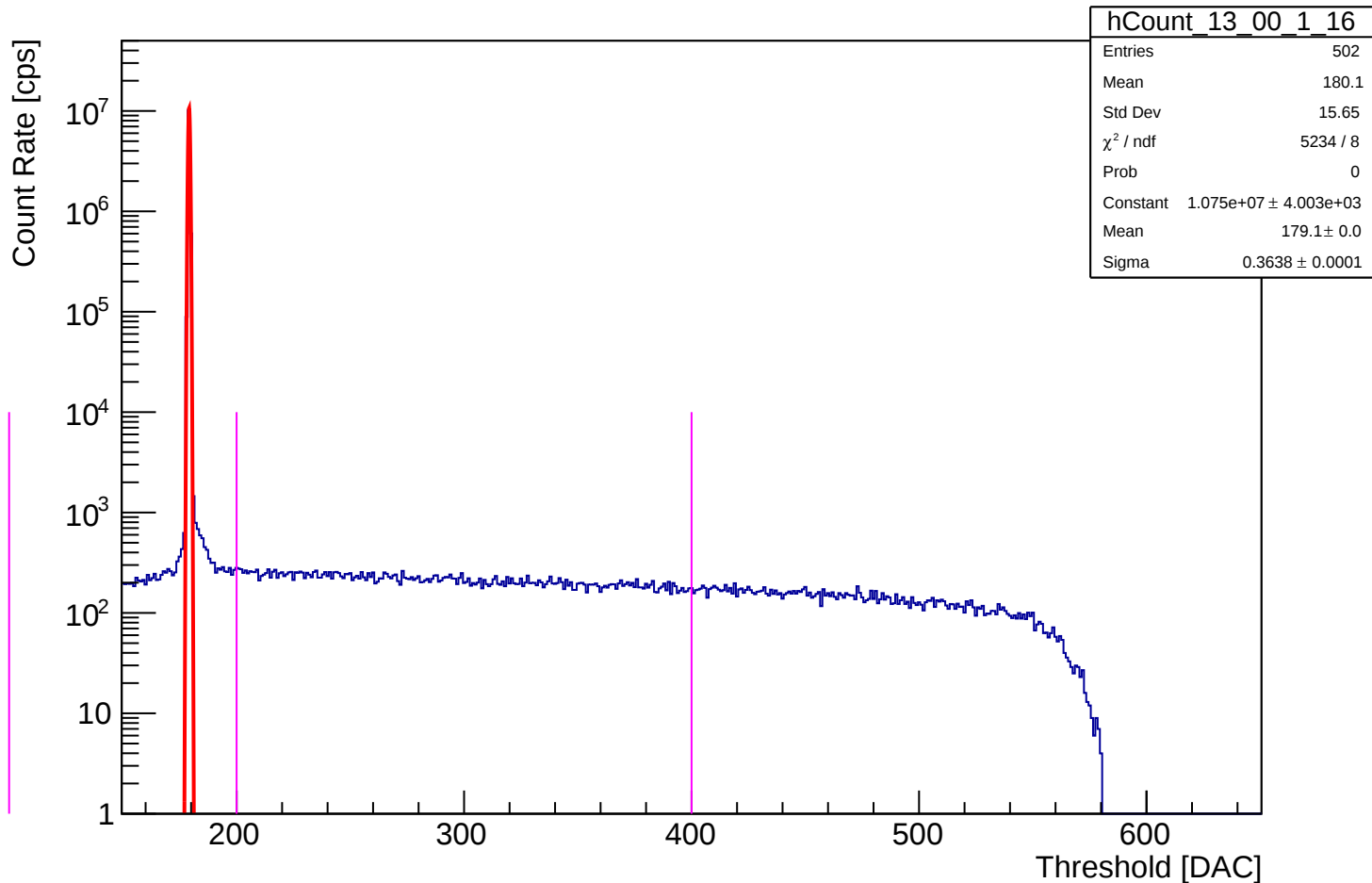
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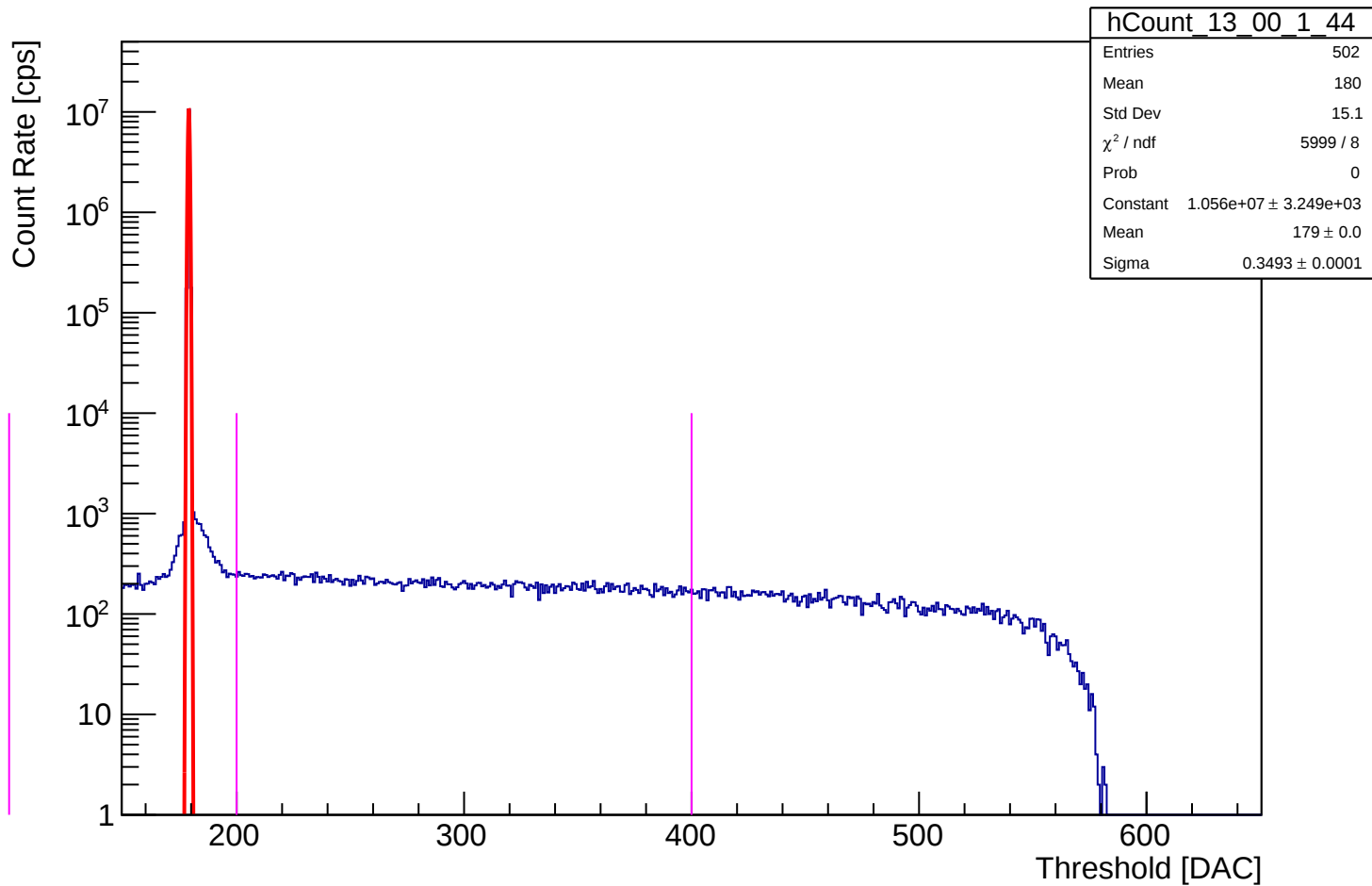
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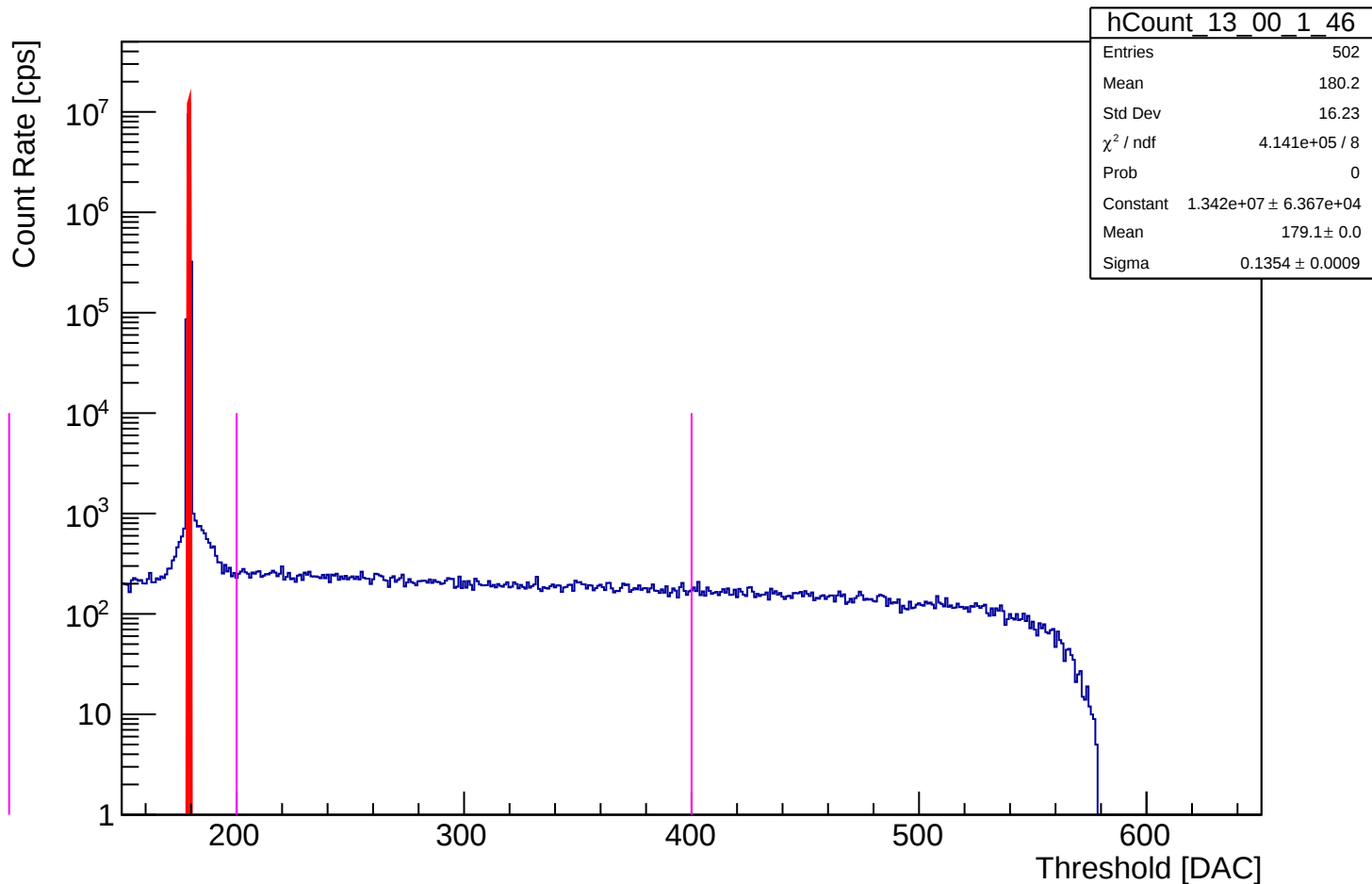
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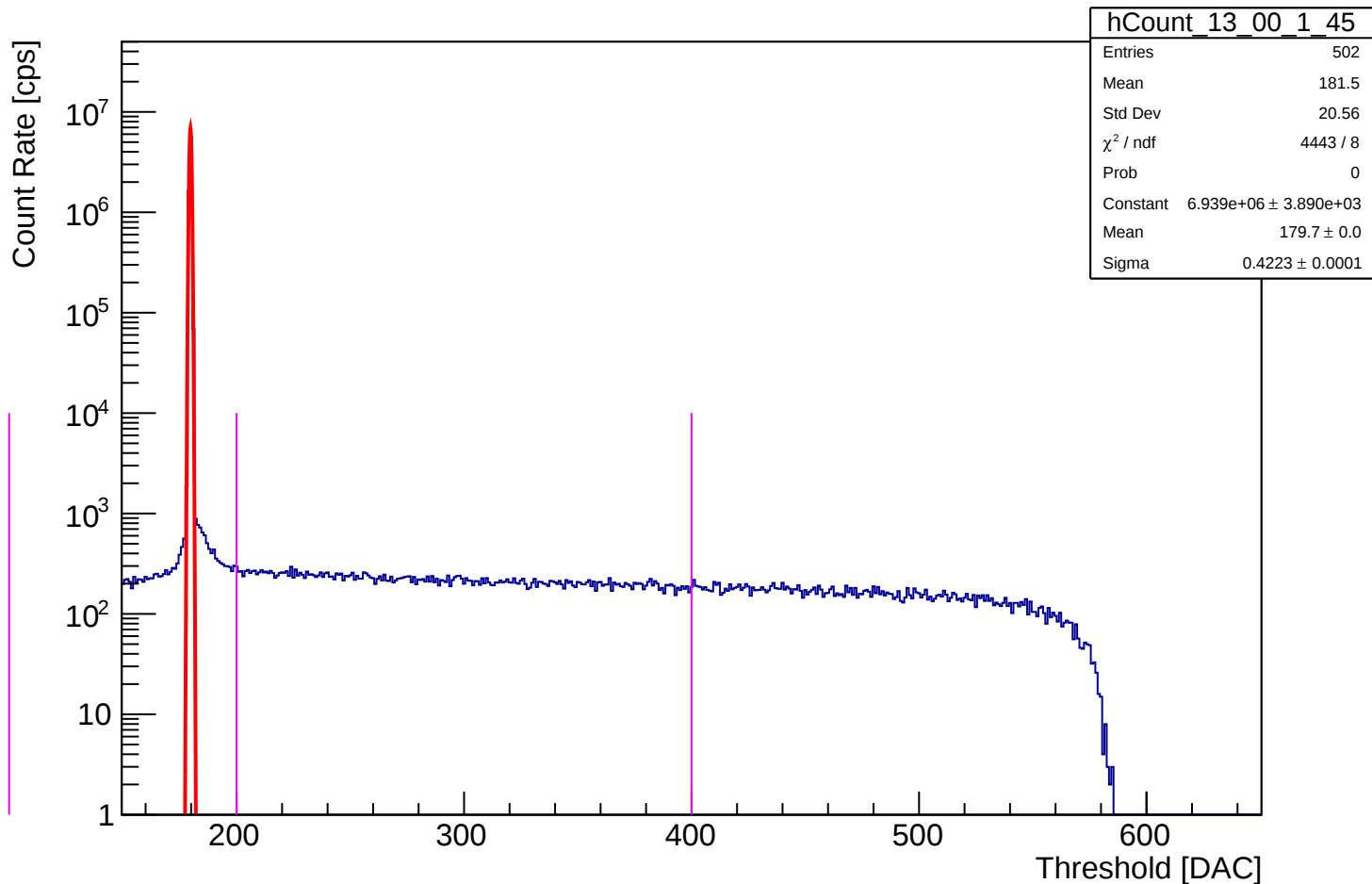
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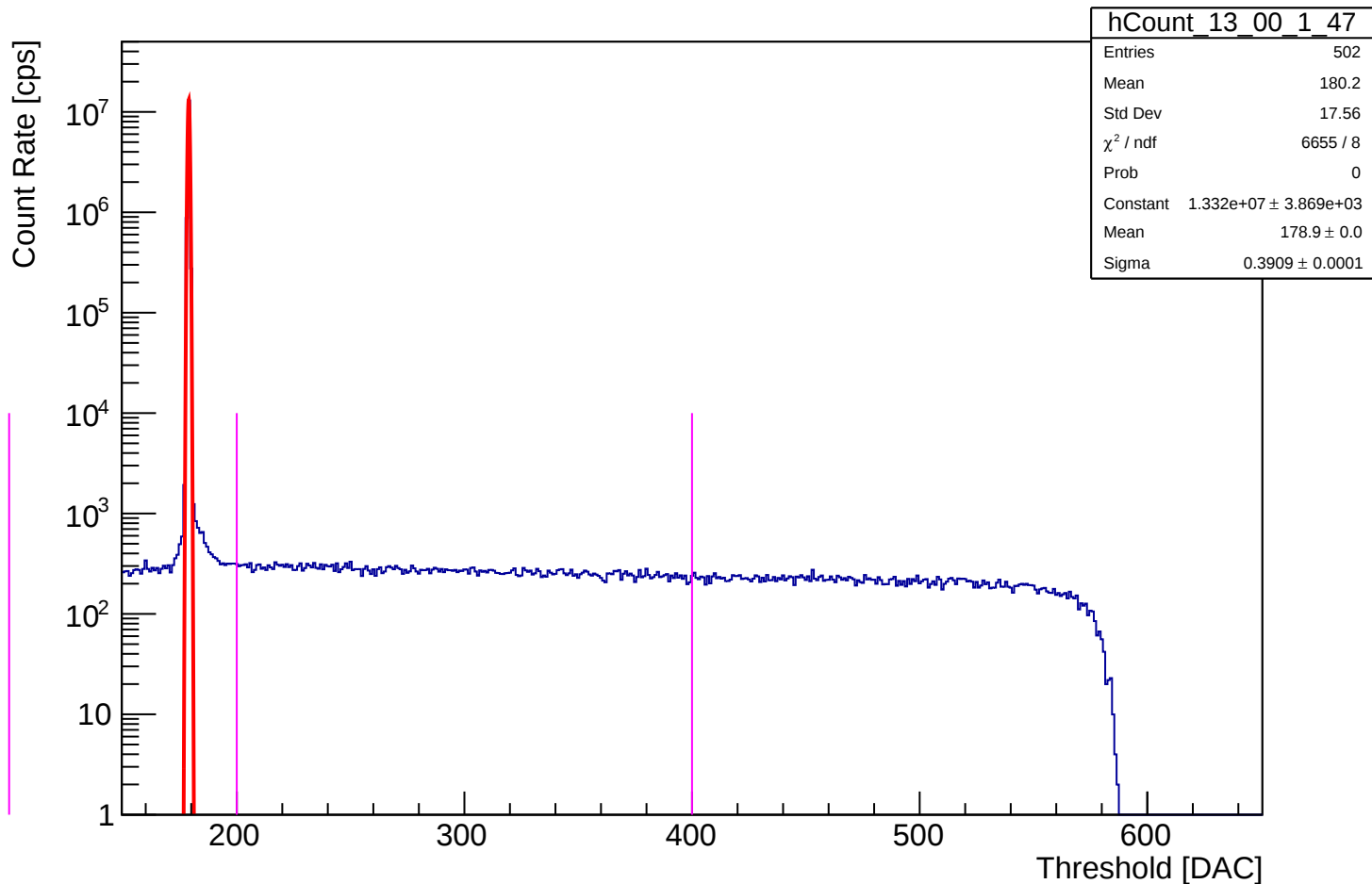
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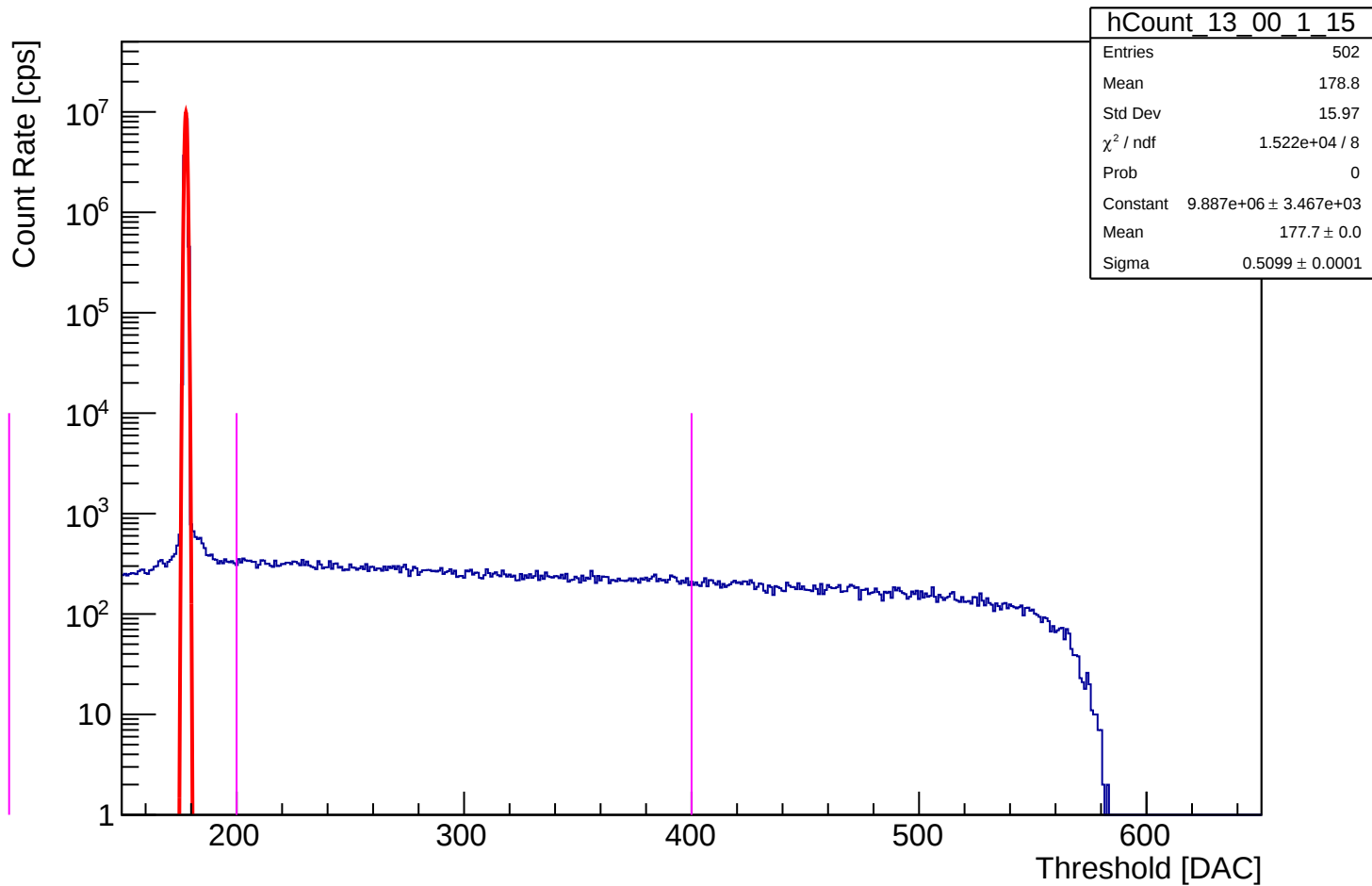
Row 1 Tile 1 Pmt 2 Pixel 31 Slot 13 Fiber 0 Asic 1 Channel 45



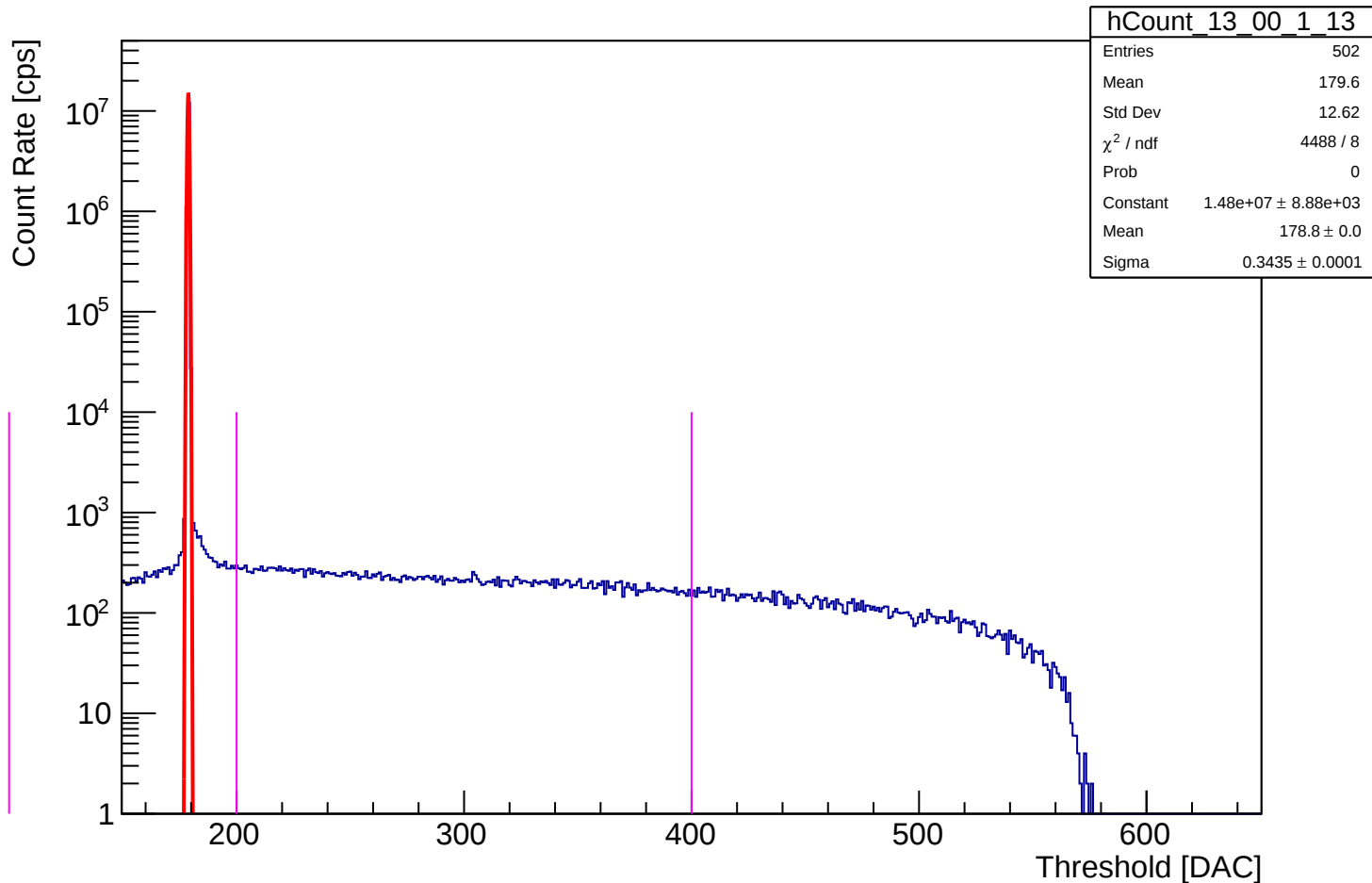
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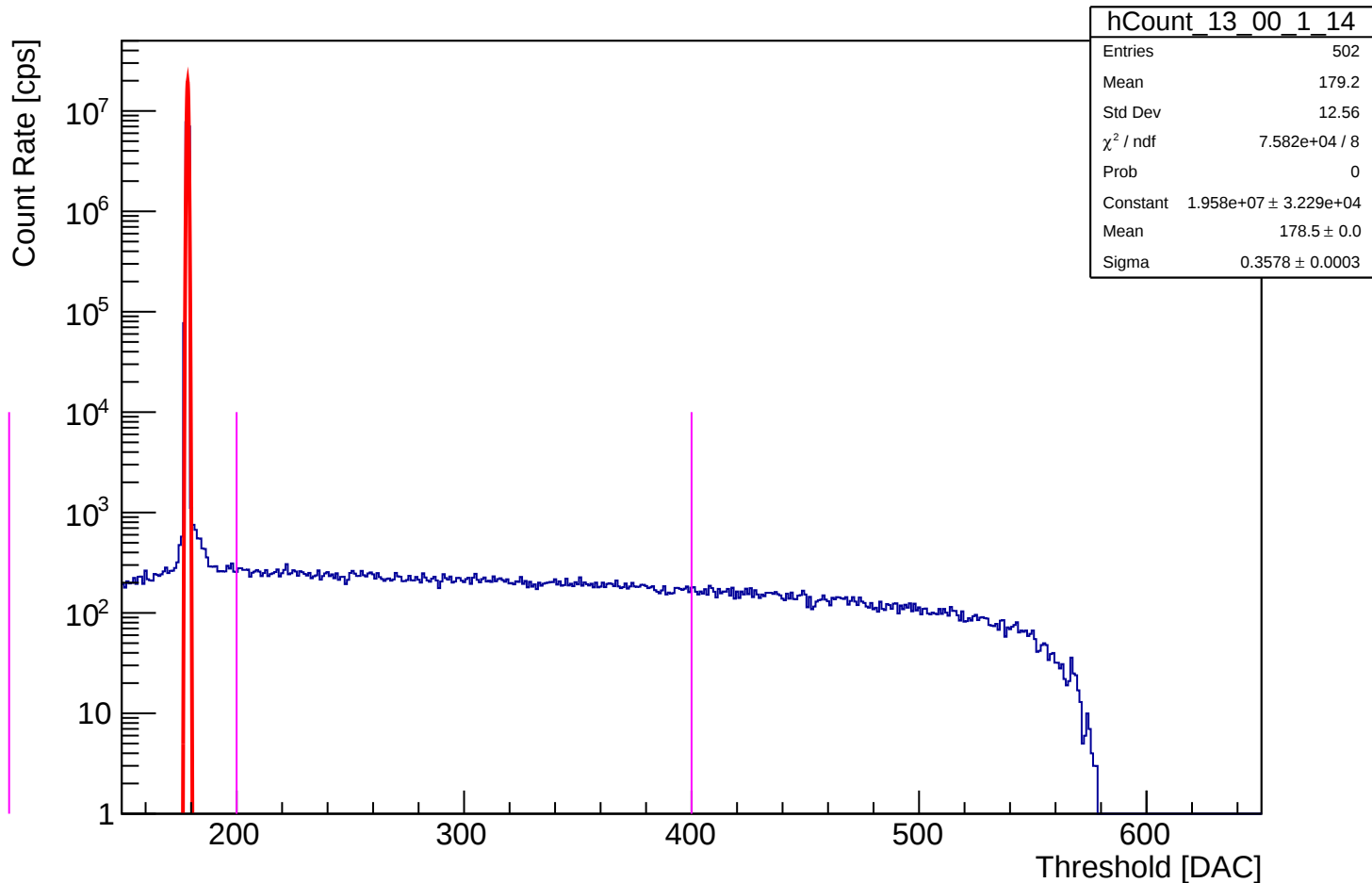
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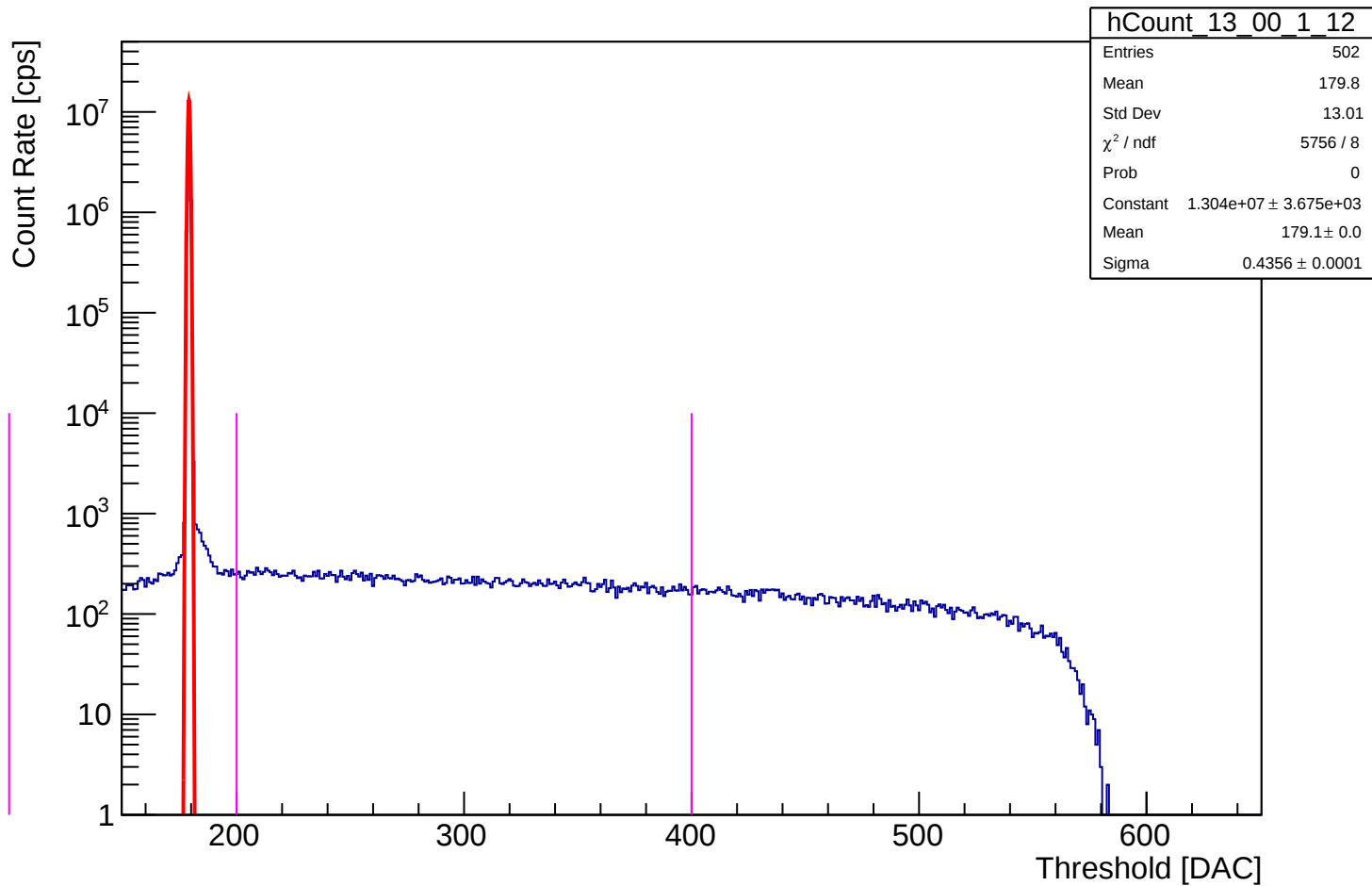
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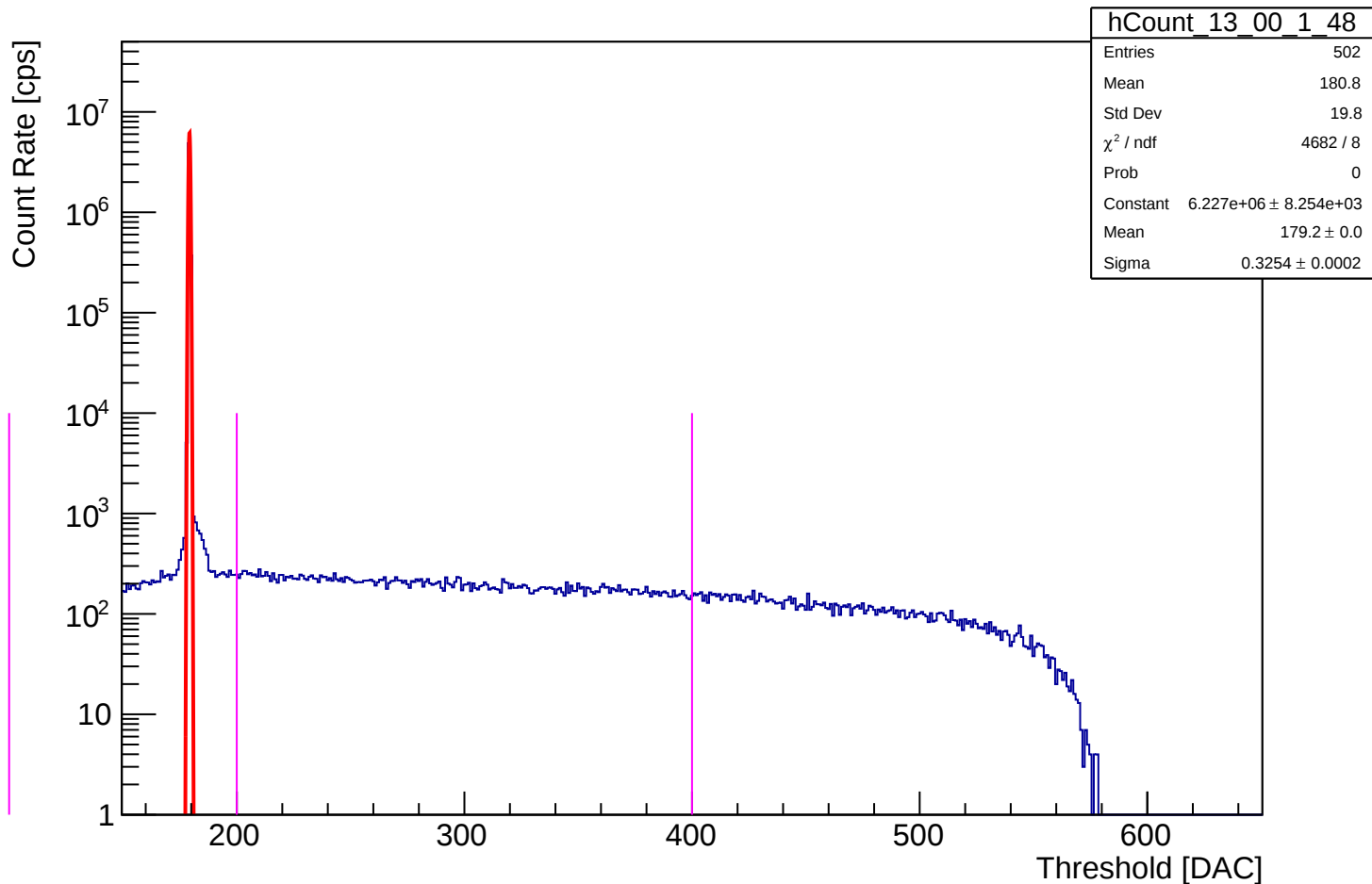
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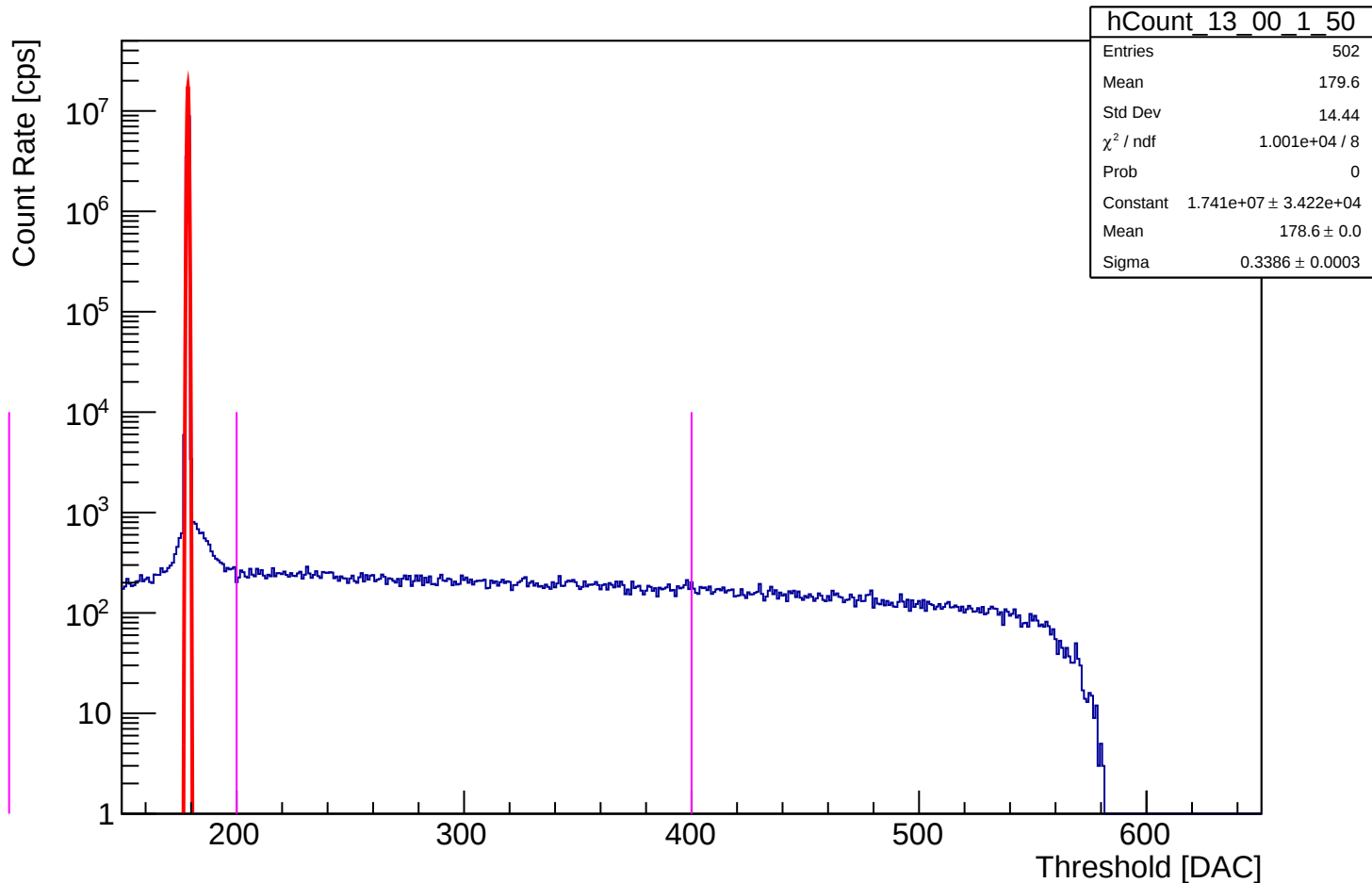
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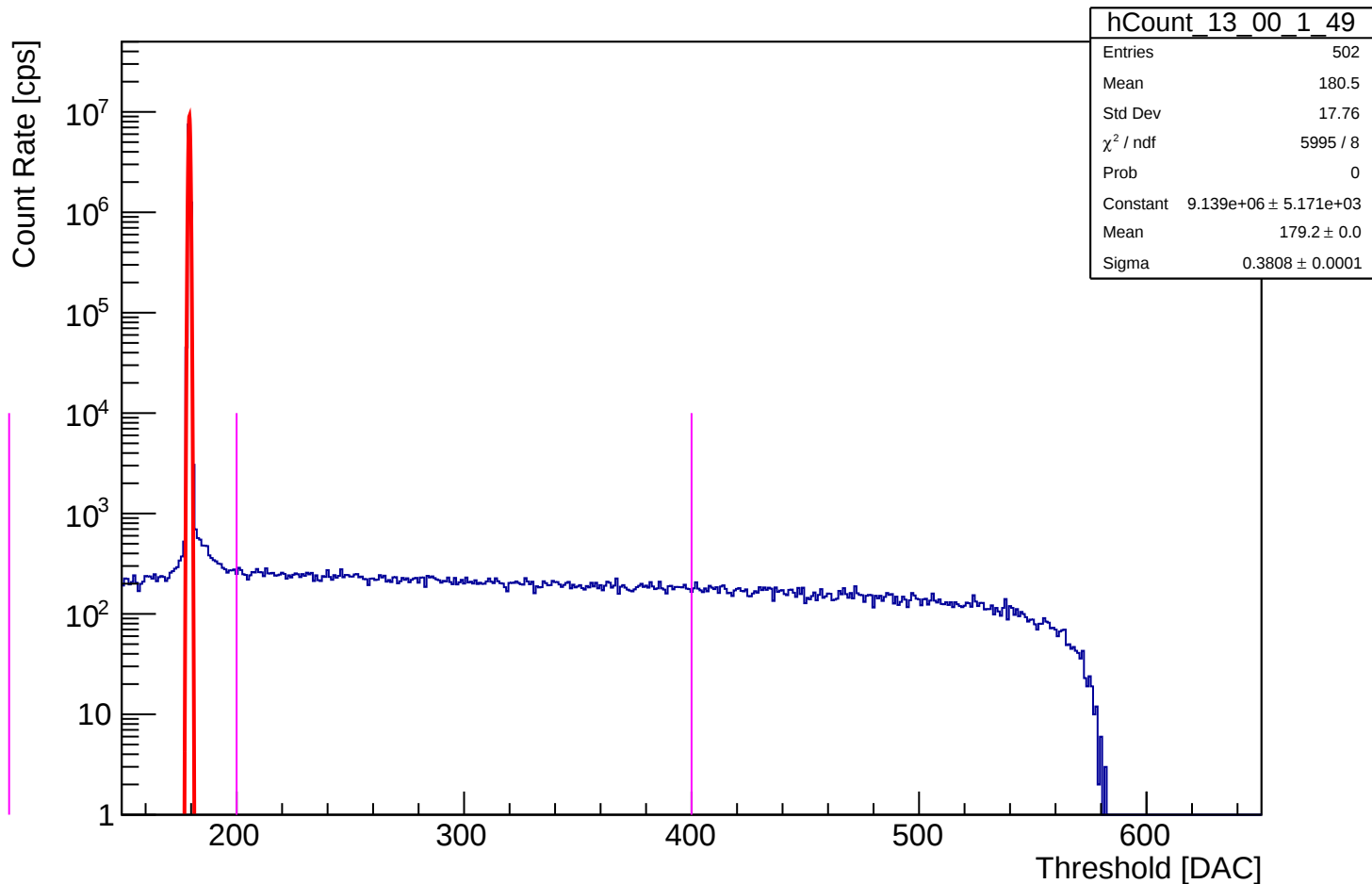
Row 1 Tile 1 Pmt 2 Pixel 37 Slot 13 Fiber 0 Asic 1 Channel 48

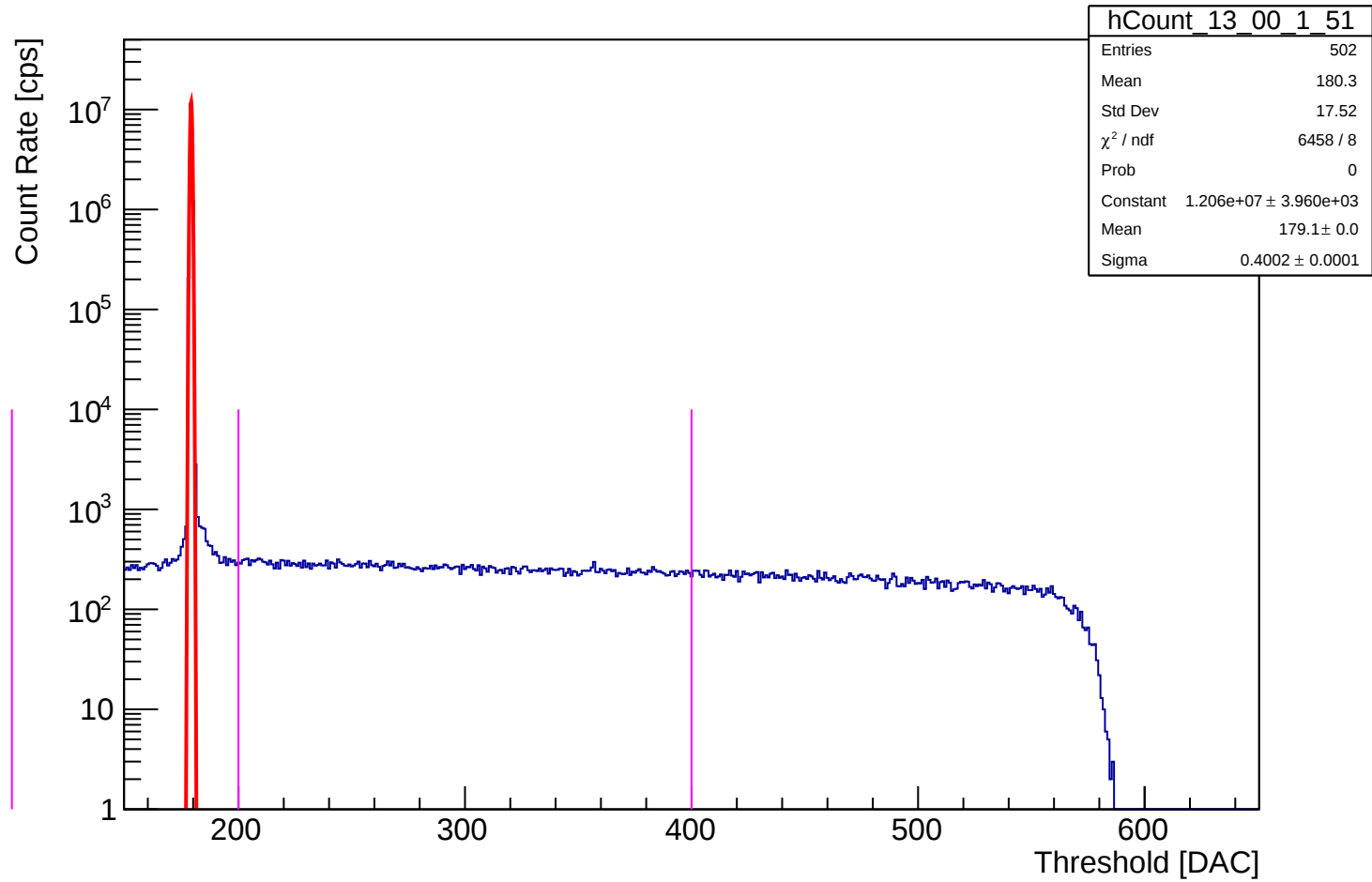


Row 1 Tile 1 Pmt 2 Pixel 38 Slot 13 Fiber 0 Asic 1 Channel 50



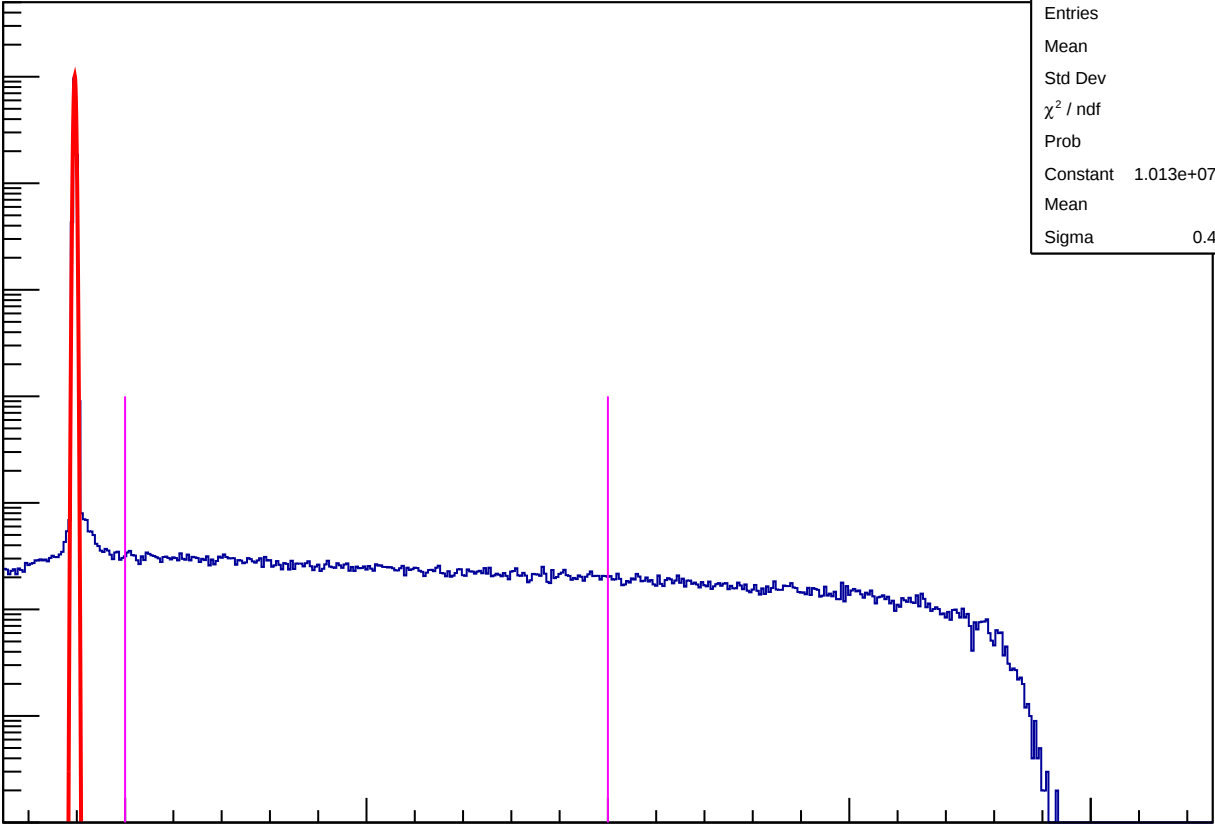
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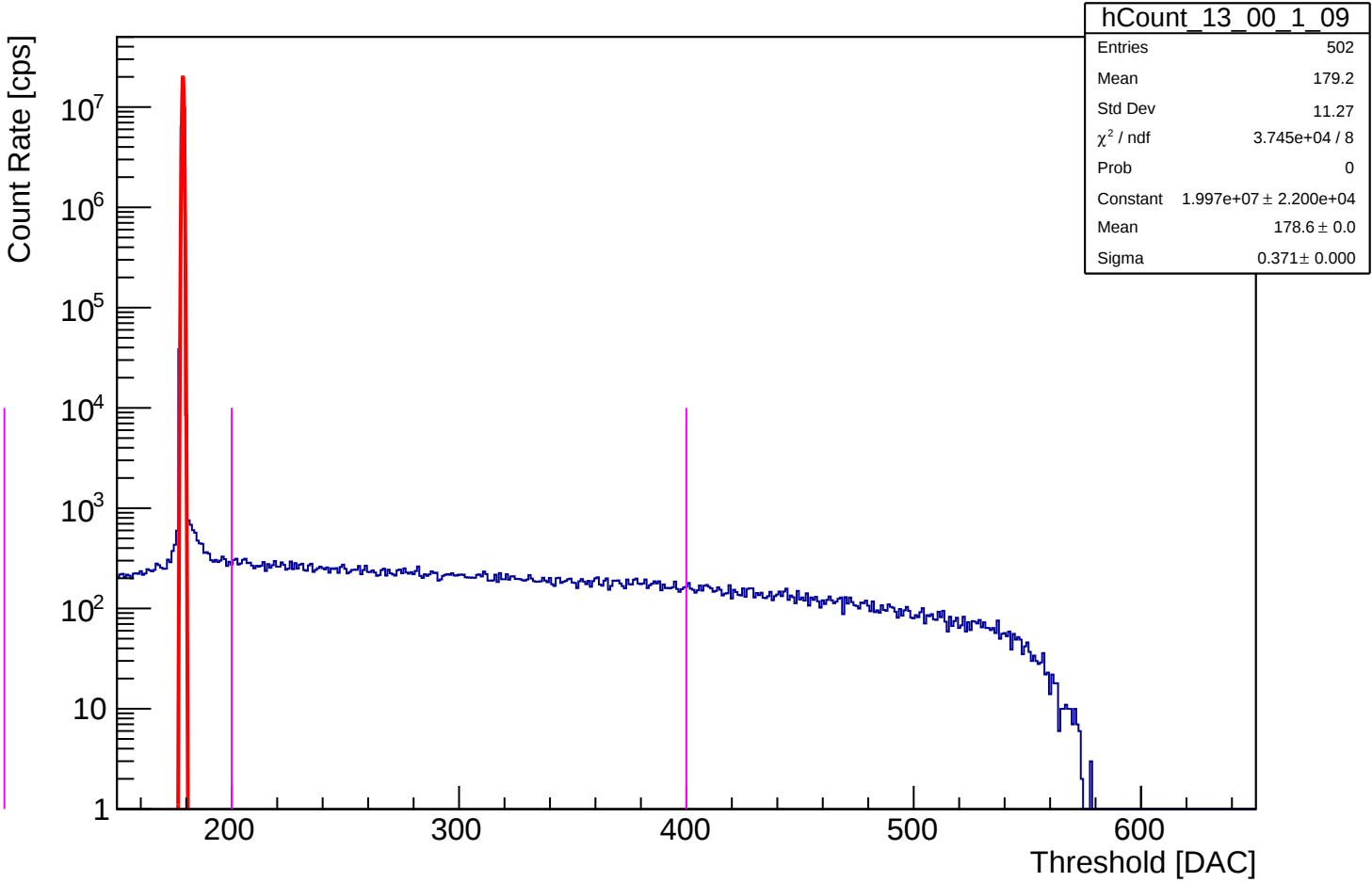
Count Rate [cps]

10⁷
10⁶
10⁵
10⁴
10³
10²
10
1

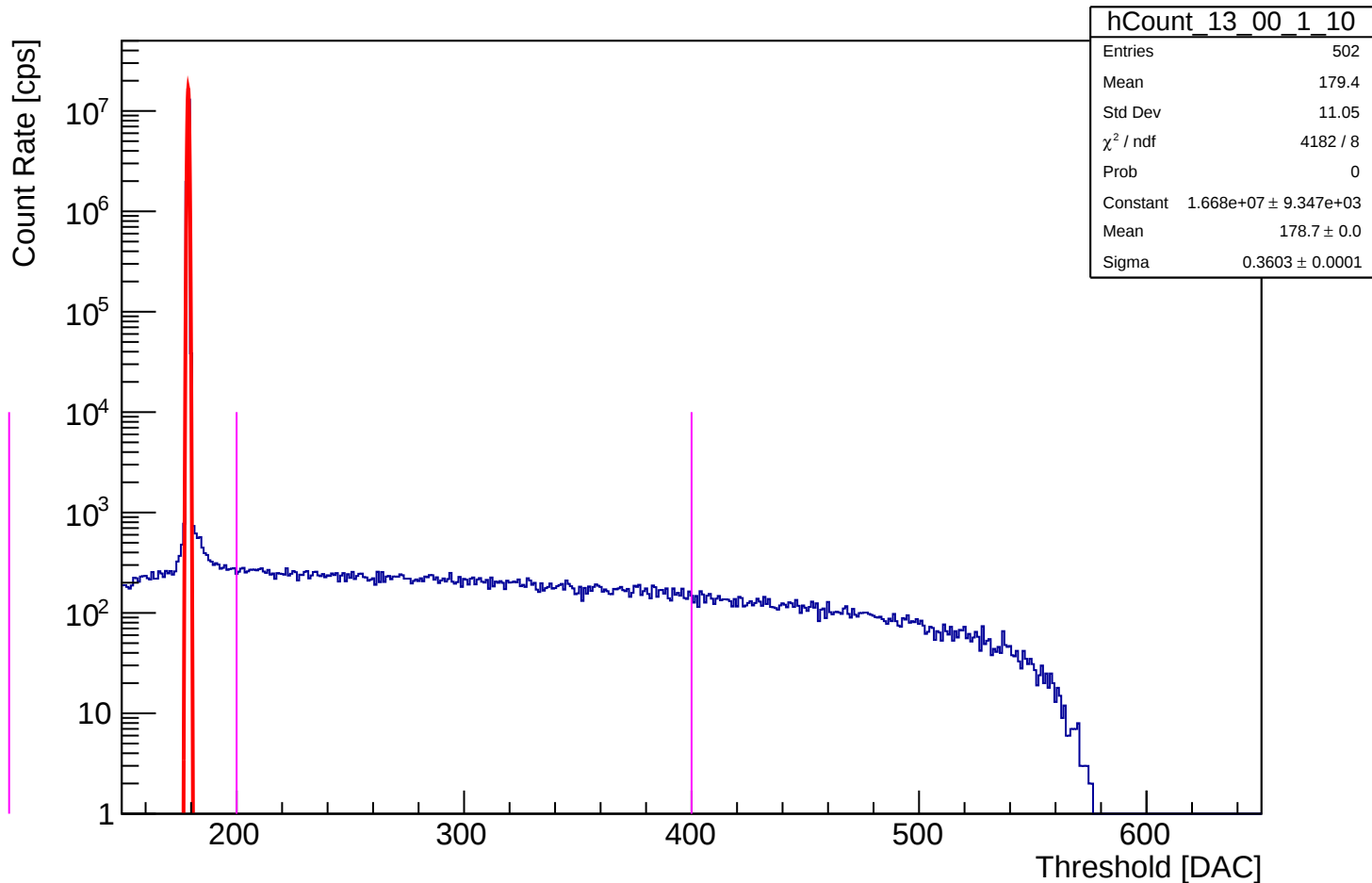


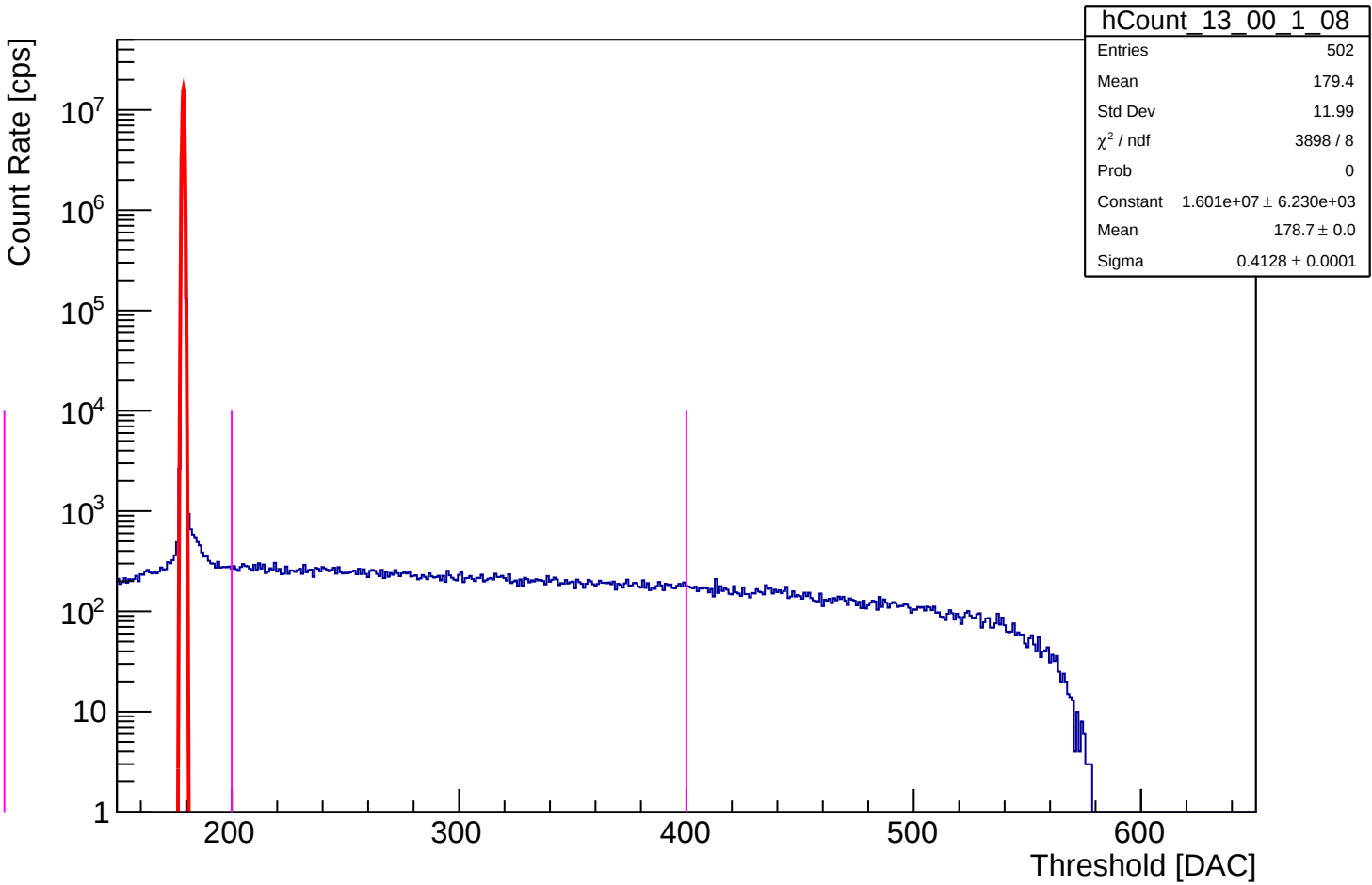
hCount_13_00_1_11	
Entries	502
Mean	180.2
Std Dev	15.51
χ^2 / ndf	7720 / 8
Prob	0
Constant	1.013e+07 $\pm$ 3.416e+03
Mean	179.2 $\pm$ 0.0
Sigma	0.4595 $\pm$ 0.0001

Threshold [DAC]

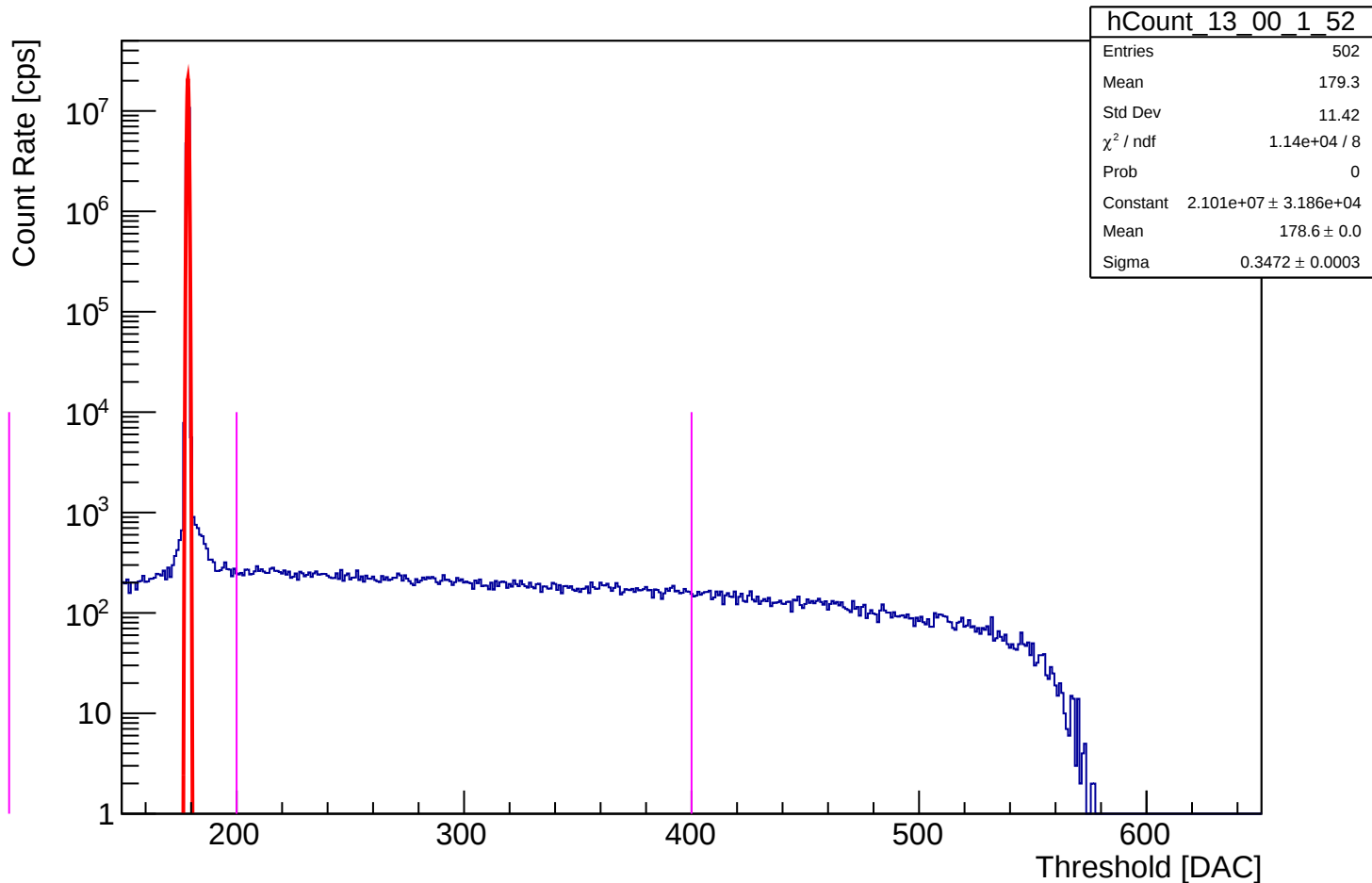


Row 1 Tile 1 Pmt 2 Pixel 43 Slot 13 Fiber 0 Asic 1 Channel 10

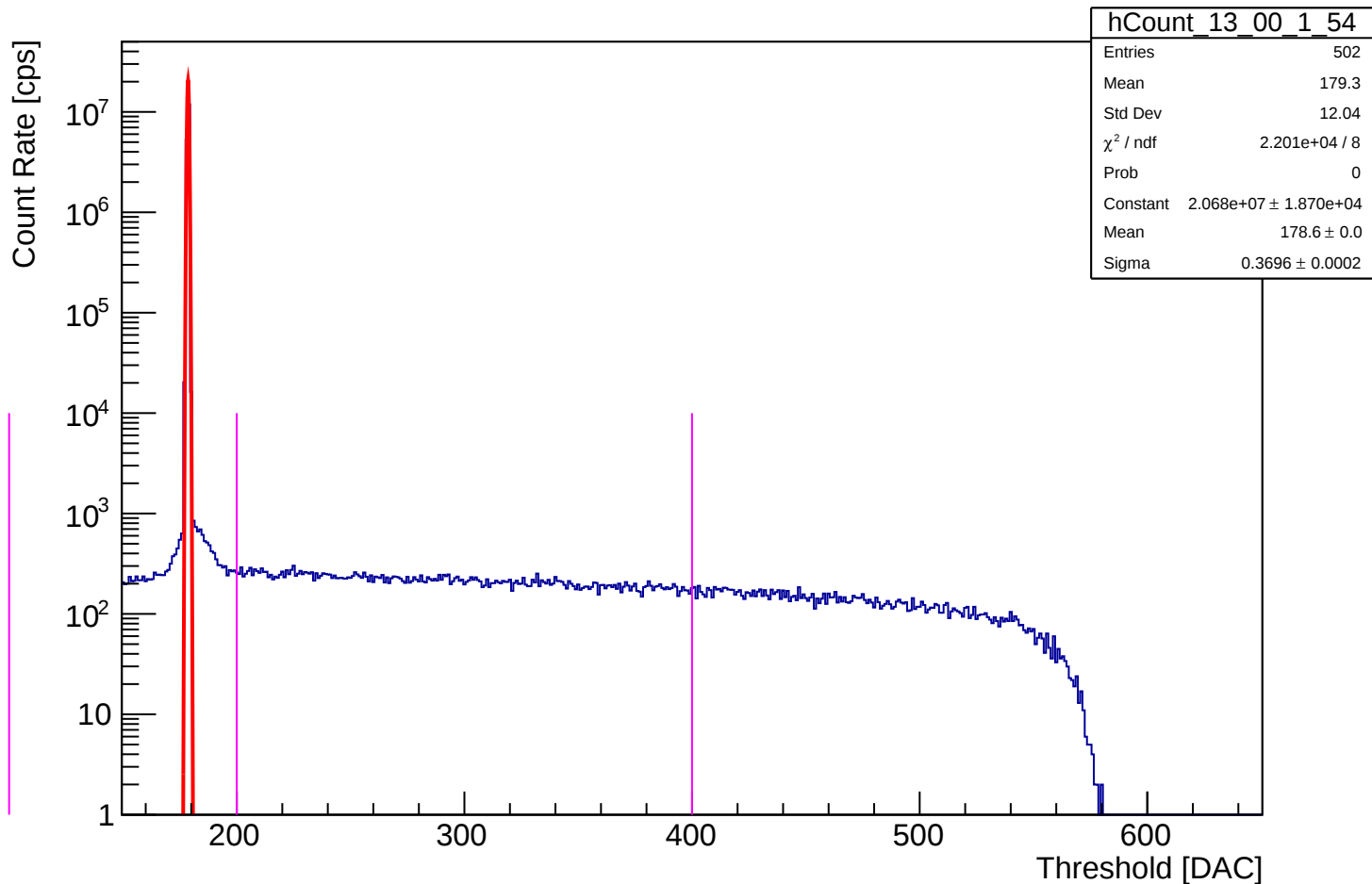




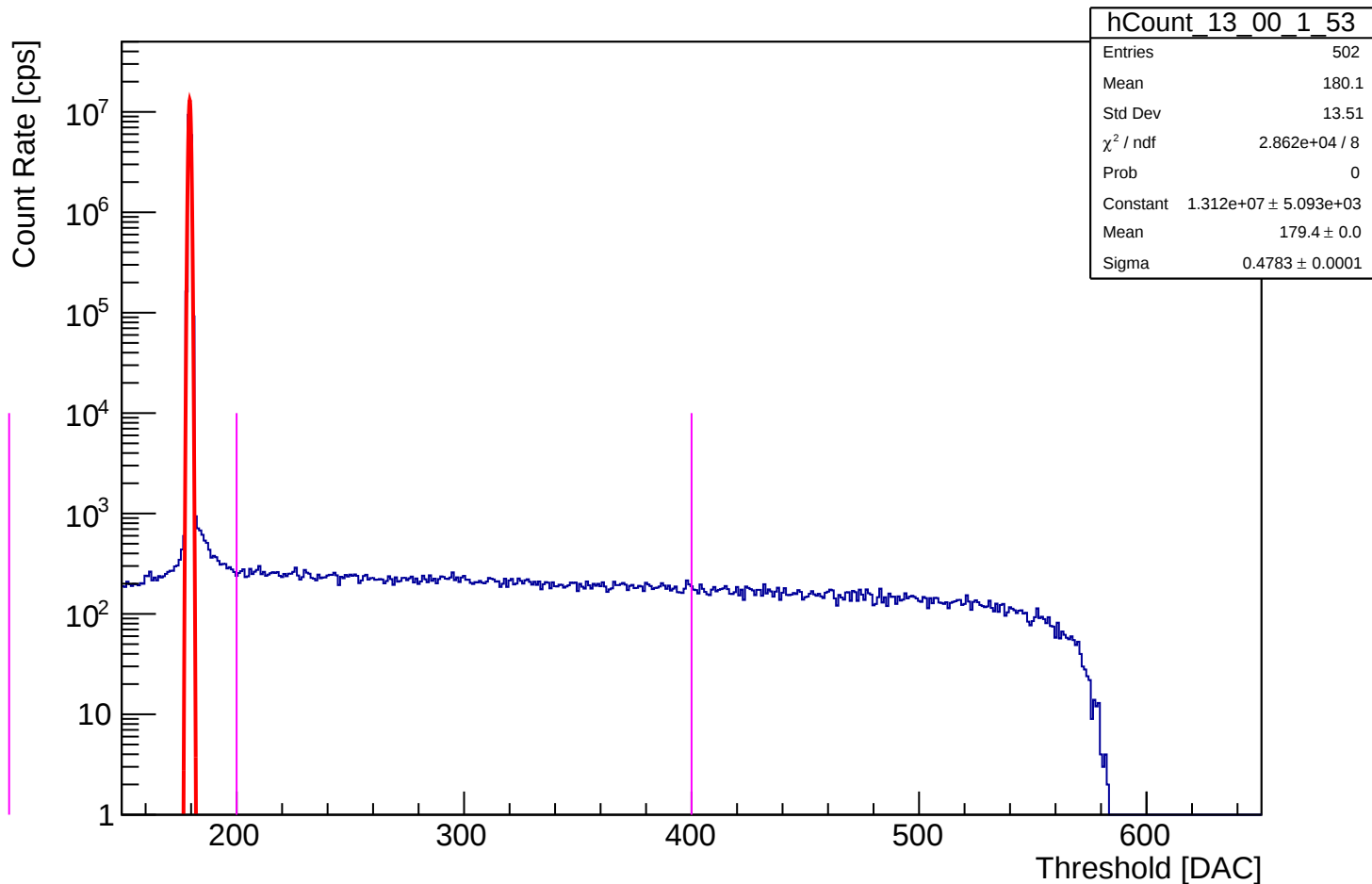
Row 1 Tile 1 Pmt 2 Pixel 45 Slot 13 Fiber 0 Asic 1 Channel 52



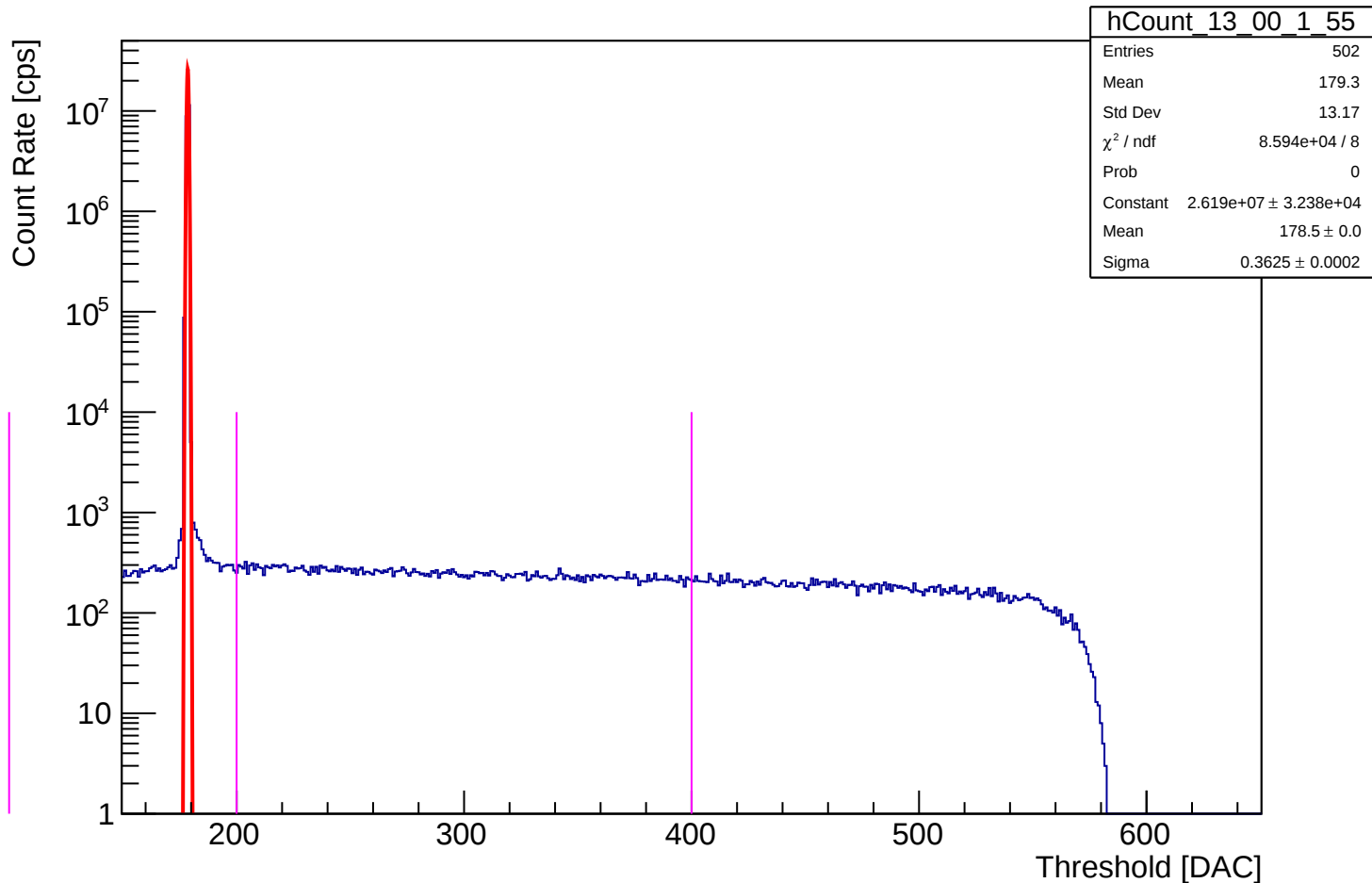
Row 1 Tile 1 Pmt 2 Pixel 46 Slot 13 Fiber 0 Asic 1 Channel 54

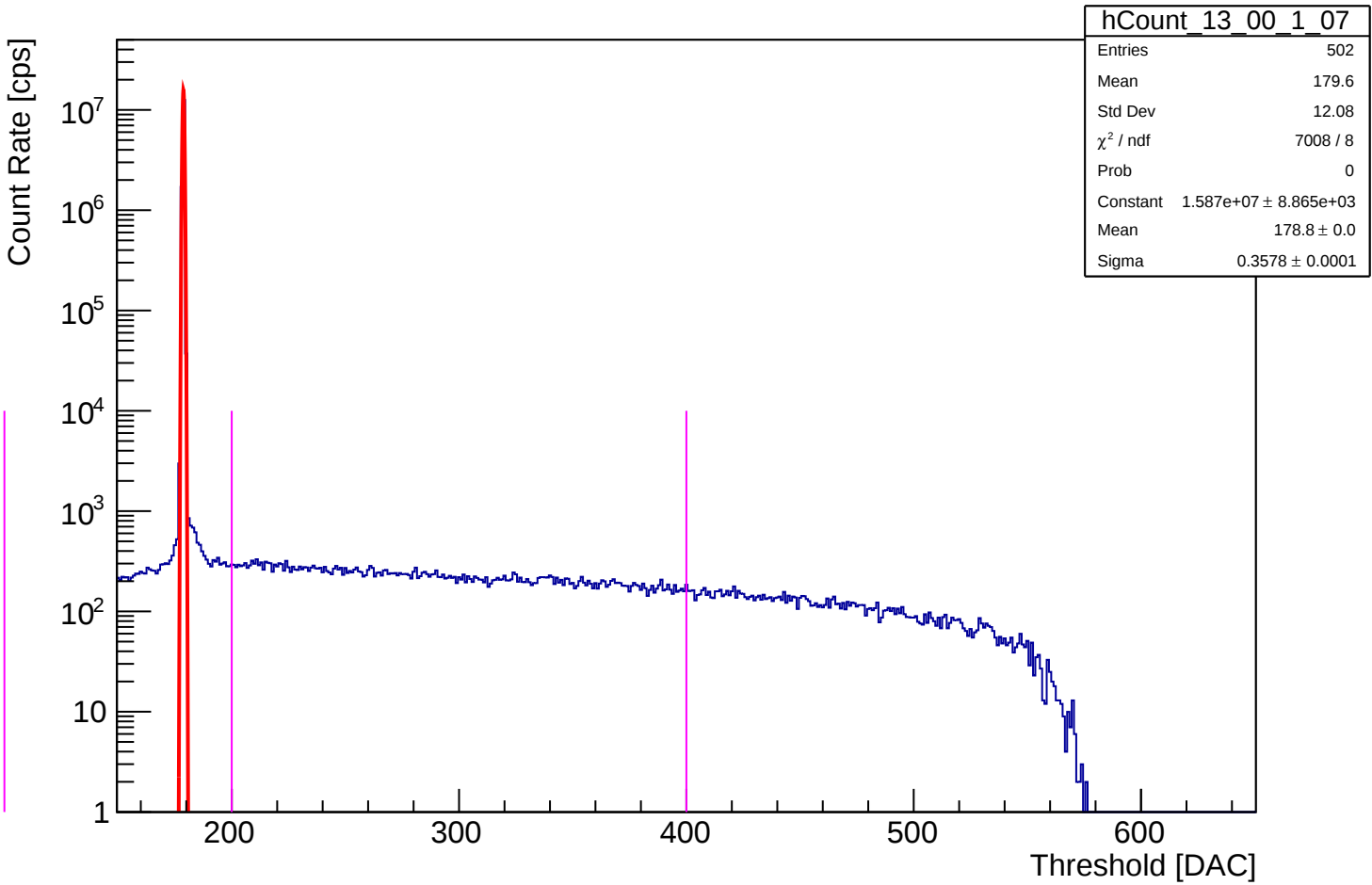


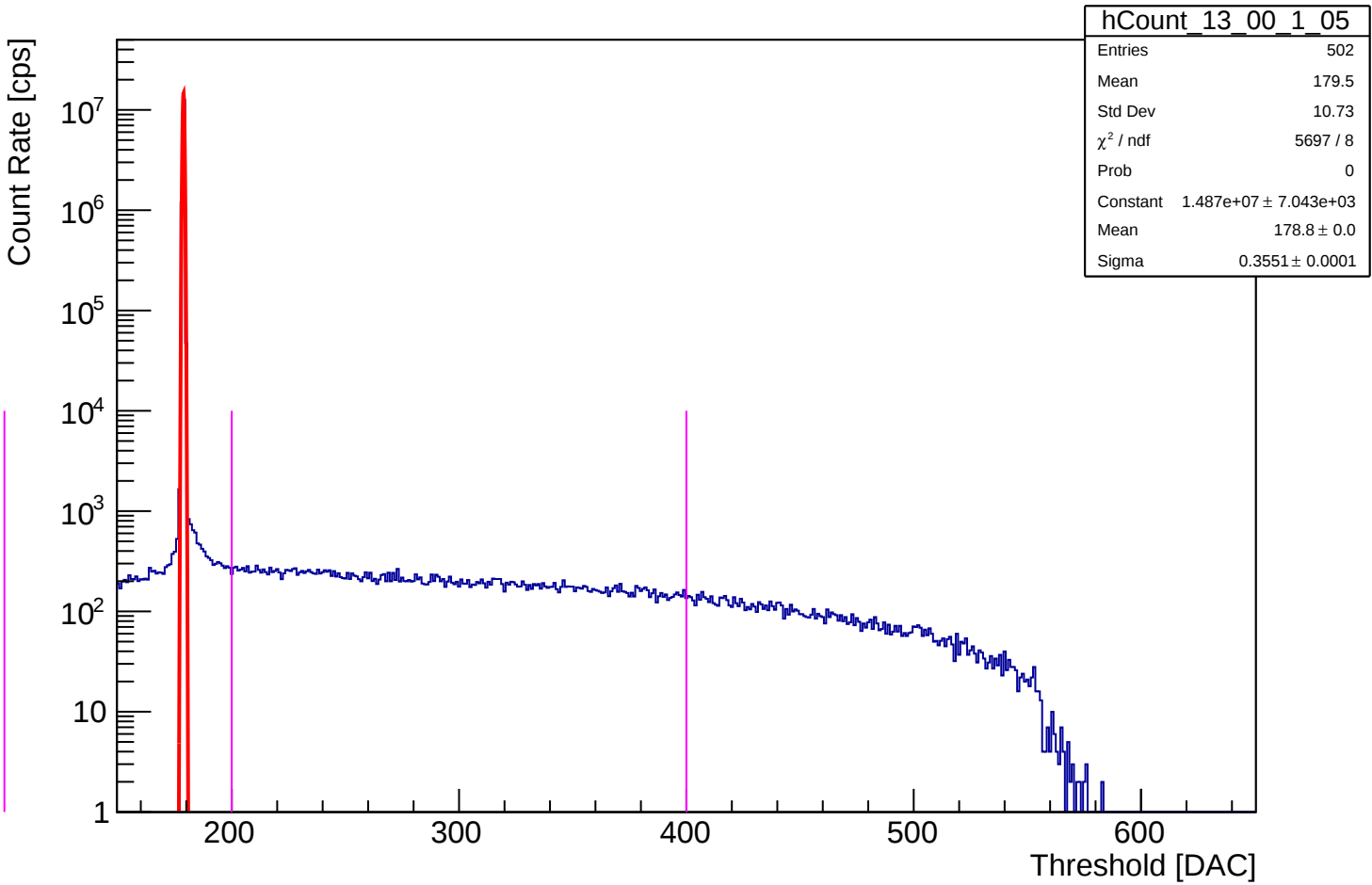
Row 1 Tile 1 Pmt 2 Pixel 47 Slot 13 Fiber 0 Asic 1 Channel 53

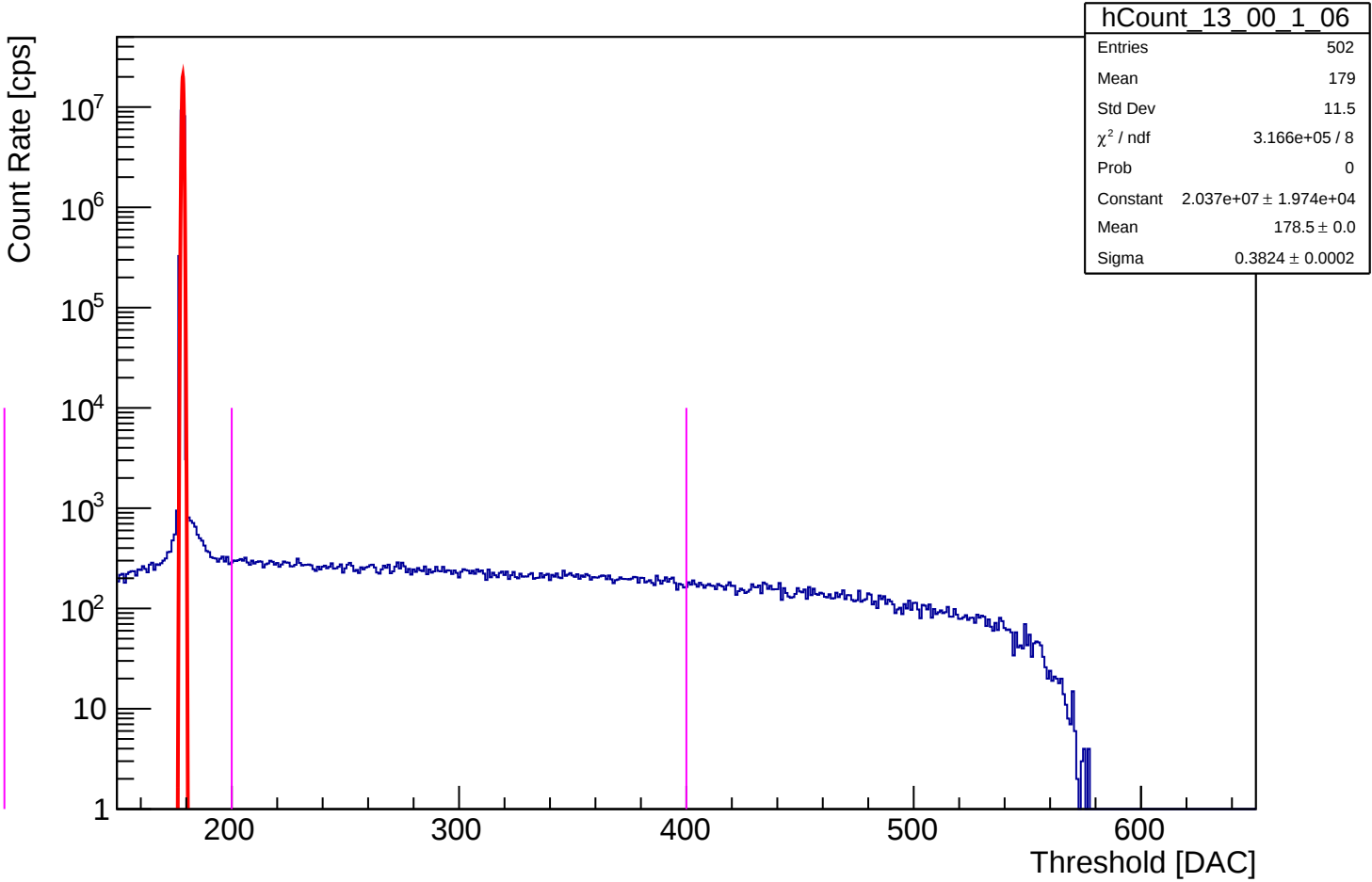


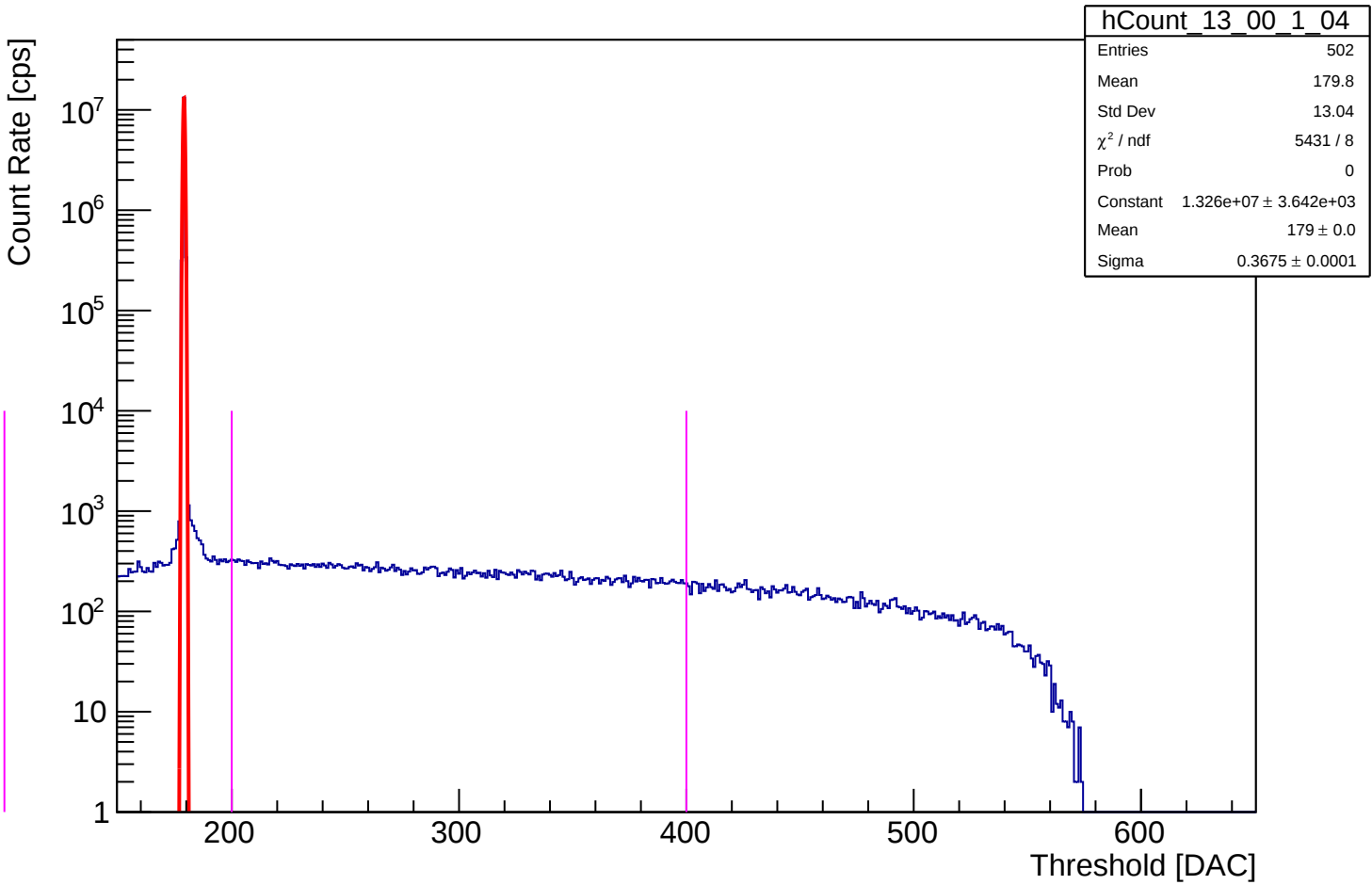
Row 1 Tile 1 Pmt 2 Pixel 48 Slot 13 Fiber 0 Asic 1 Channel 55



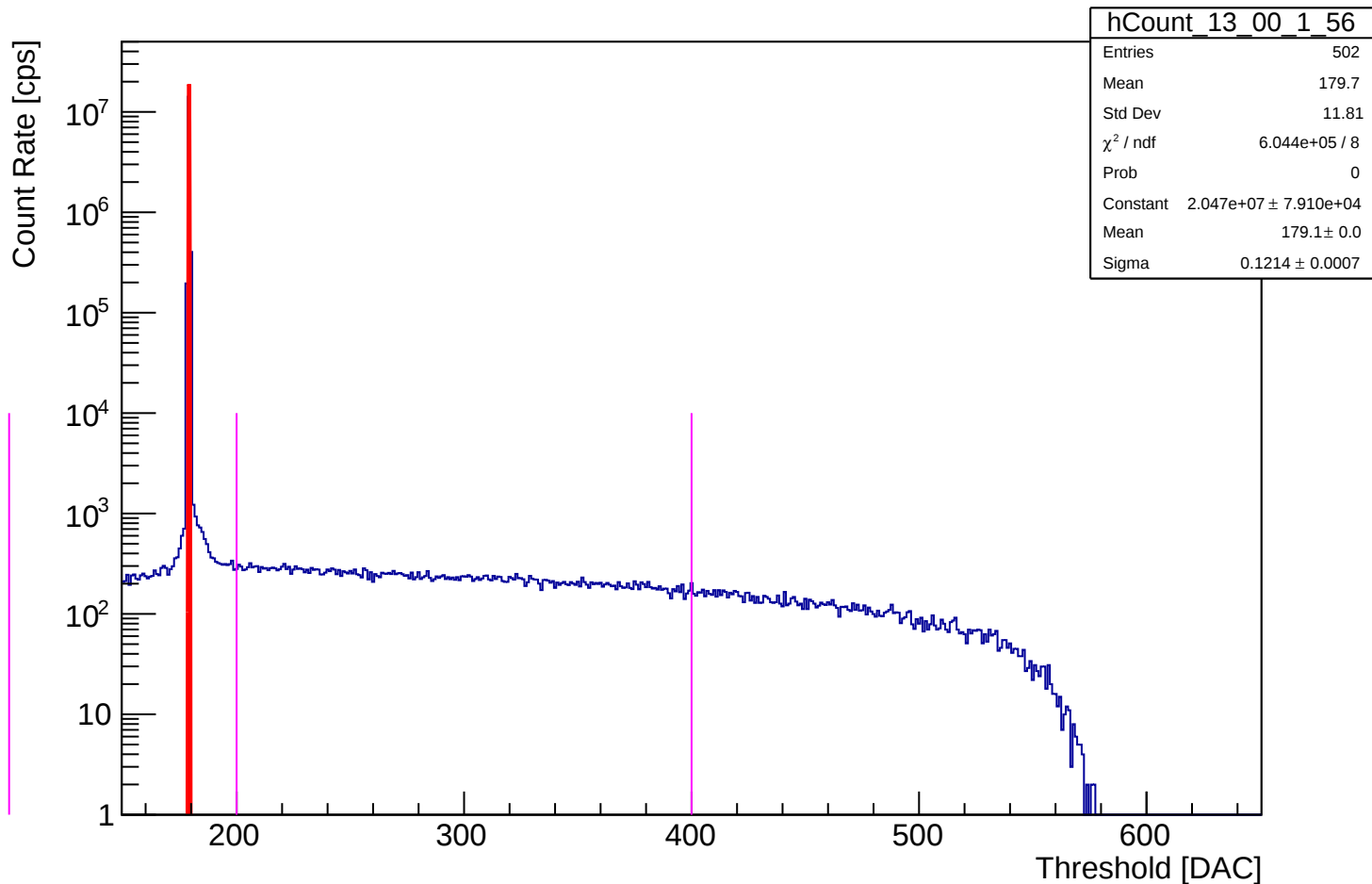




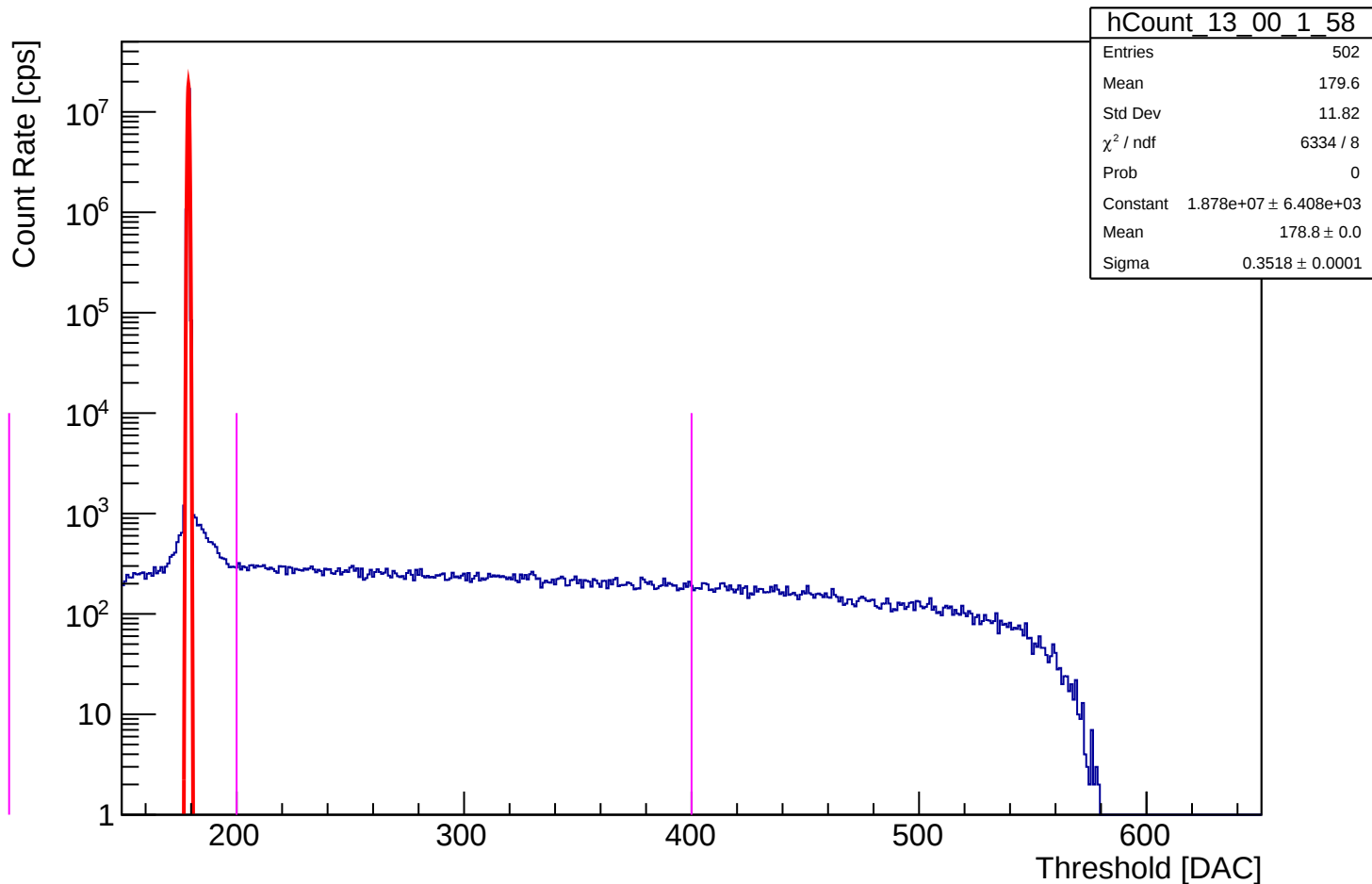




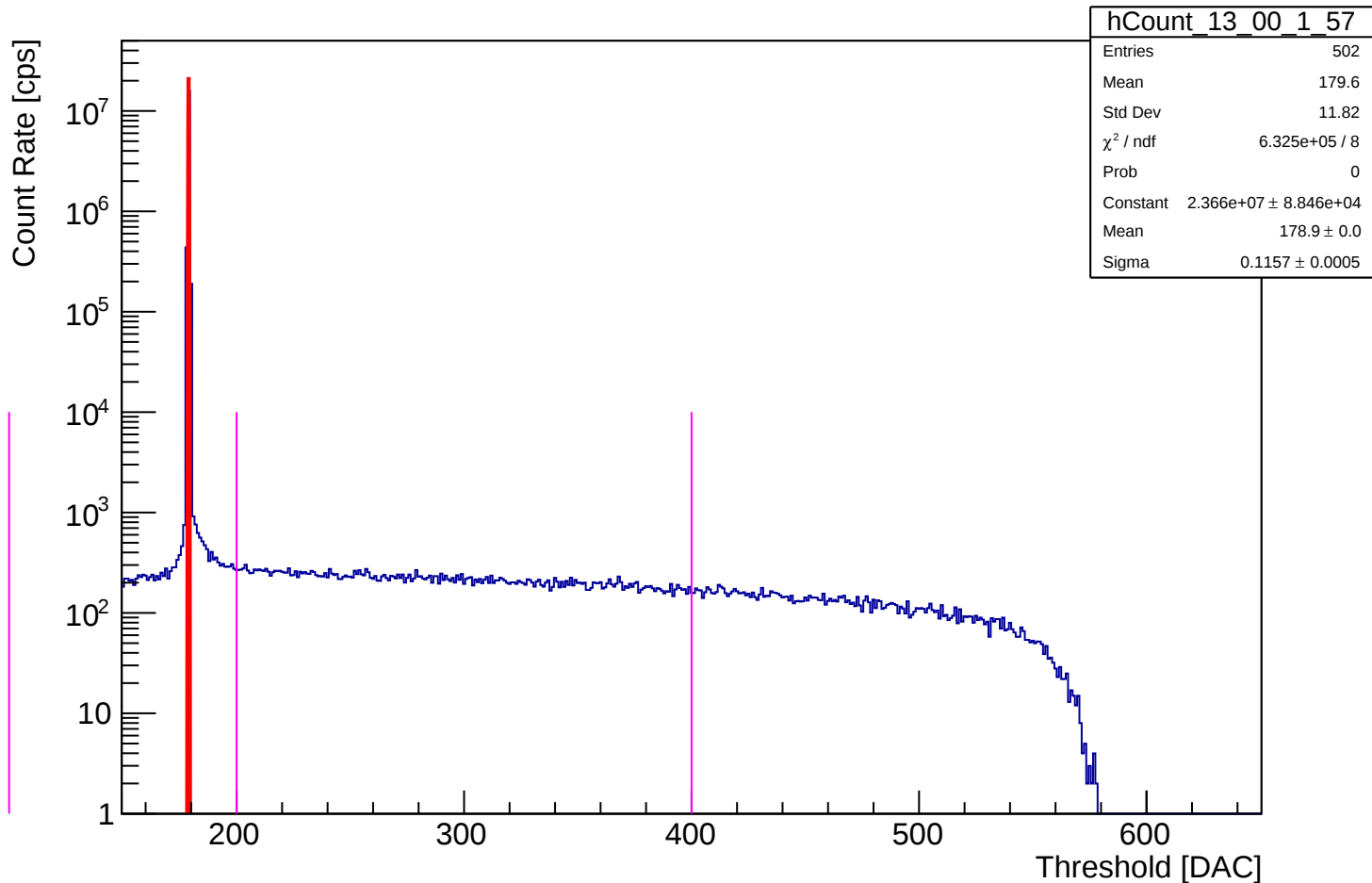
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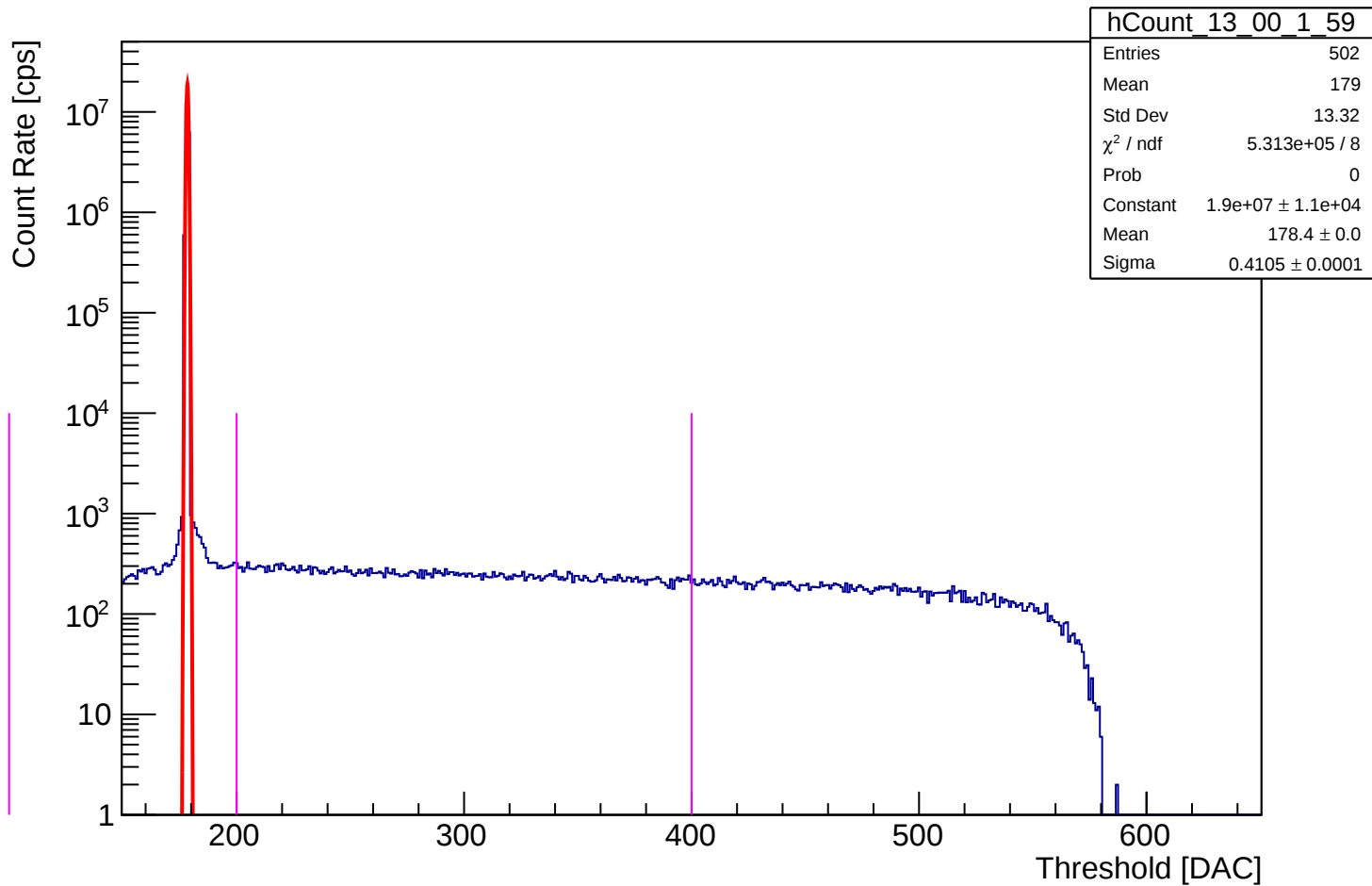
Row 1 Tile 1 Pmt 2 Pixel 54 Slot 13 Fiber 0 Asic 1 Channel 58

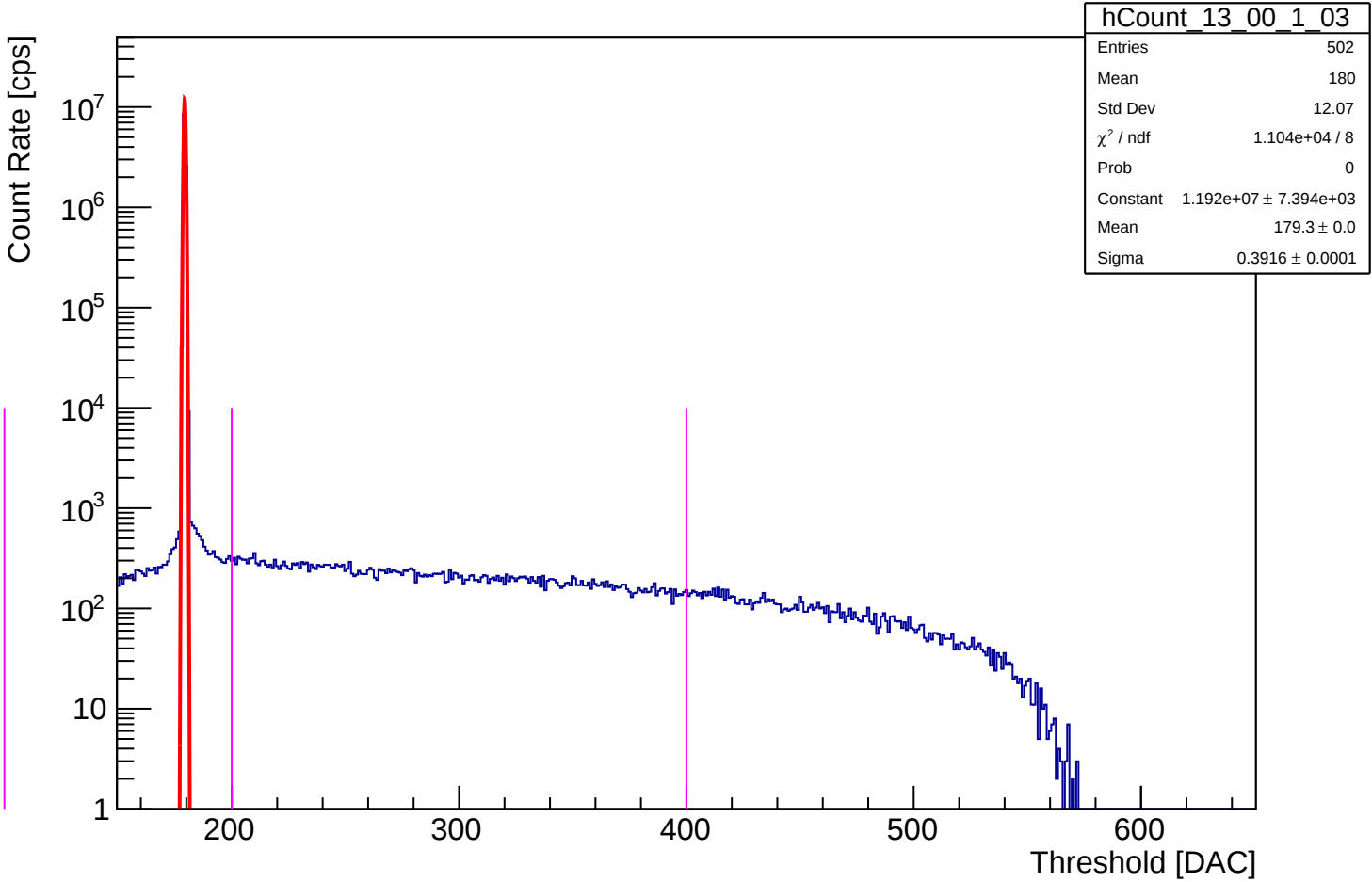


Row 1 Tile 1 Pmt 2 Pixel 55 Slot 13 Fiber 0 Asic 1 Channel 57

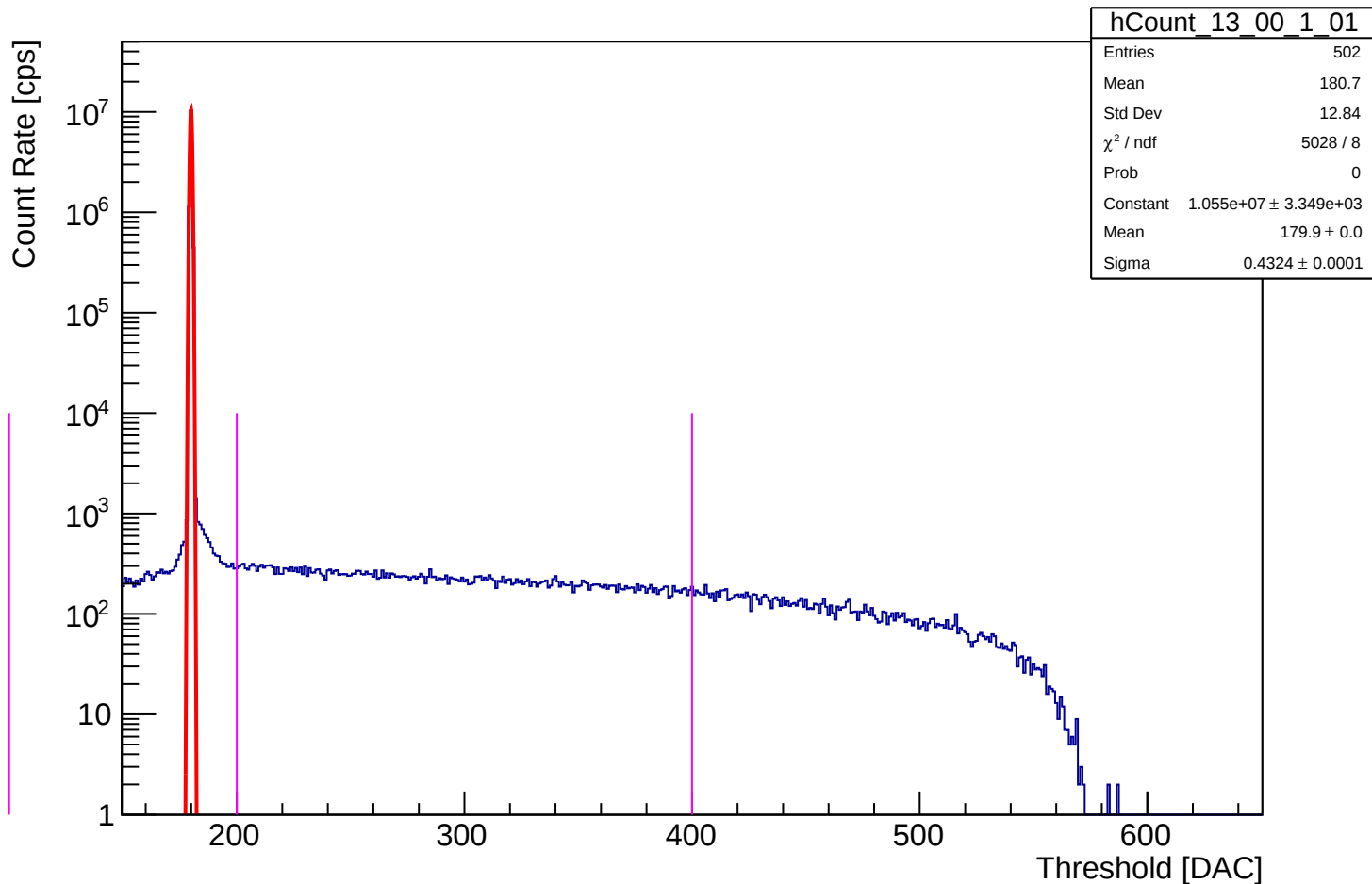


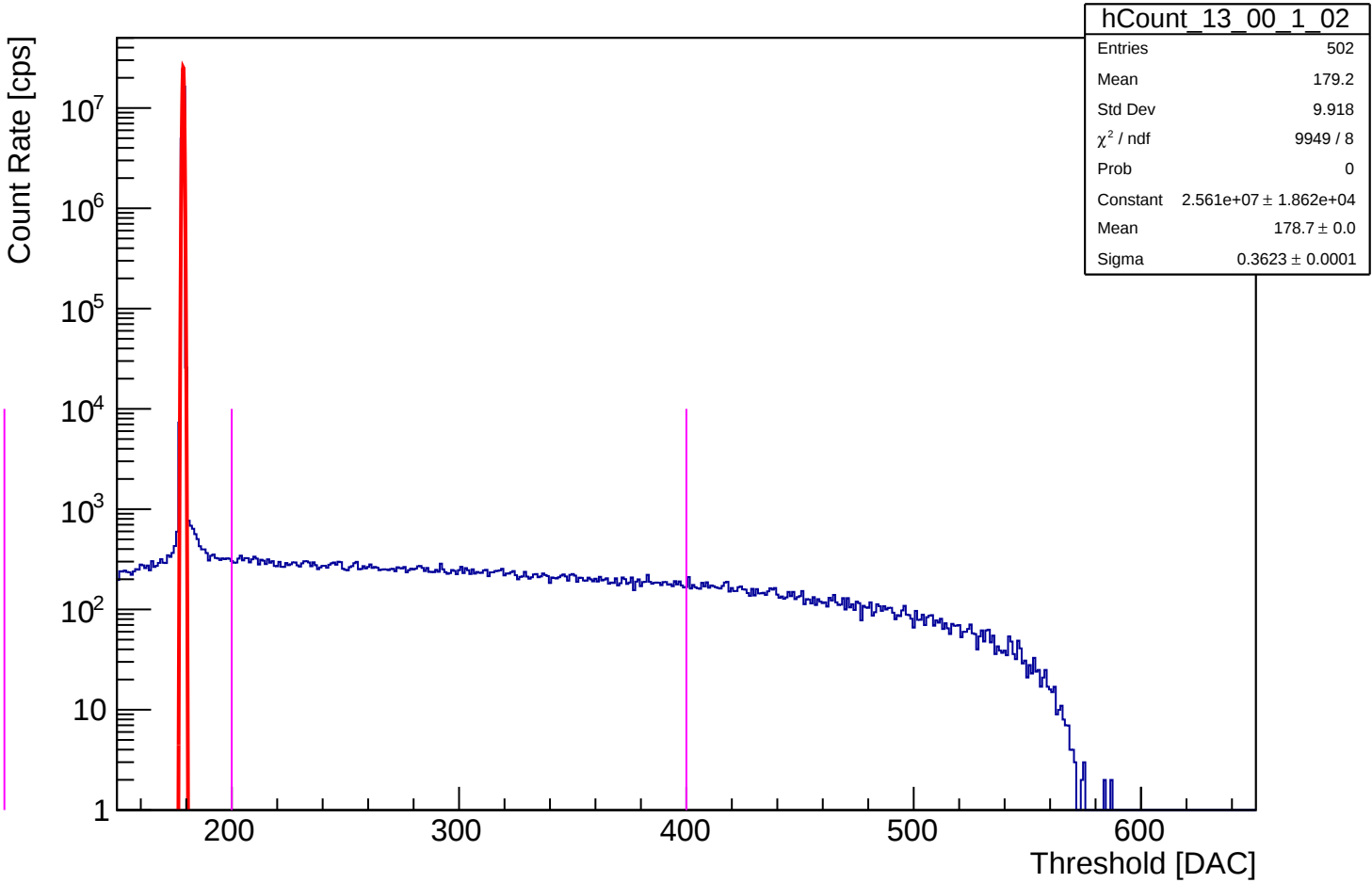
Row 1 Tile 1 Pmt 2 Pixel 56 Slot 13 Fiber 0 Asic 1 Channel 59

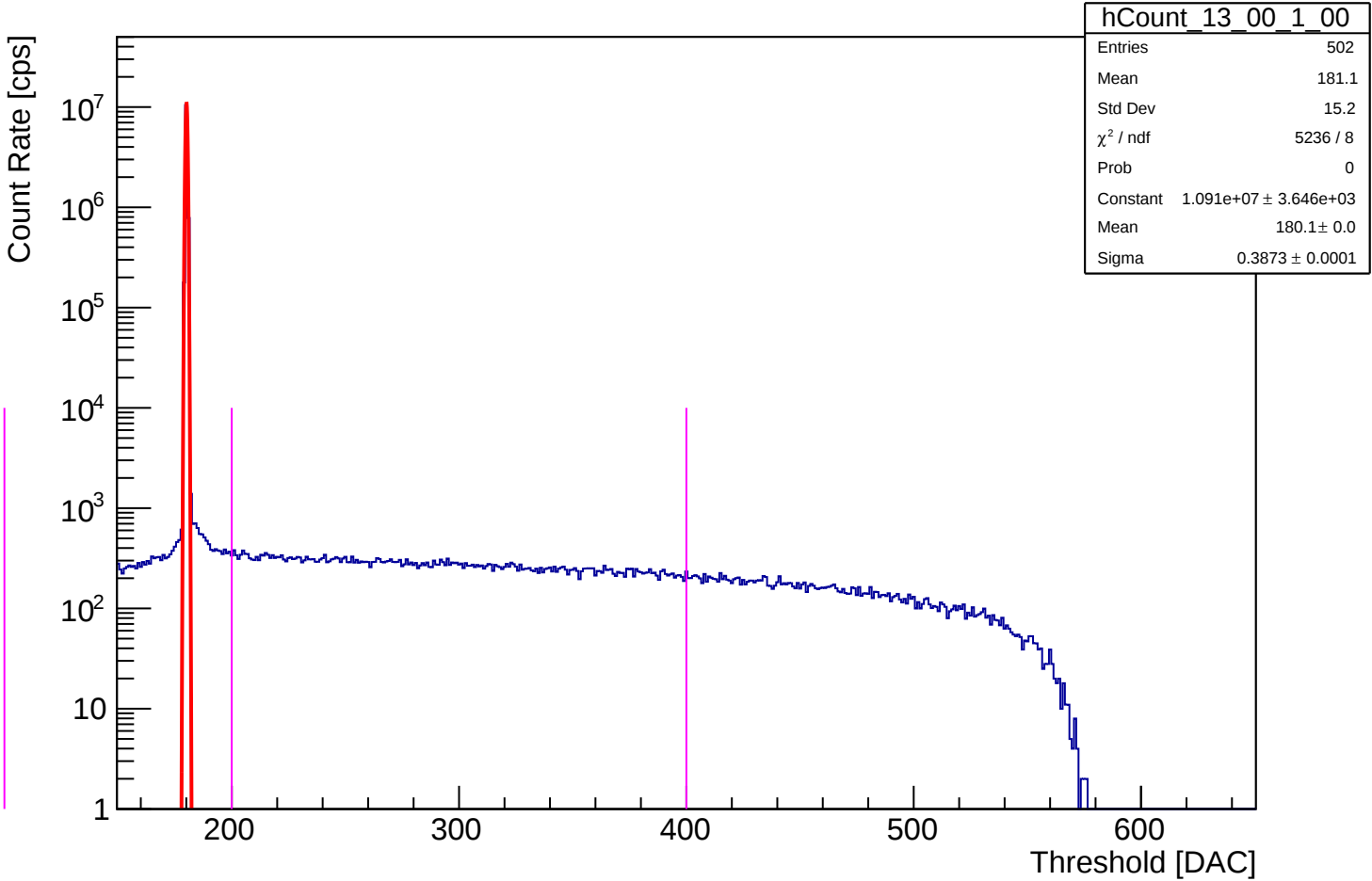




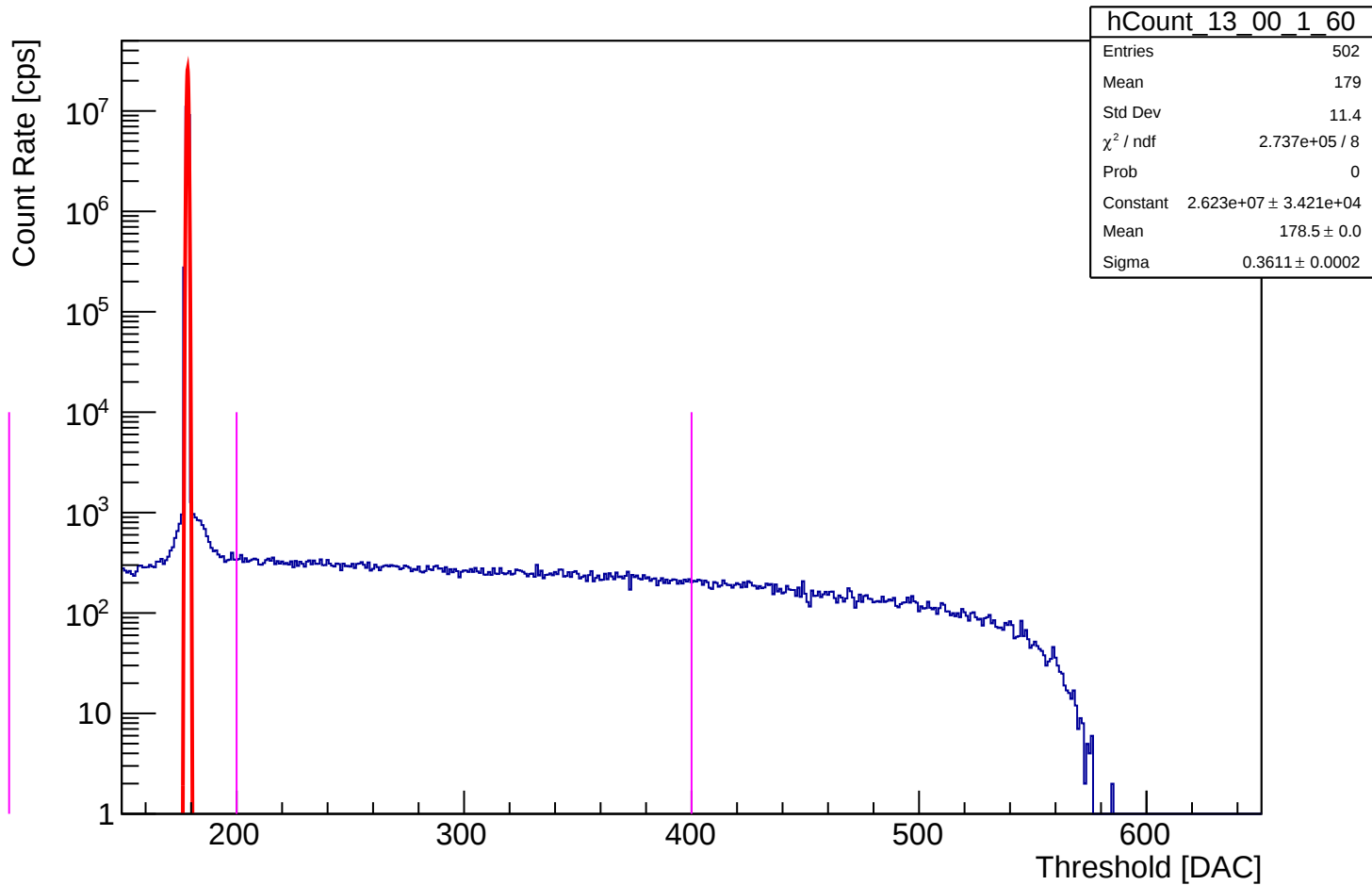
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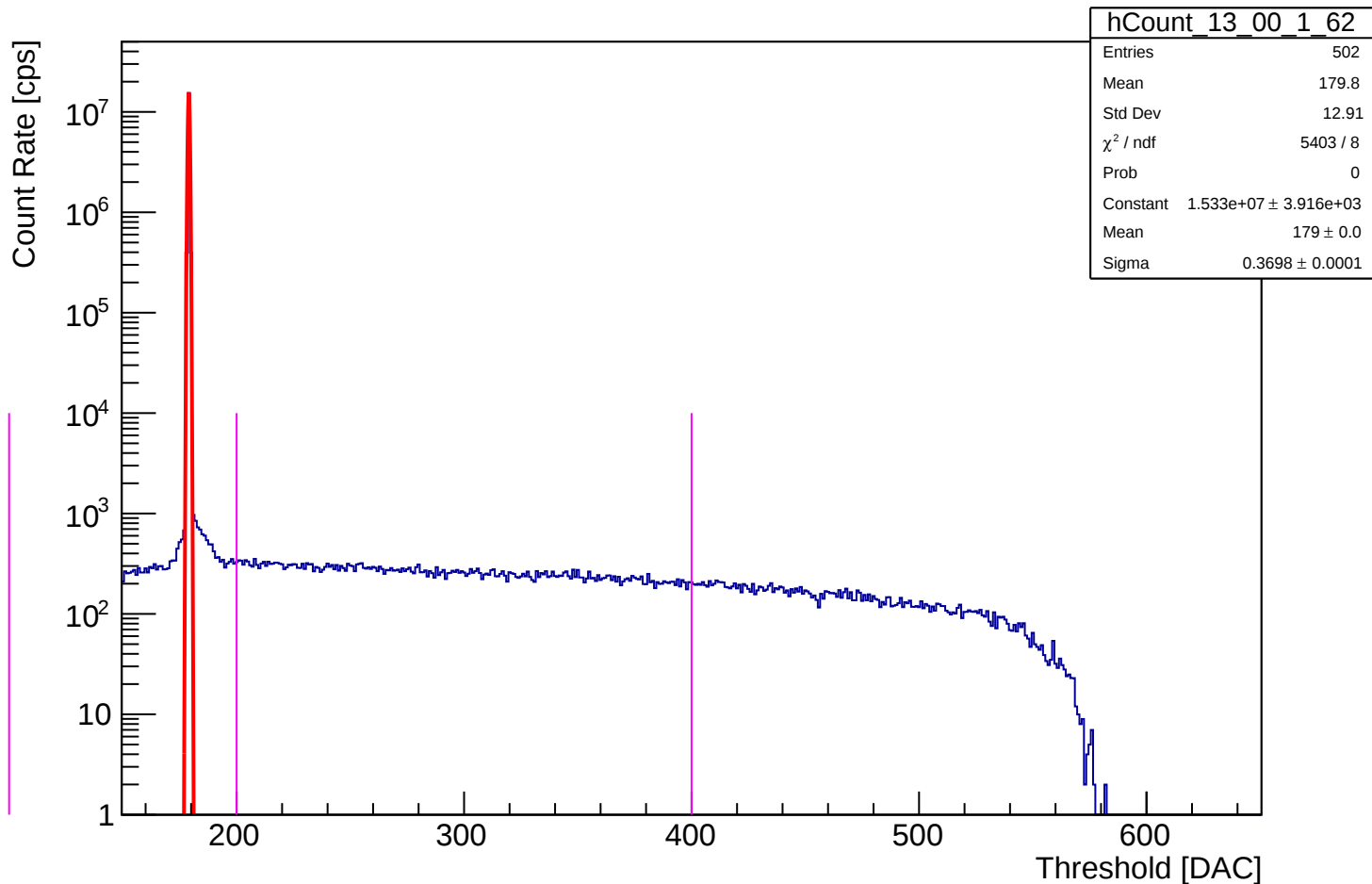


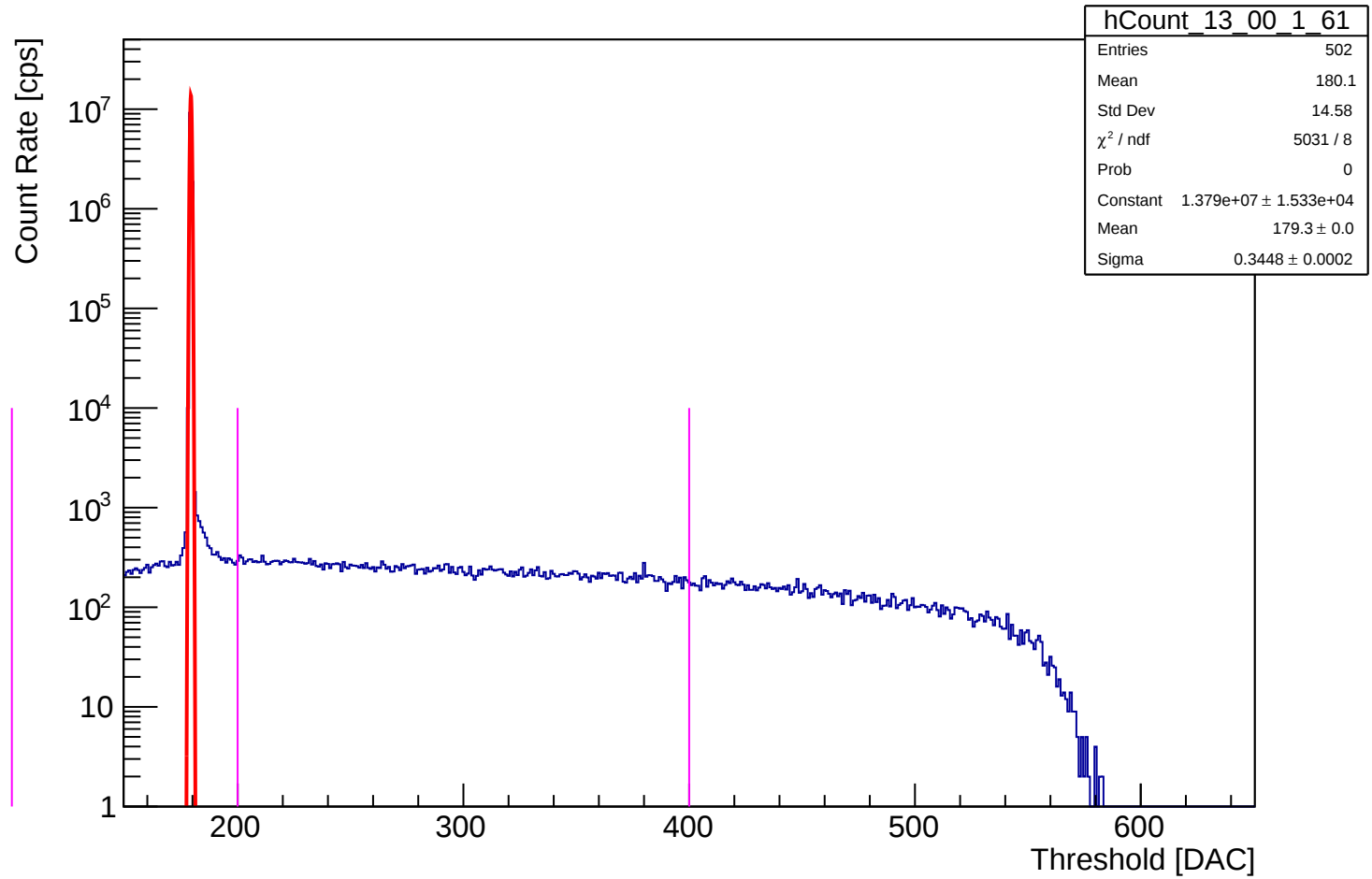


Row 1 Tile 1 Pmt 2 Pixel 61 Slot 13 Fiber 0 Asic 1 Channel 60

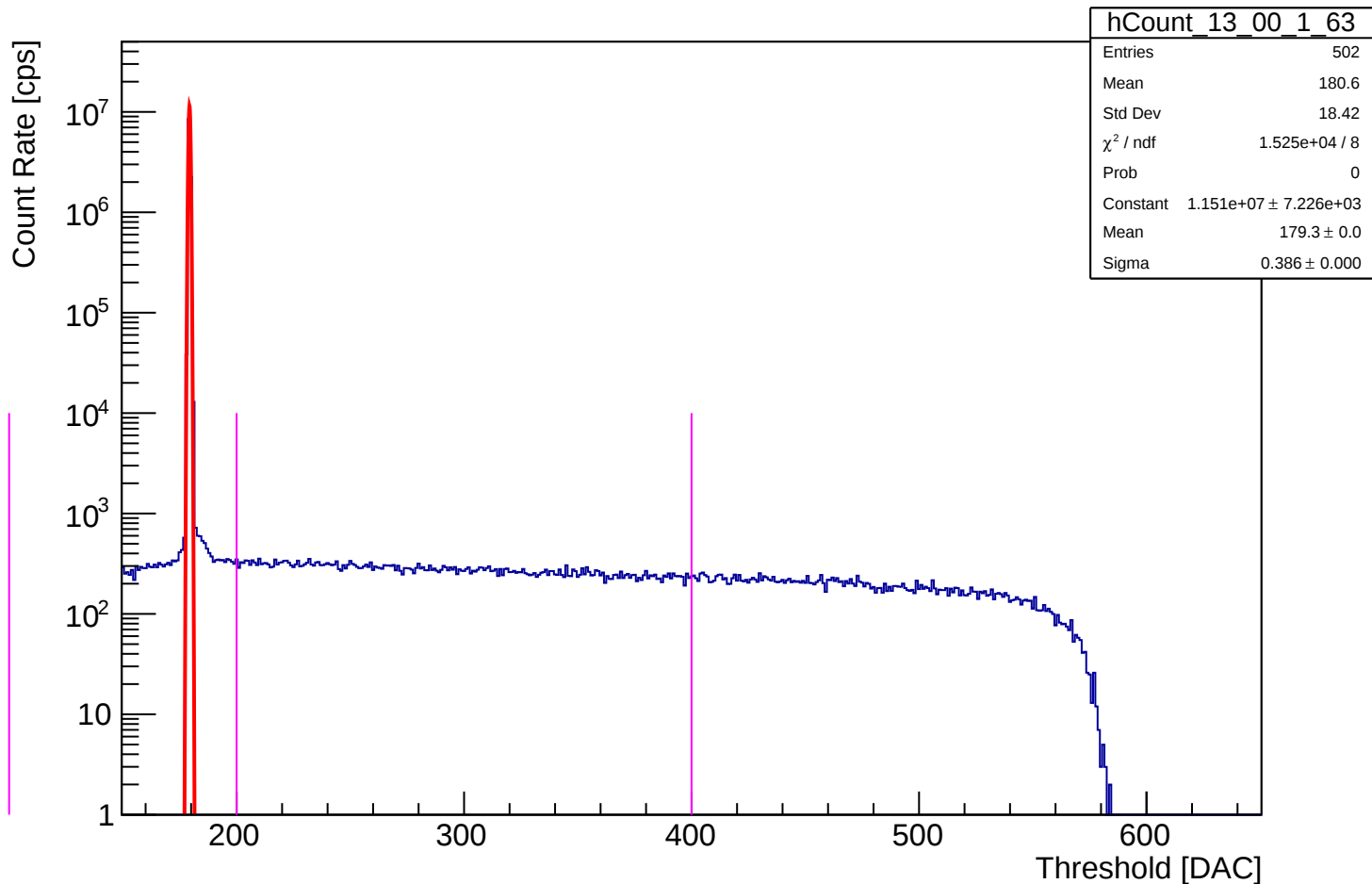


Row 1 Tile 1 Pmt 2 Pixel 62 Slot 13 Fiber 0 Asic 1 Channel 62

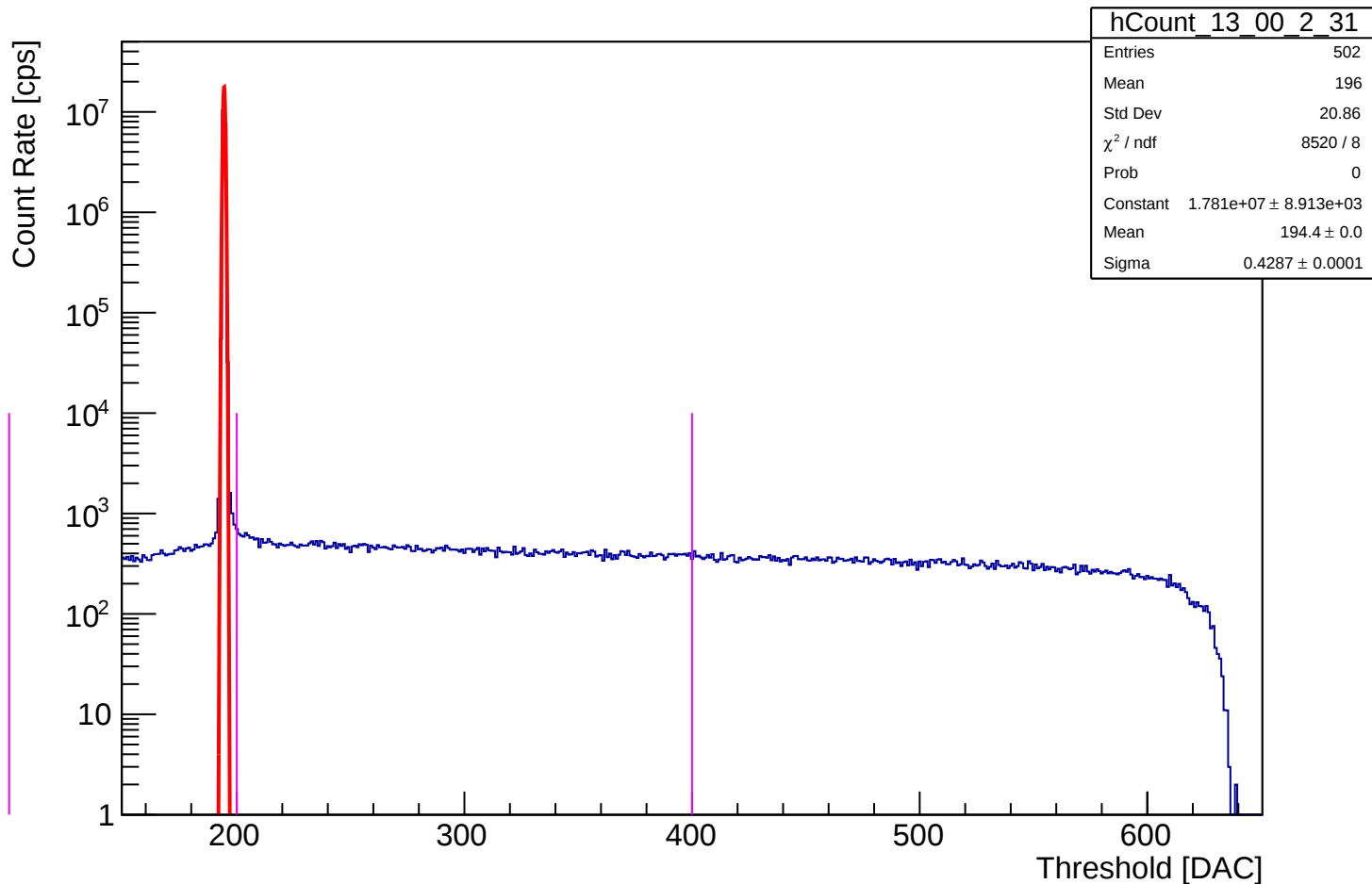




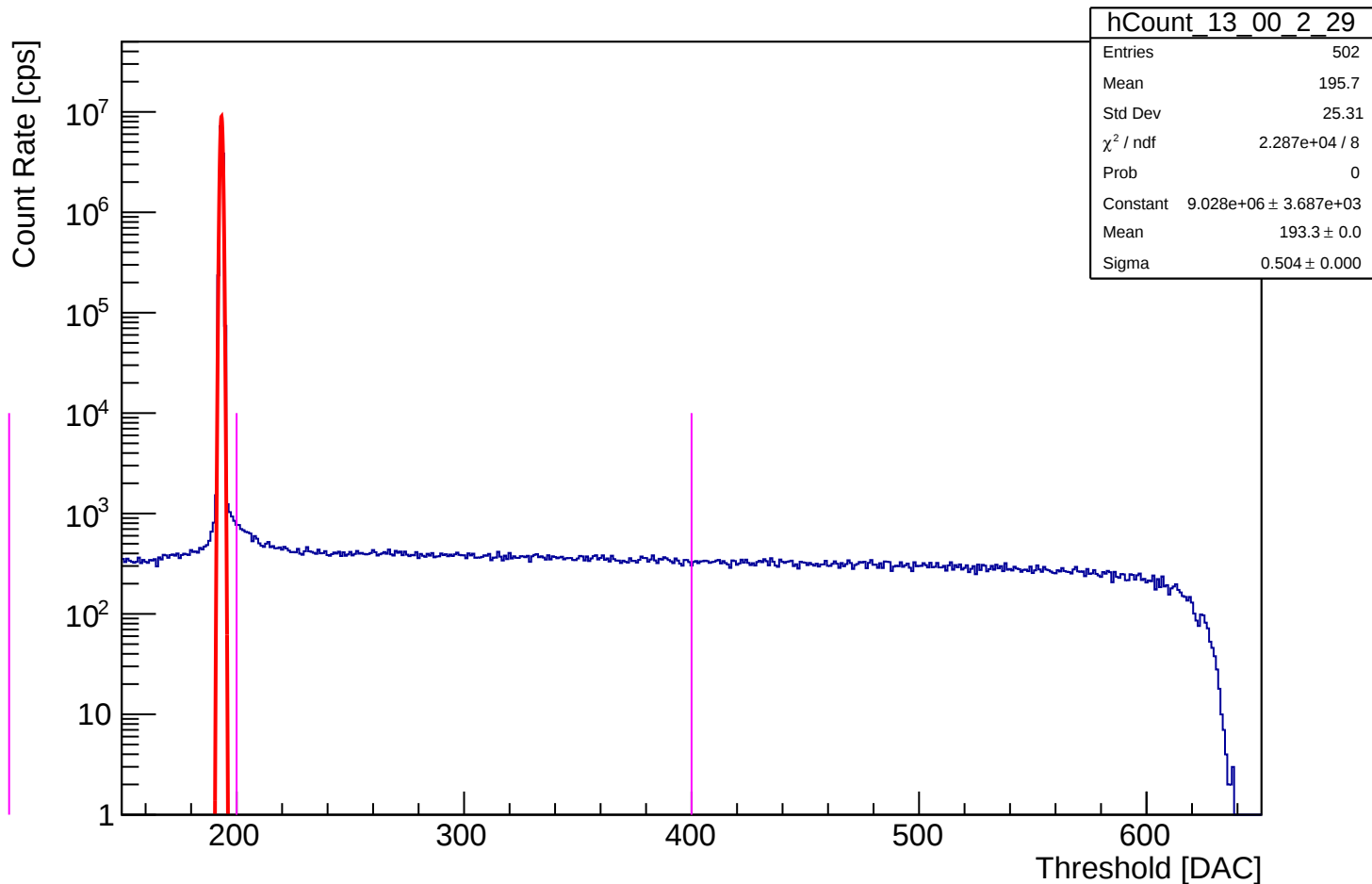
Row 1 Tile 1 Pmt 2 Pixel 64 Slot 13 Fiber 0 Asic 1 Channel 63



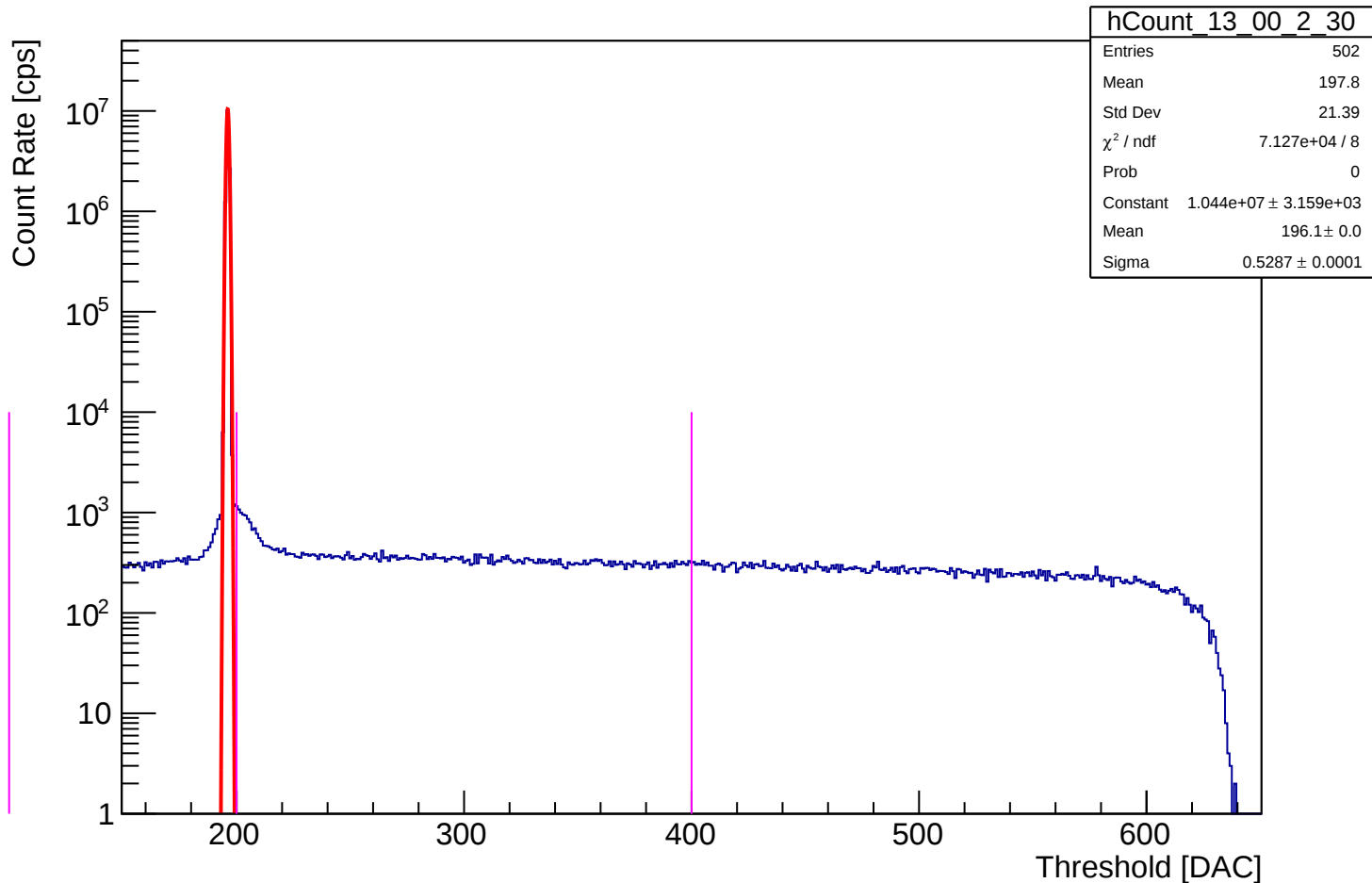
Row 1 Tile 1 Pmt 3 Pixel 1 Slot 13 Fiber 0 Asic 2 Channel 31



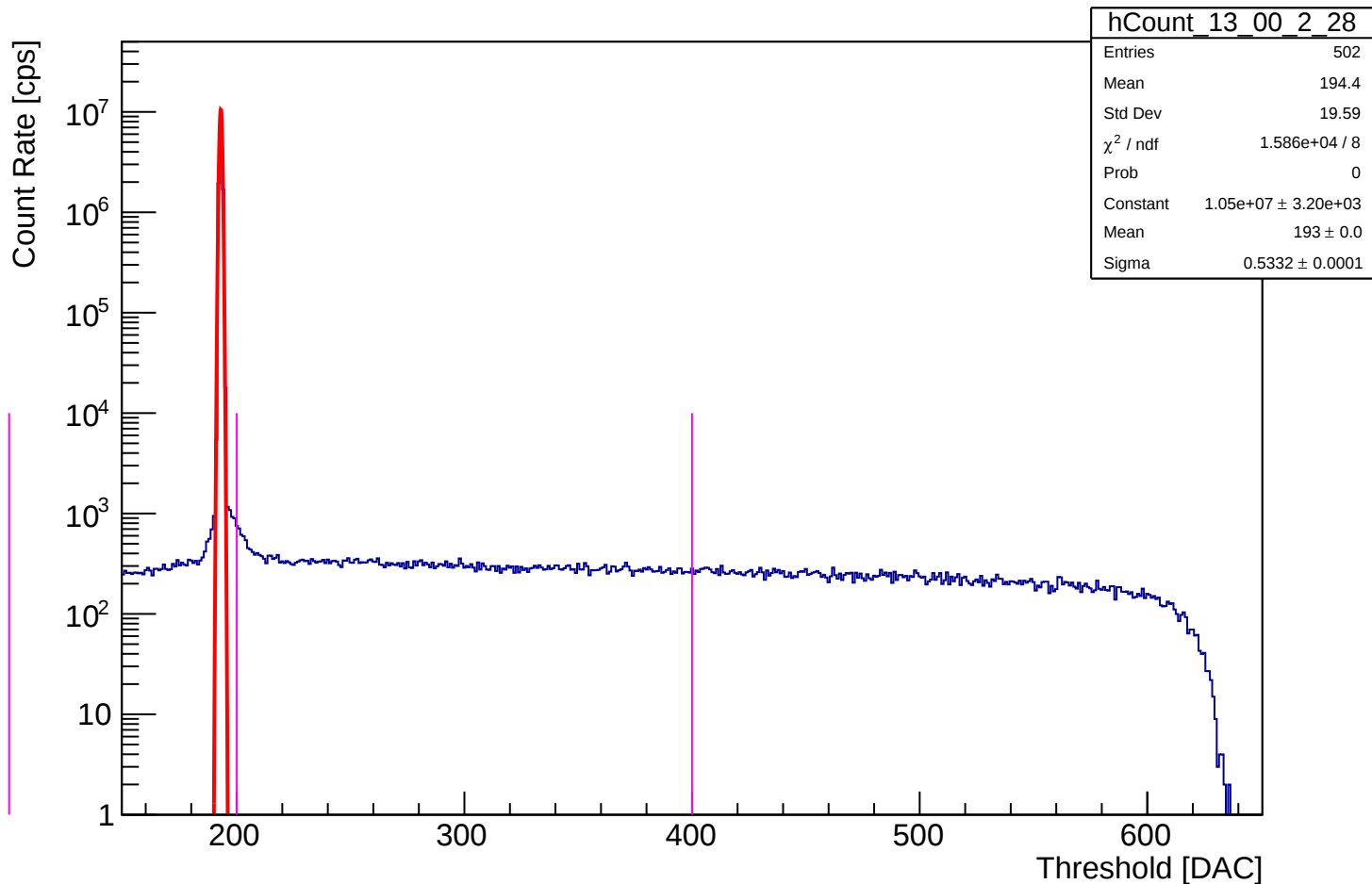
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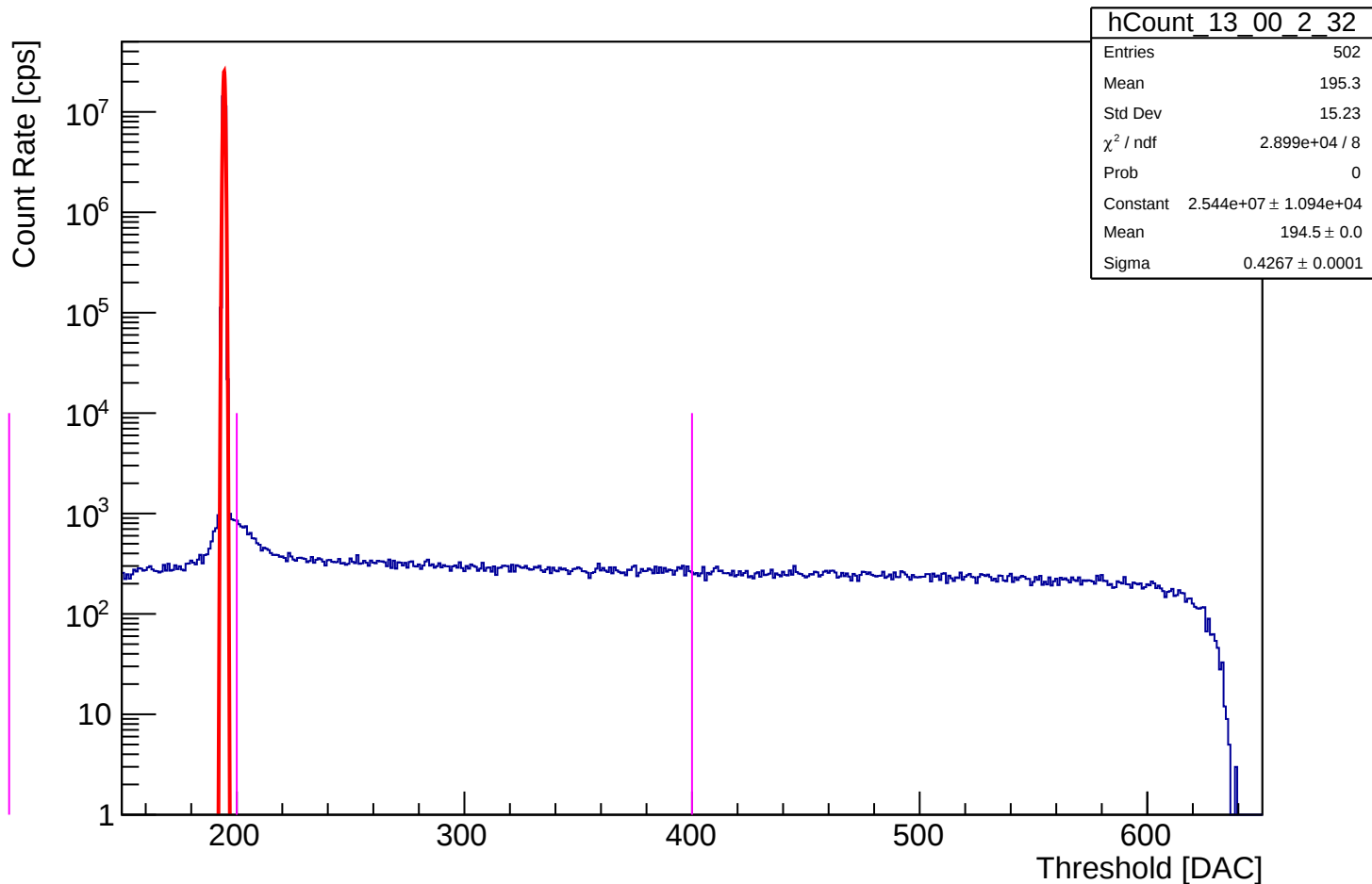
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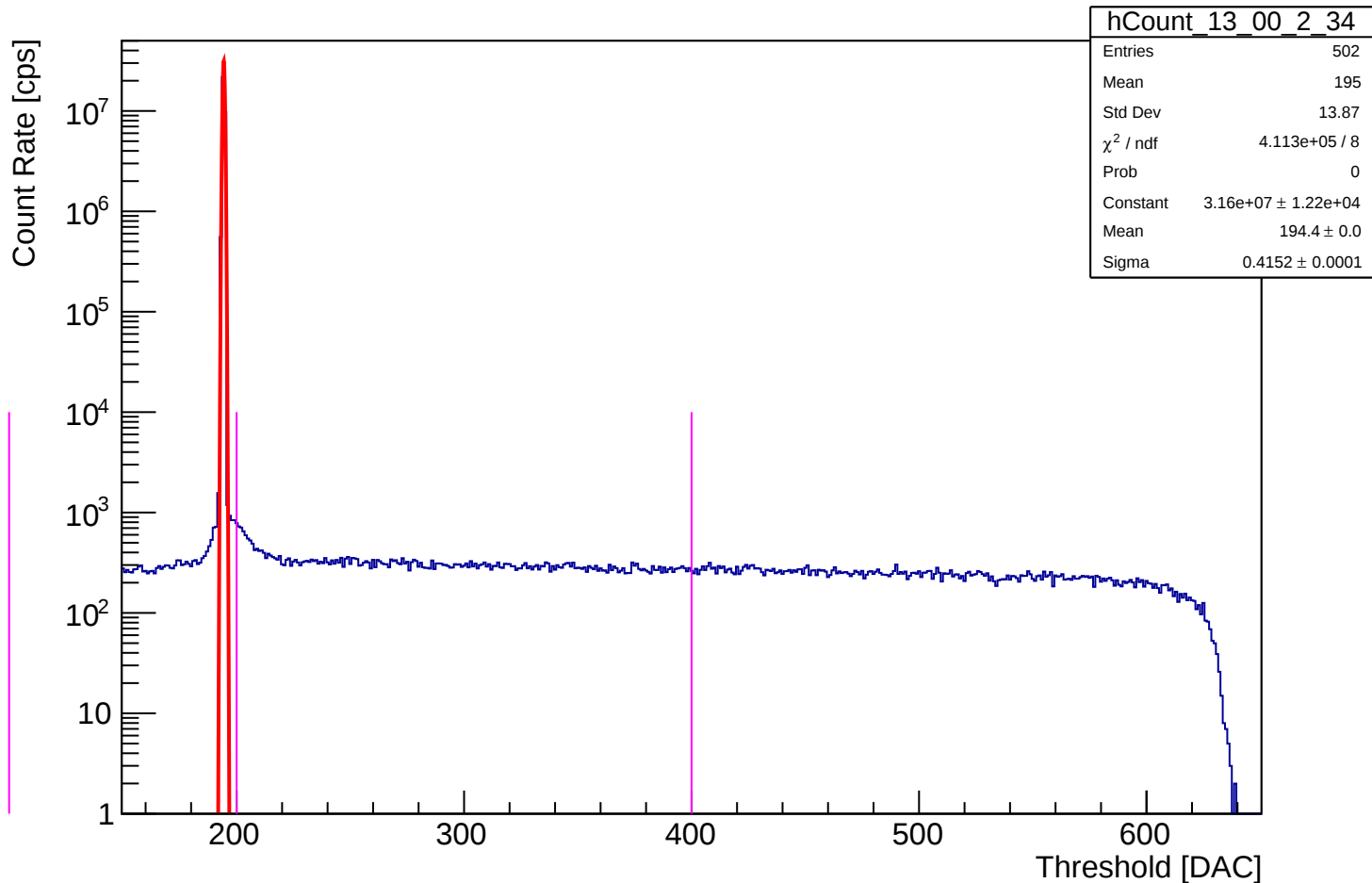
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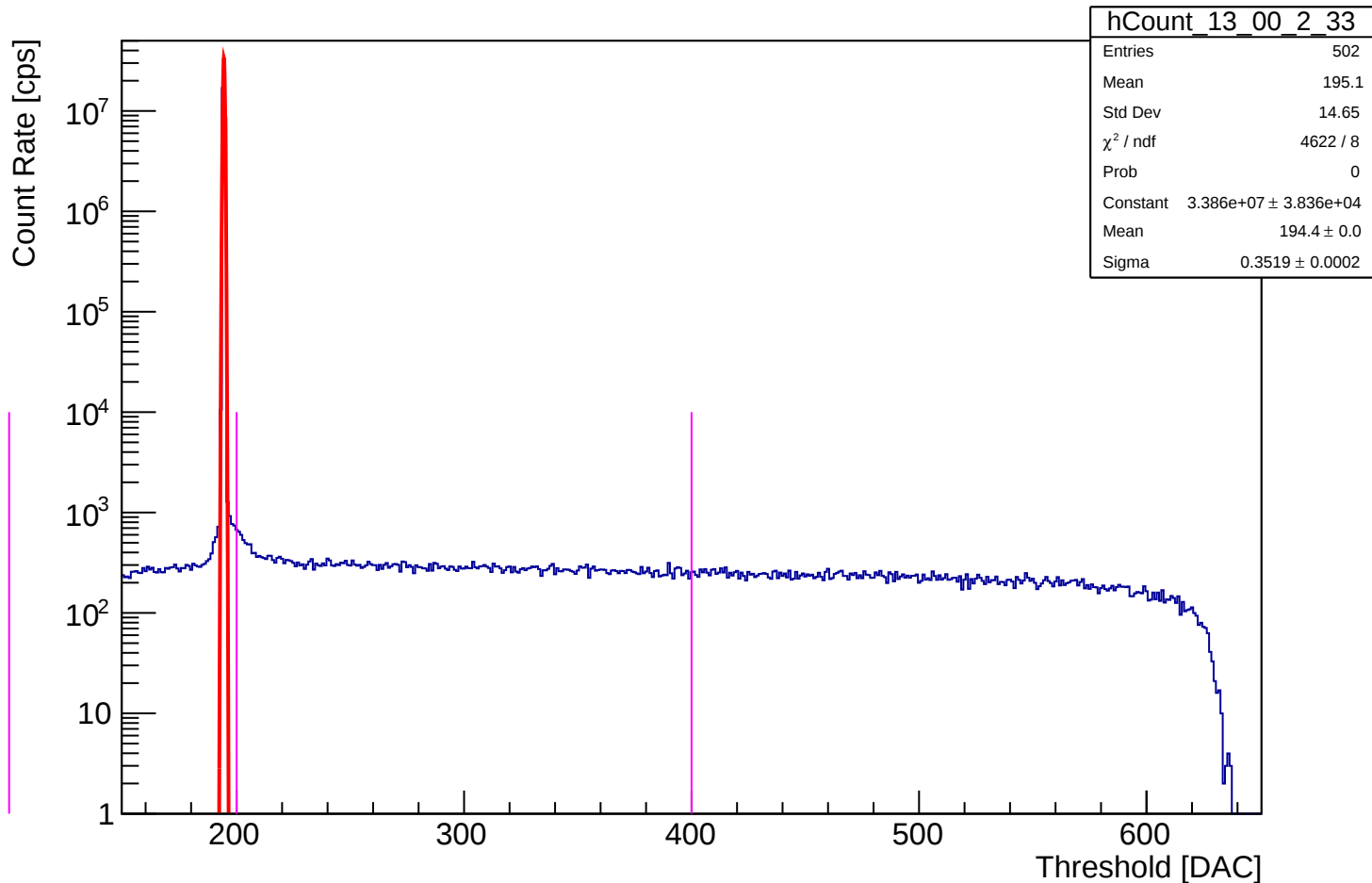
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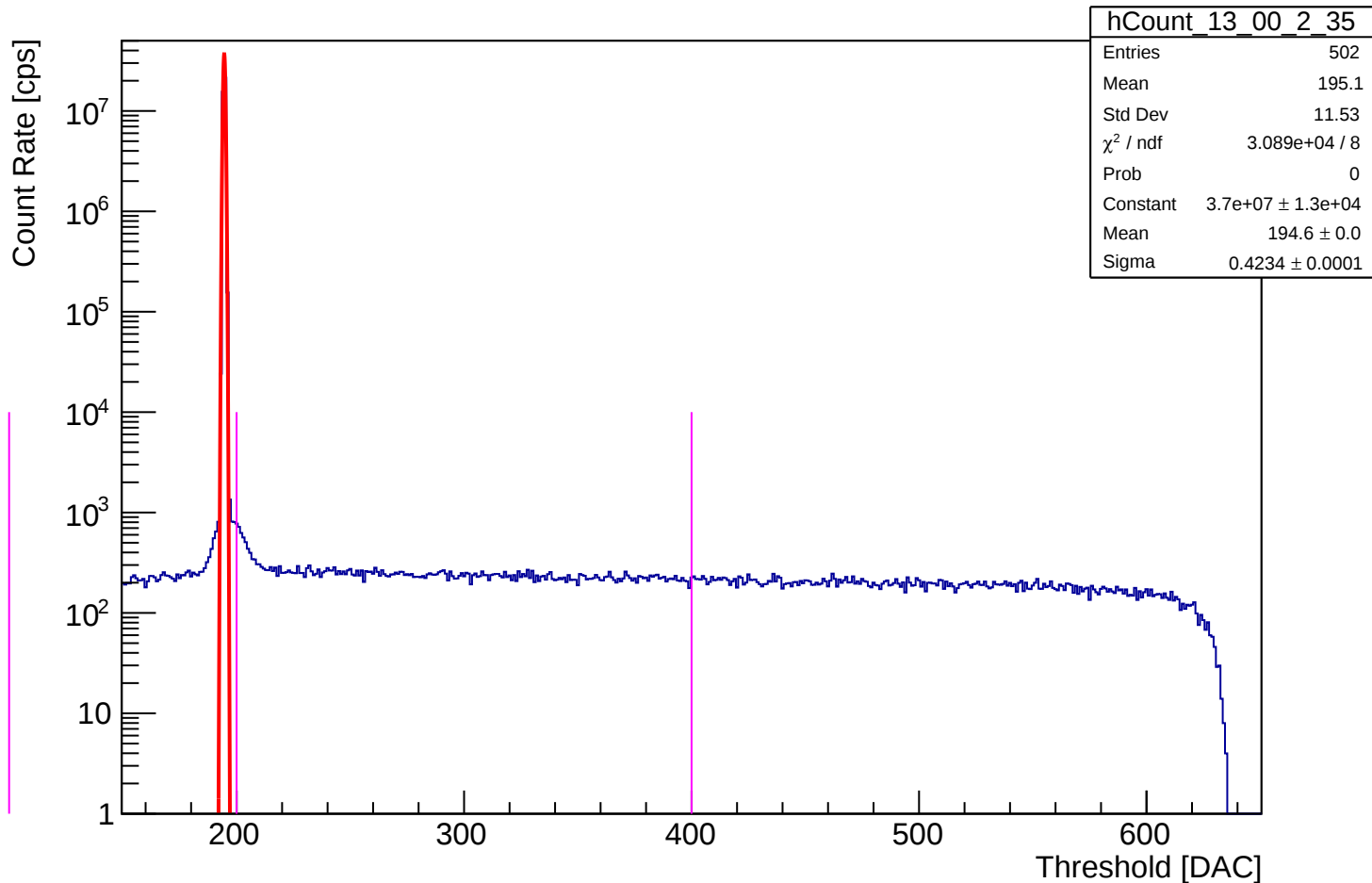
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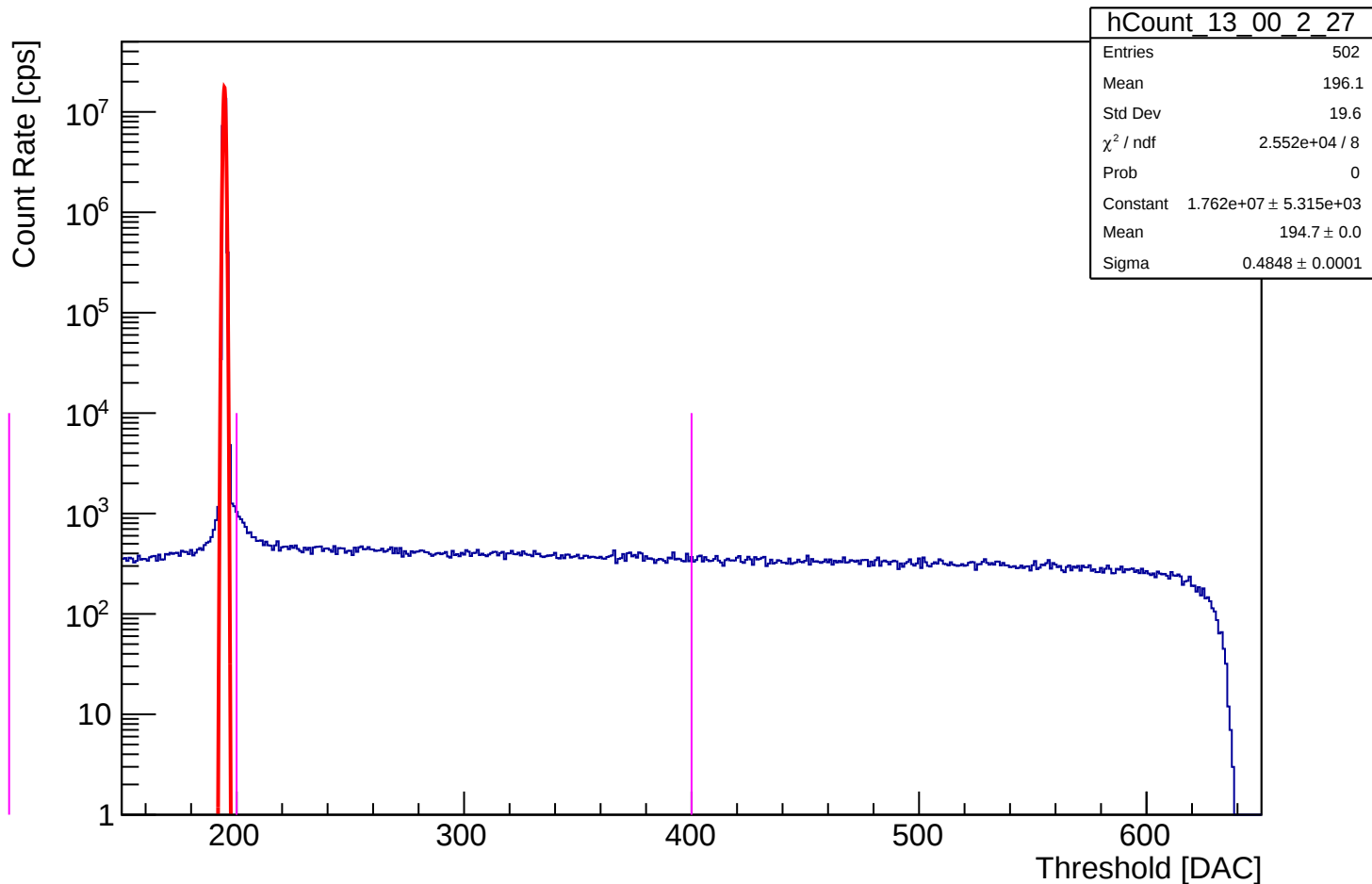
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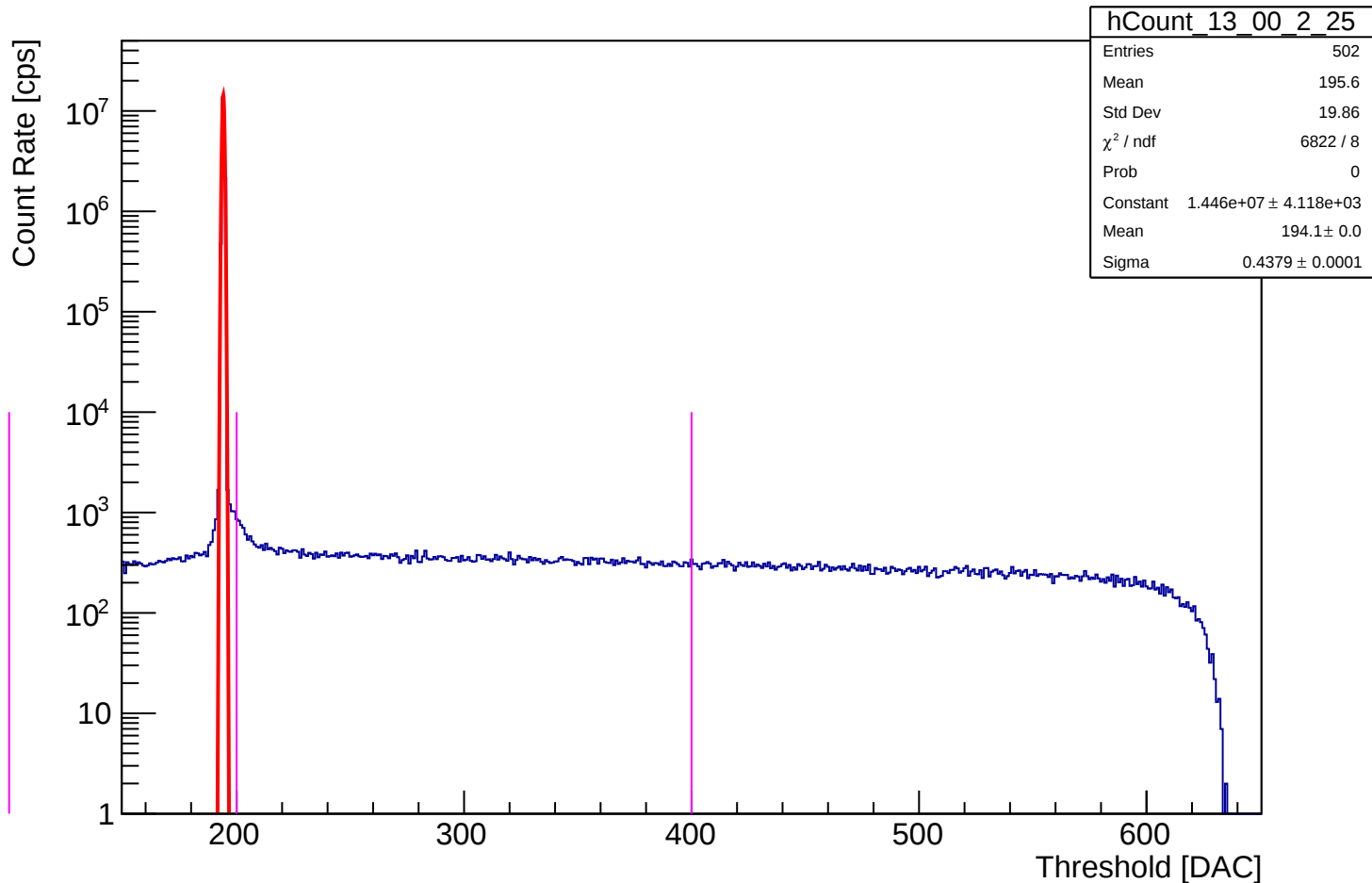
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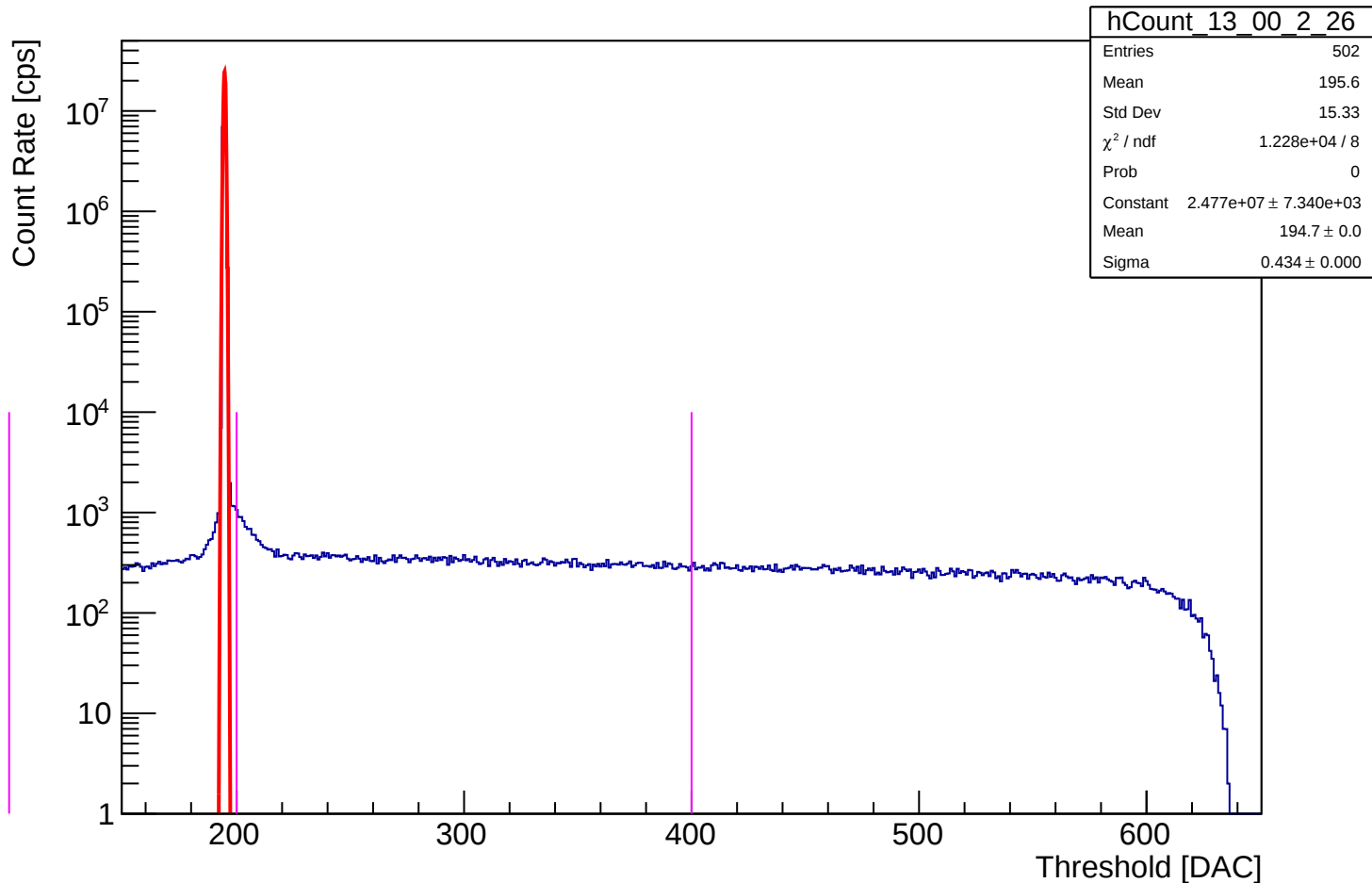
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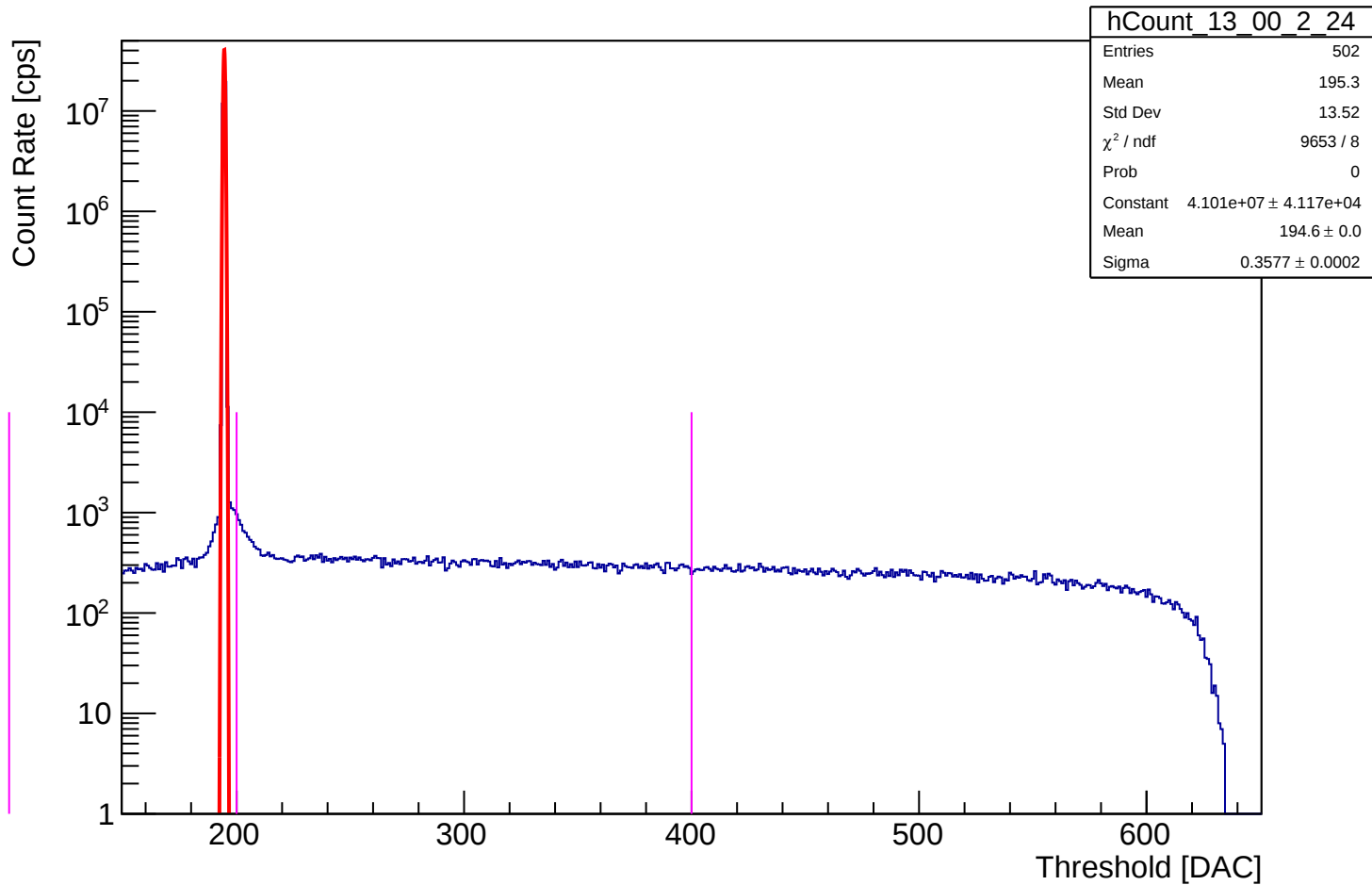
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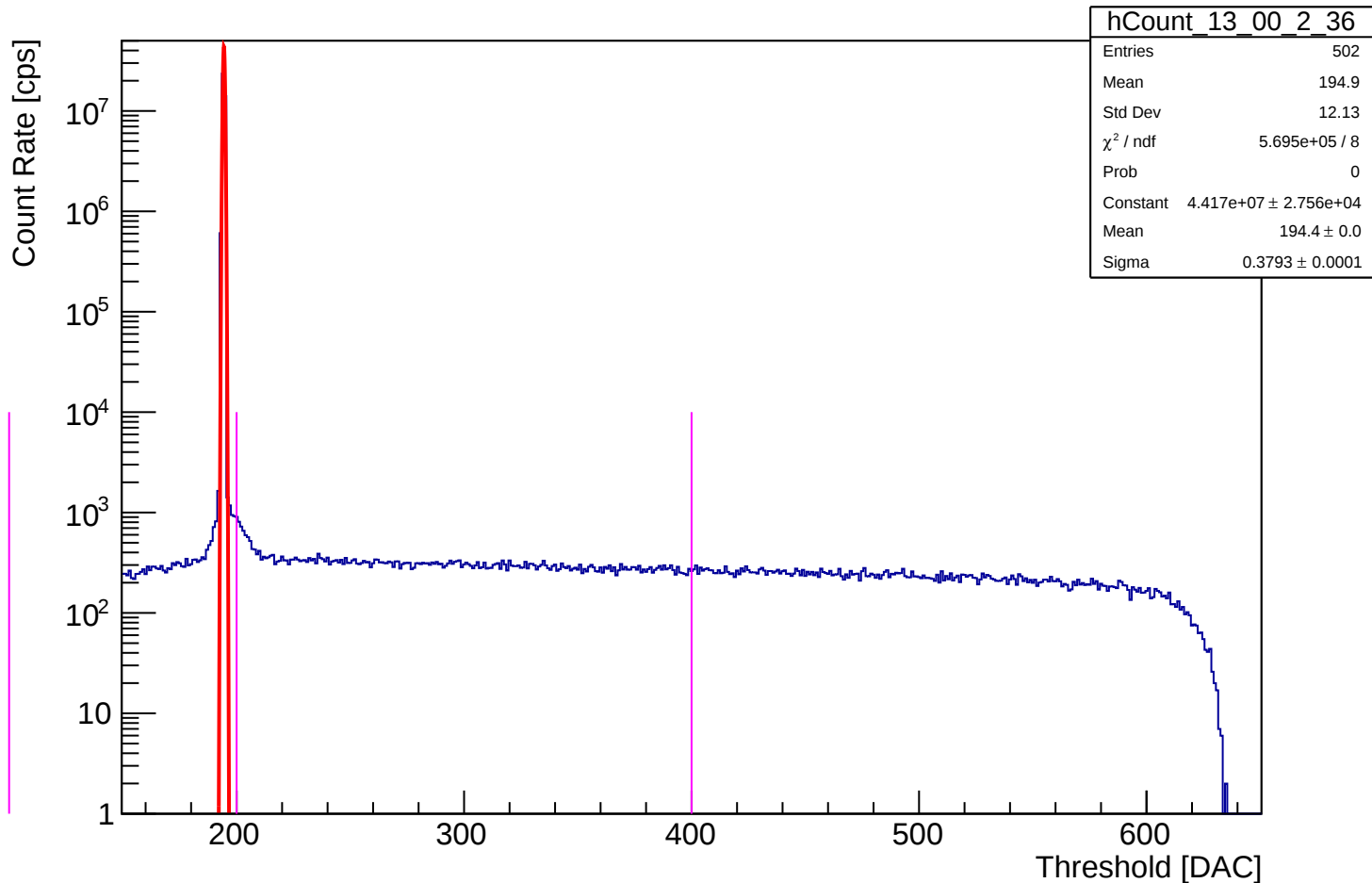
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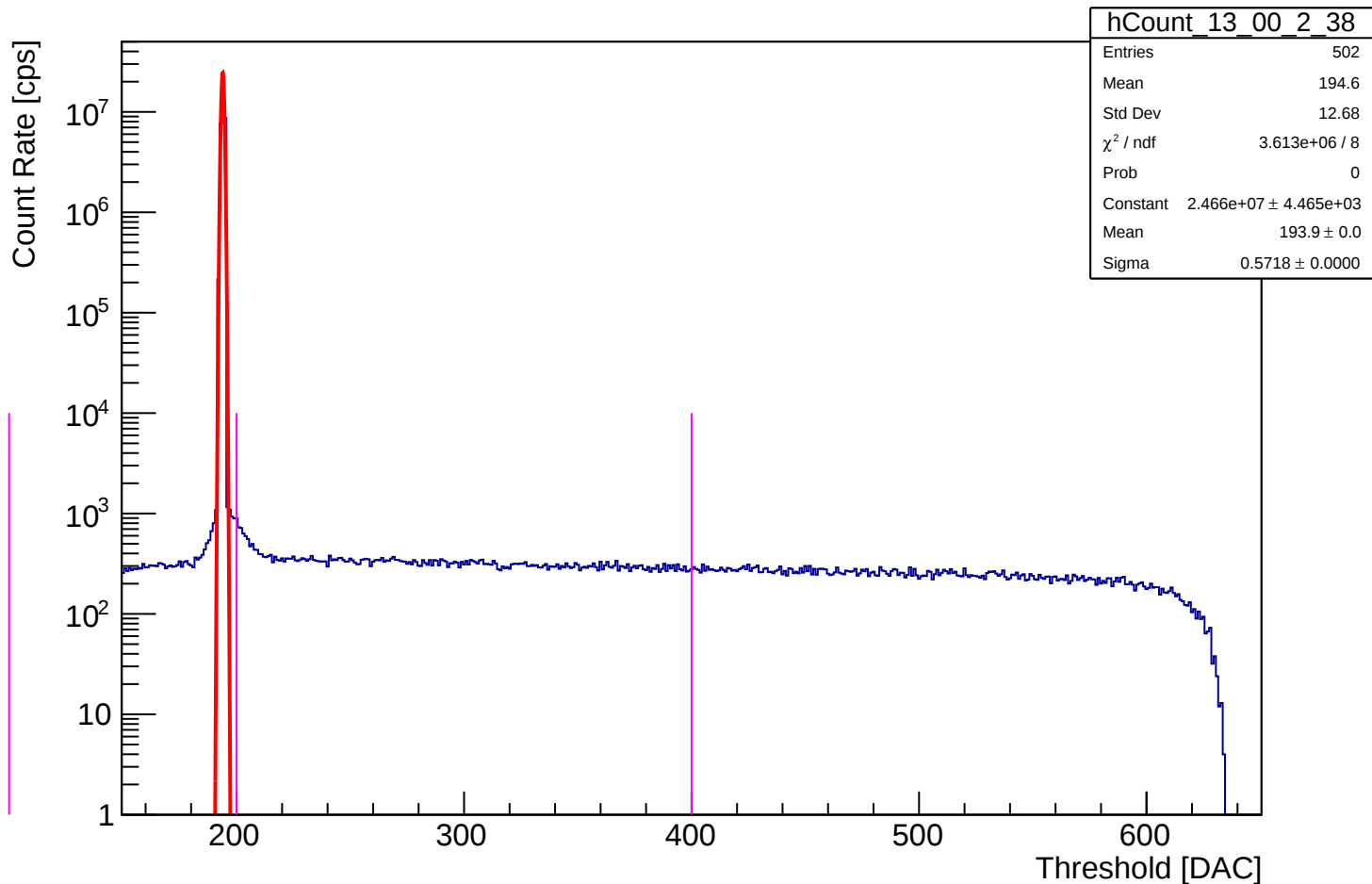
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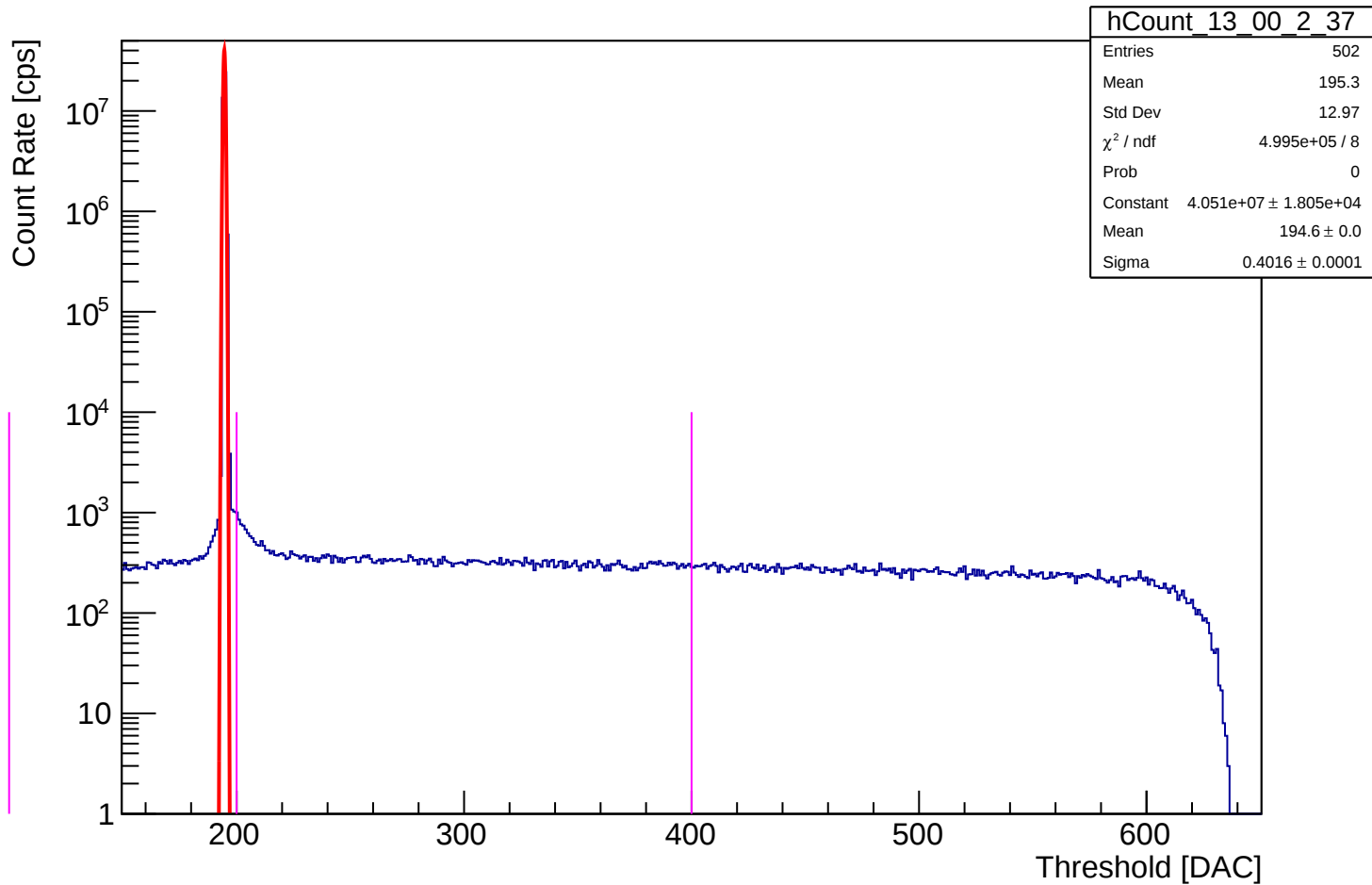
Row 1 Tile 1 Pmt 3 Pixel 13 Slot 13 Fiber 0 Asic 2 Channel 36



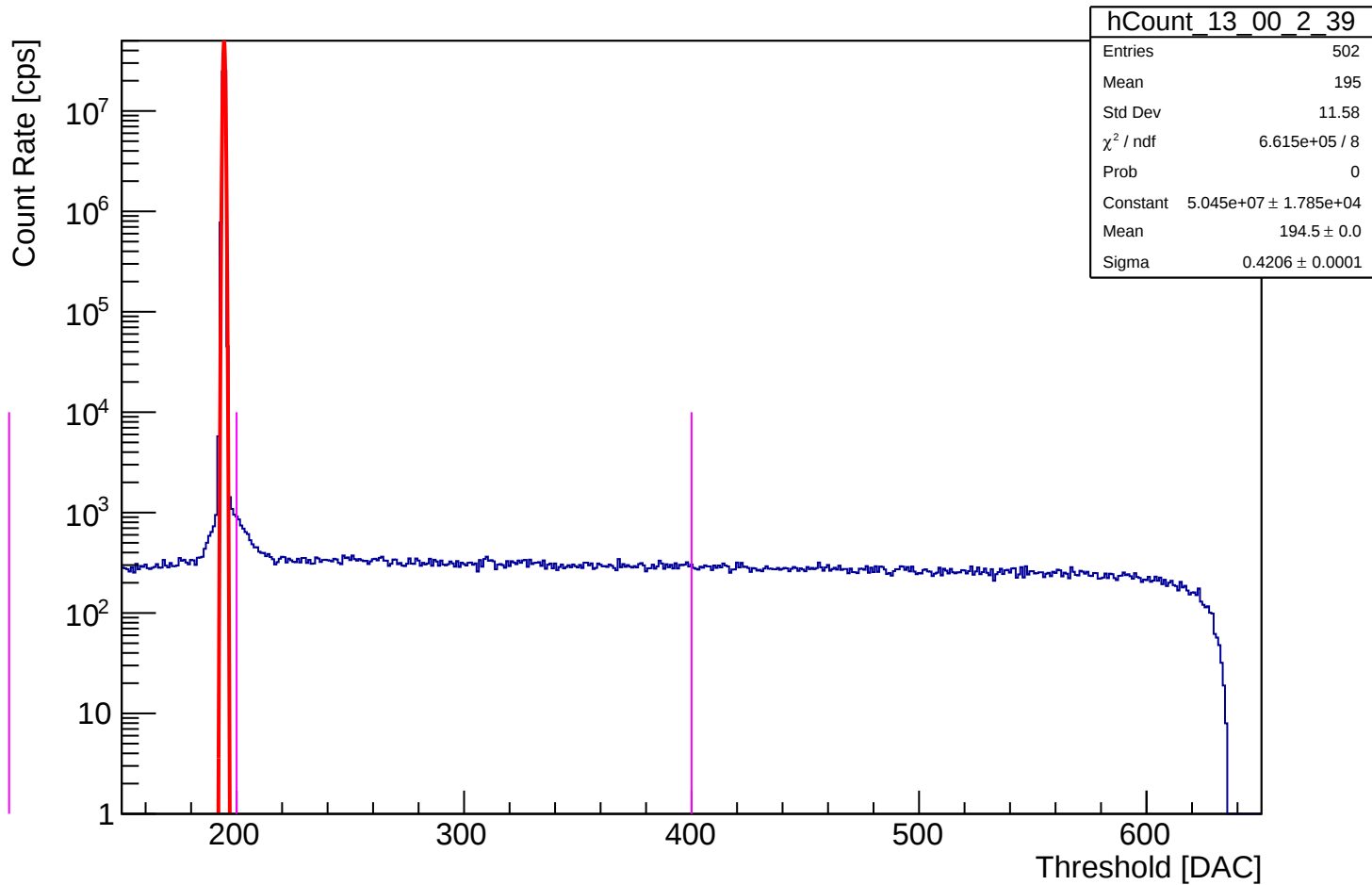
Row 1 Tile 1 Pmt 3 Pixel 14 Slot 13 Fiber 0 Asic 2 Channel 38



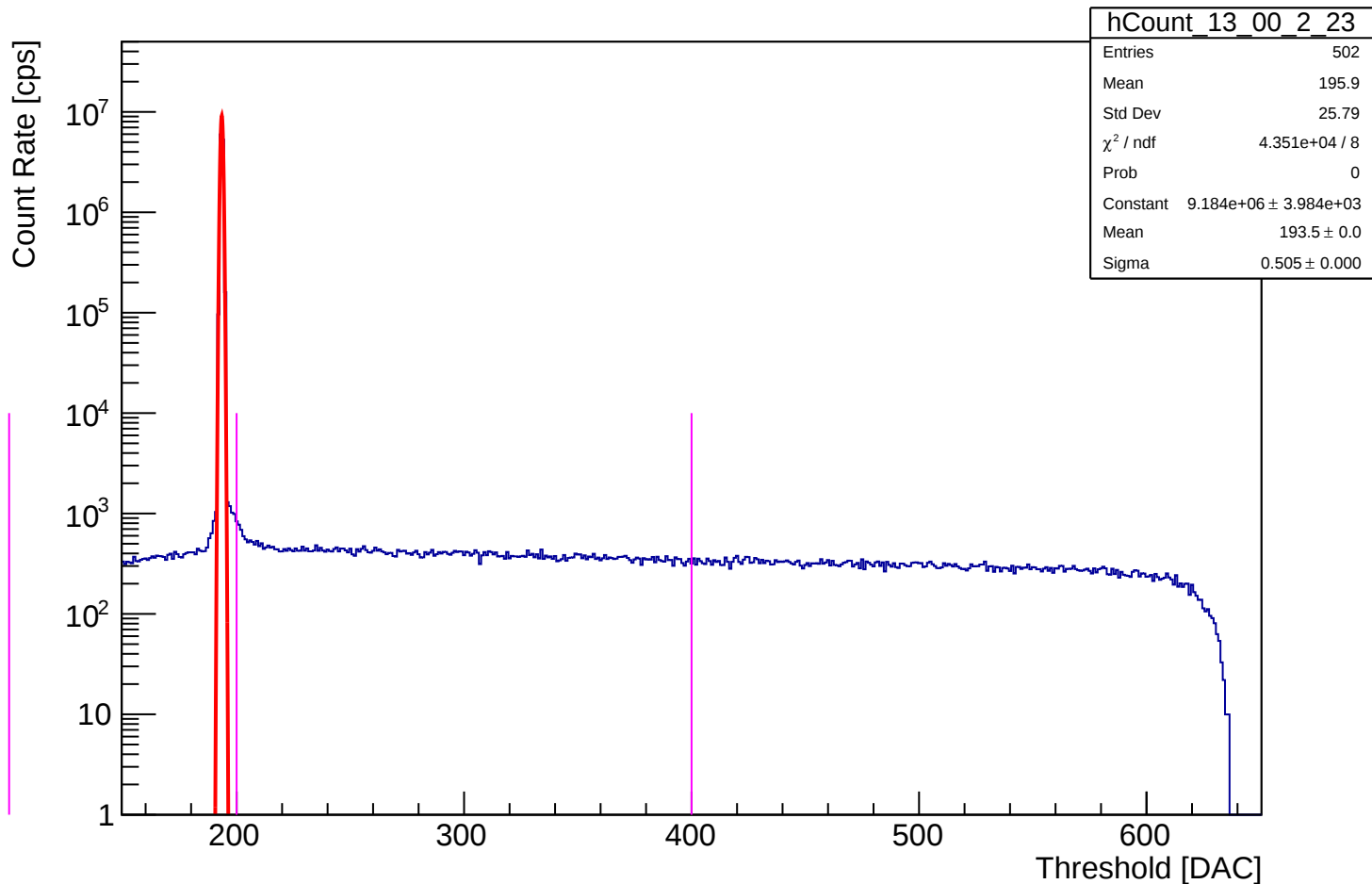
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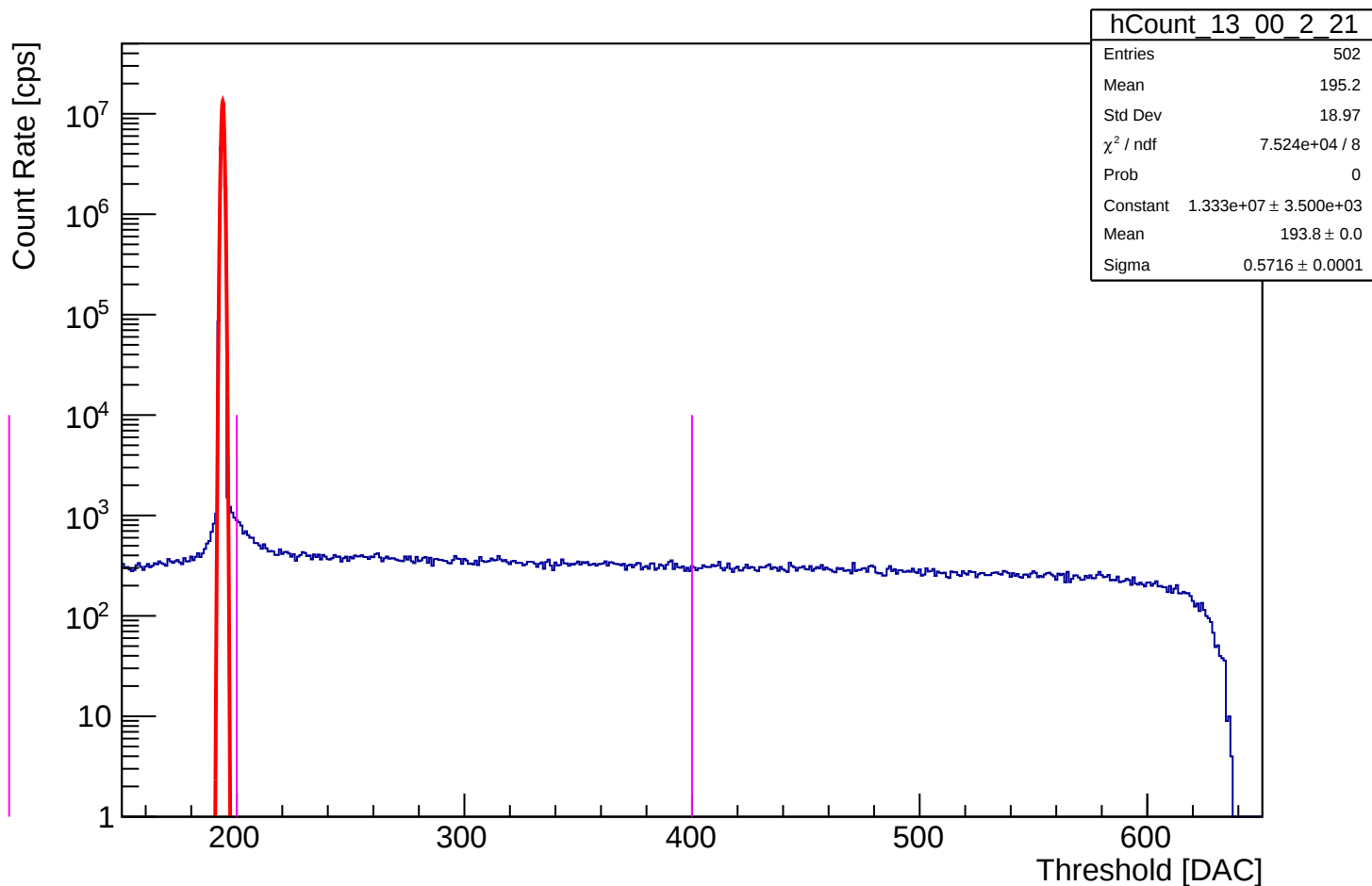
Row 1 Tile 1 Pmt 3 Pixel 16 Slot 13 Fiber 0 Asic 2 Channel 39



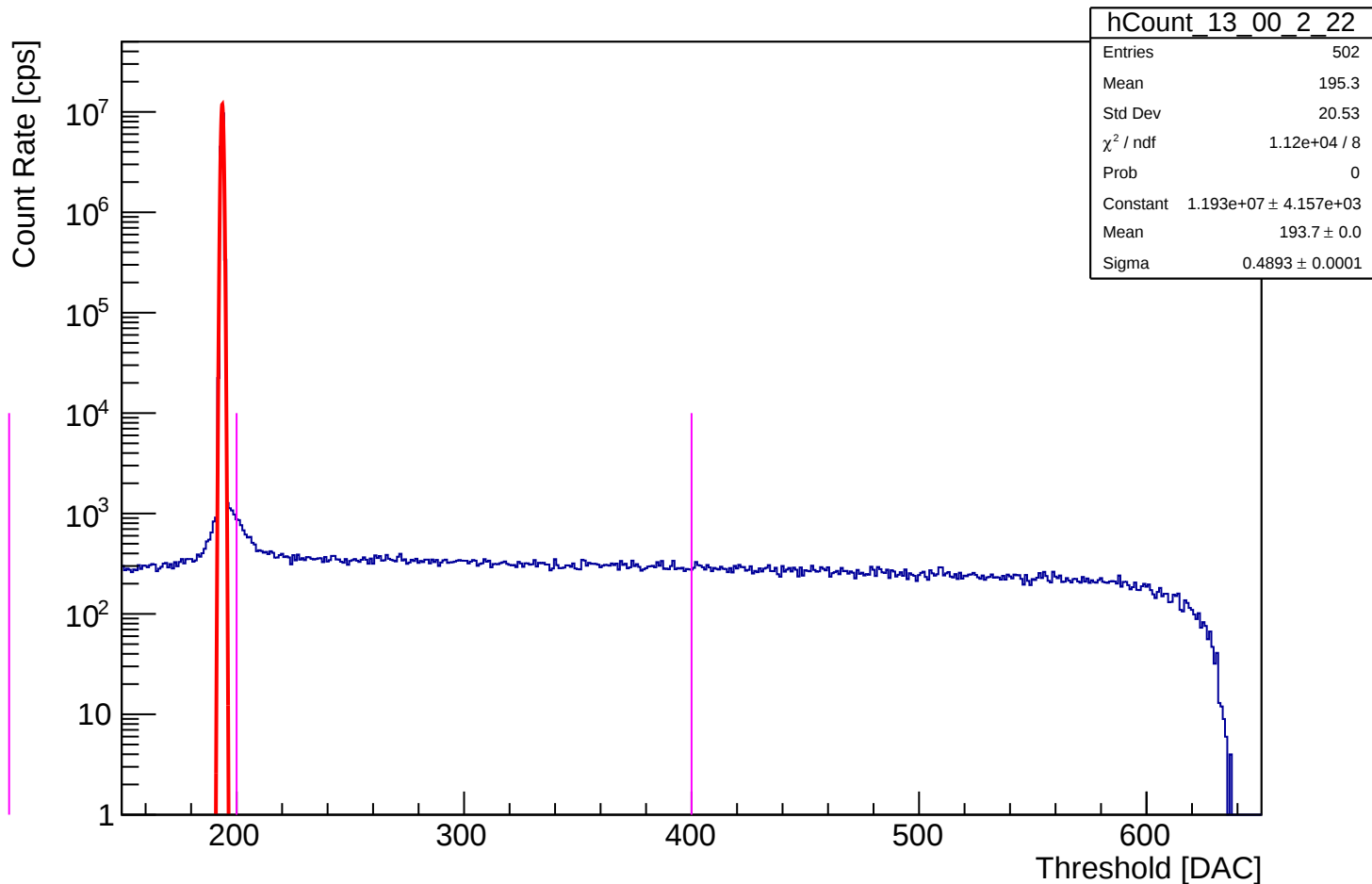
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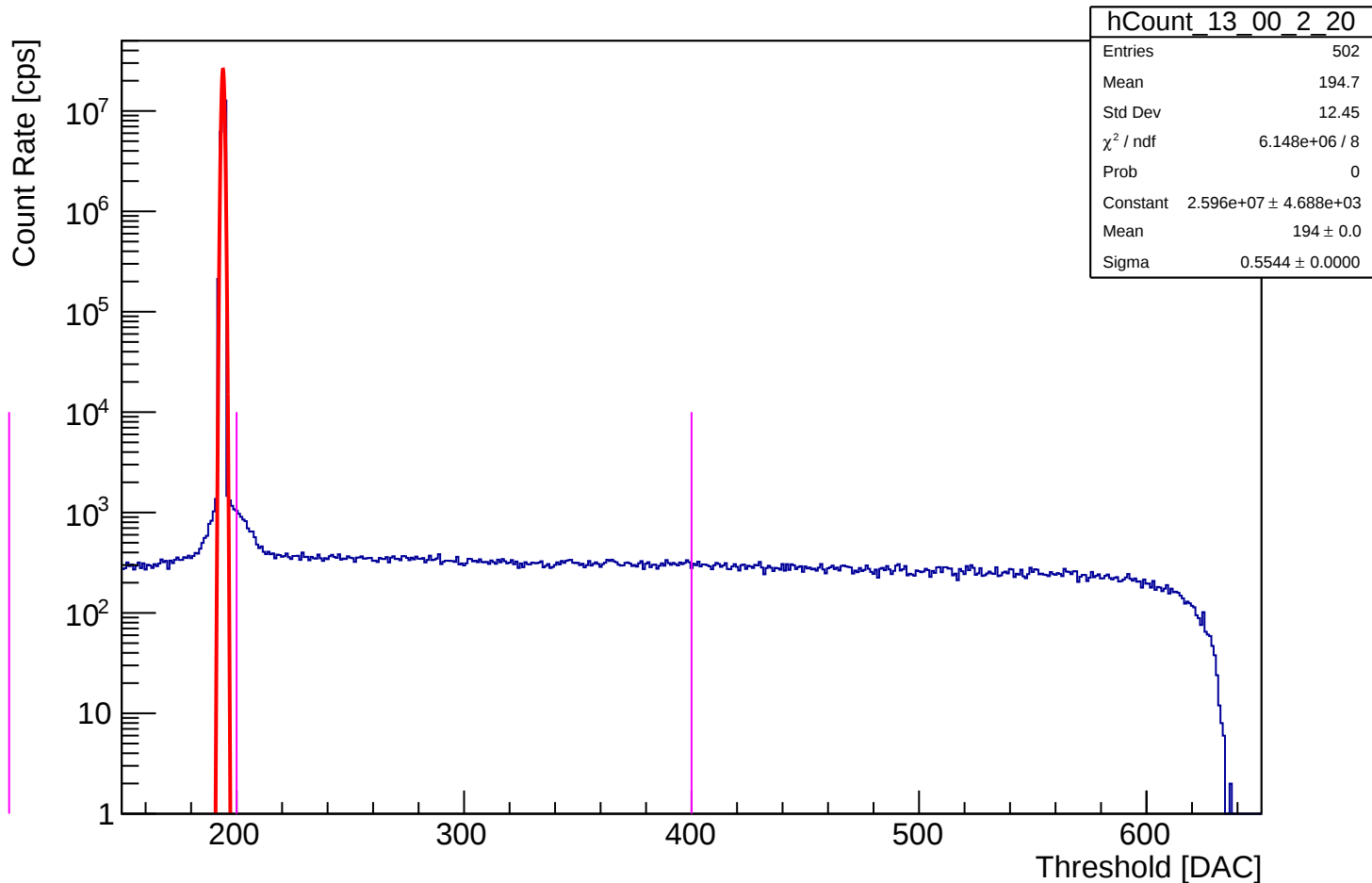
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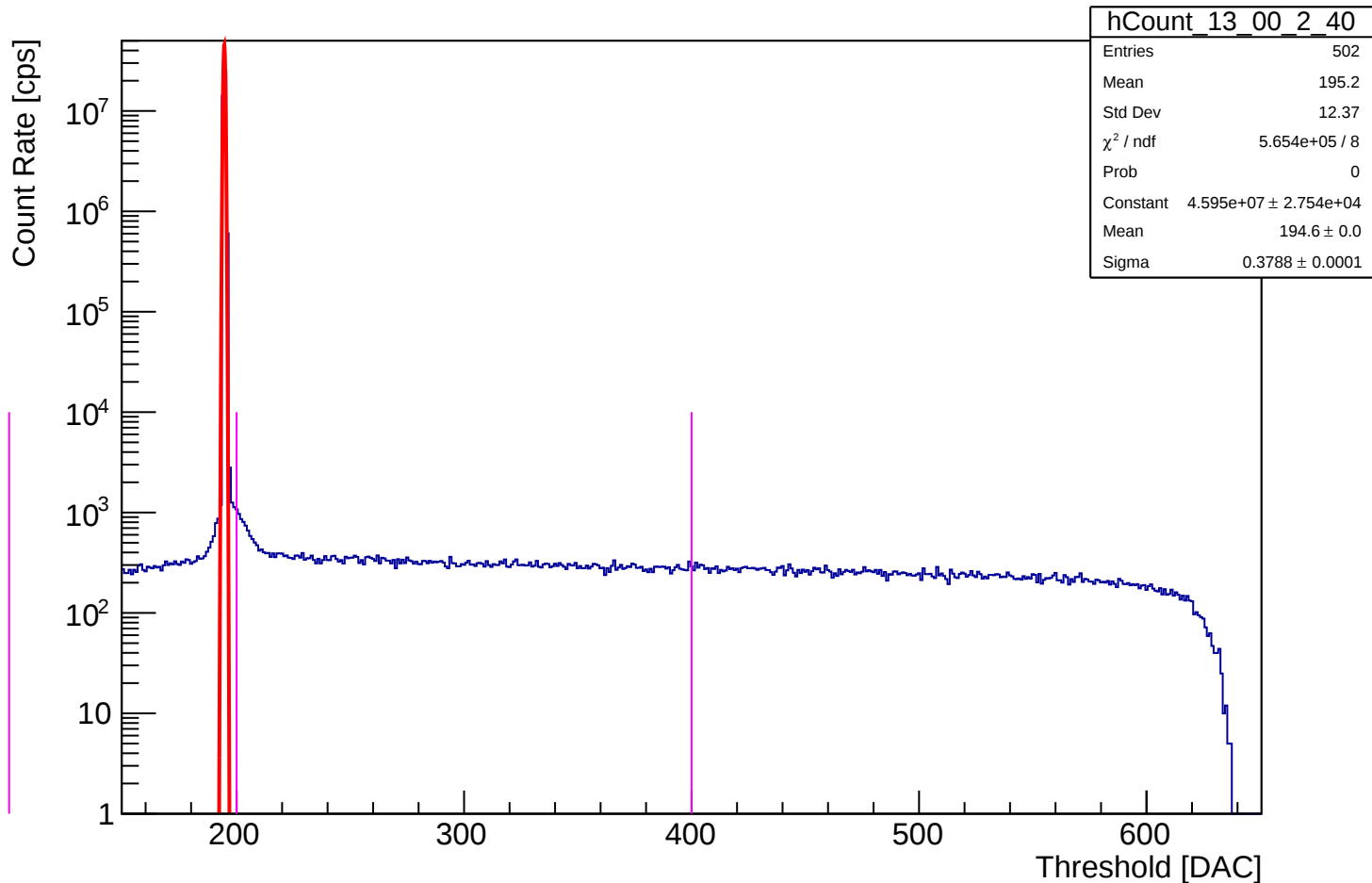
Row 1 Tile 1 Pmt 3 Pixel 19 Slot 13 Fiber 0 Asic 2 Channel 22



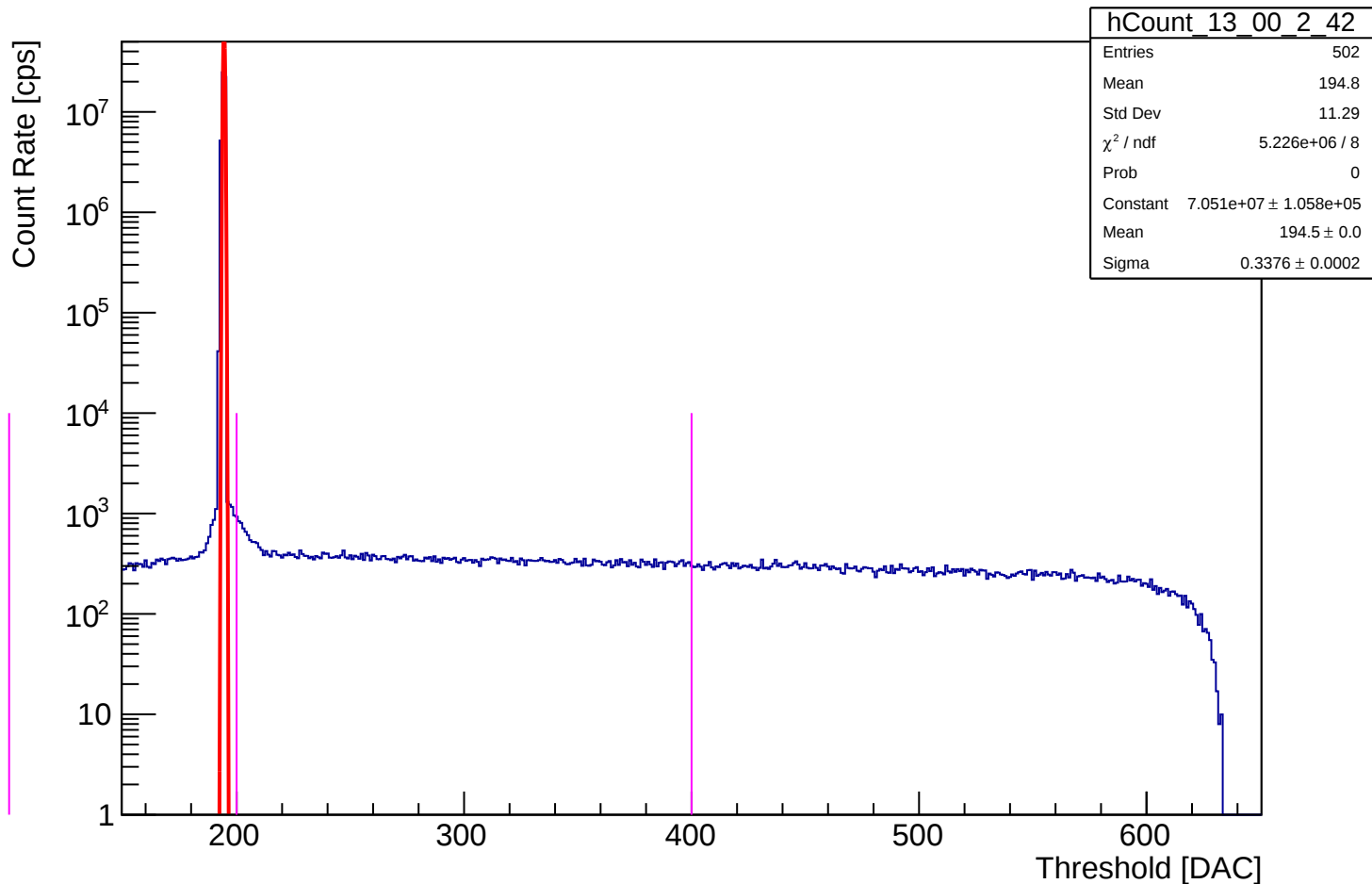
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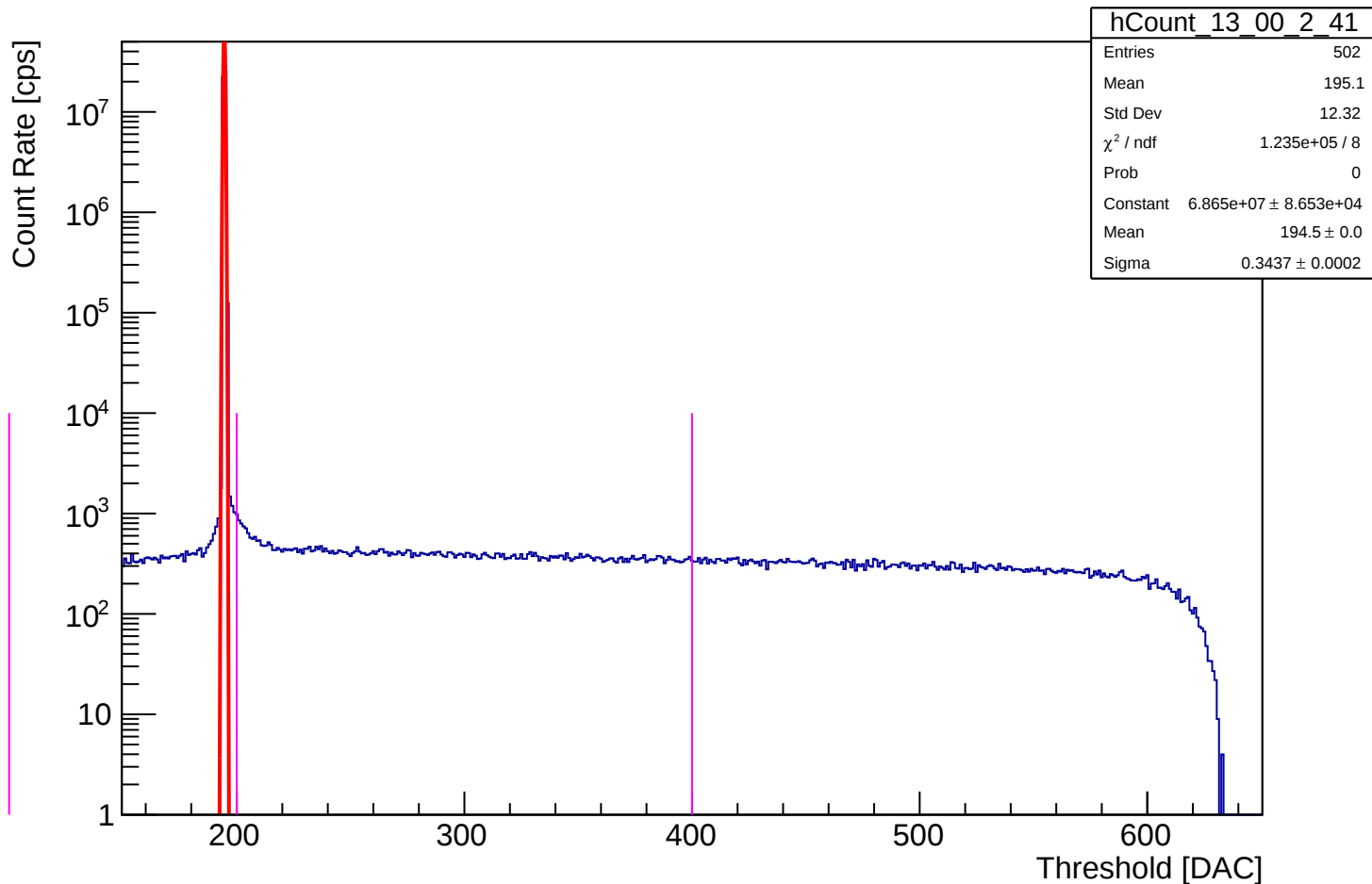
Row 1 Tile 1 Pmt 3 Pixel 21 Slot 13 Fiber 0 Asic 2 Channel 40



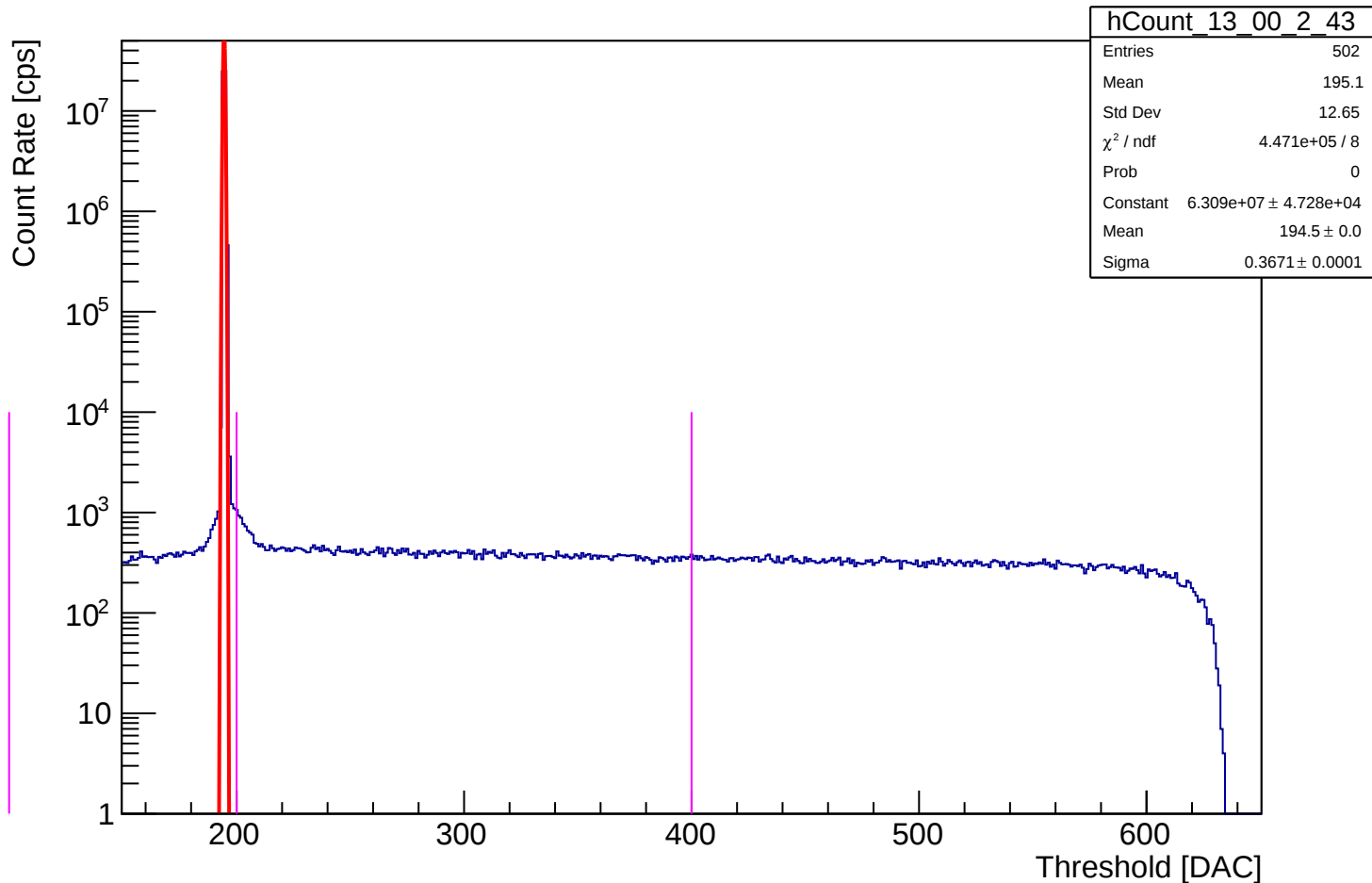
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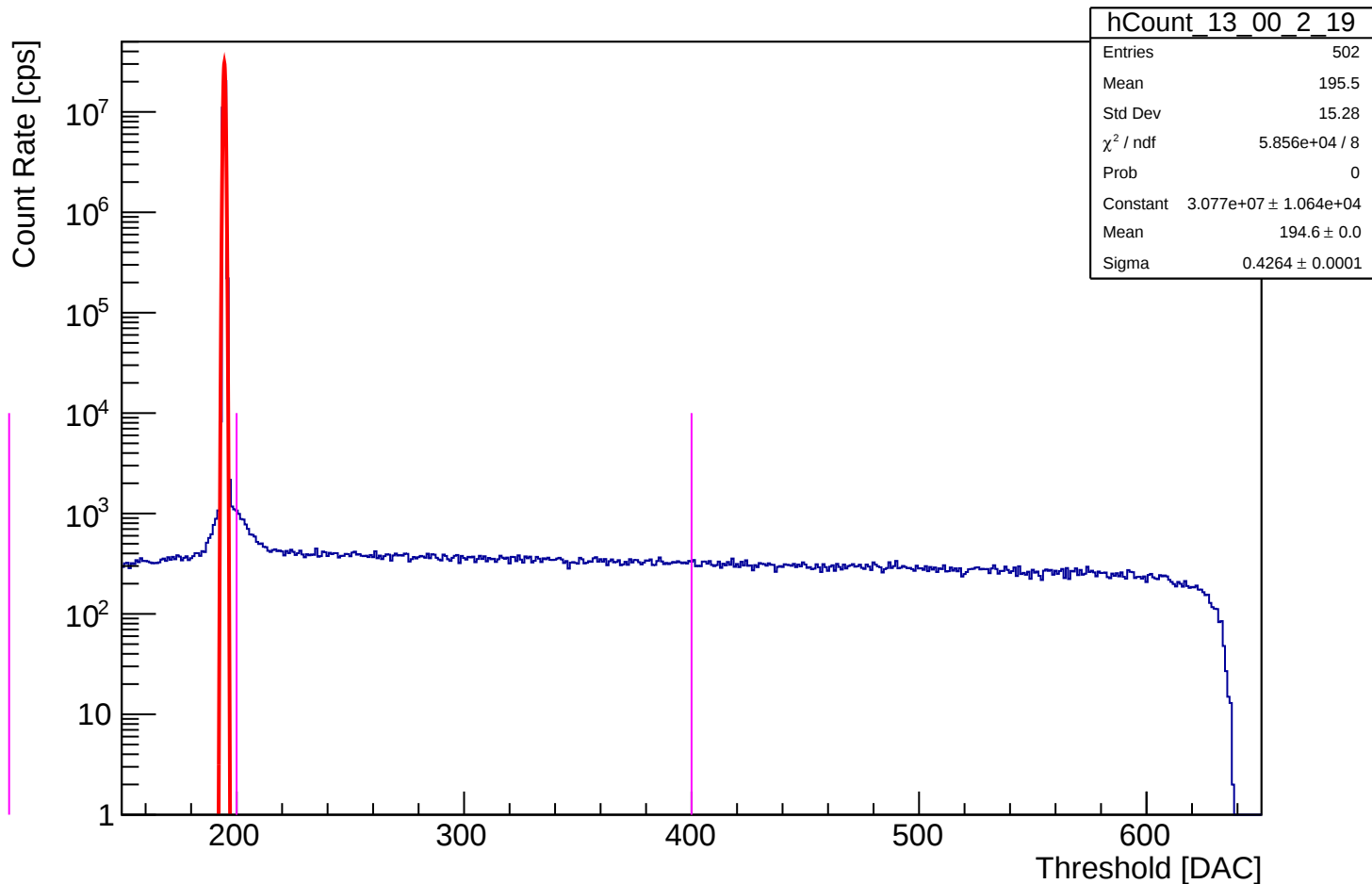
Row 1 Tile 1 Pmt 3 Pixel 23 Slot 13 Fiber 0 Asic 2 Channel 41



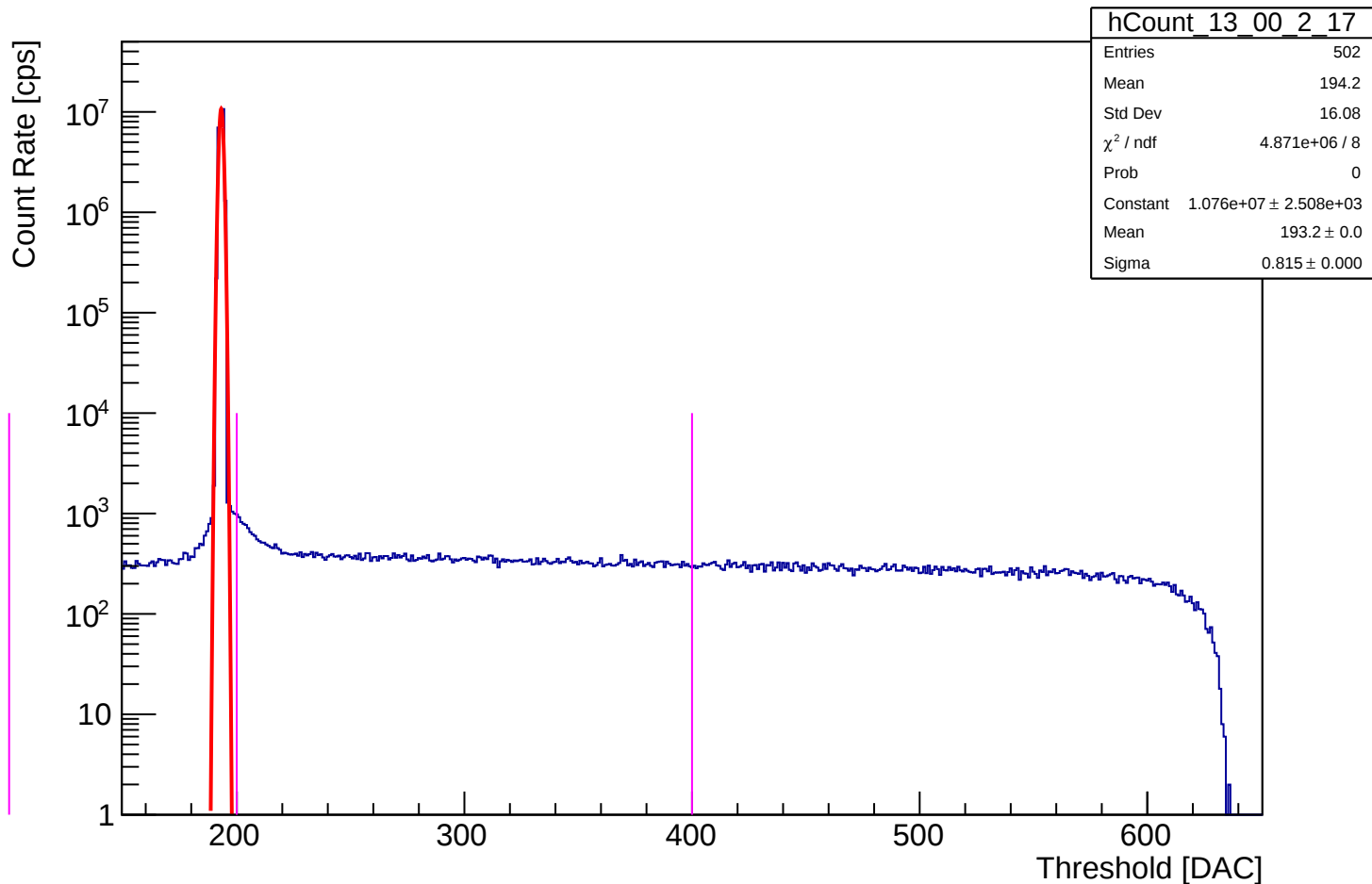
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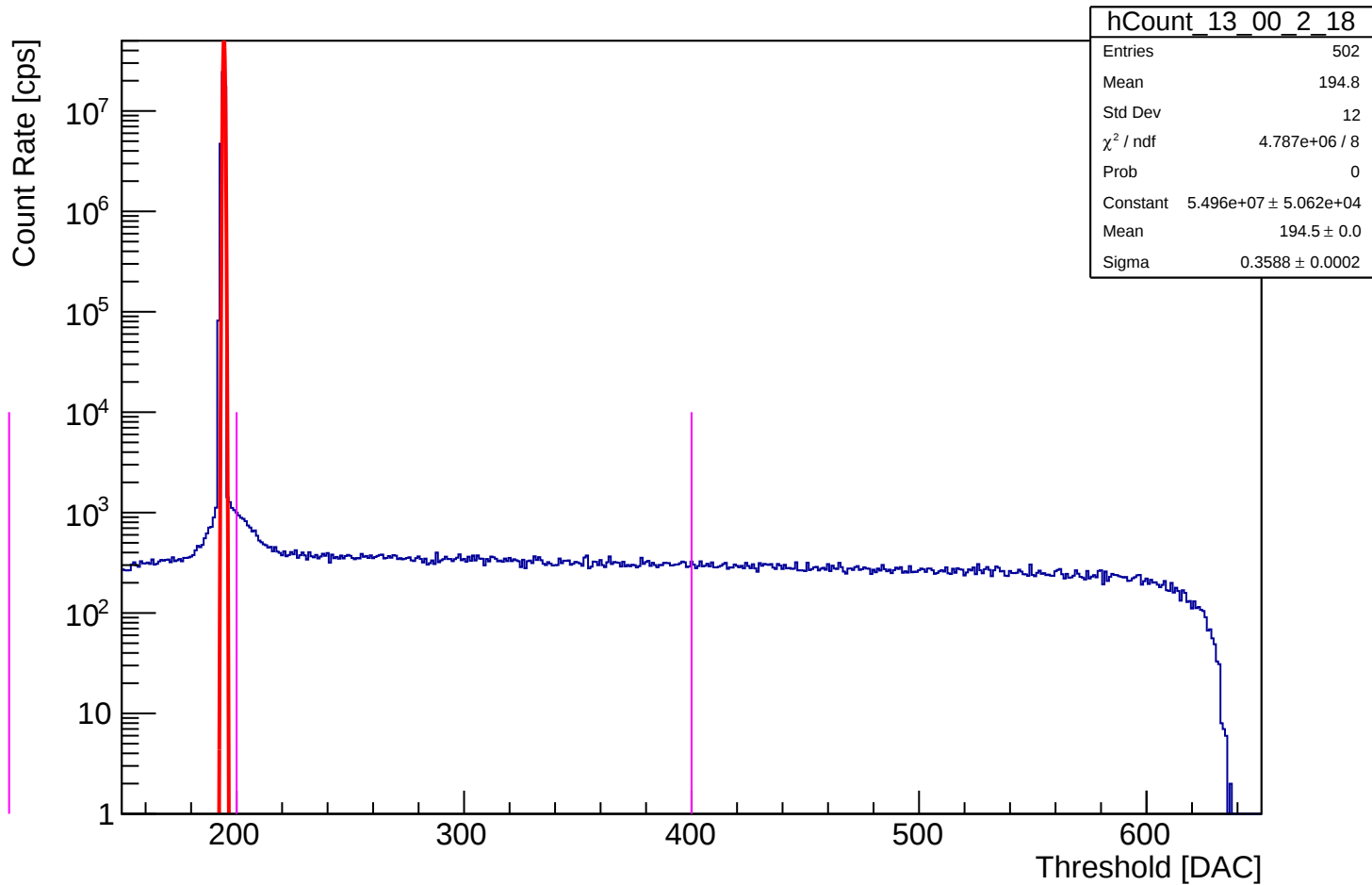
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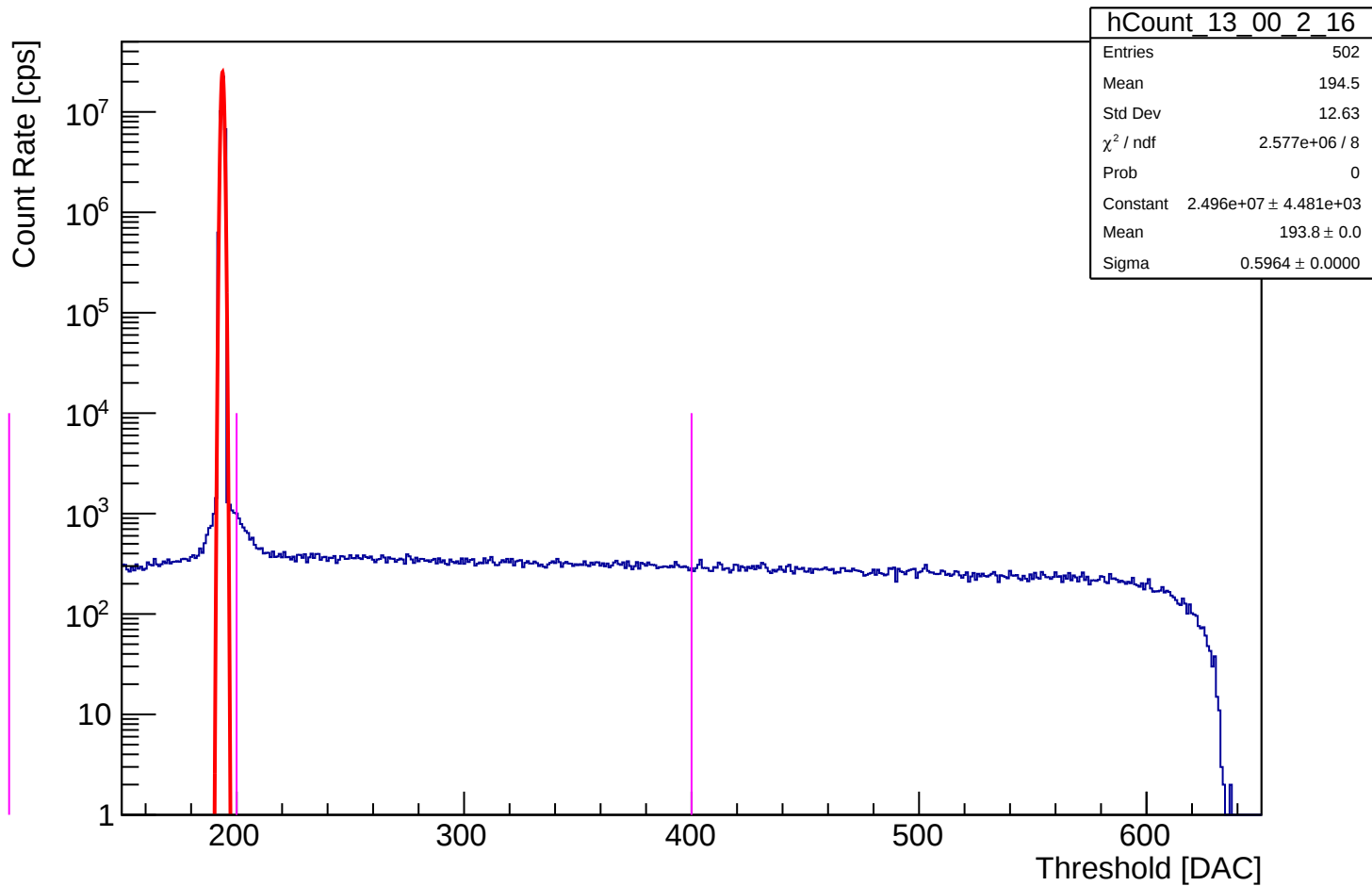
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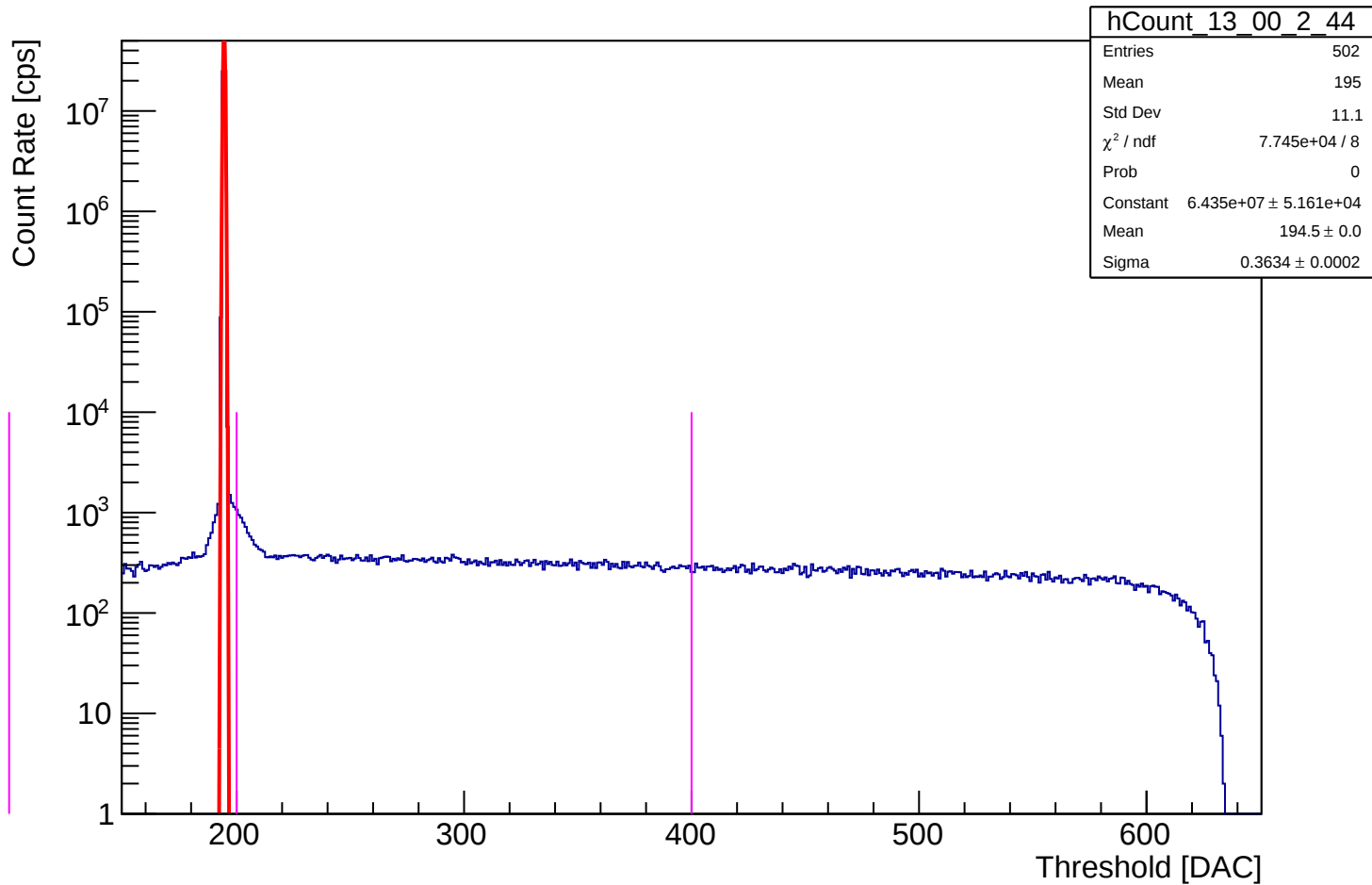
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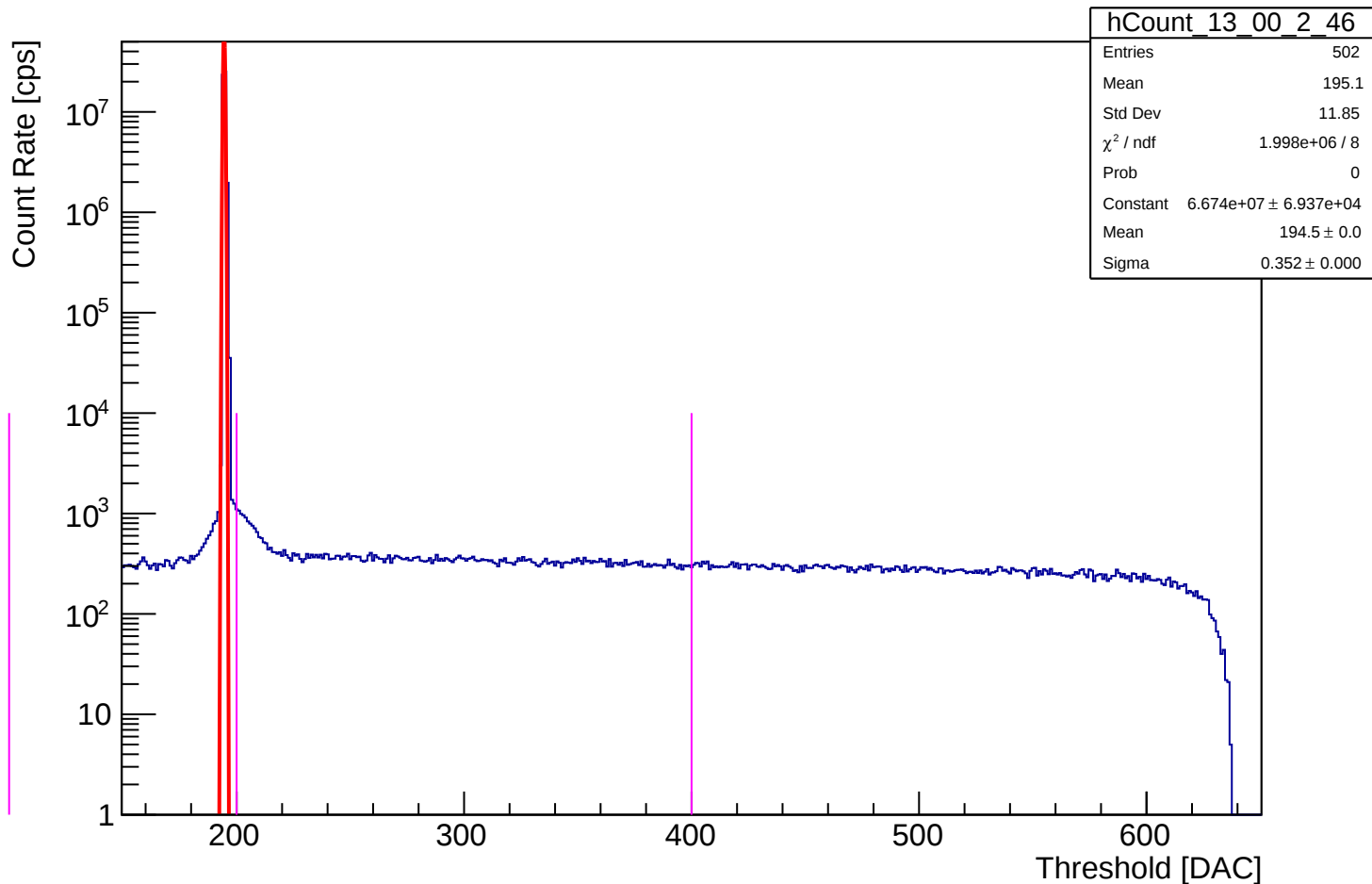
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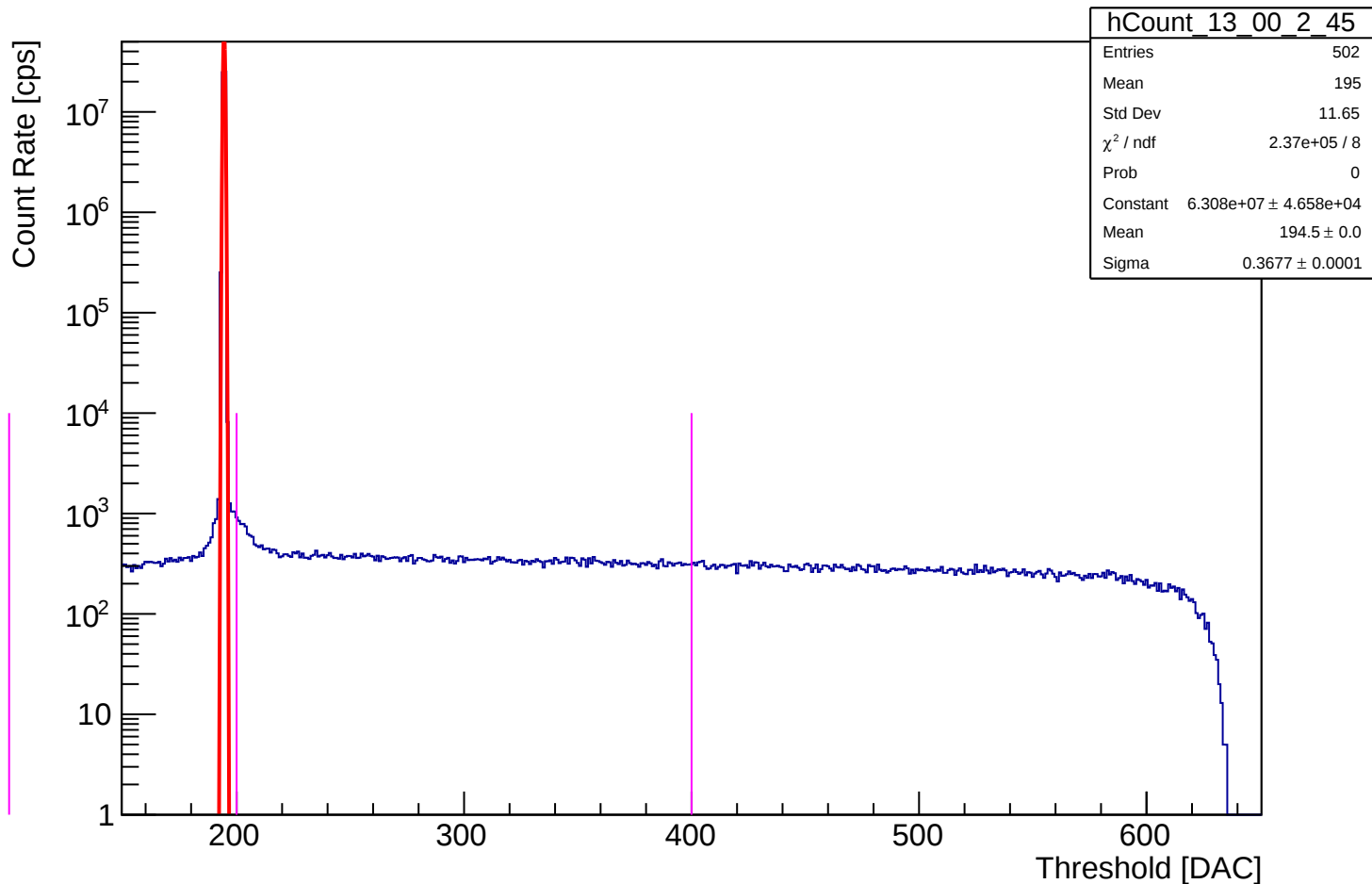
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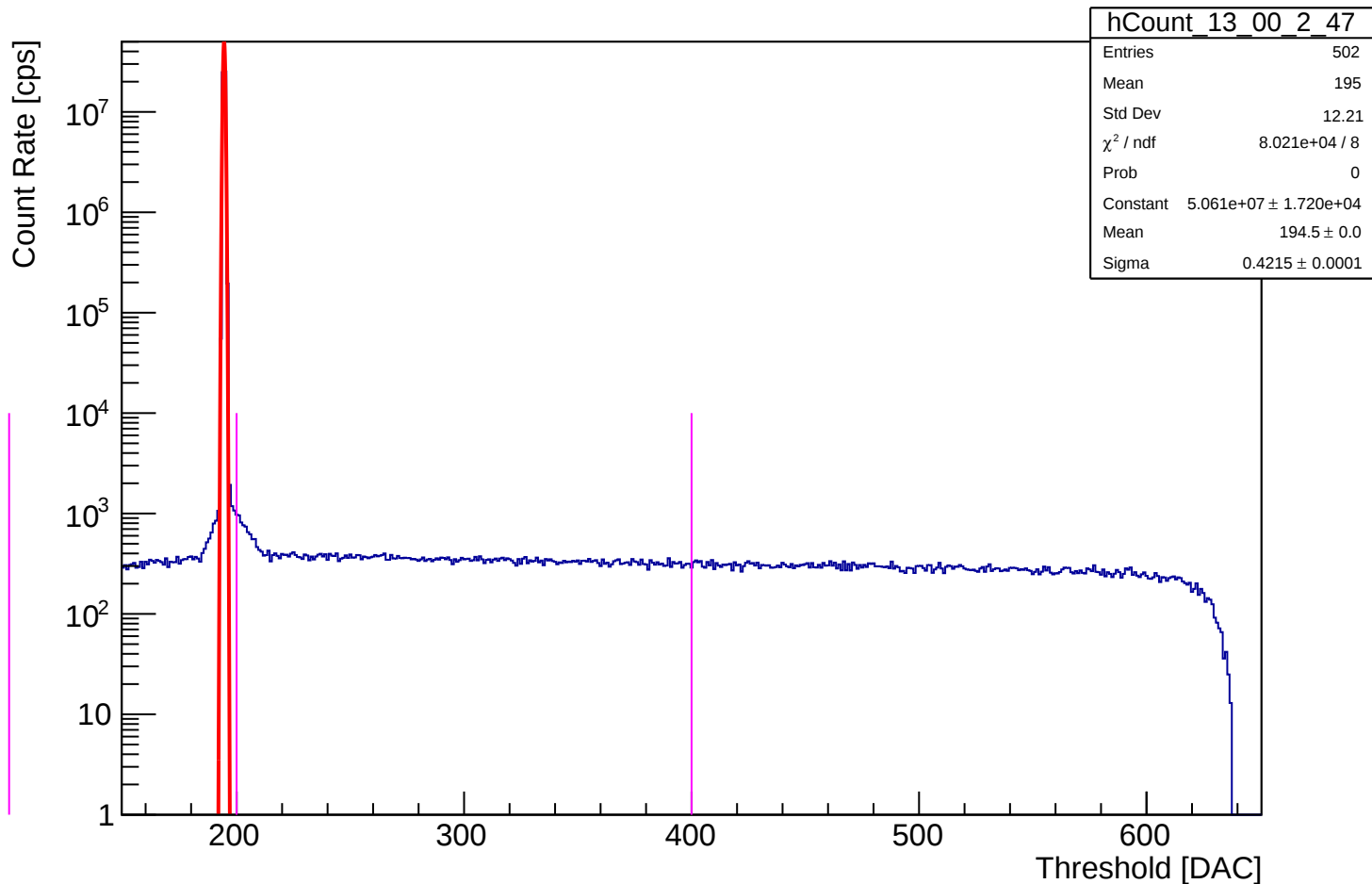
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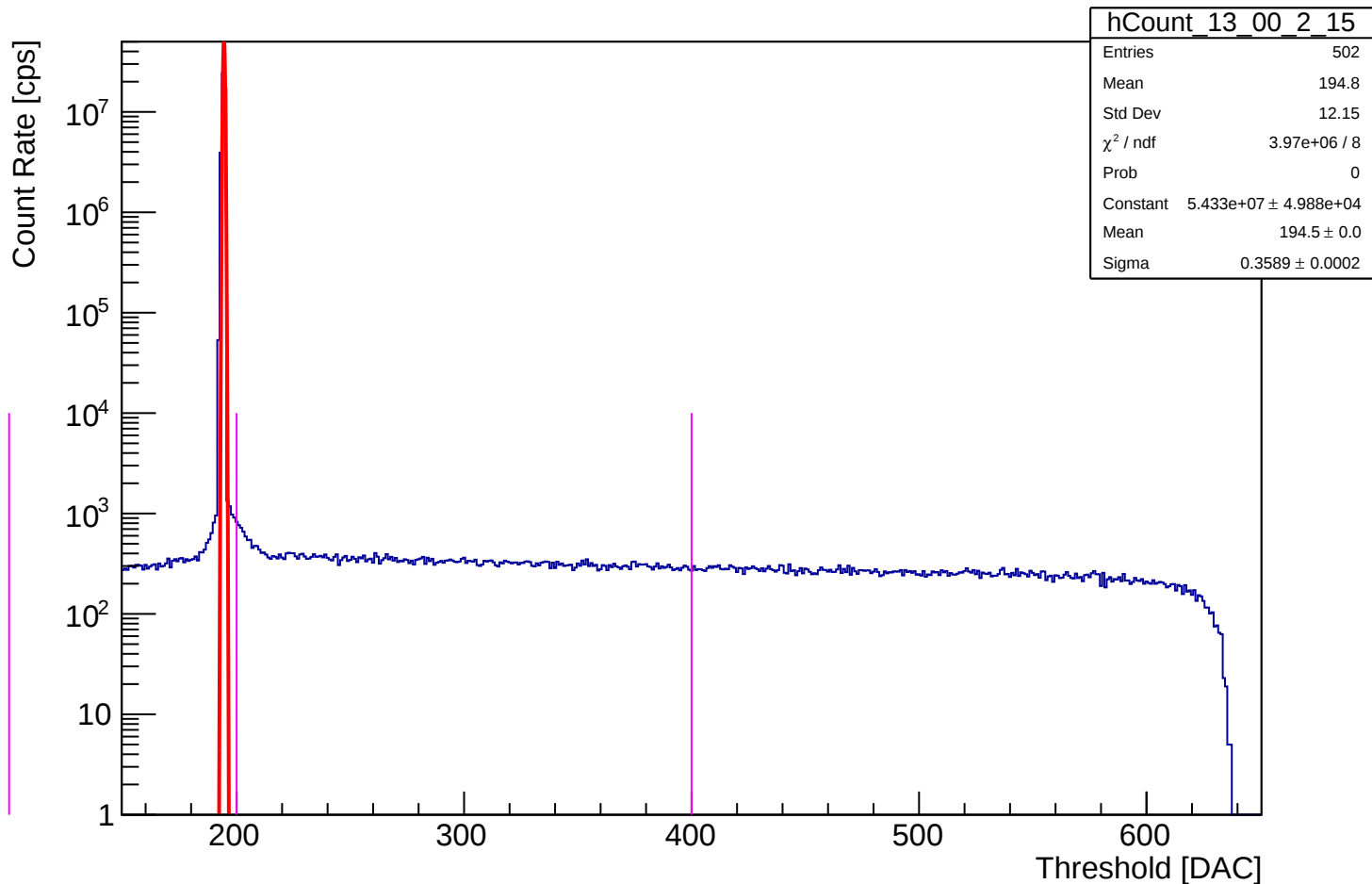
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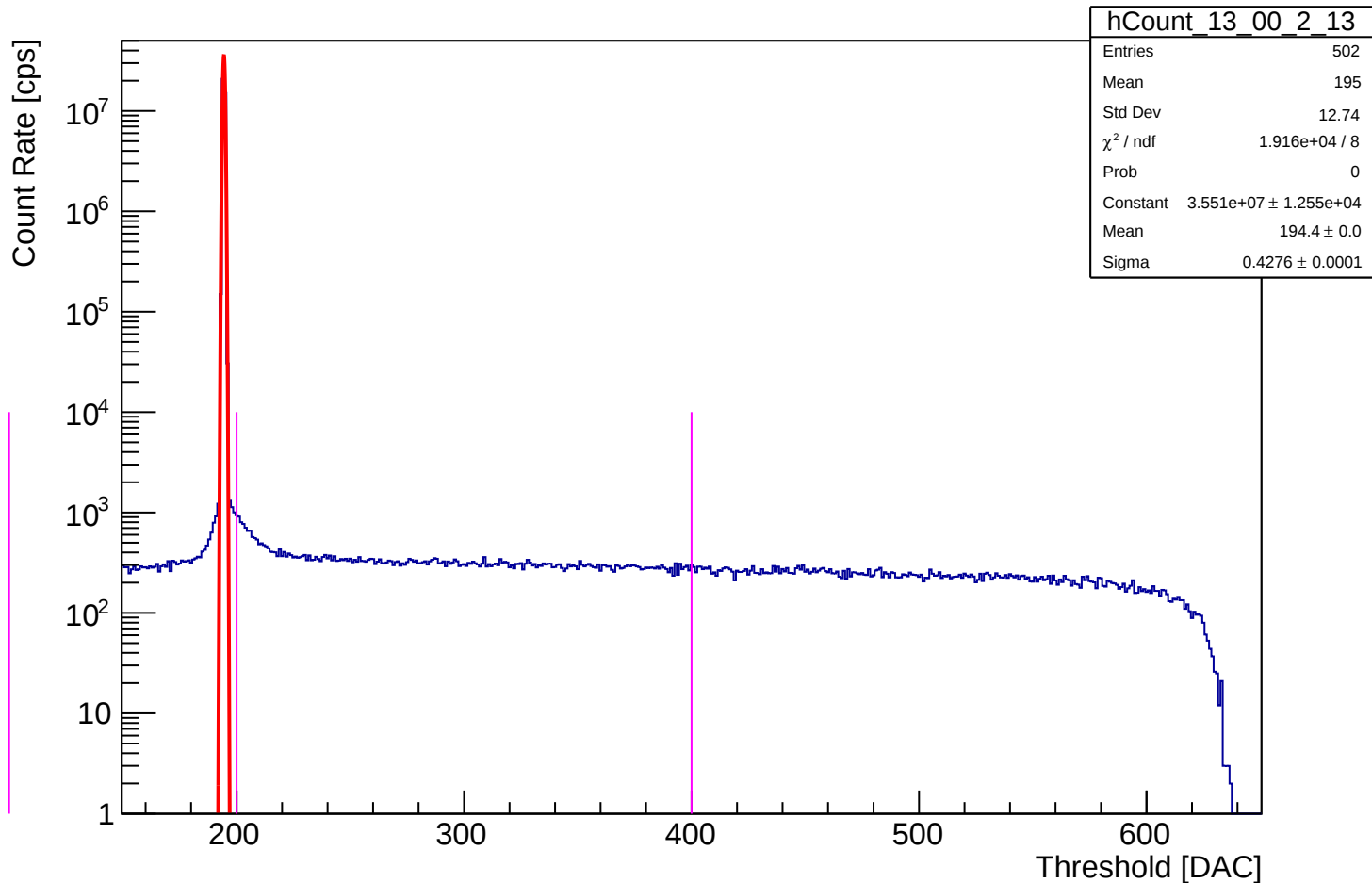
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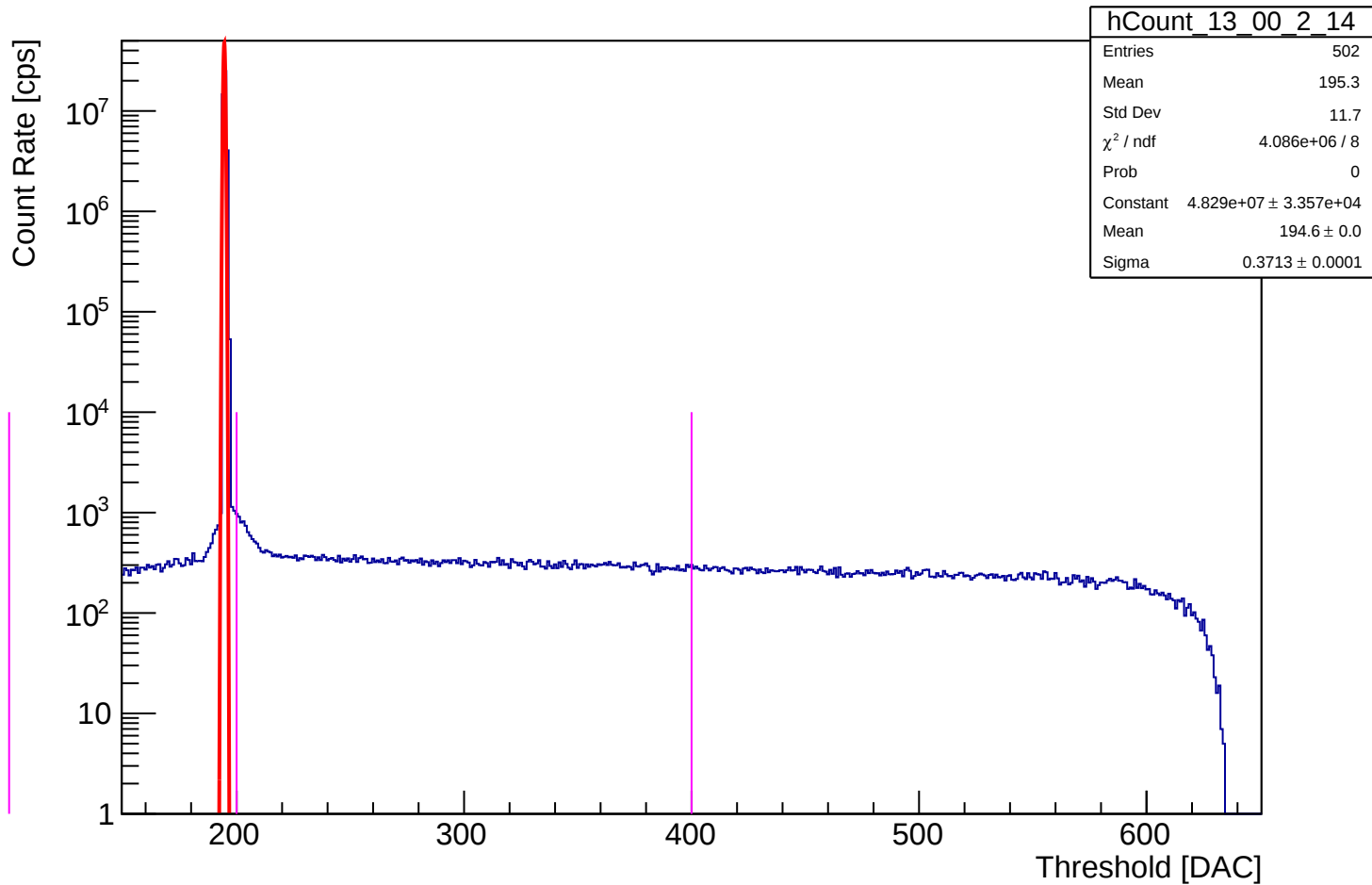
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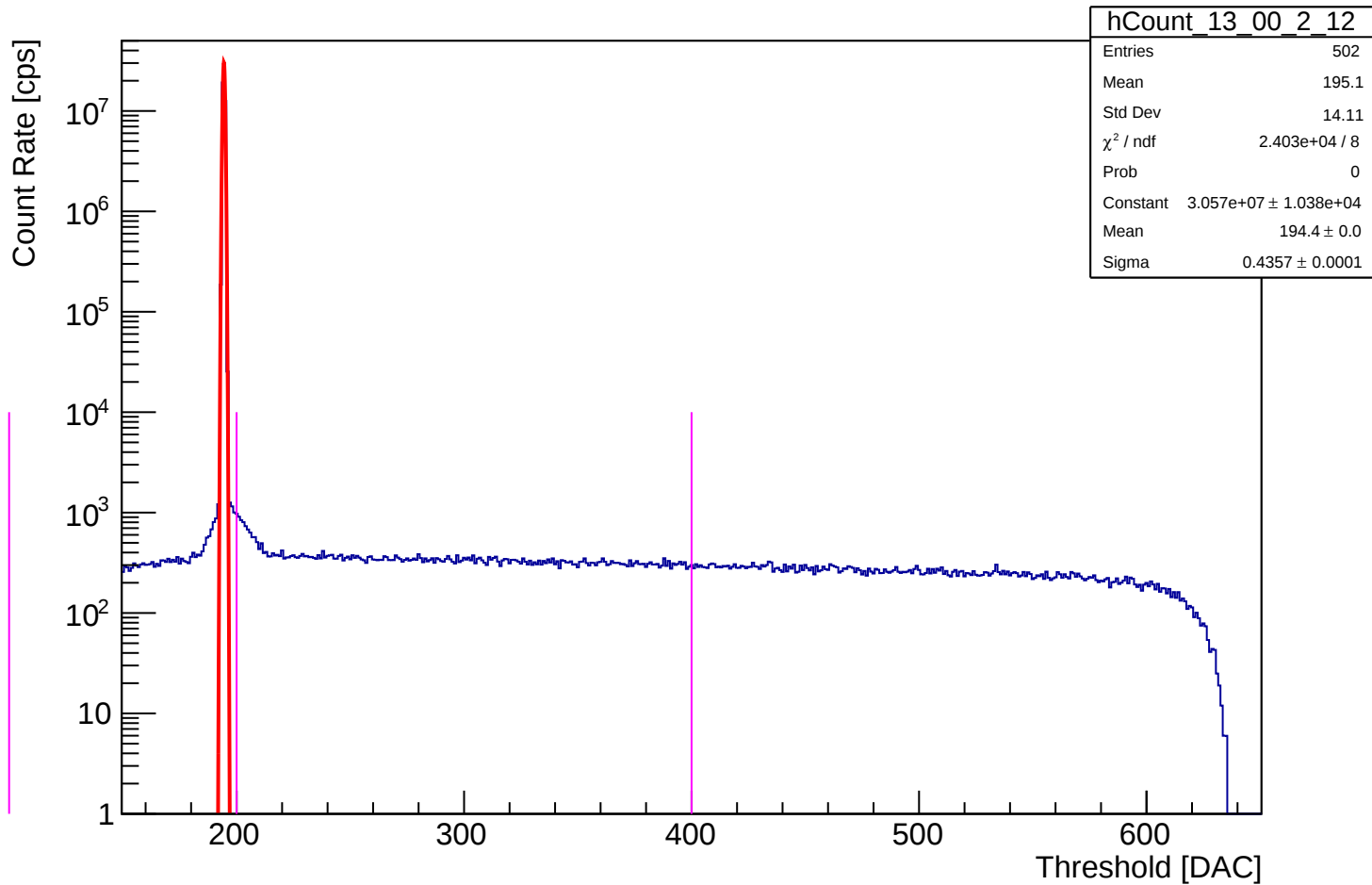
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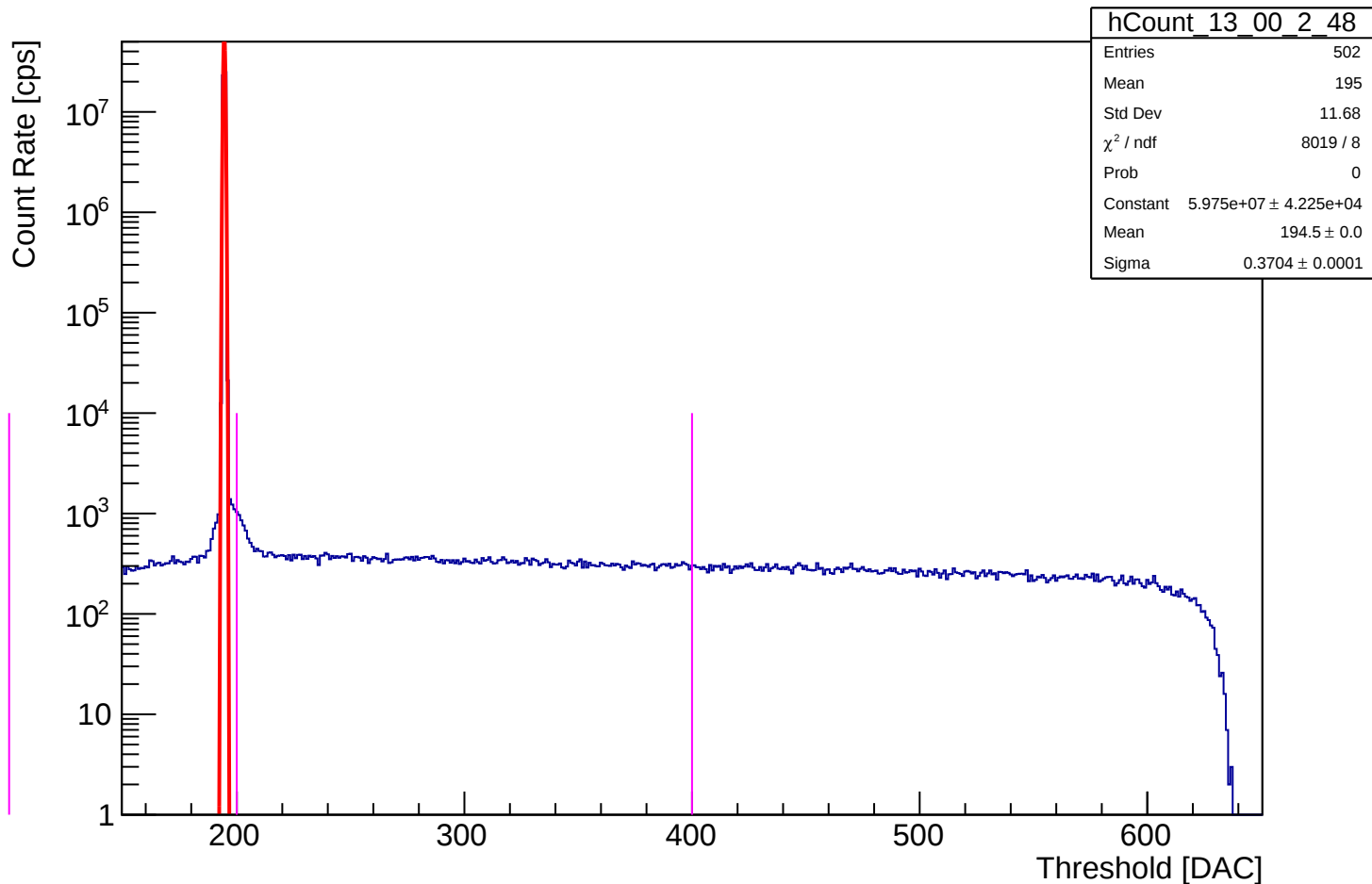
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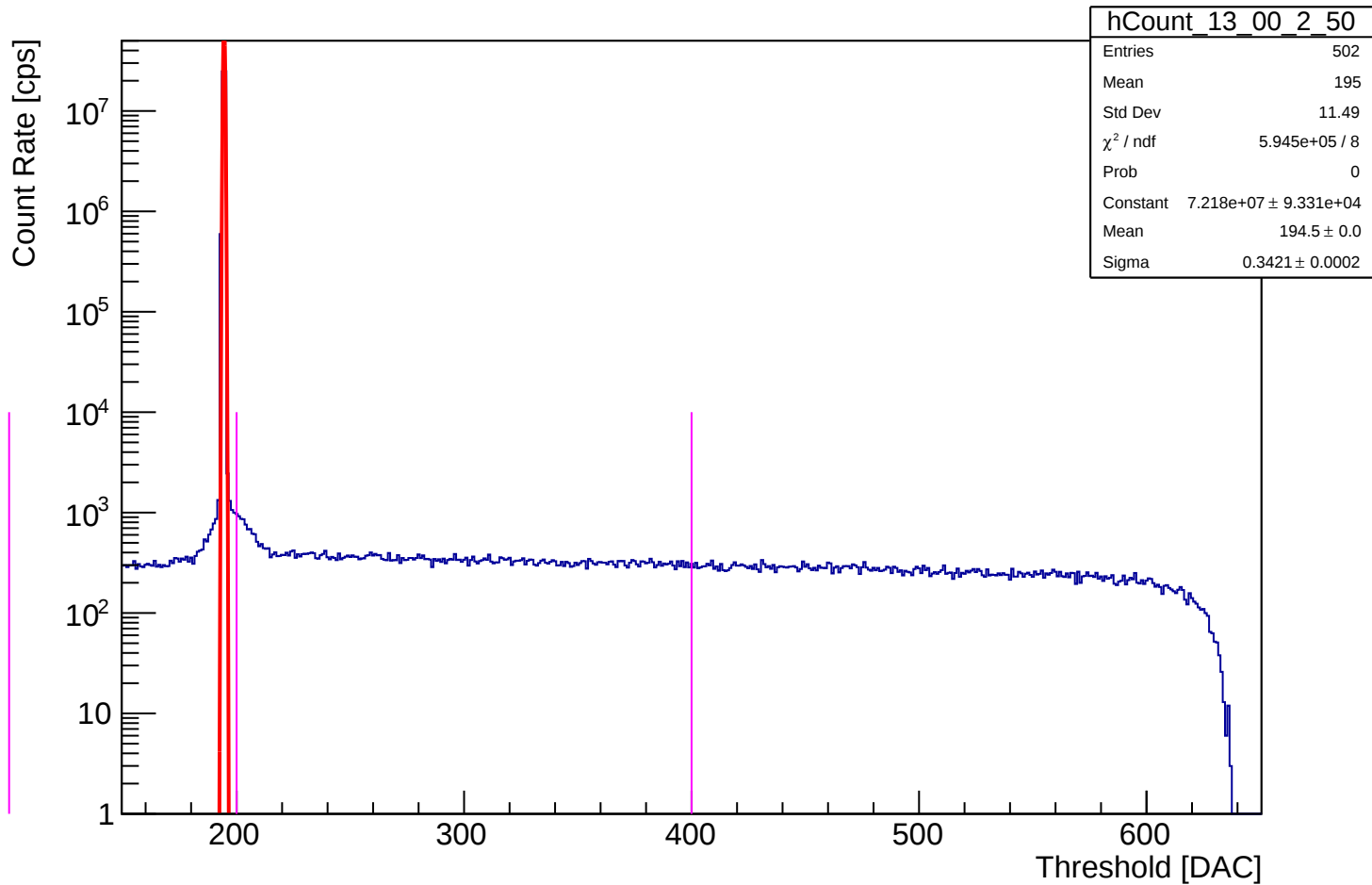
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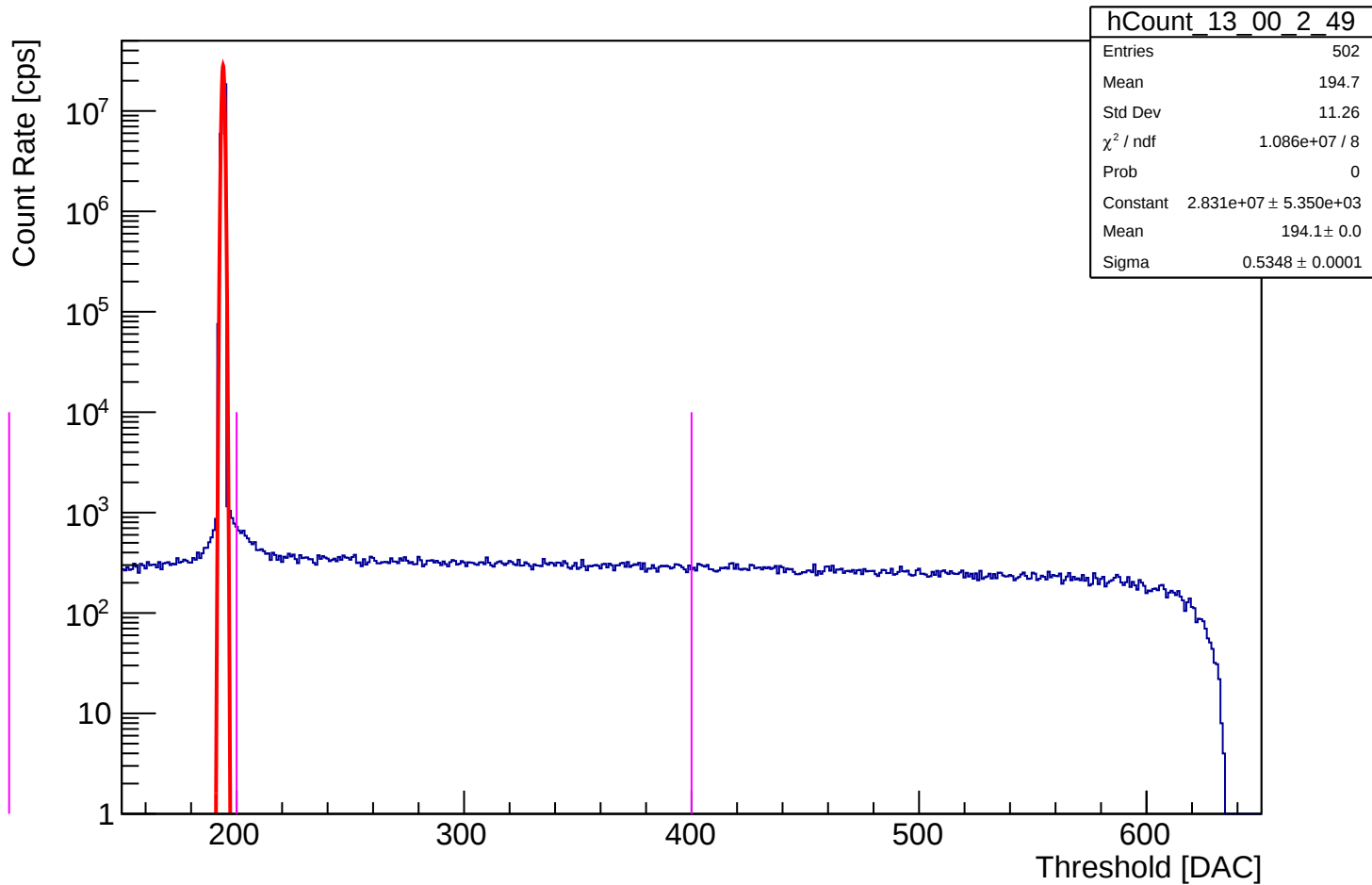
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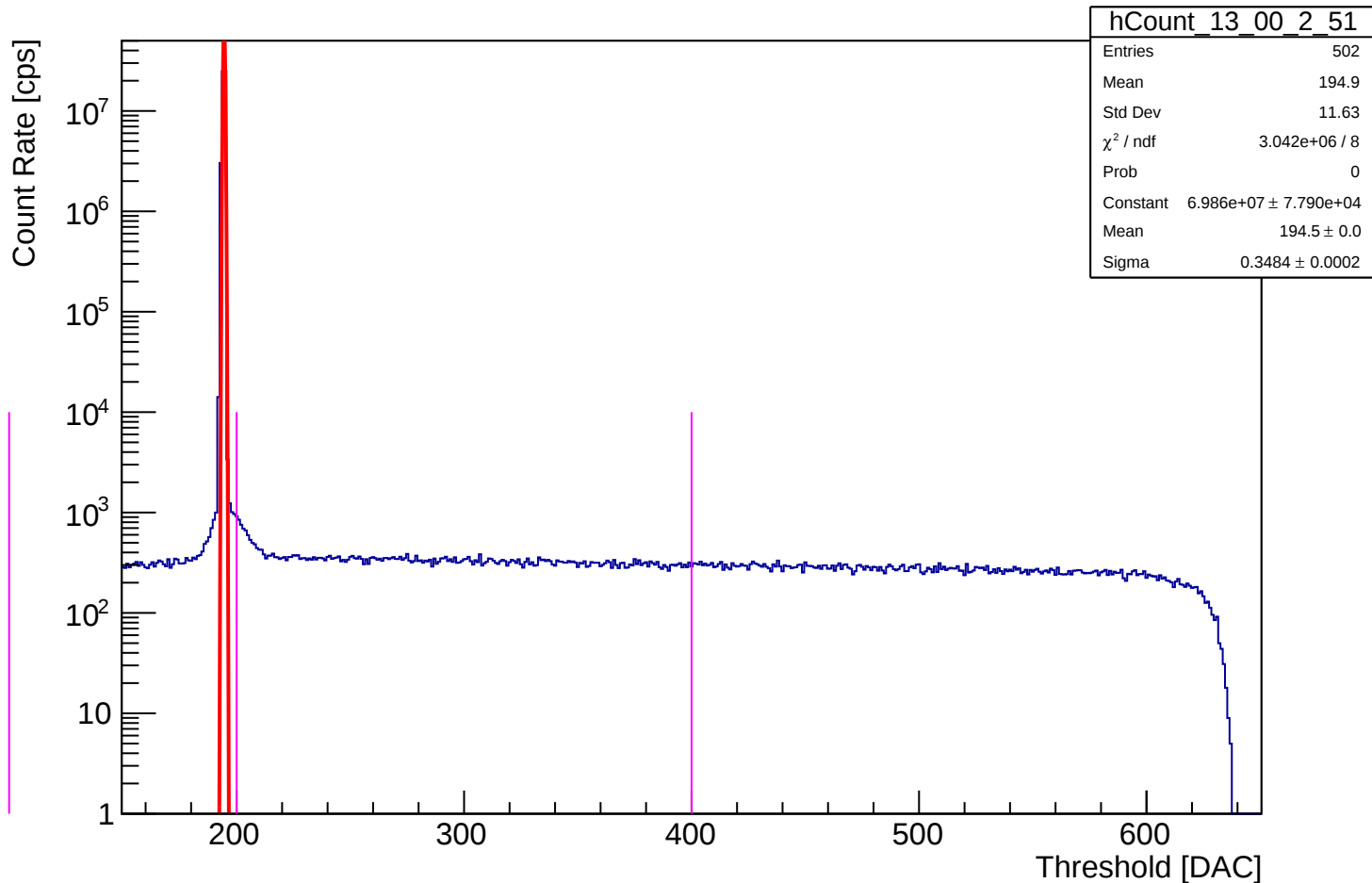
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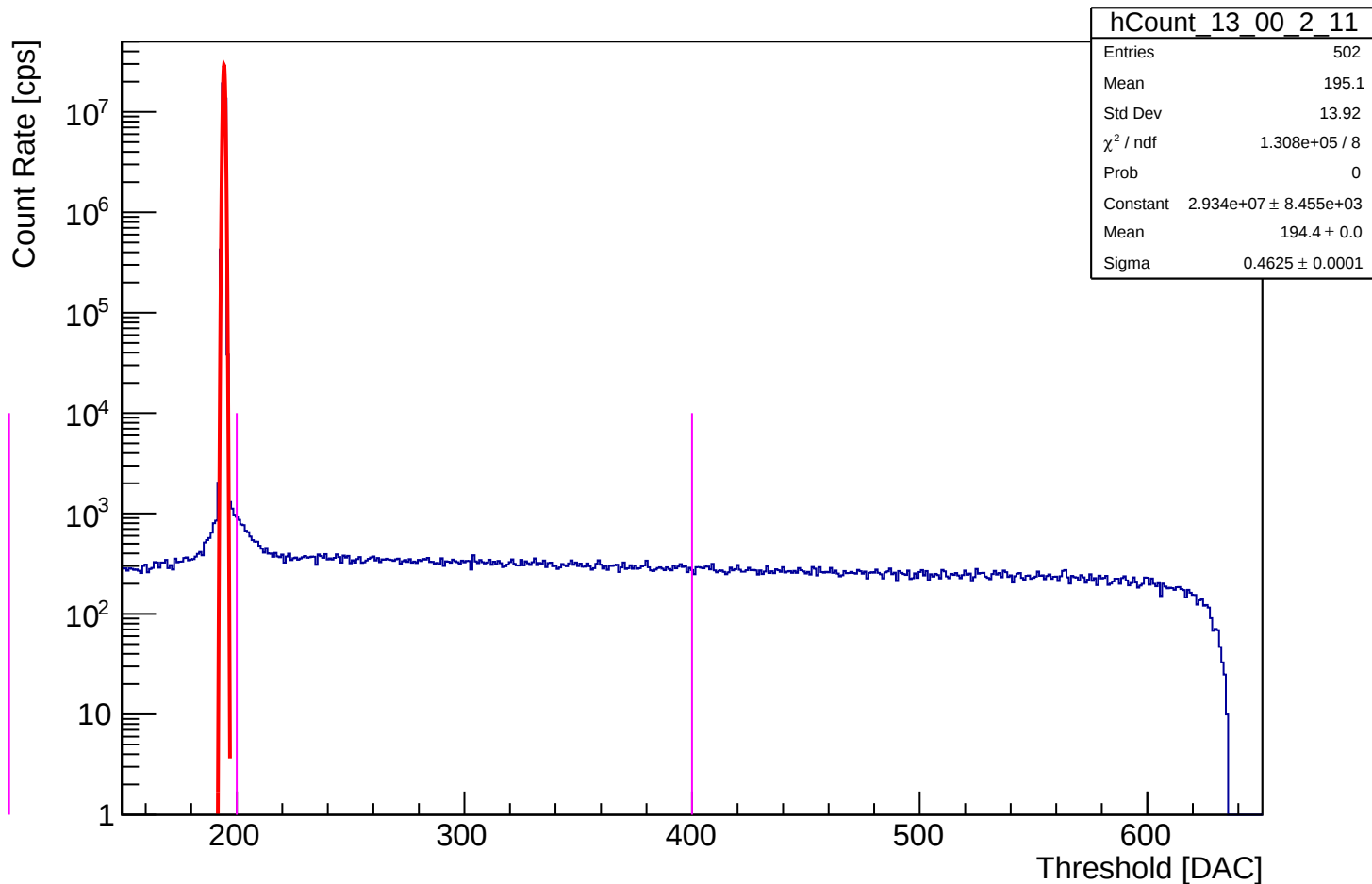
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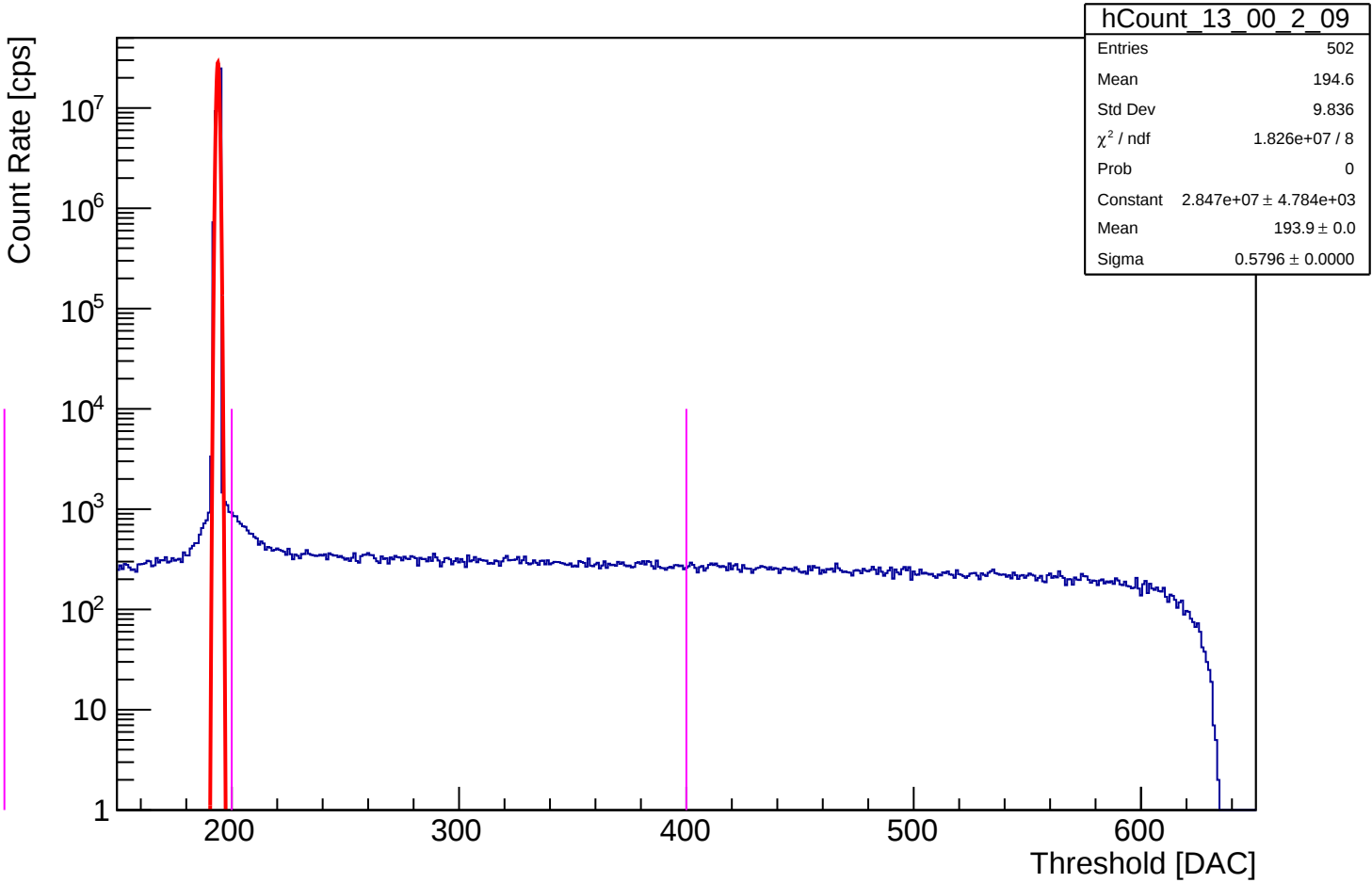


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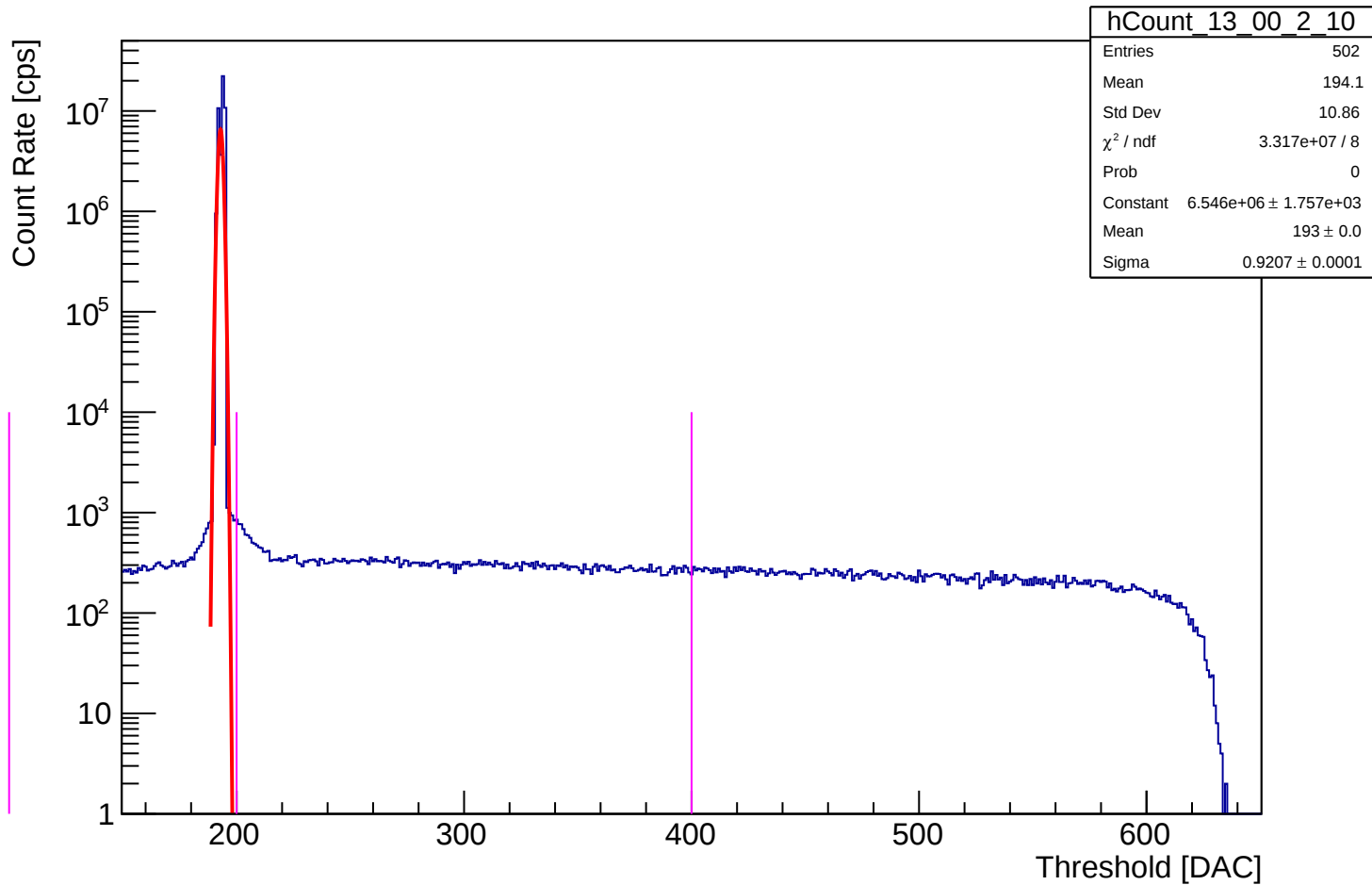


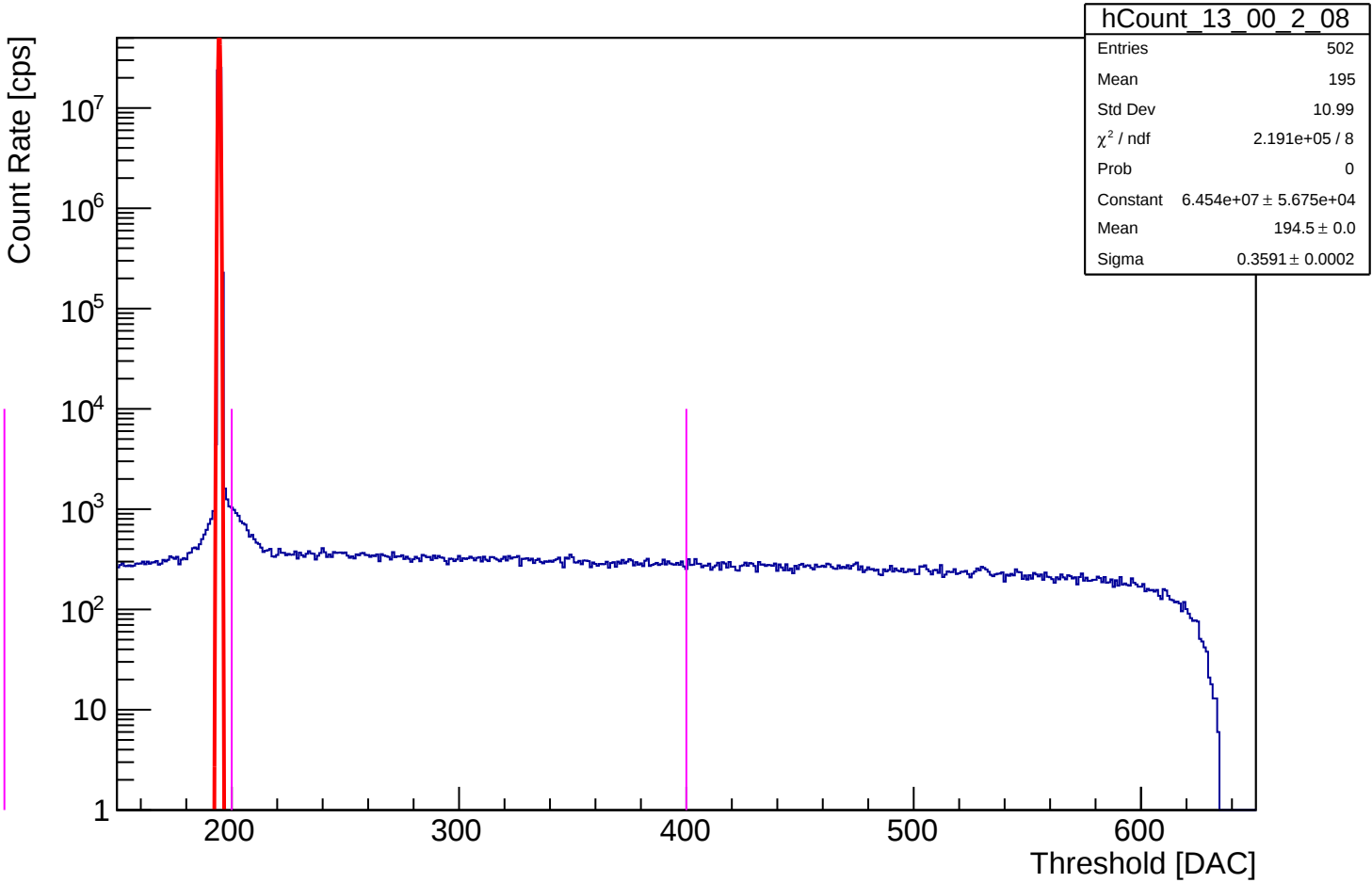
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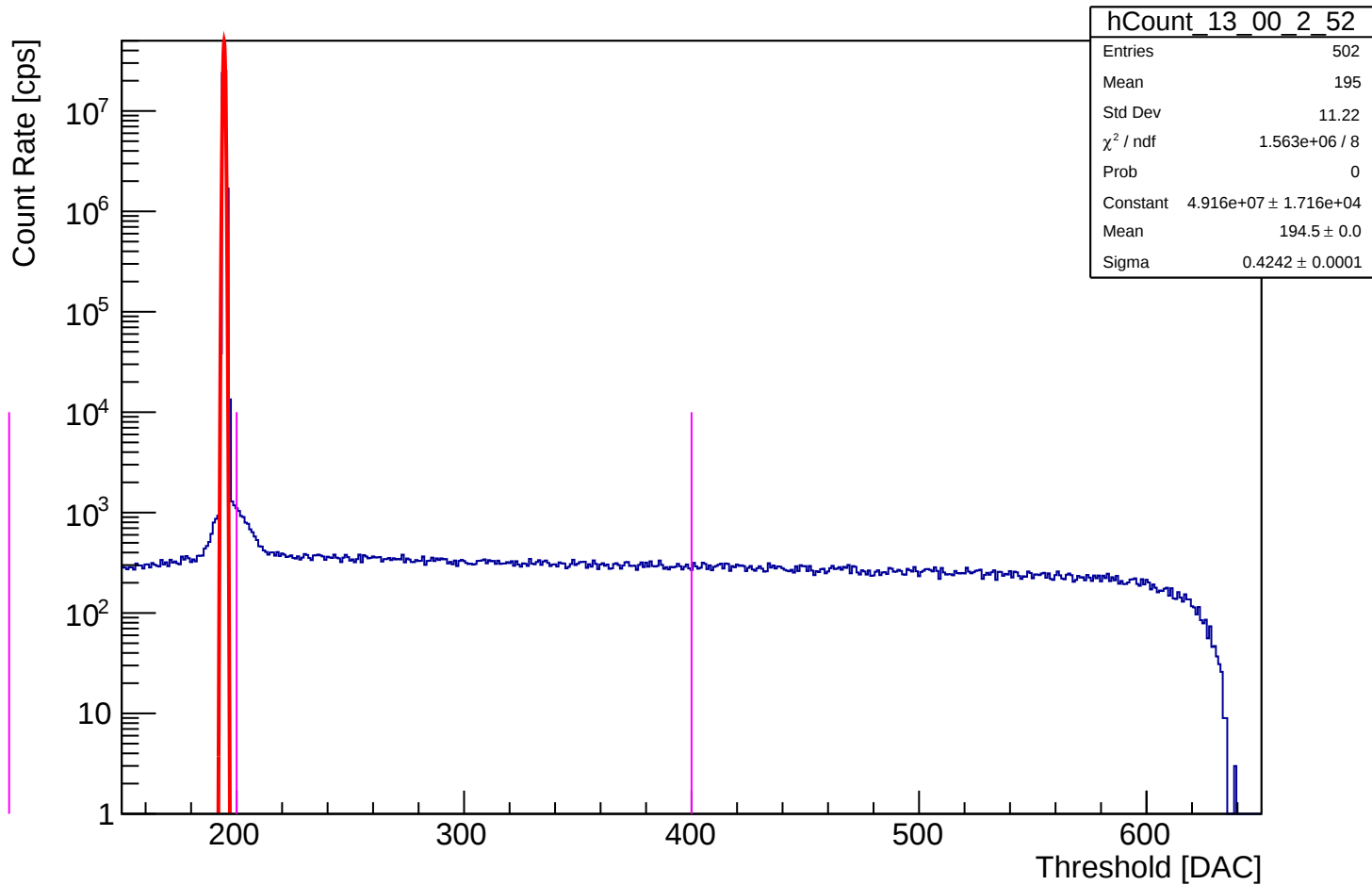


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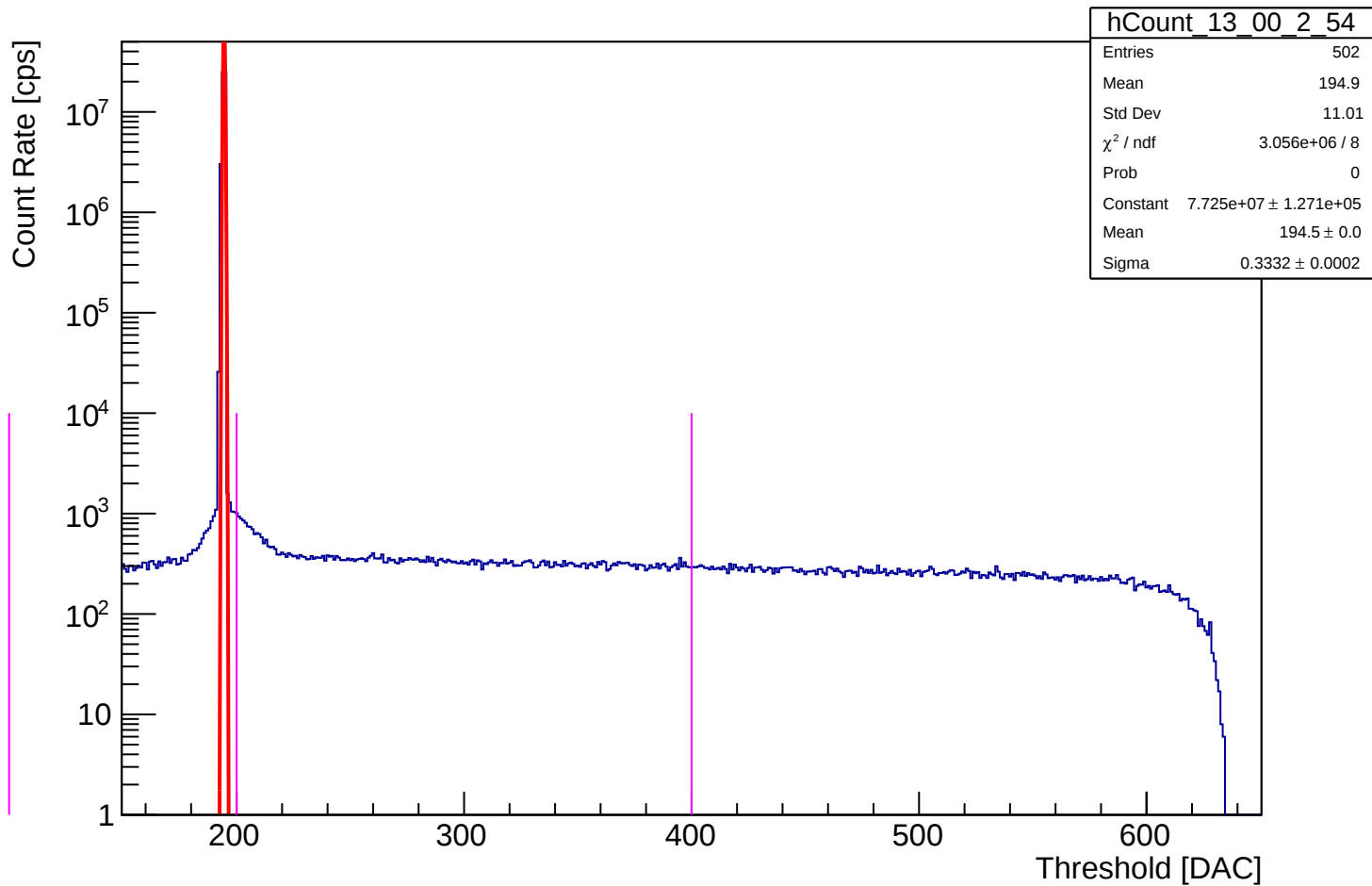




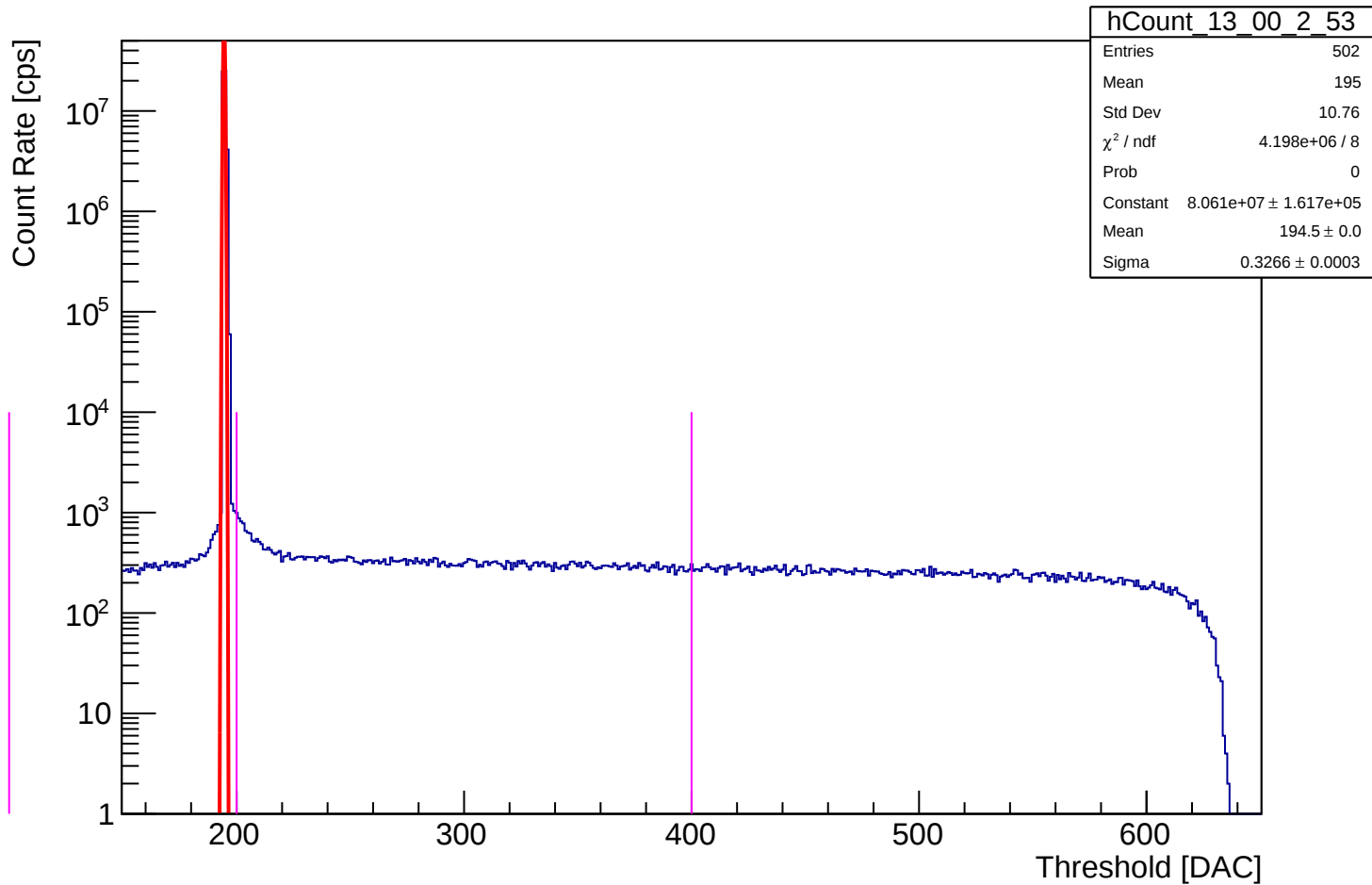
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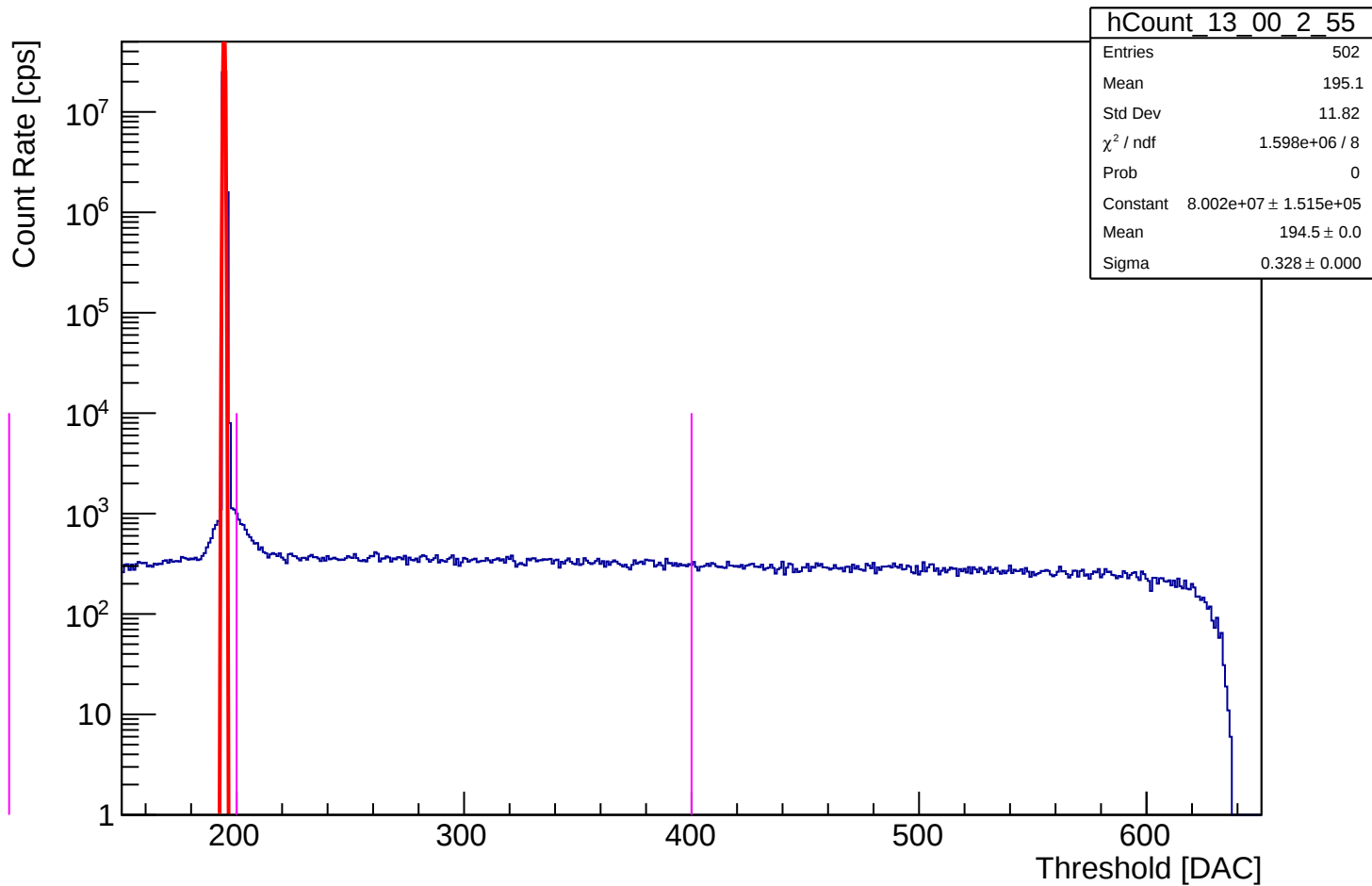
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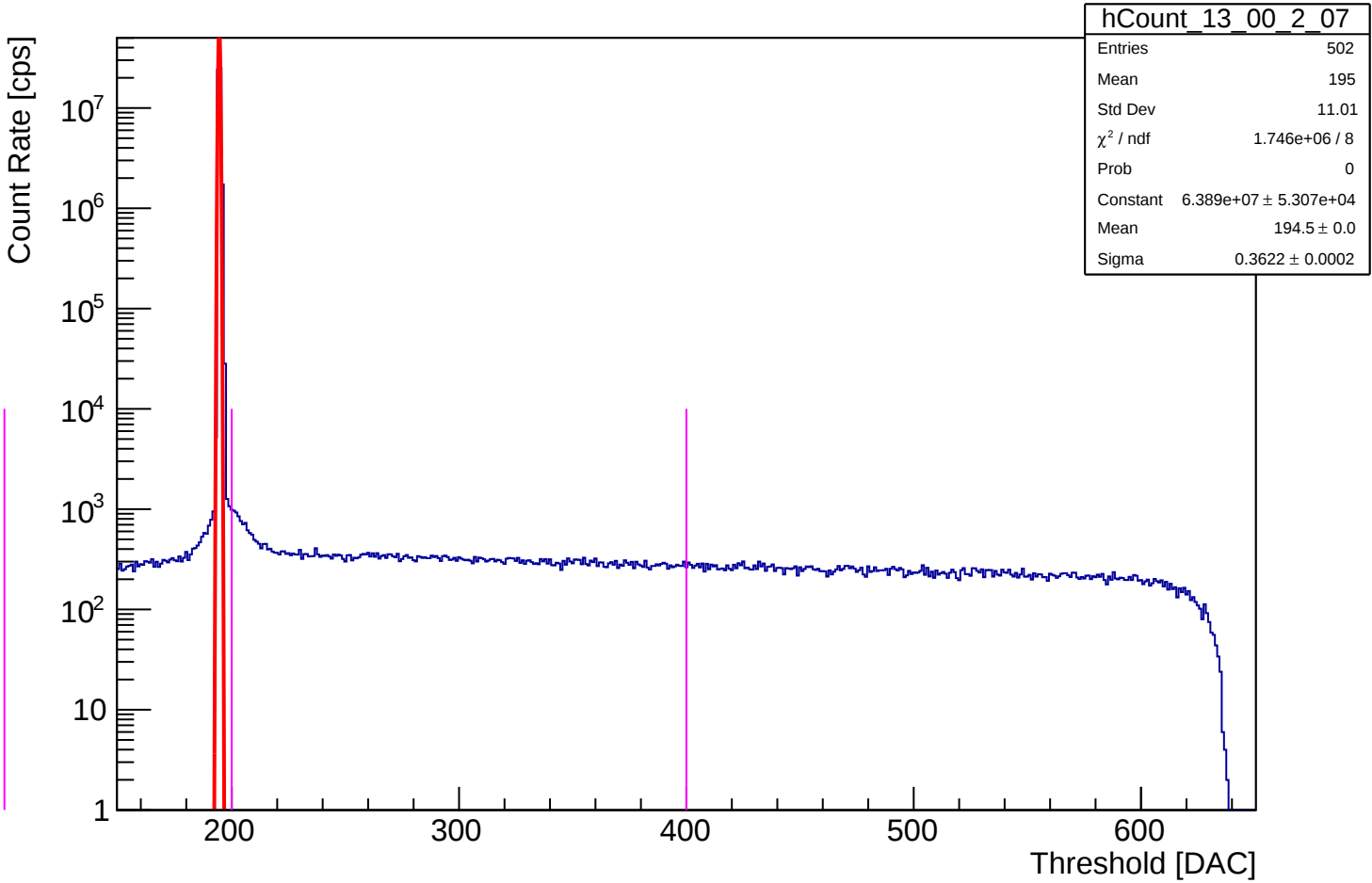


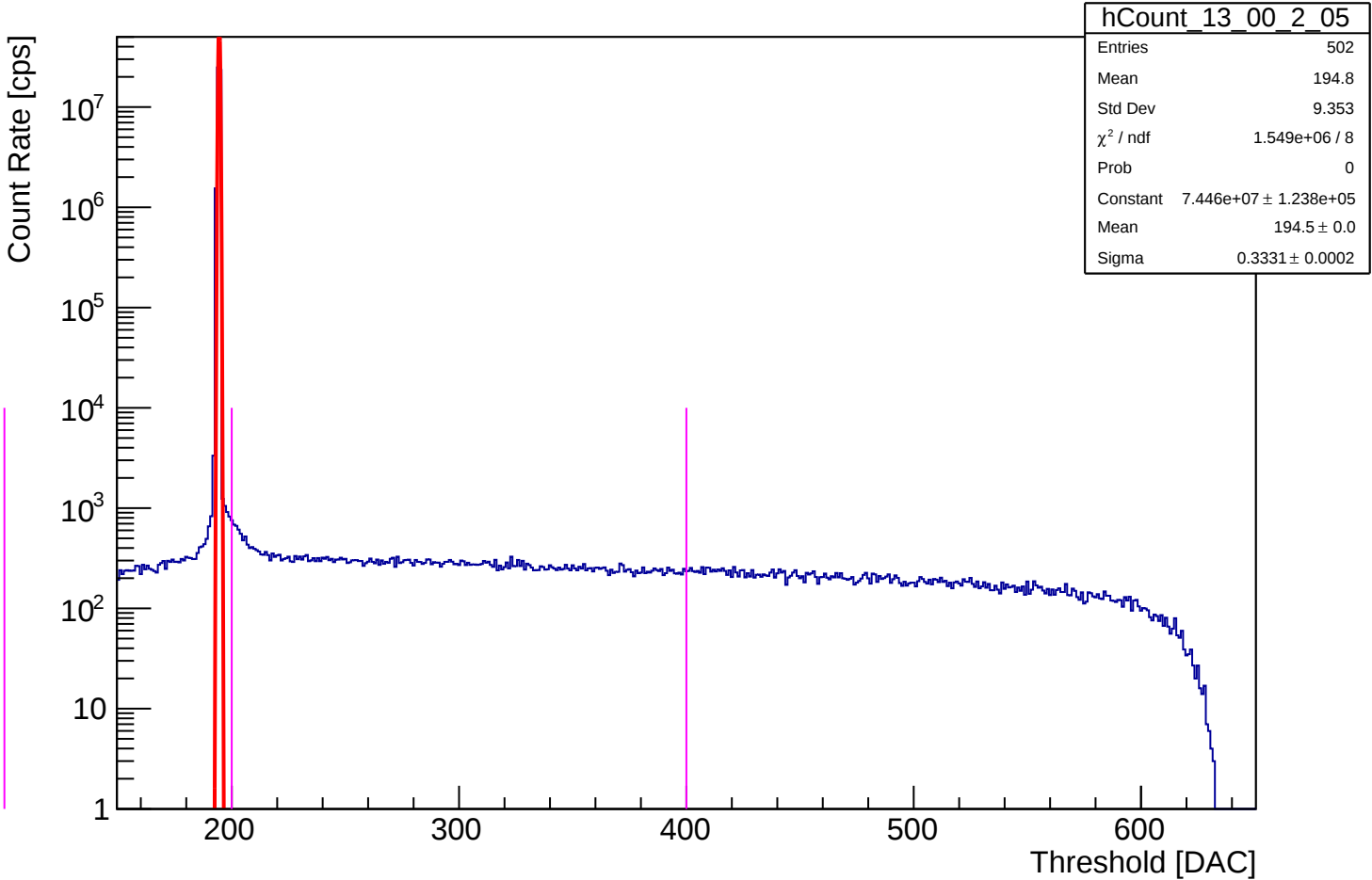
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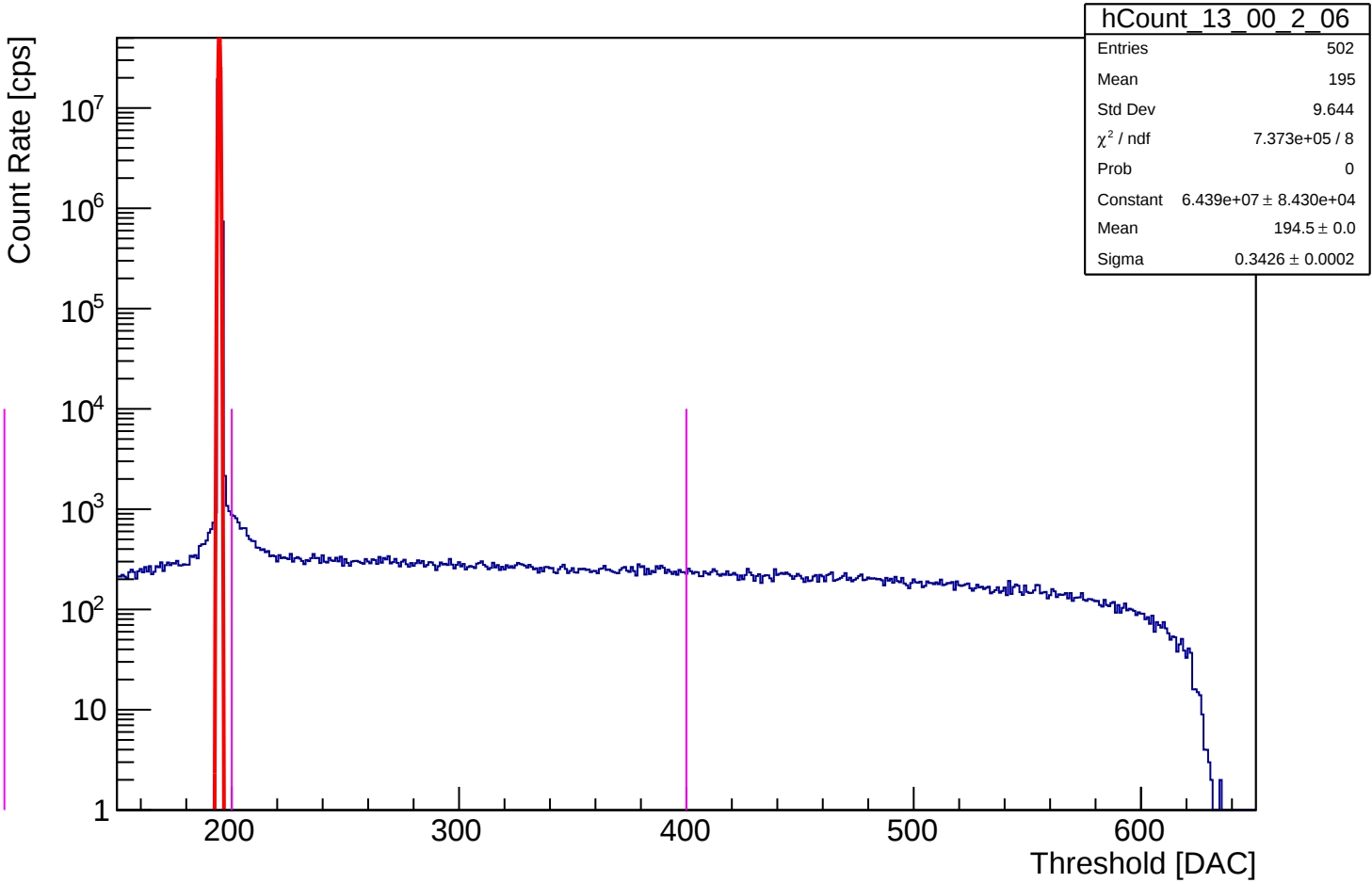


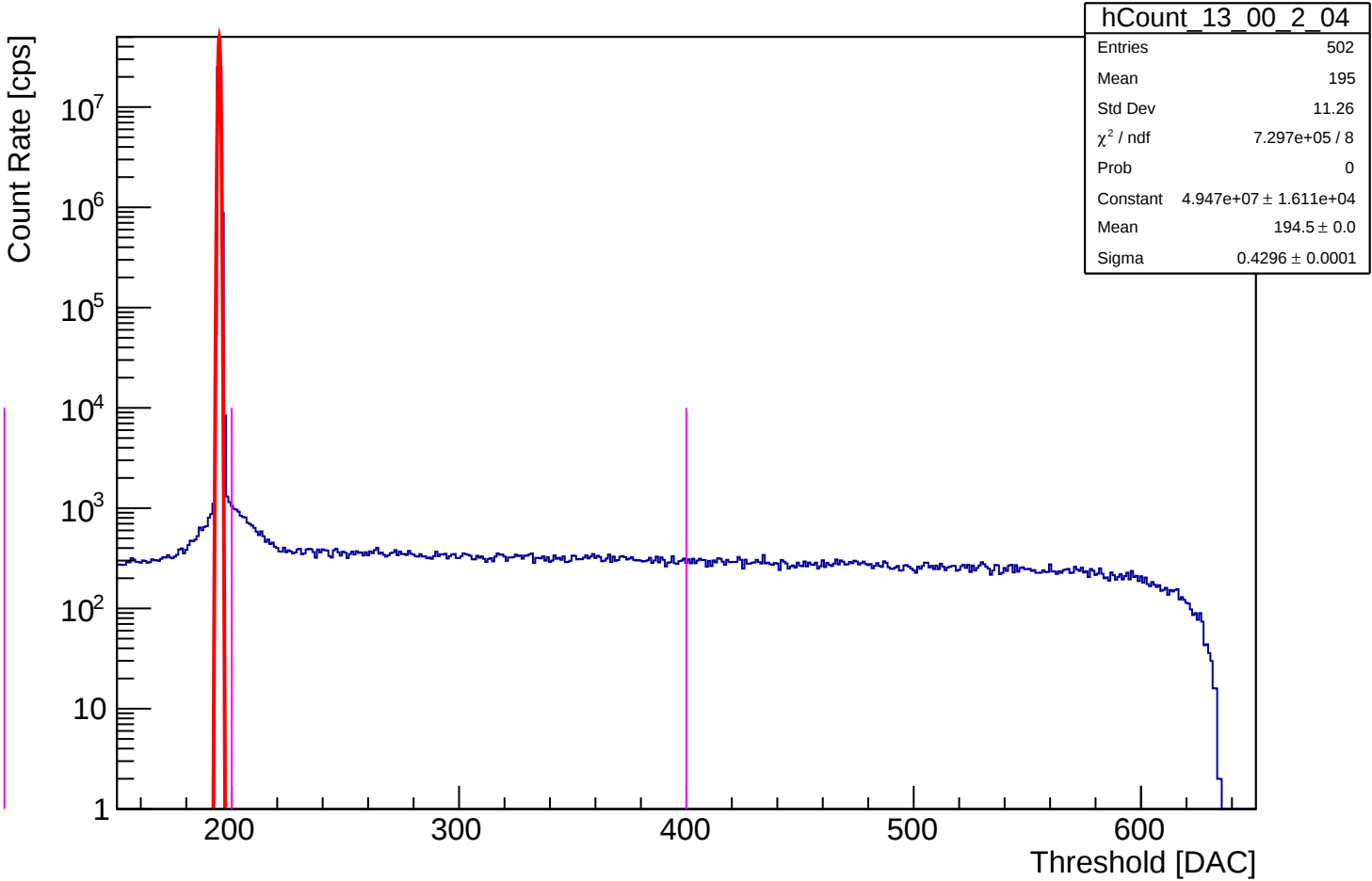
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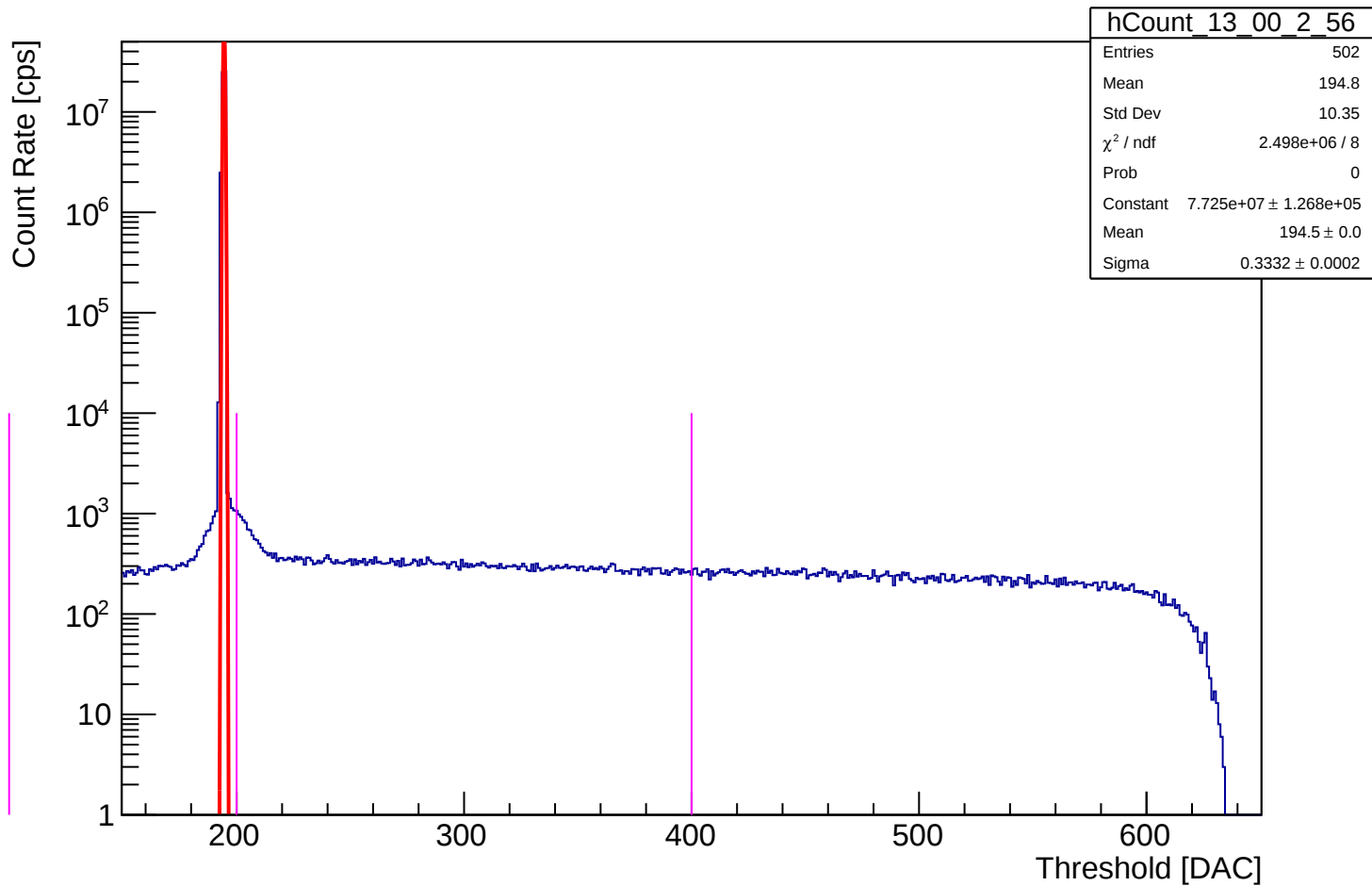




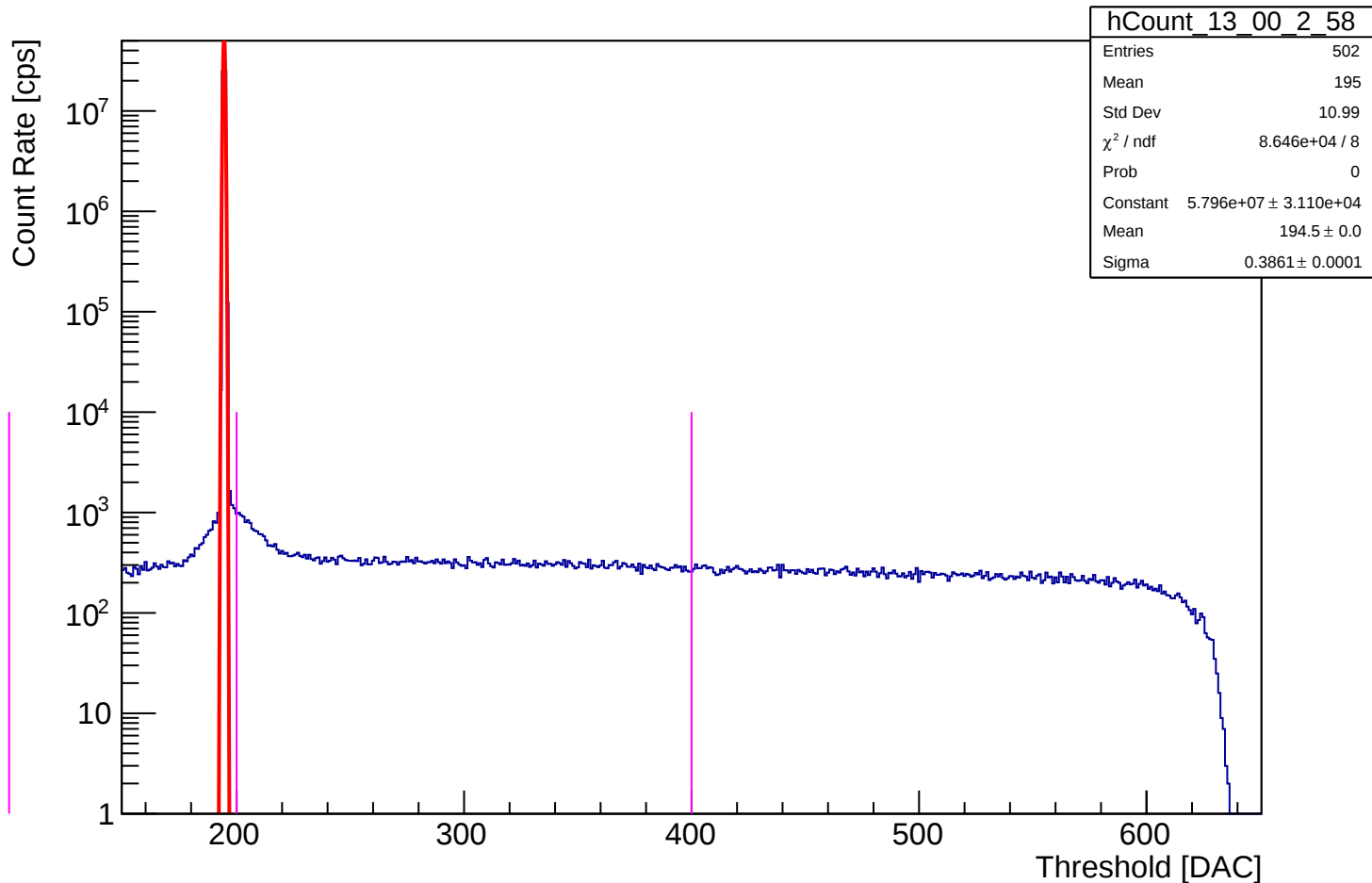




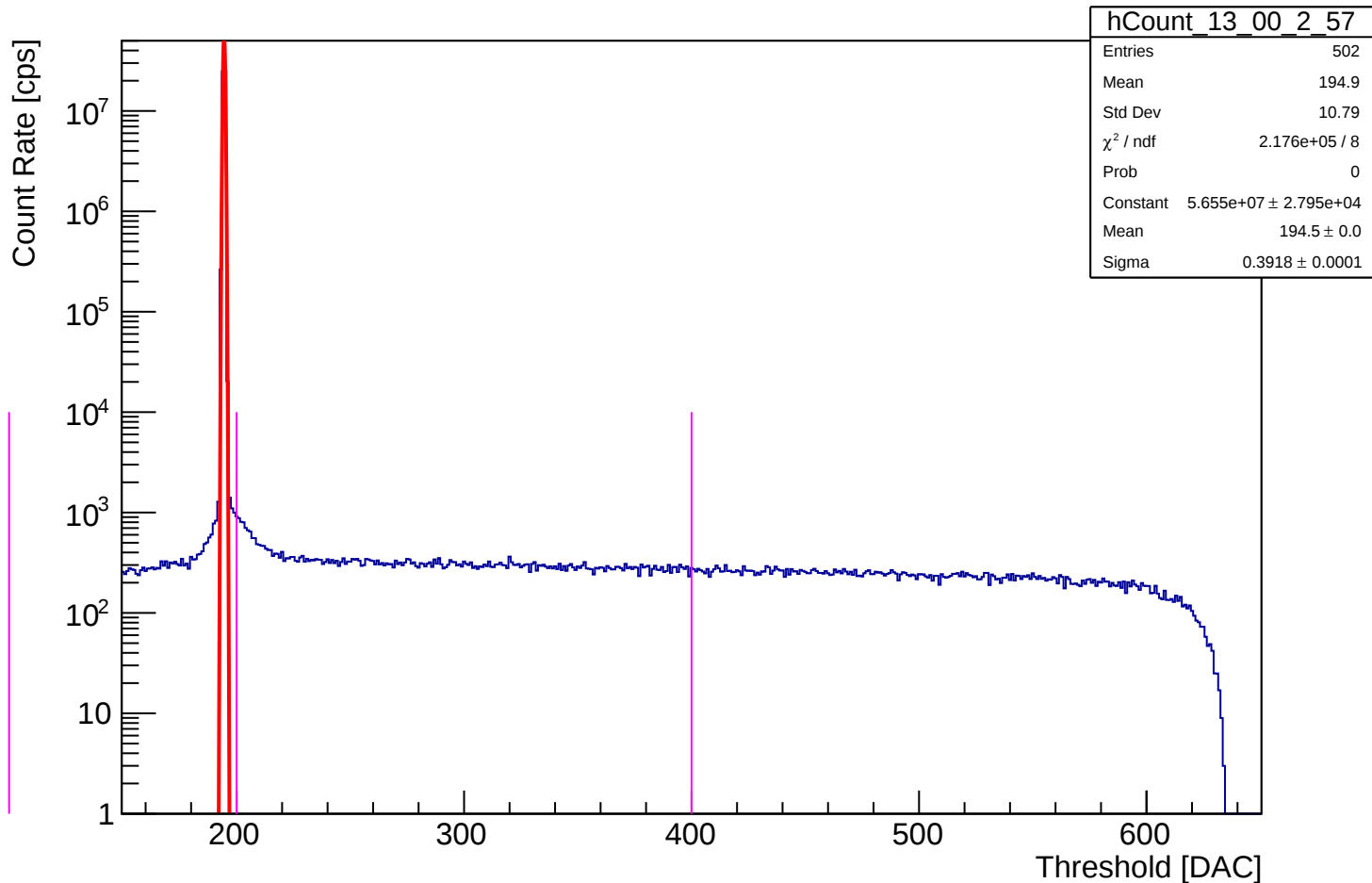
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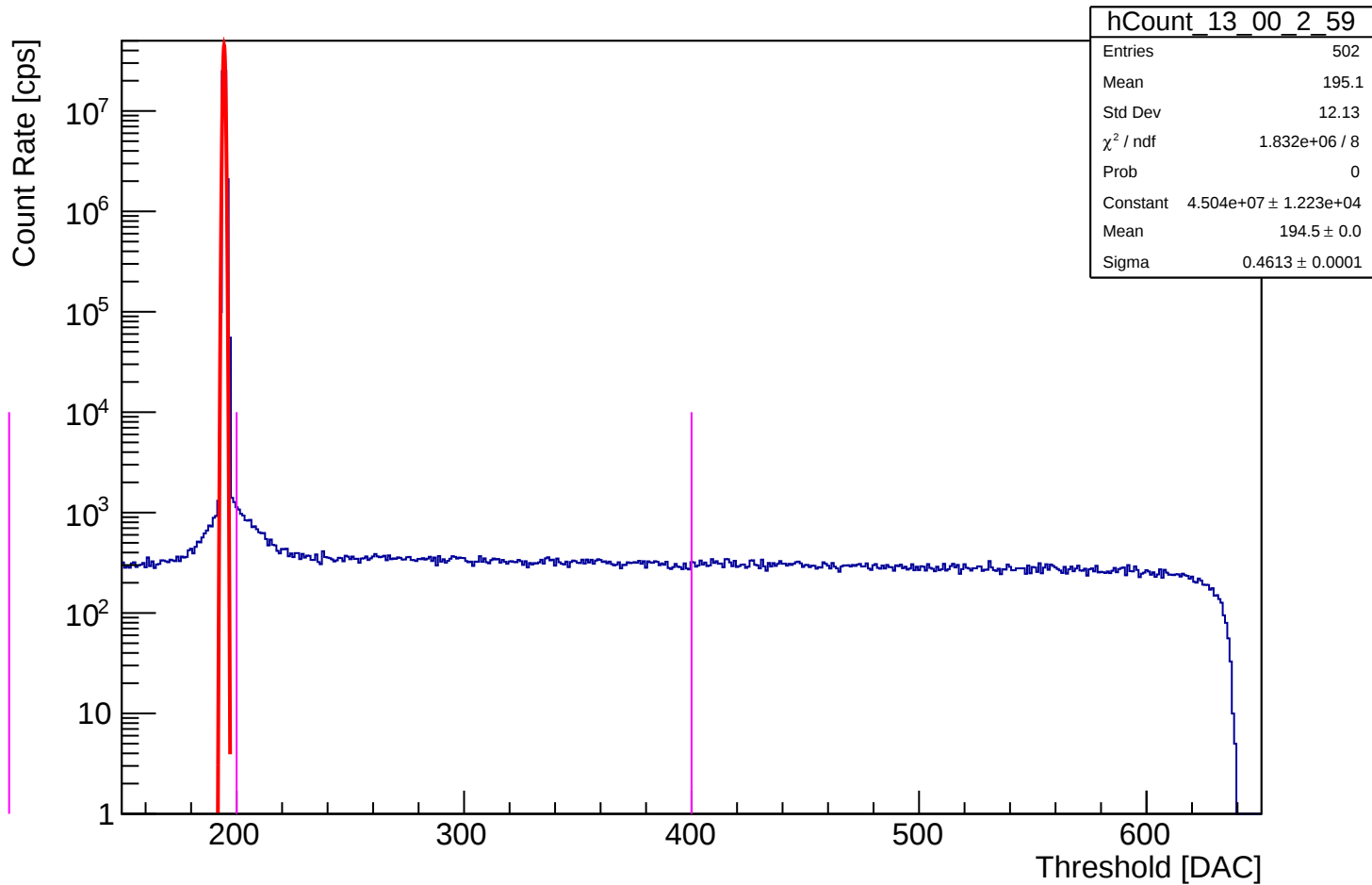
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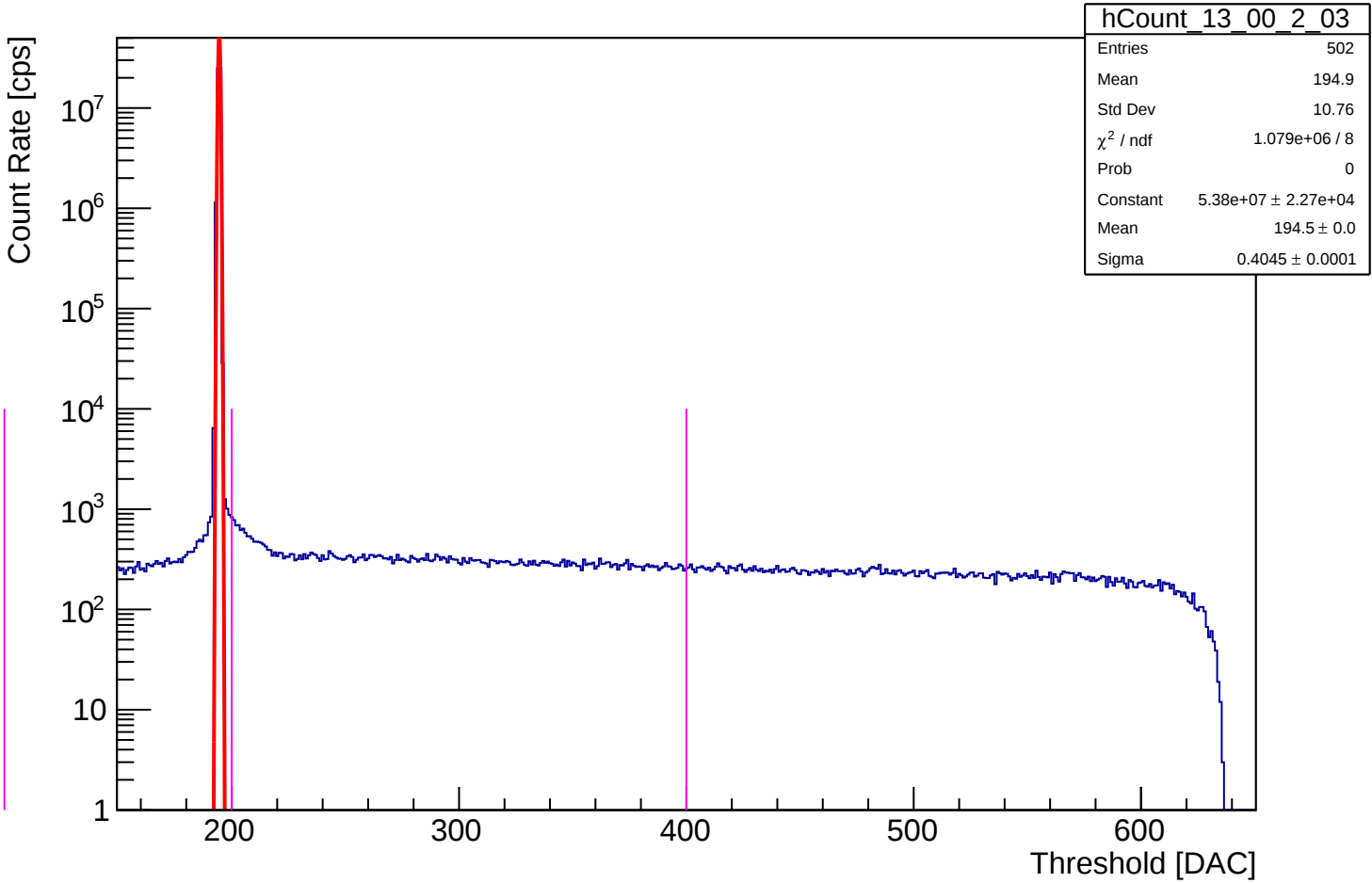


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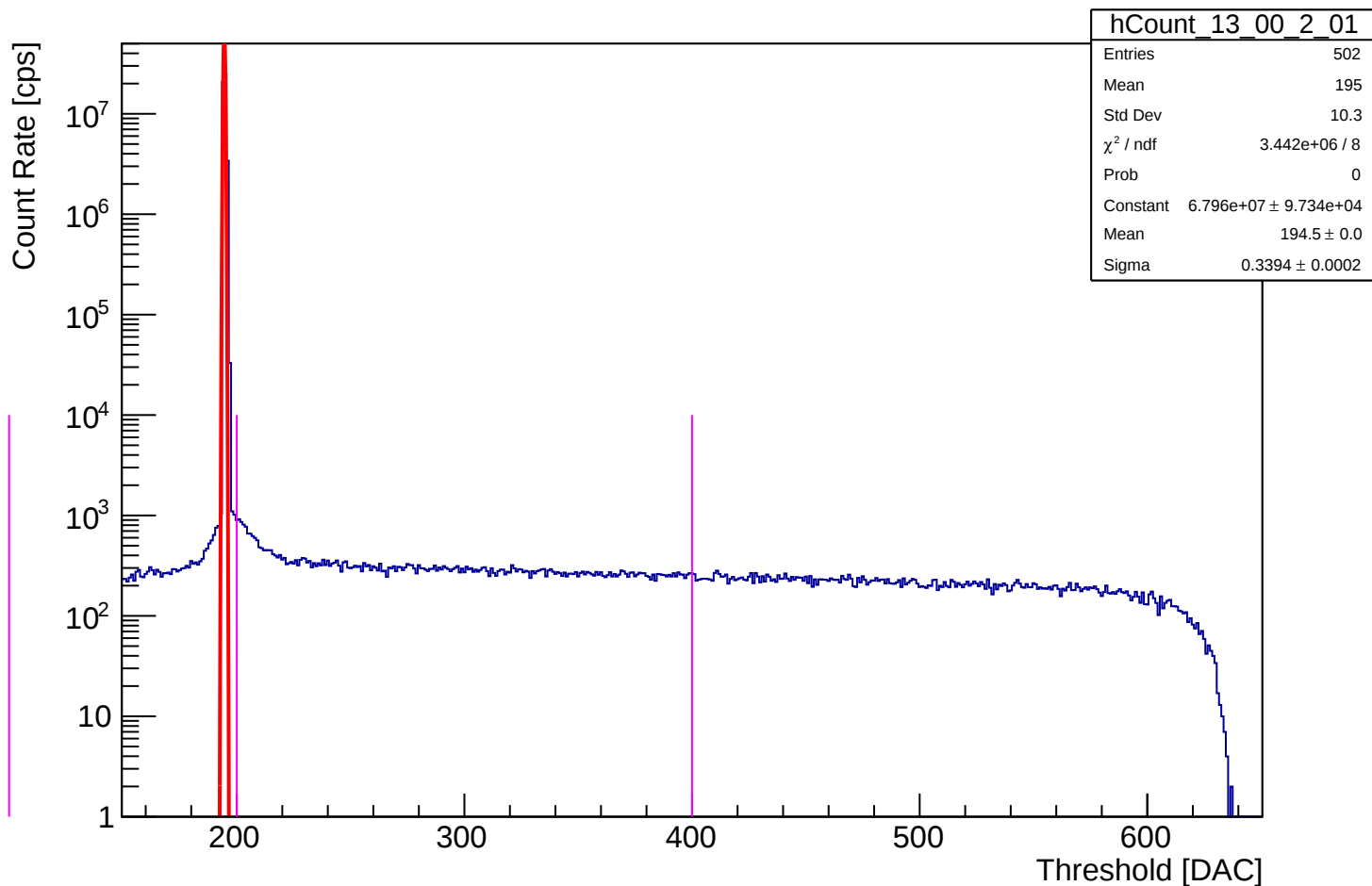


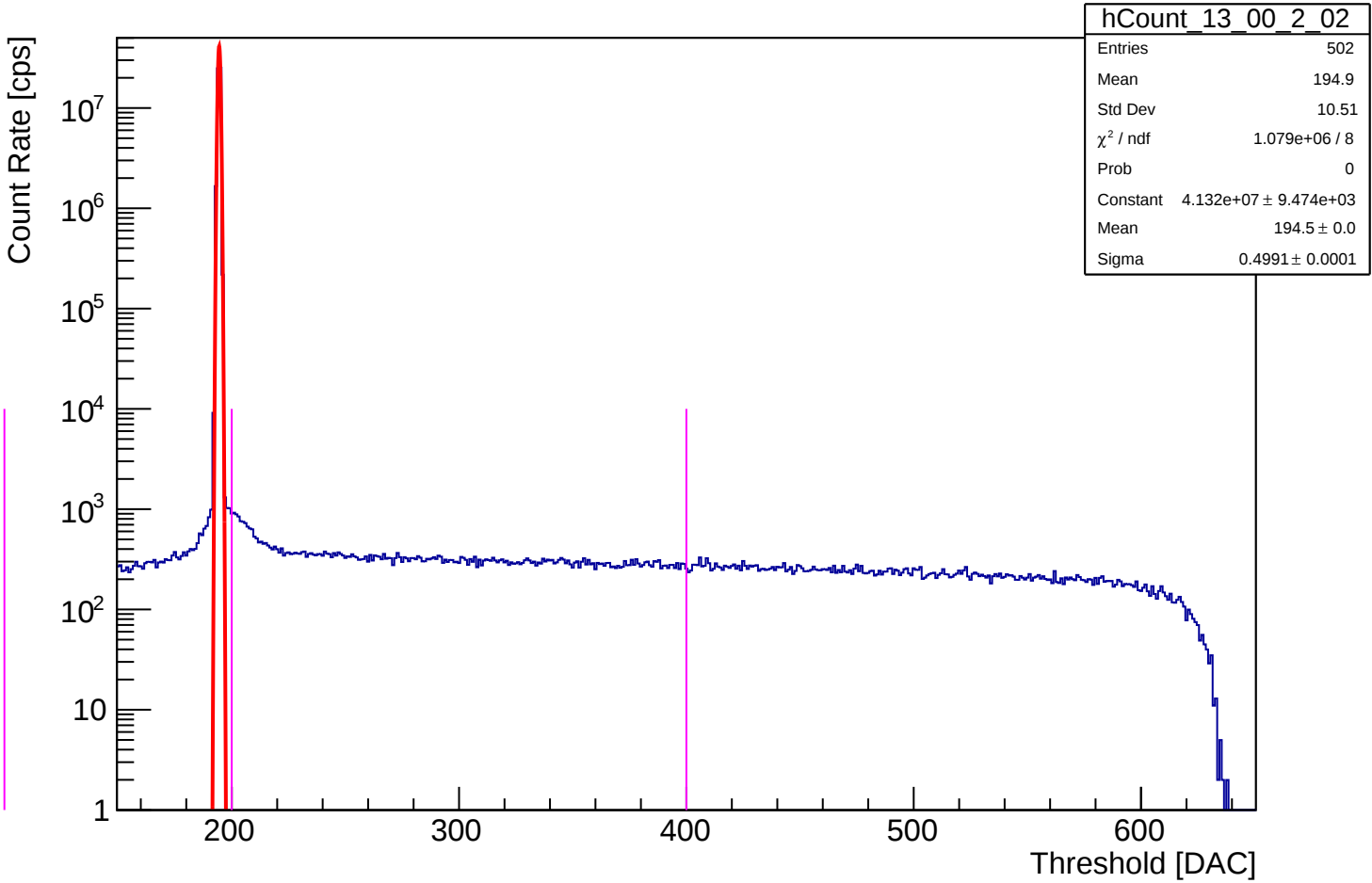
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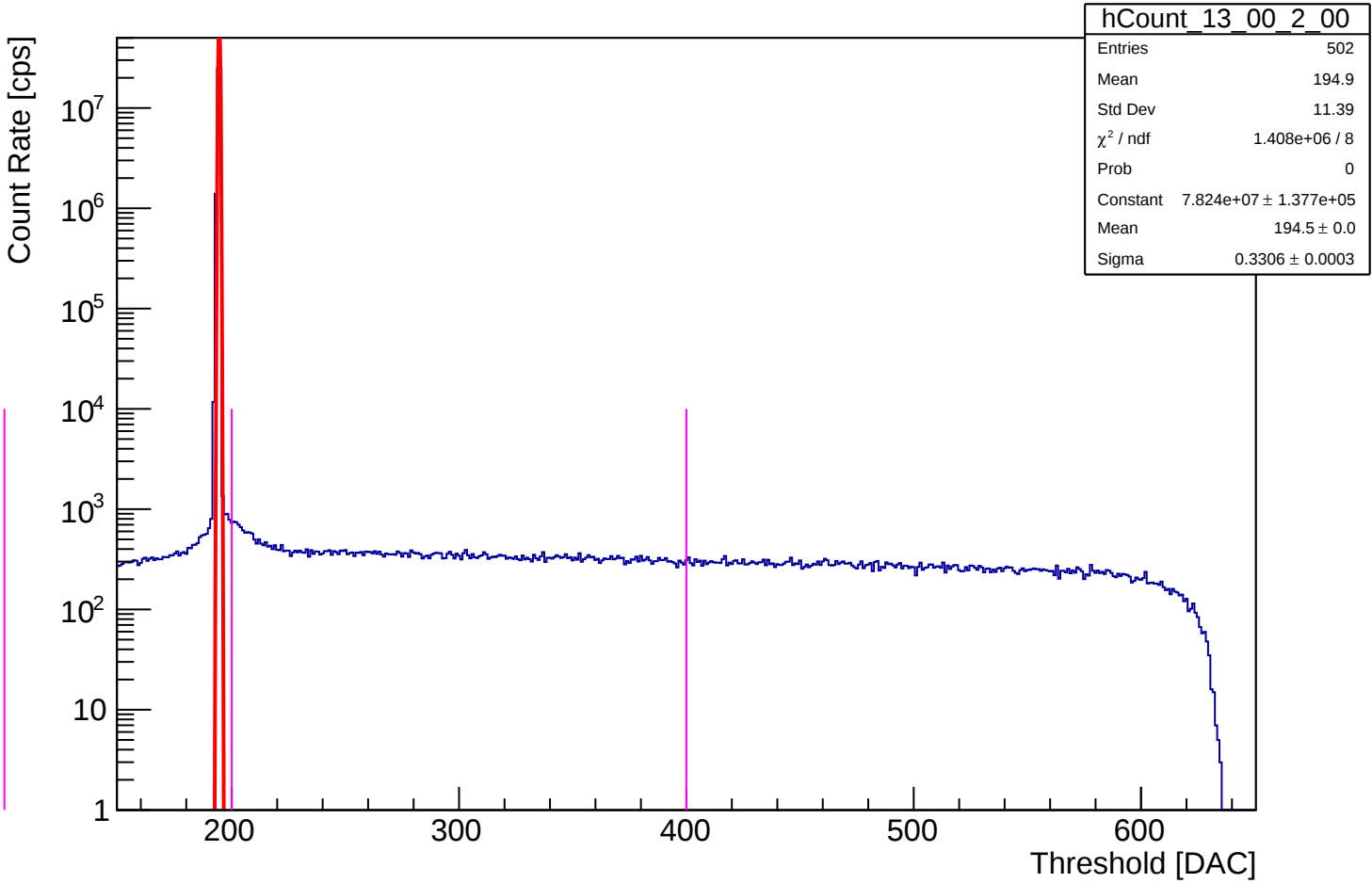




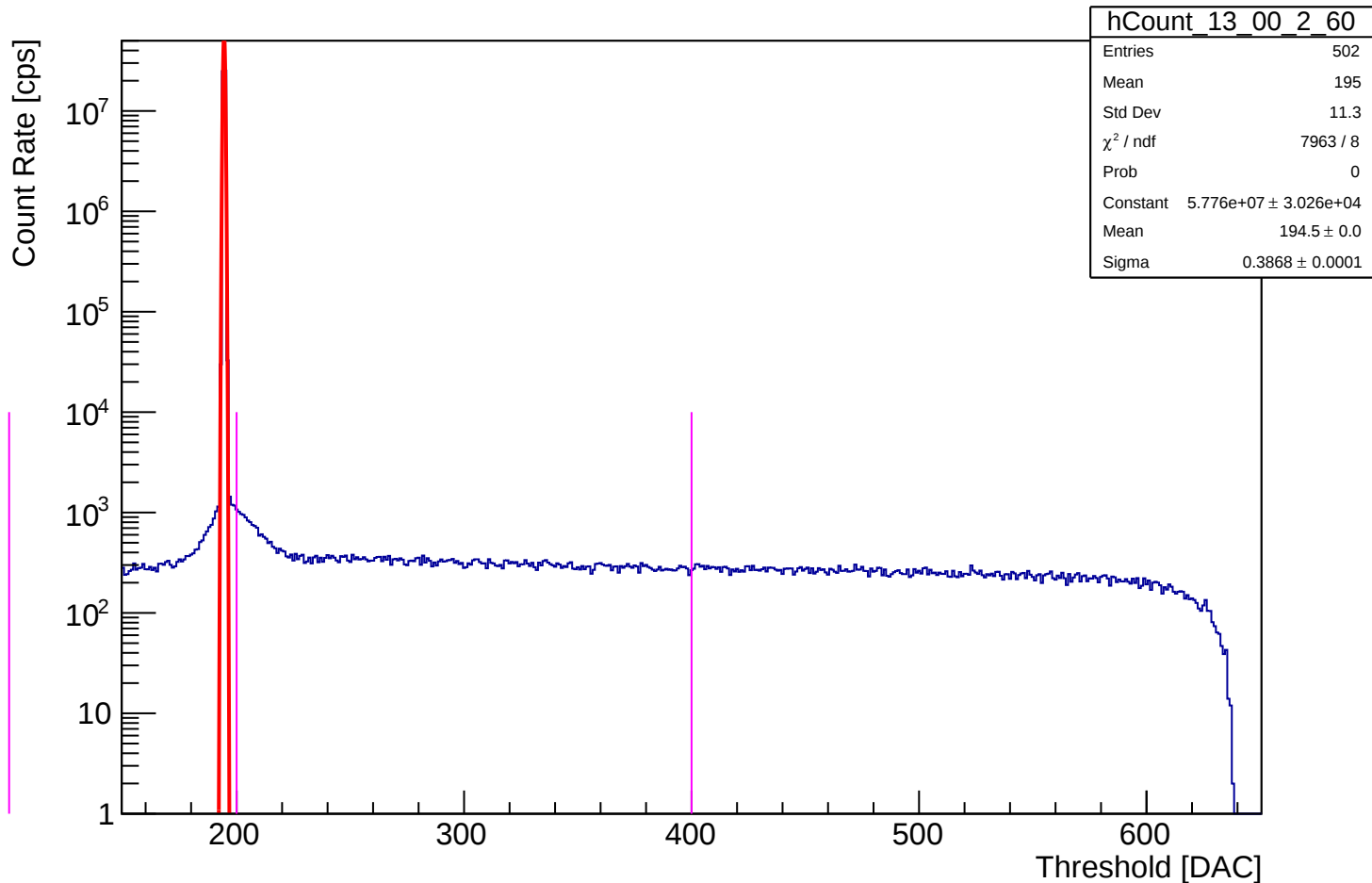
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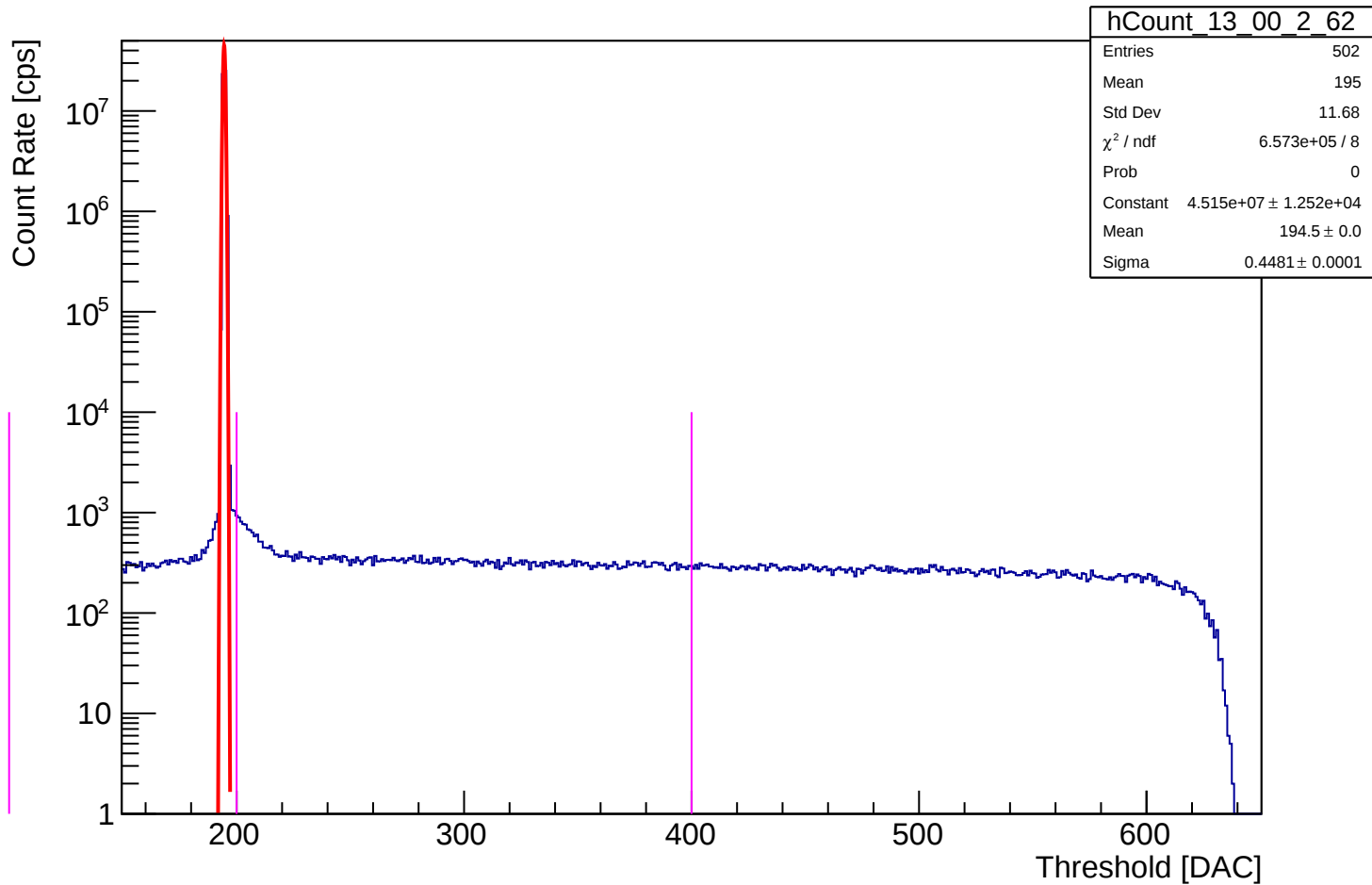




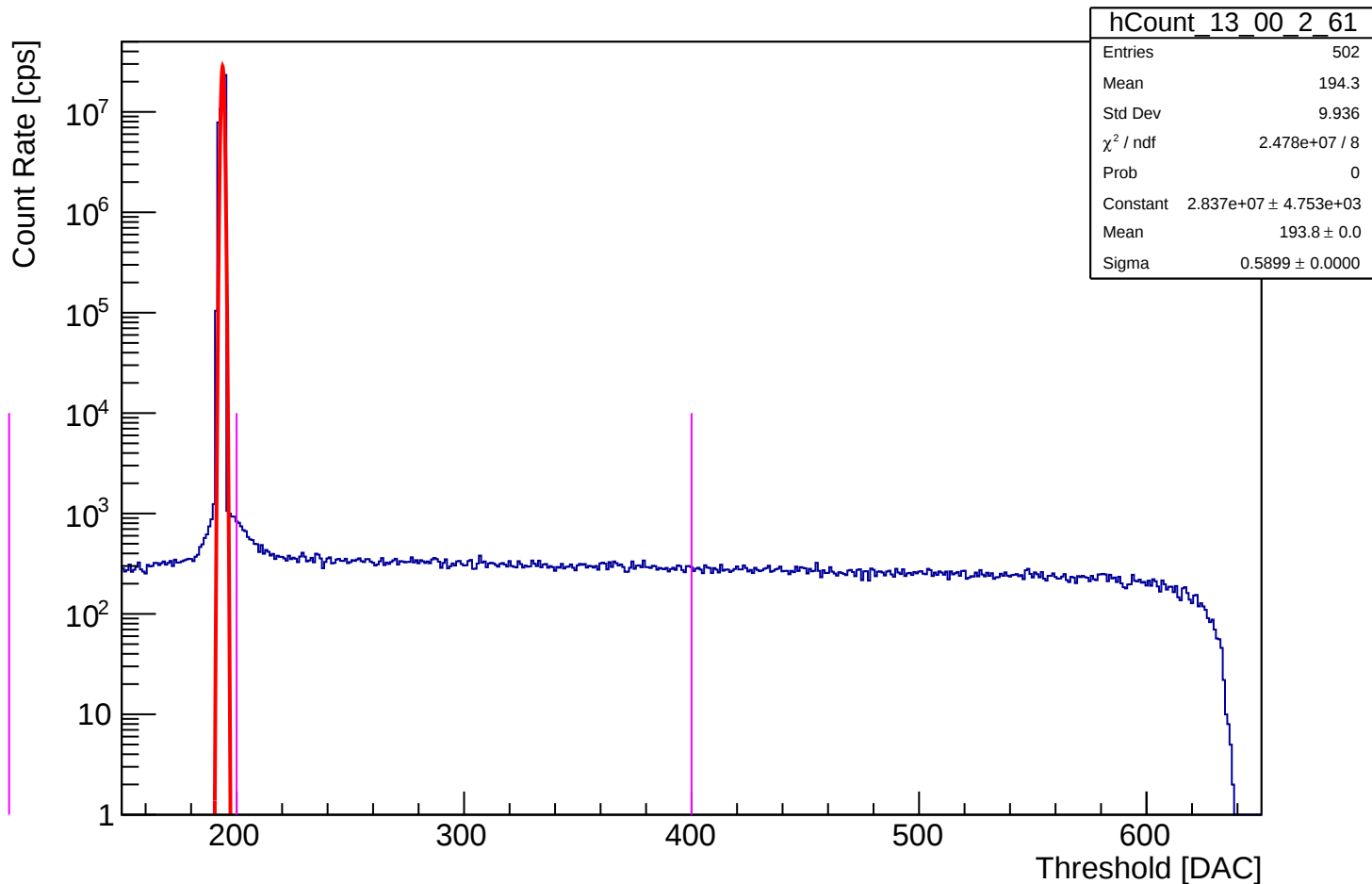
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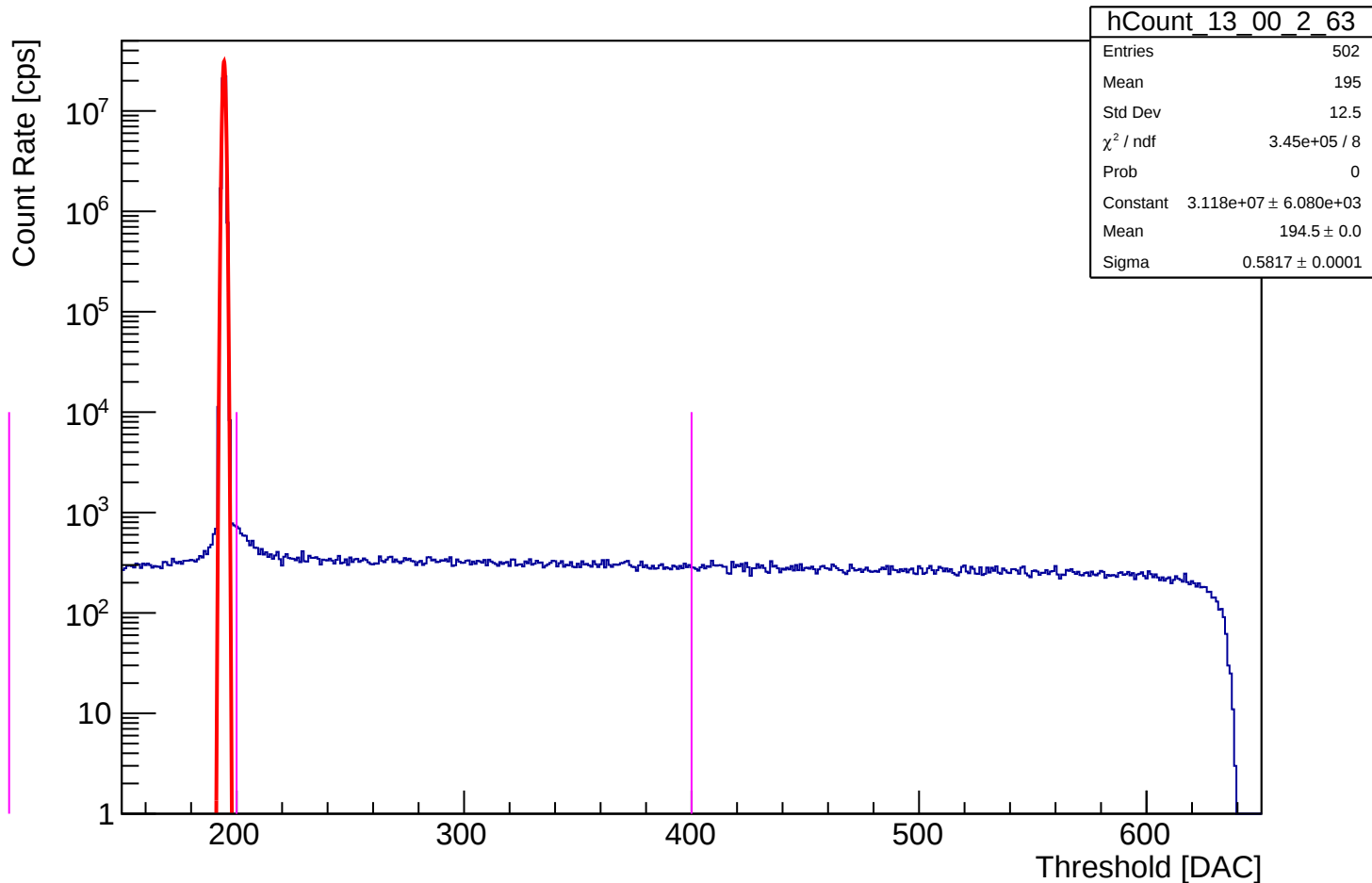
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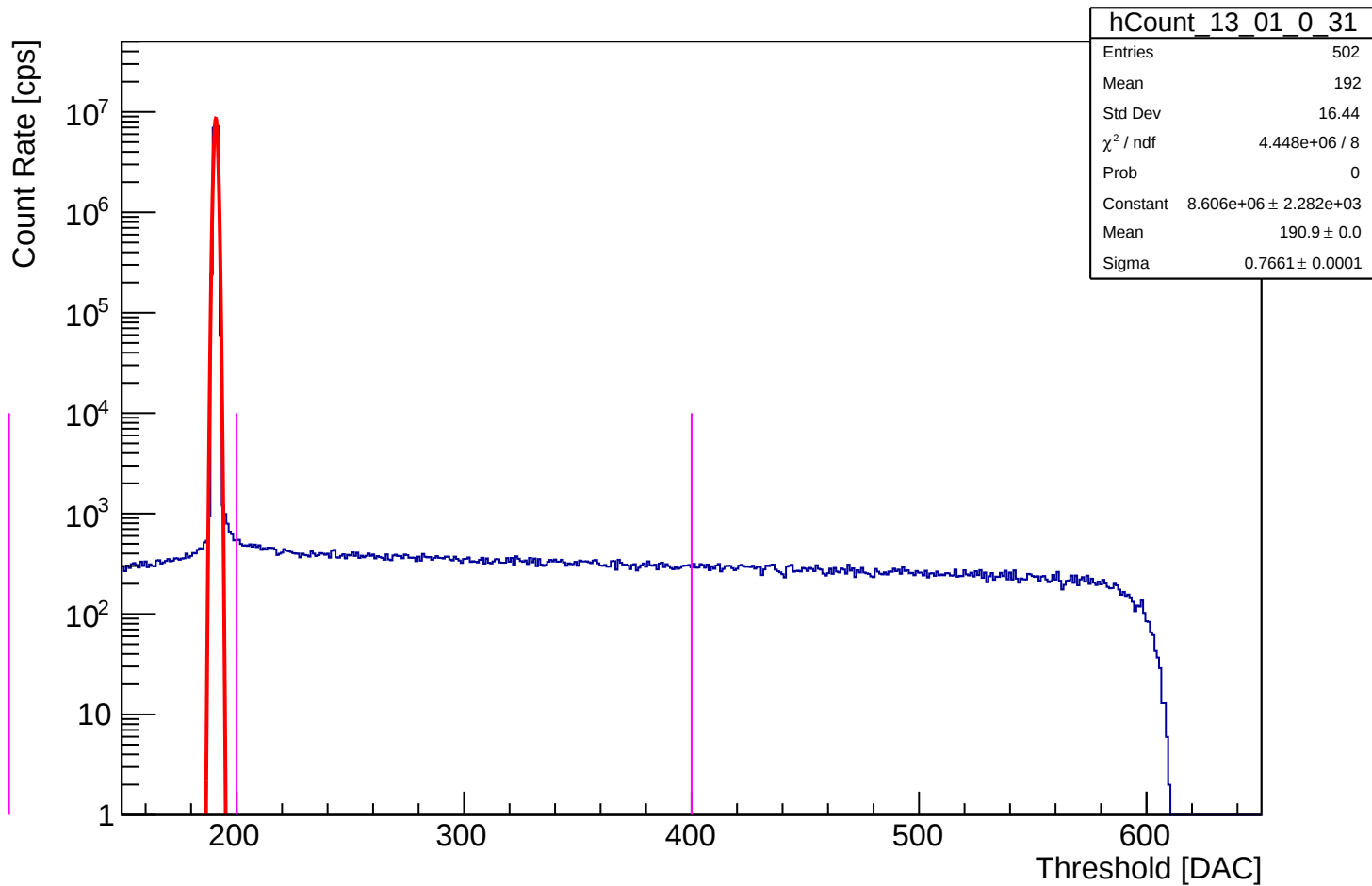
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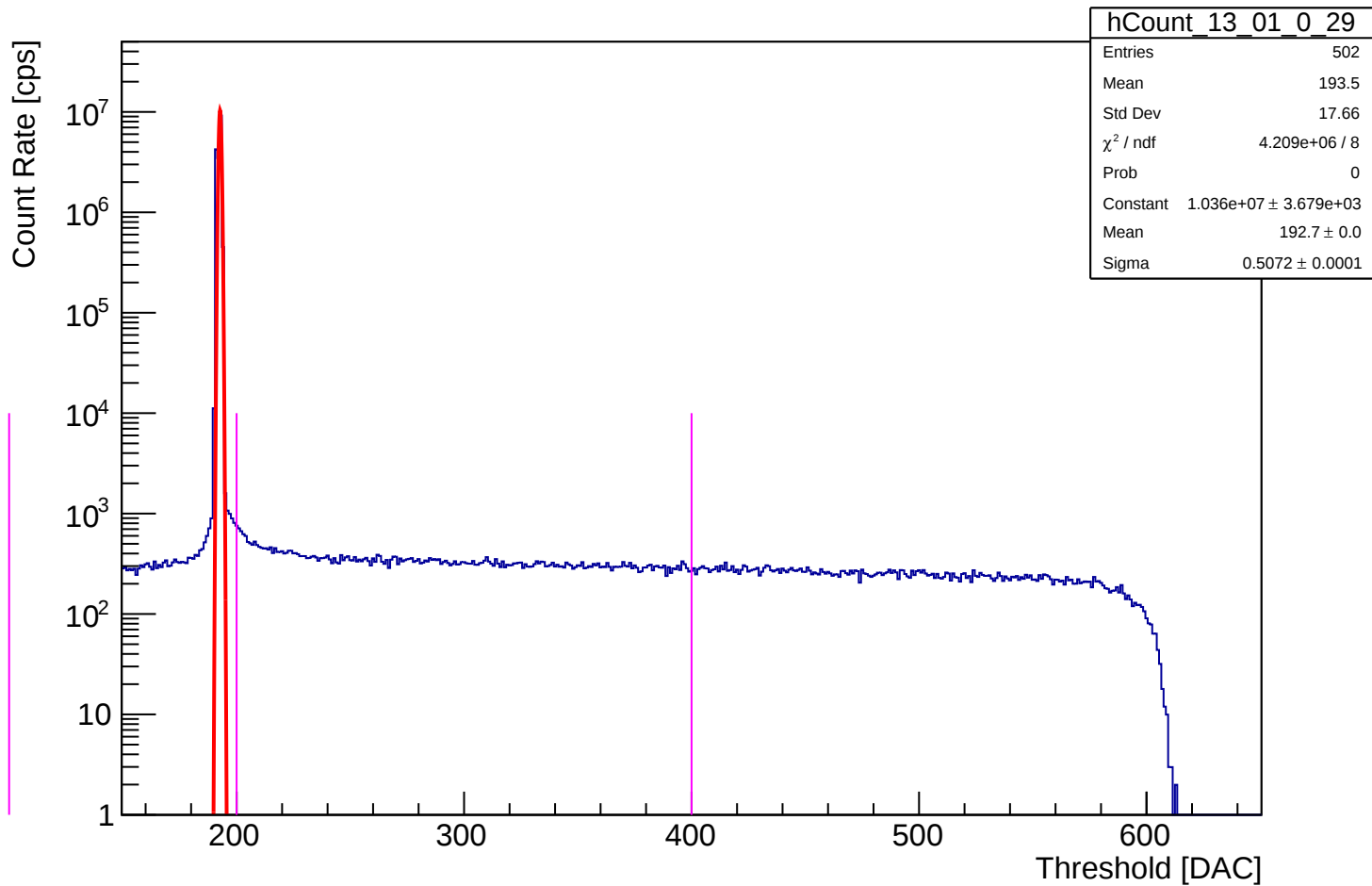
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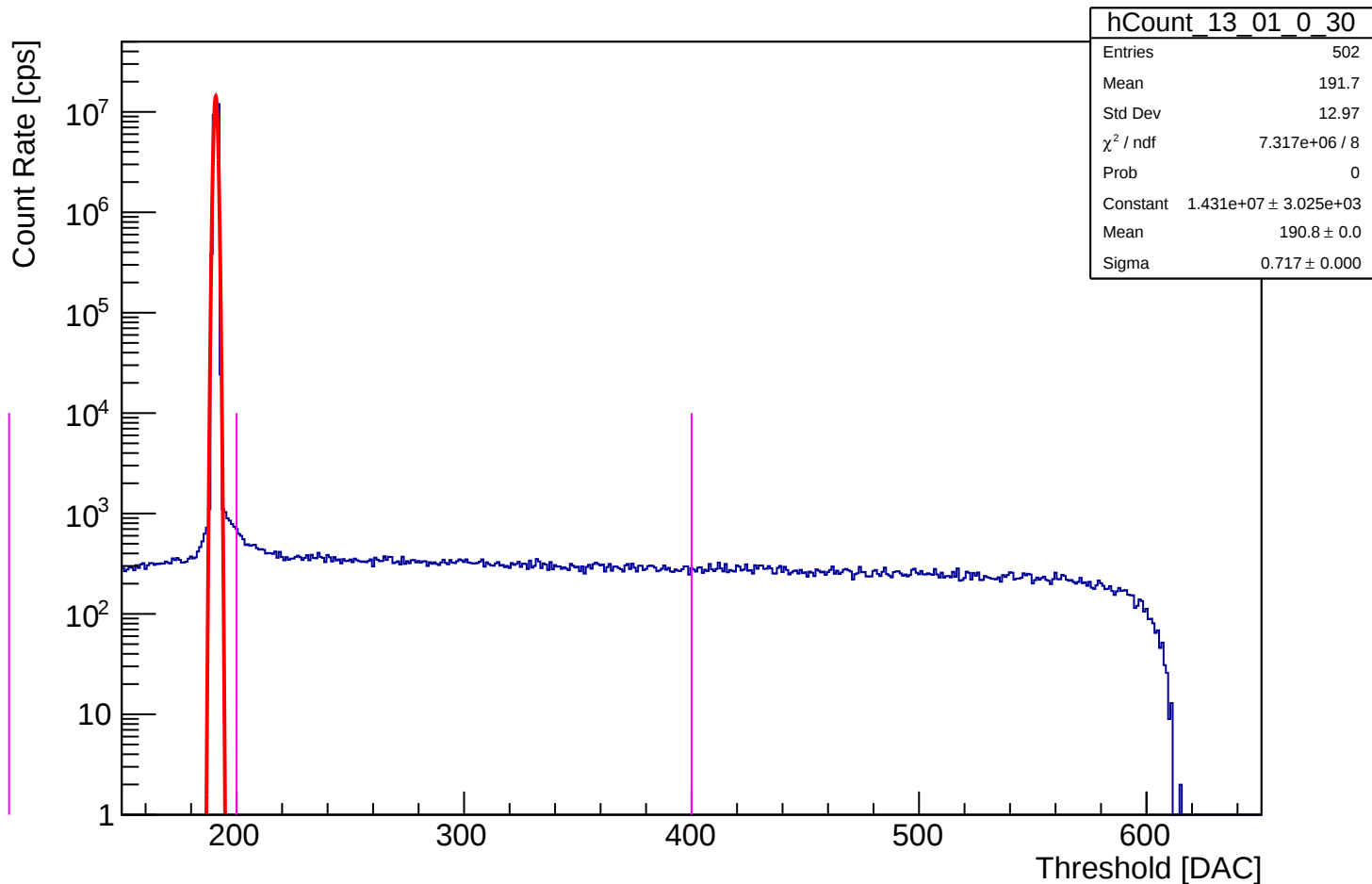
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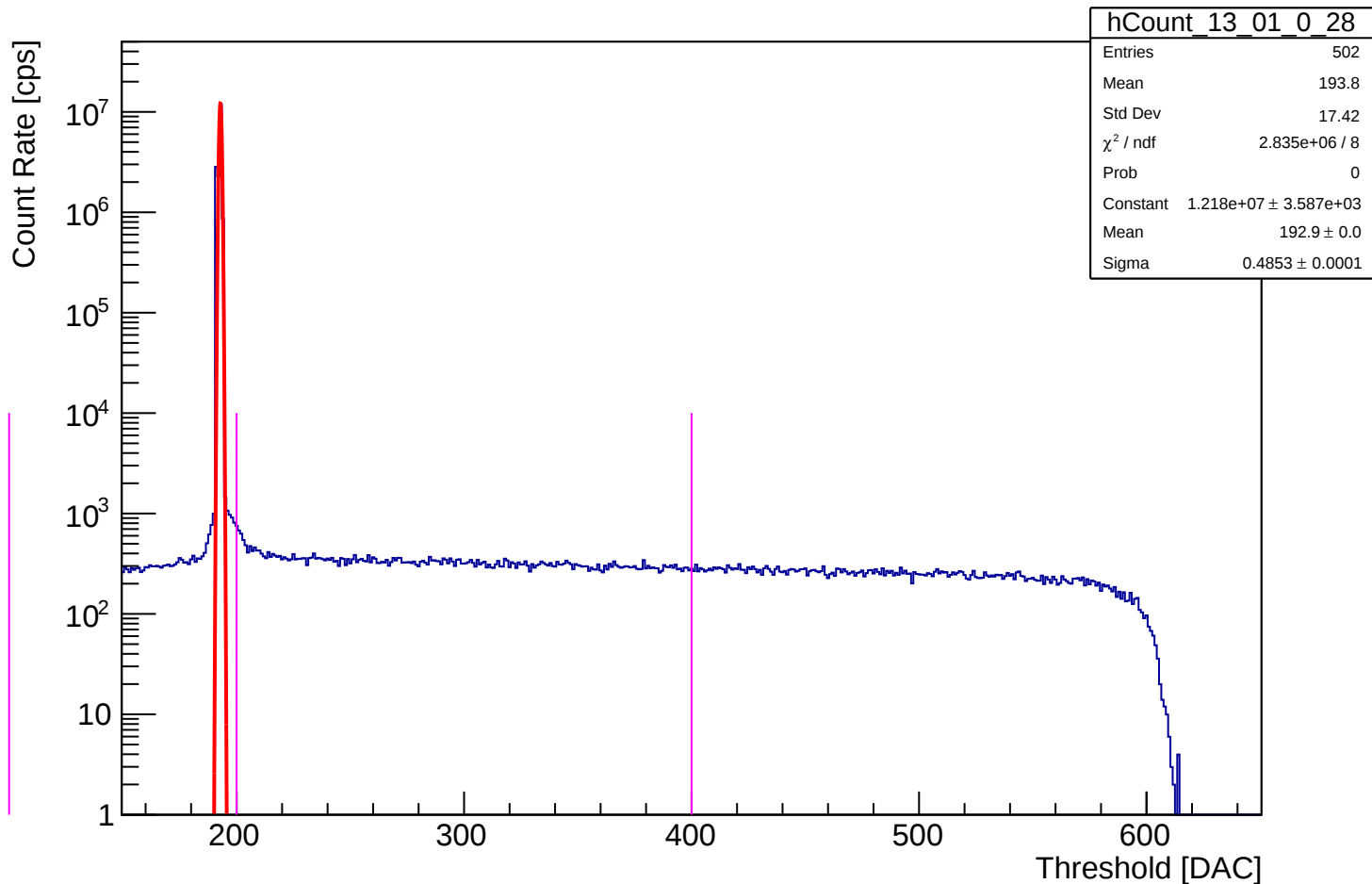
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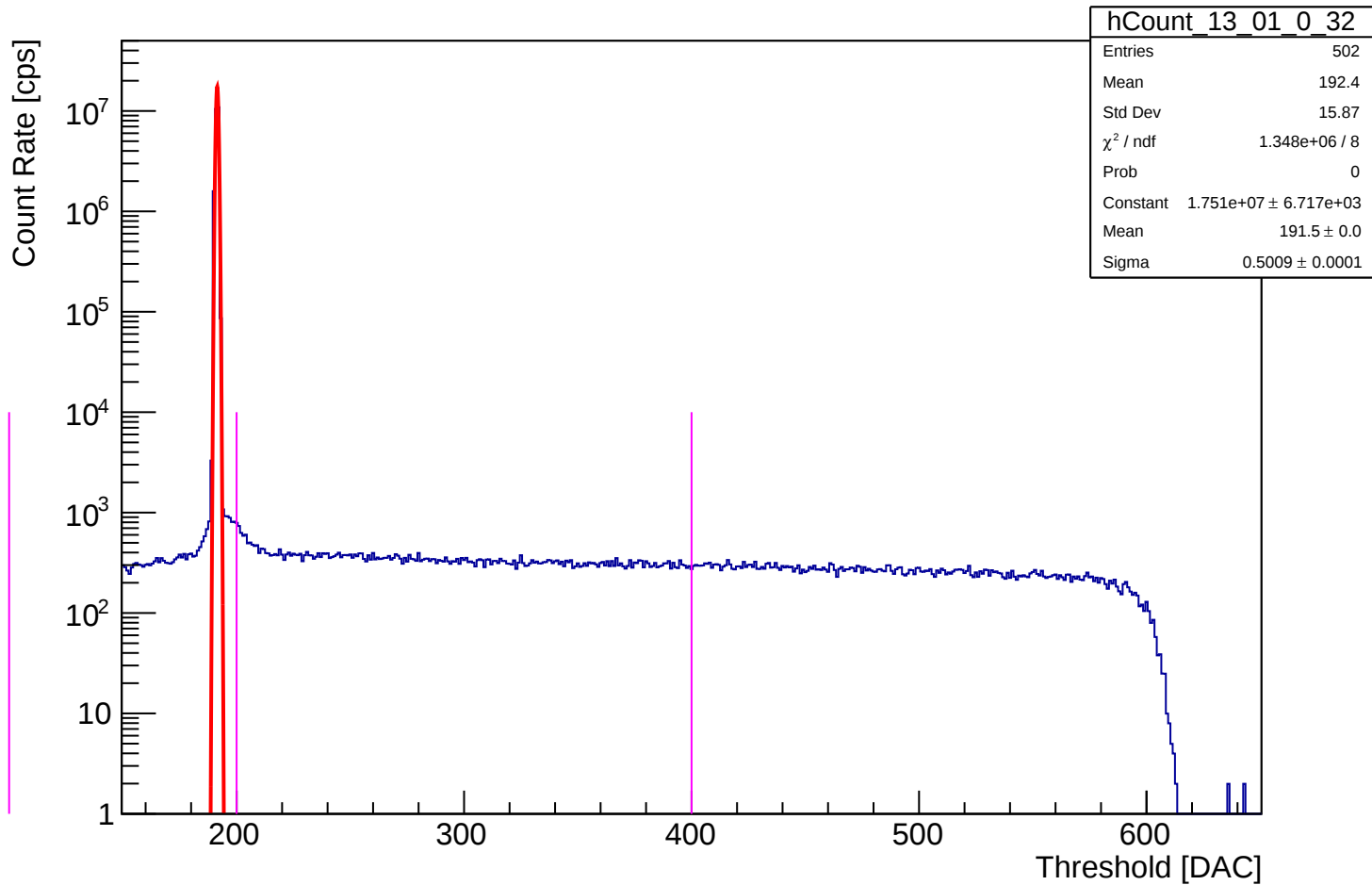
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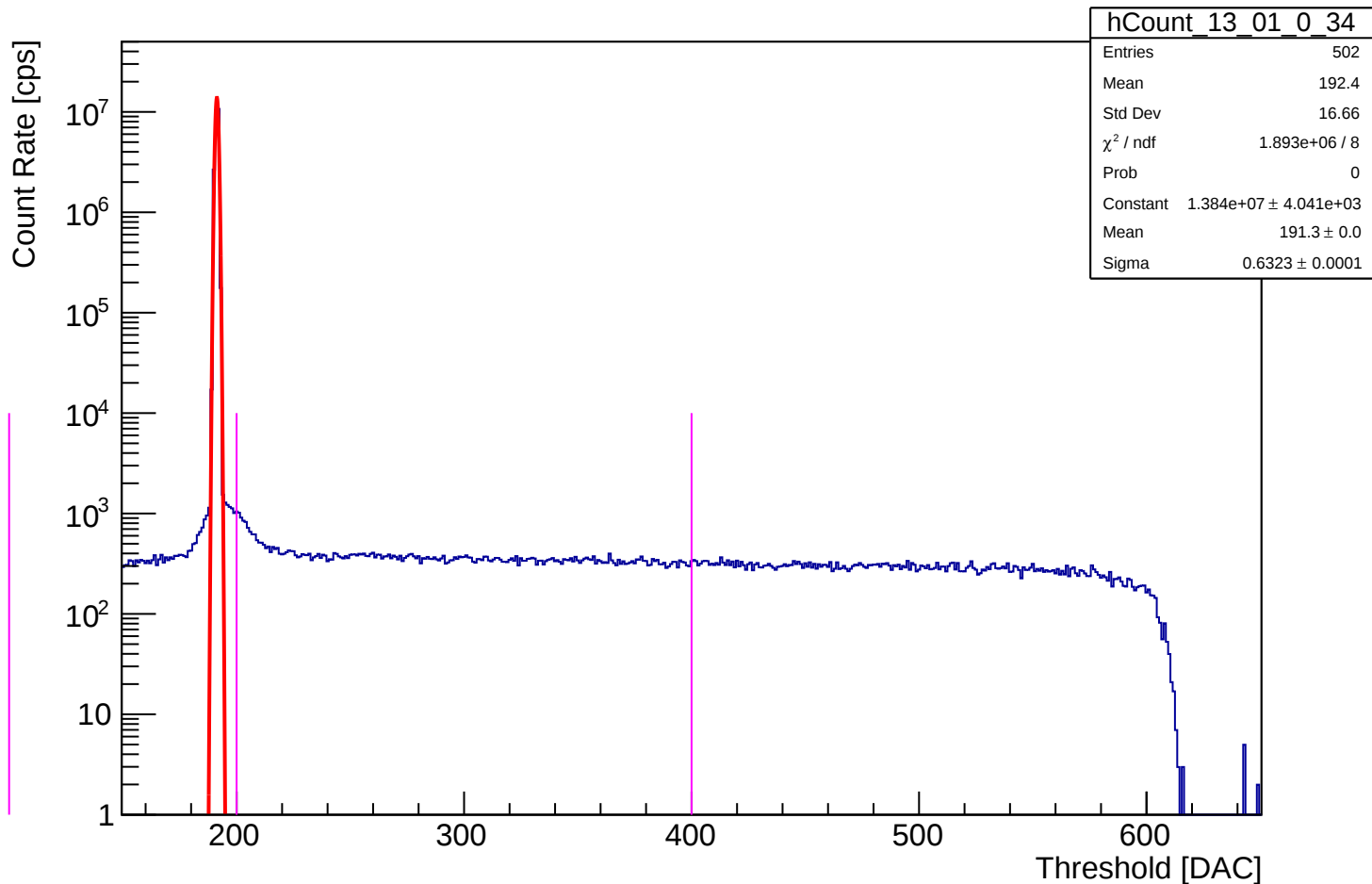
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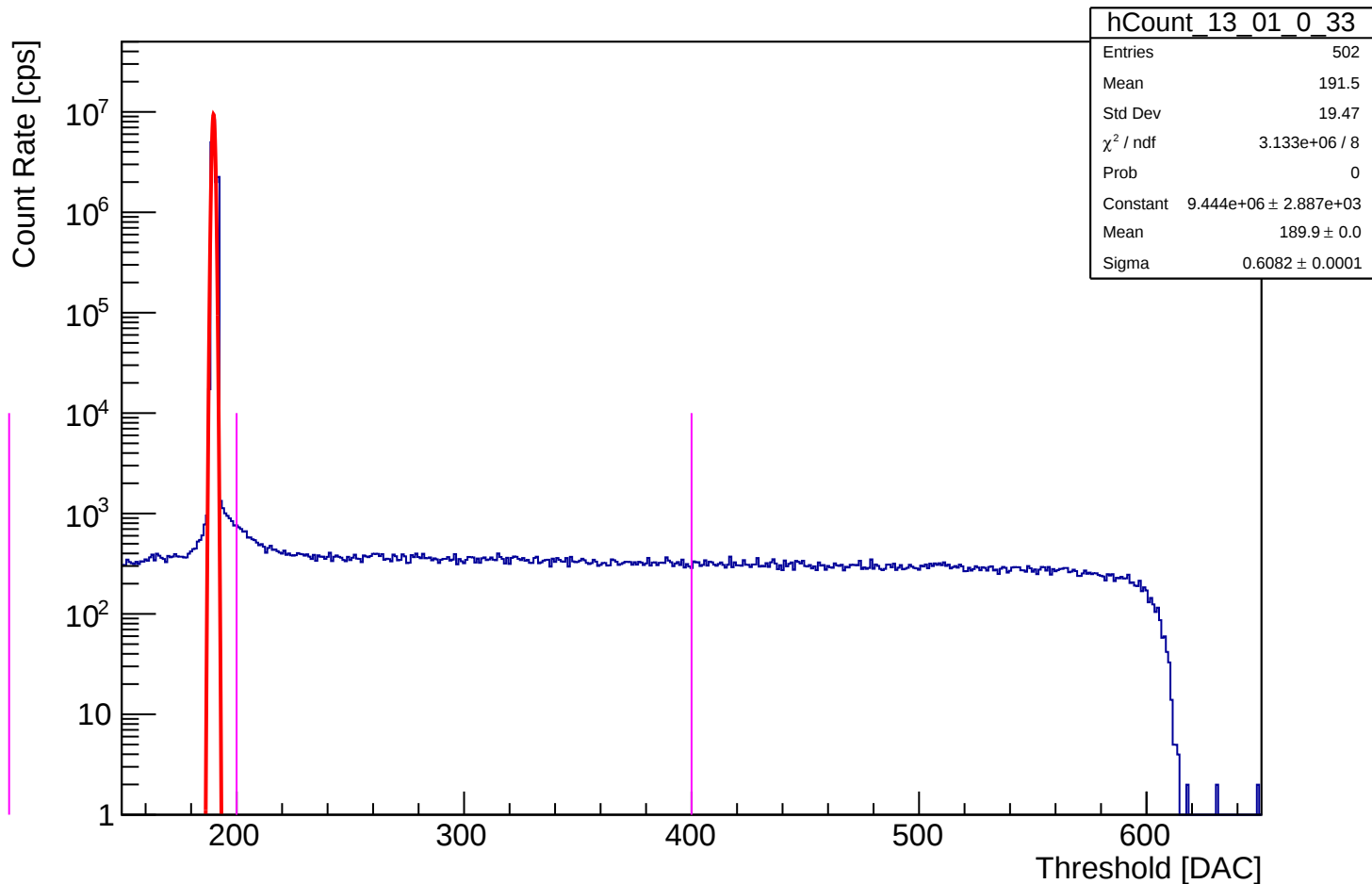
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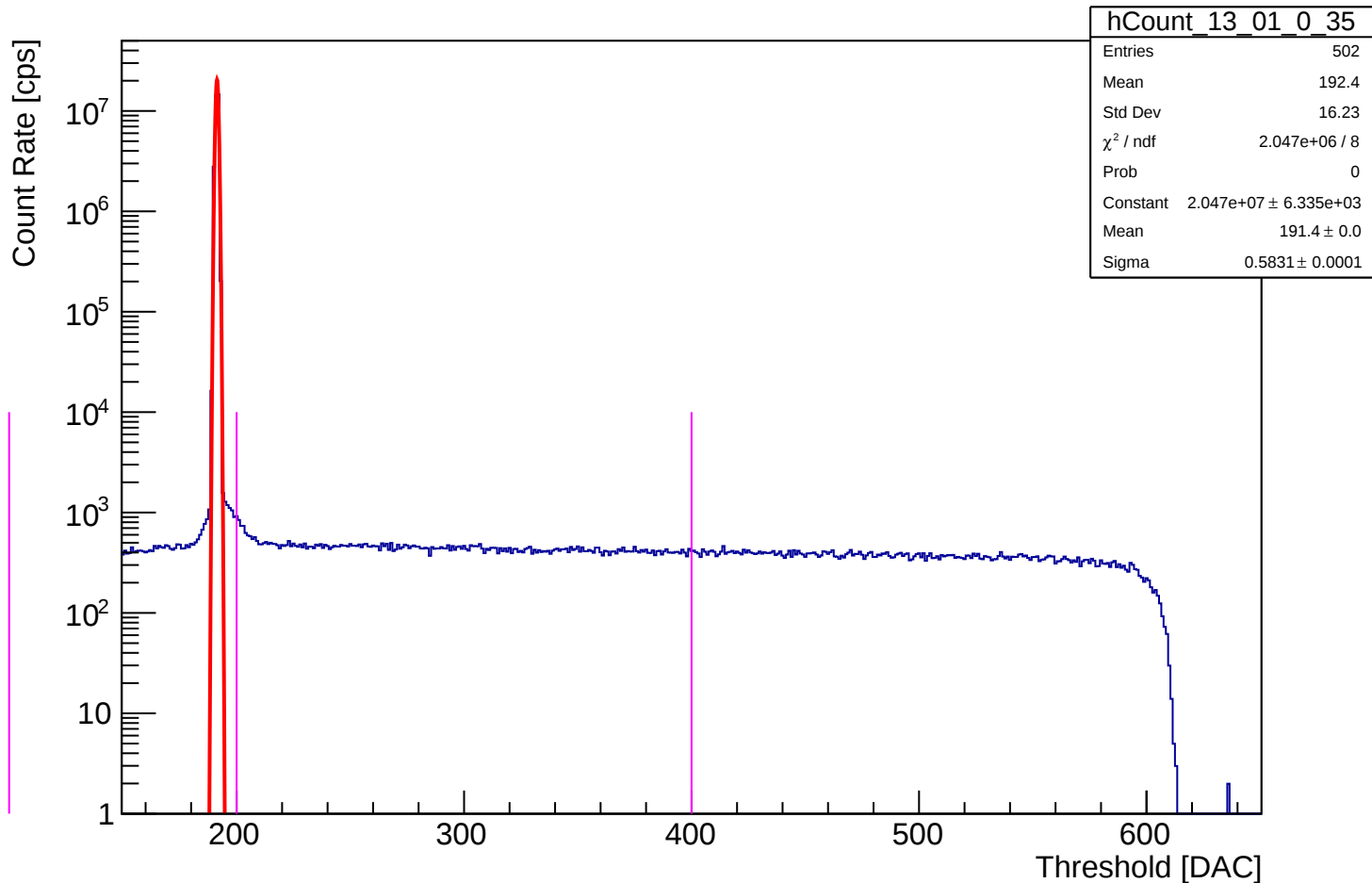
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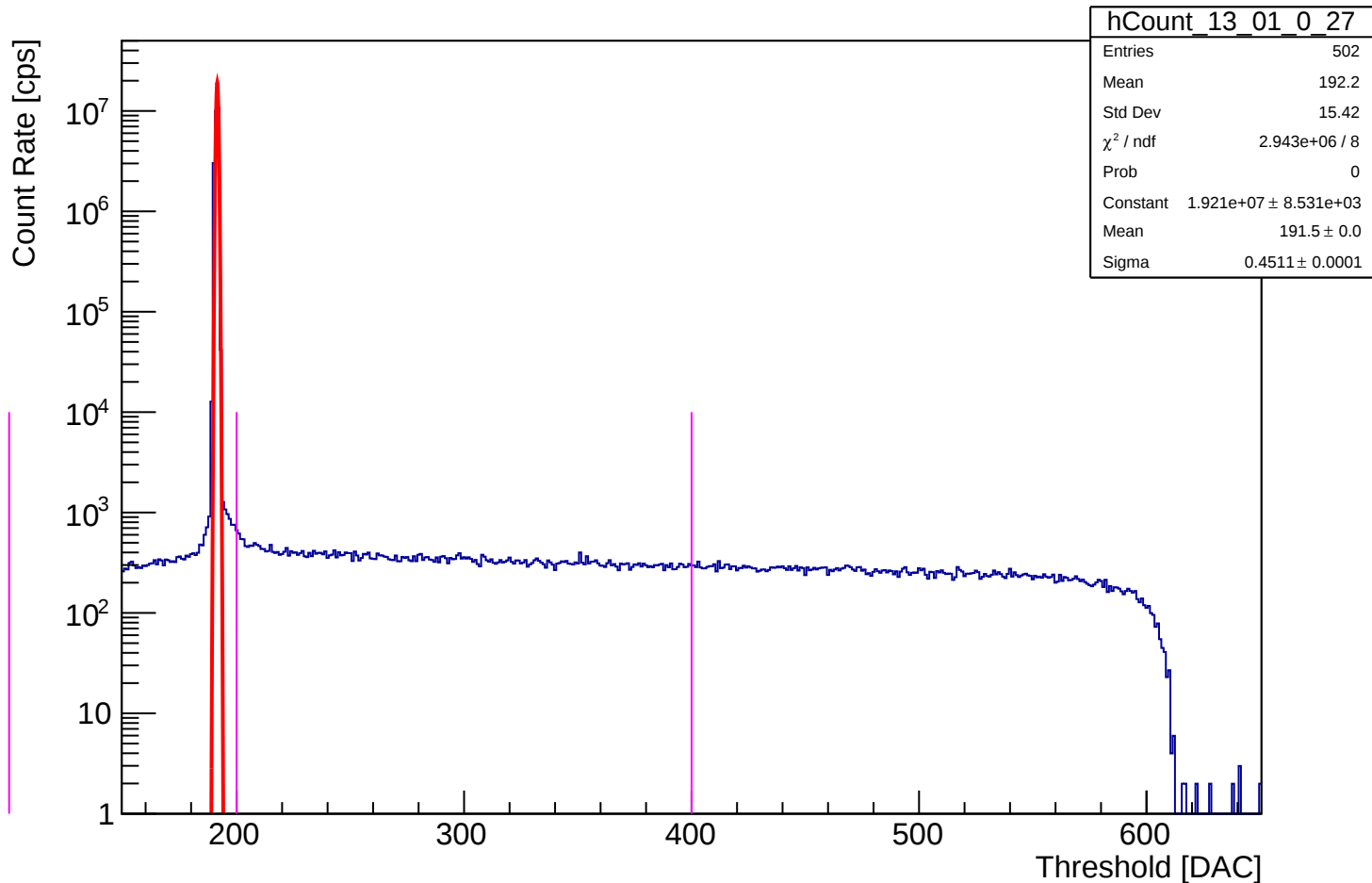
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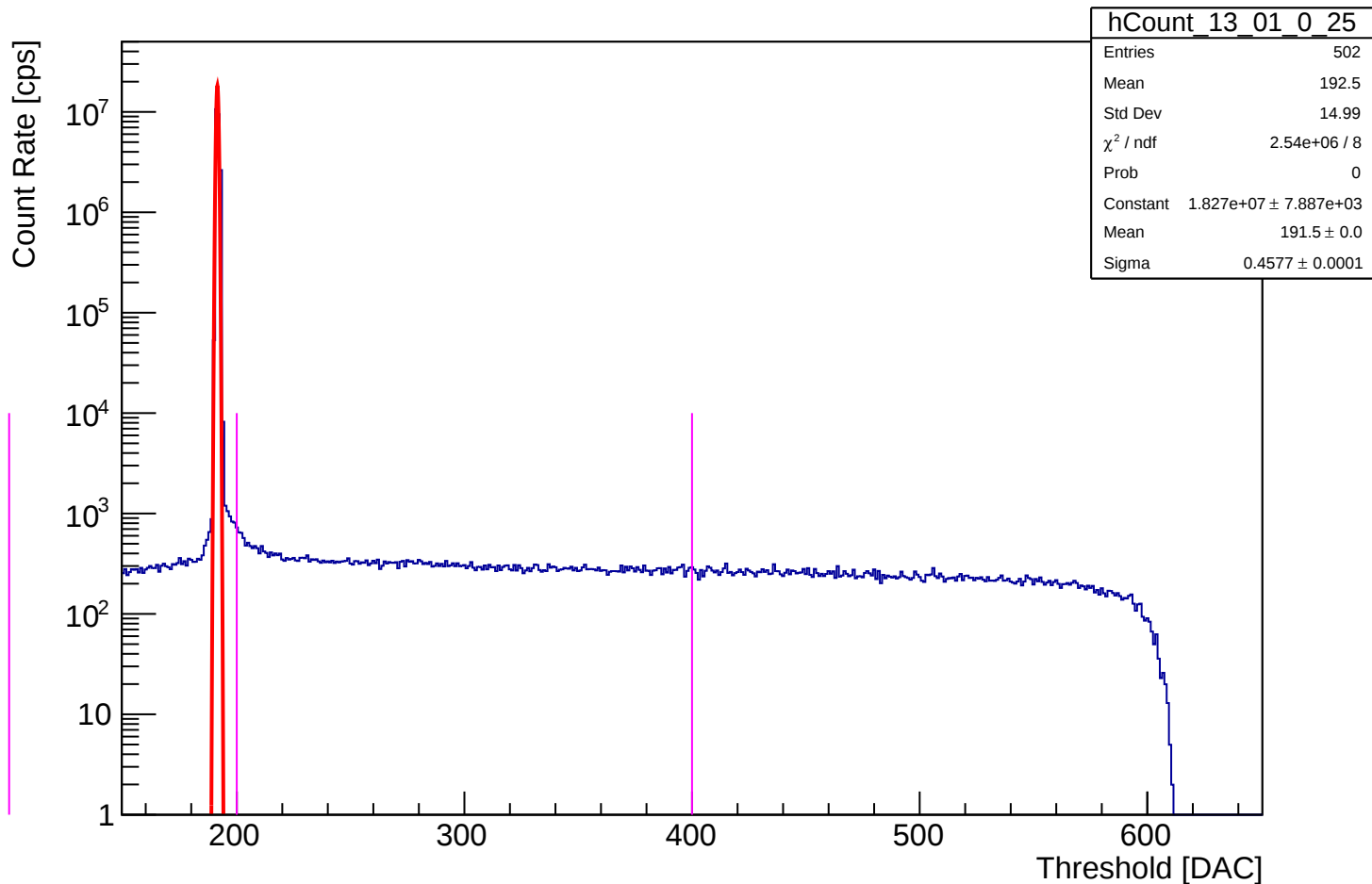
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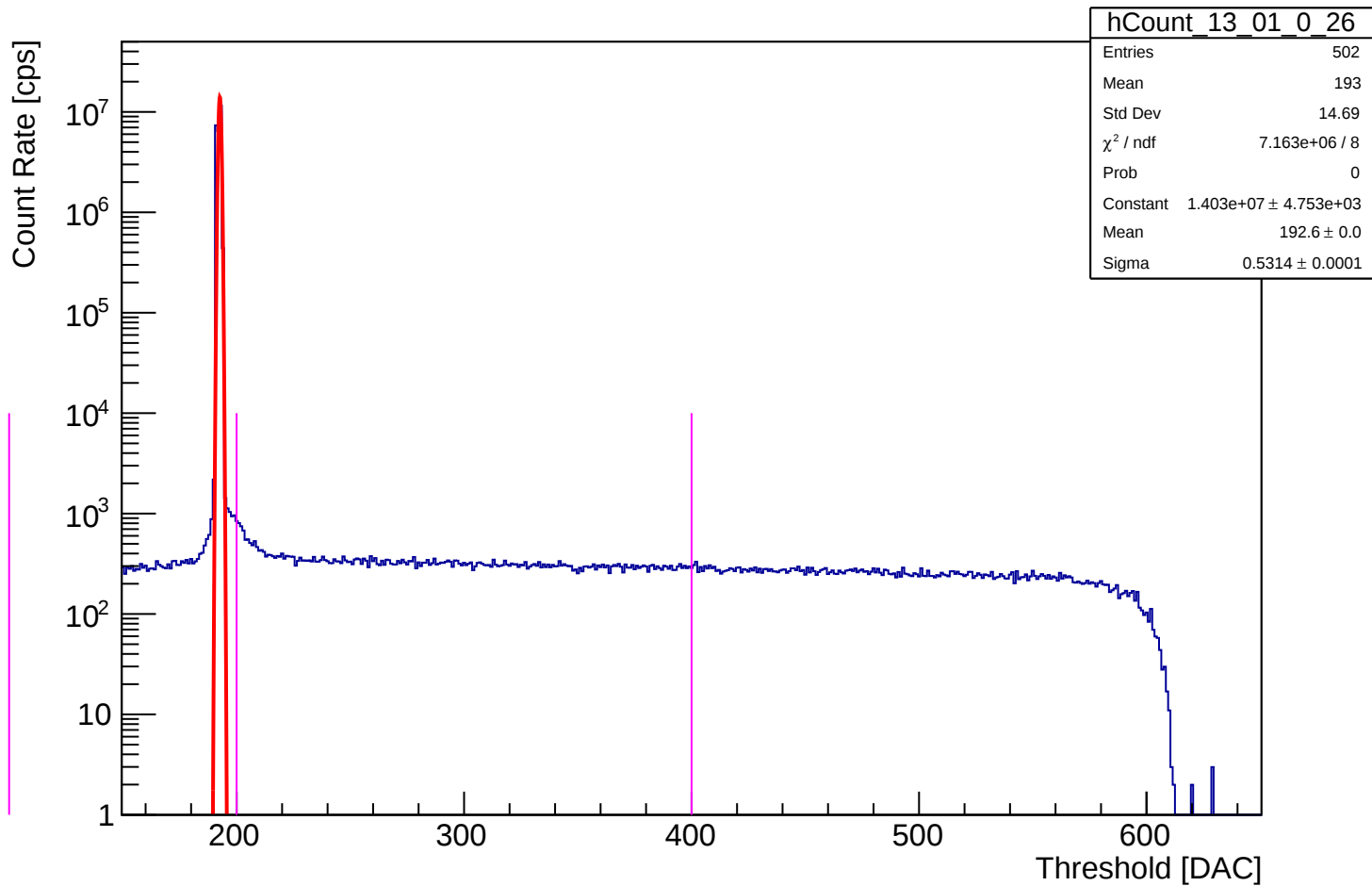
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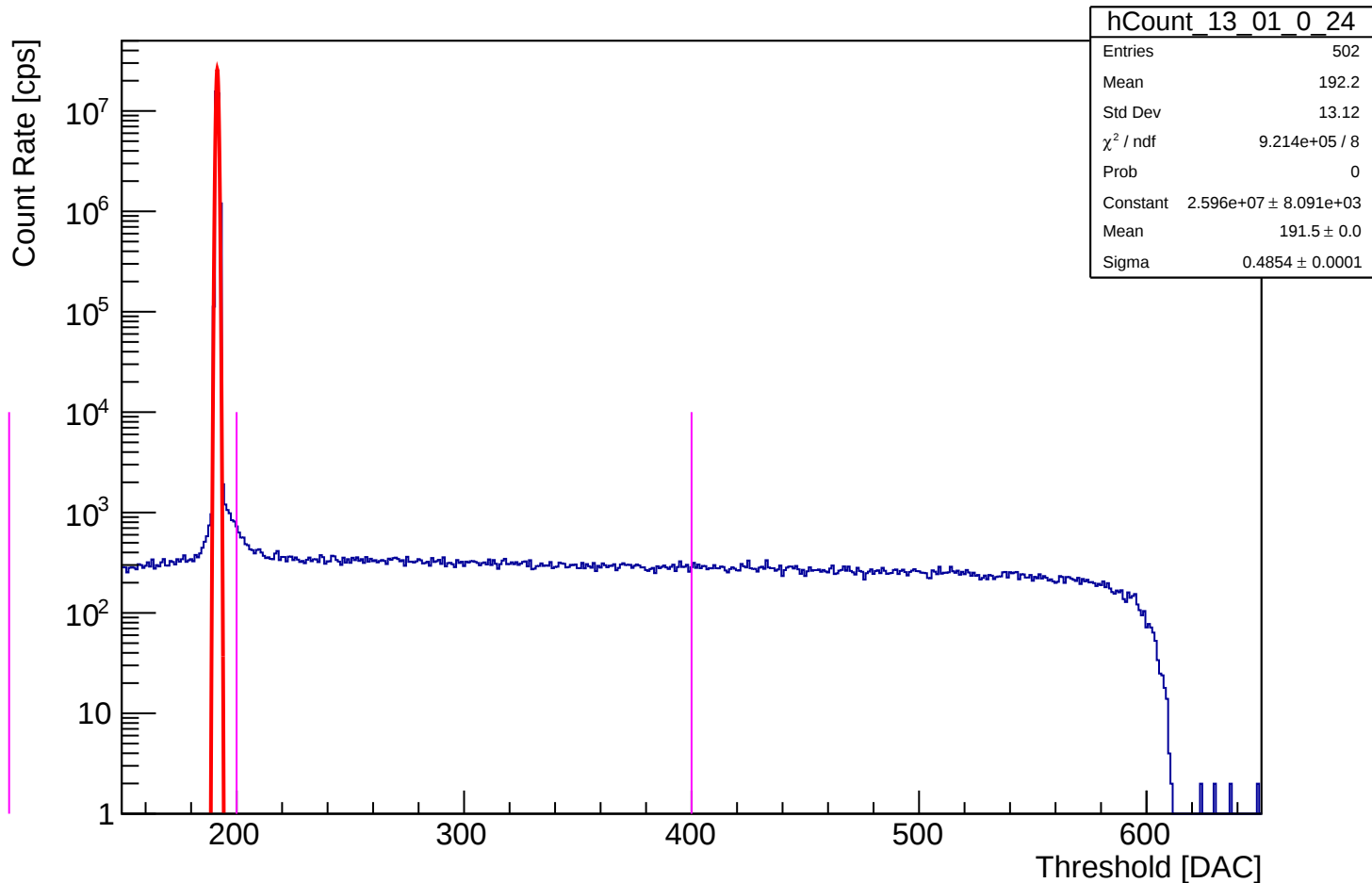
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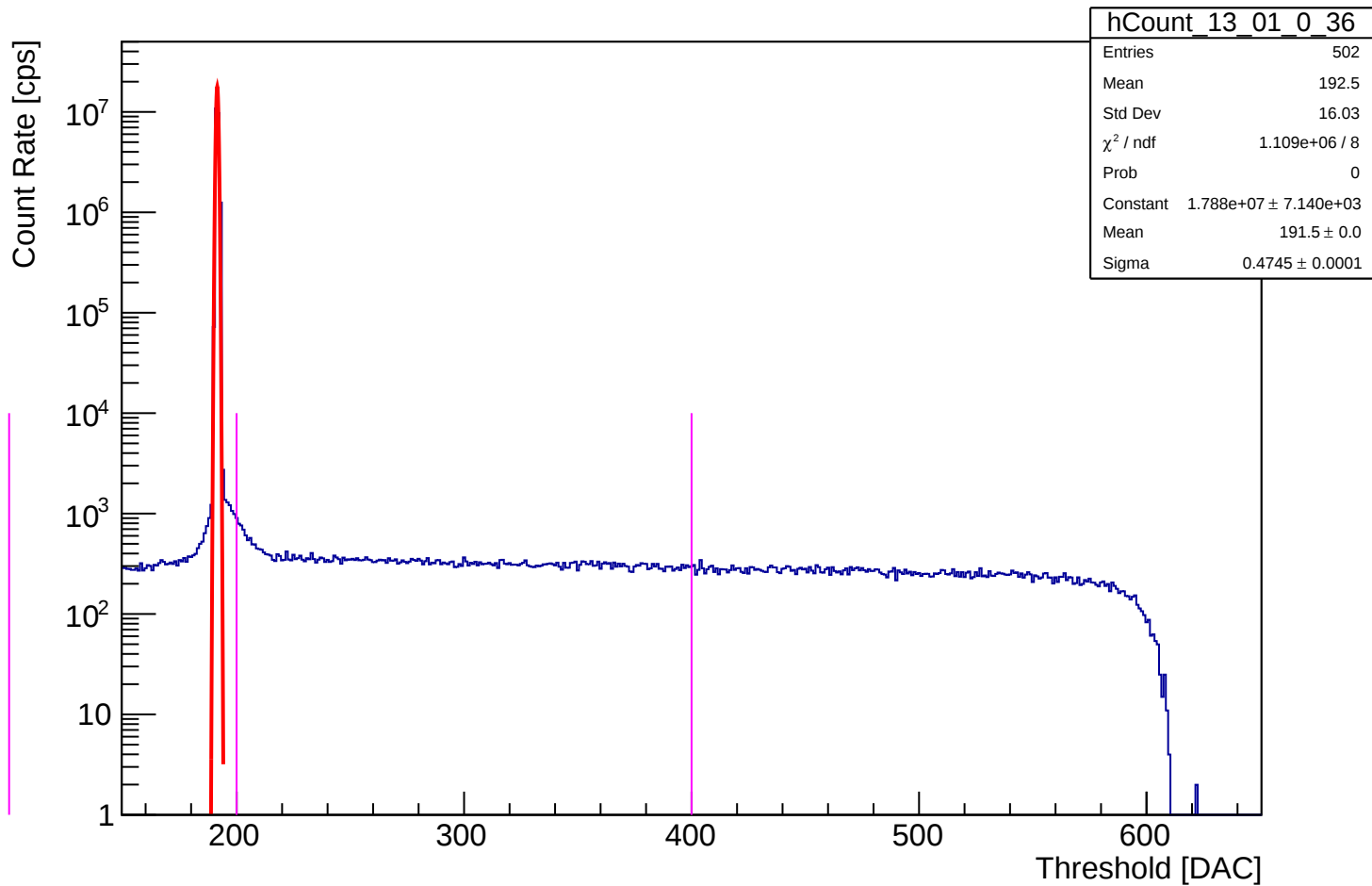
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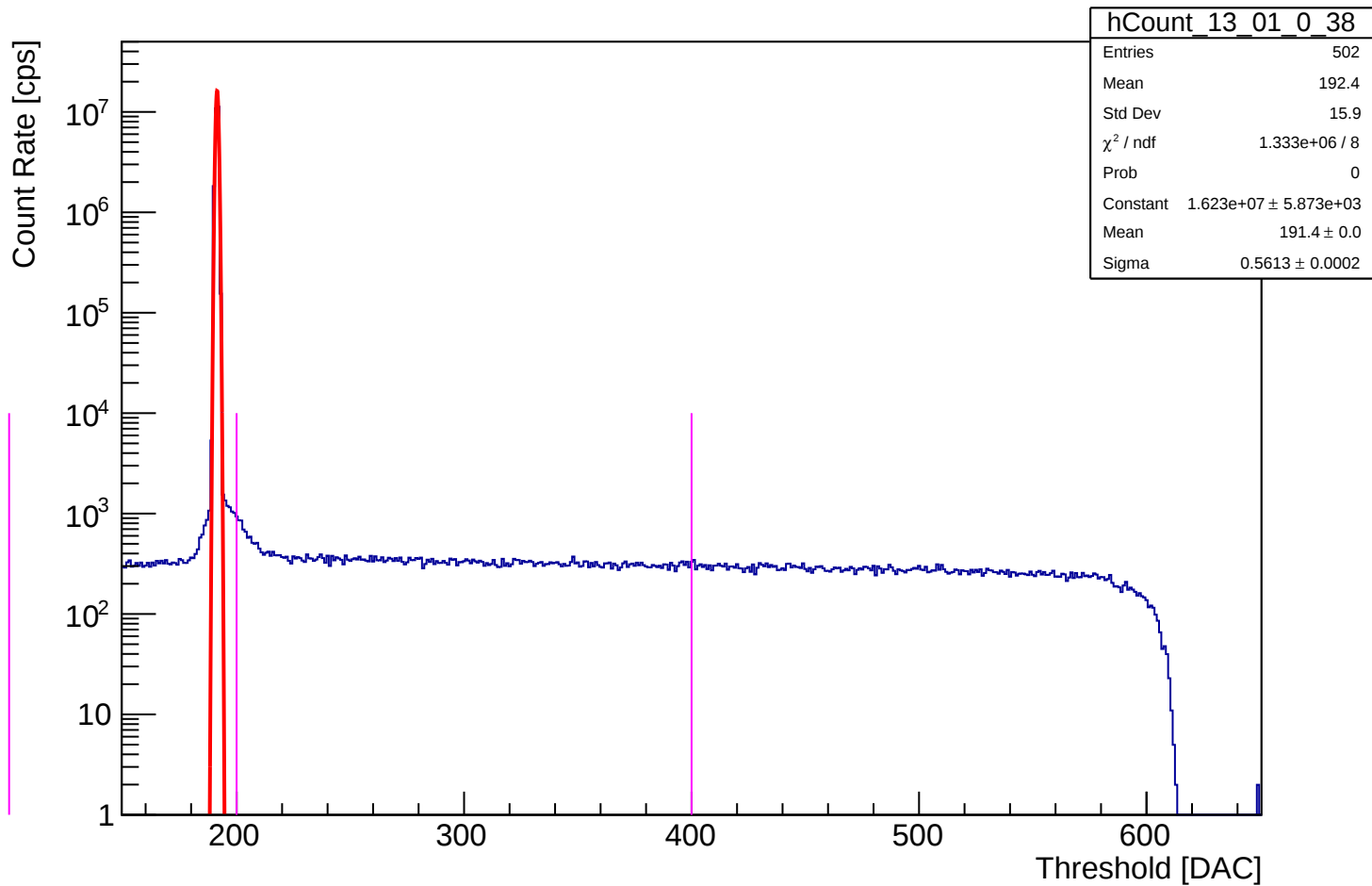
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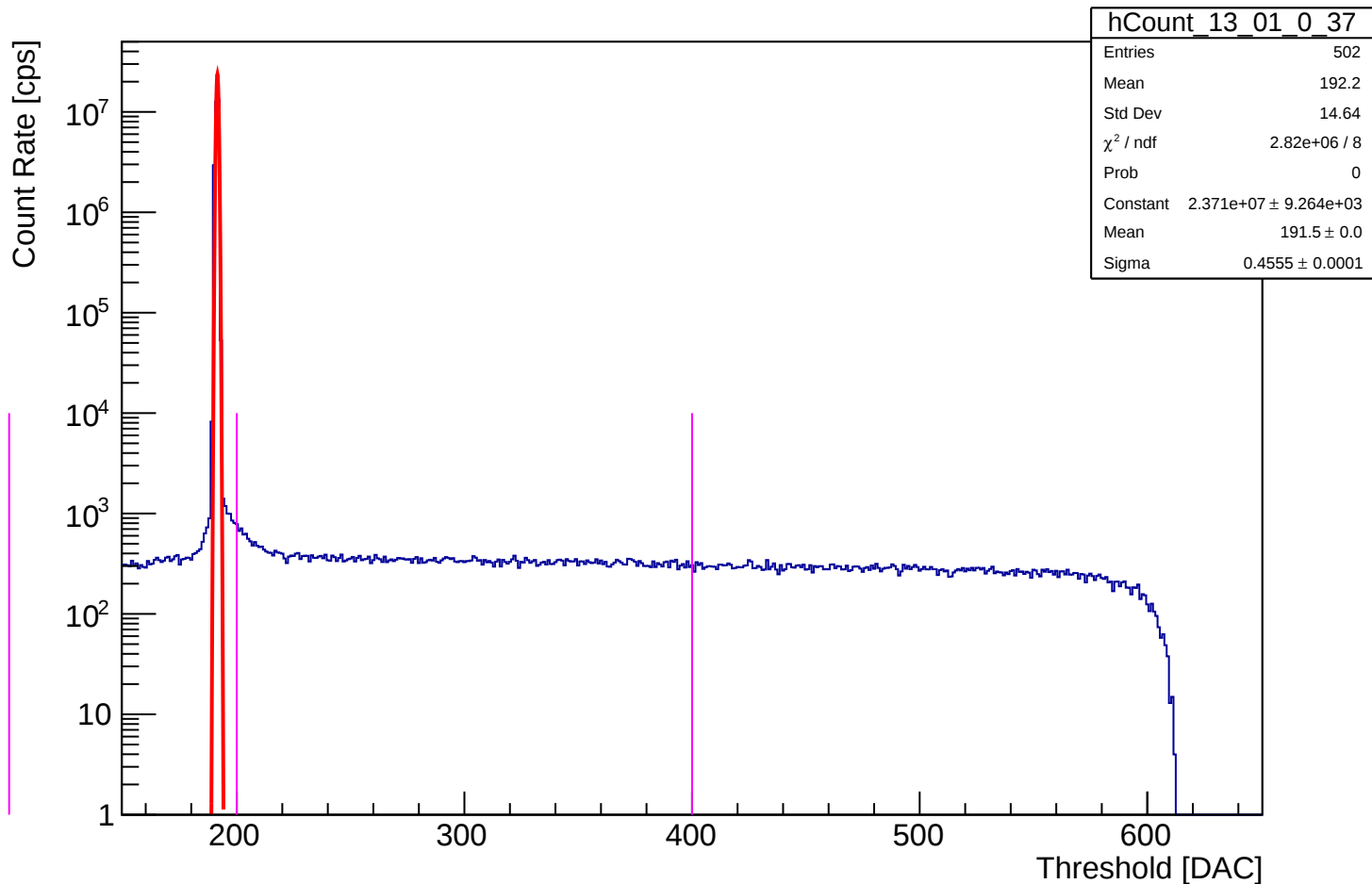
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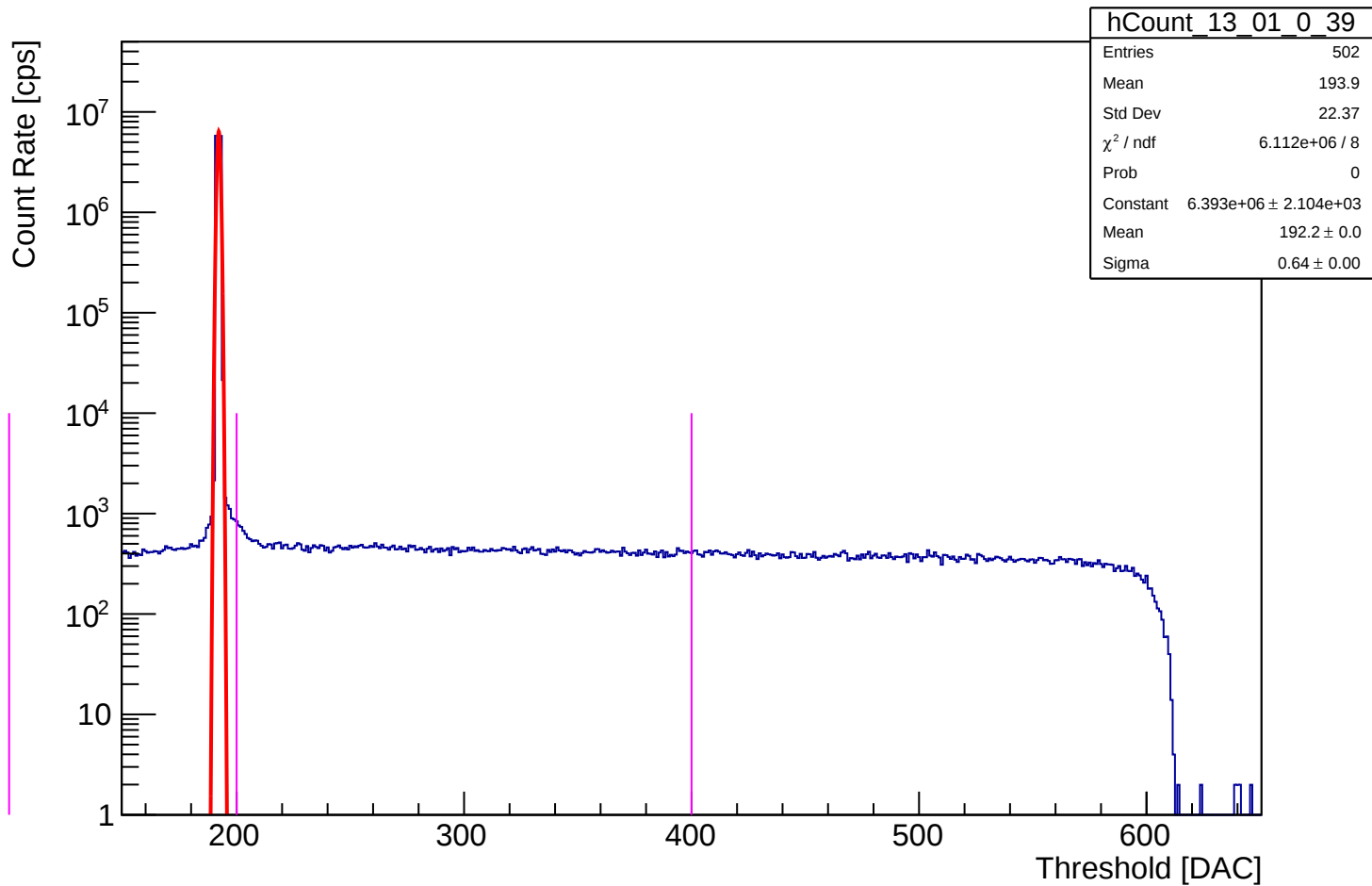
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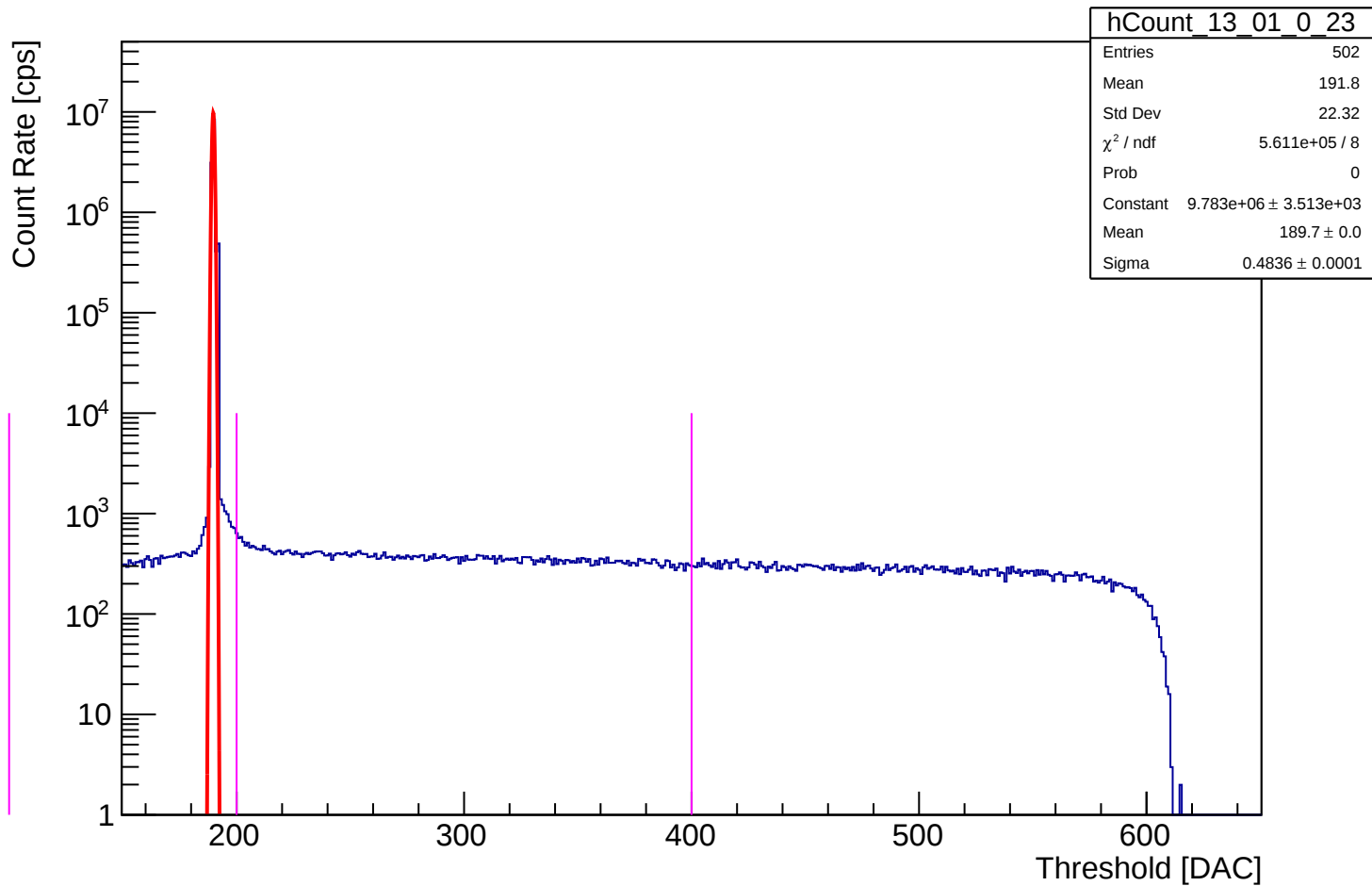
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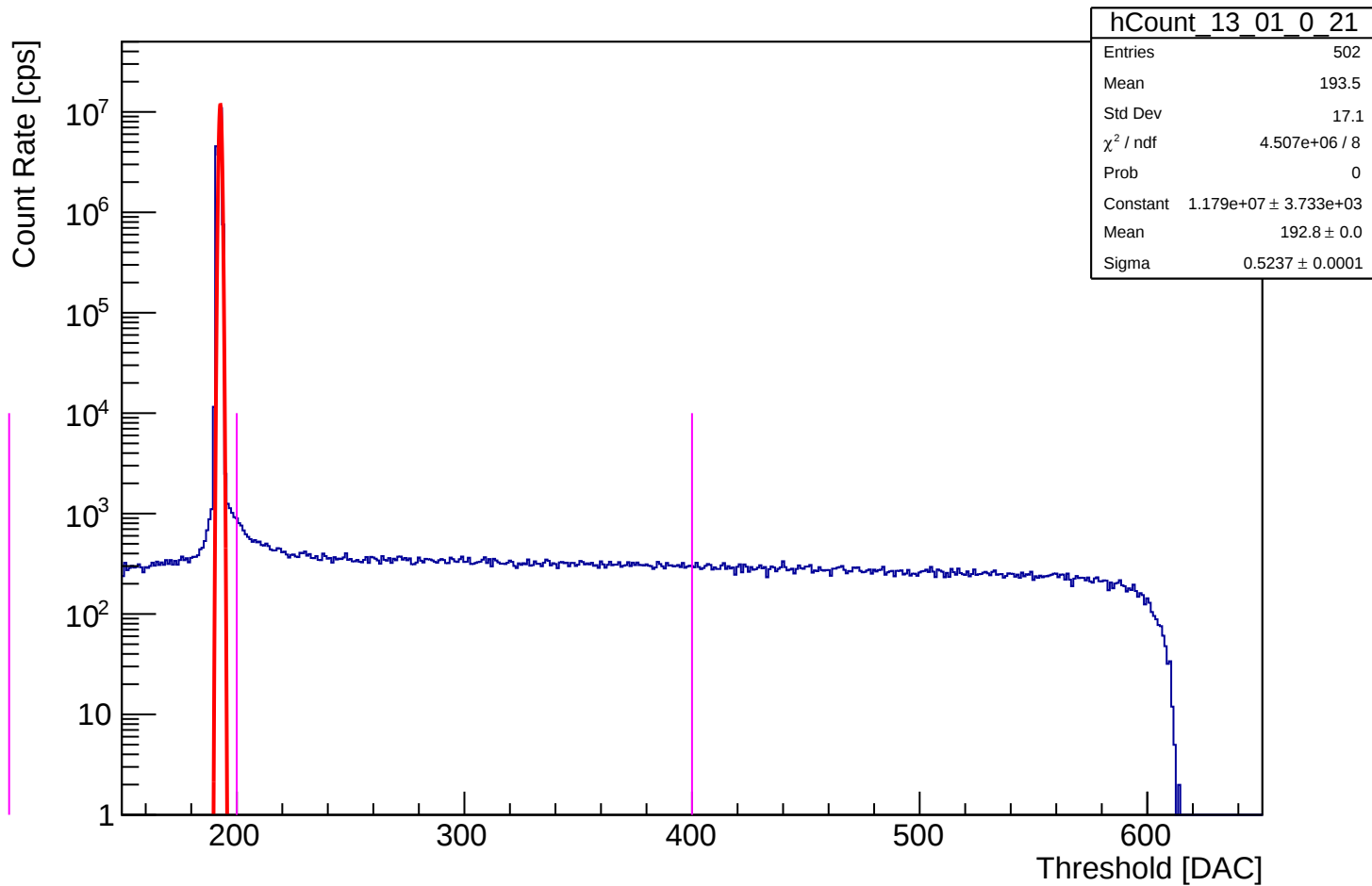
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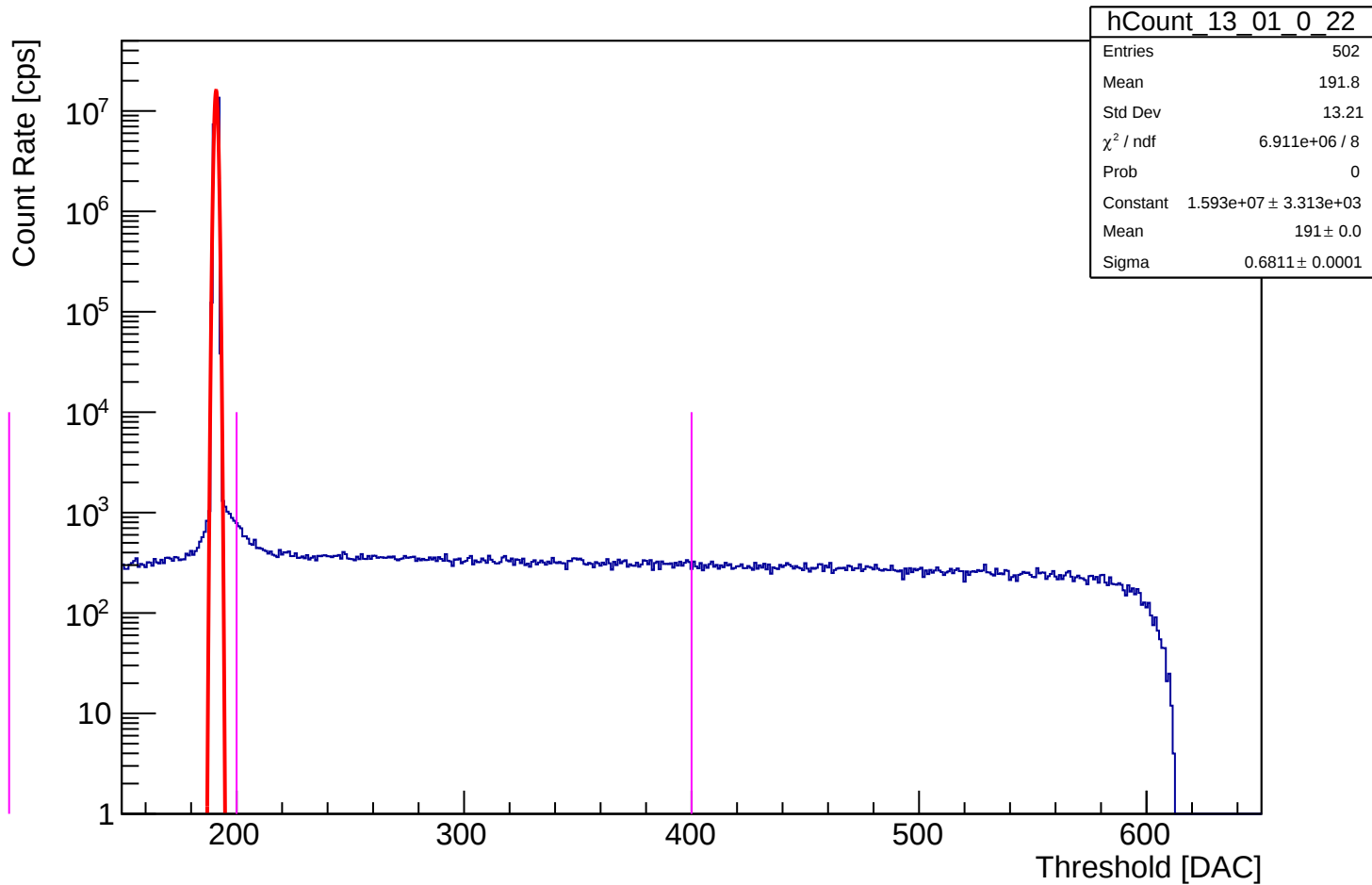
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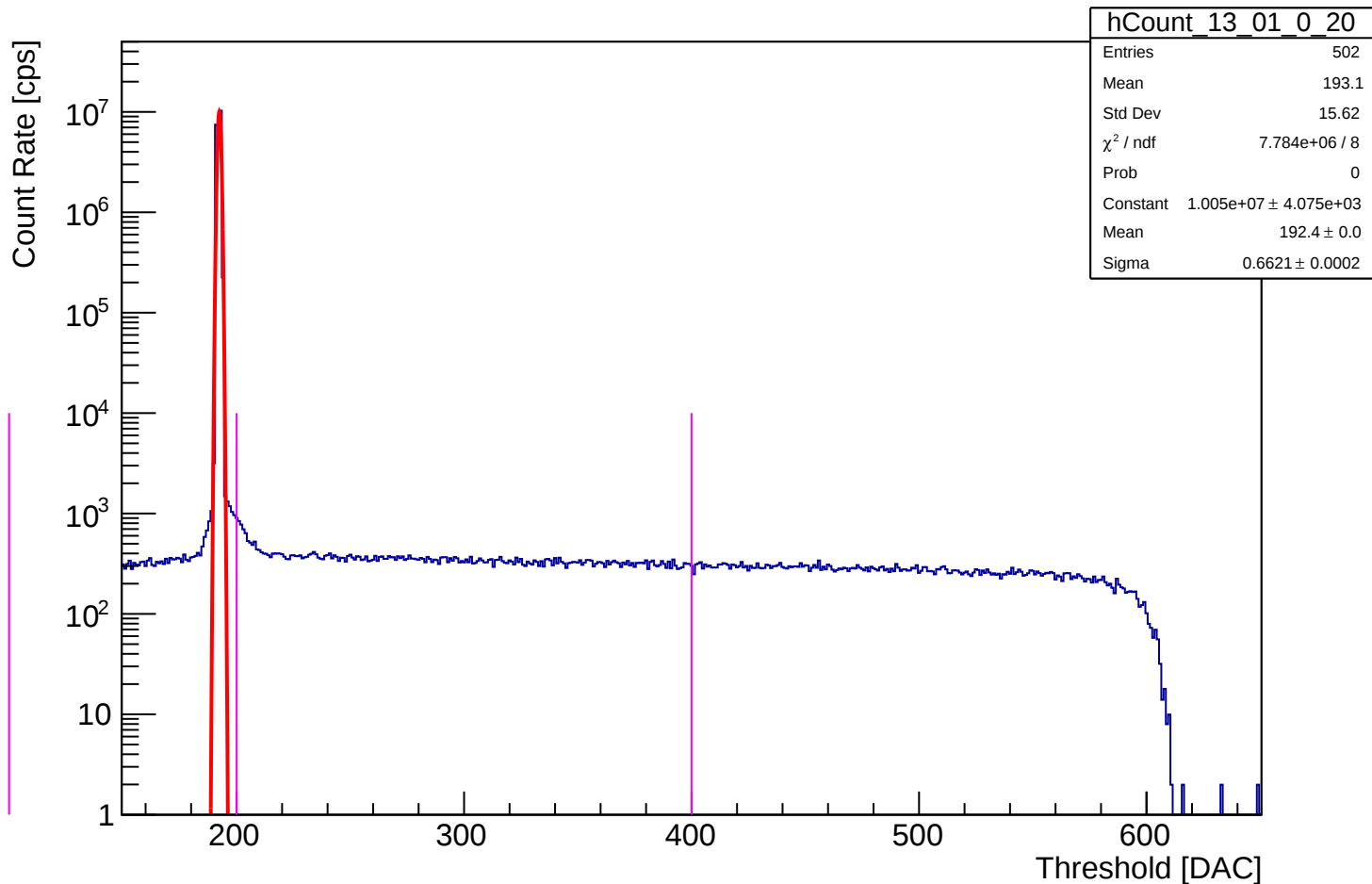
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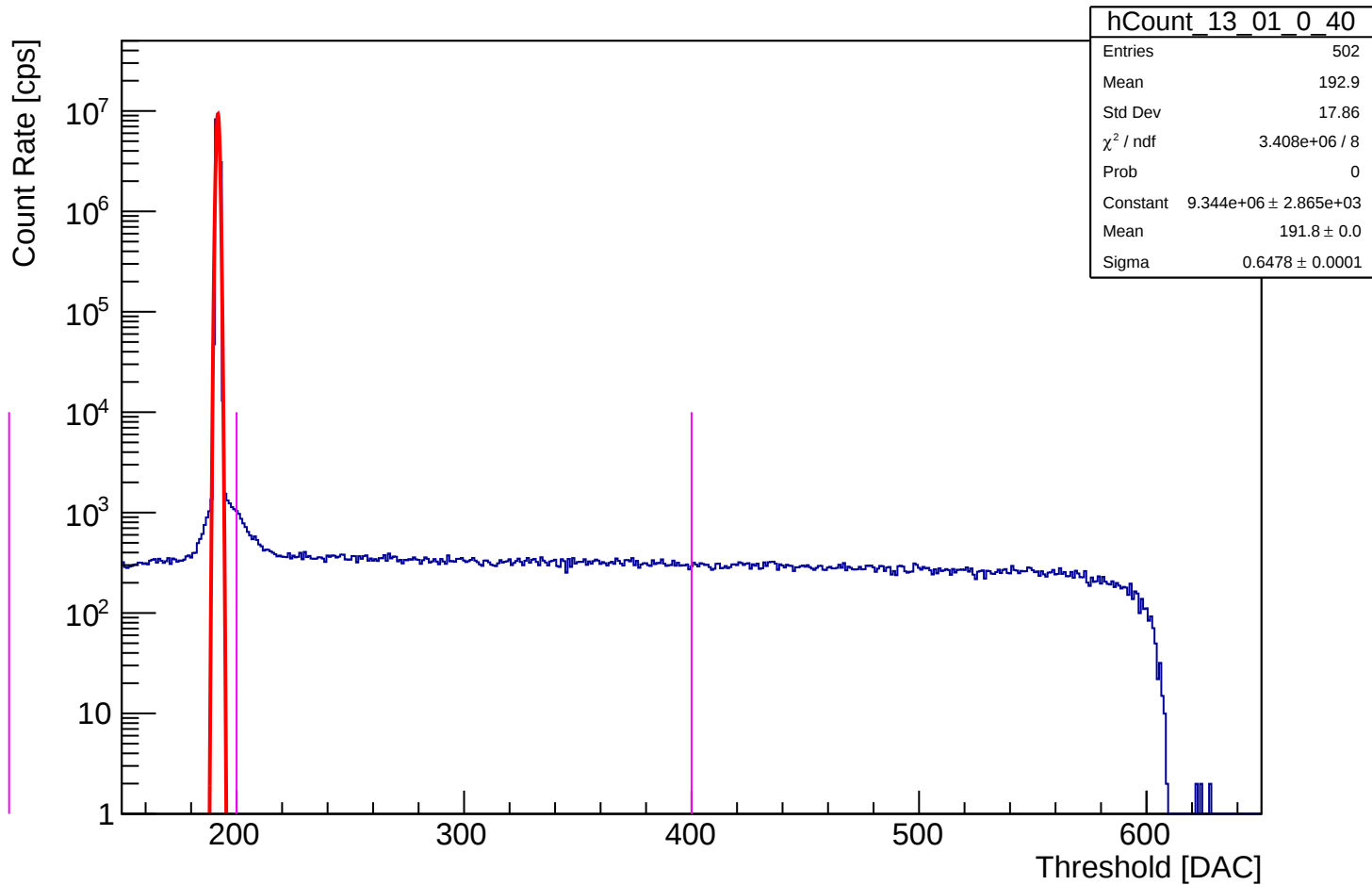
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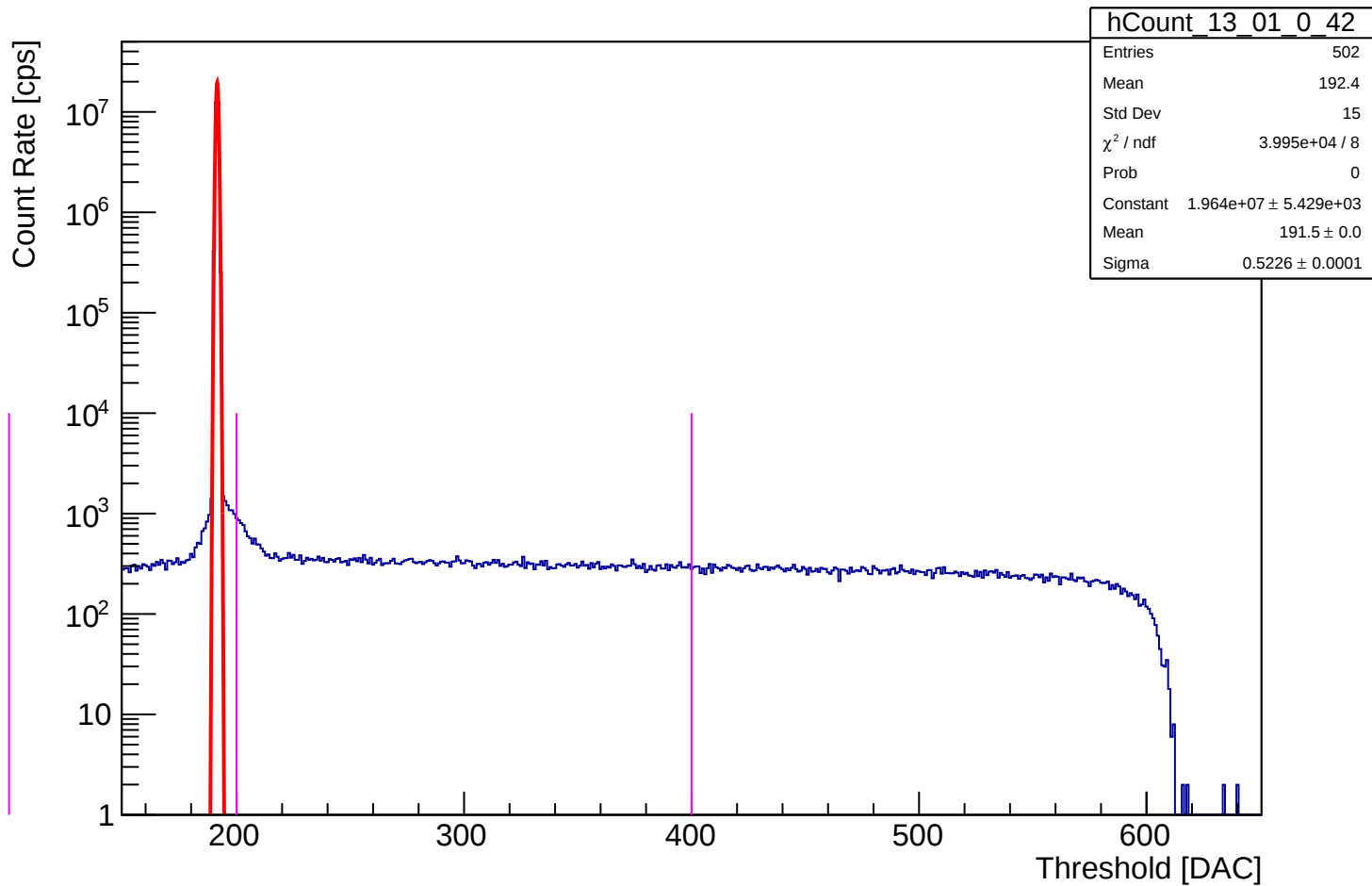
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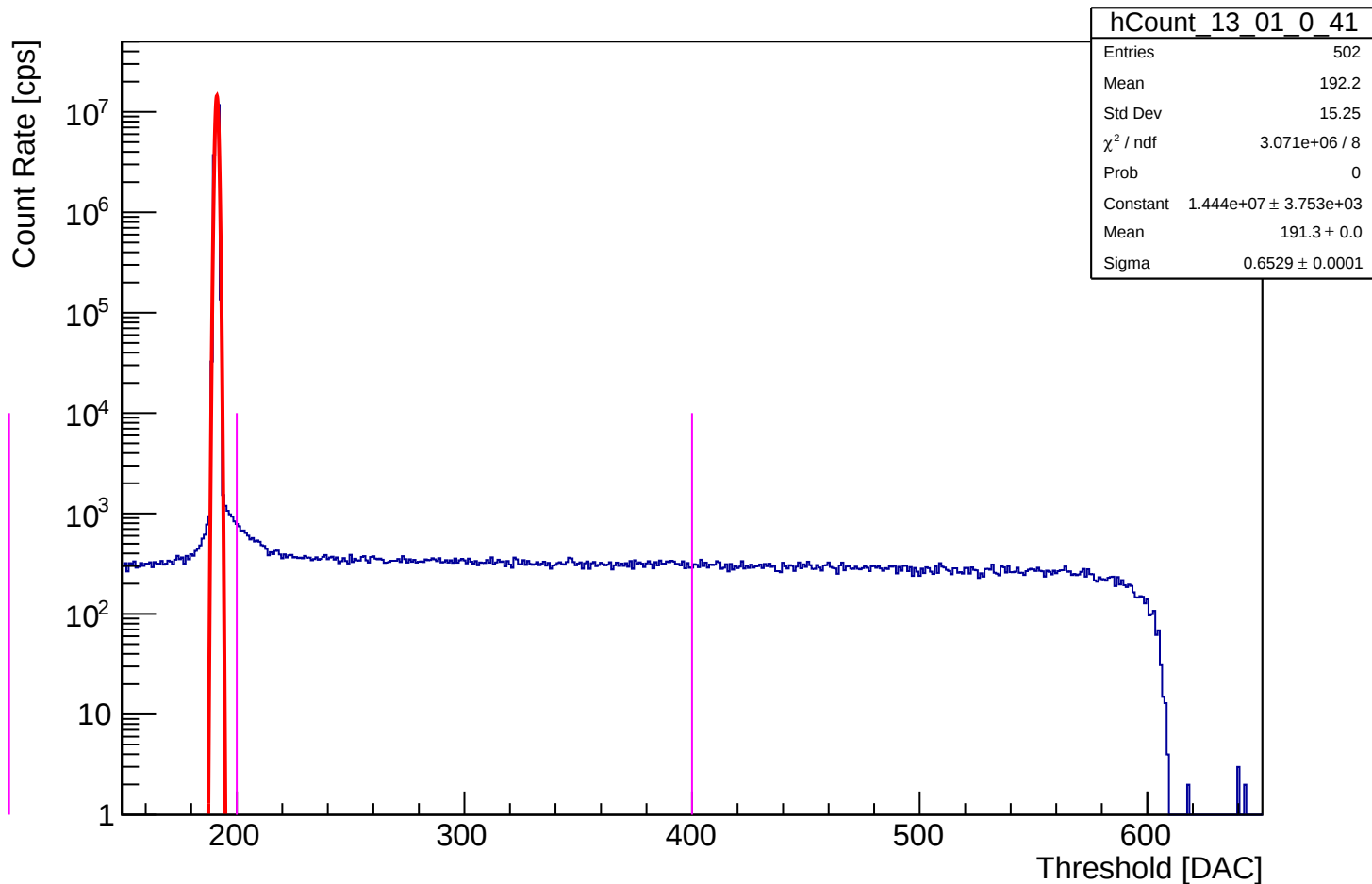
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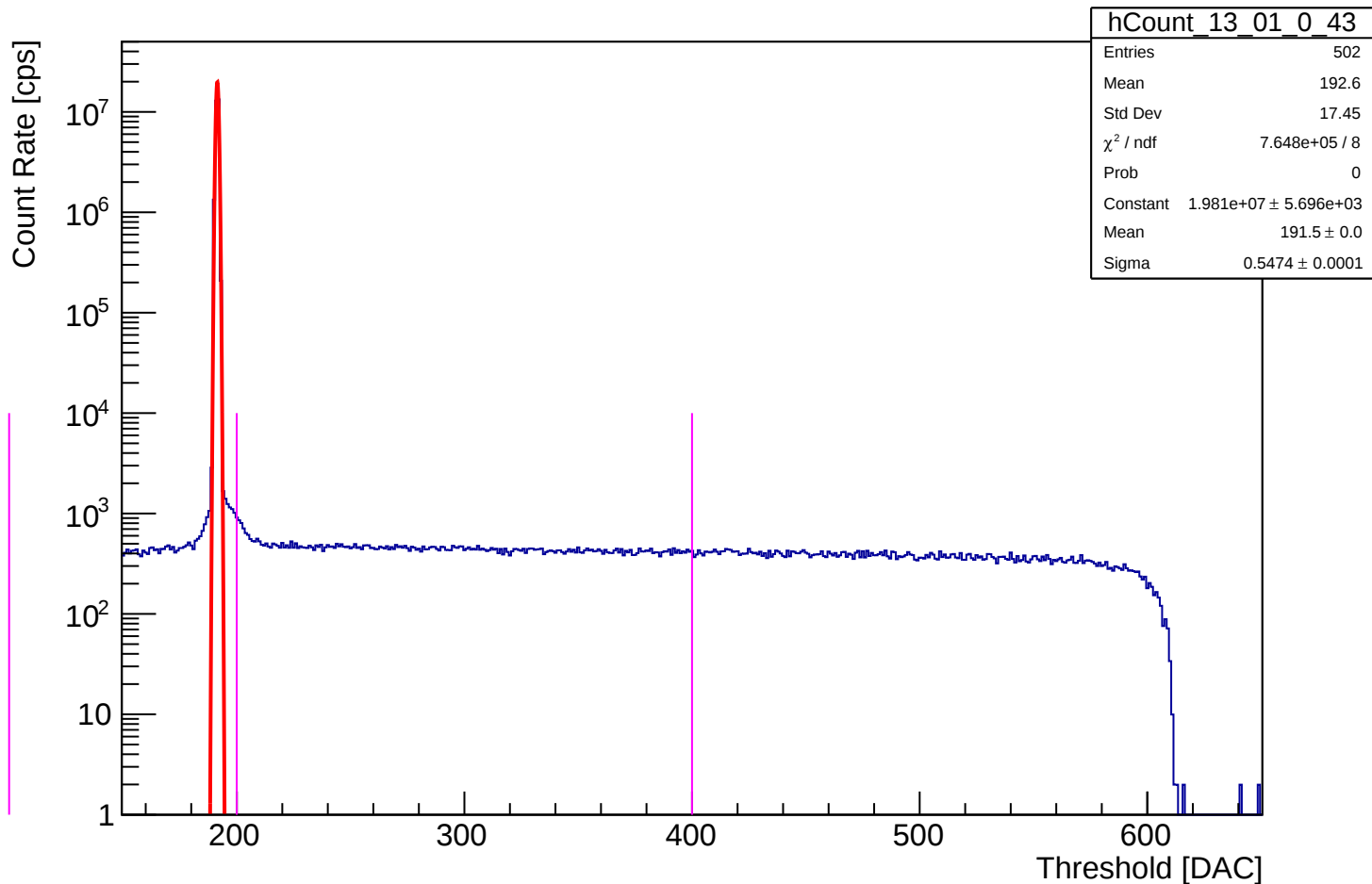
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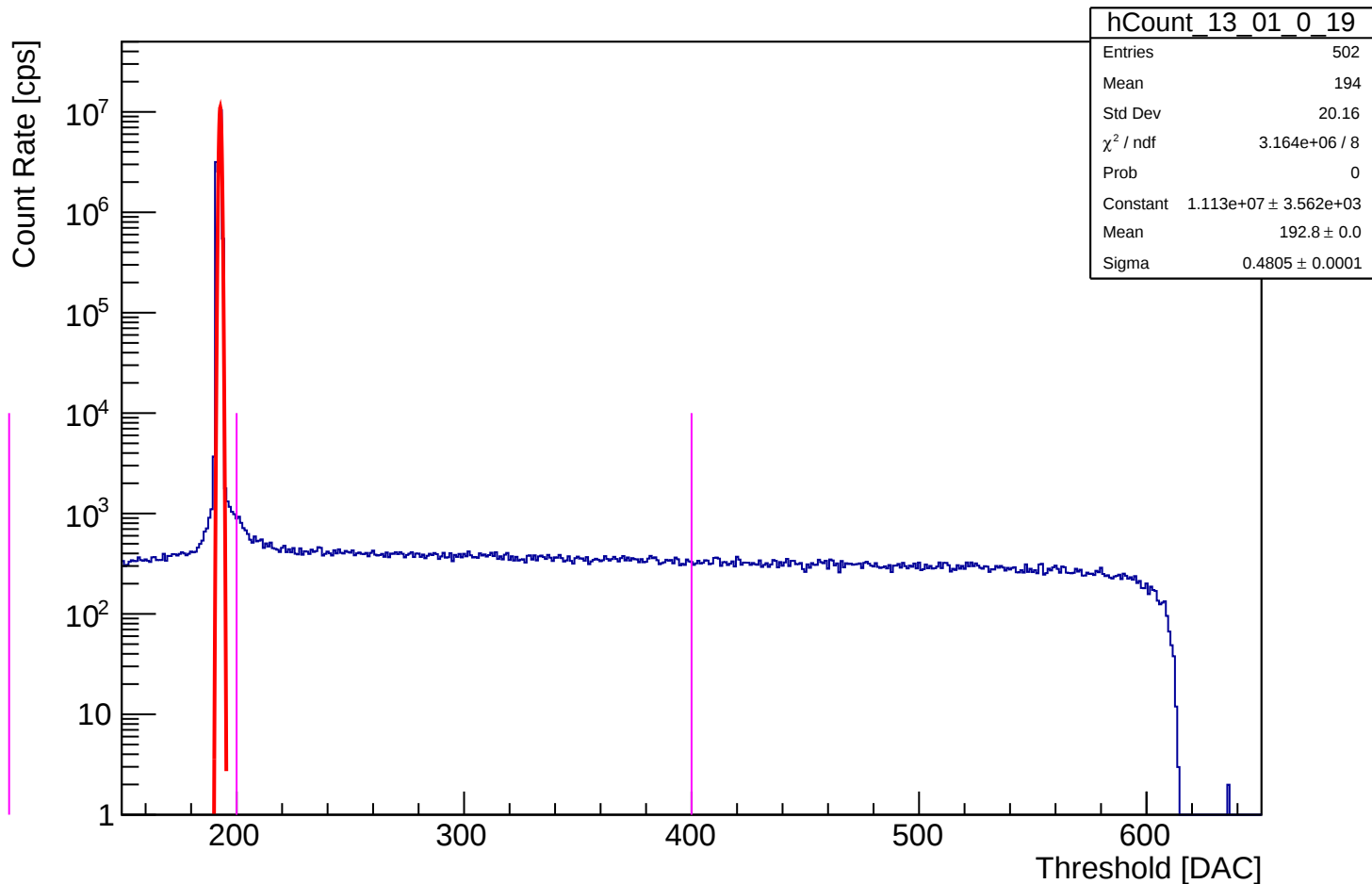
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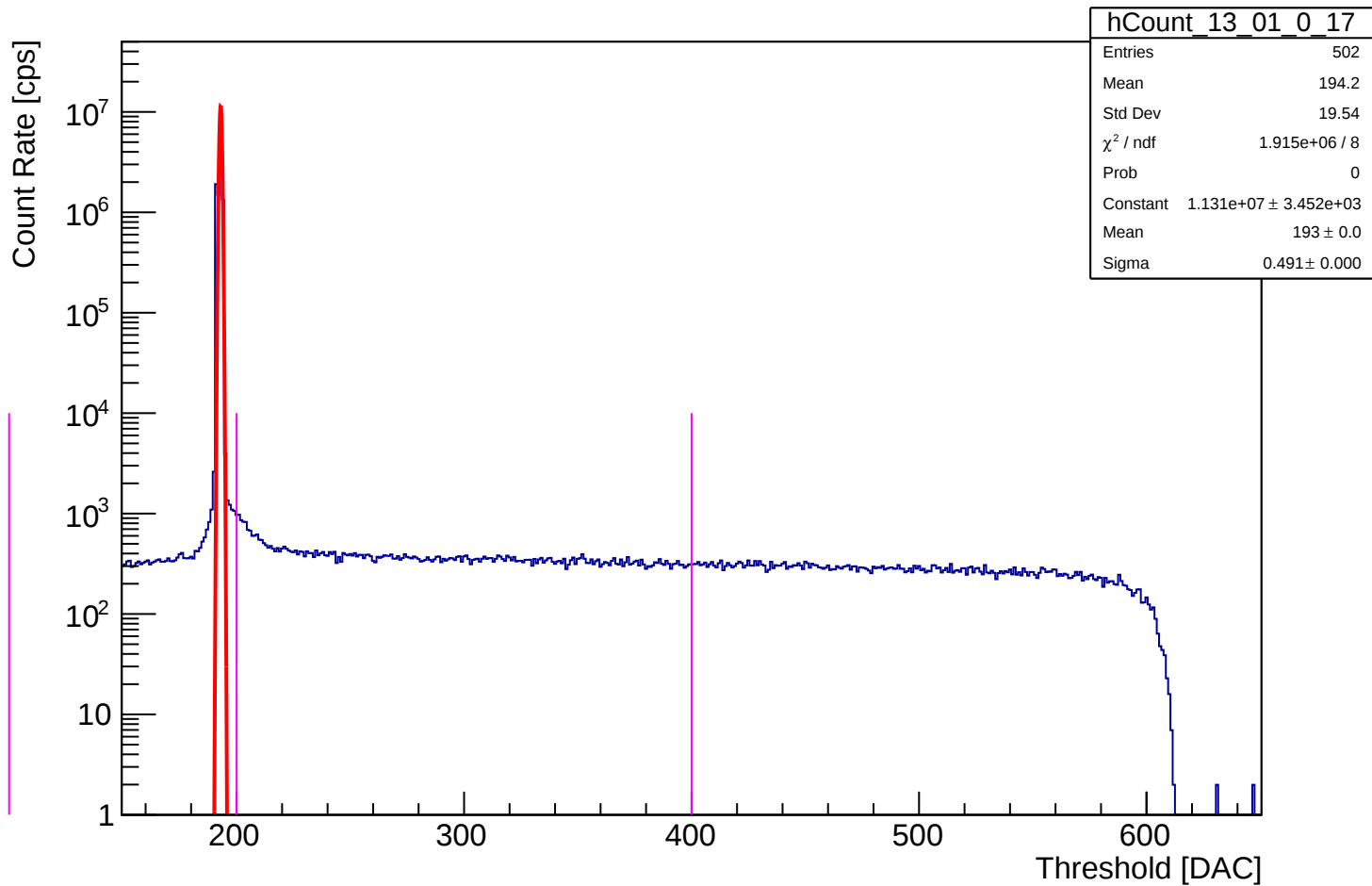
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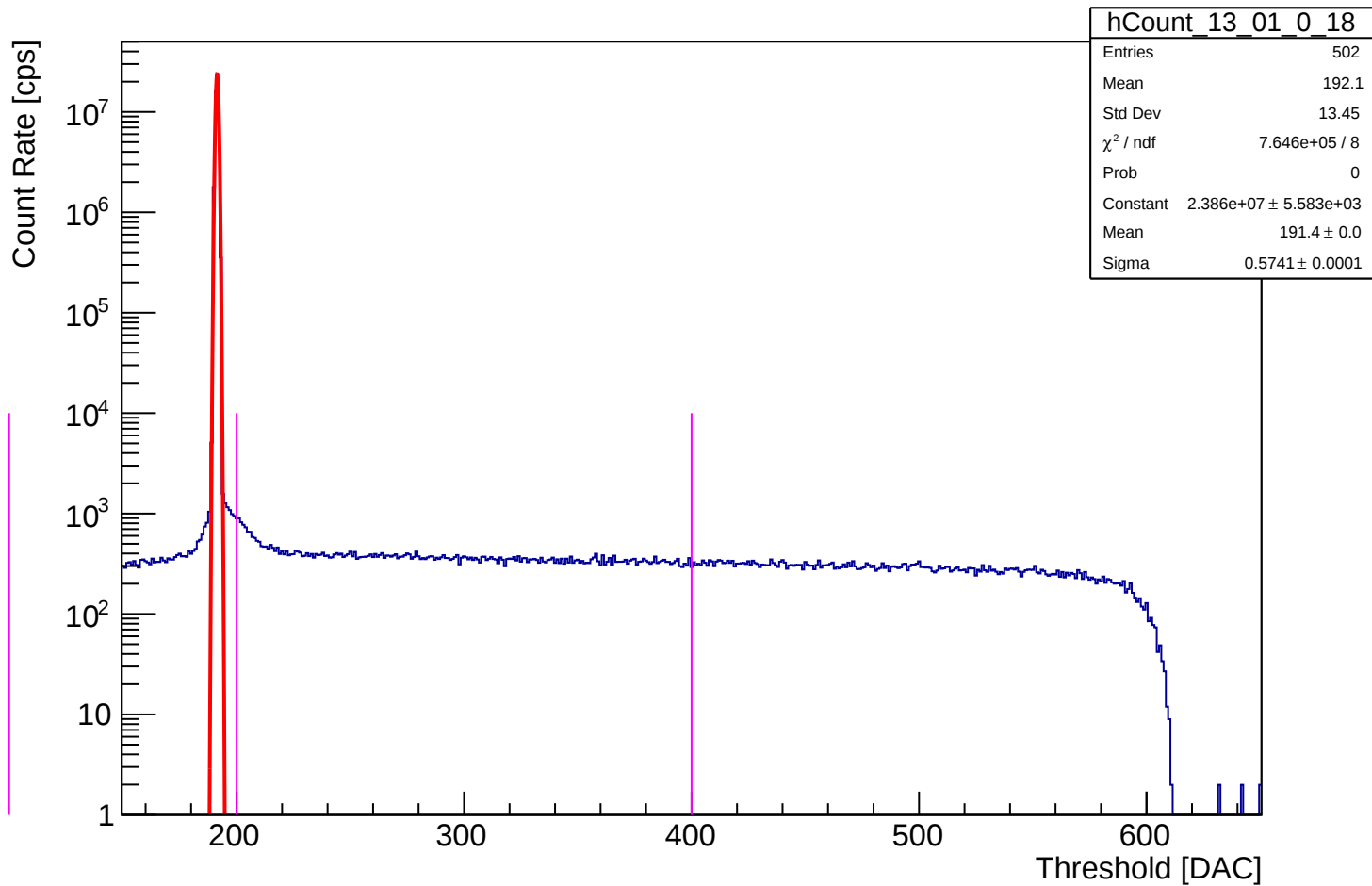
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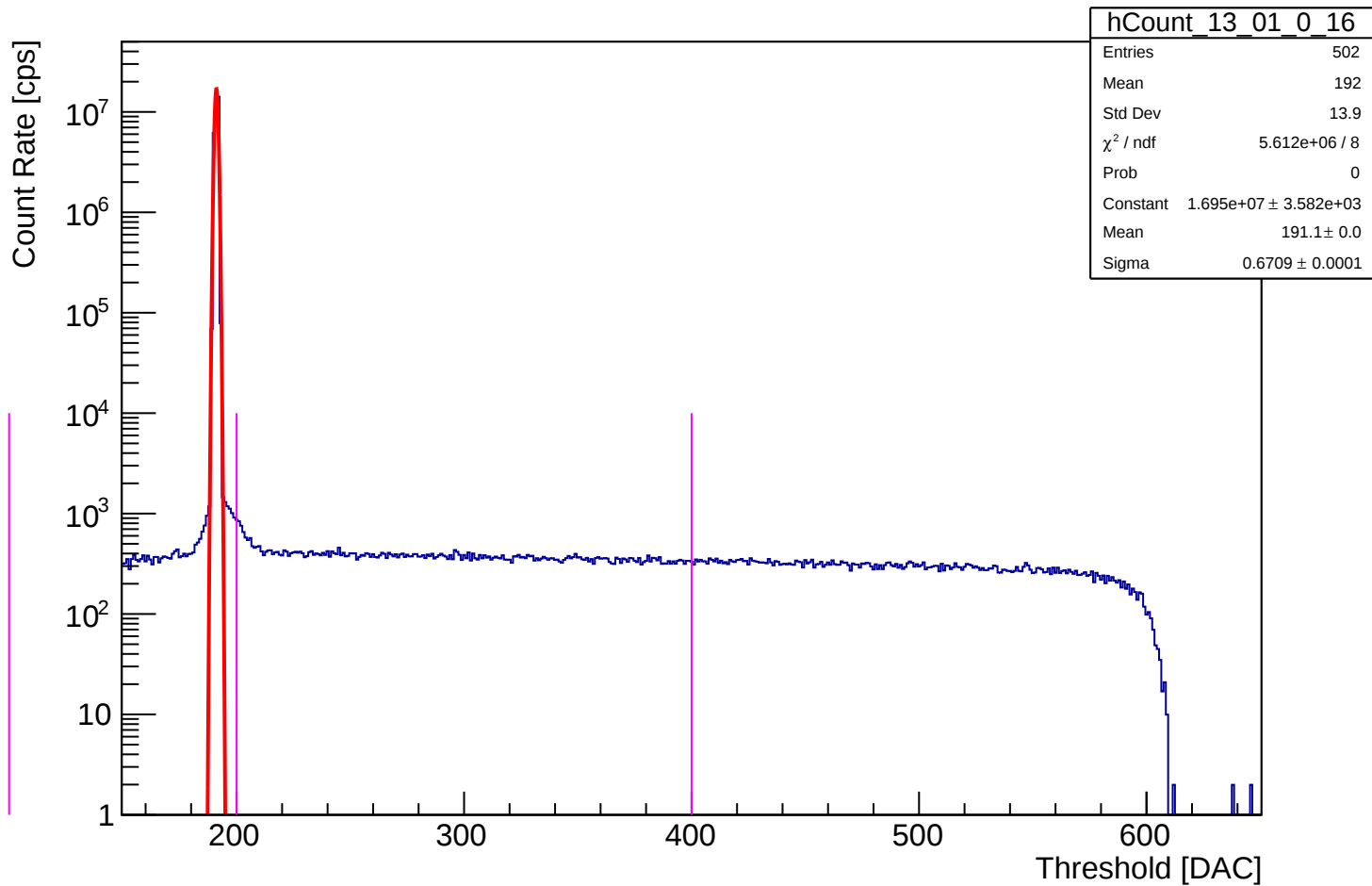
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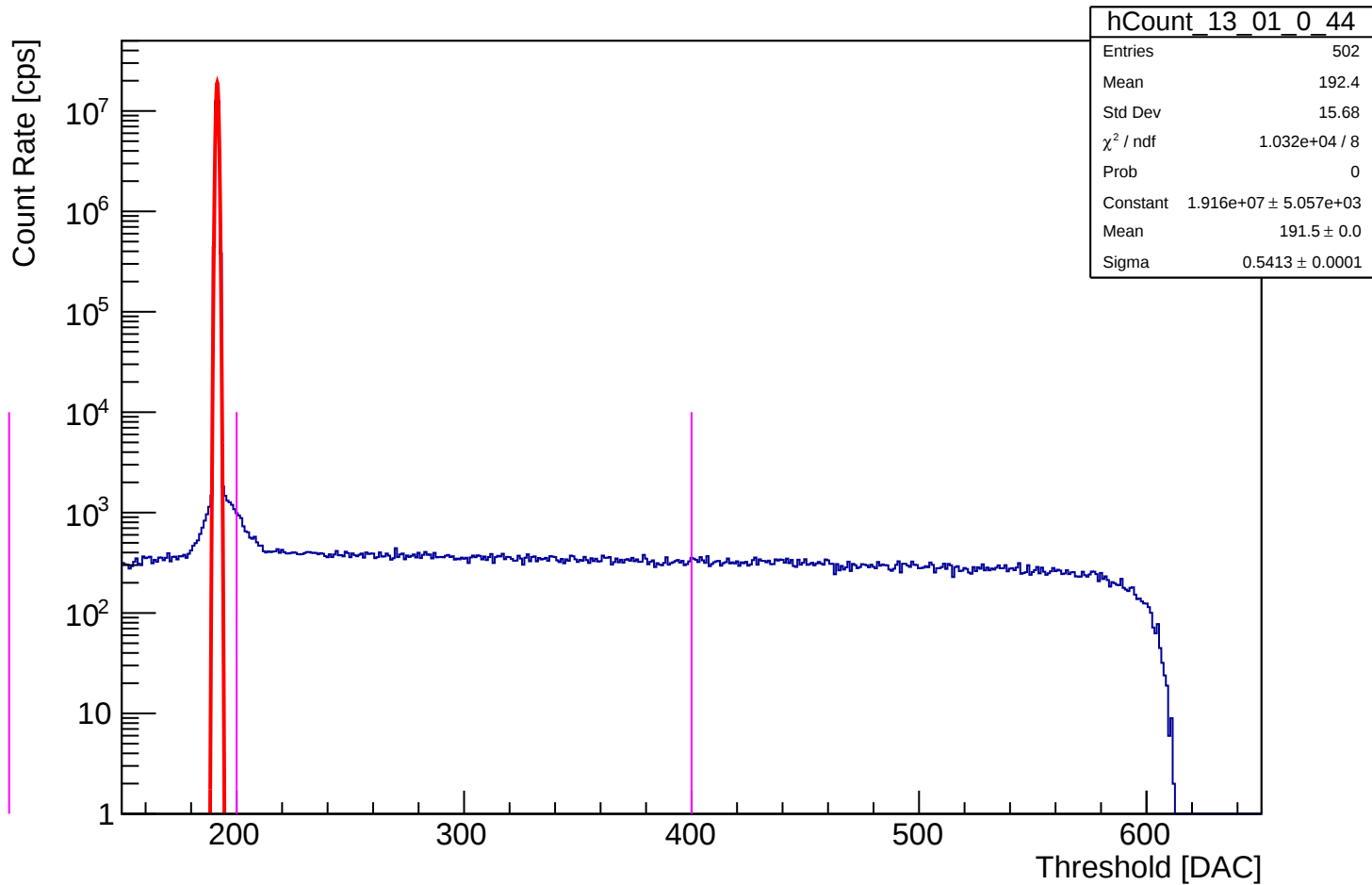
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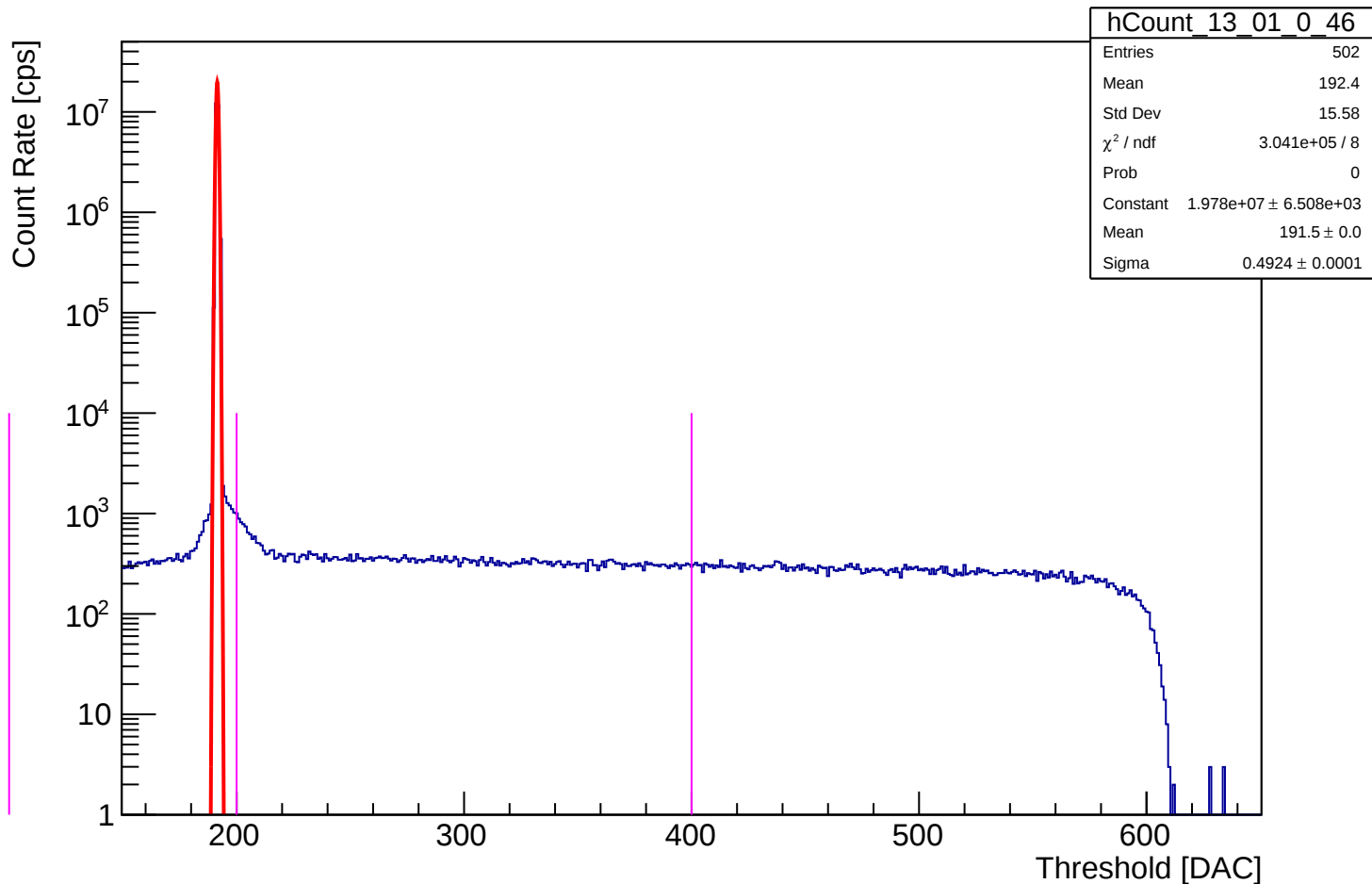
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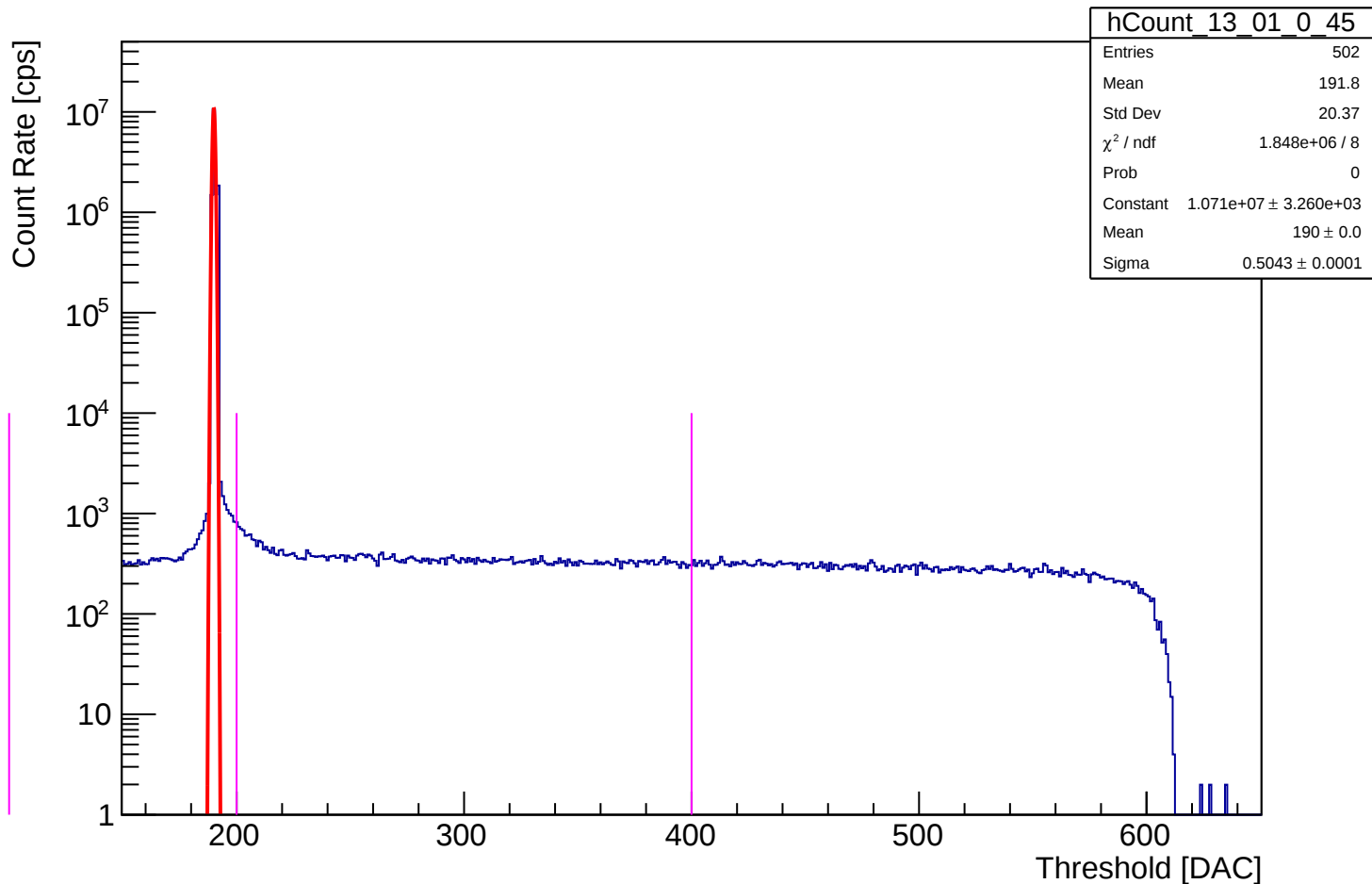
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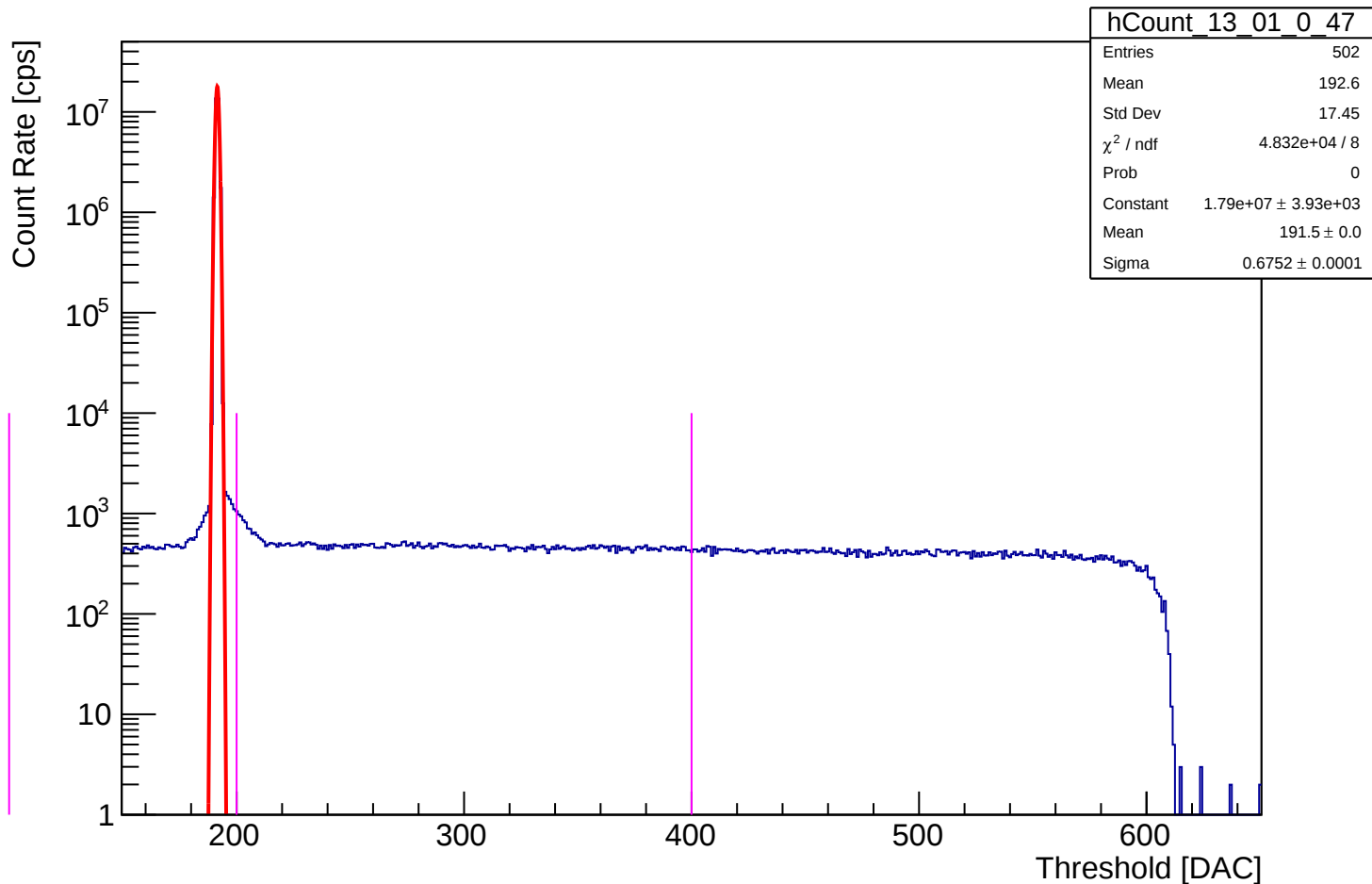
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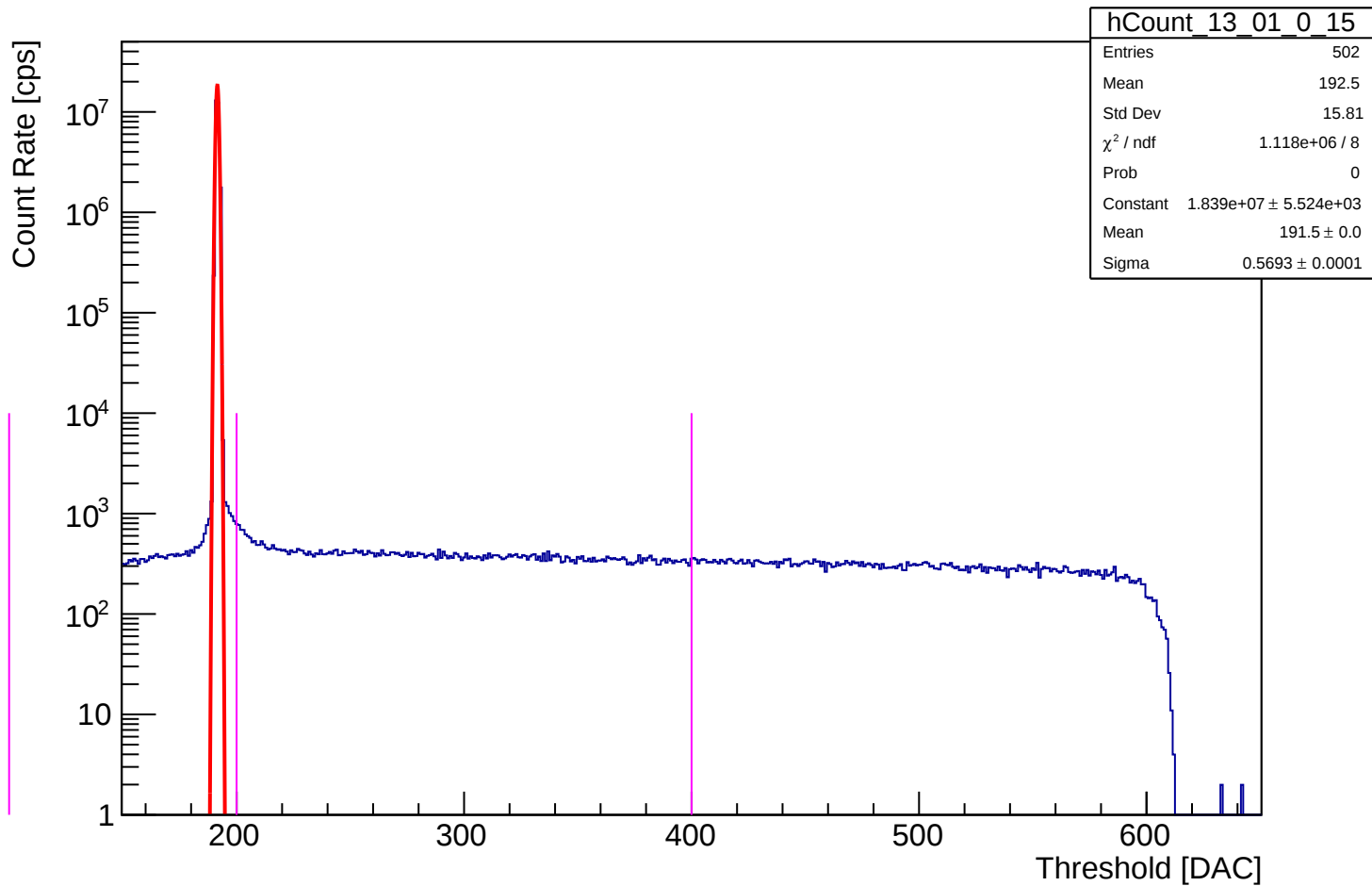
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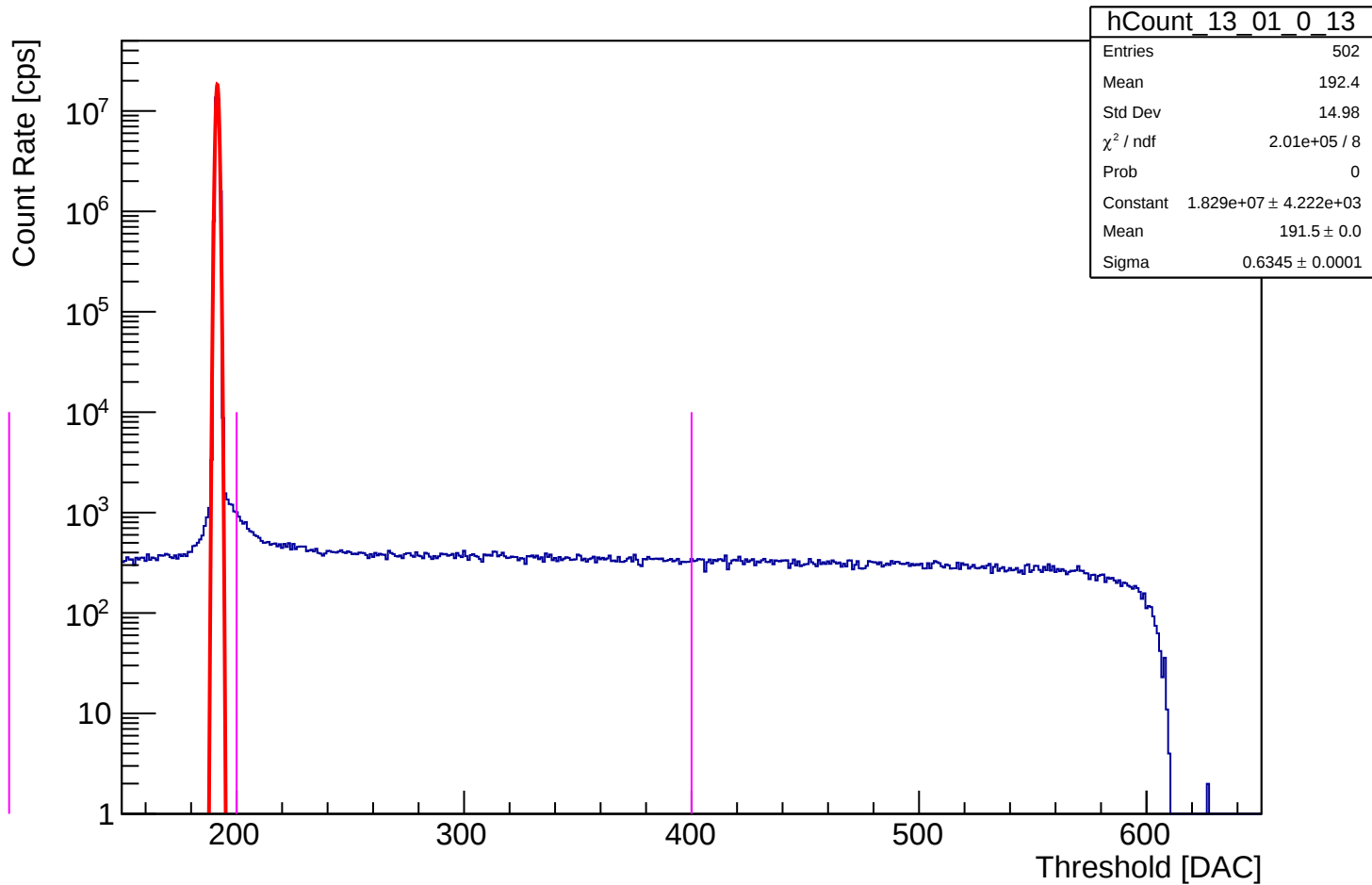
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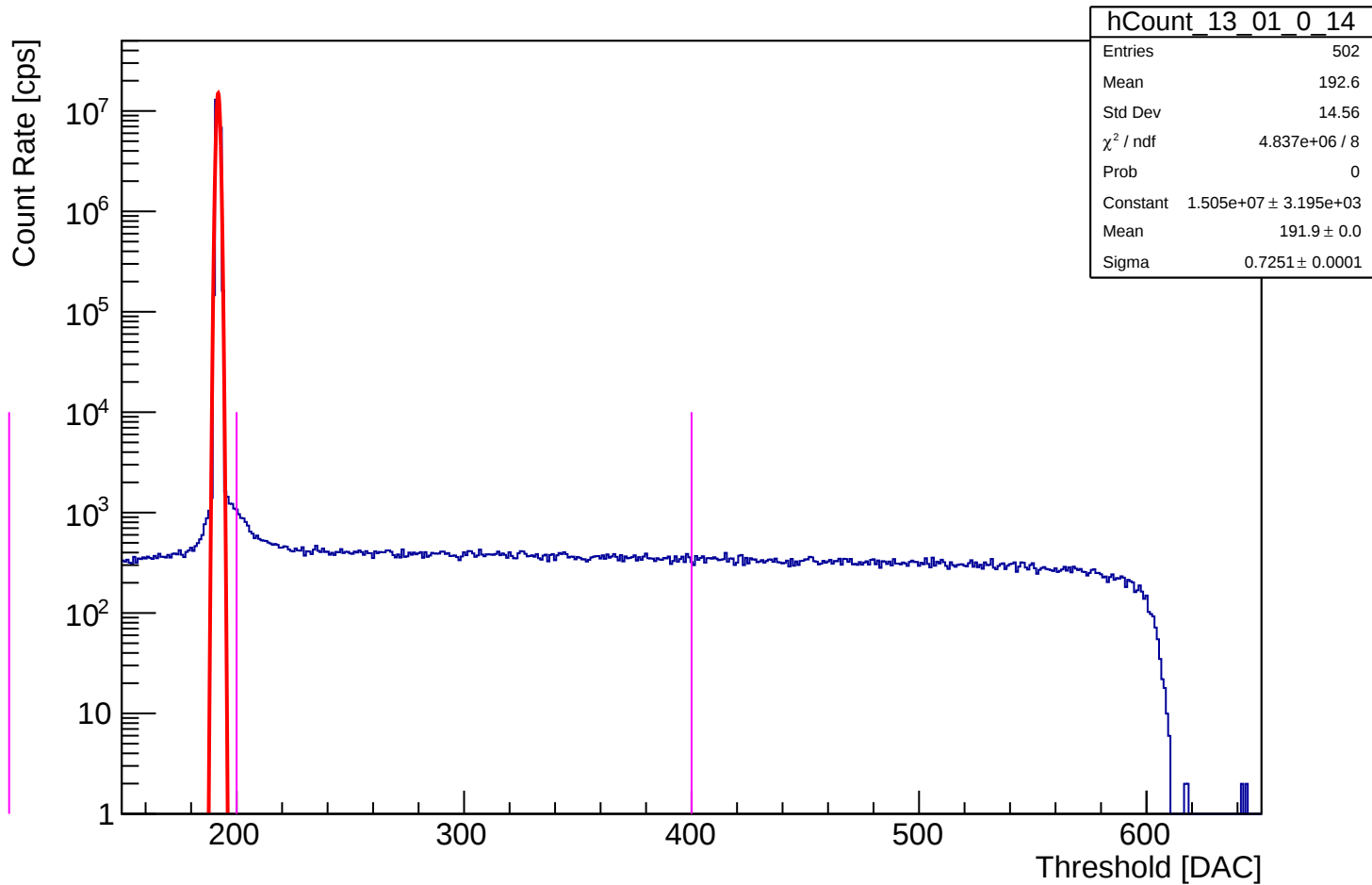
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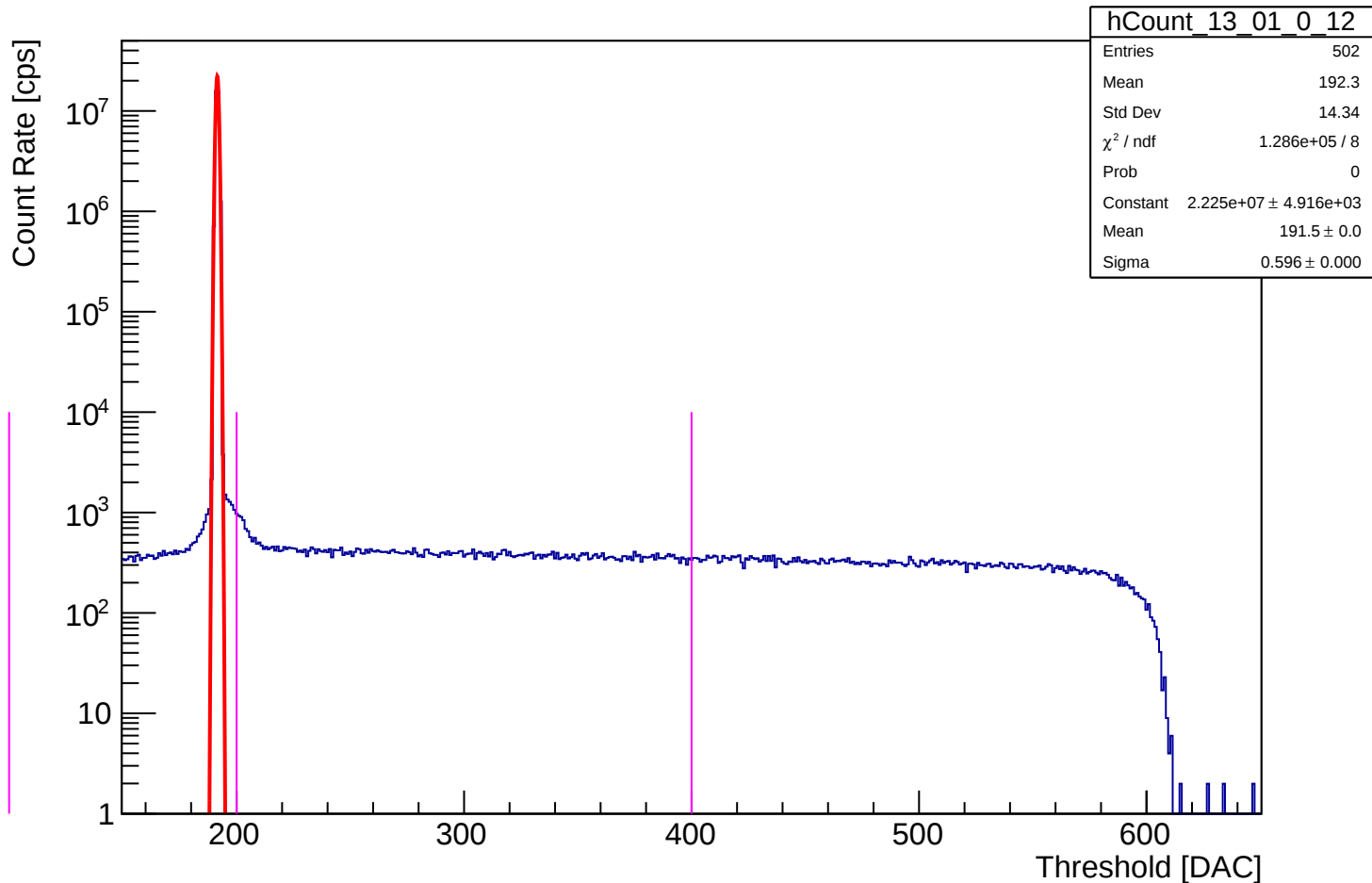
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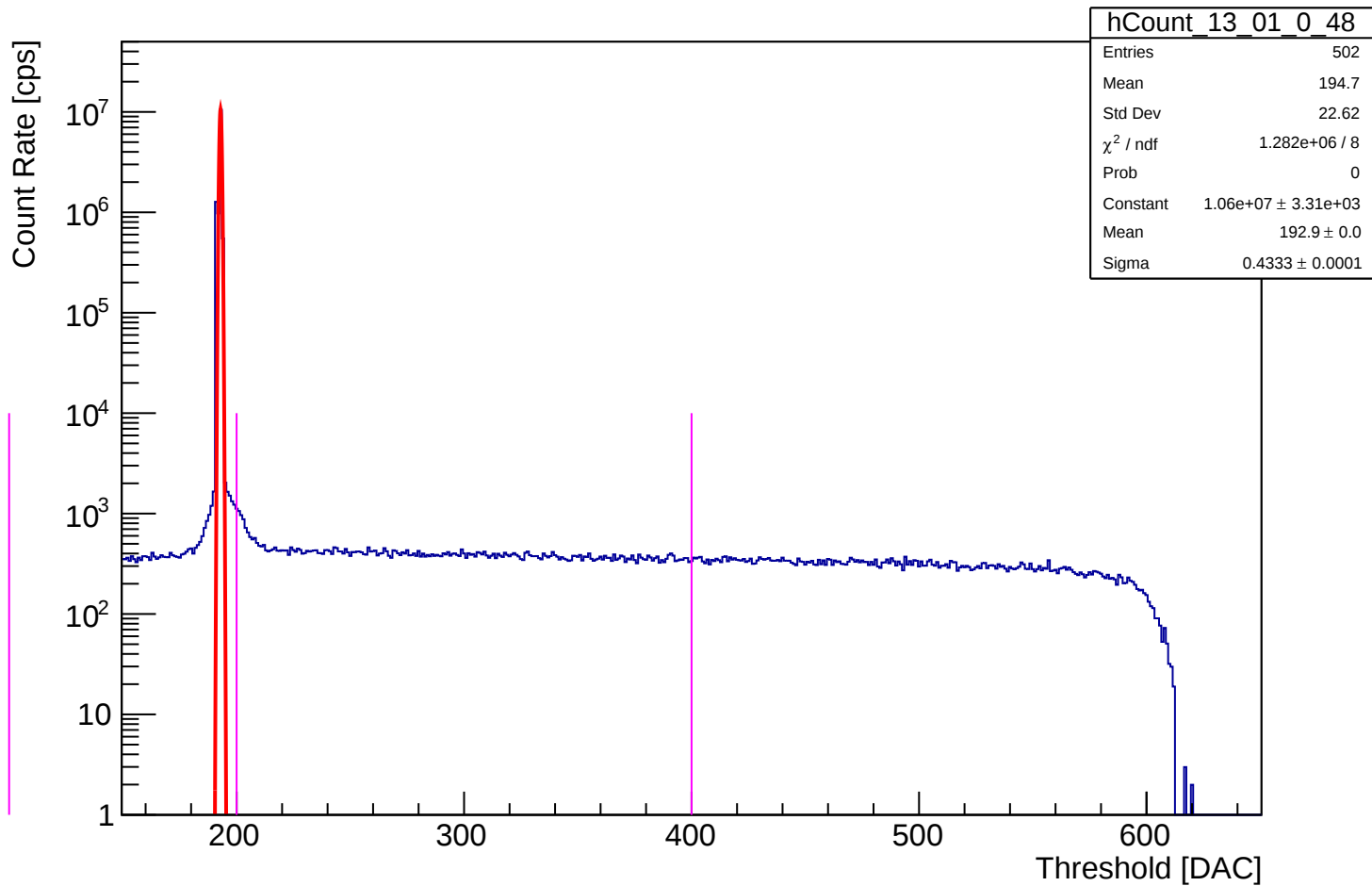
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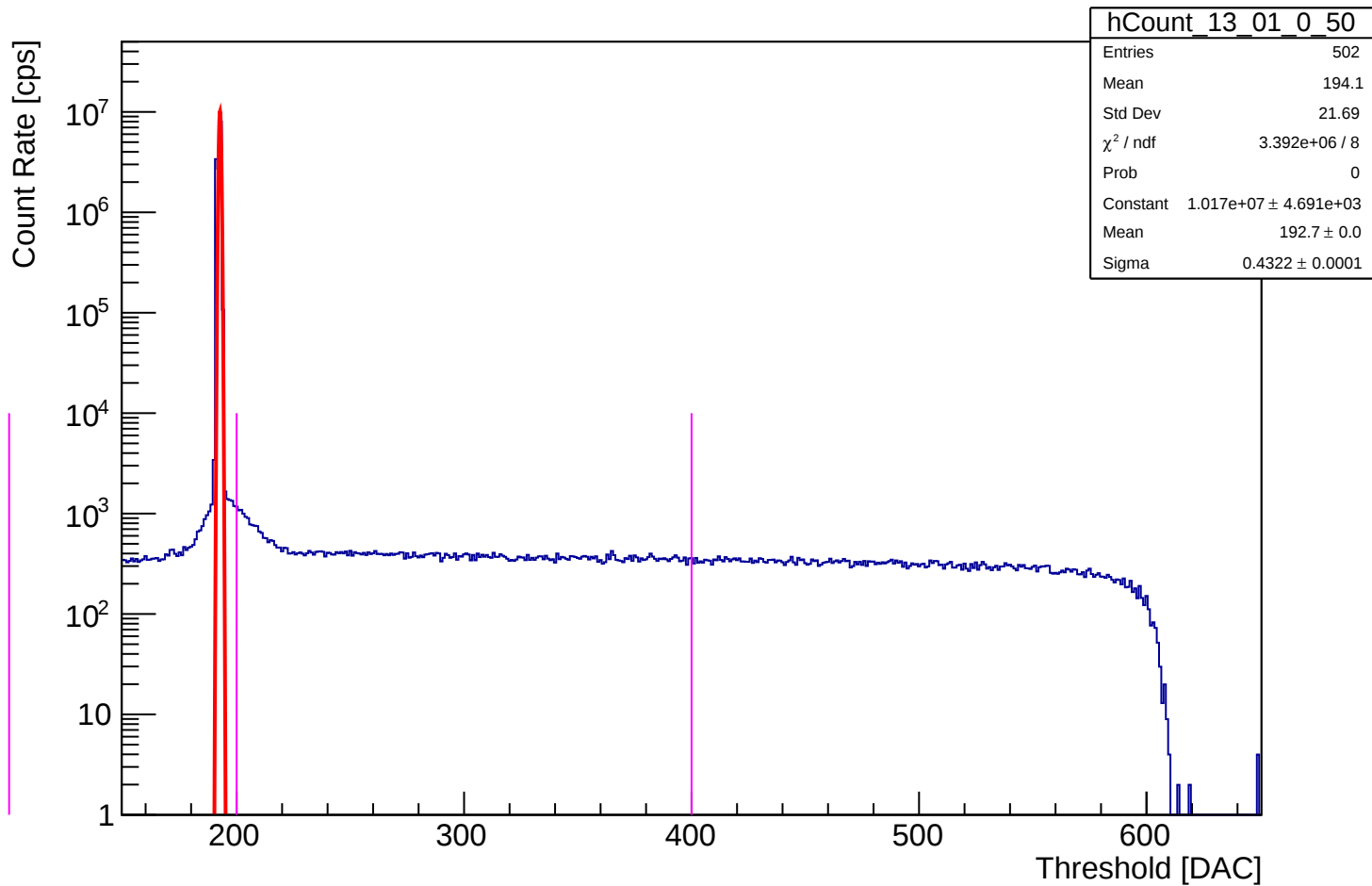
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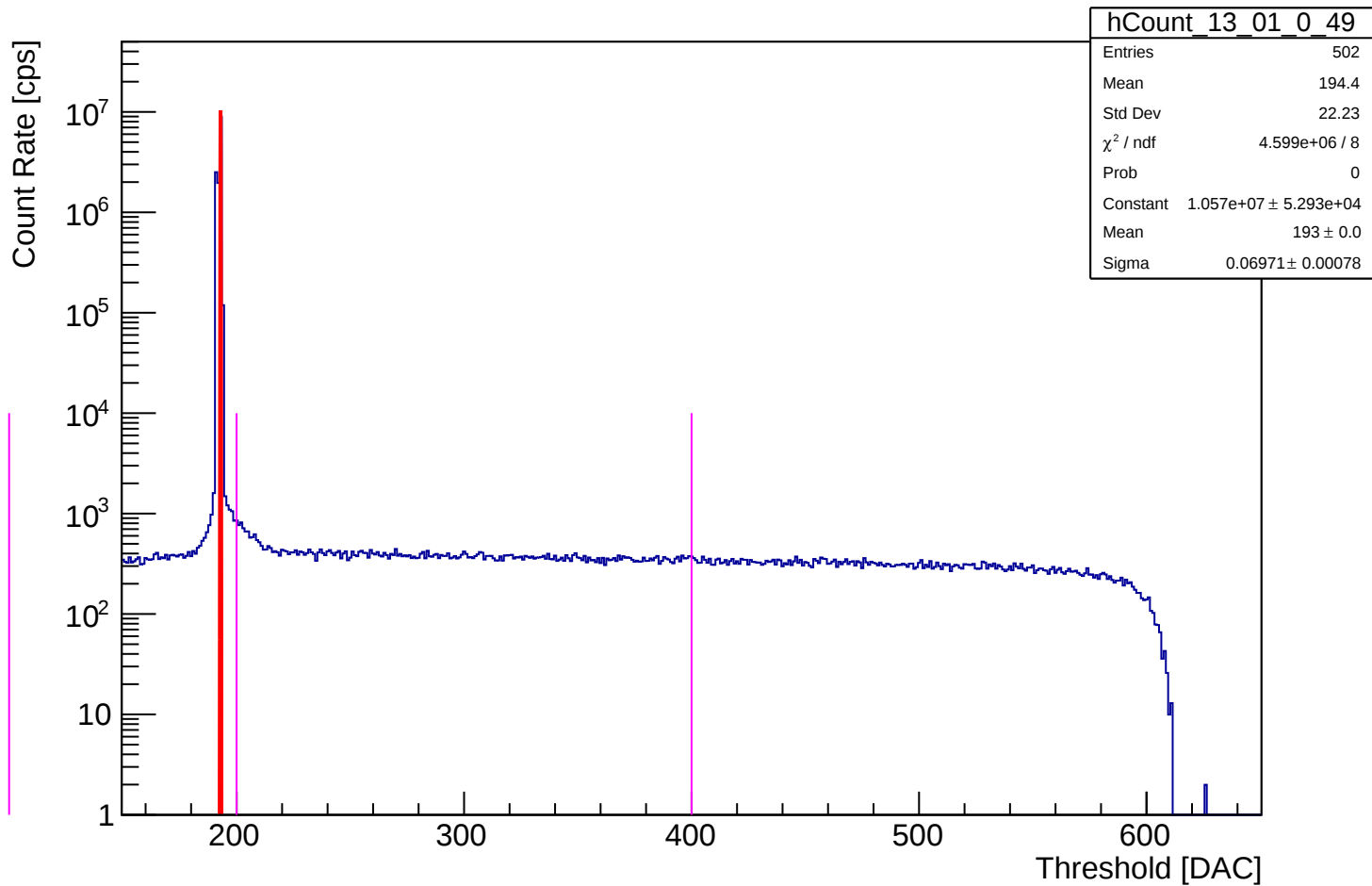
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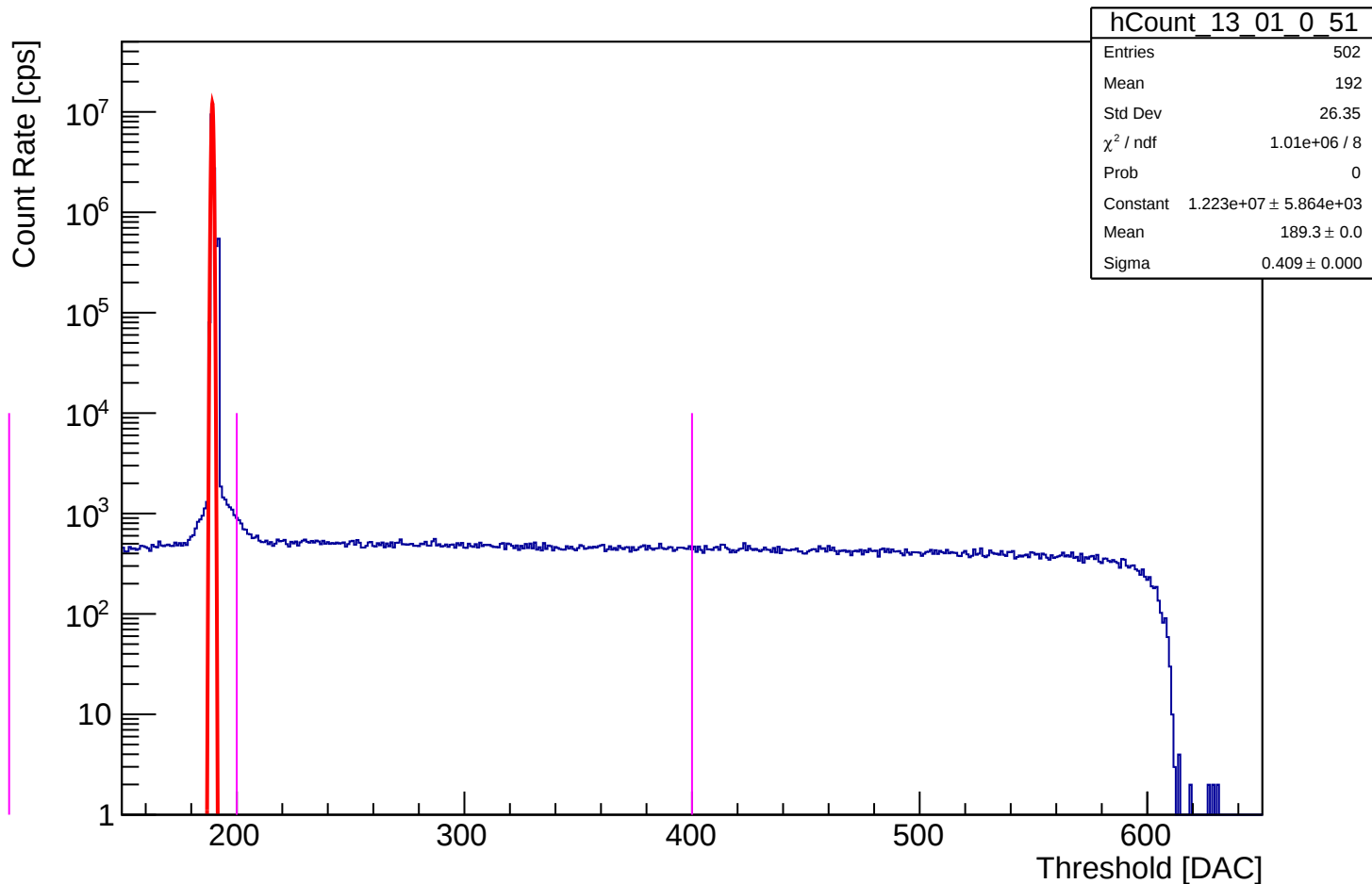
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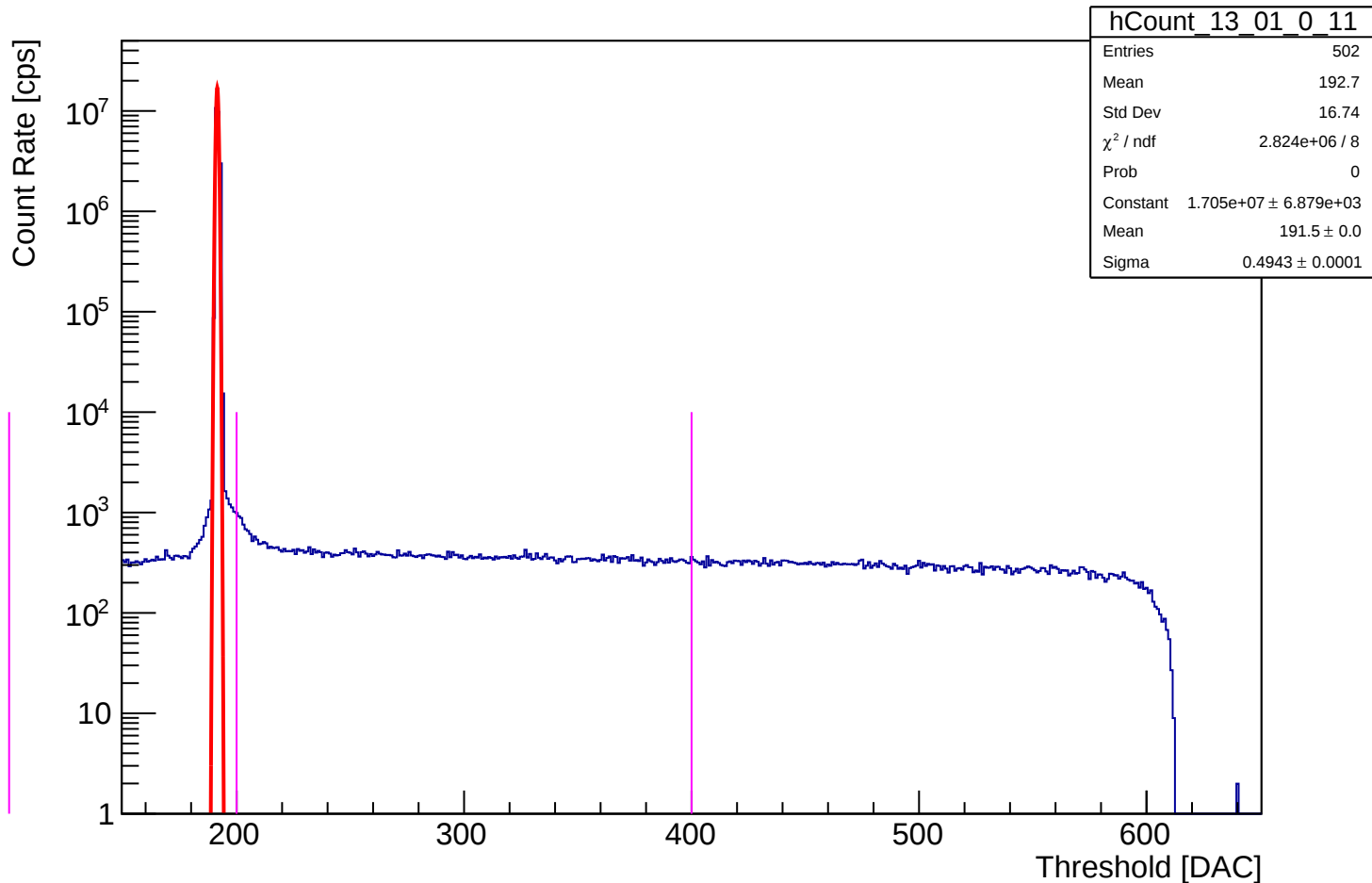
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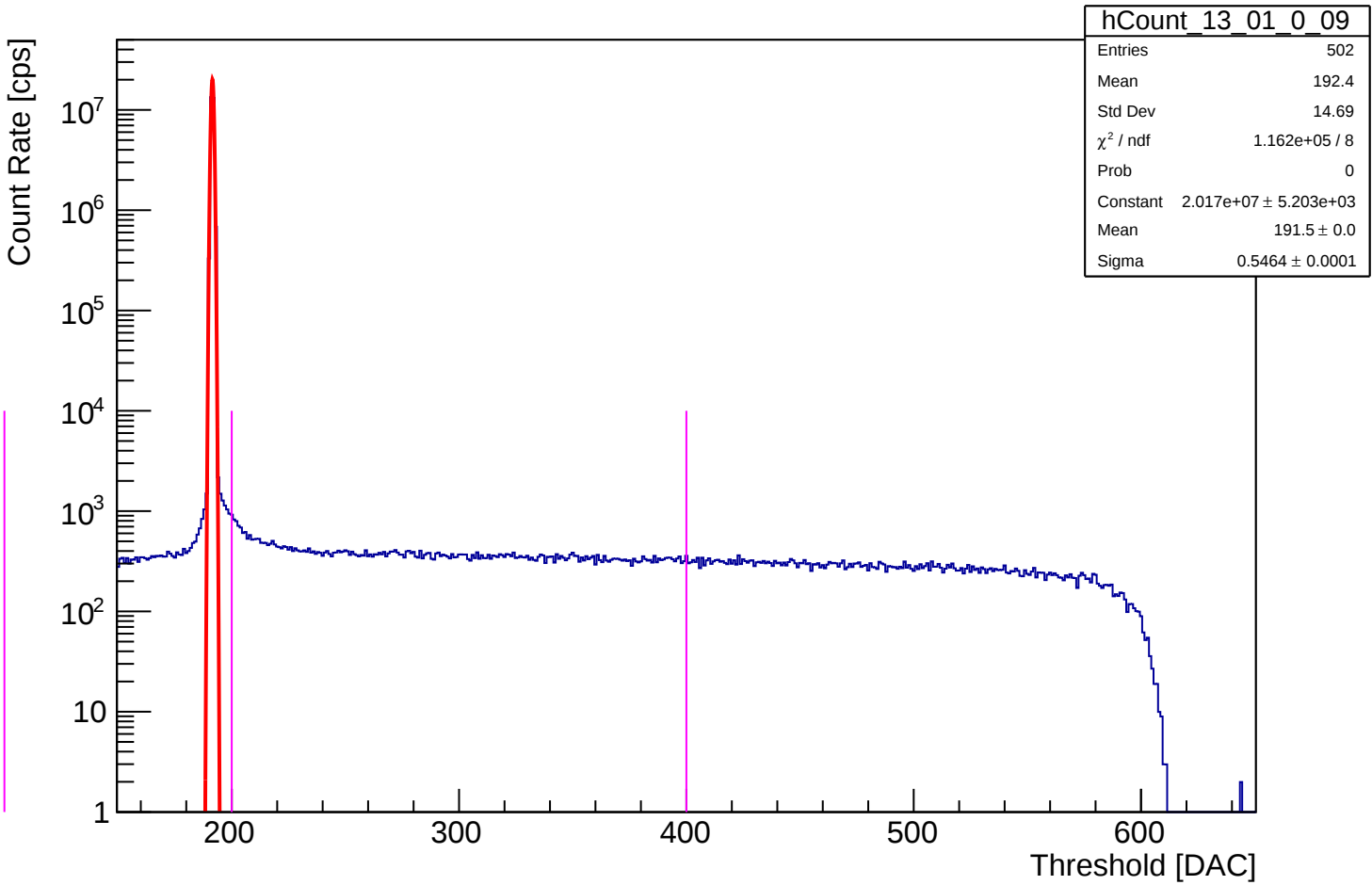


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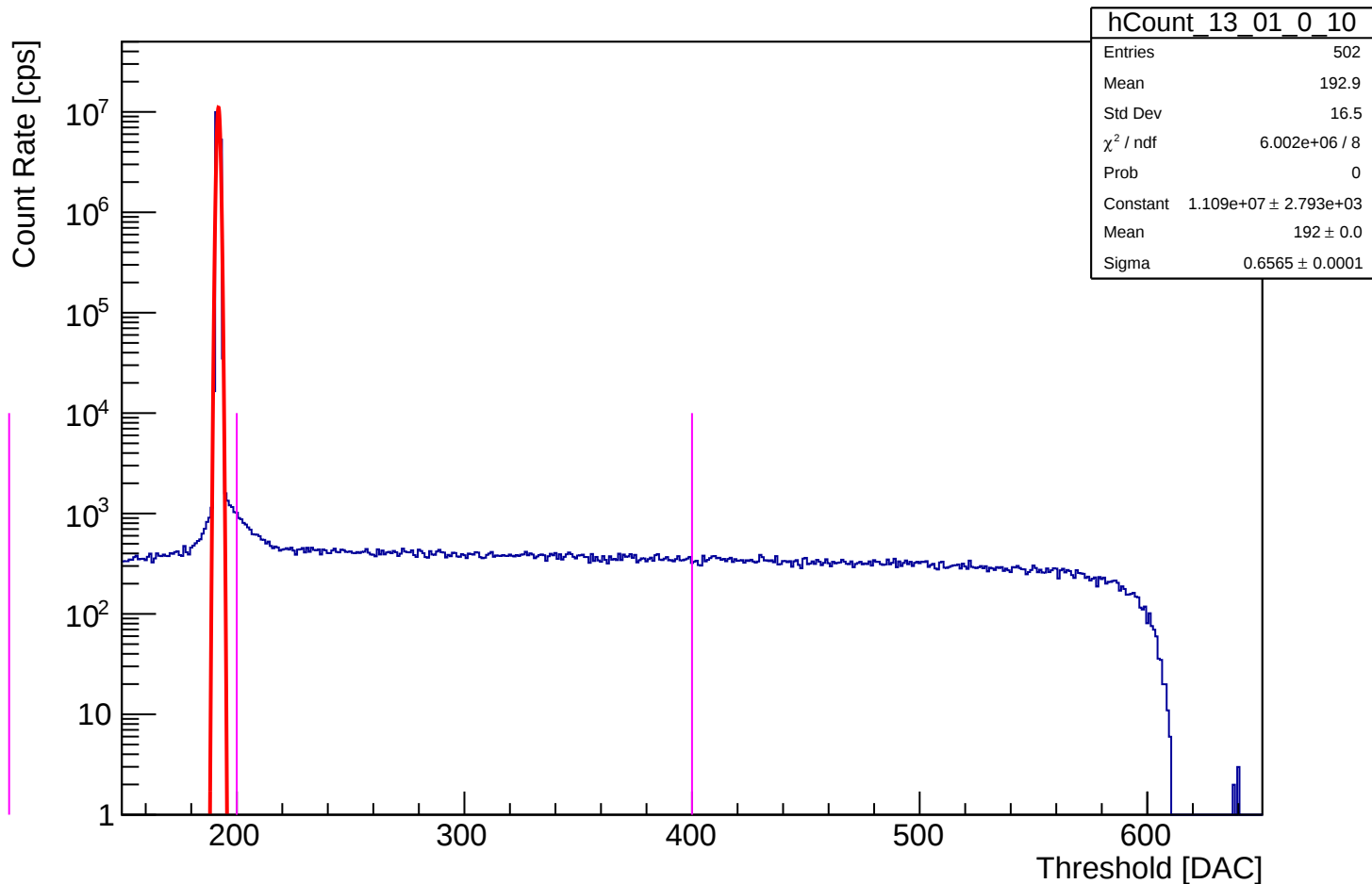


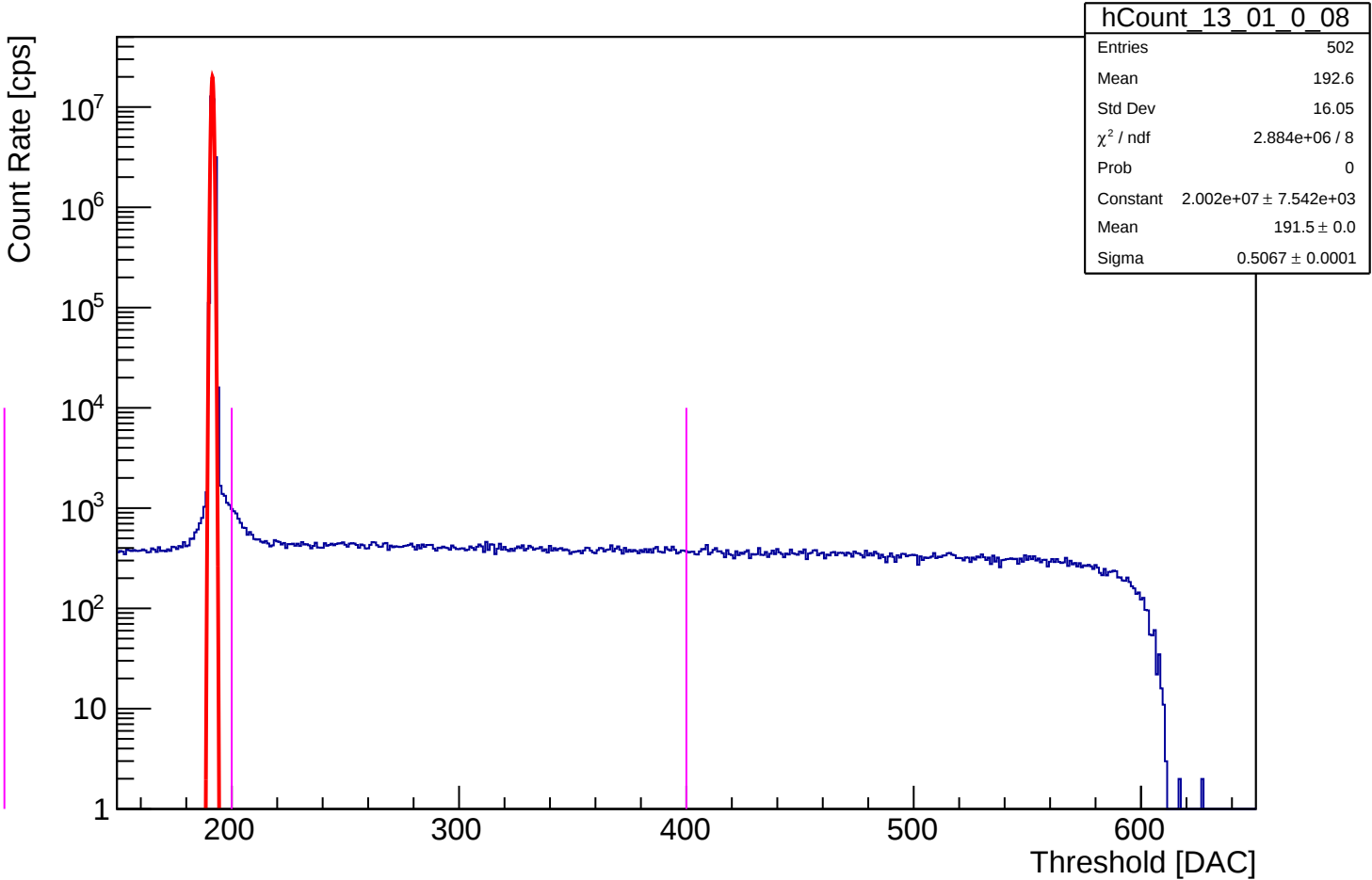
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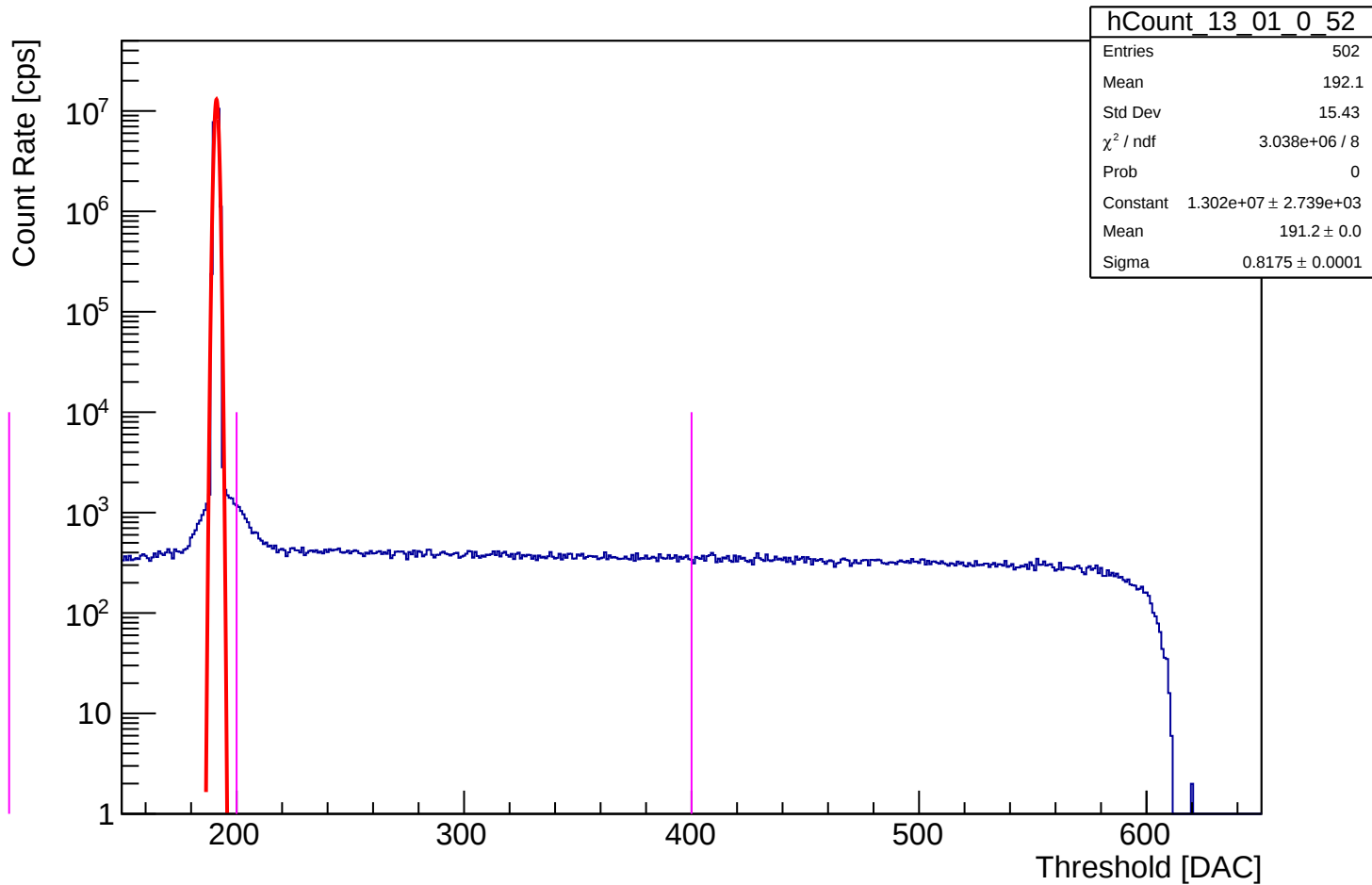


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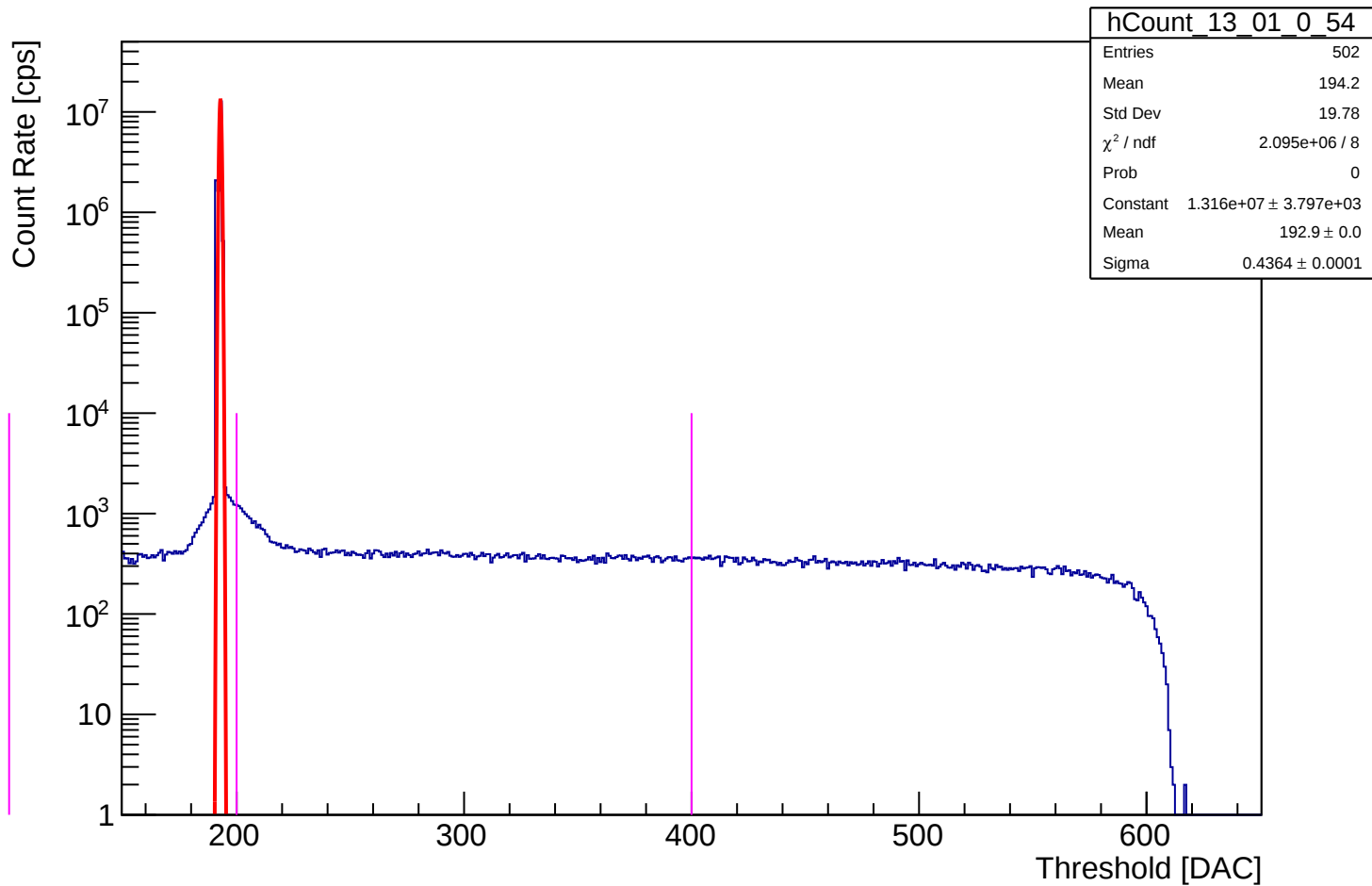




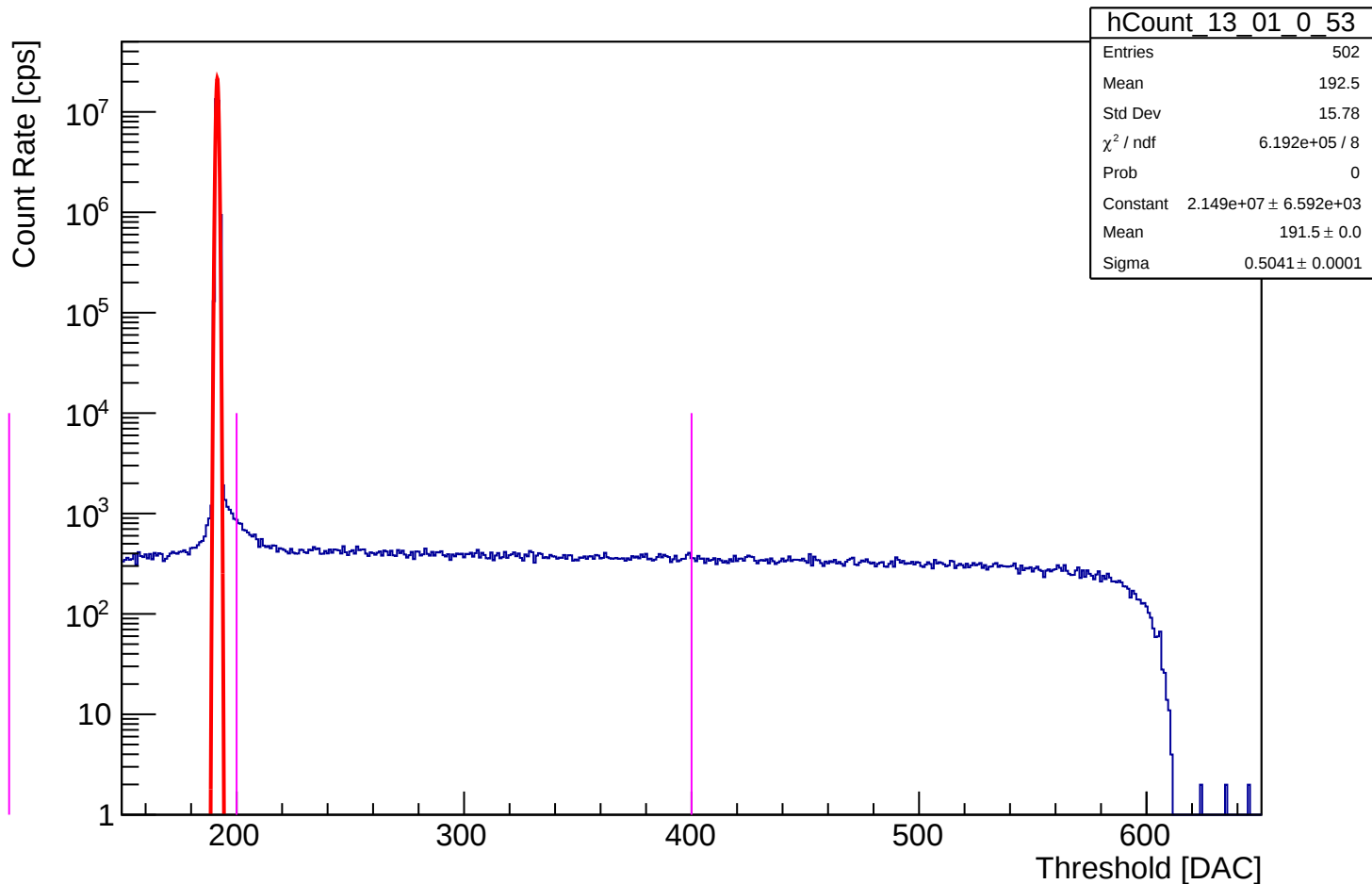
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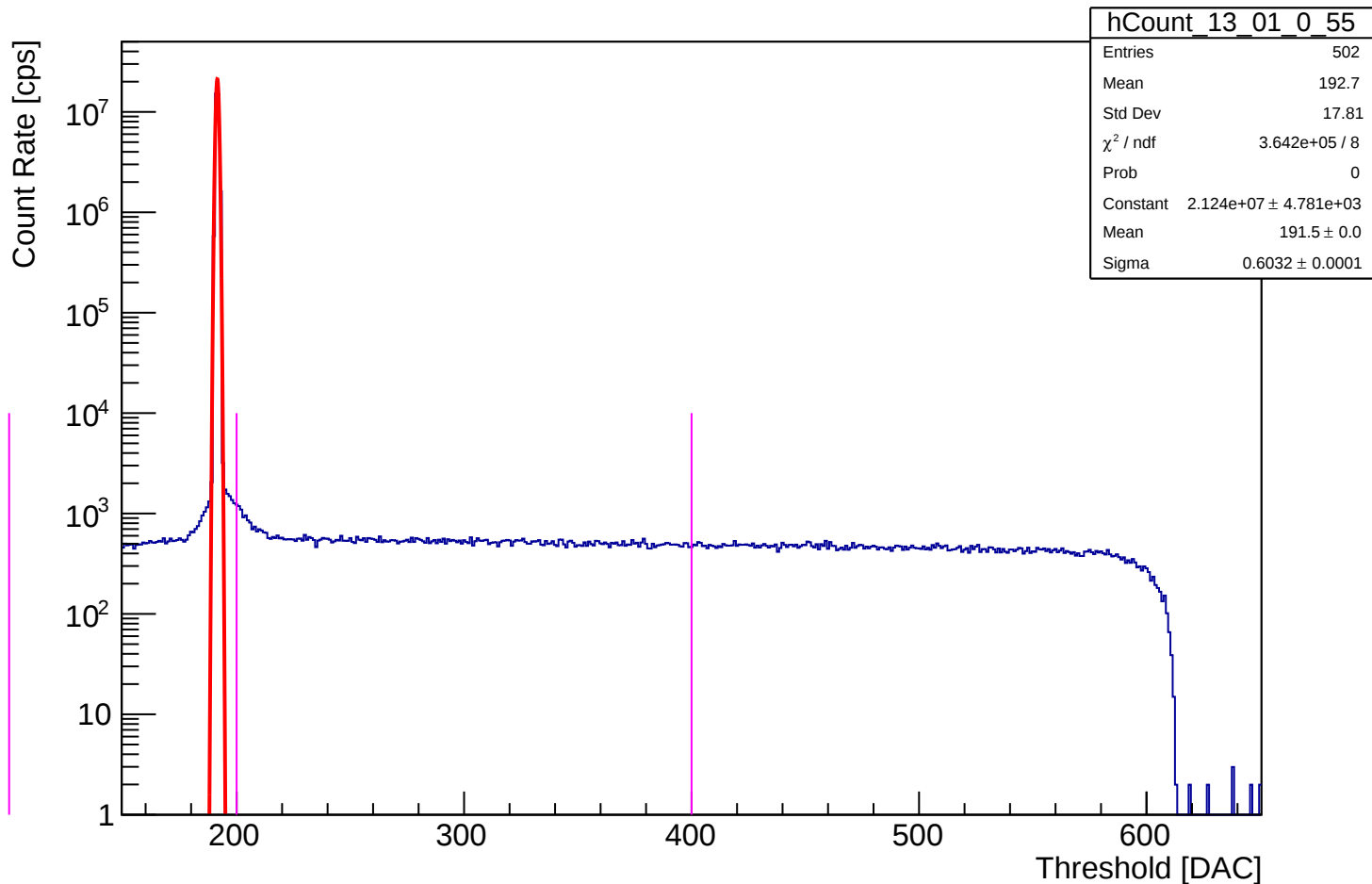
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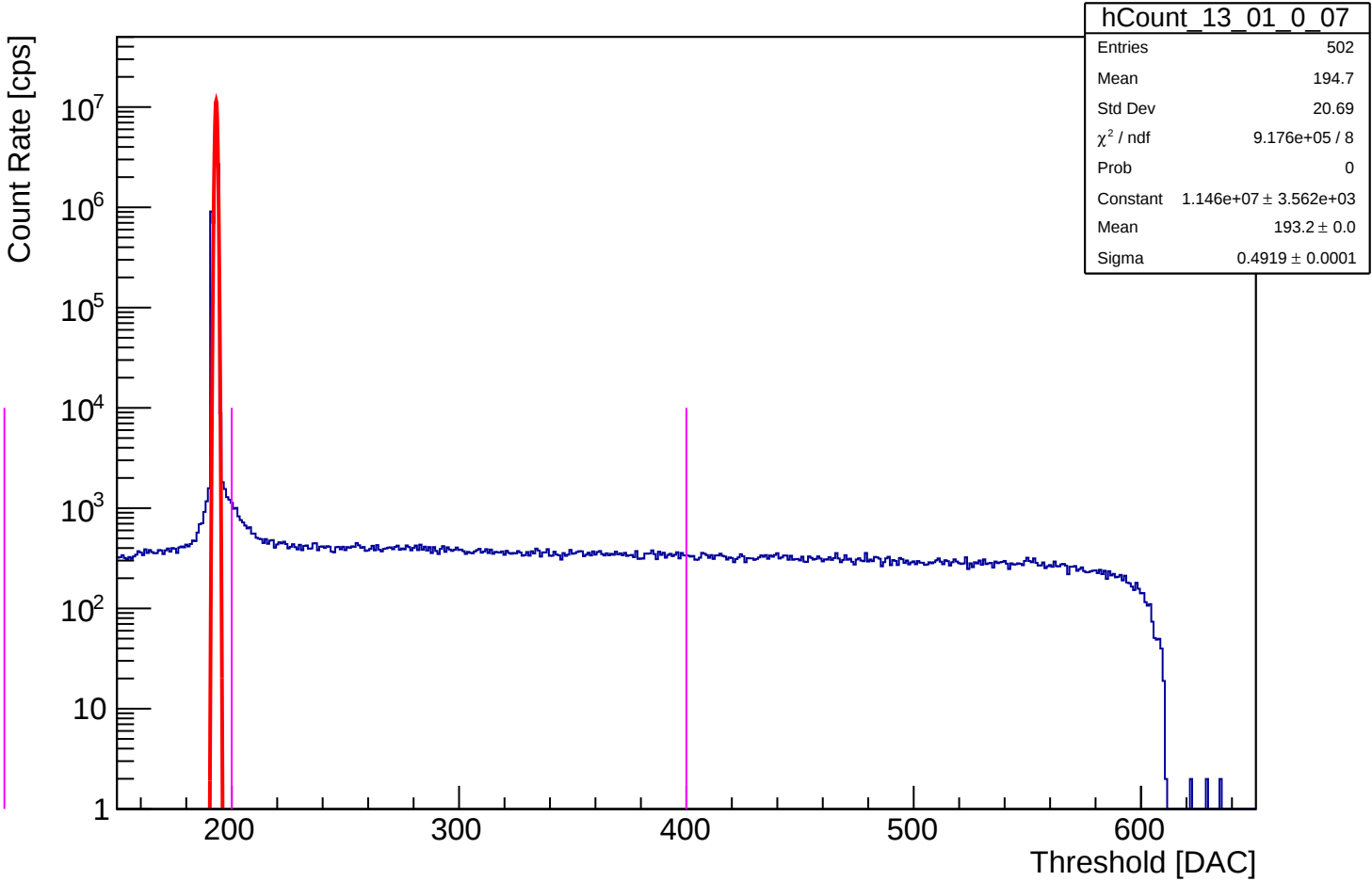


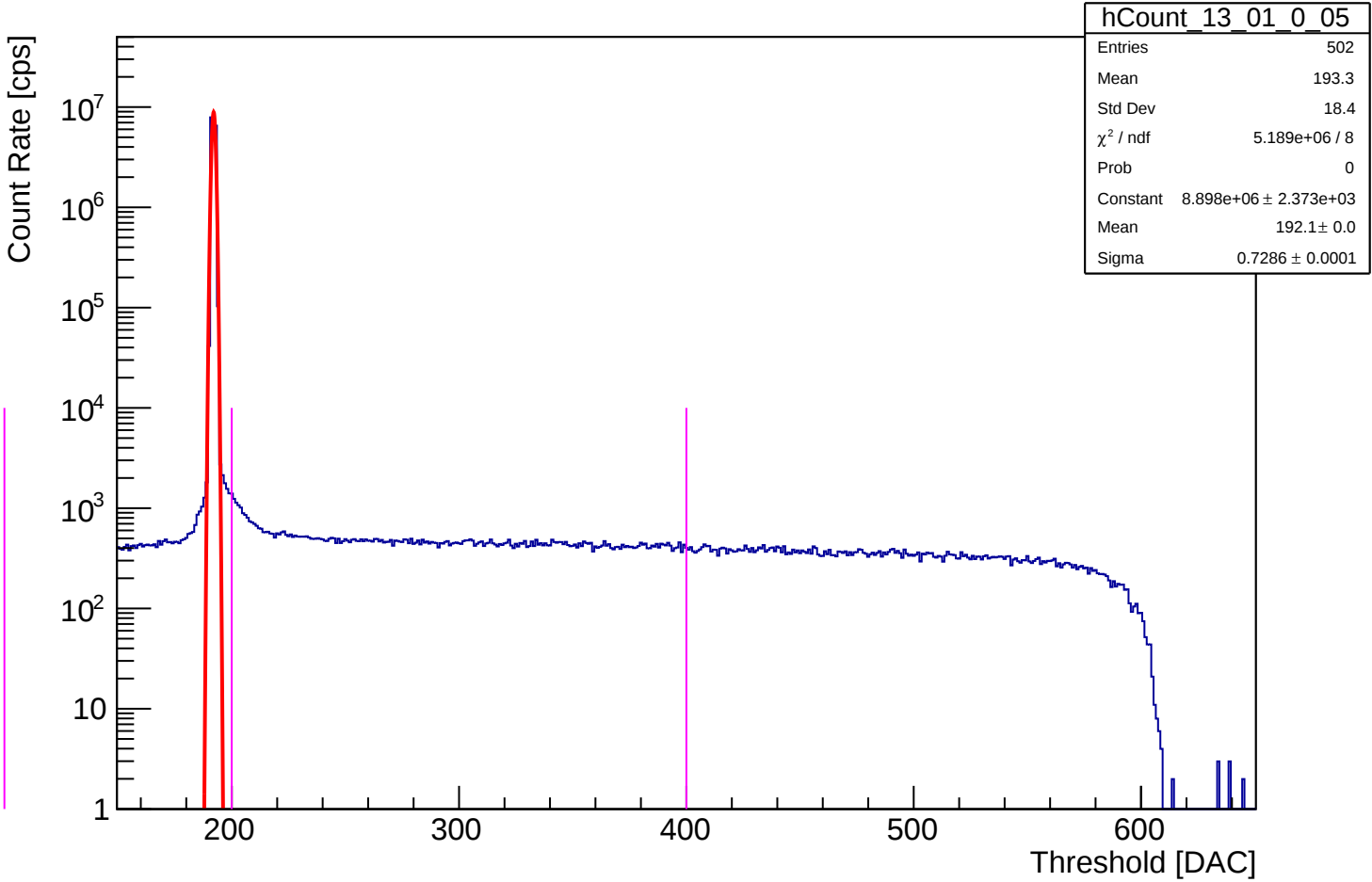
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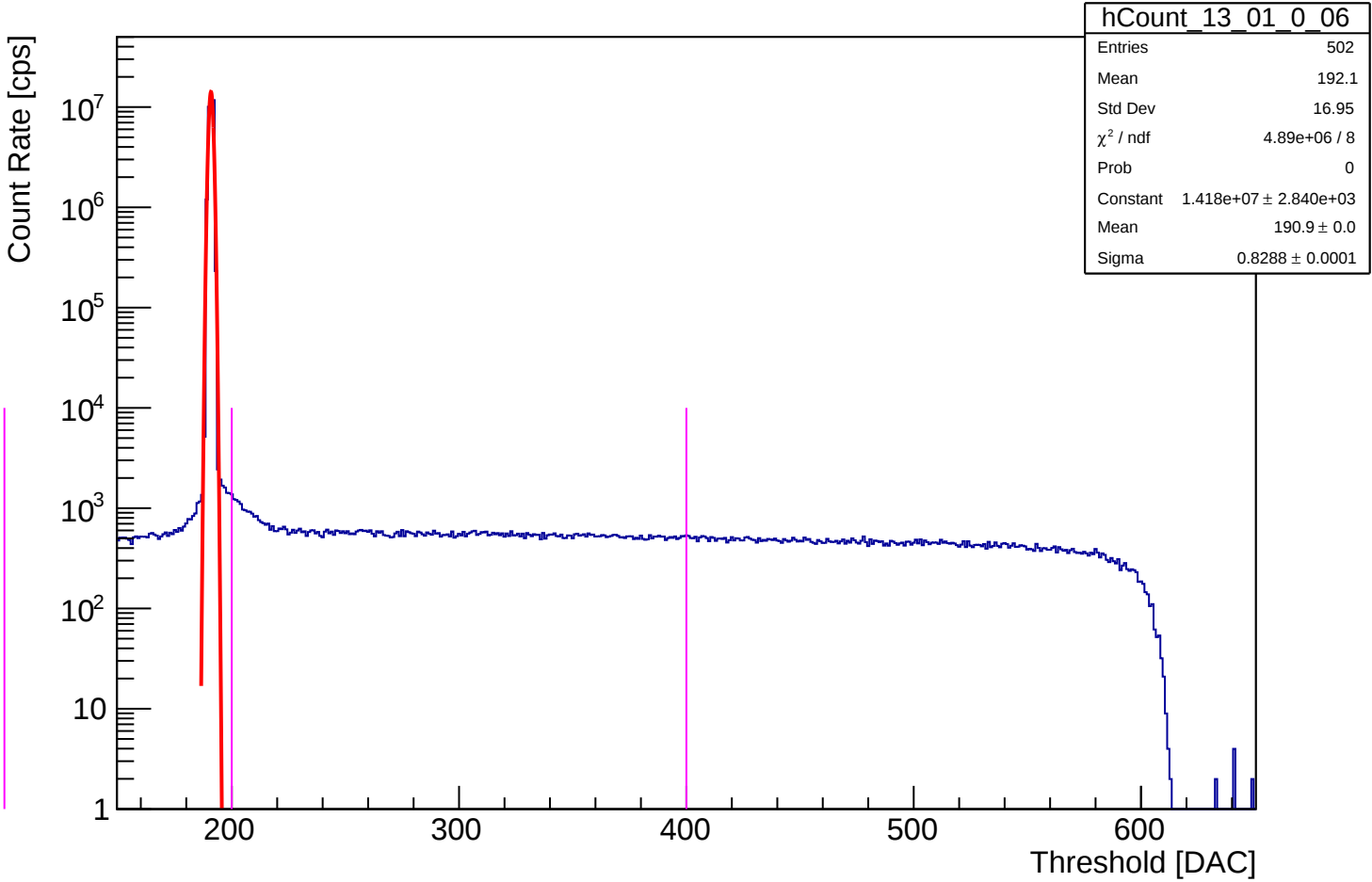


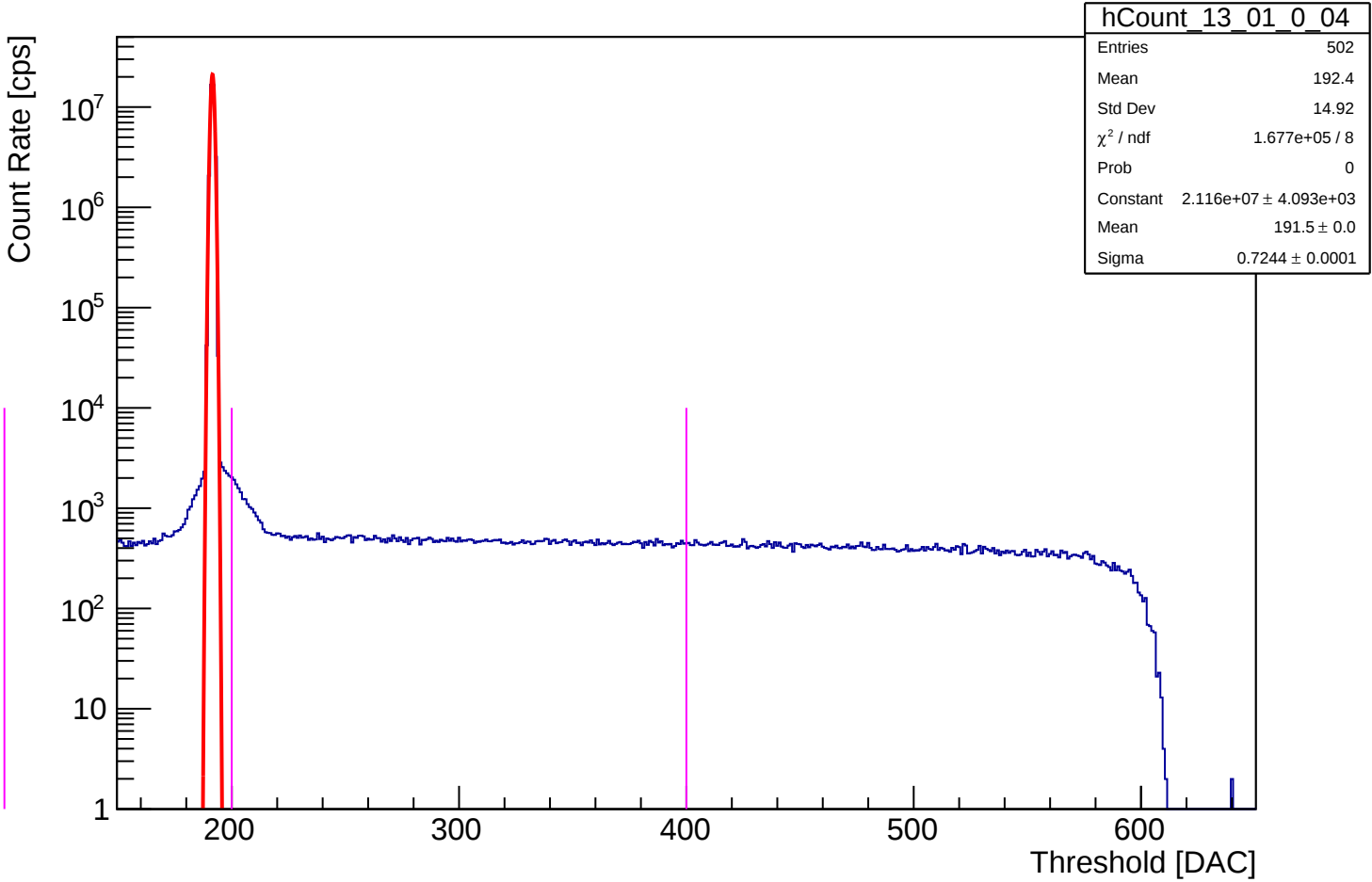
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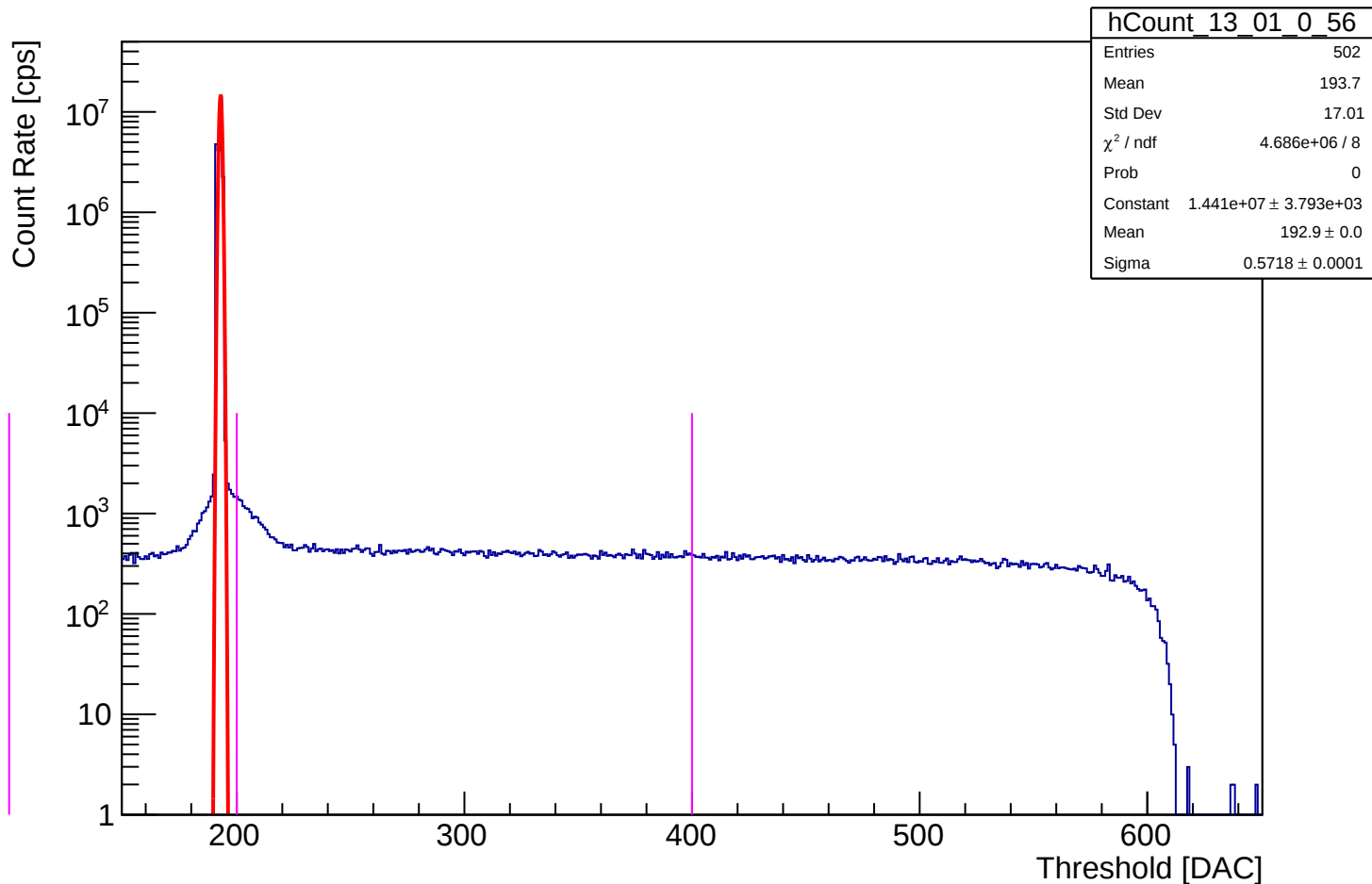




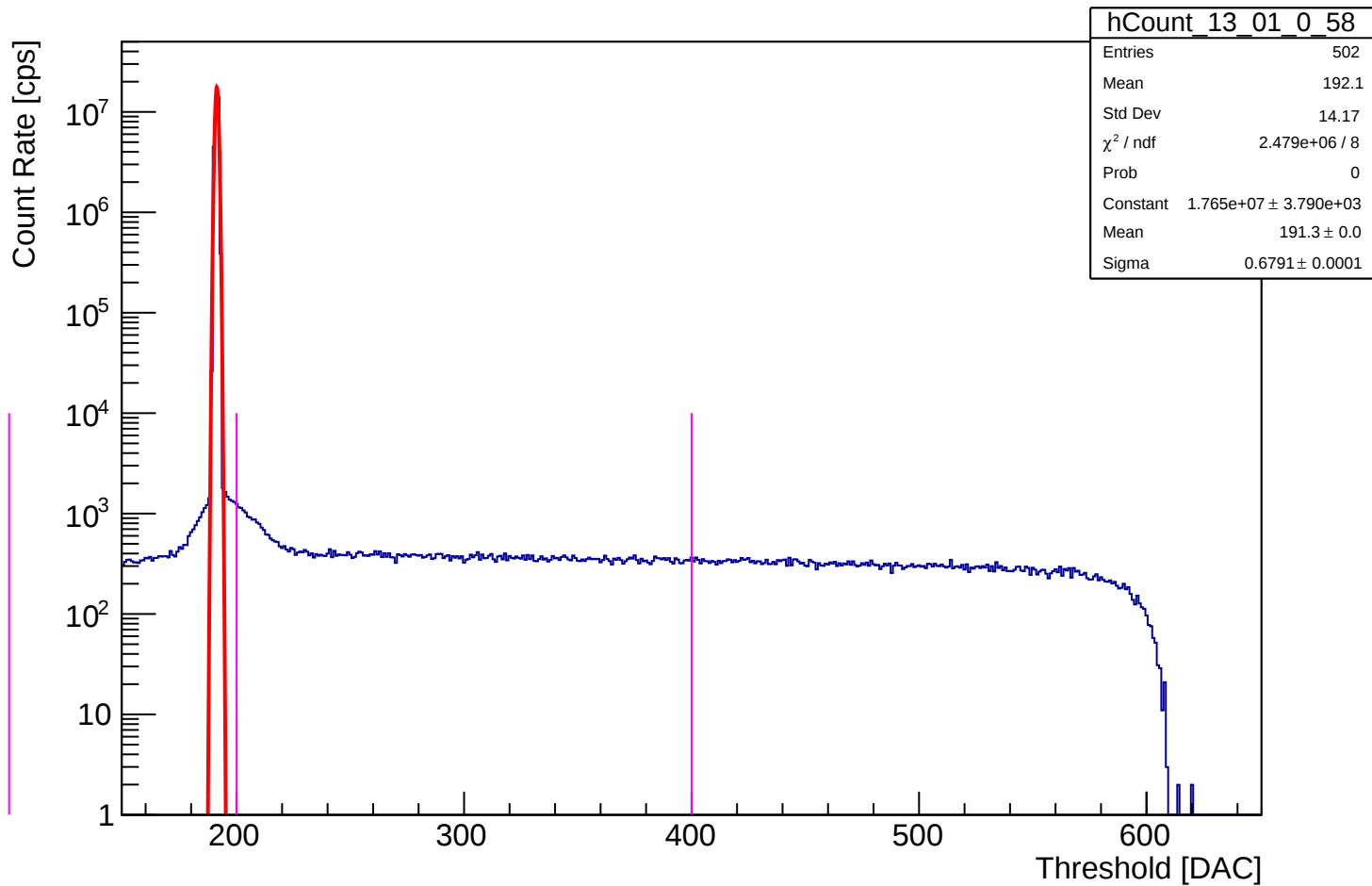




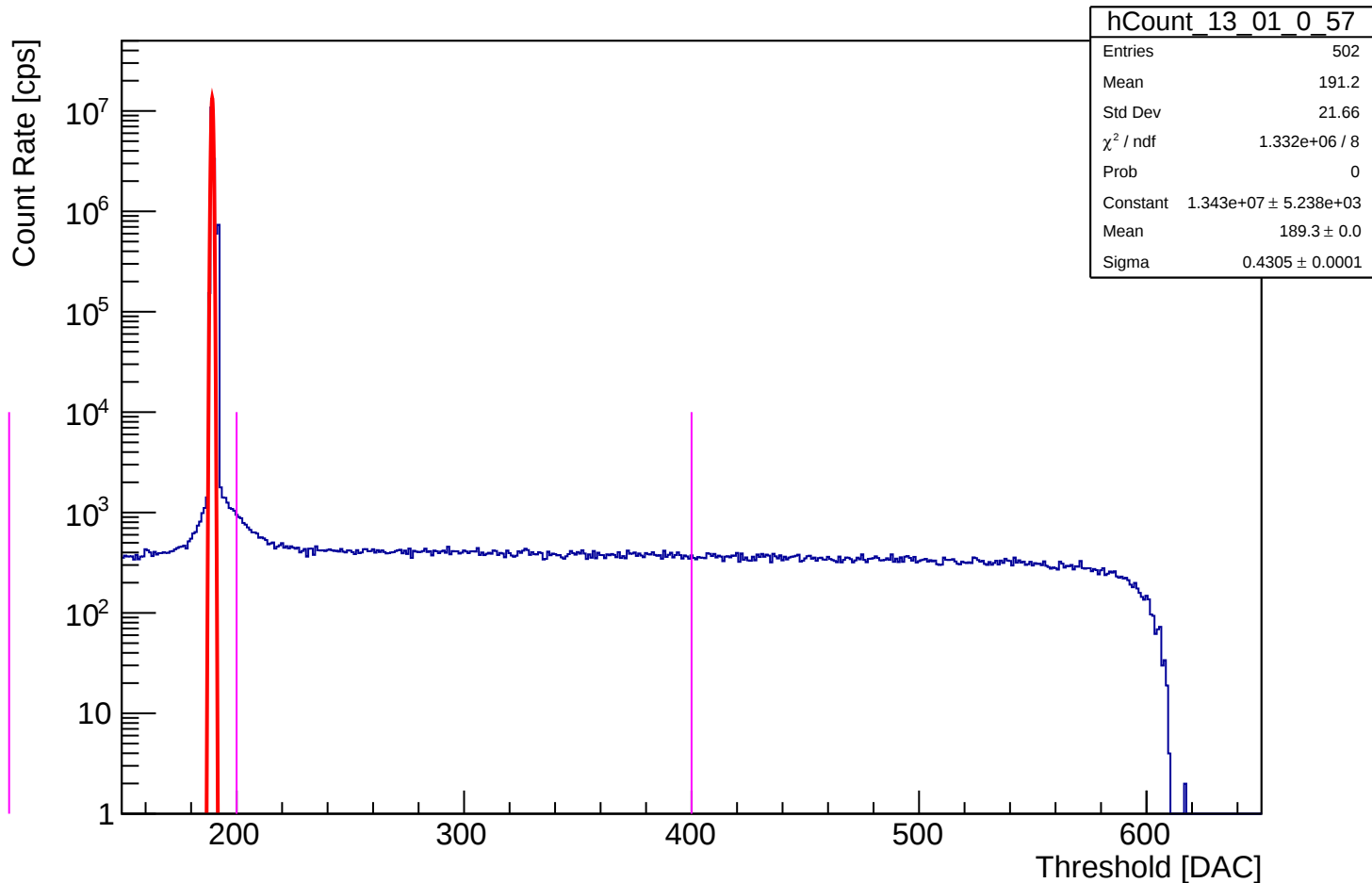
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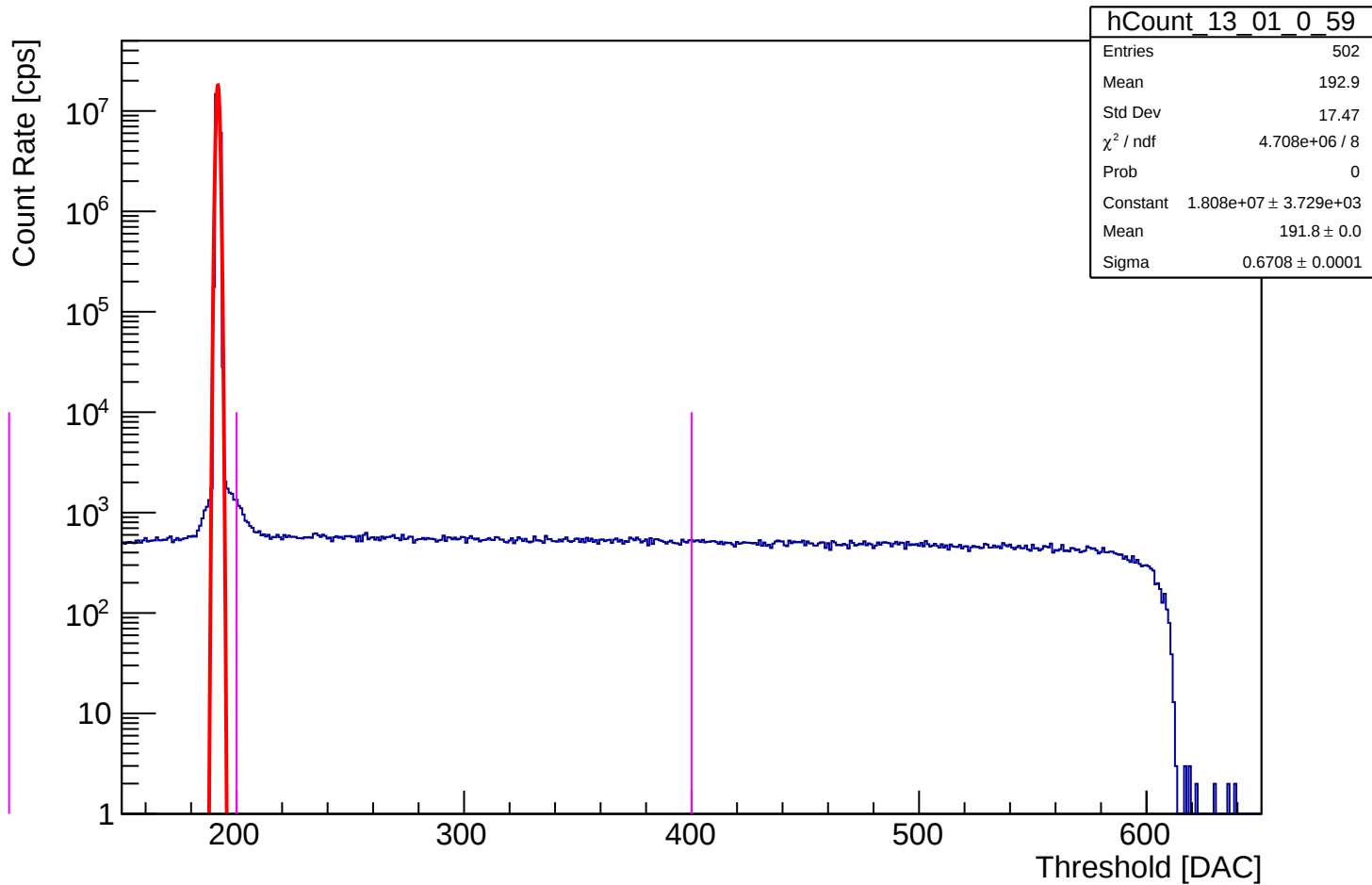
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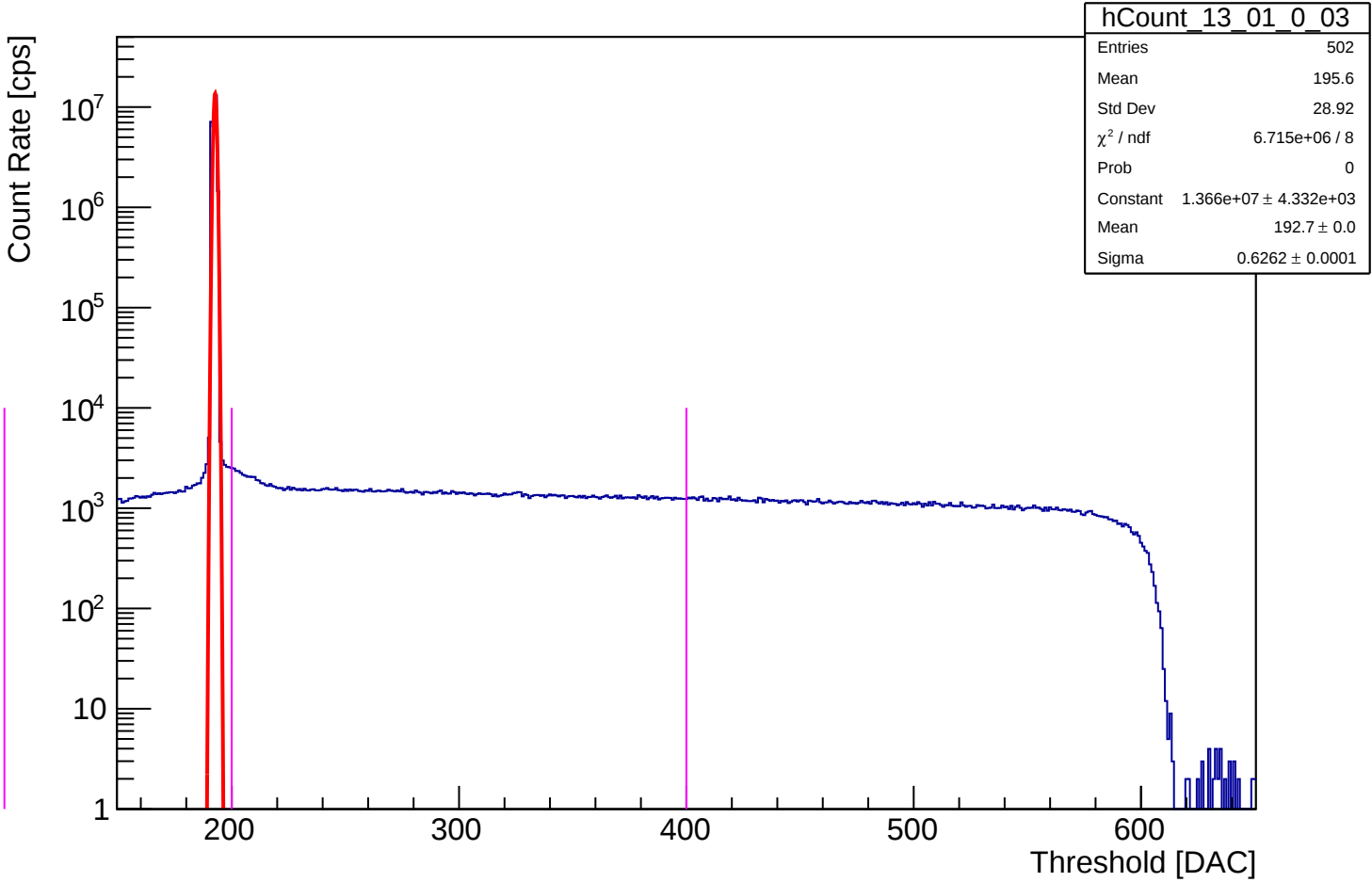


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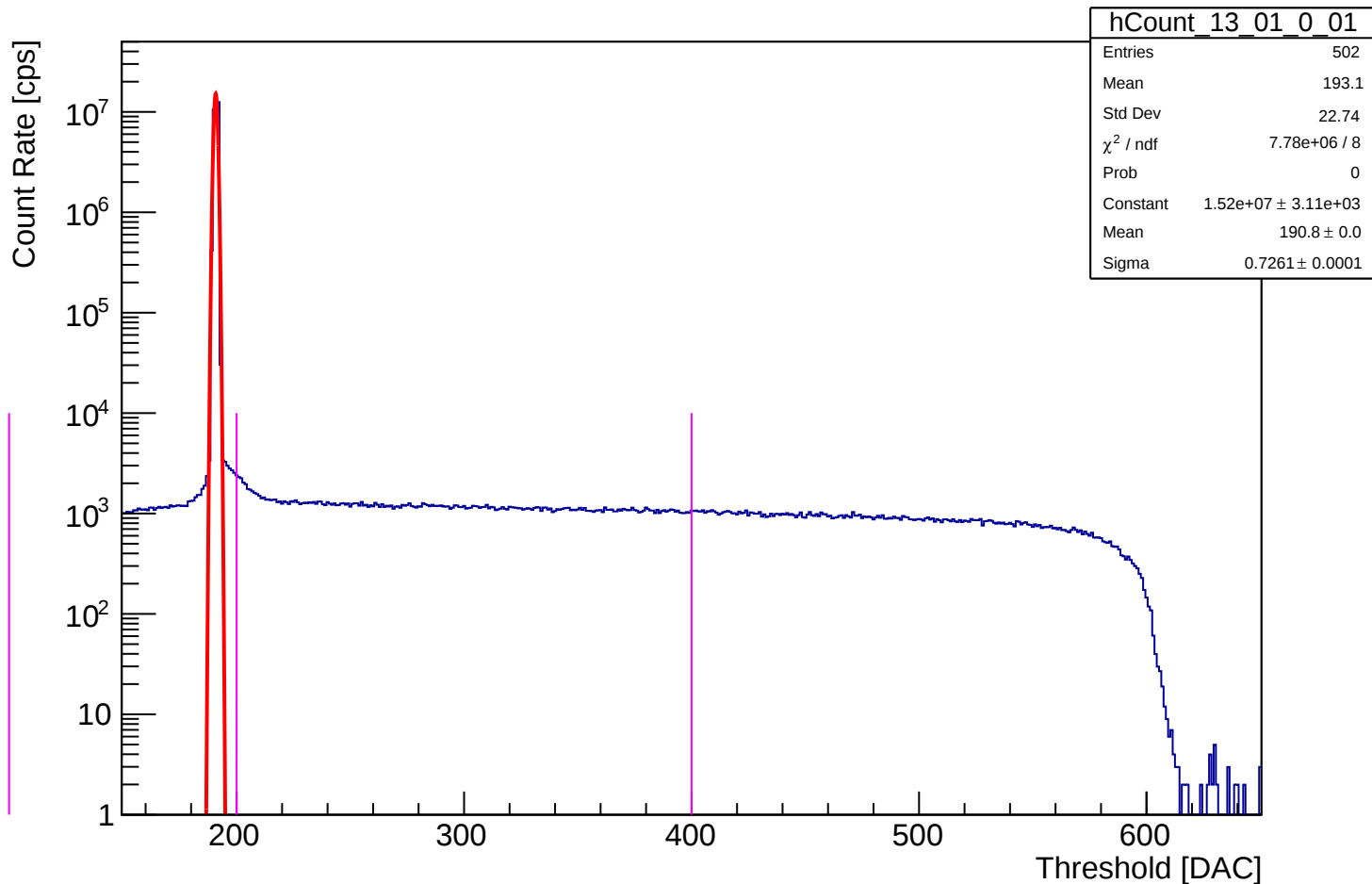


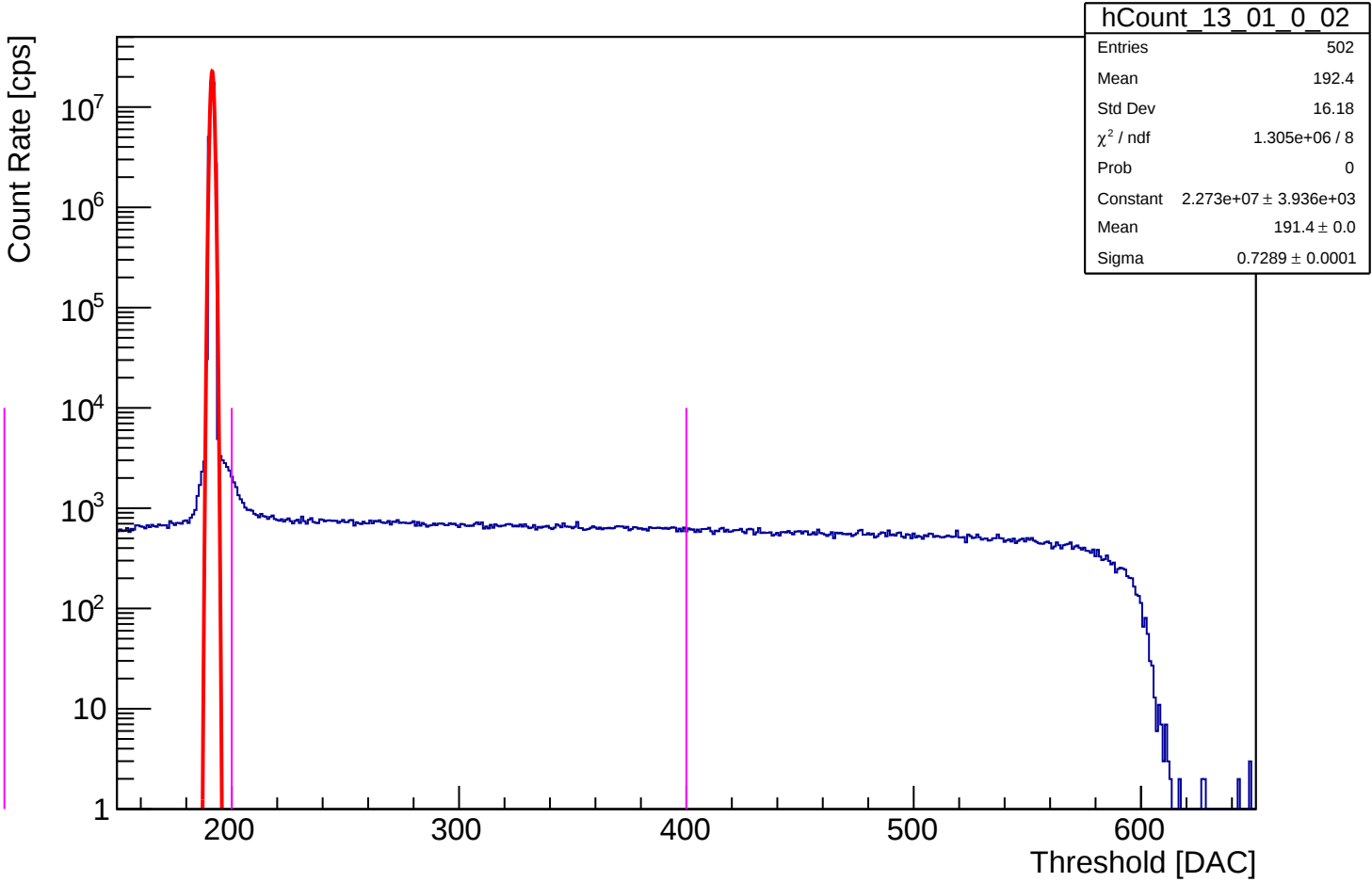
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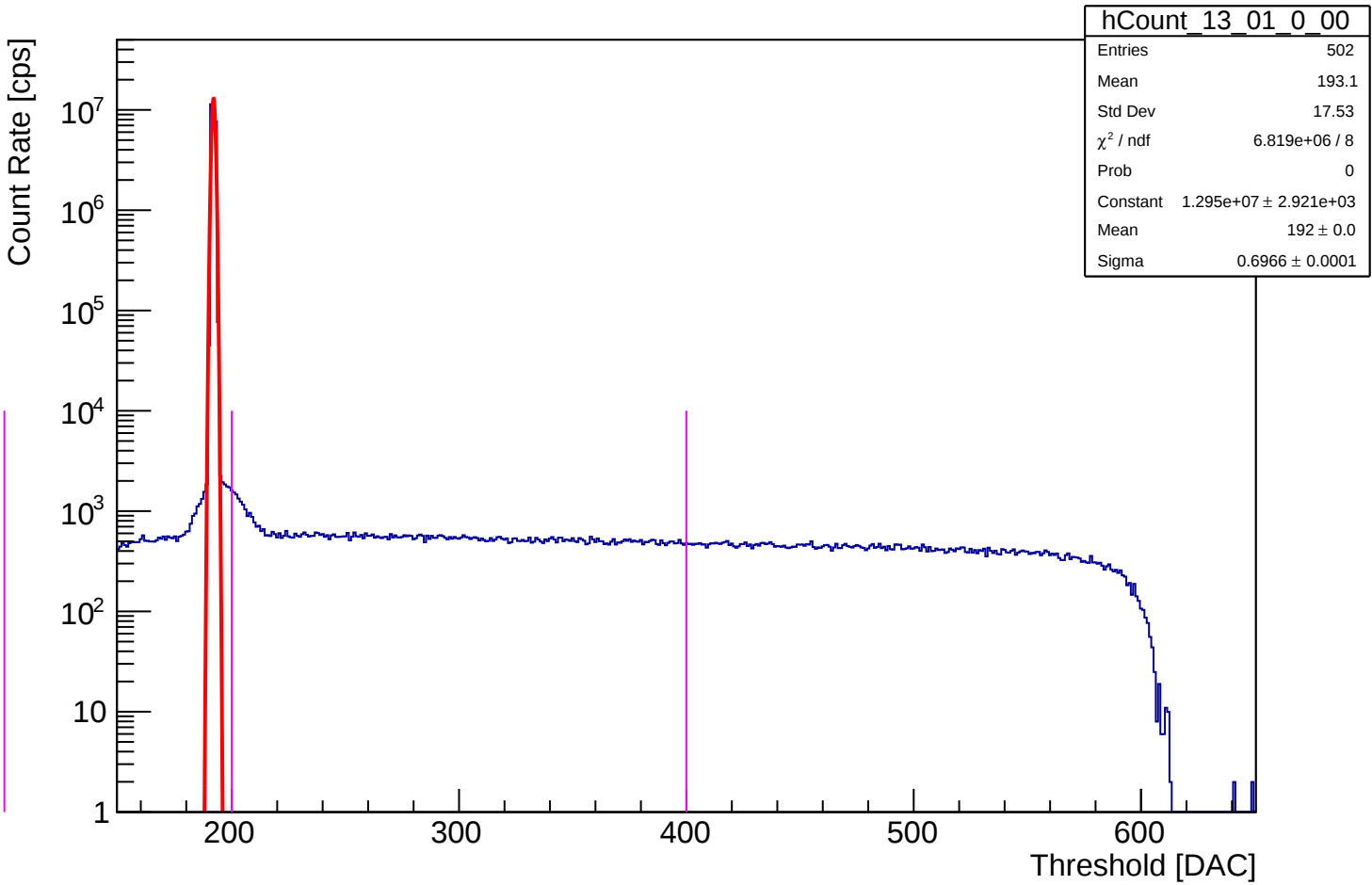




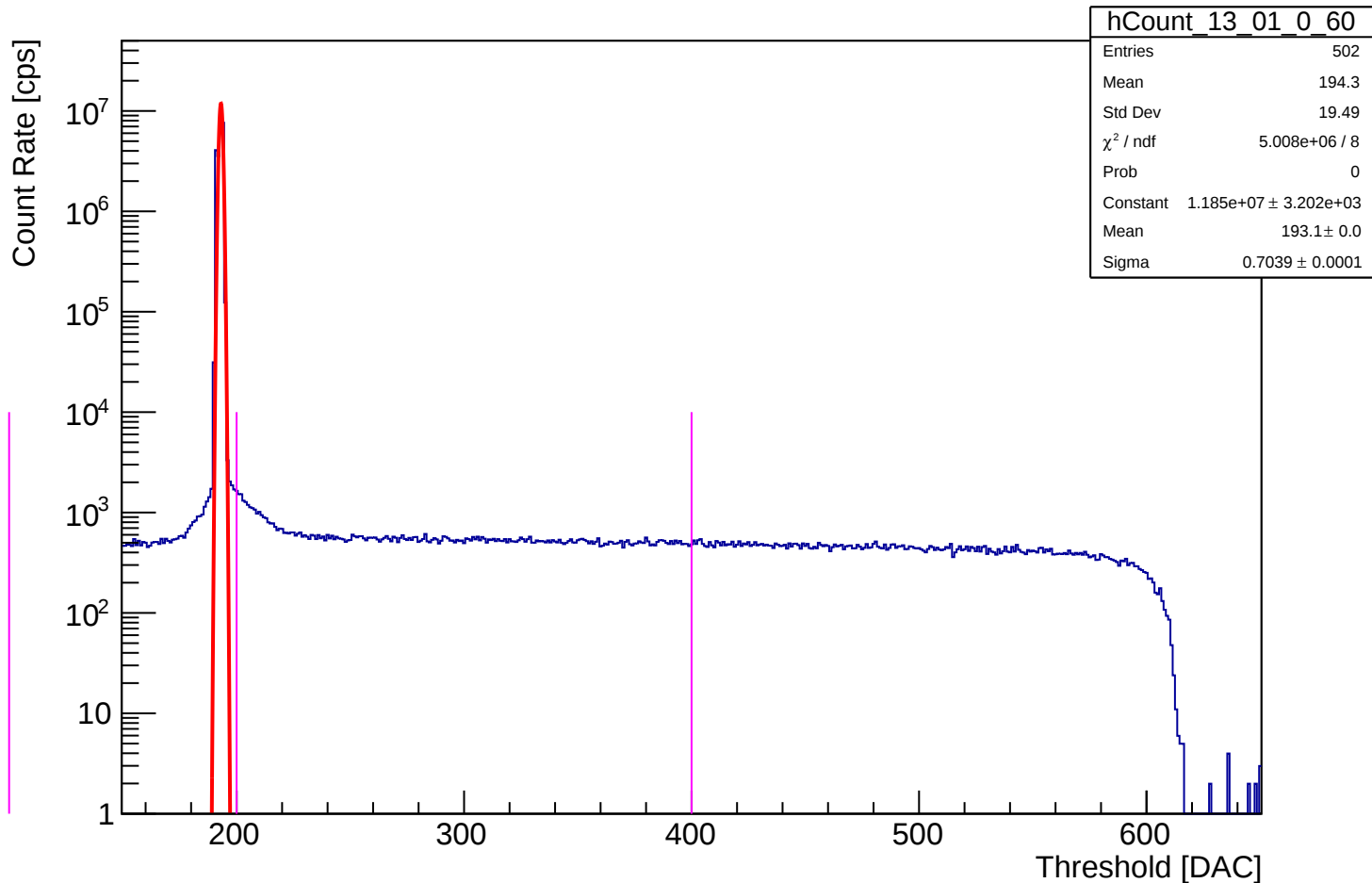
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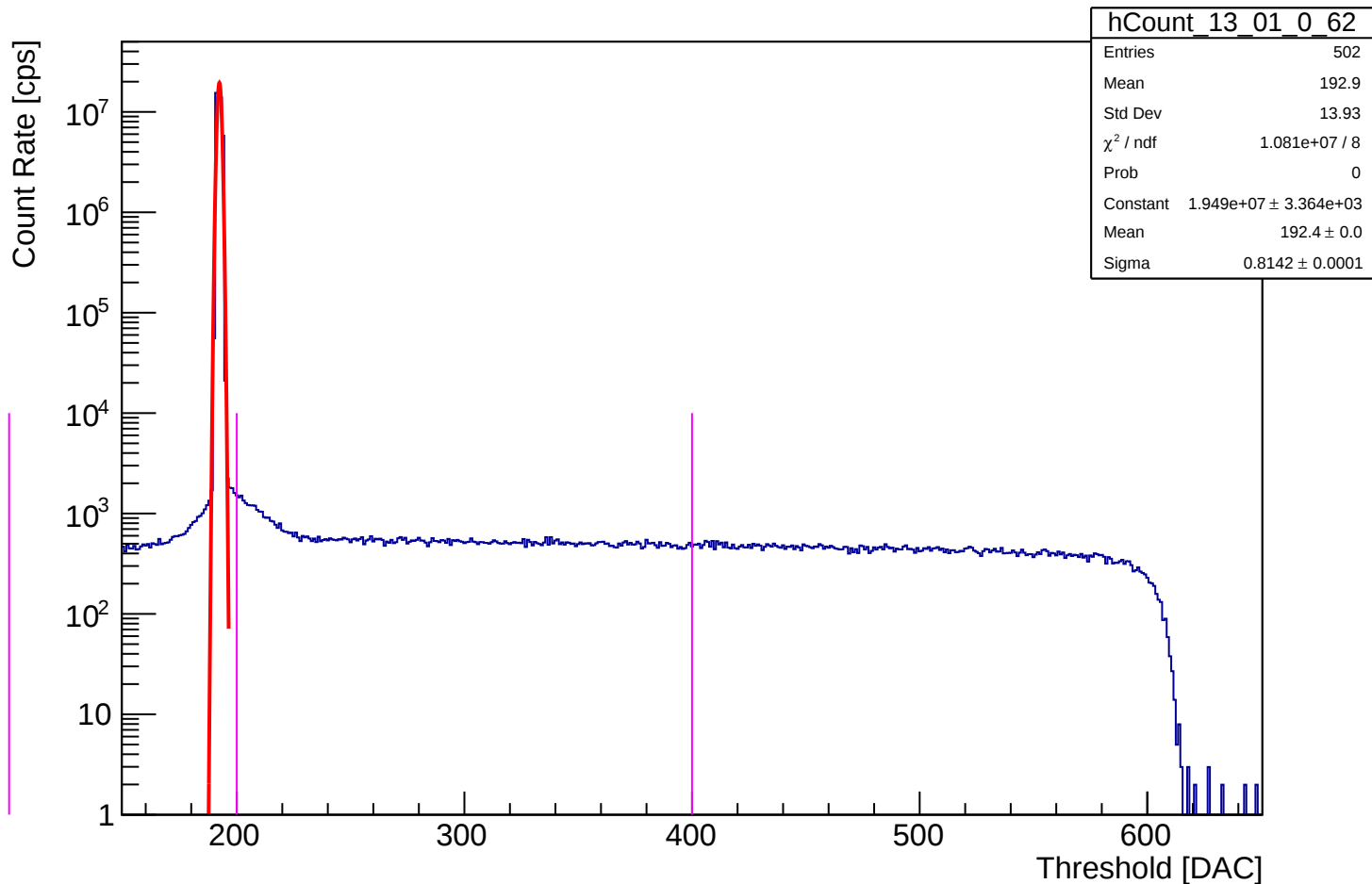




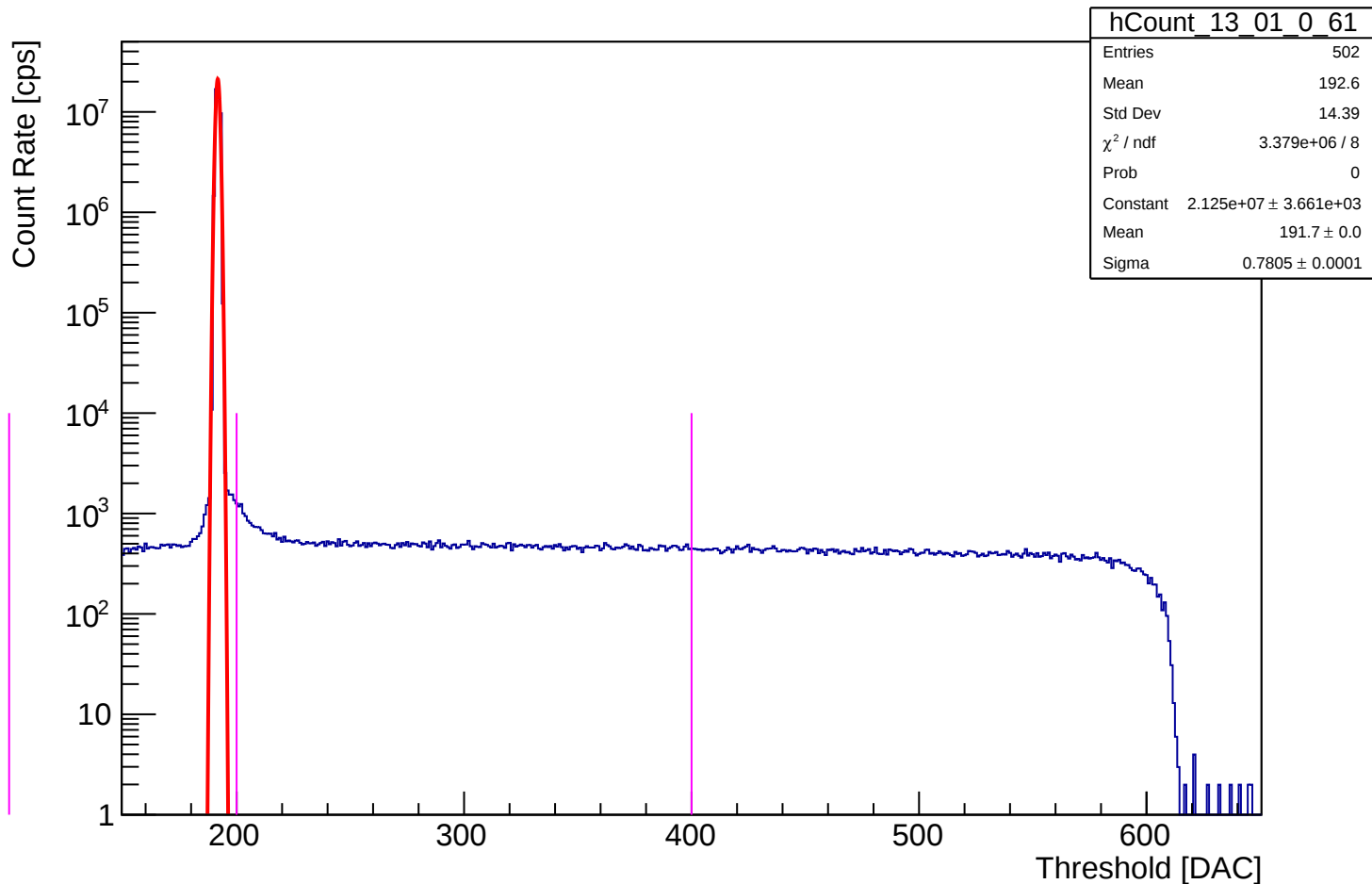
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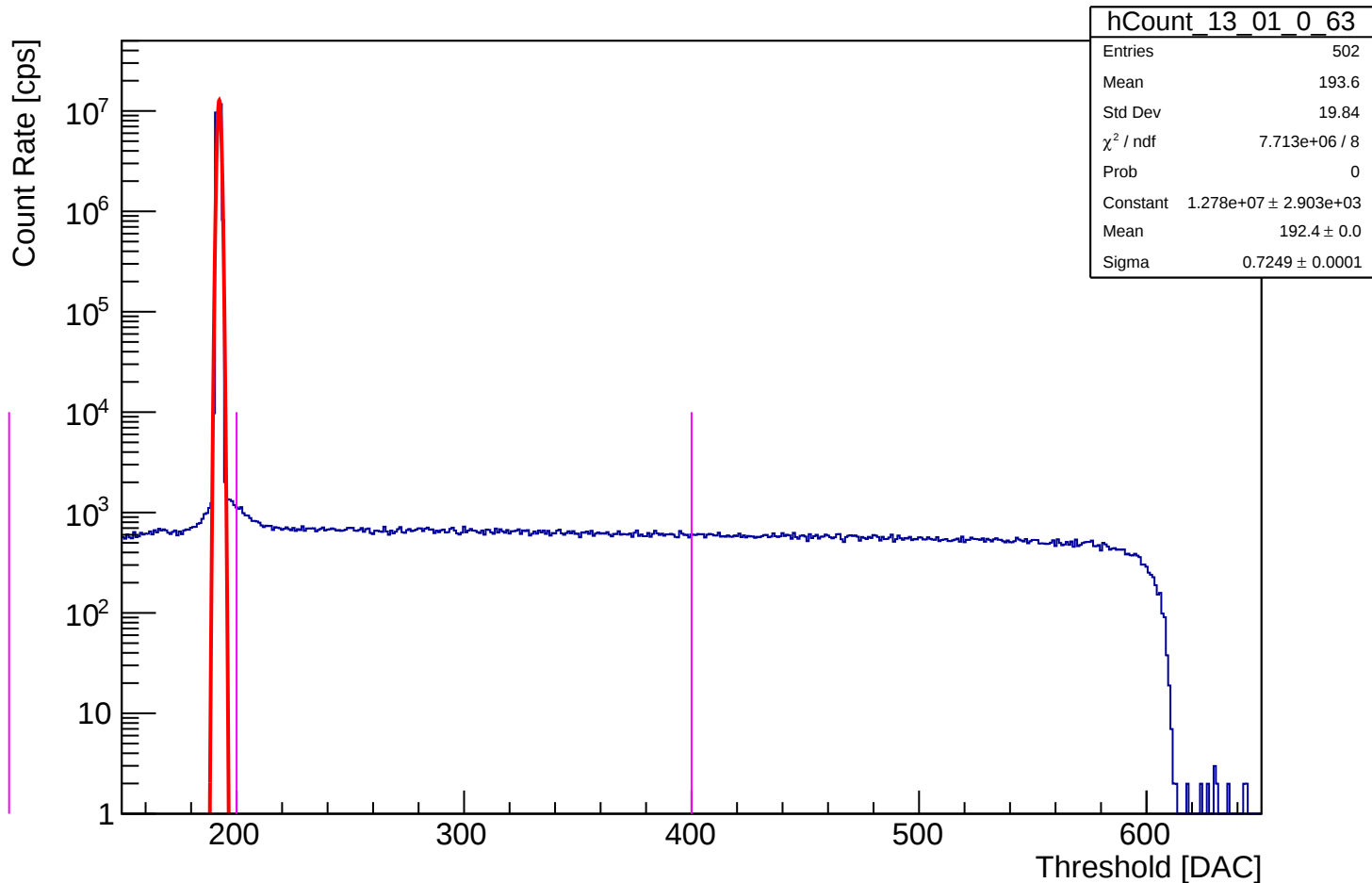
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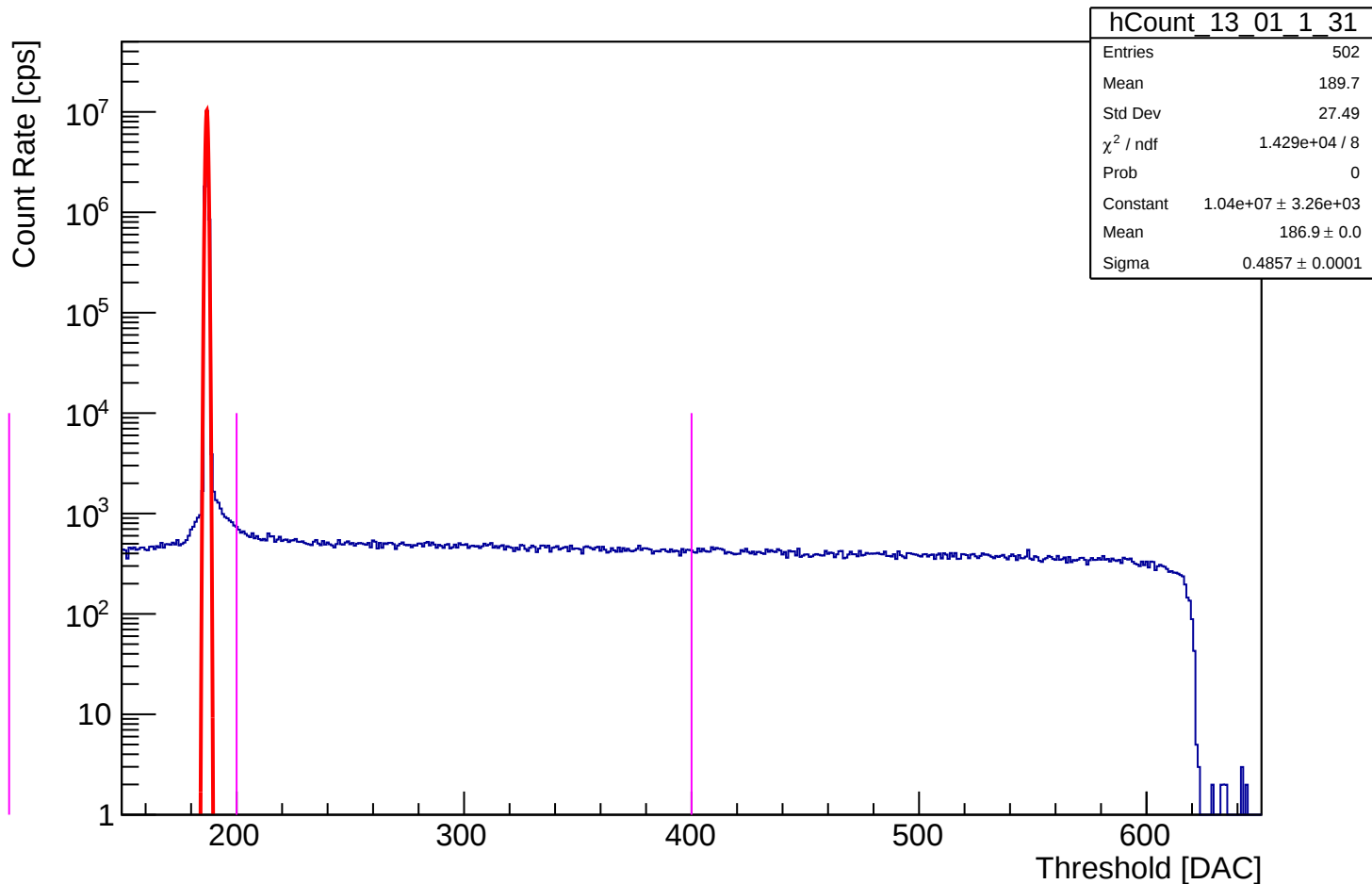
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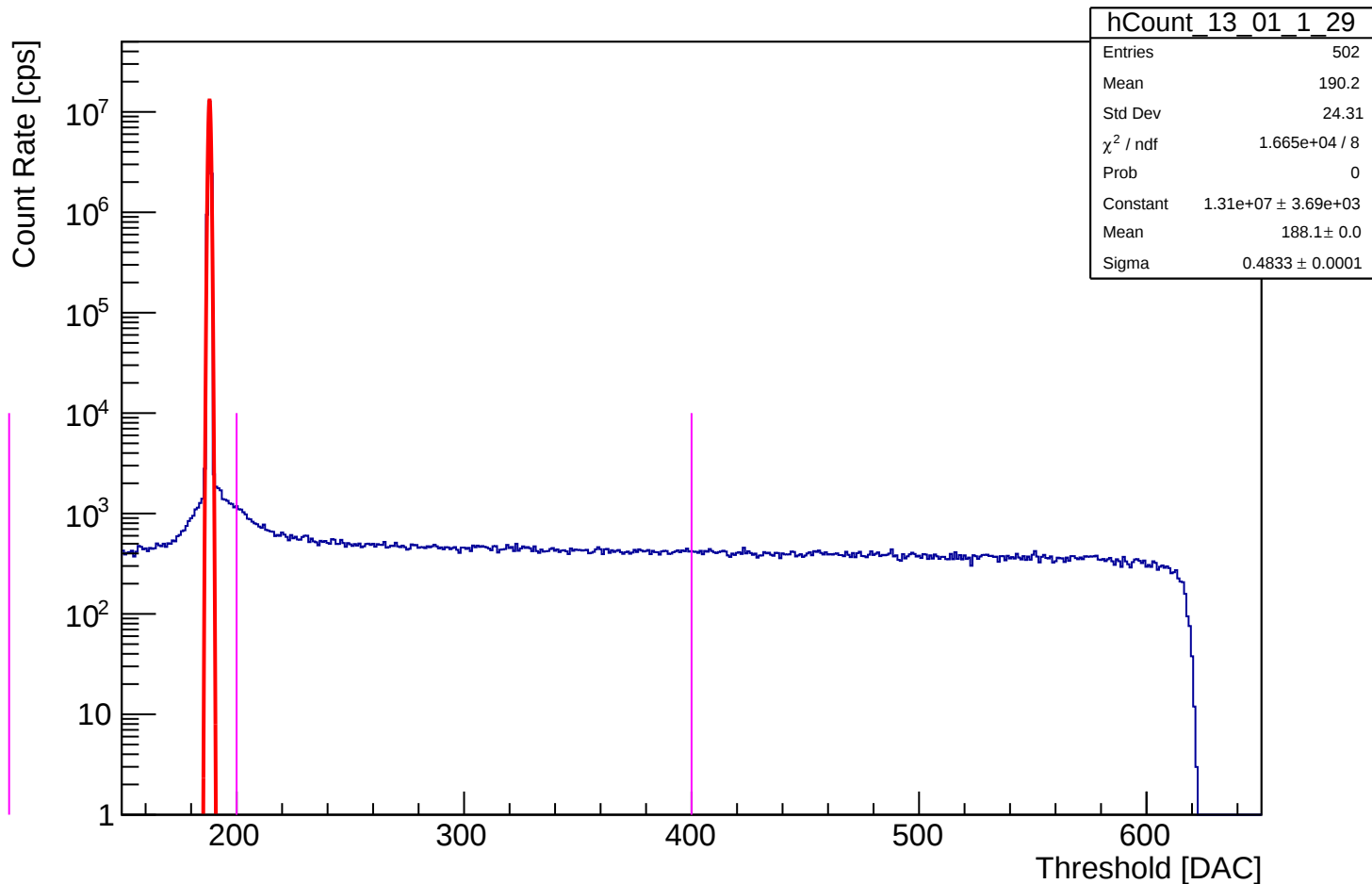
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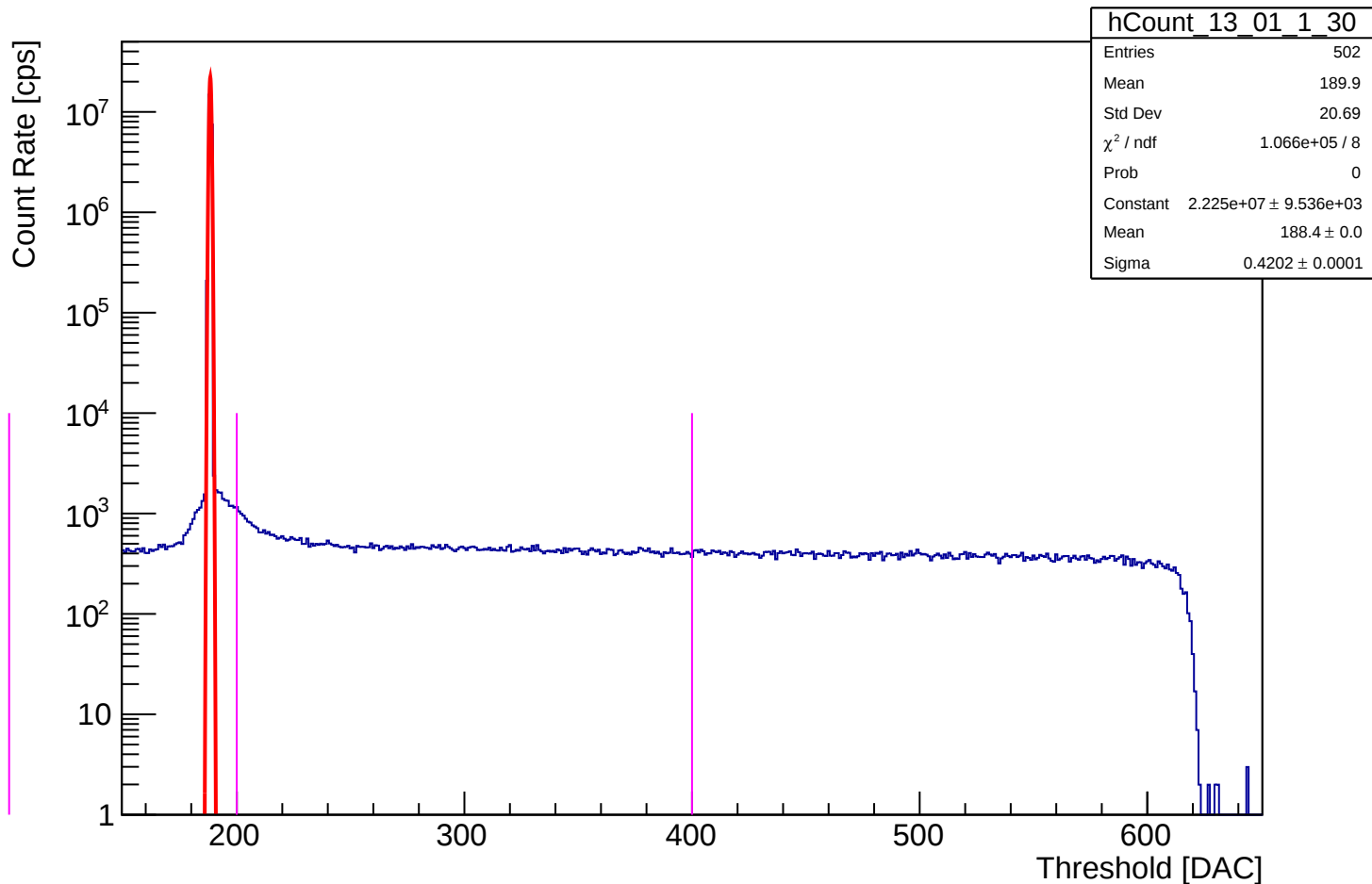
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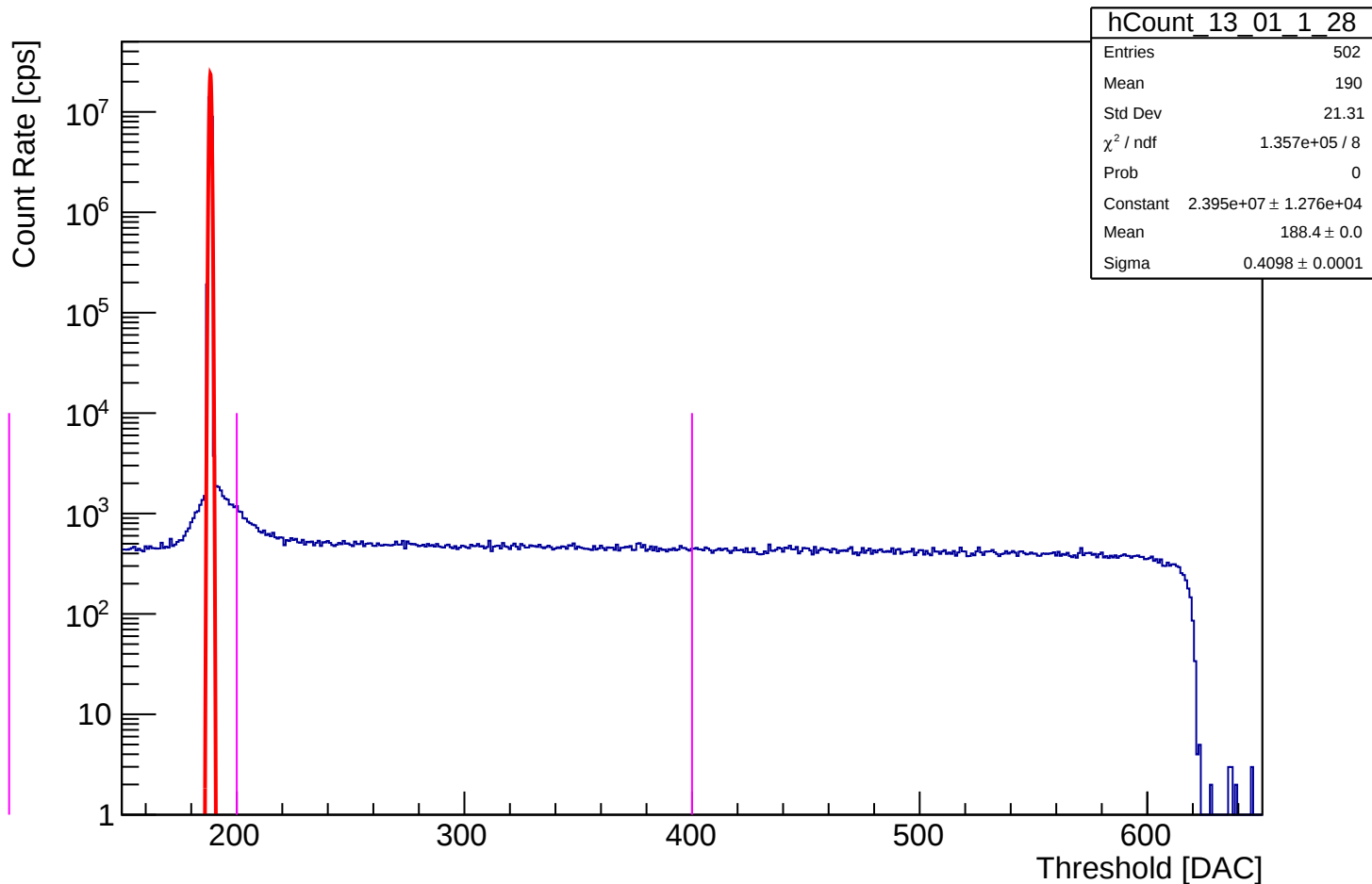
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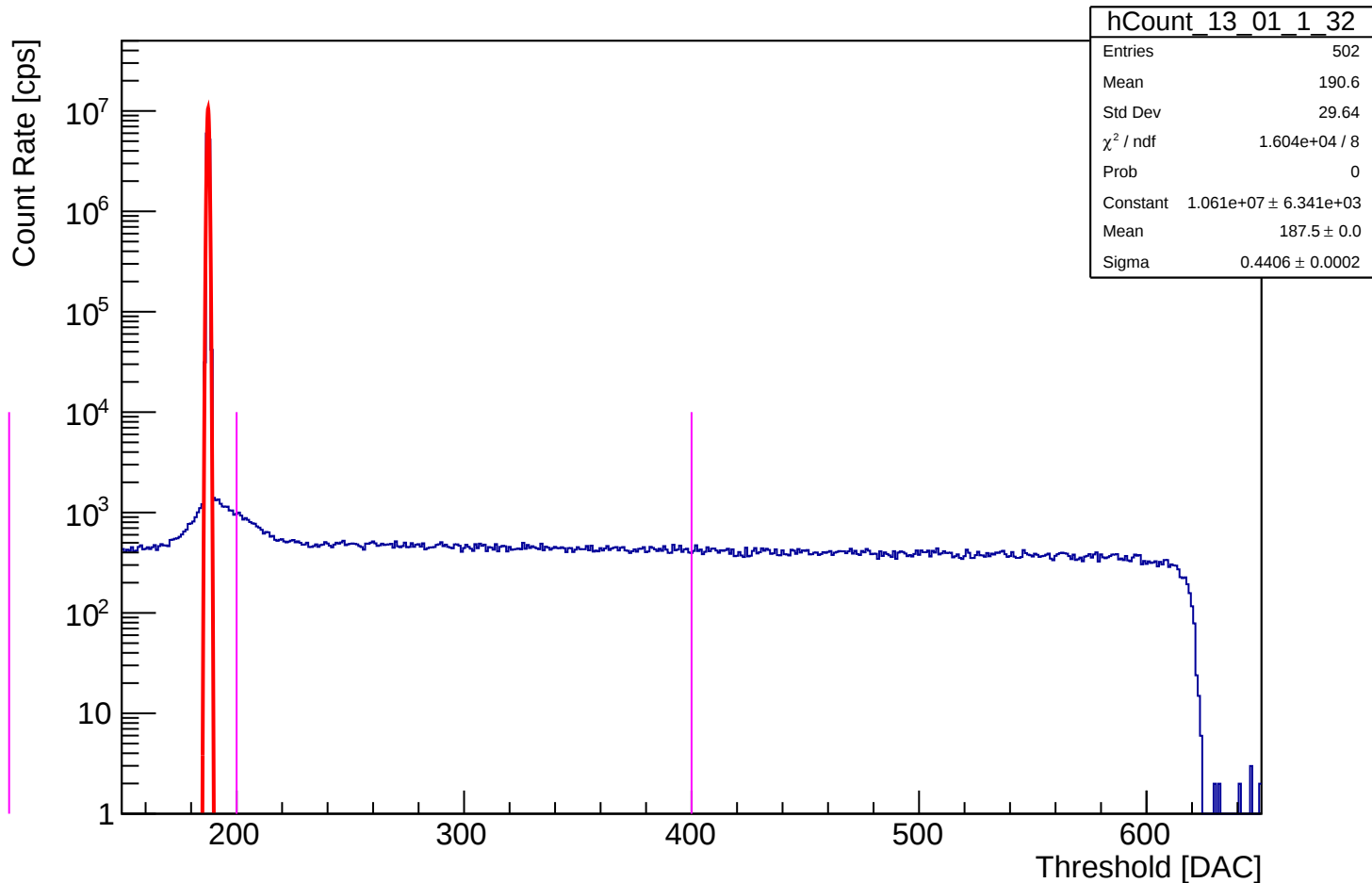
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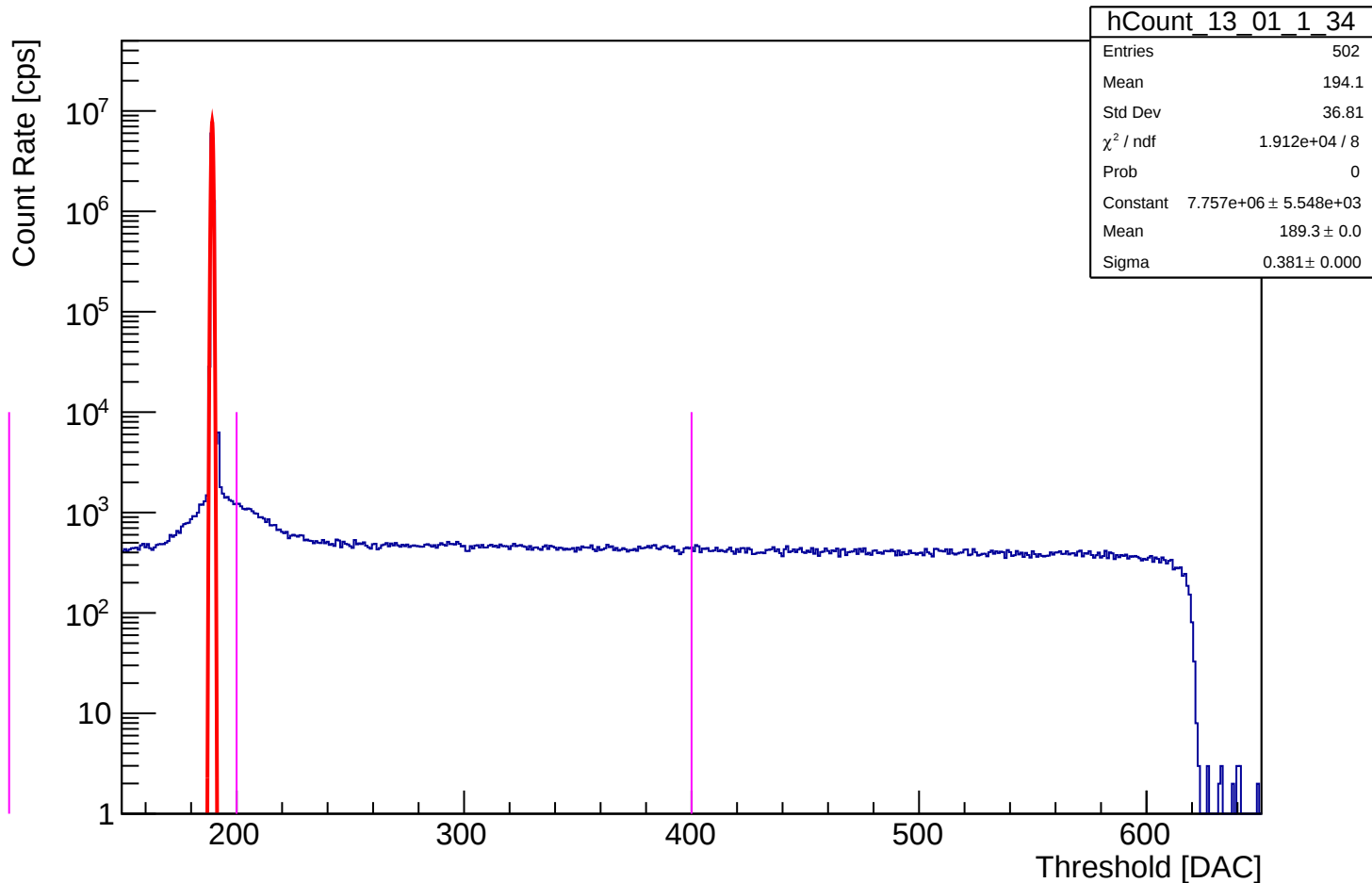
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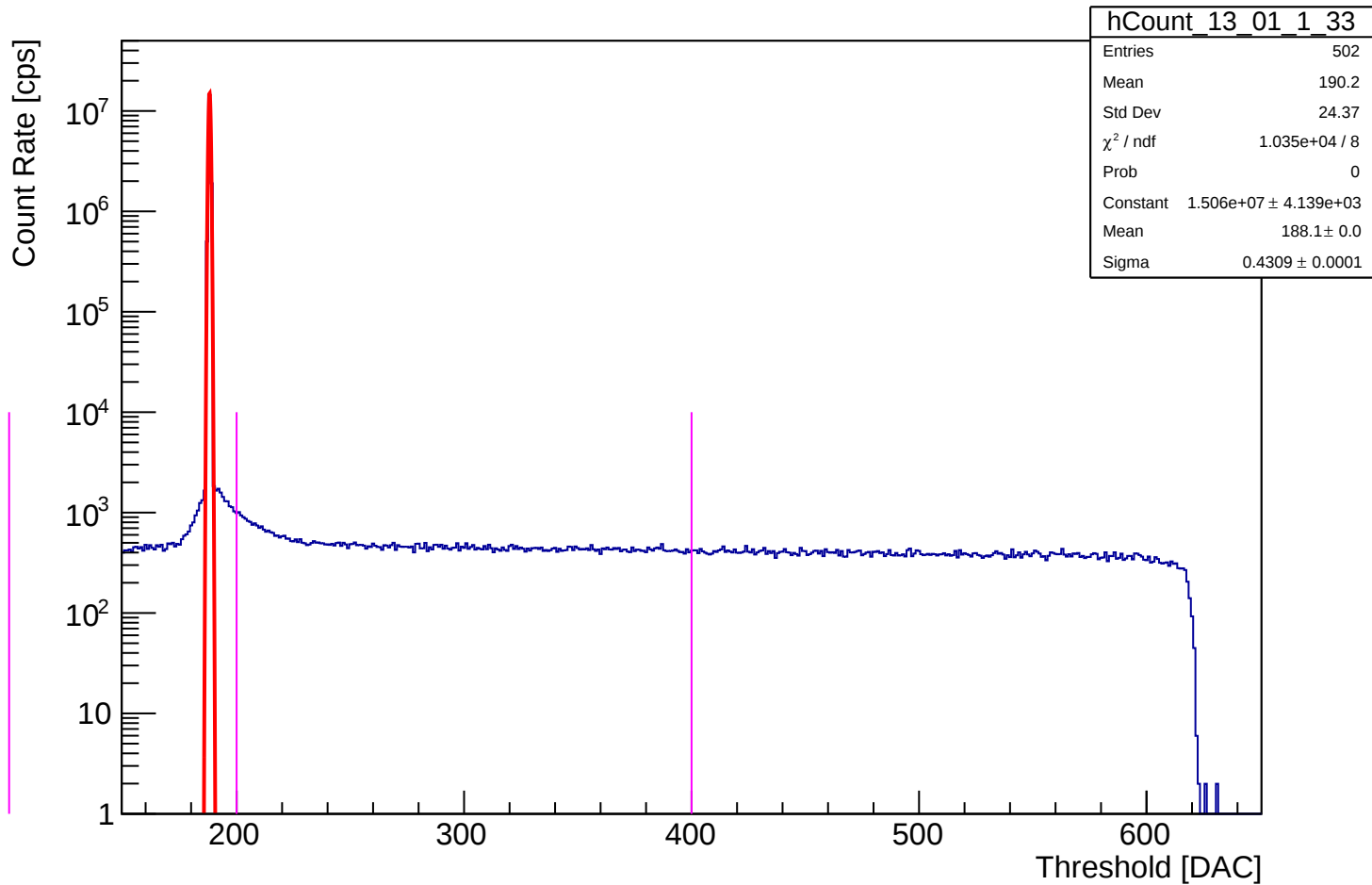
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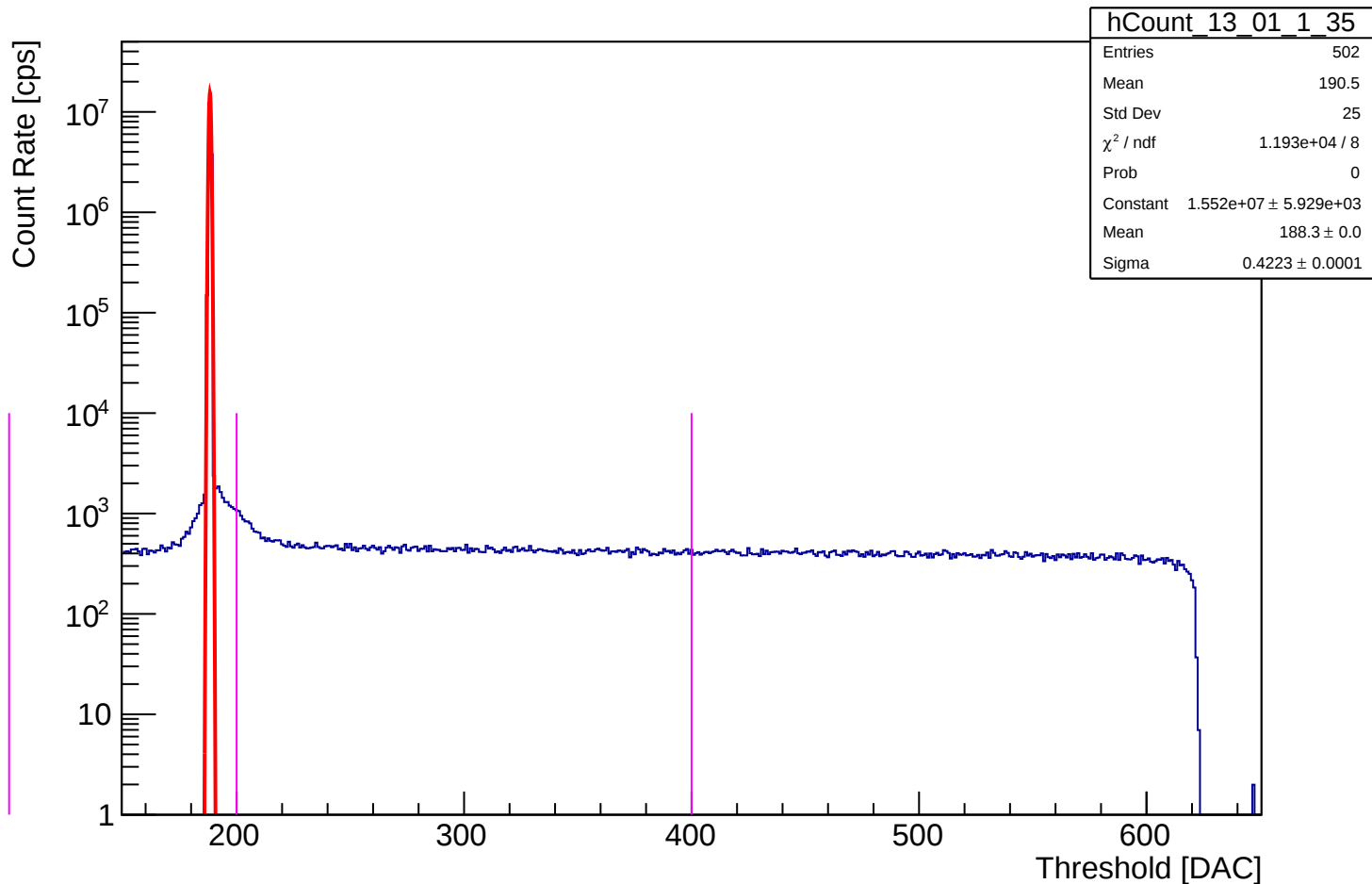
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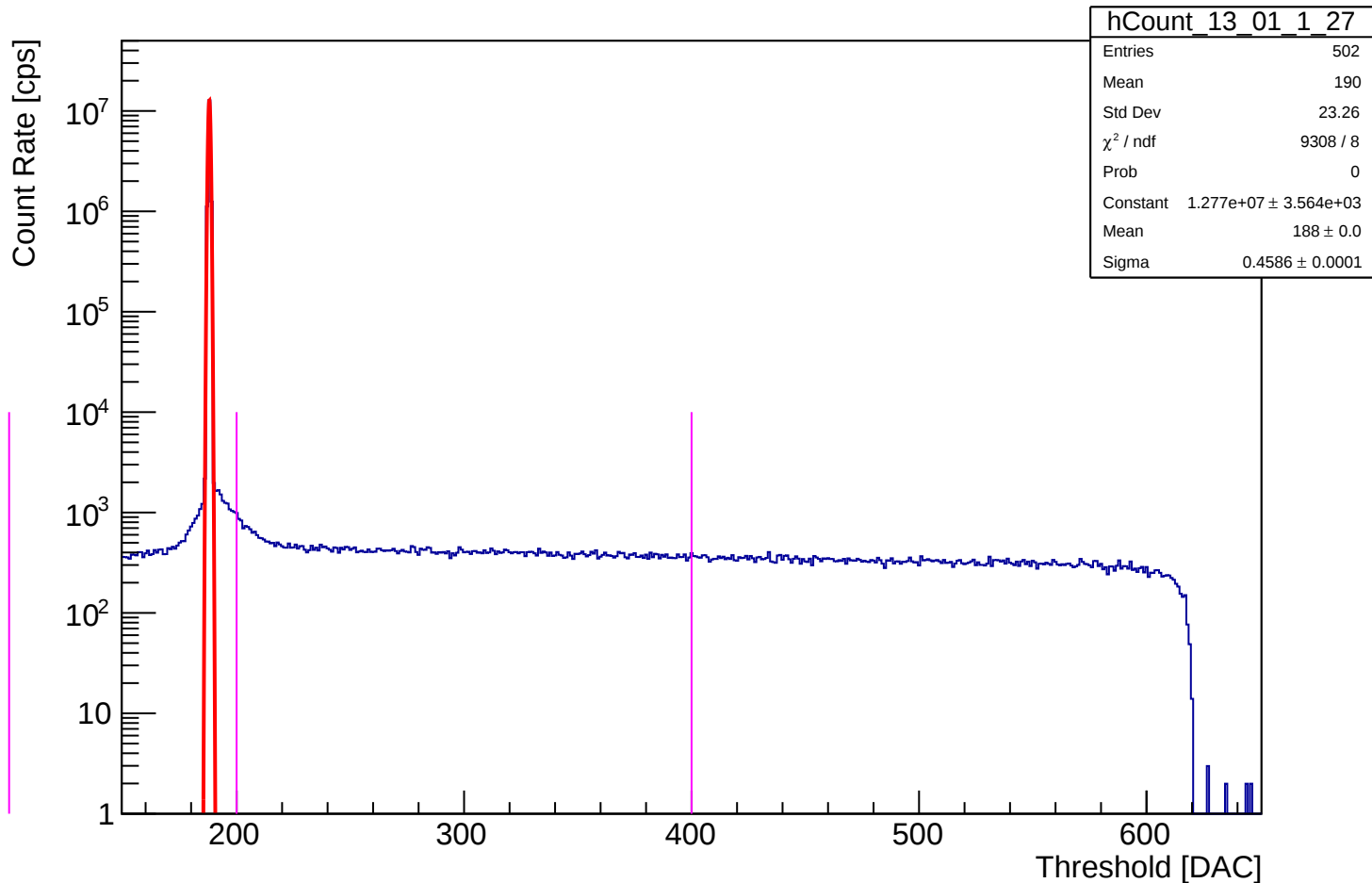
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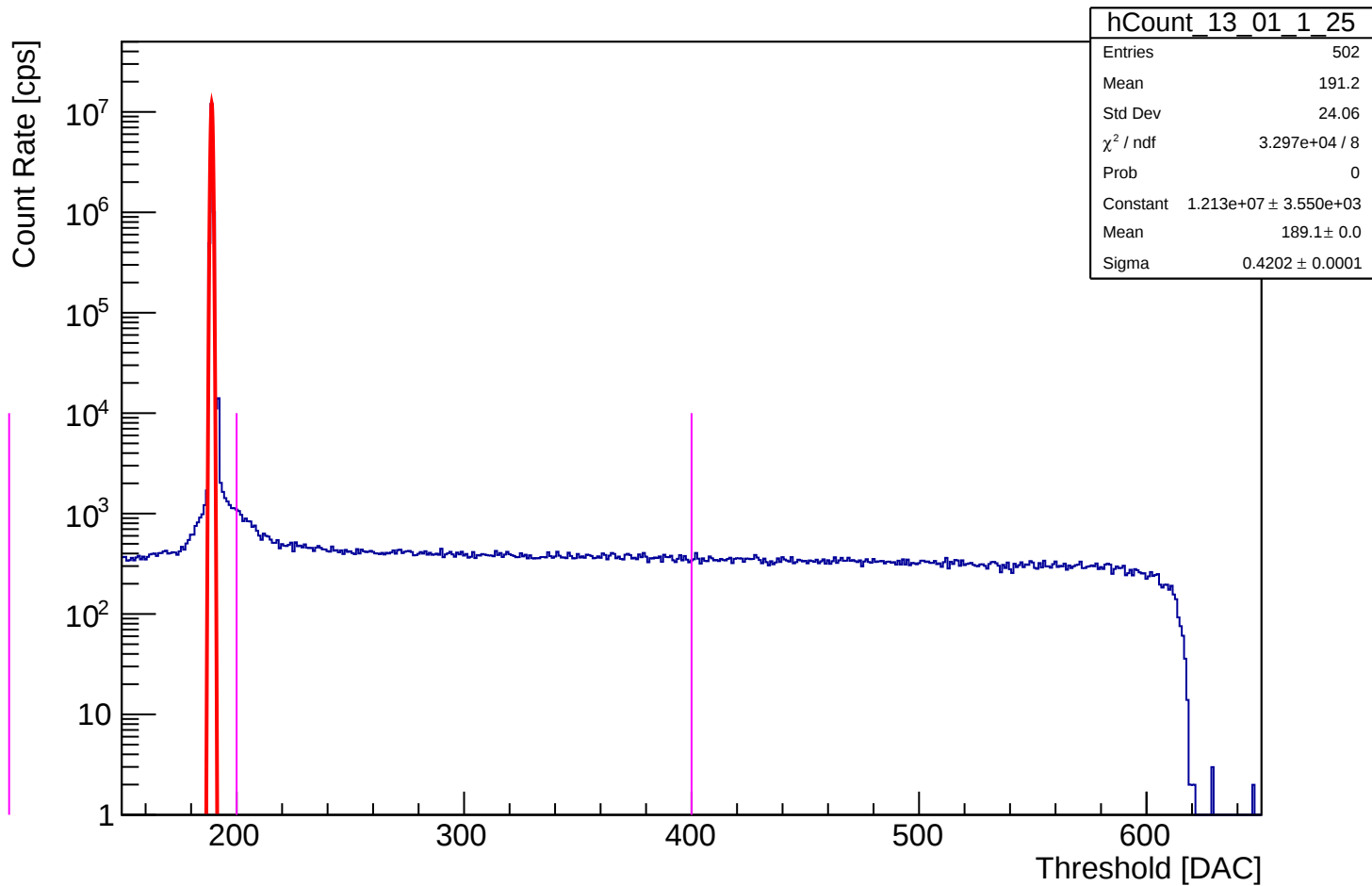
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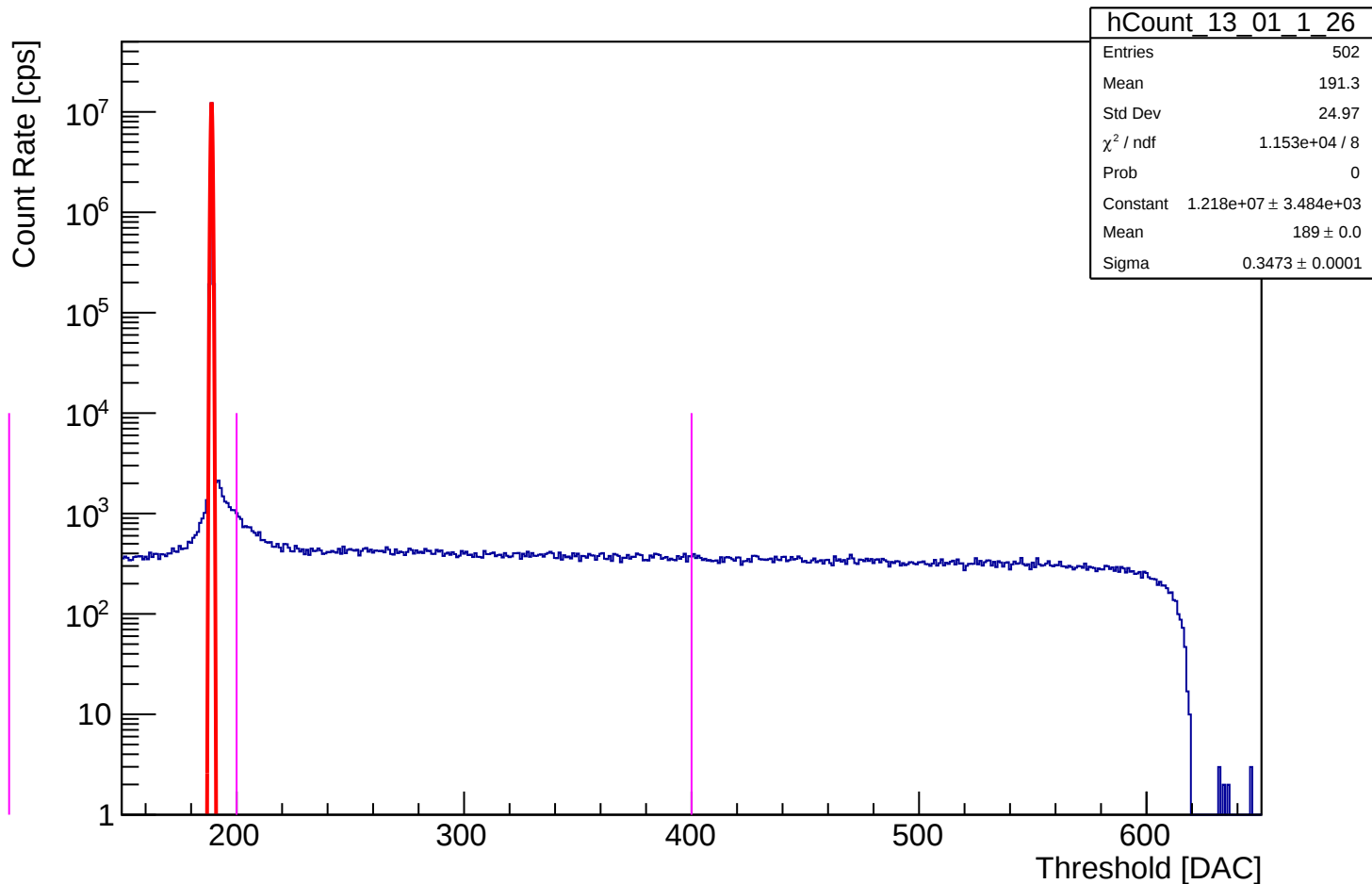
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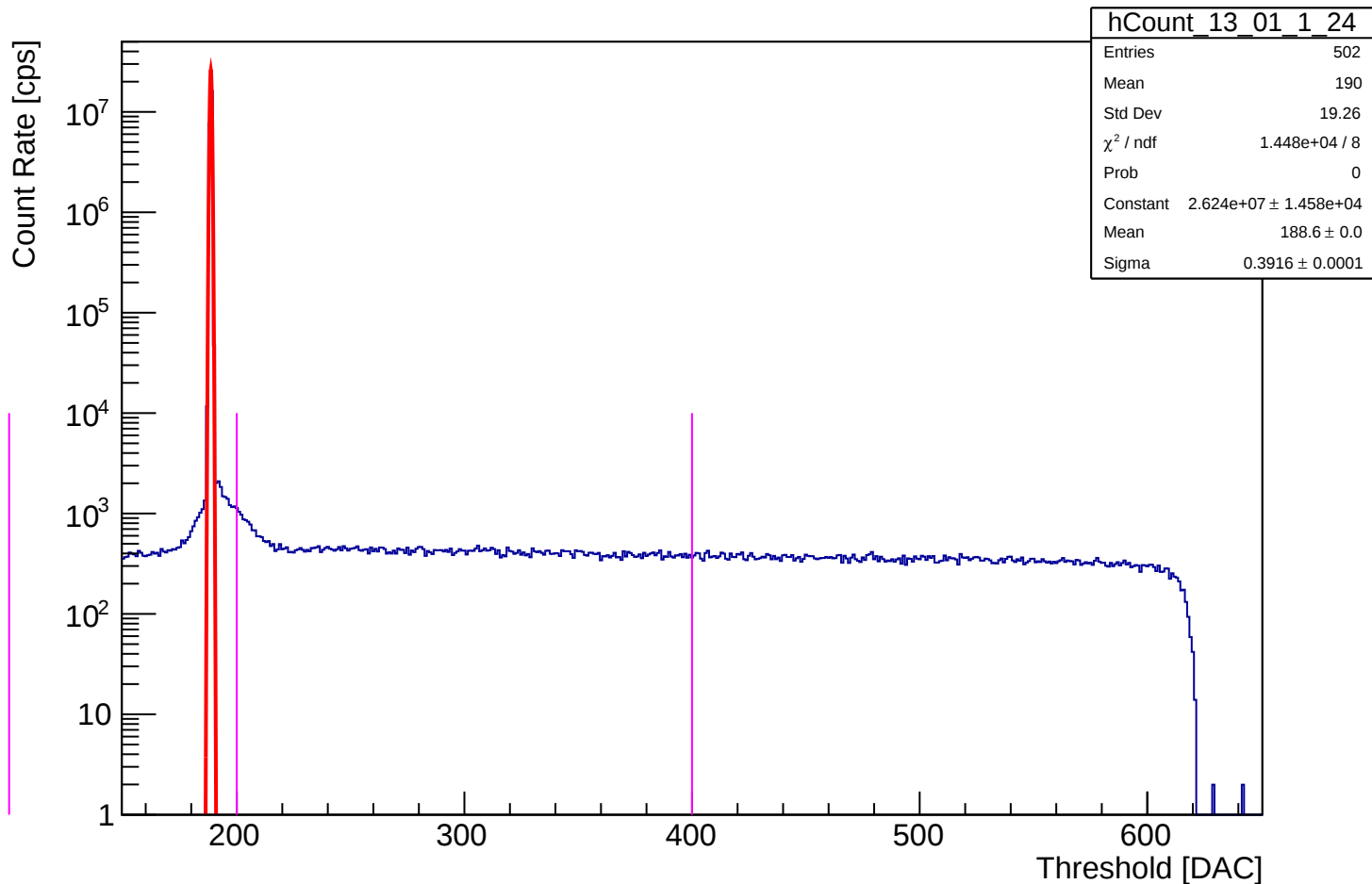
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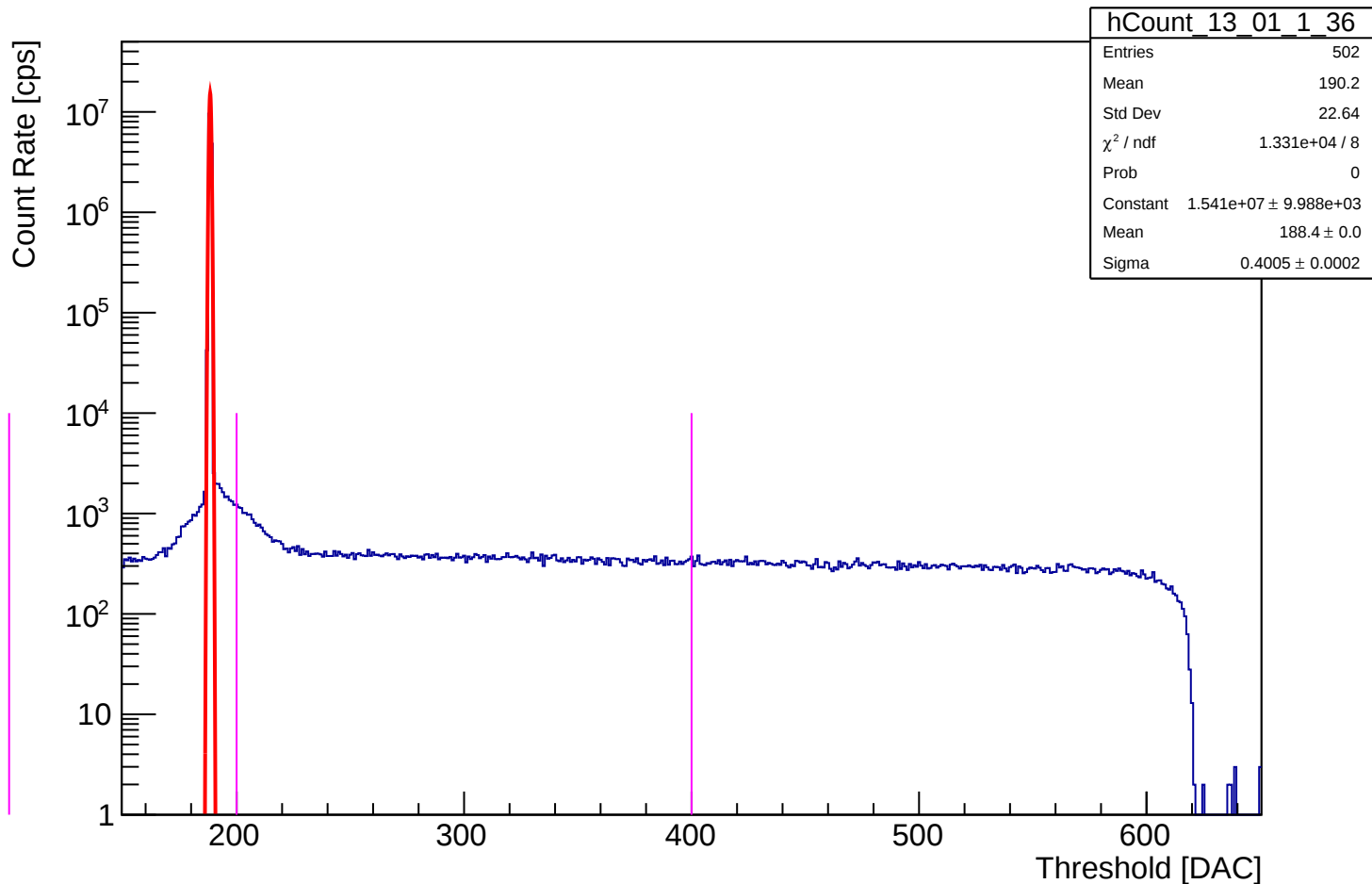
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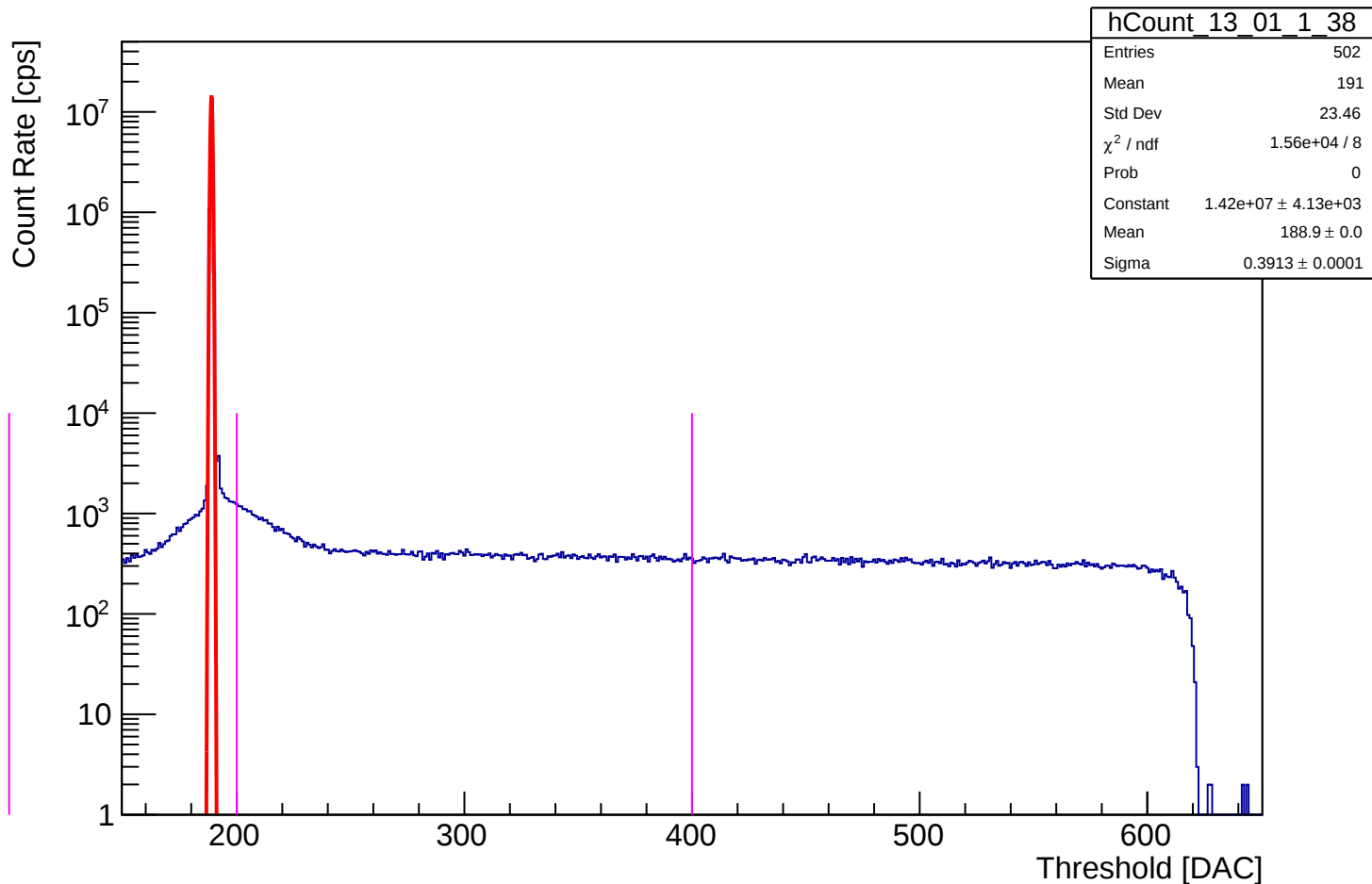
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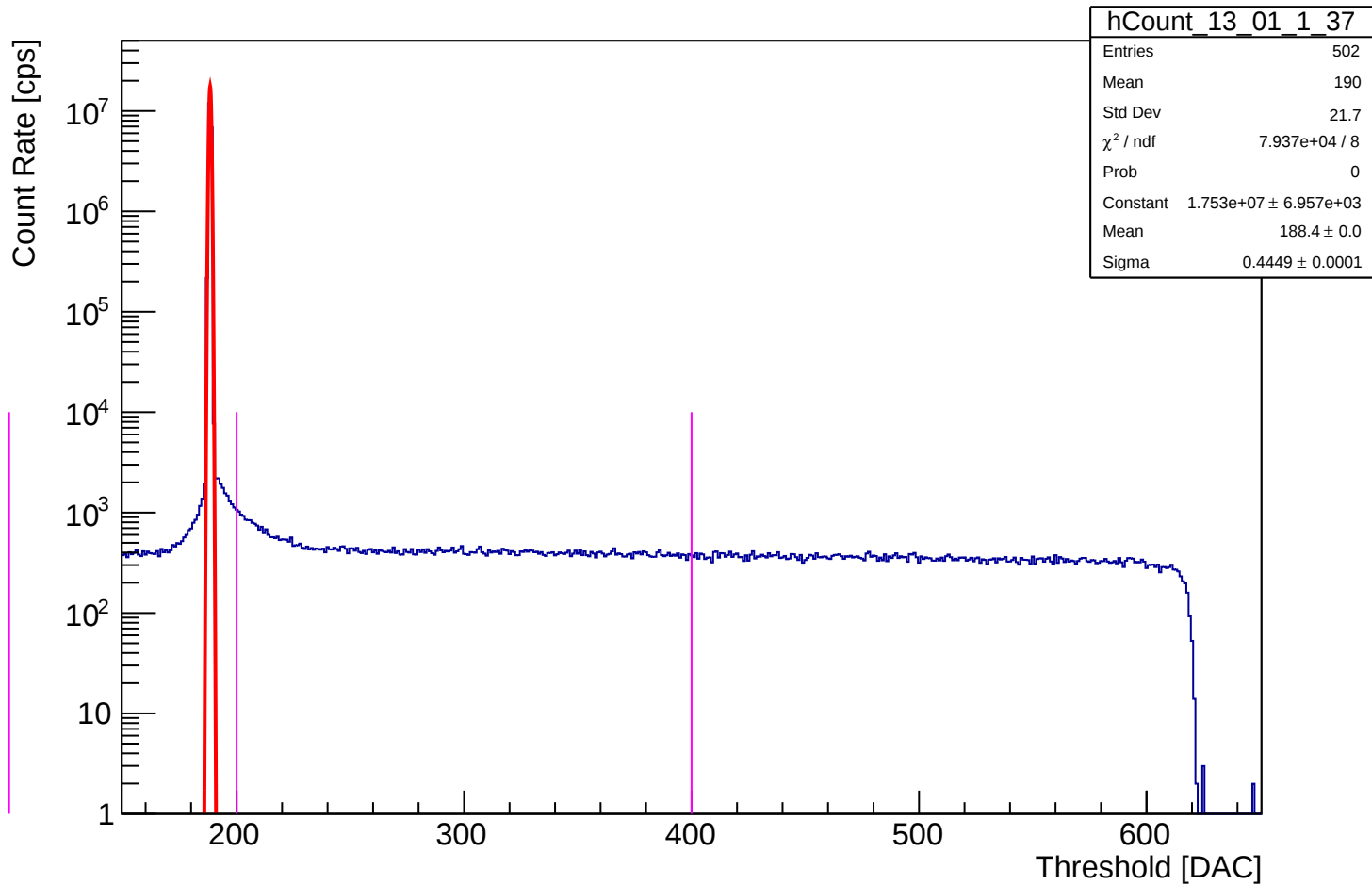
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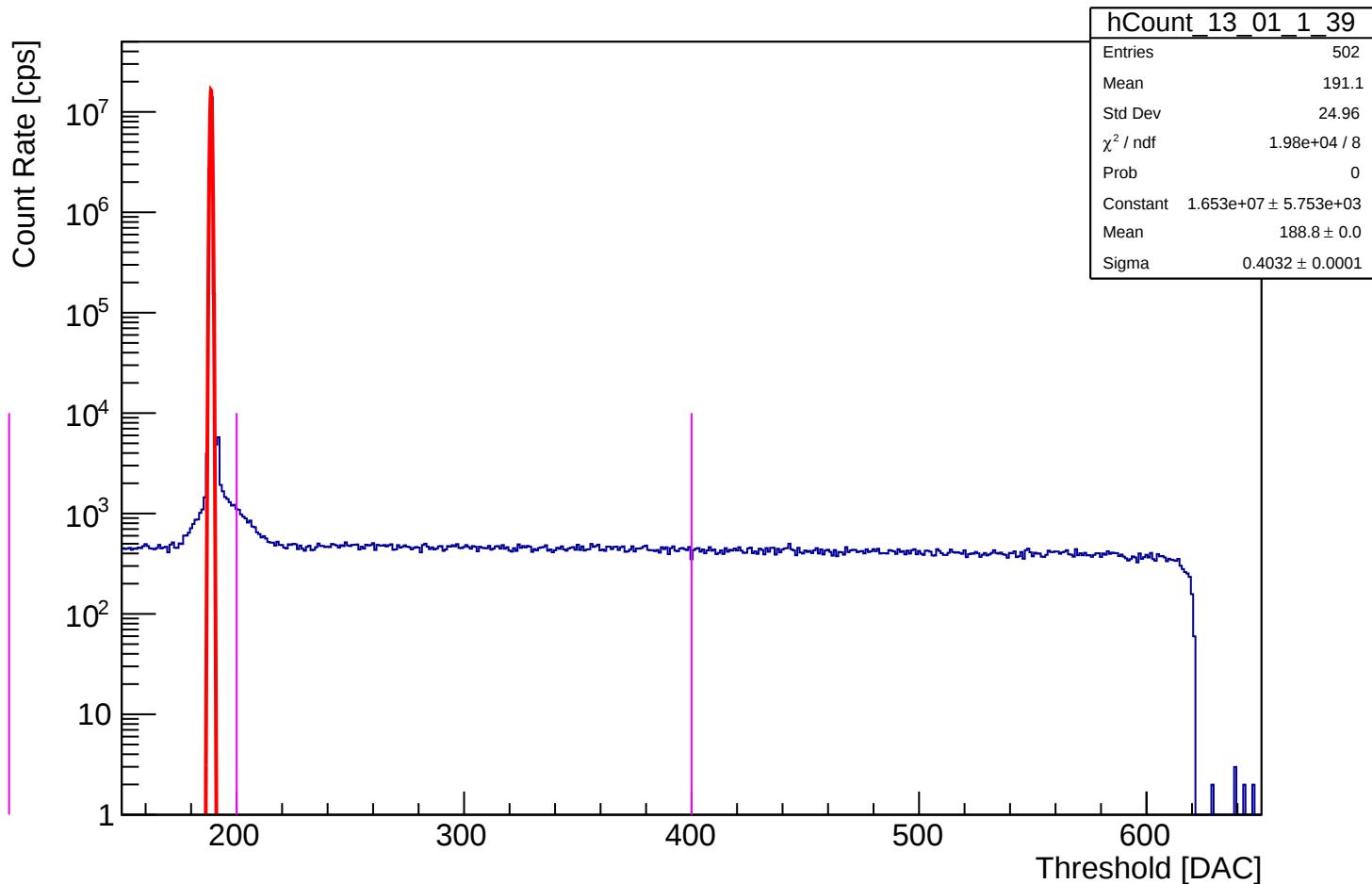
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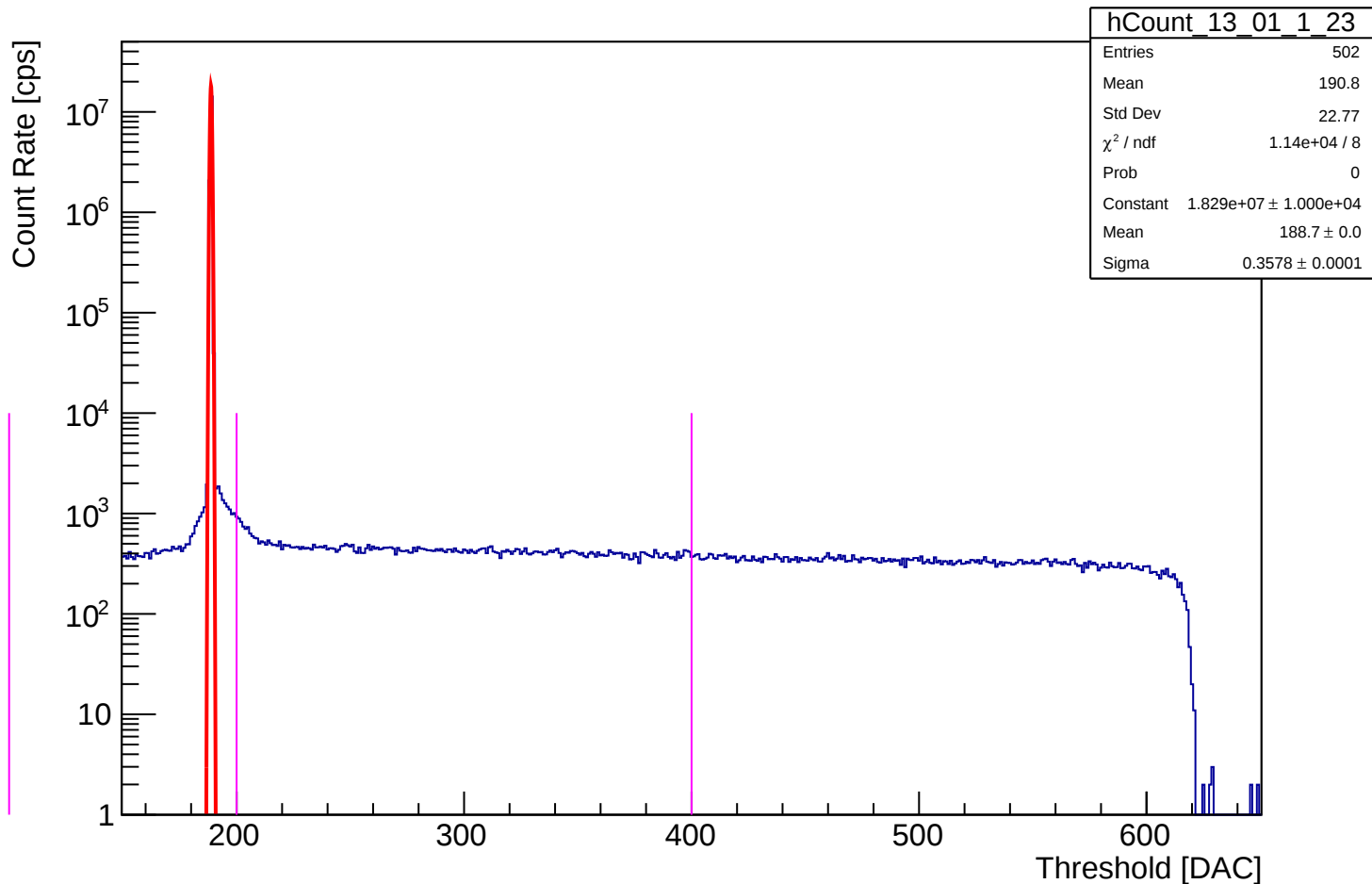
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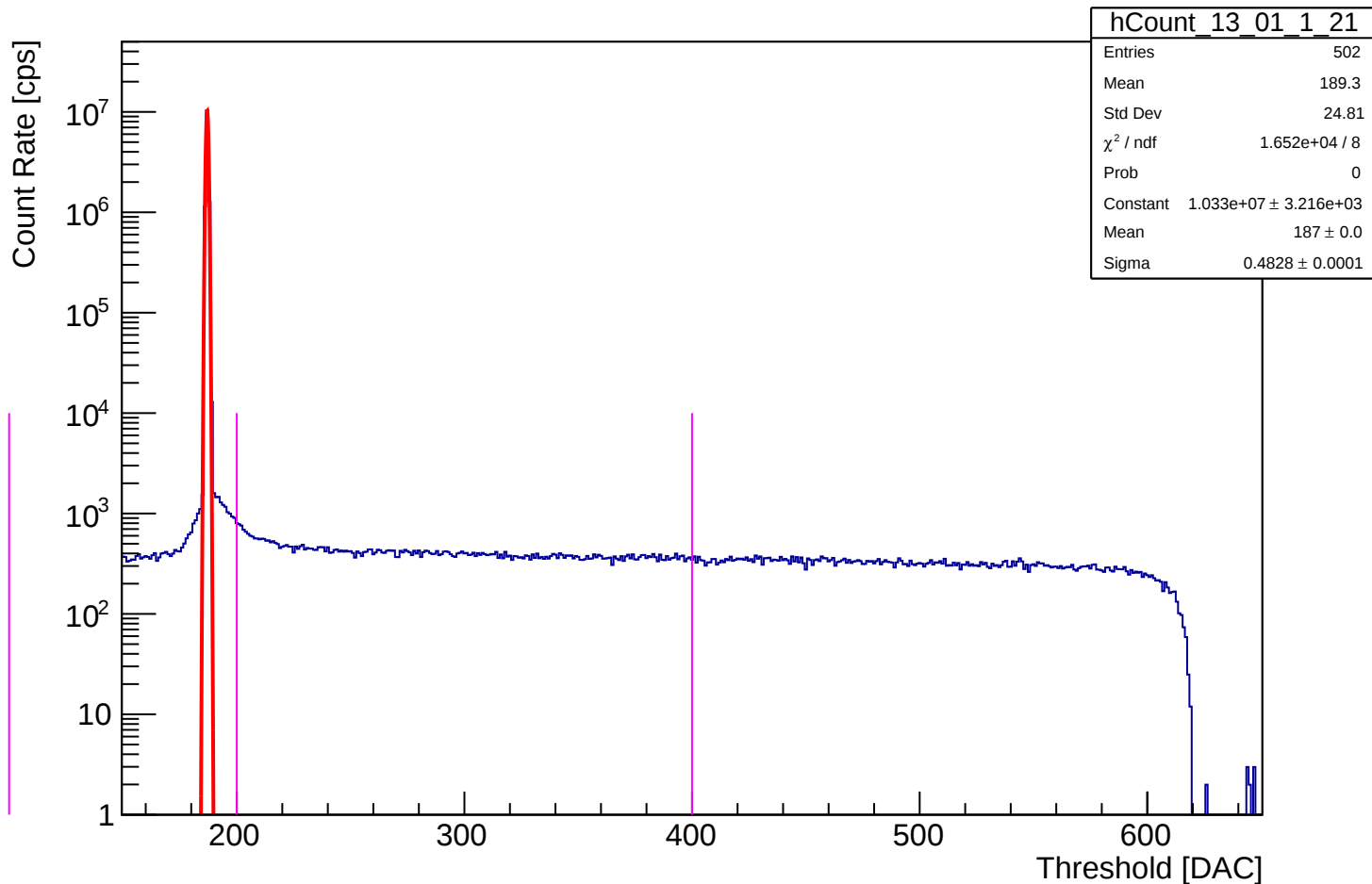
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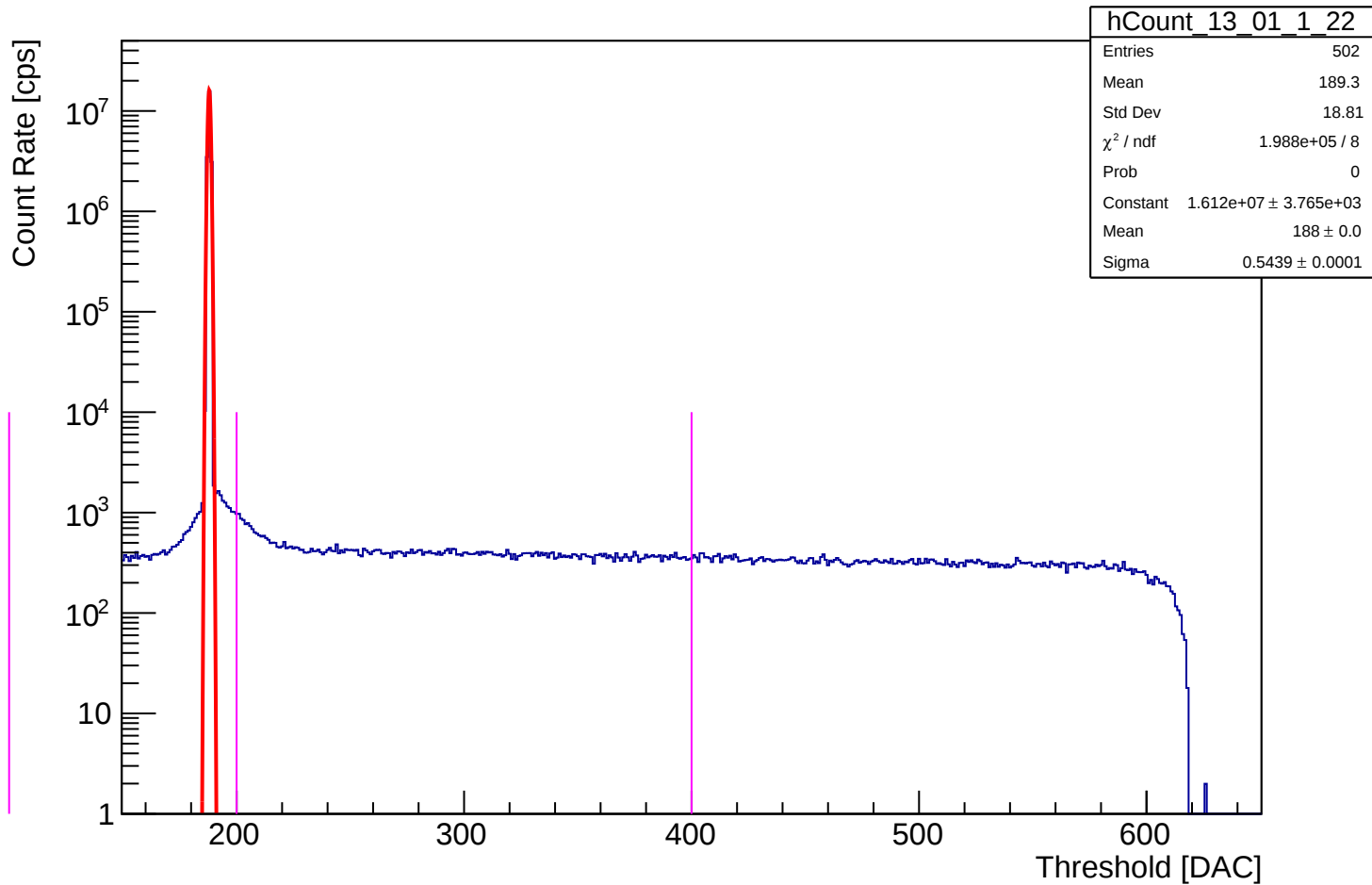
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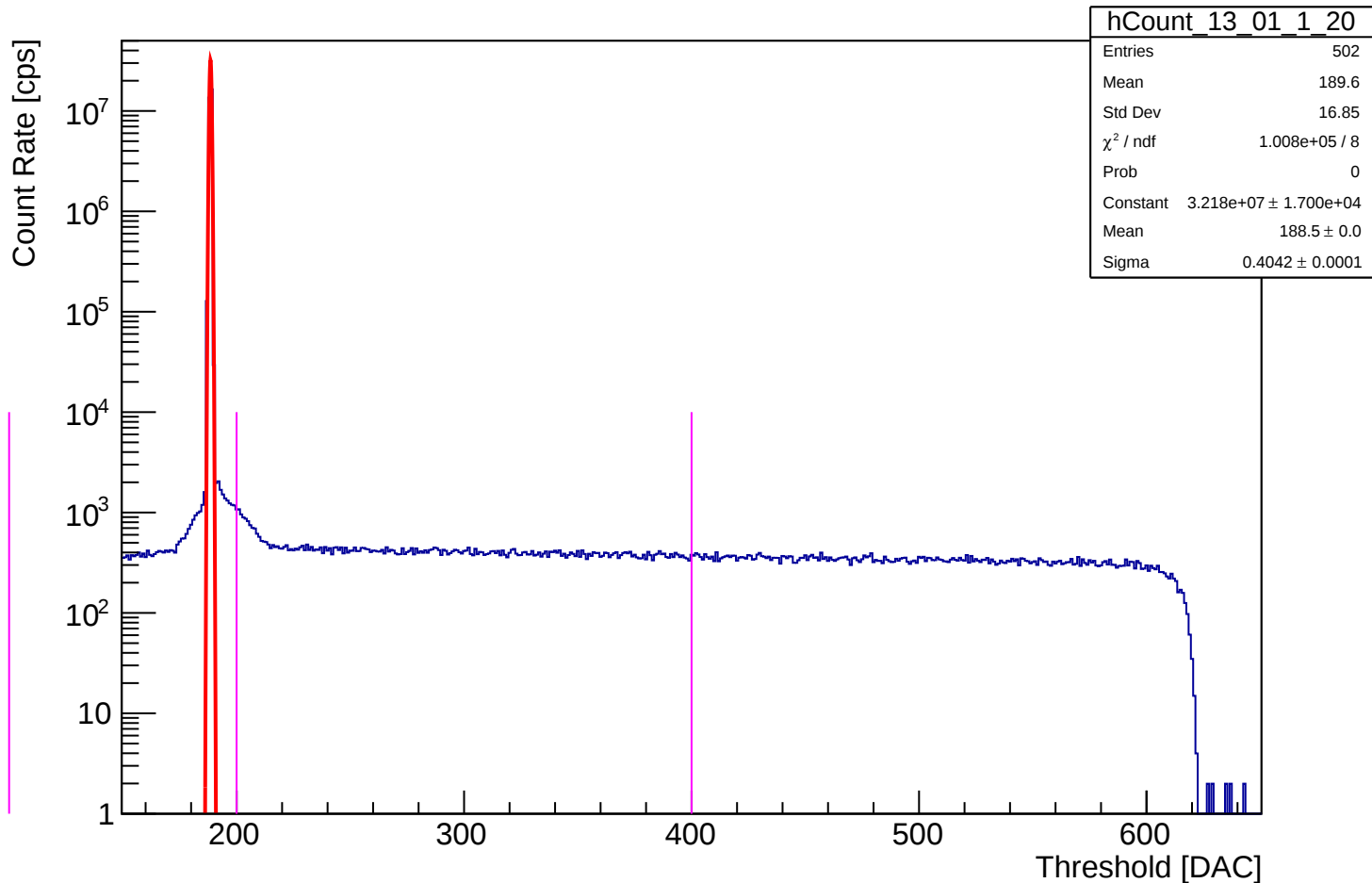
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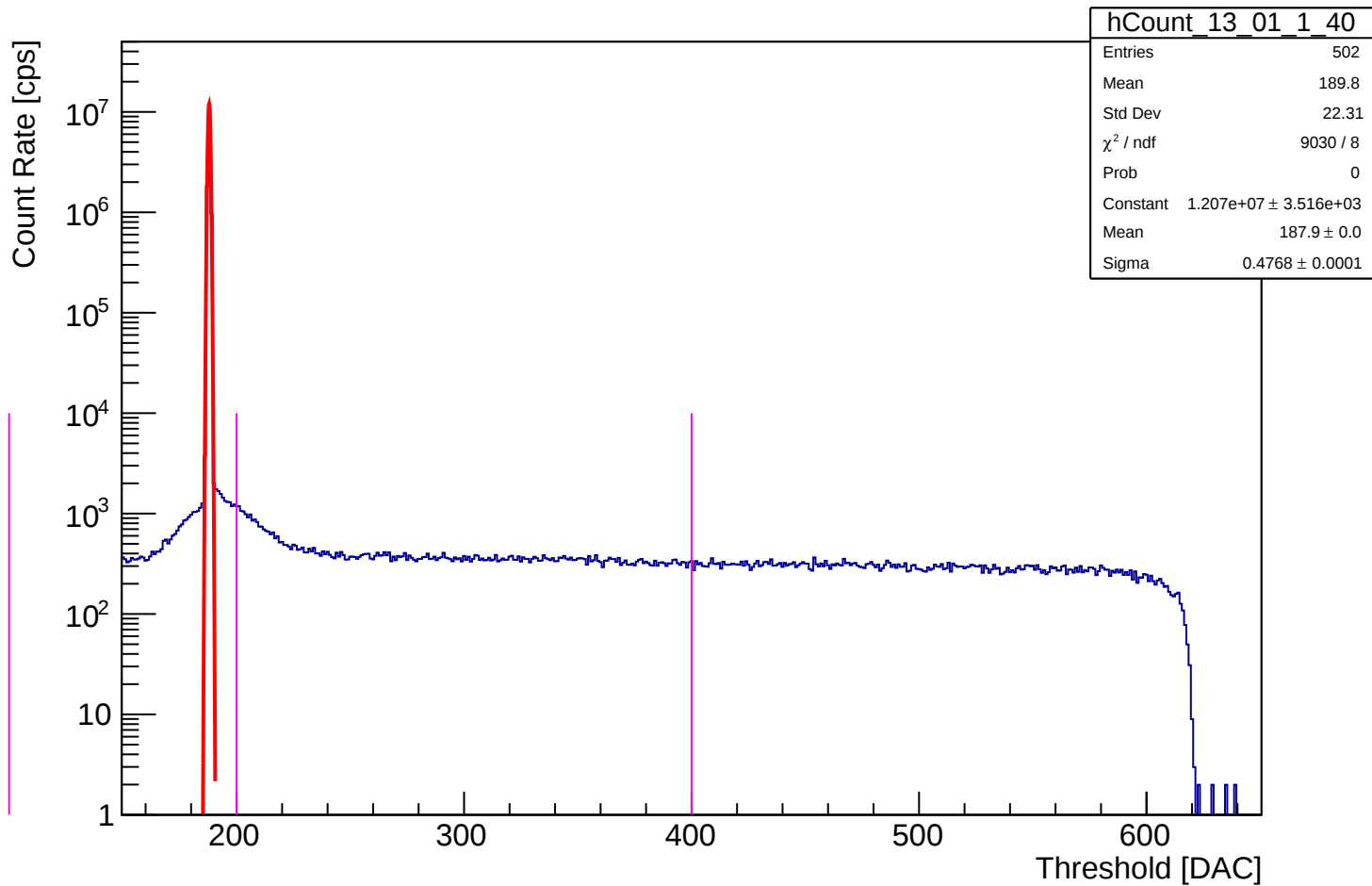
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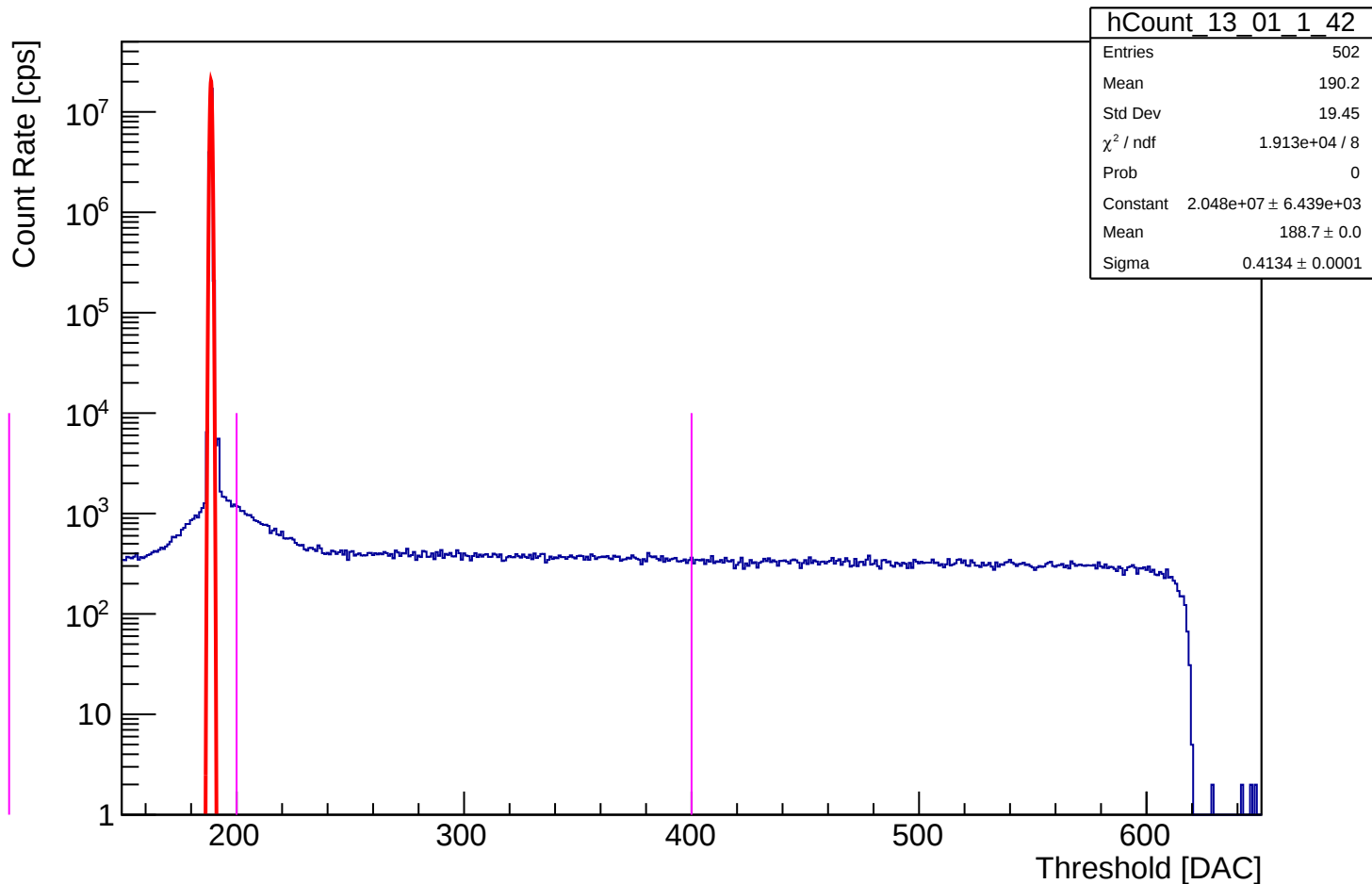
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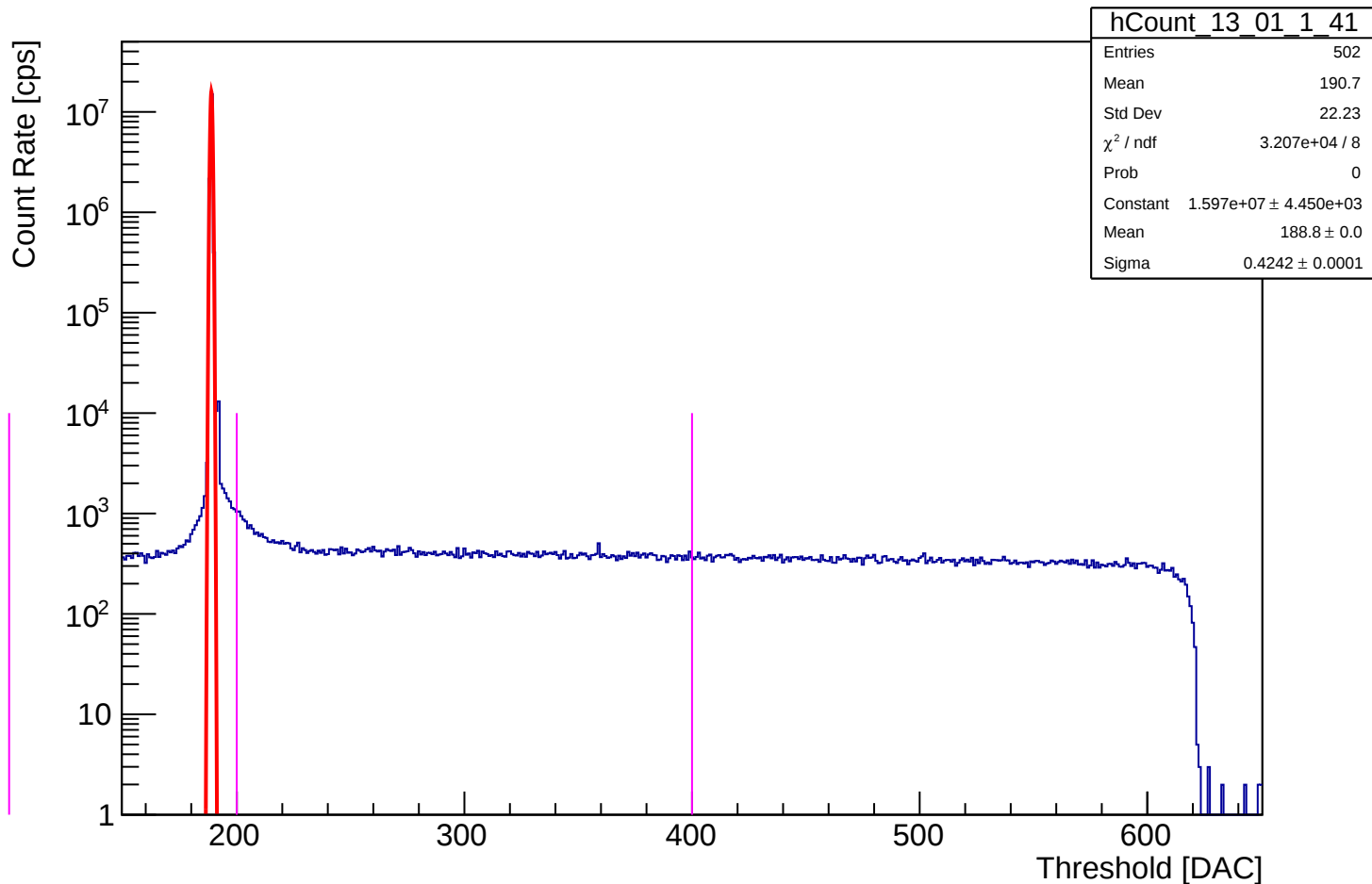
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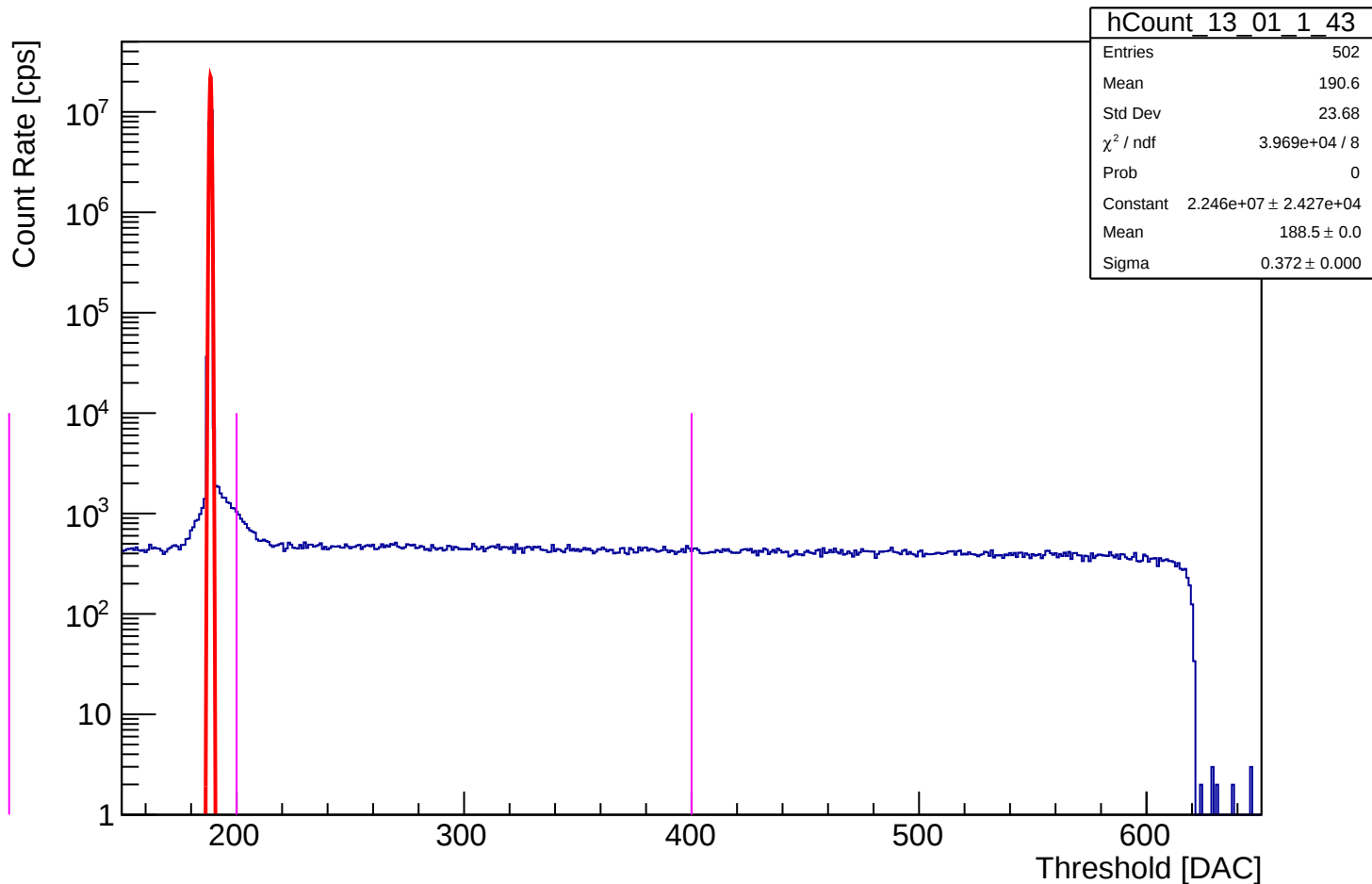
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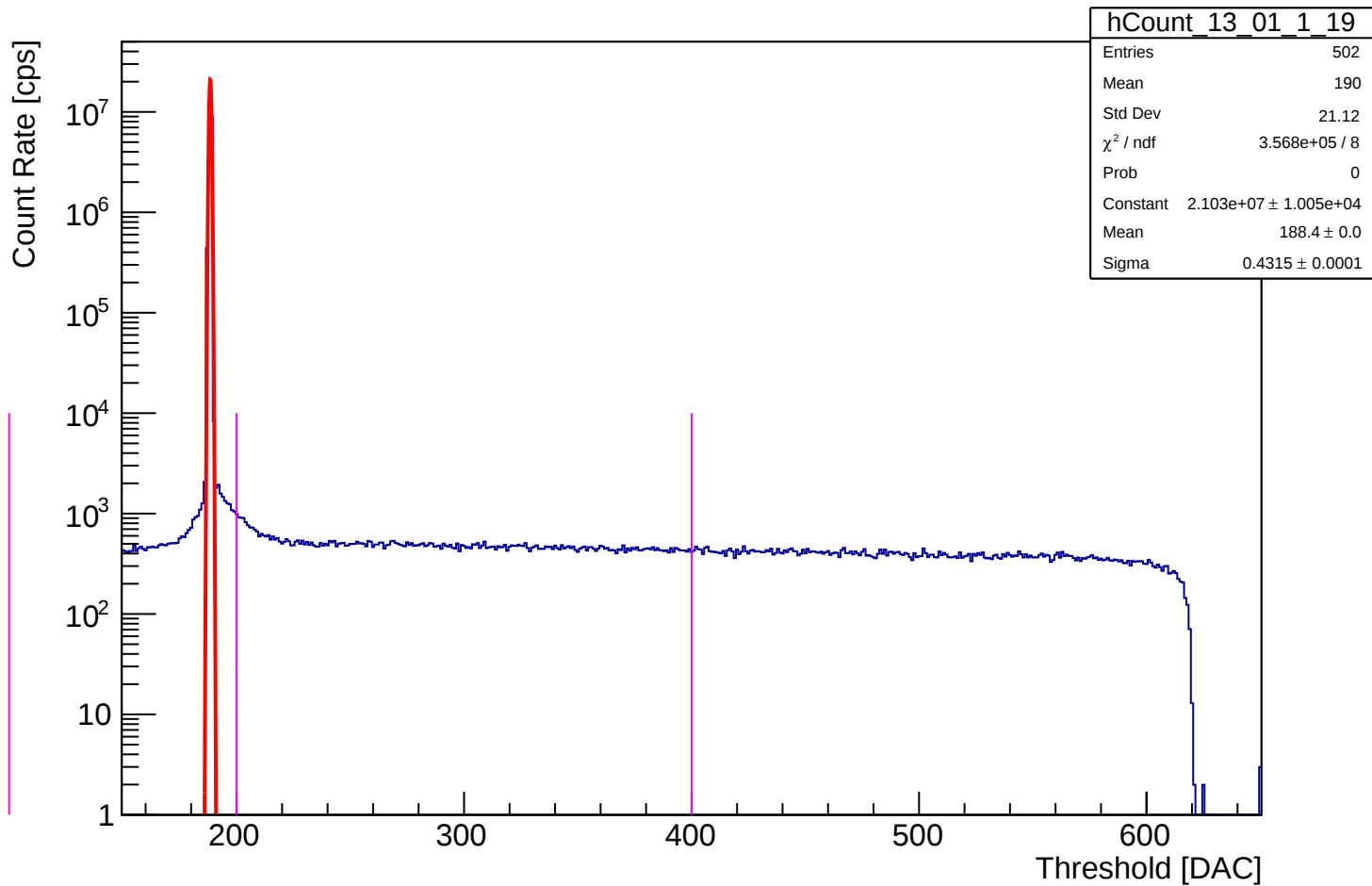
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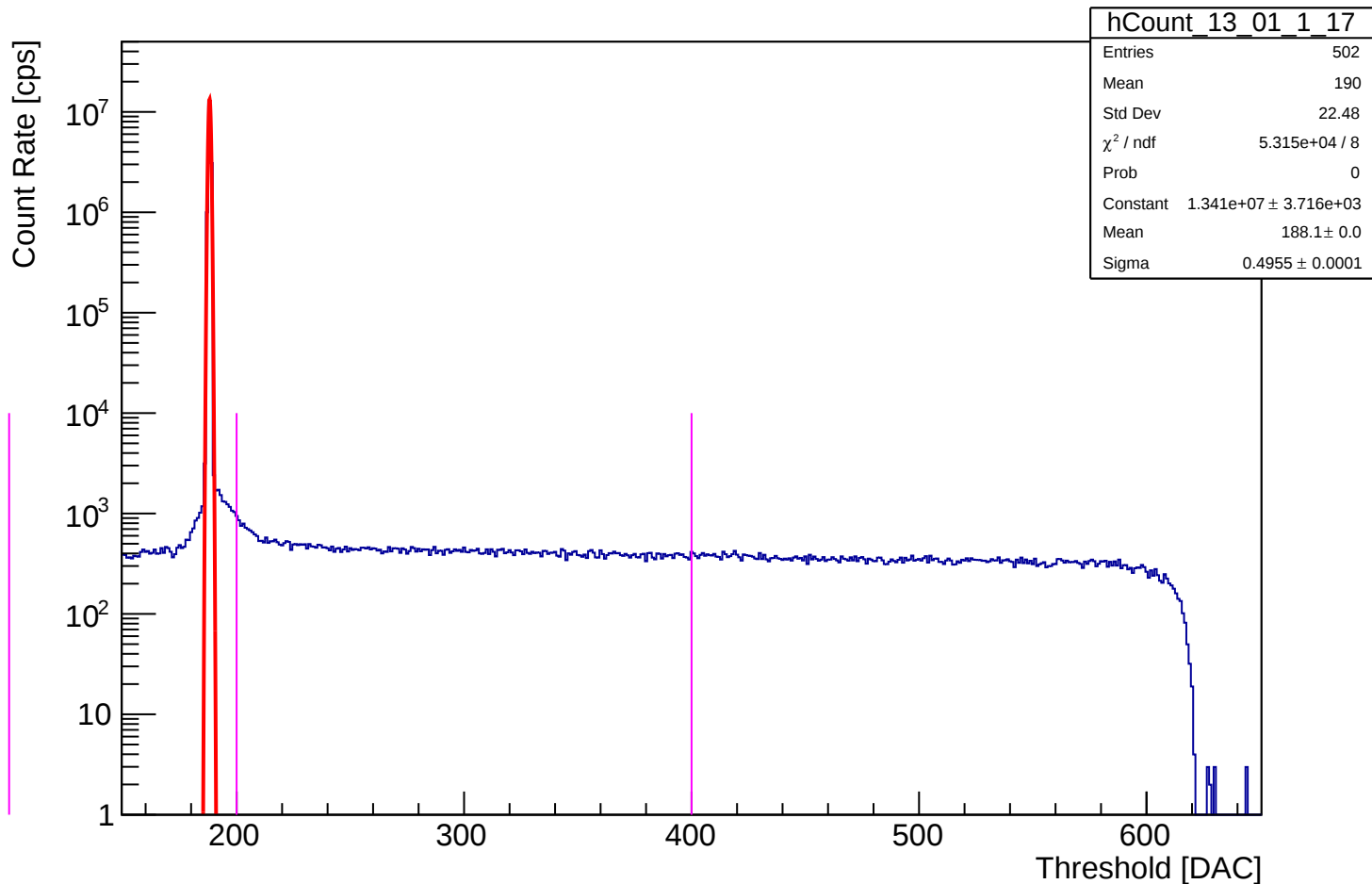
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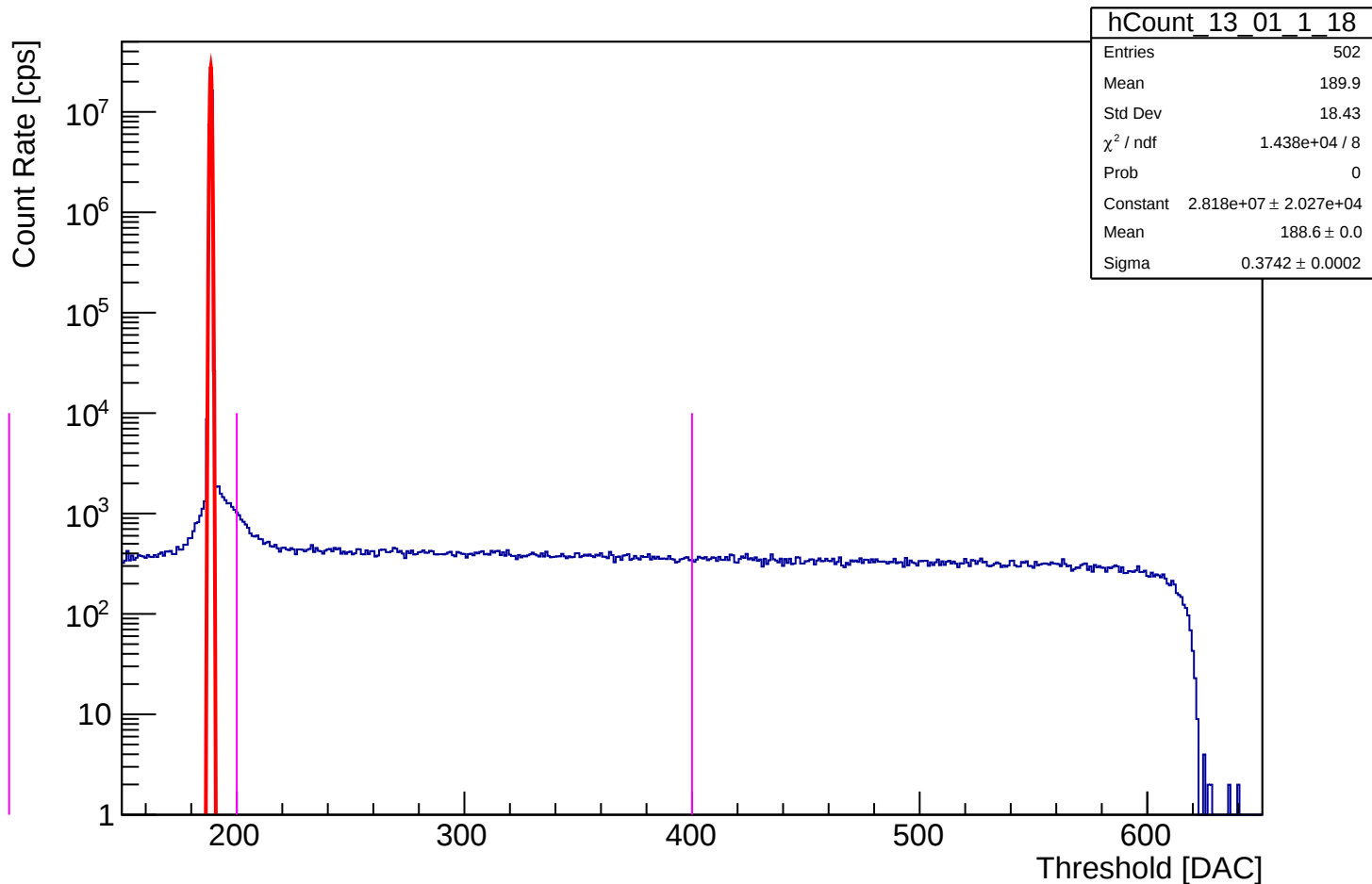
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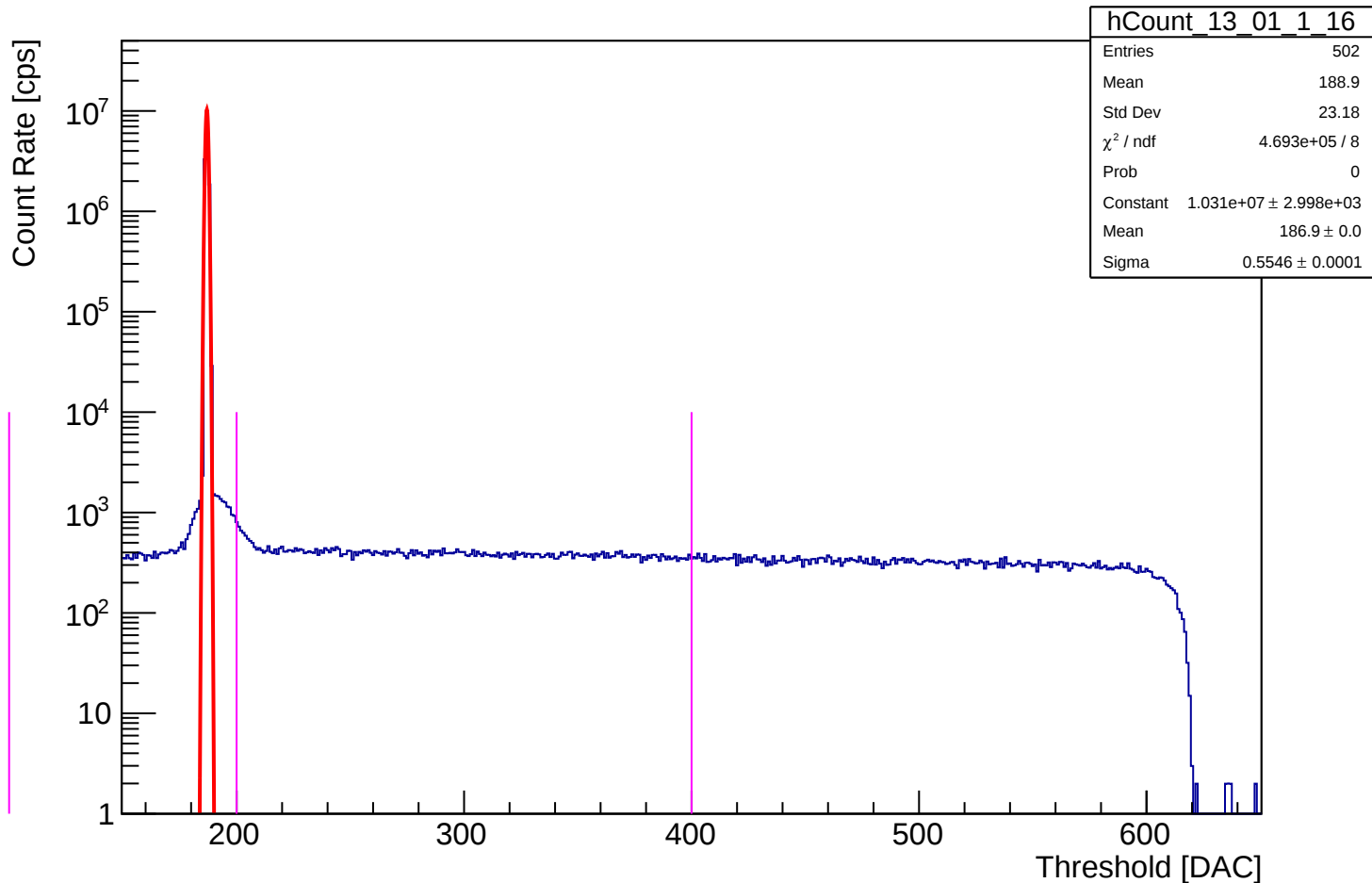
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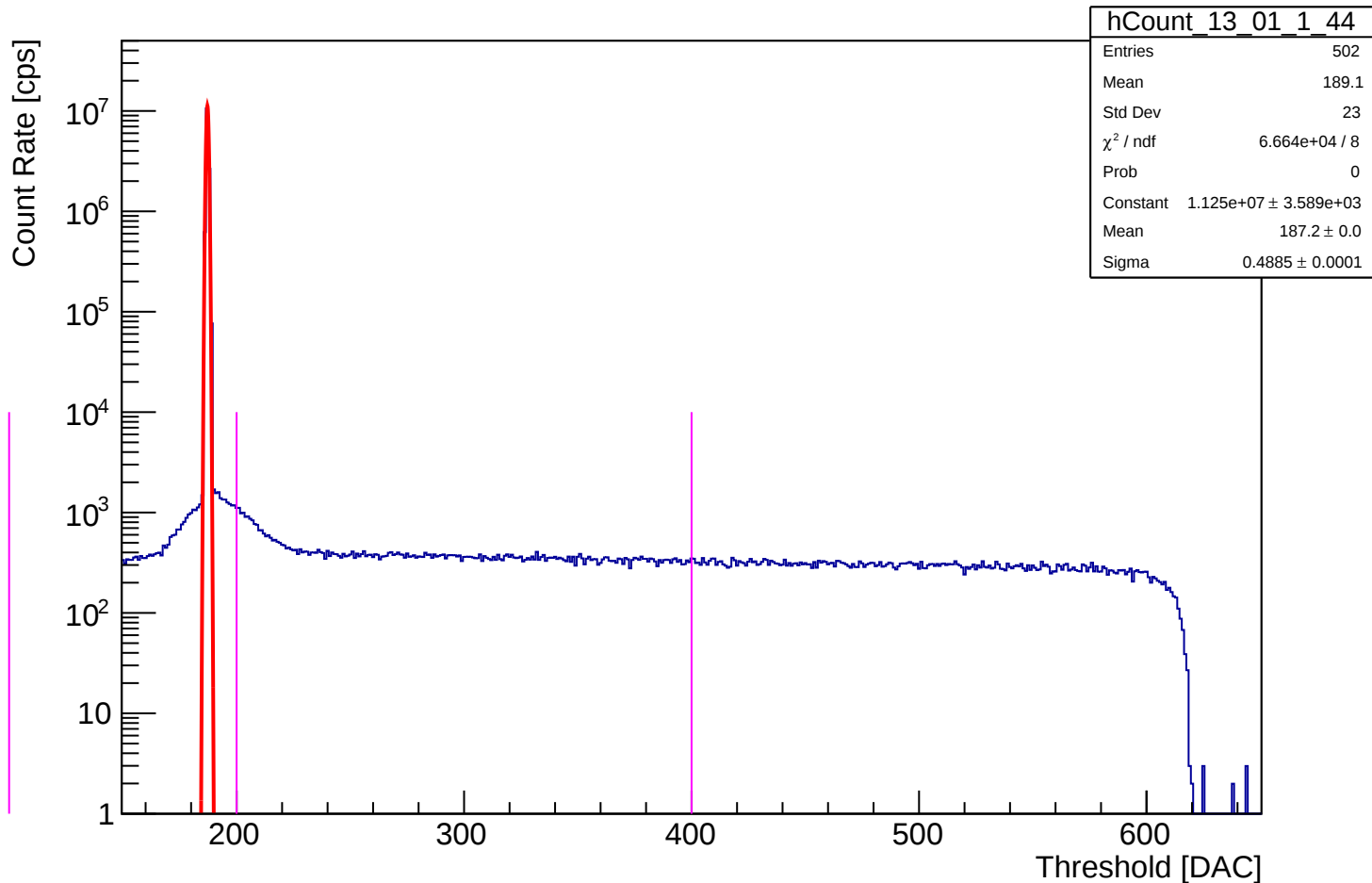
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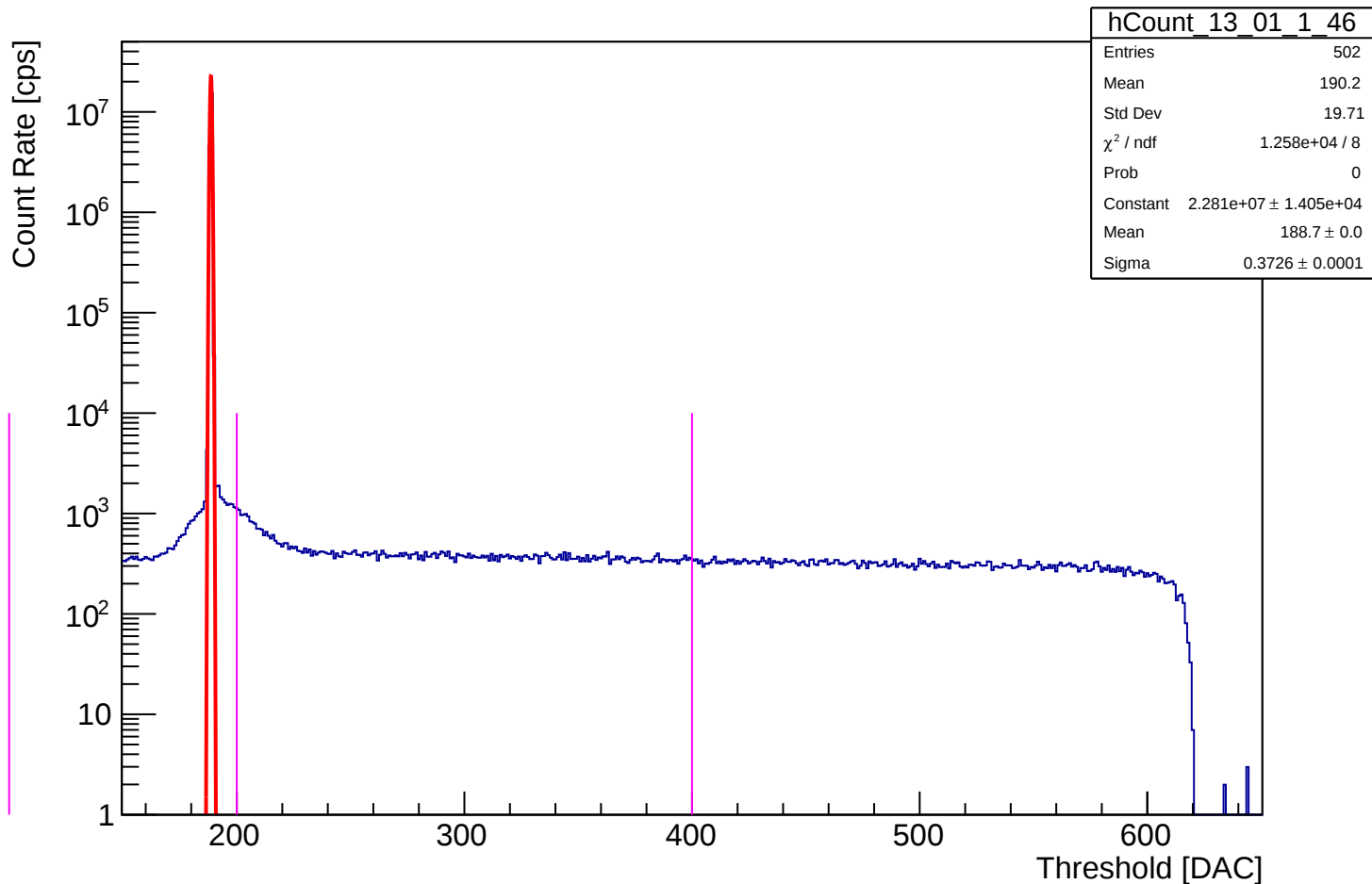


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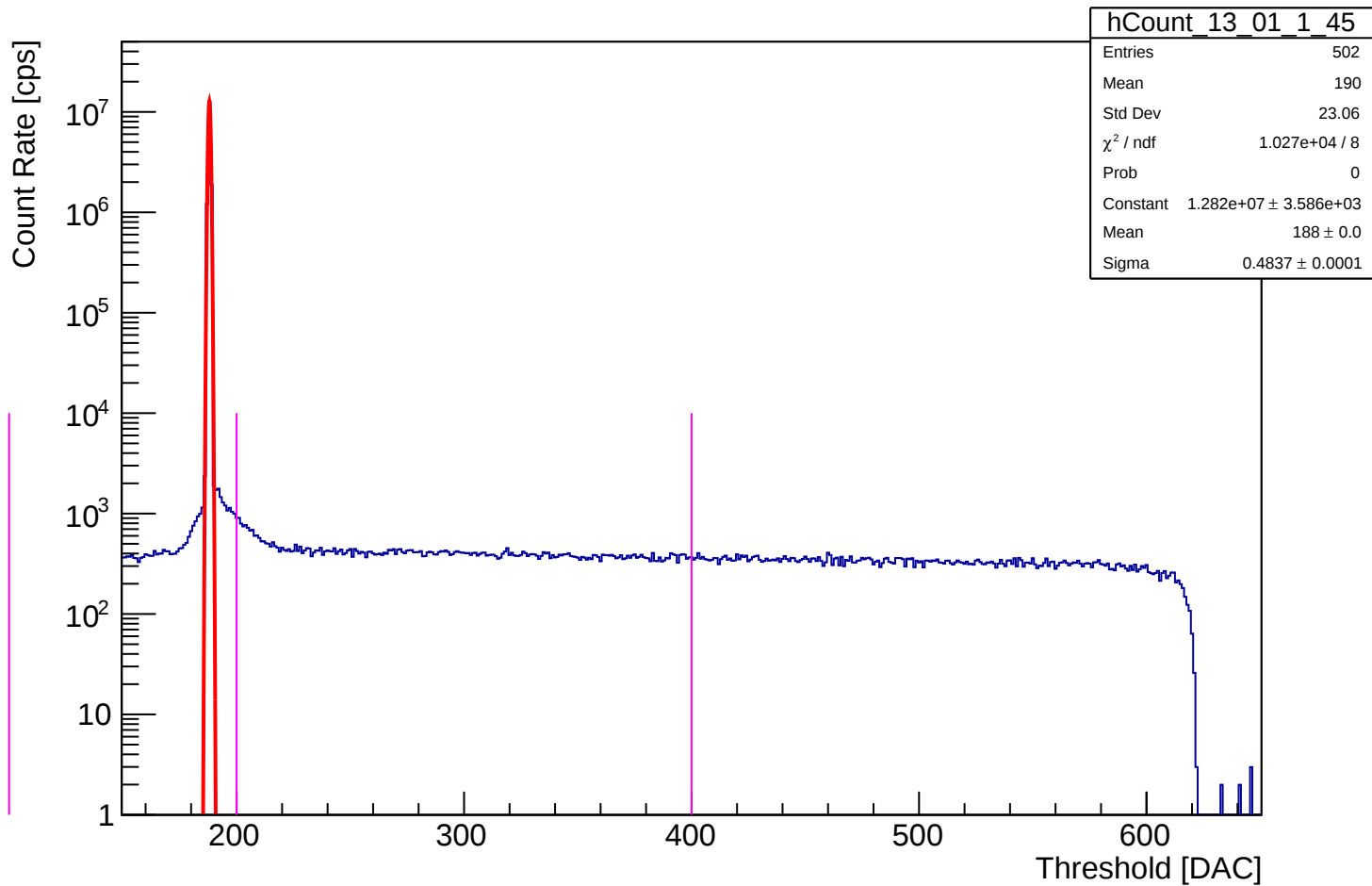


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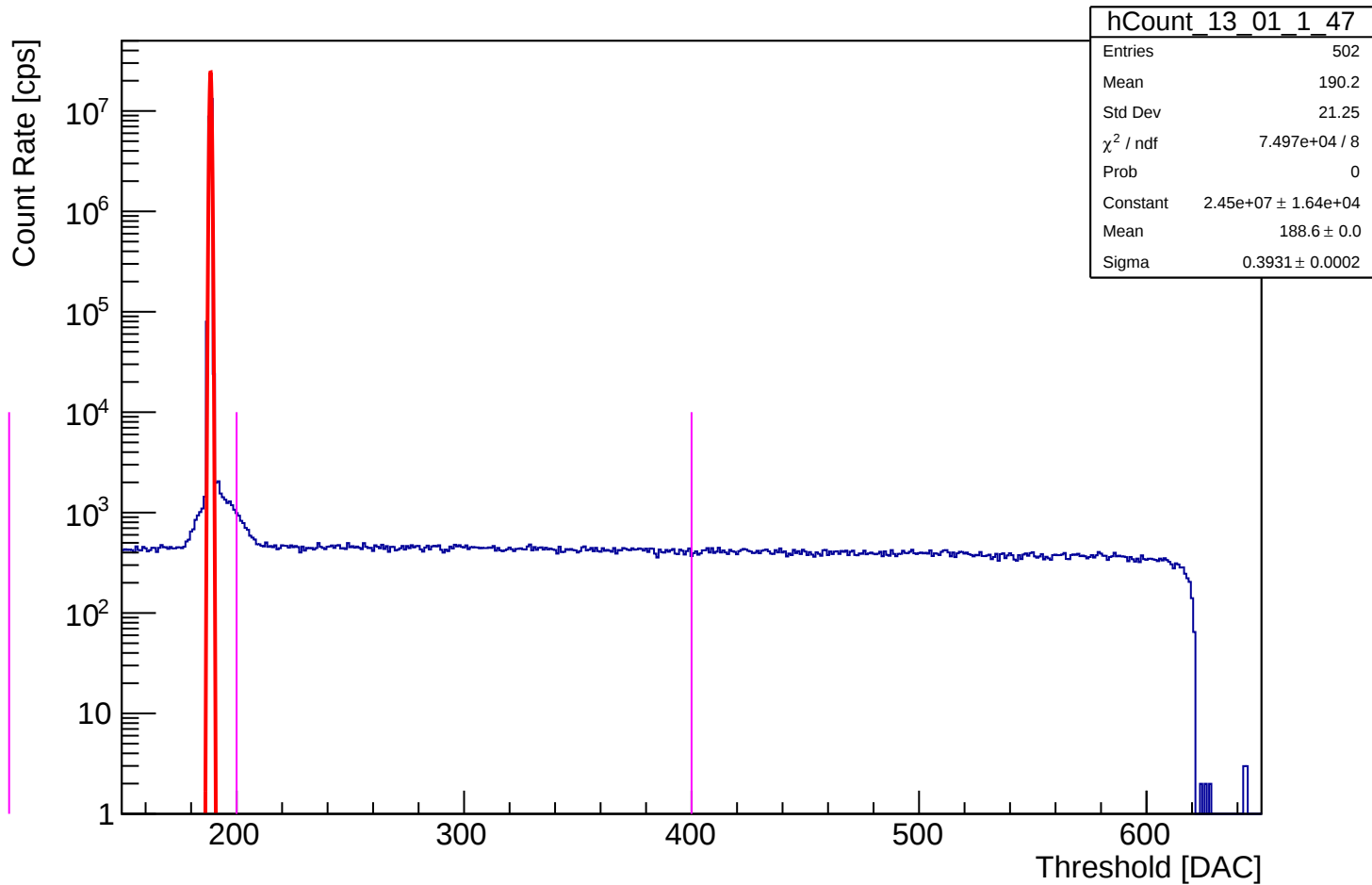




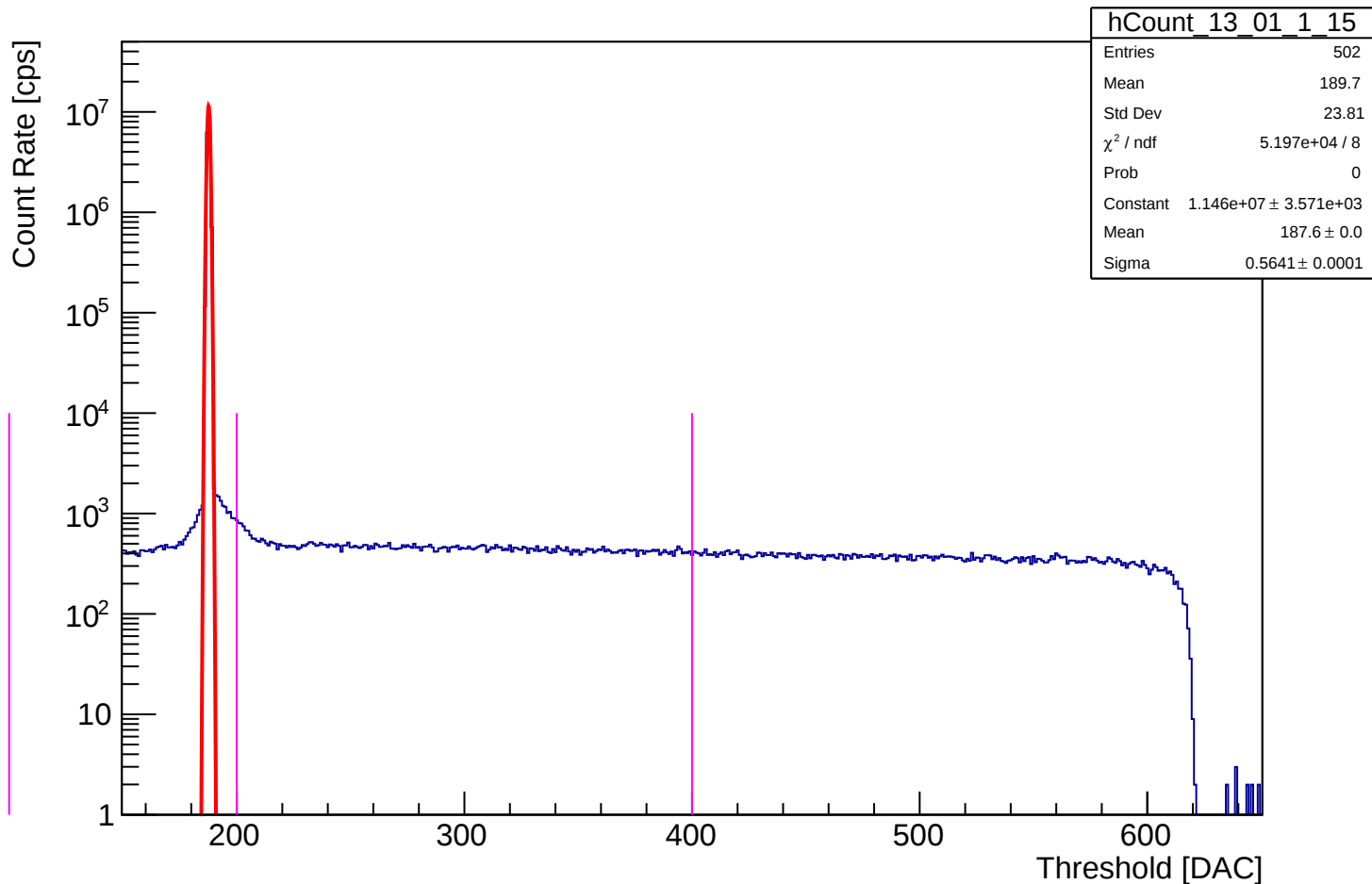
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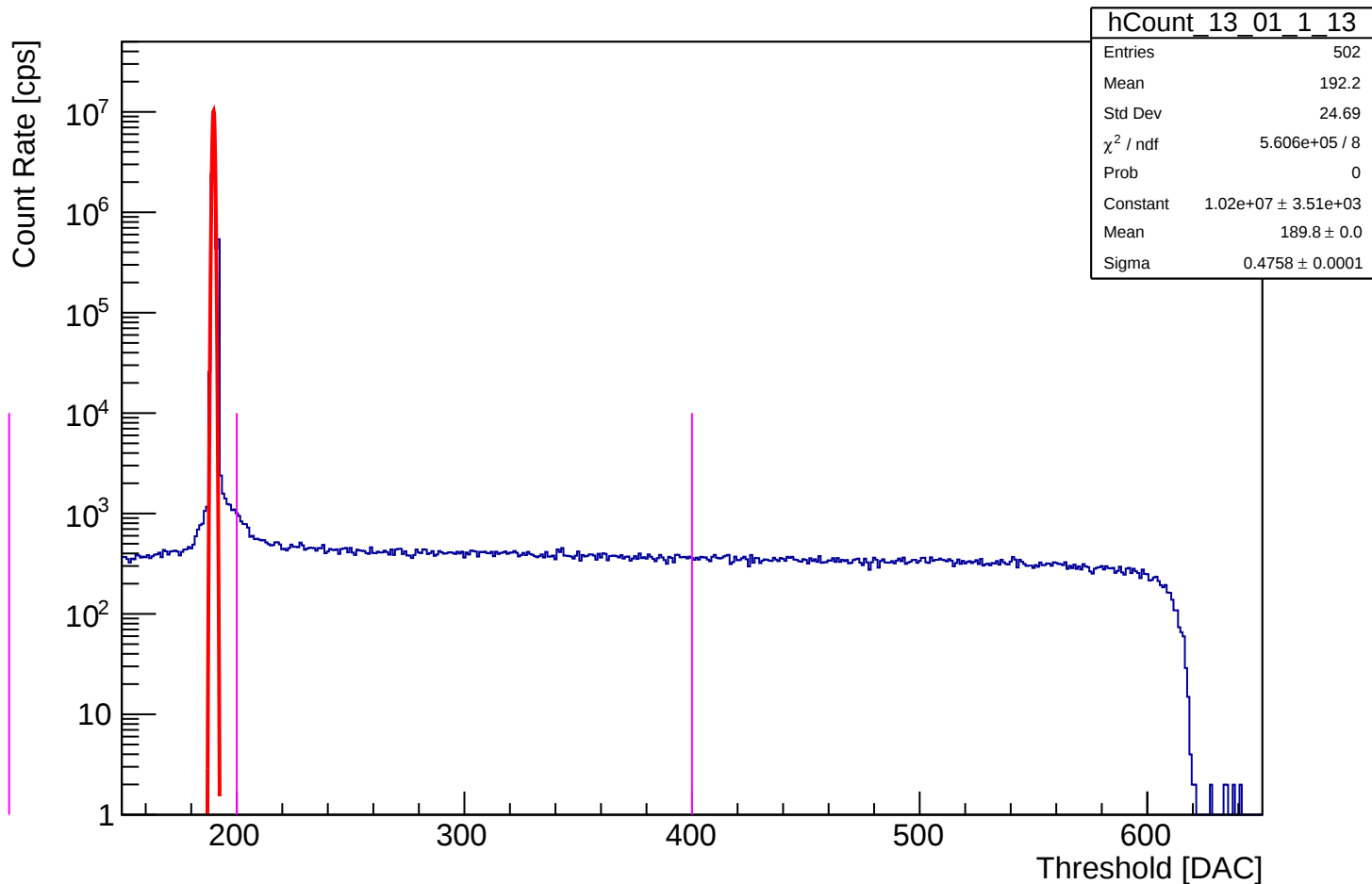
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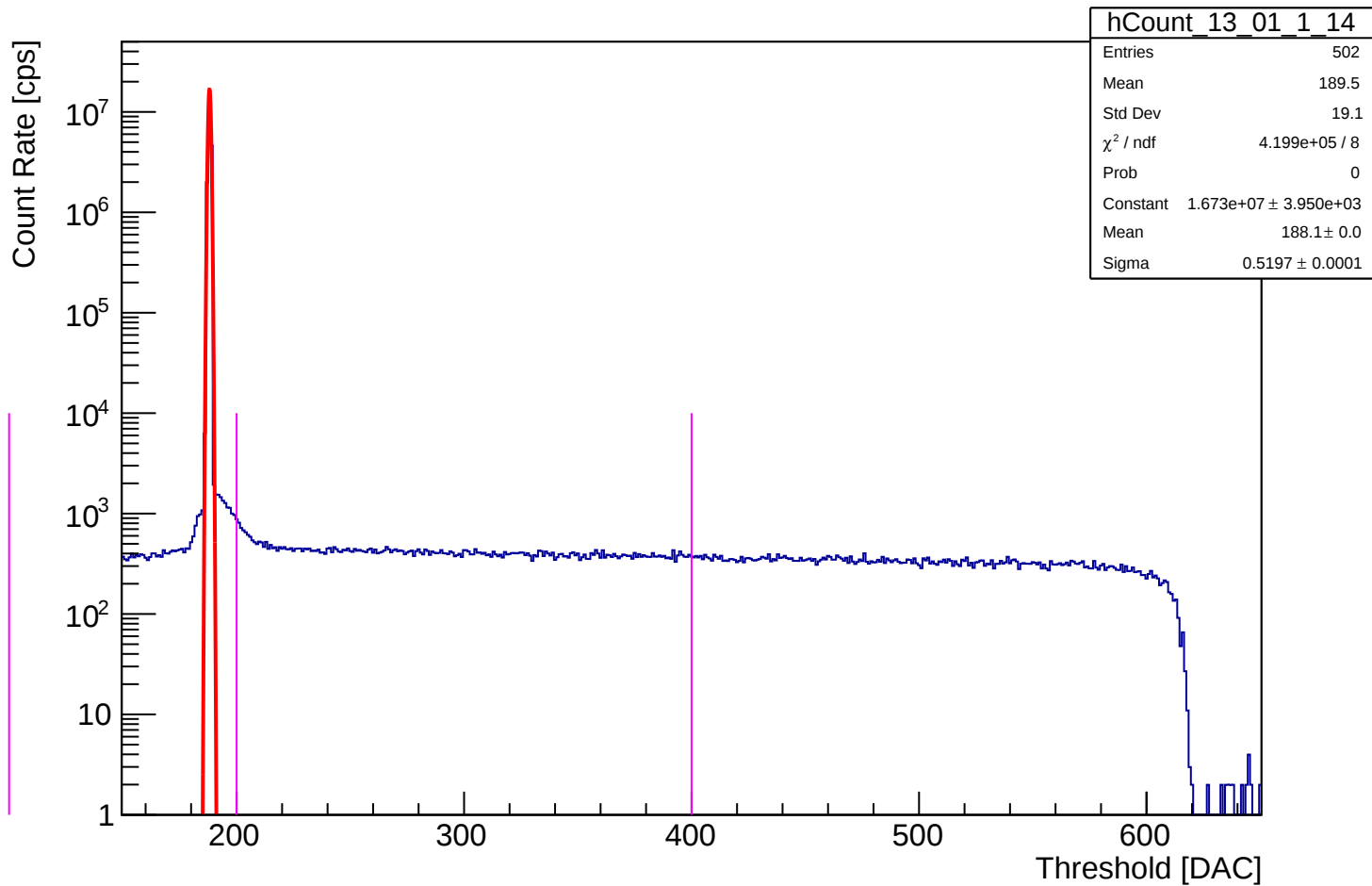
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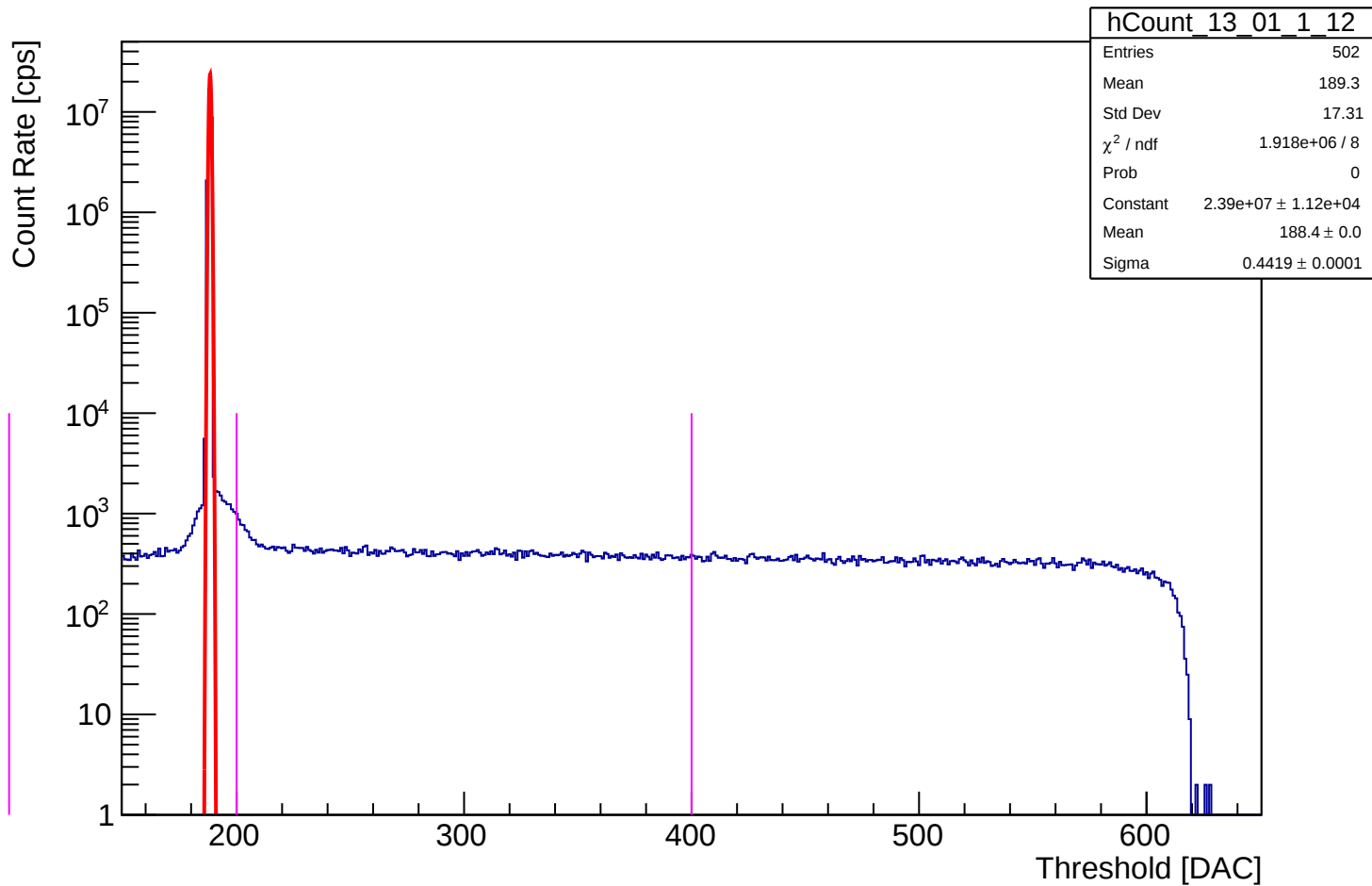
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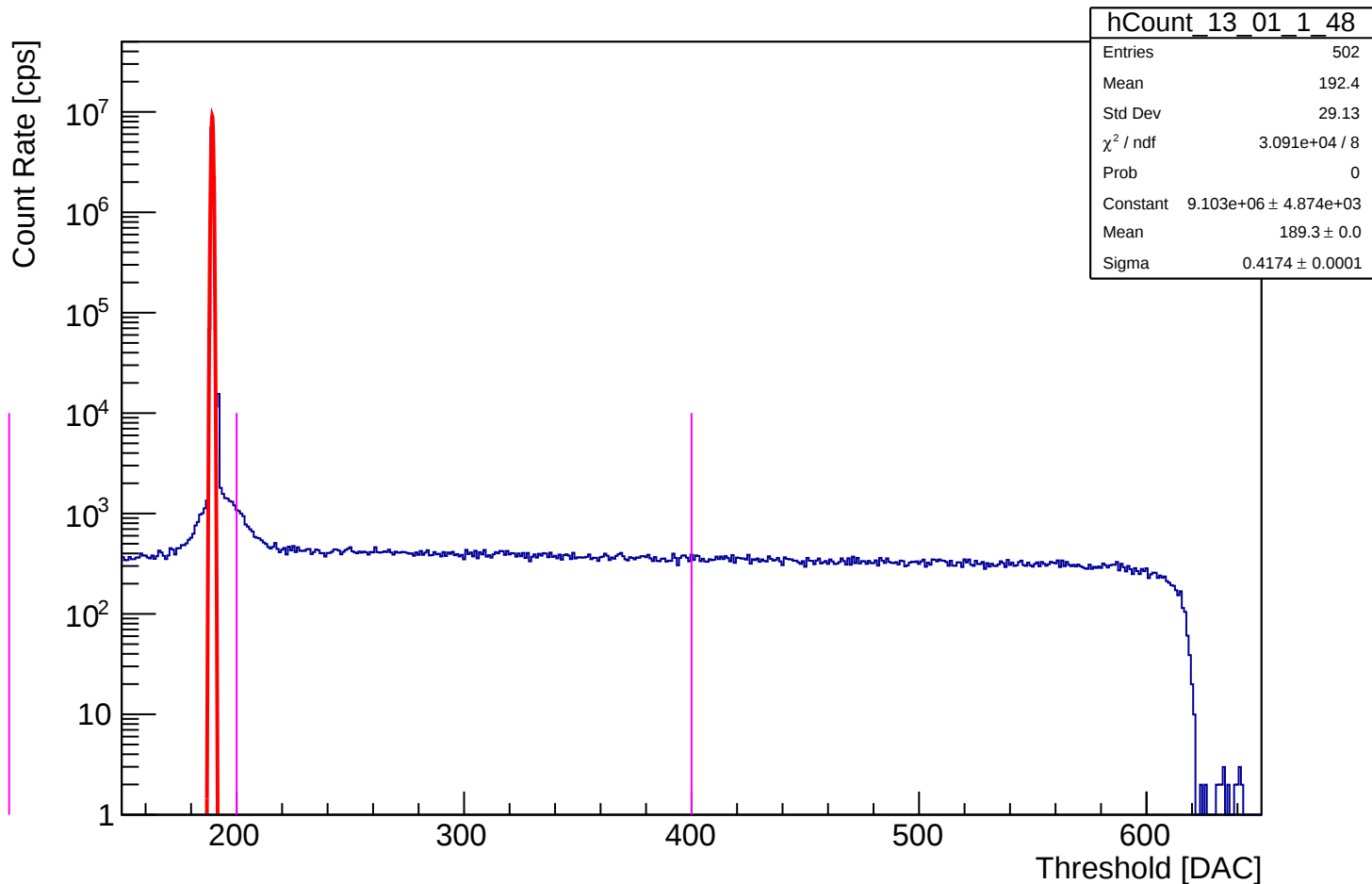
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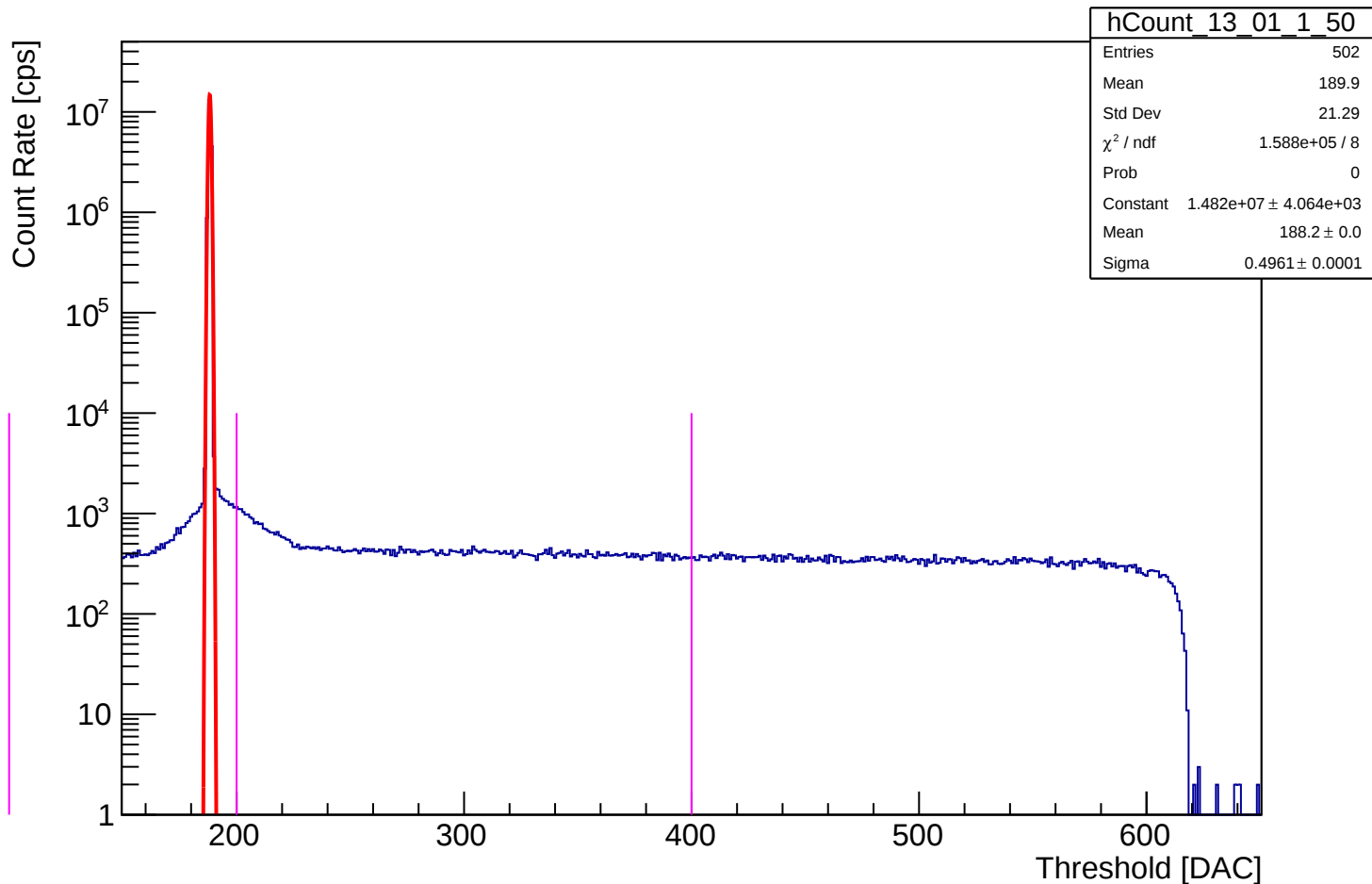
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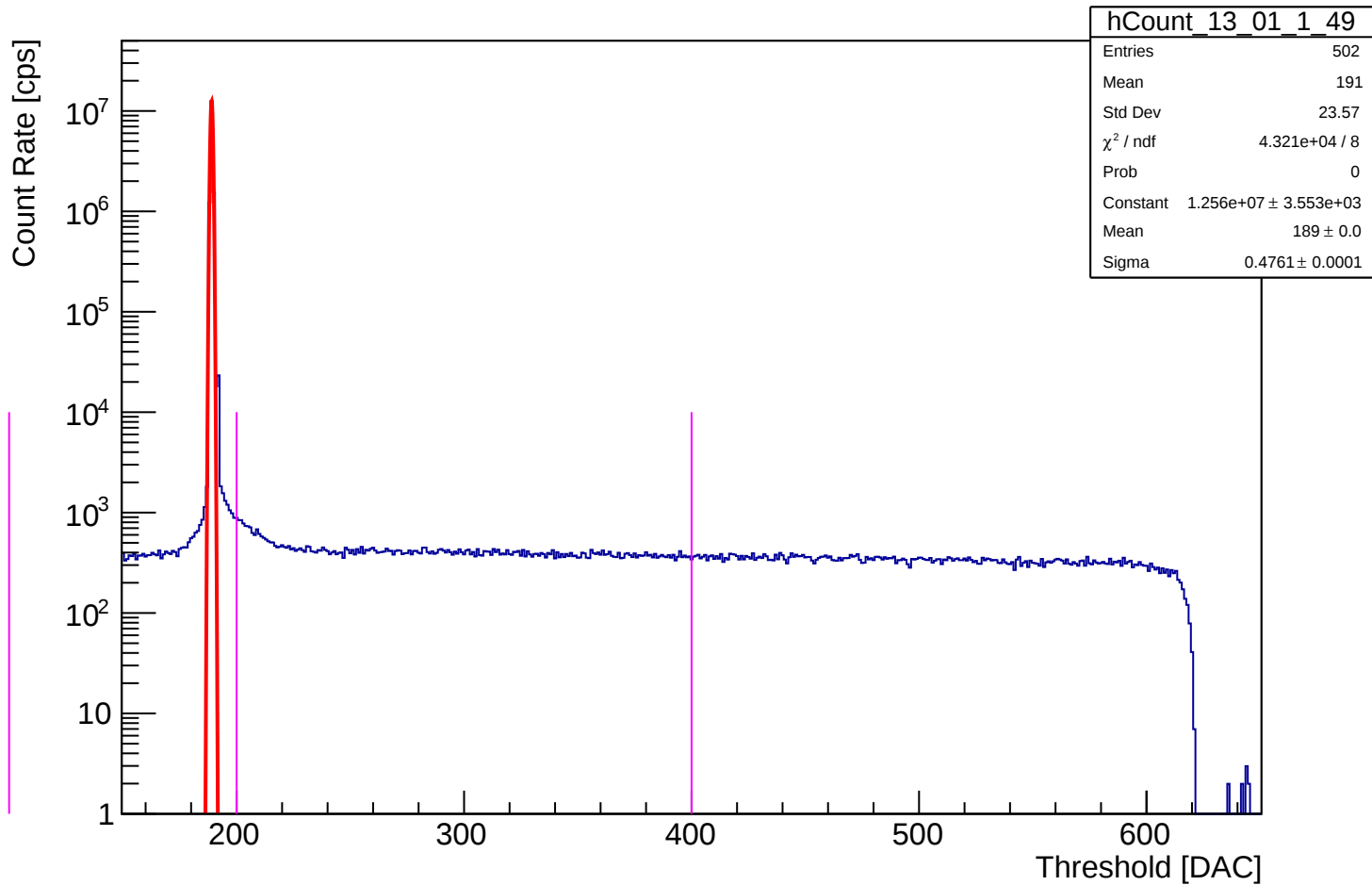
Row 1 Tile 1 Pmt 5 Pixel 37 Slot 13 Fiber 1 Asic 1 Channel 48



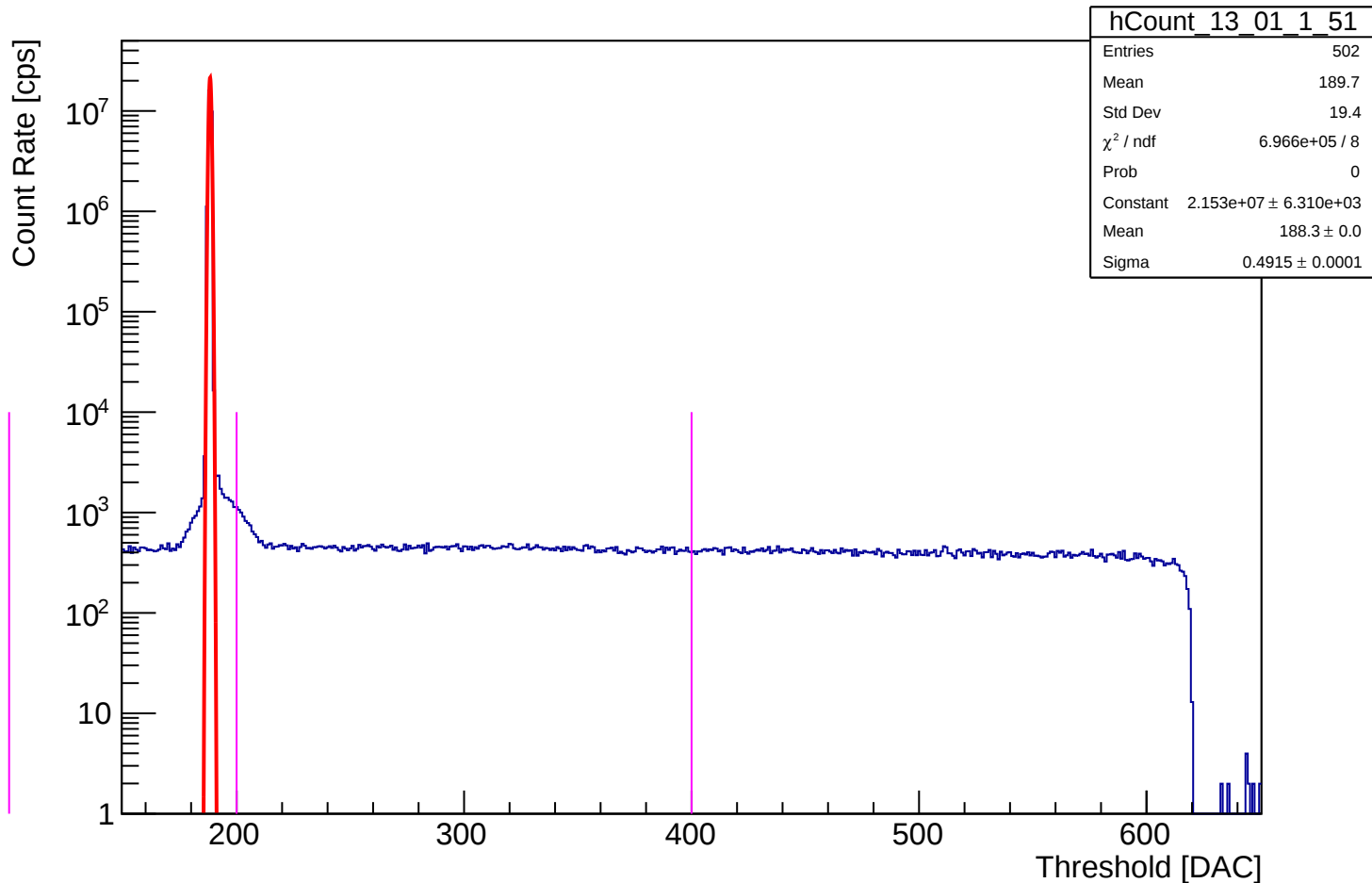
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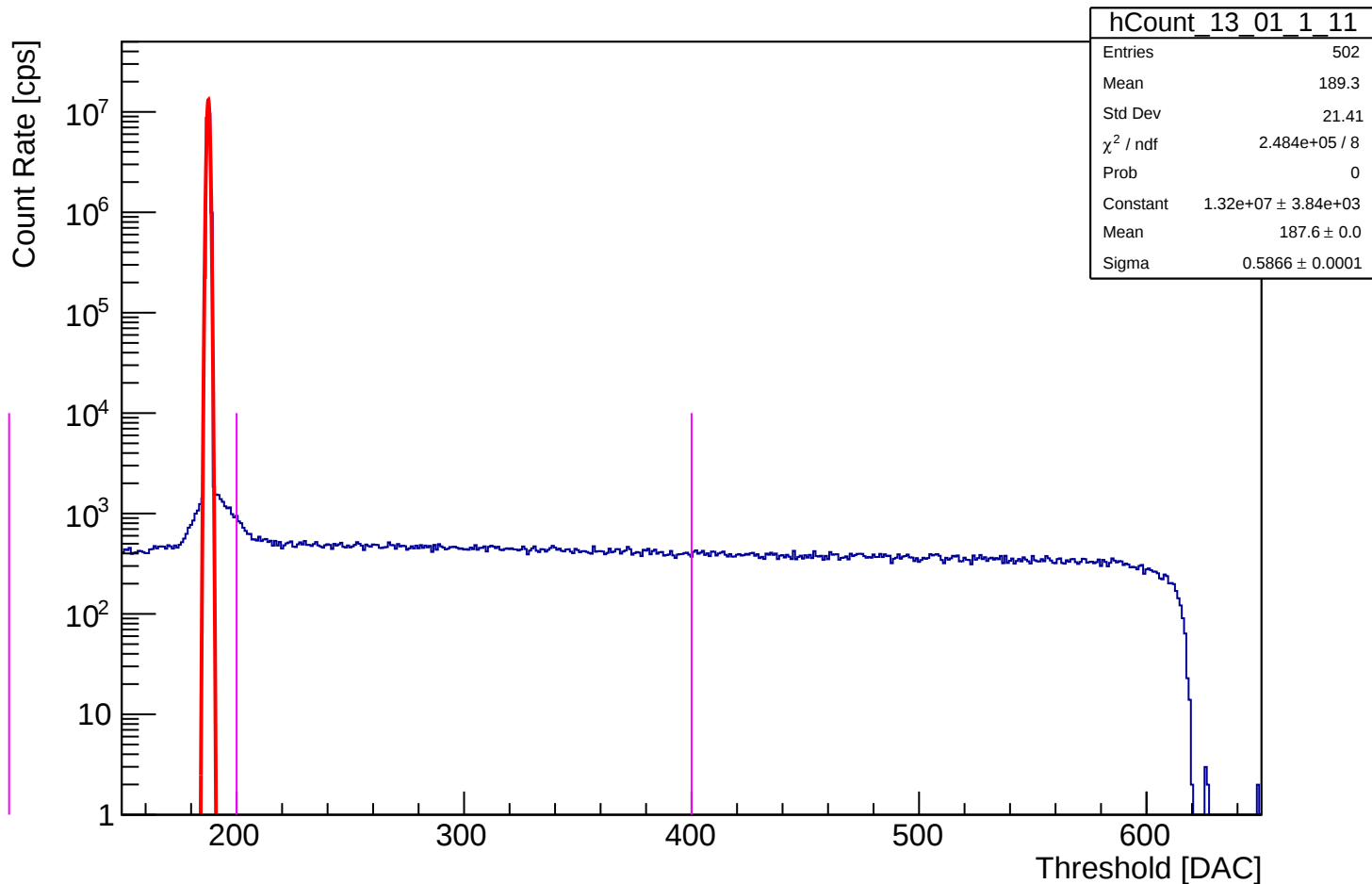
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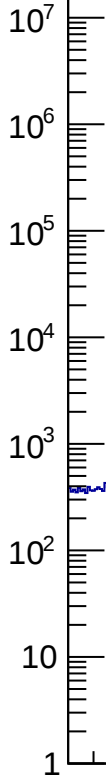
Row 1 Tile 1 Pmt 5 Pixel 40 Slot 13 Fiber 1 Asic 1 Channel 51



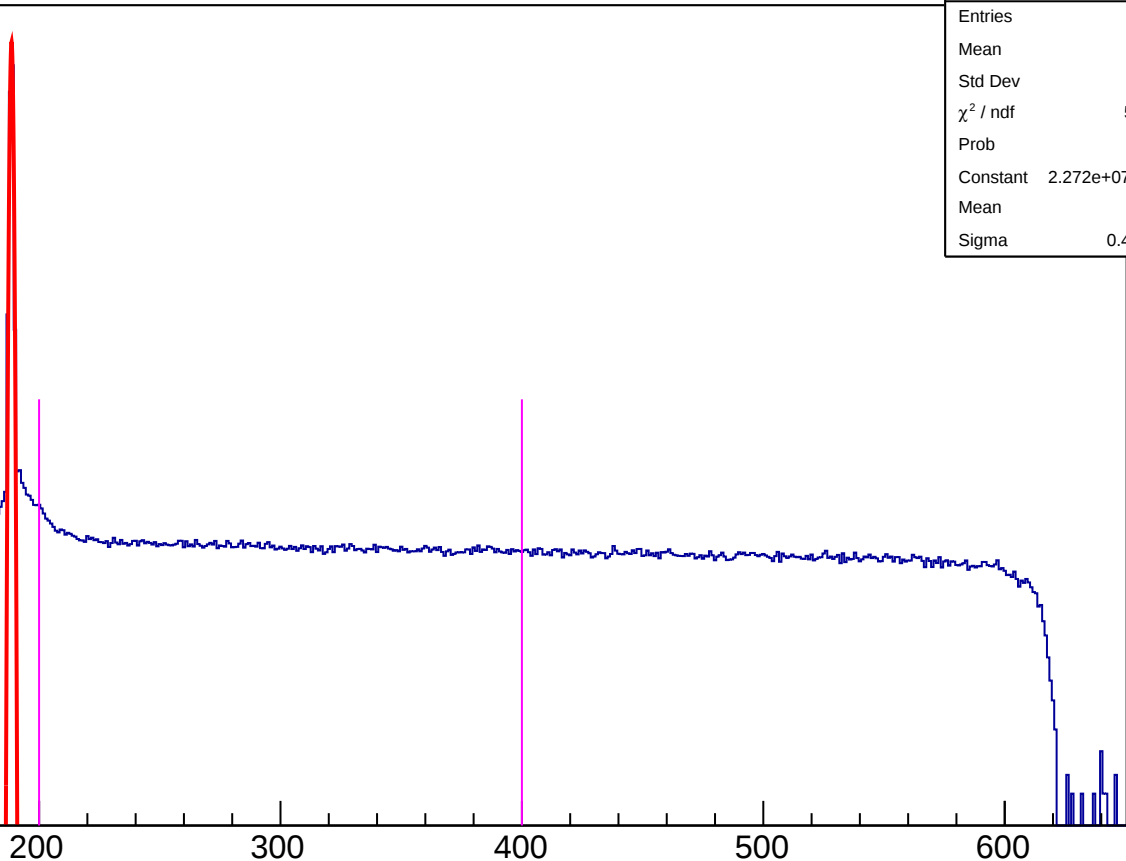
Row 1 Tile 1 Pmt 5 Pixel 41 Slot 13 Fiber 1 Asic 1 Channel 11



Count Rate [cps]

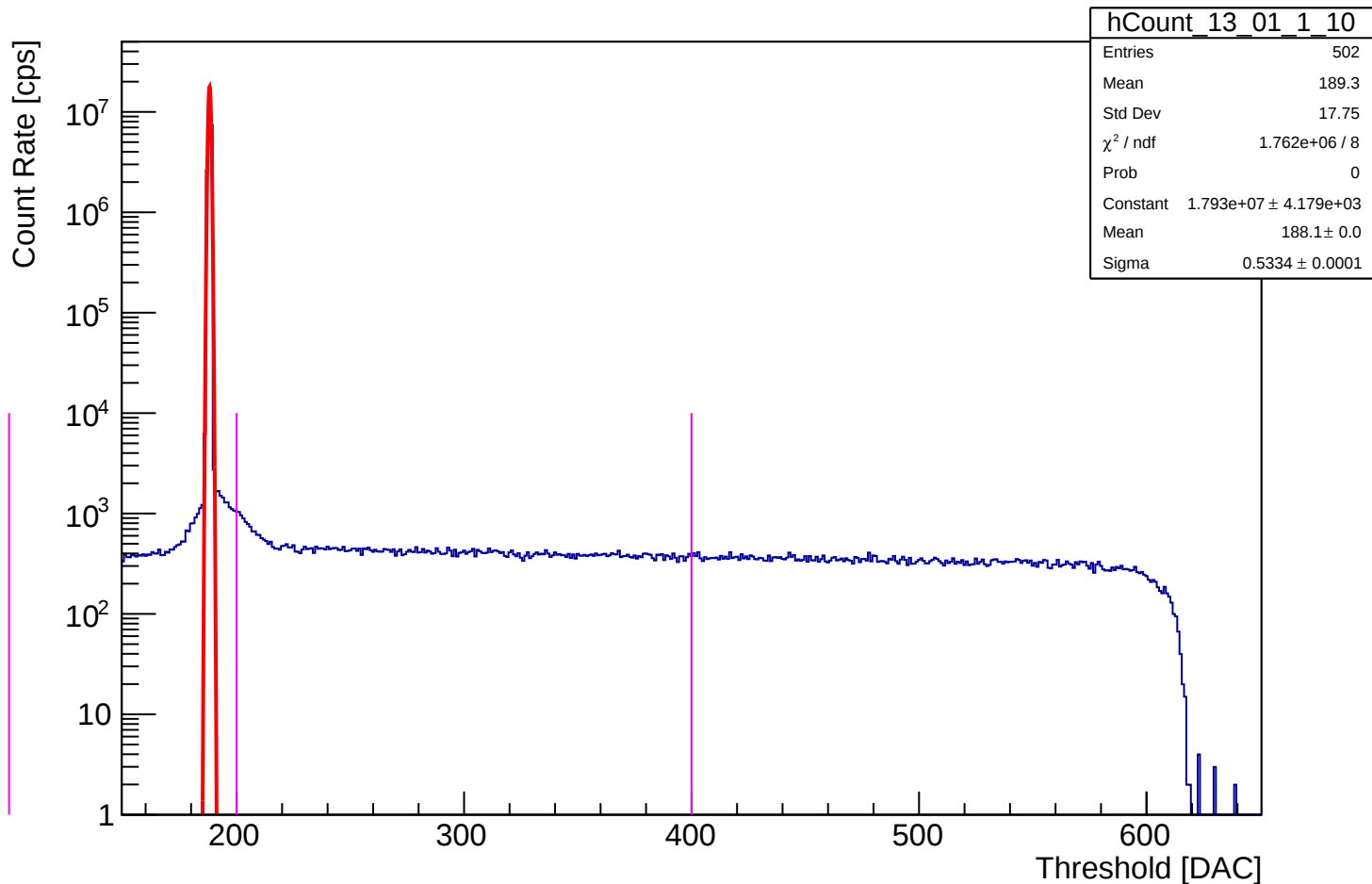


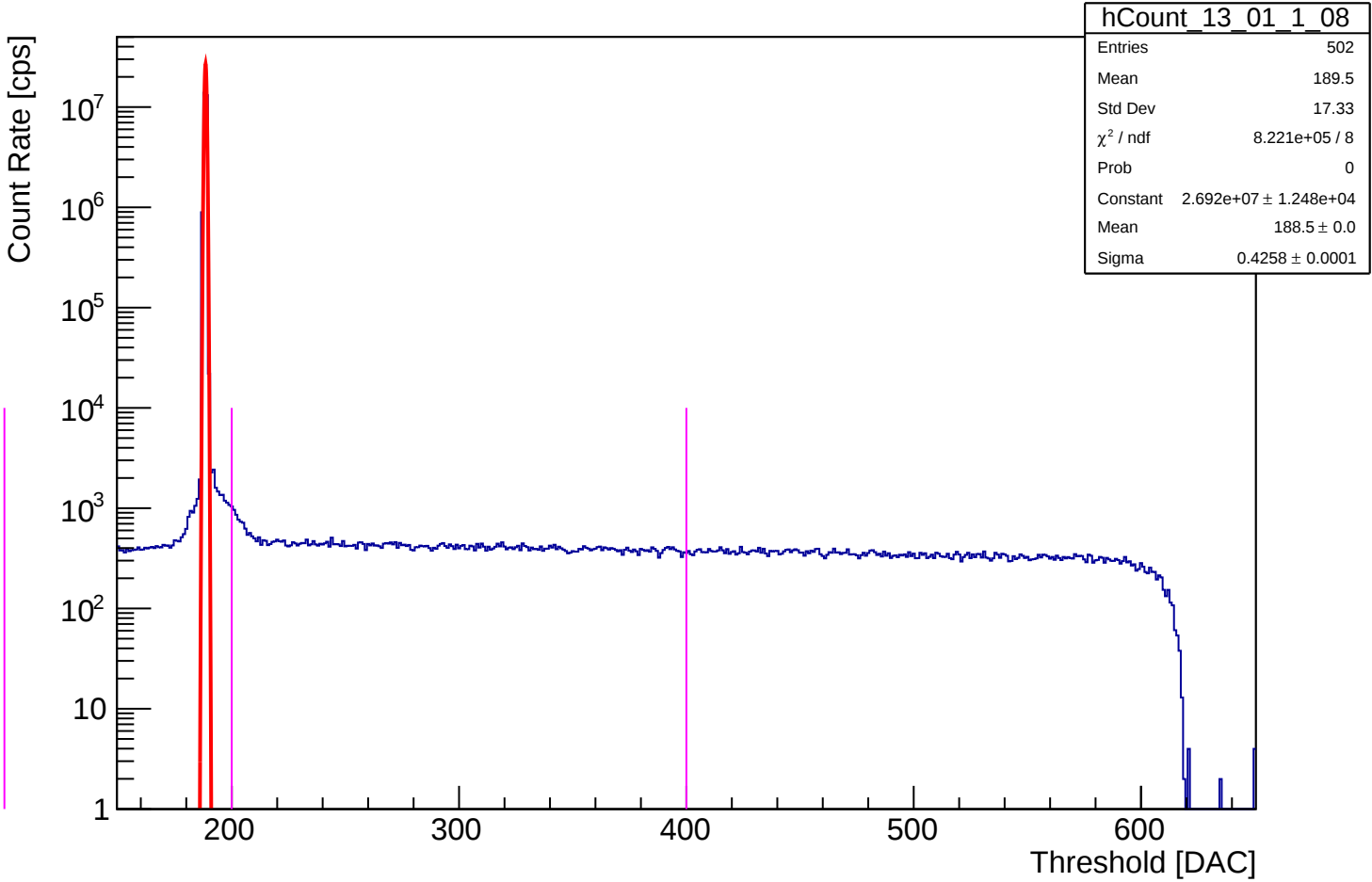
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Entries	502
Mean	190.1
Std Dev	19.55
χ^2 / ndf	5.733e+04 / 8
Prob	0
Constant	2.272e+07 $\pm$ 1.249e+04
Mean	188.6 $\pm$ 0.0
Sigma	0.4035 $\pm$ 0.0001



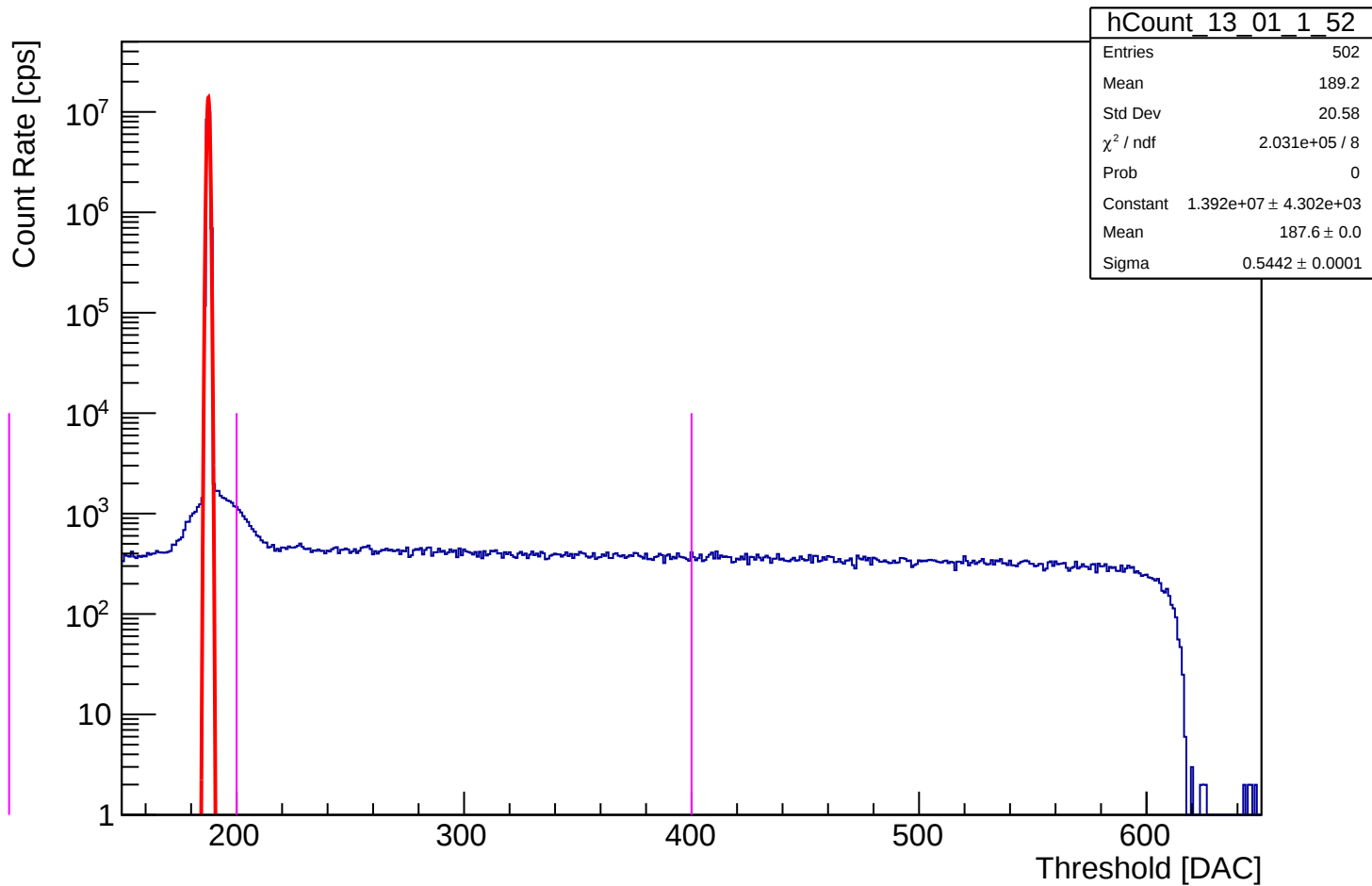
Threshold [DAC]

Row 1 Tile 1 Pmt 5 Pixel 43 Slot 13 Fiber 1 Asic 1 Channel 10

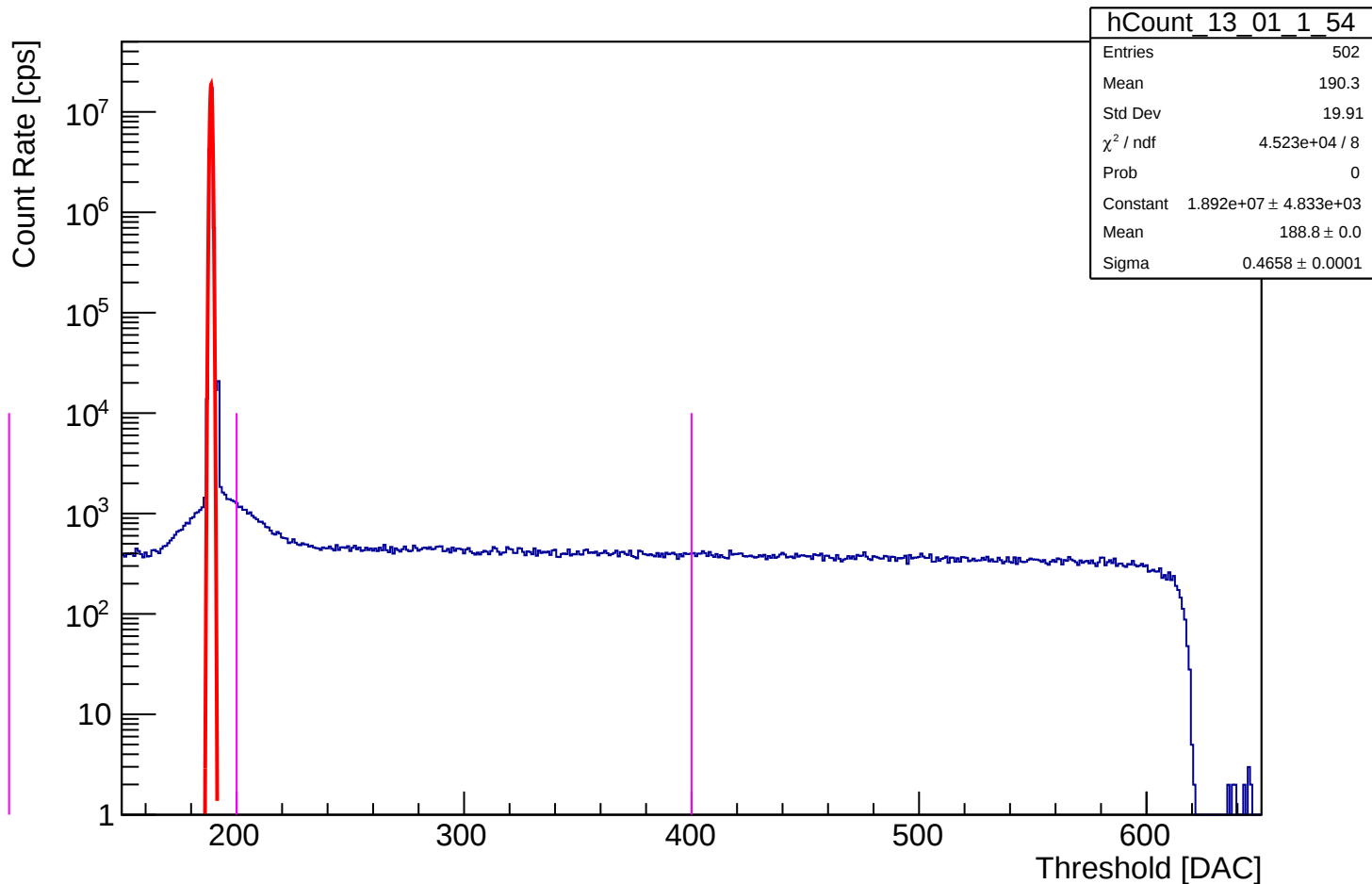




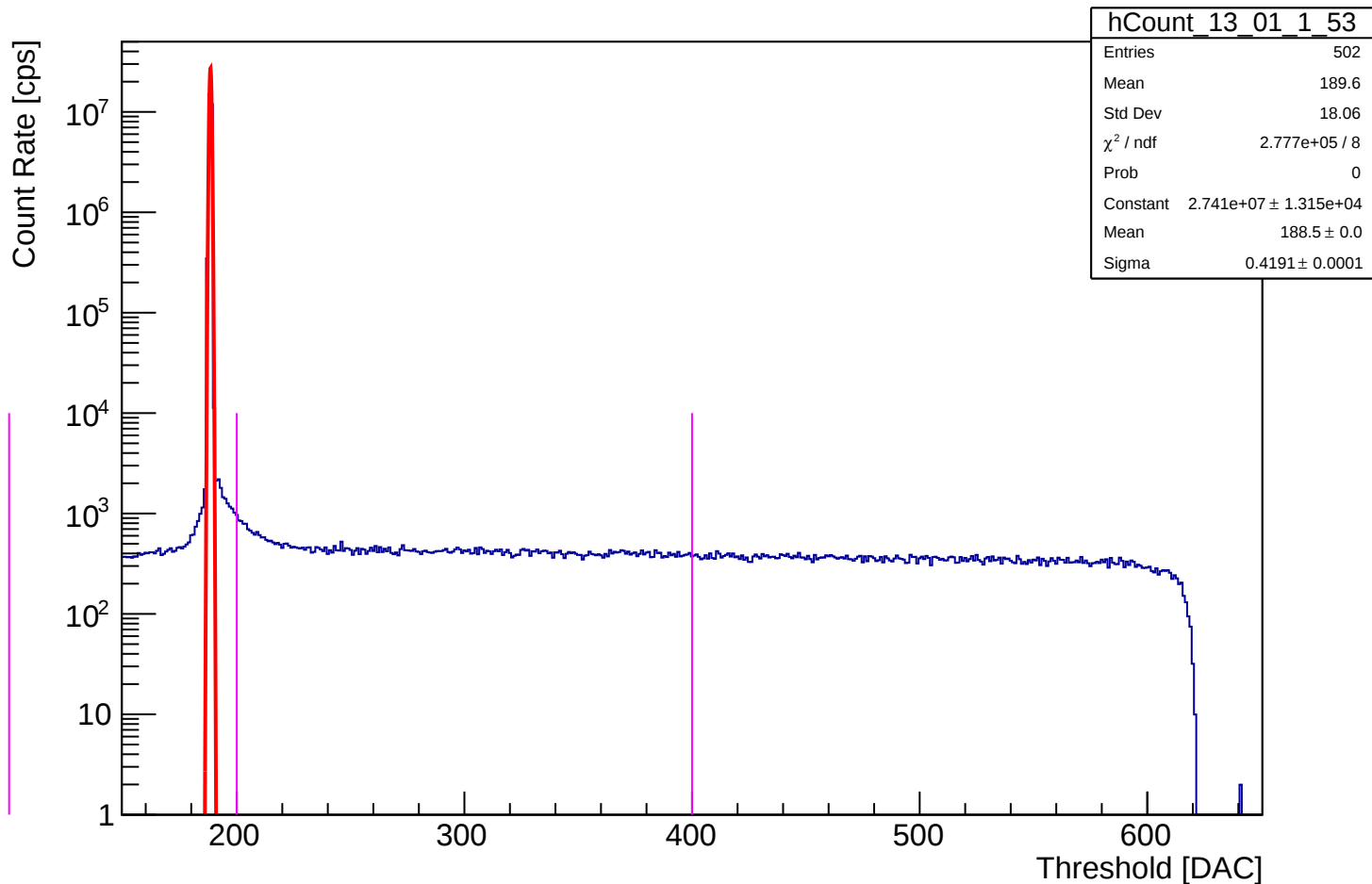
Row 1 Tile 1 Pmt 5 Pixel 45 Slot 13 Fiber 1 Asic 1 Channel 52



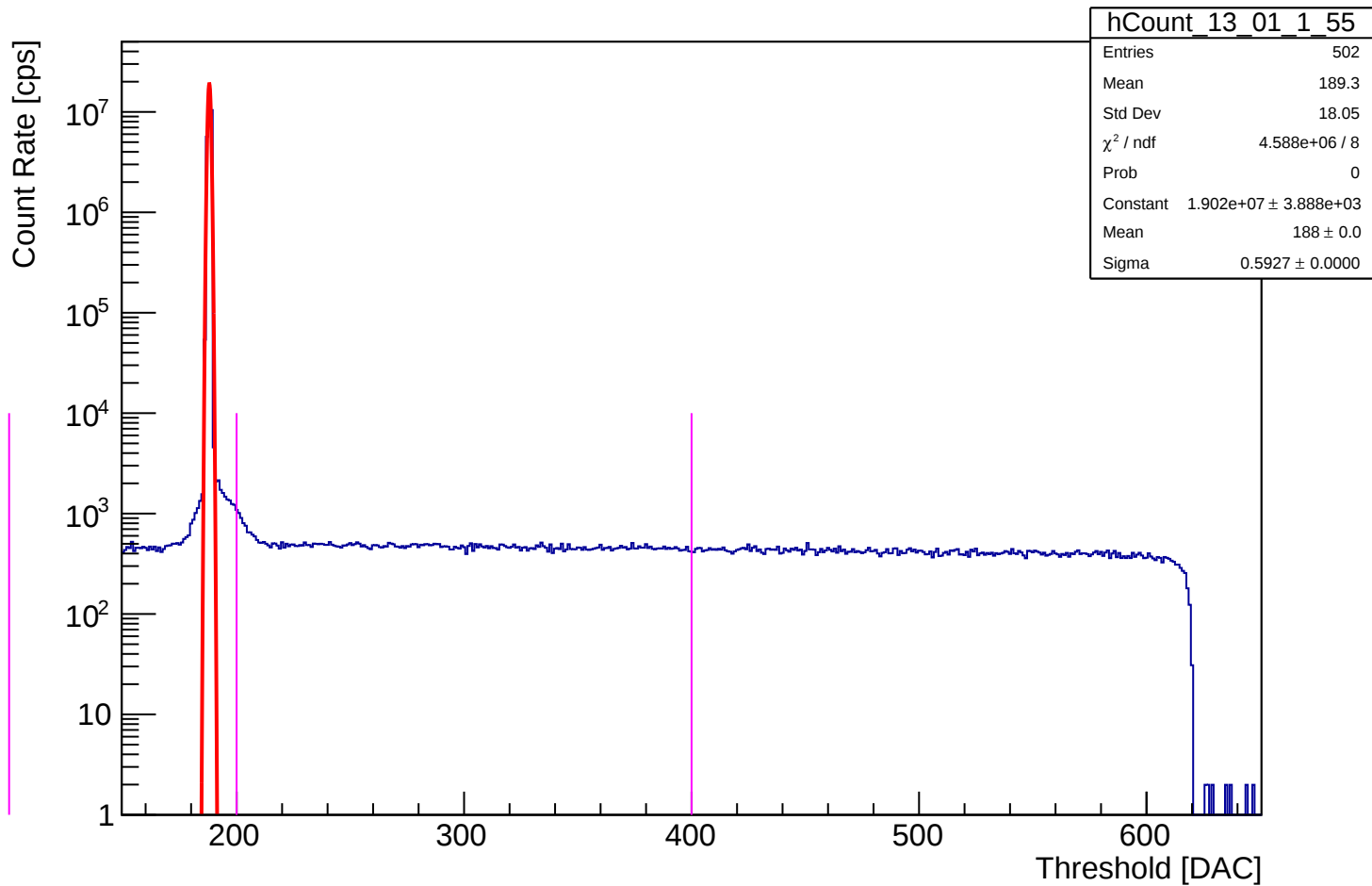
Row 1 Tile 1 Pmt 5 Pixel 46 Slot 13 Fiber 1 Asic 1 Channel 54

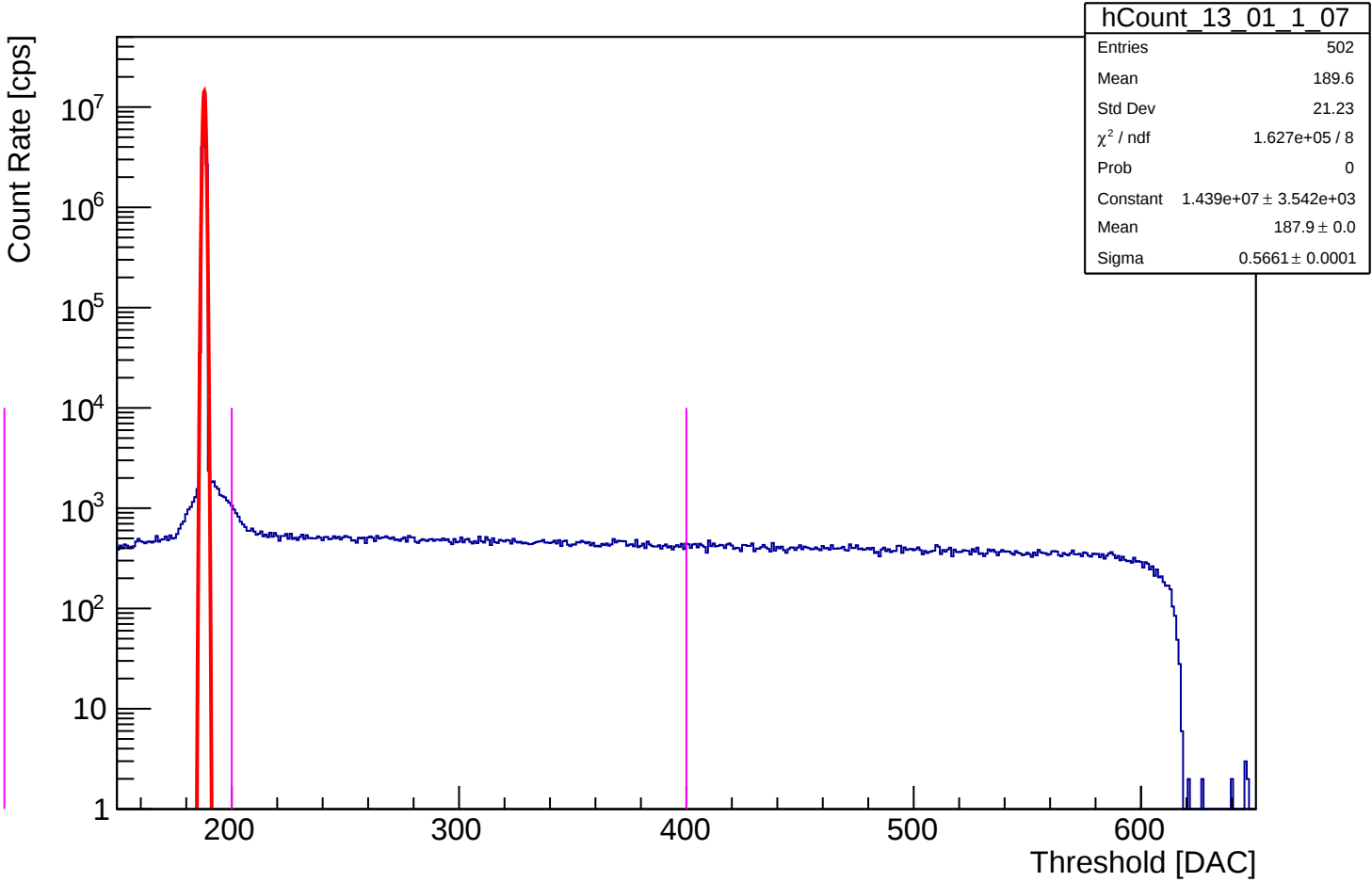


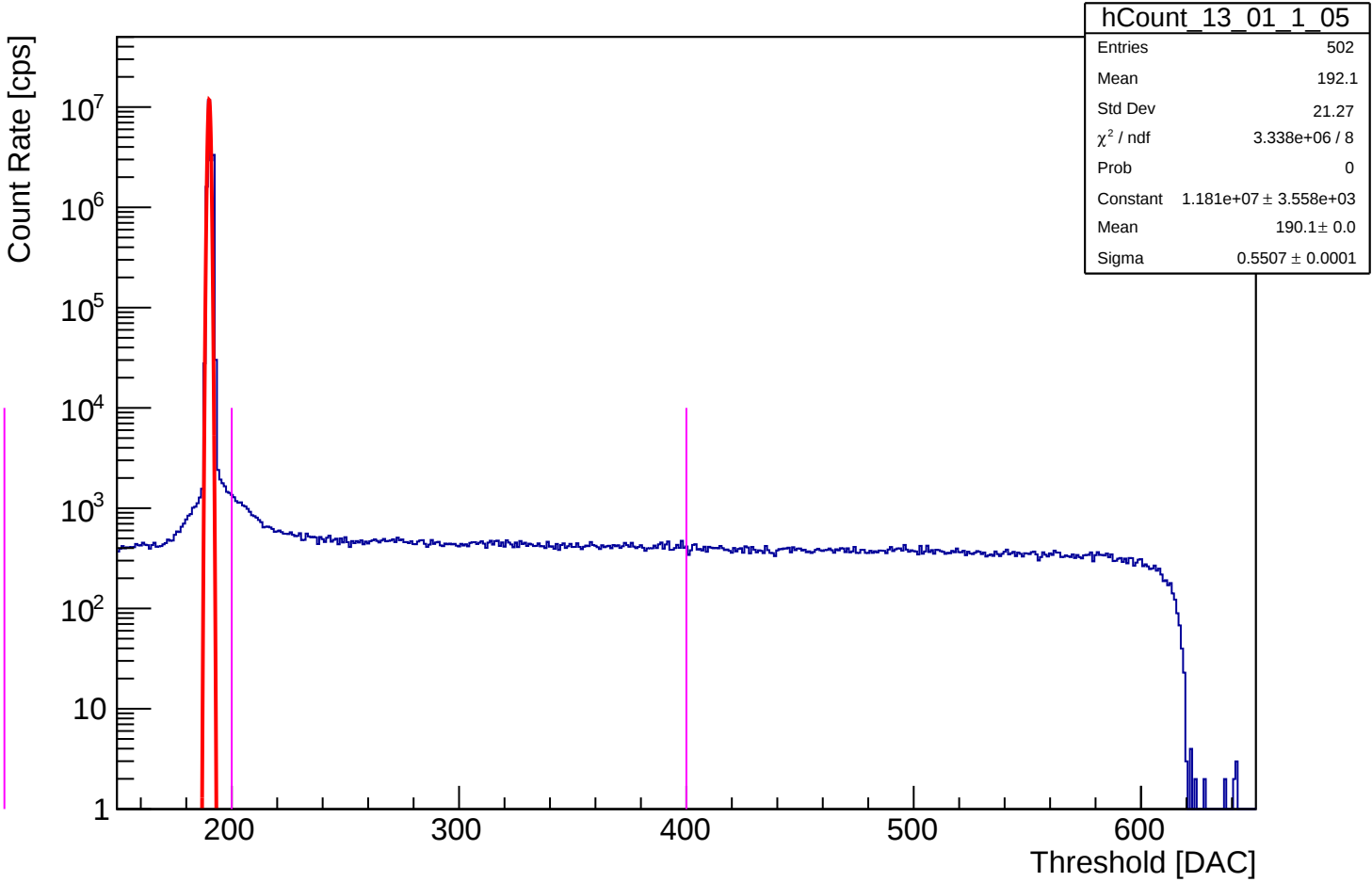
Row 1 Tile 1 Pmt 5 Pixel 47 Slot 13 Fiber 1 Asic 1 Channel 53

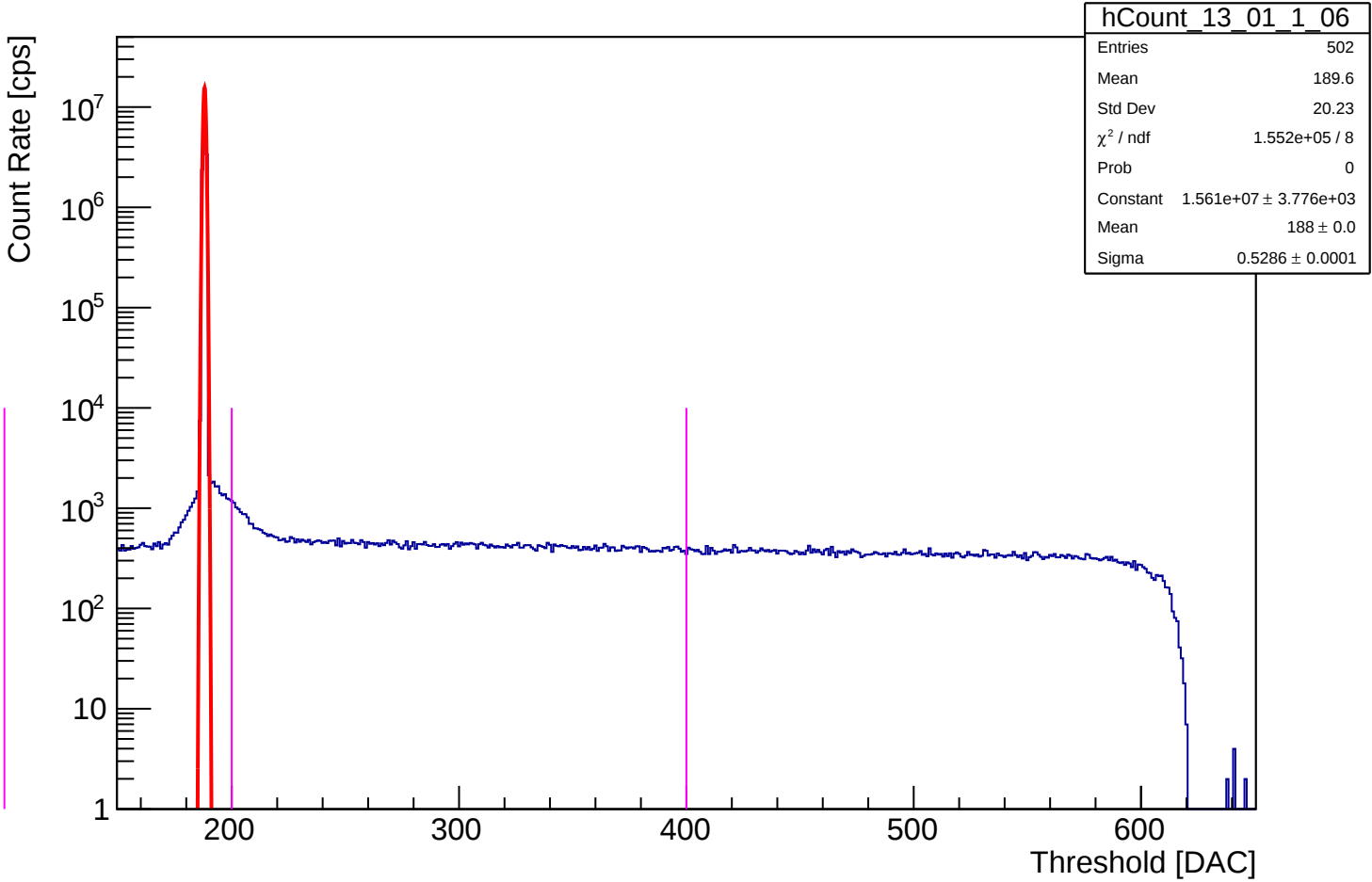


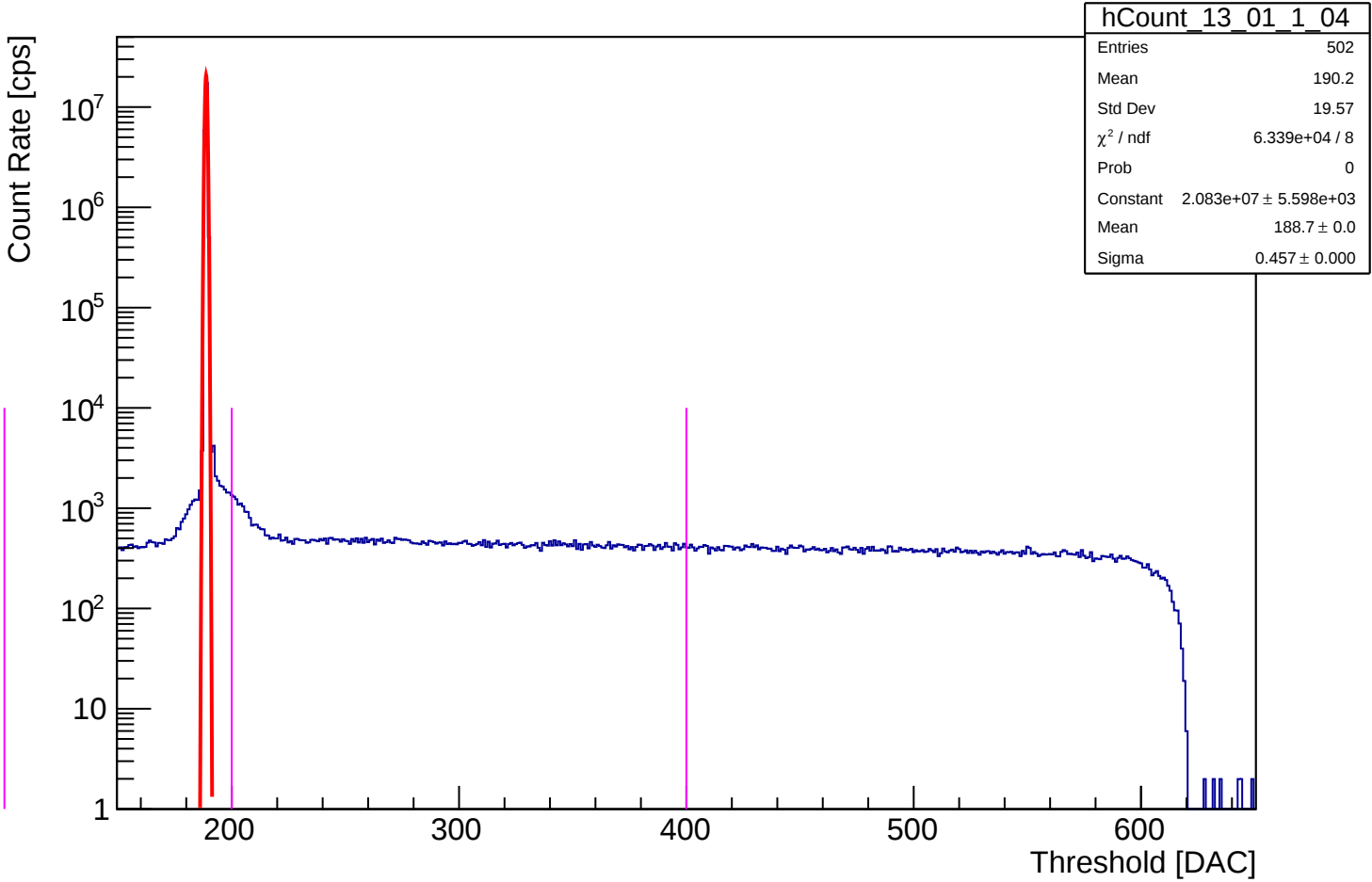
Row 1 Tile 1 Pmt 5 Pixel 48 Slot 13 Fiber 1 Asic 1 Channel 55



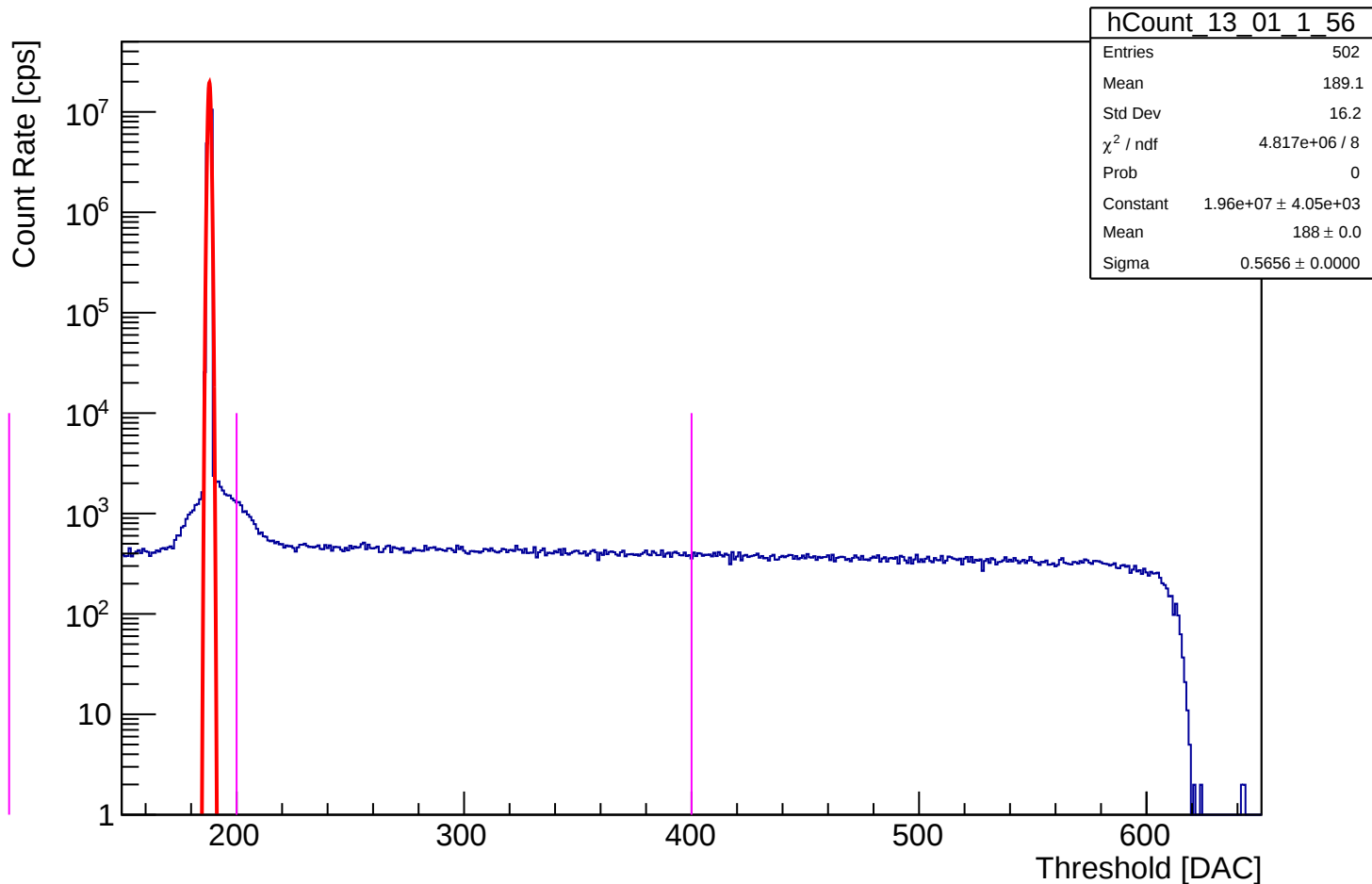




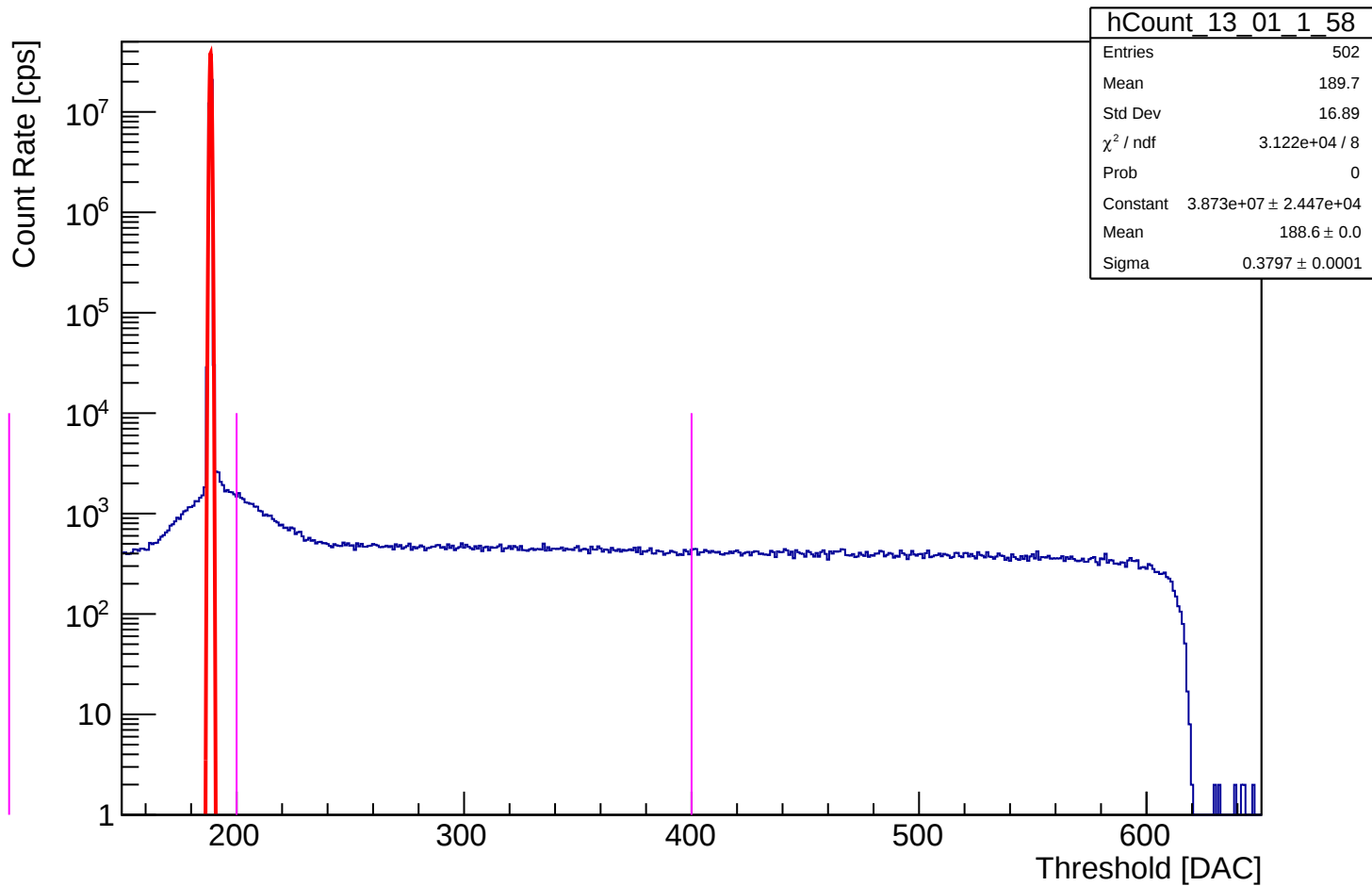




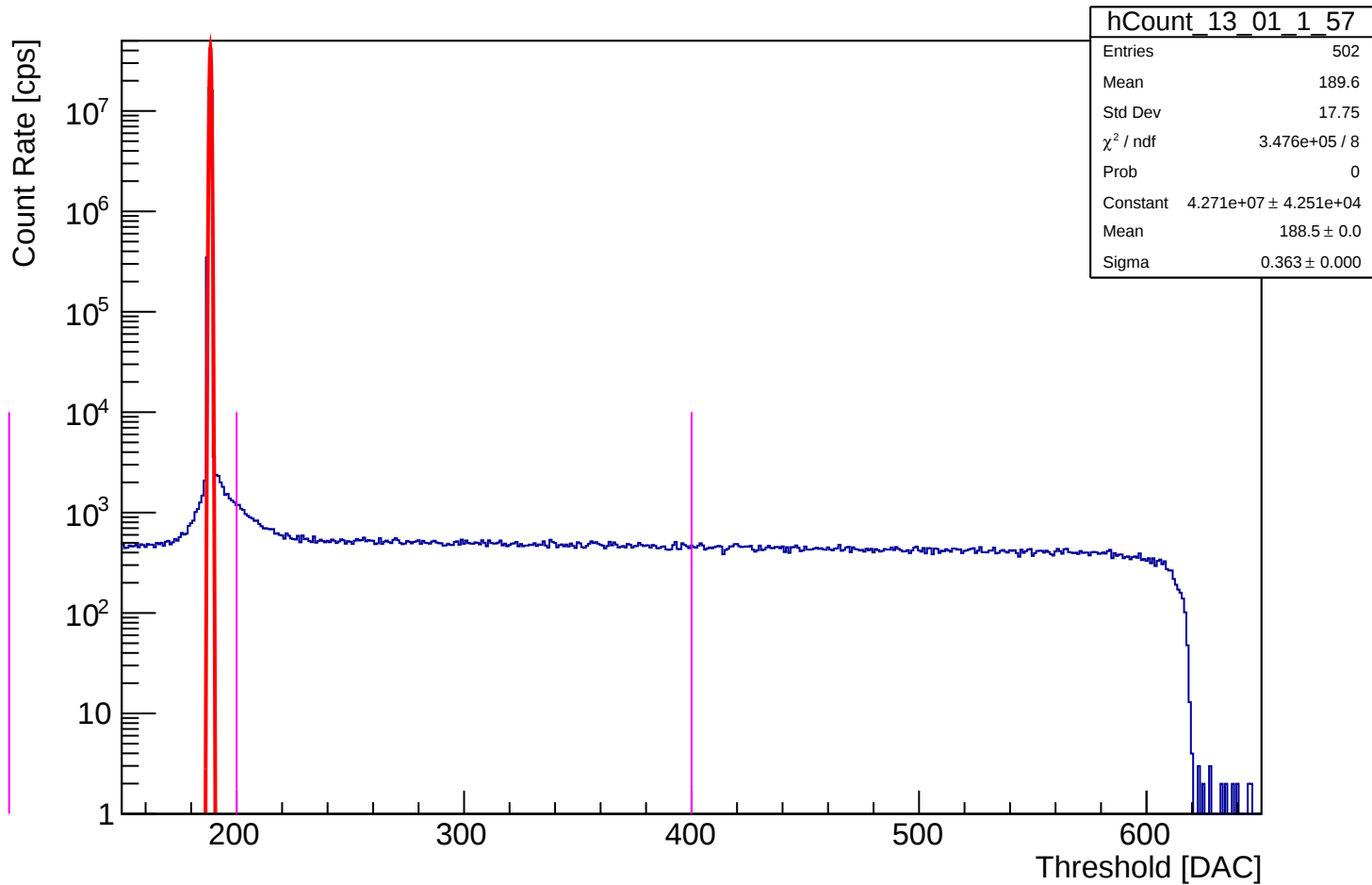
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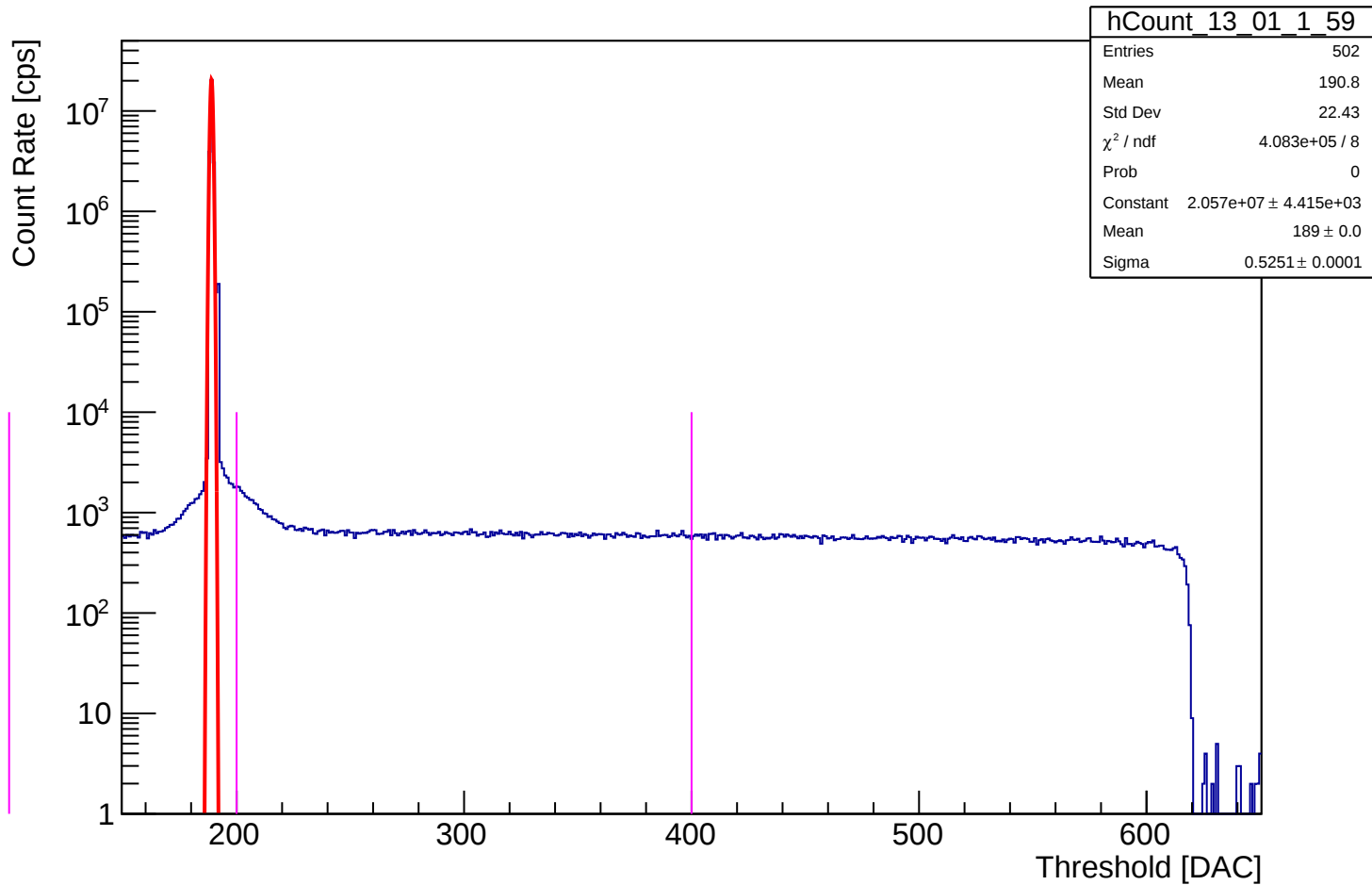
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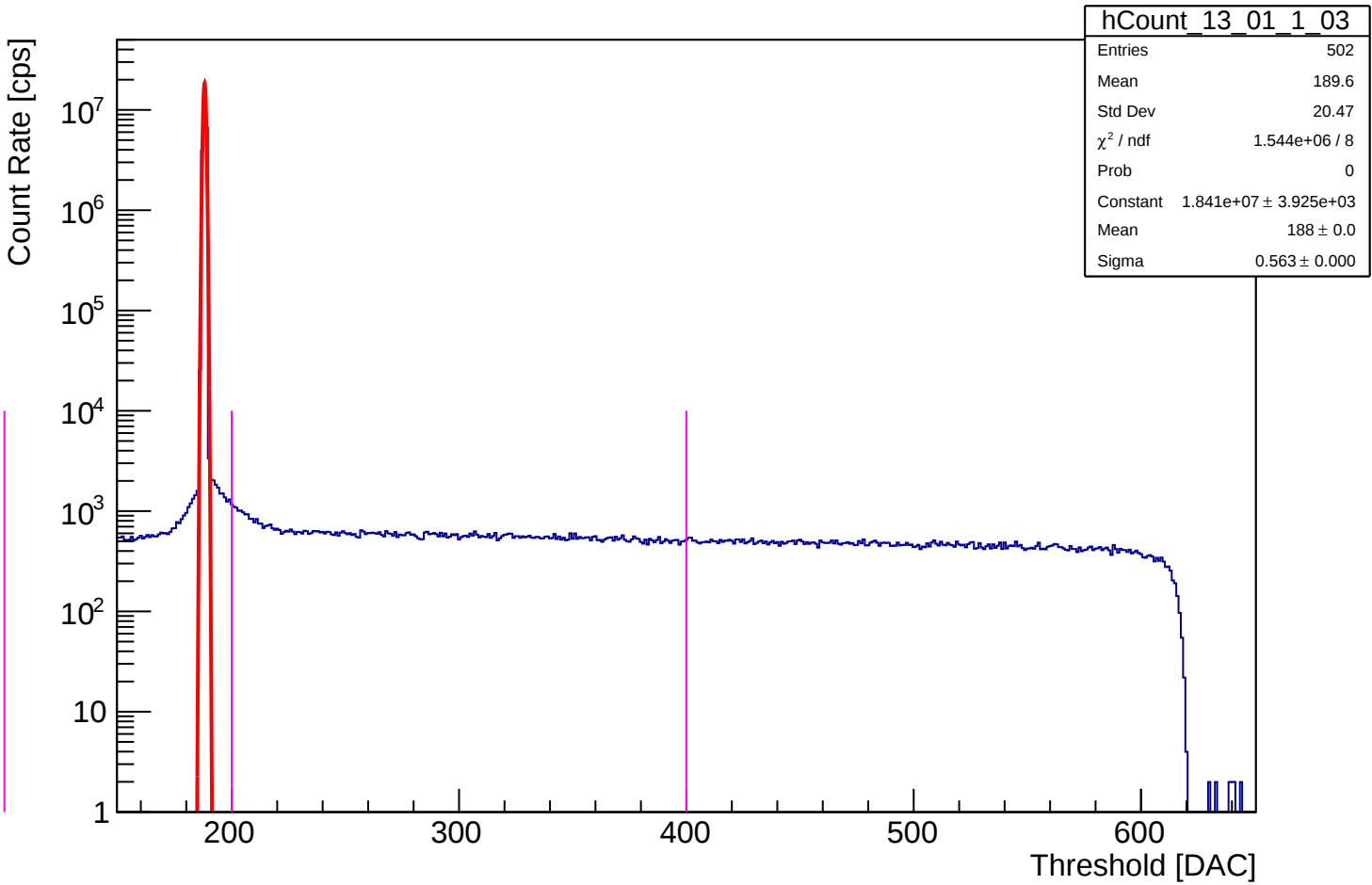


Row 1 Tile 1 Pmt 5 Pixel 55 Slot 13 Fiber 1 Asic 1 Channel 57

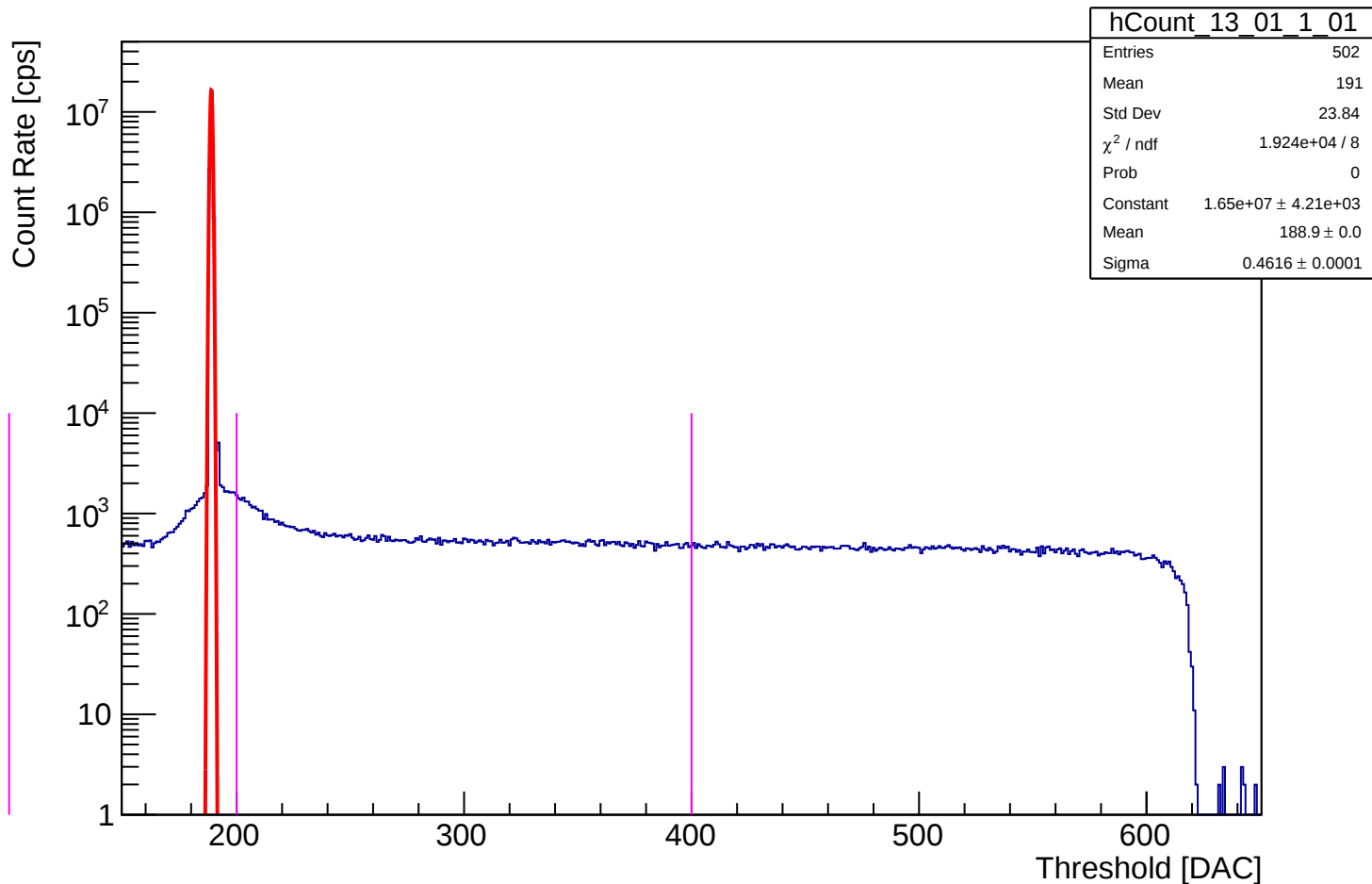


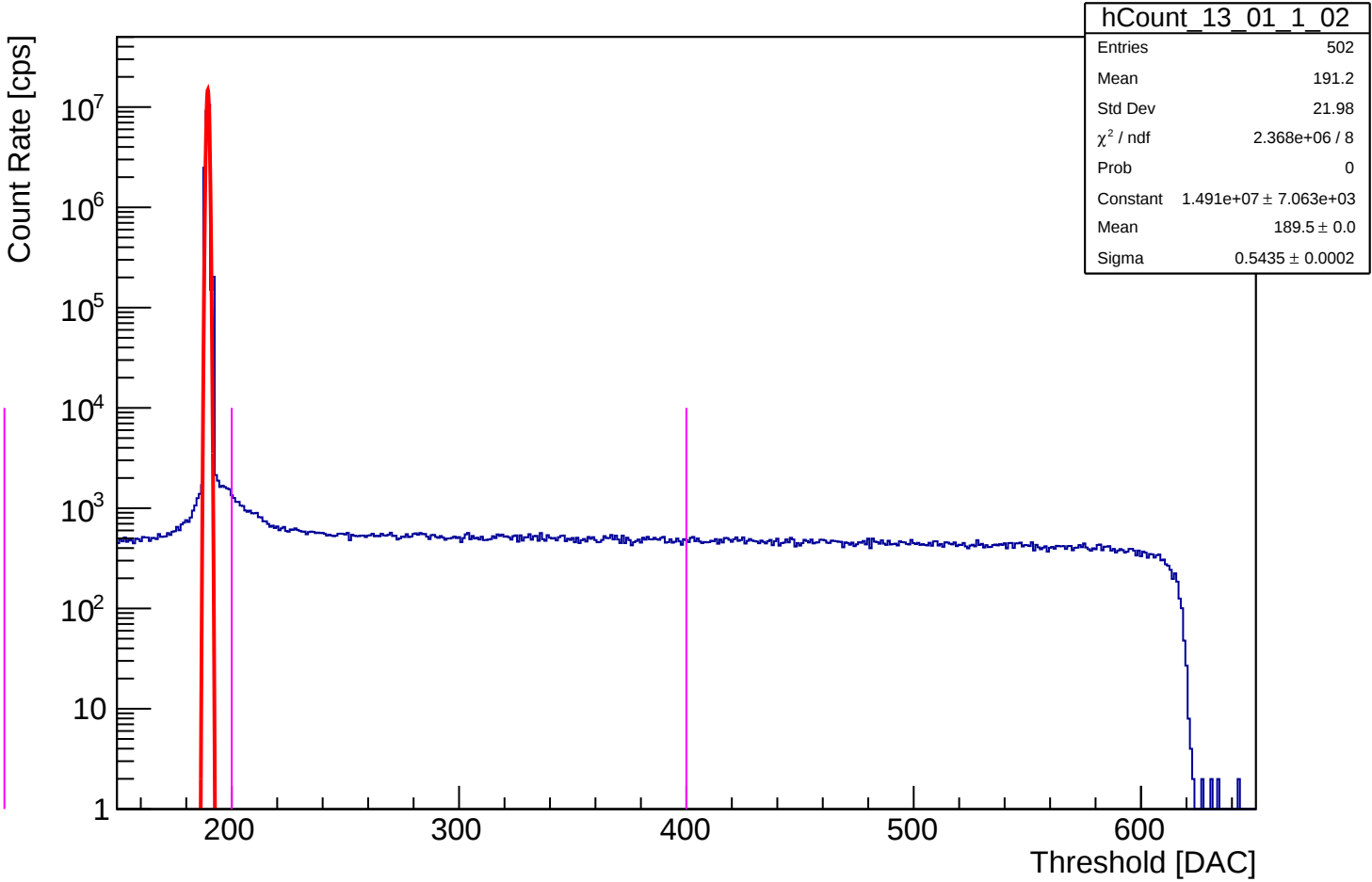
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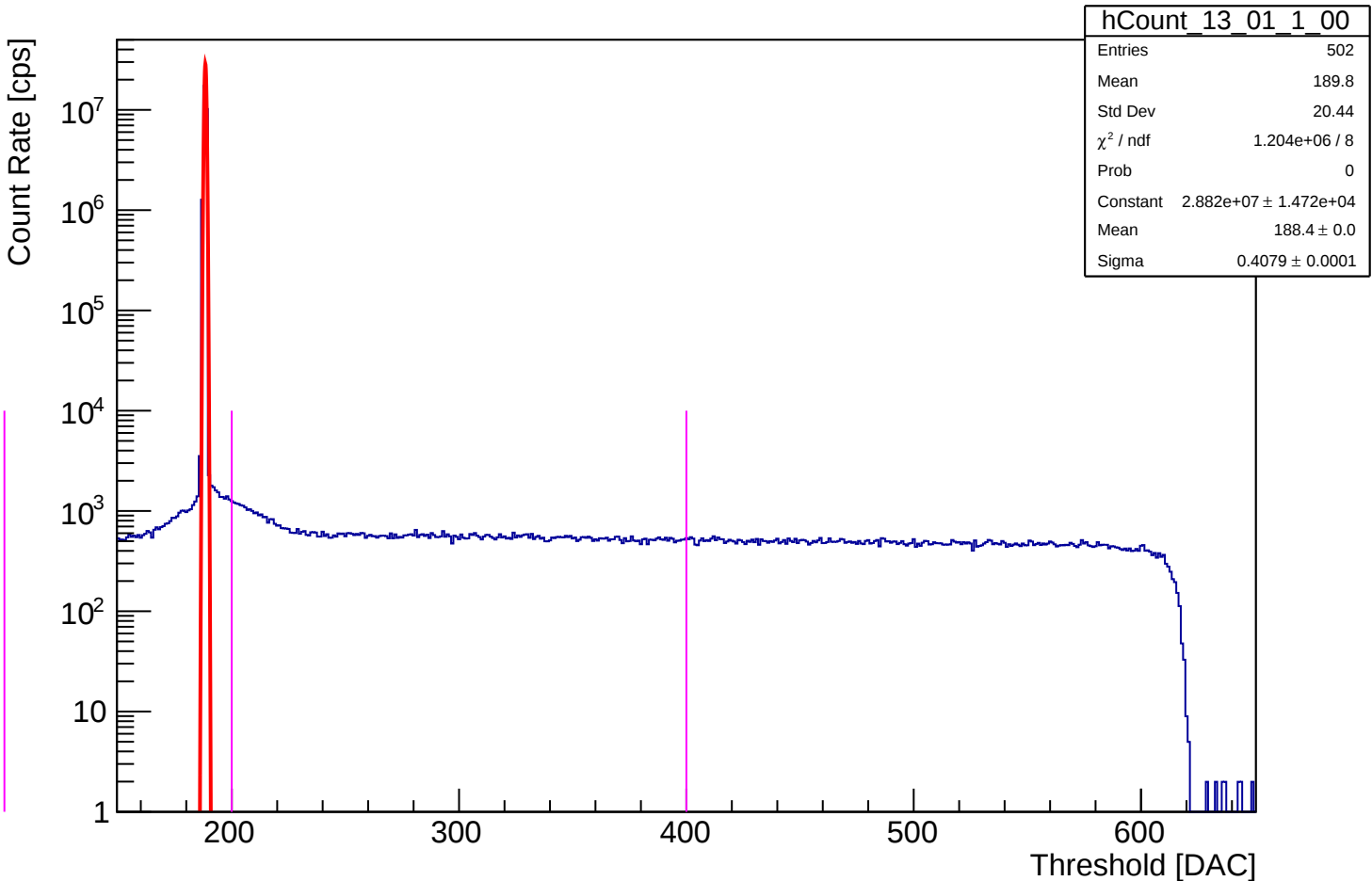




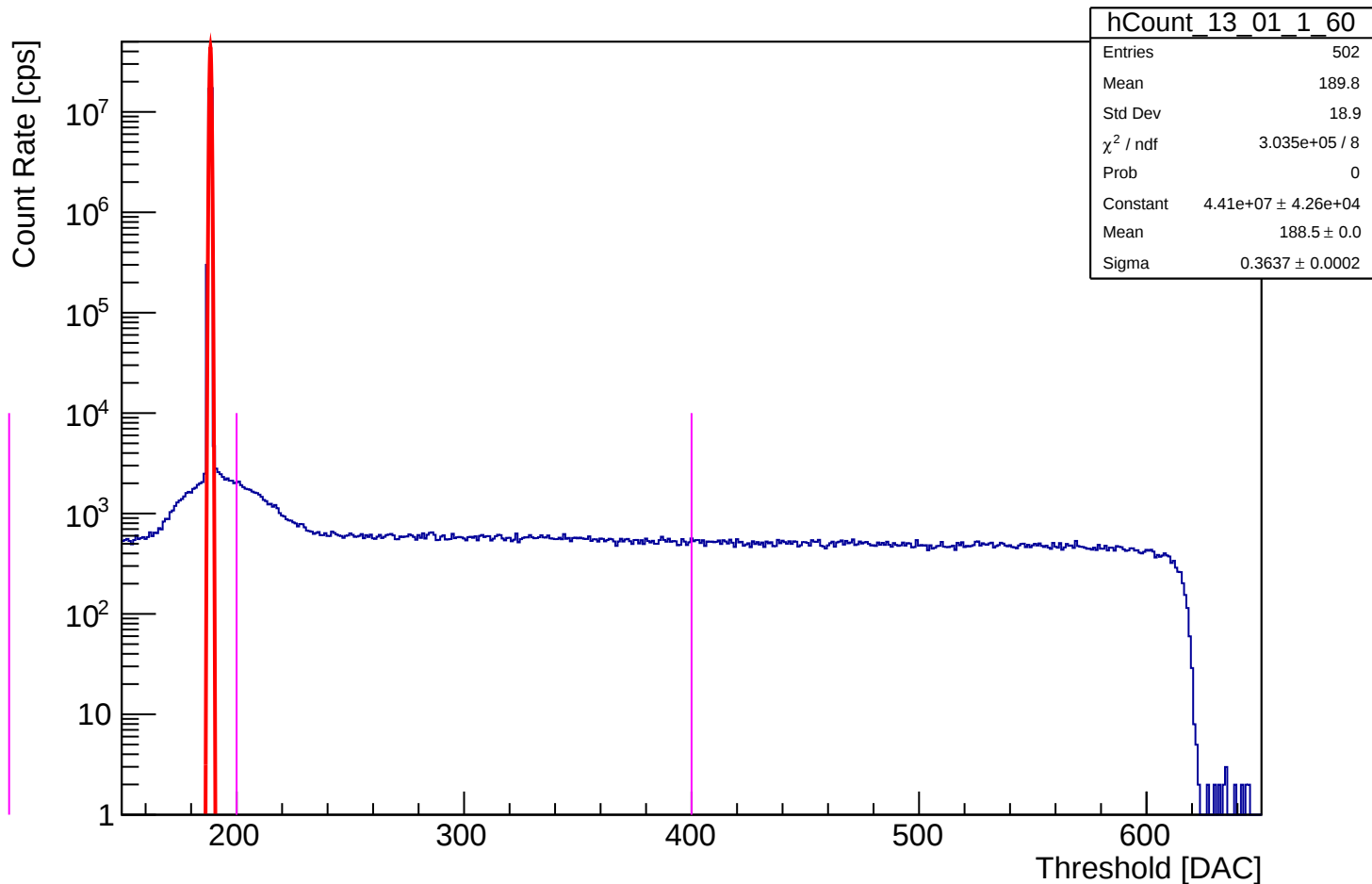
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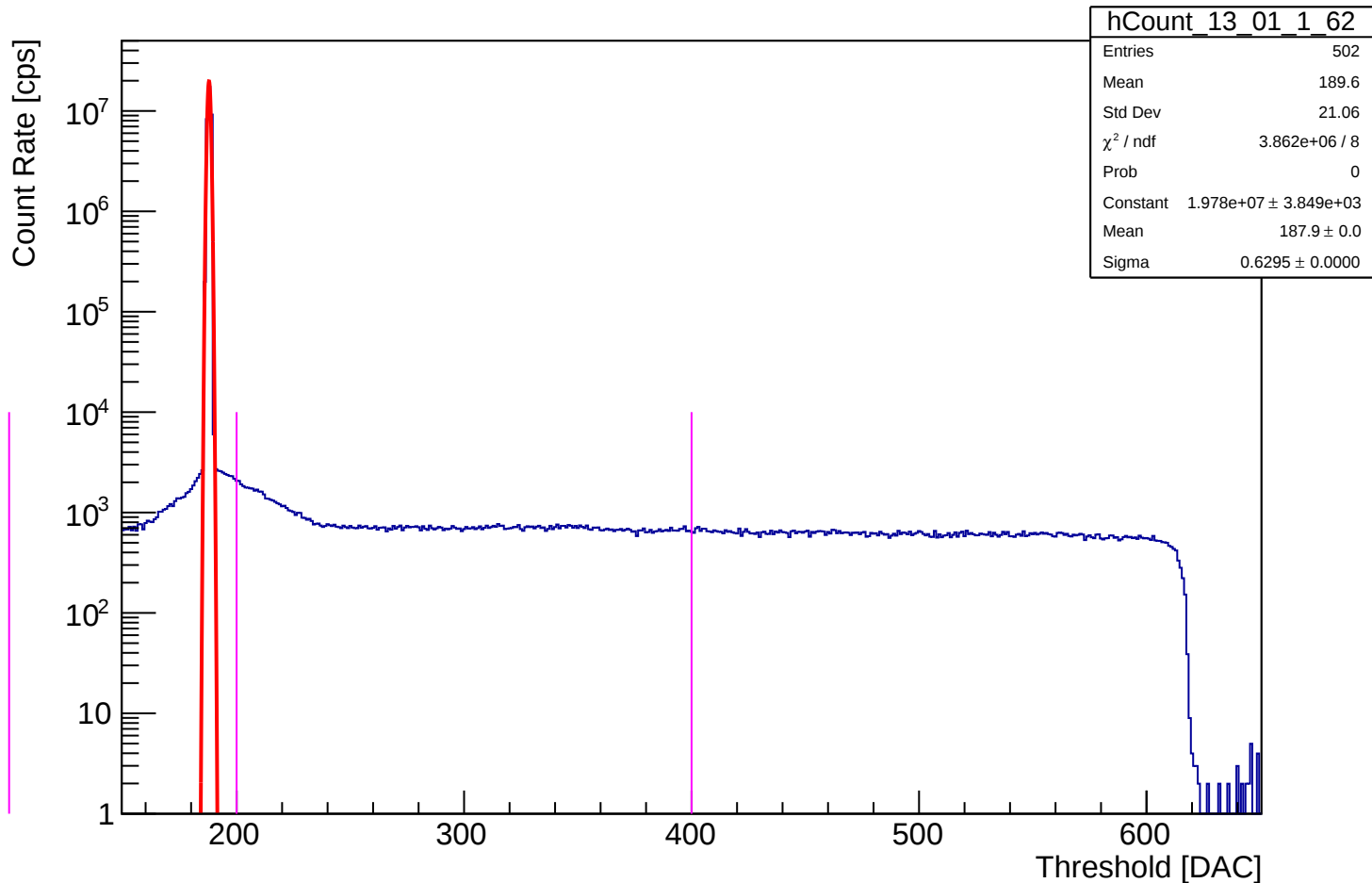




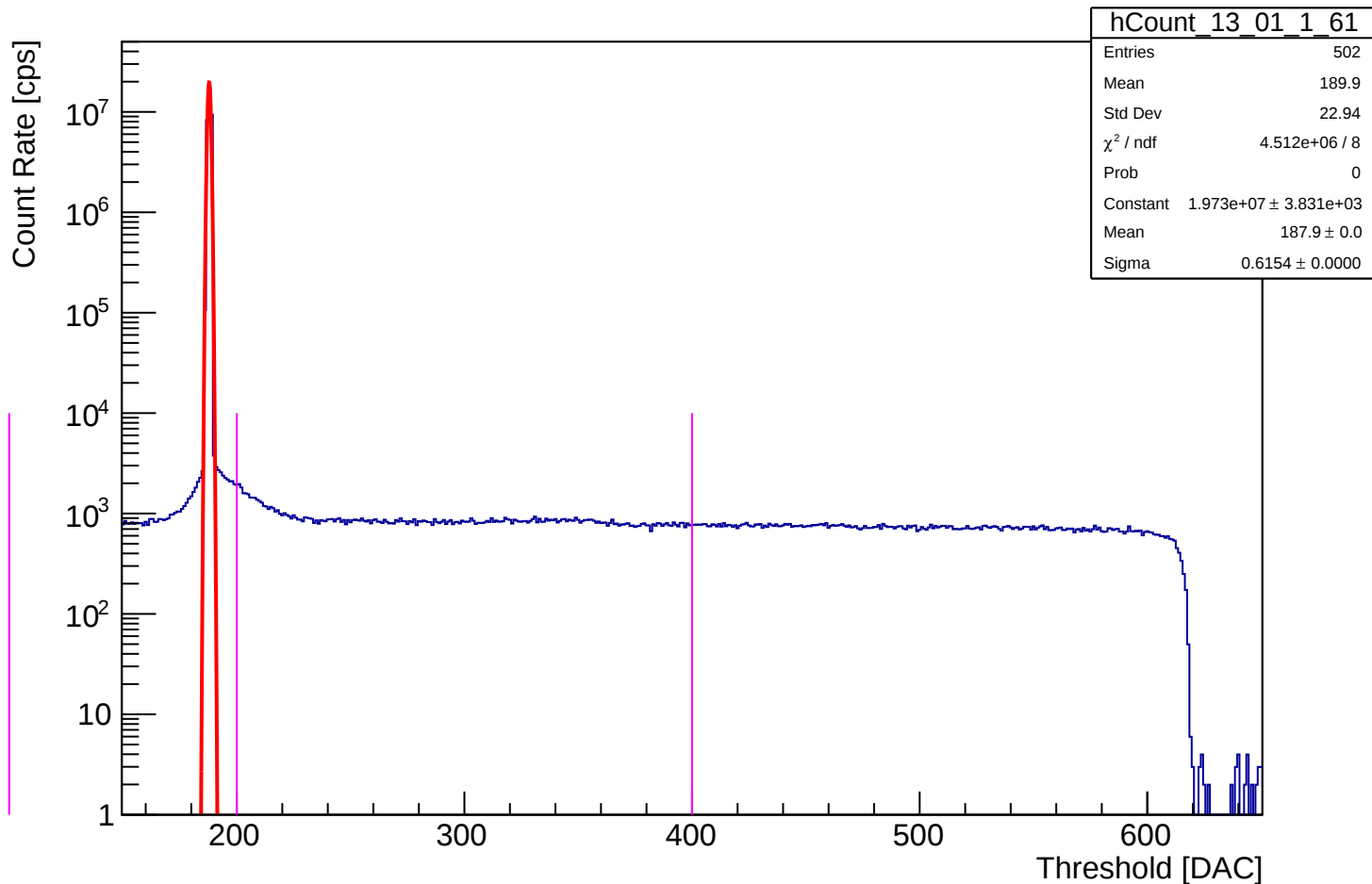
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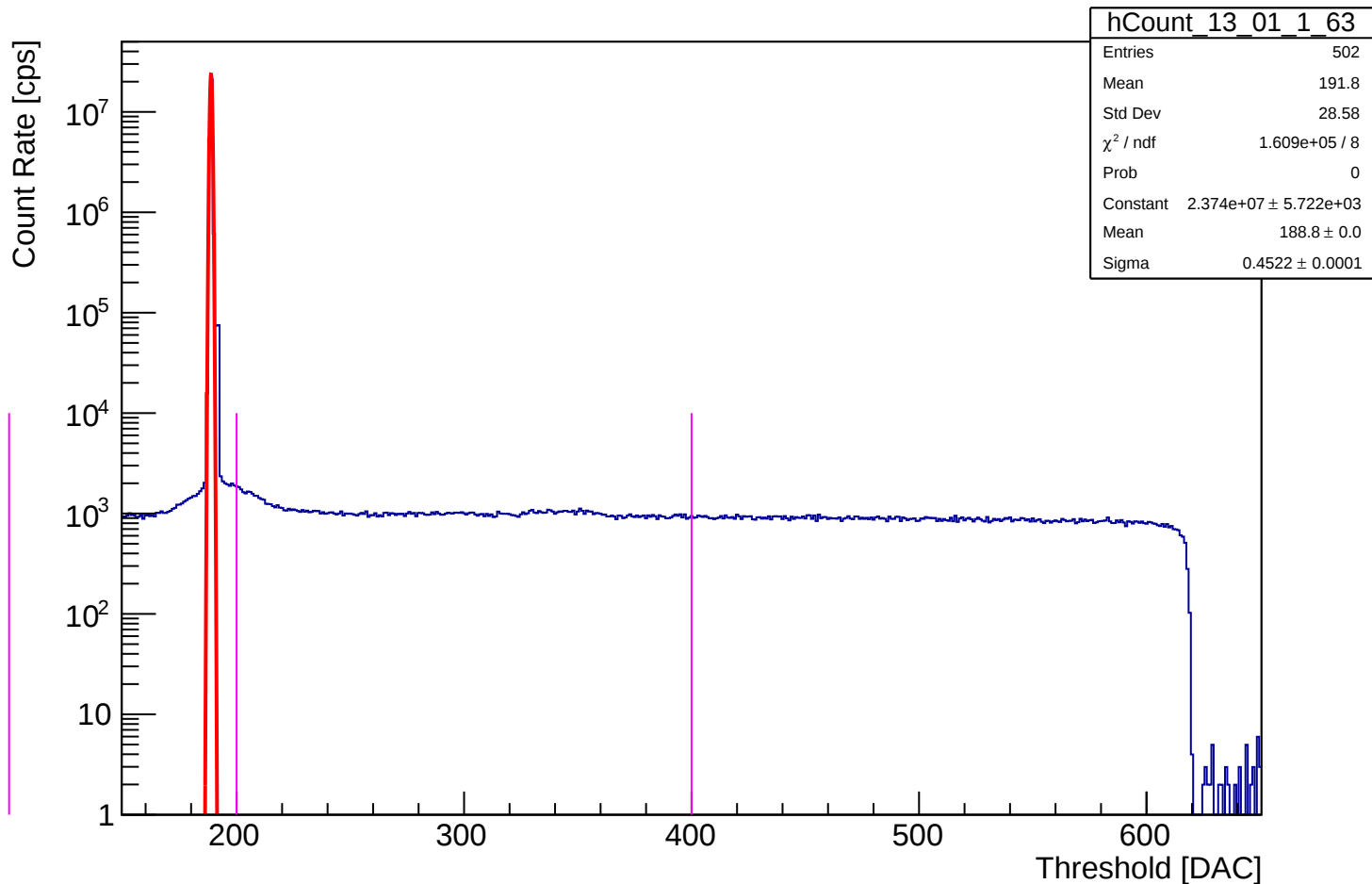
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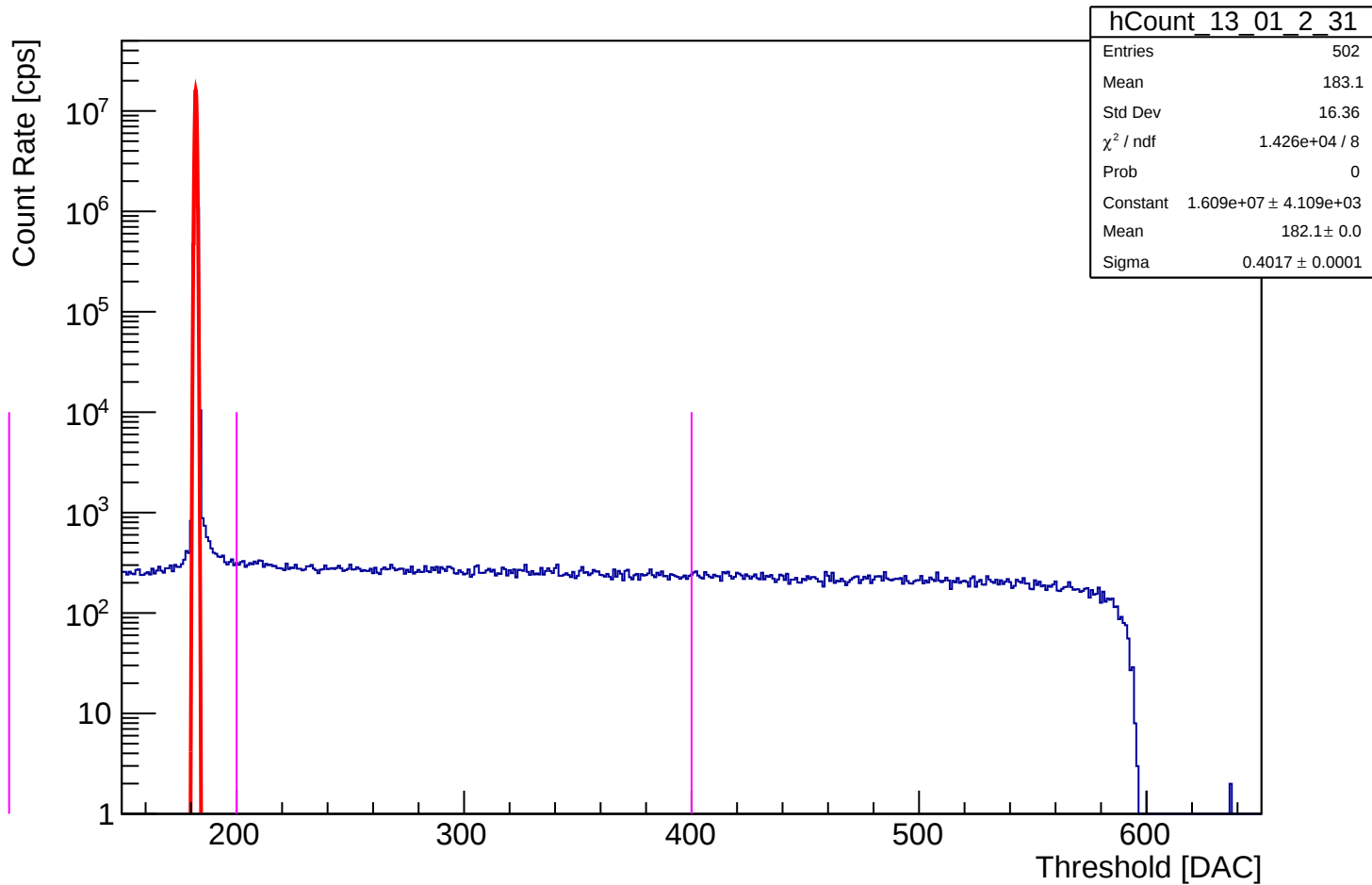
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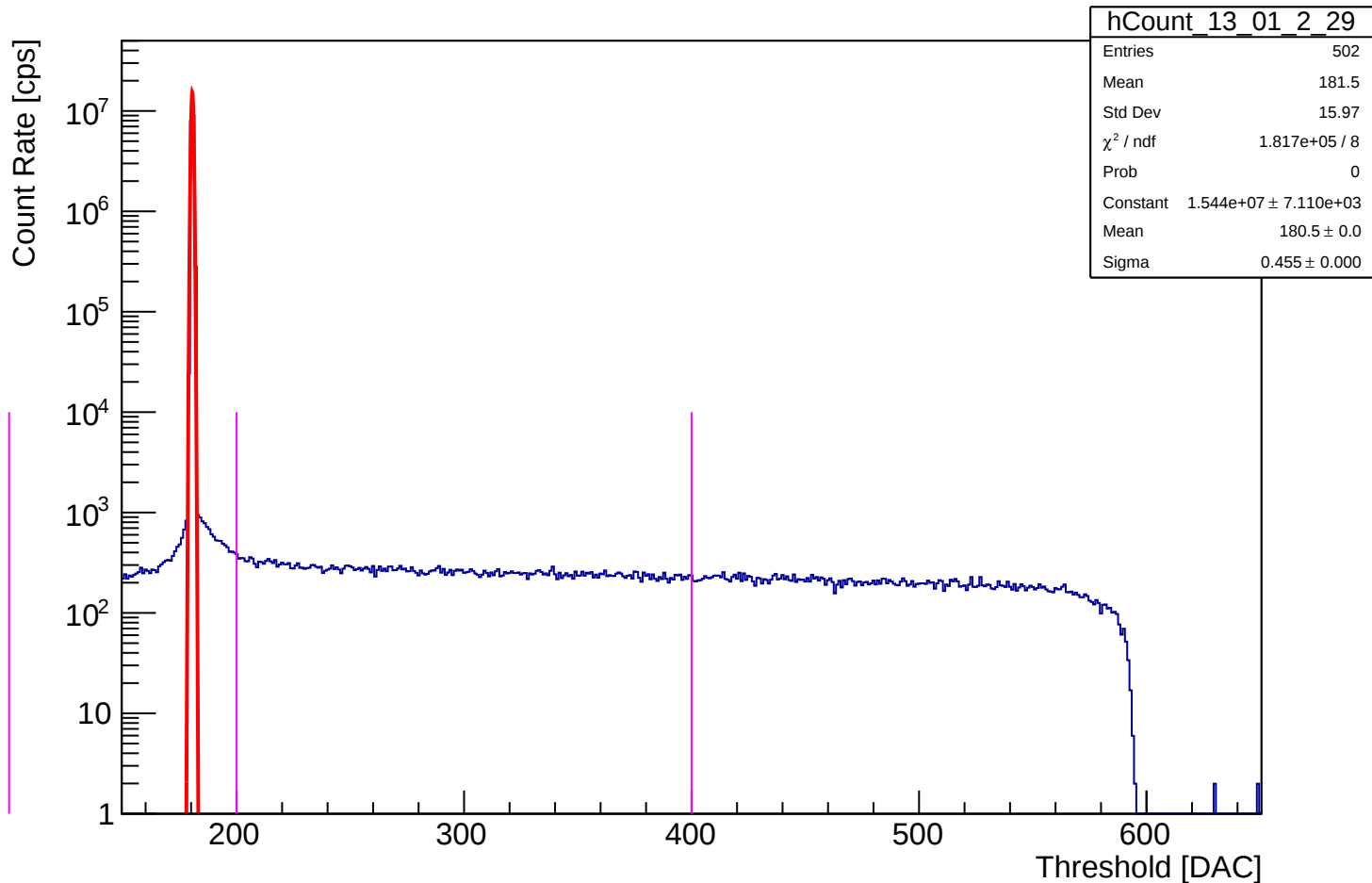
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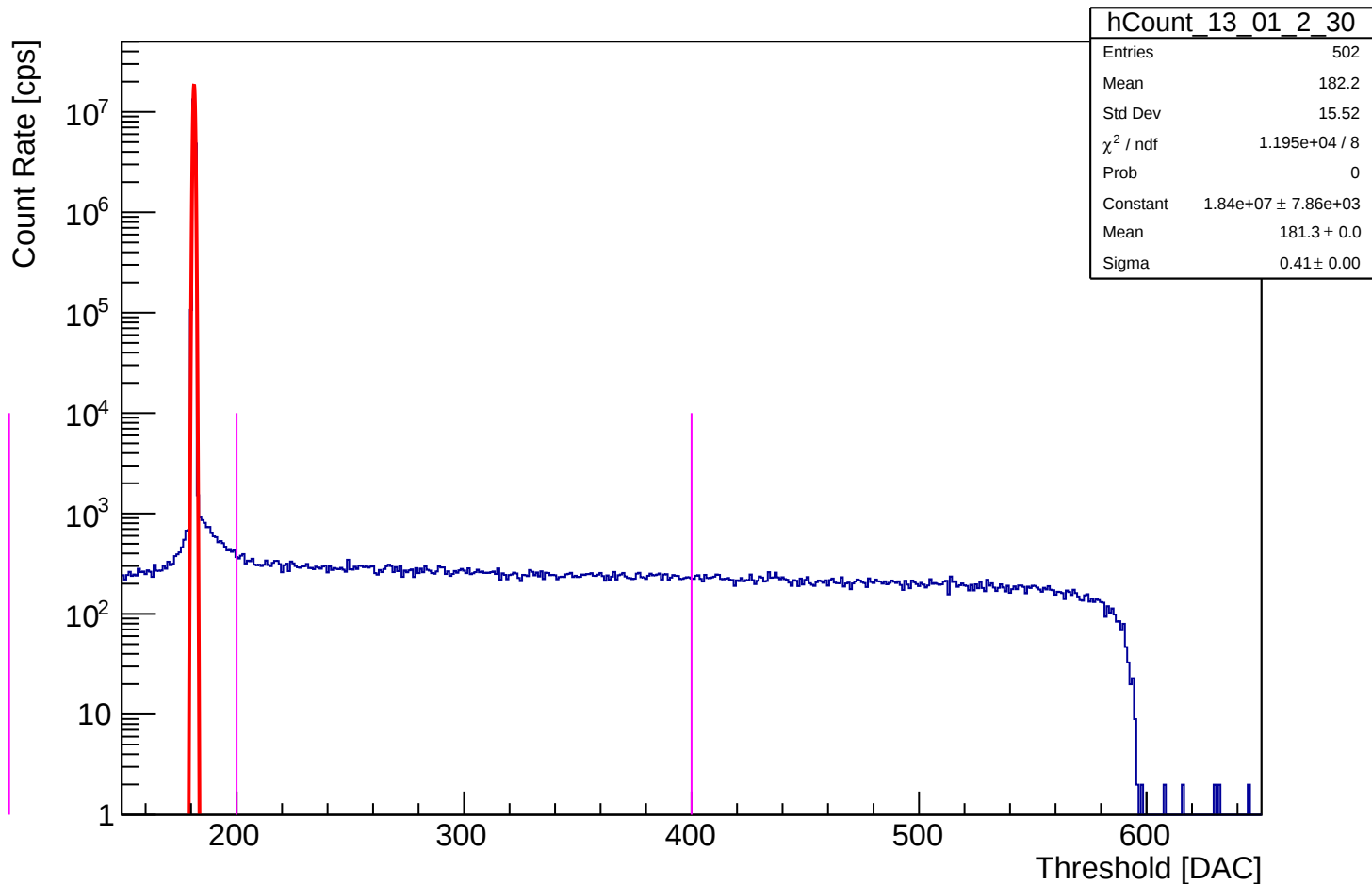
Row 1 Tile 1 Pmt 6 Pixel 1 Slot 13 Fiber 1 Asic 2 Channel 31



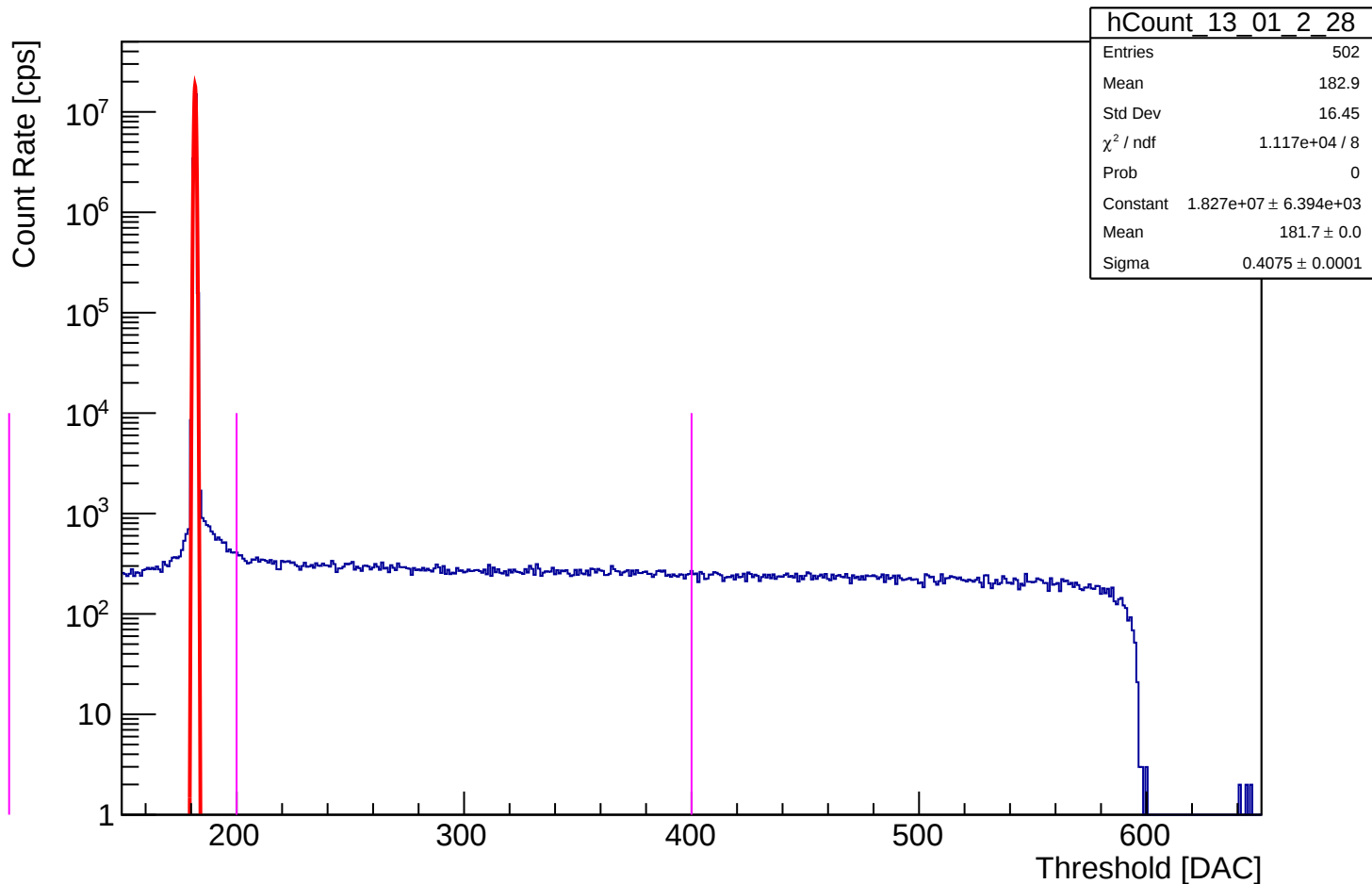
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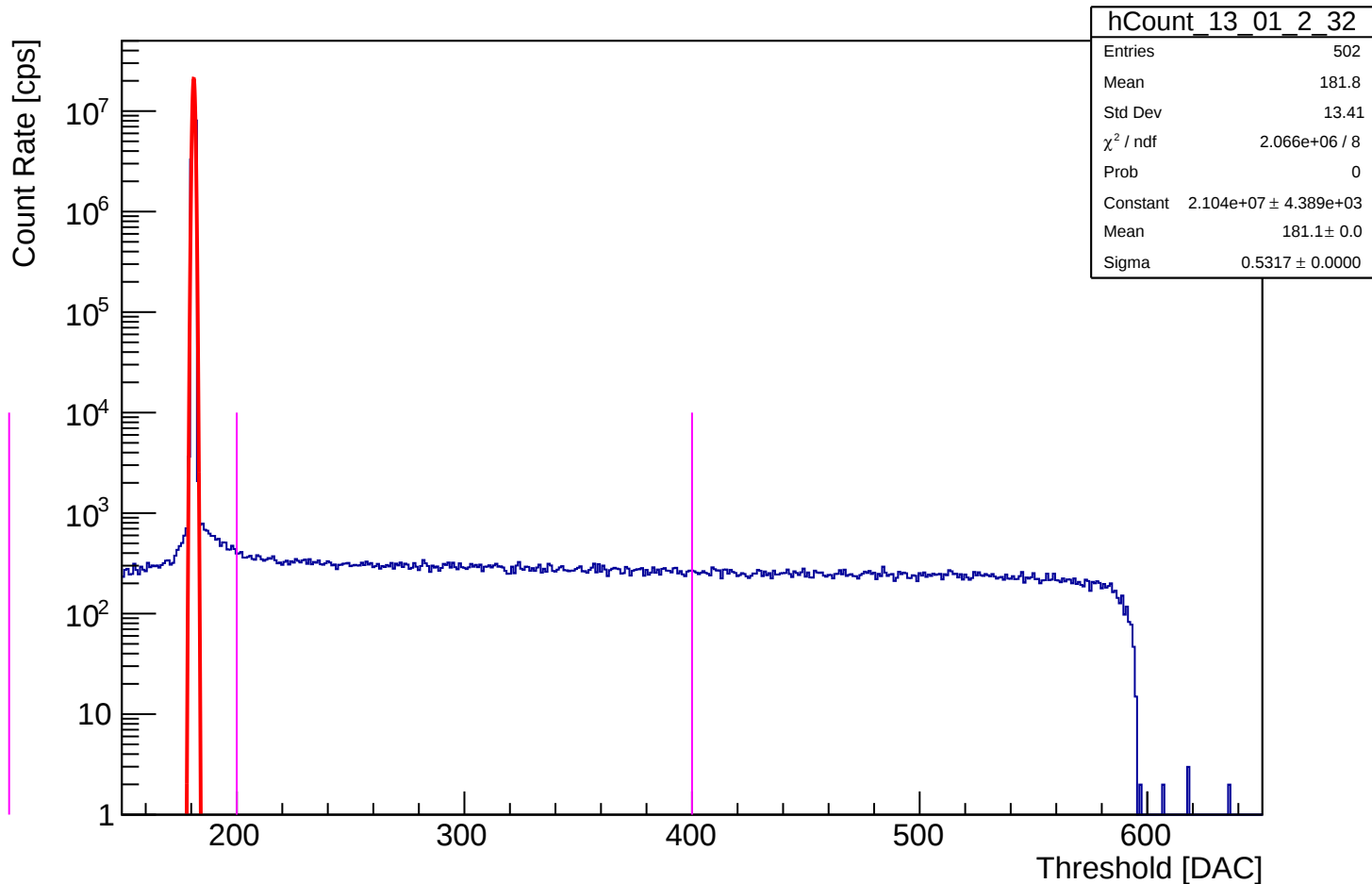
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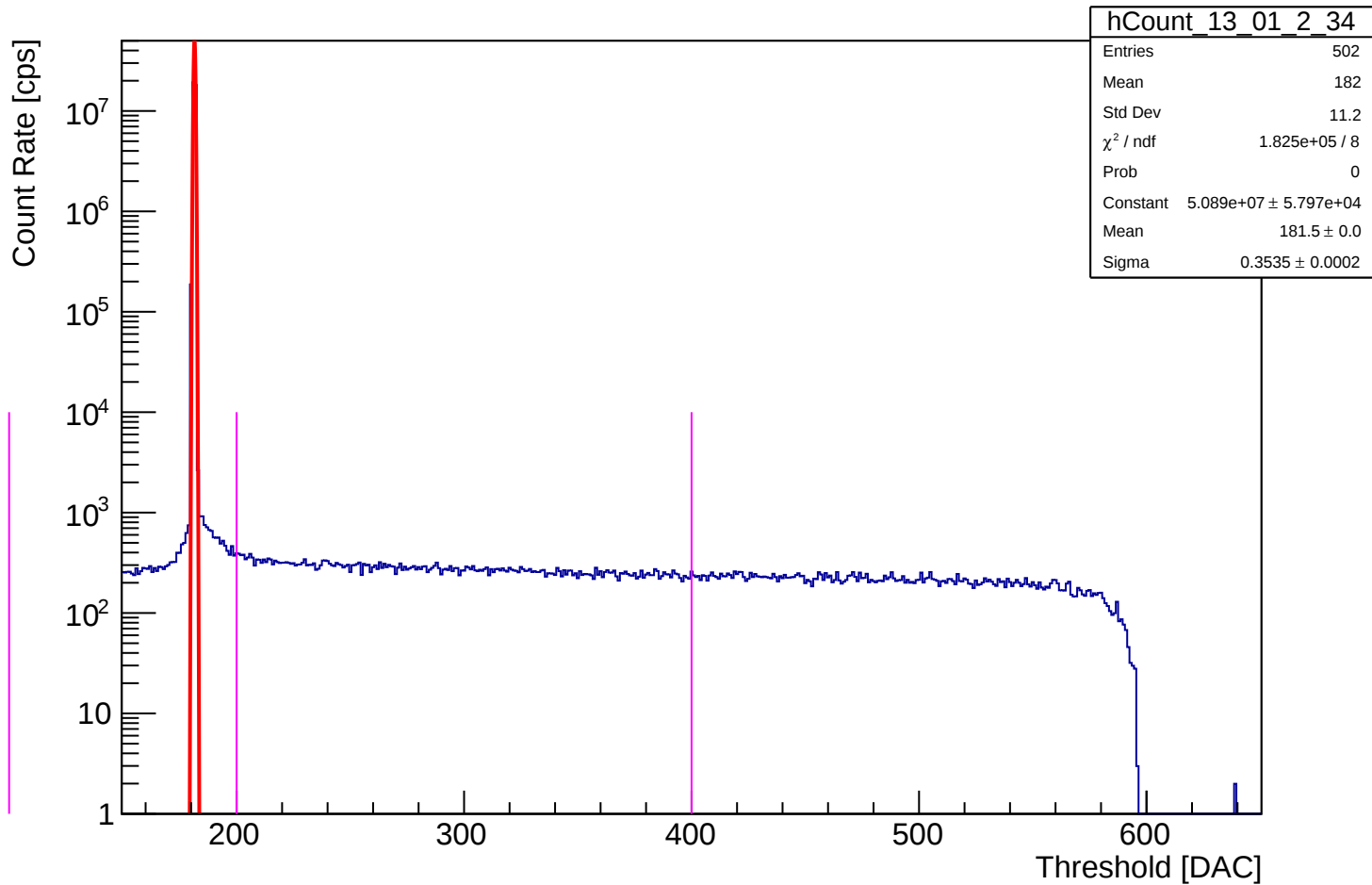
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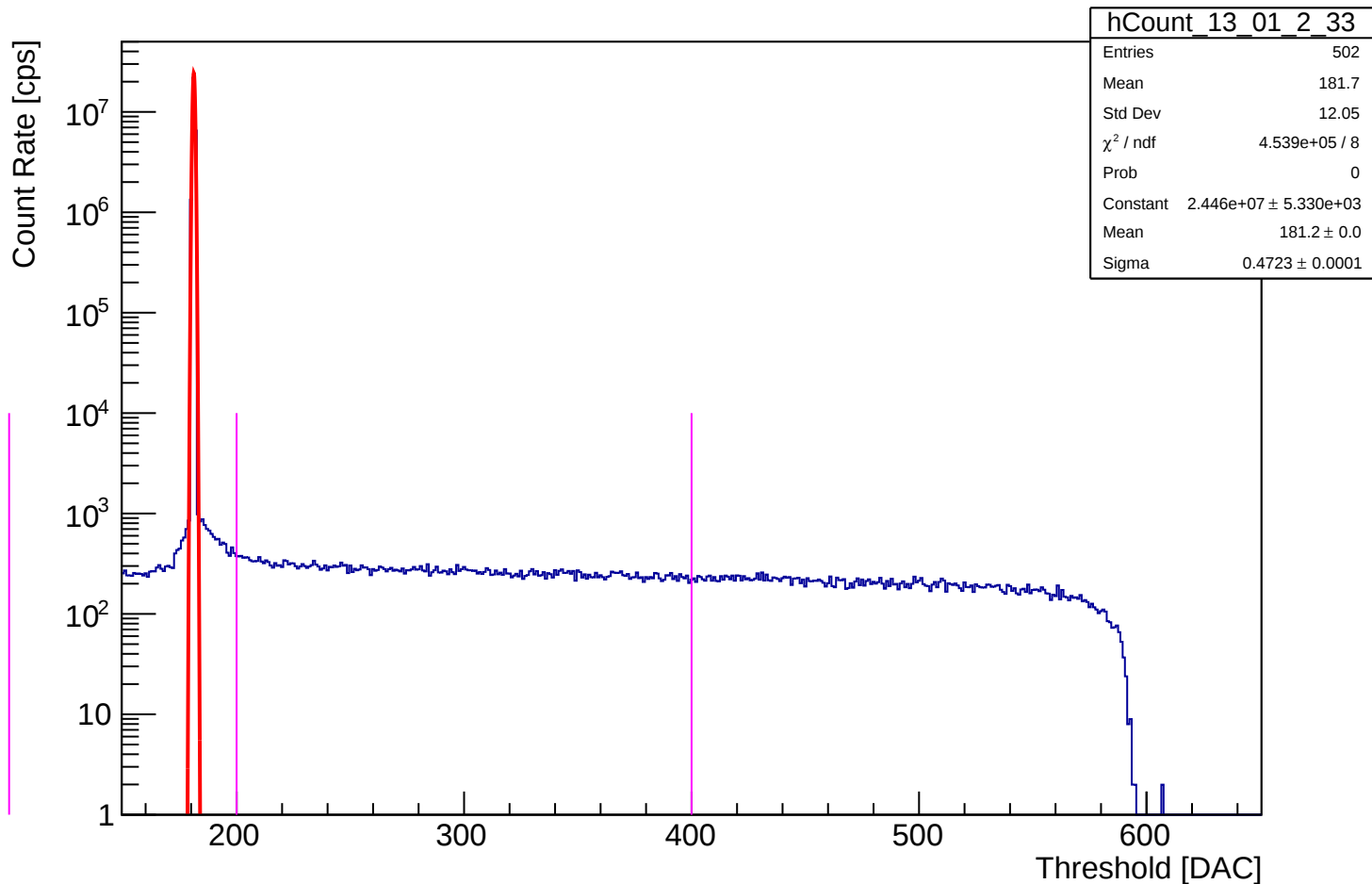
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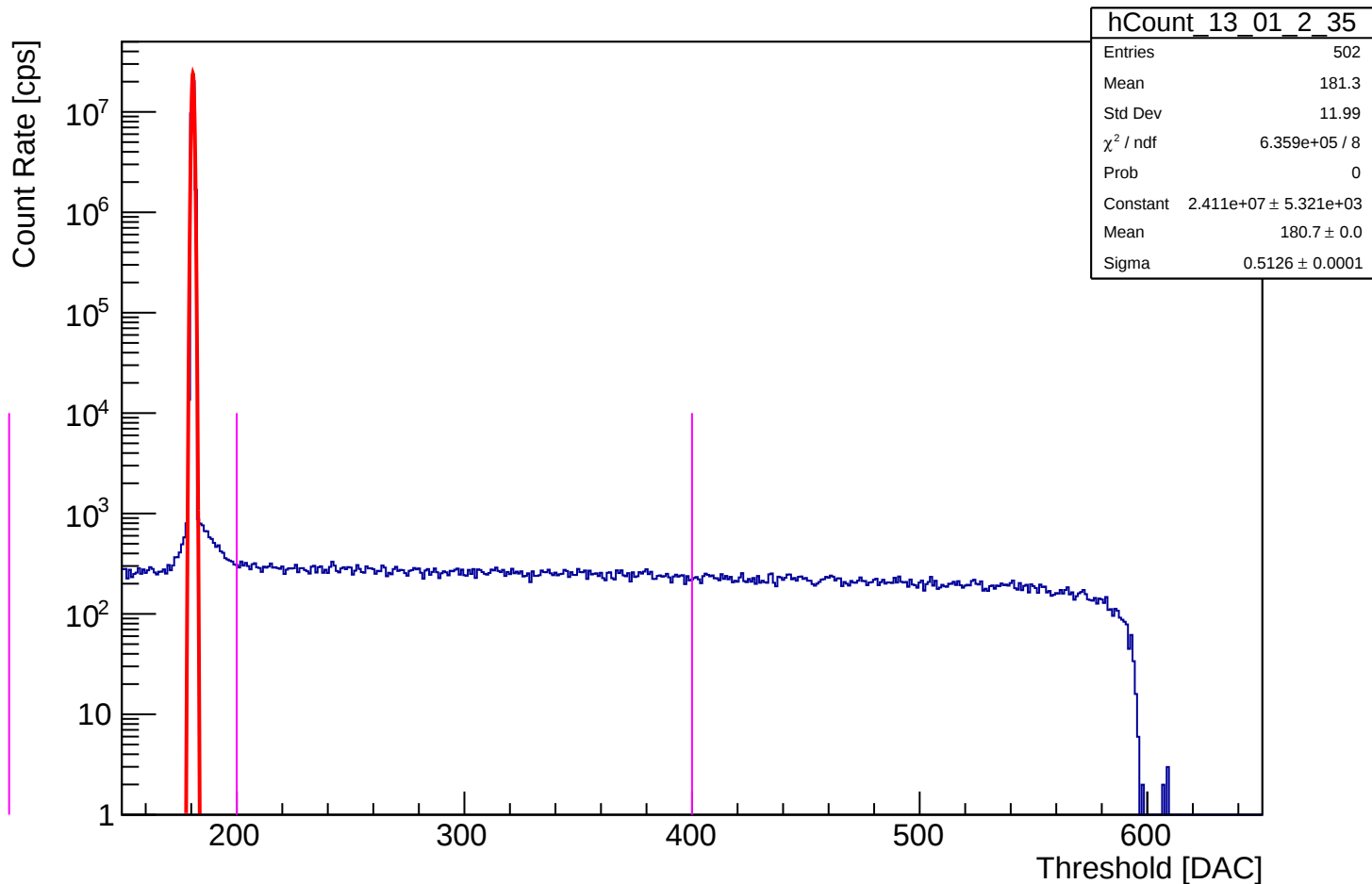


Row 1 Tile 1 Pmt 6 Pixel 6 Slot 13 Fiber 1 Asic 2 Channel 34

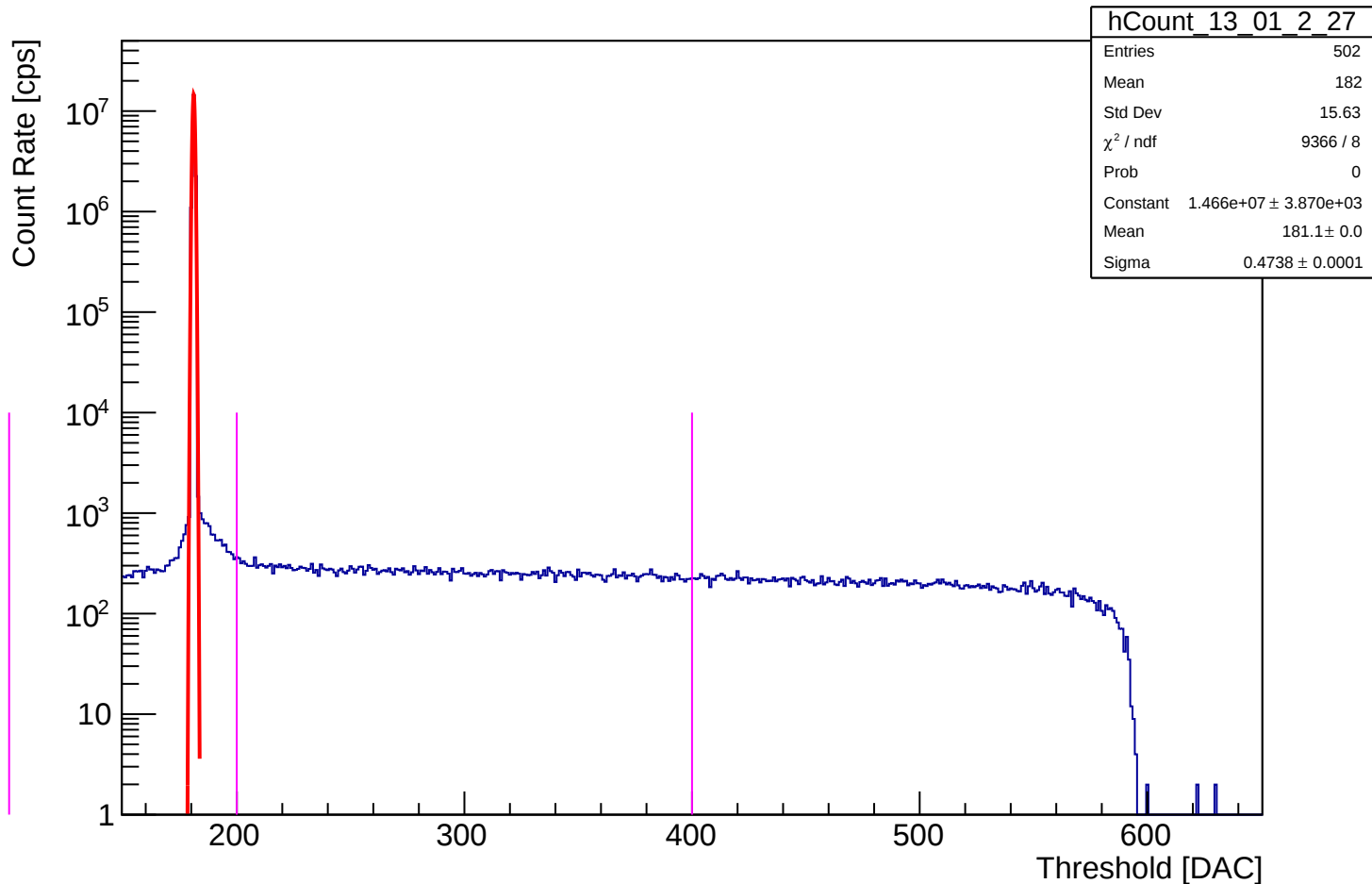


Row 1 Tile 1 Pmt 6 Pixel 7 Slot 13 Fiber 1 Asic 2 Channel 33

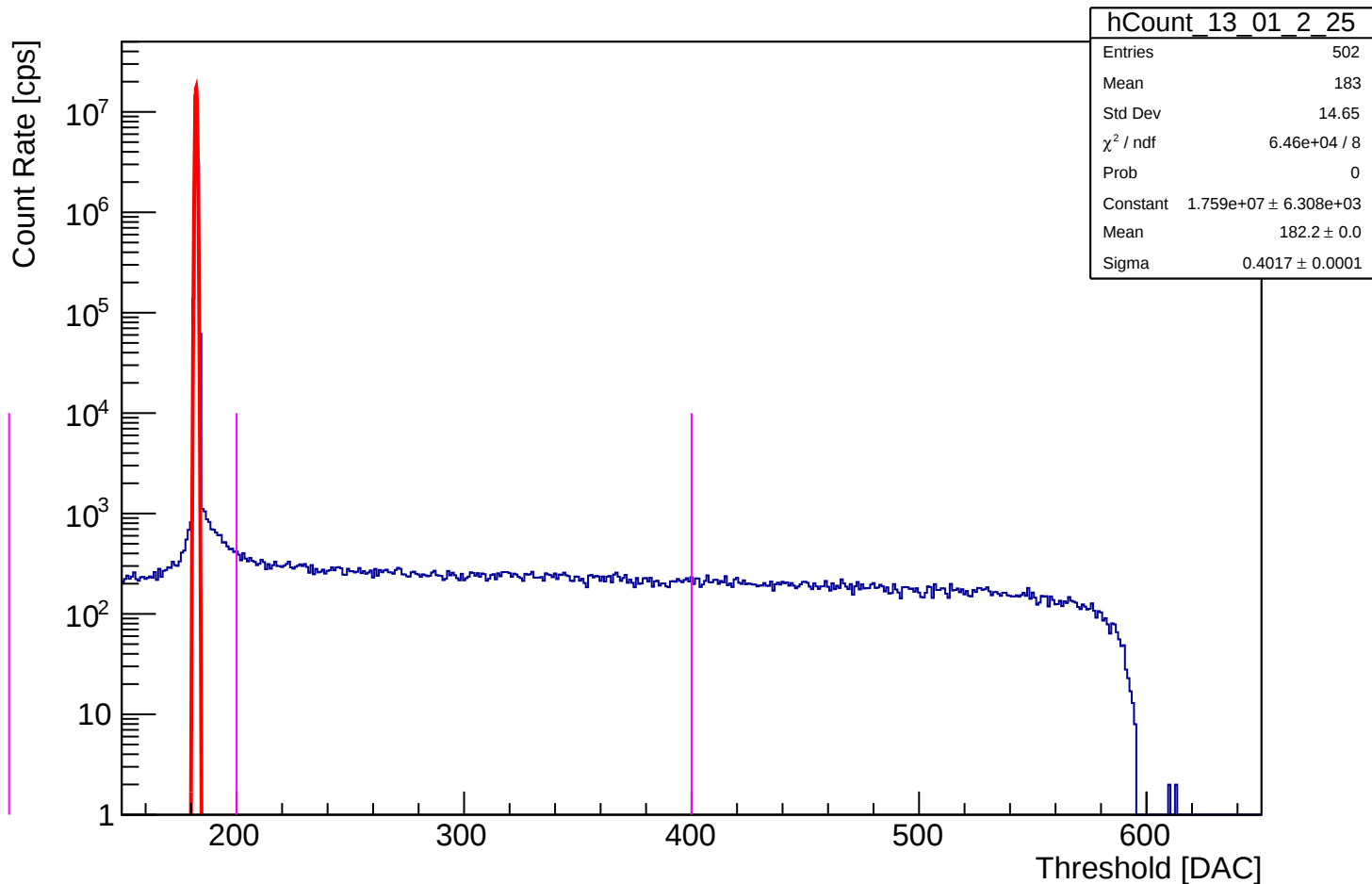




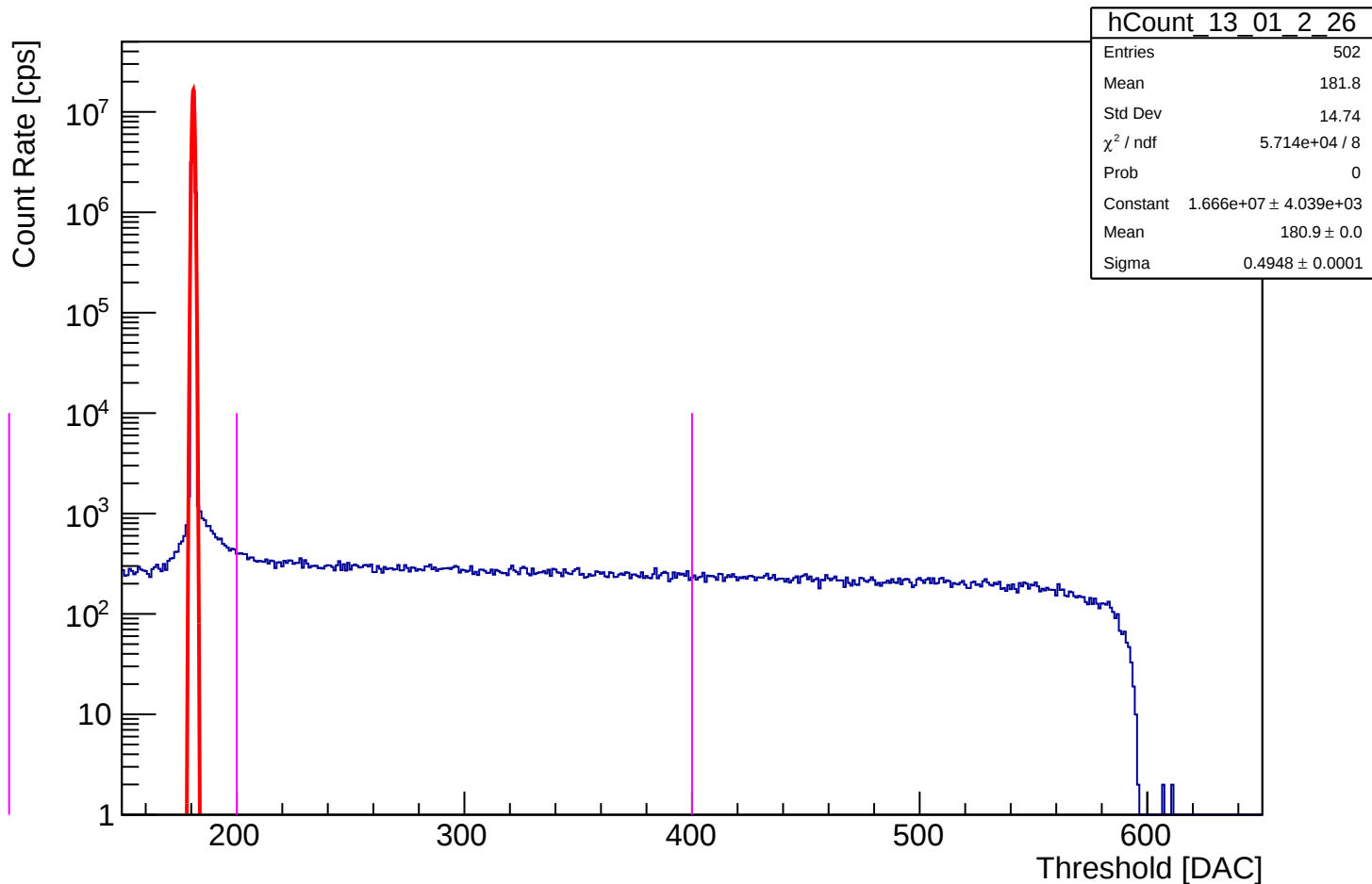
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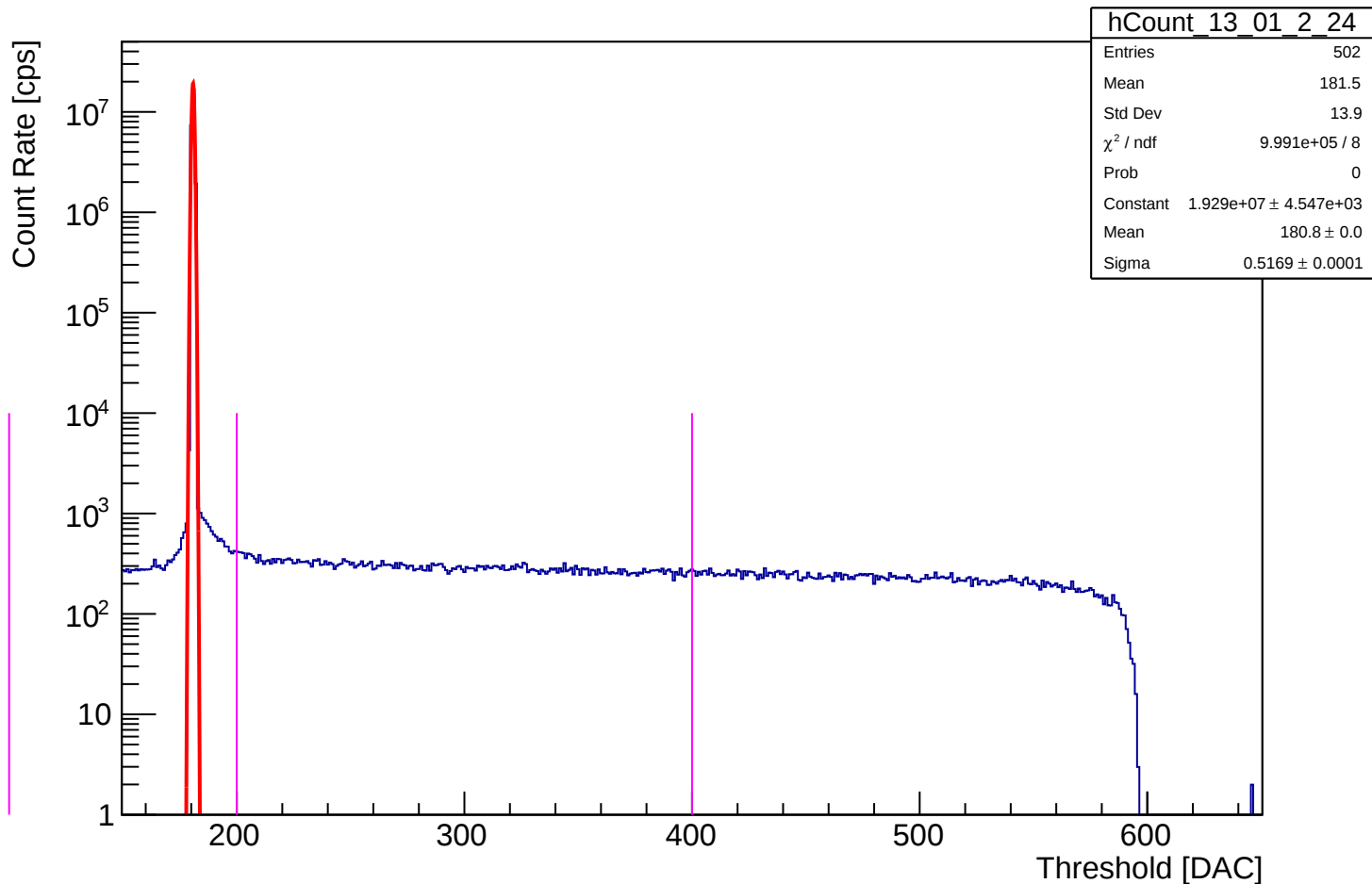
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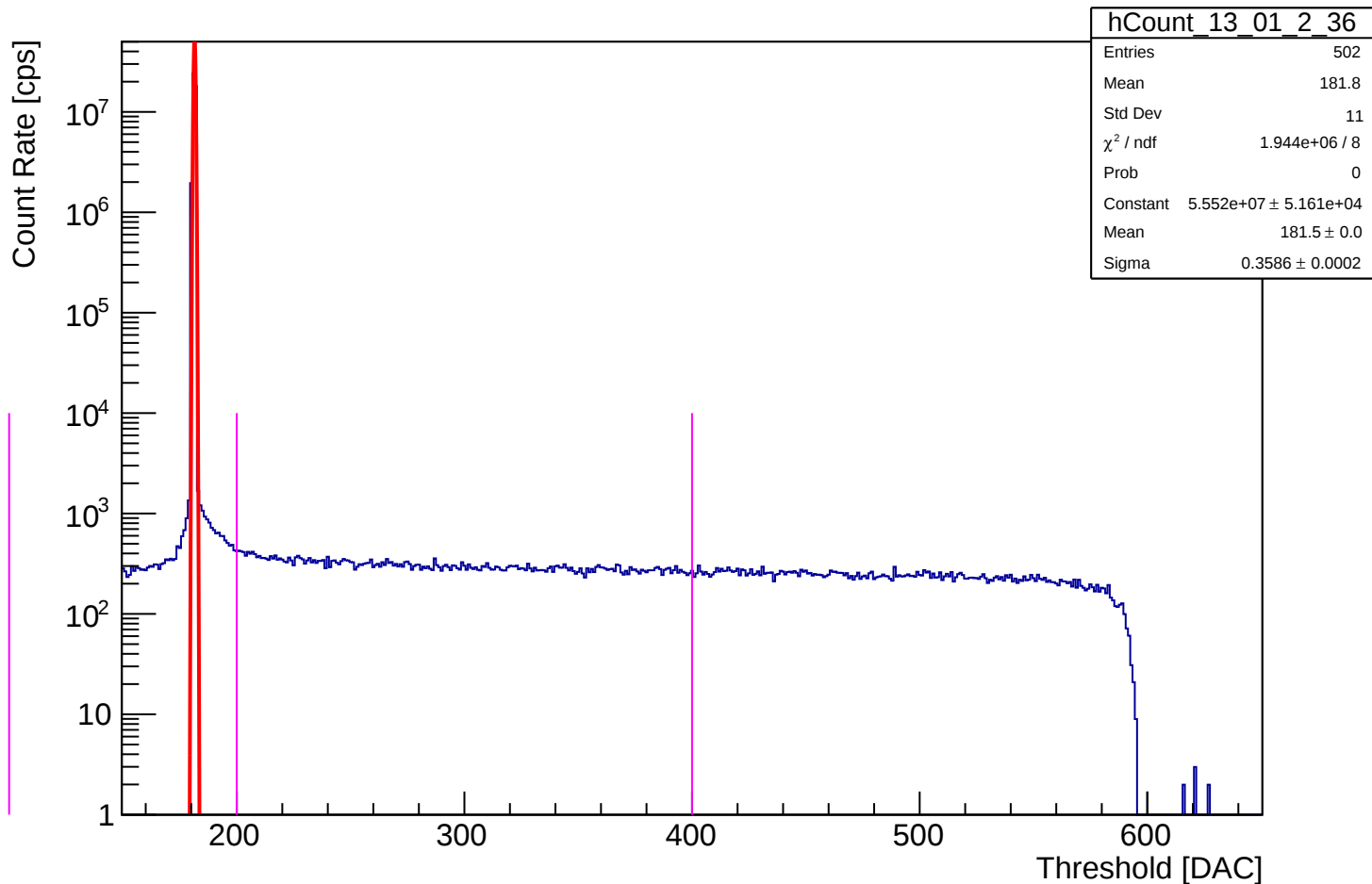
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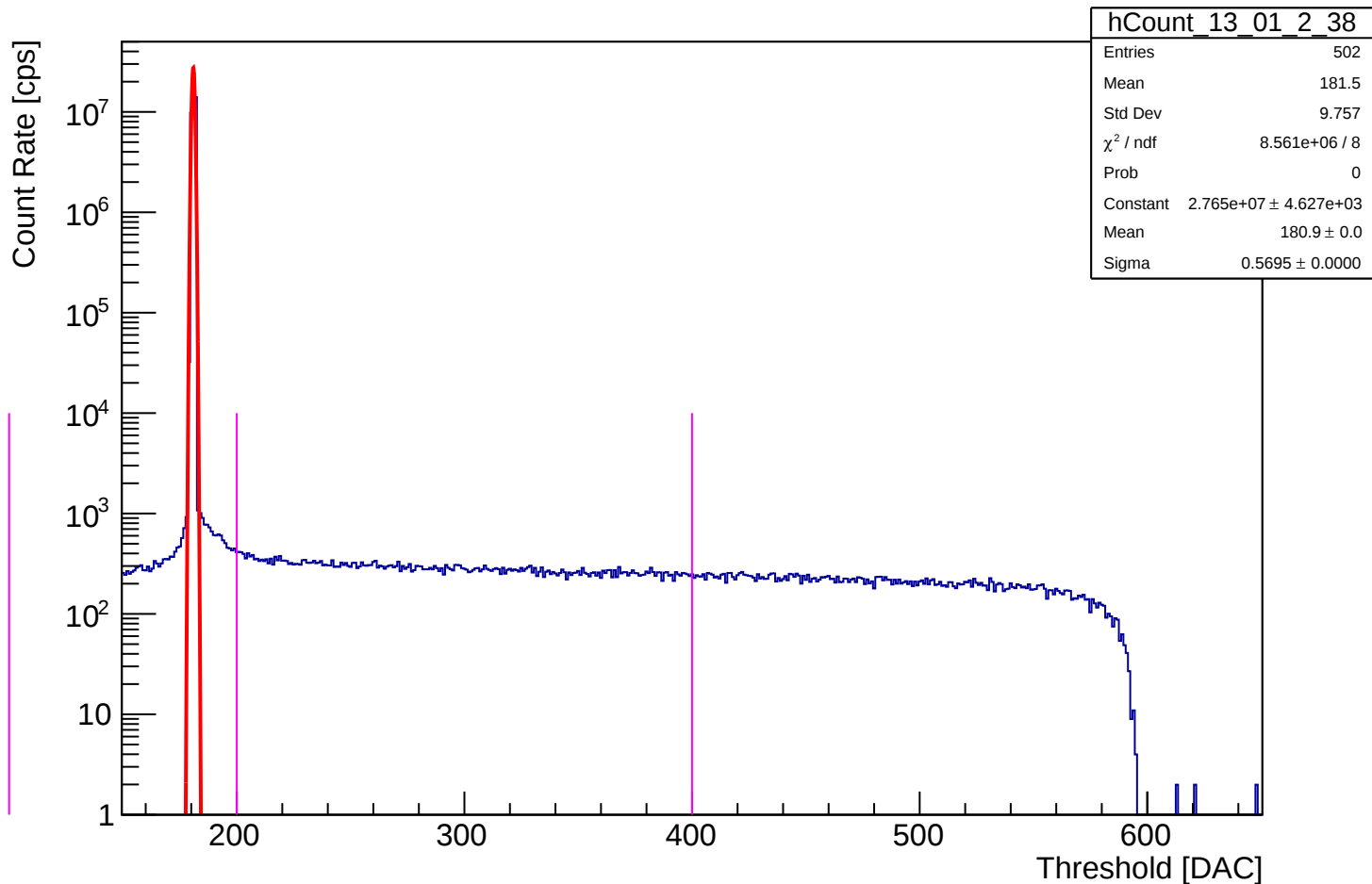
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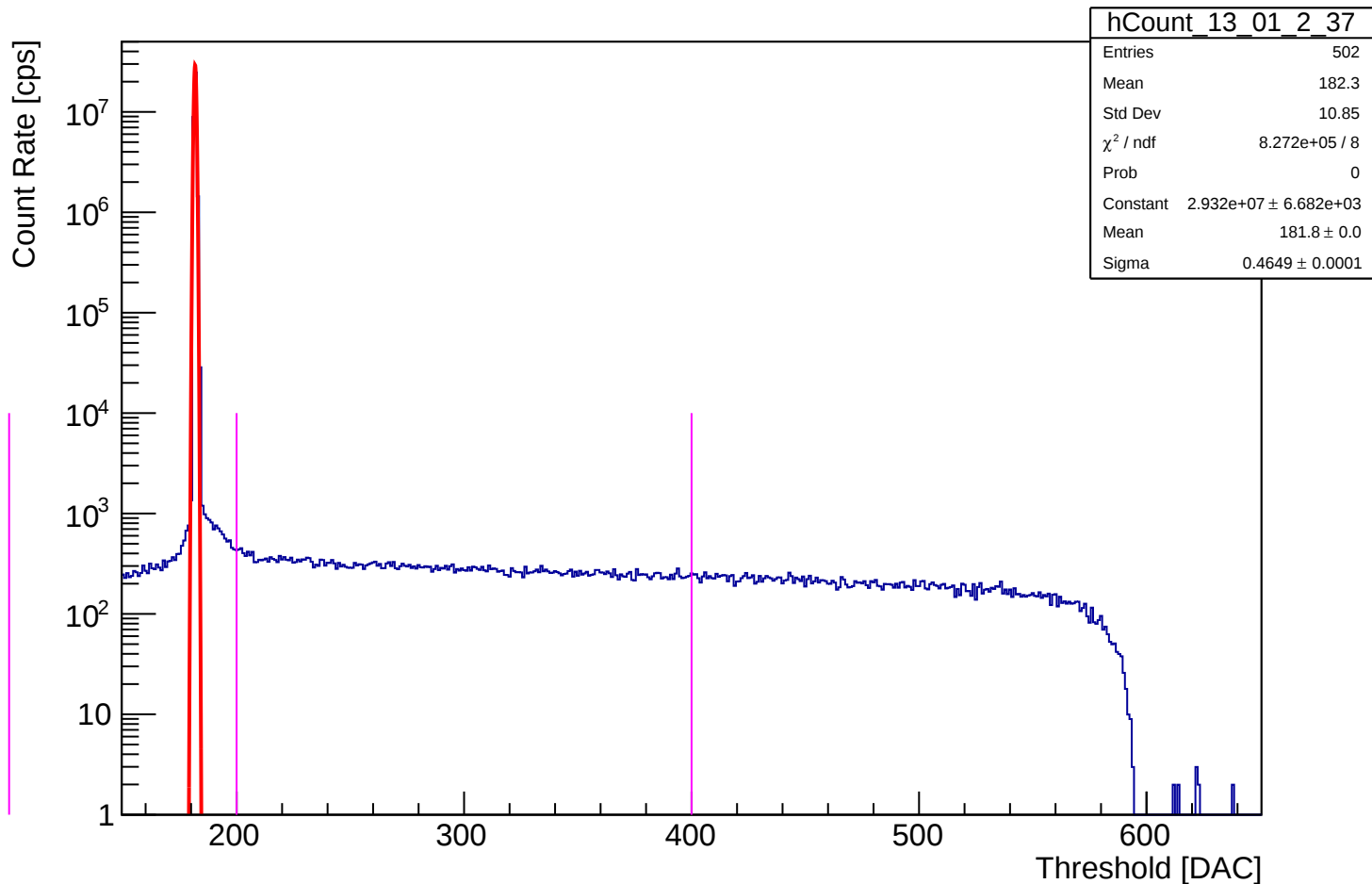
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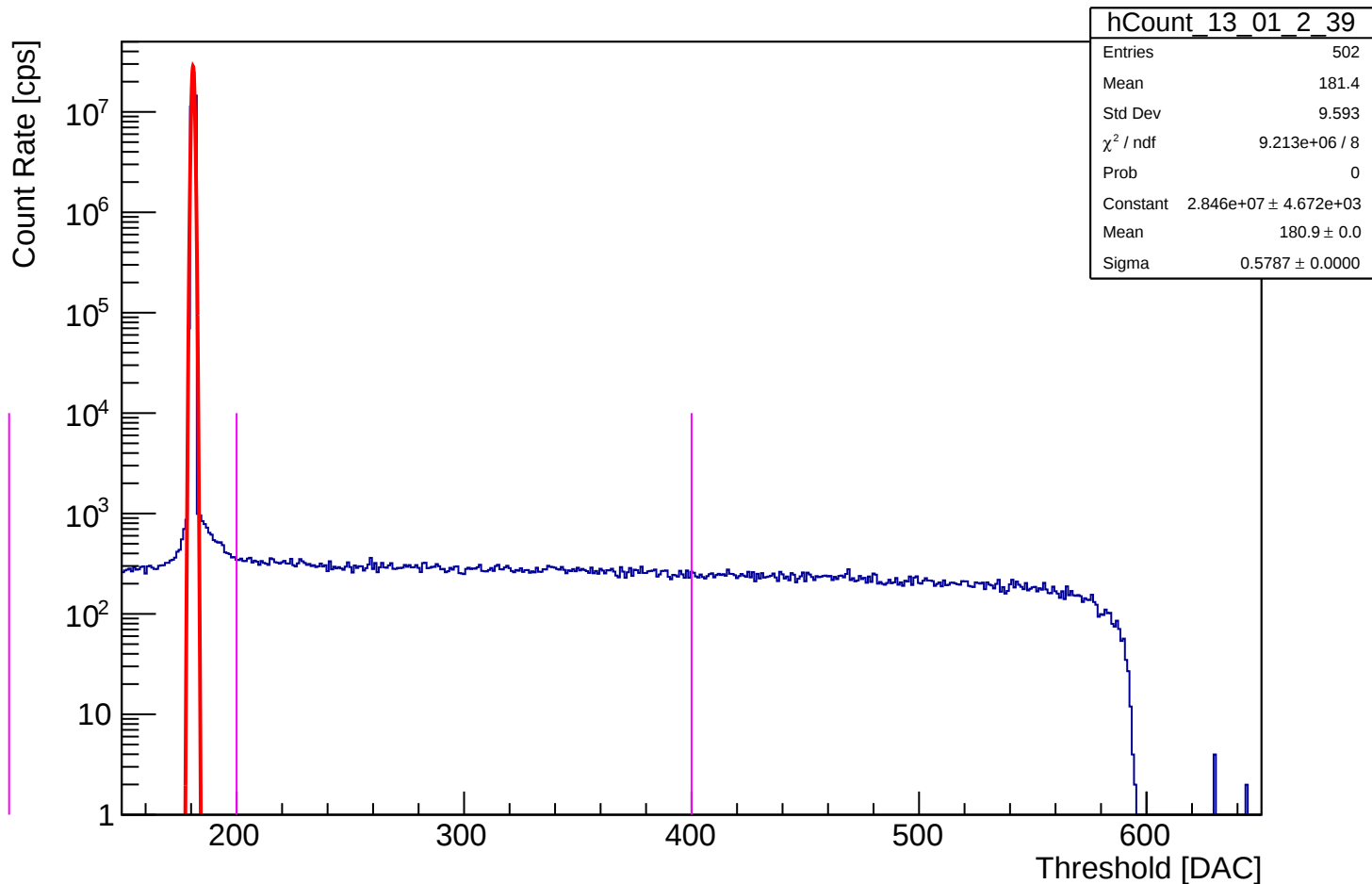
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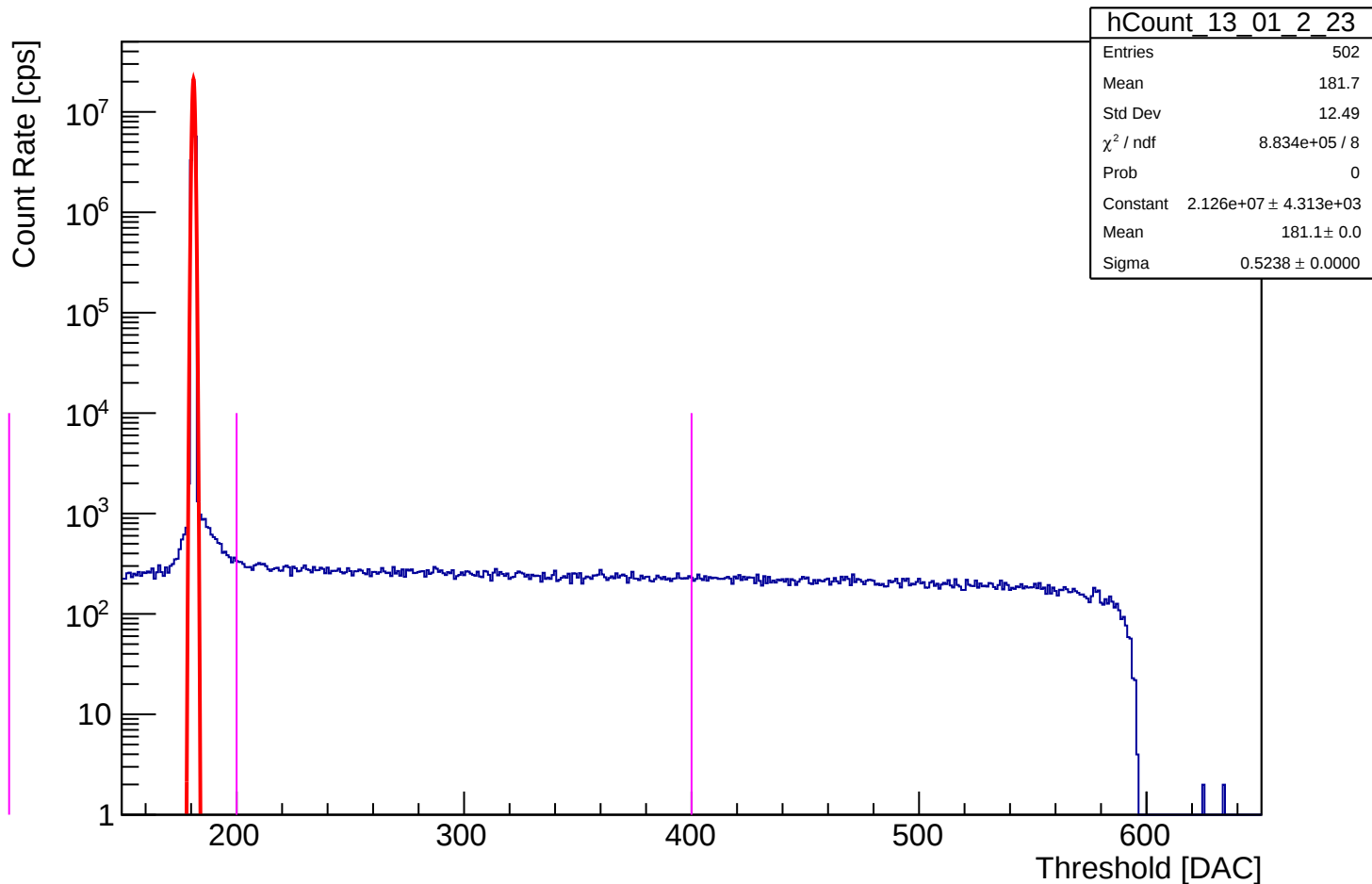
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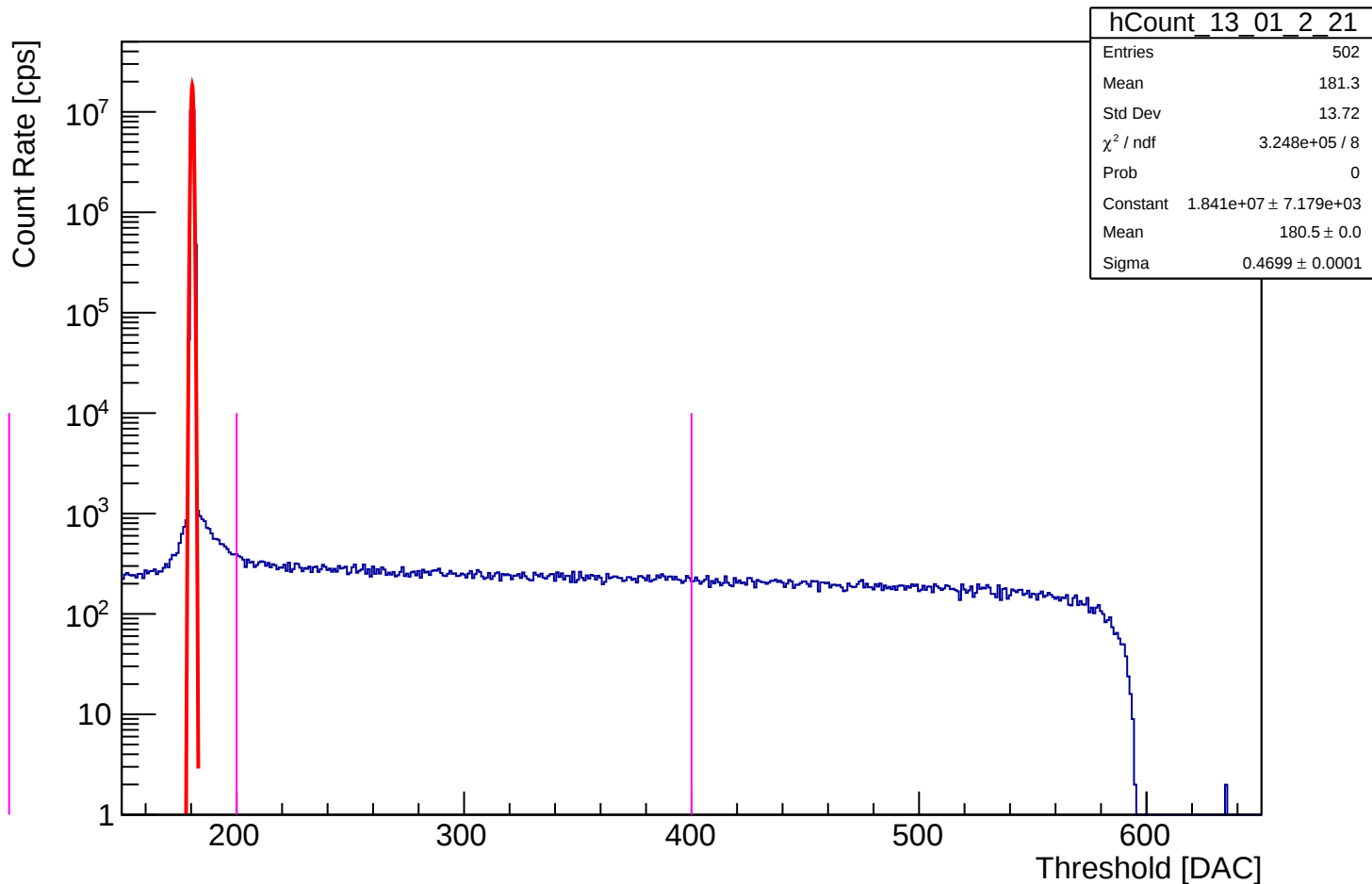
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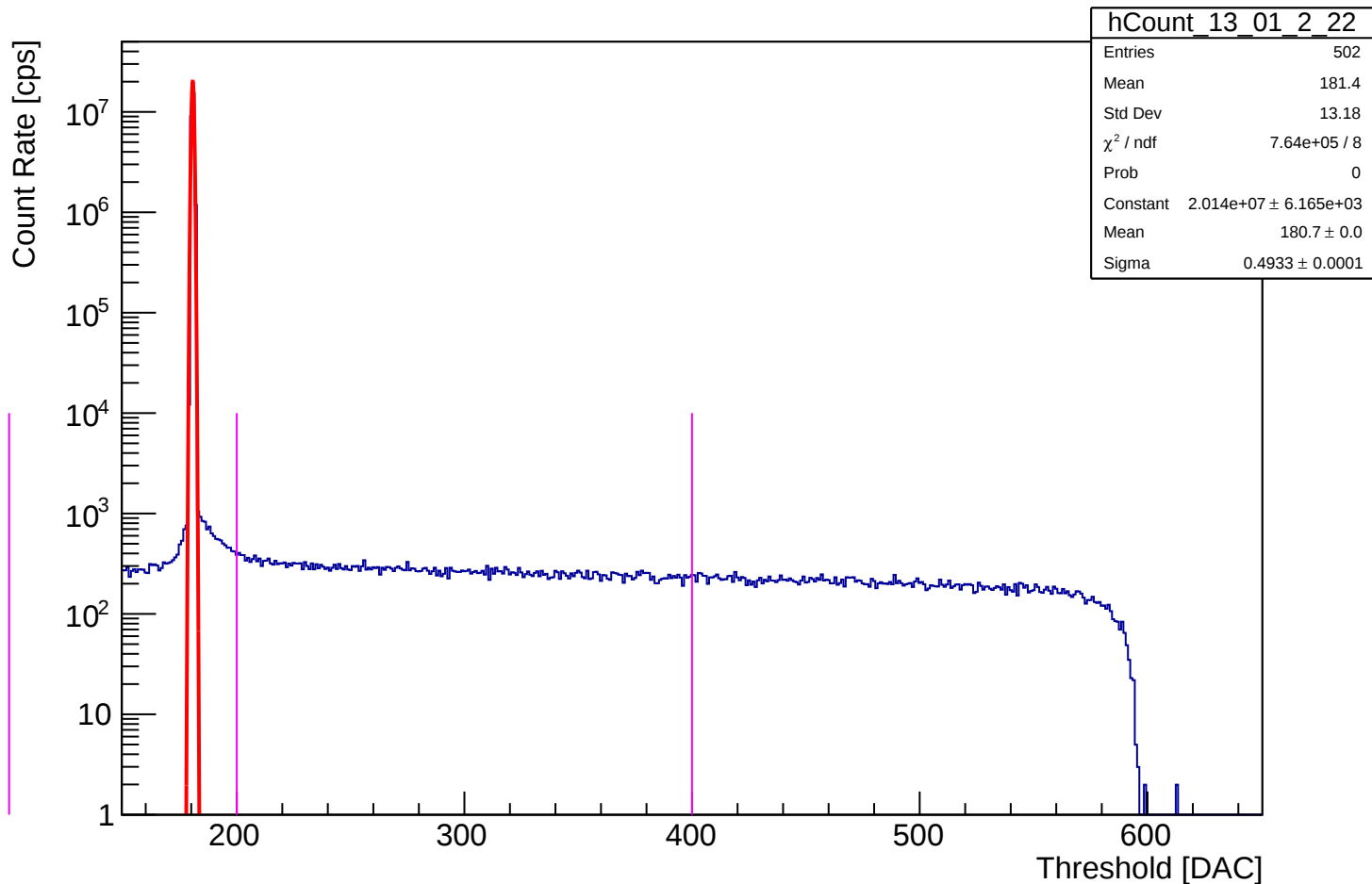
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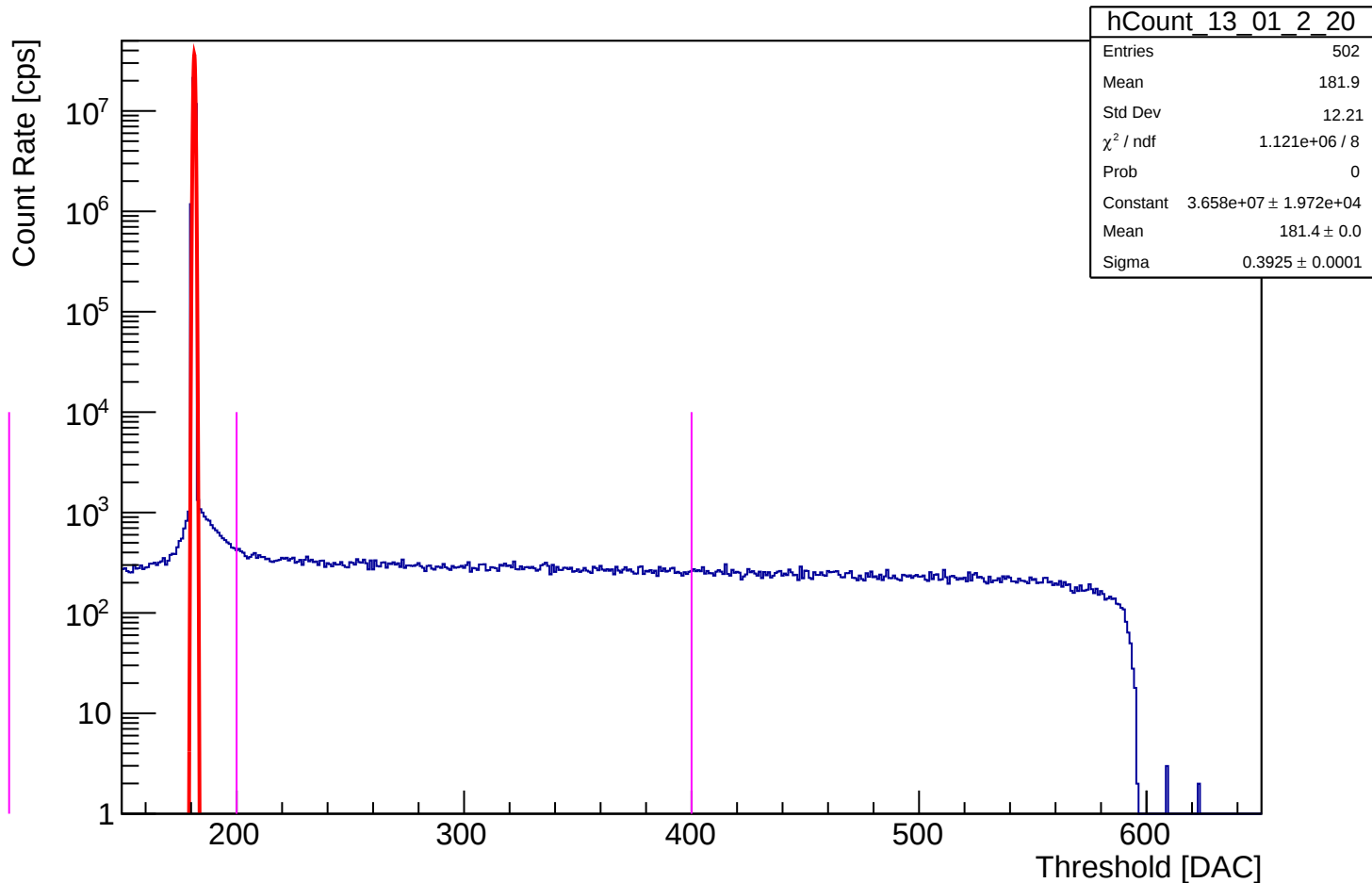
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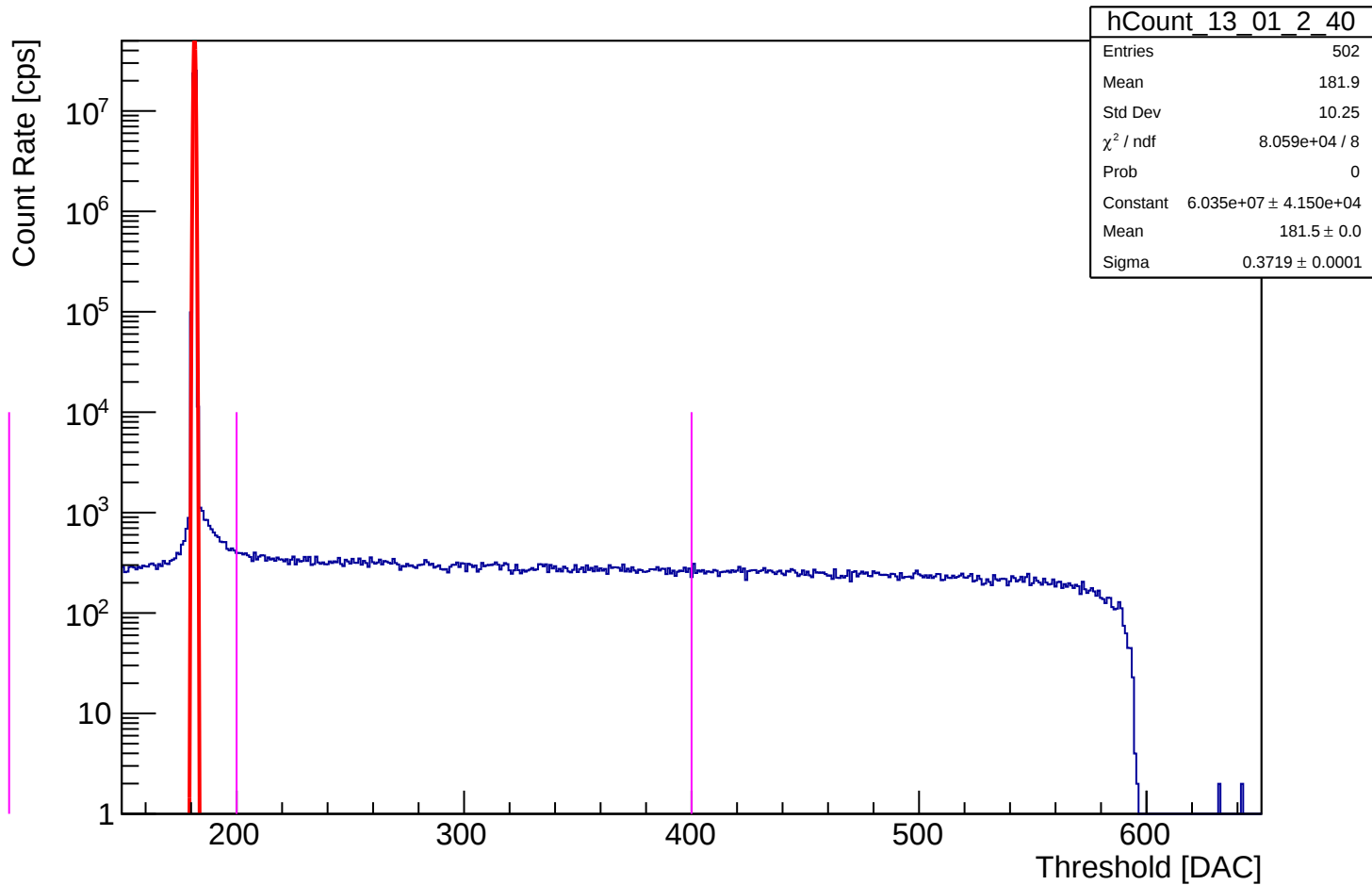
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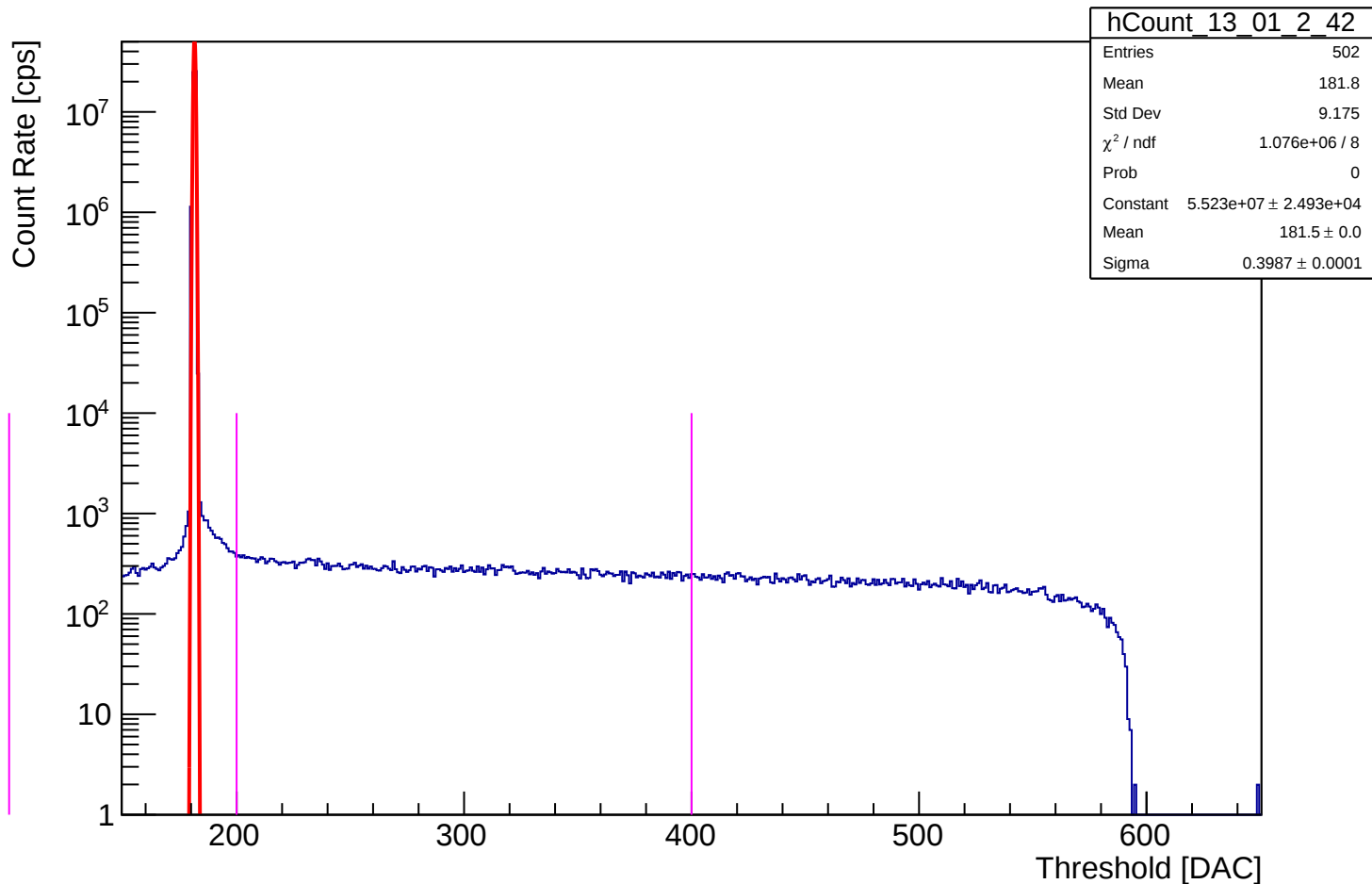
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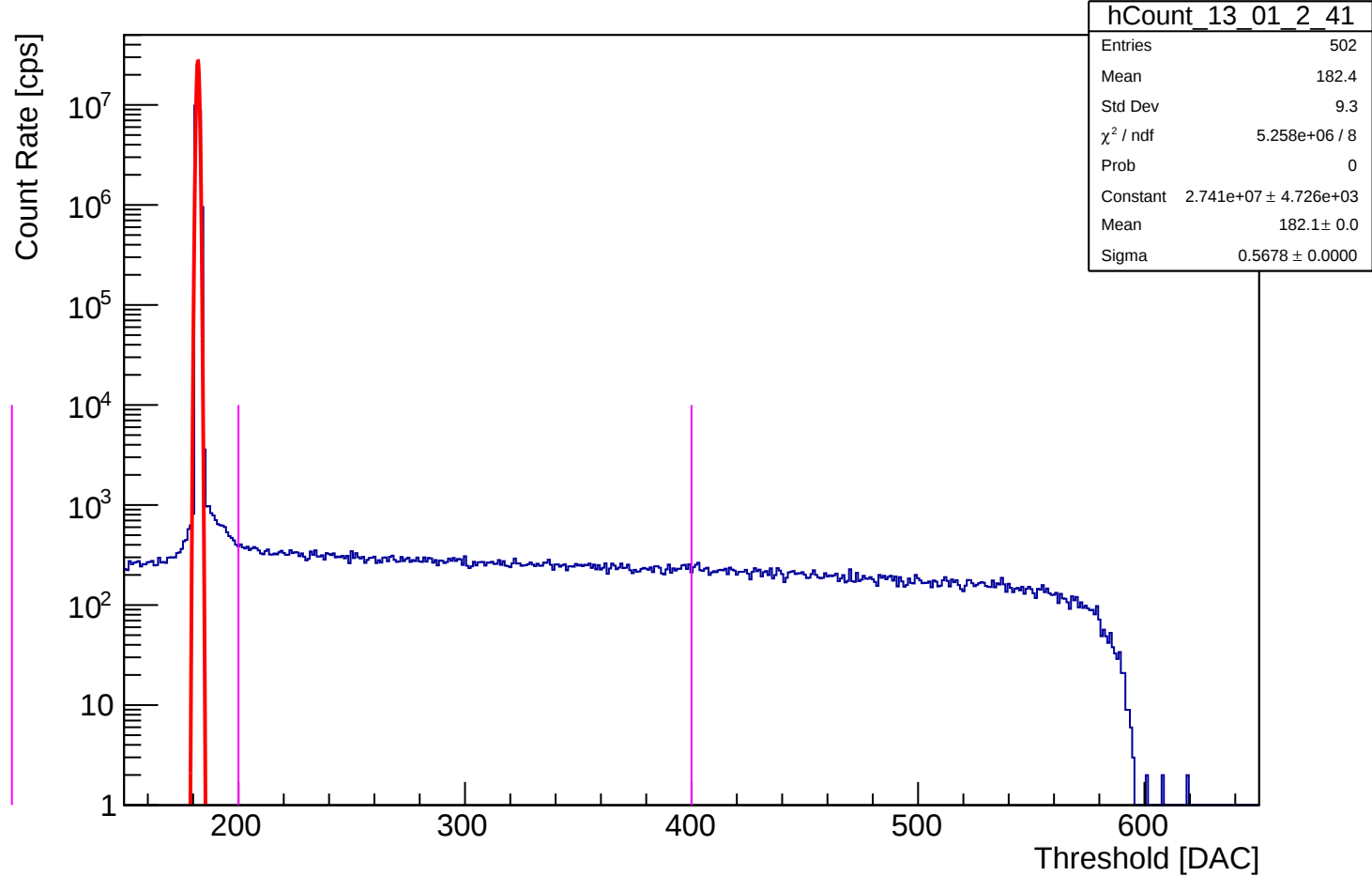


Row 1 Tile 1 Pmt 6 Pixel 21 Slot 13 Fiber 1 Asic 2 Channel 40

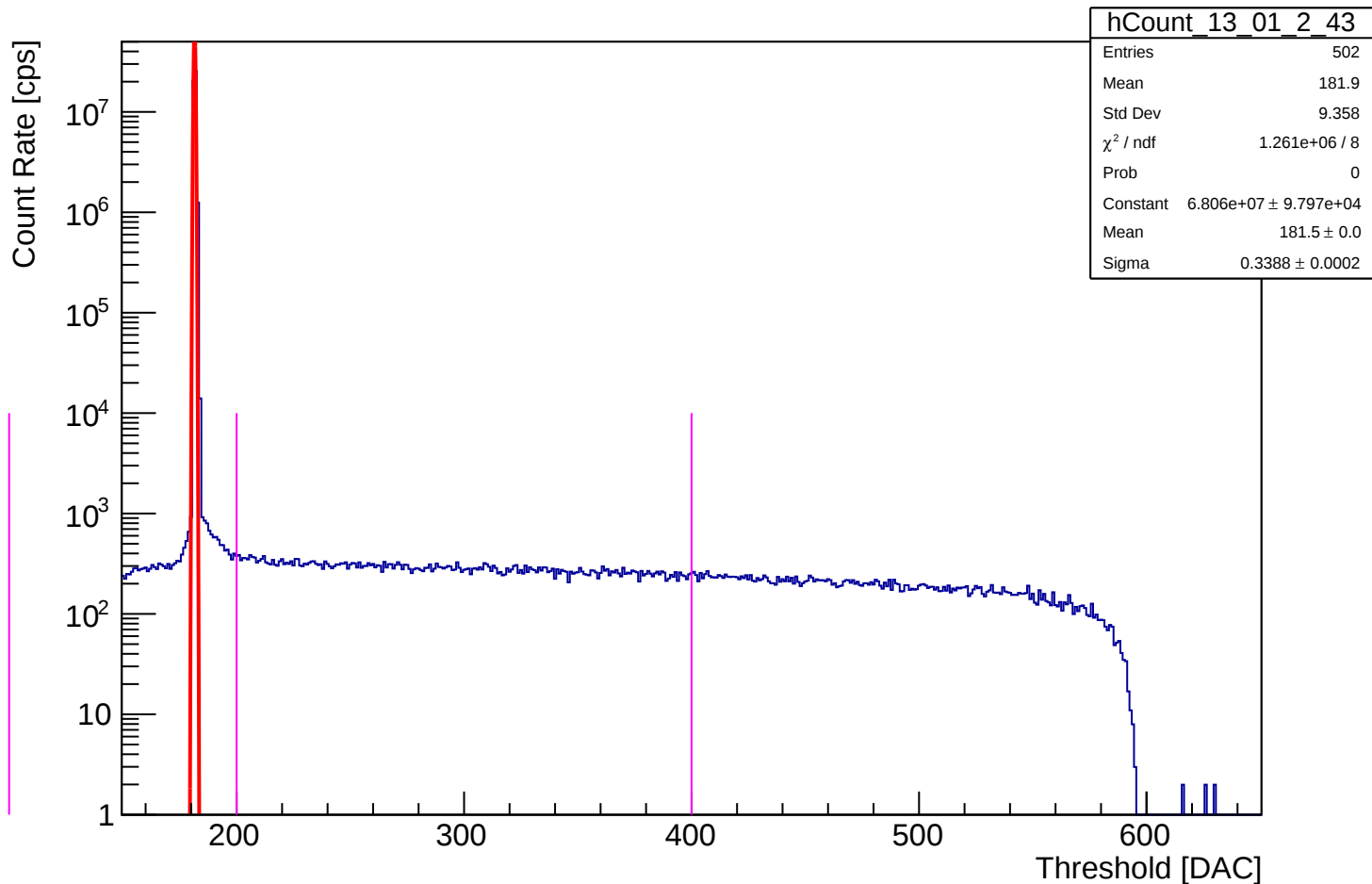


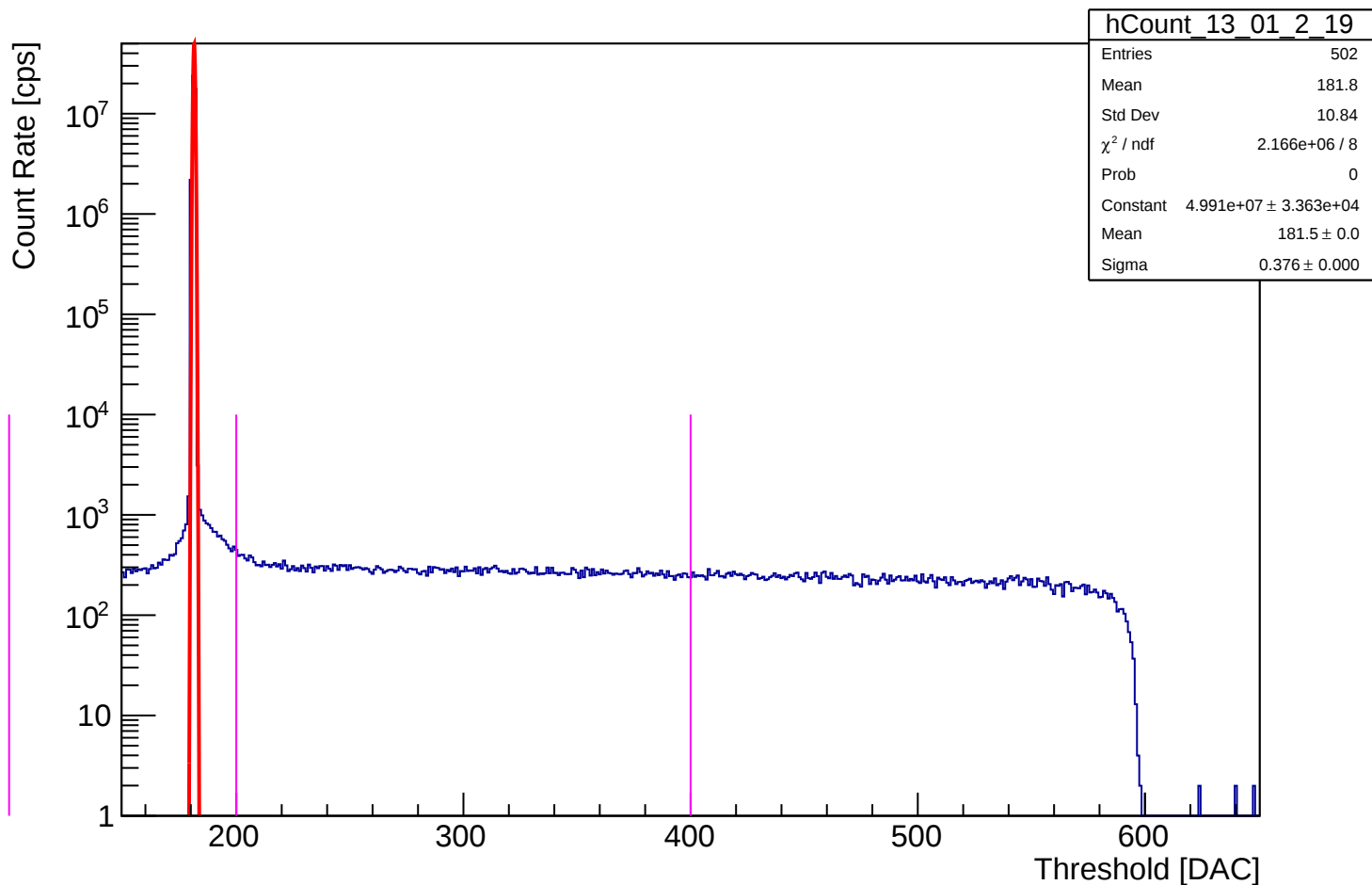
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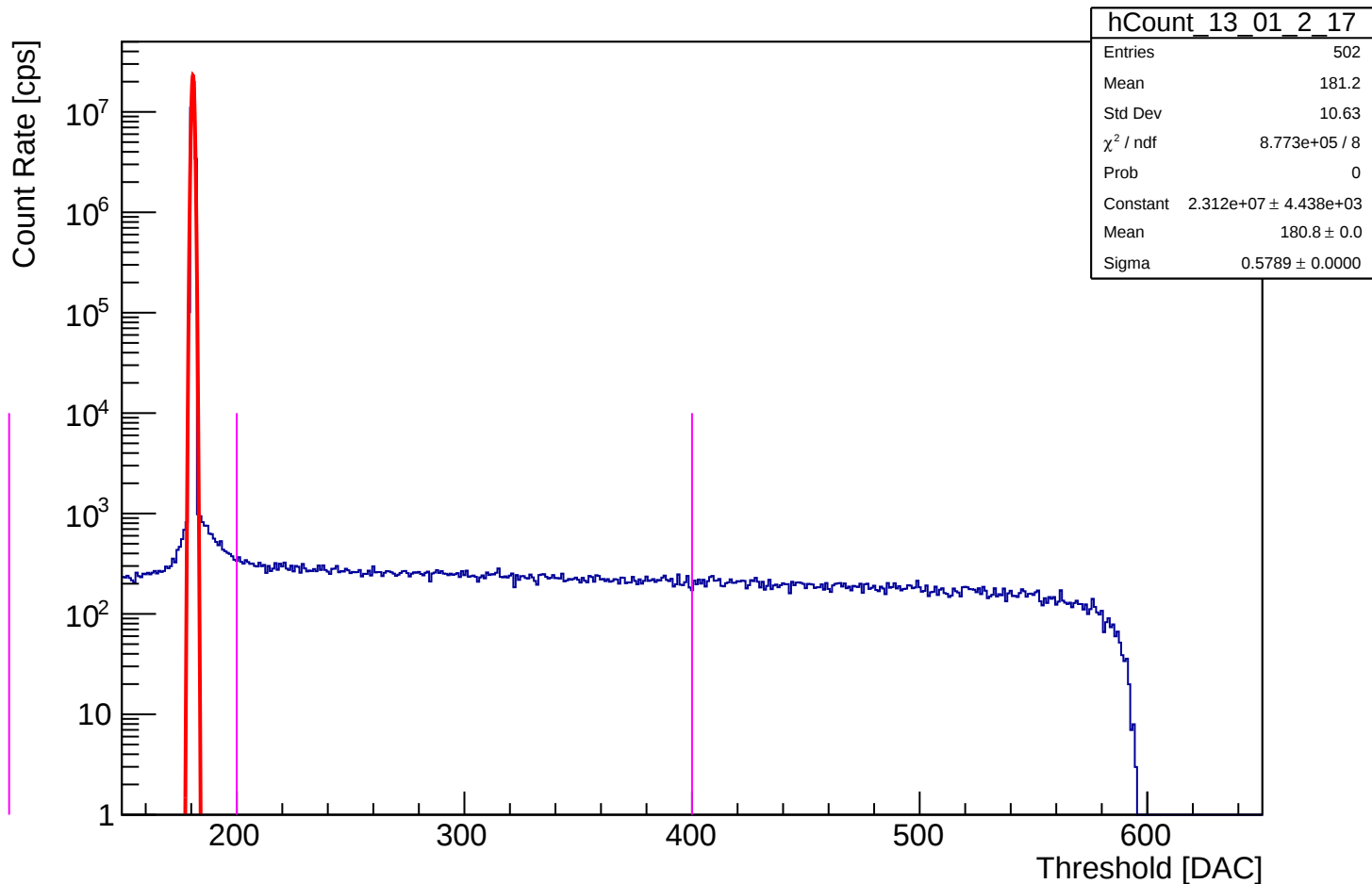


Row 1 Tile 1 Pmt 6 Pixel 24 Slot 13 Fiber 1 Asic 2 Channel 43

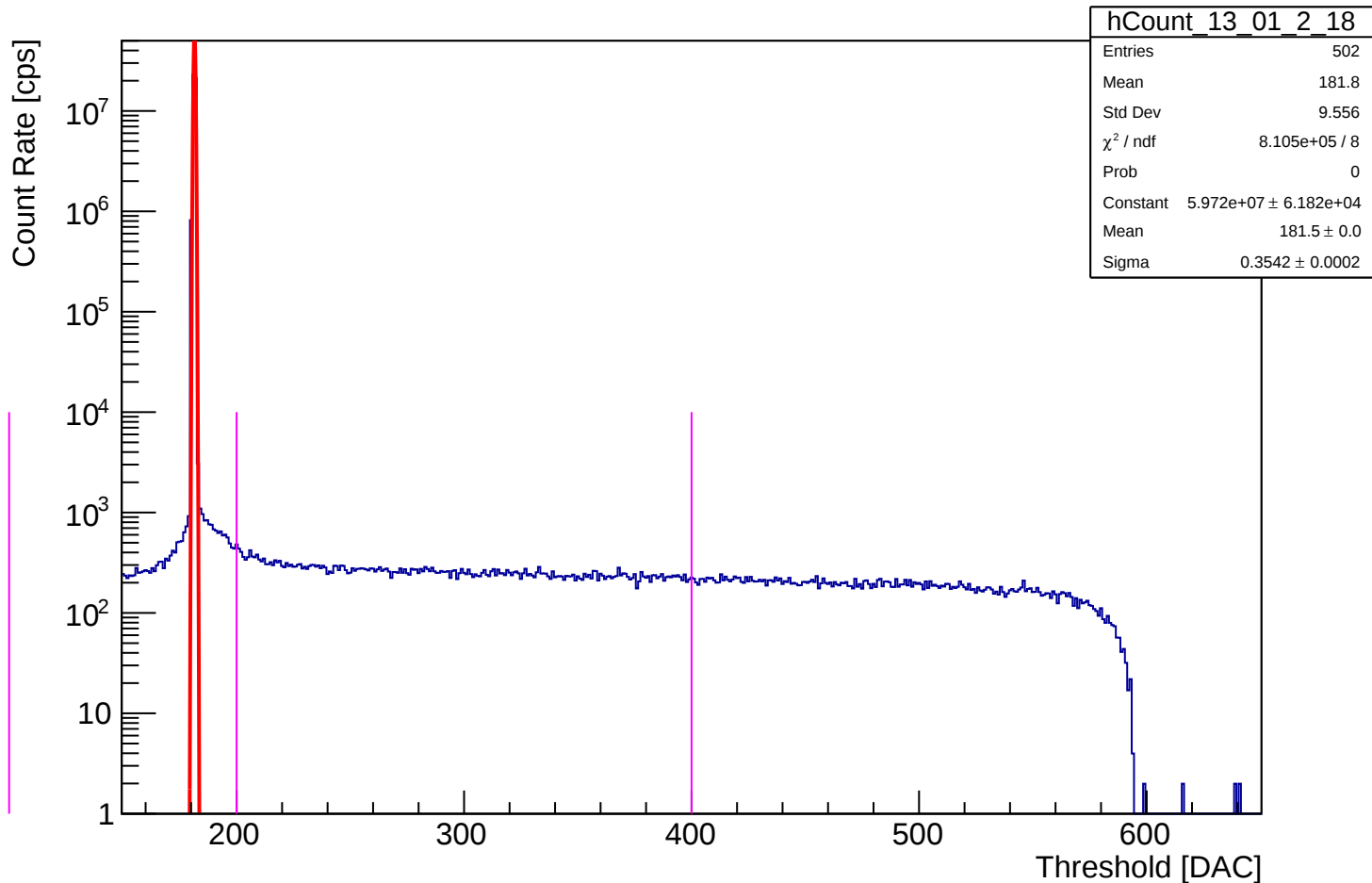




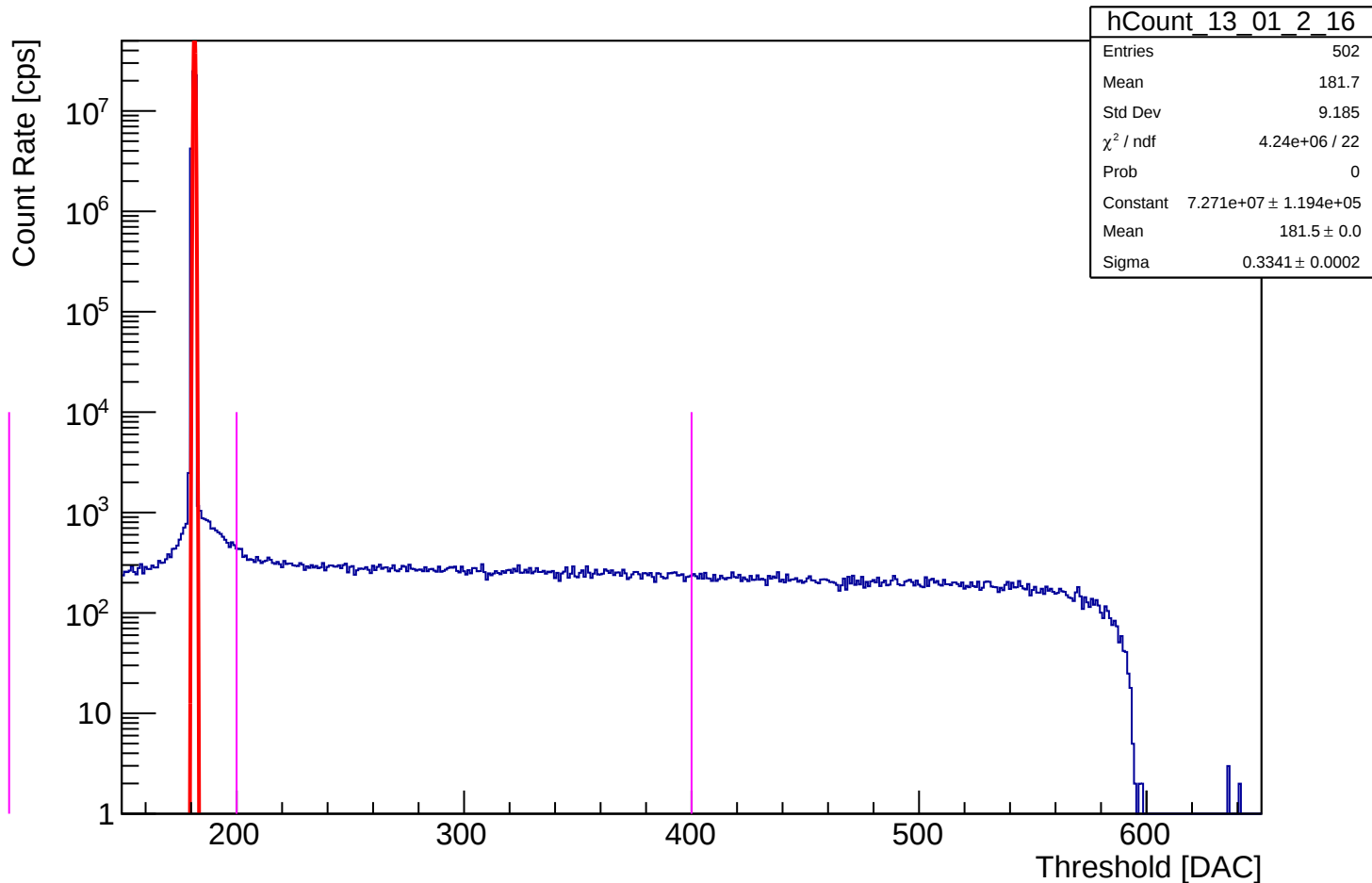
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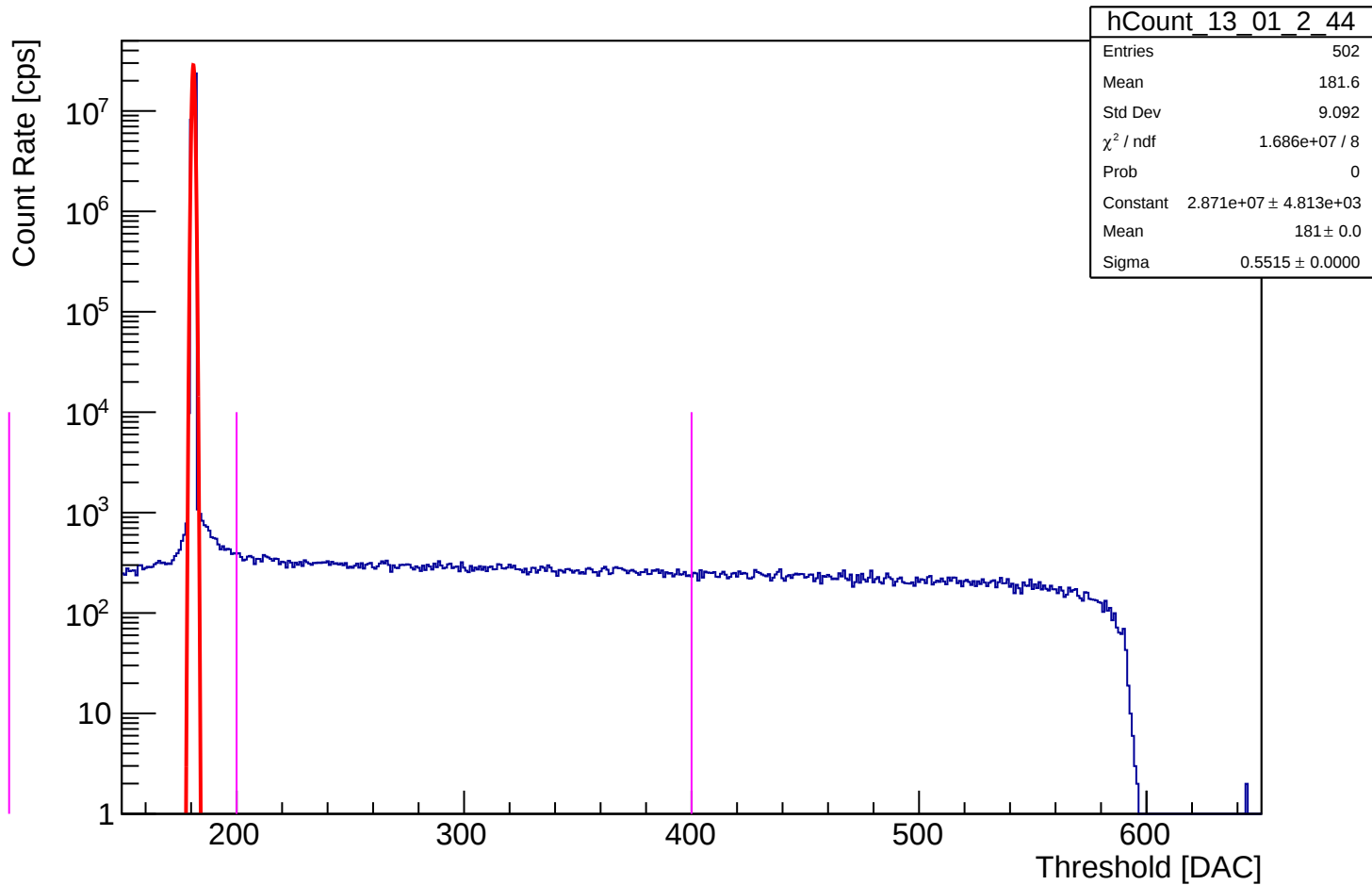
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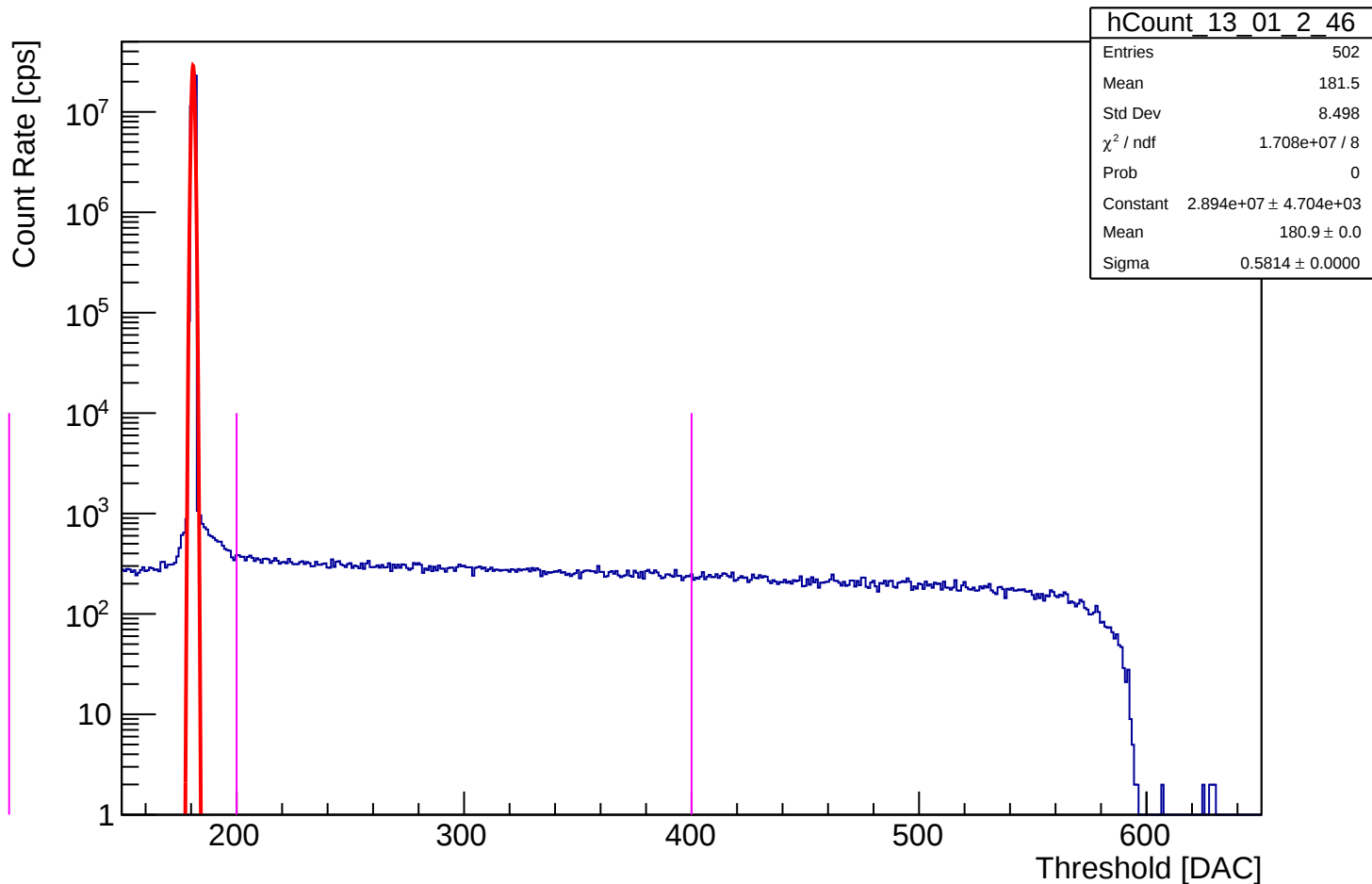
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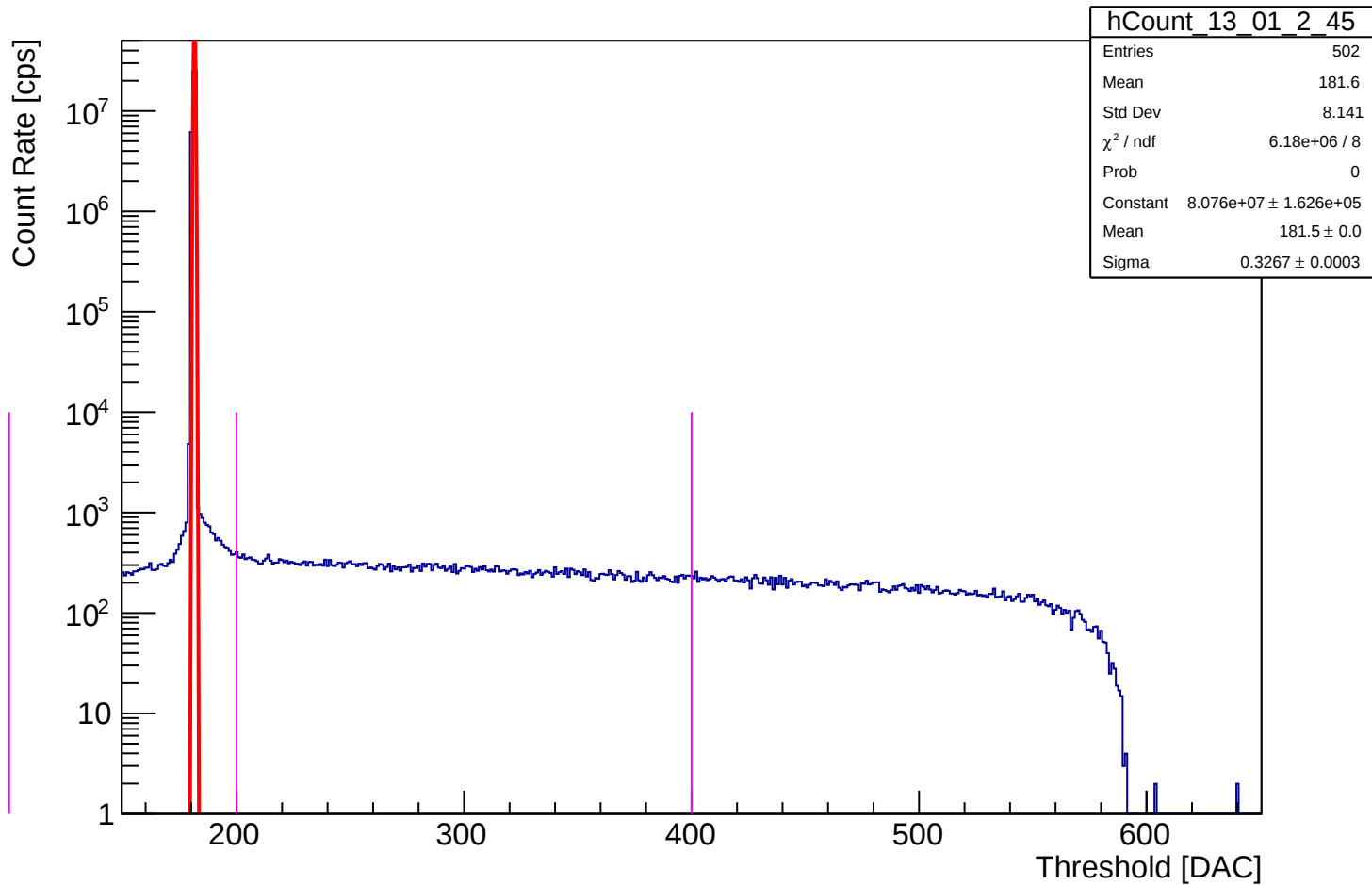
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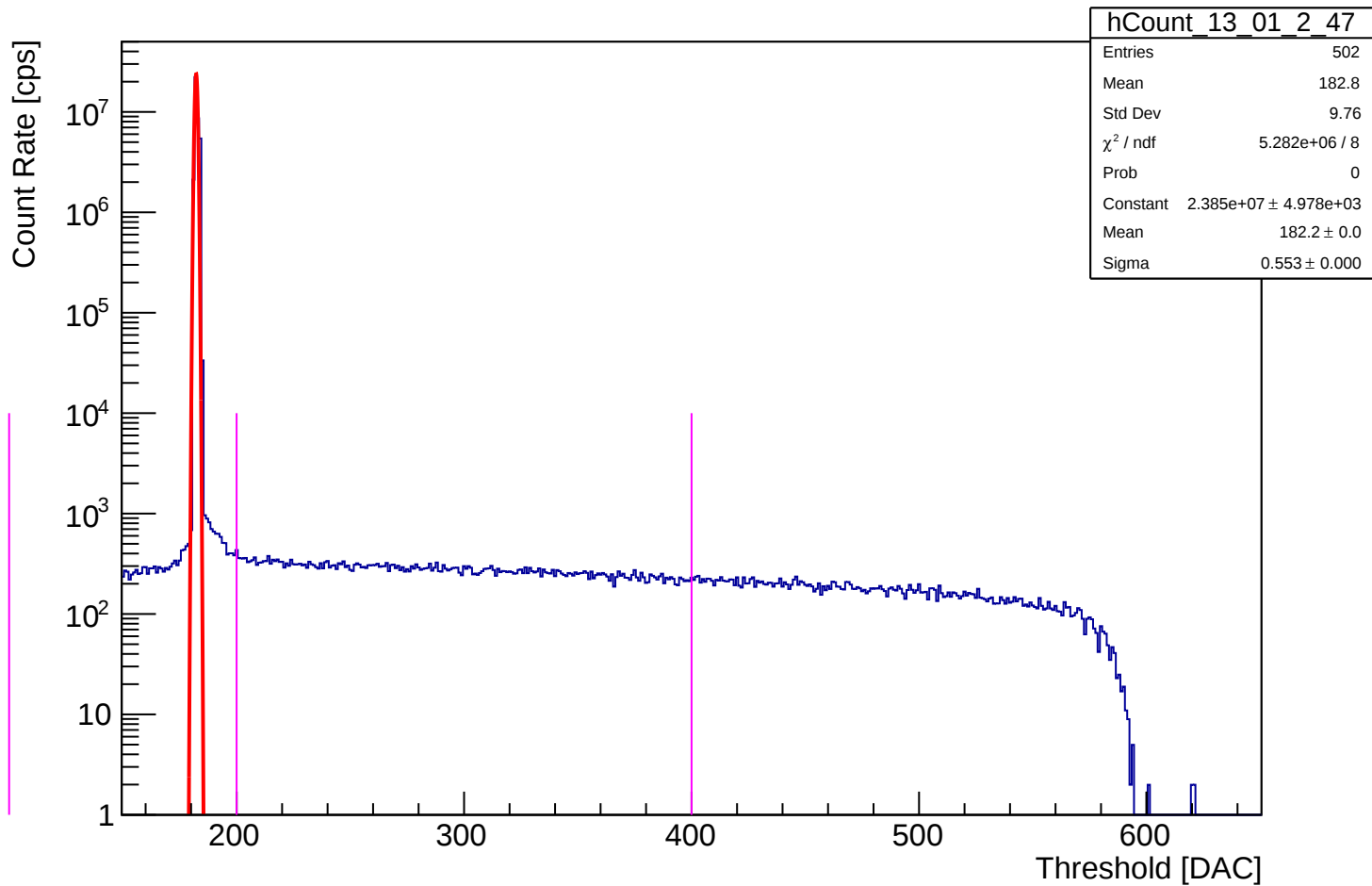
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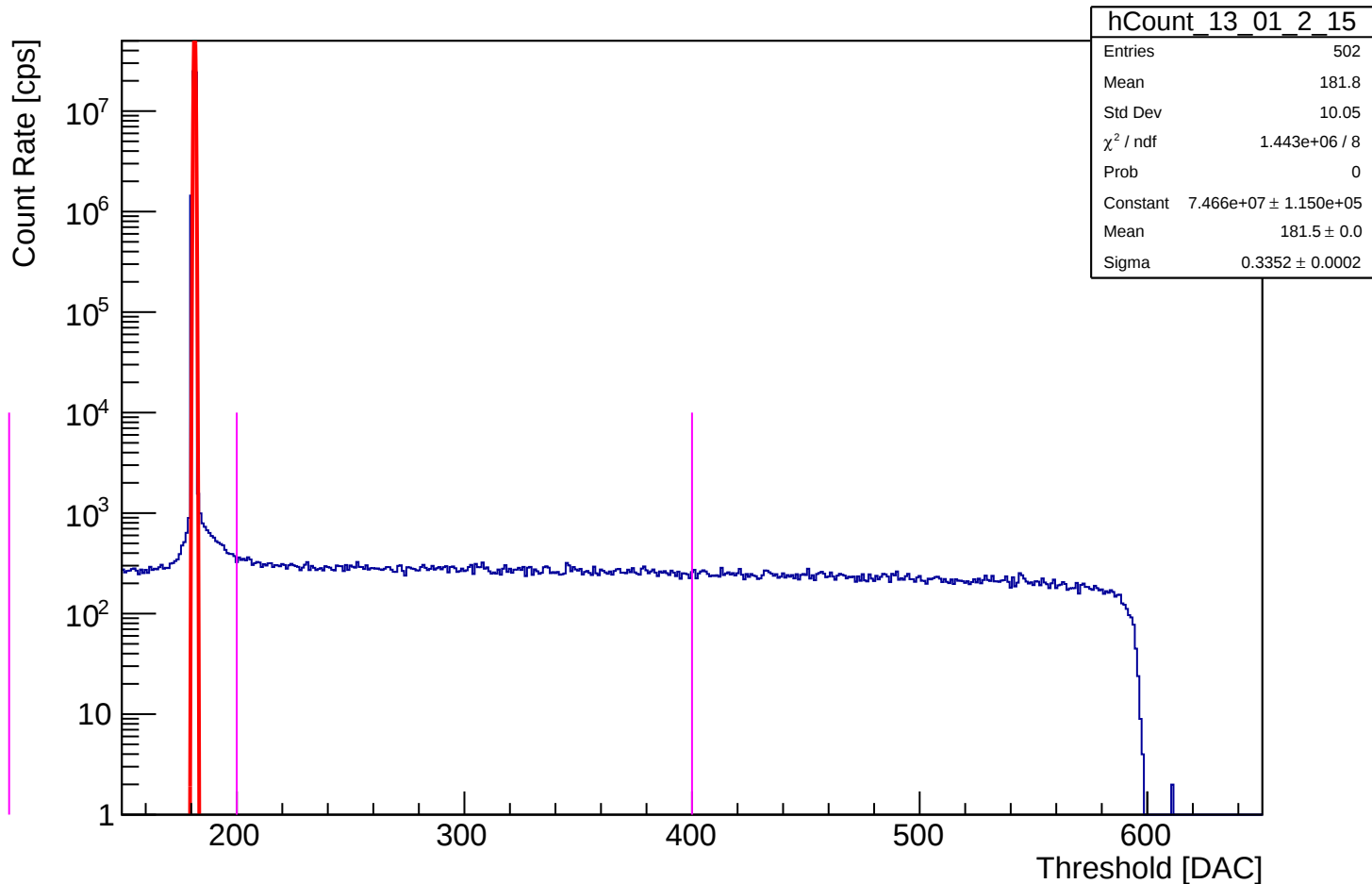
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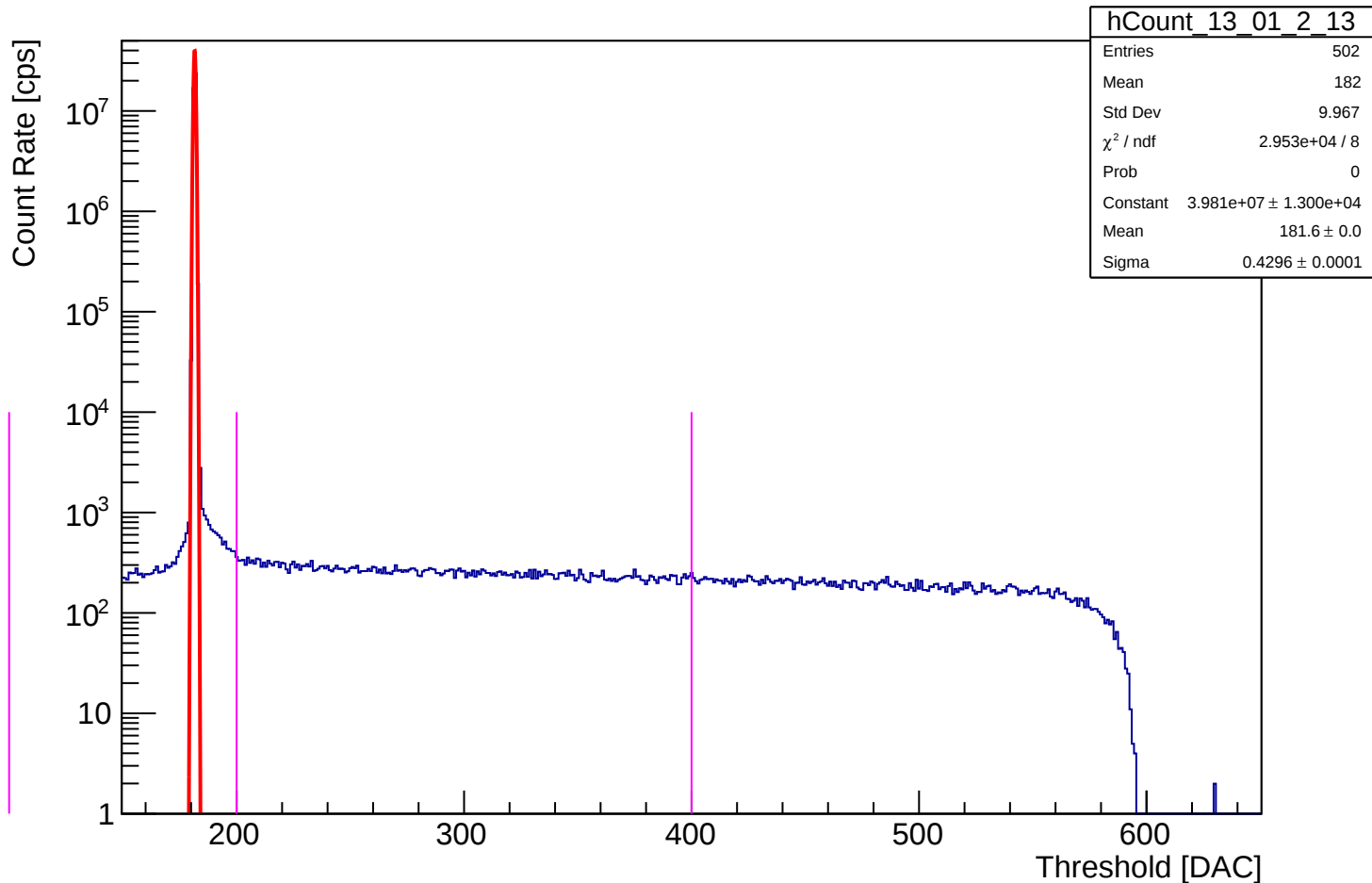
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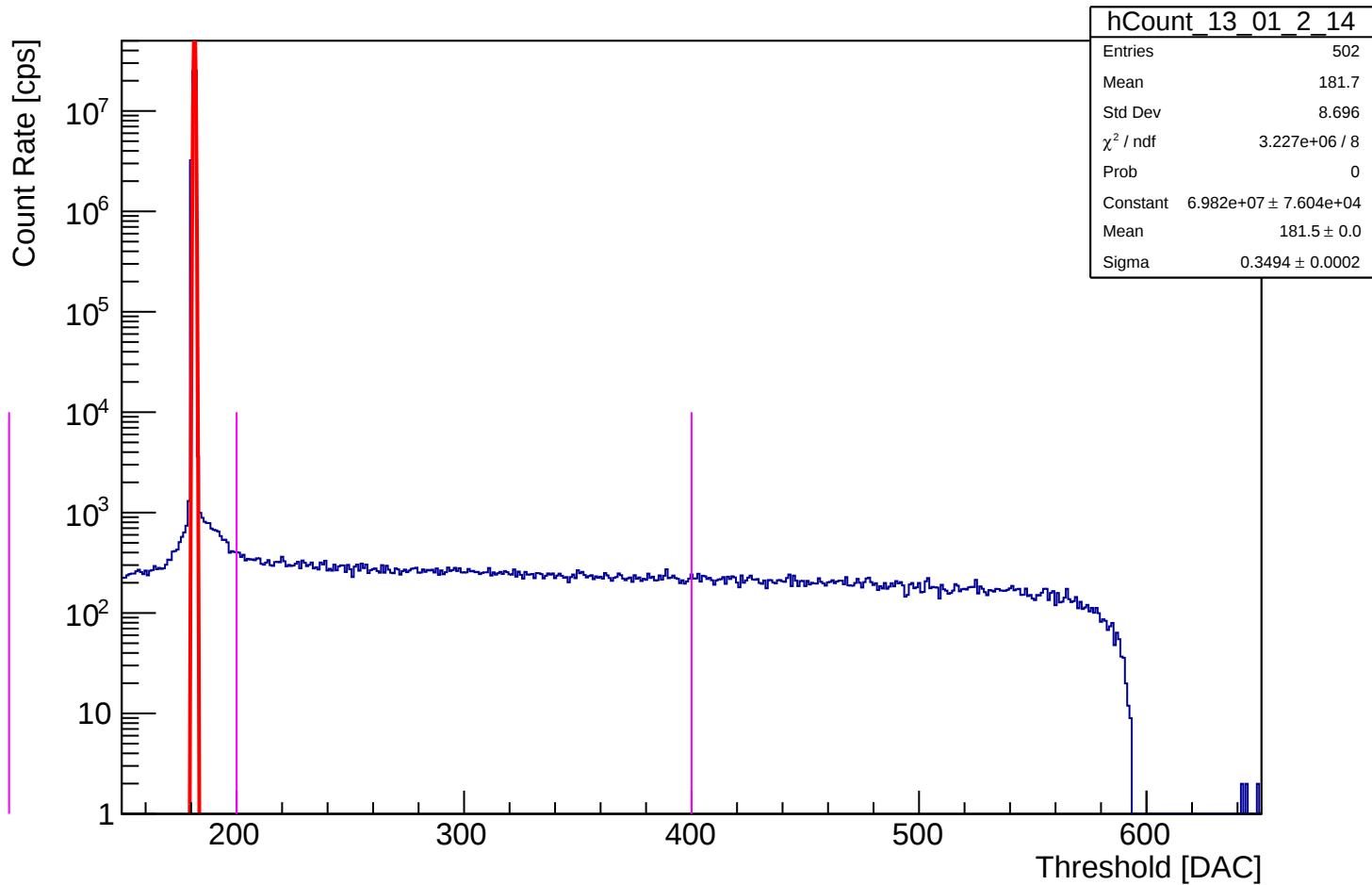
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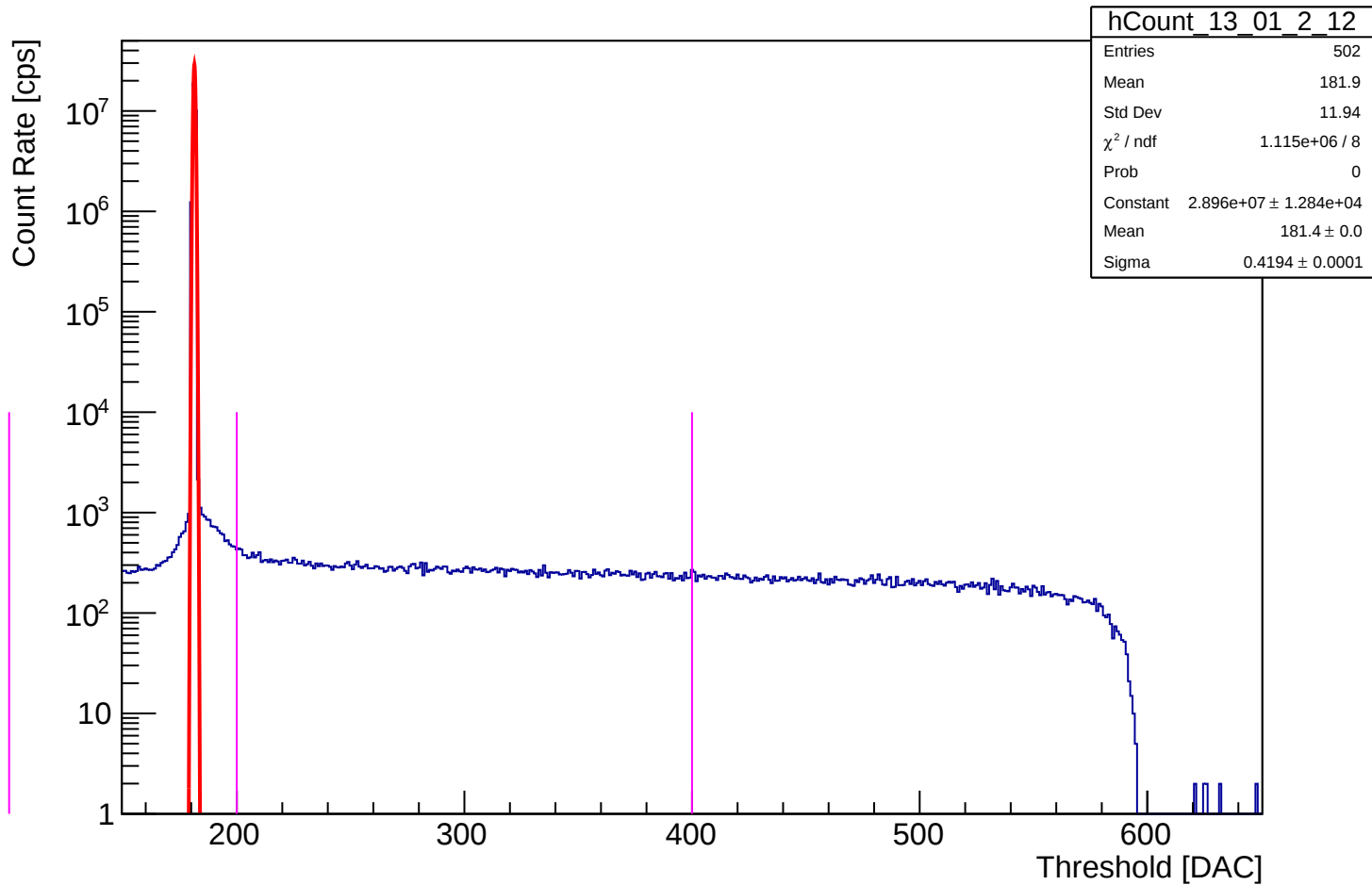
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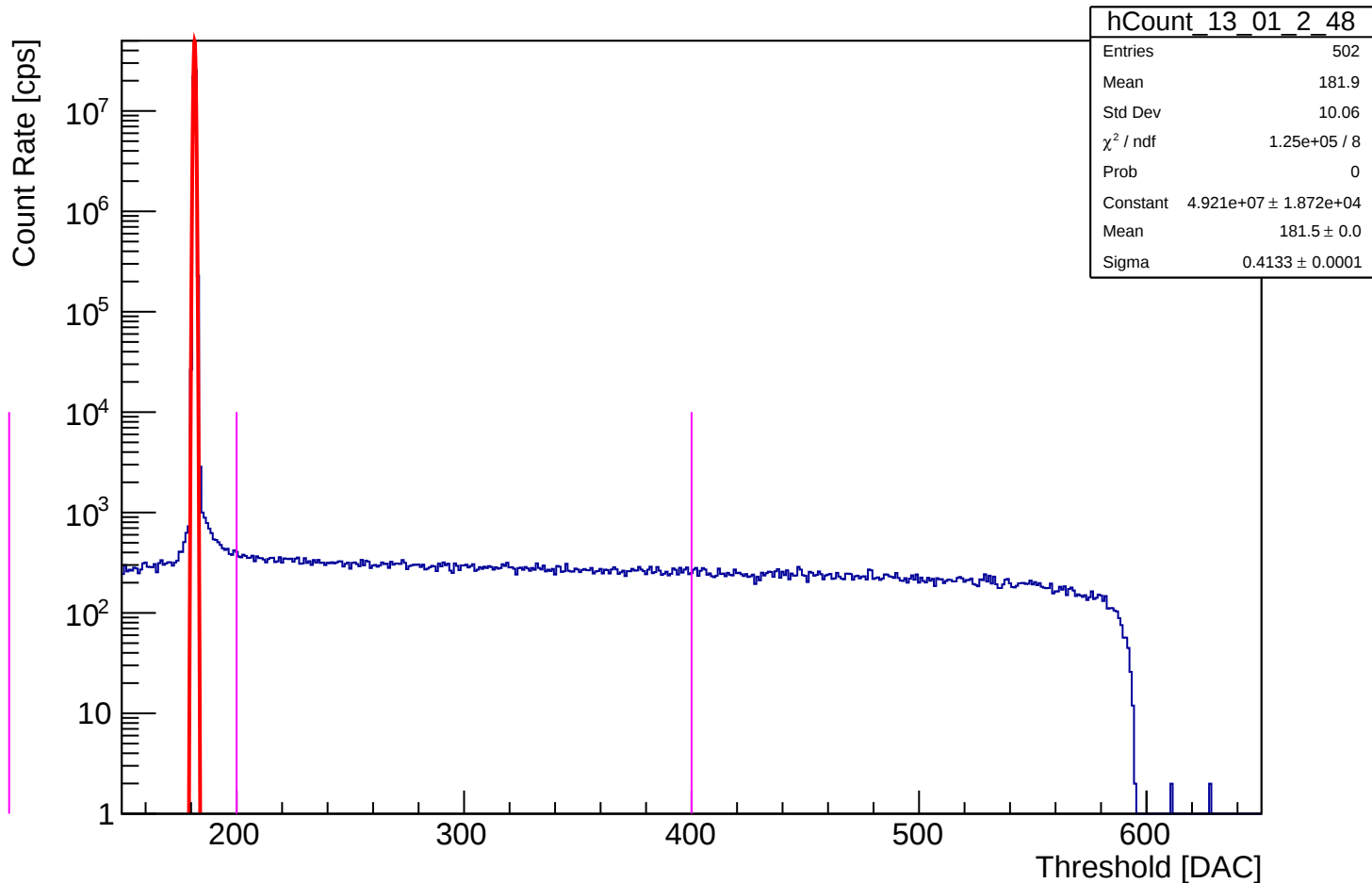
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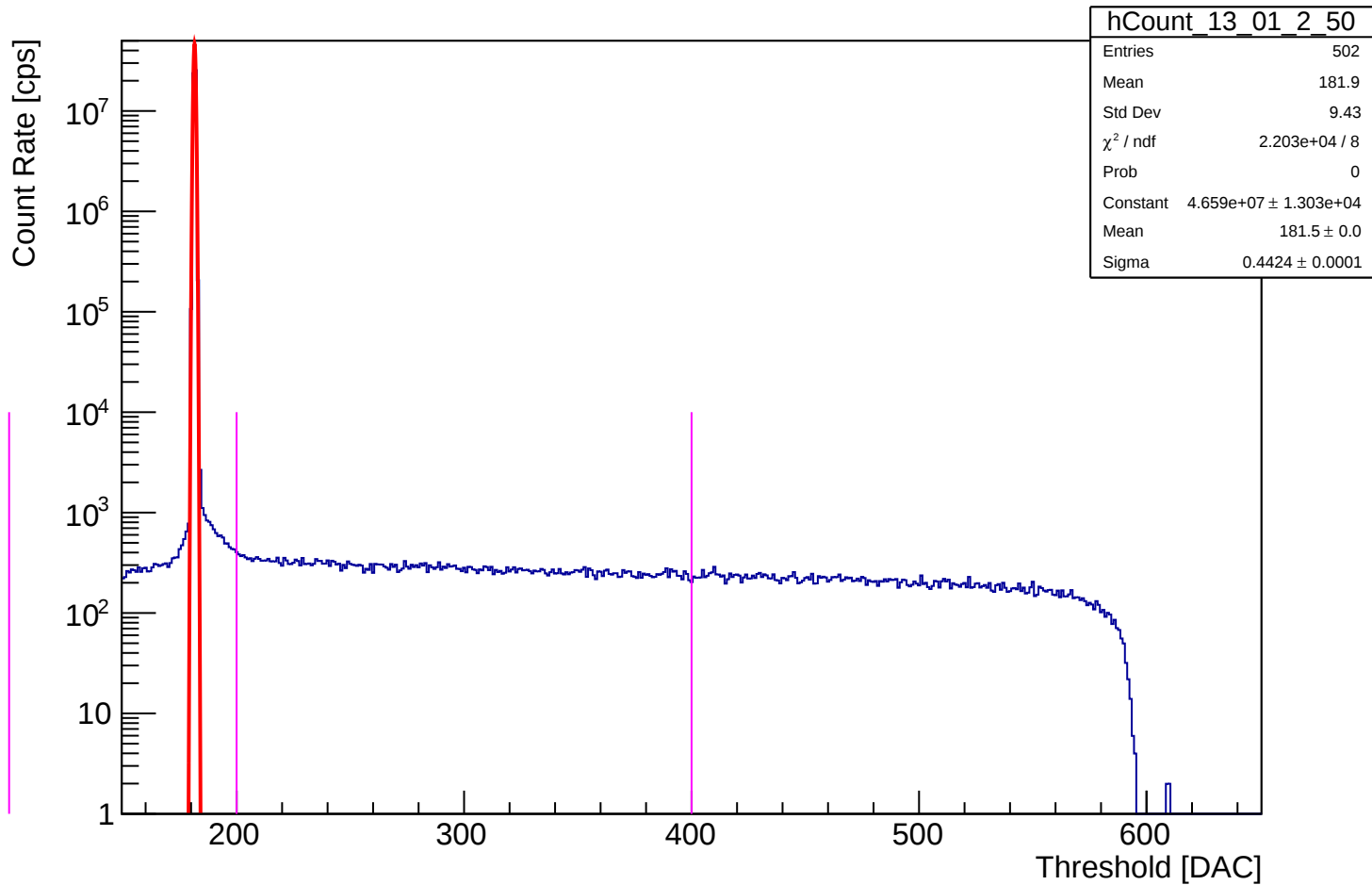
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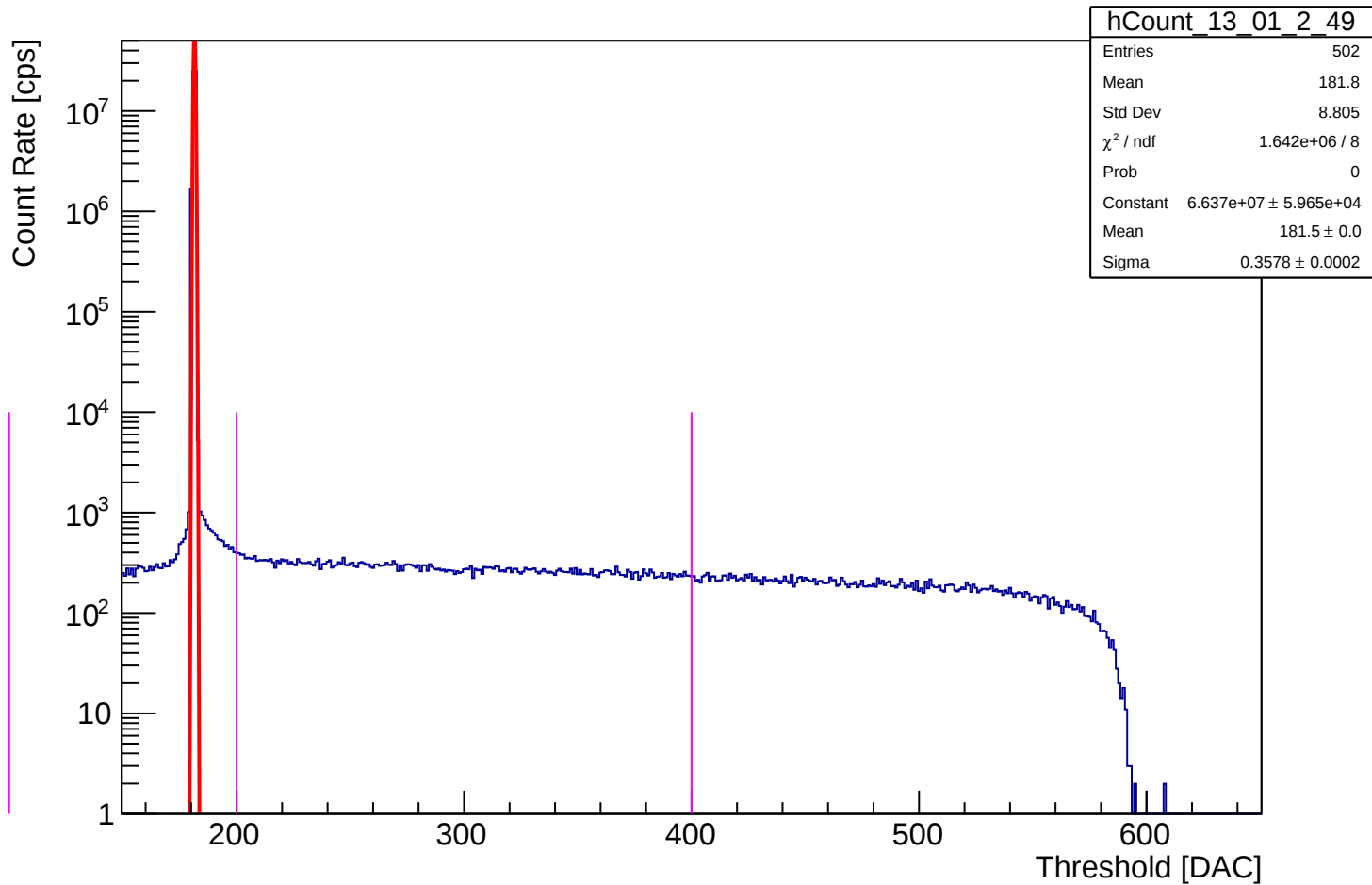
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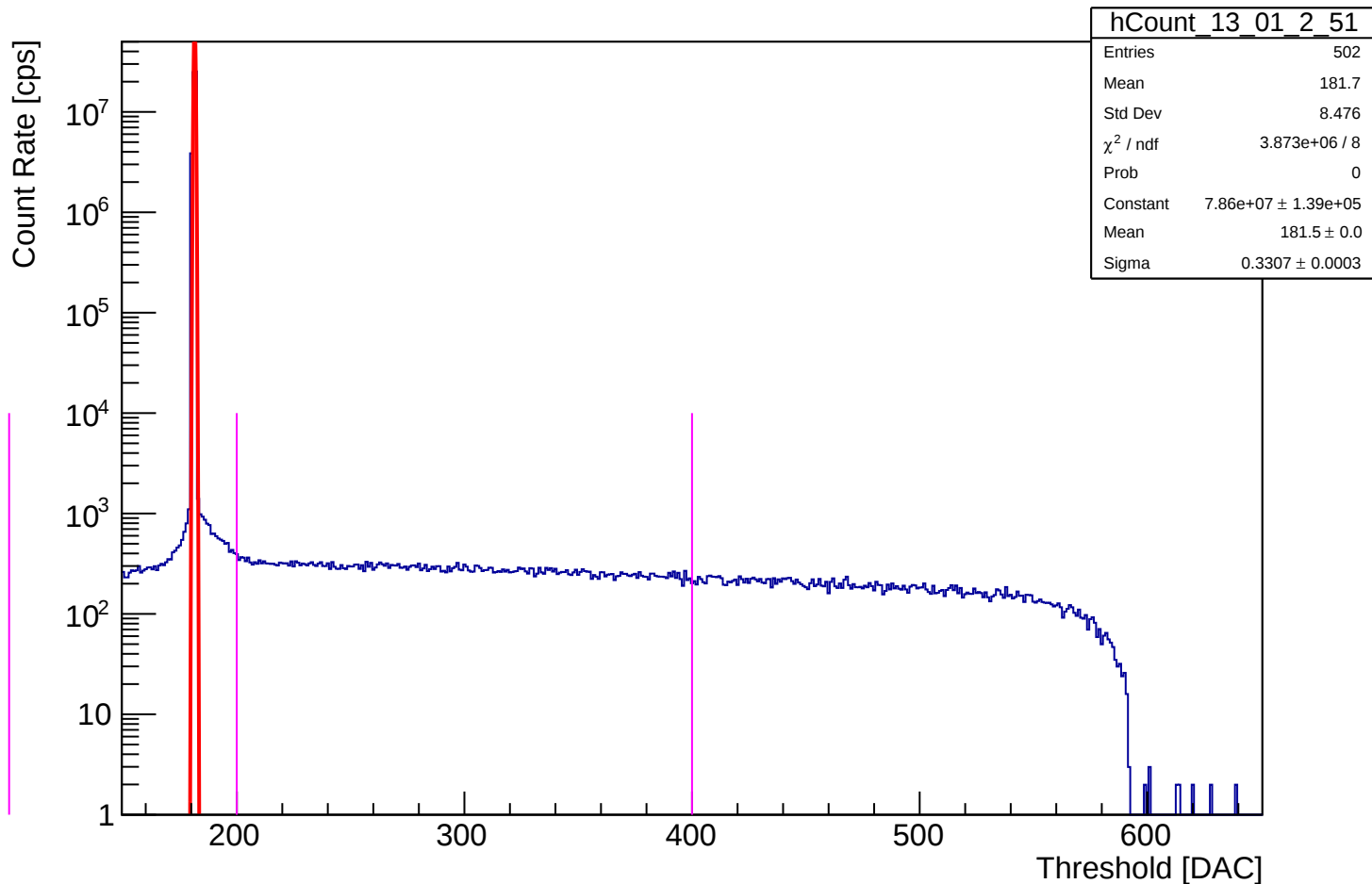
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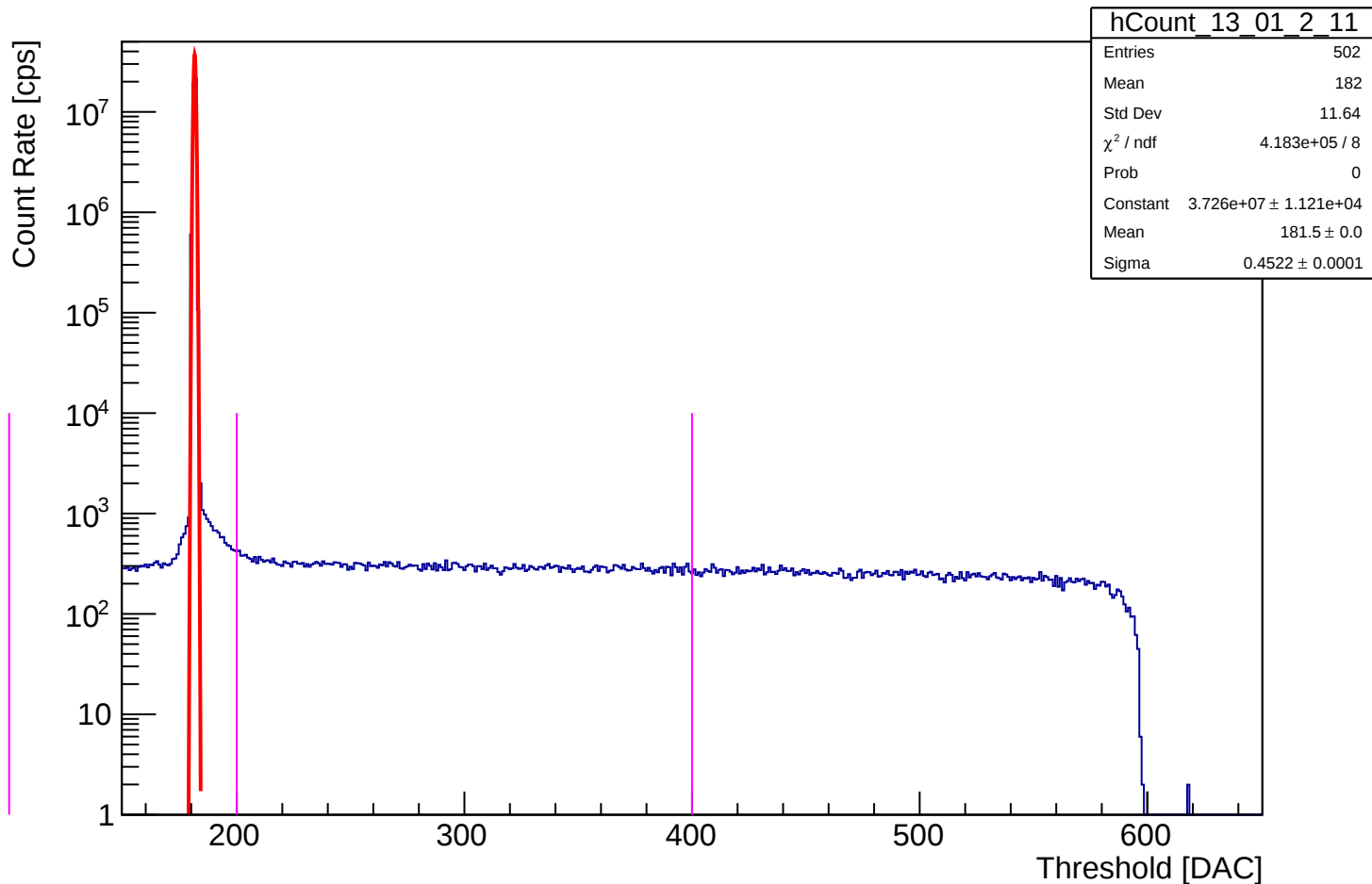
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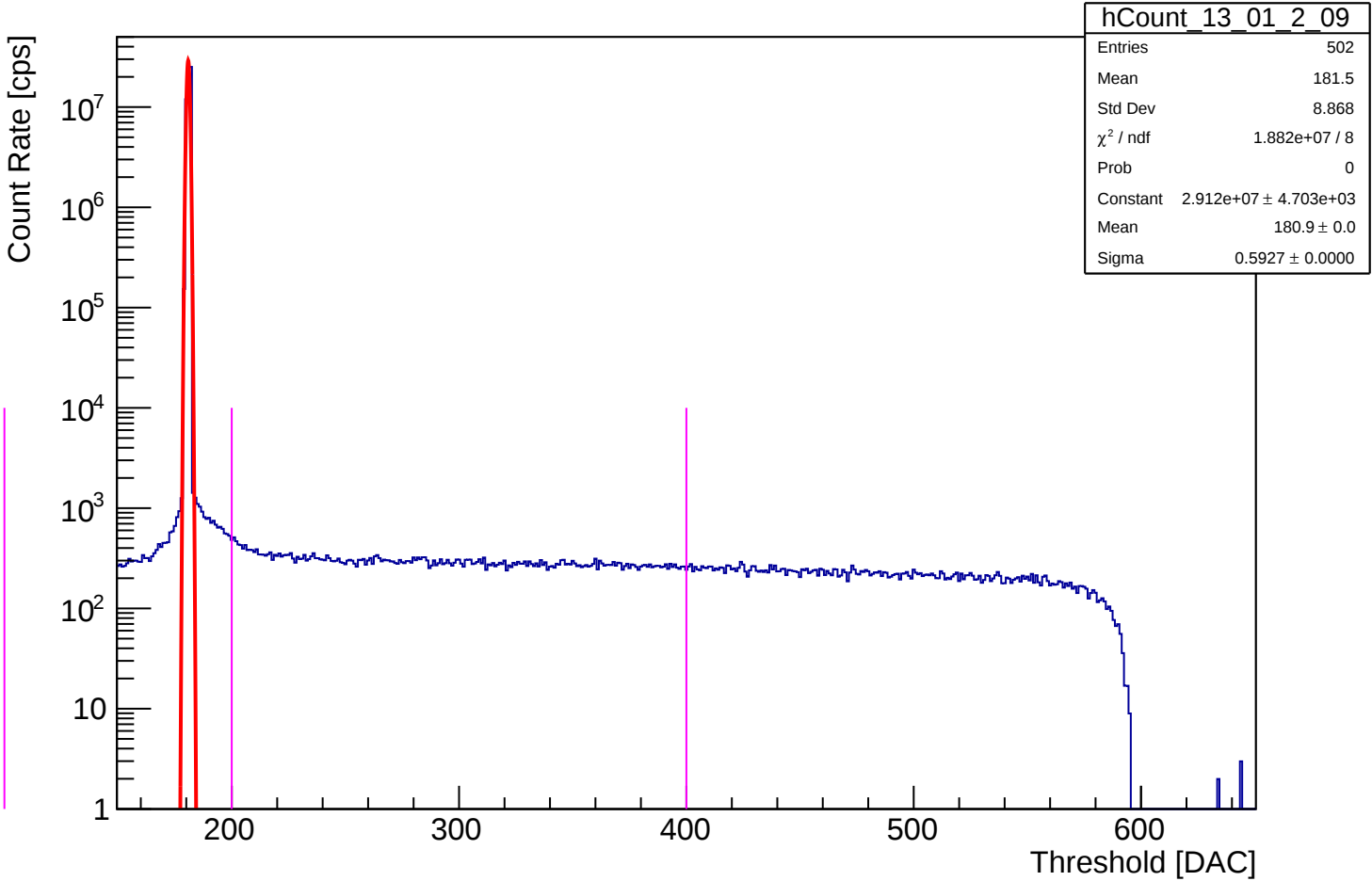


Row 1 Tile 1 Pmt 6 Pixel 40 Slot 13 Fiber 1 Asic 2 Channel 51

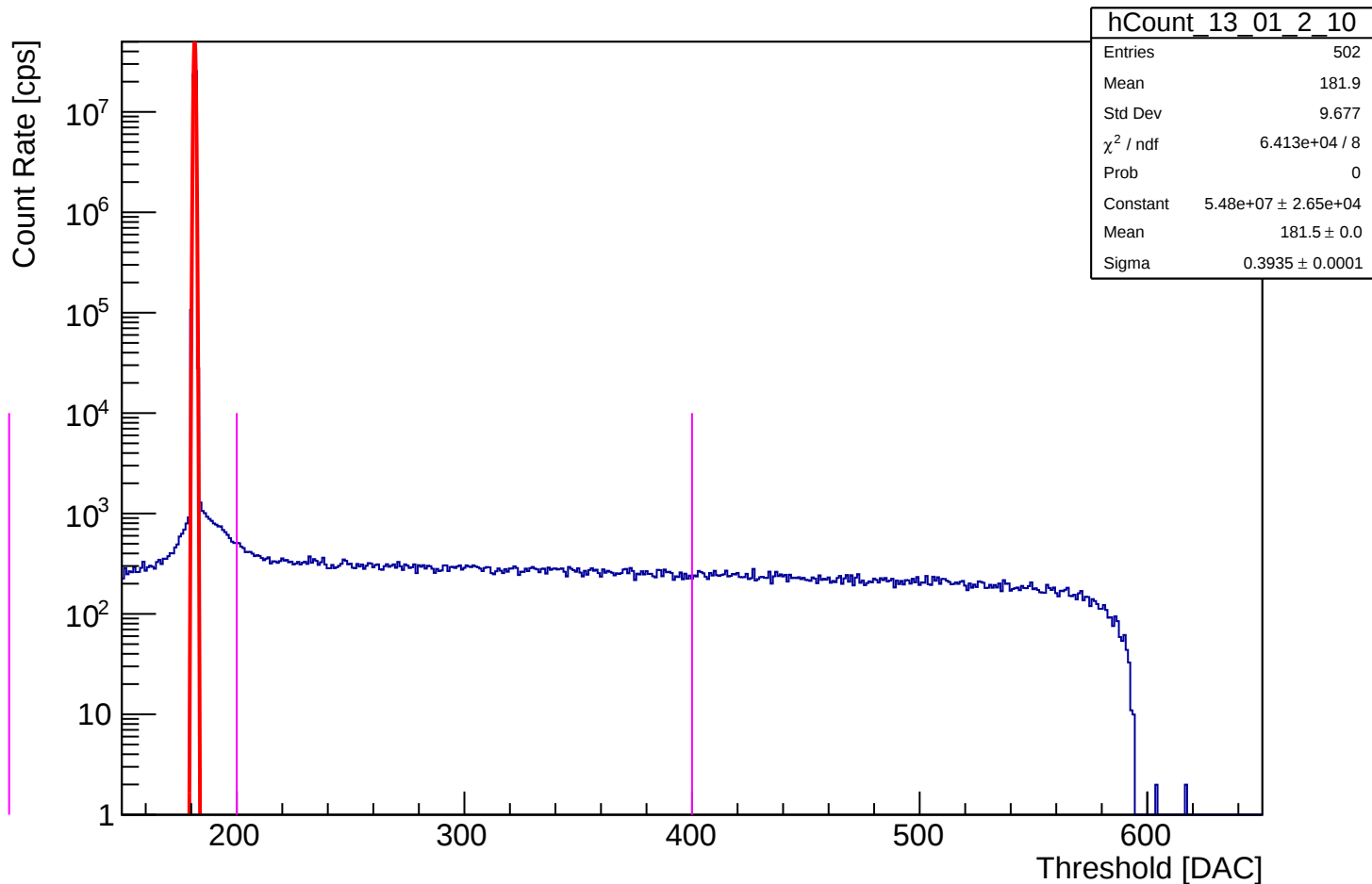


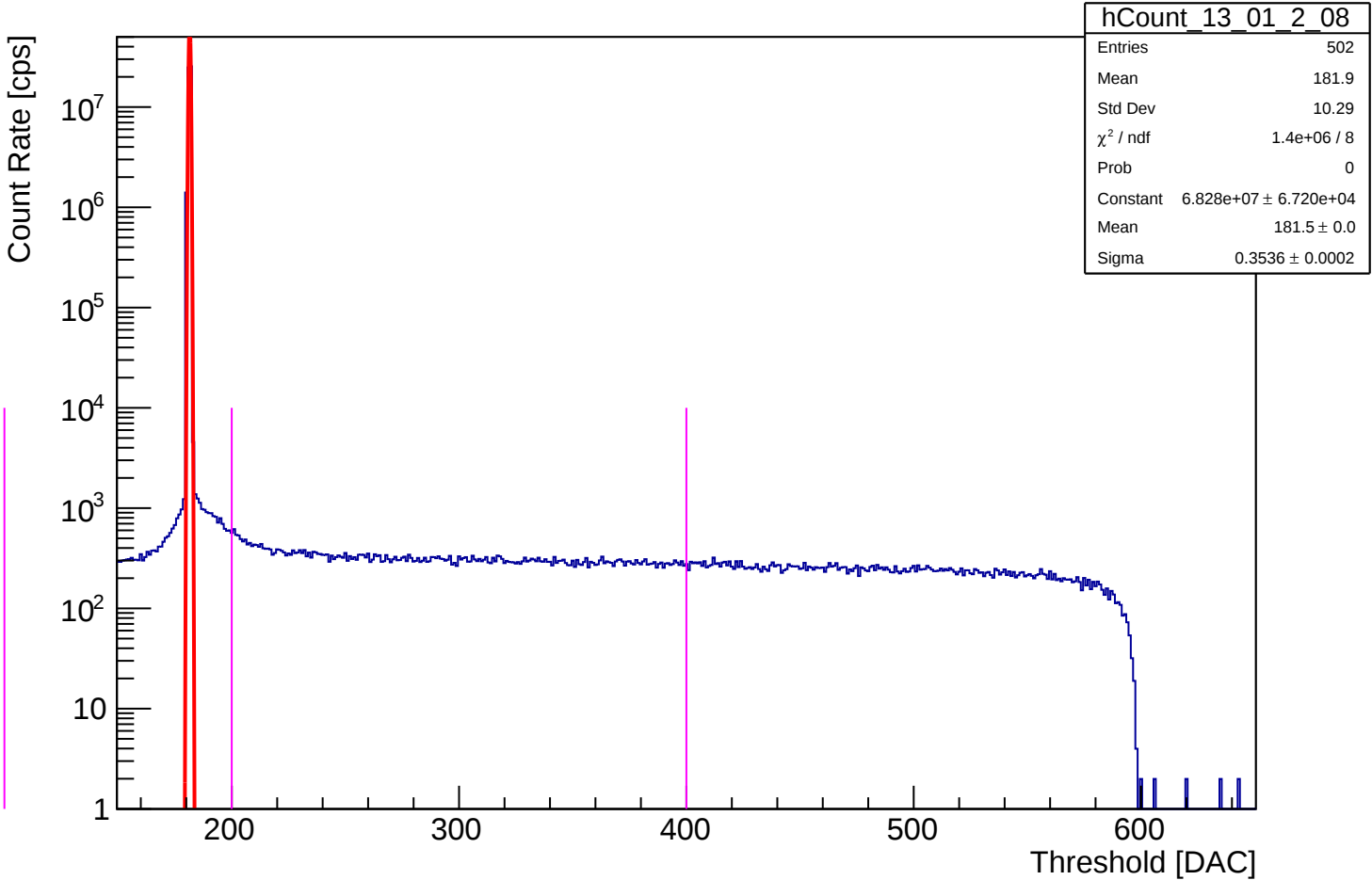
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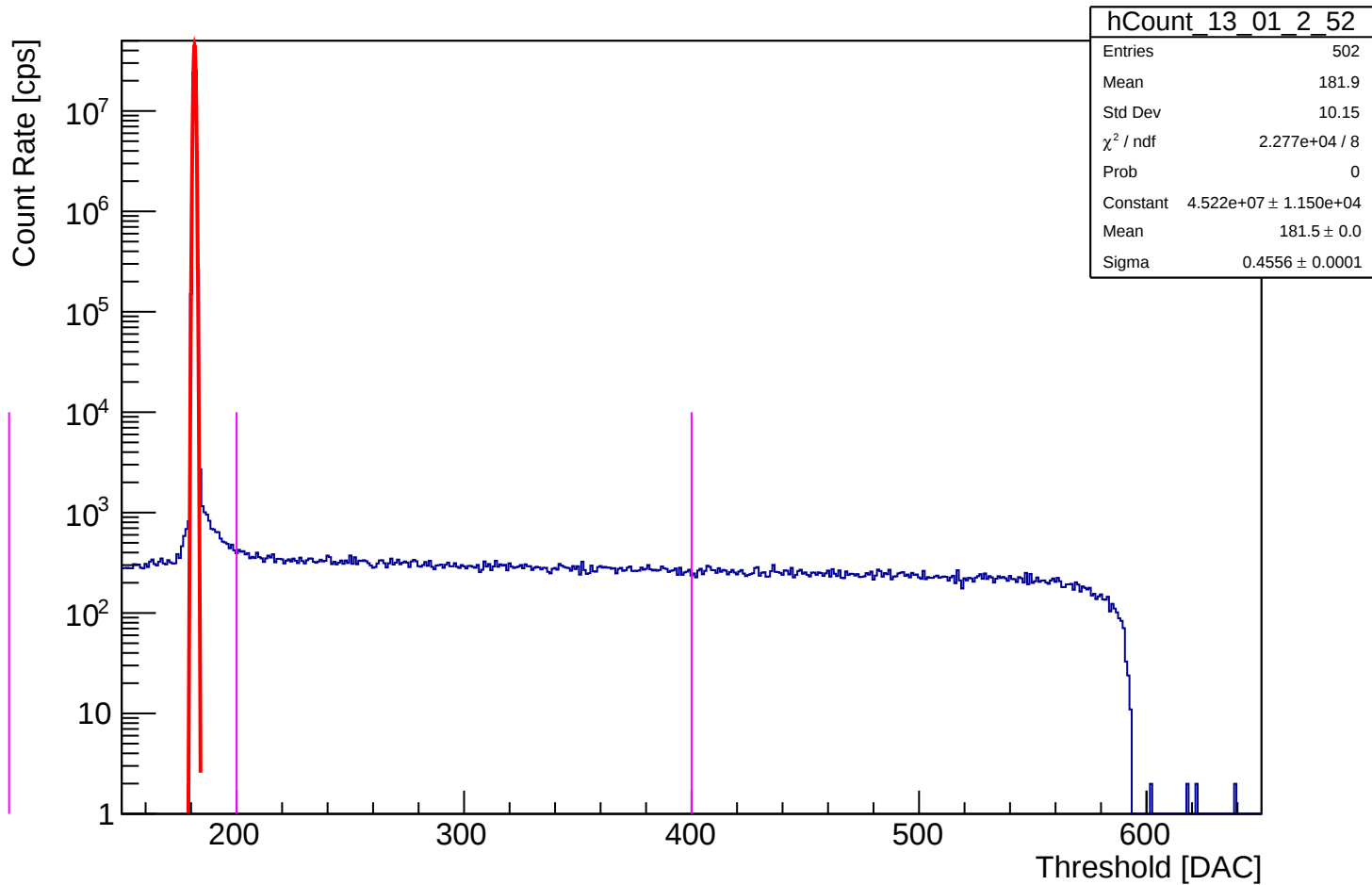


Row 1 Tile 1 Pmt 6 Pixel 43 Slot 13 Fiber 1 Asic 2 Channel 10

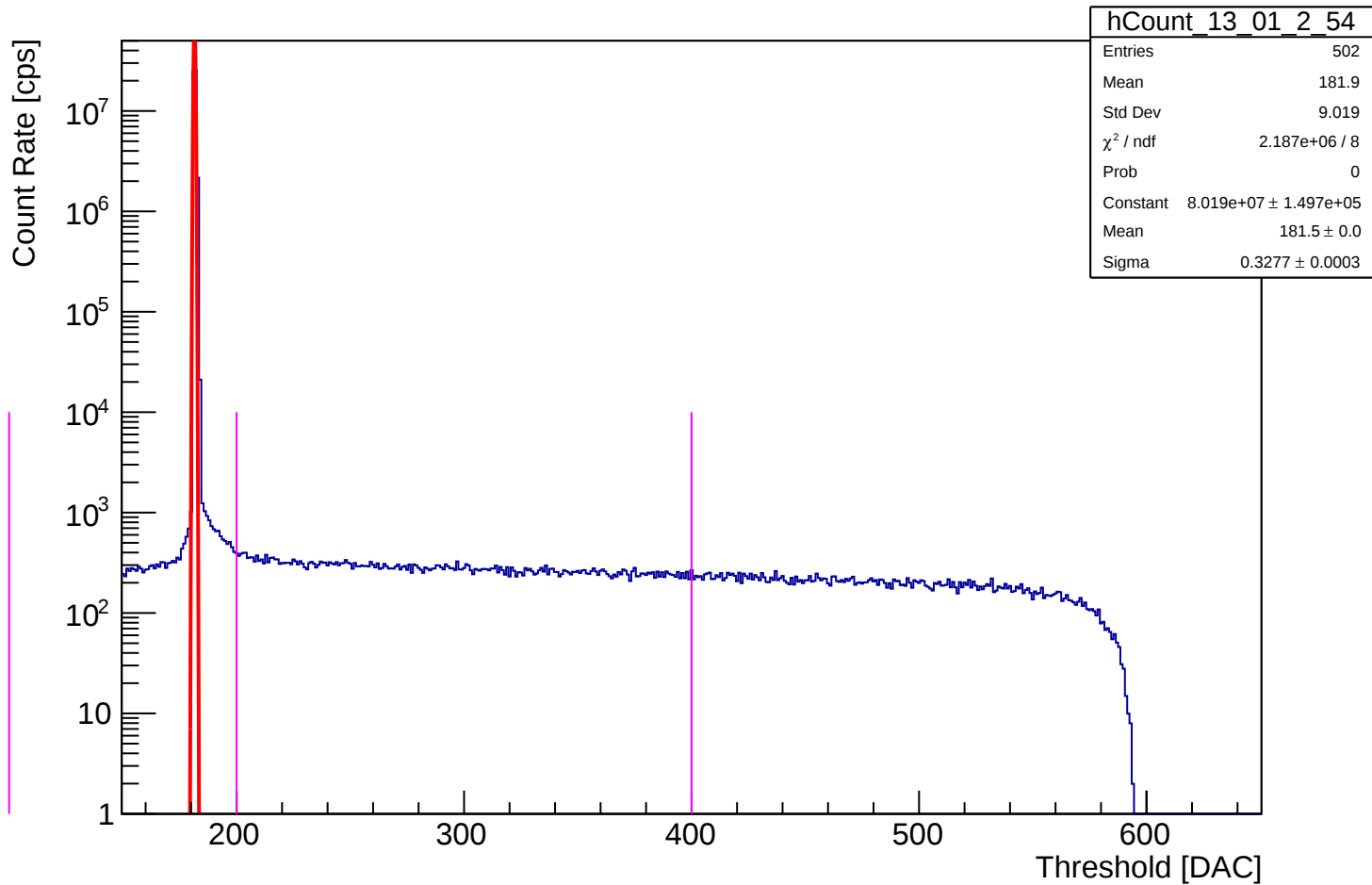




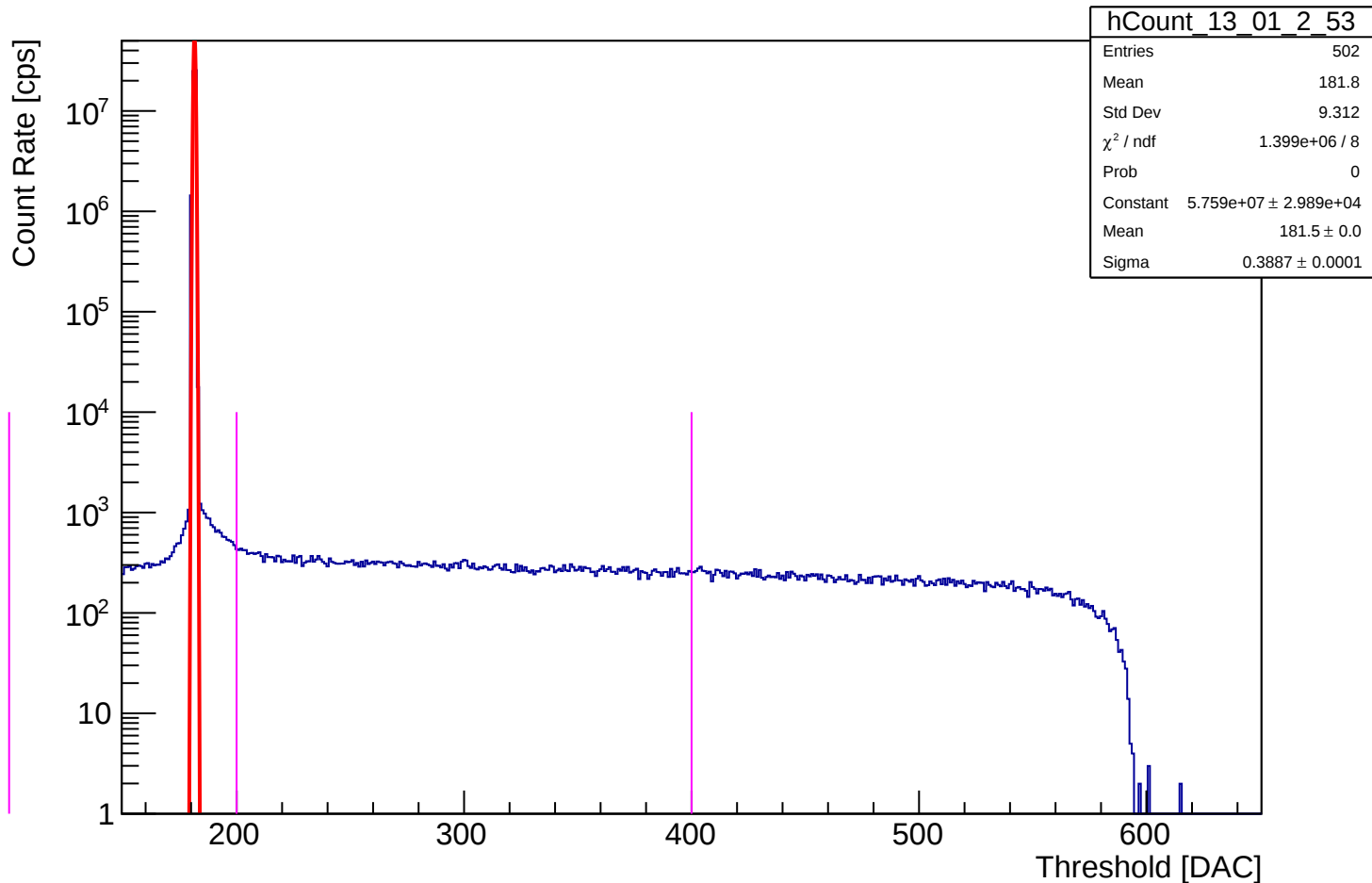
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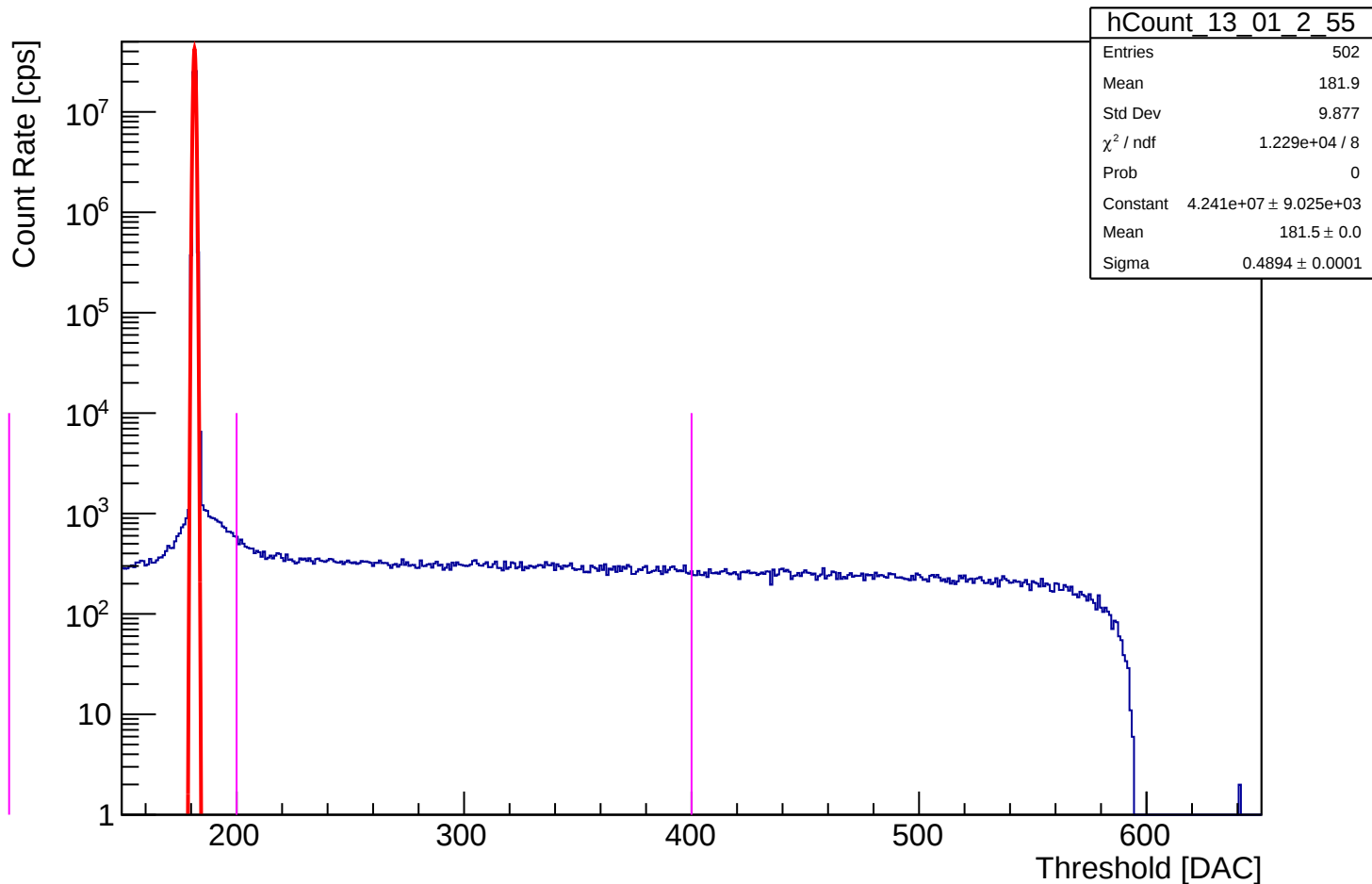
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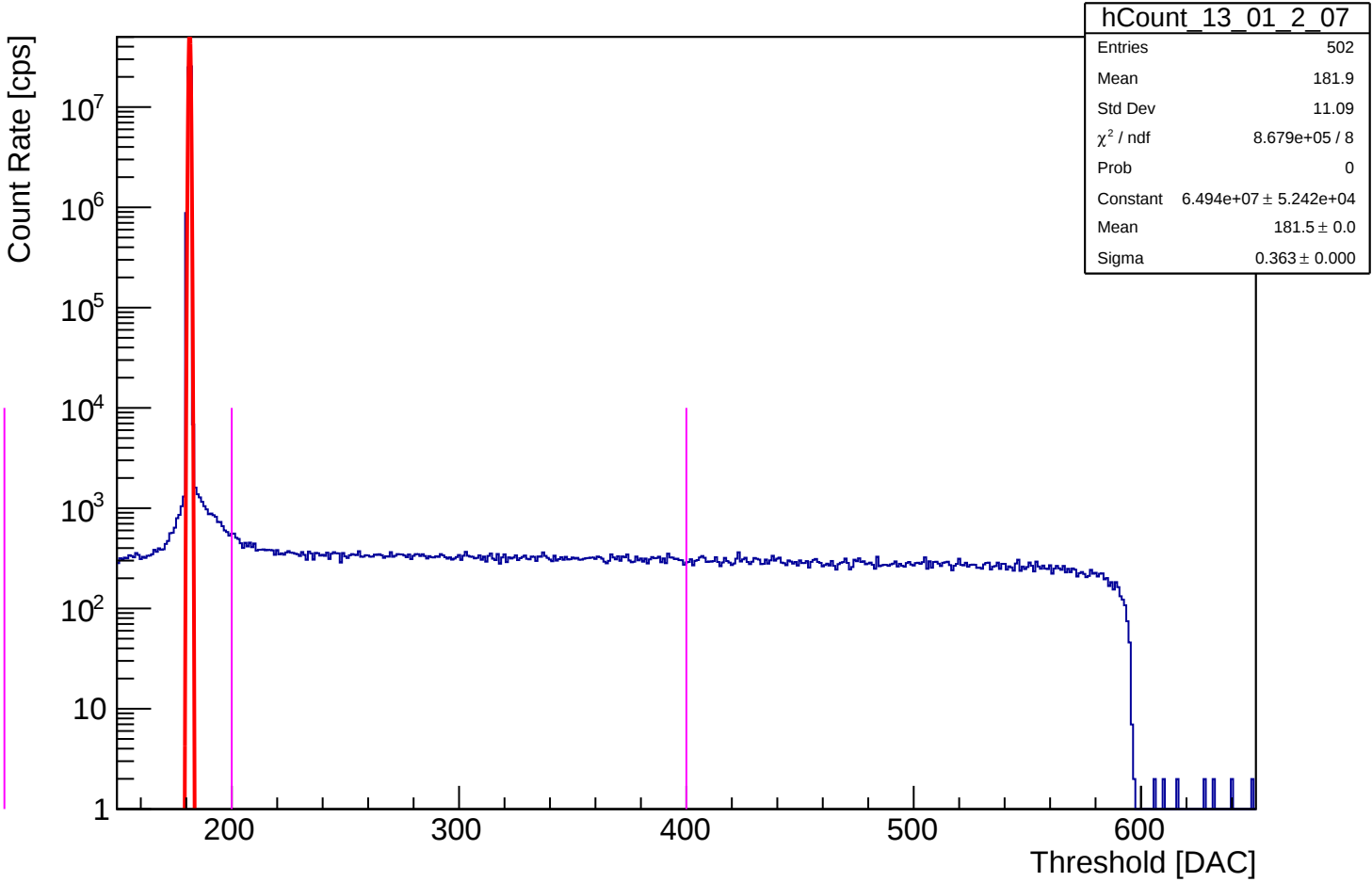


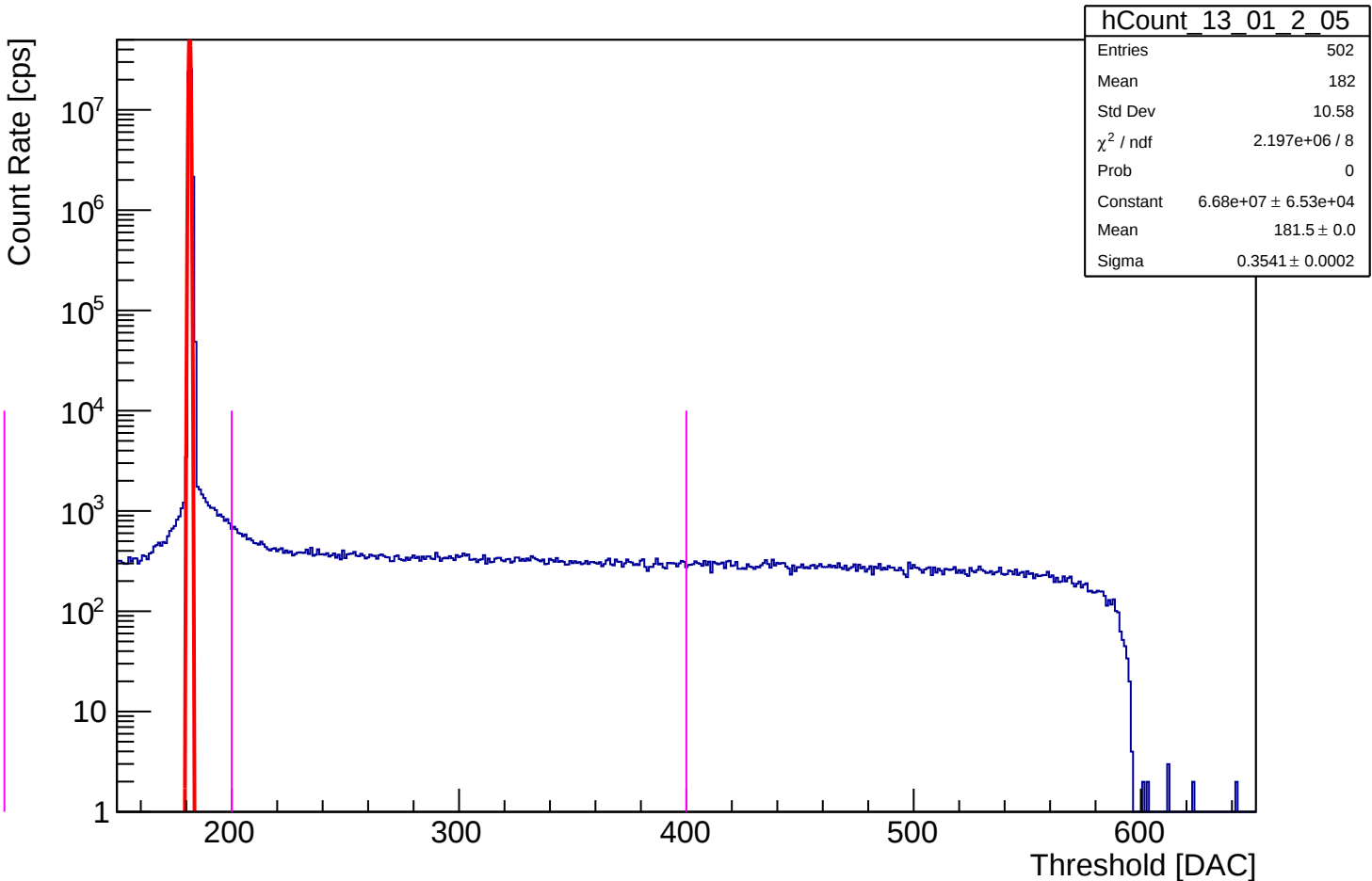
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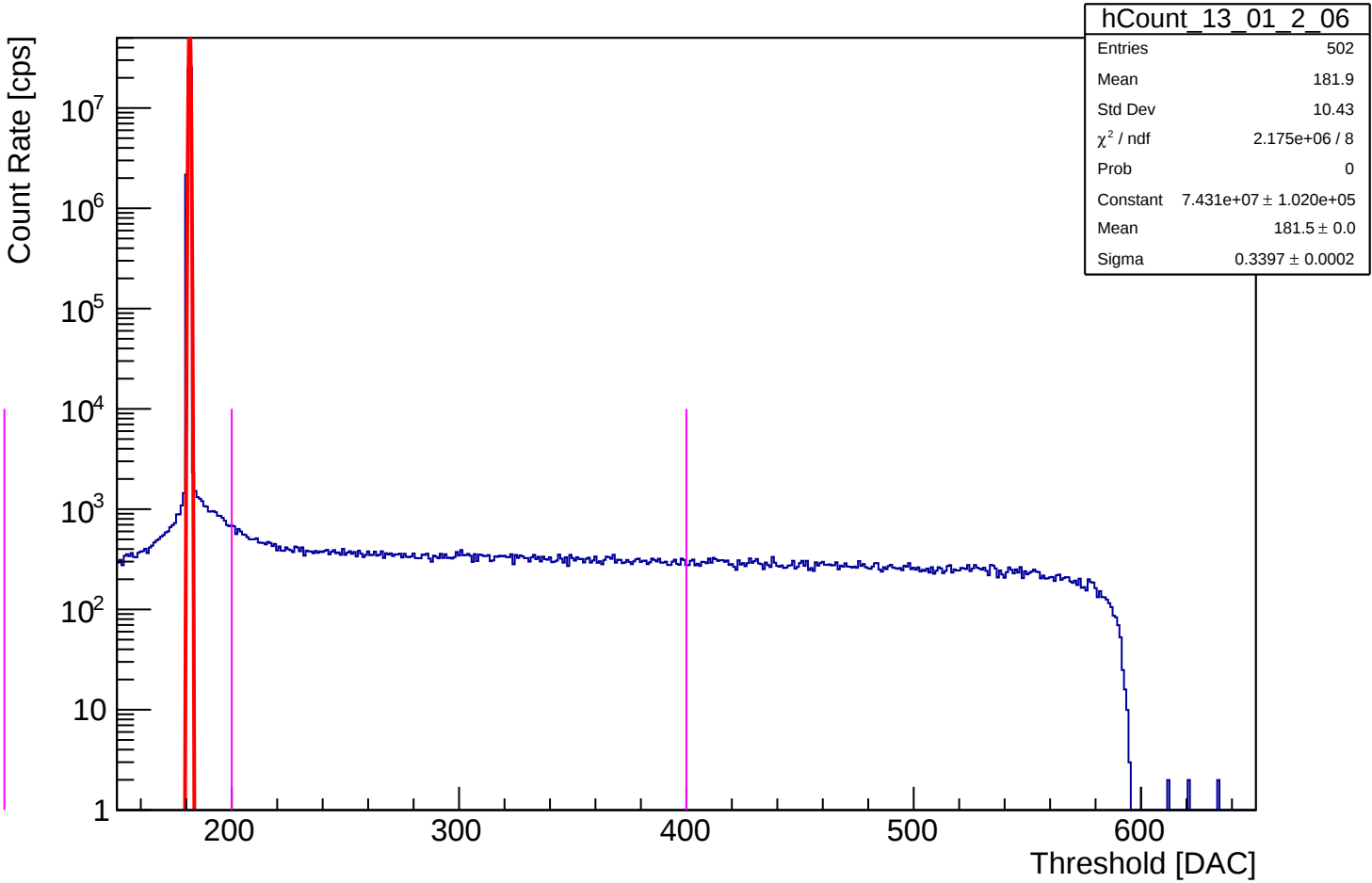


Row 1 Tile 1 Pmt 6 Pixel 48 Slot 13 Fiber 1 Asic 2 Channel 55

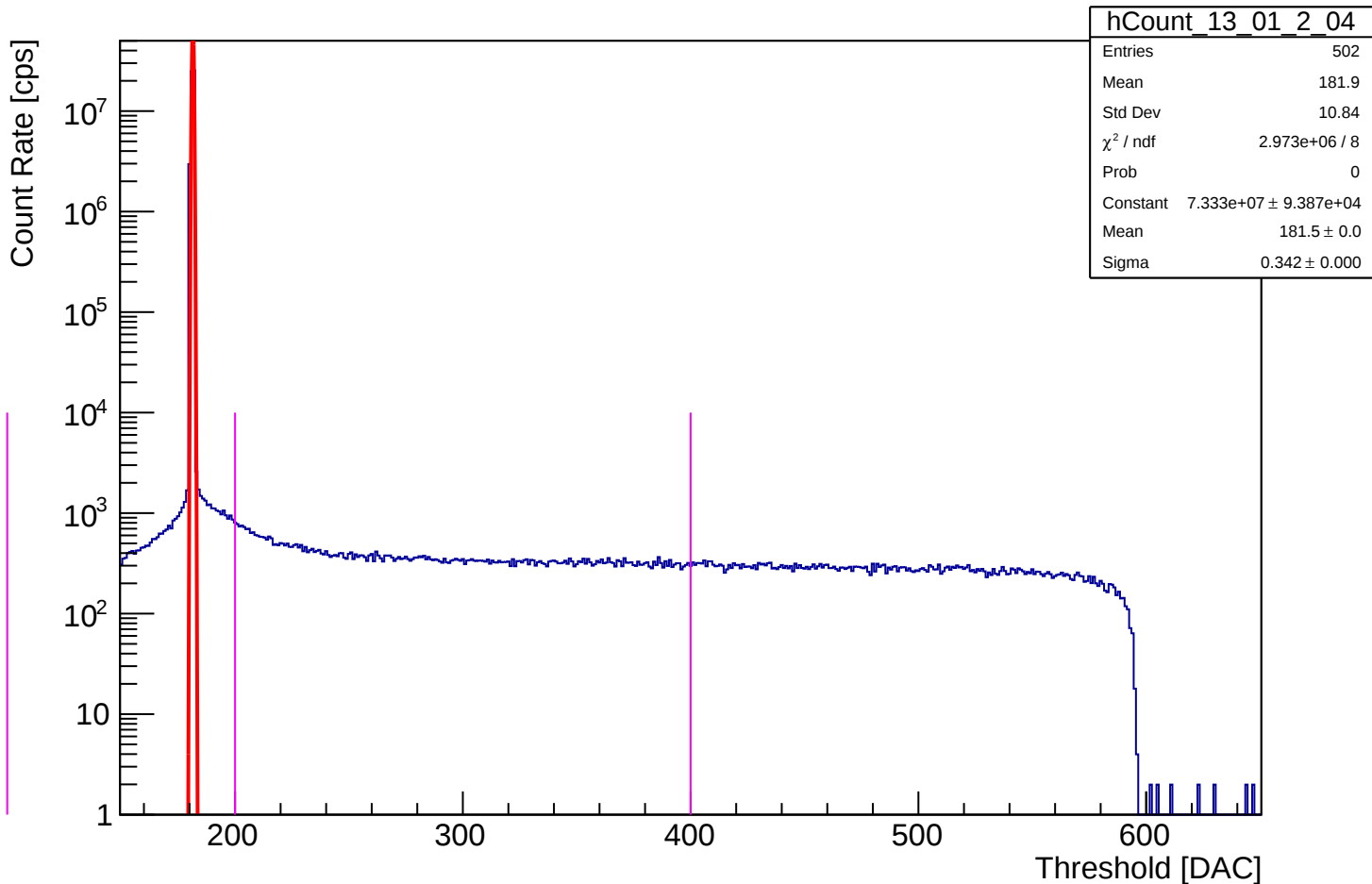




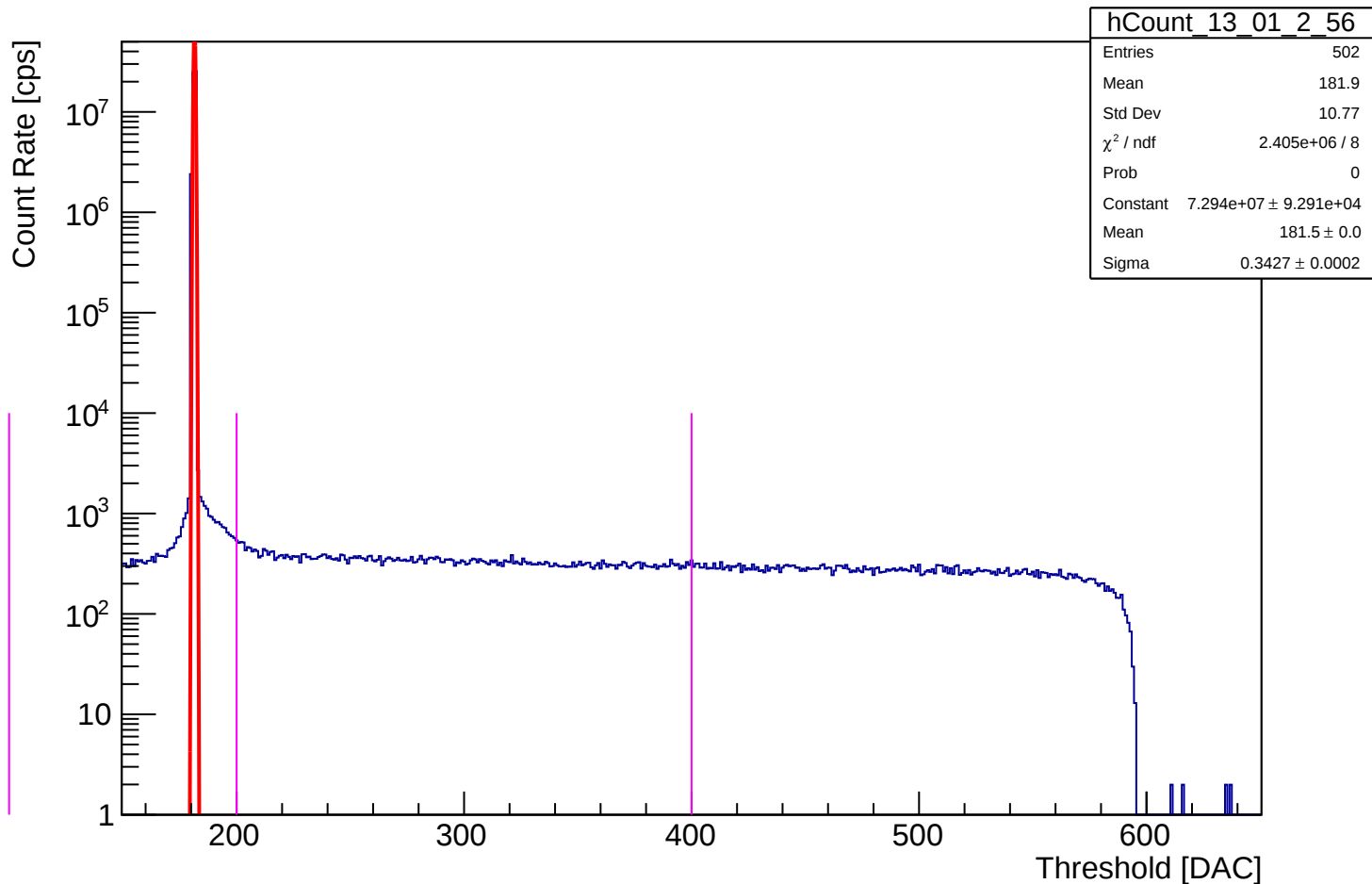




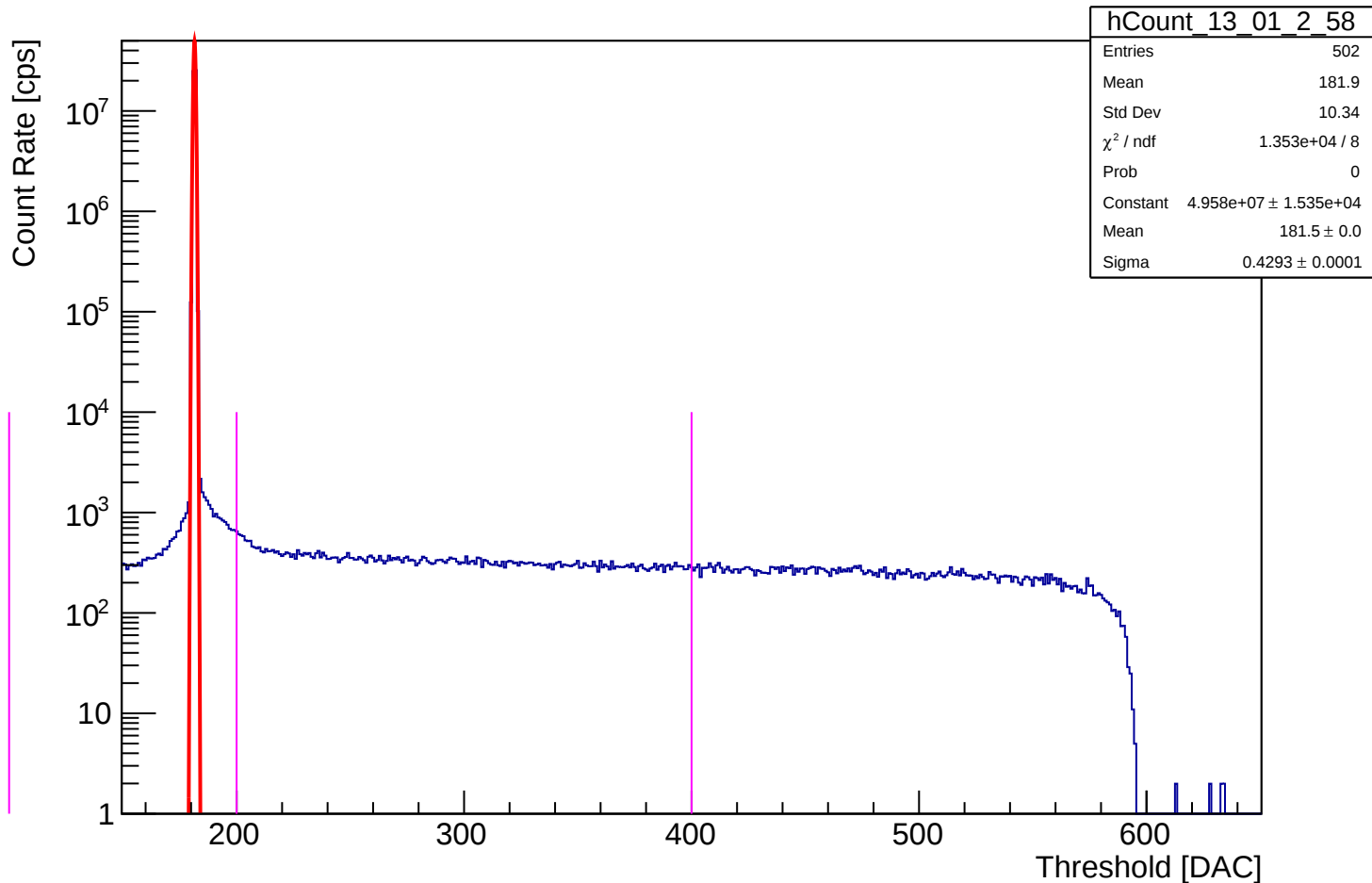
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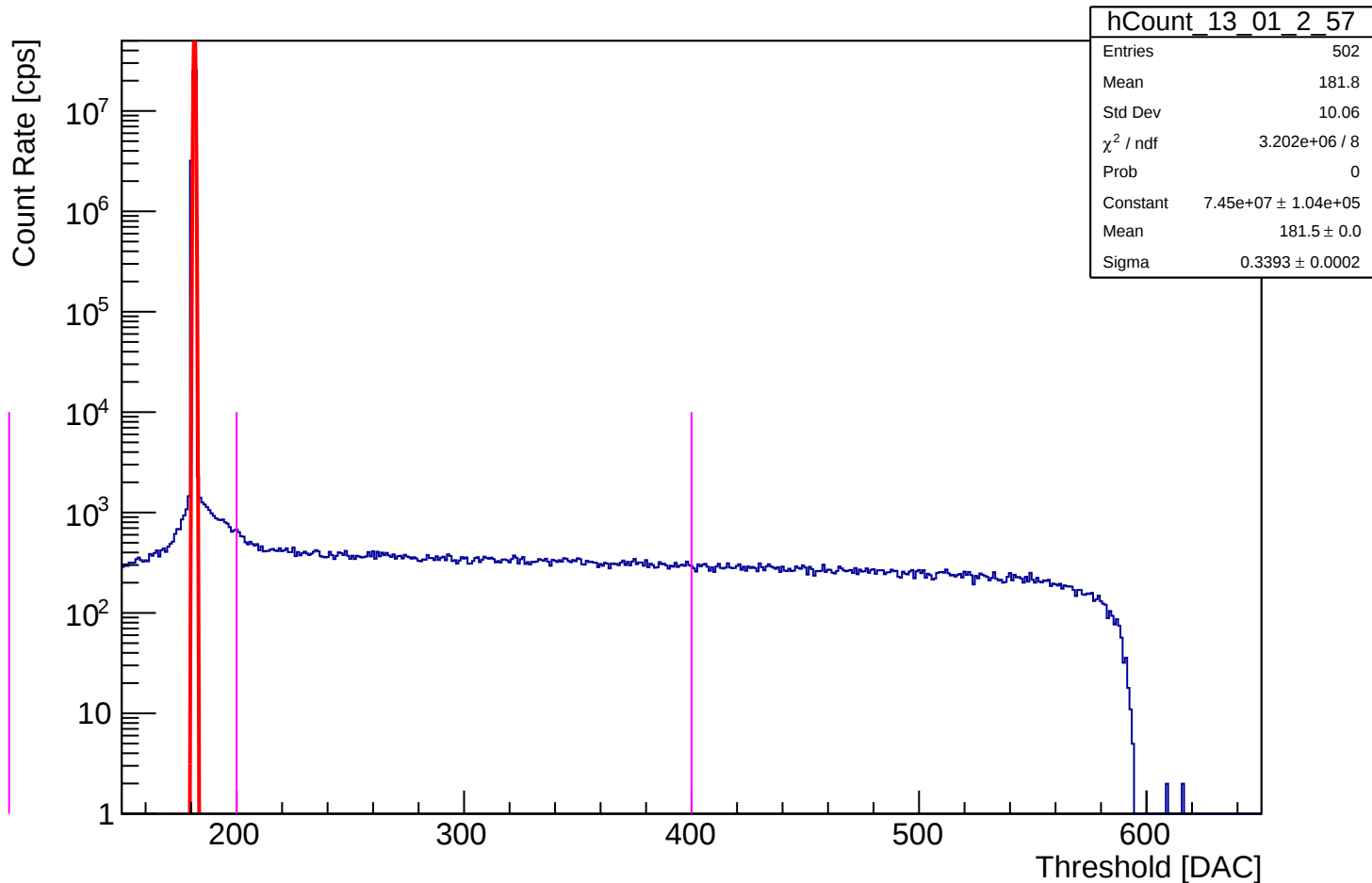
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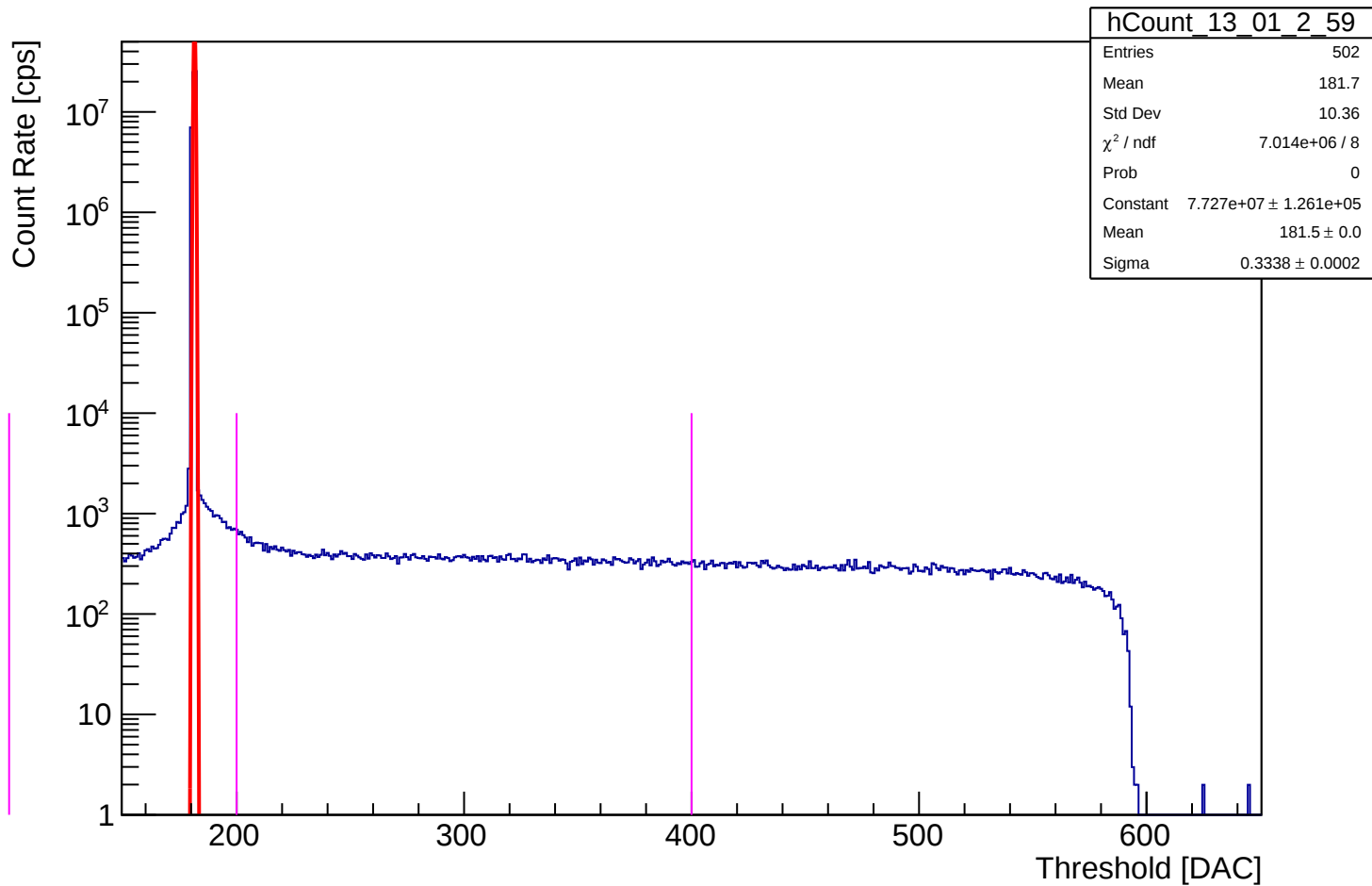
Row 1 Tile 1 Pmt 6 Pixel 54 Slot 13 Fiber 1 Asic 2 Channel 58

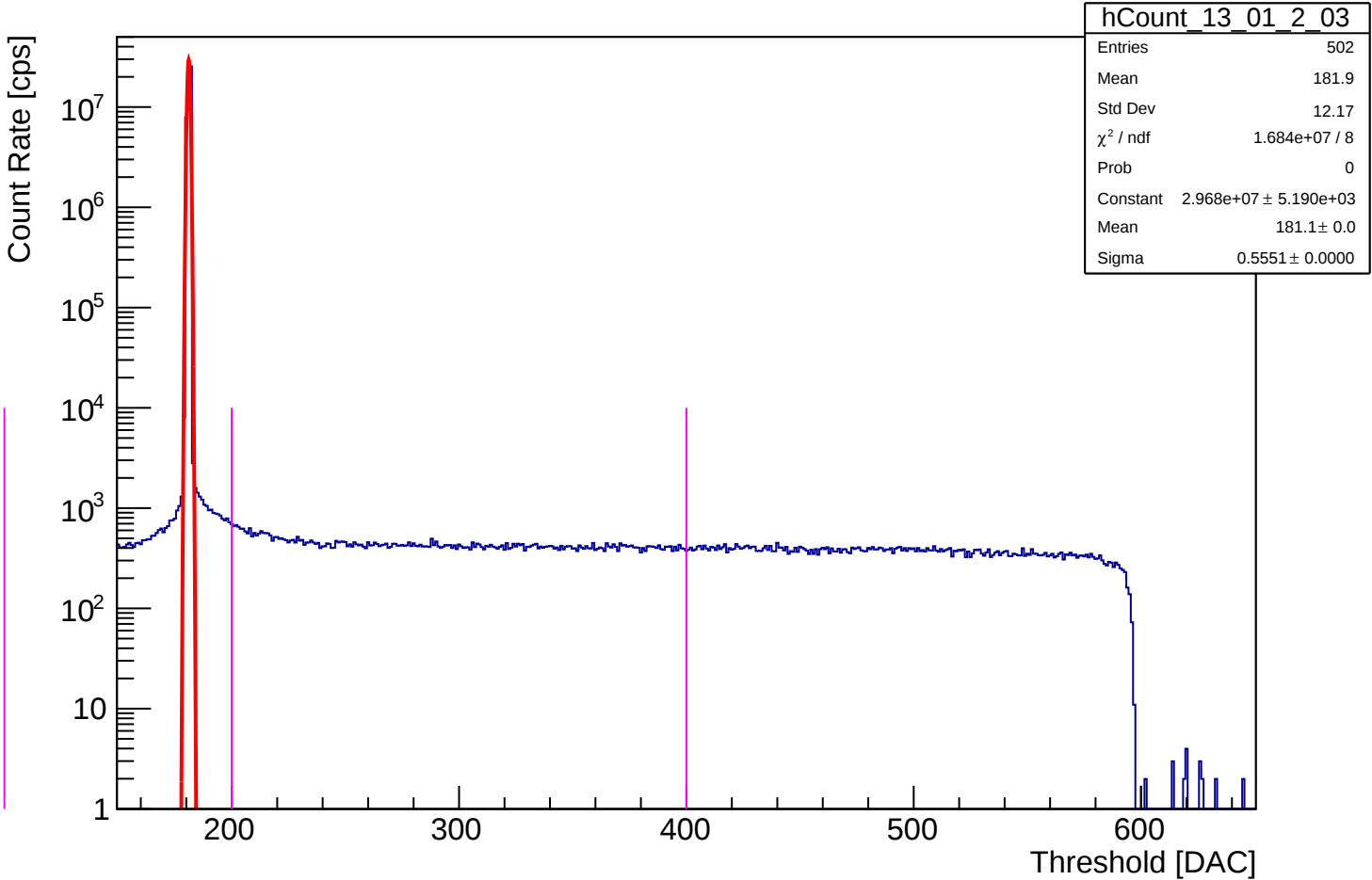


Row 1 Tile 1 Pmt 6 Pixel 55 Slot 13 Fiber 1 Asic 2 Channel 57

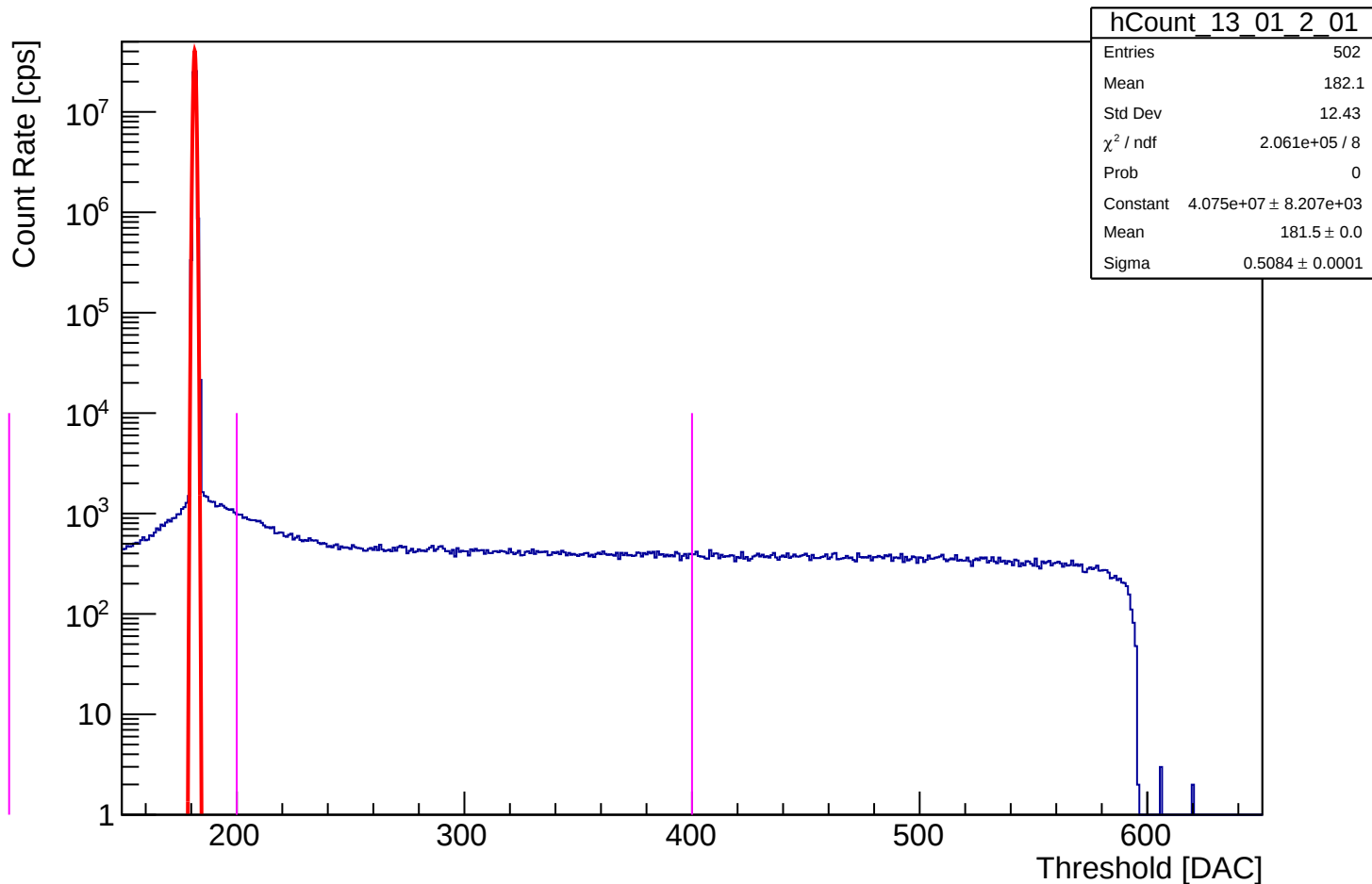


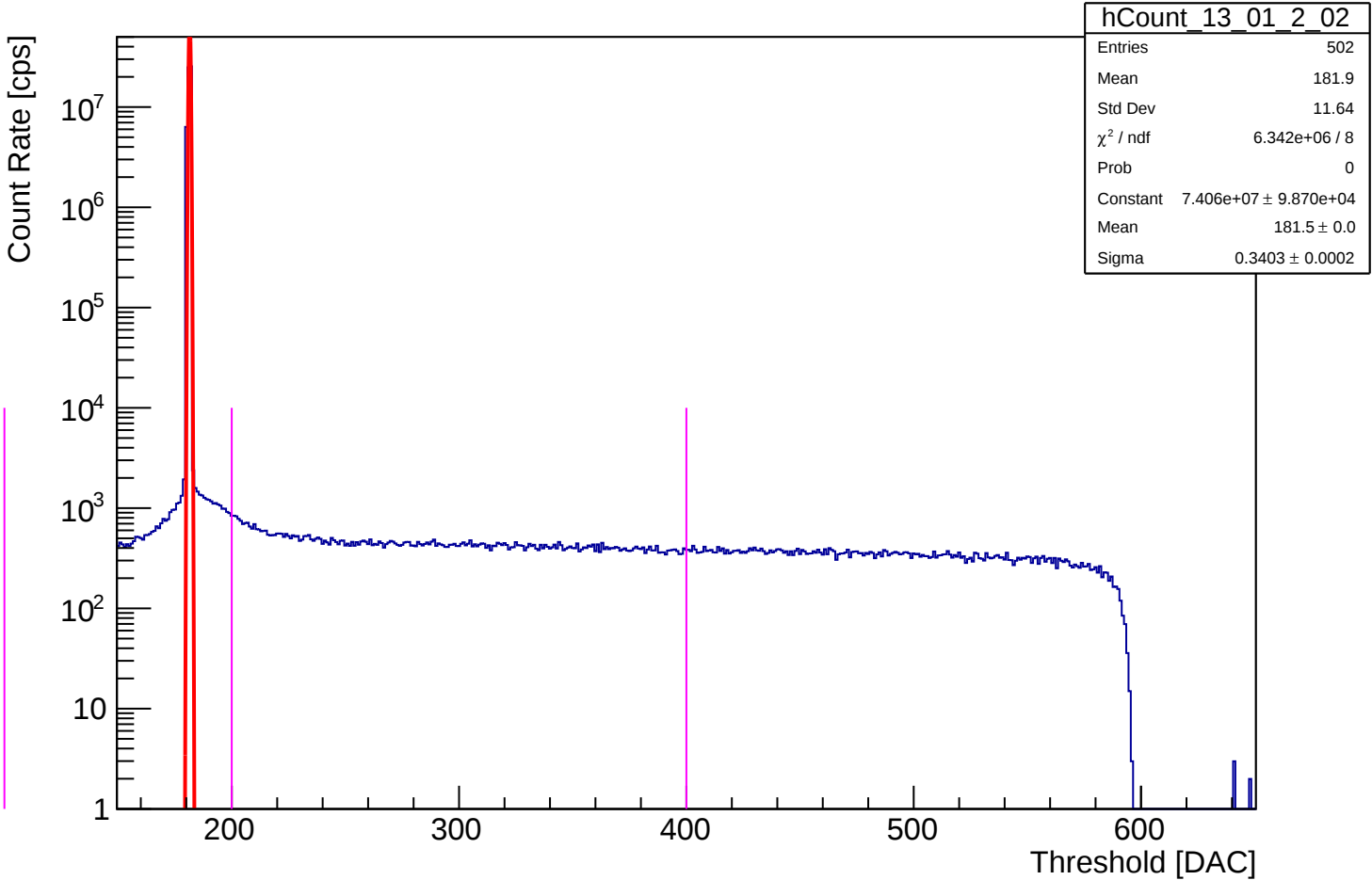
Row 1 Tile 1 Pmt 6 Pixel 56 Slot 13 Fiber 1 Asic 2 Channel 59

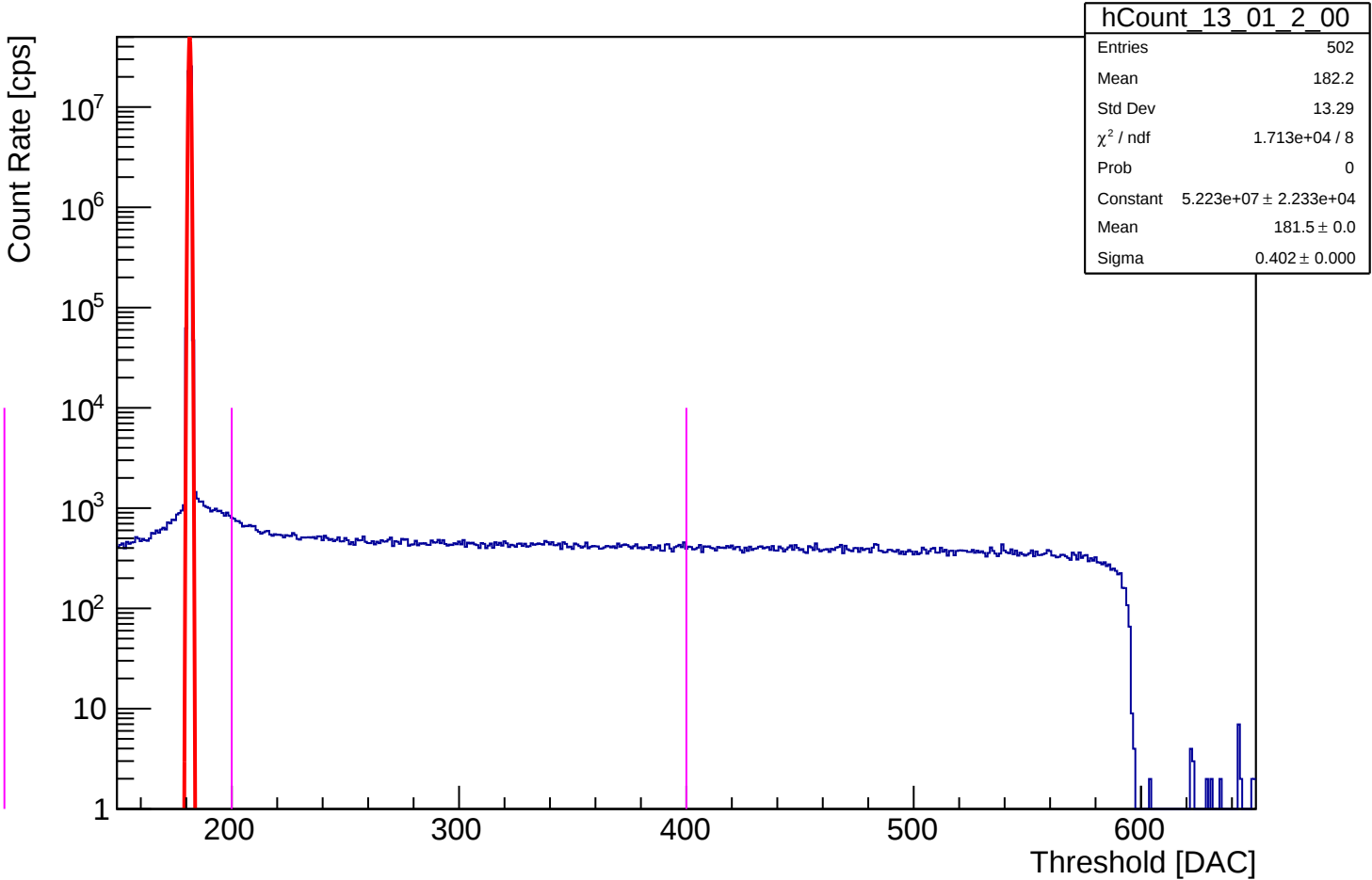




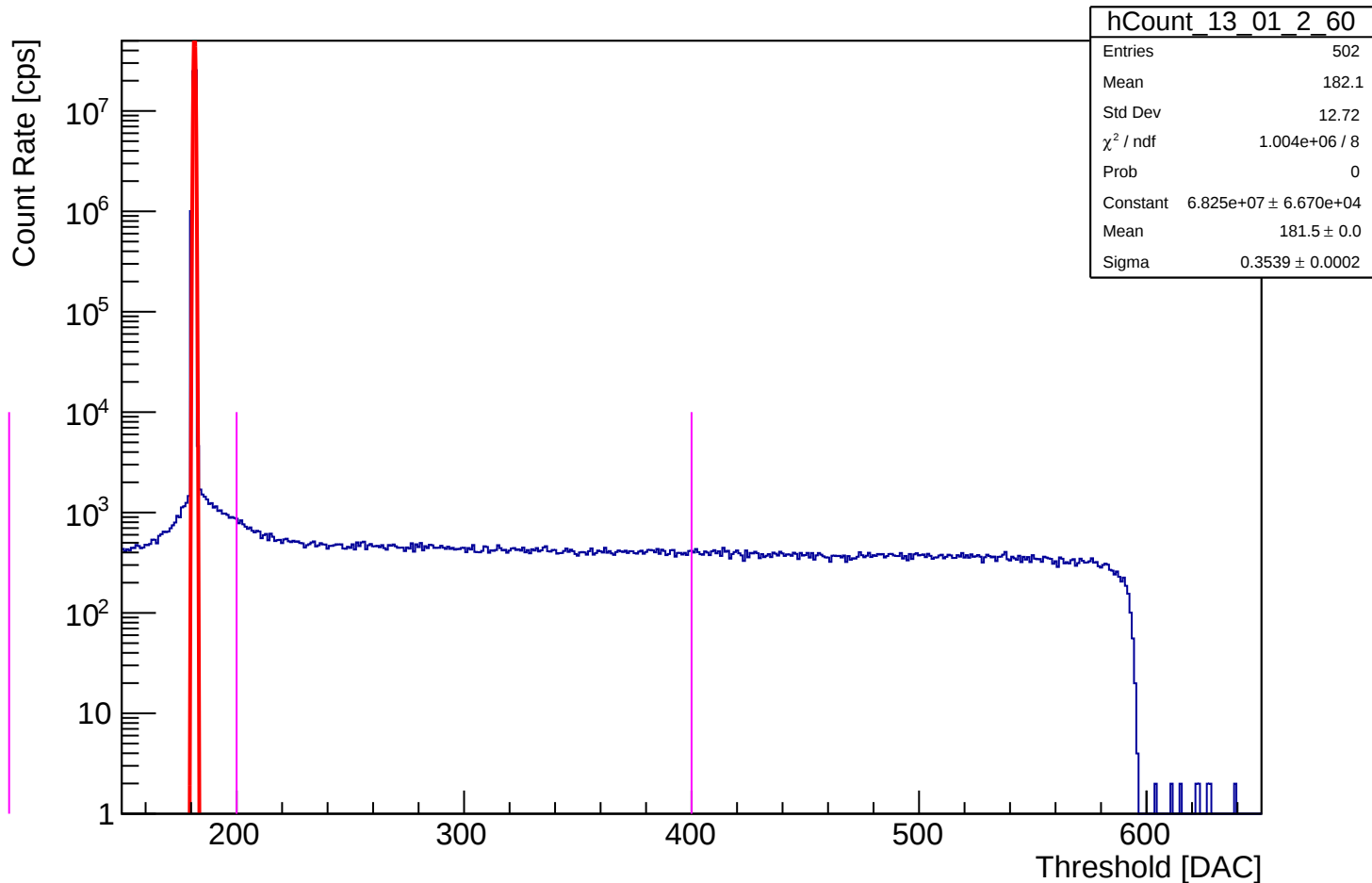
Row 1 Tile 1 Pmt 6 Pixel 58 Slot 13 Fiber 1 Asic 2 Channel 1



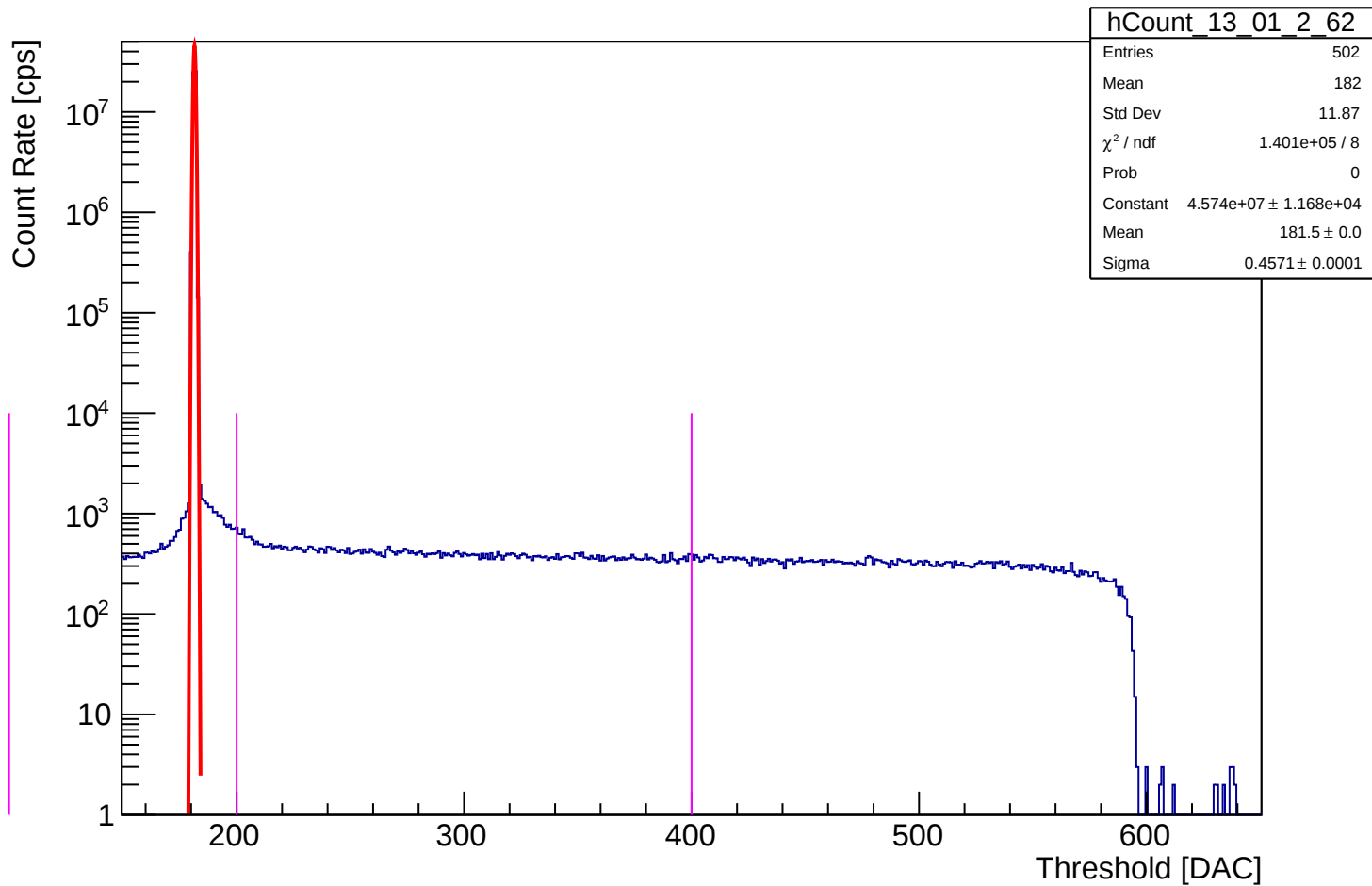




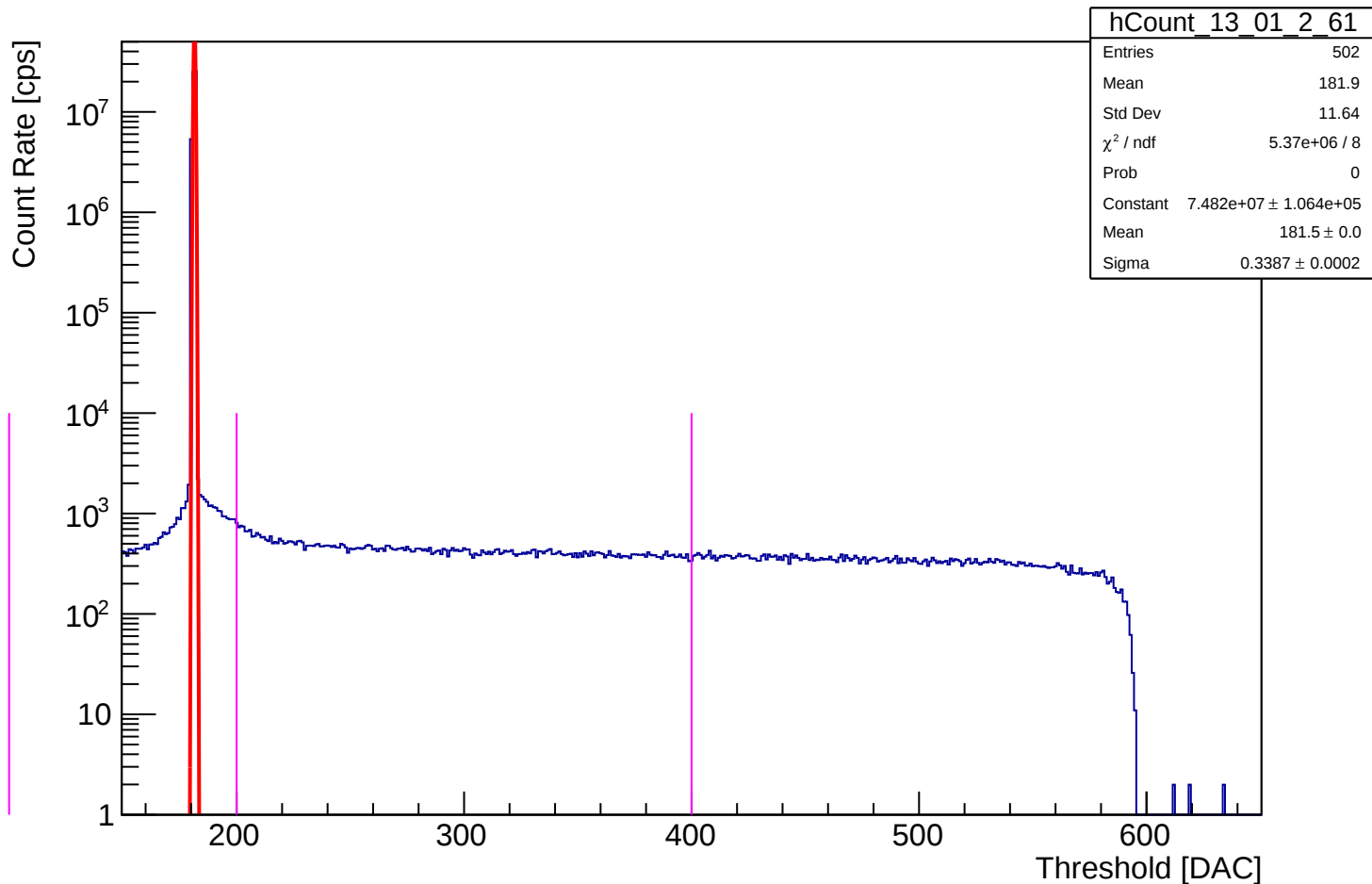
Row 1 Tile 1 Pmt 6 Pixel 61 Slot 13 Fiber 1 Asic 2 Channel 60



Row 1 Tile 1 Pmt 6 Pixel 62 Slot 13 Fiber 1 Asic 2 Channel 62



Row 1 Tile 1 Pmt 6 Pixel 63 Slot 13 Fiber 1 Asic 2 Channel 61



Row 1 Tile 1 Pmt 6 Pixel 64 Slot 13 Fiber 1 Asic 2 Channel 63

