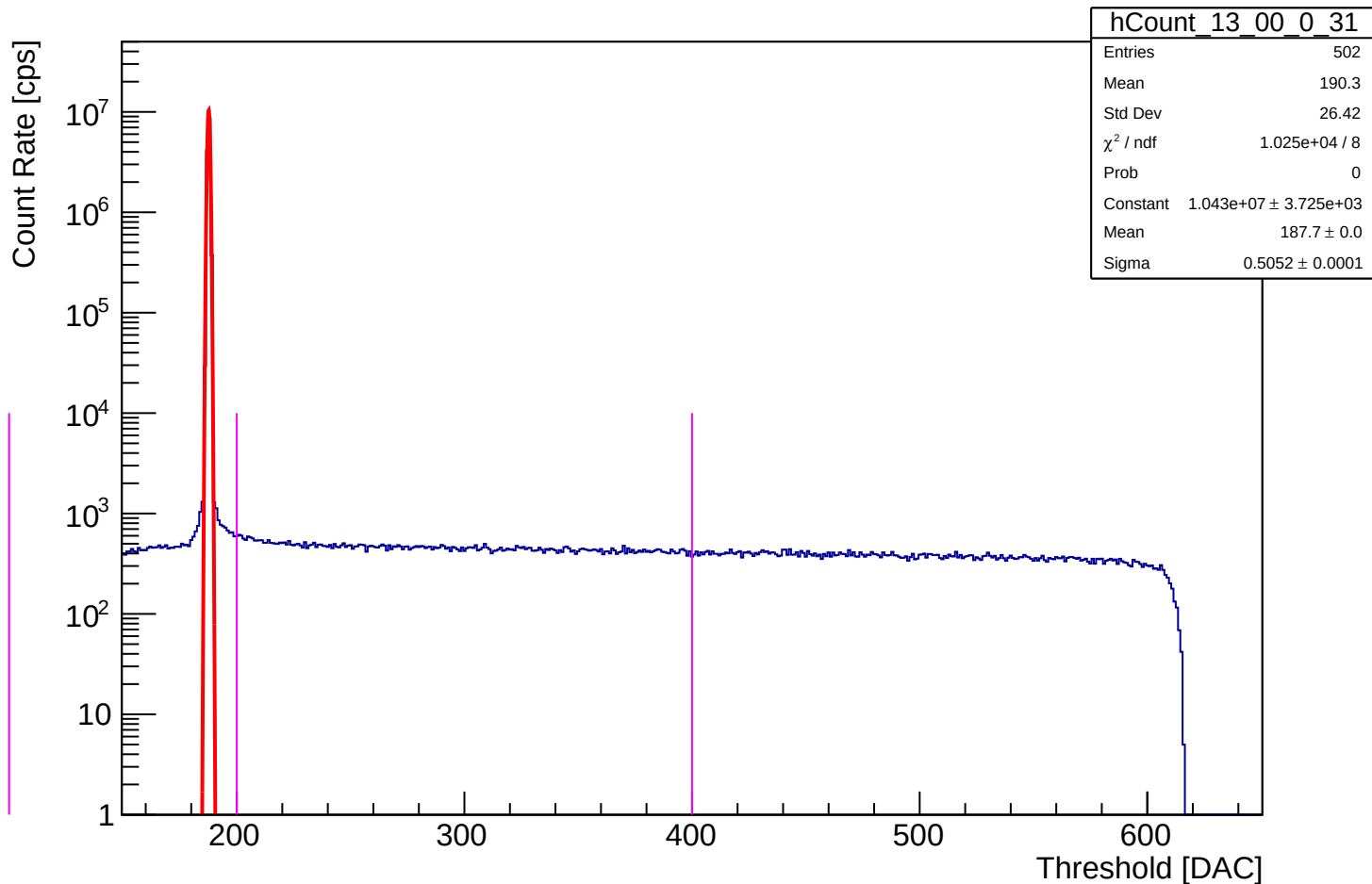
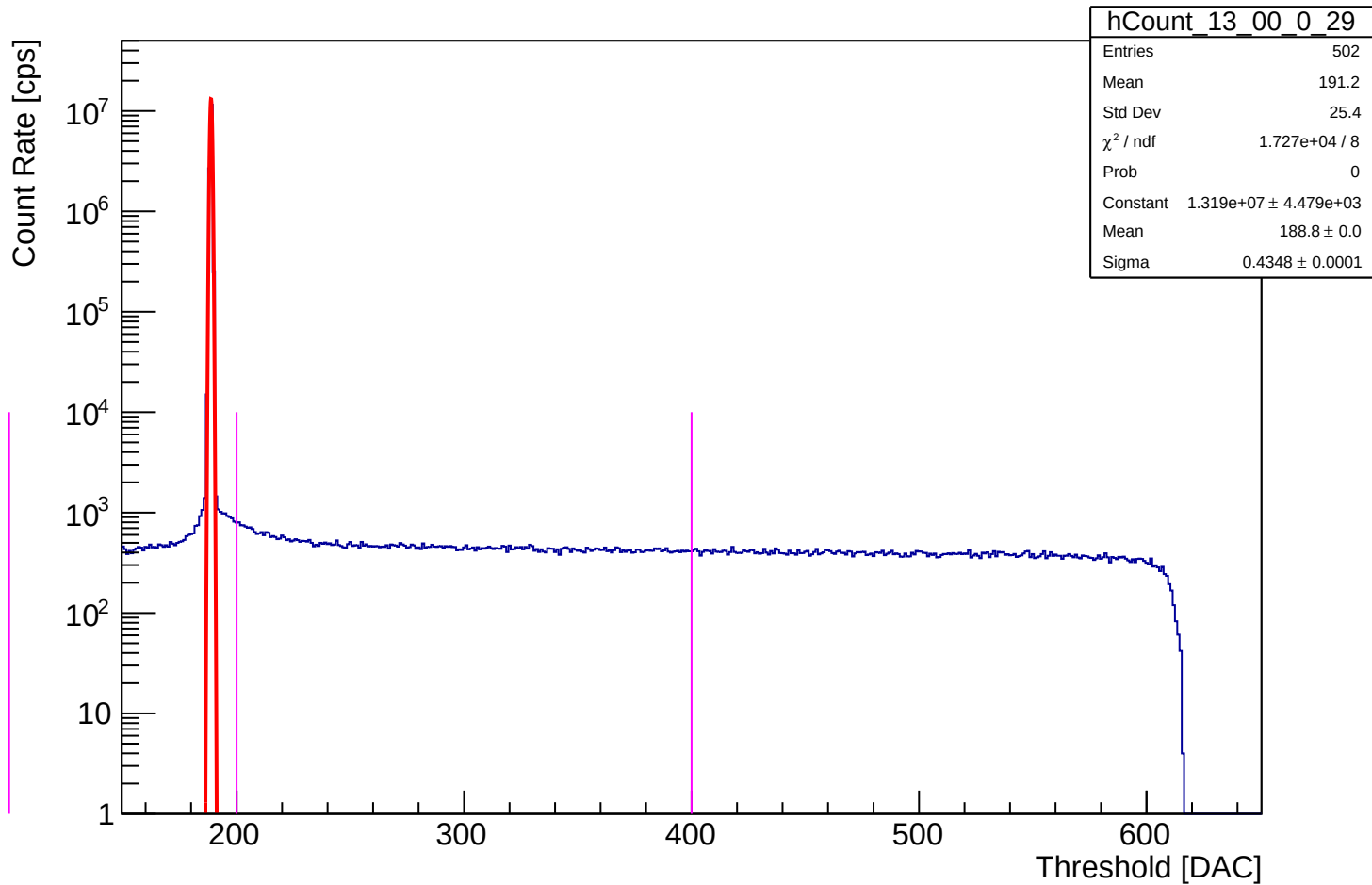


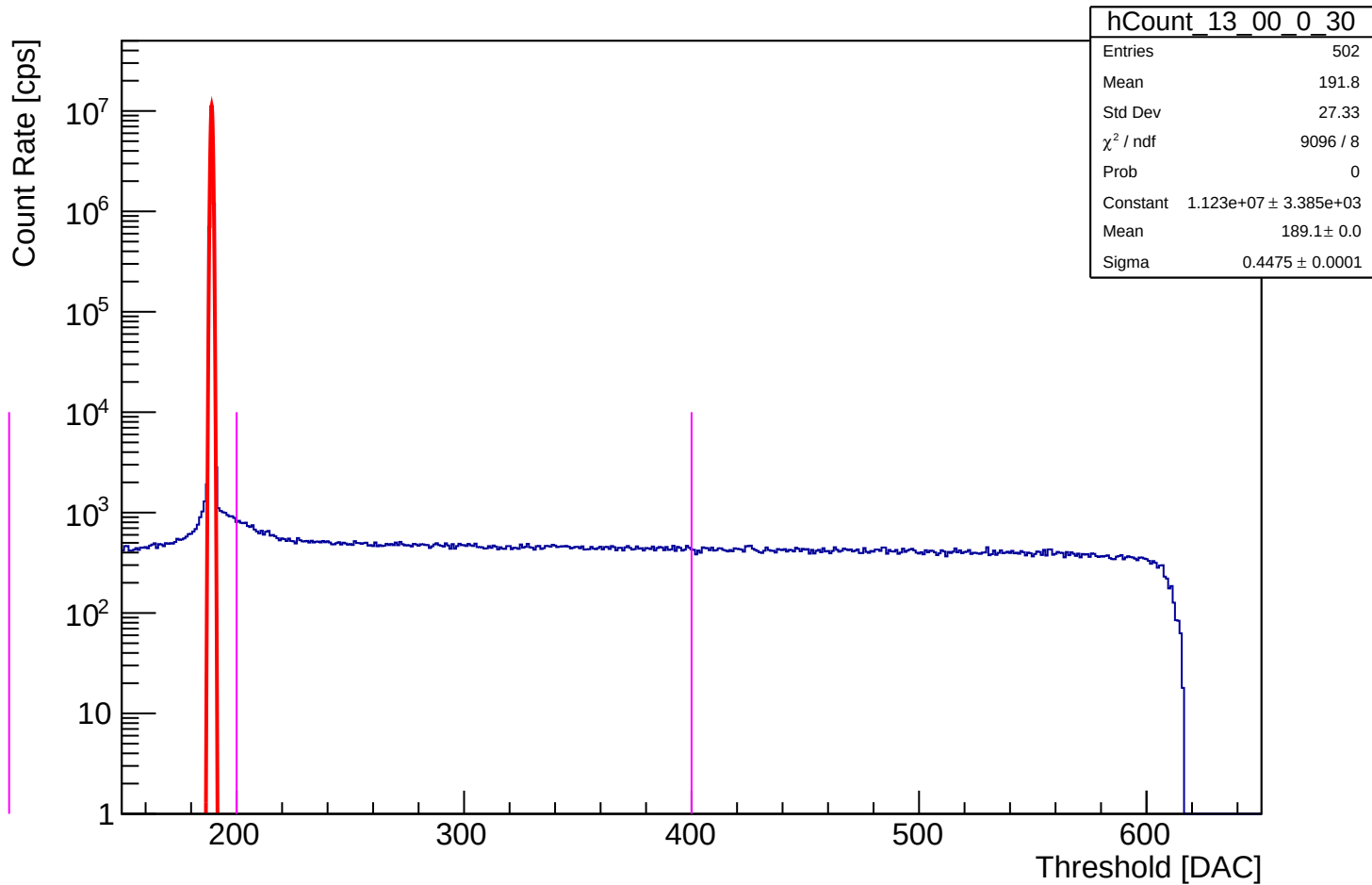
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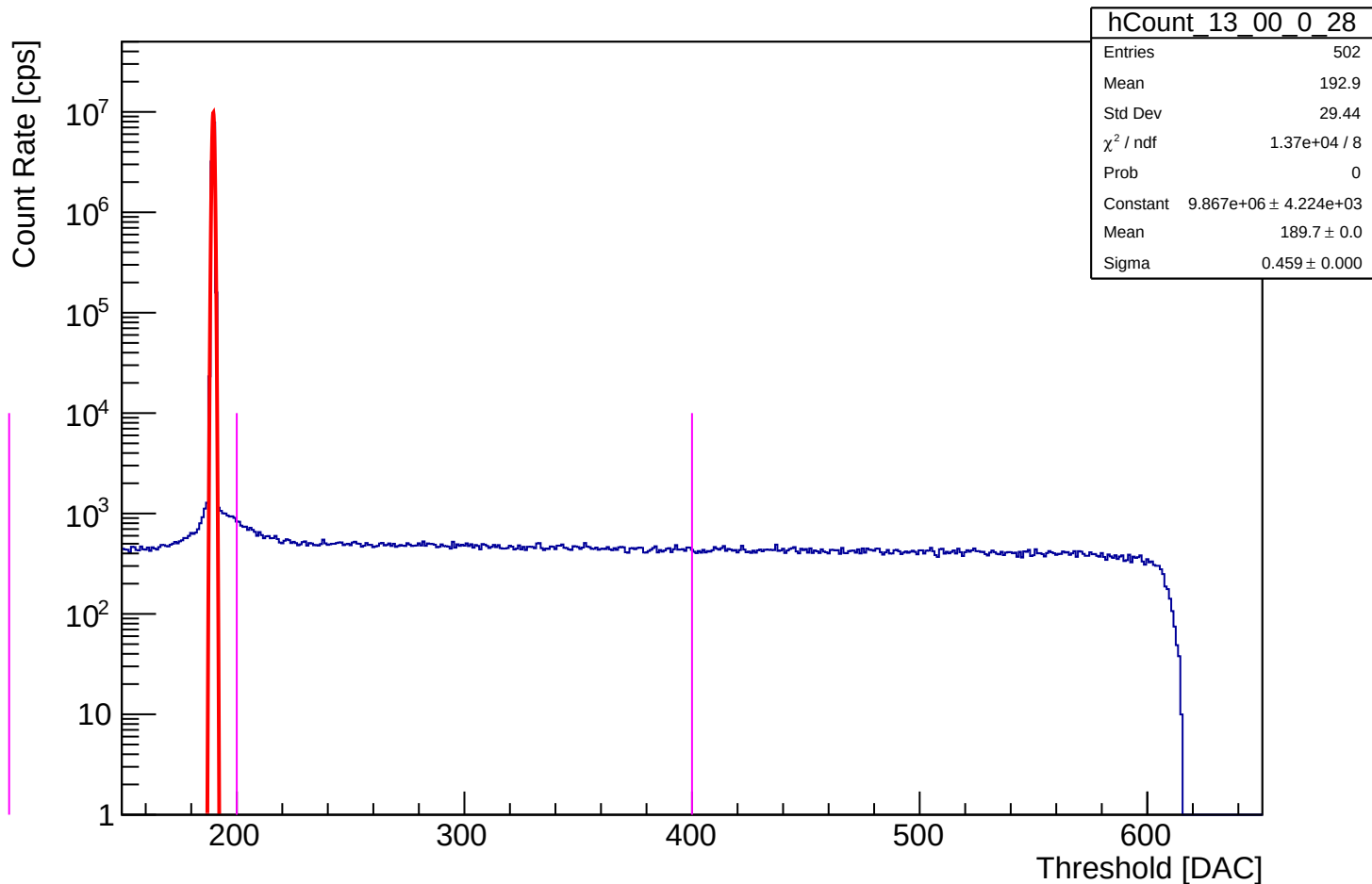
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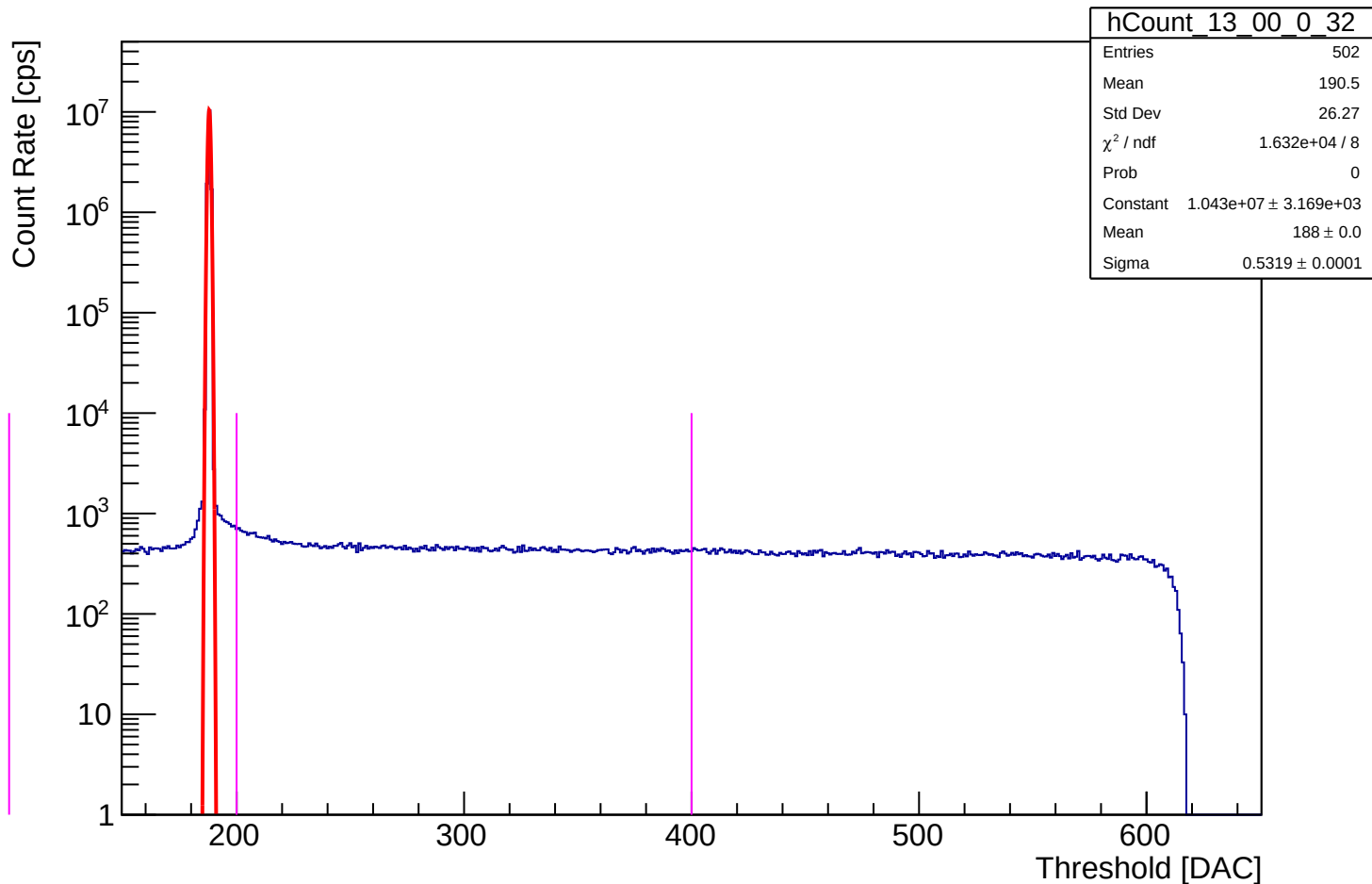
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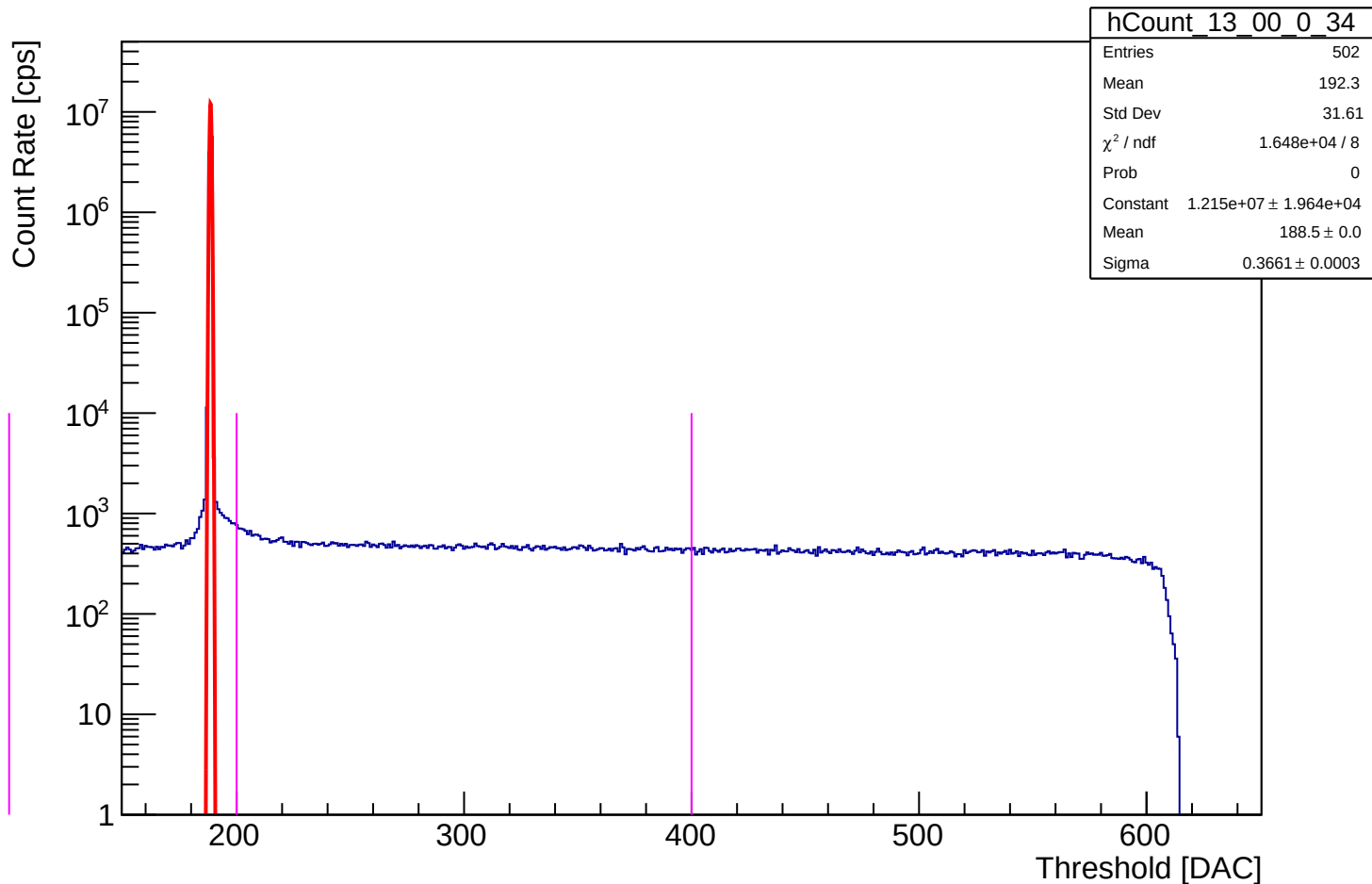
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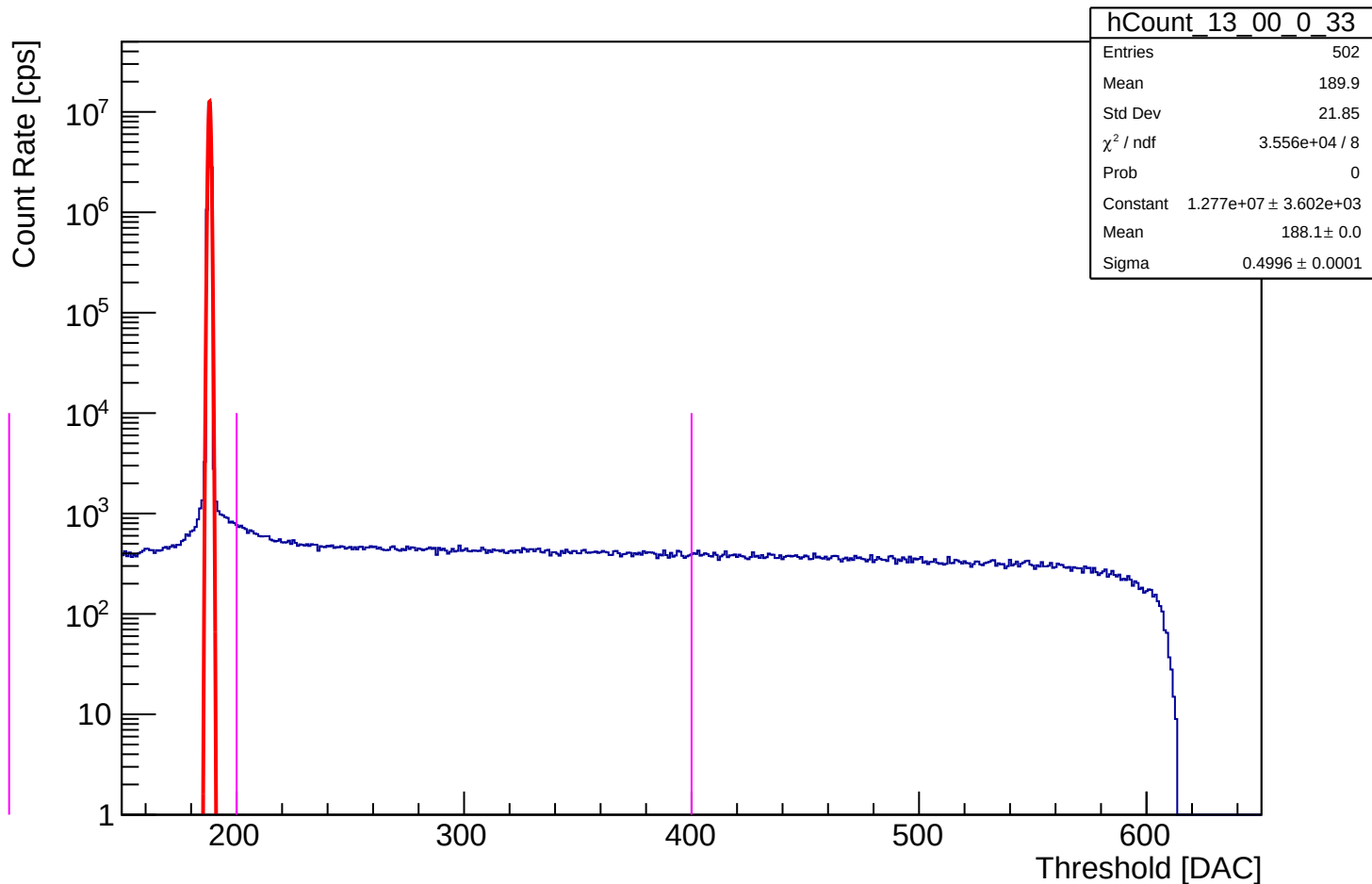
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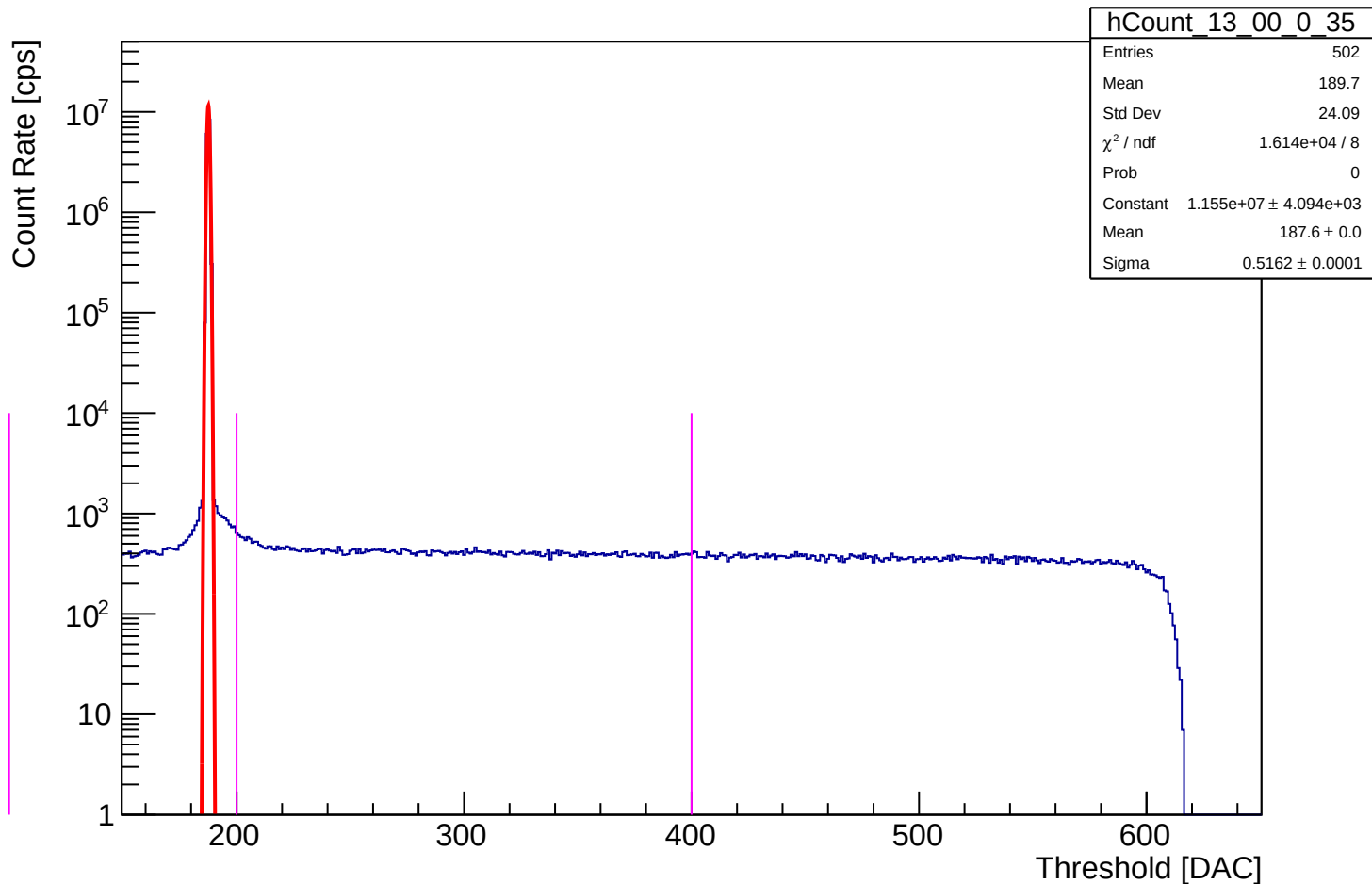
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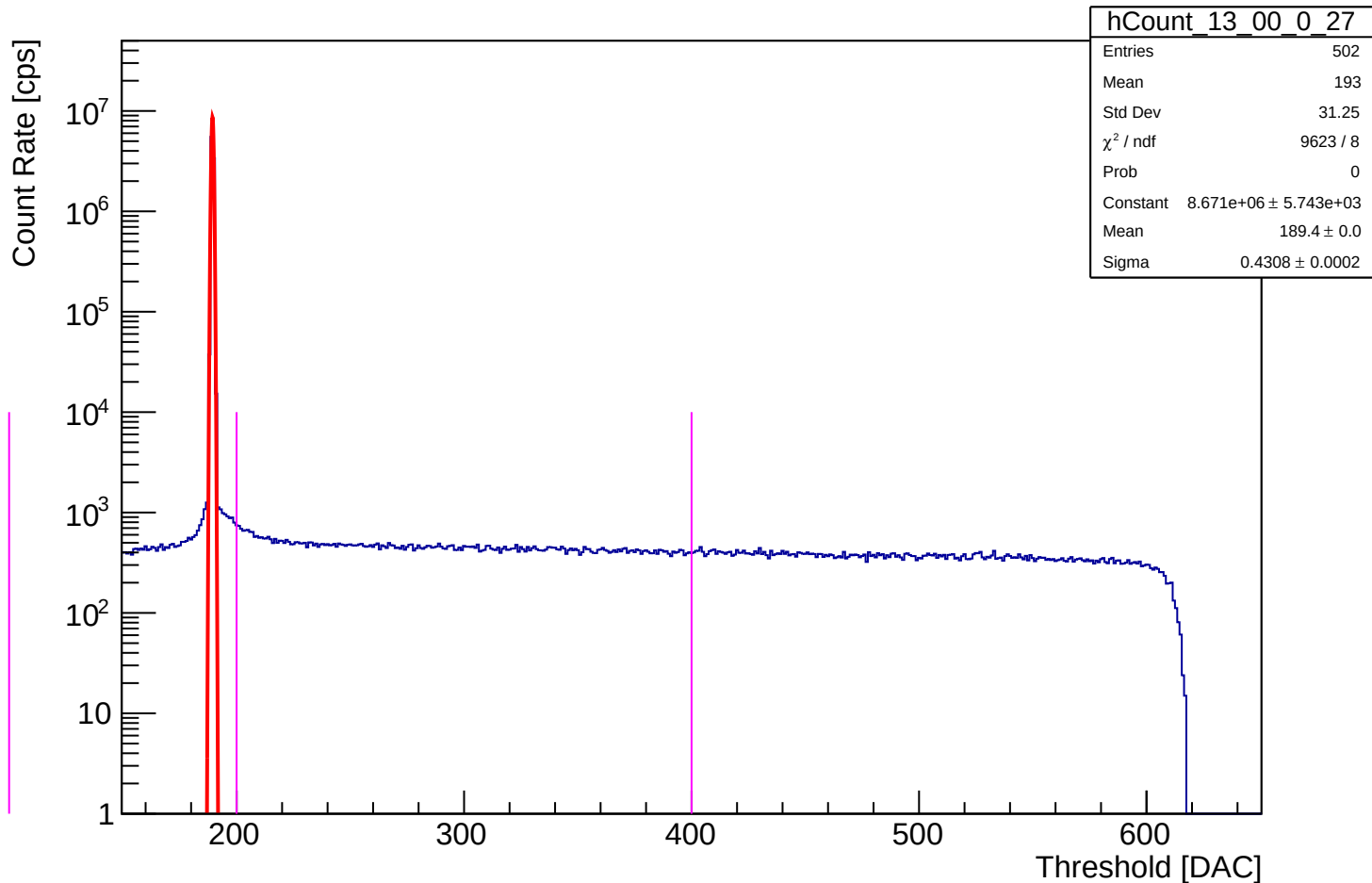
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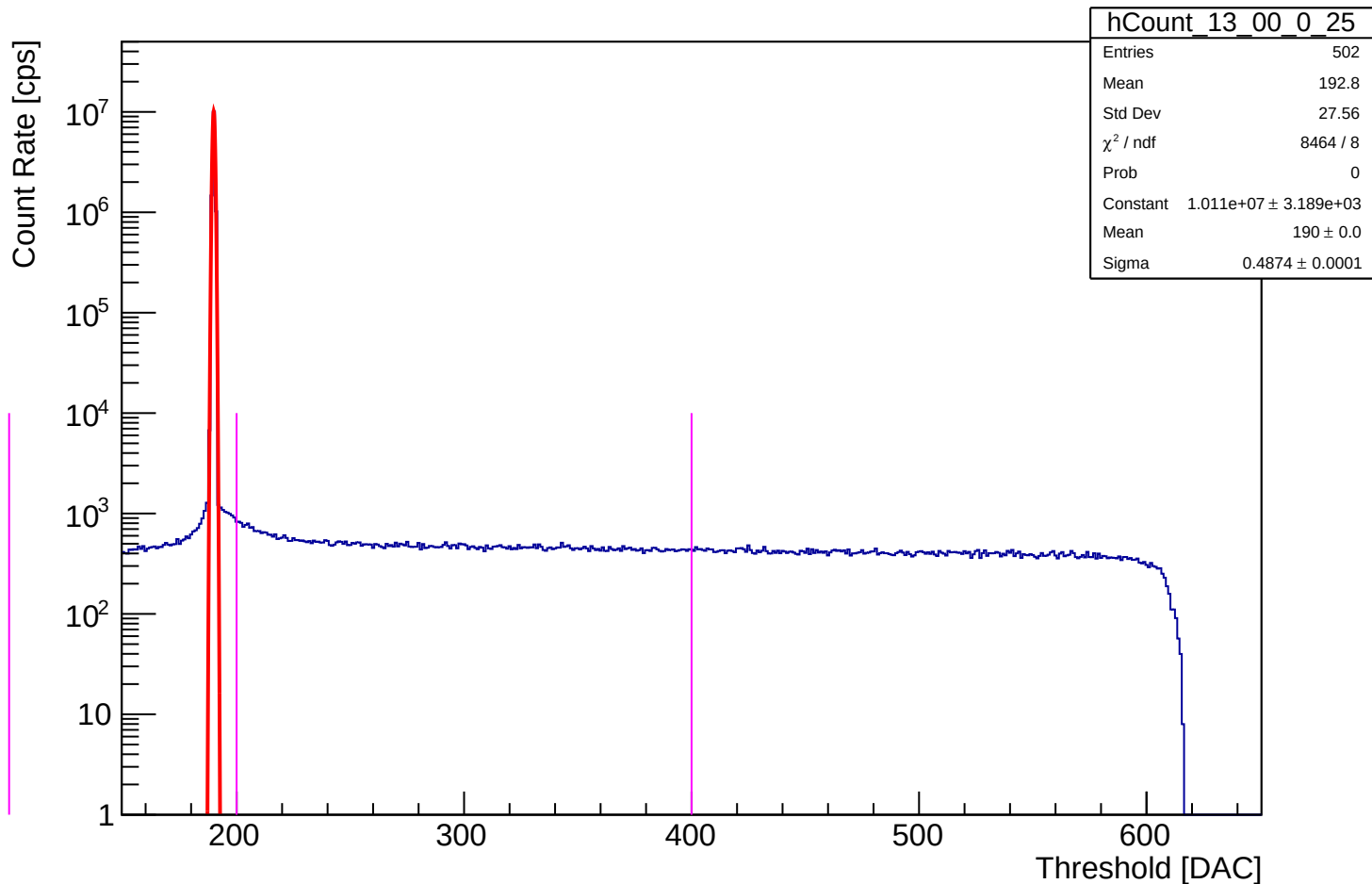
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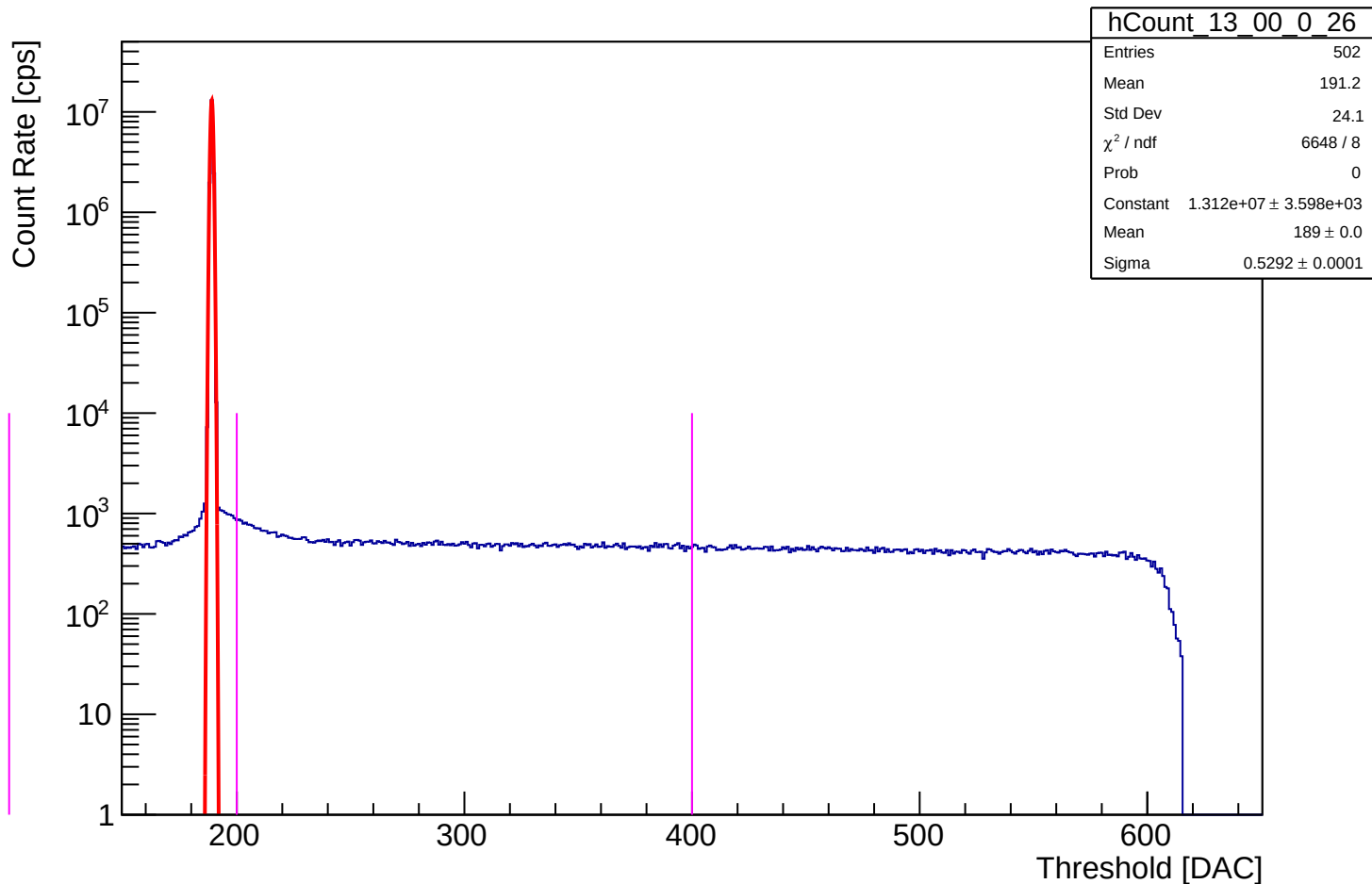
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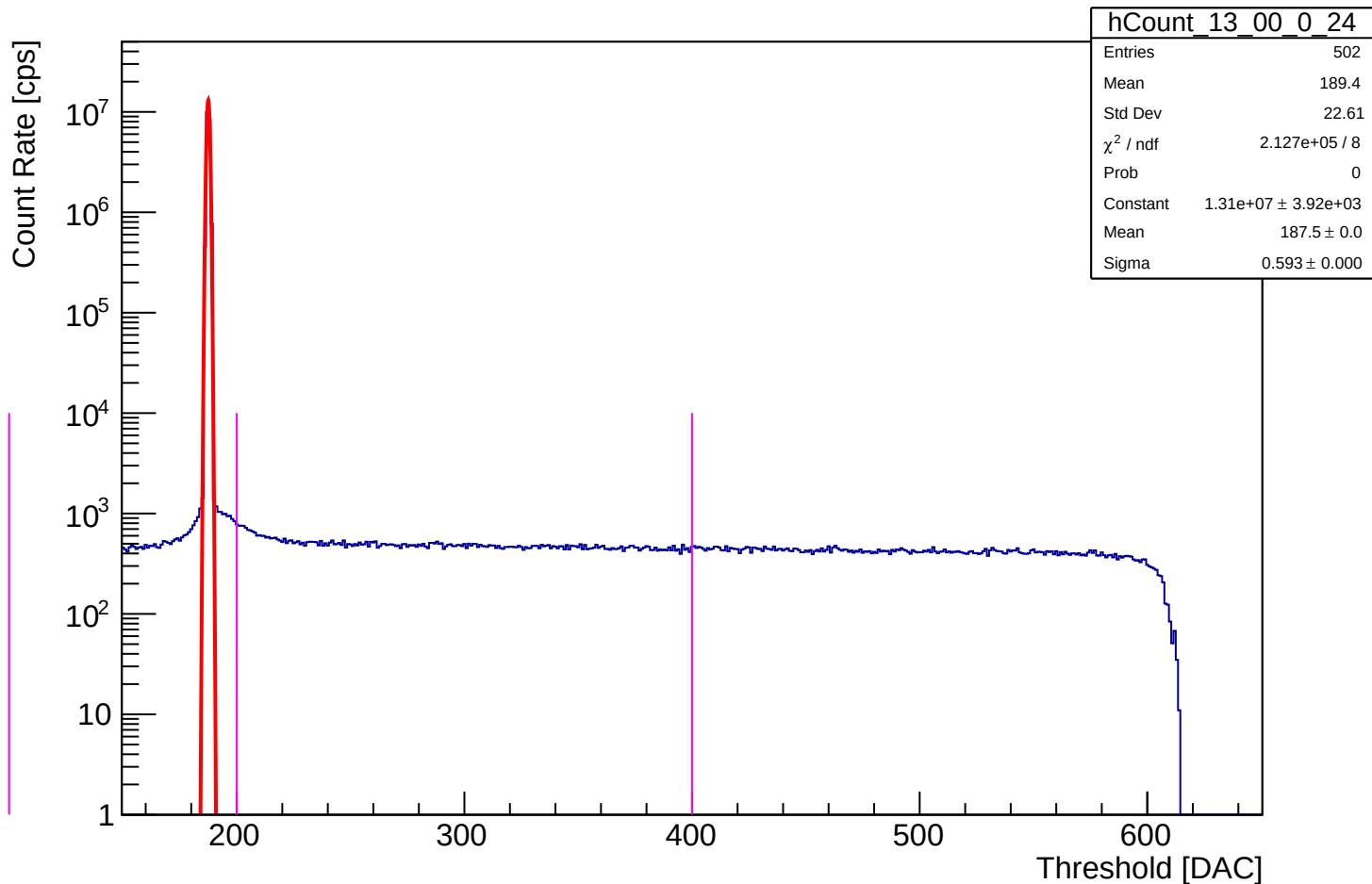
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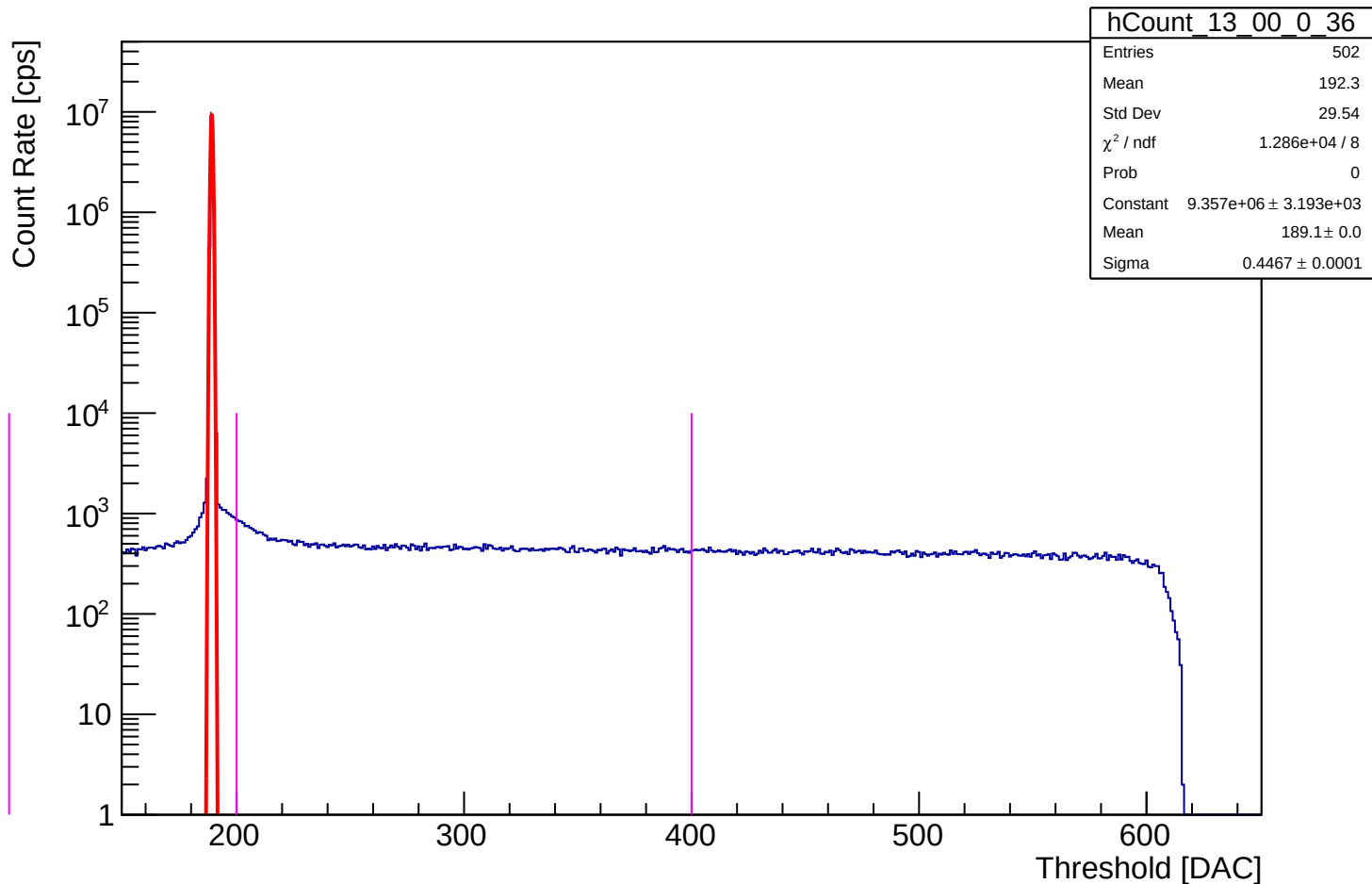
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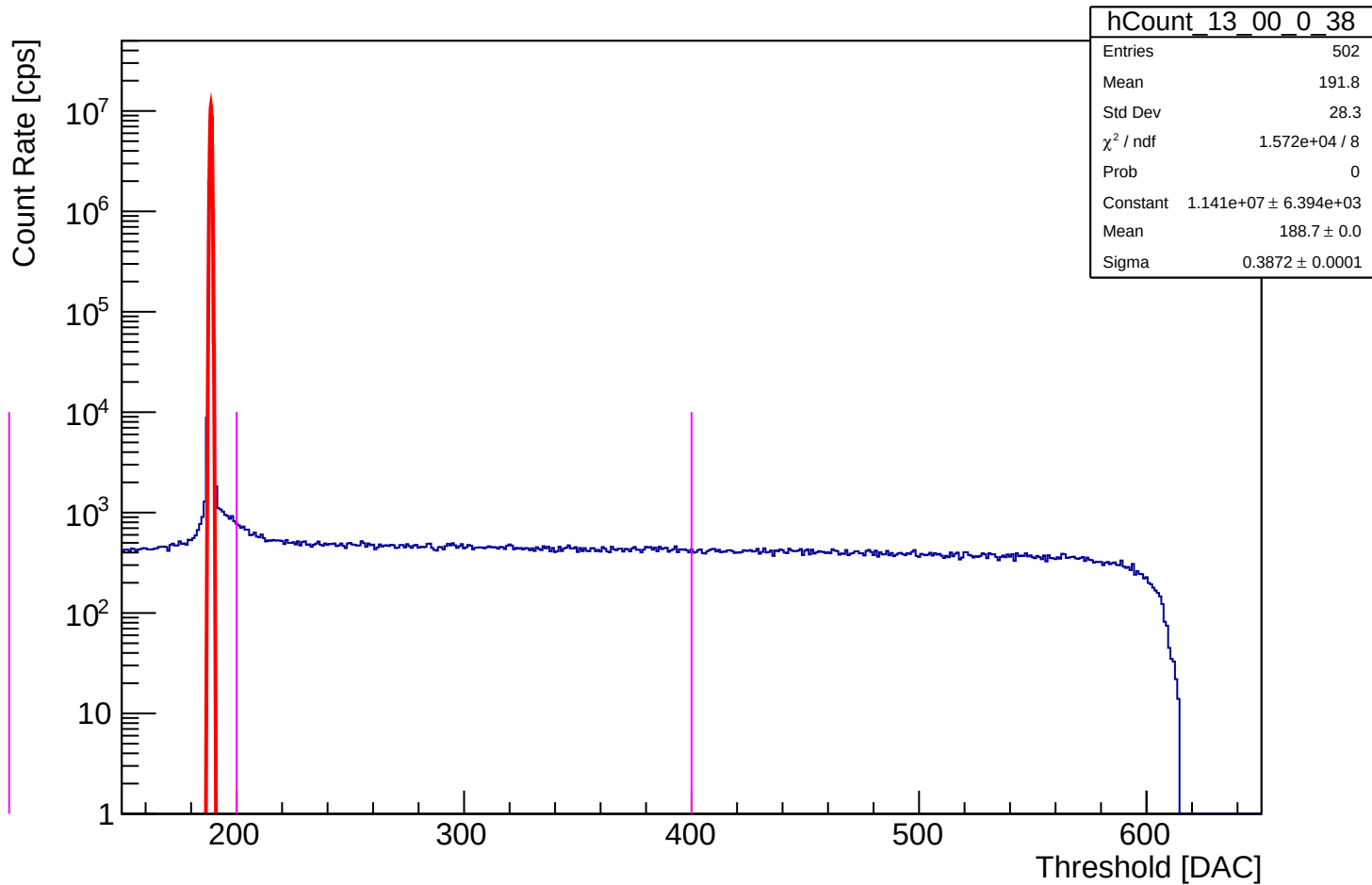
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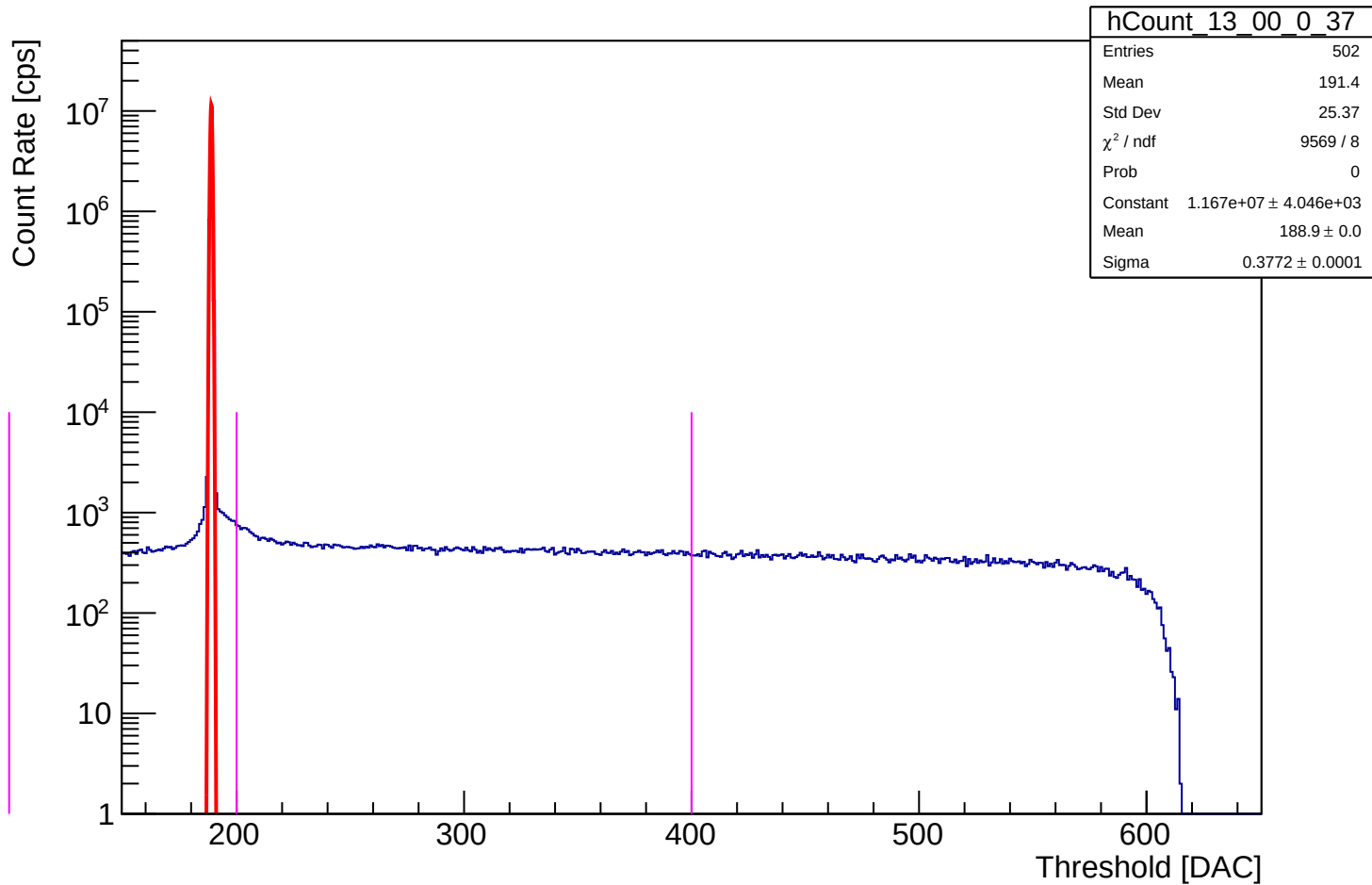
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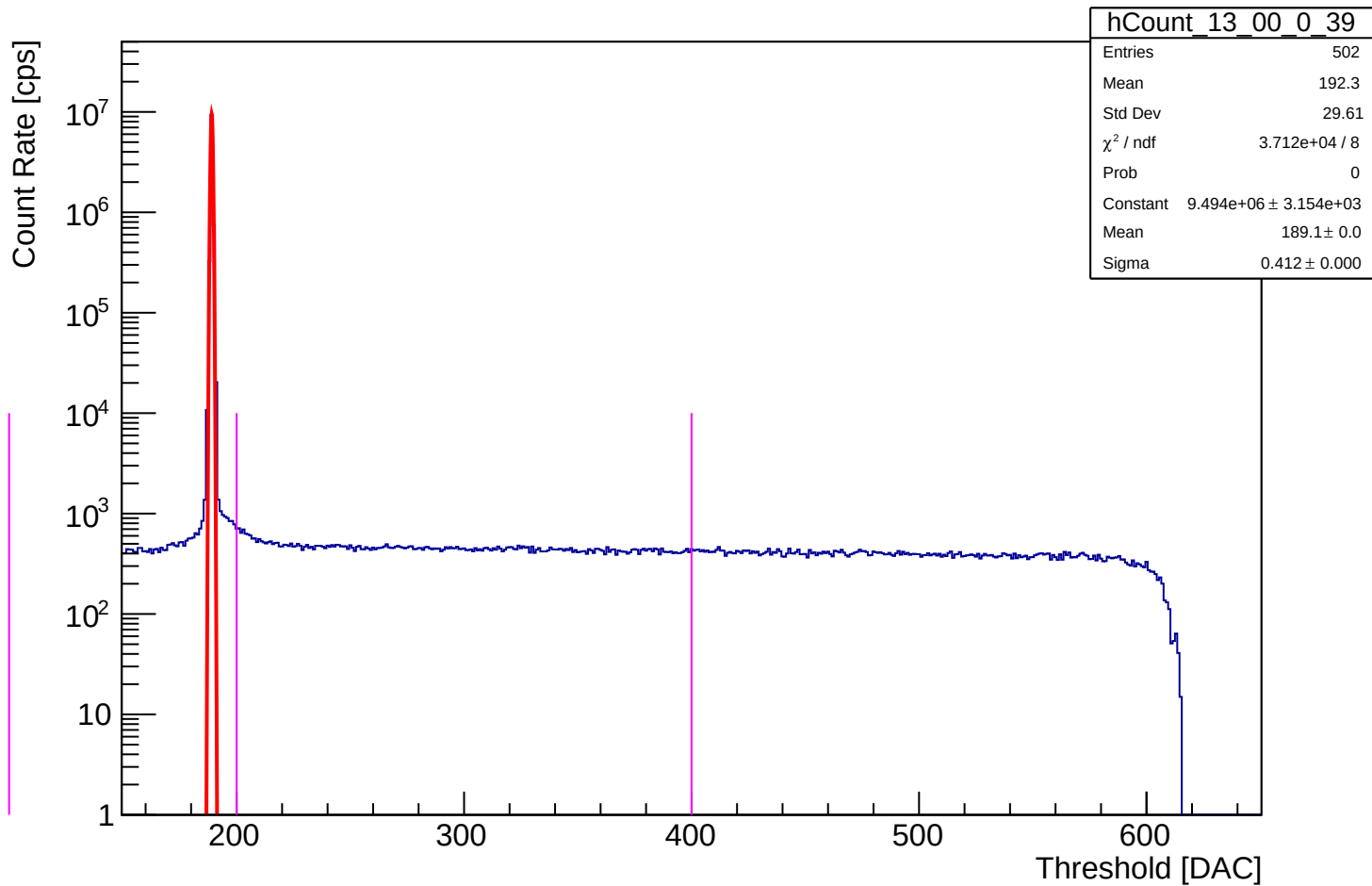
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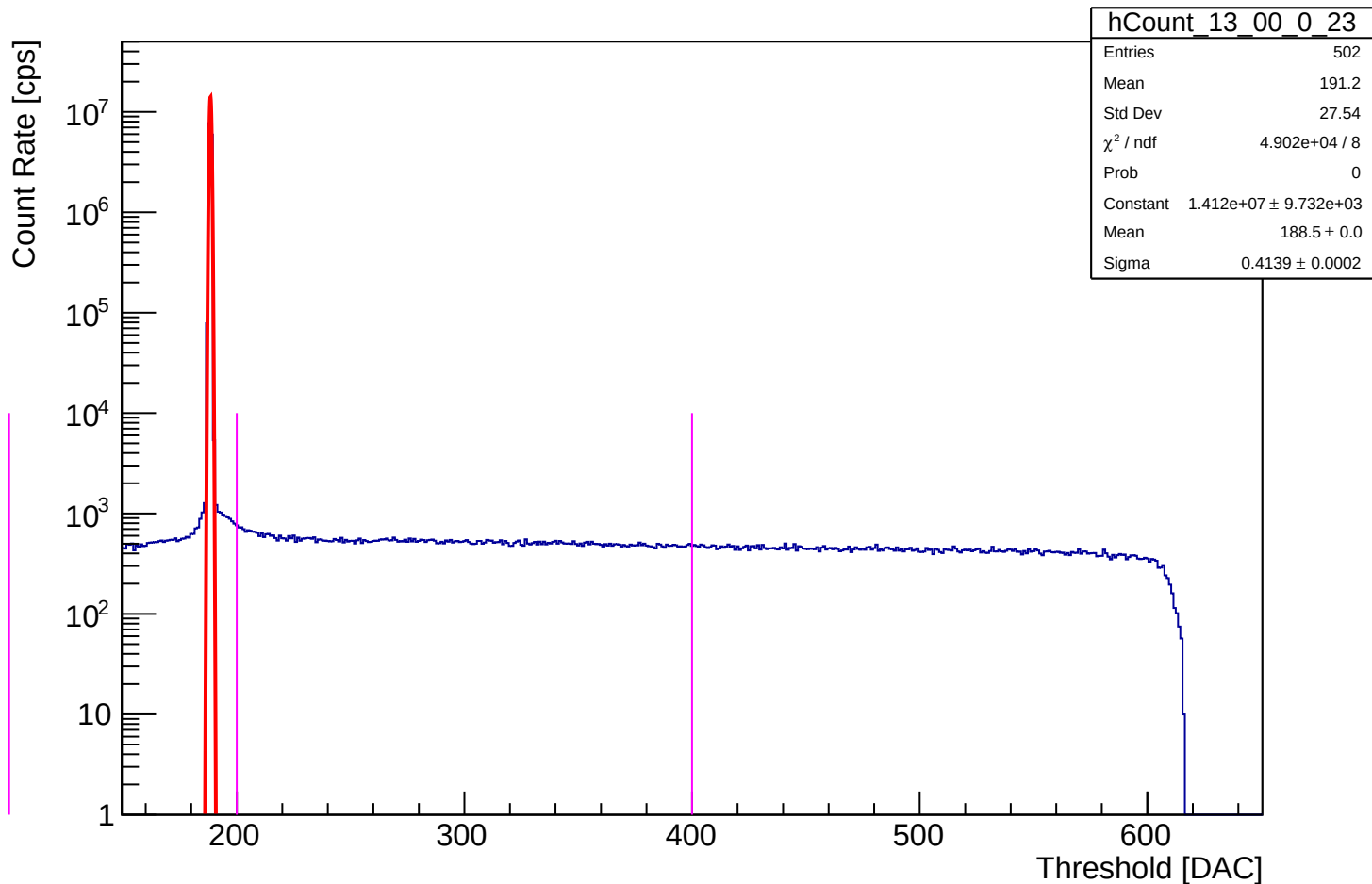
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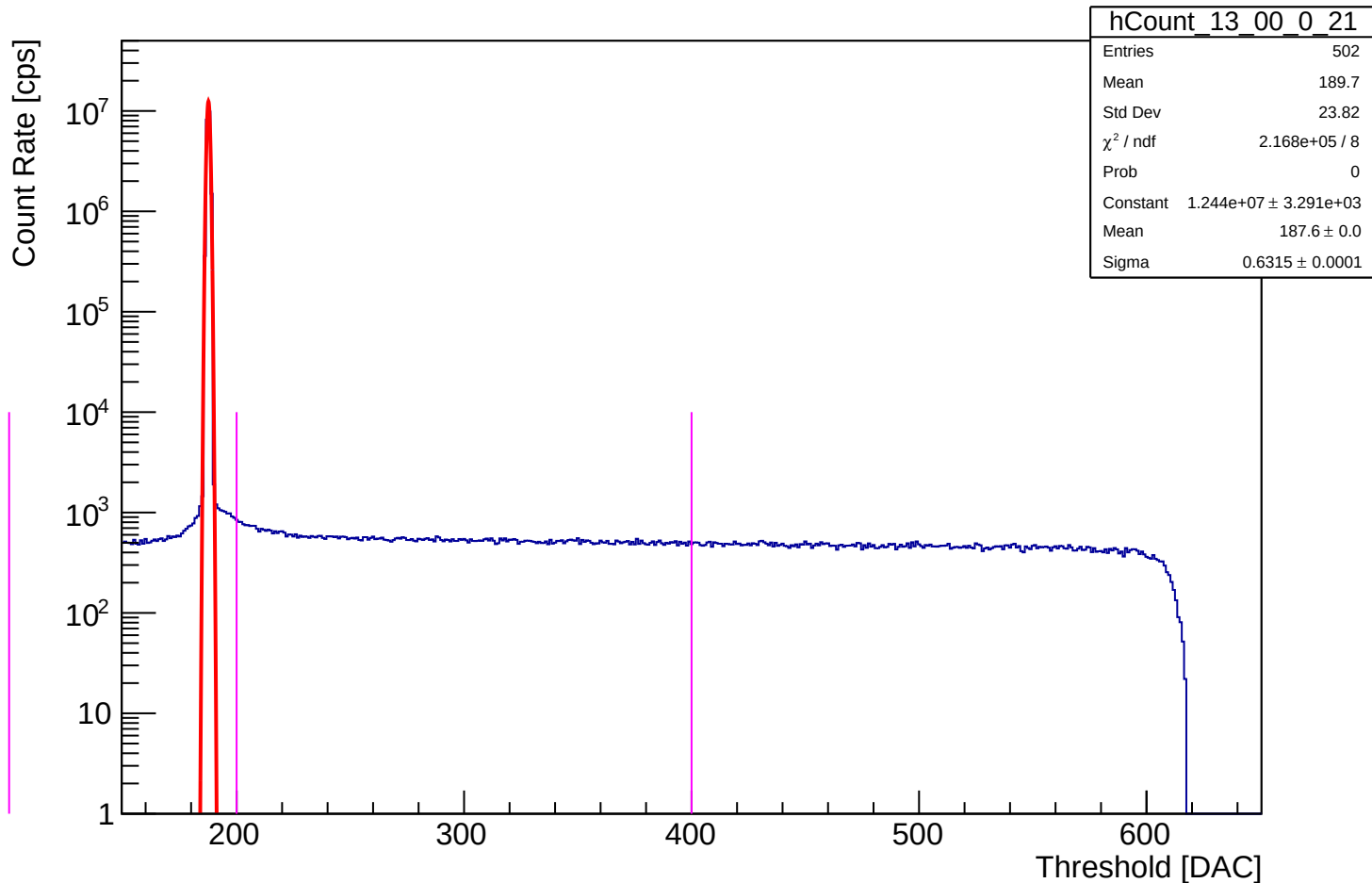
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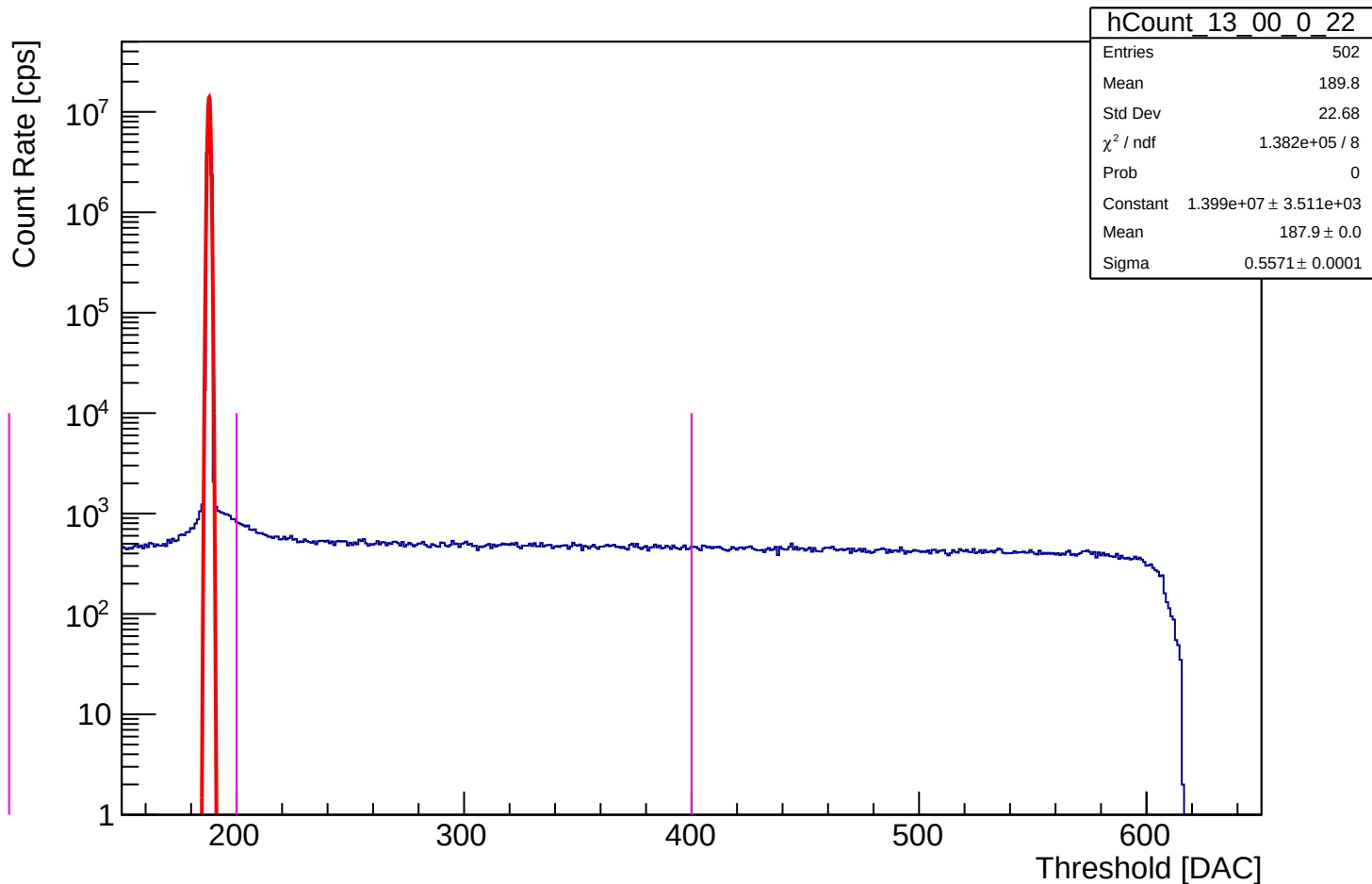
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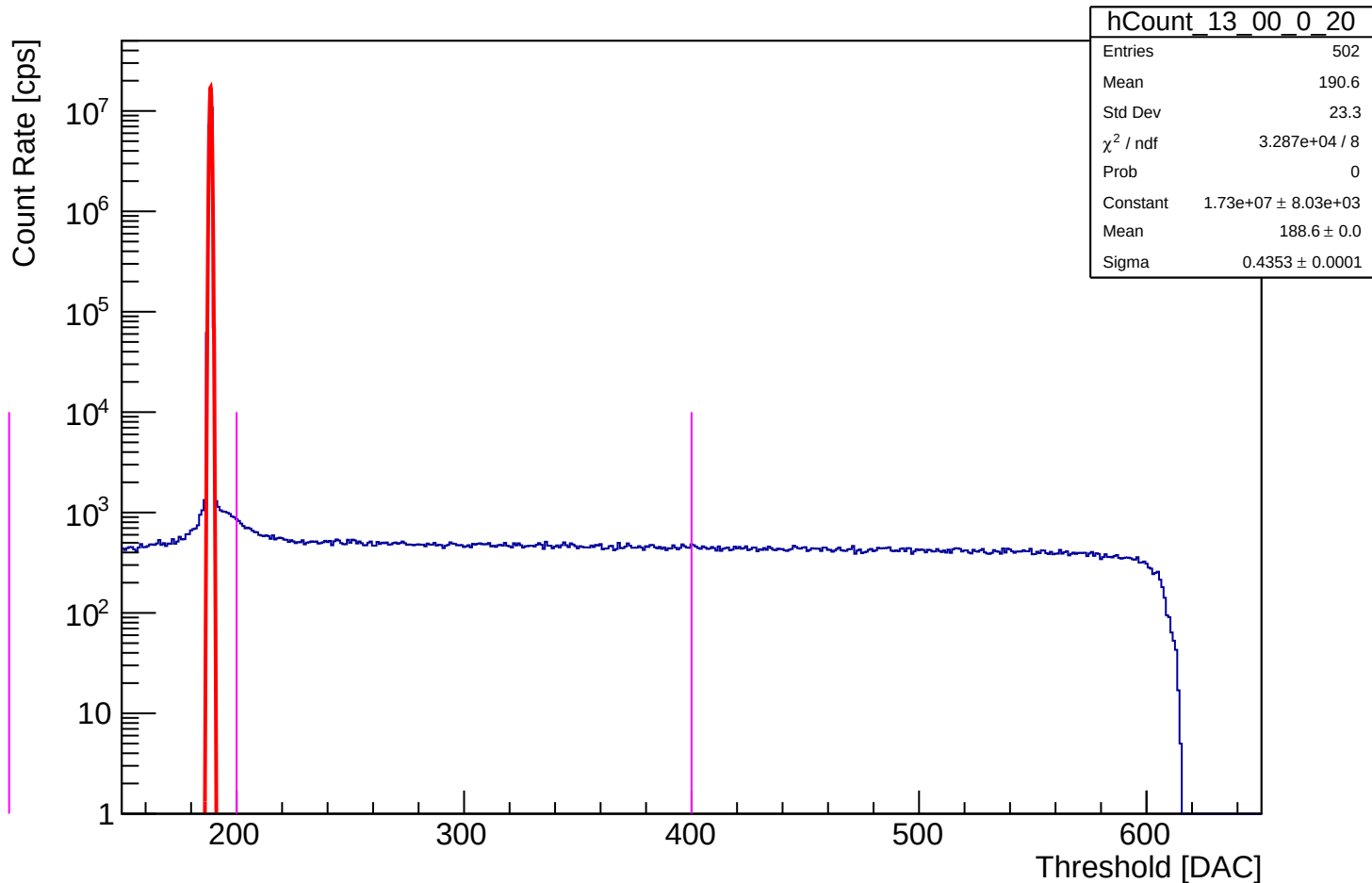
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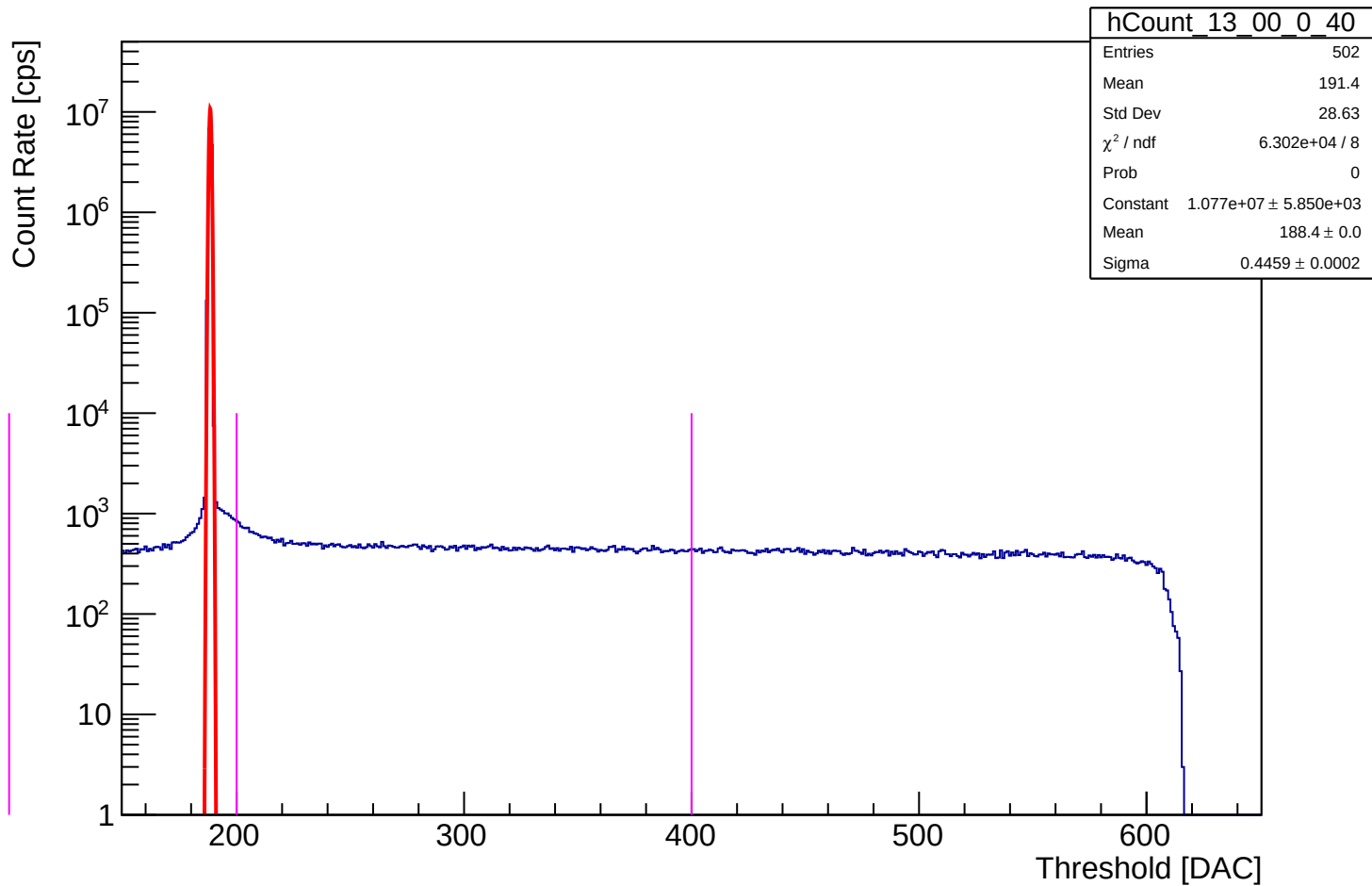
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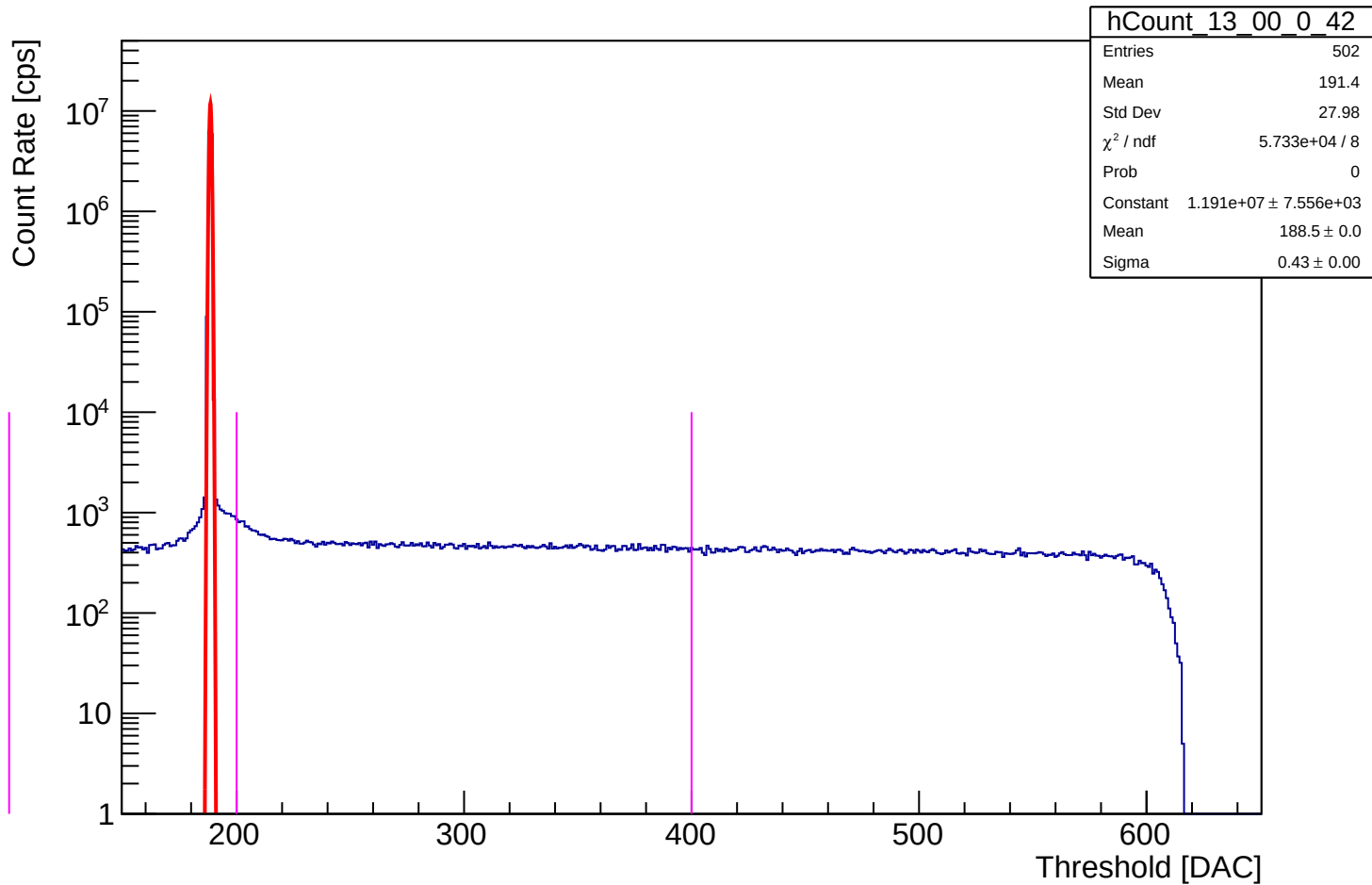
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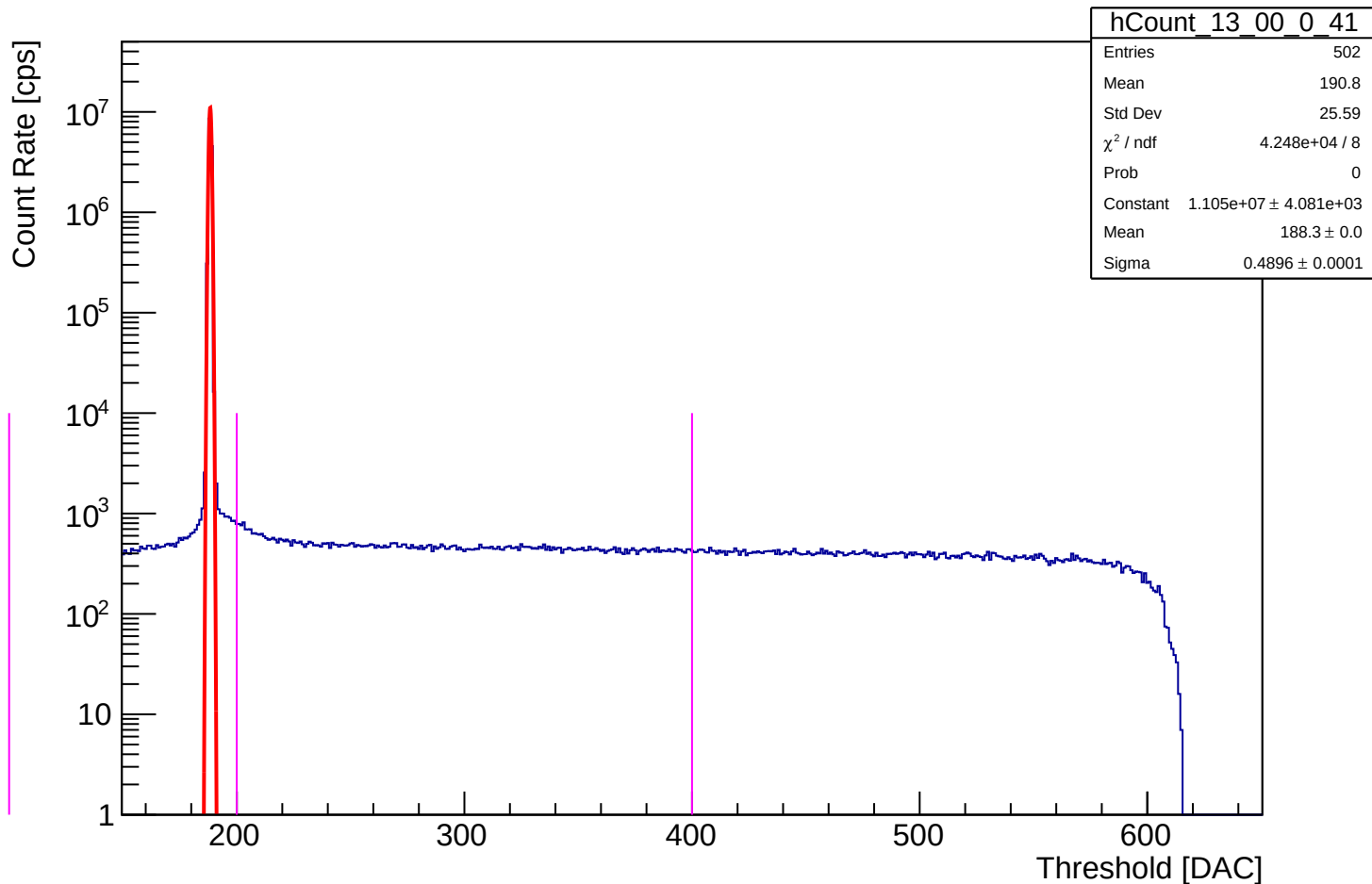
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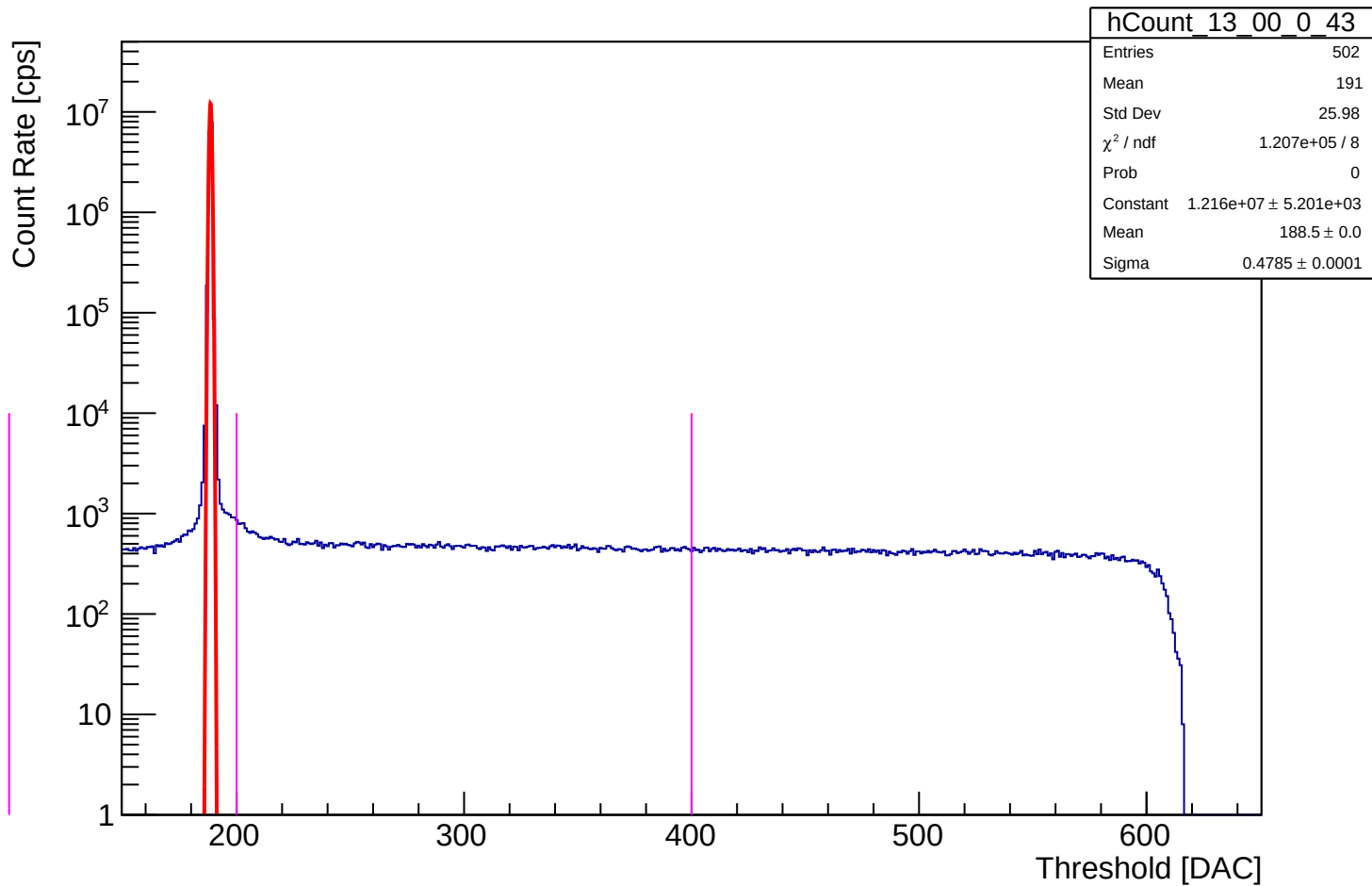
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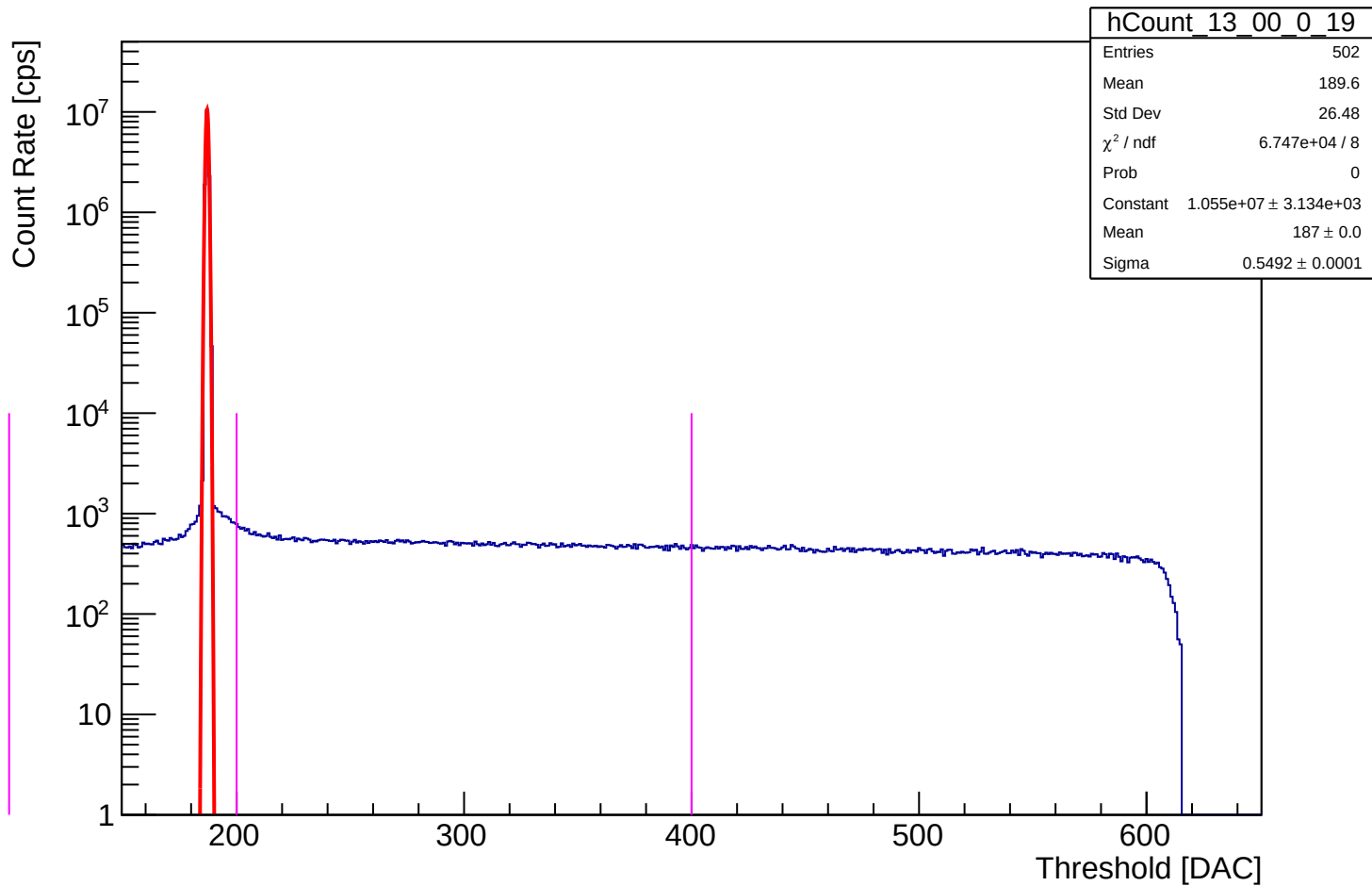
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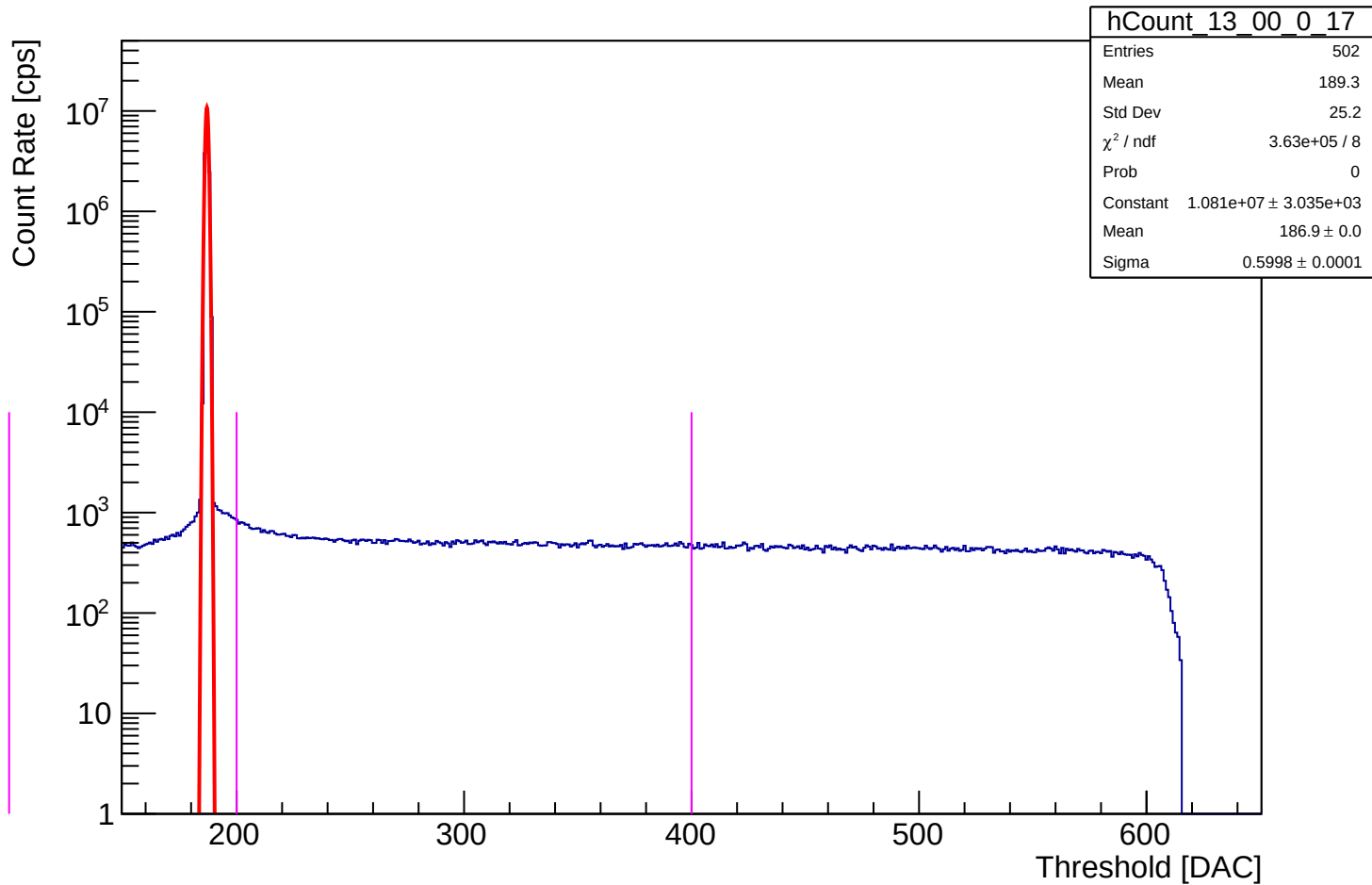
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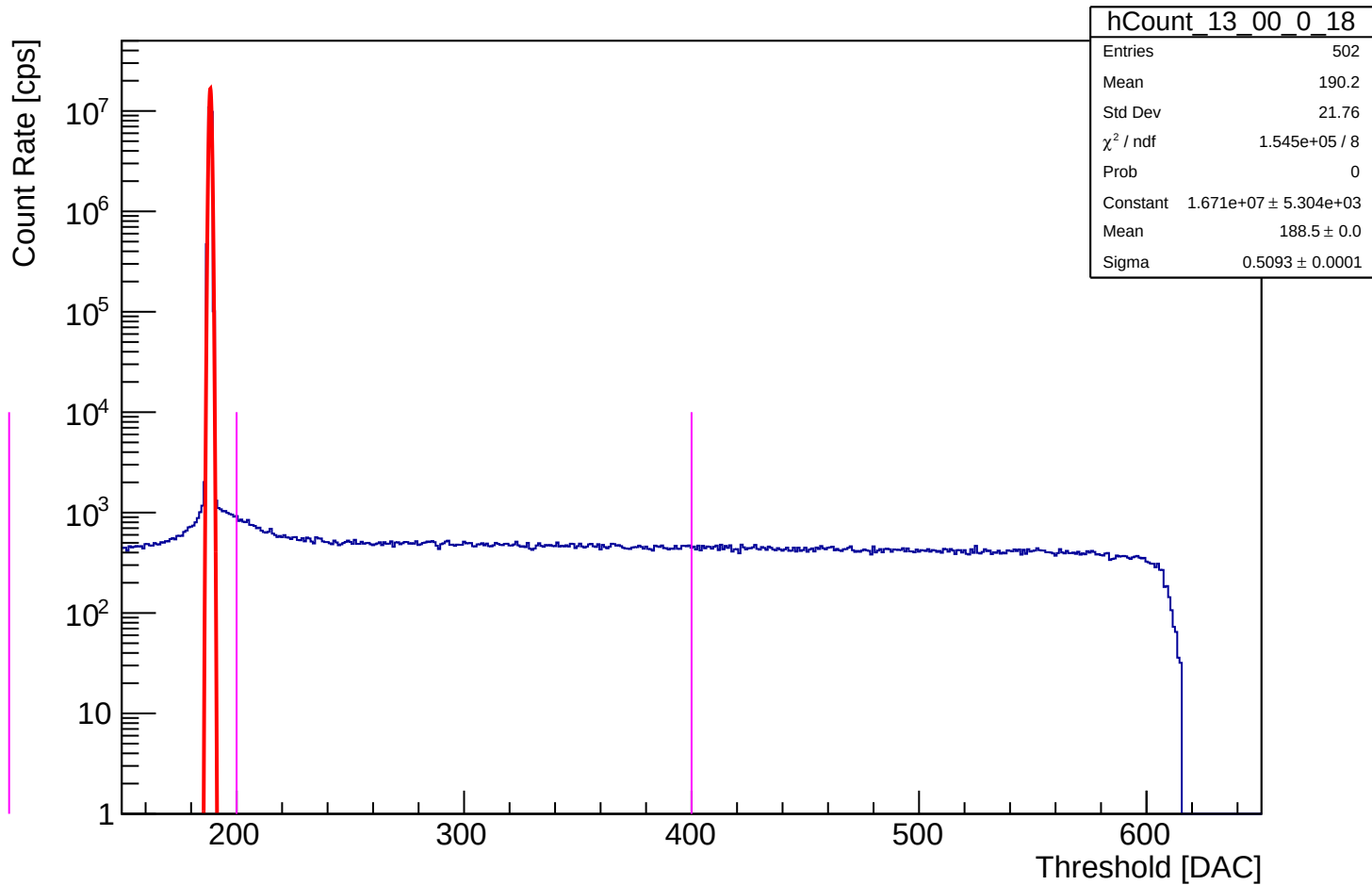
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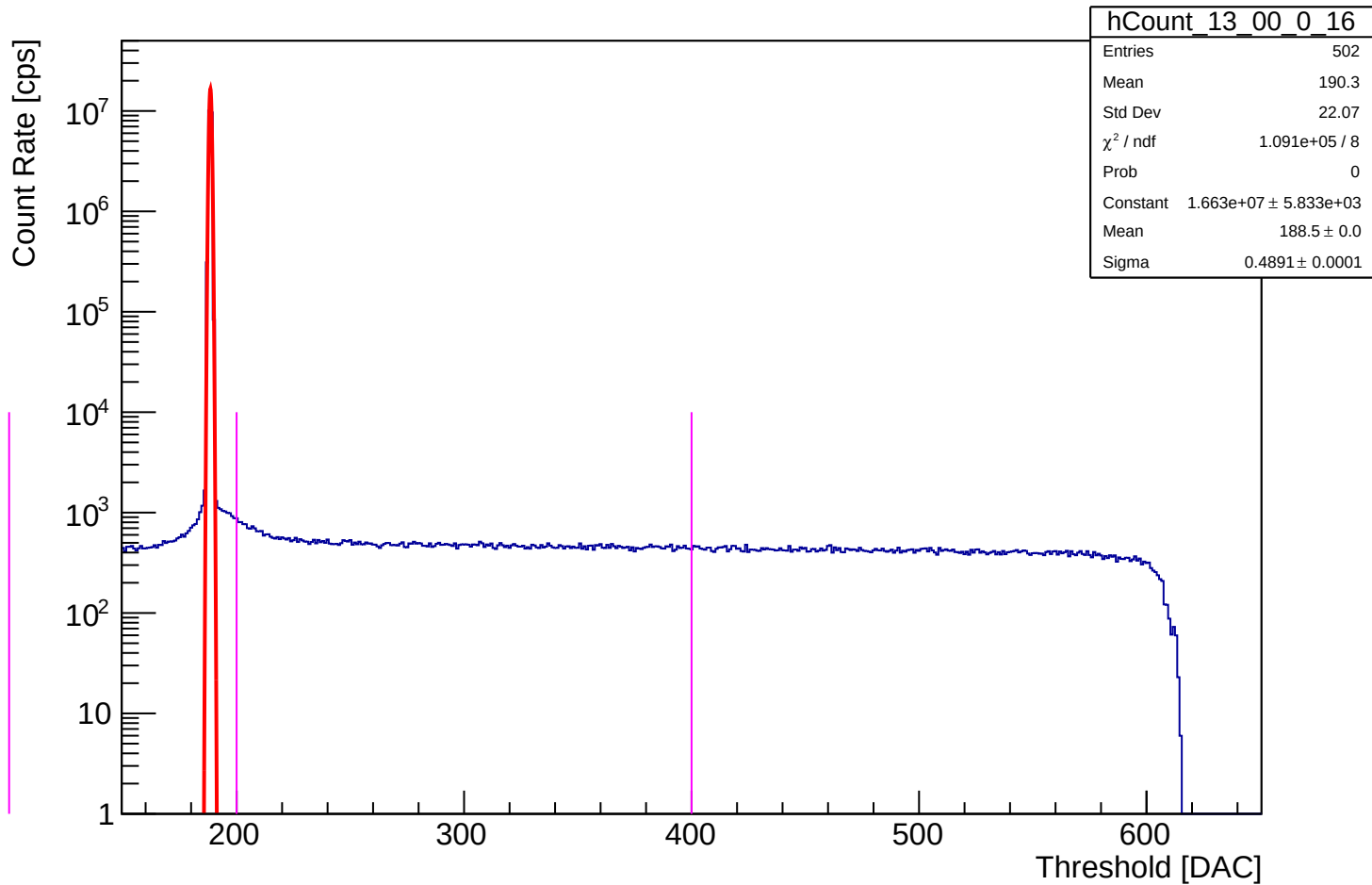
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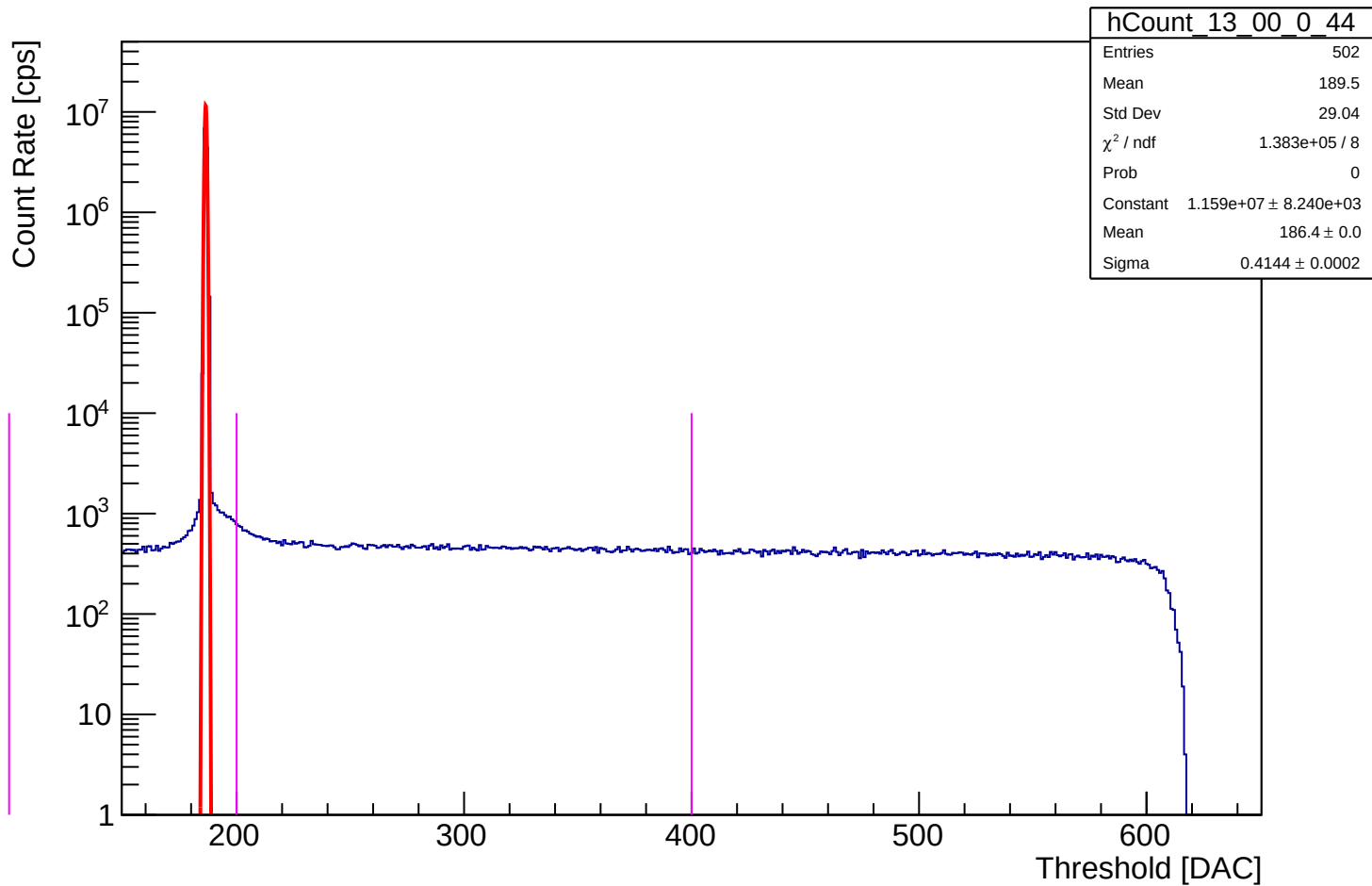
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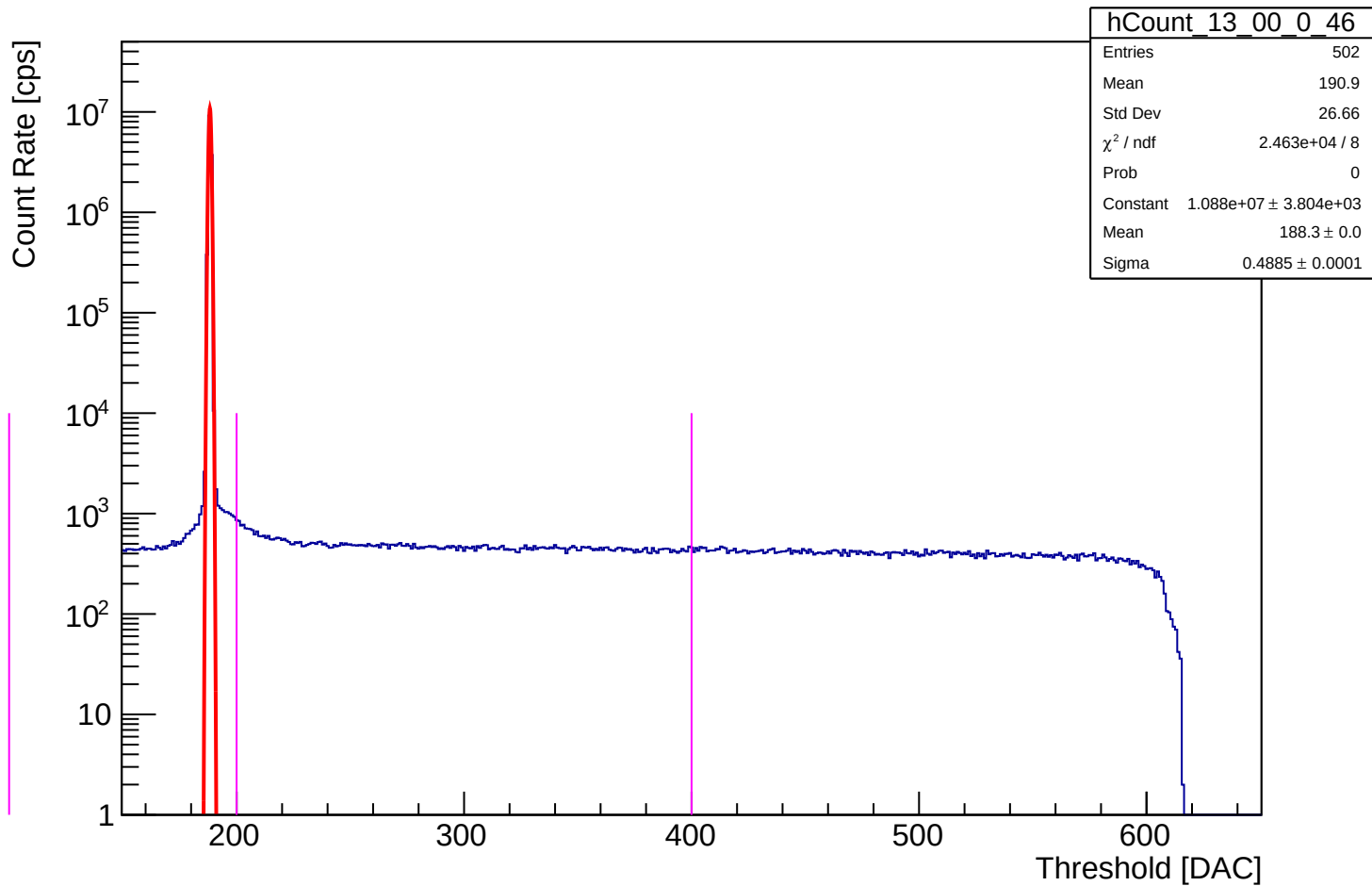
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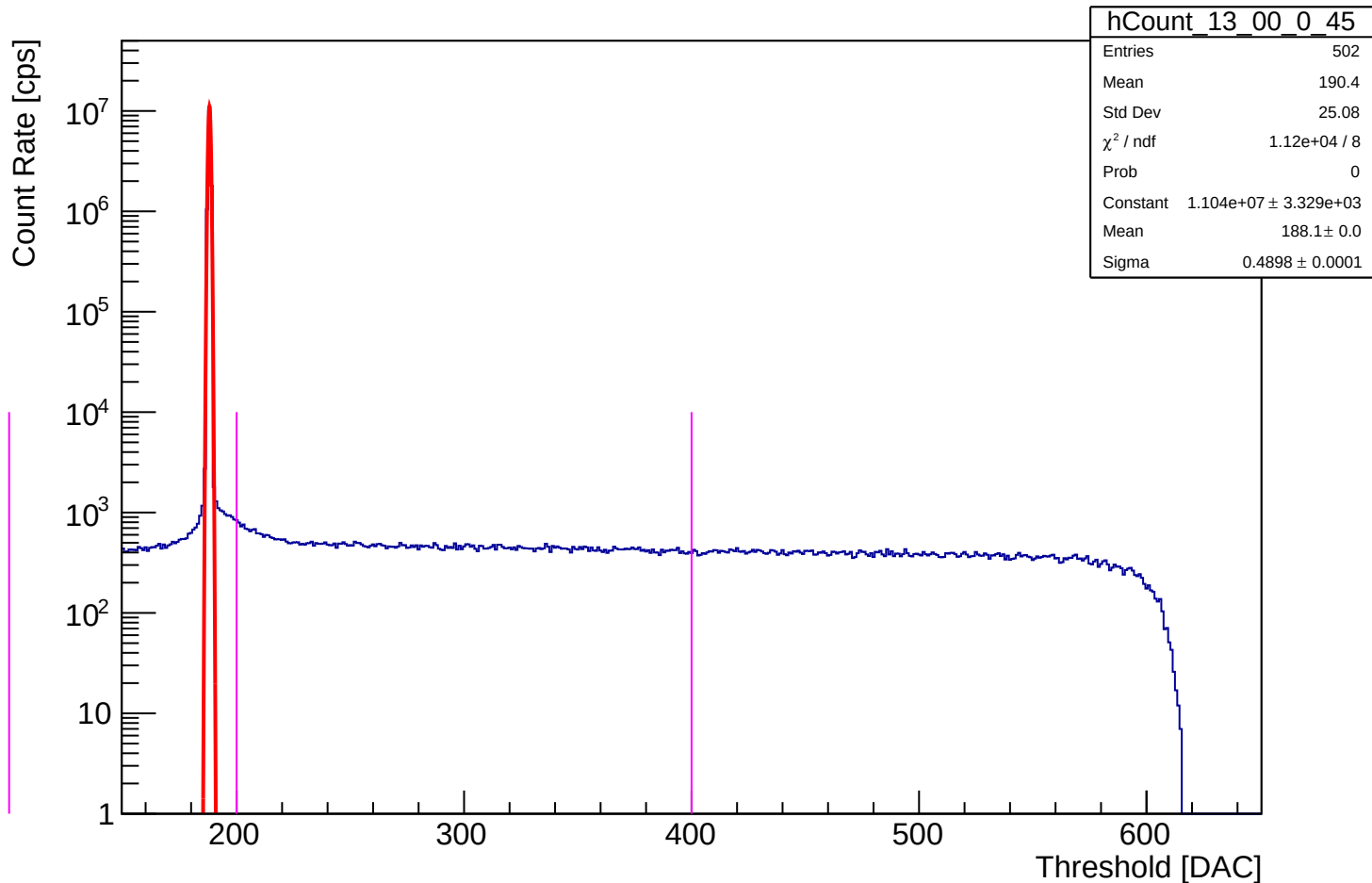
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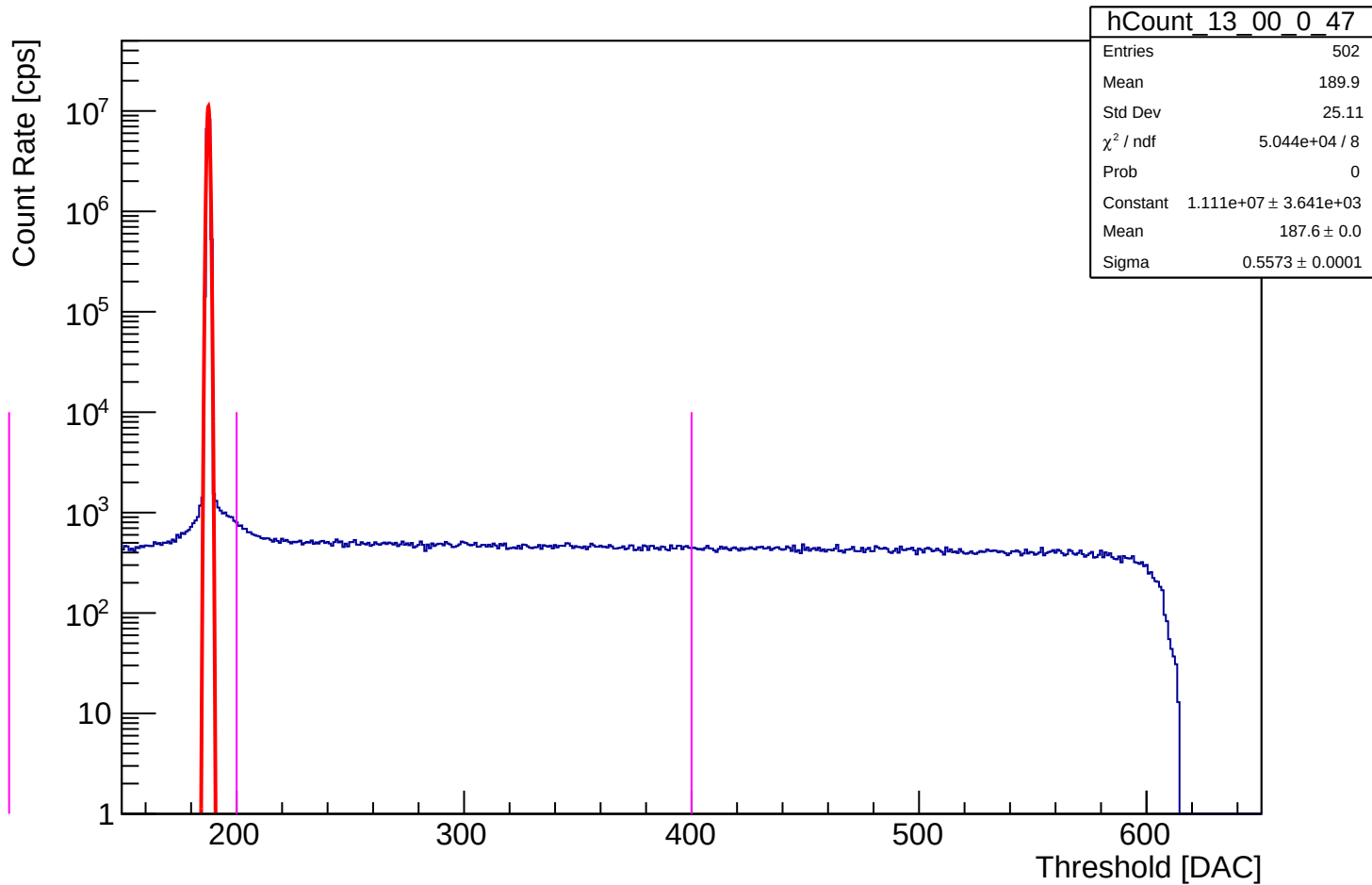
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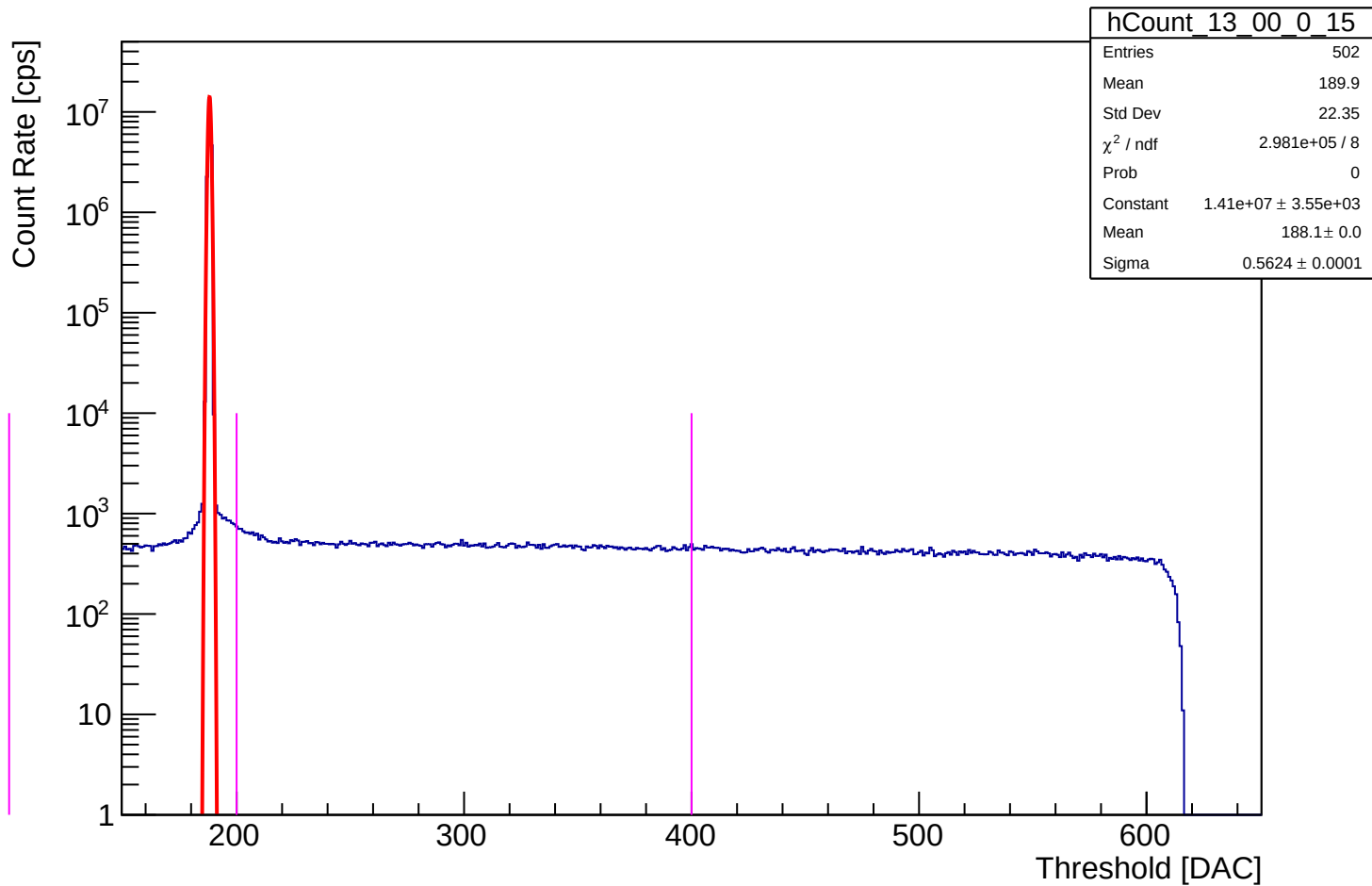
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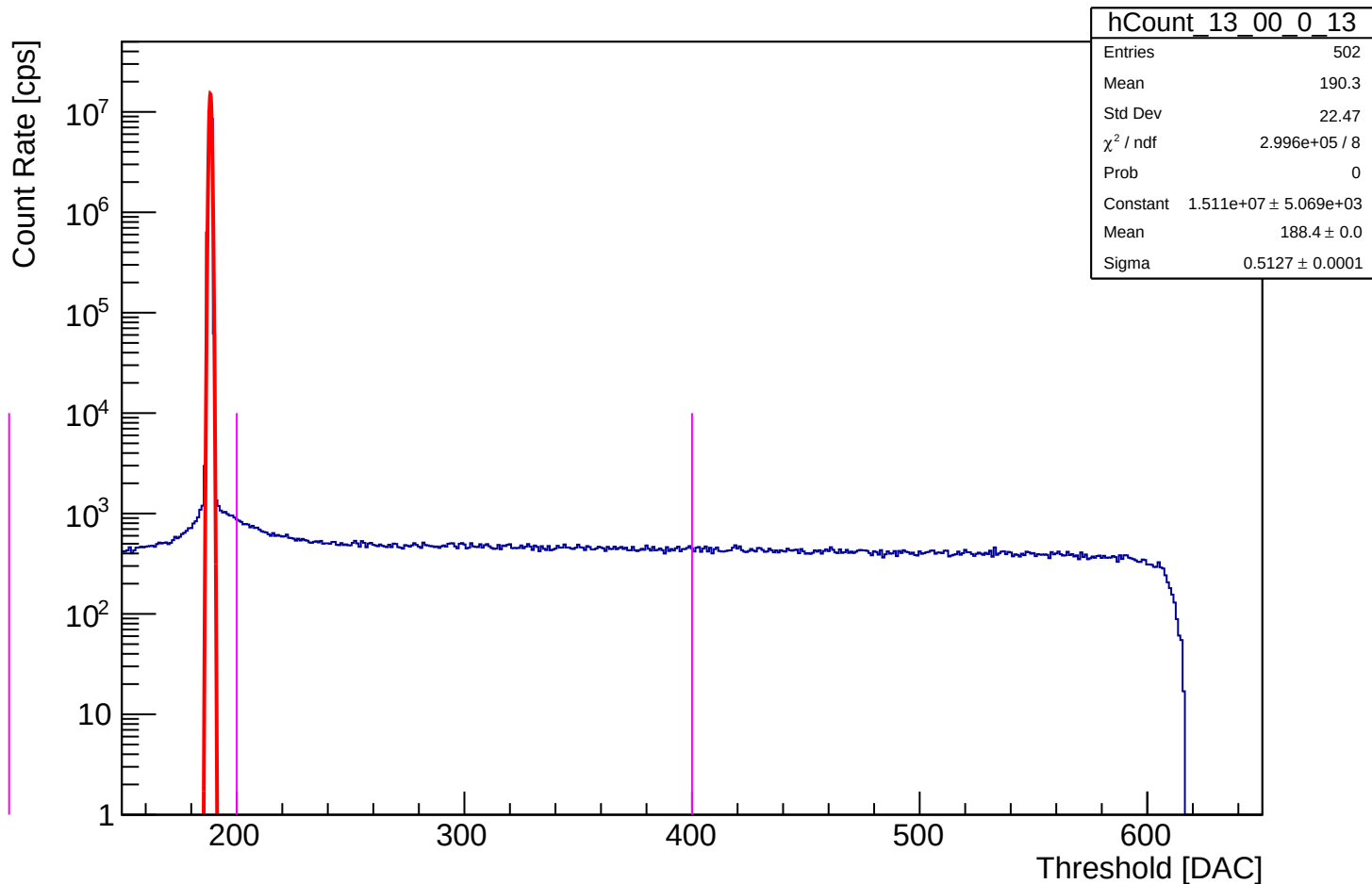
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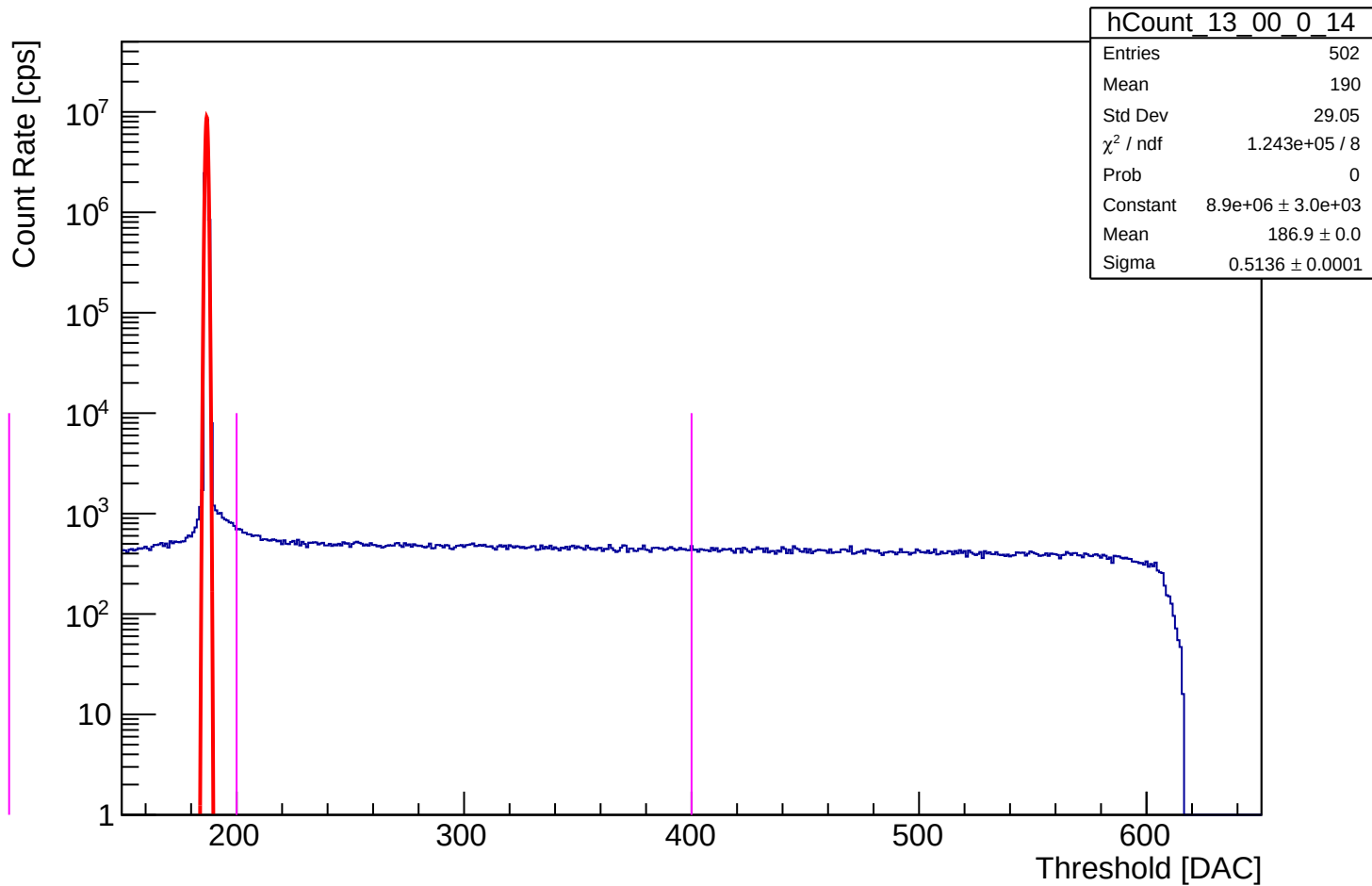
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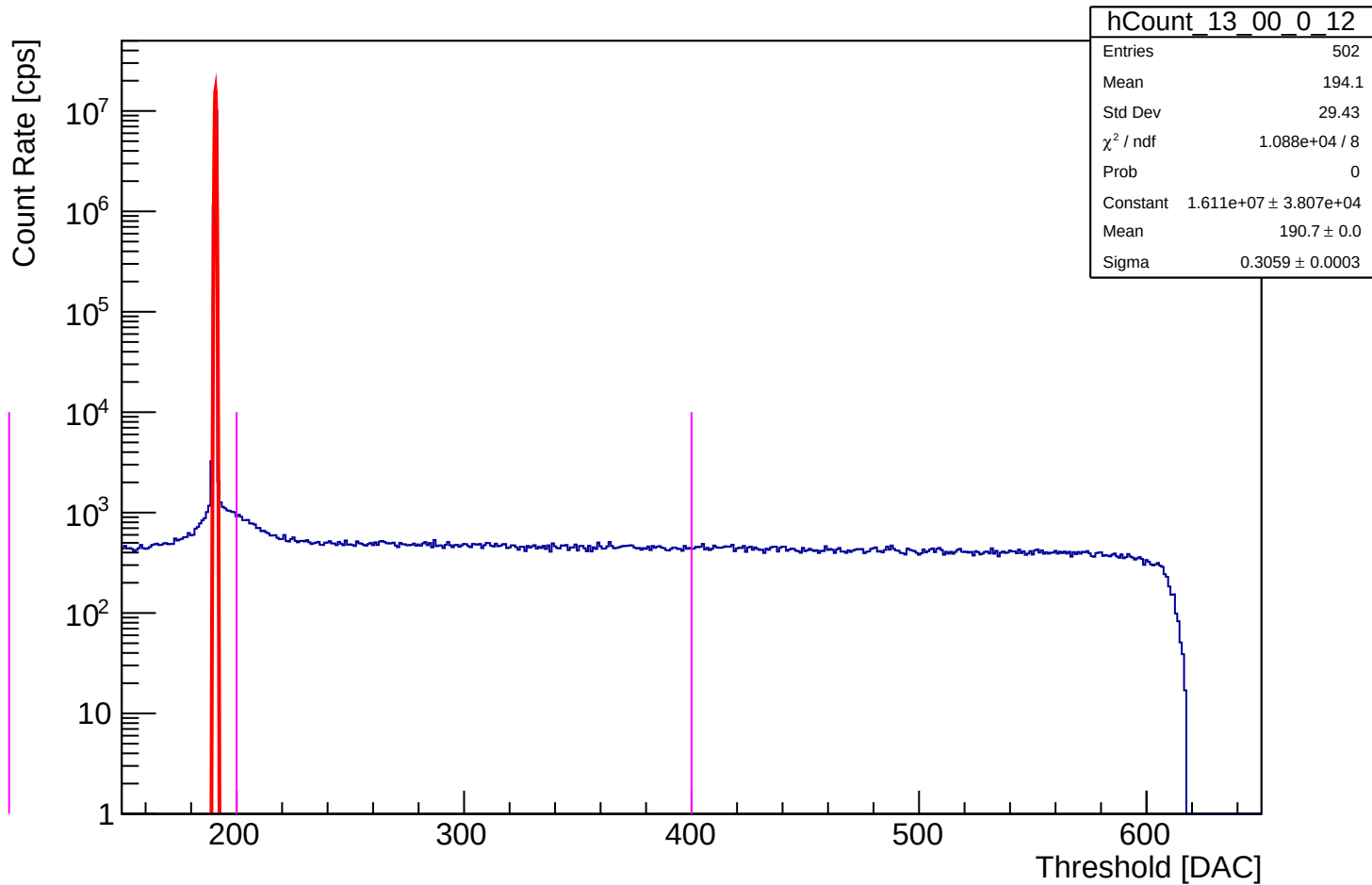
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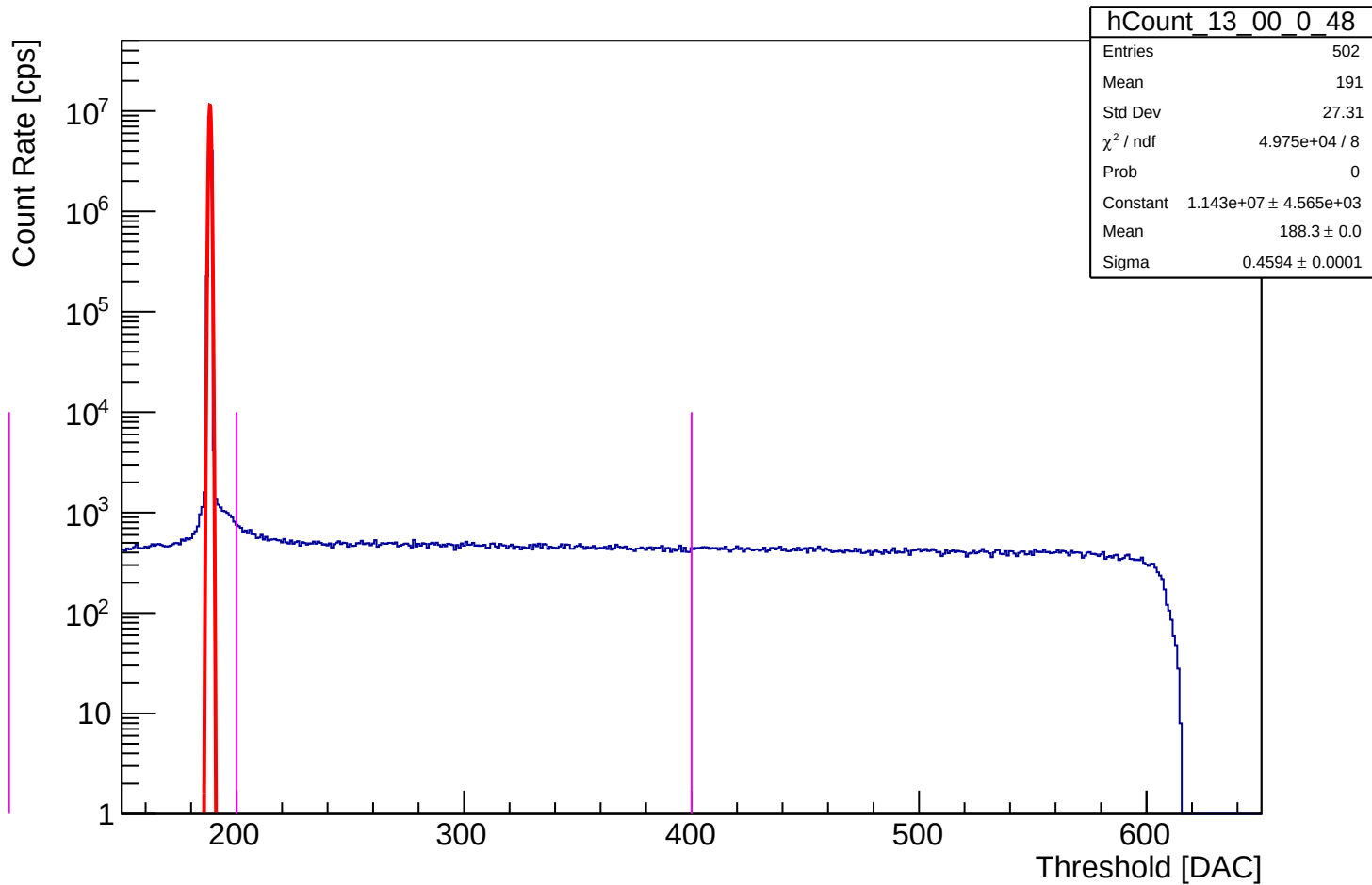
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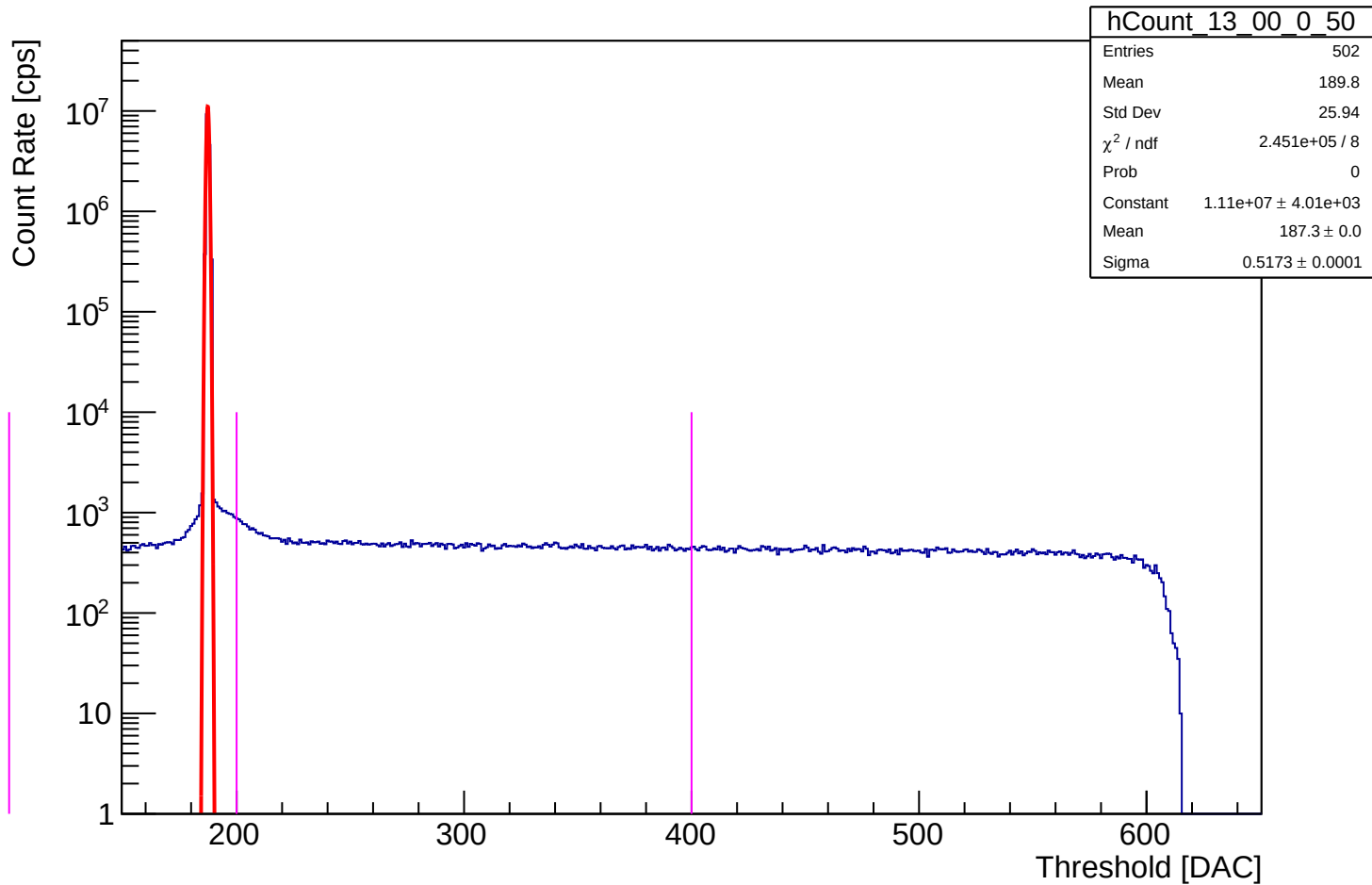
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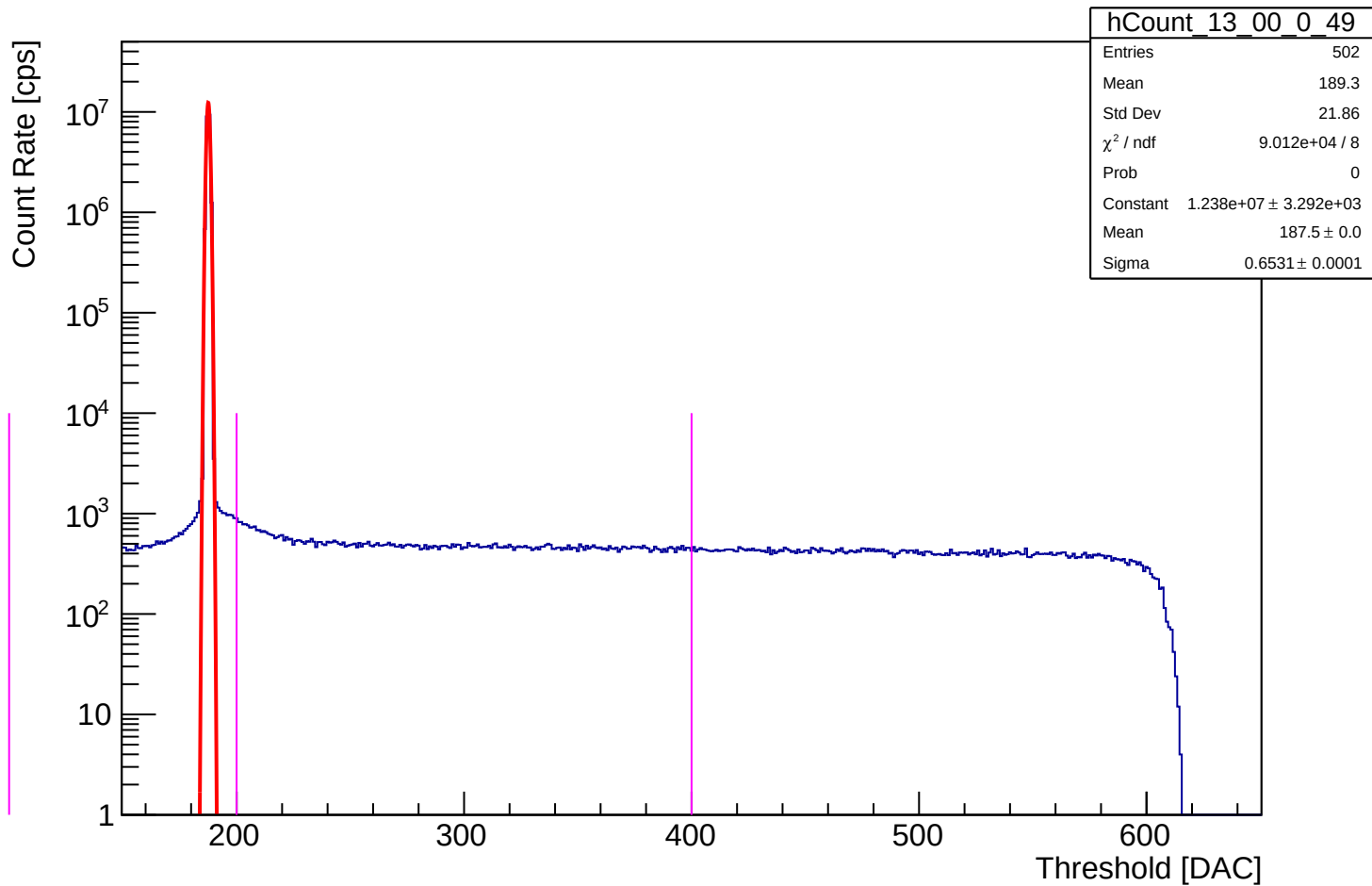
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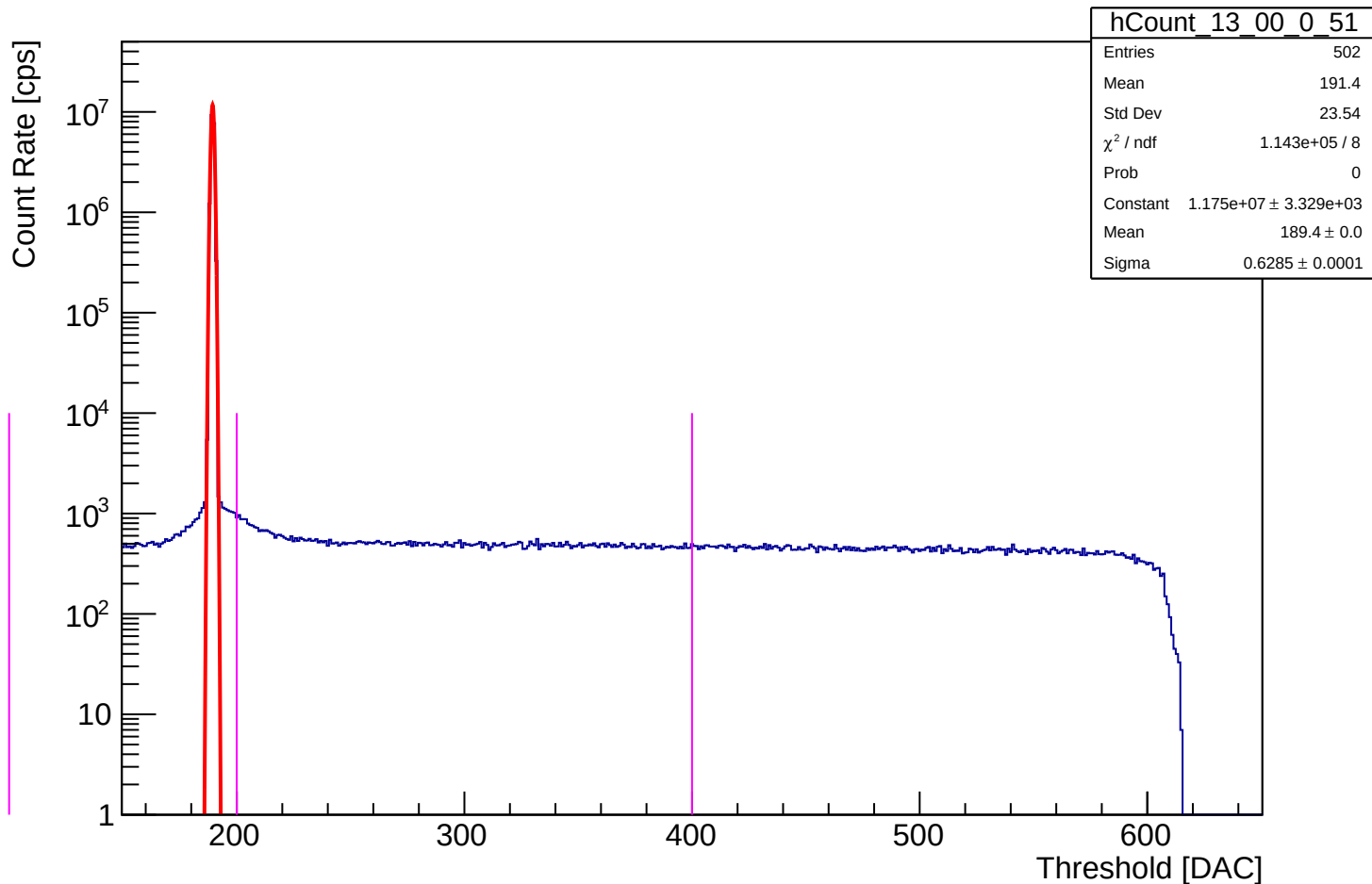
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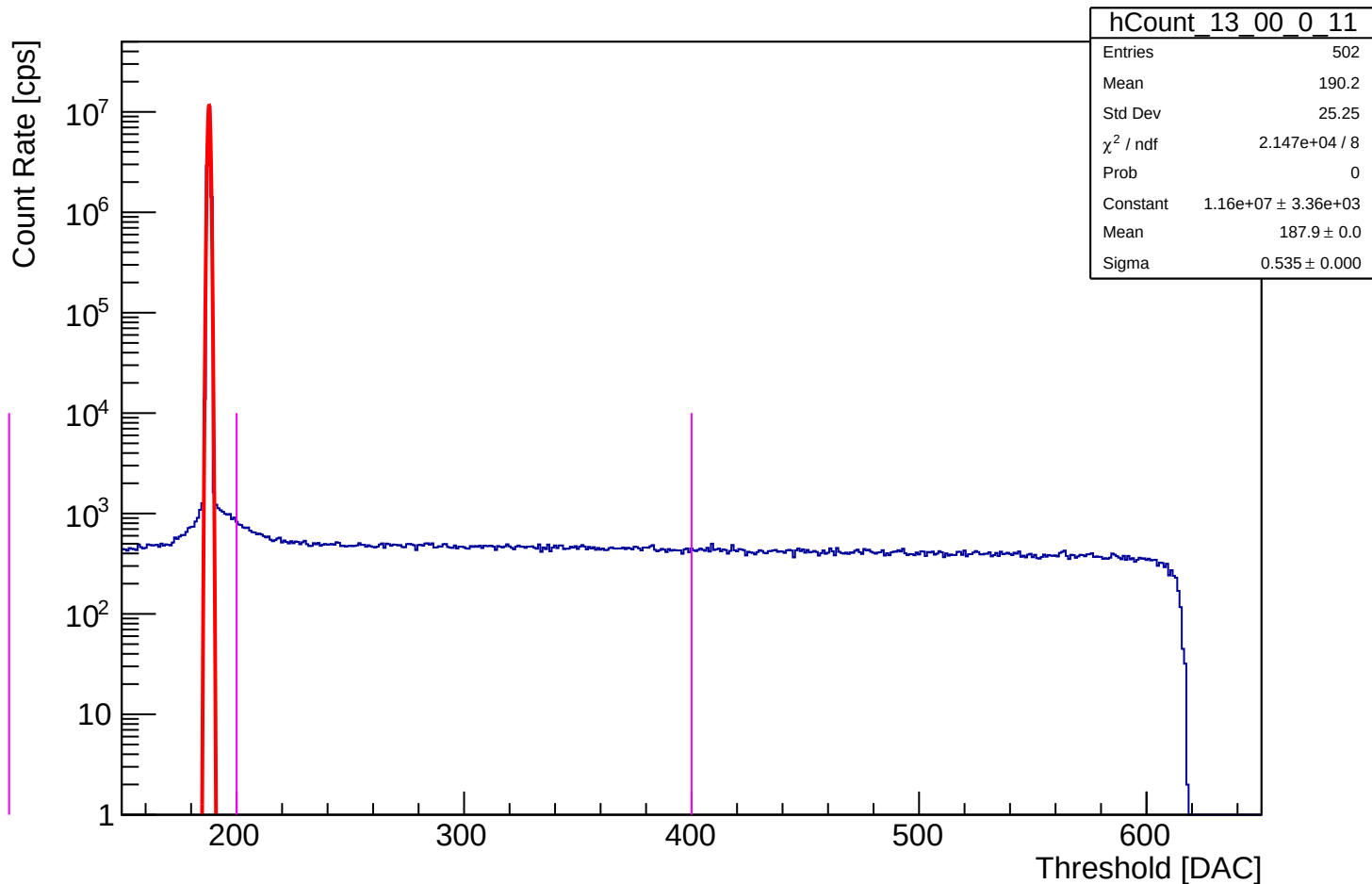
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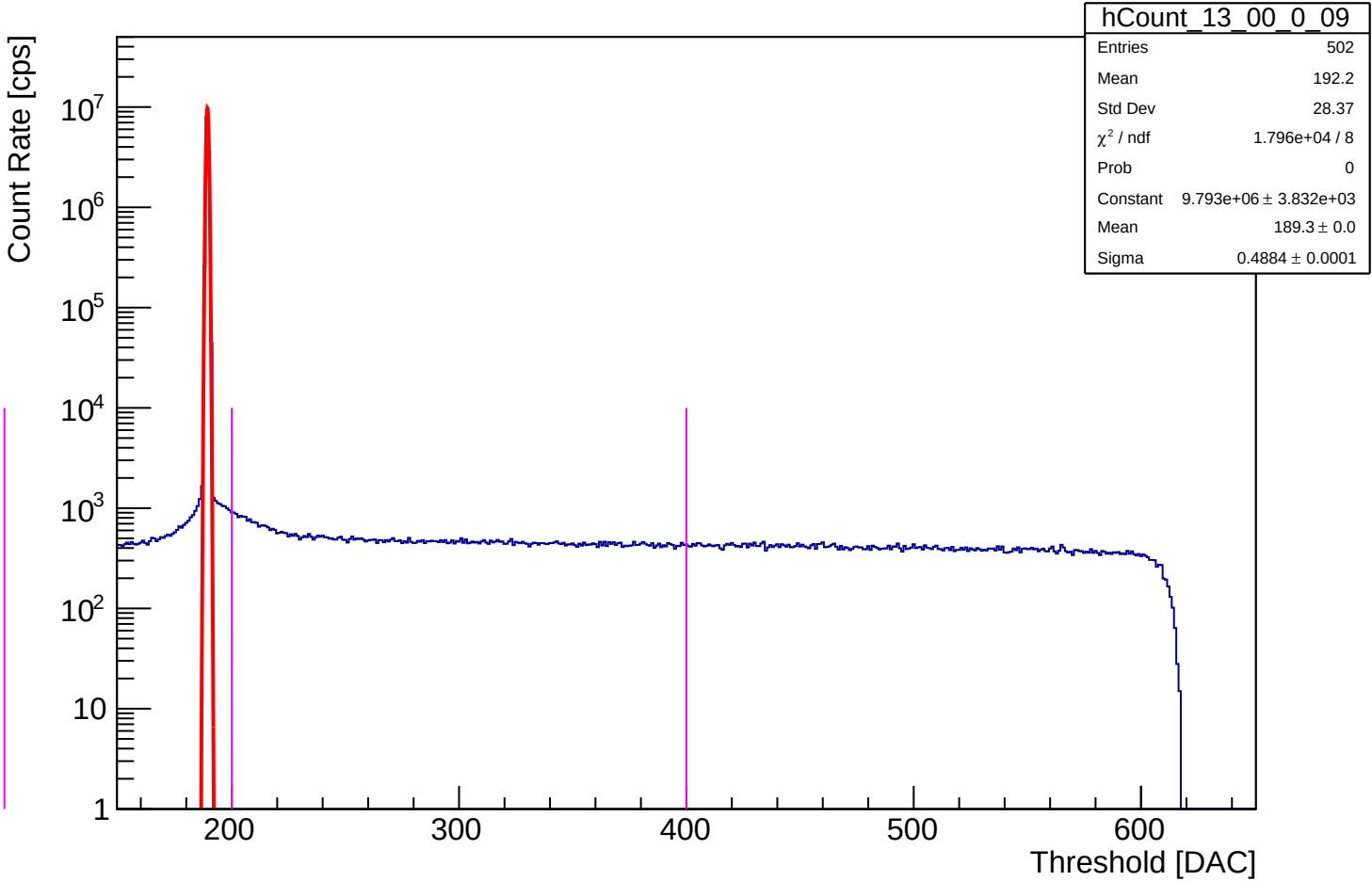


Row 1 Tile 1 Pmt 1 Pixel 40 Slot 13 Fiber 0 Asic 0 Channel 51

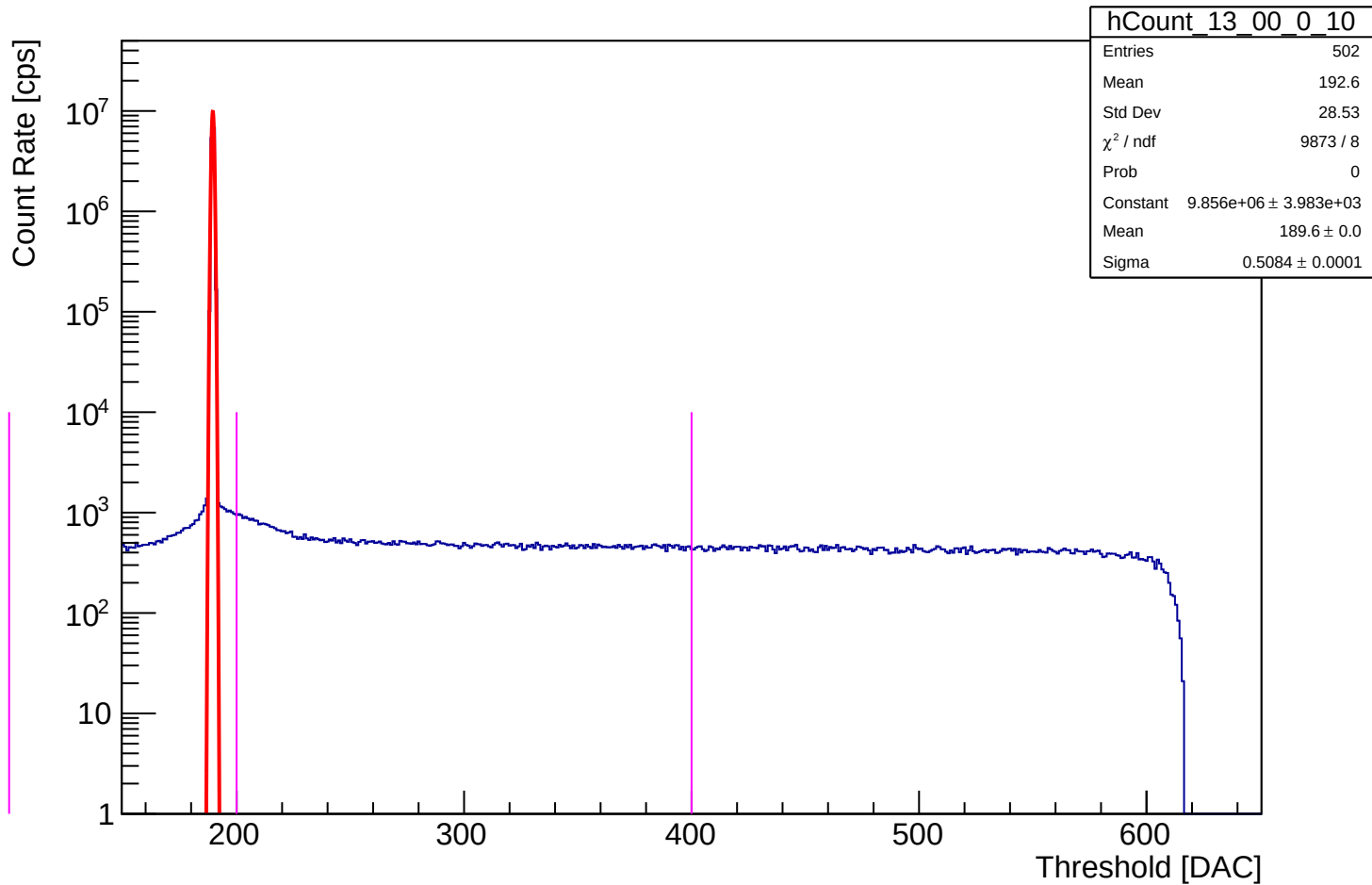


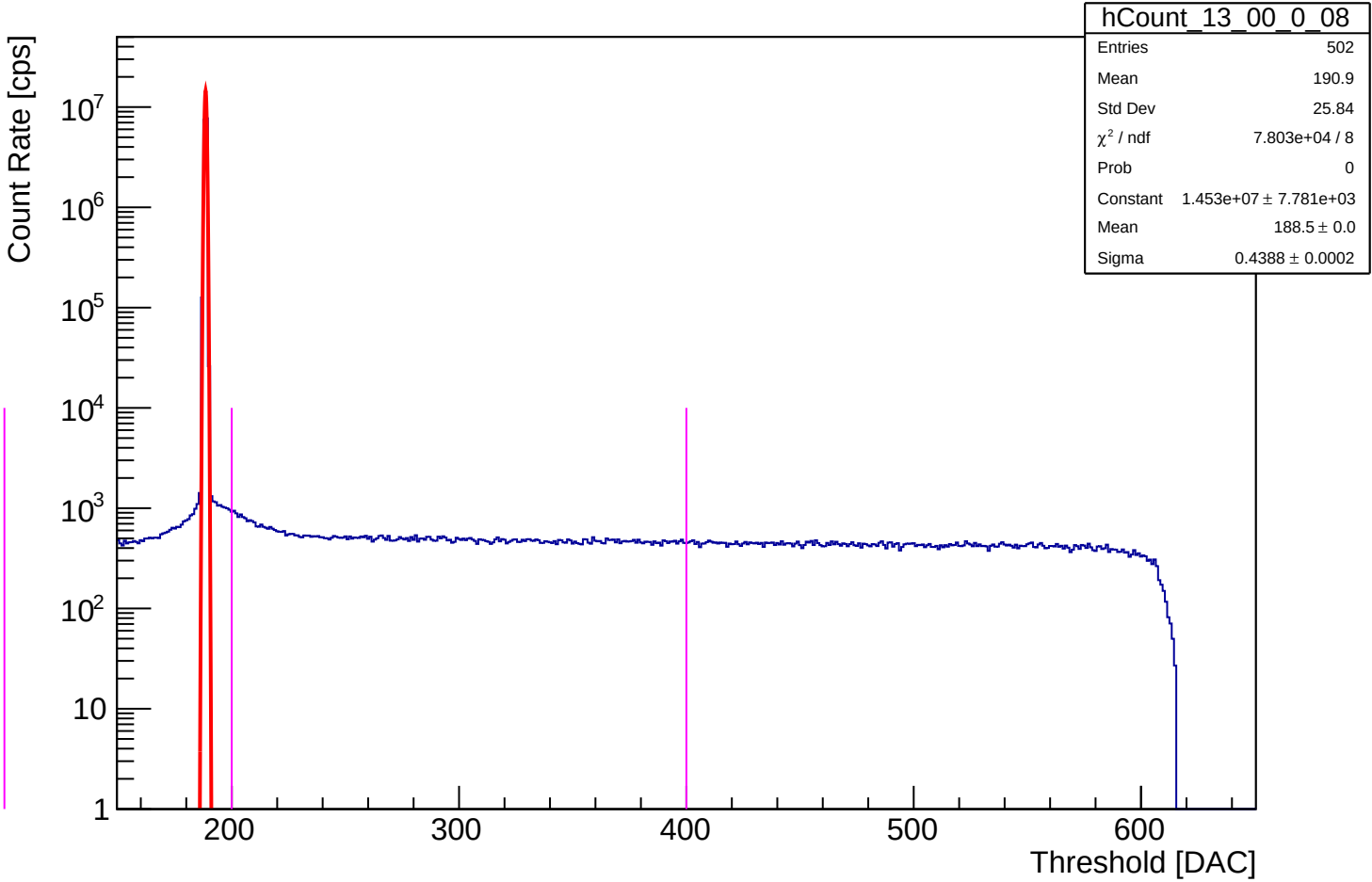
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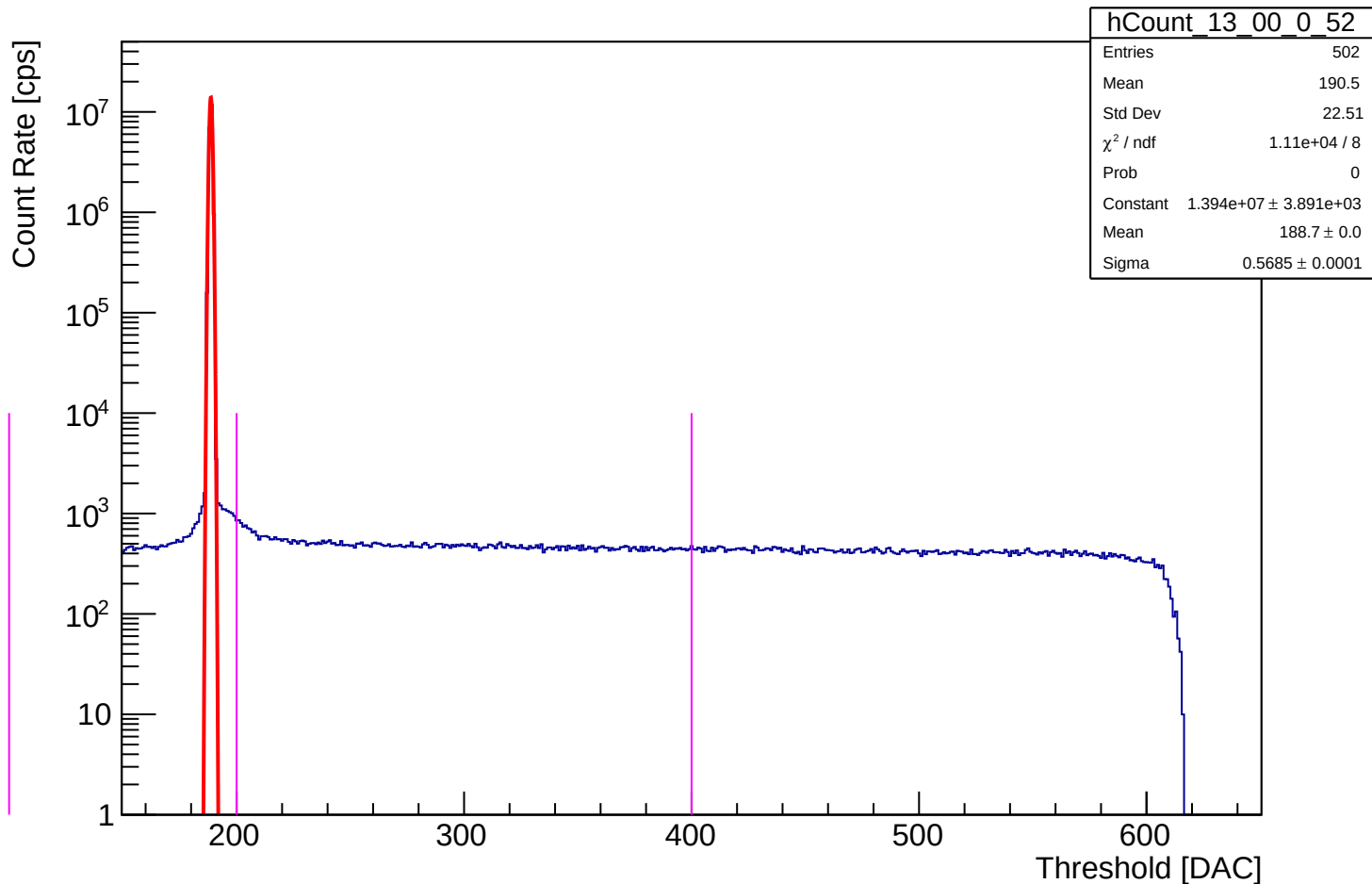


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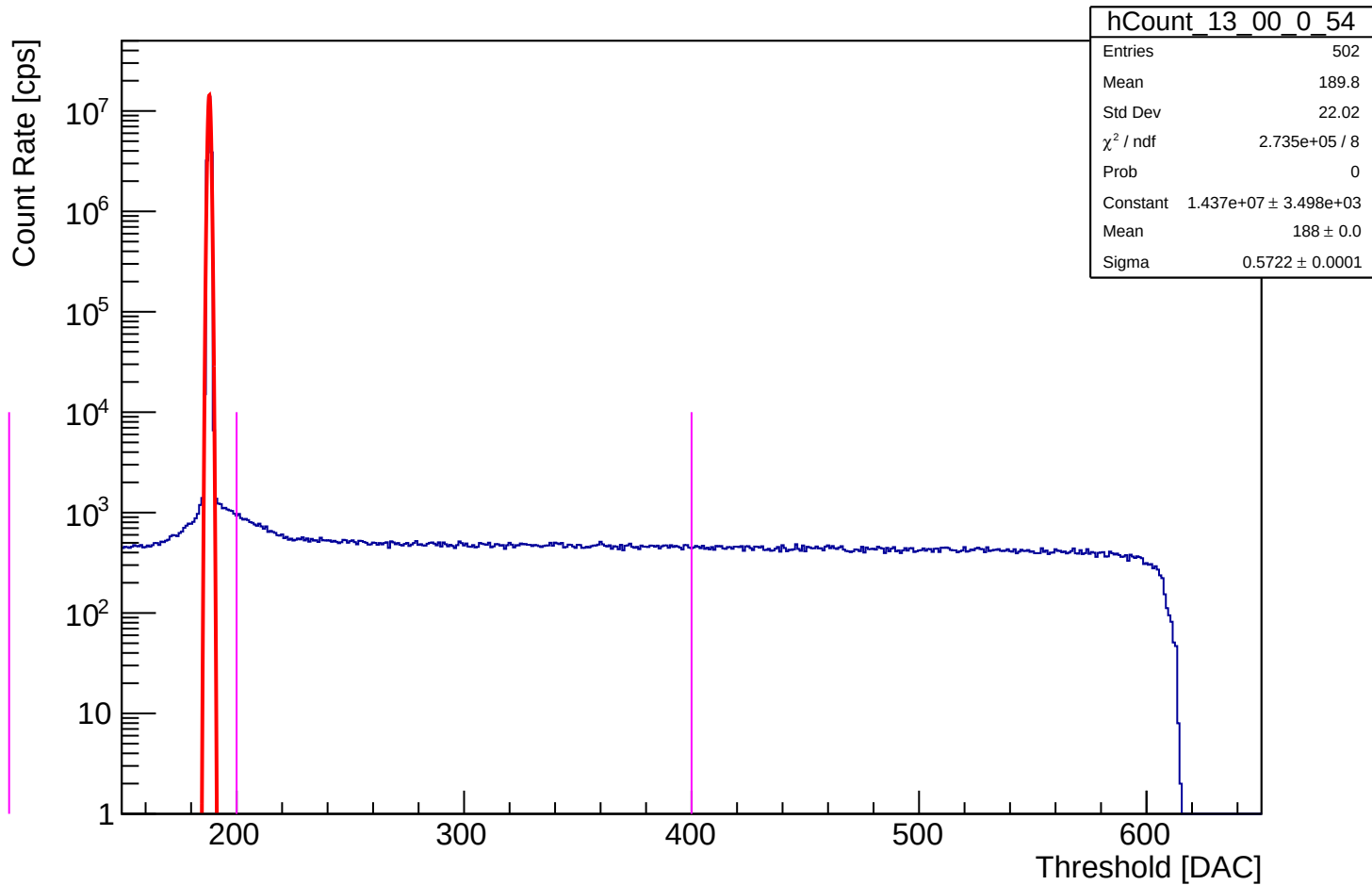




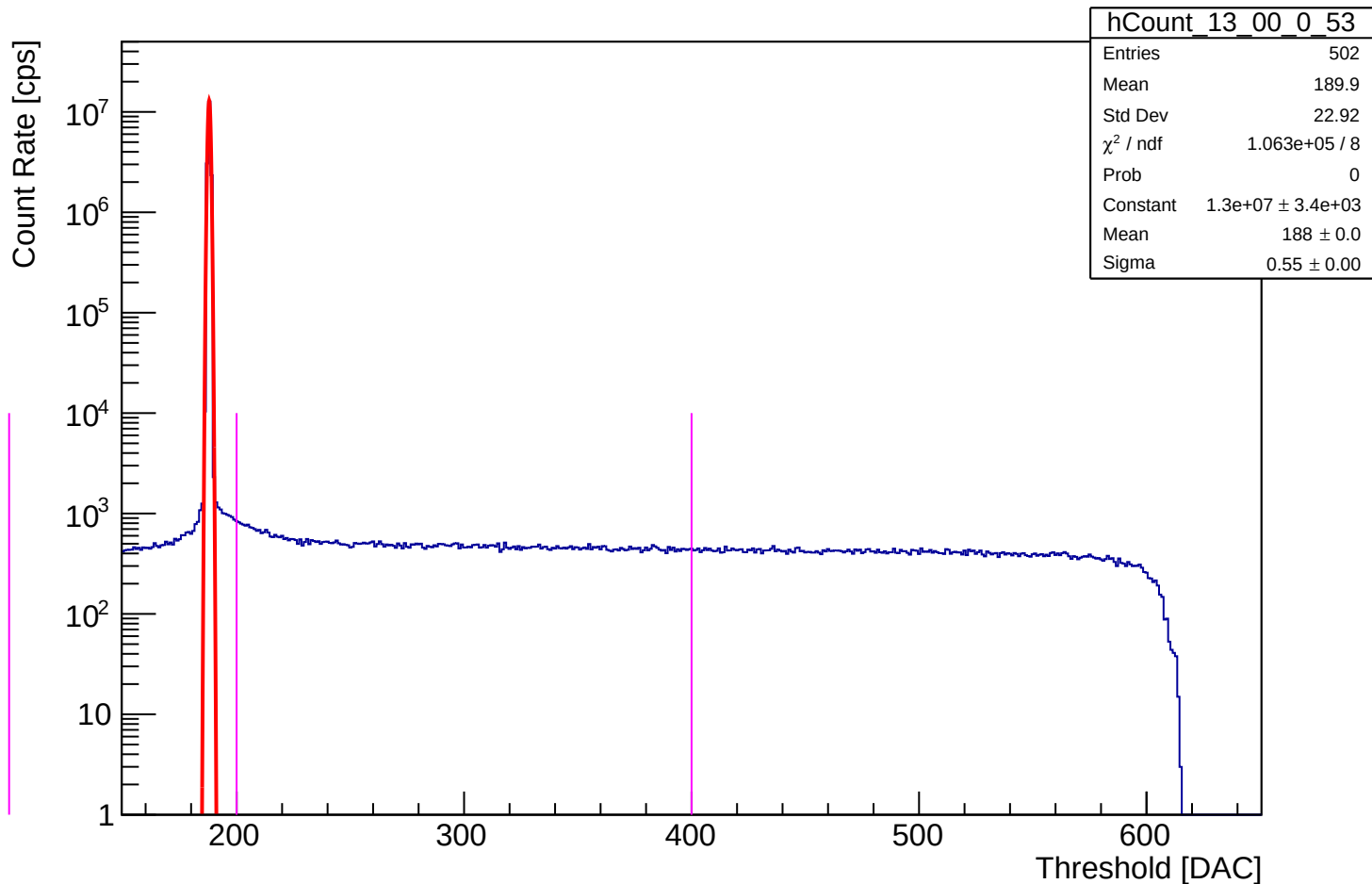
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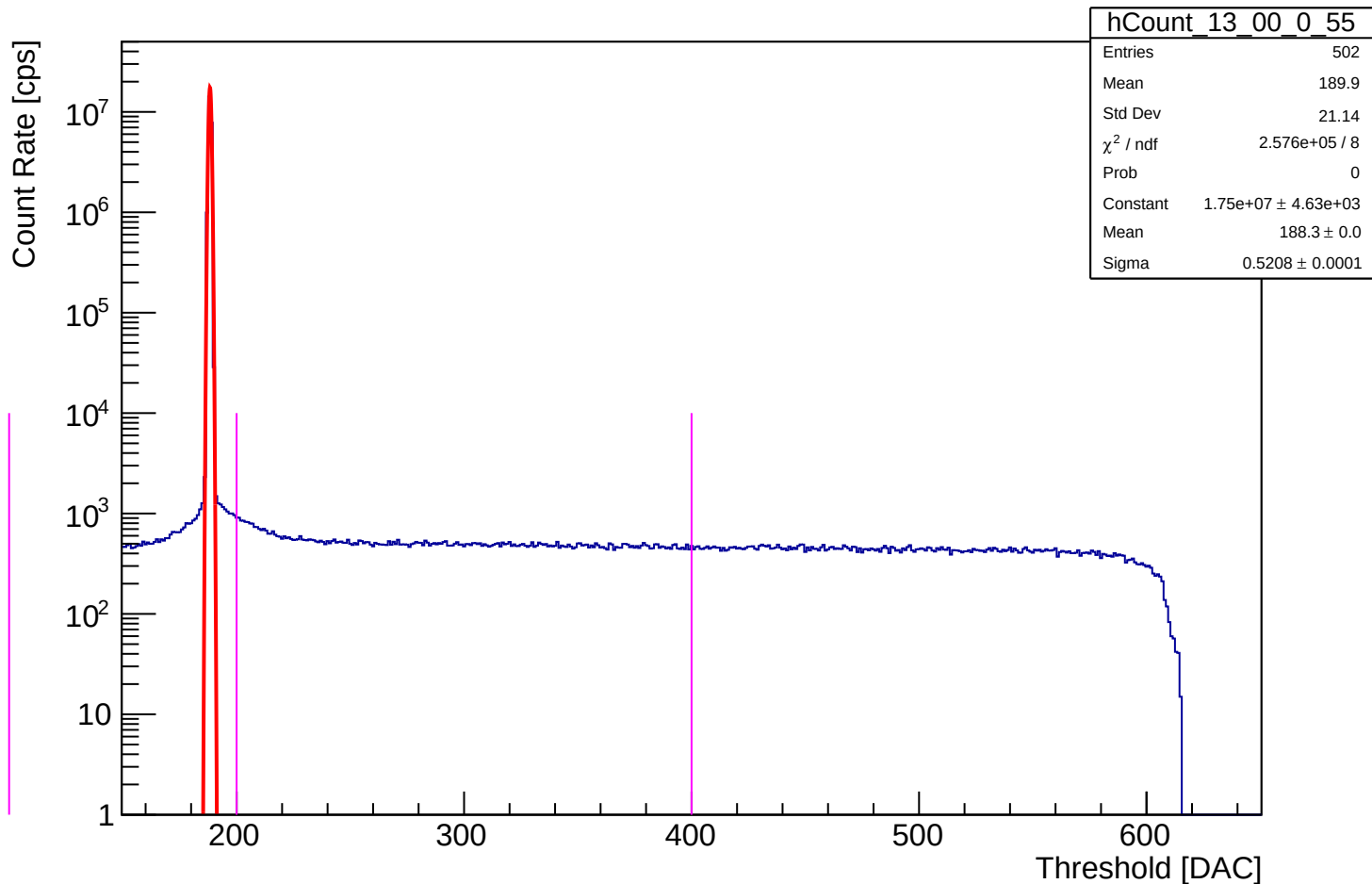
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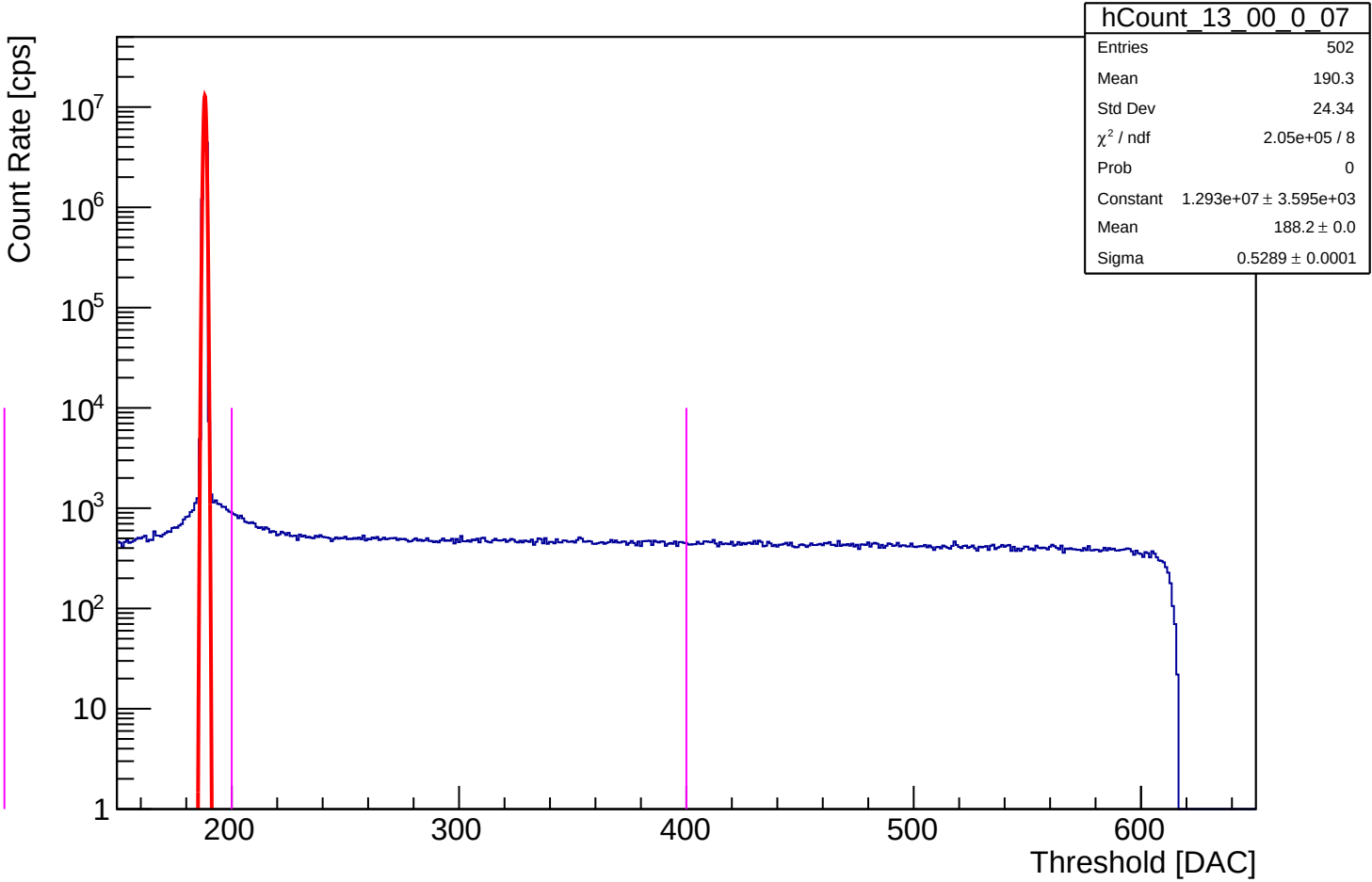


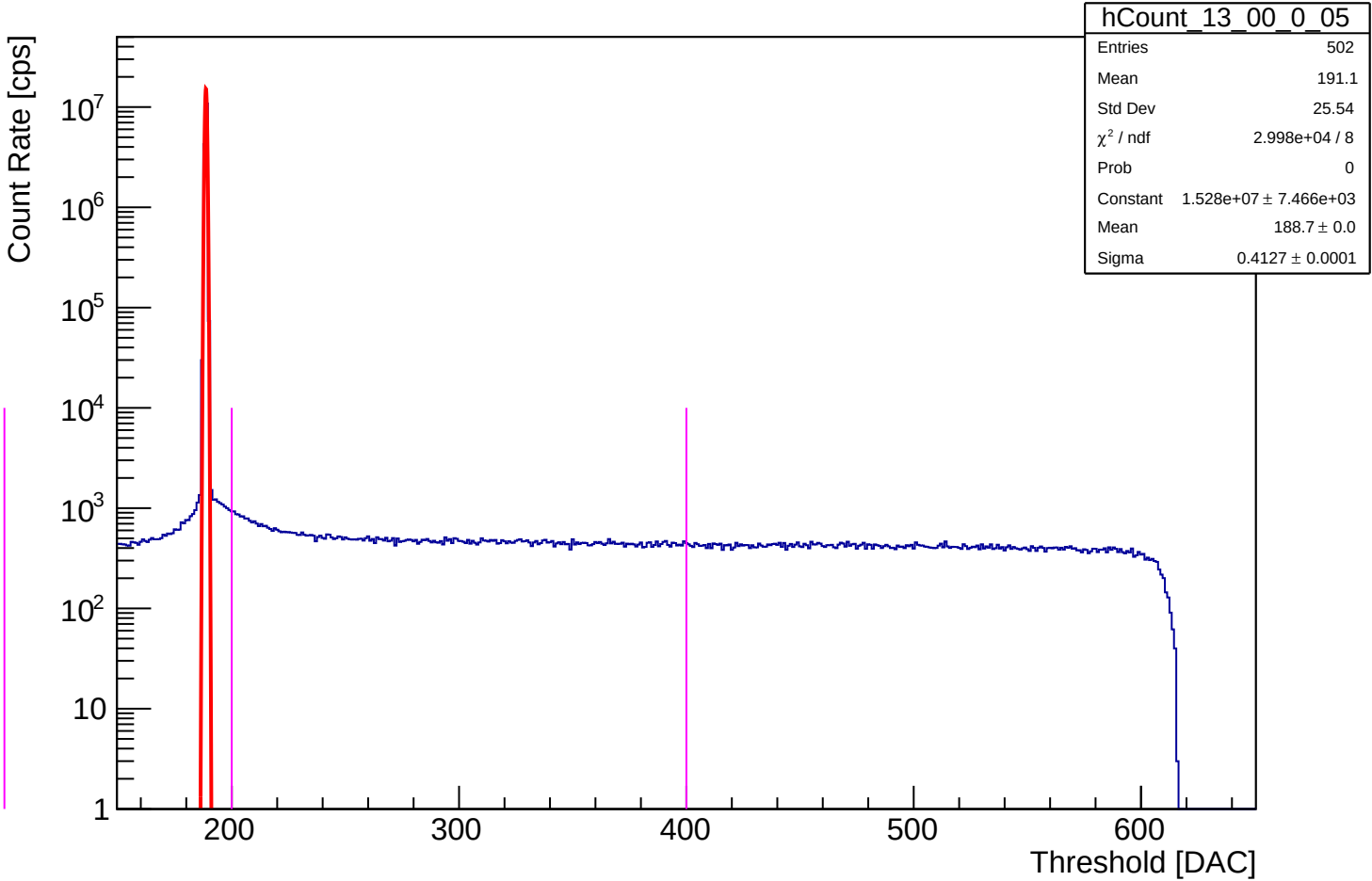
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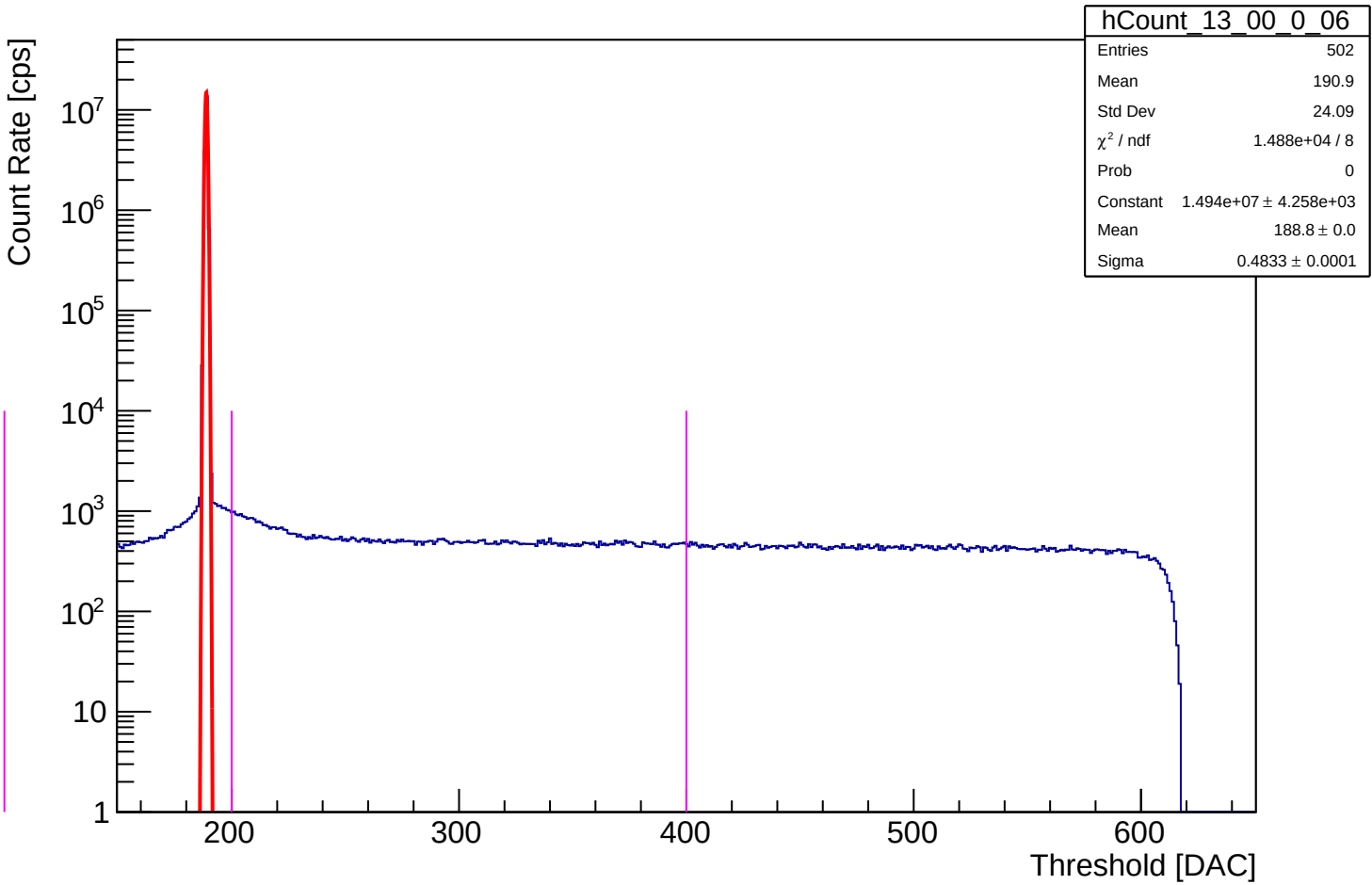


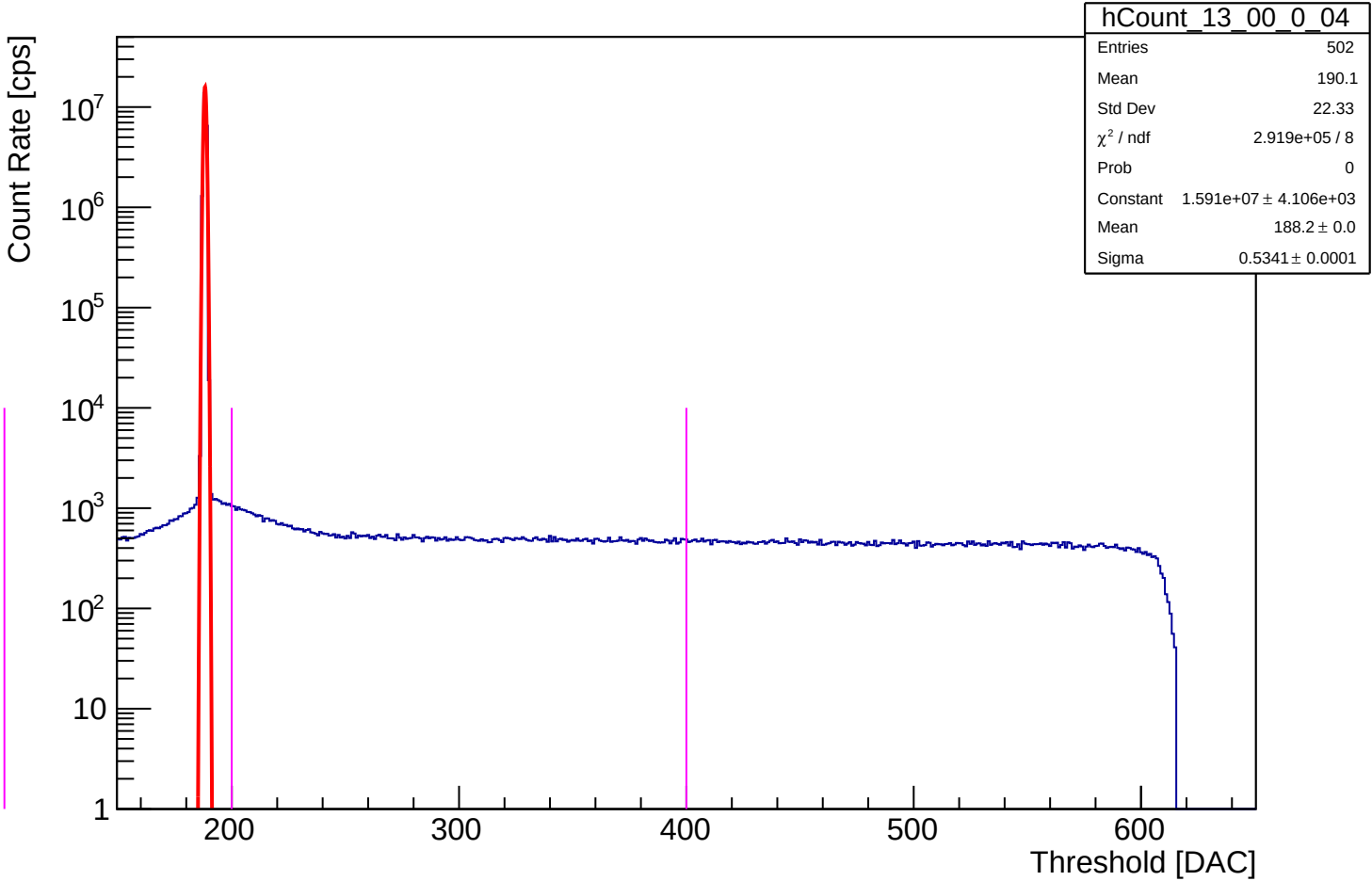
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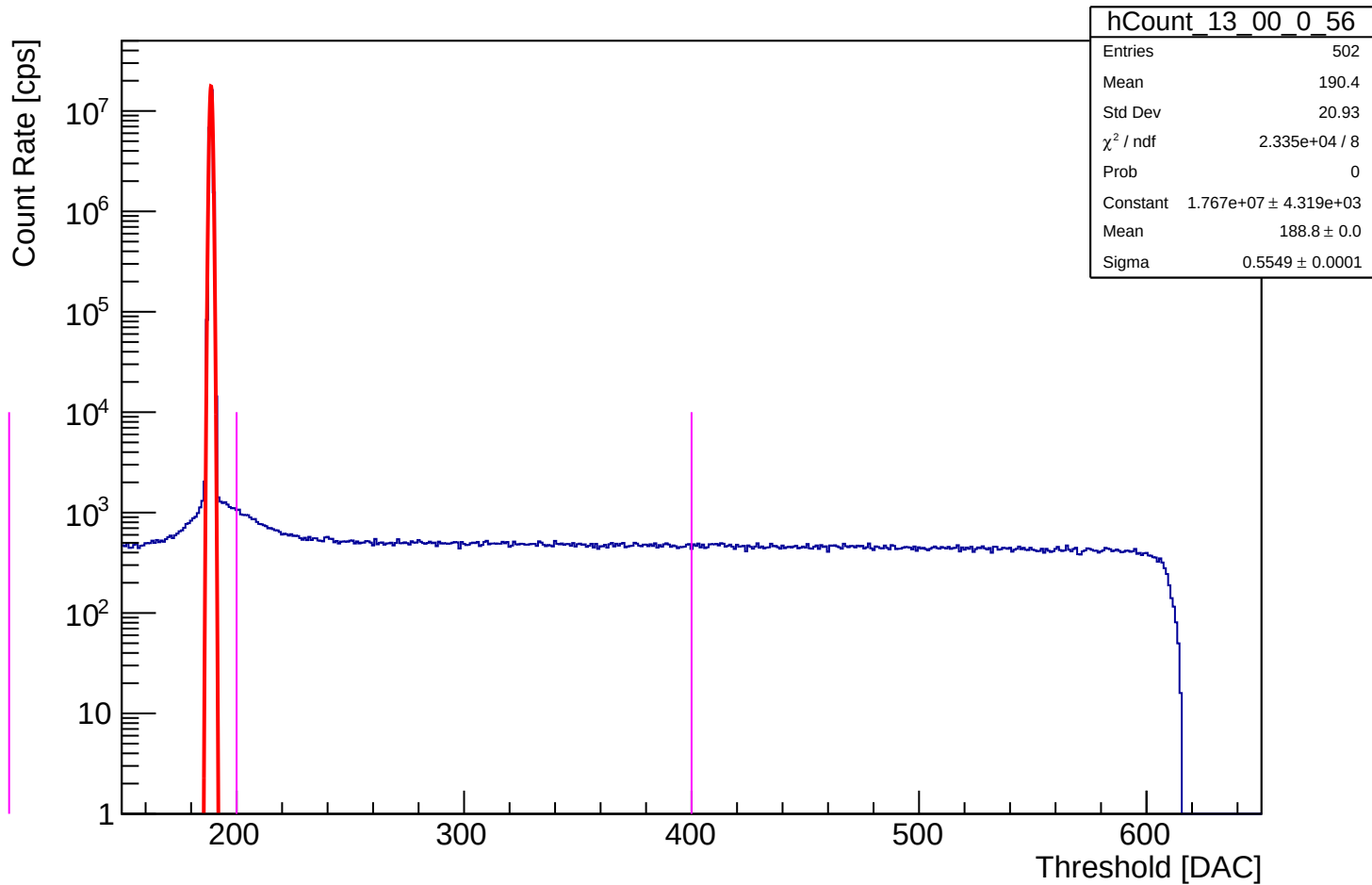




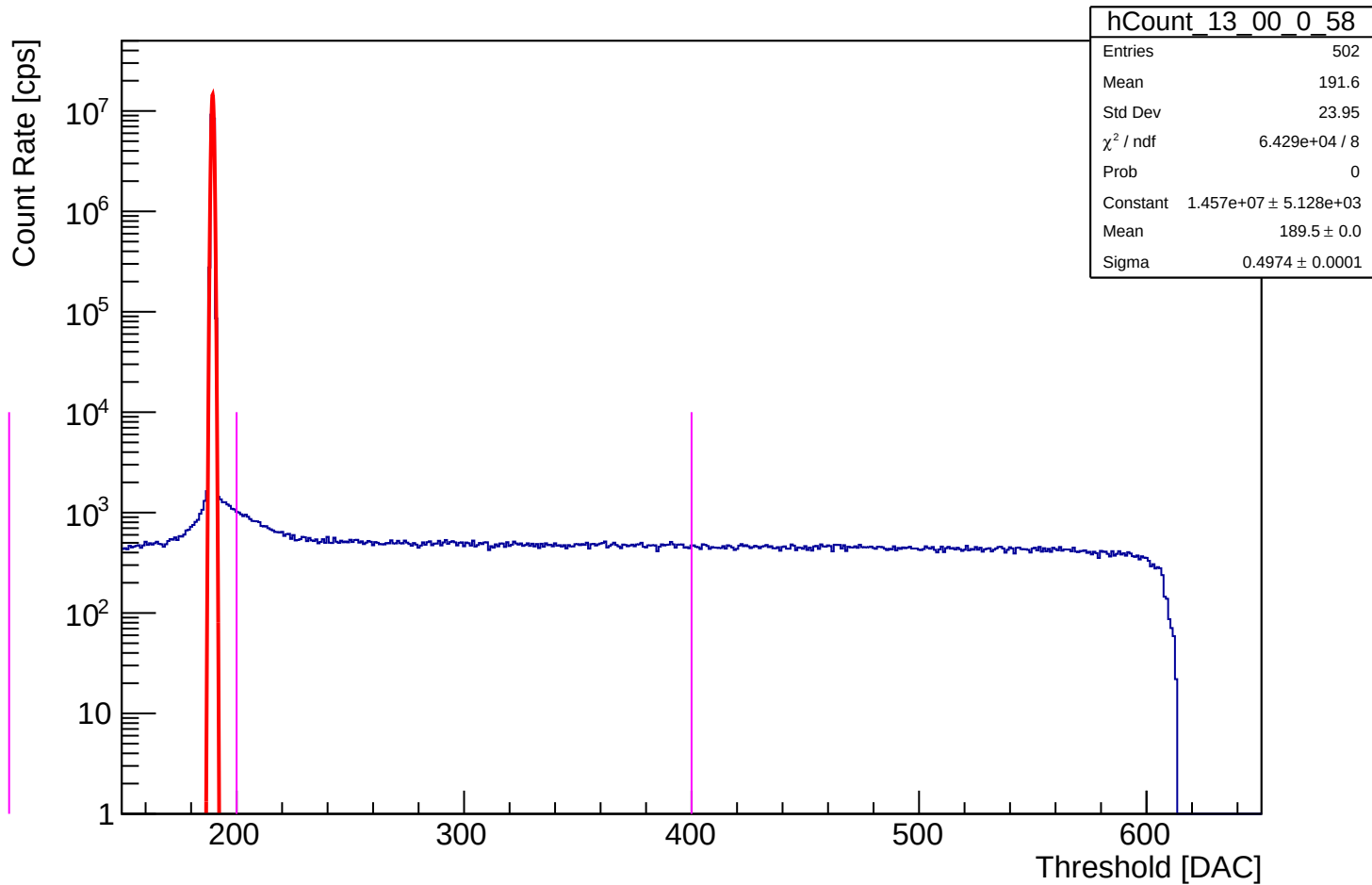




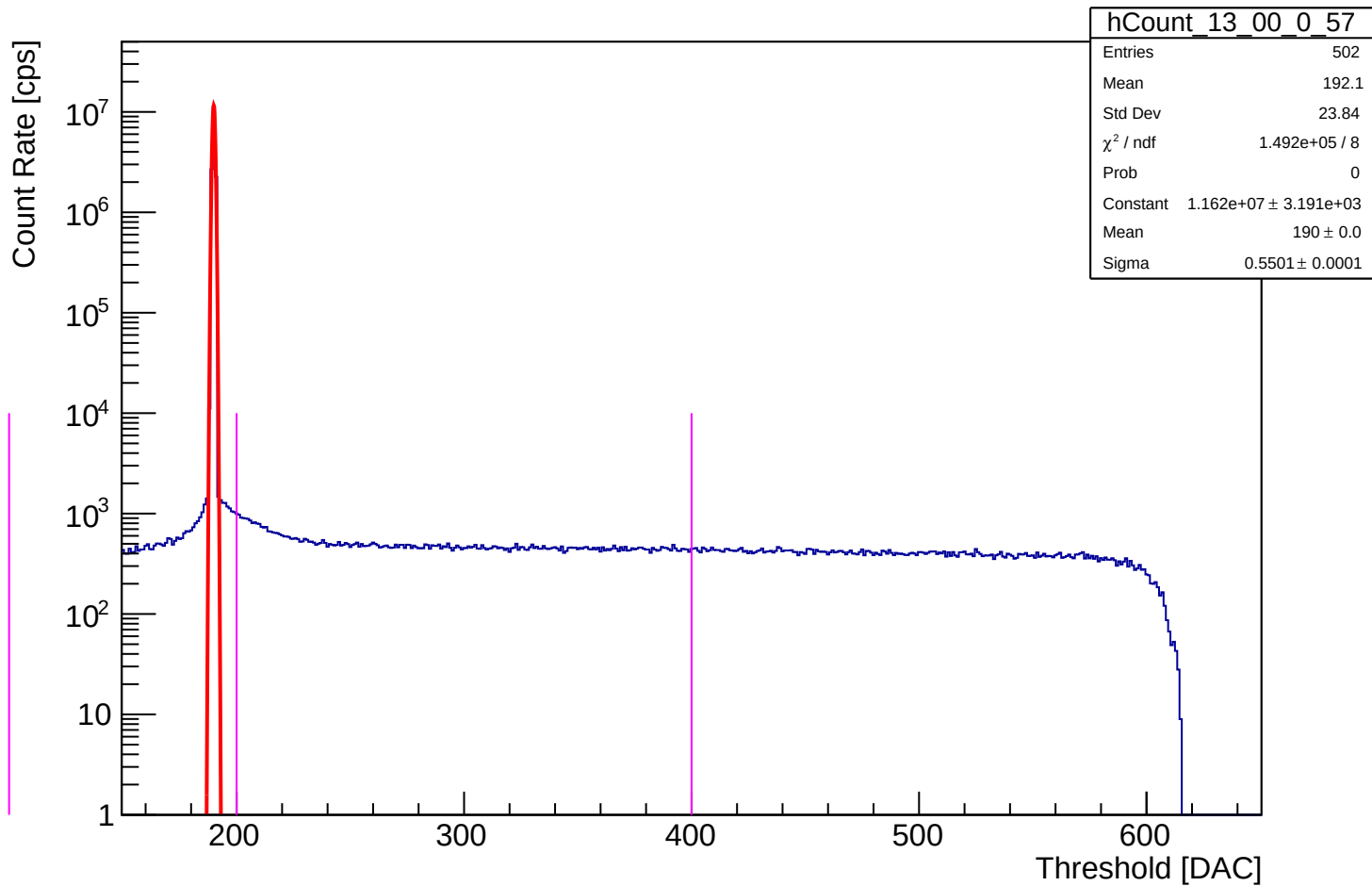
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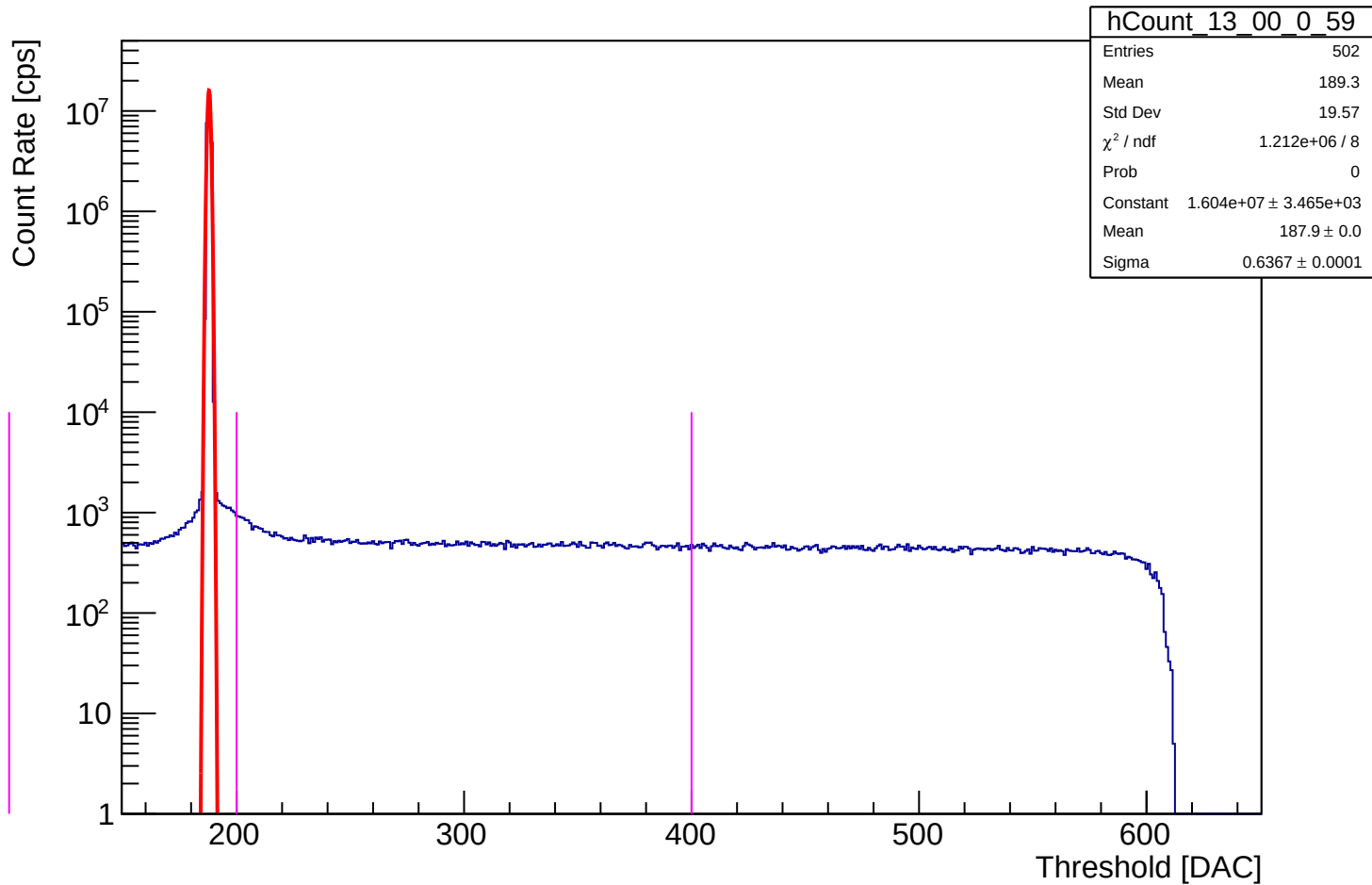
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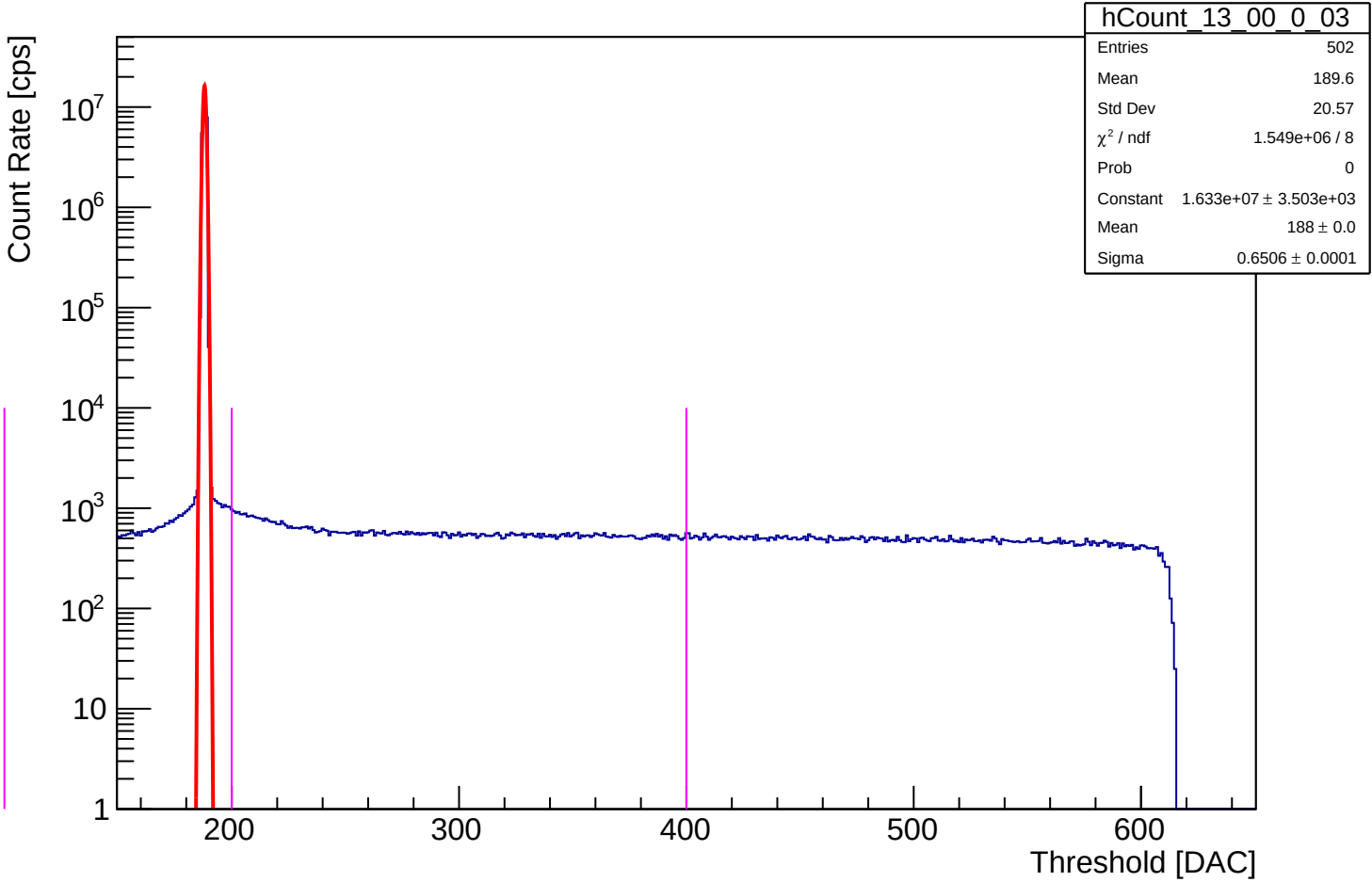


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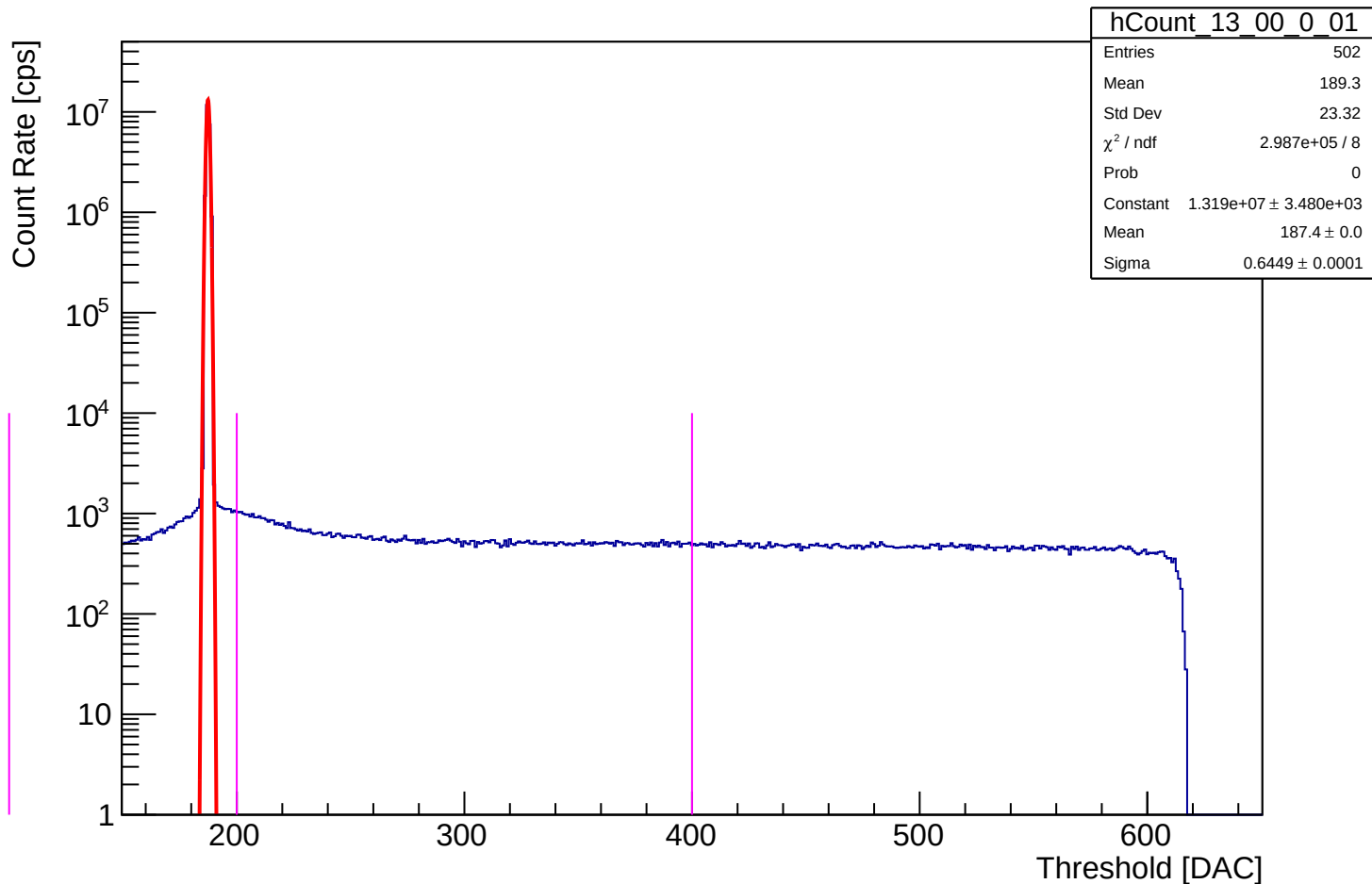


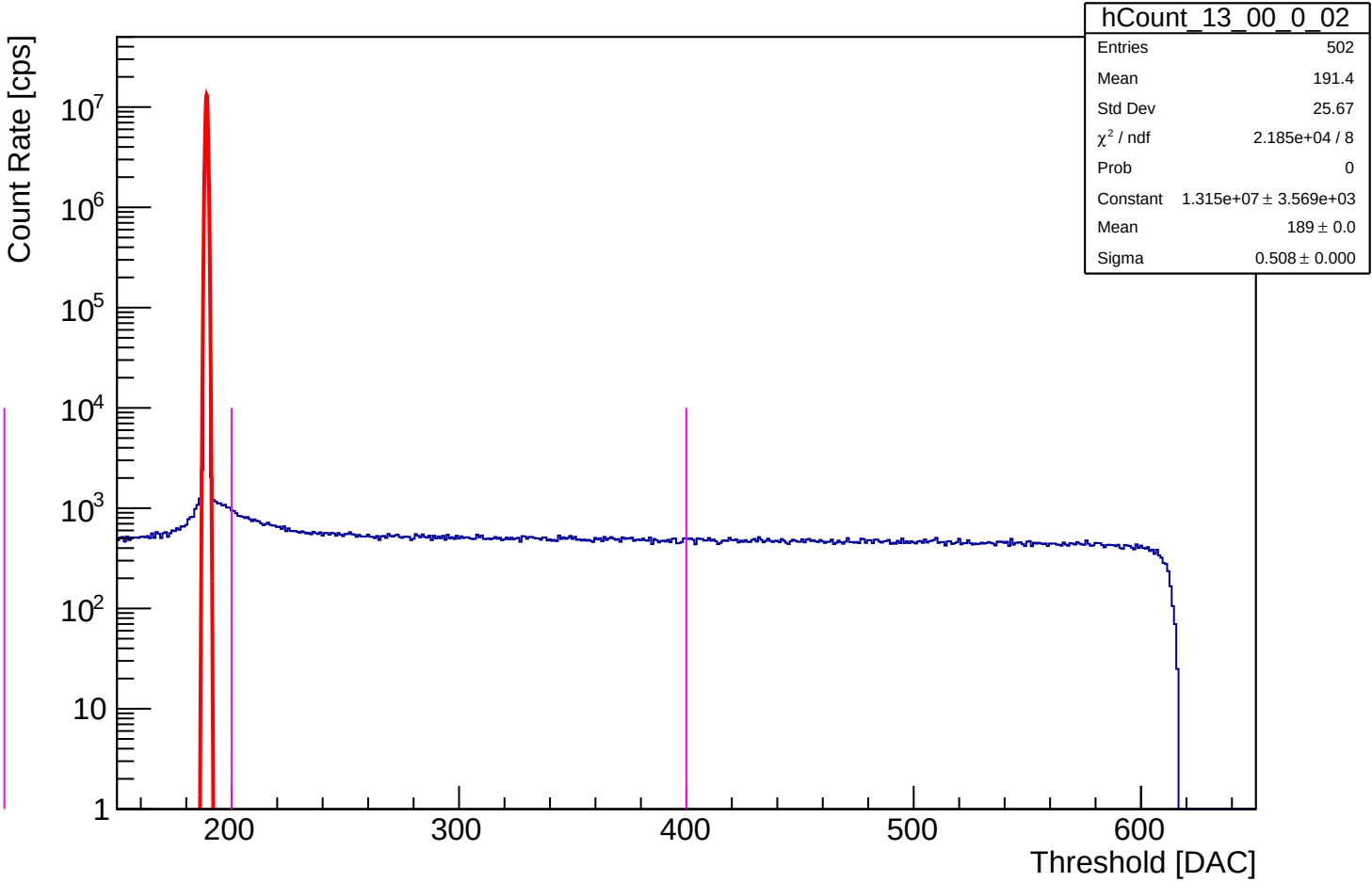
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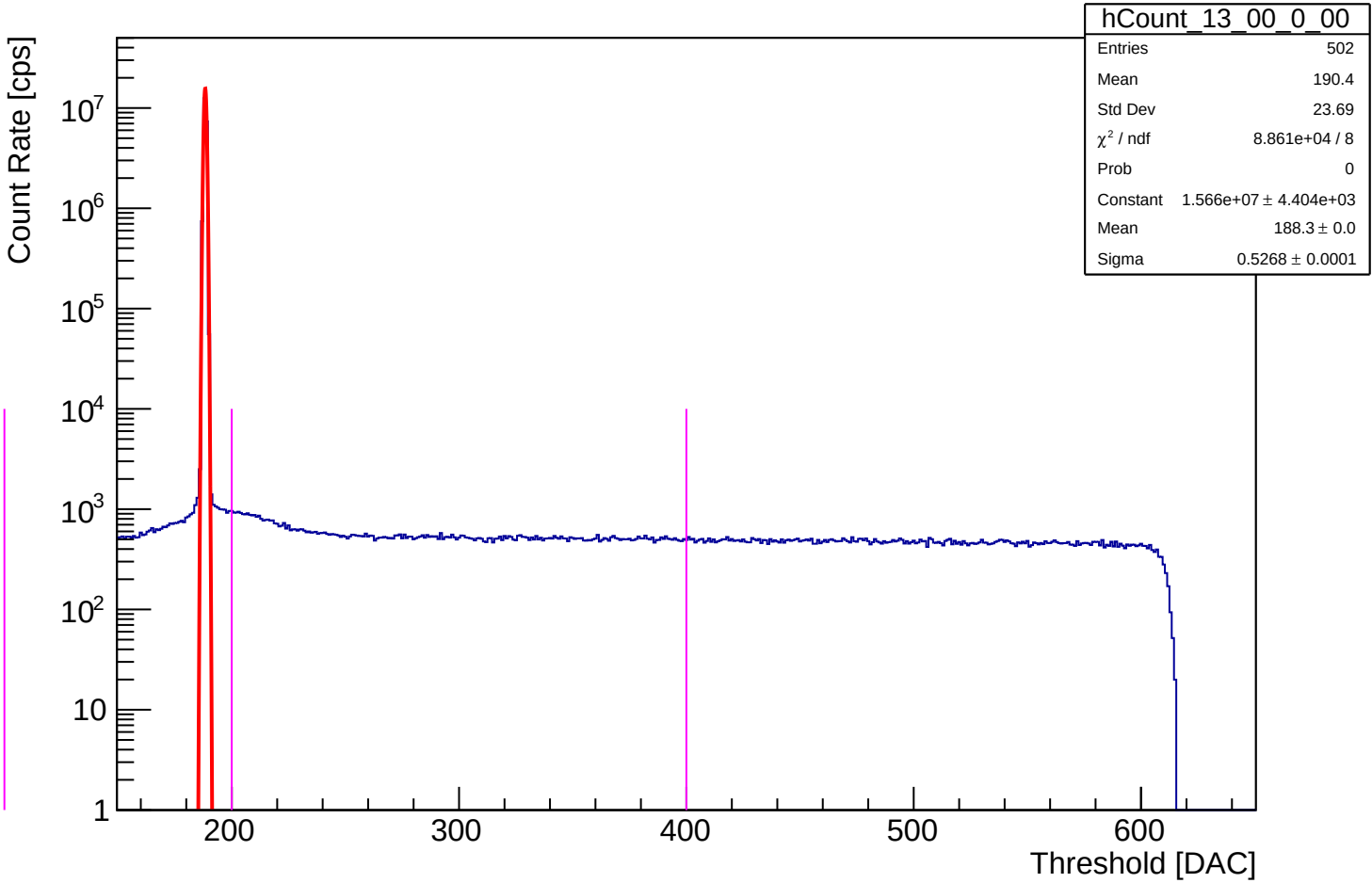




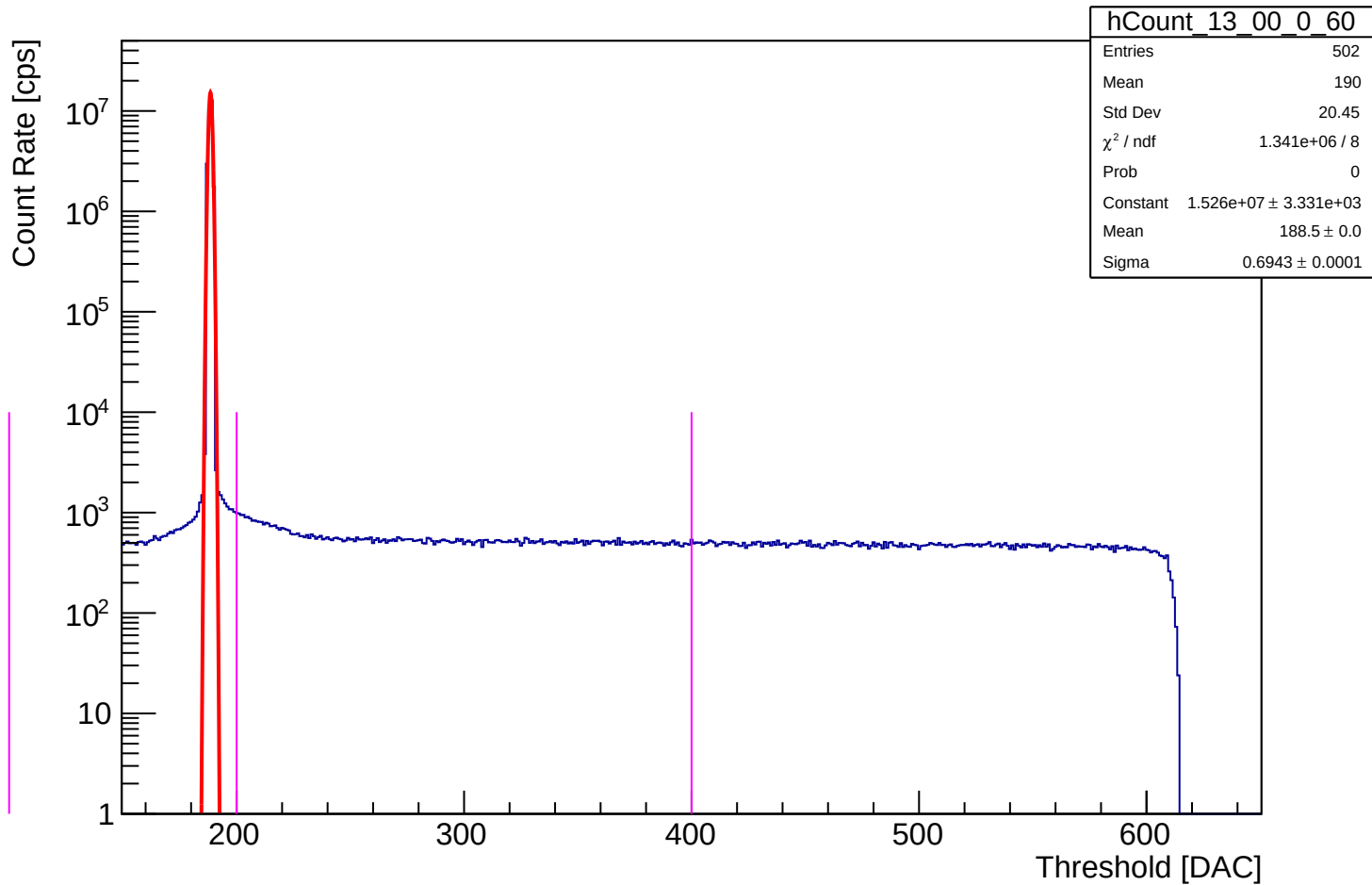
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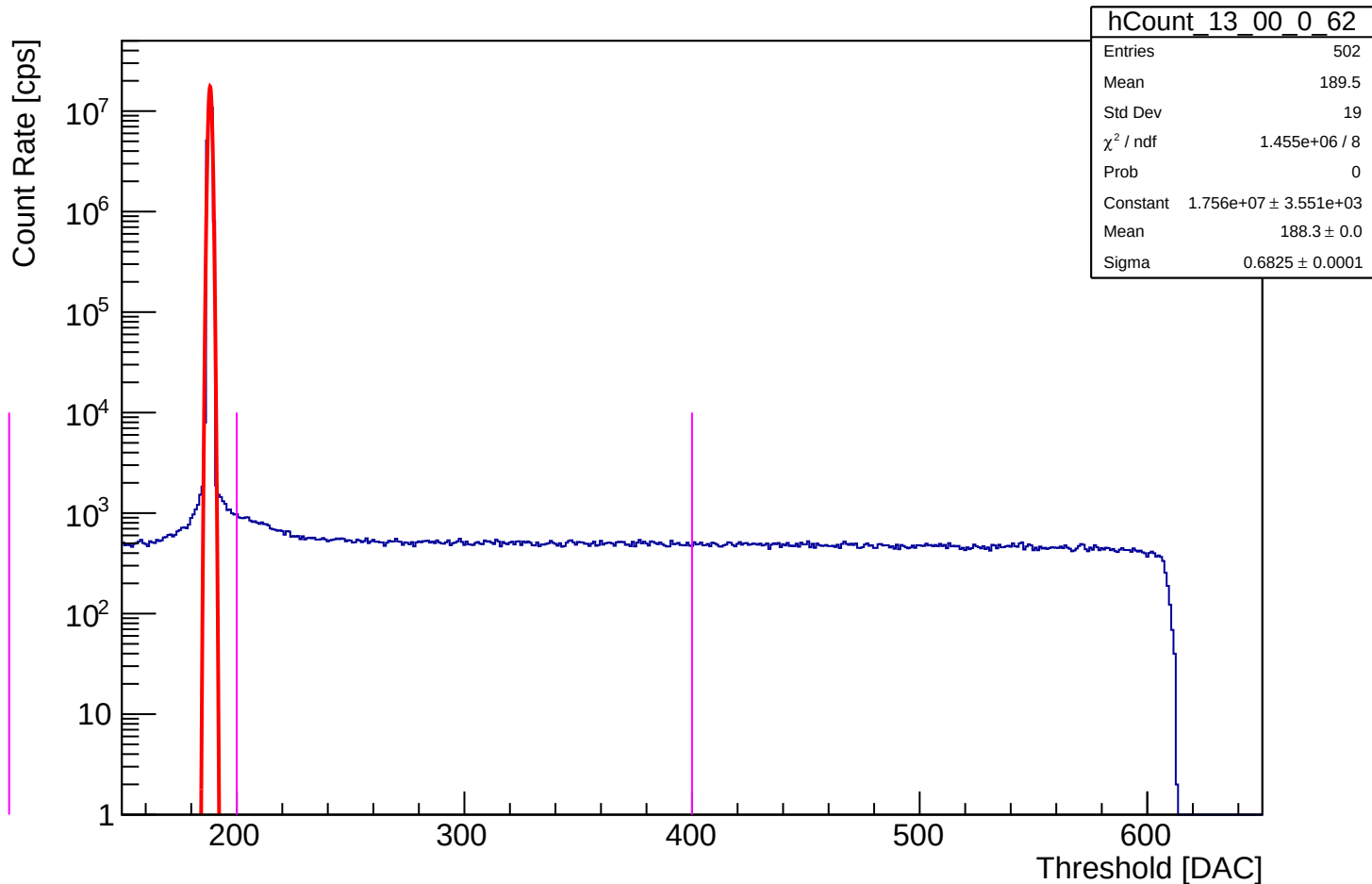




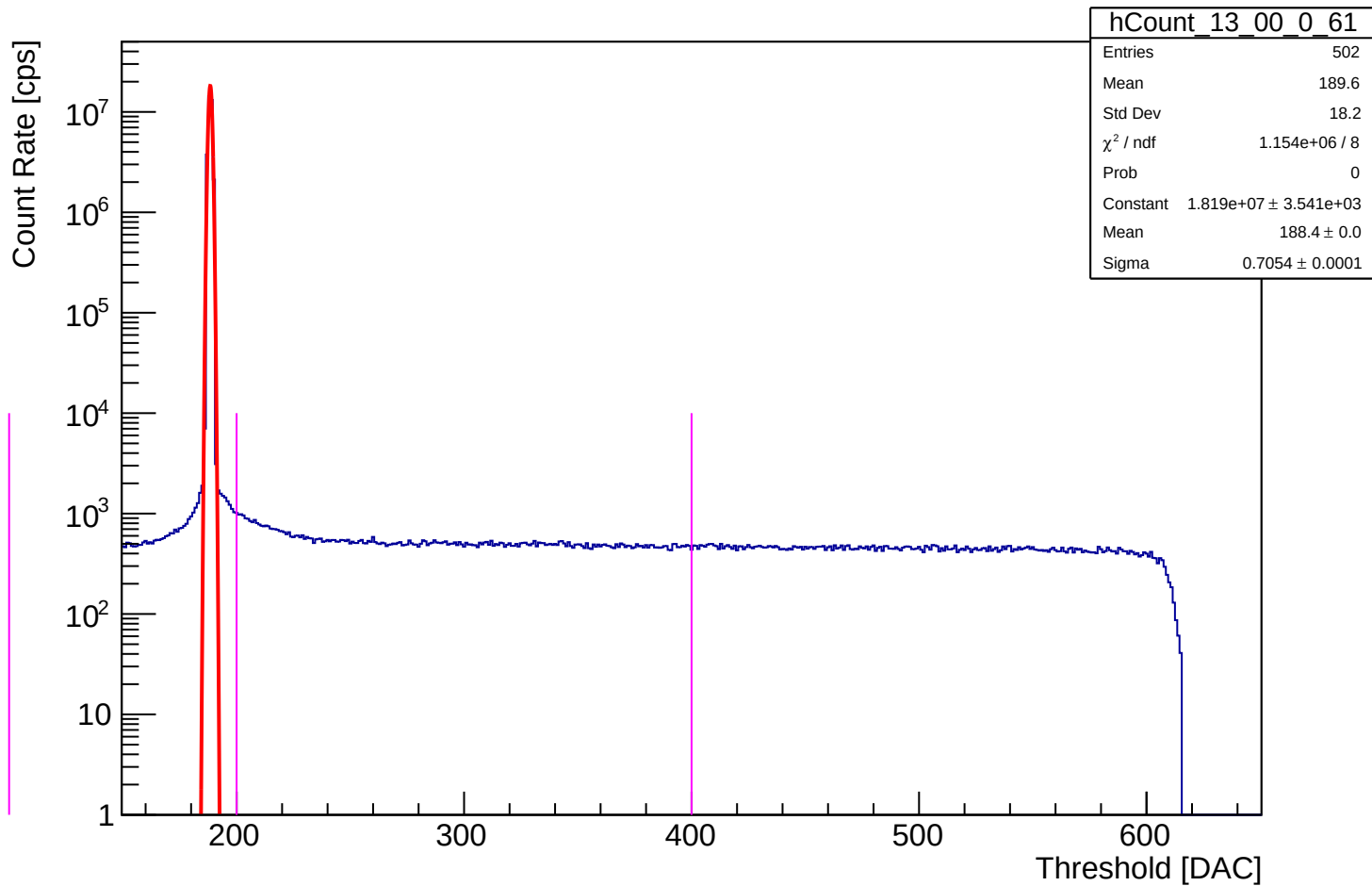
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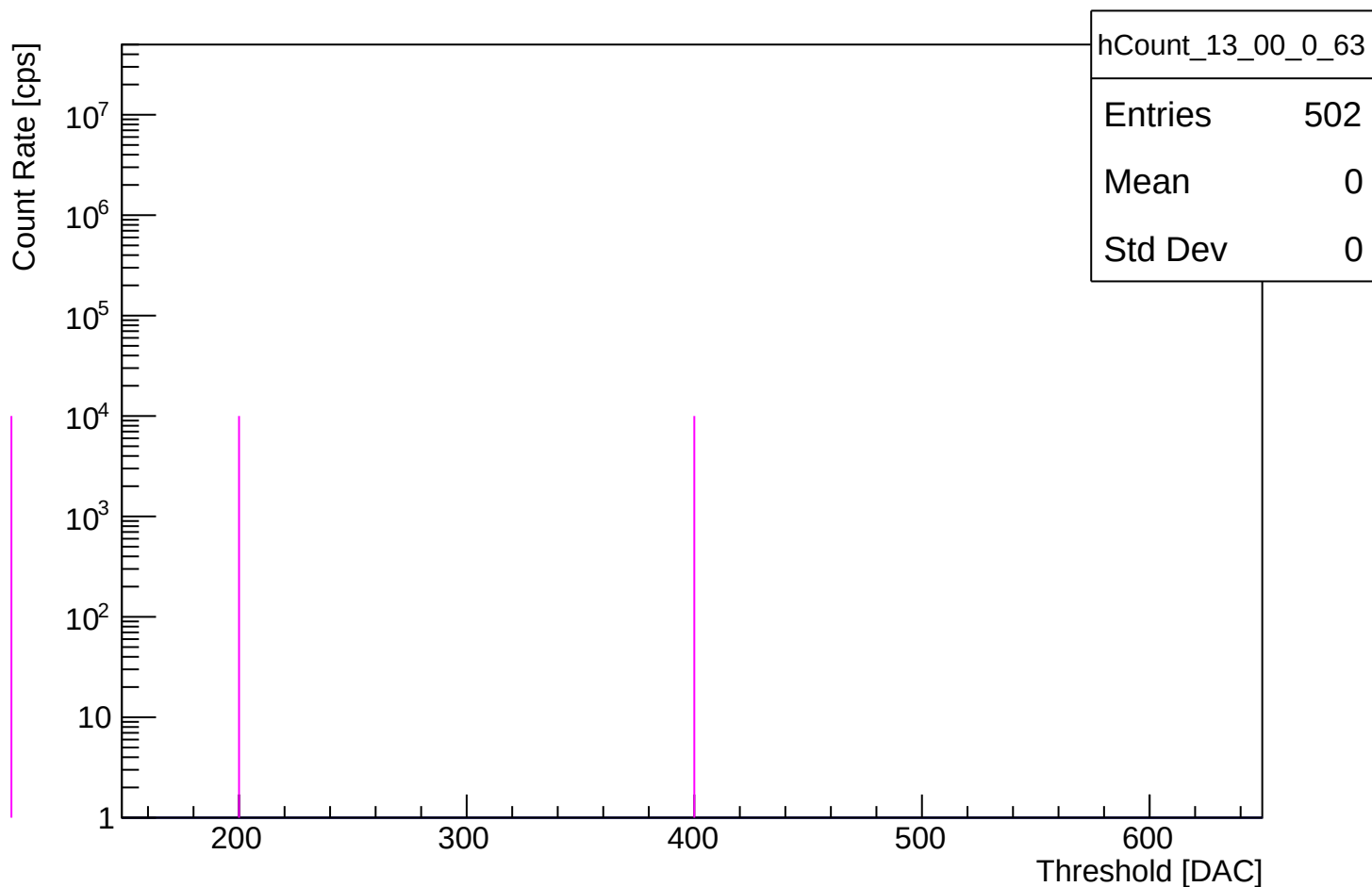
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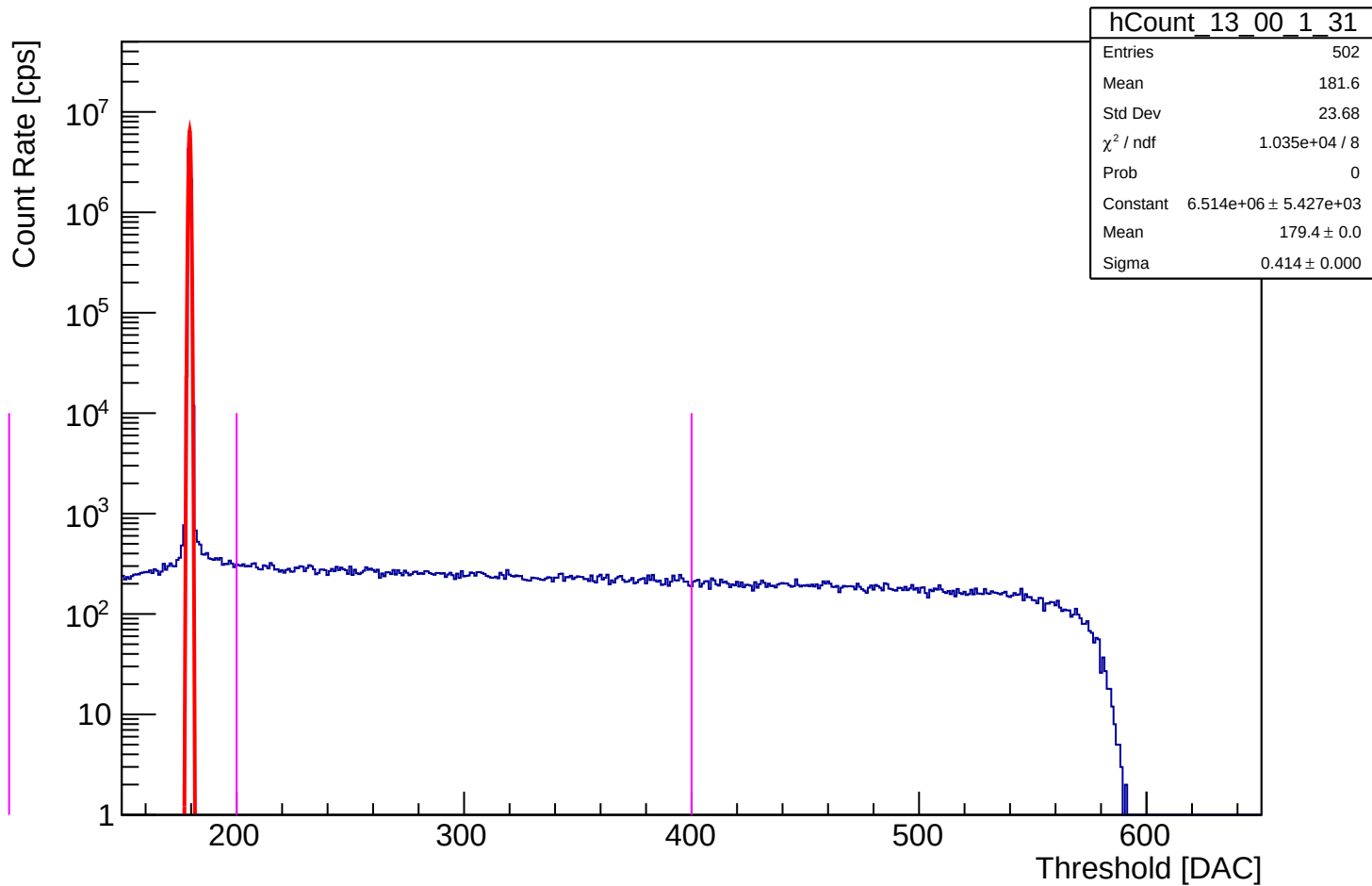
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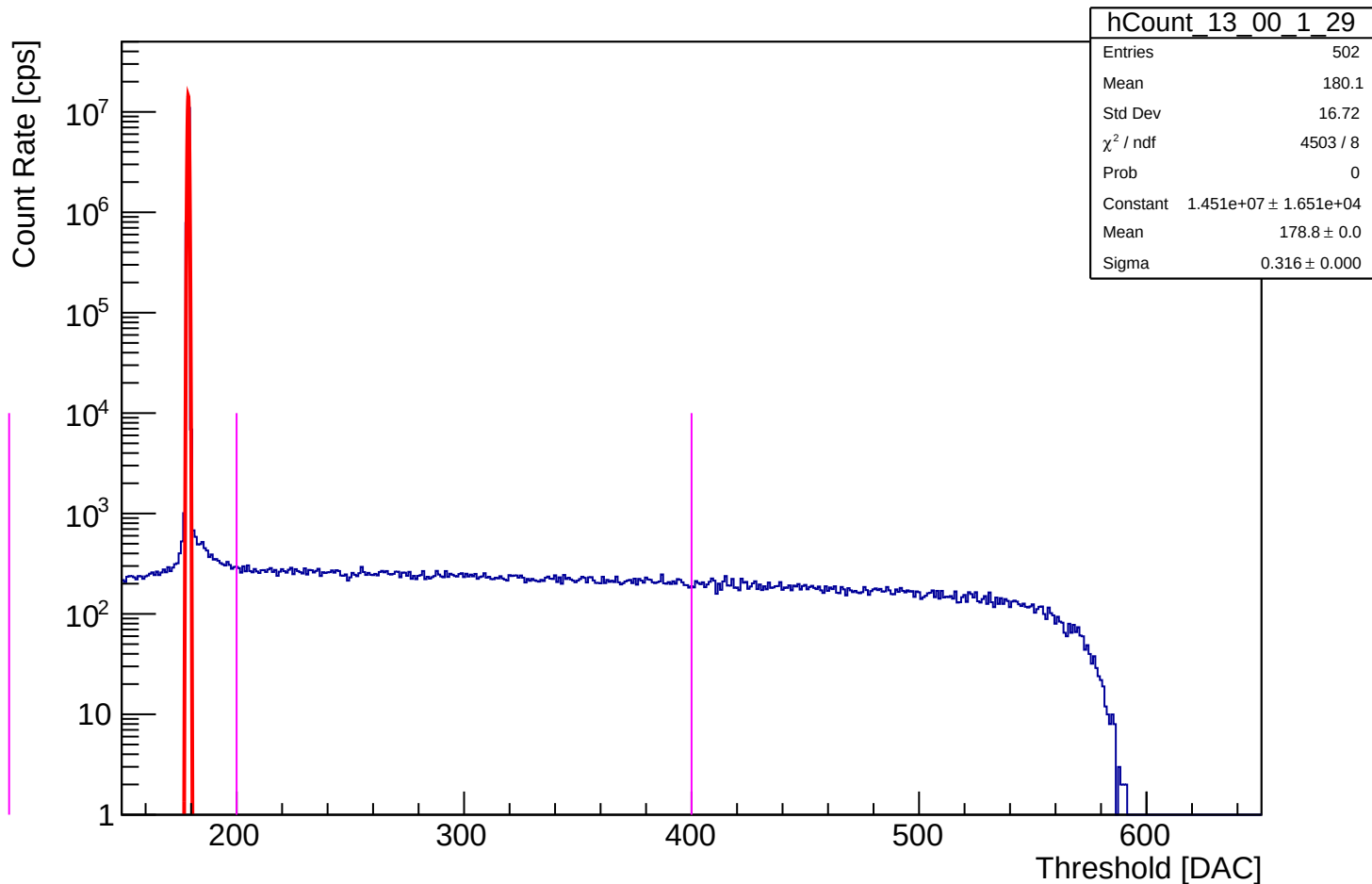
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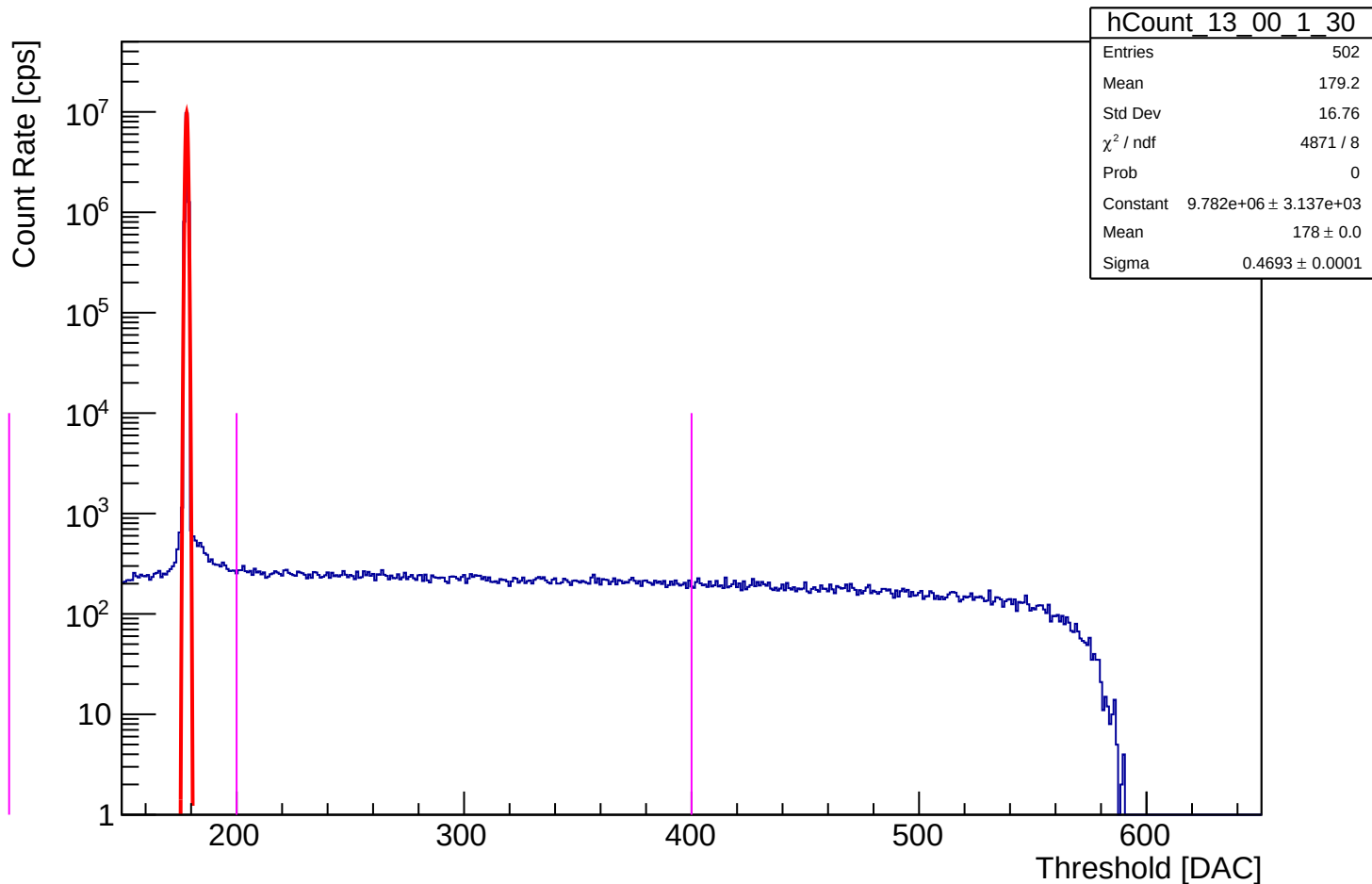
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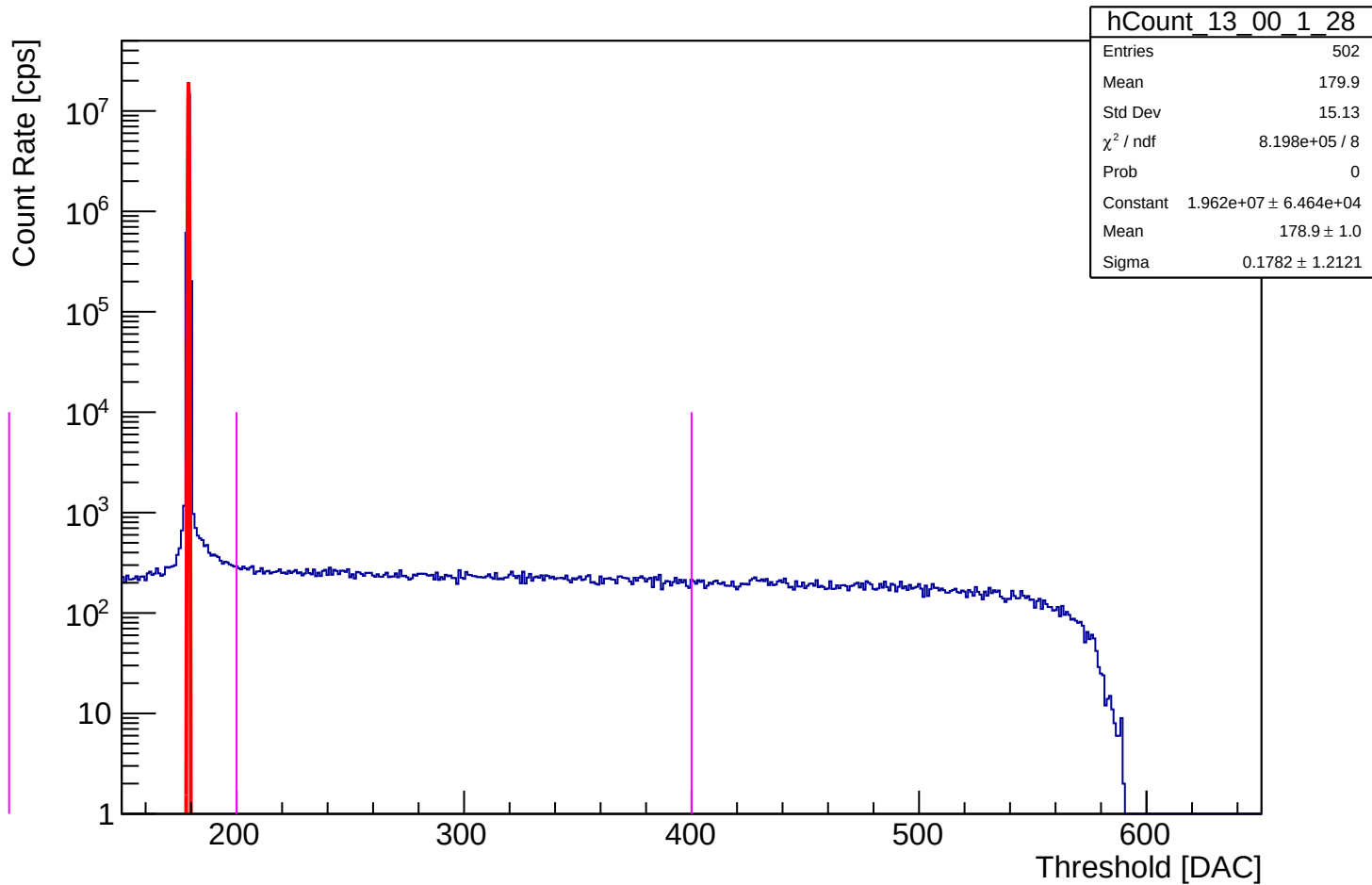
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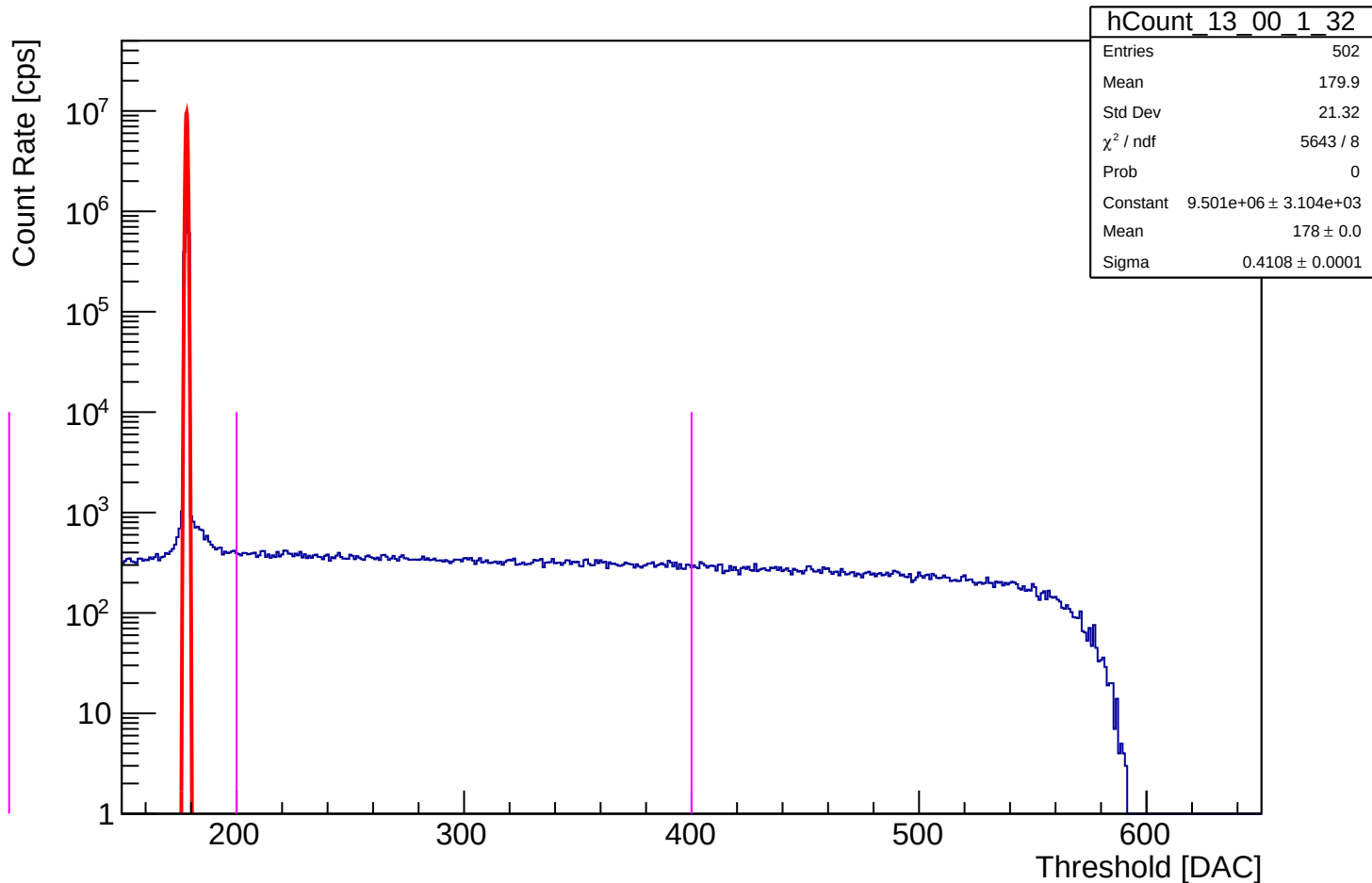
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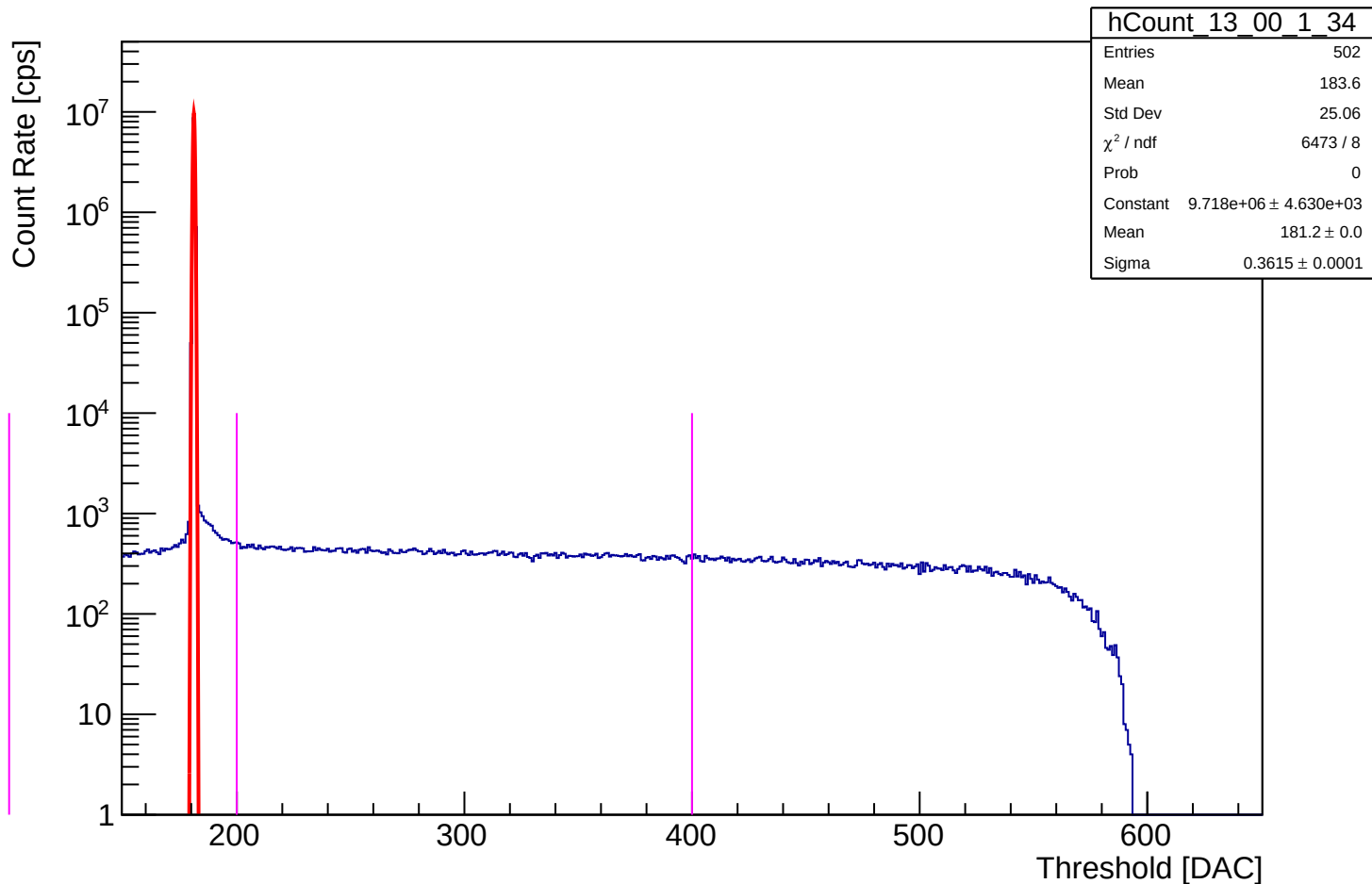
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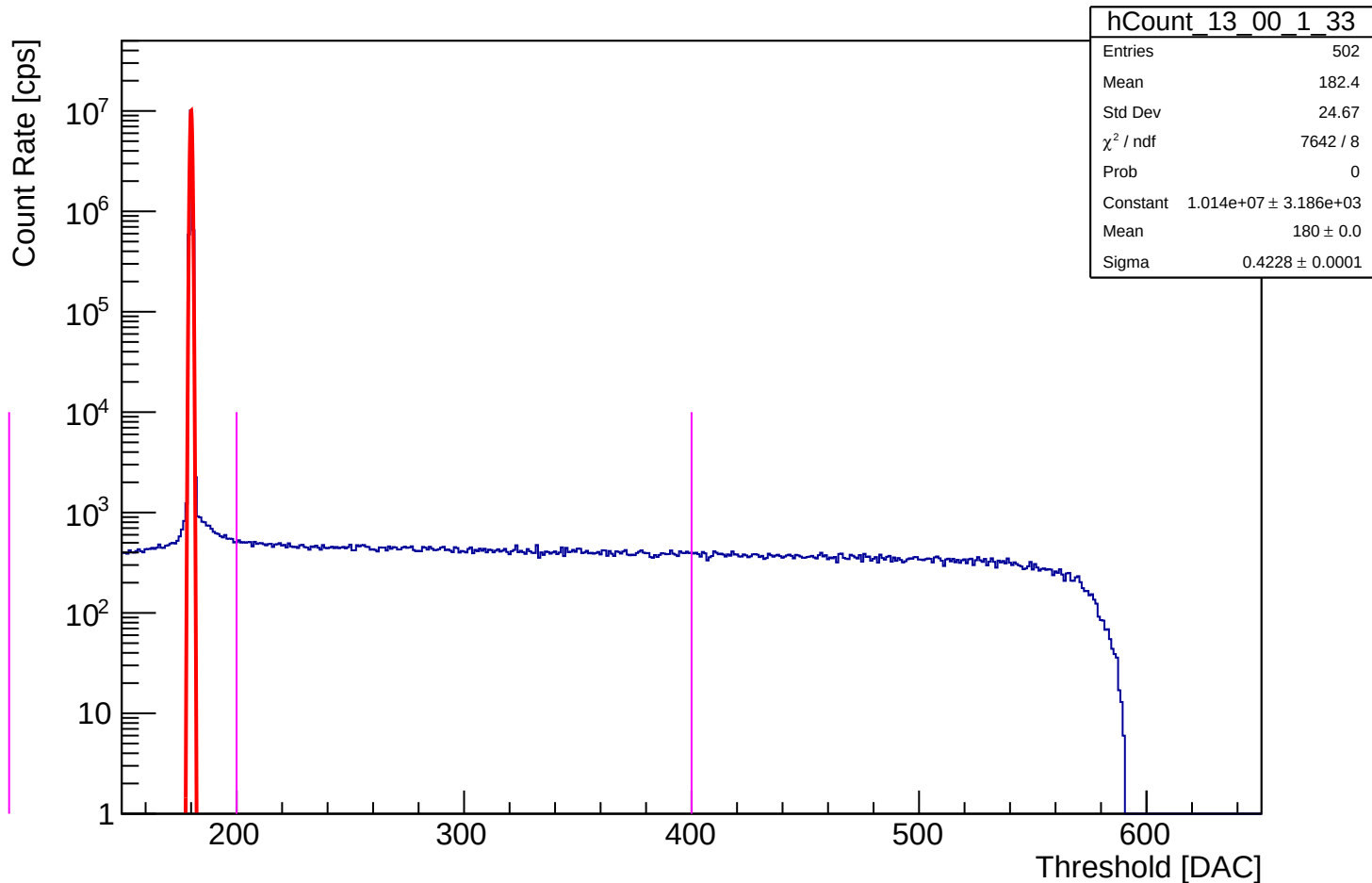
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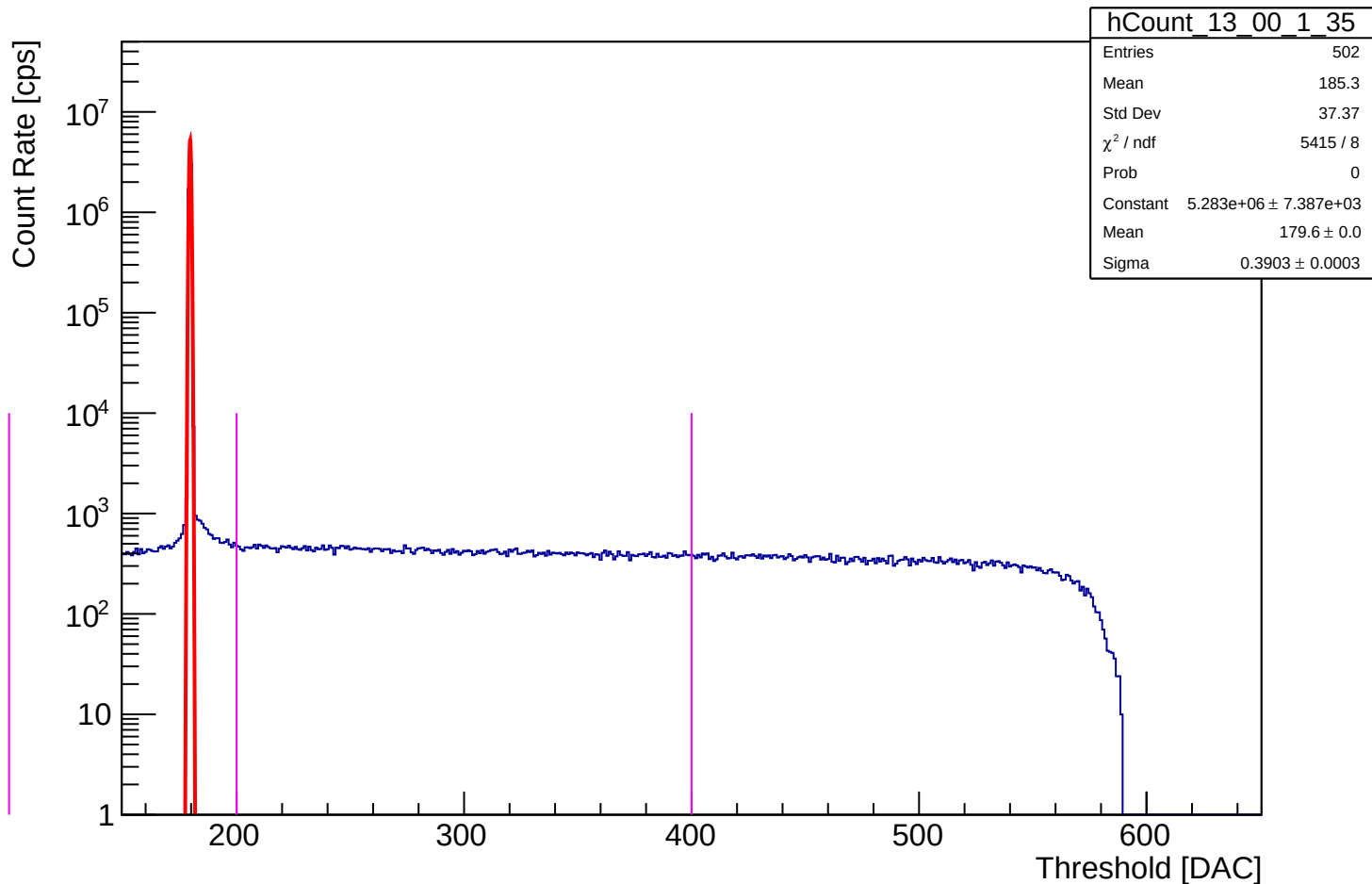
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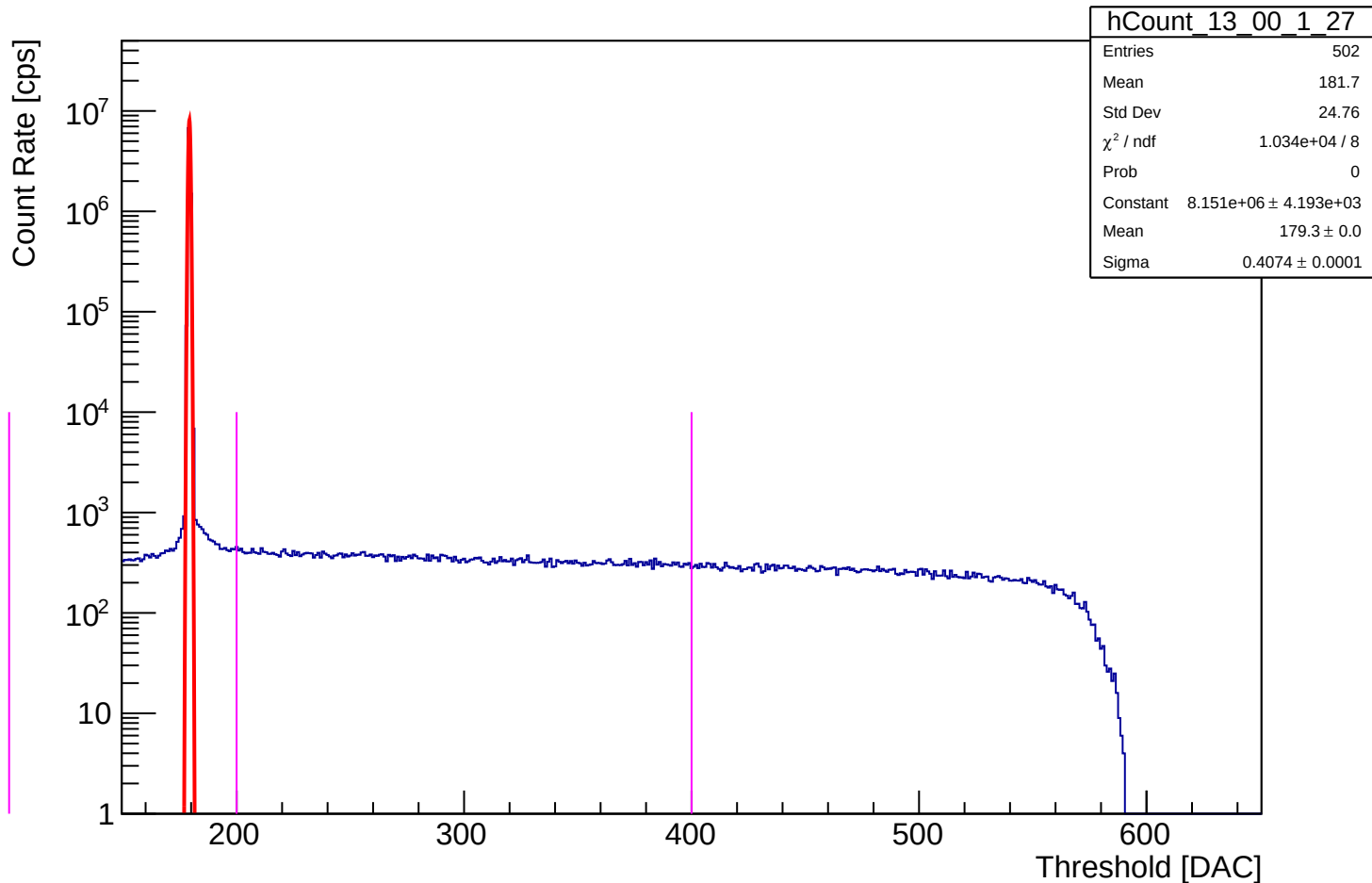
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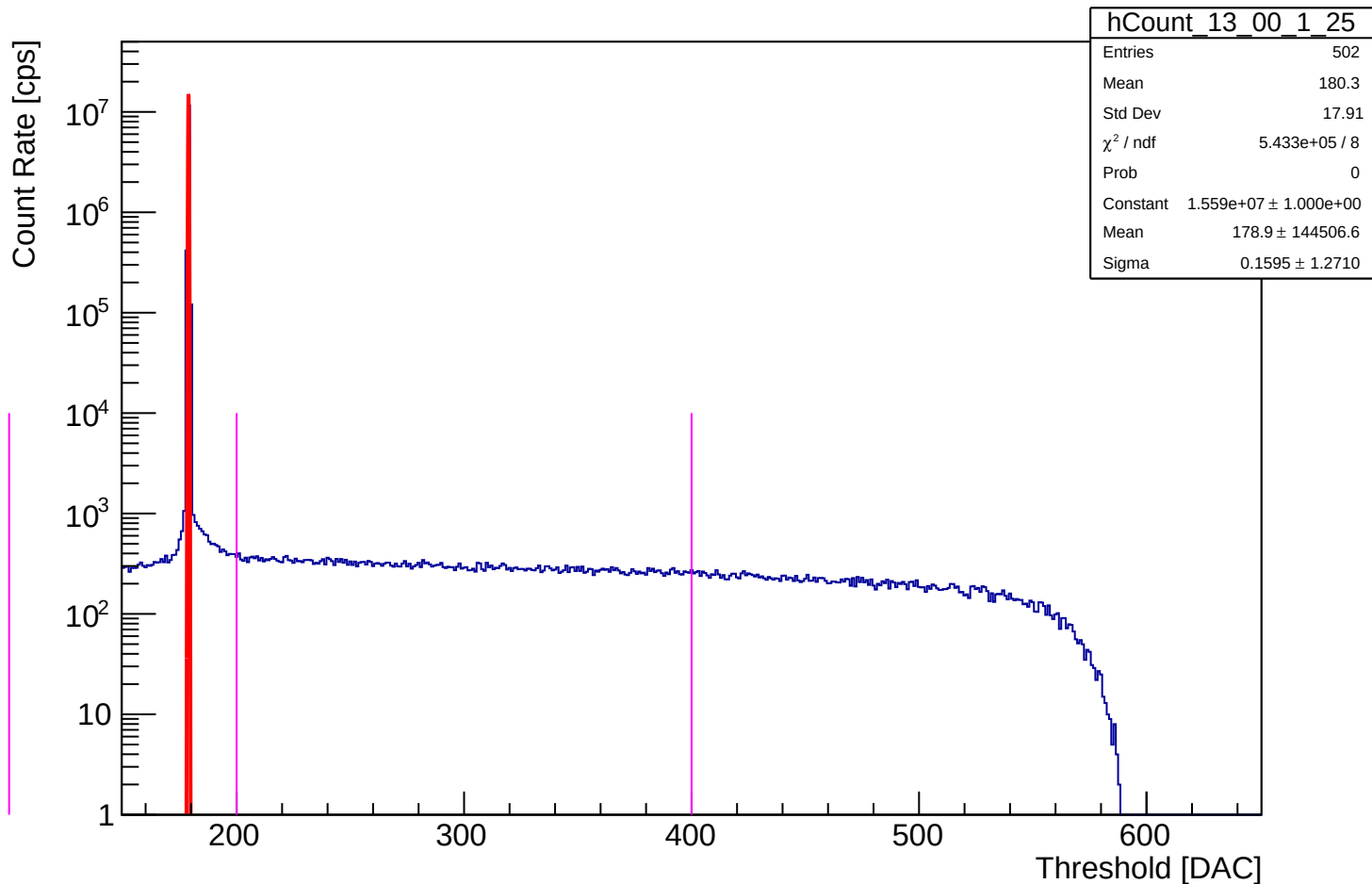
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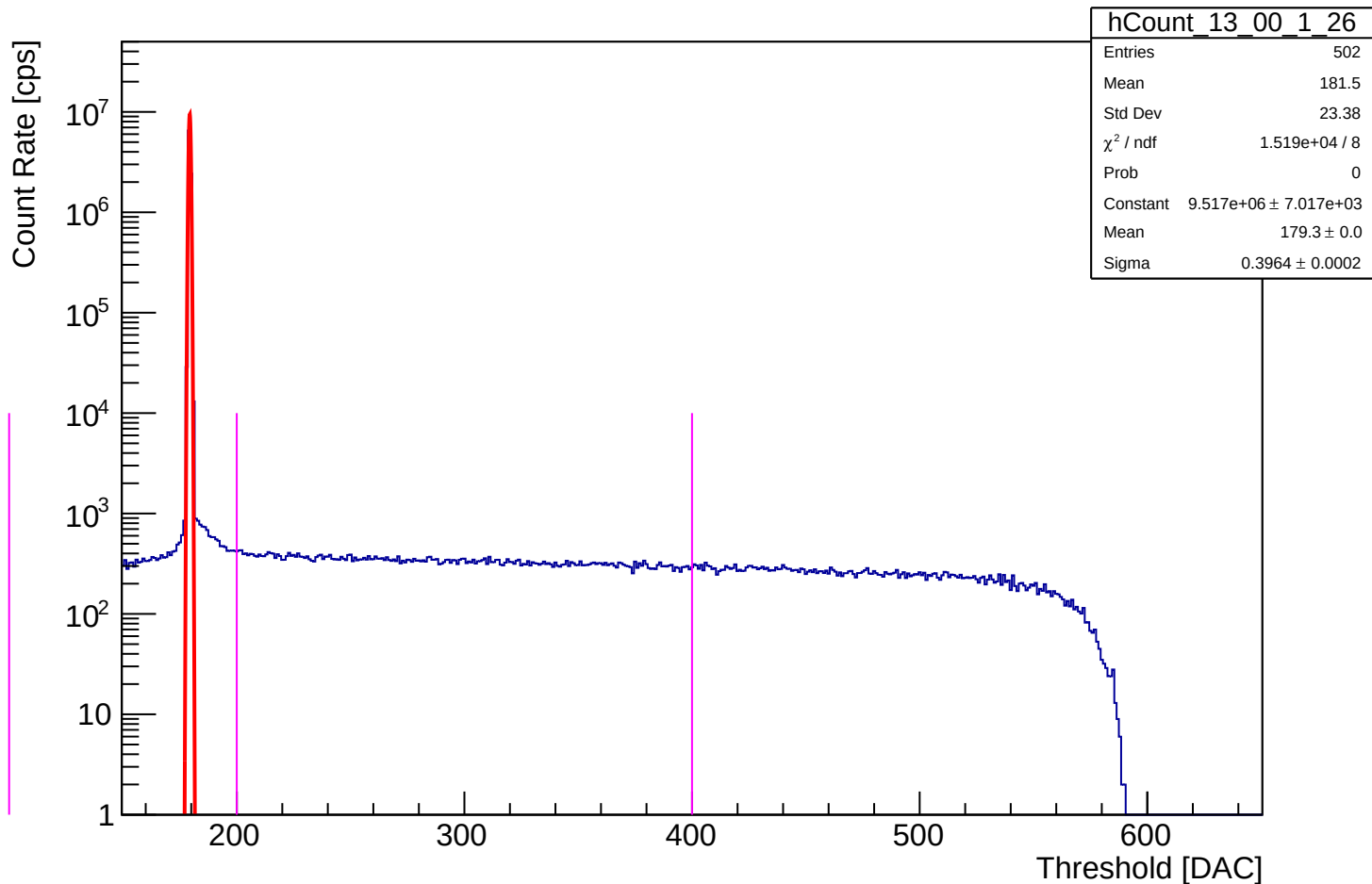
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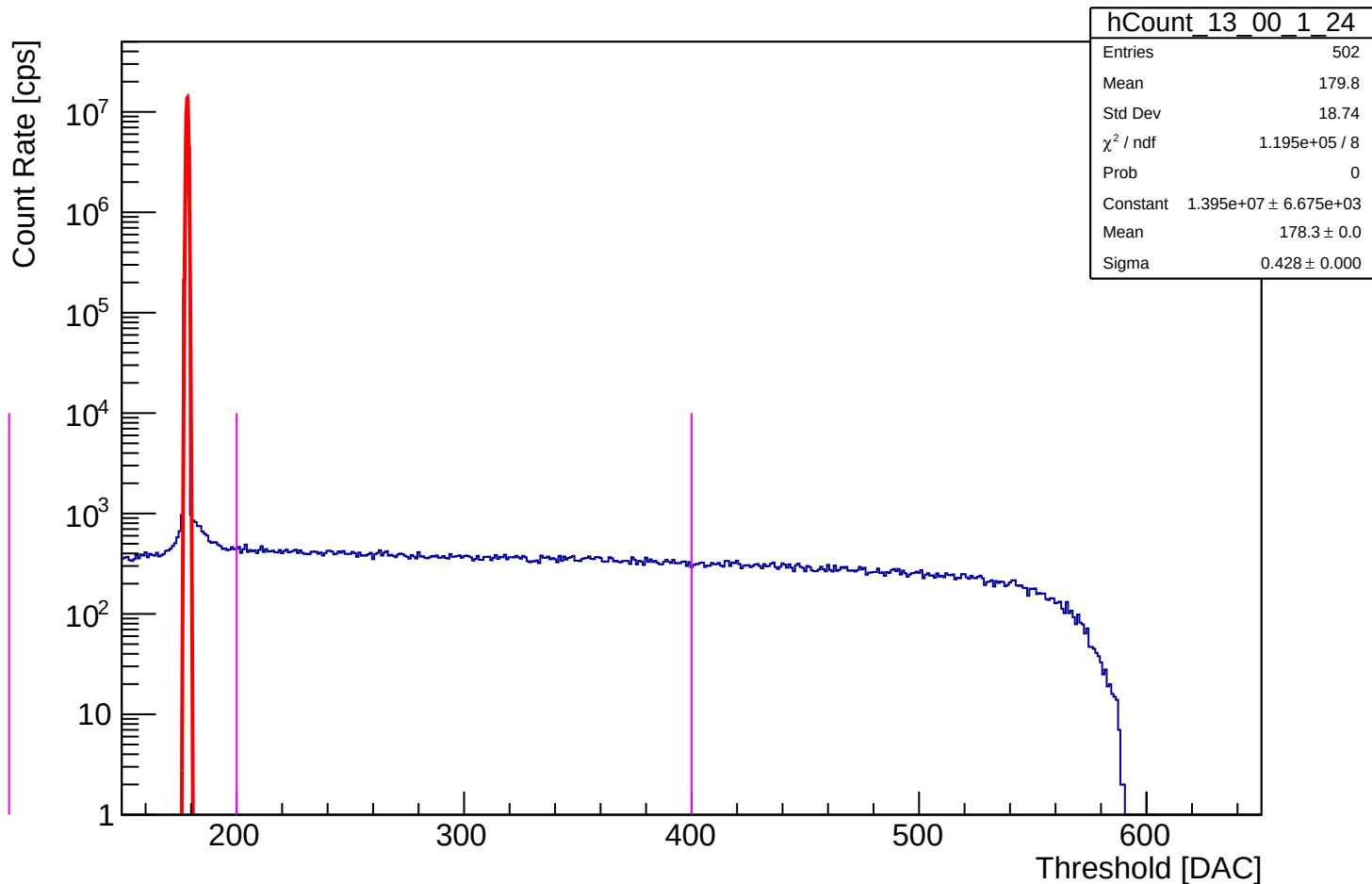
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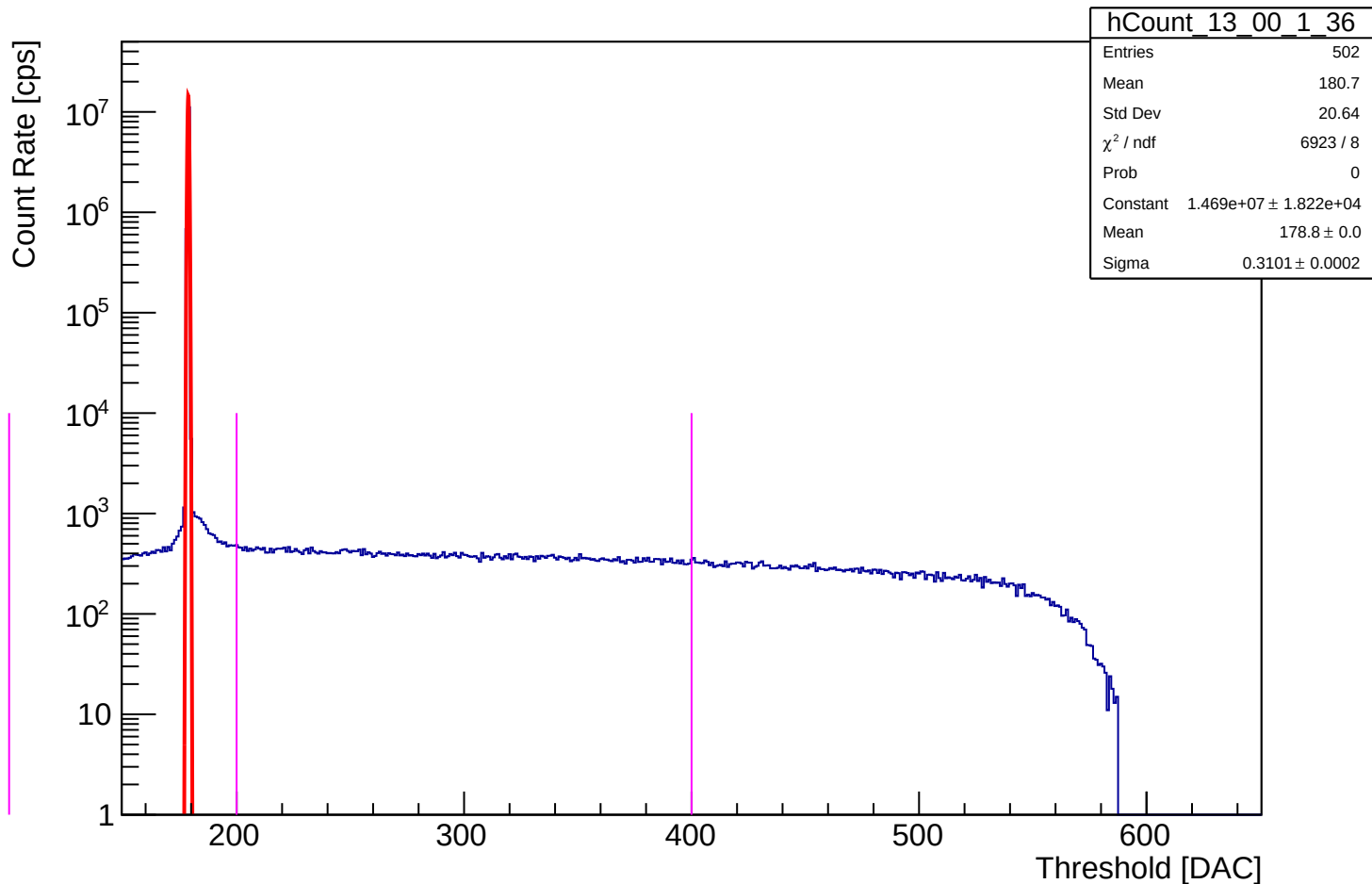
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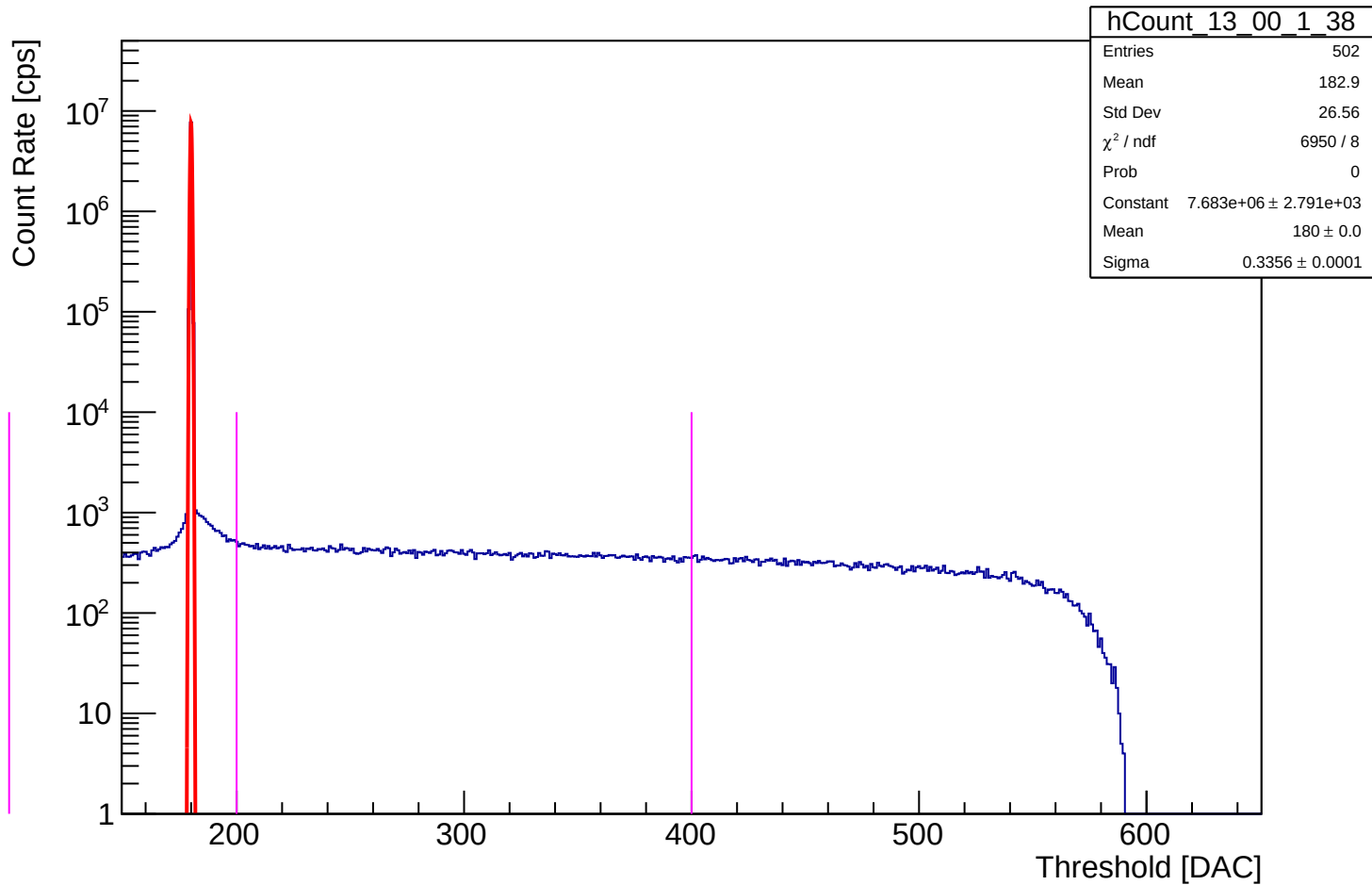
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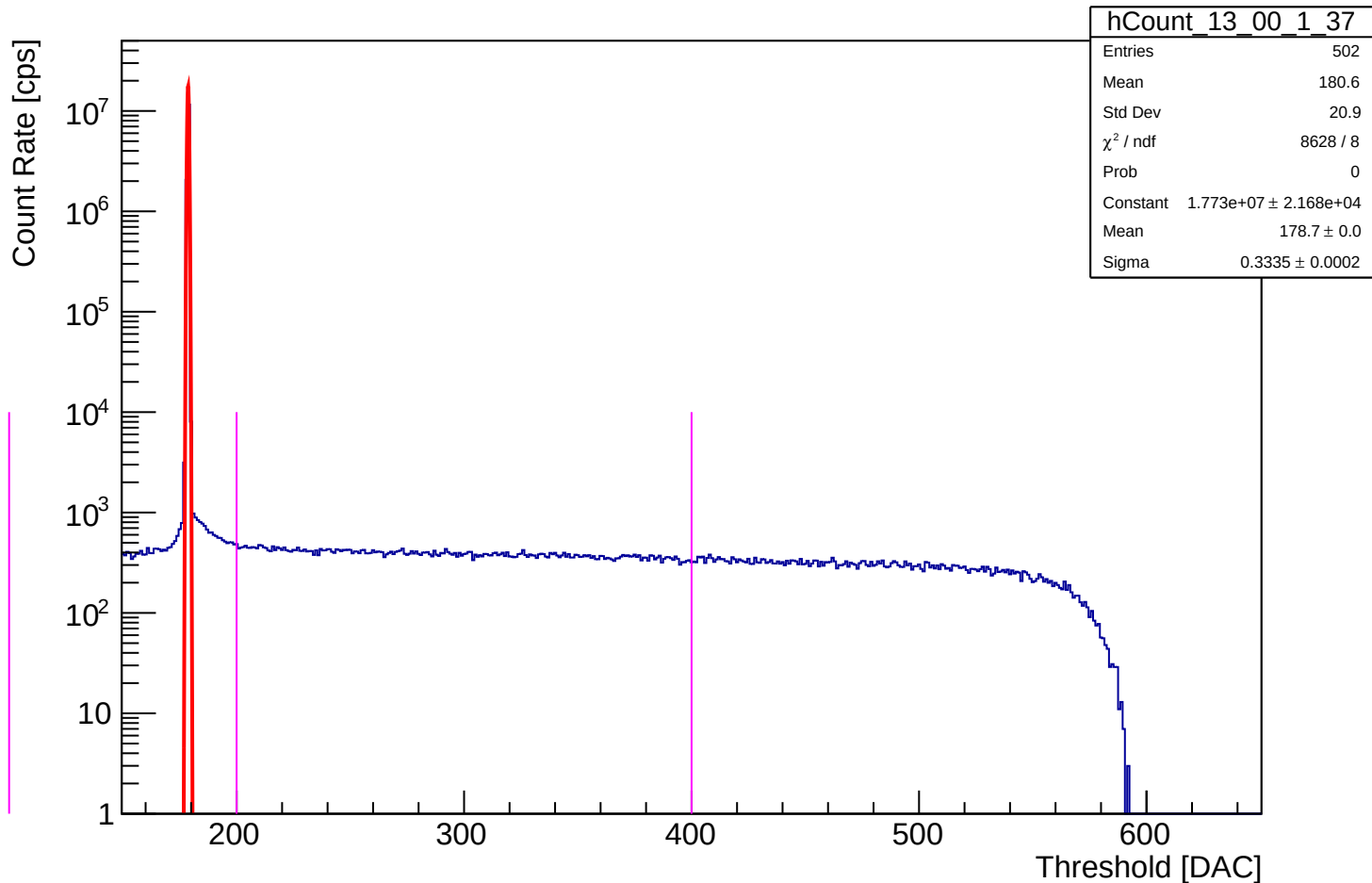
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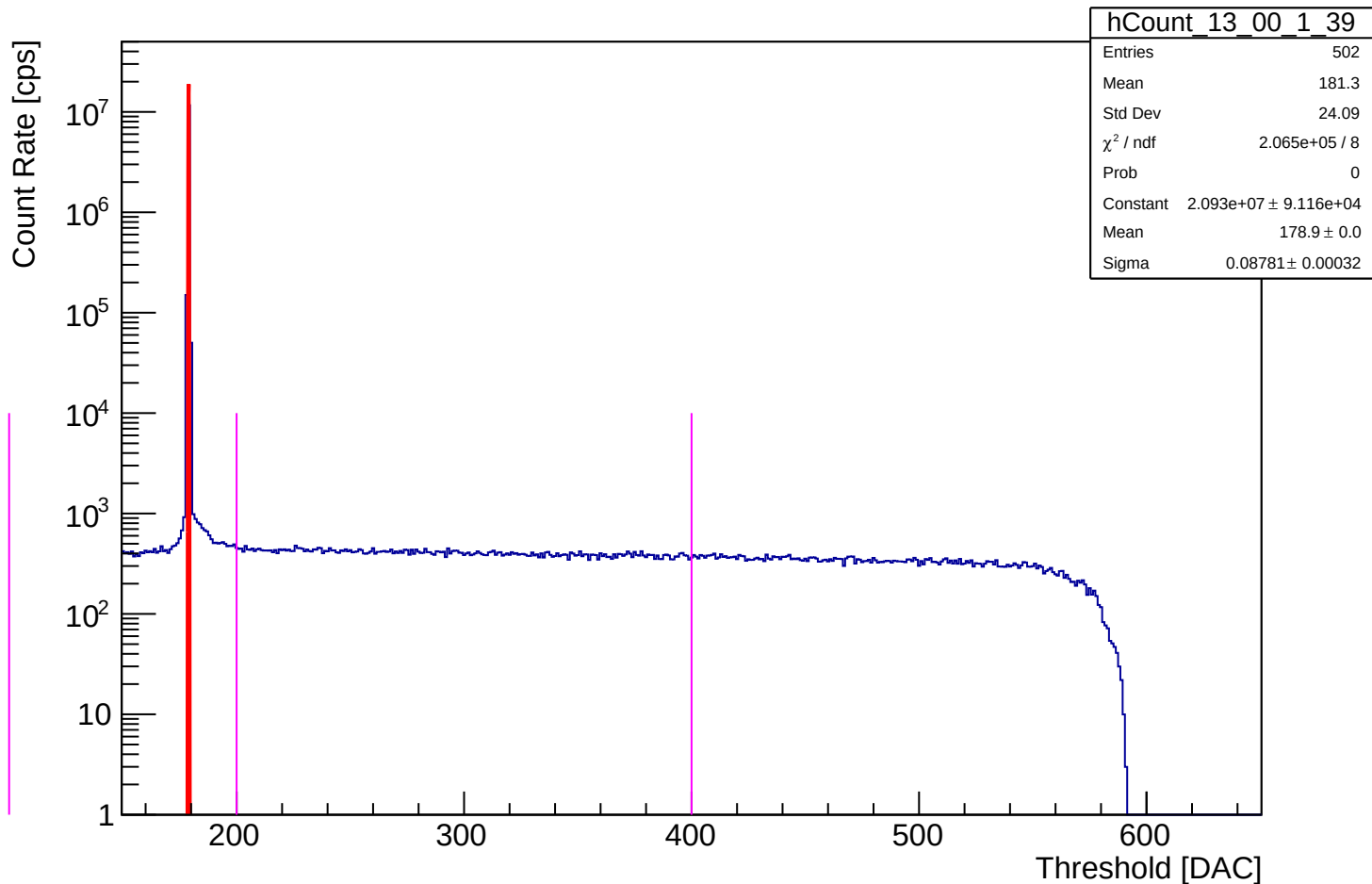
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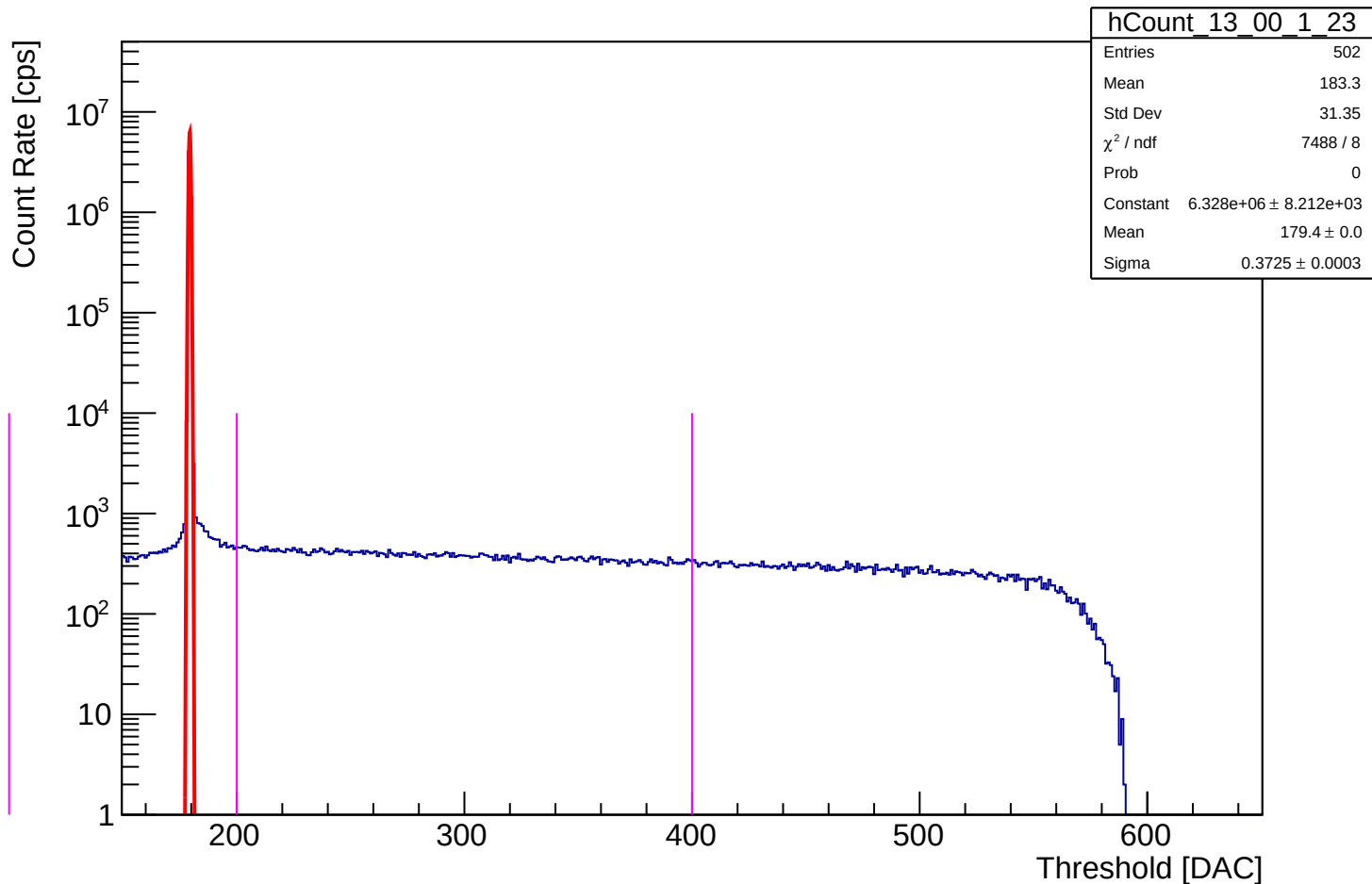
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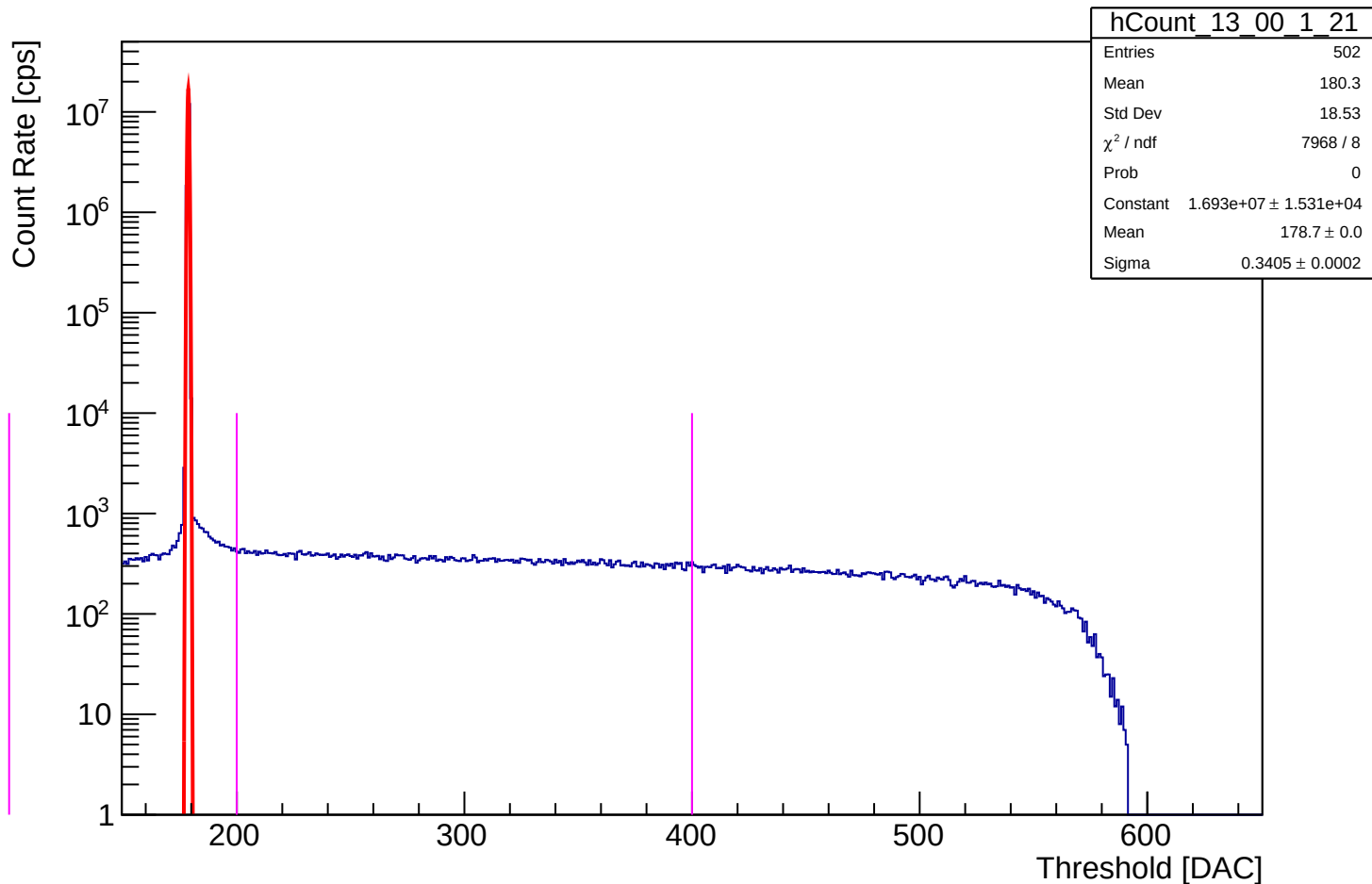
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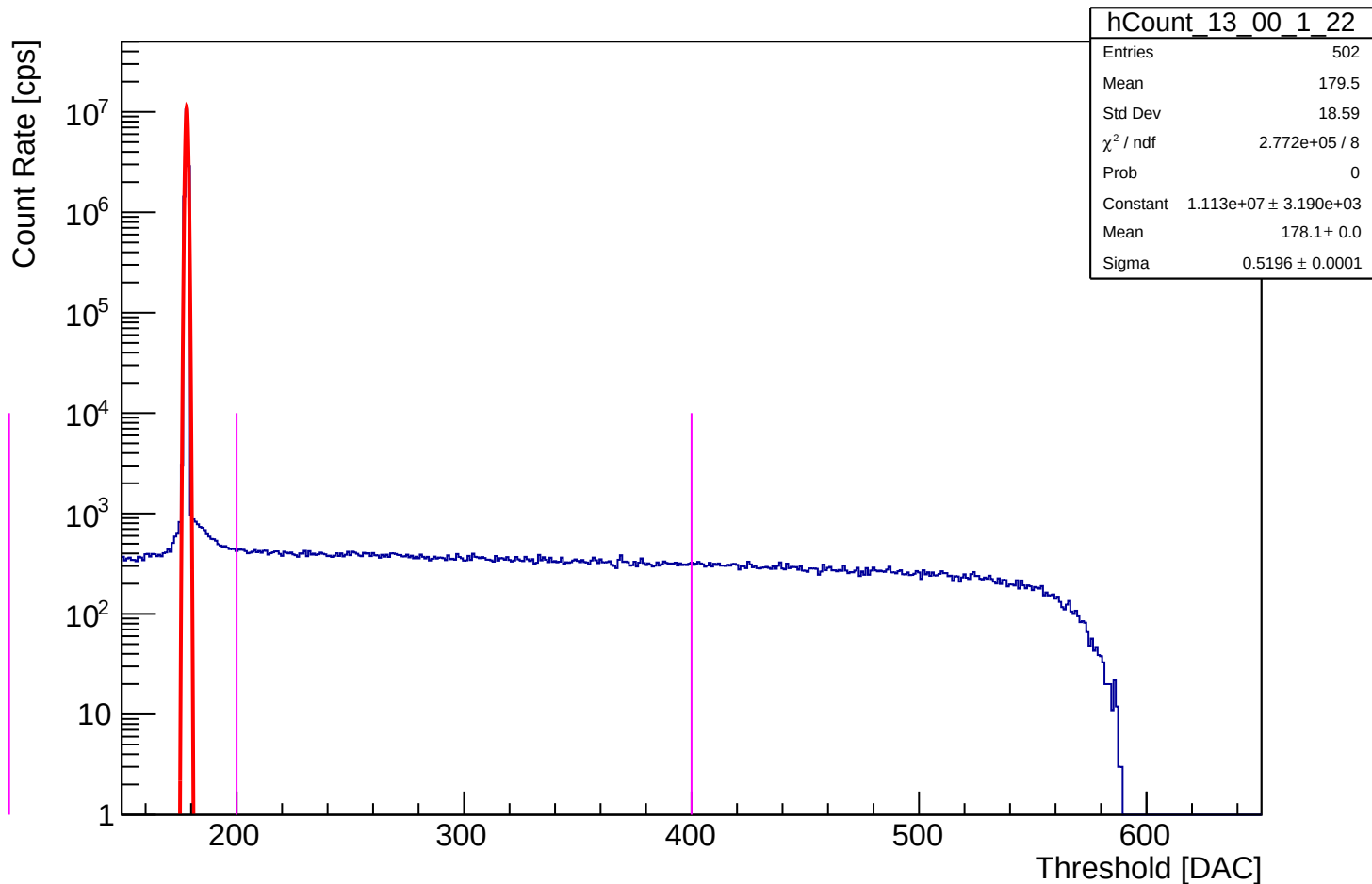
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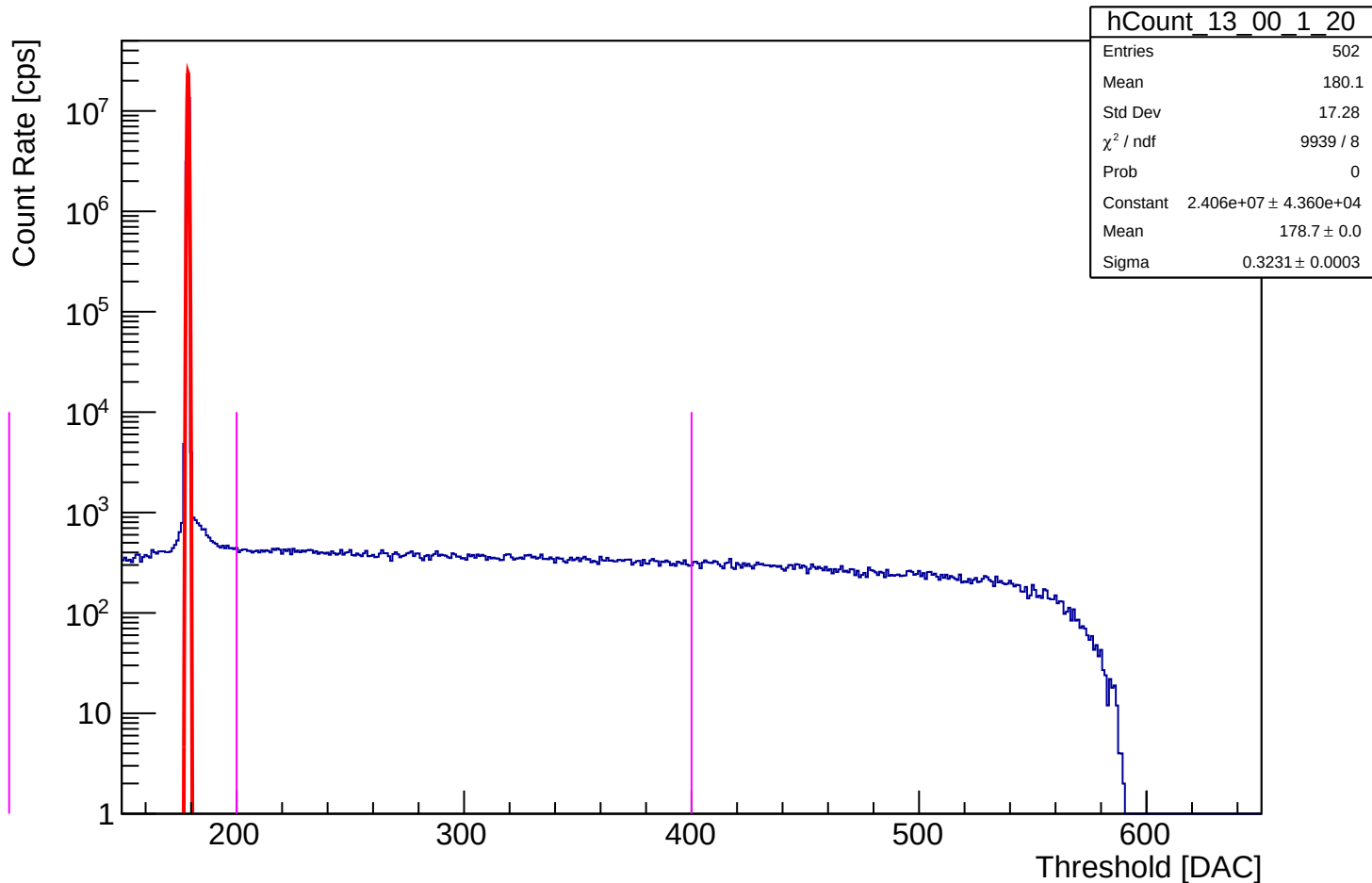
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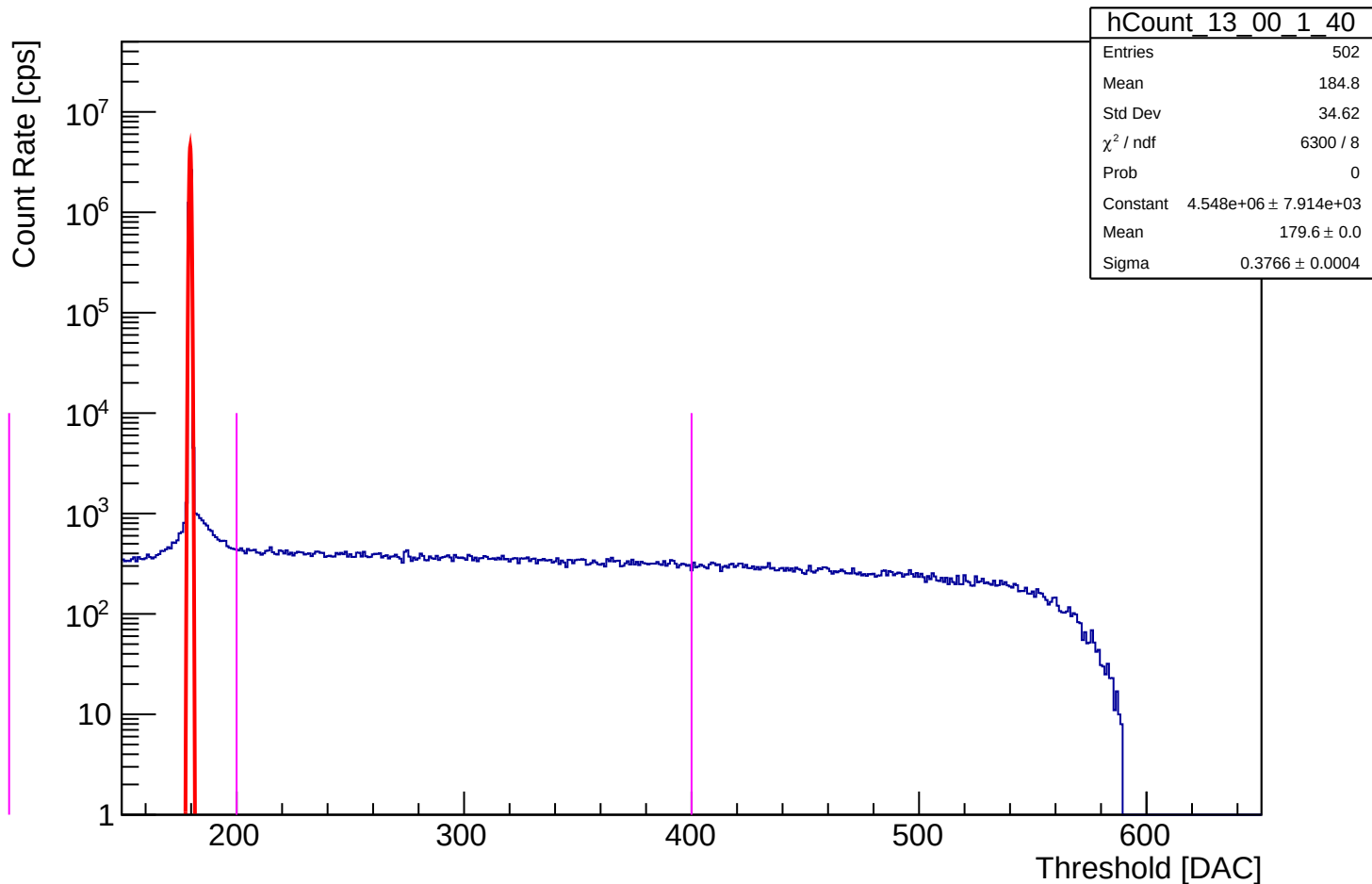
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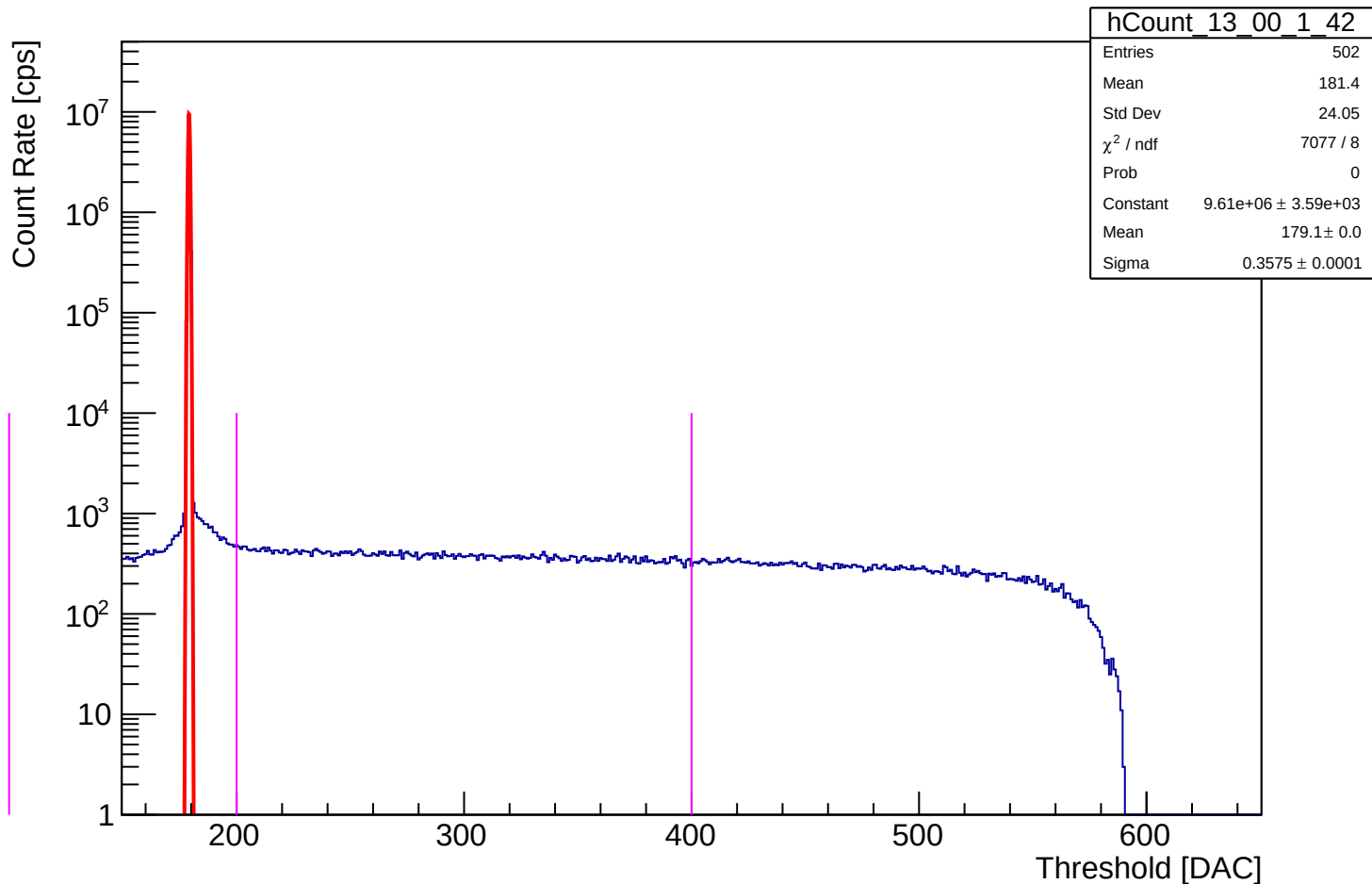
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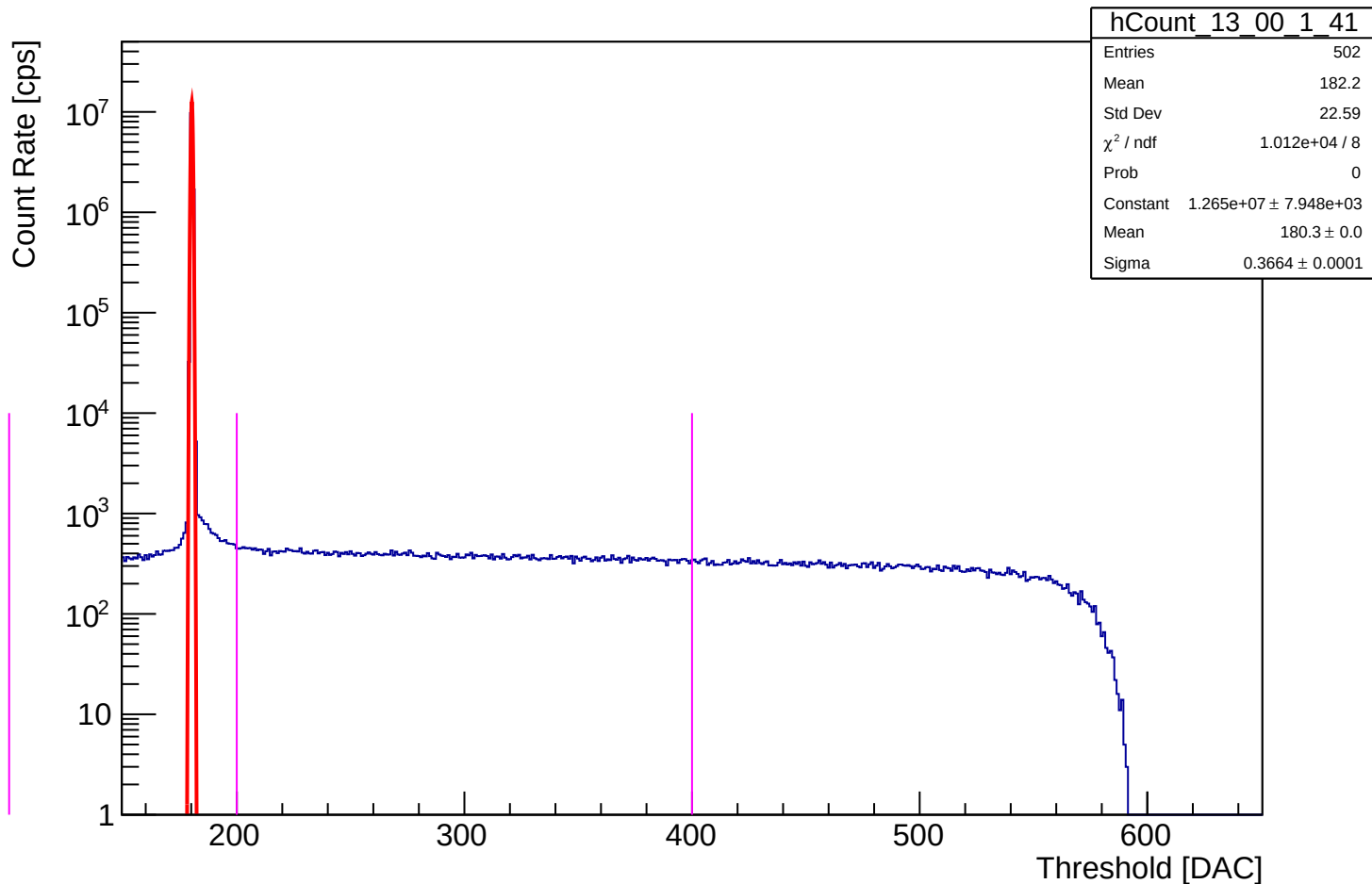
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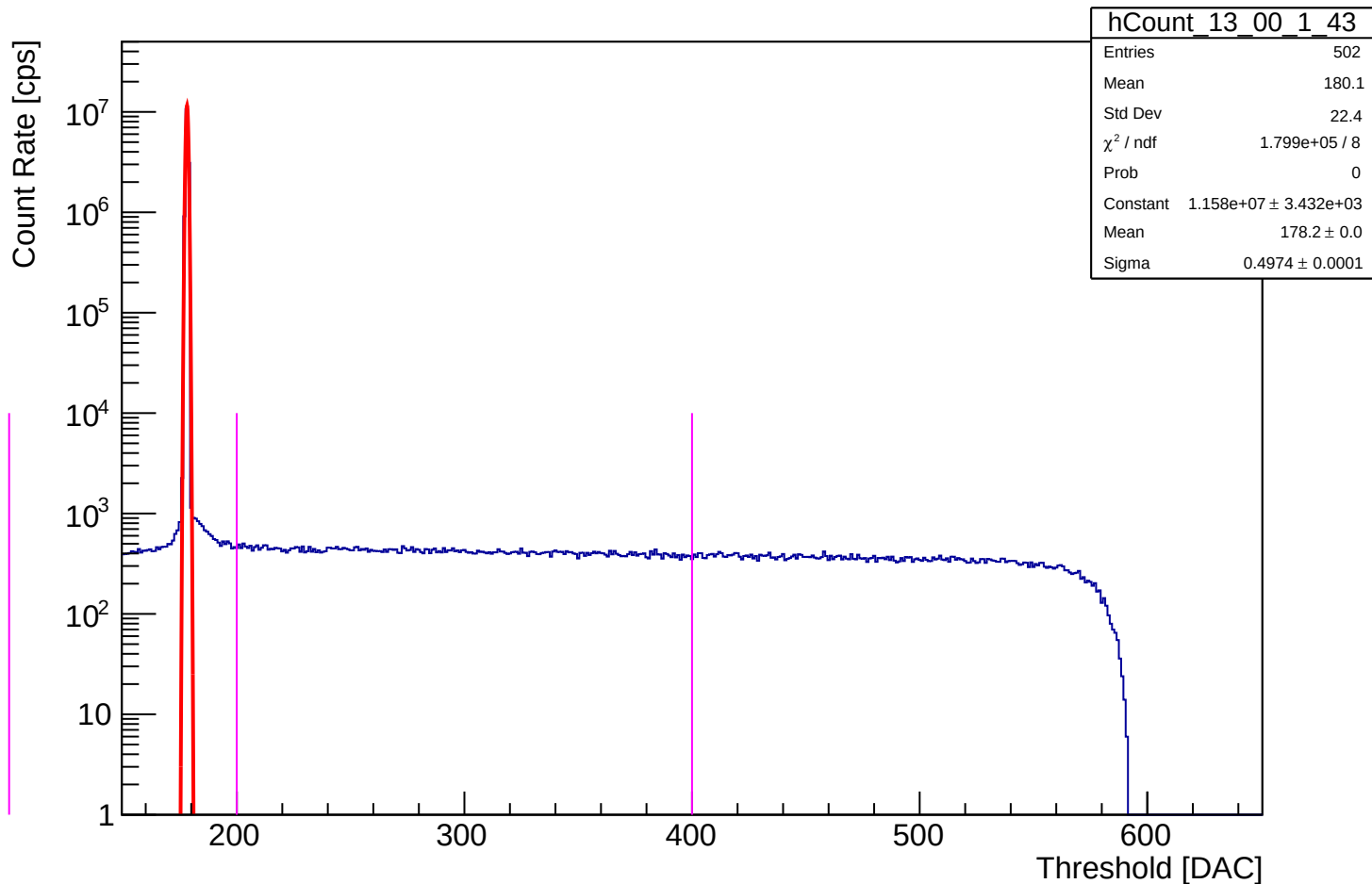
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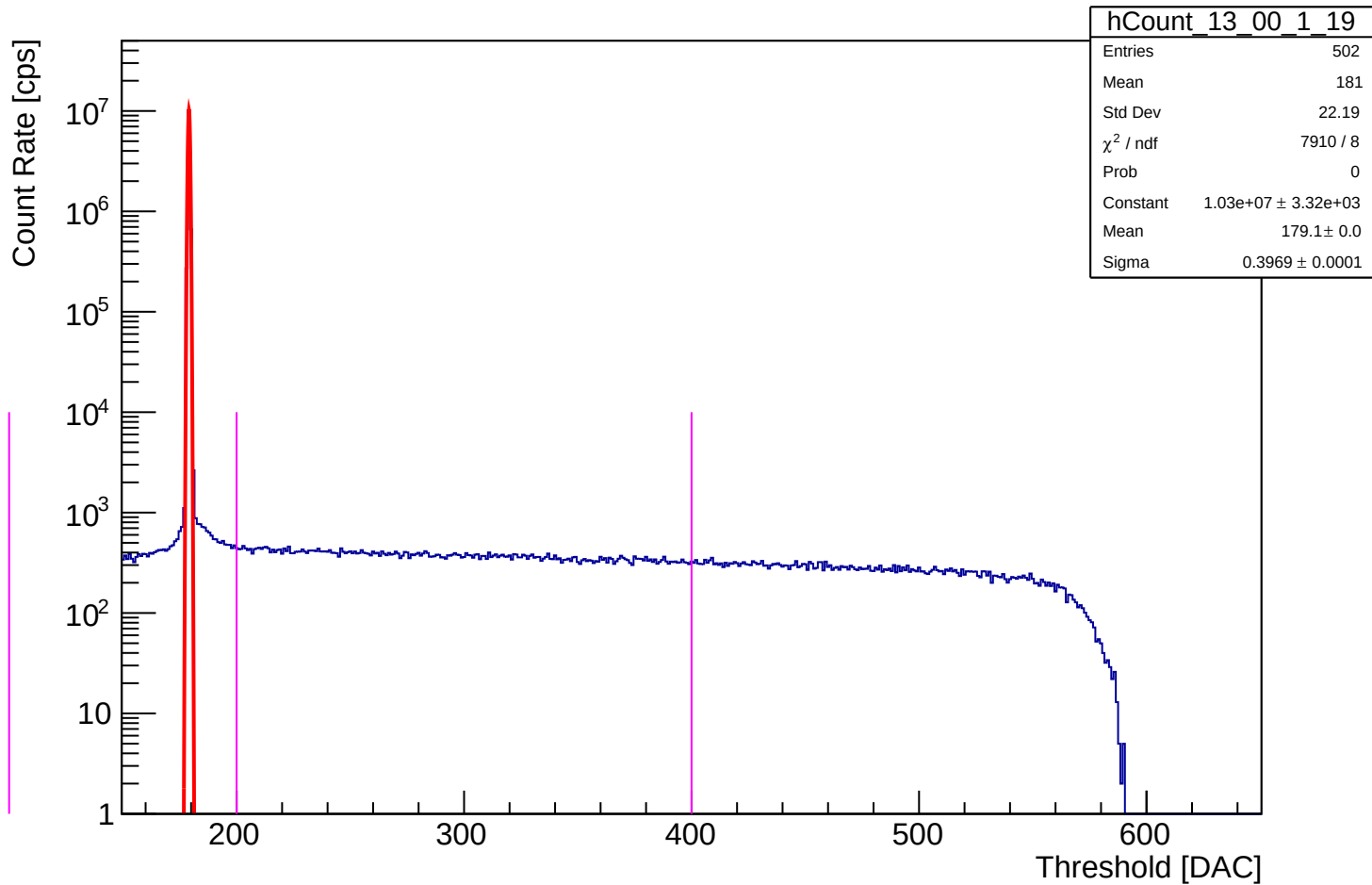
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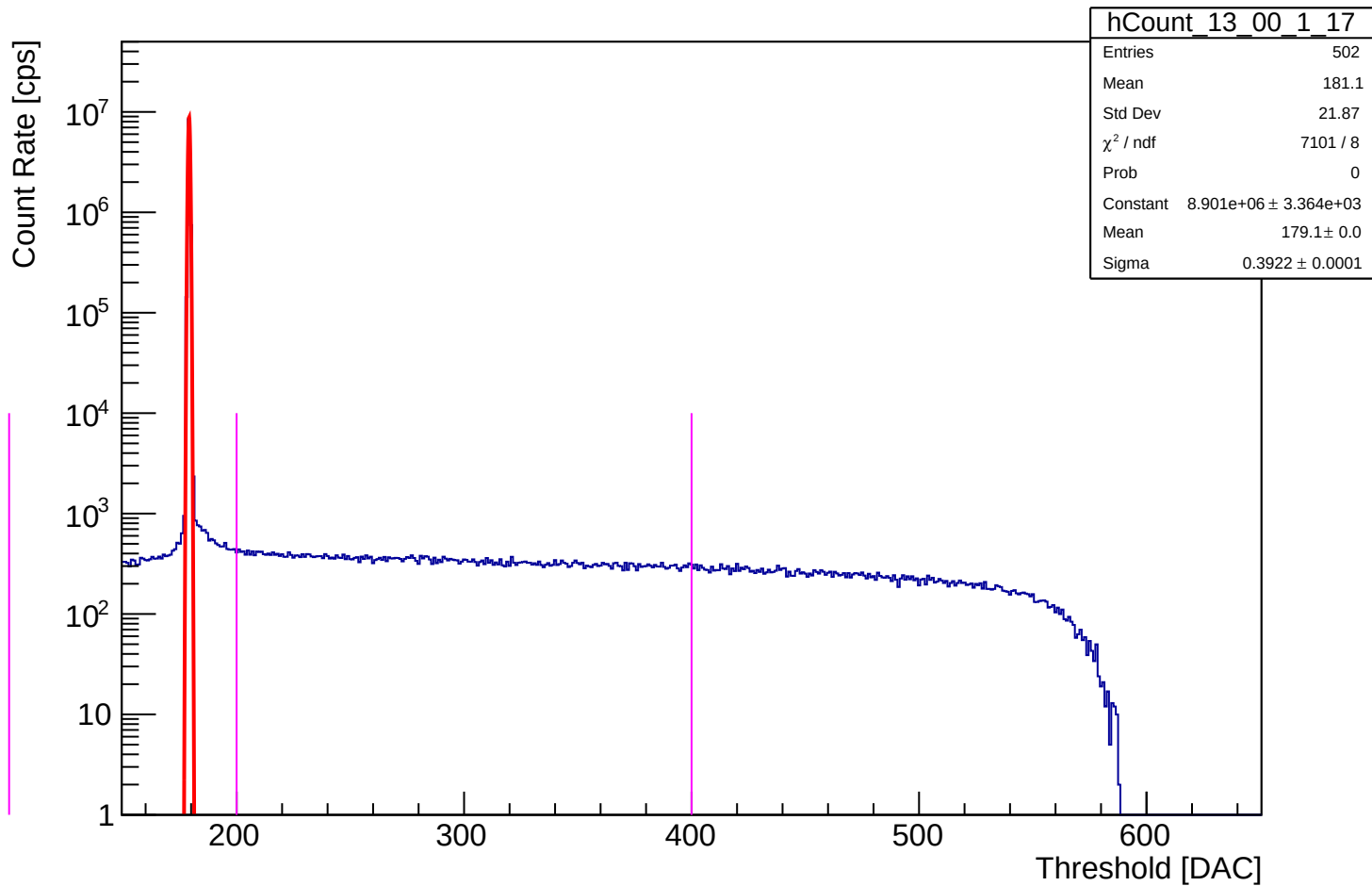
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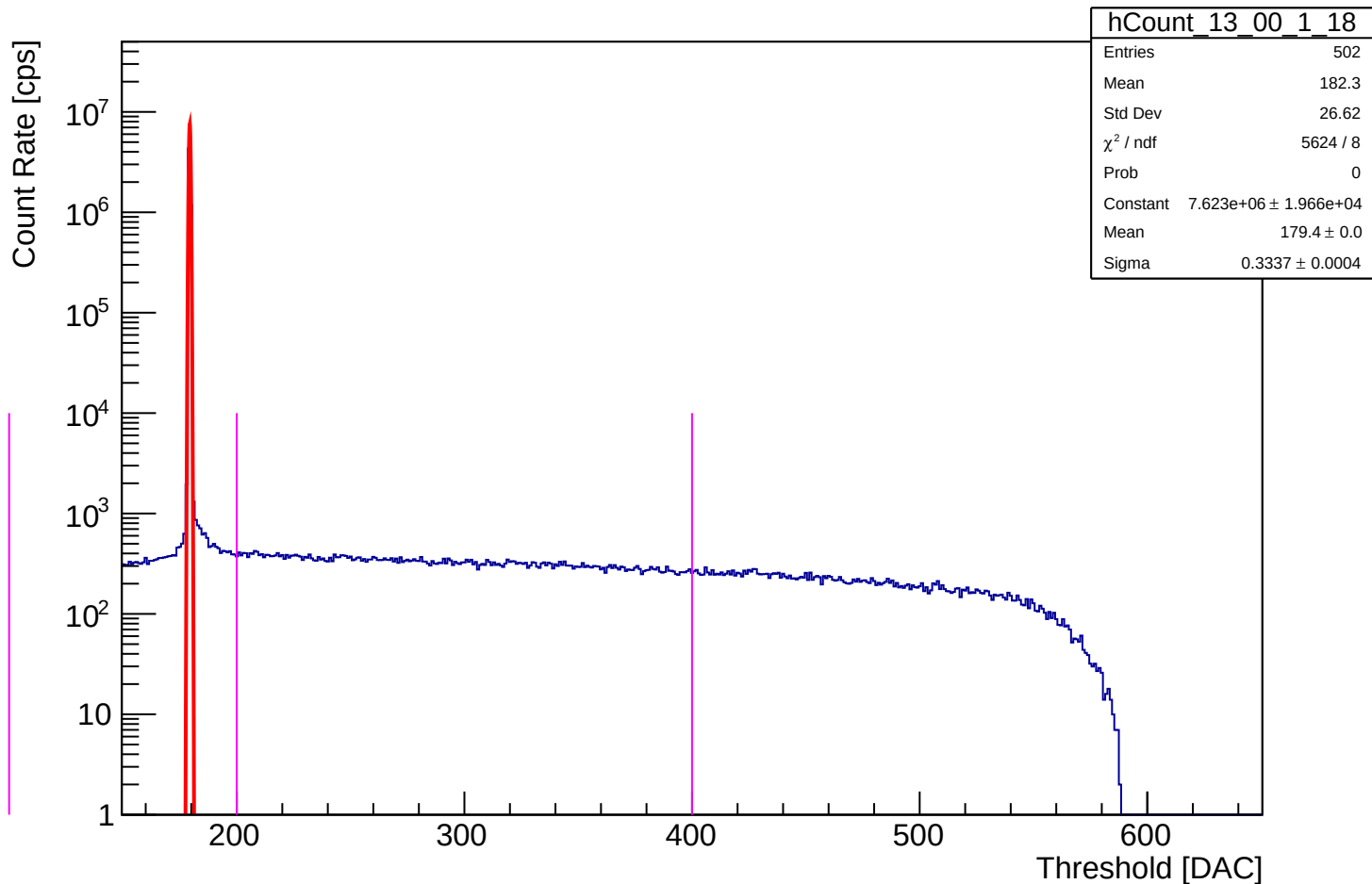
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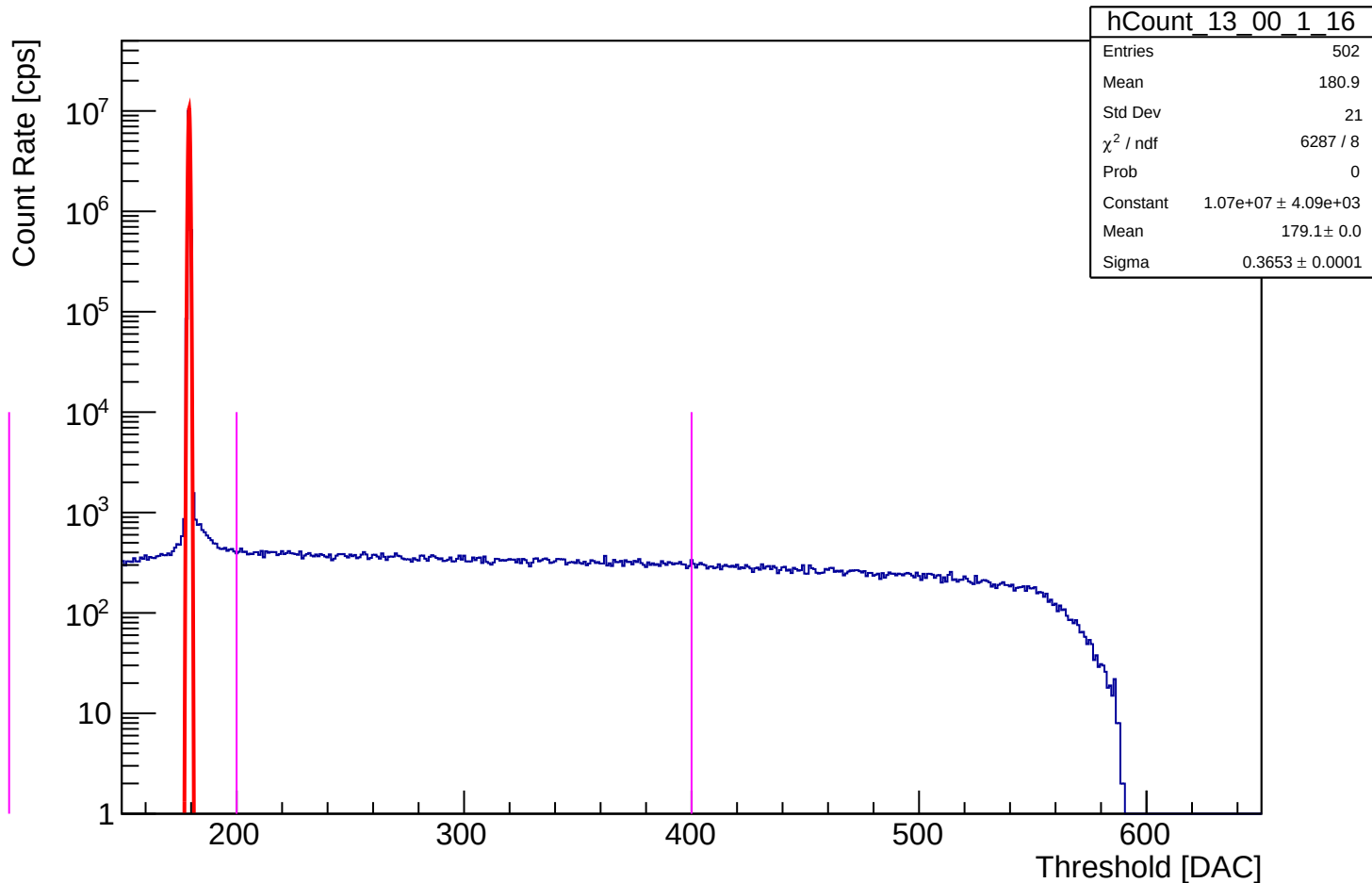
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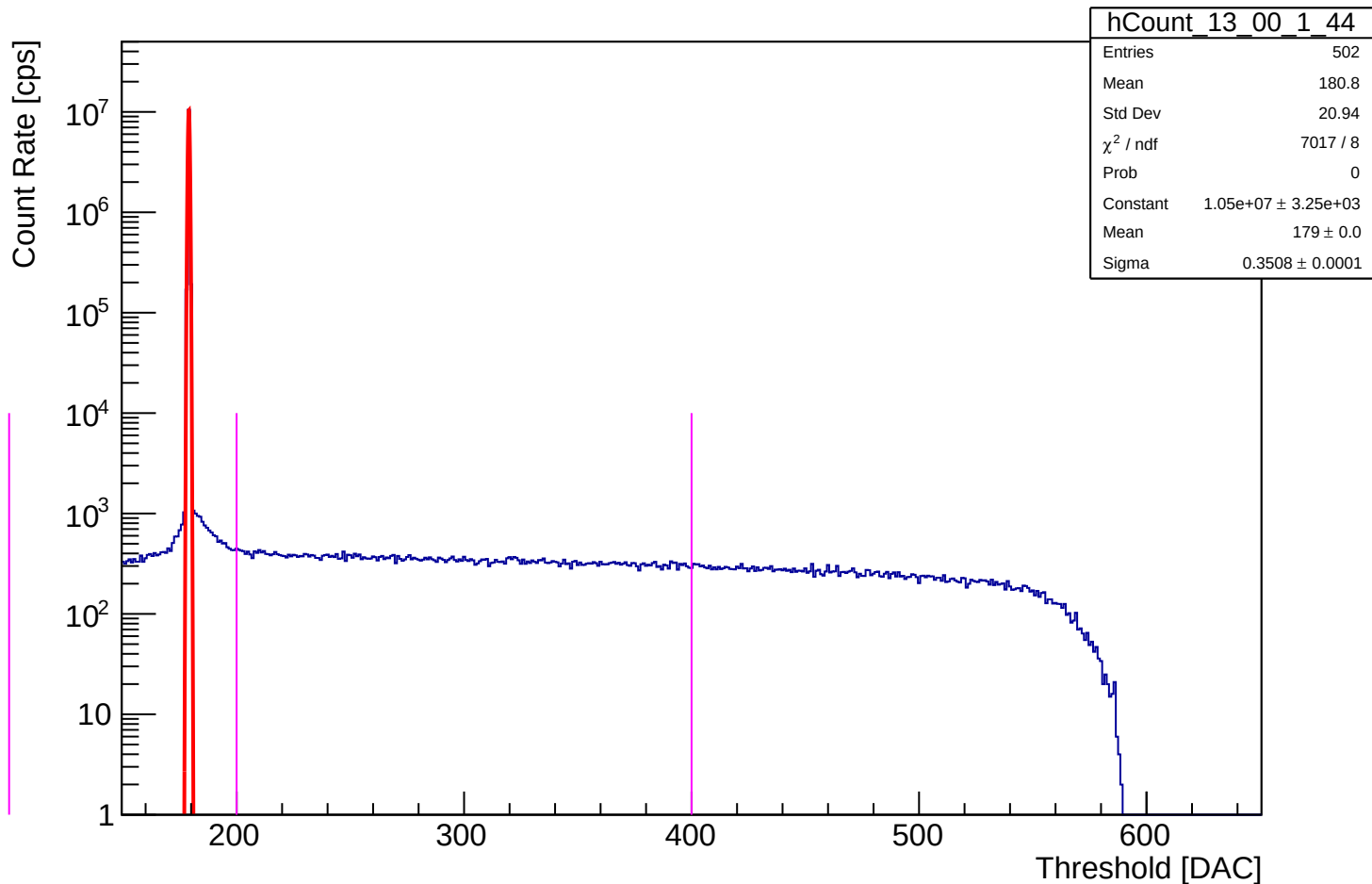
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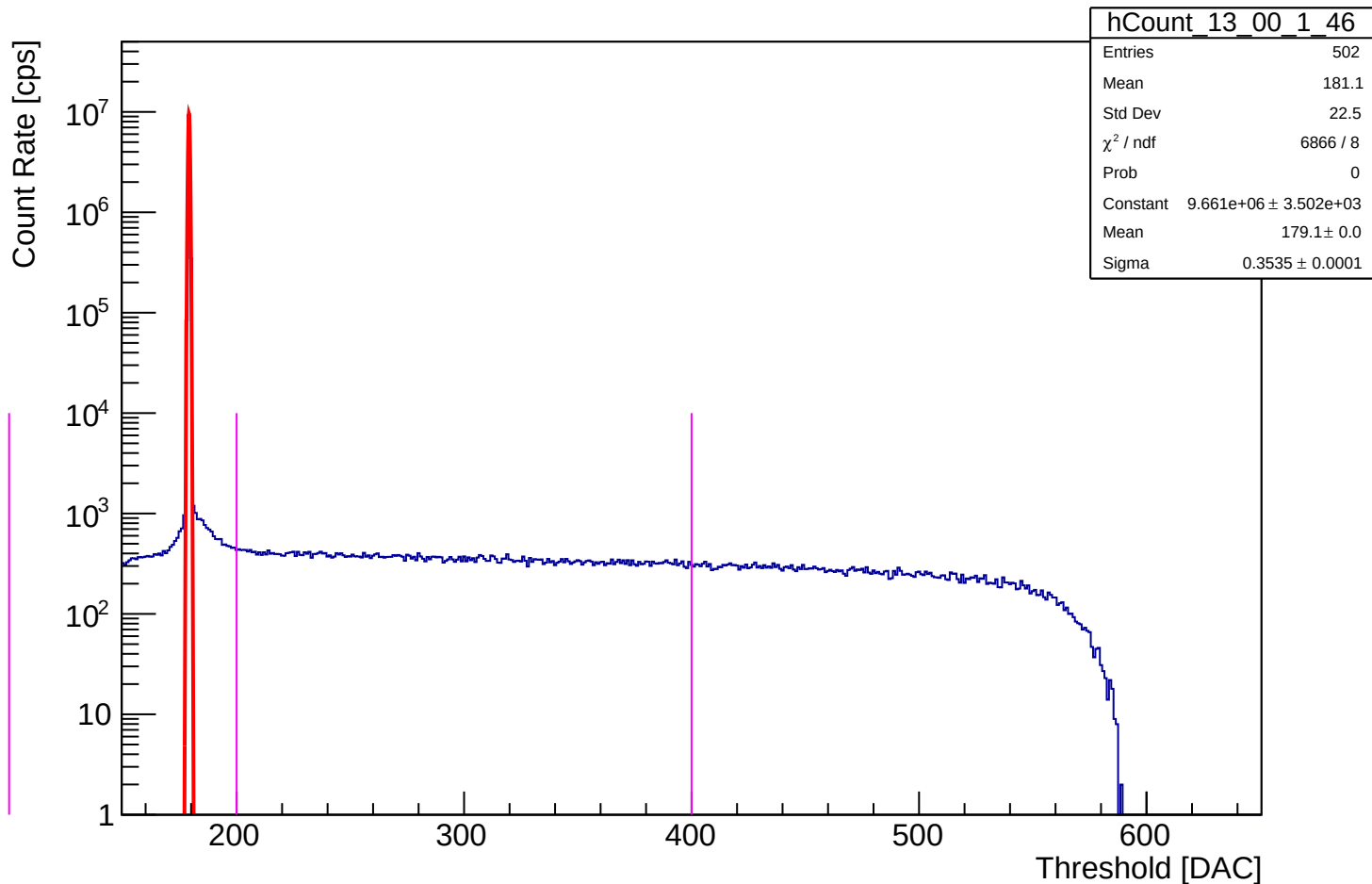
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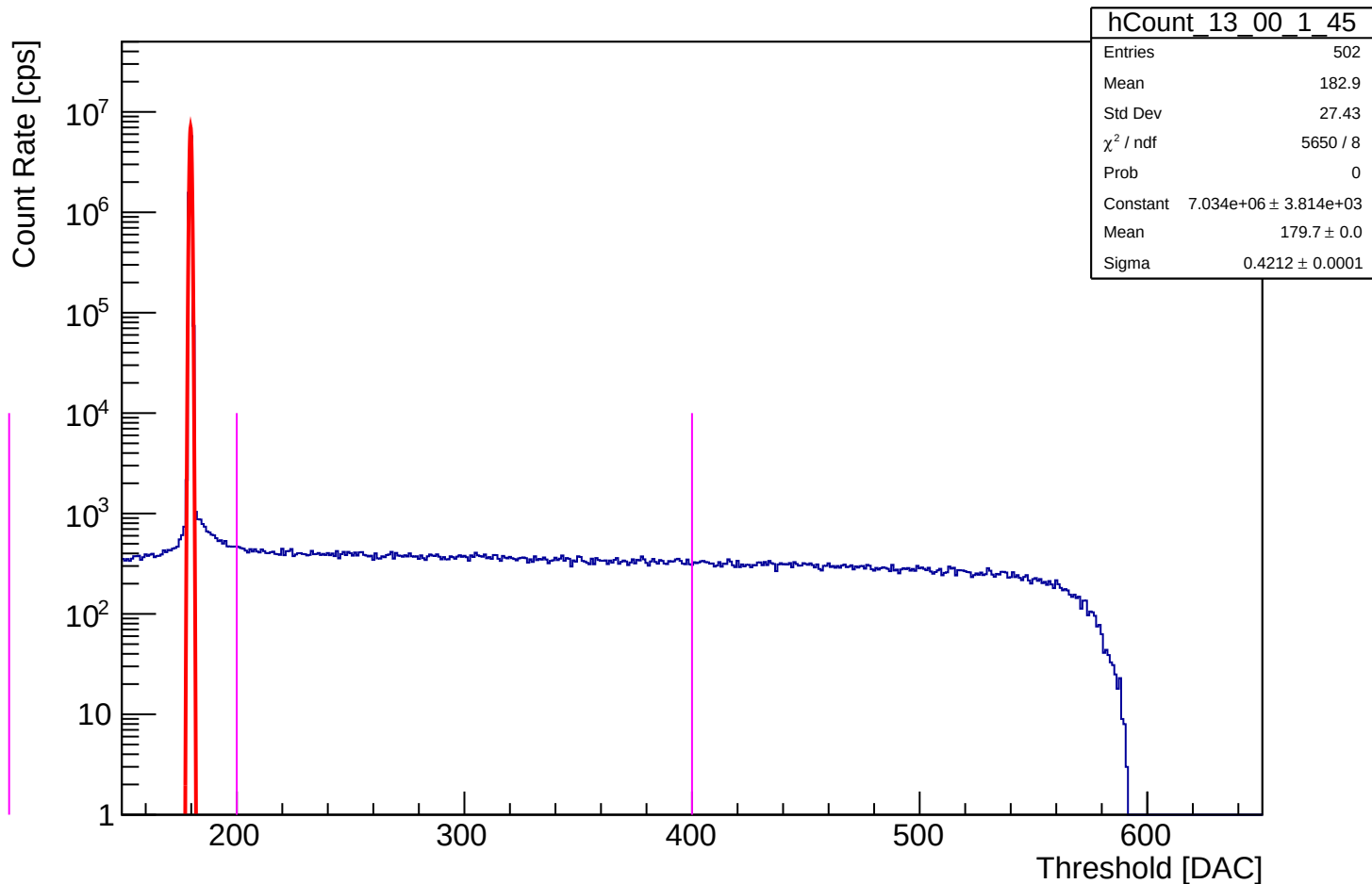
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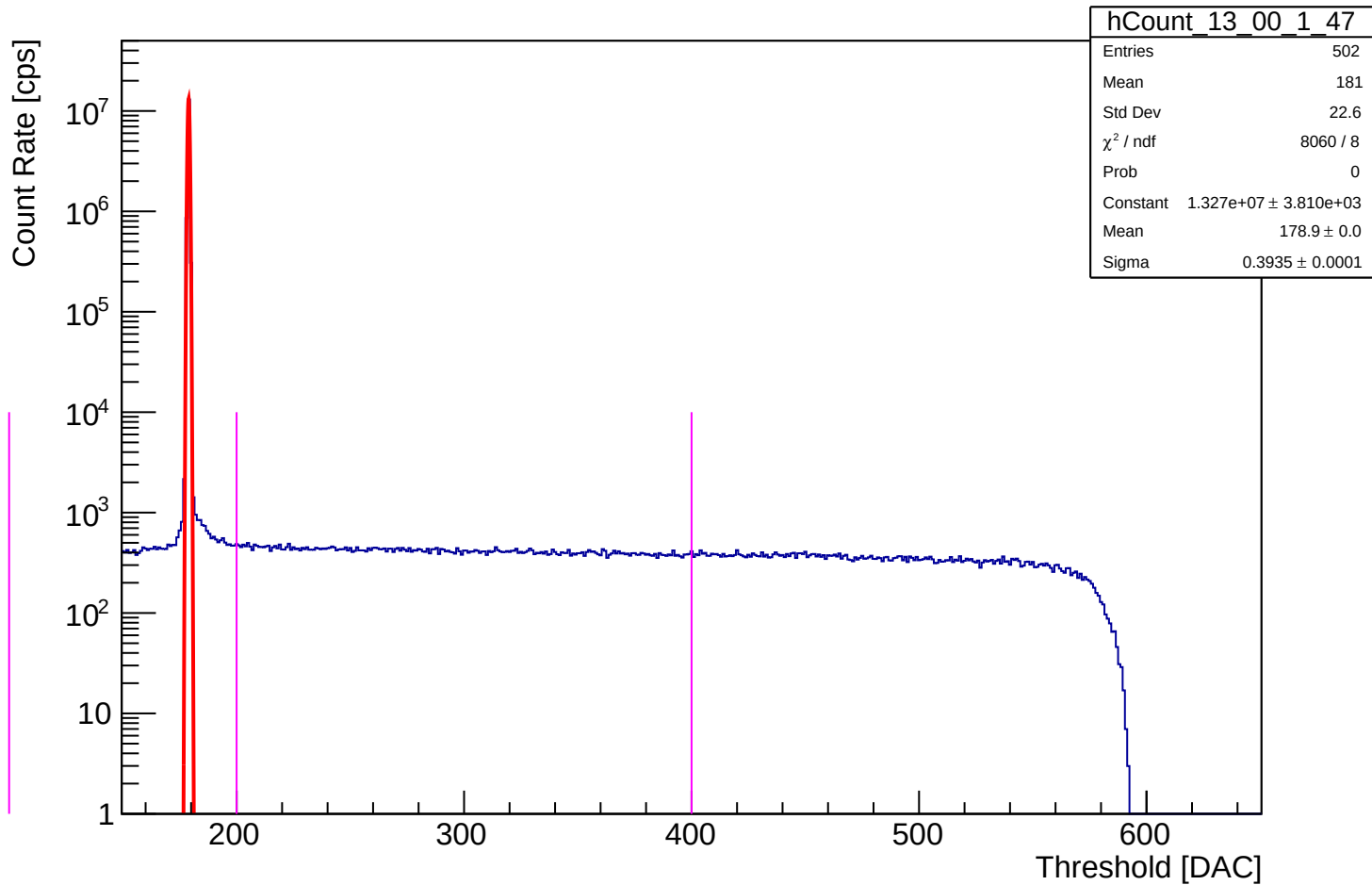
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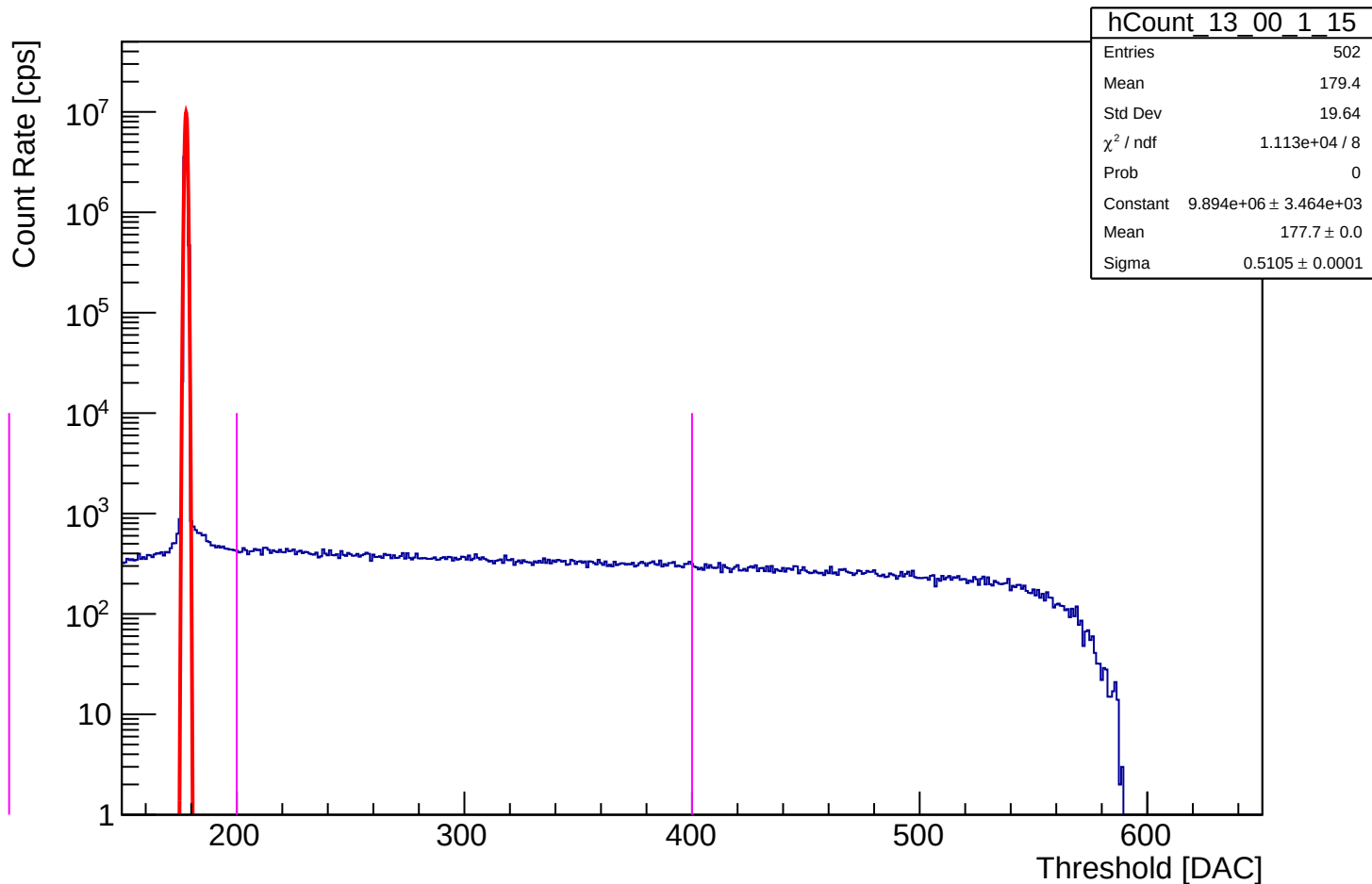
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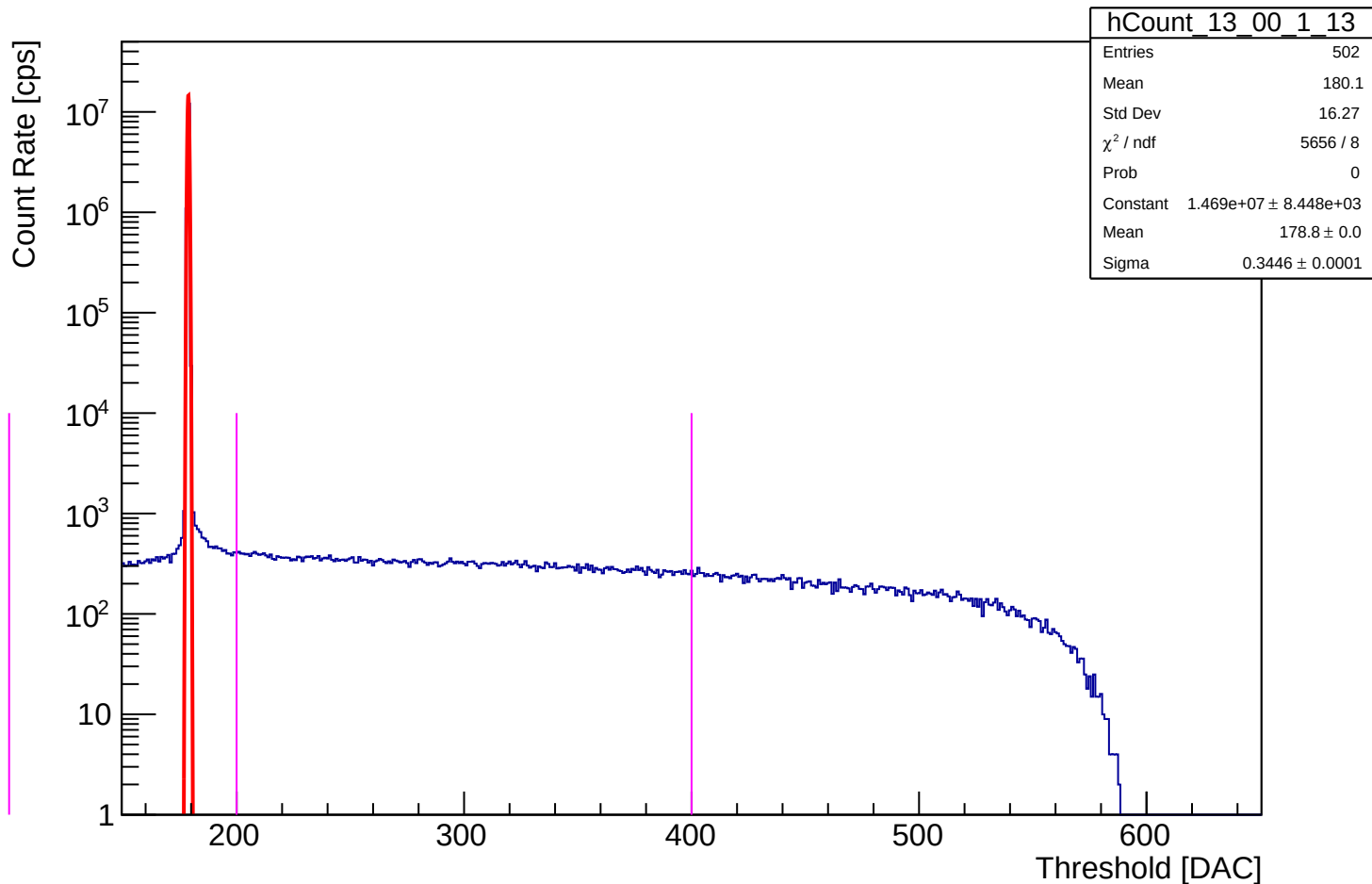
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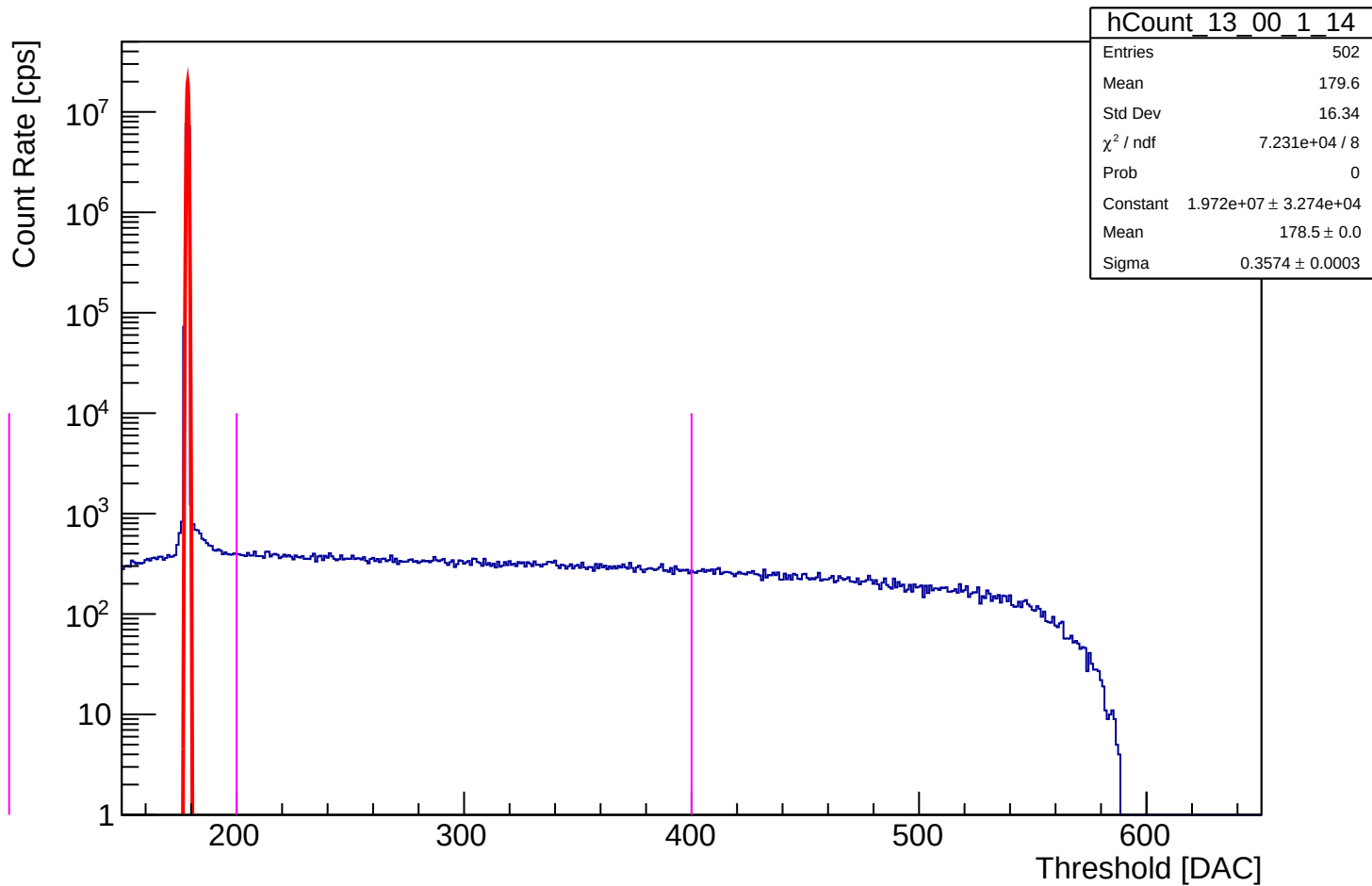
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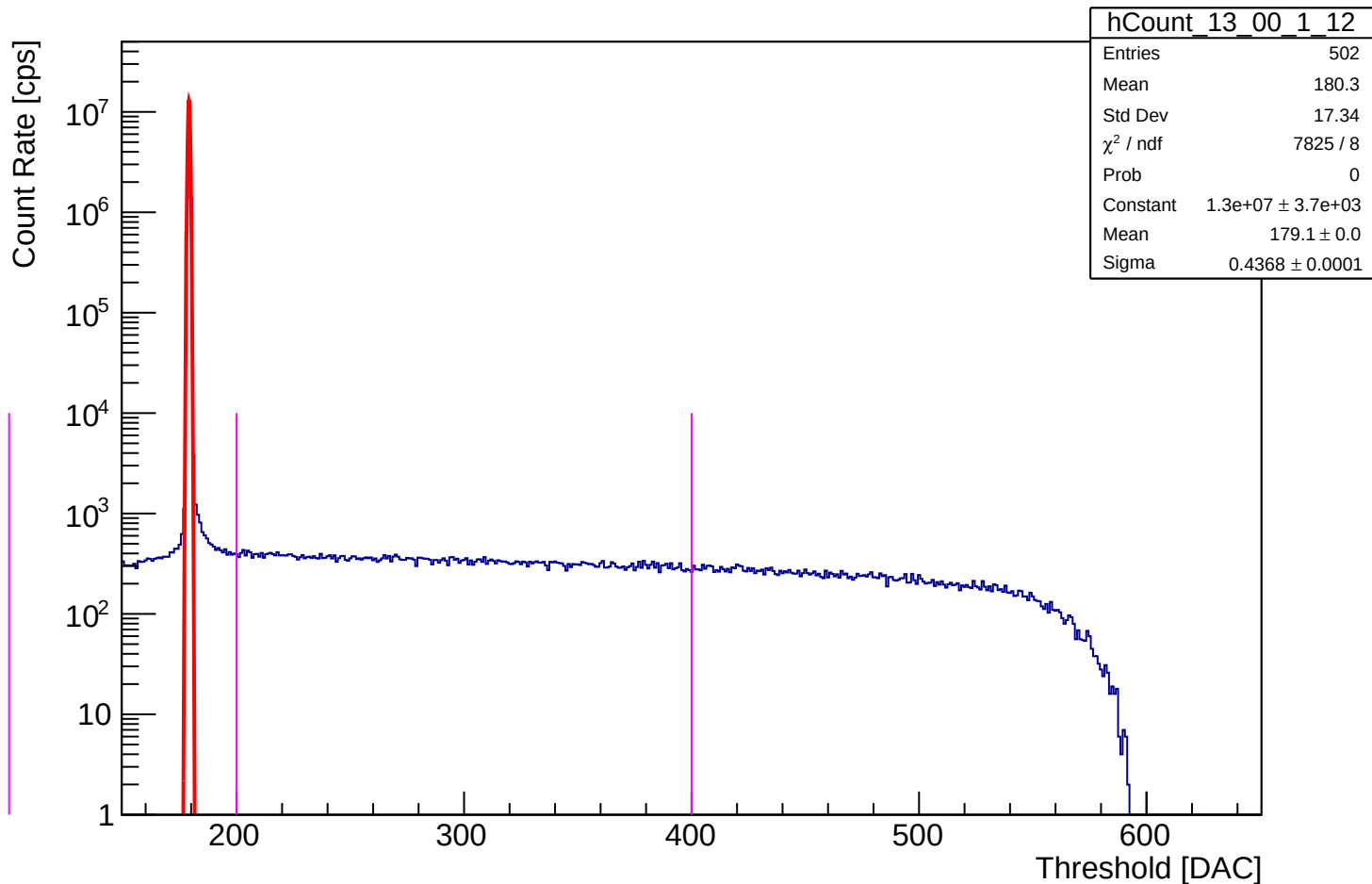
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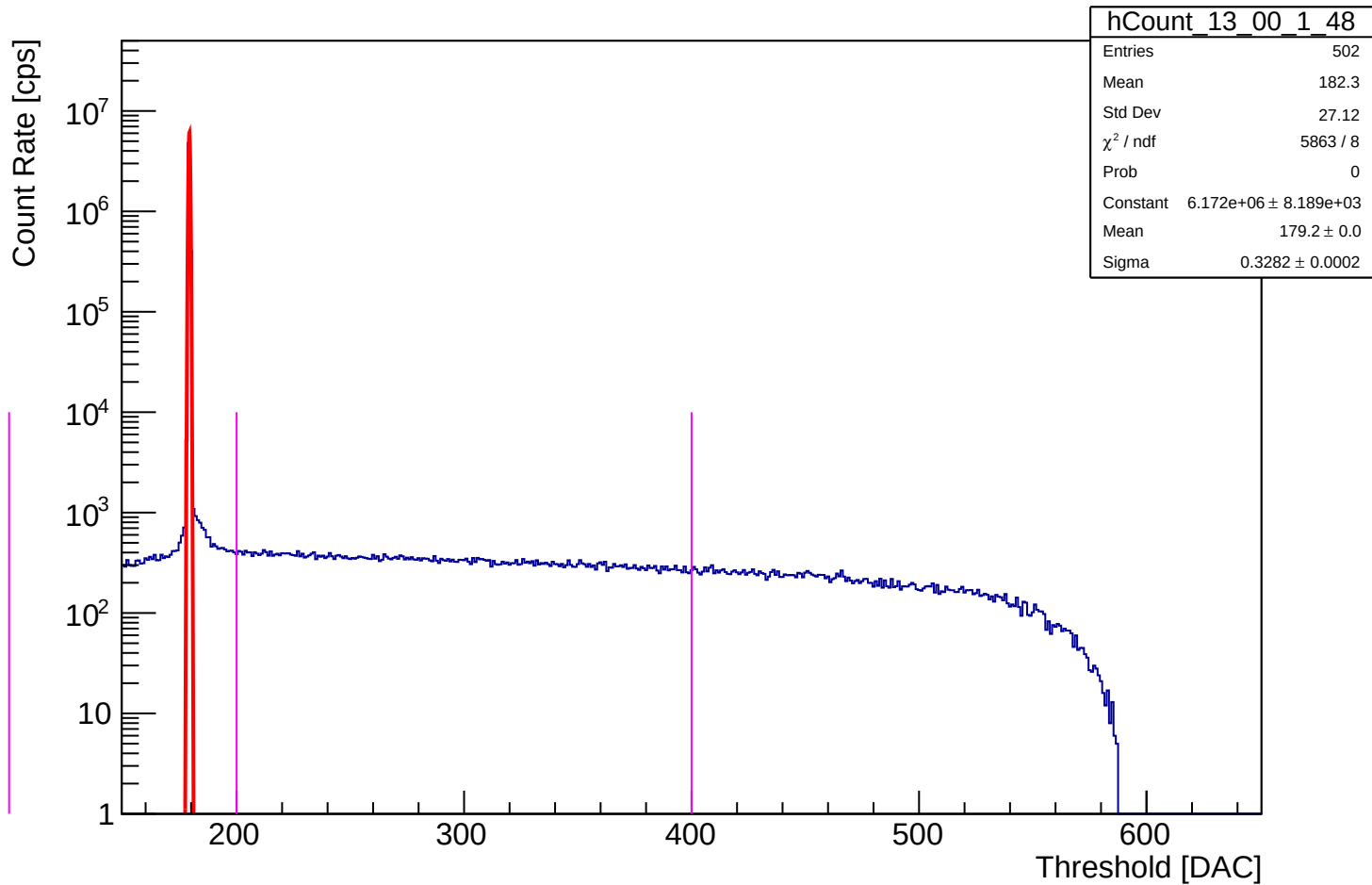
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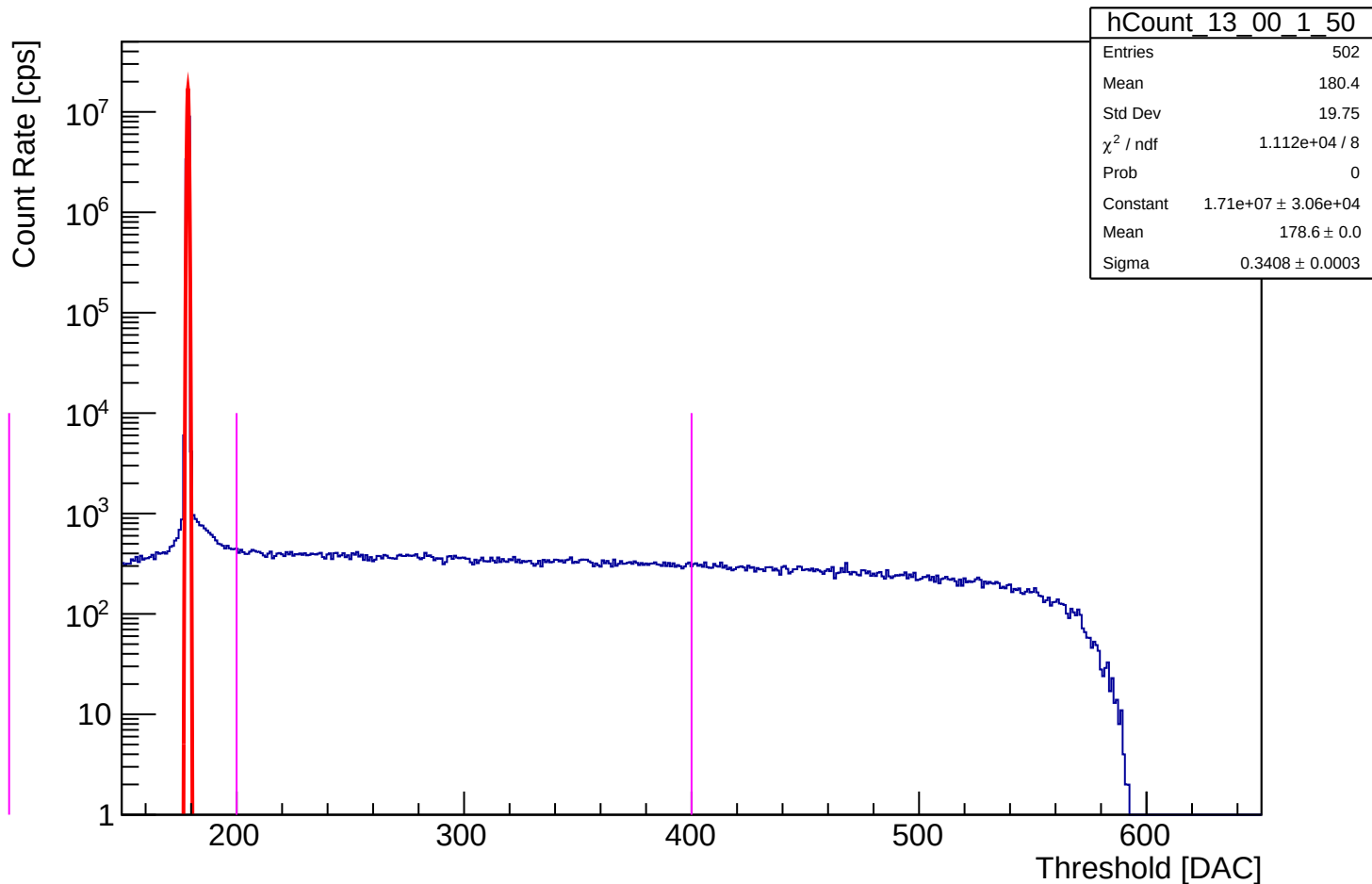
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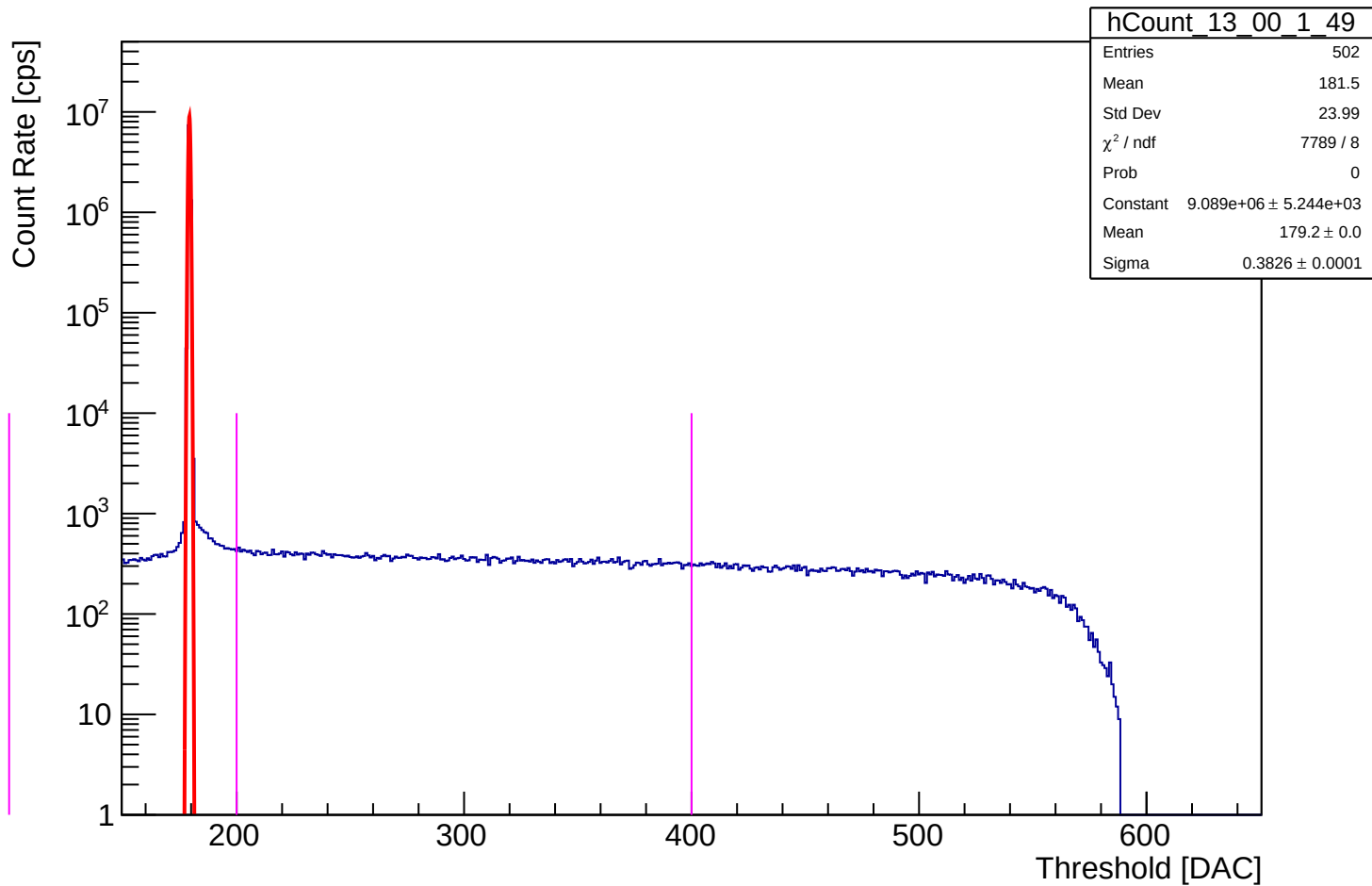
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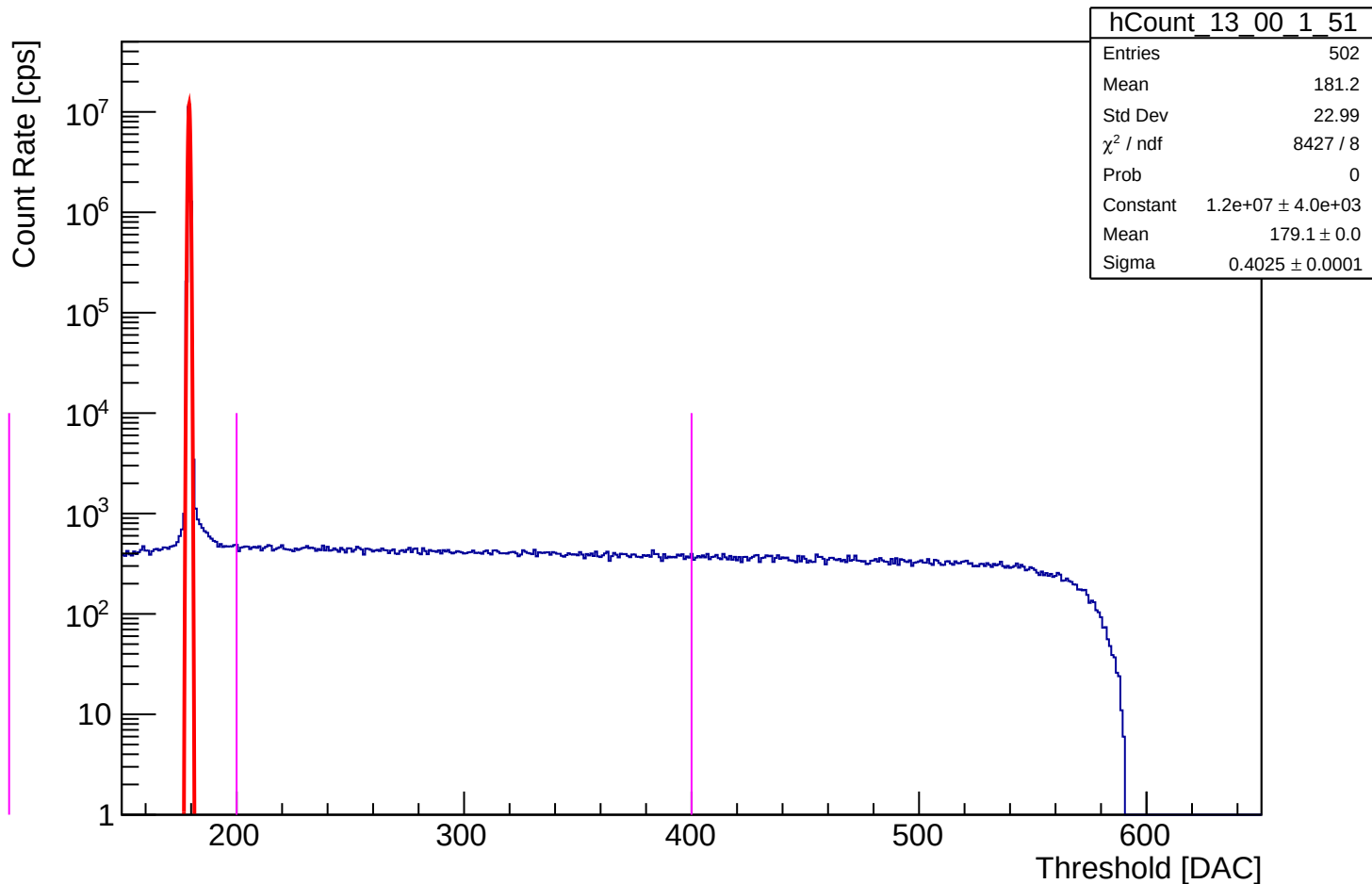
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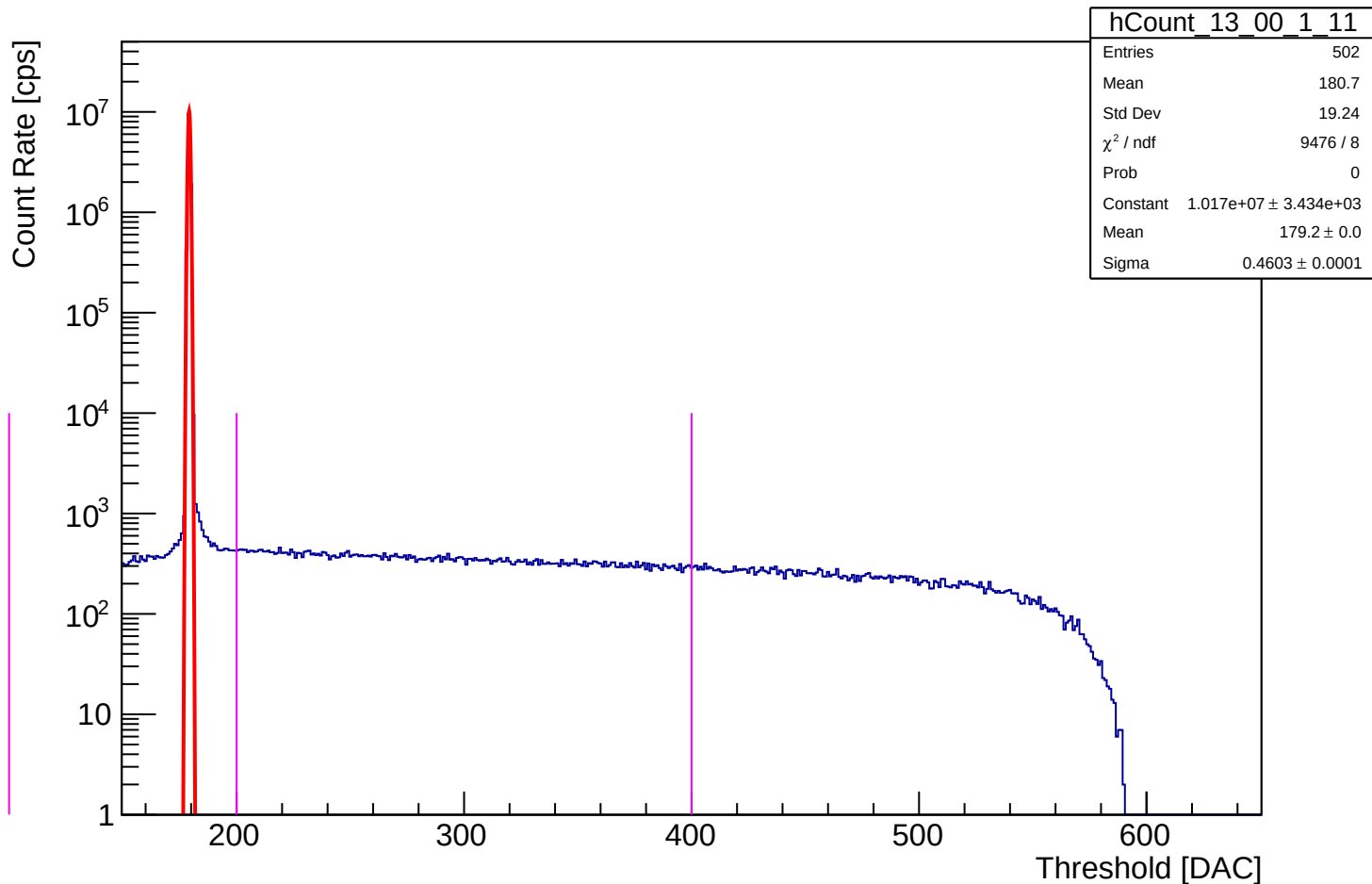
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Row 1 Tile 1 Pmt 2 Pixel 40 Slot 13 Fiber 0 Asic 1 Channel 51

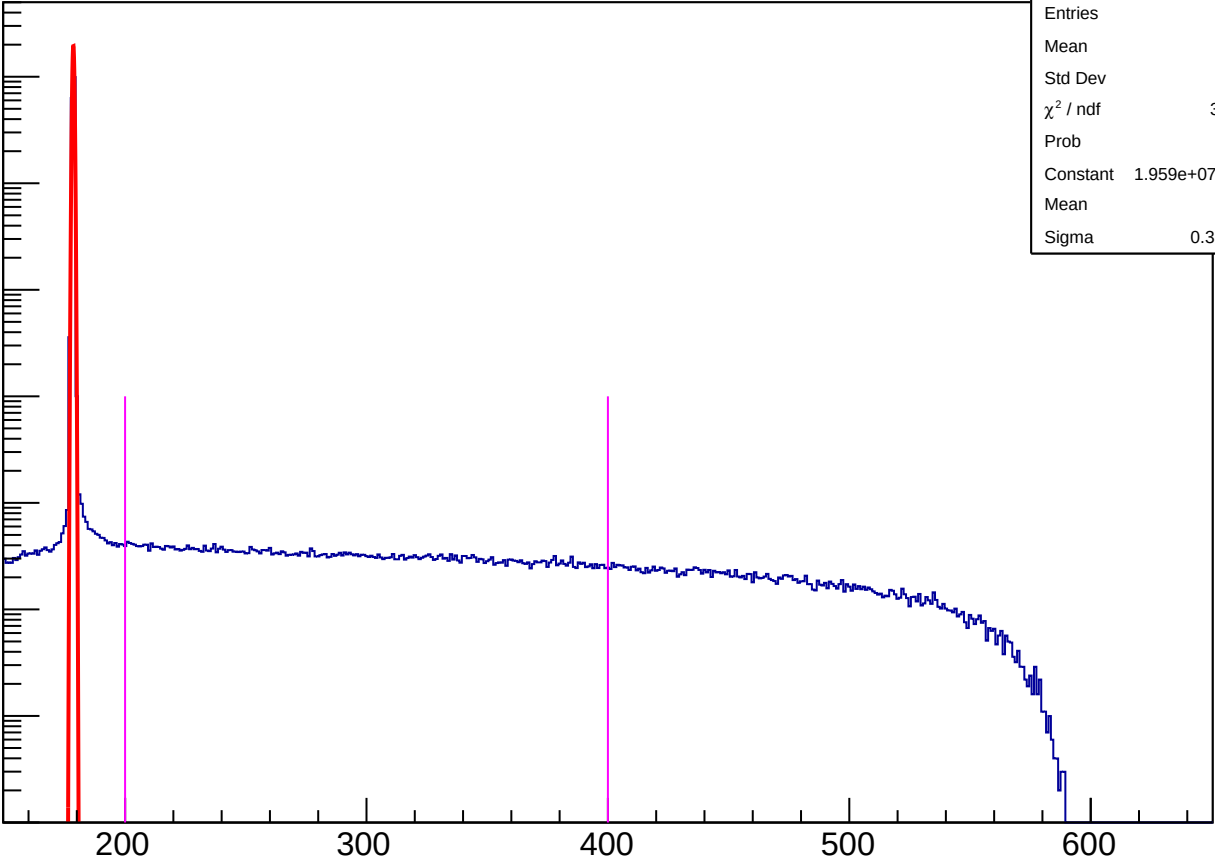


Row 1 Tile 1 Pmt 2 Pixel 41 Slot 13 Fiber 0 Asic 1 Channel 11



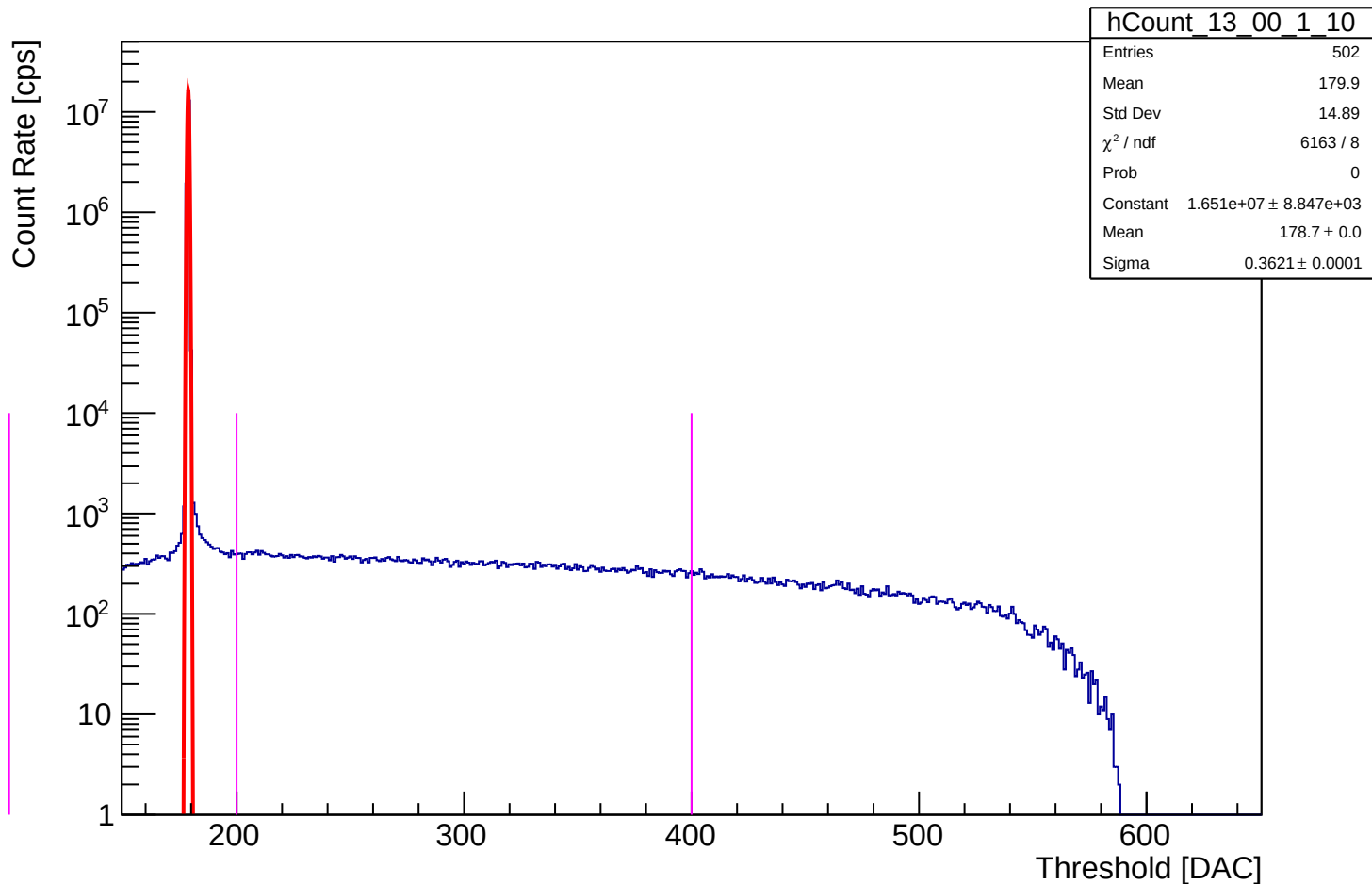
Count Rate [cps]

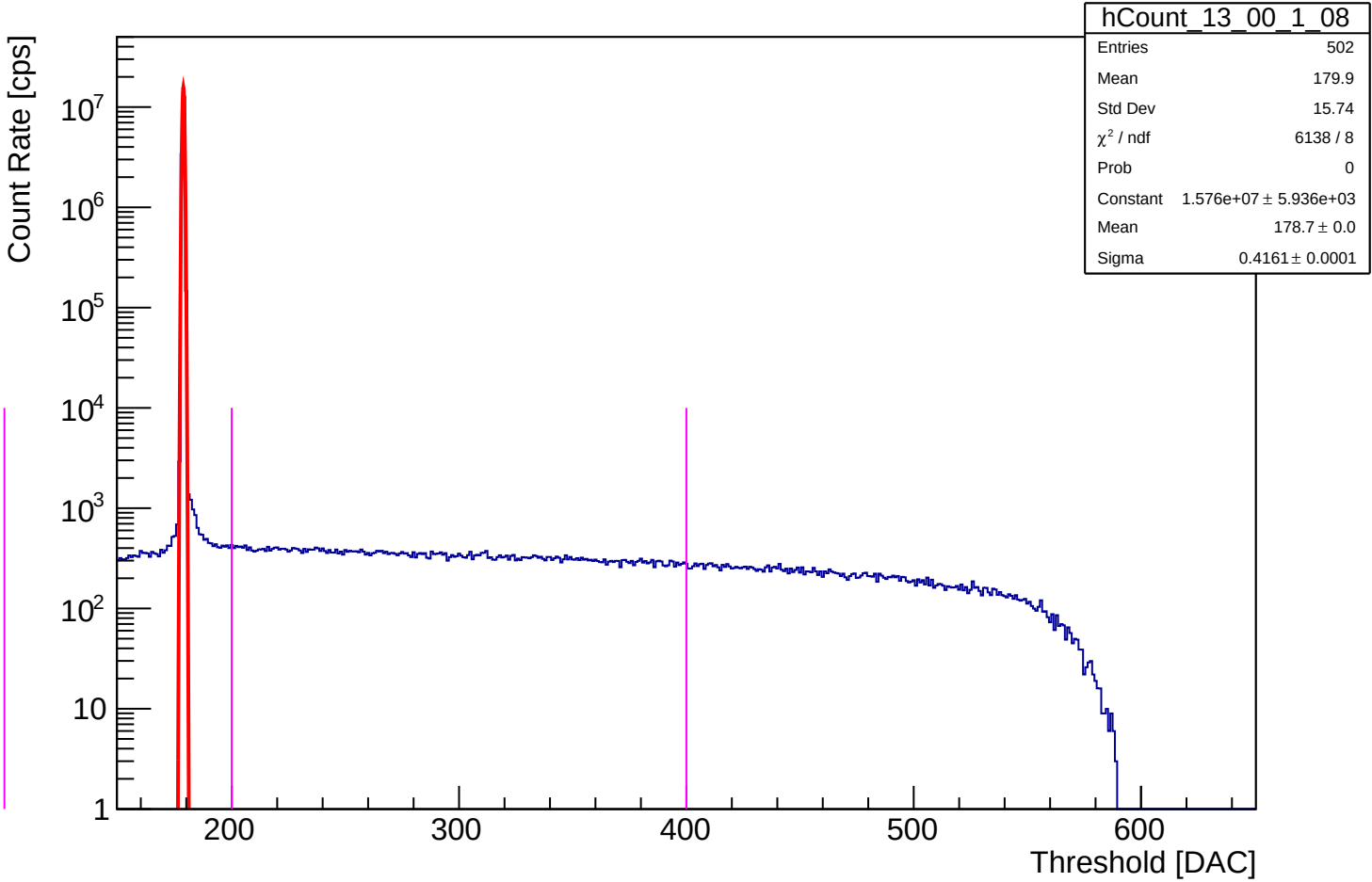
10⁷
10⁶
10⁵
10⁴
10³
10²
10
1



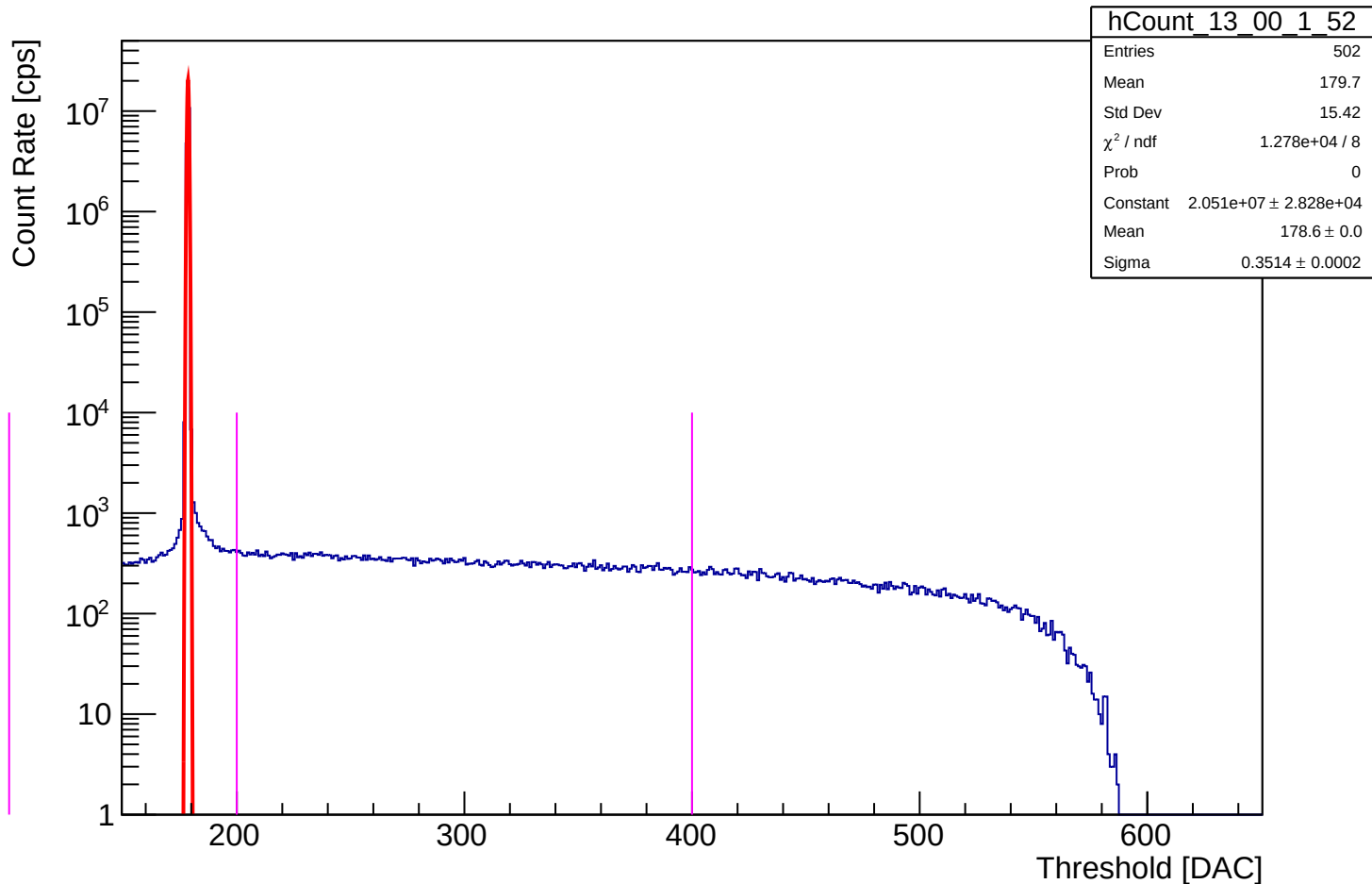
hCount_13_00_1_09	
Entries	502
Mean	179.6
Std Dev	14.74
χ^2 / ndf	3.592e+04 / 8
Prob	0
Constant	1.959e+07 ± 2.017e+04
Mean	178.6 ± 0.0
Sigma	0.3744 ± 0.0002

Row 1 Tile 1 Pmt 2 Pixel 43 Slot 13 Fiber 0 Asic 1 Channel 10

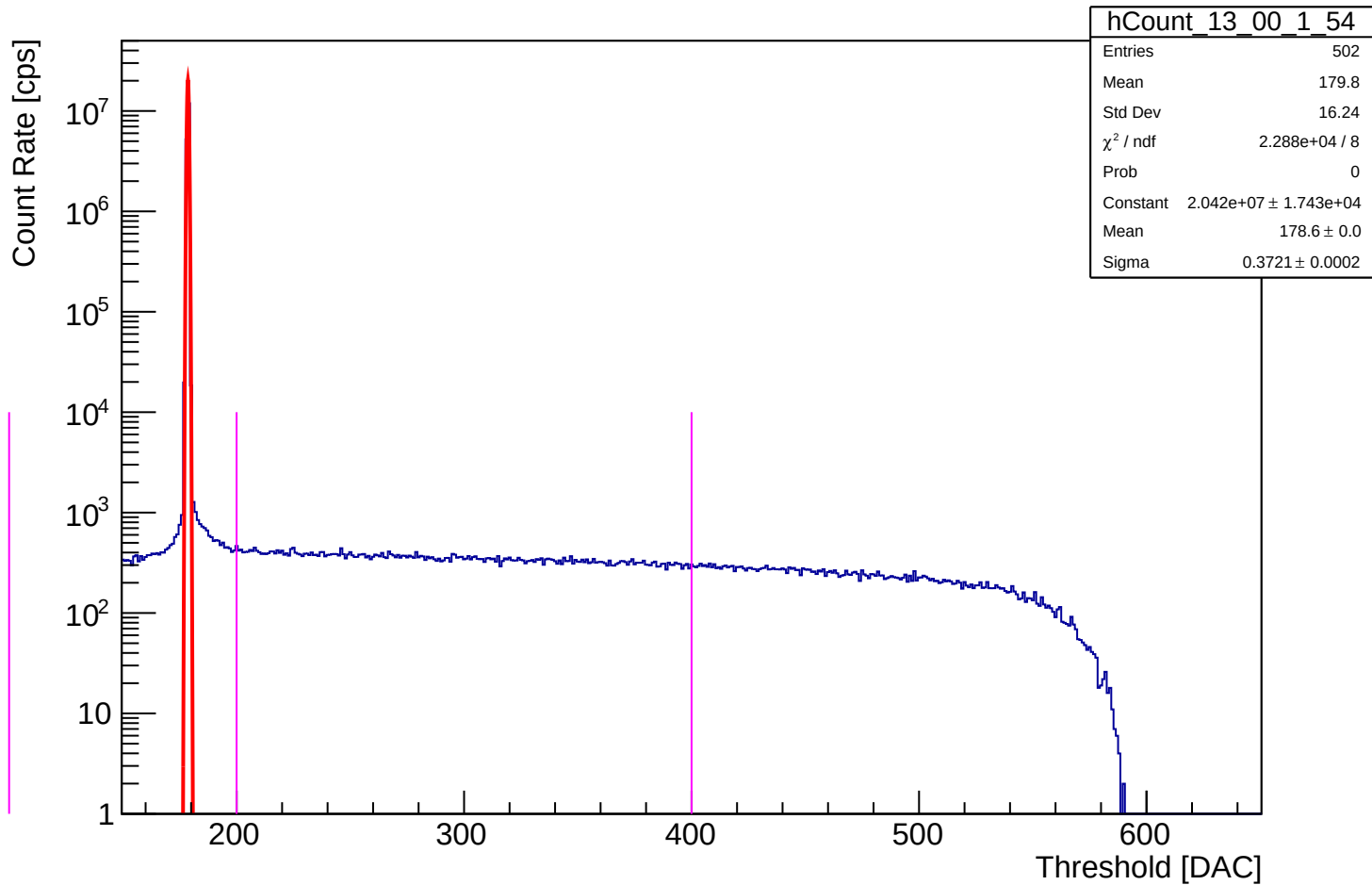




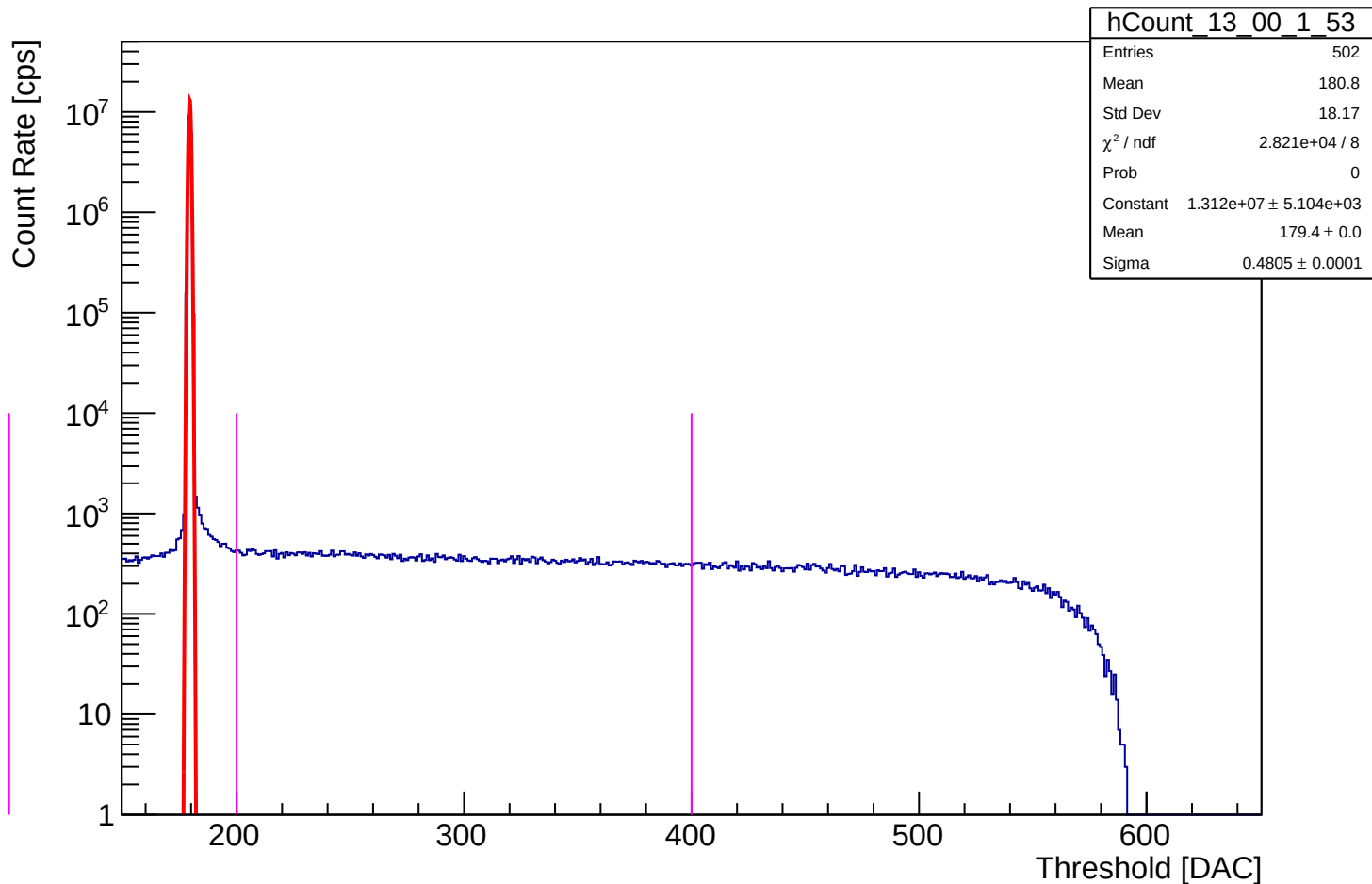
Row 1 Tile 1 Pmt 2 Pixel 45 Slot 13 Fiber 0 Asic 1 Channel 52



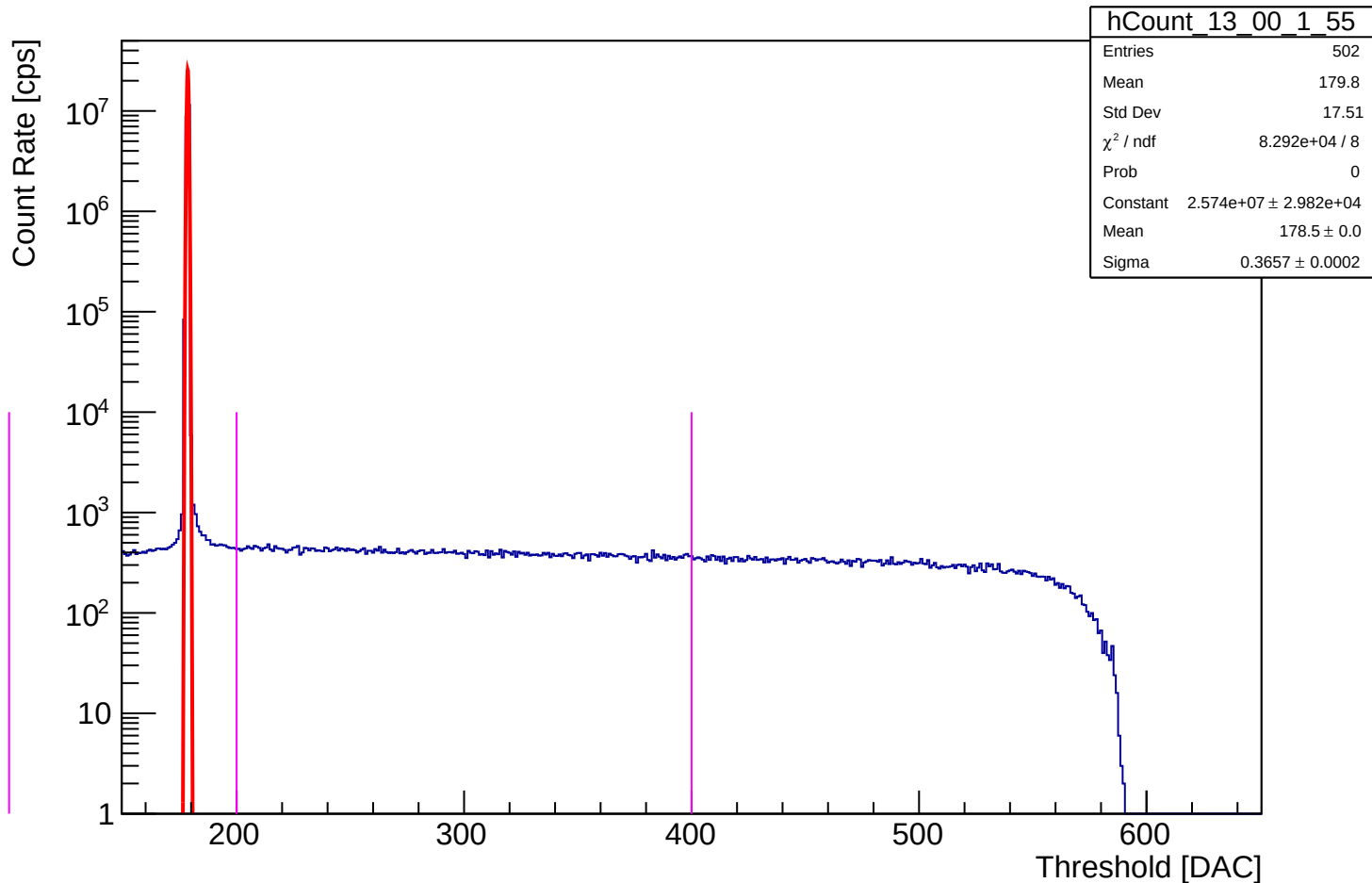
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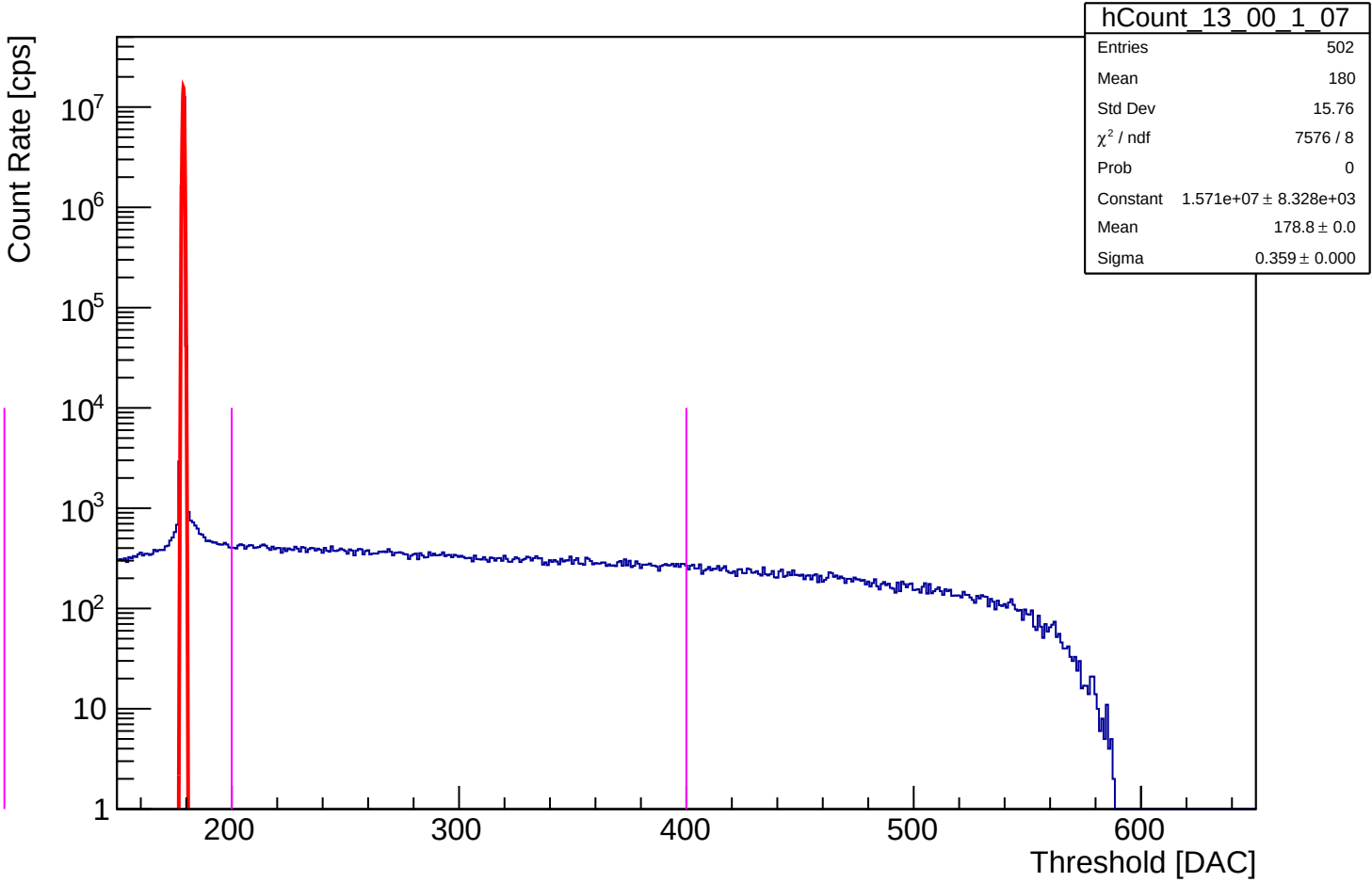


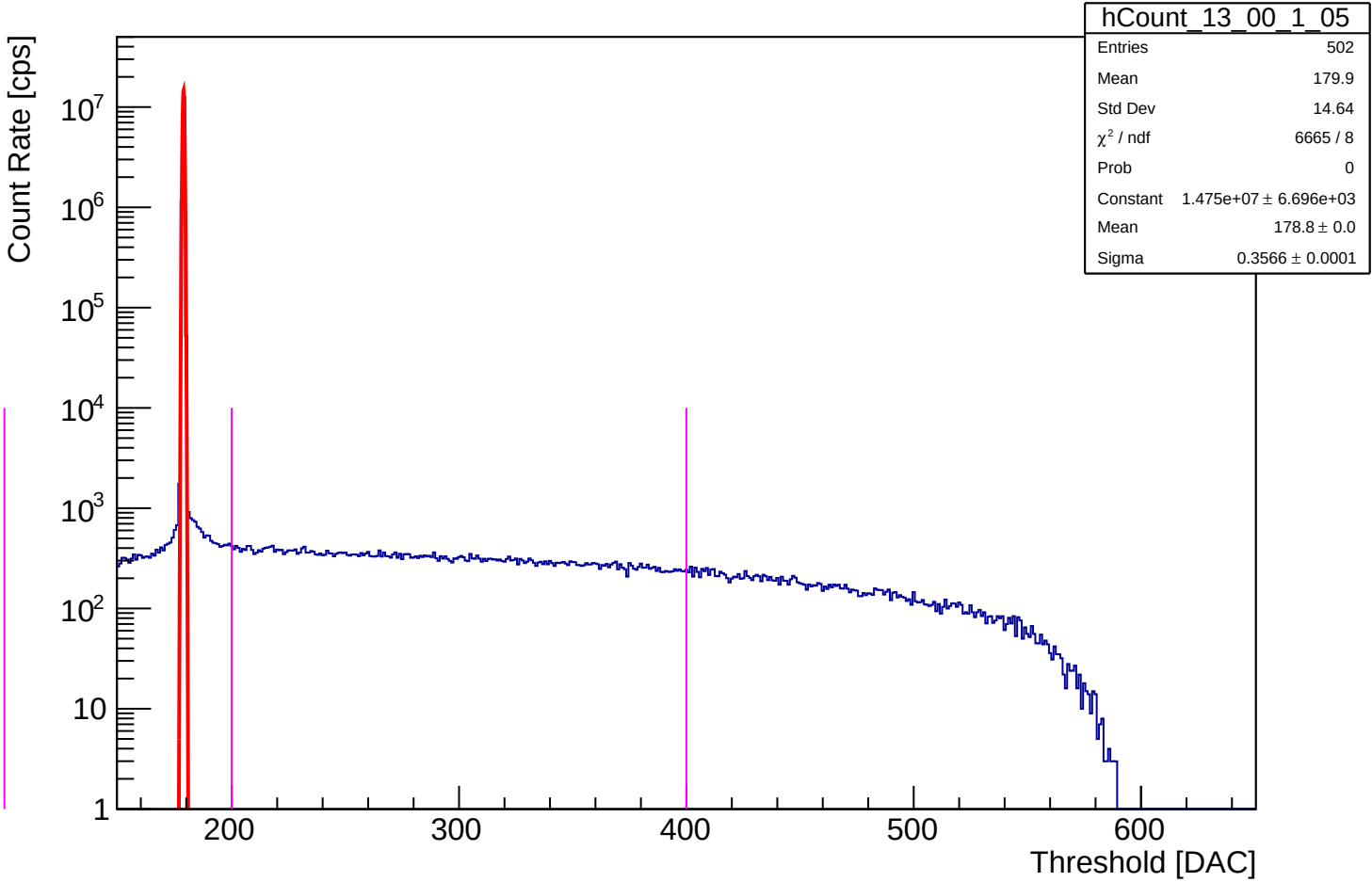
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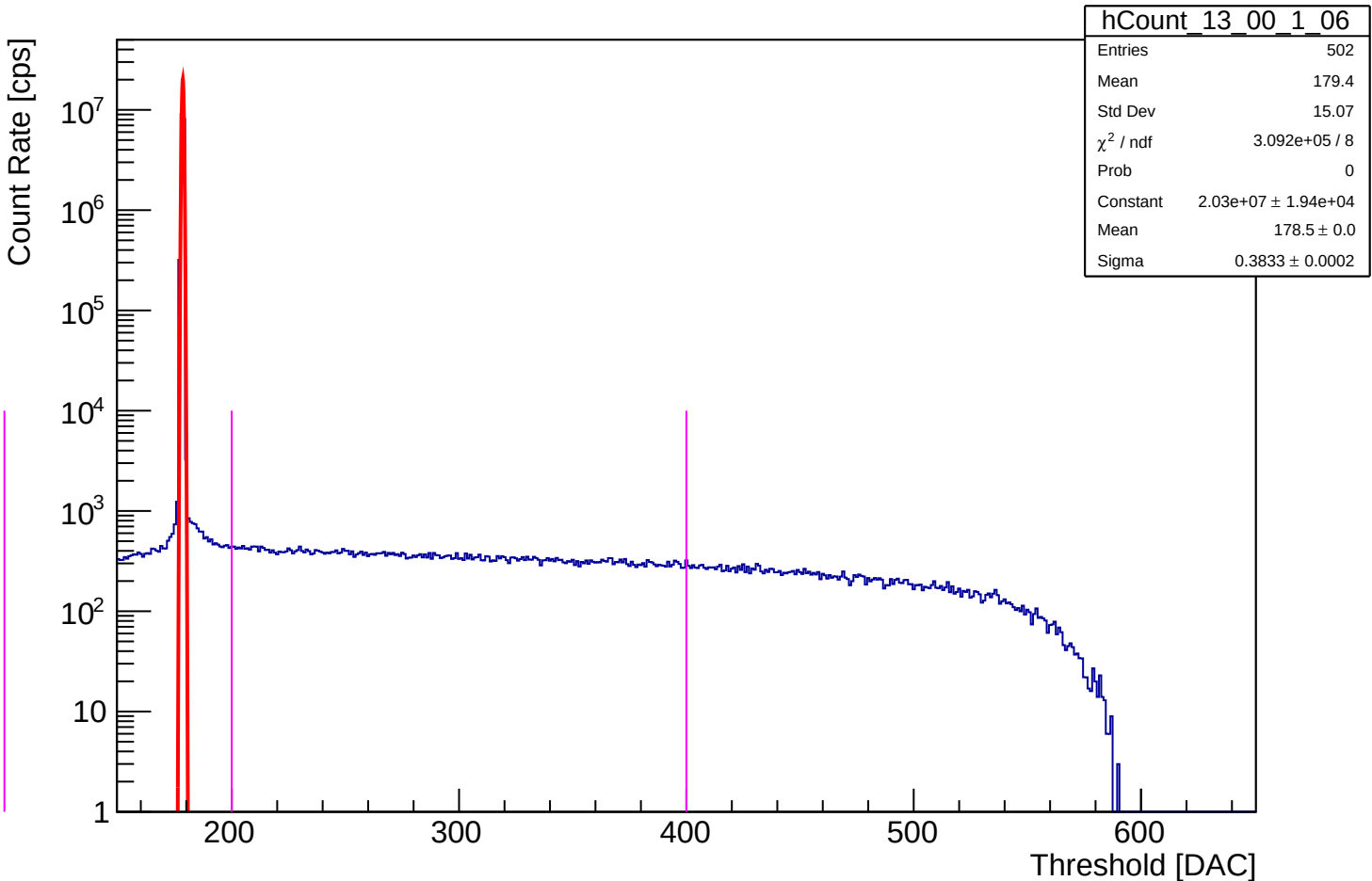


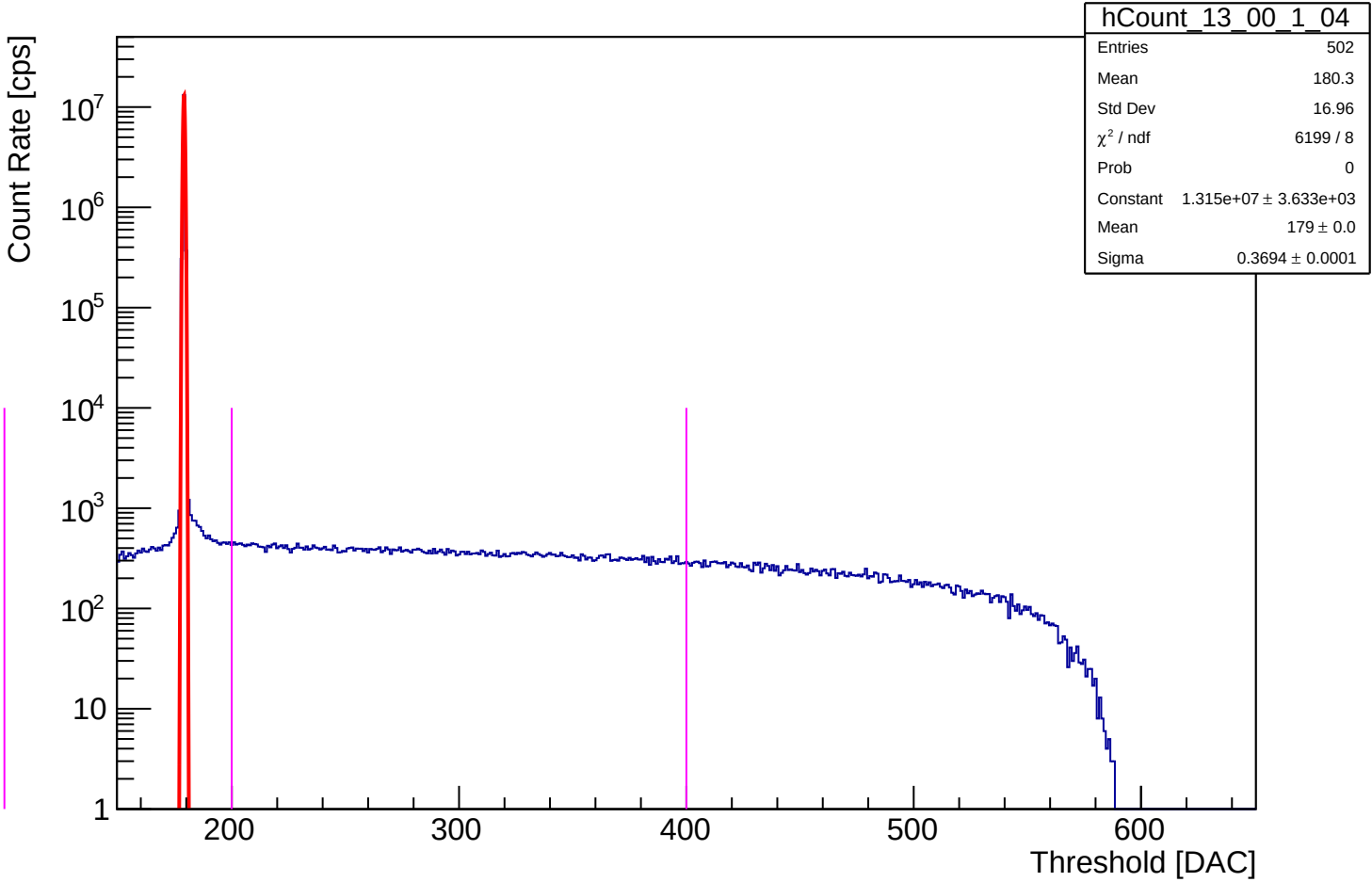
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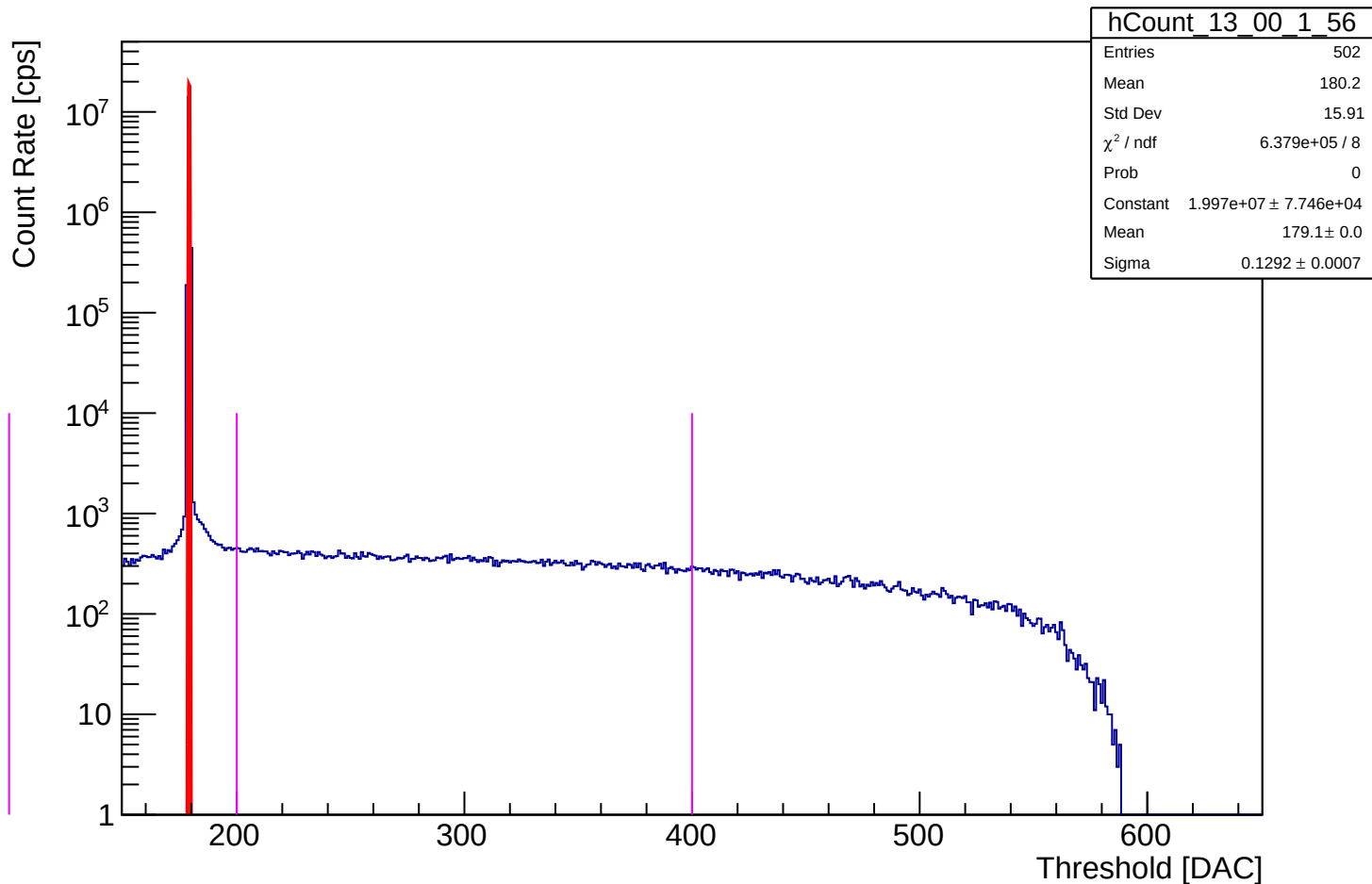




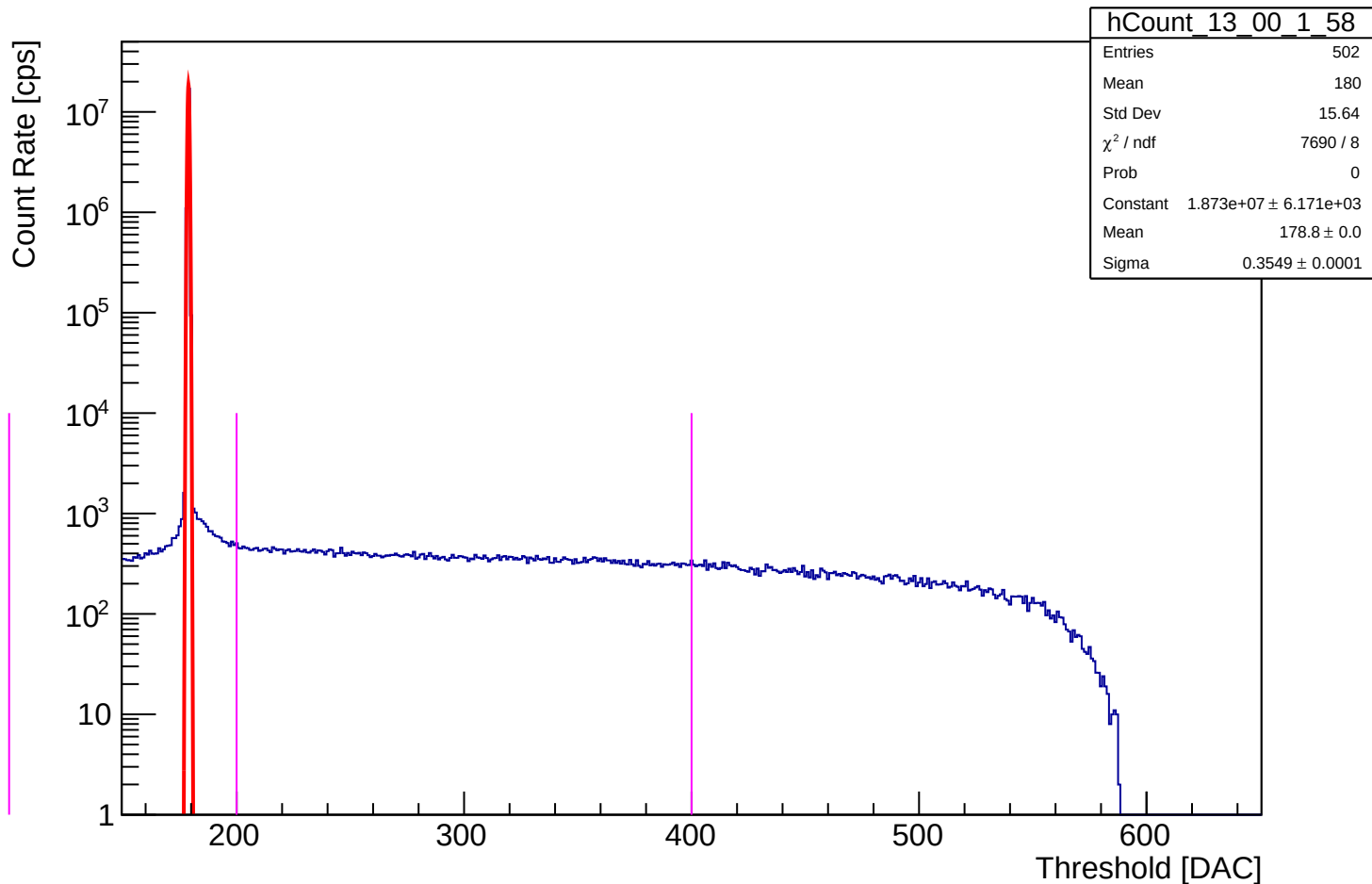




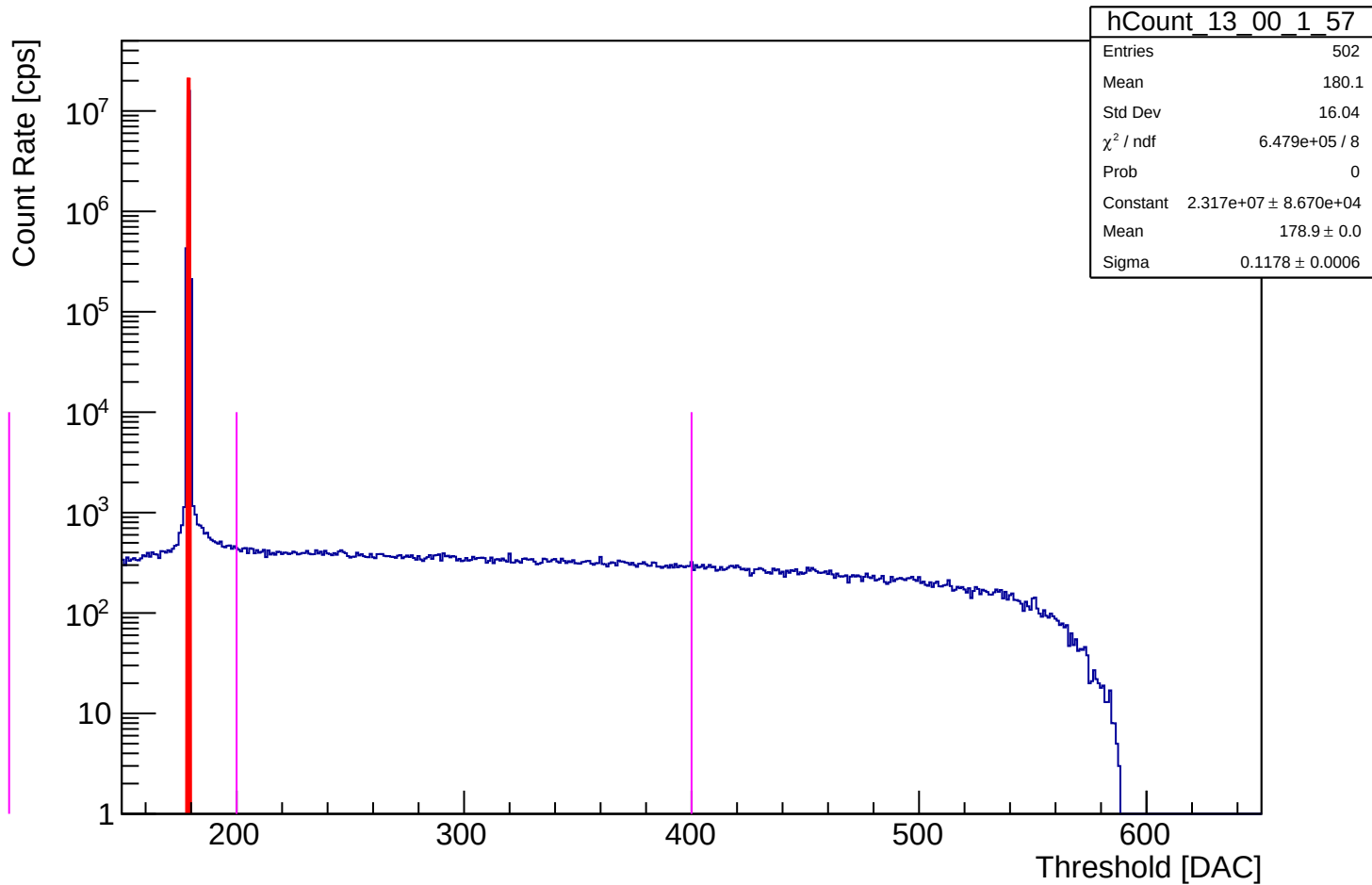
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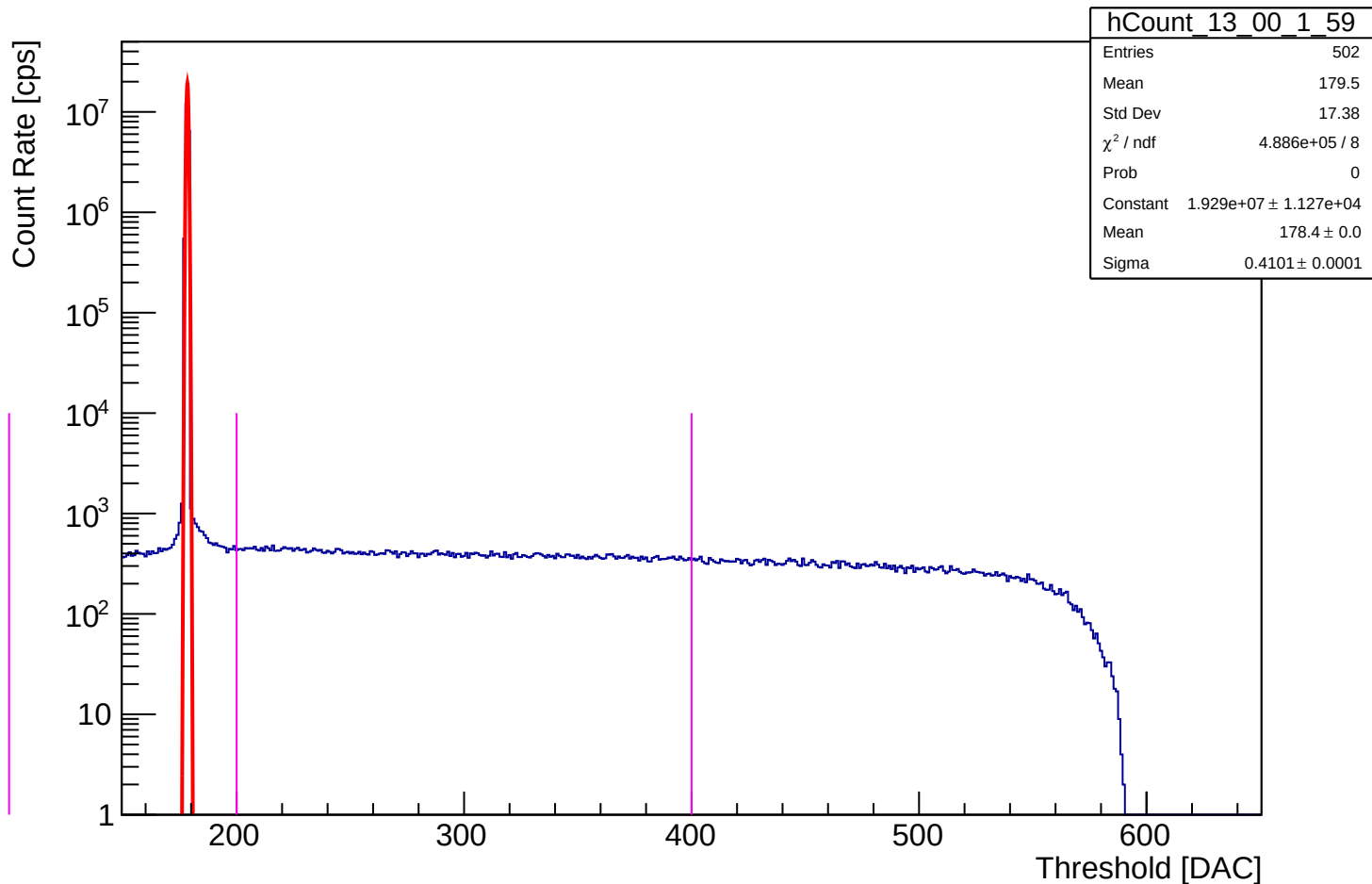
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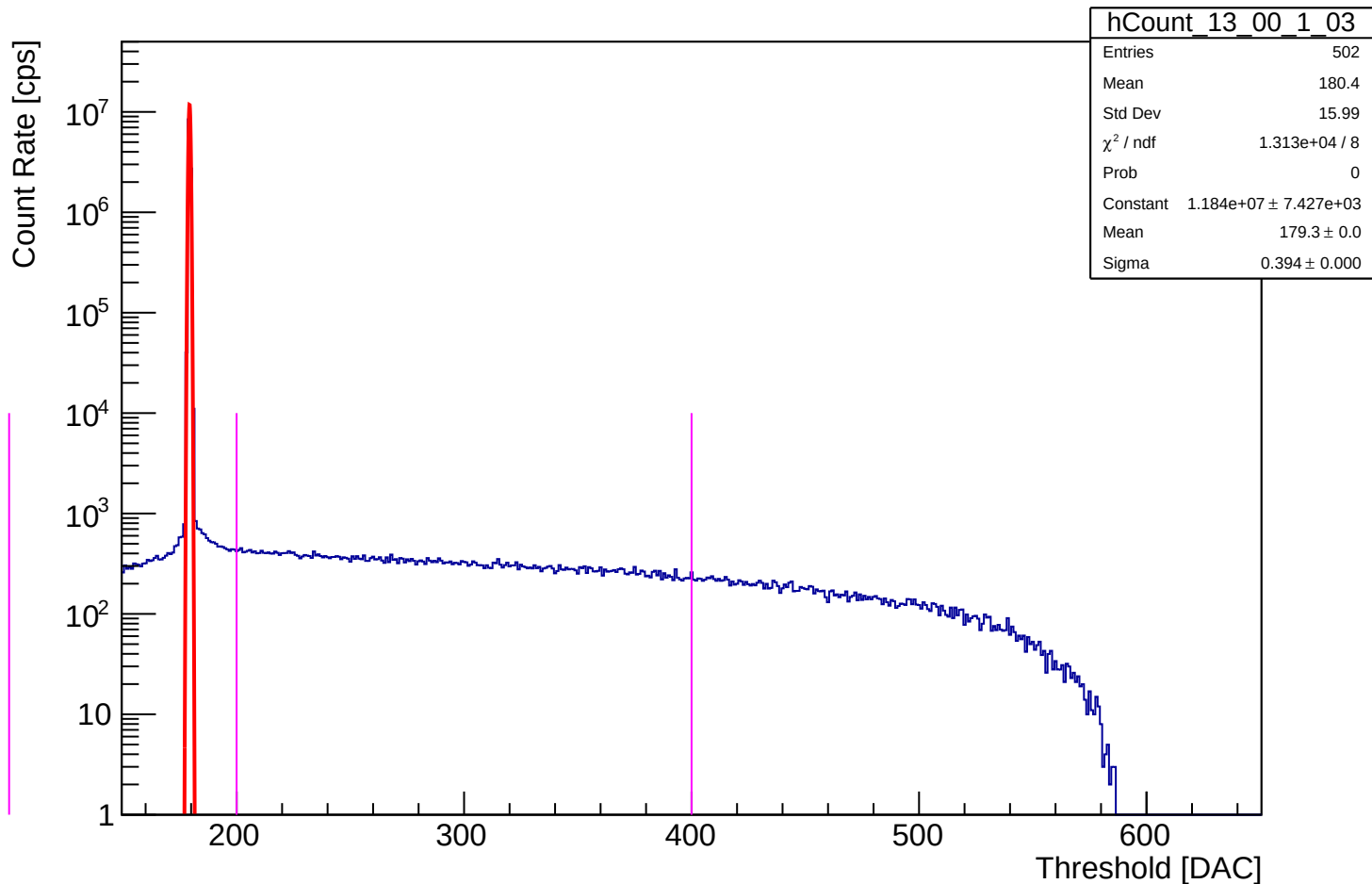
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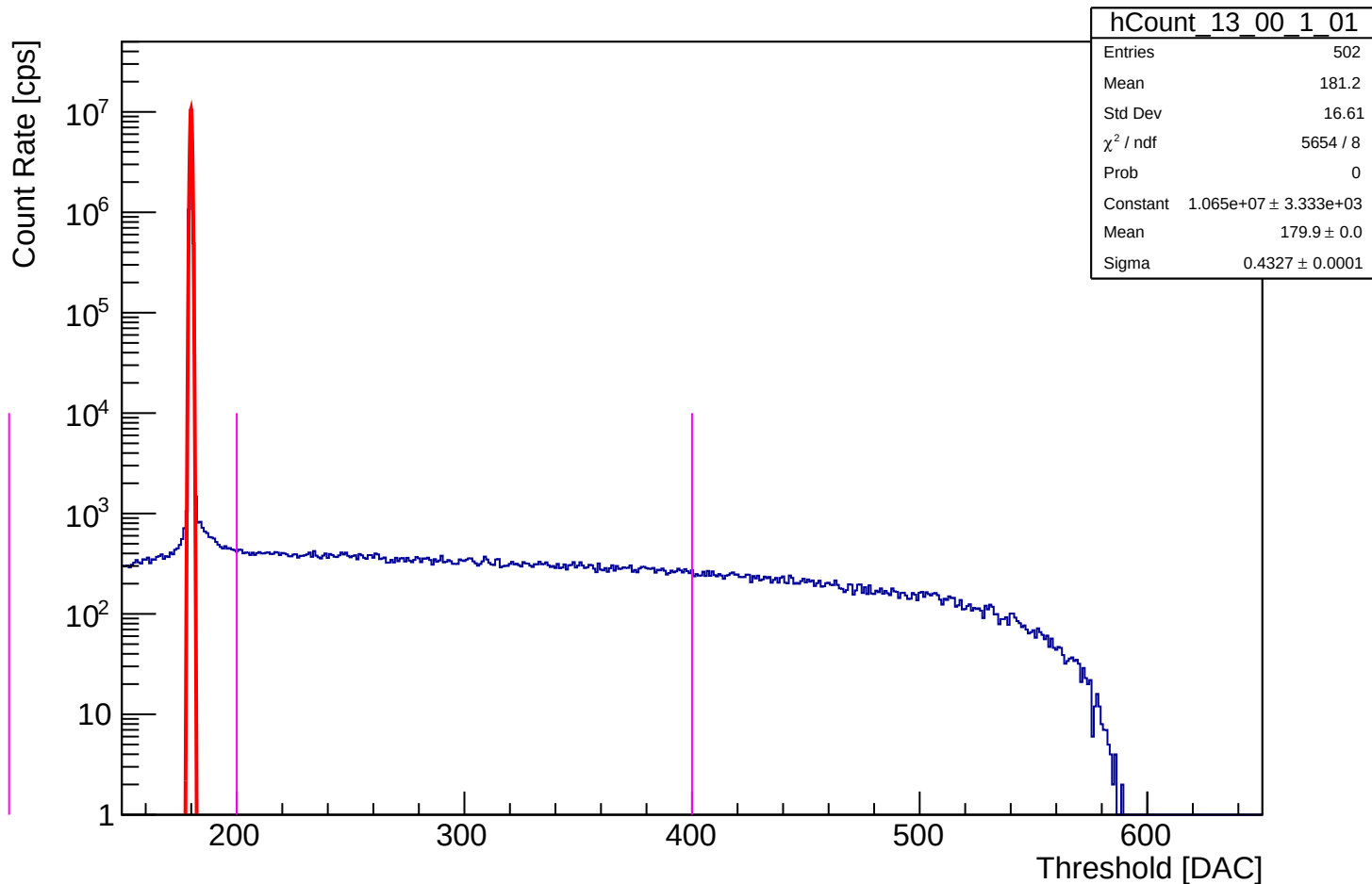
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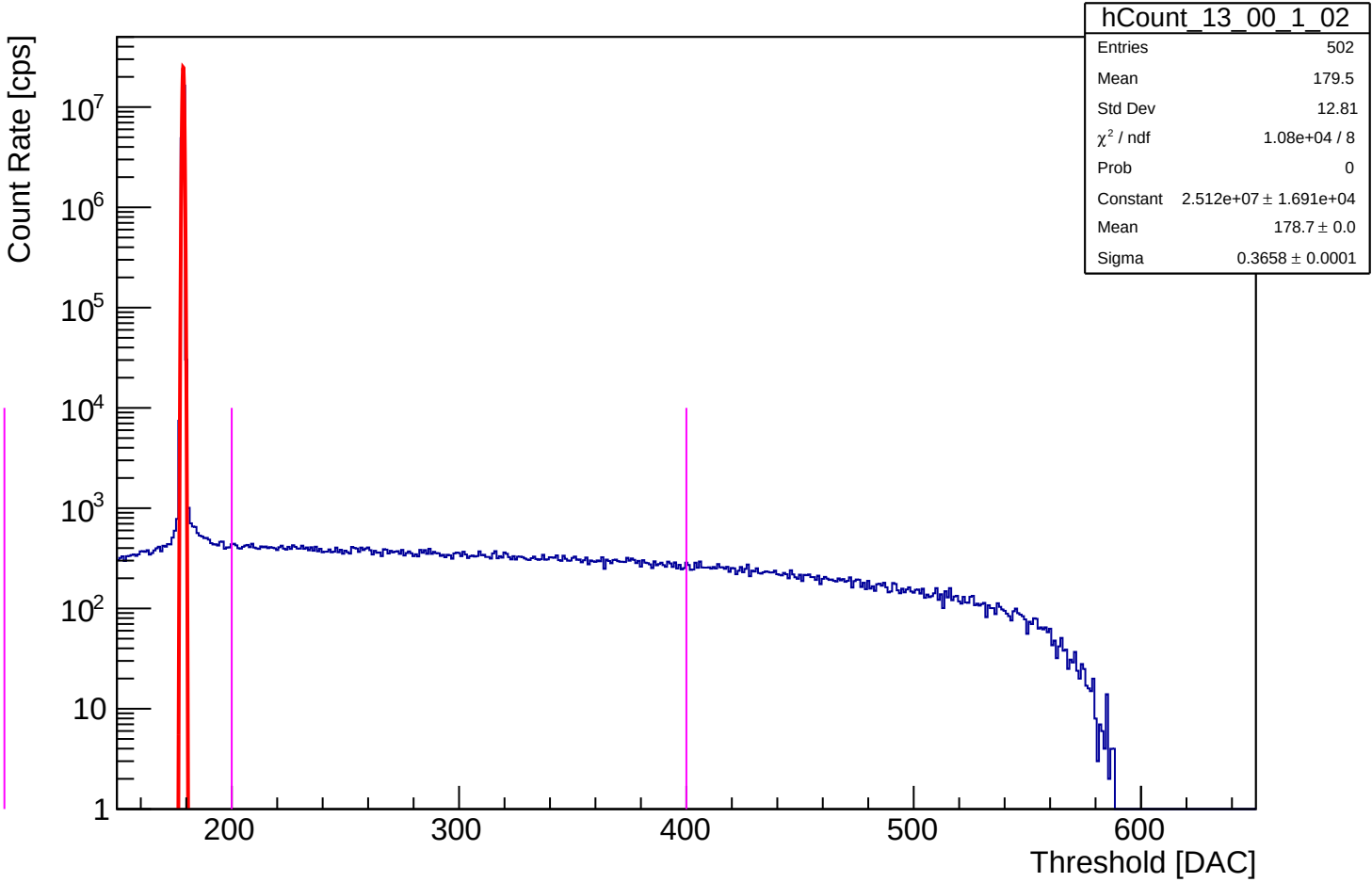


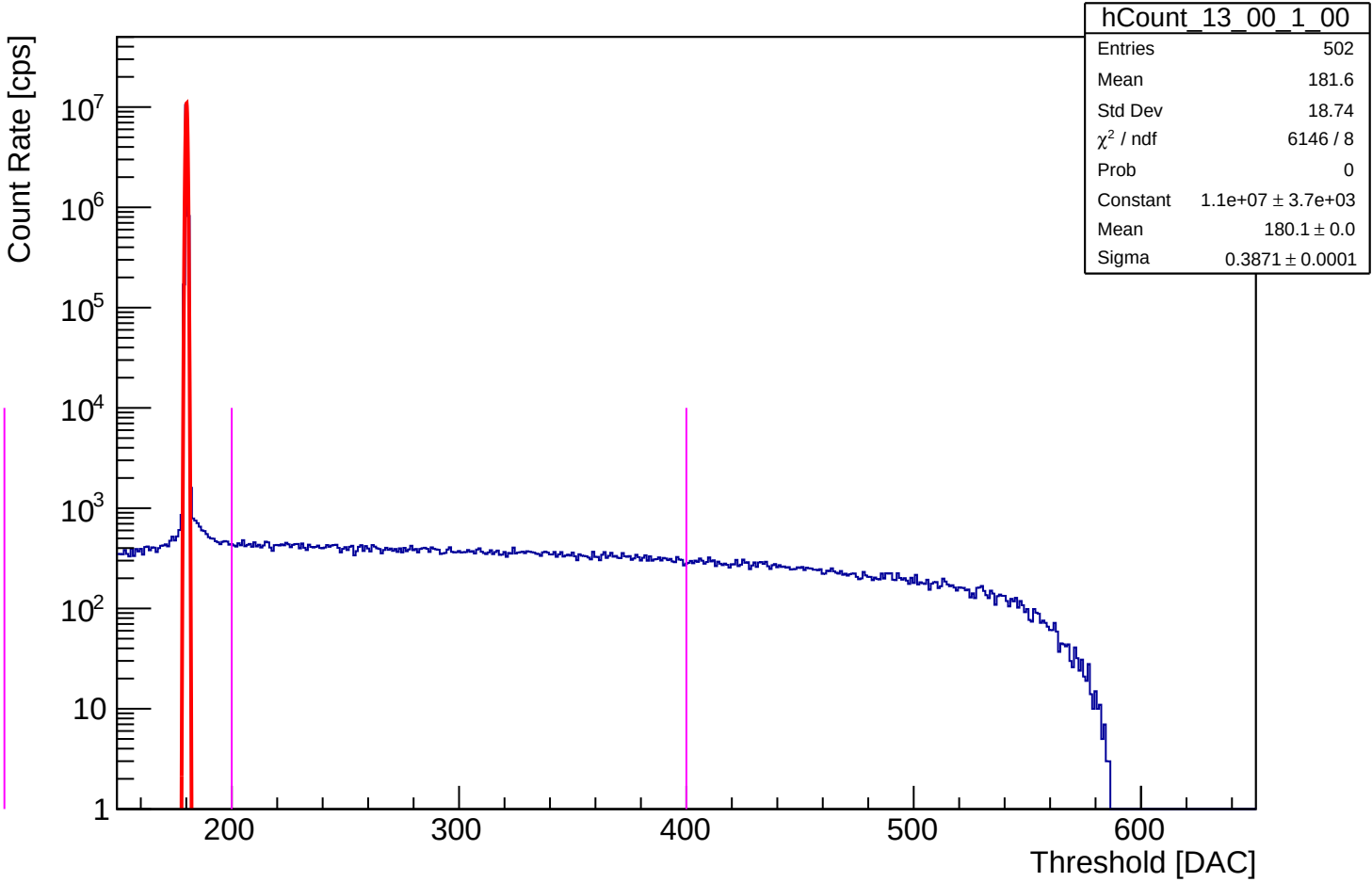
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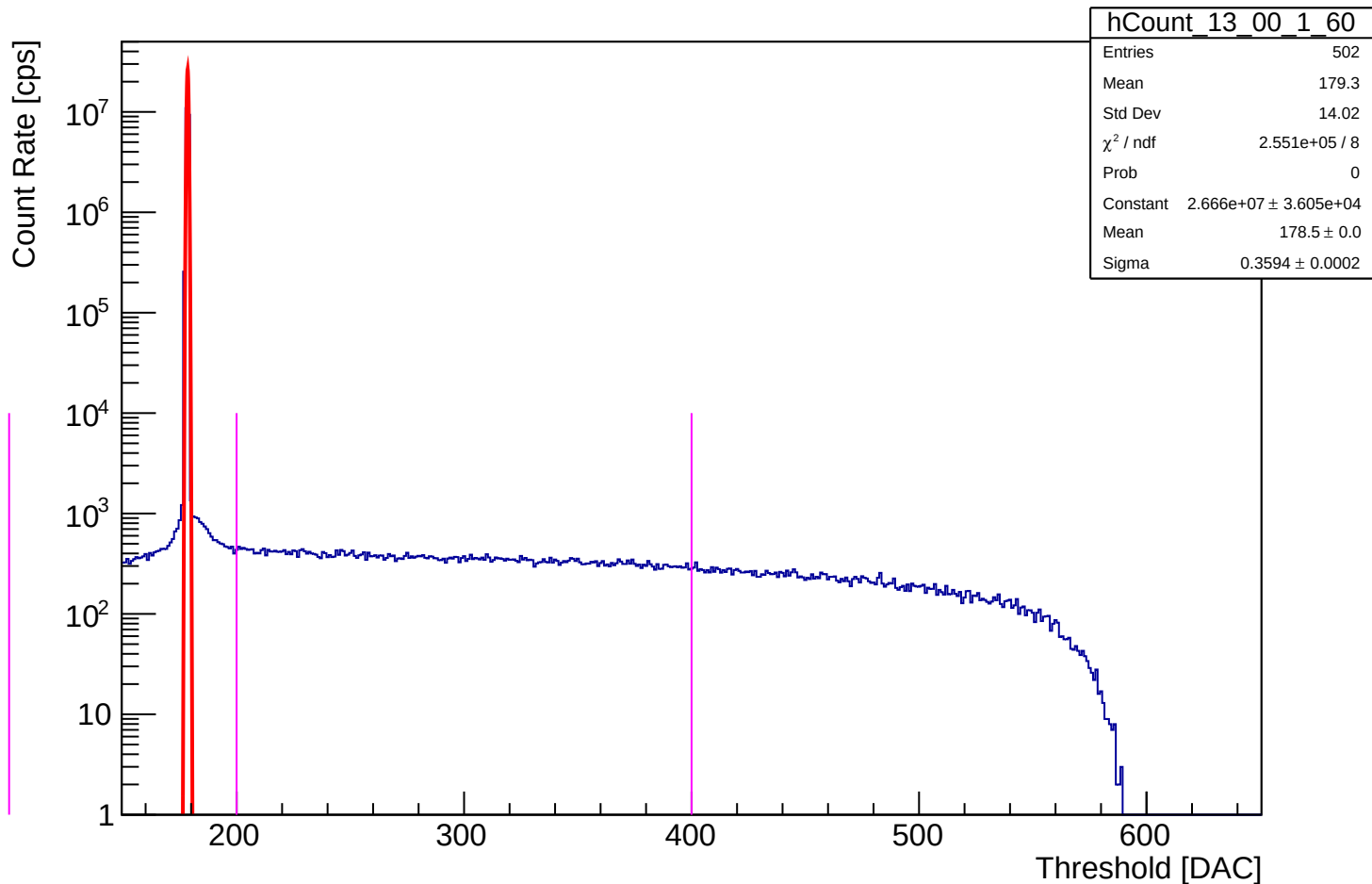
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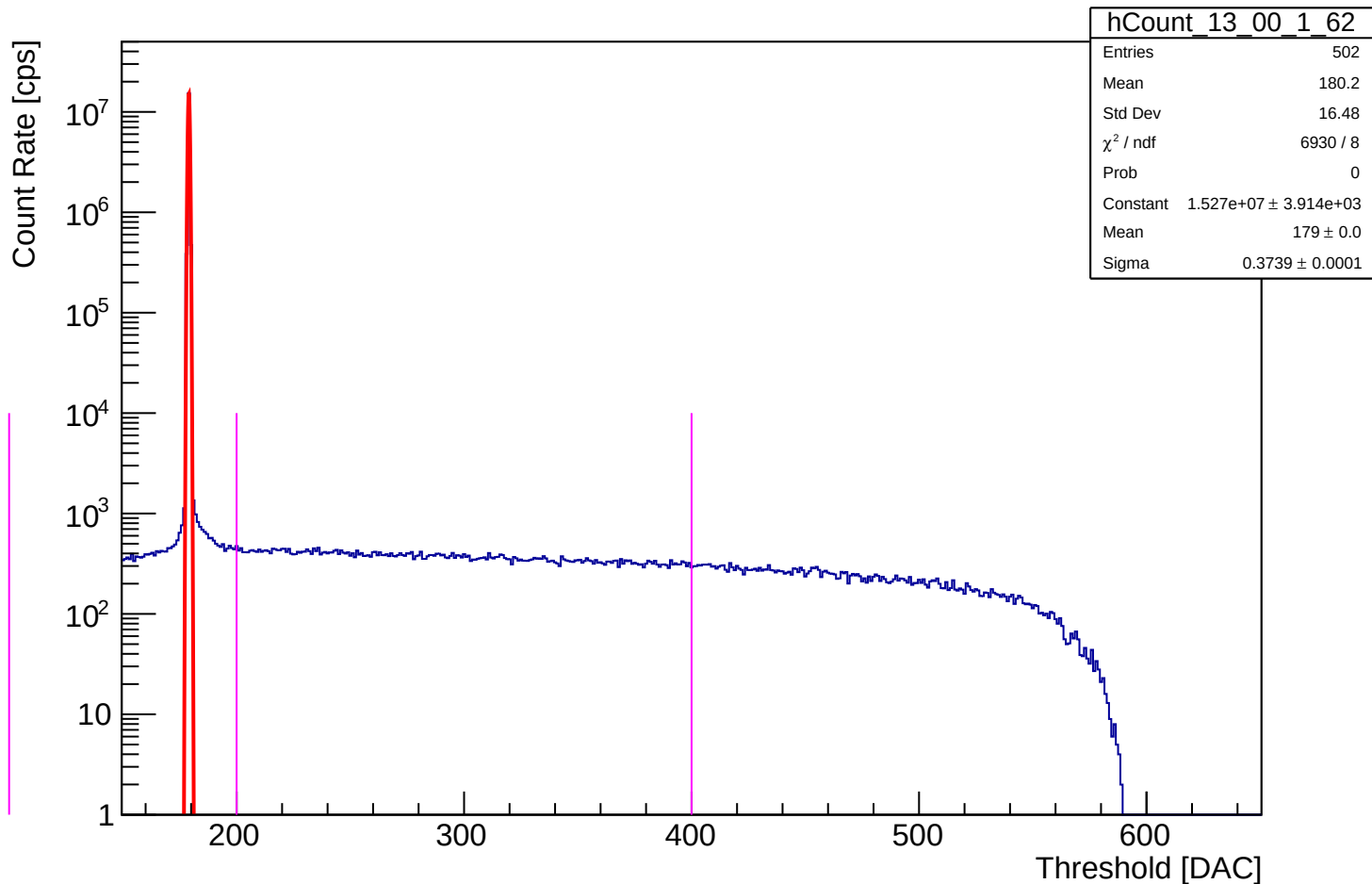


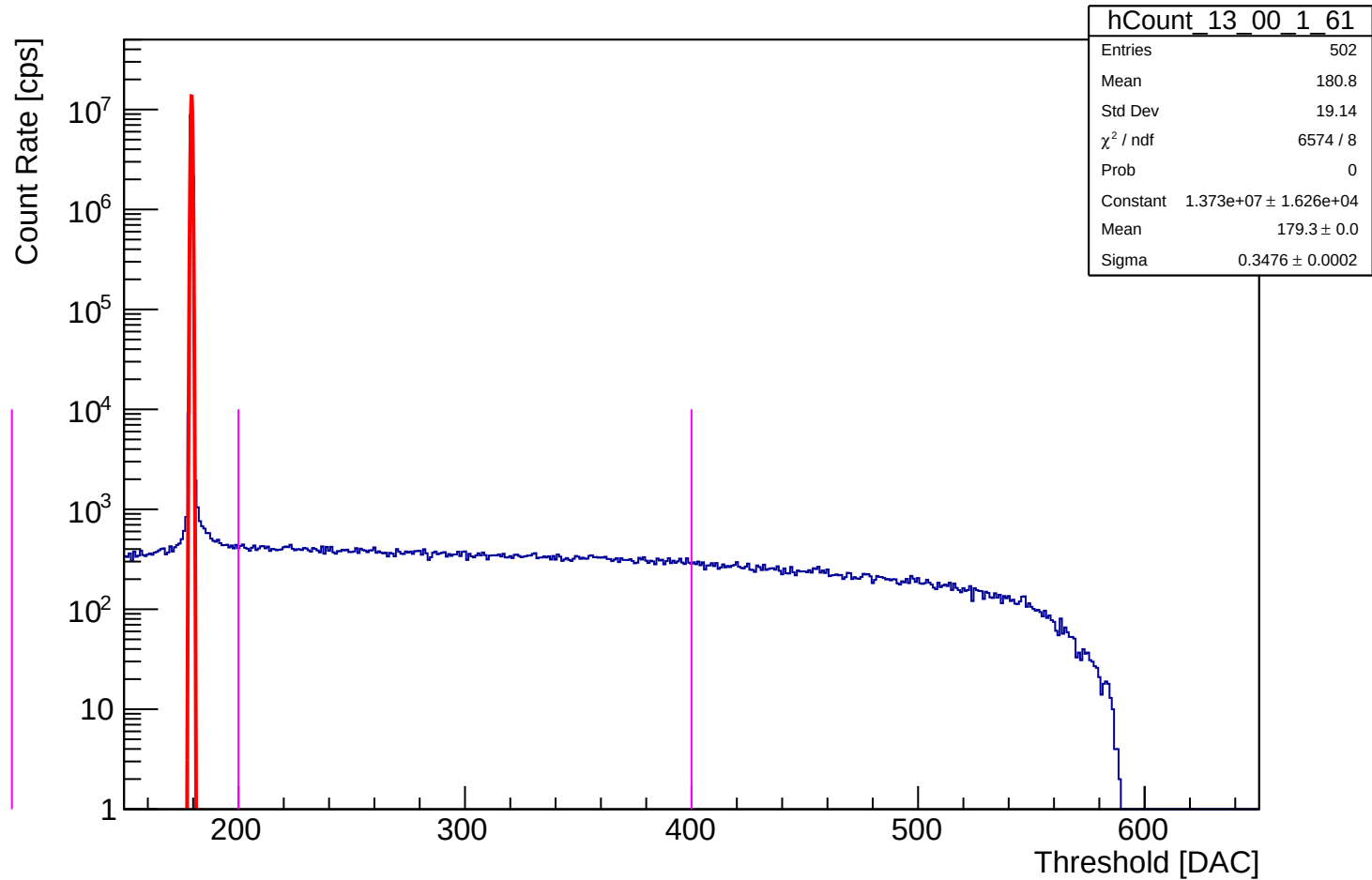


Row 1 Tile 1 Pmt 2 Pixel 61 Slot 13 Fiber 0 Asic 1 Channel 60

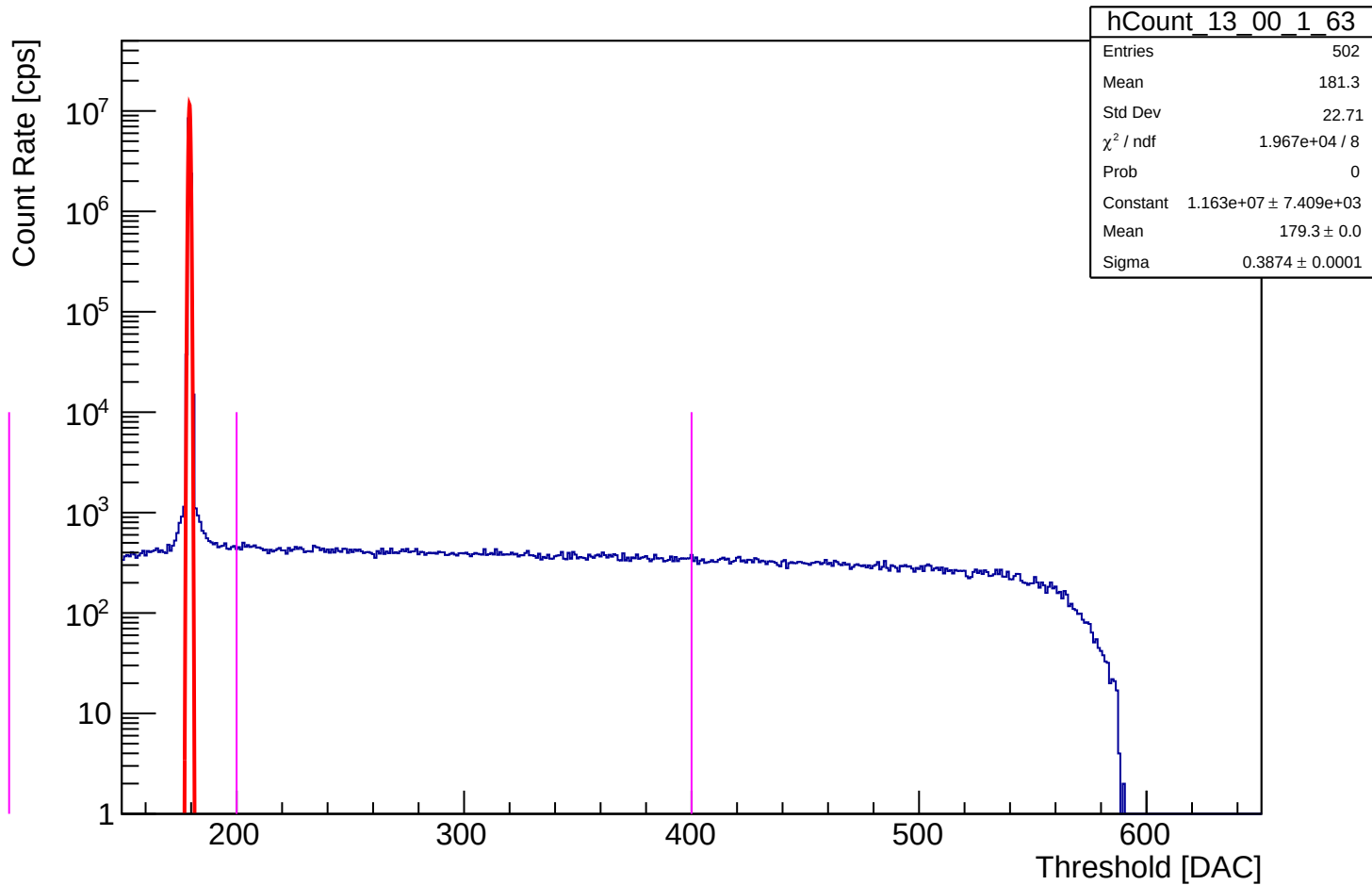


Row 1 Tile 1 Pmt 2 Pixel 62 Slot 13 Fiber 0 Asic 1 Channel 62

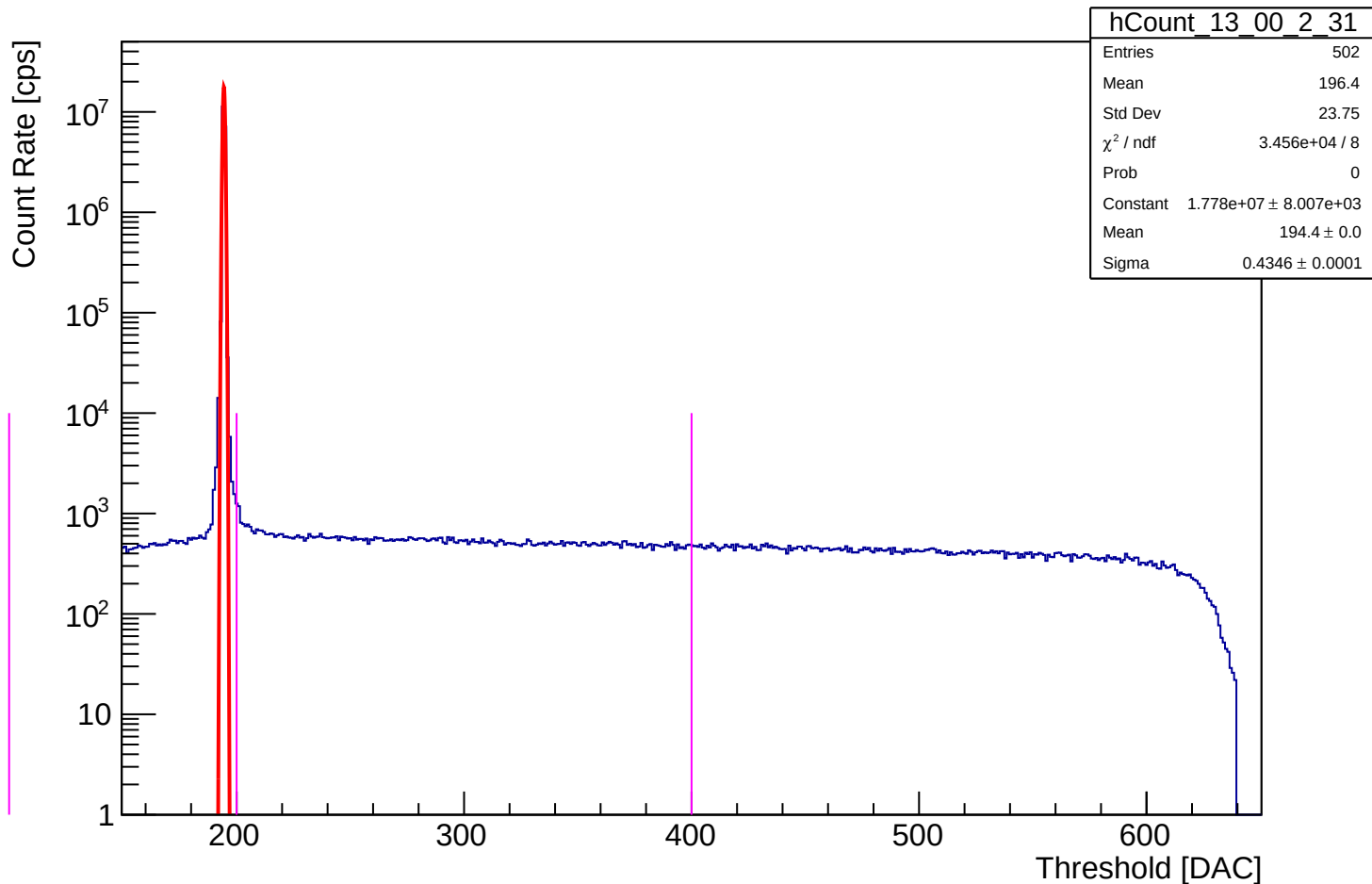




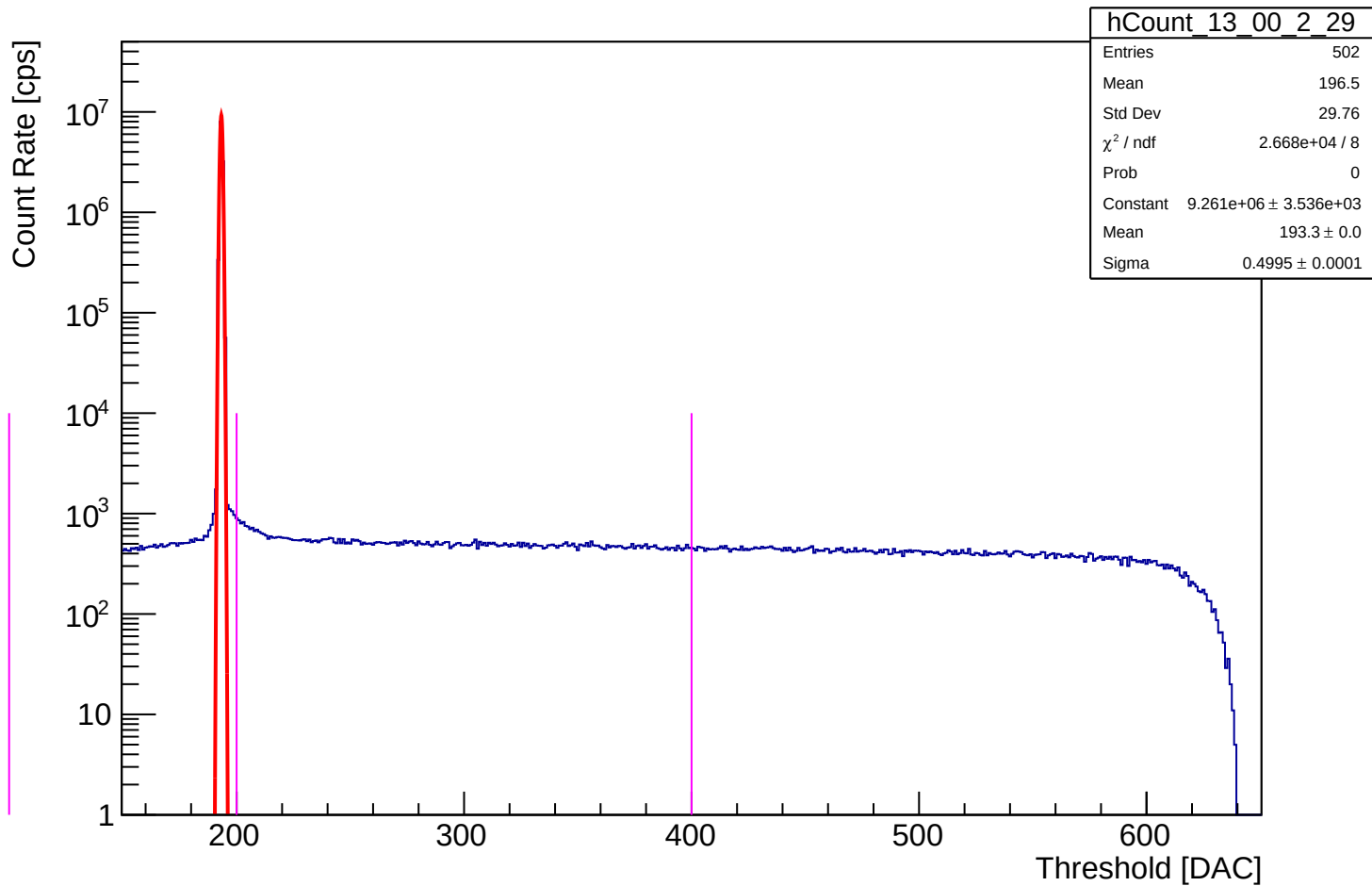
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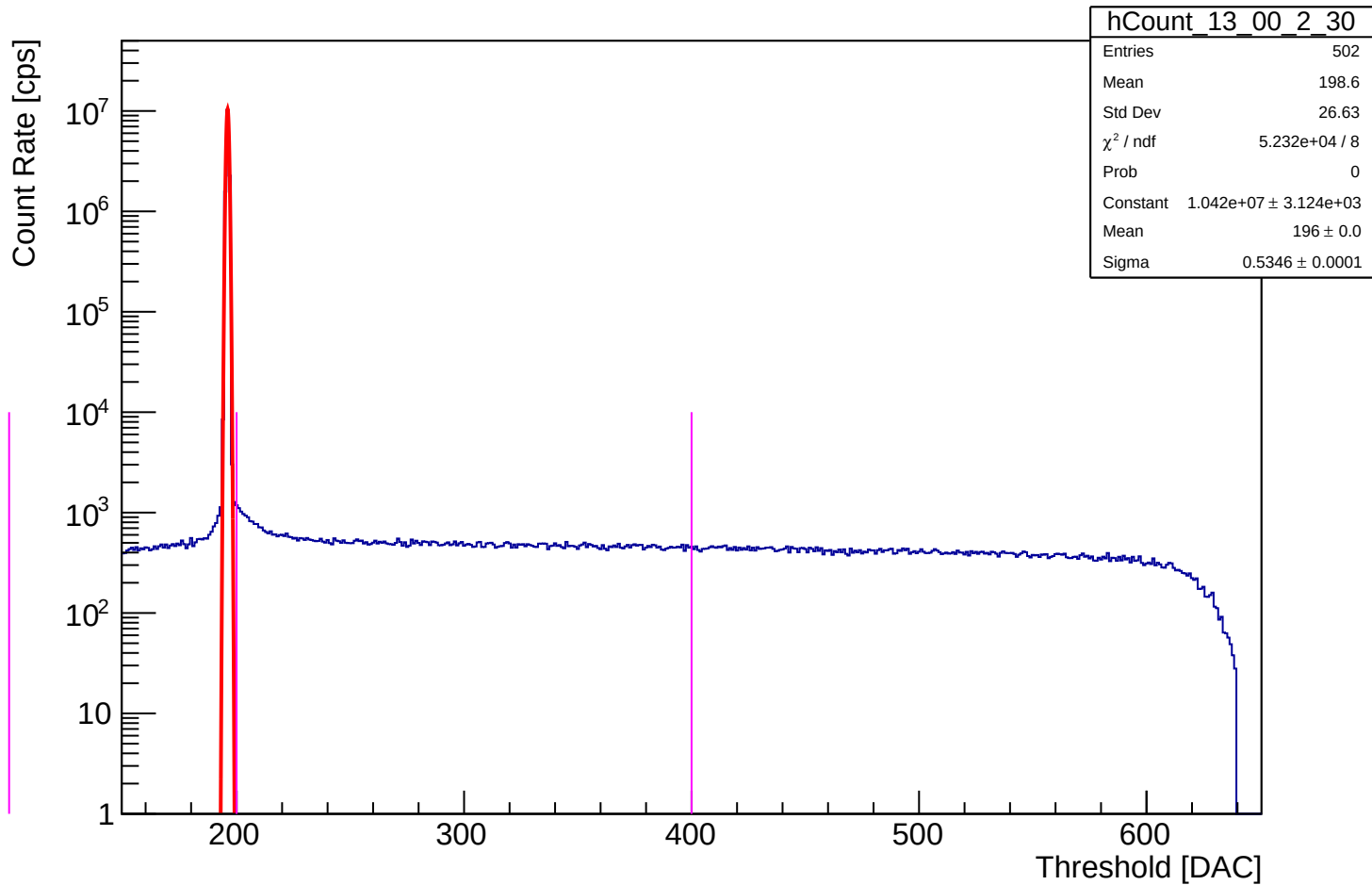
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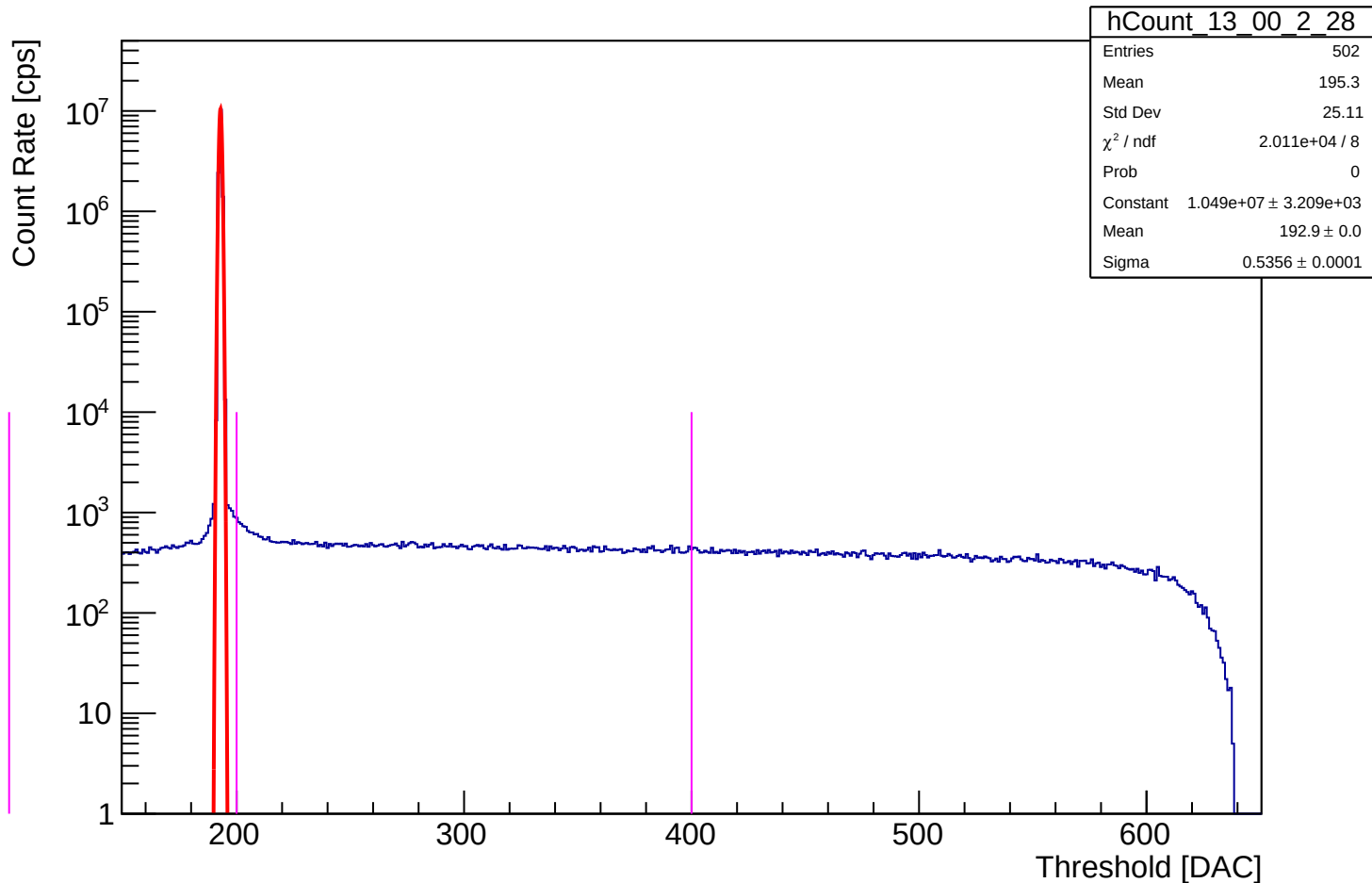
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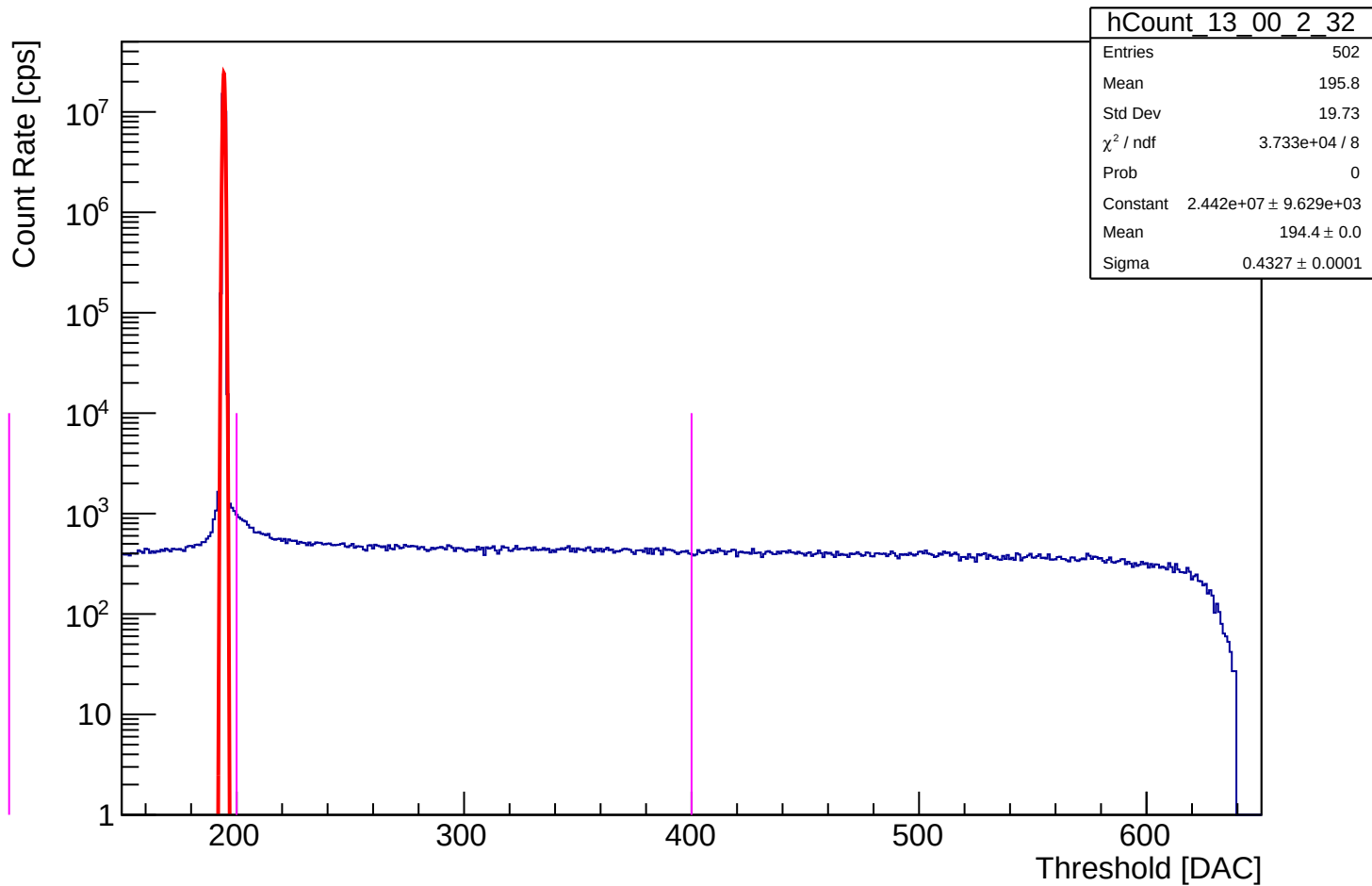
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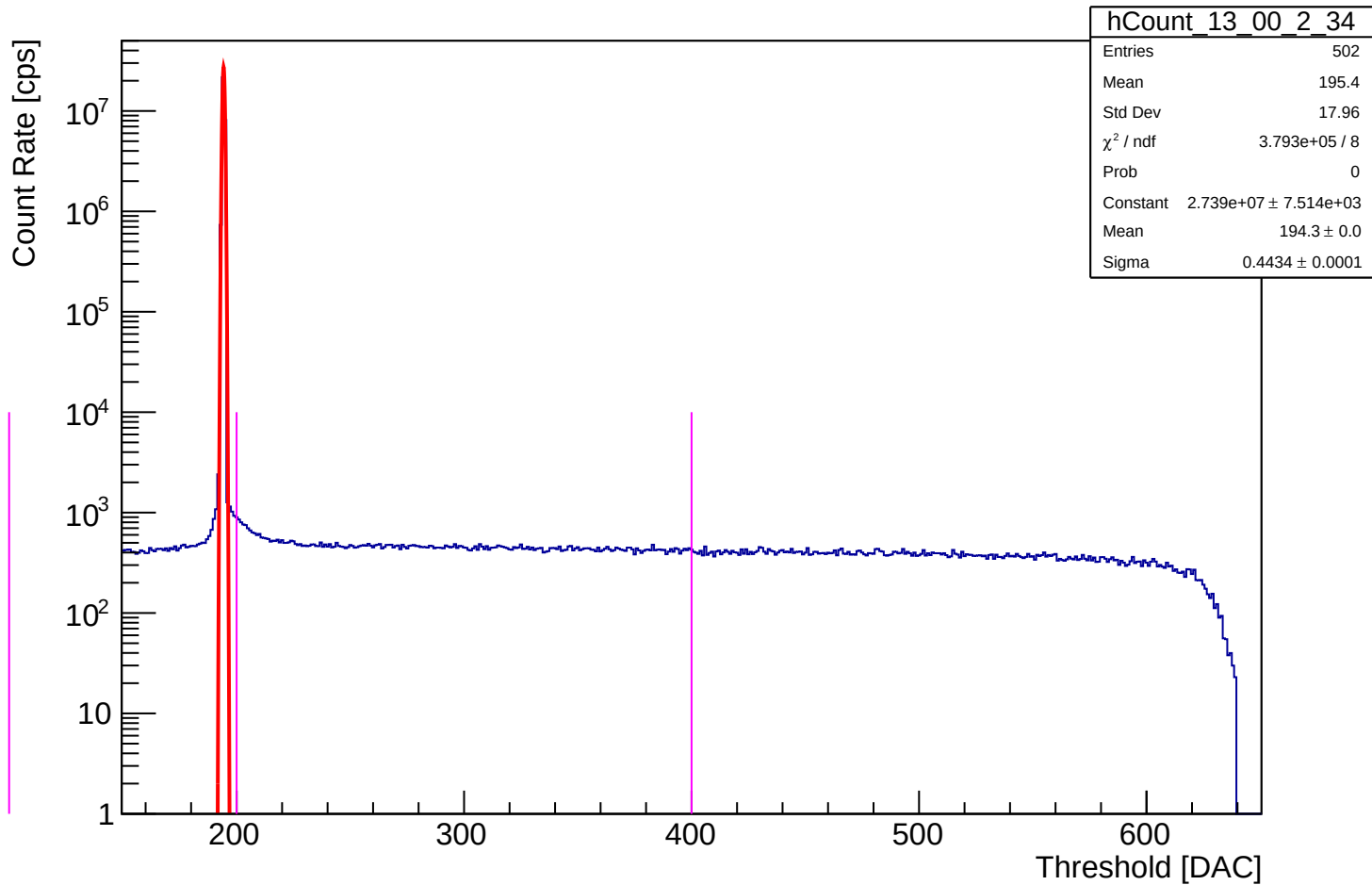
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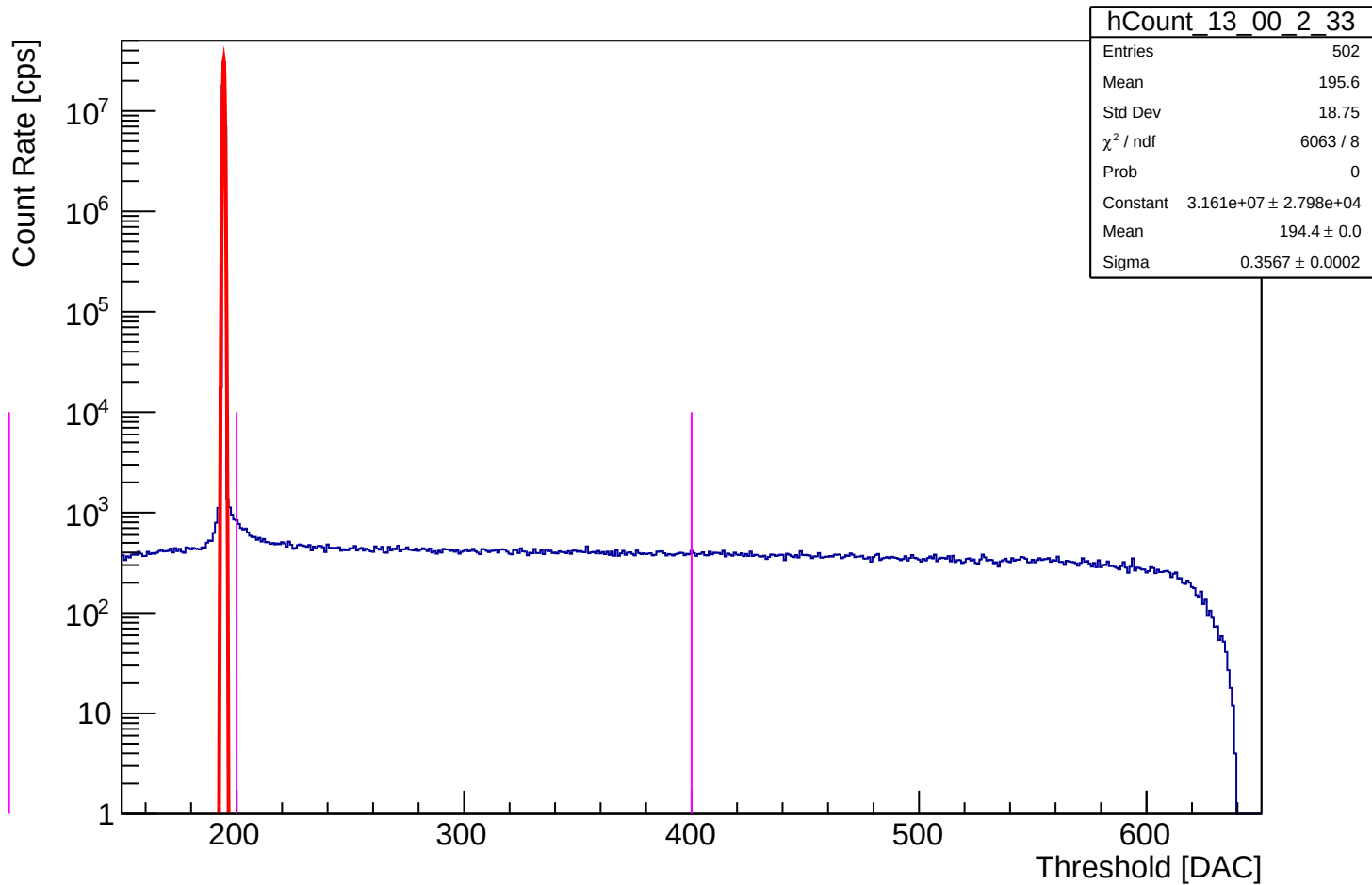
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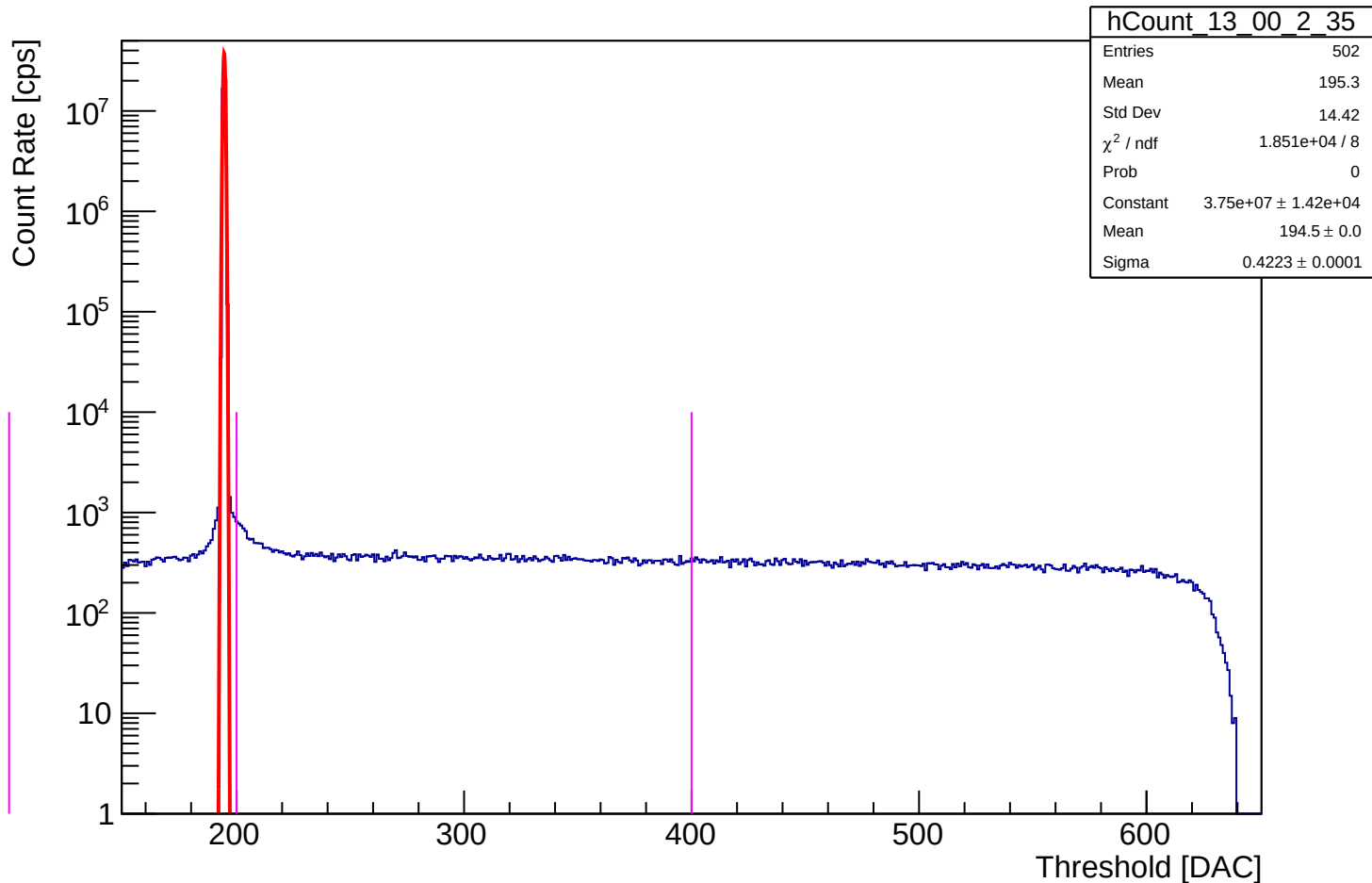
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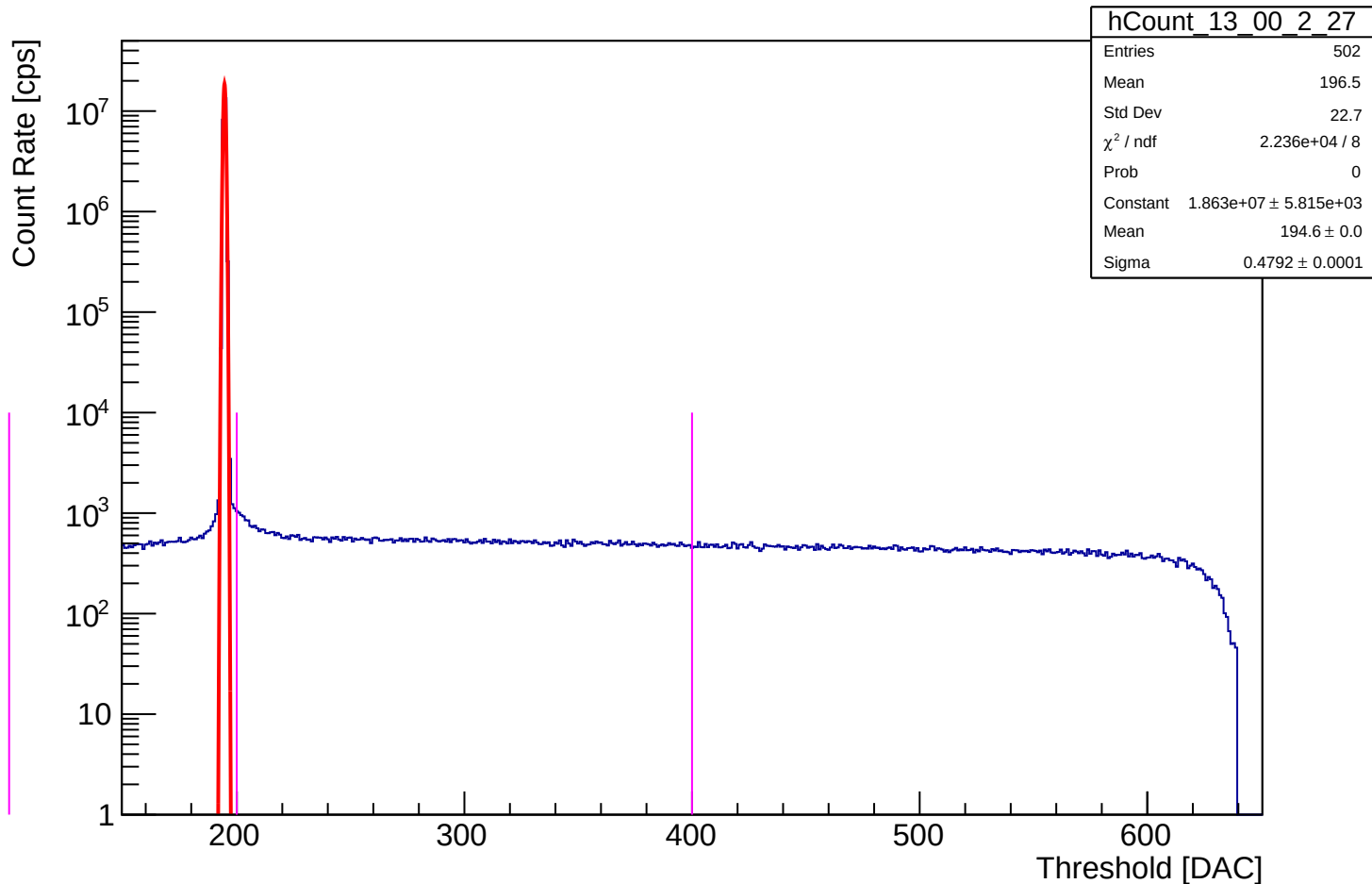
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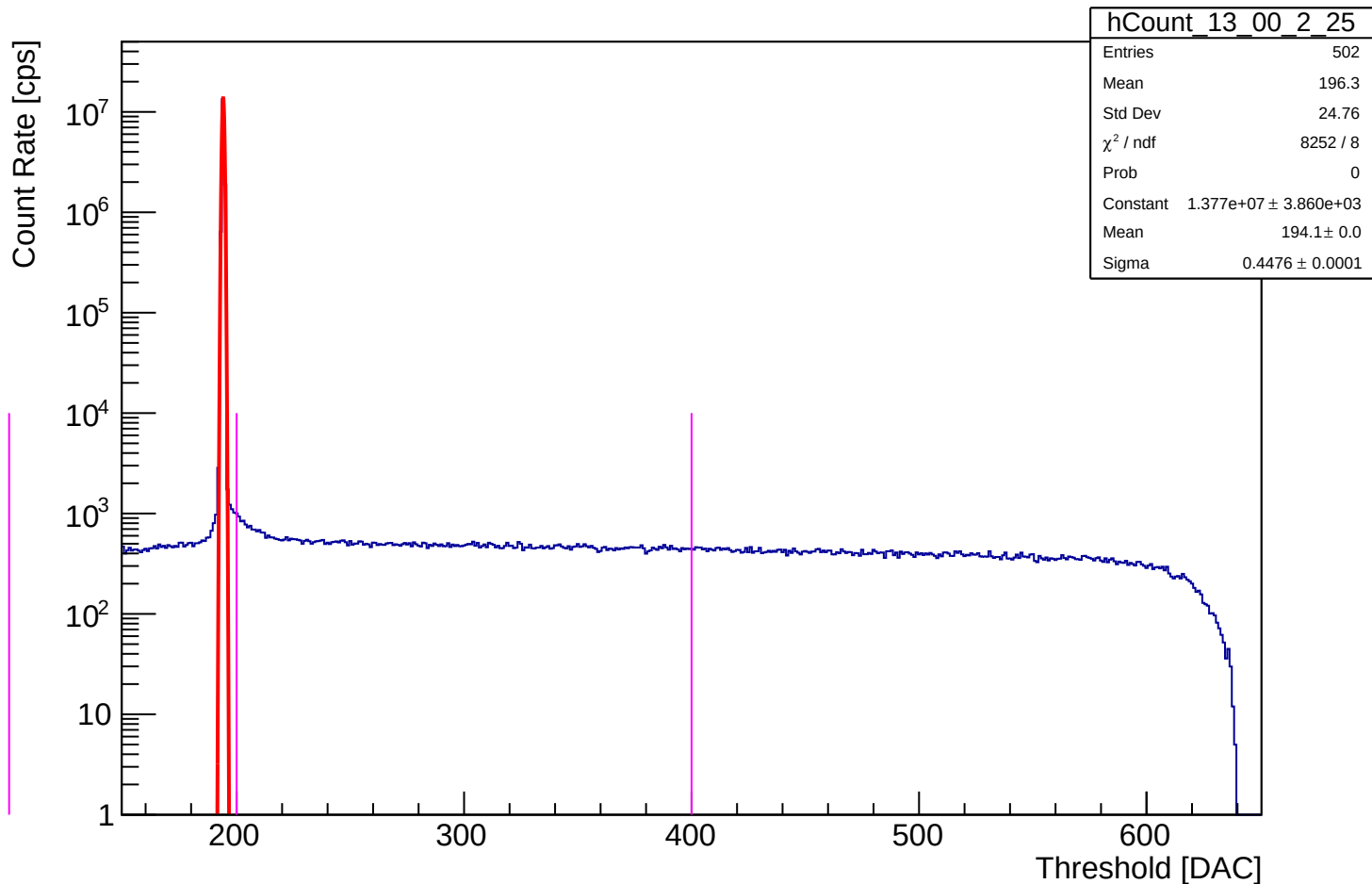
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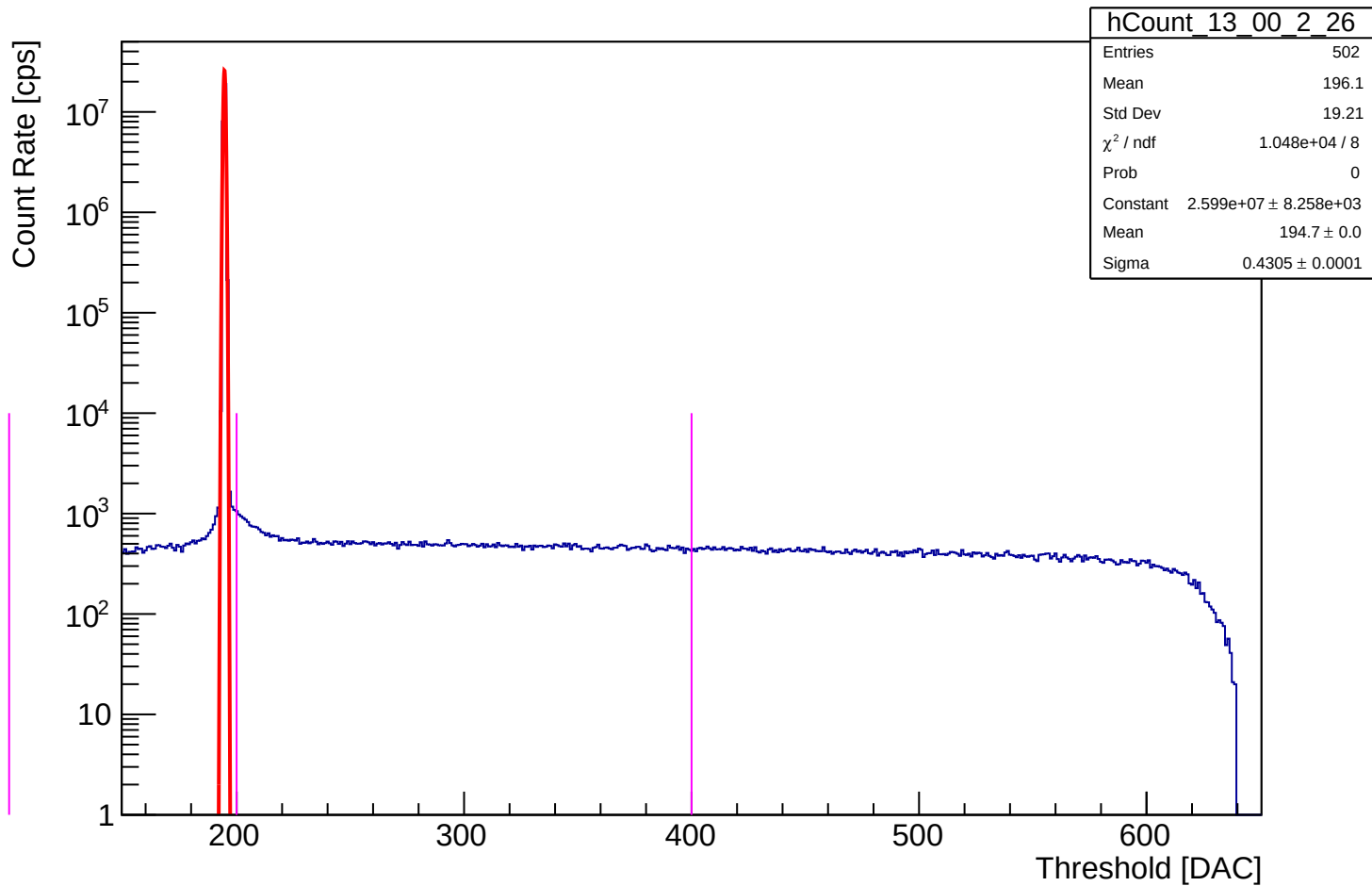
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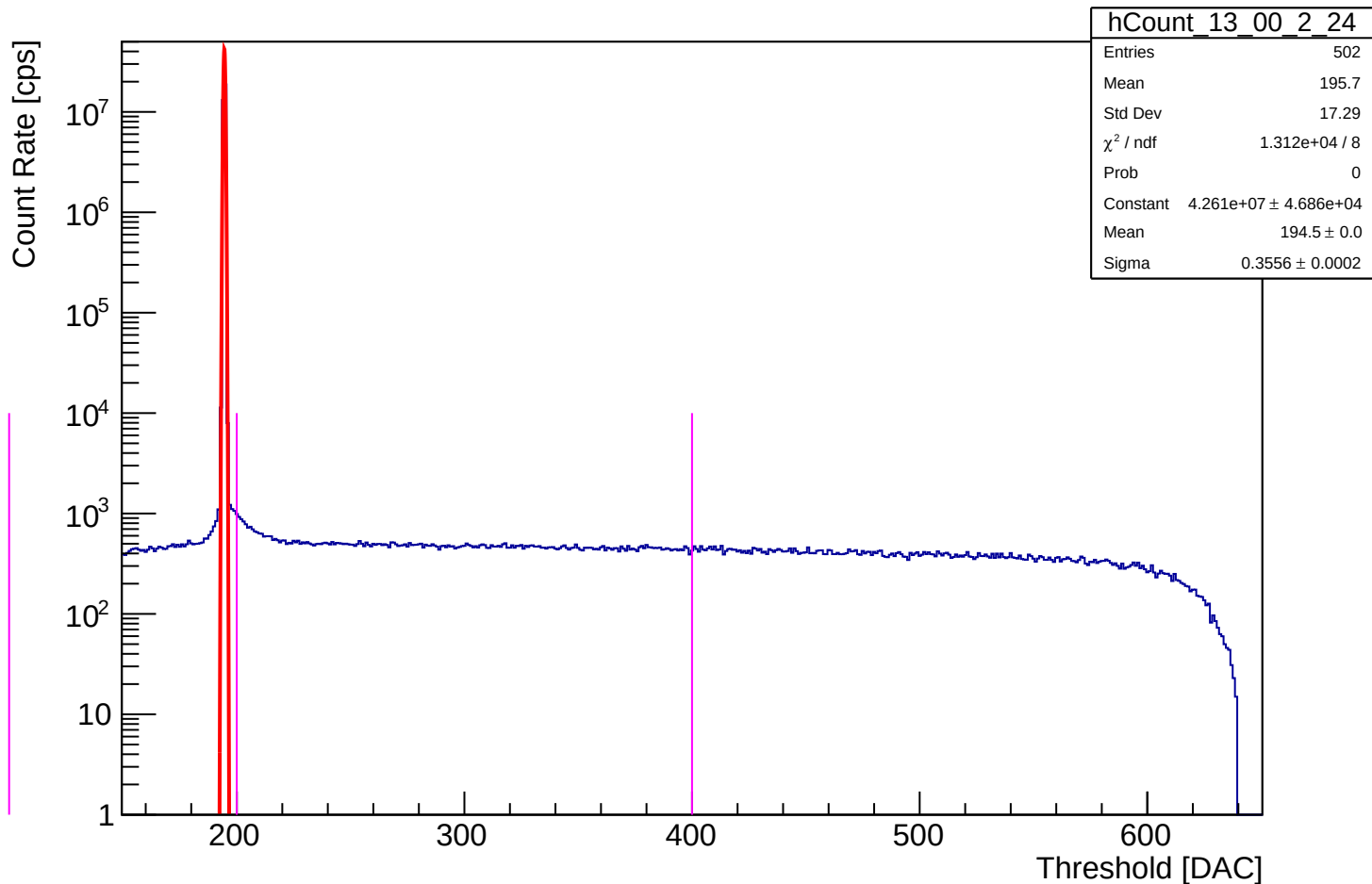
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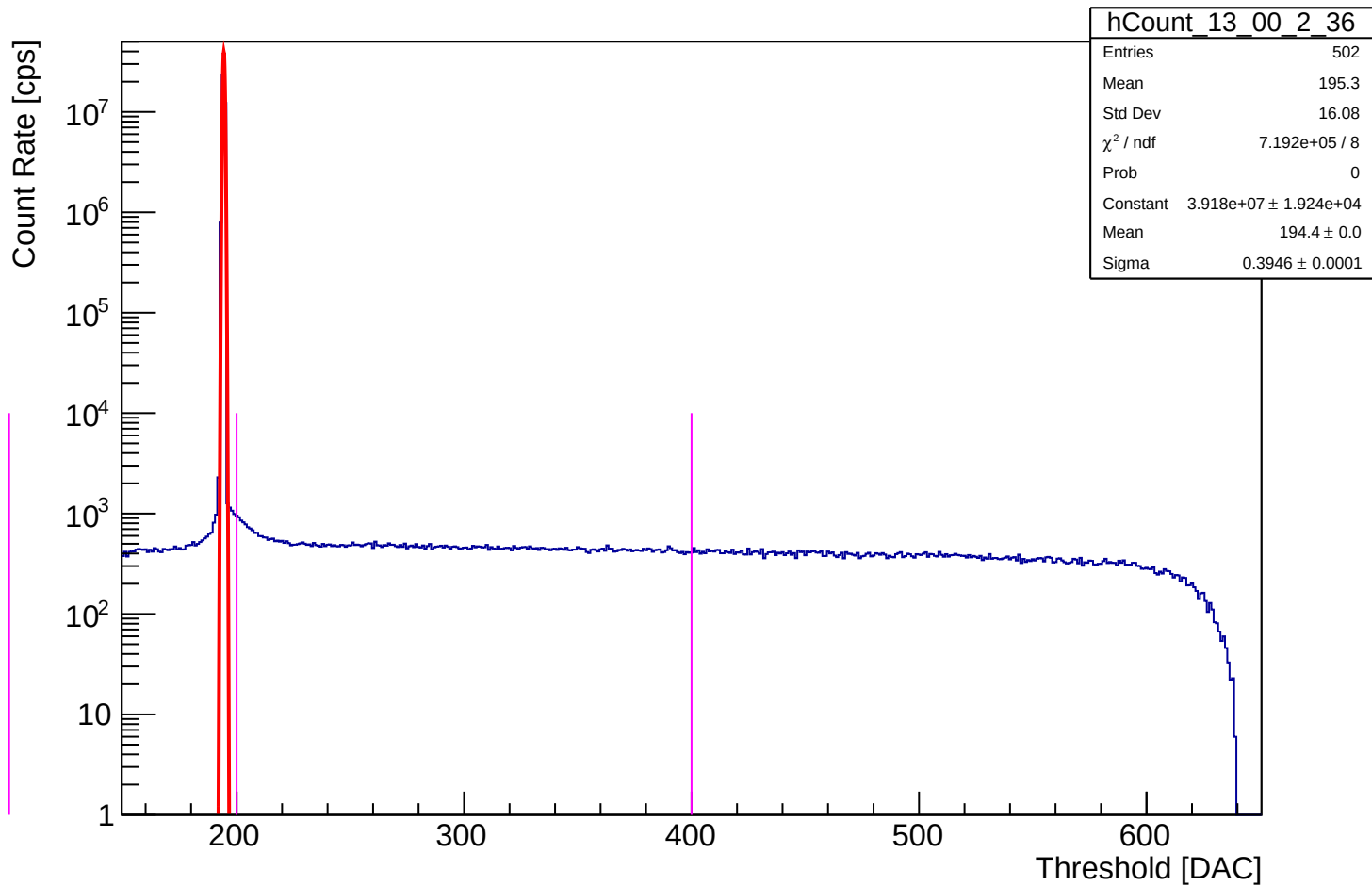
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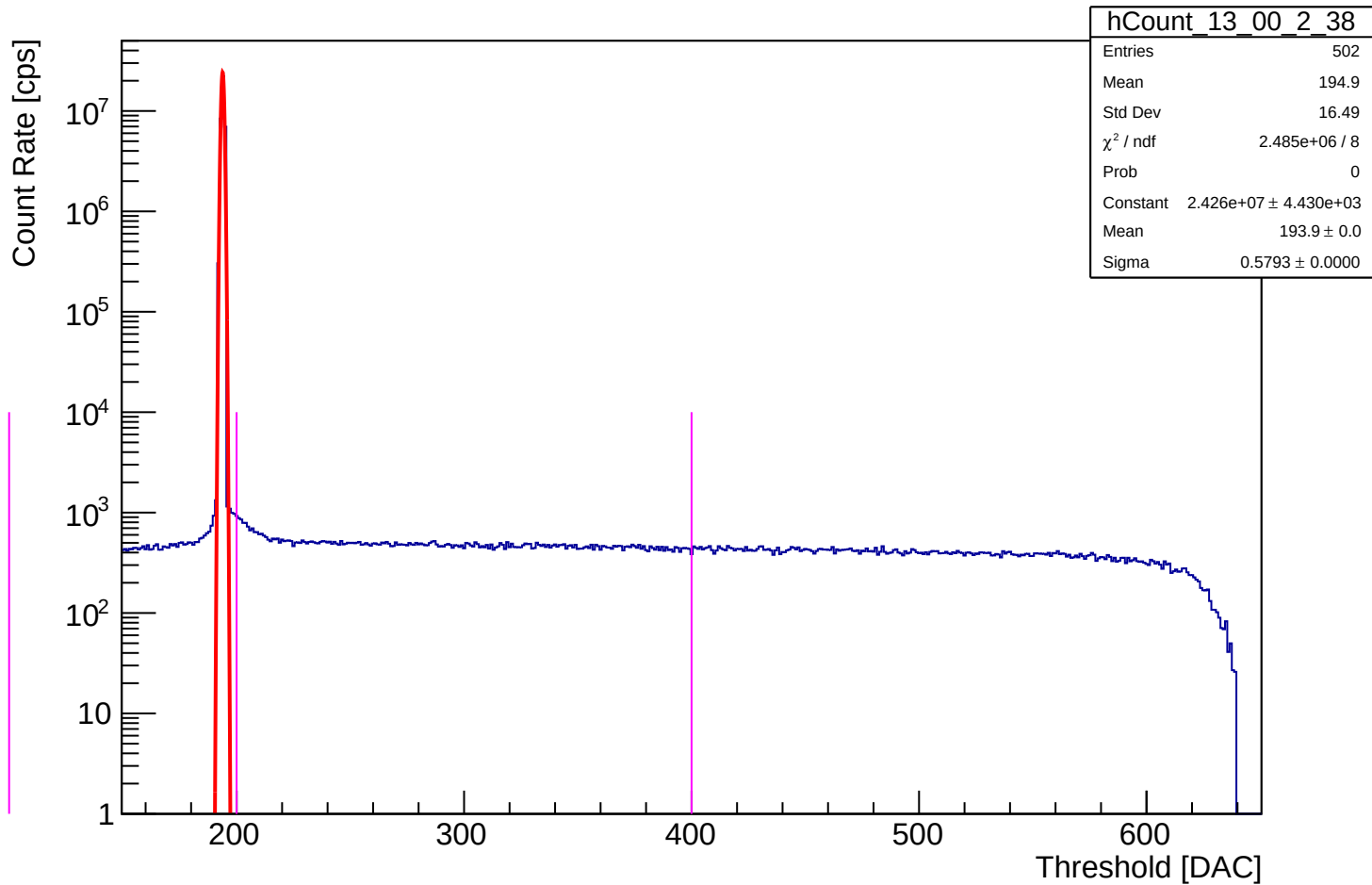
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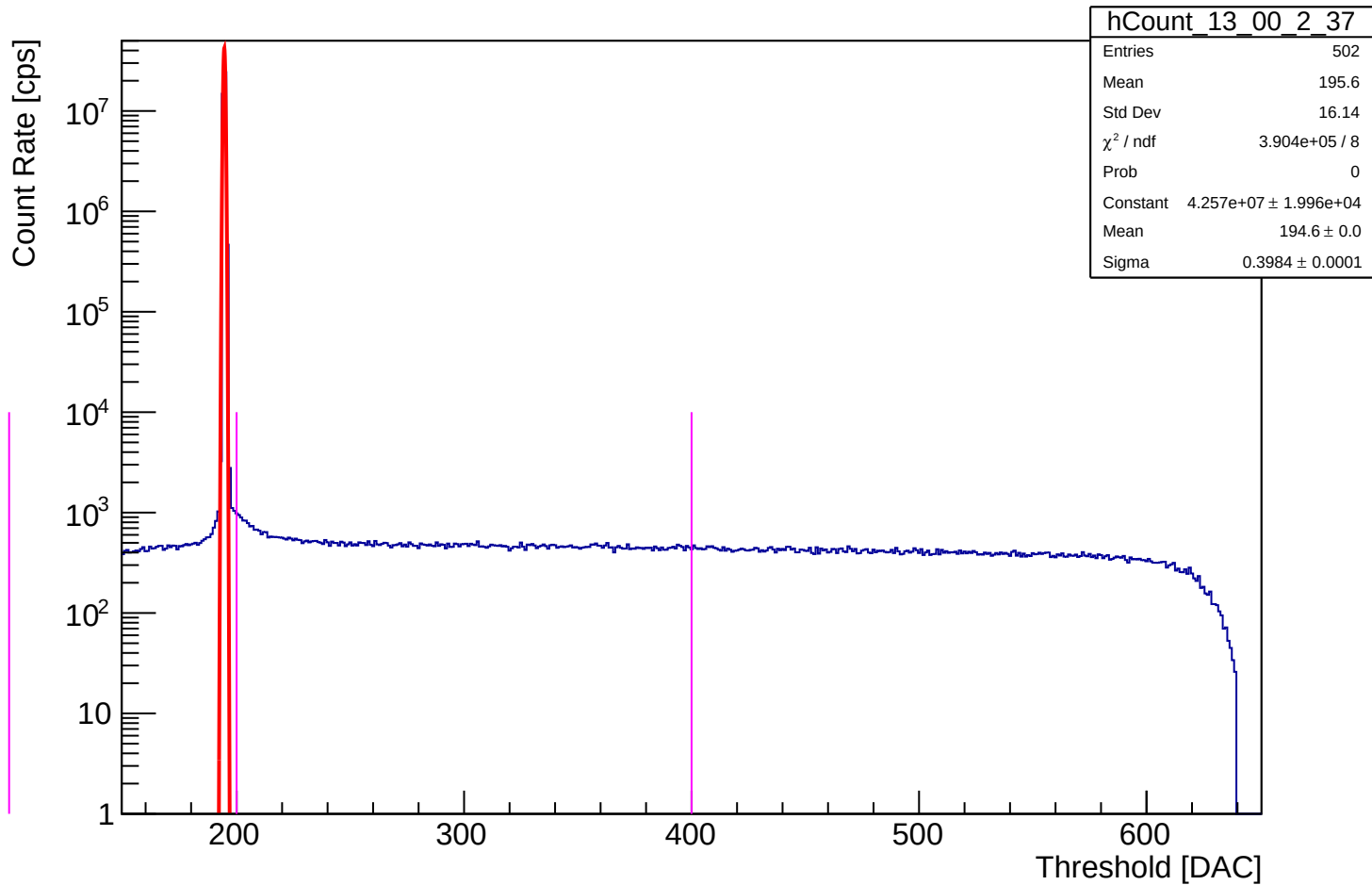
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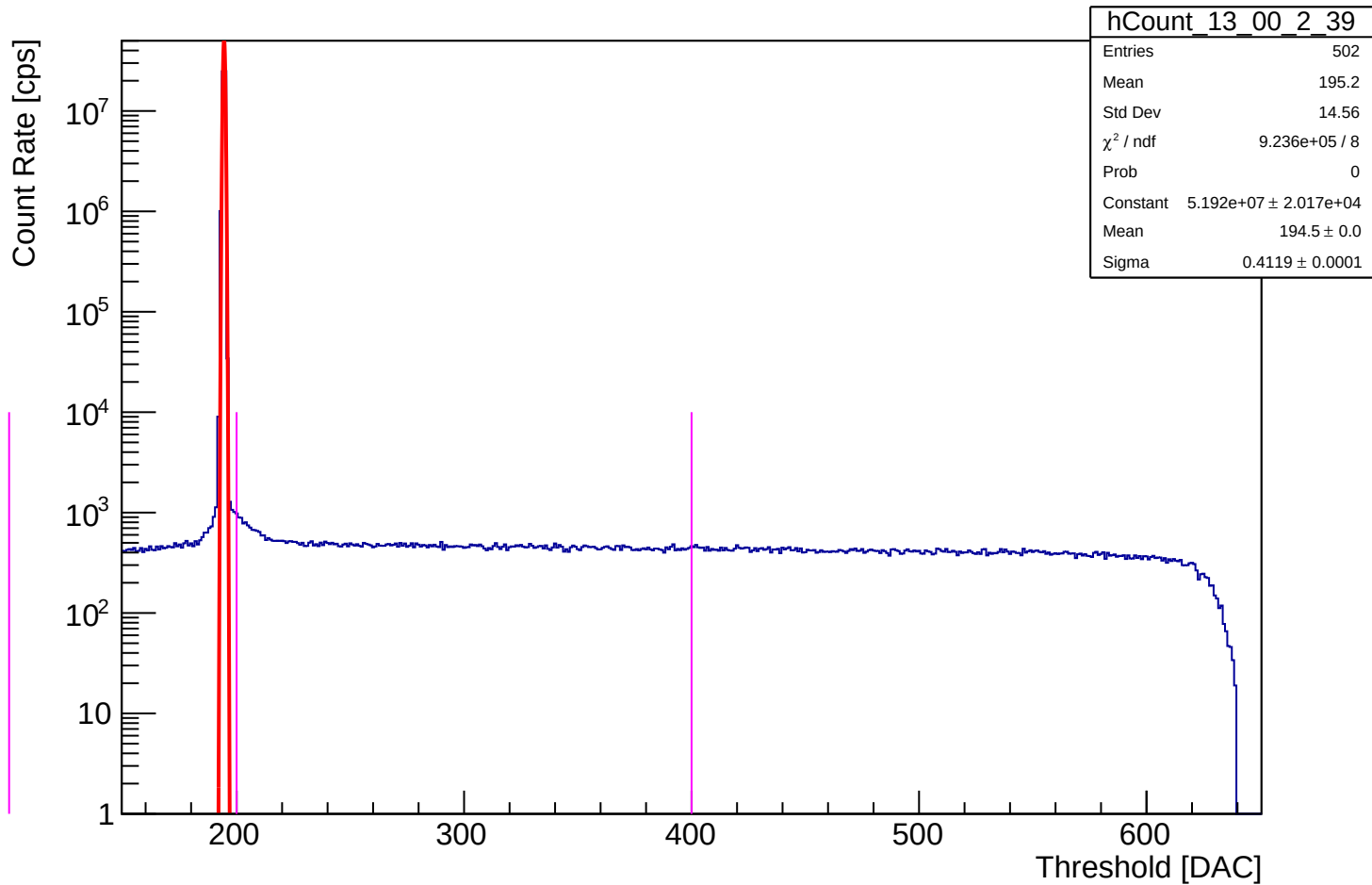
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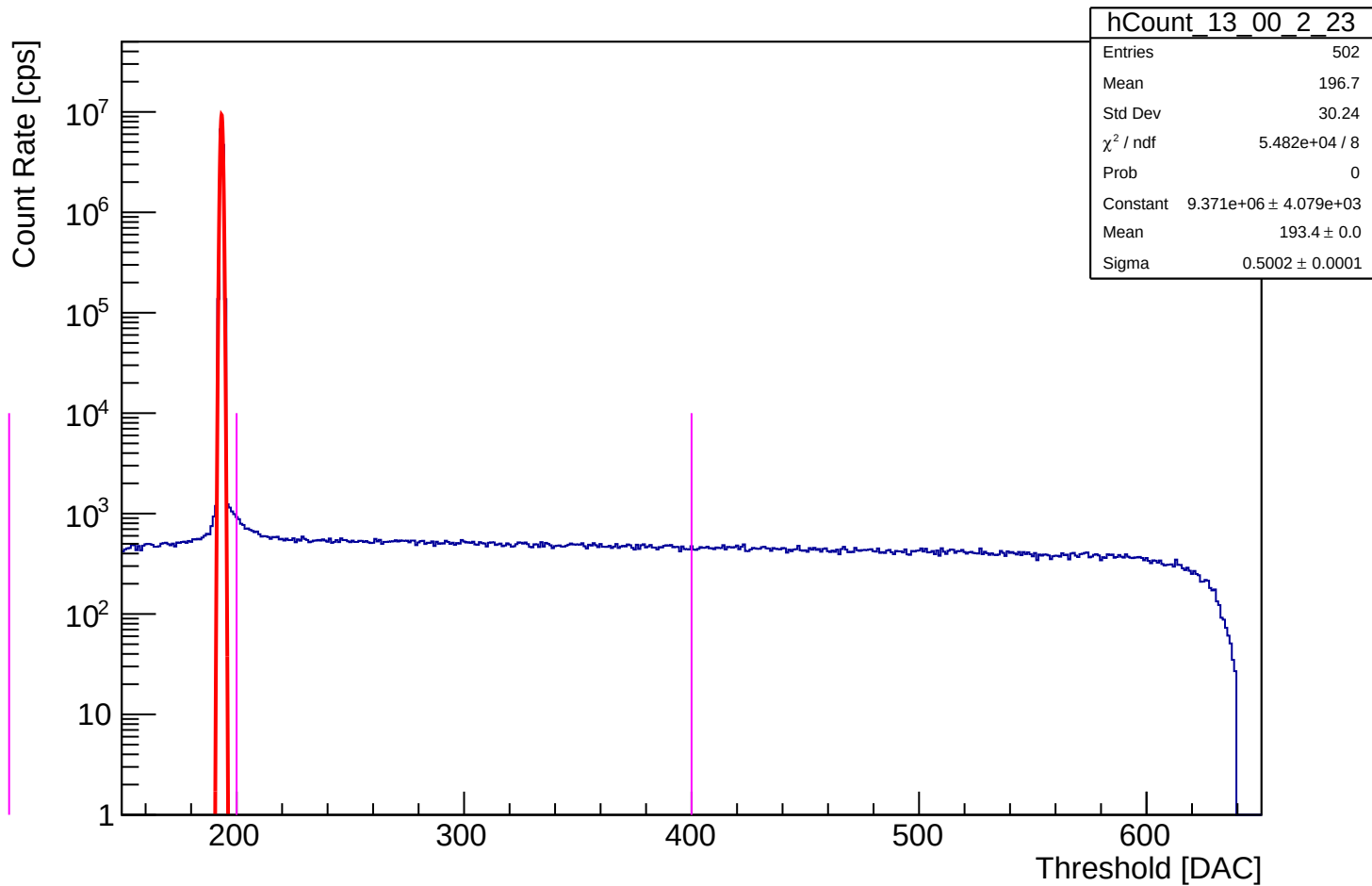
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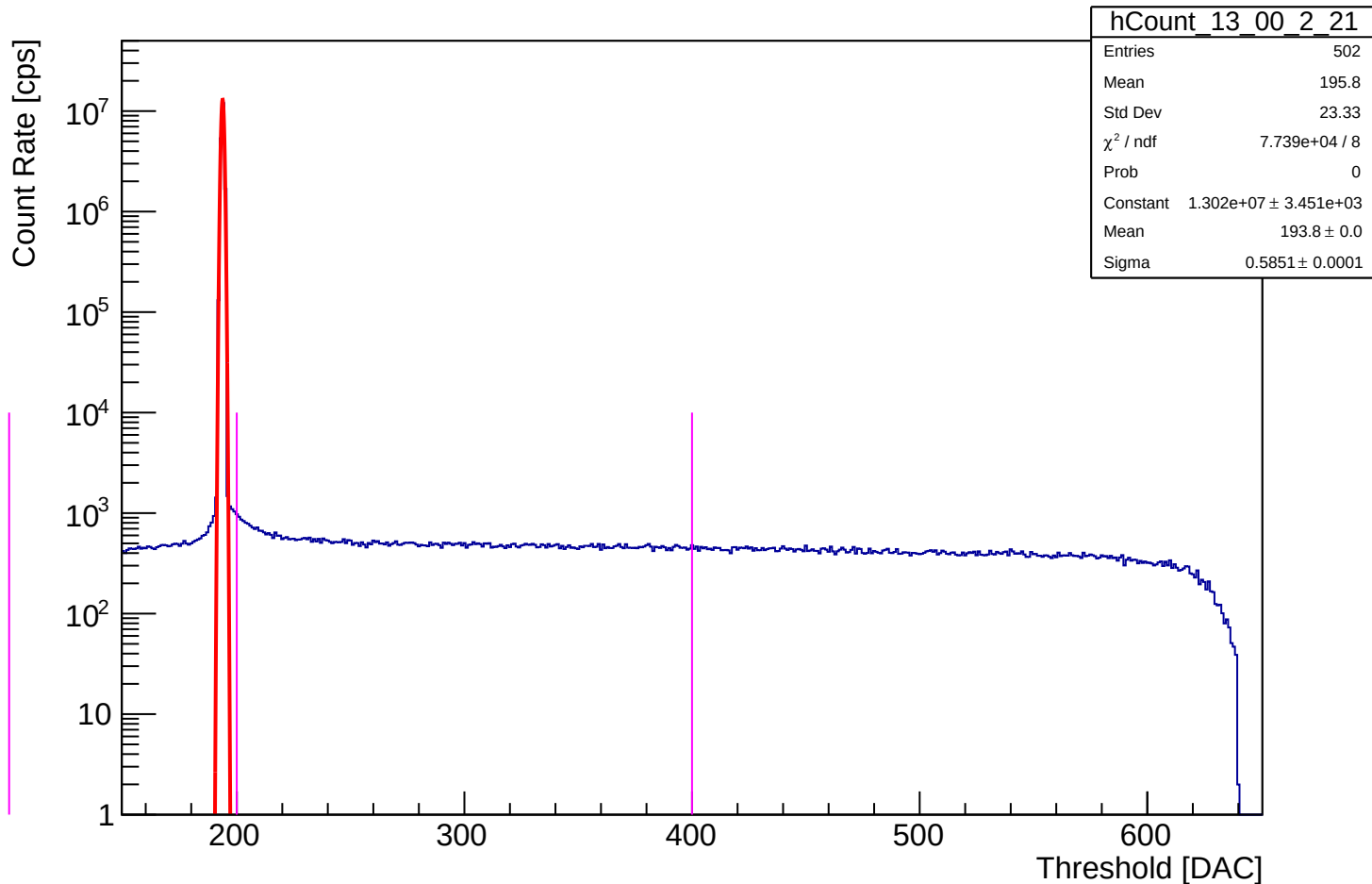
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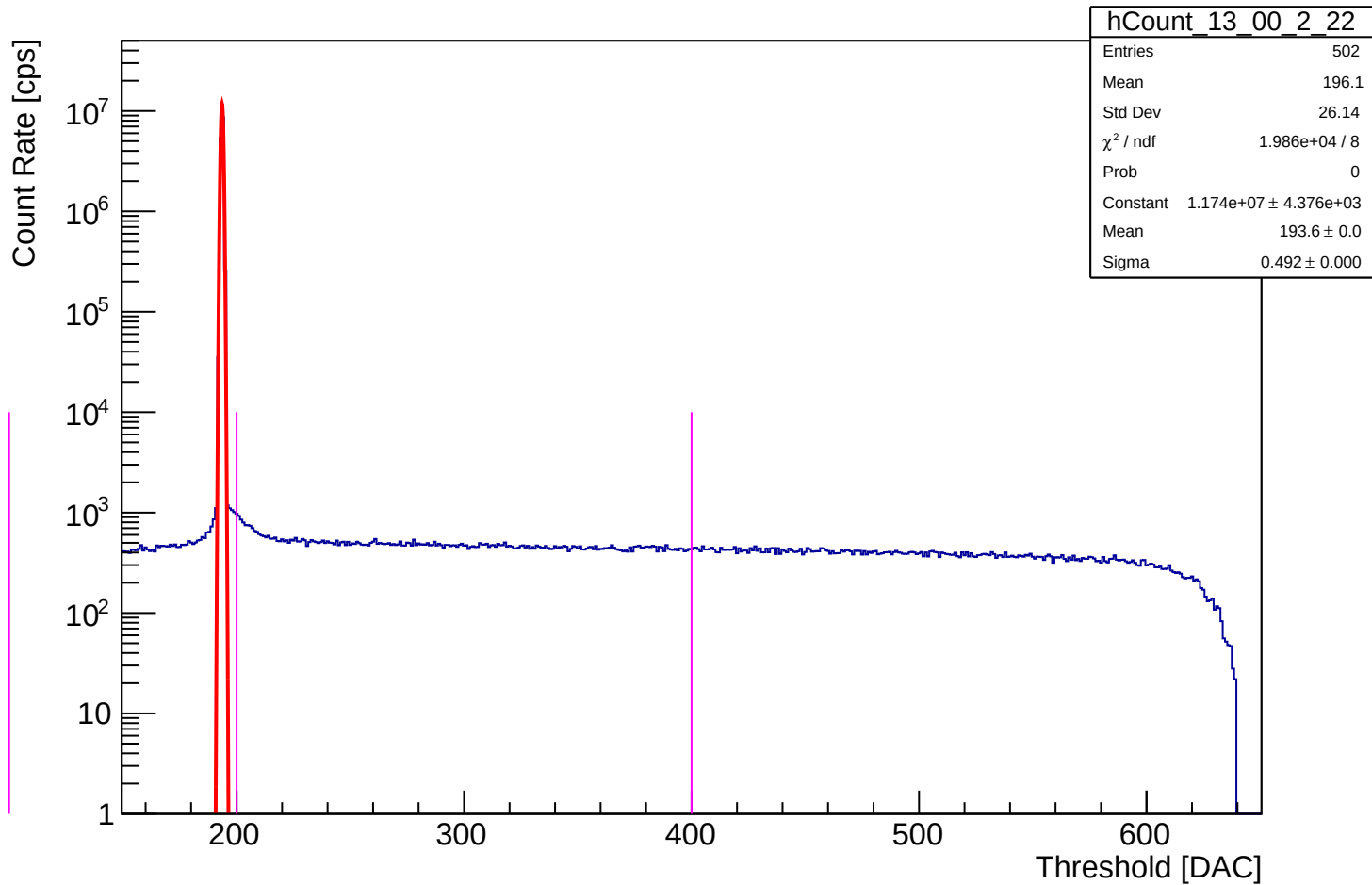
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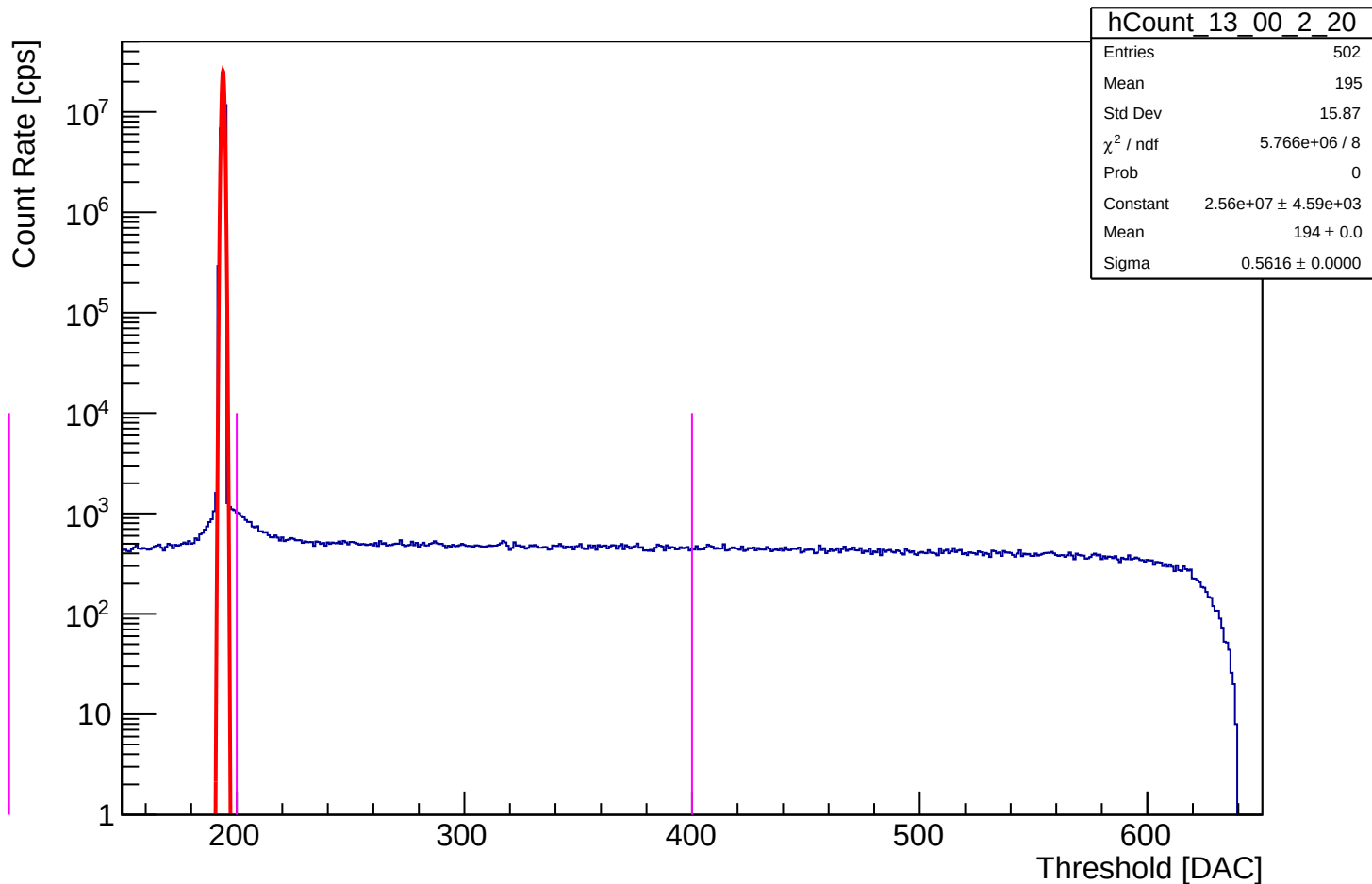
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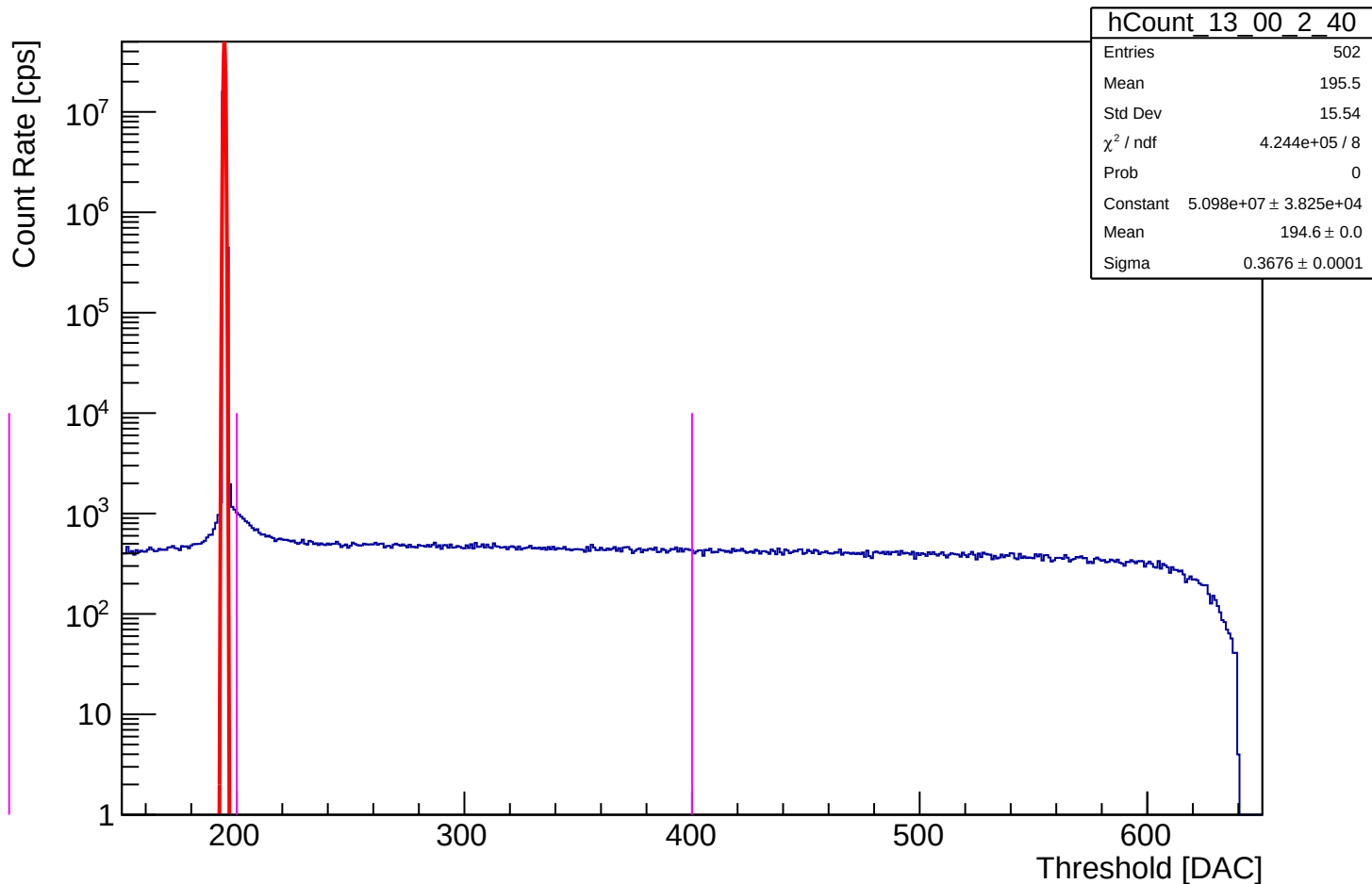
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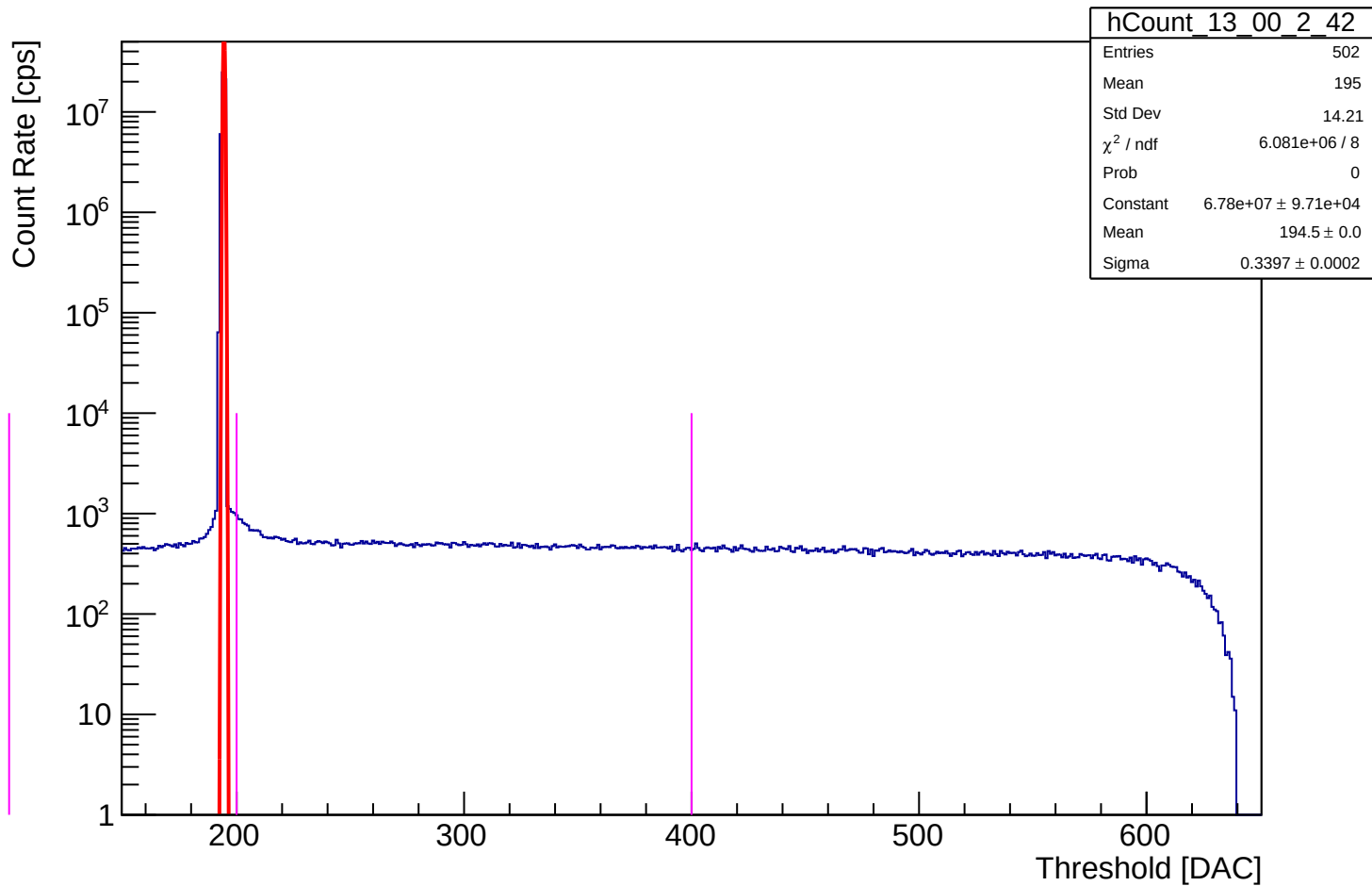
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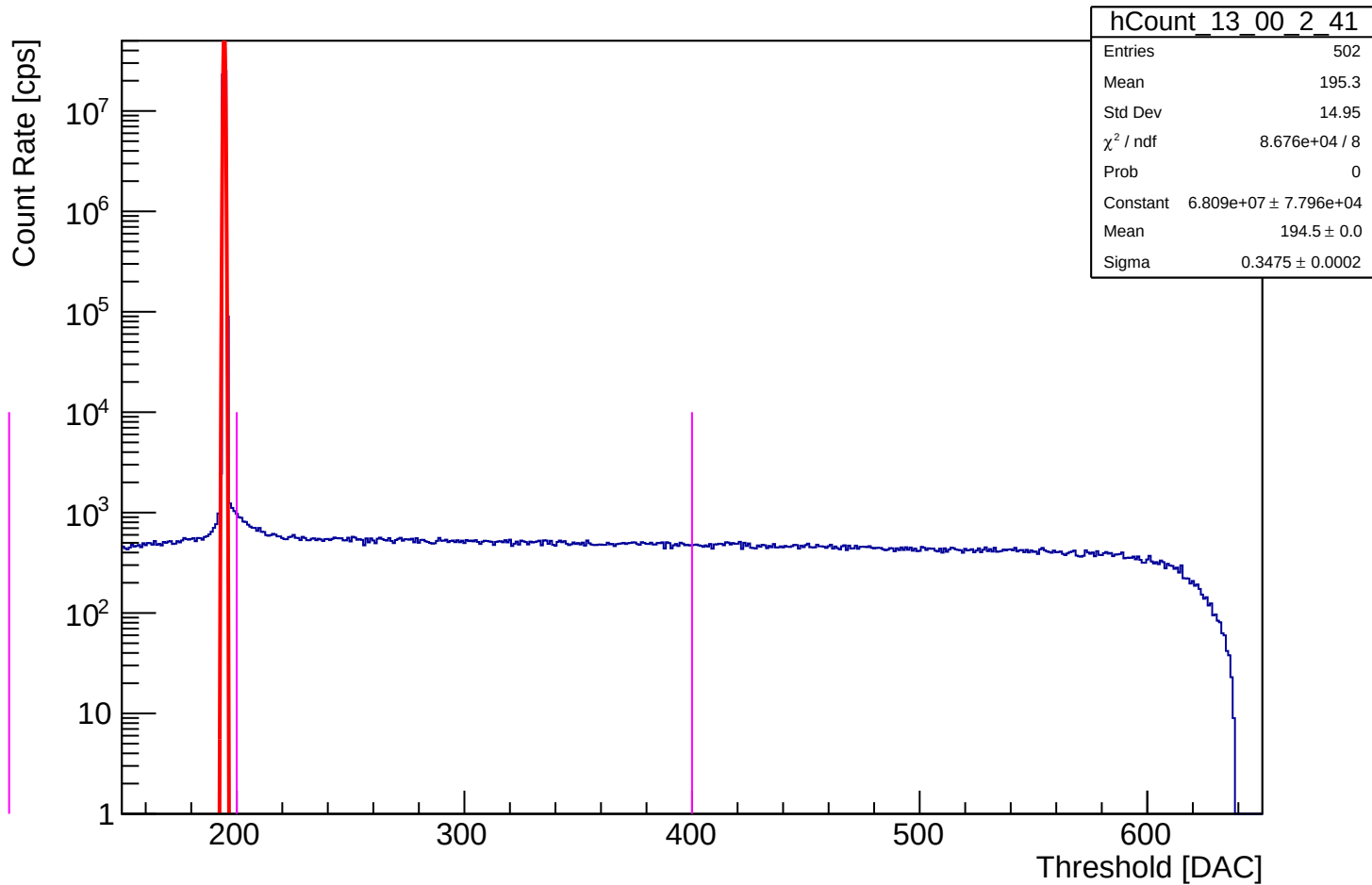
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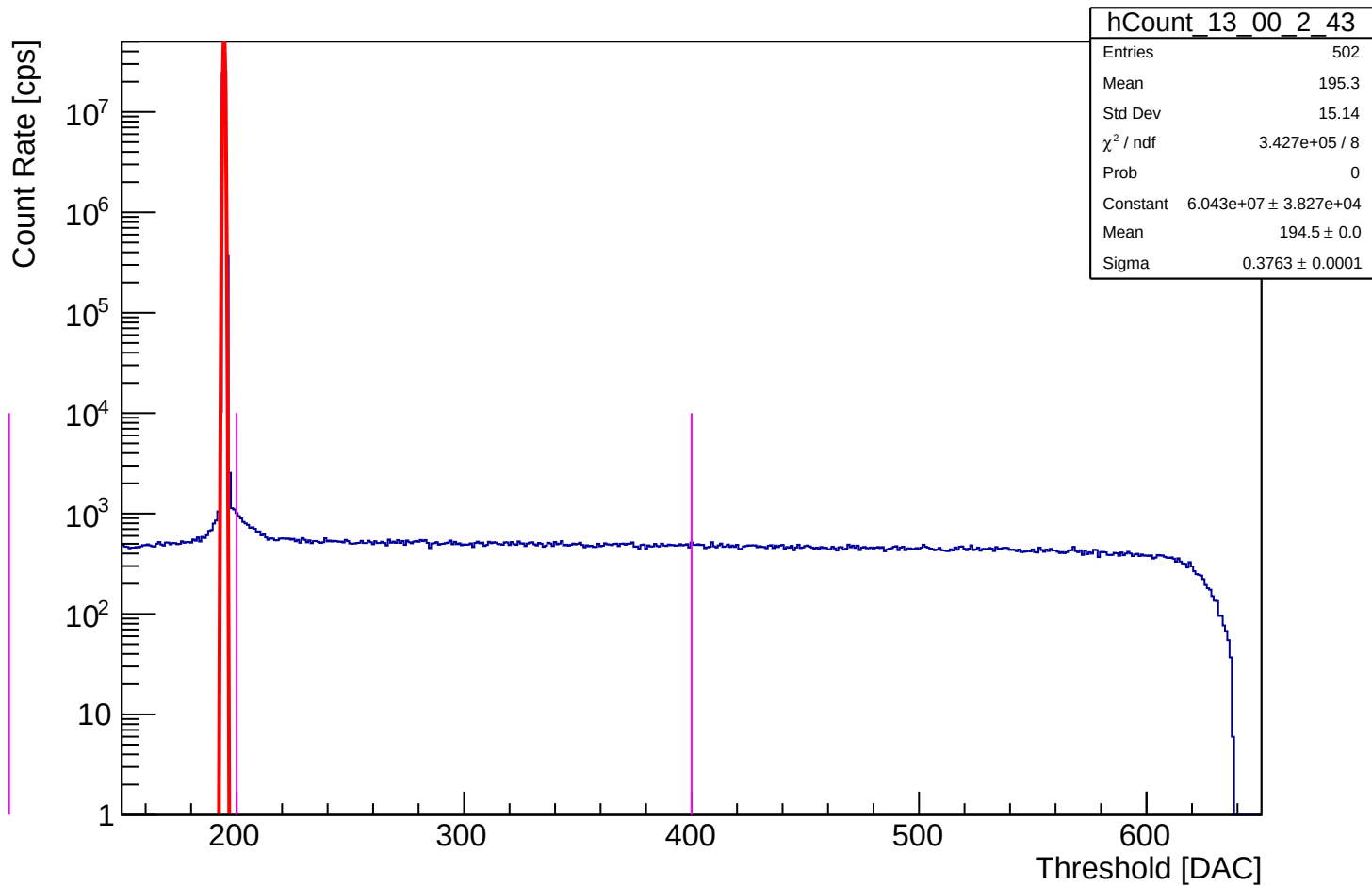
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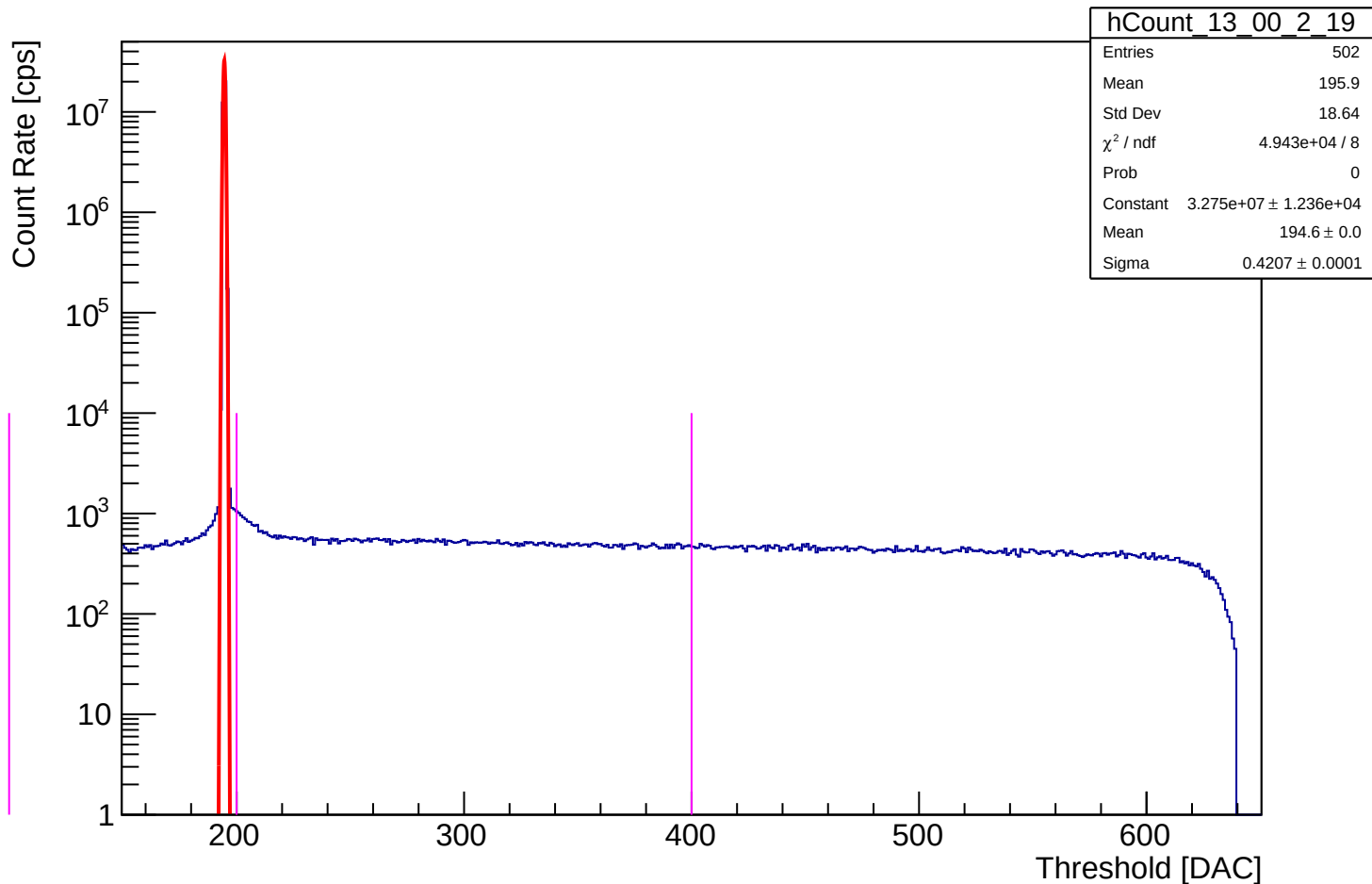
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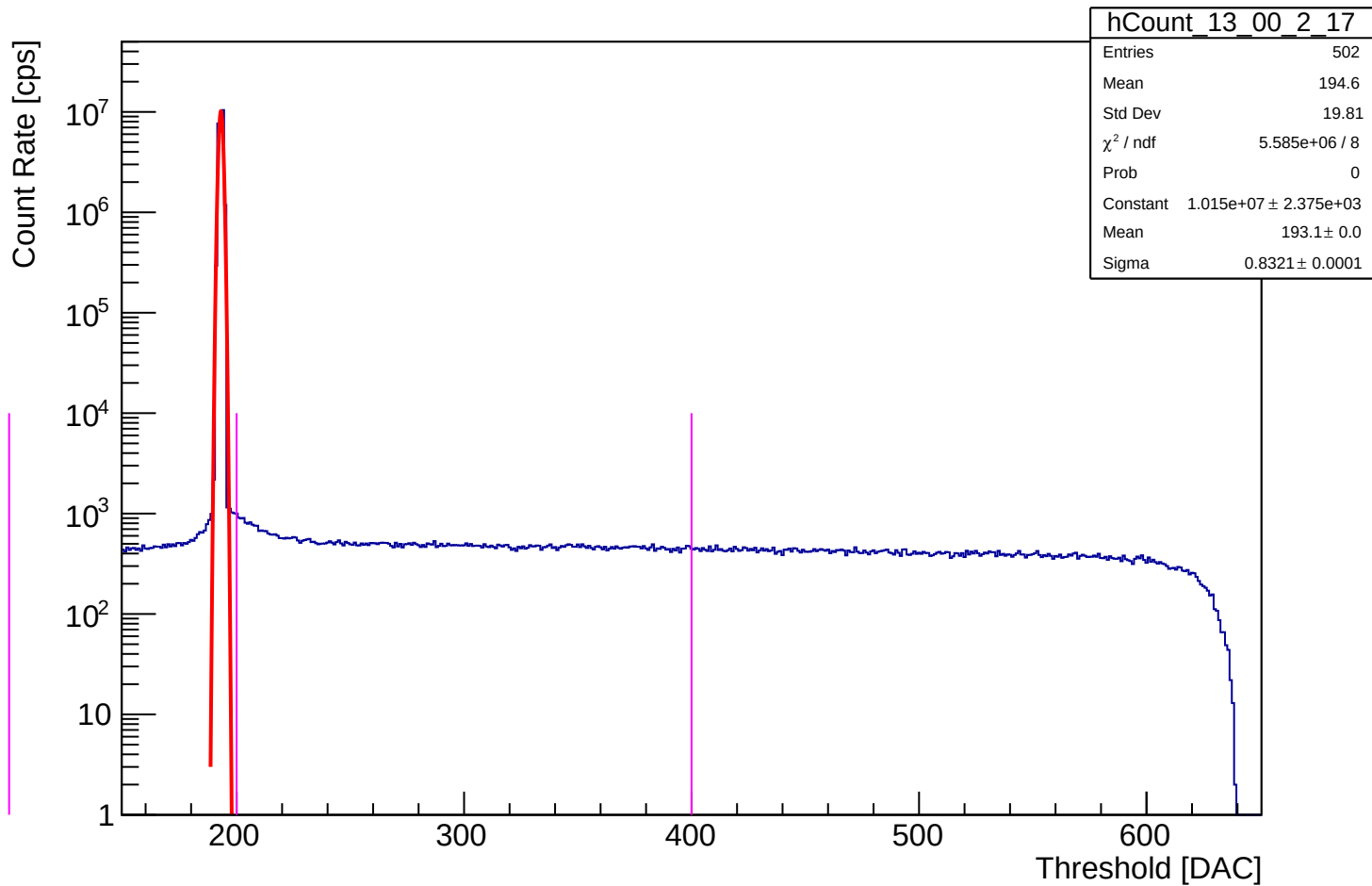
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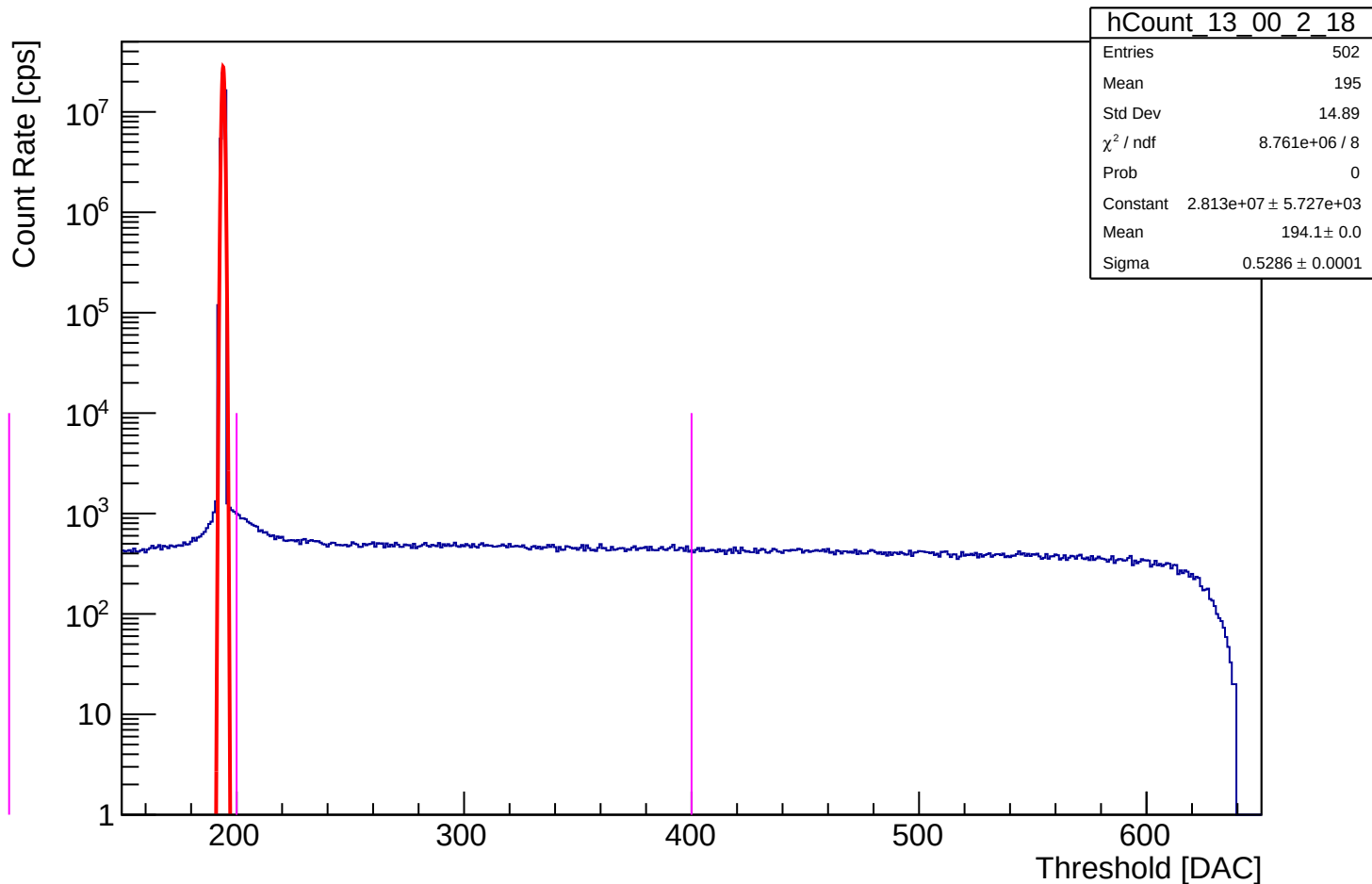
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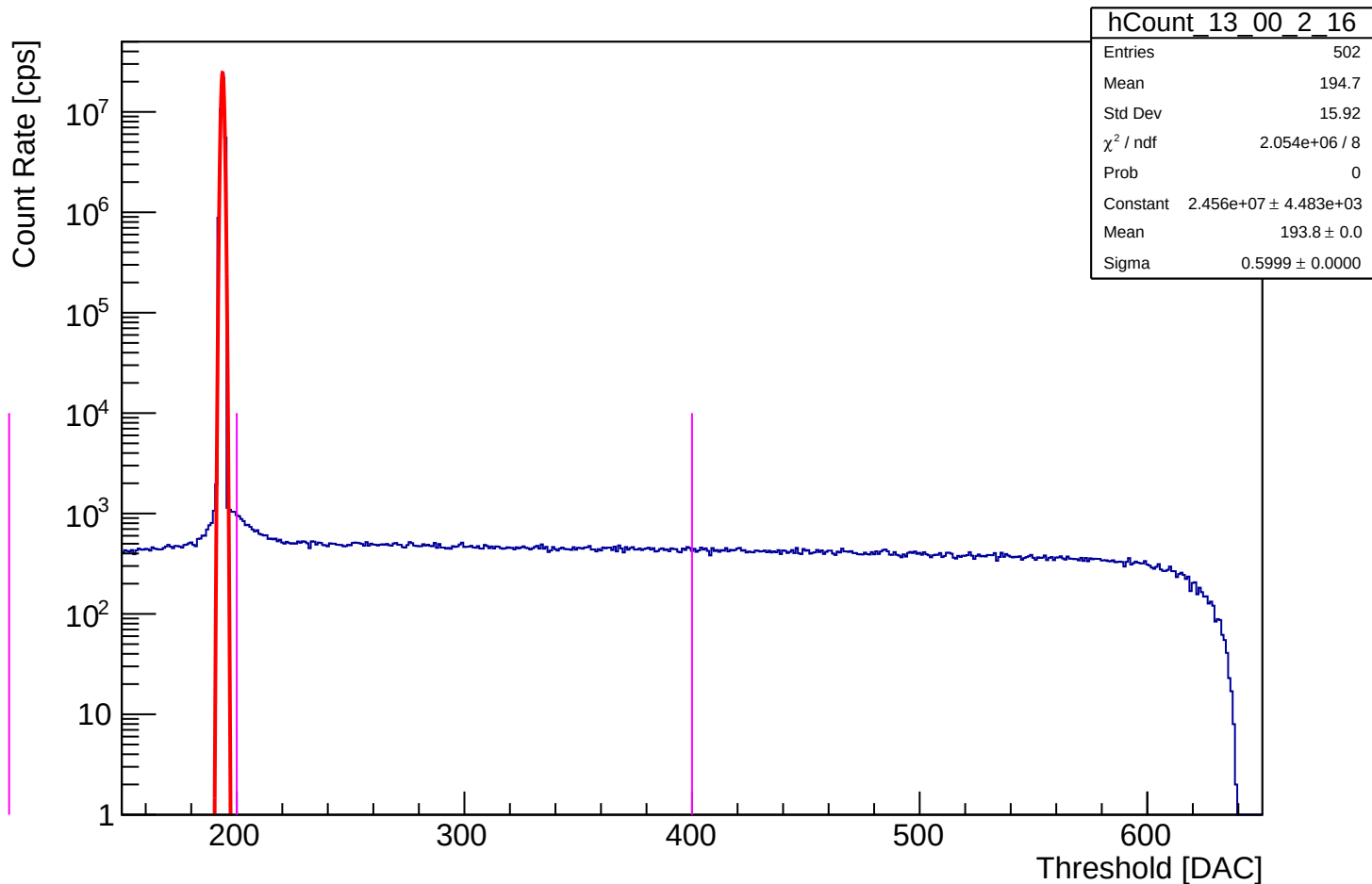
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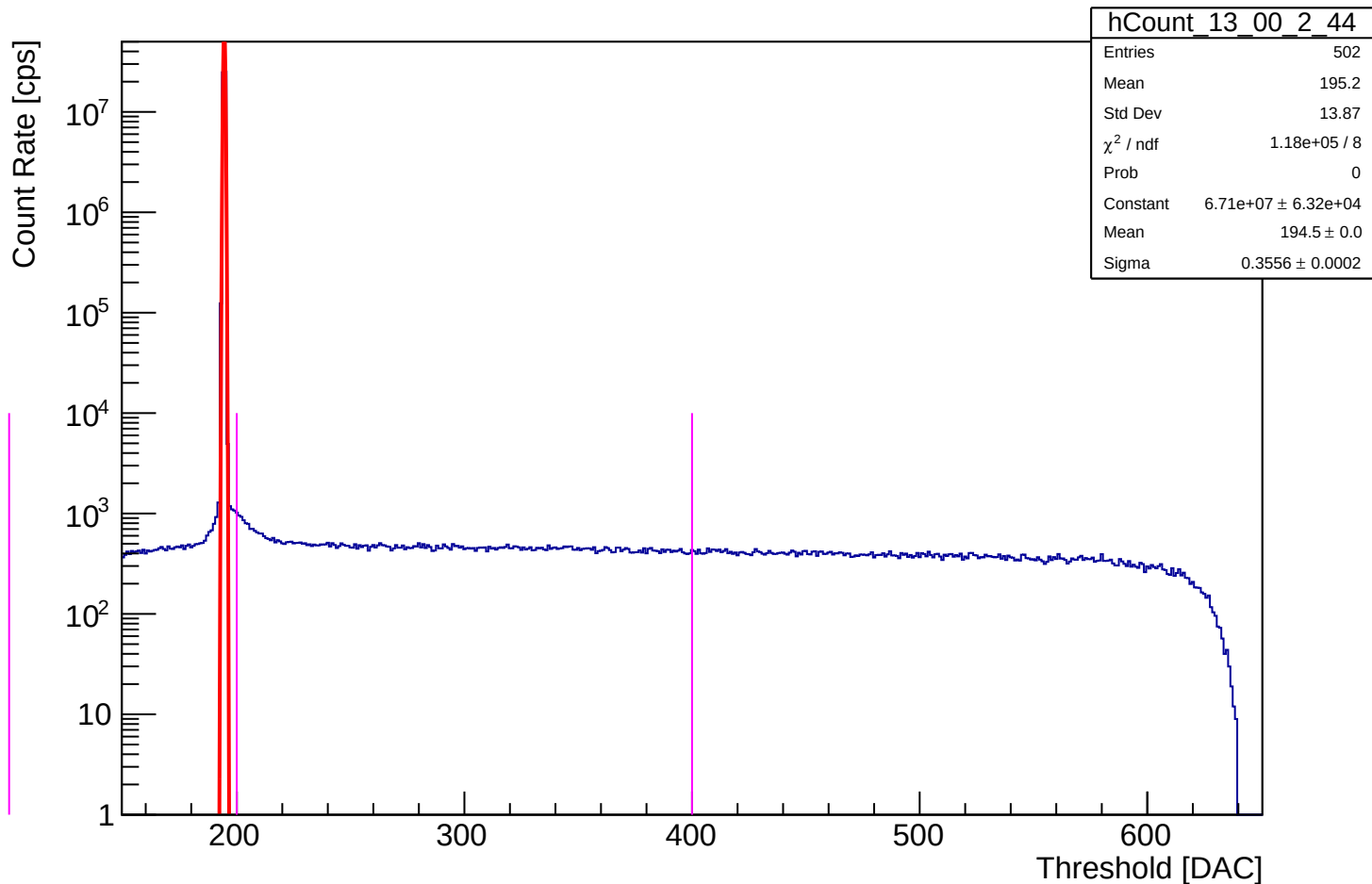
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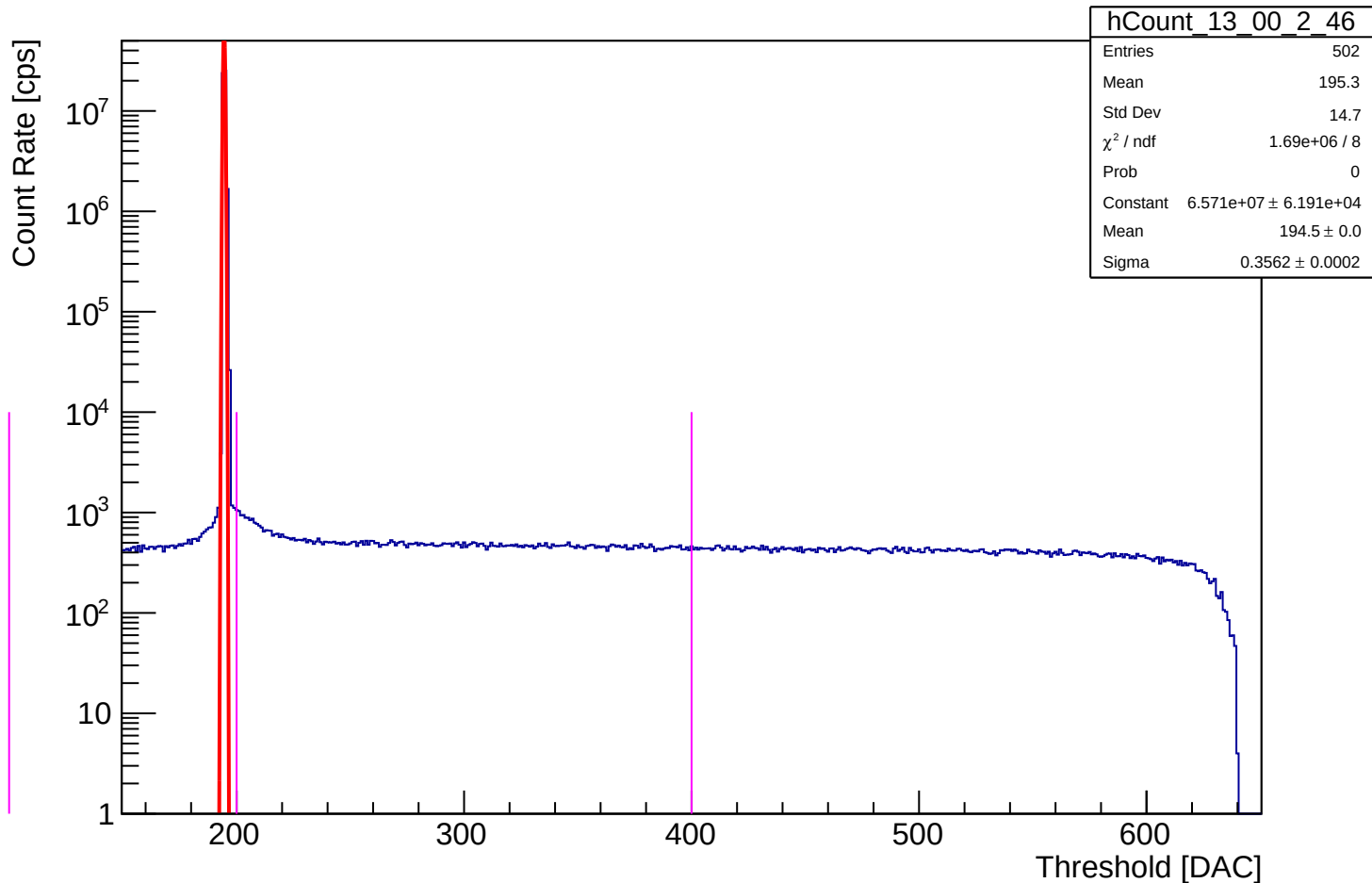
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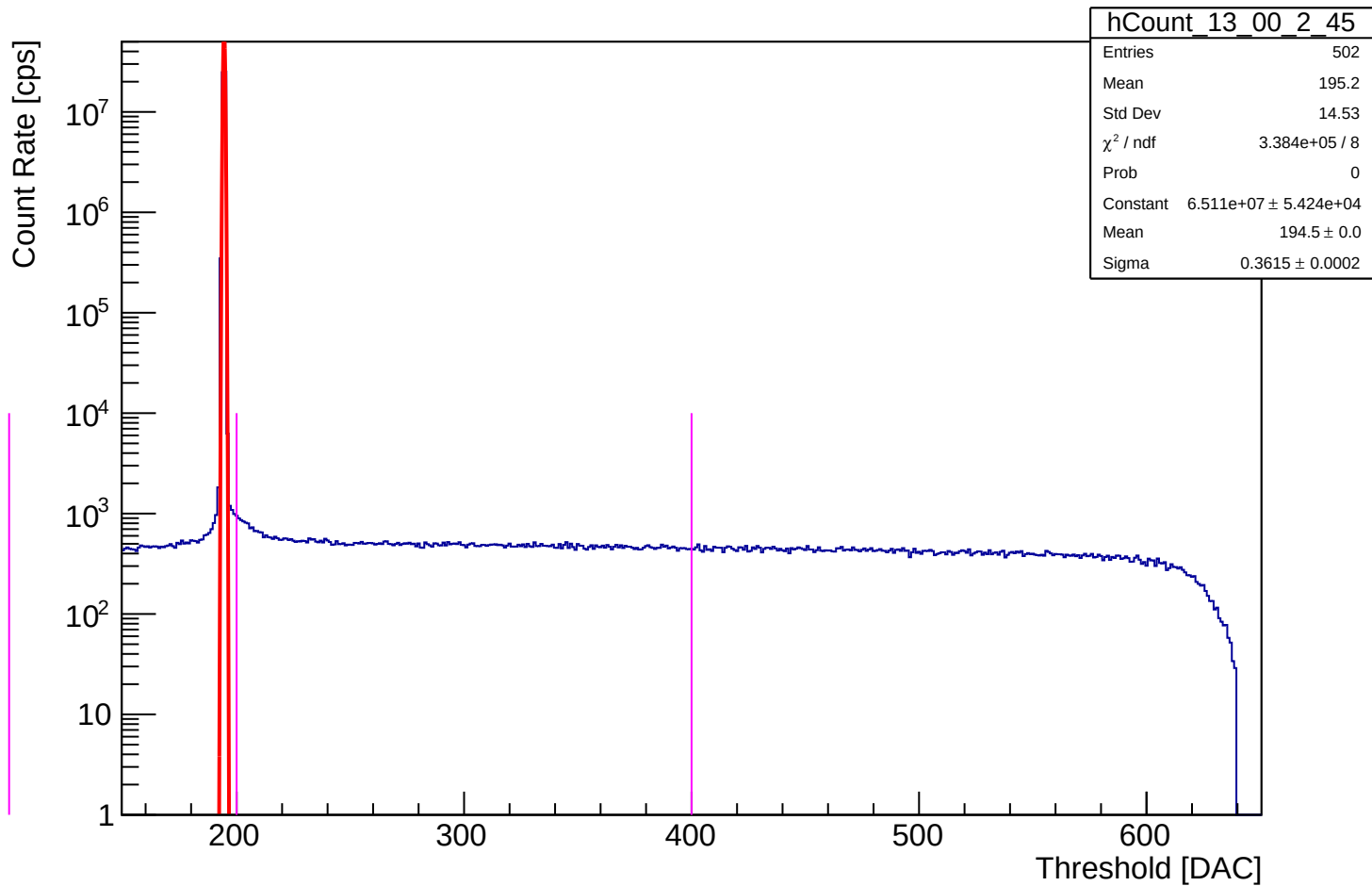
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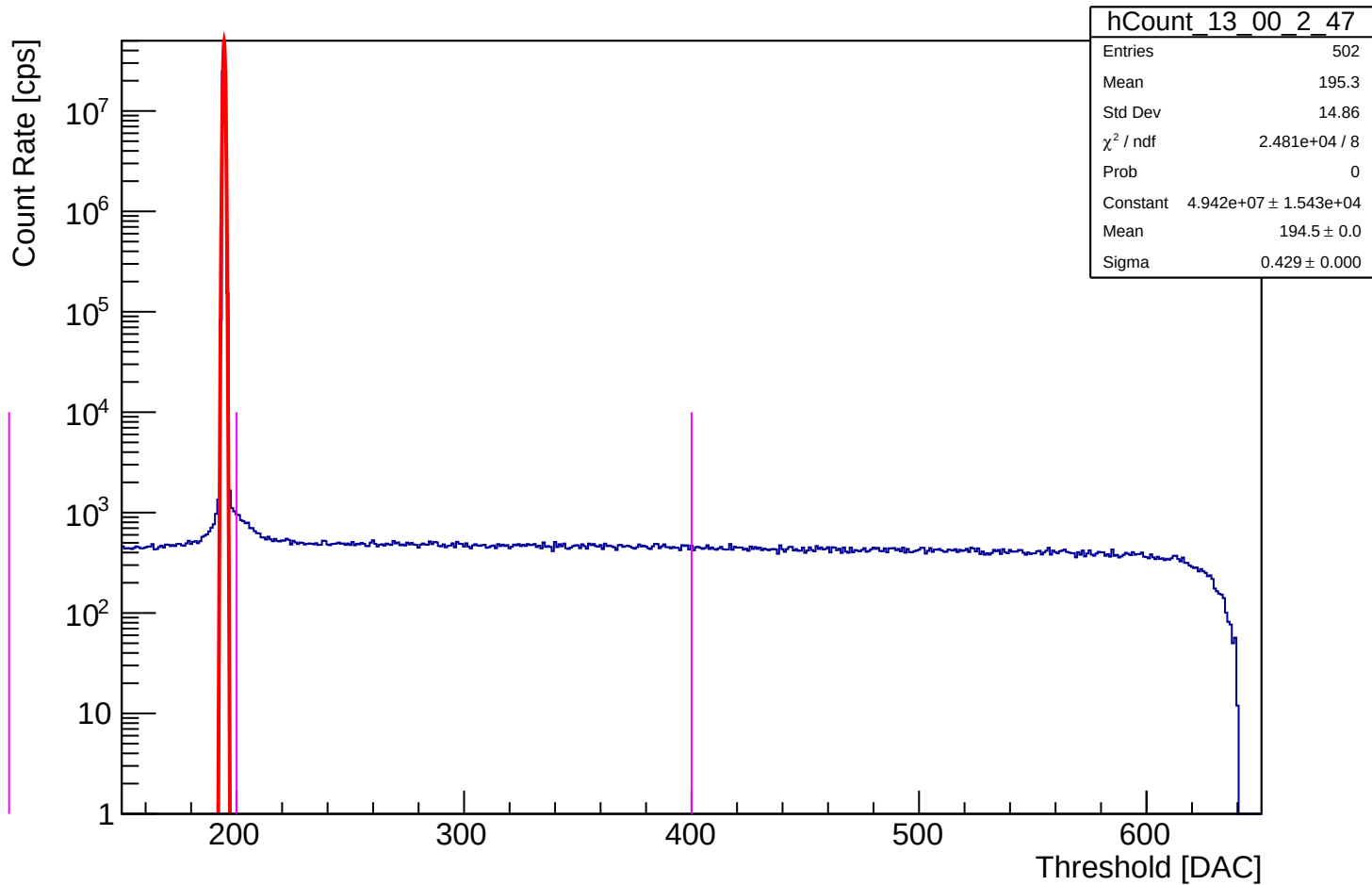
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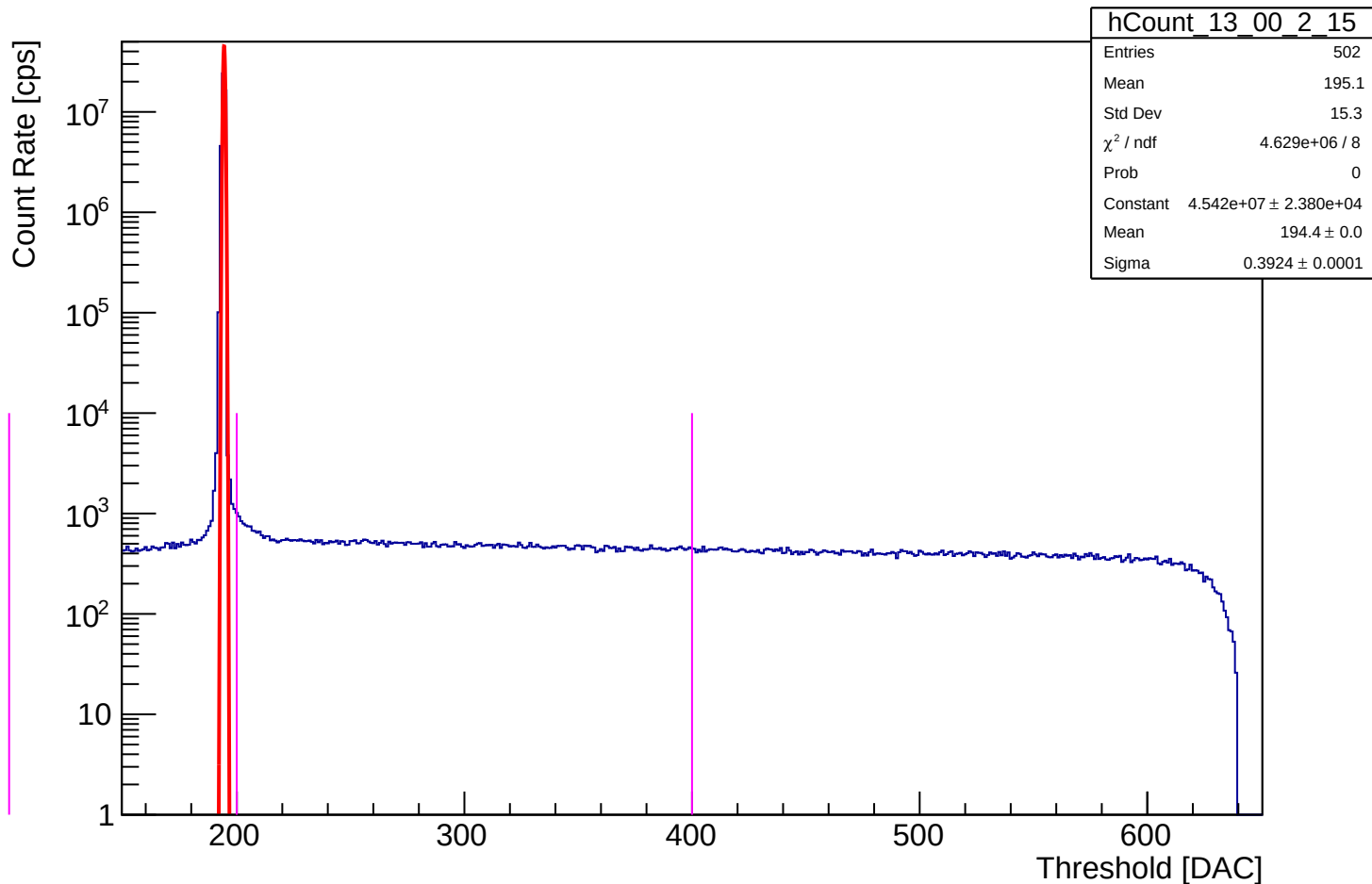
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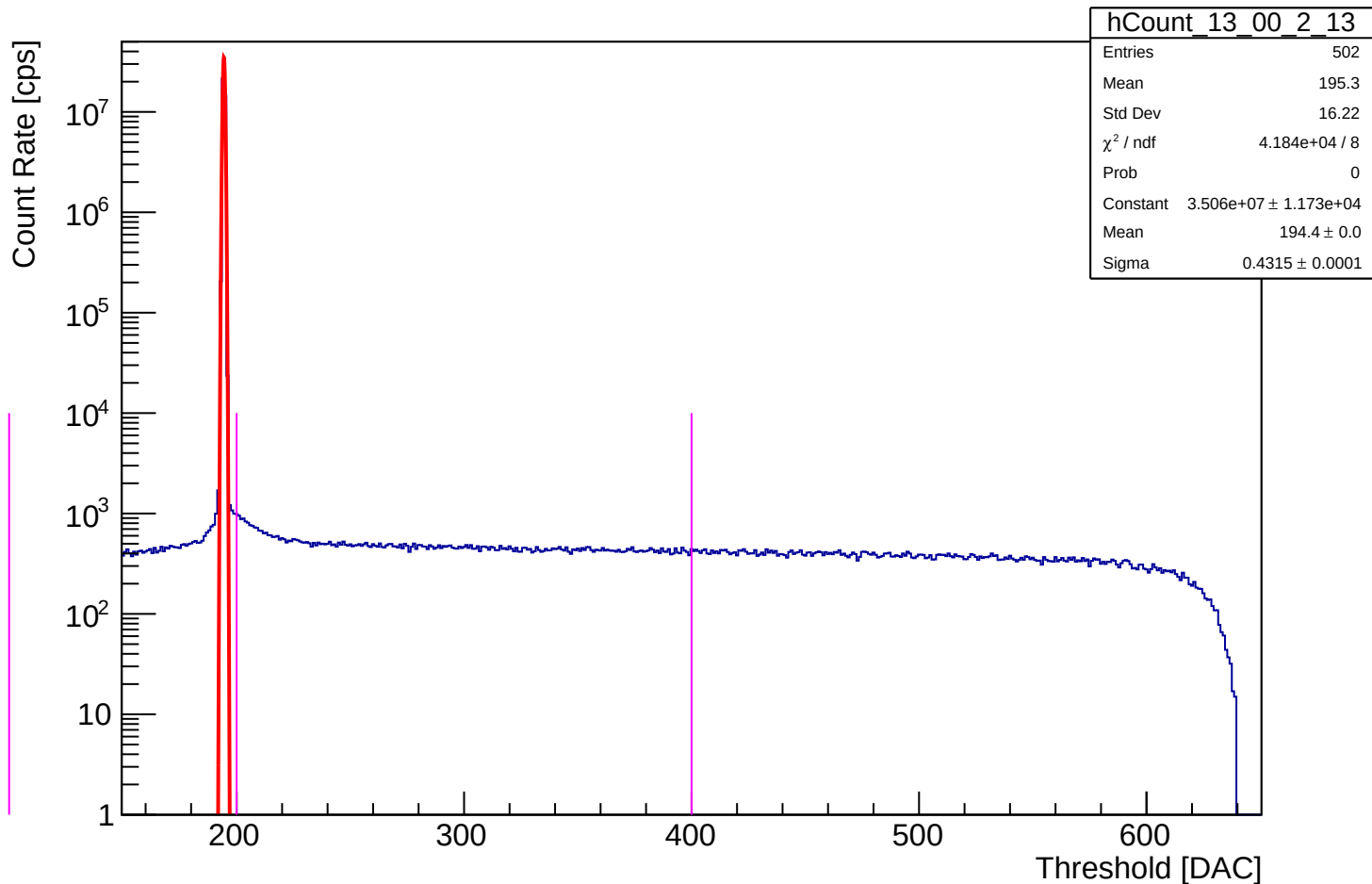
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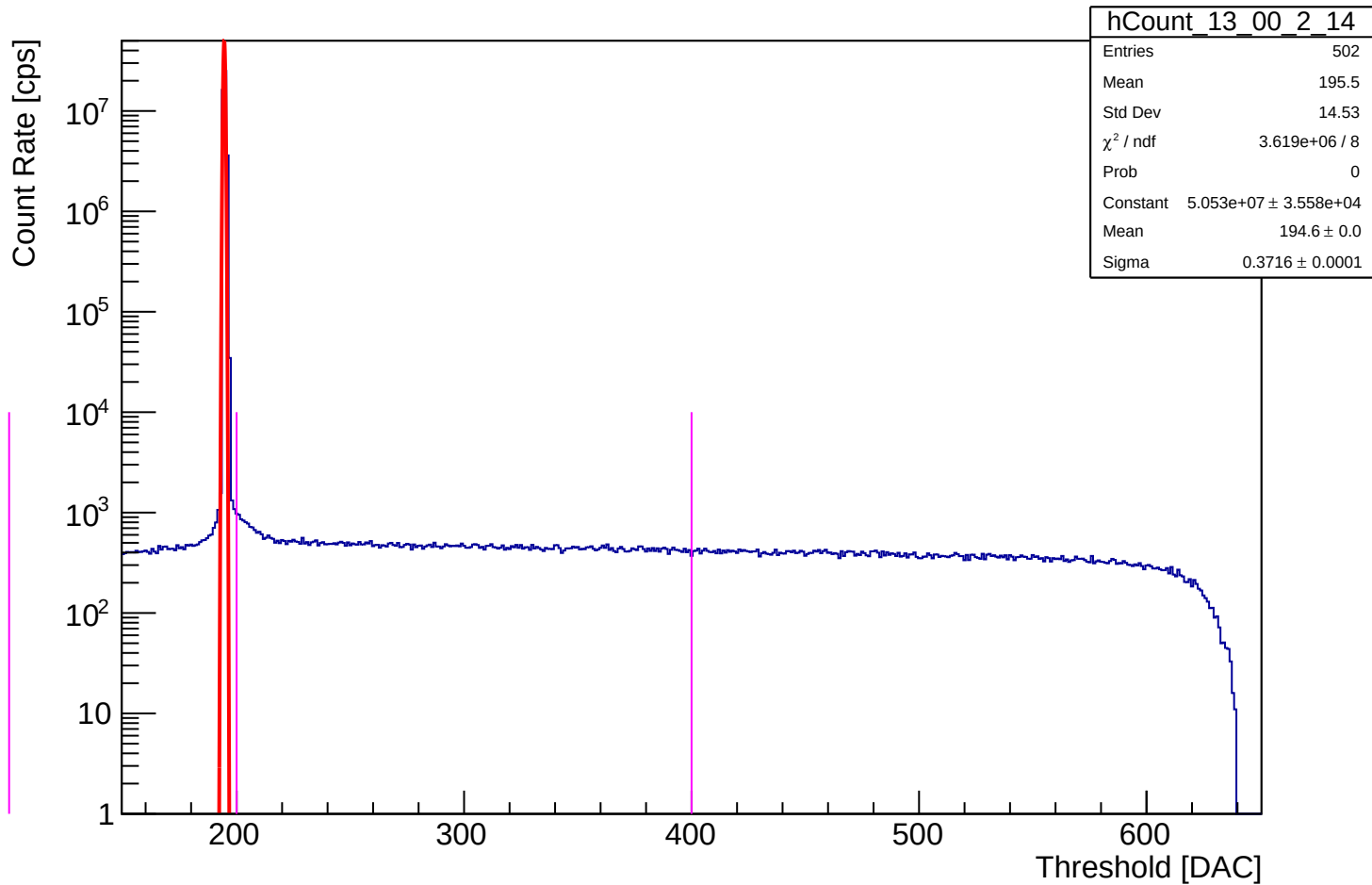
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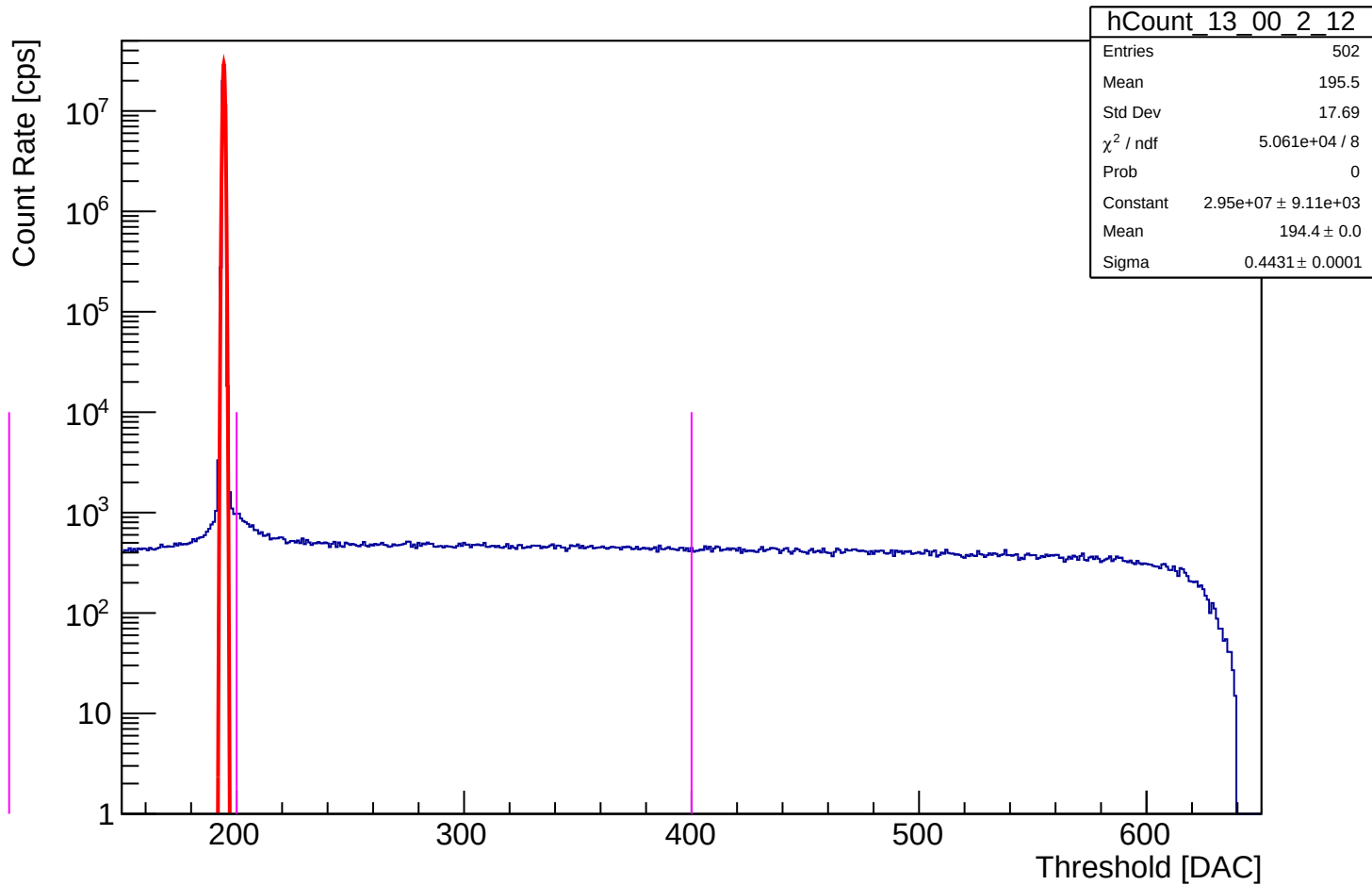
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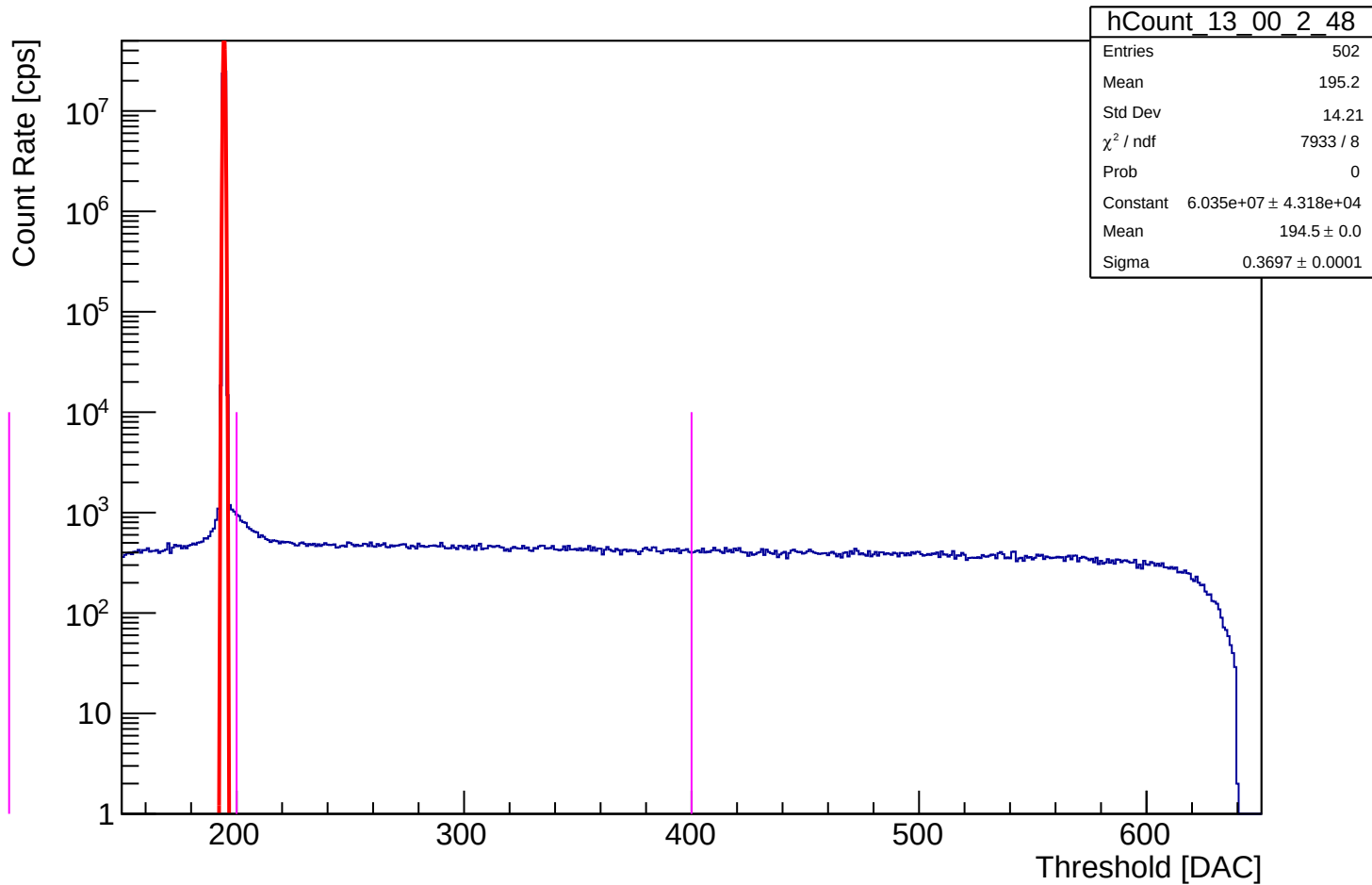
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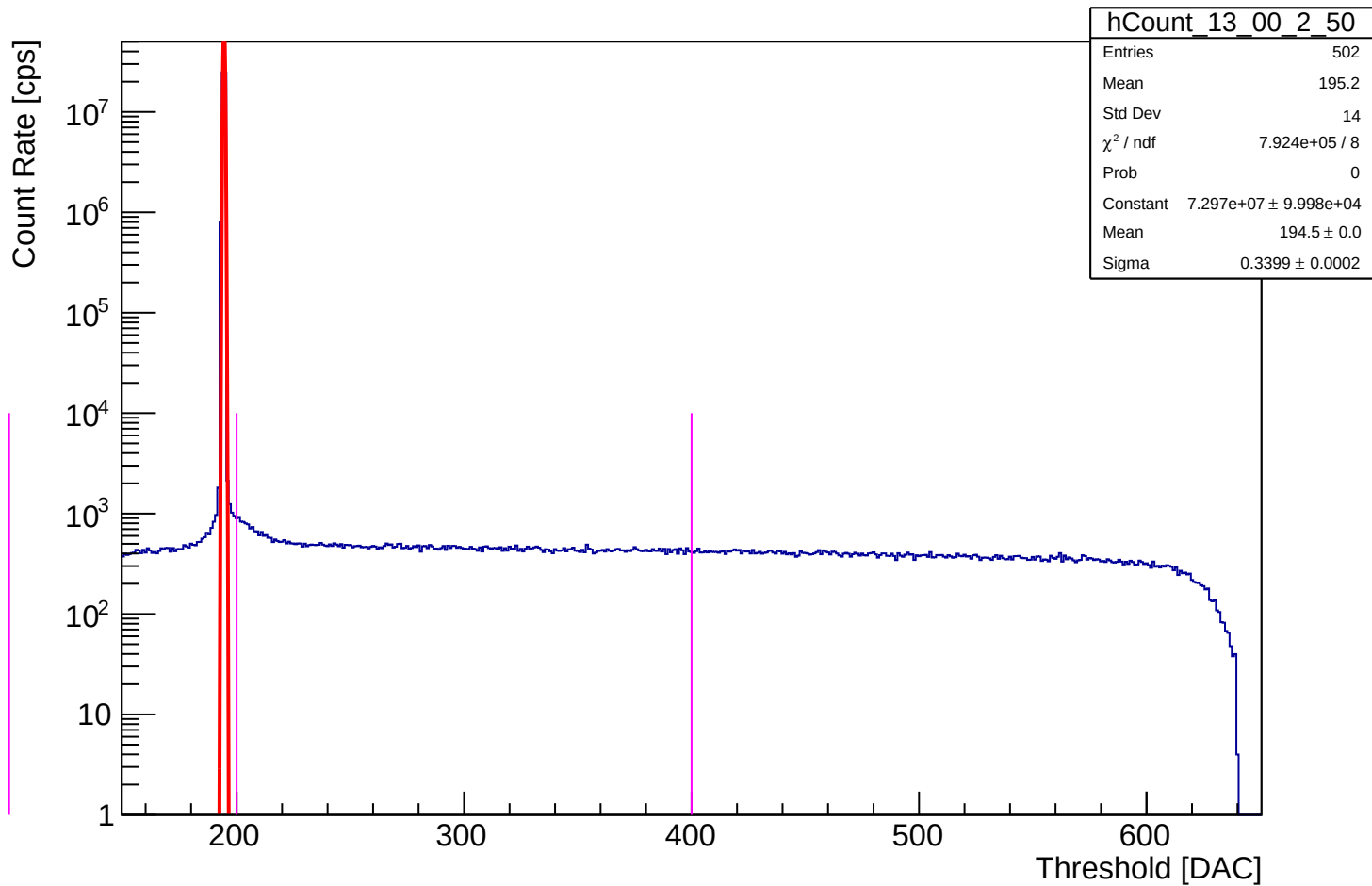
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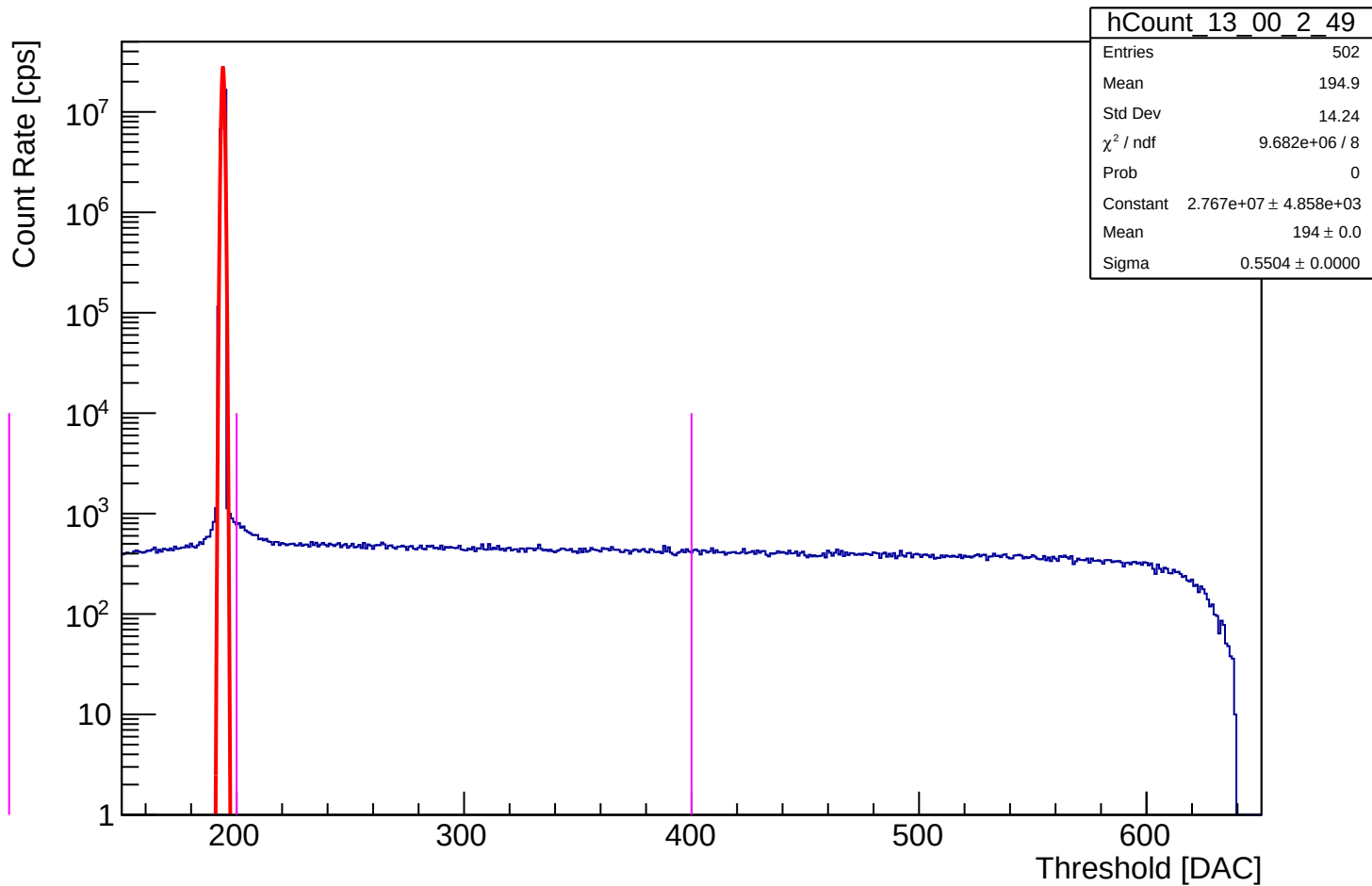
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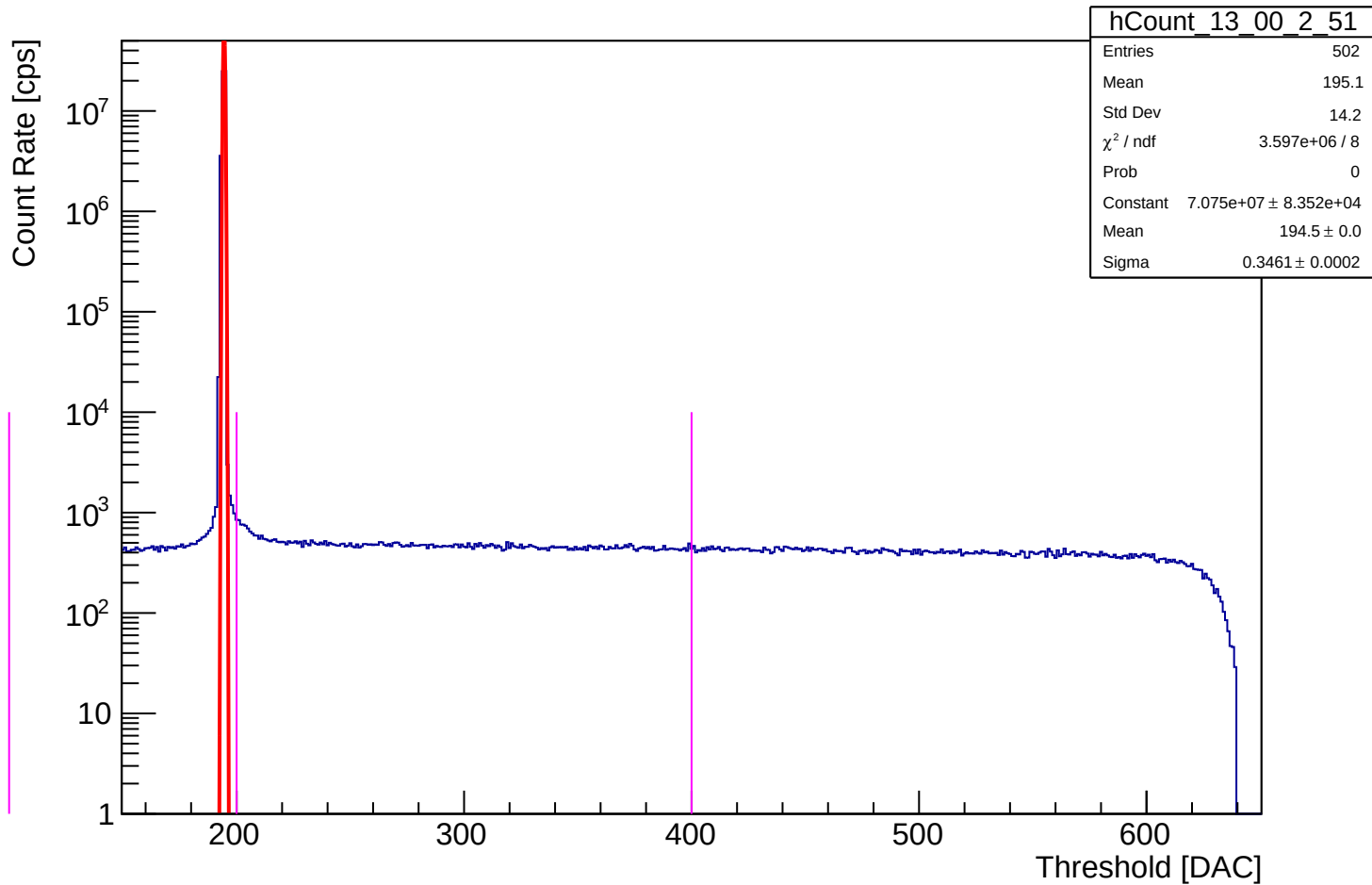
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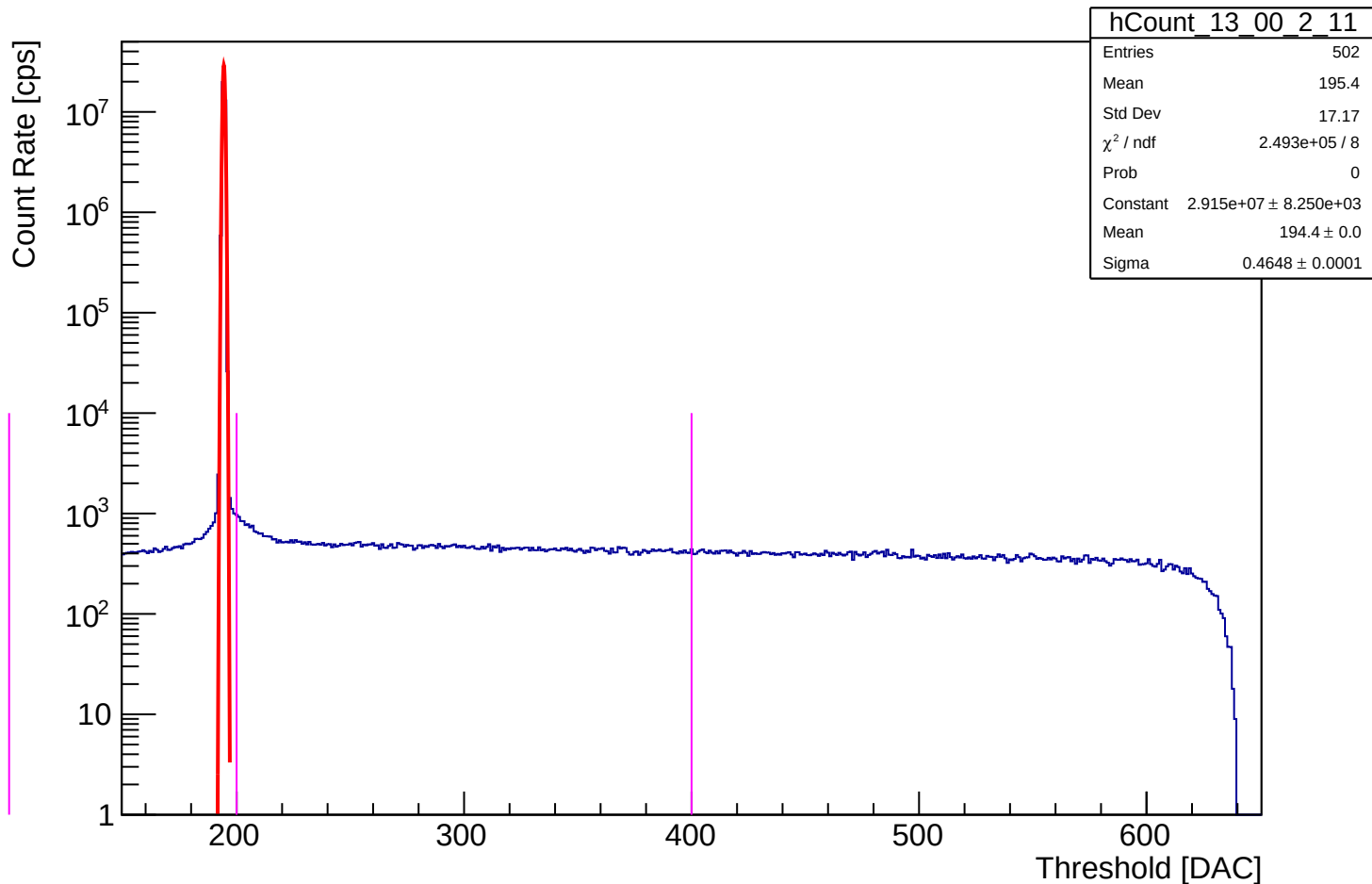
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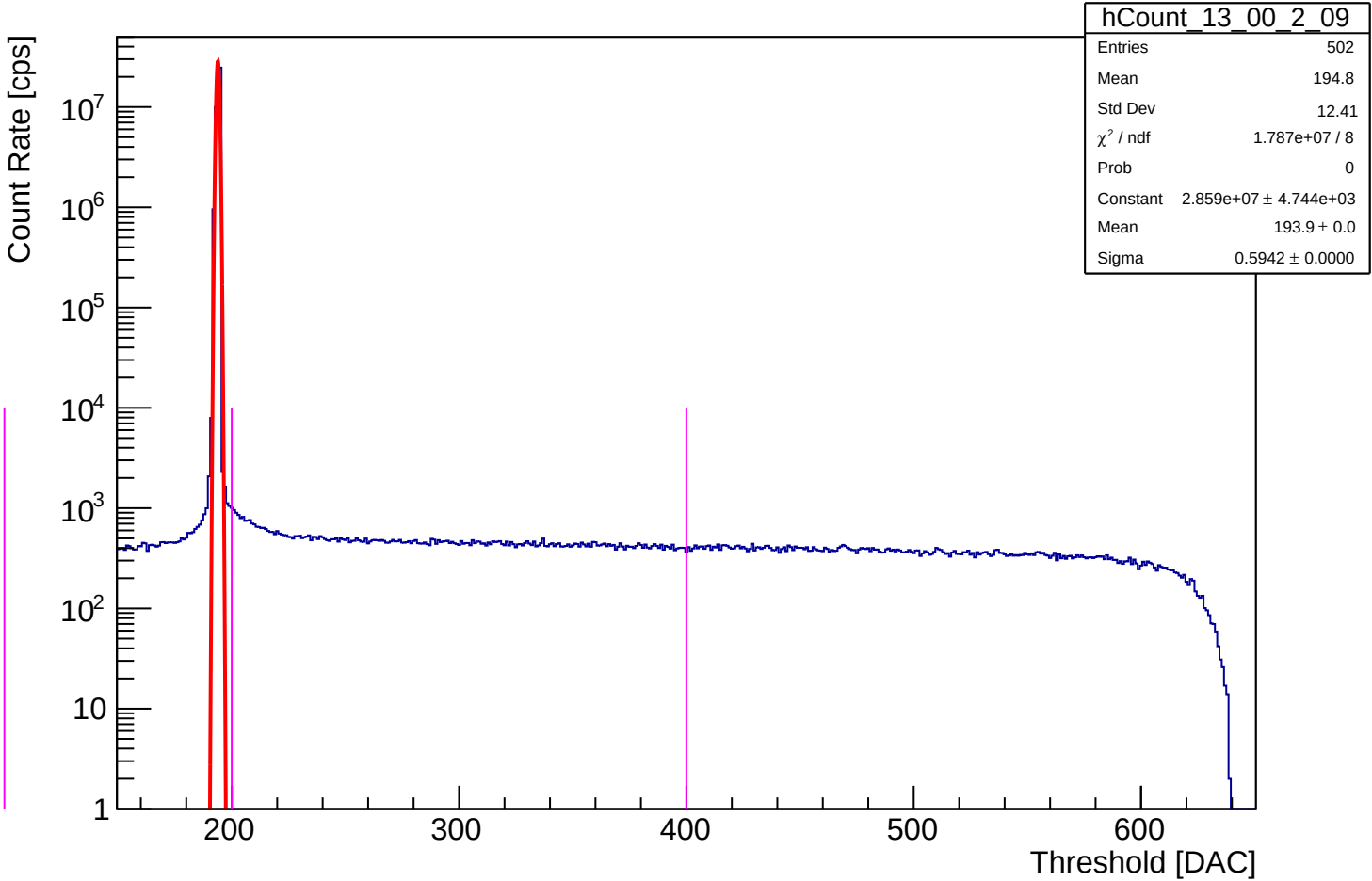


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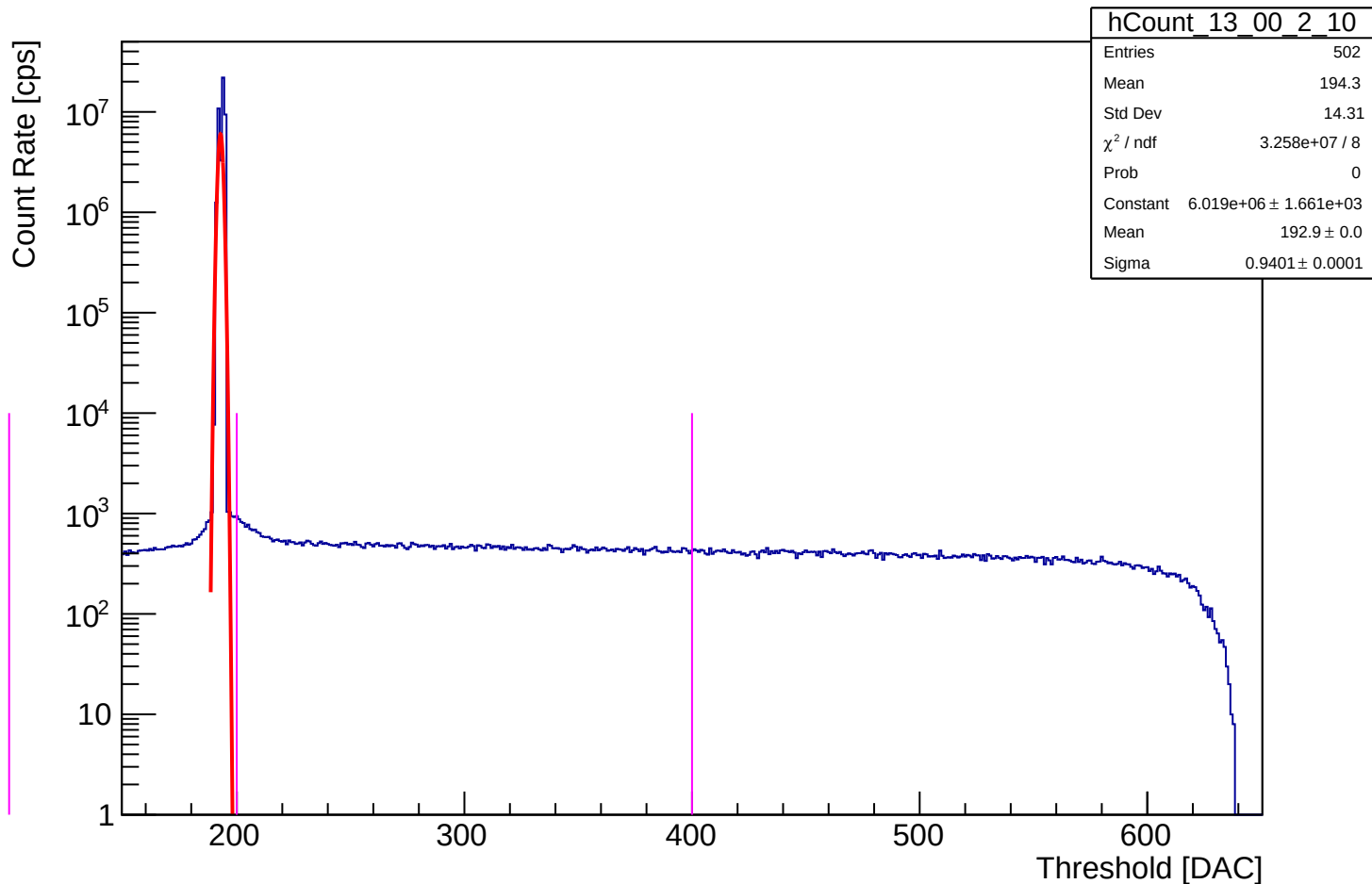


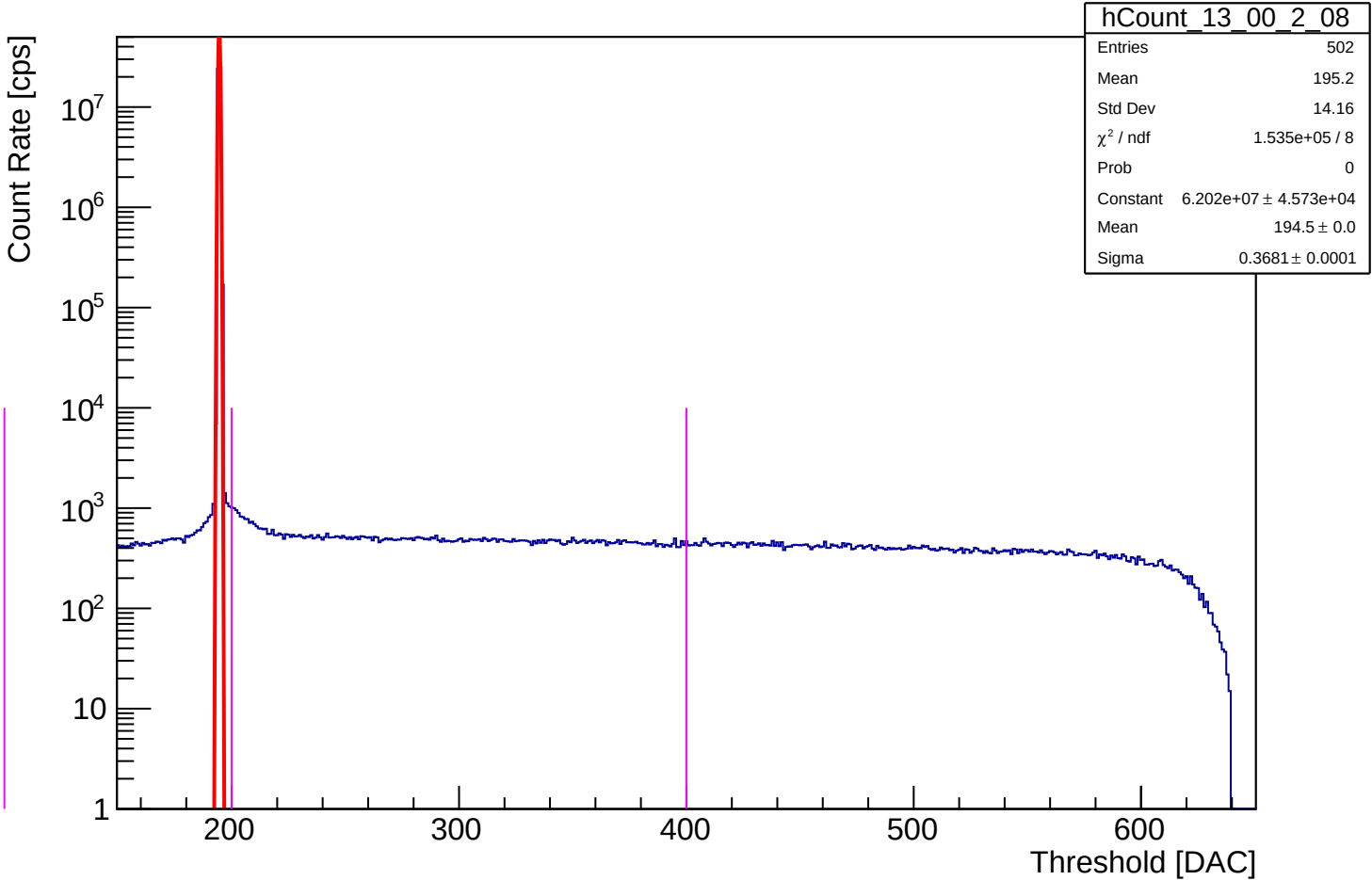
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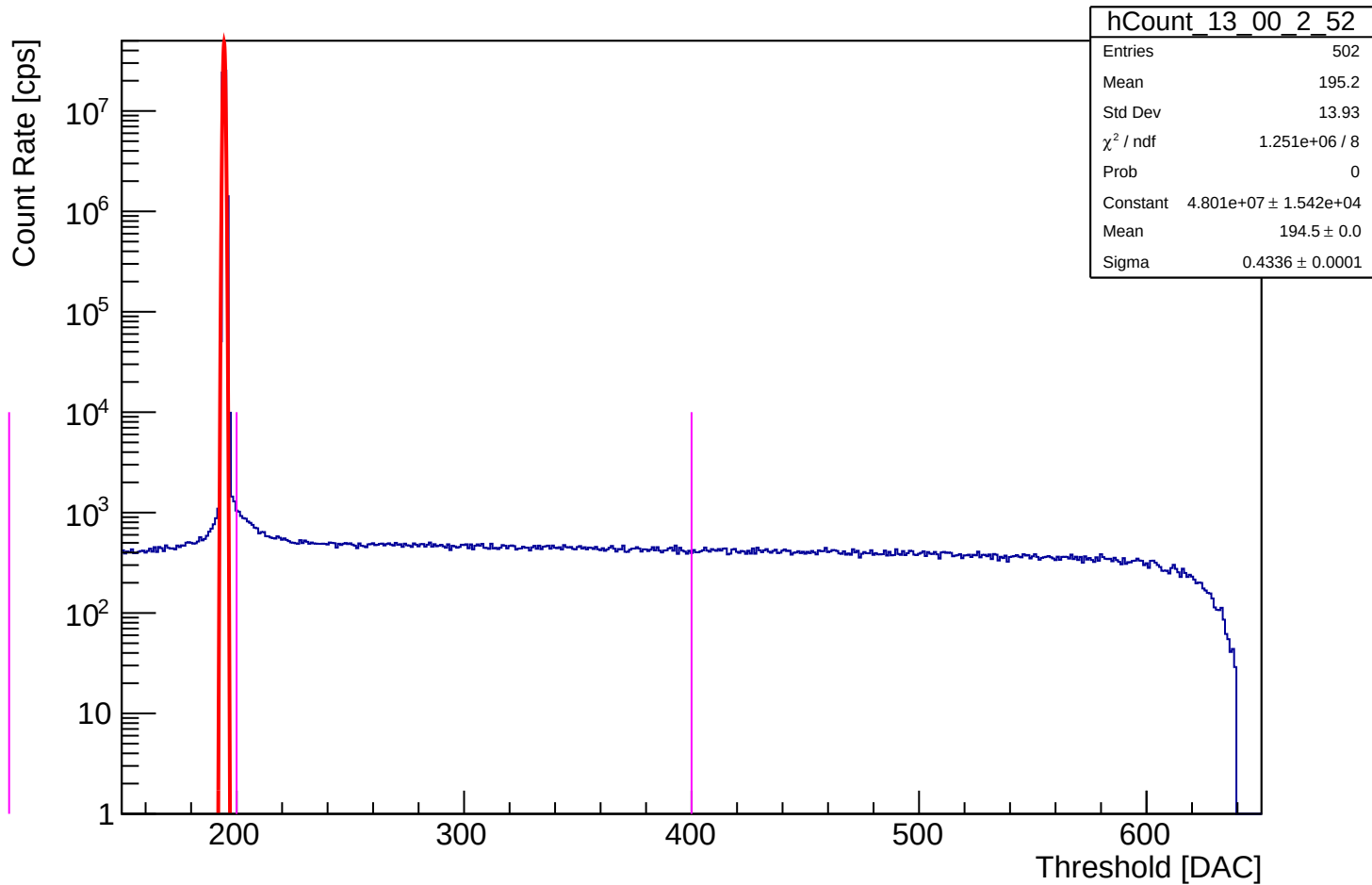


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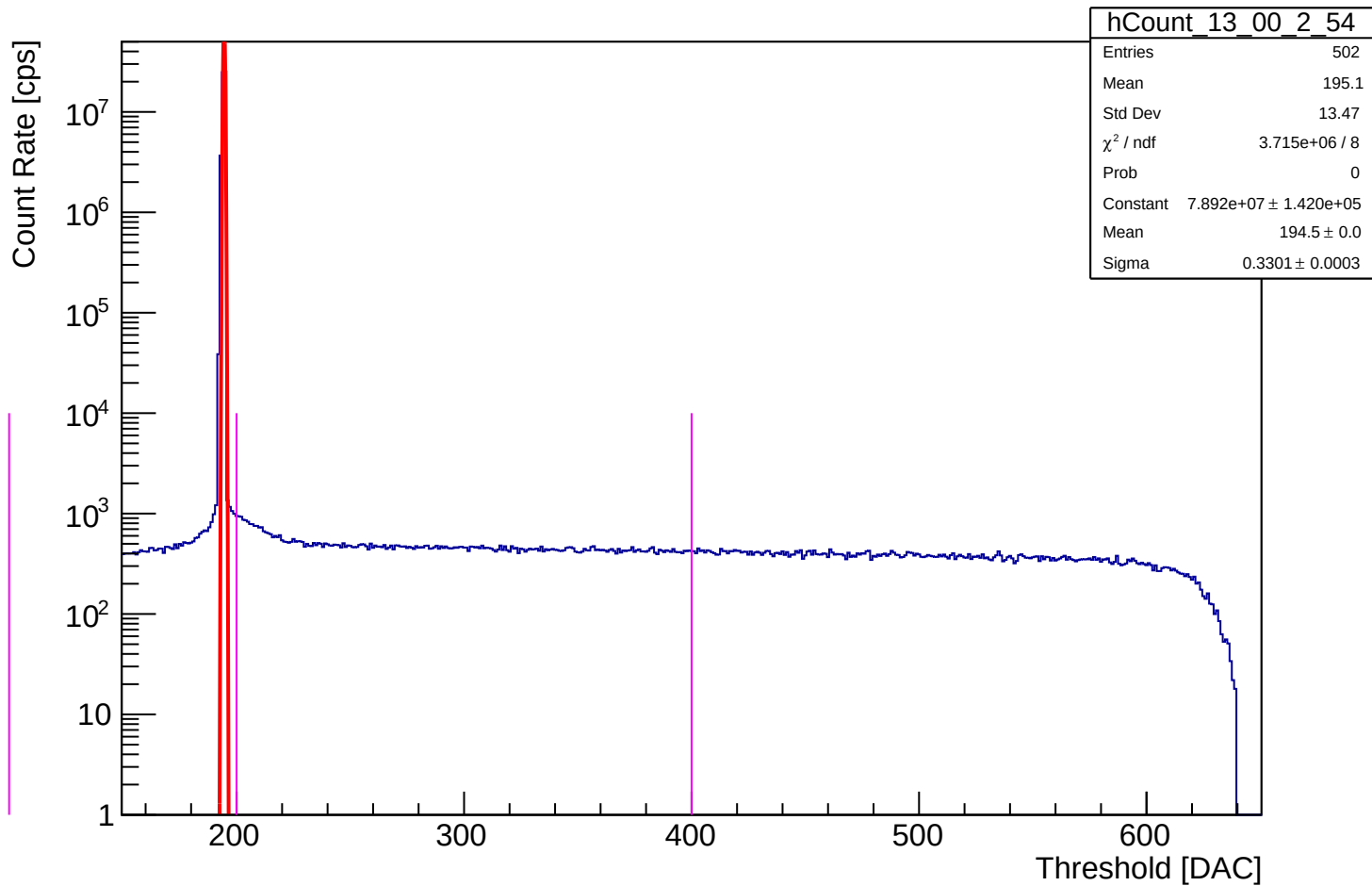




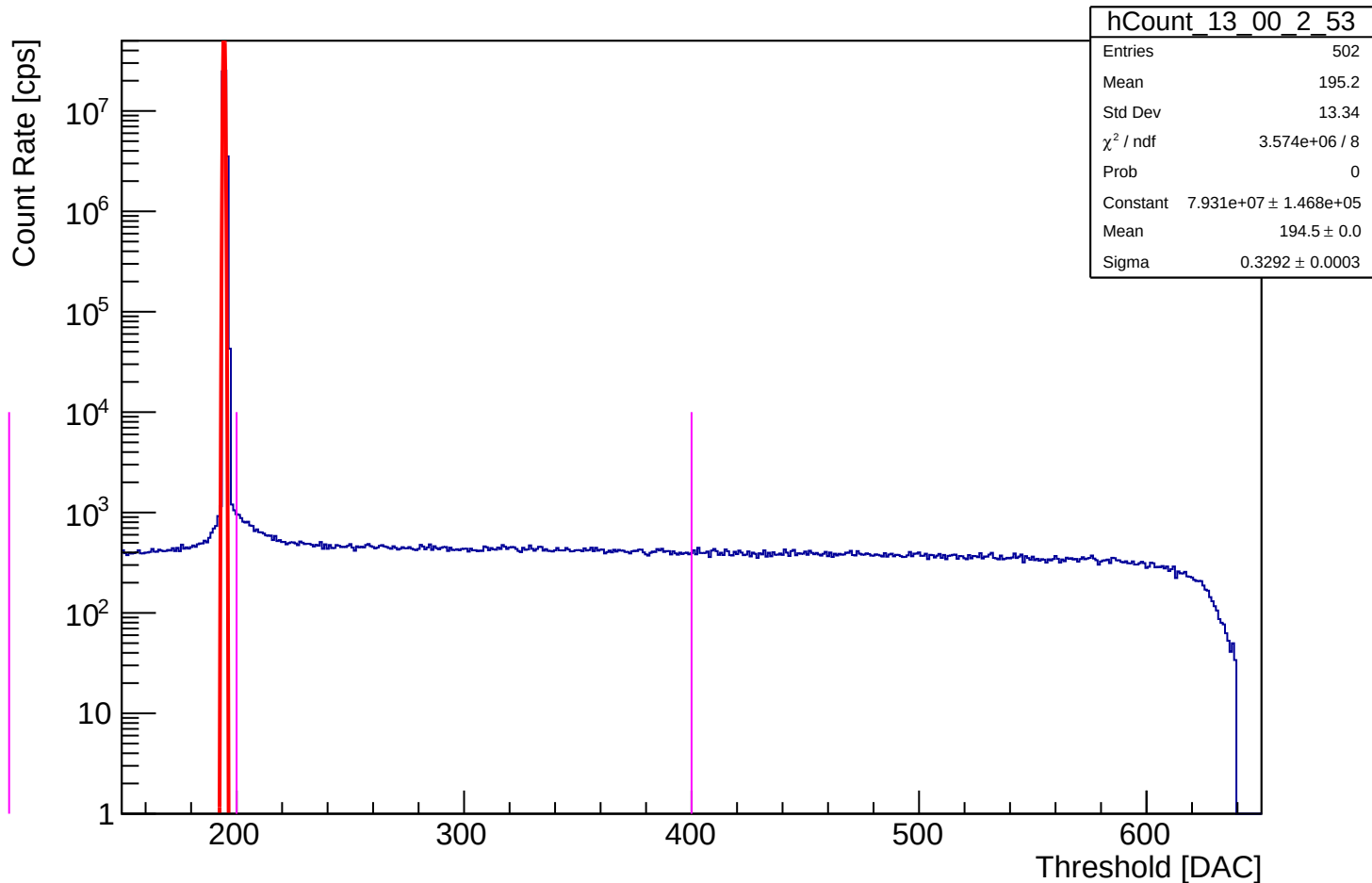
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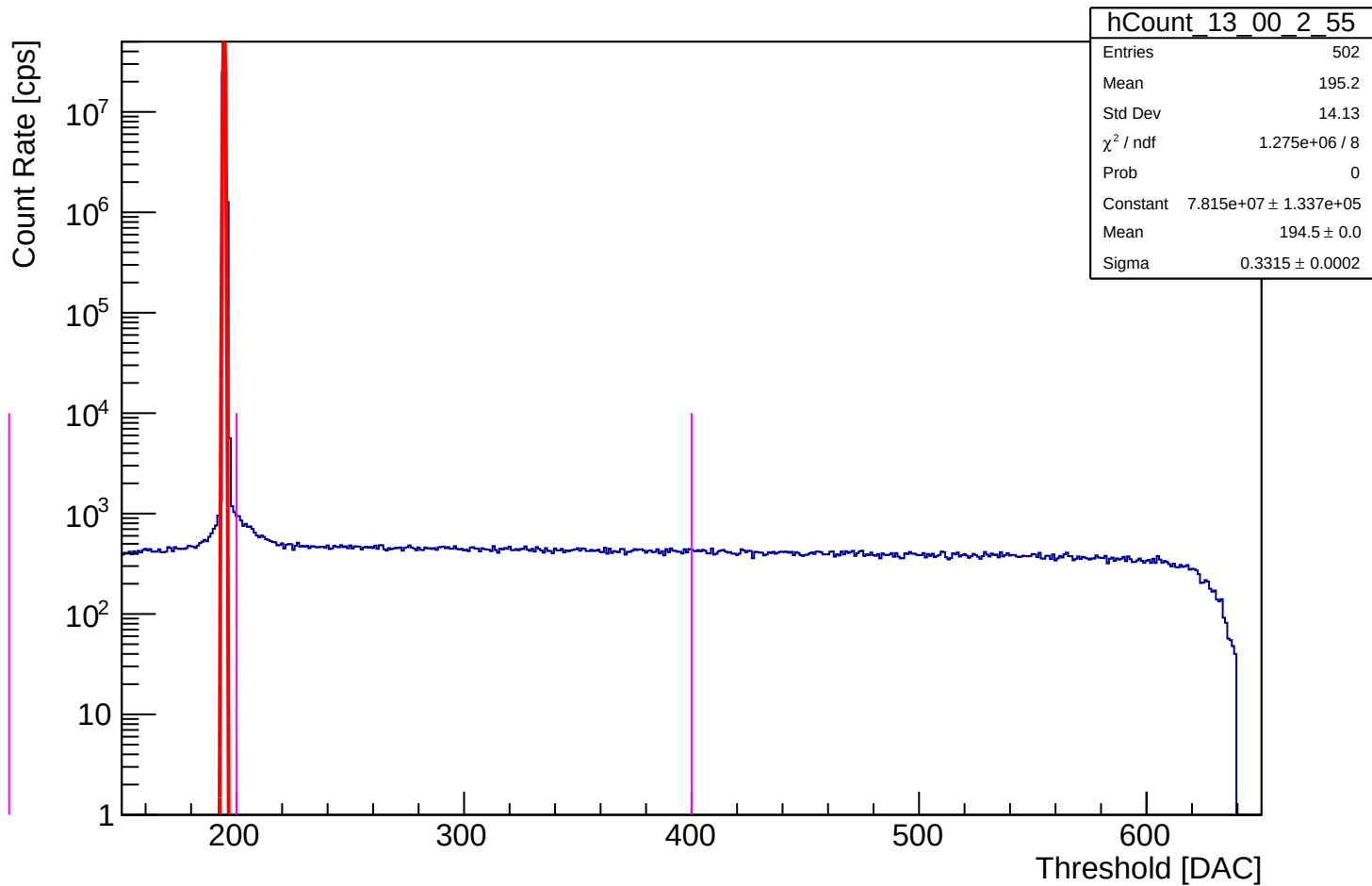
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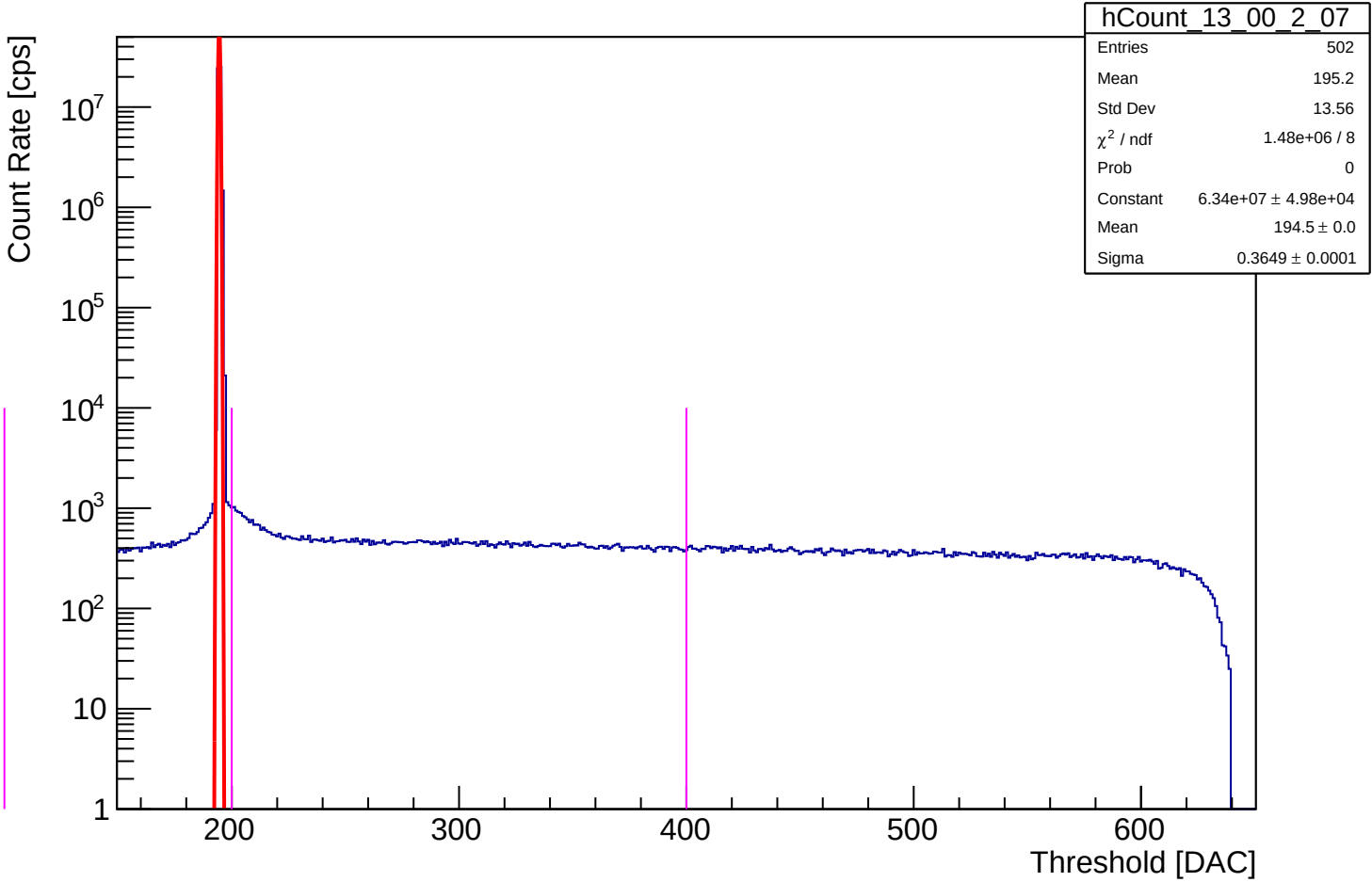


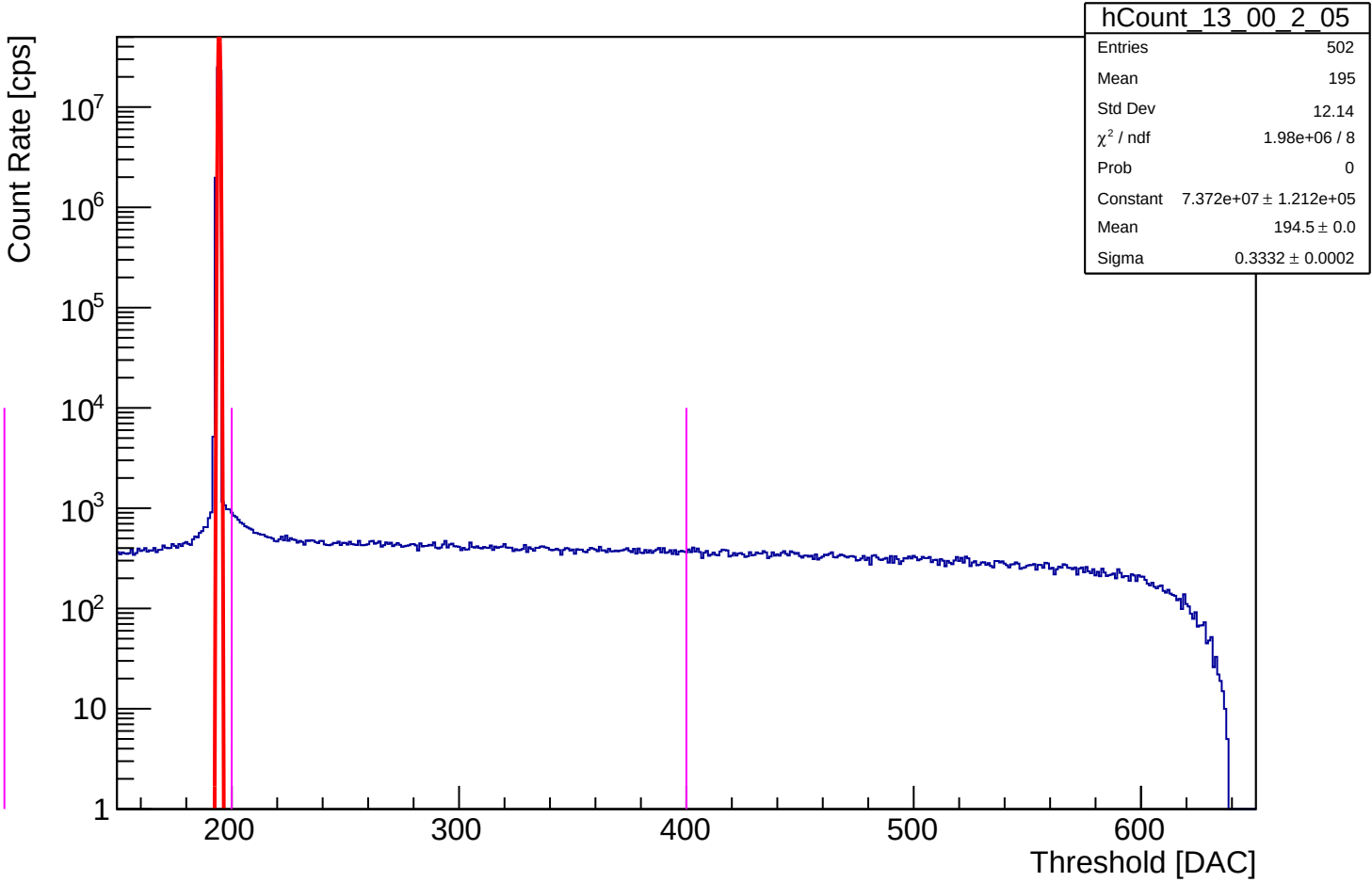
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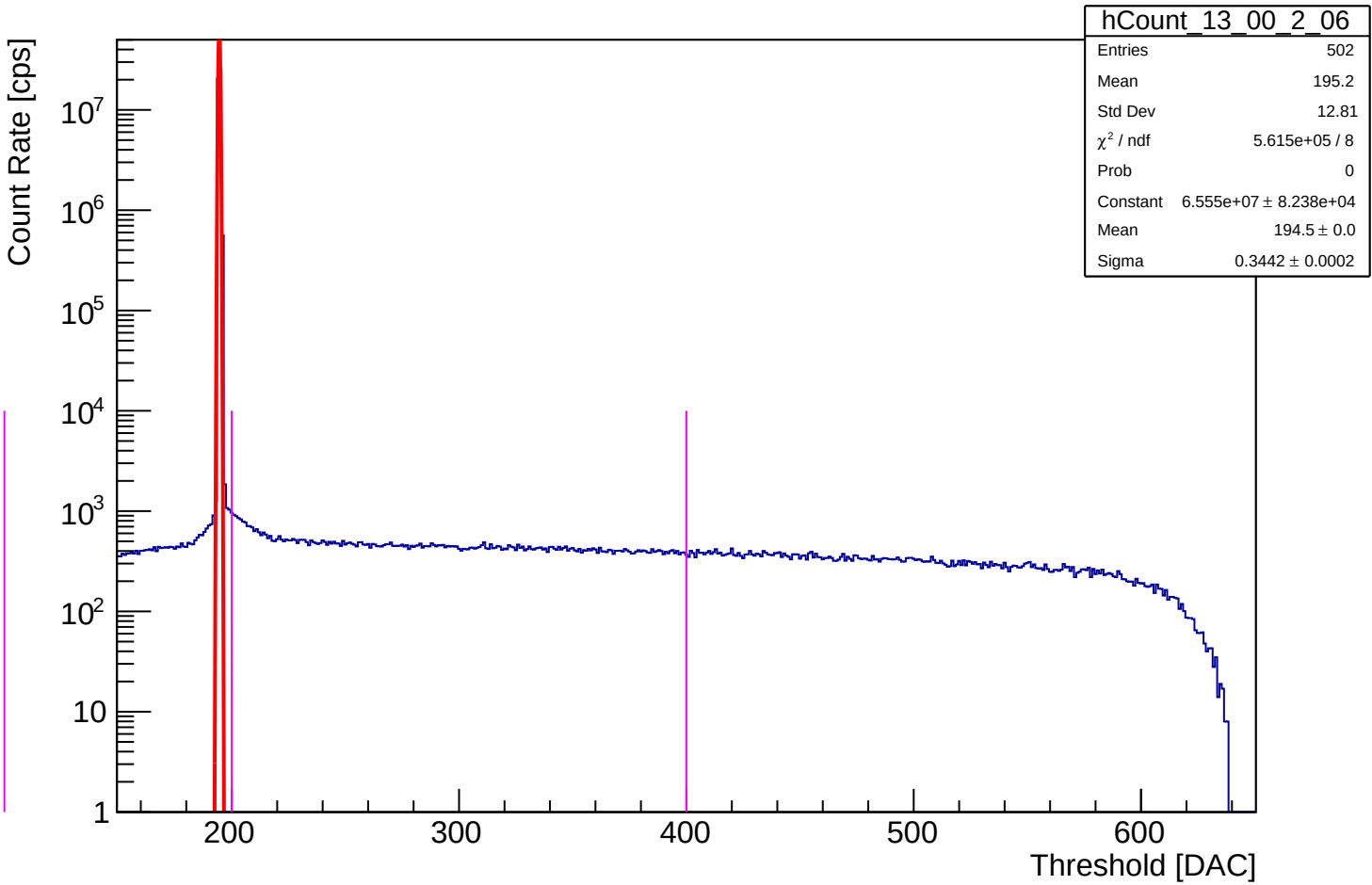


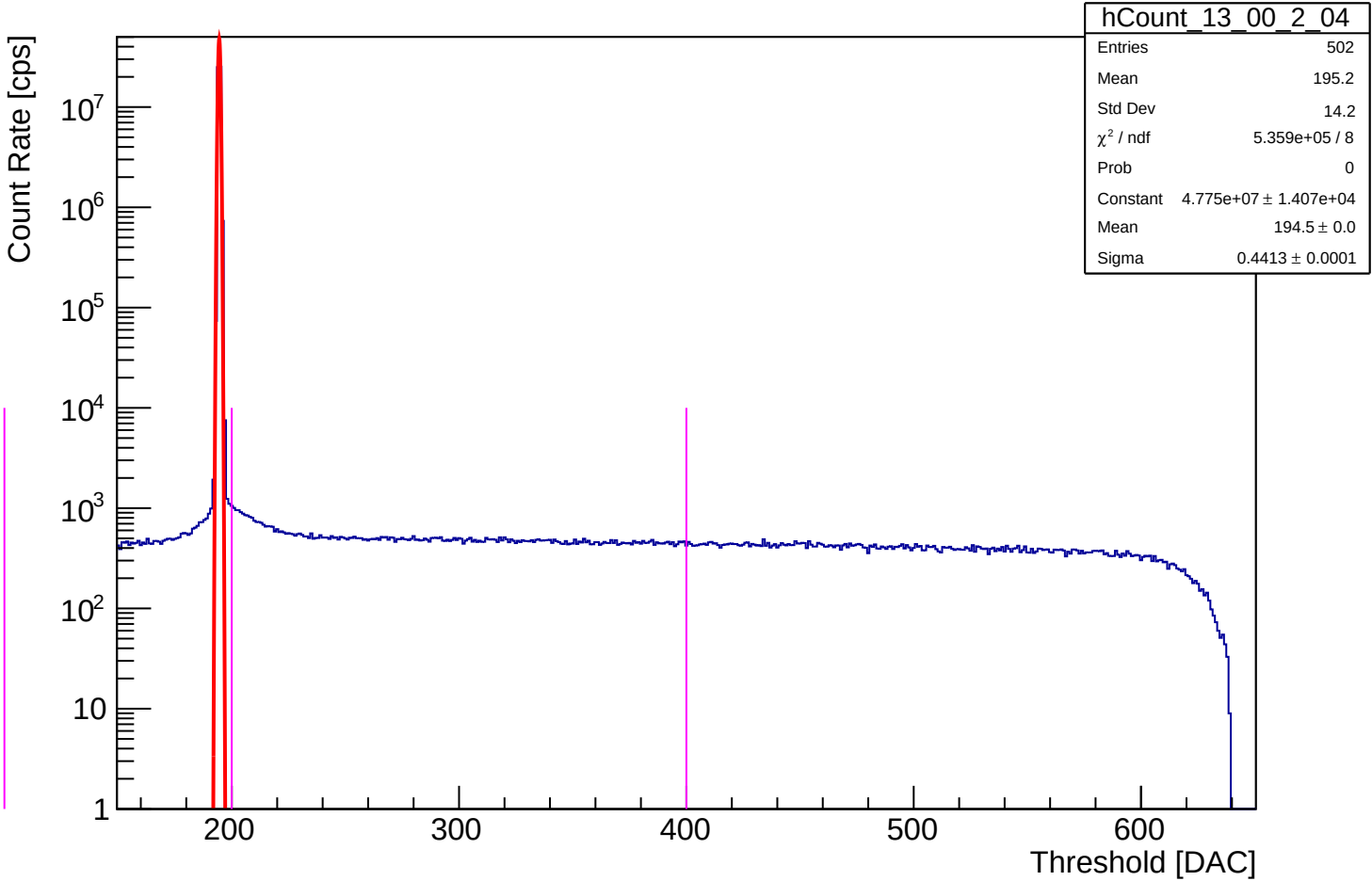
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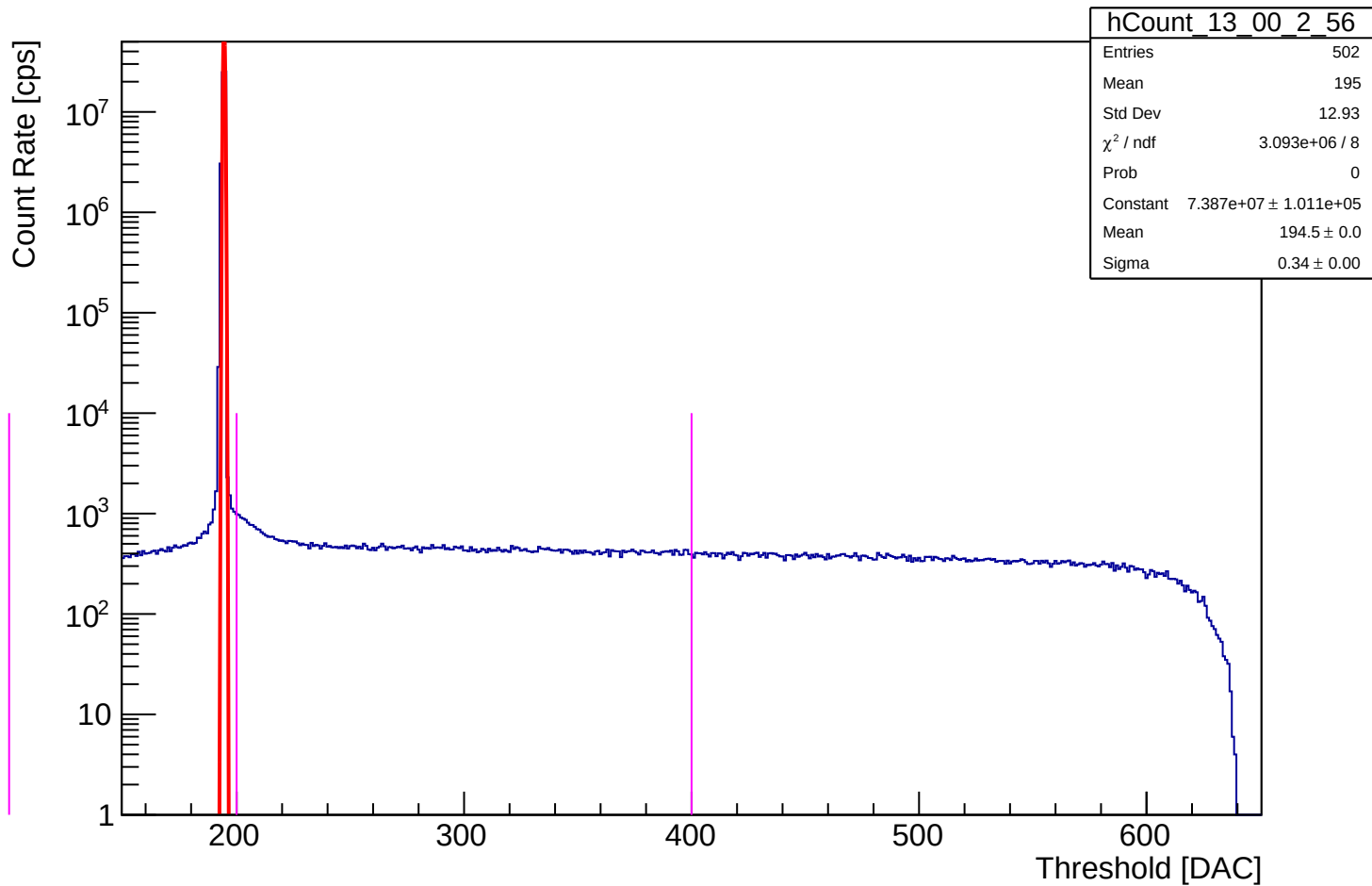




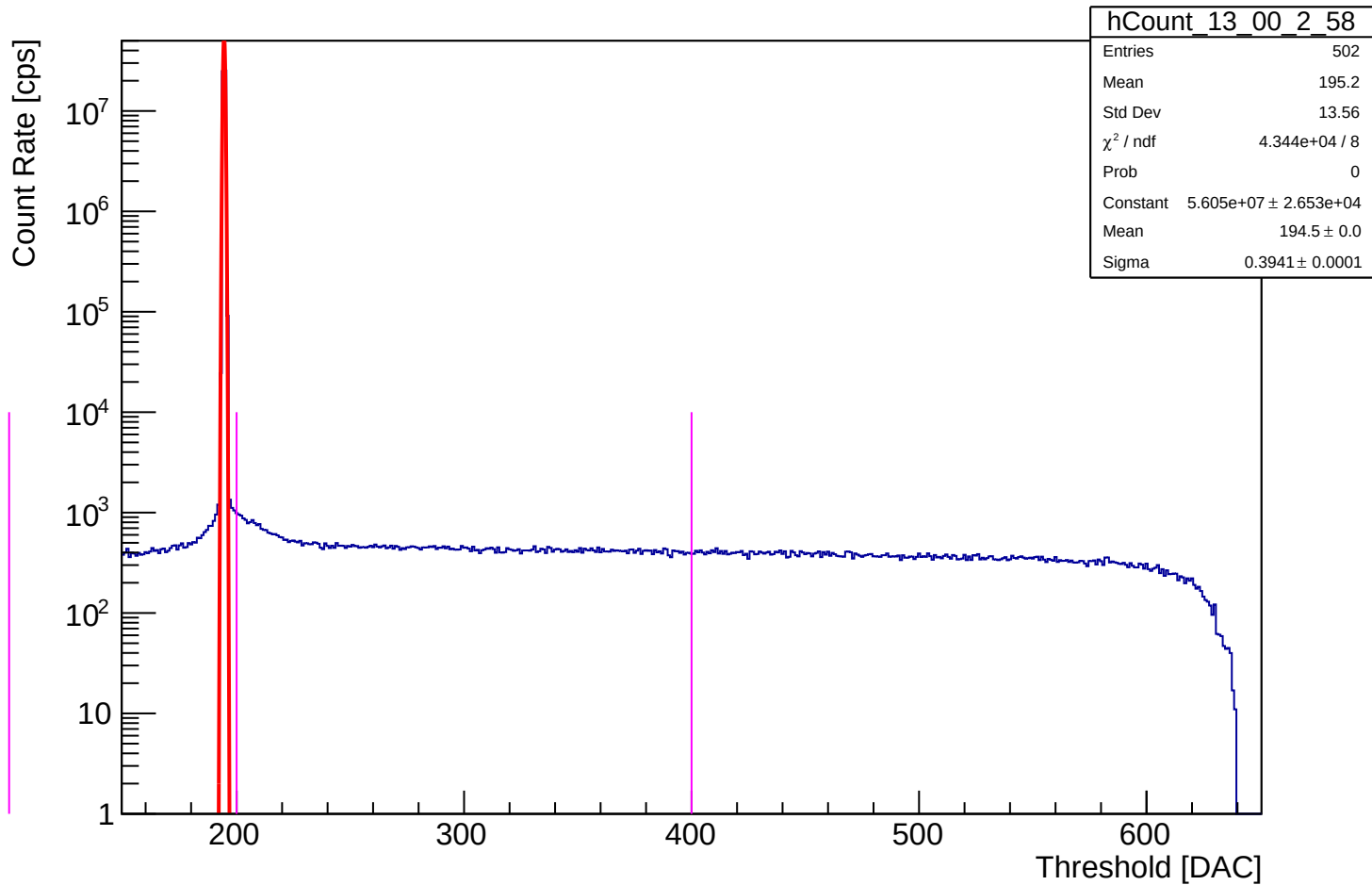




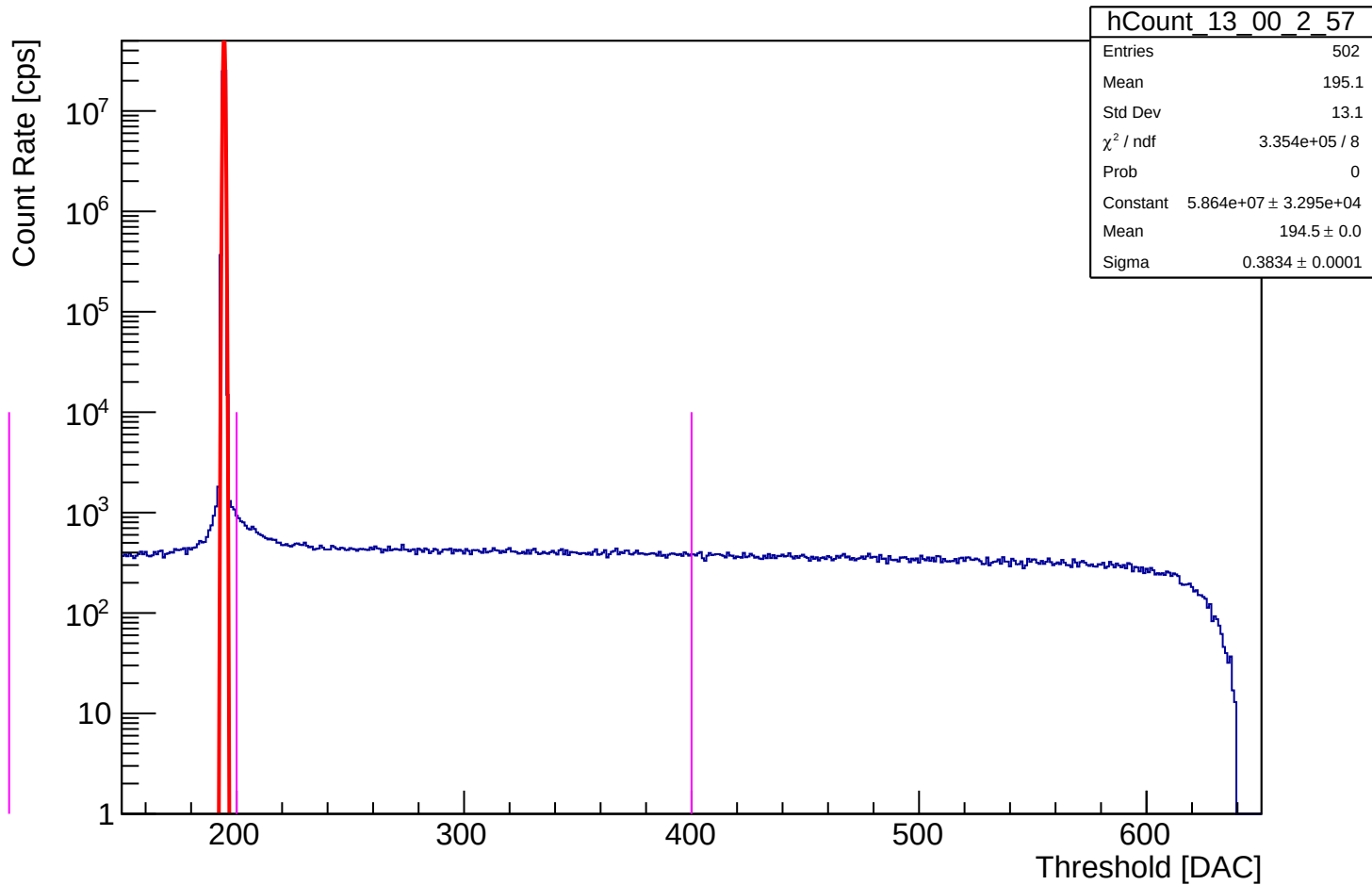
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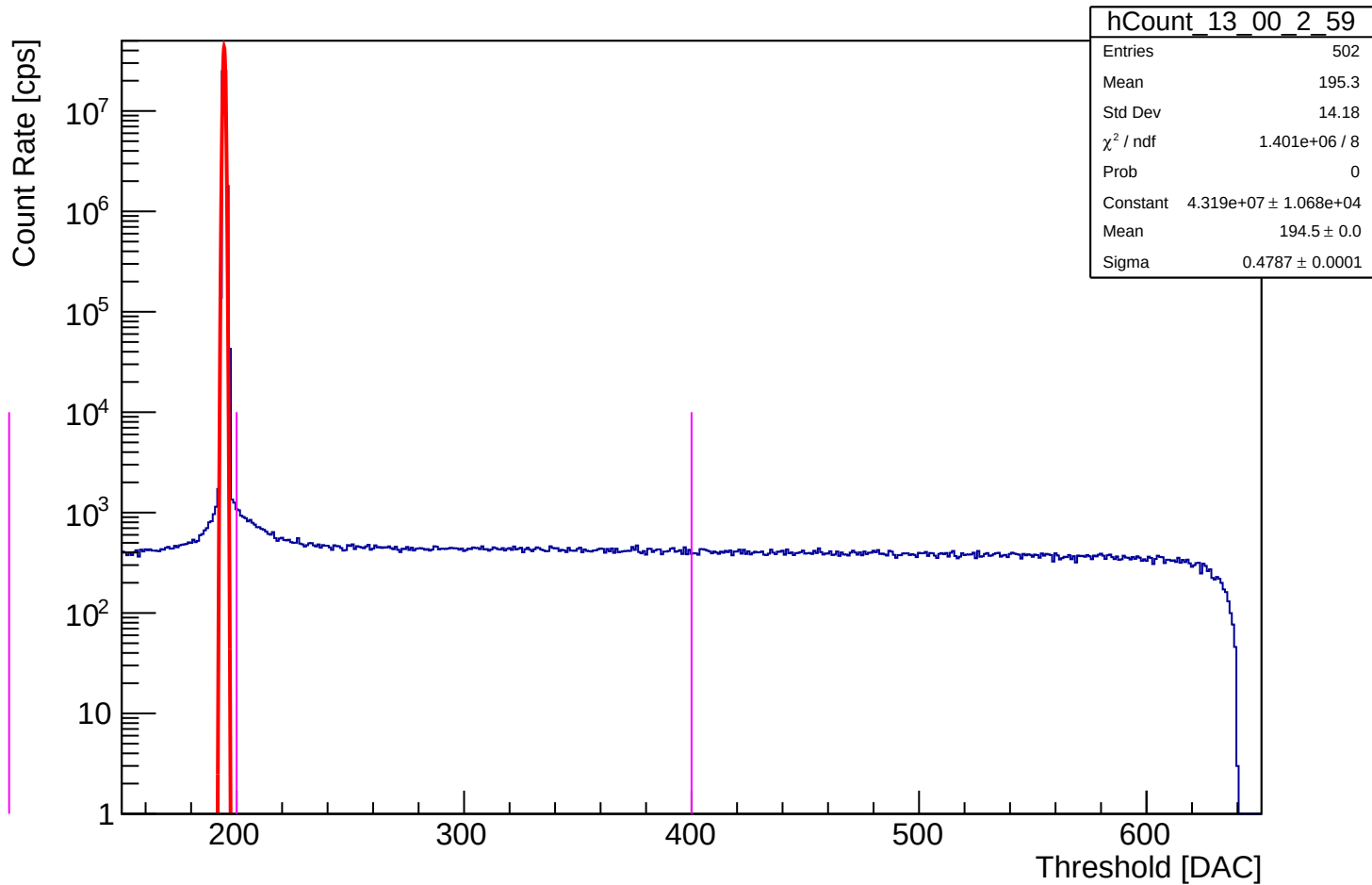
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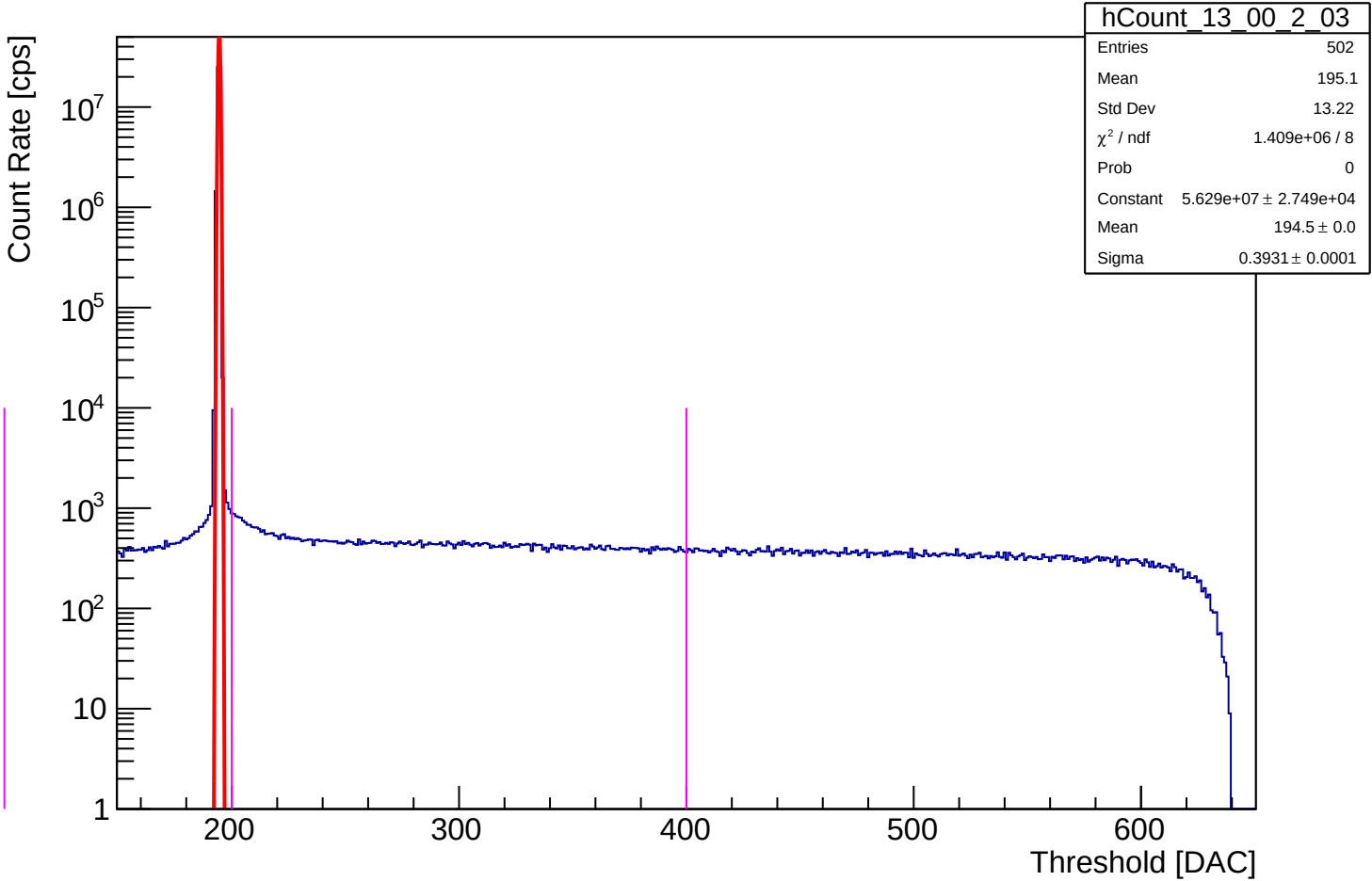


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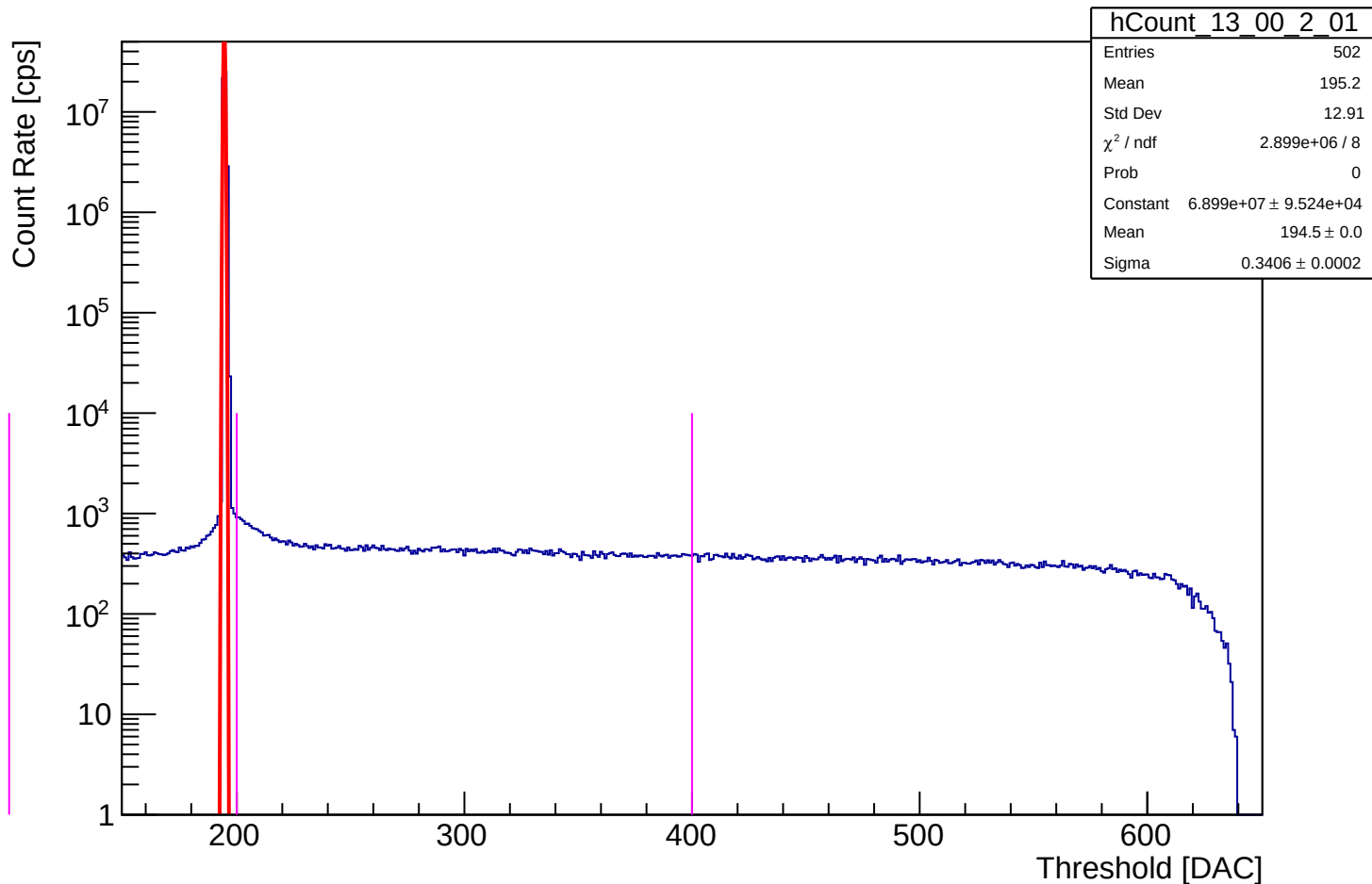


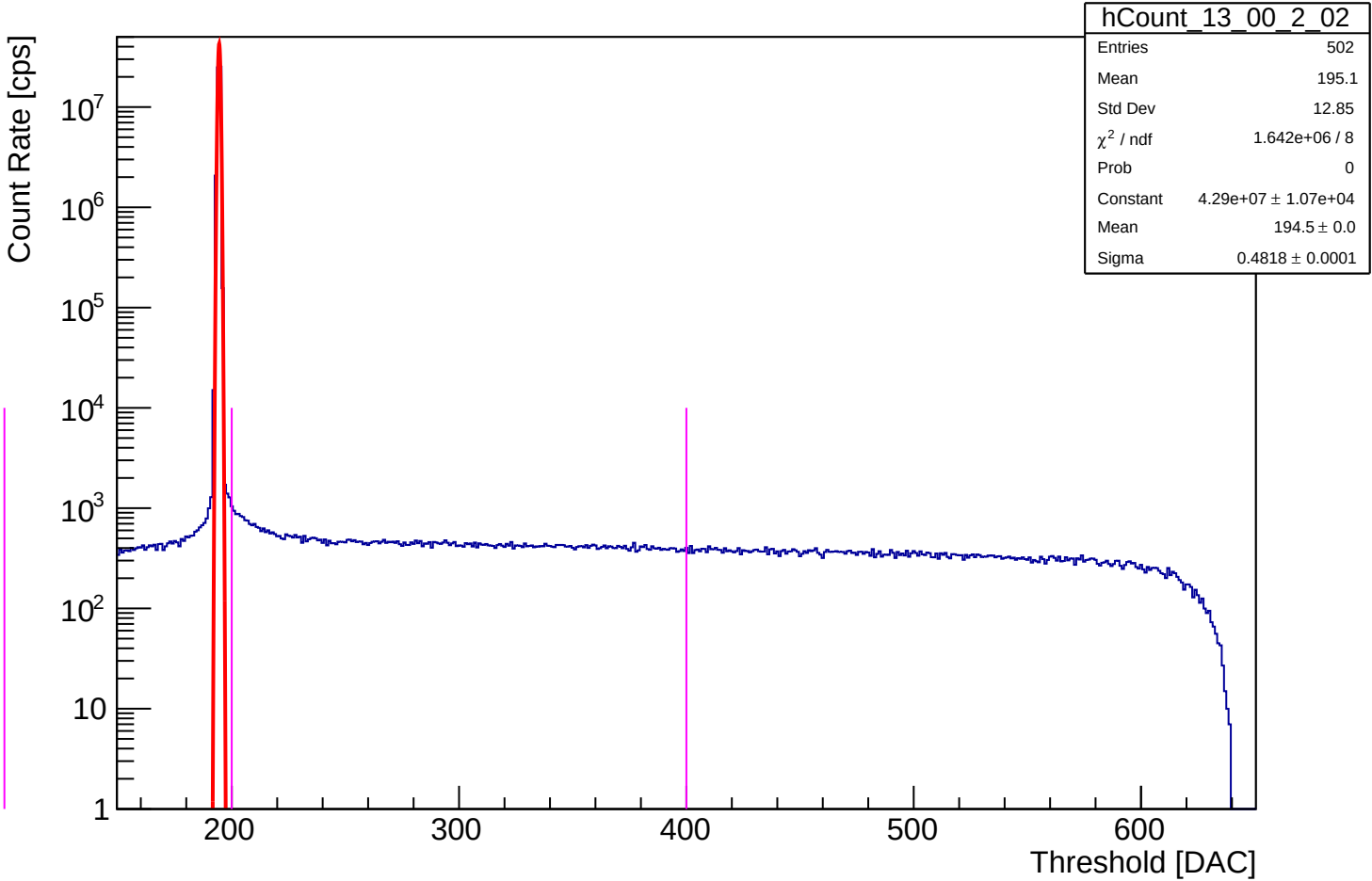
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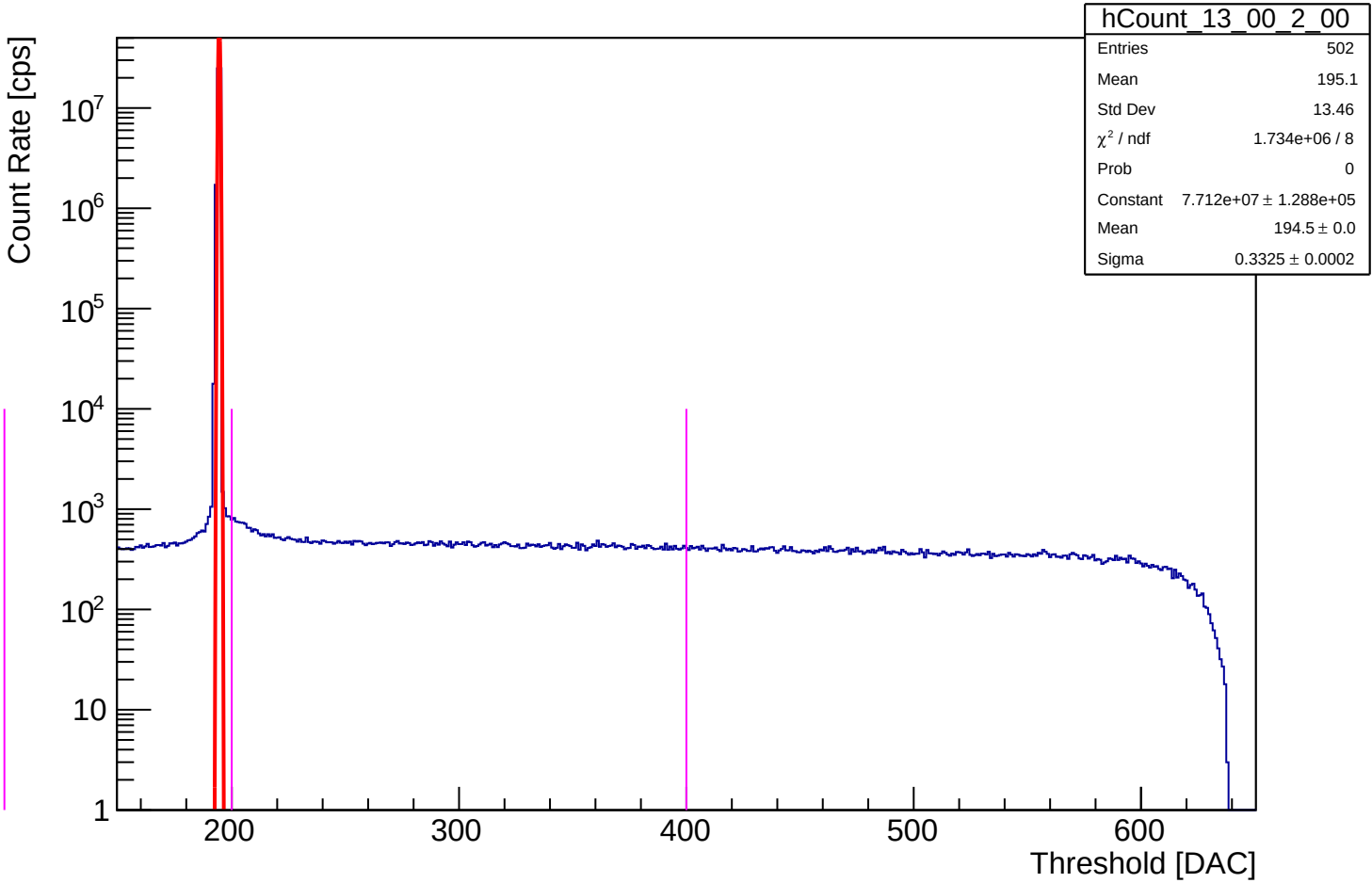




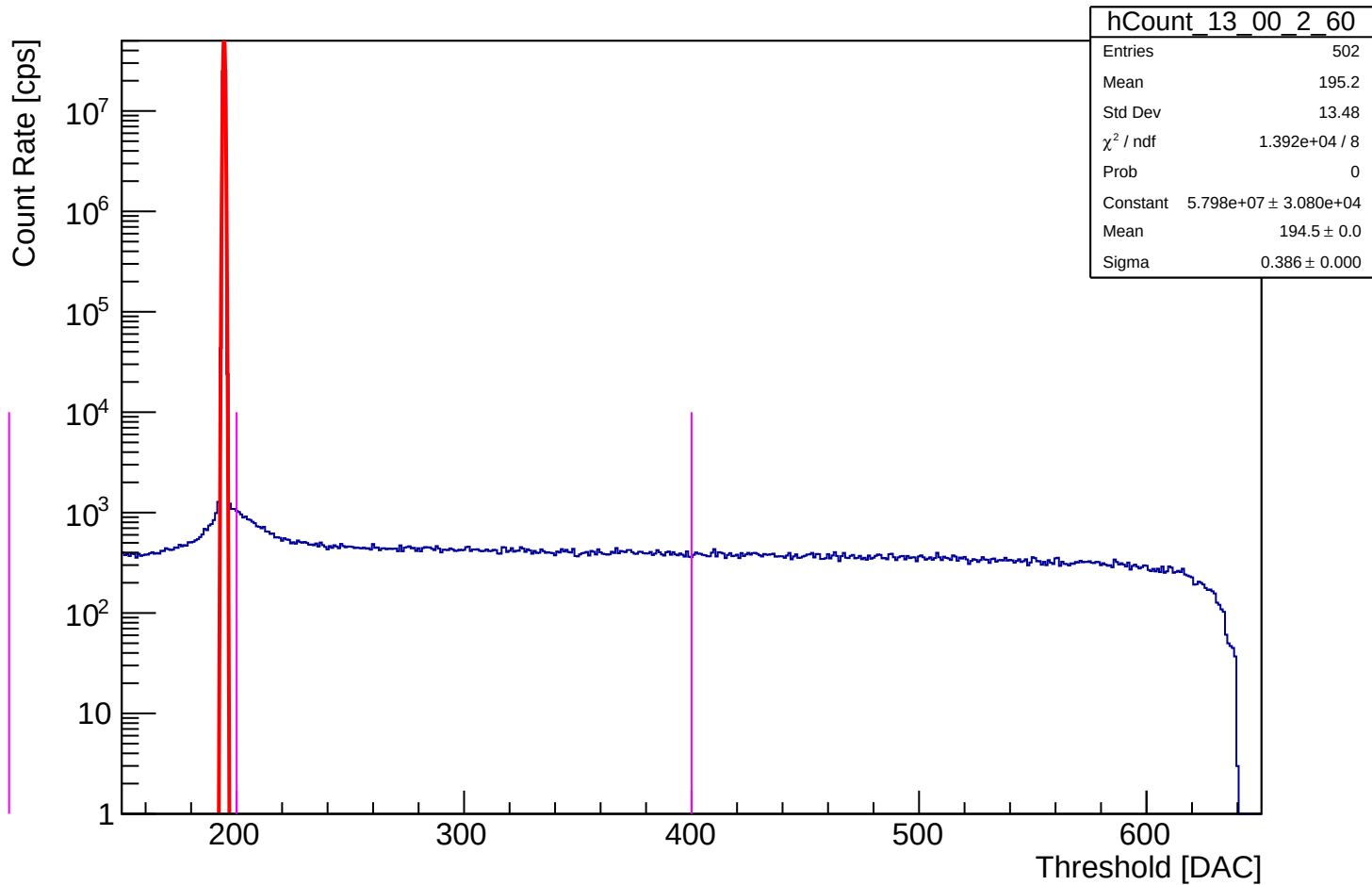
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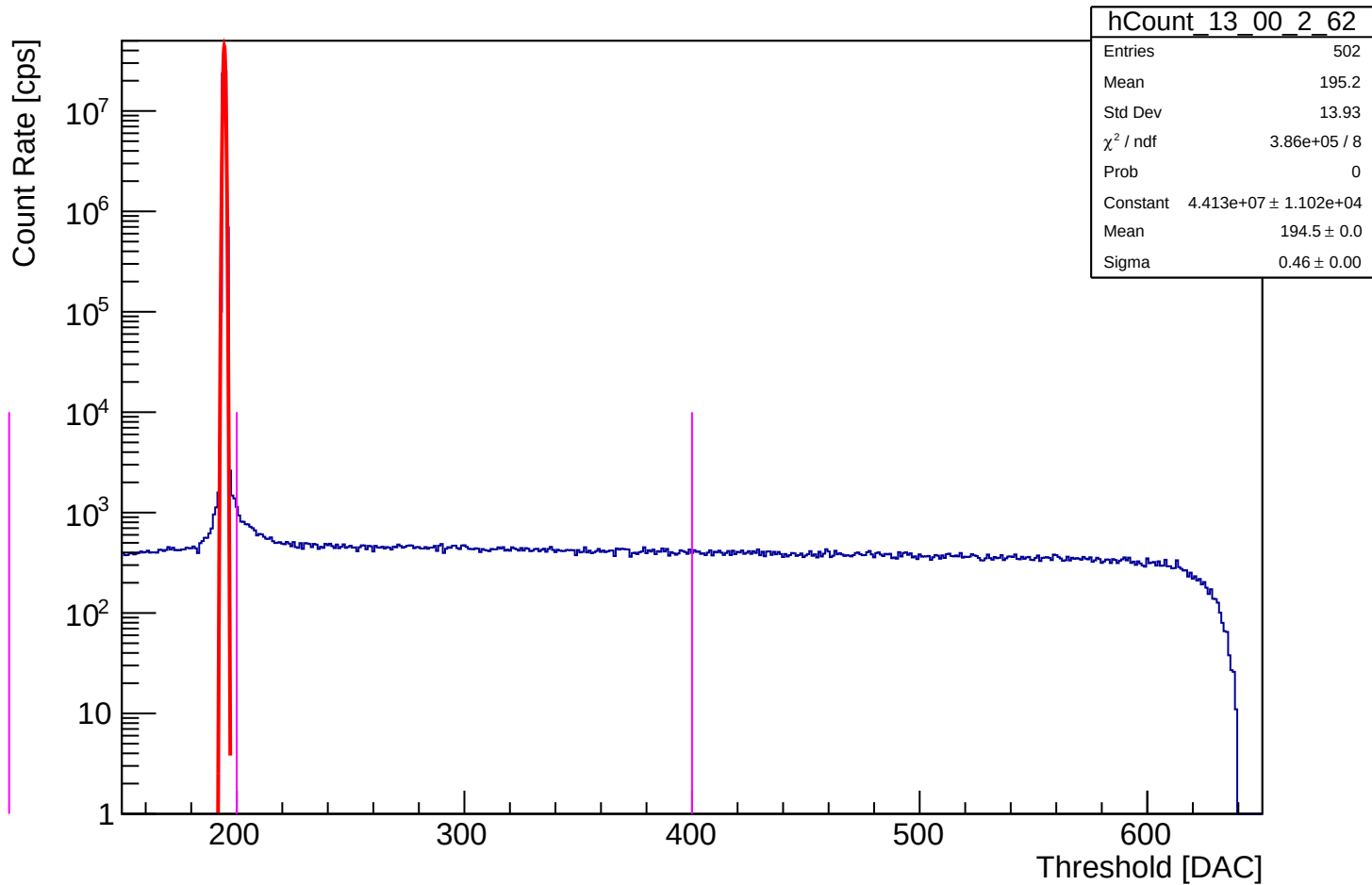




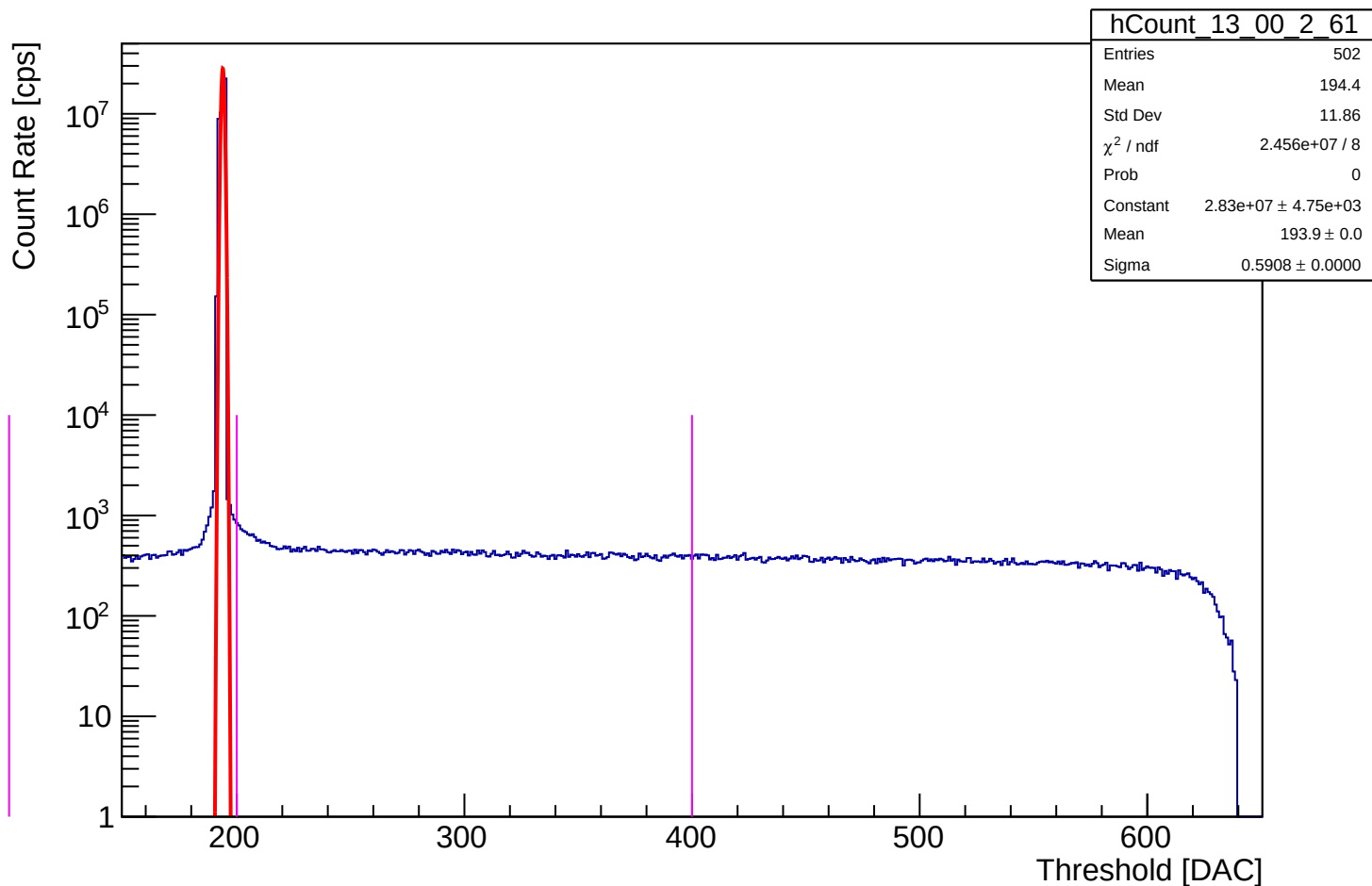
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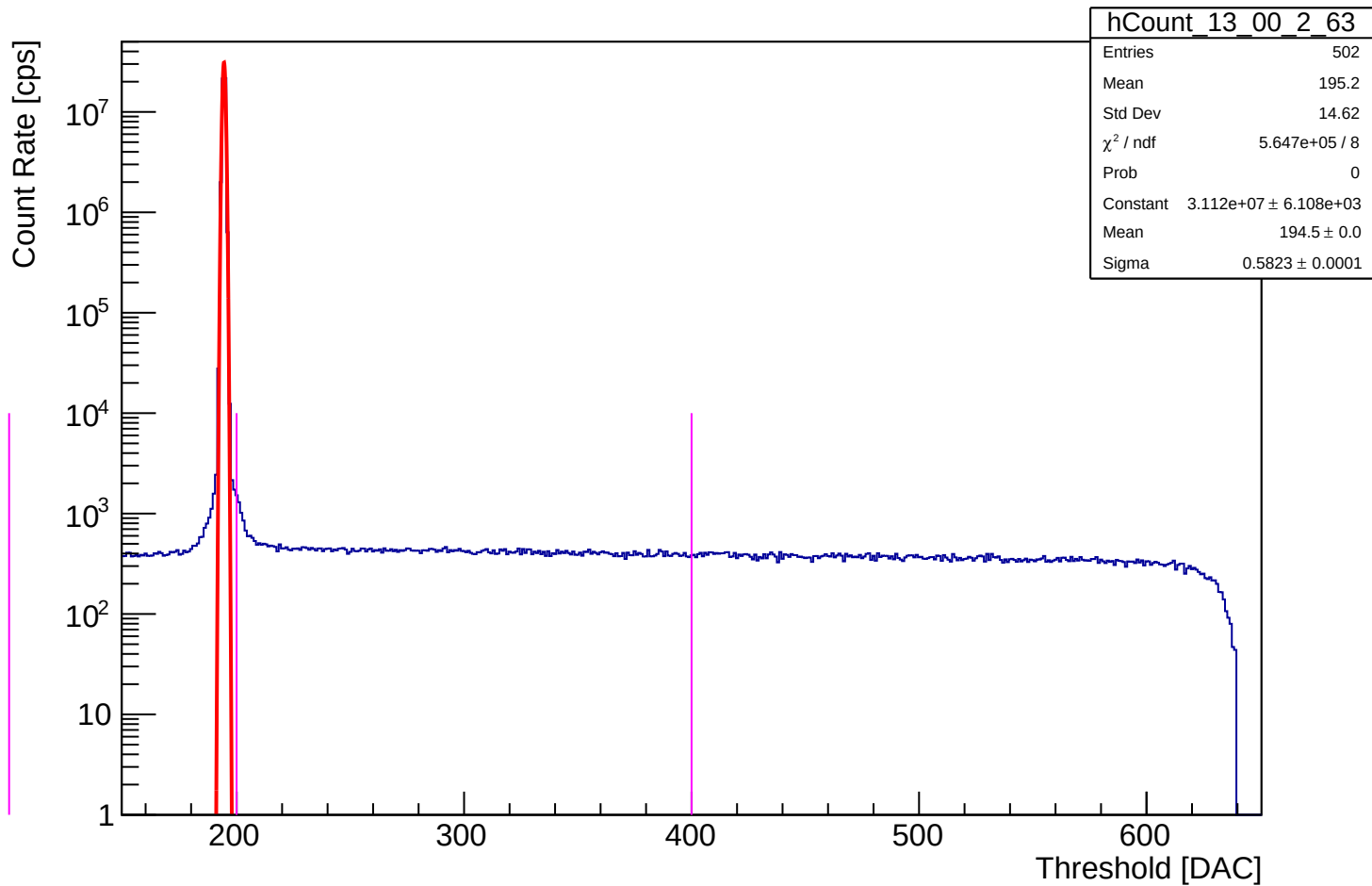
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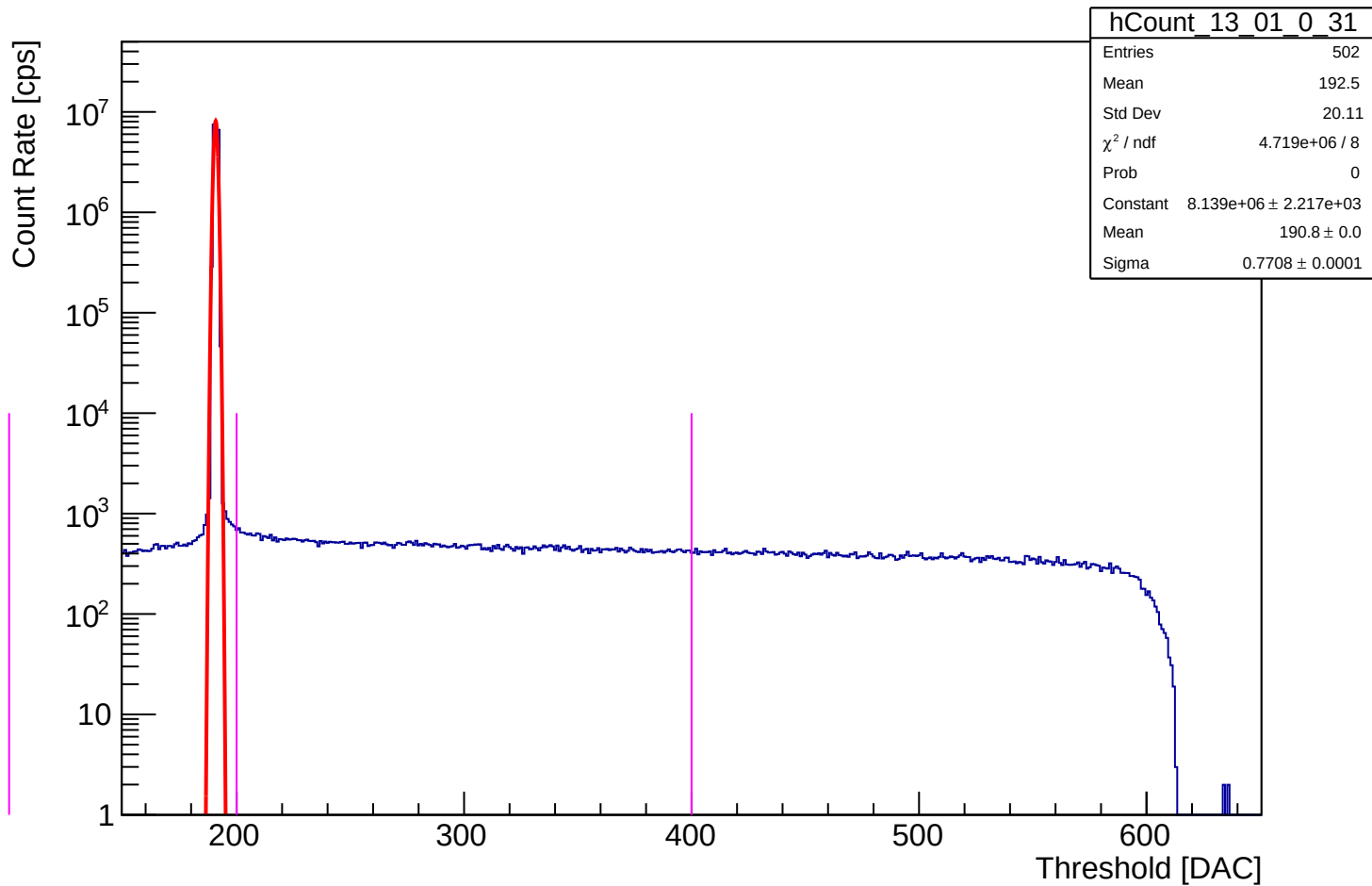
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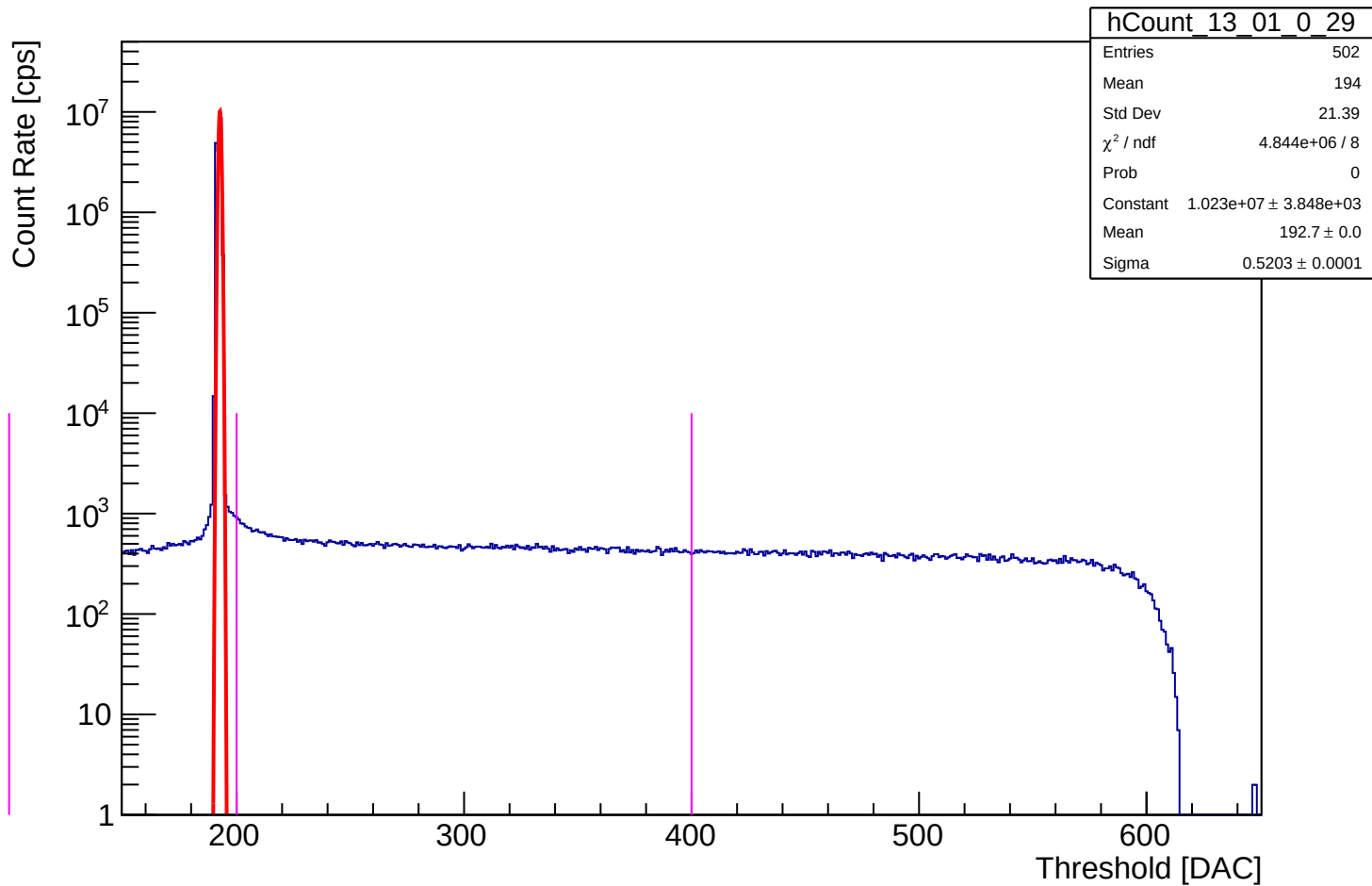
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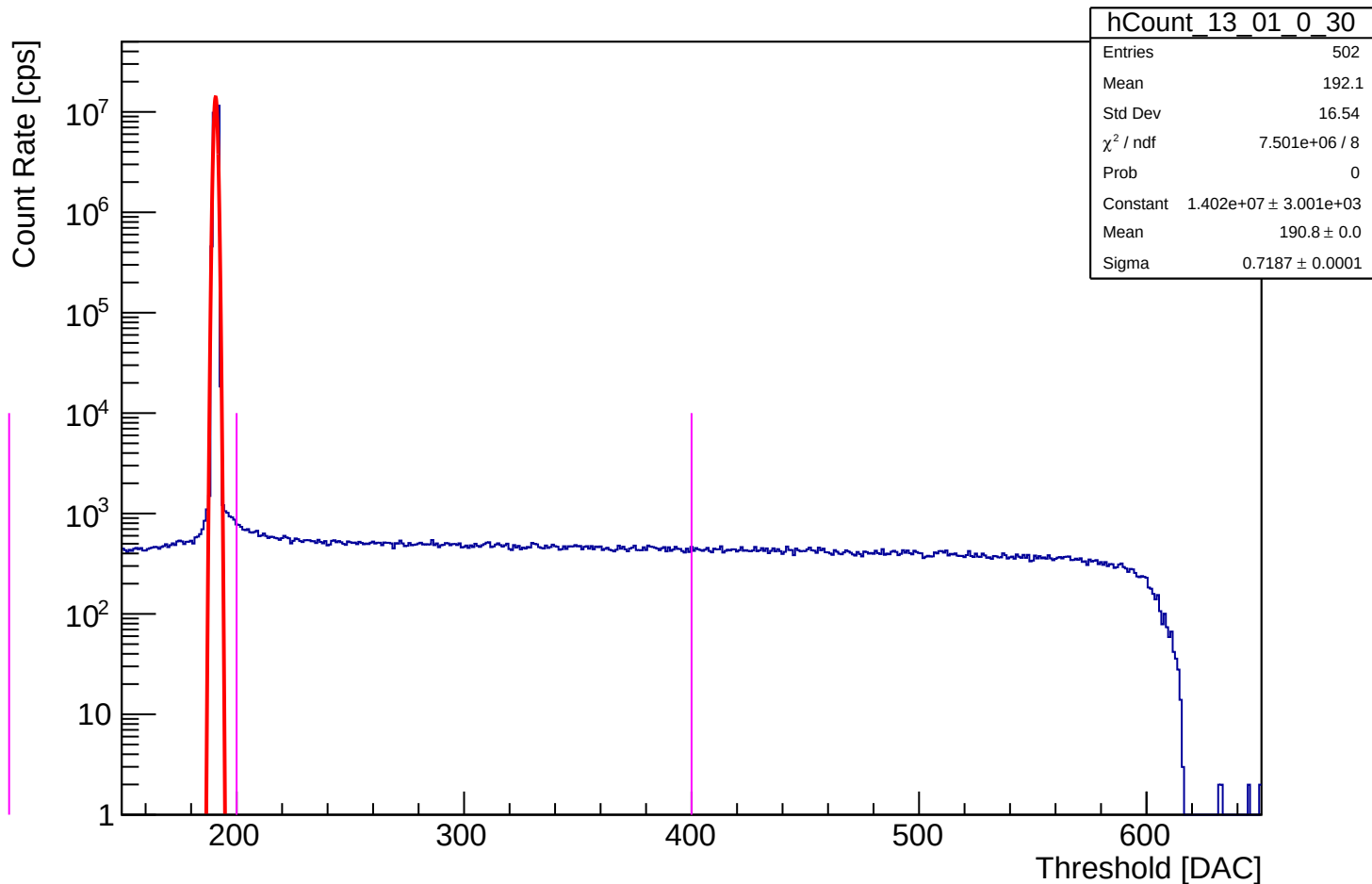
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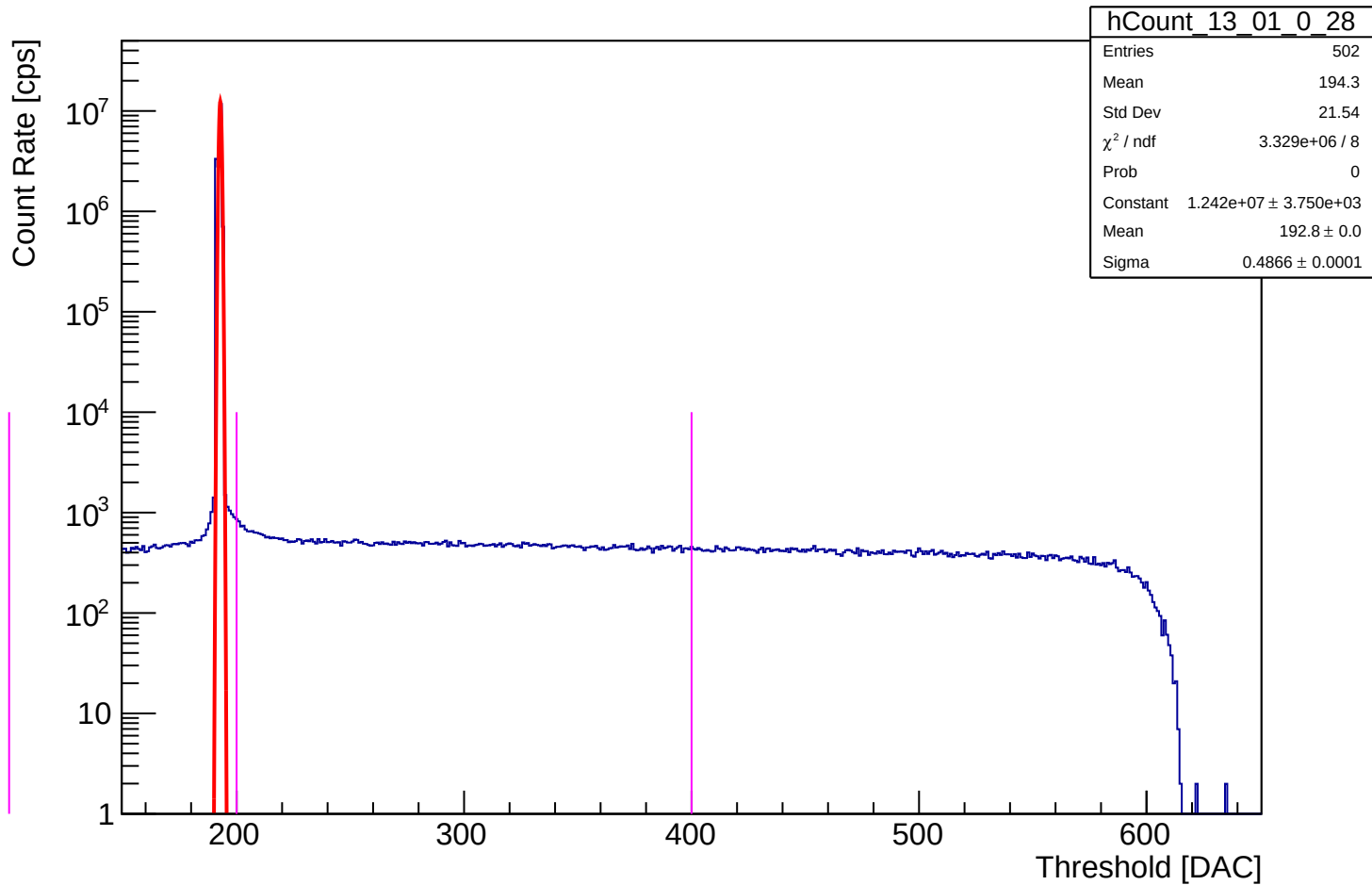
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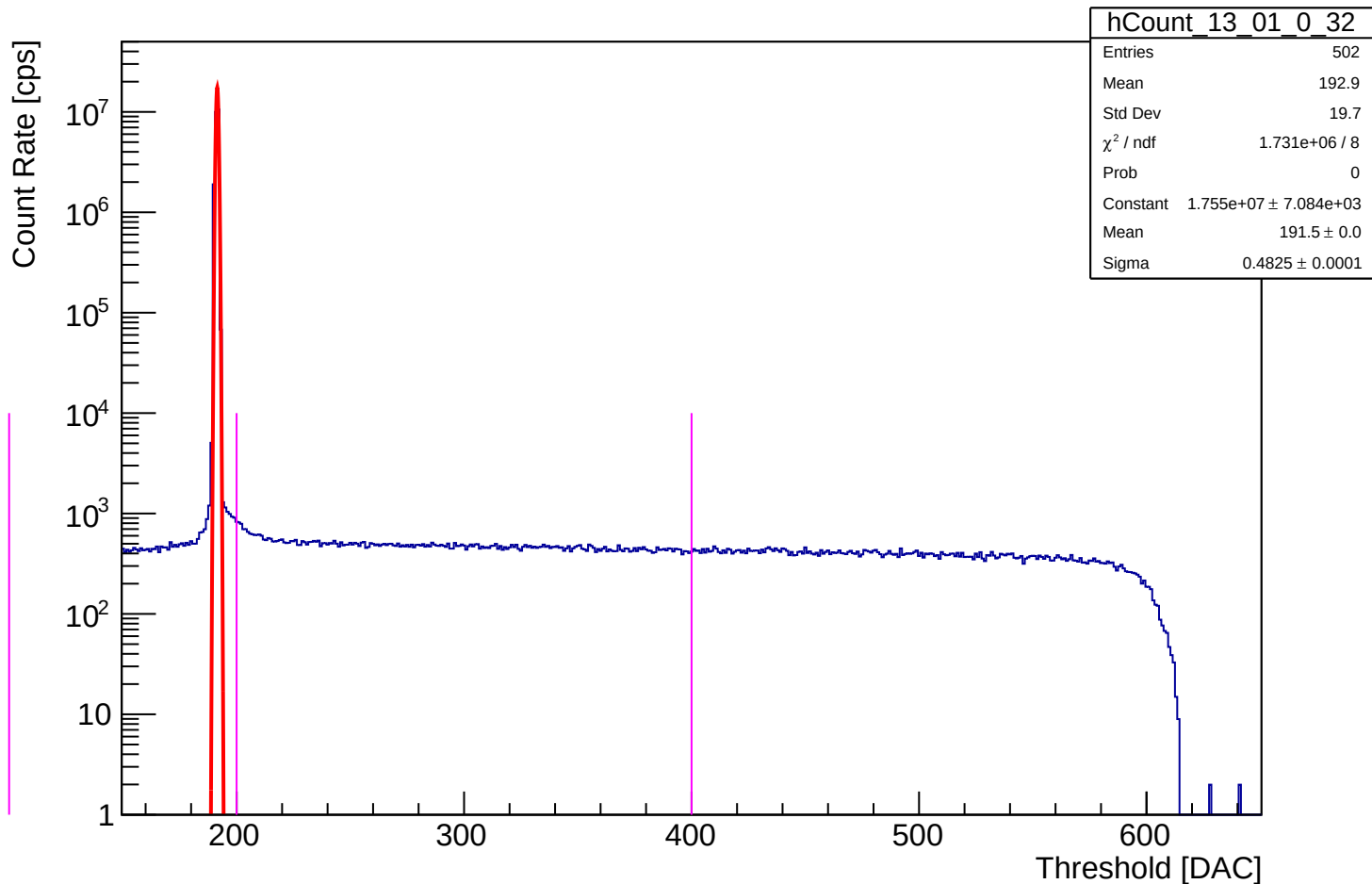
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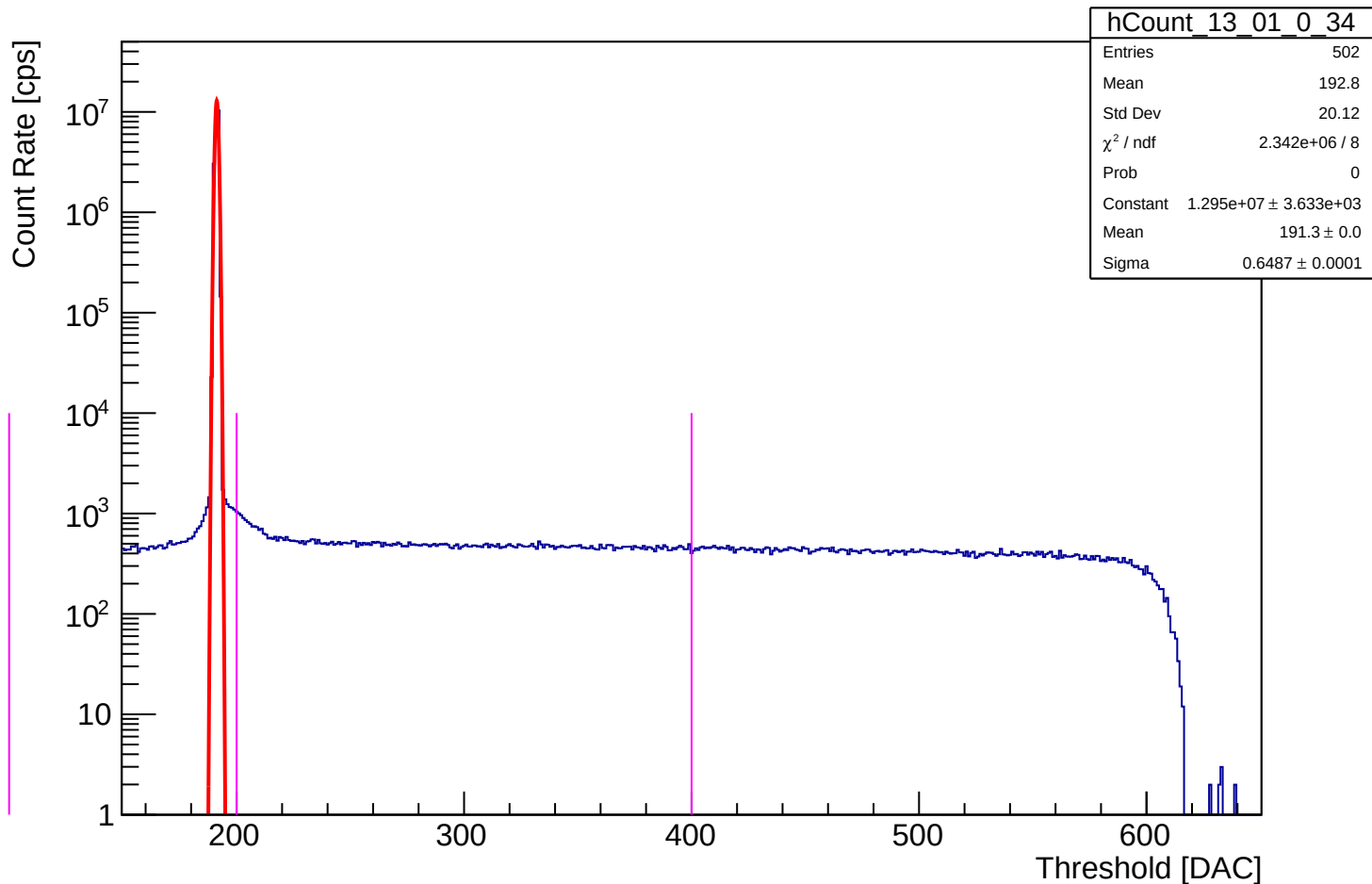
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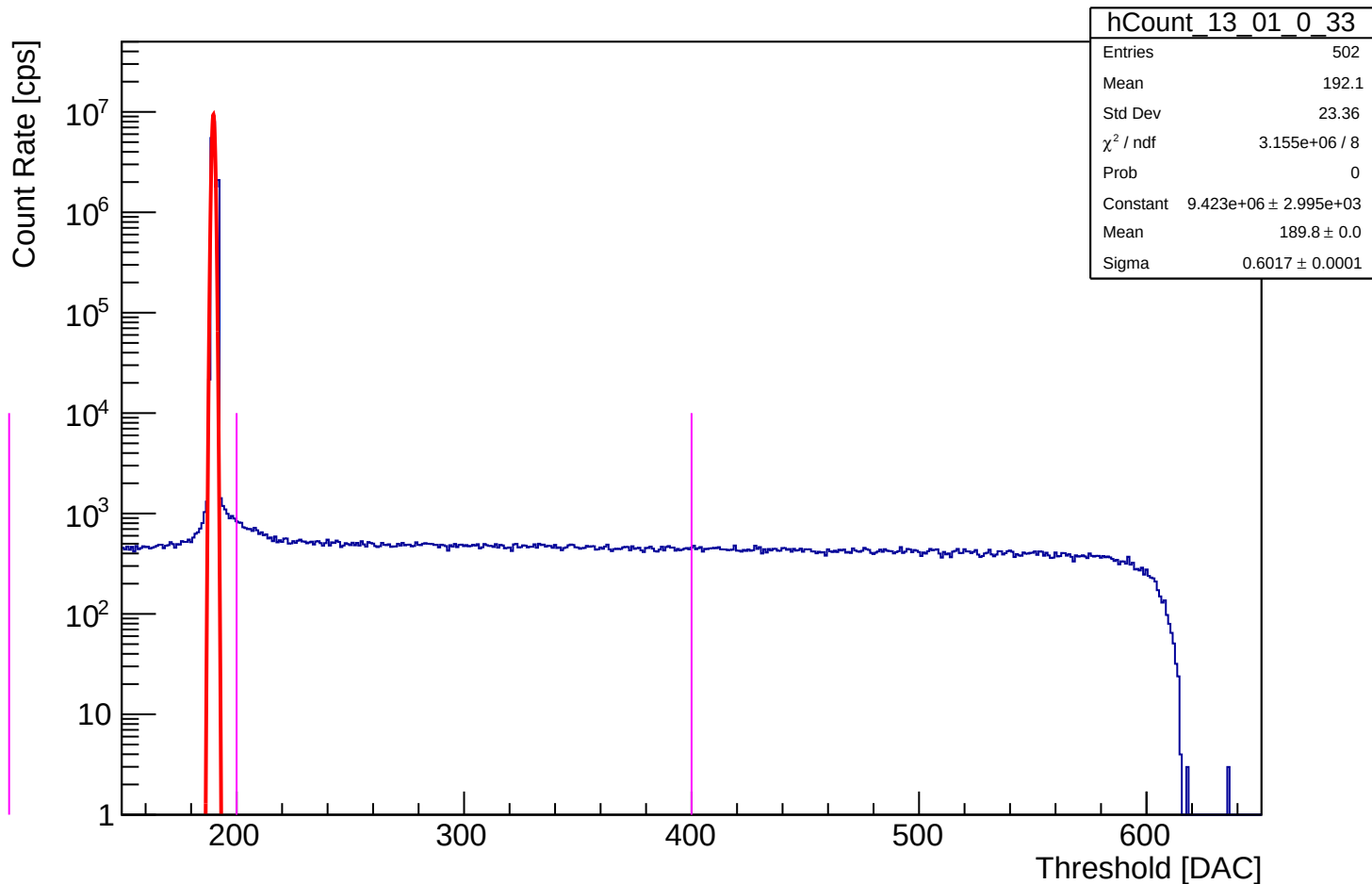
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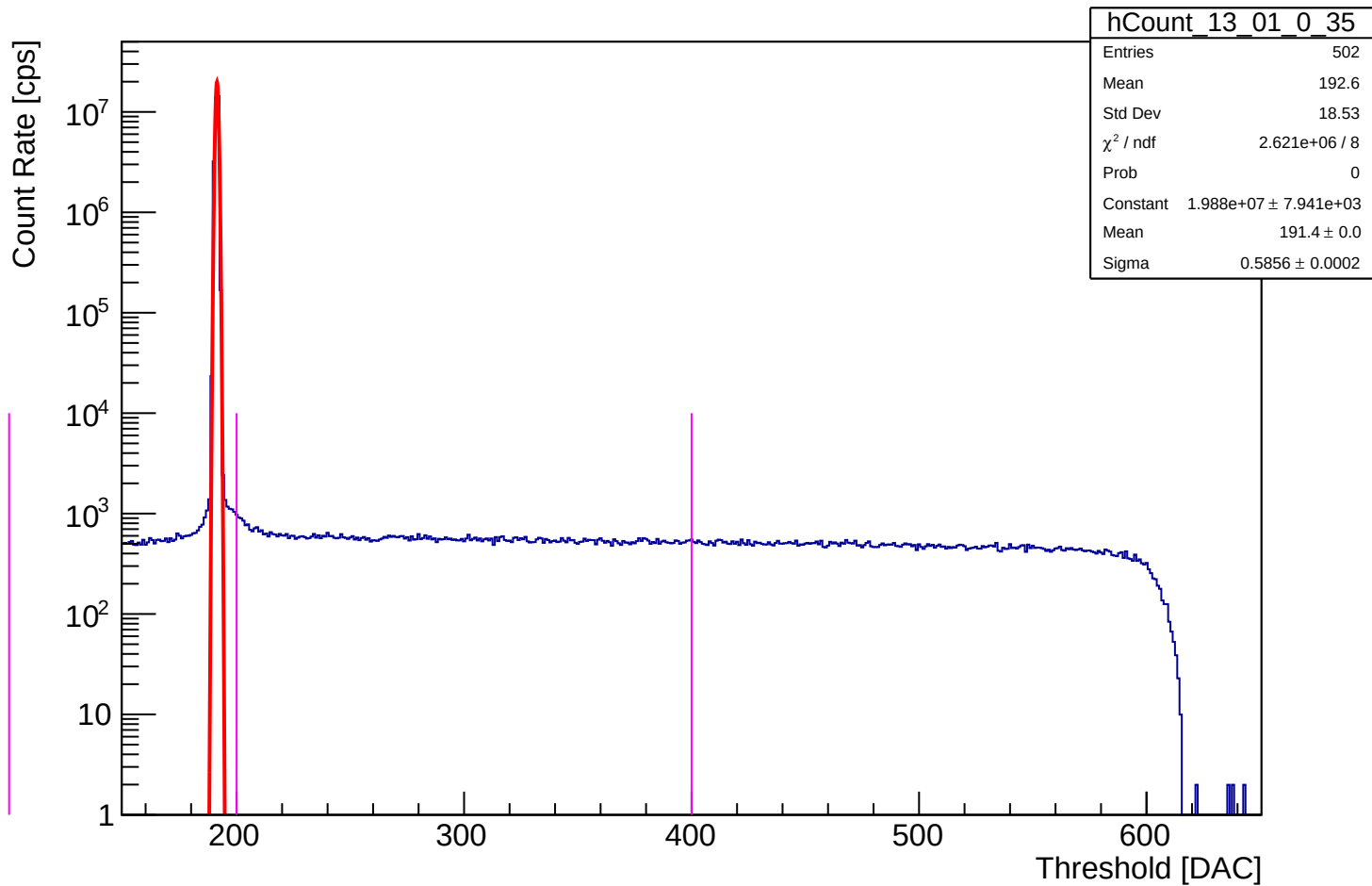
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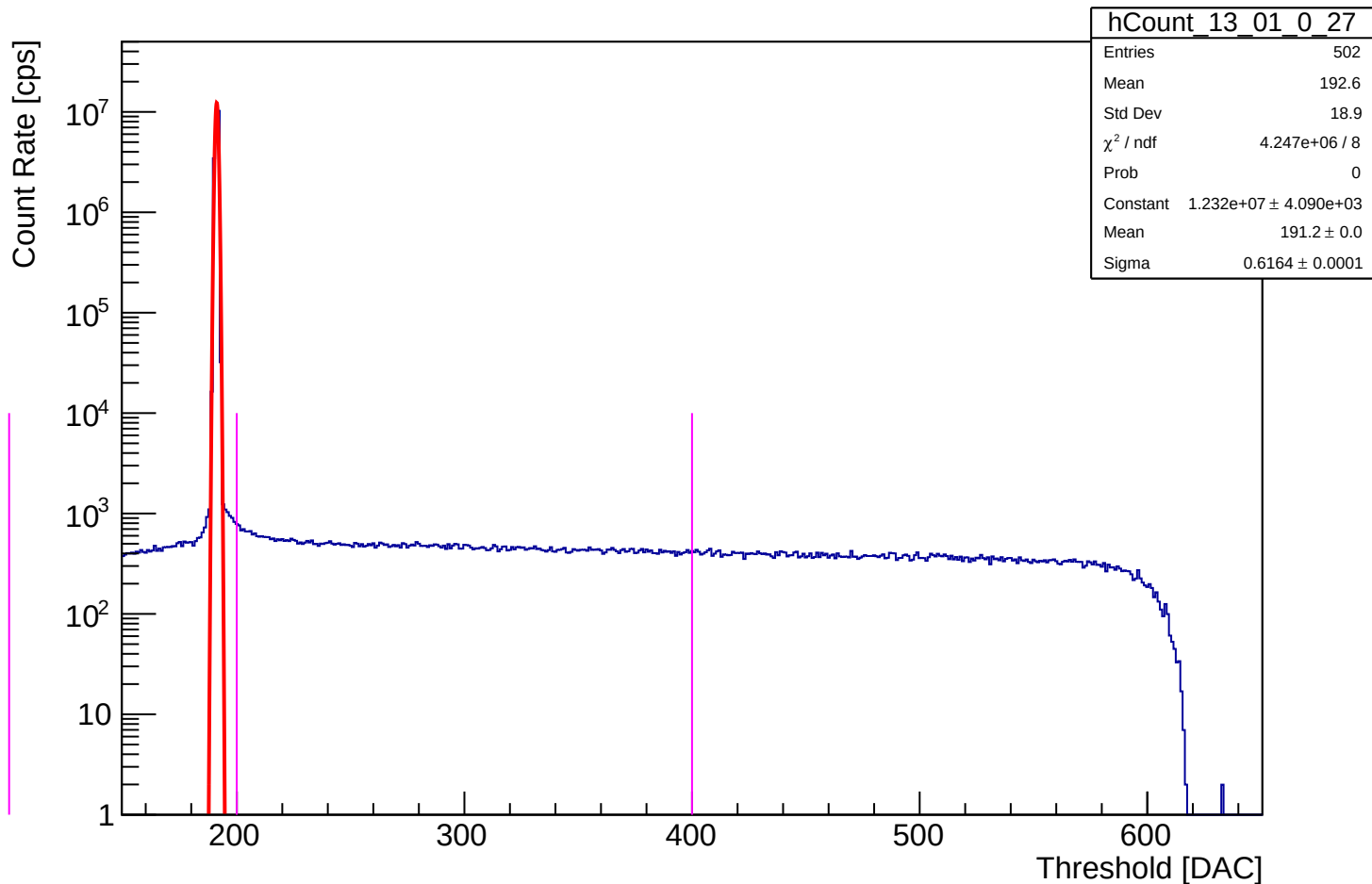
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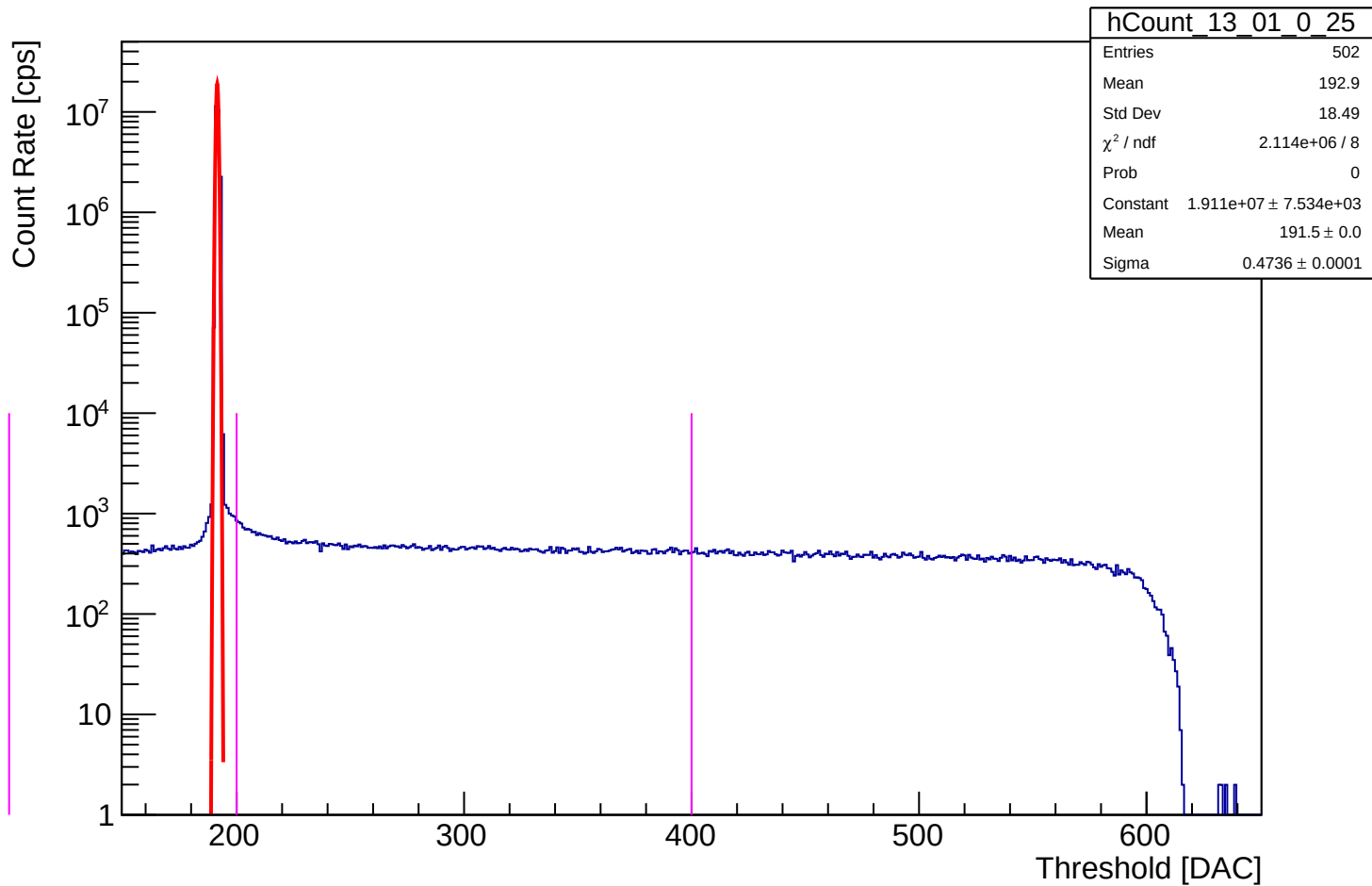
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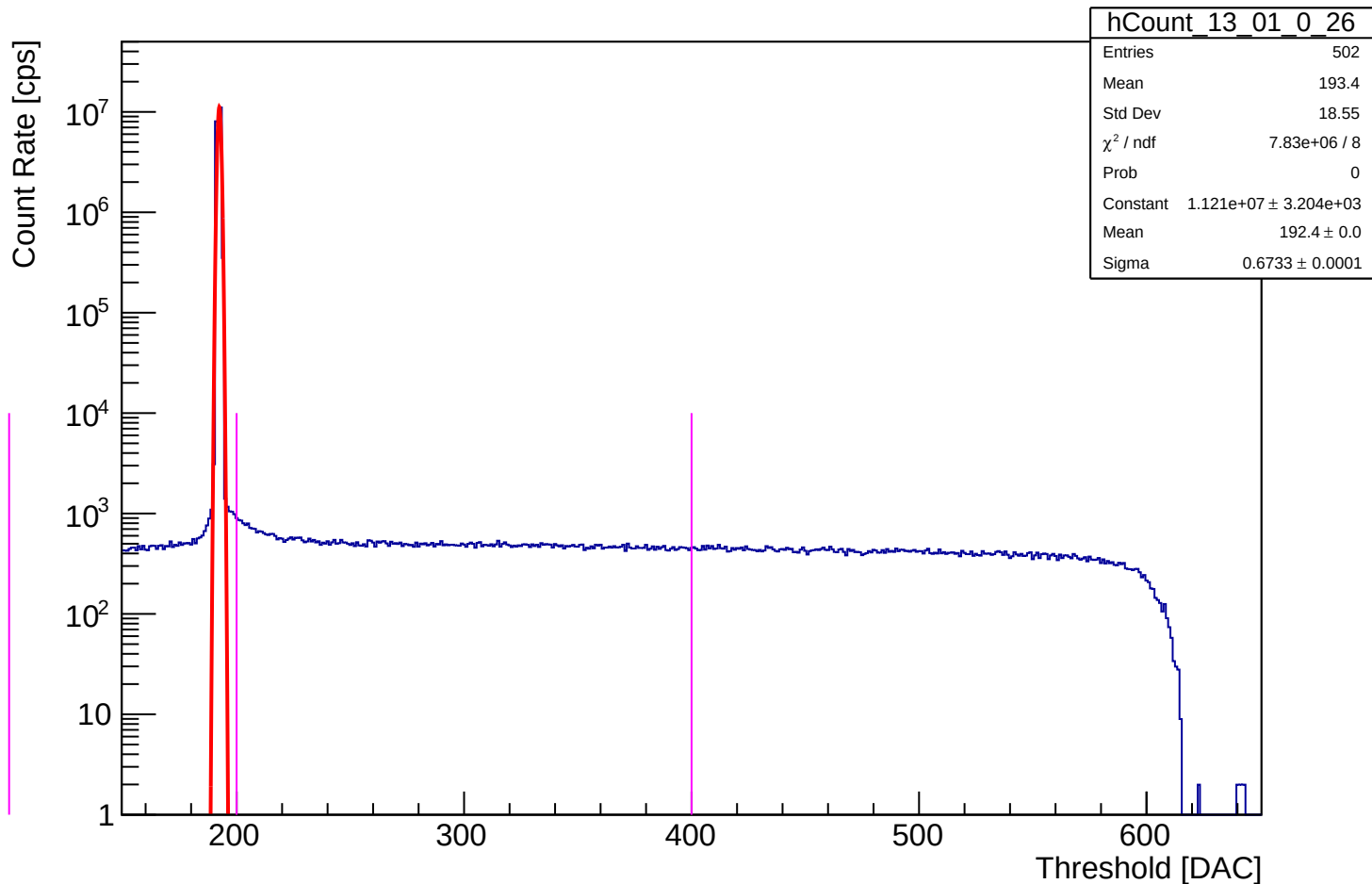
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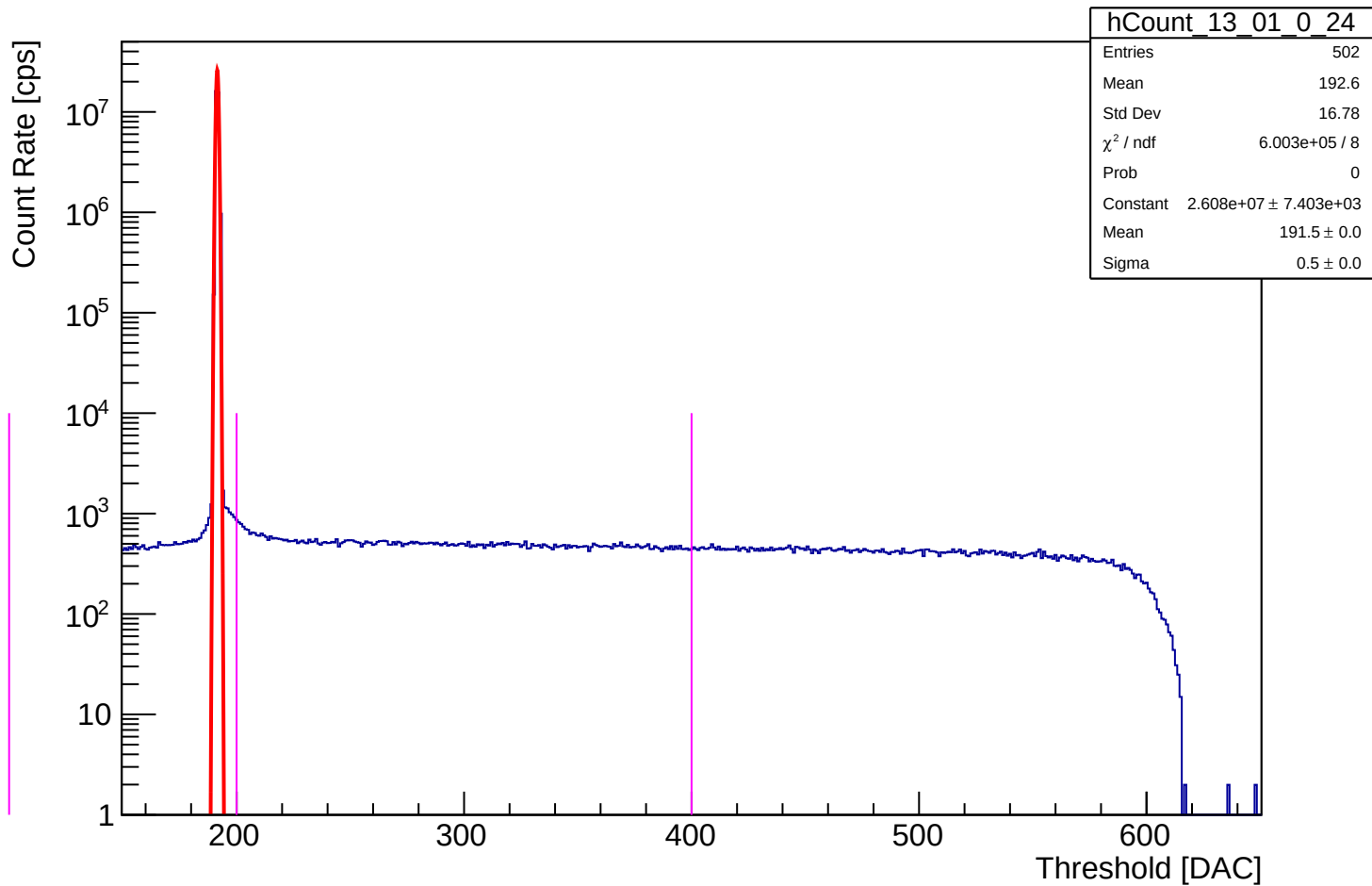
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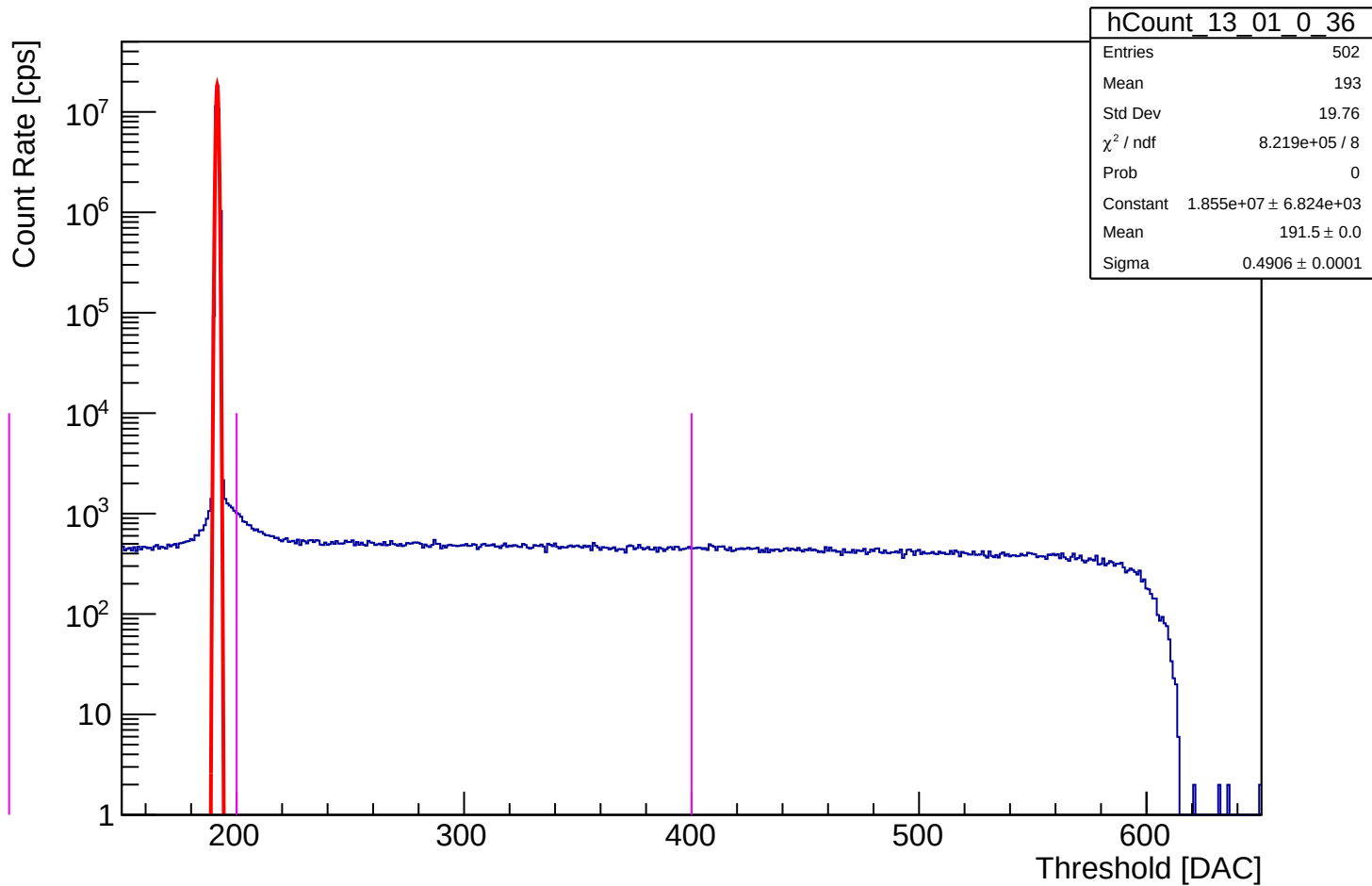
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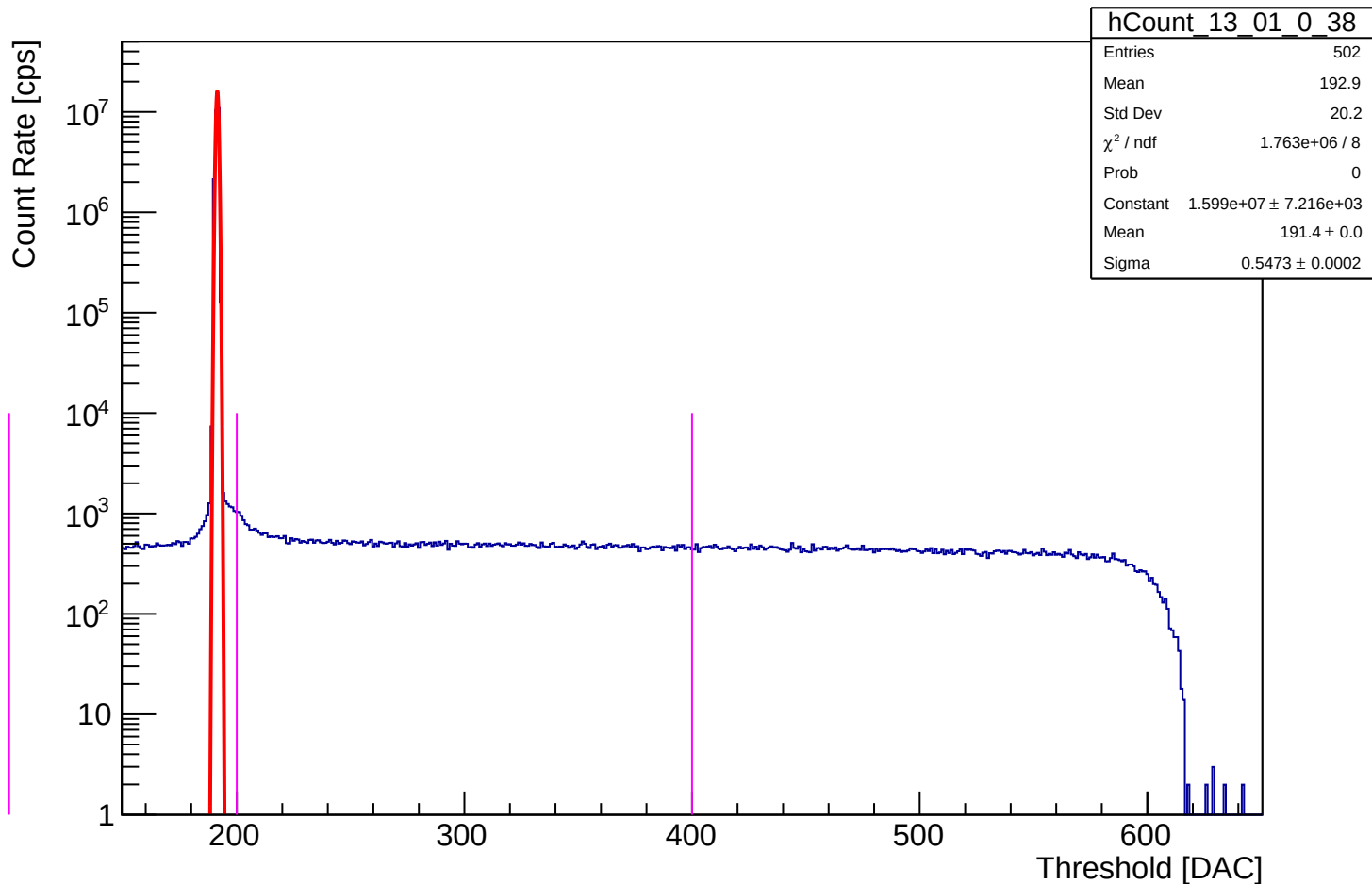
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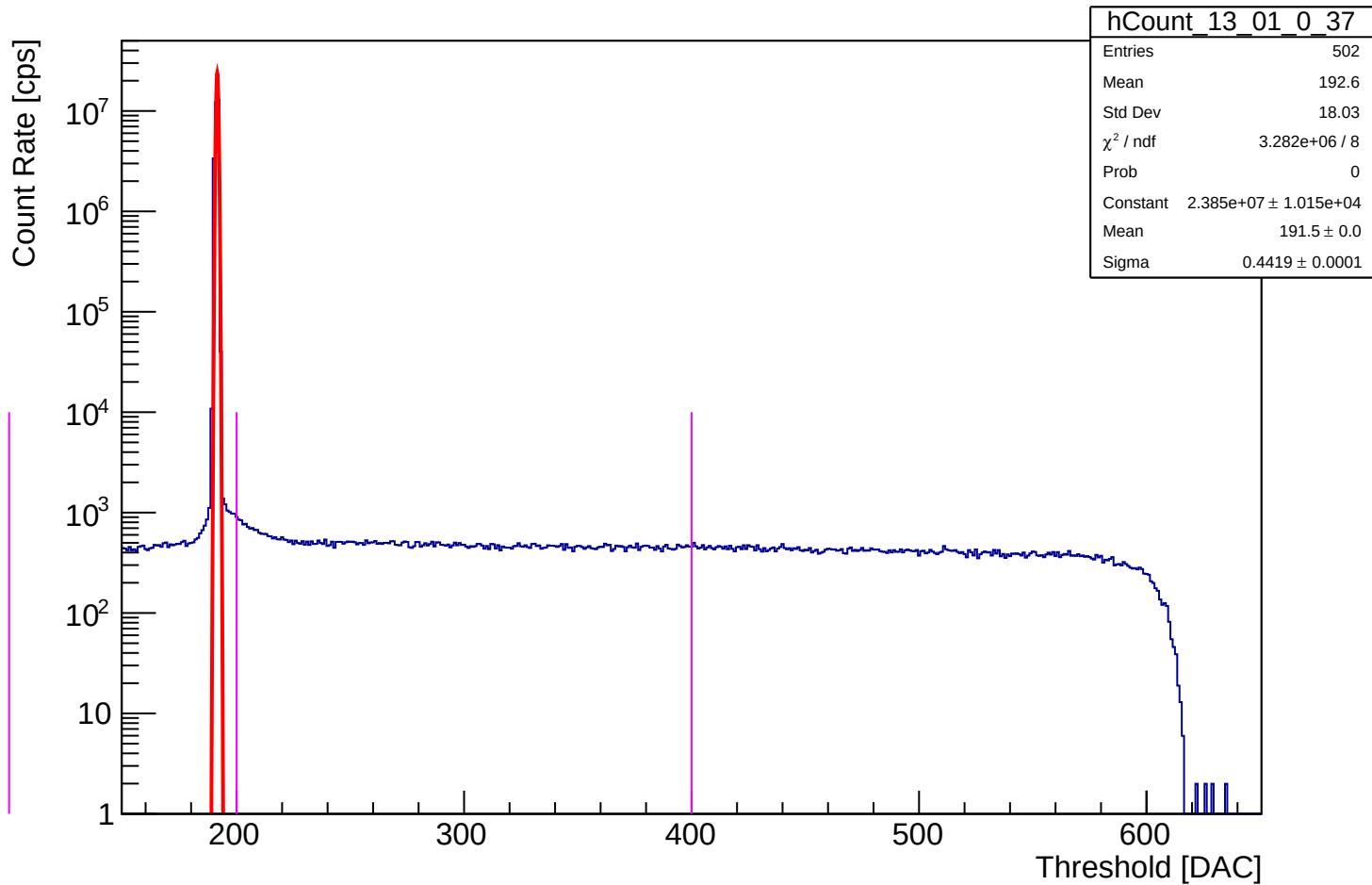
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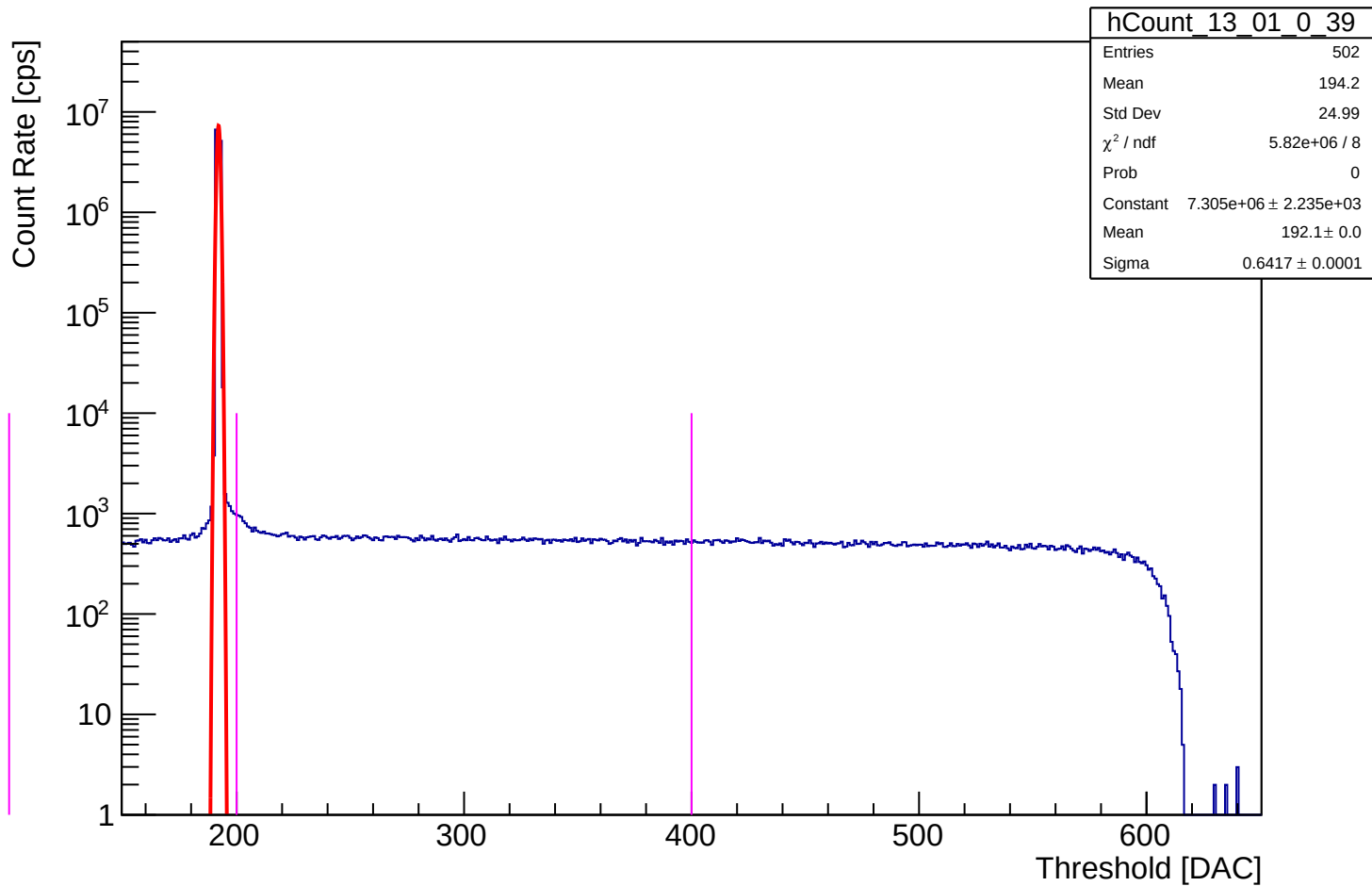
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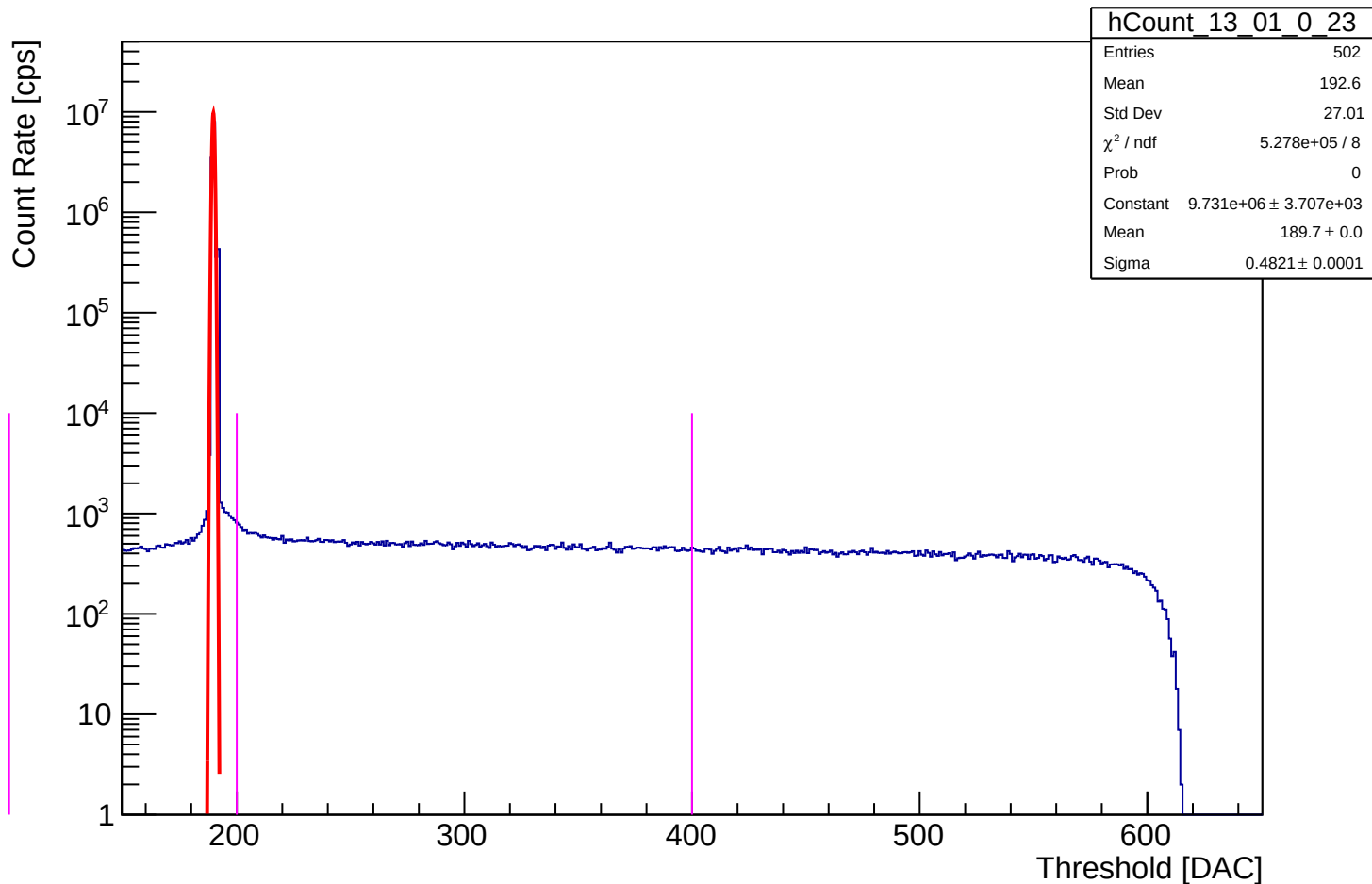
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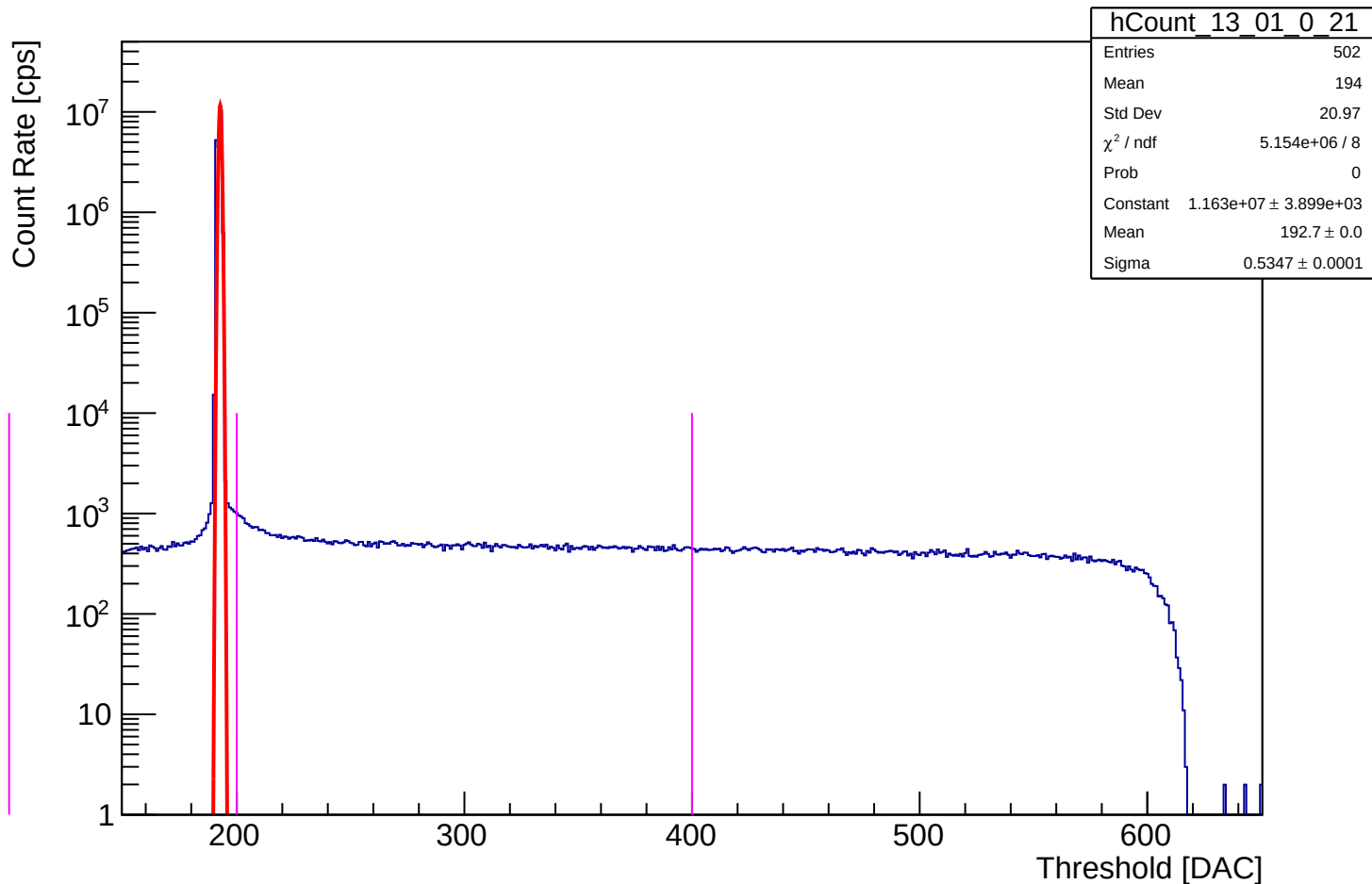
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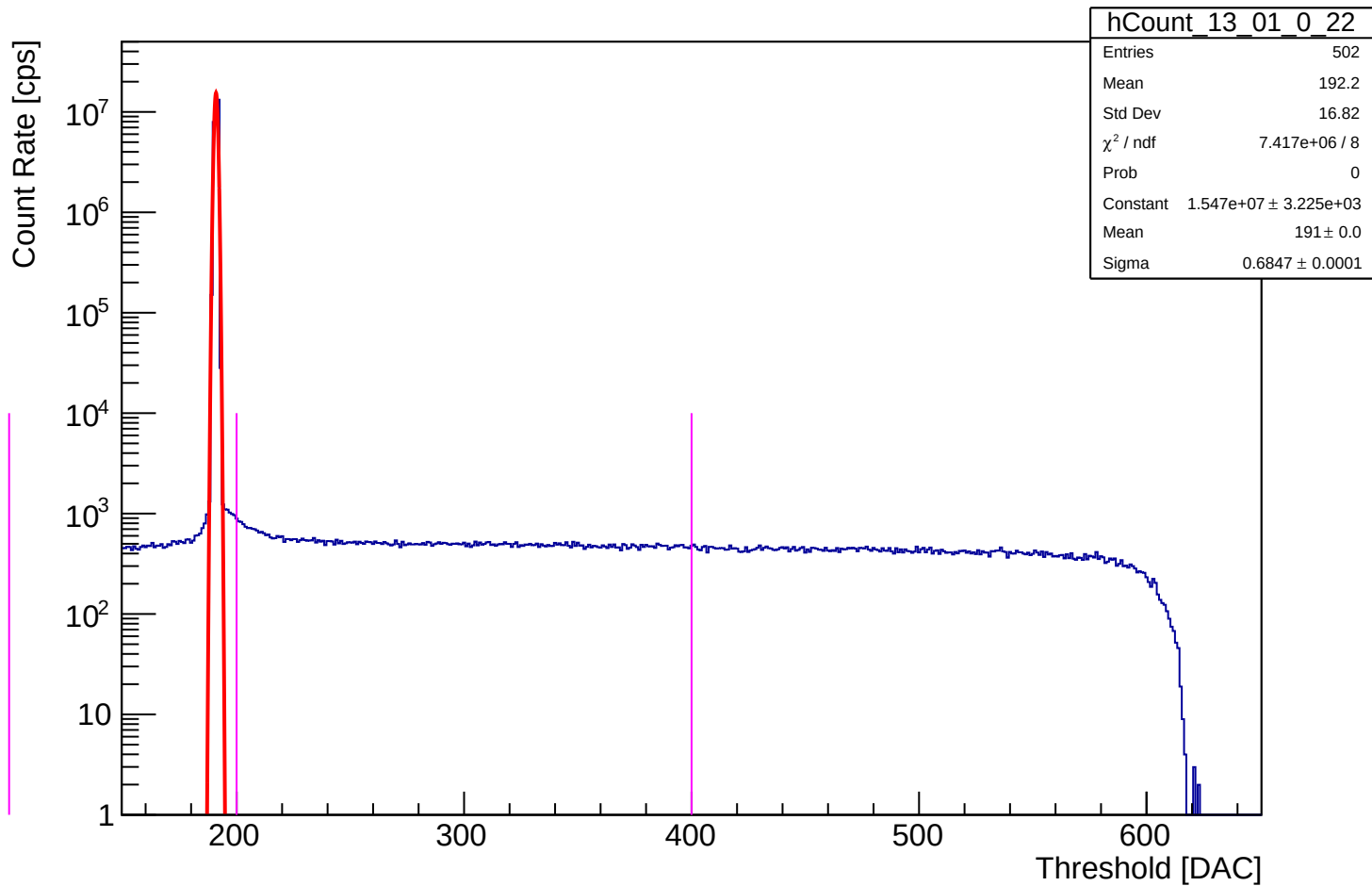
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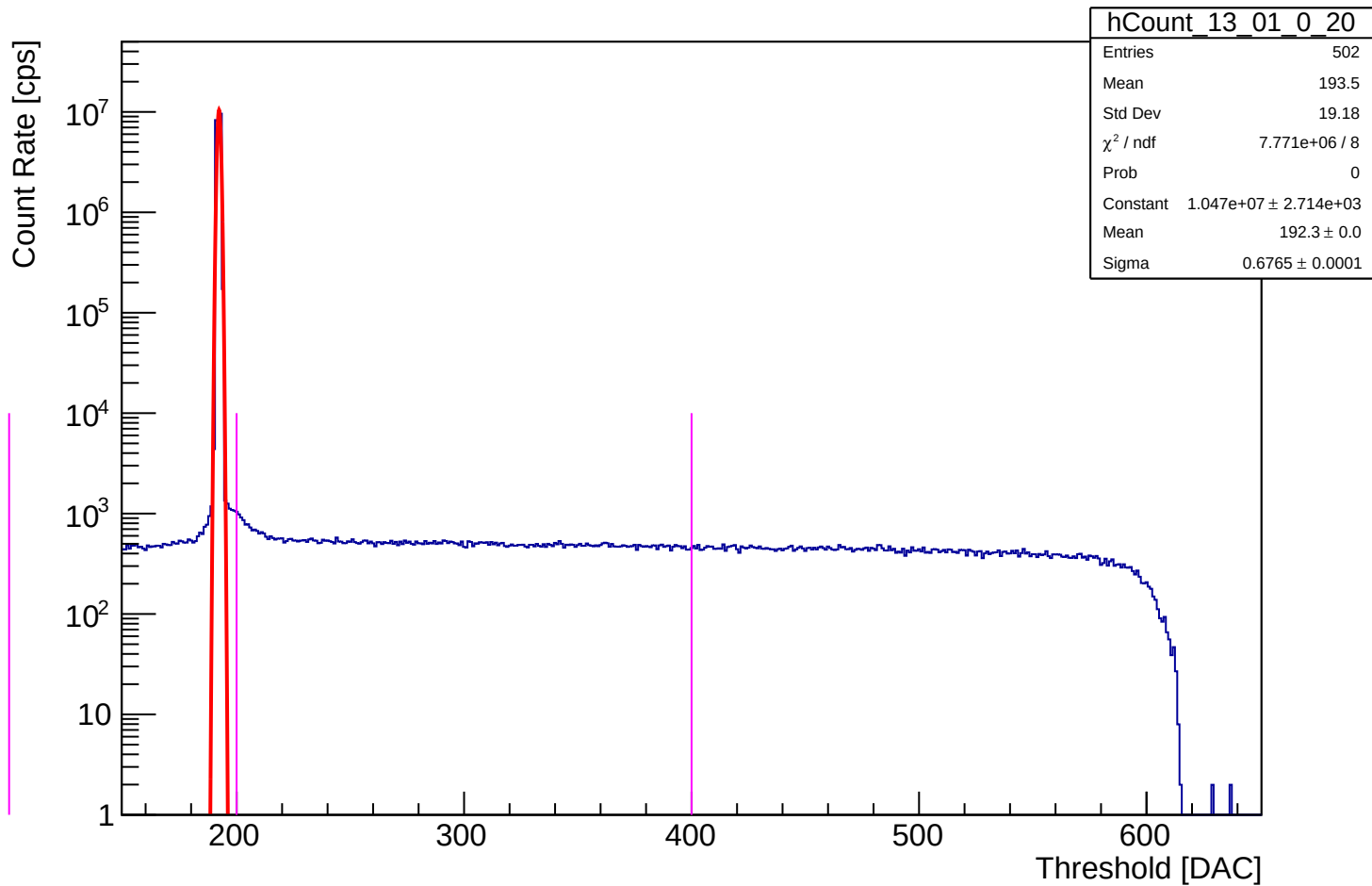
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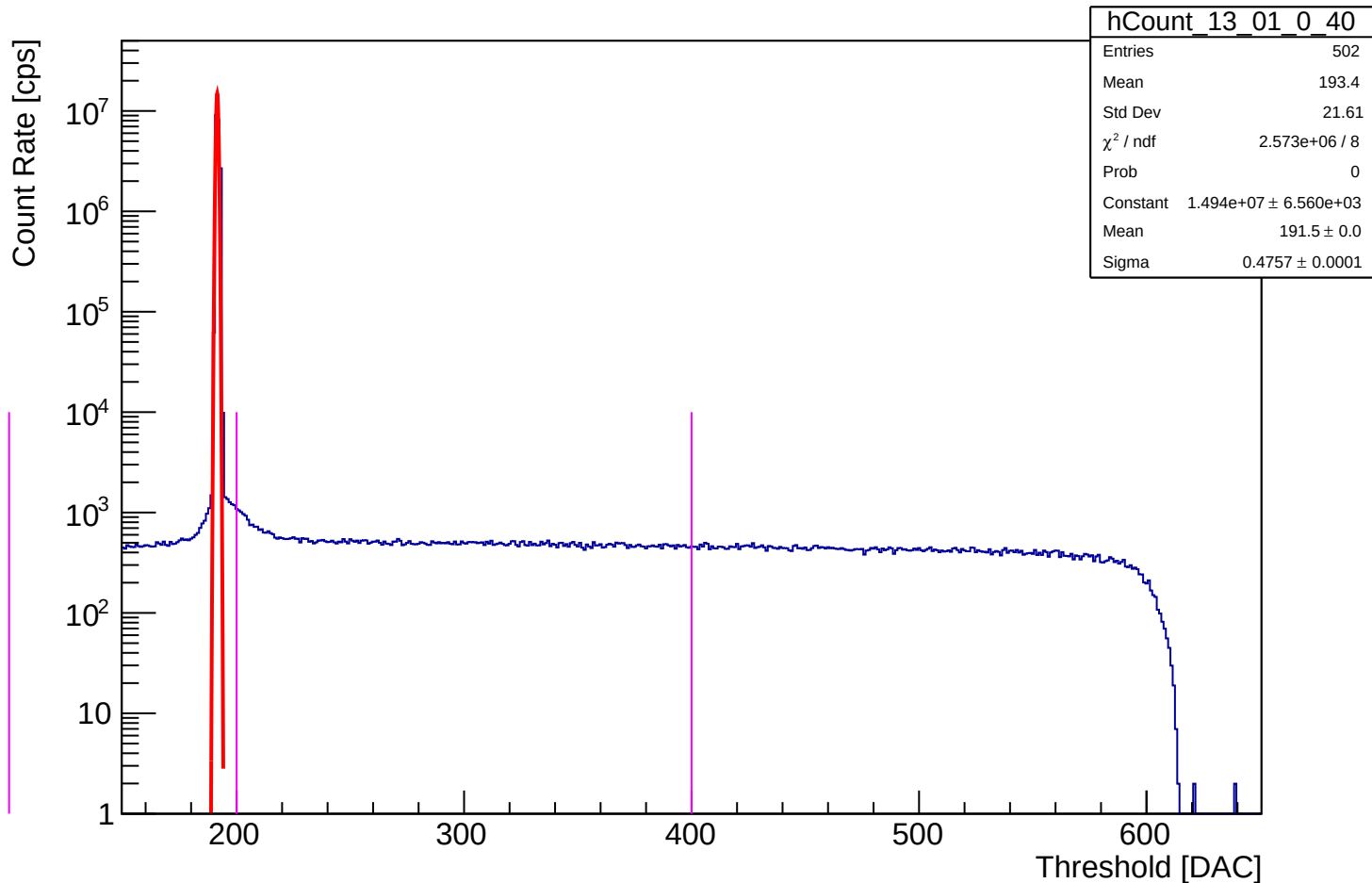
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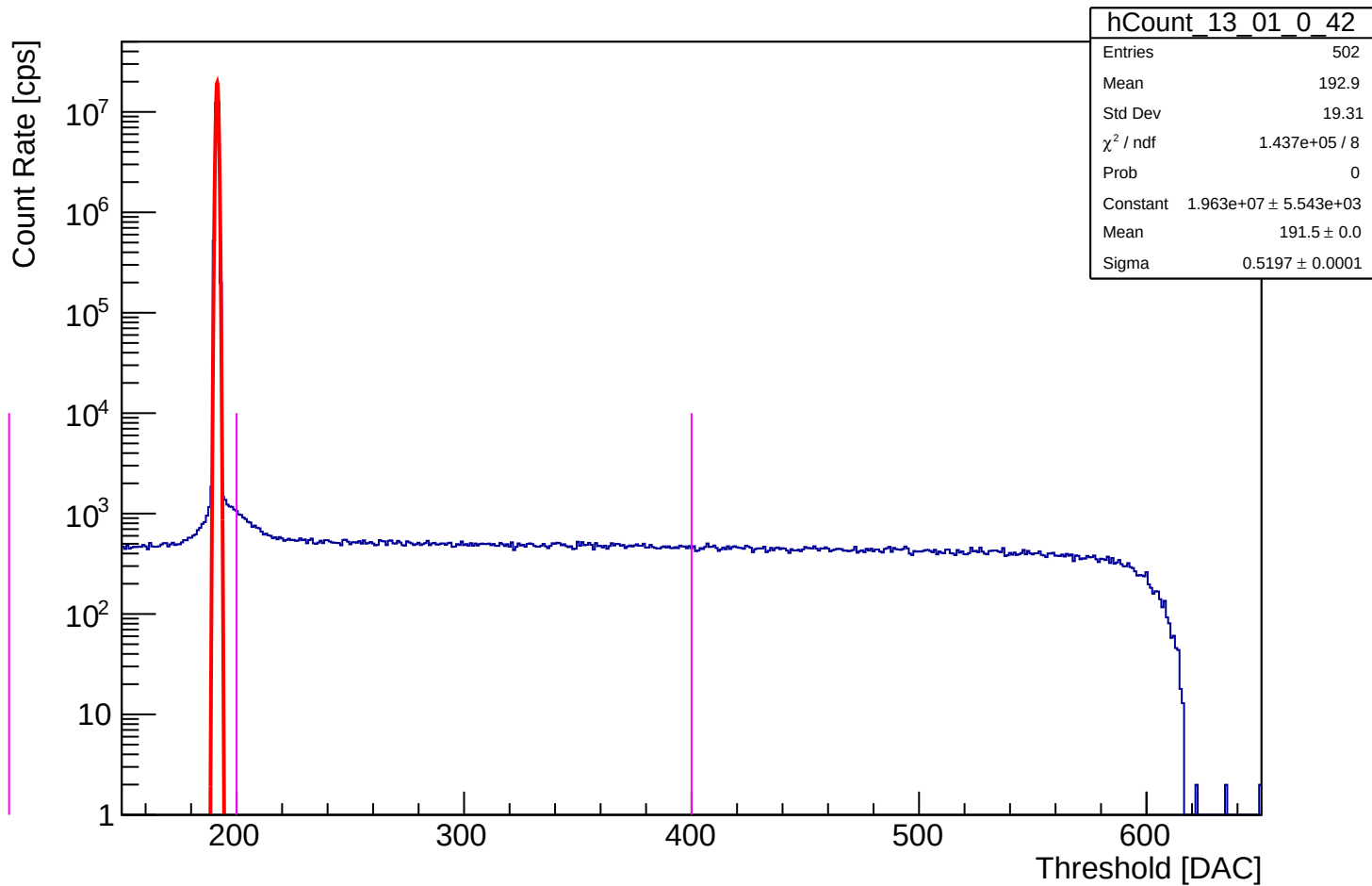
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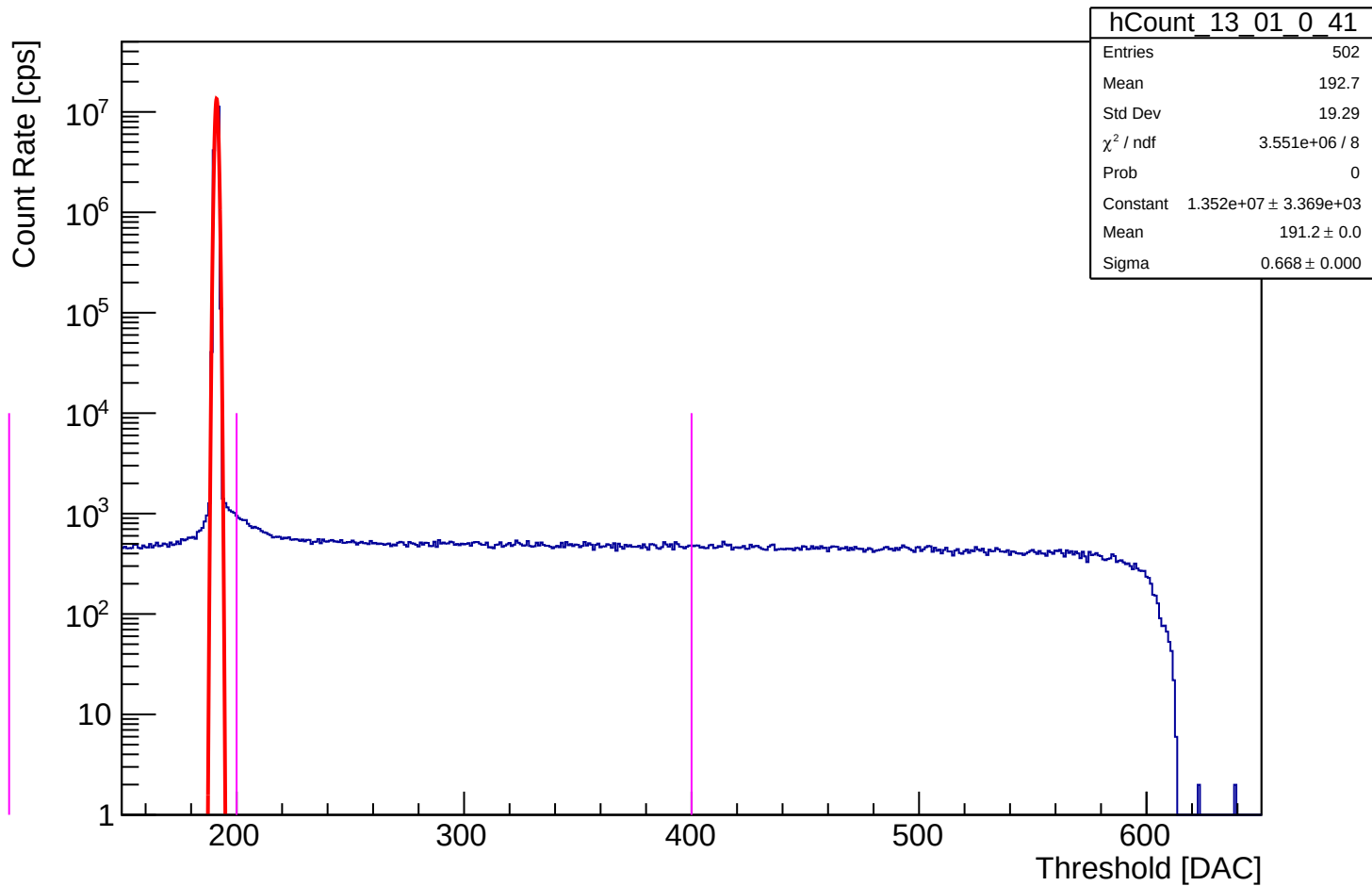
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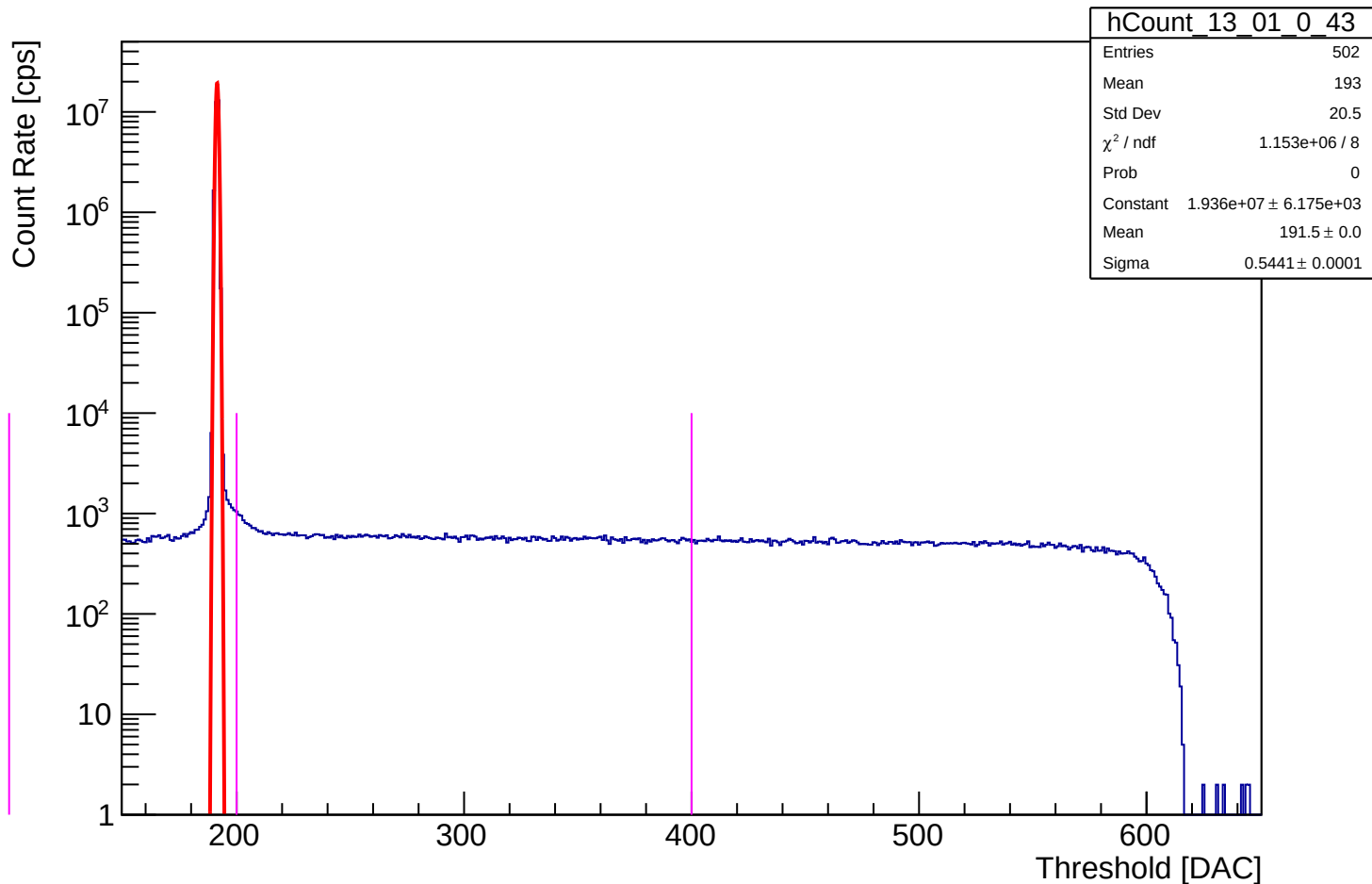
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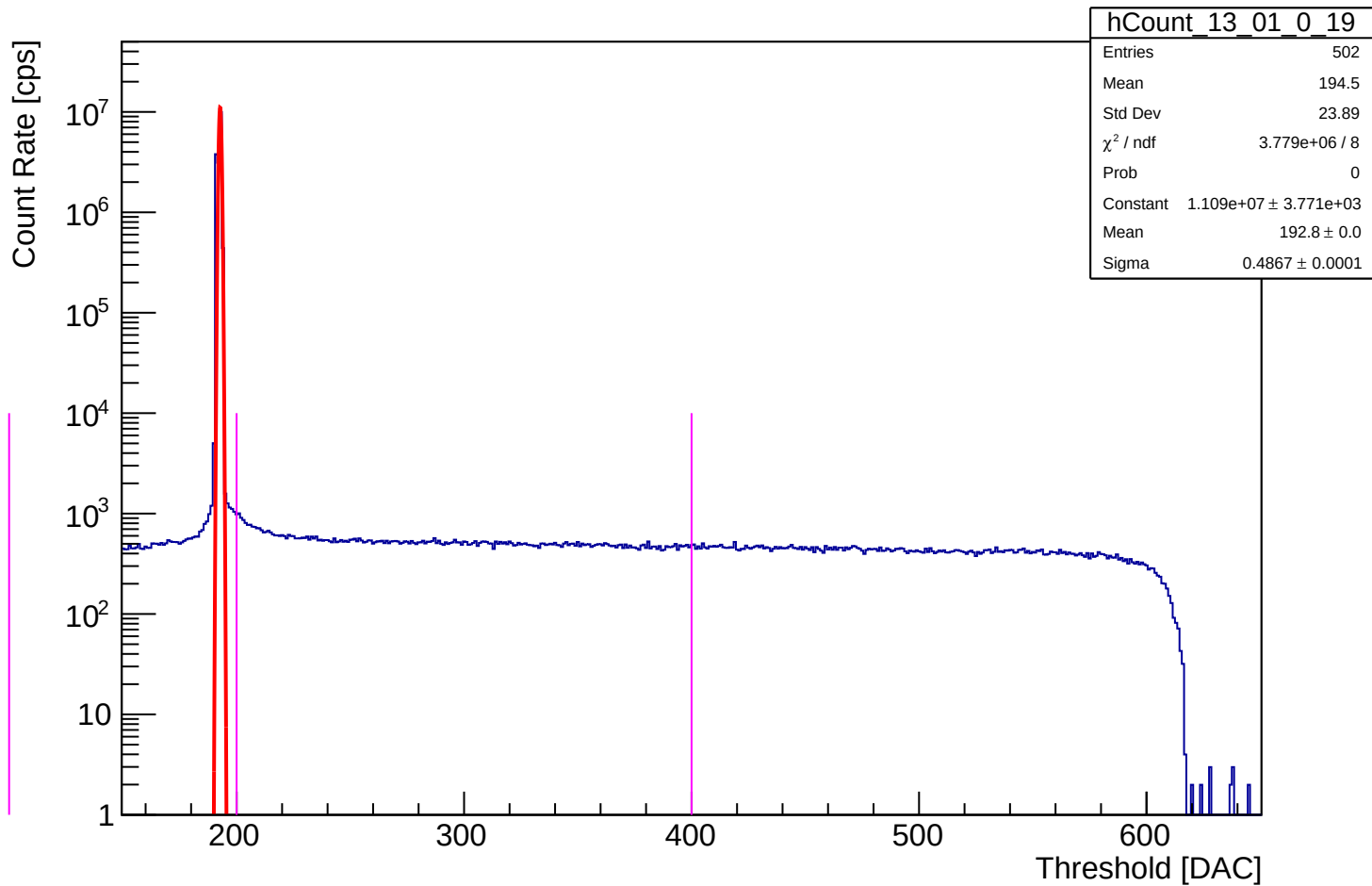
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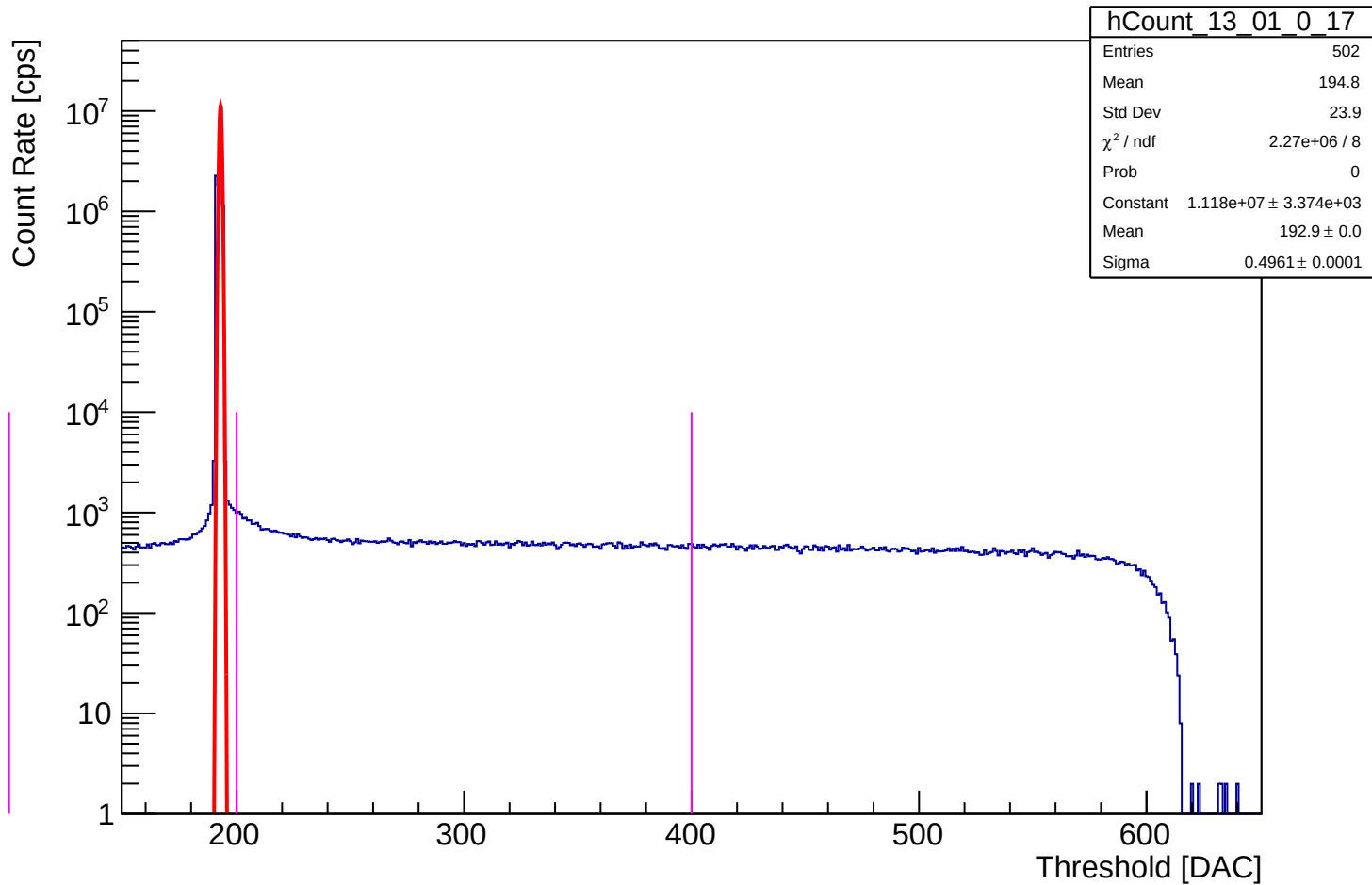
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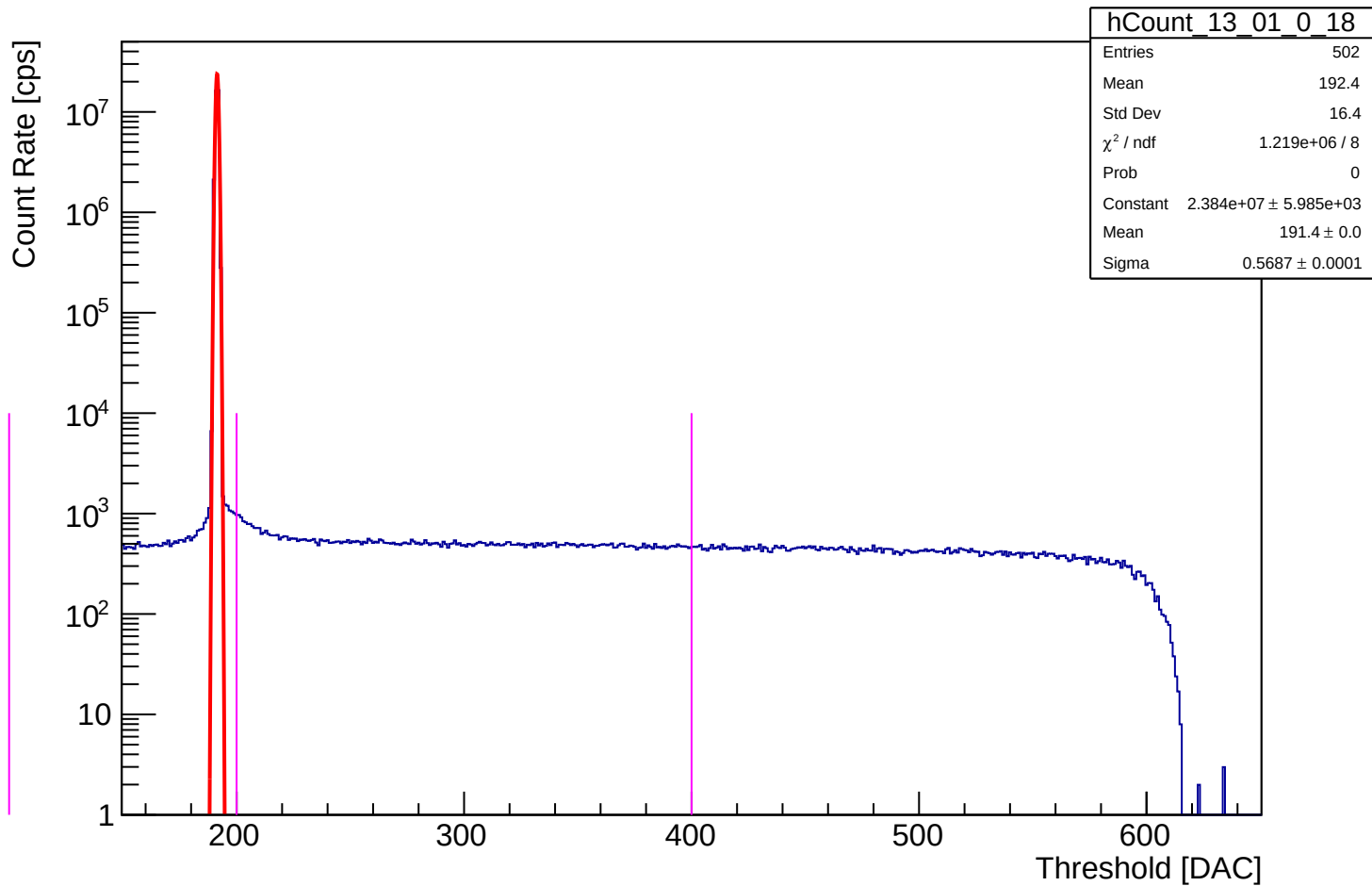
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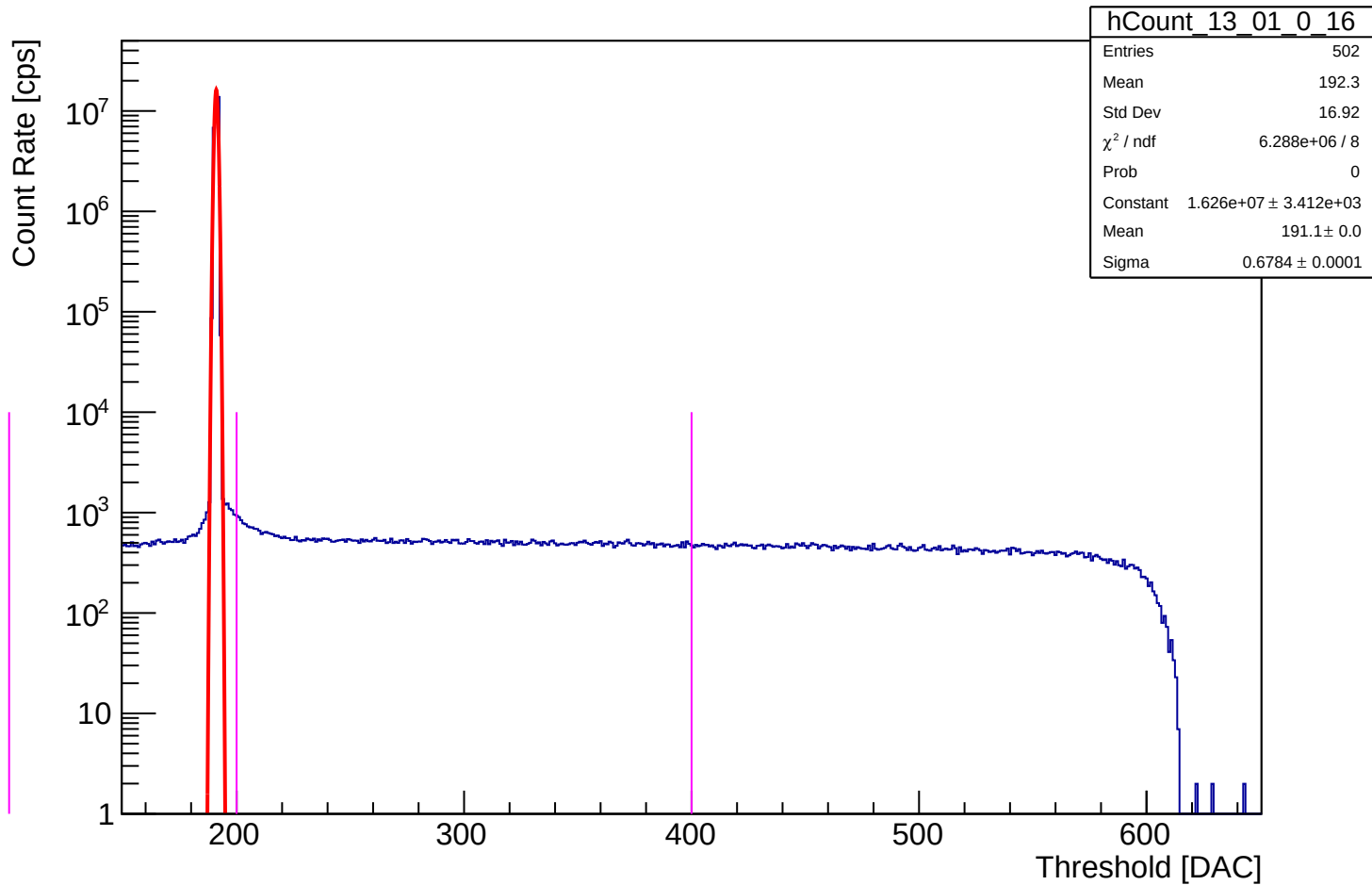
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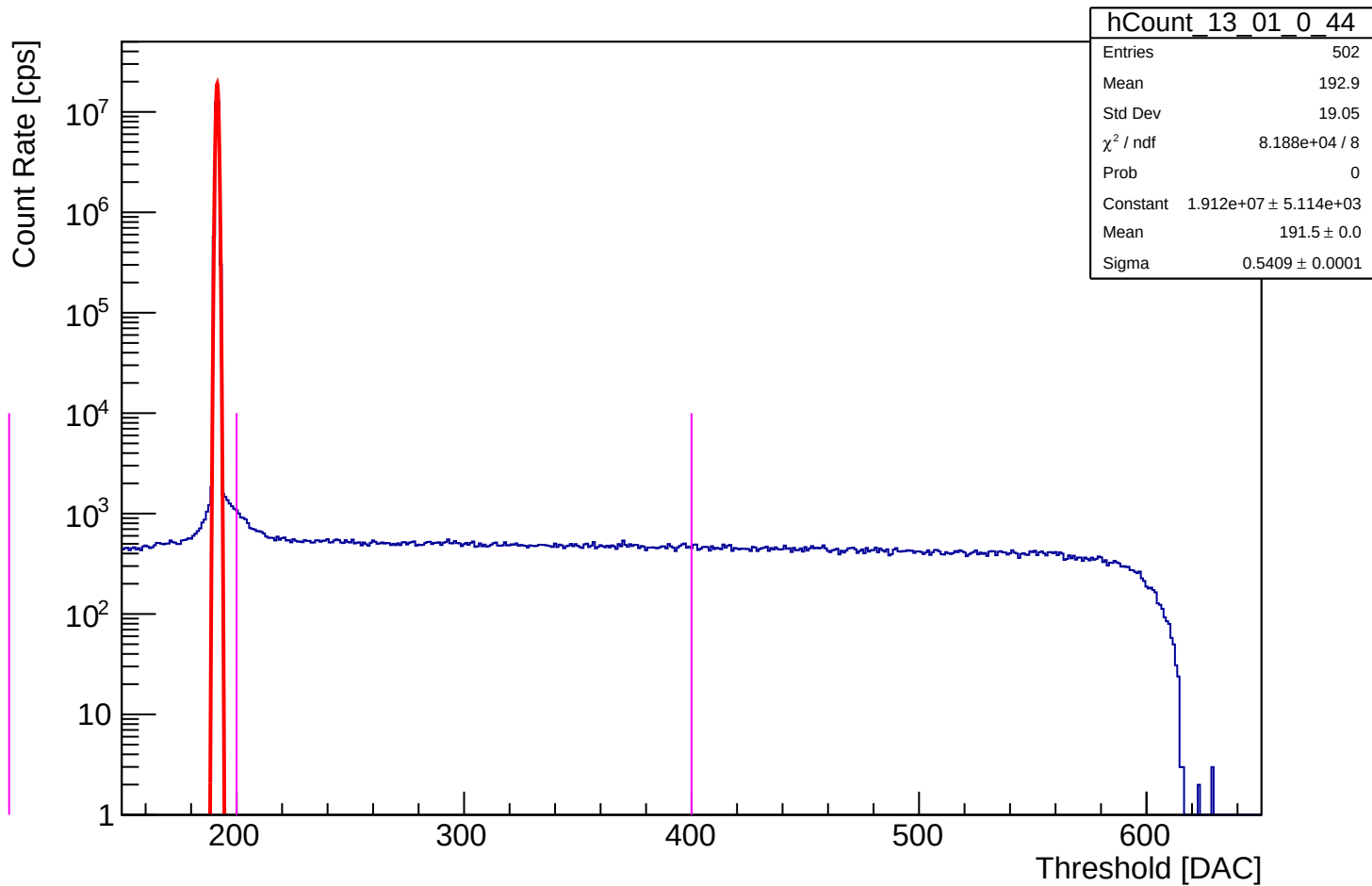
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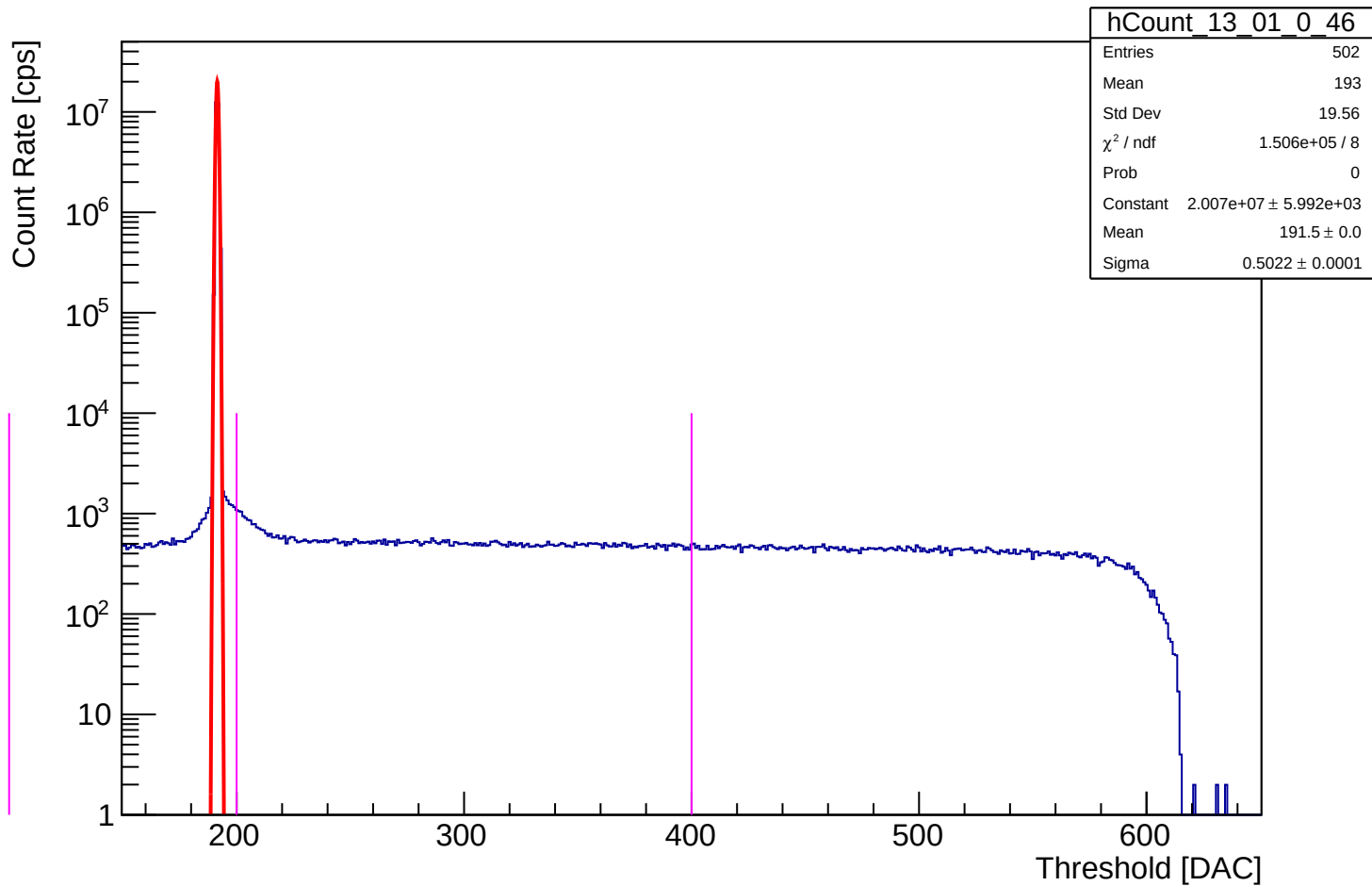
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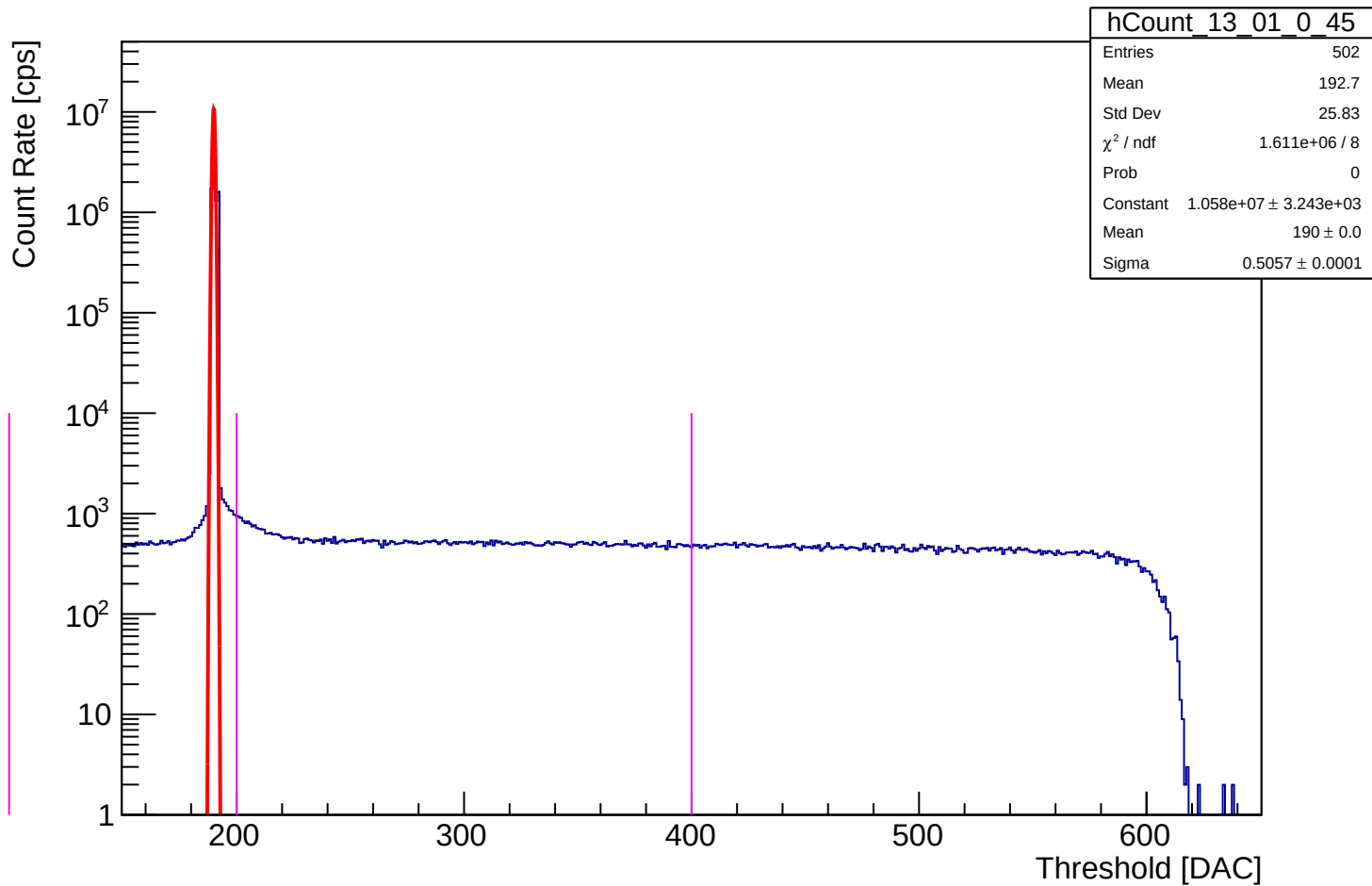
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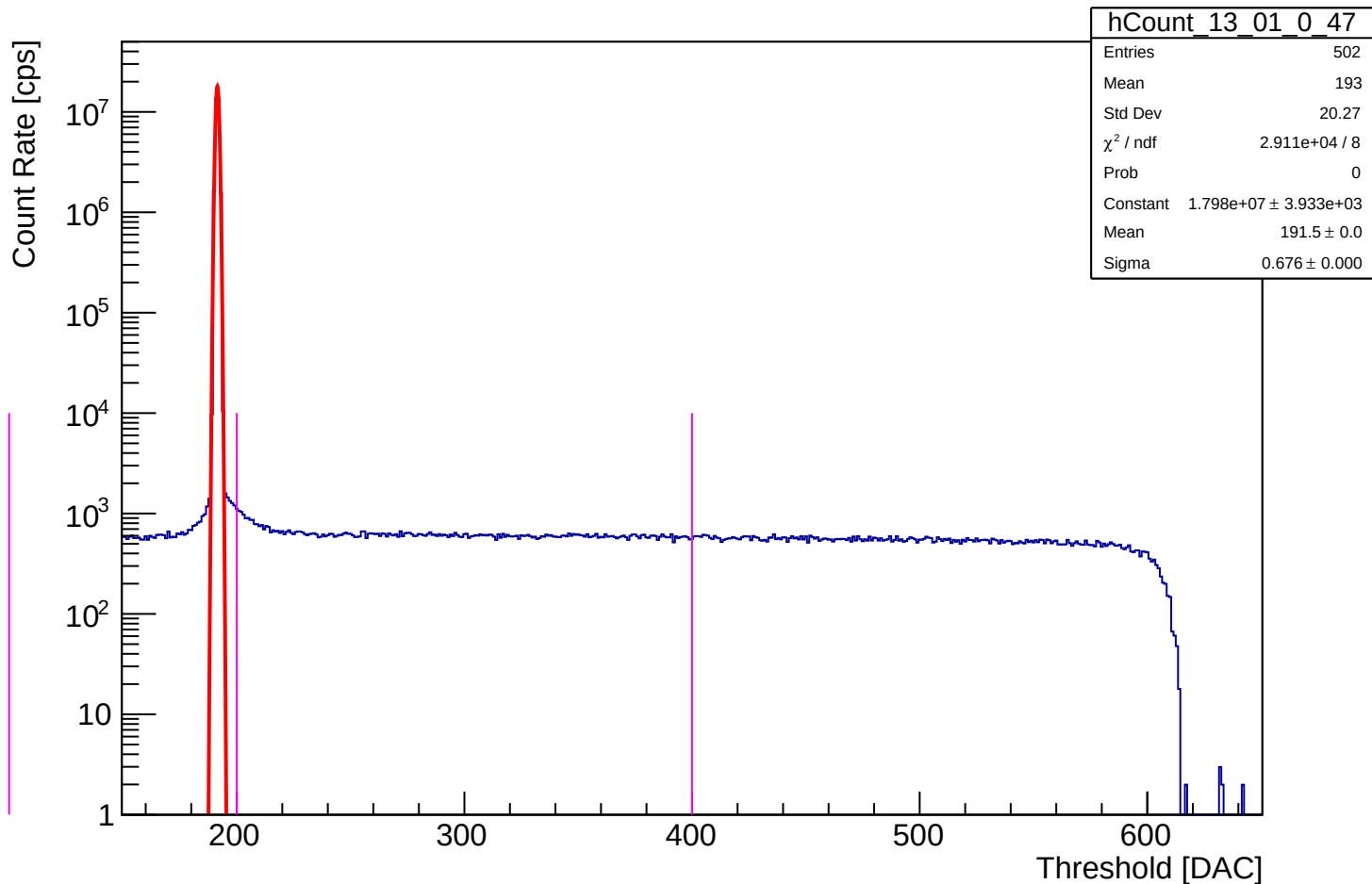
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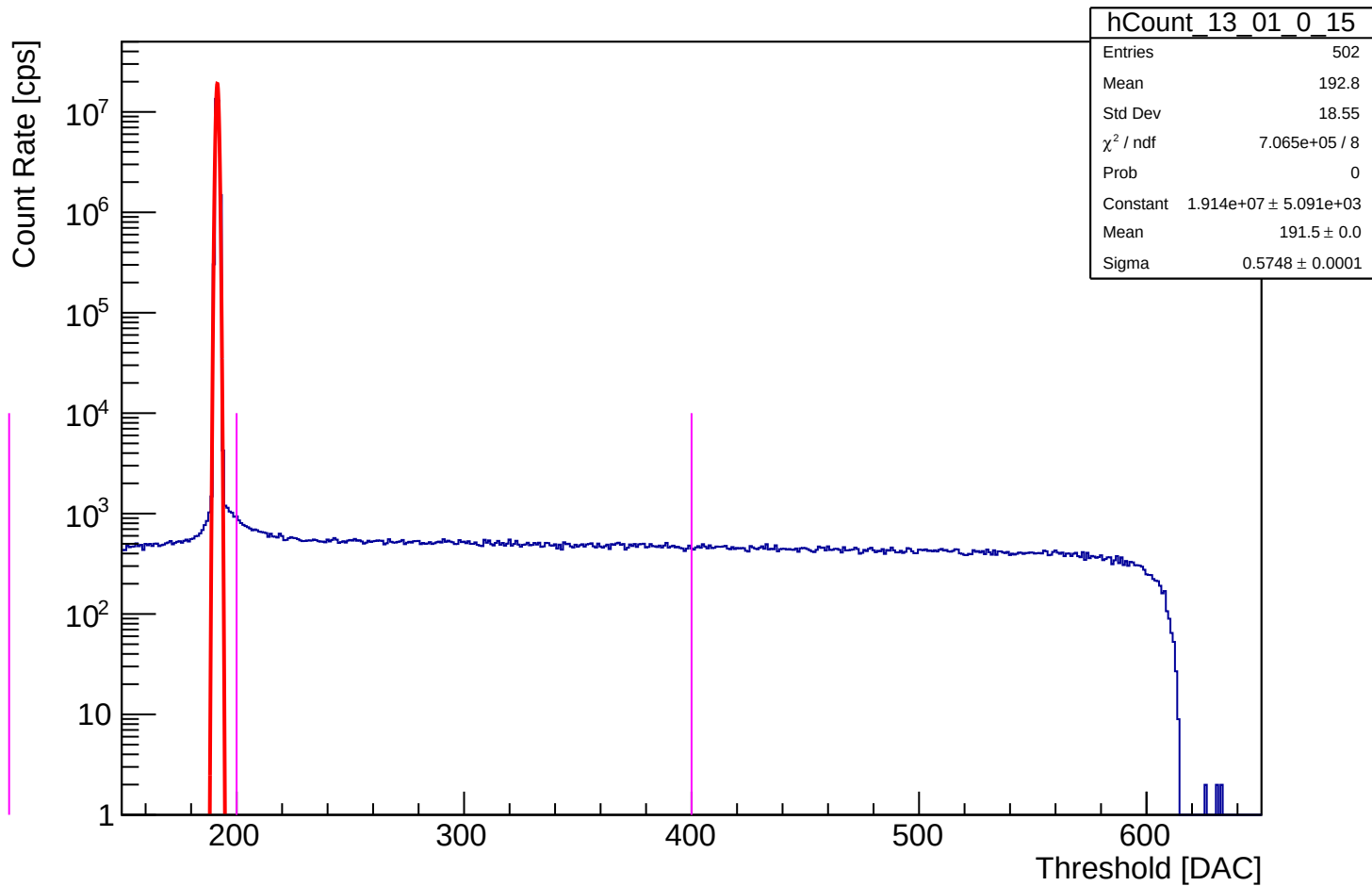
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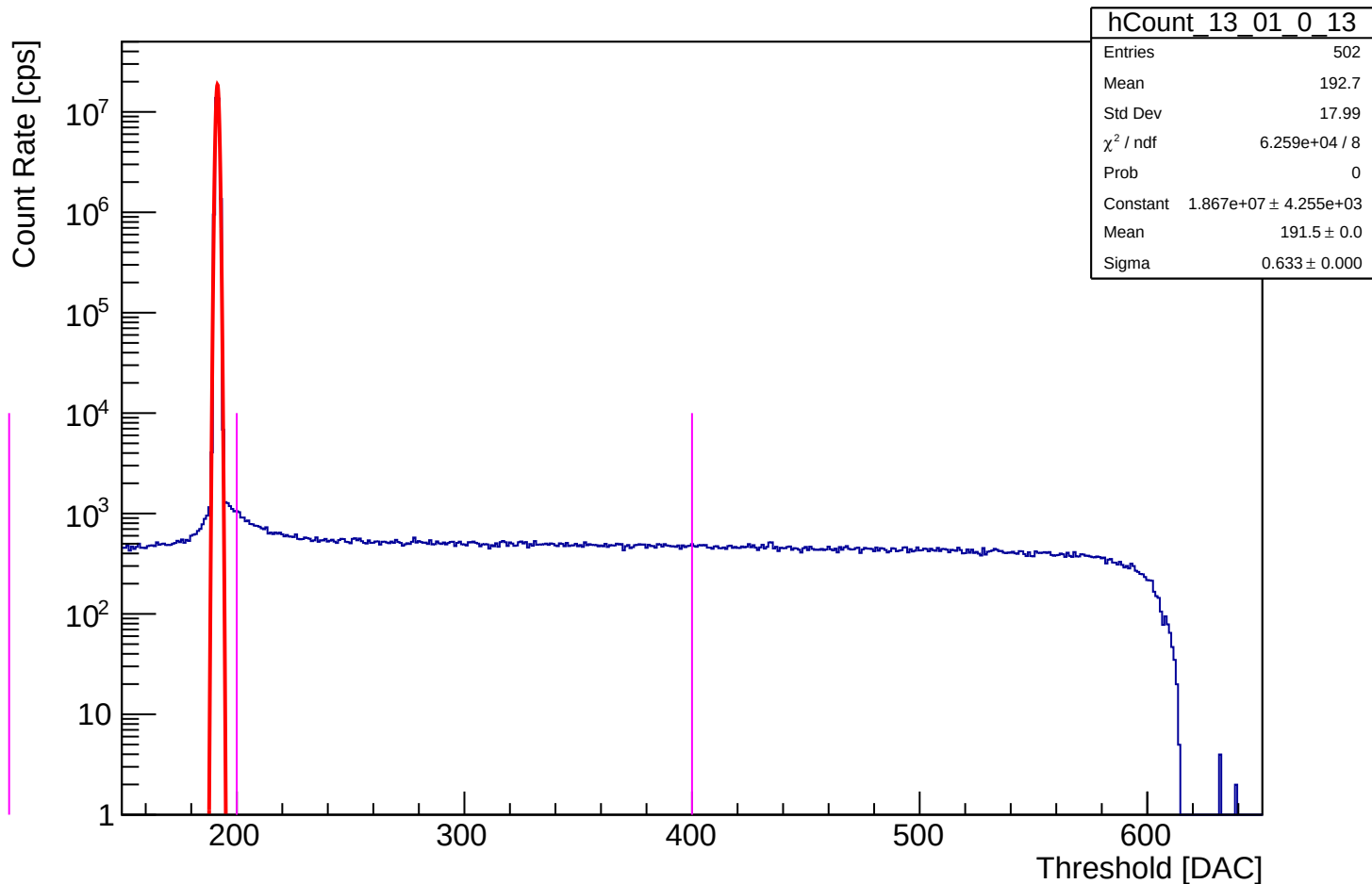
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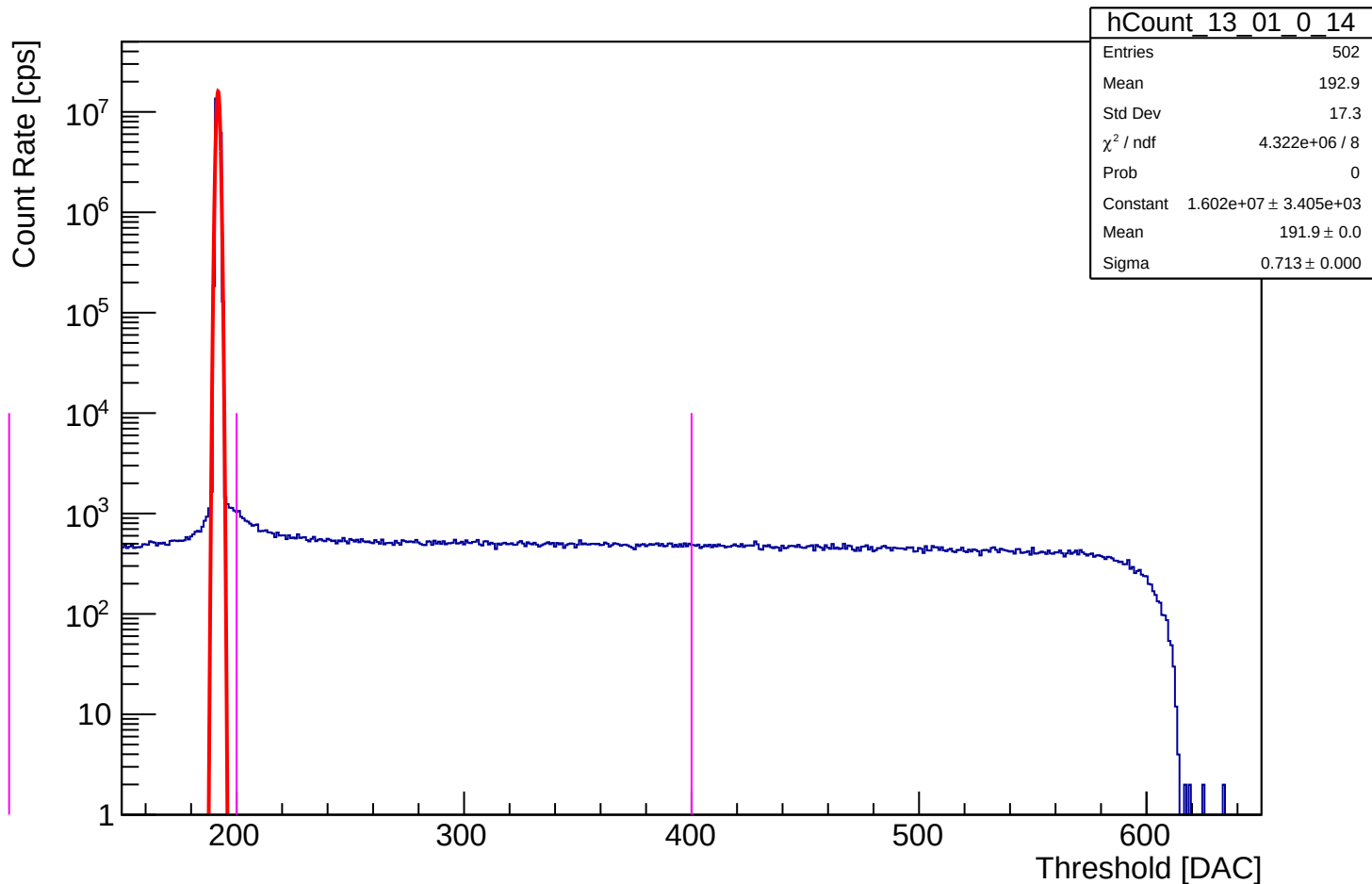
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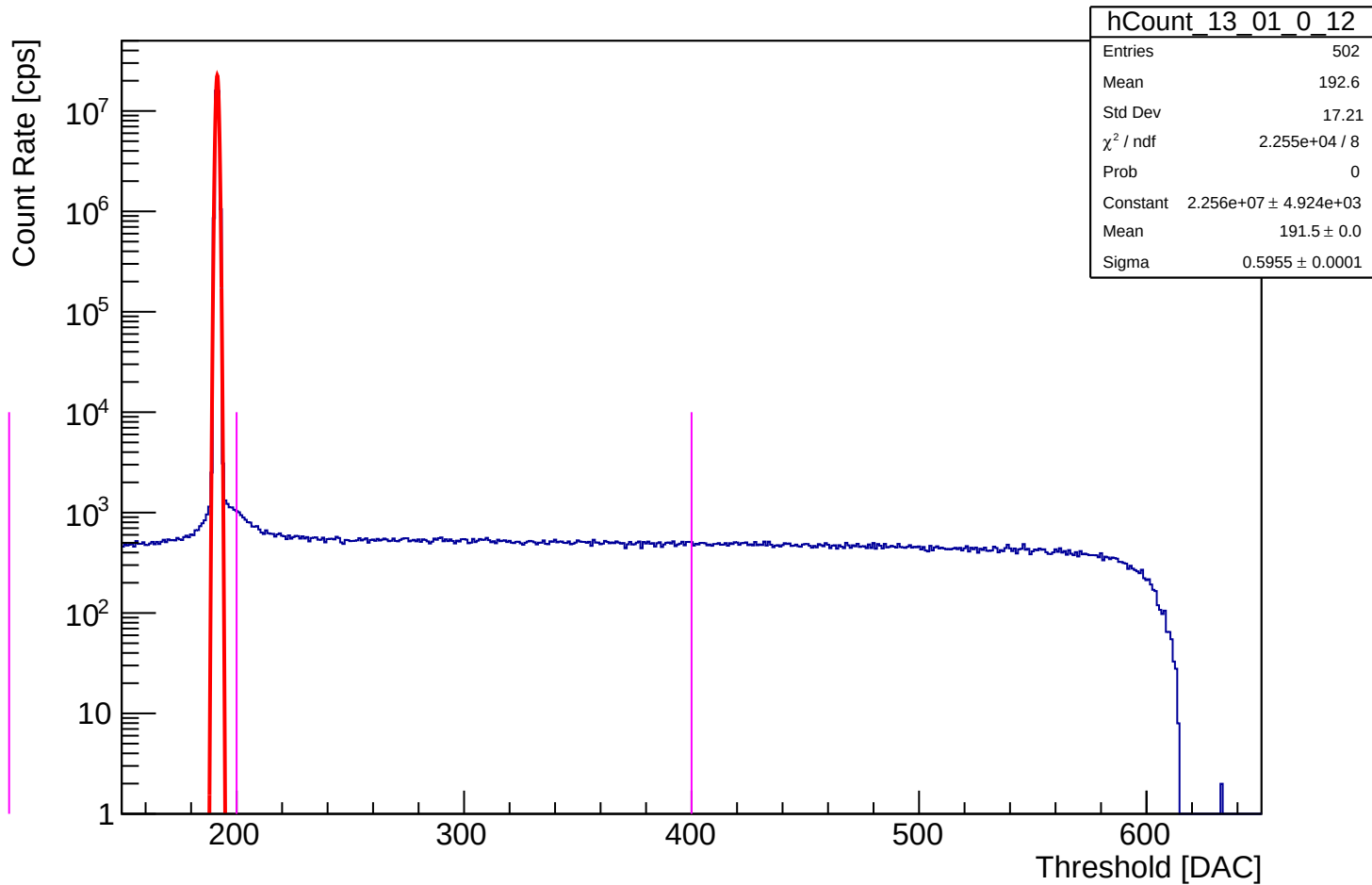
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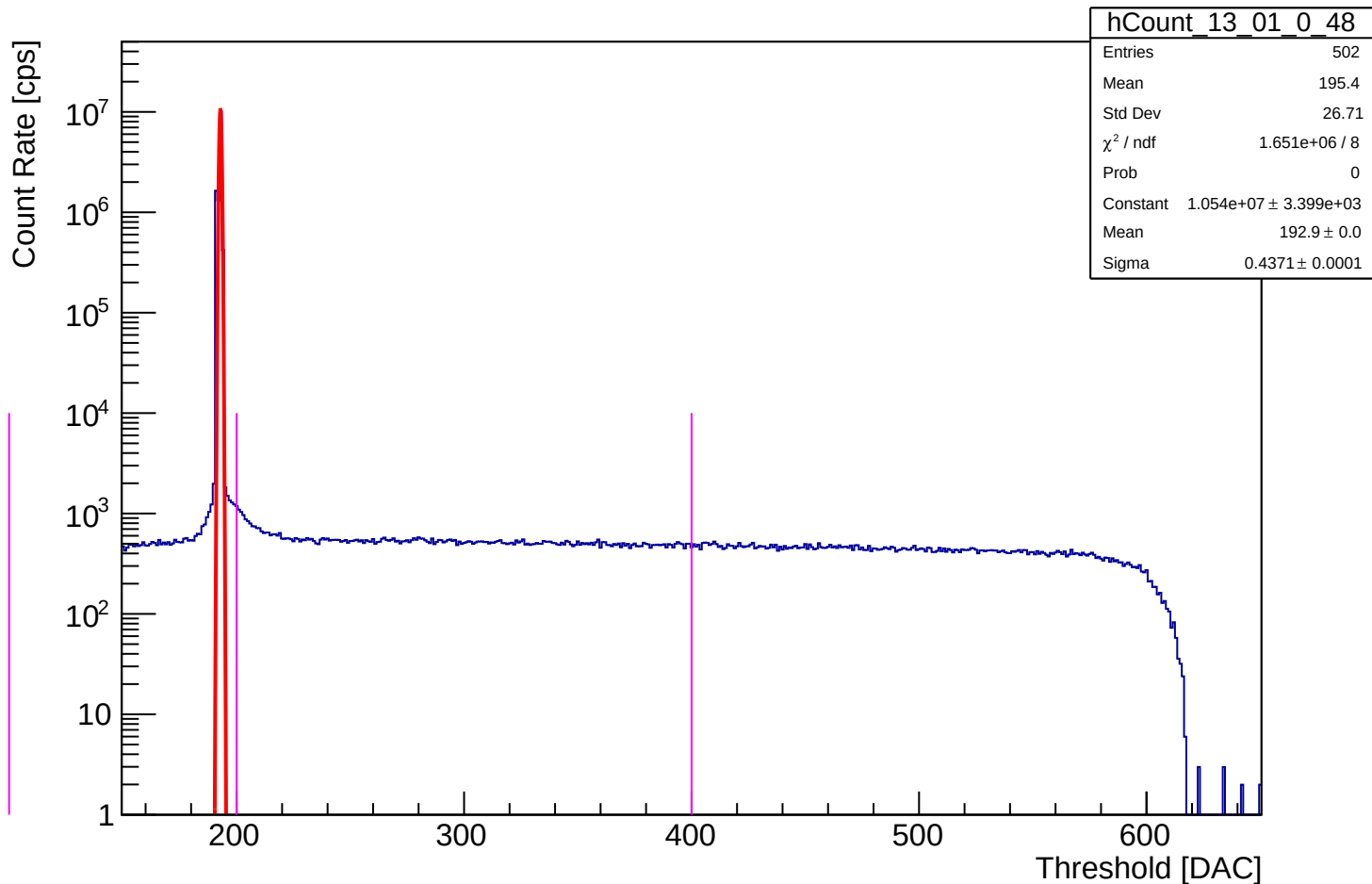
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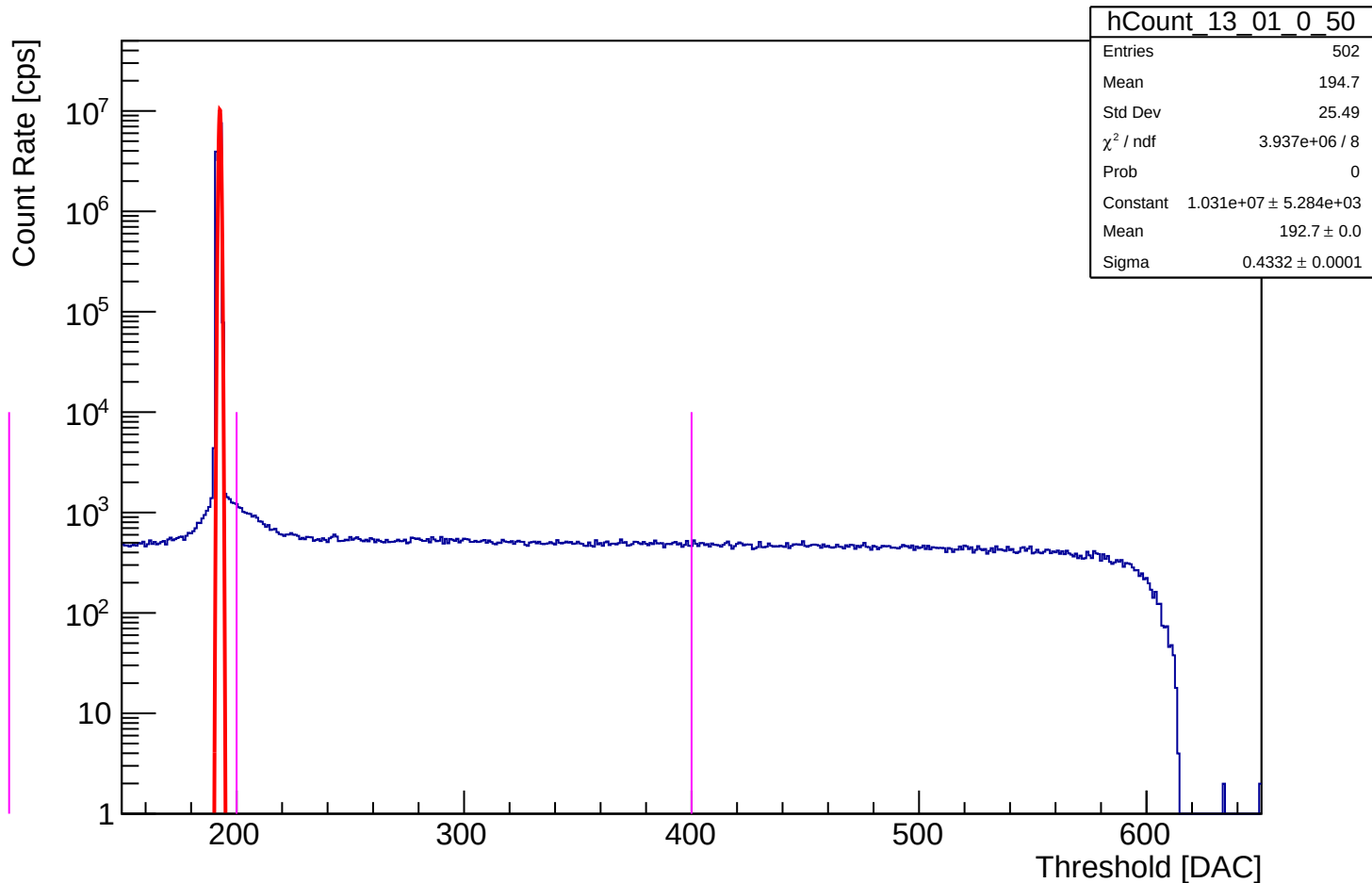
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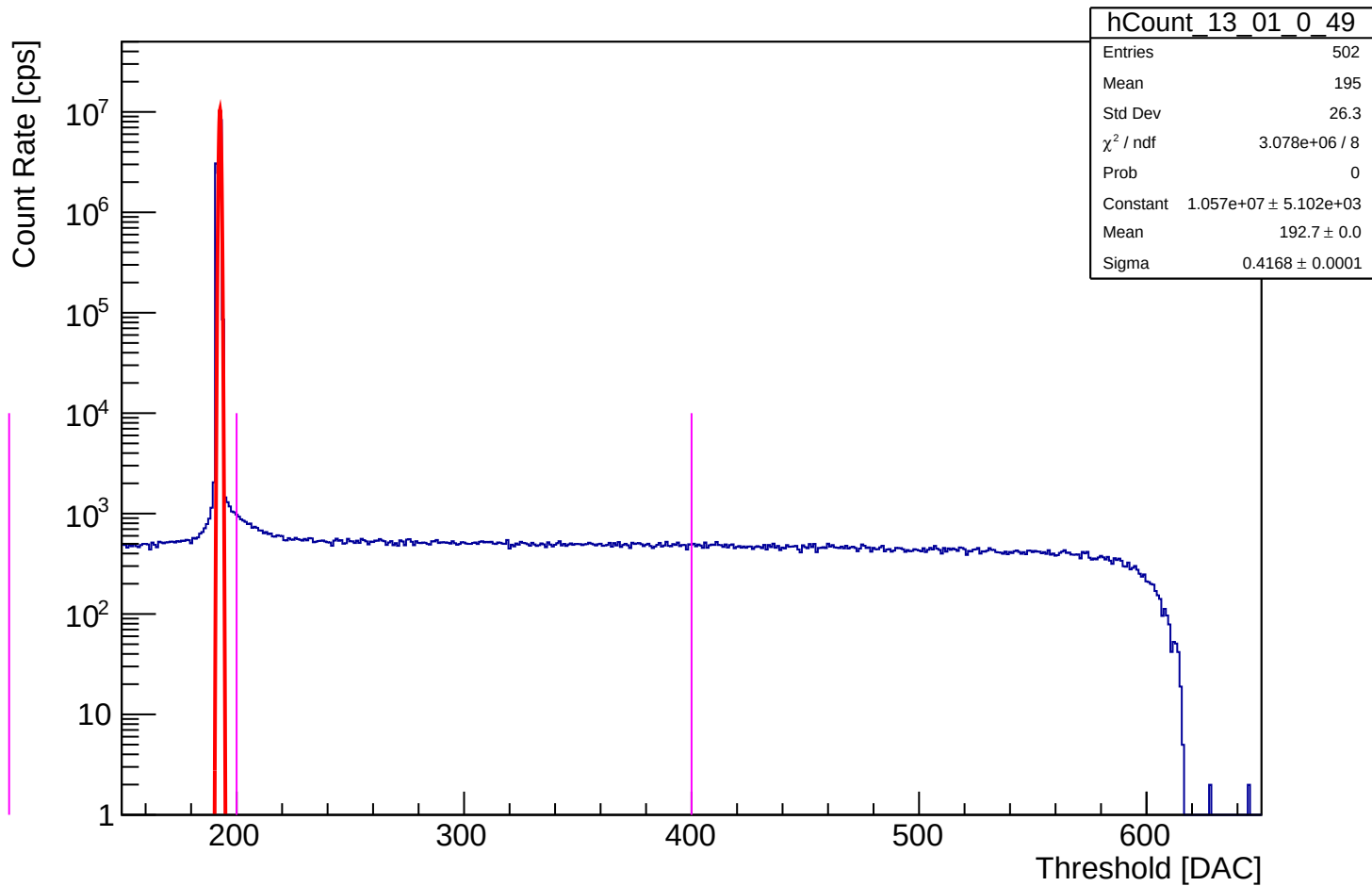
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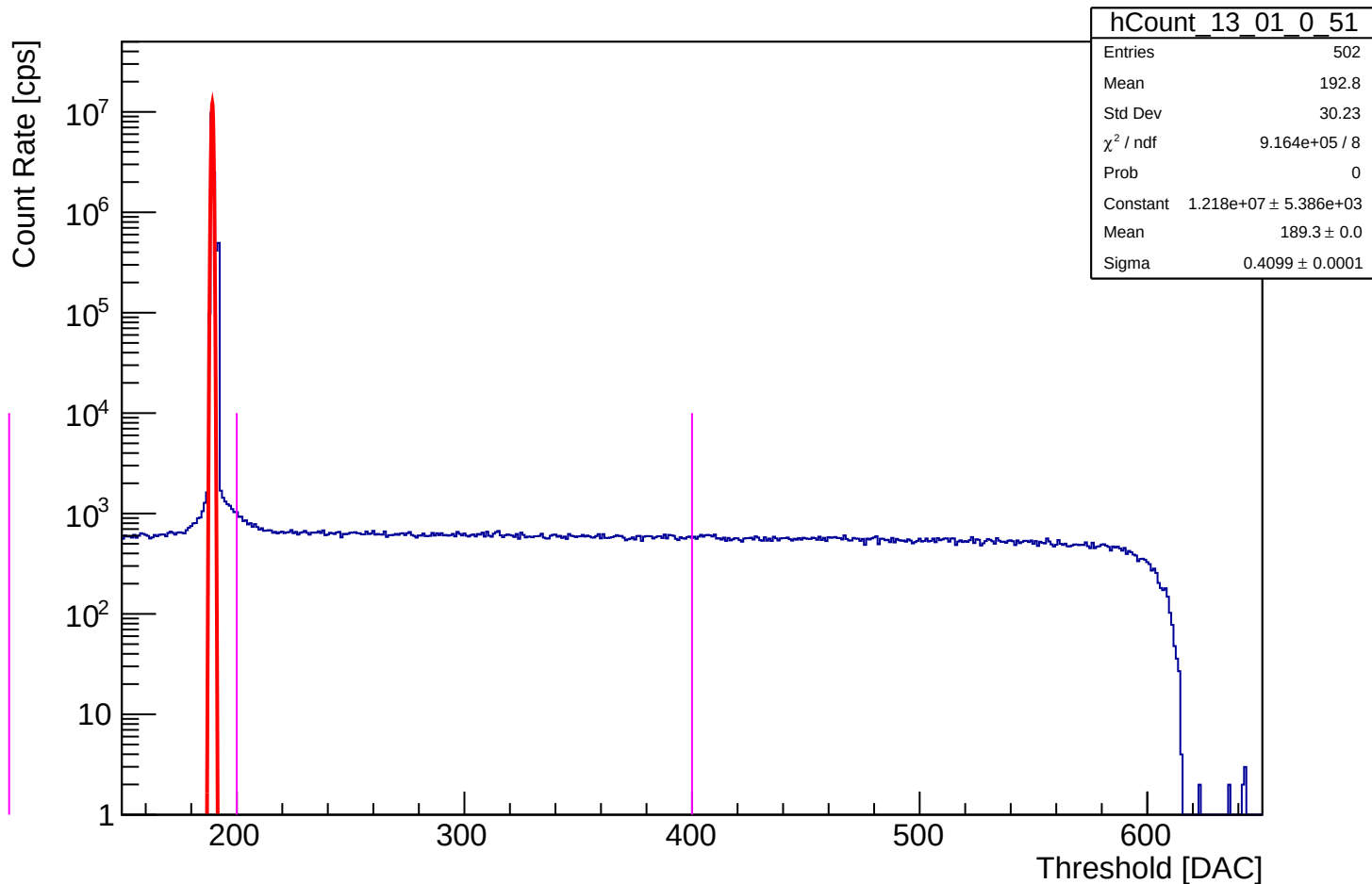


Row 1 Tile 1 Pmt 4 Pixel 38 Slot 13 Fiber 1 Asic 0 Channel 50

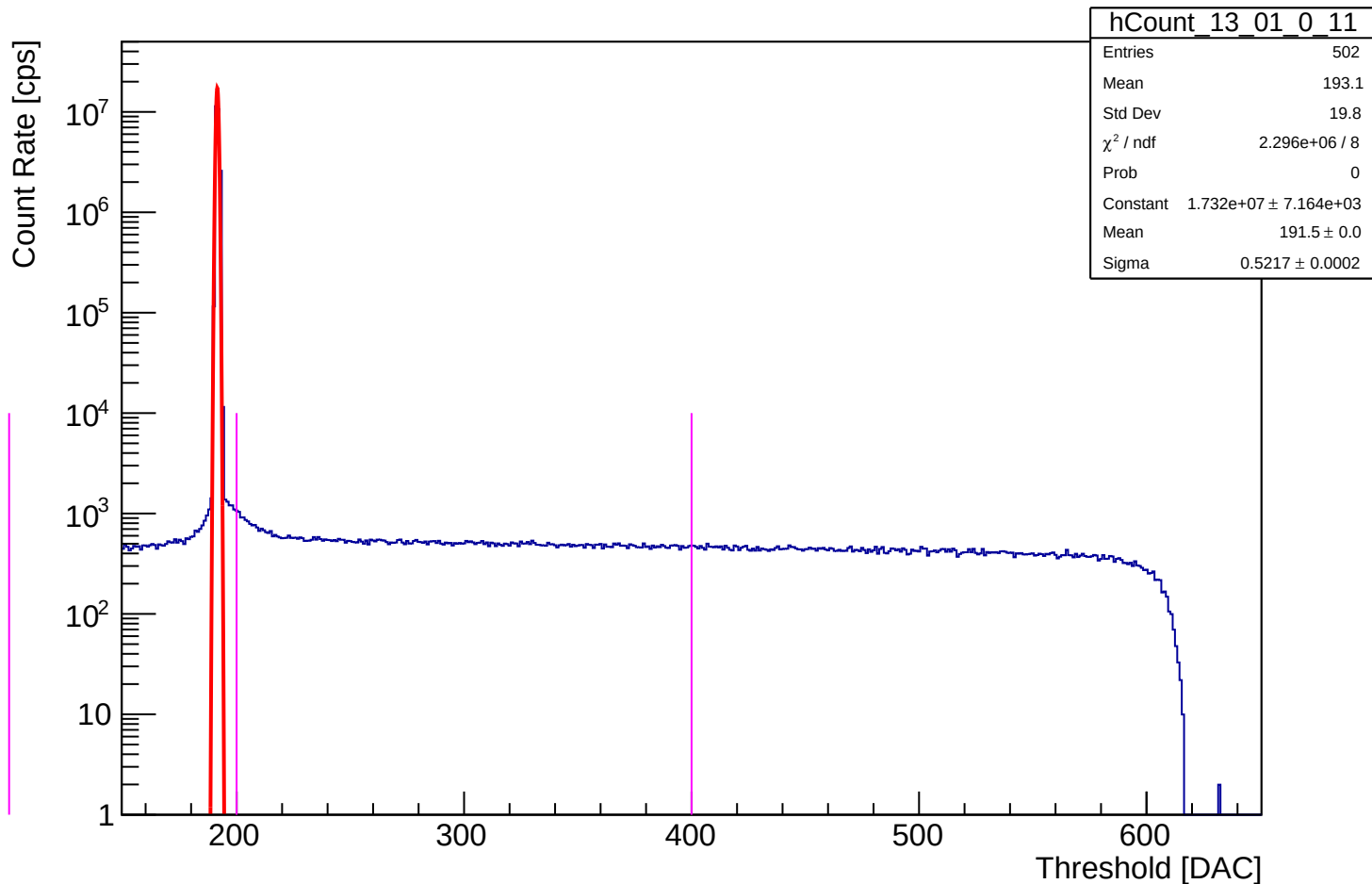


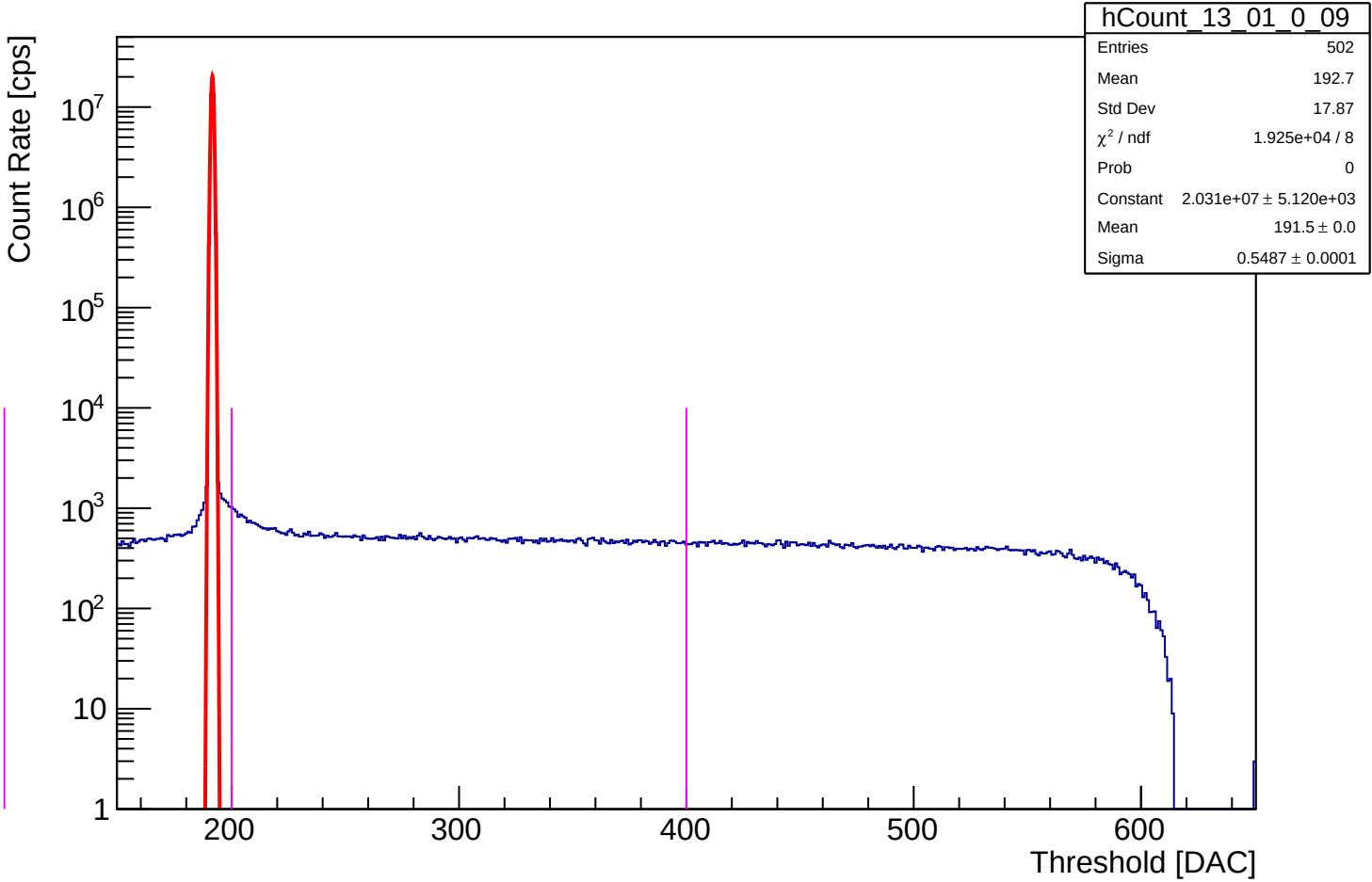
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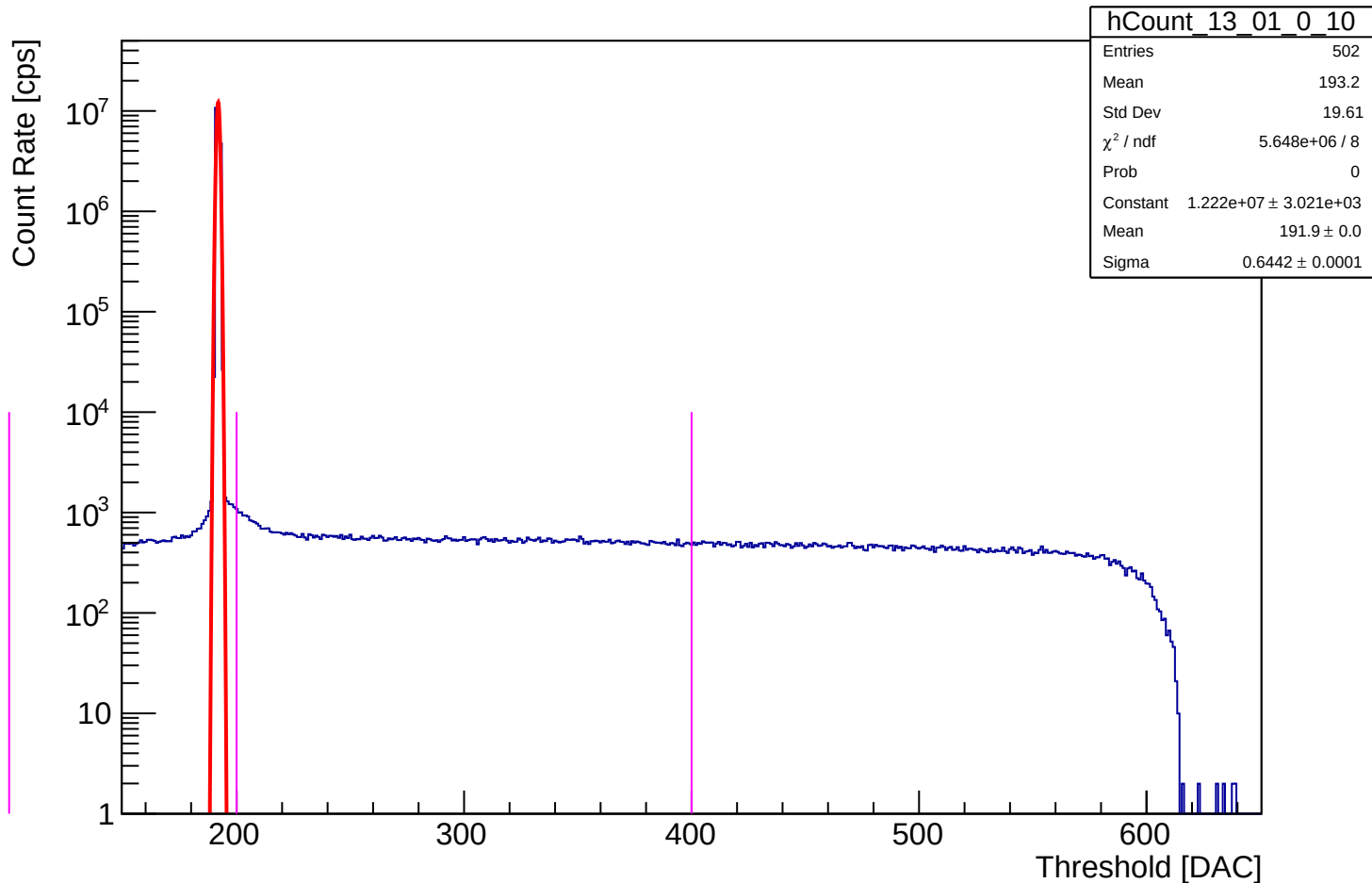


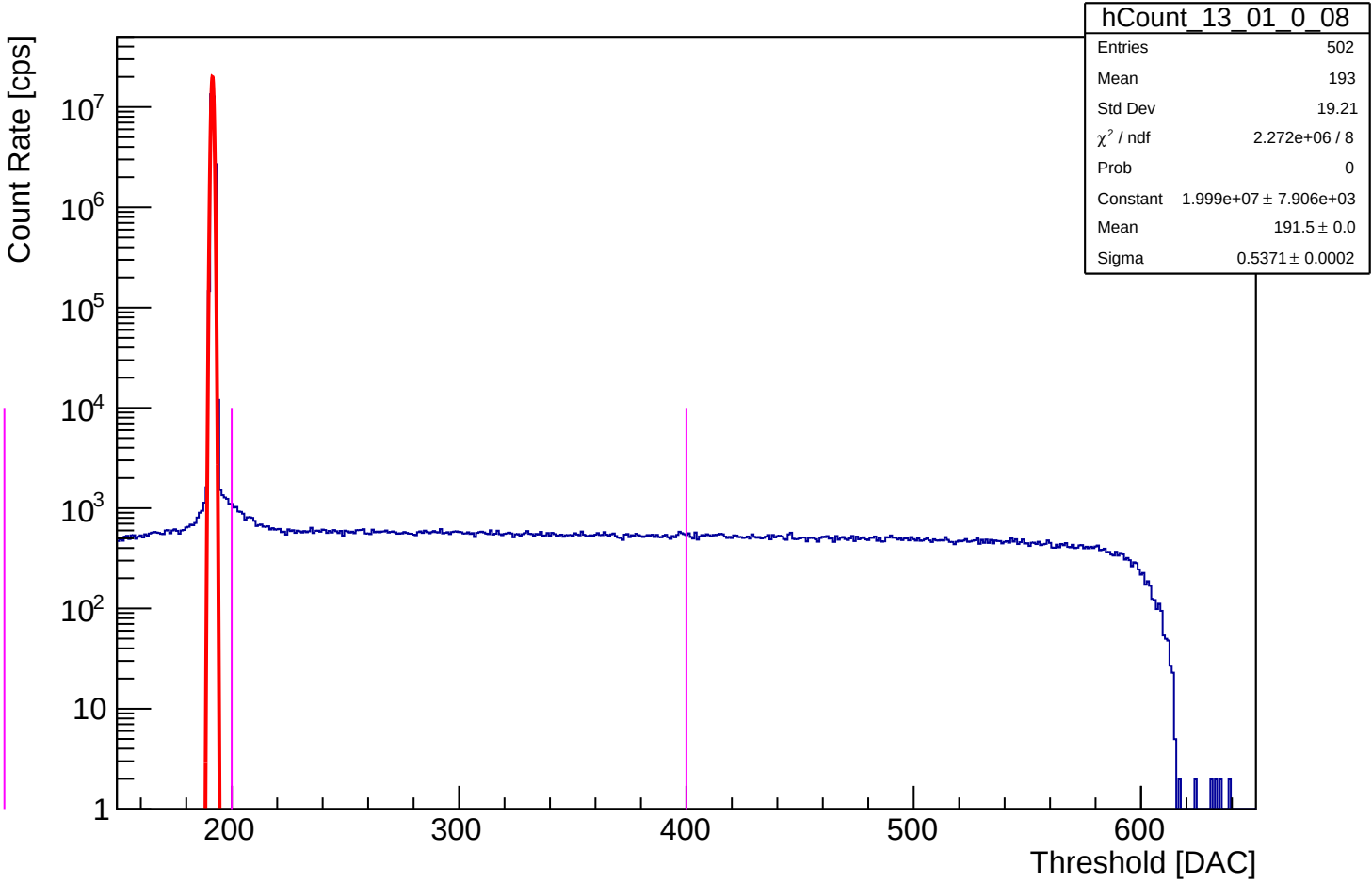
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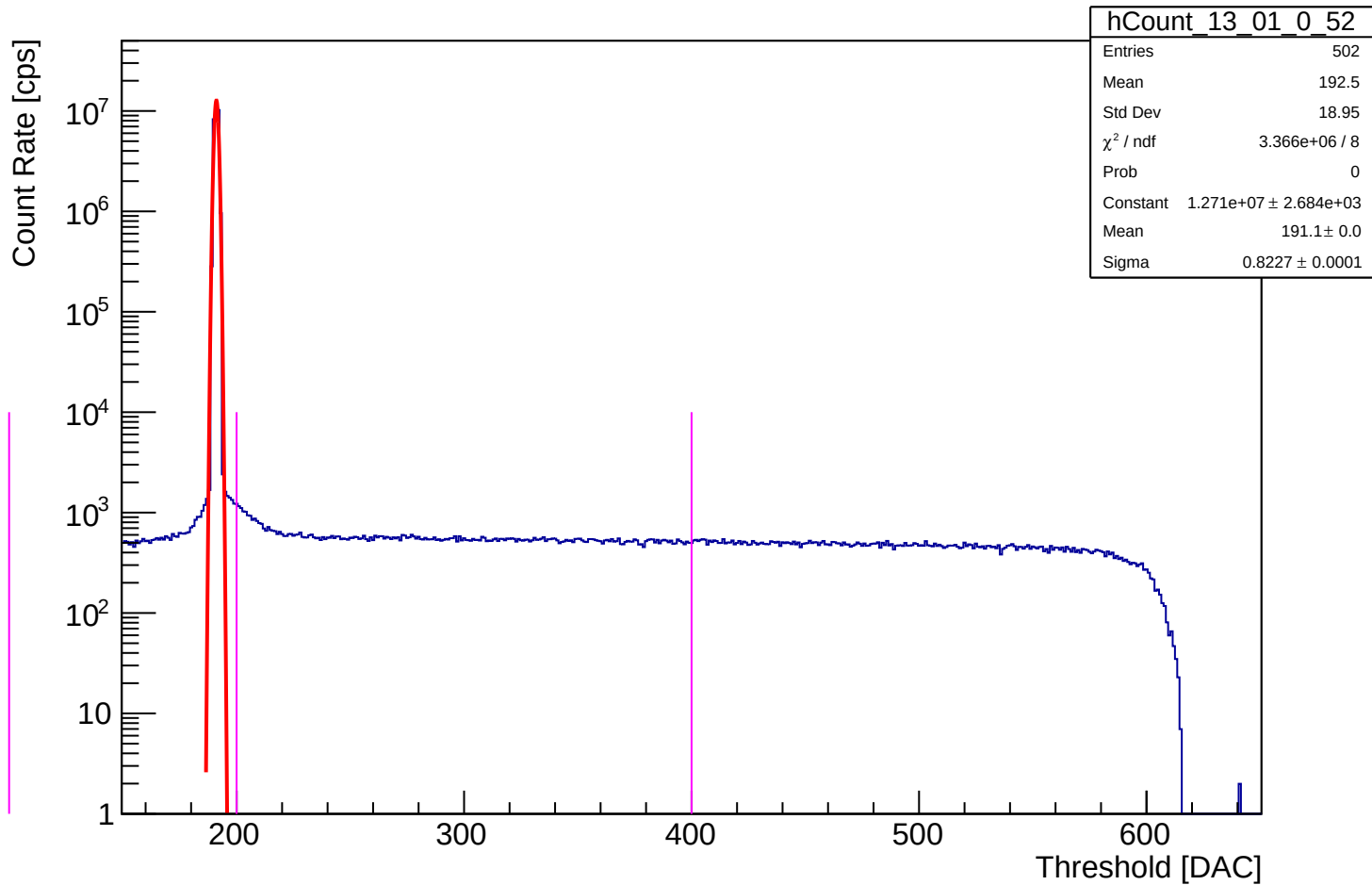


Row 1 Tile 1 Pmt 4 Pixel 43 Slot 13 Fiber 1 Asic 0 Channel 10

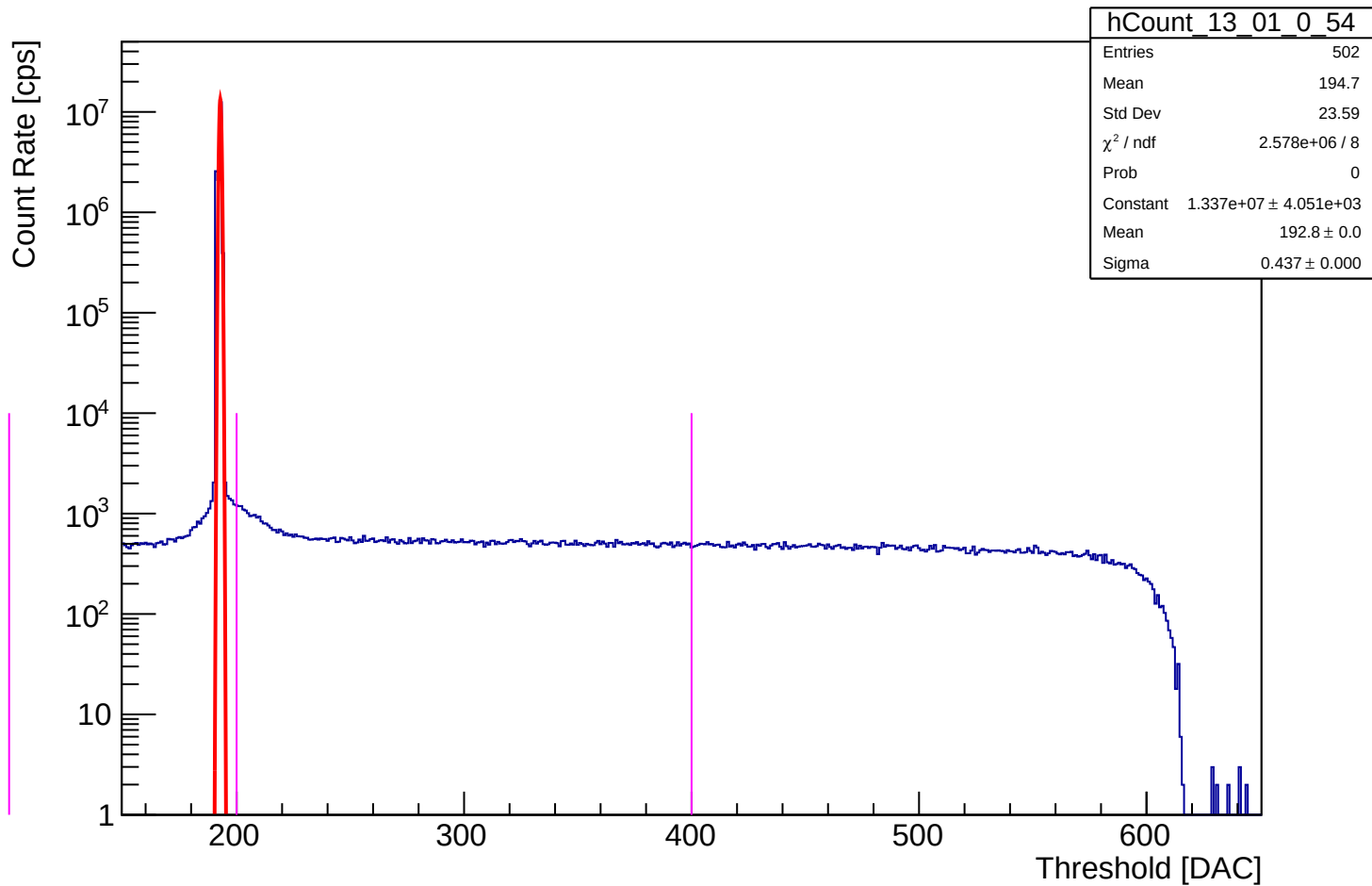




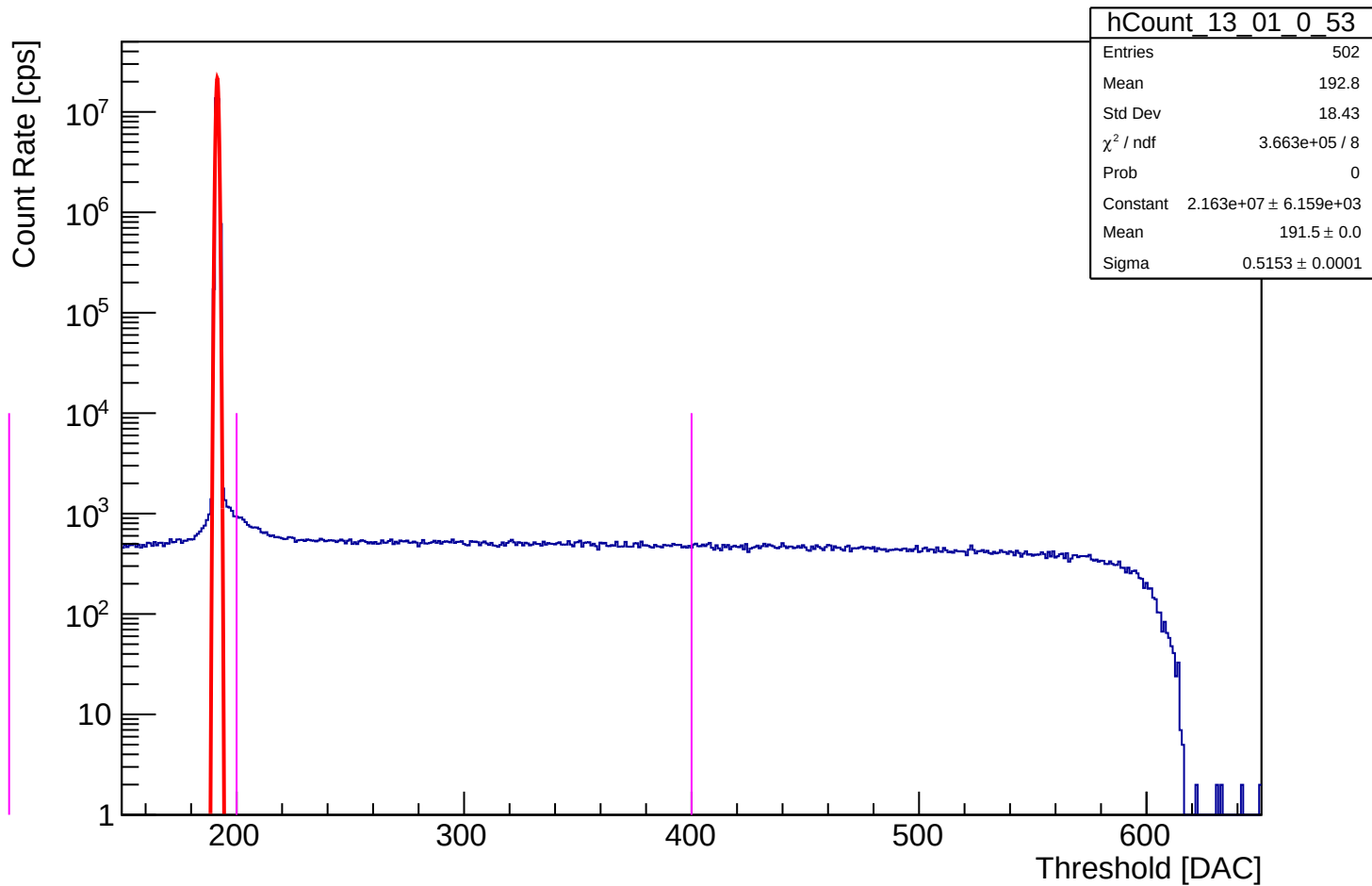
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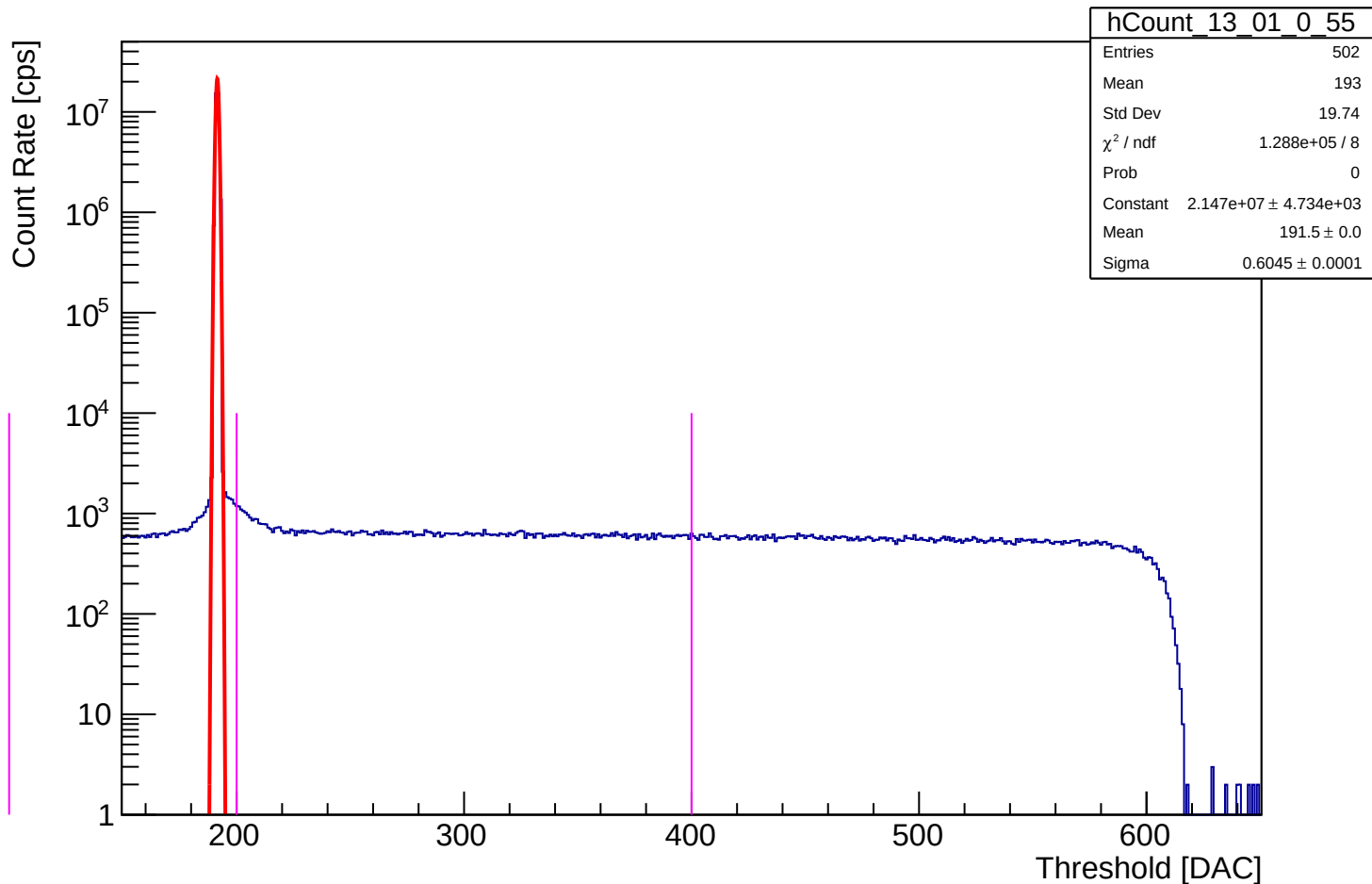
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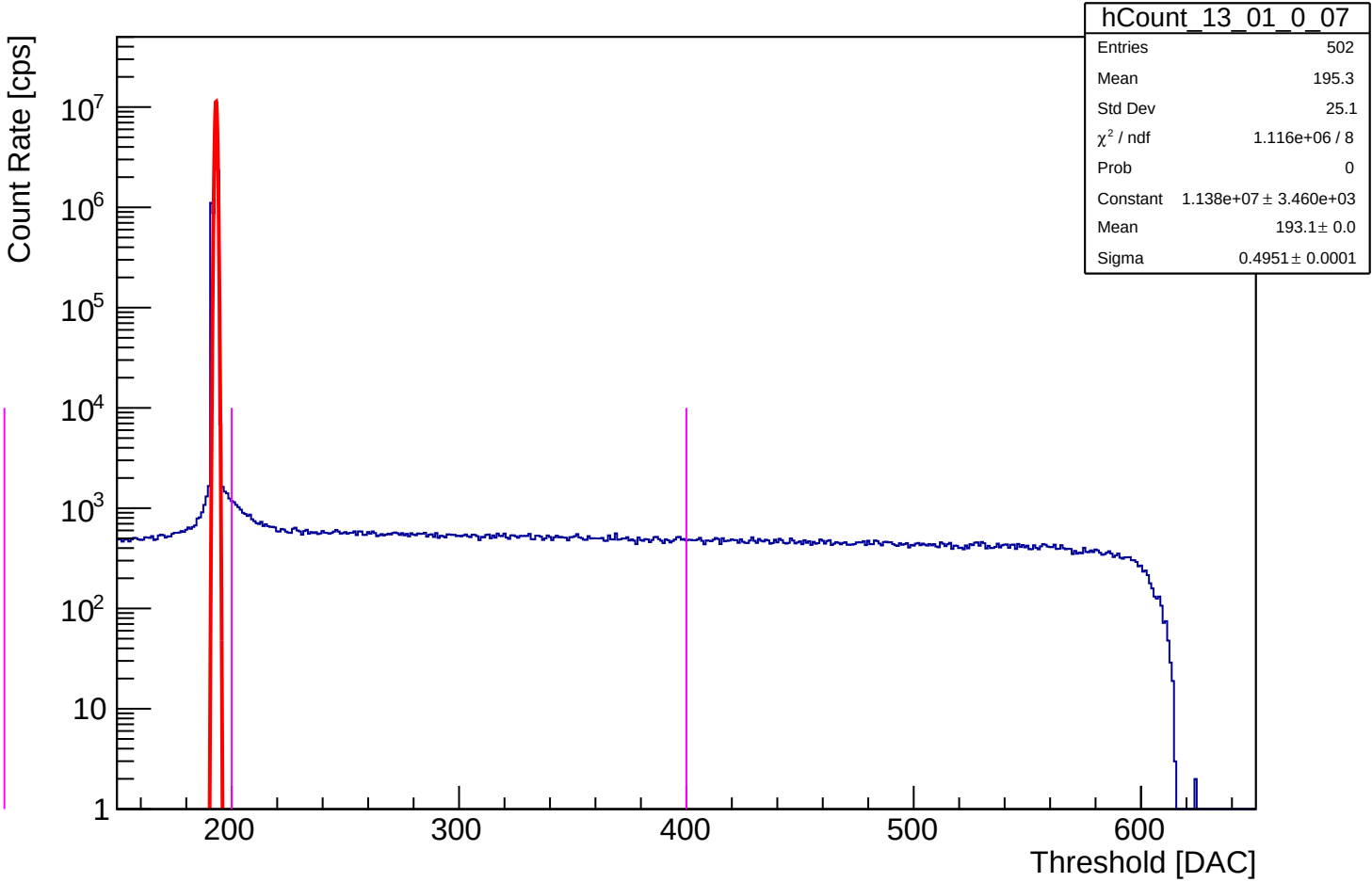


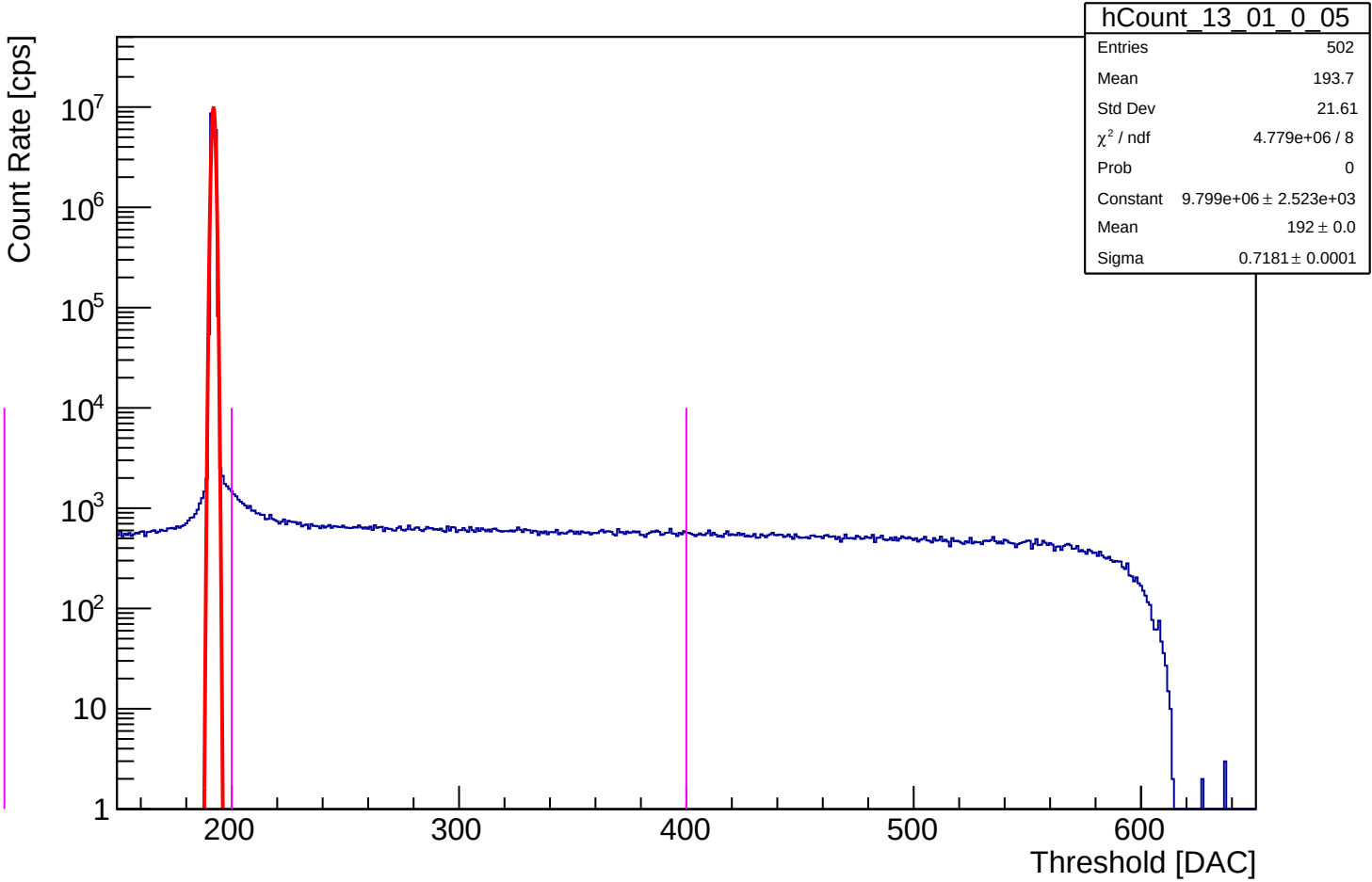
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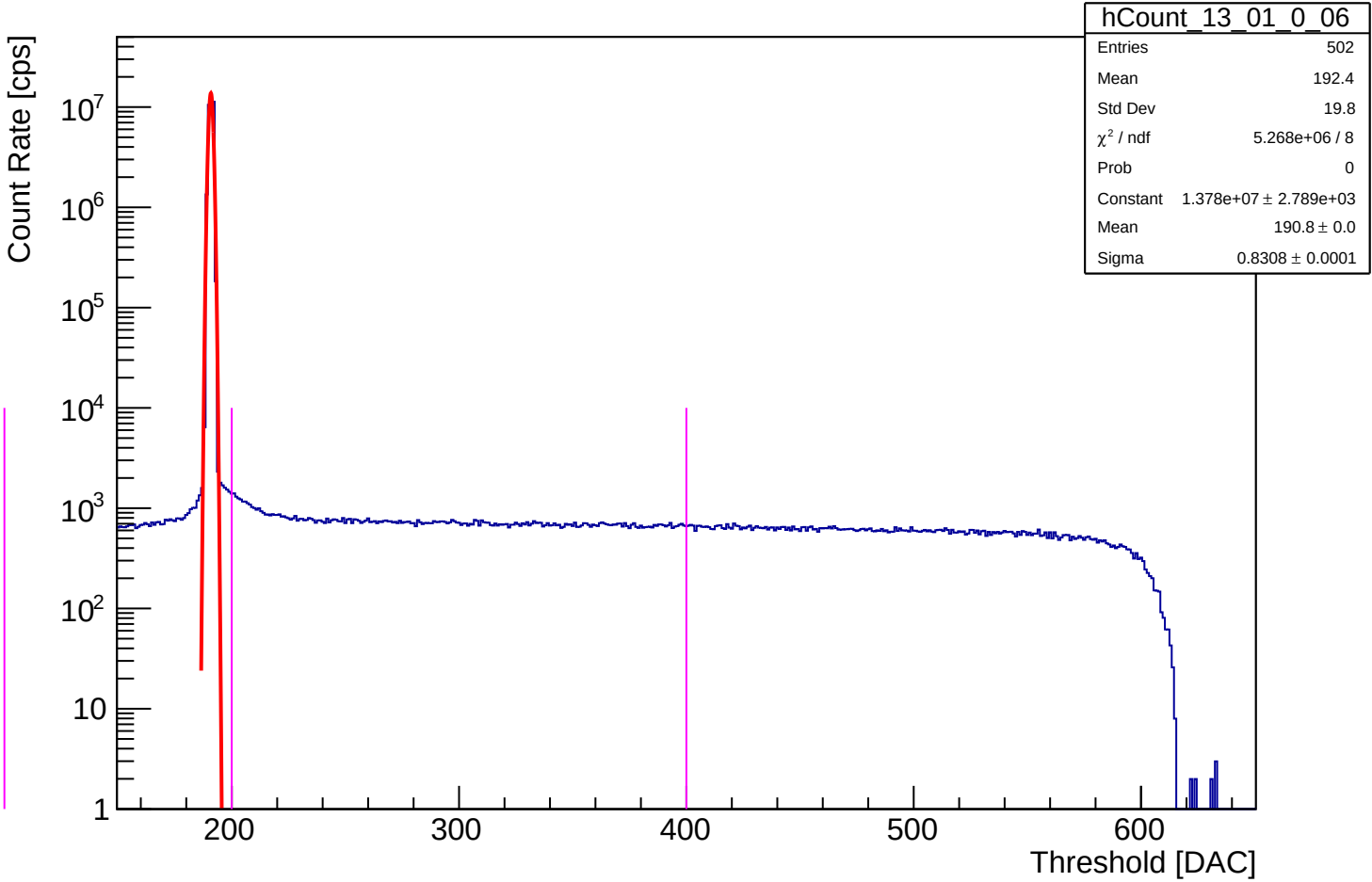


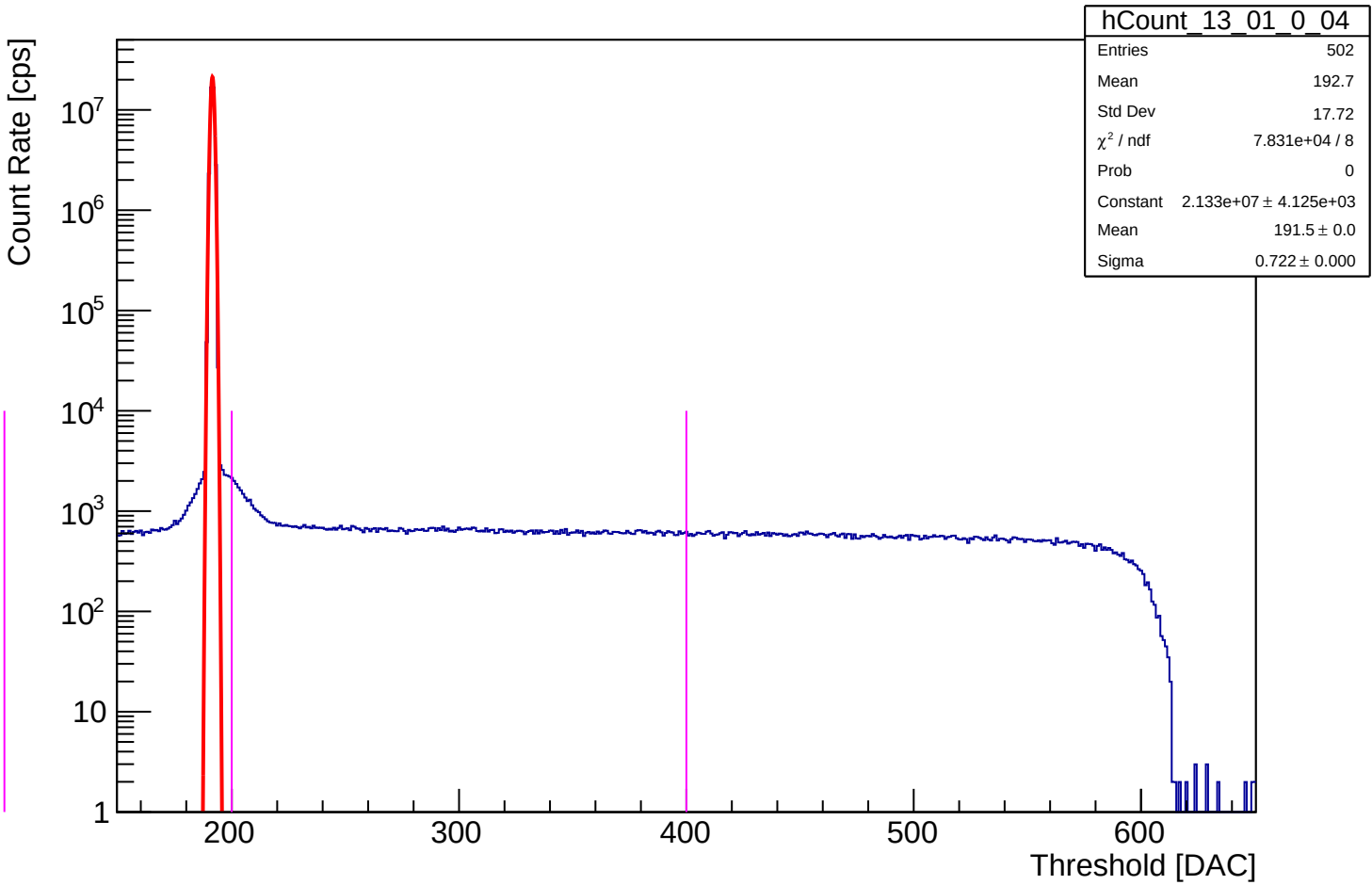
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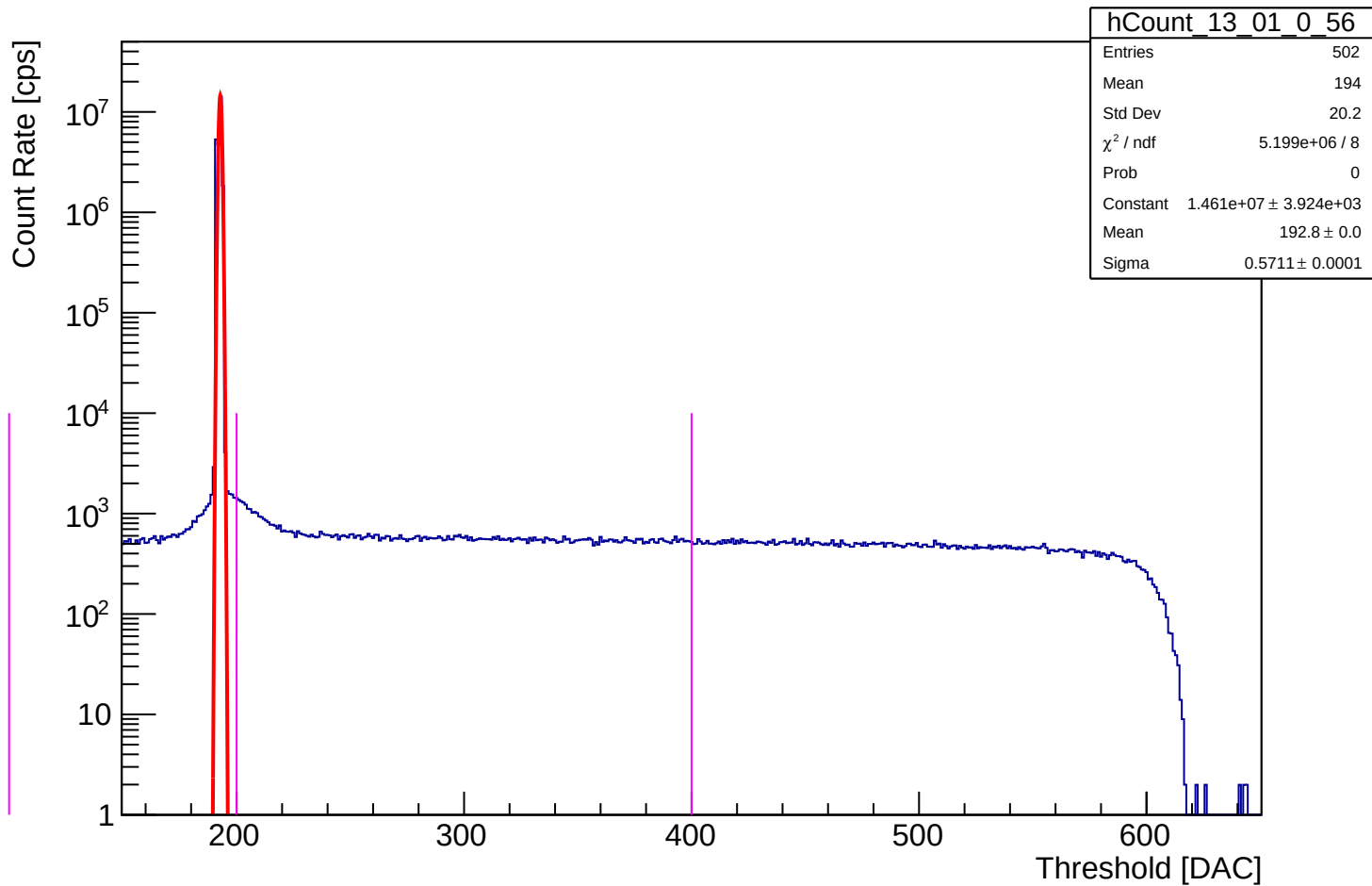




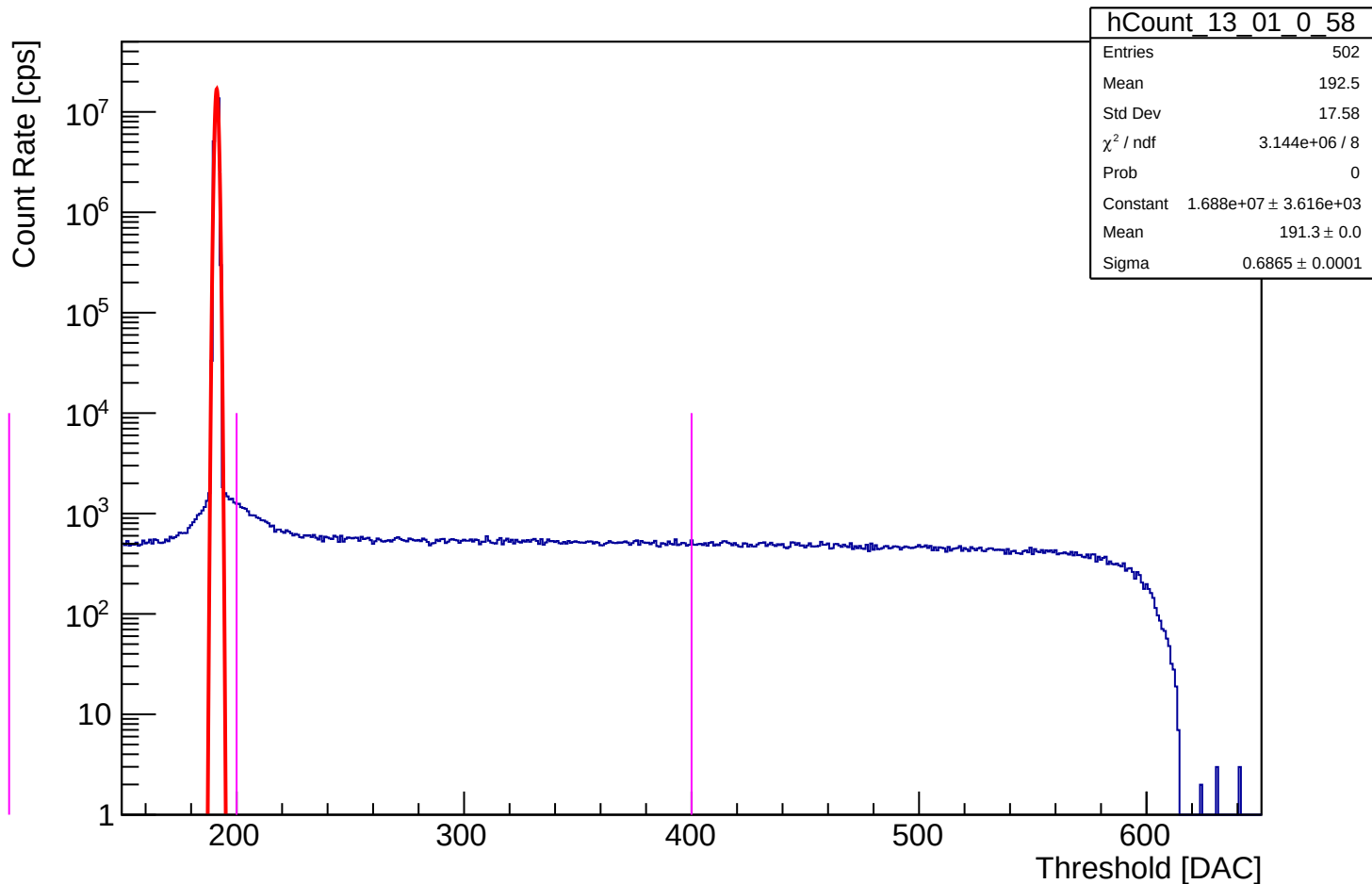




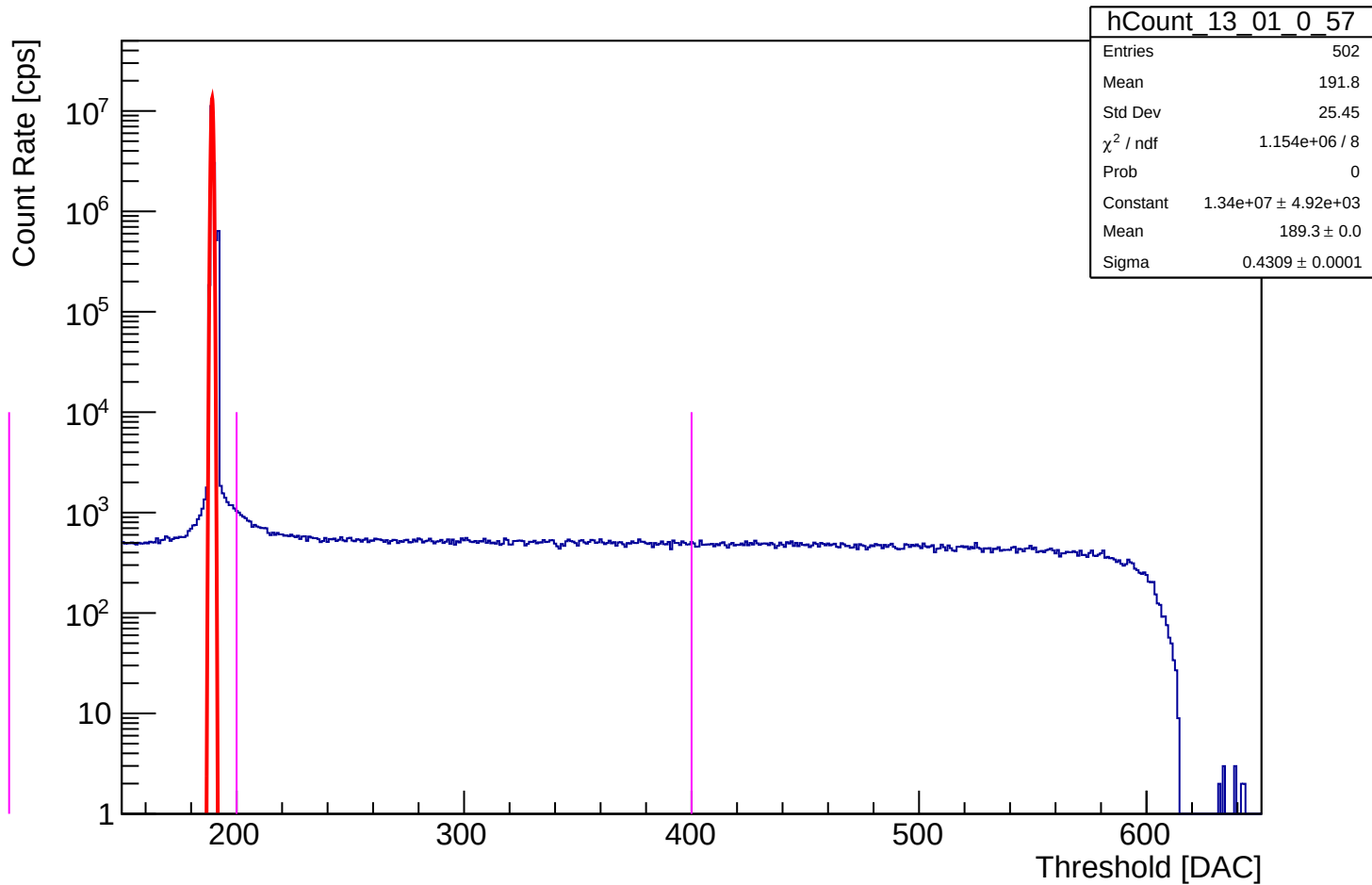
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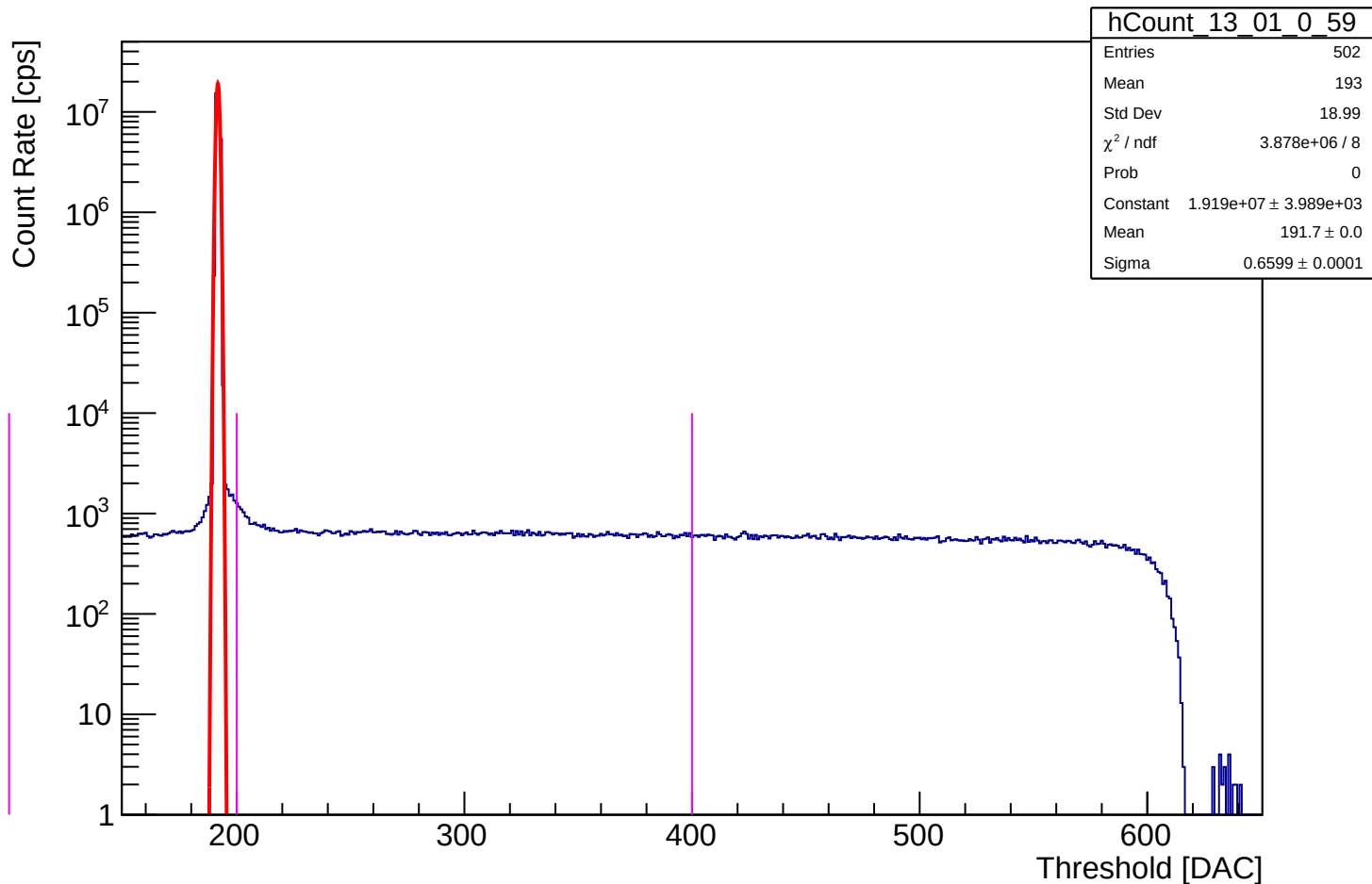
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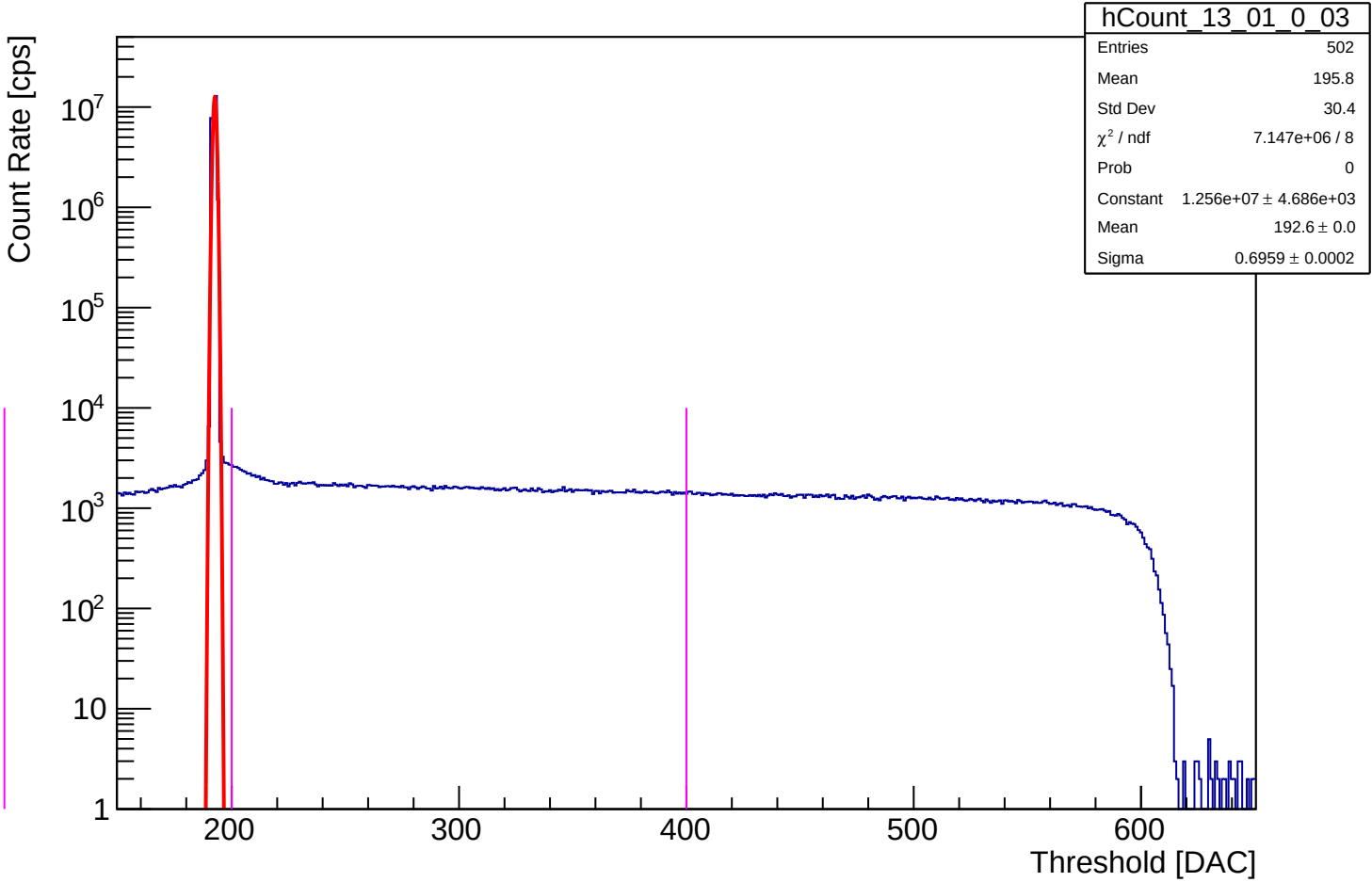


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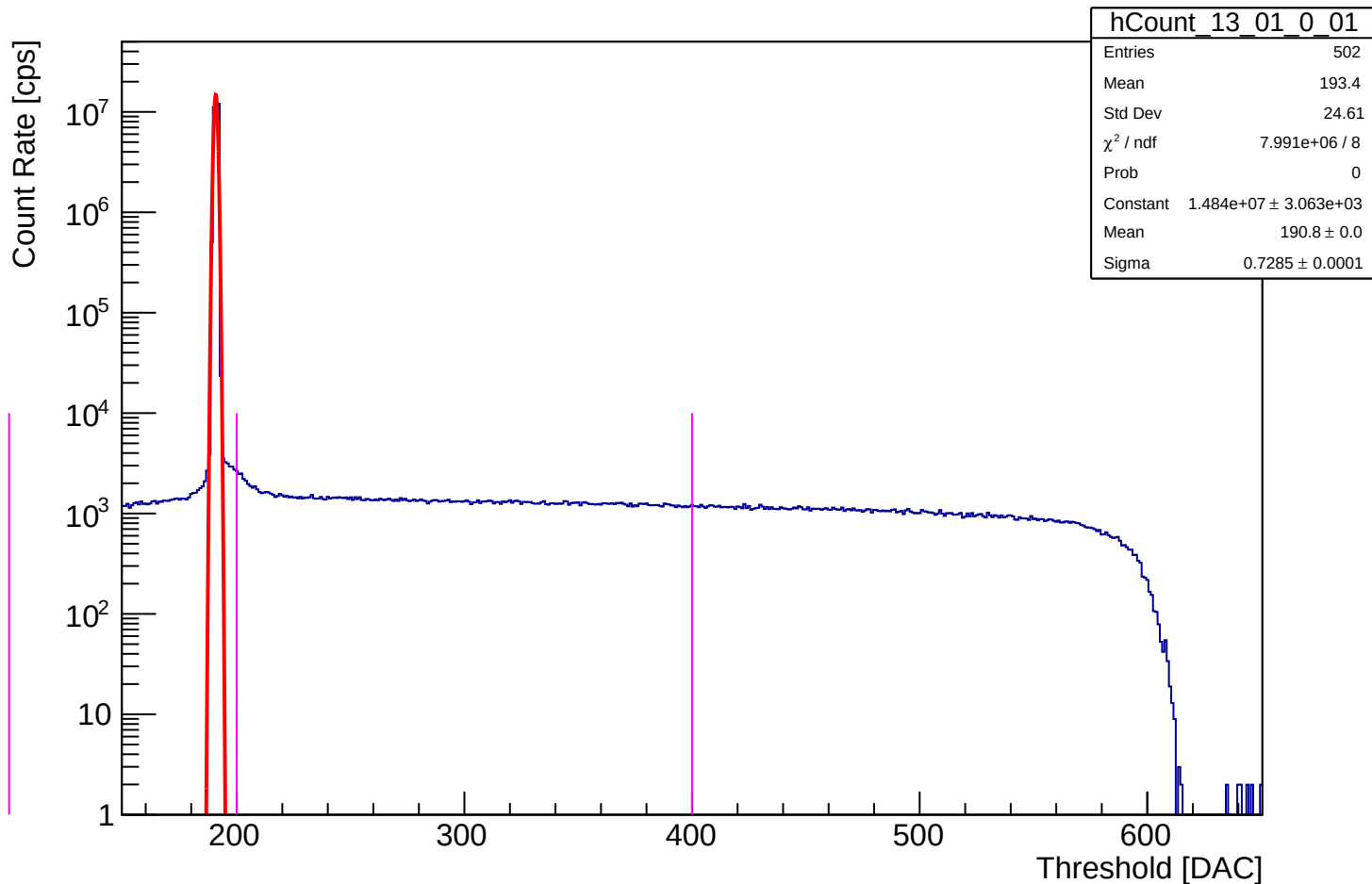


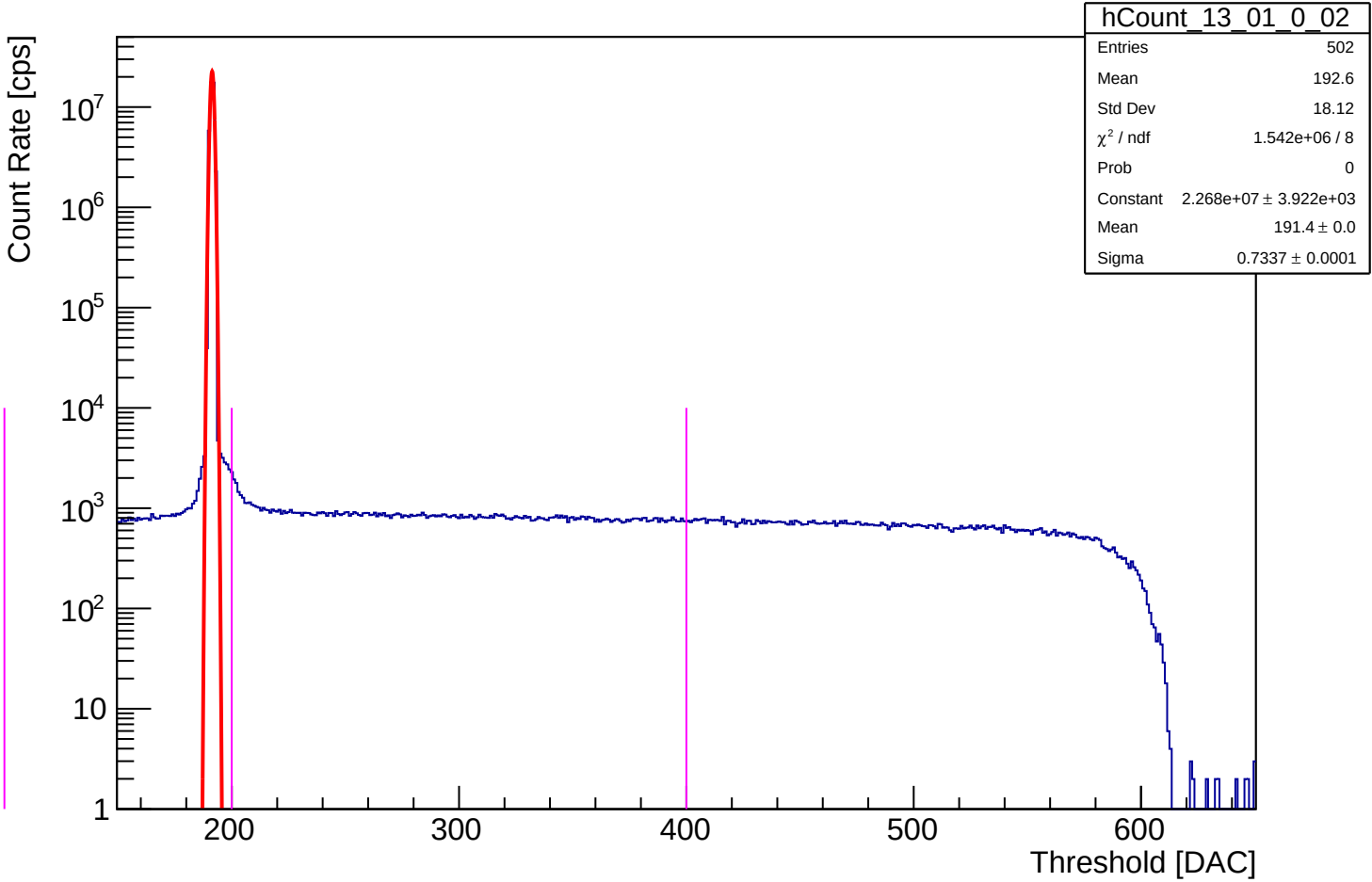
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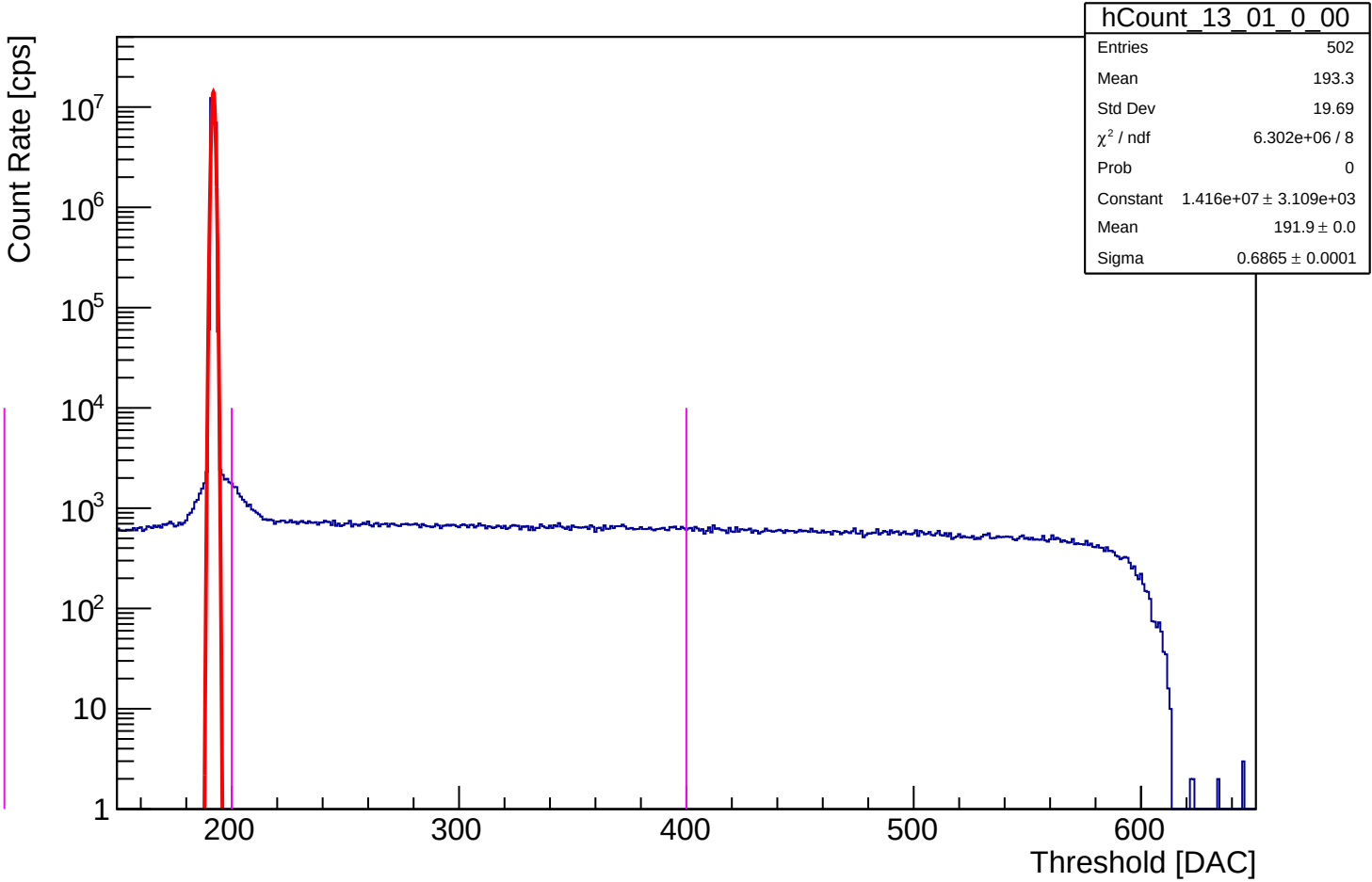




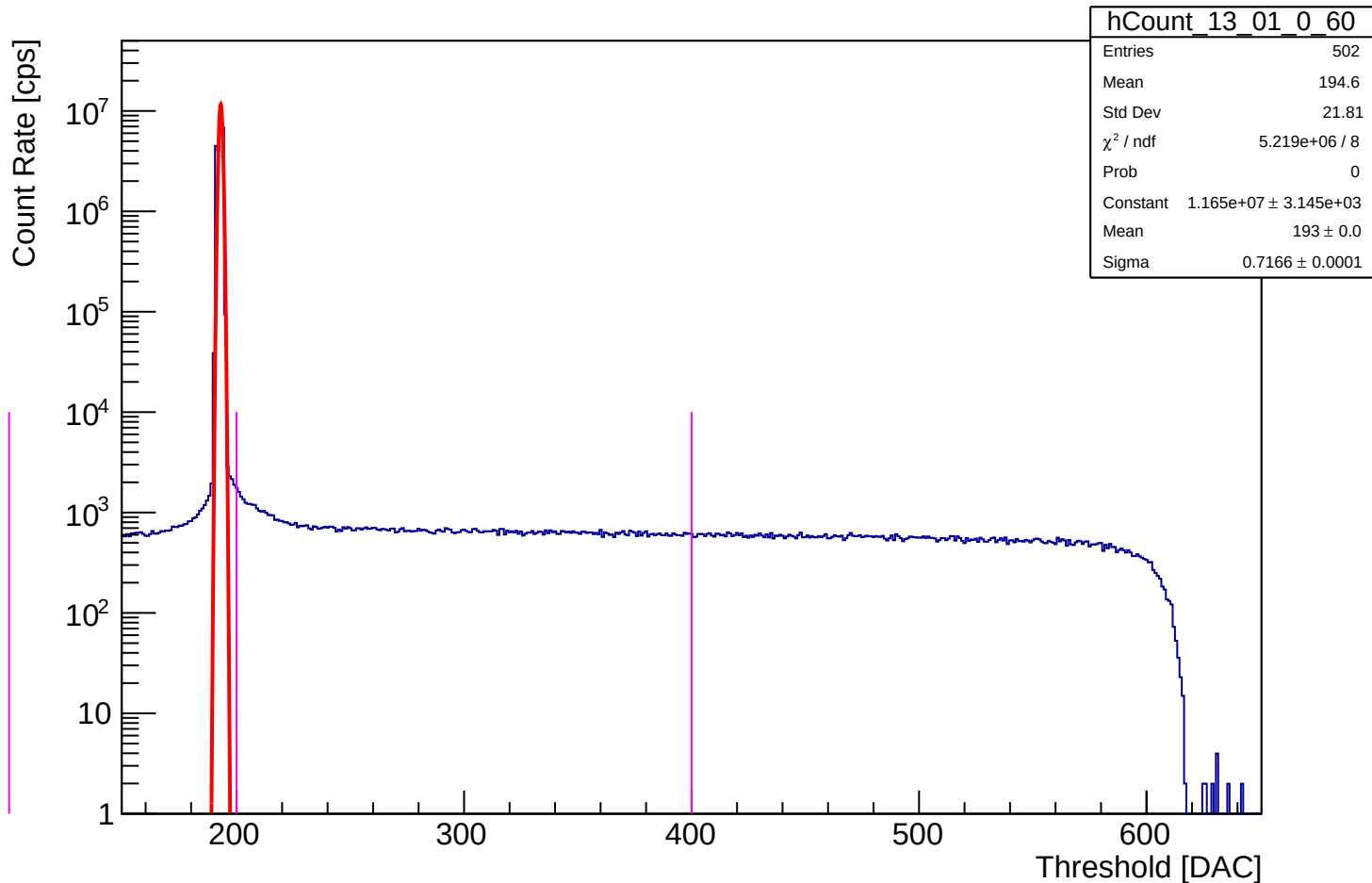
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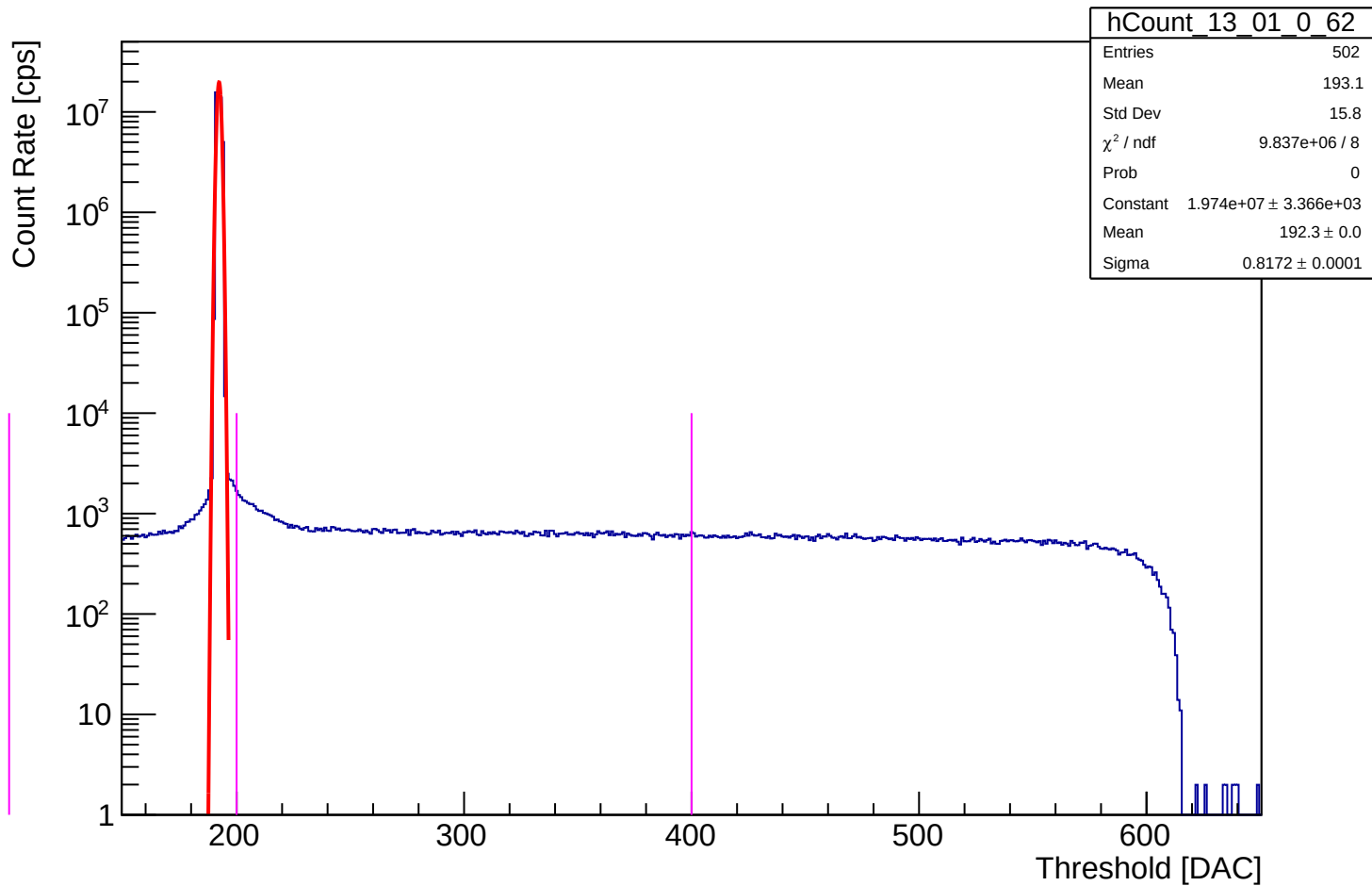




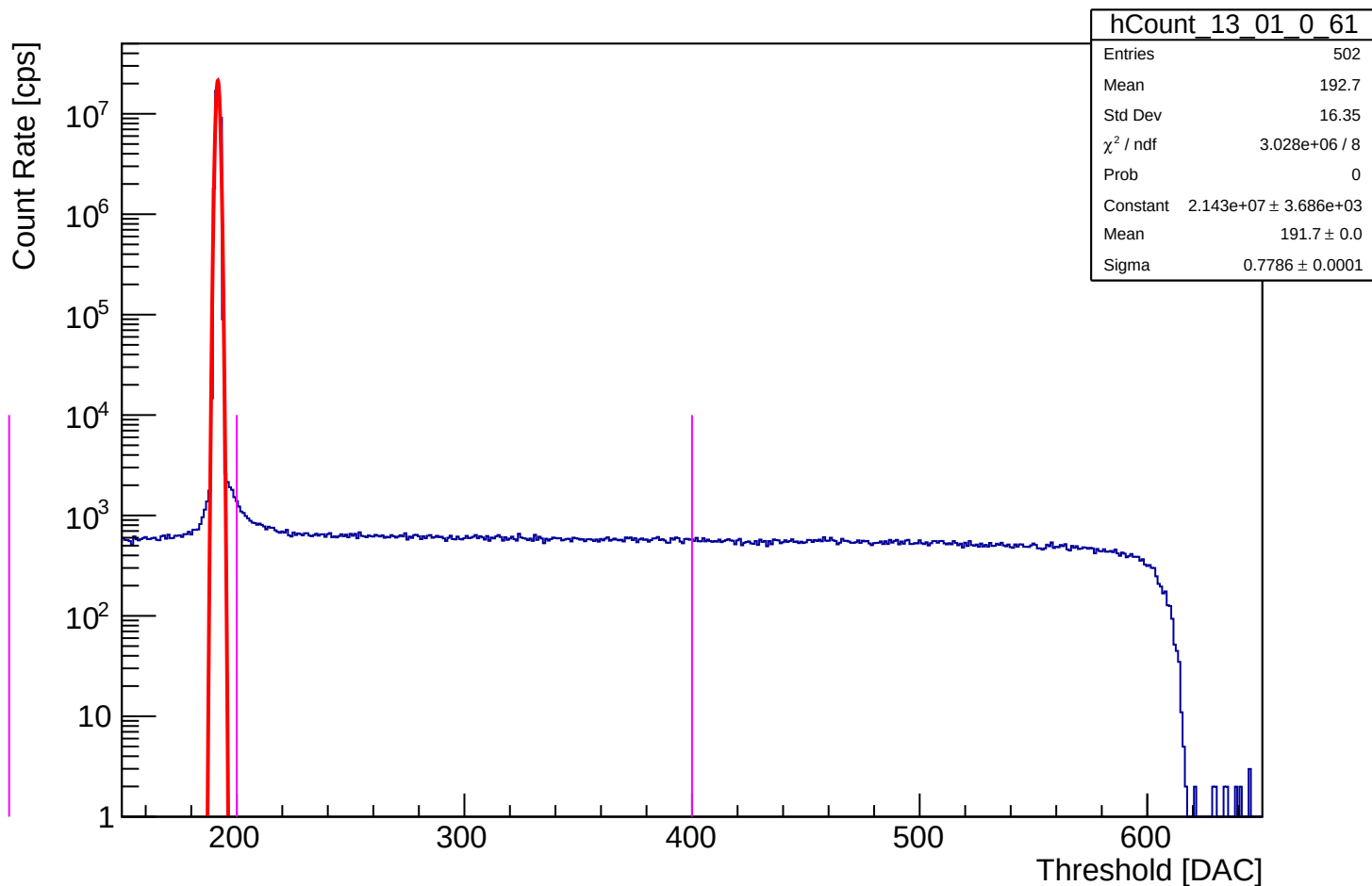
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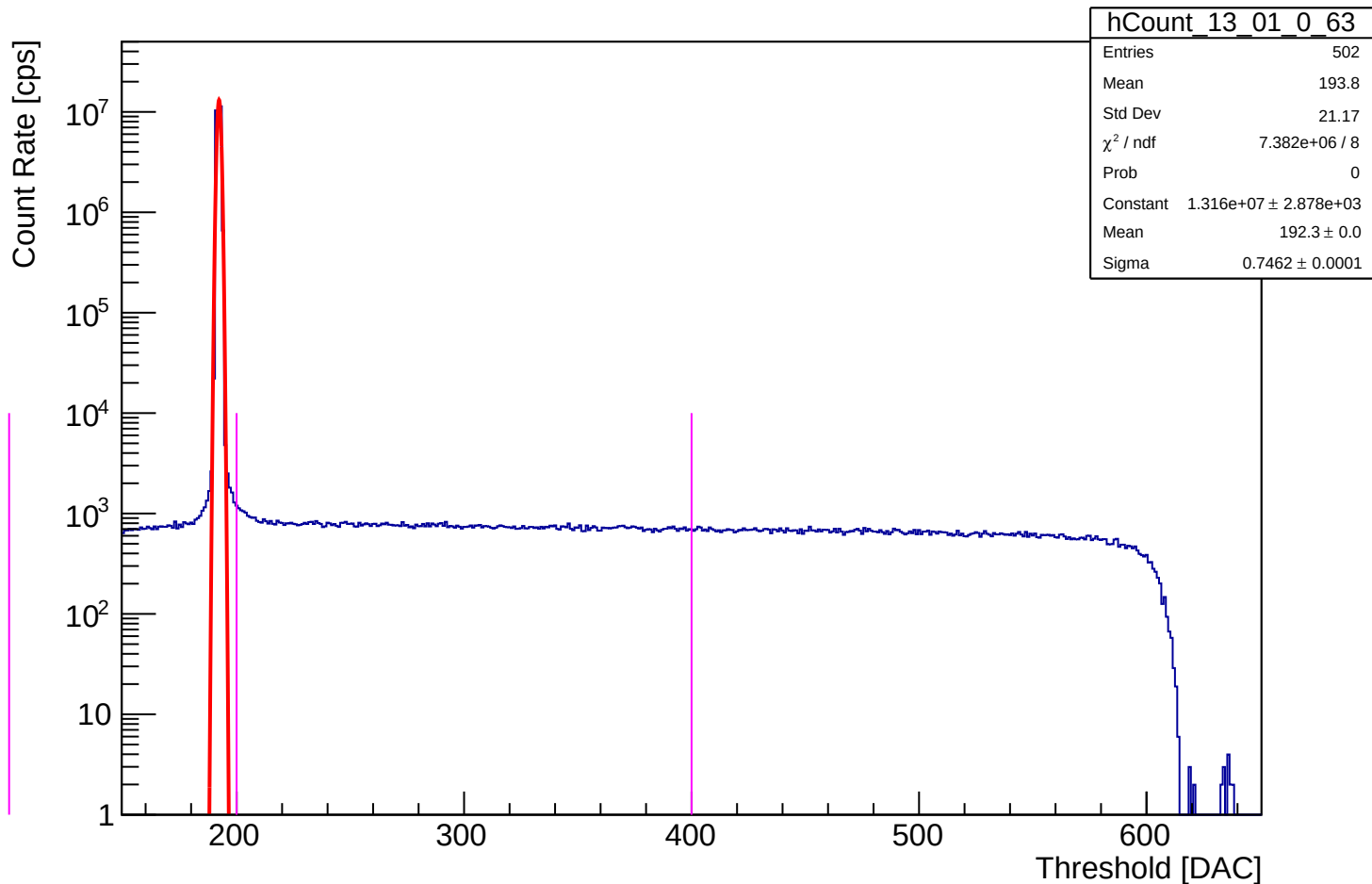
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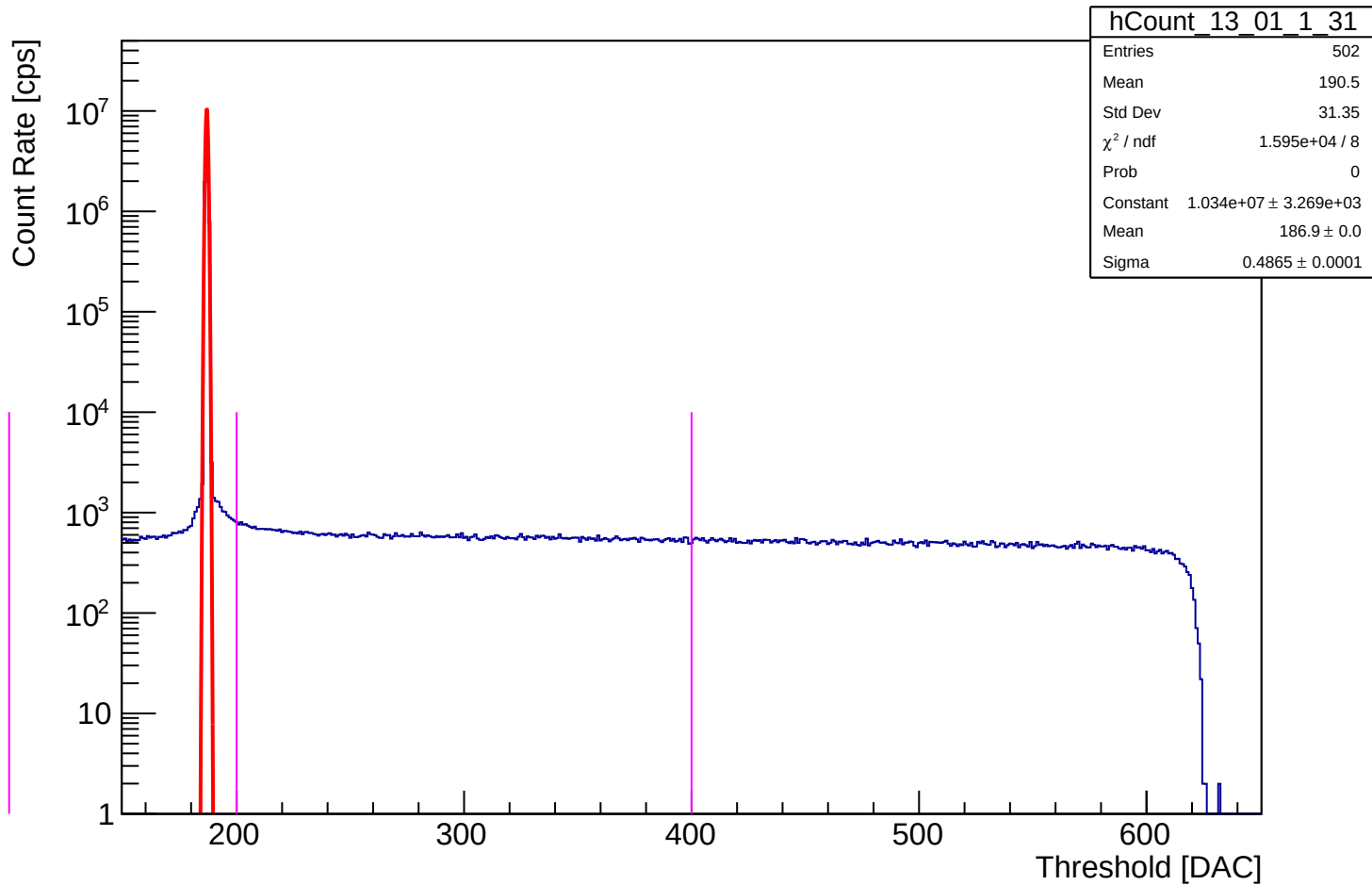
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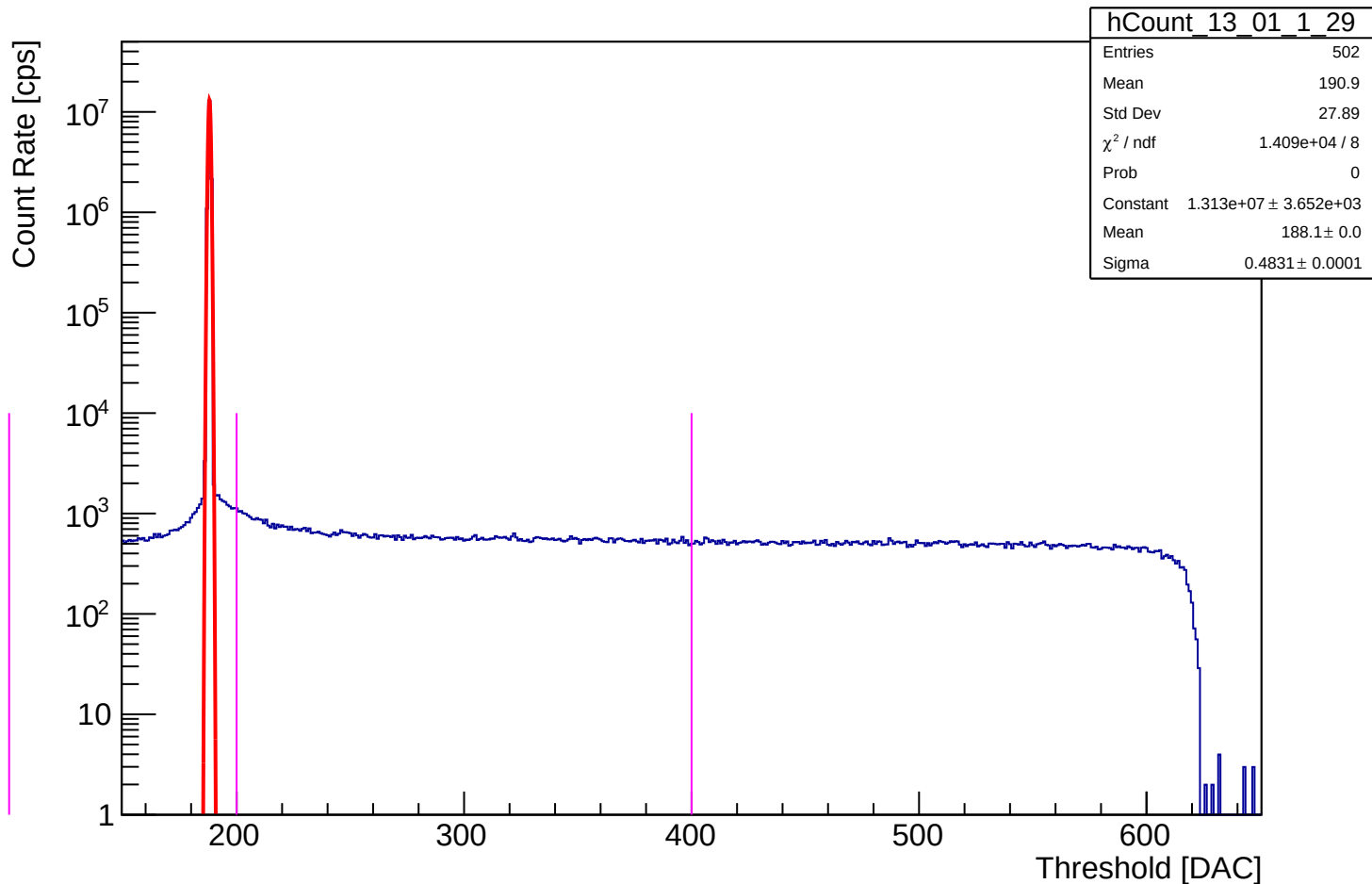
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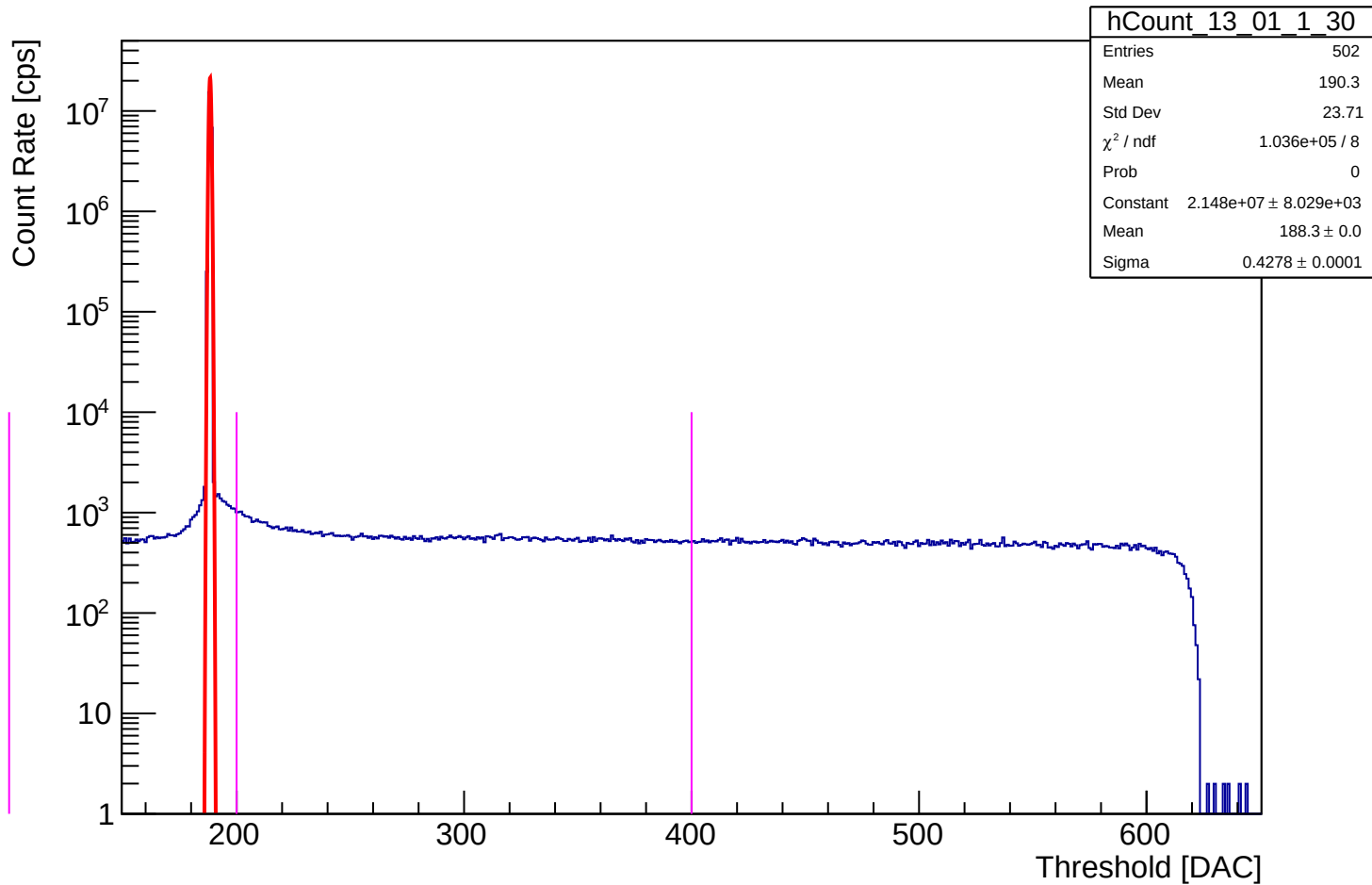
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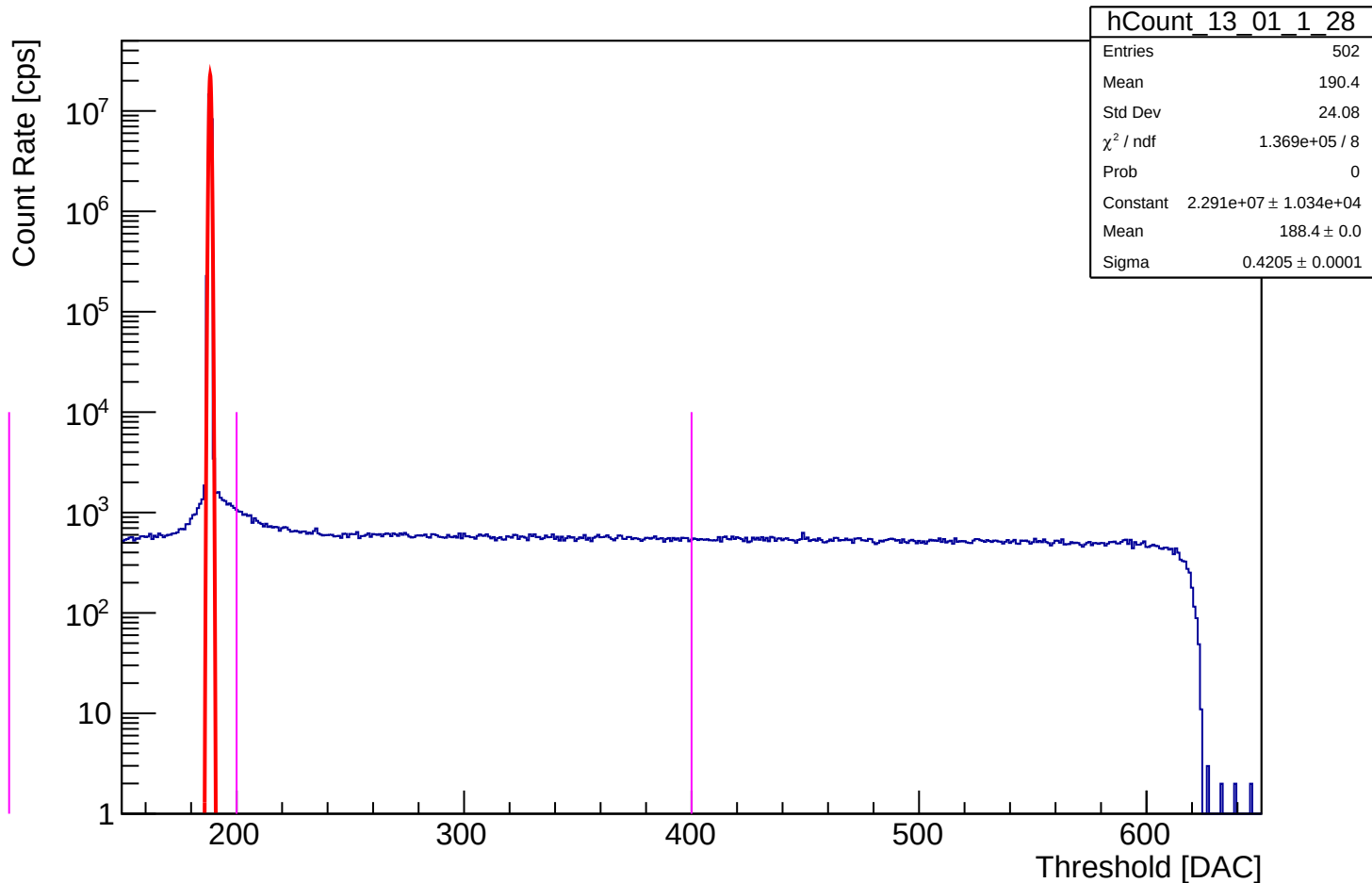
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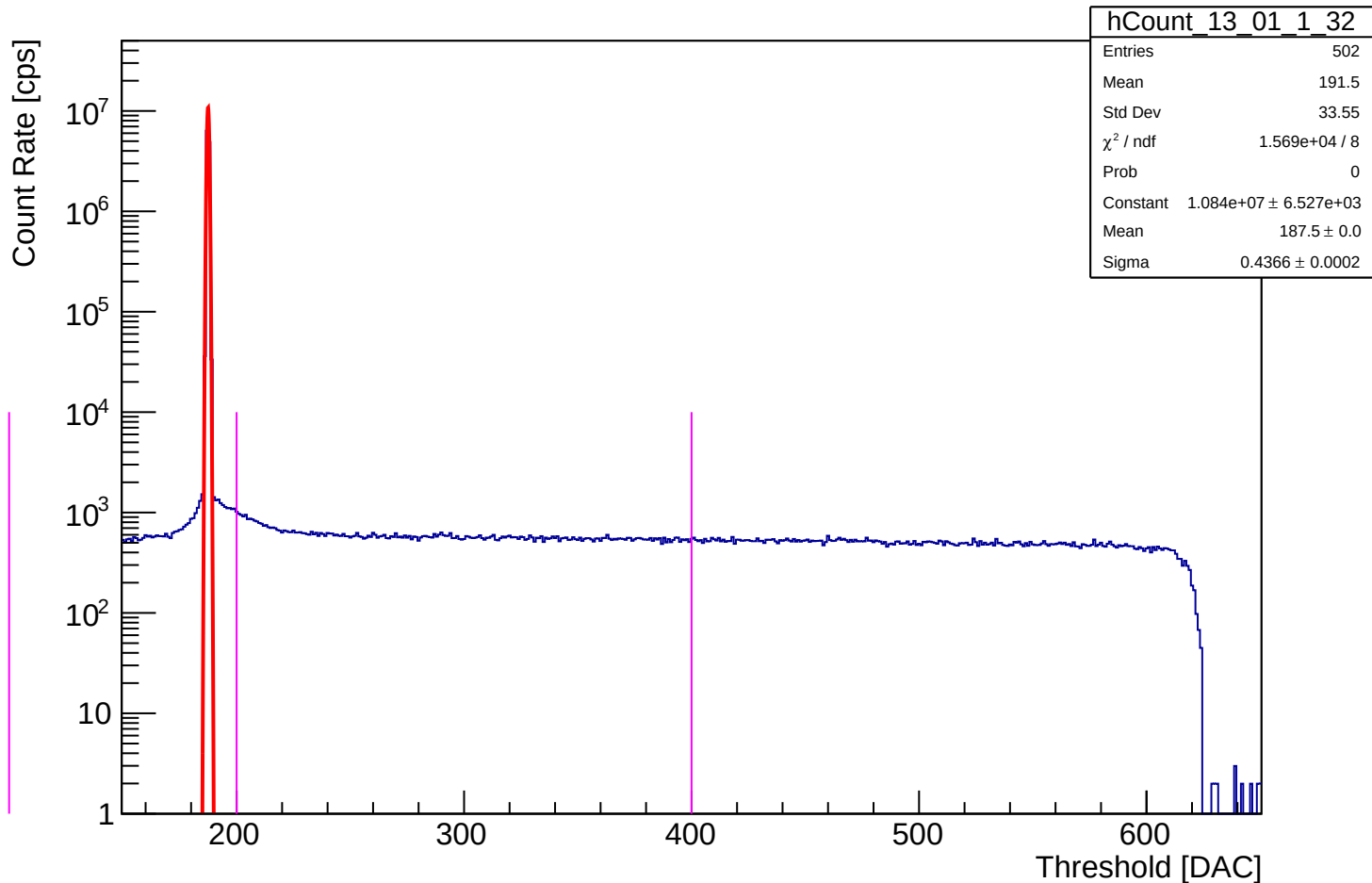
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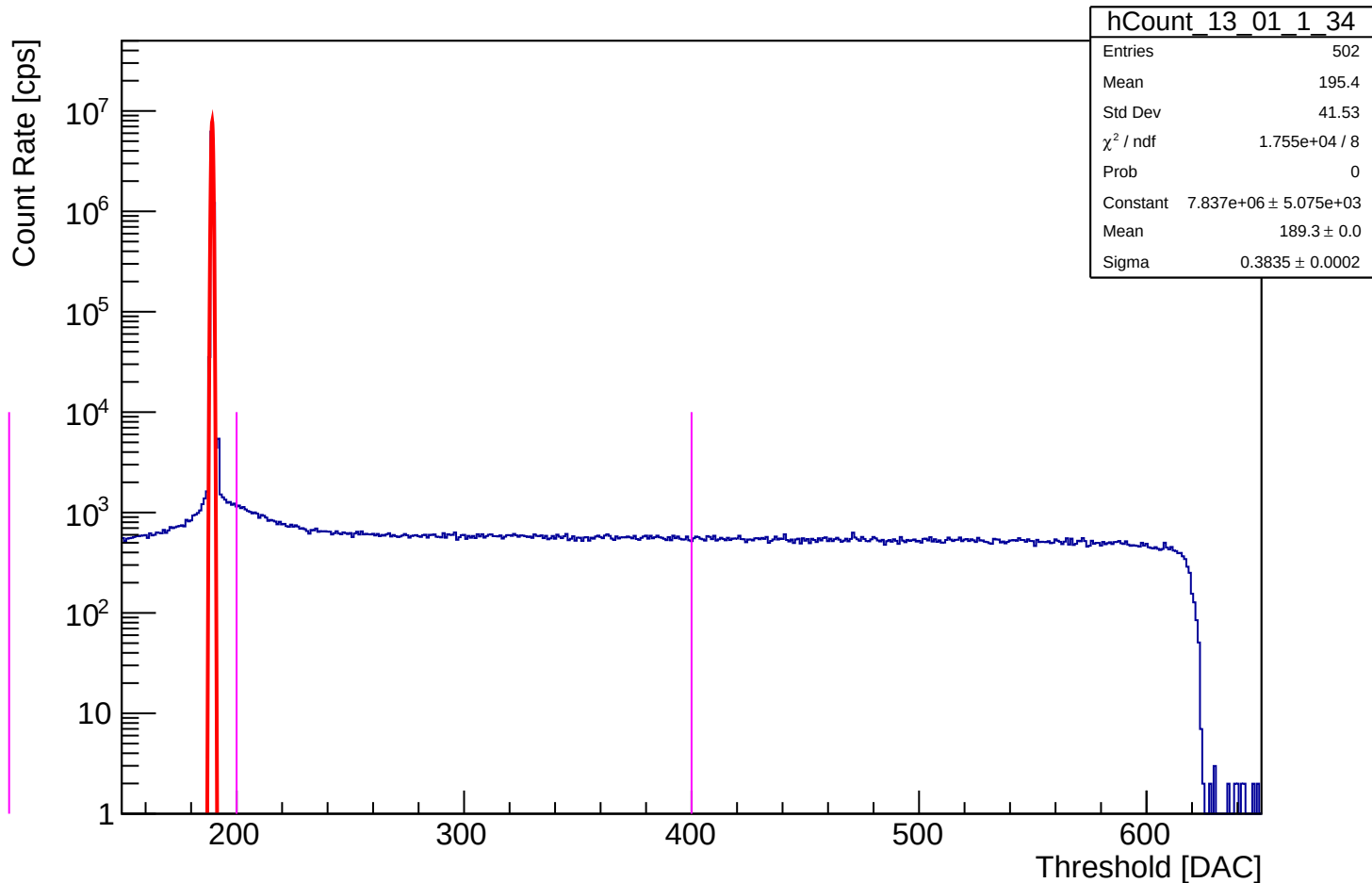
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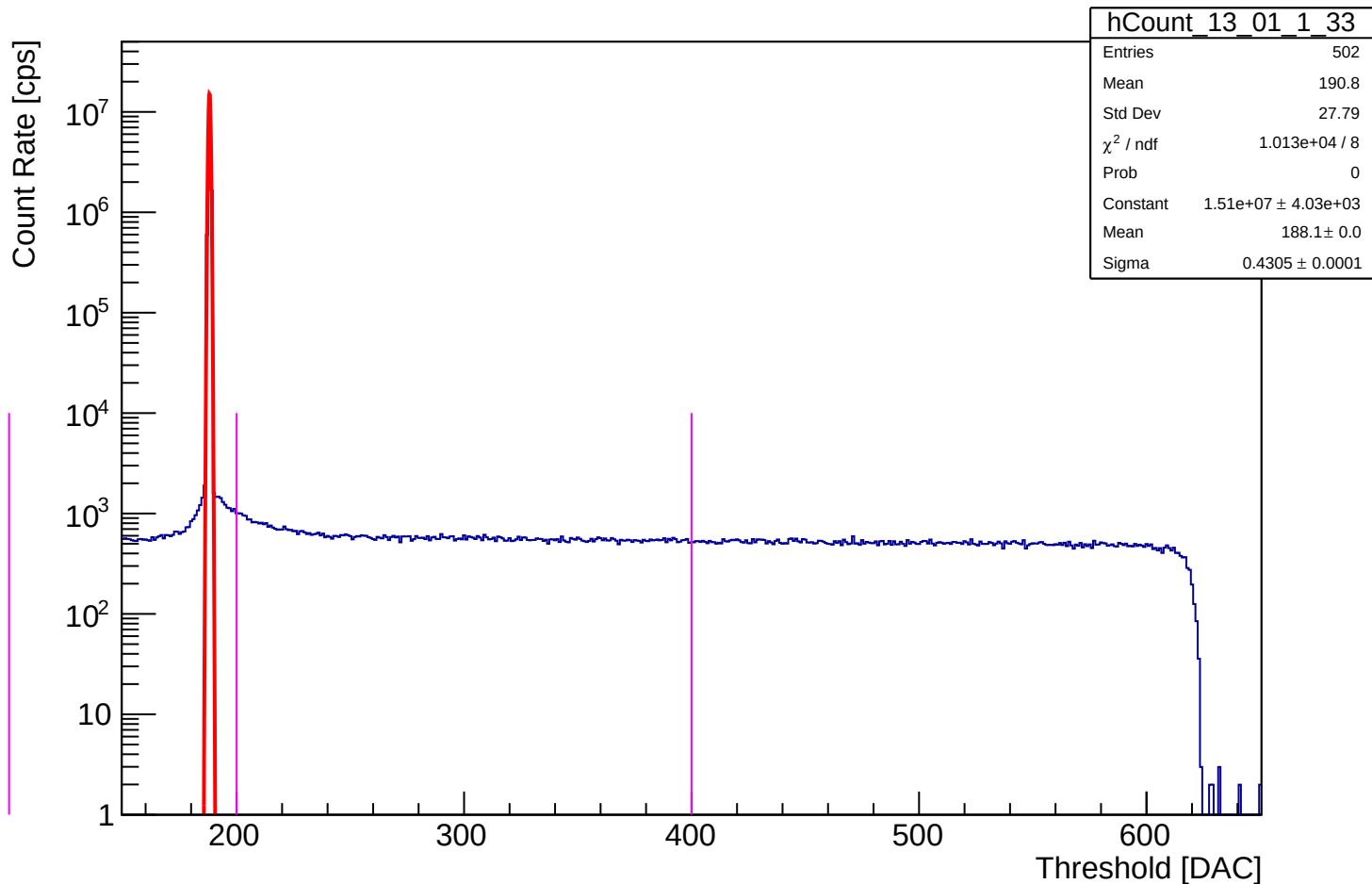
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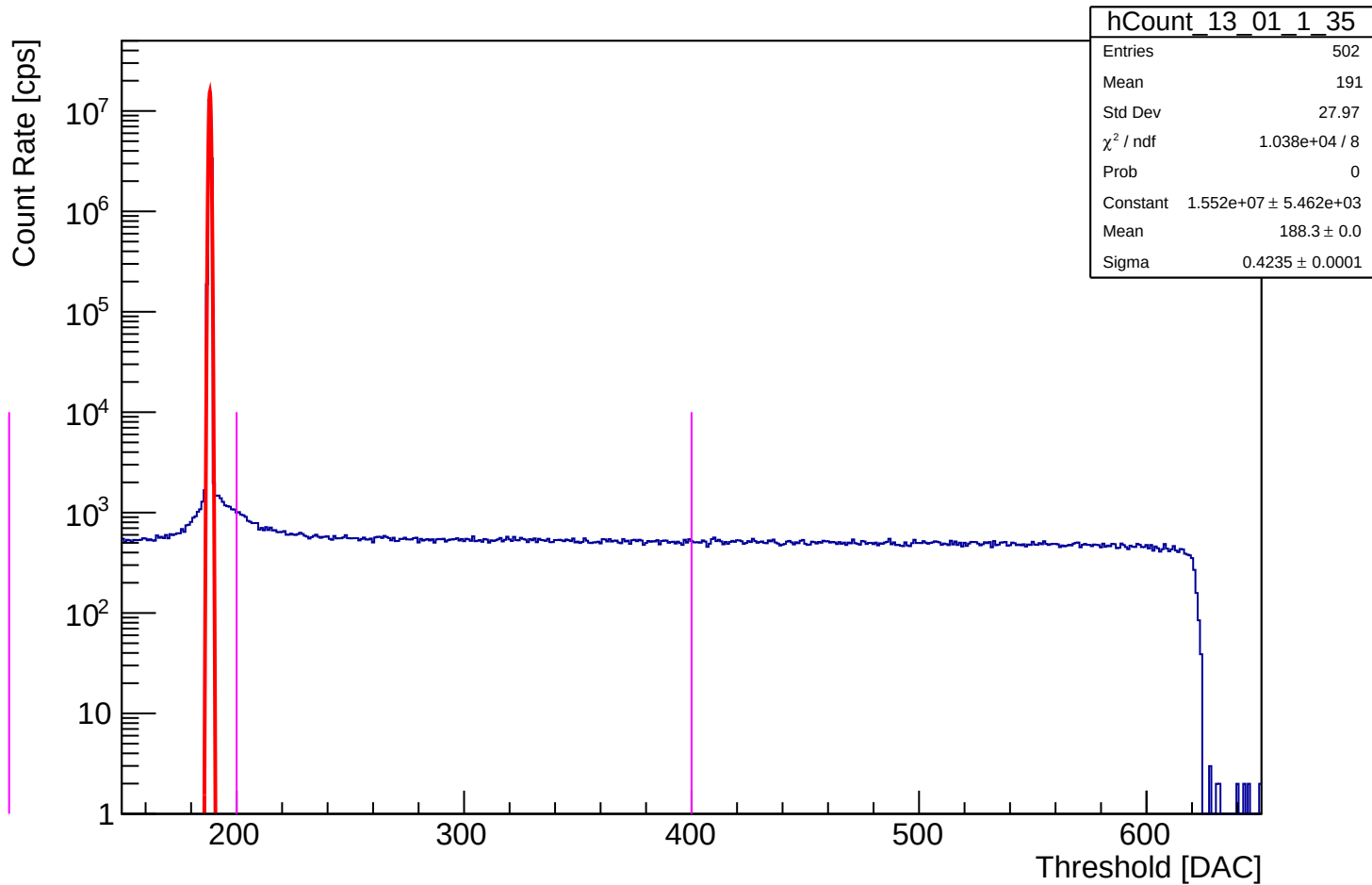
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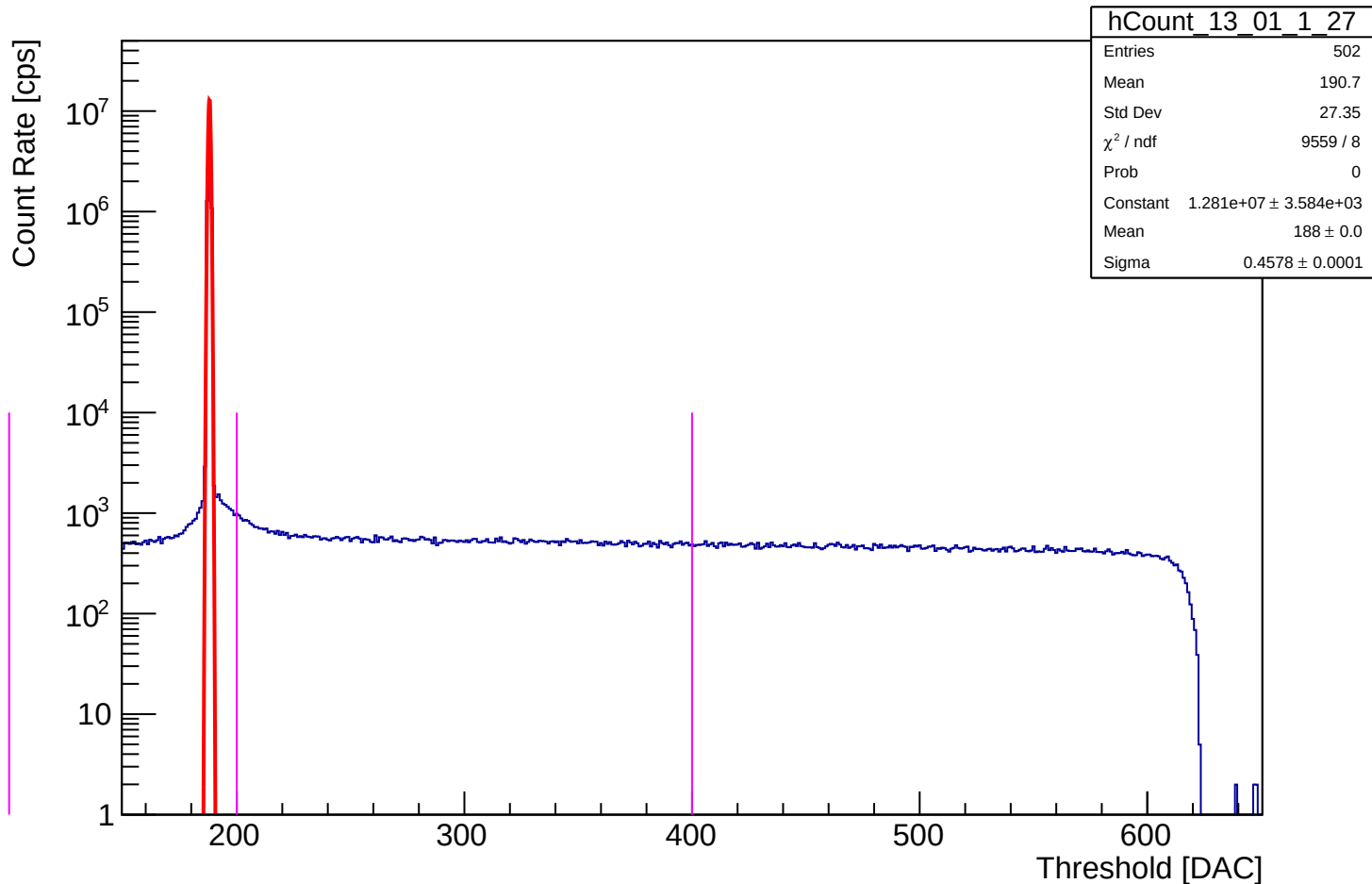
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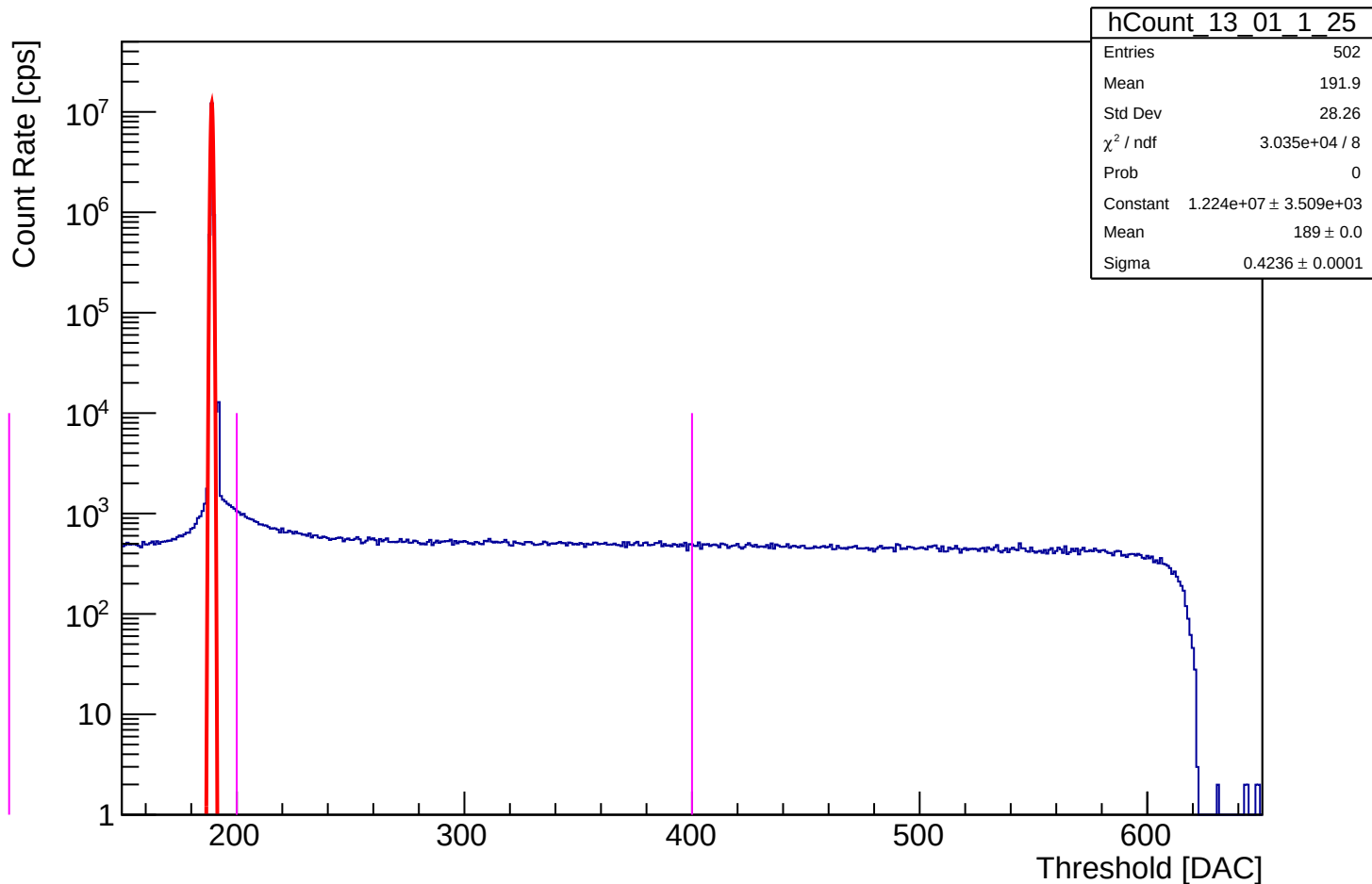
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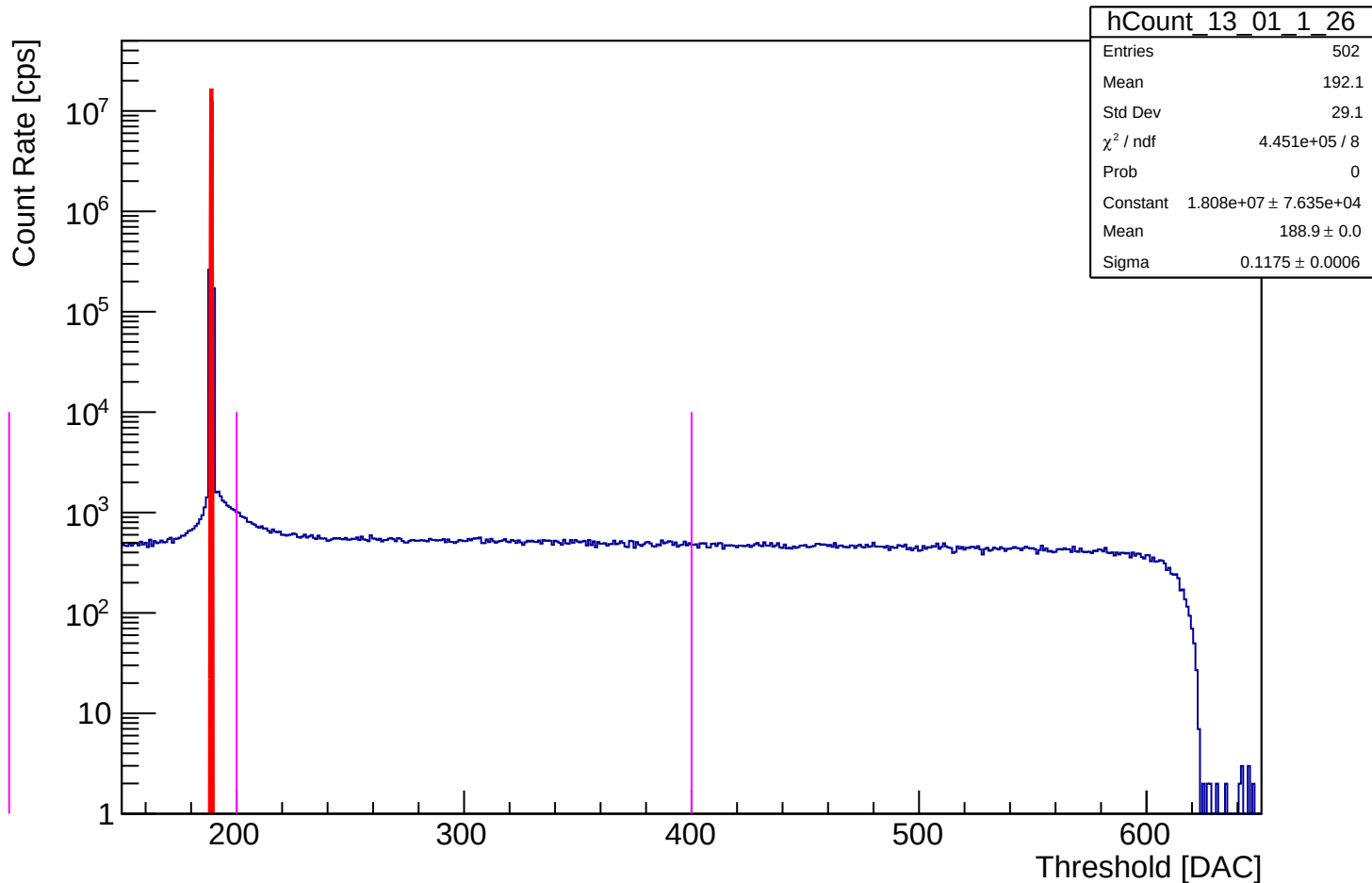
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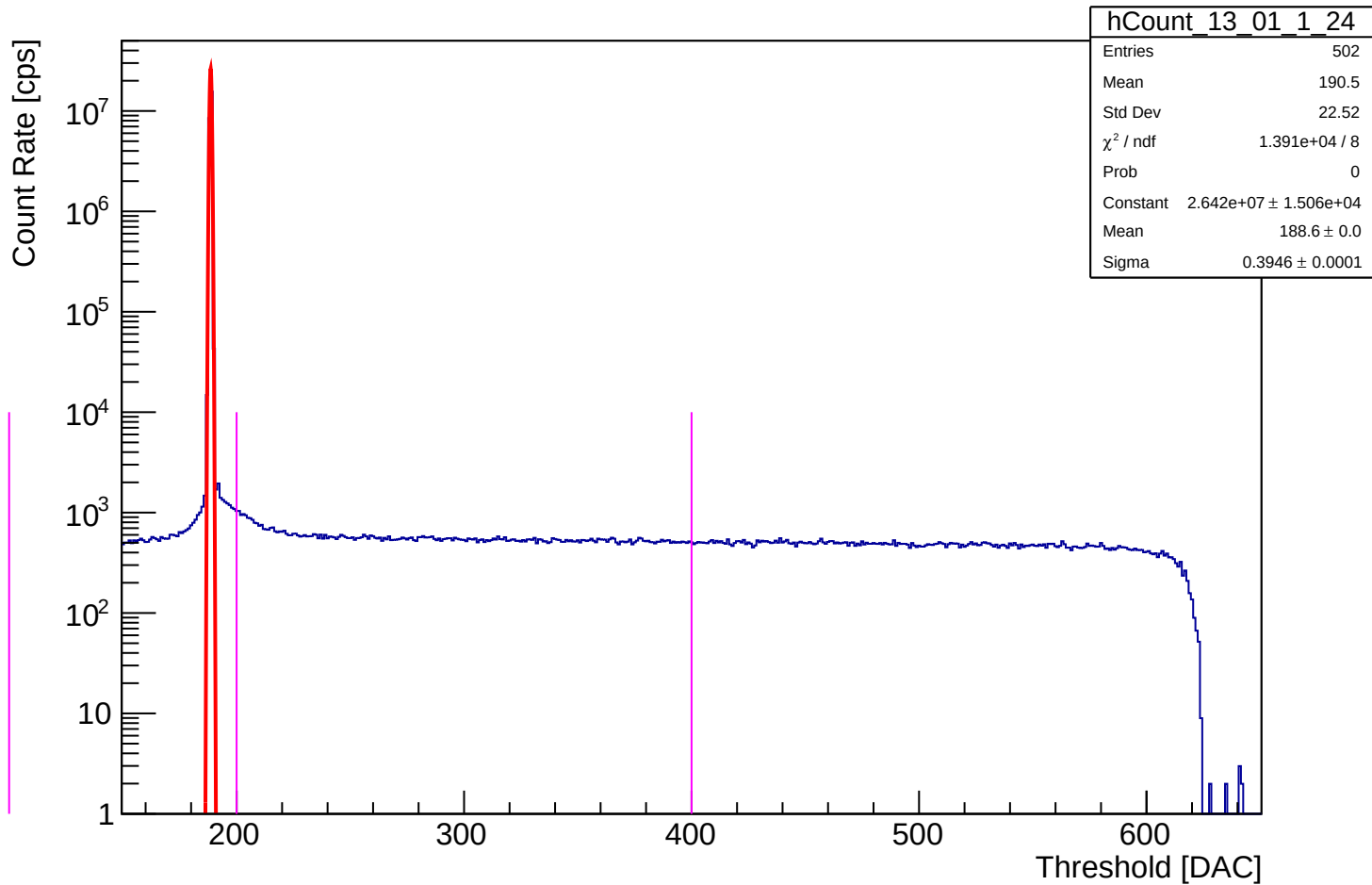
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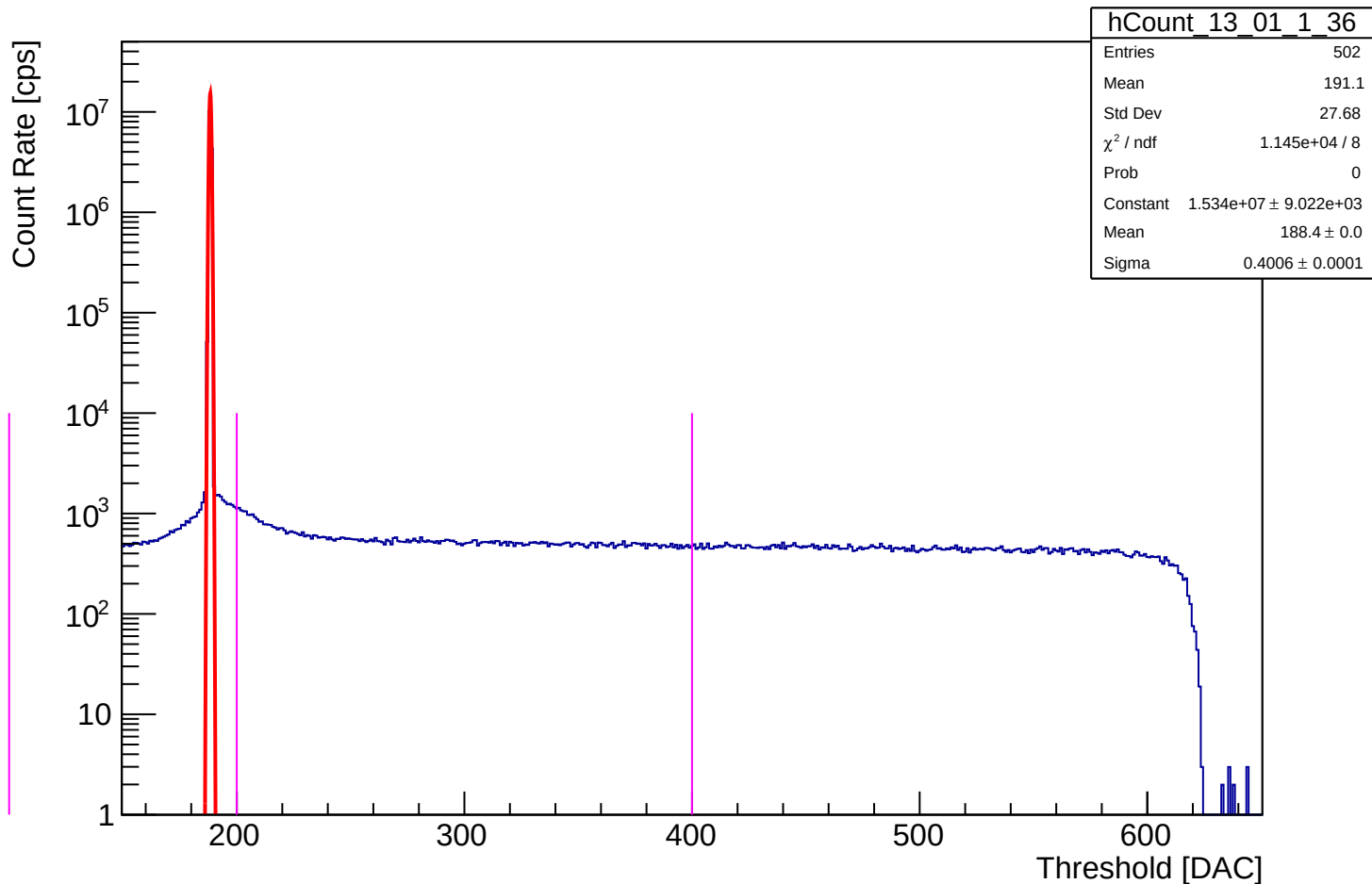
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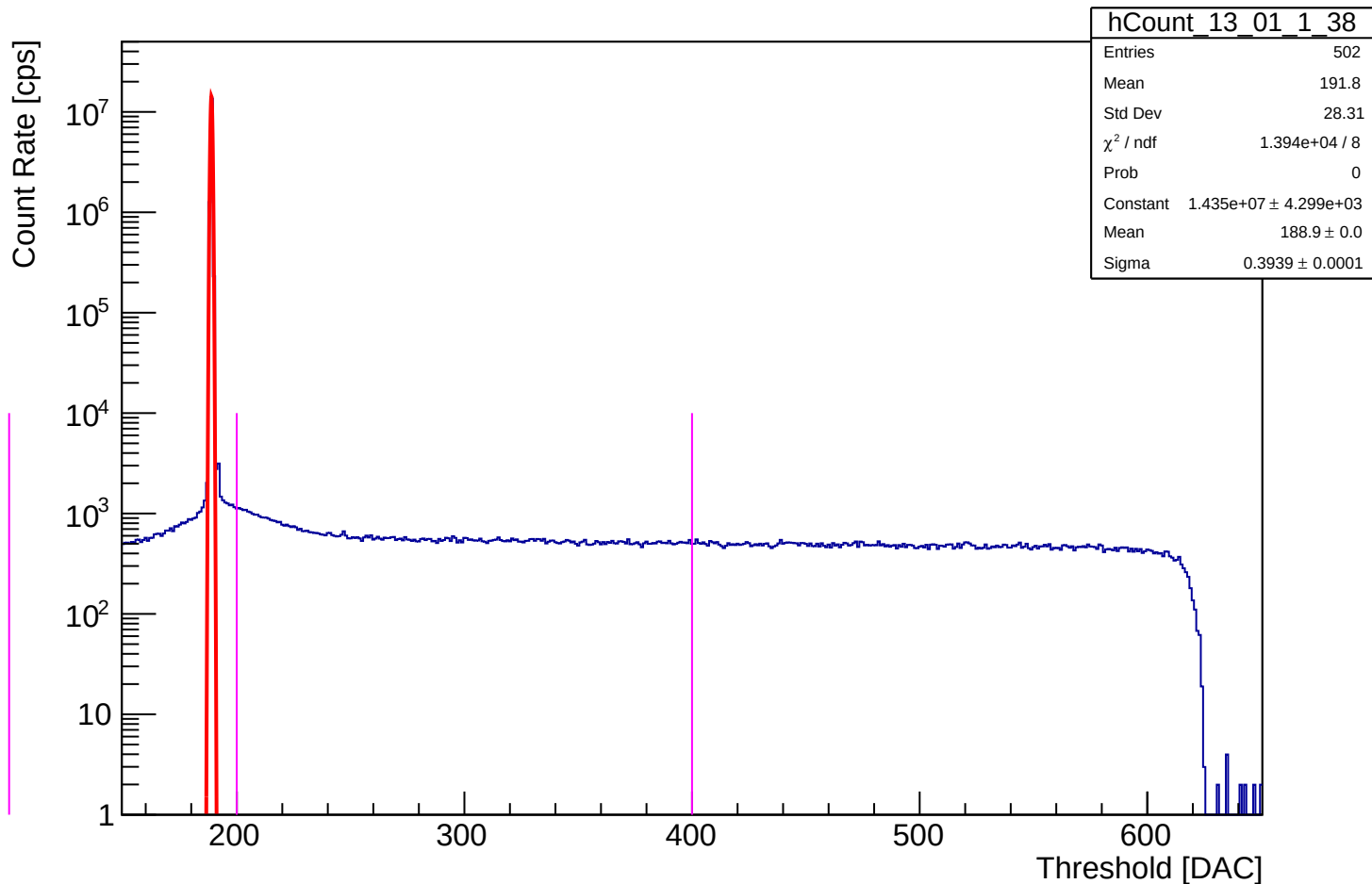
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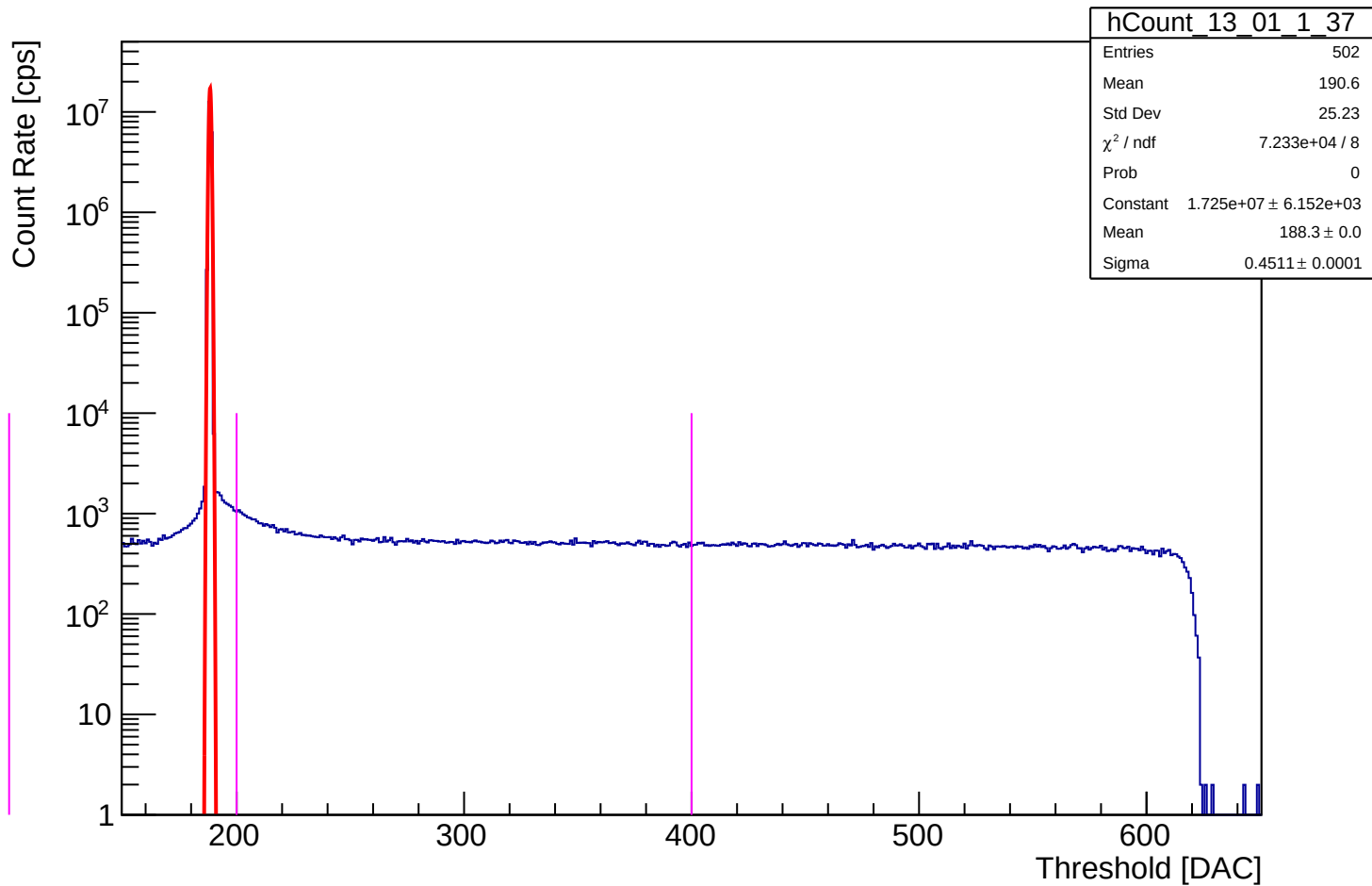
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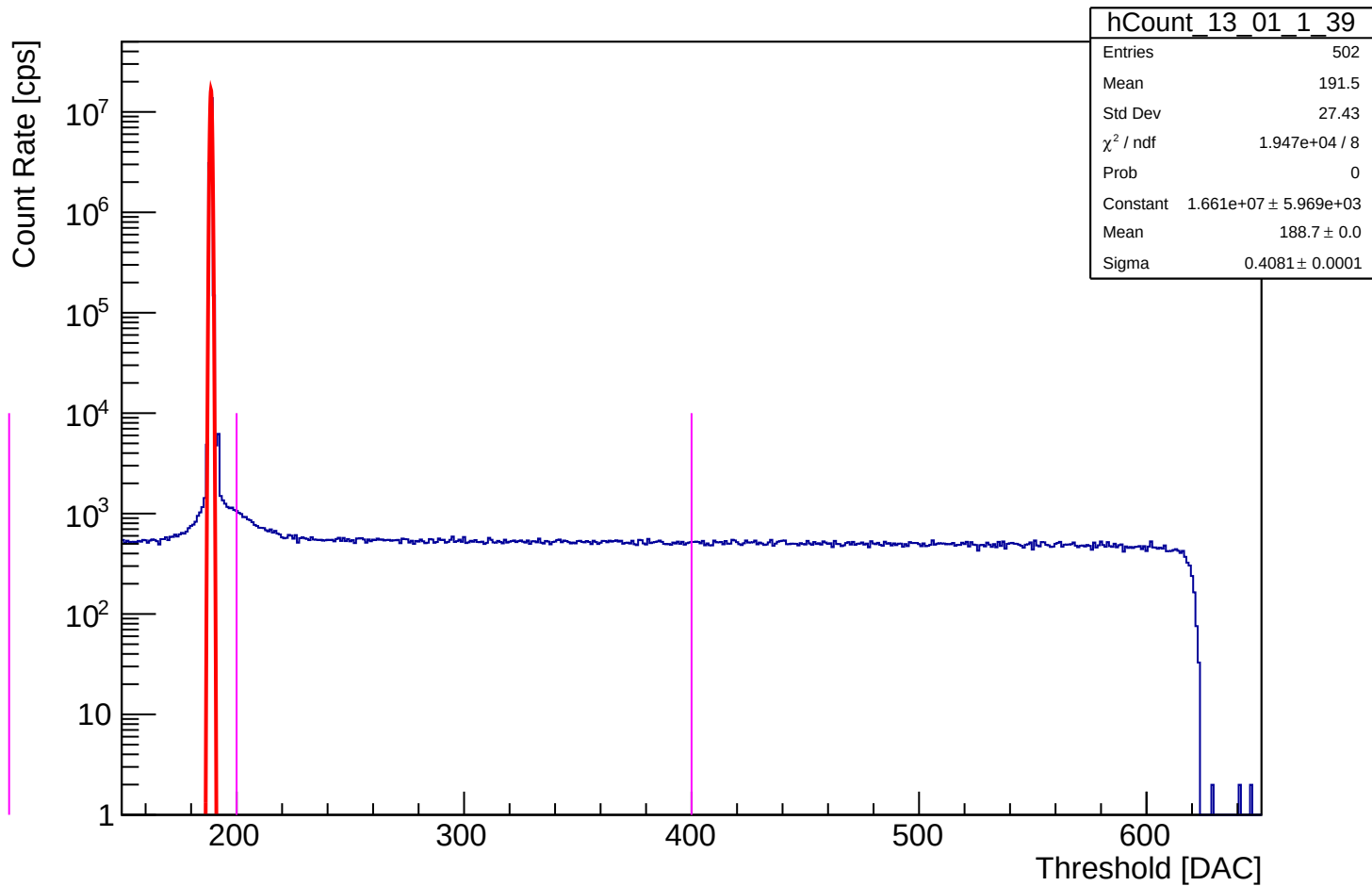
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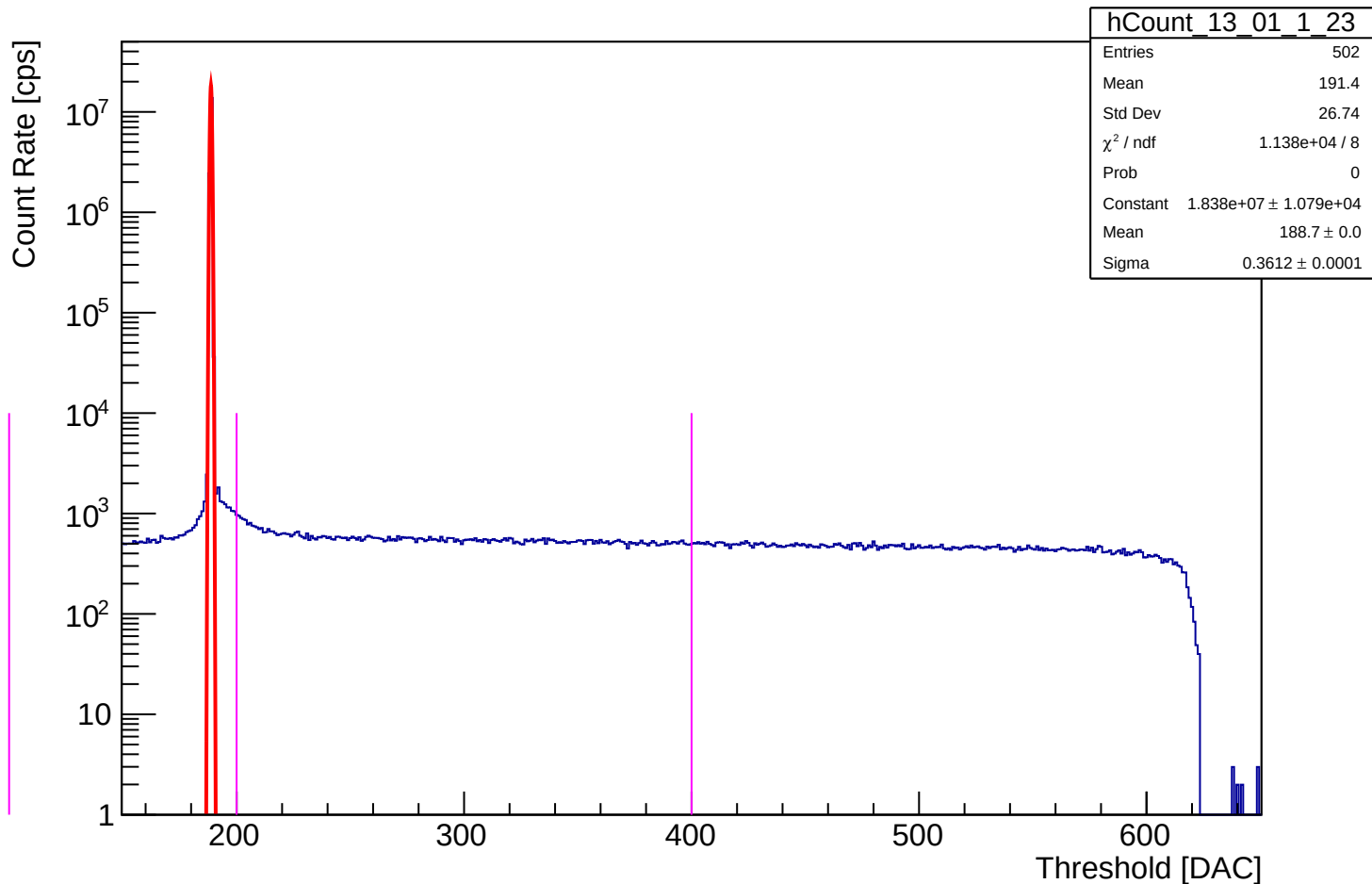
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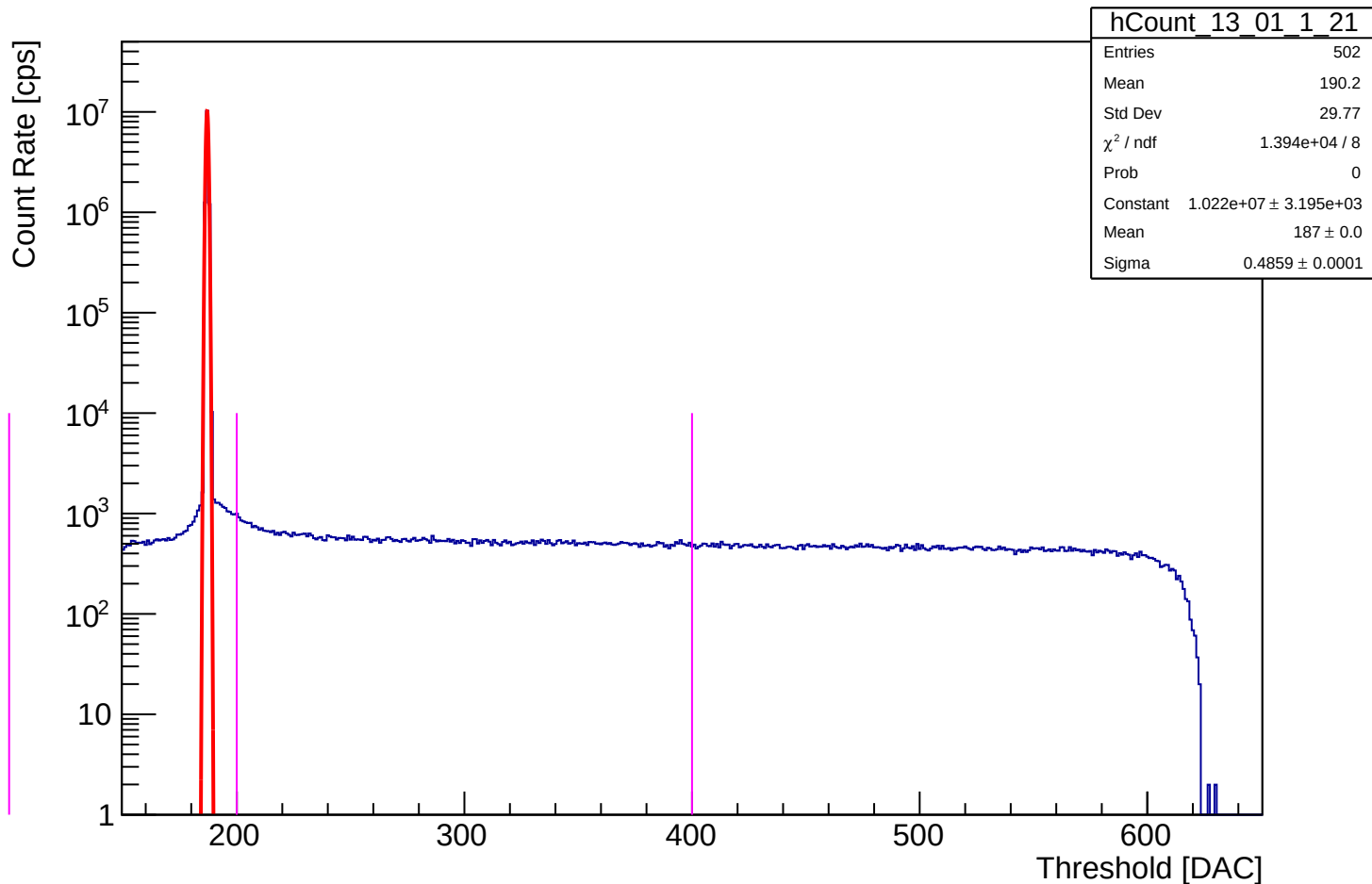
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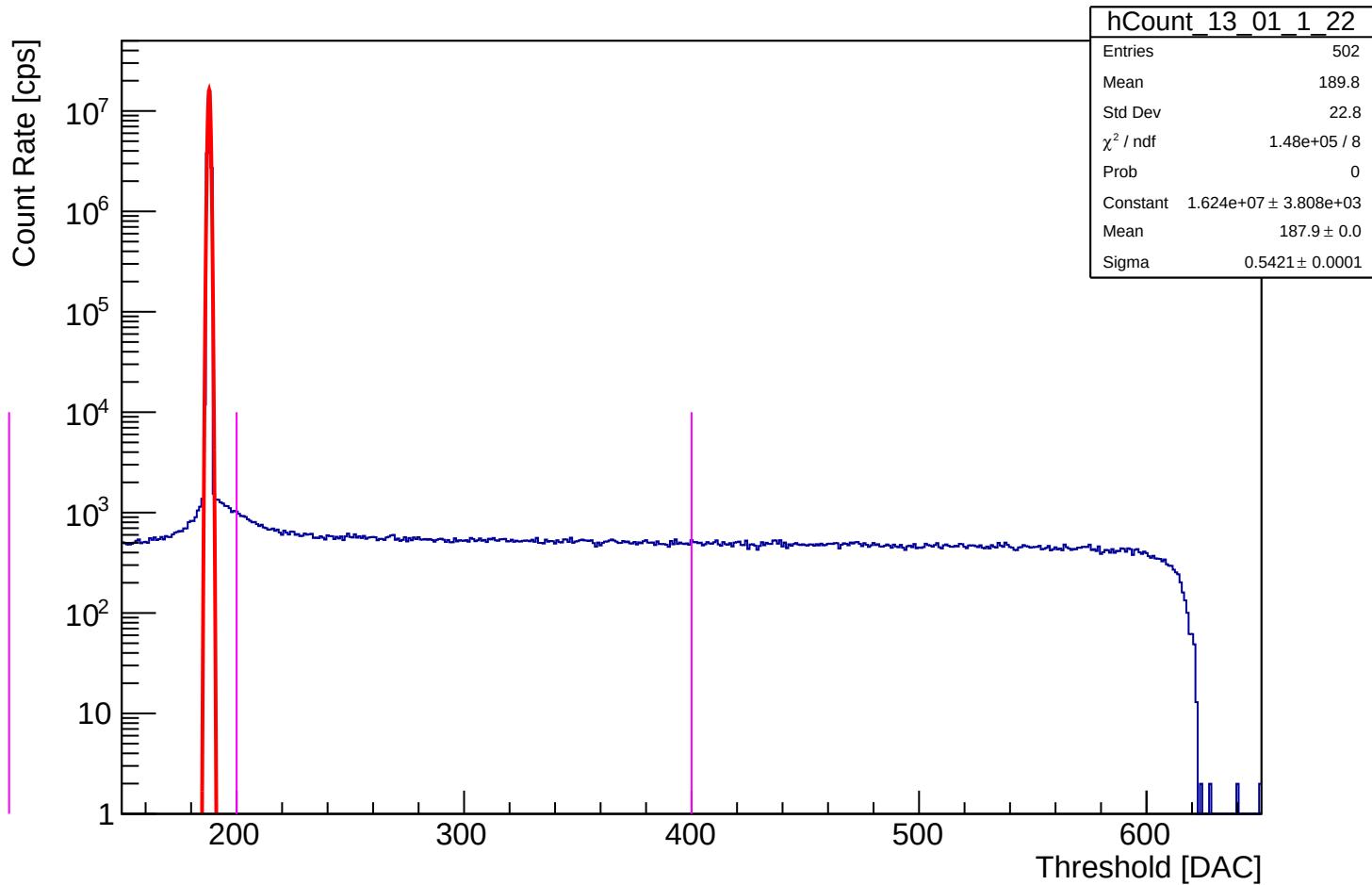
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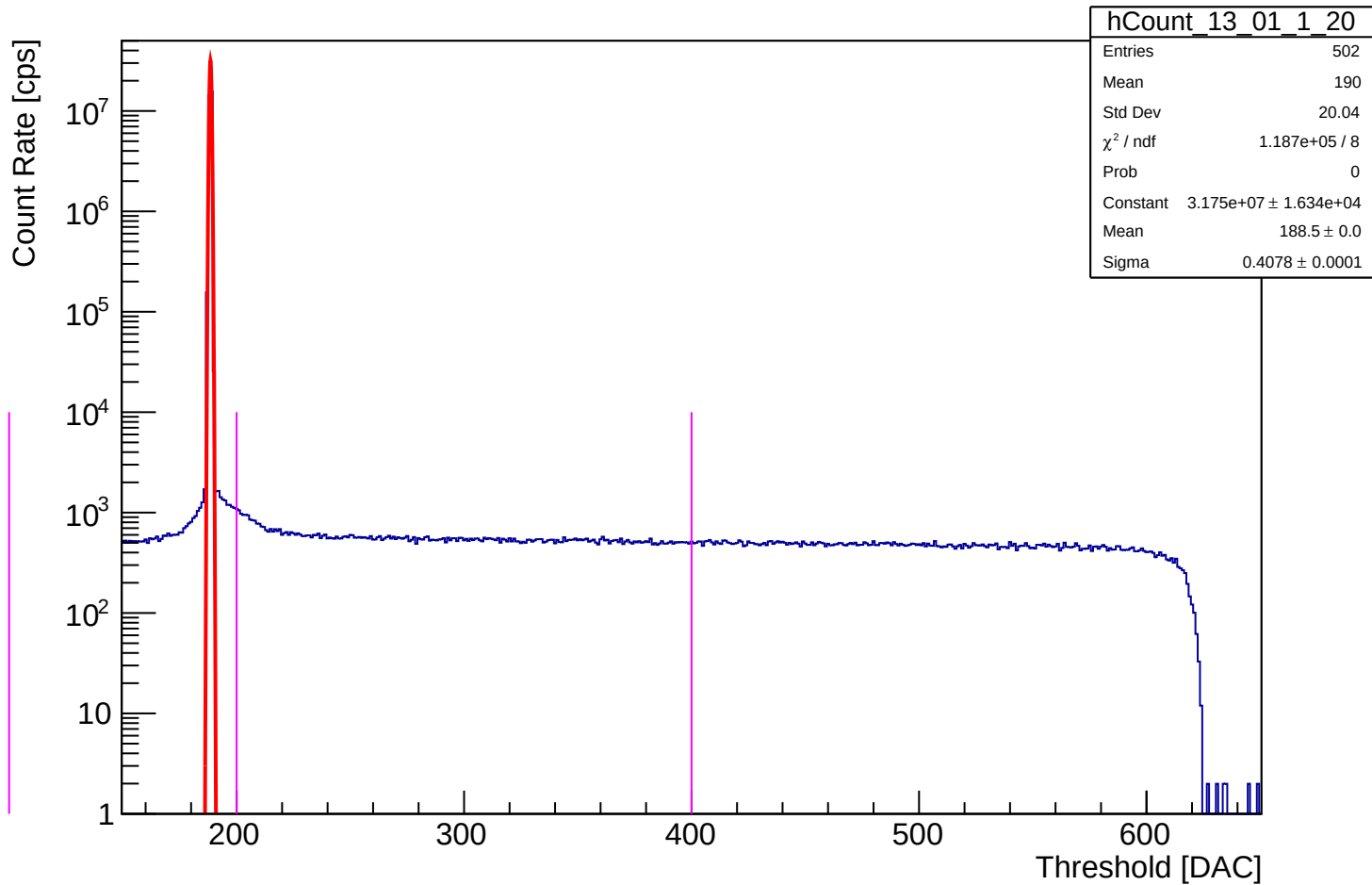
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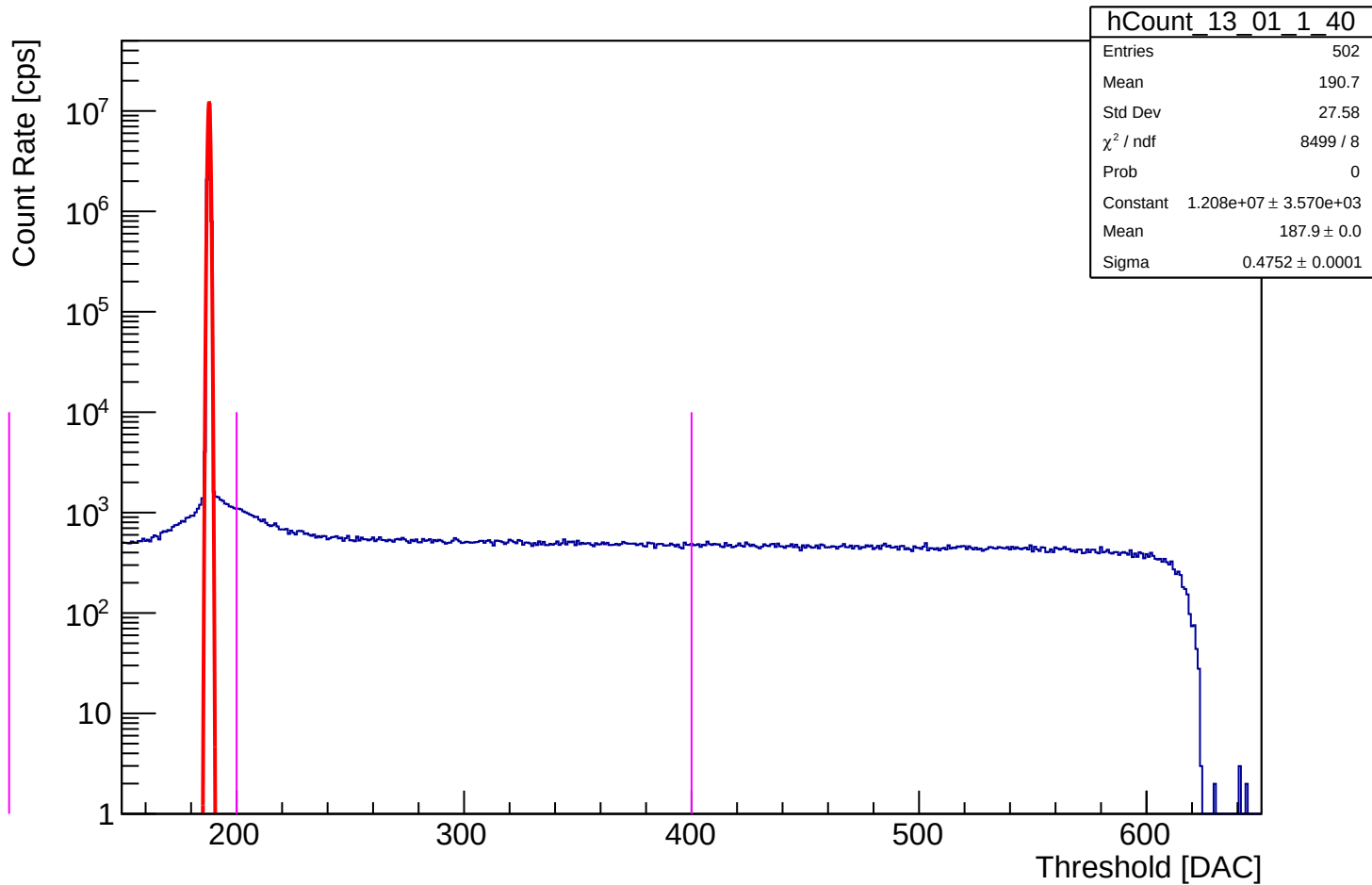
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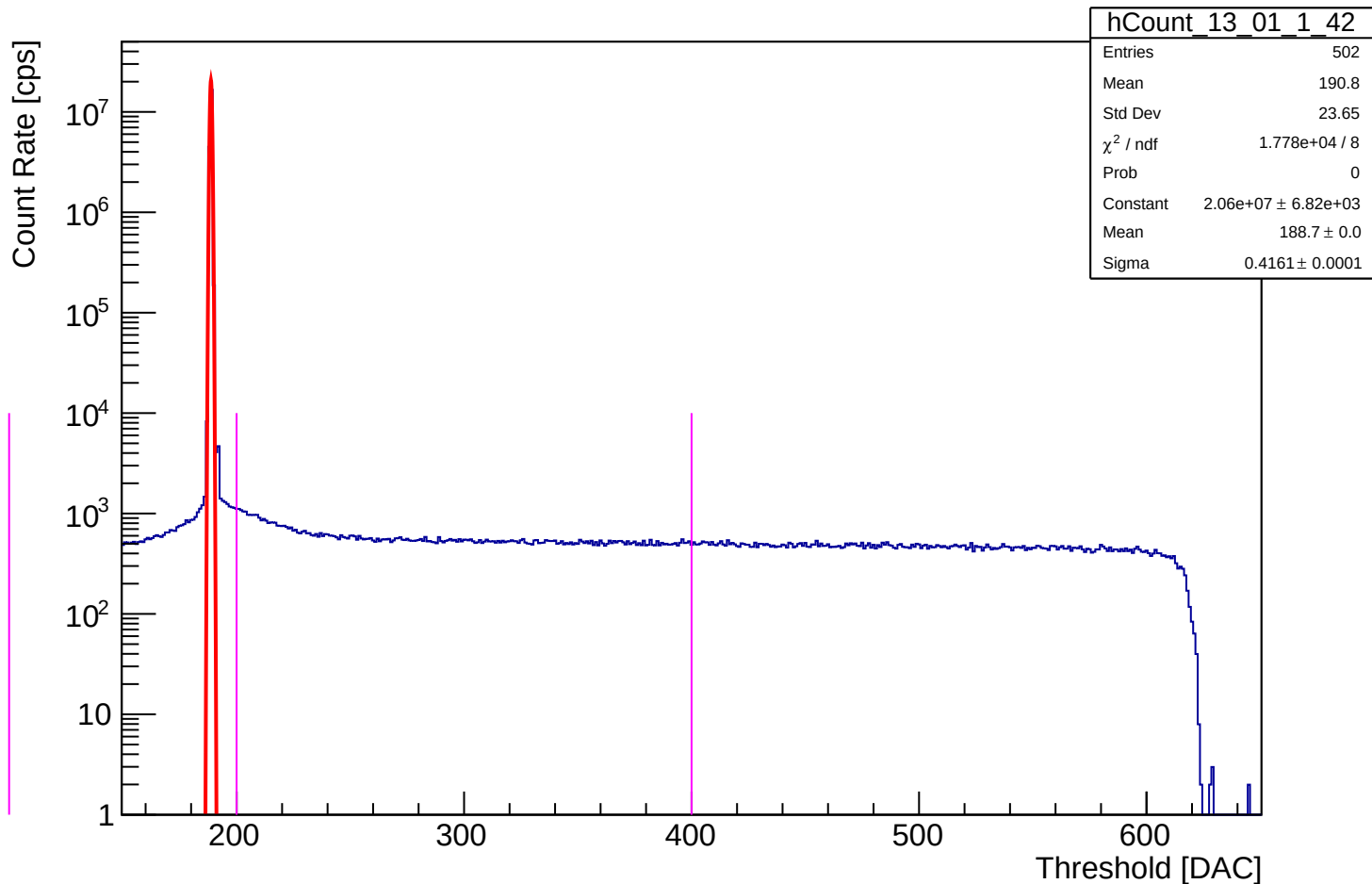
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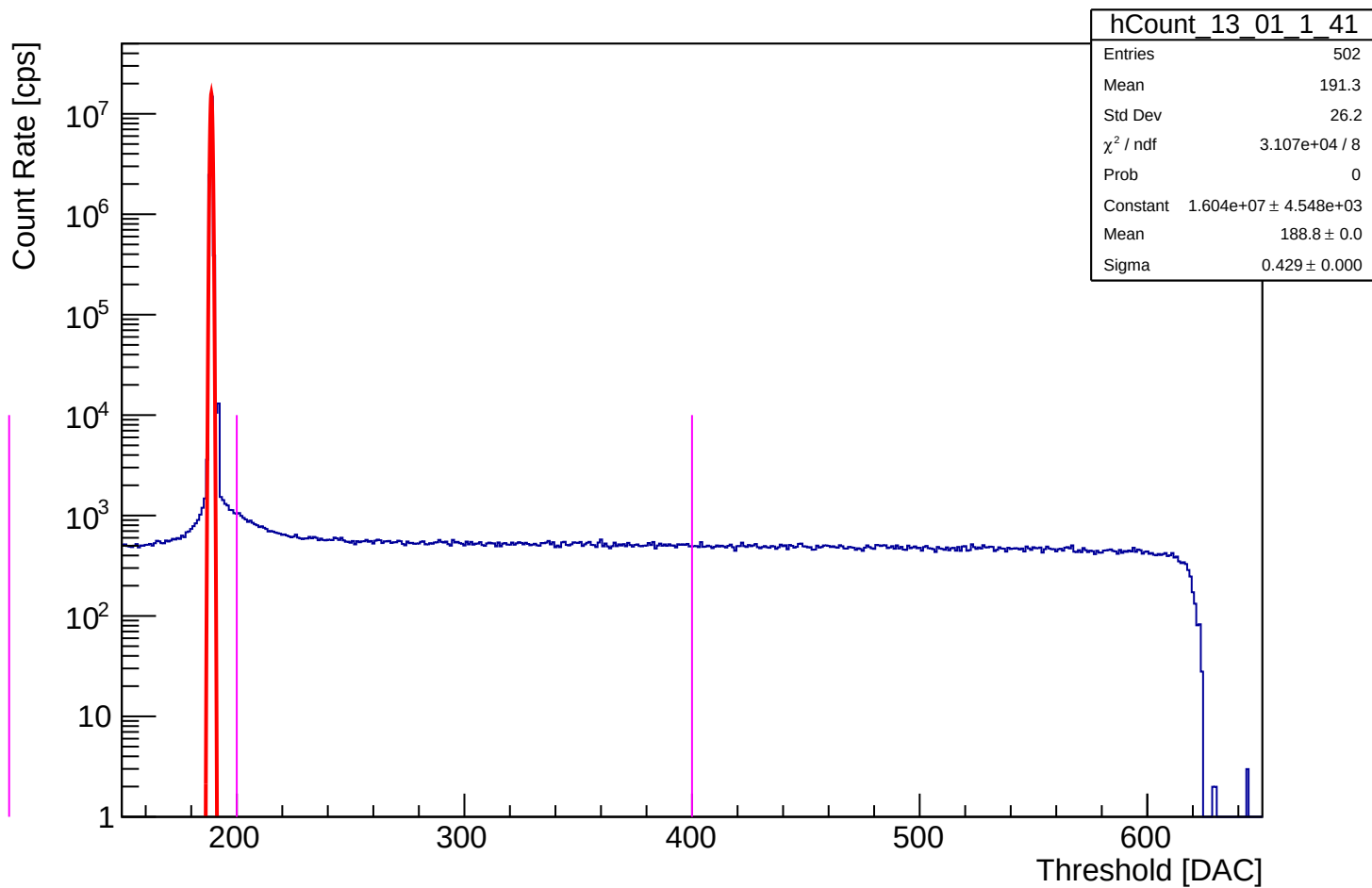
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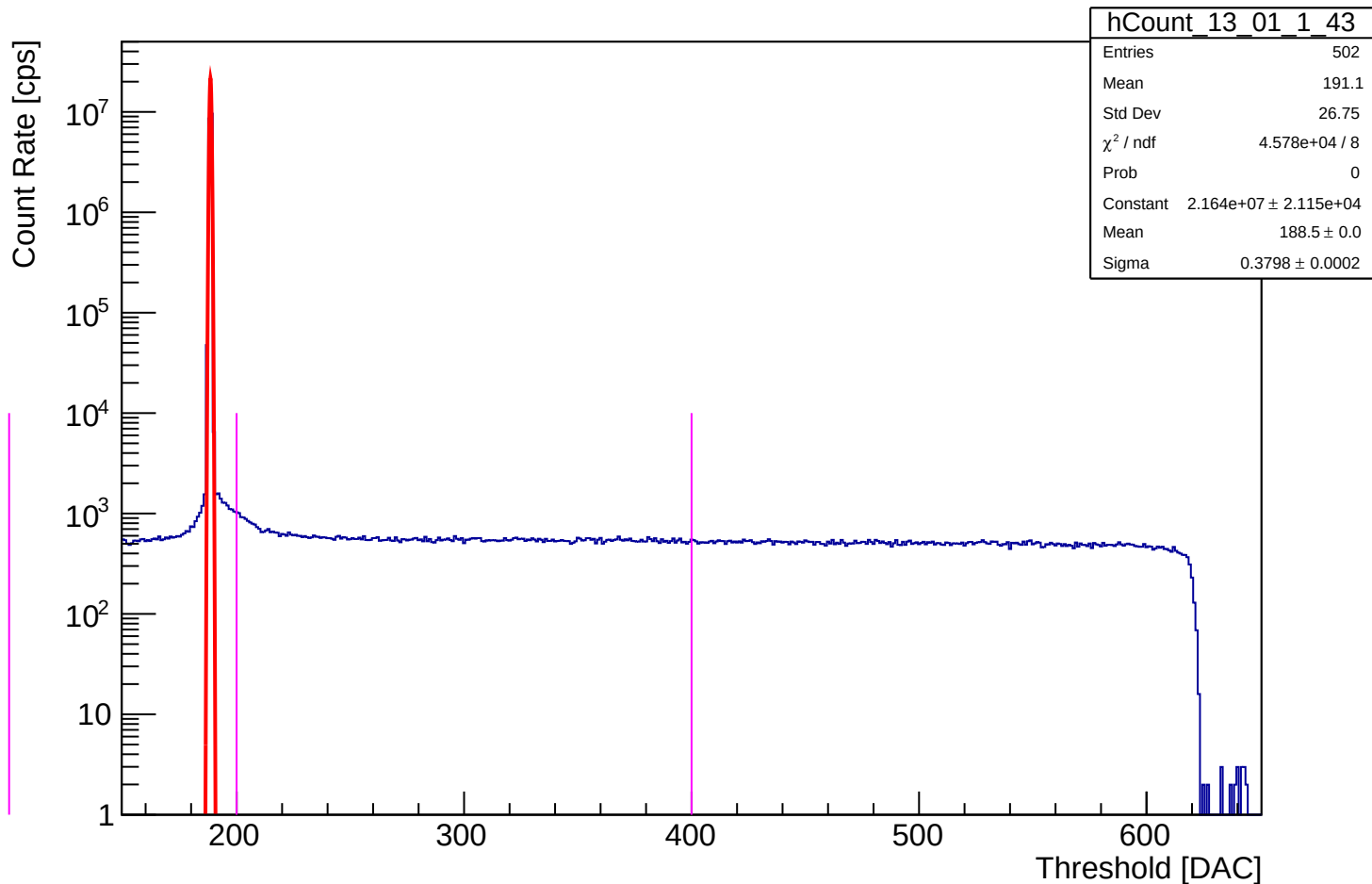
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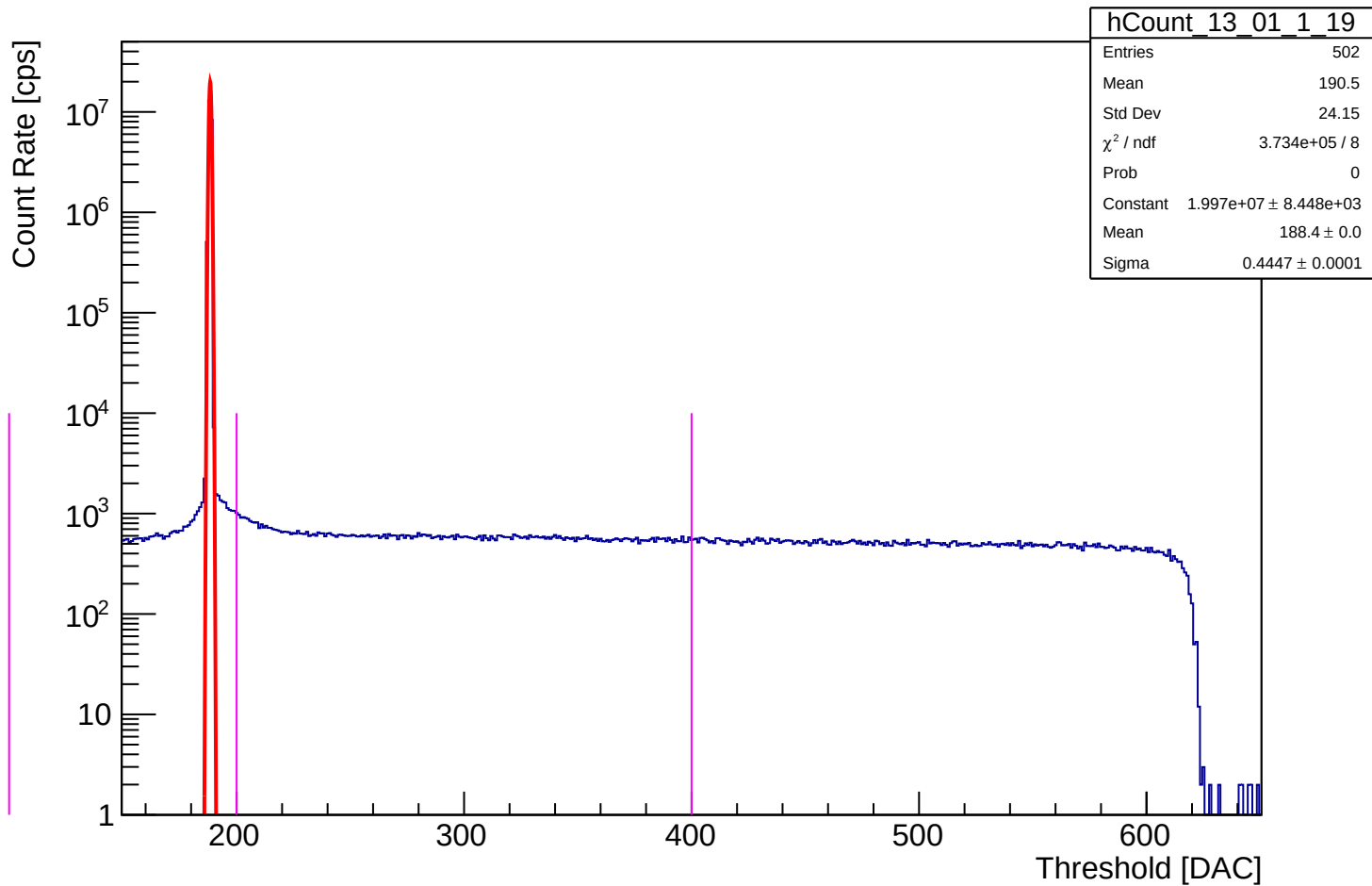
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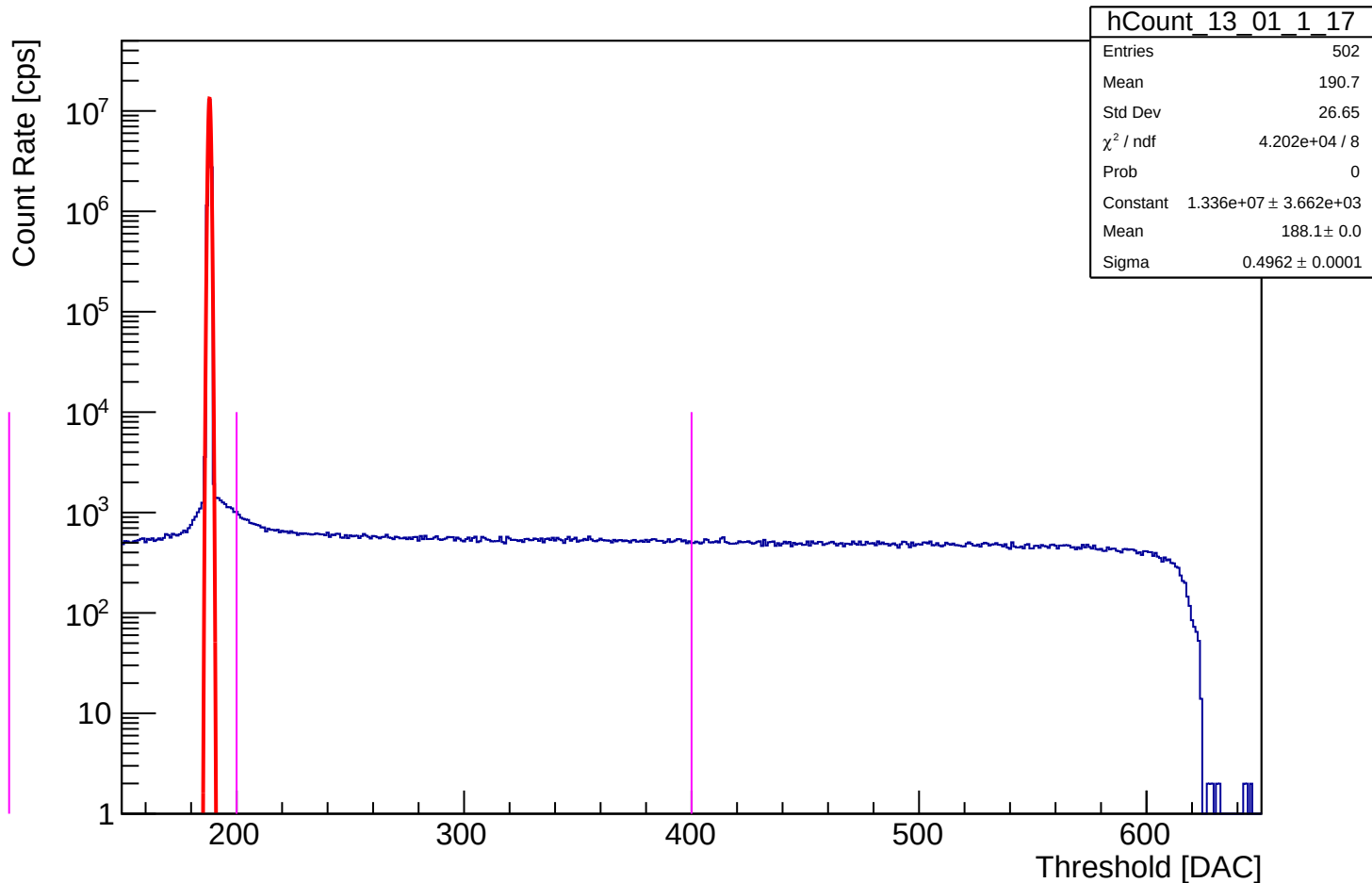
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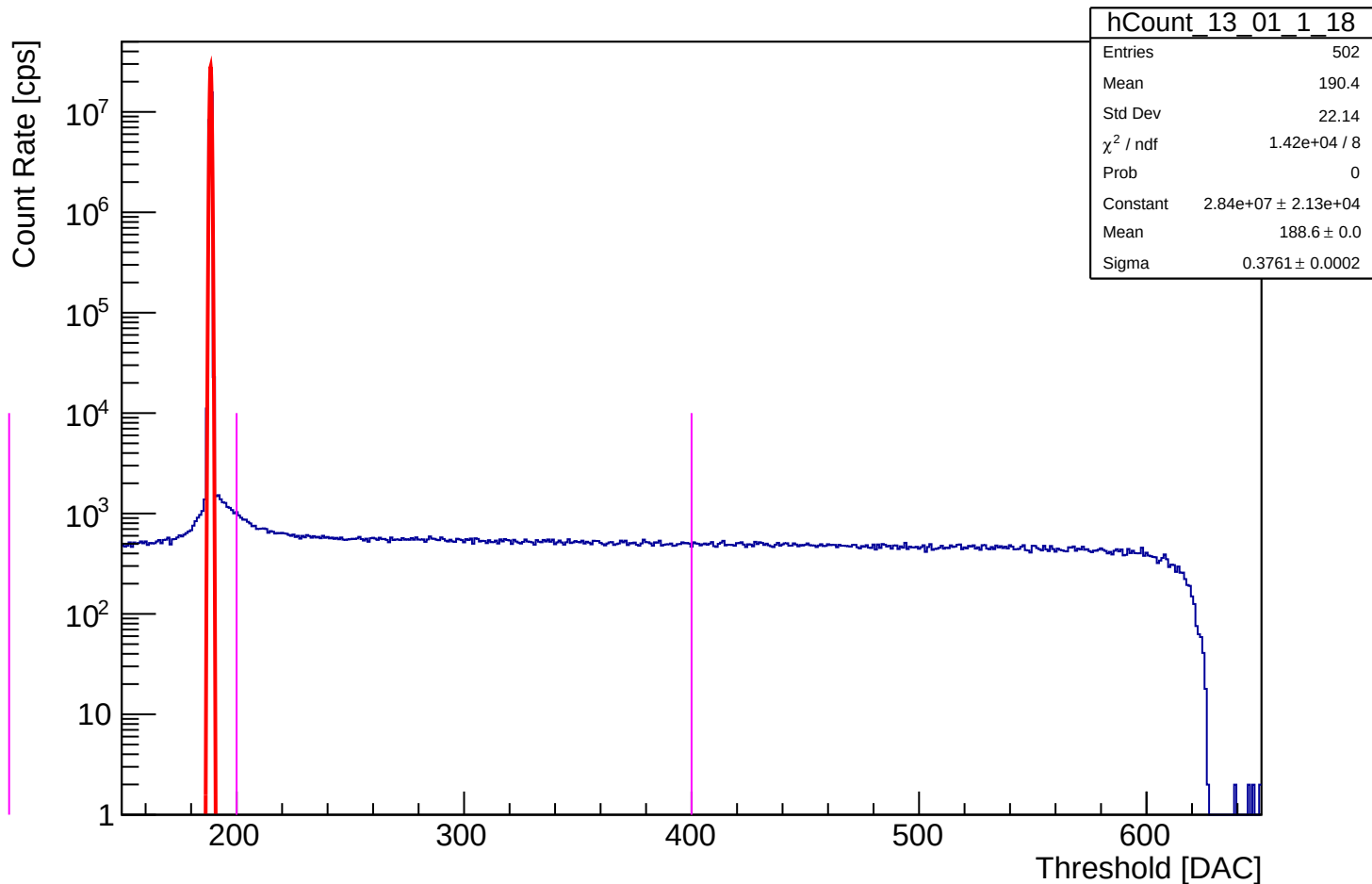
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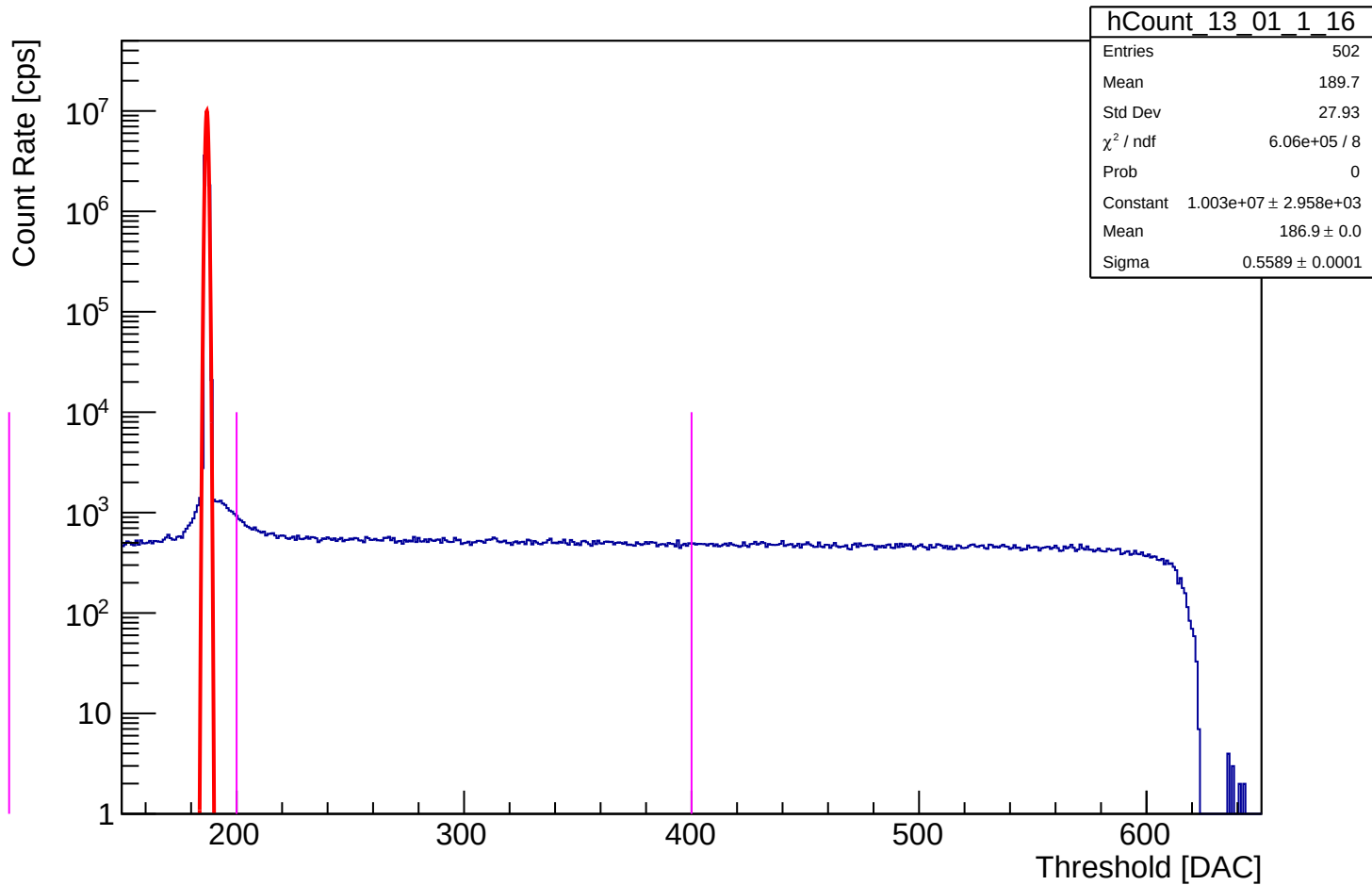
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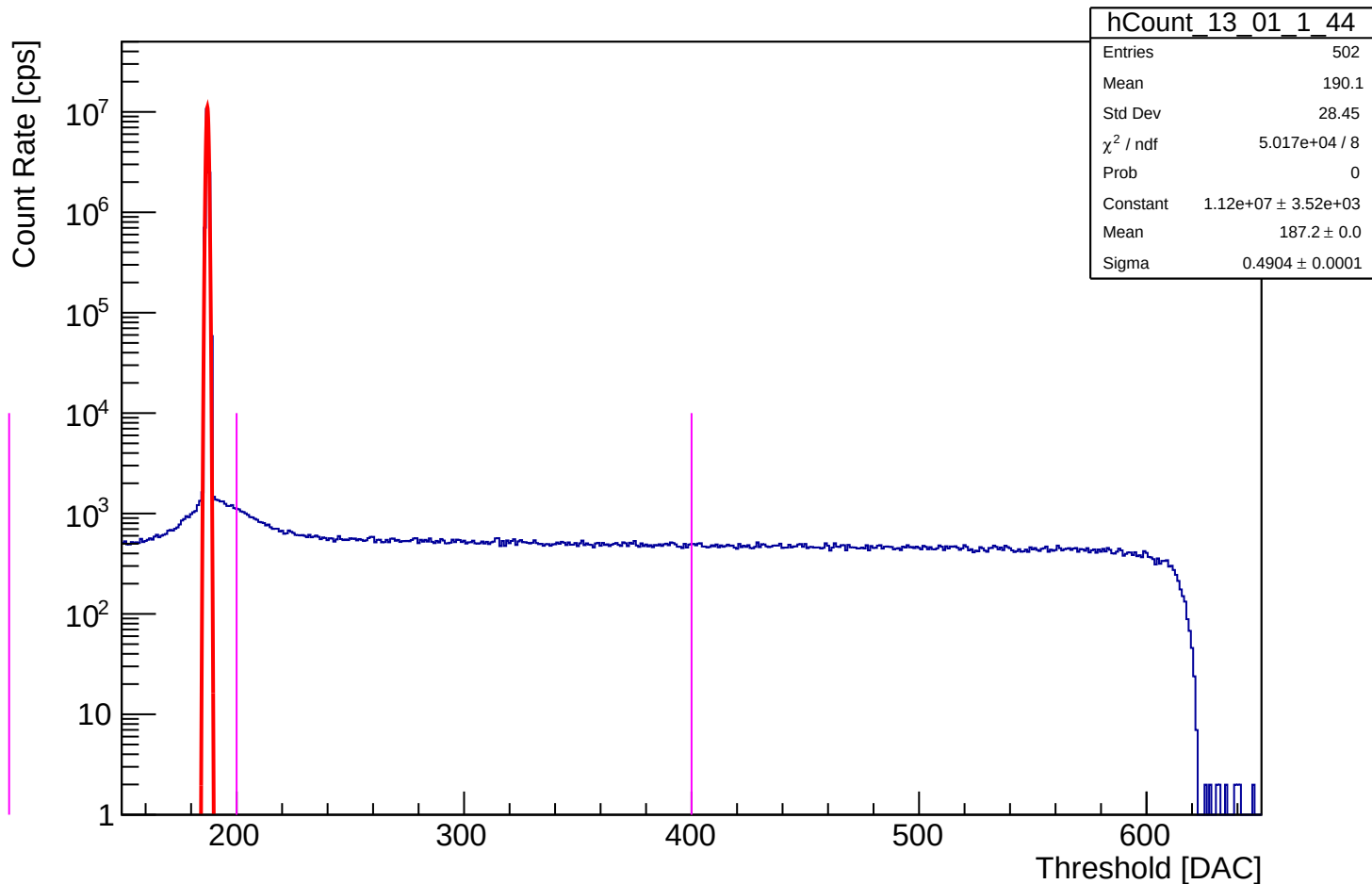
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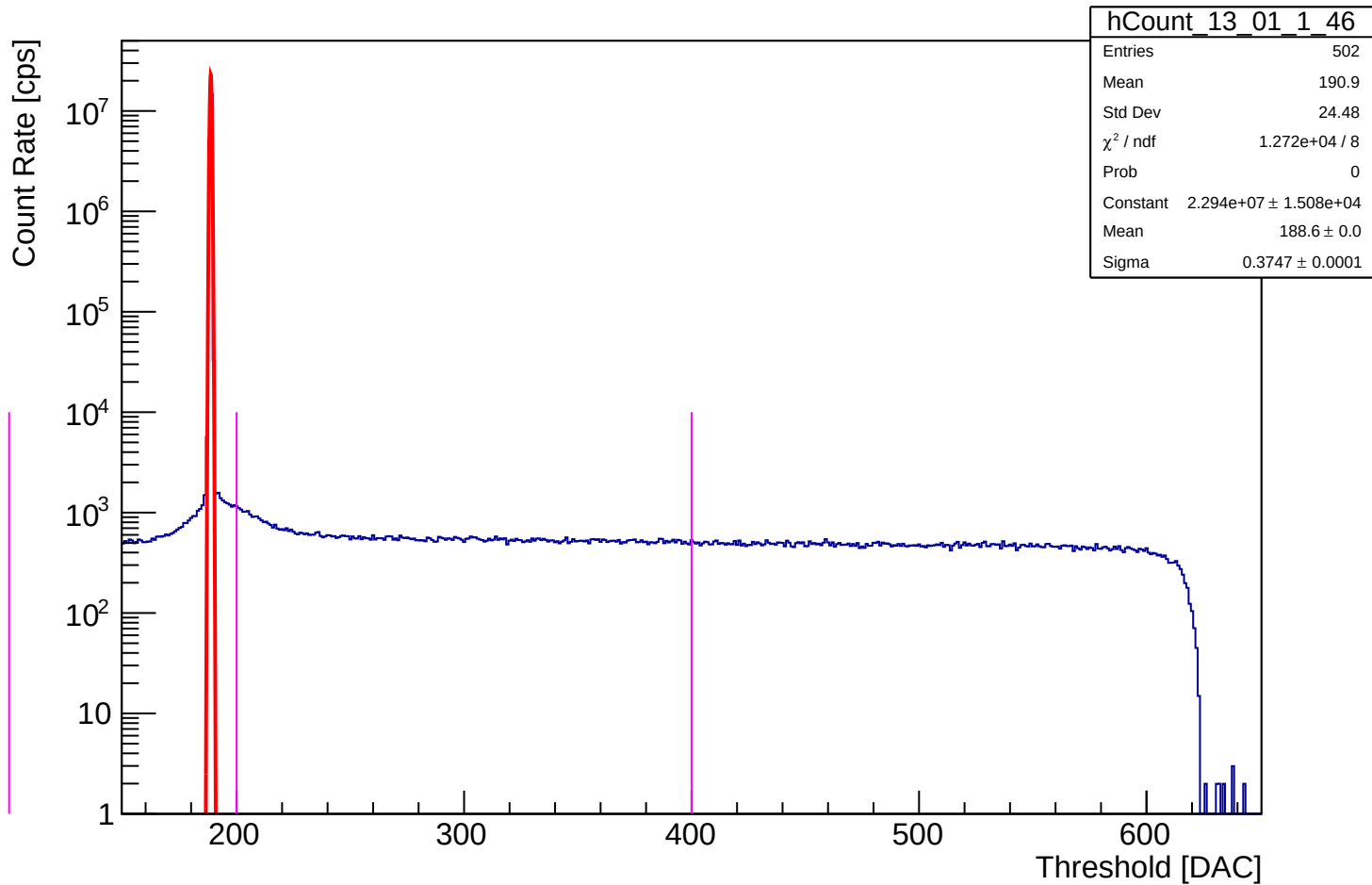
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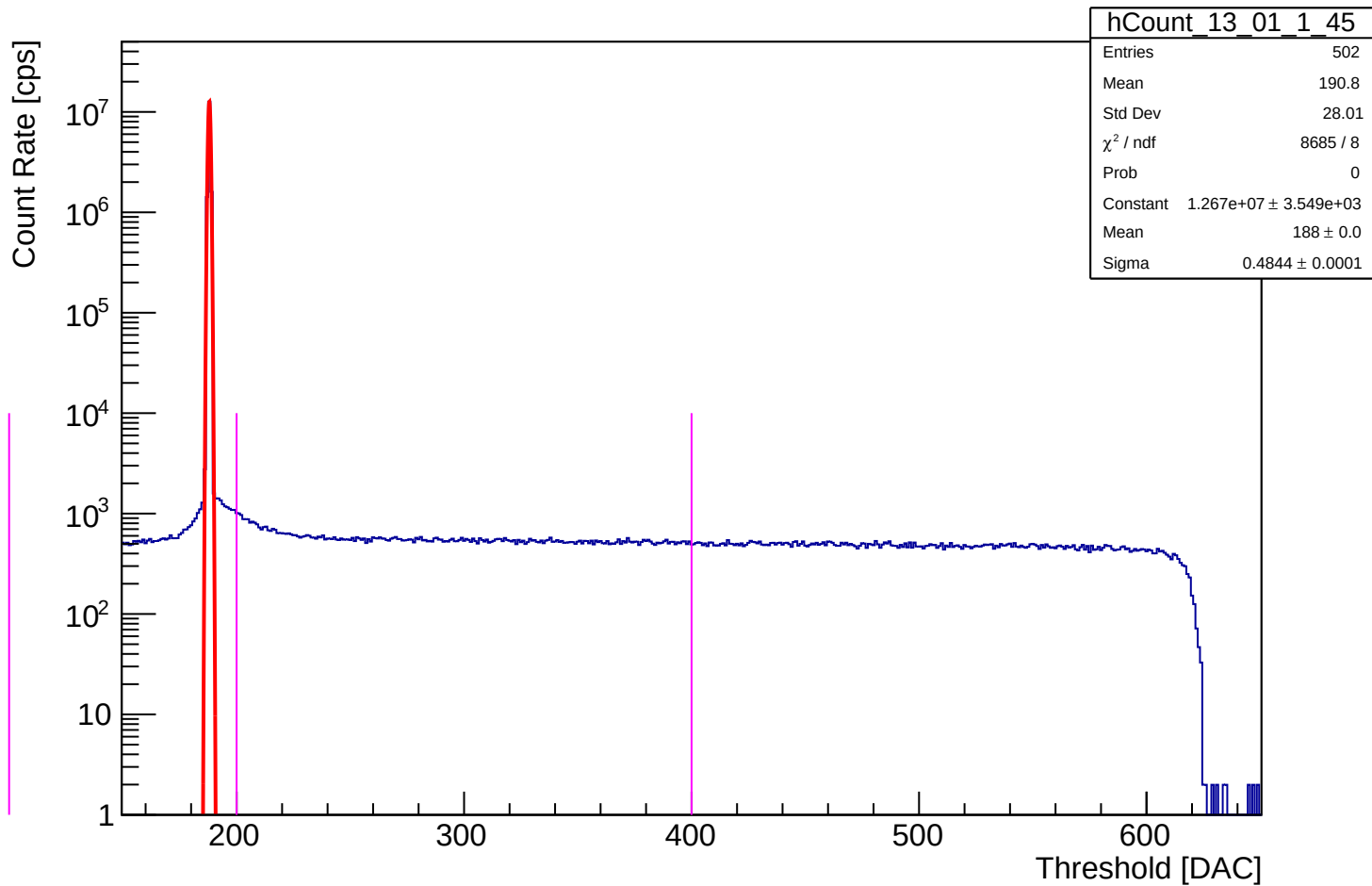
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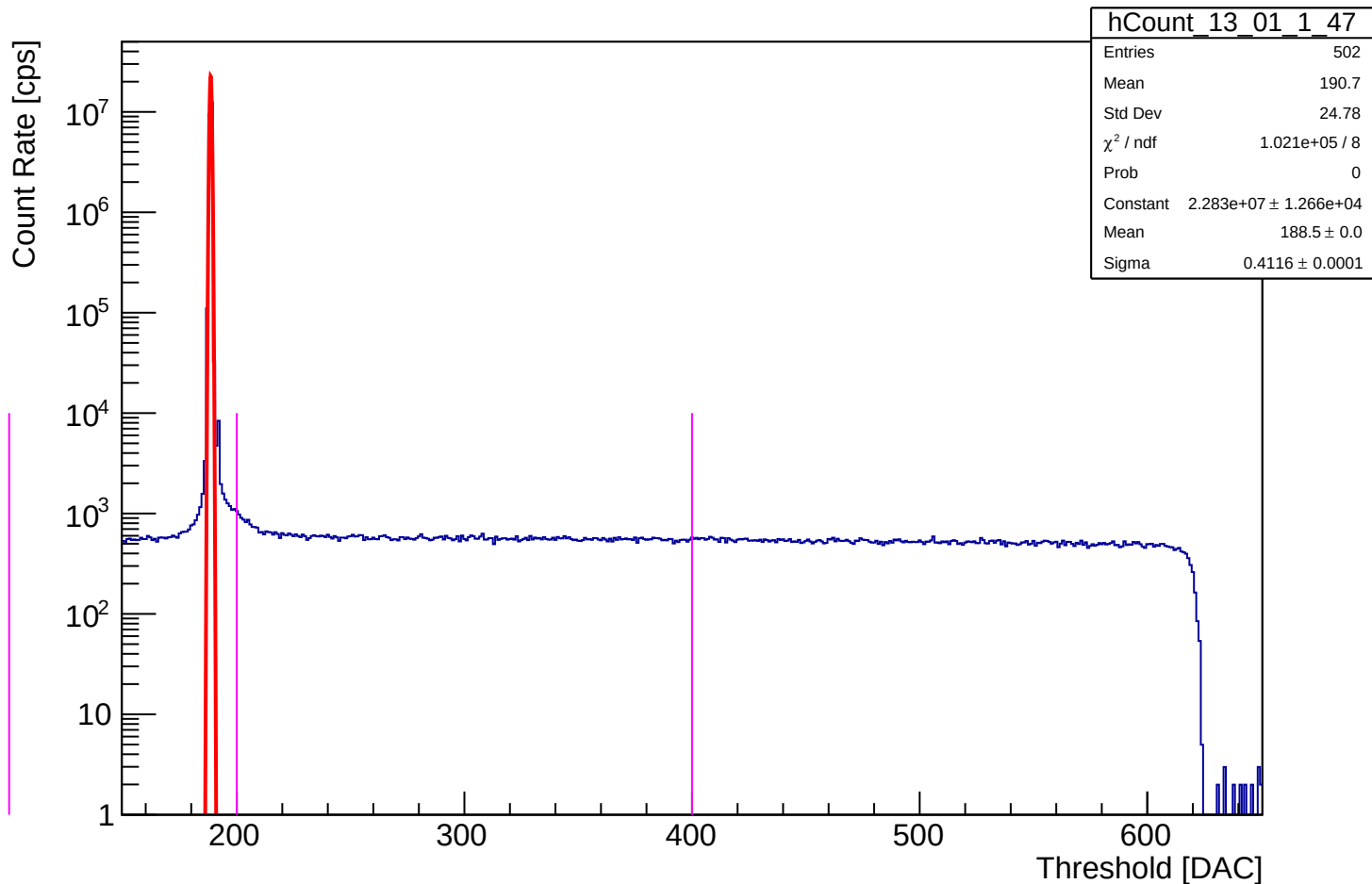
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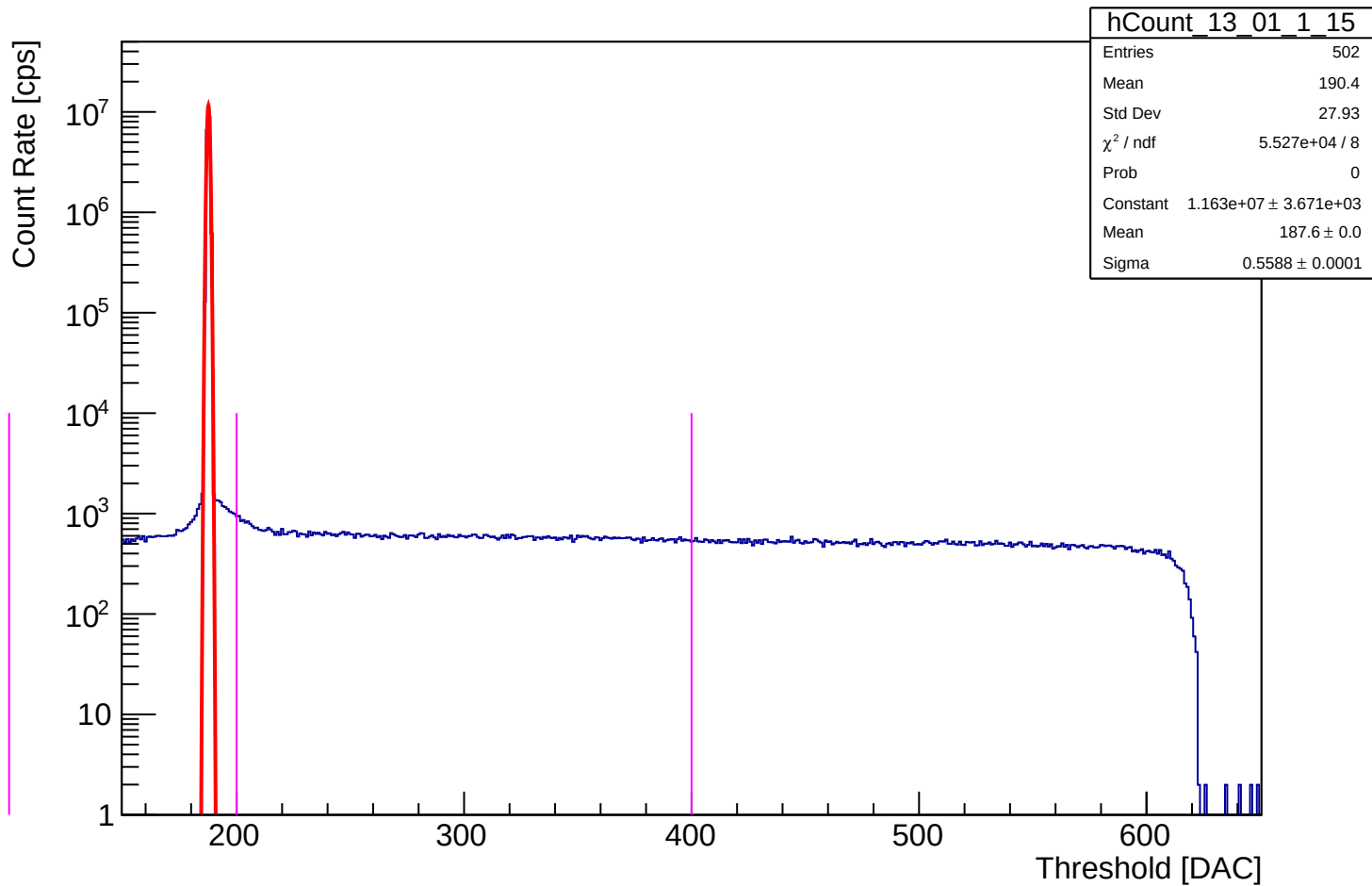
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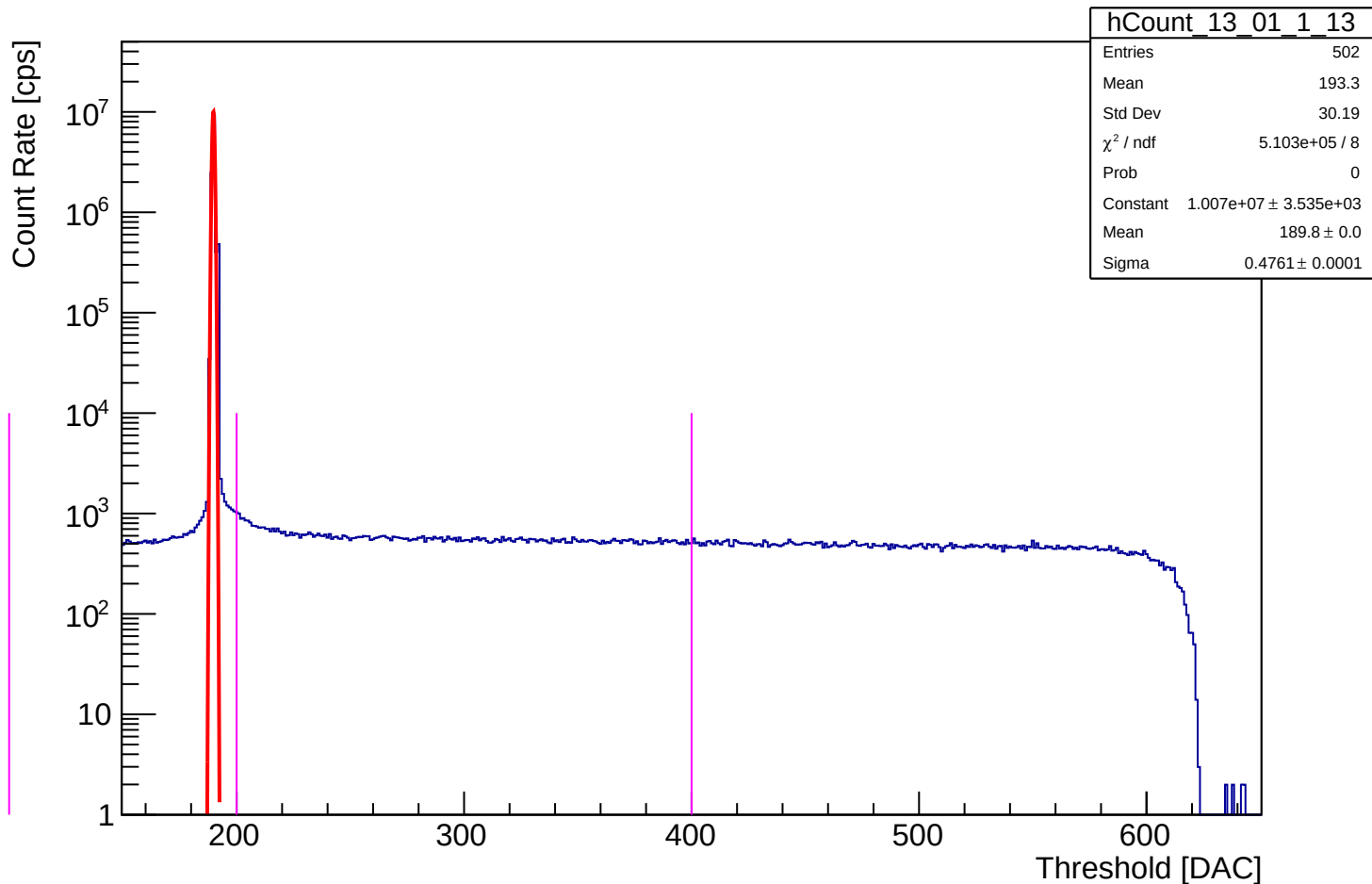
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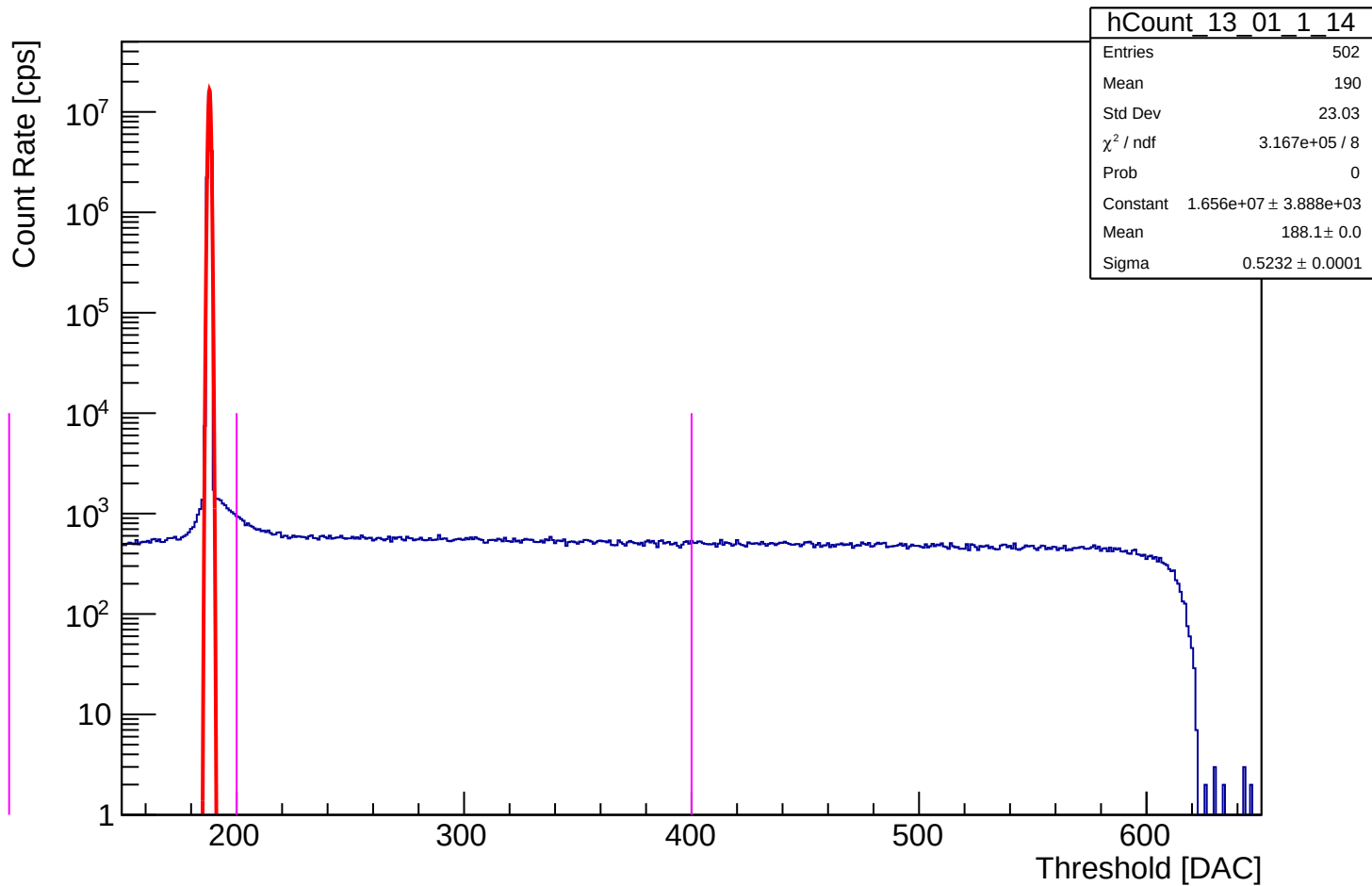
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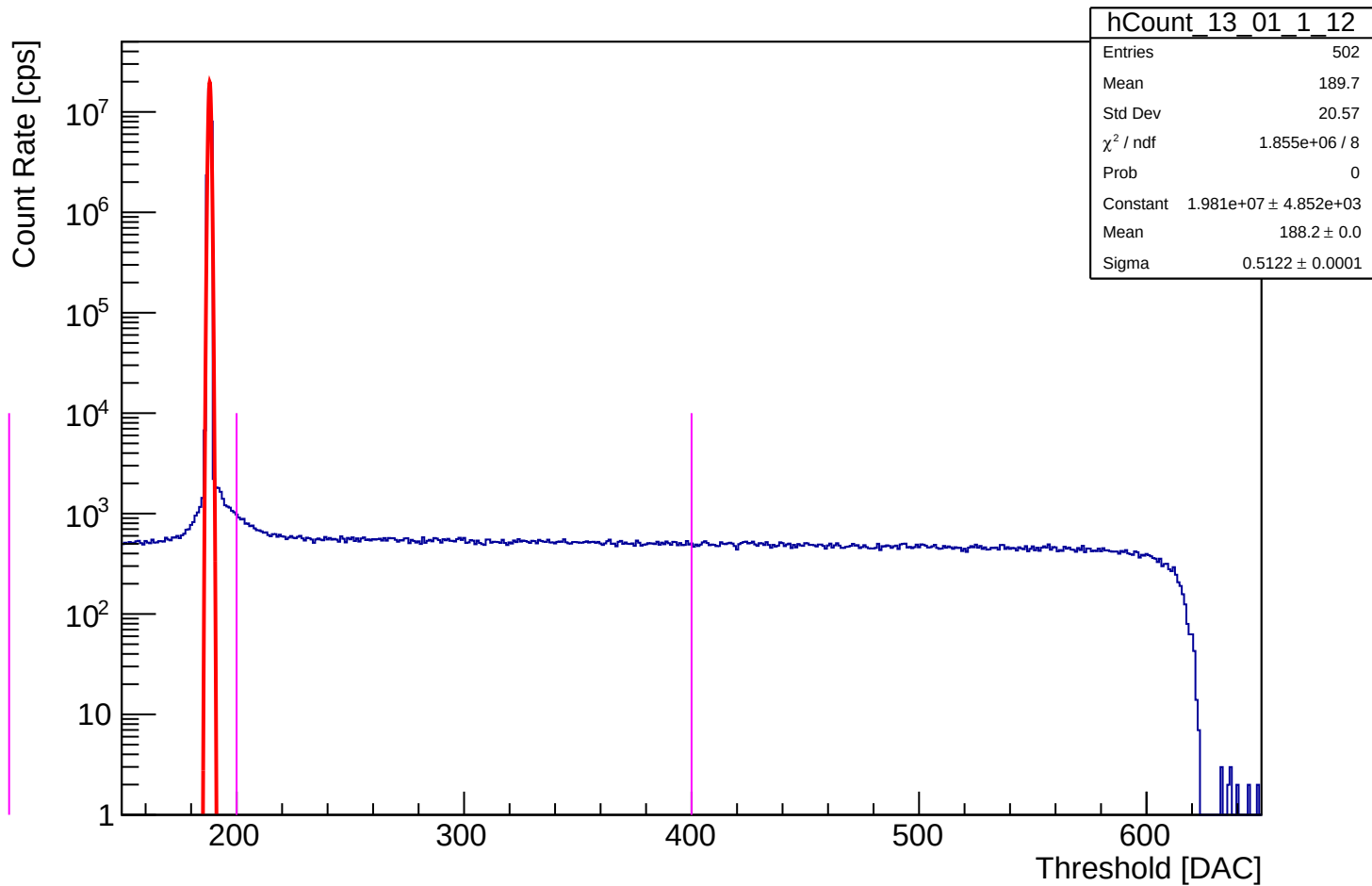
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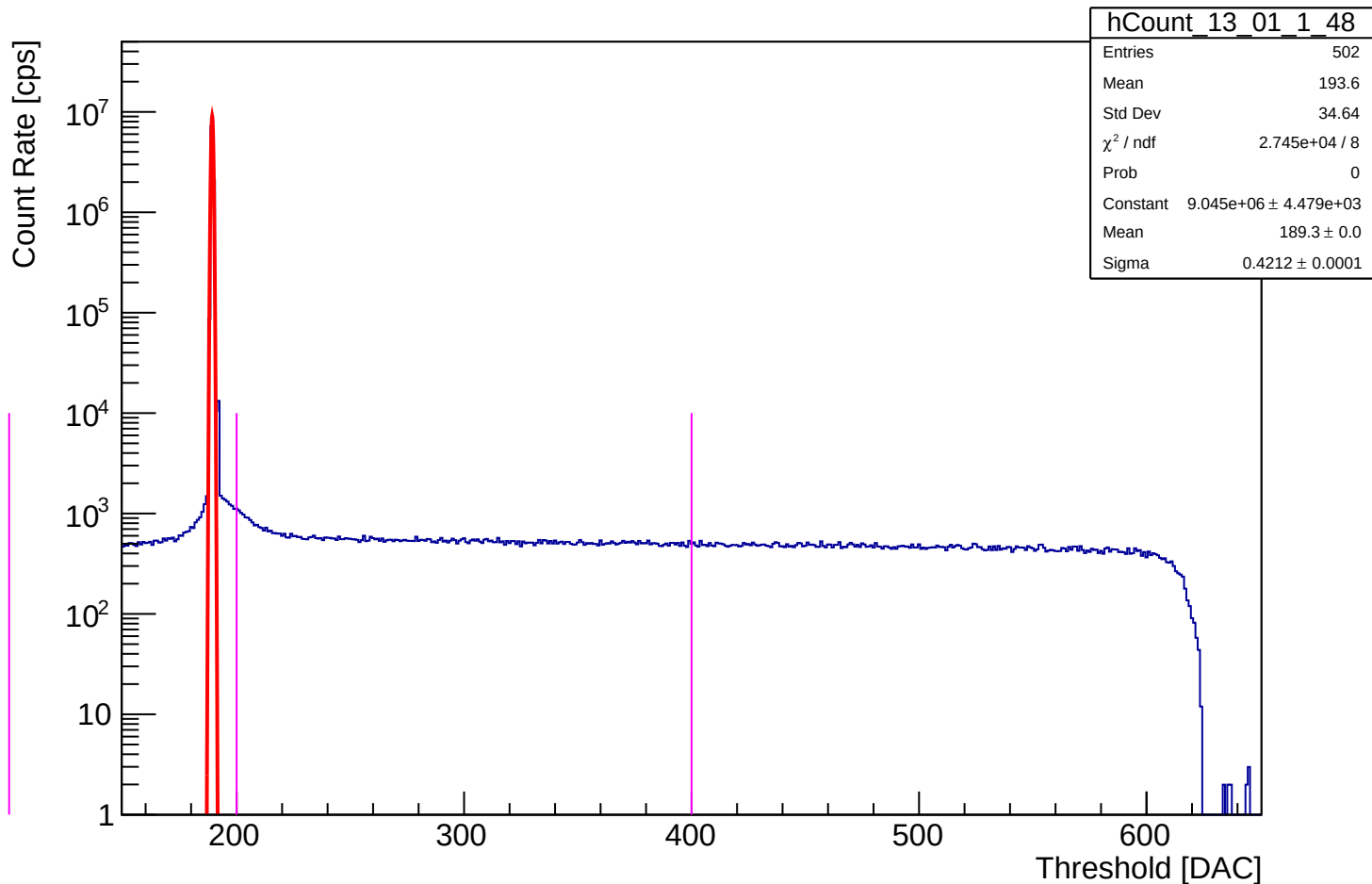
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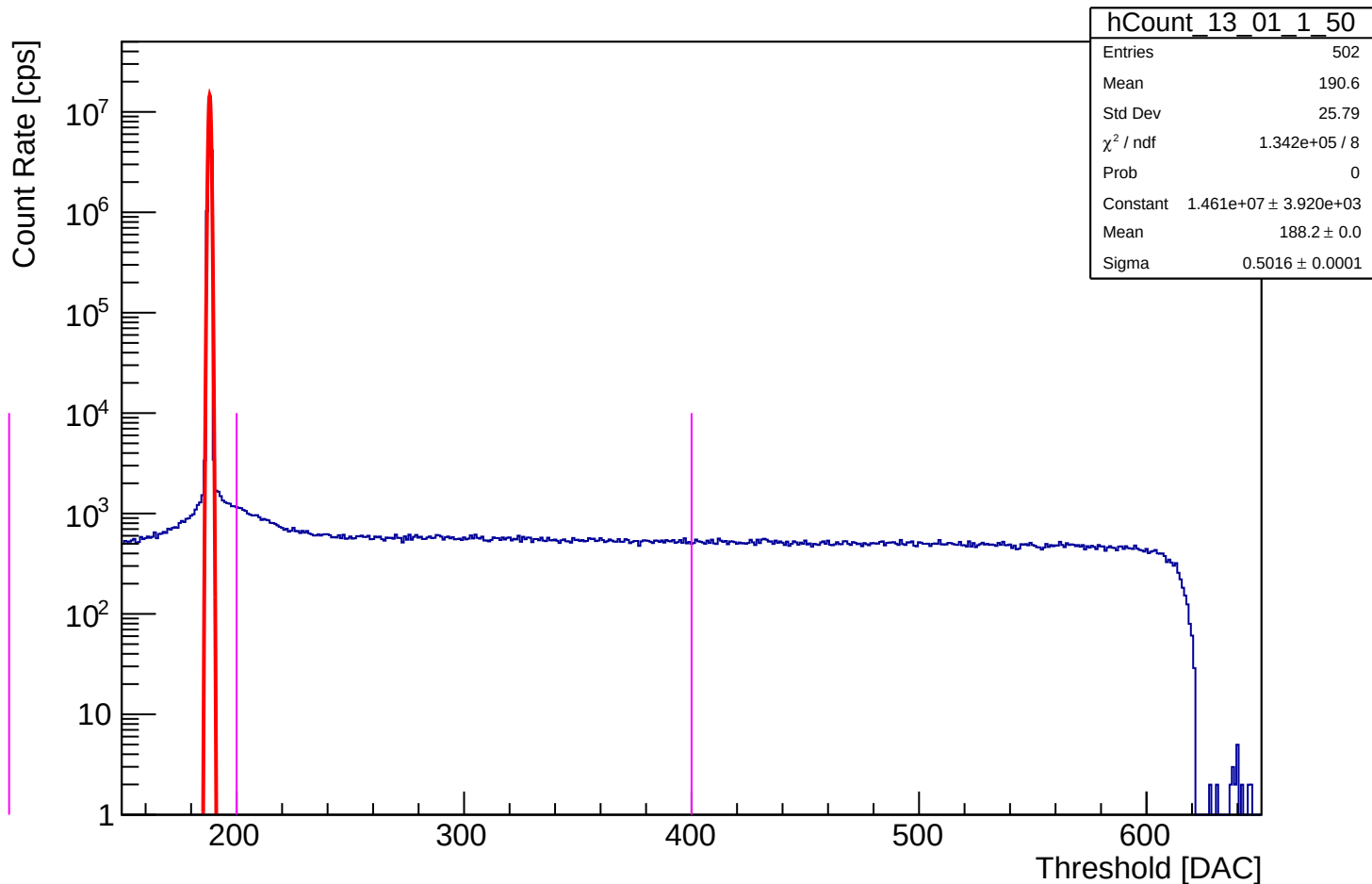
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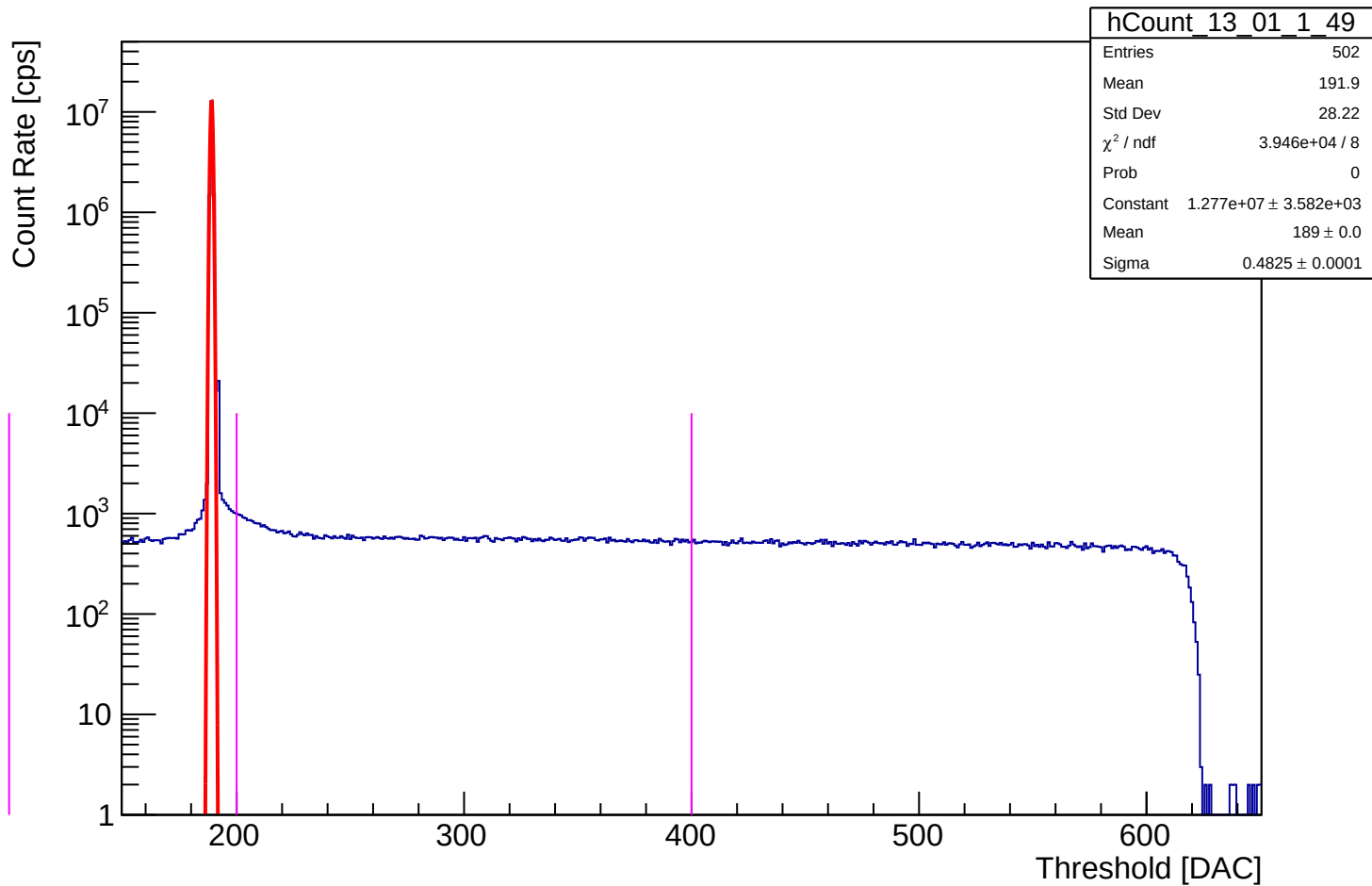
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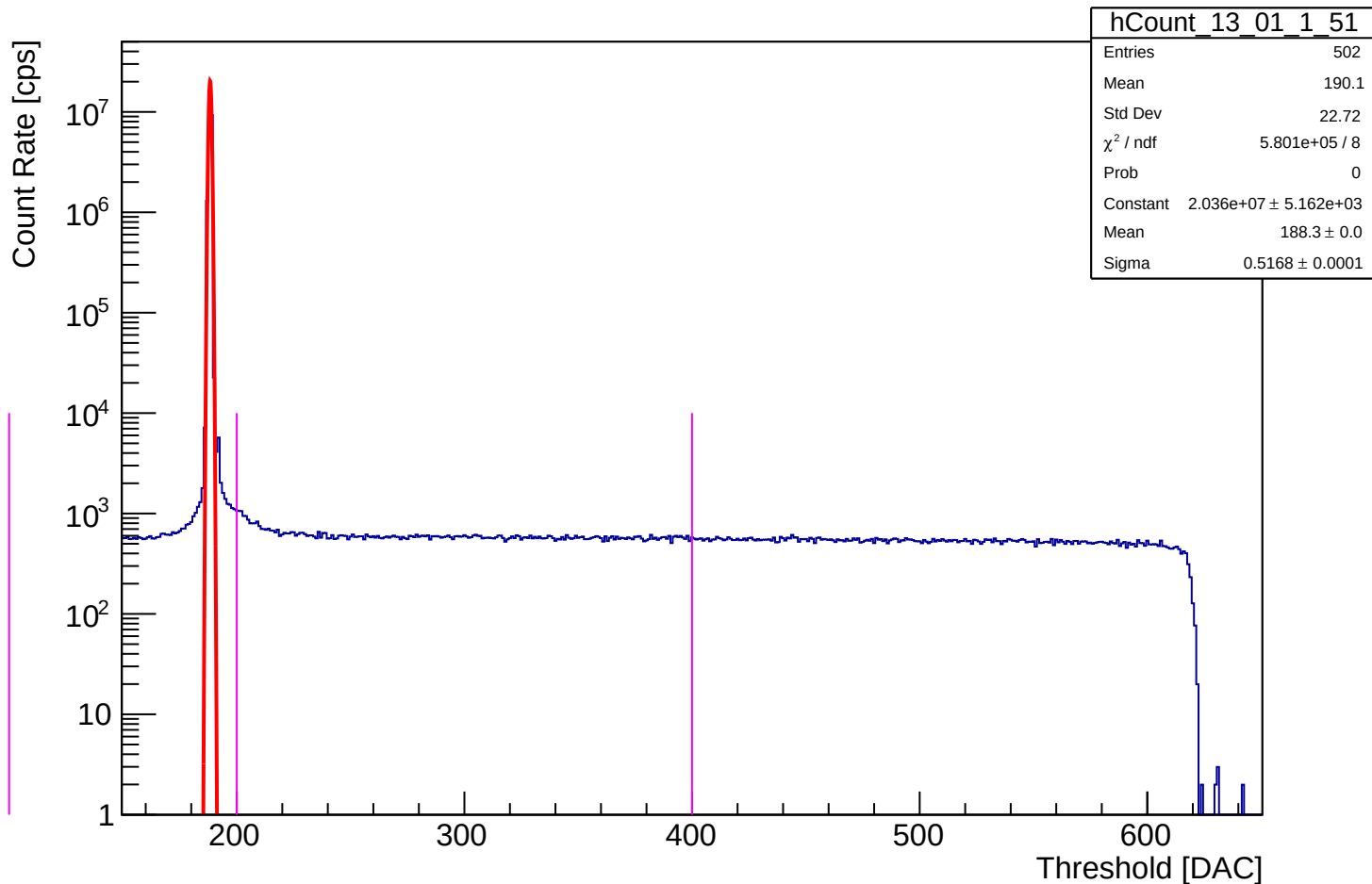


Row 1 Tile 1 Pmt 5 Pixel 38 Slot 13 Fiber 1 Asic 1 Channel 50

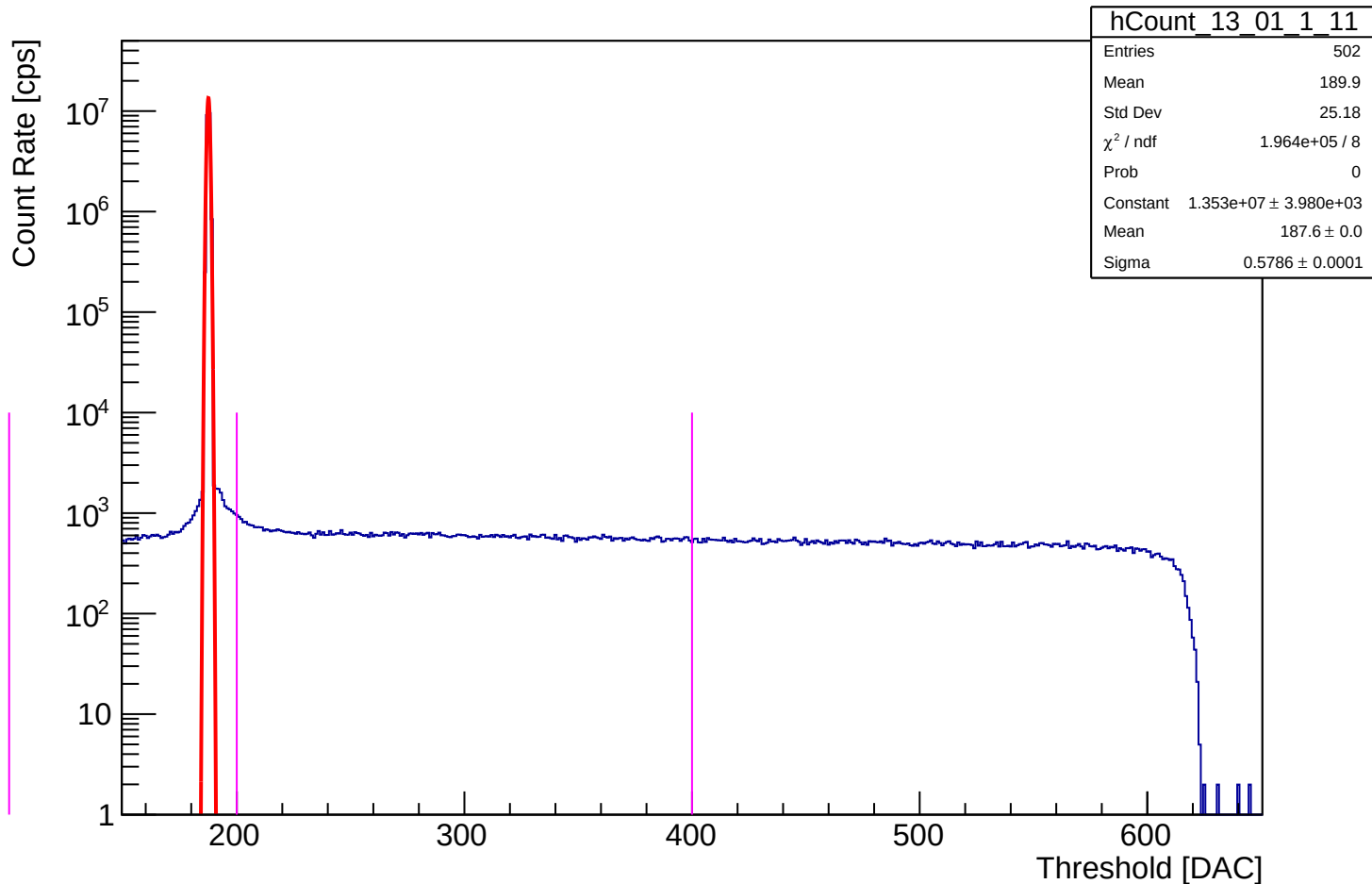


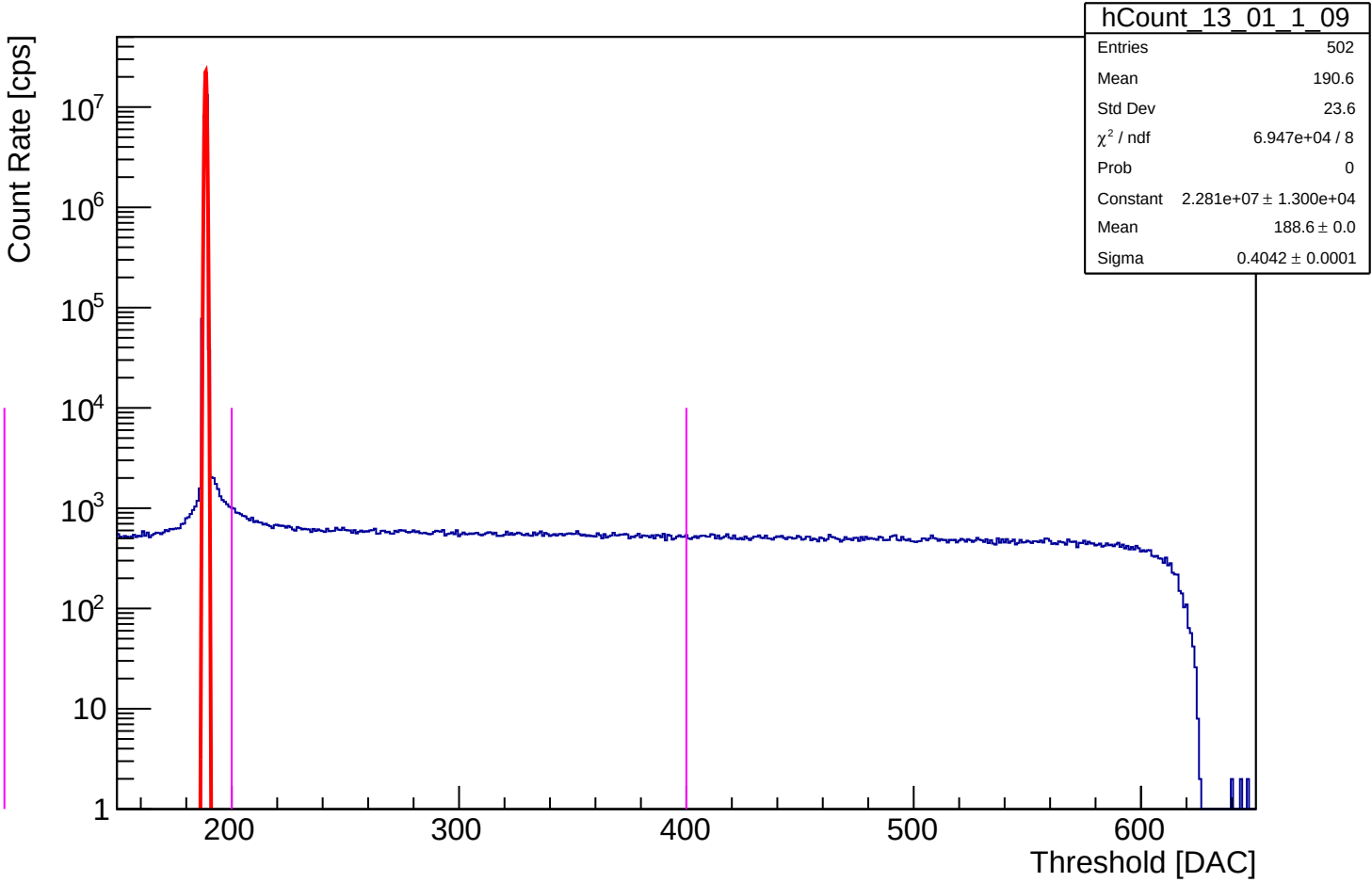
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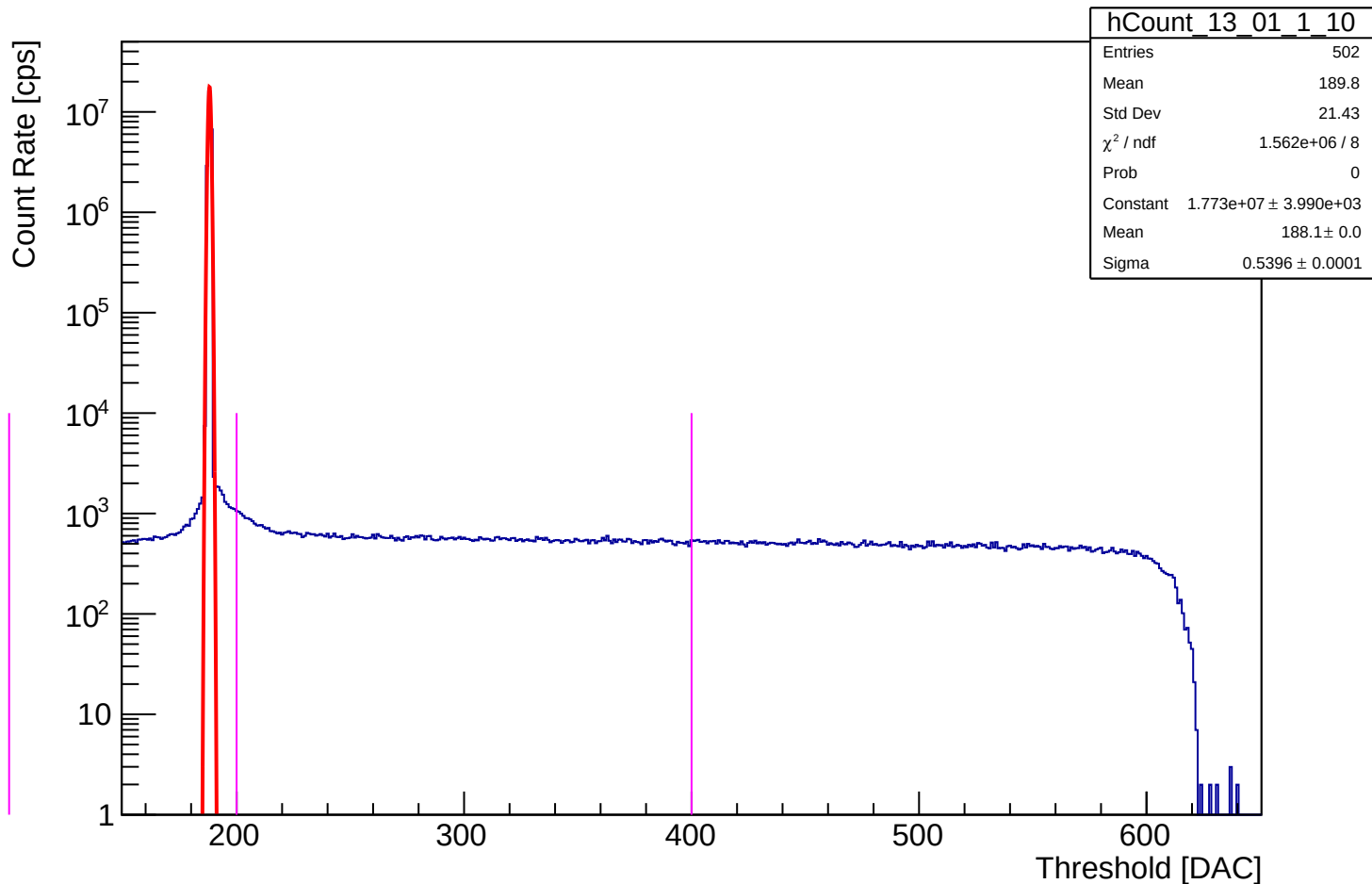


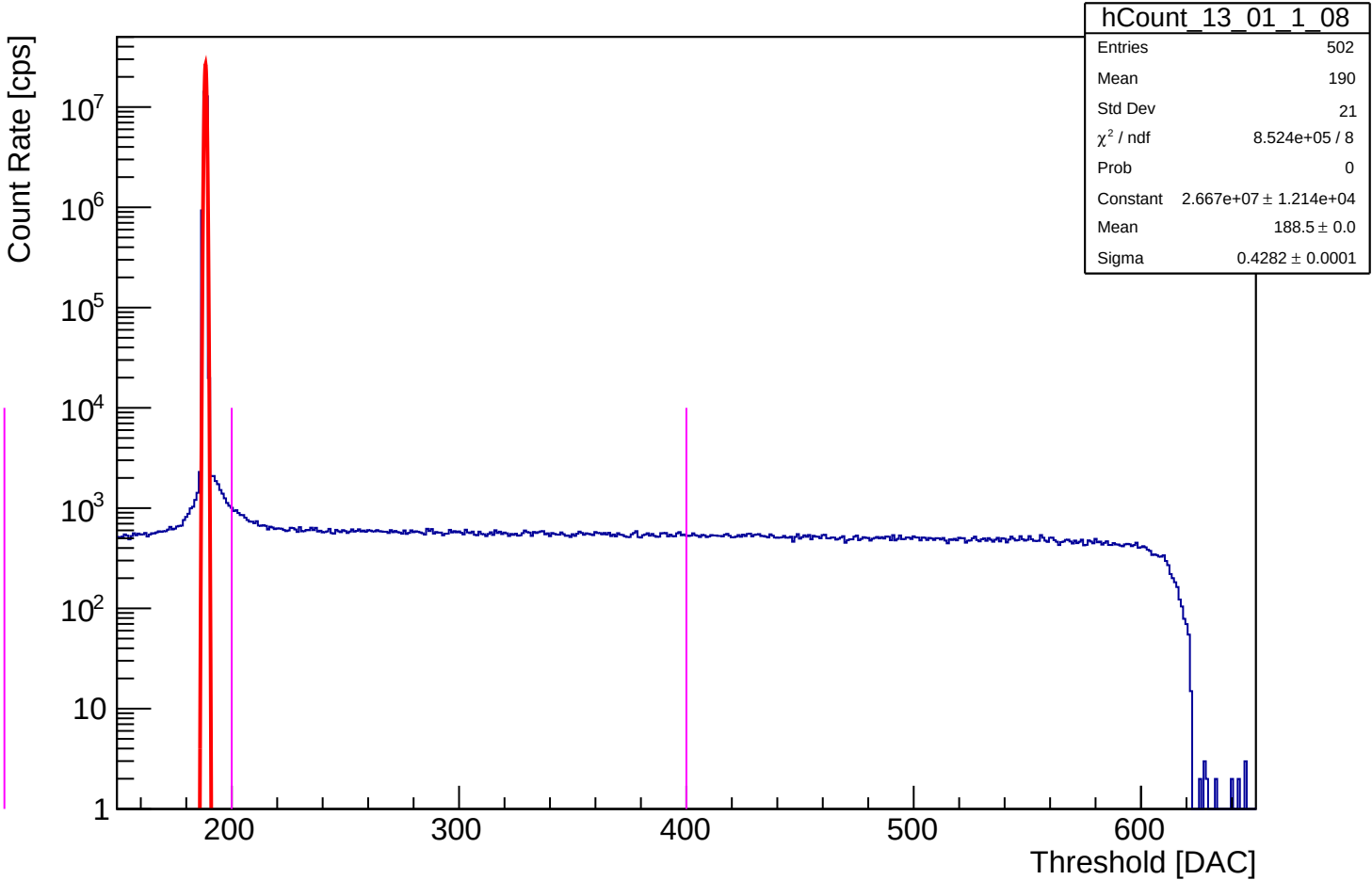
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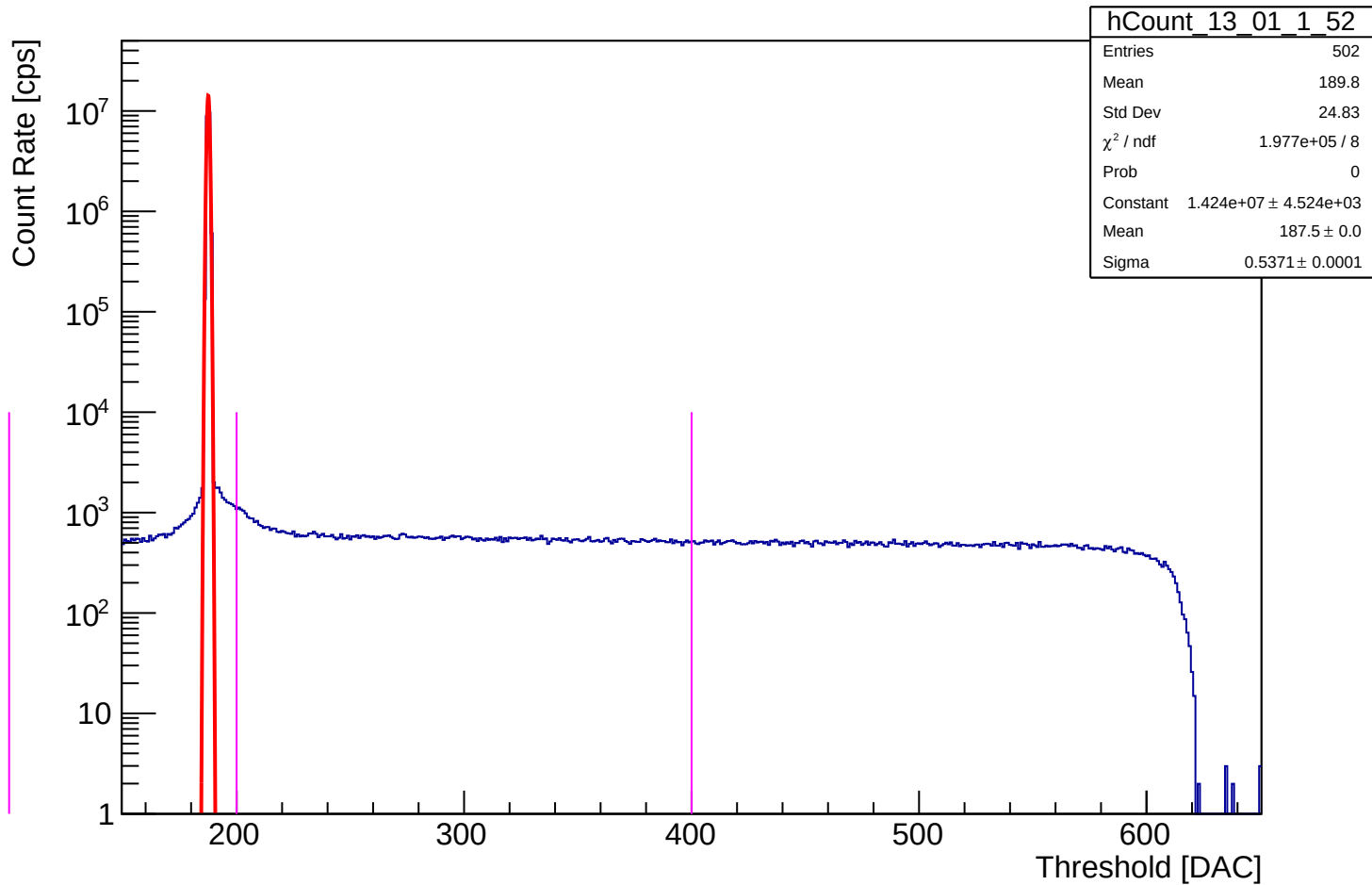


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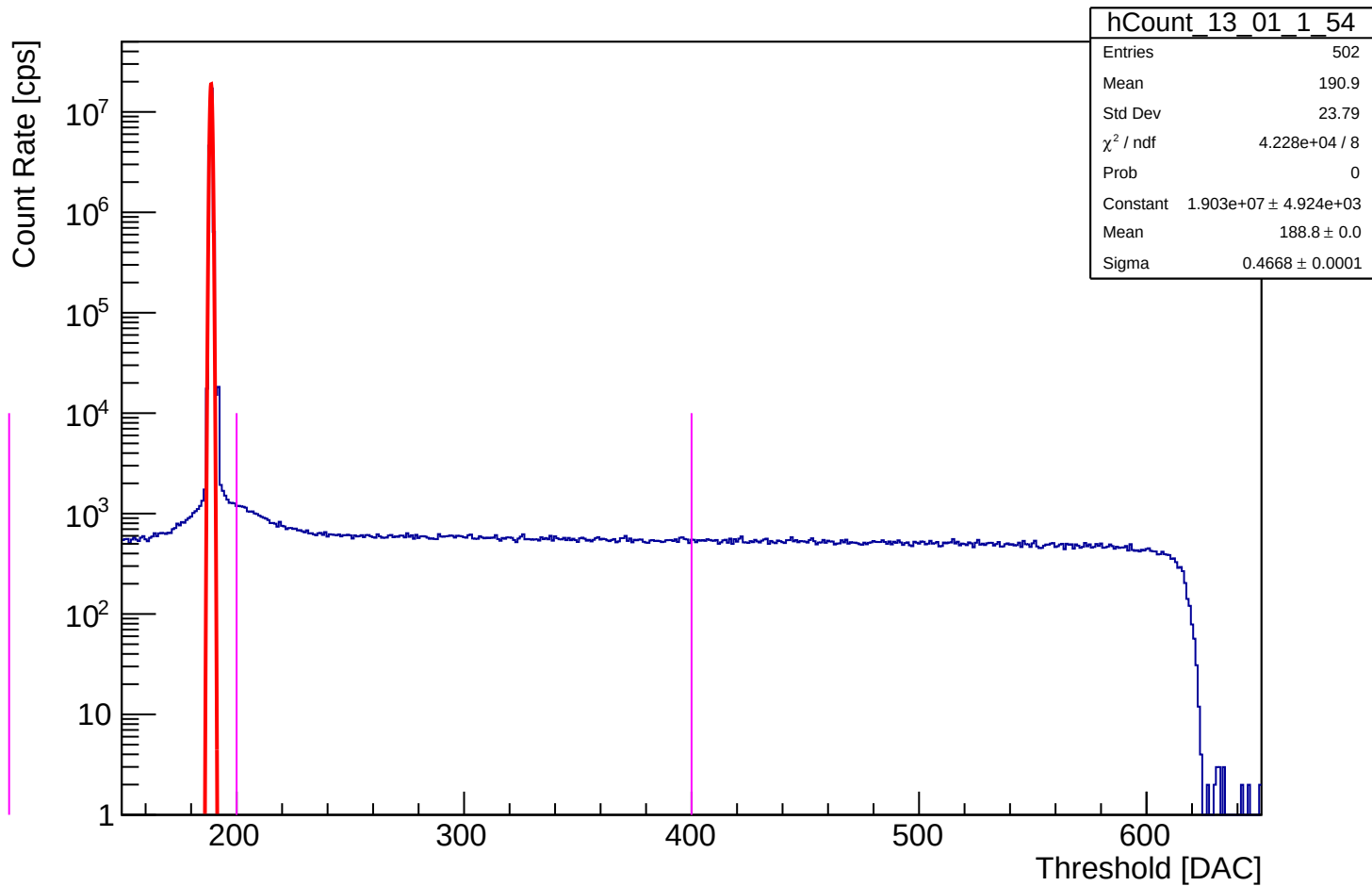




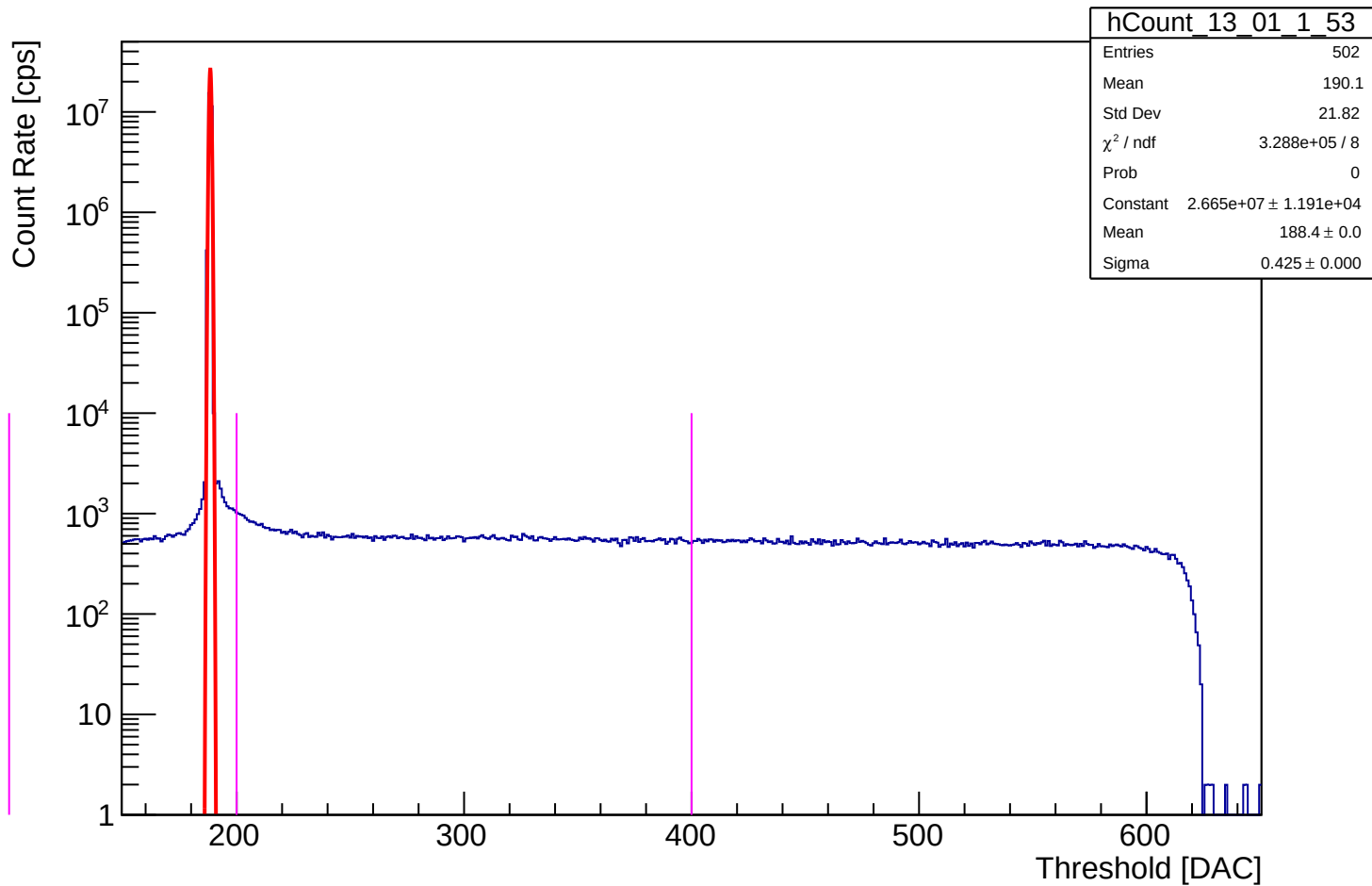
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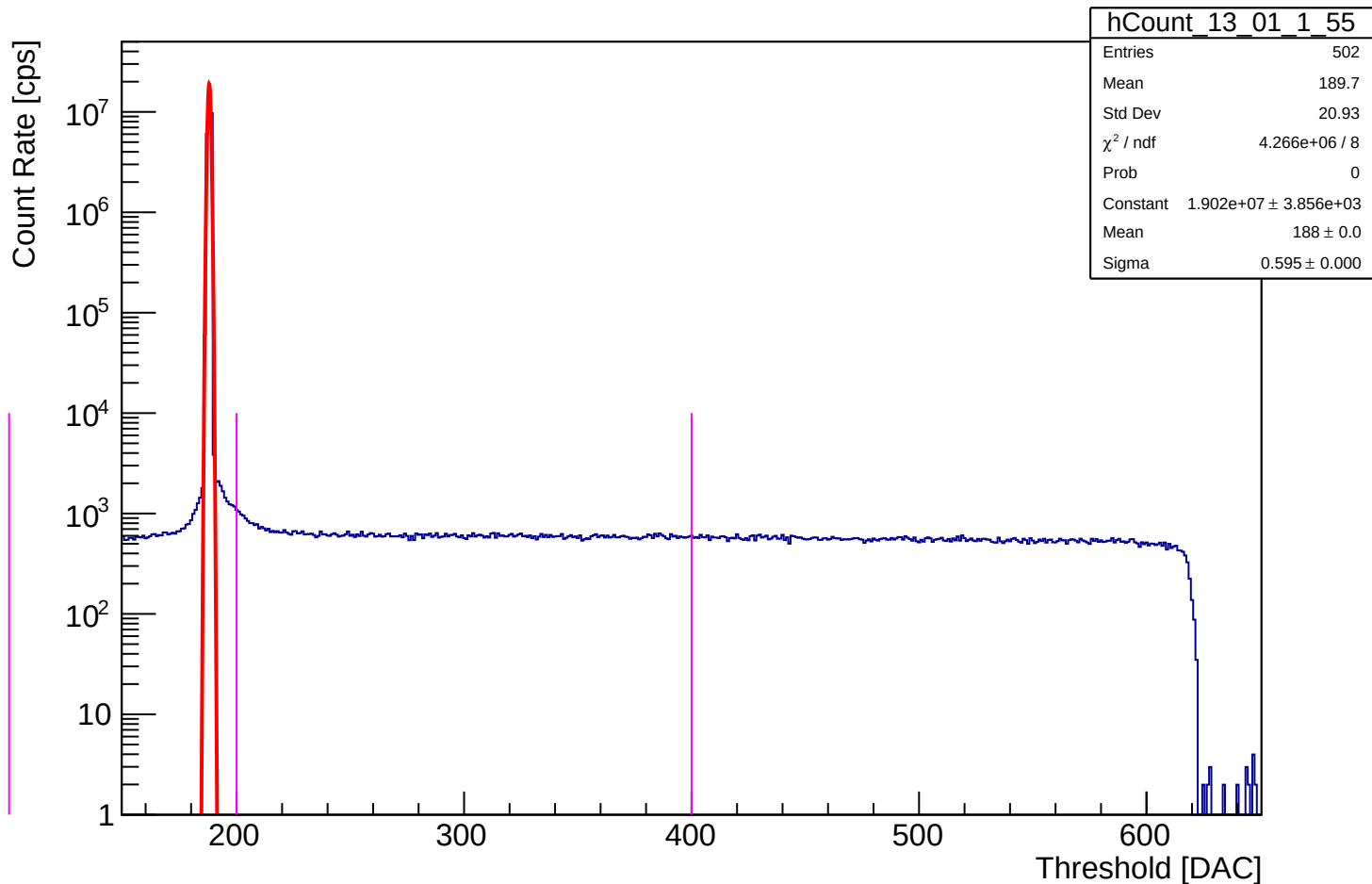
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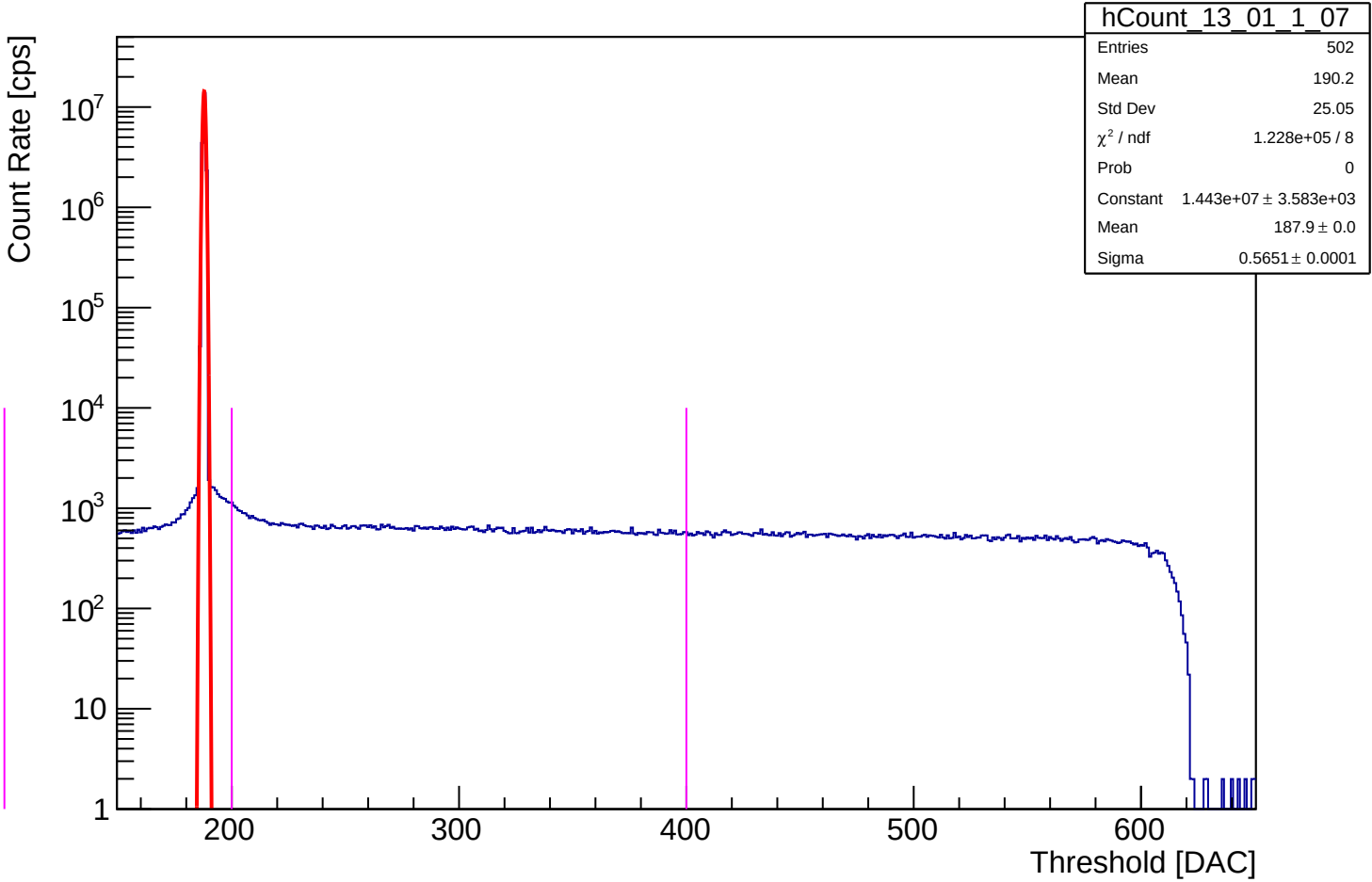


Row 1 Tile 1 Pmt 5 Pixel 47 Slot 13 Fiber 1 Asic 1 Channel 53

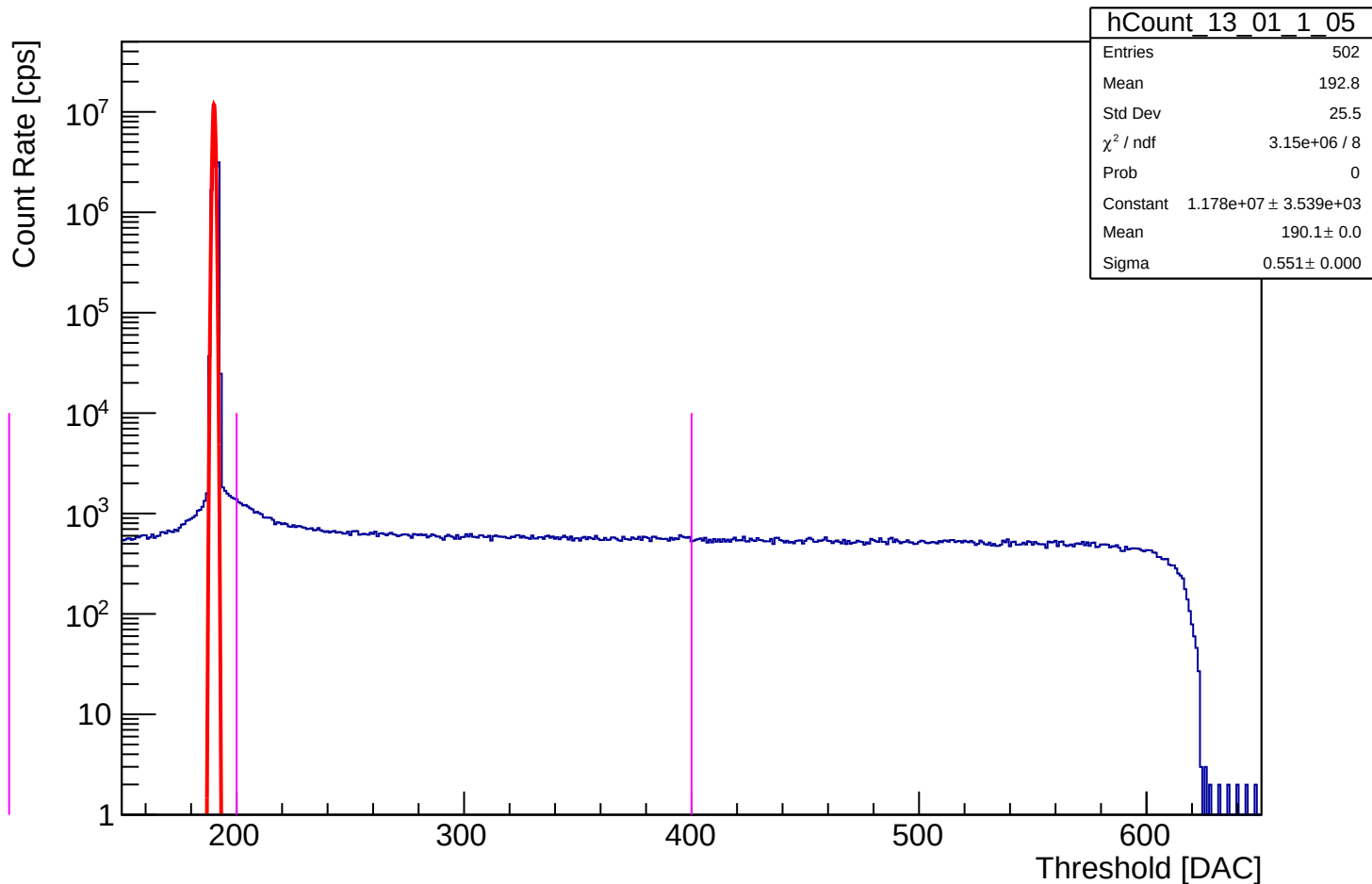


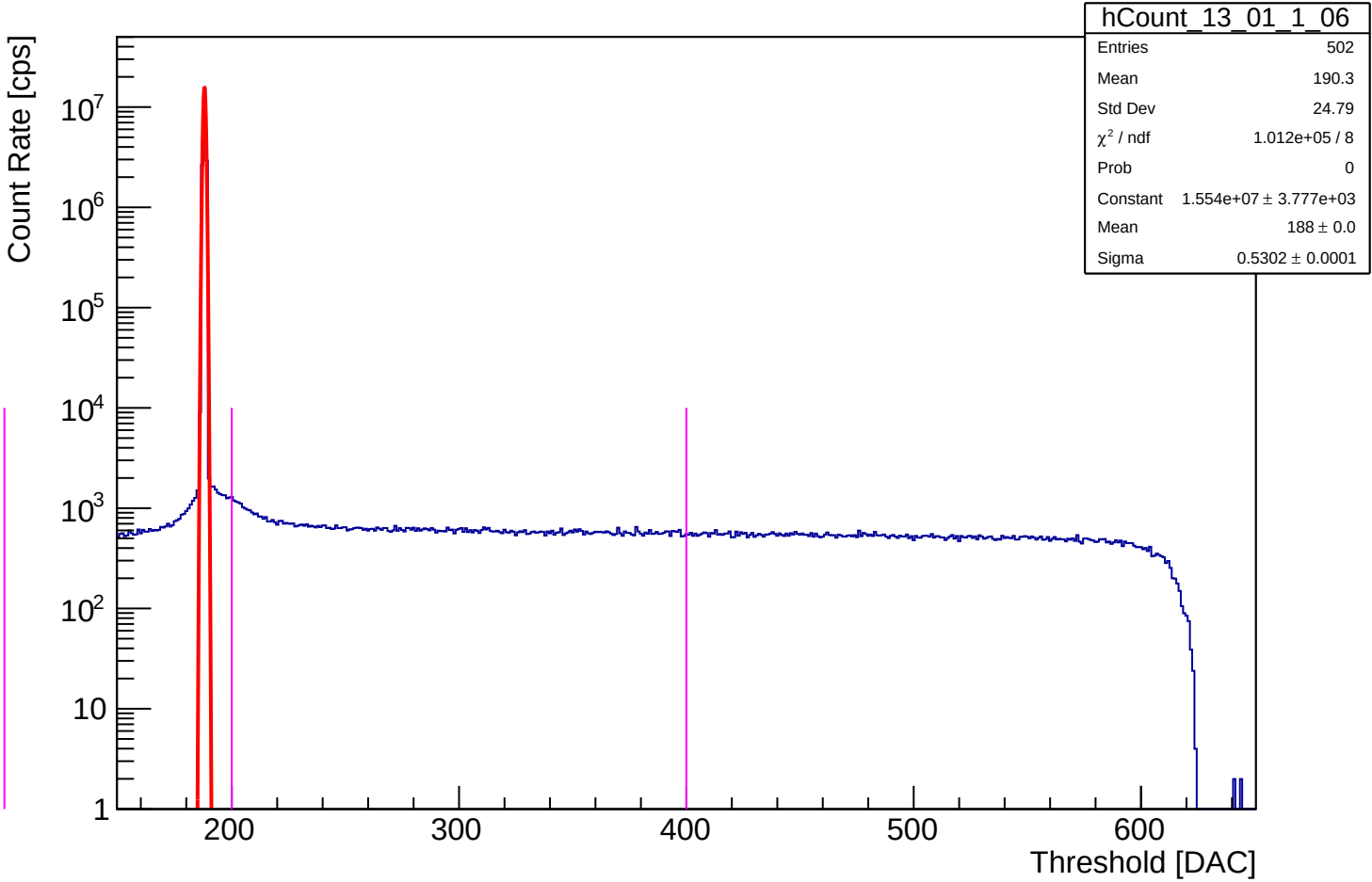
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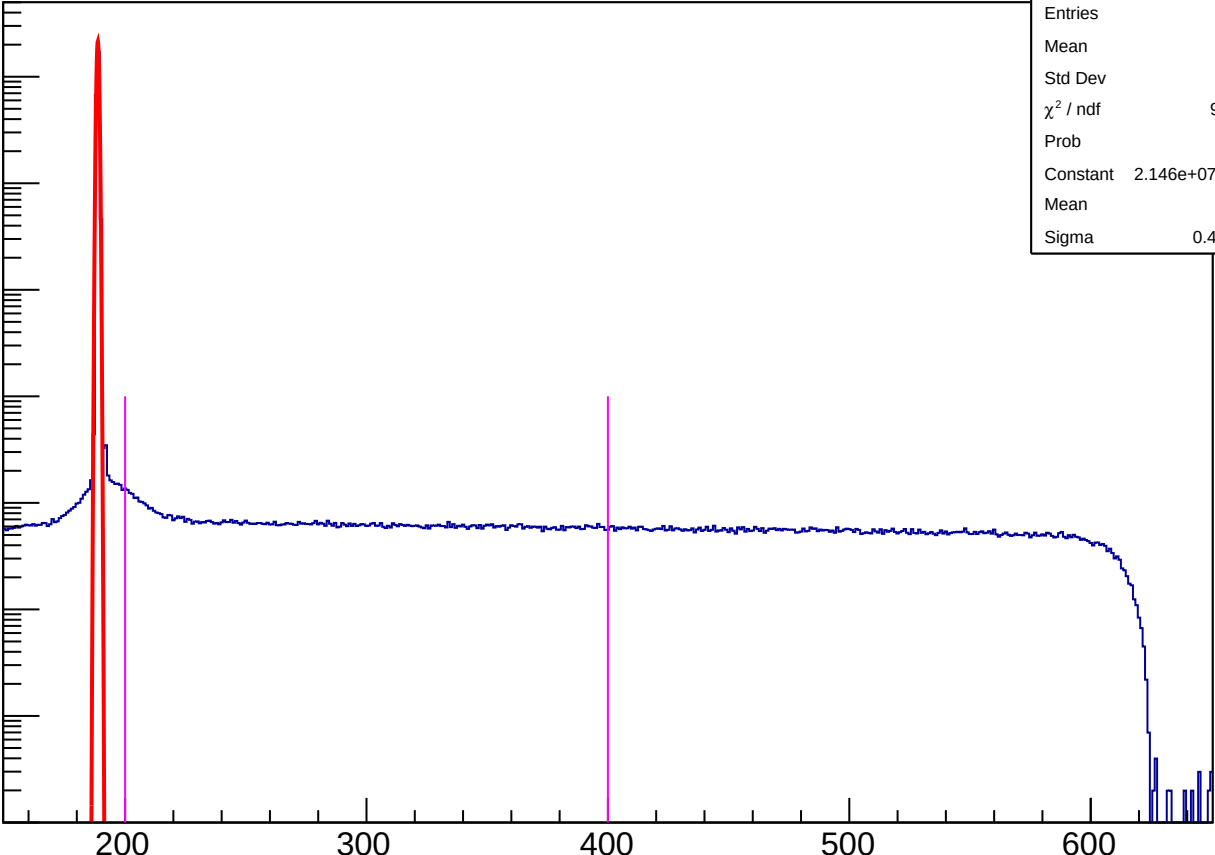
Row 1 Tile 1 Pmt 5 Pixel 50 Slot 13 Fiber 1 Asic 1 Channel 5





Count Rate [cps]

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10⁶
10⁵
10⁴
10³
10²
10
1

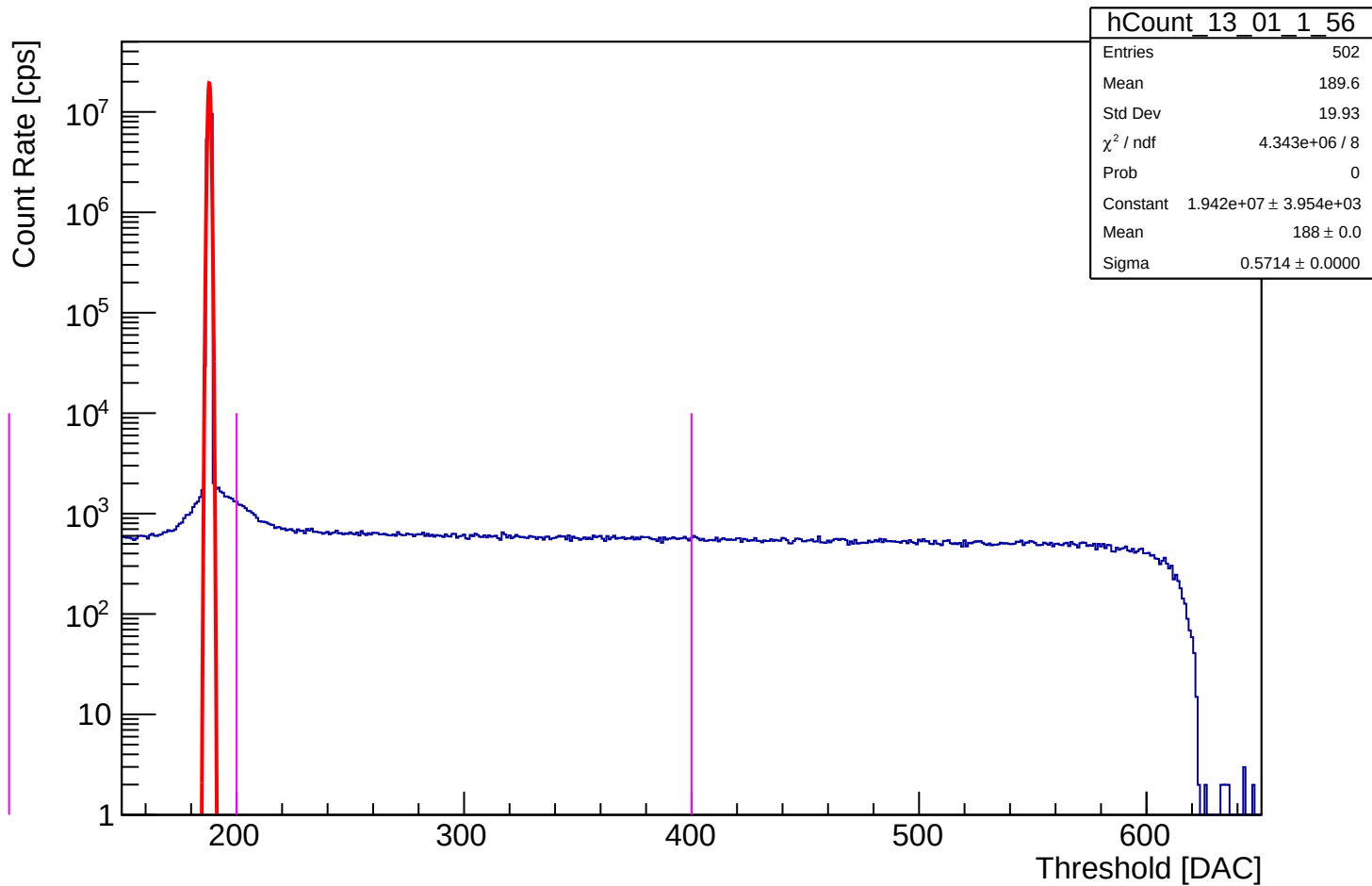


hCount 13 01 1 04

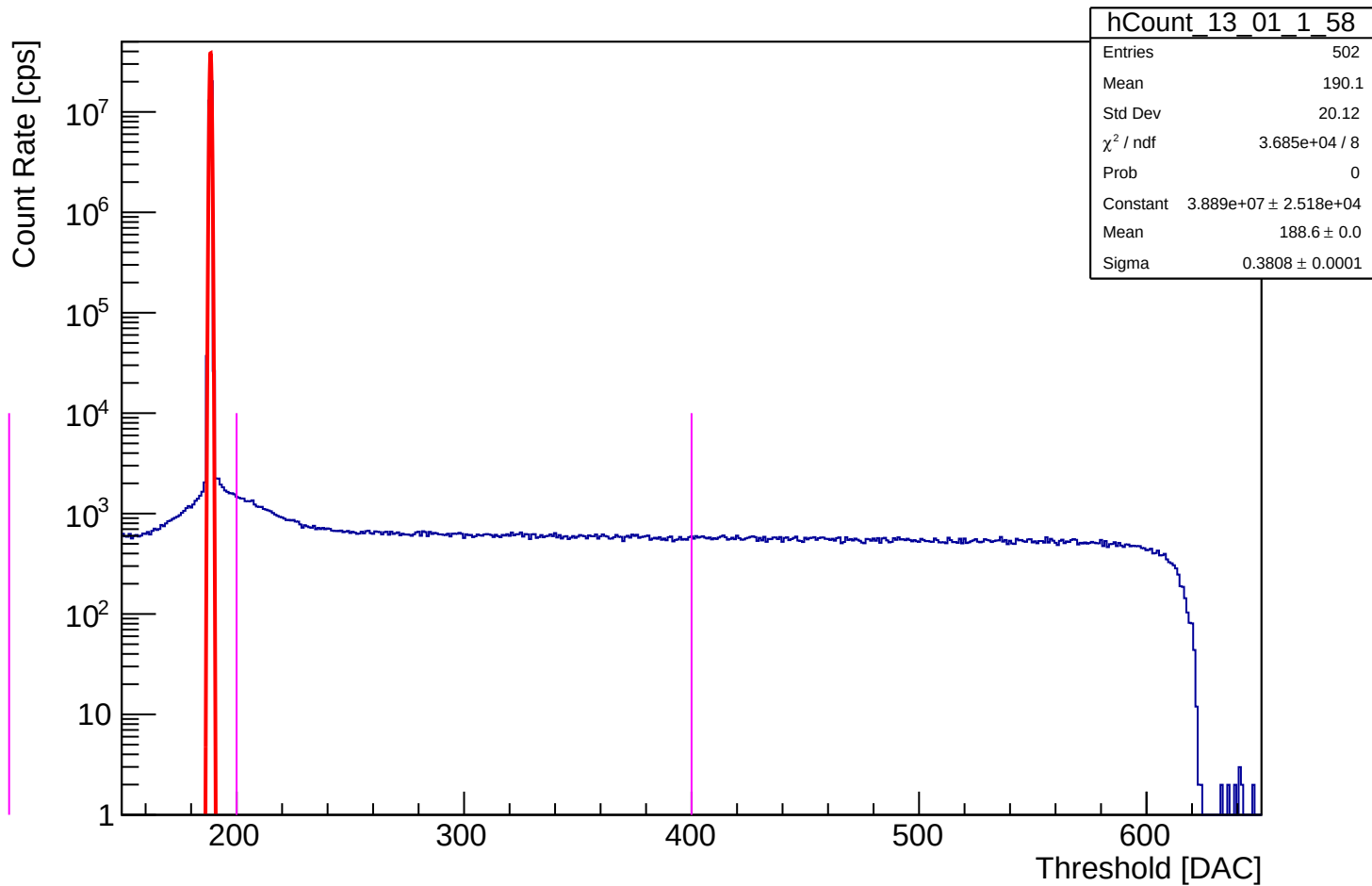
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Mean	190.7
Std Dev	23.42
χ^2 / ndf	9.132e+04 / 8
Prob	0
Constant	2.146e+07 ± 6.003e+03
Mean	188.7 ± 0.0
Sigma	0.4559 ± 0.0001

Threshold [DAC]

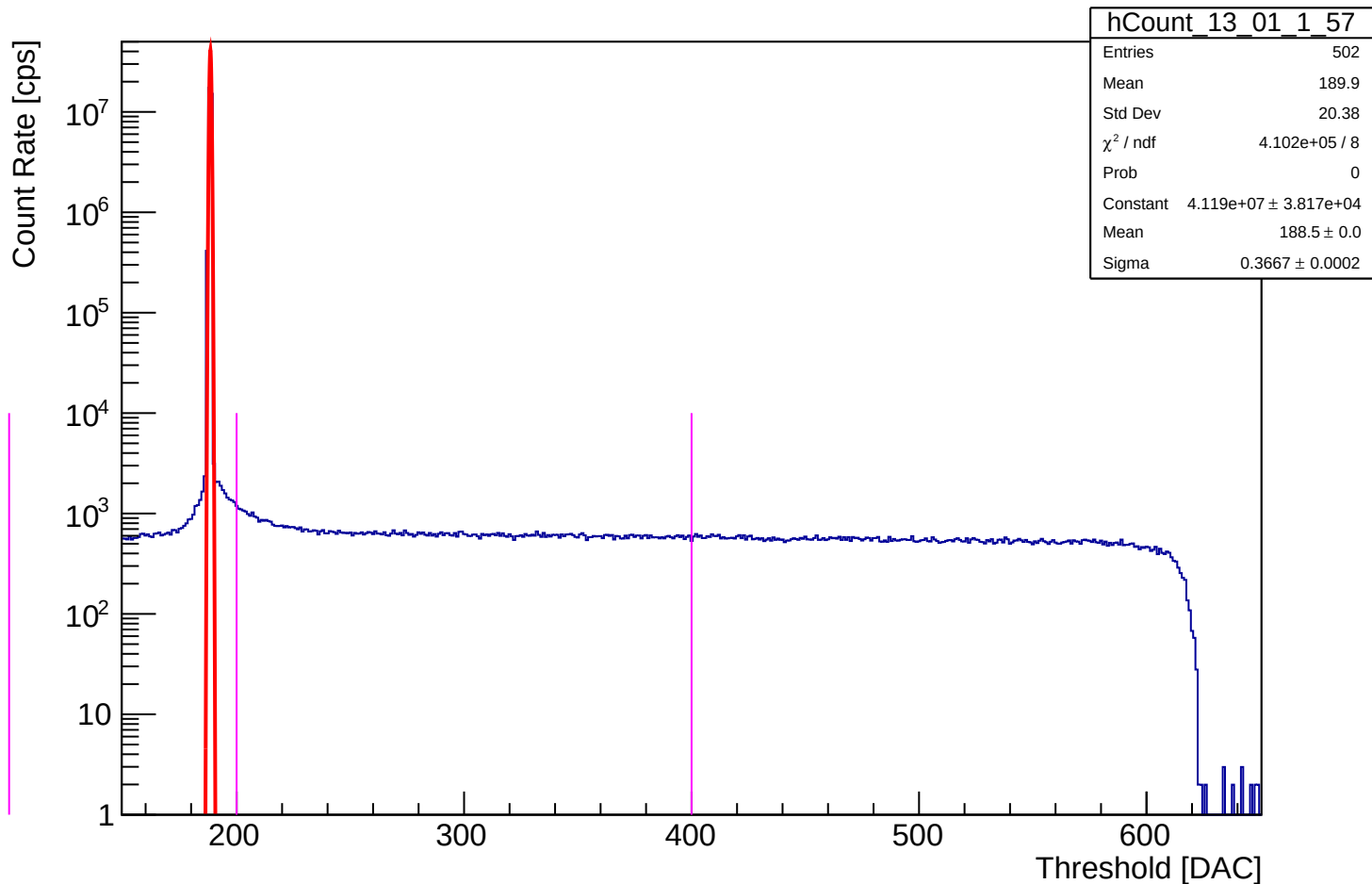
Row 1 Tile 1 Pmt 5 Pixel 53 Slot 13 Fiber 1 Asic 1 Channel 56

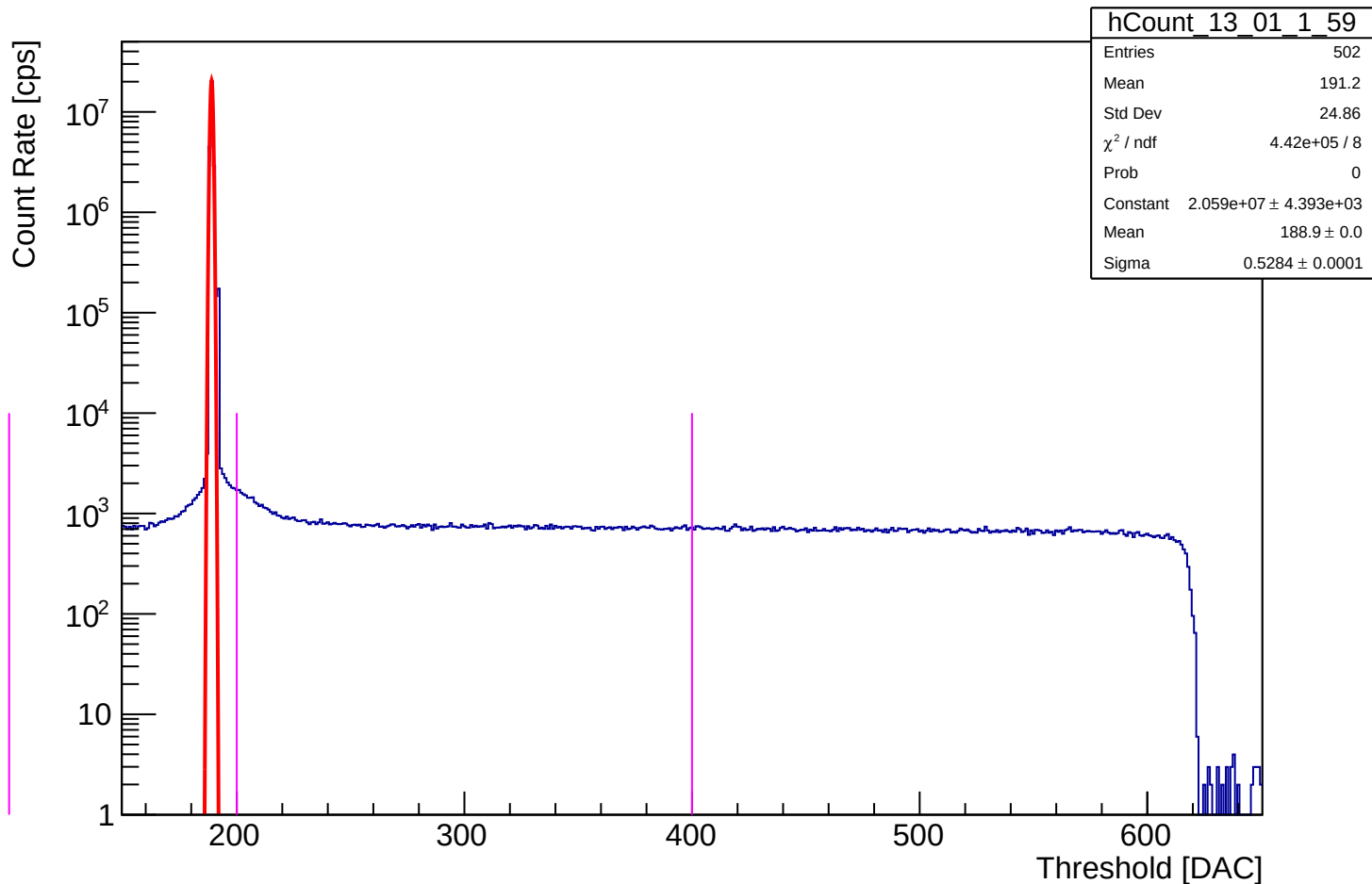


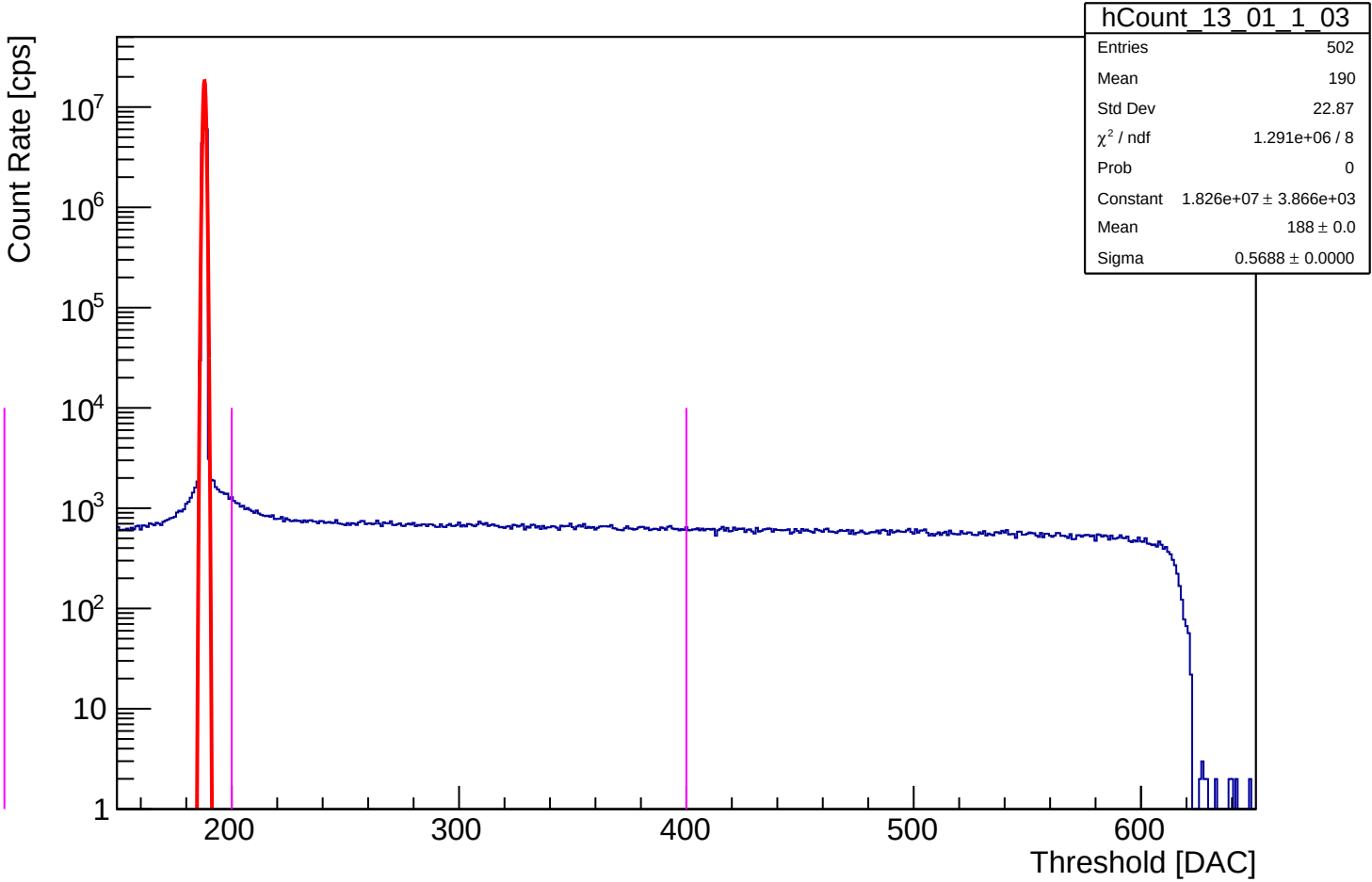
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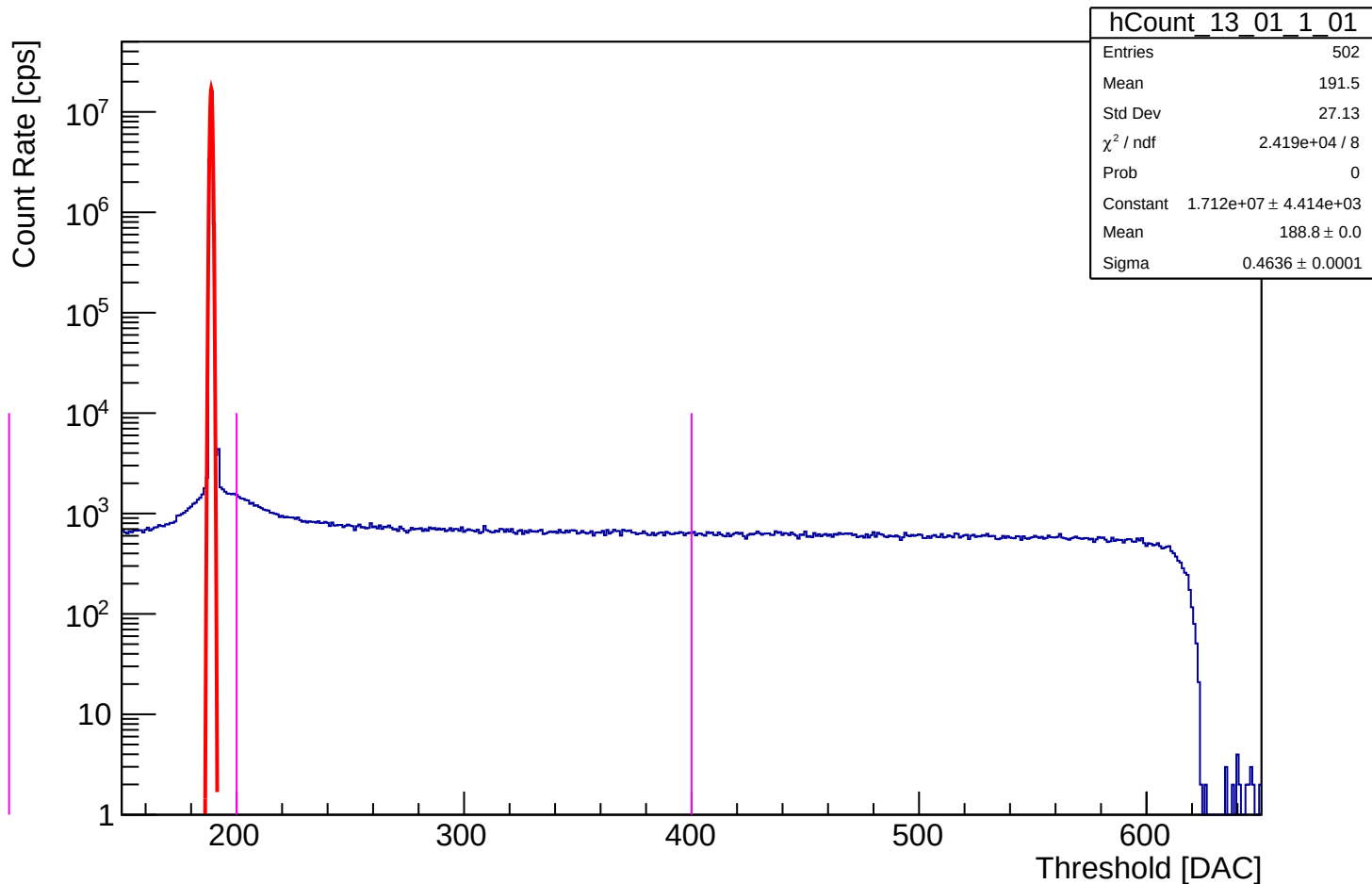
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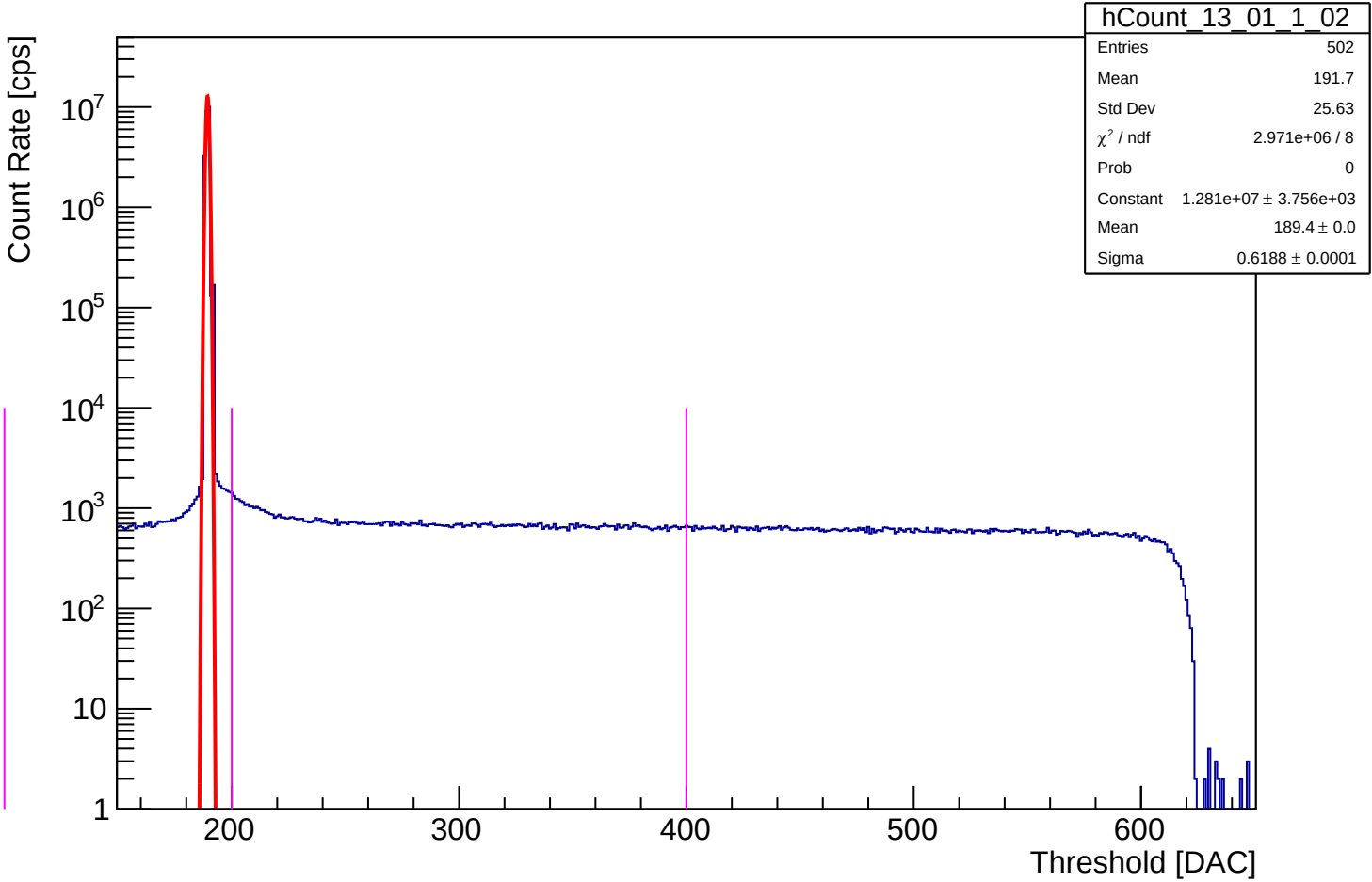


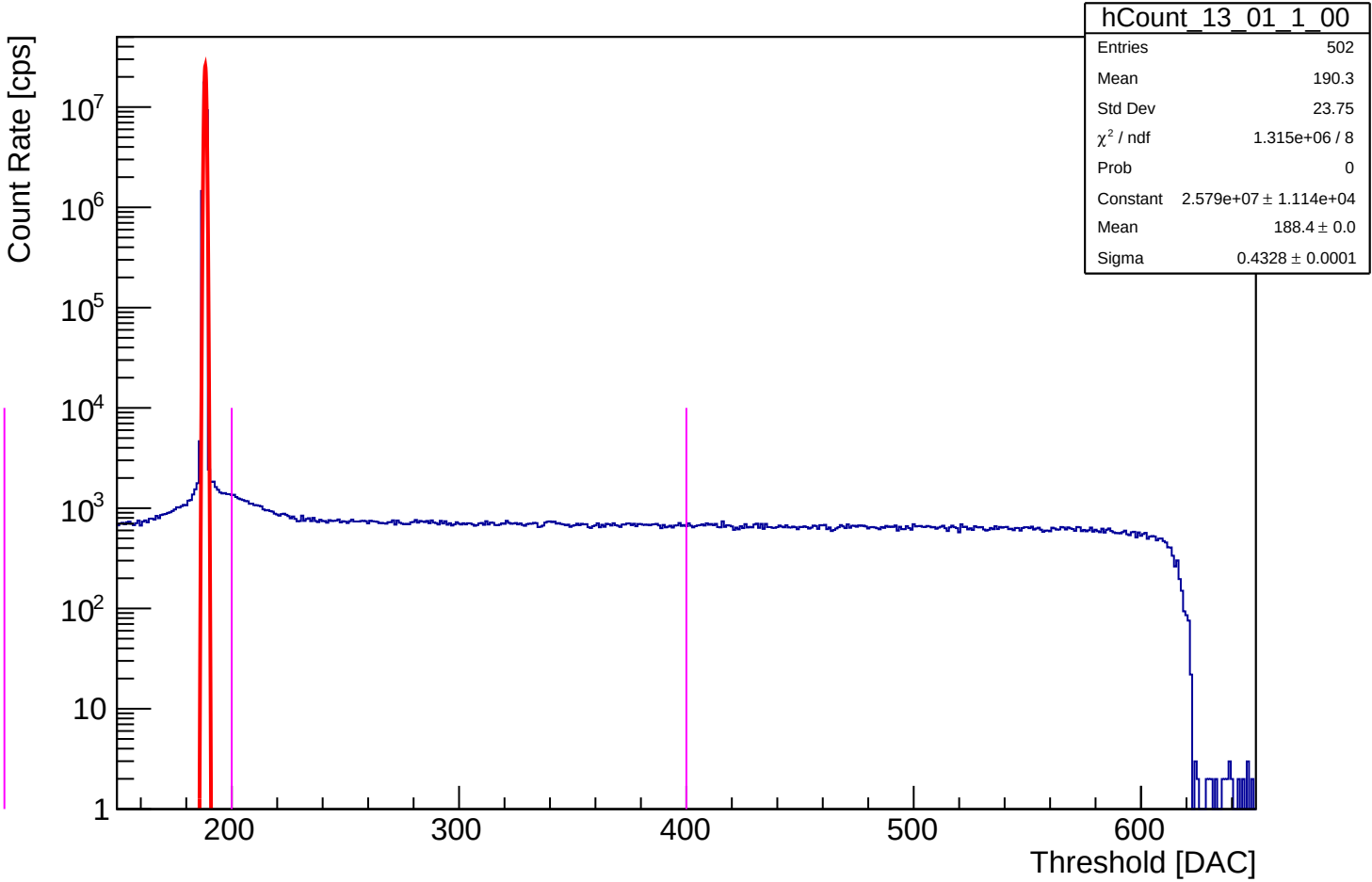




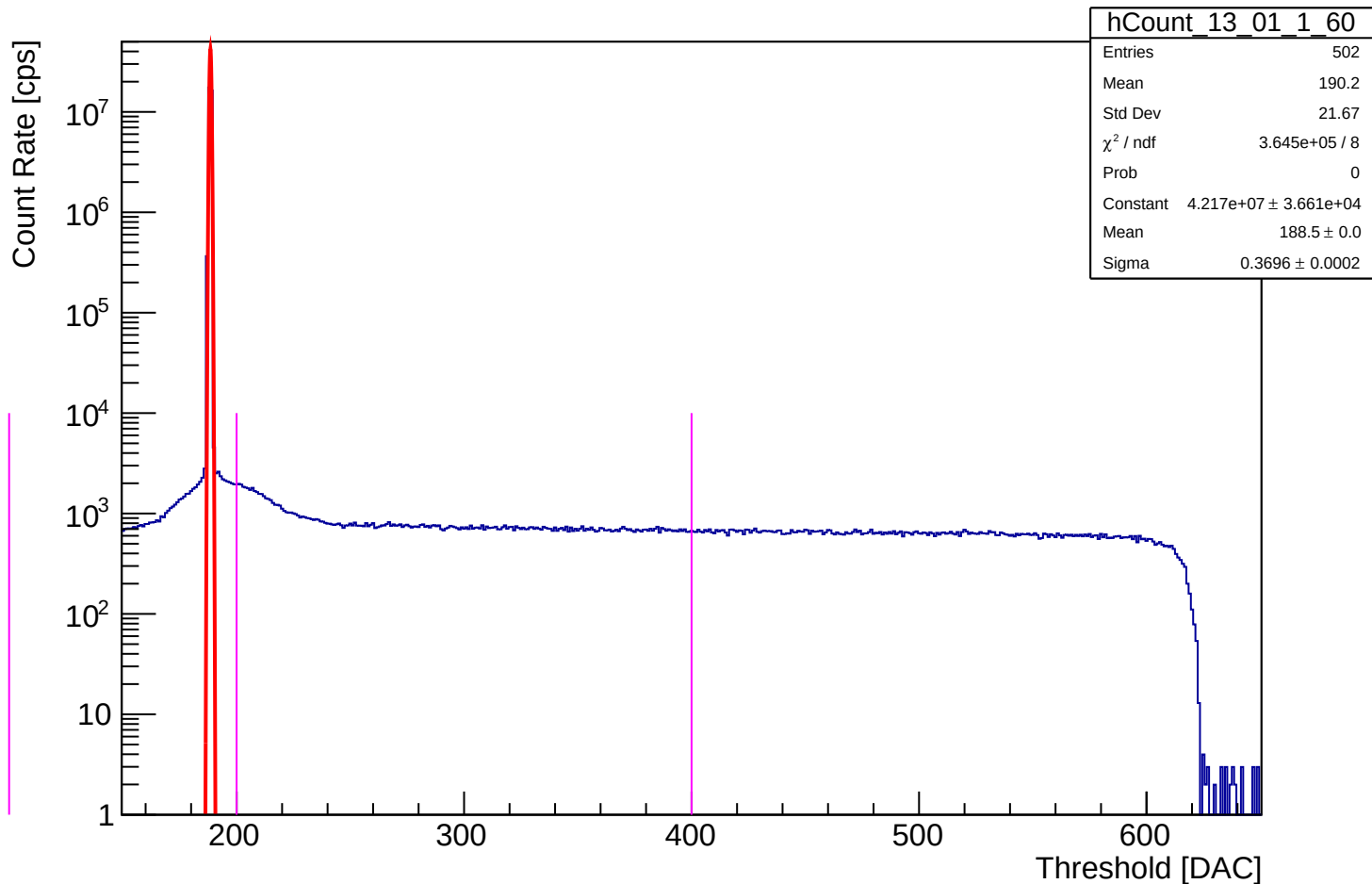
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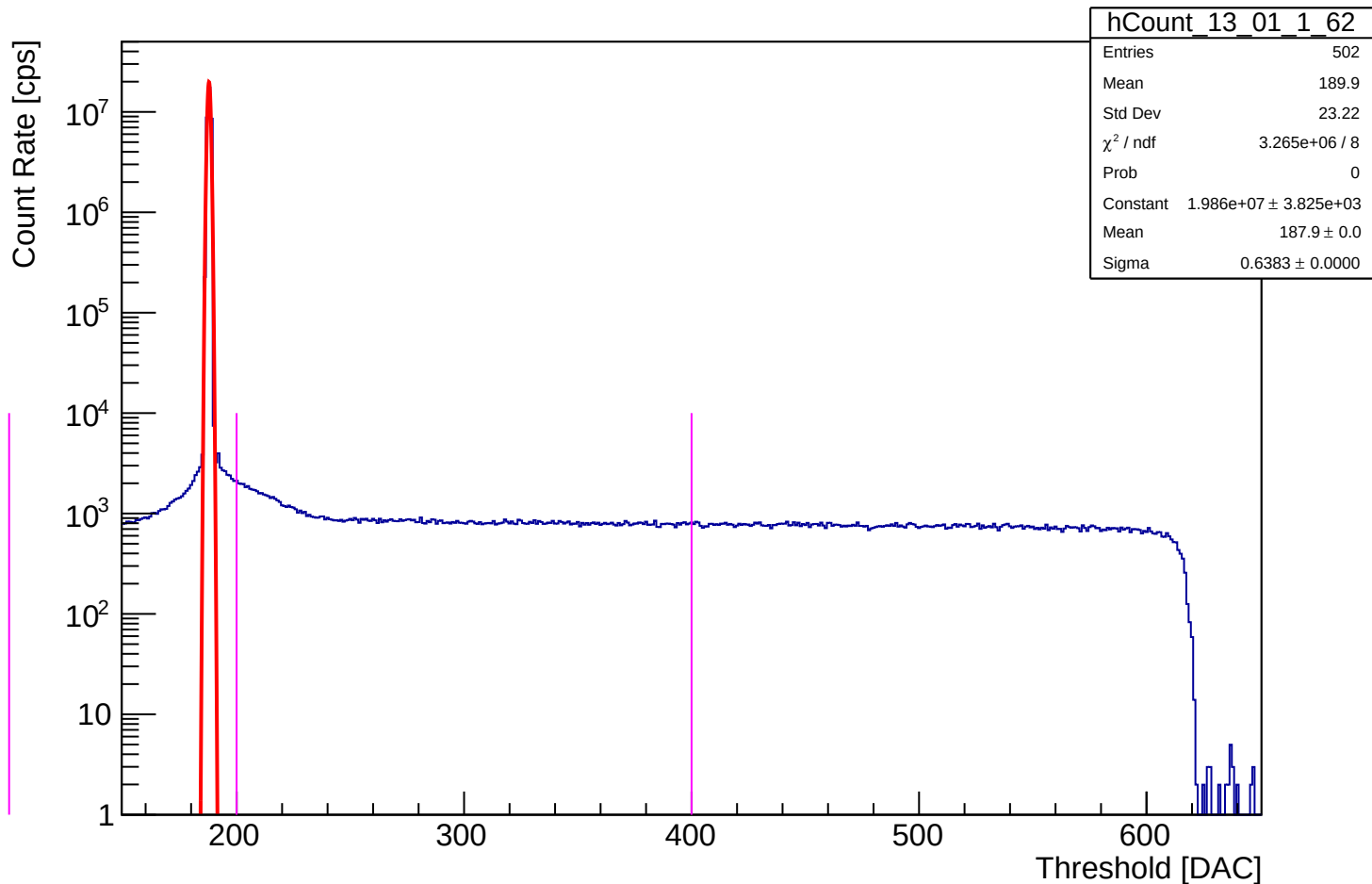




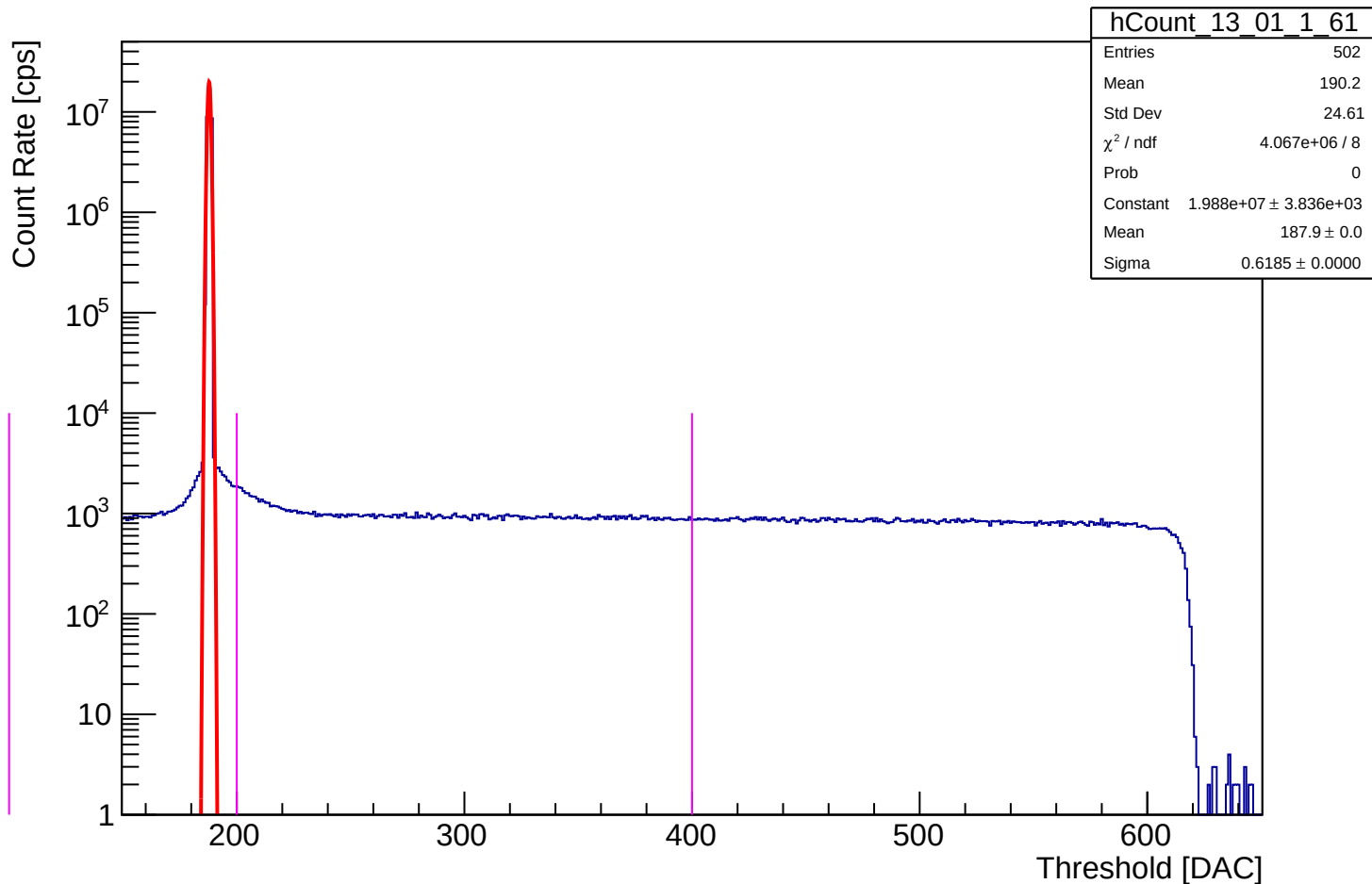
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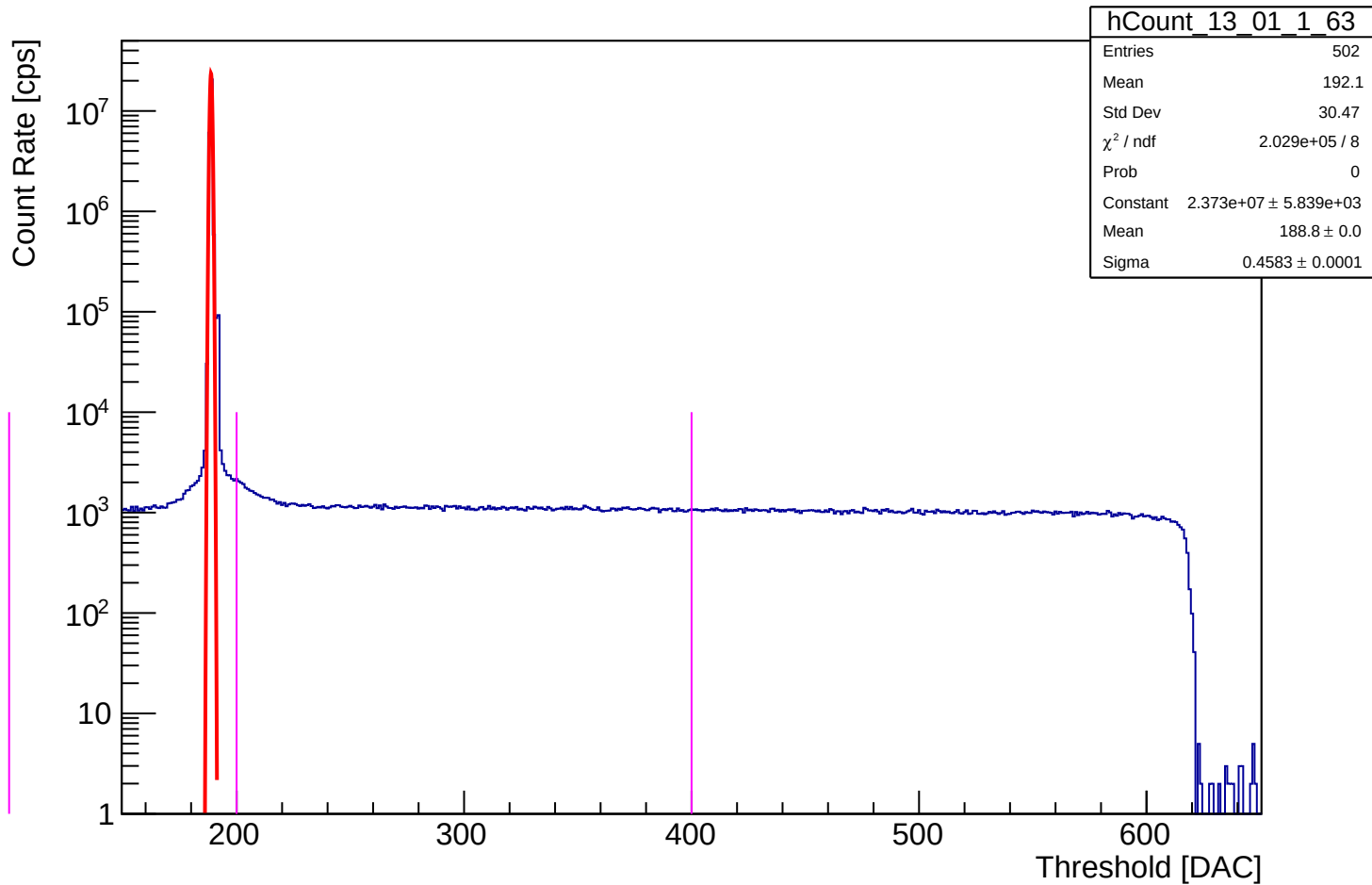
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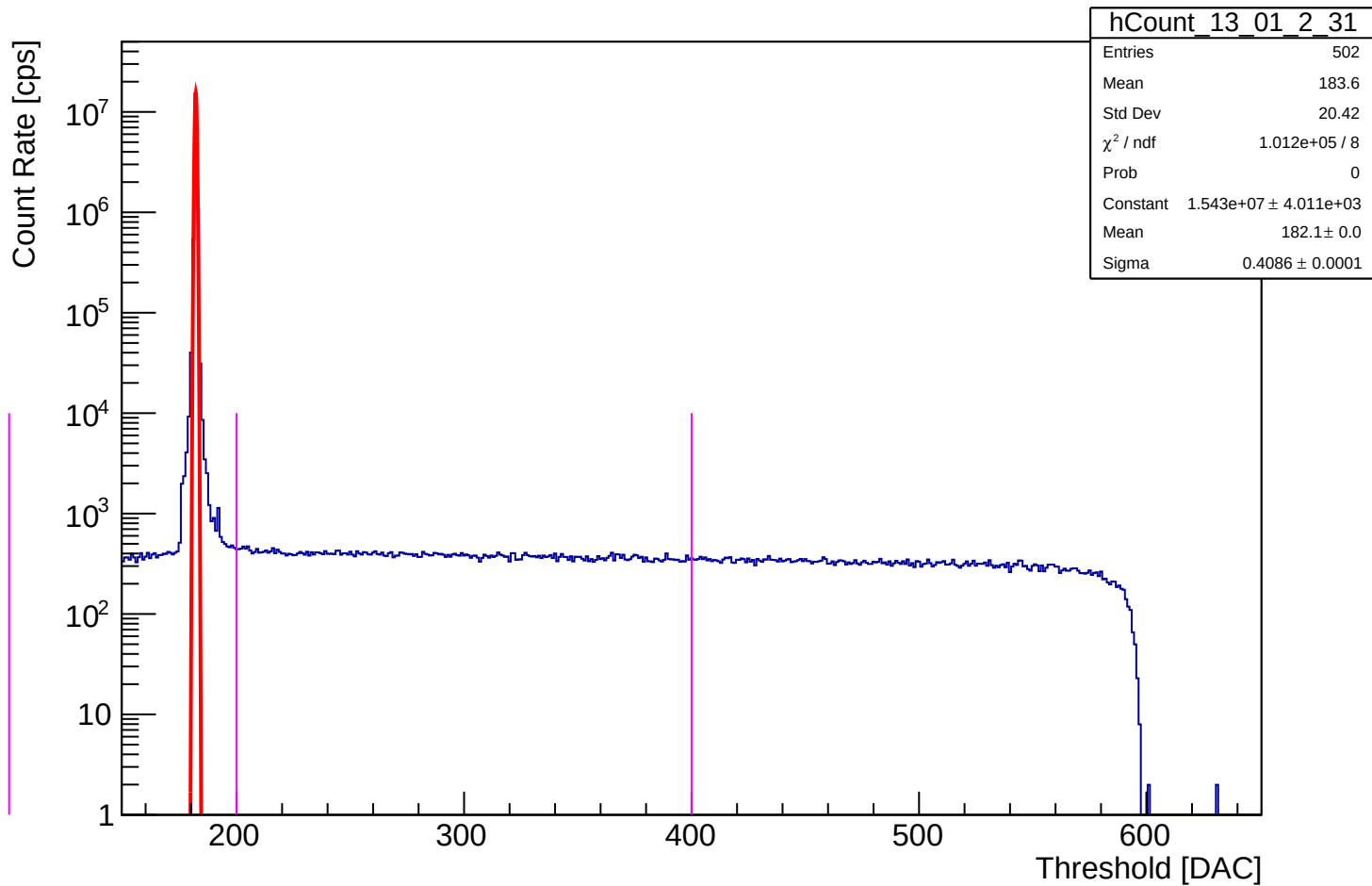
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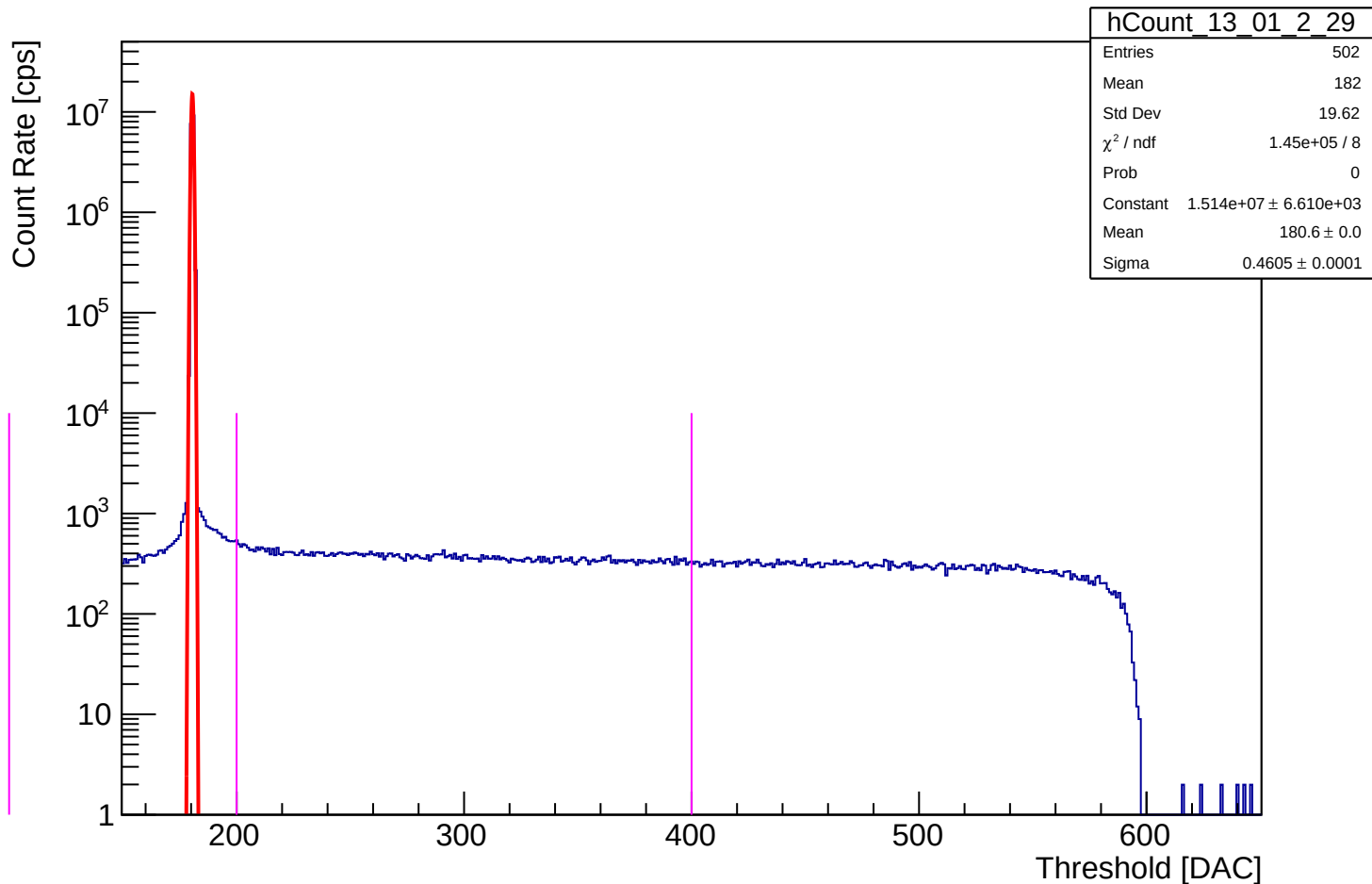
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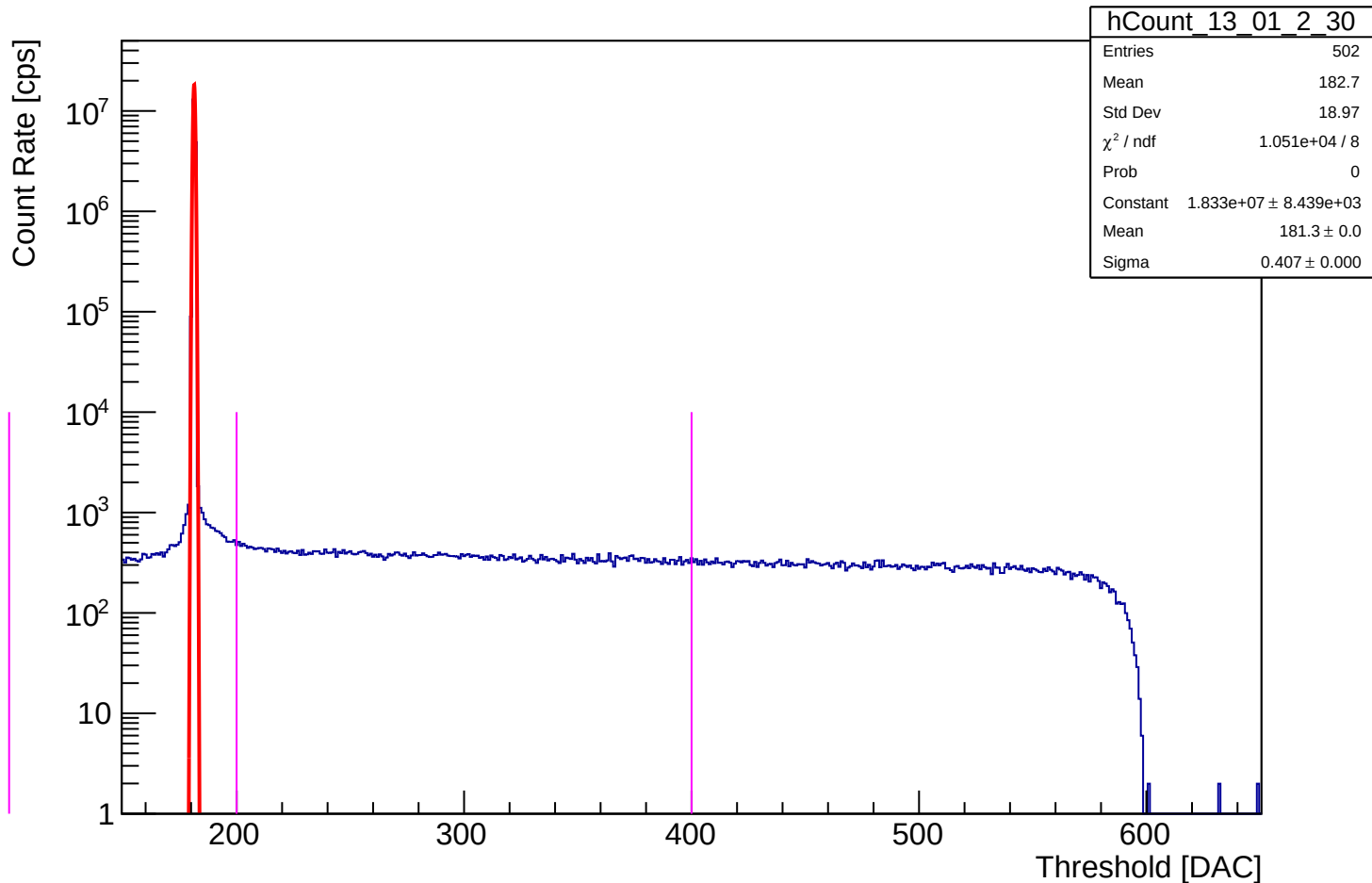
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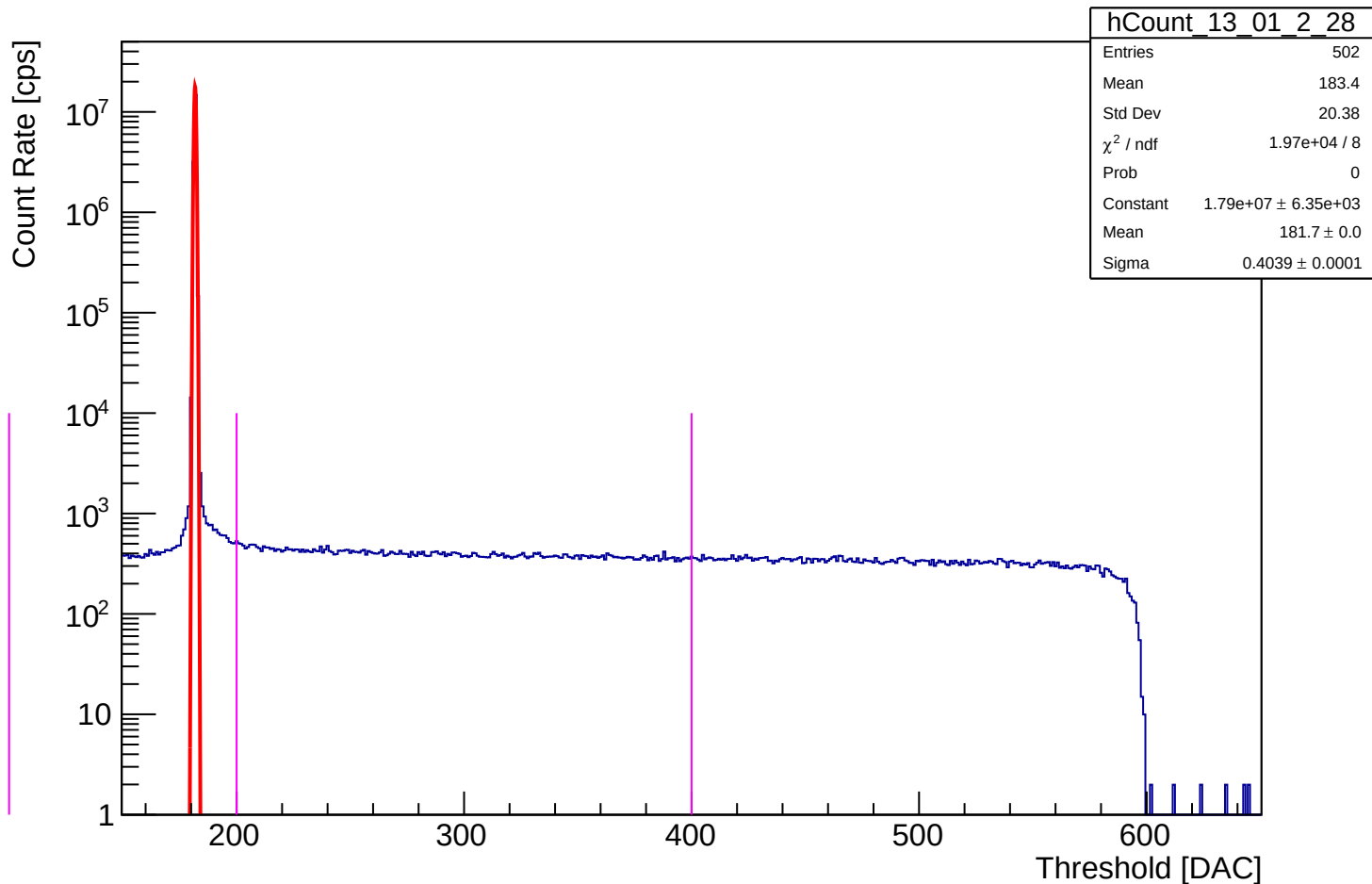
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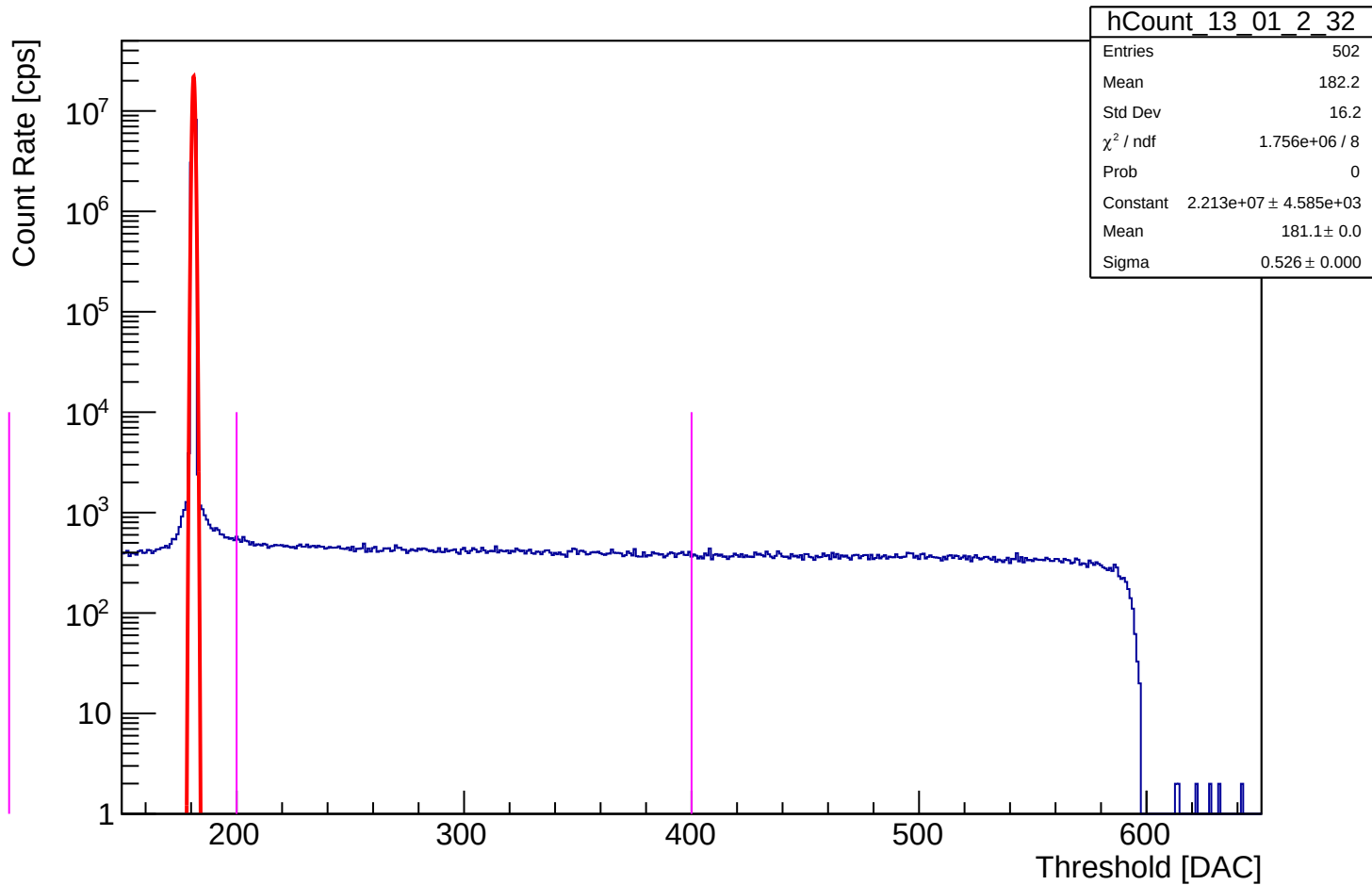
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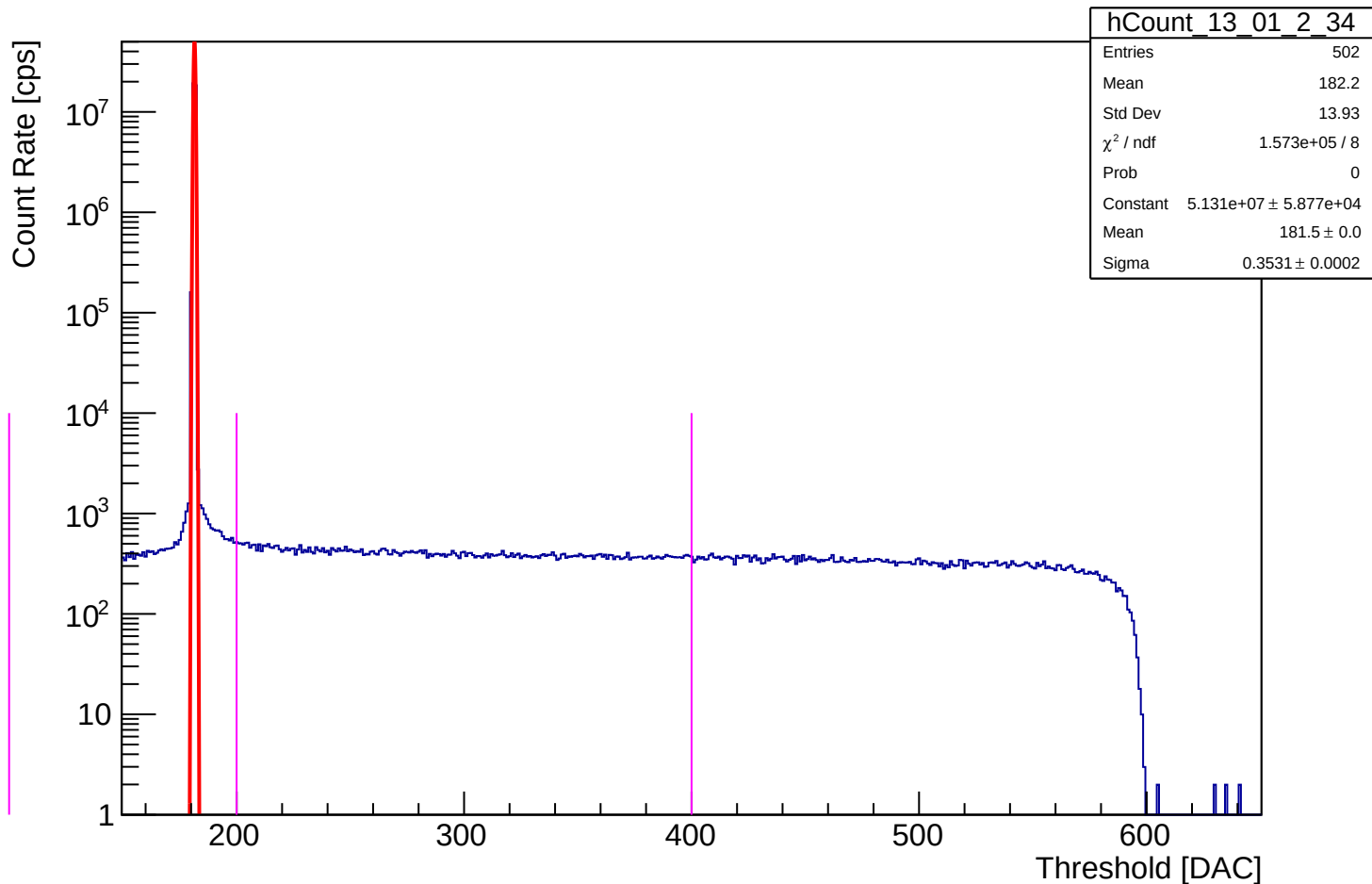
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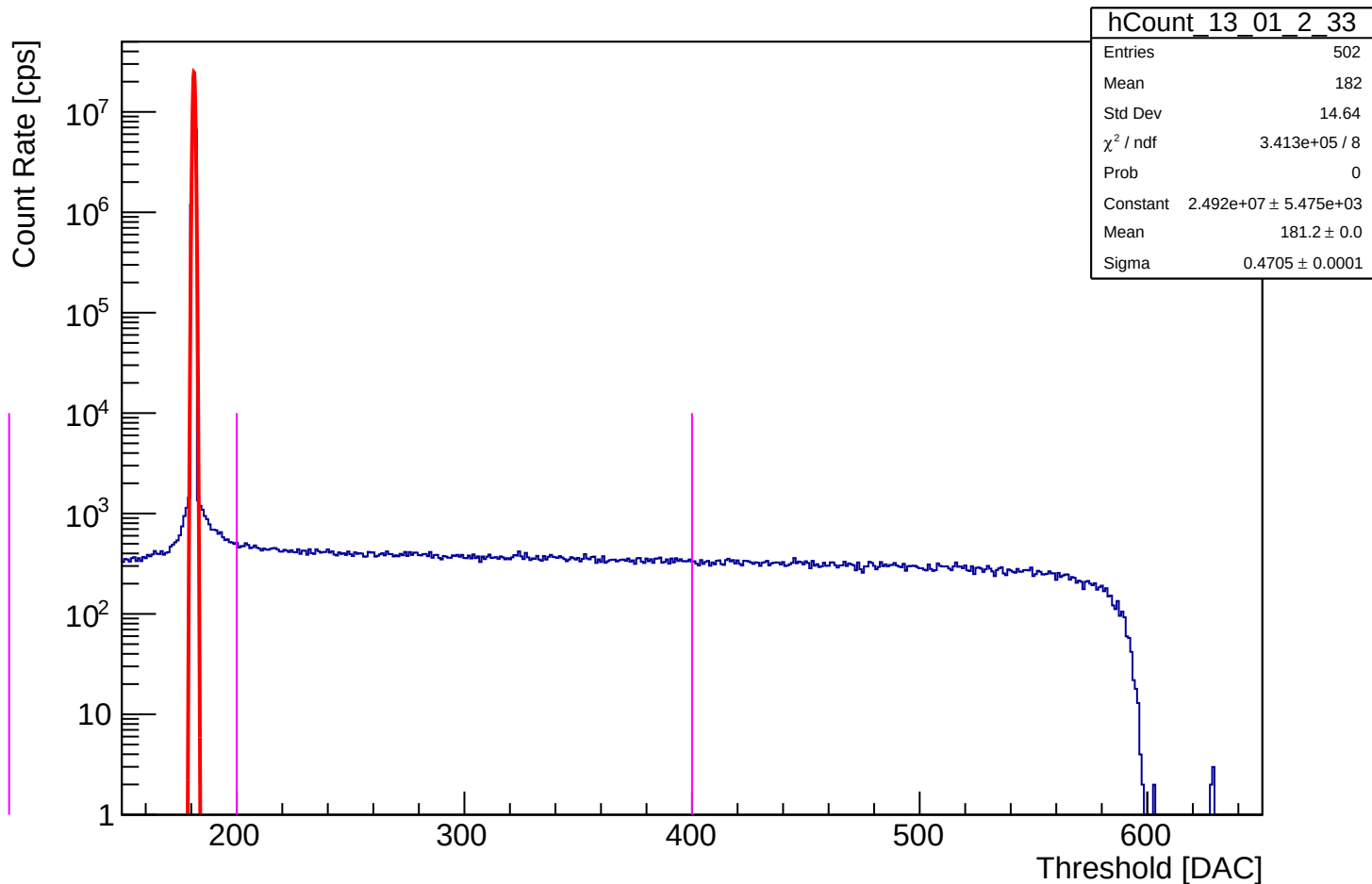
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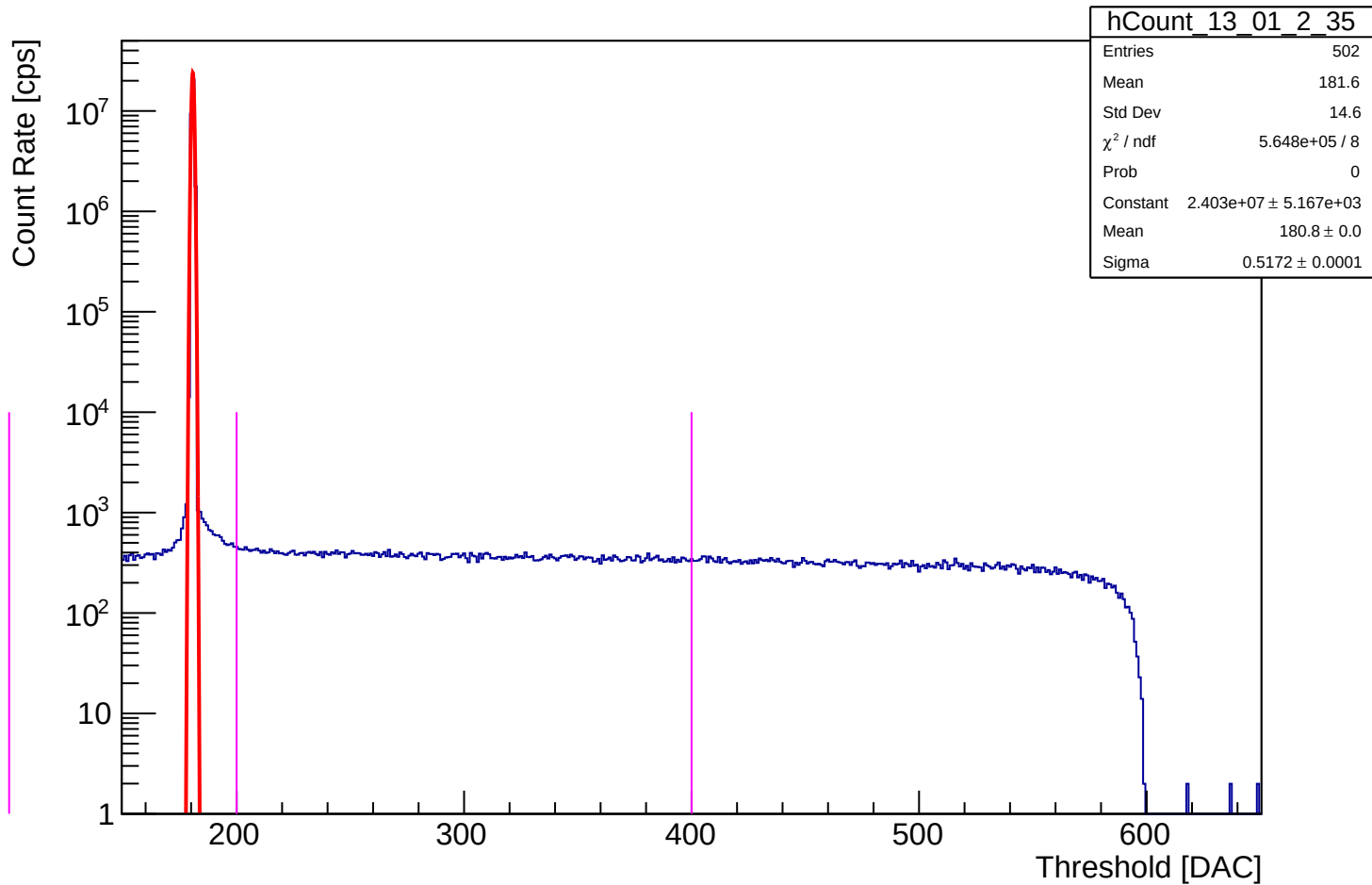
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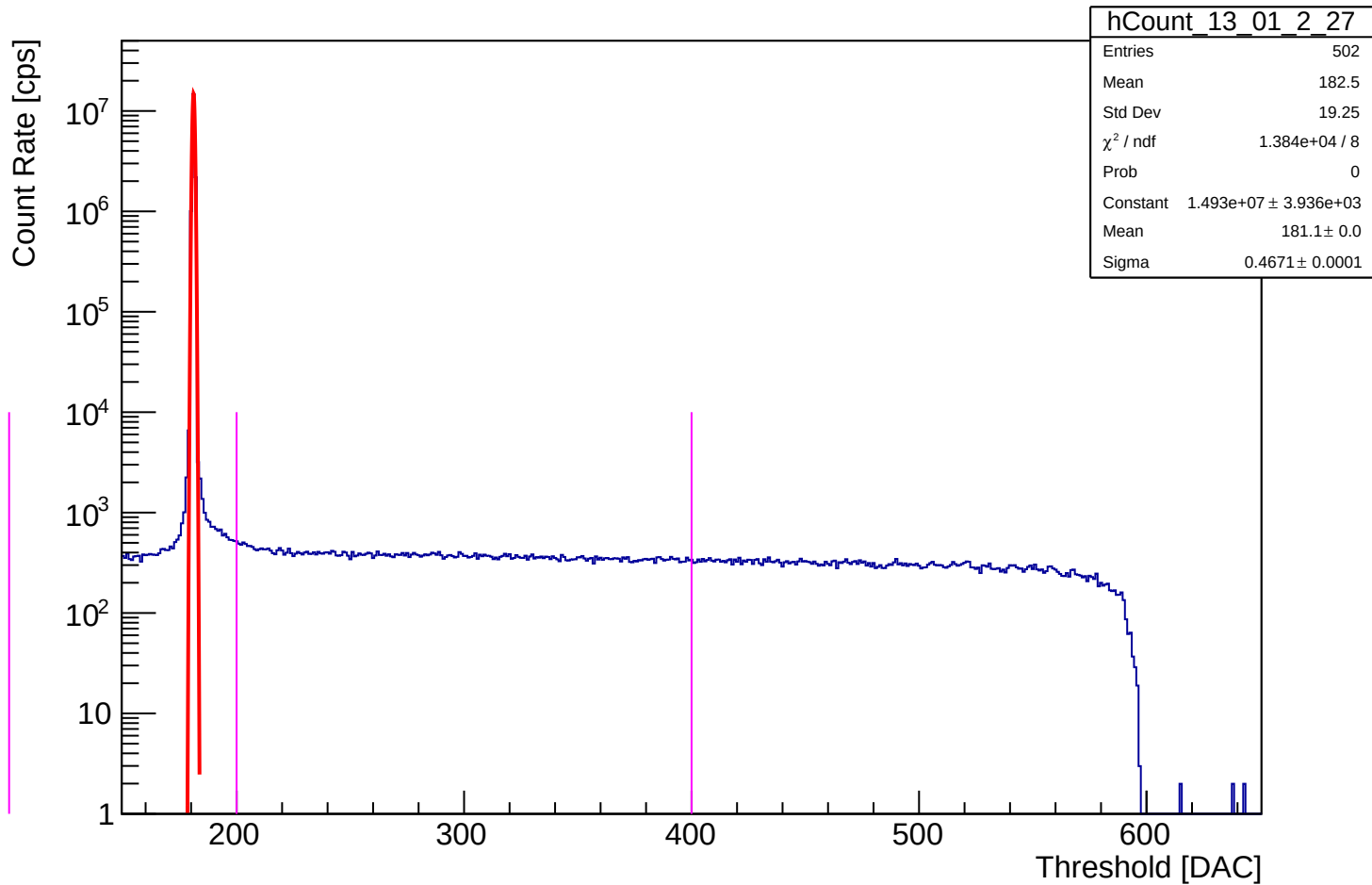
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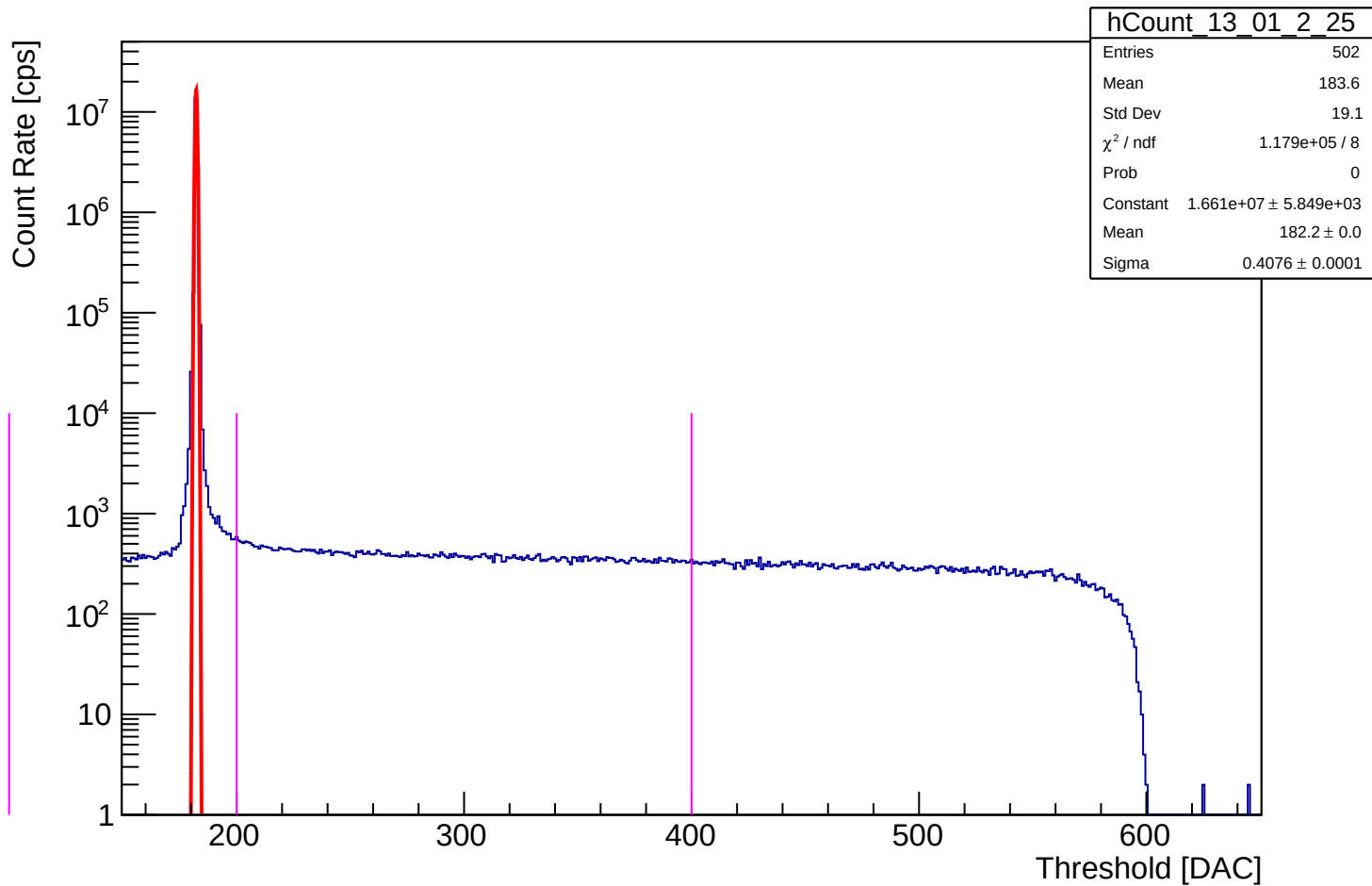
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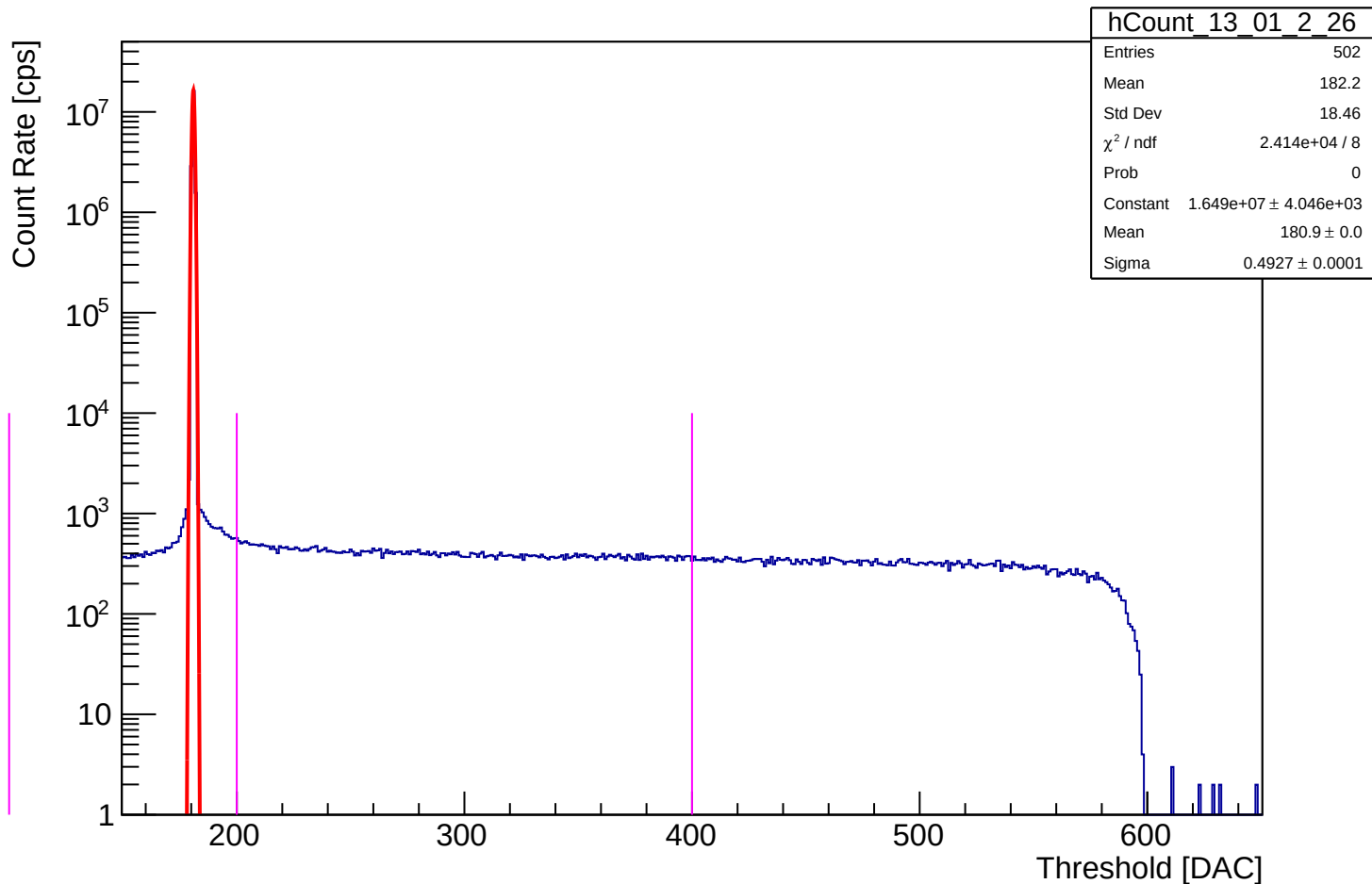
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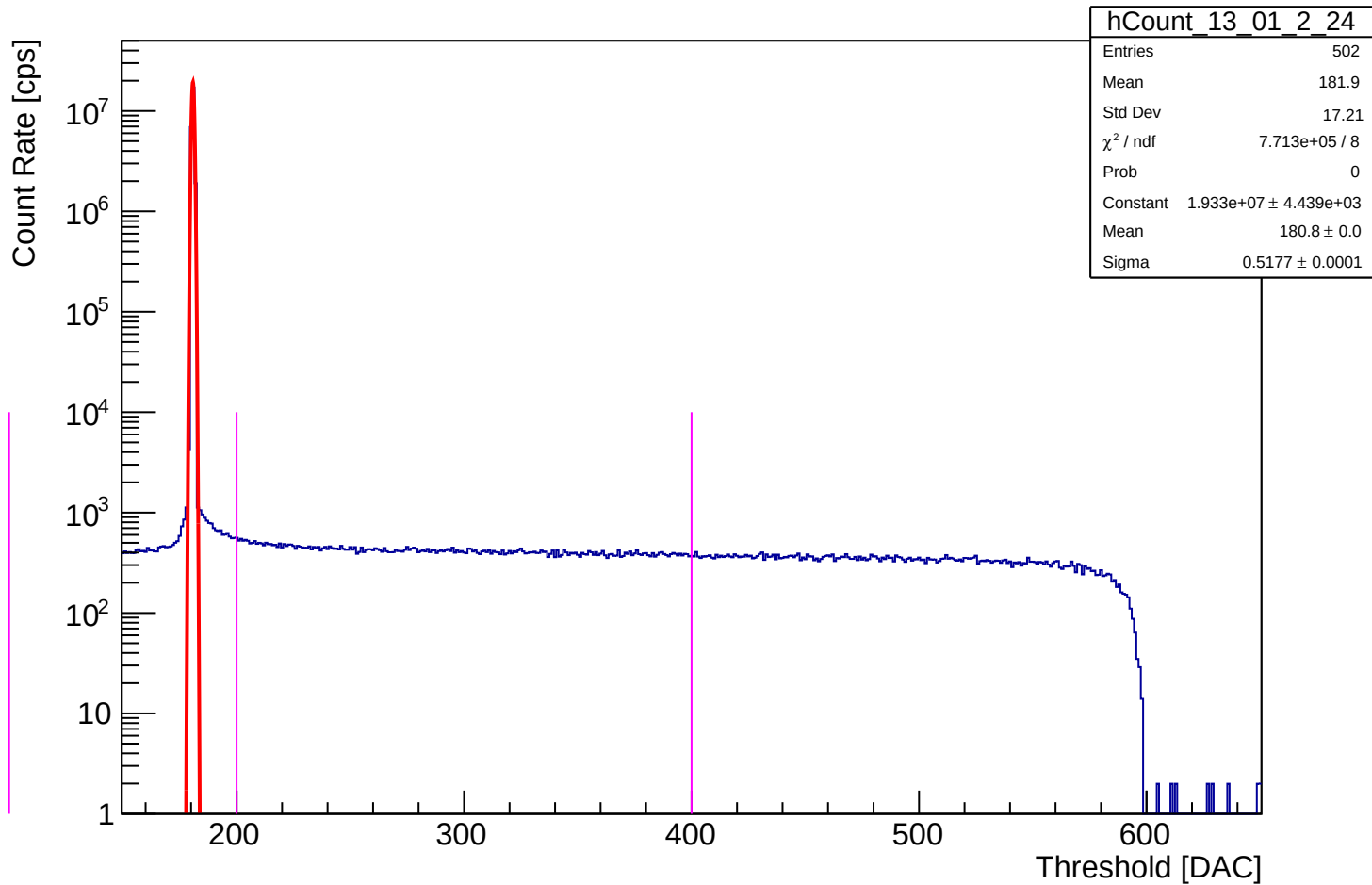
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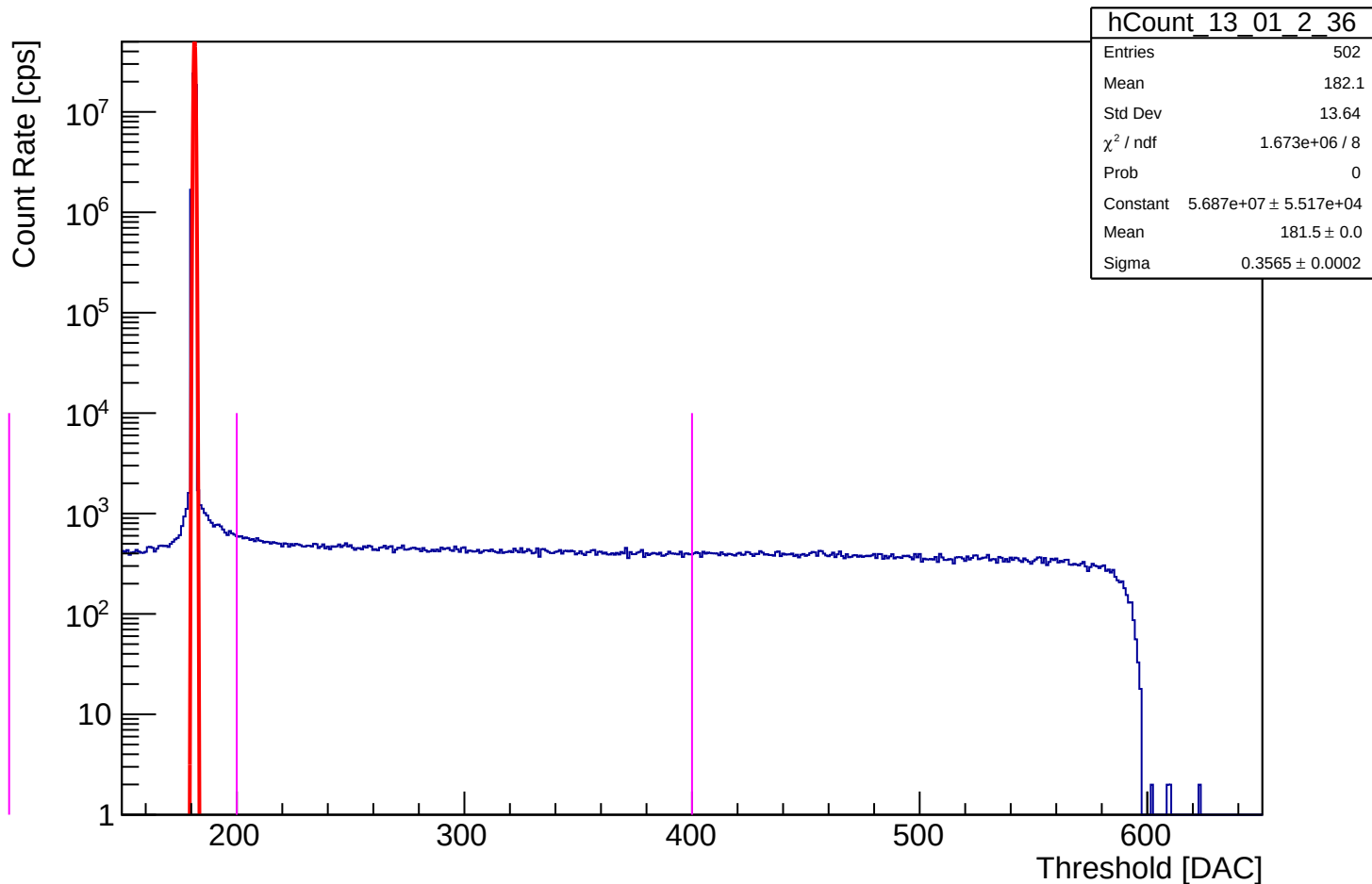
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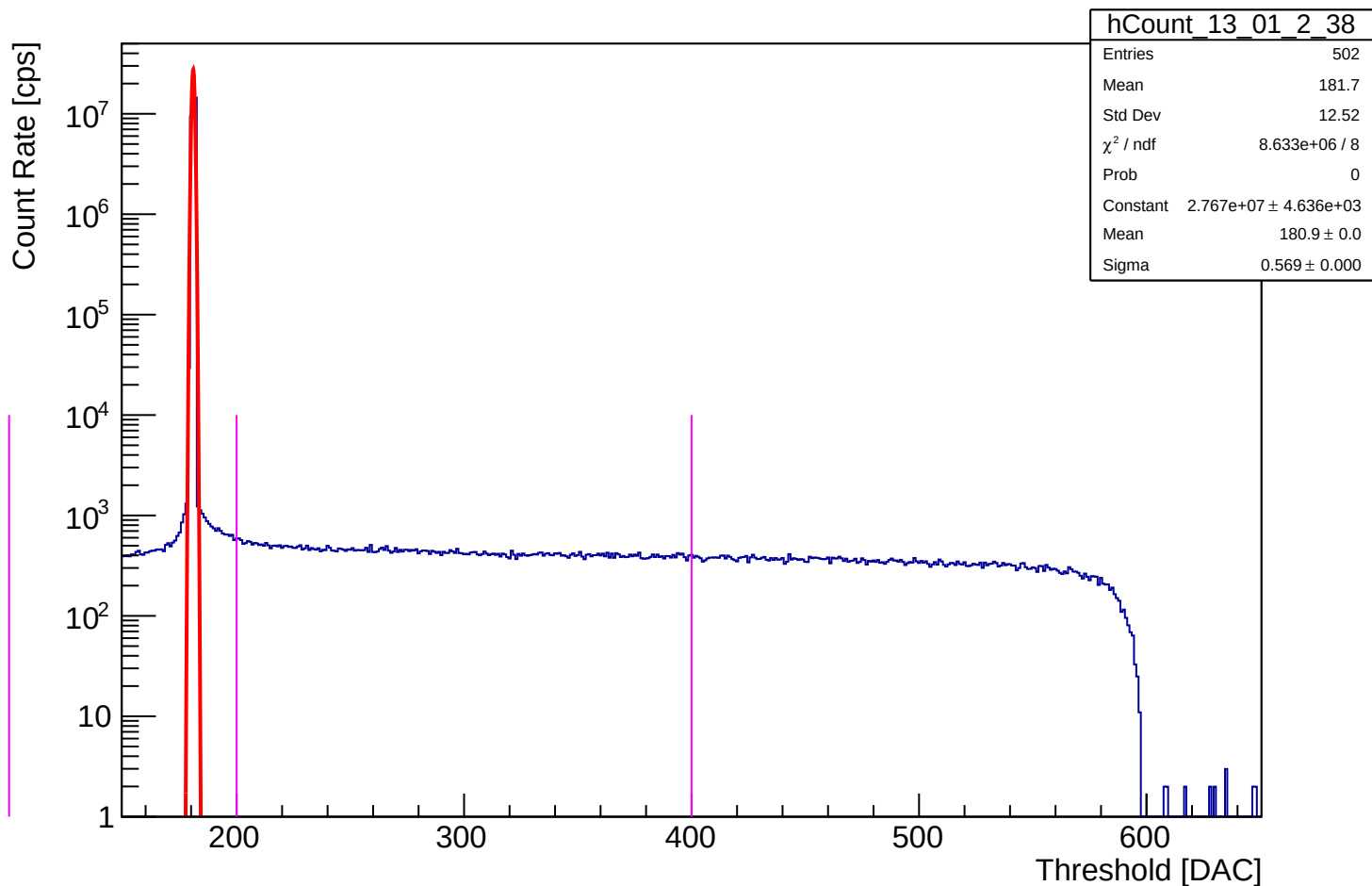
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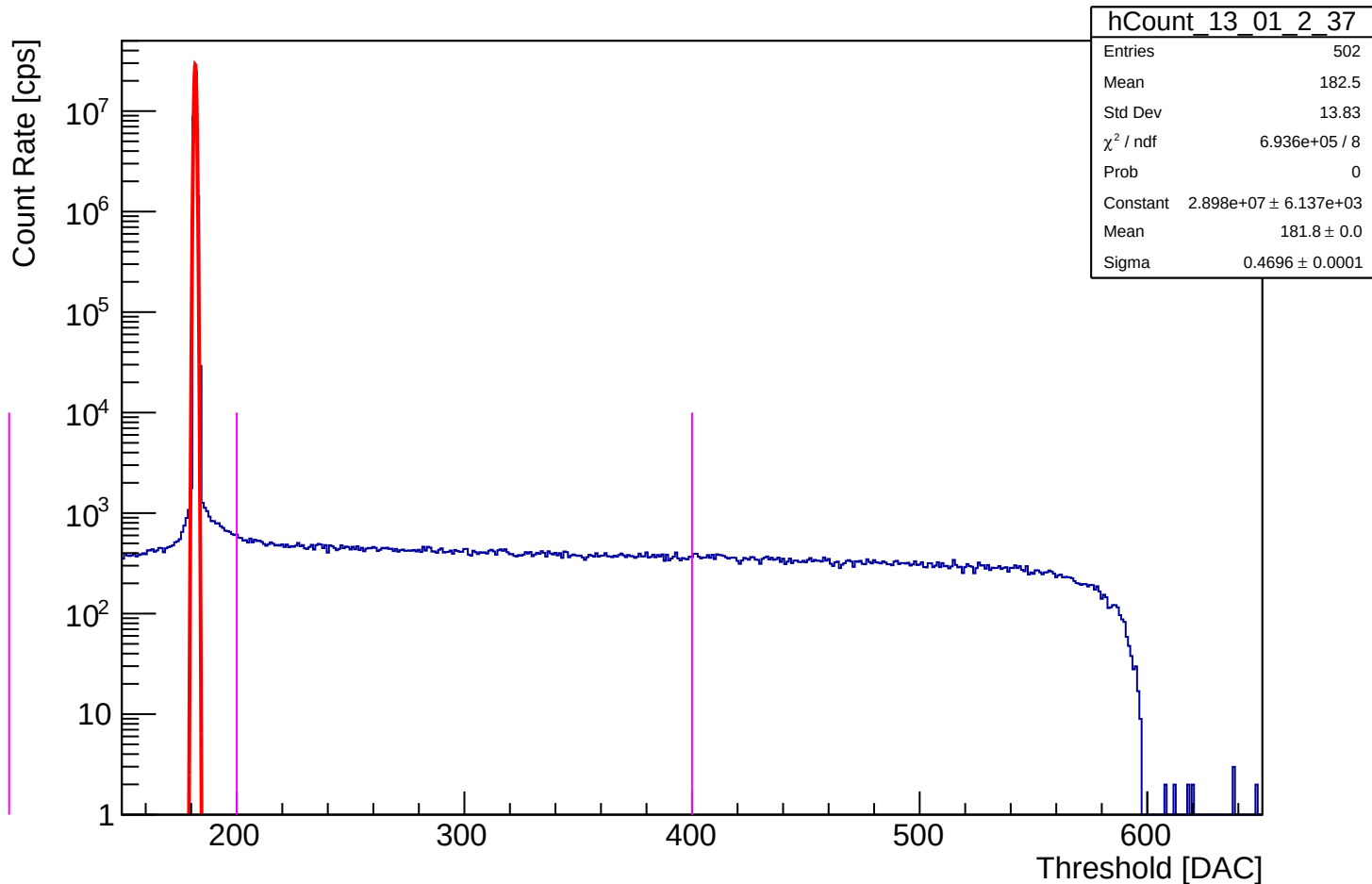
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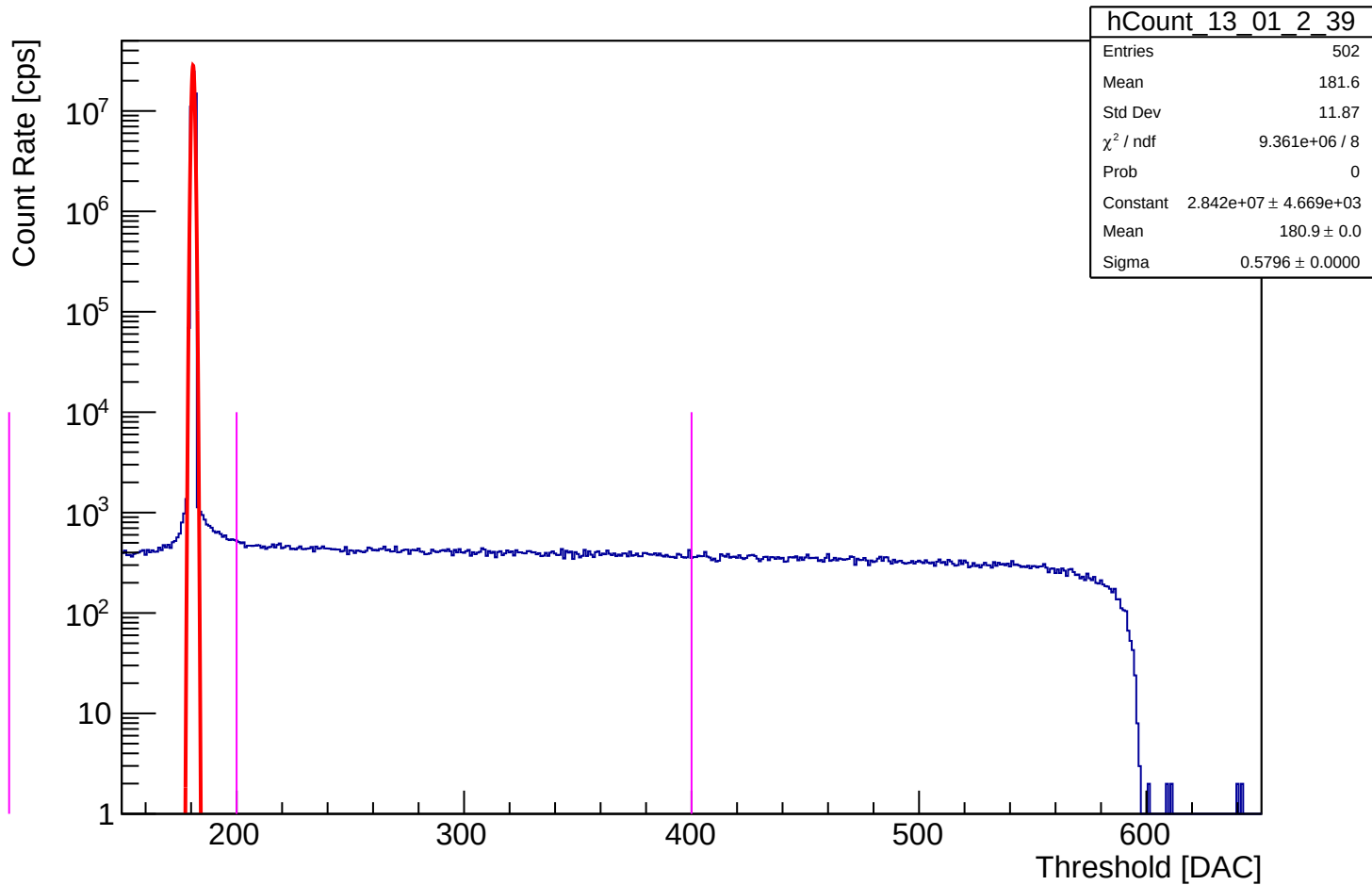
Row 1 Tile 1 Pmt 6 Pixel 14 Slot 13 Fiber 1 Asic 2 Channel 38



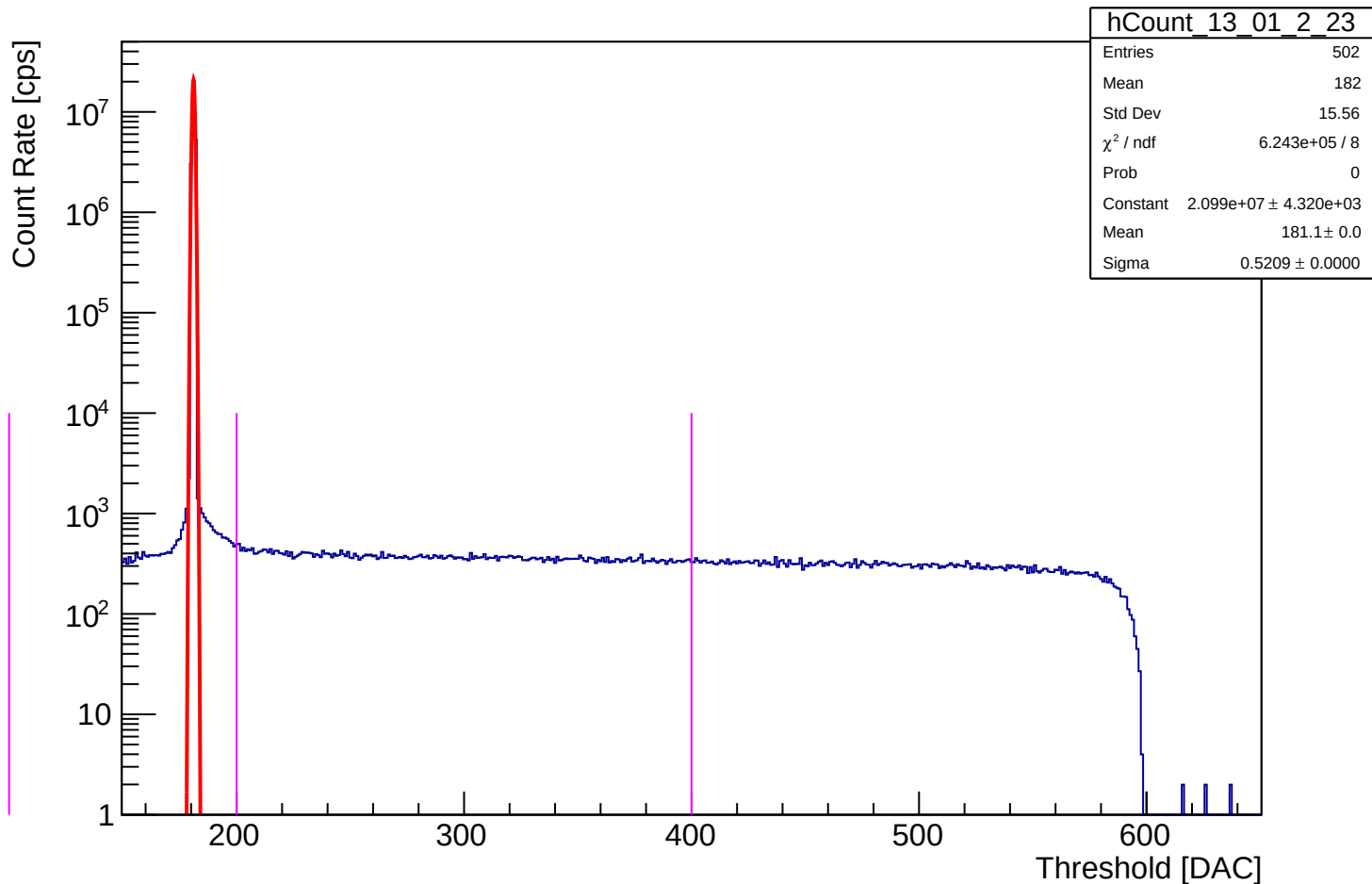
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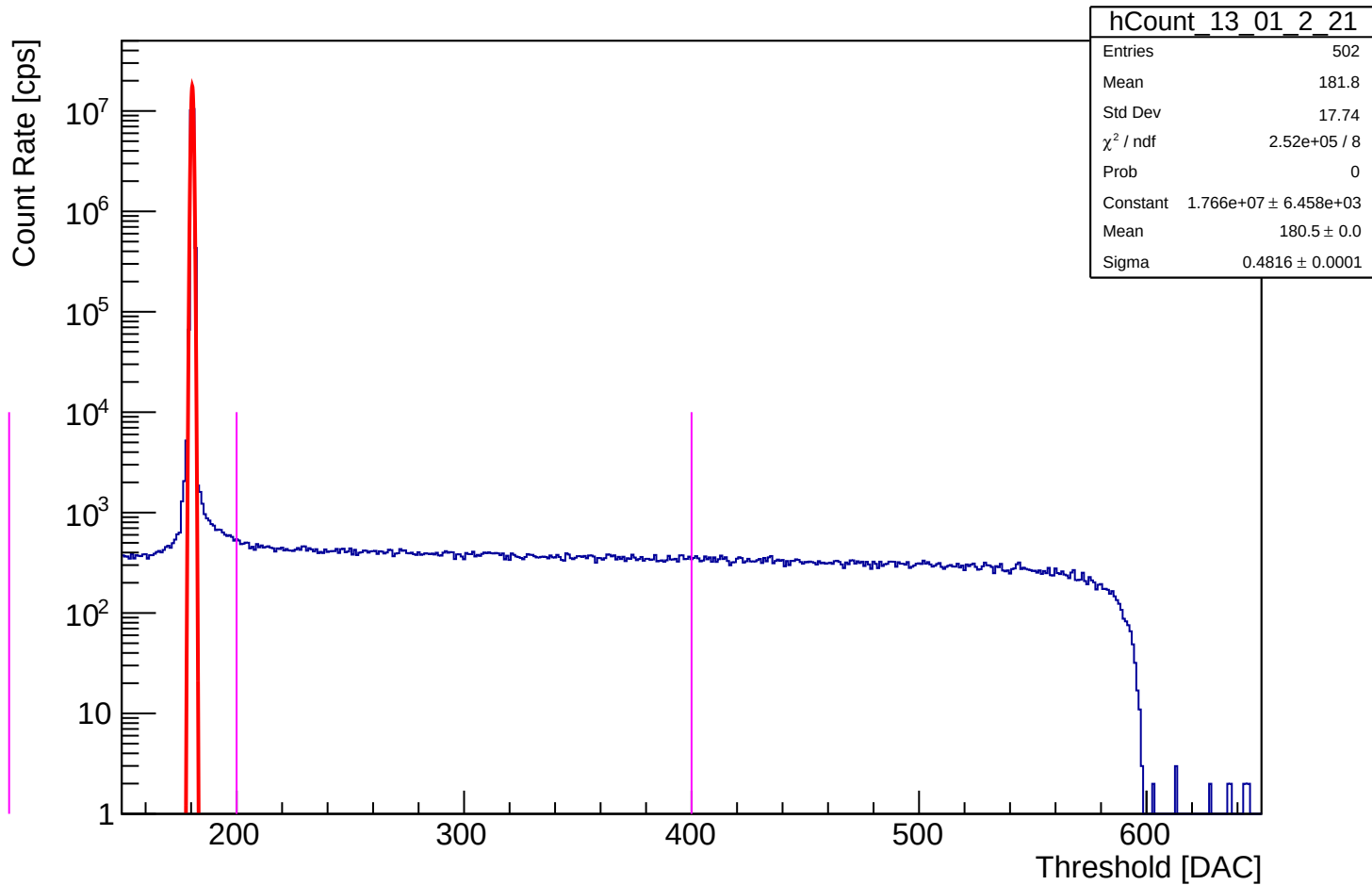
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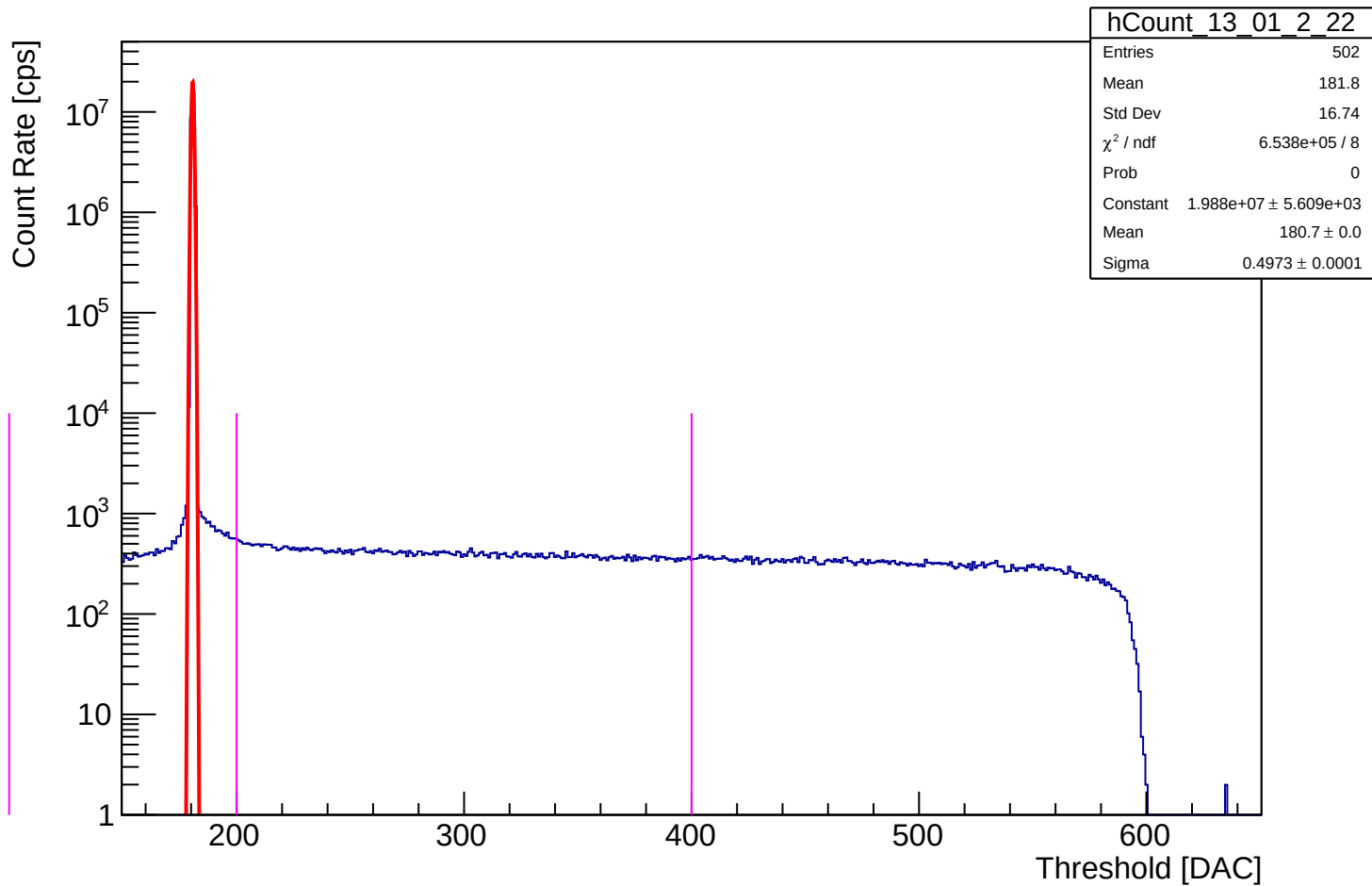
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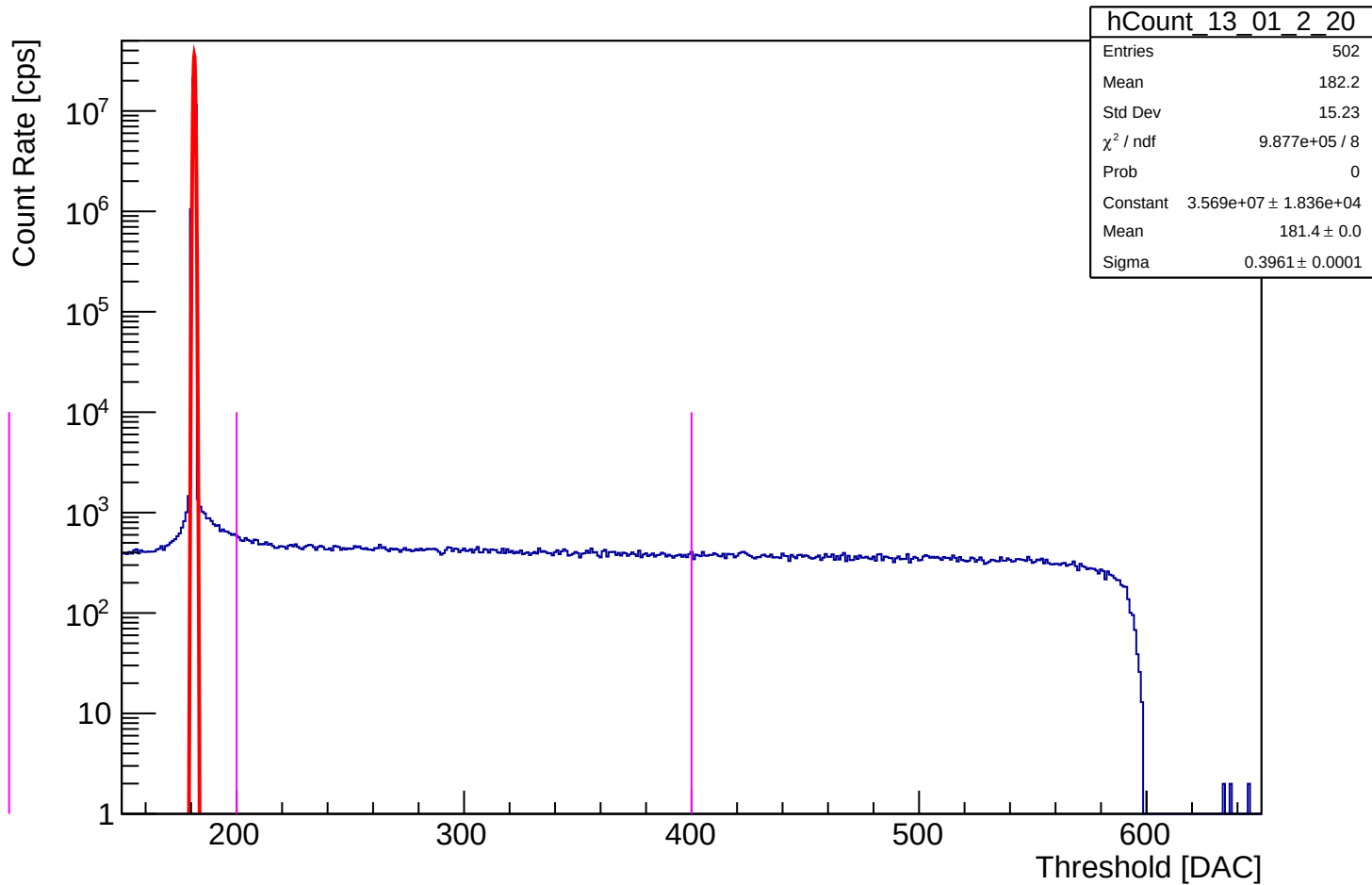
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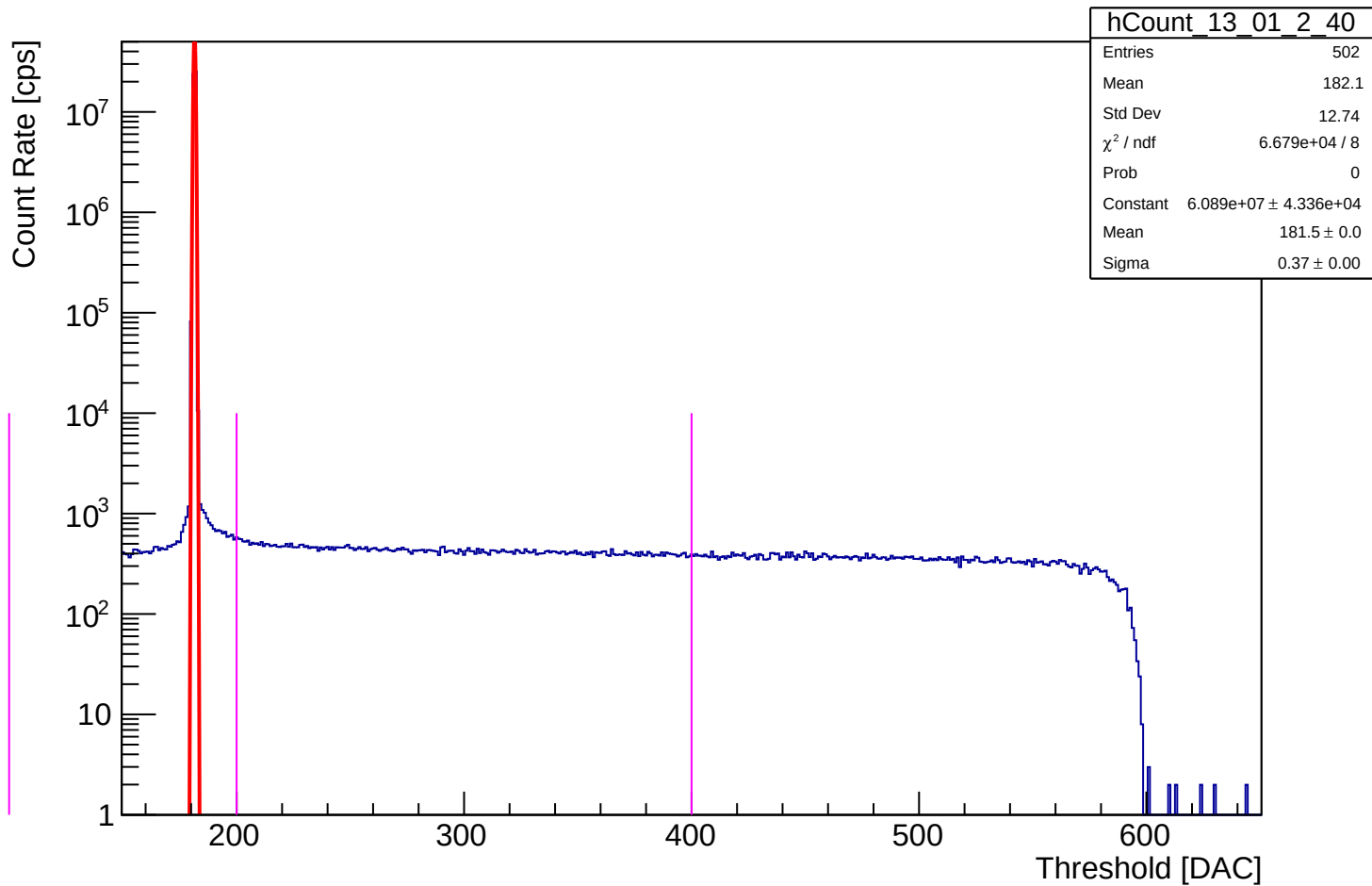
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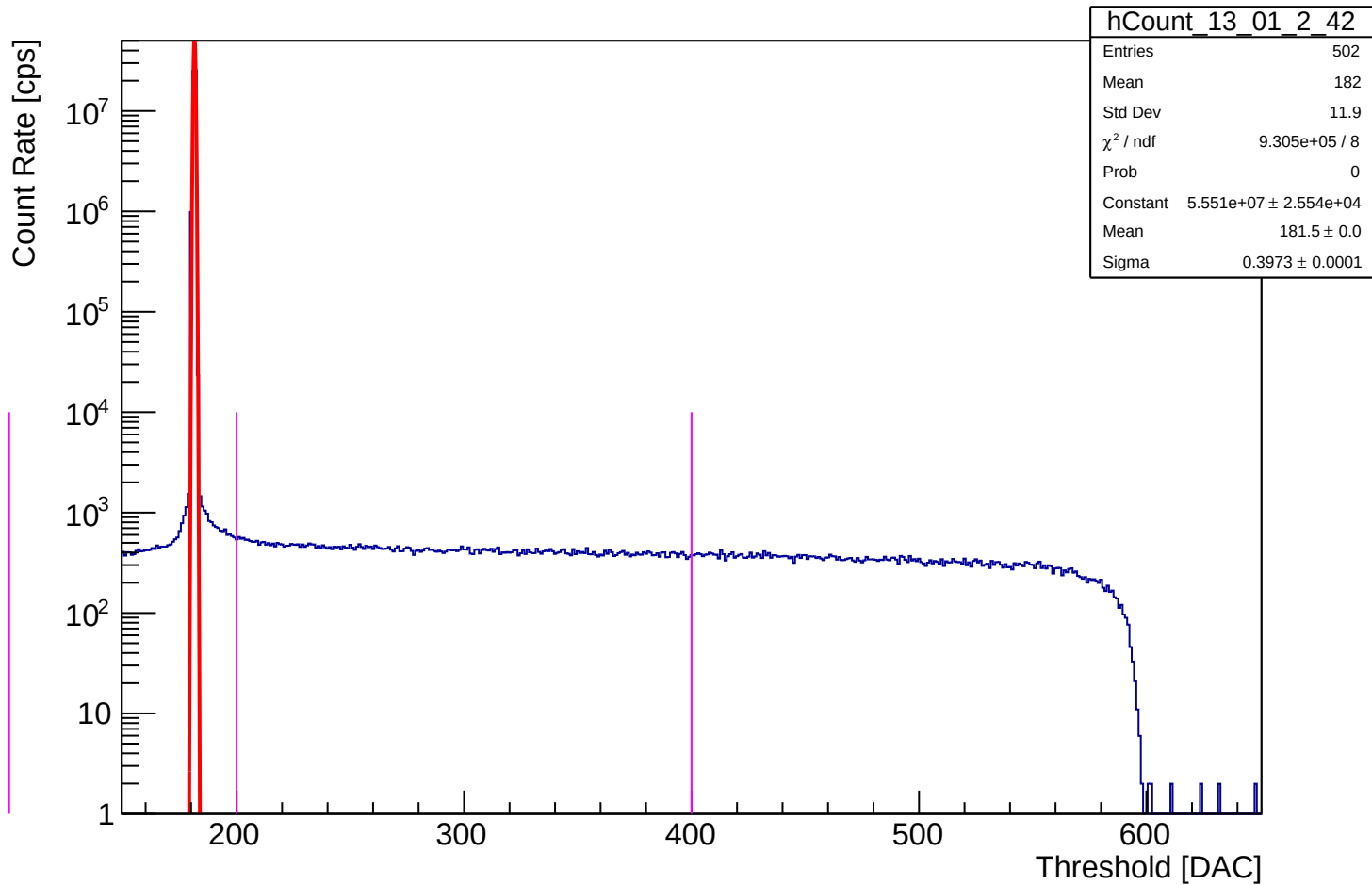
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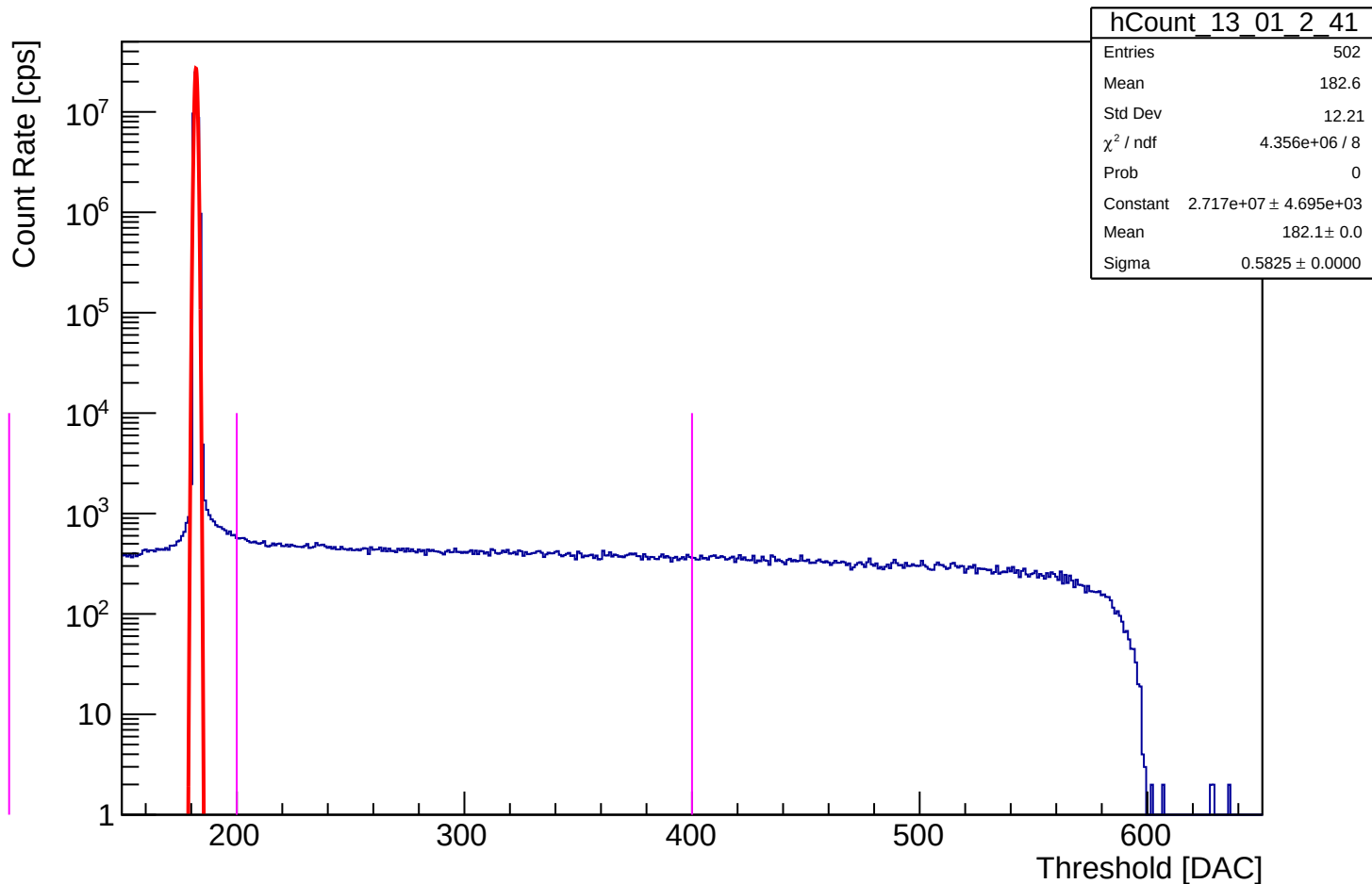


Row 1 Tile 1 Pmt 6 Pixel 21 Slot 13 Fiber 1 Asic 2 Channel 40

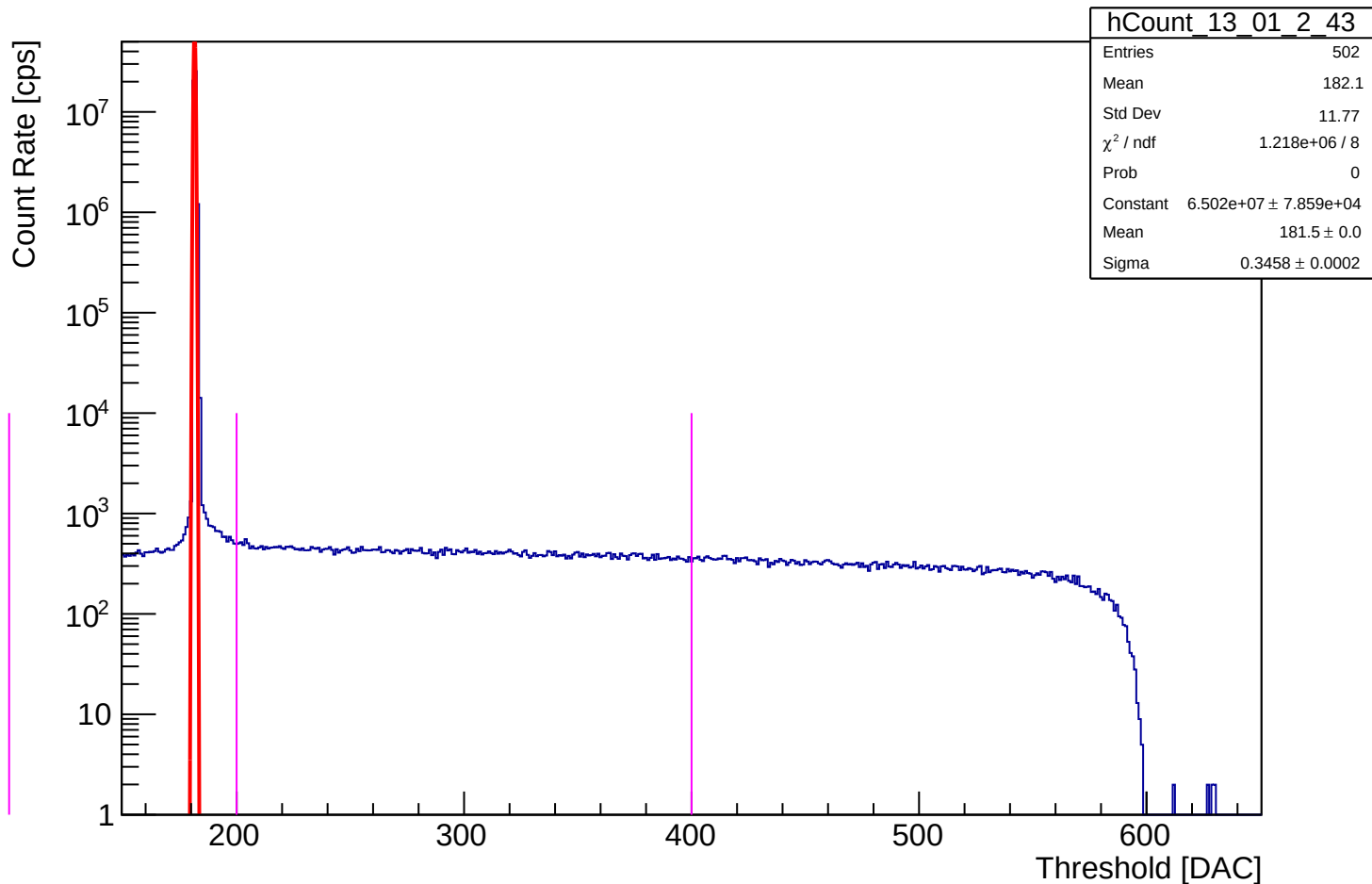


Row 1 Tile 1 Pmt 6 Pixel 22 Slot 13 Fiber 1 Asic 2 Channel 42

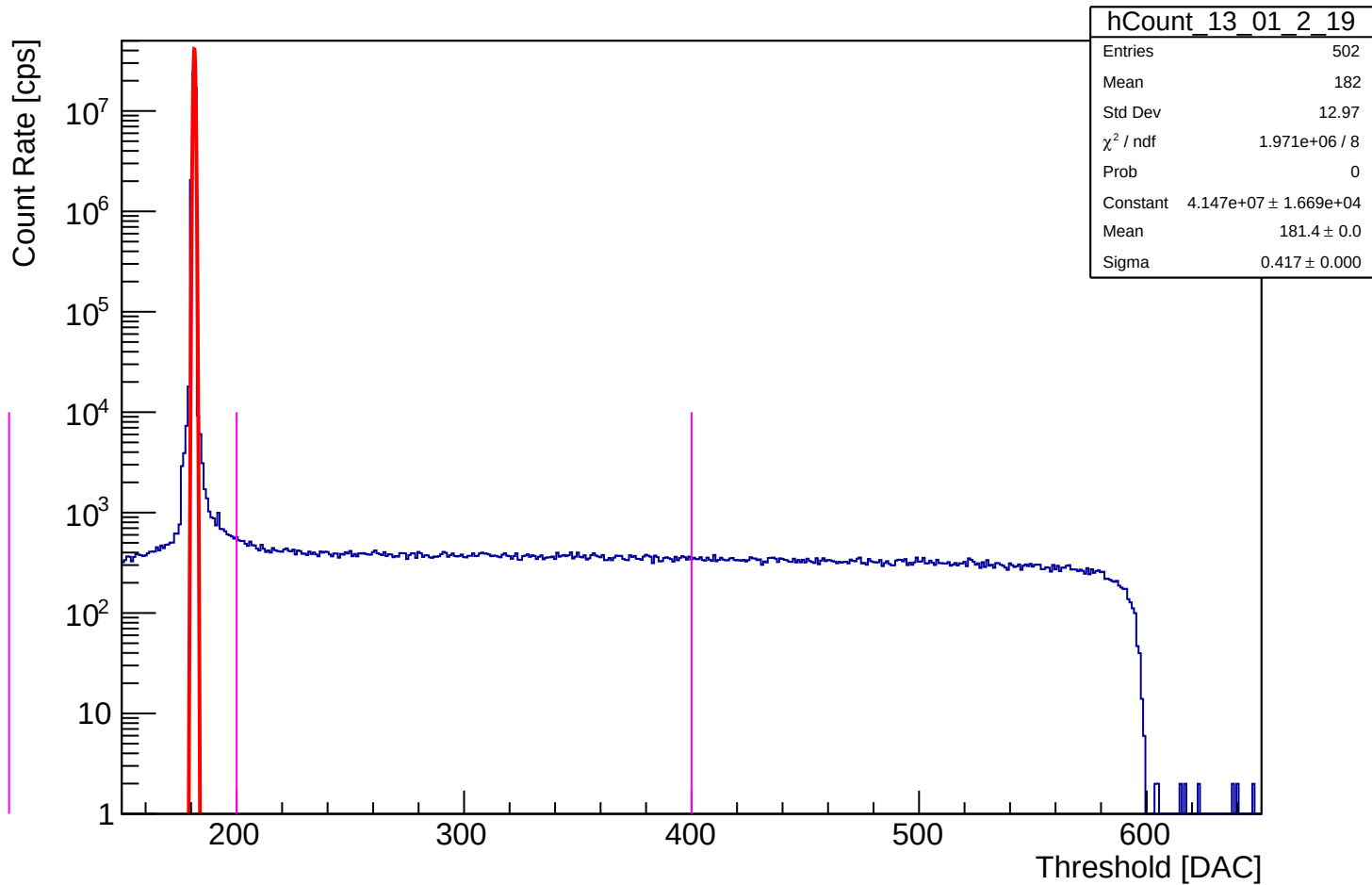




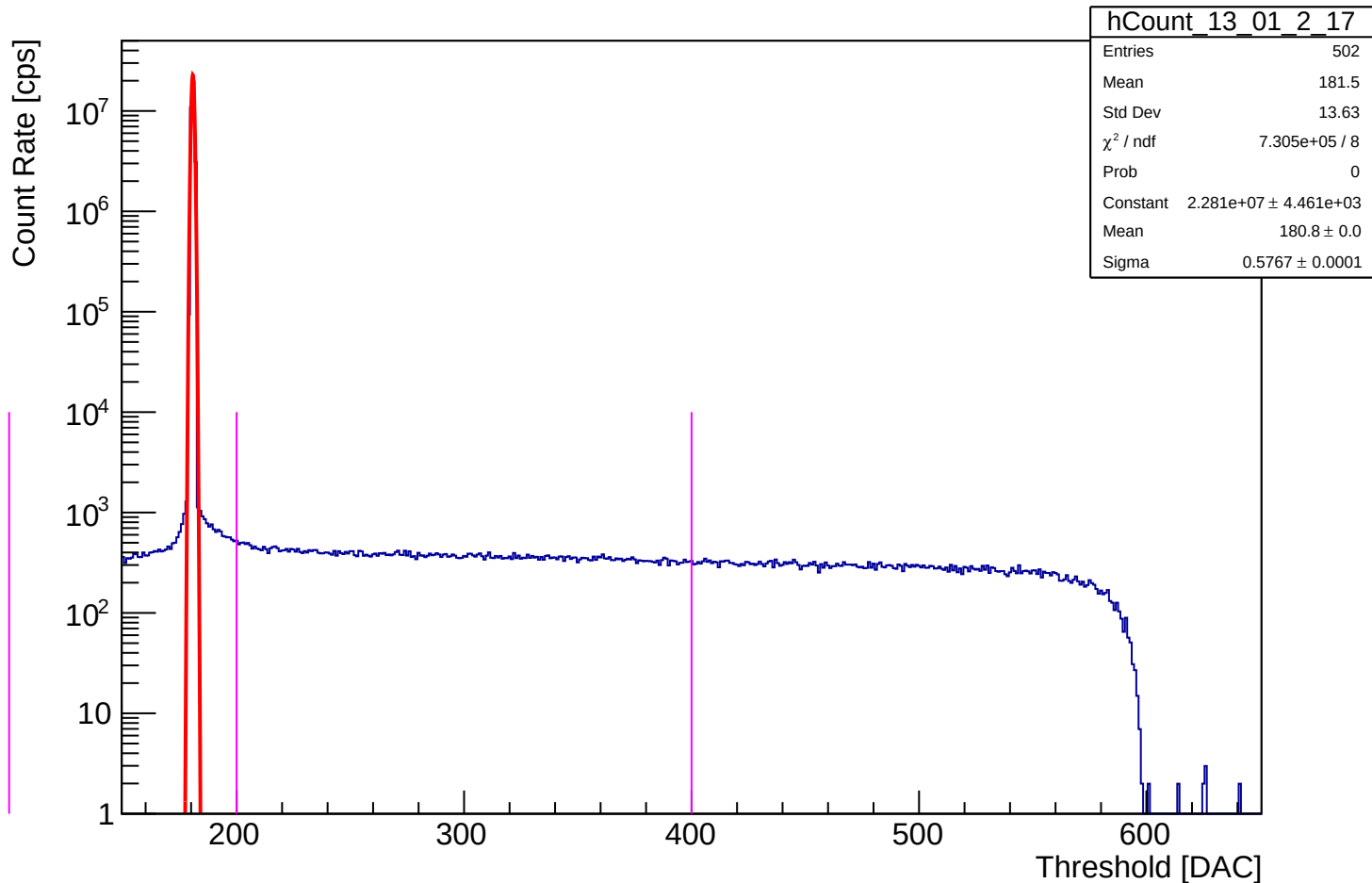
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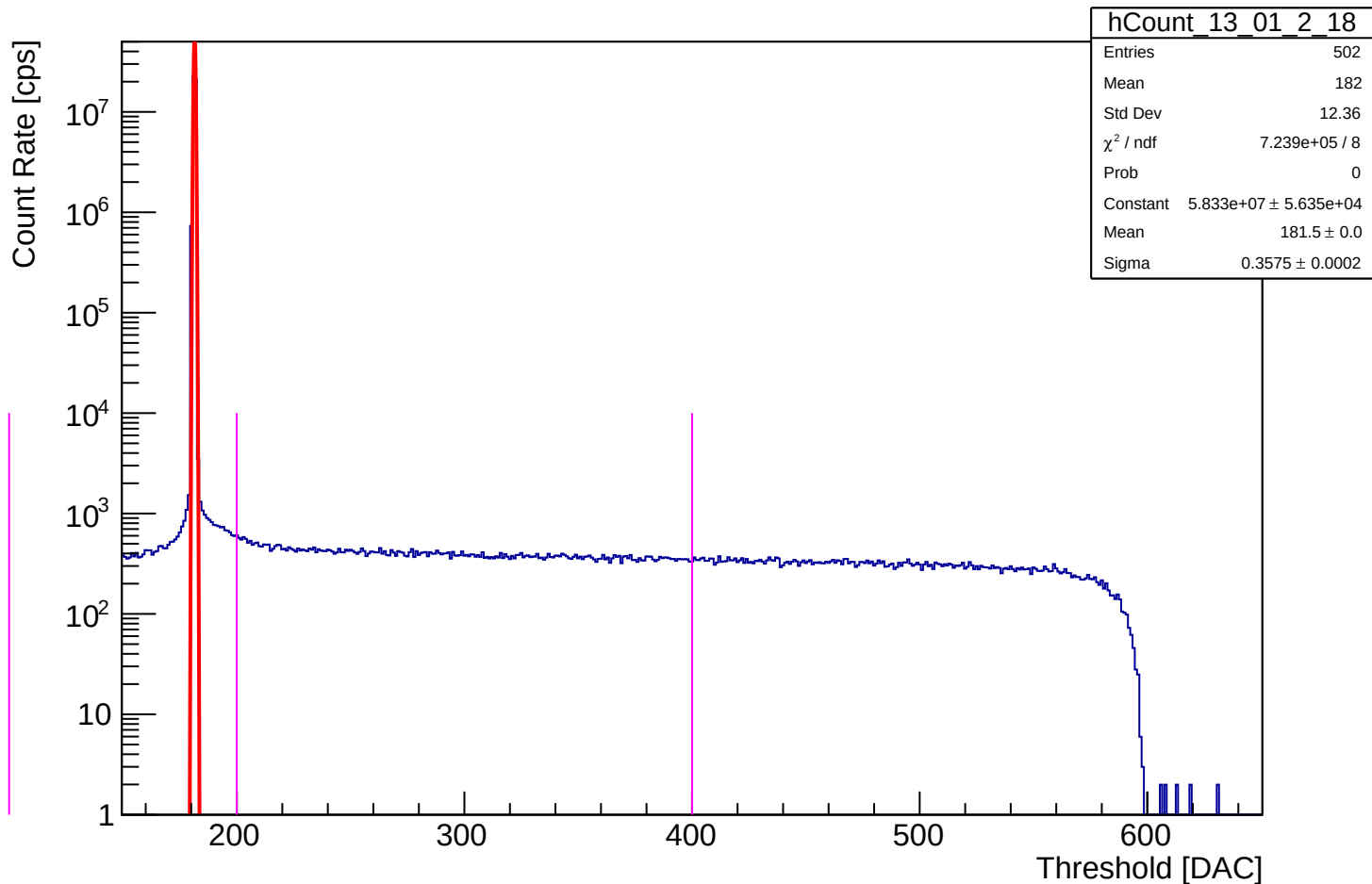
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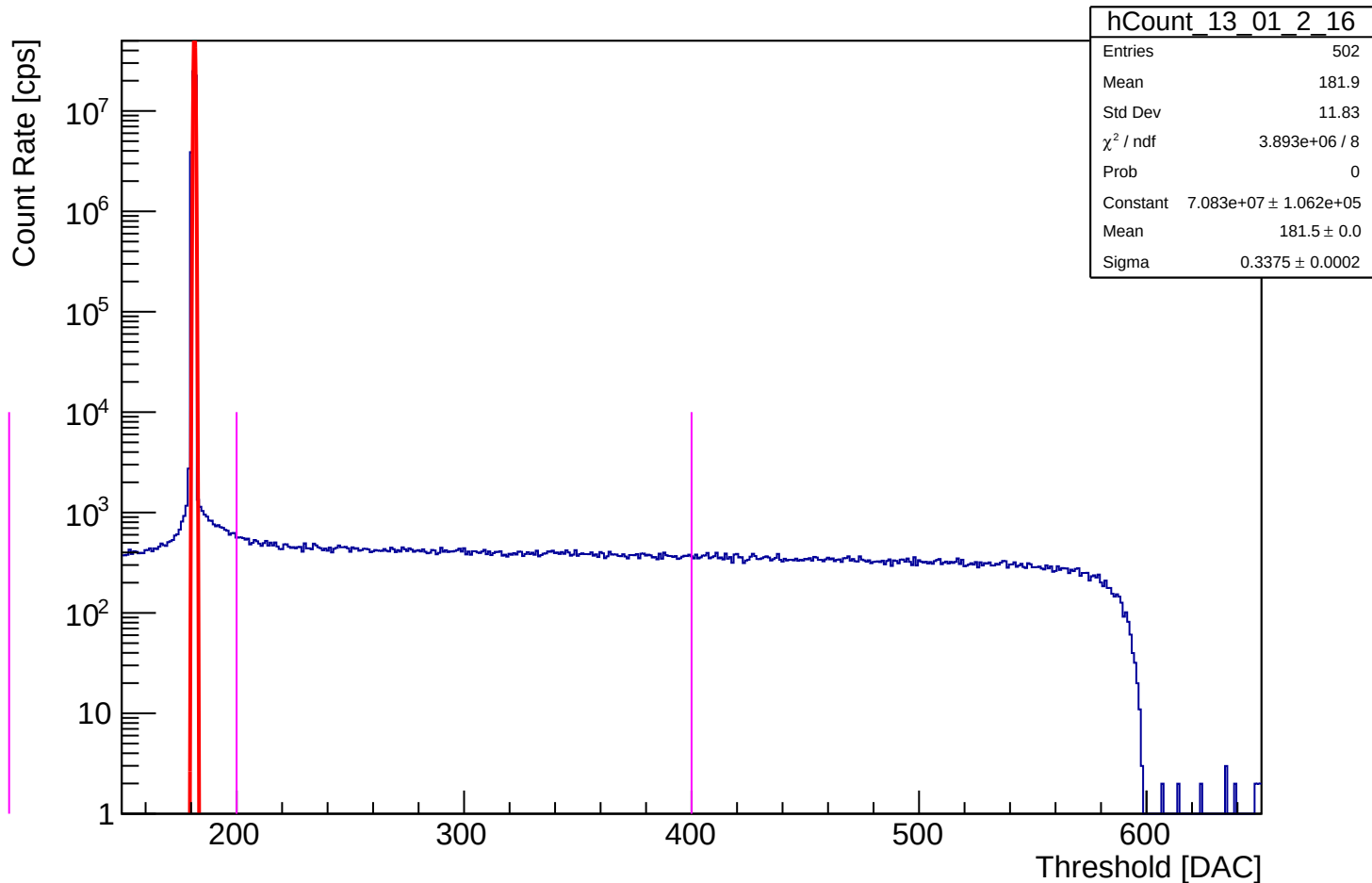
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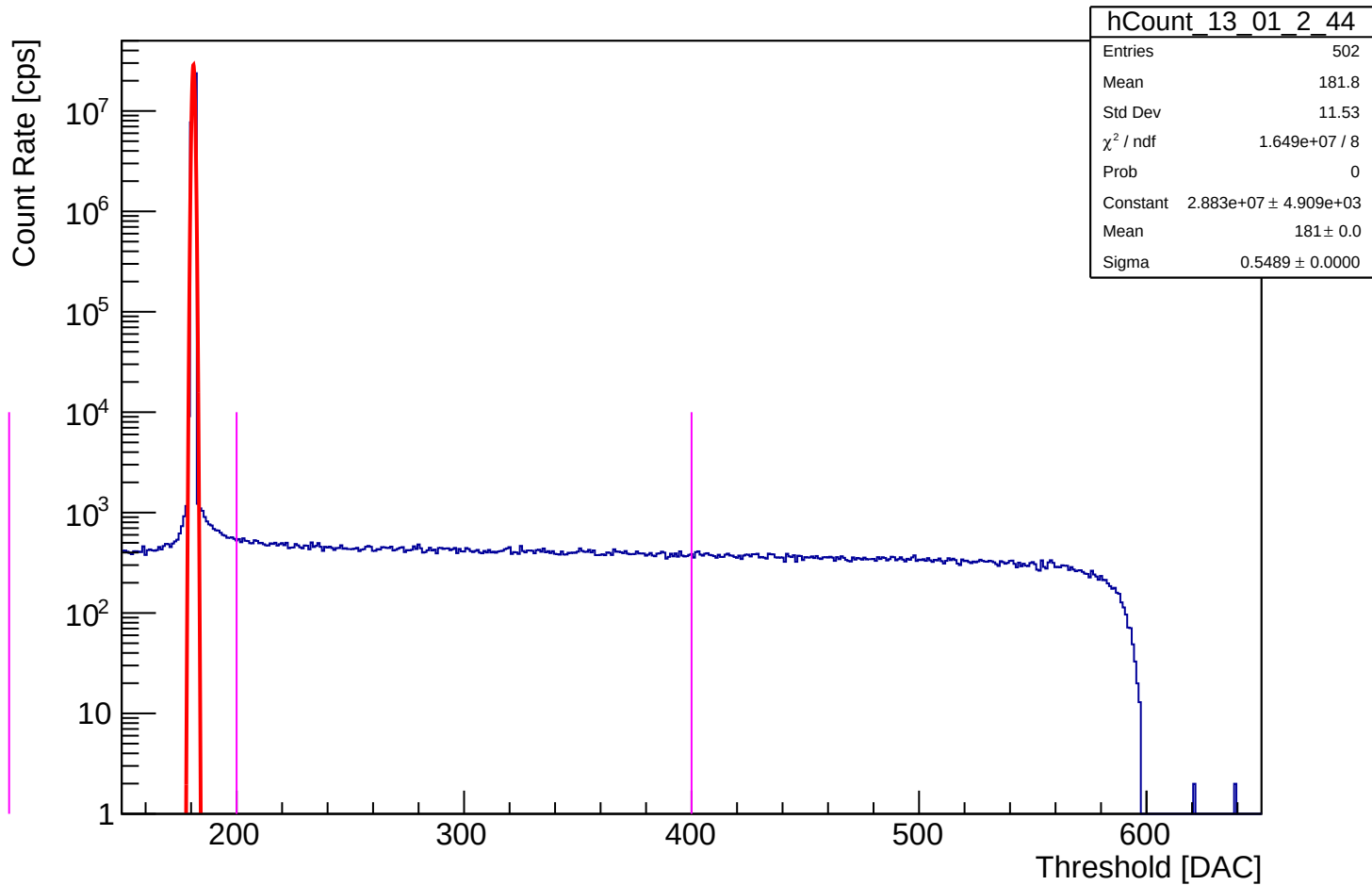
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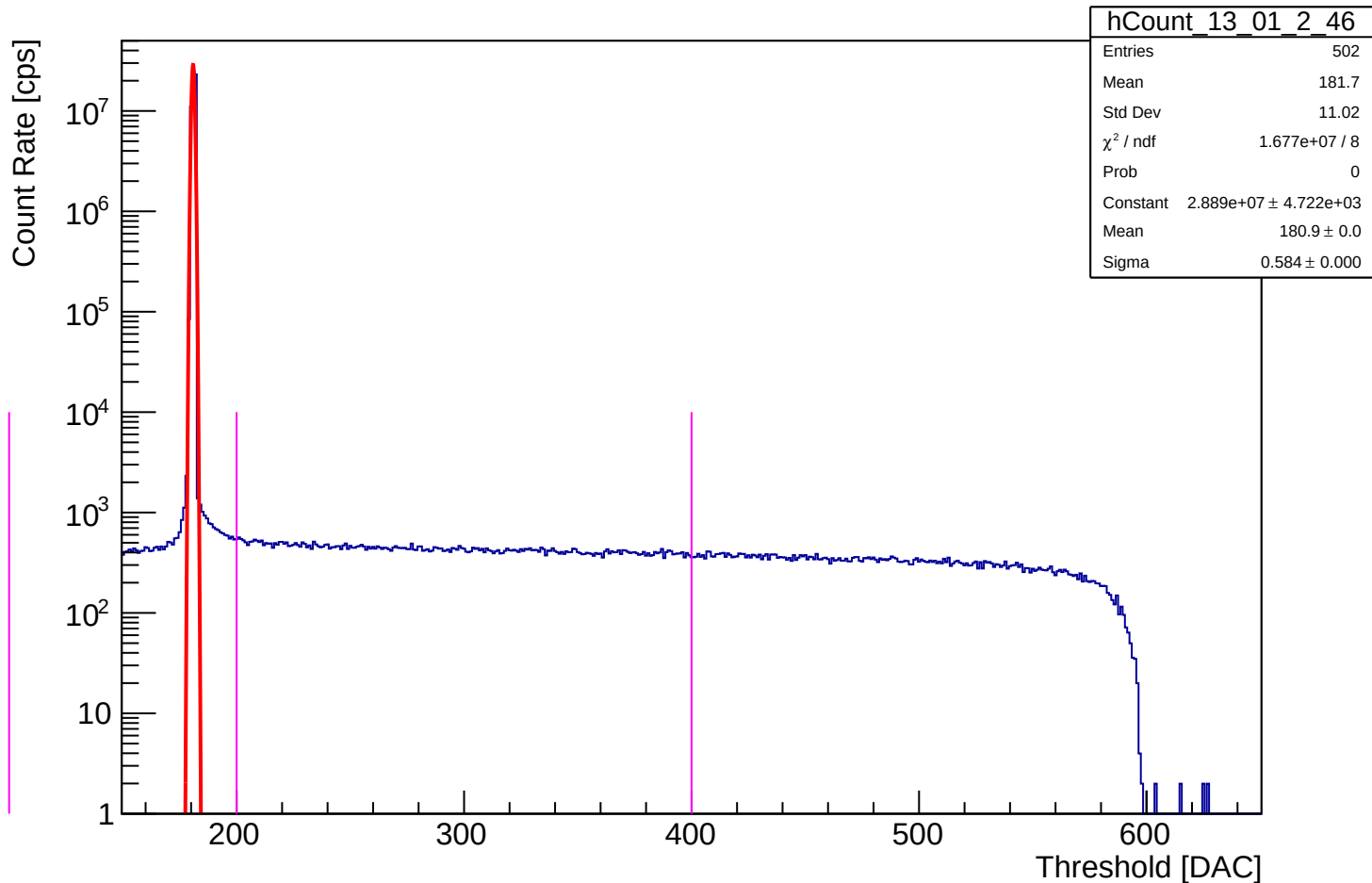
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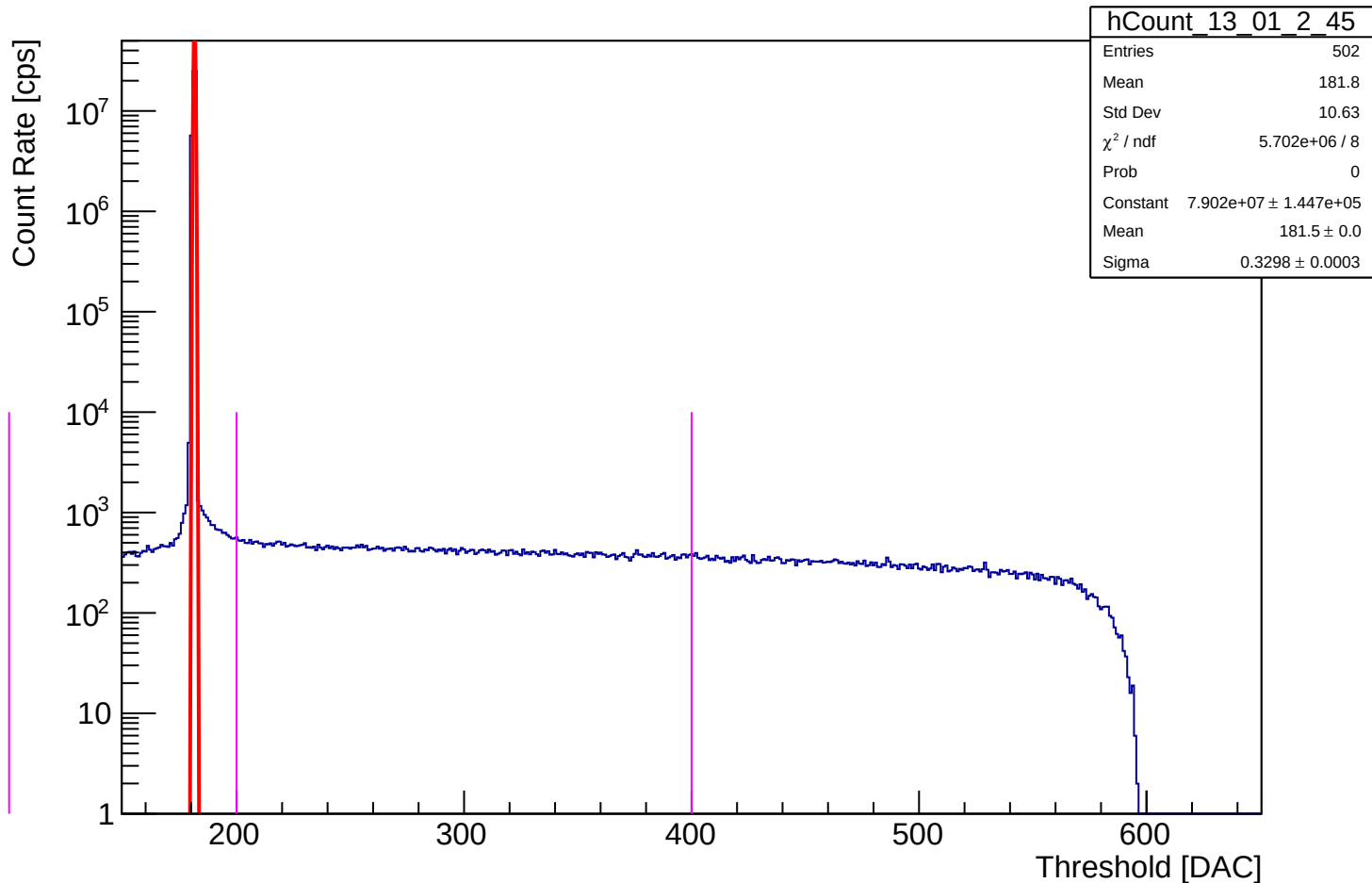
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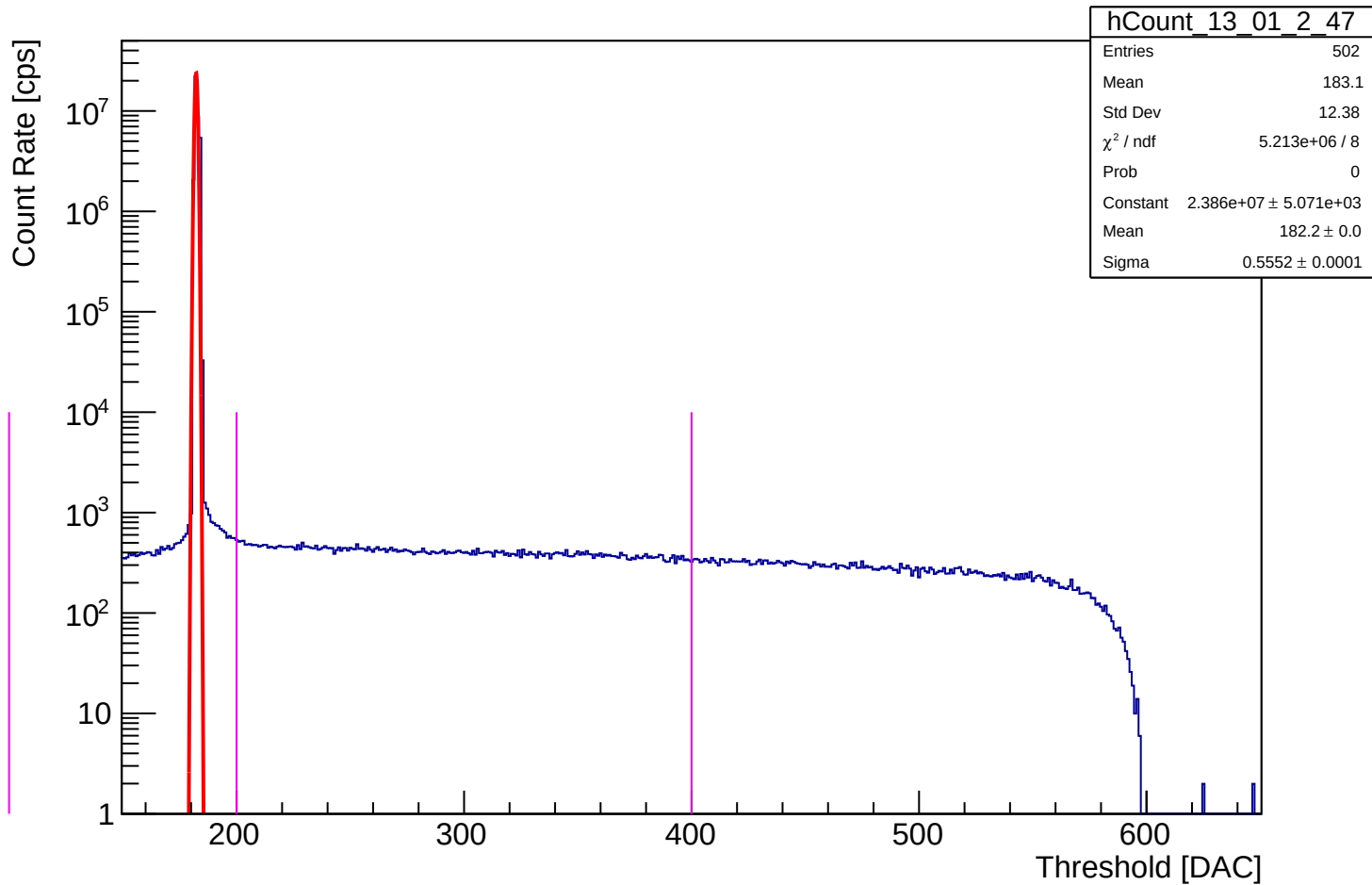
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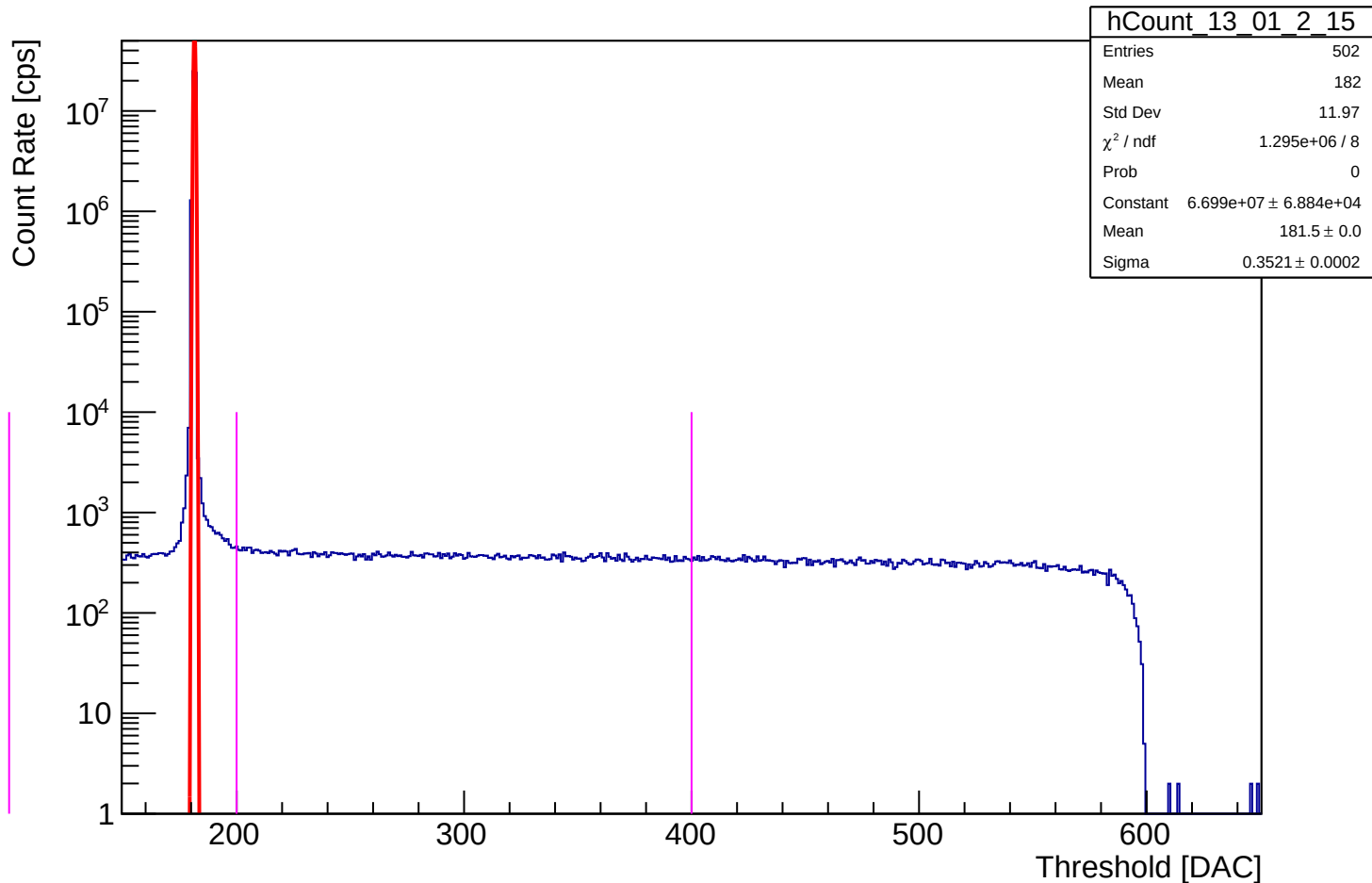
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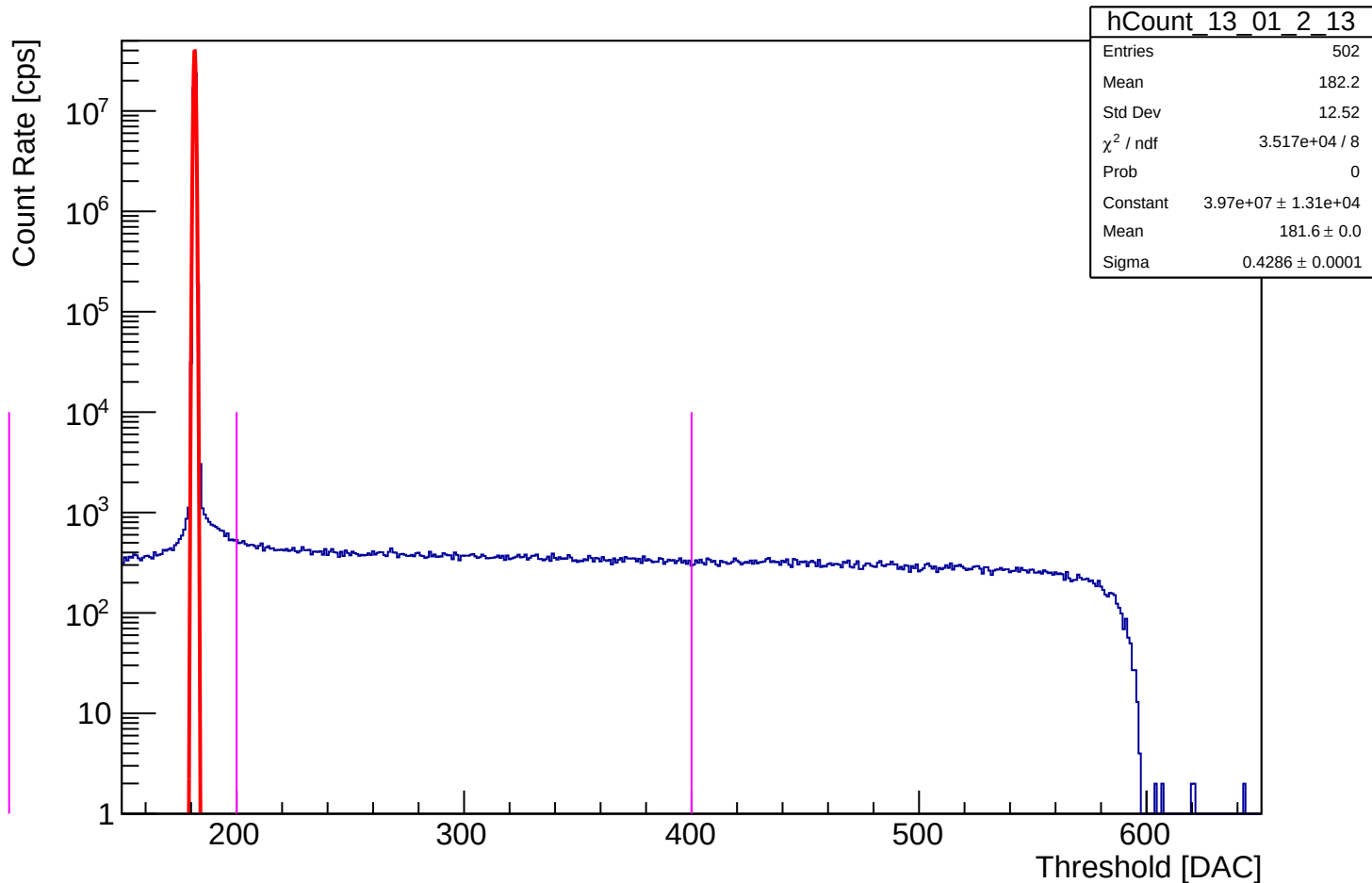
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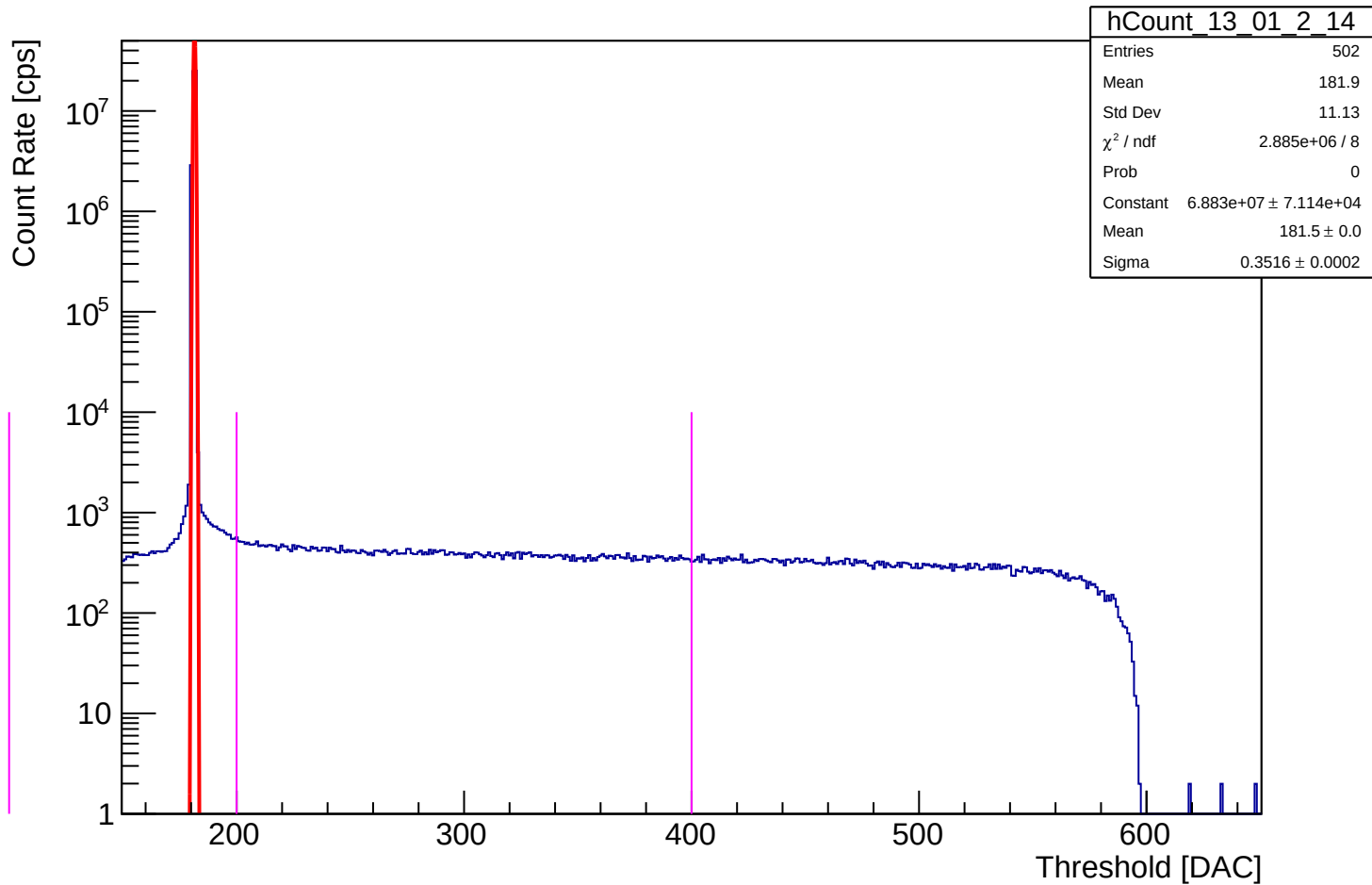
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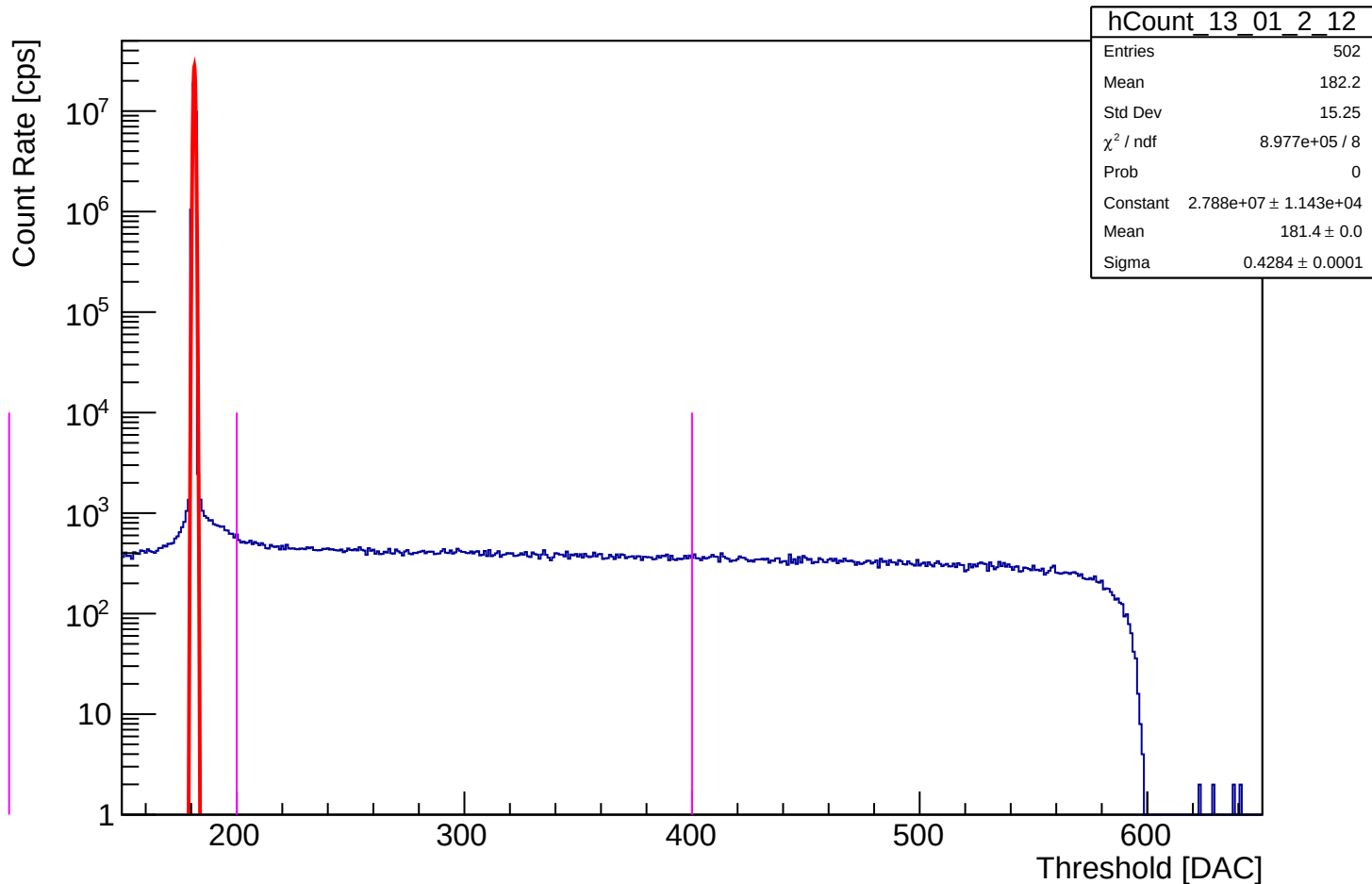
Row 1 Tile 1 Pmt 6 Pixel 34 Slot 13 Fiber 1 Asic 2 Channel 13



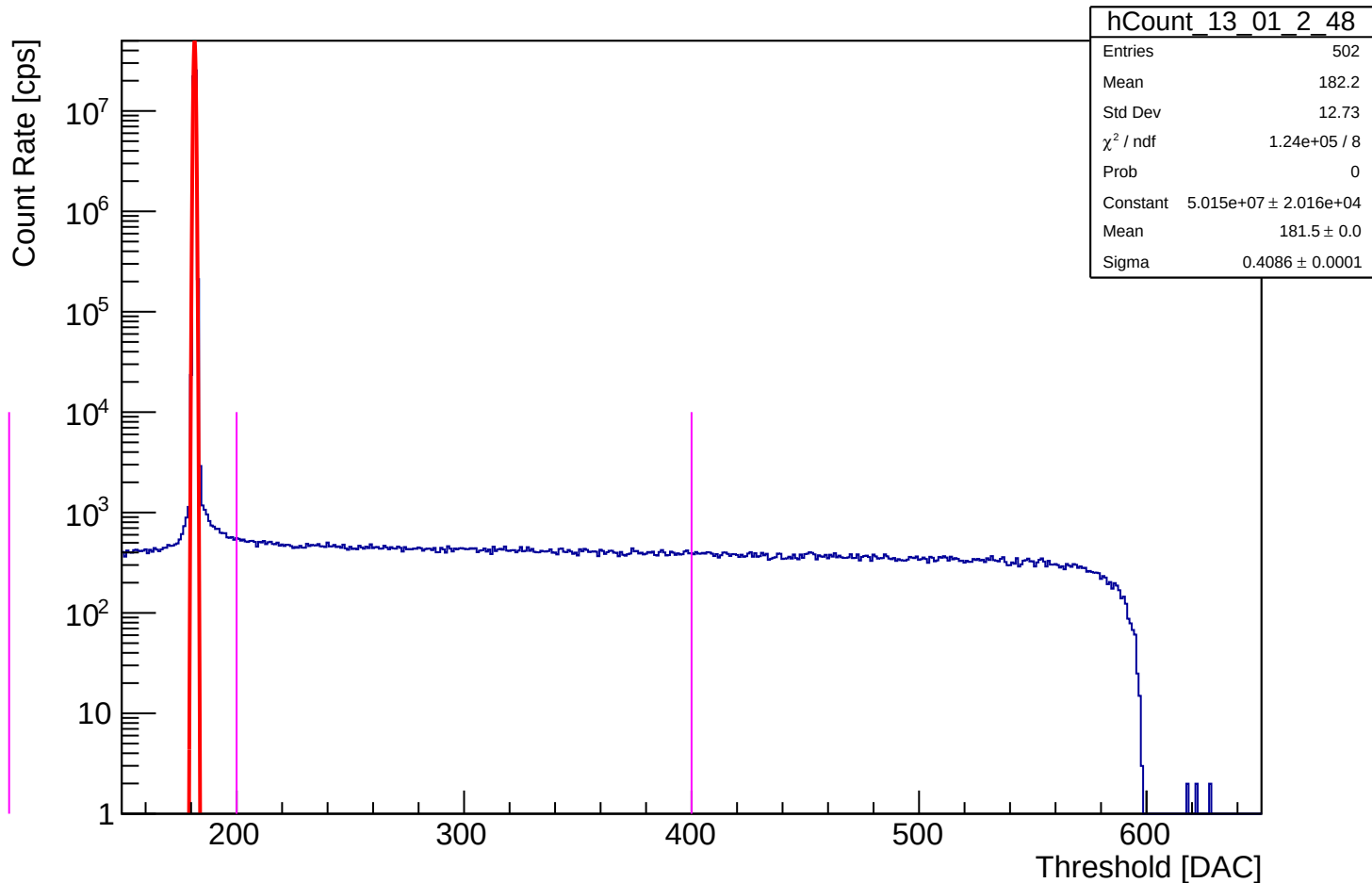
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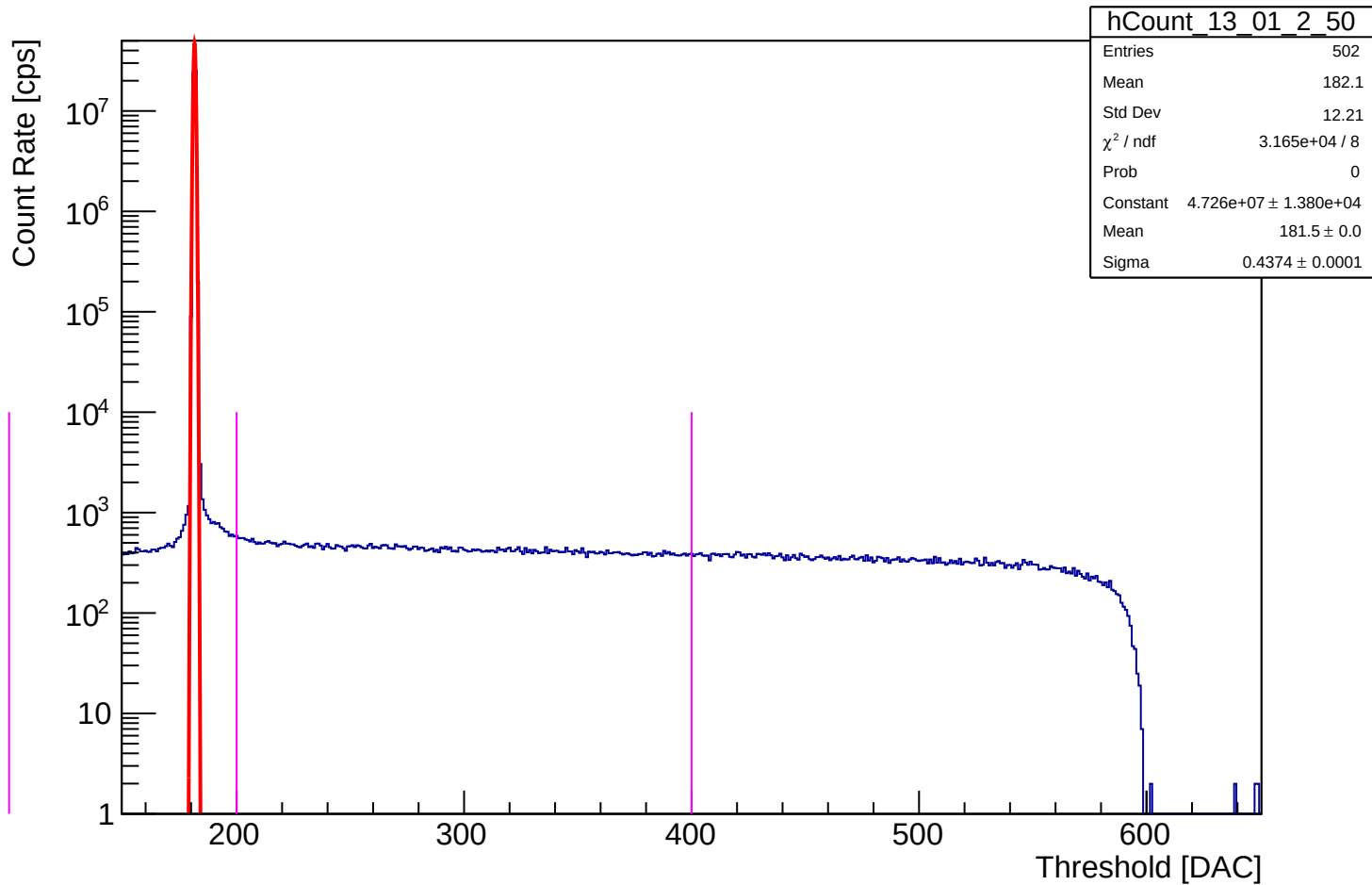
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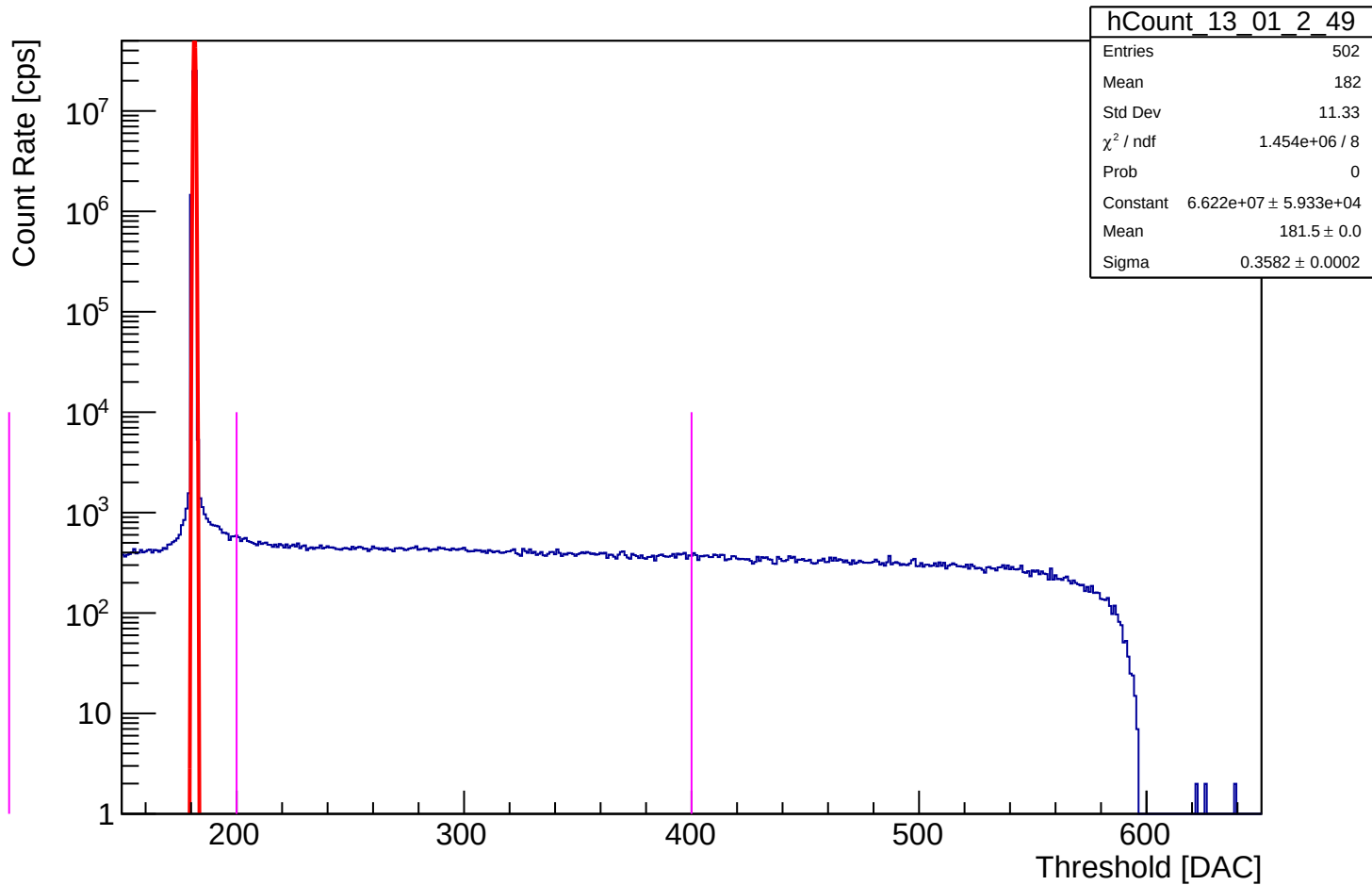
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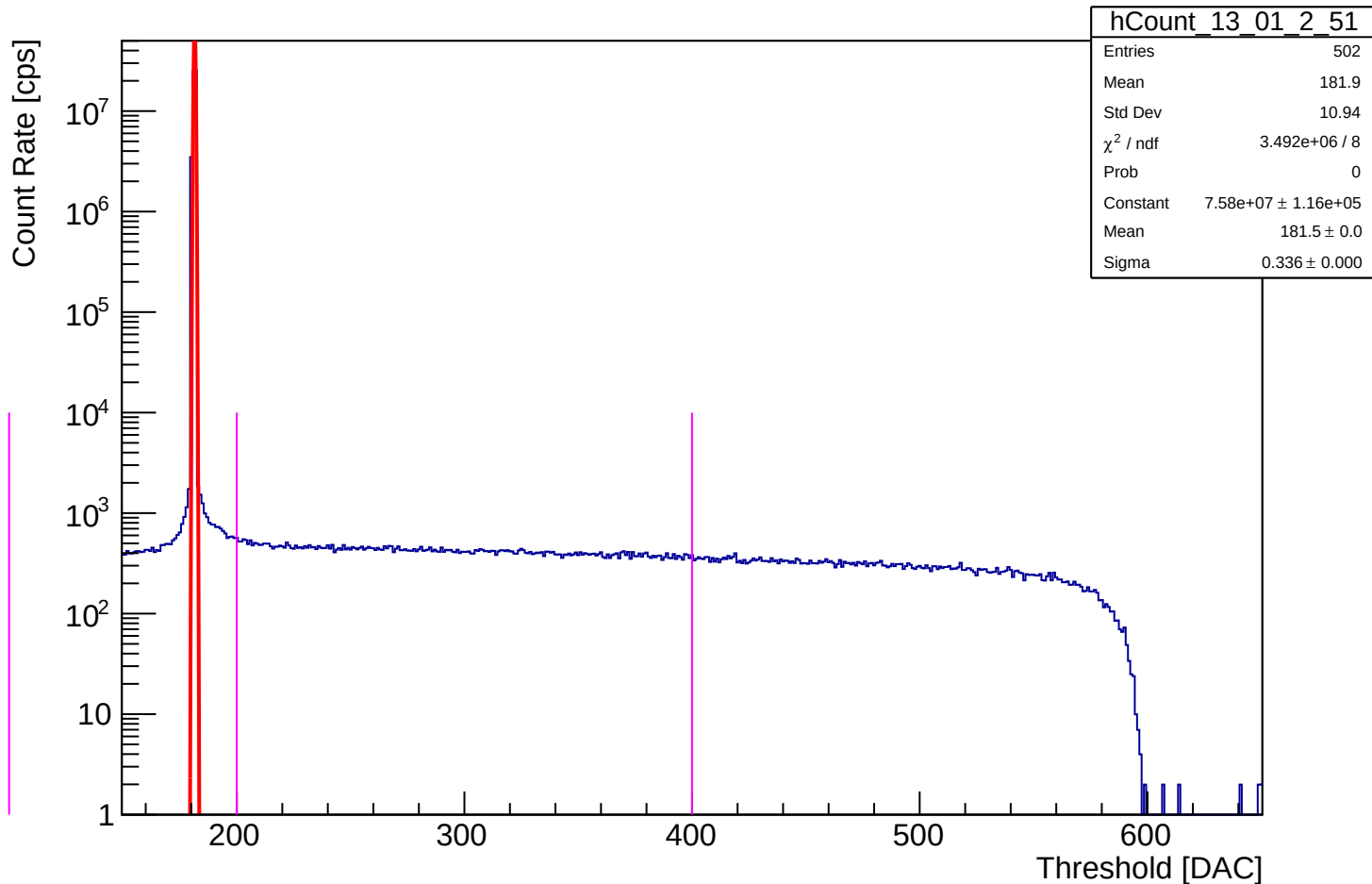
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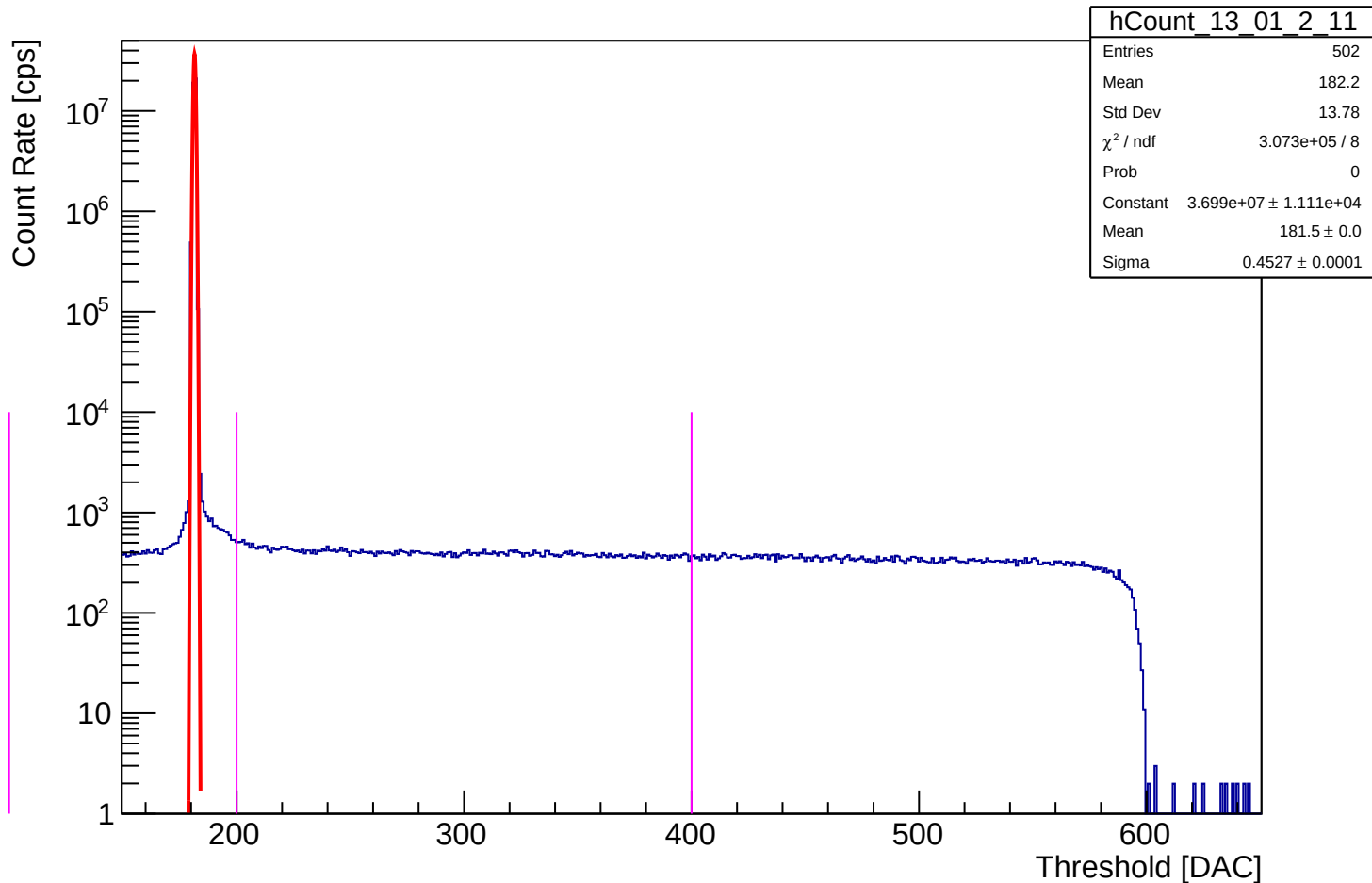
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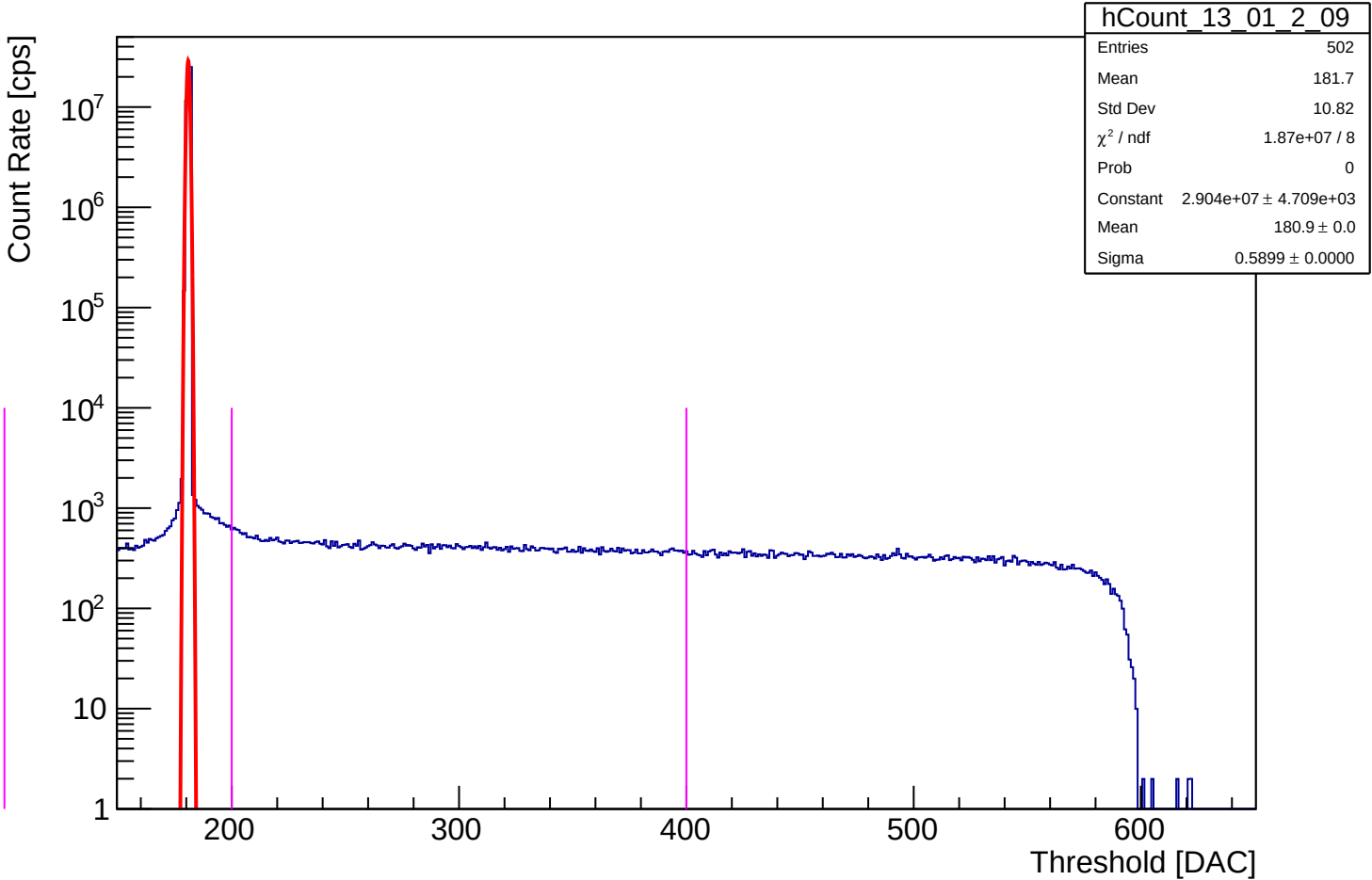


Row 1 Tile 1 Pmt 6 Pixel 40 Slot 13 Fiber 1 Asic 2 Channel 51

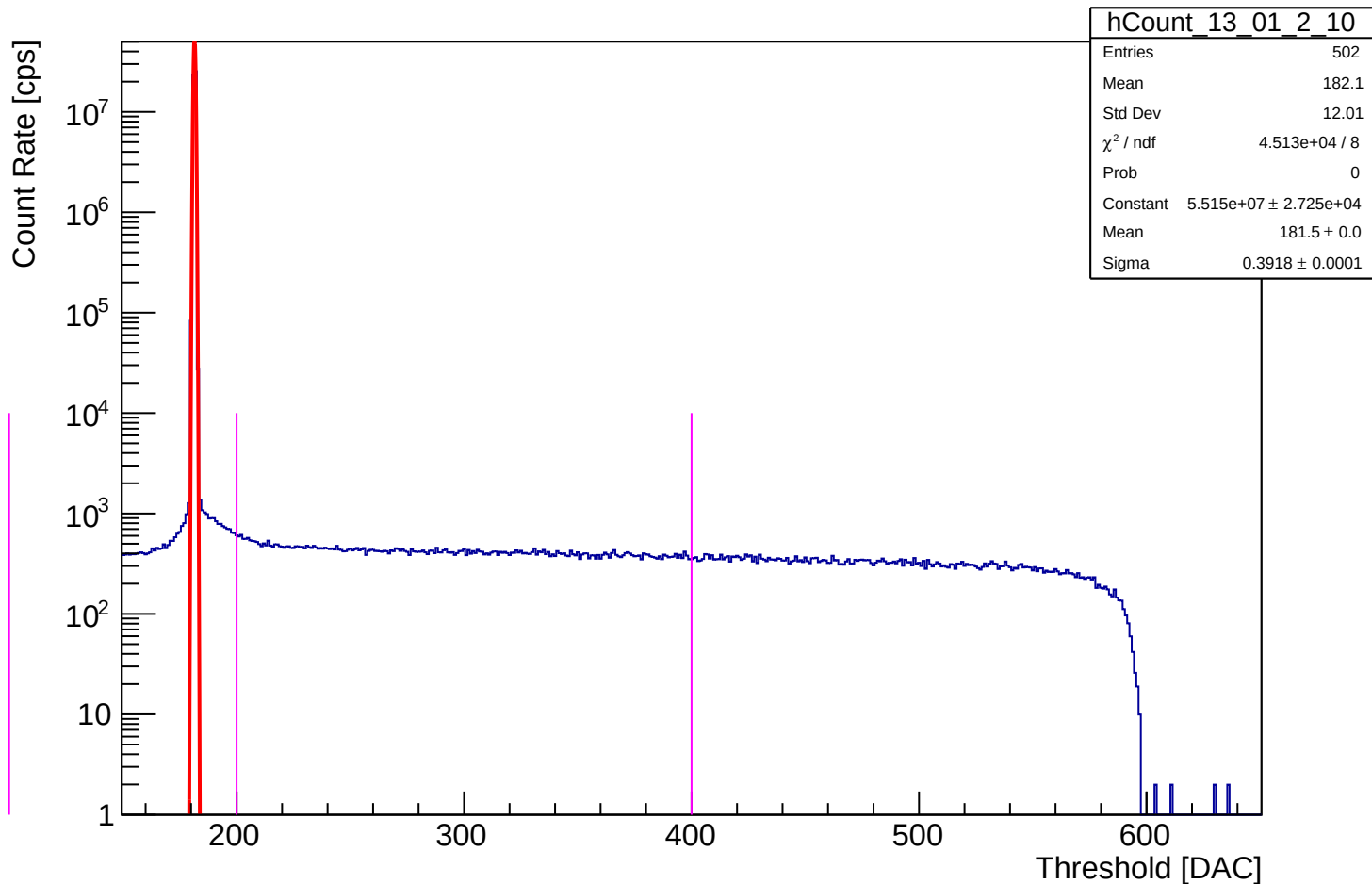


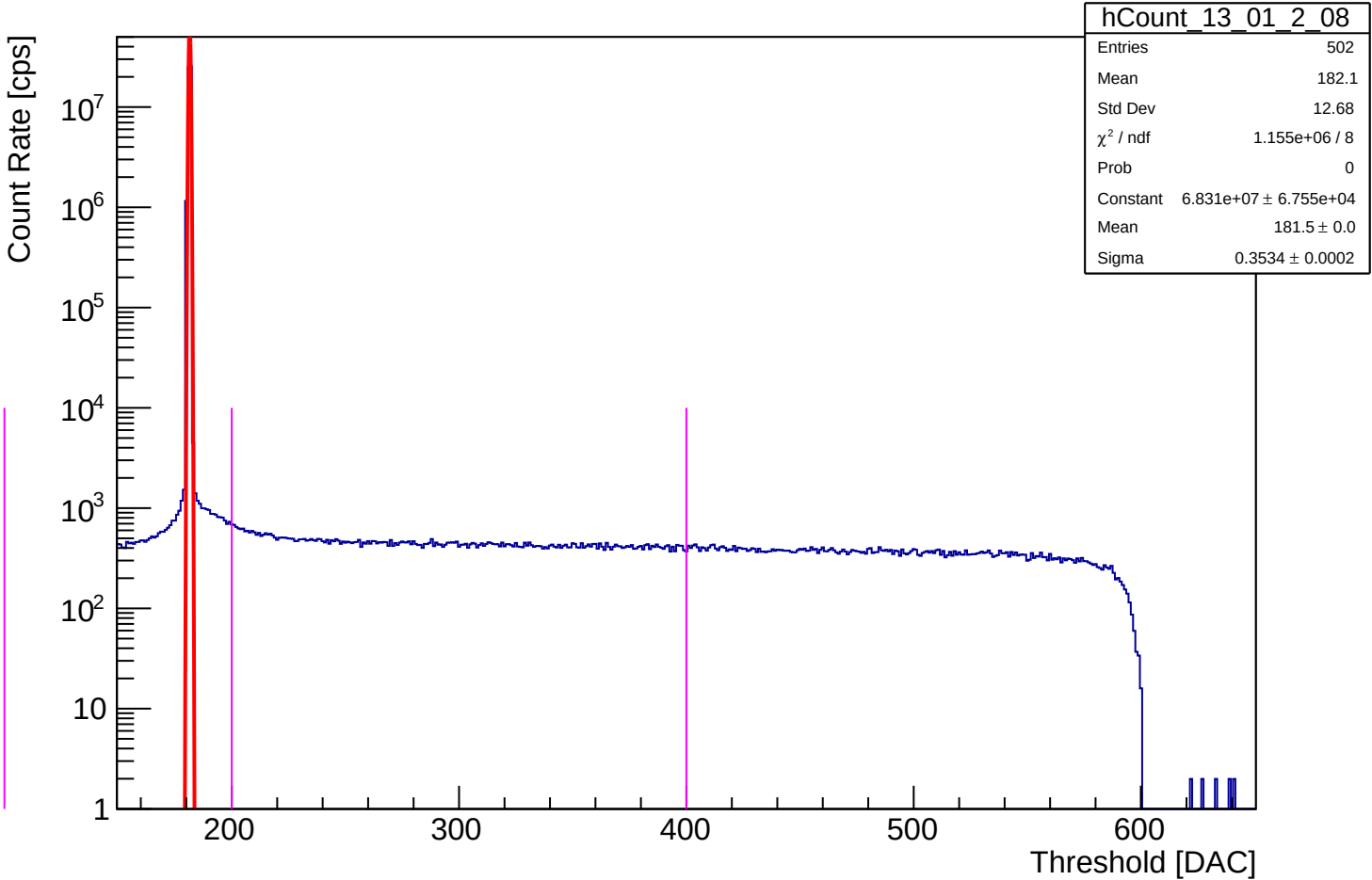
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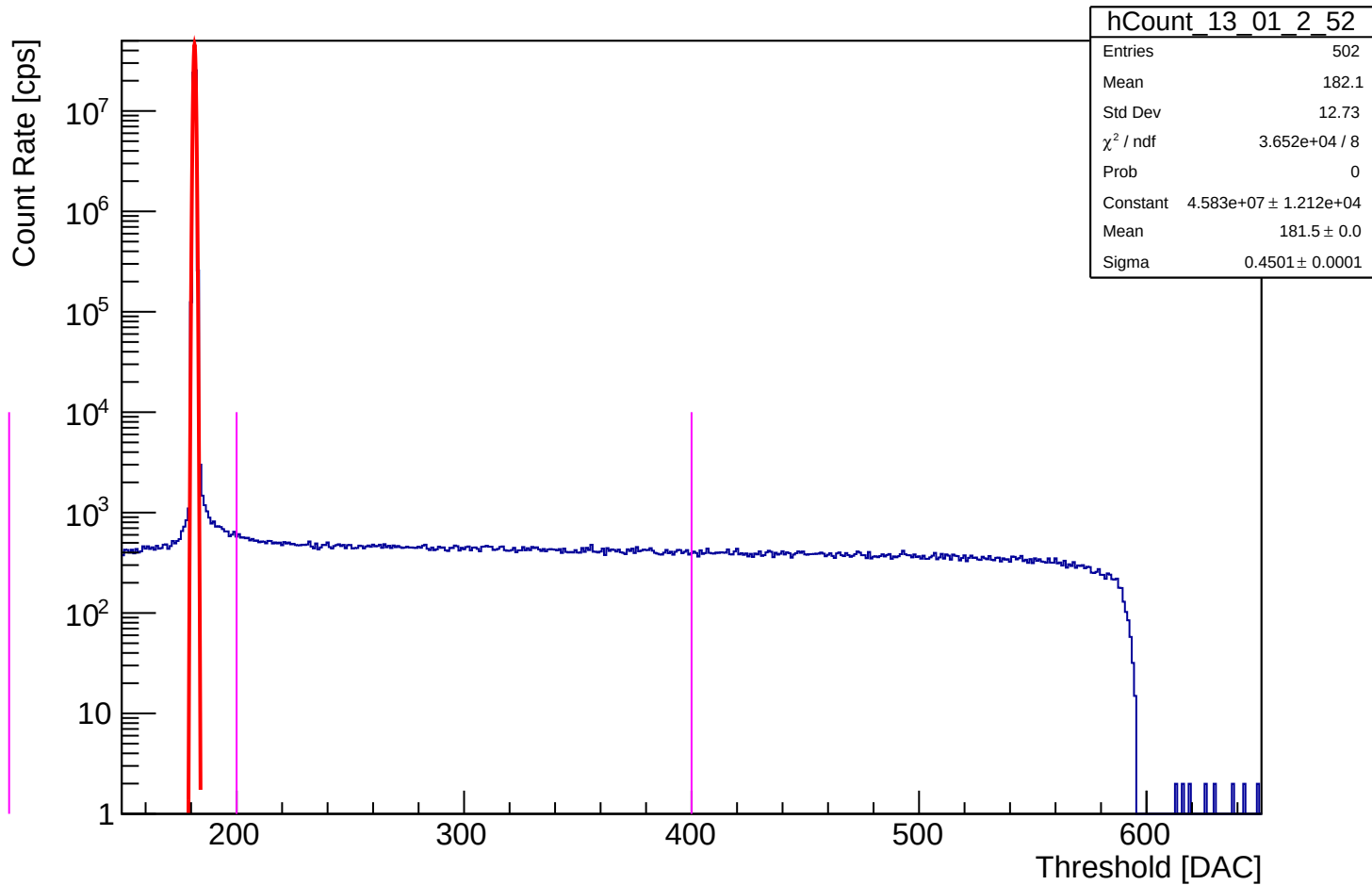


Row 1 Tile 1 Pmt 6 Pixel 43 Slot 13 Fiber 1 Asic 2 Channel 10

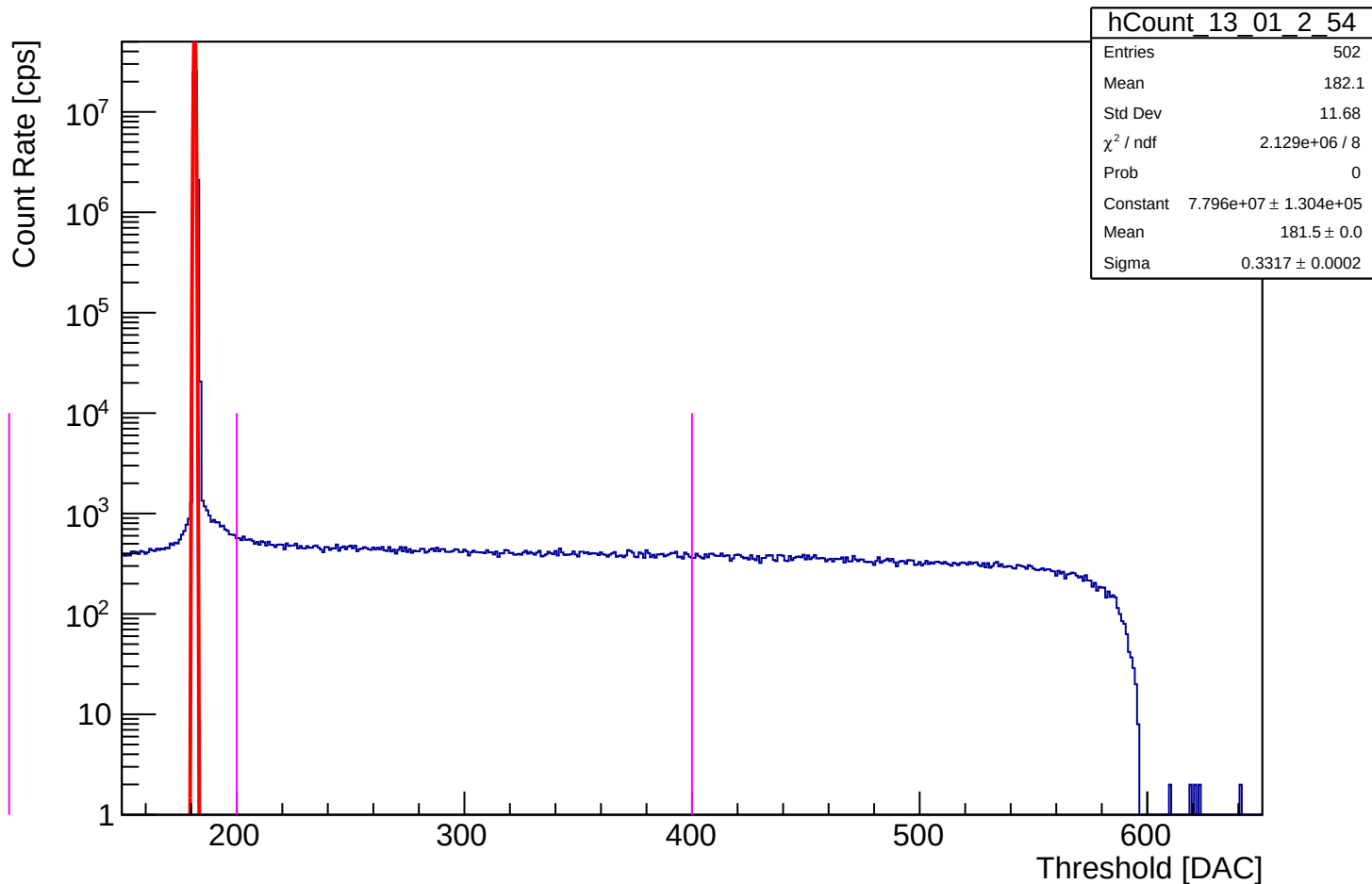




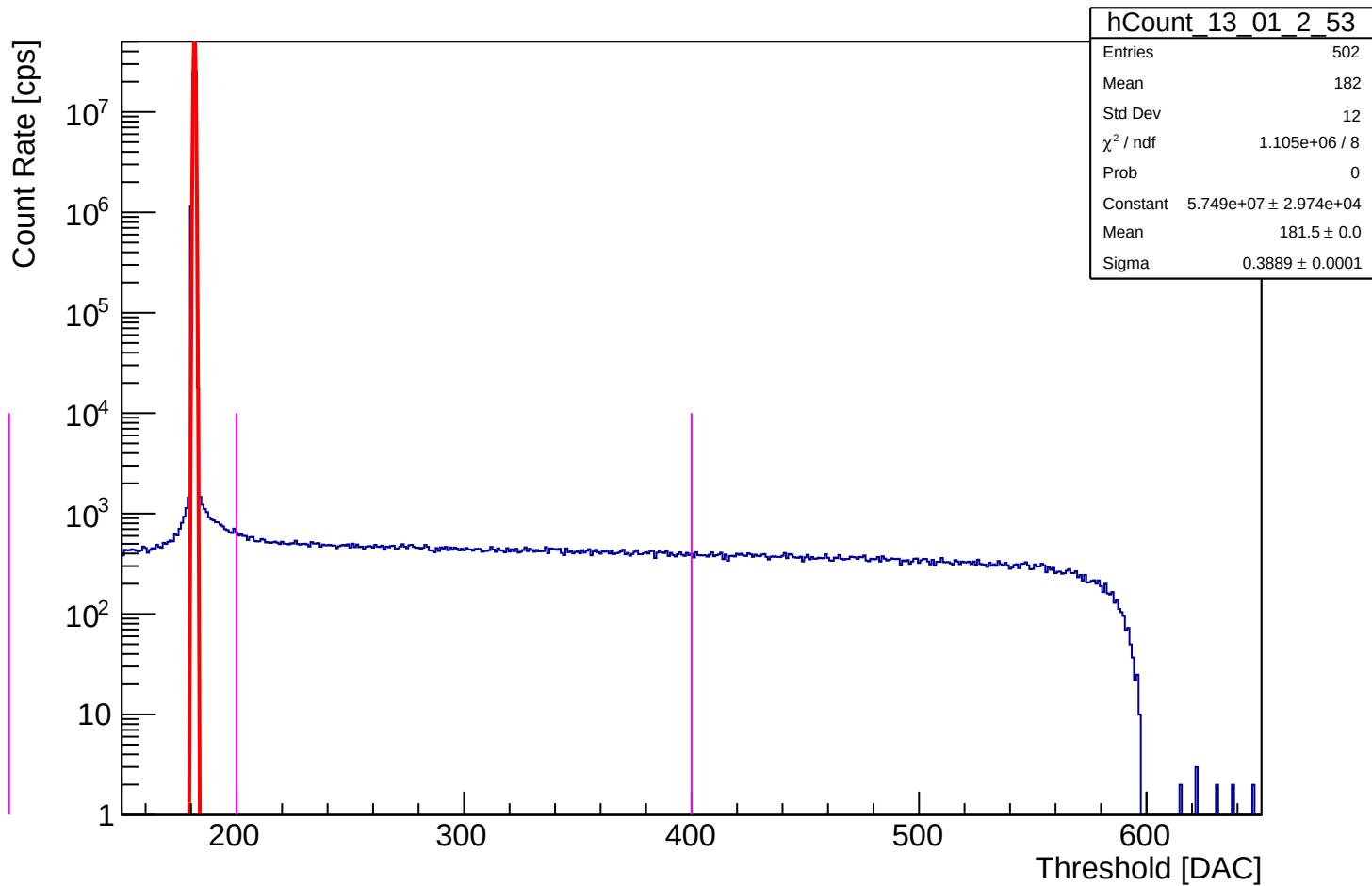
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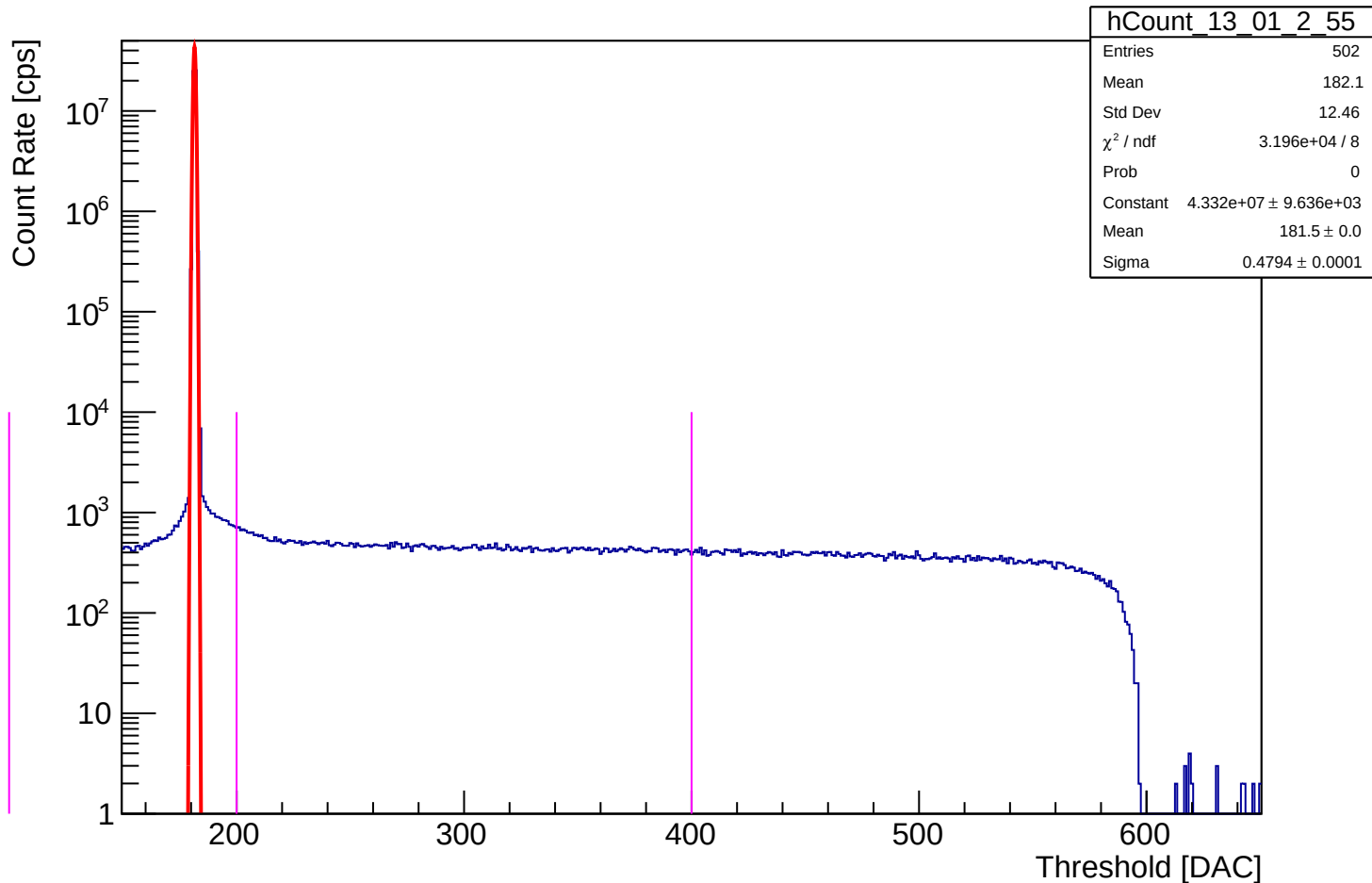
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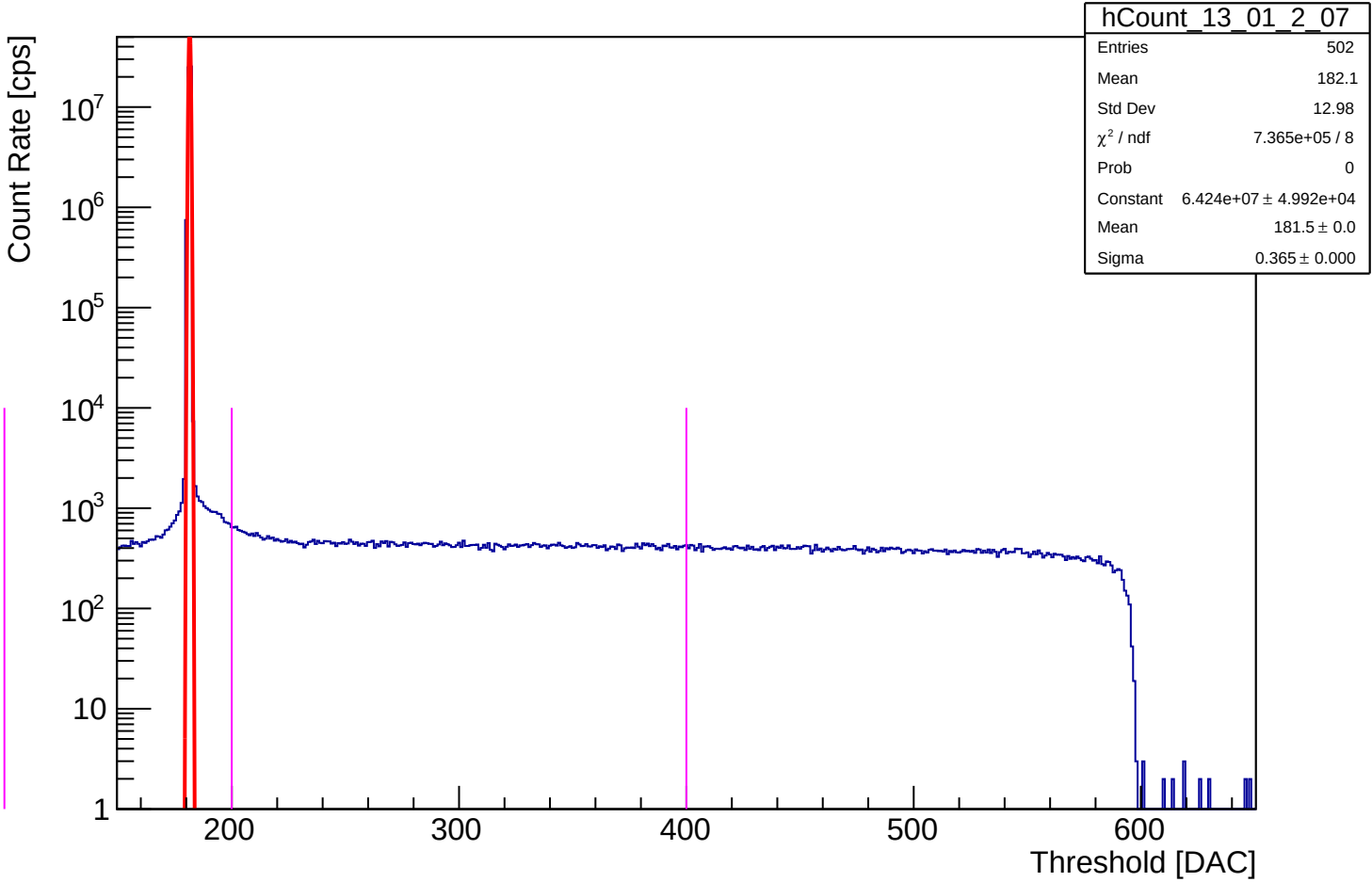


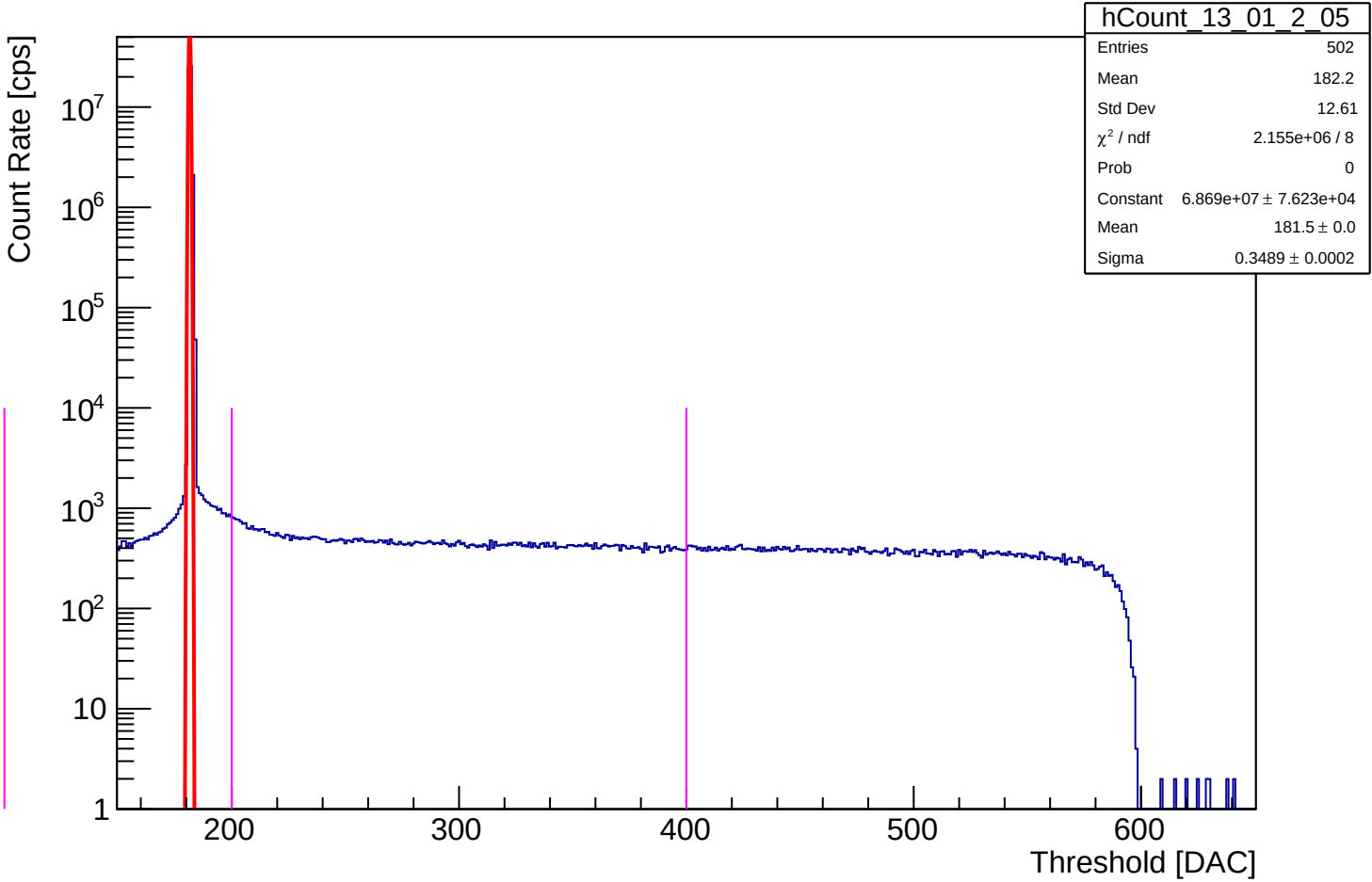
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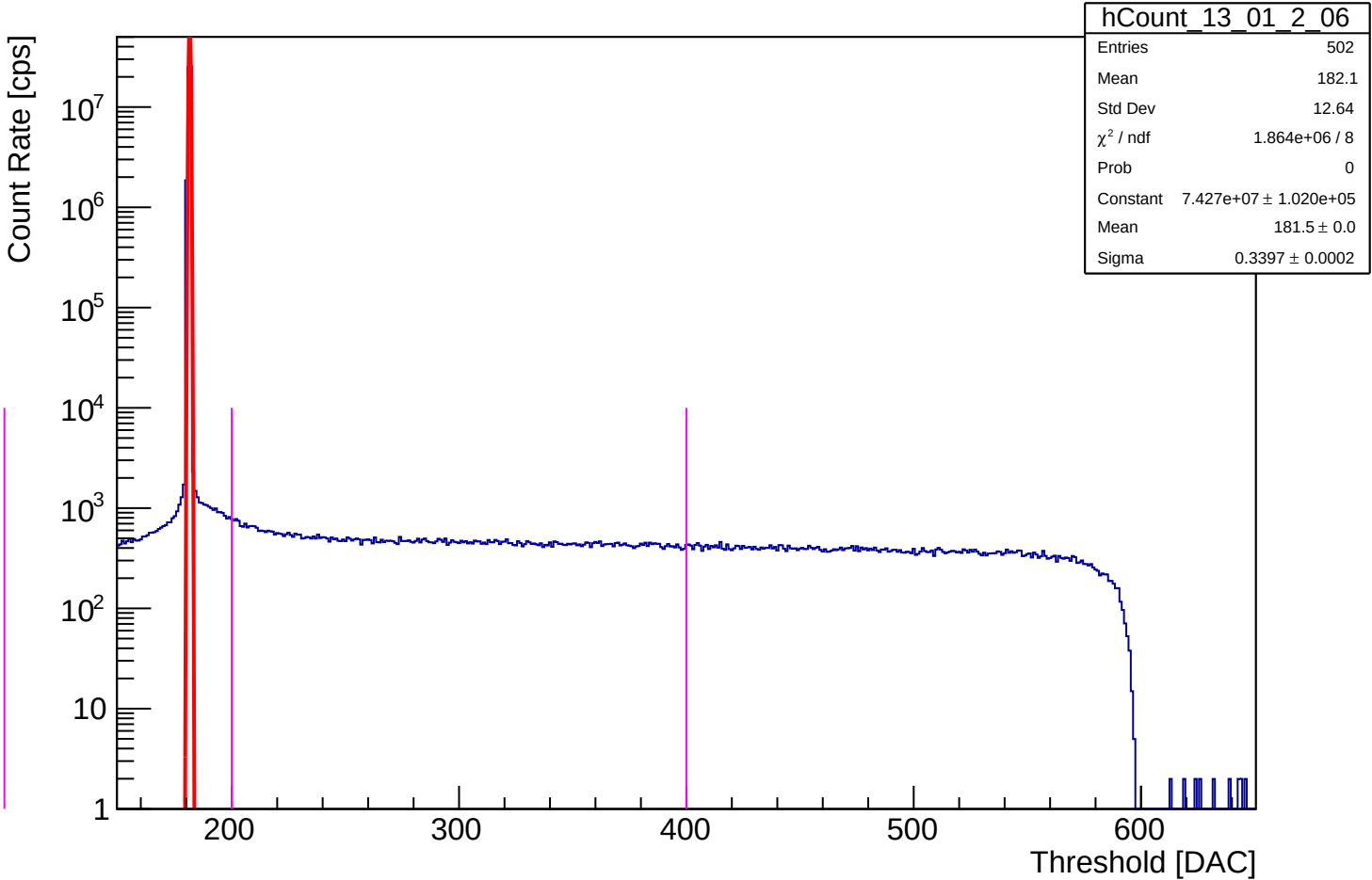


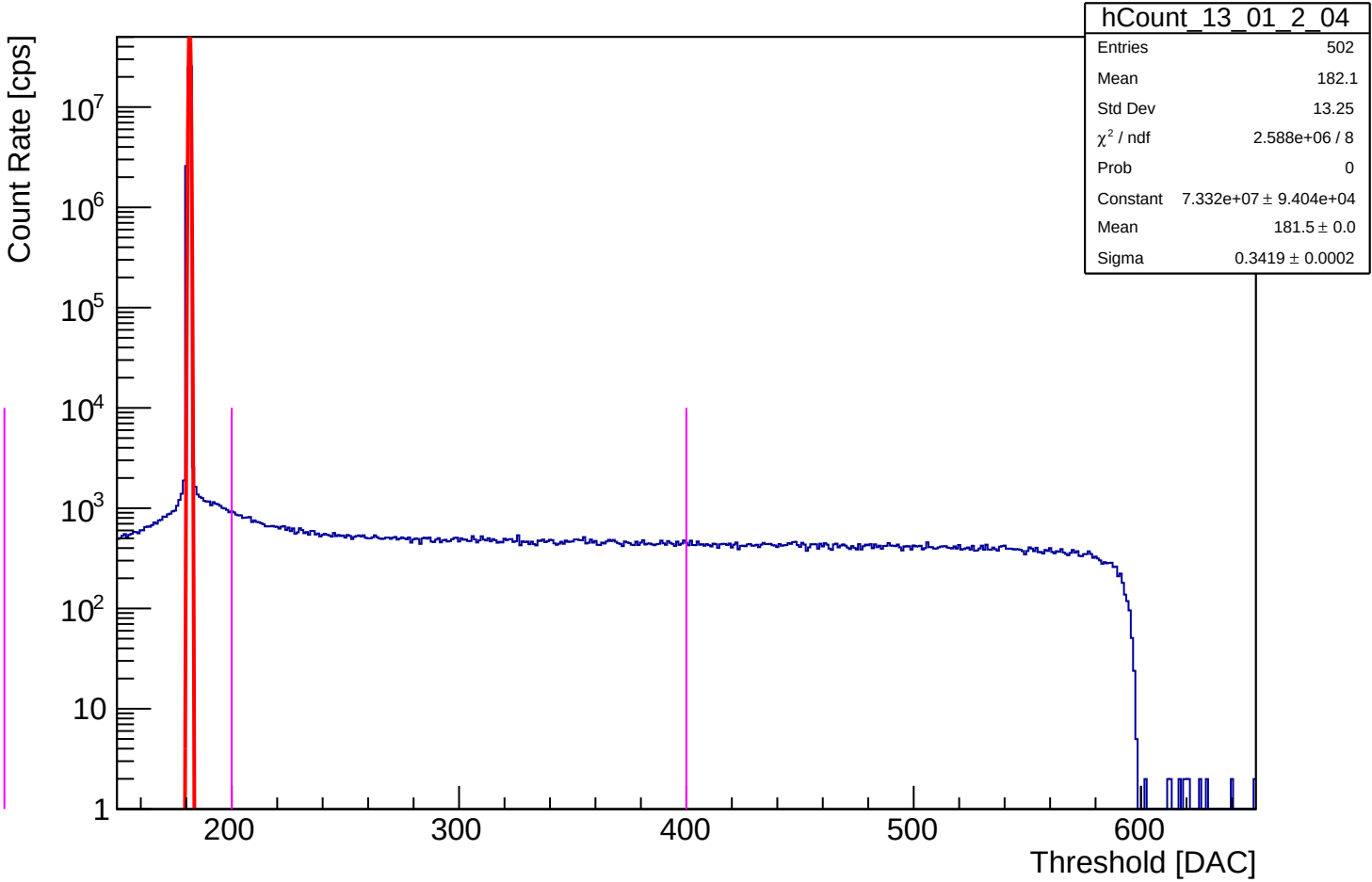
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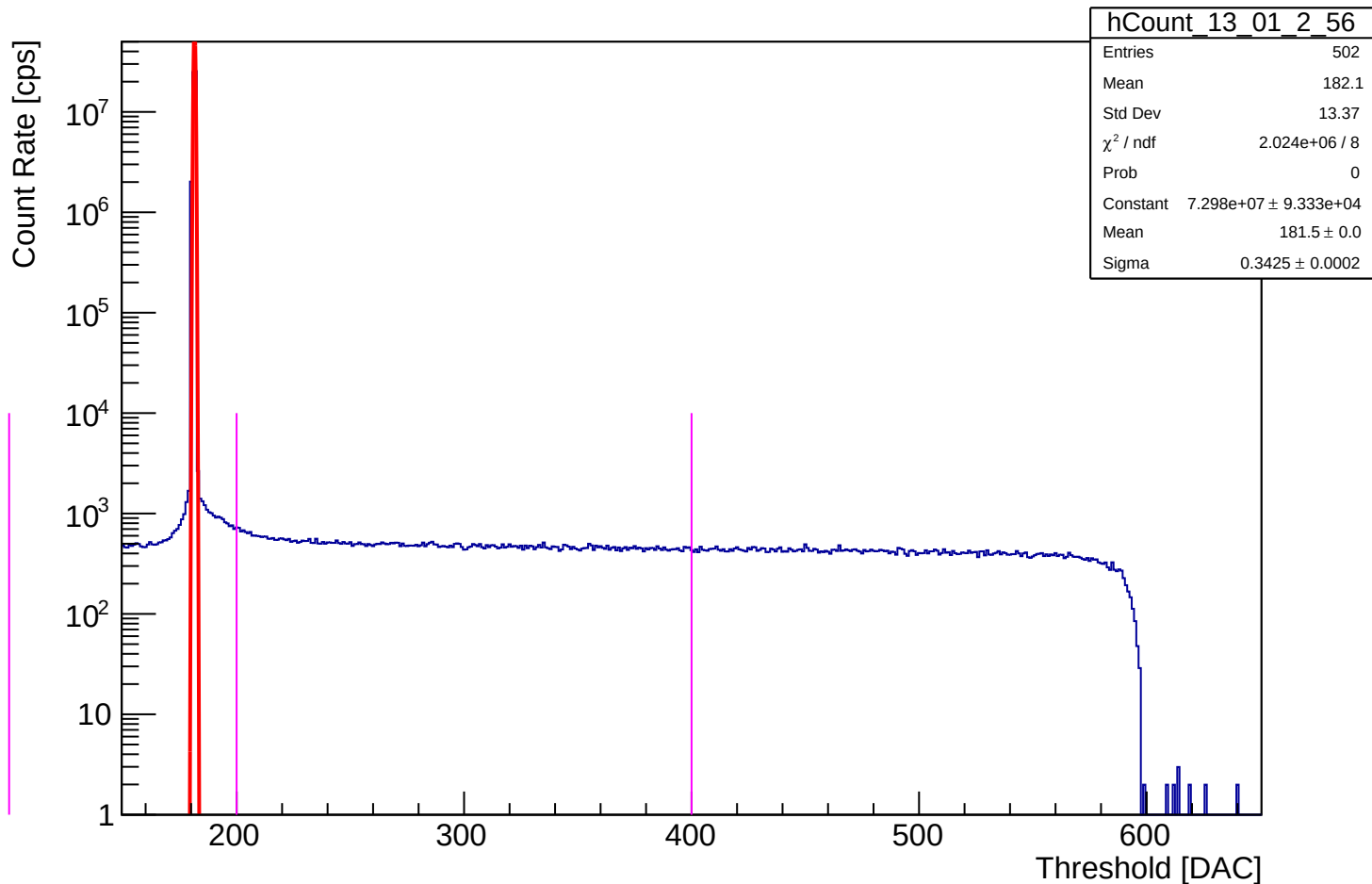




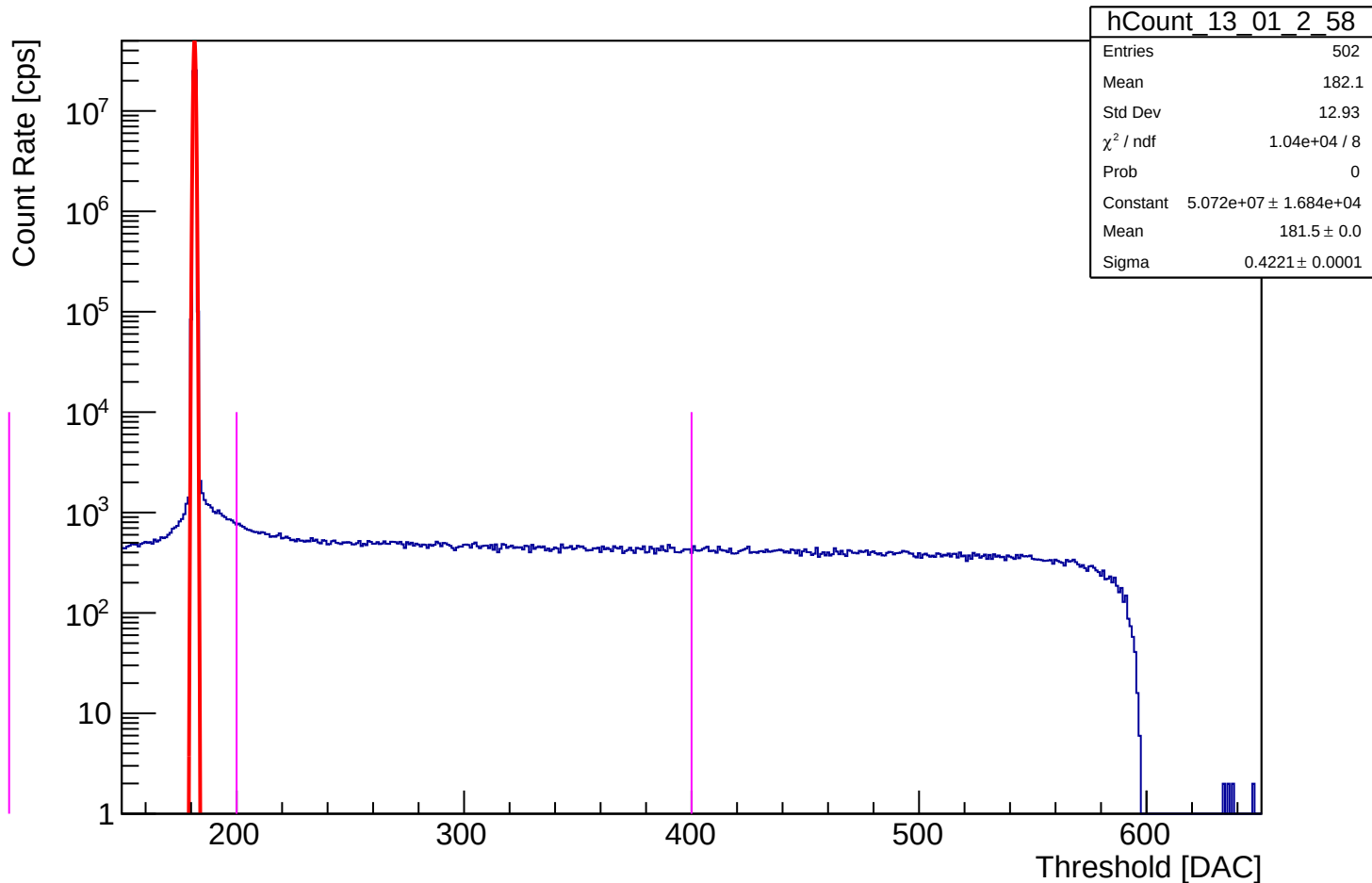




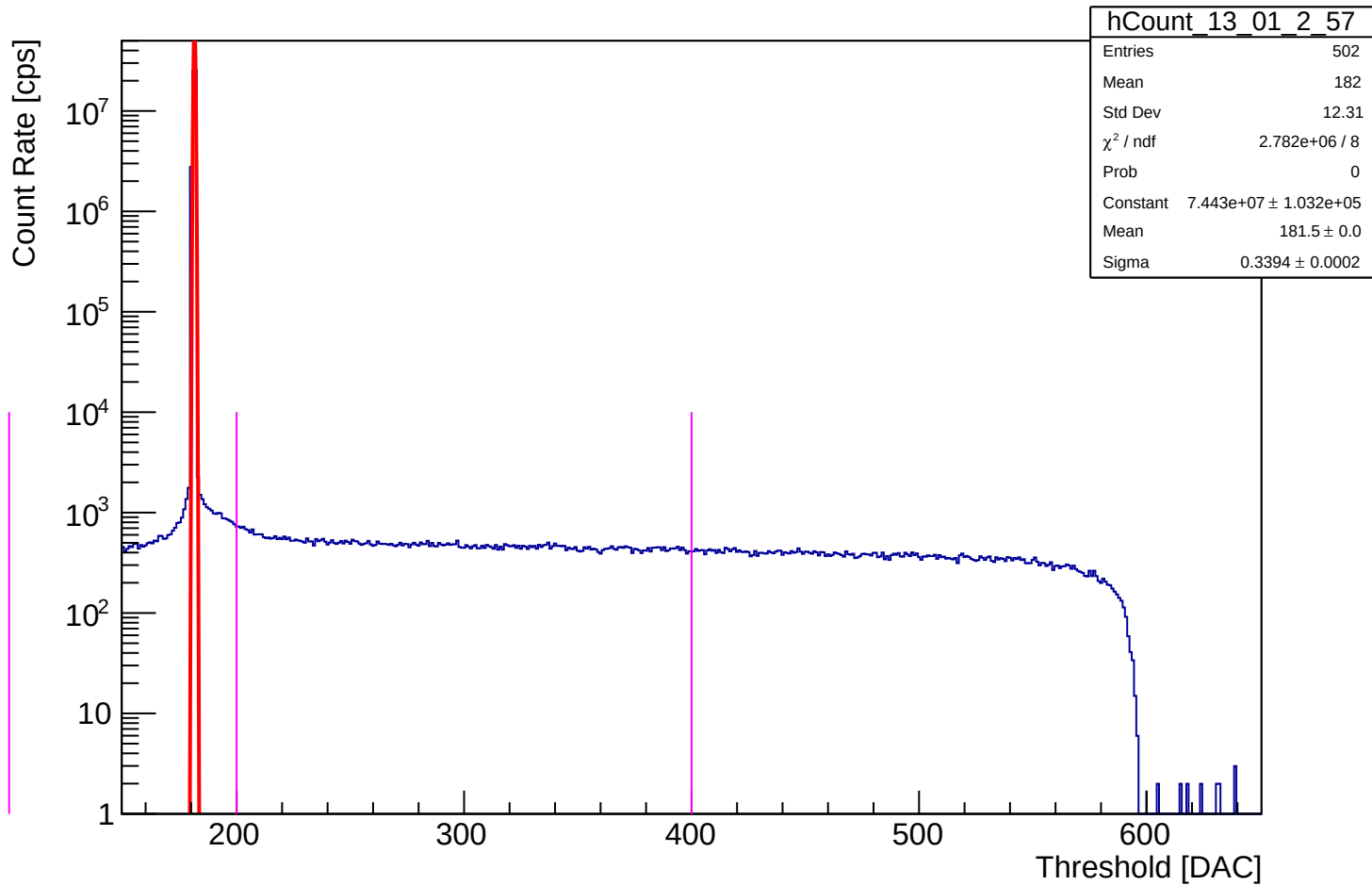
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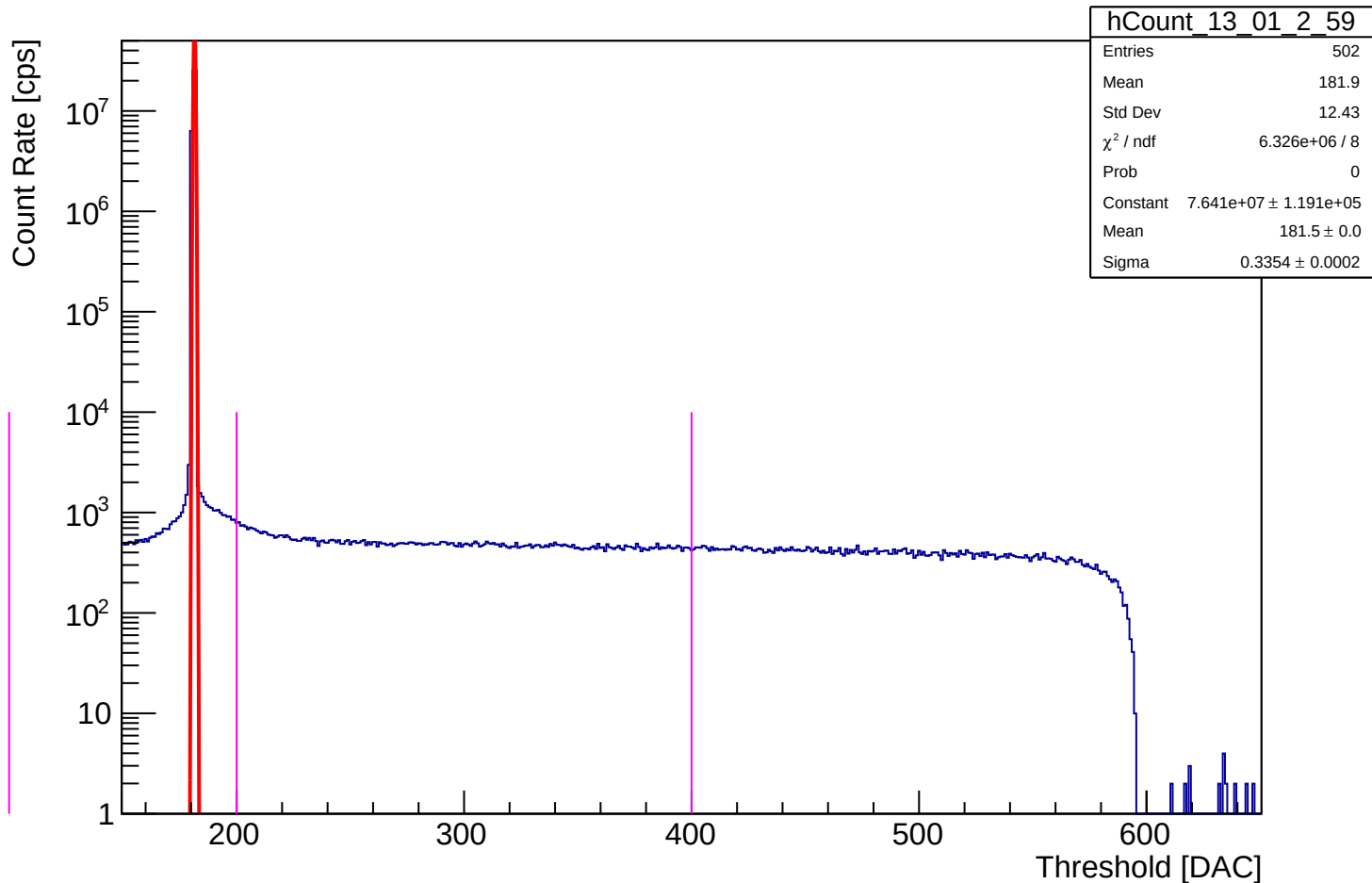
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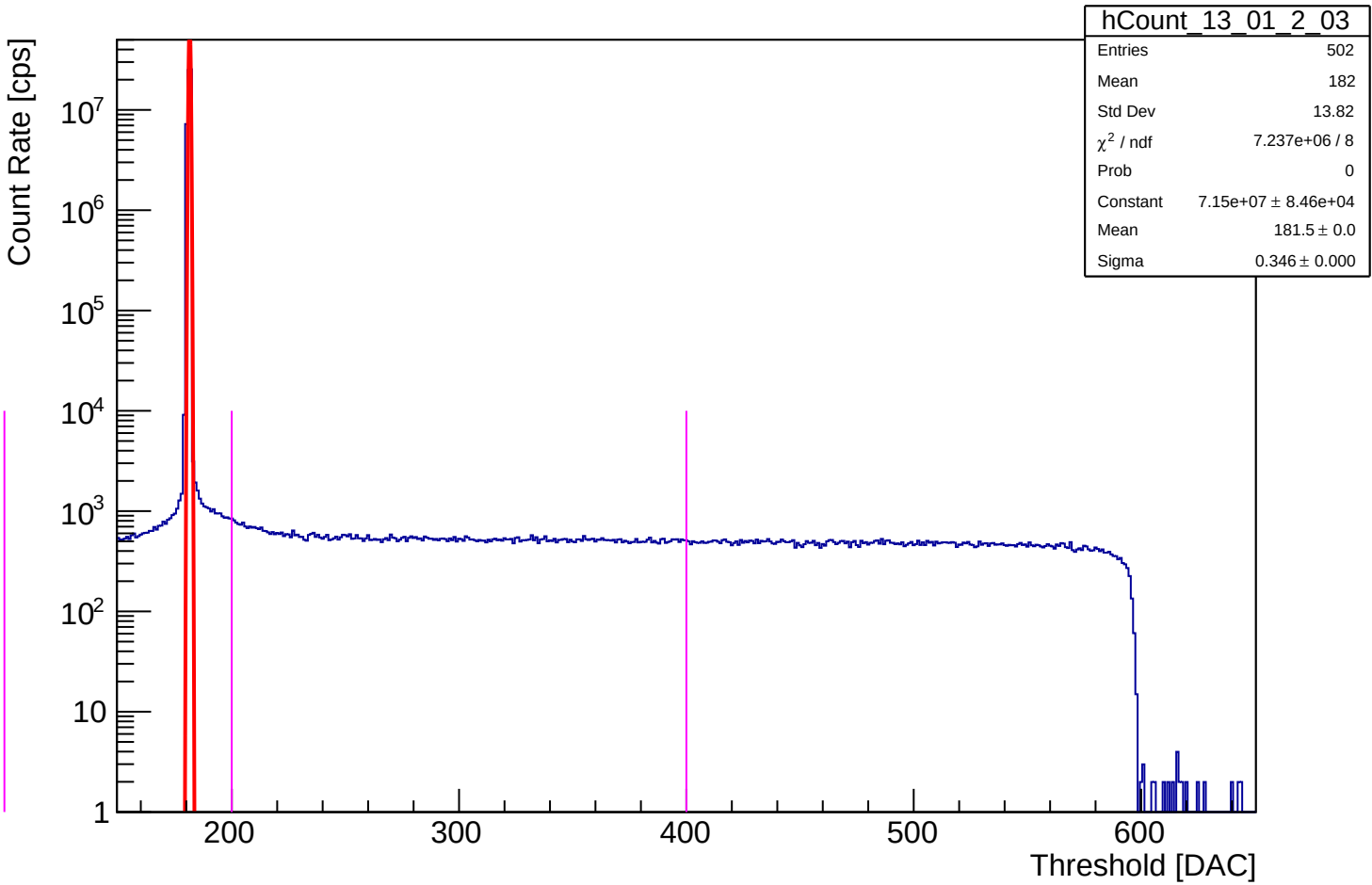


Row 1 Tile 1 Pmt 6 Pixel 55 Slot 13 Fiber 1 Asic 2 Channel 57

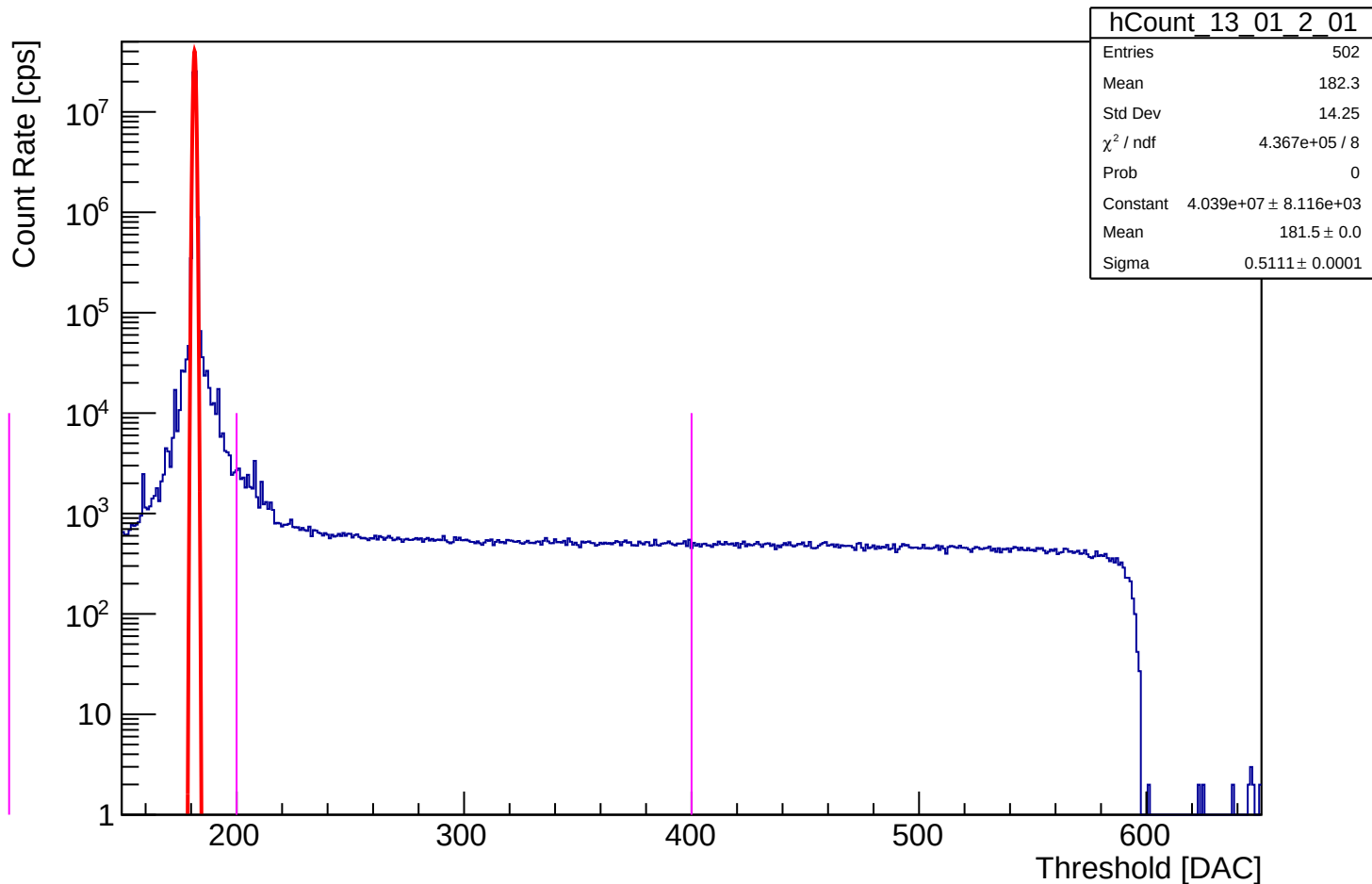


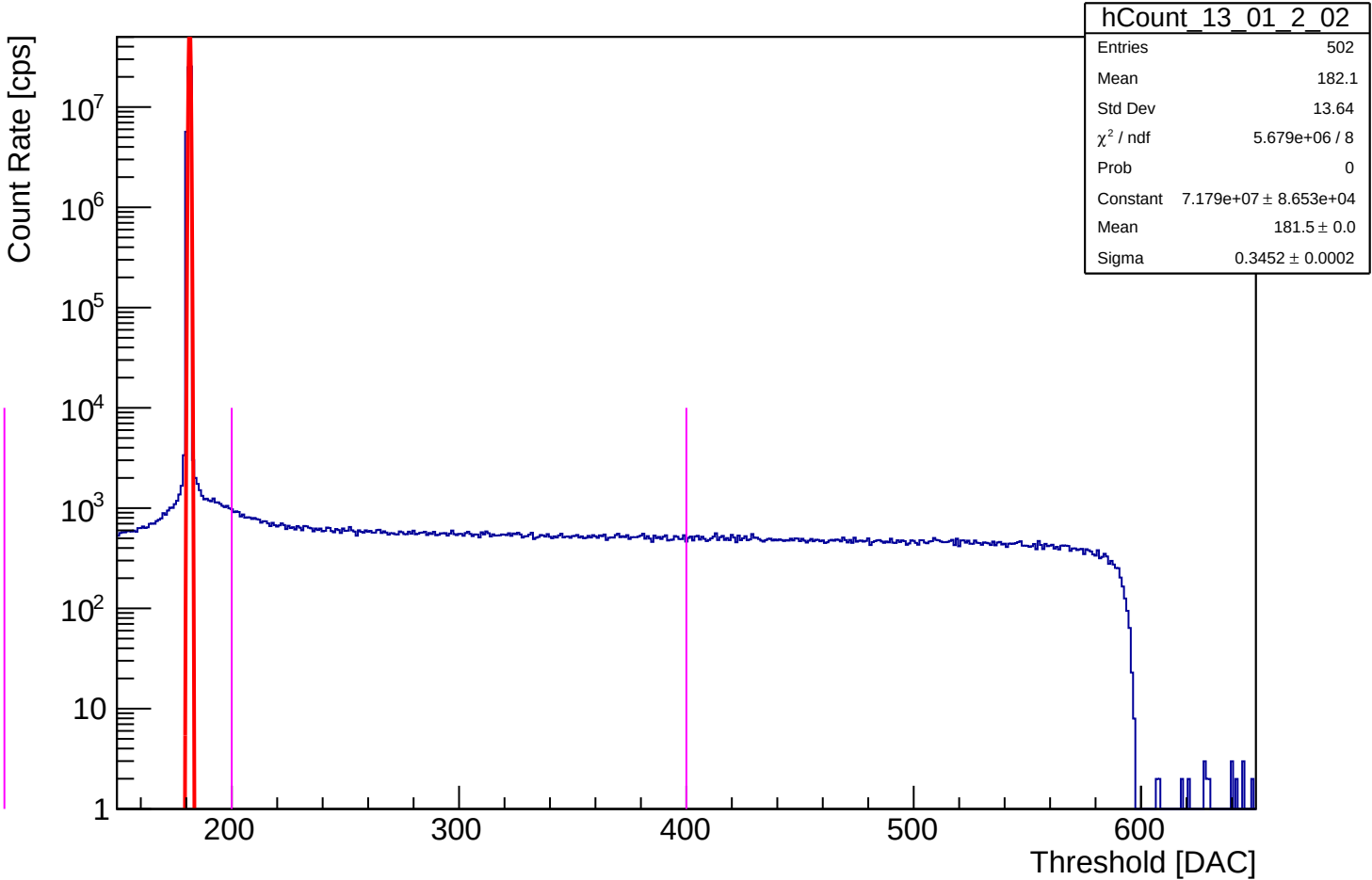
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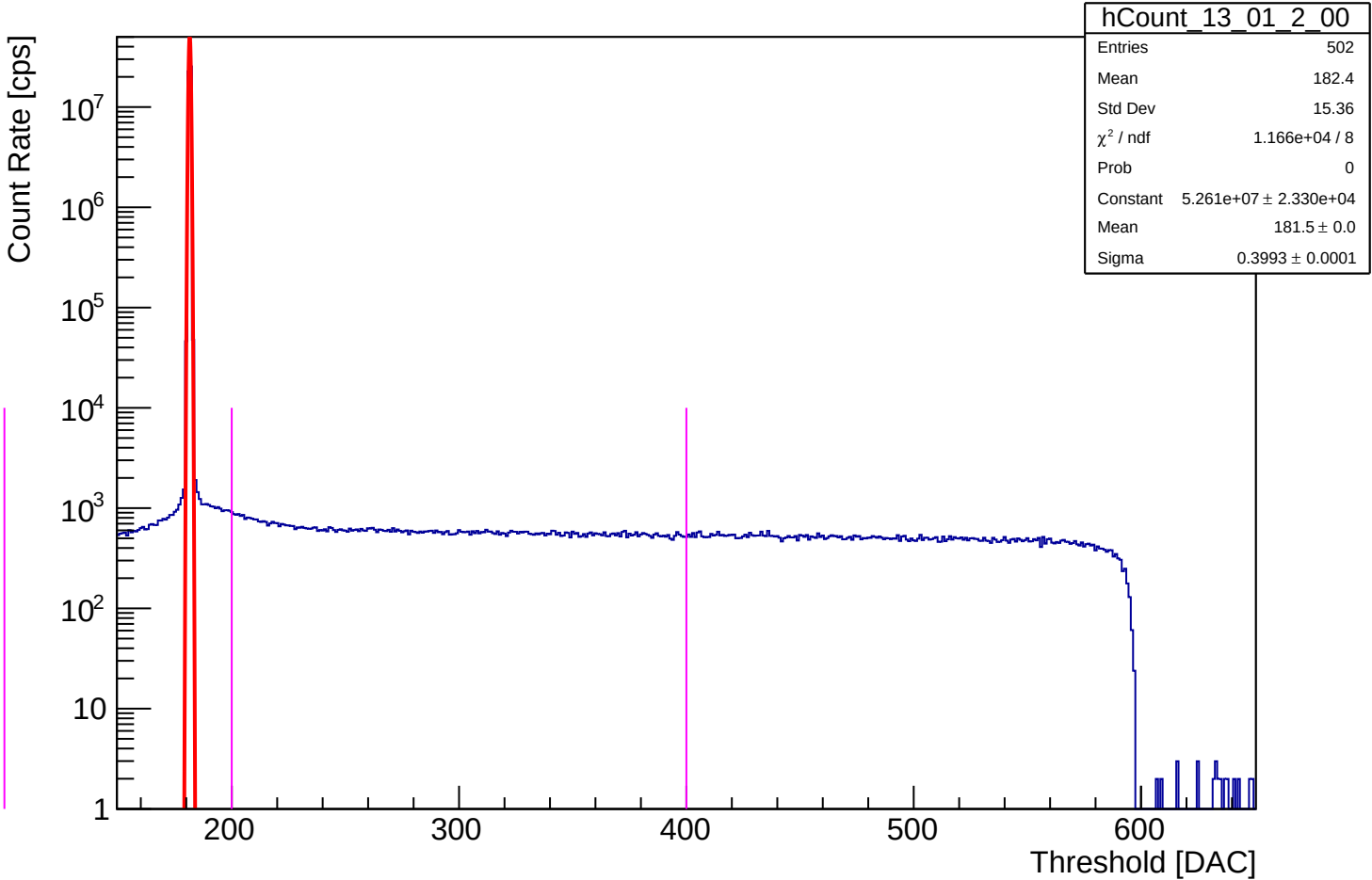




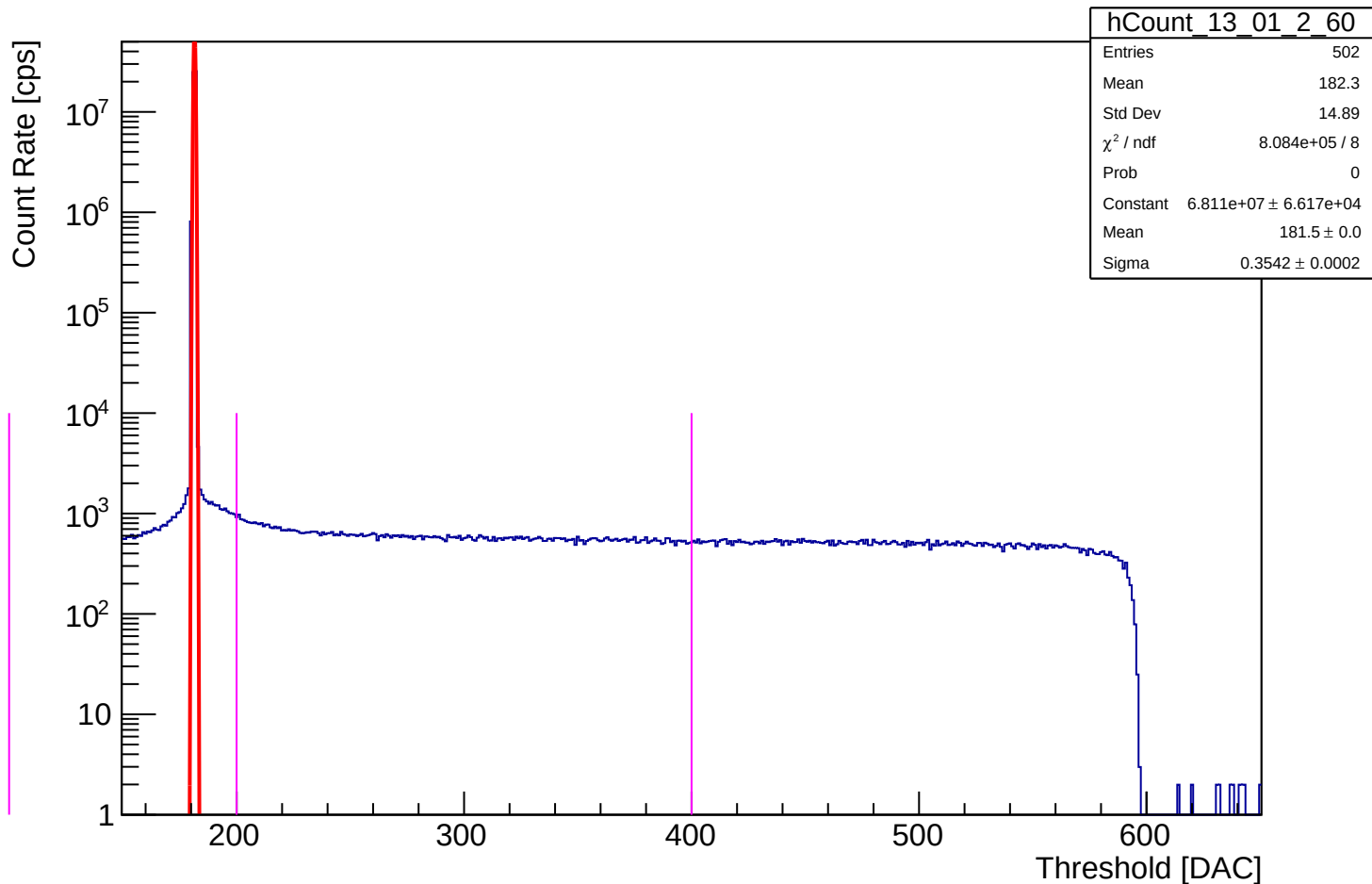
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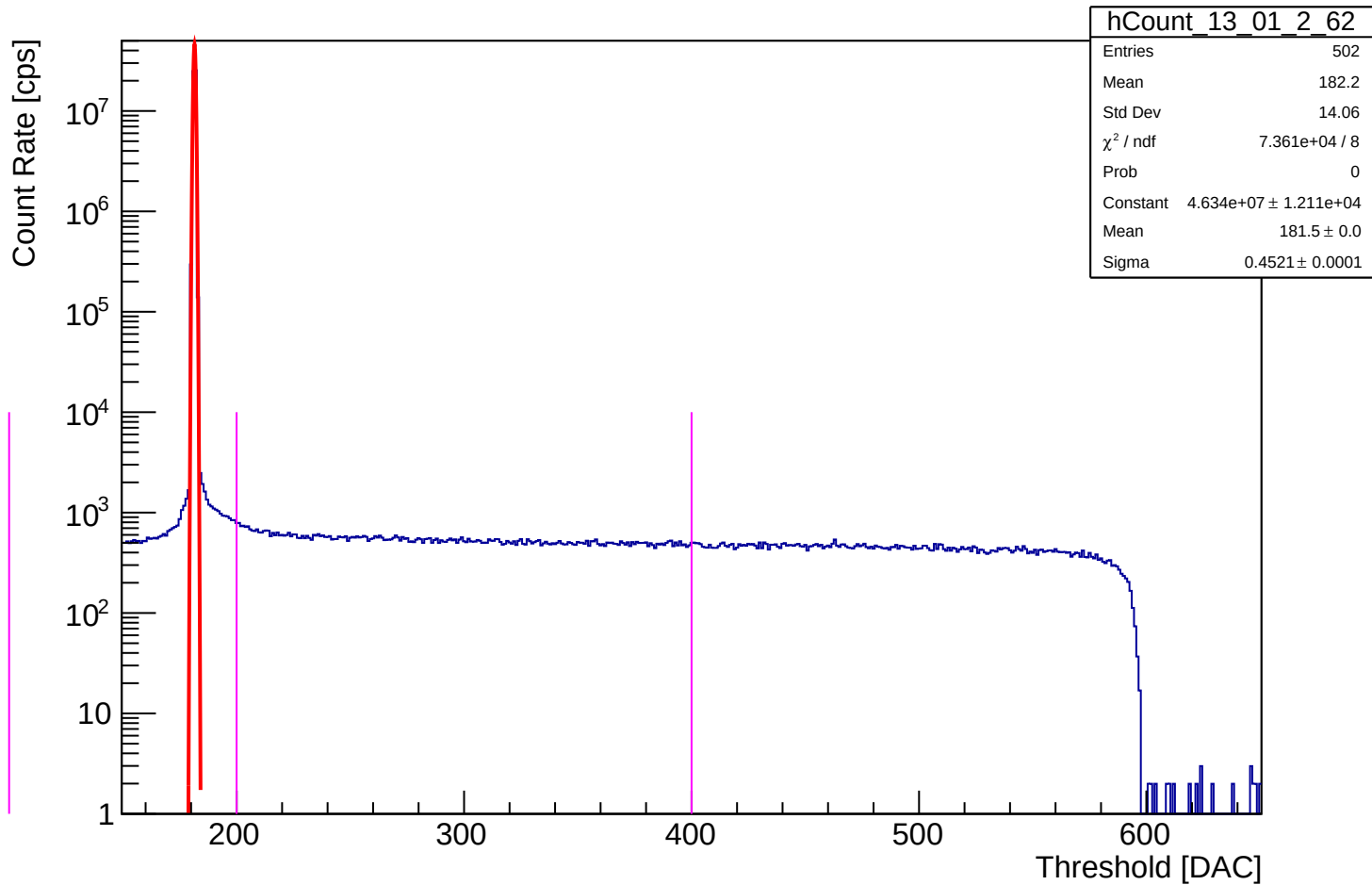




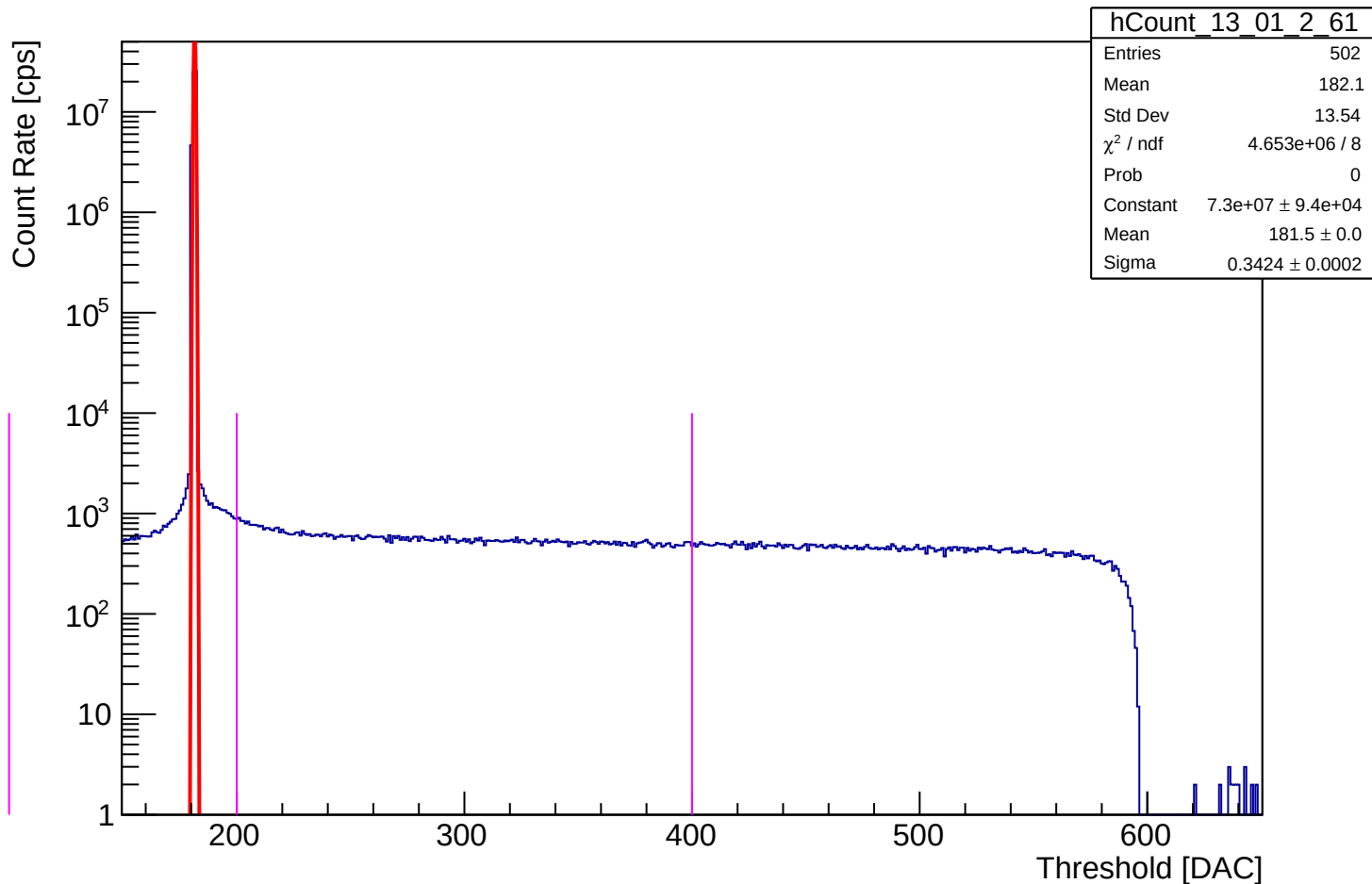
Row 1 Tile 1 Pmt 6 Pixel 61 Slot 13 Fiber 1 Asic 2 Channel 60



Row 1 Tile 1 Pmt 6 Pixel 62 Slot 13 Fiber 1 Asic 2 Channel 62



Row 1 Tile 1 Pmt 6 Pixel 63 Slot 13 Fiber 1 Asic 2 Channel 61



Row 1 Tile 1 Pmt 6 Pixel 64 Slot 13 Fiber 1 Asic 2 Channel 63

