Trigger and DAQ for SoLID SIDIS Programs

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for SoLID-SIDIS Collaboration Meeting

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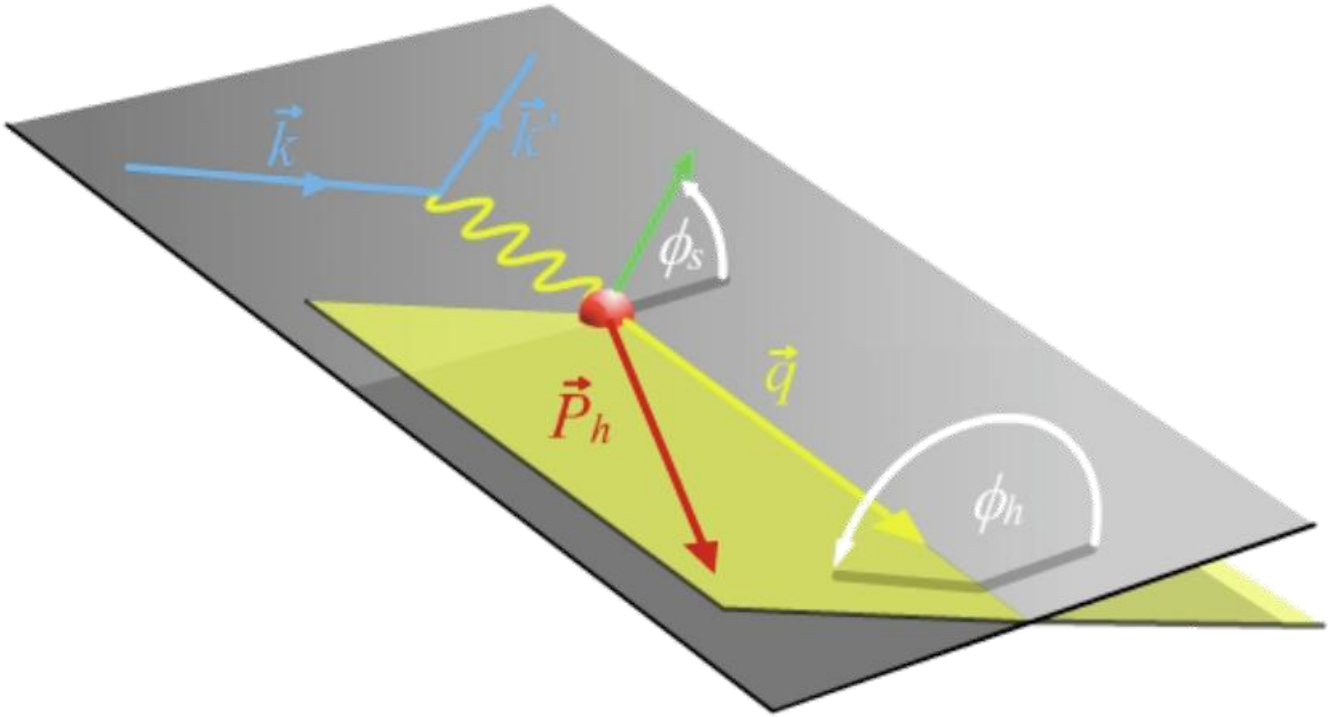
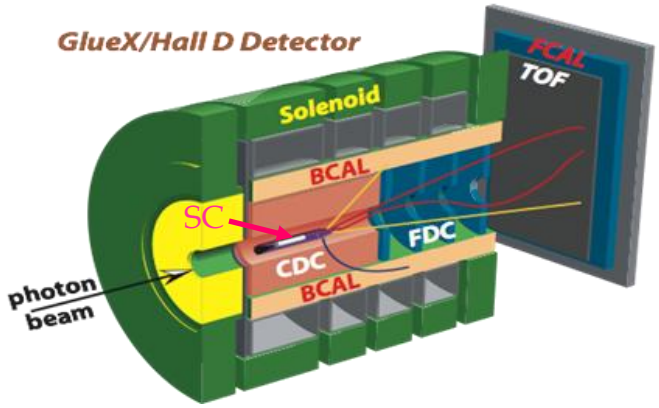
DAQ Requirement of SoLID-SIDIS

- High Luminosity: 10^{36} cm^{-2} s^{-1}
- Record coincident $^{3}He(e, e'h)X$ events



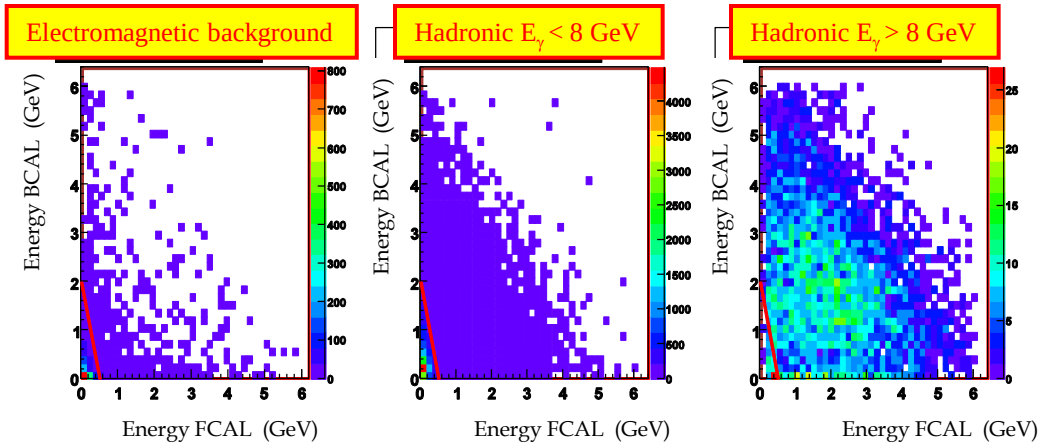
Hall D L1 Trigger-DAQ Rate

- Low luminosity (10^7 γ/s in $8.4 < E_\gamma < 9.0$ GeV)
  - 20 kHz L1
- High luminosity (10^8 γ/s in $8.4 < E_\gamma < 9.0$ GeV)
  - 200 kHz L1
  - Reduced to 20 kHz L3 by online farm
- Event size: 15 kB; Rate to disk: 3 GB/s



Detectors which can be used in the Level-1 trigger:

Forward Calorimeter (FCAL)	Energy
Barrel Calorimeter (BCAL)	Energy
Start Counter (SC)	Hits
Time of Flight (TOF)	Hits
Photon Tagger	Hits

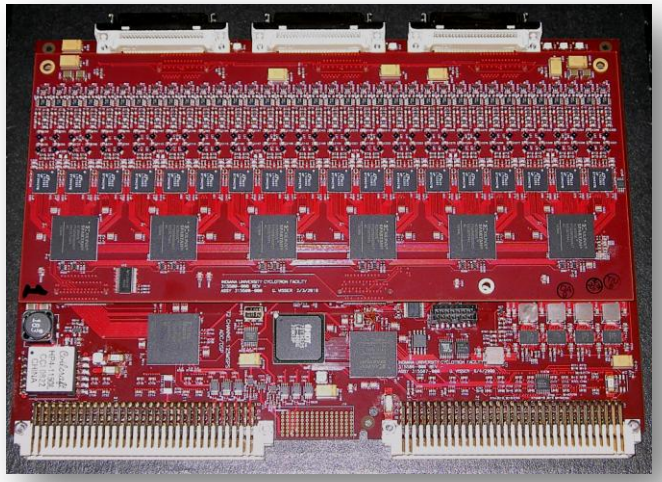


Basic Trigger Requirement:

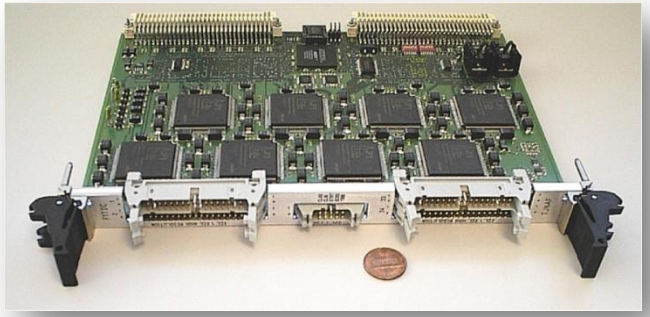
$$E_{BCAL} + 4 \cdot E_{FCAL} > 2 \text{ GeV}$$
and a hit in Start Counter

Custom Electronics for JLab

- VME Switched Serial (VXS) backplate
  - 10 Gbps to switch module (J_0)
  - 320 MB/s VME-2eSST (J_1/J_2)
- All payload modules are fully pipelined
  - **FADC125** (12 bit, 72 ch)
  - **FADC250** (12 bit, 16 ch)
  - **F1-TDC** (60 ps, 32 ch or 115 ps, 48 ch)
- Trigger Related Modules
  - **C**rate **T**rigger **P**rocessor (**CTP**)
  - **S**ub-**S**ystem **P**rocessor (**SSP**)
  - **G**lobal **T**rigger **P**rocessor (**GTP**)
  - **T**rigger **S**upervisor (**TS**)
  - **T**rigger **I**nterface/Distribution(**TI/D**)
  - **S**ignal **D**istribution (**SD**)

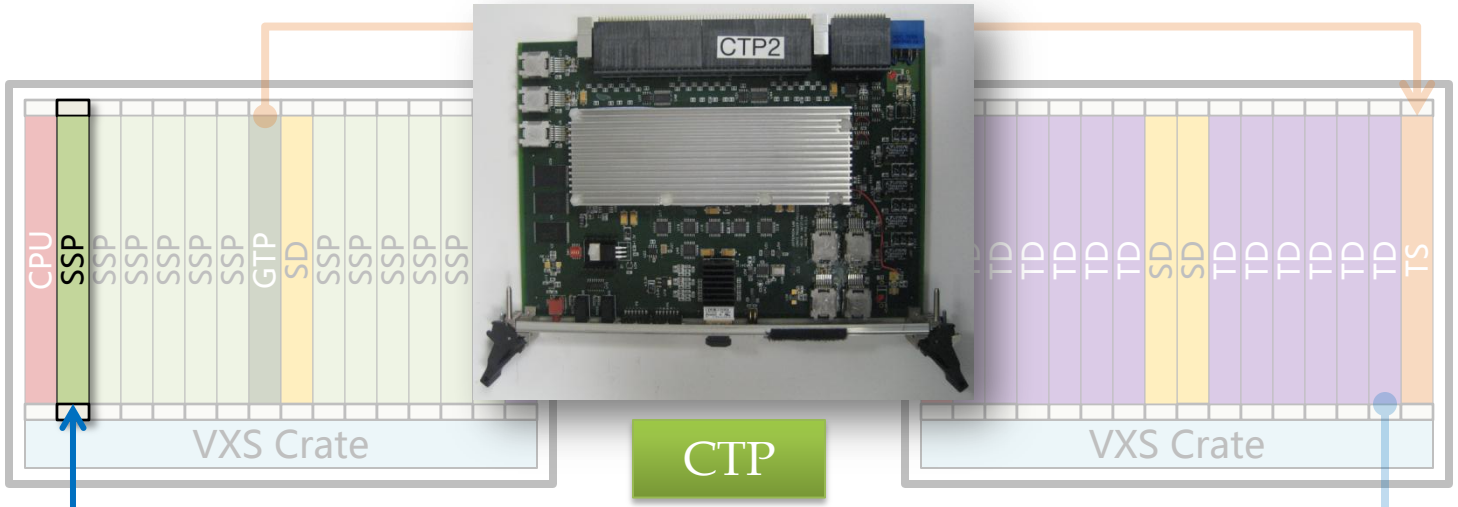


FADC125



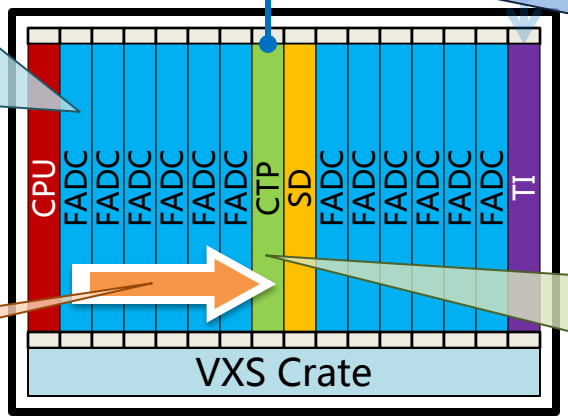
F1-TDC

L1 Trigger Diagram



FADC250
- 12 bit @ 250 MHz, 16 ch
- Sums amplitude from all channels
- Transfer total energy or hit pattern to CTP

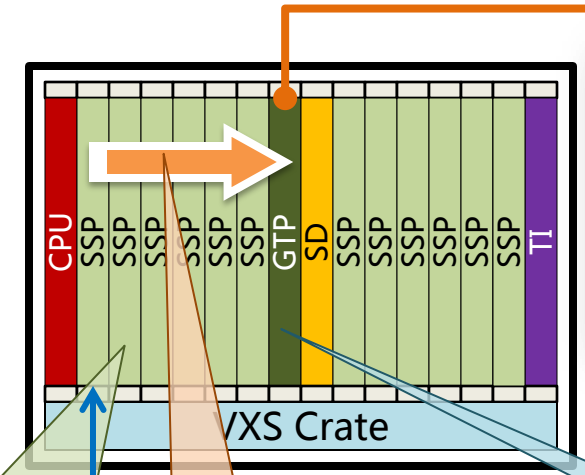
Fiber Optics
- 64 bit @ 125 MHz



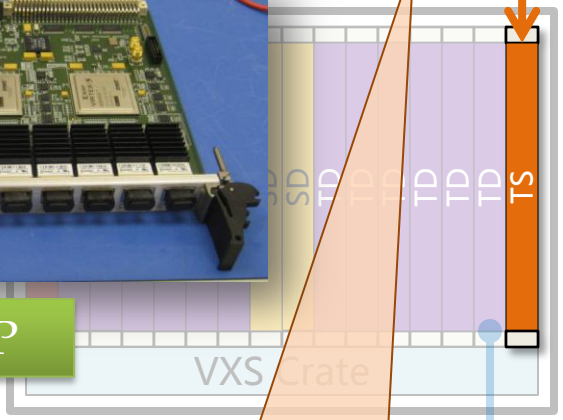
VXS Serial Link
- 16 bit @ 250 MHz: 4 Gbps

Crate Trigger Processor
- Sums energies from FADCs
- Transfer total energy or hit pattern to SSP

L1 Trigger Diagram

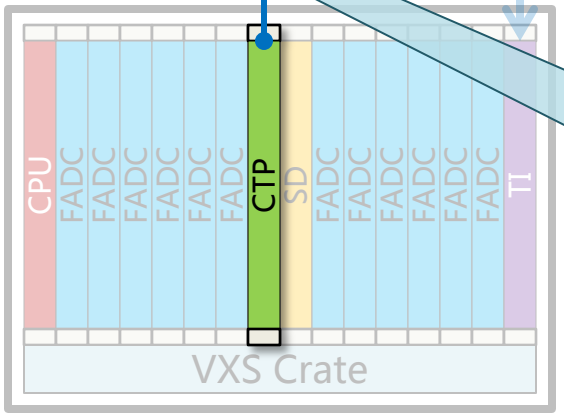


SSP



Sub-System Processor
- Consolidates multiple crate subsystems
- Report total energy or hit pattern to GTP

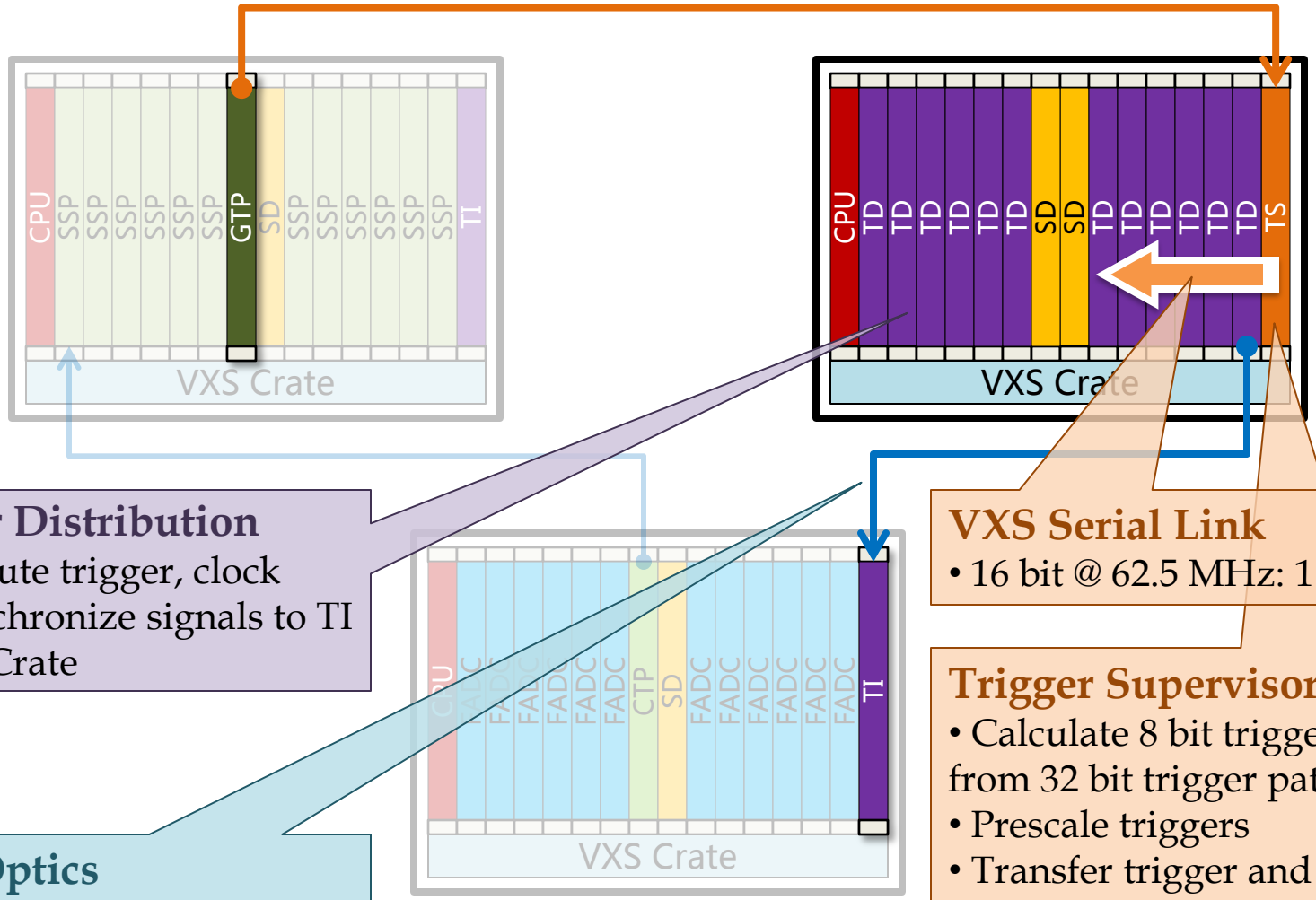
Copper Ribbon Cable
- 32 bit @ 250 MHz: 8 Gbps



Global Trigger Processor
- Collect L1 data from SSPs
- Calculate trigger equations
- Transfer 32 bit trigger pattern to TS

VXS Serial Link
- 32 bit @ 250 MHz: 8 Gbps

L1 Trigger Diagram



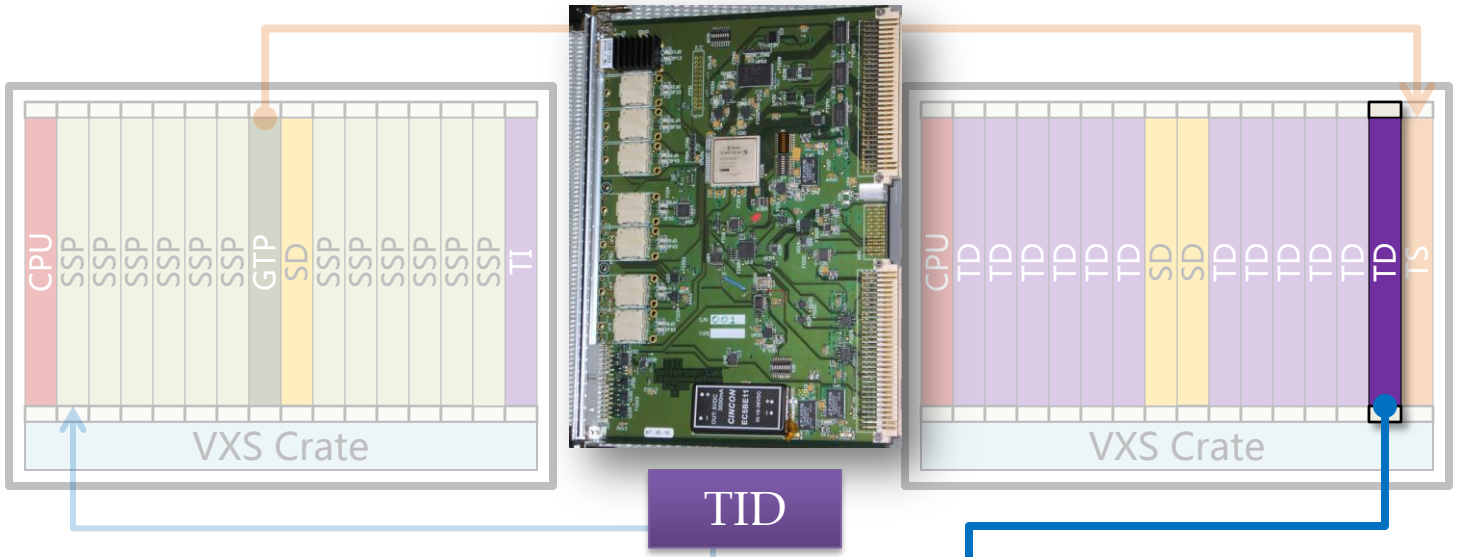
Trigger Distribution
- Distribute trigger, clock and synchronize signals to TI in each Crate

Fiber Optics
- 16 bit @ 62.5 MHz: 1 Gbps

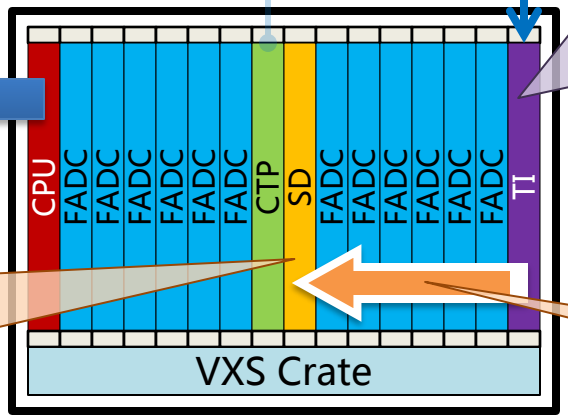
VXS Serial Link
- 16 bit @ 62.5 MHz: 1 Gbps

Trigger Supervisor
- Calculate 8 bit trigger types from 32 bit trigger pattern
- Prescale triggers
- Transfer trigger and sync signal to TD (16 bit total)

L1 Trigger Diagram



VME Readout Controller
- Gigabit ethernet

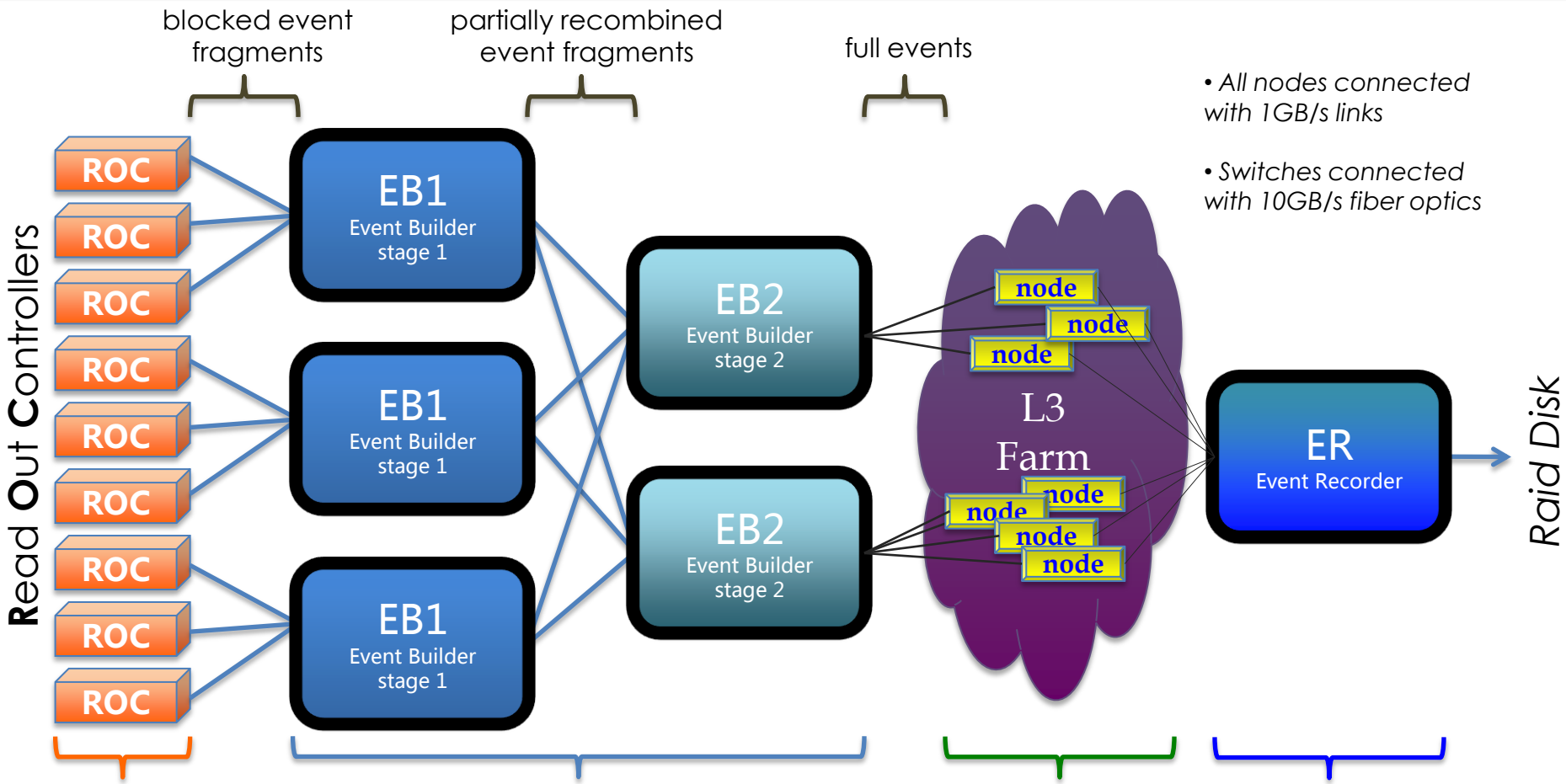


Trigger Interface
- Receive trigger, clock and sync signals from TD
- Make crate trigger decision
- Pass signals to SD

Signal Distribution
- Distribute common signals to all modules: busy, sync and trigger 1/2

VXS Serial Link
- 4 bit @ 250 MHz: 1 Gbps

L3 Farm


blocked event fragments
partially recombined event fragments
full events
• All nodes connected with 1GB/s links
• Switches connected with 10GB/s fiber optics
Read Out Controllers
ROC
ROC
ROC
ROC
ROC
ROC
ROC
ROC
ROC
EB1
Event Builder stage 1
EB1
Event Builder stage 1
EB1
Event Builder stage 1
EB2
Event Builder stage 2
EB2
Event Builder stage 2
node
node
node
L3 Farm
node
node
node
node
ER
Event Recorder
Raid Disk
Front-End Crates
~60 crates
~50MB/s out per crate
Staged Event Building
N x M array of nodes (exact number to be determined by available hardware at time of purchase)
Level-3 Trigger and monitoring
Event Recording
300MB/s in
300MB/s out

SoLID SIDIS Detector Rates

- In 50 ns windows, 11 GeV

Detector	Rate	Hits	Type	Data Size per hit
GEM	4.4 GHz	220	Hits (time)	4 Byte x 2 (X/Y)
LC	120 kHz	1	Energy, Hits	8 Byte x 2 (PS/SH)
FC	200 MHz	10	Energy, Hits	8 Byte x 2 (PS/SH)
LGC	40 MHz	3	Energy, Hits	8 Byte x 2 (split)
HGC	60 MHz	4	Energy, Hits	8 Byte x 2 (split)
MRPC	850 MHz	45	Hits	4 Byte
SC	300 MHz	15	Energy, Hits	8 Byte
Total				2.5 kB

With header and other over head
event size is ~ **4 kB**

L1 Trigger

- Electron Singles Trigger:
  - LC > 400 MeV | | (FC > 400 MeV && LGC)

$$T_L^e\,|_{11(8.8)GeV} = Y_L^e + Y_L^\gamma + \frac{Y_L^h}{R_{LC}} = 11 + 52 + \frac{56}{20} = 66(55)kHz$$

$$T_F^e\,|_{11(8.8)GeV} = Y_F^e + \frac{Y_F^\gamma}{R_{LGC}} + \frac{Y_F^h}{R_{LGC}\cdot R_{FC}} = 89 + \frac{620}{40} + \frac{6100}{40\cdot 10} = 120(180)kHz$$

  - Total event rate: 190 - 240 kHz
  - Frontend data rate: 800 – 1000 MB/s
  - ROCs can barely handle this rate
    - Assuming 10 VME crates, 100 MB/s per ROC
    - add more crates since PVDIS uses > 30
  - Maybe a little bit too much to write to the tape
  - Not much room for improvement, already very close to electron yield.

Reduce L1 Trigger: Two Options

- Make coincidence with another charged particle in Forward detector
  - FC > 200 MeV && MRPC && Scintillator

$$T_F^h\big|_{11(8.8)GeV} = Y_F^h + Y_F^e + \frac{Y_F^{\gamma all}}{R_{MRPC}\cdot R_S} = 6 + 0.1 + \frac{200}{20\cdot 6.5} = 7.7(6.9)MHz$$

  - Coincidence rate with 35 ns window ~ 50 kHz
- Use L3 farm
  - With powerful parallelism computing, we can easily reduce the rate by a factor of 5
  - Reduce the difficulty to put MRPC (customized VME board) into the trigger logic
- Both options give 200 MB/s data rate to the tape

Estimated Channels

Detector	Total Channel	Front End Module	Number of Modules
GEM	300 k ?	Customized VME	?
LC	180	FADC250/F1-ADC	12/6
FC	360	FADC250/F1-ADC	23/12
LGC	30	FADC250	2
HGC	30	FADC250	2
MRPC	3000	Customized VME	?
SC	30	FADC250/F1-ADC	2/1

Cost Estimation

Module Name	Unit Price	# of Modules	Total Cost
FADC250	$ 4,000	41	$ 164,000
FADC125	$ 4,000		
F1-TDC	$ 4,000	19	$ 76,000
CTP	$ 5,000	6 + ?? (4)	$ 30,000 + ??
SSP	$ 5,000	1 + ? (1)	$ 5,000 + ?
GTP	$ 5,000	1	$ 5,000
TS	$ 5,000	1	$ 5,000
TID	$ 3,000	10 + ?? (4)	$ 30,000 + ??
SD	$ 2,500	8 + ?? (4)	$ 20,000 + ??
VXS Crate	$ 8,000	8 + ?? (4)	$ 64,000 + ??
Total			$ 401,000 + ??? ($ 79,000)

To Do List

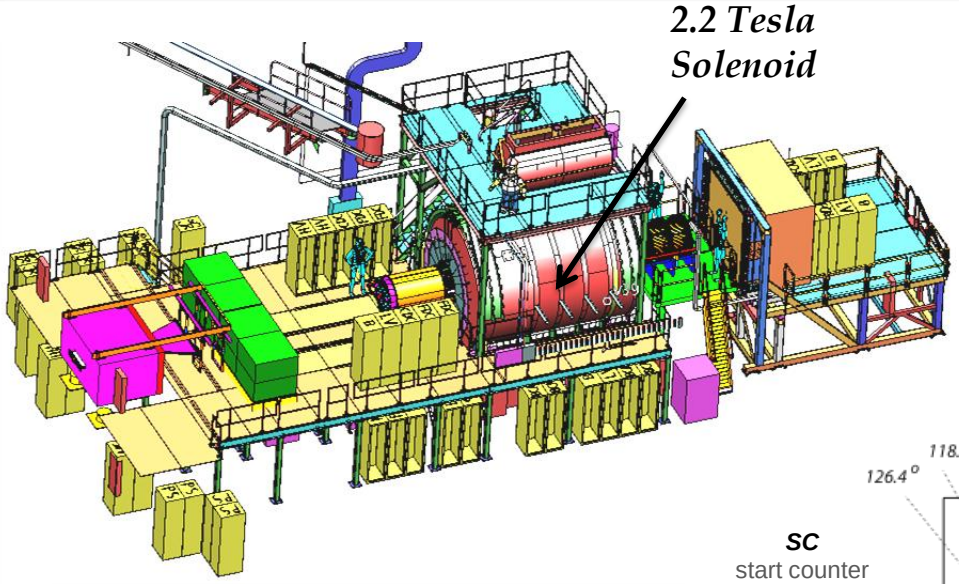
- Final VXS pair mapping has ben established, some collaborations already started their customized VXS payload modules based on it (e.g. GEM tracker of Super BigBite). We'd better start the same approach as well if we plan to use Jlab customized trigger system.

- Optimize detector granularity, estimate number of channels of each detector.

- Work with electronics and DAQ groups to acquire necessary support and hardware.

Backup Slides

The GlueX Detector

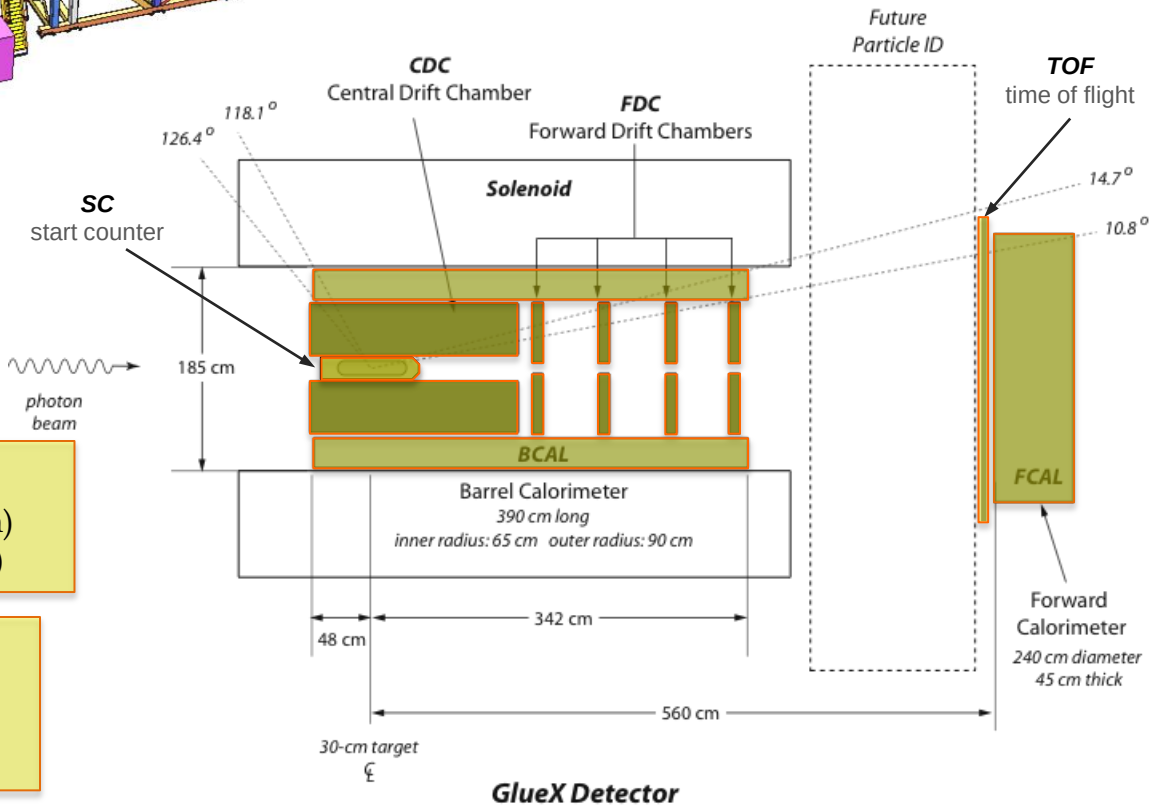


- 2.2T superconducting solenoidal magnet
- Fixed target (LH_2)
- 10^8 tagged γ/s (8.4-9.0GeV)
- hermetic

Charged particle tracking
- Central drift chamber (straw tube)
- Forward drift chamber (cathode strip)

Calorimetry
- Barrel Calorimeter (lead, fiber sandwich)
- Forward Calorimeter (lead-glass blocks)

PID
- Time of Flight wall (scintillators)
- Start counter
- Barrel Calorimeter

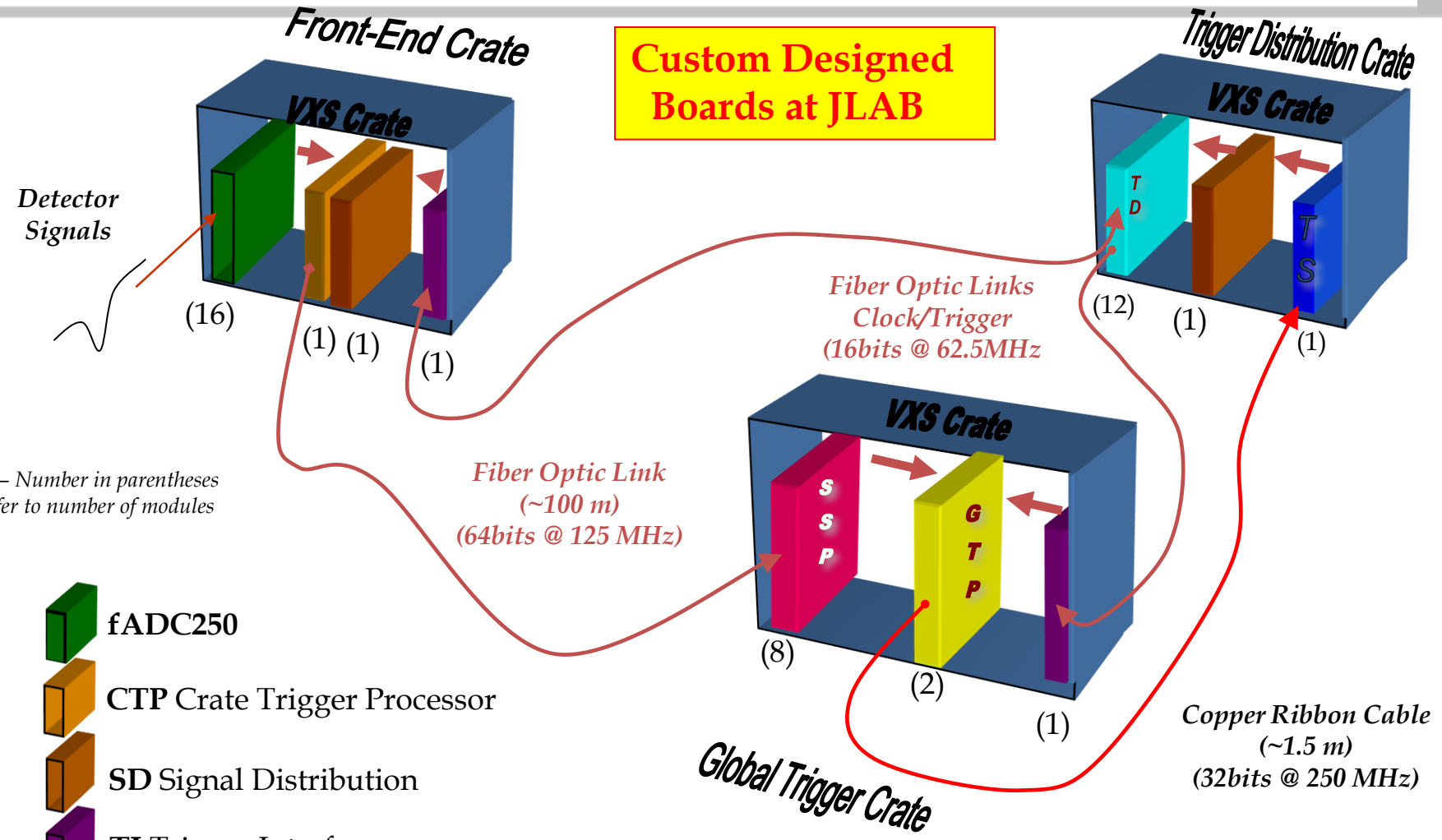


GlueX Data Rate

		Front End DAQ Rate	Event Size	L1 Trigger Rate	Bandwidth to mass Storage	
JLab	GlueX	3 GB/s	15 kB	200 kHz	300 MB/s	priva comm.
	CLAS12	0.1 GB/s	20 kB	10 kHz	100 MB/s	
LHC	ALICE	500 GB/s	2,500 kB	200 kHz	200 MB/s	CHEP2007 talk Sylvain Chapelin
	ATLAS	113 GB/s	1,500 kB	75 kHz	300 MB/s	
	CMS	200 GB/s	1,000 kB	100 kHz	100 MB/s	
	LHCb	40 GB/s	40 kB	1000 kHz	100 MB/s	
BNL	STAR	50 GB/s	1,000 kB	0.6 kHz	450 MB/s	*
	PHENIX	0.9 GB/s	~60 kB	~ 15 kHz	450 MB/s	**

* Jeff Landgraf Private Comm. 2/11/2010
** CHEP2006 talk MartinL. Purschke

Level-1 Trigger Electronics



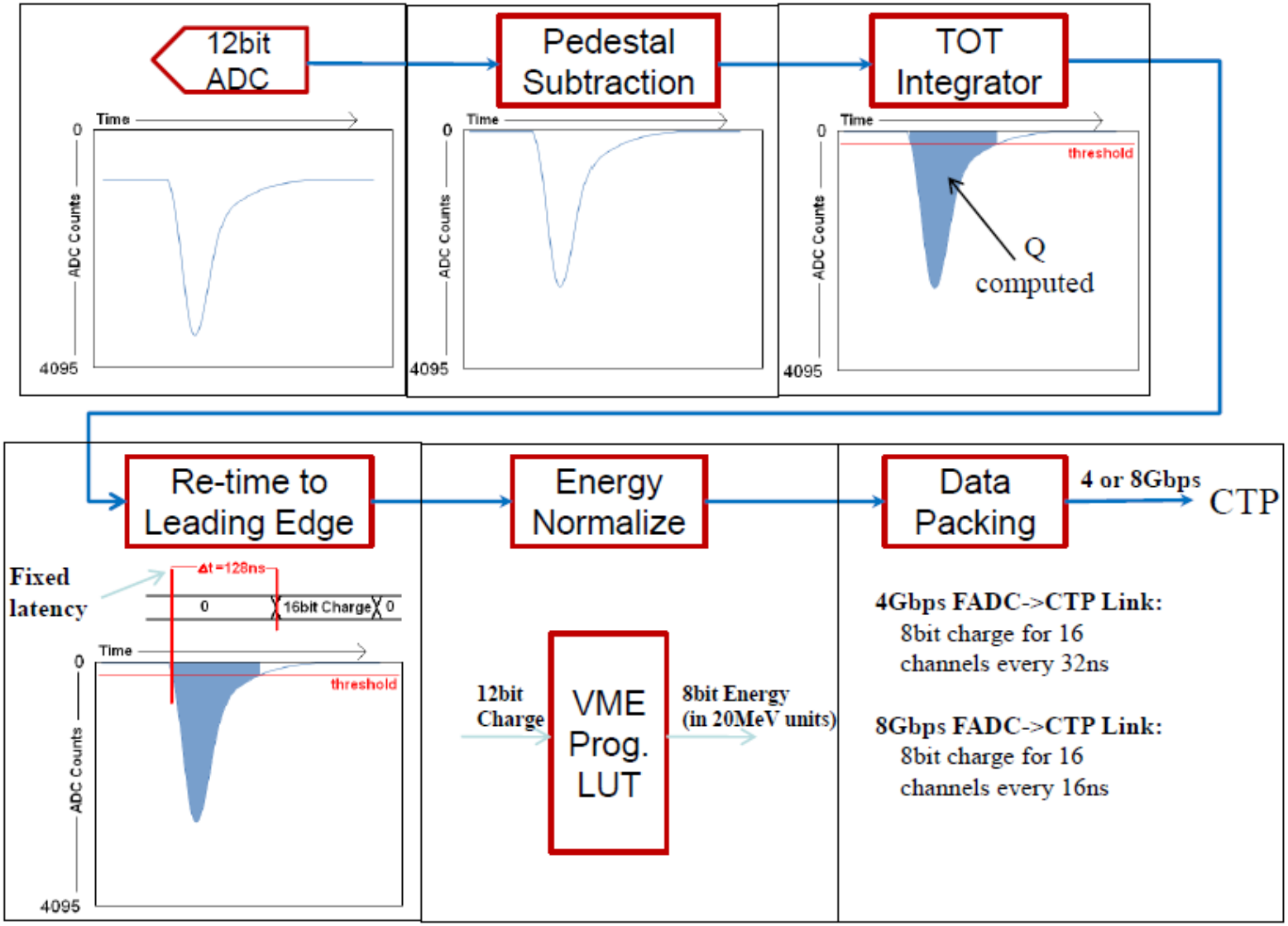
Pipelined detector readout electronics:
fADC and F1TDC

- Trigger Latency ~ 3 μs
(F1TDC pipeline ~3.9 μs)

CODA3 – What's different

CODA 2.5	CODA 3
Run Control (X, Motif, C++) (rcServer, runcontrol)	Experiment Control – AFECS (pure JAVA) (rcPlatform, rcgui)
Communication/Database (msql, cdev, dptcl, CMLOG)	cMsg – CODA Publish/Subscribe messaging
Event I/O C-based simple API (open/close read/write)	EVIO – JAVA/C++/C APIs Tools for creating data objects, serializing, etc…
Event Builder / ET System / Event Recorder (single build stream)	EMU (Event Management Unit) Parallel/Staged event building
Front-End – vxWorks ROC (Interrupt driven – event by event readout)	Linux ROC, Multithreaded (polling – event blocking)
Triggering: 32 ROC limit, (12 trigger bits -> 16 types) TS required for buffered mode	128 ROC limit, (32 trigger bits -> 256 types) TI supports TS functionality. Timestamping (4ns)

FADC Encoding Example



GTP Trigger Bit Example