SoLID DAQ for Transversity and PVDIS

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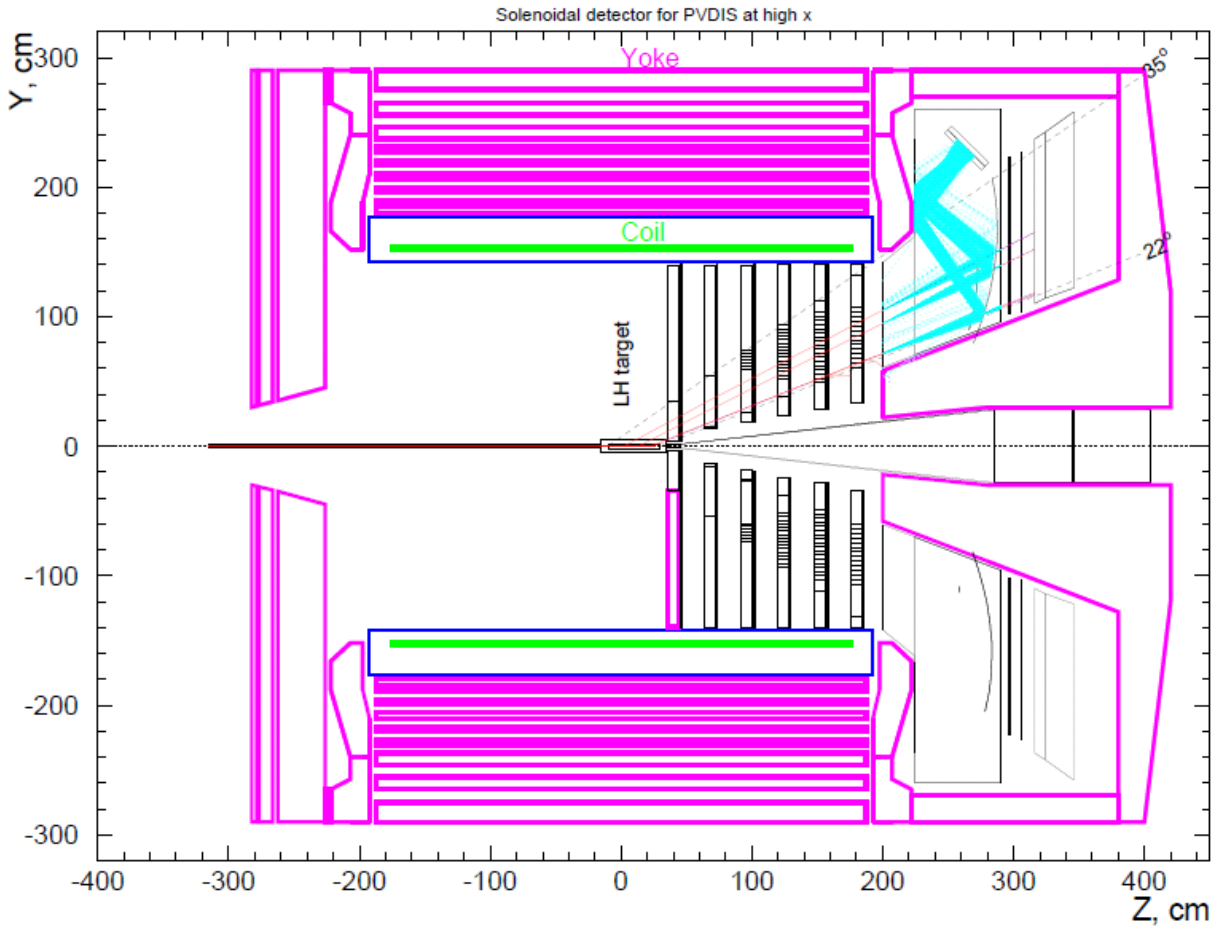
Yi Qiang

Detector layout and trigger for PVDIS



Trigger

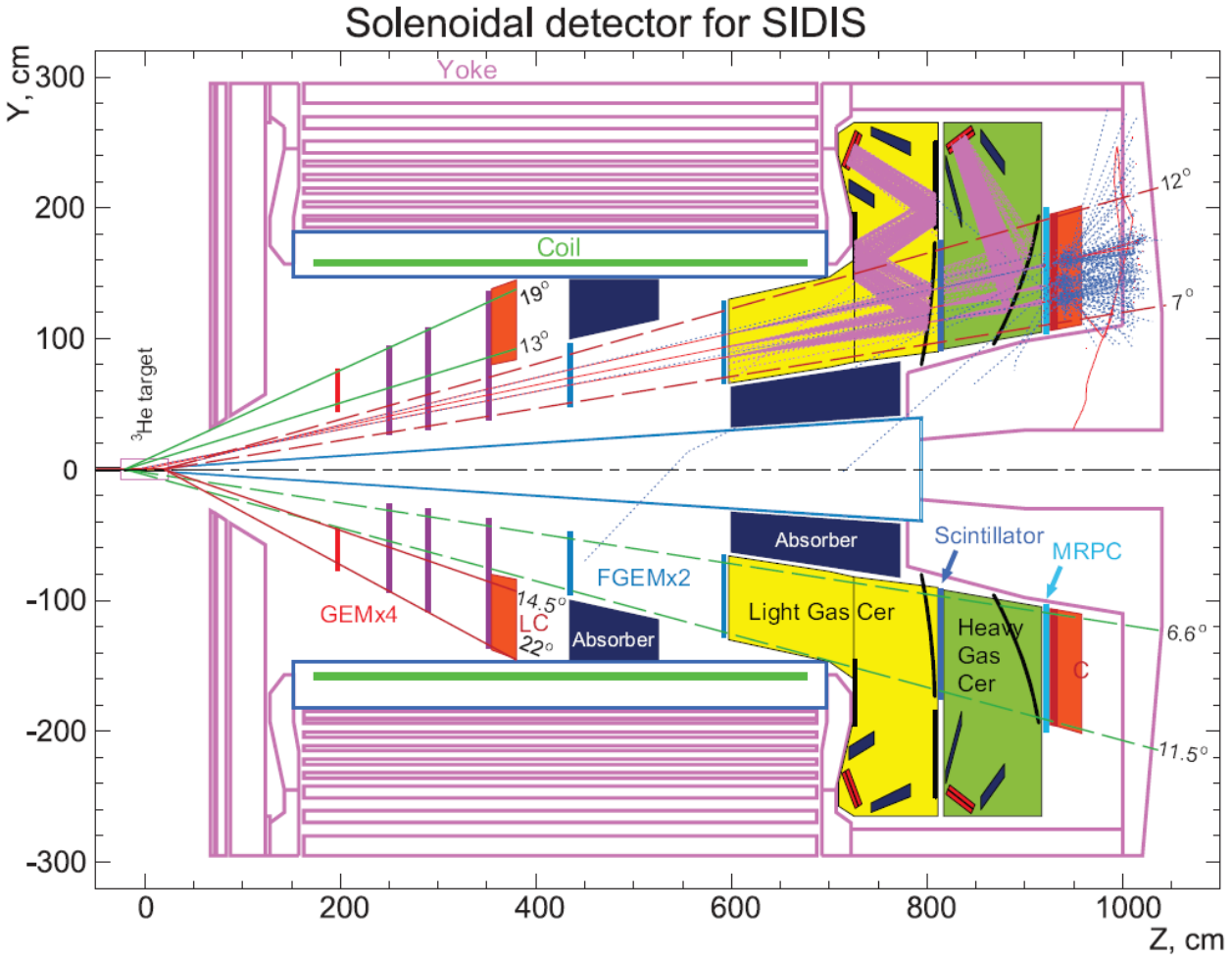
Calorimeter
+
Cerenkov

200 to 500 KHz of electrons

30 individual sectors

Max 17 KHz/sector

Detector layout and trigger for SIDIS



Trigger

Calorimeter
+
Cerenkov
+
MRPC

30 sectors
Combined
in
10 regions of
interests
Max rate 300 KHz
10 KHz/sector

GEM readout

- APV25 + VME module based
- Up to 164 000 channels
- APV 25 : 128 channels
- VME readout : 4 APV25 = 512 channels

- 1 separate VXS crate for GEM readout

- 2 crates per sectors for FADC and GEM

SoLID SIDIS Detector Rates

Detector	Rate	Hits	Type	Data Size per hit
GEM	4.4 GHz	220	Hits (time)	4 Byte x 2 (X/Y)
LC	120 kHz	1	Energy, Hits	8 Byte x 2 (PS/SH)
FC	200 MHz	10	Energy, Hits	8 Byte x 2 (PS/SH)
LGC	40 MHz	3	Energy, Hits	8 Byte x 2 (split)
HGC	60 MHz	4	Energy, Hits	8 Byte x 2 (split)
MRPC	850 MHz	45	Hits	4 Byte
SC	300 MHz	15	Energy, Hits	8 Byte
Total				2.5 kB

With header and other over head
event size is ~ **4 kB**

Pipelined Hall D DAQ

- Virtually dead time less
- Flexibility in L1

- Data online filtering with L3 farm
- Reduce data to from 800 Mb/s to 50 Mb/s

L3 Farm

- Determine data reduction algorithm
  - Crude tracking
  - Geometrical region on interests
  - Downsampling
- Determine number of nodes needed for required performance

Flash ADC work

- PEPPO : injector positron experiment
  - 2 prototype FADC
  - 2 New Hall D FADC
  - Test pipelining
  - Goal : reach 100 KHz similar to Hall A Compton DAQ
  - Some beam maybe available in October
- Umass :
  - test setup for Hall D electronics
  - Can develop PVDIS electronics

Hall D developments

- Elliot Wollin and Vardjan
  - Cosmics test stand this fall using CODA 3 alpha
  - CODA 3 support L3 farm nodes
    - All events go through L3 when going to Event Recorder
    - Events transferred using ET between nodes
    - Nodes and process managing being worked out by Vardjan
  - CODA 3 Alpha available after Thanksgiving

JLAB electronics PVDIS

Detector	Channel	Module	Unit price	Total price sector	Total price 30 sectors
Calorimeter	84	6	4500	27000	810000
LC	9				
TID		2	3000	6000	180000
SD		2	2500	5000	150000
VXS		2	11500	23000	690000
VME CPU		2	3400	6800	204000
CTP		2	5000	10000	300000
Total price				77800	2334000

SIDIS channel count

Detector	Module type	Number of channels	Number of modules
Forward Calorimeter	FADC+TDC	1896	119
Large angle calorimeter	FADC+TDC	920	58
Light Gas Cerenkov	FADC+TDC	120	8
Heavy Gas Cerenkov	FADC+TDC	270	17
Scintillator	FADC+TDC	120	8

PVDIS+SIDIS electronics required

	Module	Unit price	Number of modules	Price
	FADC 250	4500	210	945000
High Res timing	F1	4000	105	420000
High Res timing	Discriminator	2500	122	525000
High Res timing	VME crate	5000	11	55000
	CTP	5000	60	300000
	SSP	5000	8	40000
	VXS crate	11500	1	11500
	GTP	5000	1	5000
	VXS crate	11500	1	11500
	TS	3500	1	3500
	TID	3000	60	180000
	SD	2500	60	150000
	VXS crate	11500	60	690000
	VME CPU	3400	73	248200
	L3 farm node	5000	12	60000
			Total detectors	3644700

Time line

- 2011
  - Hall A computer upgrade
  - FADC tests
  - Intel VME CPU test : reach 10 KHz rate with fastbus for g2p
- 2012
  - GEM + APV25 GEM tests during g2p
  - FADC tests (achieve 100 KHz trigger rate for Compton for PEPPO)
  - HCAL Trigger development
  - 4 JLAB FADC250
- 2013
  - Small scale setup for testing : FADC + trigger + fastbus + APV25
- 2014
  - A1n :
    - Full scale test of GEM
    - Digital Trigger electronics test parasitic
- 2015
  - Full scale system

Conclusion

- SoLID requires high rate capability and advanced trigger capability
- SoLID benefits from Hall D development
  - Trigger using FADC
  - L3 farm
- Electronics and performance to be tested in the next few years
- SoLID electronics for both experiment around 4 M$

Backup slides

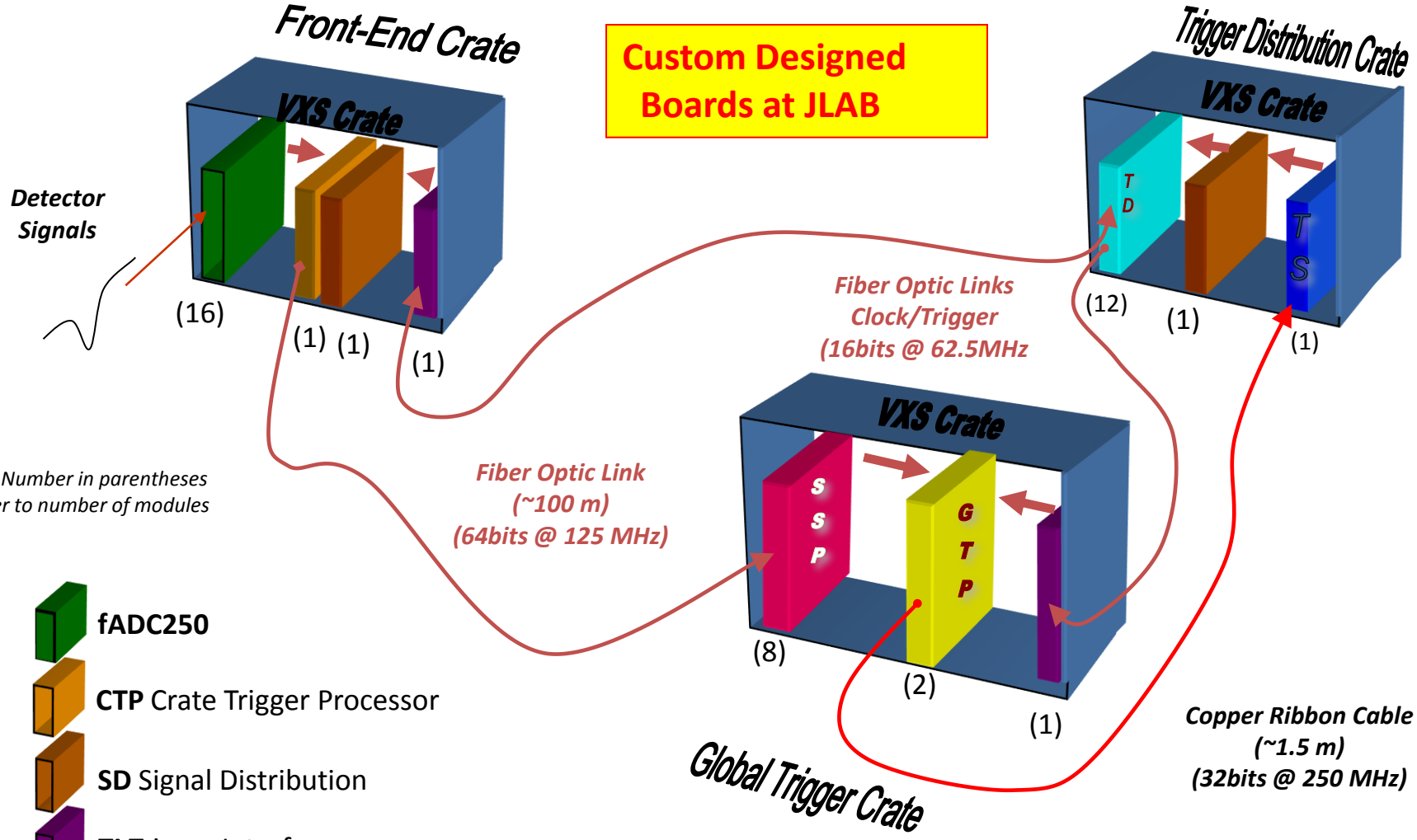
SIDIS channel count

Detector	Module type	Number of channels	Number of modules
Forward Calorimeter	FADC+TDC	1896	119
Large angle calorimeter	FADC+TDC	920	58
Light Gas Cerenkov	FADC+TDC	120	8
Heavy Gas Cerenkov	FADC+TDC	270	17
Scintillator	FADC+TDC	120	8
GEM	VME	164K	321

JLAB electronics PVDIS

Detector	Channel	Module	Unit price	Total price sector	Total price 30 sectors
Calorimeter	84	6	4500	27000	810000
LC	9				
GEM	4700	10	5000	50000	1500000
TID		2	3000	6000	180000
SD		2	2500	5000	150000
VXS		2	11500	23000	690000
VME CPU		2	3400	6800	204000
CTP		2	5000	10000	300000
Total price				127800	3834000

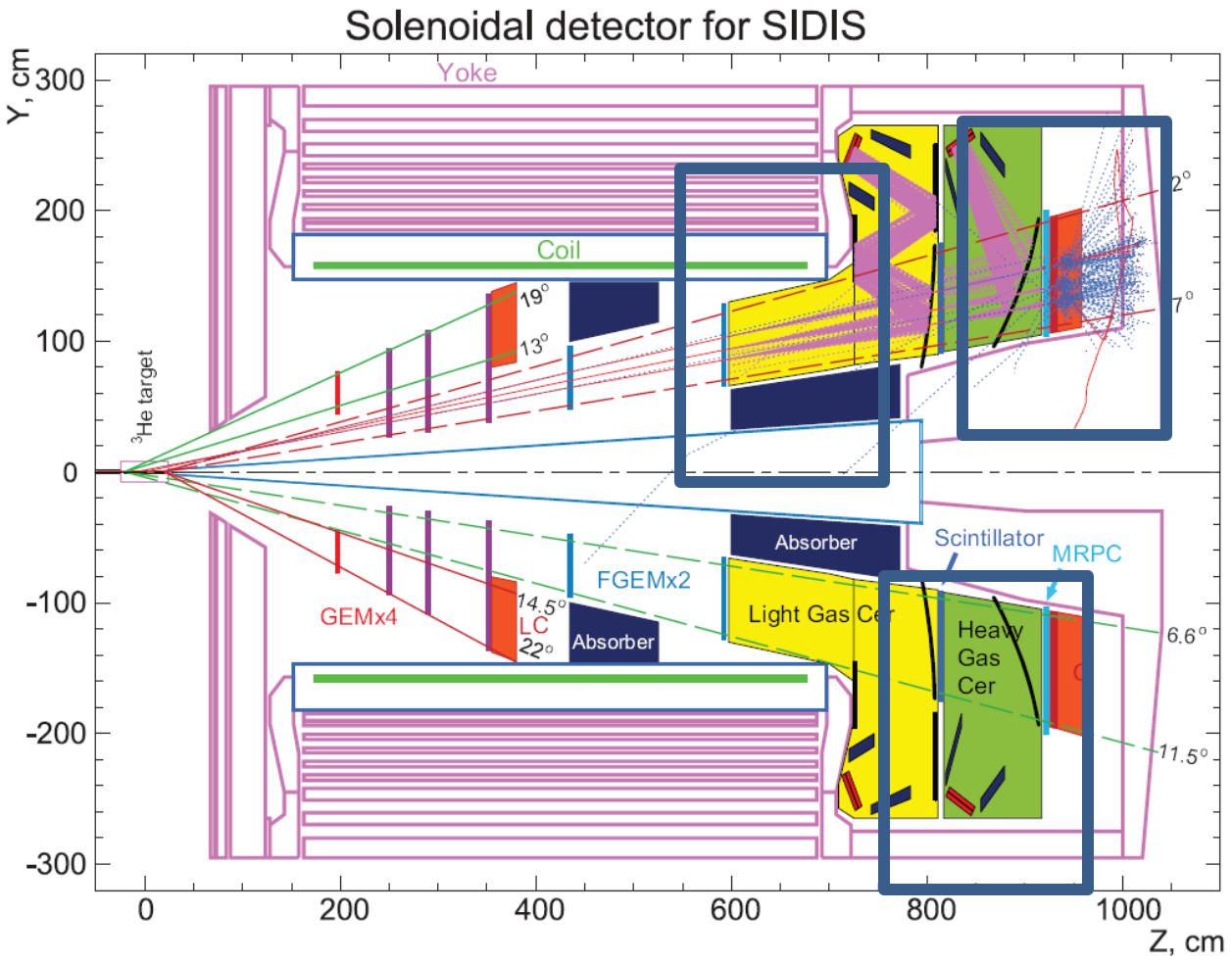
Level-1 Trigger Electronics



Pipelined detector readout electronics:
fADC and F1TDC

- Trigger Latency ~ 3 µs
(F1TDC pipeline ~3.9 µs)

Detector layout and trigger for SIDIS

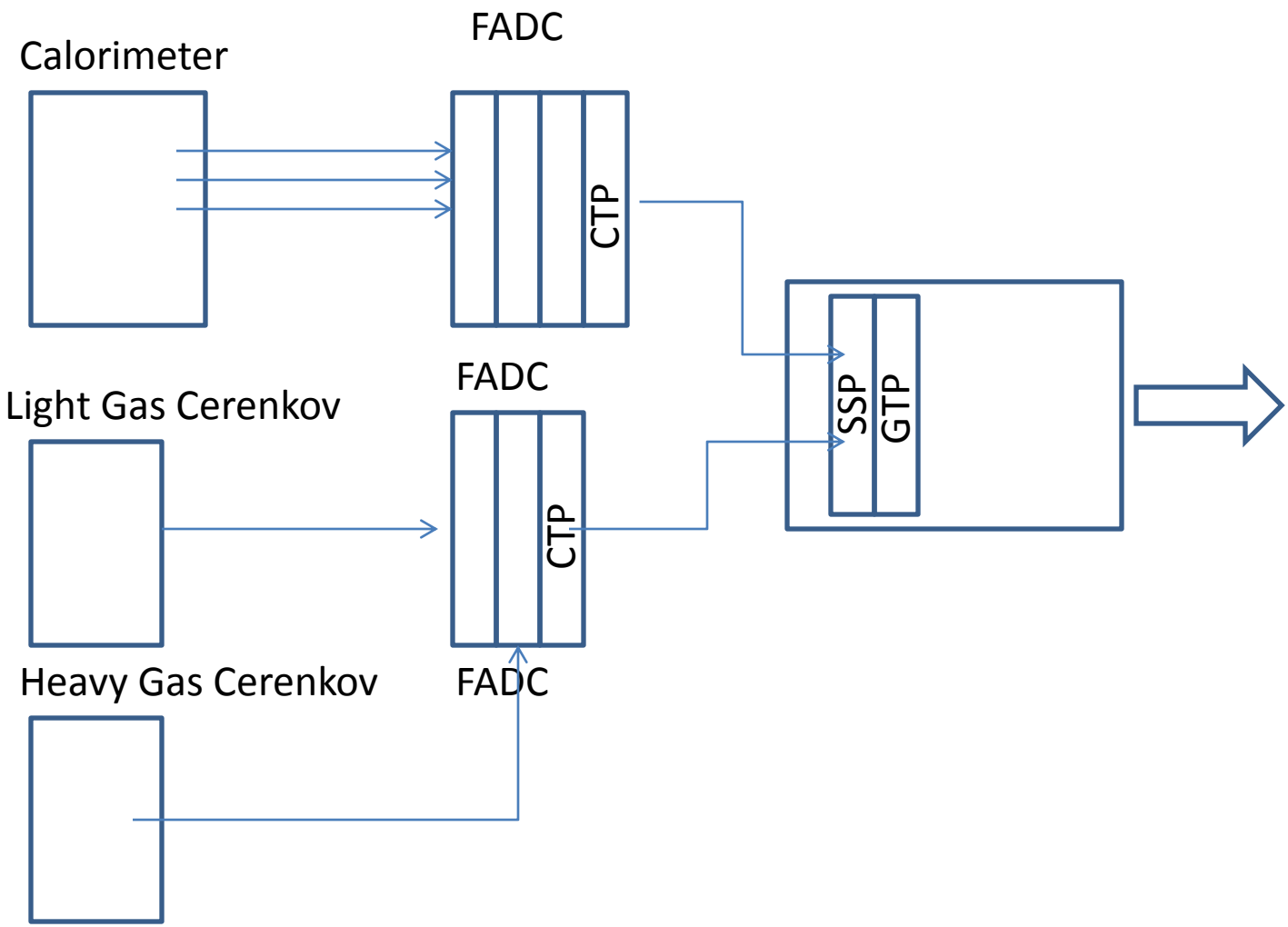


Trigger

Calorimeter
+
Cerenkov
+
MRPC

30 sectors combine

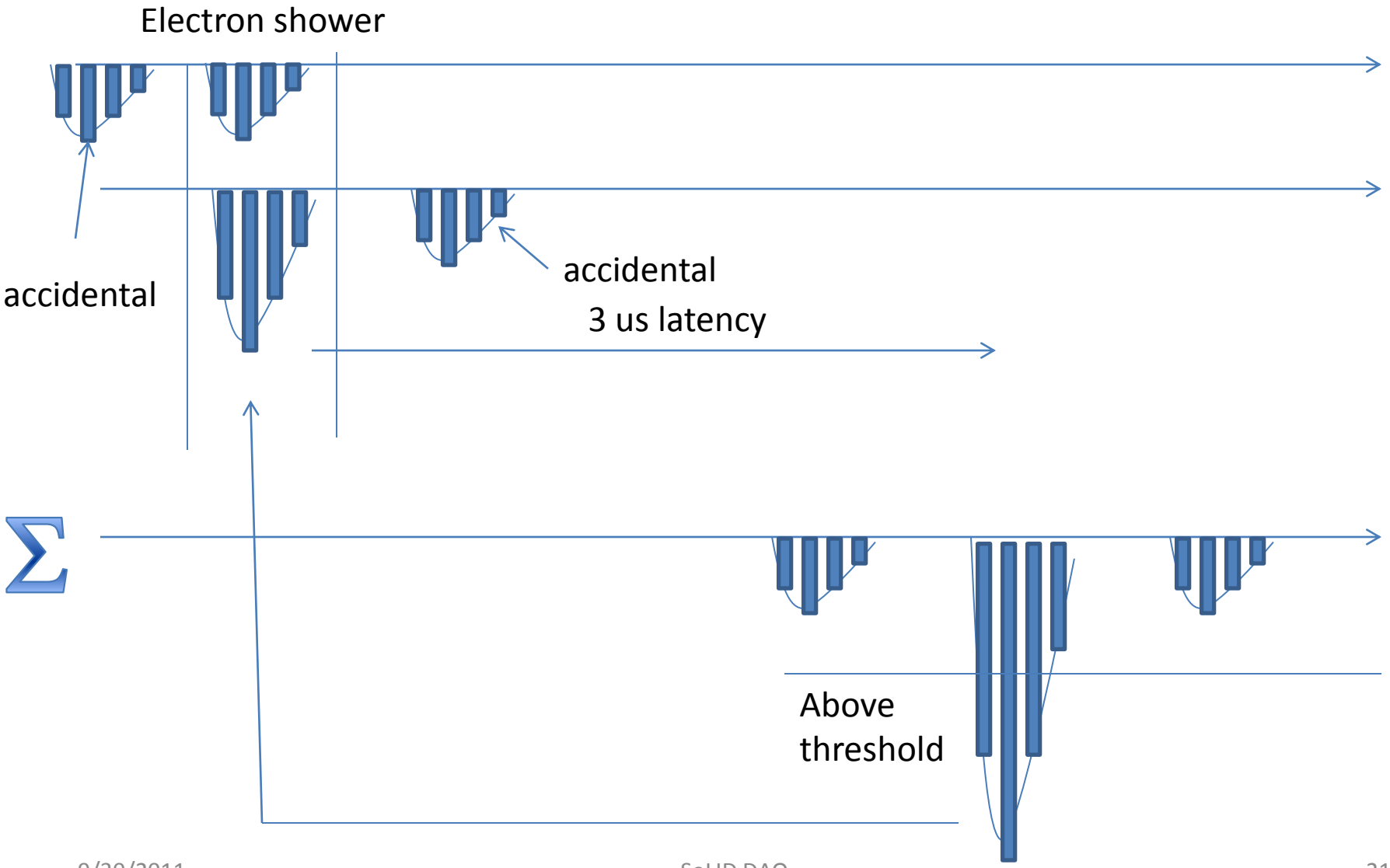
Pipelined Hall D DAQ



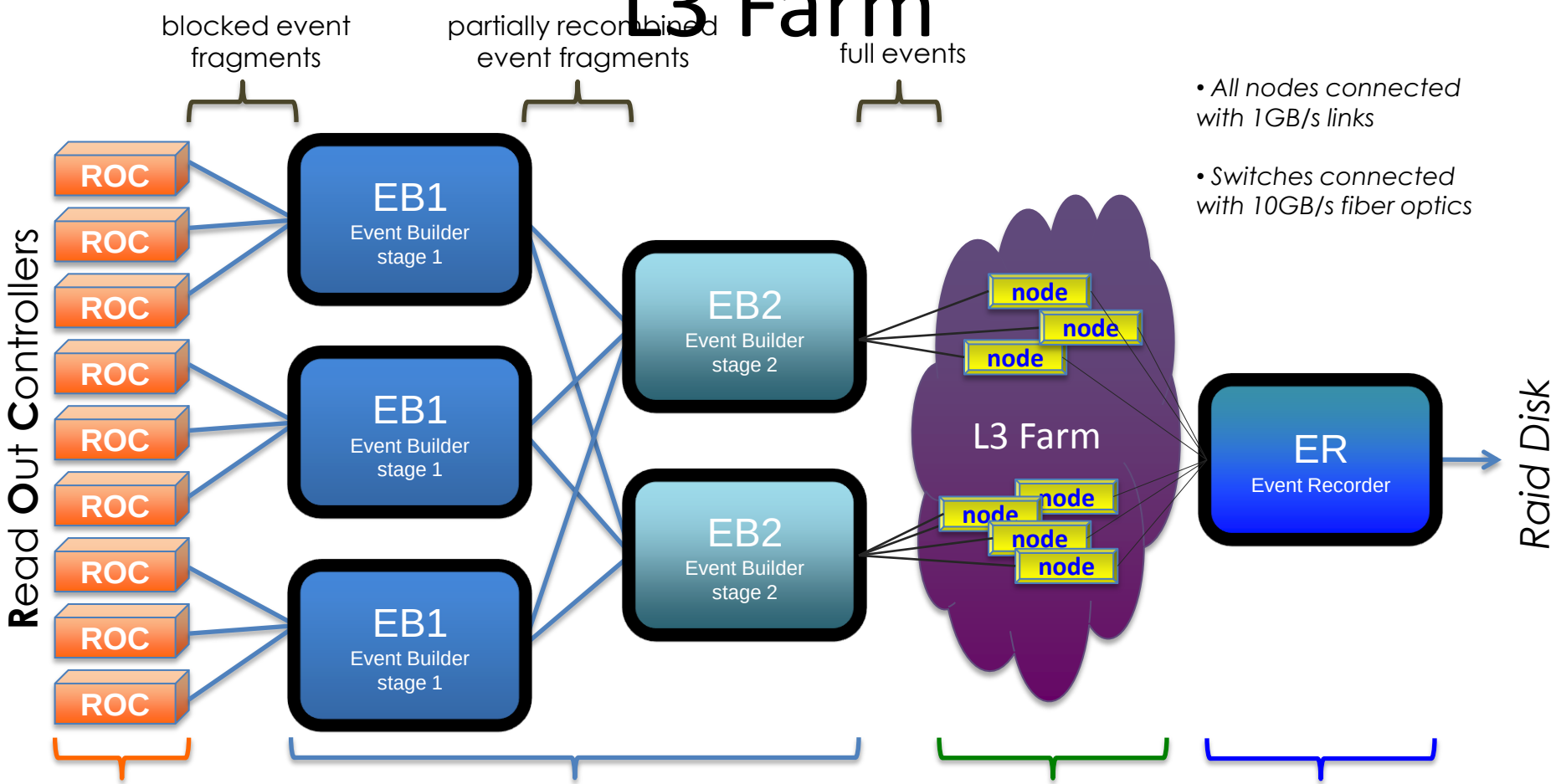
L1 trigger

Calorimeter
+
Cerenkov
+
Pion
In
3 us

Pipelined Hall D DAQ

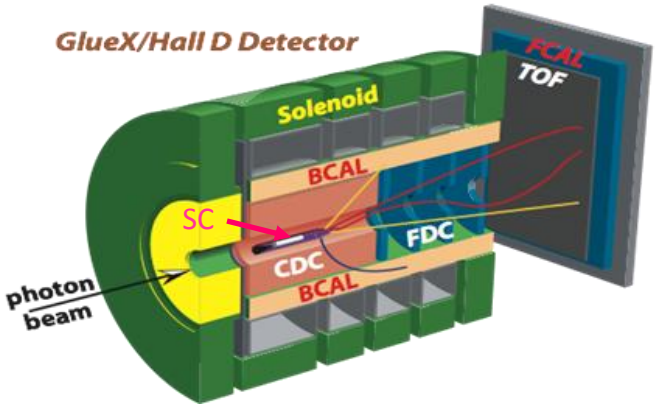


L3 Farm


blocked event fragments
partially recombined event fragments
full events
• All nodes connected with 1GB/s links
• Switches connected with 10GB/s fiber optics
Read Out Controllers
ROC
ROC
ROC
ROC
ROC
ROC
ROC
ROC
ROC
EB1
Event Builder stage 1
EB1
Event Builder stage 1
EB1
Event Builder stage 1
EB2
Event Builder stage 2
EB2
Event Builder stage 2
node
node
node
L3 Farm
node
node
node
node
ER
Event Recorder
Raid Disk
Front-End Crates
~60 crates
~50MB/s out per crate
Staged Event Building
N x M array of nodes (exact number to be determined by available hardware at time of purchase)
Level-3 Trigger and monitoring
Event Recording
300MB/s in
300MB/s out

Hall D L1 Trigger-DAQ Rate

- Low luminosity (10^7 γ/s in $8.4 < E_\gamma < 9.0$ GeV)
  - 20 kHz L1
- High luminosity (10^8 γ/s in $8.4 < E_\gamma < 9.0$ GeV)
  - 200 kHz L1
  - Reduced to 20 kHz L3 by online farm
- Event size: 15 kB; Rate to disk: 3 GB/s

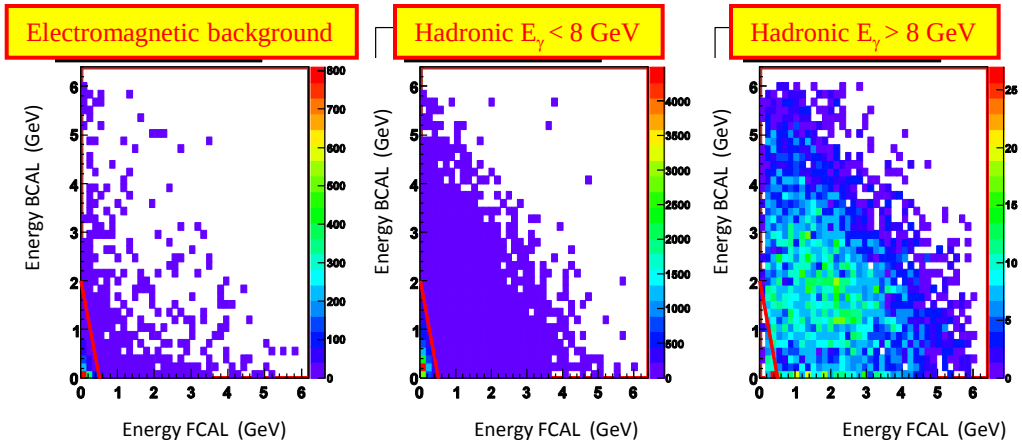


Detectors which can be used in the Level-1 trigger:

Forward Calorimeter (FCAL)	Energy
Barrel Calorimeter (BCAL)	Energy
Start Counter (SC)	Hits
Time of Flight (TOF)	Hits
Photon Tagger	Hits

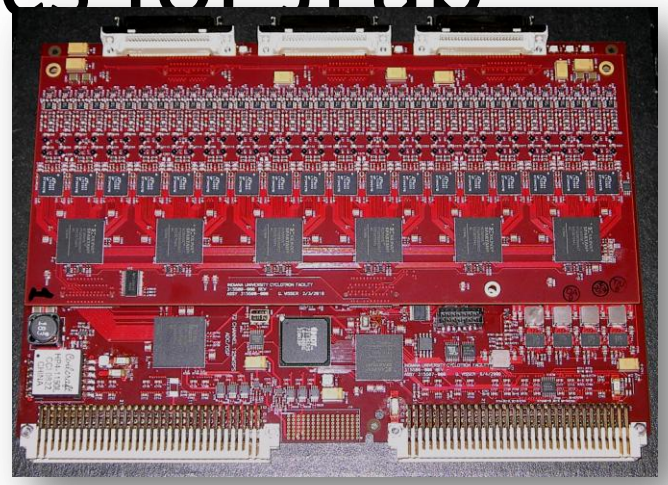
Basic Trigger Requirement:

$$E_{BCAL} + 4 \cdot E_{FCAL} > 2 \text{ GeV}$$
and a hit in Start Counter

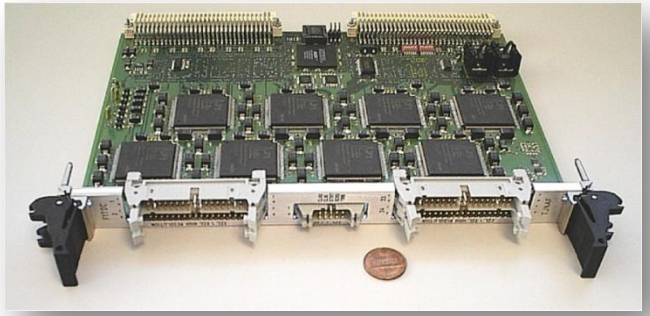


Custom Electronics for JLab

- VME Switched Serial (VXS) backplate
  - 10 Gbps to switch module (J_0)
  - 320 MB/s VME-2eSST (J_1/J_2)
- All payload modules are fully pipelined
  - **FADC125** (12 bit, 72 ch)
  - **FADC250** (12 bit, 16 ch)
  - **F1-TDC** (60 ps, 32 ch or 115 ps, 48 ch)
- Trigger Related Modules
  - **C**rate **T**rigger **P**rocessor (**CTP**)
  - **S**ub-**S**ystem **P**rocessor (**SSP**)
  - **G**lobal **T**rigger **P**rocessor (**GTP**)
  - **T**rigger **S**upervisor (**TS**)
  - **T**rigger **I**nterface/Distribution(**TI/D**)
  - **S**ignal **D**istribution (**SD**)



FADC125

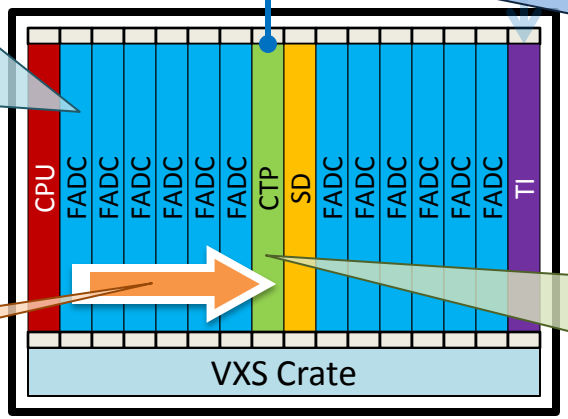


F1-TDC

L1 Trigger Diagram

FADC250
- 12 bit @ 250 MHz, 16 ch
- Sums amplitude from all channels
- Transfer total energy or hit pattern to CTP

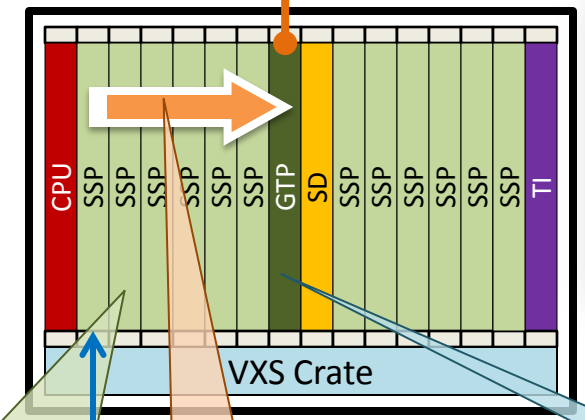
Fiber Optics
- 64 bit @ 125 MHz



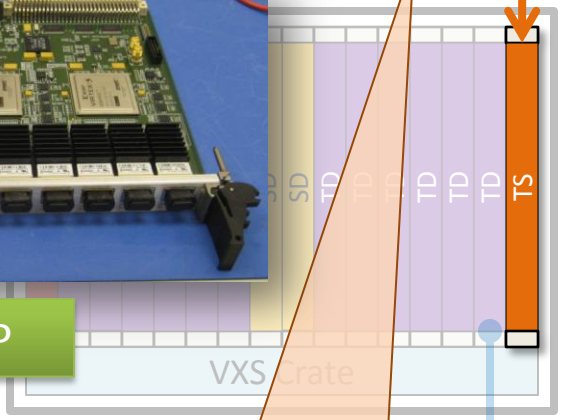
VXS Serial Link
- 16 bit @ 250 MHz: 4 Gbps

Crate Trigger Processor
- Sums energies from FADCs
- Transfer total energy or hit pattern to SSP

L1 Trigger Diagram

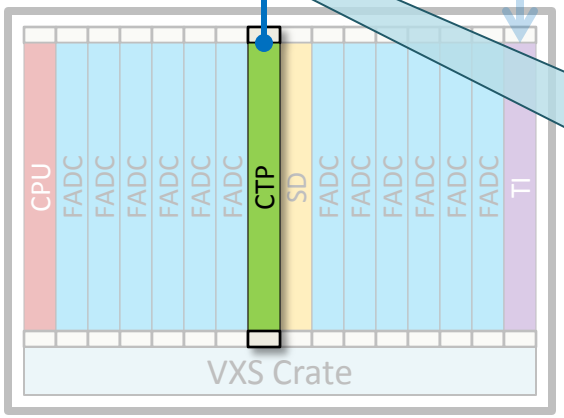


SSP



Sub-System Processor
- Consolidates multiple crate subsystems
- Report total energy or hit pattern to GTP

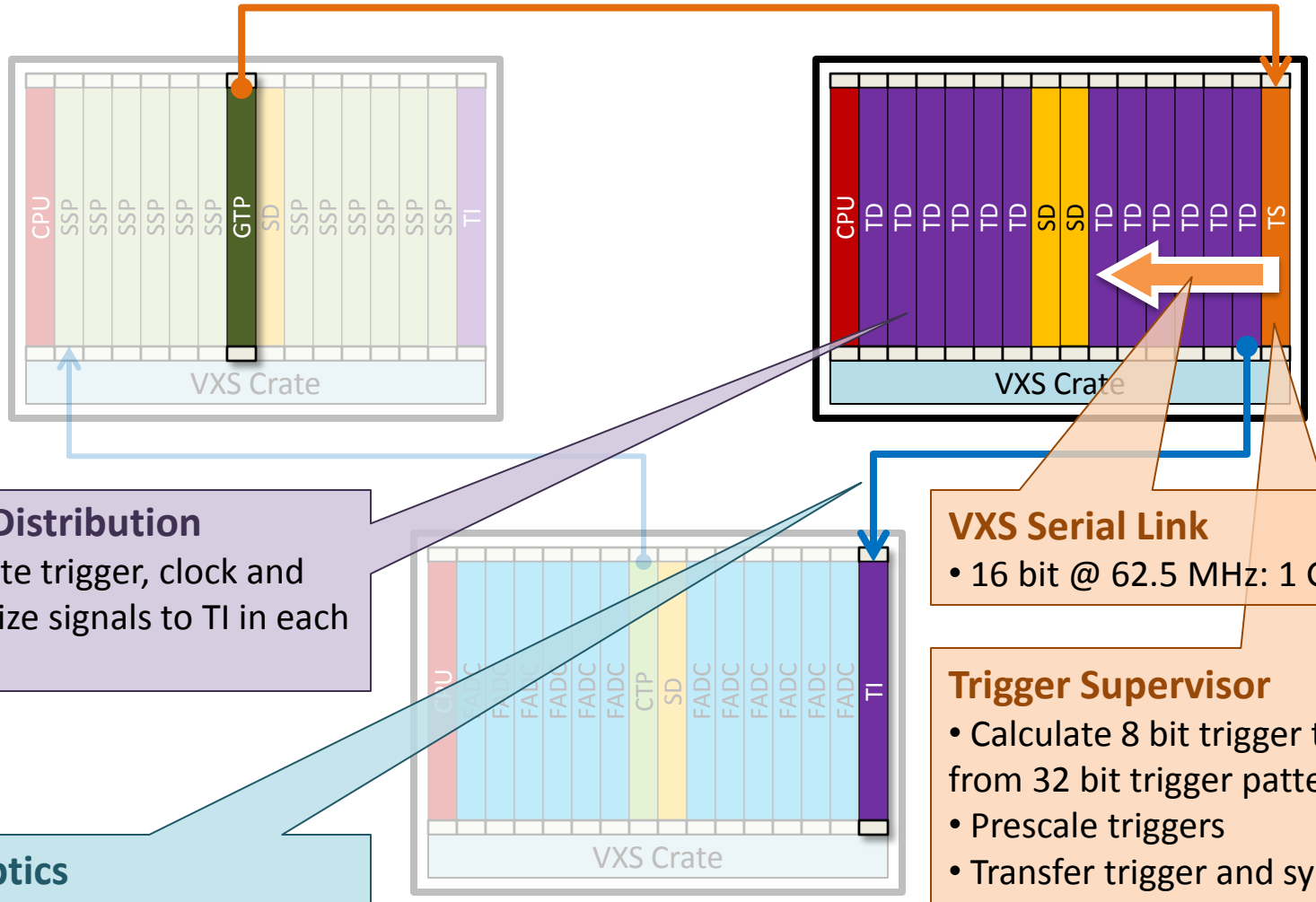
Copper Ribbon Cable
- 32 bit @ 250 MHz: 8 Gbps



Global Trigger Processor
- Collect L1 data from SSPs
- Calculate trigger equations
- Transfer 32 bit trigger pattern to TS

VXS Serial Link
- 32 bit @ 250 MHz: 8 Gbps

L1 Trigger Diagram



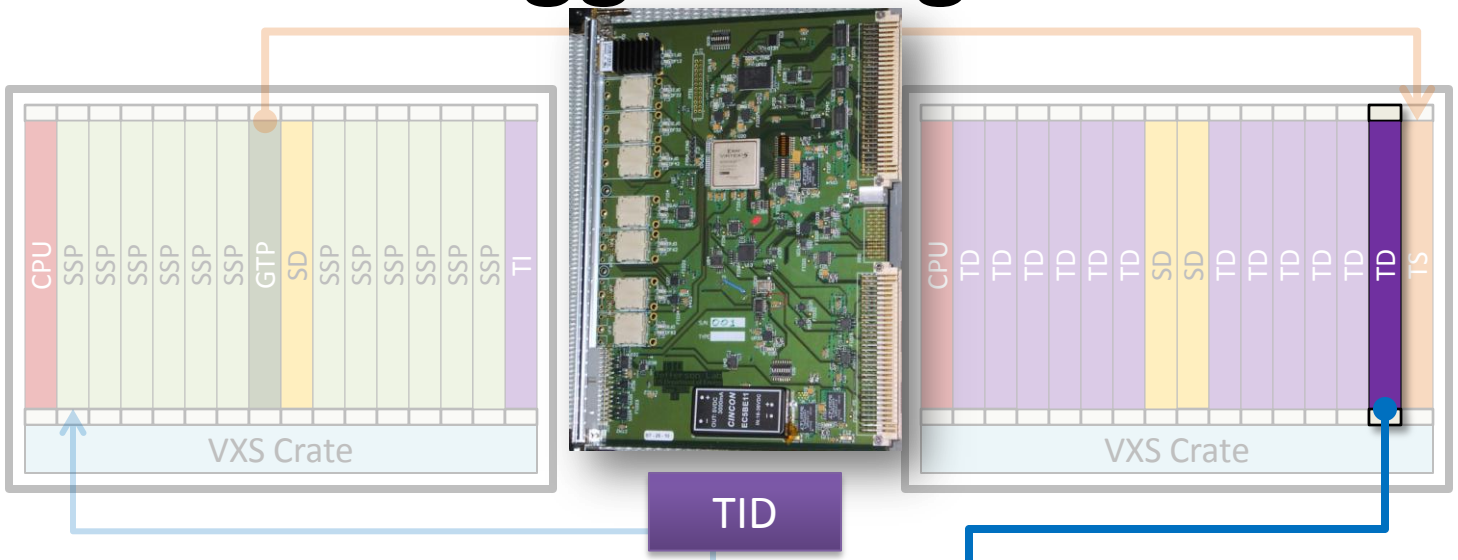
Trigger Distribution
- Distribute trigger, clock and synchronize signals to TI in each Crate

Fiber Optics
- 16 bit @ 62.5 MHz: 1 Gbps

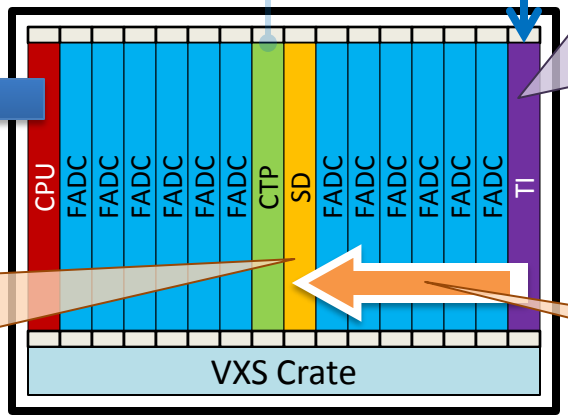
VXS Serial Link
- 16 bit @ 62.5 MHz: 1 Gbps

Trigger Supervisor
- Calculate 8 bit trigger types from 32 bit trigger pattern
- Prescale triggers
- Transfer trigger and sync signal to TD (16 bit total)

L1 Trigger Diagram



VME Readout Controller
- Gigabit ethernet

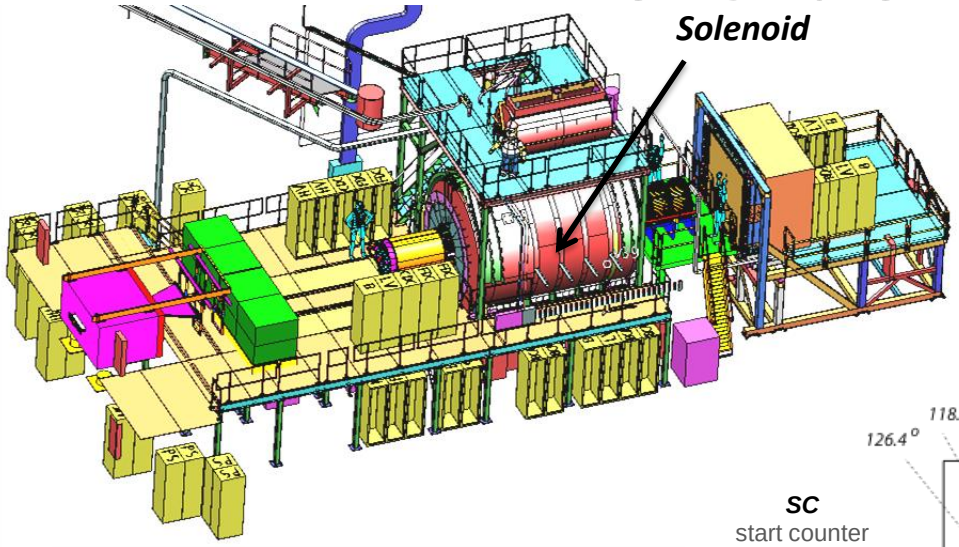


Trigger Interface
- Receive trigger, clock and sync signals from TD
- Make crate trigger decision
- Pass signals to SD

Signal Distribution
- Distribute common signals to all modules: busy, sync and trigger 1/2

VXS Serial Link
- 4 bit @ 250 MHz: 1 Gbps

The GlueX Detector

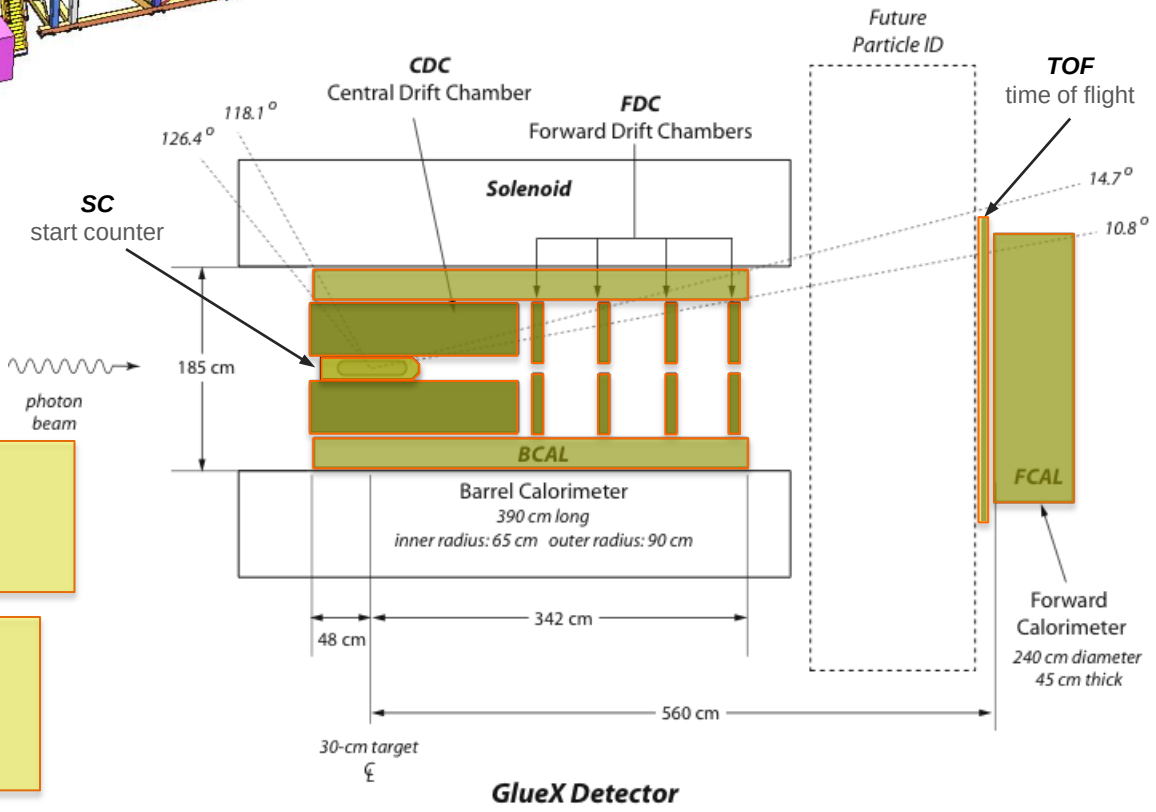


- 2.2T superconducting solenoidal magnet
- Fixed target (LH_2)
- 10^8 tagged γ/s (8.4-9.0GeV)
- hermetic

Charged particle tracking
- Central drift chamber (straw tube)
- Forward drift chamber (cathode strip)

Calorimetry
- Barrel Calorimeter (lead, fiber sandwich)
- Forward Calorimeter (lead-glass blocks)

PID
- Time of Flight wall (scintillators)
- Start counter
- Barrel Calorimeter



GlueX Data Rate

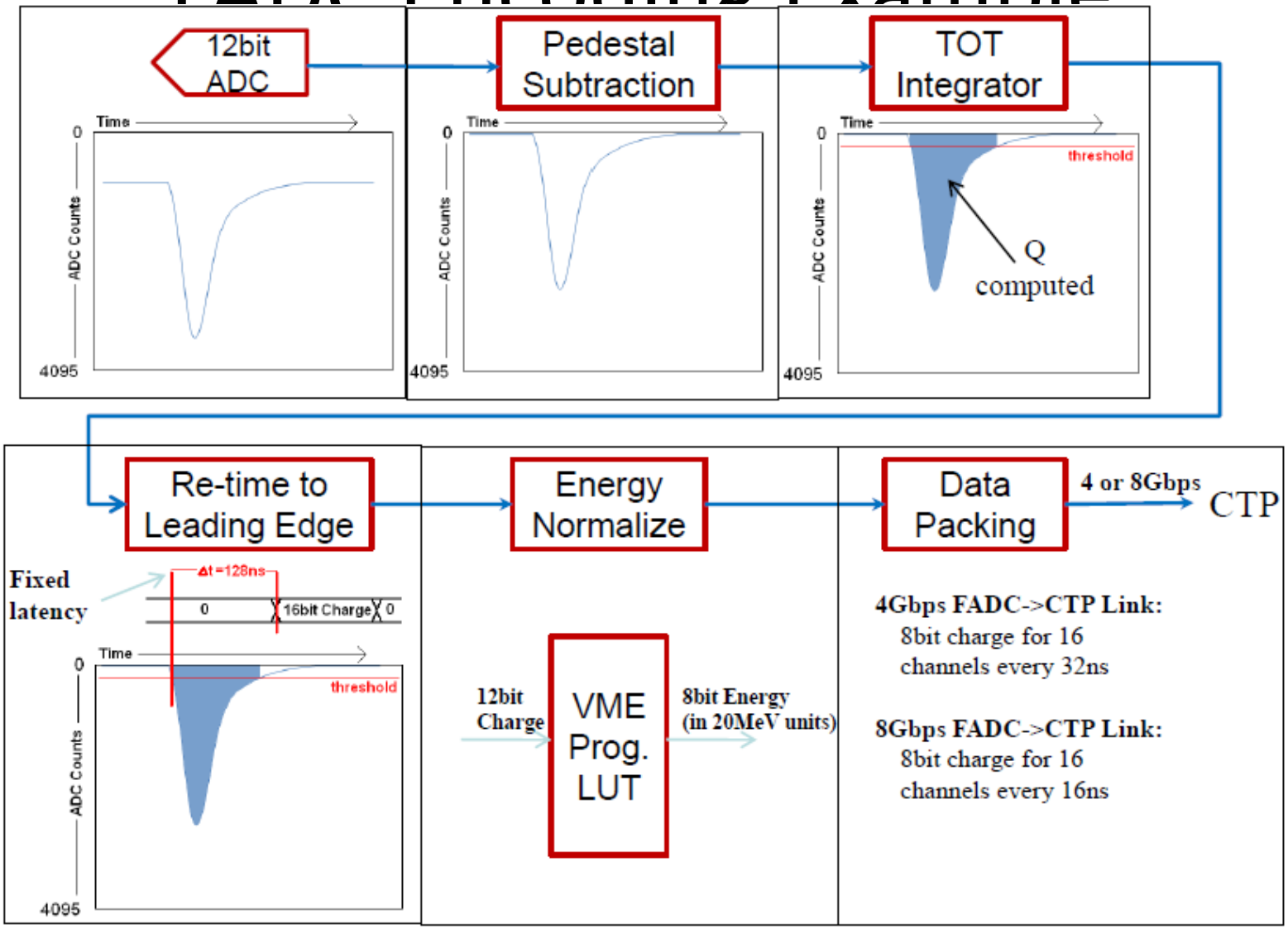
		Front End DAQ Rate	Event Size	L1 Trigger Rate	Bandwidth to mass Storage	
JLab	GlueX	3 GB/s	15 kB	200 kHz	300 MB/s	priva comm.
	CLAS12	0.1 GB/s	20 kB	10 kHz	100 MB/s	
LHC	ALICE	500 GB/s	2,500 kB	200 kHz	200 MB/s	CHEP2007 talk Sylvain Chapelin
	ATLAS	113 GB/s	1,500 kB	75 kHz	300 MB/s	
	CMS	200 GB/s	1,000 kB	100 kHz	100 MB/s	
	LHCb	40 GB/s	40 kB	1000 kHz	100 MB/s	
BNL	STAR	50 GB/s	1,000 kB	0.6 kHz	450 MB/s	*
	PHENIX	0.9 GB/s	~60 kB	~ 15 kHz	450 MB/s	**

*** Jeff Landgraf Private Comm. 2/11/2010**
**** CHEP2006 talk MartinL. Purschke**

CODA3 – What's different

CODA 2.5	CODA 3
Run Control (X, Motif, C++) (rcServer, runcontrol)	Experiment Control – AFECS (pure JAVA) (rcPlatform, rcgui)
Communication/Database (msql, cdev, dptcl, CMLOG)	cMsg – CODA Publish/Subscribe messaging
Event I/O C-based simple API (open/close read/write)	EVIO – JAVA/C++/C APIs Tools for creating data objects, serializing, etc…
Event Builder / ET System / Event Recorder (single build stream)	EMU (Event Management Unit) Parallel/Staged event building
Front-End – vxWorks ROC (Interrupt driven – event by event readout)	Linux ROC, Multithreaded (polling – event blocking)
Triggering: 32 ROC limit, (12 trigger bits -> 16 types) TS required for buffered mode	128 ROC limit, (32 trigger bits -> 256 types) TI supports TS functionality. Timestamping (4ns)

FADC Encoding Example



GTP Trigger Bit Example