SoLID DAQ for Transversity and PVDIS

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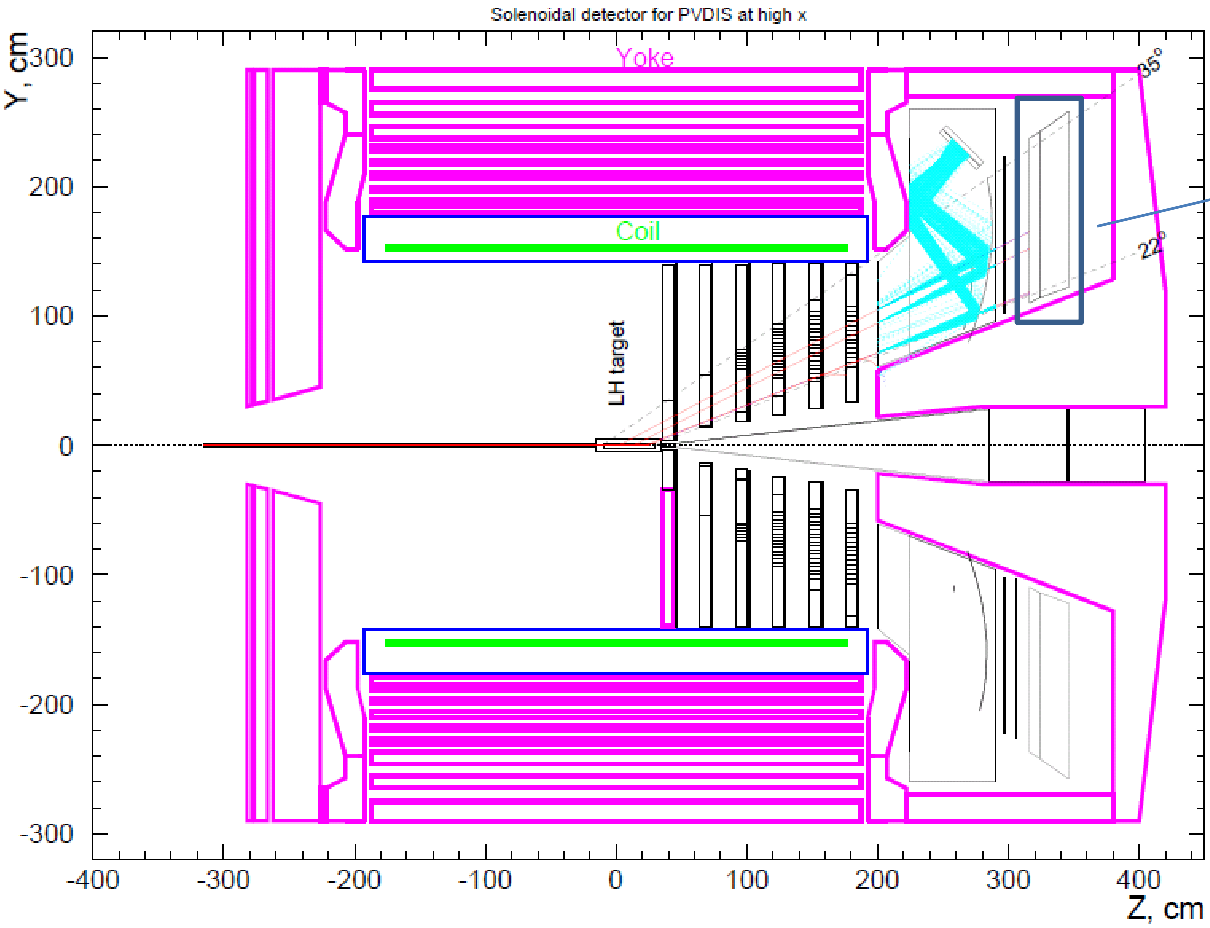
Overview

- Requirements overview
- Pipelined electronics
- GEM
- Electronics layout
- Budget
- Man Power
- Tasks list
- Test stand
- Timeline
- Conclusion

REQUIREMENTS FOR SOLID DAQ

Detector layout and trigger for PVDIS



Trigger

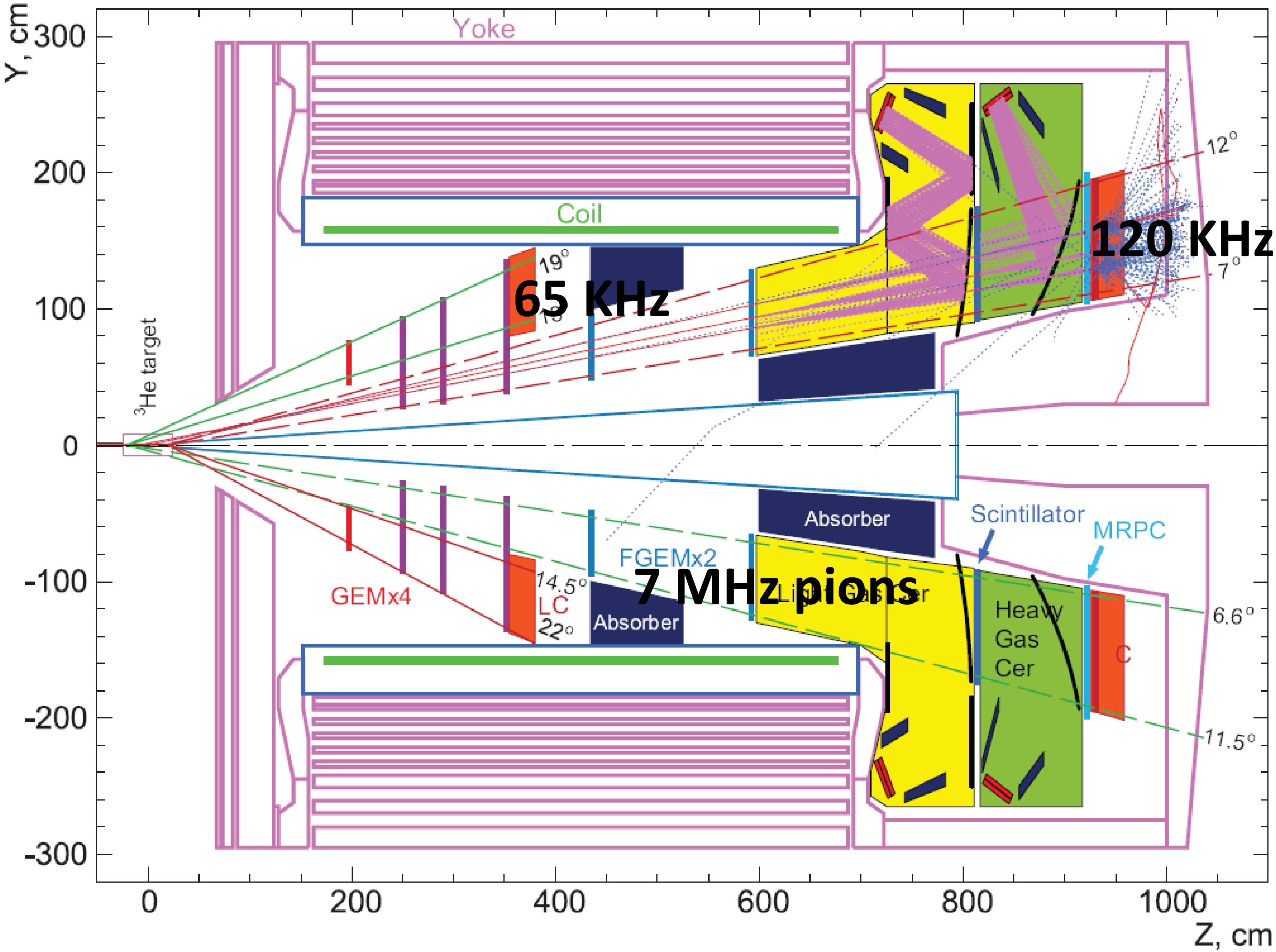
Calorimeter

200 to 500 KHz of electrons

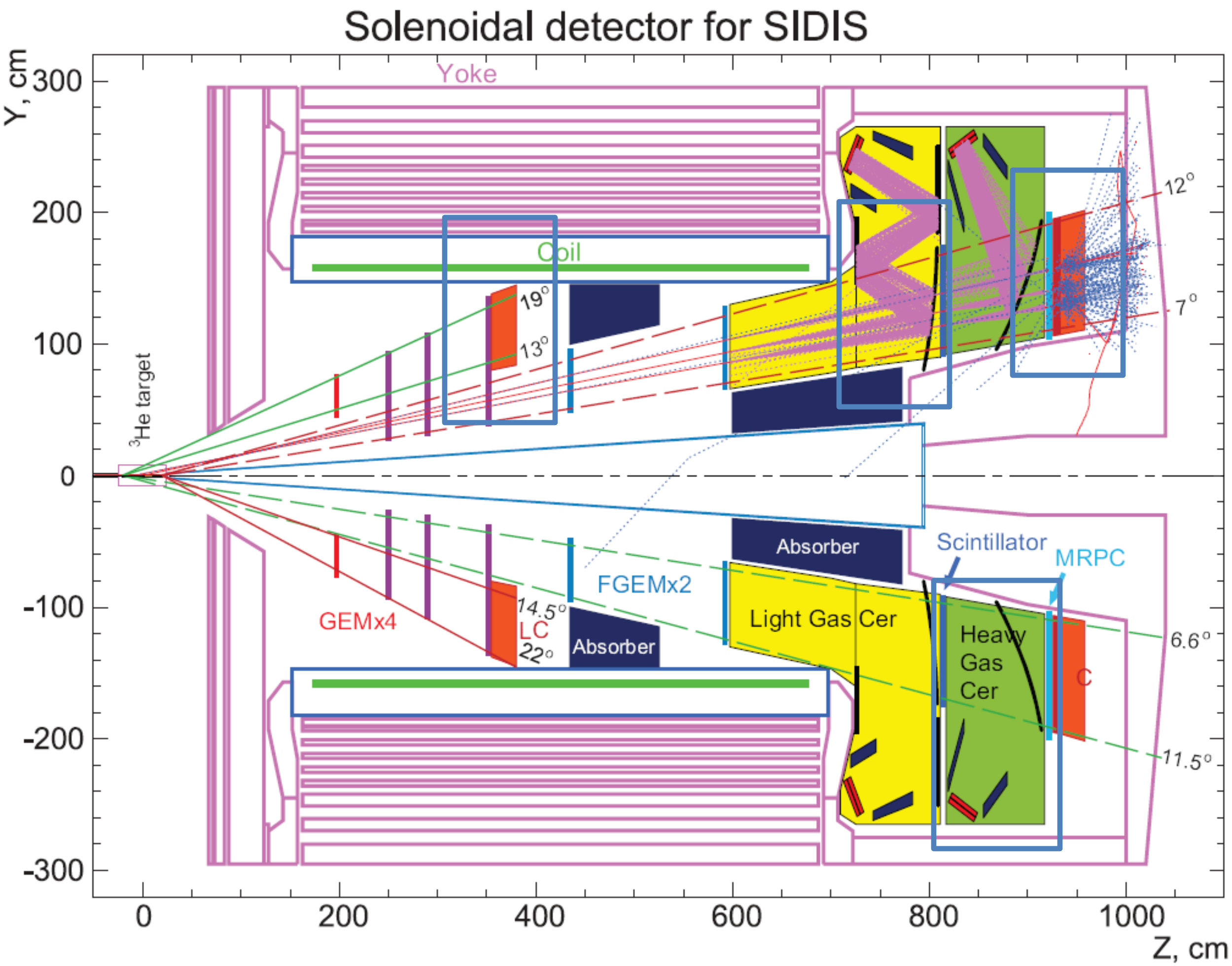
30 individual sectors
to reduce rate

Max 17 KHz/sector

Solenoidal detector for SIDIS



Detector layout and trigger for SIDIS



Trigger

Calorimeter
+
Cerenkov
+
MRPC

Coincidences and threshold for global 60 KHz trigger rates

SIDIS rates Summary

	Rates @ 11 GeV
Large Angle > 3.0 GeV	44 kHz
Large Angle with GEM Pad	13 kHz
Forward Angle:	125 kHz
Forward Angle @ 2 GeV	64 kHz
Forward Angle with P.D.S. Cut	77 kHz
Forward Angle with P.D.S. Cut + 2.0 GeV	51 kHz

Trigger rates around 60 KHz

SIDIS: Coincidence @ 35 ns window

- Assuming a 50 ns gate
- Coincidence rate: 7.7MHz x 200KHz x 35 ns = 54 kHz
- Given the safety margin, expected to handle about 100 kHz.
  - Include some single trigger to study detector performance etc.
- 4kB * 100 kHz ~ 400 MB/s to disk
  - Goal to reduce things to 50 MB/s by L3 farm

SoLID SIDIS Detector Rates

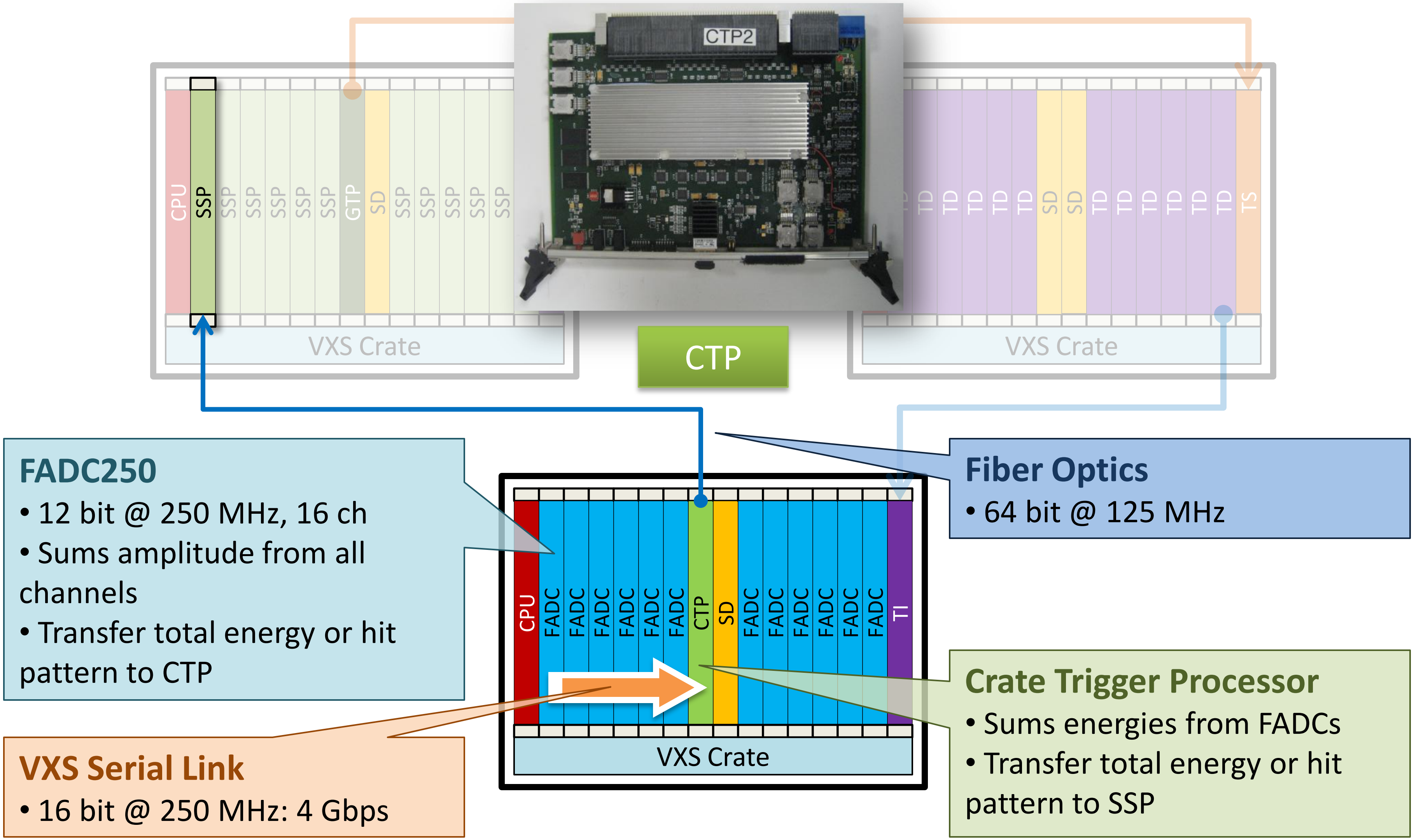
Full simulation in progress

Detector	Rate	Hits	Type	Data Size per hit
GEM	4.4 GHz	220	Hits (time)	4 Byte x 2 (X/Y)
LC	120 kHz	1	Energy, Hits	8 Byte x 2 (PS/SH)
FC	200 MHz	10	Energy, Hits	8 Byte x 2 (PS/SH)
LGC	40 MHz	3	Energy, Hits	8 Byte x 2 (split)
HGC	60 MHz	4	Energy, Hits	8 Byte x 2 (split)
MRPC	850 MHz	45	Hits	4 Byte
SC	300 MHz	15	Energy, Hits	8 Byte
Total				2.5 kB

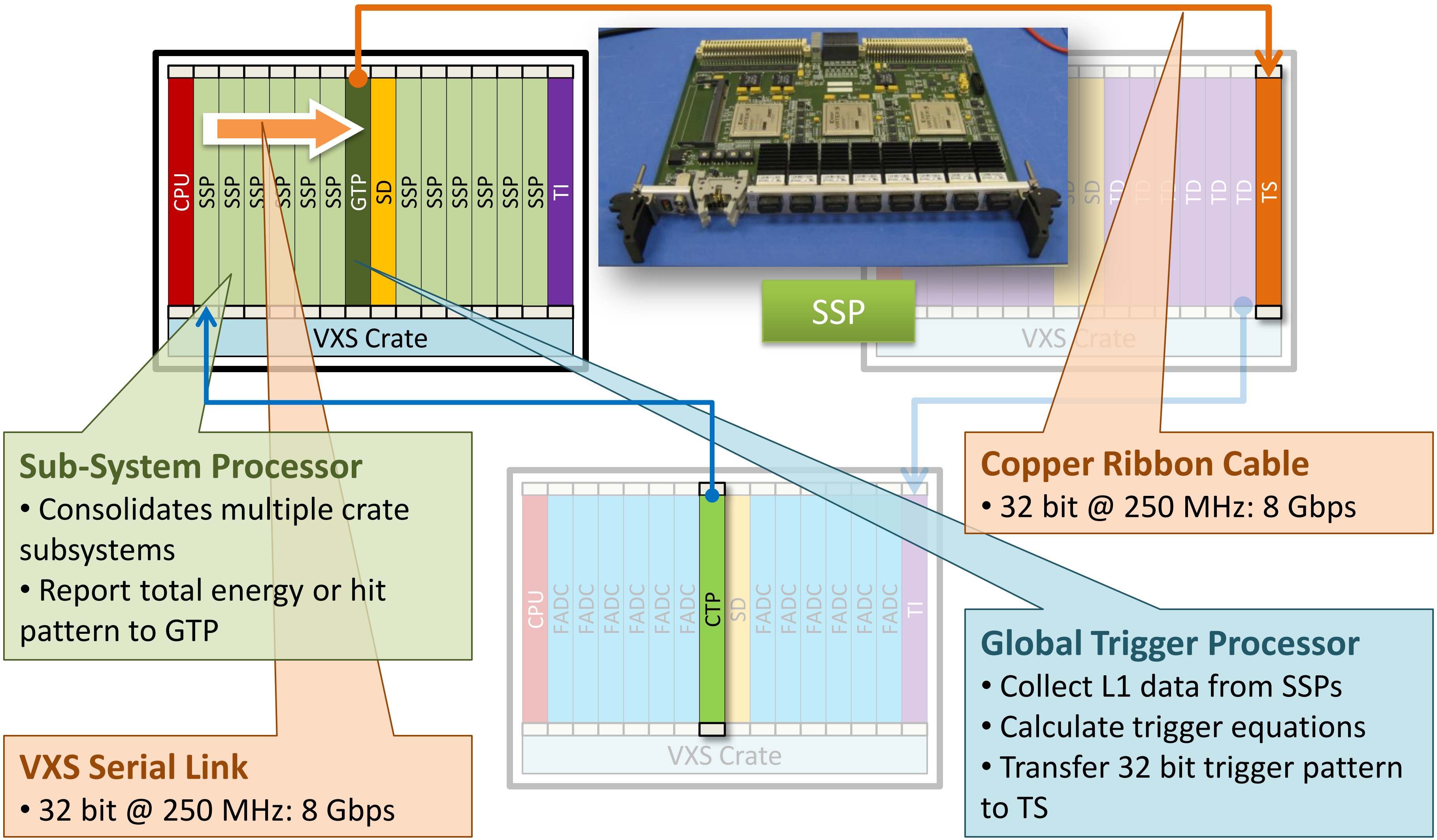
With header and other over head
event size is ~ **4 kB**

Jefferson Laboratory Pipelined electronics with CODA 3

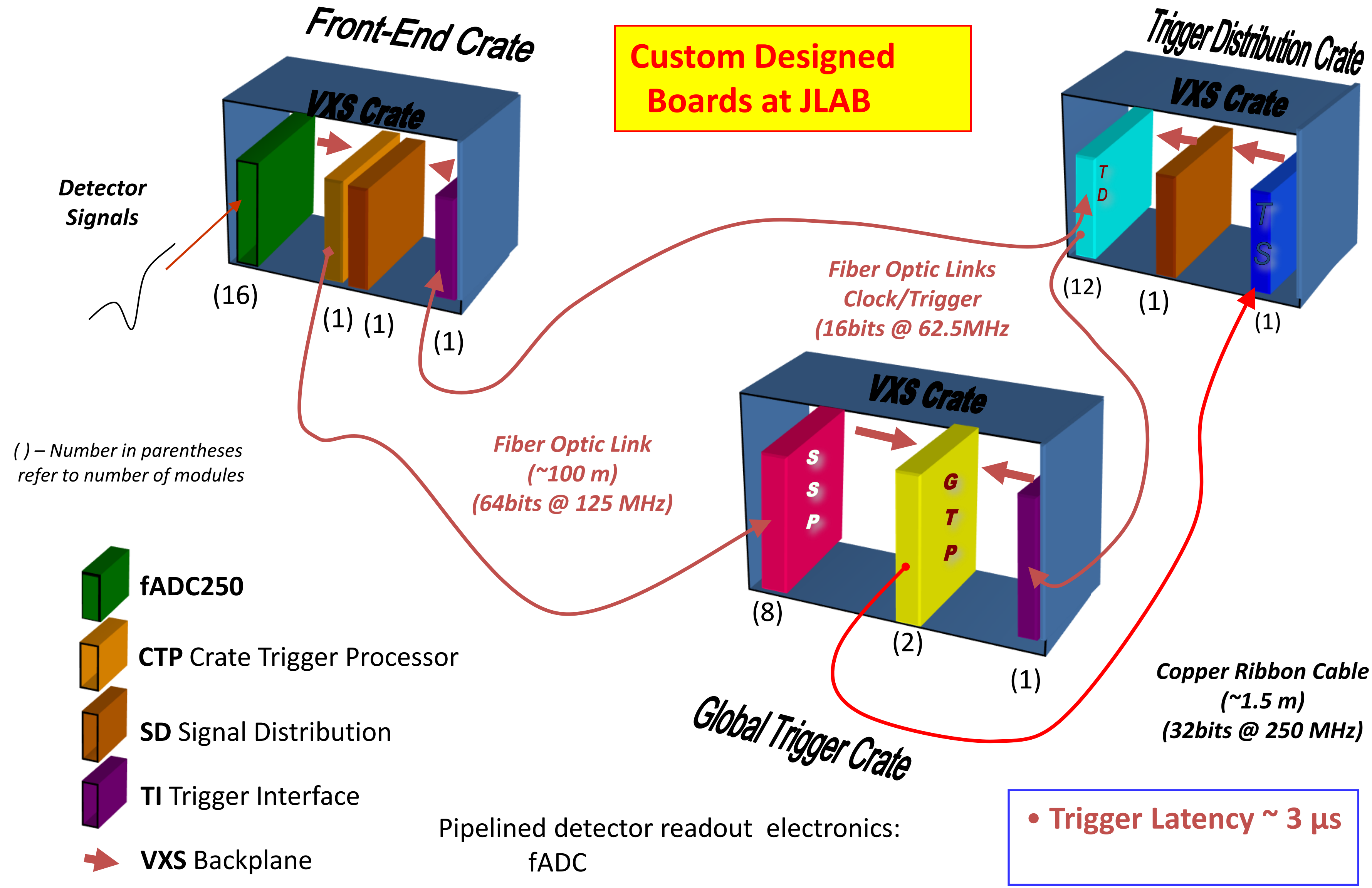
L1 Trigger Diagram



L1 Trigger Diagram



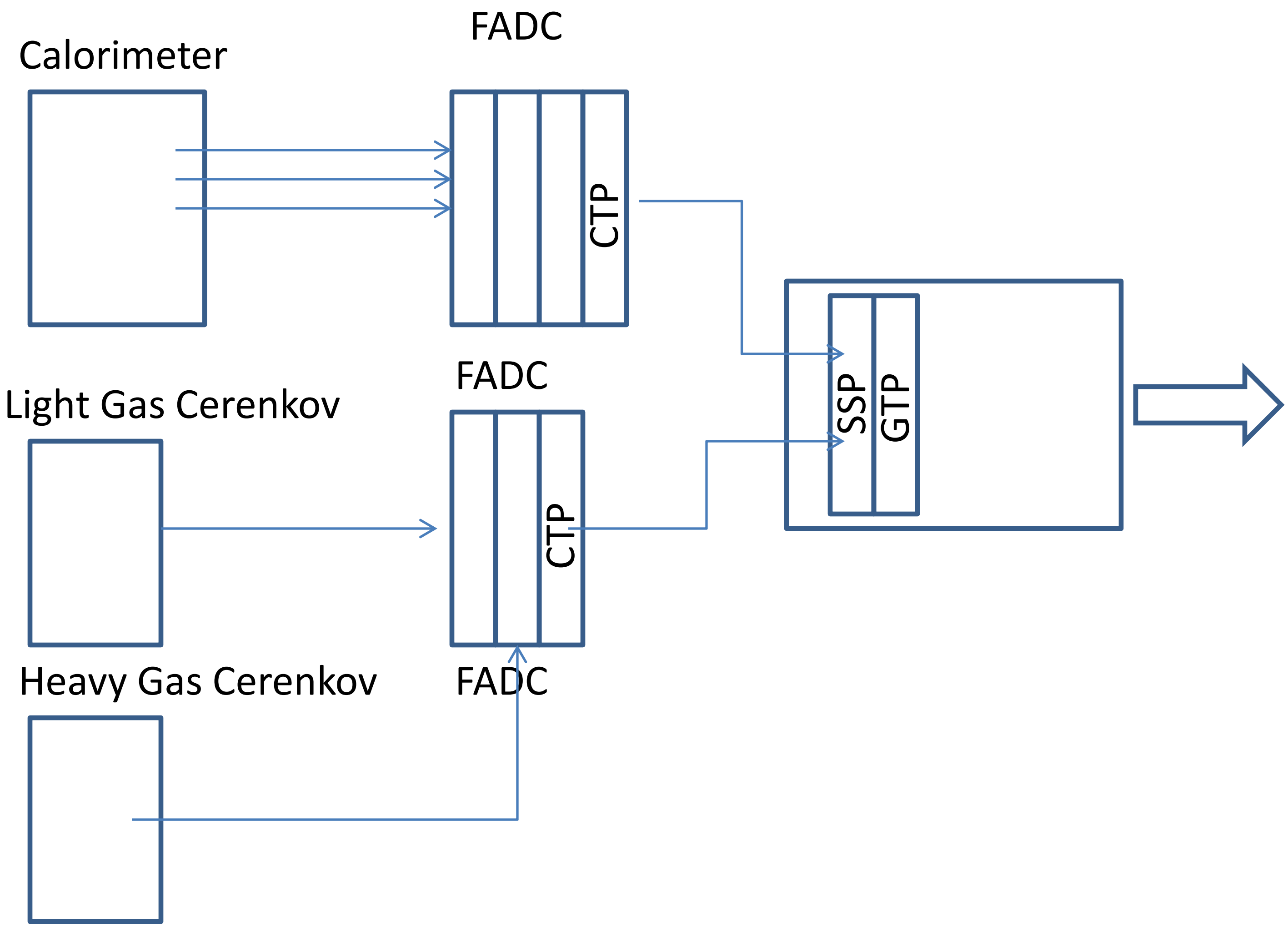
Level-1 Trigger Electronics



Pipelined detector readout electronics:
fADC

- Trigger Latency ~ 3 µs

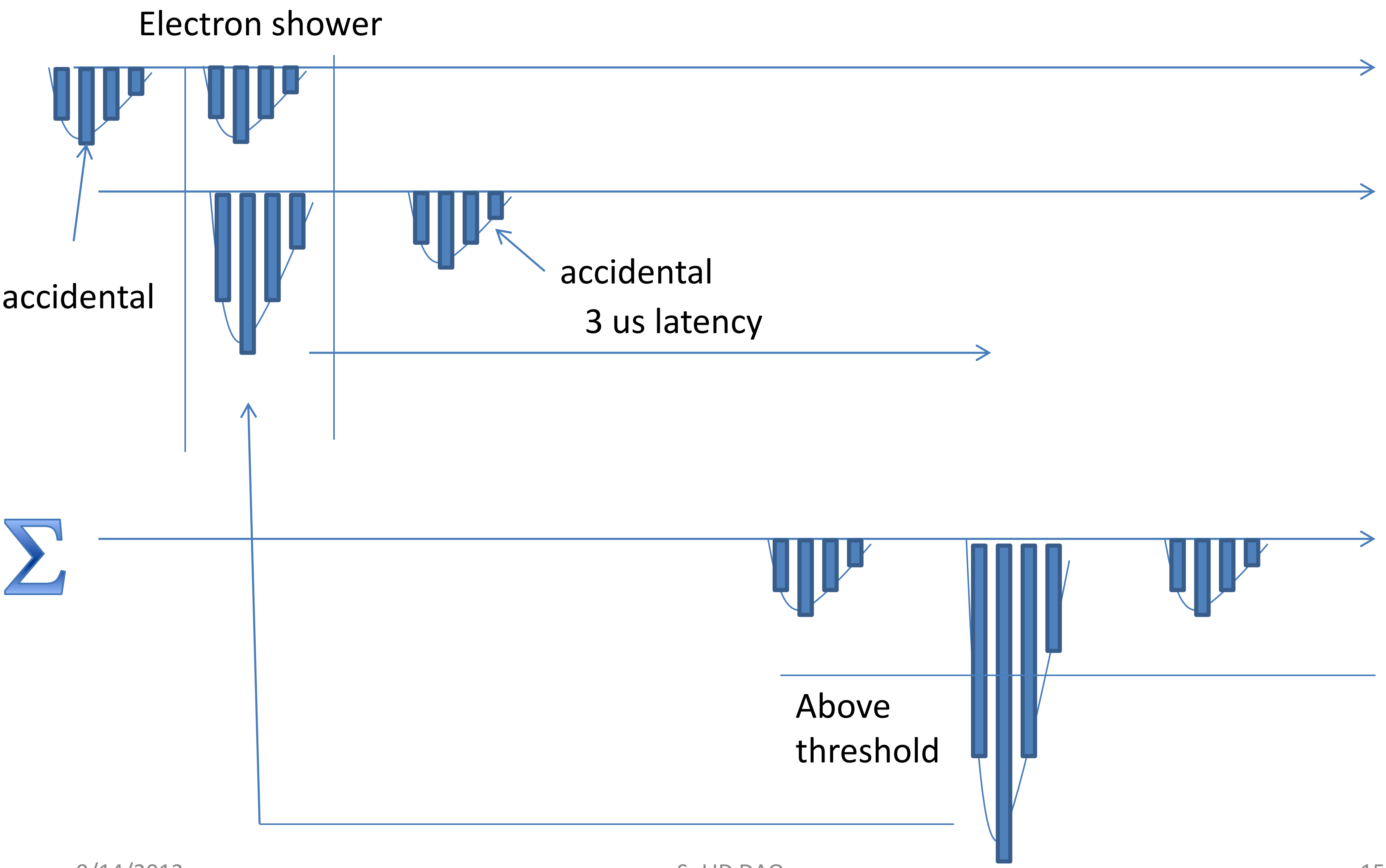
Pipelined Hall D DAQ



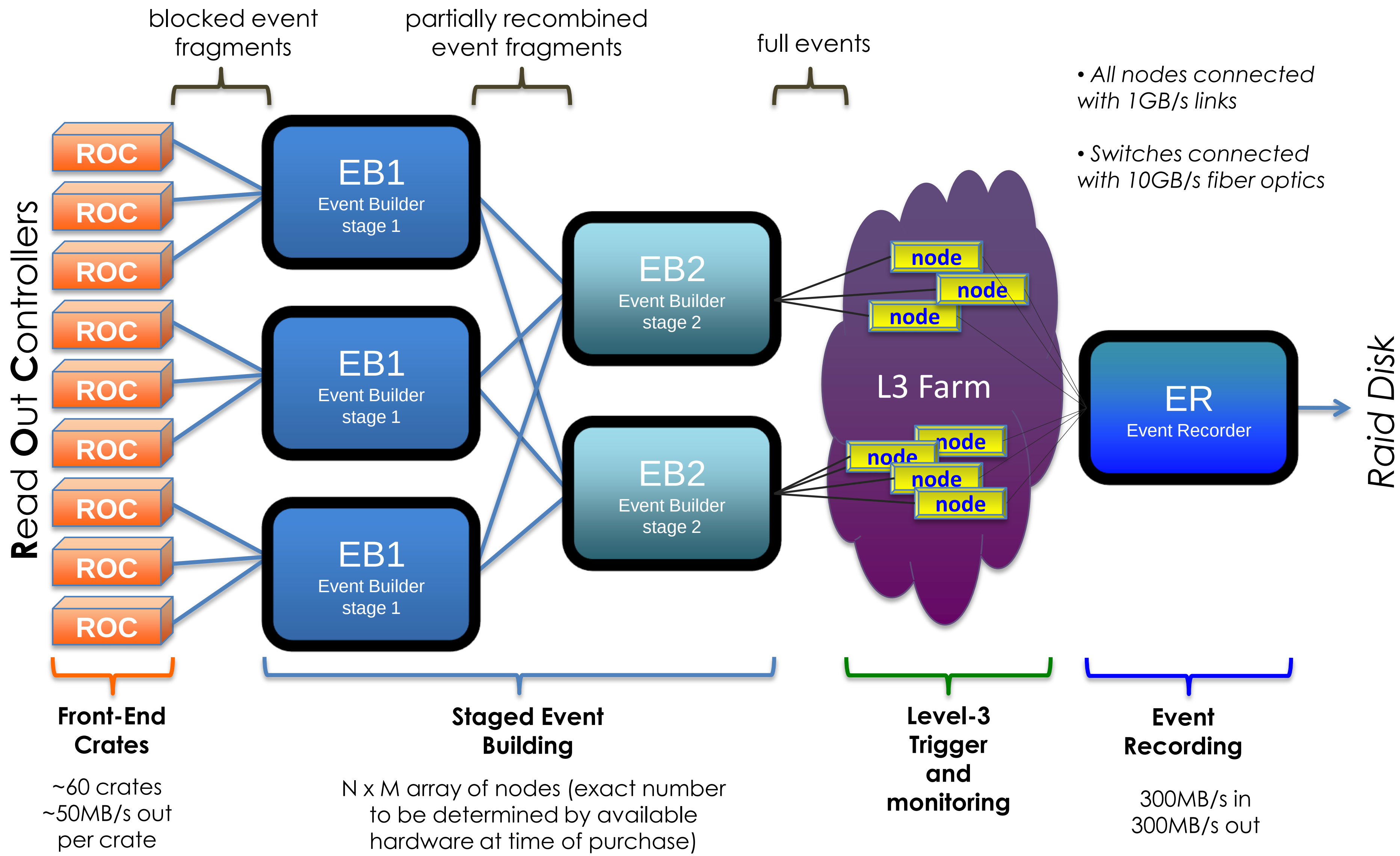
L1 trigger

Calorimeter
+
Cerenkov
+
Pion
In
3 us

Pipelined Hall D DAQ



L3 Farm



blocked event fragments
partially recombined event fragments
full events
• All nodes connected with 1GB/s links
• Switches connected with 10GB/s fiber optics
Read Out Controllers
ROC
ROC
ROC
ROC
ROC
ROC
ROC
ROC
ROC
EB1 Event Builder stage 1
EB1 Event Builder stage 1
EB1 Event Builder stage 1
EB2 Event Builder stage 2
EB2 Event Builder stage 2
node
node
node
L3 Farm
node
node
node
node
ER Event Recorder
Raid Disk
Front-End Crates
~60 crates
~50MB/s out per crate
Staged Event Building
N x M array of nodes (exact number to be determined by available hardware at time of purchase)
Level-3 Trigger and monitoring
Event Recording
300MB/s in
300MB/s out

GEM READOUT

GEM readout

- APV25 Front GEM ASICs
- Up to 164 000 channels
- APV 25 : 128 channels
- Readout
  - VME based readout : 8 APV25 = 2048 channels

  (~ 10 $ / channels)
  - SRS readout : ethernet /PC based = 2048 channels (~ 3 $ / channels)
- 1 crate per sectors for FADC and GEM

APV25 readout

- Switch Capacitor Array ASICS with buffer length 192 samples at 40 MHz :
  4.8 us Look back 160 samples : 4 us

- Estimated occupancy : 220 hits per trigger, X Y data, 440 strips

GEM : 6 Layers 164 000 channels total, 28 000 channels per planes

Occupancy : 1.6 %

- APV readout time :

t_APV = 141 x number_of_sample / 40 MHz

t_APV(1 sample) = 3.7 us.

Max rate APV front end :
270 KHz in 1 sample mode
90 KHz in 3 samples mode
Will be triggered at around 60 KHz

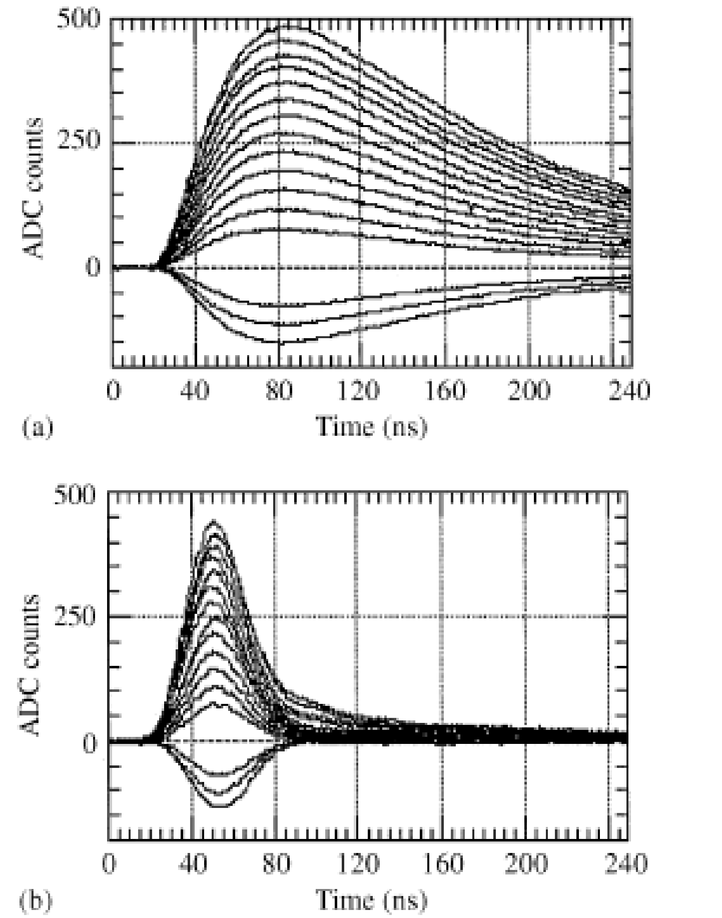


Fig. 5. Response curve of the APV25 as a function of the input signal. (a) Peak mode, (b) deconvolution mode.

GEM in trigger

- Use signal of last GEM plane HV for fast trigger
  - Large angle trackers
  - GEM based Cerenkov
- Quality of signal to be tested (signal / background)
- Could reduce rate in Large Angle from photon calorimeter by 50 KHz
- Additional FADC or discriminator channels to put in trigger

Other GEM readout chips

- APV25 limiting factor
    - Need to evaluate
    - Optimize

- Chip in development

    - CLAS12 Dream CEA/Saclay
    - ATLAS VMM1 BNL
    - ….

- SRS readout compatible with other chips
    - Ethernet + PC based

Chamber occupancy

- About 20 hits per planes
- 5 planes
- Use Shower information
- 3 samples would be useful, but 1 sample seems sufficient
- See tracking talk (Ole Hansen), simulation talk (Seamus Riordan)
- Studies on going

ELECTRONICS LAYOUT AND BUDGET

SIDIS channel count

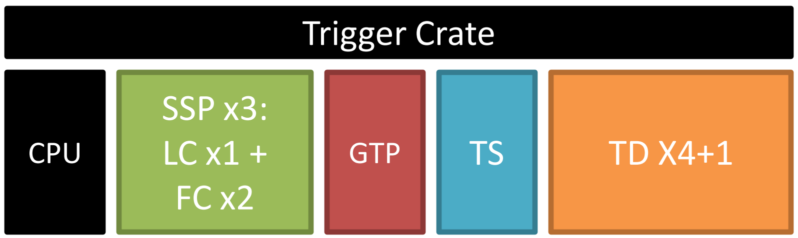
Detector	Module type	Number of channels	Number of FADC
Forward Calorimeter	FADC	1150 x 2	144
Large angle calorimeter	FADC(+TDC)	450 x 2	57
Light Gas Cerenkov	FADC	120	8
Heavy Gas Cerenkov	FADC	270	17
Scintillator	FADC	120	8
MRPC	Custom TDC		

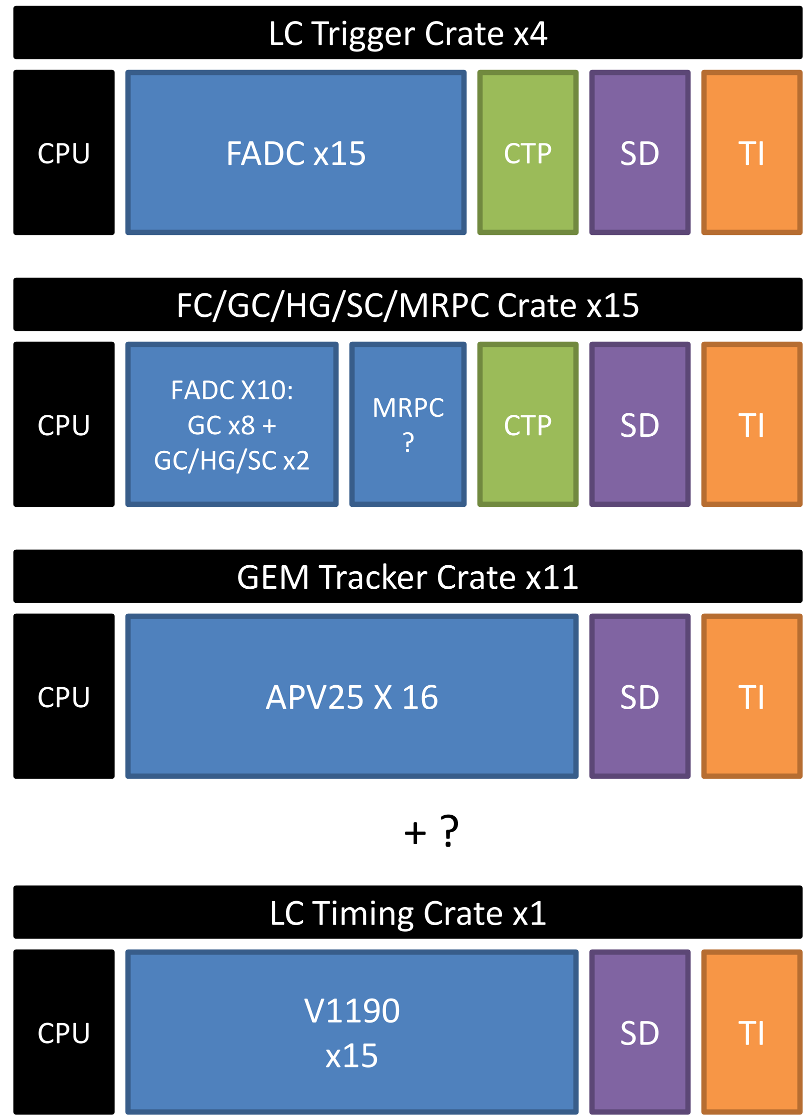
The FADC of LC can be programmed to produce timing signals with ~400ps resolution (already demonstrated by simulation) to remove the needs of TDC.

PVDIS channel count

Detector	Module type	Number of channels	Number of FADC
Forward Calorimeter	FADC	1700 x 2	240
Light Gas Cerenkov	FADC	270	(included in calorimeter FADC)
GEM	FADC	141 000	90

DAQ/Trigger for SoLID SIDIS





Total Crate + CPU: 31+4

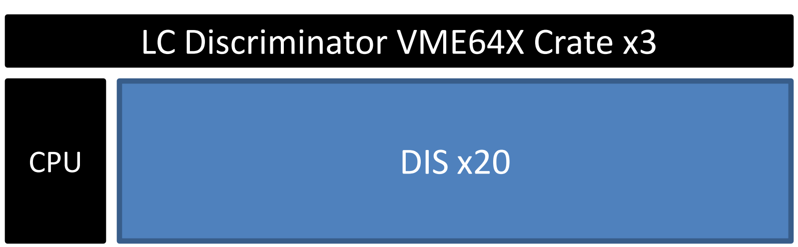
FADC: 210 TI: 30+1

DIS: 0+60 SSP: 3

F1TDC: 0+30 GTP: 1

CTP: 19 TS: 1

SD: 30+1 TD: 4+1

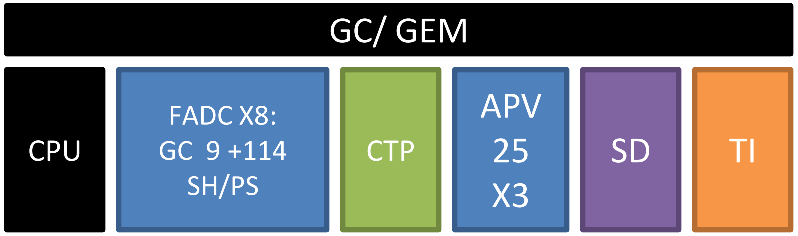


DAQ/Trigger for SoLID PVDIS

VXS crate + CPU: 30

FADC: 240 TI: 30

CTP: 30 CTP SD: 30



30 individual DAQ systems : only 20 KHz trigger rates

No major issues

JLAB electronics PVDIS

Detector	Channel	Module	Unit price	Total modules	Total price sector	Total price 30 sectors
Calorimeter	84	8	4500	240	27000	1 080 000
Cerenkov	9					
TID		1	3000	30	3000	90000
SD		1	2500	30	2500	75000
VXS		1	11500	30	11500	345000
VME CPU		1	3400	30	3400	102000
CTP		1	5000	30	5000	150000
GEM	4700	3	UVA	90	UVA/China	UVA/China
Total price						1 842 000

SIDIS electronics

Module	Unite price	Quantity	
FADC 250	4500	234	$1,053,000
CTP	5000	19	$95,000
SSP	5000	3	$15,000
GTP	5000	1	$5,000
VXS crate	11500	1	$11,500
TS	3500	1	$3,500
TI	3000	30	$90,000
TD	3000	4	$12,000
SD	2500	30	$75,000
VXS crate	11500	30	$345,000
VME CPU	3400	31	$105,400
L3 farm node	5000	12	$60,000
		Total detectors	$1,843,500
VXS crate	11500	1	$11,500
Discriminators	2500	60	$150,000
VME64X crate	8100	3	$24,300
V1190	11010	15	$165,150
VME CPU	3400	4	$13,600
TID	3000	1	$3,000
SD	2500	1	$2,500
			$370,050
		Grand Total	$2,216,950

SIDIS + PVDIS electronics

Module	Unite price	Quantity	
FADC 250	4500	240	$1,080,000
CTP	5000	30	$150,000
SSP	5000	3	$15,000
GTP	5000	1	$5,000
VXS crate	11500	1	$11,500
TS	3500	1	$3,500
TI	3000	30	$90,000
TD	3000	4	$12,000
SD	2500	30	$75,000
VXS crate	11500	30	$345,000
VME CPU	3400	31	$105,400
L3 farm node	5000	12	$60,000
		Total detectors	$1,928,900
VXS crate	11500	1	$11,500
Discriminators	2500	60	$150,000
VME64X crate	8100	3	$24,300
V1190	11010	15	$165,150
VME CPU	3400	4	$13,600
TID	3000	1	$3,000
SD	2500	1	$2,500
			$370,050
		Grand Total	$2,228,950

Costs to be estimated

- Shielding
- Shielding installation
- Cable (Patch and connectors)
- Cabling layout (Cable trays)
- Slow control
- High Voltage

Man power rough estimate

- JLAB
  - Alexandre Camsonne
  - Yi Qiang
- Umass
  - Rory Miskimen
  - Students can be available for electronics works at UMass

		Year 1	Year 2	Year 3	Year 4	Year 5
1 postdoc		Test stand	Test stand	Full electronics	Electronics cabling	Experiment
1 student		Test stand	Test stand	Full electronics	Electronics cabling	Experiment
1 tech		Rack		Rack,cables,weldment	Electronics / detector cabling	
DAQ		Support	Support	Support	Support	
Designer		Layout	Layout			
Electronics		Trigger	Trigger	Support	Support	Support

Man power rough budget

FTE		Year 1	Year 2	Year 3	Year 4	Year 5
1 postdoc		0.5	0.5	0.5	0.5	0.5
1 student		0.5	0.5	0.5	0.5	0.5
1 tech		0.05		0.3		
DAQ		0.1	0.1	0.1	0.1	
Designer		0.1	0.1			
Electronics		0.1	0.1	0.05	0.05	0.05

K$		Year 1	Year 2	Year 3	Year 4	Year 5
1 postdoc		35	35	35	35	35
1 student		25	25	25	25	25
1 tech		3.5	0	21	0	0
DAQ		8	8	8	8	0
Designer		8	8	4	4	4
Electronics		8	8	4	4	4
Total		**87.5**	**84**	**97**	**76**	**68**

about 450 K$ total including inflation

Tasks

- Hardware
  - Trigger design
  - Electronics performance testing
  - Shielding
  - Cabling layout / installation
  - L3 / event filtering
- Simulation
  - Radiation and shielding
  - Background in detector event size
  - Background in detector event/trigger rates
  - Trigger simulation for logic and timing

DAQ Test stand

- Ordered parts / collaboration with Hall A Compton
  - 2 VXS crates
  - 4 FADC
  - 1 CTP, 1SSP
  - 4 Intel VME CPUs
- CODA3 still in the work : test L3 Farm

Time line

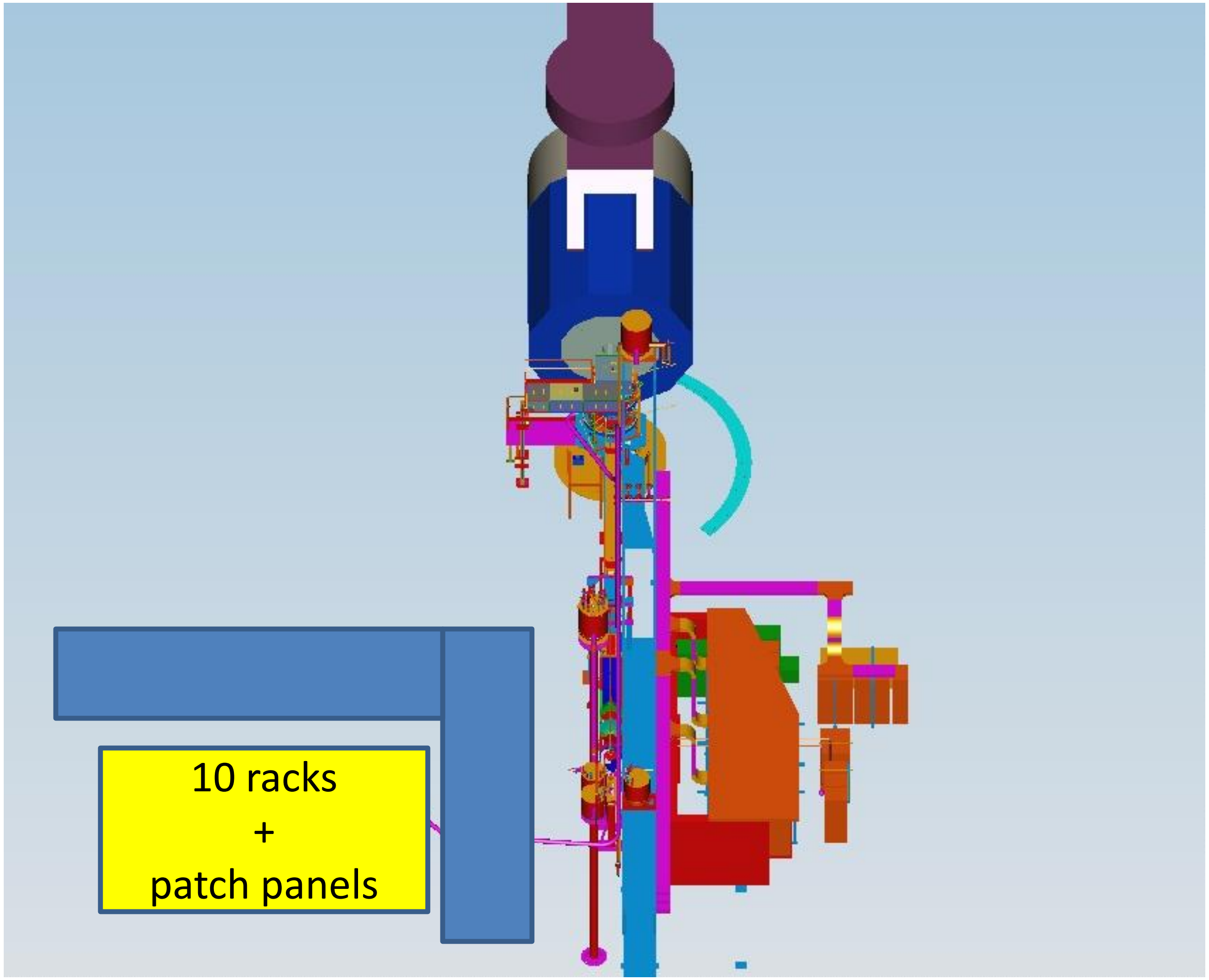
- 2012
  - UMASS Hall D test stand (380 FADC to be tested)
  - 4 JLAB FADC250
  - VXS crate
  - Test APV25 with CODA
- 2013
  - HCAL Trigger development (SBS funding accepted)
  - Small scale setup for testing : FADC + trigger + APV25
- 2014
  - A1n :
    - Full scale test of GEM
    - Digital Trigger electronics test parasitic
  - DVCS : test Intel VME CPU for large amount of data
- 2015
  - Full experiment scale system in place
- 2016-2018
  - Detector cabling and testing

Conclusion

- SoLID requires high rates low dead time, flexible trigger capability
- Rates optimization for SIDIS but push for highest rate depending of GEM chip performances
- Hall D electronics perfectly suited
  - Total cost around 2.5 M$
- GEM electronics R&D
- PVDIS has no major issue, SIDIS limited by GEM readout but APV25 sufficient
- On going testing
- Working on manpower and all inclusive costs

Backup slides

Hall staging



Other projects

- SuperBigBite
  - 242 hadron calorimeter , 1742 Electromagnetic calorimeter
    - 16 FADC
- Hall A BIA
  - VDC 2944 channels
    - 24 V1190 TDC
  - 34 FADC
  - CTP, TS, TD,SD, 2 VXS crates

Production Board Quantities – per C. Cuevas

Board ID	Hall D (Spare)	Hall B (Spare)	Hall A	Hall C	'Physics' FEG DAQ	Totals $FY12	SOLID
FADC250	350 * (36)	310 ** (25)	4 50	46	16	726	210
Trigger Interface	57 (8)	64 (8)	2	2	6	131	30
Signal Distribution	57 (8)	49 (9)	2	2	2	112	30
Crate Trigger Processor	23	21	1	2	2	49	30
Sub-System Processor	8	14	1	1	1	25	3
Global Trigger Processor	2	2	1	1	1	7	1
Trigger Distribution	10	10	1	1	2	24	4
Trigger Supervisor	2	2	1	1	1	7	1

50 → Hall A DAQ upgrade (16 of which used for SBS)

Production Board Notes – per Chris Cuevas
Other 12GeV Proposed Detectors

** CLAS12 'baseline' FADC250 board count is 239
- Central Neutron Detector is 288 channels or 18 boards
- Forward Tagger (PbWO4) calorimeter is 424 channels or 28 boards
- Total on previous page is 310 boards

- So, 25 boards are spare

* Hall D 'baseline' FADC250 board count is 282
- BCAL readout Change Request adds one layer or 32 boards
- Total on previous page is 350

- So, 36 boards are spare

+ Hall C 'baseline' FADC250 board count for SHMS is 16
- HMS is 13 boards, plus 2 spares → ordered 15 spares
- User request of ~40 boards through NSF/MRI for (PbWO4) π^0 spectrometer

Note: In FY12 thirty-five (35) Pre-Production units were purchased and will most likely not be used for the final hall installations. These units are functionally equal to the production units, but need a few very minor circuit corrections.

Potentially: 25 + 36 + 15 + 50 +35 = 161 = 145 FADCs (10 % spare)

SoLID electronics

Modules	Unit price	Quantity	Price	Borrow
FADC 250	4500	66	$297000	JLAB
CTP	5000	28	$140,000	HRS
SSP	5000	2	$10,000	HRS
GTP	5000	0	$0	HRS
VXS crate	11500	0	$0	SBS
TS	3500	0	$0	HRS
TI	3000	24	$72,000	HRS
TD	3000	2	$6,000	HRS
SD	2500	24	$60,000	HRS
VXS crate	11500	24	$276,000	HRS
VME CPU	3400	19	$64,600	HRS
L3 farm node	5000	12	$60,000	
		Total	$985,600	
VXS crate	11500	0	$0	HRS
Discriminators	2500	50	$125,000	HRS
VME64X crate	8100	0	$0	HRS
V1190	11010	0	$0	HRS
VME CPU	3400	0	$0	HRS
TID	3000	0	$0	HRS
SD	2500	0	$0	HRS
		Total timing	$125,000	
				With 10 % spare
		Total detectors	$1,110,600	$1,332,720

Production Board Notes – per Chris Cuevas
Other 12GeV Proposed Detectors

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SIDIS: Singles Electron Trigger

- Large Angle: 65 kHz @ 11 GeV
  - Calorimeter only
  - Electron: 11 kHz
  - High energy photon: 51.5 kHz
    - (possible to be rejected by including GEM in trigger, need study)
  - Hadron: <3 kHz (energy cut)
- Small angle: 120 kHz @ 11 GeV
  - Calorimeter + Gas Cherenkov
  - Electron: 90 kHz
  - High energy photon: 16 kHz (after Gas Cherenkov)
  - Hadron: 15 kHz (after Gas Cherenkov and Calorimeter)
- 8.8 GeV gives about 240 kHz

Test run setup

- MRPC
  - V1290
  - JLAB or SIS FADC
- GEM / Hadron Blind Detector
  - APV25 (UVA)
    - SRS readout
    - MPD

DAQ electronics projects at UMass: spring and summer 2012
R.Miskimen

- UMass is responsible for the final assembly and testing of all *380 FADC modules* for Hall D. This activity will take place at UMass summer 2012, probably stretching into the fall.

- An undergraduate, Fabien Ahmed, spent the summer of 2011 at JLab working with the electronics group on FADC tests. A graduate student, Bill Barnes, and team of undergraduates will work on the electronics tests at UMass.

- Operations at UMass will include mechanical assembly of the VME boards, programming the FPGA's, verifying board operation, measuring and recording noise levels.

- Readout through a Wiener USB board in the VXS crate, connected to PC

DAQ electronics projects at UMass: connection to SOLID

• This activity helps Hall D, only helps SOLID by building expertise in the collaboration for working with and debugging DAQ electronics

• With support from Hall A, we would develop a CODA based DAQ test station at UMass: replicate the one VXS crate/sector readout for PVDIS/SOLID

Need CODA, and to borrow CTP, SSP, and CPU

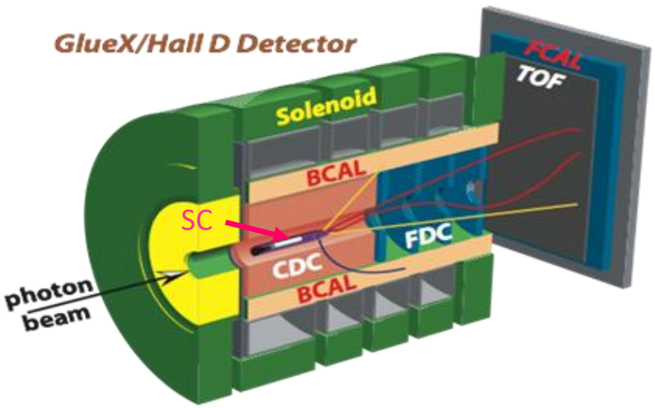
Test DAQ rates, triggers, software for FADC

SIDIS channel count

Detector	Module type	Number of channels	Number of modules
Forward Calorimeter	FADC+TDC	2x1150	119
Large angle calorimeter	FADC+TDC	2x450	58
Light Gas Cerenkov	FADC+TDC	120	8
Heavy Gas Cerenkov	FADC+TDC	270	17
Scintillator	FADC+TDC	120	8
GEM	VME	164K	321

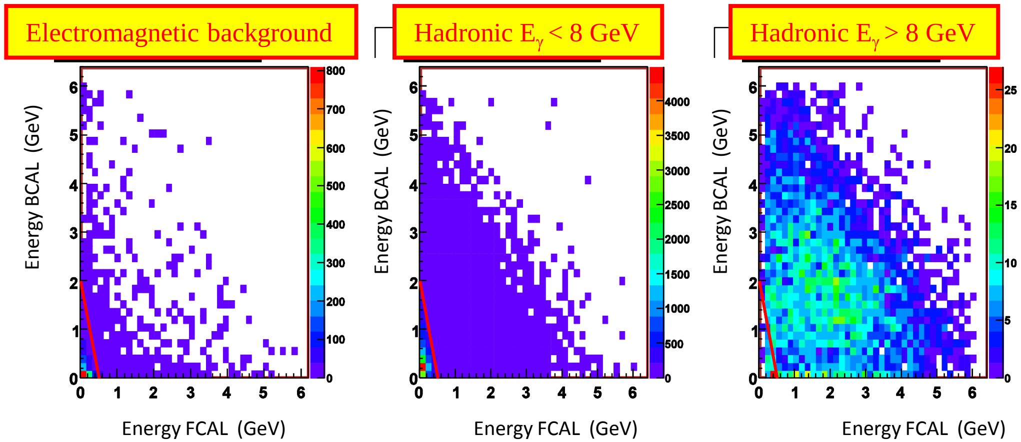
Hall D L1 Trigger-DAQ Rate

- Low luminosity (10^7 γ/s in $8.4 < E_\gamma < 9.0$ GeV)
  - 20 kHz L1
- High luminosity (10^8 γ/s in $8.4 < E_\gamma < 9.0$ GeV)
  - 200 kHz L1
  - Reduced to 20 kHz L3 by online farm
- Event size: 15 kB; Rate to disk: 3 GB/s



Detectors which can be used in the Level-1 trigger:

Forward Calorimeter (FCAL)	Energy
Barrel Calorimeter (BCAL)	Energy
Start Counter (SC)	Hits
Time of Flight (TOF)	Hits
Photon Tagger	Hits

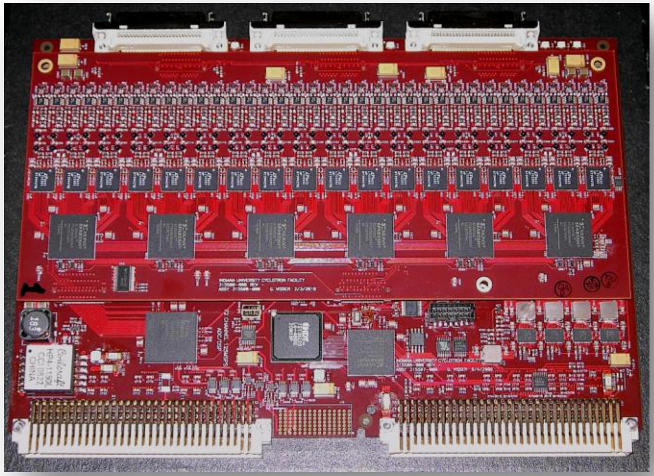


Basic Trigger Requirement:

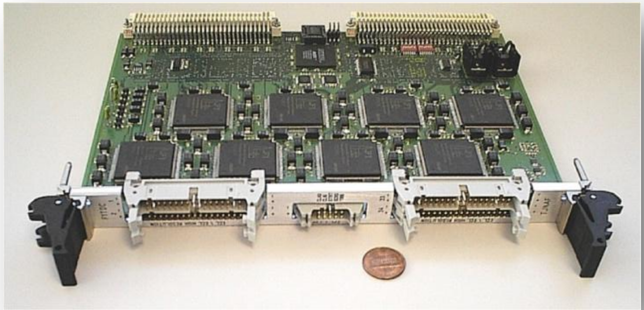
$E_{BCAL} + 4 \cdot E_{FCAL} > 2$ GeV
and a hit in Start Counter

Custom Electronics for JLab

- VME Switched Serial (VXS) backplate
  - 10 Gbps to switch module (J_0)
  - 320 MB/s VME-2eSST (J_1/J_2)
- All payload modules are fully pipelined
  - **FADC125** (12 bit, 72 ch)
  - **FADC250** (12 bit, 16 ch)
  - **F1-TDC** (60 ps, 32 ch or 115 ps, 48 ch)
- Trigger Related Modules
  - **C**rate **T**rigger **P**rocessor (**CTP**)
  - **S**ub-**S**ystem **P**rocessor (**SSP**)
  - **G**lobal **T**rigger **P**rocessor (**GTP**)
  - **T**rigger **S**upervisor (**TS**)
  - **T**rigger **I**nterface/Distribution(**TI/D**)
  - **S**ignal **D**istribution (**SD**)

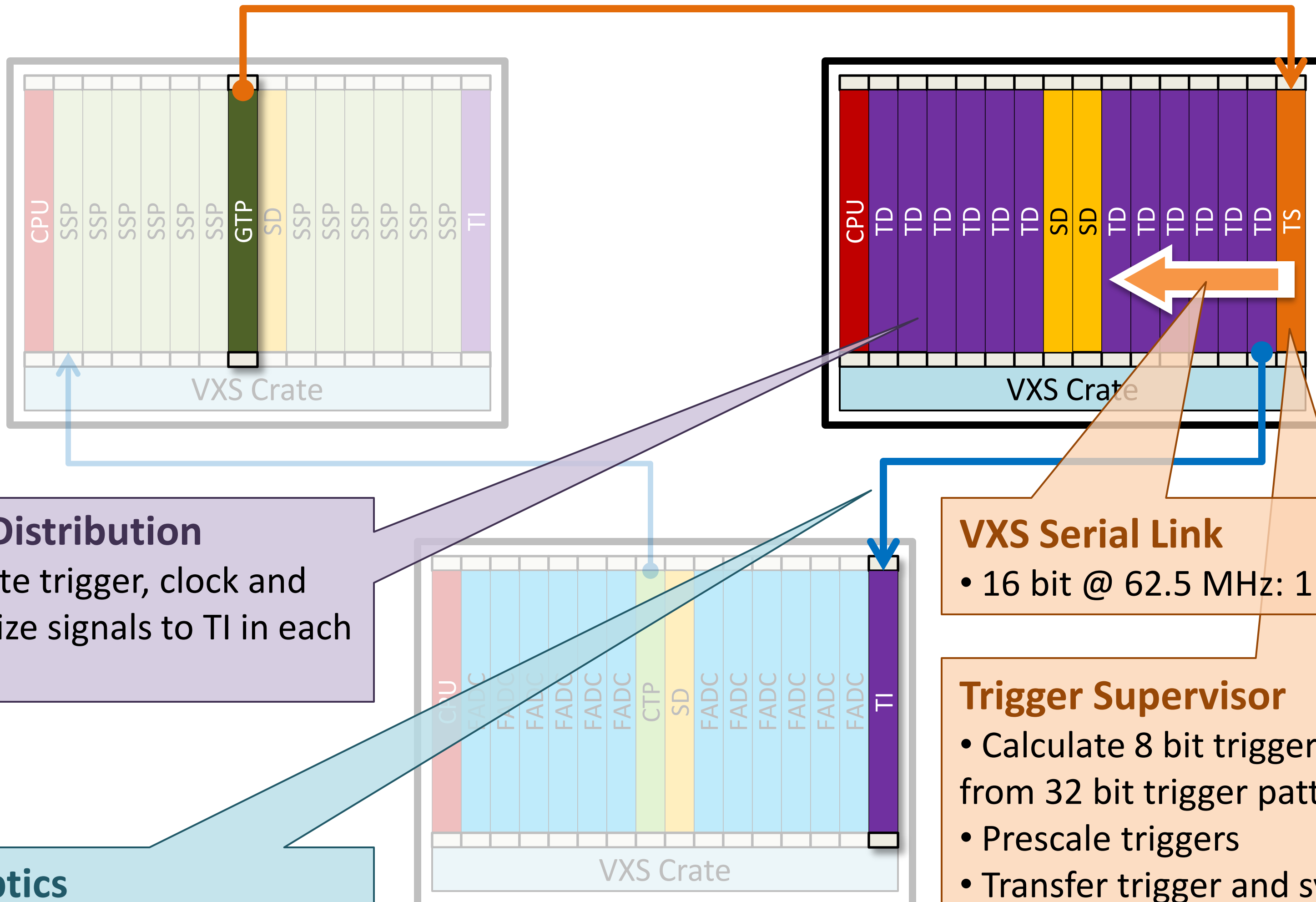


FADC125



F1-TDC

L1 Trigger Diagram



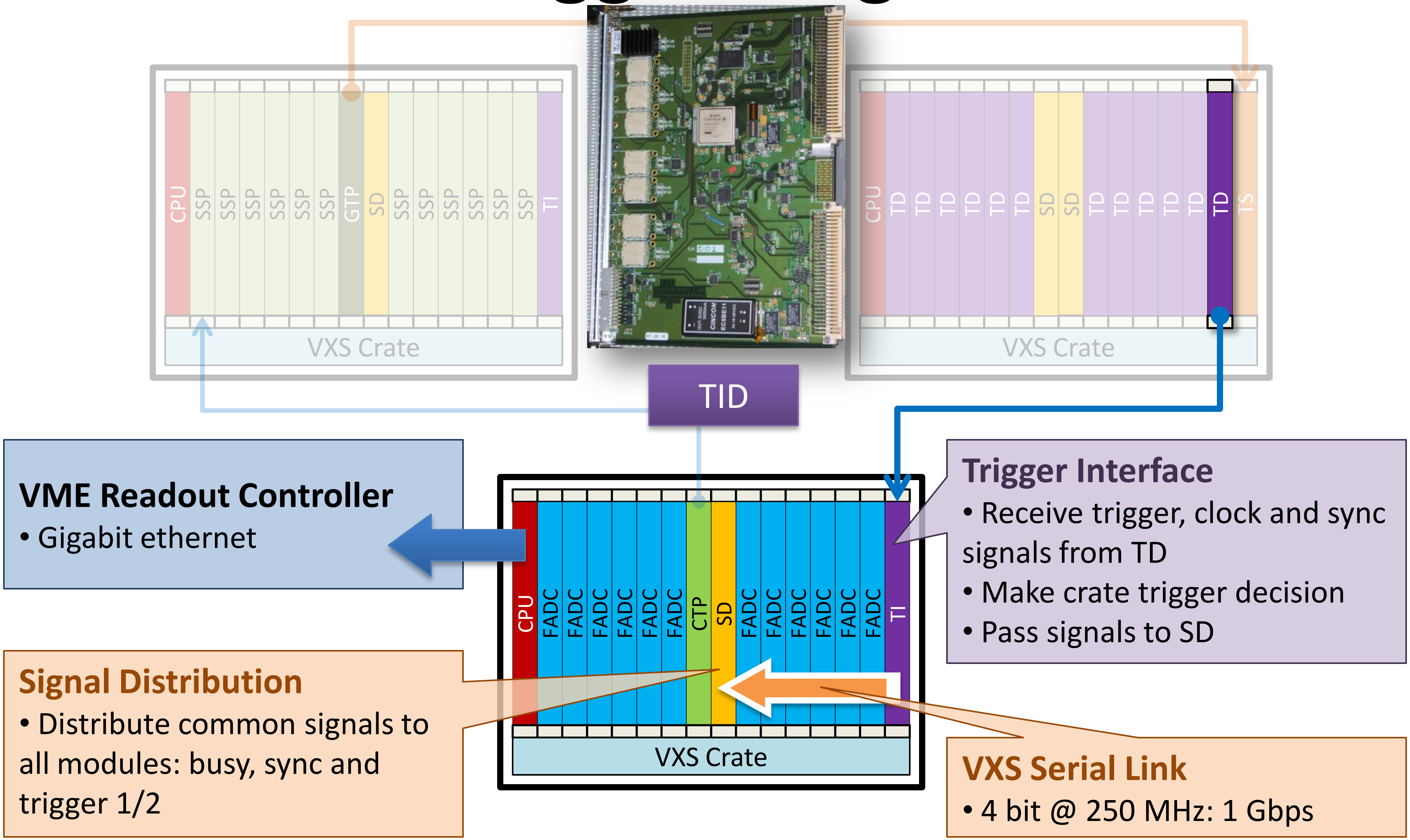
Trigger Distribution
- Distribute trigger, clock and synchronize signals to TI in each Crate

VXS Serial Link
- 16 bit @ 62.5 MHz: 1 Gbps

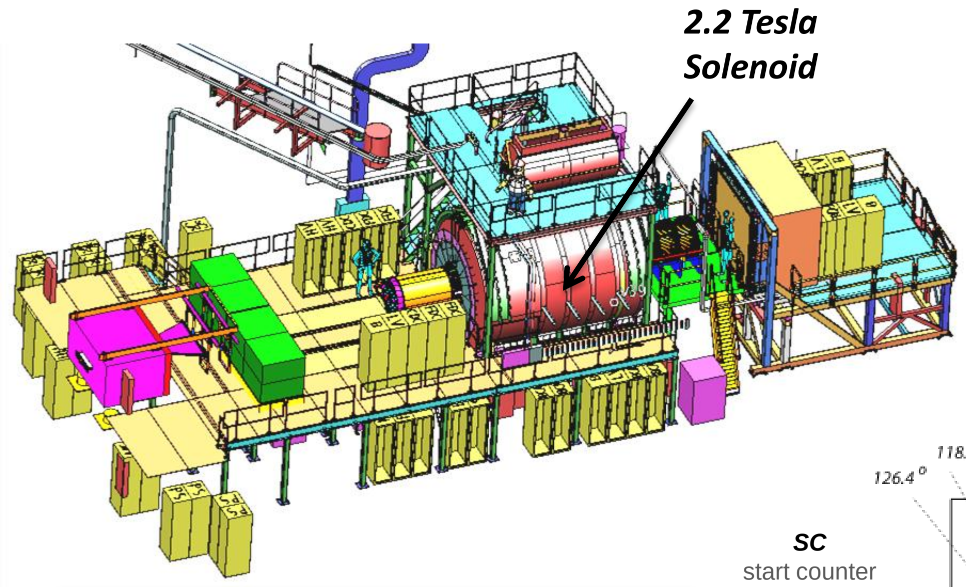
Trigger Supervisor
- Calculate 8 bit trigger types from 32 bit trigger pattern
- Prescale triggers
- Transfer trigger and sync signal to TD (16 bit total)

Fiber Optics
- 16 bit @ 62.5 MHz: 1 Gbps

L1 Trigger Diagram



The GlueX Detector

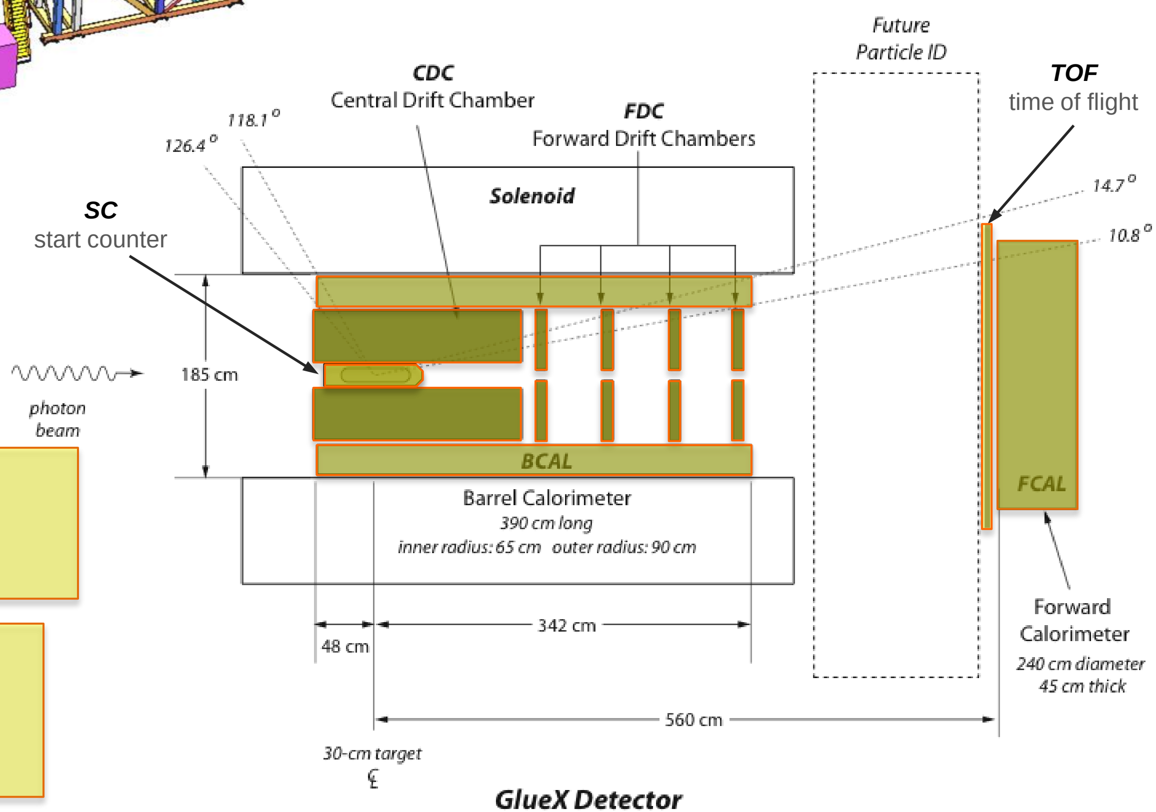


- 2.2T superconducting solenoidal magnet
- Fixed target (LH_2)
- 10^8 tagged γ/s (8.4-9.0GeV)
- hermetic

Charged particle tracking
- Central drift chamber (straw tube)
- Forward drift chamber (cathode strip)

Calorimetry
- Barrel Calorimeter (lead, fiber sandwich)
- Forward Calorimeter (lead-glass blocks)

PID
- Time of Flight wall (scintillators)
- Start counter
- Barrel Calorimeter



GlueX Data Rate

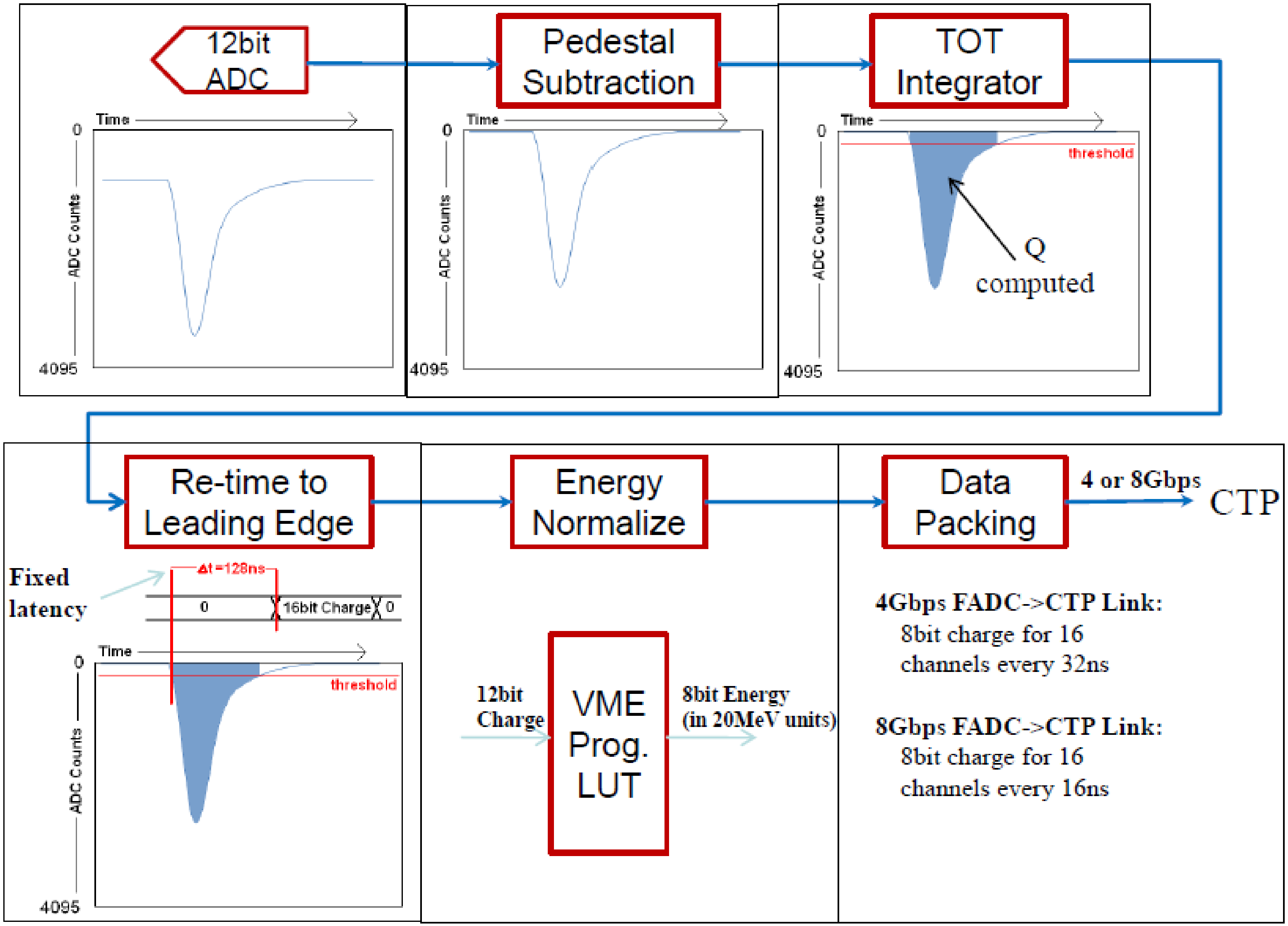
Lab		Front End DAQ Rate	Event Size	L1 Trigger Rate	Bandwidth to mass Storage	Source
JLab	GlueX	3 GB/s	15 kB	200 kHz	300 MB/s	private comm.
JLab	CLAS12	0.1 GB/s	20 kB	10 kHz	100 MB/s	private comm.
LHC	ALICE	500 GB/s	2,500 kB	200 kHz	200 MB/s	CHEP2007 talk Sylvain Chapelin
LHC	ATLAS	113 GB/s	1,500 kB	75 kHz	300 MB/s	CHEP2007 talk Sylvain Chapelin
LHC	CMS	200 GB/s	1,000 kB	100 kHz	100 MB/s	CHEP2007 talk Sylvain Chapelin
LHC	LHCb	40 GB/s	40 kB	1000 kHz	100 MB/s	CHEP2007 talk Sylvain Chapelin
BNL	STAR	50 GB/s	1,000 kB	0.6 kHz	450 MB/s	*
BNL	PHENIX	0.9 GB/s	~60 kB	~ 15 kHz	450 MB/s	**

* Jeff Landgraf Private Comm. 2/11/2010
** CHEP2006 talk MartinL. Purschke

CODA3 – What's different

CODA 2.5	CODA 3
Run Control (X, Motif, C++) (rcServer, runcontrol)	Experiment Control – AFECS (pure JAVA) (rcPlatform, rcgui)
Communication/Database (msql, cdev, dptcl, CMLOG)	cMsg – CODA Publish/Subscribe messaging
Event I/O C-based simple API (open/close read/write)	EVIO – JAVA/C++/C APIs Tools for creating data objects, serializing, etc…
Event Builder / ET System / Event Recorder (single build stream)	EMU (Event Management Unit) Parallel/Staged event building
Front-End – vxWorks ROC (Interrupt driven – event by event readout)	Linux ROC, Multithreaded (polling – event blocking)
Triggering: 32 ROC limit, (12 trigger bits -> 16 types) TS required for buffered mode	128 ROC limit, (32 trigger bits -> 256 types) TI supports TS functionality. Timestamping (4ns)

FADC Encoding Example



GTP Trigger Bit Example