SoLID DAQ for Transversity and PVDIS

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SoLID collaboration meeting

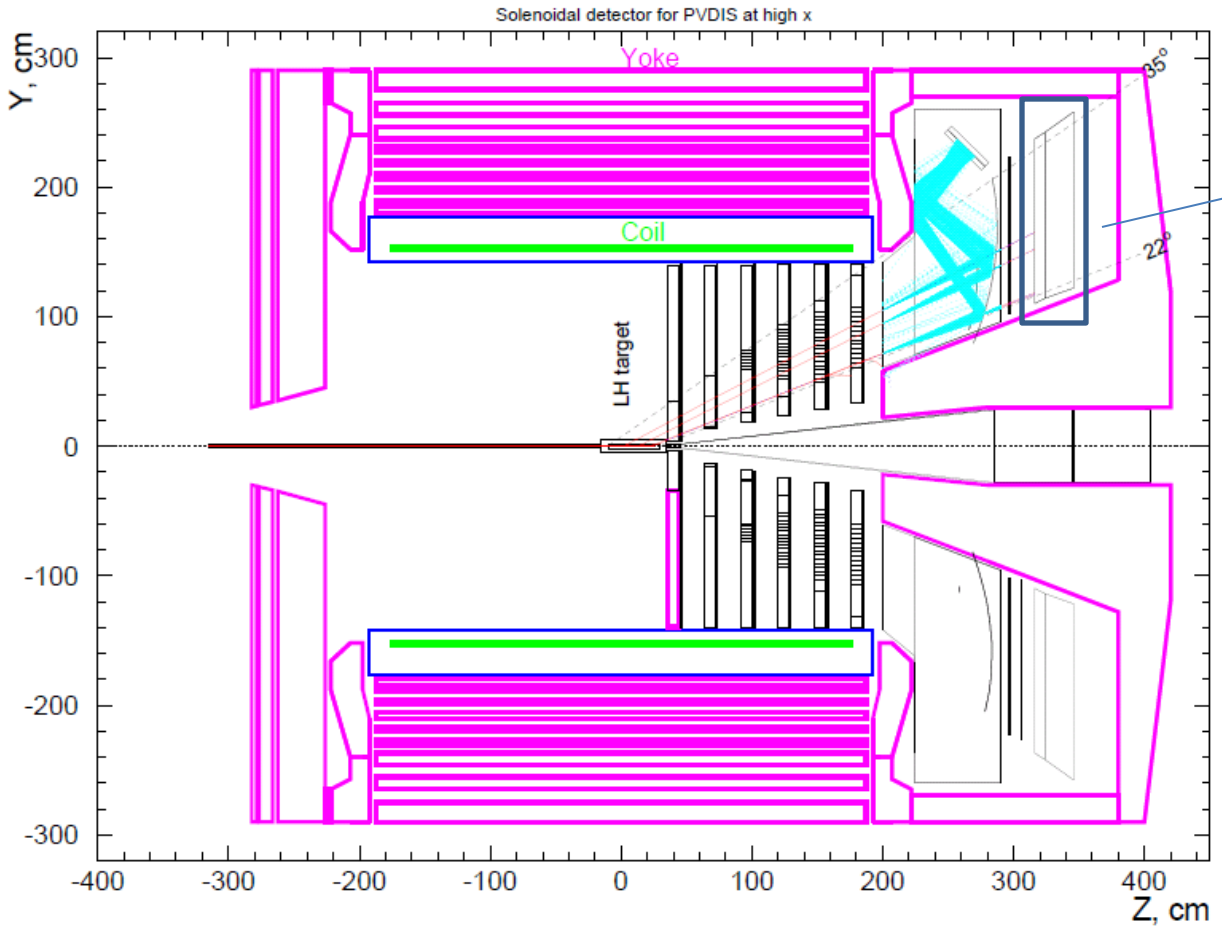
July 9th 2014

Outline

- Introduction
  - SoLID
  - JLAB Pipeline DAQ
  - GEM readout
- PVDIS
  - Calorimeter trigger
  - Trigger rates
  - Event sizes / data rates
- SIDIS
  - Electronics layout
  - Trigger rates
  - Event size / data rates
- Costs
- Tasks list
- Timeline
- Conclusion

SOLID OVERVIEW

Detector layout and trigger for PVDIS



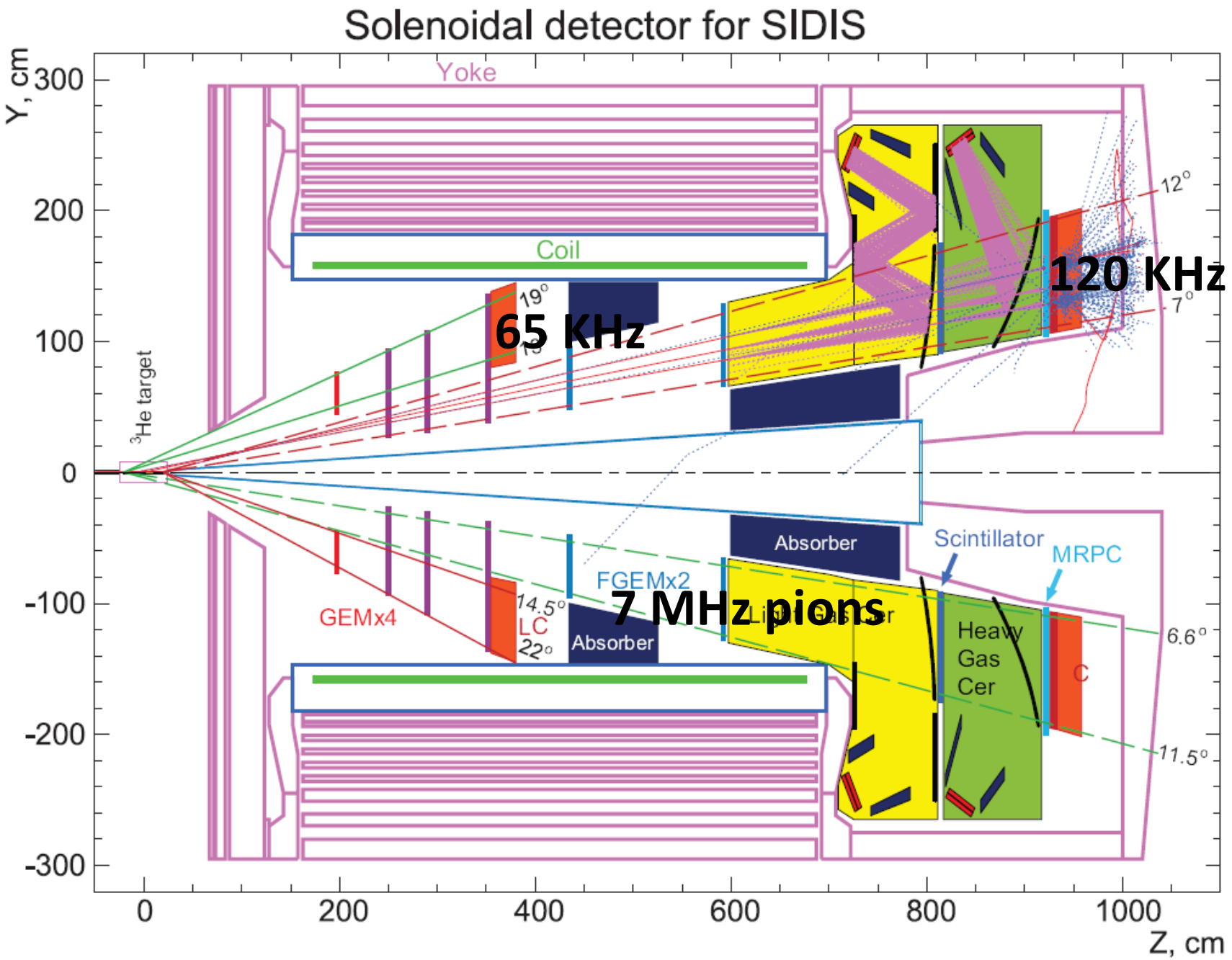
Trigger

Calorimeter and Gas Cerenkov

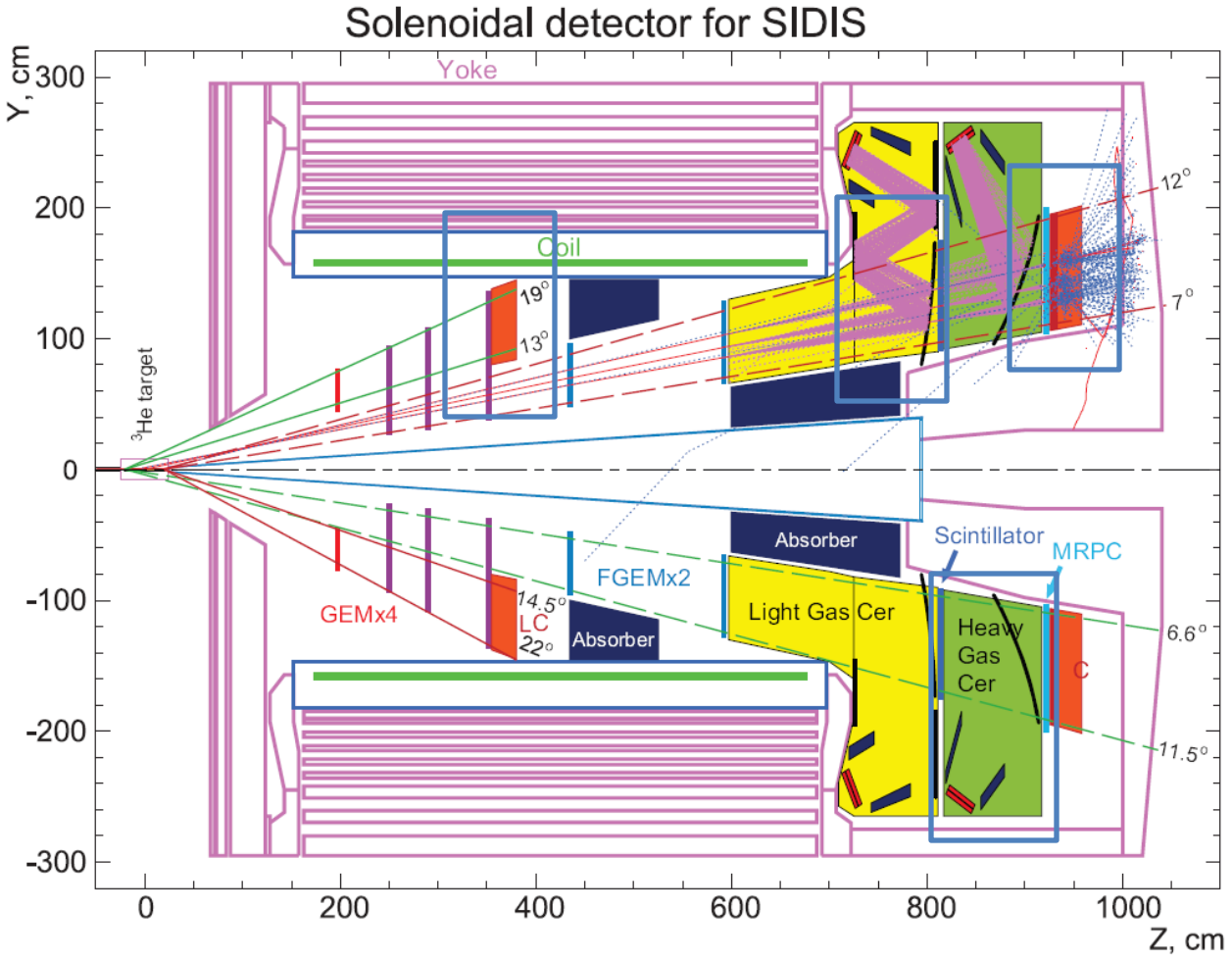
200 to 500 KHz of electrons

30 individual sectors to reduce rate

Max 25 KHz/sector


Solenoidal detector for SIDIS
Yoke
Coil
120 KHz
65 KHz
7 MHz pions
^{3}He target
19°
12°
7°
GEMx4
14.5°
LC
22°
FGEMx2
Absorber
Absorber
Scintillator
MRPC
Heavy
Gas
Cer
C
6.6°
11.5°
Y, cm
300
200
100
0
-100
-200
-300
0
200
400
600
800
1000
Z, cm

Detector layout and trigger for SIDIS



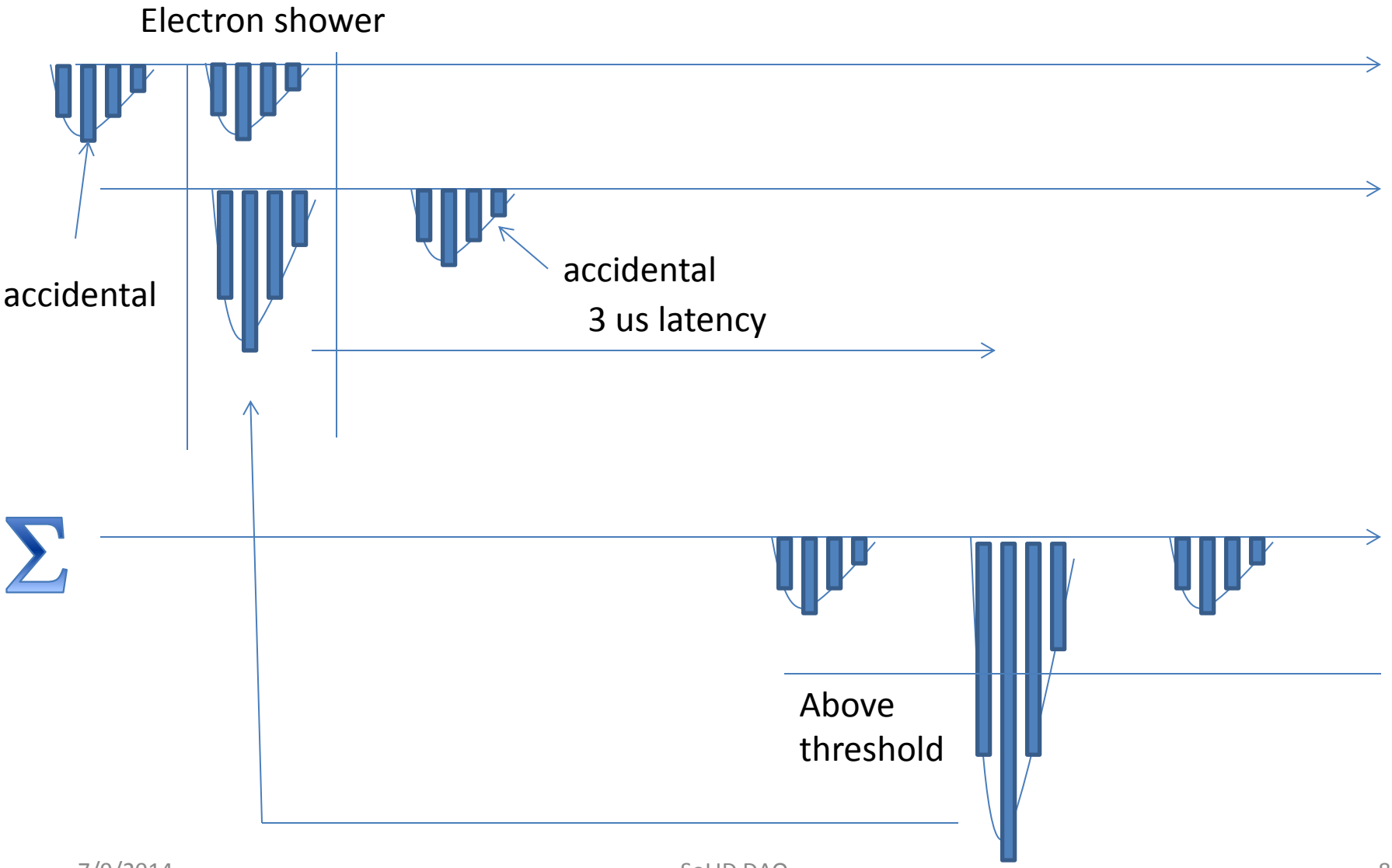
Trigger

Calorimeter
+
Cerenkov
+
MRPC

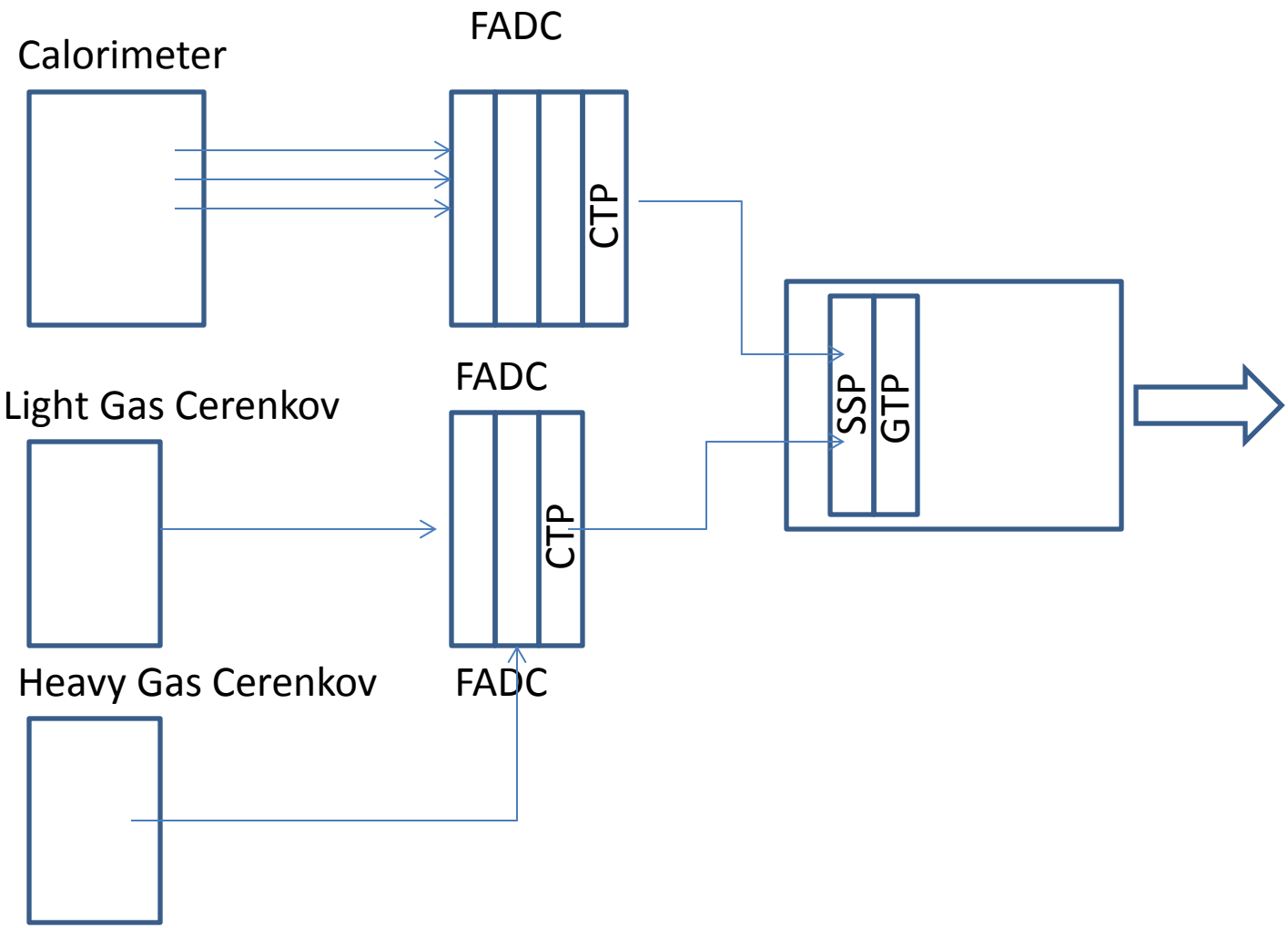
Coincidences and threshold for global 60 KHz trigger rates

Jefferson Laboratory Pipelined electronics with CODA 3

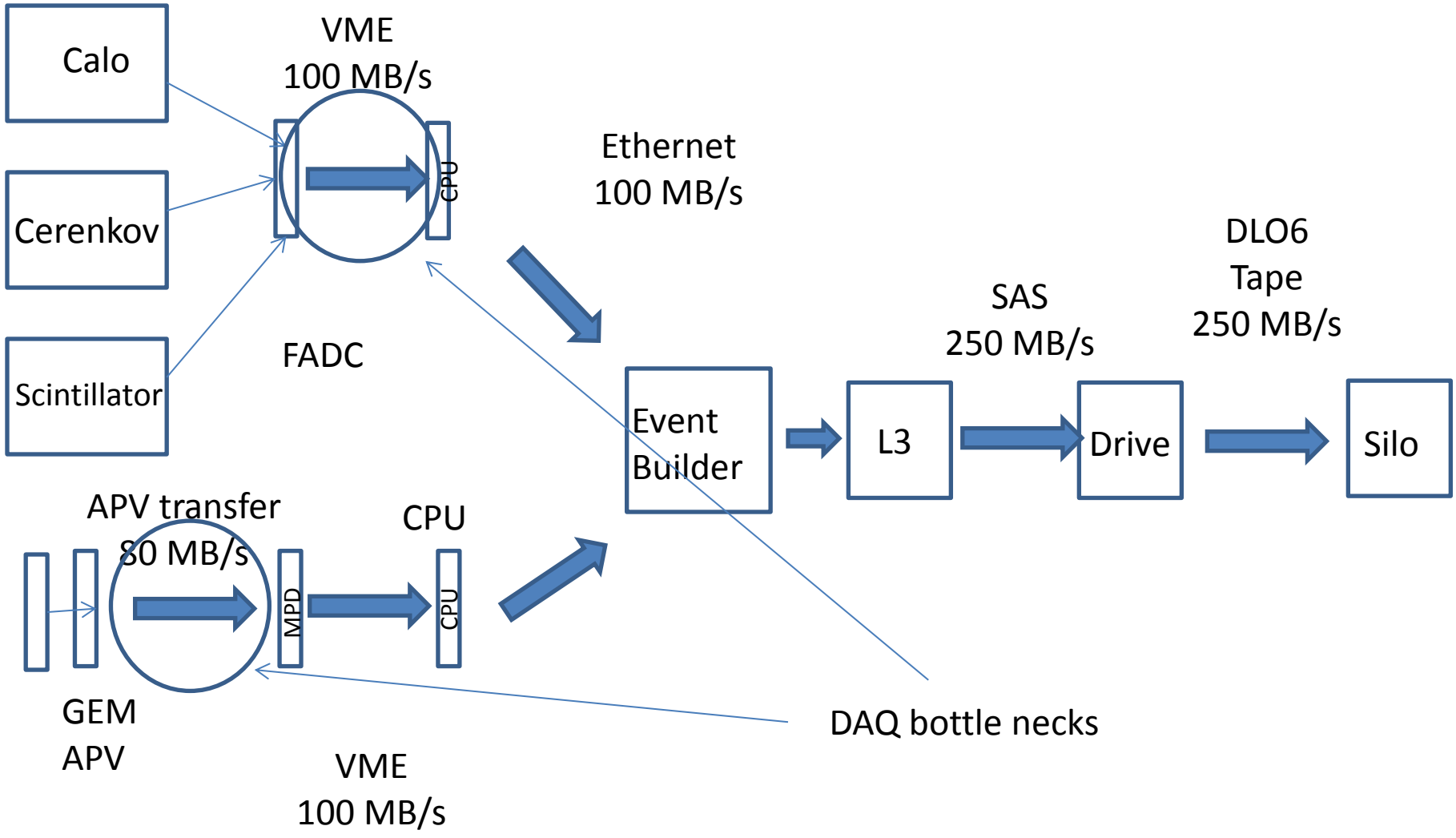
Pipelined Hall D DAQ



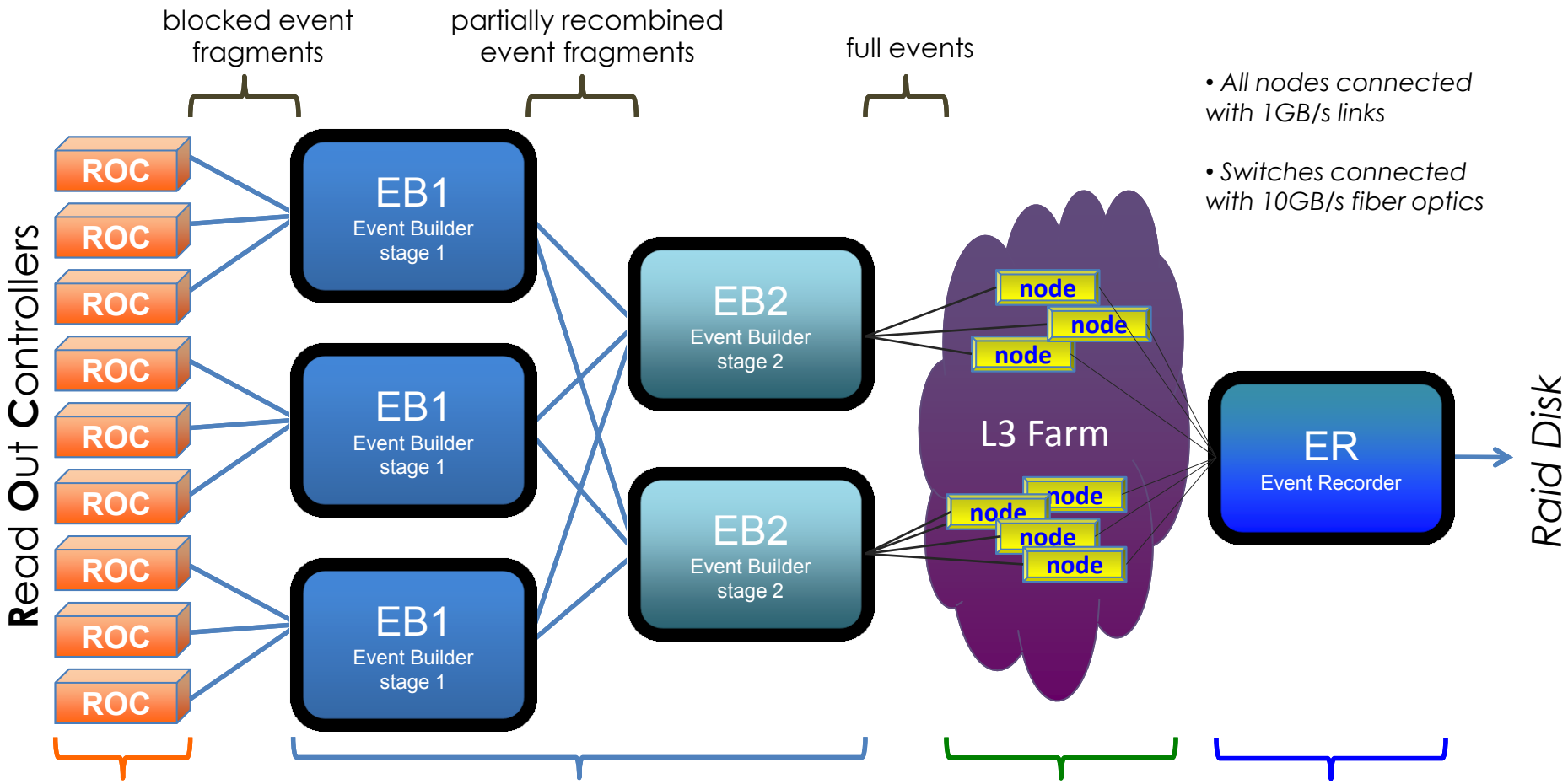
Pipelined Hall D DAQ



Data readout



L3 Farm


blocked event fragments
partially recombined event fragments
full events
• All nodes connected with 1GB/s links
• Switches connected with 10GB/s fiber optics
Read Out Controllers
ROC
ROC
ROC
ROC
ROC
ROC
ROC
ROC
ROC
EB1
Event Builder stage 1
EB1
Event Builder stage 1
EB1
Event Builder stage 1
EB2
Event Builder stage 2
EB2
Event Builder stage 2
node
node
node
L3 Farm
node
node
node
node
ER
Event Recorder
Raid Disk
Front-End Crates
~60 crates
~50MB/s out per crate
Staged Event Building
N x M array of nodes (exact number to be determined by available hardware at time of purchase)
Level-3 Trigger and monitoring
Event Recording
300MB/s in
300MB/s out

GEM READOUT

GEM readout

- APV25 Front GEM ASICs
- Up to 164 000 channels
- APV 25 : 128 channels
- Readout
  - VME based readout : 16 APV25 = 2048 channels
    (~ 10 $ / channels)
  - SRS readout : ethernet /PC based = 2048 channels
    (~ 3 $ / channels)
- 1 crate per sectors for FADC and GEM

APV25 readout

- Switch Capacitor Array ASICS with buffer length 192 samples at 40 MHz :
  4.8 us Look back 160 samples : 4 us

- Estimated occupancy : 220 hits per trigger, X Y data, 440 strips

GEM : 6 Layers 164 000 channels total, 28 000 channels per planes

Occupancy : 1.6 %

- APV readout time :

t_APV = 141 x number_of_sample / 40 MHz

t_APV(1 sample) = 3.7 us.

Max rate APV front end :

270 KHz in 1 sample mode

90 KHz in 3 samples mode

Will be triggered at max 60 KHz in 3 samples

100KHz Max in 1 sample

Deadtimeless electronics / parallel read and write

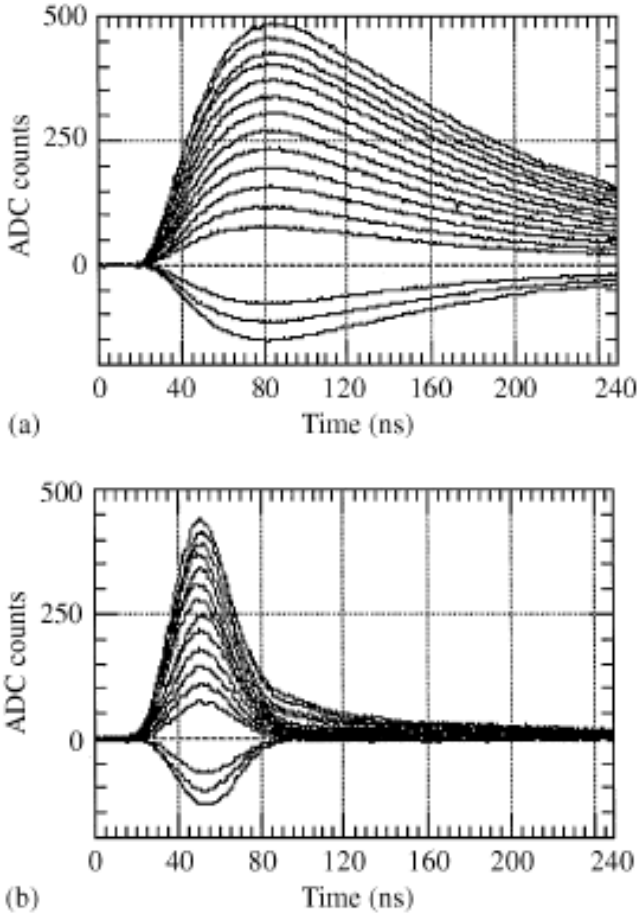


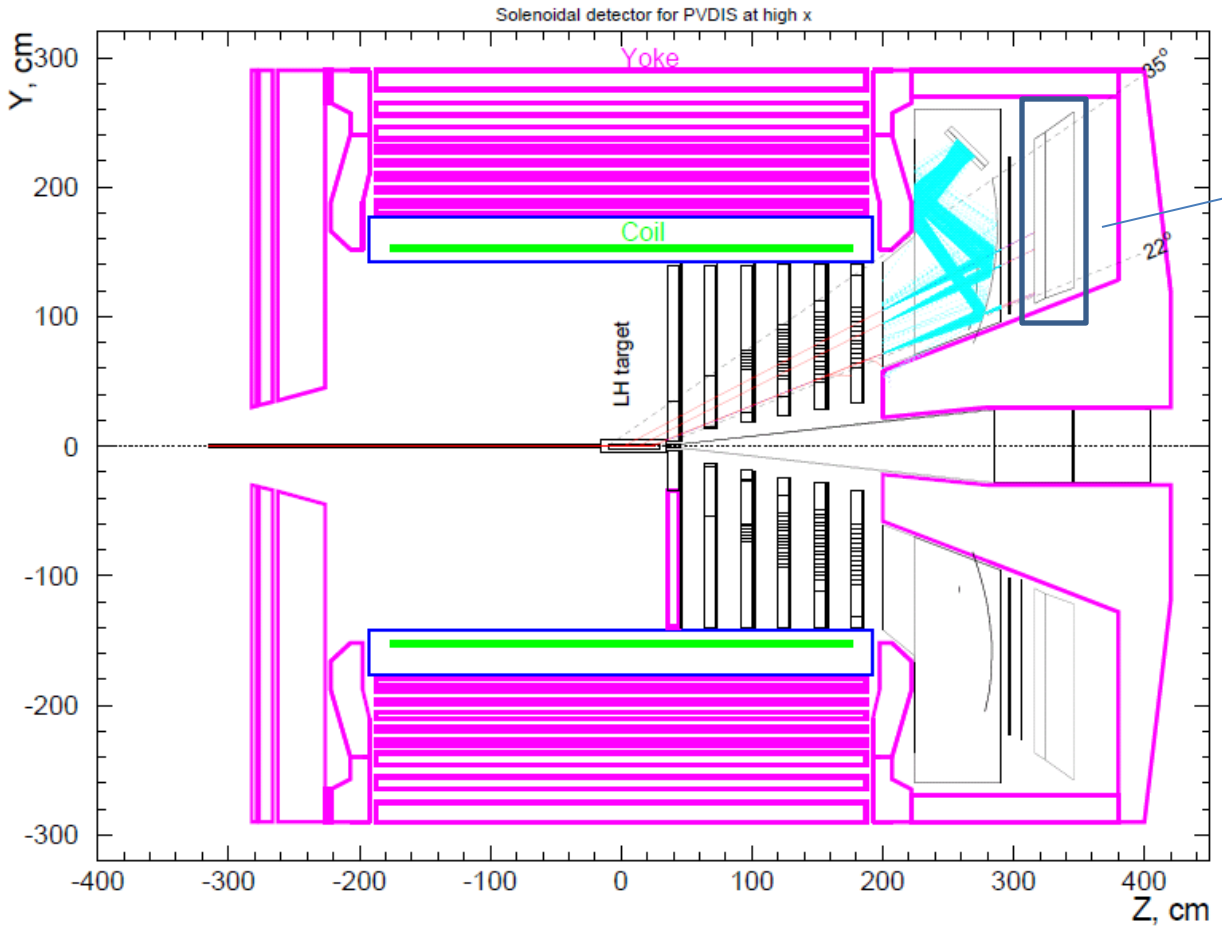
Fig. 5. Response curve of the APV25 as a function of the input signal. (a) Peak mode, (b) deconvolution mode.

Other GEM readout chips

- APV25 limiting factor
  - Need to confirm performance
  - Optimize hardware and readout
- Chip in development
  - CLAS12 Dream CEA/Saclay
  - ATLAS VMM1 BNL
  - gDSP
  - …
- SRS readout compatible with other chips
  - Ethernet + PC based

PVDIS

Detector layout and trigger for PVDIS



Trigger

Calorimeter and Gas Cerenkov

200 to 500 KHz of electrons

30 individual sectors to reduce rate

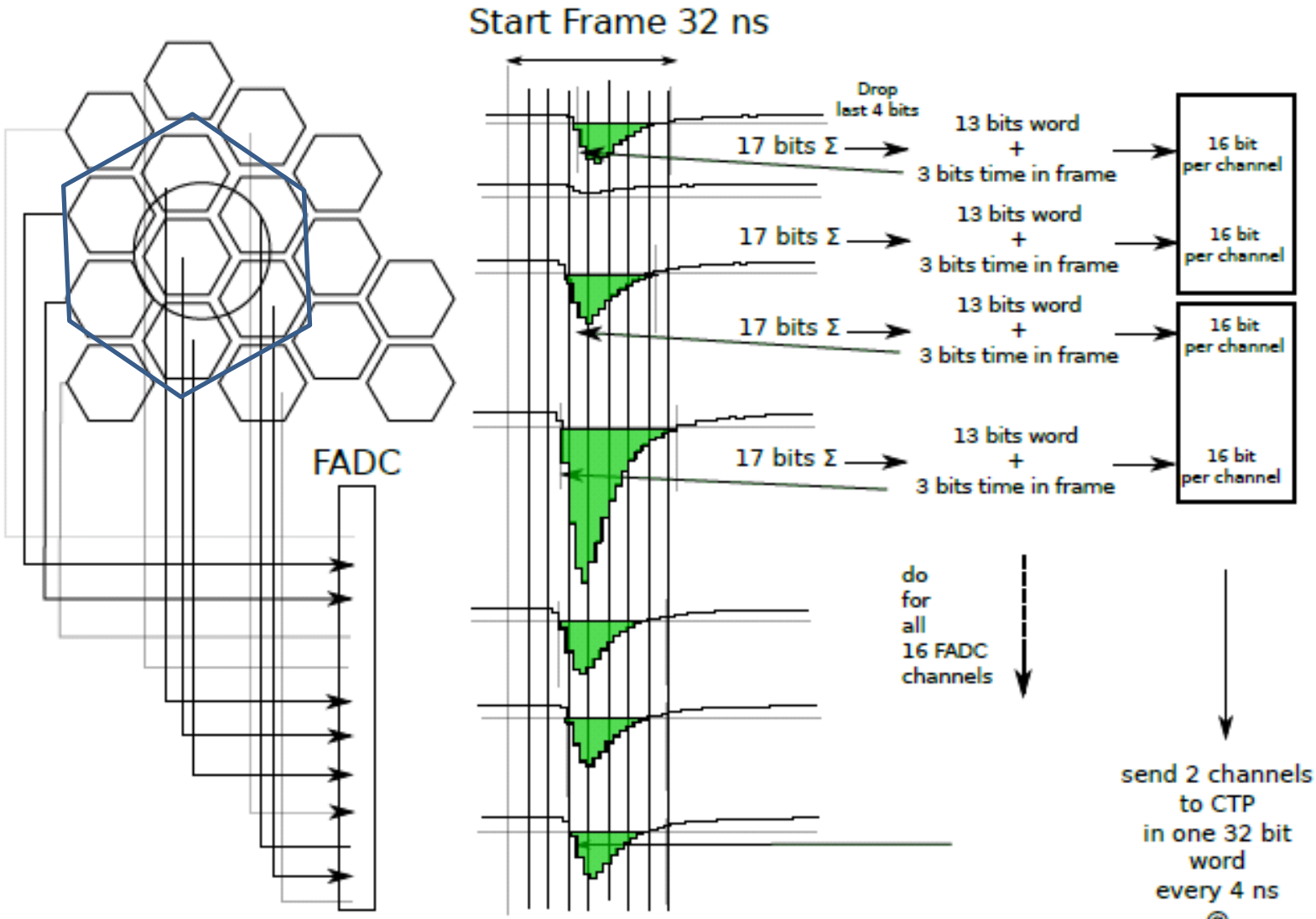
Max 30 KHz/sector

FADC readout

- FADC readout full waveform 10 samples
- Only want to readout FADC channel in the cluster to reduce number of channels readout because of background
- CTP generates a 64 bit pattern
- Send pattern to TI or FADC directly to trigger FADC

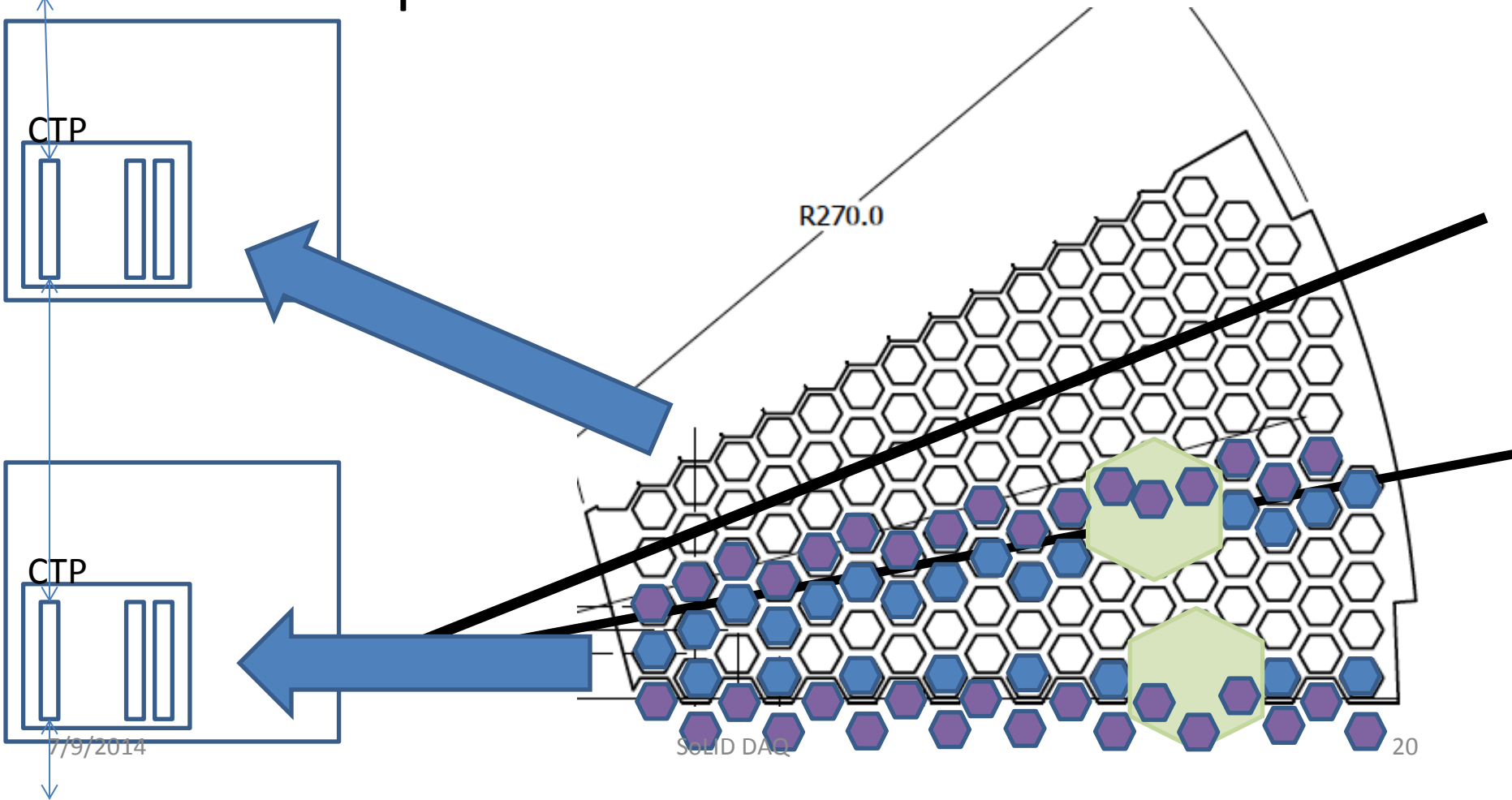
- Only channels from pattern are put in buffer

ECAL trigger

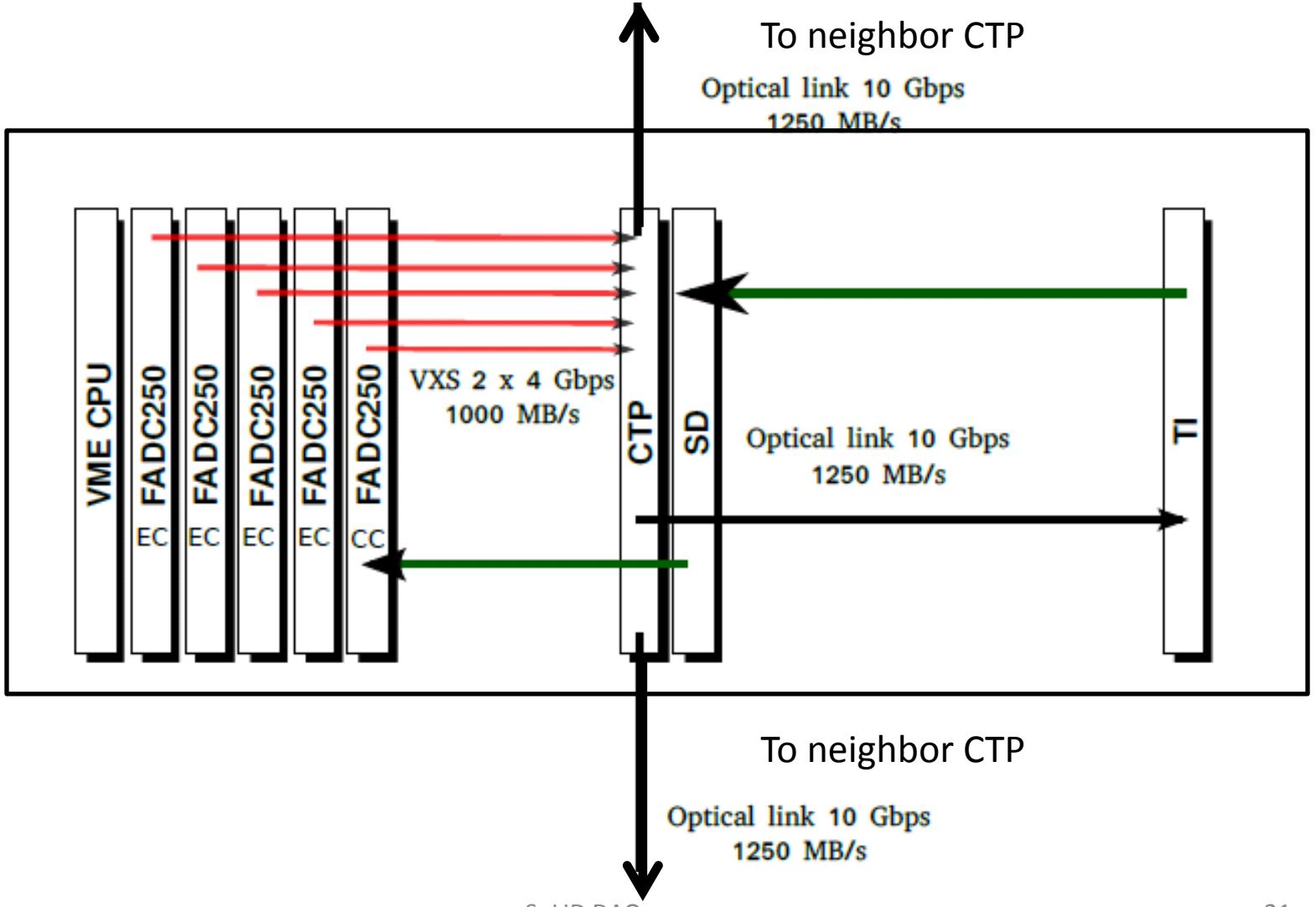


Calorimeter Geometry

- Detector segmented in 30 sectors
- One crate per sector

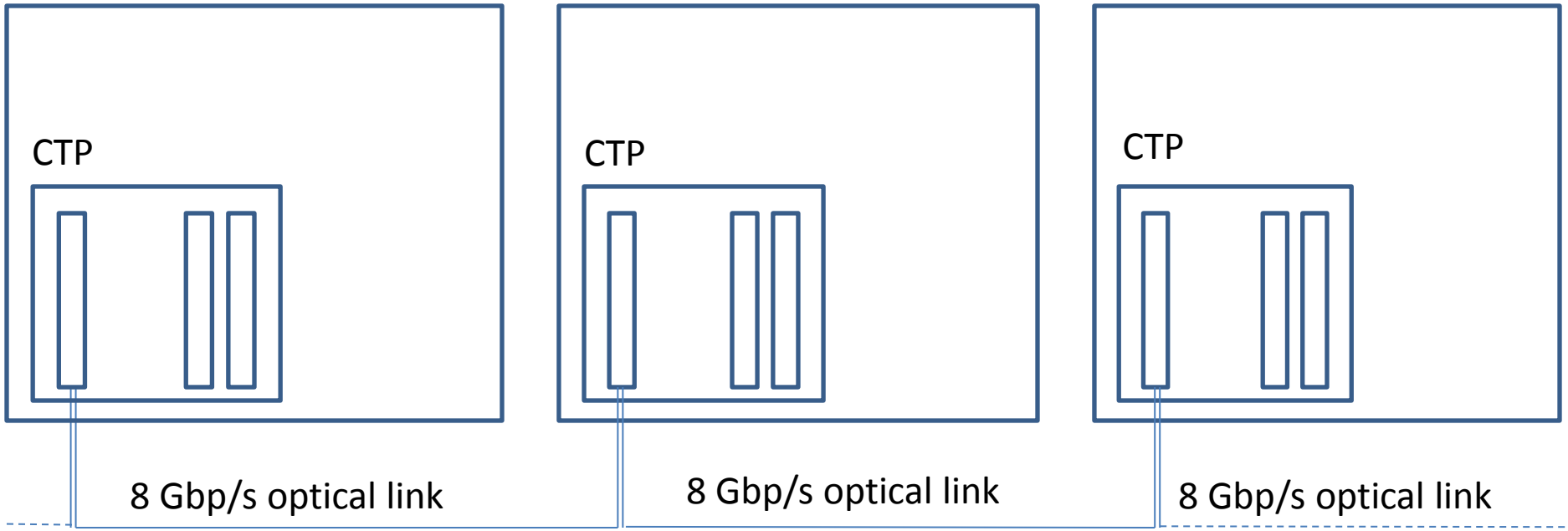


CTP connections



Neighboring sectors

New CTP : has two additionnal optical links
Can send Cerenkov and calorimeter edges to other sectors.



36 calorimeters
9 Cherenkov = 150ns overhead + 5 ns per m + 300 ns (data) = 500 ns

Trigger decision = 500 ns (Transfer) + 1us (clustering) < 4 us (APV)

Cerenkov L1 trigger

- 9 PMTs per sectors
- Correct gain per channel
- Look for channels above low threshold and coincidence between PMTs (more than one PMT hit usually)
- Sum of all channels with higher threshold

- Efficiency need to be studied

Event size FADC PVDIS with waveform

Detector	Total number of channels	Number of channels firing	Number of samples	Max size detector bytes	Minimal size detector bytes	Typical size
Shower	58	7	10	2784	336	**772**
Preshower	58	7	10	2784	336	**772**
Gas Cerenkov	9	3	10	432	144	**432**
			Max total size	46KB	0.816KB	**1.544KB**
Max rate	Assuming 100 MB/s per crate	One crate		2.1 KHz	121 KHz	**60 KHz**

FADC data rate for 30 KHz = 60 MB/s

GEM event occupancy and size

Sector	Rate	XY	Bytes	3 samples (bytes)
0	199	398	184	552
1	147	294	96	288
2	107	214	80	240
3	102	204	72	216
4	102	204	72	216
Total hits / sector	657		432	1296
Data rate / sector	30000		157680000	473040000
Data rate (sector Mb/s)			157,68	473.1
Total detector	19710		4730.4	14191.2
Occupancy detector	0.14			

- Data rate to front end reading 3 samples
- Use 4 Gigabit link = 512 MB/s not an issue with SRS

GEM event occupancy and size

Sector	Rate	XY	Bytes	3 samples (bytes)
0	23	46	184	552
1	12	24	96	288
2	10	20	80	240
3	9	18	72	216
4	9	18	72	216
Total hits / sector	63		504	1296
Data rate / sector	30000		1512000	77760000
Data rate (sector Mb/s)			15.12	45.36
Total detector	1620		453.6	1360.8
Occupancy detector	0.013			

- Rates with deconvolution 3 samples readout
- Data after processing going to tape

PVDIS electron trigger

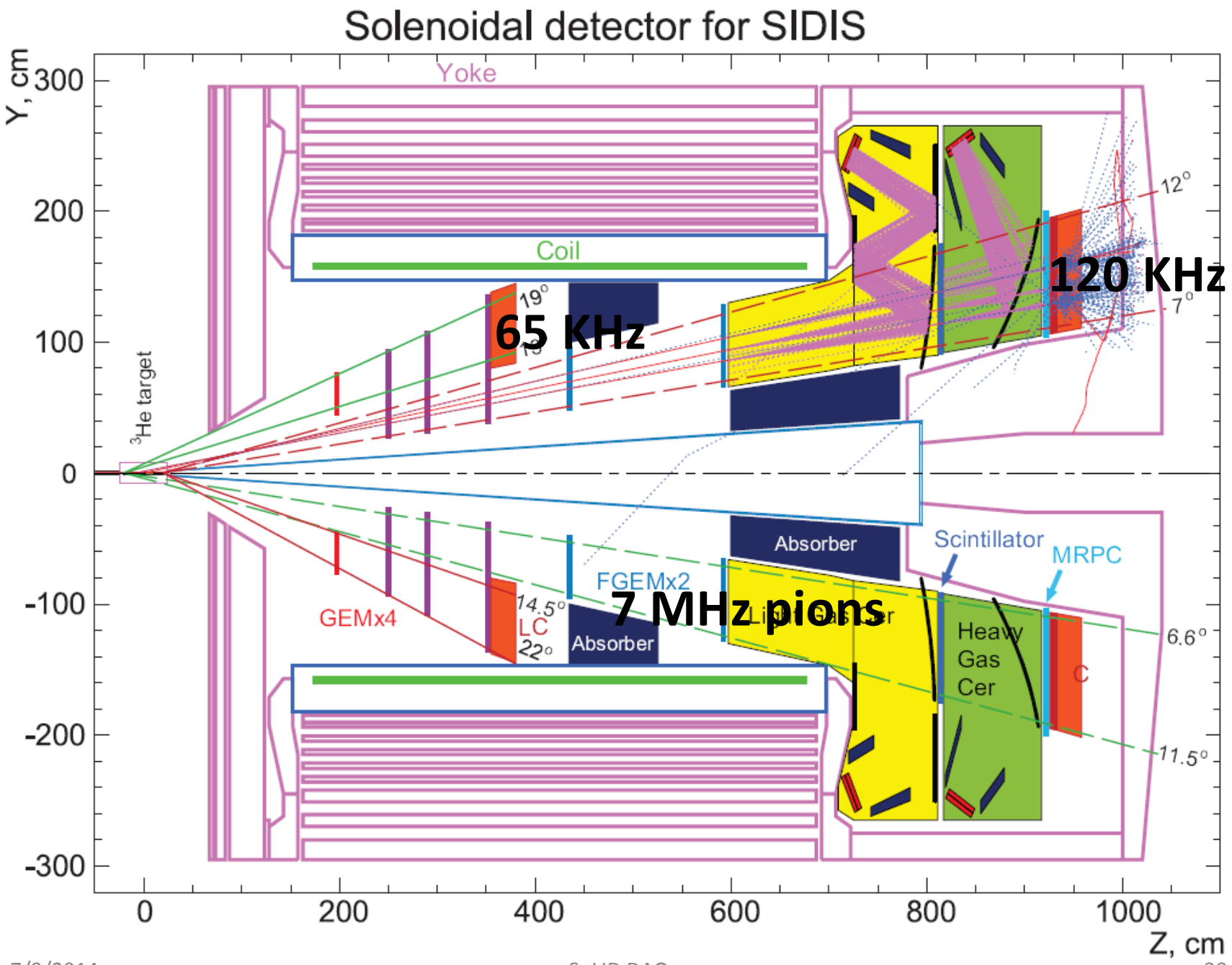
- Coincidence ECAL and Gas Cerenkov

Singles ECAL	290 KHz
Singles rates Cerenkov	1.9 MHz
Accidental 30 ns	16.5 KHz
DIS electron	8 KHz max
Total rate	**25 KHz**

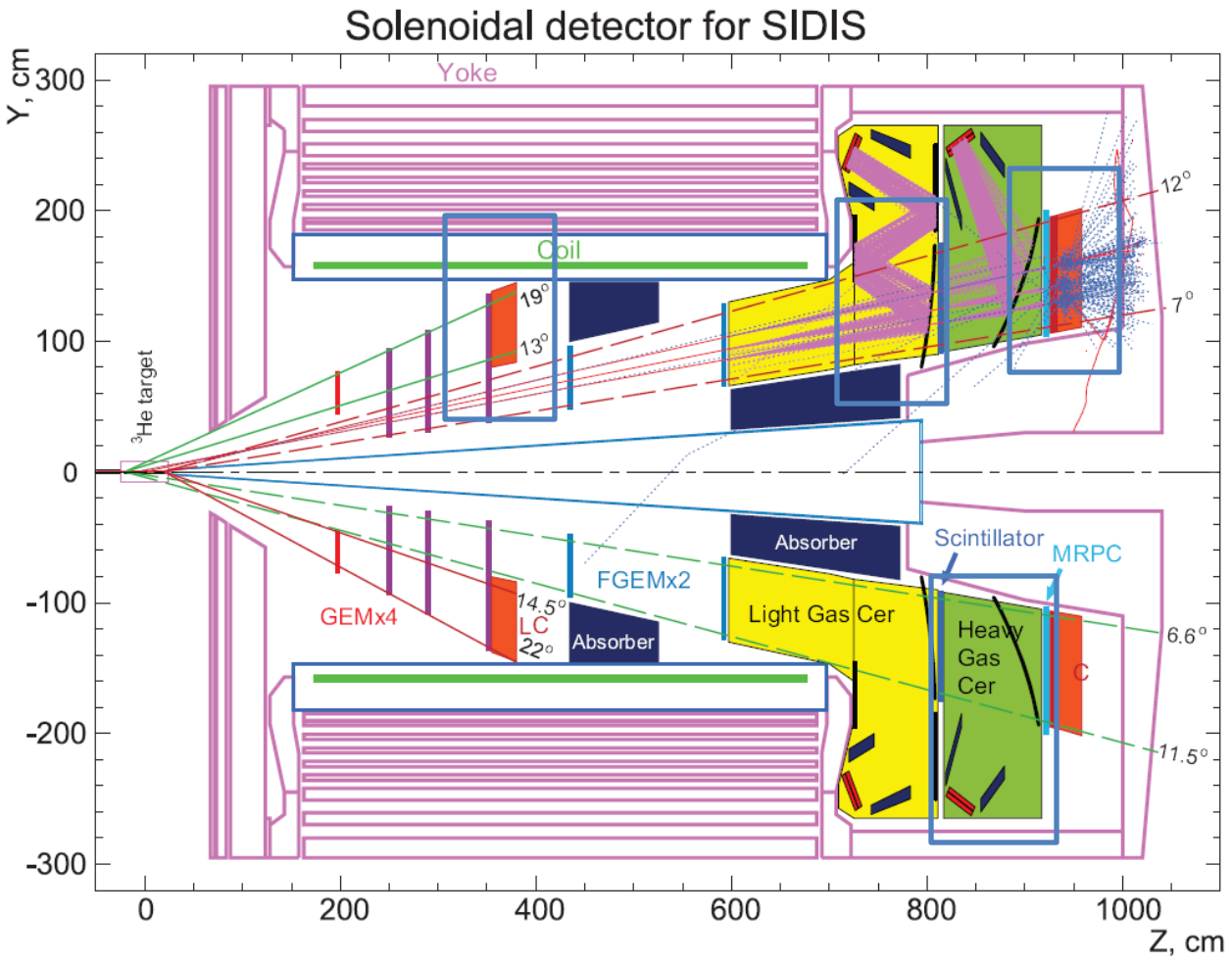
Summary PVDIS

- Simulation and trigger were checked and optimized
- Max trigger rate estimated to be 25 KHz
- GEM data rate assuming 30 KHz around 480 MB/s
- GEM data rate after deconvolution around 46 MB/s
- FADC data 60 MB/s
- Total about 108 MB/s to L3, total 3.24 GB/s
- Use L3 to reduce to 250 MB/s (similar to Hall D)

SIDIS


Solenoidal detector for SIDIS
Yoke
Coil
Absorber
Absorber
Scintillator
MRPC
FGEMx2
GEMx4
LC
Heavy
Gas
Cer
C
19°
14.5°
22°
12°
7°
6.6°
11.5°
65 KHz
120 KHz
7 MHz pions
^{3}He target
Y, cm
300
200
100
0
-100
-200
-300
0
200
400
600
800
1000
Z, cm

Detector layout and trigger for SIDIS



Trigger

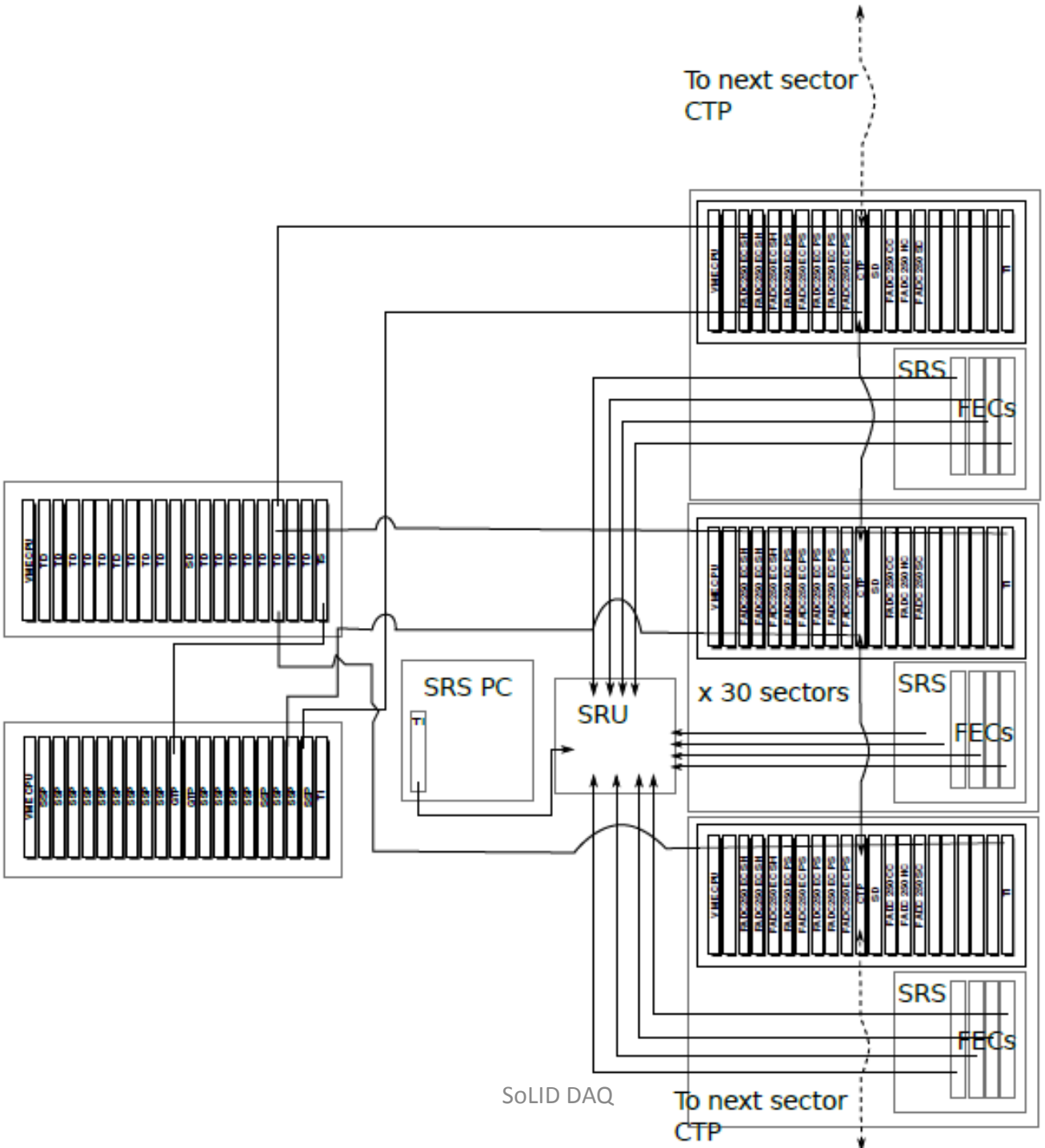
Calorimeter
+
Cerenkov
+
MRPC

Coincidences and threshold for global 60 KHz trigger rates

SIDIS channel count

Detector	Module type	Number of channels	Number of FADC
Forward Calorimeter	FADC	1150 x 2	144
Large angle calorimeter	FADC(+TDC)	450 x 2	57
Light Gas Cerenkov	FADC	120	8
Heavy Gas Cerenkov	FADC	270	17
Scintillator	FADC	120	8
MRPC	TRB3+Input Register	3300	30

The FADC of LC can be programmed to produce timing signals with ~400ps resolution (already demonstrated by simulation) to remove the needs of TDC.


To next sector
CTP
SRS
FECs
SRS PC
SRU
x 30 sectors
SRS
FECs
SRS
FECs
To next sector
CTP

SIDIS J/Psi

- Read integral and time
- Standard zero suppression
- J/Psi, look for two clusters instead of one for trigger close to SIDIS trigger
- Trigger of a few KHz

SIDIS: Coincidence @ 30 ns window

- Assuming a 30 ns gate
- Coincidence rate: 14MHz x 155.5KHz x 30 ns = 65.2 kHz
- Total with 4 KHz Physics = 70 KHz
- Given the safety margin, expected to handle about 100 KHz.
  - Include some single trigger to study detector performance etc.

MRPC readout

- 1550 detectors = 3300 channels
- Rutgers proposes use GSI TRB3
  - 10 ps resolution 256 channels around 3.5 K$
  - Front end PADIWA amplifier discriminator 200 $ for 16 channels

- VETROC trigger interface board to put signal in L1 trigger

GEM event occupancy and size

Sector	Rate	XY	Bytes	3 samples (bytes)
0	1	2	8	24
1	2	4	16	48
2	1	2	8	24
3	1	2	8	24
4	1	2	8	24
5	1	2	8	24
Total hits / sector	7	14	56	1296
Total detector	210	420	1680	5040
Data rate / sector			168000000	504000000
Data rate (sector Mb/s)			168	504
Occupancy detector	0.0015			

- Using deconvolution gives 168 MB/s for 100 KHz

FADC data

Detector	Rate	Hits	Type	Data Size per hit
LC	120 kHz	1	Energy, Hits	8 Byte x 2 (PS/SH)
FC	200 MHz	10	Energy, Hits	8 Byte x 2 (PS/SH)
LGC	40 MHz	3	Energy, Hits	8 Byte x 2 (split)
HGC	60 MHz	4	Energy, Hits	8 Byte x 2 (split)
MRPC	850 MHz	45	Hits	4 Byte
SC	300 MHz	15	Energy, Hits	8 Byte
Total				2.04kB

204 MB/s at 100 KHz

Summary SIDIS

- Readout only one sample, time and integral for GEM and FADC
- 70 KHz coincidence rate
- Design for 100 KHz gives 368 MB/s to L3 need less than factor 2 reduction
- Study feasibility to take all singles (150 KHz) should be doable but need more L3 processing power

ELECTRONICS LAYOUT AND BUDGET

Electronics

Module	Unite price	Quantity	
FADC 250	4500	287	$1,291500
Input register	2000	41	$82,000
CTP	7000	30	$210,000
SSP	5000	4	$20,000
GTP	5000	1	$5,000
VXS crate	15000	32	$480,000
TS	3500	1	$3,500
TI	3000	61	$90,000
TD	3000	16	$12,000
SD	2500	31	$75,000
VXS crate	11500	32	$345,000
VME CPU	3400	32	$105,400
SRS computer	3000	30	$60,000
		Total detectors	$2,949,300

Request

Assume use spares and additionnal FADC available : 230 units

Module	Unite price	Quantity	
FADC 250	4500	57	$256,500
Input register	2000	41	$82,000
CTP	7000	30	$210,000
SSP	5000	4	$20,000
GTP	5000	1	$5,000
VXS crate	15000	32	$480,000
TS	3500	1	$3,500
TI	3000	61	$90,000
TD	3000	16	$12,000
SD	2500	31	$75,000
VXS crate	11500	32	$345,000
VME CPU	3400	32	$105,400
SRS computer	3000	30	$60,000
		Total detectors	$1.922,300

Man power rough estimate

- JLAB
  - Alexandre Camsonne
  - Yi Qiang
- Umass
  - Rory Miskimen
  - Students can be available for electronics works at UMass
- Rutgers
  - Ron Gilman

  MRPC readout

		Year 1	Year 2	Year 3	Year 4	Year 5
1 postdoc		Test stand	Test stand	Full electronics	Electronics cabling	Experiment
1 student		Test stand	Test stand	Full electronics	Electronics cabling	Experiment
1 tech		Rack		Rack,cables,weldment	Electronics / detector cabling	
DAQ		Support	Support	Support	Support	
Designer		Layout	Layout			
Electronics		Trigger	Trigger	Support	Support	Support

Man power rough budget

FTE		Year 1	Year 2	Year 3	Year 4	Year 5
1 postdoc		0.5	0.5	0.5	0.5	0.5
1 student		0.5	0.5	0.5	0.5	0.5
1 tech		0.05		0.3		
DAQ		0.1	0.1	0.1	0.1	
Designer		0.1	0.1			
Electronics		0.1	0.1	0.05	0.05	0.05

K$		Year 1	Year 2	Year 3	Year 4	Year 5
1 postdoc		35	35	35	35	35
1 student		25	25	25	25	25
1 tech		3.5	0	21	0	0
DAQ		8	8	8	8	0
Designer		8	8	4	4	4
Electronics		8	8	4	4	4
Total		**87.5**	**84**	**97**	**76**	**68**

about 450 K$ total including inflation

HV and cables

Calorimeter shower	FADC	1830
Large angle calorimeter preshower	FADC	114.375
Forward angle calorimeter preshower	FADC	0
SPD	FADC	18.75
Light Gas Cerenkov		270
Heavy Gas Cerenkov		480
Total		2714

HV and cables

	Total	Needed	Cost
Cables	2714	714	27 K$
HV boards	113	30	194 K$
HV mainframe	17	5	57 K$
		Total	278 K$

Assume we can reuse 2000 HV channels so need around 714 channels

Tape size

		Days	Data rate	Seconds	Total data TB	Double	DLO5 in $	DLO6 in $
E12-11-108	Pol proton	120	250	10368000	2592	5184	259200	155520
E12-12-006	J/Psi	60	250	5184000	1296	2592	129600	77760
E12-10-006	Transv. Pol. 3He	90	250	7776000	1944	3888	194400	116640
E12-11-007	Long. Pol. 3 He	35	250	3024000	756	1512	75600	45360
E12-10-007	PVDIS	169	250	14601600	3650.4	7300.8	365040	219024
	Total	474		40953600	10238.4	20476.8	1023840	614304

Tasks

- Hardware
  - Trigger design
  - Electronics performance testing
  - Shielding
  - Cabling layout / installation
  - L3 / event filtering
- Simulation
  - Radiation and shielding
  - Background in detector event size
  - Background in detector event/trigger rates
  - Trigger simulation for logic and timing

DAQ Test stand

- Ordered parts / collaboration with Hall A Compton
  - 2 VXS crates
  - 4 FADC
  - 1 CTP, 1SSP
  - 4 Intel VME CPUs
- CODA3 still in the work : test L3 Farm

Time line

- 2012
  - UMASS Hall D test stand (380 FADC to be tested)
  - 4 JLAB FADC250
  - VXS crate
- 2013
  - MPD and SRS system first tests
- 2014
  - Small scale setup for testing : FADC + trigger + APV25
  - DVCS : test Intel VME CPU for large amount of data
- 2015
  - HCAL Trigger development (SBS funding accepted)
  - Full experiment scale system in place
- 2016-2018
  - Detector cabling and testing

Conclusion

- SoLID requires high rates low dead time, flexible trigger capability
- Rates optimization for SIDIS but push for highest rate depending of GEM chip performances
- GEM electronics R&D
- Background and trigger rates where checked and close proposal, data rates are sustainable by the DAQ hardware
- Hall D electronics perfectly suited
  - Total cost around 2 M$

Backup slides

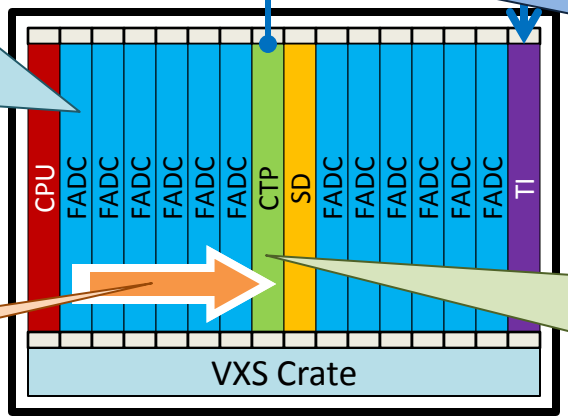
L1 Trigger Diagram

SSP

CTP

FADC250
- 12 bit @ 250 MHz, 16 ch
- Sums amplitude from all channels
- Transfer total energy or hit pattern to CTP

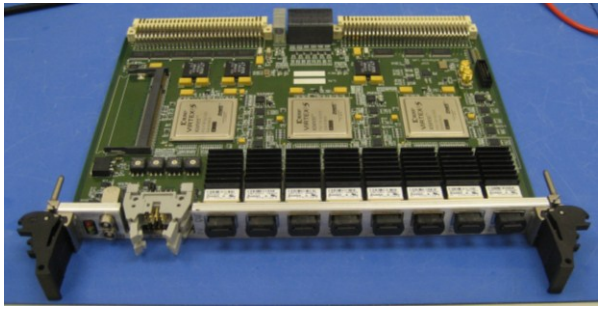
Fiber Optics
- 64 bit @ 125 MHz



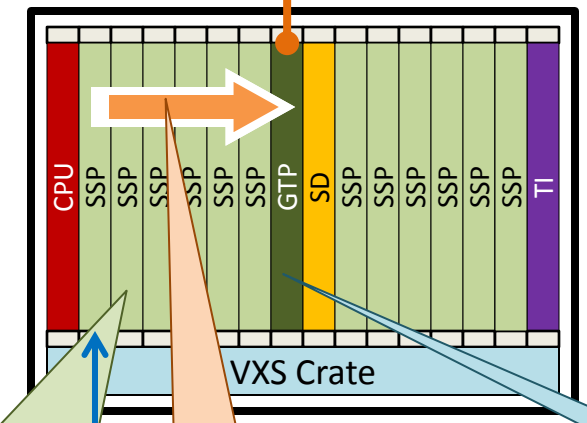
VXS Serial Link
- 16 bit @ 250 MHz: 4 Gbps

Crate Trigger Processor
- Sums energies from FADCs
- Transfer total energy or hit pattern to SSP

L1 Trigger Diagram



SSP



TS

CTP

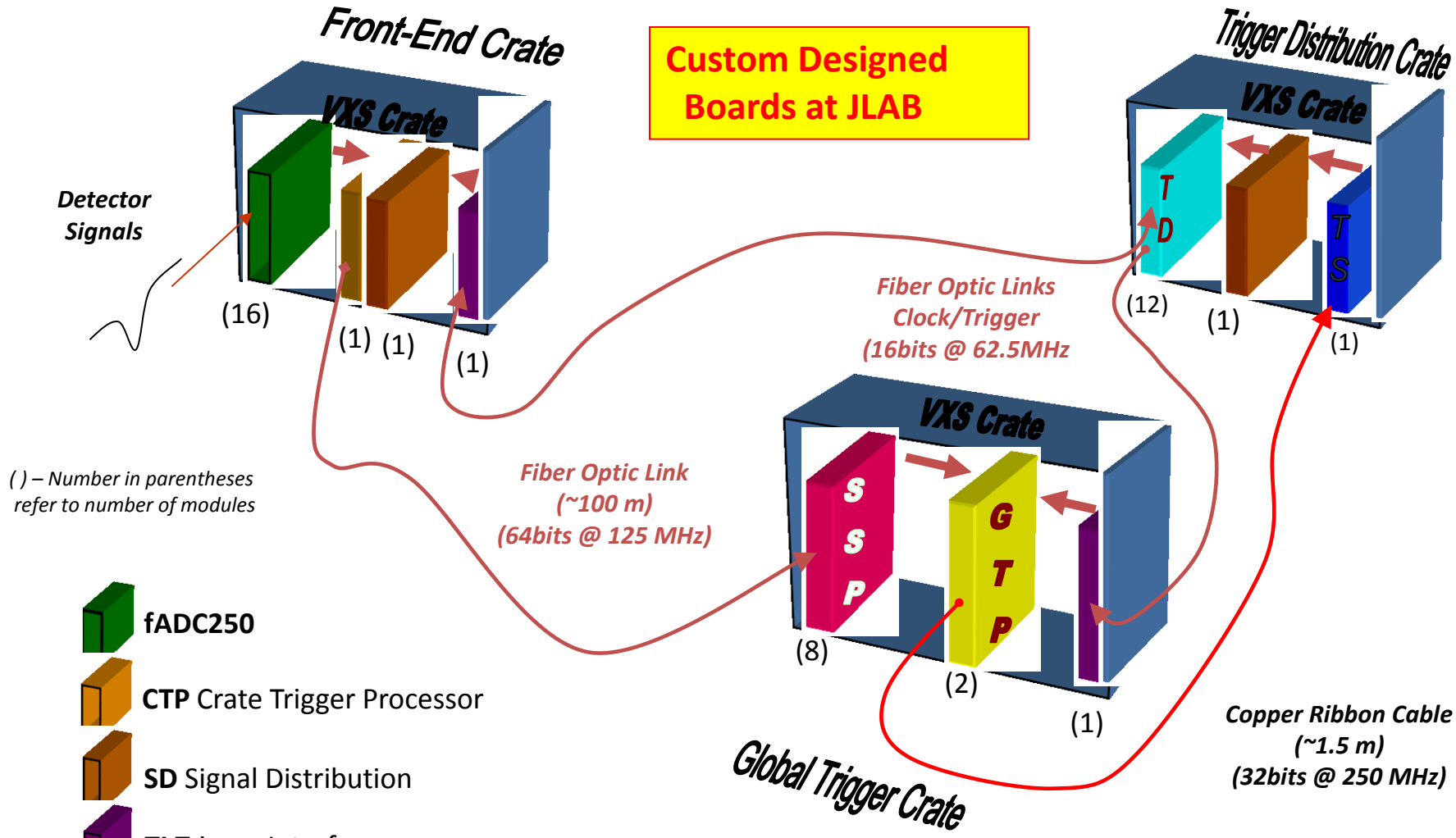
Sub-System Processor
- Consolidates multiple crate subsystems
- Report total energy or hit pattern to GTP

VXS Serial Link
- 32 bit @ 250 MHz: 8 Gbps

Copper Ribbon Cable
- 32 bit @ 250 MHz: 8 Gbps

Global Trigger Processor
- Collect L1 data from SSPs
- Calculate trigger equations
- Transfer 32 bit trigger pattern to TS

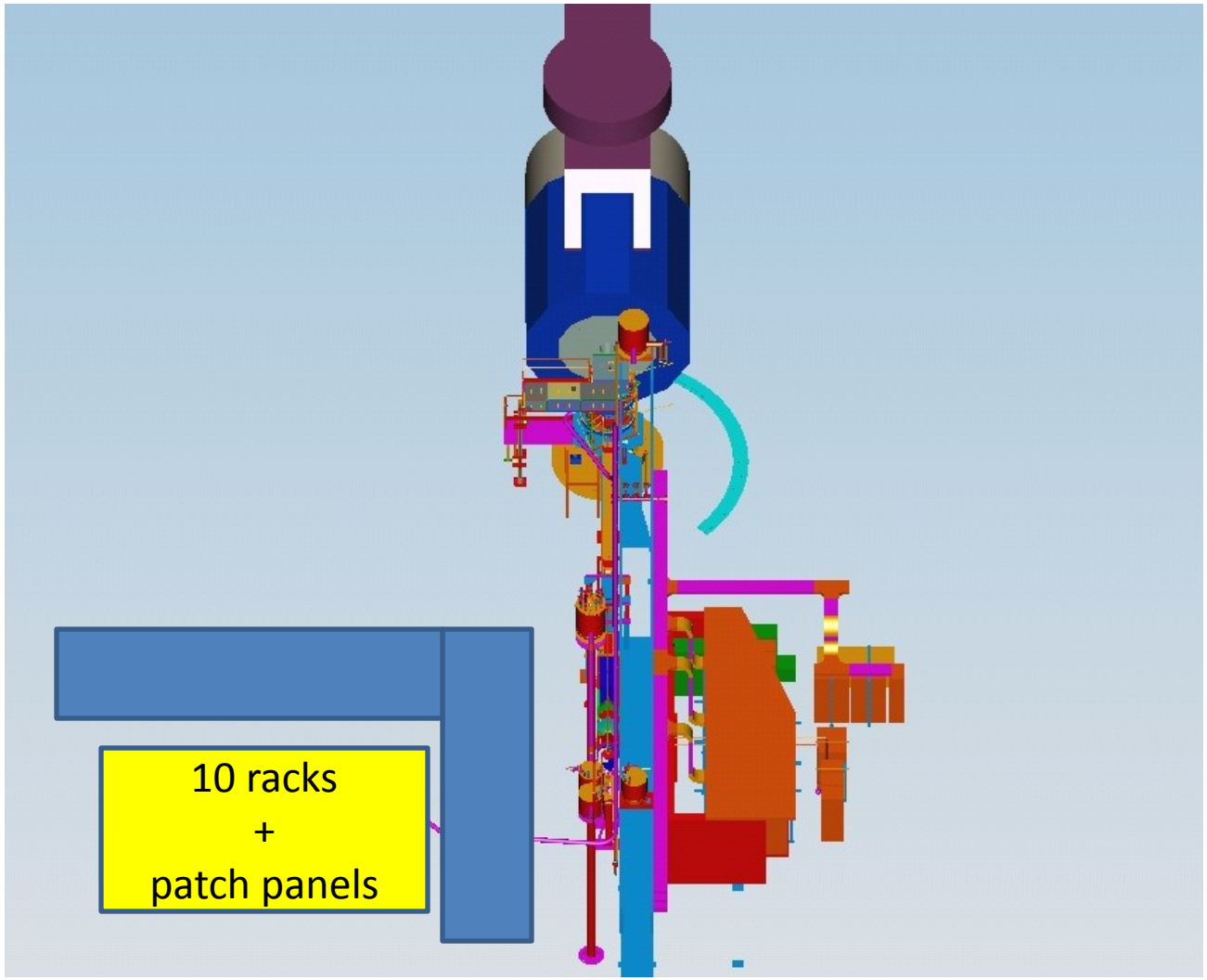
Level-1 Trigger Electronics



Pipelined detector readout electronics:
fADC

- Trigger Latency ~ 3 µs

Hall staging



Test run setup

- MRPC
  - V1290
  - JLAB or SIS FADC
- GEM / Hadron Blind Detector
  - APV25 (UVA)
    - SRS readout
    - MPD

DAQ electronics projects at UMass: spring and summer 2012
R.Miskimen

• UMass is responsible for the final assembly and testing of all *380 FADC modules* for Hall D. This activity will take place at UMass summer 2012, probably stretching into the fall.

• An undergraduate, Fabien Ahmed, spent the summer of 2011 at JLab working with the electronics group on FADC tests. A graduate student, Bill Barnes, and team of undergraduates will work on the electronics tests at UMass.

• Operations at UMass will include mechanical assembly of the VME boards, programming the FPGA's, verifying board operation, measuring and recording noise levels.

• Readout through a Wiener USB board in the VXS crate, connected to PC

DAQ electronics projects at UMass: connection to SOLID

• This activity helps Hall D, only helps SOLID by building expertise in the collaboration for working with and debugging DAQ electronics

• With support from Hall A, we would develop a CODA based DAQ test station at UMass: replicate the one VXS crate/sector readout for PVDIS/SOLID

Need CODA, and to borrow CTP, SSP, and CPU

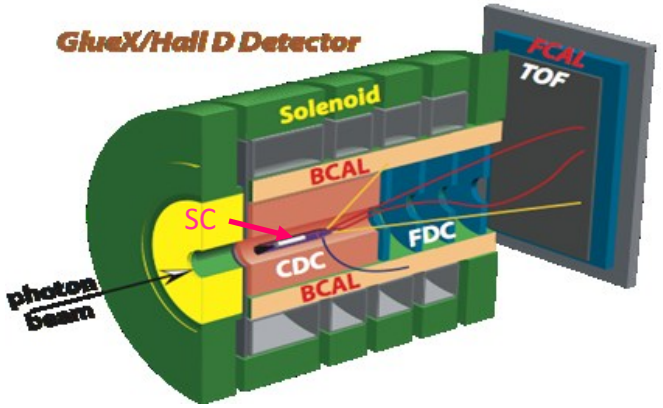
Test DAQ rates, triggers, software for FADC

SIDIS channel count

Detector	Module type	Number of channels	Number of modules
Forward Calorimeter	FADC+TDC	2x1150	119
Large angle calorimeter	FADC+TDC	2x450	58
Light Gas Cerenkov	FADC+TDC	120	8
Heavy Gas Cerenkov	FADC+TDC	270	17
Scintillator	FADC+TDC	120	8
GEM	VME	164K	321

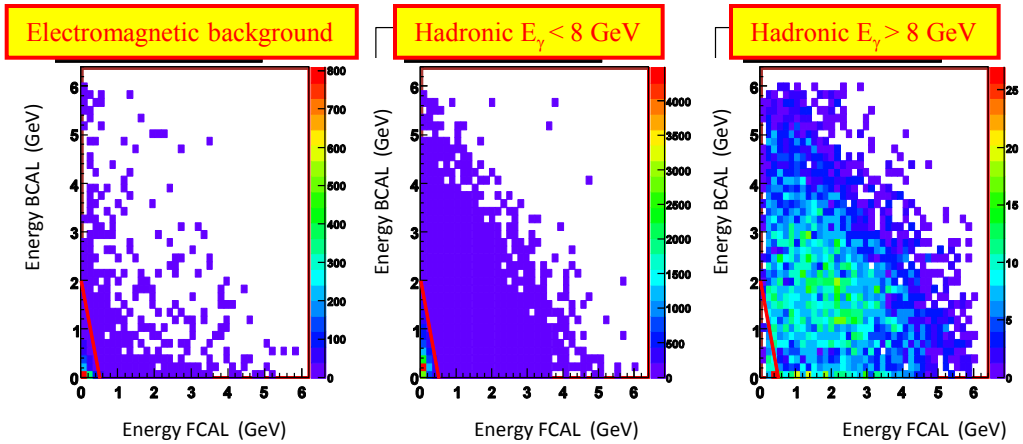
Hall D L1 Trigger-DAQ Rate

- Low luminosity (10^7 γ/s in $8.4 < E_\gamma < 9.0$ GeV)
  - 20 kHz L1
- High luminosity (10^8 γ/s in $8.4 < E_\gamma < 9.0$ GeV)
  - 200 kHz L1
  - Reduced to 20 kHz L3 by online farm
- Event size: 15 kB; Rate to disk: 3 GB/s



Detectors which can be used in the Level-1 trigger:

Forward Calorimeter (FCAL)	Energy
Barrel Calorimeter (BCAL)	Energy
Start Counter (SC)	Hits
Time of Flight (TOF)	Hits
Photon Tagger	Hits

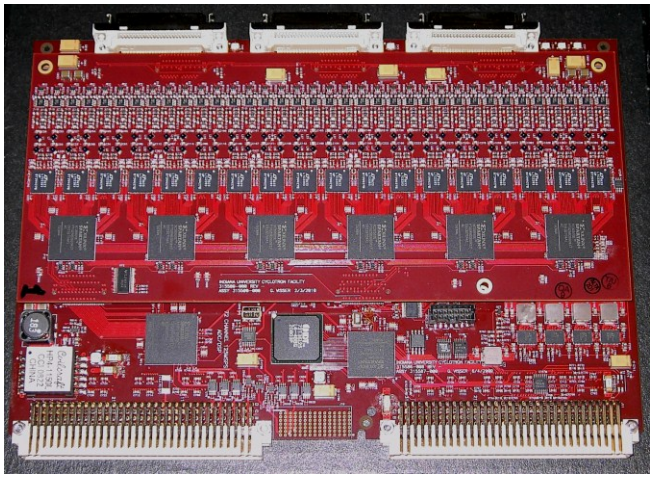


Basic Trigger Requirement:

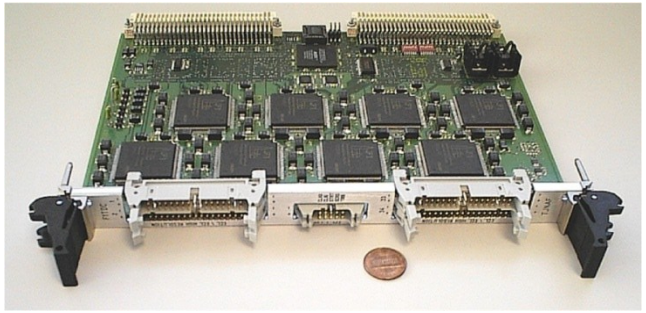
$$E_{BCAL} + 4 \cdot E_{FCAL} > 2 \text{ GeV}$$
and a hit in Start Counter

Custom Electronics for JLab

- VME Switched Serial (VXS) backplate
  - 10 Gbps to switch module (J_0)
  - 320 MB/s VME-2eSST (J_1/J_2)
- All payload modules are fully pipelined
  - **FADC125** (12 bit, 72 ch)
  - **FADC250** (12 bit, 16 ch)
  - **F1-TDC** (60 ps, 32 ch or 115 ps, 48 ch)
- Trigger Related Modules
  - **C**rate **T**rigger **P**rocessor (**CTP**)
  - **S**ub-**S**ystem **P**rocessor (**SSP**)
  - **G**lobal **T**rigger **P**rocessor (**GTP**)
  - **T**rigger **S**upervisor (**TS**)
  - **T**rigger **I**nterface/Distribution(**TI/D**)
  - **S**ignal **D**istribution (**SD**)

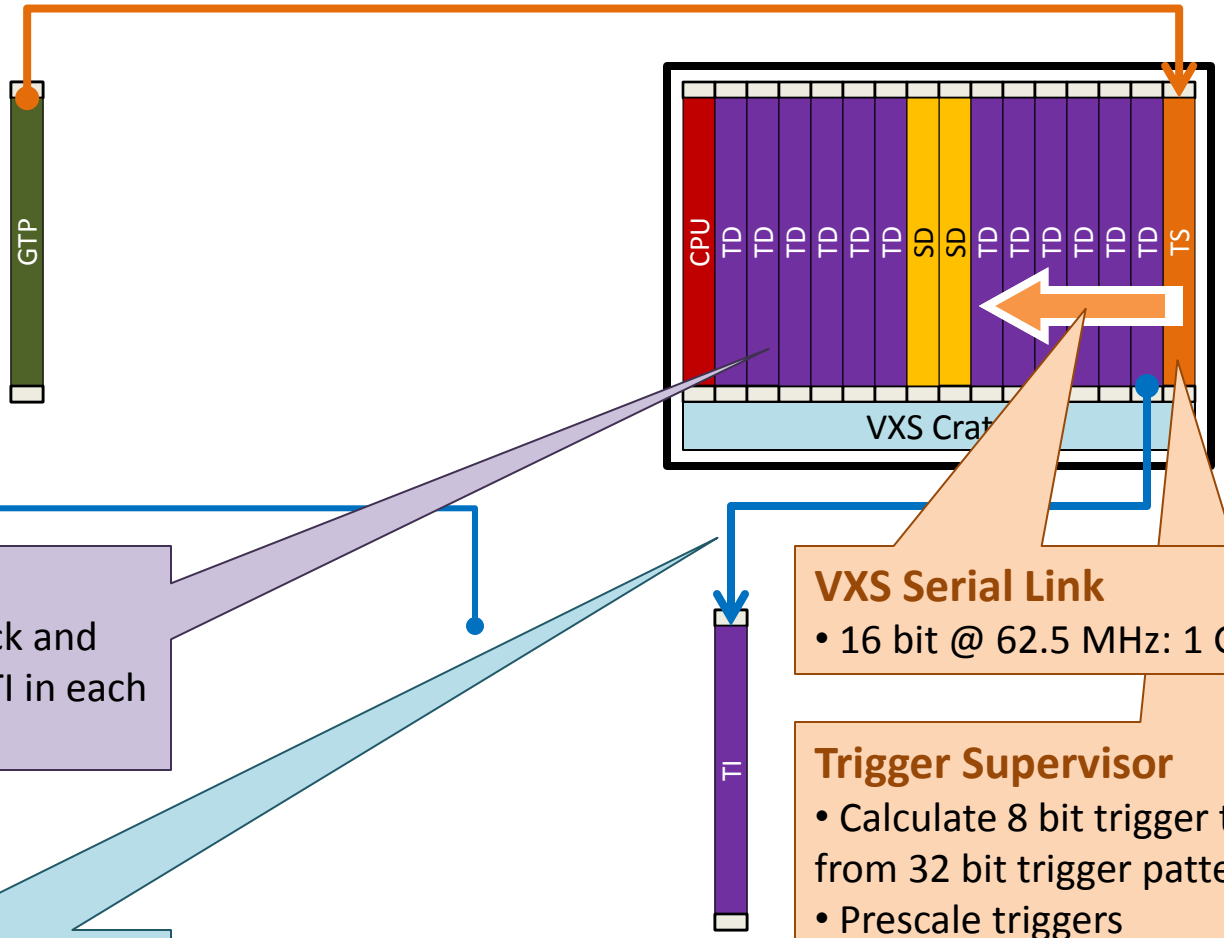


FADC125



F1-TDC

L1 Trigger Diagram



Trigger Distribution
- Distribute trigger, clock and synchronize signals to TI in each Crate

Fiber Optics
- 16 bit @ 62.5 MHz: 1 Gbps

VXS Serial Link
- 16 bit @ 62.5 MHz: 1 Gbps

Trigger Supervisor
- Calculate 8 bit trigger types from 32 bit trigger pattern
- Prescale triggers
- Transfer trigger and sync signal to TD (16 bit total)

L1 Trigger Diagram

TD

TID

VME Readout Controller
• Gigabit ethernet

Trigger Interface
• Receive trigger, clock and sync signals from TD
• Make crate trigger decision
• Pass signals to SD

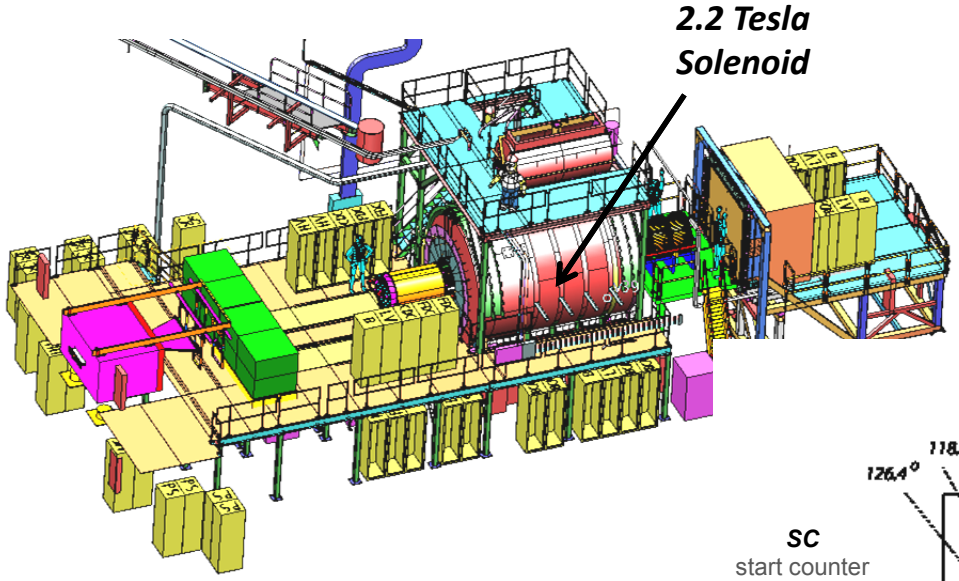
CPU FADC FADC FADC FADC FADC FADC CTP SD FADC FADC FADC FADC FADC FADC TI

VXS Crate

Signal Distribution
• Distribute common signals to all modules: busy, sync and trigger 1/2

VXS Serial Link
• 4 bit @ 250 MHz: 1 Gbps

The GlueX Detector

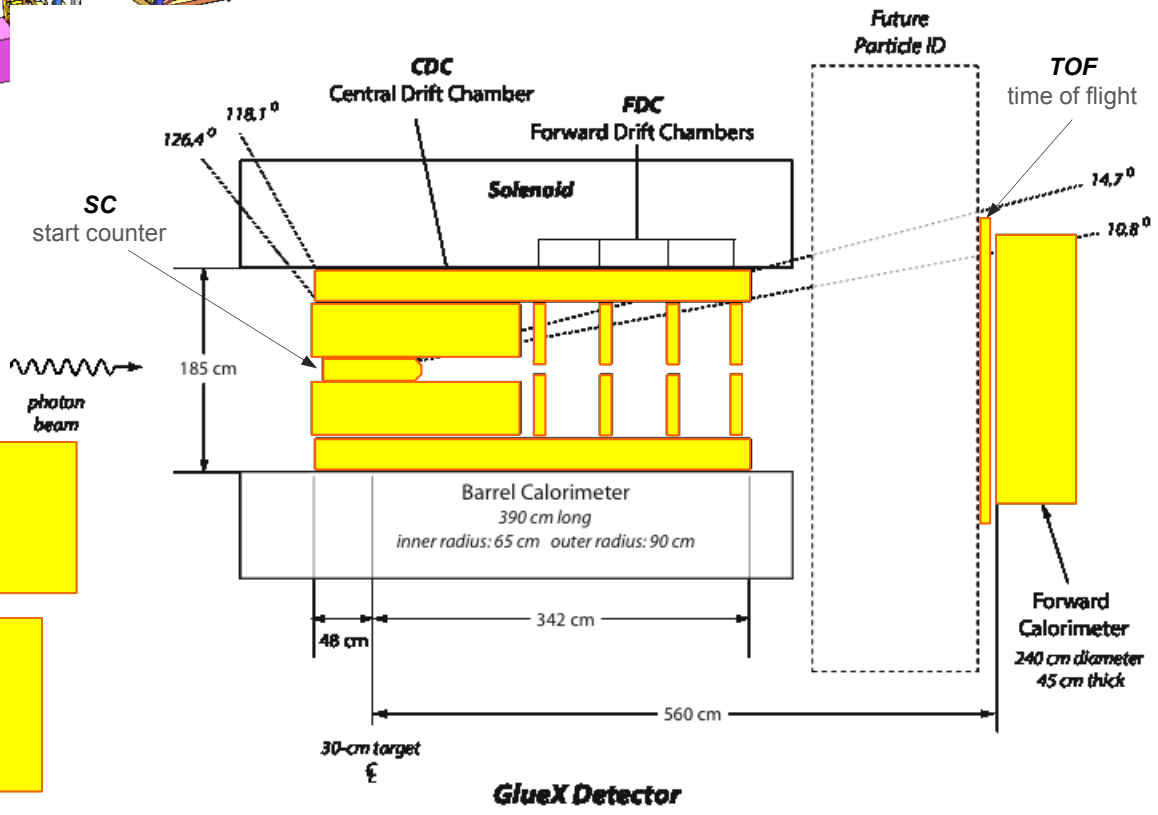


- 2.2T superconducting solenoidal magnet
- Fixed target (LH_2)
- 10^8 tagged γ/s (8.4-9.0GeV)
- hermetic

Charged particle tracking
- Central drift chamber (straw tube)
- Forward drift chamber (cathode strip)

Calorimetry
- Barrel Calorimeter (lead, fiber sandwich)
- Forward Calorimeter (lead-glass blocks)

PID
- Time of Flight wall (scintillators)
- Start counter
- Barrel Calorimeter



GlueX Data Rate

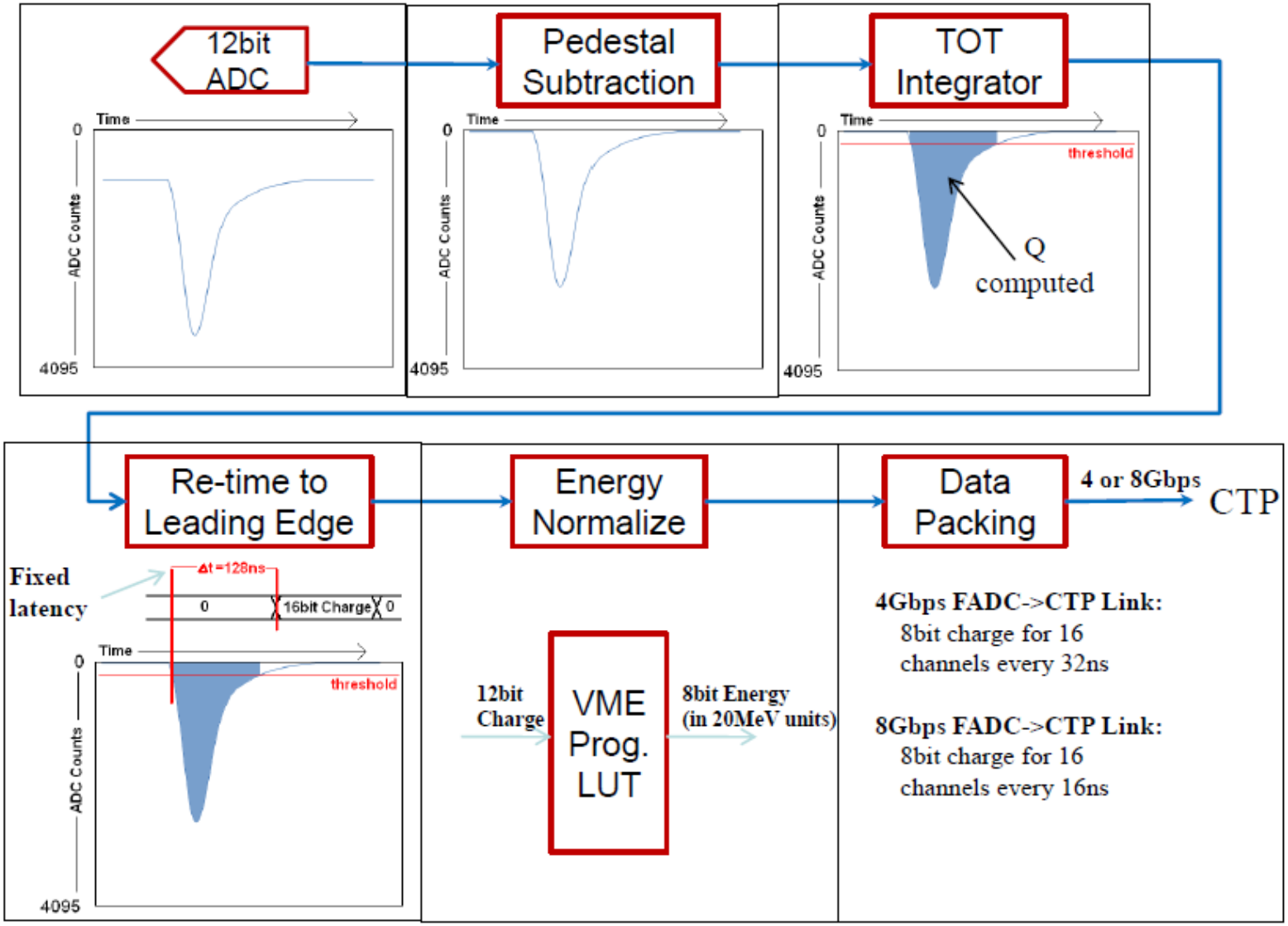
		Front End DAQ Rate	Event Size	L1 Trigger Rate	Bandwidth to mass Storage	
JLab	GlueX	3 GB/s	15 kB	200 kHz	300 MB/s	priva comm.
	CLAS12	0.1 GB/s	20 kB	10 kHz	100 MB/s	
LHC	ALICE	500 GB/s	2,500 kB	200 kHz	200 MB/s	CHEP2007 talk Sylvain Chapelin
	ATLAS	113 GB/s	1,500 kB	75 kHz	300 MB/s	
	CMS	200 GB/s	1,000 kB	100 kHz	100 MB/s	
	LHCb	40 GB/s	40 kB	1000 kHz	100 MB/s	
BNL	STAR	50 GB/s	1,000 kB	0.6 kHz	450 MB/s	*
	PHENIX	0.9 GB/s	~60 kB	~ 15 kHz	450 MB/s	**

*** Jeff Landgraf Private Comm. 2/11/2010**
**** CHEP2006 talk MartinL. Purschke**

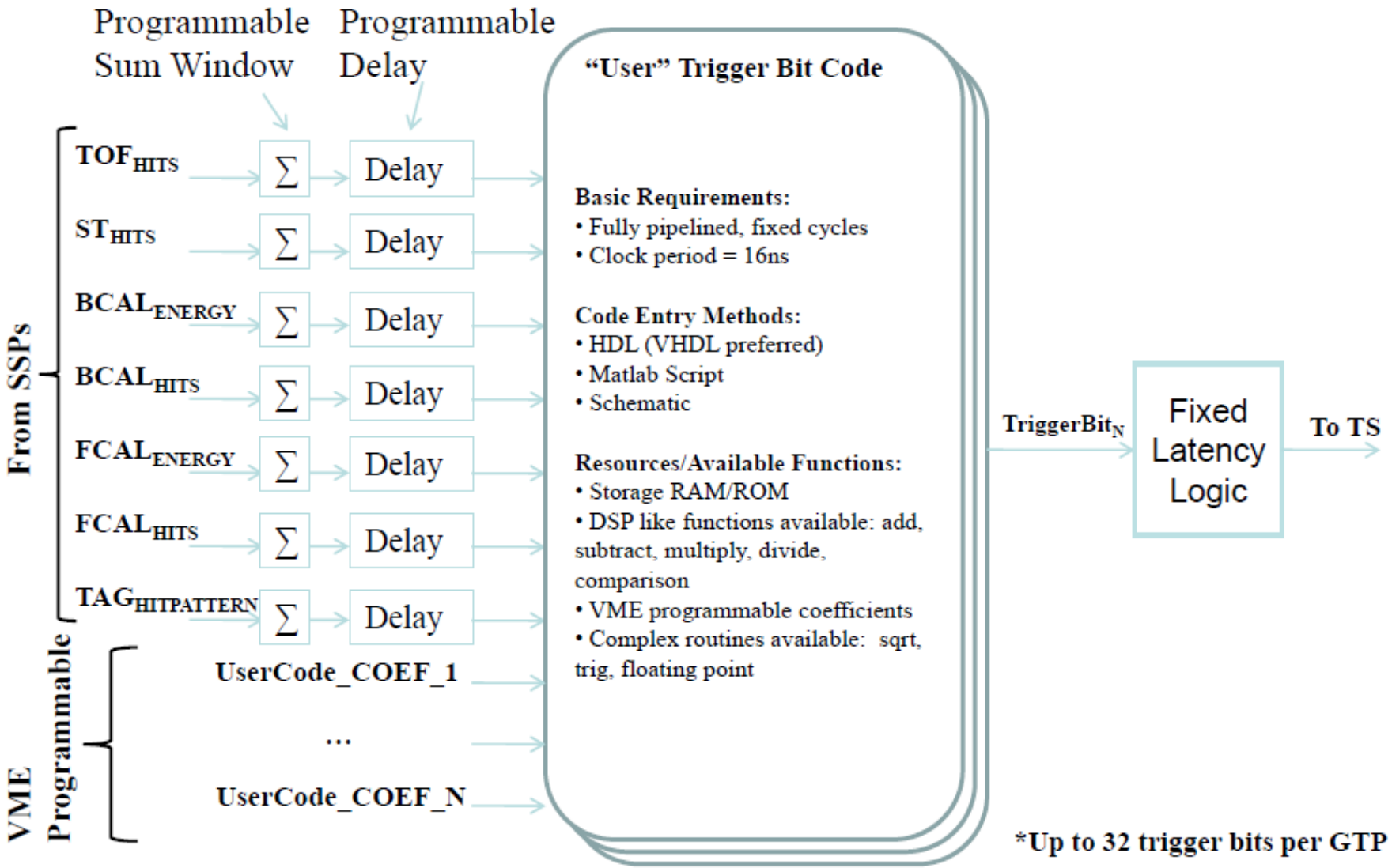
CODA3 – What's different

CODA 2.5	CODA 3
Run Control (X, Motif, C++) (rcServer, runcontrol)	Experiment Control – AFECS (pure JAVA) (rcPlatform, rcgui)
Communication/Database (msql, cdev, dptcl, CMLOG)	cMsg – CODA Publish/Subscribe messaging
Event I/O C-based simple API (open/close read/write)	EVIO – JAVA/C++/C APIs Tools for creating data objects, serializing, etc…
Event Builder / ET System / Event Recorder (single build stream)	EMU (Event Management Unit) Parallel/Staged event building
Front-End – vxWorks ROC (Interrupt driven – event by event readout)	Linux ROC, Multithreaded (polling – event blocking)
Triggering: 32 ROC limit, (12 trigger bits -> 16 types) TS required for buffered mode	128 ROC limit, (32 trigger bits -> 256 types) TI supports TS functionality. Timestamping (4ns)

FADC Encoding Example



GTP Trigger Bit Example



L3 data reduction

- Pile up detection
  - Only record sample for event with pile up
- Calorimeter clustering

- GEM readout
  - Timing cut
  - Clustering
  - Crude tracking