SoLID DAQ update

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SoLID collaboration meeting

Recommendations 2c

1. The plans for the High Level Trigger and the needs for slow control need to be worked out in detail and the implications for resources need to be evaluated.
2. The implications of the need for these resources in the context of availability of resources at the laboratory need to be understood.
3. Closer communication with the other JLab experiments and the JLab computing center is strongly encouraged.
4. Having a functional simulation and reconstruction routines as soon as possible should be a high priority in the software effort. Such software will pay off many times over in experimental design and avoiding pitfalls.

DAQ observations

Observations

- SoLID plans to use much of the current 12-GeV electronics from Jefferson Lab.
- Plans for using the APV25 chip for GEM readout were presented.
- The Level 3 trigger was not described and no costs were included.
- The slow control needs of the experiment were not presented and no costs were included.
- The SoLID collaboration currently has some simulation and limited reconstruction.
- The manpower currently associated with software for SoLID is estimated to be 6 FTE-years. Numbers from both Hall-B/CLAS-12 and Hall-D/GlueX are in the range of 30 to 50 FTE-years.
- The data scale expected from SoLID is similar to that anticipated in Halls B and D, while that in the early Hall-A experiments have a much smaller data footprint.
- No plan for data handling was presented.
- Data storage needs for Monte Carlo simulations were not included.

Findings

- Consultation with appropriate people from the other halls would be useful to get a more accurate estimate of software needs, including manpower.
- Early exploration of the tools available at Jefferson Lab that can handle the data at the expected scale of SoLID will be crucial in minimizing the false starts in software development

Dead time correction PVDIS 1b.2 (no major progress since last meeting)

- Test with small scale setup
- Simulation
- Discuss with DAQ group for particular features needed
  - Example : helicity gated deadtimes
- Rework CDR to add parity specific electronics

- Need to write a separate document about DAQ requirements for DAQ group, Electronics group and potential collaborators on electronics (Saclay)

L3 trigger 2c1

- Test on small scale L1 trigger
- L3 farm : collaborate with Hall D, try to test simulated data on their setup
- Need simulated digitized data and tracking algorithm to test online
- Need to figure out funding

- Progress : DAQ group advised to first test on simulated data the L3 farm algorithm
  - Need digitized background simulation data
  - Need algorithm to do analysis

Ressources 2c2

- Computing ressources needed for L3
- Tape SILO needs, network
- Manpower

L3 trigger 2c2

- Test on small scale L1 trigger
- L3 farm : collaborate with Hall D, try to test simulated data on their setup
- Need to figure out funding

Forgotten recommendation

- Bunker design
  - Radiation
  - Cooling of bunker to be evaluated / design

Hardware

- FADC availables
- VXS crates and Intel CPU
- GTP borrowed
- VETROC available
- R&D need
  - Individual FADC reading
  - Trigger setup
  - Deadtime measurement for PVDIS
  - (High resolution TDC)

FADC new VTP design

- New CTP for Hall B
- Allow readout FADC in parallel : 16 times faster
- FADC readout is not a bottle neck : max rate with 8 Gbps link assuming 20 samples
- Can read all channels 64 channels per sector and reduce on VTP : clustering
- 2 additionnal optical links for trigger for triggering neighboring sector
- First prototype in about 1 month

Cerenkov PMT readout

- MAROC3 close to what we need
  - 64 channels
  - Variable gain
  - Discriminated fast logic signal
  - Missing : analog sum of 8, need sum of 64

  8 sum of 8 available just need to sum them, will check with INFN for modified RICH board, requested 10 K$ preRD money
  - Radiation hardness is pretty good, need to be tested, possibility of new version to handle Single Event Upset
  - MAROC default option

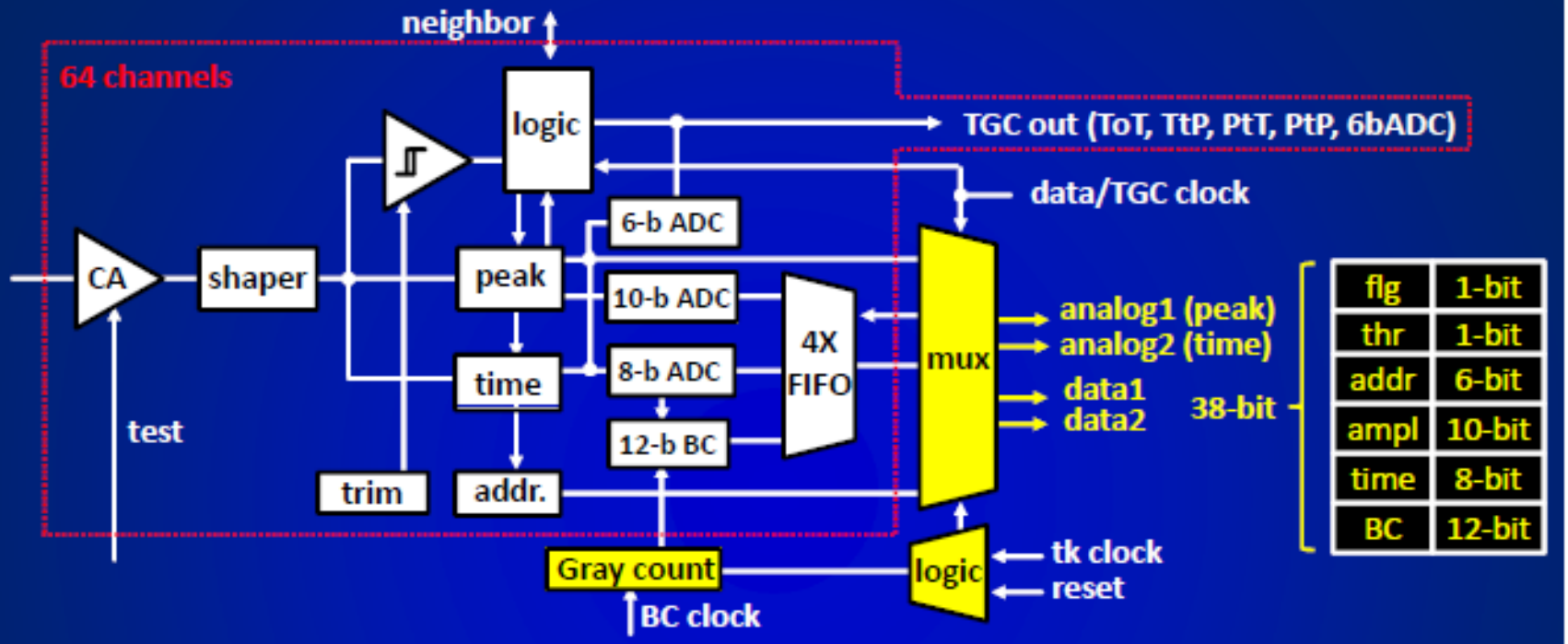
  - Will check design with electronics group for FADC analog output
- Possible readout schemes
  - FADC only (default)
  - FADC + VETROC
  - VETROC only : needs to be evaluated

  - Preferred : Add TDC readout for each Cerenkov channel 232 VETROC additionnal 700 K$, could improve Cerenkov trigger

MRPC

- Expected timing resolution 80 to 50 ps
- Default readout
  - NINO + VETROC : 20 ps timing resolution
- R&D MRPC : 20 ps
  - Sampling TDC ASICs : PSEC4/5, SAMPIC, DRS4 give 5 to 1 ps resolution
  - TDC ASIC SBIR : 2ps LSB
- Need to determine effect of background
- More details in TOF talk, would go for sampling electronics though add deadtime and event size

VMM2 Architecture - Multiplexing and Readout



- sparse readout of amplitude/timing with token passing
- readout options:
  - mixed-signal 2-phase: peak and time at analog outputs analog1,2 (peak,time)
    address serialized at digital output data1
  - fully digital continuous: 38-bit event data at digital outputs data1,2
    data1 also serves as empty flag
    data shift at each ck cycle or at each ck edge
    designed for up to 200 MHz data clock

GEM readout

- VMM3
  - Peaking time 25 to 200 ns
  - 6 bit ADC 25 ns
  - 10 bit ADC and time 200 ns : 38 bit
  - 200 MHz readout
  - Digital readout
- Promising option though no multiple samples, or low resolution ADC might be an issue with background
- Test board available after ATLAS testing (1 to 2 years)
- Requested 10 K$ preRD for evaluation board

DREAM CLAS12

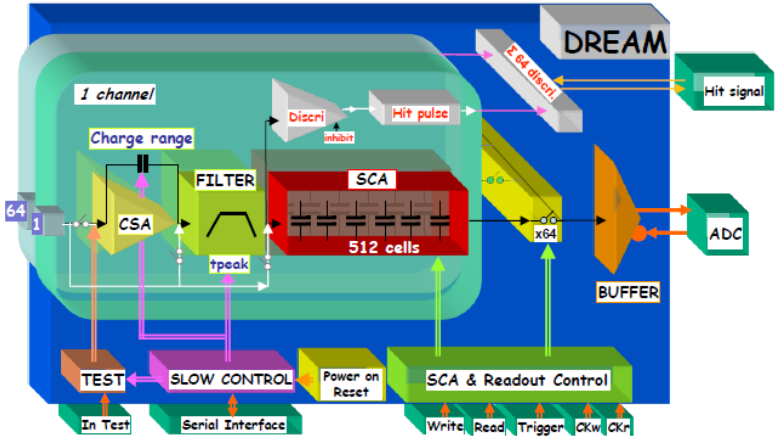


Fig. 1: Block diagram of the DREAM chip.

Parameter	Value
Polarity of detector signal	Negative or Positive
Number of channels	64
External Preamplifier option	Yes; access to the filter or SCA inputs
Charge measurement	
Input dynamic range/gain	50 fC; 100 fC; 200 fC; 1 pC, selectable per channel
Output dynamic range	2V p-p
I.N.L	< 2%
Charge Resolution	> 8 bits
Sampling	
Peaking time value	50 ns to 1 µs (16 values)
Number of SCA Time bins	512
Sampling Frequency (*WCk*)	1 MHz to 50 MHz
Triggering	
Discriminator solution	Leading edge
HIT signal	OR of the 64 discriminator outputs in LVDS level
Threshold Range	5% of the dynamic range
I.N.L	< 5%
Threshold value	(7-bit + polarity bit) DAC common to all channels
Minimum threshold value	≥ noise
Readout	
Readout frequency	Up to 20 MHz
Channel Readout mode	all channels excepted those disabled (statically)
SCA cell Readout mode	Triggered columns only
Test	
Calibration (current input mode)	1 channel among 64; external test capacitor
Test (voltage input mode)	1 channel among 64; internal test capacitor (1/charge range)
Functional (voltage input mode)	1, few or 64 channels; internal test capacitor/channel
Trigger rate	Up to 20kHz (4 samples read/trigger).
Counting rate	< 50 kHz / channel
Power consumption	< 10 mW / channel

Table 1: Summary of the DREAM requirements.

- Pro
  - Close to APV25
  - Longueur pipeline 12.8 us
  - Or64 channel trigger
- Cons
  - Designed for low trigger rate
  - No zero suppression

Proposal for 1 MHz chip development : US funding might help

Tape costs

		Days	Data rate	Seconds	Total data TB	Double	DLO5 in $	DLO6 in $
E12-11-108	Pol proton	120	250	10368000	2592	5184	259200	155520
E12-12-006	J/Psi	60	250	5184000	1296	2592	129600	77760
E12-10-006	Transv. Pol. 3He	90	250	7776000	1944	3888	194400	116640
E12-11-007	Long. Pol. 3 He	35	250	3024000	756	1512	75600	45360
E12-10-007	PVDIS	169	250	14601600	3650.4	7300.8	365040	219024
	Total	474		40953600	10238.4	20476.8	1023840	614304
Actual days	Actual years		Time in s			Per year	394200	236520
948	2.60	474	40953600					

650 K$ total tape cost, if double 1.3 M$ total tape cost
(might be cheaper with improved technology)
500 MB/s should be ok for hard drives, need estimate network upgrade (less than 100 K$ since fiber are already being pulled , to be confirmed)

Total PreRD

Cost estimation			
FADC 250	4500	4	18000
Cables			0
V1290	11000	0	0
VME64X	11000	0	0
VETROC	4500	2	9000
TD	3000	1	3000
CTP	7000	1	7000
SSP	5000	1	5000
GTP	5000	1	5000
TS	3500	1	3500
TID	3000	3	9000
SD	2500	3	7500
FADC trigger Dist	4000	3	12000
VXS crate	15000	3	45000
VME CPU	4500	4	18000
Optical fiber	100	20	2000
SRS computers	3000	1	3000
MPD	4500	1	4500
L3 farm node	5000	1	5000
Network router	10000	1	10000
	Total	49	151500

Pre RD hardware : detector test stand

FADC 250	4500	4	18000
VETROC	4500	2	9000
TD	3000	1	3000
CTP	7000	1	7000
SSP	5000	1	5000
TID	3000	1	3000
SD	2500	1	2500
FADC trigger Dist	4000	1	4000
VXS crate	15000	1	15000
VME CPU	4500	1	4500
Optical fiber	100	20	2000
Computer	3000	1	3000
MPD	4500	1	4500
Network router	10000	1	10000
Total			72500

Added additionnal 10 K$ for MAROC and 15 K$ for VMM3 : total 97 K$

Manpower

- JLAB :
  - Alexandre Camsonne
  - Robert Michaels (Compton development)
  - Steve Wood
  - Electronics group
  - DAQ group
- Stony Brook
  - Seamus Riordan
  - Krishna Kumar
  - Postdoc
  - Student
- UVA : Danning Di GEM readout (SBS / Tritium)
- Need to make detailed manpower and task schedule for R&D and experiment

Simulations needs

- GEM occupancies and digitization SIDIS for event size, occupancy (Ole, Zhiwen, Duke)
- Updated trigger rates PVDIS, SIDIS(Zhiwen, Rakitah)
- FADC digitization PVDIS : realistic PID (Zhiwen, Yuxiao?)
- Cerenkov simulation only timing readout no FADC(Zhiwen?)
- Effect 1 sample vs 3 samples GEM and 20 samples vs time integral SIDIS
- Full FADC trigger simulation SIDIS

Timeline before next collaboration meeting (September 2015)

- Summer SBS projects
  - GTP : calorimeter
  - VETROC : used by Compton
  - FADC : FADC counting DAQ deployment and HCAL trigger
  - L3 farm test will Hall D and DAQ group
  - GEM : MPD test
- Development :
  - Deadtime mesurement
  - FADC readout and trigger serialization (could be used by other experiments NPS, SBS)

Pre R&D manpower

- Test trigger rate capability (3 months + 1 JLAB)
- Test full triggering schemes (implementation 3month / test 6 month + 1 person JLAB)
- GEM APV rate capability (3 months +1 person (UVA+Stony Brook)
- MRPC : high resolution timing (6 month + 1 JLAB)
- L3 : performance tests and data reduction (1 year / 1 student or postdoc and JLAB staff)
  - Implementation of L3 farm
  - Need simulated data (software) (Ole, Zhiwen, Duke)
  - Reconstruction algorithm to test (software)

- Can be covered by operation funds DAQ and electronics
- Could use addition student for training

SBS update

- Trigger test HCAL : 16 FADC + GTP
  - Trigger test completion in about 2 months

- GEM MPD :
  - 5 MPDs
  - First iteration of CODA library
  - Implementation optical link readout (2 months)
- SRS : PRAD this year

Timeline before next collaboration meeting

- SBS projects
  - GTP calorimeter trigger test
  - GEM : preliminary performance
- DAQ document

Document update

- Add parity specific requirements ?
  - Deadtime
  - Helicity
  - BPM/charge measurement
  - Pion trigger
- Address comment :
  - L3 farm performance and cost
- New Hardware
- New GEM chip
- Tape price
- Network upgrade

- Give total price with dependencies and project price

Steve started editing

Conclusion

- Progress from SBS on calorimeter trigger and GEM
- Need digitized data for
  - SIDIS GEM occupancies
  - L3 Farm evaluation
  - Trigger rates and efficiencies
- MAROC default option for Cerenkov readout
- Request for PreRD fund
- Start work on document update