SoLID DAQ update

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August 27th 2016

SoLID collaboration meeting

Overview

- Recommendations for Director's review
- Hardware available
- Document
- Updated trigger rates
- New FADC readout
- PVDIS deadtime
- SIDIS event size and data rates
- Cerenkov readout
- TOF readout options
- Simulations needs
- L3 farm

Dead time correction PVDIS 1b.2

- Test with small scale setup (ongoing)
- Simulation
- Discuss with DAQ group for particular features needed
  - Example : helicity gated deadtimes
- Rework CDR to add parity specific electronics

- Need to write a separate document about DAQ requirements for DAQ group, Electronics group and potential collaborators on electronics (Saclay)

DAQ observations

Observations

- SoLID plans to use much of the current 12-GeV electronics from Jefferson Lab.
- Plans for using the APV25 chip for GEM readout were presented.
- The Level 3 trigger was not described and no costs were included.
- The slow control needs of the experiment were not presented and no costs were included.
- The SoLID collaboration currently has some simulation and limited reconstruction.
- The manpower currently associated with software for SoLID is estimated to be 6 FTE-years. Numbers from both Hall-B/CLAS-12 and Hall-D/GlueX are in the range of 30 to 50 FTE-years.
- The data scale expected from SoLID is similar to that anticipated in Halls B and D, while that in the early Hall-A experiments have a much smaller data footprint.
- No plan for data handling was presented.
- Data storage needs for Monte Carlo simulations were not included.

Findings

- Consultation with appropriate people from the other halls would be useful to get a more accurate estimate of software needs, including manpower.
- Early exploration of the tools available at Jefferson Lab that can handle the data at the expected scale of SoLID will be crucial in minimizing the false starts in software development

Recommendations 2c

1. a)The plans for the High Level Trigger and b) the needs for slow control (Brad) need to be worked out in detail and the implications for resources need to be evaluated.
2. The implications of the need for these resources in the context of availability of resources at the laboratory need to be understood.
3. Closer communication with the other JLab experiments and the JLab computing center is strongly encouraged.
4. Having a functional simulation and reconstruction routines as soon as possible should be a high priority in the software effort. Such software will pay off many times over in experimental design and avoiding pitfalls. (Ole)

Hardware

- FADC availables (4 + 18 = 22 all used)
- VXS (3) crates and Intel CPU (3)
- GTP borrowed , VTP received
- VETROC available (2 + 5 ordered)
- R&D needed
  - Trigger setup (preRD request)
  - Deadtime measurement for PVDIS (on going)
  - (High resolution TDC)
  - VXS FADC readout (ongoing DAQ funded)

DAQ document summary

- Add parity specific requirements ?
  - Deadtime
  - Helicity
  - BPM/charge measurement
  - Pion trigger
- Address comment :
  - L3 farm performance and cost
- Integrate new FADC fast readout
- TOF electronics options
- New GEM chip option
- Tape price
- Network upgrade

- Give total price with dependencies and project price

- Steve Wood summarizing preCDR and develop in contact with electronics and DAQ group

PVDIS electron trigger

- Coincidence ECAL and Gas Cerenkov

	Old	Hall D
Singles ECAL	290 KHz	230 KHz
Singles rates Cerenkov	1.9 MHz	803 KHz
Accidental 30 ns	16.5 KHz	4.1 KHz
DIS electron	10 KHz max	7.7 KHz
Total rate	**27 KHz**	**12.1 KHz**

Calorimeter FADC readout

- New readout scheme through VTP
  - VME backplane 100 MB/s
  - VXS 16x500 MB/s

- Can transfer a full ADC (16 channels * 20 samples =1.3 KB) up to 390 KHz, transfer is not a bottle neck any more
- GEM or SILO readout are limiting factor now

Deadtime measurement (1b.2)

- Can deadtime affect PVDIS asymmetry ?

- Test stand Compton FADC
- Helicity gated scalers
- TI firmware modification
- Generate asymmetry same order of PVDIS
- Add random background
- Check asymmetry value
- Target date August

Dead time correction PVDIS 1b.2

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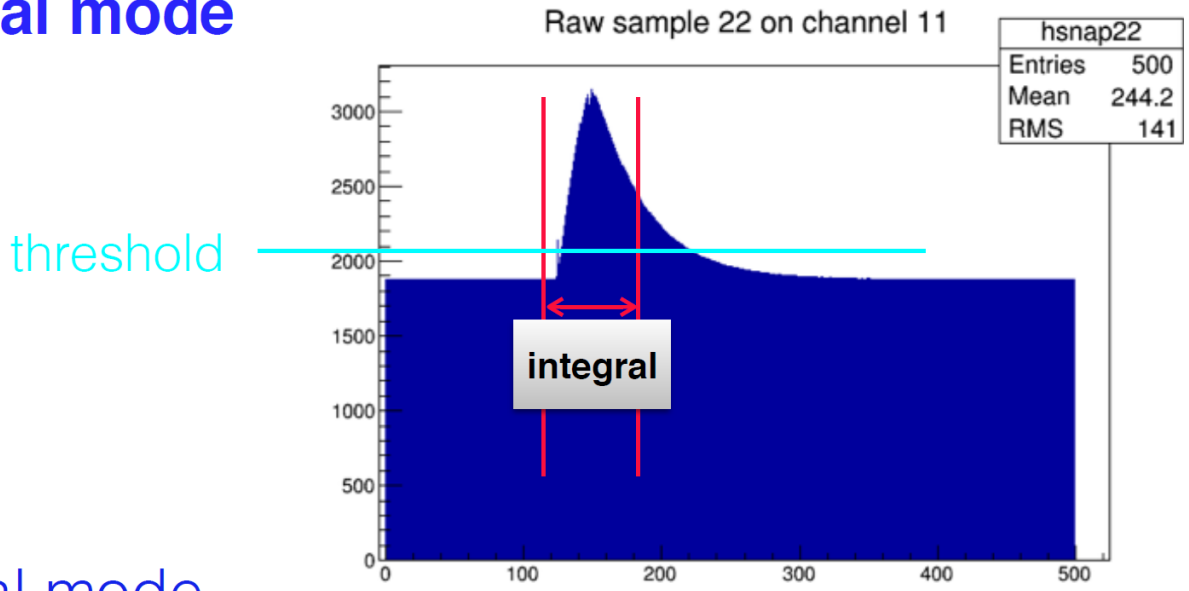
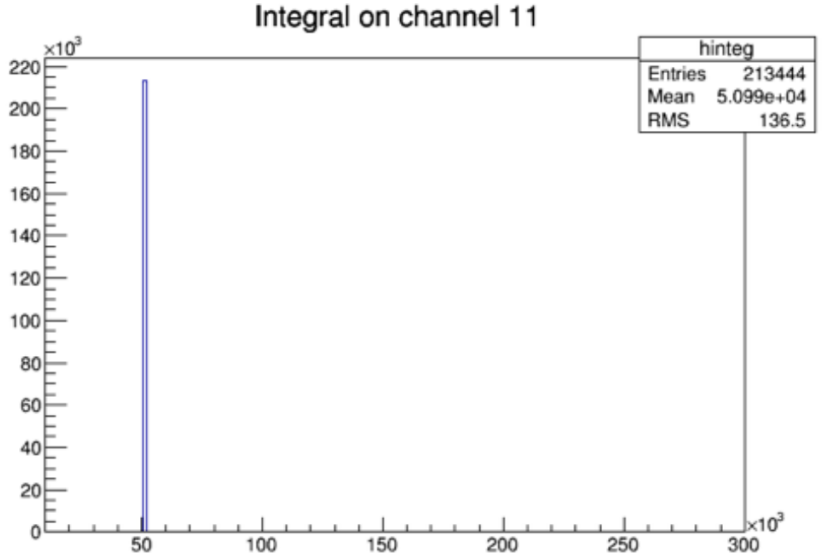
Dead time correction PVDIS 1b.2

FADC integral mode

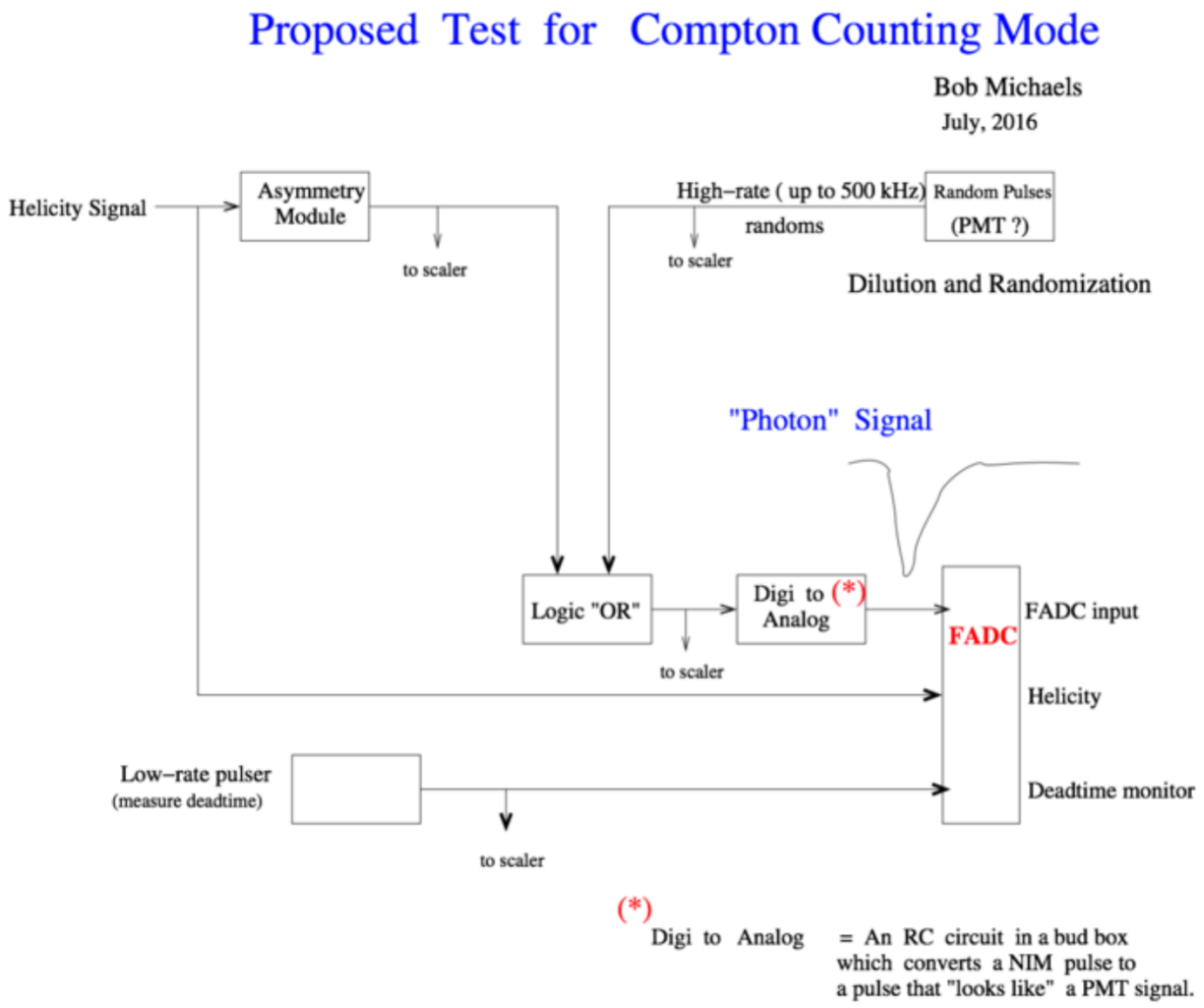


Pulse integral mode

- integral number
- time begin to integrate



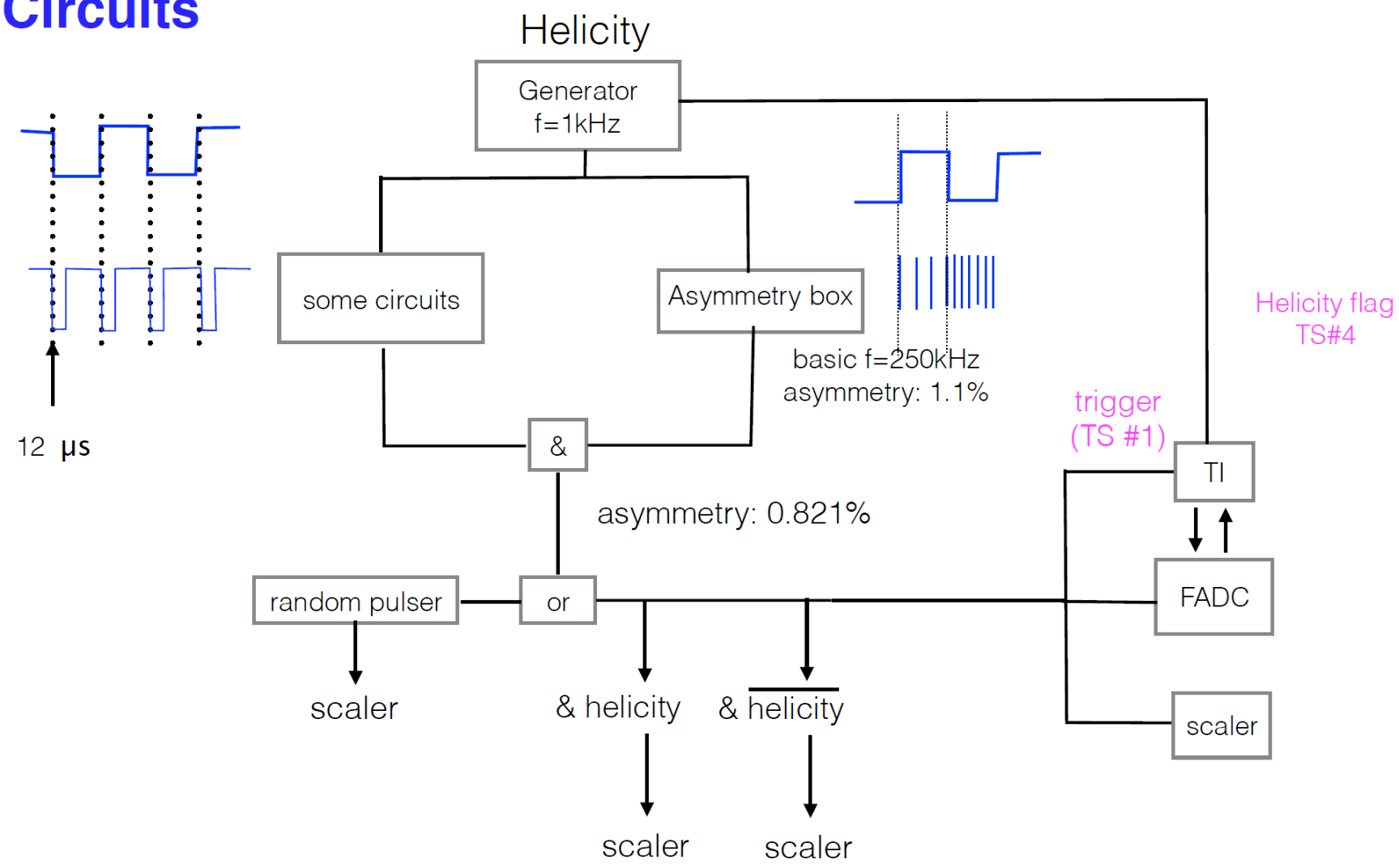
Dead time correction PVDIS 1b.2



Purpose:

1) measure an asymmetry by FADC
2) find a method to correct the asymmetry

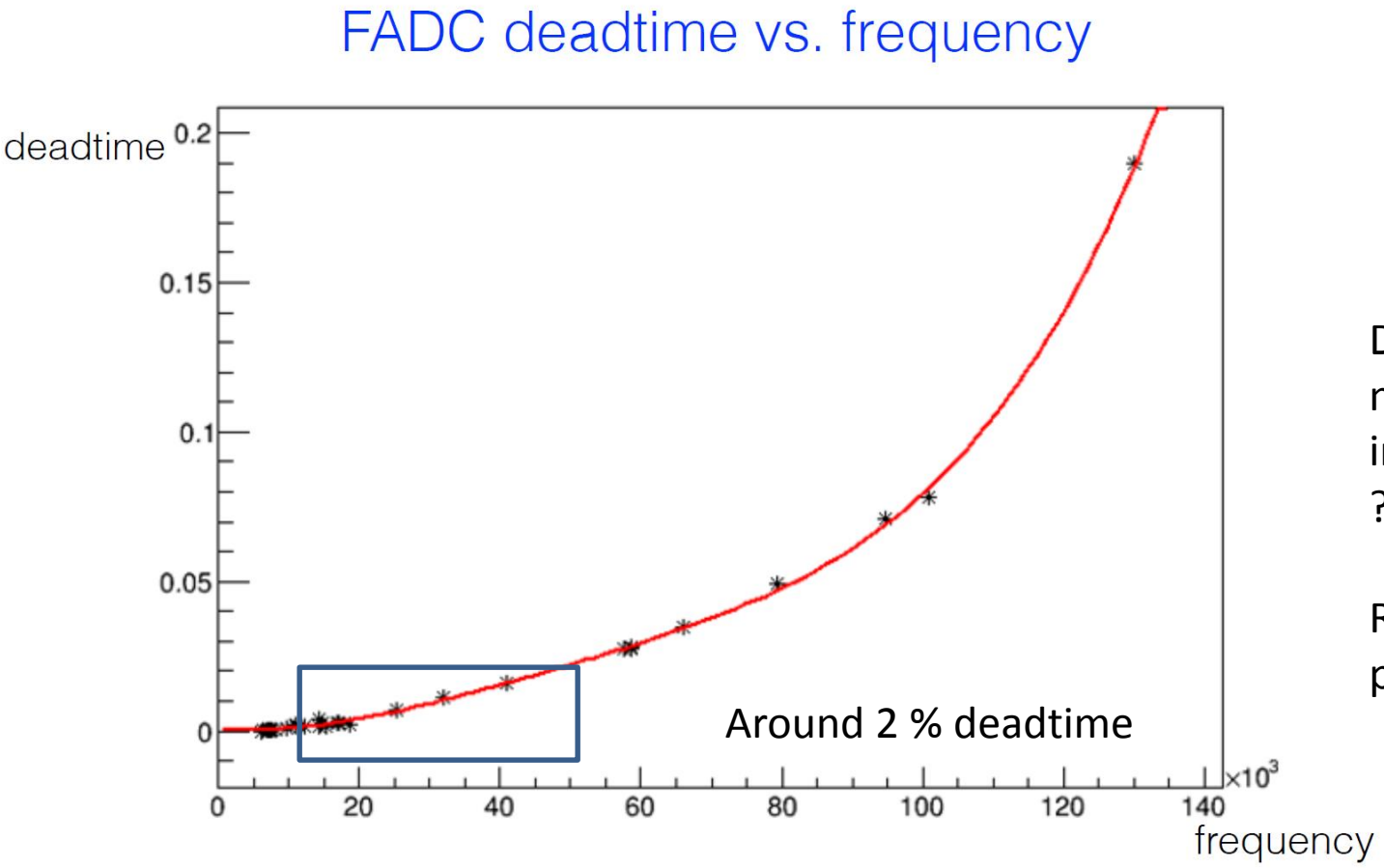
Circuits



- change the frequency of random pulser
- calculate asymmetry from scaler and FADC respectively

FADC deadtime measurement

FADC deadtime = total counts from FADC/counts from scaler



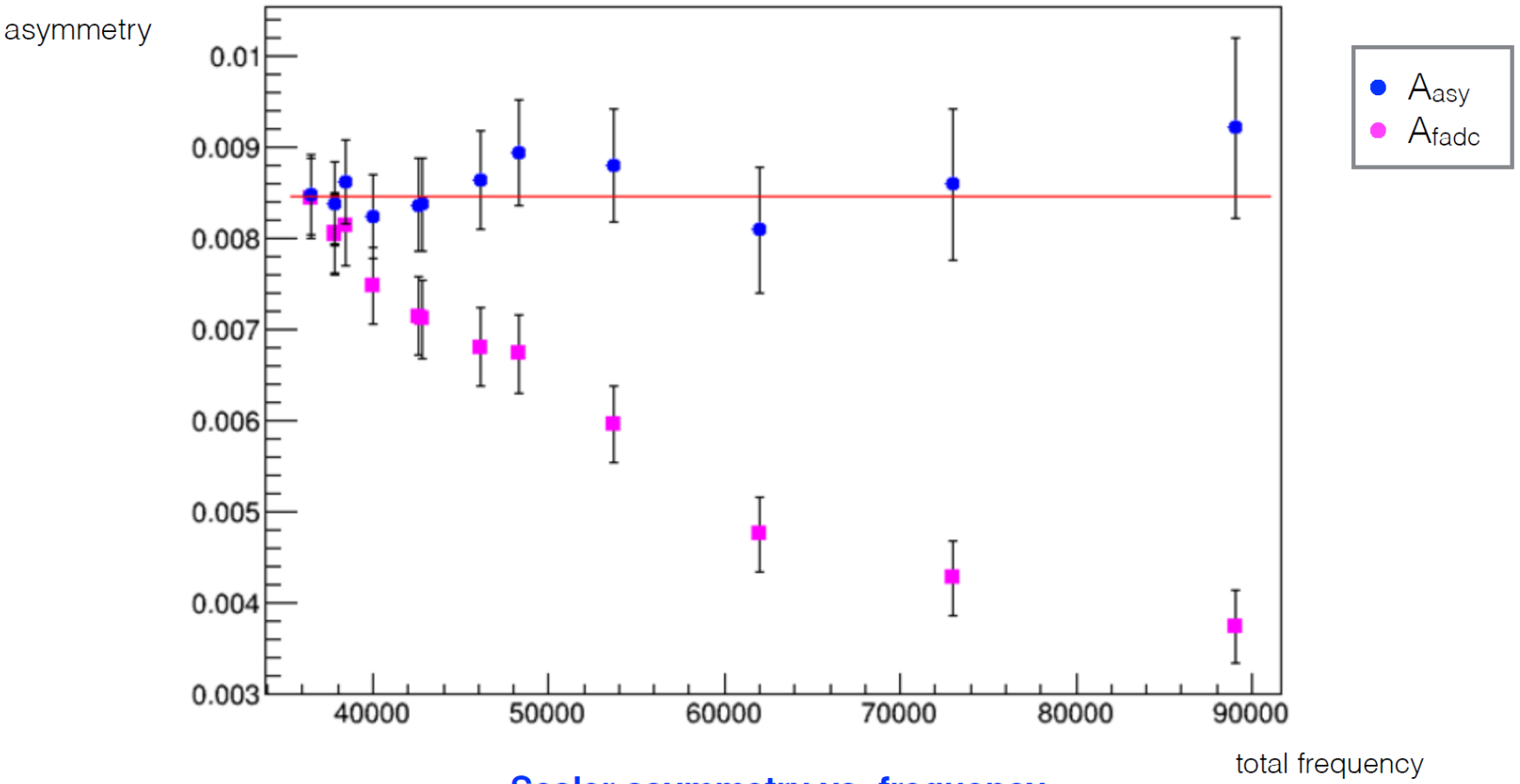
Do we need to improve it ?

R&D possible

```
Minimizer is Linear
Chi2                      =  3.50342e-05
NDf                       =          30
p0                        =  0.000914936   +/-   0.000900636
p1                        = -2.22178e-07   +/-   1.11363e-07
p2                        =  2.51556e-11   +/-   3.58349e-12
p3                        = -3.37321e-16   +/-   4.23316e-17
p4                        =  1.86471e-21   +/-   1.62946e-22
```

Measured asymmetry

$$A_{FADC} = A_{asy} \times (1 - \frac{N_{rdm}^{total}}{N_{total}})$$



Scaler asymmetry vs. frequency

Deadtime measurement (1b.2)

- FADC setup to study deadtime
- Need to understand the system and model
- Not done by August
- Continue study with Compton during run

Cerenkov PMT readout

- MAROC3 close to what we need
  - 64 channels
  - Variable gain
  - Discriminated fast logic signal
  - Missing : analog sum of 8, need sum of 64

  8 sum of 8 available just need to sum them, will check with INFN for modified RICH board, requested 10 K$ preRD money
  - Radiation hardness is pretty good, need to be tested, possibility of new version to handle Single Event Upset
  - MAROC default option
  - MAROC testboard available

  - Will check design with electronics group for FADC analog output
- Possible readout schemes
  - FADC only (default)
  - FADC + VETROC
  - VETROC only : needs to be evaluated

  - Preferred : Add TDC readout for each Cerenkov channel 232 VETROC additionnal 700 K$, could improve Cerenkov trigger

  - Need simulation to evaluate options
  - Need to follow with electronics group to start testing (anyone from Cernkov group interested ?)

TOF options

- Expected timing resolution 80 to 50 ps
- Default readout
  - NINO + TDC : 20 ps timing resolution
- R&D MRPC : 20 ps
  - Sampling TDC ASICs : PSEC4/5, SAMPIC, DRS4 give 5 to 1 ps resolution
  - Need new chip DRS5 or PSEC5 to handle SoLID trigger rate (analog pipeline) (might develop for EIC)
- Depends on final detector choice

- Need to determine effect of photon background, might need sampling to deal with pile up

GEM readout

- SRS deployed in Hall B Prad
- MPD implemented in CODA
  - BLT testing few KHz
  - Optical fiber readout to be implemented for high rate test (100 MB/s to 1.6 GB/s)
- Preliminary results from Weizhi : one sample no deconvolution not sufficient, new occupancy number
- Data reduction on SSP for SBS
- On chip deconvolution (implemented in MPD) still an option if needed
- preRD to get VMM3 chip

SIDIS event size

Occupancies with one sample readout by Weizhi , rates for 100 KHz

GEM	Occupancy	Number of strips	XY strips	Strips per chambers	Event size (bytes)	Data rate 100 KHz	MB/s
1	2.21	453	906	27180	2402.712	240271200	240.2712
2	8.78	510	1020	30600	10746.72	1074672000	1074.672
3	3.63	583	1166	34980	5079.096	507909600	507.9096
4	2.31	702	1404	42120	3891.888	389188800	389.1888
5	1.78	520	1040	31200	2221.44	222144000	222.144
6	1.3	640	1280	38400	1996.8	199680000	199.68
Total	20.01	3408	6816	204480	26338.656	2633865600	2633.8656

GEM dominating (35 bigger than initial proposal) 2.6 GB/s same requirement as PVDIS for L3

Need to look at FADC occupancies

Pre RD hardware : detector test stand

FADC 250	4500	4	18000
VETROC	4500	2	9000
TD	3000	1	3000
CTP	7000	1	7000
SSP	5000	1	5000
TID	3000	1	3000
SD	2500	1	2500
FADC trigger Dist	4000	1	4000
VXS crate	15000	1	15000
VME CPU	4500	1	4500
Optical fiber	100	20	2000
Computer	3000	1	3000
MPD	4500	1	4500
Network router	10000	1	10000
Total			72500

Added additionnal 10 K$ for MAROC and 15 K$ for VMM3 : total 97 K$

Manpower

- JLAB :
  - Alexandre Camsonne
  - Robert Michaels (Compton development)
  - Steve Wood
  - Electronics group
  - DAQ group
- Stony Brook
  - Seamus Riordan
  - Krishna Kumar
  - Postdoc
  - Student
- UVA : Danning Di GEM readout (SBS / Tritium)
- University New Hampshire : Shujie Li (part time)
- University of Columbia (summer) : Hanjie Lu

Could use a full time student

L3 farm (2c1)

- Have digitized data for GEM for SIDIS and PVDIS
- Weizhi has tracking algorithm take 2 to 10 ms to process one event so about 1000 nodes for 100 KHz
- Need :
  - Other include detector data
  - Additionnal reduction algorithm
  - Implement tracking
  - Test on Hall D or DAQ cluster
- Discussion with HPC/IT

L3 trigger (2c1)

- 2.5 to 10 ms for tracking using Kalman Filter (preliminary)
- PVDIS : 20 KHz

200 cores per sector

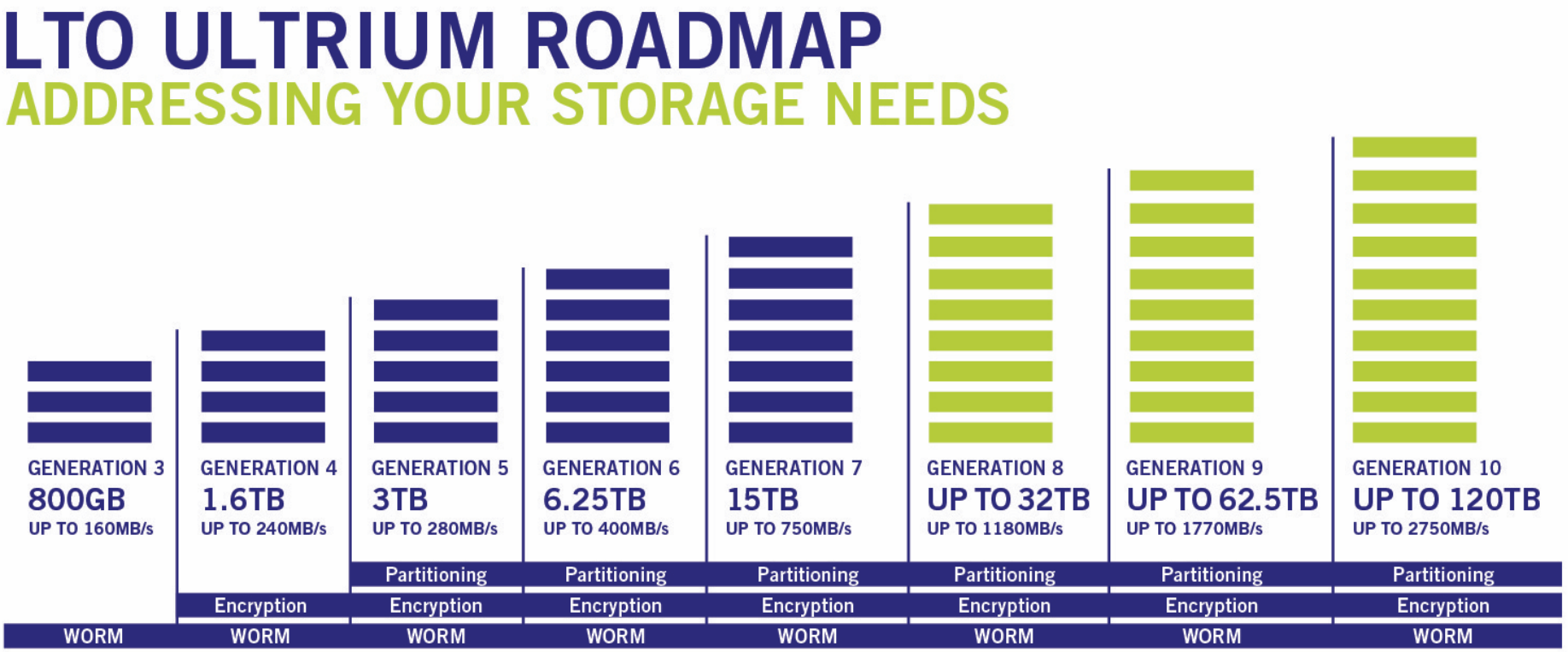
6000 cores total

- SIDIS
  - 1000 cores for 100 KHz

L3 trigger (2c1)

- Discussed with HPC and IT
  - Network upgrade :
    - Current : 2 x 10 Gbit /s = 2 * 1.2 GB/s from counting house to Computer center
    - Can be upgrade to 40 Gbit/s when cost go down (~5 years)
  - Tape SILO TS3500
    - 16 drives :
      - 6 LTO6 200MB/sx6 + LTO7 300 MB/sx8 = 3.6 GB/s
      - LTO7 300 MB/s x16 -> 4.8 GB/s
      - LTO8 472 MB/sx16 -> 7.5 GB/s
    - Could add second library (150 K$ and each drive 28 K$)
  - L3 could be located in CC and dynamically allocated (free !)
  - Need to let IT know the requirements, could invest yearly, need about 2000 today cores

LTO timeline



Bottomline : 3 GB/s is reasonable by 2020, L3 farm optional

Tape costs (2c2)

		Days	Data rate	Seconds	Total data TB	Double	DLO5 in $ 2010	DLO6 in $ 2012	DLO7 in $ 2015	DLO8 in $ 2020?
E12-11-108	Pol proton	120	250	10368000	2592	5184	259200	155520	62208	30375
E12-12-006	J/Psi	60	250	5184000	1296	2592	129600	77760	31104	15187.5
E12-10-006	Transv. Pol. 3He	90	250	7776000	1944	3888	194400	116640	46656	22781.25
E12-11-007	Long. Pol. 3 He	35	250	3024000	756	1512	75600	45360	18144	8859.375
E12-10-007	PVDIS	169	250	14601600	3650.4	7300.8	365040	219024	87609.6	42778.125
	Total	474		40953600	10238.4	20476.8	1023840	614304	245721.6	119981.25
Actual days	Actual years		Time in s			Per year	394200	236520	94608	46195.3125
948	2.60	474	40953600							

About 17K$ per PB, 11K$ per PB for tapes about 250 K$ for 20 PB
Cynthia would like about 70 K$ per year in tape (50 K$ per year at 250 MB/s), but 300 K$ is not unreasonable if planned in advance
Numbers don’t include compression (additionnal factor of 2)
Expected to go down by a factor 5 by 2020

Beam test

- 11 GeV beam available
  - Test detectors :
    - GEM
    - Calorimeter
    - MRPC
    - Cerenkov
  - Background measurements
- Some hardware available :
  - FADCs, MAROC
- Starting paperwork : getting ready for Calorimeter, GEM, LGC test

Hardware

- Trigger test HCAL : 16 FADC + GTP
  - Trigger test completion in about 2 months

- GEM :
  - 5 MPDs
  - First iteration of CODA library
  - Implementation optical link readout (2 months)
  - SRS : successfully used up to 5 KHz

Available in October

- SBS projects (DOE review November)
  - GTP/VTP calorimeter trigger test
  - GEM : preliminary performance

- PVDIS deadtime systematic using Compton test stand, implement simulation if enough time
- L3 : most likely possible and not needed

Simulations needs

- GEM occupancies and digitization SIDIS for event size, occupancy and tracking (Ole, Zhiwen, Weizhi Duke) ✓
- Updated trigger rates PVDIS, SIDIS(Zhiwen, Rakitah) ✓
- FADC digitization PVDIS : realistic PID (?)
- Cerenkov simulation only timing readout no FADC(?)
- Effect 1 sample vs 3 samples GEM (Weizhi) and 20 samples vs time integral SIDIS (?) ✓
- Full FADC trigger simulation
- MRPC simulation : response to background

Communication with other groups 2c3

- Try collaborate with Hall D
- Constant communication with JLAB DAQ and electronics group
- Hall C, SBS interested in using VETROC for logic and readout
- check experience with APV and FADC from HPS and PRAD
  - Already planning to reuse HPS trigger scheme

Forgotten recommendation

- Bunker design
  - Radiation
  - Cooling of bunker to be evaluated / design

Recommendations 2c

1. ✓ a)The plans for the High Level Trigger and b) the needs for slow control (see Brad's talk) need to be worked out in detail and the implications for resources need to be evaluated.
2. The implications of the need for these resources in the context of availability of resources at the laboratory need to be understood.
3. ✓ Closer communication with the other JLab experiments and the JLab computing center is strongly encouraged.
4. Having a functional simulation and reconstruction routines as soon as possible should be a high priority in the software effort. Such software will pay off many times over in experimental design and avoiding pitfalls. (Ole's talk)

Conclusion

- New results from Simulation
  - PVDIS rate lower 12KHz, not an issue
  - SIDIS :
    - 1 sample GEM readout seems to work and with occupancies similar to PVDIS data rate
- Up to 3 GB/s most likely can be handled by SILO, L3 most likely not required and could be available mostly for free
  - To do :
    - TOF background
    - Need to check J/Psi and TCS occupancies, rates and efficiencies
- MAROC default option for Cerenkov readout
- TOF : PSEC5 preferred option, need simulation
- PVDIS deadtime : hardware setup, ongoing study
- Test run in beam
- Start work on document update