GEM Updates from China

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University of Science and Technology of China

SoLID Collaboration Meeting

August 27, 2016

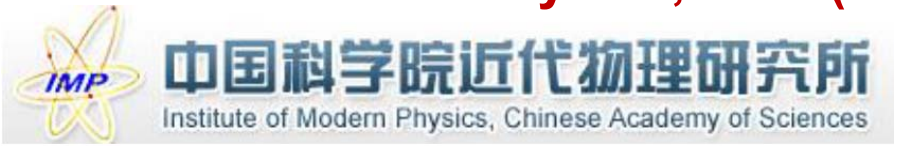
JLab

SoLID-GEM Chinese Collaboration

China Institute of Atomic Energy (CIAE)

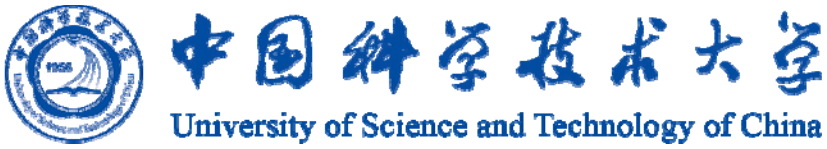
Lanzhou University

Institute of Modern Physics, CAS (IMP)



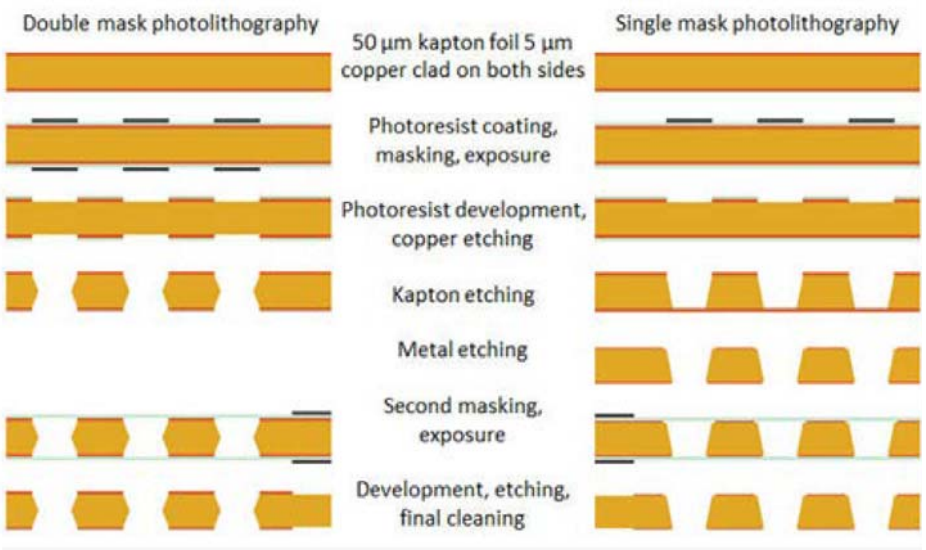
Tsinghua University

University of Science and Technology of China (USTC)



Upgrades from CIAE

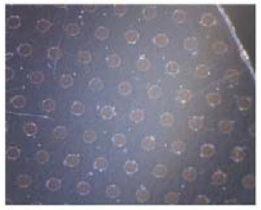
The Procedure of GEM Foil



Collaborated with a Factory

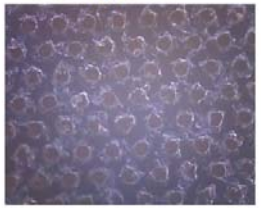
Comparison of Foils

Insufficient development

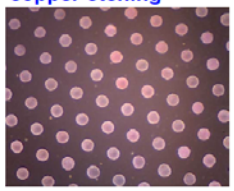


Good development

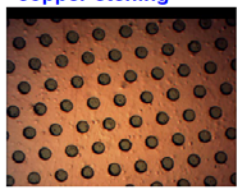
Excessive development



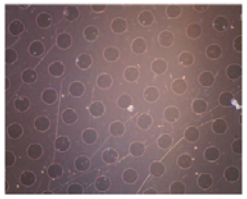
Insufficient copper etching



Good copper etching



Excessive copper etching

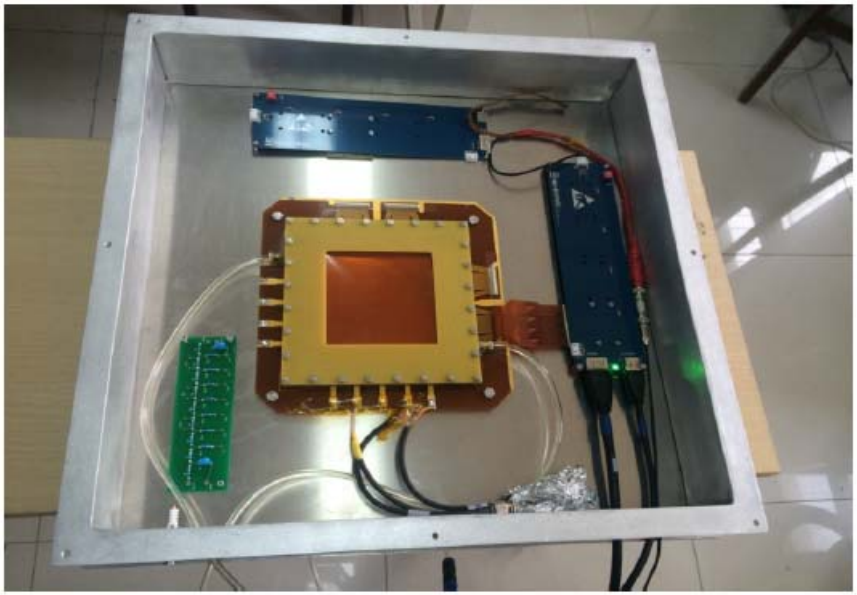


Progress on GEM foil

- CIAE has found a factory to collaborated. The factory is not very big, but has good facilities.
- The factory has produced 30 GEM foils for CIAE, but only 5 of them passed high voltage test. The reason for this is: firstly, they are not very familiar with the fabrication process of GEM foil; secondly, the solution is not very clean. To solve this issue, CIAE is going to support the factory with buying a new etching equipment, which will be used only for GEM foil.
- CIAE has delivered GEM foil to CCNU to test.

The upgrade of Lab

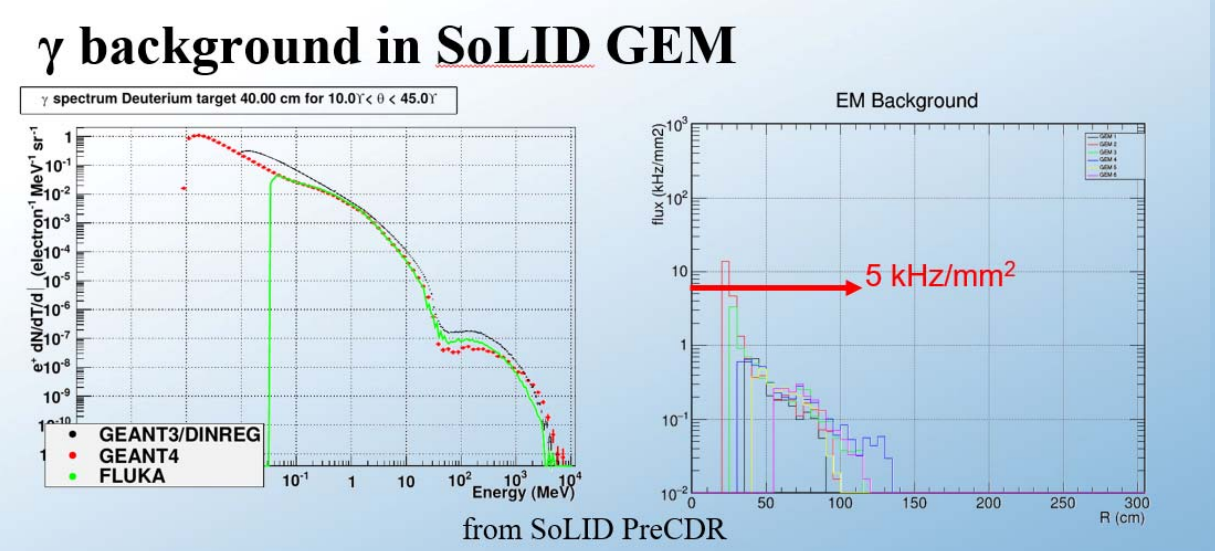
- Lead box
- X-ray generator
- 3D GEM test platform
- New test chamber



Updates from LZU

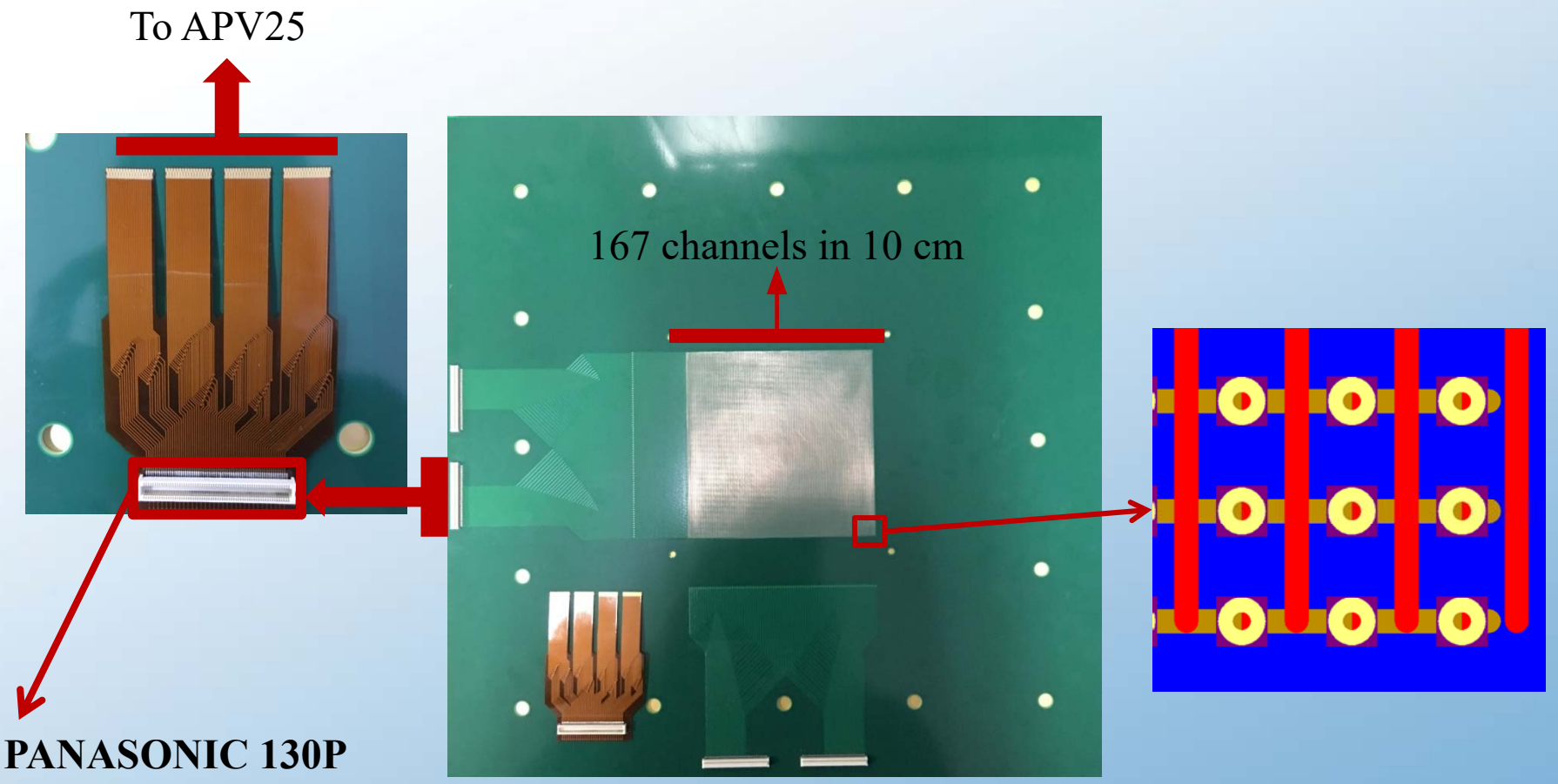
Goal

- reduce the local rates by rejecting γ signals according to the time information
- try to reduce the load of DAQ by clustering on hardware level (FPGA)

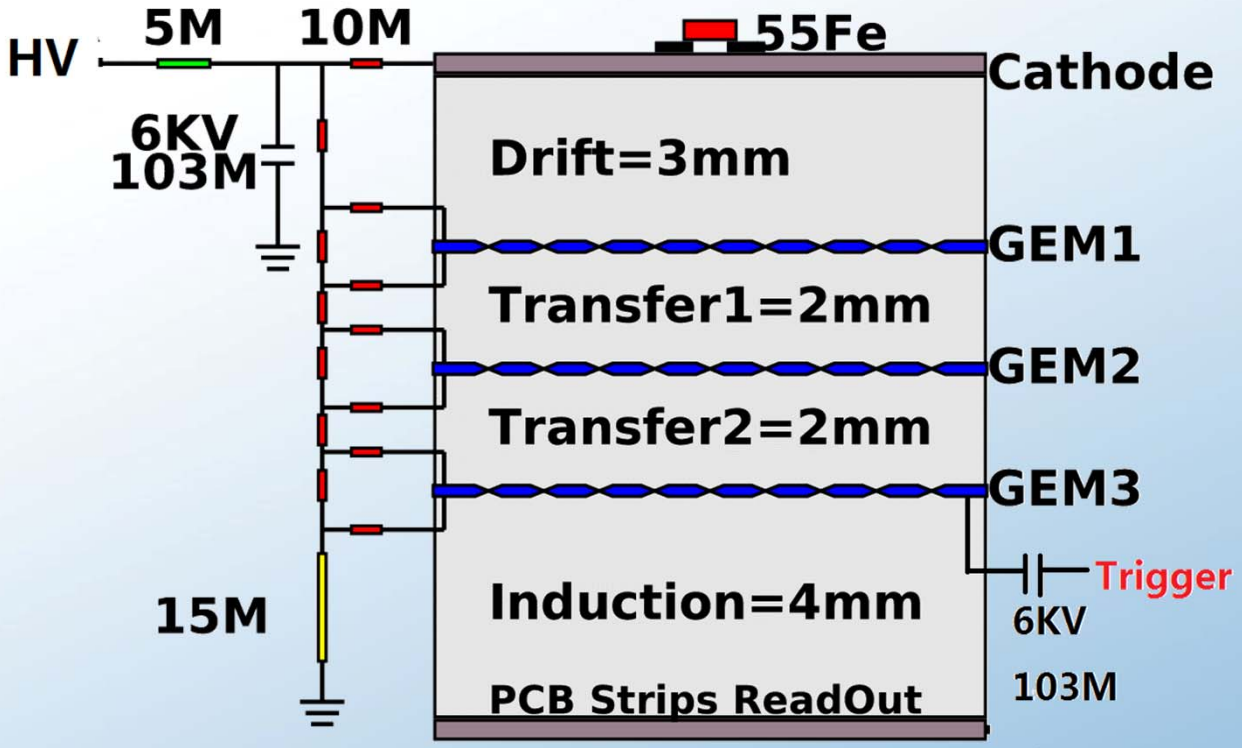


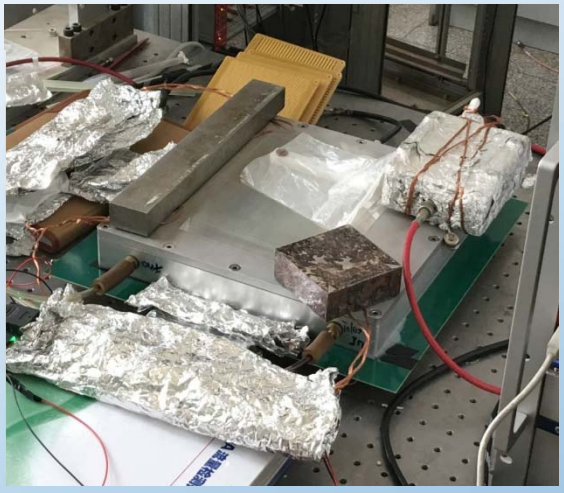
R&D of GEM detector

New readout panel

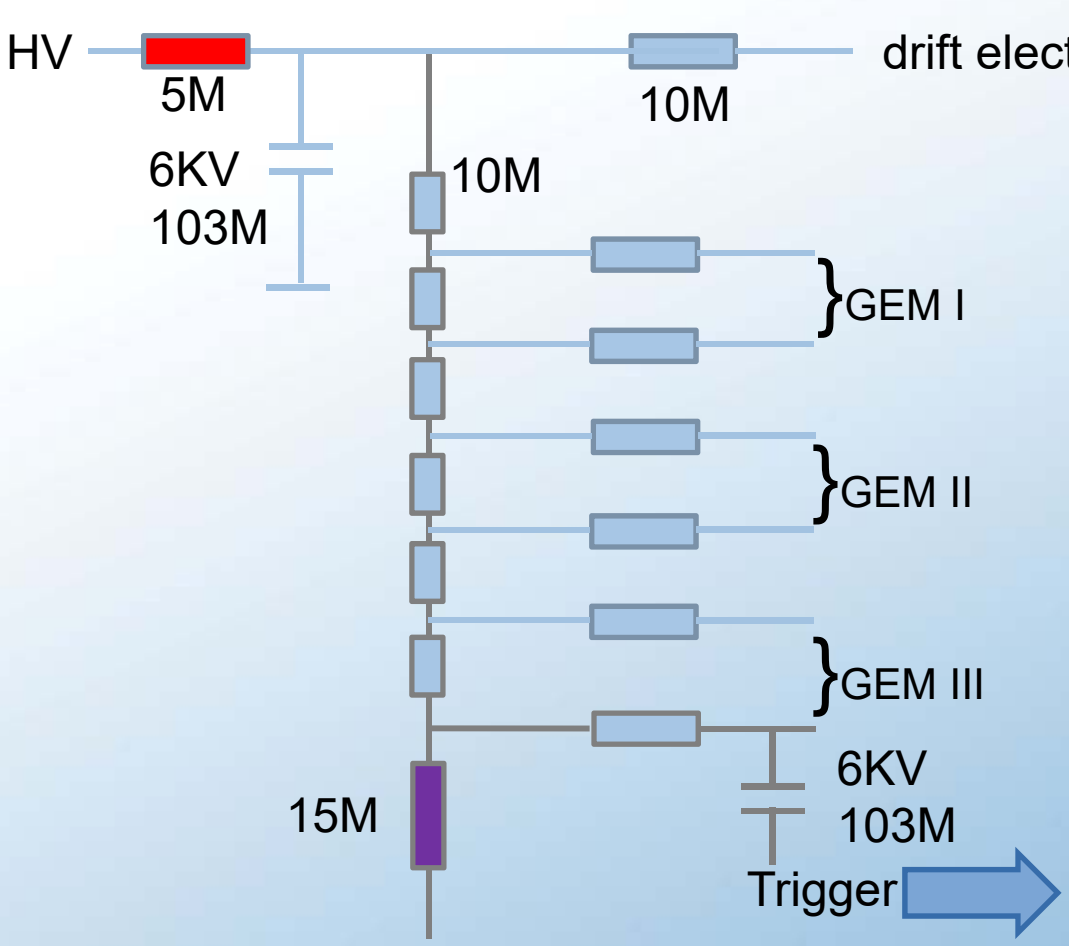


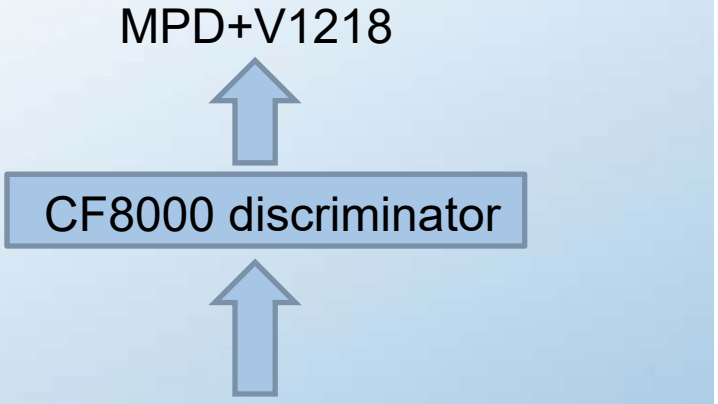
New version of triple-layer GEM detector

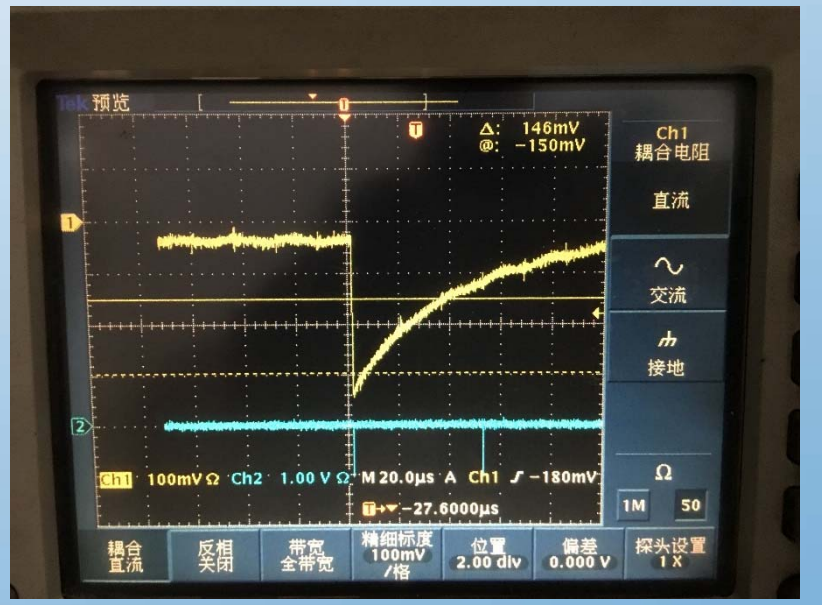




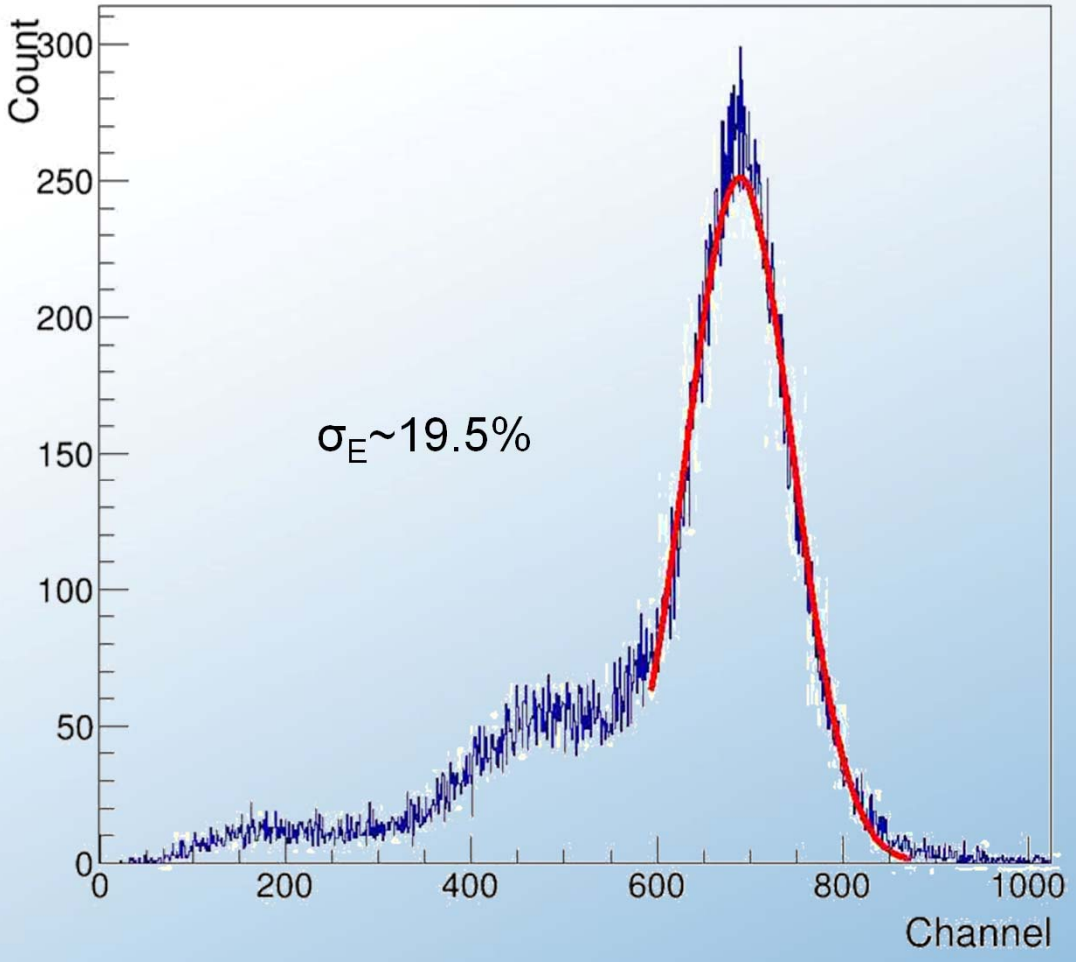
High voltage and trigger

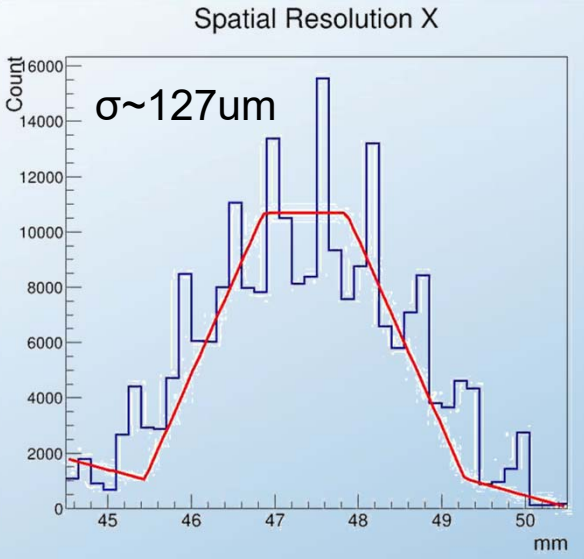


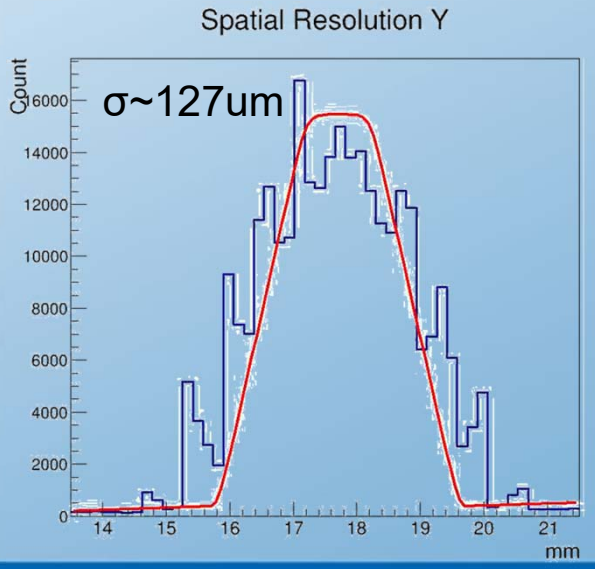




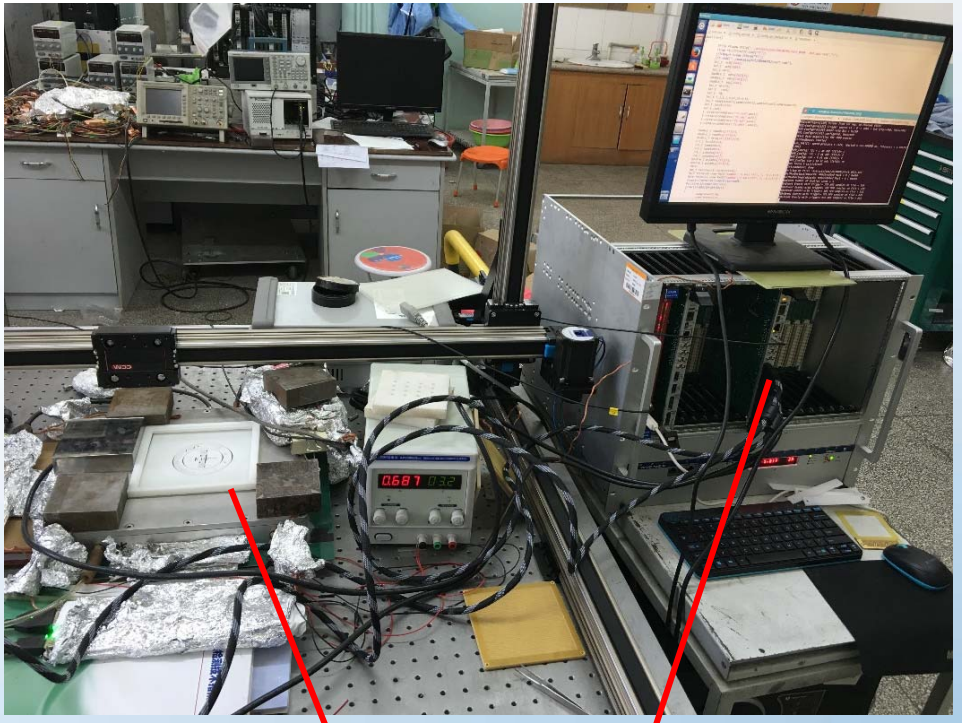
Test result of new detector (^{55}Fe)

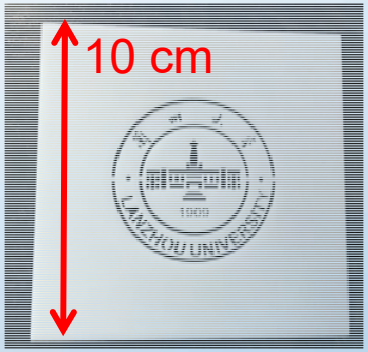


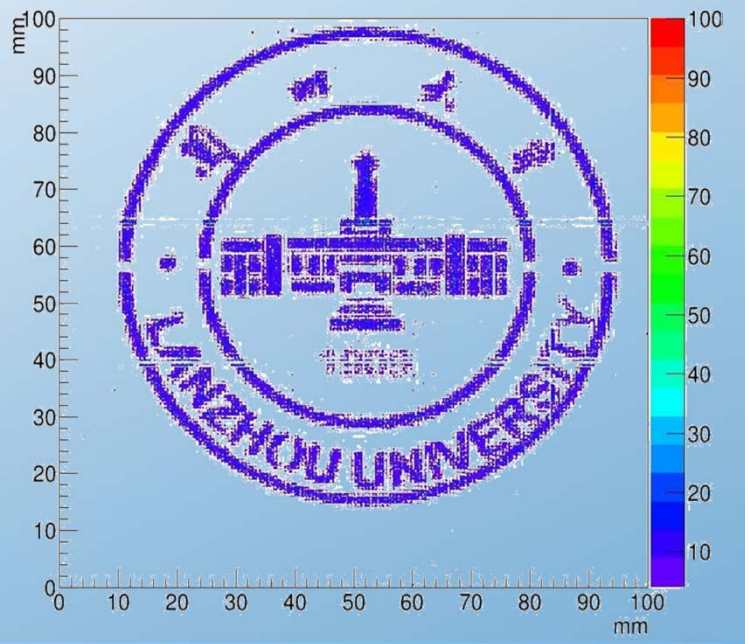




x-ray imaging by new detector and Daq

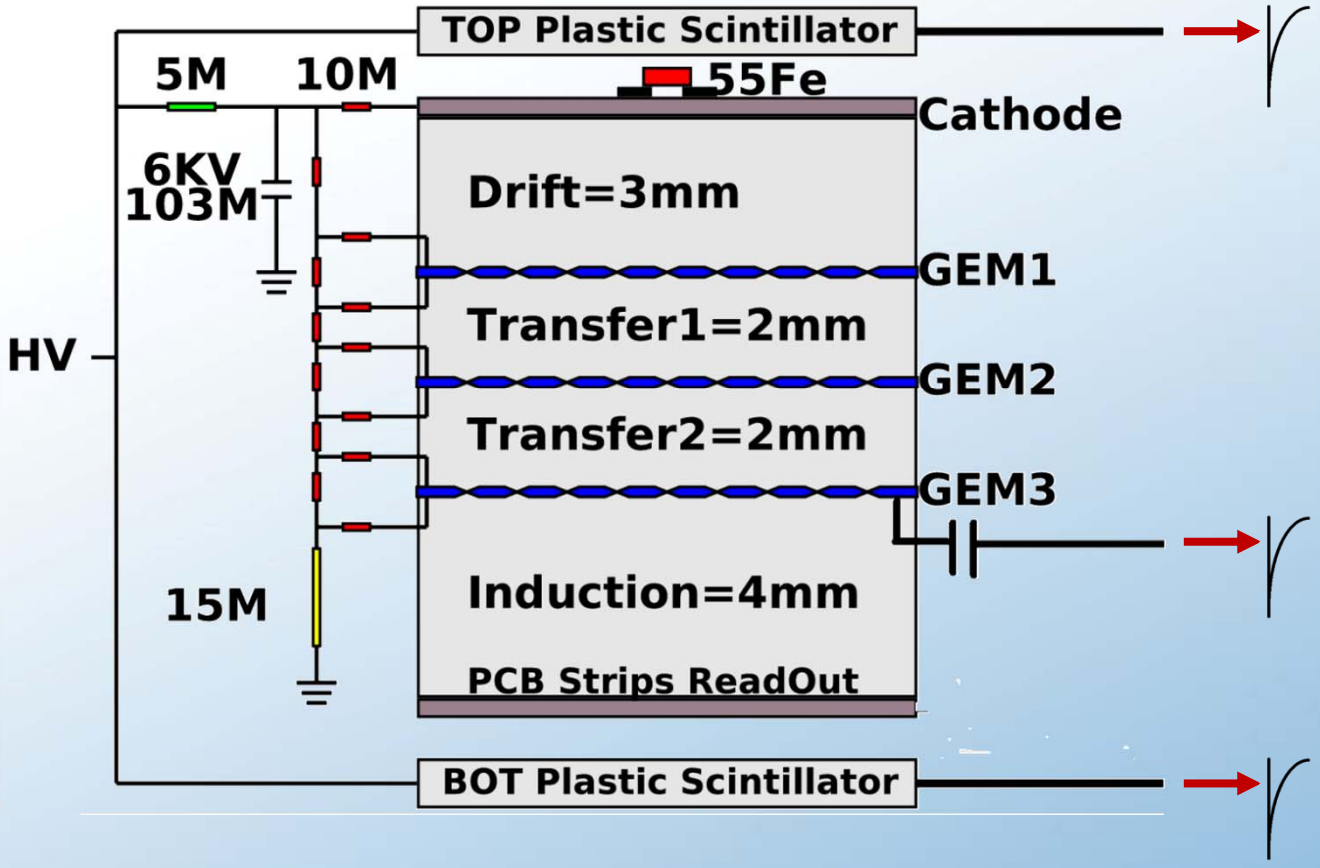


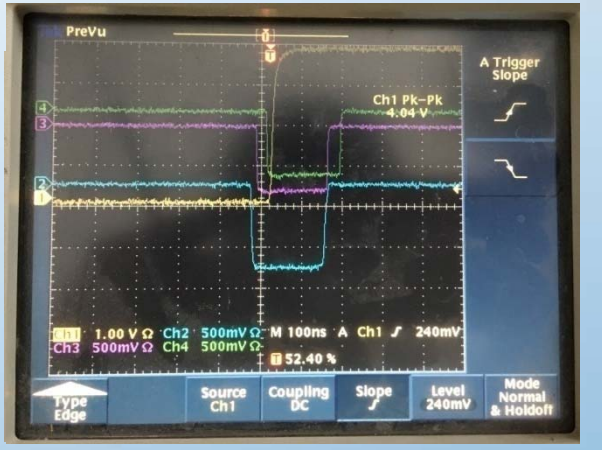




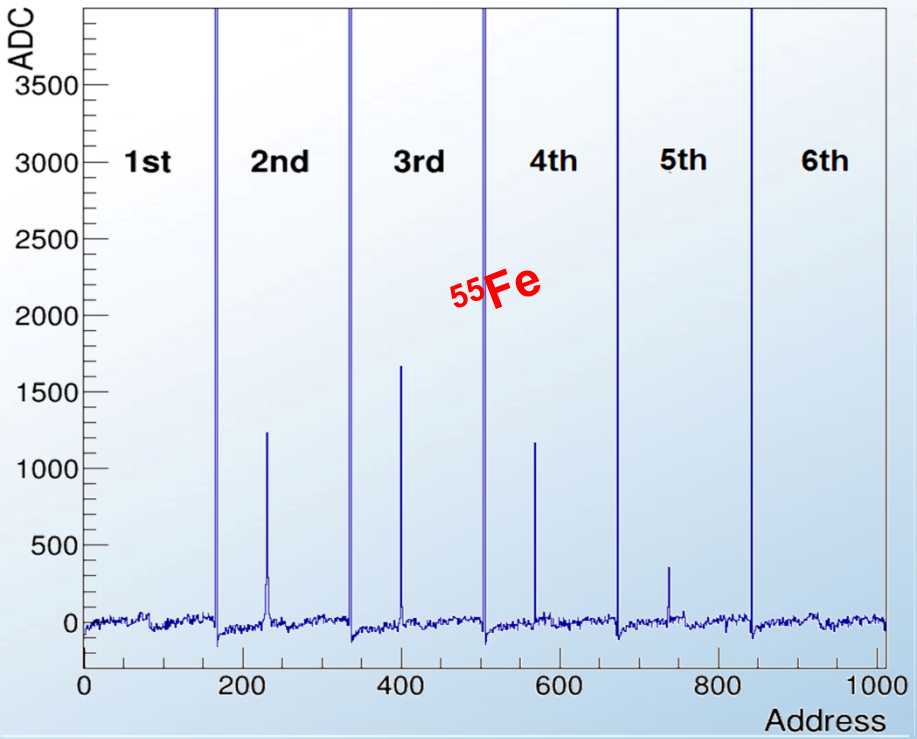
R&D of GEM-Daq

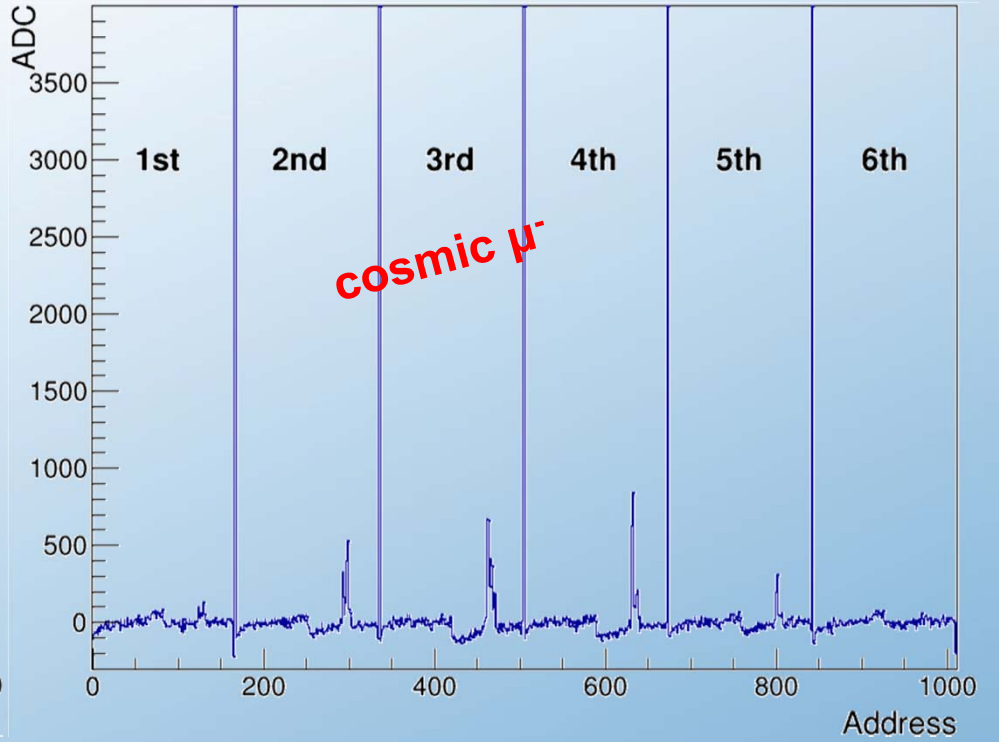
coincidence trigger to identify muon and photon



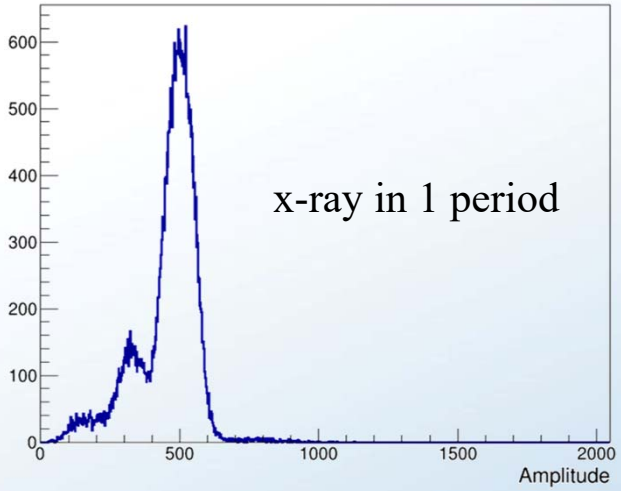


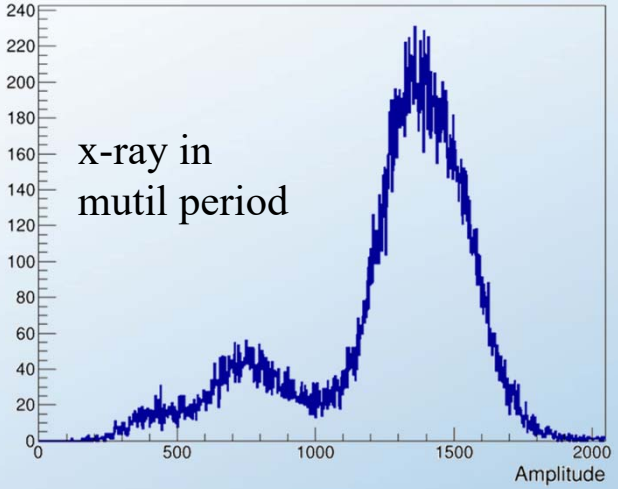
Real signals recorded in Daq

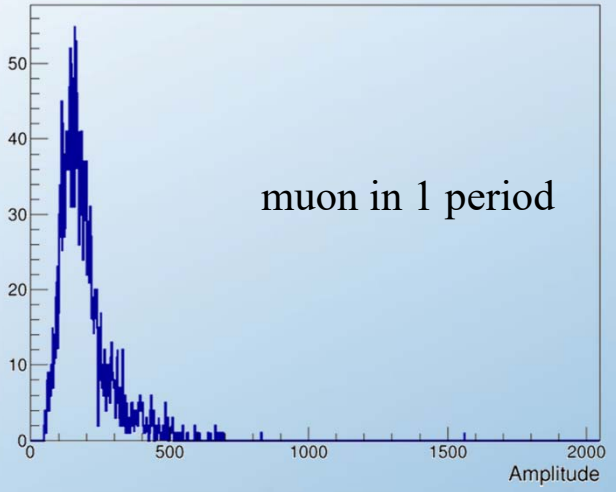


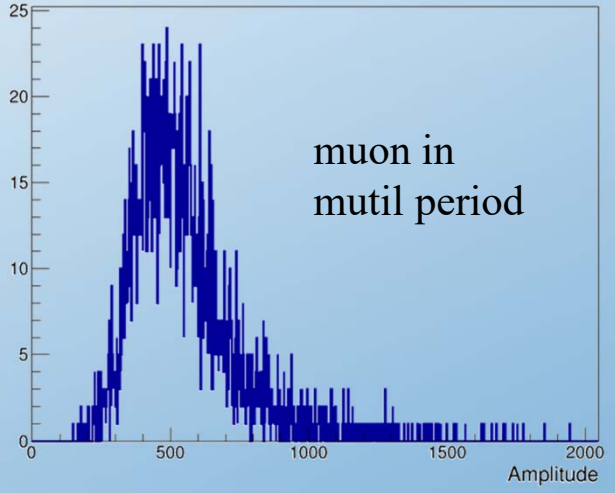


comparing signal amplitudes of different particle







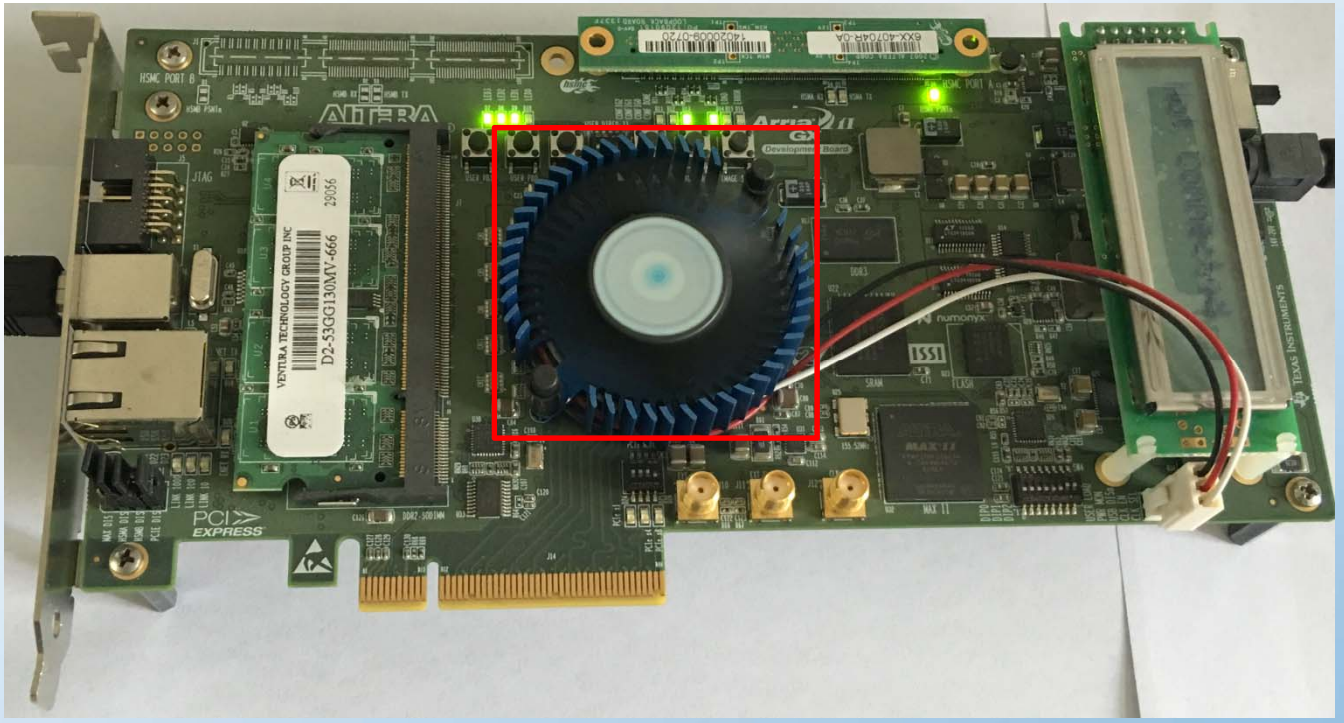


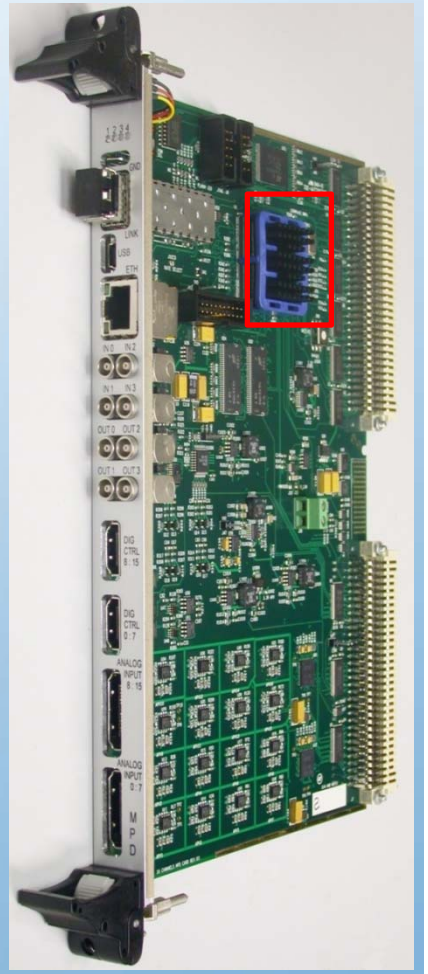
Steps of online track reconstruction

- **Divide signals into time slices (1 period for each)**
  - Segmentation in readout plane —— cut on signal amplitude
  - Combine adjacent segment —— identify clusters of hits
- **Process multi time slices**
  - Combine adjacent time slices —— distinguish if signal continues
  - Integrate multi time slices —— identify the start and end of a signal

Development board: ARRIA GX FPGA toolkit

EP1AGX60DF780C6N





Resources consumption budget (2048 chs)

reports of our code:

SPM.v

Flow Summary

Flow Status	Successful - Wed Aug 03 15:06:08 2016
Quartus II 64-Bit Version	14.1.0 Build 186 12/03/2014 SJ Full Version
Revision Name	retrack
Top-level Entity Name	retrack
Family	Arria II GX
Device	EP2AGX125EF35C4
Timing Models	Final
Logic utilization	38 %
Combinational ALUTs	14,092 / 99,280 (14 %)
Memory ALUTs	0 / 49,640 (0 %)
Dedicated logic registers	32,224 / 99,280 (32 %)
Total registers	32224
Total pins	144 / 512 (28 %)
Total virtual pins	0
Total block memory bits	73,216 / 6,727,680 (1 %)
DSP block 18-bit elements	3 / 576 (< 1 %)
Total GXB Receiver Channel PCS	0 / 12 (0 %)
Total GXB Receiver Channel PMA	0 / 12 (0 %)
Total GXB Transmitter Channel PCS	0 / 12 (0 %)
Total GXB Transmitter Channel PMA	0 / 12 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)

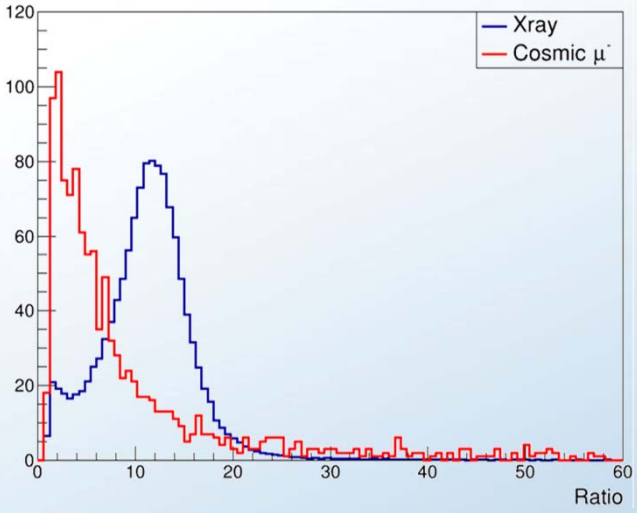
from INFN :

```
The fitting results without filters (actual version) are:
; Logic utilization                    : 56 %
;     Combinational ALUTs              : 21,247 / 48,080 ( 44 % )
;     Dedicated logic registers        : 13,382 / 48,080 ( 28 % )
; Total registers                      : 13661
; Total pins                           : 312 / 395 ( 79 % )
; Total block memory bits              : 1,808,252 / 2,528,640 ( 72 % )
; DSP block 9-bit elements             : 0 / 256 ( 0 % )
; Total GXB Receiver Channels          : 1 / 8 ( 13 % )
; Total GXB Transmitter Channels       : 1 / 8 ( 13 % )
; Total PLLs                           : 3 / 4 ( 75 % )
; Total DLLs                           : 1 / 2 ( 50 % )
```

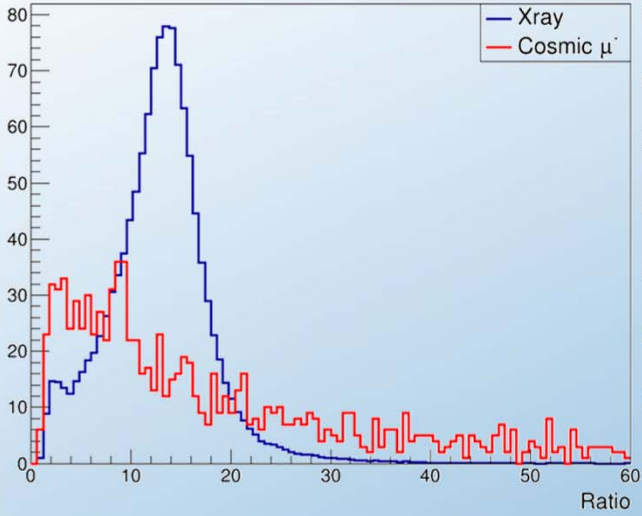
Iterms of resources	Total	Usage of current daq	Usage of out code
Combinational ALUTs	48,080	21,247 (44%)	14,092 (29%)
Dedicated registers	48,080	13,382 (28%)	32,224 (67%)
DSP	256	0	3(1%)
Block Memory Bits	2,528,640	1,808,252 (72%)	73,216 (3%)

Try to identify signals of different particle (data)

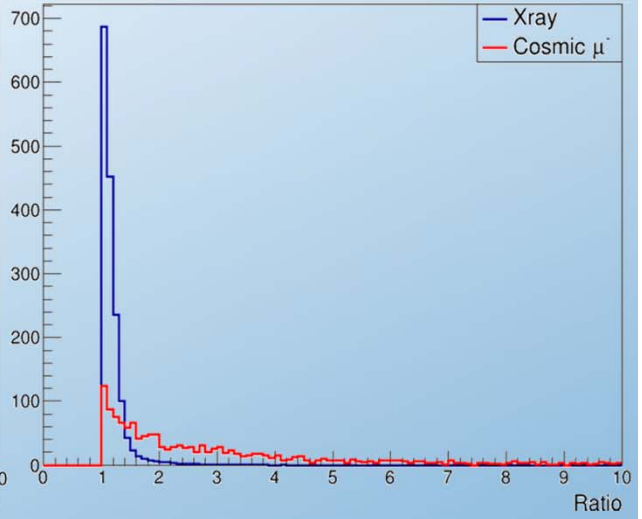
period2/period1



period3/period1



period3/period2



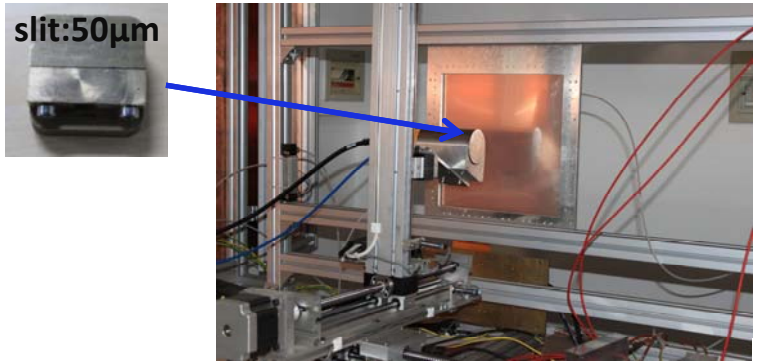
Future plan

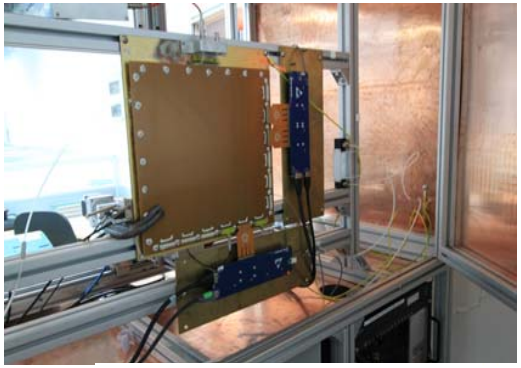
- **process multi time slices on FPGA**
- **test with real beam data?**
- **communicate with INFN experts**
  - try to merge our code into current firmware

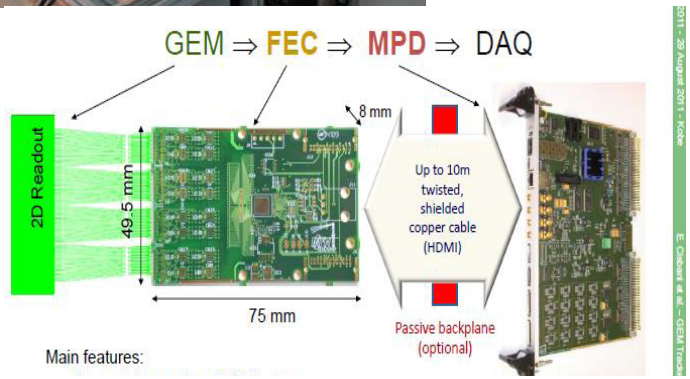
Updates from USTC

Spatial Resolution Test

- Tested GEM spatial resolution using collimated X-rays with the APV25-MPD readout system.

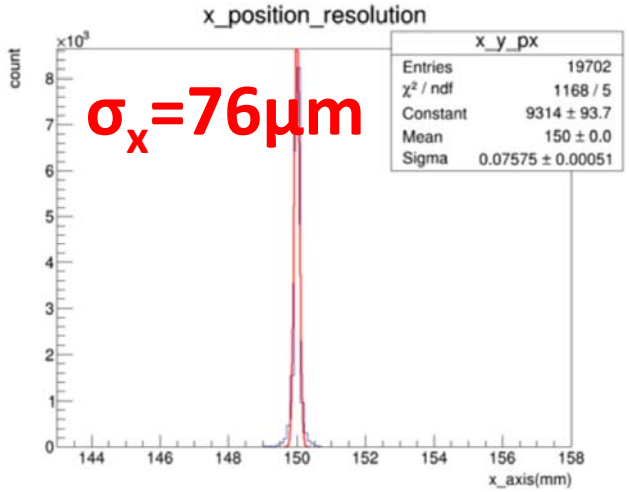




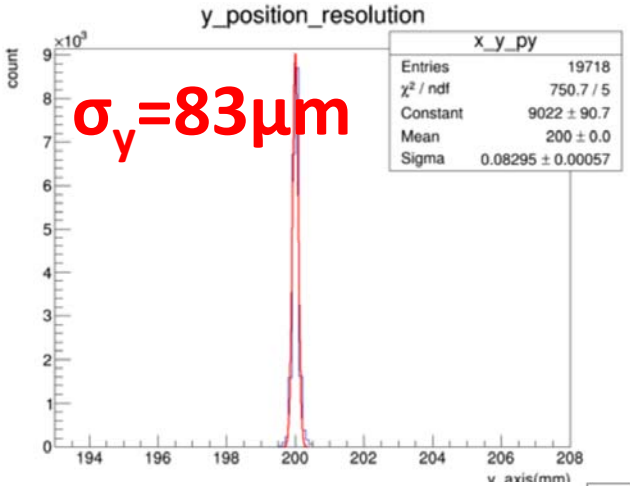


Spatial Resolution Results

- 2-d readout board with strip pitch ~ 400μm
- Position taken as the center of gravity of charge



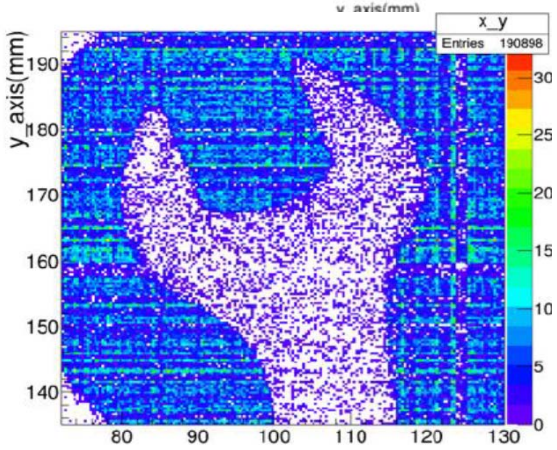
σ_x=76μm



σ_y=83μm

Intrinsic resolution better than measurement:

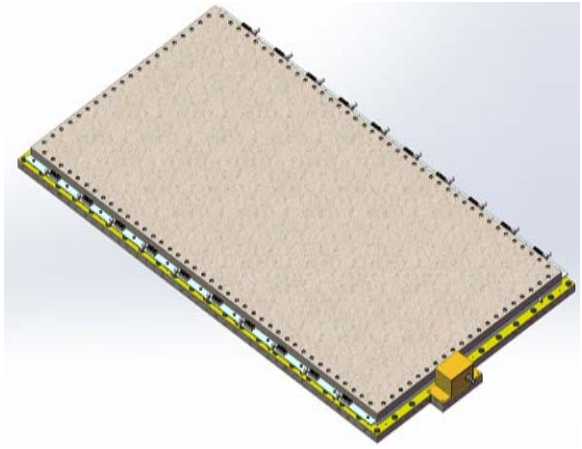
- Slit width
- Range of initial photon-electrons
- common mode noise
- APV25 saturation

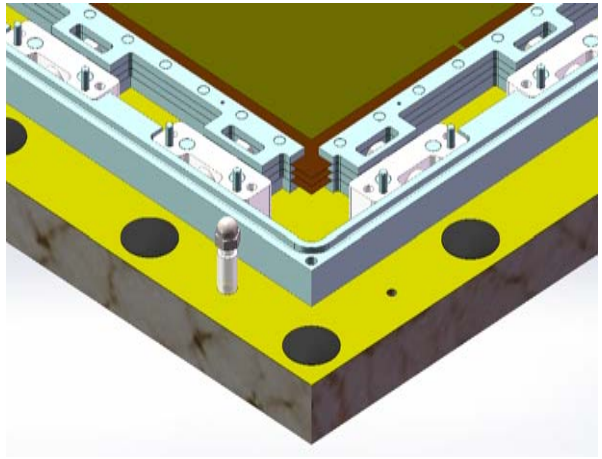


Additional test: 2D X-ray imaging

Low-mass Design with Self-stretching

- 0.5m*1m active area with no spacers.
- Drift and readout boards are made of Kapton + Cu
- All screws and nuts are plastic.
- Honeycomb on both top and bottom sides for mechanical support.



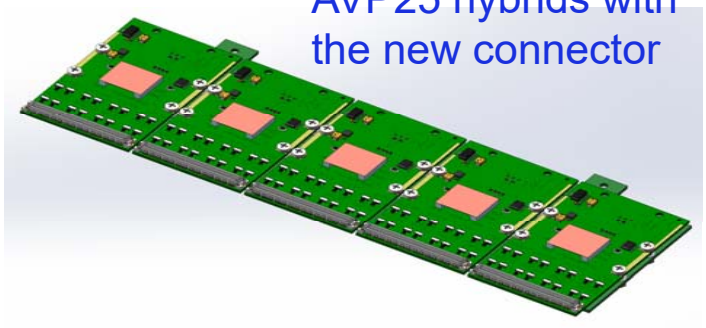


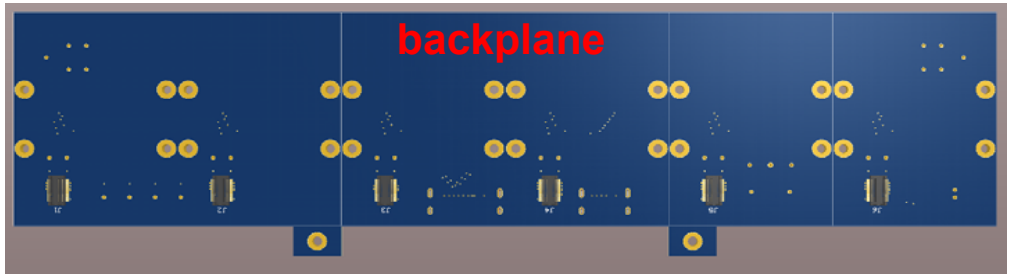
The whole design has been finished.

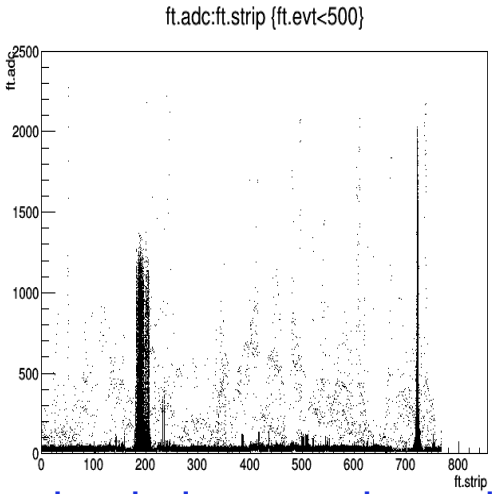
APV25 hybrid and backplane

- Changed the connector of the APV25 hybrid
  - From Panasonic 130-pin to Hirose 140-pin
- Designed and produced backplanes to host APV25 chips.

AVP25 hybrids with the new connector



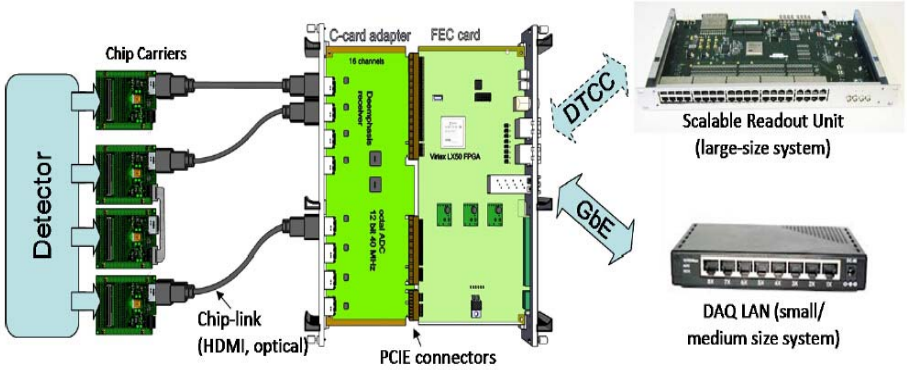


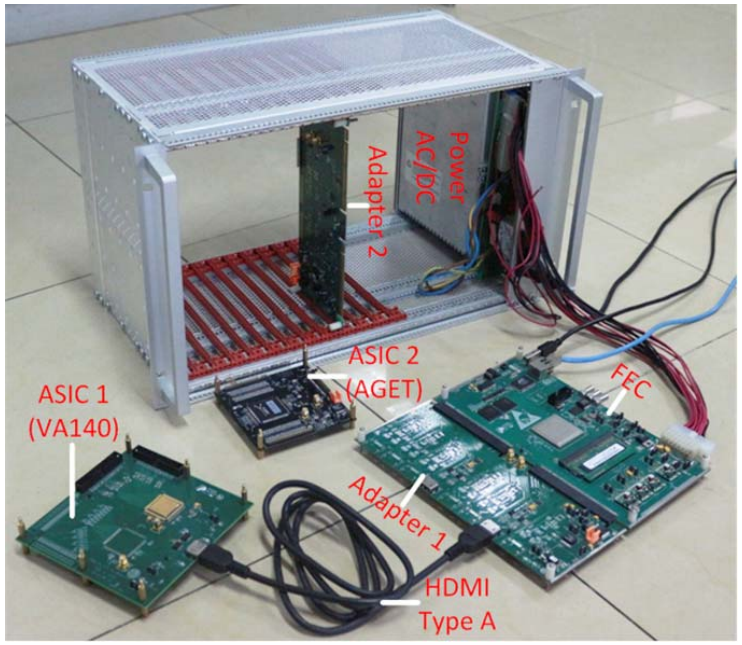


The backplane works well with APV25 and GEM. Noise level quite acceptable.

GEM Readout R&D

- Have been developing a general and scalable readout system for MPDG.
  - Main components: ASIC card, adapter card, front-end card

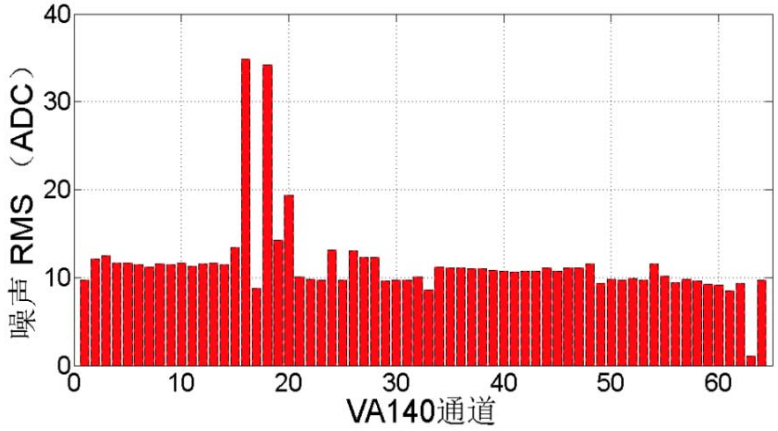


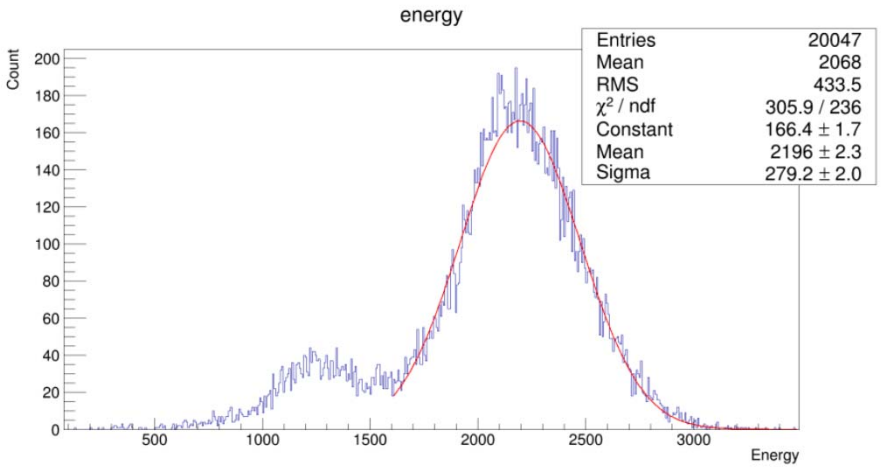


- Front-end chip: VA140 (not suitable for high rate application)
  - 64 channels
  - shaping time: 6.5µs
  - ENC<784e (Cd=100pf)
  - Dynamic range: 0-200fC
  - Linearity: 2%
  - Power consumption: 0.3mW/ch

Test with Detector

- Noise RMS ~ 0.7fC.
- Clear Fe-55 energy spectrum.
- Still a lot of work to optimize and finalize the readout system with actual detectors.





Summary

- CIAE
  - Progressing towards GEM foil industrialization
- LZU
  - Working on online gamma-rejection and clustering
- USTC
  - Low-mass self-stretching GEM and readout R&D