TOF readout for SoLID

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Readout options

- Amplifier Discriminators front end
  - NINO (CERN) (8 channels – 32 channels version)
  - GSI Padiwa (16 channels) 150 $ for 16 channels
  - MAROC (Omega IN2P3)

Need to check timing performance of discrimination and amplification

TDCs

- HPTDC 25 ps
  - V1290 (32 channels about 10 K$)
  - CAEN planning to develop better TDC
- FPGA TDCs
- TRB3 11 ps (192 channels / 2300 euros)
- VETROC JLAB 20 ps (need development) 128 channels about 6 K$ (5 board ordered for Compton, can test TDC)

Sampling chip

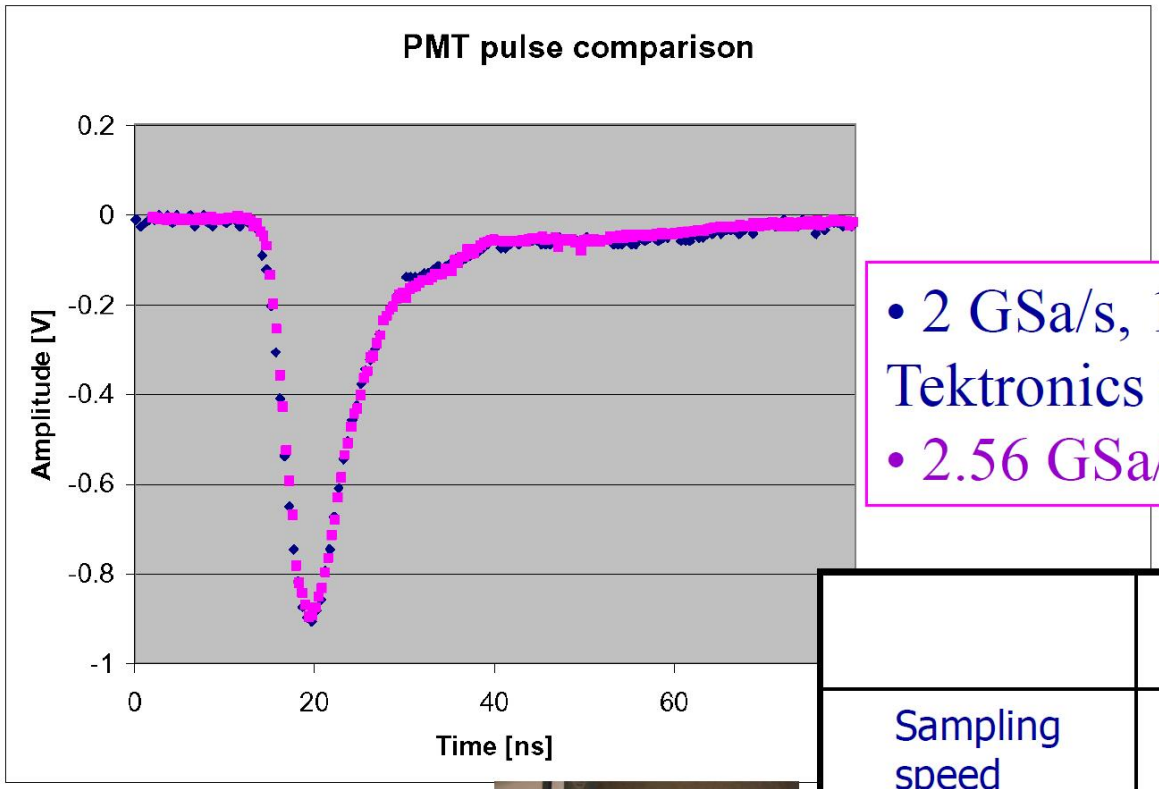
Chip	Sampling Frequency (GHz)	Bandwidth GHz	Number of samples	Number of channels	Readout frequency (MHz)	Resolution (ps)
PSEC4	4 to 15	1.5	256	6	40 to 60	9
SAMPIC	3 to 8.2	1.6	64	16 – 8 (at 10 GHz)	80	5
DRS4	0.7 to 5 GHZ	0.950	1024	9	33	1
DRS5	10	3	4096	32	300?	5?
PSEC5	5 to 15	1.5 to 2	32768	4	500	5?

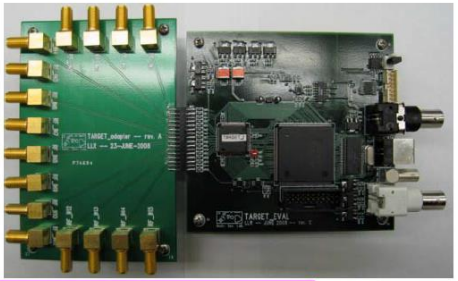
Latest generation with multilevel analog buffer : dead time less up to a few MHz and allow for L2 (DRS5)

PSEC5 update

- Interesting option
- Developed by University of Hawaii for HEP
  - Belle II
- Reasonable radiation hardness 10 to 20 MRad
- Funding by both HEP and NP
- P5p : prototype for 2017
- Commercialization and mass production being studied
- Standardization of readout (similar to SRS for TOF)
- Could go down to 15 $ per channel about 3K$ per wafer

The Giga Package

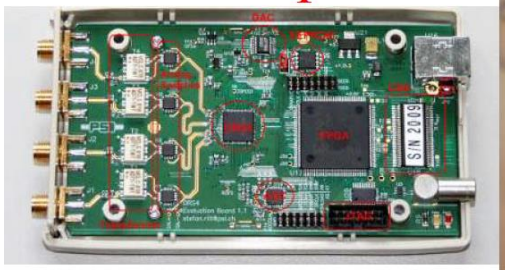


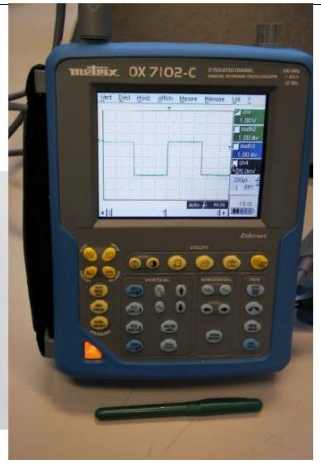


- 2 GSa/s, 1GHz ABW Tektronics Scope
- 2.56 GSa/s LAB

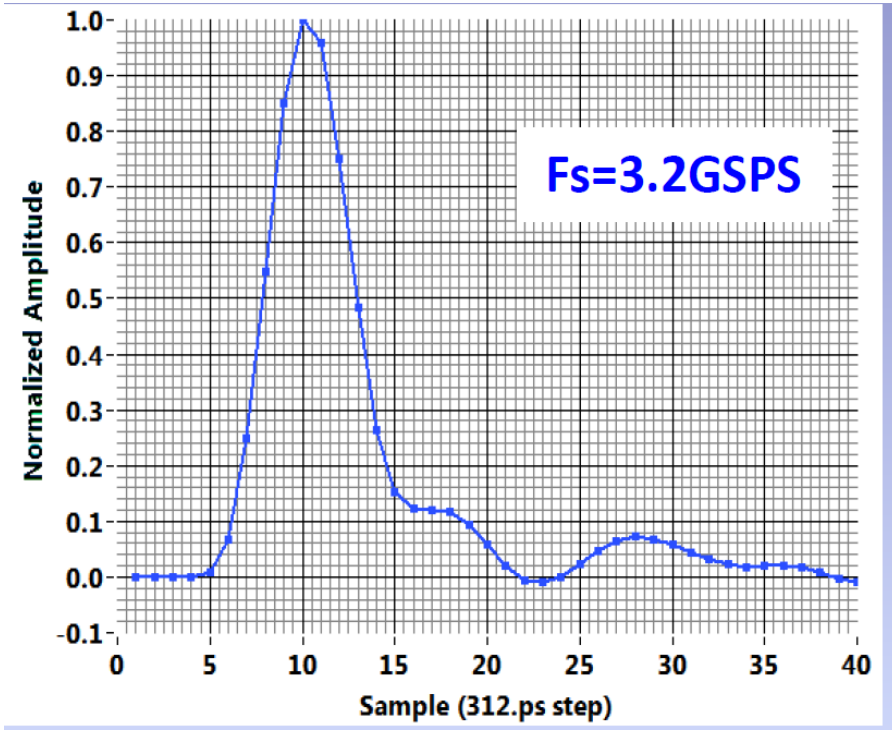
	WFS ASIC	Commercial
Sampling speed	0.1-6 GSa/s	2 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	<= 0.05W	Few W
Cost/Ch.	< $10 (vol)	> 100$

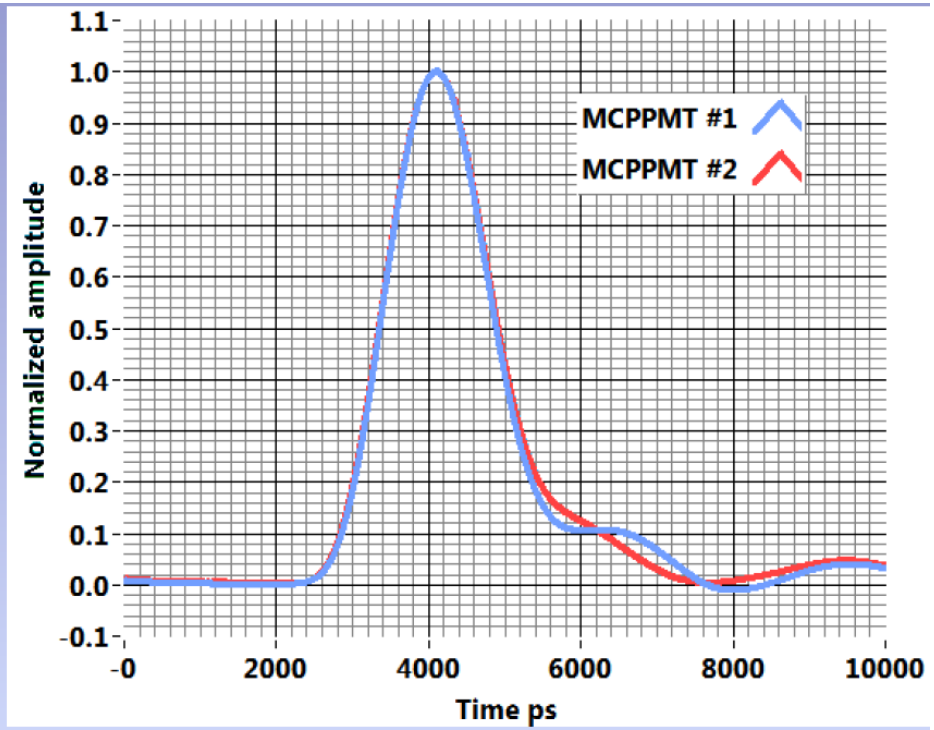
"oscilloscope on a chip"





Sampling chips





Concern for TOF

- Effect of background on TOF
  - Pile-up
- If need to record waveform :
  - Deadtime (sampling chip have deadtime, wait for new generation chip DRS5 prototype 2018)
  - Event size
    - Occupancy
    - Data reduction
- Cost (develop new electronics)

PreRD request

MRPC			
Gas system	20000		
Low Voltage	3000		
HV	10000		
VETROC	4500		
Front-end	5000		
VME64X crate	11000		
VME CPU	4500		
TID	4000		
SD	4000		
	66000		
Man power	Postdoc	0.1	TDC devel
	Electronics	0.2	TDC devel
	DAQ	0.2	
	Tech	0.2	Gas system

PreRD

- Develop high resolution TDC with VETROC
- Test stand for : additional test run in 11 GeV background environment, better PID (concern for pion efficiency)
- Test sampling chips

Conclusion

- Electronics is not a limiting factor for timing resolution (up to 1 ps)
- Baseline : A/D and VETROC for trigger and readout 20 ps resolution
- Additionnal development for better than 20 ps
- Need simulation to determine the need of sampling electronics
- Sampling electronics is better in term of timing and background but need to evaluate additional cost and data size
- Would work for MRPC or LAPPD