TOF read-out for high resolution timing

Alexandre Camsonne

SoLID collaboration meeting

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Outline

- SoLID requirements
- Sampling chips
- DRS5 example
- Option for electronics R&D
- Conclusion

Requirements for SoLID

- Timing resolution at least 50 ps
- Might need better depending on detector performances
- At least 60 KHz desired 200 KHz trigger rate
- Latency : 4 μs minimum up to 8 μs
- 3300 channels of MRPC
- Deadtimeless
- Need trigger signal to send to trigger to pipeline electronics
- Single rates : tested up to 20 KHz/cm2

Photon rate per area can range from 1-4kHz/mm2, which is 100-400khz/cm2
If we assume 5% percent photons will fire MRPC, we can have 5-20khz/cm2

Two options

- Depends on detector performance : better than 20 ps
  - Usual method : discriminator + TDC
    - Amplifier discriminator
    - TDC : ASIC or new FPGA technique
  - Waveform sampling
    - No discriminator
    - Full bandwidth
    - Better timing resolution up to 1 ps
    - Need algorithm to extract time
    - Or readout full waveform (very large amount of data)

Sampling chip

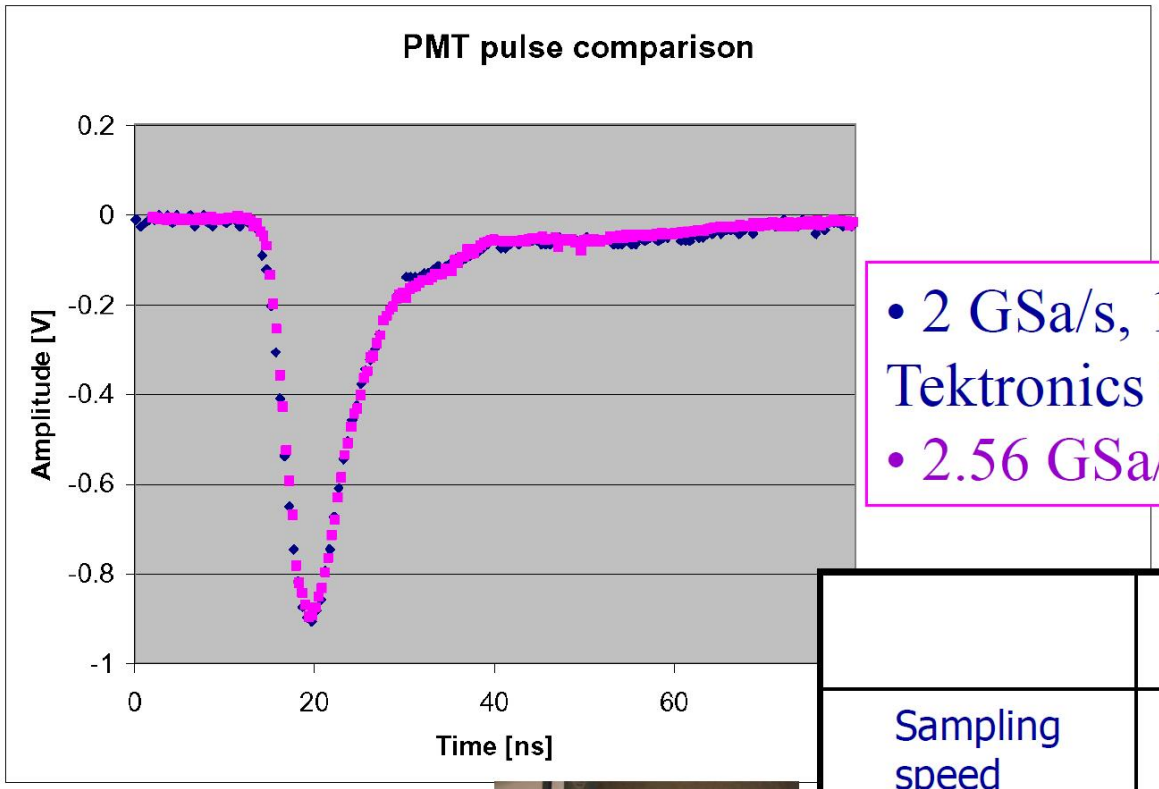
Chip	Sampling Frequency (GHz)	Bandwidth GHz	Number of samples	Number of channels	Readout frequency (MHz)	Resolution (ps)
PSEC4	4 to 15	1.5	256	6	40 to 60	9
SAMPIC	3 to 8.2	1.6	64	16 – 8 (at 10 GHz)	80	5
DRS4	0.7 to 5 GHZ	0.950	1024	9	33	1
DRS5	10	3	4096	32	300?	5?
PSEC5	5 to 15	1.5 to 2	32768	4	500	5?

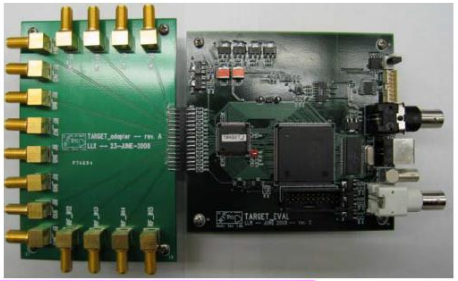
Latest generation with multilevel analog buffer : dead time less up to a few MHz and allow for L2 (DRS5)

PSEC5 update

- Interesting option
- Developed by University of Hawaii for HEP
  - Belle II
- Reasonable radiation hardness 10 to 20 MRad
- Funding by both HEP and NP
- P5p : prototype for 2017
- Commercialization and mass production being studied
- Standardization of readout (similar to SRS for TOF)
- Could go down to 15 $ per channel about 3K$ per wafer

The Giga Package

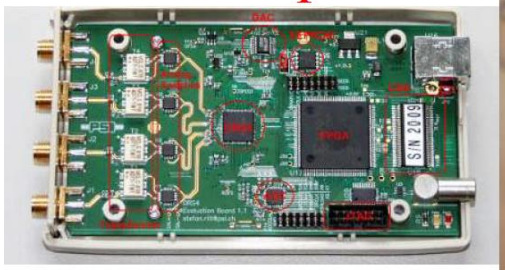


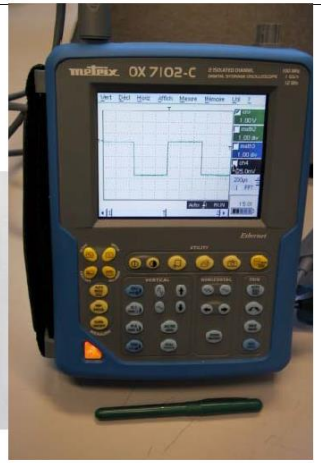


- 2 GSa/s, 1GHz ABW Tektronics Scope
- 2.56 GSa/s LAB

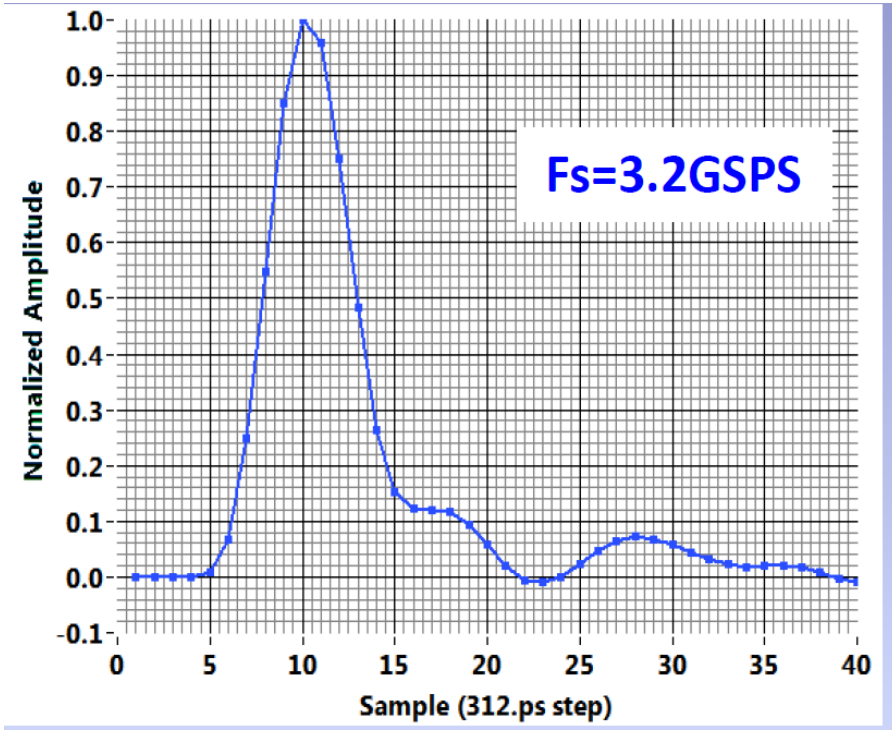
	WFS ASIC	Commercial
Sampling speed	0.1-6 GSa/s	2 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	<= 0.05W	Few W
Cost/Ch.	< $10 (vol)	> 100$

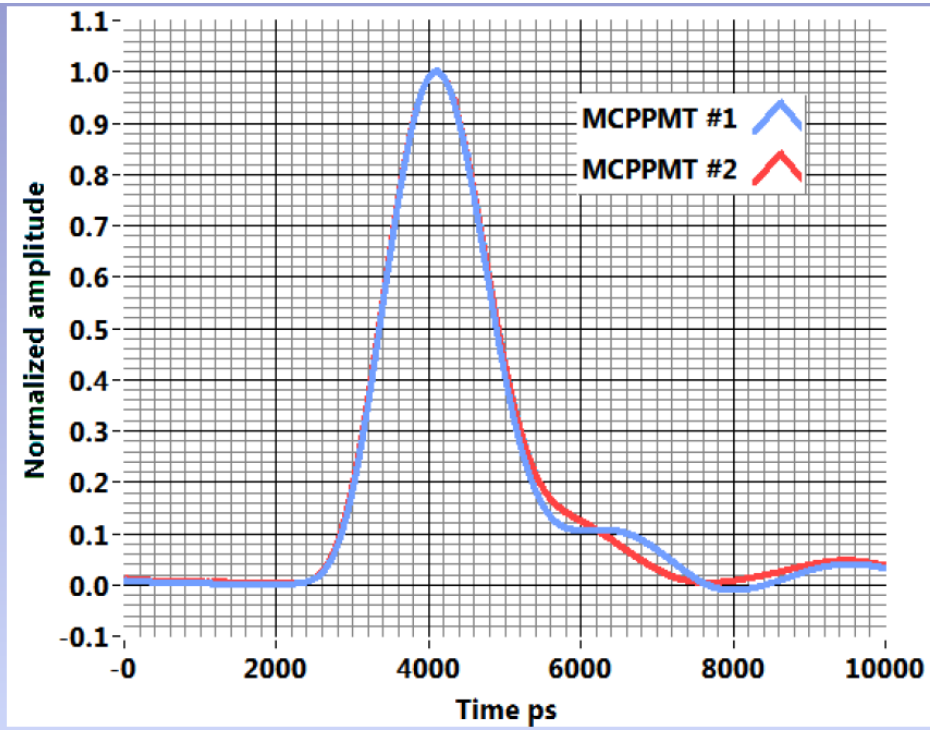
"oscilloscope on a chip"





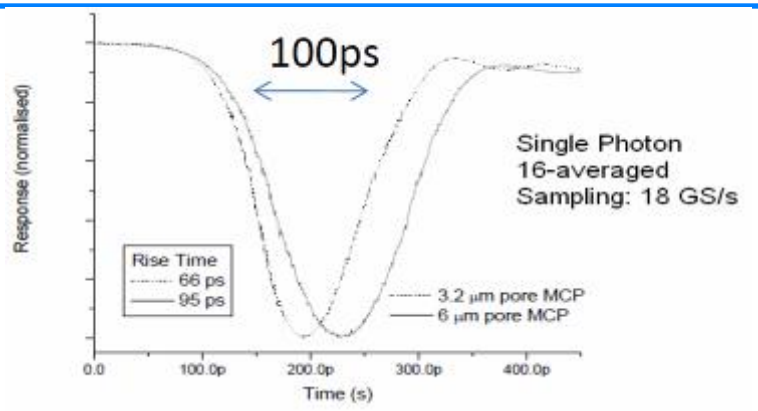
Sampling chips



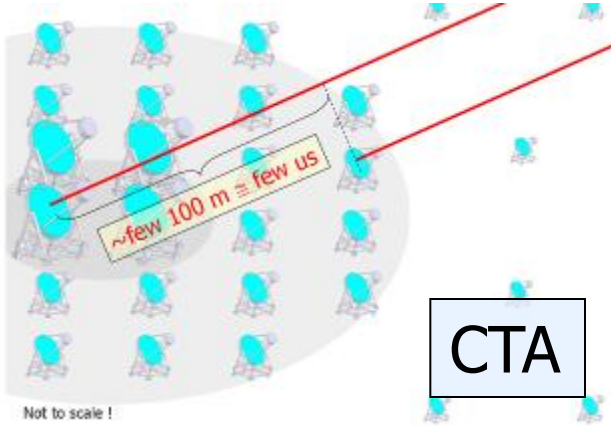


Plans for DRS5

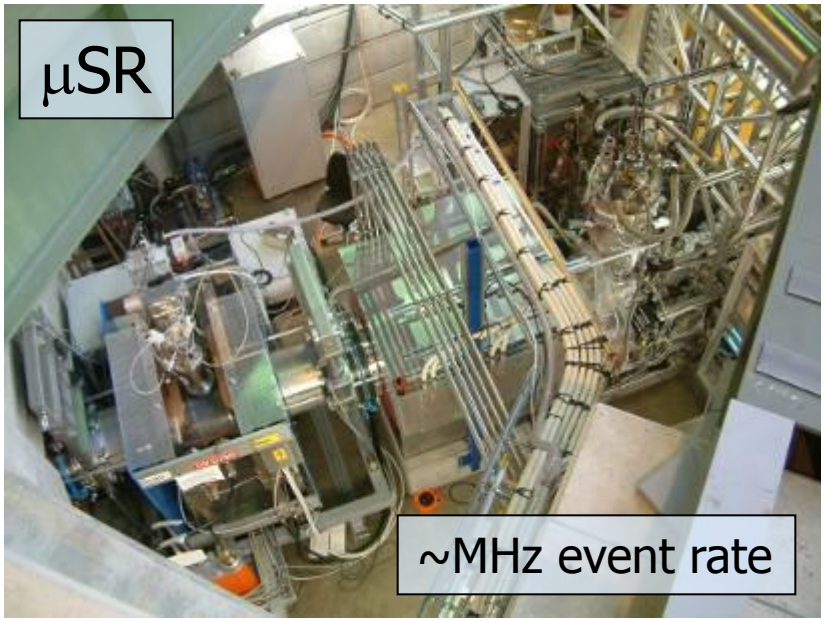
- Increase analog bandwidth ~5 GHz
  - Smaller input capacitance
- Increase sampling speed ~10 GS/s
  - Switch to 110 nm technology
- Deeper sampling depth
  - 8 x 4096 / chip
- Minimize readout time ("dead time free") for muSR & ToF-PET
  - (minor) reduction in analog → 20 ns)
  - ology



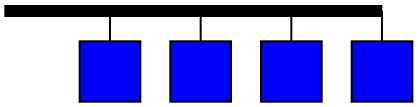
J. Milnes, J. Howoth, Photek



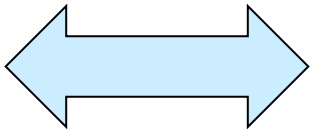
CTA

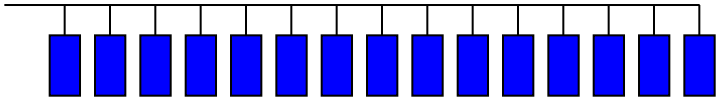


Next Generation SCA



Short sampling depth





Deep sampling depth

- Low parasitic inp… capacitance
  → High bandwid…
- Large area
  → low resistance bus, low resistance analog switches
  → high bandwidth

How to combine best of both worlds?

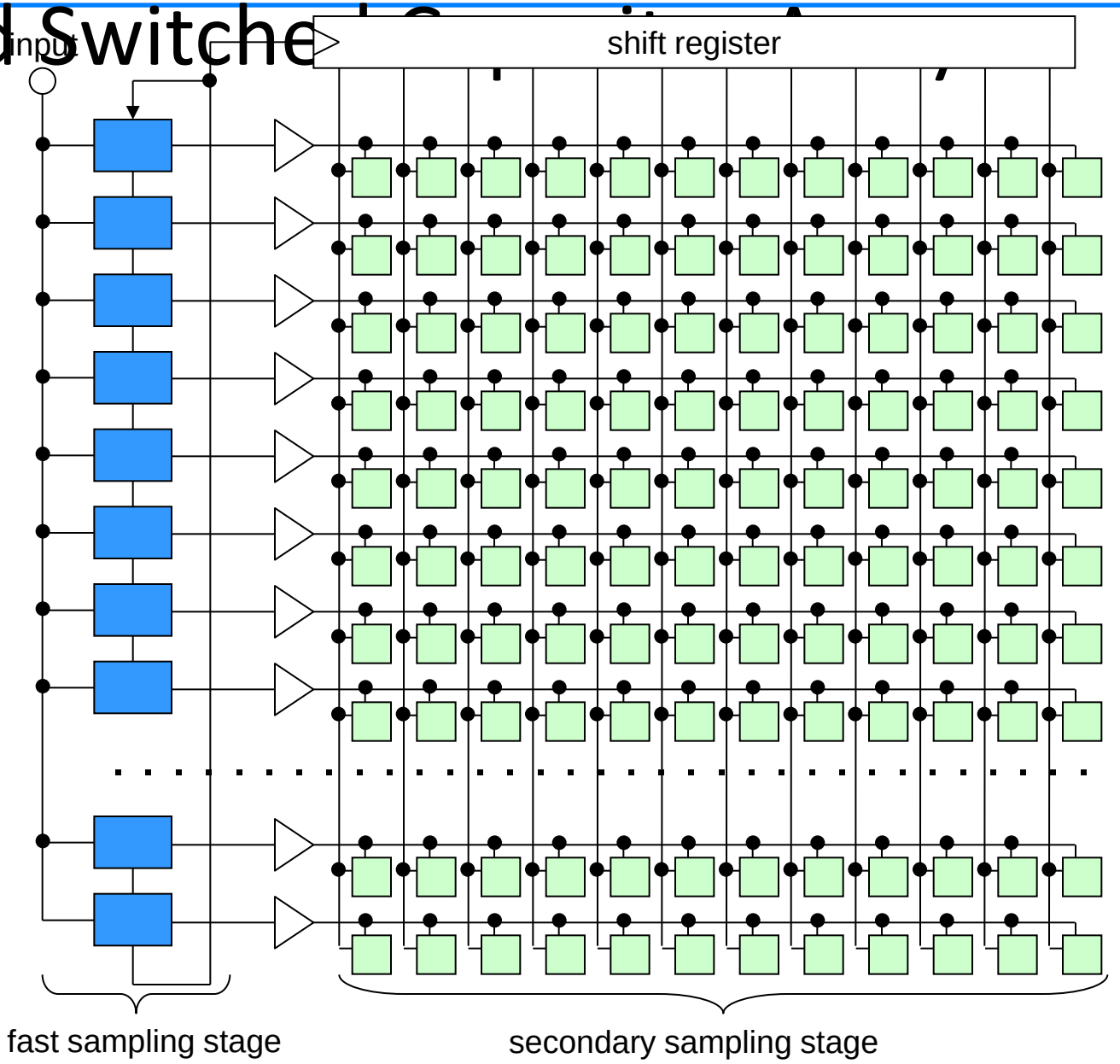
…long waveforms

…nodate long trigger delay

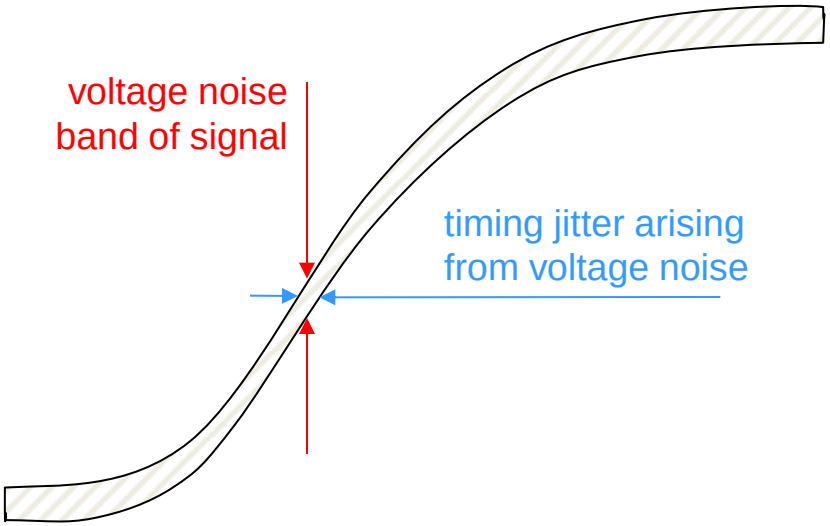
- Faster sampling speed for a given trigger latency

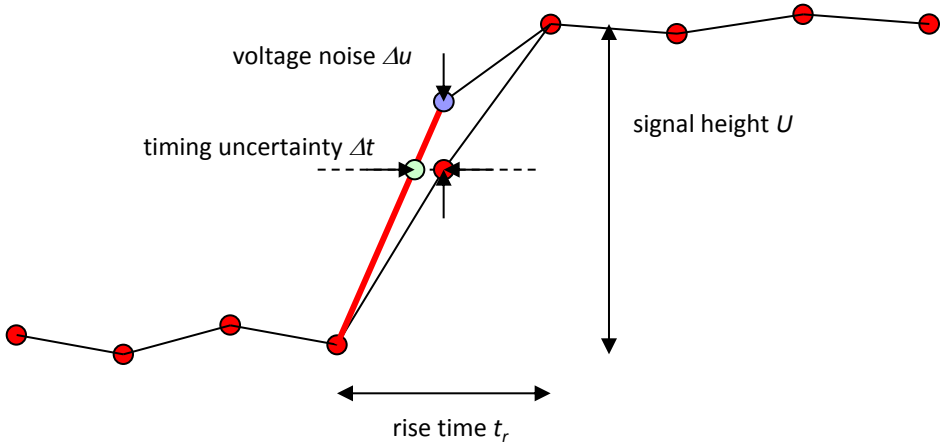
Cascaded Switched Capacitor Array

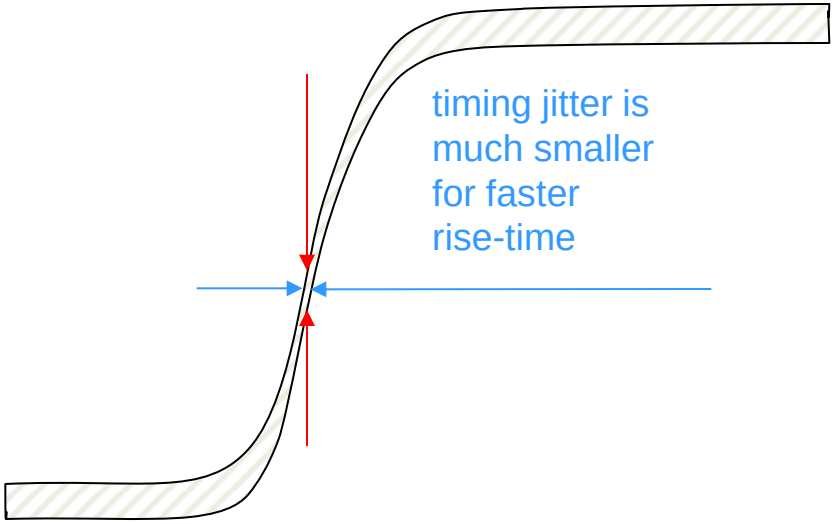
- 32 fast sampling cells (10 GSPS/110nm CMOS)
- 100 ps sample time, 3.1 ns hold time
- Hold time long enough to transfer voltage to secondary sampling stage with moderately fast buffer (300 MHz)
- Shift register gets clocked by inverter chain from fast sampling stage



How noise affects timing





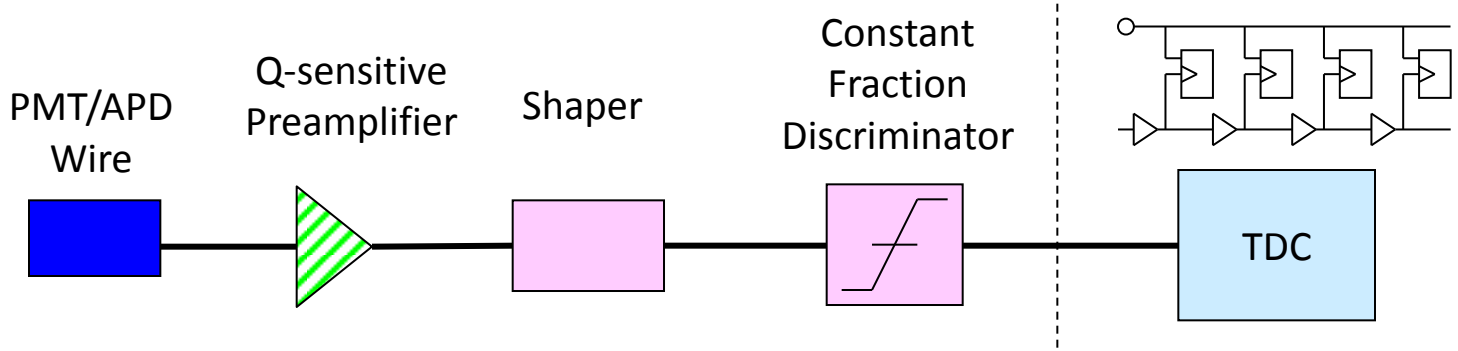


$$\Delta t = \frac{\Delta u}{U}\cdot t_r = \frac{\Delta u}{U\sqrt{n}}\cdot t_r = \frac{\Delta u}{U}\cdot\frac{t_r}{\sqrt{t_r\cdot f_s}} = \frac{\Delta u}{U}\cdot\frac{\sqrt{t_r}}{\sqrt{f_s}}$$

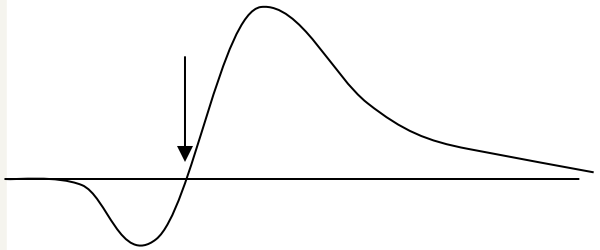
$\frac{1}{SNR}$

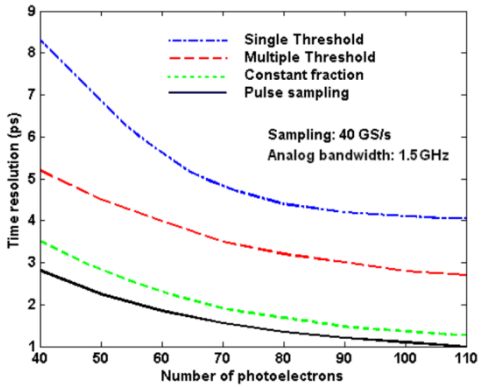
number of samples on slope

TDC vs. Waveform Digitizing

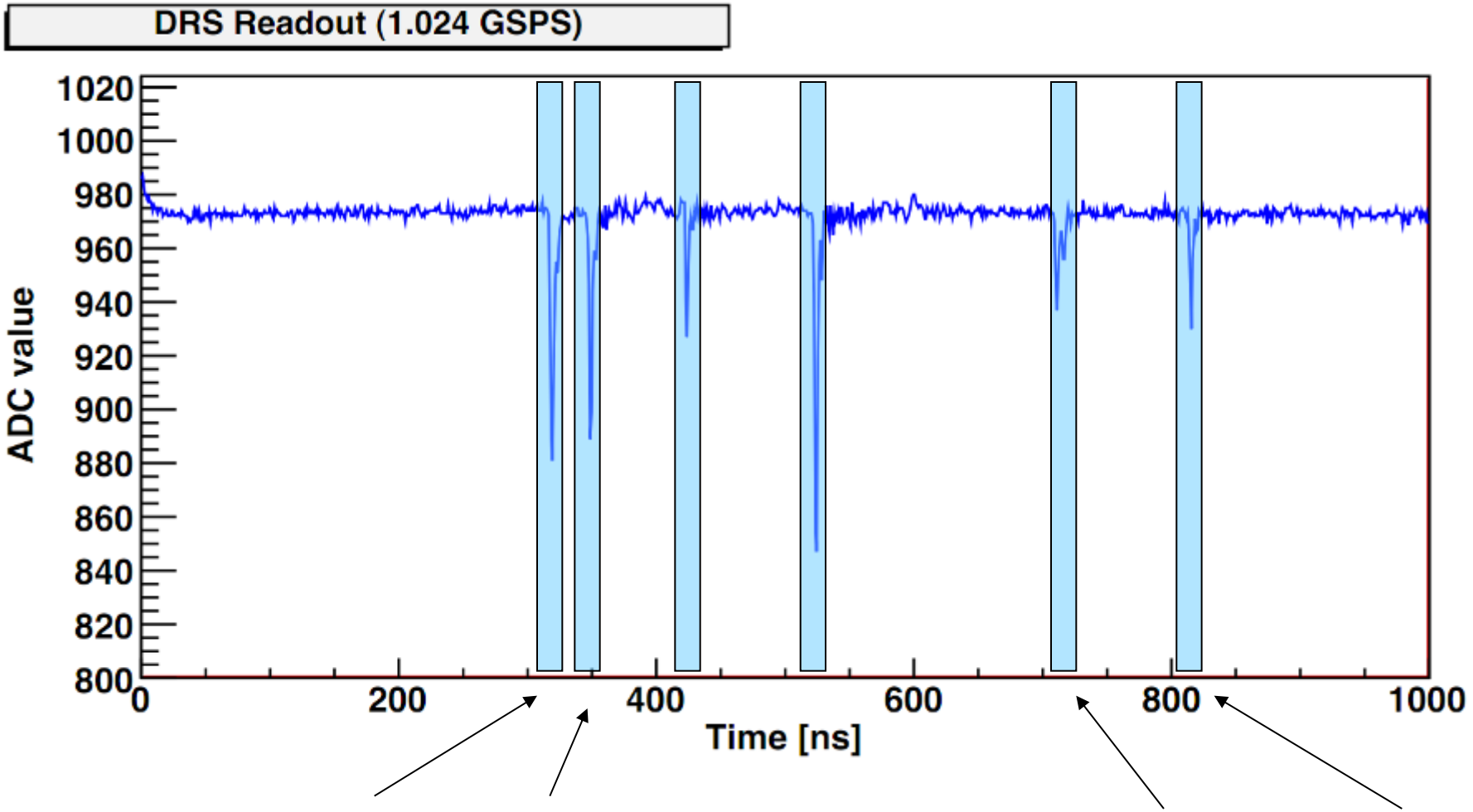


- CFD and TDC on same board → crosstalk
- CFD depends on noise on single point, while waveform digitizing can average over several points
- Inverter chain is same both in TDCs and SCAs
- Can we replace TDCs by SCAs?
  → yes if the readout rate is sufficient





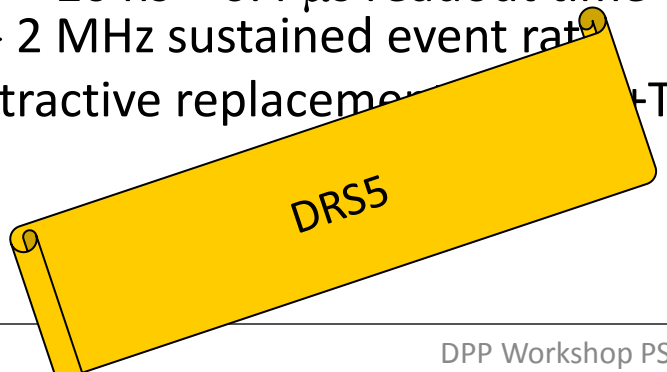
Typical Waveform

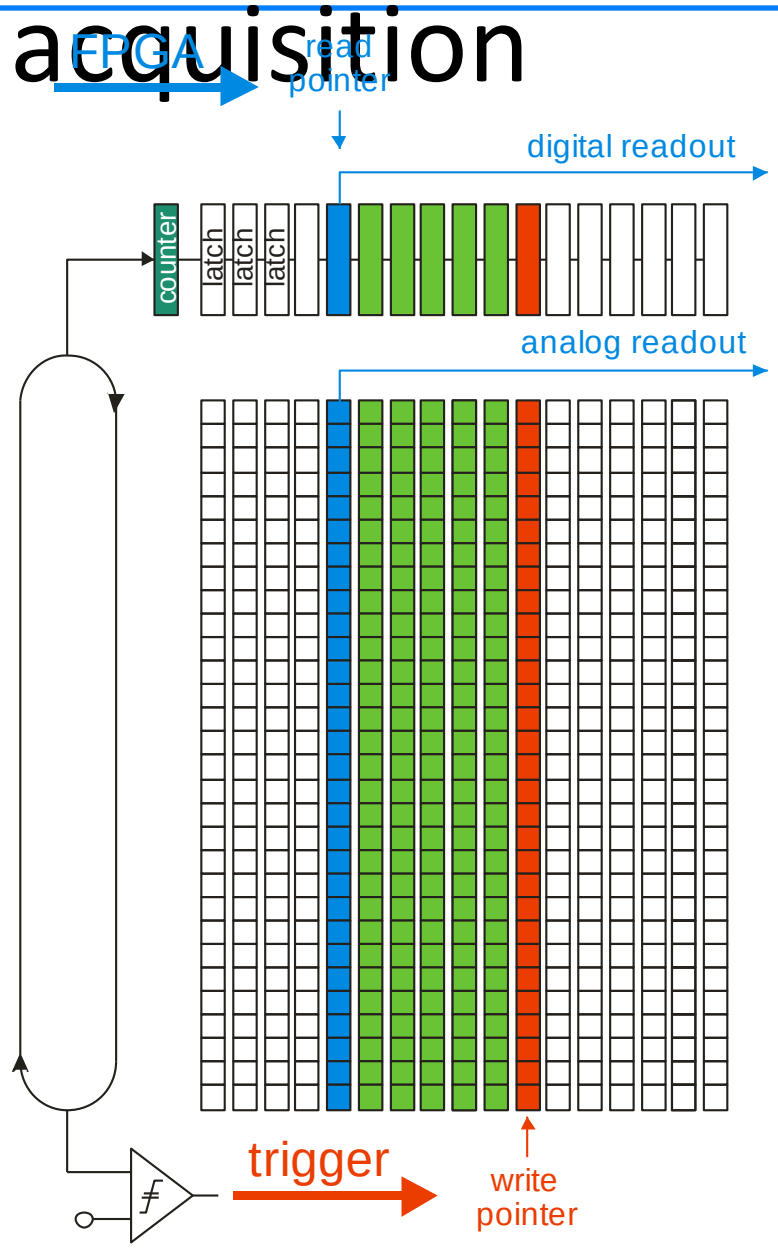


Only short segments of waveform need high speed readout

Dead-time free acquisition

- Self-trigger writing of short 32-bin segments
- Simultaneous reading of segments
- Quasi dead time-free
- Data driven readout
  - Ext. ADC runs continuously
  - ASIC tells FPGA when there is new data
- Coarse timing from 300 MHz counter
- Fine timing by waveform digitizing and analysis in FPGA
- 20 * 20 ns = 0.4 µs readout time
  → 2 MHz sustained event rat
- Attractive replacem -TDC





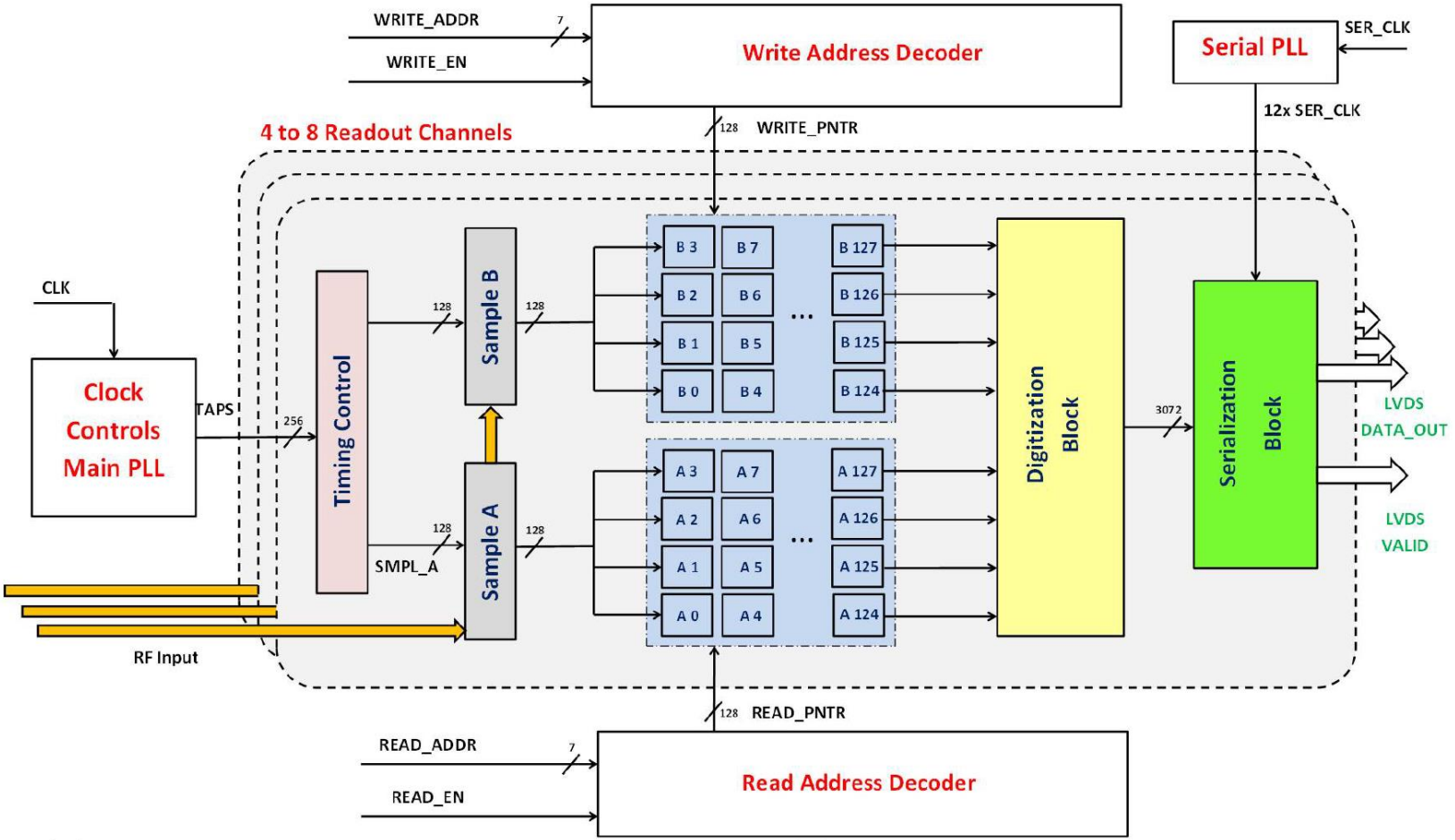
PSEC

PSEC4 compared to **deeper buffer samplers**

Parameter	PSEC4	PSEC5
Channels	6	4
Sampling Rate	4-15 GSa/s	5-15 GSa/s
Primary Samples/channel	256	256
Total Samples/channel	256	32768
Recording Buffer Time at 10 GSa/s	25.6 ns	3.3 μs
Analog Bandwidth	1.5 GHz	1.5 - 2 GHz
RMS Voltage Noise	700 μV	<1 mV
DC RMS Dynamic Range	10.5 bits	10 - 11 bits
Signal Voltage Range	1 V	1 V
ADC on-chip	yes	yes
ADC Clock Speed	1.4 GHz	1.5 - 2 GHz
Readout Protocol	12-bit parallel	serial LVDS: one per channel
Readout Clock Rate	40 MHz	500 MHz
Average Power Consumption	100 mW	300-500 mW
Core Voltage	1.2 V	1.2 V

Deeper buffer (PSEC5 and related Hawai'i ASICs)

- Potential for 'dead time-less' operation depending on chip sampling rate, readout rate, and experiment trigger rate



http://annie.uchicago.edu/lib/exe/fetch.php?media=2014_3_1_annie_electronics.pdf Eric Oberla

Concern for TOF

- Effect of background on TOF
  - Pile-up
- If need to record waveform :
  - Deadtime (sampling chip have deadtime, wait for new generation chip DRS5 prototype 2018)
  - Event size
    - Occupancy
    - Data reduction
- Cost (develop new electronics)

Options for chinese R&D

- First option
  - Development A/D ASIC
  - Development of TDC
  - Possibility A/D/TDC chip
- Digitizing
  - Develop ASIC
  - Reuse ASIC and develop readout

Amplifier

- Need cheap fast amplifier to use with readout
- High bandwidth
- Multichannel

Conclusion

- Electronics is not a limiting factor for timing resolution (up to 1 ps)
- Baseline : A/D and VETROC for trigger and readout 20 ps resolution
- Additionnal development for better than 20 ps
- Need simulation to determine the need of sampling electronics
- Sampling electronics is better in term of timing and background but need to evaluate additional cost and data size
- Would work for MRPC or LAPPD