SoLID pre-R&D
Second Quarterly Progress Report

August 2020 to November 2020

SoLID Collaboration

December 6, 2020

Contents

1 DAQ

1.1 Summary

This chapter summarizes the SoLID DAQ pre-R&D activities for the third quarter, from August, 2020 to November, 2020.

The five main on-going tasks (A-E) for this pre-R&D are:

- A) GEM VMM3 readout high rate testing to determine trigger rate capability, behavior with pile-up and readout performance
- B) GEM APV25 readout high rate testing: show that 100 kHz trigger rate is achievable with existing readout hardware developed for SuperBigBite (SBS)
- C) FADC developments for fast readout and triggering
- D) Beam test of gas Cherenkov readout with analog sums and MAROC chip
- E) Time of flight using the NALU sampling chip

Milestone A2, due November 1, 2020, is delayed until after A3 in order to have more channels with new prototype electronics available. The estimated completion date is May 15, 2021.

Milestone B2 is still on-going due to new firmware development requirements. The estimated completion is February 2021.

1.2 Milestones

1.2.1 GEM testing milestones

A) VMM3 We are studying the behavior of the VMM3 in high background and are determining the maximum trigger rate that can be achieved.

Milestone	Objectives	Expected Completion Date	Status	Updated Date
A1	Finish development of VMM3 direct readout	April 1, 2020	Complete	
A2	High rate testing with detector	November 1, 2020	Started	May 15, 2021
A3	Optimized VMM3 setup for maximum data rate	March 1, 2021	Started	

A1: Complete: The evaluation board has 12 direct outputs that can be used for initial testing.

A2: VMM3 evaluation board system (Figure 1) – The GPVMM evaluation board makes 12 direct readout outputs available on a connector. This connector is cabled to a Xilinx FPGA development board through a mezzanine card for readout of the direct outputs. No hardware design is required for this system. Readout of the FPGA board is via a 1-GbE optical path, so high-rate operation is possible. All hardware, adapters, and cables are in place. Direct output data from the VMM has been detected in the FPGA of the development board. Firmware for decoding the VMM direct output data and formatting it for readout has been completed and simulated. The integration of this VHDL code with existing 1 GbE VHDL readout code is underway. Firmware designed for this system is being scaled up for use in the Prototype VMM front-end board (1).

A3: Prototype front-end board (Figure 2) – The module supports 128 VMM3 channels and mounts on a GEM detector with a high-pin count connector. It is designed with dual readout paths. The 10 GbE optical readout path allows for easy connection to a PC or network switch and is suitable for lab test stands or low radiation environments. The GBT optical readout link uses rad hard components designed for CERN LHC experiments and will be used for the SoLID experiment data readout. The module has a hit rate capability of several MHz per channel at a 200 KHz trigger rate. The conceptual design was finalized and components were chosen. A scheme for powering the module under radiation and non-radiation conditions was developed. The printed circuit board design (layout, signal routing) is approximately 75% complete. A contract to hire VMM chip designer Gianluigi De Geronimo as a consultant has been finalized. He is currently assisting us with the circuit board layout details and power delivery for the sensitive VMM chips. Firmware already developed for the VMM evaluation board system (2) is being scaled up for the 128 channels of the prototype. This firmware will initially support 10-GbE readout.

B) APV25 To test the feasibility of reusing electronics from SBS to reduce electronics costs, we will determine if the existing APV25 based electronics can reach a trigger rate of at least 100 kHz.

- Milestone B1, June 1, 2020: While the intrinsic specs of the chip should allow a 200 kHz trigger rate using one sample, some development is needed to determine if this is achievable with the existing SBS electronics. The task involves enabling the APV25 buffering and optimizing the data transfer of the readout.

- Milestone B2, October 1, 2020: Determine rate limits of the APV25 trigger and test in a high occupancy environment.

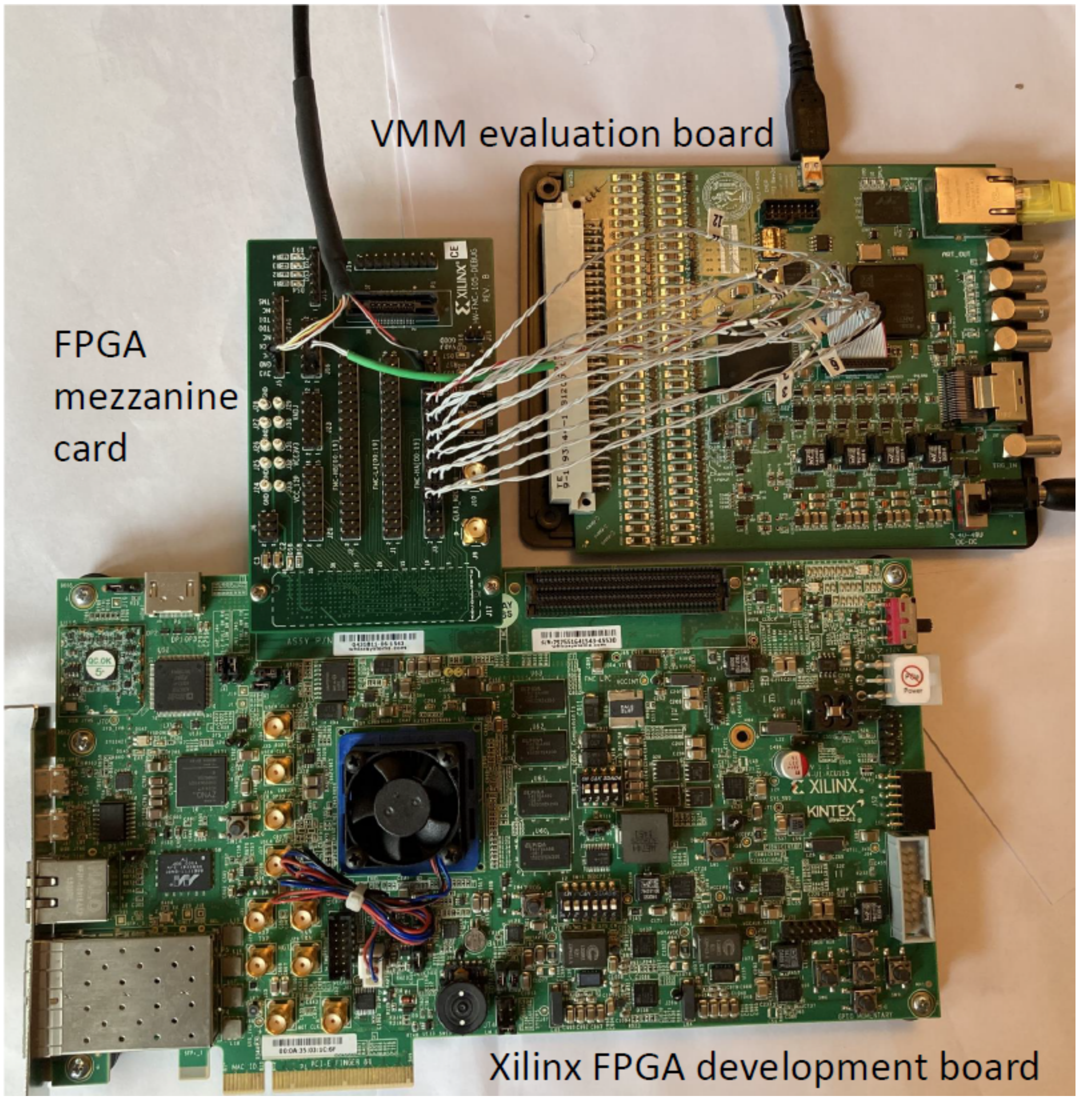


Figure 1: System for reading direct outputs from VMM evaluation board

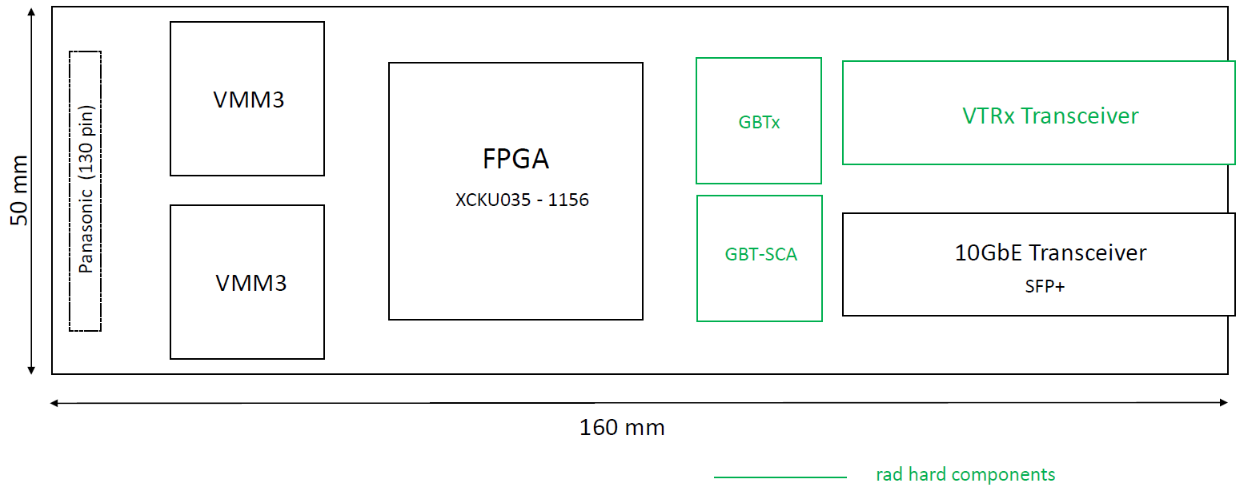


Figure 2: Prototype VMM front-end board

Milestone	Objectives	Expected Completion Date	Status	Updated date
B1	Finish development of fast APV25 readout	June 1, 2020	Complete	
B2	Determine maximum rate achievable with APV25	October 1, 2020	On-going	February 2021

B1: Complete in second quarter

B2: Some firmware development is required to double the possible amount of data to be transferred by packing two samples in a 32-bit word. Fast readout Optical-to-VXS transceivers were ordered to eliminate the VME bus bottleneck. Estimated delivery is December 15, 2020. Some firmware development will also be needed to use this new hardware.

1.2.2 DAQ test stand and rate tests

C) DAQ

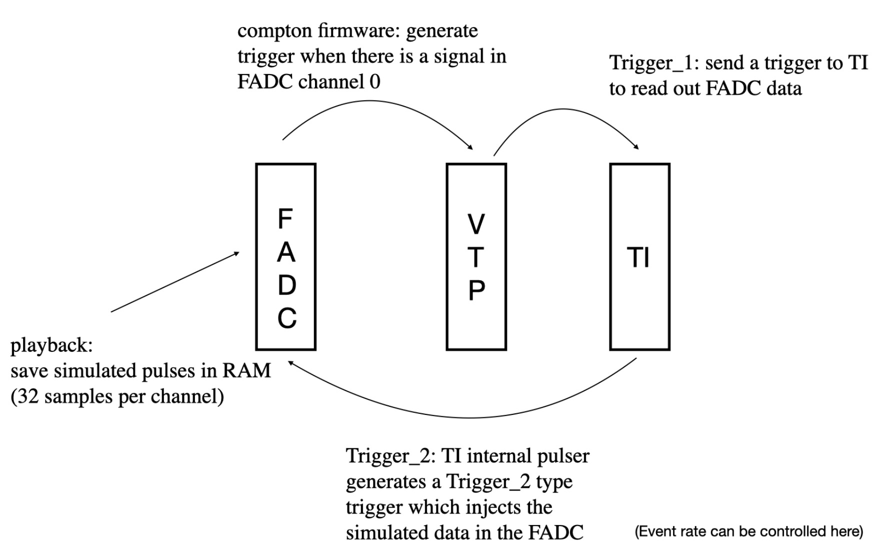
Milestone	Objectives	Expected Completion Date	Status	Updated completion date
C1	Development FADC readout through VXS	April 1, 2020	On-going	January 31, 2021
C2	Testing PVDIS trigger functionalities and rate capability	October 1, 2020	On-going	March 1, 2021
C3	PVDIS trigger test with two sectors	February 1, 2021	Not started	May 1, 2021
C4	Test SIDIS trigger	March 15, 2021	Not Started	July 15, 2021

C1: On-going.

Design and simulation of the firmware on the FADC and VTP side are being developed and at simulation stage. Implementation and testing will be done at beginning of 2020

C2: On-going.

The DAQ test stand at UMass currently has one VXS crate with one FADC, one VTP and a TI board installed. The first step of the test stand is to measure the FADC dead time under high trigger rates. We use the FADC "playback" feature to simulate the input pulses. In "playback", the simulated input pulses for FADC are saved in the RAM. When FADC receives a Trigger_2 type trigger from the TI internal pulser, it loads the simulated pulses and injects them into the processing pipeline. The VTP then collects these signals from FADC to generate a trigger and sends it to the TI so that CODA can read out the data.



Since August, we have installed the VME OS and the VTP OS required for the ROCs in the test stand and have installed CODA. This is the first time CODA3 has been installed on a smaller scale computer, so it took some time for the expert to optimize the installation package. FADC has been successfully read out by CODA and the data is decoded by a decoder inherited from the Compton electron detector DAQ. The playback feature of the FADC works. By changing the TI internal pulser rate, we could generate a trigger rate from 2 kHz to 250 kHz. The next step will be to integrate the helicity board. The VTP needs the MPS signals from the helicity board to enable the scaler counting. The helicity board has been used in the PREX/CREX experiments. Integrating it into this setup should take no more than a week. Once the VTP scaler is enabled, deadtime measurements can be performed.

C3/C4: Not started.

D) Cherenkov readout

Milestone	Objectives	Expected Completion Date	Status	Updated Completion Date
D1	Setup FADC crate for Cherenkov simple sum testing	February 15, 2020	Complete	
D2	Record beam data using simple sum and FADC	April 15, 2020	Complete	
D3	Record data using MAROC sum readout	Oct 15, 2020	On-going	Feb 15, 2021

D1: Completed in first quarter.

D2: Completed in second quarter.

D3: The MAROC sum electronics were delivered from INFN and ready for beam test. Due to lack of available beam time, the beam test of the MAROC sum electronics was cancelled. We are continuing bench testing using LED's, a laser, and cosmic rays. The details are in Cherenkov section 2.5.

E) Time of flight The current baseline readout of the TOF is based on the FADC250 with at 250 MHz sampling rate with a target goal of 100 ps timing resolution. The ASOC chip has a sampling rate from 2.4 to 3.2 GHz. We are evaluating the benefit of higher sampling rate on timing resolution in a high background environment.

Milestone	Objectives	Expected Completion Date	Status	Updated Date
E1	Acquire and setup ASOC evaluation board	February 1, 2020	Complete	
E2	Acquire data of scintillator	May 15, 2020	Delayed	December 15, 2020
E3	Complete analysis and determine achieved timing resolution with ASOC and compare to FADC resolution	February 15, 2021	Delayed	May 15, 2021

E1: Completed in first quarter.

E2: Delayed due to faulty board.

E3: while the ASOC sampling board and software were installed upon receipt, testing of board with an input signal was delayed due to COVID. Once testing started with a pulse generator, it was not possible to readout data due to a problem with the board hardware. A replacement board was delivered at beginning of November. Signals could be acquired with both a continuous trigger and self trigger mode. Testing with a detector will proceed in December to evaluate timing resolution with large backgrounds in the detector.

1.3 Budget / spending summary / procurement

Main new expenses were for the VMM3 prototype boards : 8.7 K$ for the VMM chips and hardware for testing the evaluation boards. The VXS crates, VTP and CPUs were received.

Contracts for UVA and Gianluigi De Geronimo are in place in addition to the UMass one.

System	Cost ($)	Number	Total	Spent
VXS crate for DAQ modules	15,000	2	30,000	32,388
VTP - Module for triggering and data movement	10,000	2	20,000	17,050
SSP	6,500	1	6,500	0
TI - Trigger Interface	3,000	2	6,000	0
SD - Signal Distribution card	2,500	2	5,000	1,250
FADC trigger distribution card	2,000	2	4,000	4000
VME CPU	4,500	2	9,000	11,000
Trigger Supervisor	3,500	1	3,500	0
Hardware components for VMM readout test stand	25,000	1	25,000	6,775
APV25 GEM system	23,000	1	23,000	8,480
Cables/patch	400	160	64,000	8,000
Optical fibers	100	20	2,000	2,000
MAROC eval board	23,000	1	23,000	0
ASOC eval board	10,000	1	10,000	8000
Optical transceivers	50	32	1600	1600
Total M/S direct			210,600	102,487
Total request M/S			227,300	110,575
Workforce 2020	$130,000$	1.25	162,500	90,000
Workforce 2021	$133,900	1	133,900	203,518
Contract DG electronics	78,250	1	78,250	78,250

Table 1: Budget summary

	Budget ($)	Obligated ($)
Material	227,300	110,575
Personel	372,700	371,768
Total	600,000	474,255

Table 2: Budgeted and obligated funds summary (includes overhead)

2 High Rate Test of MaPMT Array and LAPPD Using a Telescopic Cherenkov Device

2.1 Summary

The beam test of the pre-R&D was completed in Hall-C. High and low rate testing for the simple MaPMT summing electronics was completed before the end of Q2. Additionally, low rate testing for the LAPPD electronics with CO_2 and C_4F_8 gas was completed. Analysis and comparison to simulation are ongoing, and updates are presented in this report. The testing of MAROC electronics performance could not be scheduled within the truncated parasitic time-window and now moves to bench testing to complete the remaining milestones and goals. Additional bench tests are planned or underway for the simple summing, LAPPD, and MAROC electronics configurations.

2.2 Project Milestones

Milestone	Objectives	Expected Completion Date	Status
1	Construction and delivery of Cherenkov tank to Jefferson Lab.	Early January 2020	Complete (Q1)
2	Cosmic testing and installation into experimental hall.	Mid February 2020	Complete (Q1)
3	Collection and analysis of low and high rate data with electronic summing-board.	End of Year 2020 (+2 Month Contingency)	Collection complete (Q2), Analysis ongoing
4	Collection and analysis of high rate data with MAROC electronics.	End of Year 2020 (+4 Month Contingency)	Moved to Bench

2.3 Budget / spending summary / procurement

To date funds have been used to purchase all the materials to construct the Cherenkov prototype tank with pressure controls, all connectors and cables for reading out signals of 64 channels from MaPMTs or LAPPD, mirror, 16 MaPMTs, wavelength shifter coating, radiator gas, MAROC readout boards and their cabling. Funds have been used for the mechanical engineering design and machining as well as electrical engineering support, travel

	Budget ($)	Q1 Expenses($)	Q2 Expenses ($)	Q3 Expenses ($)
Material	210.0	124,736	84,414	3,311
Personnel	240.0	31,376	27,411	26,882
Travel	0	0	0	5295
Total	450,000	156,112	111,825	35,488

Table 3: Budgeted and expenditures summary from both Temple and Duke for the Cherenkov prototype (includes overhead)

and transport of the prototype from Temple to Jefferson Lab, and the research personnel support for the approved activities at Duke and Temple.

2.4 Analysis and Simulation

Recent analysis activities are focused on the quadrant signals from the MaPMT array (both high rate and low rate tests) and the pixel signals from LAPPD (low rate test). Simulations have also been carried out with the MaPMTs data as the benchmark.

2.4.1 MaPMT Array Analysis and Simulation

Significant progress has been made in analyzing the MaPMTs quadrant signals, providing more granular geometrical information about photo-detection. The analysis software has also been improved in several aspects, featuring a better determination of the pedestal for the waveform signals and the capability of integrating signals over the entire peak range. In this section, we present the analysis results focused on the MaPMTs quadrant signals, as well as the comparison between the high rate and low rate tests.

As in the previous analyses reported in the quarterly reports, the MaPMTs sum channels' signals were selected by a timing cut with a window of 20 ns on the relative timing between the signal channel and the triggered calorimeter channel. The quadrant signals were then selected by a 8 ns timing cut on the timing with respect to its sum channel. Figure 3 illustrates such an event selection process for the quadrant signals. In addition to the timing cut, a geometrical cut is also performed to select only the events that triggered the central calorimeter module out of the 3×3 array. This geometrical cut helps select the events whose Cherenkov photon rings are mostly detected within the prototype's acceptance.

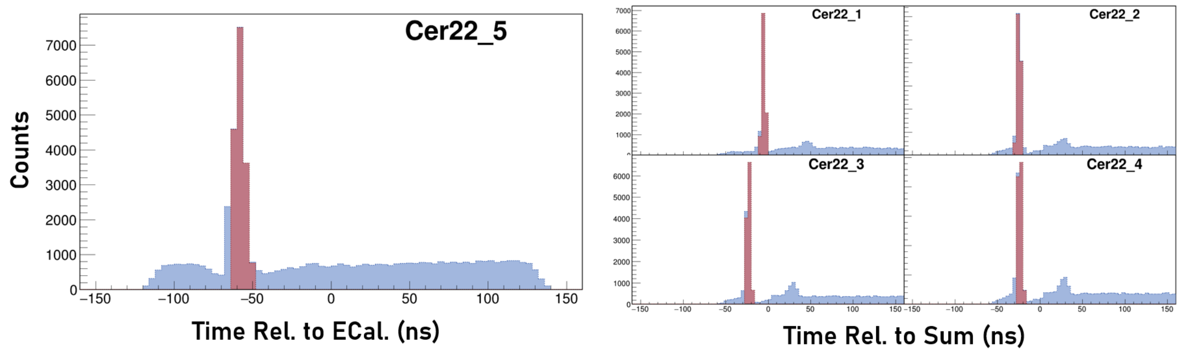


Figure 3: Relative timing distributions for a sum channel and its corresponding quadrant channels. The left panel shows the relative timing between one sum channel and the trigger channel (ECal.); the right panel shows the timing of quadrant channels with respect to their sum signal. Red histograms represent the distributions after timing cuts, and blue histograms are the raw distributions.

The quadrant signals were then normalized to their single photo-electron amplitude, and summed together. Figure 4 shows the two-dimensional distribution of the number of photo-electrons (NPE) versus the number of fired quadrant channels (N_{quads}). The results from both the high rate test (scaler rates 4.8 MHz/PMT) and the low rate test (320 kHz/PMT) are presented in the plot. An almost identical behavior of the MaPMT photo-sensors can be observed from the comparison, demonstrating that such a device can work well in a high rate environment.

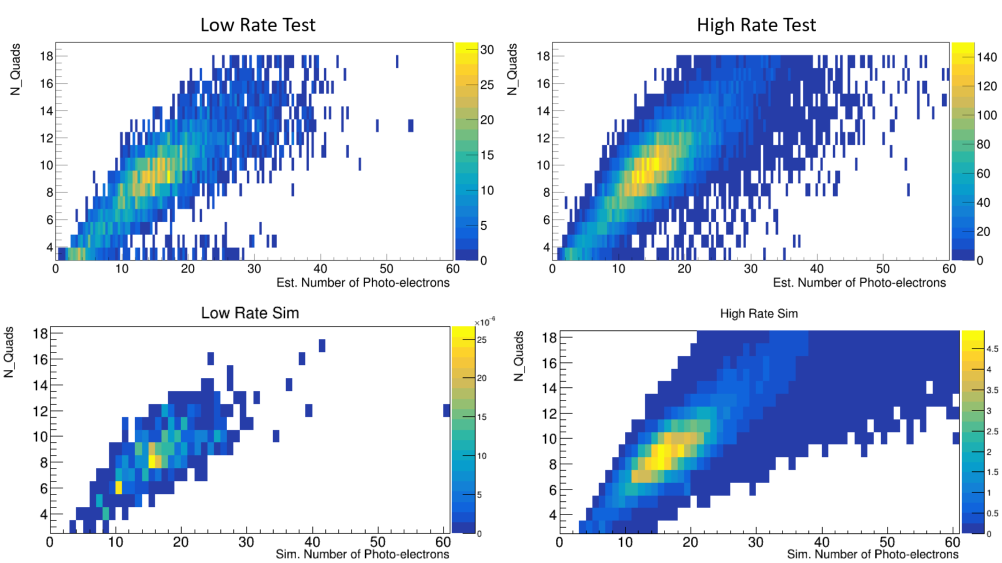


Figure 4: Two-dimensional distribution of NPE vs. N_{quads} for MaPMTs in the low rate and high rate environments. The top row is from beam test and the bottom row is from simulation.

It can be observed from Figure 4 that the Cherenkov signal centers at $N_{quads} = 9, 10$ with an approximate NPE = 17. Figure 5 shows the signal sums subgroups with different N_{quads}. The signals can be categorized into three groups: i) the random coincidence of single photo-electron signals with $N_{quads} = 1, 2, 3$, demonstrating a significant suppression when requiring multiple quadrant channels to be fired within the same time window. ii) Cherenkov signals with $N_{quads} = 9, 10$. The signals follow a Gaussian distribution centered around NPE = 17, corresponding to the heat center in the 2D distribution (see Figure 4). iii) Gaussian-like signals with $N_{quads} = 19, 20, 21$ and NPE ≥ 30, approximately double the NPE of typical Cherenkov events. These high-NPE signals are possibly the coincidence sums of both detected electron and positron from the pair production process.

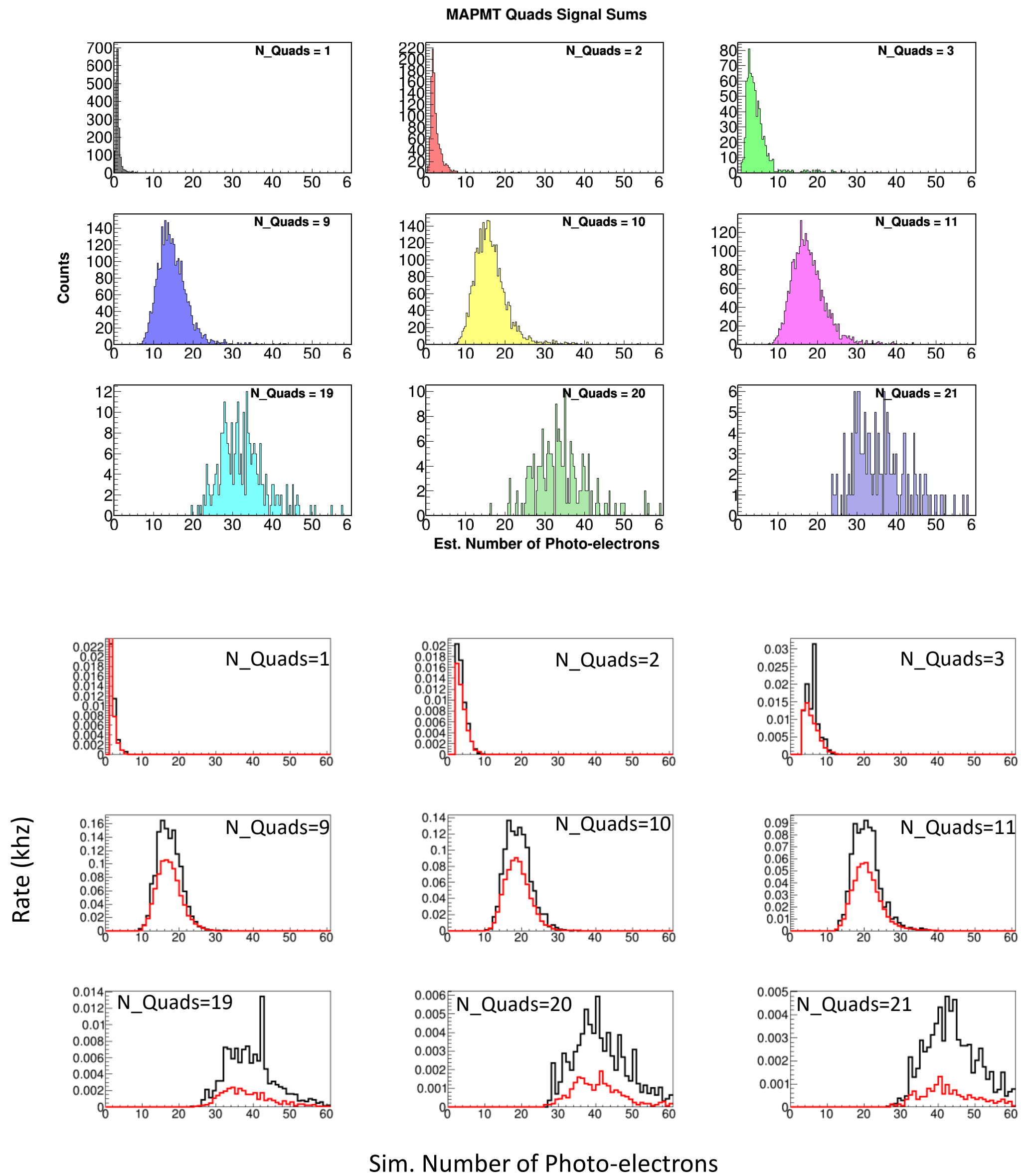


Figure 5: Distributions of NPE for a specified number of fired quadrant channels. The top panel is from the high rate beam test. The bottom panel is from the high rate simulation where the black and red lines represent high energy electrons and neutral pions from the target respectively.

2.4.2 LAPPD Analysis

The beam test data with LAPPD as the photo-sensor at the low rate environment have also been analyzed. As an alternative solution, the LAPPD provides highly granular geometrical information with the pixelized readouts. It is expected to have a picosecond-level timing resolution with a high tolerance (~ 1.5 T) for external magnetic fields, but a slightly lower quantum efficiency. In this test, the pixel size was designed to be the same size as the

MaPMTs quadrant, so these two devices' results can be directly compared.

Figure 6 shows a comparison of raw waveform signals from the MaPMTs and the LAPPD. It is obvious that the width of the LAPPD signals is much narrower than that of the MaPMTs, which results in a better timing resolution, and would benefit the signal separation in an extremely high-rate environment. The current test shows a lower signal amplitude from the LAPPD data. This issue will be studied in the ongoing bench test of the LAPPD.

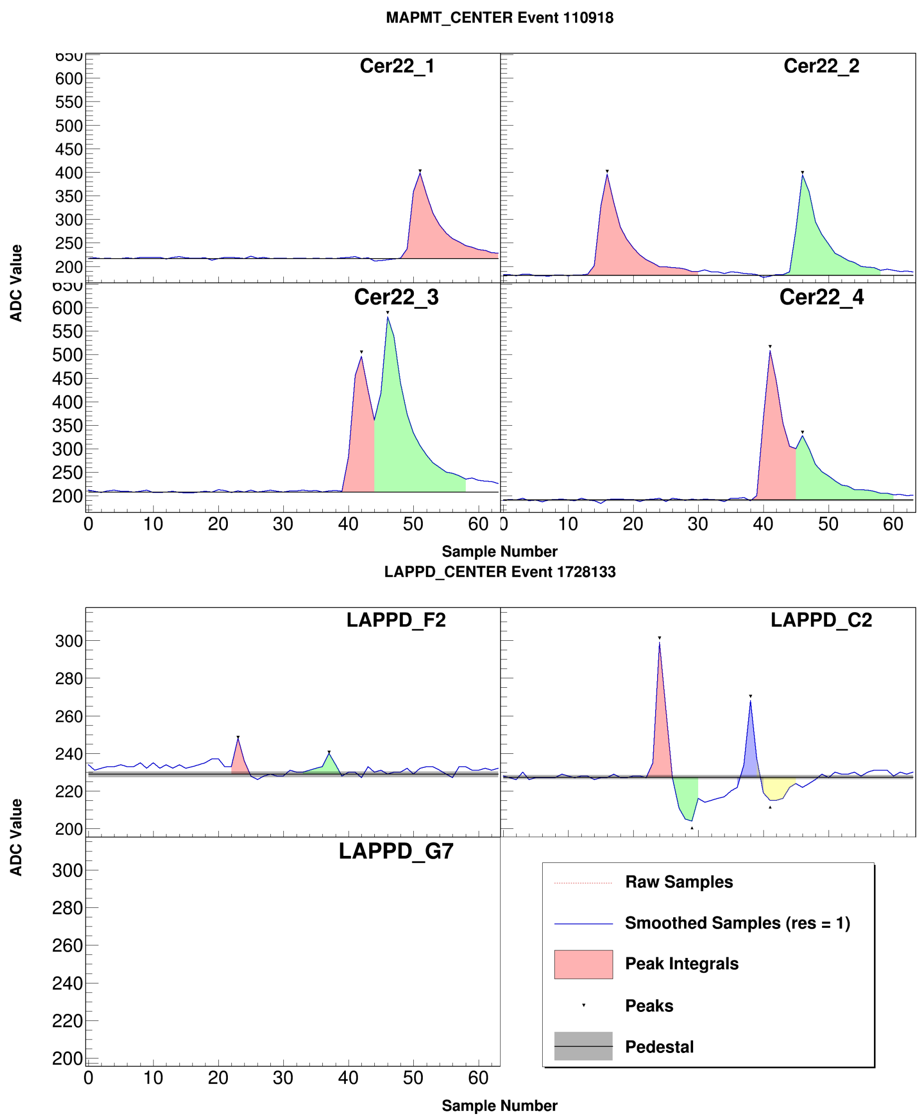


Figure 6: An event sample of raw waveform signals from central channels of MaPMT quadrants or LAPPD pixels. The top panel shows MAPMT signals; the bottom panel shows those of LAPPD. Some channels are empty because no signals pass the DAQ threshold in the specific event.

Figure 7 shows a comparison of the signal sum groups between the MaPMTs test and the LAPPD test, both performed in a low rate environment. Raw signal amplitude is used instead of NPE in the comparison, since the single photo-electron amplitude of the LAPPD will be extracted in the ongoing bench test. In general, the comparison shows a similar behavior from these two devices. The LAPPD data analysis is a work in progress, and the future results will include the data analysis of the ongoing LAPPD bench test data.

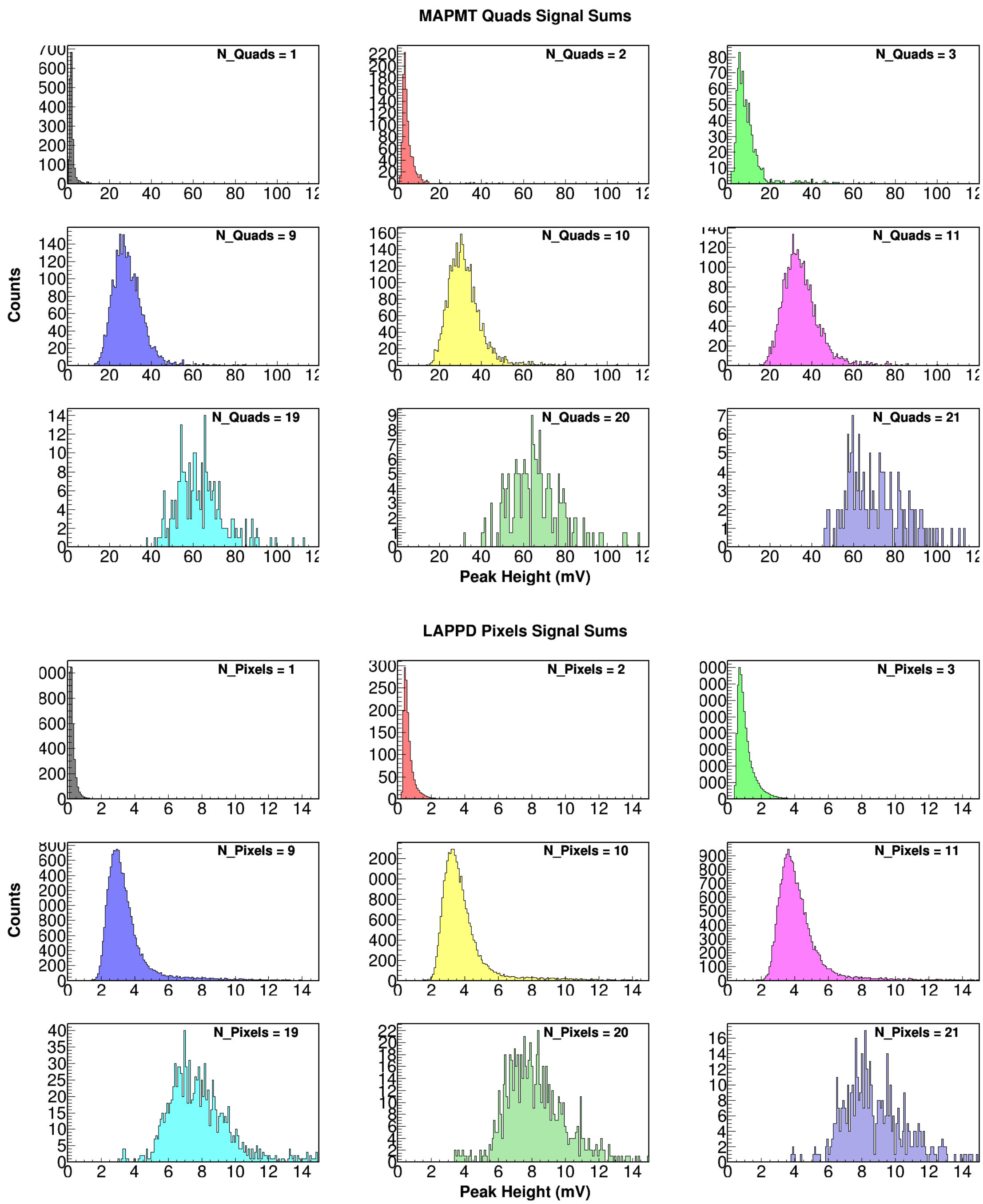


Figure 7: Comparison of signal sums between MaPMT and LAPPD data. The top panel shows MaPMT signal sum groups; the bottom panel shows LAPPD signal sum groups.

In addition, the LAPPD test includes different types of radiator gas: CO_2, a mixture of

80% C_4F_8 and 20% CO_2, and C_4F_8. The normalized distributions of the signal sum from these types of gases are shown in Figure 8. The heavy gas (C_4F_8) shows more signals with a large amplitude, indicating more photons detected, which is expected. A detailed analysis of the heavy gas run is still ongoing.

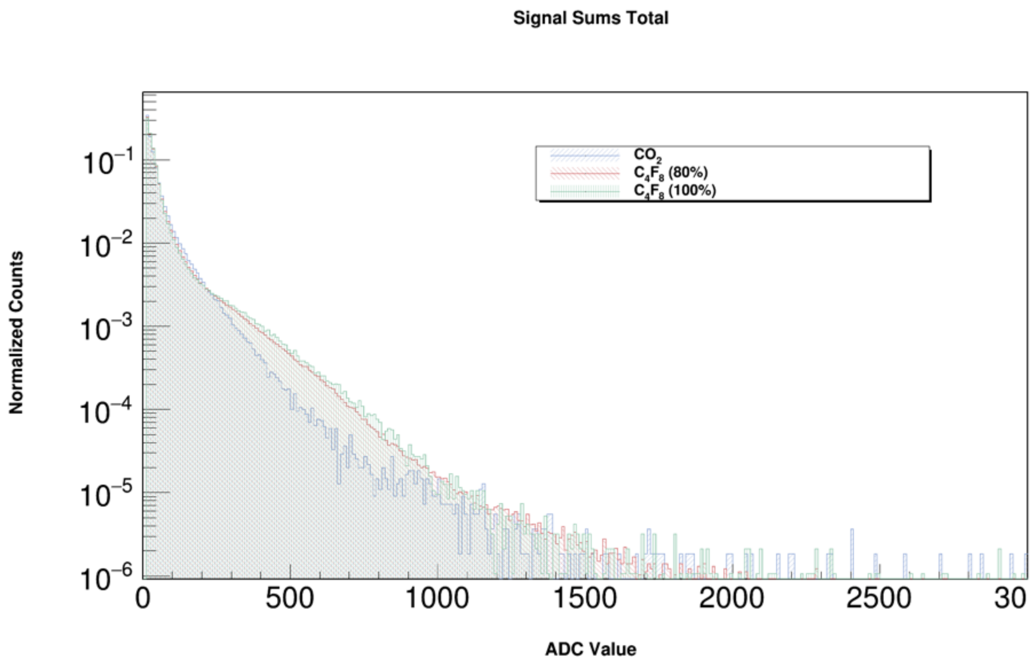


Figure 8: Signal sum distribution from LAPPD test with different gas radiators.

2.5 MaPMT with MAROC sum readout bench test

The CLAS12 RICH detector has used MAROC electronics with only pixel readout. It includes an adaptor board connecting to 3 MaPMTs, an ASIC board hosting MAROC chips, an FPGA board with optical fibers to communicate with SSP boards in DAQ to record TDC signals from 64 pixels each MaPMT. For SoLID Cherenkov detectors, to allow collecting pixel information and provide trigger with the sum of photons on pixels simultaneously, the new MAROC sum electronics was designed and manufactured in collaboration with the INFN Ferrara group and the JLab fast electronic group. By inserting a new sum board between a modified ASIC board and an FPGA board, charges in pixels are summed and separated into four quadrant sums and one total sum. A newly designed converter board then transfers the sum signals to communicate with JLab flash ADC boards in DAQ. The photos in Figure 9 shows five boards mentioned and how they work together to form the MAROC sum electronics.

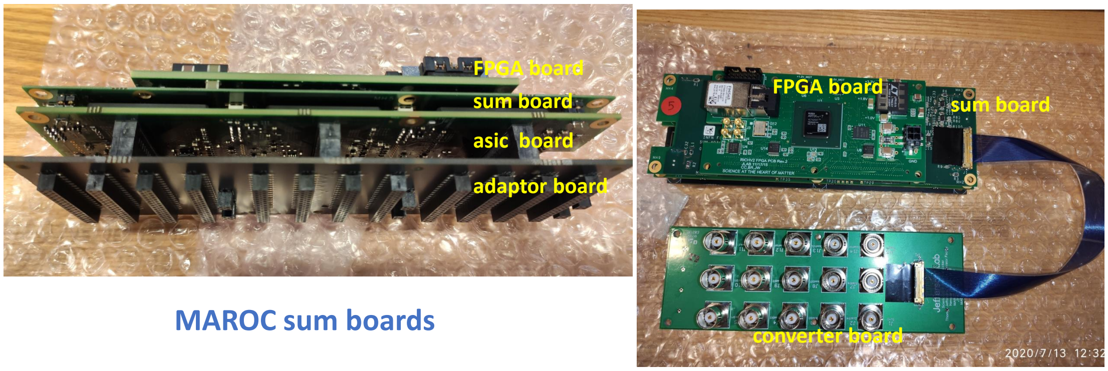


Figure 9: Photos of the MAROC sum boards, including adaptor, ASIC, sum, FPGA, and converter boards, are shown. The ASIC board is modified from its original version to accommodate the new sum board. A newly made converter board connects the new sum board output to regular BNC connectors through an I-PEX cable.

Due to the limited access and the lack of beam time, we could not carry out the beam test of the MaPMT with MAROC sum readout, although the electronics and the assembly were ready to go as reported in the last quarterly report. Since then, we have started a series of bench tests to mimic the SoLID running conditions.

It was observed that the MAROC pixel readout performed well at 2 kHz/pixel for most of the pixels and up to 16 kHz/pixel for some hot pixels during the CLAS12 data taking. For SoLID, we expect rates as high as 200 kHz/pixel for pixel readout and 4 Mhz/PMT for sum readout in the Heavy Gas Cherenkov detector. We are testing the electronics up to the expected SoLID rates using LEDs and a laser as light sources. With LEDs, the linear correlation between pixel signals readout by MAROC TDCs and sum signals readout by flash ADCs has been established, and the result is shown in Figure 10. This demonstrates that summing electronics work as expected to collect the charge from pixels. We are preparing to change to the laser setup used by the CLAS12 RICH group, which can operate stably for the high rates needed. We are also preparing a cosmic ray test using Lucite as a radiator to examine how the entire system behaves with real Cherenkov signals. Combining these tests, we can study how MaPMTs with MAROC sum readout would perform at rates similar to the expected rates under the SoLID data taking conditions.

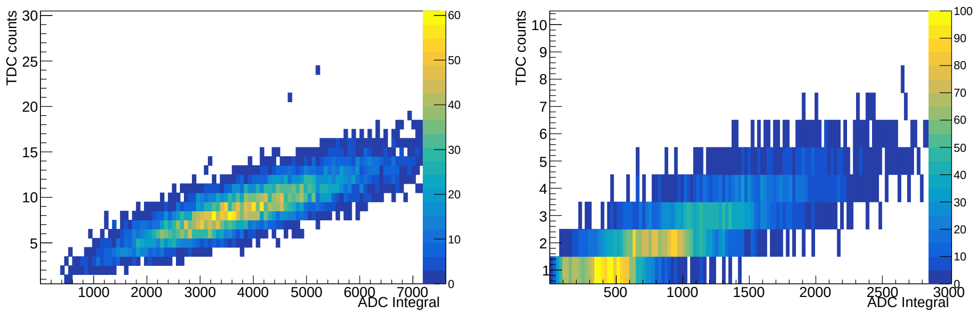


Figure 10: Left: TDC counts VS ADC total sum signal. Right: TDC counts vs ADC one quadrant sum signal. The linear correlation between pixel signals read-out by MAROC TDCs and sum signals read-out by flash ADCs is observed from the MaPMT with MAROC sum readout tested with LED.

The work is led by a postdoc of the Duke University group and we plan to finish the laser test and cosmic ray test by the next quarter.