SoLID pre-R&D
Quarterly Progress Report

April 2021 to July 2021

SoLID Collaboration

September 16, 2021

Contents

1 DAQ

1.1 Summary

This chapter summarizes the SoLID DAQ pre-R&D activities for the fifth quarter, from April, 2021 to July, 2021.

The five main tasks (A-E) are:

- A) GEM VMM3 readout high rate testing to determine trigger rate capability, behavior with pile-up, and readout performance

Milestone	Objectives	Expected Completion Date	Status	Updated Date
A1	Finish development of VMM3 direct readout	May 1, 2020	Complete Q2	
A2	High rate testing with detector	August 1st 2021	80% complete	November 1st, 2021
A3	Optimized VMM3 setup for maximum data rate	July 1st,2021	90% complete	October 1st, 2021

In order to use a larger number of channels (256 per board) which will be available after the completion of the prototype board being designed for milestone A3. Thus we plan to complete milestone A2 after A3. Milestone A1 was completed with only the 12 channels that were available with the evaluation board. Milestone A3 was delayed due to the need for a few iterations of the filtering design of the VMM3 based on reviews of the design by Gianluigi De Geronimo and Georges Iakovidis. We note that we will run with the highest gain setting of VMM3, which is more sensitive to noise. The prototype board was delayed by about 1 month because of some issues with the testing setup as explained below. The prototype board will be sent for production in September.

- B) GEM APV25 readout high rate testing: show that 100 kHz trigger rate is achievable with existing readout hardware developed for SuperBigBite (SBS).

Milestone	Objectives	Expected Completion Date	Status
B1	Finish development of fast APV25 readout	November 1, 2020	Complete Q2
B2	Determine maximum rate achievable with APV25	March 15, 2021	Complete Q3

- C) FADC developments for fast readout and triggering

Milestone	Objectives	Expected Completion Date	Status	Updated Date
C1	Development of FADC readout through VXS	November 1, 2020	Complete Q4	
C2	Testing PVDIS trigger functionalities and rate capability	August 1, 2021	90% complete	October 1,2021
C3	PVDIS trigger test with two sectors	July 15, 2021	on-going	November 1, 2021
C4	Test SIDIS trigger	August 15, 2021	on-going	October 1, 2021

Calorimeter trigger firmware was implemented and is being tested. Dead time measurement were carried out with the regular VME readout. The fast FADC readout is being implemented for the evaluation of the dead-time. Hardware for C3 and C4 is being gathered for testing in September.

- D) Test of gas Cherenkov readout with analog sums and MAROC chip

Milestone	Objectives	Expected Completion Date	Status	Updated Date
D1	Setup FADC crate for Cherenkov simple sum testing	February 15, 2020	Complete Q1	
D2	Record beam data using simple sum and FADC	September 15, 2020	Complete Q1	
D3	Record data using MAROC sum readout	Oct 15, 2020	90% complete	October 15, 2021

A test bench for testing the MAROC along with FADC readout was setup. Data with LED and laser were taken. Testing with cosmic rays is on-going.

- E) Time of flight using the NALU sampling chip

Milestone	Objectives	Expected Completion Date	Status	Updated Date
E1	Acquire and setup ASOC evaluation board	April 15, 2020	Complete Q3	
E2	Acquire data of scintillator	October 15, 2020	Complete Q4	
E3	Complete analysis and determine achieved timing resolution with ASOC and compare to FADC resolution	August 15, 2021	20%	October 15, 2021

Data were taken with cosmics and with radioactive source. Analysis software is being developed for analysis of the data from the custom NALU software.

First two milestones were completed, the remaining one consists of data analysis and testing of the performance of the system with the new firmware and hardware developments.

1.2 Detailed reports

1.2.1 GEM testing

A) VMM3 We are studying the behavior of the VMM3 with high background and are determining the maximum trigger rate that can be achieved.

A3: Prototype front-end board – The module supports 128 VMM3 channels and mounts on a GEM detector with a high-pin count connector. Power delivery to the prototype module is through a pair of power mezzanine cards that mount on the underside of the module (Figure 2). This approach has several advantages. We can design the initial power system using commercial grade components that are inexpensive and readily available. Different powering schemes can be tried during testing. Once the prototype is fully operational, the transition can be made to radiation tolerant power components that are required for the final implementation. No modifications to the prototype module have to be made when changing powering schemes. The design of the two commercial grade power mezzanine printed circuit boards has been completed. One mezzanine card supplies power to the pair of VMM chips.

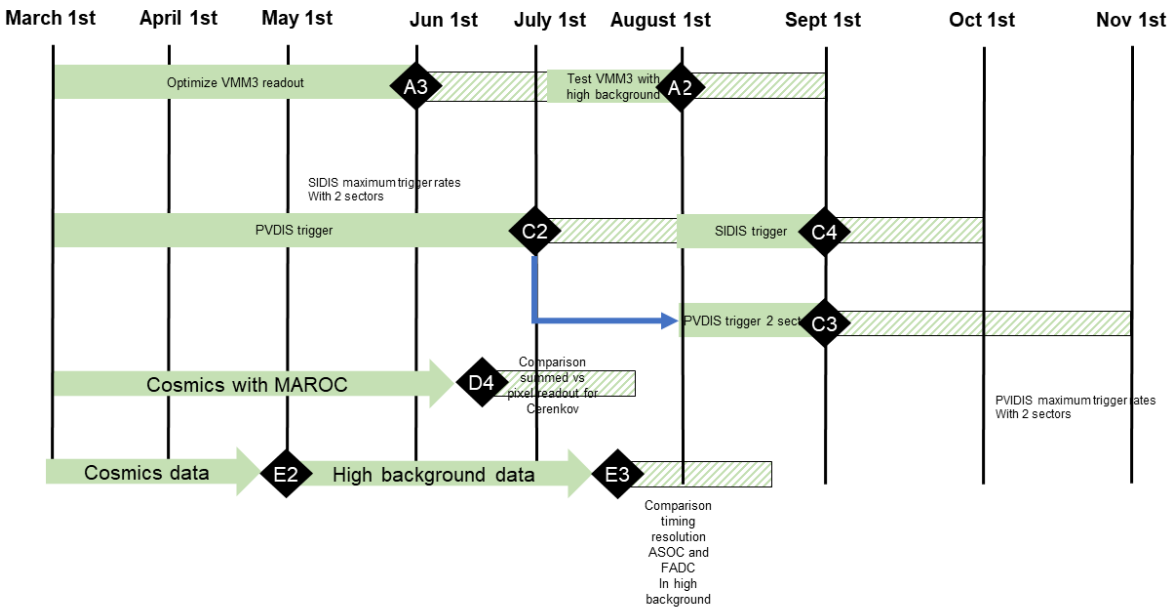

Figure 1: SoLID Pre-R&D for DAQ timeline, March 2020-November 2021 (hashed boxes are for the float)

Very low noise linear regulators are utilized in this application. The second mezzanine card powers the FPGA and all the data transport components. Because the current demands are greater, low noise switching regulators are used. Extensive simulations of the full FPGA firmware at the expected high data rates of SoLID were performed. This gave us reliable estimates of the power required by the multiple FPGA power rails in this application. The power estimates were scaled by a factor of 3 to account for the Triple Modular Redundancy techniques we will employ in the future to mitigate against logic upsets due to radiation exposure. We are preparing to have these two mezzanine cards fabricated and assembled in the next several weeks. The printed circuit board design of the base prototype module is now 90% complete. To obtain lowest possible noise levels can be achieved we are especially concentrating on the layout of the power filtering components that are in close proximity to the VMM chips. On this topic we are actively communicating with the ATLAS group. They have successfully designed several boards that use the VMM chip. Components for the prototype and mezzanine circuit boards are either already in hand or will be delivered over the next few weeks. A board for testing the VMM chips was loaned to us by CERN ATLAS collaborator and chip were tested and all the chip failed the pulser part of the test. We shipped the board back with 20 of chips to be tested at CERN, since we suspect an issue with test board. Production of the prototype board will start when the chips are validated and sent back.

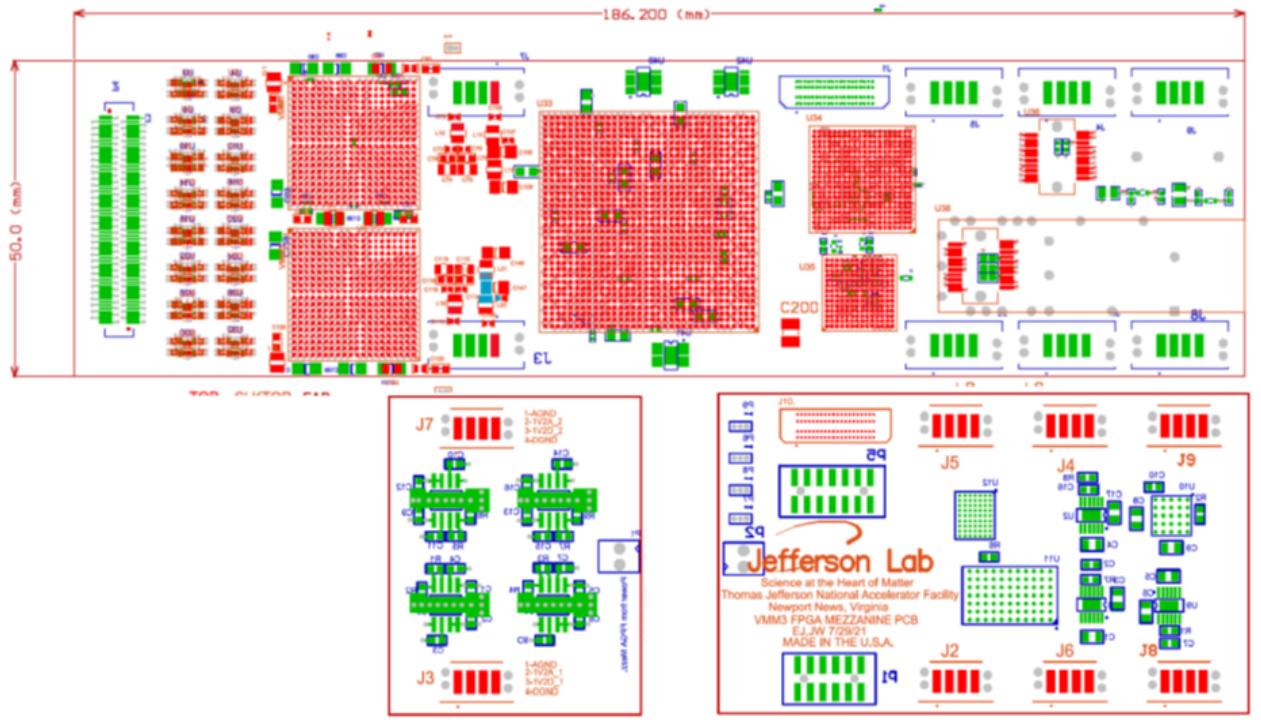

Figure 2: VMM prototype board (top) with dual power mezzanine cards

A2: Final test will use the prototype board with the X-ray setup in UVA to evaluate the performance of the chip in a high background environment.

1.2.2 DAQ test stand and rate tests

C2: Calorimeter trigger The SoLID calorimeter trigger is based on the sum of one central block surrounded by 6 adjacent blocks. A trigger is issued from the calorimeter when a sum of 6+1 is above a given threshold.

The ECAL clustering firmware was completed using Vivado HLS C++ and verified with C/C++ simulation source materials. HLS produced VHDL sources that were compiled into the VTP where other supporting firmware was in place to route trigger data from FADC250 modules and also send the trigger decision from the clustering code to the front panel for trigger the whole DAQ. The FPGA utilization was pretty low allowing for plenty of room to support the 2 sector trigger and expands requirements if needed. Results for the compile are shown in Fig.3

Additional diagnostics having been implemented where the VTP records trigger clusters to the data stream. This is has been tested uo to 30 KHz which is expected PVDIS trigger and allows offline analysis to perform a direct check on the correctness of the trigger. Trigger latency is 500ns, with a timing resolution of 4ns. Higher rate tests up to 200 KHz will be done for the SIDIS trigger test C4. The scheme is expected to work up to 30 MHz of input

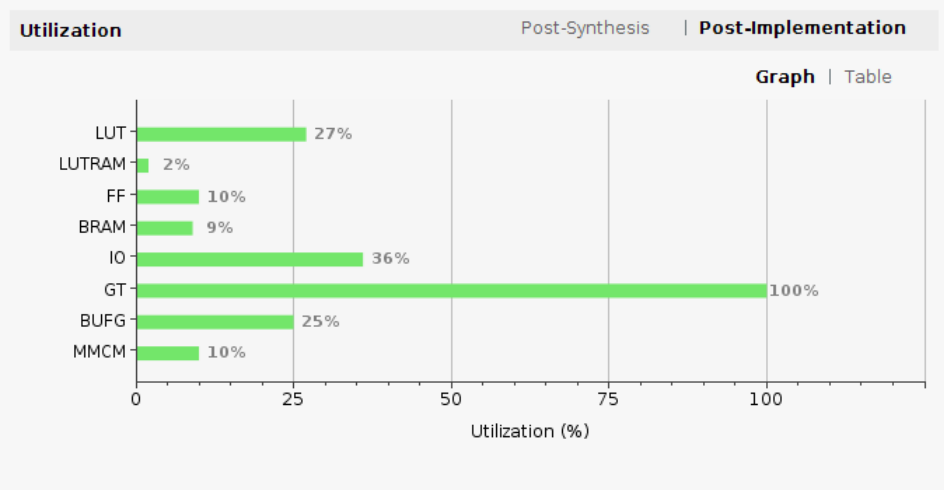

Figure 3: VTP FPGA compilation resources showing timing is met and plenty of margin remains for changes/improvements if needed (LUT (Look Up Table)=27%, FF(Flip-Flops)=10% are the important resources).

rate

C2: Dead time and asymmetry studies Two ways are used to test the ability of FADC to measure small asymmetries at high event rate up to 200 KHz. The first way is to use a pulse generator and a helicity board. The circuits design is shown in Fig.4.

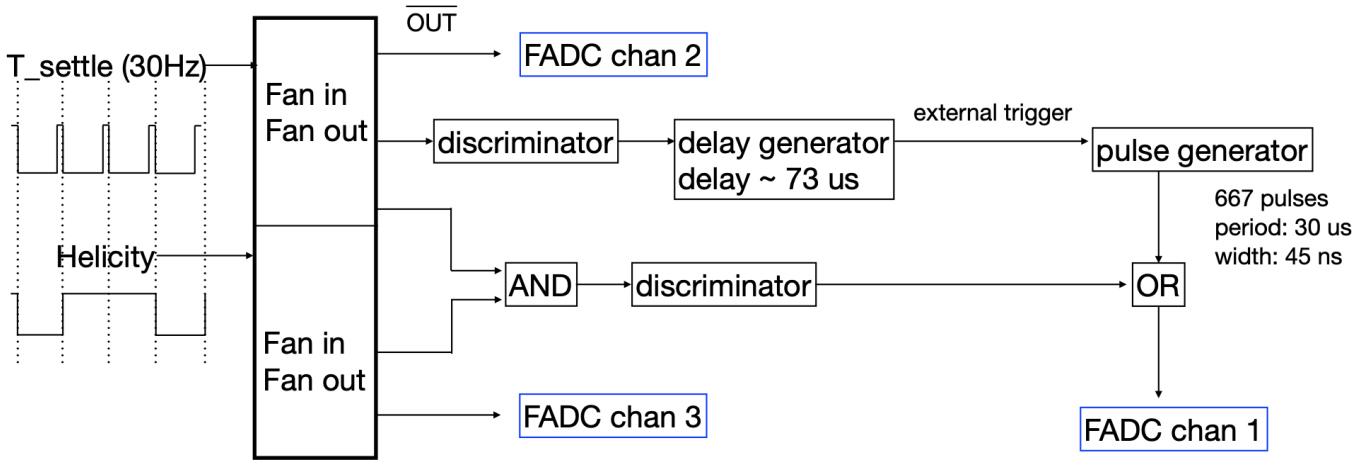

Figure 4: The layout of the fixed pulser asymmetry measurement.

The "T_settle" signal marks the beginning of each helicity window, and it is used as an external trigger to the pulse generator, which will generate 667 pulses when an external trigger is received. The "Helicity" signal from the helicity board is set up to be a 30 Hz quad pattern (+ - - + or - + + -), and it is passed through a discriminator, so a logic "OR" is

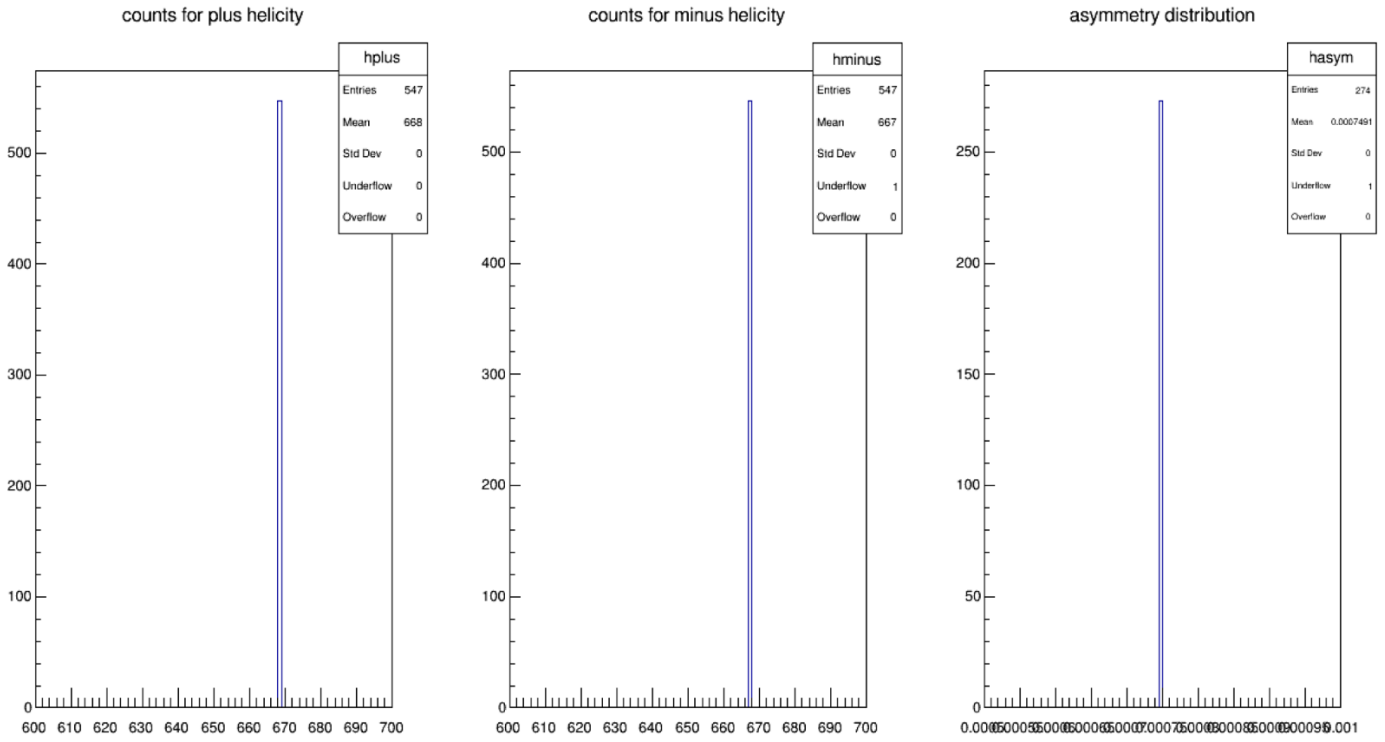

Figure 5: The results of the fixed pulser asymmetry measurement. Left: the distribution of the number of events in the positive helicity window; Middle: the distribution of the number of events in the negative helicity window; Right: the distribution of the asymmetry calculated per quad pattern in FADC.

done between the discriminated "Helicity" and the pulse generator output. As a result, in positive (+) helicity, there are 668 pulses, while in negative (-) helicity, there are 667 pulses. The designed asymmetry is 749 ppm with event rate around 20 kHz, which is the situation of PVDIS.

The number of events per helicity window recorded by FADC is counted, and the distribution is shown in Fig.5. The results are as expected. The asymmetry is calculated for each quad as $(N_+ - N_-)/(N_+ + N_-)$, where N_+ is the total number of events from the two positive helicity windows, and N_- is the total number of events from the two negative helicity windows. The distribution of the asymmetry measured by FADC is shown in Fig.5, and it's exactly equal to the designed value.

The second way to generate an asymmetry is to use a customized voltage generating module and a commercial V-to-F module. We hope in this way we will have an asymmetry generated from random pulses. The layout of the design is shown in Fig.6. The HAPPEX timing board is a JLab customized board that can generate voltage from -5V to 5 V with steps using 16 bits. Two HAPPEX timing board are used to generate two different voltages around 200 mV, and are sent to the V-to-F. The V-to-F module is a commercial module,

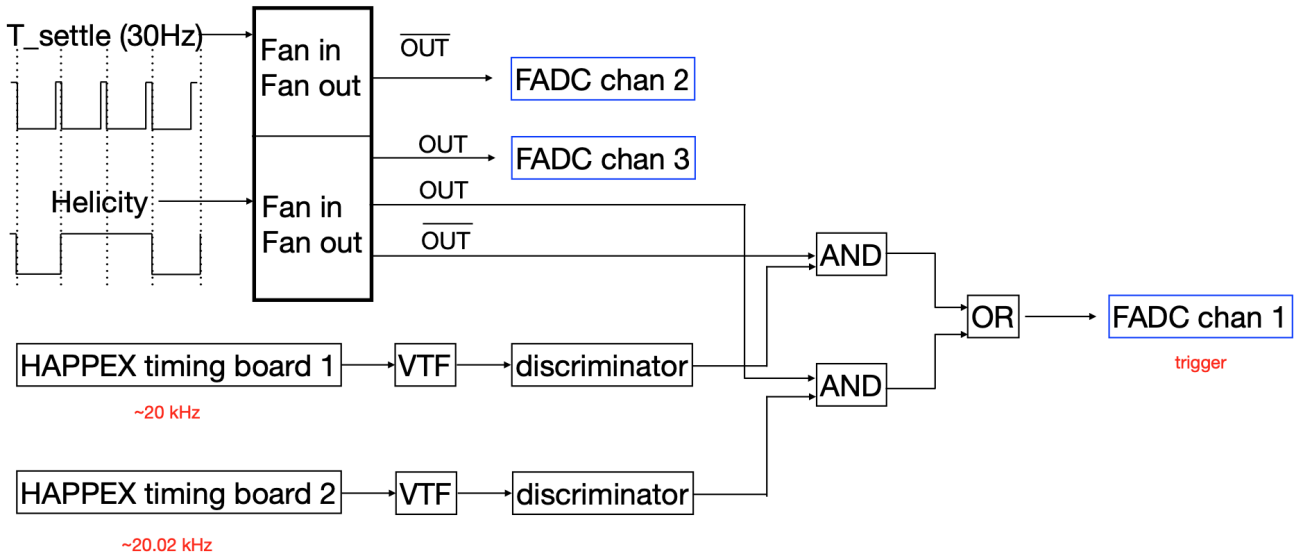

Figure 6: The layout of the "random" pulser asymmetry measurement.

where 1 V corresponds to 100 kHz output. As the output from the HAPPEX timing board could fluctuate a little bit, so as the V-to-F module, the asymmetry generated should be more "random" than using the pulse generator. The number of events per helicity window are counted both using FADC and scalers in VTP. The difference between the two numbers divided by the scaler counts are the FADC dead time. The distributions of the number of events per helicity window and the dead time are shown in Fig.7. A small dead time (<1%) is observed. The distributions of the asymmetry per quad calculated using FADC and scaler are shown in Fig.8. The asymmetry is sensitive to dead time, but since most quads don't have a dead time, the mean of the asymmetry distribution from FADC is very close to that of scaler. This can also be seen in the plot of the difference between the asymmetries measured by FADC and scaler, which is centered at 0.

One reason that there is a dead time in FADC could be due to the output from the V-to-F module are not clean TTL signals, as shown in Fig.11. The blue line in Fig.9 is the original output from the V-to-F module. I intended to pass it through a TTL-NIM translator, but the translator considers it as two pulses instead of one because of the small drop in front of the main signal. Instead, I passed it through a discriminator, which is only able to discriminate the small drop, but it is not the main signal. The V-to-F module has been sent back to the company for repair. We may get better asymmetry measurement results with the repaired module and with the FADC fast readout implemented in the near future.

The fast FADC readout will be implemented at UMass and deadtime will be evaluated with the same setup to show improvements from the faster readout.

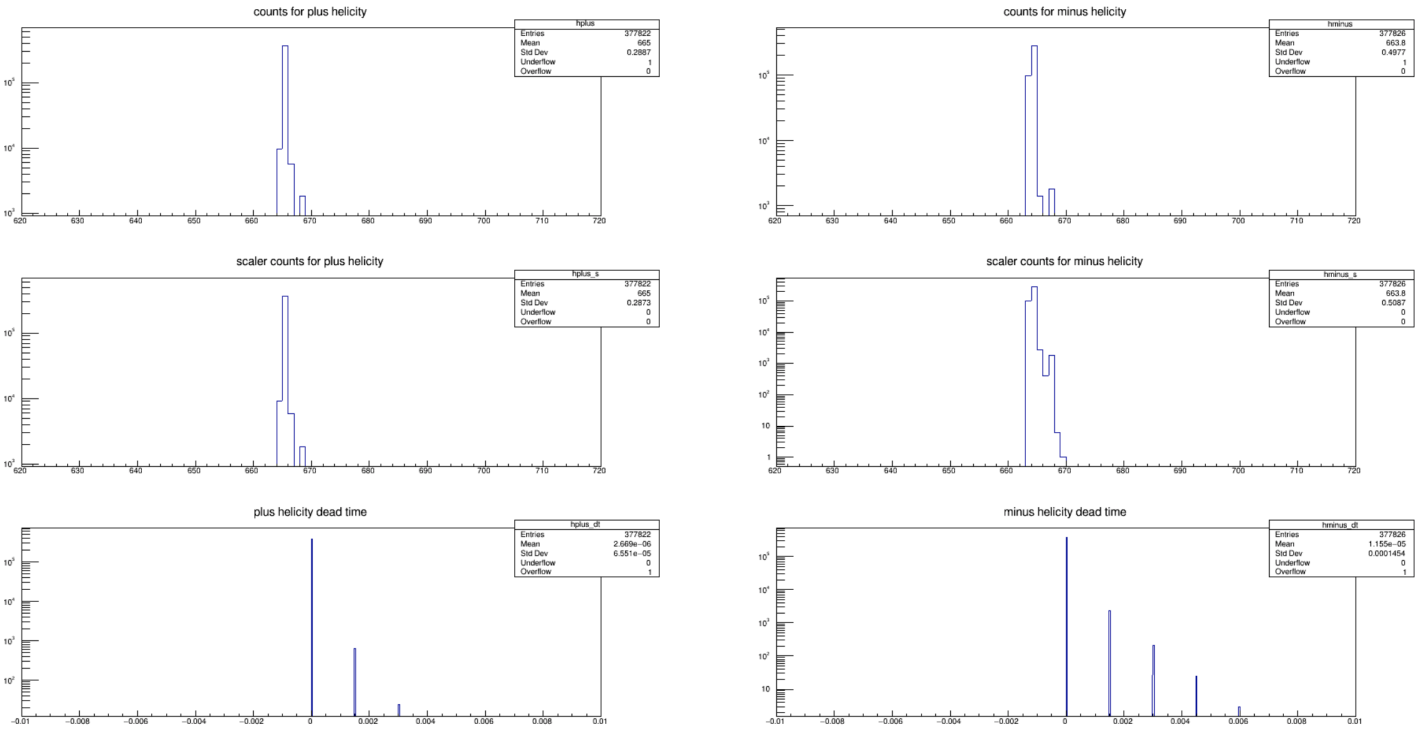

Figure 7: The distributions of the number of events and dead time per helicity window.

C3 : PVDIS trigger test with two crates Hardware for testing is setup, firmware work is starting

C4 : SIDIS trigger test The SIDIS trigger requires the PVDIS calorimeter trigger for the electron trigger. The system will be setup in parallel of the PVDIS trigger with several crates.

D) Cherenkov readout D3: The MAROC sum electronics were delivered from INFN and are ready for a beam test. Due to a lack of available beam time, the beam test of the MAROC sum electronics was cancelled. We are continuing bench testing using LED, laser, and cosmic rays. We finished the laser and LED test this quarter and the cosmic ray test is ongoing. Some issues with noise and the radiator had to be addressed, more details are in the Cherenkov section 2.5.

E) Time of flight The current baseline readout of the TOF is based on the FADC250 with at 250 MHz sampling rate with a target goal of 100 ps timing resolution. The ASOC chip has a sampling rate from 2.4 to 3.2 GHz. We are evaluating the benefit of higher sampling rate on timing resolution in a high background environment.

E1: Completed in the first quarter.

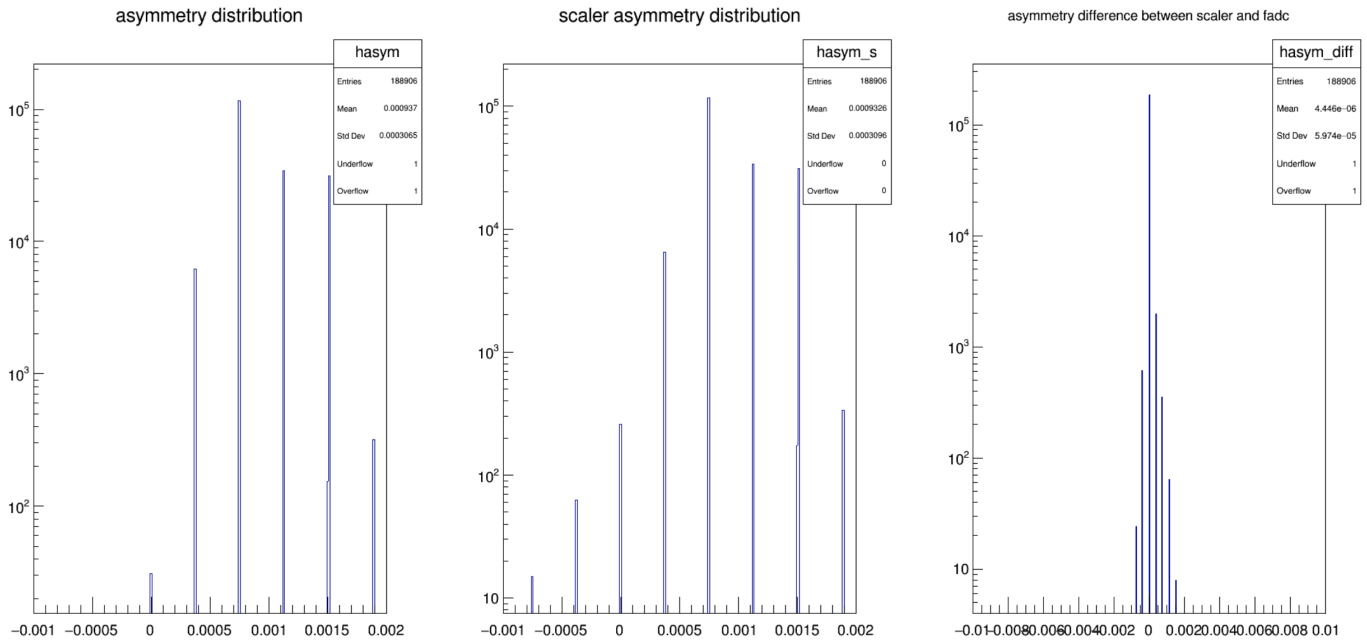

Figure 8: The distributions of the asymmetry per quad measured by FADC and scaler, and their difference.

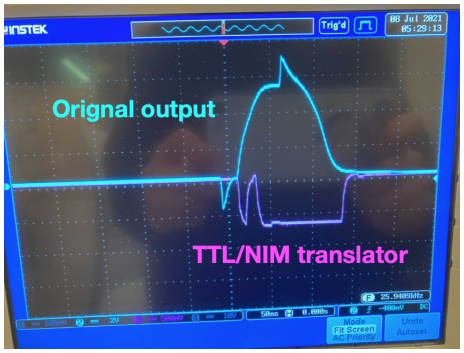

Figure 9: The original output from V-to-F module and it passes through a TTL/NIM translator.

E2: Complete Cosmics data was taken with scintillator with custom NALU software. Figure 12 shows a signal from cosmics in the scintillator.

Figure 10: The original output from V-to-F module and it passes through a discriminator.

Figure 11: Output of V-to-F module.

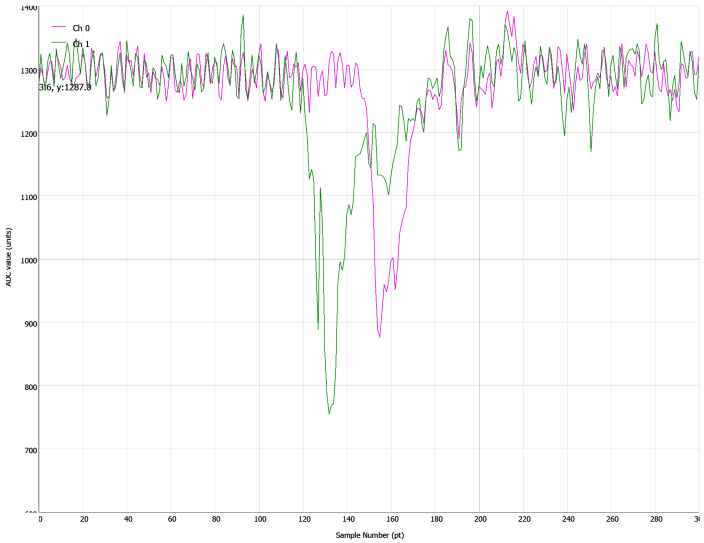

Figure 12: Example of cosmics pulse with scintillator recorded with ASOC

E3: Software is being developed for analysis the NALU DAQ data combined with other detectors for timing resolution determination.

1.3 Budget / spending summary / procurement

System	Cost ($)	Number	Total	Spent
VXS crate for DAQ modules	15,000	2	30,000	32,388
VTP - Module for triggering and data movement	10,000	2	20,000	17,050
SSP	6,500	1	6,500	0
TI - Trigger Interface	3,000	2	6,000	0
SD - Signal Distribution card	2,500	2	5,000	1,250
FADC trigger distribution card	2,000	2	4,000	4000
VME CPU	4,500	2	9,000	11,000
Trigger Supervisor	3,500	1	3,500	0
Hardware components for VMM readout test stand	25,000	1	25,000	36,000
APV25 GEM system	23,000	1	23,000	14,680
Cables/patch	400	160	64,000	42,000
Optical fibers	100	20	2,000	2,000
MAROC eval board	23,000	1	23,000	0
ASOC eval board	10,000	1	10,000	8000
Optical transceivers	50	32	1600	1600
Total M/S direct			210,600	169,968
Total request M/S			227,300	181,611
Workforce 2020	$130,000$	1.25	162,500	90,000
Workforce 2021	$133,900	1	133,900	203,518
Contract DG electronics	78,250	1	78,250	78,250

Table 1: Budget summary

Main expenses were for the VMM prototype board which is also ending up more expensive to meet the deadline because of the FPGA shortage this year. Cables for PVDIS calorimeter trigger tests were ordered. A modified MPD board was designed to increase the maximum data rate of APV readout by a factor of 2 and was ordered.

	Budget ($)	Obligated ($)
Material	227,300	181,611
Personel	372,700	371,768
Total	600,000	553,379

Table 2: Budgeted and obligated funds summary (includes overhead)

2 High Rate Test of MaPMT Array and LAPPD Using a Telescopic Cherenkov Device

2.1 Summary

This quarter, comparisons between the expected/simulated MaPMT signal and the parasitically collected data for low-rate running show a similar signal pattern over the 64 quadrant detection plane. These comparisons allow us to parameterize our simulations to better provide a more realistic response for full SoLID simulations which is a primary goal of this pre-R&D effort. Additionally, progress has been made on the bench-testing of the MaPMTs with the MAROC sum readout. After determining the signal could be cleaned by isolating the low voltage connections, and increasing the thickness of the lucite radiator, clear Cherenkov partial-rings can be identified by eye. Progress is underway to collect more cosmic data and develop algorithms to digitally detect partial-rings. These rings are analyzed in the presence of bench-simulated backgrounds (LED light), which mimic the structure of random particle backgrounds expected during SoLID high-rate production running. This test will provide information on the efficiency and reliability of signal/background separation using the pixelized digital MAROC readout in conjunction with ring-finding algorithms. This project has one remaining milestone (milestone 4), which was originally moved from parasitic beam testing to bench testing due to time constraints of the accelerator and experimental hall. This milestone is now expected to be completed by the following quarter (Nov 2021) which is in-line with the completion deadline of the entire pre-R&D project.

2.2 Project Milestones

Milestone	Objectives	Expected Completion Date	Status
1	Construction and delivery of Cherenkov tank to Jefferson Lab.	Early January 2020	Complete (Q1)
2	Cosmic testing and installation into experimental hall.	Mid February 2020	Complete (Q1)
3	Collection and analysis of low and high rate data with electronic summing-board.	End of Year 2020 (+2 Month Contingency)	Collection complete (Q2), Analysis completed (Q4).
4	Collection and analysis of high rate data with MAROC electronics.	(Modified) Quarter 6	Moved to bench and nearing completion.

2.3 Budget and expense summary

Category	Budget	Expenses Q1	Q2	Q3	Q4	Q5
Material	$210,000	$124,736	$84,414	$3,311	($228.64)	$ 0
Personnel	$240,000	$31,376	$27,411	$26,882	$47,915	$ 42,061
Travel	0	0	0	$5,295	$3,509	$ 5,048
Total	$450,000	$156,112	$111,825	$35,488	$51,195	$ 47,109

Table 3: Budget and expenditures summary from both Temple and Duke for the Cherenkov prototype (includes overhead)

To date funds have been used to purchase all the materials to construct the Cherenkov prototype tank with pressure controls, all connectors and cables for reading out signals of 64 channels from MaPMTs or LAPPD, mirror, MaPMTs, wavelength shifter coating, radiator gas, MAROC readout boards and their cabling. Funds have been used for the mechanical engineering design and machining as well as electrical engineering support, travel and transport of the prototype from Duke and Temple to Jefferson Lab, and the research personnel support for the approved activities at Duke and Temple.

2.4 Analysis and Simulation

In this quarter, we focused on improving the simulation with comparison studies between the simulation results and the experimental data. The geometrical distribution of the signals were studied and compared with the simulation. In this study, the large angle MAPMT test data were analyzed and the signals were selected by a geometrical cut on the central calorimeter block and timing cuts on the signal timing relative to the trigger timing. These cuts have been described in the previous quarterly report. The peak heights of the 64 quadrant channels of the MAPMTs are normalized to the single photo-electron signal amplitude in order to extract the number of photo-electrons (NPEs) per signal. NPEs are then integrated over the large angle test run and shown in the top plot of Fig. 13. The data shows a small shift of the signal center to the left of the geometrical center and slightly wider distribution, comparing to the simulation in the bottom plot. Without a tracking detector, those could to be due to the imperfect alignment of the TCD at 5.5m away from the target and acceptance effects from the support structure. Overall, the simulation describes the size and shape of the data distribution well.

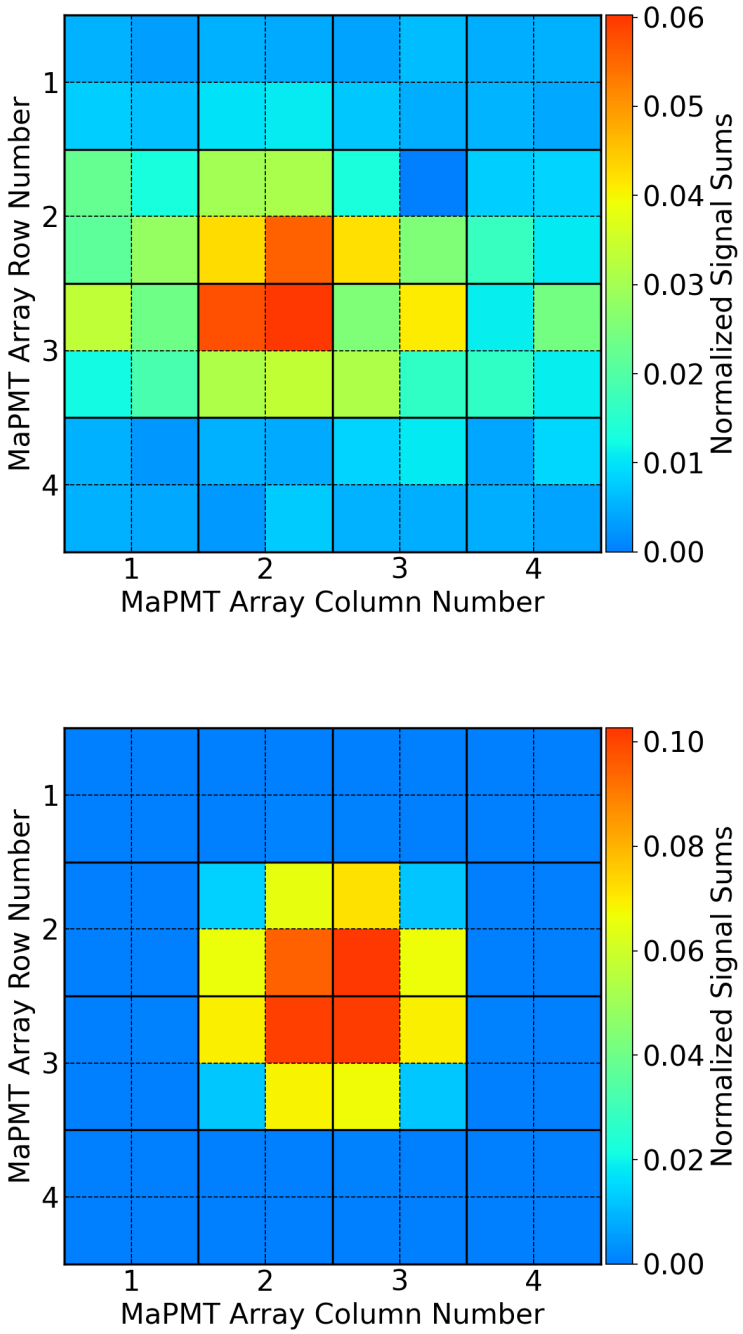

Figure 13: Geometrical distribution of the signals (integrated NPEs over the run) from the large-angle test data (top) and simulation (bottom). 16 MaPMT sensors are shown in a 4 by 4 array in accordance to the front view of the geometrical layout. Quadrant channels are separated by dash lines. A geometrical cut selecting the center calorimeter block and timing cuts described in the previous quarterly report were applied to the experimental data. In general, the simulation describes well the size and shape of the data distribution.

2.5 MaPMT with MAROC sum readout bench test

Comparing to the simple sum readout used during the beam test which provides quad and total sum signals, MAROC sum readout provides pixel information in additional to quad and total sum signals and can be very useful for background suppression at high rate environment. After the high rate bench test of the MAROC sum electronics mentioned in the last quarterly report, we started a cosmic test using lucite as a radiator to examine how the entire system behaves with real Cherenkov signals. To observe the Cherenkov ring we used an array of 15 MaPMTs. Each MAROC board (combination of one ASIC, one sum, and one FPGA) reads 3 MaPMTs. In total 5 sets of MAROC boards were used to read 15 MaPMTs. The array is arranged in 4 x 4 format with the top right corner missing due to the limitation of the 3-MAPPMT readout board form factor. This is not a problem for the future application as we can use some 2-MAPPMT readout boards.

2.5.1 sum signal oscillation reduction

The sum and FPGA boards in each set of MAROC boards are powered by one low voltage (LV) cable. We found a huge oscillation in the quad and total sum signals through FADC when all 5 sets of boards were powered at once. Figure 14 shows an example of FADC total sum signal oscillation for a pedestal run. We did not observe any oscillation during the high rate test where we had used one set of MAROC board to read one MaPMT.

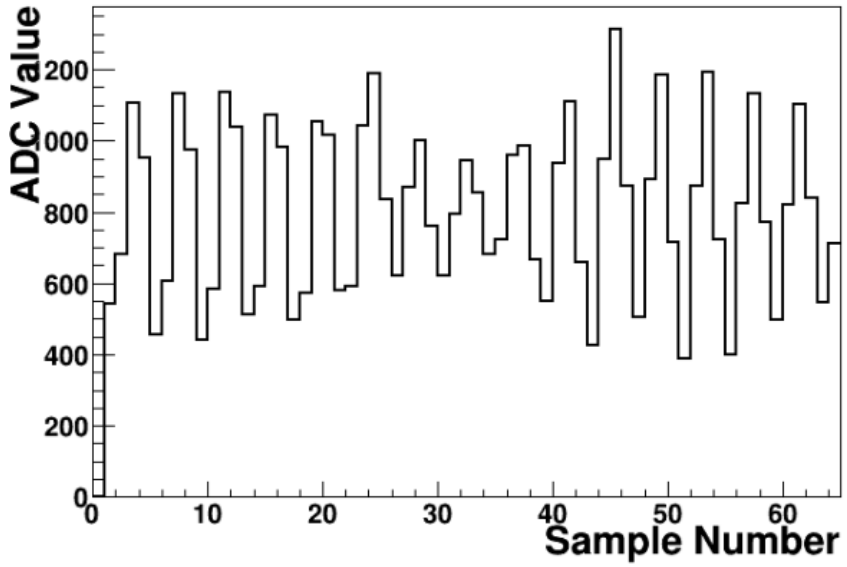

Figure 14: FADC waveform of one of the total sum signals for a pedestal run. Due to the cross-talk between the boards, the pedestal was highly unpredictable.

The origin of oscillation was found to be from the sum board mainly due to the coupling of LV between boards. To reduce the oscillation, we modified the MAROC boards with the

help of the JLab fast electronics group. First, we separated the LV connector to FPGA and sum board. Second, a voltage regulator was added to the sum board. These modifications helped to reduce the pedestal width by a factor of 5 and Figure 15 shows the width of the pedestal after modifications. With the modification of the sum board, the width of the pedestals are comparable to that one we had with one set of MAROC boards.

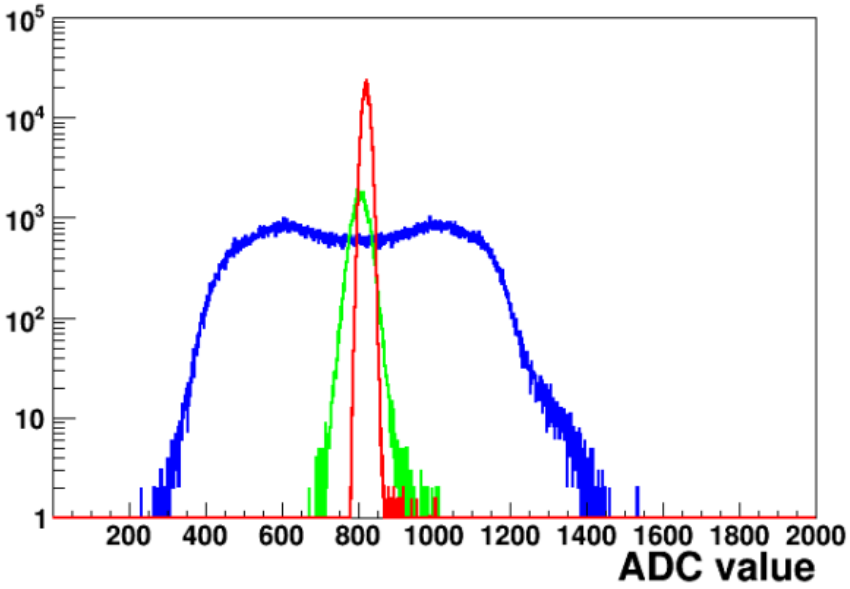

Figure 15: Comparison of the total sum FADC pedestal before and after the modification of the boards. The red histogram is with one set in use. The blue and green histograms are with 5 MAROC board powered at once before and after the modification of the sum board respectively.

2.5.2 Cosmic test

We are performing a cosmic test using lucite as a radiator. As the cosmic muon passes through the lucite, refractive index (μ) of 1.5, the Cherenkov light is emitted. The opening angle of Cherenkov light (θ_{cone}) is 48.19° and the critical angle for total internal reflection is 41.8°

As the $\theta_{cone} > \theta_c$, the Cherenkov photons suffer total internal reflection from lucite surface for an angle of incidence less than 6°. For lucite radiator, only inclined muon can form a ring and due to total internal reflection only a partial ring is observed. In order to take the advantage of vertical muon flux, the lucite is tilted at an angle 12° as shown in Figure 16. In the current setting, the angular acceptance of muon is ± 6° within the vertical direction. Due to the total internal reflection from the lucite surface and MAPMT array size, only about half of triggered events can form a ring. The Cherenkov light produced by the inclined muon incident on one side of the vertical line represented by the red line in Figure 16 would mostly

miss the MAPMTs. With 4 cm thick lucite, we expected around 15 photo-electrons in a partial ring considering the quantum efficiency and transmittance of lucite for Cherenkov light.

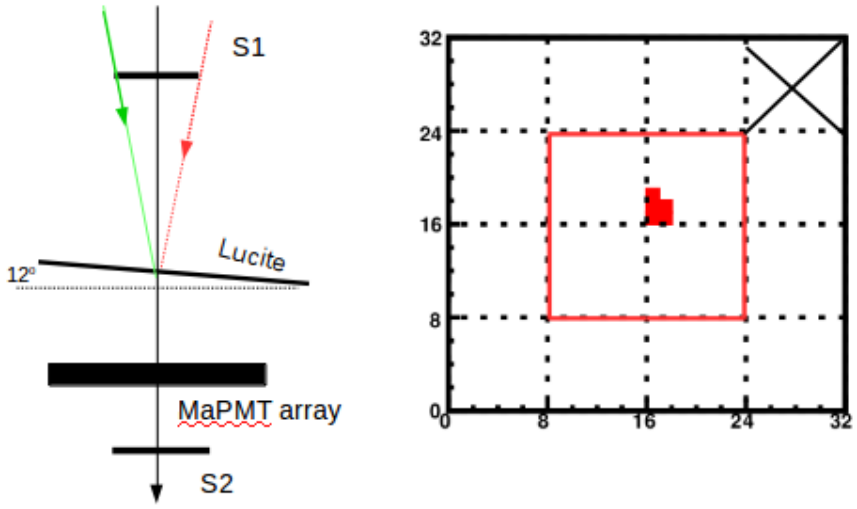

Figure 16: Left: Schematic layout for cosmic test. Two scintillators, one at the top and another at bottom of the PMT array form a trigger. Lucite is tilted at an angle 12° with horizontal. The red and the green lines represent the extreme of scintillator acceptance. Due to the total internal reflection and the limited size of MaPMTs array, only about the half of the triggered events form the partial ring. Right: The 15 PMTs array of dimension $\sim$ 20 x 20 cm is used to detect the Cherenkov ring. The cosmic muon can hit any of the central 4 PMTs represented by the red rectangular box.

The trigger is formed by two scintillators in coincidence placed at the top and bottom of the PMT surface. Figure 17 shows two scintillators in coincidence for a cosmic trigger. In order to well constrain both the position and angular distribution of incident muon the small size scintillators with an overlapping area of about 5 x 5 cm^2 is used. The Cherenkov light emitted is detected using an array of 15 MaPMTs. Each PMT is $\sim$ 5 x 5 cm in dimension, forming the dimension of the PMT array $\sim$ 20 x 20 cm. Figure 18 shows some potential rings for 6 randomly selected events. The dashed arc is drawn to show the potential ring. For about half of triggered the Cherenkov ring can not be observed due to total internal reflection. The cluster at central PMTs represents a comic muon hit.

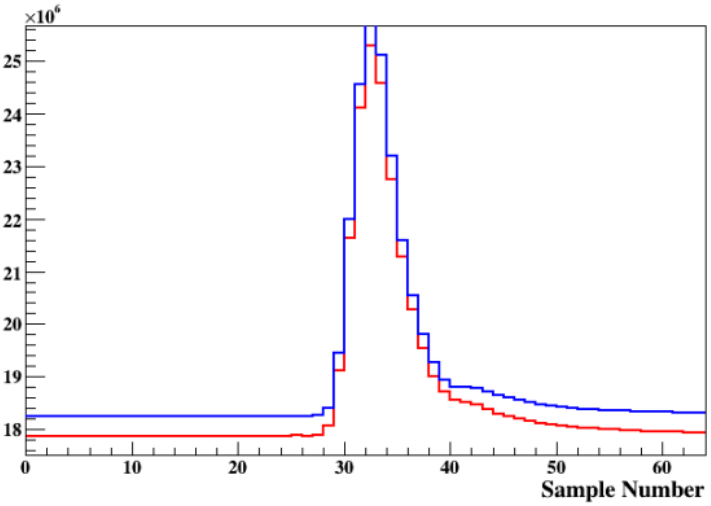

Figure 17: The FADC waveform for two scintillators in coincidence forming the cosmic trigger. The red and blue histograms show the scintillators signal for 64 samples each of 4 ns for the top and bottom scintillator respectively.

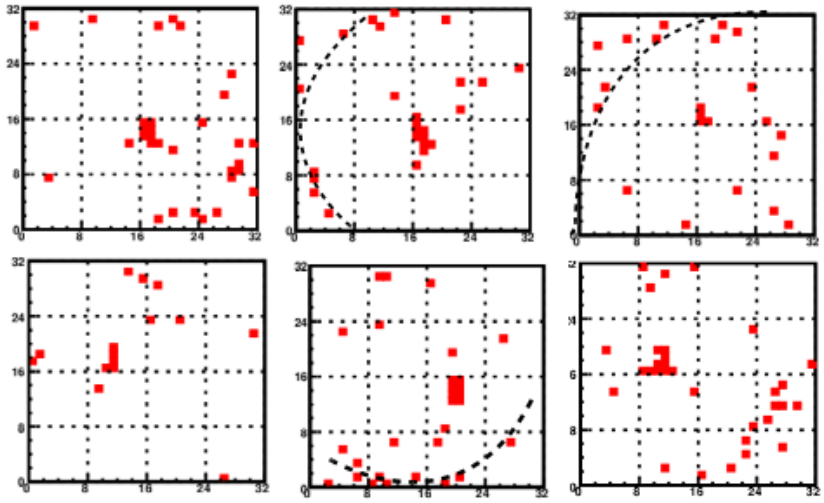

Figure 18: The X and Y positions of pixel for 6 different randomly selected events. The cluster represents the muon hit and the potential partial ring is highlighted by the dashed curve. About half of triggered events form the partial ring. In this setup, rings are expected mostly on left half of the PMT array.

One of the main goals of the cosmic test is to utilize the spatial information to identify Cherenkov rings and suppress background. We have collected enough pure cosmic data as shown above. For the next step, we plan to add a continuous random background created by a LED powered by a continuous DC voltage while taking cosmic data. Then we will analyze

the cosmic data using ring finding algorithms to identify the Cherenkov rings for both cases with and without background. We expect to finish the cosmic data taking and have some analysis done by the next quarter.